FEBRUARY 24, 1981

ISSCC: YESTERDAY'S GLITTER TURNS INTO PURE GOLD/138

Military electronics comes under fire for unreliability/104

Plasma etchers line up to meet demands of wafer production/183

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Electronics

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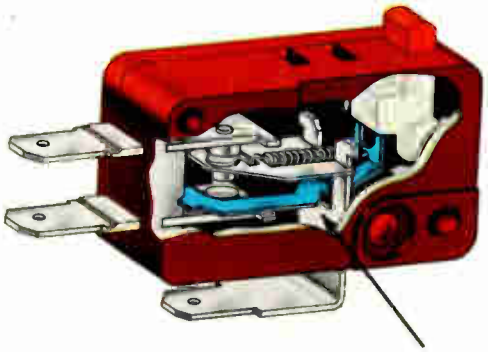

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Circle 2 on reader service card

Electronics
The International Magazine of Electronic Technology
Vol. 4, No. 54 • February 24, 1981

Electronics

Highlights

Cover: 32-bit microprocessor takes up with Ada, 119

Representing dramatic achievements in very large-scale integration, a 32-bit microprocessor called for major changes in most aspects of microcomputer technology, including the development of a high-performance MOS process and a new package with a high pin count. Best of all, it meets the challenge of software-intensive applications by going with Ada as its system implementation problem, making it easier to develop large, modular programs.

The cover illustration is by Art Director Fred Sklenar.

Signature analysis writes a new chapter, 127

An off-board source of stimuli brings the advantages of signature analysis to existing digital, microprocessor-based equipment. The testing technique till now had to be designed into a product but is shown here being retrofitted to a display terminal.

VLSI makes a splash at ISSCC, 138

This year's International Solid State Circuits Conference, held last week in New York, marks the true arrival of very large-scale integration. Perhaps most noteworthy in that regard is the appearance of four 32-bit microprocessors (p. 138). In the memory area, the attention-getters were fast static random-access memories (p. 141). In communications, the focus was on monolithic devices to interface standard analog telephone systems with digital switching or transmission systems (p. 146). For microwave integrated circuits, gallium arsenide is clearly the material of choice, while data converters, low-level operational amplifiers, and power transistors are reaching new levels of performance (p. 150).

Microprocessor family is prepared for VLSI, 157

A new generation of microprocessors, 16 bits wide, is designed to welcome future very large-scale ICs while maintaining software compatibility with members of the earlier 9900 family. The speed needed comes mainly from an extremely fast on-chip memory that can be addressed separately from the main memory.

Plasma etching comes of age, 183

Makers of wafer-etching equipment are turning to dry or plasma etching to achieve the fine lines of large-scale and very large-scale integration. The six upcoming systems described in this Product Roundup show how manufacturers have brought the process variables under control.

And in the next issue . . .

Special report on word processing and office automation . . . a one-knob oscilloscope . . . the third article in a series on speech synthesis . . . marrying electronic mail to word processing.

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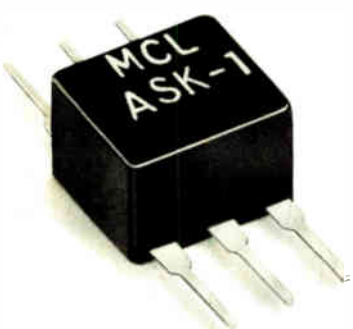

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Circle 5 on reader service card

Publisher's letter

In one of the Gilbert and Sullivan operas a character sings about having a little list. Justin Rattner and William Lattin of Intel Corp.'s Oregon facilities had a little list too.

On it were the things they had to accomplish in order to realize the 32-bit microprocessor that is now labeled iAPX 432. It was quite a list.

"Early on we realized that we couldn't design the 432 with technology then available [early 1975]," recalls Rattner. What neither engineer expected as the project wore on and moved from the Santa Clara headquarters to Aloha, Ore., was the impact that accomplishing the list would have on the company.

First off, the design team devised a new architecture. Next on the list, a new process, turned out to be Intel's high-performance MOS, or H-MOS. The 432 required a new package. Result: the 64-pin quad in-line package, or QUIP. And because the development team was working with basically the same programming methodology that produced the Ada program language, the 432 features one of the first compilers that runs on the Defense Department's standard programming language now gaining commercial acceptance.

Details of the 432 are in the cover article (p. 119) written by Rattner, principal engineer and department manager of the 432 architecture group, and Lattin, general manager of the original-equipment–manufacturer microcomputer systems operation. Microsystems and software editor Colin Johnson edited it.

There were other 32-bit microprocessors featured at this year's International Solid State Circuits Conference. In addition to Intel, Hewlett-Packard described a new six-chip set that features the amazing density of 450,000 transistors on the central processor, and Bell Laboratories had a paper on its latest MAC 32 unit.

These and other new developments unveiled at ISSCC are described in our special report starting on page 138. Colin Johnson organized the report, and he notes that "last year's ISSCC was full of new technology, but this year's topped even that."

There is, for example, a description of Digital Equipment Corp.'s interesting approach to the design of a single-chip version of its popular PDP-11 minicomputer. To execute a minicomputer instruction set, DEC has used only 13,000 transistors on the chip in an effort to get minimum die size. This approach is opposite those that load more and more transistors on ever-larger dice.

As usual, there was also a large representation of Japanese papers.

The push into very large-scale integration is itself pushing integrated-circuit production technology on many fronts. Linda Lowe of the Boston bureau looks at one of these—plasma etching—in the Product Roundup starting on page 183.

"The difficulties in cutting VLSI geometries are enormous," she says, "but so are the spoils for those who succeed."

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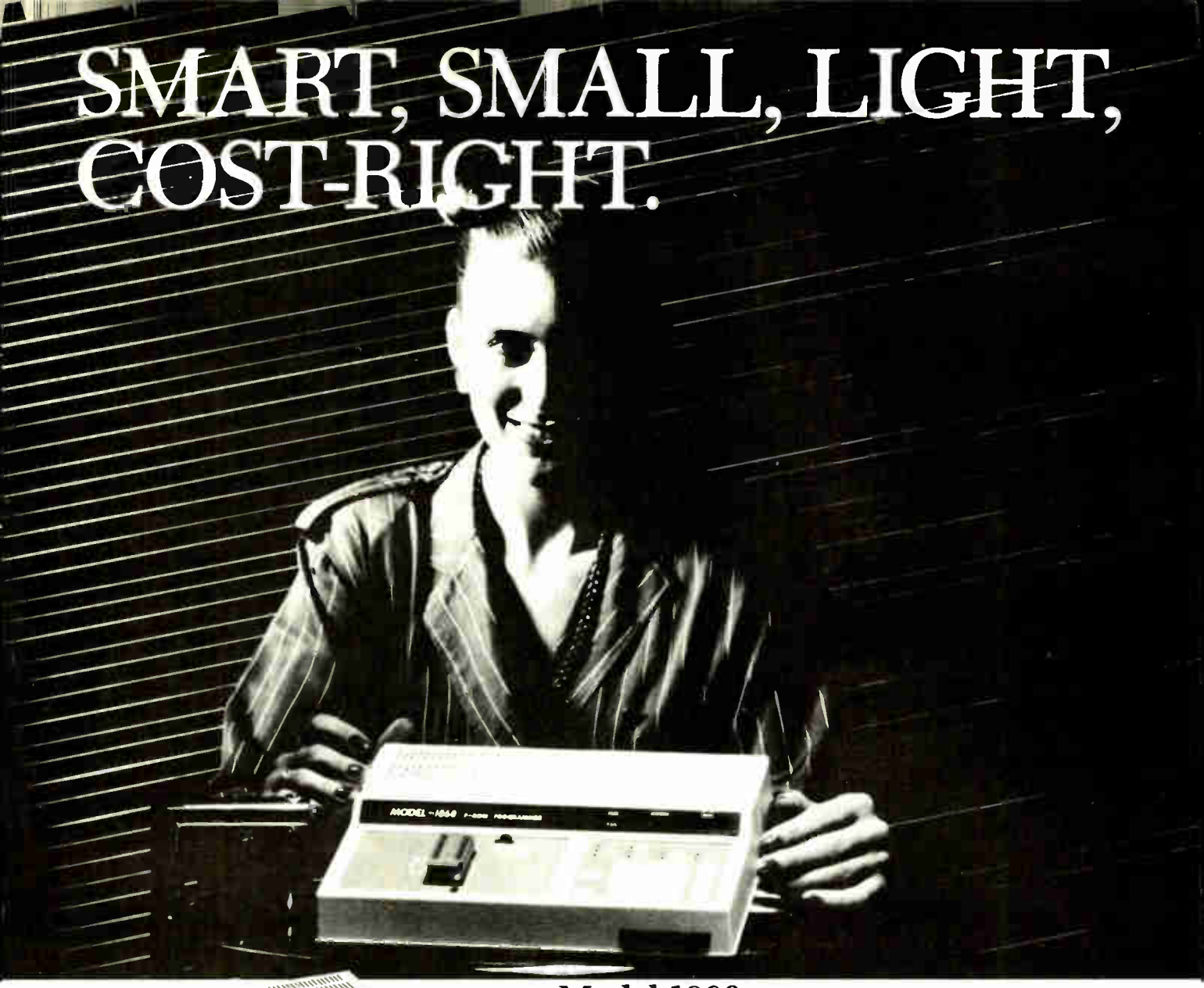

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Circle 7 on reader service card

Readers' comments

What's in an array?

To the Editor: With regard to "Gate arrays: a special report" [Sept. 25, p. 145] and to Frank Deverse's letter about it [Dec. 18, p. 8], I would like to point out that gate arrays are arrays of basic cells, not gates. The basic cell is a configuration of n- and p-channel transistors interconnected and arranged in such a way that they can, at the user's discretion, be further interconnected via metalization to become gates or portions of gates.

Two n-channel and two p-channel transistors can be configured as a two-input NAND gate, so if a cell with these devices is wired for this function, a gate and a cell could be considered synonymous. However, for more complex gates—to perform, say, an AND-OR-INVERT function—several basic cells may be required. The configuration of the basic cell differs from vendor to vendor but is seldom, if ever, a gate equivalent until metalization.

In choosing a vendor, some subtle and some not-so-subtle factors make comparisons of cell configurations misleading. Factors such as levels of customizable interconnection, input/output pin count, speed, loading, power dissipation, percentage of utilization of available cells, and computer-aided design support are more important.

Jim E. Coe
Fujitsu Microelectronics Inc.
Santa Clara, Calif.

Using captive charge

To the Editor: In "Single-slope a-d converter makes a comeback with 20-bit linearity" [Nov. 6, p. 151], the author states that with respect to dielectric absorption, "electrolytic capacitors are the worst." But judging from my own experience, the oil-impregnated types must take the cake. Large oil caps are notorious for spontaneously accumulating a charge, and for this reason large units are shipped with a shorting wire.

In our high school ham shack, we removed a large oil cap from a high-voltage power supply and set it unconnected on the workbench. Each lunch period in the ensuing week or so, we'd go up to the shack and discharge this cap with a satisfying bright blue bang.

The amount of energy that can be stored in the parasitic capacitance is truly prodigious, perhaps hundreds or thousands of times what you'd expect from the textbook formula $Q = CE$. Back in the days of the vacuum tube, I used an oil cap as the bias "battery" for a transmitter rf power-amplifier stage; it would stay charged indefinitely.

In another experiment, I used an 0.1-microfarad oil cap to power a Geiger counter. Once the dielectric had been "set up" by a prolonged charge, it would power the instrument for two hours at ambient radiation levels.

Perhaps if this effect were exploited, a new kind of "battery" could be developed to supply small amounts of power for limited periods—as for the emergency supply of a computer memory, to take only one example.

Dale Hileman
Woodland Hills, Calif.

Corrections

Several errors crept into the description of a novel electrolytic display from France (Jan. 27, p. 82). A gap of 0.2 millimeter, not 2 mm, separates the display's back and front panels, and the back one is coated on the inside with a layer of silver, not silver iodide, that serves as a common electrode. Each active display area requires a single lead, not two, and the display's overall size is limited by voltage drop, not current loss.

In "CHAS seeks title of global CAD system" (Feb 10, p. 100), typographical errors caused the omission of some information. The first full paragraph in column two should read: "Mudge says that, to a degree, the philosophy behind CHAS draws on and extends the approach developed by Carver Mead of the California Institute of Technology and Lynn Conway of Xerox Corp., as well as the bristle-blocks approach of David Johannson. . . . " On page 102, the first sentence in the first full paragraph should end " . . . stations, thus cutting calendar design time."

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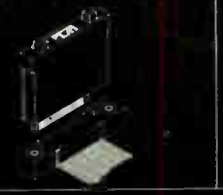

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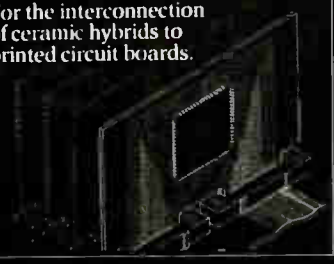

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Getting a start on defense changes

A recent report by the House Armed Services Committee [*Electronics*, Jan. 27, p. 24] paints an ominous picture of a U. S. defense industrial base as not only incapable of providing the "surge capability" vital to a fast upgrading of the military, but in trouble over simply keeping up with today's workload. Actually, it confirms what many leaders in the military, the defense industry, and a few in Congress have warned about since the 1960s and reflects an ongoing effort by prime contractors to put their concerns before Congress.

One of the key conclusions is that suppliers of essential components increasingly opt out of military business for many reasons but chiefly because of low (or no) profits, crushing paperwork, excessive contract changes, and the uncertainties of yearly contract renewal. All in all, this report spells out dismal defense prospects unless basic changes occur.

Now, however, there is a ray of hope in the form of growing efforts intended to make some of the recommendations in the House report happen. Equally encouraging, in John H. Richardson, the defense industry has an effective spokesman able to dramatize the needed changes and their benefits. The energetic president of Hughes Aircraft Co., who has logged some 32 years at top levels of aerospace management, ran through his presentation earlier this month at the 22nd annual Winter Convention on Aerospace and Electronic Systems (Wincon) held in Los Angeles.

Richardson's overall message is simple and hardly controversial anywhere except in defense work: contracting should be based on tested business practices so that planning and execution can take place in a stable manner. His proposal sets out several key requirements, starting with smoother cash flow to prime contractors and thence to their suppliers. That would not necessarily mean higher total payments—merely more and faster payments to keep contractors away from the increasingly expensive bank borrowing that runs up costs.

Closely allied to that is the need for better procurement practices that promote multiyear contracting. Even for systems accepted for production, contracts are in one-year segments, a policy that ties the hands of both prime contractors and their suppliers, preventing the economies of scale attainable in nondefense work. The U. S., by the way, is the only Western nation with such a limitation.

The objective has been to get changes through Congress and into the Pentagon, and although these are only just getting under way, there is a good chance of success. For example, House bill, H. R. 745, introduced on Jan. 6 by Rep. Dan Daniel (D., Va.), proposes amendments to establish more flexible contract procedures, specifically multiyear types. Support for the bill in the House, is growing, according to Richardson. And influential new leaders in the Senate's Republican majority—many from Western states—are taking interest.

Opposition to such changes is bound to arise, largely from middle management levels at the Defense Department who would fear loss of tight control over contracts. And Richardson, for one, though confident about the chances for reforms, is experienced enough in these matters not to expect miracles overnight. Still, quite a bit has happened already. Most of the problems have been identified, hearings have taken place, and a bill has been introduced in the House. Considering that the condition of the defense industry has gone largely unacknowledged for the last decade, that is a lot of progress.

The House report and others such as the one recently released by the General Accounting Office (see p. 104) seem to be the splash of cold water needed to wake up the rest of Washington and get positive action.

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People

Mayhew puts education, safety on the AEA's menu

Things are always stirring around Lawrence L. Mayhew, acclaimed by many as the master chef who came up with the recipe for Tektronix Inc.'s successful penetration into the information displays field. Now operations and marketing group vice president for the Beaverton, Ore., firm, the 47-year-old executive will be cooking on more than one range this year, inasmuch as he is also the newly elected chairman of the American Electronics Association.

Programs. As presiding officer of the prestigious industry trade association, Mayhew is likely to have a hand selecting the programs the AEA presents both to lawmakers in Washington and to industry management. He feels that some of the issues pressed by his predecessors, such as a further reduction of the maximum capital gains tax and enactment of a 25% tax credit for increases in corporate R&D, will make it through Congress.

Thus, Mayhew is focusing his efforts primarily on two new main courses—industry's technical manpower needs and a safer work environment for its employees. He plans to assemble a blue-ribbon panel of industry executives and leading academics who will interact with state legislators and, he states, "perhaps go to the White House for support." He believes the electronics industries are better than most in their support of education, but adds: "There just aren't enough sources of capital," and so "we have to get our industry to change its funding attitude."

What's more, Mayhew says, "we in industry should analyze what contribution we are making to the shortfall in graduating-class size by our snatching away those who might have gone on to graduate school and become professors."

Similarly, Mayhew wants the AEA to "contribute to improving the health and safety environment of employees in our industry" and "not to interfere with the discovery of unsafe working conditions or implementations of laws that prevent health hazards to employees." He feels industry needs to understand the "vagaries and consequences" of such laws.

Industry voice. AEA chairman Mayhew feels U. S. needs new education funding.

A native of Santa Paula, Calif., Mayhew joined Tektronix as a circuit design engineer in 1961, following graduation from California State Polytechnic University with a bachelor's degree in electronics engineering. He was a Navy pilot from 1953 through 1958, but has not flown since. Rather, his "myriad of interests," as he puts it, includes working in an elaborate home workshop, gardening with his wife, and getting his son interested in electronics.

"Sailing is another one of my interests," he recalls. "That's the problem—I have so many things cooking, I sometimes forget one."

Mostek's Quinn carries on leadless carrier crusade

Leadless chip-carriers are due to make their mark in packaging by 1985. But at Mostek Corp., Carrollton, Texas, this compact integrated-circuit package is already finding a place on motherboards that use the carriers to double memory density.

According to Bobby G. Quinn, 49-year-old marketing manager of military high-reliability products at Mostek, the technique of pairing the leadless packages on ceramic moth-

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	RL01 Controller	DLV11-J Serial (4)	RL01 Controller	RX02 Controller
	DLV11-J Serial (4)	OPEN	RL01 Controller	DLV11-J Serial (4)
	OPEN	OPEN	DLV11-J Serial (4)	OPEN
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SS-3

Circle 15 on reader service card.

erboards will lead the way toward solving the No. 1 problem with chip-carriers—how to mount them on printed-circuit boards.

"The benefit is that the product going on the motherboard is the chip-carrier," explains Quinn, who was first sold on the concept while working at Texas Instruments Inc., Dallas. With this approach, the motherboards will be the learning vehicle that will advance chip-carrier technology.

"Right now, I think motherboard products are going to run off and leave the chip-carrier ones behind—in terms of volume," observes Quinn, a recently appointed member of the Joint Electron Device Engineering Council's solid-state panel.

Crusaders. So much does Mostek believe in the interim period of motherboard-mounted chip-carriers that it is considering a wide range of products using side-by-side configurations, including a dual-chip 128-K dynamic random-access memory [*Electronics*, Jan. 27, p. 34]. The 128-K model—to be offered initially as a military part made up of two 64-K RAMs—will follow a successful 32-K version (two 16-K RAMs) that propelled Mostek into a top volume position in chip-carriers.

"That's not what we first intended to do," says Quinn, whose military department is working with Mostek's commercial memory departments to develop chip-carrier products, "but we changed our emphasis from being a chip-carrier supplier to one of also being a supplier of building blocks on motherboards."

"When individual chip-carriers finally do make it," he adds, "most of the country's high-volume customers will be using the chip-carrier directly on pc boards, while many medium-size users will continue to use the motherboards."

When it comes to military memory, the former Air Force captain says the motherboard and chip-carrier combination is just what the general ordered. "The military needs chip-carriers because of the problems in getting more horsepower—memory power if you will—into a smaller area." □

MEASUREMENT COMPUTATION news

product advances from Hewlett-Packard

FEBRUARY 1981

HP's new 1980 with μP-based intelligence and a new front-panel design combine to provide an oscilloscope system of great power. The 1980 is fully programmable in three ways: through HP-IB; through local built-in, nonvolatile registers which can be controlled via HP-IB; and through optional feature ROMs which plug in and expand resident firmware capabilities. In automated applications, the 1980 simplifies and reduces the time required for repetitive, complex tests. A computer can lock out front-panel controls, set up the instrument, and direct a measurement through the CRT readout.

New fully-programmable oscilloscope measurement system

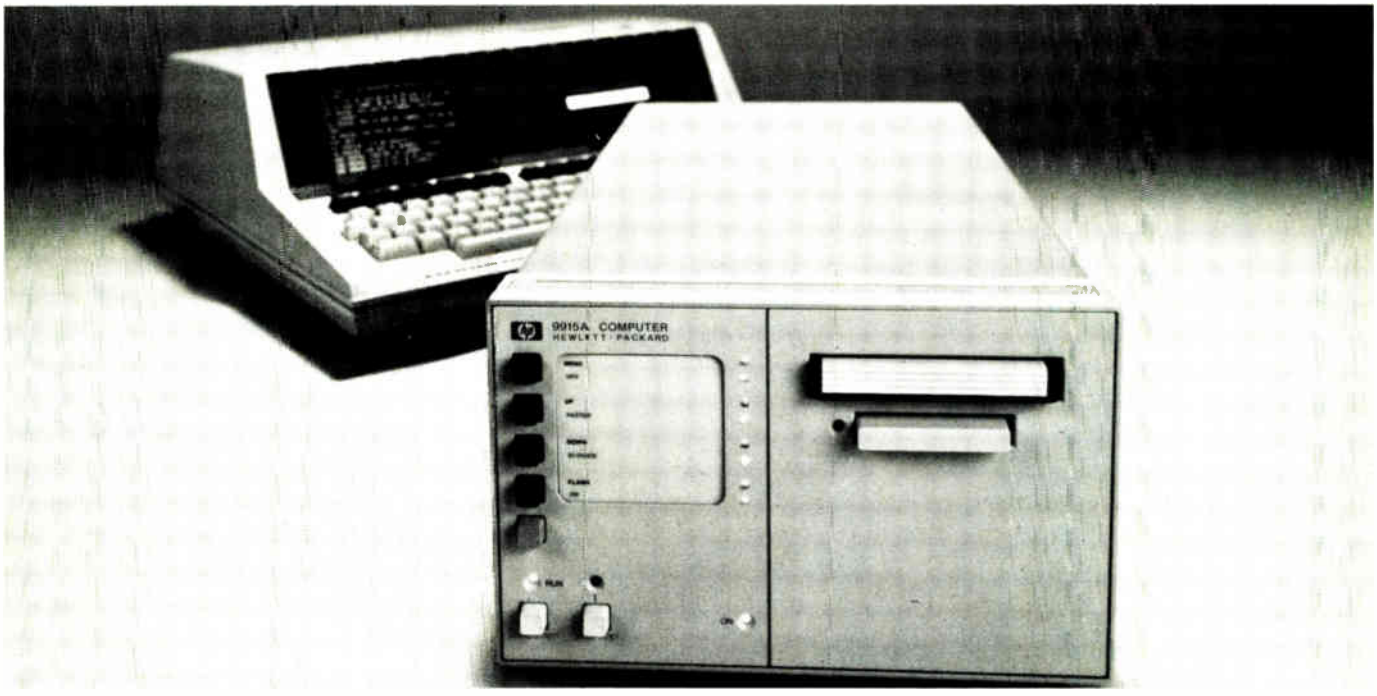
Hewlett-Packard's new, HP-IB compatible 1980 Oscilloscope Measurement System makes significant contributions in measuring, viewing and processing of time domain waveforms. This revolutionary instrument improves productivity by reducing measurement time while providing greater measurement confidence. All measurement parameters are continuously calibrated through software routines which eliminate uncalibrated operating modes. In addition, character generation permits instructions to be written on the CRT by a computer to speed complex measurements.

All measurement related front panel controls are fully programmable by an external computer. This includes variable functions such as deflection factors, sweep speeds and trigger

(continued on sixth page)

Modular Computer: A new concept in automated test, measurement and control

DESIGNED FOR HP-IB SYSTEMS



Designed for dedicated test, measurement and instrument-control applications, a new computer system also features the low system-development cost of a desktop computer at the low unit cost of a board computer. Extensive SELF TEST, AUTOSTART and error-trapping capabilities make the HP 9915A ideal for applications requiring minimal attention or unattended operations.

The new HP 9915A Modular Computer—the first in a new class of products from HP—is basically the heart of an HP-85 Desktop Computer. Consisting of a central processor, memory, operating system, and input/output ports, the 9915A is packaged in a small, rack-mountable box suitable for easy integration into instrument systems. The new modular computer solves a number of system-design problems by making it possible to buy relatively low-cost hardware, spend relatively little on software development, plus have the advantage of bringing a completed product into use quickly.

Powerful Development Station

The HP 9915A is designed to run programs developed on the HP-85 Desktop Computer. With a Program Development ROM and I/O ROM installed, the HP-85 becomes a development station featuring a powerful, interactive BASIC-language operating system. This makes it possible to write and debug application software in a fraction of the time it would take using lower-level languages. The HP-85, with all its interactive editing and debugging aids, can also serve as an HP 9915A emulator for in-system software debugging.

Once system software is complete, it can be transferred to the HP 9915A via either EPROM (erasable/programmable read-only memory) or magnetic tape. Software is available for the system designer to program EPROMs with any of several commercially available PROM programmers. The HP 9915A can accept up to 32 kilobytes of EPROM-stored information. EPROM storage is ideal for harsh environments or when program security is required.

With an optional tape unit, the HP 9915A can also exchange programs and data with HP data cartridges whenever it is necessary to change programs often or to record test data. Capacity of a data cartridge is approximately 200 kilobytes.

Economical, Integrated Interfaces

The HP 9915A frees system designers to design and pay for only the exact operator interfaces needed. Eight front-panel LEDs and eight software-definable special function keys provide an economical, integrated operator interface for many applications. Yet, the interfaces and I/O drivers required for easy connection to the system designer's choice of CRT displays (with full HP-85 graphics), keypads, typewriter keyboards, and custom control panels or keyboards are also available.

Flexible I/O Capabilities

The HP 9915A Modular Computer has the same flexible I/O capabilities as the HP-85. These include interrupt, bit manipulation, high-speed transfer, software control of interface configuration and easy data formatting. Both computers have built-in I/O drivers and use these same, plug-in interfaces: HP-IB; serial (RS-232-C or 20 mA current loop); general-purpose I/O (8 or 16-bit parallel); and binary coded decimal.

The standard HP 9915A comes with 16 kilobytes of user-available read/write memory that can be expanded to 32 kilobytes by plugging in an optional memory module. The operating system contained in 48 kilobytes of ROM, can be expanded by adding optional ROMs for matrix math, plotter/printer control and mass storage control.

Check **B** *on the HP Reply Card for more details.*

New HP technology cuts cost of high-performance plotting in half

HP has entered the large plotter market with a new technology that cuts the cost of high-performance plotting in half. The basis of this new technology is an aluminum grit covered wheel that is capable of moving single sheets of paper, polyester film or vellum. The low-mass, low-inertia mechanics in the drive system replace the heavy, bulky components of flatbed and drum plotters. This permits the use of smaller, less expensive motors and drive mechanisms, resulting in a substantial cost reduction.

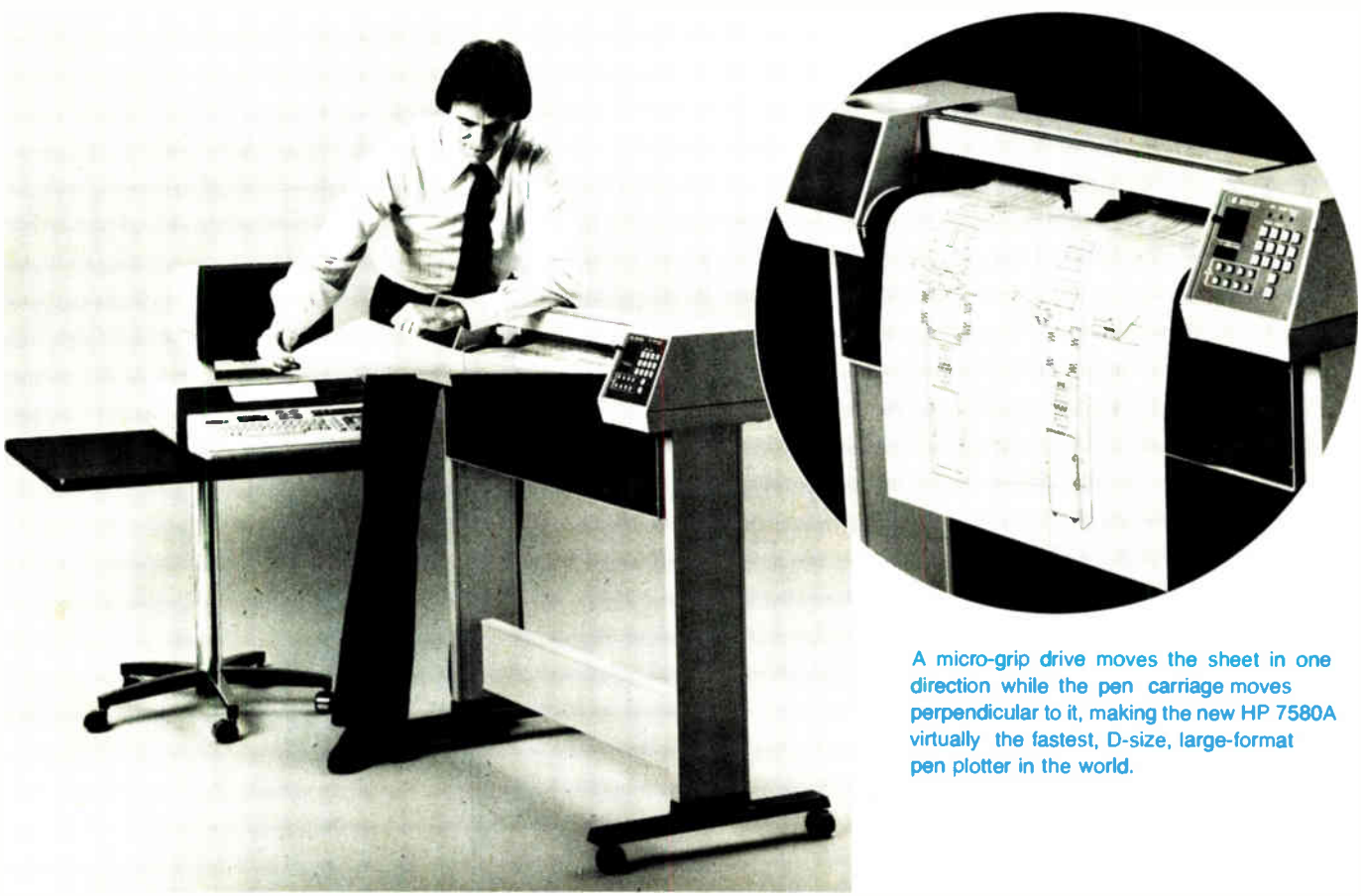
Versatility for Many Applications

This new 7580 DraftingPlotter brings low-cost/performance to such demanding applications as PC board layout, IC layout, CAD/CAM, drafting, architecture and civil engineering. The versatility required for these varied applications is impressive. The plotting media sizes range from 20cm × 27cm (8" × 10½"), smaller than ANSI A or ISO 4, to 62cm × 119cm (24½" × 46.85"), larger than D or A1 sizes. Pen types include fiber tip, liquid ink and roller ball, giving the operator a tremendous choice of different colors, line widths and line types. What's more, pen speed and force can be finely controlled to match special pen and medium combinations for maximum quality output.

Exceptional Friendliness

But the 7580A is a lot more than a new technology. The 7580A represents an advance in the ease with which plots can be made. Sheets of drawing media can be loaded within seconds. Plot size is automatically set for media size. Pen force and pen speed are automatically set for pen type. Automatic pen capping keeps pens from drying out. A VIEW mode permits viewing the plot before it is completed. Last but not least, a joystick provides interactive control of pen positioning.

Check **C** *on the HP Reply Card for many more outstanding features and benefits of this plotter.*



A micro-grip drive moves the sheet in one direction while the pen carriage moves perpendicular to it, making the new HP 7580A virtually the fastest, D-size, large-format pen plotter in the world.

The professional alternatives to meet your different memory needs. . . New HP-41CV and HP-41C

In addition to their built-in capabilities, these two calculators can be further expanded by three plug-in peripherals offering vast growth potential.

Now Hewlett-Packard offers a choice in alphanumeric, full-performance, programmable calculators with the new HP-41CV and the HP-41C. Both calculators are powerful yet easy to use.

Need lots of memory? Choose the HP-41CV—it contains up to 2,000 program lines or 319 storage registers—that's five times more built-in memory than the HP-41C. And with all this memory built-in, you can store a host of programs and still have four free ports to add the peripherals of your choice, making your system even more powerful and versatile.

If you do not require full memory capability immediately, start with the HP-41C. It has up to 400 program lines or 63 storage registers. As your needs increase, you can add The New Quad Memory Module, or up to four Memory Modules to meet your computational needs.

The new Quad Memory Module contains 256 registers or up to 1600 program lines. With this Quad Memory Module you can expand your HP-41C memory up to 2,000 program lines or 319 data registers—the equivalent of the HP-41CV.

By itself either the HP-41CV or the HP-41C may be all the calculator you'll ever need. But if you need more capability, you can expand either calculator by plugging in a thermal Printer/Plotter, an "Extra Smart" Card Reader or an Optical Wand for reading bar codes.

For more information, check **A** *on the HP Reply Card.*

Desktop computers directly measure dc voltages without conventional voltmeter

A new HP interface card now enables you to measure analog dc voltages, and directly enter digital readings of the values measured to a desktop computer.

The HP 98037A four-channel, analog-to-digital converter enables any HP 9825, Series 9800 System 35, or System 45 computer to measure dc voltages without using a conventional digital voltmeter/interface-bus system. The unit is useful for measuring applications requiring 3½-digit resolution and one-percent overall accuracy.

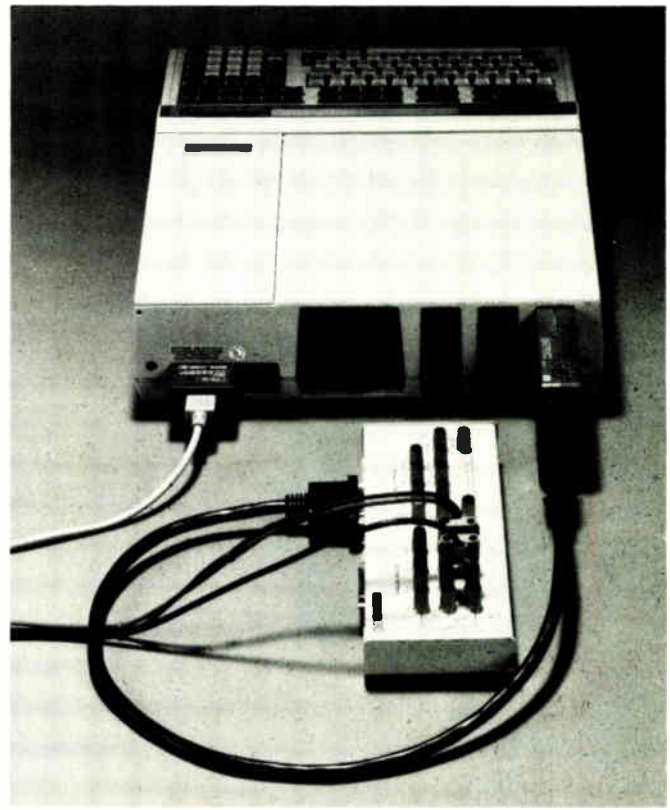
The new interface has an internal four-channel scanner and four control outputs. The user can program the HP 98037A for scan sequence, time delay, external triggering, various data formats and self testing.

The HP 98037A takes up to 150 readings per second over two software-selectable ranges (1 or 10 V), and can provide measurements to ±18.99 V dc.

A companion product to the new interface card is the HP 98637A terminal box for easy experimental breadboarding.

Standard HP OEM and volume-end-user discounts are available.

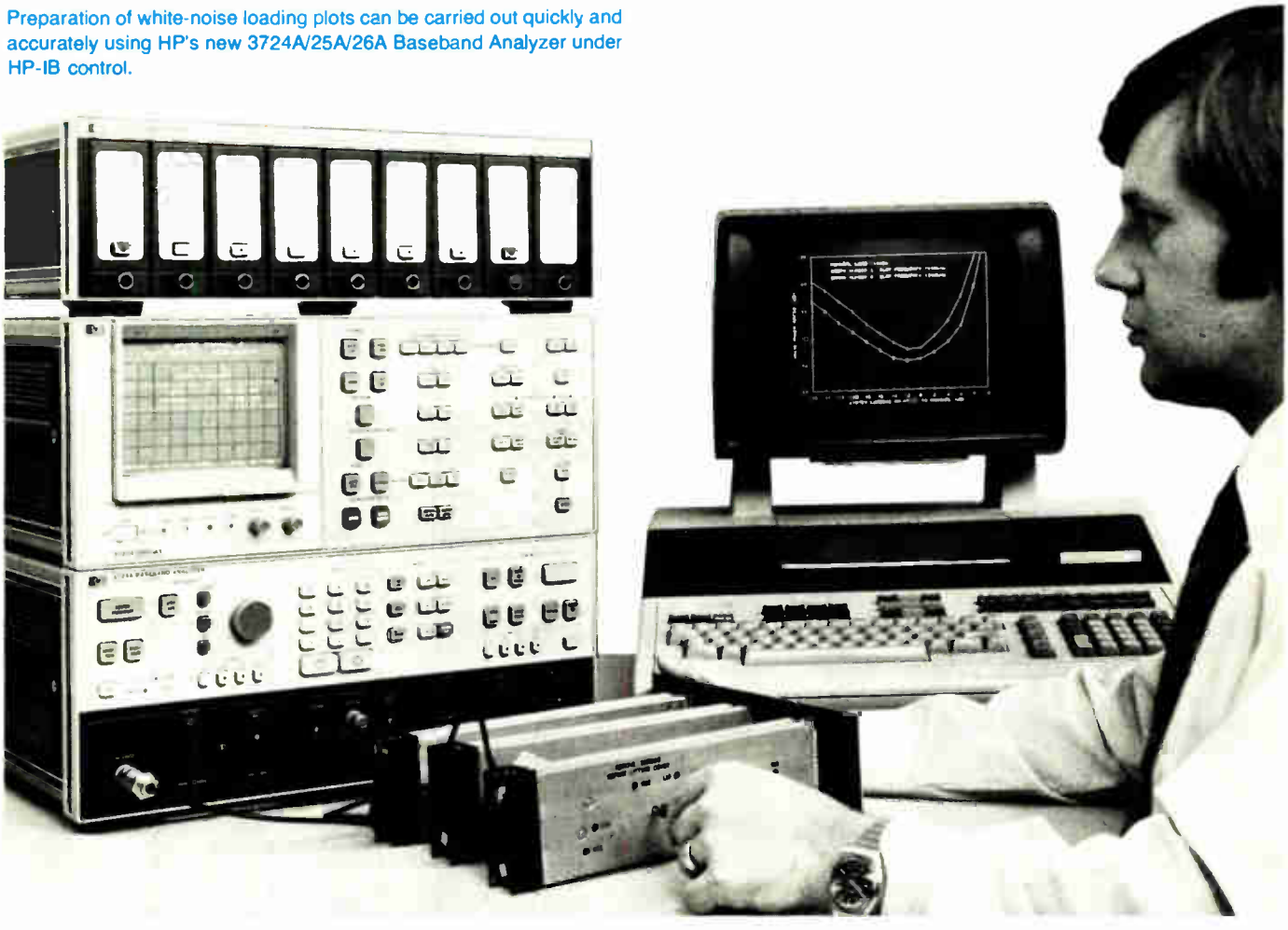
For details, check **D** *on the HP Reply Card.*



HP introduces a new approach to microwave radio measurement

DESIGNED FOR HP-IB SYSTEMS

Preparation of white-noise loading plots can be carried out quickly and accurately using HP's new 3724A/25A/26A Baseband Analyzer under HP-IB control.



The new 3724A/25A/26A Baseband Analyzer from Hewlett-Packard combines all the instruments used on the baseband of a radio system in one integrated test set and links them through a common CRT and keyboard. Measurement modes can be changed at the press of a key without any of the recabling and retuning required for a collection of stand-alone products. The baseband analyzer replaces: wideband power meter, selective voltmeter, synthesized signal generator, frequency counter, spectrum analyzer, and white-noise test set.

The result is one instrument with real flexibility, very high measurement accuracy and new ways of performing measurements. Model 3724A/25A/26A is ideally suited for commissioning and troubleshooting microwave radio links. And, with dedicated software routines, it is an invaluable tool for both in-service and out-of-service measurements.

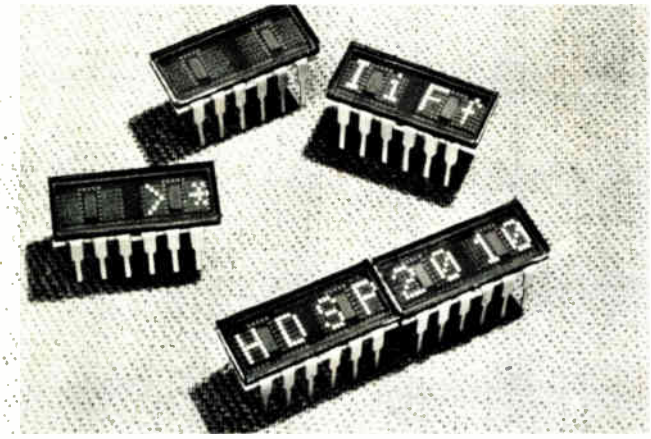
The new test set is HP-IB compatible. At its simplest the bus may be used to dump hard copy of the CRT display to a printer/plotter without an additional controller. However, the addition of an HP-IB controller will considerably enhance the capability of the baseband analyzer. For example, time-consuming routines such as preparation of white-noise V-curves can be completely automated to relieve the tedium and improve the accuracy and speed of results. Further, the baseband analyzer, under HP-IB control, can be a key part of a manufacturer's automatic final test system or be included as part of a centralized surveillance system for monitoring and analyzing a complex microwave radio network.

The new baseband analyzer has been designed with those who manufacture, commission and maintain microwave radio links in mind. It offers these benefits:

- Increased production throughput at final test and reduced time outside inspectors need to spend in the plant carrying out acceptance trials.
- Faster system testing and reduced on-site time of commissioning engineers.
- Reduced main channel downtime by allowing maintenance personnel to perform out-of-service checks much more quickly and accurately.

For more information, check **E** *on the HP Reply Card.*

New display with temperature range down to −40°C



HP's new compact, standard red alphanumeric display, the HDSP-2010/TXV-2010, has the high reliability required for military, space, medical and industrial control applications. It has a guaranteed operating range of −40°C to +70°C. The upper temperature range can extend to +85°C by special heat sinking techniques described in HP's Application Note #966.

Based on HP's highly successful HDSP-2000, a compact, package-efficient, 5-by 7-dot matrix alphanumeric component, these displays have a (3.8 mm) 0.15" character font and integrated shift registers plus constant current drivers to greatly simplify design. The HDSP-2010, has a guaranteed leak rate of 5×10^{-7} cubic centimetres per second and temperature cycles from −55°C to +100°C. The TXV-2010 is subjected to the standard military screening program.

For more information, check **F** *on the HP Reply Card. For Application Note #966, check* **G**.

Terminate fiber optic cables with speed, quality and ease

This new HFBR-0100 Fiber Optic Connector Tooling Kit supplies the user with everything needed for terminating fiber optic cable. It is a complete kit designed for quick field installation of Hewlett-Packard HFBR-4000 connectors onto HFBR-3000 through HFBR-3400 series 100/140 μm optical fiber cable. The kit includes a set of common connectoring tools, a set of connector piece parts (HFBR-4000) for terminating ten connector ends, adapters (HFBR-3099) for making connector to connector junctions, a step-by-step illustrated user's manual, and a consumables kit (available separately as HFBR-0101) with enough material for assembling ten fiber optic connectors, plus a set of custom tools (available separately as HFBR-0102). This kit enables the novice fiber optic technician to quickly and easily make factory quality connections (1.5 dB typical) while an experienced user will be able to assemble a connector onto fiber optic cable in less than 20 minutes. The Kit is available from authorized HP distributors.

Check **H** *on the HP Reply Card for additional information.*

New power field-effect transistors from HP

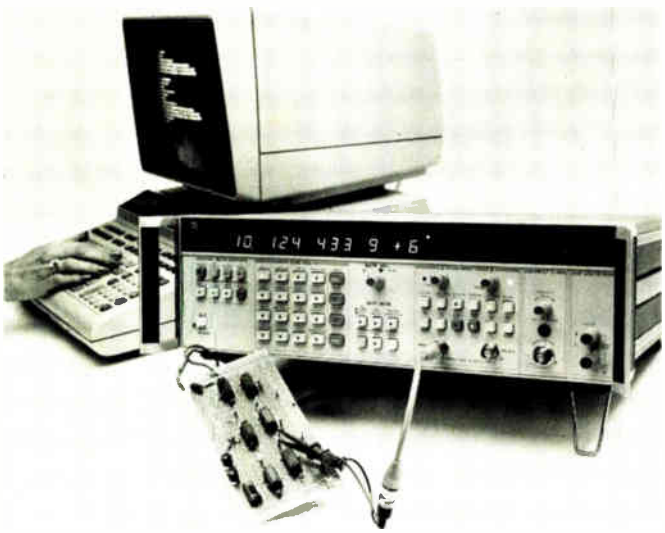
HP's new Power MOS field-effect transistors (MOS FETs) are designed primarily for use in off-line switching power supplies, power inverters and converters—but are also ideal for ultrasonic transducer drivers, audio amplifiers and general industrial applications.

Called Hewlett-Packard's HPWR-6501 family, these four, high-performance power FETs feature high breakdown voltage (V_{DSS}): 450 V minimum; low on-resistance ($R_{(on)}$): 0.85 Ω maximum; and fast switching speed: 50 nanoseconds typical. They operate at high frequencies (200 KHz or more), with simple drive circuits and are not limited by "second breakdown" phenomena in their rated safe operating areas.

These Power MOS FETs are available in the industry-standard TO-3 steel hermetic package.

Check **I** *on the HP Reply Card for more details.*

HP's HP-IB counter goes fully programmable



Automatic test equipment and bench top systems users can employ the new, full programmability option for HP's 5335A. It brings high performance to universal counter measurements and automatically measures many parameters not usually measured by counters.

With this newest option for the 5335A Universal Counter you'll be able to remotely control all front panel controls, even the trigger levels, via HP-IB. Option 040 makes the 5335A HP's most versatile, high performance universal counter.

The counter's automatic interpolators and reciprocal-taking technique give an outstanding resolution of nine digits/s in frequency measurements up to 200 MHz (1.3 GHz optional), and a single-shot time interval resolution of two ns. This remarkable counter also automatically measures voltage, phase, slew rate, duty cycle, rise/fall times and statistics. It can apply math (+, −, ×, ÷) to any measurement.

Four modes of triggering and six modes of arming further enhance the 5335A's versatility. The standard 5335A is already extensively programmable via HP-IB. Option 040 remote controls trigger levels, input filter, attenuators, AC/DC coupling and input impedance.

Check **K** *on the HP Reply Card.*

New signature multimeter speeds μP troubleshooting

This compact, lightweight instrument conveniently serves the basic needs in troubleshooting microprocessor-based products:

To locate bad synchronous digital nodes, this 5005A Signature Multimeter has two signature analysis modes, normal and qualifier. The qualifier mode speeds your job by ignoring bit stream sections of no interest to the test at hand.

To help locate bad asynchronous digital nodes, it measures time interval and will totalize pulses.

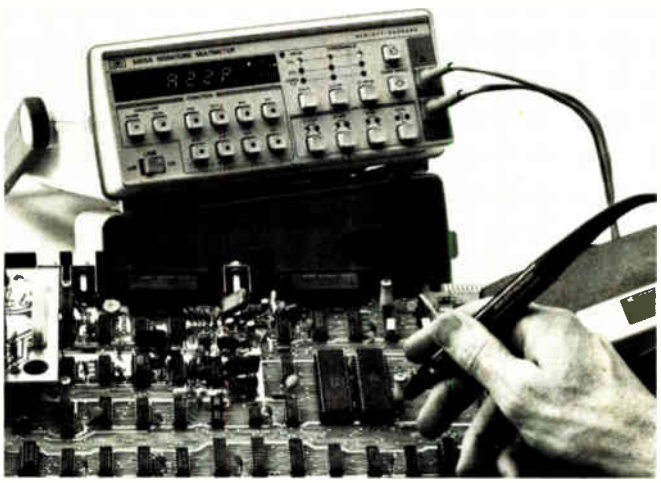
To help locate bad analog components, it measures voltage, differential voltage, resistance and frequency to troubleshoot power supplies, clocks and dividers, etc.

To help locate other faulty elements, its ohmmeter and peak voltmeter trace stuck nodes and intermittent faults.

And for a wide variety of faults, it serves as a high-speed, digital logic probe sensing pulses as brief as 10 ns.

The 5005A also handles higher speed bit streams than other HP signature analyzers.

For full details, check **J** *on the HP Reply Card.*



The 5005A Signature Multimeter speeds μP products troubleshooting in production and field service. It serves as a signature analyzer, DMM and frequency counter for TTL, ECL, and CMOS circuits.

Simplify and reduce complex oscilloscope tests

(continued from first page)

levels. The computer can integrate the front panel control settings and then calculate and print out measurement results. In addition, any or all of the front panel keys can be "locked-out" to prevent inadvertent actuation which could result in erroneous measurements. This automated operation improves productivity by increasing through-put while improving the quantity and quality of measurements.

In manual applications, the 1980's approach to instrument setup eliminates the need for adjusting many controls to speed measurements and analysis. A press of the Auto-Scope key directs the 1980 to seek, scale and display input waveforms. When coupled with a computer in a laboratory environment, the 1980 provides fast analysis of data for circuit development and characterization. Thousands of measurements may be performed and analyzed in minutes.

The standard 1980 includes two 100 MHz vertical input channels, independent five ns main and delayed sweeps, eight built-in nonvolatile registers for saving measurement setups, HP-IB interface, and can be calibrated from the front panel in less than 45 minutes without external test equipment.

Check **L** *on the HP Reply Card for more exciting details.*

HP designs electronic coordinate determination system for industrial applications

A new electronic X,Y,Z coordinate determination method designed for dimensioning large objects in industrial environments is now available from Hewlett-Packard. The HP 3822A Coordinate Determination System provides accurate, non-contact measurement to a variety of items with a specified repeatability of 1:100,000 (repeatability specification based on a 50-foot object–order technical data sheet for specifications on larger objects). Designed to be transportable, the HP 3822A is small and light enough to be moved quickly and easily to the object to be measured. This eliminates the problems associated with moving large objects to a coordinate measuring machine.

The new 3822A requires the operator to aim two electronic digital theodolites at a measurement point. The system's computer then automatically reads the theodolite angles, translates the angle information into X,Y,Z coordinates and prints the results along with measurement information. To accomplish this, the 3822 was designed utilizing a time-tested methodology based on triangulation. Hewlett-Packard has combined this technique with electronic digital theodolites and a powerful HP computer. The result is a system with computational power to solve the scores of difficult coordinate determination equations and display virtually instantaneous results.

The HP 3822A is designed for determining the X,Y,Z coordinates of large objects in industrial environments. Easily transportable, this system solves scores of difficult coordination equations and displays them virtually instantaneously.

Obtain further information on this exciting new product by checking **N** *on the HP Reply Card.*

New application note describes semi-automatic transceiver test set

DESIGNED FOR HP-IB SYSTEMS

Application Note #300, *High Performance Semi-Automatic Transceiver Testing*, describes a benchtop test set that makes in-channel tests on 150 kHz to 990 MHz AM, FM and PM transmitters, receivers, and transceivers.

This E85 8903A Test Set makes optimal use of today's fully-programmable, microprocessor-based measuring instruments by linking them via HP-IB under the HP-85 desktop computer control. The result is a miniature distributed system wherein much of the work formerly handled by the computer is done locally by instruments that are experts at their tasks. Those key instruments are the new Hewlett-Packard 8656A Signal Generator, 8903A Audio analyzer and the 8901A Modulation Analyzer.

For a free copy of AN #300, check **M** *on the HP Reply Card.*

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HEWLETT PACKARD

hp MEASUREMENT COMPUTATION news
product advances from Hewlett-Packard

January/February 1981

New product information from

HEWLETT-PACKARD

Editor:
Bojana Fazarinc

Editorial Offices:
1507 Page Mill Road
Palo Alto, California, 94304 U.S.A.

Siemens infrared products now visible in the U.S.

Introducing the world's broadest infrared/photodetector product line

In Europe, Siemens IR/PD products are rated number one for quality and dependability.

So when we got the go-ahead to begin distributing the Siemens infrared/photodetector product line in the U.S., we were naturally excited.

Siemens makes over 200 different IR/PD products. These include: IR emitters, photodiodes, and phototransistors.

They range from high reliability, hermetically sealed products for military applications to low cost products in plastic packages for commercial uses.

Siemens offers many different sizes and shapes. Single packages to 10-unit arrays. Production volume is huge. Certain miniature types are produced in the millions of units per month.

The Siemens IR/PD product line is now available through the extensive Litronix distributor network in whatever supply you require...and at highly competitive prices.

So welcome, Siemens. We are pleased to assist you in becoming the most visible "non-visible" product line in America.

IR/PD Product Selector Guide available from Litronix, 19000 Homestead Road, Cupertino, CA 95014. (408) 257-7910, or the following distributors.

U.S. Distributors: Advent, Almac-Stroum, Arrow, Component Specialties, Gerber, Hamilton Avnet, Harvey, Kirkman, Lionex, Marshall, Moltronics, Pioneer-Standard, Summit and Zeus

litronix A Siemens Company

Circle 27 on reader service card

Intel's HMOS.* Setting memory designs of the

Intel's high-performance production process – HMOS – makes possible a new generation of memory products: 64K dynamic and 16K static RAMs, a 64K EPROM and 16K E²PROM. Putting a whole range of new design possibilities on the memory map.

Intel's total line of HMOS memory products continues to set industry standards for performance, density and functionality. It includes the new 2164 and 2167 RAMs, 2764 EPROM and the 2816 in-circuit Electrically Eraseable PROM.

These devices represent the most recent advances in the evolution of our HMOS process technology, which began in 1977. As Intel continues to apply this technology, increasingly higher performance and higher levels of integration are being achieved. Plus, as manufacturing knowledge accumulates, higher yields and increased reliability are attained. Hence, Intel's HMOS technology and planned product upgrades protect your investment in existing designs. How? By reducing your overall product lifecycle costs, and maintaining your competitive advantages in a rapidly changing technology area.

New 64K dynamic RAM now available

When you're designing today's commercial computer systems—micro, mini or mainframe—you need readily available memories with all the built-in quality and reliability you can find. Memories like our new 2164 dynamic RAM. The 2164's wider operating margins and increased yields are the results of our design priorities and use of new redundancy fabrication techniques.

The +5V 2164 now offers high density in a compact, industry standard 16-pin DIP, along with access times ranging from 150 to 250 ns. And it's the logical extension to the 16K industry standard, our +5V 2118. So now your overall system designs can be simpler and more compact—enhancing both economy and reliability. And upward compatibility means your investment in existing designs is protected.

New high-density 16K static RAM

If you're designing high-density static RAM memories for buffer, cache, control store or main memory in computer and microprocessor applications, our

the course for future.

new 2167 should be part of your plan. Like the 2164, it incorporates component-level redundancy in fabrication, leading to greater device availability.

In its 16K x 1 format, this double poly HMOS II part combines in one device the speed and power features of our industry-standard 2141 and 2147 4K RAMs. Our high-density 2167 offers a standard 20-pin device with access times in the 55 to 100 ns range. Like the 2147, the 2167 features low active power dissipation and automatic power down on deselection, drastically reducing power consumption when compared to constant-current static RAMs. An alternate 4K x 4 format—the 2168—will also be available soon.

A new 64K EPROM family member

With the addition of our new 64K device—the 2764—you now have a universal solution for designing in EPROMs. When you're on the Intel price/performance curve, you can select the optimum memory solution: 2716, 2732, 2732A or 2764. If you need high-speed memory (up to 200 ns) to improve microprocessor performance, and high densities to save board space, you can now design in the 2764.

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Best of all, as HMOS-E technology matures, memory cost-per-bit will continue to decrease significantly. By mid-1982, high-speed, high-density EPROMs will cost no more per bit than the EPROMs you currently buy. The 2764 is already in volume production, so it's available.

New E²PROM is byte eraseable in-system

The announcement of our 2816 in-system Electrically Eraseable PROM marks the beginning of a whole new class of non-volatile memory applications. Consider the microcomputer design possibilities. Reconfigurable systems. Self-calibrating equipment. Self-adjusting machine tools. Self-diagnosing/correcting products. And since the 2816 is manufactured by the HMOS-E process, it will follow the EPROM learning curve, and dramatically change all cost-per-function relationships in systems using program store or configuration constants.

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Meetings

Fifth International Conference on Digital Satellite Communications, IEEE, Intelsat, and Telespazio SpA, Fairgrounds Conference Building, Genoa, Italy, March 23–26.

Digital Communications Techniques Seminar, IEEE and Princeton University Department of Electrical Engineering, Princeton University, Princeton, N. J., March 24.

FOC 81 East—International Fiber Optics and Communications Exposition, Information Gatekeepers Inc. (167 Corey Rd., Suite 111, Brookline, Mass. 02146), Hyatt Regency, Boston, March 24–26.

High-Temperature Electronics Conference, IEEE Solid State Circuits Society, Department of Energy, and University of Arizona, Ramada Inn, Tucson, March 25–27.

Semiconductor Microlithography VI Conference, Society of Photo-Optical Instrumentation Engineers (P. O. Box 10, Bellingham, Wash. 98225), San Jose Hyatt House, San Jose, Calif., March 30 31.

1981 IEEE International Conference on Acoustics, Speech and Signal Processing, IEEE, Sheraton-Atlanta Hotel, Atlanta, March 30–April 1.

Interface '81—Ninth National Data Communications/Distributed Data Processing Conference, The Interface Group (160 Speen St., Framingham, Mass. 01701), Las Vegas Convention Center, Las Vegas, Nev., March 30–April 2.

Optical Characterization Techniques for Semiconductor Technology Conference, Society of Photo-Optical Instrumentation Engineers (P. O. Box 10, Bellingham, Wash. 98225), San Jose Hyatt House, San Jose, Calif., April 1–2.

First International Conference on Robot Vision and Sensory Controls, IFS Conferences Ltd. (35/39 High St., Kempston, Bedford MK42 7BT, England), Hilton Hotel, Stratford-upon-Avon, England, April 1–3.

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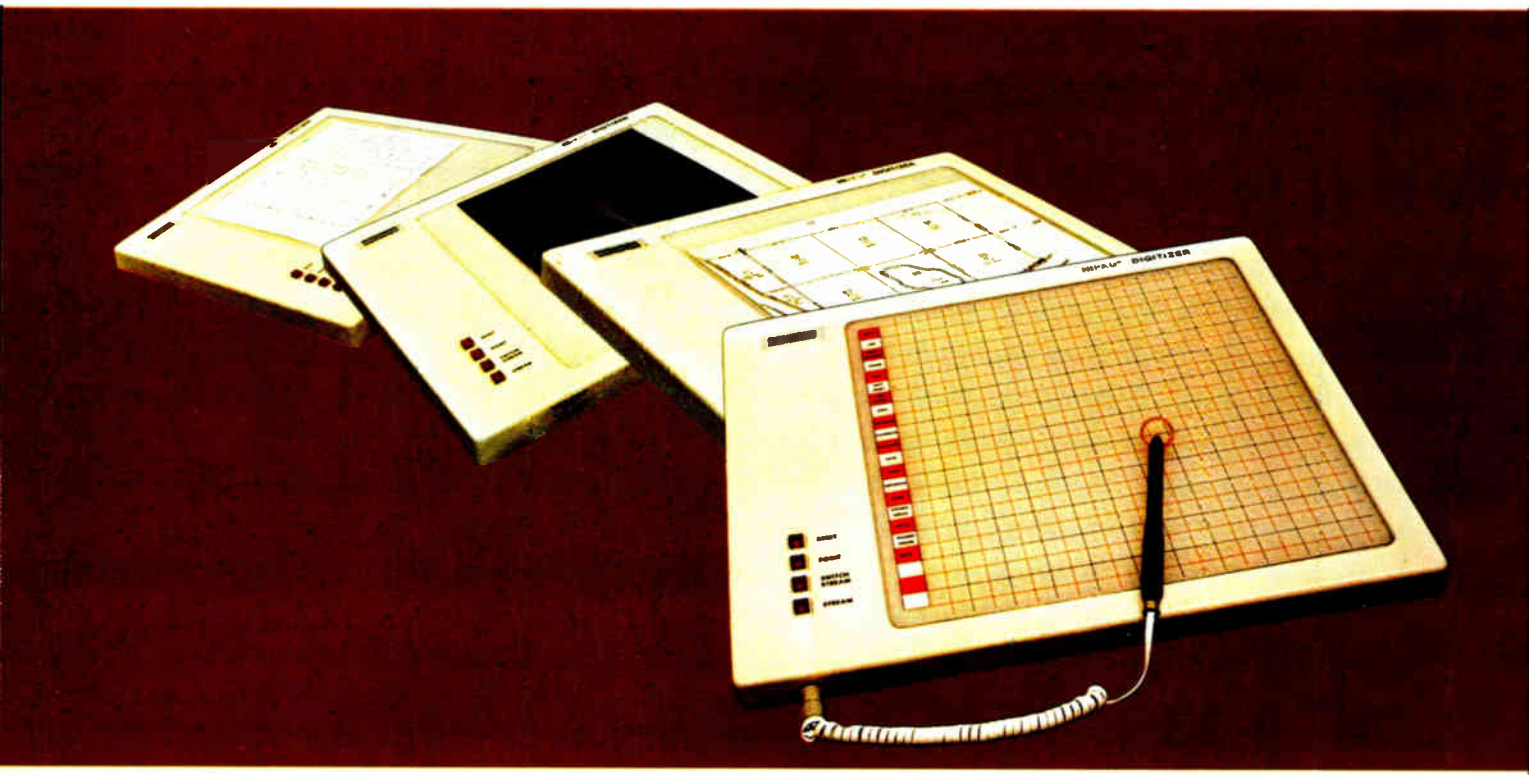

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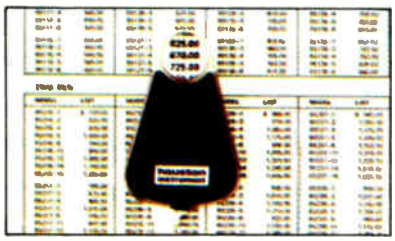

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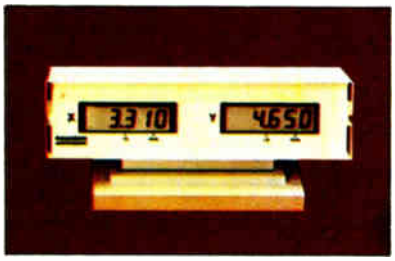

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Electronics newsletter

Rockwell quits commercial bubbles

Rockwell International Corp. is dropping out of the commercial market for magnetic-bubble memories, though it will continue to build units for military customers. It says it is making the move **because of the market's slow development,** compared with the immediate potential of the military side. A spokesman at Rockwell's Electronic Devices division, Anaheim, Calif., says Rockwell will continue support of existing commercial bubble customers but is not taking new orders. What effect the decision has on second-source agreements with the Motorola Semiconductor Group and Siemens AG is the subject of discussions with them, the spokesman says.

Oki plans push for 64-K RAM

Not yet known as a maker of 64-K dynamic random-access memories, Oki Semiconductor has actually been selling a two-supply part to Nippon Telegraph & Telephone Public Corp. for over three years, just as Fujitsu has been. And like Fujitsu, it now has a 5-V-only device, the MSM 3764, that it will market aggressively. In fact, Oki, from its Santa Clara, Calif., outlet, intends to sell 5,000 units this month, then 200,000 per month by October, and double that by early 1982. **The 3764's big plus is its speed, with 80% of the good dice faster than 150 ns, says Oki.** The 46,000-mil^2 (29.7 mm^2) chip uses 128-cycle, 2-ms refresh and is laid out like Motorola's 64-K RAM, but with two layers of polysilicon.

Motorola itself shipped over 150,000 of its 64-K RAMs last year alone, but the device's reputation has been marred by soft errors due to alpha radiation. Fighting back, Motorola is switching to a more substantial type of polyimide coating. Moreover, it has added an implant—and a mask step—to give its memory high-capacitance cells. Parts with the Hi-C structure, as it is called, will be available in the second half of this year.

New material at Argonne boasts high resistivity

Researchers at Argonne National Laboratory in Argonne, Ill., are preparing a patent application for a new material made with alternating ultrathin layers of metal said to exhibit resistivity at room temperature up to two orders of magnitude higher than commonly used pure resistor materials. As one of a new class of materials dubbed LUCs (for layered ultrathin coherent structures) by inventors Charles M. Falco and Ivan K. Schuller, the new substance **may hold promise in very large-scale integrated circuits where packing density is important.** The distinguishing characteristic of LUCs is that they are built by sequential deposition of ultrathin layers (between 1 and 4 atoms thick) of two metals with differing crystal structures and dimensions.

GenRad STI to introduce more VLSI testers

Continuing its aggressive move into the market for automated test systems for very large-scale integrated circuits, GenRad Semiconductor Test Inc. of Santa Clara, Calif., has announced plans for three new systems. According to president Brian Sear, **the company will introduce two focused testers,** one for memory and another for microprocessors, by early 1982. Based on the same architecture as the general-purpose GR16 [*Electronics,* Jan. 13, 1981, p. 187], the production-targeted systems will sell in the $200,000-to-$300,000 range. The company also plans to introduce a complex general-purpose tester—one with up to 144 pins per test head—in the near future, even though Sear says he has "seen some softness" in the market, paralleling that for semiconductors.

Electronics newsletter

Systems house formed for local networks

The local-computer-network field, virtually nonexistent four years ago and now including more than 100 companies building hardware, has added its first systems house. The new company, Architecture Technology Corp., has been formed in Minneapolis with a unique approach: **it will not develop hardware but will instead concentrate on meeting the need for system-oriented services** such as system integration, consulting, and educational services.

Signetics to source Fairchild FAST logic

Signetics Corp. of Sunnyvale, Calif., will be the initial second source for the FAST (Fairchild advanced Schottky TTL) family of logic devices via an accord with Fairchild Camera & Instrument Corp. of Mountain View, Calif. The licensing agreement will allow Signetics to make and market all 37 products currently in the 74F line as well as offer some proprietary products of its own. The 74F family is pin-compatible with existing Schottky series (74S) parts, **while reducing power consumption up to 75% and improving speed about 50% over these devices.**

Controller LCD works like a tube display

Engineers at the Modicon division of Gould Inc. in Andover, Mass., in building a small programmable controller, have come up with a liquid-crystal display that functions much like one using a cathode-ray tube. **Ladder diagrams and logic circuits to be used by the controller can be displayed** on its 1.5-by-5-in. surface. The controller itself is based on a Zilog Z80 microprocessor and is small enough to be rack-mounted on manufacturing process-control equipment. Modicon will sell it for less than $500, and plans to market the display separately on a programming panel.

Allied Chemical offers tunable alexandrite laser for annealing

Allied Chemical Corp.'s new electro-optical products department in Morristown, N. J., will begin shipping laser-based systems for commercial, industrial, and military applications later this year. A synthetic alexandrite laser with a 700-to-815-nm wavelength will be the basis for a semiconductor annealing system costing $100,000 to $125,000 to be offered in the second quarter. Comparable with other solid-state lasers, the alexandrite device is tunable over its entire bandwidth, **and becomes more efficient at higher power levels as the operating temperature increases.**

Data General adds units in reorganization

In an effort to decentralize authority and delegate responsibility, Data General Corp. of Westboro, Mass., is reorganizing itself along market lines. The firm's three new divisions—Information Systems, Small Business Systems, and Technical Products—**each will have a general manager with profit and loss responsibility.** The new divisions will report to executive vice president Herbert J. Richman.

Addenda

Mattel Electronics, the Hawthorne, Calif., division of Mattel Inc., will break away from electronic toys and games to enter the self-improvement market. At this June's Consumer Electronic Show, Mattel will show **a line of electronic aids for calorie counting and other "me-generation" pursuits.** . . . An image-processing system for the robotics market is coming this spring from Octek Inc. of Burlington, Mass. The model 4200 **digitizes and manipulates video inputs and outputs,** the eyes of robotic systems.

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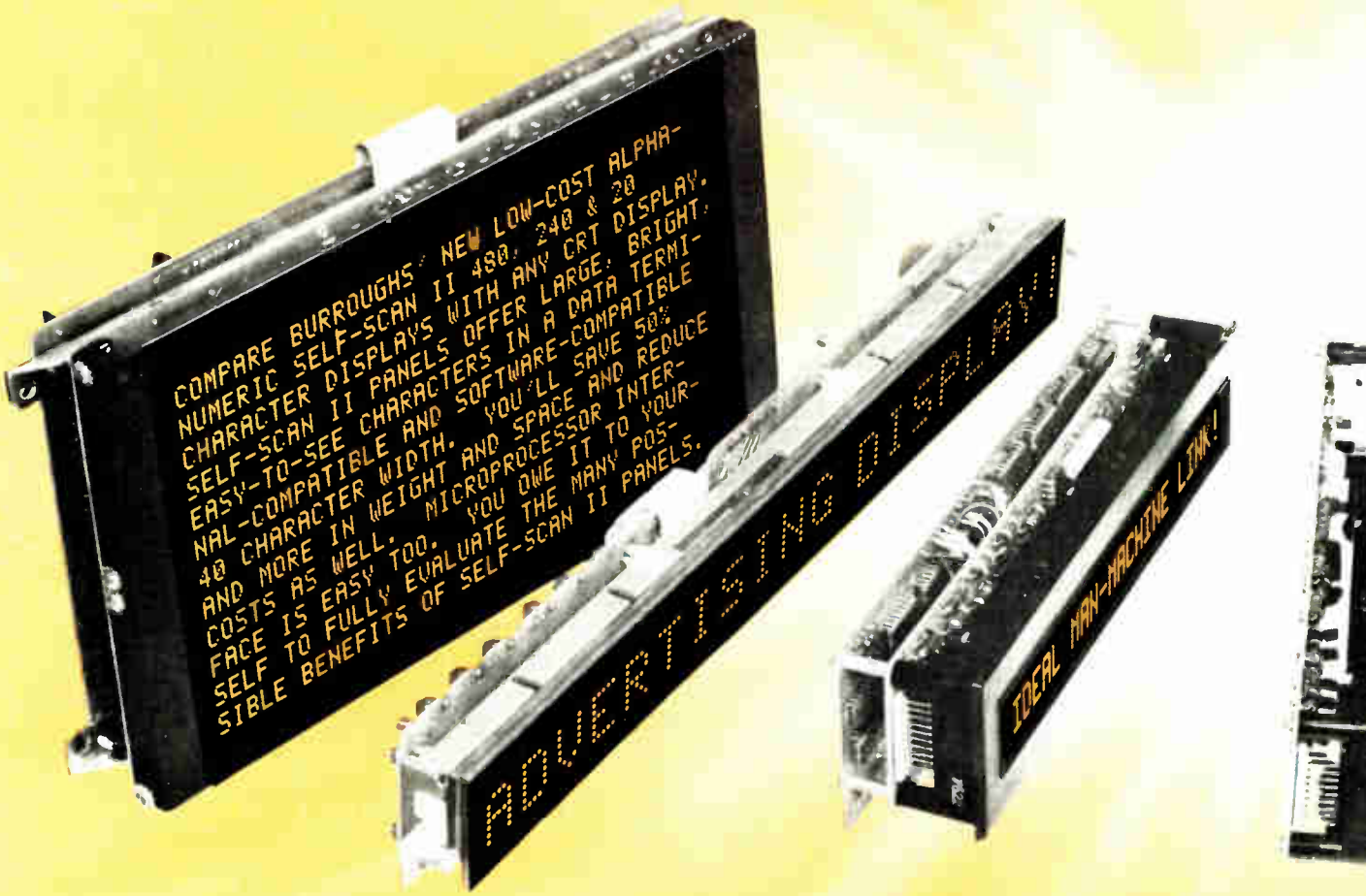

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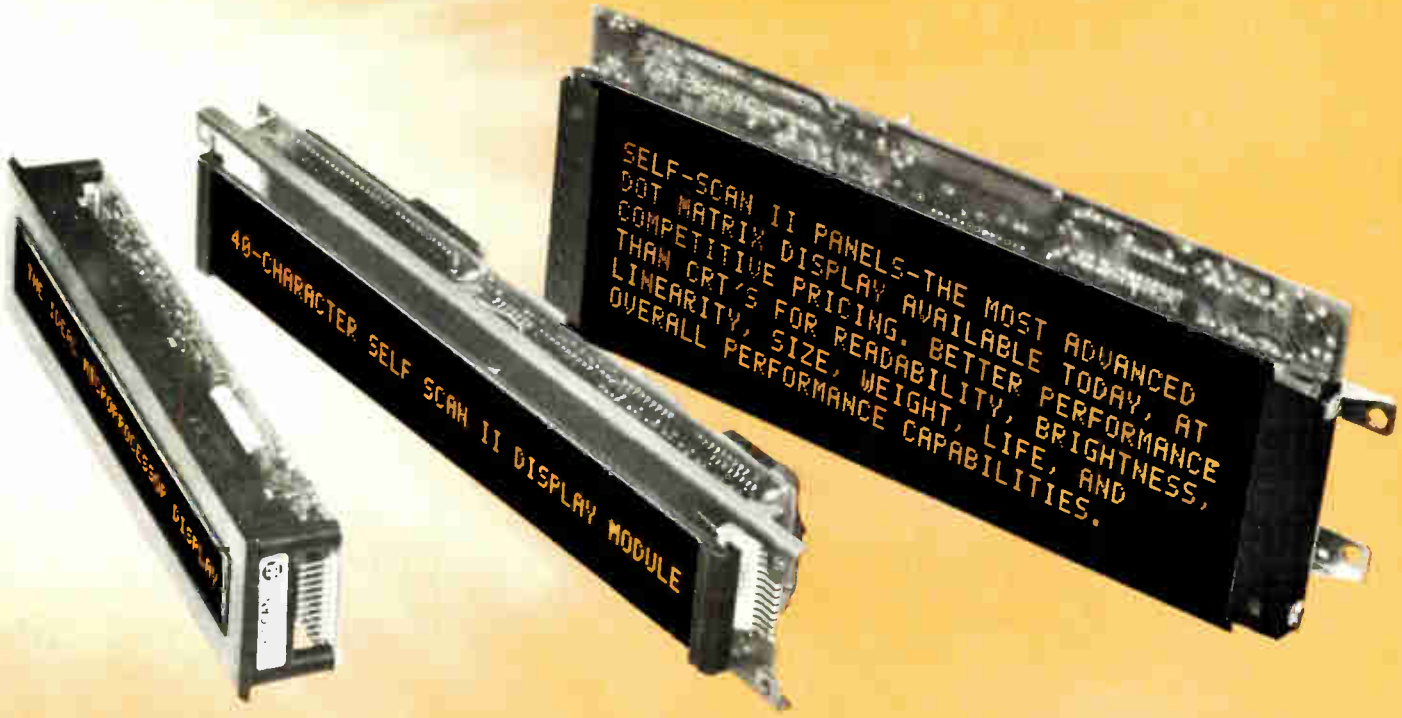

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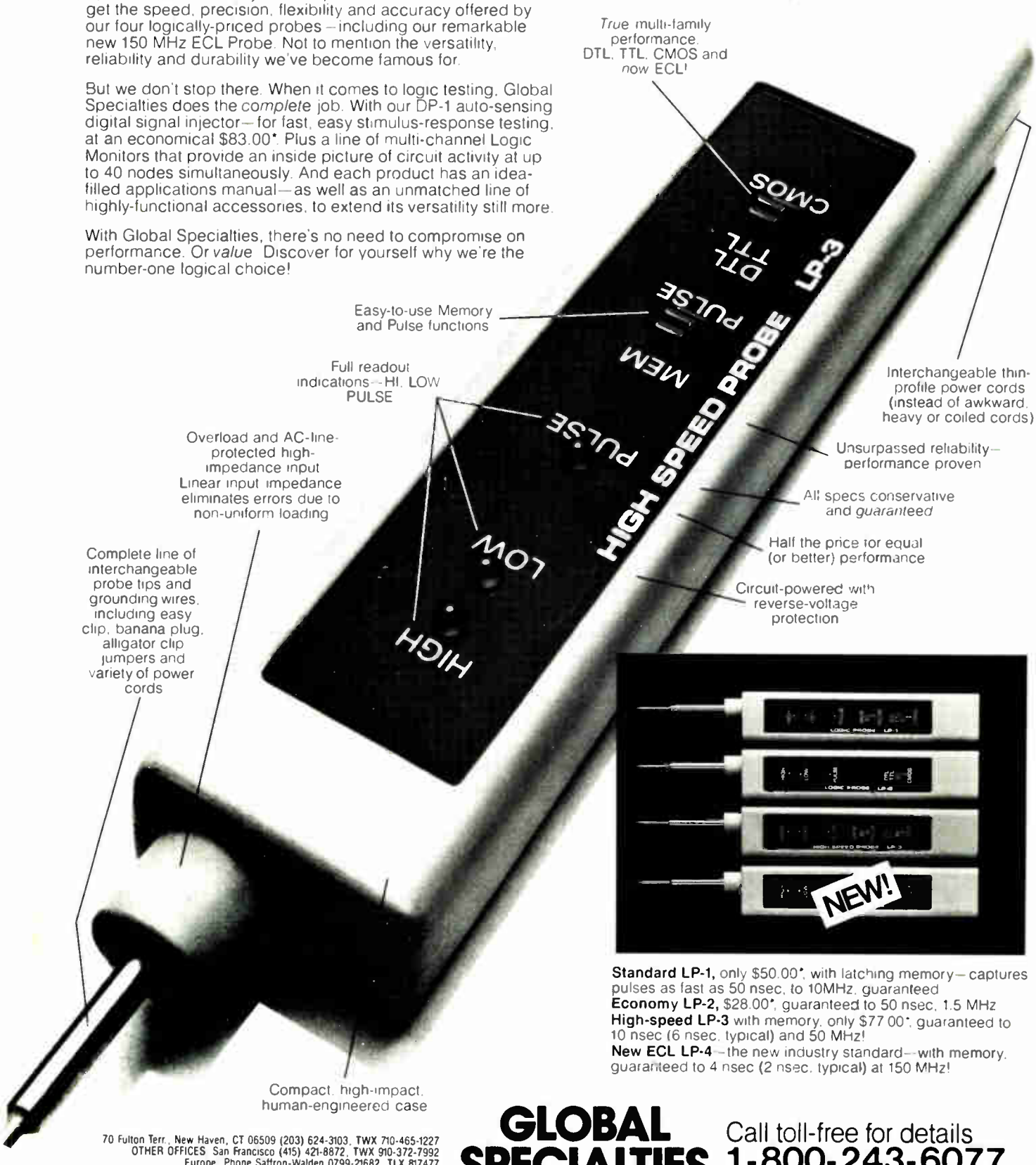

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Circle 40 on reader service card

Low-V inverter logic outperforms ECL yet saves power

by John G. Posa, Solid State Editor

New IBM bipolar approach cuts delay time with two-stage NOR cell; shrinks die area as well

Using standard bipolar technology, International Business Machines Corp. has developed a circuit configuration that outperforms emitter-coupled logic. Not only is it about twice as fast as ECL; but it uses a fraction of the power.

What's more, the low-voltage inverter logic, as it has been named, takes up little more die area than TTL cells, and much less than its ECL counterpart. IBM is using rather aggressive 2.5-micrometer minimum features to build its developmental chips, but circuit design, not processing, is the essence of the performance gain.

NOR gate. The primitive function in LVI logic is a NOR gate built with two stages—fewer than ECL or TTL requires—as part (a) of the figure shows. The first stage, made up of transistor Q_1 and resistors R_L and R_E, sets up appropriate dc levels in the circuit. The second, containing transistors Q_2 and Q_3 and resistor R_O, is a push-pull output driver.

"The unique interconnection of dc level-setting and driver sections results in a delay of only one collector time," explains Richard R. Konian, senior designer at IBM's East Fishkill, N. Y., facility. In other words, "any line you draw from any input to the output only passes through a single transistor." One such path is colored in (a).

As in ECL, the basic gate structure is nonsaturating, which shortens propagation delays, because saturation leads to much more stored charge. Also, the output stage supplies low impedance and hence high drive. "Push-pull output stages can also be built with ECL," remarks Konian, "but not without at least two collector time delays."

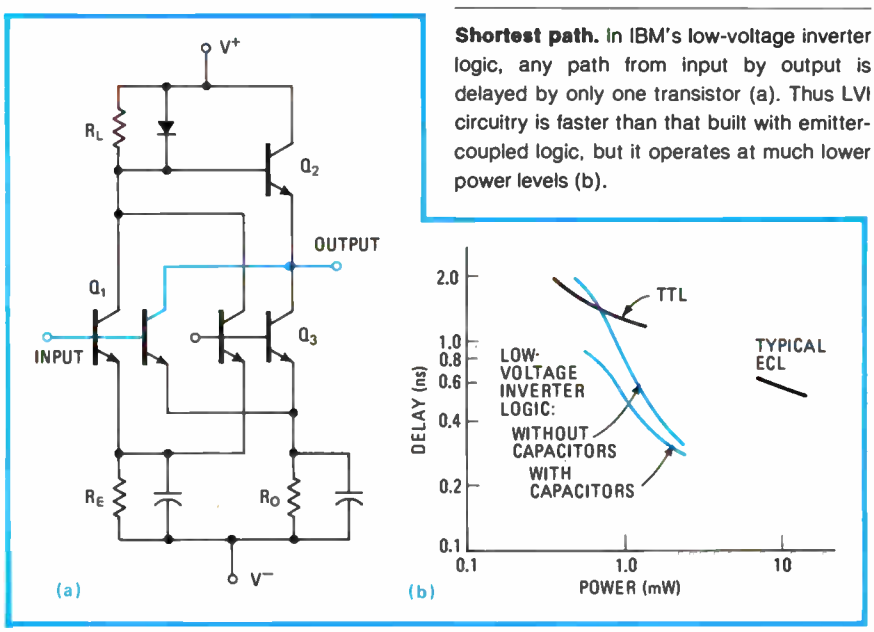
The two-input LVI NOR cell occupies an area of 86.6 by 116 μm, or just over 15.5 square mils. With the same 2.5-μm layout rules, a TTL gate consumes 14.5 mil² of silicon; in ECL 18.6 mil² is required. The curves in (b) show that gate delay in LVI logic approaches 350 picoseconds at power levels under 2 milliwatts, whereas ECL consumes 10 mW in reaching about 700 ps.

"I personally feel that the circuit is most applicable at power levels from 1 to about 2 mW," Konian says. At these levels, propagation delay neatly bridges the gap between TTL and ECL. "Here we have the promise of a circuit that has drive constants similar to that of ECL but at considerably lower power levels."

LVI gets its name and its lower power consumption from the fact that logic swings can be as low as 2 volts—less than half that of ECL. "The supply voltage only has to be comfortably greater than two V_{BE} drops," explains Konian. A V_{BE} drop, the voltage across a transistor's base-emitter junction, is equivalent to the voltage across a forward-conducting diode.

Supply side. Also unlike with ECL, the negative supply terminal can be grounded. "It will operate from a single positive supply," he says, although the two supplies can also be adjusted for direct interfacing to ECL circuitry.

For even higher performance, the



Shortest path. In IBM's low-voltage inverter logic, any path from input by output is delayed by only one transistor (a). Thus LVI circuitry is faster than that built with emitter-coupled logic, but it operates at much lower power levels (b).

circuit can include two bypass capacitors—shown in the figure—that provide overdrive currents. When an input rises, a capacitor temporarily shorts the emitter of the associated input transistor to ground, "allowing it to conduct about 1½ times the norm," he says.

This high current helps discharge the parasitic capacitors along the input-to-output path. When the input falls, the added capacitor stabilizes the emitter voltage, facilitating a quicker turnoff.

Extra capacitors. "Depending on the size of the transistors, the capacitors are somewhere between a half-puff and two puffs (0.5 to 2 picofarads)," says Konian. "They would appear underneath the wiring channels, so they do not add to the gate area." Where it proves impossible to hide the capacitors and space saving is an important consideration, circuits without them will show delays that are about 200 ps more.

Konian cannot yet speak about IBM's plan for the new logic form, but he does hold that it can replace ECL for any application, "or even TTL because of the low power dissipation." A simpler structure than those of the other two bipolar technologies, LVI circuitry may be a prime candidate for very large-scale integration.

Test equipment

System helps create production tests

Engineers at Xerox Corp.'s Electronics division have put together a $5,000 benchtop system that cuts the time needed to generate programs for production testing by 75% to 80%. FAST, for functional algorithmic simulator-tester, is designed for the development engineer, automating the task of creating the truth table that represents the test stimuli and desired responses and saving it in a very deep memory.

The development engineer programs in assembly language a set of stimuli for an integrated circuit he plans to use in a system—or, for that matter, for an IC that he is designing. Since he is the person most familiar with the component and its intended use, his creation of the test programs saves the time it would take a test engineer to learn and translate the stimuli information into a test program.

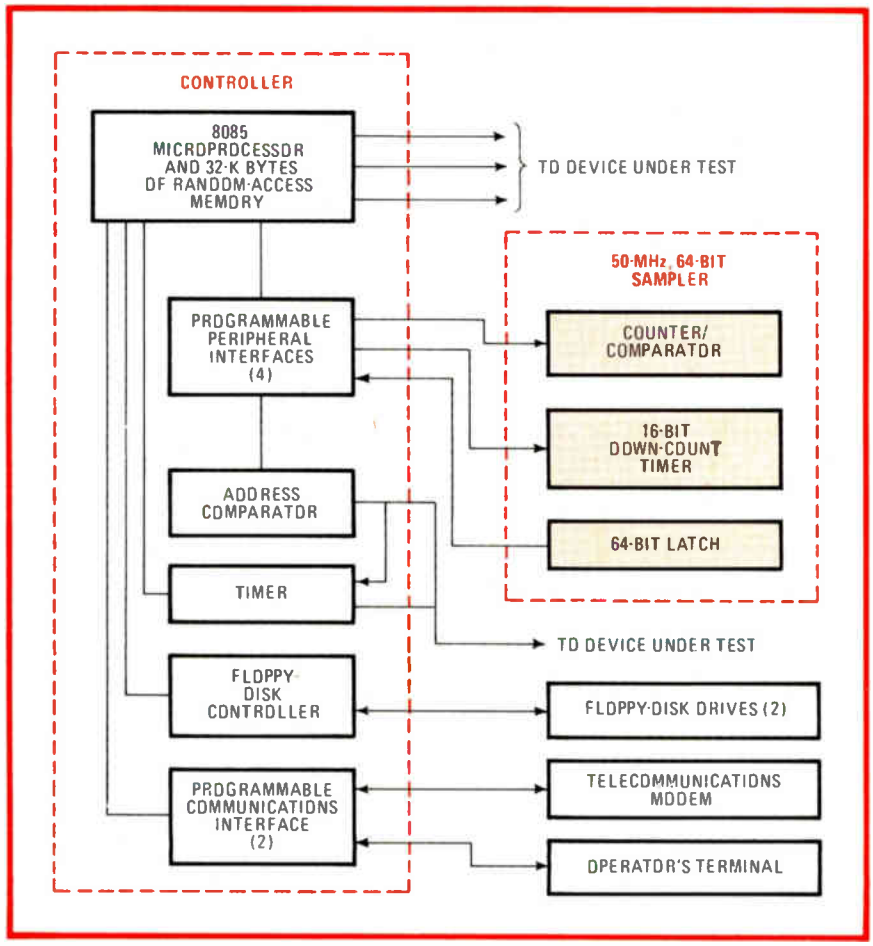
The use of assembly language is important, says James Lindwedel, manager of the El Segundo, Calif., division's large-scale integrated component engineering unit. "Engineers don't want to get involved with all that binary pattern stuff," he explains. "But, typically, they know assembly language or can pick it up."

Time-saver. The FAST project group, of which he was a key member, knew that writing the binary code for the average production test system could take eight man-months, and program writing for a comparison tester working with a known good IC cuts only two man-months from that. With the FAST system, engineers were creating test software in only six man-weeks, including the time to make the hardware interface.

Licensing. Xerox does not plan to offer FAST as a product, but it will license the plans. Similar products are in development at major test-equipment makers, who are not ready to talk about them.

The system is divided into two major subsystems (see figure). The controller turns the assembly-language stimuli into binary code and applies it repeatedly to the device under test. The sampler unit can grab 64 pins' worth of data, both stimuli and responses, for each pass through the test.

The data for each pass is stored on



FAST samples. Xerox's Electronics division has developed a functional algorithmic simulator-tester to create production-line test programs with the aid of the development engineer.

dual 128-K-byte floppy disks, in effect making FAST a 64-channel logic analyzer with a memory depth of 32,000 samples (or about 50,000 samples with data reduction of identical passes). The controller can format this data into a truth table for production testing. It also can send the data to a computer for translation for a production test system.

The major challenge in building FAST was creating the pseudo-50-megahertz sampling system, says George Eldridge, a member of the division's engineering staff. "There weren't any 50-MHz real-time logic analyzers with 64 channels at that time [early 1979] or any with the memory depth we wanted," he says.

Looping. So Eldridge built a unit that, by exercising the IC in a loop, can pick up samples as little as 20 nanoseconds apart in successive passes. It employs Schottky logic for high speed and a look-ahead technique for setting up data capture. Using a state-of-the-art logic analyzer to build a similar system is now possible, but it would be expensive overkill in such a dedicated application, he says.

FAST also can be employed for system-level testing when ICs of a given type are found to be failing. The unit is attached to a properly working on-board chip; and then it exercises the system repeatedly in the mode in which the failure occurred. The data that has been gathered in this way may be used in a production-line tester to screen out ICs that will not work at the system level. **-Richard W. Comerford**

Materials

No shortfall now in polysilicon

Remember that polysilicon shortage predicted to hit semiconductor makers in late 1980? "It's pretty much gone away," admits the industry consultant who most loudly warned of an impending shortfall.

Important but unanticipated changes on each side of the supply and demand equation combined to allay the shortage spectre, says Daniel J. Rose, president of Rose Associates, Los Altos, Calif. His prediction of a year ago [*Electronics*, Feb. 14, 1980, p. 45] was based on moderate supply increases on the part of the polysilicon producers coupled with much sharper hikes in demand from the semiconductor makers.

Demand drops. The current slump in semiconductor orders has blunted the feverish pace of the 30% to 40% annual projected growth in demand for polysilicon. "The late 1980 crunch was predicted on that, as a worst-case scenario," says Rose. He predicts back-to-back 14% growth for 1981–82.

The other unexpected development was a big jump in production on the part of the polysilicon suppliers. The 1980 boost amounted to 20%, instead of the 10% or so expected by most everyone, he says.

Here, the credit must go to rapid industry response to "customers putting heavy pressure on suppliers," Rose says. European and Japanese polysilicon producers especially came up with more of the basic material faster. In fact, Japanese suppliers are moving to become a major factor in world markets.

After charting a revised supply and demand balance through 1983, Rose is confident of a 10%-to-15% excess of polysilicon—"no great margin," however, if device orders should suddenly soar. Fortunately, a worldwide rapid buildup of polysilicon manufacturing capacity in both new and expanded facilities is coming—although new plants take two to three years to start up.

By 1984, Rose thinks, capacity will jump nearly 80% from 4,420 metric tons at the end of 1981 to about 7,840 metric tons. His projections are based on his knowledge of suppliers' plans, including some not yet announced. "Every major producer is adding 500 to 1,000 tons extra," he notes.

Japan's role. As in so many other areas of electronics, Japan is assuming a new importance in the materials business. With marketing techniques that Rose calls "a quiet invasion," Japanese materials firms have boosted their share of the world market from 8% in 1977 to more than 20% and could easily grab a third of the total by 1985. In addition to silicon, ceramics, thick- and thin-film pastes, and other materials are included in these figures, he says.

U. S. suppliers, such as Hemlock Semiconductors Inc. (see "Major U. S. supplier expands") and Monsanto Co.'s Electronics division, can be expected to counter the Japanese invasion with increased production capacity. Also, European polysilicon

Major U. S. polysilicon supplier expands

One indicator of the speed with which polysilicon makers moved to fill the demand gap last year is the nearly 30% production jump reported by the major U. S. producer, Hemlock Semiconductor Corp. What's more, the Hemlock, Mich., firm will add more than 20% this year and is "looking at further expansion," depending on what the market does, according to sales specialist Daniel C. Closs. Though last year's jump took place in existing production facilities, a newly renovated polysilicon plant will go on line next month. It was closed in 1977, but the decision to upgrade was made last year when a shortage loomed, he says.

Prices are at the $75-per-kilogram level, up from $65 a year ago. After factoring in inflation, the price hike does not amount to much—yet last year most industry hands argued that substantial price hikes were needed before the polysilicon makers would invest in additional capacity.

A jointly owned subsidiary of Dow Chemical Co. and Corning Glass Works, Hemlock gained market position in the past year by increasing production to the point where it nearly equals that of long-time leader Wacker Chemitronic GmbH, sources say. Wacker is said to have had a third of last year's $270 million world market, with Hemlock taking a quarter of the market before it began its jump in output.

makers are expanding in the U. S.

A new entrant will be Dynamit-Nobel AG, a member of the West German Flick group and recently the buyer of the Italian polysilicon manufacturer SMIEL SpA. It plans a plant in the U. S. Southeast. Also, West Germany's Wacker Chemitronic GmbH will be bringing a Portland, Ore., polysilicon facility on stream at its Wacker Siltronic Corp. wafer-processing subsidiary.

The new plants are virtually all slated to use the conventional Siemens polysilicon process, rather than any newer technology, Rose points out. Hesitation over pushing ahead last year stemmed from the chance the U. S. Department of Energy would come up with a process that was cheaper and better, but this has not materialized. **-Larry Waller**

Consumer

Toy firms cautiously consider speech chips, as list of talking products starts to grow

A small but growing band of toymakers is embracing speech synthesis as a means of adding extra appeal to their wares. At last week's annual Toy Fair in New York, many manufacturers were talking about putting speech in their products, but only a handful have thus far done so.

The talking toys at the fair scheduled for general introduction this fall use speech-synthesis chips from varying manufacturers. Their makers are divided into two camps—those exploiting the feature purely for its entertainment value and those using it as an educational tool.

Caution. For the most part, the traditionally conservative and price-sensitive toymakers are cautiously approaching this latest high-technology offering from the electronics field. For one thing, the feature adds from $15 to $20 to their unit costs.

Also, "it's very hard to find a product that can use speech synthesis. It's almost a novelty application now," says Anthony Clowes, president of Entex Industries Inc. "When the cost comes down and some improvements in the technology are made, there'll be more products on the market."

Nevertheless, his Compton, Calif., company introduced its first speaking product at the fair. The $60 Do As I Say issues instructions for pressing a combination of buttons in sequence. The players—as many as four—score points if they correctly repeat the sequence. Entex's unit uses a National Semiconductor SPC speech chip.

The first denizen of the toy world to use speech for its entertainment value was last year's $60 phrase-matching game called Milton. Now its developer, Milton Bradley Co., is offering the $40 Say It Again Sam, a bingo-like card game.

"Whether speech synthesis is a big hit or fizzles depends on the application," says James A. O'Connell, vice president of research and development for the Springfield, Mass., company. "It's not a technological challenge to create the products now. The onus is on the creative people." Milton Bradley is developing its speech chips in conjunction with Speech Technology Corp. and General Instrument Corp.'s Microelectronics division.

Catch-up. Another prominent toymaker, Mattel Inc., is working hard to catch up on speech synthesis. Its Hawthorne, Calif., Mattel Electronics division is doing much of its own development work, although speech-synthesis pioneer Texas Instruments Inc. has been lending a hand.

Later this year, the company will add a speech module to its Intellivision line, which at base level is a package of electronic video games and at the high end is a personal computer. Next year, it will add speech to its tabletop toys.

Already shown is another video

Soulmates. The K-2-8 Talking Learning Computer comes in two versions: for computer stores and for toy departments (inset). Only the packaging differs.

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game package that incorporates speech. Mego Corp. brought its $220 Video Voice System to the fair after introducing it at last month's Consumer Electronics Show. The company is using TI's TMS-5200 speech chip and should have the product on the market later this year. The unit uses the home TV set for both display and sound, and the New York company says it will offer game, sport, and educational cartridges.

Firmly in the educational camp is Tiger Electronic Toys Inc. The Mundelein, Ill., company is introducing a three-member family of learning aids selling for $25 and more and aimed at tots to preteens.

Learning tool. The products, built around Votrax's SC-01 synthesizer chip, include the K-2-8 Talking Learning Computer (see photograph on p. 44). Math, spelling, and reading modules will be available with the $99 K-2-8, intended to be an all-in-one counter to the various TI products derived from its pioneering Speak & Spell.

In its own talking products, TI plays up speech as an educational enhancement worth the extra cost. But it thinks speech can succeed across the board in the toy world.

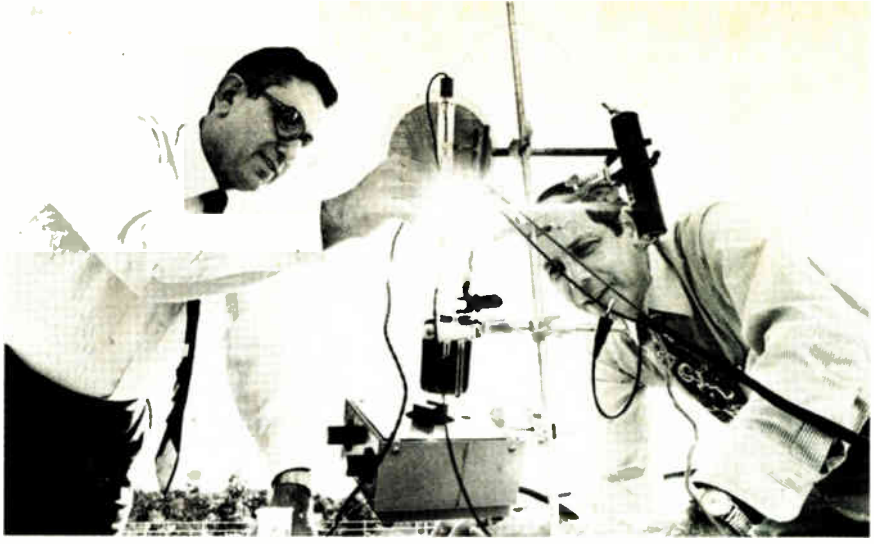
"To people who are in the toy business, price is such an issue. If speech-based products are . . . properly positioned, they will sell," says Randy N. Robinett, merchandising manager for TI's Lubbock, Texas, Educational Products division. "We can justify the [entry] price of speech synthesis by taking advantage of the learning curve."

-Pamela Hamilton and Gil Bassak

Photovoltaics

Liquid-junction cells move in on silicon

Researchers at Bell Laboratories are shedding new light on the problem of building photoelectrochemical solar cells that combine efficiency and corrosion resistance. Using single-crystal indium phosphide, they have built an experimental semiconductor liquid-junction solar cell that converts light into current with an 11.5% efficiency while avoiding surface oxidation.



Teamwork. Adam Heller (left) and Barry Miller are part of a Bell Labs team that has devised a liquid-junction photocathode solar cell with 11.5% efficiency—comparable to silicon cells'.

Thus the six-year-old technology has yielded a chemically stable liquid cell with efficiency levels comparable to those of the classic silicon photovoltaic cell. In a liquid-junction solar cell, semiconductor electrodes are immersed in electrolyte solution, and the action induced by sunlight produces an electric current.

Bell Labs' new cell could not be mass-produced economically, stresses Adam Heller, head of the electronic materials research applications department at Bell Labs in Murray Hill, N. J. Indium is much too scarce and expensive, he notes.

A contender. Nevertheless, Heller thinks the liquid-junction technology could reach solar cell price goals set by the U. S. Department of Energy faster than the silicon solar cell, developed originally by Bell Labs in 1954. The DOE's photovoltaic systems program calls for solar cell module prices between 15¢ to 50¢ per watt by 1990 [*Electronics*, July 19, 1979, p. 106].

So the next challenge for the Bell research team will be to adapt the technology to a cheaper semiconductor material. Finding that alternative will be "an extremely nontrivial task," as one solar cell researcher at another lab puts in.

Heller is quick to caution that mass production may be as much as a decade away, but he also notes between 20 and 30 research groups around the world are working on liquid-junction cells. "It's extremely likely that within the next few years there will be inexpensive materials developed," he ventures.

A photoelectrochemical solar cell's electrodes are immersed in a solution containing two ions, one of which is in a higher oxidation state than the other. Sunlight is allowed to illuminate one electrode—either an n-type photoanode or a p-type photocathode—thereby forming electron-hole pairs.

The holes within a photoanode are attracted to its surface, where they oxidize the solution. The electrons flow in the opposite direction, passing through a resistance before flowing to a counter electrode where they reduce the solution. Thus there is no net chemical change in the system.

With a photocathode, the opposite reduction takes place, and drawing electrons to the cell-electrolyte junction prevents the oxidation of the cell surface that shortens the life of the photoanode-based cells. Unfortunately, the photocathode cells have exhibited much less conversion efficiency, a drawback some researchers believed to be inherent.

Solution. "What we have solved . . . is the surface recombination problem," says Heller, who headed the Bell research team that included Barry Miller, Hans J. Lewerenz, and Klaus J. Bachmann. The recombination of electrons and holes on the surface of the photocathode has been the primary cause of the inefficient conversion of photocathode cells.

The researchers form a single atomic layer of oxide over the p-type cell's surface, and it significantly

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Switching power transistors in TO-3

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	V_{CEO} (V)	$I_{C(sat)}/I_{B(sat)}$	P_{tot} (W)	$t_{f(typ)}$ at $I_{C(sat)}$ (μs)
2N6306/7/8	250-350	3/0.6	125	0.3
2N6542/3	300-400	5/1	100	0.3
2N6544/5	300-400	5/1	125	0.3
2N6546/7	300-400	10/2	175	0.3
2N6671/2/3	300-400	5/1	150	0.3
2N6674/5	300-400	10/2	175	0.3
BUR 23/4	325-400	20/4	250	0.4
BUW 32(PNP)	400	5/1	125	0.3

HIGH CURRENT NPN

	V_{CEO} (V)	$I_{C(sat)}/I_{B(sat)}$	P_{tot} (W)	$t_{f(typ)}$ at $I_{C(sat)}$ (μs)
2N5038/9	90-75	12/1.2	140	0.2
2N5671/2	90-120	15/1.2	140	0.1
2N6032/3	90-120	50/5	140	0.3
2N6354	120	5/0.5	140	0.15
BUR 20	125	50/5	250	0.15
BUR 21/2	200-250	25/3	250	0.2
BUR 50	125	70/7	350	0.1
BUR 51/2	200-250	50/5	350	0.25

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News briefs

RCA communications unit looks to new horizons

RCA Corp. may be pondering an entry into the high-speed communications business. It has just announced a newly formed subsidiary, RCA Communications Inc., to serve as a holding company for the New York firm's existing communications businesses and to develop new communications services. A company spokesman acknowledges that a soon-to-be-created subunit, RCA Network Services Inc., will have the initial task of expanding the corporate voice and data network into a nonregulated business. Though proposed offerings like AT&T's Advanced Communications Service and Xerox's Xten would be regulated under present law, some industry observers expect those constraints to evaporate. The new subsidiary will incorporate RCA American Communications Inc. and RCA Global Communications Inc., whose president, Eugene F. Murphy, will move up to head RCA Communications Inc.

IBM weighs into the relational data-base game

Joining such suppliers as Tandem Computers Inc., Tymshare Inc., and Control Data Corp., International Business Machines Corp. has introduced its first relational data-management system: Structured Query Language Data System, or SQL/DS. Designed to operate with IBM's hierarchical data-management system DL/I DOS/VS, the new offering from the White Plains, N. Y., Data Processing division can extract data from the DL/I data base and insert it into its own tables.

slows the electron-hole recombination. The Bell Labs cell immerses the single-crystal indium phosphide photocathode in a solution that uses vanadium dichloride and vanadium trichloride as the ion couple in aqueous hydrochloric acid.

Heller points out that liquid-junction semiconductor cells might be made of deposited polycrystalline material that may be 100 times cheaper than the single-crystal or large-grain materials that present silicon solar cells require. Bell has reached 7.8% efficiency with a photoanode cell employing thin-film polycrystalline gallium arsenide deposited on a graphite substrate, he says. -Wesley R. Iversen

Displays

Computer line art looks like 3-d image

A display technique an illusionist would admire is behind Genisco Computers' development of a system that will show three-dimensional images but uses a two-dimensional format. The Costa Mesa, Calif., division of Genisco Technology Corp., which produces graphics display equipment, is already well along with a system that turns line-drawing data in computer-processed form into a 3-d–like image.

Setup. The drawing is produced on a cathode-ray-tube display whose image is focused onto a vibrating mirror to give the 3-d effect. The concept, called SpaceGraph, was developed several years ago by Bolt Beranek & Newman Inc., the Cambridge, Mass., research, development, and consulting firm. Genisco got an exclusive license for SpaceGraph about a year ago and has put together a financing package that began with a tax-sheltered limited partnership, an increasingly popular route for electronics firms [*Electronics*, Jan. 17, 1980, p. 40].

SpaceGraph uses a mainframe data base of digital representations of objects. This data may be obtained, for example, from seismic investigation of the earth's geological strata or from X-ray probings of cross sections of the human body. Successively deeper layers of the digital representations add up to the seemingly rounded image.

A PDP-11/34 minicomputer processes the images and sends them to a high-resolution CRT display. The CRT image, on an overhead assem-

bly, is focused onto a mirror facing the viewer.

The round, flexible plastic mirror vibrates, driven by air pressure created by a woofer just like those in the best audio systems. In SpaceGraph, the woofer is controlled by the minicomputer.

The back-and-forth vibration varies the focal length of the image, itself changing at a rate of five layers a second. The mirror has a 3-millimeter vibration arc, which creates an apparent image depth of some 25 centimeters. An anisochronous clock compensates for the sinusoidal vibrations of the mirror.

The thrust of Genisco's development effort is toward increasing the system's data-handling capacity, improving the CRT, and doing the engineering to turn the prototype into a production item. SpaceGraph is attracting attention from oil companies, which use seismic exploration data to create 2-d line drawings of the earth formations; from hospitals, for use with computerized axial tomography; and from the military, for use with reconnaissance data.

Shipments are planned to begin in late 1981, with the first units expected to cost about $100,000 apiece. By then Genisco may have designed its own minicomputer to run the system, since the expanded processing capacity will push the 11/34 to its limits. **-Larry Waller**

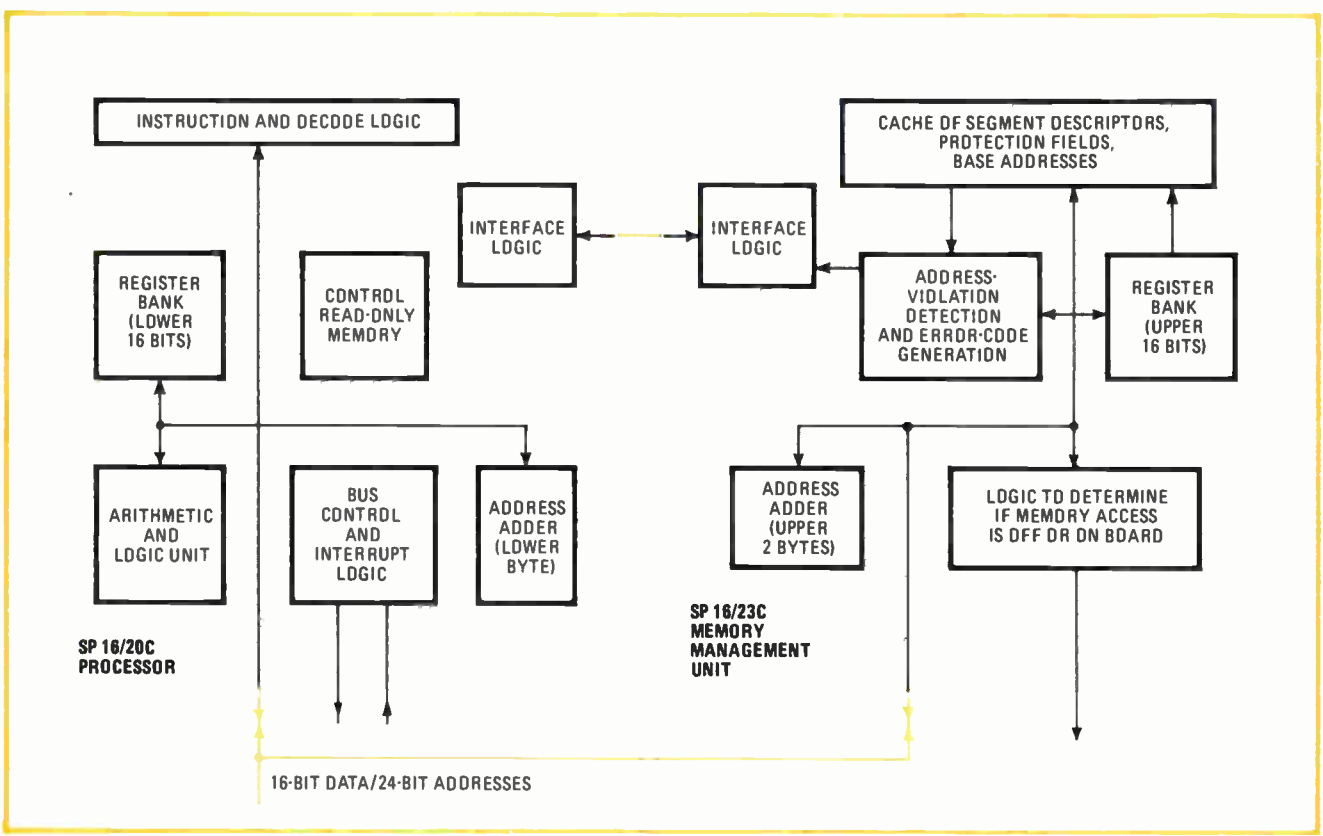
Microsystems

16-bit processor runs mini's instructions, addresses 4-gigabyte virtual memory space

With an eye to updating its minicomputer line, Philips Gloeilampenfabrieken is developing a 16-bit microprocessor that implements a large virtual memory. When Philips completes its chip set, it will in effect have a minicomputer in very large-scale integrated circuits.

Working closely with their Signetics Corp. affiliate, engineers at Philips Data Systems of Apeldoorn, the Netherlands, have designed a two-chip set (see figure) built in an n-channel MOS process with 3.5-micrometer minimum features. The set [*Electronics*, Jan. 13, p. 34] is software-compatible with the Philips P800 minicomputer family.

The processor has a virtual memory space defined by a 32-bit-wide address, "which means the user sees an address space of 4 gigabytes," says Frans C. Schiereck, manager of electronic development for Philips Data Systems. That is four times the virtual address space of Intel Corp.'s forthcoming iAPX-286 16-bit processor [*Electronics*, Nov. 20, p. 42]—but the 286 is a single-chip part. The virtual memory capability lets the



Teamwork. Philips uses two chips for its 16-bit microprocessor, software-compatible with its minicomputers. The memory management unit addresses 4 gigabytes of virtual memory. It works with the processor to come up with the 32-bit-wide addresses.

NO. 22

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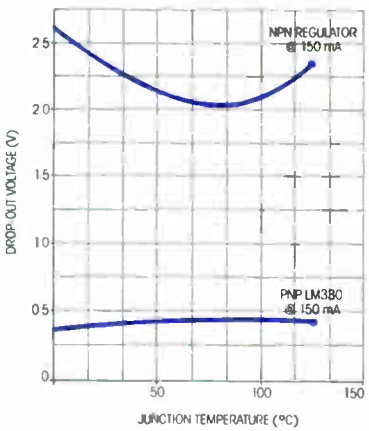
Longer system life with the new LM330 voltage regulator.

A striking reduction in drop-out voltage extends battery life beyond old limits.

The new LM330 offers the lowest drop-out voltage of any fixed regulator on the market: 0.32V at 150mA. So instead of requiring 7.0V to operate (as do standard regulators), the LM330 provides a 5.0V output even when the input voltage dips as low as 5.32V.

As a result, the useful life of the battery is much longer with this advanced new voltage regulation and system efficiency is significantly improved.



National's better way. To accomplish this feat, National's LM330 incorporates a pnp transistor enhanced by a deeper diffusion of the p-type material. This provides a higher current gain in the series-pass regulators.

Both the LM330 and its sister version, the LM2930 (designed primarily for automotive applications), feature this new pnp process (see the pnp technology article).

Efficiency plus. Because the LM330 has a lower drop-out voltage, it runs cooler, and thus more reliably.

Since system designs using the LM330 won't need as much heat sinking the designer can now cut his costs to a minimum by using lower power/voltage components.

Ultimate system protection. This $.70* part protects other expensive devices by preventing both high voltages and negative voltage from getting through. The LM330 also offers protection against reverse battery, mirror image insertion, automotive load dump and input voltage transients.

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Higher gains from deep base diffusion.

The Practical Wizards once again display their linear leadership. This time, they've improved the current gain on pnp transistors in voltage regulators by using a deeper base diffusion of p-type material (see diagram below).

When applied to their new LM330 and LM2930 5V fixed regulators, the enhanced pnp transistors result in a striking reduction in the IC's drop-out voltage.

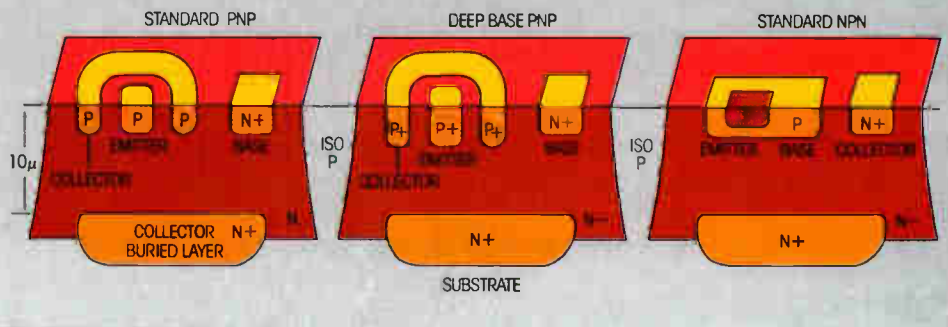
So rather than requiring a 2V input-to-output differential, National's new regulators have a typical drop-out of only 0.32V at full-rated current (150mA). This allows the LM330 to operate at a much lower input voltage, resulting in reduced power dissipation and improved reliability through lower chip operating temperature.

Plus, they offer intrinsic protection that npn-type voltage regulators can't match: reverse input voltages up to 30V, voltage overload, thermal overload and short-circuits.

So even if the 3-terminal regulators have been inserted backwards – which is not uncommon for TO-220 packages – they're fully protected from burning out.

All thanks to the linear experts.

Unlike the relatively shallow diffusions of the npn or standard pnp transistor, the deeper diffusions of the p-type material offer higher current gain in series-pass voltage regulator ICs.



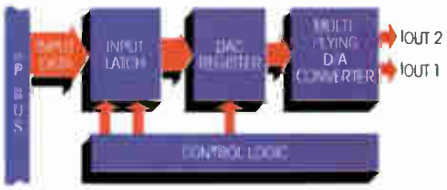
New μP-compatible converters bridge the gap from D to A.

National's line of low-cost 8-, 10- and 12-bit CMOS MICRO-DAC™ converters are double-buffered for maximum versatility.

The number of microprocessor-based designs requiring digital-to-analog conversion is increasing at an incredible rate.

In response to this demand, the linear wizards are now offering a full line of low-power CMOS D/As that interface very easily to any 8- or 16-bit μP bus. These double-buffered converters contain both an input latch and DAC register plus all the μP logic necessary for simplified design and reduced board space.

DOUBLE BUFFERED MICRO-DAC CONVERTERS



And since they're all monotonic with differential non-linearity specified over temperature, they fit particularly well in either fixed or multiplying reference applications such as servo control or synchro-to-digital converters. Thanks to their low cost, these new 8-, 10- and 12-bit D/As can also be used as programmable gain amps, digital attenuators, band-pass filters and more.

All digital inputs are TTL-compatible for more extensive interface flexibility. Their 20-pin (.3" wide) packaging keeps board space usage down while their 20mW power consumption – a factor of 10 lower than bipolar – extends battery life in portable equipment.

The high accuracies obtained by using these devices is due to their "end point" linearity: just set zero and full scale and linearity is met.

And to make them even more versatile, National's 8-bit DAC0830/31/32, and 12-bit DAC1230/31/32 D/As have identical pin-outs for easy interchangeability.

For complete details on the entire line of low-power MICRO-DAC converters, check boxes 051 and 057 on this issue's National Archives coupon.

At National, the practicality keeps on coming through.

MICRO-DAC is a trademark of National Semiconductor Corporation.

PRODUCT SUMMARY TABLE

PART NUMBER	DIP SIZE	RESOLUTION (BITS)	ACCURACY (% OF FSR)
DAC0830	20	8	0.05
DAC0831	20	8	0.10
DAC0832	20	8	0.20
DAC1000	24	10	0.05
DAC1001	24	10	0.10
DAC1002	24	10	0.20
DAC1006	20	10	0.05
DAC1007	20	10	0.10
DAC1008	20	10	0.20
DAC1208	24	12	0.01
DAC1209	24	12	0.02
DAC1210	24	12	0.05
DAC1230	20	12	0.01
DAC1231	20	12	0.02
DAC1232	20	12	0.05

Worlds ahead in data acquisition technology.

National Semiconductor, the Practical Wizards of Silicon Valley, is the world's largest supplier of data acquisition components. Over the last year, for example, they shipped over 5 million A/Ds – more than anyone else in the industry.

The key to their lead over the rest of the pack is their high volume production capabilities and extensively broad line, and their commitment to high performance at a low cost. With all of their transducers, amplifiers, filters, MUXs, sample and hold circuits, references, A/Ds and D/As, there's a National part for every application.

In addition, they're the only supplier utilizing technologies of bipolar, CMOS, NMOS and hybrid along with thin-film resistors and laser trim.

This is just a glimpse into what they're up to – designing high technologies into practical high performance data acquisition components.

National, the dedicated leader in data acquisition technology and components.

The intelligent new 8050— generations beyond the 8048.

The new pin-compatible apex of the INS8048 Series carries a full 256 bytes RAM and 4K ROM for the most intelligent single-chip solution to 8048 applications.

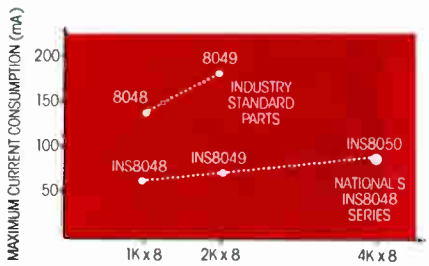
National Semiconductor announces the largest step forward in microprocessor technology since the 8048.

Their new INS8050, with a full 256 x 8 RAM and 4K x 8 ROM, is the industry's first single-chip solution for more complex 8048 applications.

XMOS™ makes it all possible. National's new INS8050s are pin-for-pin architecturally and software compatible with their entire line of 8048 Series μPs. This includes 27 I/O lines (expandable with the INS8243), an 8-bit timer/counter, binary and BCD arithmetic, the same 96 instructions and a built-in clock oscillator.

As a direct replacement for 8048s and 8049s, the 8050 provides a degree of convenient upward flexibility that until now was simply unavailable.

THE INS8050. TWICE THE MEMORY, HALF THE POWER.



And because of their leading edge XMOS technology, the 8050s consume over 50% less power in full operation (max 75mA at 5V) and 12 to 35 times less power in standby mode (8.5mA) than do competitive 8048 series devices.

More speed, intelligence and versatility. National's INS8050 is currently available in a fast 6MHz version with a cycle time of 2.5μsec. An 11MHz version (1.36μsec cycle time) will be available very soon. So an 8050-based design is not only more intelligent and versatile, it's faster too.

And that simply means that an 8050 can do more than any other 8048 series microprocessor on the market. More self and system diagnostics, table look-ups, truth tables and character storage, plus it can perform interpretive commands with a high level language. The list is endless.

Available now at competitive prices. But the 8050 is only one of several microcomputer devices already in production at National – all of which may be programmed using their STARPLEX™ development system with ISE™ (In-System Emulation).

For prototyping or low volume usage, they also offer a ROMless version of the 8050 called the INS8040. And both are available right now at very competitive prices.

The INS8050 breakthrough. Just another reason why they're called the Practical Wizards of Silicon Valley.

Check boxes 029, 037 and 050 on this issue's National Archives coupon for additional literature.

XMOS, STARPLEX and ISE are trademarks of National Semiconductor Corporation

8050 software and hardware emulation made simple.

STARPLEX, National's complete μP development system, with real-time ISE (In-System Emulation) is the time-saving solution for 8050 program development.

Made by the same people who designed the 8050, STARPLEX with ISE includes 32K bytes of real-time map memory, plus all the necessary logic for breakpoints, tracing and memory mapping.

The ISE module uses an 8050 target card that plugs directly into the microprocessor socket on the 8050-based prototype.

The target card approach allows simultaneous emulation of two of the same or even two different microprocessors by the use of dual target cards.

The 8050 ISE can be used to emulate any 8048 series microprocessor. ISE support is also available for the 8070, 8080, 8085 and NSC800 μPs.

All told, STARPLEX is the easiest system for both hardware and software development of μPs, μCs, microcontrollers and programmable logic circuits.

For complete information on STARPLEX, ISE and the 8050 emulator package, circle box 037 on the National Archives coupon.

STARPLEX. The fully developed development system.

What's new from the National Archives?

006 ☐ Special Functions Data Book ($6.00)
029 ☐ INS8050 μP Data Sheet
036 ☐ Optoelectronic Handbook ($3.00)
037 ☐ STARPLEX and ISE Information
050 ☐ 1980 48-Series Microcomputers Handbook ($3.00)
051 ☐ 1980 Data Conversion/Acquisition Handbook ($7.00)
052 ☐ Free Data Update Subscription
053 ☐ 1980 Linear Data Book ($9.00)
054 ☐ LM330-5.0 Fixed Regulator Data Sheet
057 ☐ MICRO-DAC™ Converter Data Sheets
060 ☐ 1980 Voltage Regulator Handbook ($6.00)

Enclose check or money order based upon appropriate currency. Prices shown are U.S. prices only. Make checks payable to National Semiconductor. Allow 4-6 weeks for delivery. This coupon expires on May 31, 1981.

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microprocessor treat every memory location in the system as if it were in the main memory. However, "the translation of the logical to the real addresses in the virtual scheme and the inherent checks normally slow down the processor significantly by the many memory references," Schiereck says.

Speed schemes. To speed up the data fetching, Philips uses microprogramming to load the segment descriptors that identify each page into the cache memory, just as National does with its 16000 family [*Electronics*, April 24, 1980, p. 123]. Also in the interest of speed, the memory management unit performs the necessary checks in parallel with instruction execution.

Philips chose to implement in hardware the checks on residence errors that occur when a particular item needed by the processors is still in off-line memory. What's more, the microprogram checks for residence errors with every instruction, to provide a restart when it is necessary to fetch an off-line item.

"This slightly complicates the microprogram, but it appears far preferable to overhead in the software to check the moment a memory segment is swapped in from disk to line memory," Schiereck says. "It also eliminates the possibility of interrupts occurring between the loading of a segment descriptor and the execution of an instruction in the segment," he notes.

This approach is in contrast to the space-saving tack Intel is taking with the 286, in which memory management is performed by software. Morever, the 286 allows restart only of those instructions that load or store the descriptors.

Addressing. The virtual-memory–addressing scheme is based on 16-bit-wide arithmetic. The 16 bits of the memory management unit's register bank indicate the page location in off-line memory and the 16 bits of the processor chip's register bank give the individual location on that page.

Once the segment is in the 16-megabyte on-line memory, the memory management unit forms a 24-bit real address. It performs an overlapping addition of the 16 bits in the register and the base address of the segment to come up with that 24-bit address.

The address space of the Philips processor is divided into 64,000 segments, each capable of holding from 256 to 64-K bytes. "The flexibility of the segments enables them to comprise a complete software task," Schiereck notes.

Flexible paging. Some 16-bit processors will have a paging system that pulls a fixed block of data into main memory: the Zilog Z8003, for example [*Electronics*, Oct. 23, p. 41]. "This inflexibility leads to a waste of memory space, because a lot of the tasks will ask for pages smaller than the fixed, big size," Schiereck says. However, keeping track of the flexible page sizes does take more processor hardware.

Philips expects to see first silicon on the two chips during the second quarter, with a decimal coprocessor following by year-end and a floating-point coprocessor likely next year. The parts will be made both in Europe and at Signetics in Sunnyvale, Calif., which is doing the layout and initial fabrication.-**Bruce LeBoss**

Industrial

6800 helps monitor steel-rolling process

A 6800-based instrument is easing the job of rolling steel by giving a precise digital readout of the position of the rollers' shafts. As well as displaying data from a selsyn, the SI-500 from ILC Data Device Corp. can feed its information to a computer controlling the process—an important feature in an era of ever-increasing steel-mill automation.

In most U.S. mills, however, a skilled operator controls the rolling through commands to the motors that drive the screws that position the pairs of giant rollers turning slabs of steel into ribbons or sheets. The steel can go through the rollers at speeds up to 6,000 feet a minute, with the operator fine-tuning the rollers' positions in thousandths of an inch.

"In most rolling mills today, mechanical displays such as counters are an integral part of the monitoring system used by the operators,"

CAD system proves itself with VLSI design

The first very large-scale integrated circuit designed using Digital Equipment Corp.'s new Chip Assembler, or CHAS "global" computer-aided design system, is a 77,000-transistor floating-point processor chip (FPP). Designed as a proof-of-principle exercise for CHAS, the complementary-MOS chip may never see the inside of a diffusion furnace, but it gives an idea of the power of the Maynard, Mass., firm's new design system [*Electronics*, Feb. 10, p. 100].

The FPP chip, brainchild of DEC engineers William Herrick and Henry Walker, would occupy relatively little area for its complexity—84,100 square mils, 290 mils on a side—and require more than 80 pinouts.

The chip design has a very high regularity factor—the ratio of its total number of transistors to those designed by hand—of 74 versus about 4 or 5 for commercially available VLSI chips. Higher regularity means that more of the overall design task is handled by computer, speeding design time. DEC spokesmen also note that, compared with the commercial state of the art, the CHAS-aided design uses far less space-consuming random routing.

The FPP chip was designed to implement the full VAX-11/780 floating-point instruction set and to deal with 128-bit binary numbers. The chip's simulated data path cycles in 150 nanoseconds. According to DEC spokesmen, there is no comparable LSI or VLSI device available with this combination of speed and capability. The only realistic comparisons, they say, lie with 400-odd-chip TTL FPPs, which are faster but far less attractive in terms of volume, power dissipation, and design time. **-James B. Brinton**

notes Steven N. Friedman, applications engineer for the company in Bohemia, N. Y. Selsyns feed their positioning information to electromechanical receivers and associated counters: an SI-500 replaces both a receiver and a display.

Position data. An operator must continuously monitor the rollers to ensure that the steel is being rolled to the desired thickness. The SI-500 [*Electronics*, Jan. 13, p. 34] gives real-time positioning data on a five-digit light-emitting-diode readout to ease this task.

The selsyns measure the shaft angles of the screws, and the SI-500's 10-bit synchro-to-digital converter and 8-bit processor convert these measurements, which help the operator determine the relative positions of the two rollers in a pair as the steel goes through.

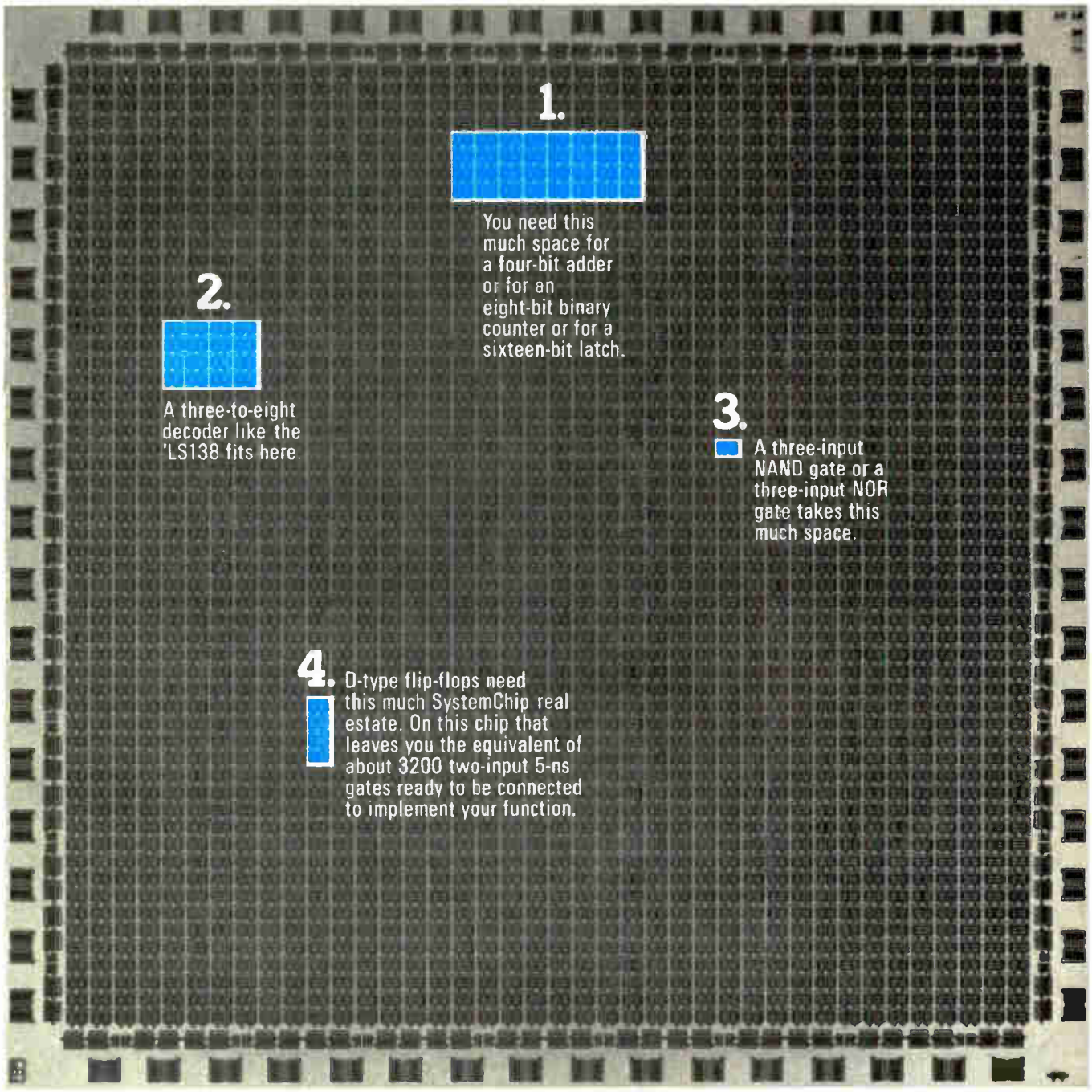
The processor also eases the recalibration of the monitoring mechanism, which must be done every time the roller pairs are changed. At rest, the two new rollers will have a different relationship from the two they replace. Since this resting position is the base from which the positioning data is calculated, it is helpful to be able to show this position as the zero level. The SI-500 has a preset button that takes care of the recalibration.

A further chore the processor can undertake is the scaling of the readout, which expands the relatively small measurements taken by the selsyn. The SI-500 has internal rocker switches that can change the scaling factor; with mechanical displays, a gearbox was often necessary.

Savings. "I can electronically replace the gear box and the selsyn receiver with its mechanical counters at about 70% of the cost," says Robert E. Soden, assistant supervisor of maintenance at the Hot Rolling division of U. S. Steel's Gary, Ind., works. The base price of a single SI-500 is about $2,500, reflecting the cost of making a product for an industrial environment.

Such options as serial or parallel digital data outputs, fiber-optic serial output, and multiplexed 10-wire digital data let the instrument display its data remotely or send it to a

The SystemChip™ Gate Array



Unretouched photo of the new G82240 gate array before metalization.

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Electronics review

computer. The American steel industry lags behind such foreign counterparts as the Japanese in automating its production lines, and a vitally needed computerized catch-up effort is just beginning.

For steel mills with computers, the instrument can serve as a part of a fail-safe system. "I'm using two SI-500s at the slabbing position mill as backup for the process control system. If there's a failure in the main system, we still have a real-position readout," says Frederick C. Miller, programmer for automatic controls at Jones & Laughlin Steel Corp.'s Indiana Harbor Works in East Chicago, Ind. "It's definitely something that the steel industry really can use," he adds. **-Pamela Hamilton**

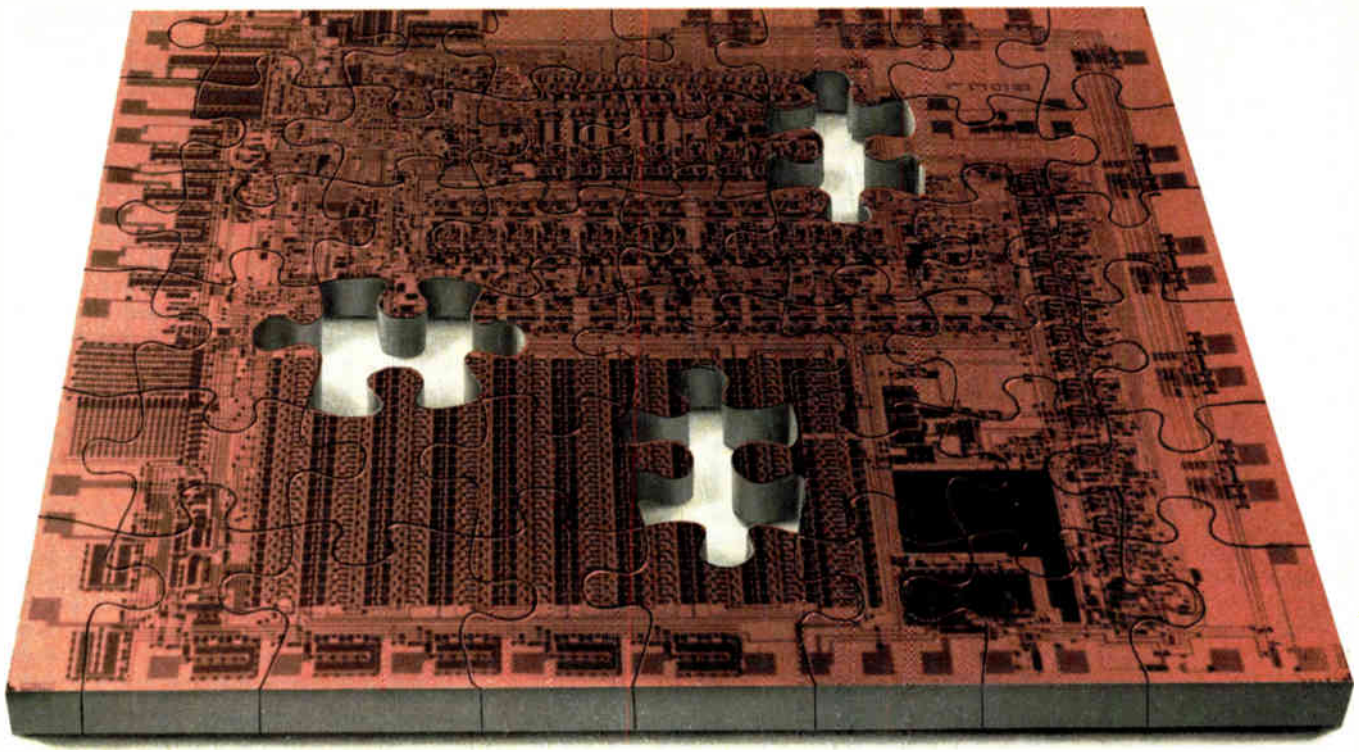
Instrumentation

Microsystem analyzer 'learns' on the job

The Microsystem Troubleshooters now being readied by the John Fluke Manufacturing Co. of Mountlake Terrace, Wash., for a June introduction have been designed for on-the-job learning. The reason is that this family of instruments, which will be marketed as the Fluke 9000 Series, has self-contained intelligence with which it can "learn" the characteristics of undocumented microprocessor-based systems and then test them using compact algorithms [*Electronics*, Feb. 10, p. 33].

The instrument's entry into the system under test is through the socket of the microprocessor, although Fluke will also supply its customers with the information necessary for adaptation to soldered microprocessors. In both cases, the instrument can control the address, data, and control buses, as well as the reset and hold lines.

Learn algorithm. The details of Fluke's complex learn and test algorithms are cloaked in the secrecy of patent proceedings. Simply put, however, the instrument basically increments the system under test through its entire address range,



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The Corporate Research & Development Laboratories is investing $50 million for new facilities to advance the state of the art in VLSI process technology.

The Electronics Laboratory is adding LSI facilities and people to develop CAD software for the company-wide Microelectronics program and to bring monolithic microwave technology to advanced practical applications.

And the Aerospace Electronic Systems Department is developing military VLSI technology and heading the VHSIC effort for leadership in technology, processes and products.

We're also building new capabilities like the GE Microelectronics Center at Research Triangle Park, N.C. for custom integrated circuits which will be among the nation's most advanced facilities. Although GE will remain a major buyer of standard ICs, this custom capability will add value to our products and enrich our plants and processes with microelectronics-based production tools and systems for even greater reliability and productivity.

If it's new in microelectronics, it's at General Electric, where technological leadership and manufacturing success are standard. At GE, we're putting microelectronics to work.

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GENERAL ELECTRIC

Circle 59 on reader service card

while reading the responses on its bus lines, as well as the chip-select responses. The stimulus is picked from 4-K bytes of read-only memory controlled by 10-K bytes of learning algorithm ROM.

The learning algorithm determines whether the system can both write and read back signals over a given address range. If it can, and if the address range is greater than 256 bytes, then the learn mode labels that address range as random-access memory. If it can write and read back, but over less than 256 bytes of address, then it labels the address range as an input/output port. If the learning mode reads a consistent response over an address range greater than 256 bytes but that response is different from the stimulus routine, then it labels the address range as ROM. If it consistently reads a response for a range under 256 bytes, then it concludes that address range is write-only I/O.

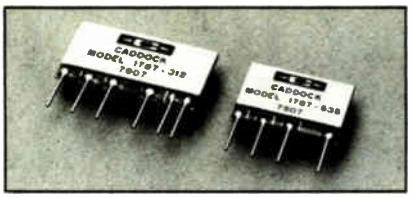
On the model 9010, a tape cassette and RS-232 link can be used to store results and comparison values employed in the learning mode. Model 9020 will add IEEE-488 programmability. The instrument's full keyboard with functional key groupings also helps the user develop guided fault-isolation proceedings in an on-line fashion.

Added probing. The prompting instructions can include directions for using a separate probe, which is contained in the instrument. The probe is capable of signature analysis, as well as event counting and logic probing that is synchronized to address and data information. This last capability is important, because it enables the user to catch a logic state that is linked to others on the fly and display it as though it were static. Coupled with the stimulus algorithms, this feature lets the user observe the toggling of a single bit in the system under test.

The 11-pound troubleshooter can handle 8-bit, 16-bit, and later 32-bit microprocessors. Its price—$3,295 for the basic unit, $695 for each 8-bit pod, and $1,495 for each 16-bit pod—is affordable by most field-service setups. **-Martin Marshall**

Current sensing resistors for multi-range instruments.

NEW



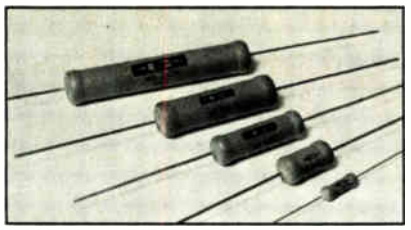
Caddock's Type 1787 Current Shunt Resistor Networks.

Absolute resistance tolerances of 0.25%, 0.1%, 0.05% and 0.02% make these 2-, 3- and 4-decade current shunt resistor networks the ideal replacement for expensive, bulky discrete resistors.

16 standard models are now available. The basic network design provides a series total resistance of 1000Ω , 100Ω , 10Ω and 1Ω . Other standard models provide commonly used variations of this basic design.

For Type 1787 data, circle Number 201.

Non-inductive precision resistors for power switching circuits.



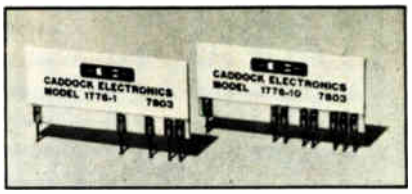
Caddock's Type MS Power Film Resistors.

Caddock's patented Non-Inductive Design in power ratings from 2 watts to 15 watts assures minimum voltage transients in all types of power switching circuits.

High stability Micronox® resistance films operate to +275°C and years-long load-life tests demonstrate extended-life stability better than 0.05% per 1000 hours.

For Type MS data, circle Number 203.

Off-the-shelf precision decade voltage dividers.



Caddock's Type 1776 Precision Decade Resistor Voltage Dividers.

When used as a 10 Megohm input voltage divider, the Type 1776 family can provide high accuracy voltage division in ratios of 10:1, 100:1 and 10,000:1.

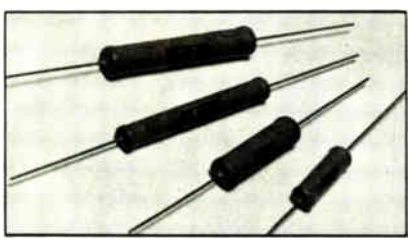
Type 1776 Precision Decade Resistor Voltage Dividers are now available in 25 standard models with ratio TCs from 50 ppm/°C to 5 ppm/°C. Caddock's laser production techniques keep OEM quantity prices low, too.

For Type 1776 data, circle Number 205.

CADDOCK Resistor Technology solving problems across the board!

NEW

High stability resistors for very-high voltage control and measurement circuits.



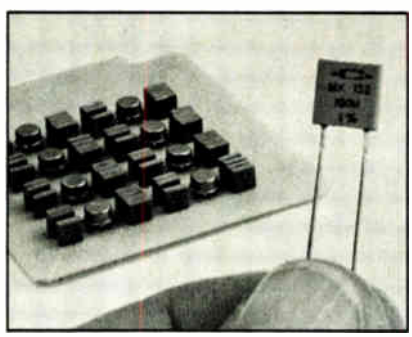
Caddock's Type MG High Voltage Resistors.

High voltage probes and control circuits make wide use of Type MG resistors for precision high voltage regulation and high voltage measurements.

Long-term stability — plus proven reliability — have also made these precision resistors first choice in communications satellite voltage control circuits.

For Type MG data, circle Number 202.

100 Megohms in a miniature package.



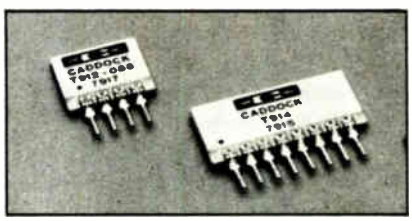
Caddock's Type MK Precision Film Resistors.

Precision values to 100 Megohms in a miniature CK 06 case make the Type MK ideal for low current designs.

These non-inductive resistors find wide application in high-impedance analog circuitry.

For Type MK data, circle Number 204.

Resistor pairs and quads with very low ratio TC.



Caddock's Type T912 and T914 Precision Resistor Networks.

Ratio tolerances to ±0.01%, ratio TCs of 2, 5 or 10 ppm/°C and ratio stability within ±0.01% at full load for 2000 hours provide exceptional stability in precision analog circuits.

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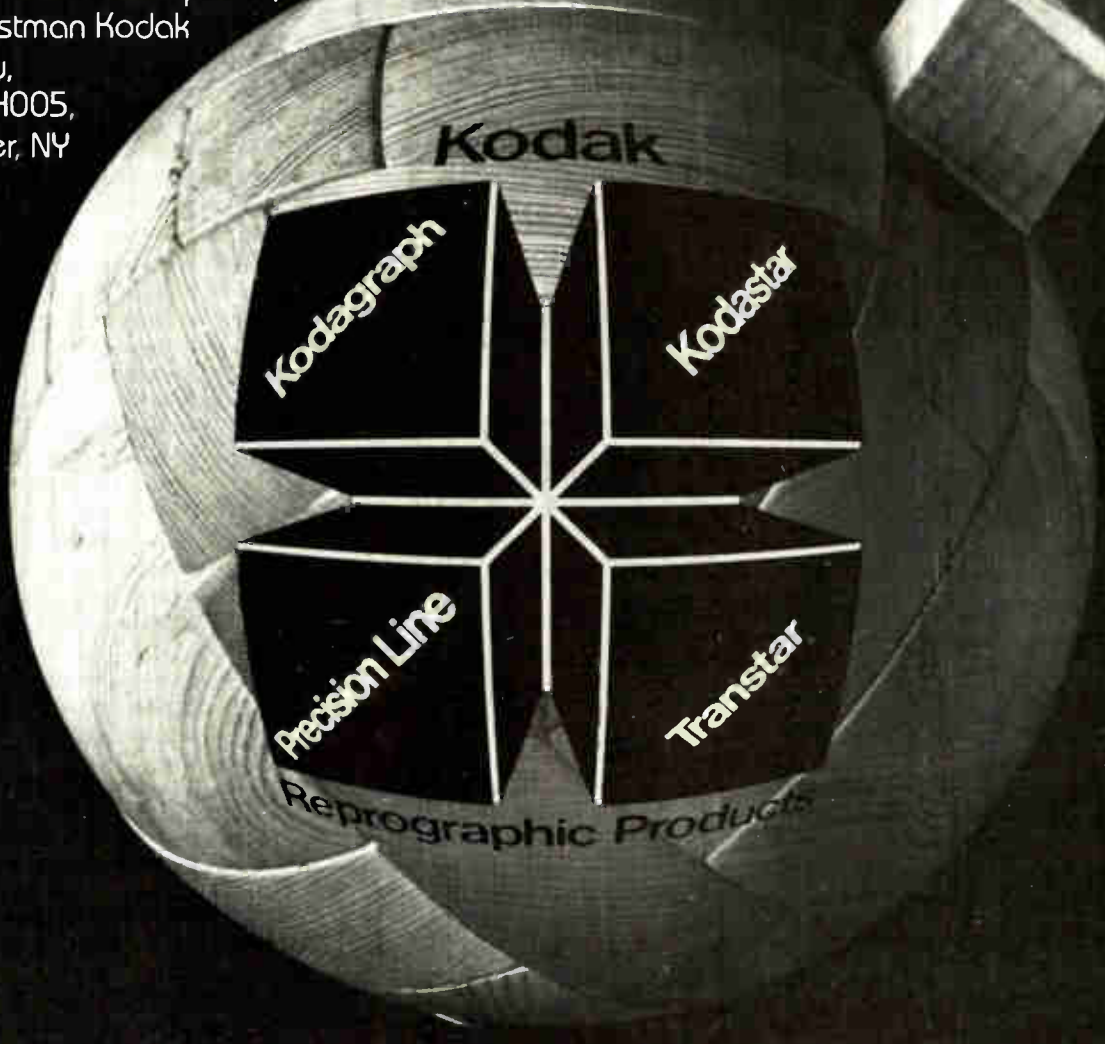

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Washington newsletter

DOD outlays will lag behind bigger budgets . . .

Military spending outlays for fiscal 1981, which ends in October, and for fiscal 1982 will rise by only $1.3 billion and $7.2 billion, respectively, under President Reagan's budget revisions now set to go to Congress on March 10, according to the Office of Management and Budget. The spending levels are lower than anticipated in view of Pentagon reports that increases in its authority to spend total about $12 billion and $25 billion in each of the two years, which will push the respective Defense budgets up to nearly $170 billion and $220 billion. The explanation by Office of Management and Budget sources is that **some of the budget authority will be carried over to be spent in later years** when the Defense Department has a better handle on its priorities. For example, outlays in the fiscal 1983–86 time frame are expected to climb steadily by $20.7 billion in fiscal 1983, $27 billion in 1984, and $50.2 billion in 1985 and to peak with a $63.1 billion increase in fiscal 1986.

. . . as Reagan cuts hit NASA hard

Though program specifics were carefully avoided in the Reagan defense budget revisions during the Office of Management and Budget's Feb. 18 briefing, proposed cutbacks in other agencies with high technology content were spelled out in detail. Outlays for the National Aeronautics and Space Administration, for example, are proposed to be cut $60 million in this fiscal year to $5.22 billion, followed by even sharper slashes in fiscal 1982 and 1983 of $241 million and $334 million, respectively, leaving annual outlays of $6 billion and $6.3 billion in those years. Fiscal 1985 and 1986 outlays are $5.7 billion and $5.3 billion. The space shuttle and the Orbiting Space Telescope systems remain intact, **but the agency stands to lose space science missions** such as the Venus Orbiting Imaging Radar, the gamma-ray observatory, and Spacelab experiments, and U. S. participation in the international solar polar mission will be reduced.

NSF could lose funds to upgrade college instrumentation

Funds for the National Science Foundation, which President Carter sought to boost significantly in his fiscal 1982 budget request [*Electronics,* Jan. 27, p. 98], would also be cut back under the Reagan plan. The NSF's annual outlays, which hover around $1 billion yearly, would be reduced by $26 million this fiscal year and by $15 billion in fiscal 1982. **Reductions would continue steadily through fiscal 1986 to a level of $155 million.** On the Office of Management and Budget's hit list this year are instrumentation grants for colleges, as well as selected science and engineering education programs.

Protests greet plan to tax users for FAA, Coast Guard

One novel Reagan cost-cutting approach calls for putting the Federal Aviation Administration and the Coast Guard on a pay-as-you-go basis by invoking new user taxes. The air-traffic control system, for example, would be funded along with other FAA functions by a 20% tax on airline fuel, 9% on tickets, and 5% on freight. Similarly, the Coast Guard would derive new revenues from taxes on yachts and ships that use its services. Already objecting are congressional advocates of Federal funding of these programs and those protesting plans to eliminate Department of Energy research and development for photovoltaics, along with other solar energy R&D, **which the Reagan Administration believes should be left to private industry.** This approach would cut solar programs by 60% in fiscal 1982, says the Office of Management and Budget.

Washington commentary

Military readiness: must reading for Congress

The issues of military force readiness and the U. S. "tooth-to-tail" ratio—combat equipment and manpower versus hardware and personnel support costs—are getting the attention they deserve from the Reagan Administration. And there is evidence that Congress, which ordinarily emphasizes weapons procurement in its annual budget battles, will devote more of its attention to military preparedness, as well.

The most recent sign of increased congressional interest is Senate Appropriations Committee chairman Mark Hatfield's call for a third under secretary of defense, one who would speak for all three services on preparedness and combat readiness and complement the under secretaries for policy and for research and engineering. The Oregon Republican may get his wish since the outgoing Carter Administration was considering just such a move by upgrading the job of assistant secretary for manpower, reserve affairs, and logistics.

Unfulfilled promises

The move is encouraging. Yet Hatfield, his colleagues, and their staffs should also look deeper into the misapplication of the old "bigger-bang-for-a-buck" philosophy of weapons that is spawning increasingly complex equipment. Inadvertently encouraged by Congress, the system produces the expected response from the military services and their contractors—promises of "wonder weapons" that do not always work well.

The resultant technological complexity, however, invariably requires larger maintenance crews, more spare parts, and a proliferation of automatic test equipment—all producing a longer and costlier support tail at the expense of the teeth, combat-ready systems.

Automatic test equipment, long recognized as a problem by industry and the military, was extensively analyzed in a three-year study involving 500 Government and industry specialists [*Electronics*, Dec. 4, 1980, p. 102]. Yet the "Industry/Joint Services Automatic Test Project" is still no more than a voluminous study that is a long way from implementation. It is also a product of narrow ATE interests, rather than a broad view of the readiness issue.

Nevertheless, the military ATE analysis does make a crucial point when it notes that more than 60% of the problems occur in the acquisition and management of equipment, rather than in the technology. Congress should take note, in addition to considering the related problems specified in two smaller, more recent criticisms of readiness developed by the DOD's program analysis and evaluation group and the General Accounting Office (see p. 104).

The DOD's "Defense Facts of Life" is signed by Franklin C. Spinney, who calls it an "independent minority view." He maintains that system complexity is not necessarily the product of advanced technology, but rather of a lack of program discipline. Spinney calls the complexity problem a challenge for leadership, not "management gimmicks," like blue ribbon panels and zero-based budgeting, that "do not work." Such gimmicks, Spinney contends, "have the effect of a placebo rather than a cure—in effect, they contribute to the problem by conveying the false impression of a solution. What is required is leadership than can make real national defense take precedence over the component interests involved in defense."

Top industrial and academic experts in weapons systems indirectly supported that view when they told the GAO that overly complex weapons systems are the product of incorporating too many unproven technological innovations into a single system—an approach that would never be undertaken by any successful company in the commercial and industrial electronics marketplace. Nevertheless, weapons system primes are regularly prodded to propose such multiple advances to achieve the biggest bang for the fewest bucks. Such systems are virtually guaranteed to cost far more than proposed.

Cut paperwork

Contractors argue—correctly, it seems—that they have the "knowhow" to design more supportable systems if the procurement system can be changed to provide them with design responsibility and financial incentives. They also told the GAO that industry's lead time could be shortened and weapon performance improved if the 3,000 pages of Defense Acquisition Regulations and some 27,000 additional pages of procurement rules could be simplified and abbreviated. The Congressional Budget Office concurs on the latter point, saying that regulations increase a major system's cost by 20% to 100%.

With so many disparate interests in agreement, it seems that Sen. Hatfield and his colleagues should use their leadership roles to initiate some significant changes in the system that will make best—if not the most—use of technology in weapons that will work when needed. But without strong support from Congress, one more under secretary of defense simply will not be able to change the system. **-Ray Connolly**

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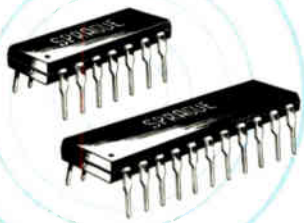

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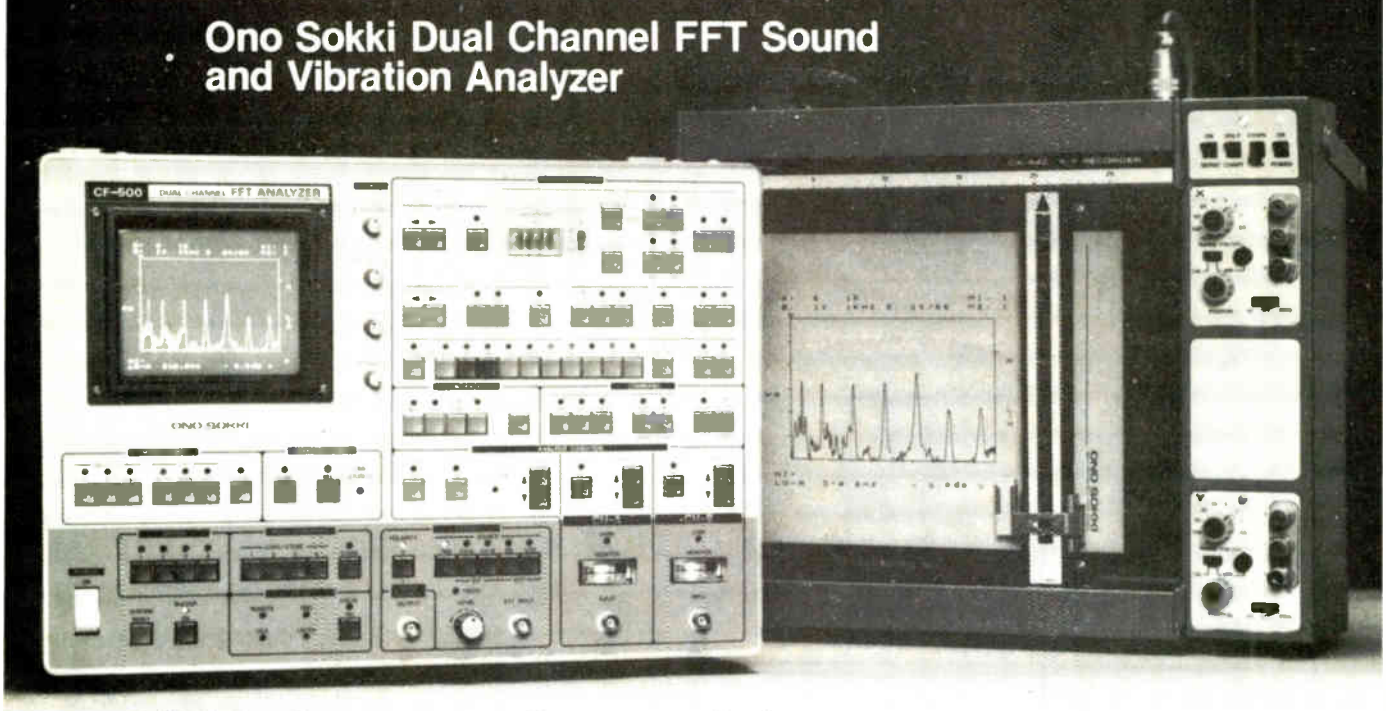

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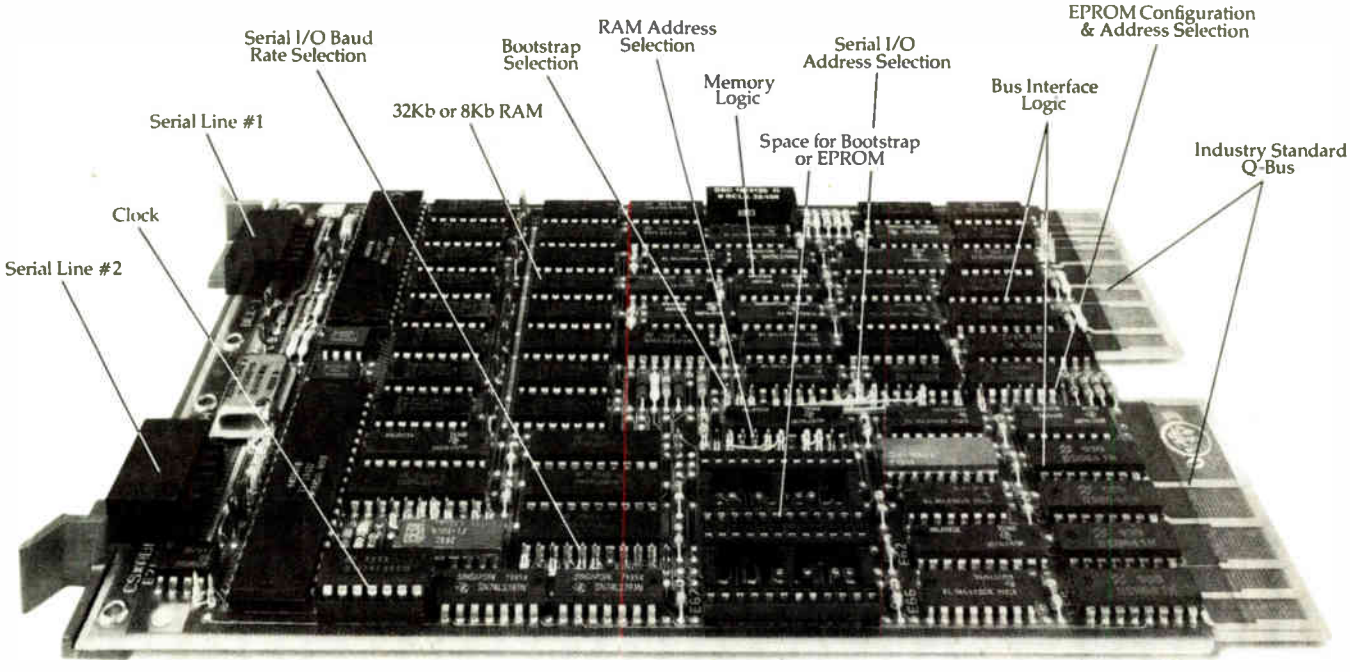

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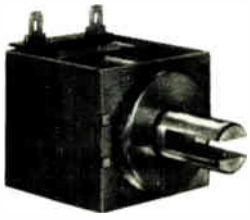

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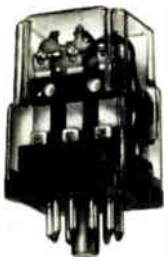

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International newsletter

New Hitachi computer surpasses the 3081

As a single processor with 2.1 to 2.4 times the performance of IBM's 3033, Hitachi Ltd.'s new Hitac M-280H is somewhat ahead of IBM's 3081 dyadic processor, rated at 1.9 to 2.1 times the 3033's performance. The new computer has **8 to 32 channels for an input/output throughput of 90 megabytes/s,** versus the 3081's 24 channels and 71 megabytes/s.

Contributing to those figures are two emitter-coupled-logic arrays built with 2-μm technology. One has a maximum of 550 gates and a propagation delay of 0.45 ns; the other has 1,500 gates at most and a 0.8-ns delay. For control and buffer memories, 4-K and 1-K bipolar memories with an access time of 7 ns are used. The 16-to-32-megabyte main memory is populated with the firm's 16-K dynamic devices that when used in an 8- or 16-way interleave have an access time of less than 100 ns. This hardware gives a single-processor performance of **30 megaflops when the optional array processor for scientific calculations is attached.** Two to four processors may be linked in a multiprocessor configuration.

Monthly rental for the smallest practical system is $195,000. The Japanese company is in the course of negotiating agreements with the firms that sell plug-compatible versions of its machines abroad—National Semiconductor in the U. S., Italy's Olivetti, and West Germany's BASF.

Sinclair flat-screen TV gets volume go-ahead

Success with his ZX80 personal computer—over 50,000 of which were sold in their first nine months of production [*Electronics*, Feb. 14, 1980, p. 80]—together with government agency grants totaling $6 million, has given British electronics entrepreneur Clive Sinclair **the financial resources to fund a four-year $11.7 million program** for putting his flat-screen tube into volume production. Cambridge-based Sinclair Research Ltd. will subcontract the manufacture of both the tube and the microvision radio-TV combination to Timex. In the first, $2.9 million phase, a highly automated flat-tube production line is being built at Timex's plant in Dundee, Scotland. The first product, a multistandard radio-TV combination with a monochrome 3-in. screen and measuring 6 by 4 by 1 in., will debut in the second half of 1982, retailing for around $115.

One-chip codec filter from Canada uses just 15 mW

A one-chip complementary-MOS codec and filter with exceptionally low power consumption is being developed by Mitel Corp. of Ottawa. The company, which manufactures communications systems and associated integrated circuits, is **tailoring its Iso²C-MOS part to its forthcoming SX2000 private automatic branch exchange** for voice and data, but it is likely also to introduce a commercial version. Based on switched-capacitor technology, the ±5-V-to-±8-V, 18-pin part will measure about 145 by 105 mils (3.7 by 2.7 mm), consuming about 15 mW in the active mode and almost nothing in the power-down mode.

Plessey to offer bubble support ICs

After a major redesign of its quad sense amplifier for bytewide magnetic-bubble memory systems, the Plessey Co.'s Allen Clark Research Centre of Caswell, Northants., is now providing British firms and a West Coast company with samples of both this integrated circuit, the SB9001, and the complementary SB9002, a quad write driver IC with integral protection of the magnetic-bubble write circuitry. These two special-purpose support circuits are for **use in the 256-K-byte bubble modules that will go into Britain's System-X all-digital exchange** and the Project Wavell battlefield

information display system. They would also make it easier and more economic to configure custom bubble memory systems, but sister company Plessey Semiconductors Ltd. has not yet decided whether to produce custom bubble boards commercially.

Thinner video tape plays role in VCR-camera battle

As Japan's manufacturers of video cassette recorders vie for the lead in setting standards for combined camera and VCR units, video tape producer Fuji Photo Film Co. has gotten into the act by announcing two new prototype tapes—a metal and a deposited-metal kind. Matsushita's hand in the struggle to become the standard is greatly enhanced by the existence of a second source for deposited-metal tape (see p. 80). For a signal with a recorder wavelength of 1 μm, the respective outputs of the metal and deposited-metal tapes are **13 and 22 dB higher than that of the tape now used for Beta format or VHS VCRs.** For each hour of video recording, 0.25 to 0.3 square meter of the metal tape and 0.125 to 0.15 m^2 of the other is needed. Since their respective coatings are 2.5 μm and 0.15 to 0.20 μm thick, the volume improvement for the deposited-metal tape is still greater—Fuji says enough of it should squeeze into a cassette the size of the standard Philips audio cassette to record for three hours.

VCRs to do well in West Germany

The sector for video cassette recorders continues to stand out as a bright spot in West Germany's lackluster market for entertainment electronic products. According to the Deutsche Video Institut, a newly established video consulting organization in West Berlin, **domestic VCR sales should exceed the $500 million level this year, up from $380 million in 1980.** In terms of units, the figures for 1981 and 1980 are 550,000 and 374,000 respectively.

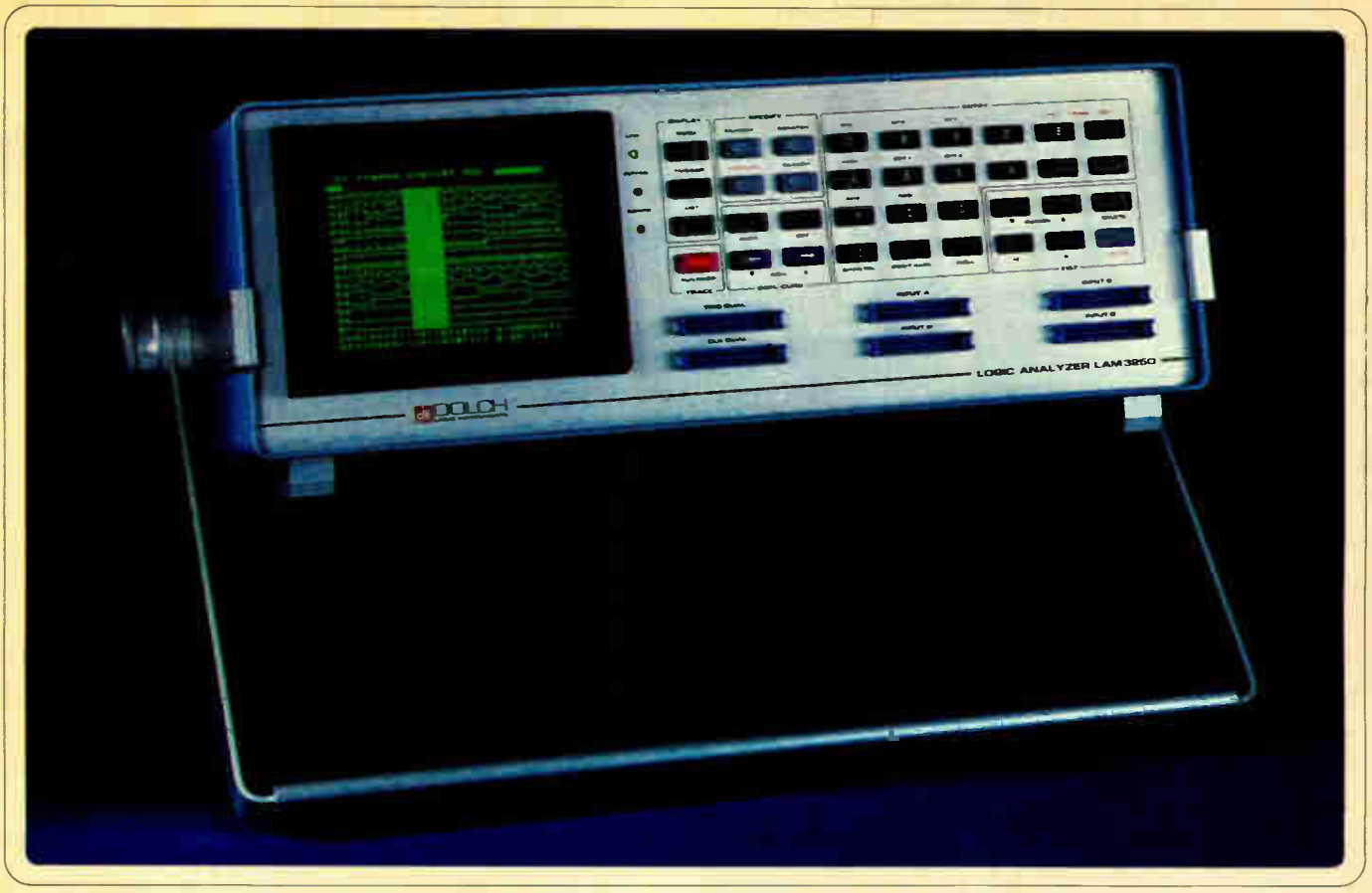
NTT opens doors to new suppliers

Motorola Inc. will become the first U. S. firm to sell telephone subscriber equipment to the Nippon Telegraph & Telephone Public Corp. when purchases of its pocket bell paging units begin on April 1, the start of Japan's 1981 fiscal year. The small, portable devices beep to indicate the subscriber should contact his office. As the market for them has been monopolized by five Japanese firms, next year's orders for 130,000 units will be split six rather than five ways. Motorola's product will be assembled in Fort Lauderdale, Fla.

Meanwhile, **23 foreign and domestic firms have officially applied to take part in open bidding** on nine categories of electronic instruments and other products that till now have been bought only from 21 designated Japanese firms. More firms are expected to apply before the end-of-February deadline.

Canada, Japan, try standards accord

The Canadian Standards Association and its equivalent in Japan, the Electrical Testing Laboratory, have agreed to try a reciprocal testing agreement according to which each country will accept the other's word that standards have been met for such consumer and industrial products as hand tools and appliances. Later more sophisticated gear like communications equipment could be included. **No other country has such an agreement with Japan.**



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Dolch Logic Instruments' third generation logic analyzer, the LAM 3250, lets you meet your troubleshooting needs now, and expand for the future. The LAM 3250 records up to 32 channels of information at sampling rates to 50 MHz, and with optional Channel Expansion Probes, its capability can be extended to 64 channels. And there's more.

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Since it incorporates dual 16-channel X 1000-bit recording blocks, the LAM 3250 can accept up to two independent external clocks for sampling data, letting you independently monitor both address and data on a multiplexed bus.

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Check these features and compare:
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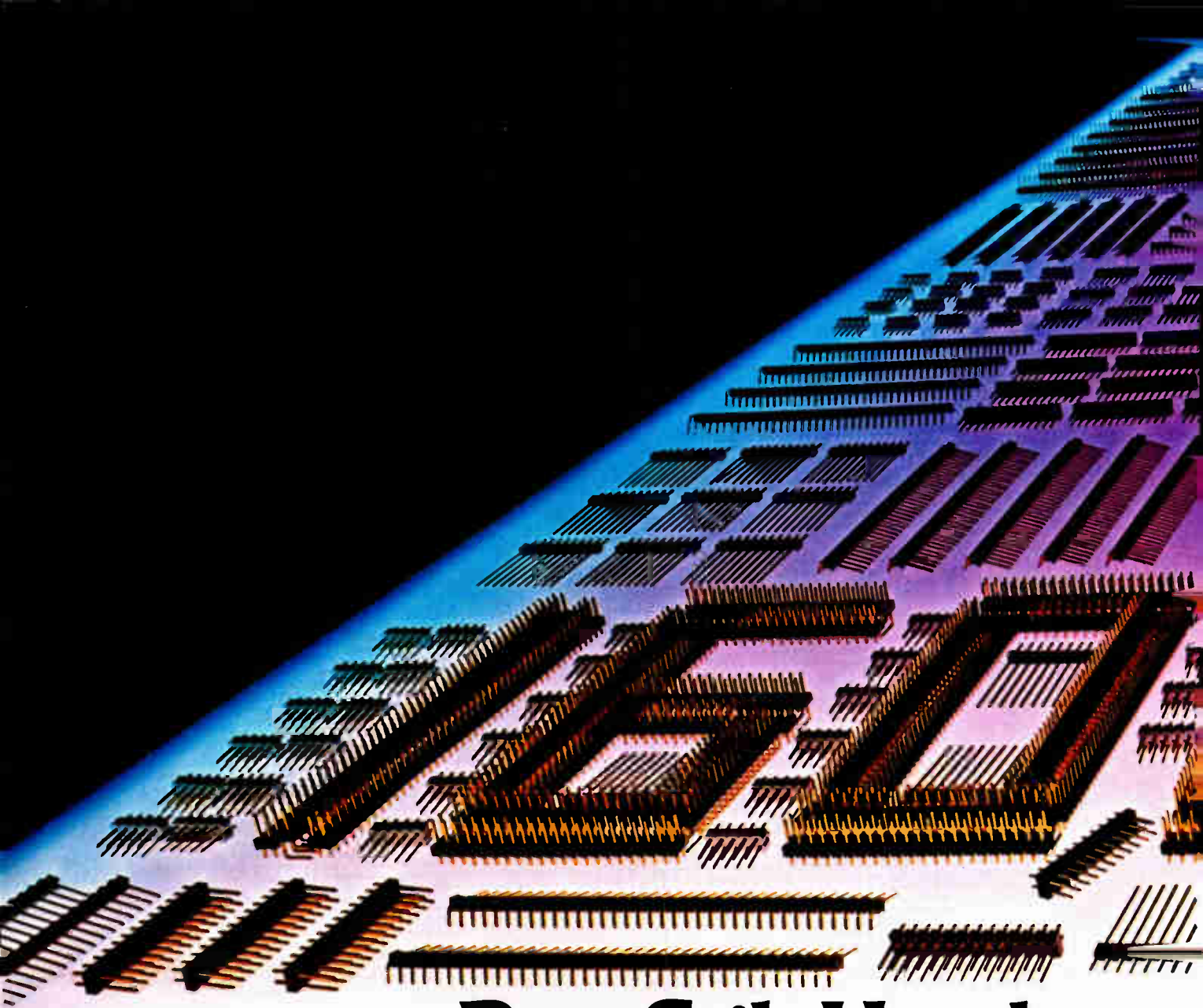

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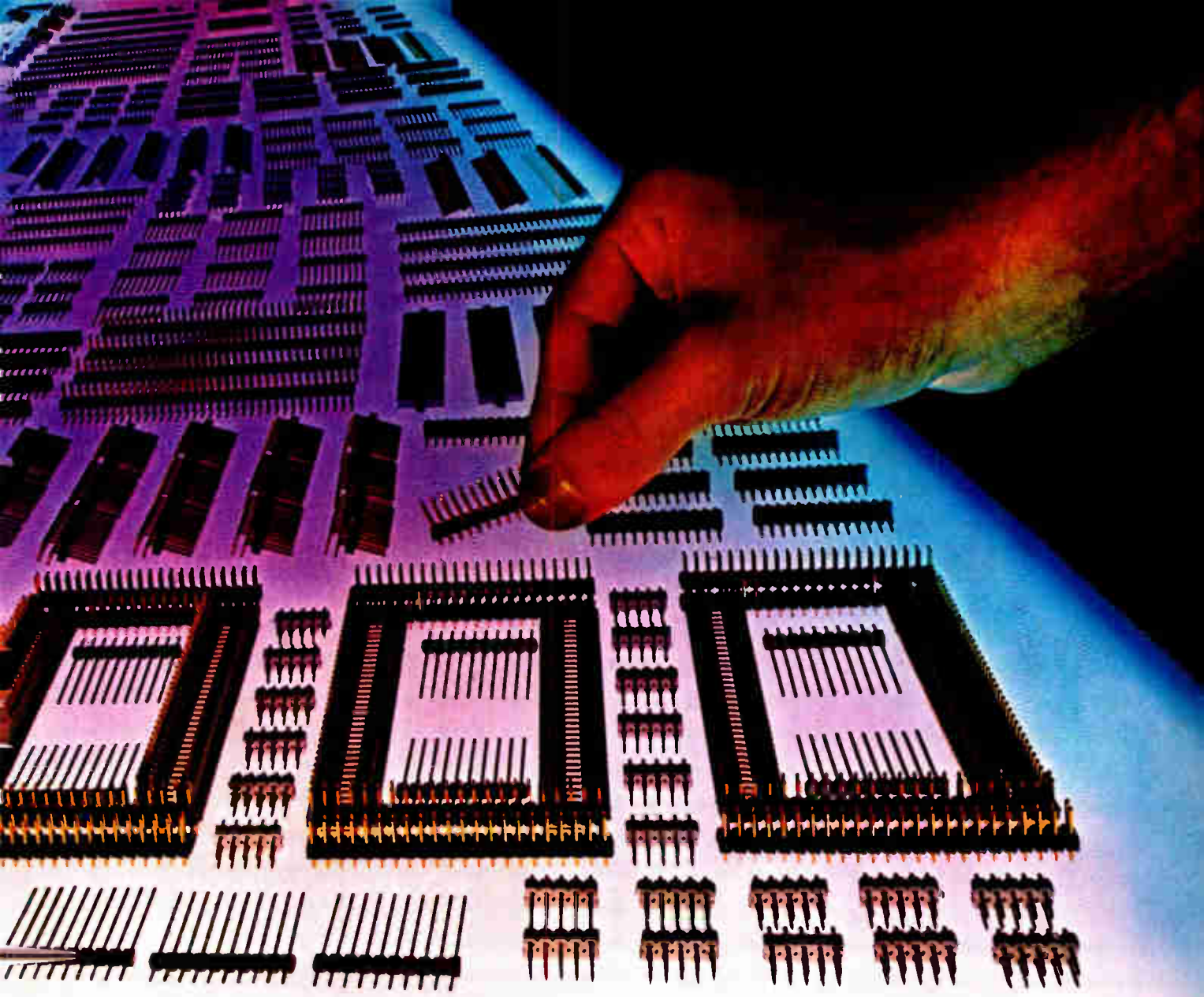

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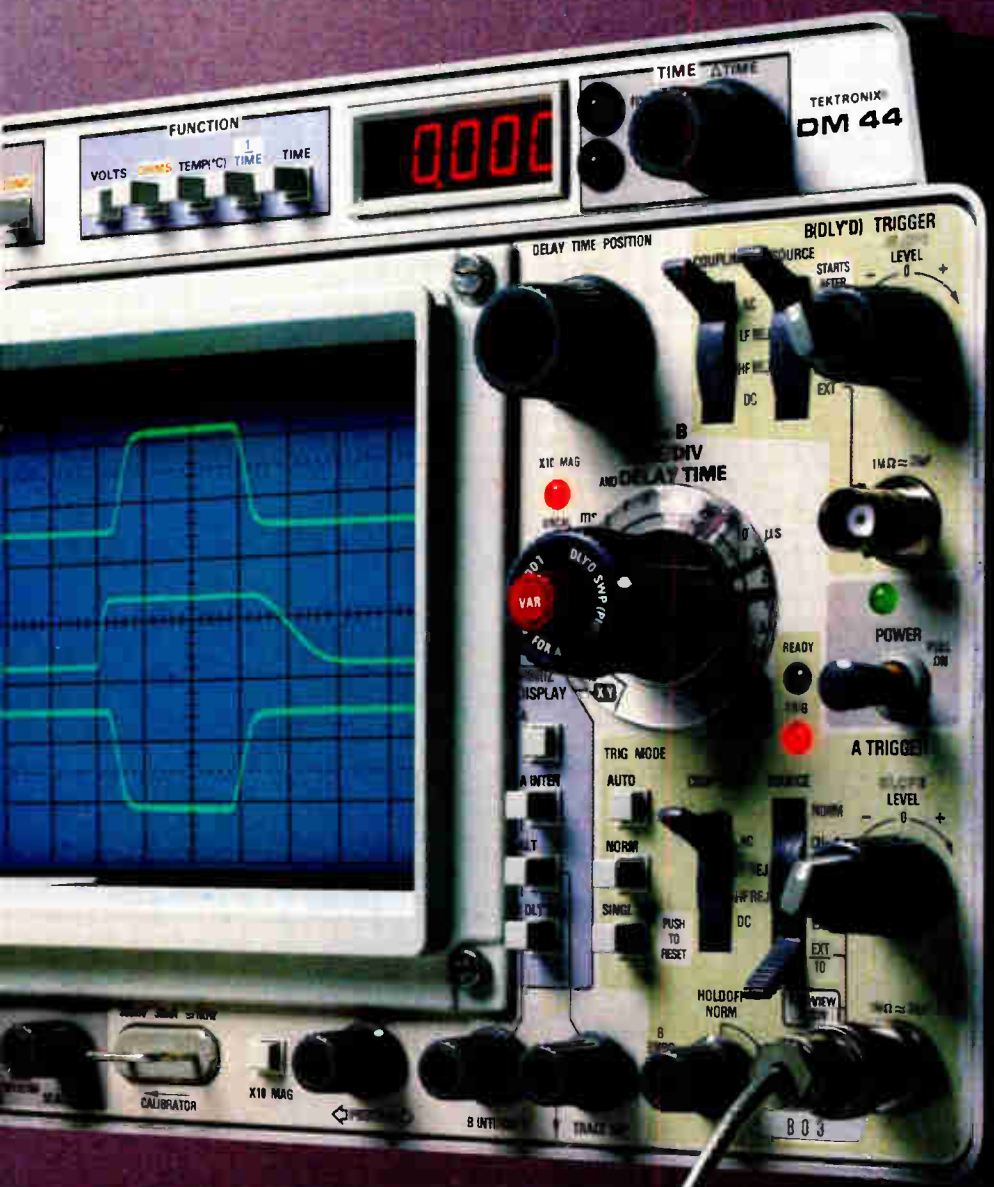

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Technology for the times

Monolithic filter derives design from wave theory

by Kevin Smith, London bureau manager

'Voltage-wave' device that cascades sections of transmission line could be built with C-MOS process

Even as the relative merits of charge-coupled-device and switched-capacitor monolithic filters are debated, researchers have come up with yet a third technique that threatens to upstage them both. Based on wave theory and using analog sampled-data circuitry and techniques, it has the dual virtues of design simplicity and ease of integration.

It made its first public bow this week in New York, in a paper presented to the International Solid State Circuits Conference (see p. 138) by the microcircuit group of Edinburgh University and a group of filter design specialists from University College, Dublin.

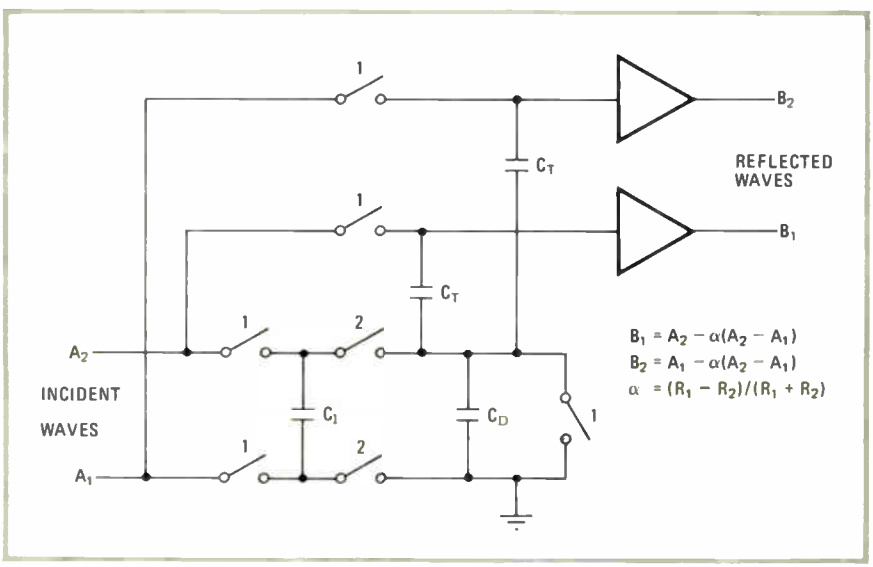
They have demonstrated the elegance and potential power of the technique in a prototype circuit that combines three separate filters—third-, fifth-, and seventh-order low-pass devices—and gives excellent agreement with theory. As a practical design, though, this first chip has shortcomings primarily due to the use of an unsuitable 6-micrometer polysilicon-gate n-channel MOS 15-volt process and purposely overlarge capacitors. But the Edinburgh group believes it could have a competitive complementary-MOS version working in a little over a year's time.

Benefits. Ease of integration and hence low cost is the most significant advantage claimed for the switched-capacitor voltage-wave filter, as it is called. For active elements, it employs simple unity-gain buffers instead of the several, more onerous operational amplifiers needed in a conventional RC switched-capacitor filter. Explains John Mavor, head of the Scottish group, "In C-MOS technology the buffer amplifiers can be built with just a couple of transistors and present a trivial design problem. Dual-input operational amplifiers used in switched-capacitor filters, however, are difficult both to design and to process."

Conventionally, analog filters even of the switched-capacitor type use capacitive or inductive storage elements to create frequency-sensitive circuits. The Edinburgh-Dublin group discards this "physical" approach in favor of a purely mathematical implementation. Their starting point is the fact that filters can be constructed by cascading sections of transmission line that are unequal in impedance. A transmission line, after all, incorporates distributed inductance and capacitance.

In itself that is no advantage, but a body of theory developed at yet a third European university, the Ruhr-Universität Bochum in West Germany, provides a means of representing such a cascaded array with great mathematical simplicity. Its author, A. Fettweis, showed that each section could be modeled by a time delay, representing the wave propagation time, and an adaptor, representing discontinuities between sections of transmission line.

Like the now almost extinct analog computer, the mathematical equations describing these cascaded sections of transmission lines are modeled by connecting together switched capacitors used as computational elements (not as resistors,



Filter on a chip. In a new technique, two transmission line segments with R_1 and R_2 characteristic impedances are linked by adaptor (above) and delay; the ratio of C_1 to C_D sets α.

their role in conventional switched-capacitor filters). These switched-capacitor elements are used to perform such mathematical operations as addition, multiplication, and subtraction in real time on successive data samples. The needed time delay is inherent in the clocking system.

Rationale. "A digital implementation of the storage, multiplication, and addition processes necessary to solve these equations, while possible, is not elegant in integrated circuit form," says Mavor. "We chose an analog, sampled-data realization where the internal calculations are performed using switches, capacitors, and unity-gain buffers, with no basic requirements for operational amplifiers."

The switched-capacitor elements provide a convenient computational element. For example, when voltages to be subtracted are applied to opposite ends of an input capacitor, a charge proportional to the voltage difference is collected during the sampling period. Again, multiplication by a factor of less than unity is accomplished by connecting a second capacitor in parallel with the first. Both functions are employed in modeling the transmission line section, as in the diagram.

Proven. A first silicon implementation adequately demonstrates the design theory. It yields low-pass filter sections with accurately defined pass-band edges at one eighth of the clock frequency and exhibits low sensitivity to variations in capacitor ratios and a good dynamic range of better than 50 decibels.

However, because a C-MOS process was not available at the time and the prototype chip was intended to demonstrate only the theory, chip capacitors were made larger than necessary, operational amplifiers were used for convenience between buffer stages, and more buffer stages than necessary were provided. Now the Edinburgh group plans an optimized version.

Japan

Third prototype of camera-VCR system introduces yet another cassette-tape format

The jockeying over which cassette, tape and recording formats will become the industry standard for the forthcoming video cameras with built-in cassette recorders is heating up. Matsushita Electric Industrial Co. has just announced its entrant.

The new prototype's formats differ from those used in two earlier entries from other leading Japanese consumer electronics manufacturers. Also it incorporates an inexpensive half-inch vidicon as image sensor rather than the solid-state sensors in the other two—a move on Matsushita's part to demonstrate that the cassette-camera combination need not wait for affordable semiconductor sensors and the lack of agreement on standards is what is holding up this new consumer product.

The use of a new high-coercivity tape with a deposited metal coating enables Matsushita to squeeze two hours of recording time into the cassette. That recording time is the same offered in Hitachi Ltd.'s prototype [*Electronics*, Sept. 14, 1980, p. 64] and six times that of the Sony Corp. prototype [*Electronics*, July 17, 1980, p. 48].

Measurements. The Matsushita tape is 7 millimeters wide, and its 10-micrometer thickness is less than half that of standard video tape. The 94-by-63-by-14-mm cassette will hold 103 meters of tape, running at 14.3 mm a second.

The Hitachi metal-coated tape is 6.25 mm wide and 14 μm thick, and 115 m of it fit into the 112-by-67-by-13.6-mm cassette, running at 15.76 mm/s. The Sony tape is 8 mm wide, 14 μm thick, and 25 m of it fit into a 56-by-35-by-13-mm cassette, running at 20.34 mm/s. Sony says thinner tape would extend recording time to 30 minutes from 20 min.

Since recording time is a key feature for the user, the wide divergence between the Matsushita and Hitachi prototypes and the Sony version is notable. However, Sony is not interested in developing a product that could compete with its present line of home video cassette recorders, whose recording times range from 2 hours upwards.

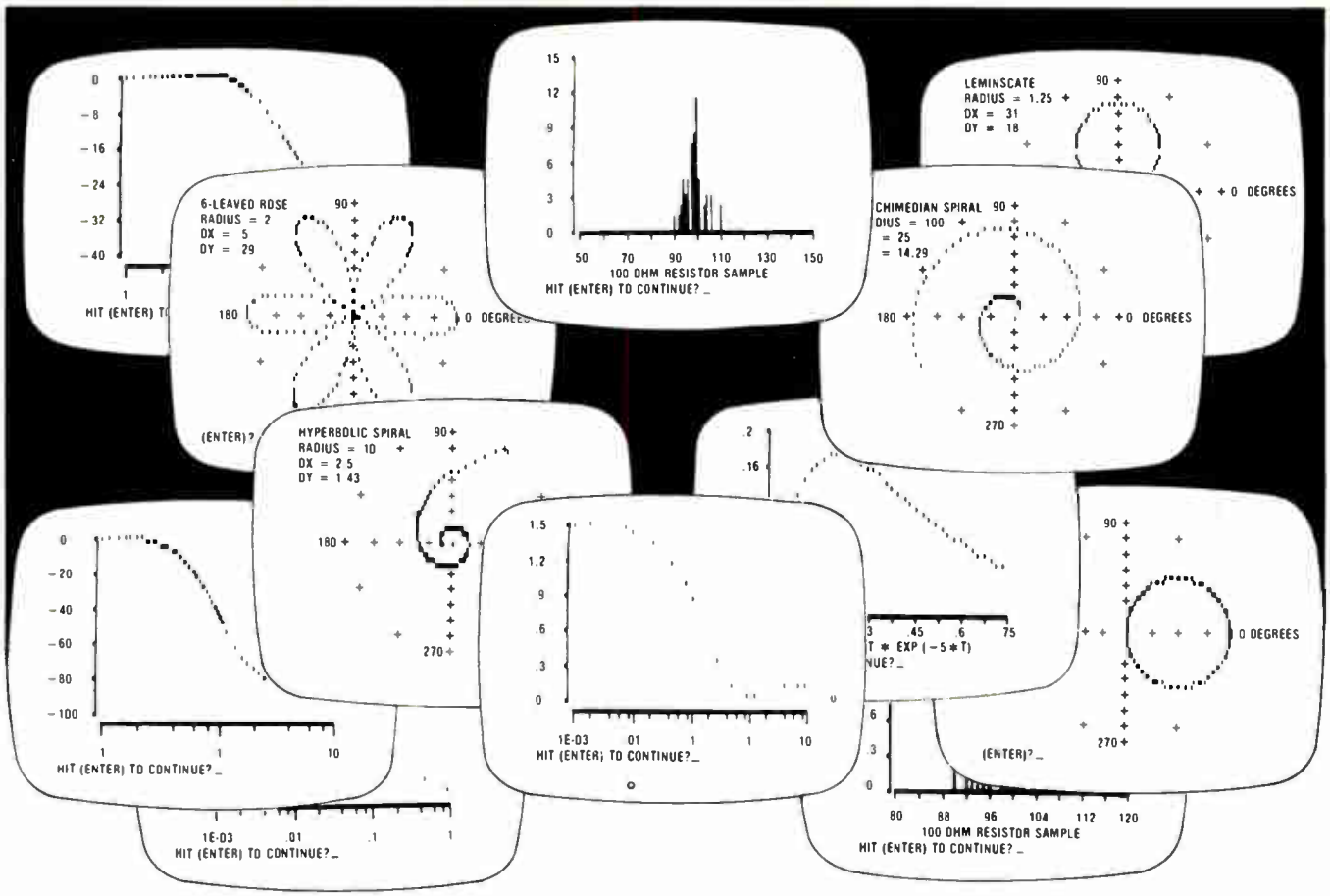
Still, a 20- or 30-min. recording time betters that of the 8-mm home movie camera that these video units are expected to replace. So strong is the threat that the Japanese firms expect photography giant Eastman Kodak Co. to enter the market—and Kodak is known to be doing research in the area.

Although Matsushita's system features the highest recording density of the three, in all the systems the high-coercivity tape supplies picture quality as good as that of 6-hour conventional VCRs.

Sensors. Just as the Japanese companies disagree on a possible cassette and tape standard, they also present different imaging systems in their prototypes. Matsushita's half-inch vidicon, a new tube slightly smaller than the one used in color video cameras today, would speed introduction of a product because it would not be necessary to wait for the price of solid-state image sensors to come down out of the clouds.

However, Sony and Hitachi think the smaller size, higher reliability, and easier producibility inherent in the prototype semiconductor sensors warrant their inclusion in the camera-recorder prototypes. Sony's prototype uses a charge-coupled-device color sensor, and Hitachi's uses an MOS sensor already in production for the firm's consumer video camera that goes on sale in April.

While the consumer may not care about the type of image sensor he has, small size and minimal weight are likely to be important considerations. The small cassette, the 0.5-in. vidicon with only half the volume of the near-universal $^2/_3$-in. versions, and extensive use of very large-scale integrated circuits enable Matsushita to squeeze both recorder and camera into a box measuring only 229



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mm deep by 118 mm high by 67 mm wide. The unit weighs 2.1 kilograms to Sony's 2 kg and Hitachi's 2.6 kg.

Matsushita's prototype uses six Penlite-size nickel-cadmium rechargeable batteries that will run the camera for 40 min. Sony uses a 9-volt rechargeable silver-oxide battery for its 20-min. unit, and Hitachi's 9-v NiCd battery will power the unit for 30 minutes.

With all the differences between the Sony and Matsushita prototypes, they do have a common requirement. They require a tabletop adapter to convert the camera into a playback machine; Hitachi's version incorporates the adapter.

It will take several years for the units to arrive on the market, however. They are expected to cost about $1,000 each. **-Charles Cohen**

Great Britain

Unit identifies words in run-on speech

Though a machine capable of understanding conversations is still a distant goal, a first step in that direction has been taken by Britain's National Physical Laboratory. It has developed prototype hardware that can identify key words and numbers in continuous speech.

In contrast, first-generation hardware works best when words are spoken in isolation and, according to NPL researchers, will never be able to cope with the run-on sounds of conversation. The NPL setup potentially costs much less, too, for the use of preprocessing hardware shrinks the recognition task to one that can be handled by a Digital Equipment Corp. LSI-11 microcomputer.

To help the technique move from the laboratory into production systems, NPL has formed a club of nine users. Within two to three years members like office equipment manufacturers Nexos and the Plessey Co. or CAD equipment manufacturer Quest Automation Ltd. could be putting a speech-recognition capability in commercial systems.

In conversation the beginnings and ends of words can run together, fazing hardware that adopts a word-matching strategy. So instead of isolating words or even phonemes, the British researchers split the incoming waveform into 10-millisecond snapshots and classify each sample into 1 of 16 distinctive phonetic categories. A similar approach is adopted in a speaker-recognition system from Threshold Technology [*Electronics*, Jan. 27, p. 53].

The 16 categories each correspond to one of the characteristic resonant modes of the human vocal tract, and the duration of each phonetic feature is also taken into account. The approach works equally well with every language and every speaker, and the phonetic features lie within the bandwidth of all communications systems.

A form of frequency analysis based on auto correlation techniques is used, according to Brian Pay, a researcher at NPL's laboratories in Teddington, Middlesex. Data bandwidth is so reduced that recognition decisions can be performed in real time using relatively little power.

Matched. Each category is defined by a 32-bit word, and this is transmitted every 10 ms to a short-term memory where a sequence of sounds is built up. At this stage, comparison logic, under the control of a software director, attempts to match each of the items in the store with the templates of admissible sequences in a 64-word vocabulary. To shorten the process, the matching logic can take account of the context—for example, by inspecting only those templates that correspond to spoken numerals.

At this intermediate level, a list of matches with attached probabilities is stored. The overall match is subsequently deduced in terms of the permitted syntax. For example, in an avionics application, in the command "set height 20,000 feet," the key word "set" triggers the system and "height" defines a context requiring a numerical value. At this level, says Pay, "We are moving towards speech understanding rather than speech recognition." **-Kevin Smith**

Japan

GaAs uhf amp IC has low noise, wide band

With the aid of a simple gallium arsenide integrated circuit, extremely low-noise wide-band amplifiers spanning the very high and ultrahigh frequency bands can now be built without tuned circuits. Although a variety of applications is envisioned by the engineers at Matsushita Electronics Corp. who developed the ICs, most of them could wind up in TV tuners made by parent Matsushita Electric Industrial Co. and others.

Over a frequency range of 50 to 2,000 megahertz, the new devices have a noise figure of only 1.7 to 2.2 decibels and a gain of 8 to 10 dB. Noise is least at about 100 MHz, increasing slowly at higher frequencies as well as at low frequencies because of 1/f noise. The input and output impedances are 50 ohms, with standing-wave ratios less than 2.5—low enough to build multistage amplifiers with no matching circuits between stages. Noncritical radio frequency chokes to supply bias voltages and coupling capacitors are the only other amplifier elements.

For use in TV tuners, the devices could be designed for the narrower frequency range of 50 to 900 MHz and hence a higher gain than the 15 to 20 dB normally required in this application. Also, the impedance level would probably be higher.

The device that gives this superb performance consists of a single transistor with a Schottky-diode capacitor and epitaxial island resistor connected in series between its drain and its gate to give a negative voltage feedback.

Recessed gates. The transistor resembles the one developed earlier by Matsushita [*Electronics*, July 31, 1980, p. 56]. It has recessed gates and a narrow, 1-micrometer source-to-gate spacing for low series resistance of less than 5 Ω. Gate length is also 1 μm, the same as the source-to-gate spacing, for good high-frequency characteristics. Feed-

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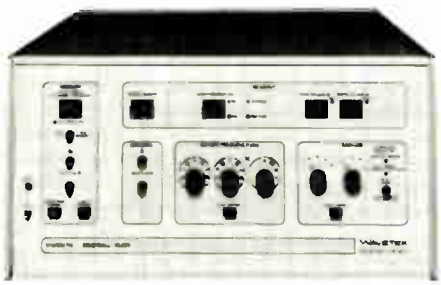

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back resistance is about 250 Ω, while the series capacitor is about 50 picofarads, but either value can double or halve without greatly affecting device characteristics.

As fabricated for low-noise operation, the device runs on 20 to 30 milliamperes from a 3-to-5-volt power supply. The same device fabricated for a current of 100 mA will operate as a power amplifier with several hundred milliwatts' output.

Other firms have also made GaAs microwave ICs, some with even wider bandwidths, but they have higher noise figures and appear to use different circuits. Hewlett-Packard has a device that will operate over the range of direct current to 4 gigahertz, but its noise figure is said to be about 12 dB. Siemens has just announced a GaAs IC in the same frequency range, but it has a noise figure of 4 dB. **-Charles Cohen**

West Germany

Circuitry for black-on-white CRT cuts flicker and raises resolution

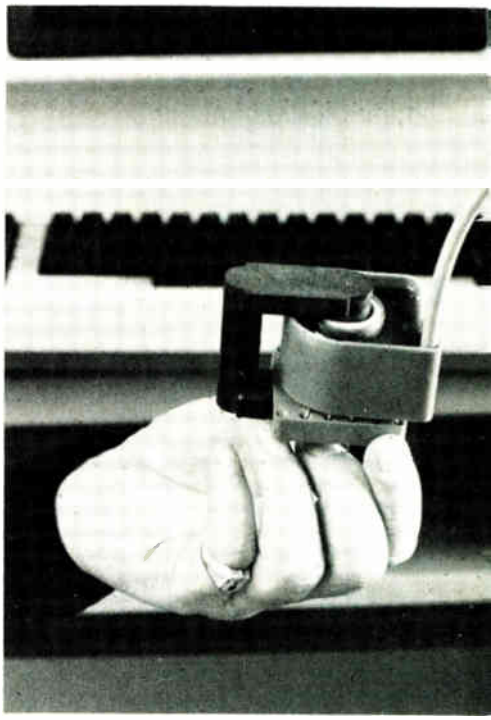
A circuit proposal from Siemens AG promises to be an economical way of ridding cathode-ray-tube terminals of eyestraining flicker and of producing many more high-resolution characters on the screen than can conventional CRT displays. Worked out at the applications laboratories of the company's components group in Munich, the proposal provides for the display of 2,560 black characters against a light background.

As the number of these terminals mounts, so do the demands of labor unions and health authorities that their manufacturers come up with displays that reduce eye strain at close viewing ranges. Thus CRT makers are considering switching from bright characters on a dark-green background to dark characters against a white background.

Flicker. Such a display lessens strain on the eyes because they need no longer alternately adapt to black-on-white printed copy and a dark display of bright characters. However, the white background introduces another problem: luminance flicker, which is noticeable even out the corner of the eyes.

Since flicker becomes imperceptible above 75 hertz, the Siemens proposed circuitry provides for a picture frequency of 80 Hz, 20 Hz more than for conventional data displays, explains Wolfgang Winkler, head of the applications lab that worked out the proposal. With the 80 pictures per second, some 40 million picture elements, or pixels, are transmitted—two to three times more than in conventional data displays.

To obtain a high resolution, the circuitry increases the line frequency to 45 kilohertz, up from 25 kHz or so for high-quality conventional CRT displays. This measure gives 32 80-



Easy on the eye. Siemens's 2-D-Transformer (right) is part of a low-cost deflection unit in circuitry designed to raise CRT display frequency above the threshold for flicker.

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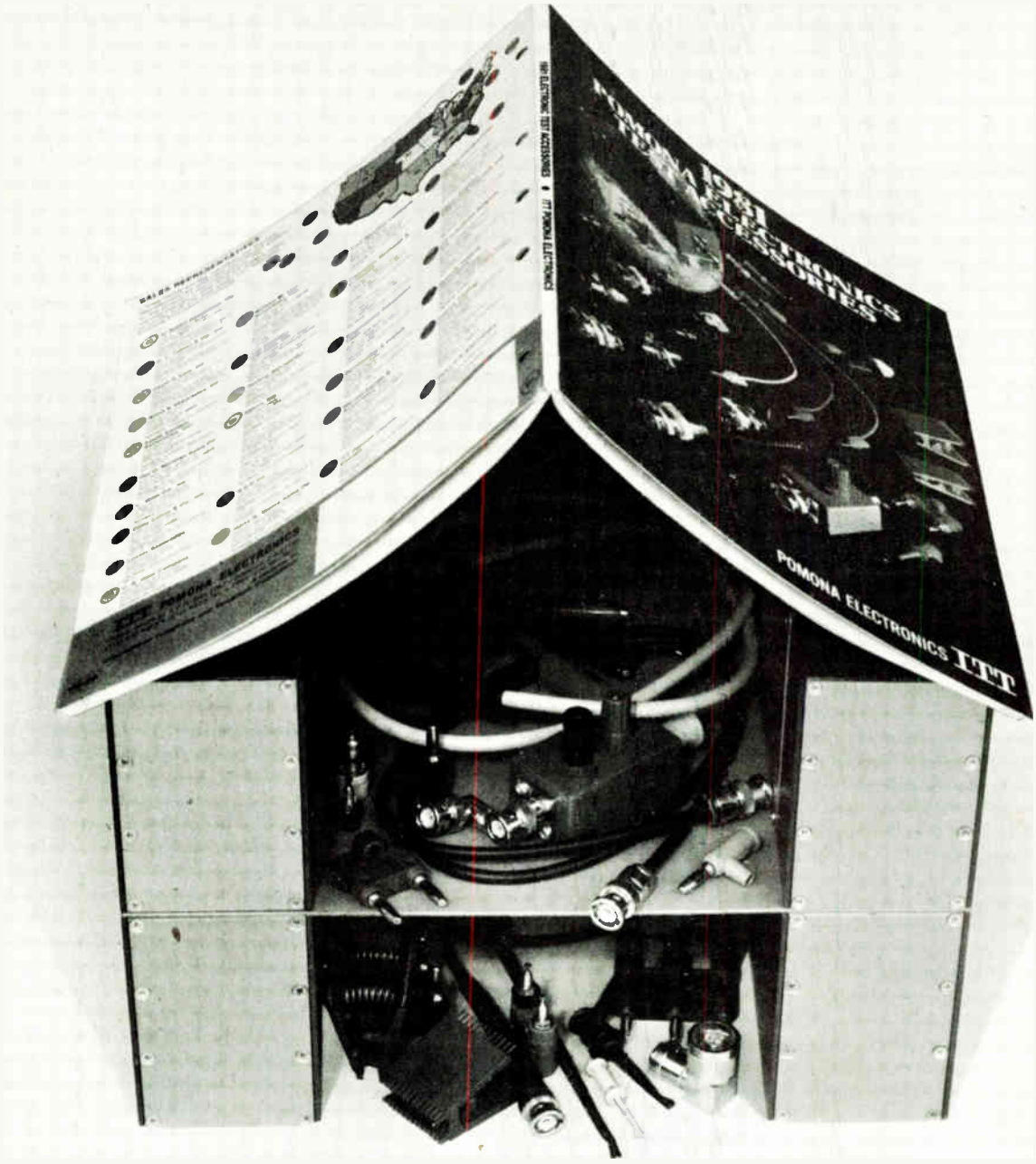

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character lines of high-resolution 8-by-16-dot characters, eight more lines than do present-day displays.

This performance, Winkler says, can be economically realized with relatively new components that his company has developed. Contributing to the high information flow of 40 million pixels/s are power MOS transistors of the Sipmos variety [*Electronics*, Aug. 28, 1980, p. 145], featuring switching speeds of 300 nanoseconds at 1 kilovolt. Sipmos parts are also used for signal amplification and beam deflection.

The company is using its new 2-D-Transformer that works according to diode-split transformer principles and is combined with a ferrite core. Winkler says this combination constitutes a low-cost deflection unit for 45-kHz line-frequency operation. A bipolar integrated circuit, the TDA 4610 widely used in TV sets, controls a diode modulator circuit that corrects the picture geometry without loss of sharpness.

Economy claim. To support his claim of circuit economy, Winkler points to the low components count: 15% fewer than would be in a conventional CRT terminal if it were designed to achieve the same flicker-free, high-resolution performance. The 1-KV power transistor replaces an IC plus its peripherals, as well as a complete driver stage. The 2-D-Transformer replaces a conventional transformer and a cascade circuit or a high-voltage transformer and an integrated half-wave rectifier. The Sipmos transistors, he says, make it possible to design flicker-suppressing, resolution-enhancing display circuitry "with fewer components than has a color TV set without high-frequency and intermediate-frequency stages."

The Siemens circuitry also offers a distinct advantage over another possible solution to the flicker problem. Tubes with a long after-glow, or persistence, would eliminate the flicker—but their long persistence spells a loss of contrast and streaking during abrupt transitions from black to white and vice versa as occurs with the display of rapidly changing information. **-John Gosch**

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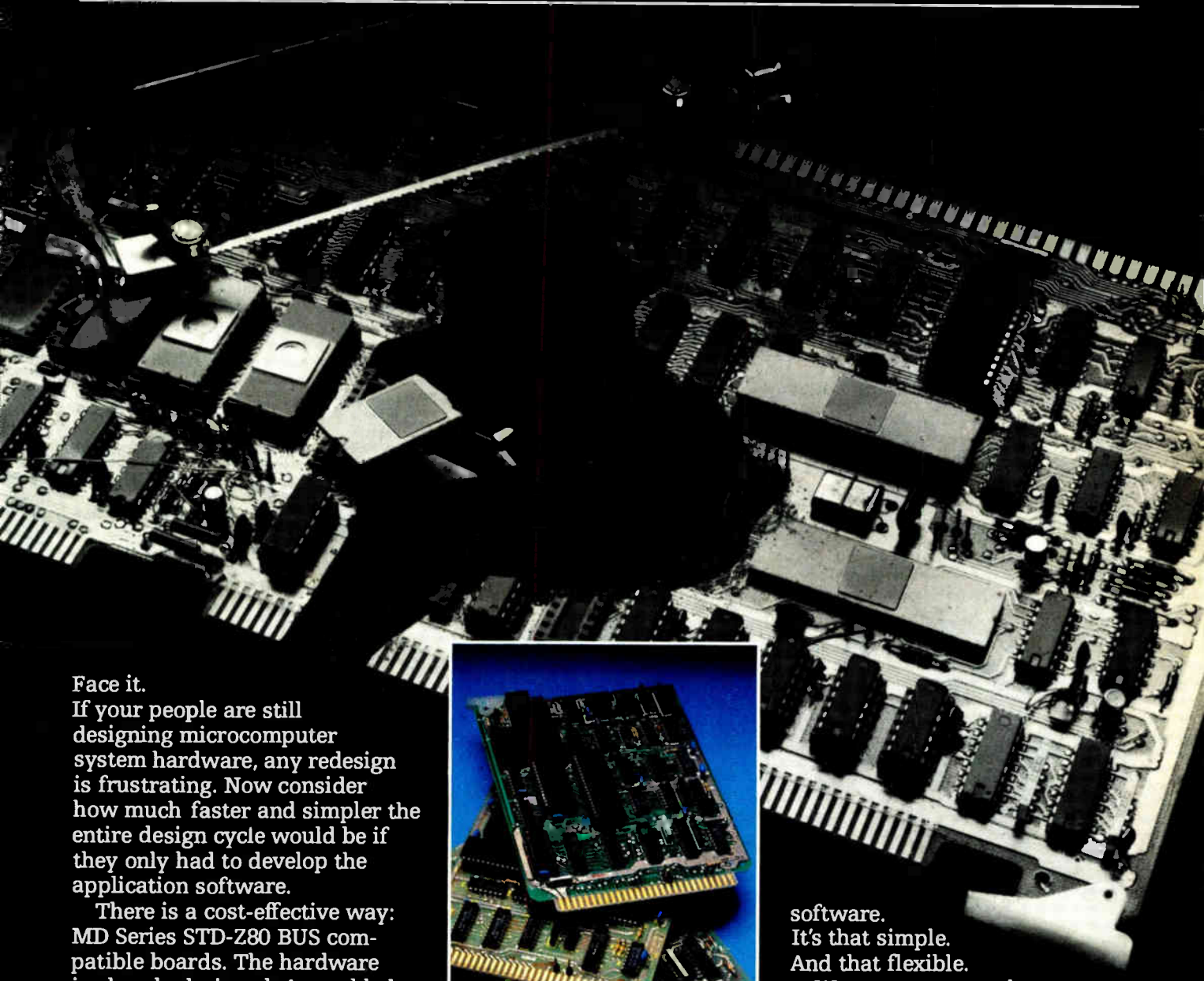

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At the same time the counter is set, branch to the second test. (bracketing allows simultaneous actions).

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Or if counter #1 has reached 100 mS, then activate the trigger.

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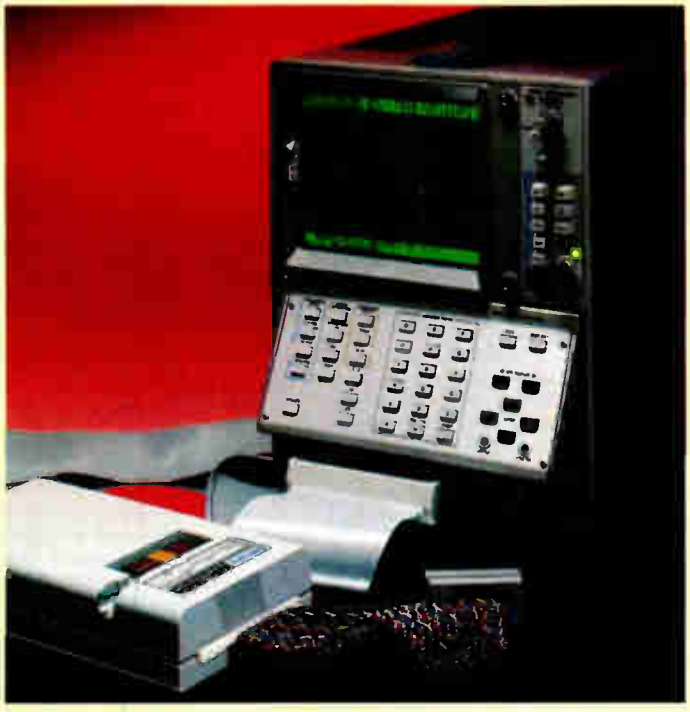
Locating an intermittent fault. The following program gives a limited demonstration of the simplicity and power behind the 7D02's user language. Here the object is to trigger when a second event on the bus does not occur within 100 mS of a first event.



The 7D02 is a 3-wide plug-in for the popular Tektronix 7000 Series oscilloscope. Shown above is a Tek 7603 mainframe housing the 7D02 logic analyzer with a personality module supporting the 6802 microprocessor.

By using the proper personality module, software flow can be displayed using the mnemonics of the chip under test, here the Motorola MC6802.

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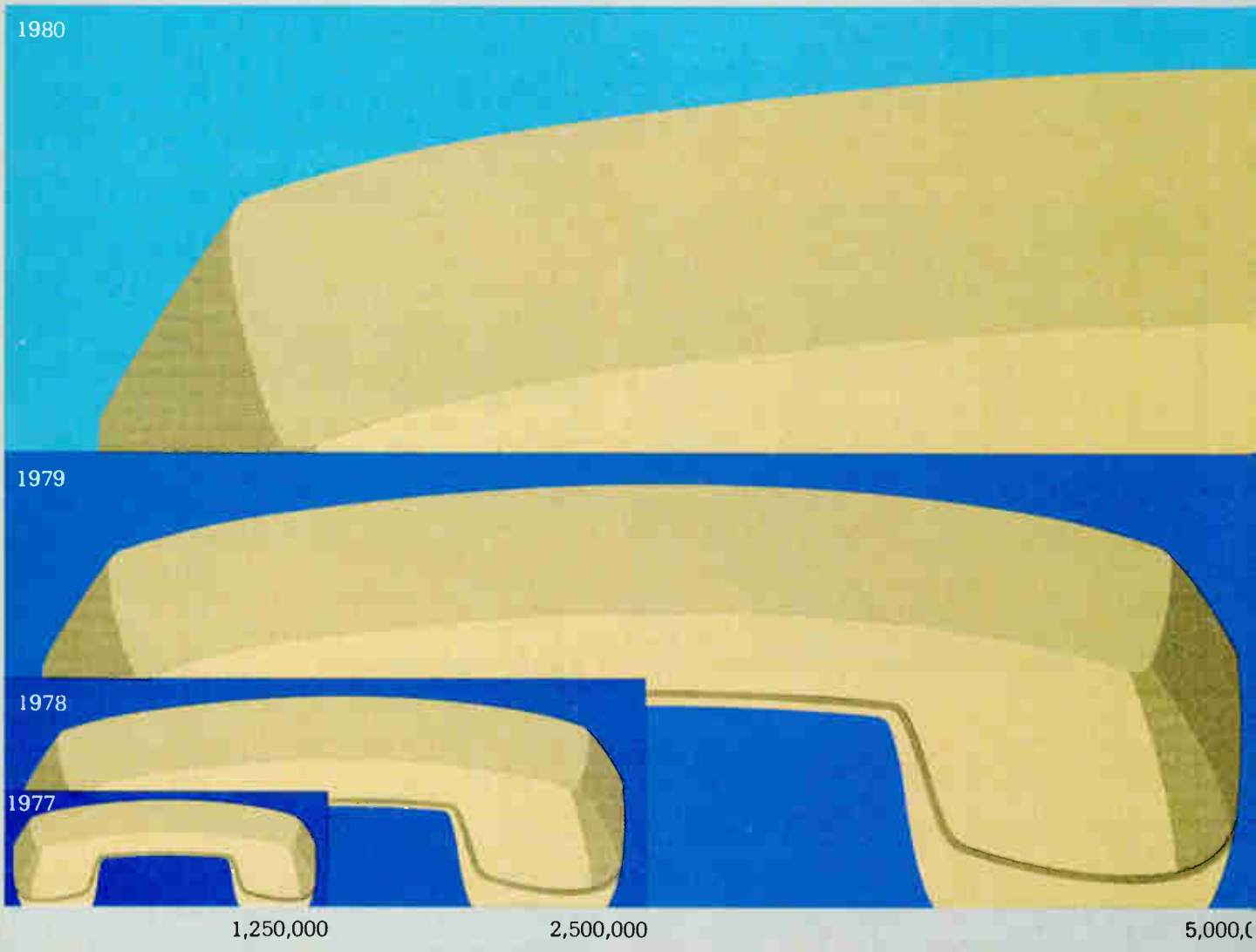

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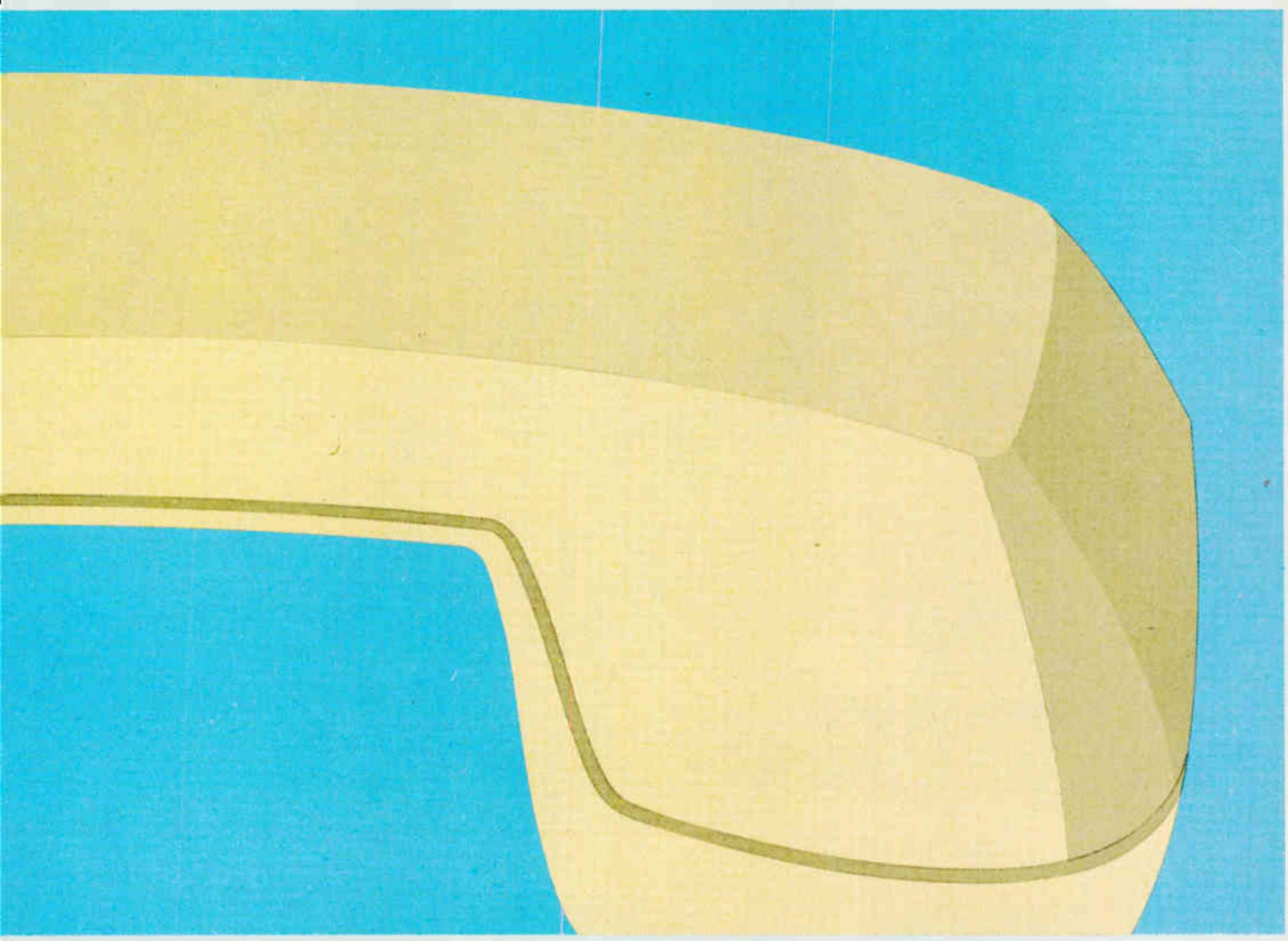

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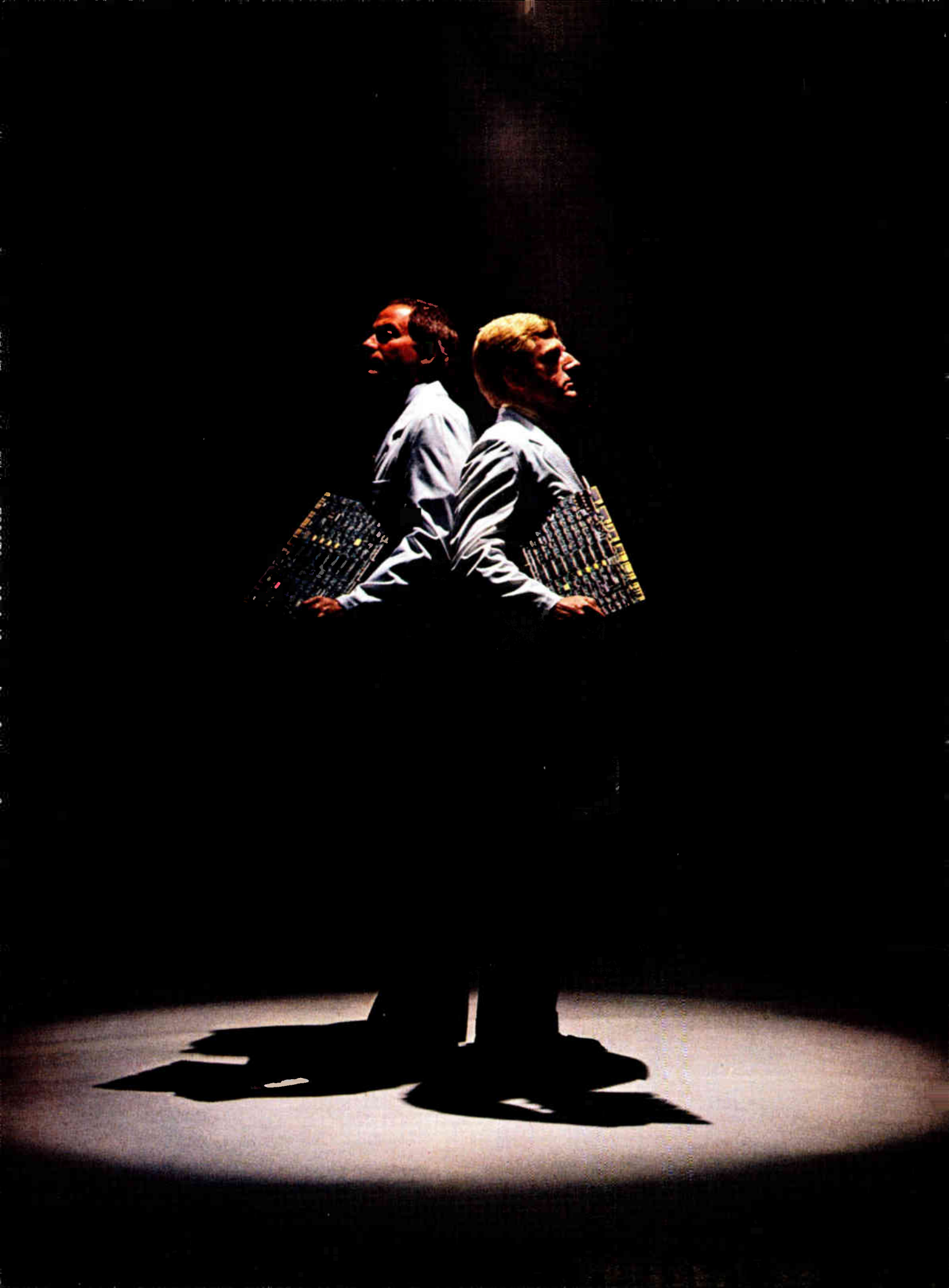

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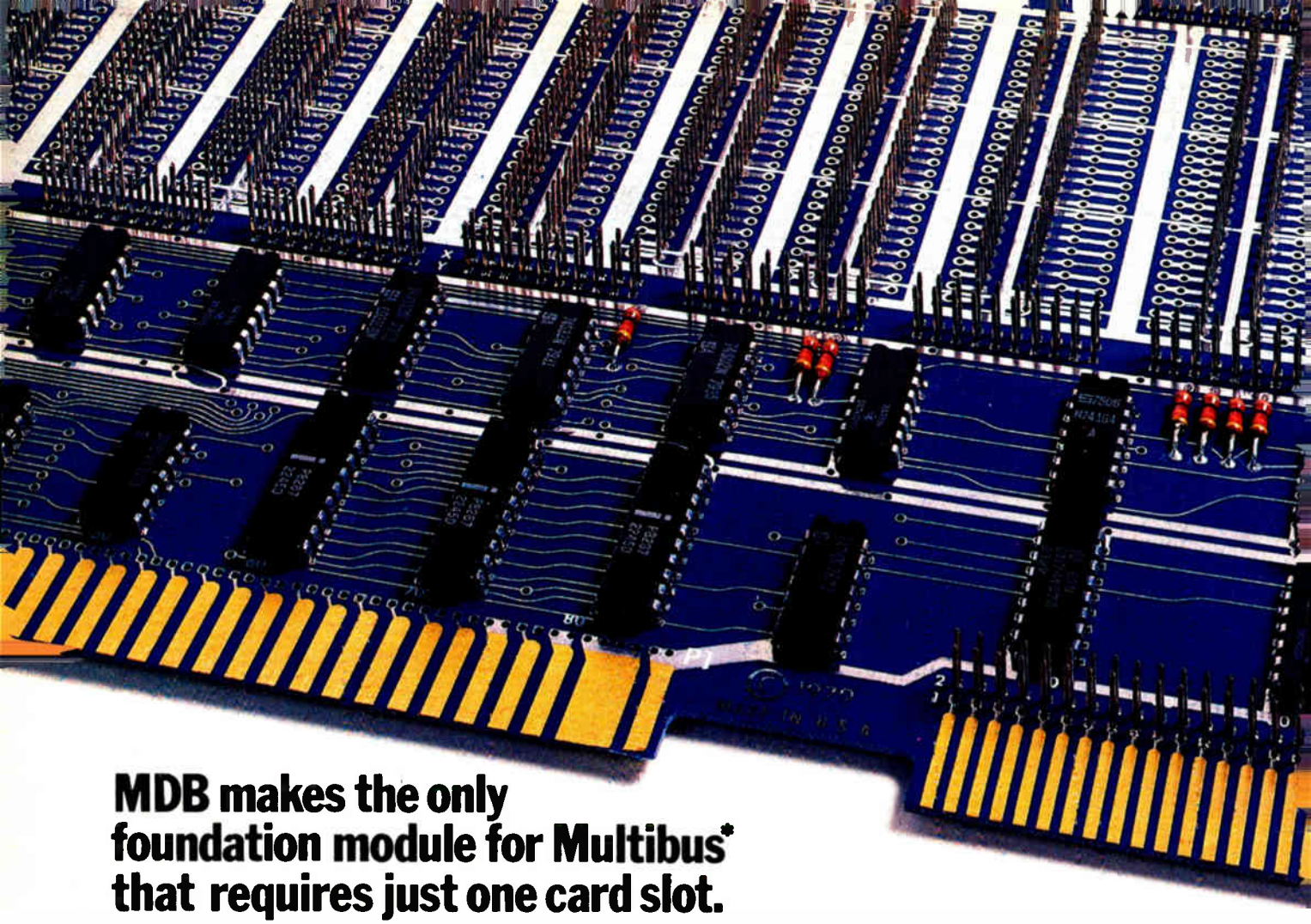

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GE launches major LSI technology push

The company is committed to gaining a leadership role in advanced technologies targeted for internal use

by Pamela Hamilton, New York bureau manager

About a decade has passed since General Electric Co. dropped out of the digital integrated-circuit market, folded its computer manufacturing operations, and slipped into the background of digital logic and memory technology. Now the international conglomerate is making a comeback in this direction.

The familar GE logo will not be seen in the rough-and-tumble merchant market, however. This time the company will be manufacturing custom semiconductors in large quantities, to supply internal needs brought about by the increasingly complex systems it plans to produce in the next two decades.

Like those computer companies that have already established internal semiconductor capability [*Electronics*, May 22, 1980, p. 106], GE found that the merchant market is not always ready to gear up production to meet the relatively low demands of systems manufacturers for custom ICs. The problem of maintaining proprietary designs is another reason for establishing an in-house capability.

As an international supplier of power generators, communications equipment, home appliances, and industrial products, General Electric, Fairfield, Conn., believes that it now needs in-house capabilities to design and fabricate large-scale ICs for these systems. In fact, GE estimates that as many as 60% of its products will use LSI and very large-scale integrated-circuit technology by 1985. And for a company with sales of nearly $25 billion last year, that adds up to a lot of devices.

A major supplier of power semiconductors, GE, with its new solid-state push, wants to move into a leading position in the LSI arena. To that end, the firm has participated in the Defense Department's very high-speed integrated-circuit program, which, most agree, will serve as a stepping stone to advanced computer-aided-design techniques and high-density processing know-how.

The first internal customers for GE's homemade ICs will be in the Aerospace Business, the Industrial Electronics Business, the Information and Communication Systems groups, and the Medical Systems Business division. There are numerous other product departments in line as well, from consumer and power systems sectors (see chart).

"Trends in electronics today for total solutions [on a chip] are giving systems houses a better opportunity to serve individual market needs than wafer bashers," observes Roland W. Schmitt, vice president, Corporate Research and Development, Schenectady, N.Y. "That's why you see such increasing activity in GE today. At the time that we got out of the merchant market the need for those [semiconductor] technologies internally wasn't as obvious as it is now. It has become vividly clear that we need the technologies not just for the products we sell, but also for automating internal design and manufacturing."

Robert T. Cornell, first vice president for the New York–based investment firm of Paine Webber Mitchell Hutchins, sees GE's semiconductor push as a first step. "GE's move into semiconductor components is a piece of an extremely grand strategy. Not only should it eventually improve the com-

Ringmaster. As head of Advanced Microelectronics operations, Donald S. Beilman will oversee GE's VLSI effort.

pany's growth, but it should also help to increase productivity in GE's own plants," he says.

The plan. To achieve these goals, the company has taken a two-pronged approach—an internal companywide push into all phases of VLSI design and development and the establishment of a technical-resource and personal-training center to implement any IC technology to come out of the VLSI program. Company officials also expect the recent Intersil Inc. acquisition and the pending Calma Co. addition to aid in this endeavor—although peripherally, as both operations will remain vendors to outside customers.

Heading up the technology thrust will be Donald S. Beilman, formerly the vice president and chief technologist for GE's Aerospace Business group in Valley Forge, Penn. As the new vice president and general manager for the recently formed Advanced Microelectronics operations in Valley Forge, Beilman will report directly to the executive vice president and sector executive in charge of the Technical Systems and Materials sector (see chart). But his responsibilities extend through all parts of the company as well.

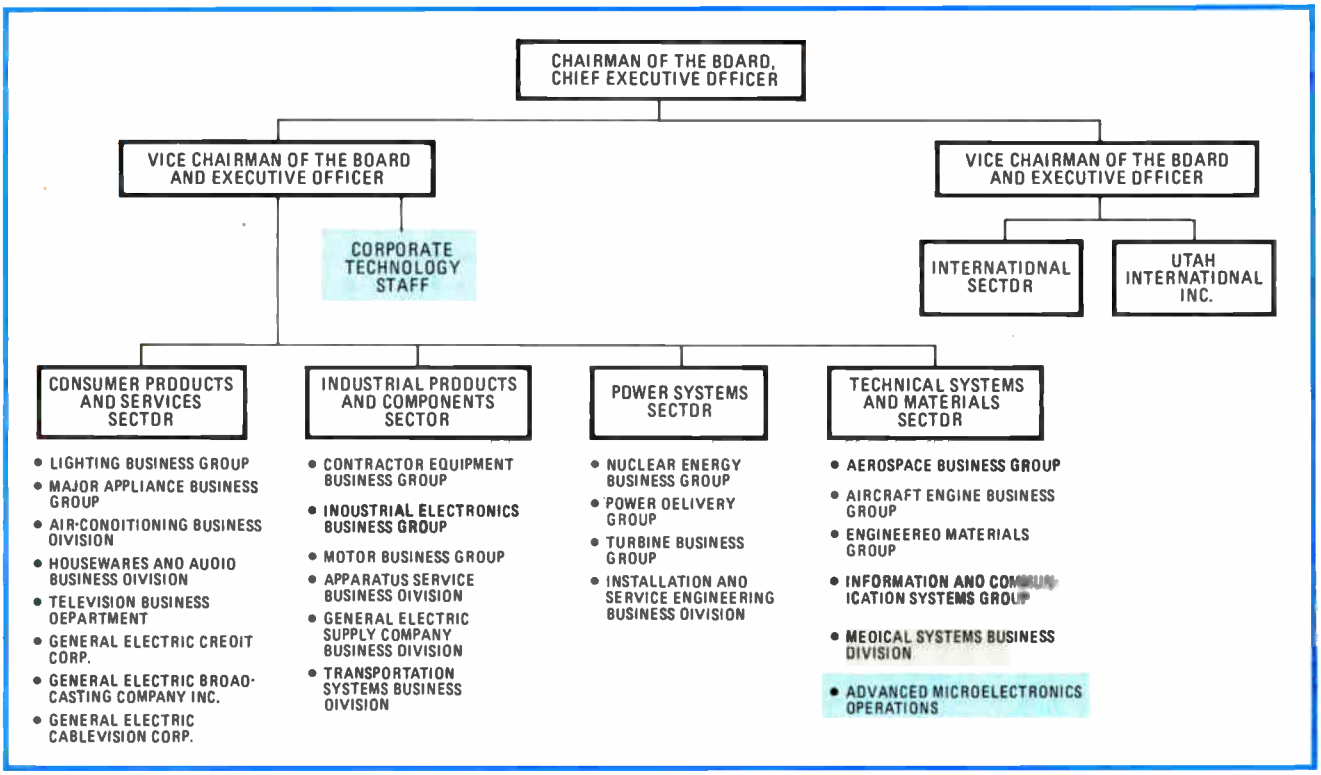
The Advanced Microelectronics operations consist of the Electronics Laboratory, Syracuse, N. Y.; the military microelectronics program (VHSIC), Utica, N. Y.; and the soon-to-be-completed Microelectronics Center (MEC) in Raleigh, N. C. Corporate Research and Development will support this fledgling enterprise with process and design know-how.

Double dual-function. "The MEC is a dual-function laboratory. Not only will it serve as a research facility, but production will also be done there," notes Beilman. In addition, the center will serve both as IC supplier and internal training center for the design teams from throughout GE. "These people may want to take the production capability from the MEC back to their own product areas once they know how to do it," he adds.

The $55 million center will begin shipping custom ICs to GE's business divisions in 1982. More than 160 people are scheduled to be hired over the next two years, with a total of about 500 on board in the next 10 years. James E. Dykes, former vice president and general manager at Harris Corp.'s Semiconductor Products division, Melbourne, Fla., has been hired as general manager of the center. Dykes brings with him considerable experience in MOS technology.

Beilman estimates that the Research Triangle Park facility will initially produce 75,000 wafers a year. Up to five modules providing both research and production capabilities will be built on the North Carolina site, with each one turned completely into a production line as internal demand grows. "We have a capability of producing 275,000 wafers a year if both process and engineering development are being carried out in the same module," Beilman explains. Output jumps to 400,000 wafers per year if the module is dedicated completely to production.

Although Beilman expects to leave silicon on sapphire and gallium arsenide technologies to Utica and Syracuse, respectively, he does see certain advanced processes being implemented on the MEC's product lines. Among them are an advanced bipolar process—probably an oxide-isolated I^2L process; an advanced n-channel MOS process—either H-MOS



LSI permeation. Both the Advanced Microelectronics operations and the Corporate Technology staff will be helping other GE businesses increase in-house LSI design and fabrication capabilities. Initial programs are slated for the industrial and technical systems sectors.

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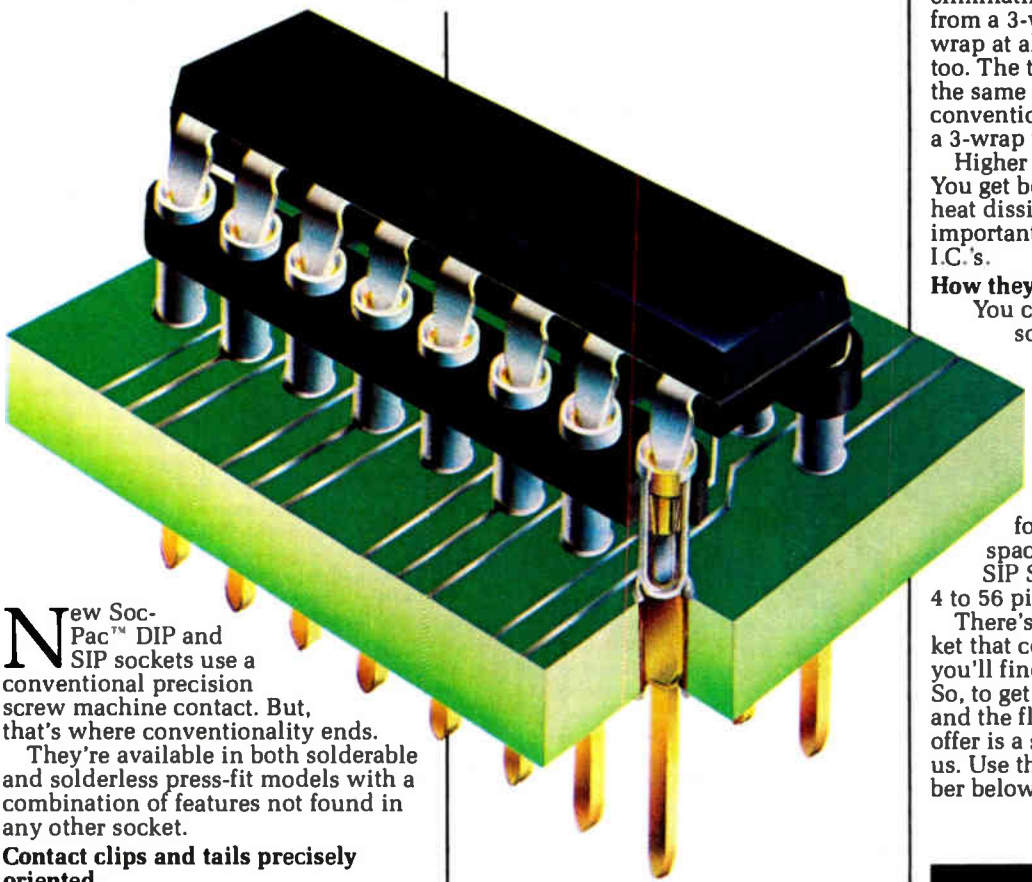

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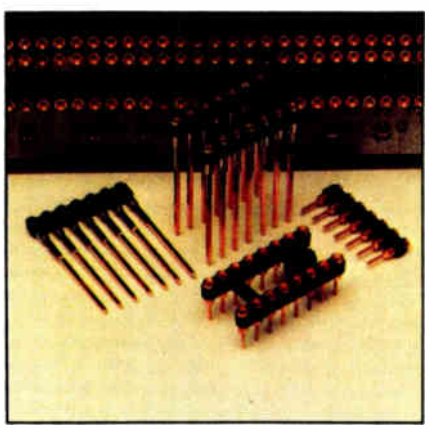

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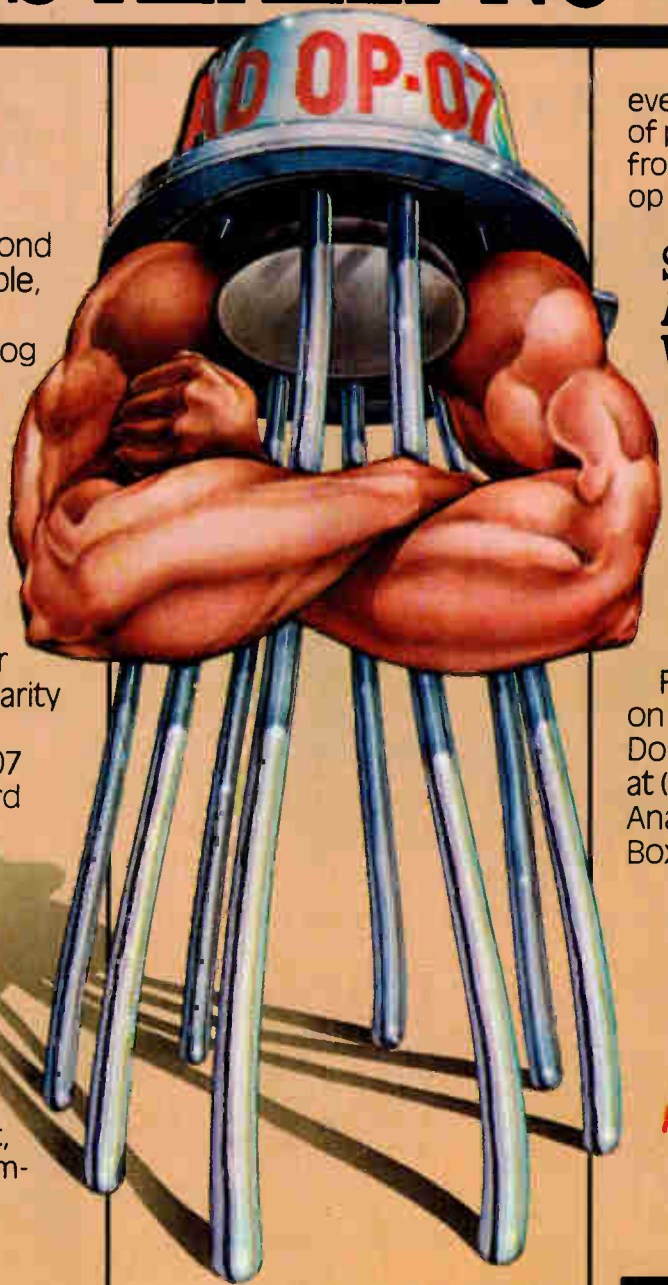

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Circle 98 on reader service card

or H-MOS II; and bulk complementary-MOS processing. Initial IC production will be directed at mobile communications applications, according to Beilman, with gradual growth into other electronics-dependent areas. Among those he cites are data-processing and medical systems businesses. Flight simulation and other aerospace needs will also have to be met eventually.

Software a key. Advanced computer-aided circuit design concepts, as well as new architectural approaches for circuits, are being developed and tested at the Electronics Laboratory under the aegis of GE's internal VLSI program and the federally funded VHSIC program. Central to GE's work in this area is automated physical-layout software based on binary decision diagrams (BDD), according to Richard A. Kashnow, manager of the Laboratory. "BDD is a method of approaching design that doesn't grow exponentially with complexity," he notes. "The system gives a functional description, not a gate-level description, and so it doesn't use as much computer memory as earlier LSI computer-aided-design programs." Thus the set of test vectors this BDD software generates is almost an order of magnitude smaller, he says. The layout software will find use both in GE's part of the VHSIC program and work that will be done at the MEC.

Two advanced circuit programs at the Syracuse lab may also be employed at MEC. The first is a self-testing multiplier fabricated with a C-MOS-on-sapphire process. The second is a monolithic microwave low-noise amplifier using MES FETs on gallium arsenide and being developed under a Phase III VHSIC contract. The latter is the technology Beilman would like to see applied to mobile communications—but on silicon.

Much of the process development work for the company as a whole, and for the Electronic Laboratory and Microelectronics Center in particular, will take place at the Corporate Research and Development center (CRD) in Schenectady, N. Y. "We have the lead role for process development," notes David C. Golibersuch, manager of the signal electronics laboratory at CRD. Among the processes his group is looking at are: 3-micrometer C-MOS on sapphire, 1.25-μm bulk C-MOS, and gallium arsenide MES FET on sapphire for the monolithic microwave circuit work being undertaken in Syracuse. "We're laying the groundwork for a 0.5-μm process now—a likely candidate is bulk C-MOS—by developing vital unit process steps such as dry etching," he notes.

Corporate R&D will also help the MEC get up and going on some of the custom circuit design work. "We're doing much of the head-end design work for the custom circuits manufactured outside of the company now," notes Virgil L. Stout, research and development manager, electronics science and engineering at CRD.

Industrial links. The Industrial Electronics Business group is well positioned to benefit from technology coming out of both CRD and the Microelectronics Center. "VLSI technology will continue to have the type of impact on industrial electronics that LSI technology has had," observes Donald K. Grierson, senior vice president and group executive.

Both Intersil and Calma will be part of his operations, and he fully expects CRD's and the MEC efforts to benefit them as well. In fact, although the Intersil acquisition was completed only this month, CRD already has research projects started for the new addition.

"If there are some areas of overlap between the MEC, CRD, and industrial electronics, we'd rather have it that way, than to have areas of void," he says.

One area of overlap may be the Industrial Electronics laboratory being constructed as part of a $31.3 million expansion begun last August in Charlottesville, Va. "My laboratory will be more of a systems prototype lab than a group developing state-of-the-art devices," notes Grierson. Projects under way include development of systems software architecture for use with various factory and process automation systems; equipment and software for automated inspection; and robots, for internal use and to be offered externally as products. □

Solid state

Multivalued logic takes new paths

Successful implementations of once-elusive technology are showing up in MOS, CCD, and ECL versions

by John G. Posa, Solid State Editor

If only integrated-circuit interconnections could carry more information . . . If only memory cells could store more bits . . . Such wishes have led to the development of multivalued logic circuits—circuits that go beyond binary, using base 3 or base 4 arithmetic instead of base 2. For a decade, logic designers chased after multivalued circuits, but early implementations did not perform as well as expected because of lagging process technology and poor operating margins. Also, an essential element—a latch or memory cell that could efficiently hold multiple levels—proved elusive.

Recently, however, interest in multivalued logic has been rekindled. One of the reasons, ironically, is the advent of very large-scale integration. True, VLSI continues to incorporate more and more devices, but an even greater percentage of the die is being consumed by on-chip wiring. Interchip interconnections, too, have grown unwieldy, necessitating packages with upwards of 100 pins in some cases.

Even if all dimensions of the active elements were reduced to zero, the packing density of a binary logic chip would hardly change, says Tich T. Dao, a researcher at Fairchild Camera & Instrument Corp. in Palo Alto, Calif., who has been investigating multivalued logic since the early 1970s. At this week's Compcon 81—the 22nd Computer Society International Conference—in San Francisco, he will join five other speakers in a session devoted to multivalued logic.

To reduce wiring, says Dao, the information content carried through each connection must be increased, either by time or by level multiplexing. Whereas the first approach is mainly limited to interchip pin connections, the second technique can be applied to interchip circuitry.

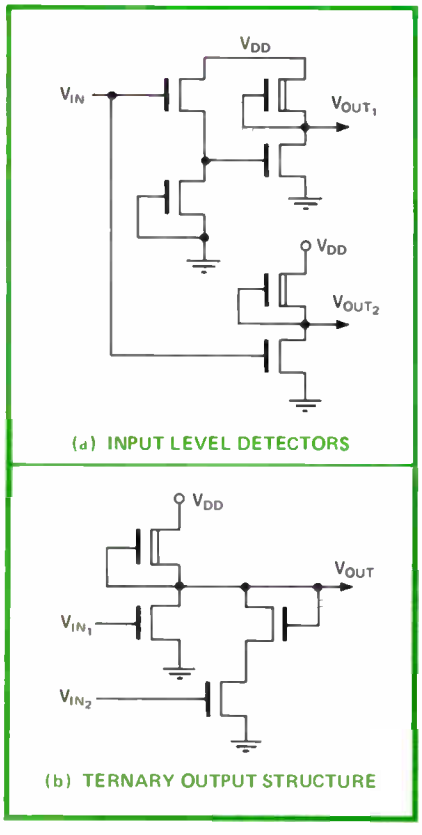
The MOS way. Early attempts to build multivalued chips centered on integrated injection logic, but recently attention has turned away from bipolar technology toward LSI MOS circuitry. Work with I²L does continue, but the faster offshoot, integrated Schottky logic, or ISL, seems more promising now. Multivalued logic is also being tried with charge-coupled devices and emitter-coupled logic. Nor have experiments been limited to silicon, either, as multivalued gallium arsenide ICs have also been proposed.

Results with MOS have been most encouraging, but for all practical purposes, it is confined to three-level, or ternary, logic because of tight noise margins, particularly if 5-volt logic is assumed. L. Keith Russell, formerly with Signetics and now at National Semiconductor Corp., Santa Clara, Calif., has devised some elegantly simple ternary logic elements that can use standard silicon-gate enhancement- and depletion-mode MOS technology if transistor gate-width and -length ratios are appropriately adjusted.

The illustration shows Russell's input level detector (a) and ternary output structure (b). Logic level 0 ranges from 0 to 0.5 V, level 1 from 2 to 3 V, and level 3 from 4.5 to 5 V. Thus, the levels are separated by a 1.5-V margin. The ternary output structure converts two binary signals into these three voltage levels; likewise, information represented in ternary logic will be translated back into two binary outputs via the input level detector.

Other functions. Besides binary-to-ternary translators, Russell has constructed a number of primitive ternary functions. The most primitive function in binary logic is simply inversion, but in ternary and higher logic forms a number of additional functions, like replicators, predecessors, and successors, are important. Replicators act as double inverters to

2 to 3 to 2. These standard n-MOS circuits convert ternary logic into binary (a), and binary input signals into a three-state signal. Many three-state circuits are also available.



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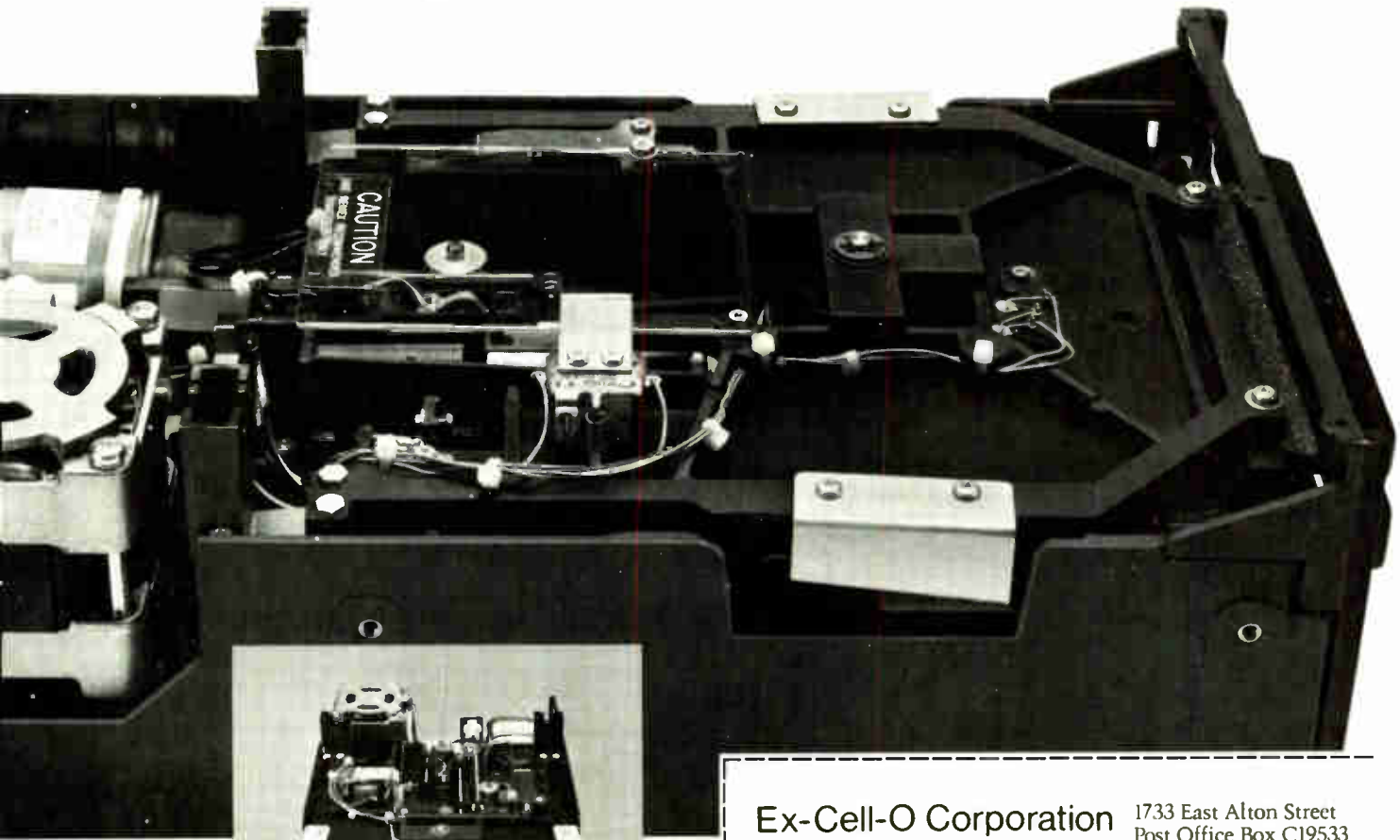

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reestablish the logic levels. Predecessors and successors produce the previous and the next logic outputs, respectively, based on the input; for instance, in ternary, a predecessor yields a 0 for a 1, a 1 for a 2, and a 2 for a 0.

Russell has also built up arithmetic circuits like half-adders and -subtractors and multipliers. He has also devised storage structures such as master-slave flip-flops and even a ternary static random-access memory cell. The cell requires 14 transistors, however—more than double that of a binary static RAM cell.

The reason the ternary RAM cell is so complex is that it must be written into as well as read out of. Multivalued read-only memory cells could be much more area efficient, a fact that Intel Corp., Santa Clara, Calif., has already proven with a quaternary ROM cell [*Electronics*, Oct. 9, p. 39] developed for the microcode sections of its 8087 numeric processor and the execution unit of its iAPX 432 32-bit microprocessor (see p. 119). Both applications store about 30,000 bits of microcode.

In fact, Intel's four-state cell stores 2 binary bits in less area than that of a standard ROM cell or the more compact X-shaped cell pioneered by Mostek for its MK 36000 64-K ROM (see table). In the 2-bit cell, there is still only one transistor per bit, but four different channel widths are used to vary its impedance. When a cell is selected, the voltage developed across it is based upon its impedance. So, to sense what is stored, Intel feeds this voltage to one of three comparators that have their other input tied to reference potentials equaling the memory's three interlevel voltages.

The ROM cell's worst-case access time is less than 100 nanoseconds. As shown in the table, although the area saved per cell is 46%, the total area saved is only 31% because the overhead per bit is similar to other designs. Intel explains that even more area can be saved—if performance is compromised—by employing a single comparator, instead of three, that goes through a series of tests using the different reference potentials until a match is found.

Intel has also looked into storing more than 2 bits per cell, but only 13% more area per cell is saved by moving to 3 bits. However, overhead per bit diminishes as the number of stored bits goes up, so that higher levels warrant continued investigation.

CCDs too. IBM Corp.'s Thomas J. Watson Research Center in Yorktown Heights, N. Y., is exploiting the analog nature of charge-coupled devices to store multivalue data in serial shift registers. The idea is to create variable-depth charge packets proportional to an input voltage, clock the charge around memory loops, and then convert the packets back into a representative voltage at the output. Binary data can be used to generate the input voltage, and an appropriate sense amplifier can bring back binary once again.

This basic principle has been used previously—indeed, a 128-K CCD memory was built by Mitsubishi Electric Corp. but processing tolerances and supply variations have degraded the operating range of the input and output interfaces—the launch and sense circuits, as IBM calls them. IBM's contribution improves upon these circuits, using a digital-to-analog converter for launching and an a-d converter for

COMPARISON OF READ-ONLY MEMORY CELLS

	Standard ROM	Mostek MK36000	2-bit-per-cell ROM
Area per bit, (μm^2)	210	169	112.5
Area per bit savings, (%)	0	20	46
Area overhead per bit,[a] (μm^2)	95.0	92.0	96.6
Normalized area overhead[b]	0.45	0.54	0.86
Area savings, (%)	0	13	31

[a](Total ROM area – cell array area)/number of bits [b]Value of [a]/area per bit

Source: Intel Corp.

sensing. Moreover, to minimize tracking errors, the converter in the launch circuit is also used in the sense amplifer.

The input converter is capacitively coupled to a common well used to both generate and detect charge packets. To launch one, the converter simply builds up the right amount of charge in the well and this packet gets shifted out. To measure a packet for sensing, the converter first empties the well to its greatest depth. Next the packet is moved in. Finally, a counter feeding the converter causes the level of the common well to move up in steps, and when the packet reaches the top, charge spills into a trigger that indicates the level.

By generating and decoding in the same well, virtually all geometry effects are eliminated, says IBM. The scheme is also faster and needs fewer control circuits. IBM folded its recirculating shift register into a circular series-parallel-series loop so that input and output are adjacent. The sensitivity of the detector is 1.5 femtocoulombs, and the company has simulated shift rates of 1.5 megahertz for three levels of storage using 4-micrometer gate lengths.

At the Twente University of Technology in Enschede, the Netherlands, quaternary CCD full adders are being built for a 31-bit binary correlator. In binary form, 26 full adders would be required; but with four-valued logic.

High speed. At the Université Pierre et Marie Curie in Paris, quaternary ECL circuits are being investigated with the hope of constructing a supercomputer. In particular, researchers are looking at the so-called Bayan network, which can contain up to 64 processors, each with 40 input and output lines. So the university decided to build a quaternary logic chip using a fast oxide-isolated process. In fact, two such chips are now being processed. One contains the four-state encoder and decoder and a reference bias network, and the second is mainly to test and characterize the process. According to researcher Daniel Etiemble, the multivalued approach must be carefully studied by IC designers so long as LSI is not easily realized in a technology significantly faster than silicon. □

Military

Advanced weapons come under fire

Military gear too complex to use and test systems that do not work are targets of two Government reports

by Ray Connolly, Washington bureau manager

Is advanced electronic technology too complex for military personnel to use and maintain? Does it take too long to prove out the latest technology and incorporate it to improve weapons systems?

These are a couple of the questions being raised in and around the Pentagon these days. As a result, military electronic systems have been caught in a crossfire of criticism that the high performance promised in prototypes is not being demonstrated in the operational systems deployed in the military forces.

The arguments are that electronic systems in particular have become overly complex, designed by highly skilled engineers for use by troops with limited skills; incorporate too many unproven innovations, while stressing the lowest bid rather than quality and life-cycle costs; and are difficult to maintain despite a $15 billion inventory of automatic test equipment in the Air Force and Navy alone.

The critics. Two new critiques of advanced military technology and its failure to perform as promised are getting increasingly widespread readership in the capitol. First is a slim but strong statement titled "Defense Facts of Life" produced by the Defense Department's Office of Program Analysis and Evaluation and signed by Franklin E. Spinney. The Spinney Report, dated last Dec. 5, but only made available in early February, contends that "advanced technology and high complexity are not synonymous." They often become so, however, because the military bureaucracy, its contractors, and the Congress make it happen, it argues.

Better known is the General Accounting Office's report to the Congress that the "effectiveness of U. S. forces can be increased through improved weapon system design." The GAO's 61 pages, replete with appropriate horror stories of "undependable" sophisticated weapons [*Electronics*, Feb. 10, p. 59], calls for greater consideration of quality assurance and logistics support. It also calls for greater consideration of human, user issues—including combat stress and fatigue, as well as relatively low skill—early in a design process that now stress program cost, schedule, and performance.

Too much technology? Using complex and often unproven technology to achieve weapons system superiority generates more problems than it resolves, says the GAO. And the argument is supported by military leaders as well as a panel of 18 industrial and academic leaders consulted by the investigators in its study (see "The view from the outside"). "Constant striving to achieve technological excellence is causing undue technical complexity, leading to high cost and long gestation" in weapons development, former Army Chief Bernard N. Rogers told the Congress last year.

The GAO also notes that William J. Perry, the DOD's former under secretary for research and engineering, believes that "a dangerous communications gap" between weapons users and their developers has led to technology-driven systems that "are poorly united to the operation need because the user did not know how to state his need in terms of available technology." Compounding that are R&D programs that give inadequate weight to field support costs and user skill levels. The result: low readiness and large outlays for retrofits.

Relatively low military skill levels and inadequate training, the industry advisory panel told the GAO, is leading to phasing men out of the system in favor of more built-in test equipment, removable/replaceable modules, and factory or depot repair, rather than on-line diagnosis and repair. The approach, the industry managers noted, "leads to rather complex electronic components and can increase the number of 'black boxes' needed in the supply sys-

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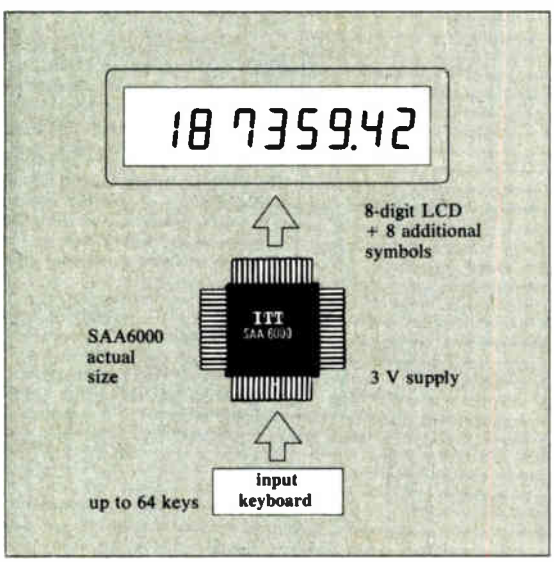

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tem"—another costly approach.

The Spinney Report is considerably more scathing than its GAO counterpart, but makes many of the same points using the weapons experience of the Tactical Air Command to address the larger issue of changing the DOD's Planning, Programming and Budgeting System (PPBS). Though Spinney notes the TAC was chosen because it was less subject to budget cutbacks in the late 1970s than other services, the critique has some Air Force leaders burning. The report states that TAC has the same problems with maintenance equipment, spares, and personnel skills as everyone else.

Excessive system complexity, Spinney says, is encouraged by military project officers and their contractors who know their chances of being funded improve when they can promise more "kills per dollar," since this is an accepted measure of system capability. Like the GAO's criticism of project emphasis on cost schedule, and performance at the expense of lifetime operation and support costs, Spinney notes that project competition is intensified by rewarding a sponsor "in accordance with how successfully he moves 'his' program through the bureaucracy."

The squeeze. One product of this PPBS approach—particularly as few systems are canceled outright after a significant investment—is, he points out, "a cost-budget squeeze," in which "the sharply increasing cost of replacement slows modernization, and the rising cost of low readiness—operating costs that must be absorbed—squeezes the overall investment budget, leaving less money to modernize with more expensive equipment."

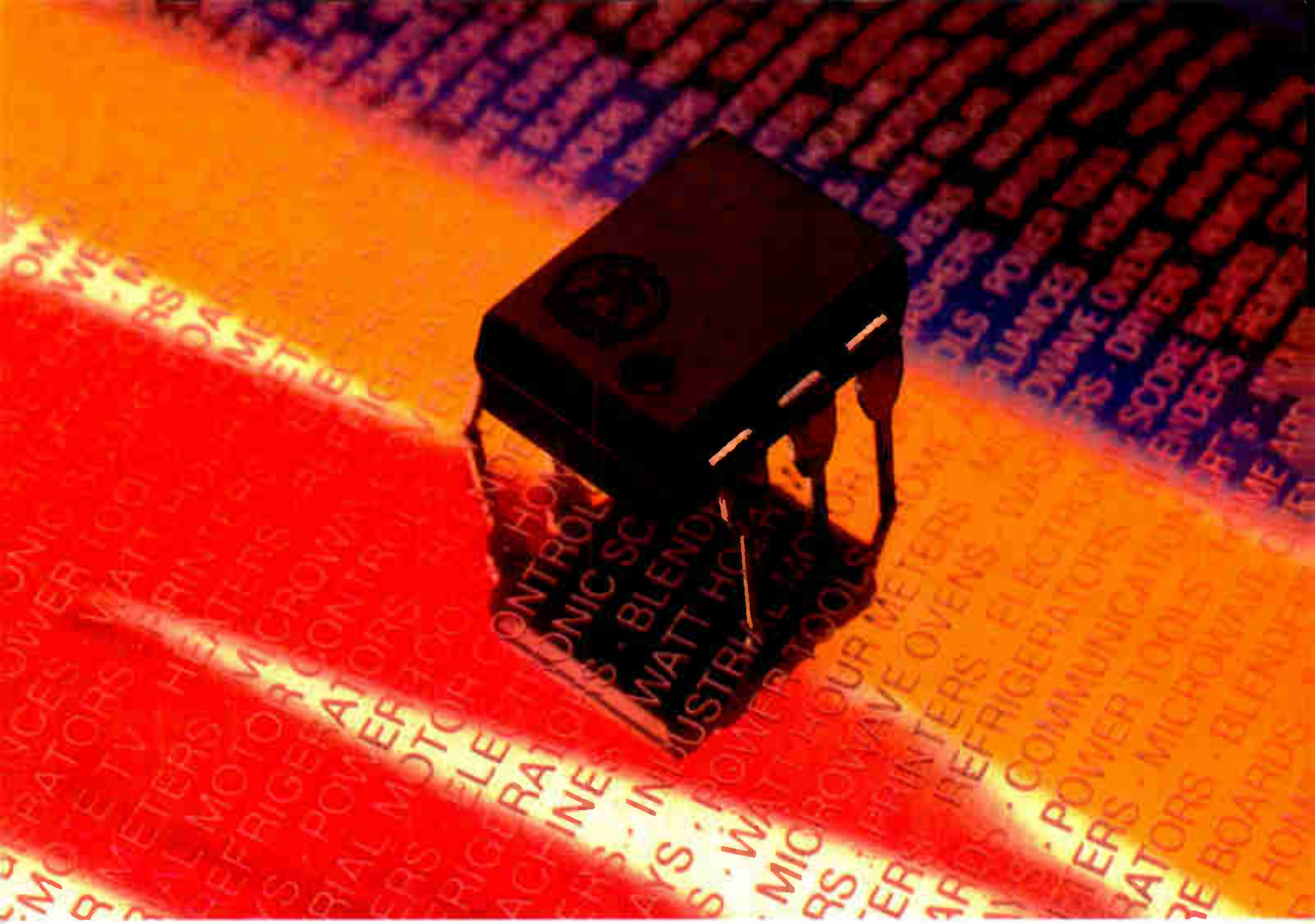
The Pentagon and the services' planning systems and economics "tend to discount the present and inflate the future" by arguing that newer and better systems on the drafting boards will more than compensate for today's low readiness. Yet the complexity is just not working. "We need to change the way we do business, and in particular, we should use our superior technology in a positive way. Technology should and can increase readiness, not draw it down," Spinney argues. □

The view from the outside

One uncommon feature of the GAO report is that it solicited the views of 18 top management officials from the defense industry and academic community and incorporated a summary of their recommendations separately. "Their agreement with most of our recommendations was a pleasant surprise," says one source at GAO, who was even more surprised that the Defense Department called the congressional investigators' analysis "excellent and well-balanced."

The special procurement advisory panel contributed some 19 recommendations of its own on systems design procedures, quality, and usability, too. Key suggestions among them were to:

- □ Assign civilian program managers to projects from beginning to end, instead of military officers whose three-to-four-year tours of duty are dominated largely with a concern about what happens on "their" watch.
- □ Provide contractors with financial incentives and responsibility for designing more supportable systems with reduced operating and maintenance costs. A rating system should be included that emphasizes logistics support for use in development systems proposal requests.
- □ Improve military systems for reporting on problems experienced with fielded systems, so that engineering analysis can identify causes.
- □ Emphasize direct evaluation of a contractor's quality assurance program by program offices, instead of using system design evaluation as a means of identifying quality assurance goals.
- □ Revise the DOD's glossary defining supportability—a subject with serious semantic problems.
- □ Make "a major effort" to reduce the number of DOD directives, specifications, and regulations.
- □ Make sure that manuals and training courses intended for secondary-school-level users are not written by "the wrong people"—engineers.



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Business

Detour ahead for IC equipment makers?

Semiconductor capital equipment spending is predicted to drop, but there is little agreement on how far and when

by James B. Brinton and Linda Lowe, Boston bureau

The road signs for makers of semiconductor manufacturing equipment are pointing every which way. Good times could be ahead or they might not. There could be a dip in the road for capital equipment buys by semiconductor makers in 1981—or not until 1982.

After two boom years, in which capital expenditures increased by 60% to 70% in 1979 and by another 30% to 50% in 1980, market analysts disagree on how bright or dim the picture for 1981 will be.

The mix of optimism and pessimism, coupled with the uncertain timing of the various market projections, is making almost everyone associated with the capital equipment end of the semiconductor business a little nervous, and it is making the stock market nearly panicky (see "A case of market jitters").

Poles apart. The differences in opinion between observers is evident in the contrasting views of Michael J. Krasko, technology group vice president for New York–based Merrill Lynch Pierce Fenner & Smith Inc.; his associate Thomas P. Kurlak; and Kent A. Logan, vice president of Goldman Sachs & Co. in New York.

Logan feels that 1981 can be a good year and cites the capital expenditure plans of Intel, National Semiconductor, Signetics, and Fairchild. As recently as last month all of these firms had planned to spend anywhere from 20% to 70% more on plant expansion in 1981 than in 1980. "There's sure to be some scaling down of these figures later," comments Logan, "I expect 1982 to be the soft year, not 1981."

He adds that until six months ago he would have projected less growth. "During the last two recessions, semiconductor makers halved their capital equipment expenditures, and I expected similar behavior this time, too. So far it isn't happening—the industry appears to be living up to its pledge to 'build through' the recession, even in the face of soft orders and profits. They are running now to stay competitive with Japan later."

Krasko and Kurlak are less sanguine. "Yields are up, money is tight, orders are down, and profit margins are narrowing for semiconductor houses," says Krasko. "Though some semiconductor capital equipment sectors will be strong—notably plasma etchers [see p. 183], wafer processors, and VLSI testers—others are going to be weak and some very weak." Krasko expects a 10% to 20% growth rate for the capital equipment sector in 1981. Thus Logan's 1982 slump already is written into Merrill Lynch's 1981 scenario. But Kurlak looks for a return to health in 1982.

Still, there is reason for pessimism. At the Information Services Seminar held earlier this month by the Semiconductor Equipment and Materials Institute in Newport Beach, Calif., capital equipment makers listened to gloomy reports from industry observers. Howard Z. Bogert, director of technology for Dataquest Inc., the Cupertino, Calif., market research firm, noted that the 48% growth rate of capital equipment sales of the past five years could not be maintained. Dataquest's forecast for the next five years is nearer 20% to 25%.

Good performers. Other observers, though, distinguish between the poor prospects for mature production technologies and the bright outlook for advanced ones like dry processing. Buoying orders for advanced equipment are the increased yields and throughputs they promise, making such high-priced equipment attractive to semiconductor houses fearful of losing market share. Says Goldman Sachs' Logan, "It's as if the Japanese have forced U. S. firms into long-term planning." □

A case of market jitters

As an example of how close analysts are watching semiconductor equipment firms these days, take the case of GCA Corp. Last month its shares dropped 22% to $49 in one day's trading. The trigger was pulled by a Merrill Lynch advisory issued in spite of GCA 1980 sales and earnings increases of 76% and 145% respectively.

Merrill Lynch vice president Thomas P. Kurlak blew the whistle for three reasons: a drop in GCA's backlog from just over $157 million to about $143 million—not a typical cause for executive suicide; what he deemed to be the stock's high price-earnings ratio; and the expectation of a marketwide falloff in orders.

Though GCA stock is more volatile than many a firm's in this market, the Burlington, Mass., company's experience underlines the uncertainty about the future of the semiconductor capital equipment market.

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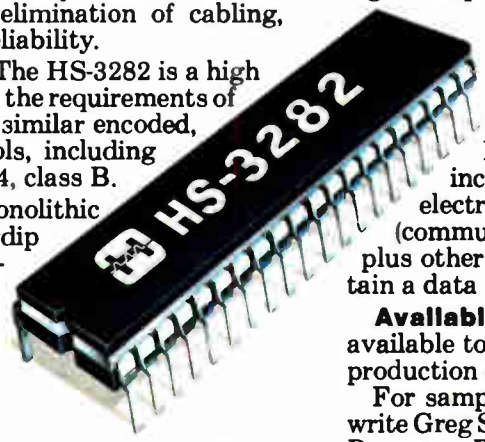

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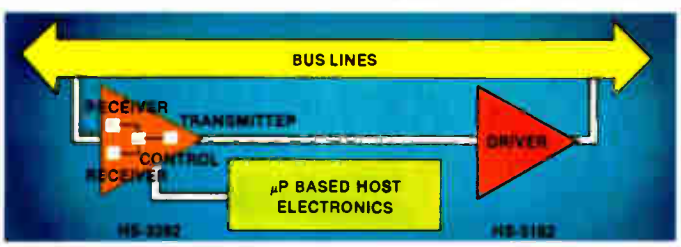

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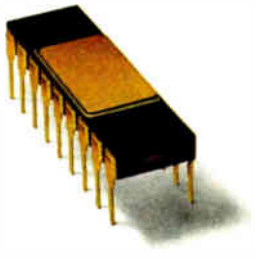

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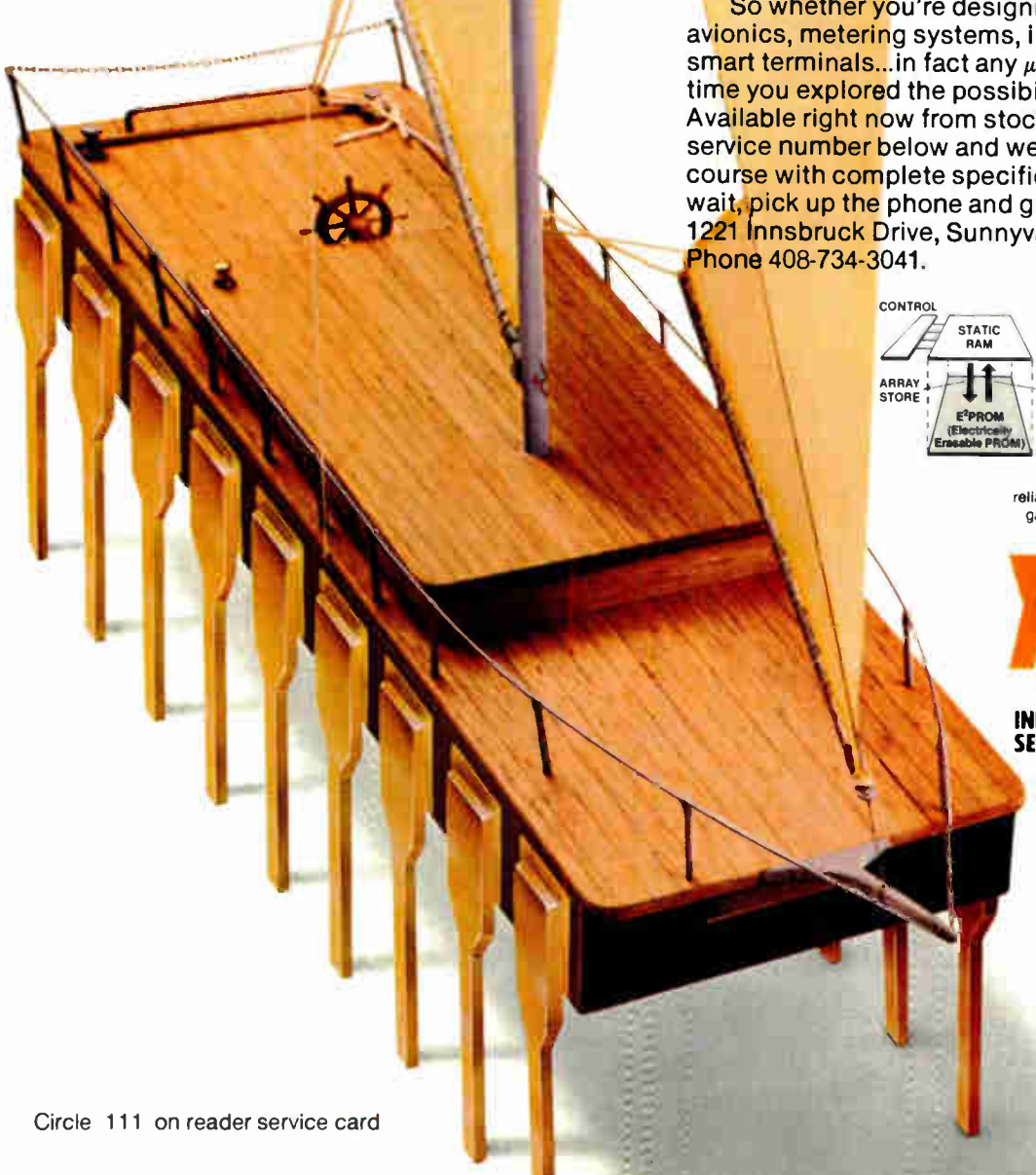

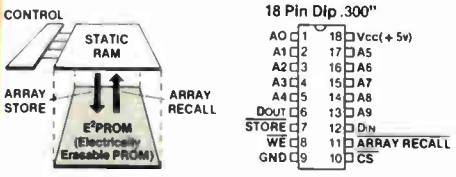

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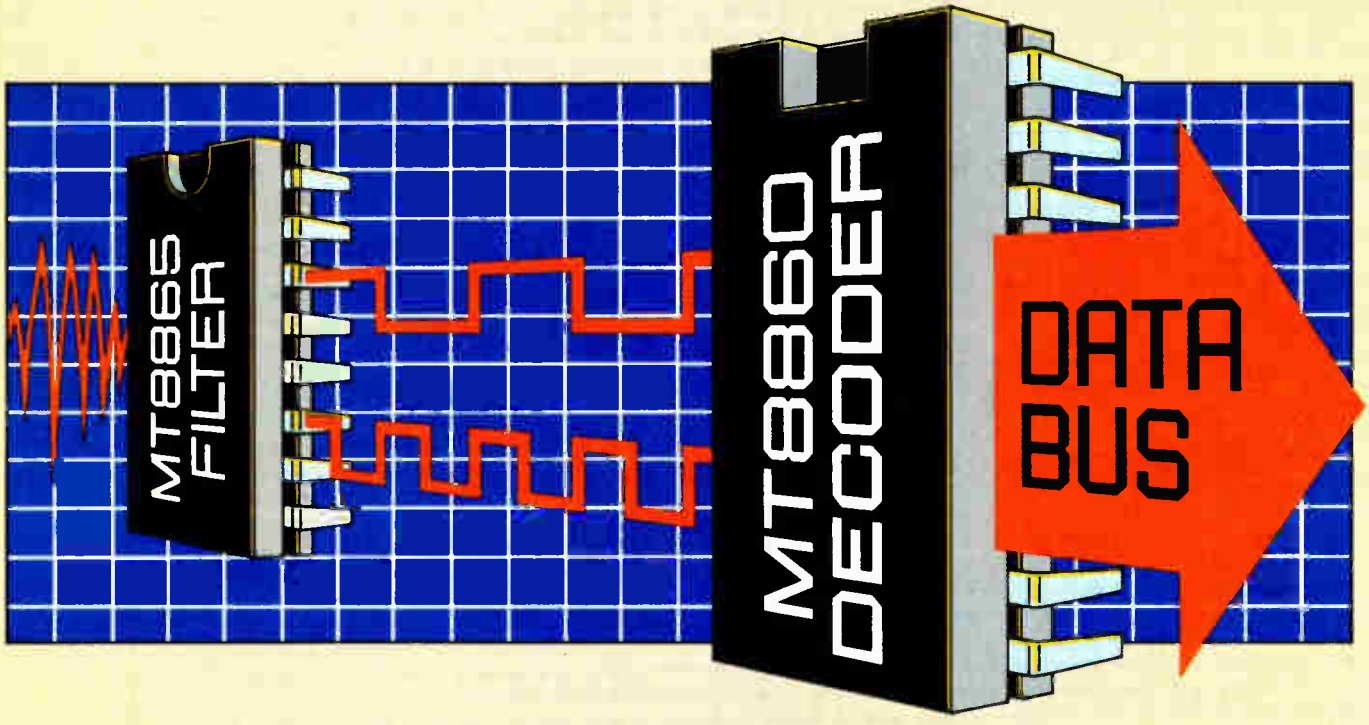

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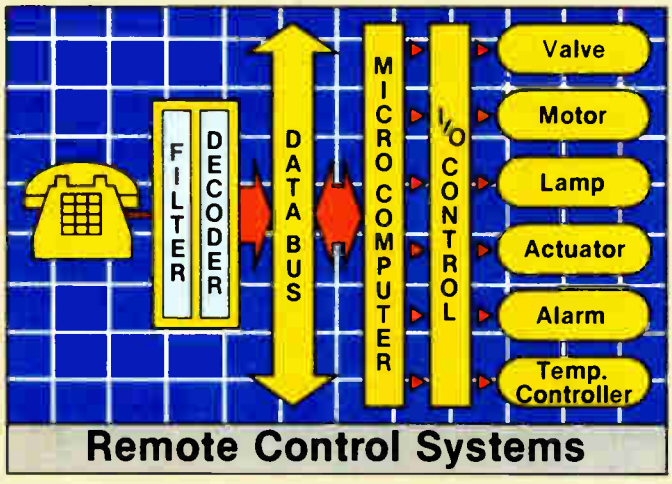

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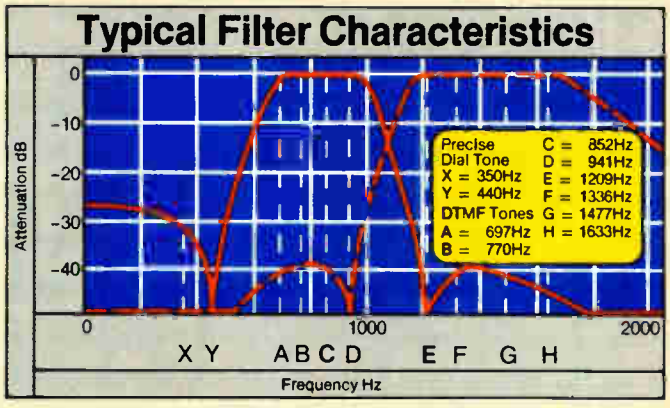

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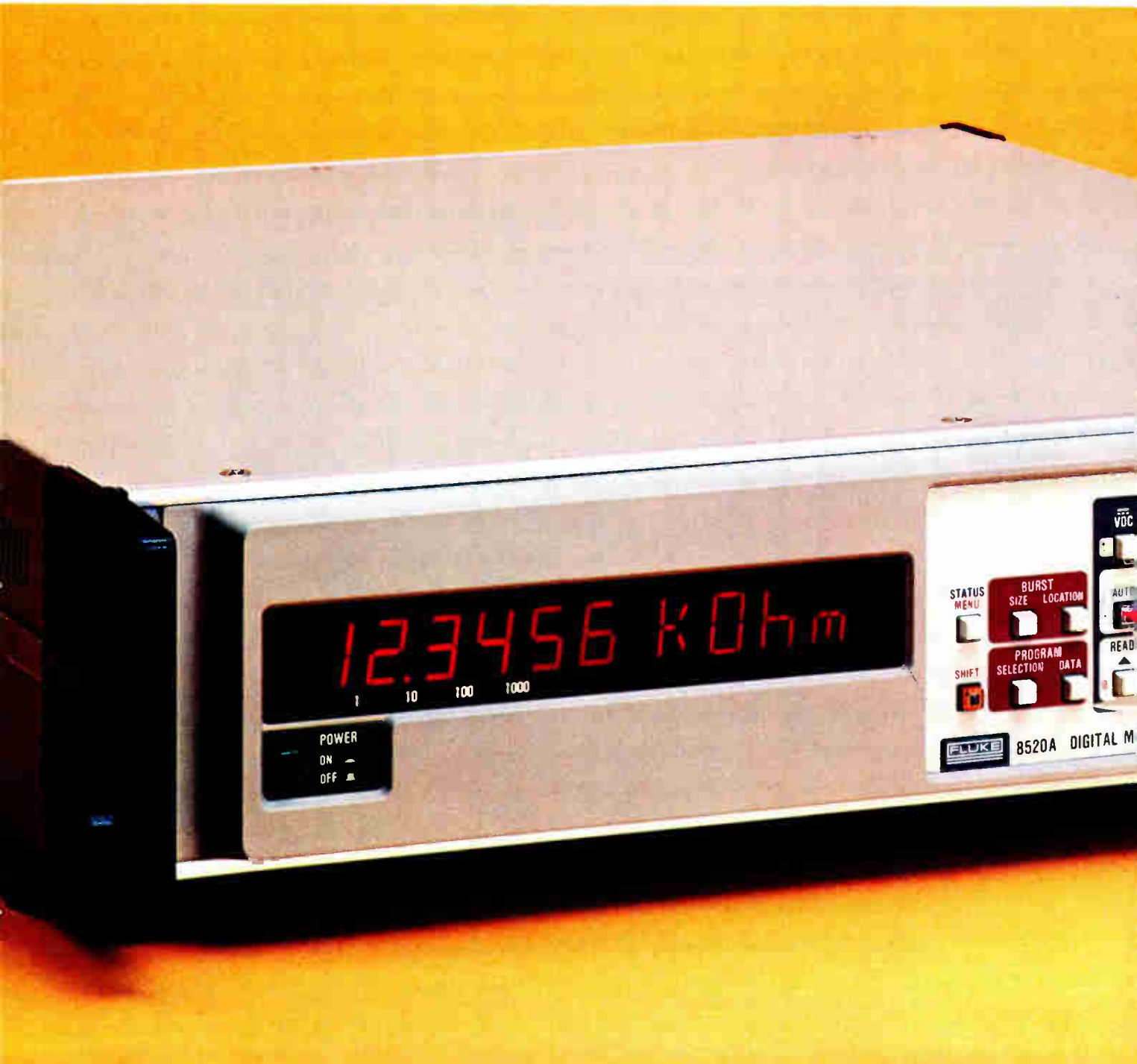

systems/bench DMM from Fluke

Readings can be captured at high speed for subsequent processing. Or they can be printed-out. Both operations had previously slowed the data acquisition process.

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In your system, the internal processing of the 8520A reduces software overhead and makes your system controller more effective at doing its job, controlling instrumentation.

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For Technical Data Circle # 115

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Fluke has good news for builders of automated test systems: instrument control just got easier. With our new 1720A, we've provided the missing link in available systems technology that gives you total control: from design, through software development, to the production environment.

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Instead, the operator interacts directly with the screen on the 1720A—a soft-labelled CRT display

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that you program according to the skill of the user and the specifics of your test procedure. Your software presents instructions, choices and even safety warnings to the operator via the display, as well as measurement data from instruments in the test system. The operator responds by touching designated areas of the display, and is able to work through even complex routines quickly after a minimum of training.

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With the operator's attention focused only on the 1720A display for all control functions—instead of being split between an assortment of devices—productivity can be improved dramatically.

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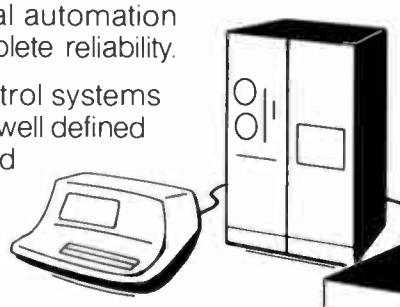

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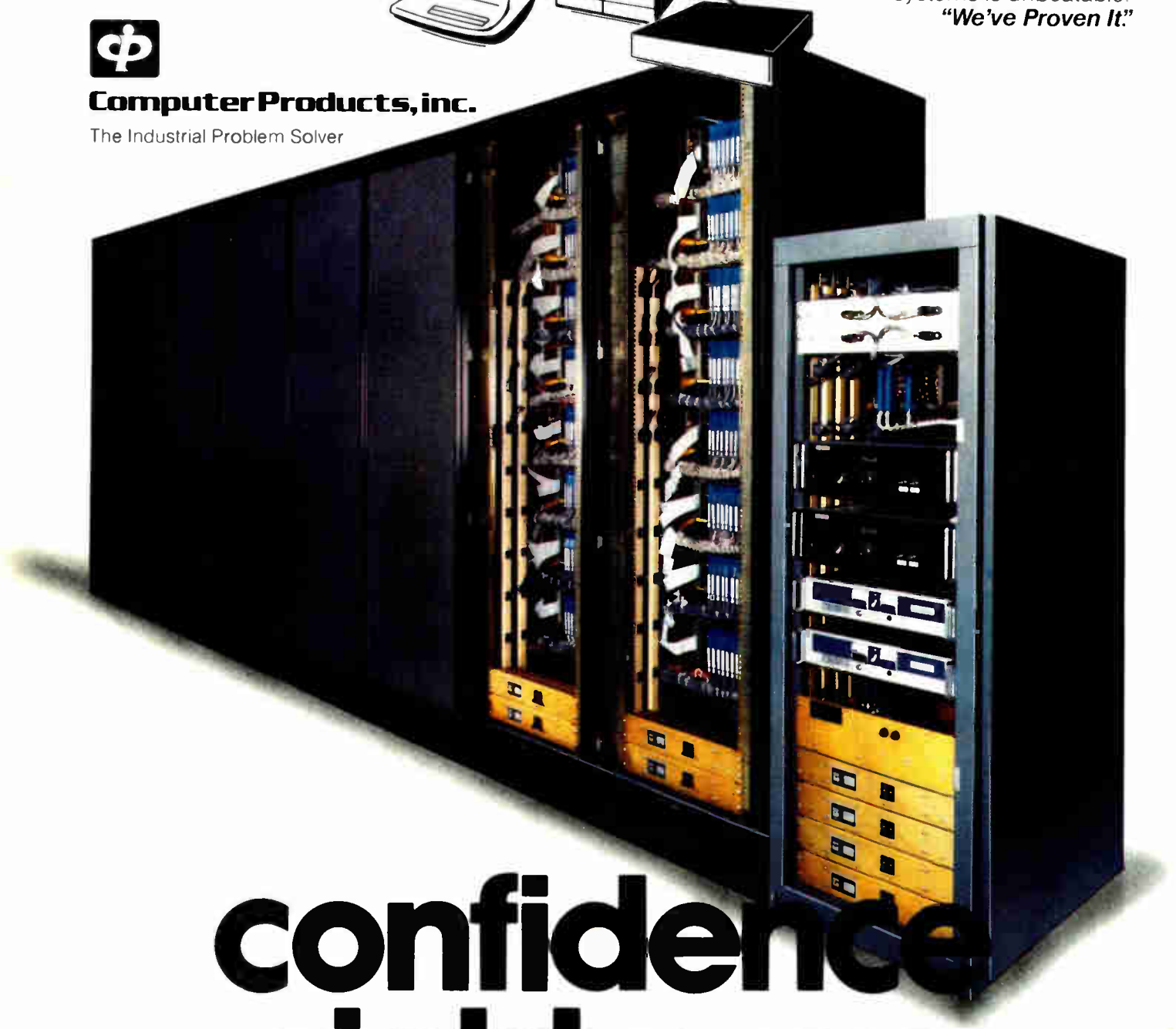

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Ada determines architecture of 32-bit microprocessor

Its use of the high-level language makes the chip set easy to program for multiuser, multifunction applications like office systems

by Justin Rattner and William W. Lattin *Intel Corp., Aloha, Ore.*

☐ Generation after generation, microprocessors increase in sophistication. And the time and cost of developing new applications for them escalates also, till by now skilled system designers and programmers are in very short supply.

Anticipating this critical situation, Intel Corp. undertook to develop a microcomputer system that can be made to handle complex, software-intensive applications in much less time and at much lower cost than has been usual. The project encompassed nearly all aspects of computer technology and resulted in the development of a new semiconductor process—high-performance MOS, or H-MOS—a new package with a high pin count—the quad in-line package or QUIP—and three of the largest integrated circuits in history (see "A history of the Aloha project," p. 125).

Its crowning achievement thus far is a 32-bit microprocessor—the iAPX 432—that has a major new architecture, a new operating system (iMAX), and one of the first compilers for Ada, the Department of Defense's new standard programming language.

As the first 32-bit microprocessor designed specially for multiuser applications, the two-chip general data processor (GDP) is a significant milestone in computer technology (Figs. 1 and 2). Together with the single-chip interface processor (IP) shown in Fig. 3, it was designed to serve the kind of cooperative, multifunction applications typified by future office information equipment and distributed data-processing systems. Similar systems are also envisioned for use in computer-aided design and factory automation.

Cooperative multifunction applications share four important characteristics. They are large in scale and broad in scope, requiring mainframe computing power. They are software-intensive, each discrete function or service requiring considerable programming. They are expected to evolve over time, so the design must allow for future software enhancement and increments in performance. Finally, they are applications where the failure of the computer system can have serious consequences to human life or the cost of doing business, so that long-term dependability of both hardware and software is essential.

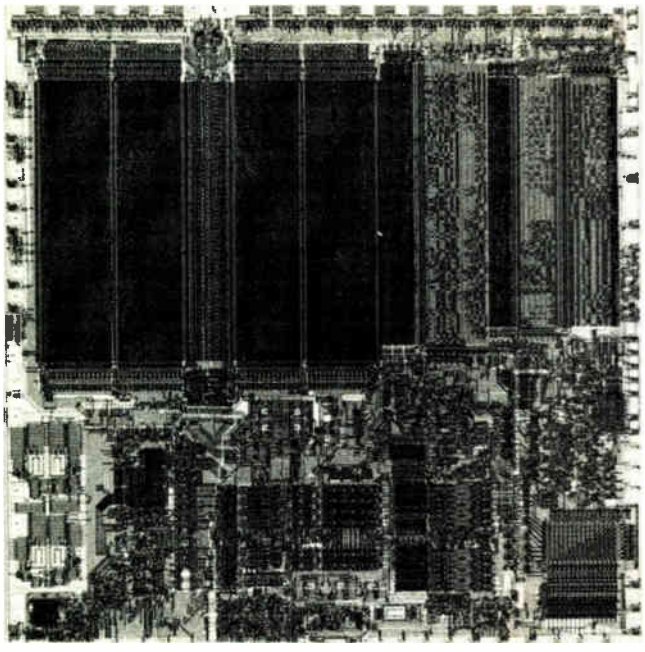
Those characteristics of cooperative multifunction applications guided the 432 designers to its major goals. The breadth of computing power required, in terms of both function and performance, includes support for multiprogrammed and virtual memory operating systems; as such, ultimate performance for fully configured systems was to be that of a mid-range mainframe.

Further, it was decided that the long-dreamed-of incremental performance capability—adding power to a 432-based product already in the field simply by plugging in additional GDPs and IPs—would gracefully accommodate planned or even unplanned growth in computational power over the life of an application. The goal of increased programmer productivity was met by supporting a comprehensive methodology for modular software development, served by using Ada as the 432's native tongue. And finally, to ensure high hardware and software dependability, the 432 includes extensive hardware fault detection and software-protection mechanisms.

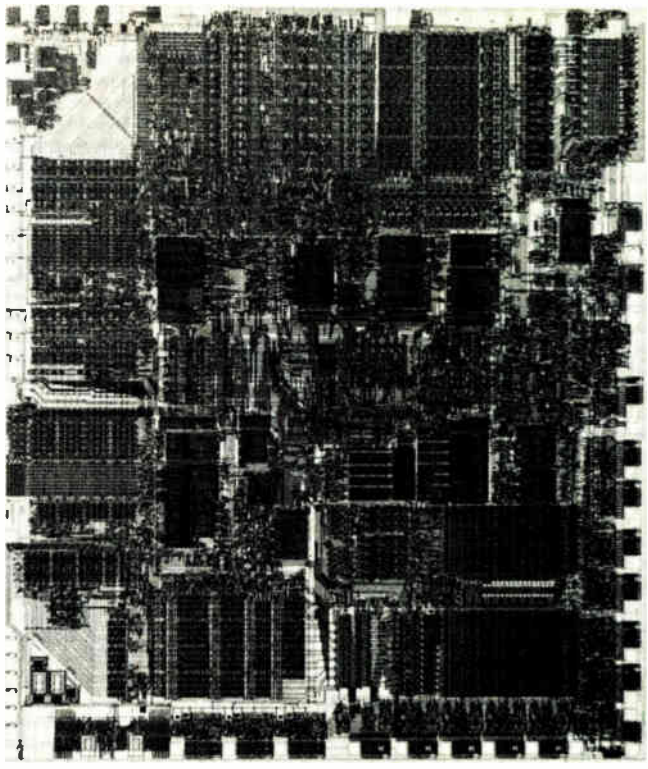
Transparent multiprocessing

Through careful attention to multiprocessing issues in the definition of both its system organization and its architecture, the 432 successfully implements the long-sought-after idea of transparent multiprocessing for general-purpose computation. This simple but important concept means that the number of data processors in a 432 system can be increased or decreased without software modification. It is even possible to start or stop a processor at any time without informing, let alone damaging, a single piece of software. More importantly, neither the operating system nor the application programs need rewriting to exploit an increase in the number of processors.

A principal challenge in the development of any multiprocessing system is the design of the interconnection



1. Instruction decoding. One of the two chips that make up the general data processor, the 43201 is the instruction decoder. It contains more than 100,000 devices on a single die, making it one of the densest VLSI circuits to have been fabricated so far.



2. Microexecution unit. Decoded instructions from the 43202 are executed by the 43202, which has over 60,000 devices on chip. Its unusual horseshoe-shaped data bus can be discerned from the photograph. The device is housed in a 64-pin quad in-line package.

structure that ties the processors and memory subsystem together. The 432 approach to this problem is unusual: rather than define a standard bus, the 432 simply defines a standard way for processors to communicate with memory and each other. This frees the designer to choose his own bus structure, optimizing the cost/performance ratio of the application. All 432 processors are compatible with the interconnect protocol.

The main goal of the interconnect protocol is to reduce bus use. For that reason, it puts requests and replies in separate packets, so that the first need not monopolize the bus while waiting for the second. For example, a processor generates a request packet in order to access memory but expects a reply packet (Fig. 4) from the memory system only if the request specified a read cycle. The result is that the processor ties up the bus only long enough to transmit a packet to the interconnect; sometime later a reply packet will be returned, if necessary, to the requesting processor. In the interval, other processors may be active on the interconnection.

For still greater efficiency, the protocol defines packets as variable in length. A single request or reply may transmit from 1 to 16 bytes of information. Fewer individual storage accesses need be made to obtain long operands, and designers using the 432 can improve system performance by widening the interconnect's bus.

Communication between processors is one of several additional functions supported by the interconnect protocol. Because of the packet format, a processor can send an attention signal to one processor or broadcast it to several processors simultaneously. Upon receiving a signal, a processor examines an interprocessor message area defined in memory. The message previously deposited there by the sending processor will instruct the receiving processor as to the desired course of action. Typical interprocessor messages can direct either one or a set of processors to start, stop and redispatch.

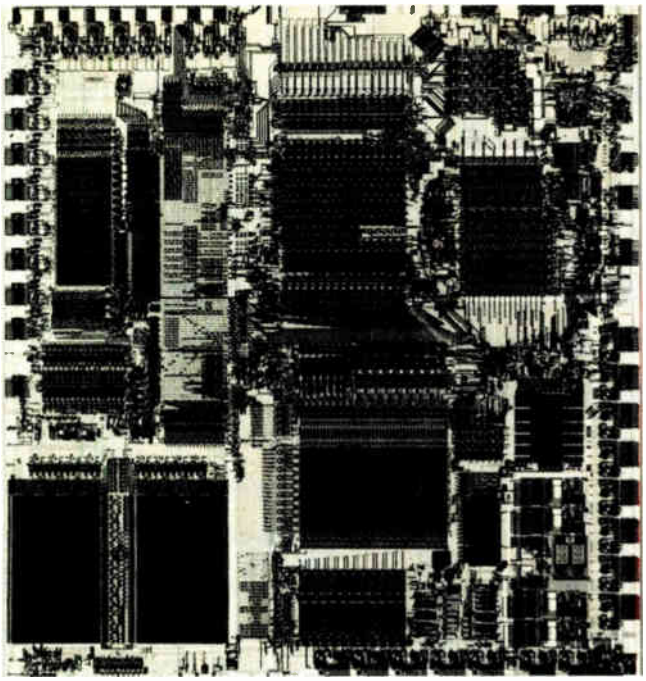
Many bus structures can be designed to meet the 432 packet protocol. A simple, single bus interconnect implemented in discrete logic is shown in Fig. 5. On this bus, the packets are demultiplexed as they leave the processors. The separate address and data lines are interfaced to a static memory subsystem in the conventional way. Up to four processors can be supported without serious contention by this simple interconnect.

A conventional mainframe often offloads onto a minicomputer all responsibility for low-level device control and data transfers. The 432 general data processor (GDP) uses an attached input/output processor in the same way. Device driver execution, device interrupts, direct-memory-access channel initialization are all handled within the I/O subsystem.

Offloading I/O chores

A typical I/O subsystem is built around a Multibus or other standard microprocessor system. A standard microprocessor, such as an 8086, is connected to the bus along with memories and peripheral devices to form a complete, attached I/O processor.

The GDP is connected to the microprocessor-based I/O subsystem by the 432 interface processor (IP). Under software control, a group of programmable, associative memories in the IP called window registers can be programmed to map a subsystem's address space into the 432's. The mapping operation is totally transparent to the attached I/O processor, so that both read and write



3. Input/output support. The single-chip interface processor, 43203, offloads the general data processor of the tasks involved in communicating with input/output devices. It includes 65,000 devices and can emulate many of the general processor's instructions.

cycles on the subsystem bus can proceed normally.

All communication in the 432's central system is based on messages and not interrupts. The IP receives those messages sent to an I/O subsystem and holds them in its window registers while signaling the I/O processor with an interrupt. The I/O processor then fetches the message through the IP window.

Communication in the opposite direction is slightly more complex. Since conventional interrupts do not exist in the central 432 system, the IP must give the attached processor the ability to send messages in the same way as a 432 data processor. The IP looks like a memory-mapped peripheral to the I/O subsystem as the latter writes commands to the IP registers. In passing those messages into the central system the microprogrammed logic of the IP emulates many of the same functions found in the high-level instruction set of the 432 data processor. Among the available commands is one to send message. Consequently a 432 data processor cannot detect any difference between messages sent by an IP and those sent by another data processor.

Multiple I/O subsystems may also be used to incrementally increase I/O processing power much as mulitple data processors increase processing power for general computation. By multiprocessing both I/O and data, the 432 serves many more applications than existing microcomputer systems can and meets the major goal of incremental, field-expandable, processing capability.

On chip

The processing units of the 432 are designed to exploit very large-scale integrated H-MOS technology to the full. The two-chip 43201/2 GDP, whose microphotographs appear in Figs. 1 and 2, contains 160,000 transistors. Over 100,000 devices are on the 43201 alone. The single-chip IP in Fig. 3 holds roughly 65,000 transistors. Each of the three 432 chips is housed in a 64-pin QUIP, as shown in Fig. 6 [*Electronics*, Jan. 4, 1978, p. 130], and each dissipates less than 2.5 watts of power from a single 5-volt supply. Two-phase clocking at 8 megahertz yields the nominal 125-nanosecond microcycle time.

These complex components could not have been developed without several advances in design techniques and tools. Among these was the use of regular logic structures and wiring topologies.

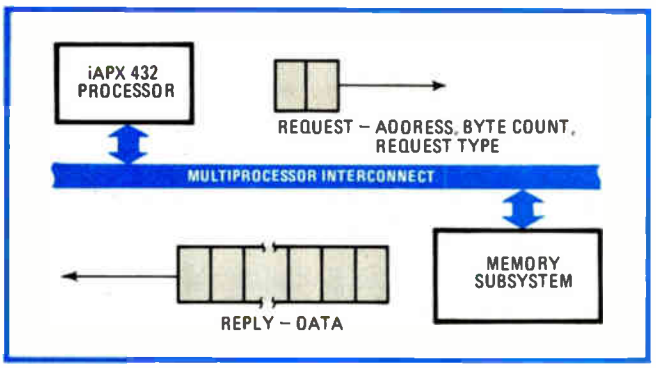
This technique, developed almost simultaneously at Intel by Sam Schwartz and at the California Institute of Technology by Carver Mead, dramatically reduces the number of randomly drawn transistors. Creating a structured integrated circuit design is hard but gets easier with practice. The micrographs reveal a general increase in geometric regularity from the earliest of the chips to be developed, the 43201, to the latest, the 43203.

Both the GDP and the IP are microprogrammed and rely on high-performance microarchitectures to minimize microprogram size. The two-chip GDP contains a 4-K-by-16-bit microprogram ROM, and the IP contains a 2-K-by-16-bit ROM. The physical size of the IP's microprogram ROM is further reduced by having 2 bits stored in each ROM cell, a technique developed for the 8087 numeric data processor [*Electronics*, Oct. 9, 1980, p. 39] and improved upon in the 432.

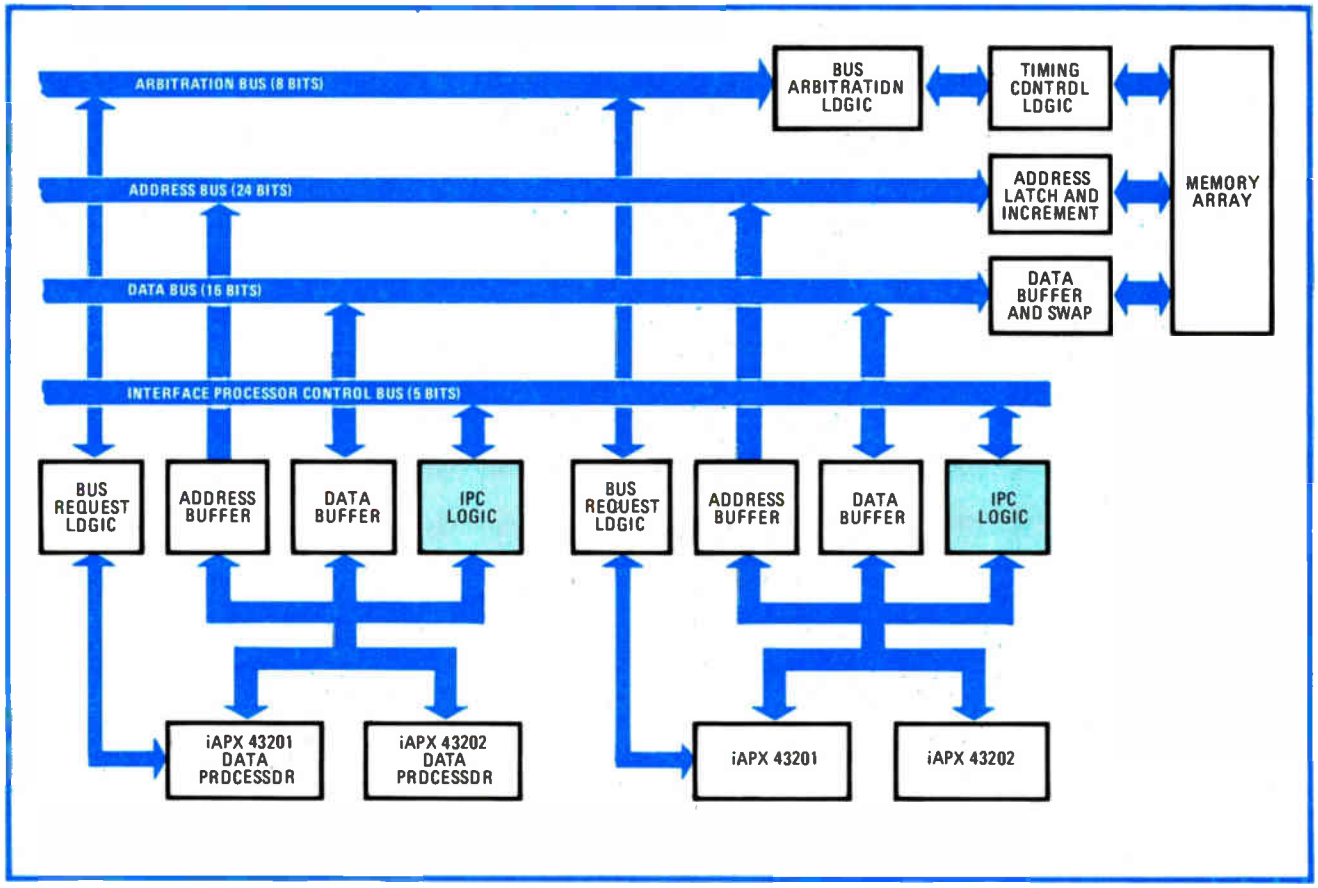
The last two entries of Table 1 mention two of the more interesting functional capabilities of the 43201 and 43202. The address generator on the 43202 is responsible for mapping or translating 432 logical addresses into the physical addresses used to access the memory system. To accelerate the translation process, the address generator maintains a cache of recently used addresses, so that a new entry automatically replaces the one least recently used.

The silicon operating system is largely in microcode with some simple hardware assistance. Consequently the execution time for a typical operation like "send message" is five times faster than for a highly tuned minicomputer operating system and 20 to 30 times faster than for the best mainframe operating system.

Table 2 describes the allocation of microcode in the 43201/2 data processor and provides one of the most



4. Quantized memory requests. Since memory is shared by several processors, requests to access it are optimized by being quantized into packets. A processor controls the bus just long enough to make a request and receives a reply only if the request was to read.



5. Many bus structures. Illustrated is the minimal bus structure consistent with the iAPX 432 architecture. Many other configurations are possible as long as they adhere to the quantized packet protocol of the 432. For example, a faster bus might use wider data paths.

important clues to the functional power of its microarchitecture: only 6% of the total microprogram is required to implement the basic instruction set. The low percentage is due to the close match between the basic instruction set and the microinstructions. Many instructions can be executed by just a single microinstruction. These microinstructions emerge directly from the instruction decoder located on the 43201 and therefore do not take up space in the main microprogram ROM.

Virtual addresses

Virtual addressing, another important 432 function, uses only 7% of microprogram space on the 43201. This percentage is kept small by a little extra hardware, in the form of back-up copies of certain key registers. When a requested memory segment is not in RAM, microcode can restore the machine to the state it was in when the requesting instruction started. System software can then bring the missing segment in from secondary storage and execute the instruction afresh. The entire operation is transparent to the executing program.

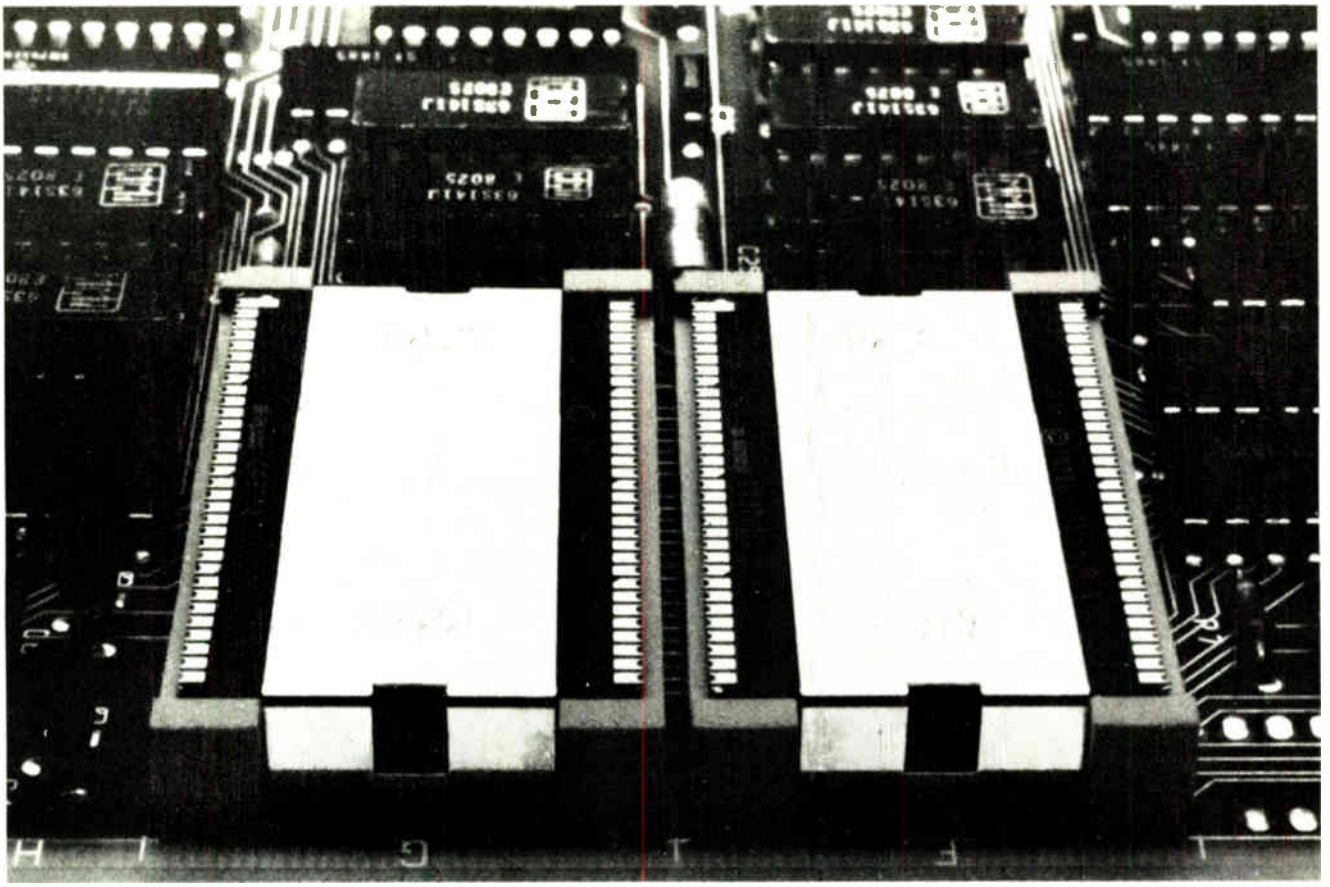
Table 2 also shows that a large amount of microcode is devoted to the silicon operating system. Many of the high-level 432 instructions, such as send message, are included in this total. Equivalent functions, programmed in the instruction set of a typical microprocessor, would take four to eight times as many bits.

All 432 components are designed to operate in two modes so that highly fault-sensitive systems can be built from them. In the master mode, a component operates normally. But in the checker mode—a feature never before found in a microprocessor—all the pins that would normally operate as outputs reverse themselves to function in a special input mode. Instead of asserting output data, they sample the states of their signal lines. The sampled data is compared internally, by an exclusive-OR gate built into each output stage, with the data that would have been asserted in master mode. A mismatch on any pin indicates an error.

A fault-sensitive unit is formed, as shown in Fig. 7, by simply wiring together two identical 432 components. One chip is placed in the master mode and the other in the checker mode by asserting the checker-mode pin. Any error signal asserted by the checker is routed to a special input on the master. In operation, the master and checker stay in lock-step synchrony. Any disagreement apparent at the output pins of the master is flagged immediately by the checker and freezes the operation of both units.

Longer and shorter

The instruction formats are designed to simplify and to reduce the size of code. Consequently, instructions vary in length and have from zero- to three-operand references. The operand addressing modes are modeled after the structures found in high-level languages like Ada to support scalar, vector, and record data types. These correspond roughly to the base-plus-displacement,



6. Quad in-line package. To house the 432 devices, a more reliable package was developed. The QUIP combines a leadless chip-carrier with a socket that has four staggered rows of pins on 100-mil centers. A metal clip helps dissipate heat, and test points are easily accessible

base-plus-index, and base-plus-displacement-plus-index addressing modes, respectively, found in conventional machines. Instructions also never refer to a register, since registers can be hard to manage during compilation. Instead, operands may come either from memory or from the hardware-supported expression-evaluation stack. Any mix of memory or stack-based operands is allowed. Lastly, the instructions may start and end on any bit boundaries. Naturally, branch instructions are designed to branch to a bit location, too.

With instruction formats such as these, the most frequent statements of a high-level language like Ada compile to single 432 instructions. Some examples are shown in Fig. 8, along with the corresponding instruction lengths (in bits).

An object orientation

The 432 has an object-oriented architecture. Objects provide an identical framework for everything from a simple piece of data, like a byte, to a message being sent to another processor. They are responsible for most of the facilities found in the 432 architecture, including basic computation, language run-time environment, resource management, interprocess communication, and protected addressing.

A data object supports basic computation. It is simply a linear, logical address space from 1-K to 64-K bytes in length. Any type of binary data can be stored in a data object, and a given element within the object is accessed by specifying its byte displacement from the starting address of the object. The complete logical address of a single data item, as found in the operand fields of a typical instruction, contains both the displacement and the program's local name (or nickname) for the data object. This short, local object name selects the much longer access descriptor, which indicates the location of the object's full name (or absolute address). The local name often runs as few as 6 bits in an operand reference.

More than ordinary

Just as data objects support basic computation in the 432, more complex objects are used to support higher-level functions. The hardware knows from their descriptor-type code that they contain more than just ordinary

TABLE 1: EXECUTION TIMES OF THE iAPX 432 32-BIT MICROPROCESSOR

Functional unit	Typical operation	Execution time at 8 MHz (μs)
Variable-precision integer arithmetic unit	32-bit integer multiply	6.25 (16 μs on IBM 370/148)
Microprogrammed floating-point arithmetic unit	80-bit floating multiply	26.125 (38.5 μs on IBM 370/148)
Barrel-shift unit	32-bit field extract	1.875
Address generator with associative cache of least recently used addresses	32-bit memory access	0.75
Silicon operating system	send message	80.875

TABLE 2: ALLOCATION OF MICROCODE IN THE iAPX-43201/2 DATA MICROPROCESSOR

Function	Bits	Percentage
Basic instruction set	3,680	6
Floating-point arithmetic	11,680	18
Run-time environment	6,400	10
Virtual addressing	4,800	7
Fault handling	2,640	4
Silicon operating system	26,400	40
Multiprocessor control	8,640	13
Debug services	1,280	2
Total	64 K	100

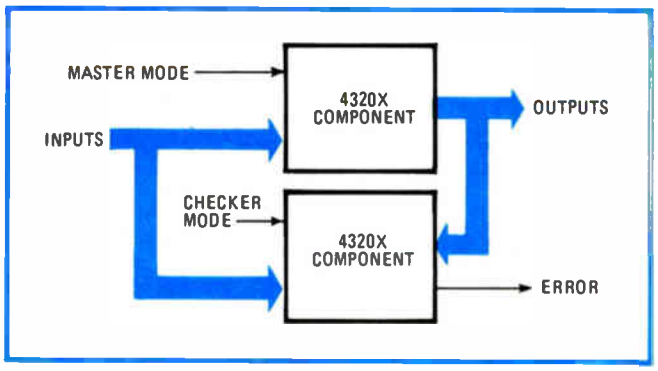
data and uses that knowledge to implement many functions carried out by software on conventional machines. The hardware-recognized objects are referred to generically as system objects.

System objects include domain objects and context objects. Both of these primarily support the run-time environments of high-level languages.

A domain object represents the addressing environment of a program module. Contained within the domain object are all the access descriptors for both the module's instruction objects and its data objects. The domain also contains links to other domains and thus is part of a network of domains representing a completely linked but still modular program.

A domain is actually composed of two parts—public and private—that are analogous to the interface and body portions of an Ada package [*Electronics*, Feb. 10, 1981, p. 127]. The public part contains the links to the objects defined by a module's interface specification, while the links to other objects not defined in the interface but used to implement the module are located in the private part. Only objects whose links are found in the public part of a domain object can be accessed from other connected domains.

Context objects support the dynamic allocation of memory every time they are activated. A context is created dynamically when a procedure is called and is deleted dynamically when the procedure returns. Since a new context is created for every activation, contexts directly support shared, recursive, and re-entrant procedures. Their second major function is to provide each procedure activation with a data object for its local data and an operand stack for expression evaluation.



7. **Error-checking mode.** Each 432 chip has a checker mode as well as a master mode. Two devices can be wired in parallel and one put in the checker mode to duplicate all the operations of the master and signal an error when it detects a discrepancy.

The remaining 432 system objects support the hardware-based operating system services called the silicon operating system. A data structure representing an individual GDP is called a processor object. There is one processor object for each physical GDP in a 432 system.

Some more objects

An object representing an independent concurrent program or task is called a process object. Processes may be scheduled to run on a processor and thus represent a claim on some part of the system's total processing resources. A process object contains, among other things, the priority of that process.

An object representing a portion of the allocatable or free storage in the system is called a storage resource object. Many such objects may exist in a system to partition storage in accordance with claims and grants. Through storage resource objects, new objects are created dynamically for software by the hardware.

A very flexible object that is used to support the buffered transmission of messages between processes, or programs, is called a port object. Port objects also support the scheduling and dispatching of processes on multiple processors in a multiprogrammed fashion. Ports are able to serve both functions because scheduling and dispatching is modeled as sending a message (the process object) to a process (the processor). In practice, the message is nothing more than an access descriptor. Since an access descriptor can reference any object, the send instruction can be used to send any object and, hence, any complex message. A message might be a data object containing a string of text or a complex object including executable code and perhaps representing an important system resource. Objects, therefore, present a consistent framework in which both processes and processors may communicate conveniently.

Object addressing

Objects are stored in pieces of the address space called segments. Simple objects can be stored by a single segment, but complex ones may occupy many of them. Important information about each object, including its type and location in physical memory, is found in its object descriptor. An object is always addressed via this descriptor, the location of which is indicated by an access descriptor (Fig. 9).

Length information is used to protect the object from out-of-range addresses, and presence information, along with other data in the object descriptor, is used to implement virtual memory. To simplify storage management, all object descriptors are grouped in a central table. Naturally, the object table is an object, too, and its object descriptor is contained within itself.

To select or refer to an object requires a 32-bit access descriptor that contains the identity of the object it references. Each access descriptor also contains other information to help control access to the object to which it refers. Different access rights can be represented by different access descriptors for the same object. This fact

A history of the Aloha project

The iAPX 432 32-bit microprocessor has been in gestation for over six years, a third of that time in Santa Clara, Calif., and the remainder in Aloha, Ore. There its development eventually became known as the special systems operation, or SSO, with Jean-Claude Cornet as director. But its shroud of privacy led some to think SSO stood for "secret systems operation."

In the beginning the 432 was called the 8816, then the 8800. It had to be given a number because at Intel, "as soon as you give something a number, it is instantly perceived as this little thing with side-brazed connections coming out of it," jokes principal engineer Justin R. Rattner (see photo). By November of 1975 the endeavor had coalesced into a working unit under William W. Lattin. He remained 432 program manager until April of last year, when he moved over to another Intel division.

The original idea was to "do something interesting" with very large-scale integration, but with Schottky TTL performance. The team looked at and then discarded a double-diffused MOS process and a modified charge-coupled-device structure, before it finally came up with a short-channel technology that could squeeze 100,000 transistors onto a single chip yet still support future geometry reductions. It was the birth of the high-performance MOS, or H-MOS, process.

After some preliminary design work, the group presented prospective users with a specification. "They were responsible for our emphasis on multiprocessing," says Rattner. "It was the No. 1 thing they wanted." Back then, the notion of software objects as a way of simplifying programming barely existed. "But suggested mechanisms began to get very ad hoc," he adds. "Every new feature seemed to involve a different machine facility, a different hardware unit."

Early one Saturday morning Rattner woke up convinced software objects were the solution. "I wrote for about six hours and called George Cox [a staff scientist], and that Sunday morning we met at Intel to start working out the details," he recalls.

Then came the hardware design, which "made extensive use of regular logic cells and wiring topologies, very much along the lines of the work done at Cal Tech" by Carver Mead, who had begun consulting on the project in 1975. "We knew we couldn't just randomly wire 100,000 transistors," so computer-aided design and simulation tools had to be designed.

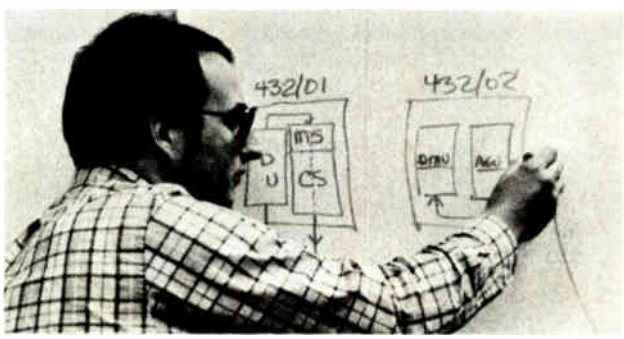
Portions of the chips' architecture were implemented directly in silicon—so intimately that they have no logic-gate equivalent. "We looked at each function, but instead of drawing a logic diagram and figuring out a gate implementation, we asked if there was a way to do it with MOS transistors directly," says Rattner. For the processor's control store, the team adapted a read-only memory cell designed for the 8087 numeric processor that stores 2 bits [*Electronics*, Oct. 9, 1980, p. 39]. Without tricks like the ROM cell, "the chips couldn't have been built."

Rattner feels the modular design methodology was "a spectacular success." At least one of the chips, the complex execution unit, "could have been shipped in sample quantities the first day out of fab," he says, adding that all in all, "productivity was five, six, seven times that of some other Intel projects."

The SSO now employs over 100 engineers designing follow-on board computers and design aids for the 432 family. Many of them have worked with minicomputer or larger machines in the past, as also has marketing manager Dave Best.

The project "cost a bundle," says Best, adding that "it was the largest investment in a single program that Intel has ever made—larger even than the magnetic stuff," the bubble memories.

-John G. Posa



is the basis of the 432's need-to-know protection system: in order to refer to an object, a program must contain an access descriptor for it; a program may only access an object according to privilege rights encoded in the access descriptor it holds.

Access descriptors are found only in a special type of segment called an access segment. This protects the integrity of access descriptors by preventing them from being treated as ordinary data. Only certain instructions are permitted to move or manipulate access descriptors.

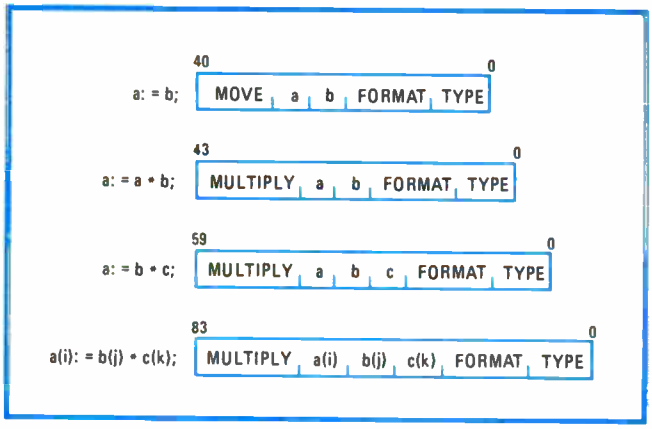
Selective entry

An access descriptor selects one of the 2^{24} entries in the object table, and each entry can specify a single-segment object of up to 2^{16} bytes. That gives a system-wide logical address space of 2^{40}—1 trillion—bytes of information. At any instant, however, the logical addressing environment of a program is restricted to 2^{16} objects of up to 2^{16} bytes, or 4 gigabytes. The instantaneous addressing environment is represented by four access segments, each of which is limited to 2^{14} access descriptors.

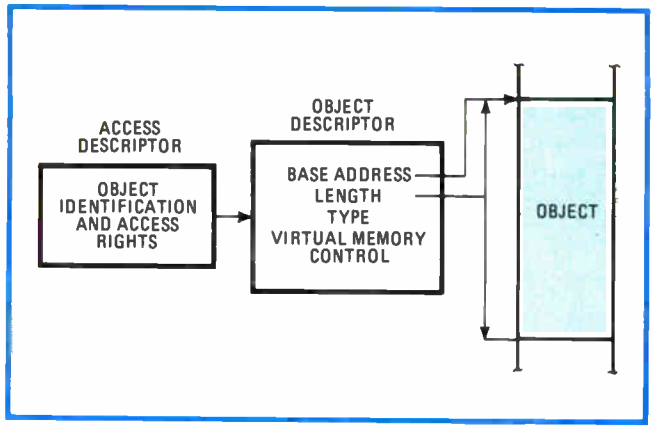
To implement the 432's two-level addressing architecture efficiently, each processor contains a buffer or cache of the most recently used object addresses. Cache data made stale by a software alteration of an object descriptor (which is a relatively infrequent occurrence) can be flushed by the operating system through interprocessor communication.

The key computing resources of the 432, unlike conventional systems, are controlled by hardware-defined system objects rather than by user-supplied software. This difference dramatically changes the way resources are managed by, and ultimately the structure of, the entire system.

For each type of system object, the hardware automatically handles some part of the operations that can be carried out on an object. Some of the operations are



8. Variable-size instructions. Since users are not expected to program the 432 in assembly language, its instructions are not aligned on convenient byte boundaries but instead can be any length of bits. The statements illustrated compile to single 432 instructions.



9. Address calculations. All memory requests are calculated via a two-level operation in which an access descriptor points to an object descriptor and the object descriptor in turn indicates the location and size of the desired memory contents (called an object).

available as instructions, while others are involved only when the hardware determines, independently of any particular instruction, that the operation is needed, such as fetching an absent memory segment. Software is responsible for providing the remainder of the operations defining the complete interface to the object.

This organization presents an important hardware-software tradeoff, involving just which operations should be put into hardware and which would be better left to software. In the 432, the decision to put an operation in hardware is based on one of three factors. First, the timing of an operation may be critical, affecting overall system performance in a fundamental way. Second, an operation may be security-critical, affecting the integrity of the protection system and the isolation of important information. Third, its reliability may be critical, affecting the ability of the system to function correctly in delicate programming situations.

The software part of the object management function is still by no means trivial. Software is largely responsible for creating new objects and disposing of old ones.

Generally speaking, objects work to remove the traditional barriers between the operating system and the application environment. The packages that make up iMAX are tools with which the user may build an application. If the iMAX package for a particular service is not quite right, the user is free to replace it with a package of different design.

Ada: implementation language

Ada, the Department of Defense's new standard programming language, is an ideal systems implementation language for the 432. The goals established for Ada's design were very like those set for the 432 since the language's designers drew upon the same body of research. The ultimate goals of both Ada and the 432 are increased programmer productivity, increased software reliability, and low software life-cycle costs.

Ada is inspired by the Pascal language and has much in common with it. But it differs from Pascal, and moves far beyond the older high-level language, in its support for large-scale, modular software. While several attempts have been made to repair this deficiency in Pascal, none has been widely accepted or used. Ada makes these efforts obsolete.

Through its "package" construct, Ada provides a natural way to put together large programs based on object-oriented modularization. A package defines an object and the operations that can be done on it. Following the object-oriented view further, a package restricts access to an object as specified in a separate interface portion and thus succeeds in hiding the details of its implementation.

Ada turns out to be an ideal language for the 432 not only because they embody the same idea of modularization but because many Ada constructs map directly onto the hardware. For example, the Ada package construct is directly supported in the 432 architecture by the concept of a domain object and Ada subprogram activations become contexts in the 432 architecture.

In those cases where the hardware of the 432 goes beyond Ada's built-in constructs, Ada's definition allows for a special machine-access package. Any 432 instruction or feature can be accessed via this package, eliminating the need for a 432 assembler. Ada is thus the only language used to write the iMAX executive and programmers are not ordinarily expected to require machine access. Hence even systems programmers will use Ada, resorting to direct machine access only rarely.

Ada and the 432 architecture cooperate to provide complementary checks on a program's design. Ada checks data types and interfaces during compilation, and the 432 subsequently rechecks them at run time in order to catch errors missed or possibly caused by the compiler. The 432 architecture also provides those checks on interfaces and data types that in Ada can only be made during execution.

Finally, Ada is the basis of the 432's integrated programming system. This software development system is built around Ada to provide separate compilation of programs with fully checked interfaces as well as link-time checking of module version numbers. The latter capability ensures that old versions of programs will not sneak back into a system. A symbolic source-level debugger lets the application programmer debug programs in Ada rather than 432 machine language. □

Applying signature analysis to existing processor-based products

With the advent of an off-board source of stimuli for signature analysis, it is possible to retrofit this efficent test method without extensive redesign

by Robert Rhodes-Burke,* *Hewlett-Packard Co., Santa Clara, Calif.*

☐ The digital test technique known as signature analysis (SA) is now widely regarded as the best way to service digital, processor-based boards. Until recently, however, products had to be designed to meet the special requirements of SA. In particular, the digital test patterns needed to stimulate the board during SA had to be generated by an on-board processor working from a user-supplied program.

Consequently, the many processor-based products designed before the technique's introduction could not be tested by it unless they underwent expensive redesign. However, now that an inexpensive, general-purpose stimulus source—the model 5001 microprocessor exerciser—is available, existing products can be serviced with little or no modification using signature analysis.

The application of SA to the Memorex 1377 display terminal will demonstrate the ease with which the technique can be used on equipment not designed for it. Although the terminal has been in production for several years and was not originally designed for signature analysis, it is a good SA target. Large portions of its circuity can be accessed through its processor using the 5001, so that a reasonably thorough check of its operation can be performed.

Understanding the application of SA to the 1377 demands familiarity with both the technique (see "Signature analysis revisited," p. 128) and the tools of the process. A brief description of the 5001 exerciser, its capability, and general application therefore precedes an explanation of the 1377 retrofit.

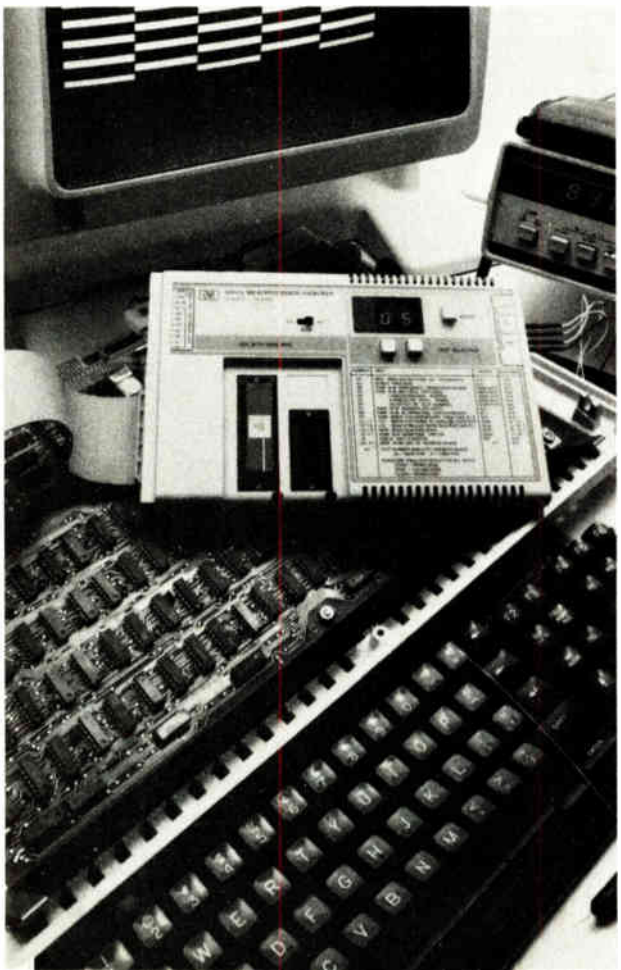
The model 5001 microprocessor exerciser, or Stimpod, as it is nicknamed, is a companion to the signature analyzer. It provides the digital stimuli to the board from which the analyzer takes bit streams for translation into hexadecimal signatures. Weighing only 3 pounds and measuring 9¼ by 5½ by 1 inch, the Stimpod is portable and travels easily into the field (Fig. 1).

Each Stimpod is designed for use with a particular type of microprocessor. The 6800 is supported at present, and the 8080, 8085, and Z80 will be supported in the coming year.

To employ the Stimpod, the processor on the board under test is removed and plugged into a zero-insertion-force connector on the front panel of the 5001. A ribbon cable from the Stimpod is then connected to the board socket that has been vacated by the processor.

The processor and board can then be exercised by the 5001. Contained in the Stimpod's internal memory are 52 test programs (see Table 1) applicable to a general class of microprocessor-based designs. For testing special aspects of a design, another ZIF socket is provided on the 5001's front panel. It accepts a 2716 erasable programmable read-only memory in which the user has placed a stimuli program. Thus the 5001 lets users apply signature analysis techniques without designing in or disturbing on-board program memory.

To use one of the internal test programs, a user sets the front-panel switch to



1. Retrofit in a box. Using signature analyzers to troubleshoot products not designed for use with them like the Memorex 1377 terminal is easy, thanks to the 5001 microprocessor exerciser (center). The checkerboard pattern (top) is produced by a 5001 program.

*The author is now with Apple Computer Corp., Cupertino, Calif.

INT and calls up the test by number, pressing the tens and units buttons below the light-emitting-diode display. Pressing the enter button then starts the test. Putting a preprogrammed PROM in the smaller front-panel socket and moving the double-throw switch to the external position permits custom tests to be called up and run in the same manner.

Since the 5001 was designed for use with a signature analyzer, it produces the start, stop, and clock signals needed by that unit to gate the bit stream and form a signature. These signals are provided at ports on the right of the exerciser, along with a common ground and a qualifier signal that is applicable in some of the preprogrammed tests.

On the left side of the Stimpod is an eight-bit output port, a qualifier input, and a power input and ground. Using the byte-wide port, the 5001 can stimulate the input side of input/output devices on the product being tested. The qualifier line can be used to recognize when a particular device is enabled, so that the 5001 can tell the signature analyzer to collect bits going to or coming from the device. The external power ports need only be used when the exerciser's power requirements—nominally 2.75 watts, exclusive of the processor—exceed the power available directly from the board under test.

Signature analysis could be applied to most of the 1377 by the 5001 and a 5004 signature analyzer alone. The general methodology of SA application involves deriving a set of signatures for a known good board, analyzing possible faults to determine how they change the signatures, and verifying that the set of signatures thus generated is valid and unique using other boards of the same type.

Although all this was done by hand for the 1377, it can now be almost completely automated with a automatic board tester that incorporates signature analysis. Such a board tester is available from Hewlett-Packard—the 3060A with option 100. In either case, once valid signatures are obtained, the board designer or test engineer can generate a fault tree—a listing or schematic that tells what points to check next if a fault signature is found. A field technician otherwise ignorant of SA can then use this tree to troubleshoot a system.

Applying signature analysis to many microcomputer-based products is often straightforward, using only the preprogrammed tests in the 5001. The 1377, however, is a special challenge to SA application because of some unusual aspects of its design. These can be understood by examining the functional layout of the terminal.

Choice target

The digital electronics used in the model 1377 display terminal are contained on a single, 9-by-16-in. multilayered printed-circuit board (Fig. 2). The board can be functionally segmented into five separate areas: the microcomputer, the display memory, the display-refresh algorithmic state machine (ASM), the communications ASM, and the clock and timing circuitry.

It should be noted that in normal operation three machines—the microcomputer, the communications

Signature analysis revisited

Signature analysis, a patented troubleshooting technique available under license from Hewlett-Packard Co., is based on the principle that a good digital circuit in a known (initialized) state will produce the same output when stimulated repeatedly by the same input. If the repeated output of a device is not the one it has been designed to produce, it has failed.

While this principle is simple and fairly obvious, signature analysis implementation is a bit more complex, relying on mathematics similar to that for cyclic redundancy coding. (For a thorough explanation of the signature formation process, see *Electronics*, March 3, 1977, p. 93.) But once signature analysis techniques have been applied to a design, using them to troubleshoot it is extremely simple.

All a technician has to do, either in production or in the field or depot, is follow the time-honored technique of signal tracing. He or she checks one test point and compares the measurement result to that in a table or schematic. If it does not match, the troubleshooter checks another point in accordance with the test plan.

The point between the last bad measurement and the next good one is the failure location. It should be noted that the technician does not need to know anything about signature analysis or, for that matter, digital logic. Thus, by requiring less from the troubleshooter, the technique can greatly reduce service costs.

In the past, a repetitive digital stimulus, or bit stream, was generated by the microprocessor of the product under test, which would execute a special test program residing in an on-board memory. A signature analyzer is used to check the response at the board's various test points, or nodes.

The analyzer works by monitoring the bit stream on one line for a specified period determined by the clock rate of the circuit under test. In this process it compresses the data and translates it into a four-character hexadecimal word, or signature.

A set of signatures, one for each test node in the circuit, must be generated; the designer or test engineer generally does this by exercising a known good unit—the prototype perhaps—with routines designed to exercise each area of the board. The good signatures are recorded; then the board is analyzed for the effect of failures on the bit stream. Once this is done, the test designer can create test procedures and test-point schematics for use by production-line and field technicians.

The three key conditions for the application of signature analysis are the ability to:

- ☐ Initialize circuits that can hold two or more different states (RAMs, flip-flops, and counters, for example).
- ☐ Synthesize the timing needed for signature sampling, both in terms of framing the sequence (sample start-sample stop) and clocking the bit stream.
- ☐ Apply the stimulus.

The first of these requirements is really a basic tenet of design for testability and can only be achieved by design. Designers who fail to observe it will be faced with a major testing problem. The other two conditions, however, need no longer be absolute design imperatives, thanks to the introduction of the 5001. **-Richard W. Comerford**

TABLE 1: MICROPROCESSOR EXERCISER TEST SET

Number	Test	Address range	Qualifier
00	Microprocessor: 6800 instruction set, interrupts	–	–
01	Buses: free-run	all	–
02	RAM: read/write 6800 direct addressing range	0000 – 00FF	–
03	RAM: read/write multiple patterns (checker-	0000 – 3FFF	–
04	board, inverse, address-as-data);	4000 – 7FFF	–
05	address range is selected according	8000 – BFFF	–
06	to test number	C000 – FFFF	–
07	RAM: read/write address as data	all	–
08	RAM: read/write alternating checkerboard	all	–
09	RAM: write checkerboard, then free-run	all	–
10/11	I/O: write patterns to qualified outputs	as qualified	0/1
12/13	I/O: read stimulus from qualified inputs	as qualified	0/1
14/15	ROM: read qualified data	as qualified	0/1
16/17	ROM: bus signature (pin X_0)	as qualified	0/1
18,19	5001: self-exercise	–	–
20 – 51	ROM: read 2-K address range	*	–

*Test number indicates 2-K address range, for example, 20 is 0000 to 07FF, 51 is F800 to FFFF

ASM, and the display refresh ASM—are jointly responsible for the terminal's workings. They operate concurrently in a complex, interleaved fashion, using various bus arbitration methods to share the data and address lines and access the shared display memory. The challenge, then, was to find a way of checking the functional areas independently, yet as they really performed.

Other aspects of the 1377's design were challenging, too. The use of two programmable interface adapters (PIAs) in the microcomputer section required a somewhat custom approach, since the designation of these devices' ports for input or output is determined and programmed to fit a specific application. In the 1377, the PIAs scan the terminal's keyboard and configuration switches, as well as drive its audio output (bell) and status indicator. Data from the PIAs can directly control some of the functions of the ASMs, such as selecting different segments of the display RAM or inhibiting the display or its reset. Therefore, it was essential to find a way to check the operation thoroughly.

The most elaborate part of the board is the timing and clock circuitry. Like other clock circuits, it generates timing waveforms independently of the microprocessor. On the 1377, it generates 11 phased clocks—more than usual—which are in turn used by the other functional blocks for timing generation. Despite this circuitry's complexity, SA checked it 100% with the least difficulty.

Of the other four functional blocks, the microcomputer also was 100% tested with SA. But the display memory block could be only 90% tested and the display-refresh ASM could be only 80% tested because of the communications ASM.

The communications ASM operates asynchronously with respect to the rest of the system, so that it could not be checked using the 5001 and the 5004 alone. However, a special test tool designed previously by Memorex had been used for some time to check this portion of the terminal. With some adaptation of such a tool (to be described later), even this asynchronous segment could be tested with signature analysis techniques.

The microcomputer section was (and in general is) the logical place to begin applying signature analysis. It is the area in which the 5001 exercises most direct control over the system operation. Further, the elements of the block are extremely common and hence can be easily checked out with the 5001's preprogrammed tests.

The 5001 was connected to the 1377 as described earlier, and the 5004's start, stop, and clock inputs were connected to the Stimpod. The 5004 was set to operate from the rising edge of the clock and start signals and the falling edge of the stop signal. For most of the tests performed, this was the only setup needed.

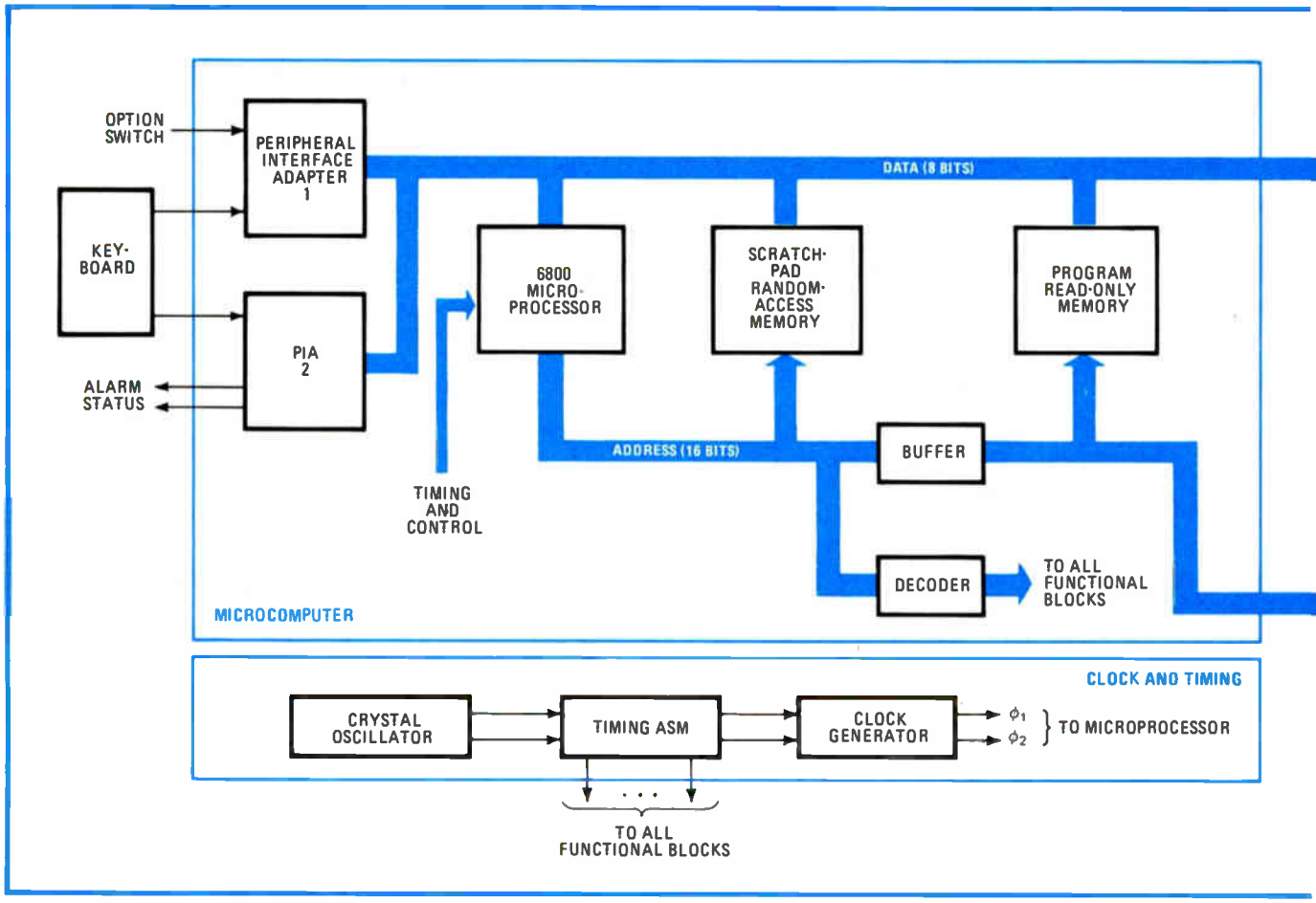
Test 00 (see Table 1) was the first performed. It checks the 6800's functionality by running it through its entire instruction set, except the wait-for-interrupt instruction, while it is isolated from the board. Other instructions in the test sequence serve to verify the interrupt line operation and the processor's ability to service interrupts.

Checking out the kernel

While the test is running, the functioning of the kernel—the processor, its clock and power—can be verified by taking a single signature. If the kernel is operating, holding the 5004's data probe to the processor's +5-volt supply produces a bit stream of 1s, which results in a signature of $28PH_{16}$. This provides an 80% confidence level that the processor is good.

To provide an even higher confidence level (95%), each pin of the 6800 can be probed while the test is run. This will result in the signatures shown in Fig. 3 and takes about 30 seconds to perform. Unless other tests indicate that the processor could be at fault, however, this check is not absolutely necessary.

Once the kernel's operation is verified, the next step is to check that the address lines and decoders are operational so that the Stimpod can access other circuits for test. Another preprogrammed test, 01, is used to do this



2. Shared facilities. In the 1377, the microprocessor, display refresh ASM, and the communications ASM share buses and the display memory. A major challenge is finding a way to independently analyze how these blocks work through the shared facilities.

check. In this free-run test, the CPU runs through its entire address repertoire, the analyzer's data probe is placed on each of the address lines, and a signature is obtained for each (Table 2). These signatures will be the same for any 6800 processor tested in this way.

Using the same test, signatures can be obtained at the outputs of the address decoders, but since their output is product-dependent, the signatures will vary from one design to another. After the ability of the processor, and thus the Stimpod, to access the various components of the system has been verified, they can be checked. The most logical area to investigate next is one closest to the processor, such as the memory in which the operating program is contained.

One-signature checking

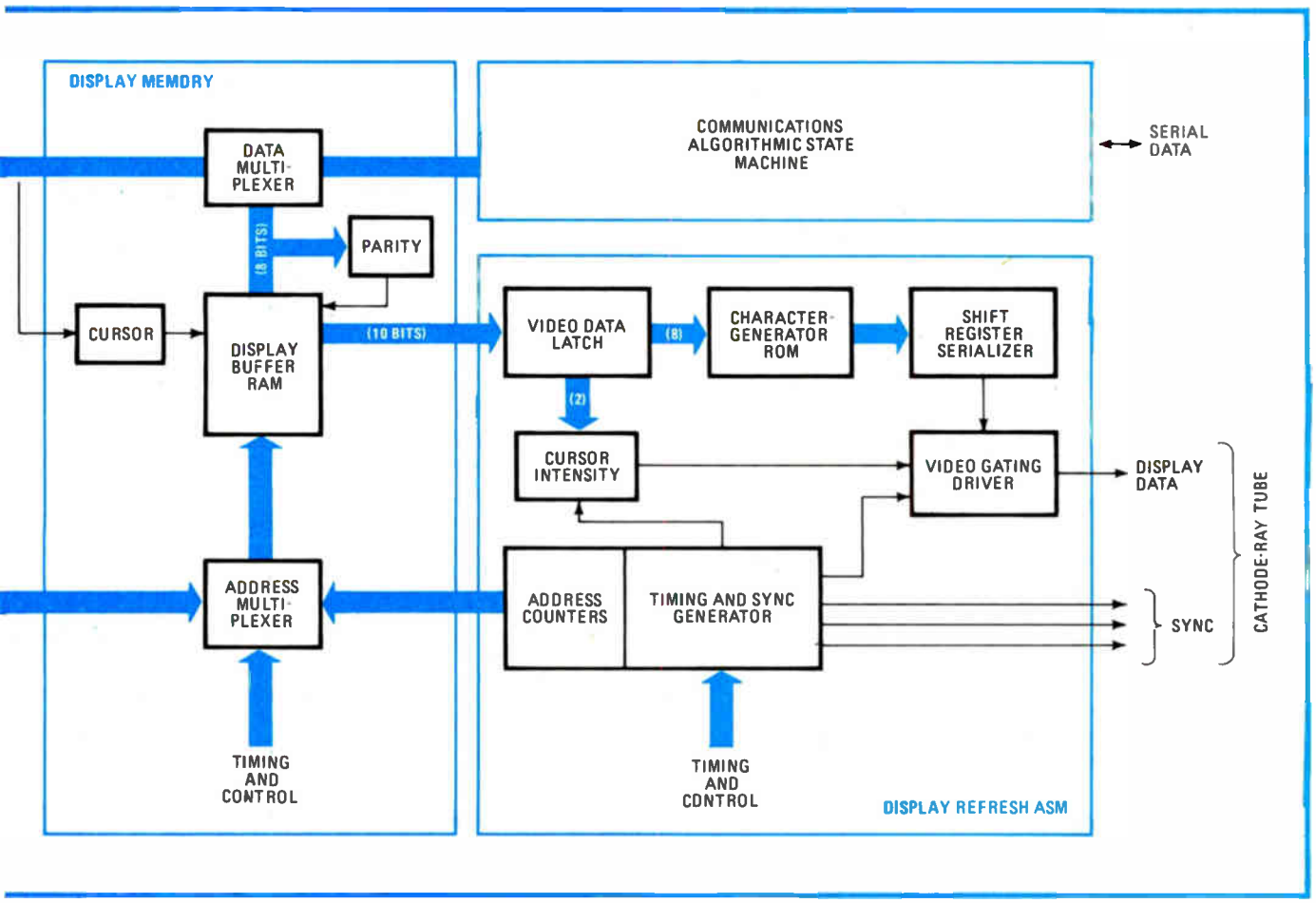
Depending on the product design, the program memory—read-only memory, or ROM—can be checked with a single signature or one signature for each memory device in it. This is done using either preprogrammed test 16 or 17, depending on whether the memory-enable line is active high or low, respectively.

In both tests, the entire contents of the enabled memory are read by the 5001 and formed into a single bit stream, which is output through port X_0 on the Stimpod's left side. By placing the data probe of the signature analyzer on this port, a signature that is unique to the content of the memory being tested can be taken.

Up to three ROMs contain the operating program in the 1377. To check each individually, the 5001's Q-in is tied to a chip-enable line and the contents of the chip are read by the Stimpod; test 16 does this since the 1377's chip-enable lines are active low. Were a block-enable line used in the design, the entire chip set could be checked with a single signature. Then, if an incorrect signature resulted, the contents of each chip could be checked individually.

The 128-byte scratchpad random-access memory was checked next, using test 02, read-write 6800 direct-addressing range. This test uses a sliding-1 pattern with a reverse background fill, which detects address interdependency. After the Stimpod writes the pattern, it reads it and the values written and read determine the clocking signal it supplies to the signature analyzer. Thus, by placing the signature analyzer on the +5-V supply line as in the microprocessor test, a signature is produced that reflects the number of good cells in the RAM. RAMs with less than 256 bytes can be checked using this test; other tests are provided for larger RAMs.

In the 1377, PIA_2 falls within the direct address range of the 6800. Thus, the PIA was partially exercised using test 02, when it was responding as though there were two extra scratchpad RAM cells when it was operating properly. If an incorrect signature appeared, the PIA-enable



line was grounded and the test rerun to see if the fault was actually in the RAM or the PIA.

With the completion of the scratchpad RAM test, the entire microcomputer block with the exception of the PIAs was completely checked. To test the PIAs, it was determined that a custom program would be needed. Rather than change the test setup and insert a custom programmable ROM, it was decided to save time and continue testing whatever could be checked with the preprogrammed tests and the present setup. The custom PIA test will be described later, along with a discussion of other custom tests.

The display memory, or display buffer RAM, in the 1377 is a 4,098-by-10-bit store composed of 10 1-K RAMs. This is divided into two pages, each consisting of 2,049 10-bit words. As the microprocessor can handle only bytewide data, two accesses (and therefore two addresses) are needed to obtain the data set; one address maps to the cursor portion of the stored data, while the other maps to the character portion.

Since the display memory address range is therefore large, two preprogrammed tests were first used to check its operation: test 03, which covers the address range from 0000_{16} to $3FFF_{16}$, and test 04, from 4000_{16} to $7FFF_{16}$. Before these tests were run, the display refresh was disabled by grounding a single pin, in order to prevent it from interfering with the 5001's control of the display RAM.

As shown in Table 1, these tests cause a number of different patterns to be read from and written to the RAM, thoroughly checking its operation. While the tests are run, the analyzer's data probe is set on each of the data-in and data-out pins of the two-port RAMs. The test resulted in only 20 signatures being generated for the entire display RAM.

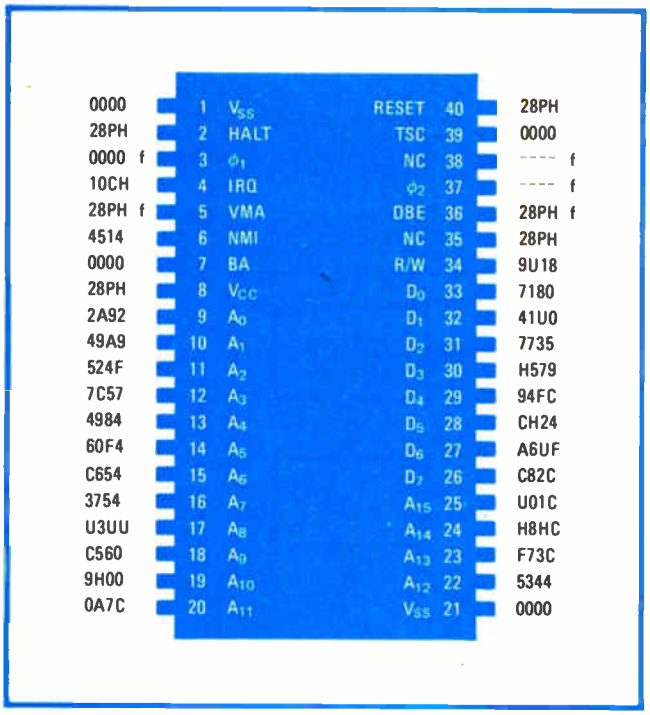
Though the preprogrammed routines were well suited to testing the display memory, it was subsequently found that a custom program needed to test the display refresh circuitry could also check display-memory operation, and was more effective in that it resulted in the need for even fewer signatures. This test will be described later, together with other custom programs.

Clock and timing

As previously noted, the clock and timing circuitry of the 1377 terminal is elaborate and takes up a considerable portion of the board's electronics. Even so, it was a relatively straightforward matter to derive a set of signatures for it.

Since the circuit is self-stimulating, it runs asynchronously and independently of the processor. For this reason, the start, stop, and clock inputs to the 5004 were moved from the Stimpod to the circuit itself; it was not necessary to reset the edges for these inputs.

Carrying out the tests at the clock rate of the circuit was very desirable; taking signatures in this way is simpler and the results are more easily interpreted. The 1377's clock rate is very high—greater than 17 mega-



3. 6800 pin signatures. Running the 5001's test 00 on a good 6800 yields the above set of signatures. A good signature at pin 2 is enough to indicate that the processor kernel is operational; other signatures can be taken if further testing indicates a problem.

hertz—but with option H02, the 5004 is able to test at rates up to 18 MHz. With HP's latest signature analyzer, the 5005 [*Electronics*, Nov. 20, 1980, p. 44], rates of up to 20 MHz can now be checked.

Before checking the circuit, two preprogrammed tests were run on the Stimpod. Test 09 was run first to fill the display RAM with a checkerboard pattern; this predictable pattern allowed some stable signatures to be taken in the area of the character generator. Before any signatures were taken, however, test 32 was run. This test tells the processor to read a 2-K address range that does not affect the shared buses and thus limits its activity to an area removed from the one to be checked. Thus, timing circuits outside the actual clock generator itself could also be investigated.

The 1377's clock and timing circuit is a long, chain-like circuit with a fair amount of feedback. It was therefore necessary to move outside the loop to verify correct inputs. Though it may be necessary to break a loop when extensive feedback exists, it is not absolutely required. When provision is made for resetting the counter chain, as it was in the 1377, it is often not necessary to break it, particularly if the loop contains only two or three elements. Isolating a fault to such a loop is then sufficient, permitting the faulty element to be easily found with the signature analyzer's built-in logic probe.

As noted previously, two areas of the board required some custom approaches to generating signatures: the PIAs and the display-refresh circuitry. Both tests involved programming a 2716 erasable PROM, but this was the only thing necessary for testing the display-refresh ASM.

TABLE 2: 6800 ADDRESS BUS SIGNATURES FOR TEST 01

Line	Signature	Line	Signature
A_0	UUUU	A_8	7791
A_1	FFFF	A_9	6321
A_2	8484	A_{10}	37C5
A_3	P763	A_{11}	6U28
A_4	1U5P	A_{12}	4FCA
A_5	0356	A_{13}	4868
A_6	U759	A_{14}	9UP1
A_7	6F9A	A_{15}	0002

For the PIA test, jumpers were needed to ensure complete exercise of the devices; that was not due to any deficiency in the test, but rather to the layout and partitioning of the design itself. Accessing several lines connected to the device required looping back to other lines in order to thoroughly stimulate the device, and this looping would have been required for other test techniques as well.

The custom program developed for the PIAs is of a general nature and could be used for other such devices. It is a 150-byte program and copies of it will be made available this year by Hewlett-Packard. The reason it is not included in the preprogrammed tests is that, though general, it requires that the user specify the address and the port functions (input or output) specific to his or her application. Given that information, the program is simple to adapt to a design.

Testing display-refresh

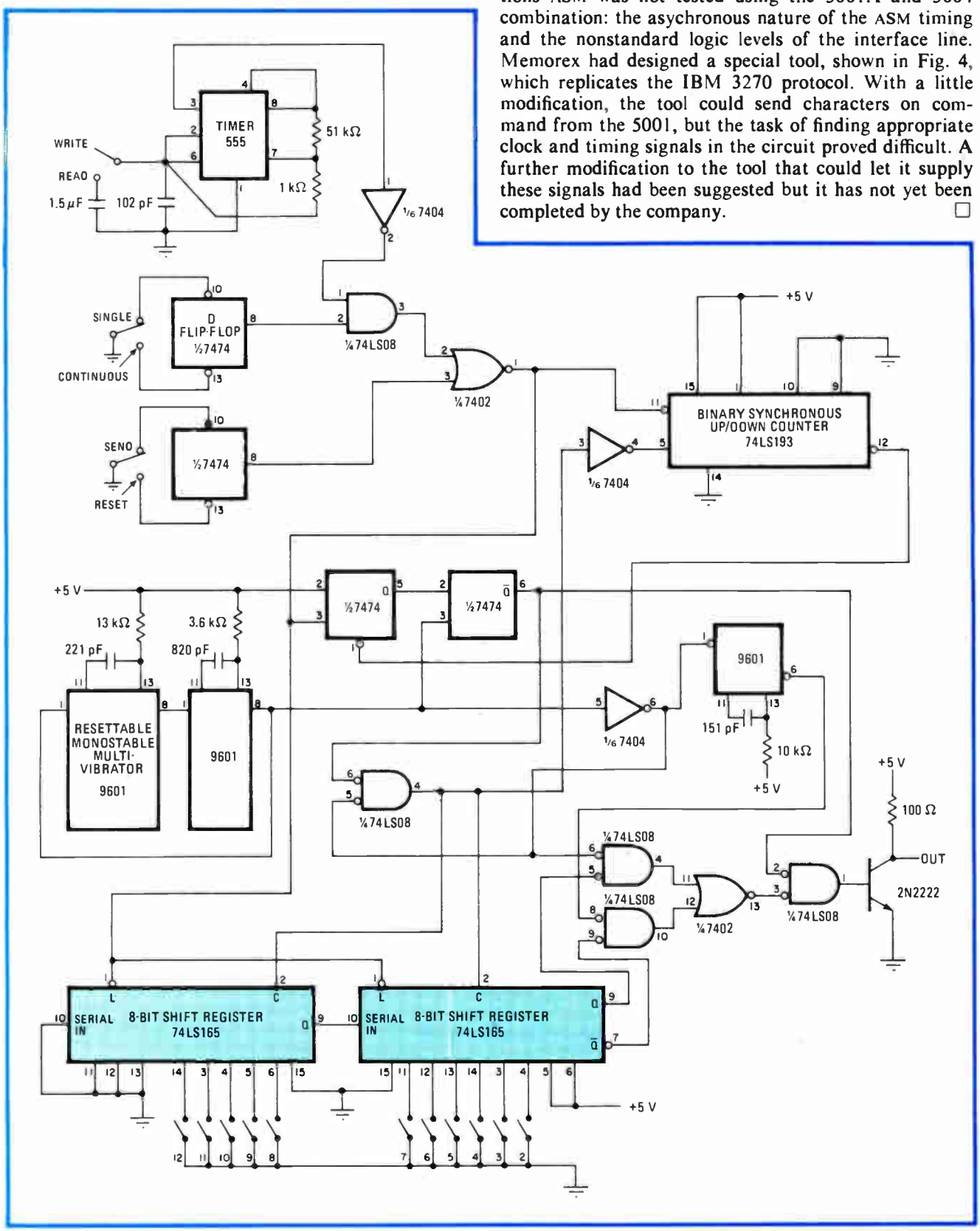
Two levels of display-refresh testing—functional and diagnostic—were provided for the 1377 with one custom program. This program initialized the display RAM with all possible display characters and some nondisplayed control sequences. It was, in effect, similar to the "quick brown fox . . ." type of test often used in data communications testing.

For both tests, the framing and clock signals input to the signature analyzer were taken from the display-refresh ASM, since it runs asynchronously with respect to the microprocessor. The clock signal for the functional test was taken from the dot-clock that controls the video gating drivers. Using this clock, the analyzer can verify that about 40% of the terminal's circuits are functional with only one signature, which is taken by placing the analyzer's data probe on the display-refresh ASM's video output. This quick and easy go/no-go test also provides a full CRT display.

It should be noted that with this custom program both the microcomputer and display-refresh ASM are running concurrently, just as they would in normal interleaved operation. For the diagnostic check of the display-refresh ASM, the signature analyzer's clock is moved to the character clock, which is synchronous with direct memory accesses performed by that ASM. Thus, by using this clock to check activity on the system buses, signatures are generated only when the display-refresh is using them—the interleaved operation is separated for testing.

Both the functional and diagnostic approaches used in

4. Serial stimuli. For checking out the serial interface (the communications ASM) of the 1377, Memorex has been using the in-house tester, which simulates IBM 3270 protocol. Setting toggle switches causes two 8-bit registers (shaded) to create a test word.



the 1377 could easily be applied to other products. They may, in fact, prove invaluable in testing the increasing number of processor-based CRT products.

There were basically two reasons why the communications ASM was not tested using the 5001A and 5004 combination: the asychronous nature of the ASM timing and the nonstandard logic levels of the interface line. Memorex had designed a special tool, shown in Fig. 4, which replicates the IBM 3270 protocol. With a little modification, the tool could send characters on command from the 5001, but the task of finding appropriate clock and timing signals in the circuit proved difficult. A further modification to the tool that could let it supply these signals had been suggested but it has not yet been completed by the company. □

Reed-coil relay is behind flexible fault detection

by Daniel Appiolaza
Mendoza, Argentina

Mechanically providing such functions as undercurrent and overcurrent protection for power supplies and fault indication for an automobile's turn signals or stoplights is easier to achieve inexpensively with relays having a separate reed and coil. Using the coil as a remote current-sensing device also makes the relay flexible enough to do a myriad of other jobs not possible with self-contained units.

Consider the example of current-overload monitoring (a). Here, the normally open reed switch serves to activate the shunt formed by the light-emitting diode, resistor R_1, and the zener diode when excessive supply current flows.

The coil, made from four turns of No. 12 gauge wire, is tightly wound over the reed so that an instantaneous line current equal to or larger than approximately 5 amperes dc will close the reed relay and trigger zener diode D_1. Thus the reference voltage will drop to zero until the line current is reduced and the reset switch is depressed.

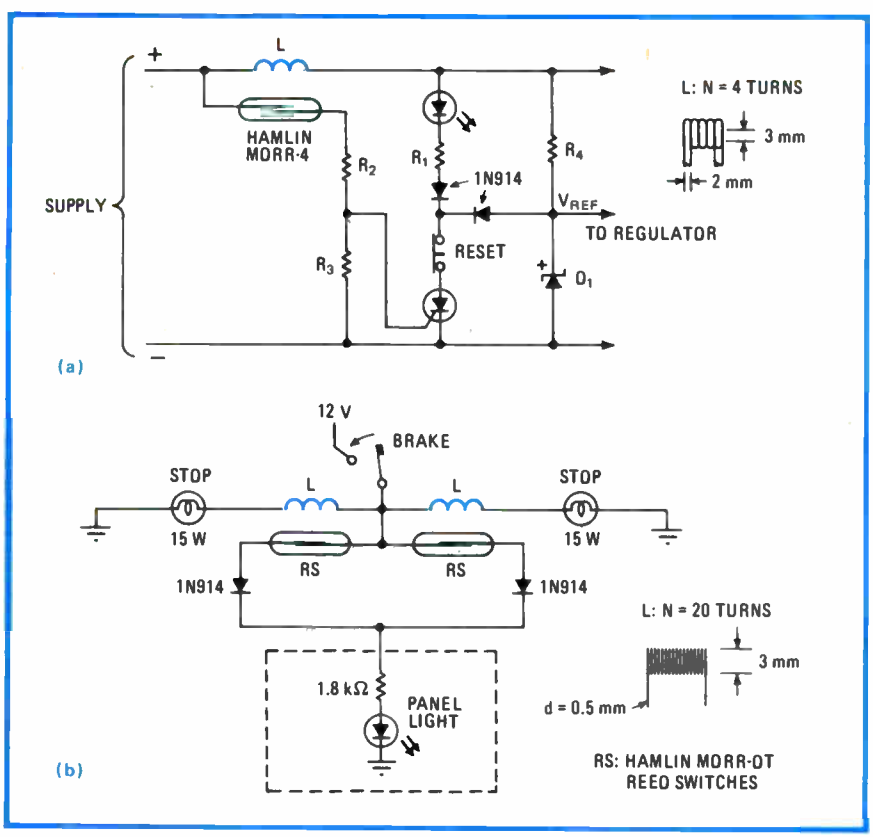
A second example is the fault detector of an automobile's brake signals (b), where it is important to know when a stop or turn lamp has failed (a feature not supplied by auto makers). Here, two reed/coil assemblies are required, with the reed contacts being normally closed.

If for any reason either of the stoplights does not turn on when the brake is applied, no current can flow through either coil. Consequently, the reed switches will not open and the panel LED will indicate trouble with the signalling system.

With normally closed relay contacts, however, the stoplights may still turn on despite a failure in the reed circuit or even the LED/resistor itself. Alternatively, it might be better if the reeds are of the normally open type. Then the circuit can be wired to switch on the panel LED only when the car's stoplights become active.

This latter arrangement will positively indicate a failure in the system. If the LED does not turn on when the brake is applied in the normally open reed system, however, it does indicate difficulty with either the lamp or the monitor circuit. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $75 for each item published.



Switching separates. Two-element relay having remote four-turn current-sensing coil and normally open reed switch (a) provides inexpensive overcurrent protection for power supply. When implemented in car's brake-signal system, relay detects faulty turn or stoplights. A normally open relay circuit might be preferable to the normally closed configuration shown.

Four-chip meter measures capacitance to within 1%

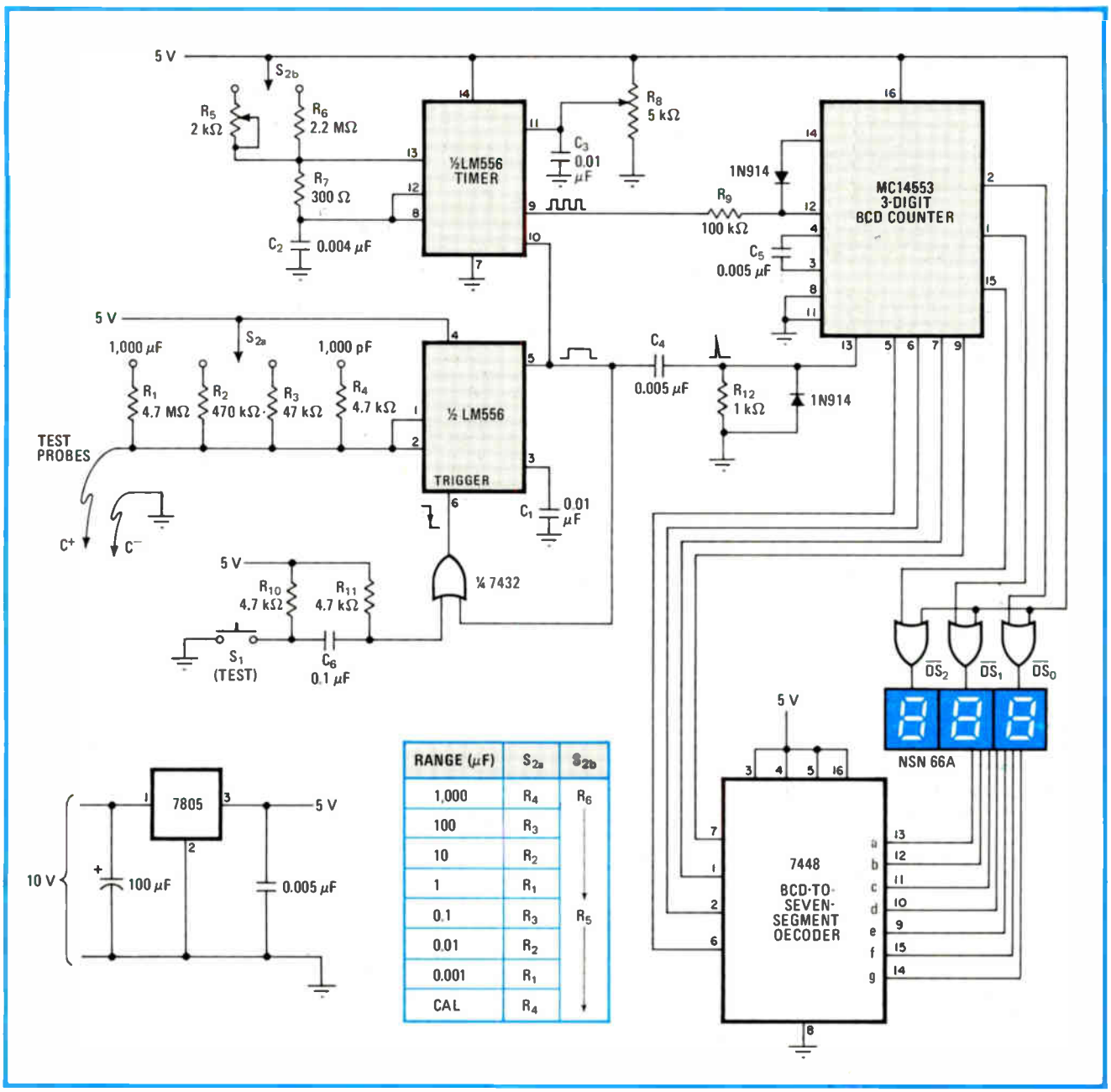
by Peter Henry
Seattle, Wash.

Measuring capacitance over the range of 1,000 picofarads to 1,000 microfarads, this four-chip meter has an overall accuracy of 1%. Costing less than $20, the unit has a digital readout and is built from parts that are readily available.

Engaging switch S_1 momentarily fires timer A_1, whose pulse width is determined by capacitor C_1 and one of four timing resistors, R_1 through R_4. The timer enables an astable multivibrator, A_2, and resets a three-digit decimal counter, which then counts the number of pulses from A_2 until the timer runs out or a count of 999 (overflow) is reached. The number is then displayed.

A seven-decade range (see table) is achieved by switching in R_1–R_4, and R_5–R_6, which sets the frequency of A_2 to approximately 1 or 1,000 hertz. For best performance, R_1–R_4 should be hand-picked to achieve the desired 1:10, 1:100 or 1:1,000 ratios if an accuracy to within 1% is required.

Calibration is achieved with a known capacitance of



RANGE (μF)	S_{2a}	S_{2b}
1,000	R_4	R_6
100	R_3	
10	R_2	
1	R_1	
0.1	R_3	R_5
0.01	R_2	
0.001	R_1	
CAL	R_4	

Charge check. This digital capacitance meter measures accurately over the range of 1,000 picofarads to 1,000 microfarads. The circuit displays the number of pulses from astable multivibrator A_2 in the measurement count period during which 555 timer A_1 is active. The measurements are repeatable to within a few counts on all but the lowest scale, giving an overall accuracy to within 1%.

Wavetek Model 189 sells for $695.* Yet it has digital storage of sweep settings just like the expensive instruments.

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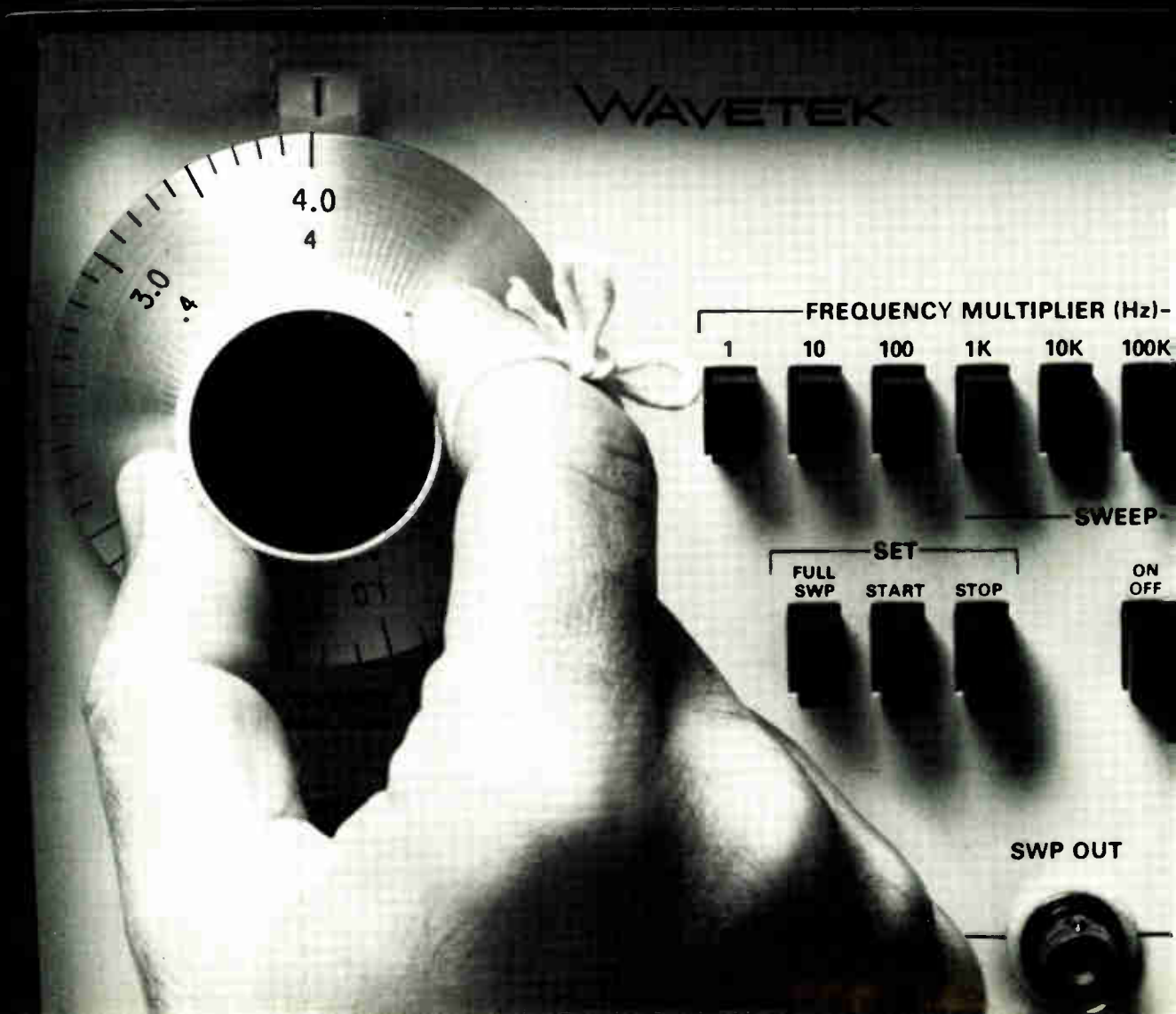


approximately 0.3 μF. Potentiometer R_5 is adjusted for identical readings on the calibrating and 1-μF scale. Then potentiometer R_8 is adjusted for the same readings on both scales. This procedure is repeated as often as necessary for perfect agreement.

The circuit is very reliable and will yield repeatable measurements to within a few counts on all but the lowest scale. Differences in capacitance of 10 pF can be detected. Leaky capacitors may be difficult to measure because of their series resistance. □

Stabilizer boosts current of ±dc-dc converter

by Gerald Girolami, *Université Pierre et Marie Curie, Physique et Dynamique de l'Atmosphère, Paris, France*

The power-handling capacity of Intersil's popular positive-to-negative voltage converter can be increased by a factor of 10 with this circuit. Using an efficient, low-cost stabilizer to hold output voltage constant for an operating current generally above that which the ICL7660 is normally used, the circuit is a viable alternative to using an expensive modular dc-dc converter when a 0-to-10-volt, 0-to-100-milliampere source is required.

Although the ICL7660 is used almost exclusively in low-power applications, its maximum load current is in excess of 50 mA for a 5-V, 100-mA input. At this level, however, the output voltage drops from the expected −5-V value to near zero. By using the LM301 operational amplifiers (A_1 and A_2) in a feedback loop, however, the output voltage, V_{out}, can be made to equal the negative of the given reference voltage, $-V_{ref}$, at the desired output current.

As seen, the output voltage, V_{out}, is compared with V_{ref} at op amp A_1. As a consequence of the circuit configuration:

$$V_1 = V_{ref}\left[1+\frac{R_4}{R_3 \| R_5}\right]\left[\frac{R_2}{R_1+R_2}\right]-\frac{V_{ref}R_4}{R_3}-\frac{V_{out}R_4}{R_5}$$

where $R_3 \| R_5 = R_4$, $R_1 = R_2$, and $R_3 = 2R_4$. Thus $V_1 = \frac{1}{2}(V_{ref} - V_{out})$. Similarly, op amp A_2 generates a voltage:

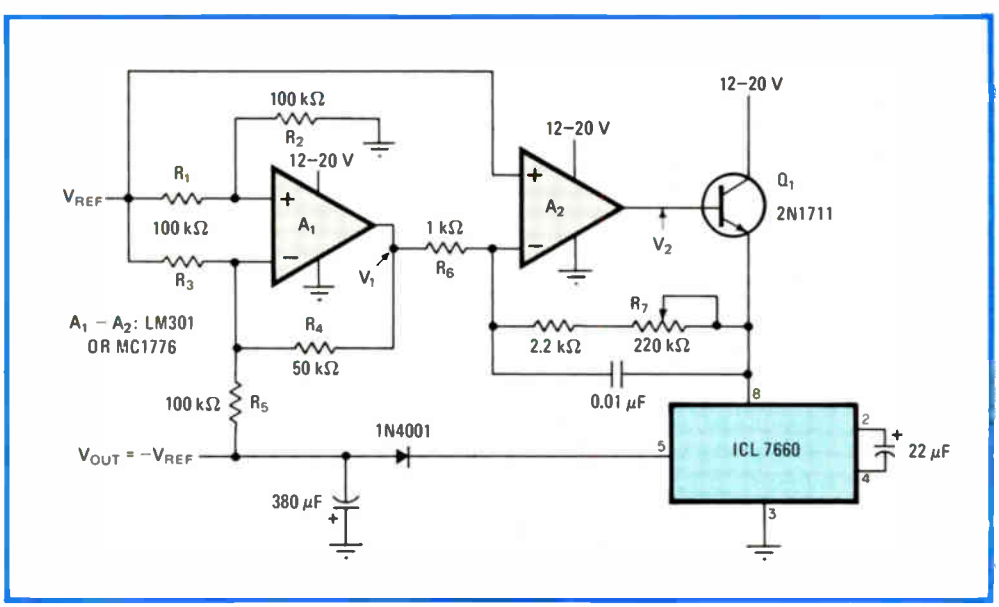
$$V_2 = V_{ref}[1+(R_7/R_6)] - V_1 R_7/R_6$$

where $R_6 = R_7$, and so $V_2 = 2V_{ref} - V_1$. Combining the final expressions of V_1 and V_2 yields $V_2 = 3/2\ V_{ref} + \frac{1}{2} V_{out}$.

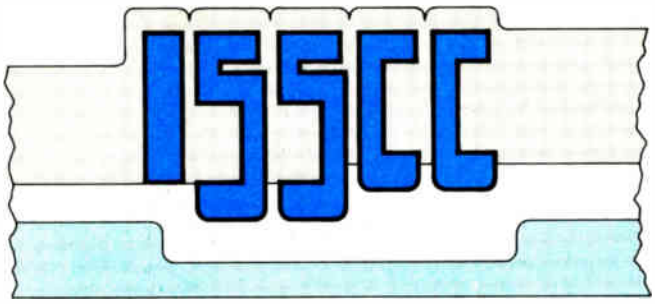
Thus, an increase in V_{out} will cause V_2 to increase. Because $V_2 = -V_{out}$, as specified under normal conditions for the ICL7660, an increase in V_2 will cause V_{out} ultimately to decrease, and vice versa, and negative feedback is achieved. Thus, under conditions for stabilization, $V_2 = -V_{out} = 3/2\ V_{ref} + \frac{1}{2}\ V_{out}$, or $V_{out} = -V_{ref}$, and only V_{ref} will have any effect on V_{out}, with the required driving and load currents provided by A_1 and A_2 and power transistor Q_1.

In practical applications, the output voltage is adjustable from −2 V to −10 V for a positive V_{ref} of similar range. The maximum output current is 100 mA at $V_{out} = -5$ V and drops thereafter. But it is possible to use two such circuits and two diodes to double the output current. That may not seem too interesting because many good dc-dc converters that deliver high current are available, but note that this circuit allows selection of the output voltage, a feature not usually found in commercial units. The regulation is good and the mean output voltage variation will be only 70 millivolts at I_{load} = 100 mA. This specification is adequate for digital circuits that can withstand a ±5% variation (that is, 250 mV) at the 5-V level.

Note that the MC1776CG is suitable for use as A_1 and A_2. It is necessary to add an 8.2-megohm resistor between pins 4 and 8 of each device, however, to set the operating current in the amplifier. □



Steady power. Negative feedback provided by A_1 and A_2 stabilize output voltage of ICL7106 converter for medium-range currents giving user a 2-to-10-V negative voltage source capable of delivering 100 mA. Reference voltage controls output such that $V_{ref} = -V_{out}$. Output voltage regulation is only 70 mV at 5 V.



The main events: VLSI processors, fast static RAMs, precise linear ICs

Chips with upwards of 10,000 transistors are becoming commonplace. So are 32-bit microprocessors, sub-20-nanosecond complementary-MOS memories, extremely accurate monolithic filters, and chips that can withstand hundreds of volts. As the 28th annual International Solid State Circuits Conference, held last week in New York, proves, all that is possible—and more.

With very large-scale integration in hand, Intel, Bell Laboratories, National Semiconductor, and Hewlett-Packard have sculpted 32-bit microprocessors out of silicon. All bear the VLSI look: regularity through programmable logic arrays and microcode. They appear as intelligent memories, which, indeed, they are.

Speaking of memories, the word this year is static. Whereas last year's conference highlighted ultra-LSI dynamic memories, this year's stars are superfast C-MOS and n-channel static random-access memories.

In telecommunications circuits, where the marriage of codec and filter has been an obvious one for some time, C-MOS seems to be the technology of choice as well. Active filters in general are being designed with frequency and bandwidth electrically adjustable to within cycles.

Advanced integrated-injection-logic processes have made possible a 14-bit digital-to-analog converter that needs no on-chip trimming, a 16-bit analog-to-digital converter that shares its die with emitter-coupled logic, and a 14-bit C-MOS a-d converter that pulls trimming values from an on-chip memory. These techniques, plus a host of high-voltage processes, are expanding the role of electronics in consumer, industrial, and other areas.

32-bit microprocessors inherit mainframe features

by R. Colin Johnson
Microsystems & Software Editor

It seems that the era of 32-bit very large-scale integrated microprocessors is here, given the appearance of no fewer than four such devices at this year's ISSCC. Most have been rumored for years, as would be expected for projects hundreds of man-years in the making.

One of these is the three-chip iAPX 432 from Intel Corp.'s Aloha, Ore., Special Systems Operation division. It has been coming for quite some time [*Electronics*, May 22, 1980, p. 39] and has finally arrived with more features and subtleties of architecture than might have been imagined (see p. 119).

Two of the other 32-bit offerings may come as more of a surprise; one, a single-chip microprocessor from Bell Laboratories, is loaded with such unusual attributes as separate fetch and execution units and a 32-megahertz clock; the other is from Hewlett-Packard, which has become increasingly involved in the making of such custom chips in the last few years. Finally, National Semiconductor revealed more details of its upcoming NS16000 family of 32-bit components, including both the memory management unit and the central processing unit itself.

Several new 16-bit offerings have arrived as well, including a fast complementary-MOS processor from Toshiba and a single-chip implementation of Digital Equipment Corp.'s PDP-11/34 minicomputer. Also, several unique parts were discussed, like an 8-bit microprocessor with on-chip nonvolatile memory from Hitachi, a biomedical microprocessor with analog input/output from Intersil, a single-chip graphics display controller from Nippon Electric, and a self-testing microprocessor from West Germany's Institut für Theoretische Elektrotechnik.

Bell Labs does it again

The single-chip 32-bit C-MOS microprocessor developed by Bell Labs in Murray Hill, N. J., is known as the Mac-32. A register-based machine with a 17-by-32-bit file, its architecture is clearly the result of serious forethought. The chip has two independent subunits, one optimized for fetching instructions, the other for executing them (Fig. 1)—which is an increasingly popular method used on both the 8086 and Texas Instruments' forthcoming 99000 (see p. 157). The fetch unit in the Mac-32 has an instruction queue for storing upcoming instructions, as well as a special-purpose arithmetic address unit to do its own address calculations. The execution unit features a barrel shifter that requires only a single machine cycle to shift from 1 to 32 bits. The arithmetic and logic unit for the execution section uses

an extremely low-power dynamic C-MOS technology that the labs calls "domino" cells. The part is also fast, executing a 32-bit addition in just 60 nanoseconds.

The instruction set, like that of the Motorola 68000, is extremely orthogonal, allowing all of the microprocessor's rich set of data types to be used with any instruction. Included are bit-manipulation instructions that work not only on single bits but on fields and blocks of bits as well. The part also has instructions to push and pop data in multiple registers to and from the stack for easy context switching, plus extensive exception-handling facilities and a hierarchy of four privilege levels similar to National's 16000 that serve to isolate system and user software.

The Mac-32 is cast in Bell Labs' exclusive "twin tub" C-MOS technology [*Electronics*, Nov. 20, 1980, p. 136]. The huge chip comprises more than 100,000 transistors laid out according to 3.5-micrometer design rules—a process that took only three months to accomplish with computer-aided design. Extensive use has been made of programmable logic arrays, and the registers, barrel shifter, and instruction queue all are formed from gate arrays. The part will be shrunk to 119,350 square mils (77 square millimeters) when 2.5-μm rules are employed, and it operates off a 32-MHz clock that derives from two phase-shifted 8-MHz external clock sources. The Mac-32 will be used internally in equipment made by Western Electric Co.

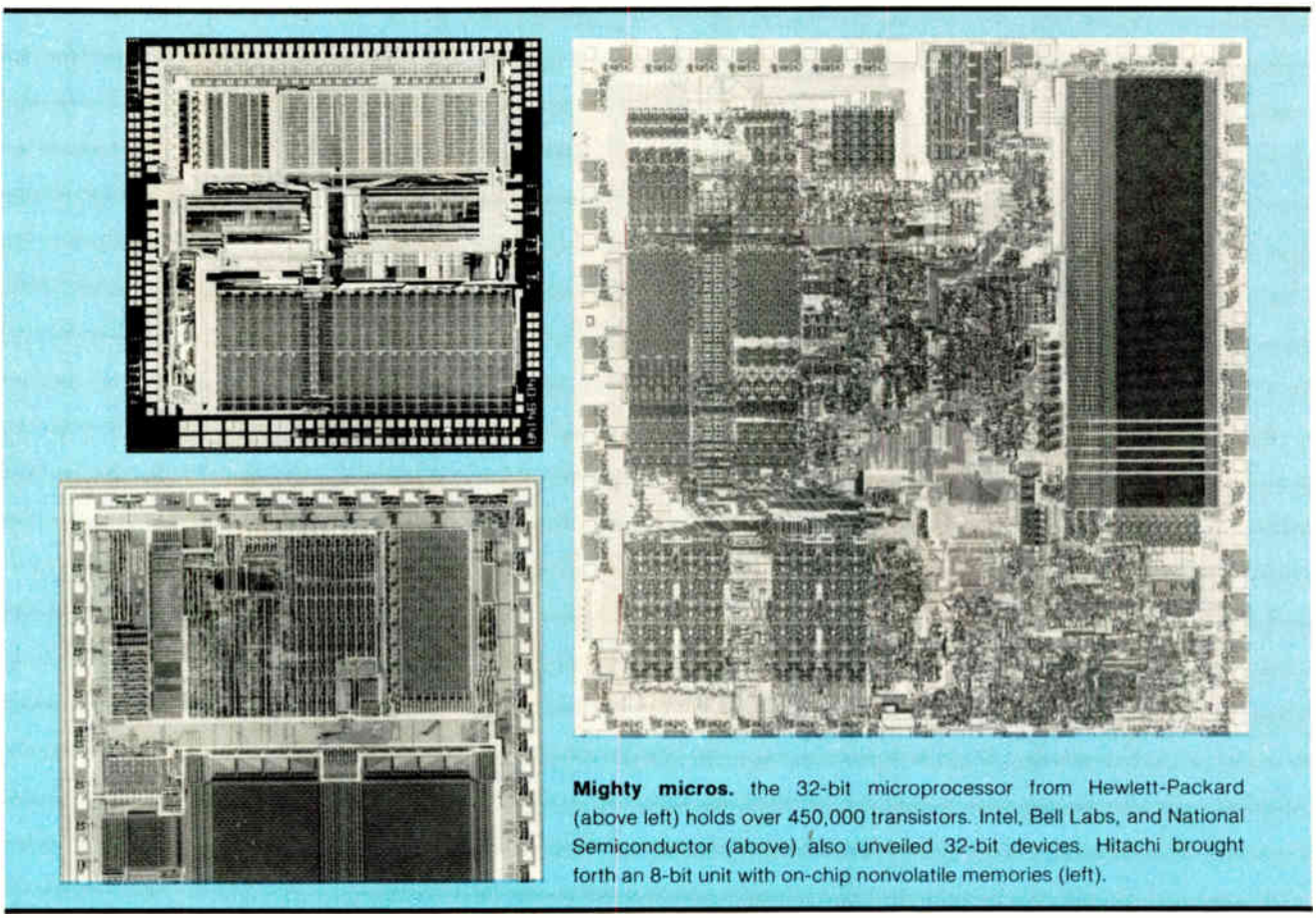
The most highly integrated logic chip ever produced is the new 32-bit microprocessor from Hewlett-Packard Co. in Fort Collins, Colo. [*Electronics*, Feb. 10, 1981, p. 39]. This n-channel MOS device has over 450,000 devices incorporated into a high-resistance substrate. An eight-mask, silicon-gate part that uses 1.5-μm ($\pm$0.25-μm) lines and 1-μm ($\pm$0.35-μm) spaces, it achieves its density partially through the use of electron-beam lithography.

Special hardware

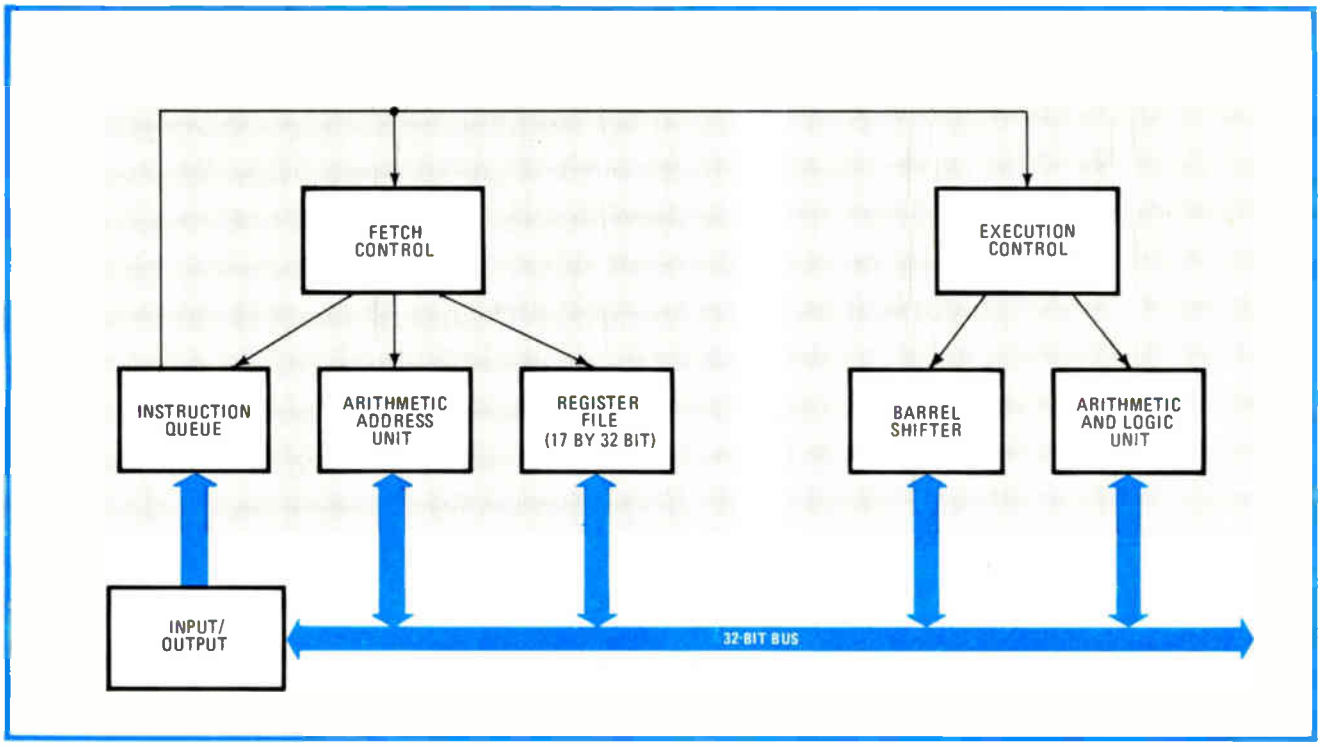
The microprocessor has a register-based architecture that incorporates a 28-by-32-bit file on chip. It also contains several other special-purpose hardware units, including an N-bit shifter (called a barrel shifter on the Mac-32 and the iAPX-432) and a hardware multiplier that yields a 64-bit result from two 32-bit operands in a fast, 1.8 microseconds. It also provides 64-bit floating-point multiplications, conforming to the standard set by the Institute of Electrical and Electronics Engineers, in only 10.4 μs—a feature that is highly desirable but seldom found as directly executable instructions.

Many other unusual features are included as well, like four separate stack pointers and a three-level pipelined instruction sequence that overlaps the fetching, decoding, and execution portions of three instructions simultaneously. This sequence results in a basic-instruction throughput equal to the part's clock period of 55 ns derived from its 18-MHz clock.

Like practically all contemporary microprocessors of 16 bits or more (excepting, perhaps, Zilog's Z8000), HP's part is fully microprogrammed. Its 9,000-by-38-bit



Mighty micros. the 32-bit microprocessor from Hewlett-Packard (above left) holds over 450,000 transistors. Intel, Bell Labs, and National Semiconductor (above) also unveiled 32-bit devices. Hitachi brought forth an 8-bit unit with on-chip nonvolatile memories (left).



1. Pipelined. Separate fetch and execution units allow those two operations to be overlapped in Bell Labs' Mac-32. The fetch unit has its own address calculation hardware to offload that chore from the execution unit, which features a barrel shifter.

control store works in conjunction with a programmable logic array that performs the actual instruction decoding. Besides the definition of the basic instruction set, the microcode also includes special debugging code for operations like breakpointing, single stepping, and tracing instruction execution.

A feature that will probably be mandatory on all VLSI chips is self-testing. When power is turned on and before the microprocessor fetches its first instruction from main memory, it runs the self-testing routines that are kept in microstore, thereby ensuring the user that if it comes up at all it is working properly.

The Institut für Theoretische Elektrotechnik in Aachen, West Germany, is one of those experimenting with self-testing procedures for microprocessors. To that end, it has built a self-testing device that consists of a microprogram counter, a microinstruction register and the actual microprogram read-only memory itself (Fig. 2). The researchers estimate that about 15% of a chip's area is required for self-testing hardware to build a fully self-testing microprocessor.

New family

A processor family that features 32-bit internal data paths and a 16-bit memory interface (a technique also used in Motorola's 68000) is the NS16000 from National Semiconductor Corp., Santa Clara, Calif. The microprocessor itself, the 16032, can be married to the memory management unit, the 16082, to form a true virtual-memory microprocessor system [*Electronics*, April 24, 1980, p. 123].

Like HP's part, the 16032 has separate fetch and execution units, but in addition it pipelines the execution in three stages: instruction loading, decoding, and finally execution itself. The pipelining technique will likely show up in many future microprocessors as designers attempt to squeeze more throughput out of register-based von Neumann architectures.

The device is also fully microcoded and like the HP part includes self-testing routines (127 bytes) in its total microcode space of 1,300 by 18 bits. The microprogram unit cycles in 100 ns.

The 16032 is an n-MOS device incorporating over 60,000 transistors onto a 290-mil-square (8.4-mm-square) chip that is housed in a 48-pin package.

16-bit arena

Sixteen-bit microprocessors have carved out a significant share of the total market of late, making it likely that even more manufacturers will be competing shortly. Two new 16-bit parts were discussed at the conference.

One, the result of a collaboration between Digital Equipment Corp. in Hudson, Mass., and Integrated Circuit Systems in nearby Worcester, is a single-chip implementation of DEC's PDP-11/34 minicomputer. This 38,750-mil² (25-mm²) n-MOS chip has been highly optimized, so that only 13,000 transistors are required to realize a microprocessor with a minicomputer's instruction set. It uses programmable logic arrays containing 50% fewer gates than the TTL version of the PDP-11/34. The chip can add a register to any memory location in 2.4 μs at the 7.5-MHz clock rate and dissipates 0.8 watt.

From the East

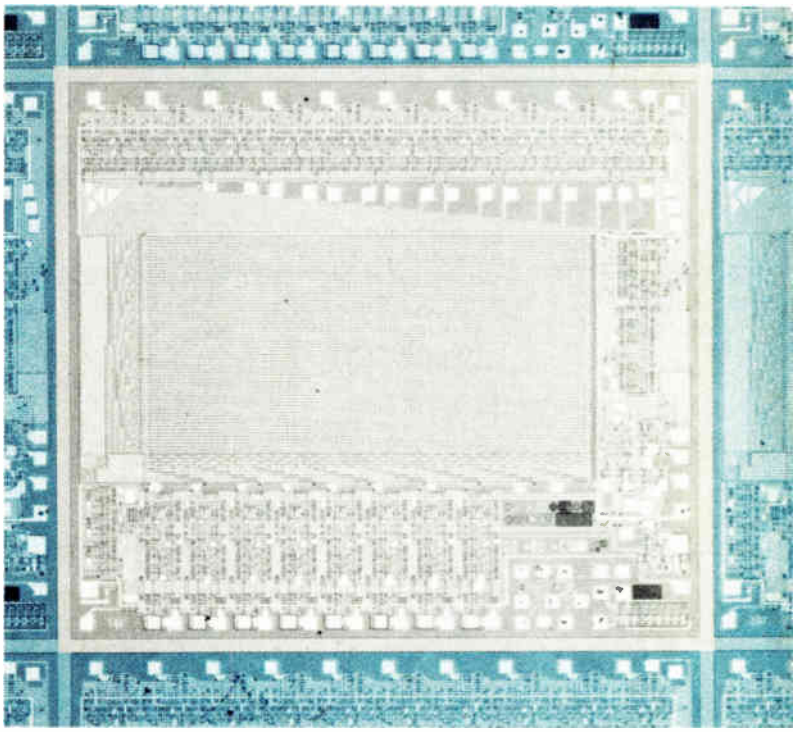
Toshiba Corp.'s proprietary 16-bit C-MOS microprocessor is fabricated on a sapphire substrate that speeds the part along to a 300-ns microcycle [*Electronics*, Oct. 9, 1980, p. 75]. It, too, uses a parallel-pipelined architec-

ture, a barrel shifter, multiplication hardware, and an instruction prefetching queue. It also has a full range of floating-point instructions. All this capability fits on a 264-by-295-mil (6.7-by-7.5-mm) die that houses 12,000 gates and is powered by a single +5-volt supply. It comes in a 64-pin dual in-line package.

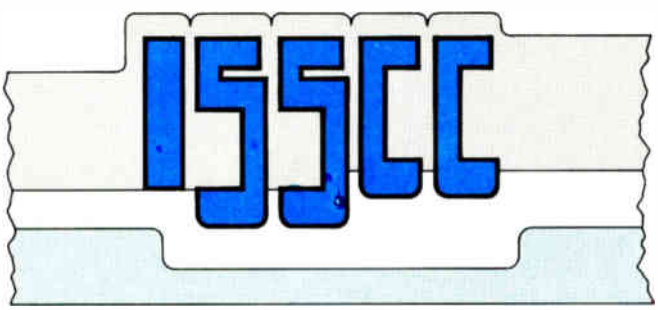
The other Japanese offering is an 8-bit unit that has on-chip electrically erasable programmable ROM, from Hitachi Ltd. One kilobyte of the EE-PROM can be erased in blocks, and 60 bytes can be erased and programmed a word at a time. The EE-PROM requires 500 milliseconds to erase and 5 ms to program and endures 10,000 such erase and write operations. In addition an unlimited number of reads can be done with an access time of 500 ns. The presence of nonvolatile memory on a single-chip microprocessor is something all the major contenders will go to eventually; Hitachi just happens to be first.

Most instructions are executed in approximately 3 μs at the nominal 1-MHz clock rate. Design rules of 4 μm are used to lay down 30,000 transistors on a 236-by-232-mil (6-by-5.9-mm) die. It runs off +5 and +25-v supplies and dissipates 900 milliwatts. The nonvolatile memory is implemented in metal-nitride-oxide-semiconductor technology.

Nippon Electric Co. discussed its single-chip graphics display controller, which turned out to be a very sophisticated device indeed. It can refresh a screen at the tremendously fast rate of 800 ns per dot from its 512-K-byte memory and can zoom, pan and, scroll.



2. Self-tester. The ability of a microprocessor to test itself becomes more important in the VLSI era of superdense chip. The experimental die illustrated, from West Germany's Institut für Theoretische Elektrotechnik, uses routines stored in ROM to test itself.



In memories, C-MOS speeds up and redundancy catches on

by John G. Posa
Solid State Editor

If 1980 was the year of the big 256-K MOS dynamic random-access memory, then 1981's ISSCC will be remembered for its fast static RAMs. Complementary-MOS static parts are achieving access times of less than 20 nanoseconds as 16-K MOS chips reach for 25 ns, and a 1-K bipolar static device waits less than 3 ns to present its data.

A second 64-K static RAM MOS was also unveiled, as was a 32-K chip needing only three transistors per cell. In addition, new techniques surfaced for implementing redundancy, self-refreshing, and nonvolatility. Also, improved bipolar processes are merging more different device types for high density or high voltage and, as always, new applications.

In all, seven MOS static RAMs were revealed. Their salient features are listed in the table.

The three fast C-MOS 4-K static RAMs illustrate the different ways to cut delays. First, all three designs scale down to 2-micrometer gate lengths. Beyond that, Toshiba uses a sapphire substrate and molybdenum silicide gates [*Electronics*, Sept. 11, 1980, p. 80], Hitachi employs a second-generation high-performance process—Hi-C-MOS II—and a sense amplifier with feedback, and Intel has turned to n-type wells in a p-type substrate [*Electronics*, Dec. 4, 1980, p. 39].

Hitachi dopes separate n- and p-type wells in a near-intrinsic substrate and uses vertical npn bipolar transistors for higher drive currents—as it did in its older Hi-C-MOS—while adding a second polysilicon layer to Hi-C-MOS II for a cell area about two thirds smaller. In its sense amplifier, a capacitor shunts the data input line, DATA, with the complementary output line, $\overline{\text{OUT}}$, and another capacitor connects $\overline{\text{DATA}}$ to OUT. The capacitors act as short circuits to the steep signal edges in the circuit. Thus, when the inputs change, the outputs assume their correct polarities almost instantaneously, then either supply or sink current, reducing the delay for latching to under 5 ns.

Like several other memories at the conference, Hitachi's design adds redundancy. Though that seems exces-

NEW MOS STATIC RANDOM-ACCESS MEMORIES

Company	Organization (bits)	Technology	Typical access time (ns)	Typical power dissipation (mW)		Design rule (μm)	Channel length (μm)	Cell area[a]		Chip area[a]		Comments
				active	standby			(mil²)	(μm²)	(mil²)	(mm²)	
Hitachi	4 K by 1	Hi-C-MOS II	18	150	0.5	n.a.	2	0.61	392	9,300	6	redundancy, feedback sense amplifiers
Intel	4 K by 1	C-H-MOS	25	90	10-0.05[b]	>3	2	2.7	1,742	18,300	11.8	n-type wells
Toshiba	4 K by 1	C-MOS on sapphire	18	200	0.05[b]	3.5	2	2.0	1,296	19,620	12.7	molybdenum silicide gates
Nippon Electric	16 K by 1	scaled-down n-MOS	25	575	70	n.a.	1.5	1.2	787	41,840	27	pure molybdenum word lines
Texas Instruments	16 K by 1	scaled-down n-MOS	30	550	70	3	2.5	1.6	1,032	41,712	27	column sense amplifiers
Mostek	4 k by 8	scaled-down n-MOS[c]	150	350	1	3	n.a.	0.86	555	52,000	33.5	three-transistor cell, redundancy
Nippon Electric	64 K by 1	scaled-down n-MOS	150	400	40	1.5	1.5	0.45	291.5	44,020	28.4	16-pin, 300-mil package

[a]Some rounding off was done. [b]With C-MOS input levels. [c]Single-polysilicon process. n.a. = not available

sive on a 4-K RAM, Hitachi's method of swapping in a spare column of cells with its associated decoder is nonetheless noteworthy for its uniqueness. A laser programs the part, but instead of burning out links the way Bell Laboratories does, Hitachi heats up the polysilicon between two highly doped regions, allowing impurities to diffuse in and lower its resistance from over 1 gigohm to less than 1 kilohm; these regions appear to be ordinary polysilicon load resistors placed in the decoder circuit. Another asset is that the laser pulses can be administered through the final passivation layer.

Like Toshiba, Nippon Electric Co. employs molybdenum, but to speed up a 25-ns 16-K RAM in bulk silicon. However, NEC uses it as pure metal—not as a silicide—and not for gates. Rather, it shorts out the first polysilicon film through six contact vias along each word line, cutting the line's delay by 6 ns. To subdue alpha radiation, NEC implants boron under each cell node, forming a buried junction to sweep away generated carriers.

The other 16-K-by-1-bit static RAM hails from Texas Instruments Inc.'s MOS Memory division in Houston. Contributing minimally to its 30-ns access time are the column-line sense amplifiers that replace the usual column (or Y) decoders. Decoders exhibit a high diffused capacitance; the much lower transistor gate capacitance presented by the sense amps improves overall speed by 20%, but at the expense of slightly greater power dissipation and chip area.

NEC also built, using 10:1 step-and-repeat photolithography, the second 64-K static RAM, following the recent announcement of an 8-K-by-8-bit memory from Matsushita Electric Industrial Co. [*Electronics*, Nov. 6, 1980, p. 145]. NEC's chip is 1 bit wide and stuffed into a 16-pin 64-K dynamic RAM's dual in-line package. This arrangement is not as inappropriate as it might first sound, as static parts are inherently faster than dynamic ones and more easily used. Though a big difference remains in the number of devices per cell for each memory type, processing complexities to enhance the performance of dynamic RAMs are narrowing that gap.

Moreover, if an idea from Mostek Corp. pans out, there may well be fewer devices per static RAM cell, as well. The Carrollton, Texas, company is testing a 32-K chip that needs only three transistors and one capacitor per cell to appear fully static.

The cell, shown in Fig. 1, stores a logical 1 with both kick and storage nodes high and a 0 with both low. With a high word line, data is transferred to and from the storage node through transistor Q_1. A 1 is written into the cell with the line labeled PC low; when PC is returned to the V_{CC} potential, the kick node, too, is charged—via Q_3. The pump signal bears a low-to-high triangular wave. If a 1 is stored, the capacitor couples the kick node high, replenishing the storage node through Q_2. With a 0 stored, Q_3 remains off and the kick node is kept discharged on account of substrate leakage.

Three-transistor cell

Because its contents are held actively, the cell's alpha-particle immunity is high. The cell area is 0.86 square mil (554 square micrometers)—roughly three times more than for a dynamic RAM's single transistor and capacitor cell. The chip, made with a single-polysilicon process, is organized as 4-K bytes, and Mostek will put it in a 28-pin package with 1-for-32-bit redundancy.

Based on density, a self-refreshing 4-K-byte RAM from Intel Corp., Santa Clara, Calif., could be seen as competing with Mostek's device—but not really, since Intel's entry is no more than a self-refreshing dynamic (or pseudostatic) RAM, controlled through a refresh-enable pin ($\overline{\text{REFEN}}$) on its 28-pin package. External refreshing is accomplished by strobing $\overline{\text{REFEN}}$ 128 times in 2 milli-

seconds; but with the pin low, the device will refresh itself with an on-chip counter. A separate ready line is asserted during self-refreshing to avoid contention. The device will perform a hidden refresh—even if it is not selected—if it receives an address-latch-enable signal. The memory also has redundancy—eight rows' worth. Its 400-ns cycle time is double its access time.

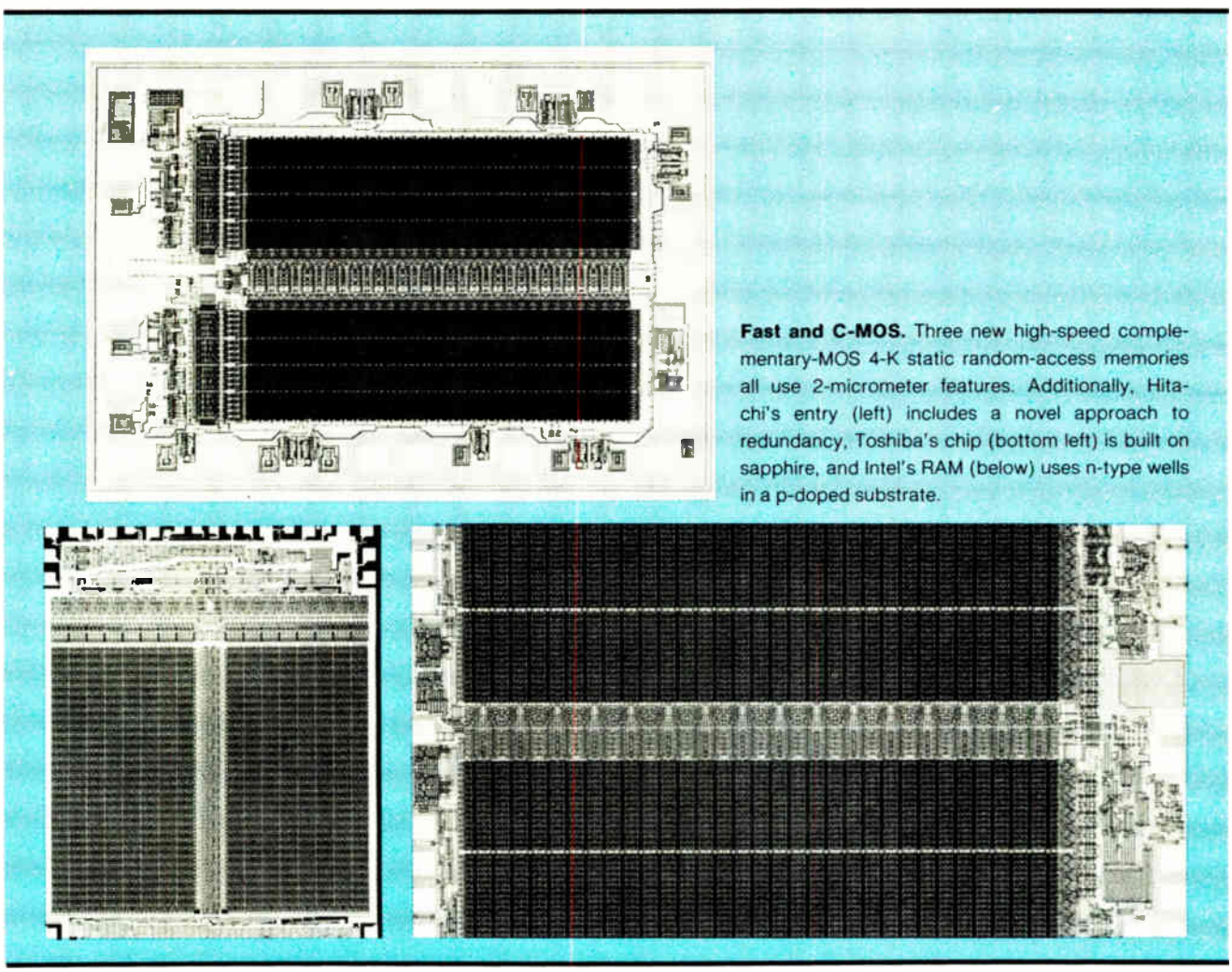
Self-refreshing and redundancy are also part of a 64-K dynamic RAM from Inmos Corp. The Colorado Springs, Colo., company is opposed to laser programming because of the precise mechanical positioning required. So, like a mounting majority of suppliers, it opted for fusible polysilicon links. However, fusible links in general usually mean a compromise between a large number of spare elements and the large area consumed the oversized interconnections and drive transistors involved with the high fusing-current pulses. Generally both cannot be minimized simultaneously because the arbitrary substitution of a small number of cells demands fuses to both route in the good elements and mask out the bad.

This tradeoff led at least one manufacturer to append large blocks of spare circuitry for a 25% redundancy to limit the number of fuses and related circuitry [*Electronics*, March 13, 1980, p. 115]. However, Inmos developed a circuit that consumes less than 5% of the chip area yet allows eight rows and four columns to be substituted arbitrarily. Intel Corp. also got more specific about its 16-K static RAM with redundancy [*Electronics*, Jan. 13, 1981, p. 196], and Bell Labs presented a paper stating that the redundancy on its 64-K RAM improves yield by 30%, typically.

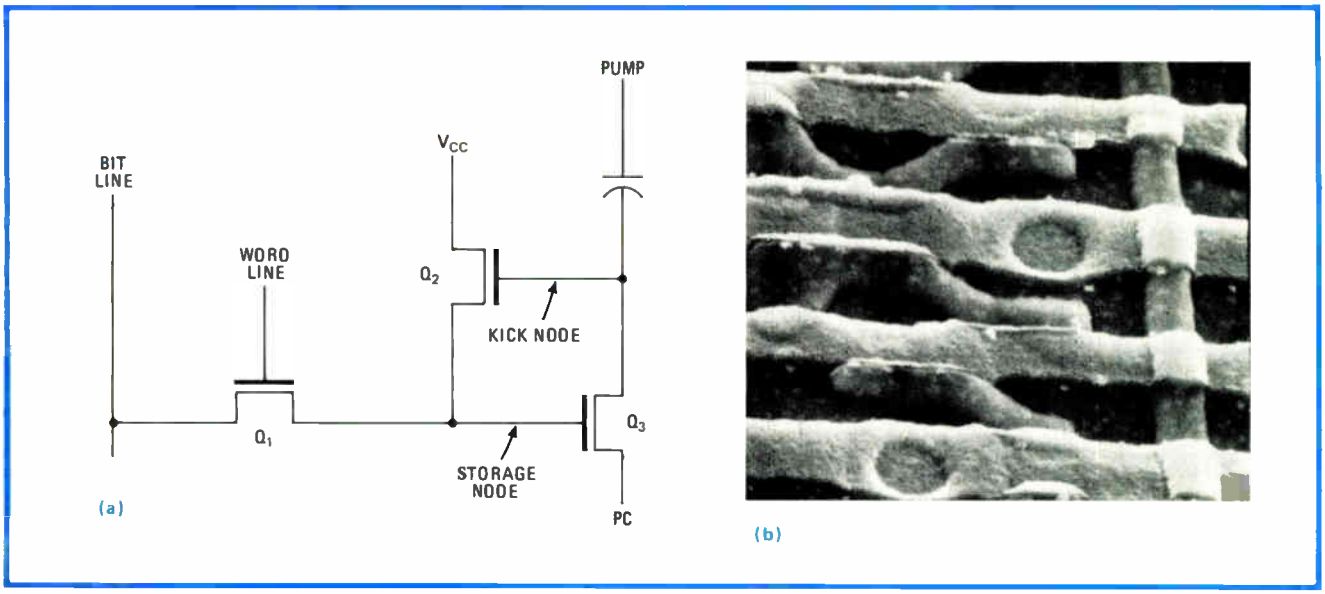
Inmos's 64-K RAM incorporates a so-called shared sense amplifier that connects to four bit lines instead of two, halving the number of sense amps and allowing full-sized dummy cells. A similar approach was taken by National Semiconductor and Fairchild in their RAMs [*Electronics*, May 22, 1980, p. 119], except that Inmos's layout also permits folded metal bit lines.

The part's internal organization is 16 K by 4 bits, enabling 4 bits of data to be shifted out in 80 ns, 20 ns per bit; this arrangement is similar to that of Texas Instruments' 64-K RAM [*Electronics*, Oct. 23, 1980, p. 26]. The die size, too, is similar to that of TI's chip, although slightly larger, but at 34,529 mil² (22 mm²) it is still tiny compared with most other designs. Inmos's self-refreshing is activated with the column-address strobe ($\overline{\text{CAS}}$) low as the row-address strobe ($\overline{\text{RAS}}$) falls. Thus, unlike the scheme of Mostek's and Motorola's 64-K RAMs, which depend on pin 1 for refreshing, Inmos's idea will remain valid at the 256-K level when that pin is considered for an address line.

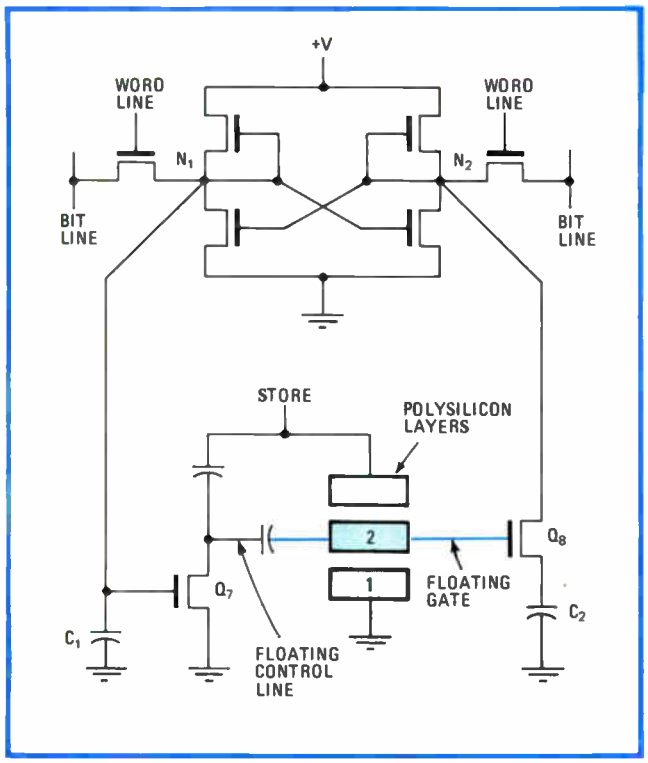
At 131 μm^2, Inmos's is the smallest 64-K RAM cell yet



Fast and C-MOS. Three new high-speed complementary-MOS 4-K static random-access memories all use 2-micrometer features. Additionally, Hitachi's entry (left) includes a novel approach to redundancy, Toshiba's chip (bottom left) is built on sapphire, and Intel's RAM (below) uses n-type wells in a p-doped substrate.



1. Dynamic static. Mostek has invented a fully static random-access memory cell that needs only three transistors and a capacitor per bit (a). A closeup of about two of the 0.86-mil² cells is shown in (b). Mostek will first use the idea in a 4-K-by-8-bit memory.



2. Xicor revealed. Xicor Inc. gave many more details about the nonvolatile cells in its 1-K shadow RAM. It uses three layers of polysilicon, and two transistors and four capacitors had to be added to a standard six-transistor cross-coupled flip-flop.

reported. But a new cell from International Business Machines Corp.'s Thomas J. Watson Research Center in Yorktown Heights, N. Y., needs less than a third that area, albeit with 1-μm rules. Cells in the Japanese 256-K RAMs described last year measured about 70 μm^2. Actually, with polysilicon word lines that double as capacitor plates, IBM's cell looks very much like Motorola's 64-K dynamic RAM cell. Differences include the use of tungsten silicide for a 2.7-ohm/square polysilicon sheet resistance and a high-capacity, or Hi-C, implant for a relatively high, 13.3-femtofarad node capacitance.

Both of the electrically erasable programmable read-only memories discussed rely on rough-textured polysilicon—with asperities—to enhance electron tunneling in order to charge and discharge a floating gate [*Electronics*, Sept. 13, 1979, p. 39]. One of the devices, from IBM, uses what it terms a dual electron-injector structure with a cross section resembling that of a floating-gate avalanche-injection MOS cell in a modern, double-polysilicon E-PROM. A key difference, though, is IBM's growth of a rough, silicon-rich oxide film on both the polysilicon control gate and the polysilicon floating gate, on the surfaces that face each other; between these, it grows a thin tunnel oxide. The rough oxide films enhance electron injection, so that a voltage of less than −16 V on the control gate will write the cell, and a like positive voltage will erase it.

IBM's idea reduces the programming from the 20 to 25 V required for today's EE-PROMs and E-PROMs, but a drawback is the necessity of the negative potential for programming. However, a new configuration from the company adds a second control gate to each cell, and this gate capacitively couples to the bottom side of the floating gate, thereby making possible all-positive-voltage operation.

The shadow is back

The other EE-PROM, from Xicor Inc. of Sunnyvale, Calif., connects to both sides of the floating gate by having three layers of polysilicon—one on either side. As shown in Fig. 2, layers 1 and 2 are given asperities so that electrons can flow up from level 1 to 2 for programming and from 2 to 3 for erasing. It is not yet known exactly how large the inducing voltages have to be, as these potentials are all generated on chip, so that the user needs only +5 V for all operations.

Xicor has discussed its shadow RAM previously [*Elec-*

tronics, Oct. 11, 1979, p. 111], but this is the first time it has disclosed full functional details of its cell. As the figure shows, two transistors and four capacitors are added to a standard six-transistor cross-coupled flip-flop to give each cell its nonvolatility.

If power fails, the store line is raised, and the flip-flop's data is transferred into the nonvolatile portion of the cell. If node N_1 is low, transistor Q_7 will be off, allowing the floating control line to go high when the store signal is raised. The high control line couples the floating gate high, and it becomes charged as electrons are attracted from the grounded first polysilicon layer.

If N_1 is high, Q_7 will be on, capacitively grounding the floating gate. However, the store signal can still be raised, attracting the electrons off the floating gate and erasing it. When power returns to the flip-flop, it will latch in accordance with the status of the floating gate. If the gate was charged, Q_8 will be on, capacitor C_2—which is larger than C_1—will load node N_2 as power ramps up, and the flip-flop will latch with N_1 high. Similarly, if Q_8 is off, C_1 will load N_1 and latching will occur with N_2 high.

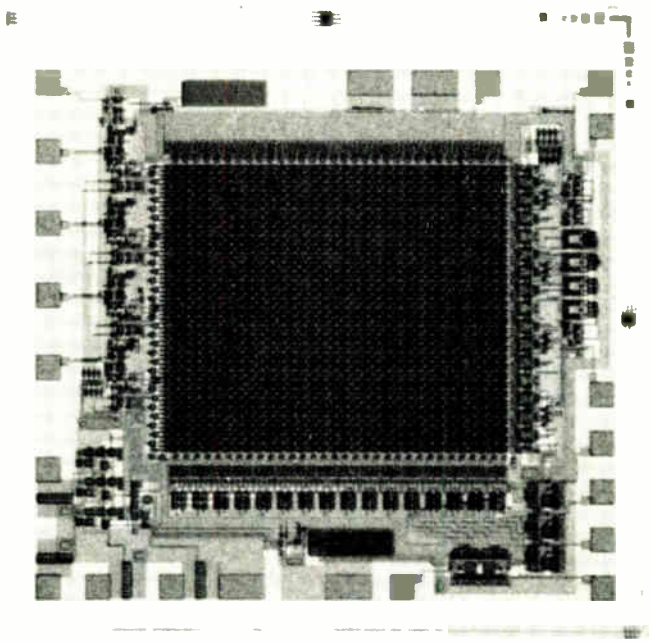
Respectable bipolar advances

The MOS memories at this year's ISSCC are impressive, but bipolar designers are not coasting either. Indeed, engineers at Nippon Telegraph & Telephone Public Corp.'s Musashino Electrical Communication Laboratory in Tokyo have measured access times of 2.7 ns on a 256-by-4-bit emitter-coupled-logic RAM—again, that is the access time, not a gate delay (see Fig. 3).

As might be expected, NTT uses local oxidation for device isolation and polysilicon for multiple self-alignment. Responsible for the high speed, though, is a submicrometer base width, formed as impurities diffuse down from a 2-by-2-μm doped polysilicon emitter. The completed cell measures 2,050 μm^2. NTT also developed something like a look-ahead reference circuit for the memory's sense amplifier that cuts the word line by about 15% while increasing the chip's 0.5-W power dissipation by only 3%. The company says that with a 1-μm process, access times could get as short as 1 ns.

At present, NTT is employing standard optical lithography, and so is Hitachi for another self-aligned bipolar process, developed at its Central Research Laboratory. A key feature of this structure is an npn sandwich formed with a single emitter mask. Contact to the collector is made to the bottom of the stack by way of the usual diffused underpass; aluminum connects to the emitter, and doped polysilicon makes contact to the base from the side, around its perimeter. So far, Hitachi has only fabricated experimental integrated-injection-logic gates, but has found that devices with 6-by-50-μm^2 emitter areas perform as well as conventional bipolar transistors with emitter areas half the size.

Speaking of I^2L, researchers at IBM's Yorktown Heights, N. Y., and Böblingen, West Germany, facilities continue to improve their combined I^2L and merged-transistor-logic memory cell, introduced in 1978. Two beauties of this cell are its compactness and its built-in high-impedance load. A limitation, however, is the use of the voltage differential across an injector diode as a sensing signal. Only about 25 millivolts to begin with, it decreases as the reading current increases and this limits performance.



3. Blink and miss it. This 256-by-4-bit emitter-coupled-logic RAM from NTT's Musashino lab has a 2.7-nanosecond access time. It is made out of silicon, not gallium arsenide. The researchers say that with 1-micrometer-wide lines, 1-ns access times are possible.

IBM solved the problem by splitting the emitter common to the two cross-coupled npn storage transistors in the cell, connecting them through individual resistors to the word line. The voltage developed across the resistors is now the basis for sensing, which is much more substantial.

The I^2L-MTL memory cell does not pay too heavy an area penalty either, because the resistors are formed in an n-type epitaxial layer and so are buried. Secondly, a pair of resistors can be shared among a group of cells. With 3.5-μm features, the cell is 1,200 μm^2, about 15% larger than previous cells without the split emitters. But then, whereas a 16-K static RAM made with the older cell accesses in 45 ns [*Electronics*, Feb. 14, 1980, p. 142], the latest version cuts that figure to 25 ns.

High-voltage I^2L

While IBM is optimizing I^2L for memory applications, Siemens is raising its operating voltage for phase-locked-loop chips and other complex integrated circuits that combine analog and digital functions on a single die. Siemens' new device, which it named the gate-underlaid transistor, gets its high-voltage integrity from junction field-effect transistors formed without added processing steps because the devices are well merged. When the collector voltage reaches the pinch-off voltage of the J-FET, it saturates, limiting current and shielding the overall device—to 40 volts, so far.

Some other applications of bipolar technology at the conference include a convolver chip from TRW Inc.'s Microelectronics Center in Redondo Beach, Calif., that uses 1-μm design rules [*Electronics*, Dec. 4, 1980, p. 44]

and a master slice from Mitsubishi Electric Corp.'s LSI Research and Development Laboratory in Itami, Japan. It integrates 2,500 0.83-ns 0.54-milliwatt ECL gates on a huge, 7.76-by-10-mm (120,520-mil²) die. The chip is housed in a 224-pin package, of which 148 serve for input/output, 16 for power, and the rest are unused.

ISSCC

Telecom chips near goals, GaAs unlocks microwaves

by Harvey J. Hindin
Communications & Microwave Editor

One of the points of impact of large-scale integration for the communications industry is the interface between standard analog telephone lines and digital switching or transmission systems. Each ISSCC meeting in recent years has emphasized devices for this purpose, and that is even more true this year.

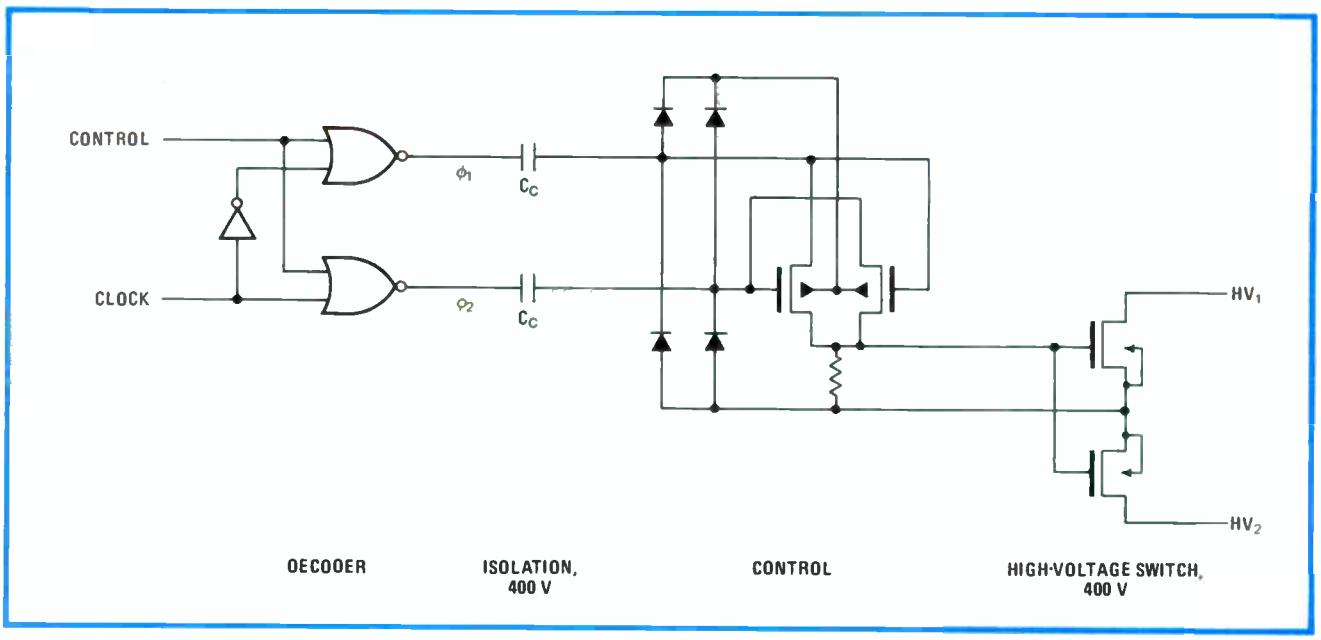
Monolithic codecs, high-voltage cross-point arrays, and subscriber-line interface circuits with low power consumption are what is desired. But they must be available at a low price, since hundreds of thousands if not millions have to be purchased.

Perhaps the chief chip of interest is the codec. In fact, recent years have seen the emergence of what one industry figure called the codec-of-the-month club. For Bell Laboratories' Harry Mussman, who is presiding at a session with three codec papers, there is a good reason for this flood: "There is a very necessary continuing effort to keep codec performance high and reduce its size so that it can be produced cheaply and reliably." And, he adds, the lower the power consumption, the better. At previous meetings, all the codecs discussed but one had their associated filters on separate chips. That is not the most cost-effective way for a codec to do its chores. Now, Mussman says, this is the first conference where each codec has its filters on chip, and "they all seem to work well and meet their required specifications."

All three codecs are amazingly similar in design (see figure, p. 147). They all use complementary-MOS technology, and each chip is about 46,500 square mils (30 square millimeters). Two have reference voltage generators on chip and one does not—yet. Some, according to Mussman, are able to select A- or μ-law companding for European or U. S. use, respectively, with a metal mask option. This approach yields flexible parts that can be sold all over the world. Moreover, the chips can usually be turned off when they are idle. All these similar features, he says, show that "we are converging on a standard part."

From Japan . . .

The cross-point array designed by a team from Nippon Telegraph & Telephone Public Corp. and Oki Electric Corp. in Tokyo is a refined version of the one presented by the same group at the ISSCC in 1979. This



1. High voltage. ITT's Bell Telephone Manufacturing Co. in Antwerp has built a chip that can switch up to 400 volts under isolated low-voltage control. It is a precursor of more elaborate cross-point arrays that will handle multiple signal paths.

device is used as a concentrator. For example, a central office may have four times as many input lines as codecs and they are interconnected with a solid-state cross-point array [*Electronics*, March 1, 1979, p. 41].

The major advance the Japanese researchers have made is to reduce the triggering current that the array's light-emitting-diode drive needs by about 75%. That makes it easier to control the array and reduces the power needed. Another accomplishment was the mounting of the pnpn switches with solder rather than with wire bonds, which means easier fabrication. Finally, instead of dielectric isolation, a form of air insulation is used, dubbed "canal isolation" by the designers. It is achieved by cutting into the die with a saw.

. . . and Belgium

Not to be outdone, ITT's Bell Telephone Manufacturing Co. in Antwerp has produced a 400-volt cross-point array comprising four separate parts—a control logic decoder, 400-V isolation capacitors, a switch controller, and a 400-V switch (Fig. 1). The switch is really two back-to-back vertical double-diffused MOS transistors that are turned on and off by a series of pulses generated by the controller. The low-voltage control inputs and the high-voltage output terminals are completely isolated dielectrically, even though the switches and control and decoding logic are fully integrated.

A subscriber-line interface circuit—often called a SLIC—is the device that connects the telephone subscriber's local loop in his or her home or office with the codec and associated filter used in the telephone company's office. A full-fledged SLIC performs what is known as the Borsht functions [*Electronics*, June 5, 1980, p. 113], which are concerned with feeding battery power to the subscriber's phone, two-to-four wire conversion, lightning protection, and other maintenance and test functions necessary to telephone service.

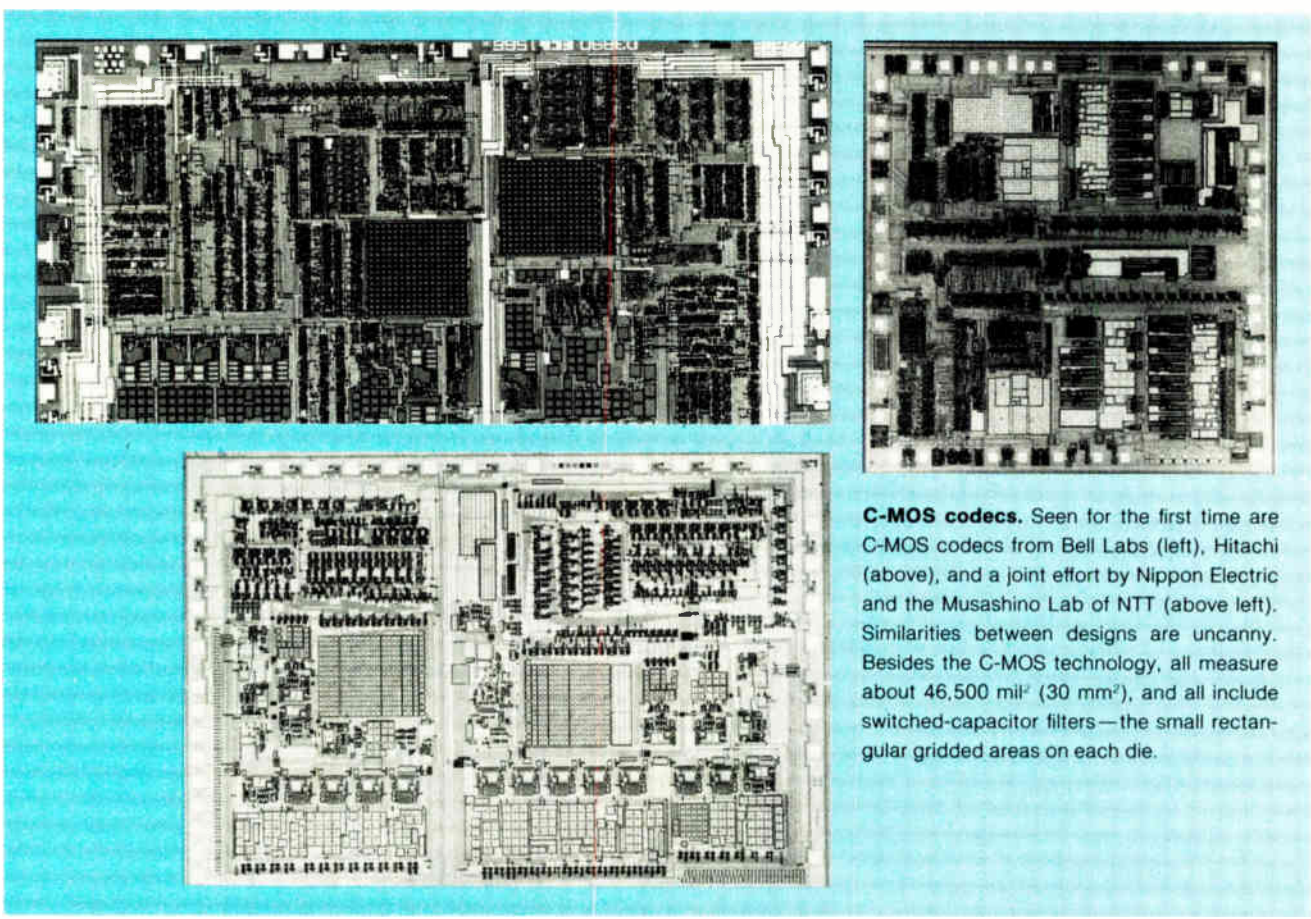
Although these devices have been available in hybrid-circuit form for some time now [*Electronics*, May 8, 1980, p. 41], the race is on in the semiconductor industry to produce one in monolithic form that performs as many of the Borsht functions as possible, since it is clearly desirable to use as few external components with the SLIC as possible.

For the Harris Semiconductor operation in Melbourne, Fla., a monolithic subscriber-line interface means a chip that uses 80-V dielectric-isolation technology, needs but a single 12-V power supply, and consumes 110 milliwatts. It is suitable for use in both private automatic branch exchanges and central offices, even though the requirements for these two applications differ insofar as the Borsht specifications are concerned.

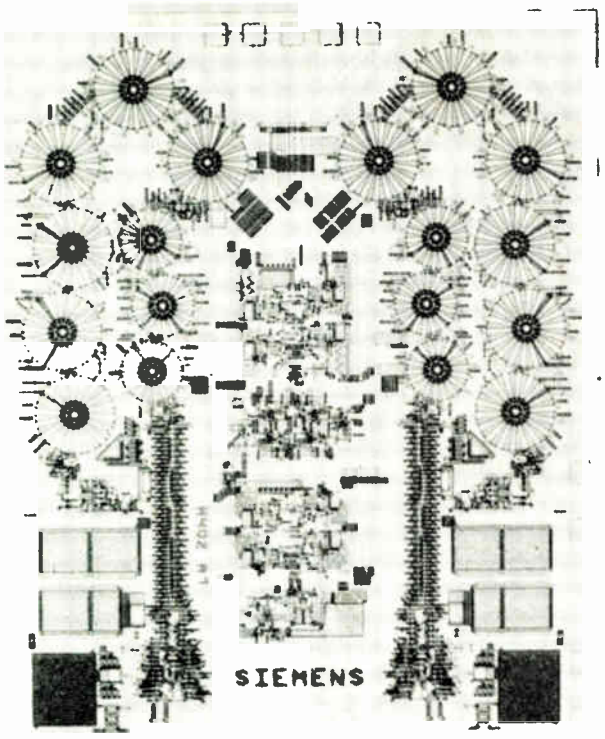
A selection

Harris's SLIC cannot perform all the Borsht functions but it is not unique in that regard. Both Motorola and Siemens have introduced SLIC-like chips. And Bell Labs' offering does not even call itself a SLIC.

With Harris's approach, both protection circuitry for lightning and relay ringers are necessary between the



C-MOS codecs. Seen for the first time are C-MOS codecs from Bell Labs (left), Hitachi (above), and a joint effort by Nippon Electric and the Musashino Lab of NTT (above left). Similarities between designs are uncanny. Besides the C-MOS technology, all measure about 46,500 mil² (30 mm²), and all include switched-capacitor filters—the small rectangular gridded areas on each die.



2. Modern art. Siemens' analog filter is suitable for frequency-division multiplexers. The CCD chip offers resonator quality factors, bandwidth, and stability that substantially improve the performance of radio-frequency communication equipment.

subscriber-loop two-wire connection—called the tip and ring—and the SLIC itself. A balance network between the SLIC and the codec plus filter is needed to maintain current flow at the proper levels in what is now a four-wire connection. Also, external resistors and capacitors are required for tuning and filtering. Among other features, the SLIC will perform battery feeding, overvoltage protection (with some external devices), ringing control, line supervision, off-hook condition detection, and two-to-four-wire conversion. In addition, it features an uncommitted operational amplifier for the external balance network.

At Bell Labs' facilities in North Andover, Mass., and Reading, Pa., another device—not a SLIC but a chip for a SLIC, says Bell—called a "transformerless trunk and subscriber-line interface" has been made using a 60-V, beam-leaded, junction-isolated bipolar technology. The Bell researchers call it a "straightforward" realization of transformerless line circuits with operational amplifiers. The op amps contain both vertical pnp and npn transistors with current gains (betas) of 100 and cut-off frequencies of about 200 megahertz.

Current balance

The high-voltage integrated circuit needs some low-voltage control off chip to achieve such Borsht functions as battery feed, auto coupling, and current limiting. Its designers are particularly proud of its current balance and note that good longitudinal performance has been difficult to obtain with transformerless interface circuits. However, the Bell team has come up with 86 decibels of longitudinal balance at 1 kilohertz on a 127-by-127-mil (3.2-by-3.2-mm) chip. The quiescent dissipation from the attached 48-V battery is only 8 mW in the powered-down condition and 65 mW when the device is on.

For communications systems, a monolithic filter means high-performance processing of analog signals with a minimum use of hard-to-come-by power. Of the several choices possible, West Germany's Siemens AG prefers a charge-coupling approach because devices manufactured using this technology do not suffer from self-oscillation. Furthermore, charge-coupled-device filters have center frequencies that are independent of fabrication tolerances and bandwidths that are dependent solely on MOS capacitance ratios. Therefore, they can be specified and built precisely.

CCDs for FDM

The Munich-based firm has taken advantage of the CCD approach with two analog communications filters. In one, a company research team built a completely self-contained bandpass filter for frequency-division–multiplexed modems (Fig. 2). It needs only 37 mW and achieves a bandwidth of 97 hertz at 131.85 kHz, which is equivalent to a quality factor (Q) for the CCD passive resonators of 1,350. That is extremely high compared with what can be obtained at this frequency with lumped-constant filters. (Normally, a Q of a few hundred at most can be expected.) The tolerance achieved for the center frequency specification was ±3 Hz—again a figure that is first-class and not obtainable with lumped-constant technology.

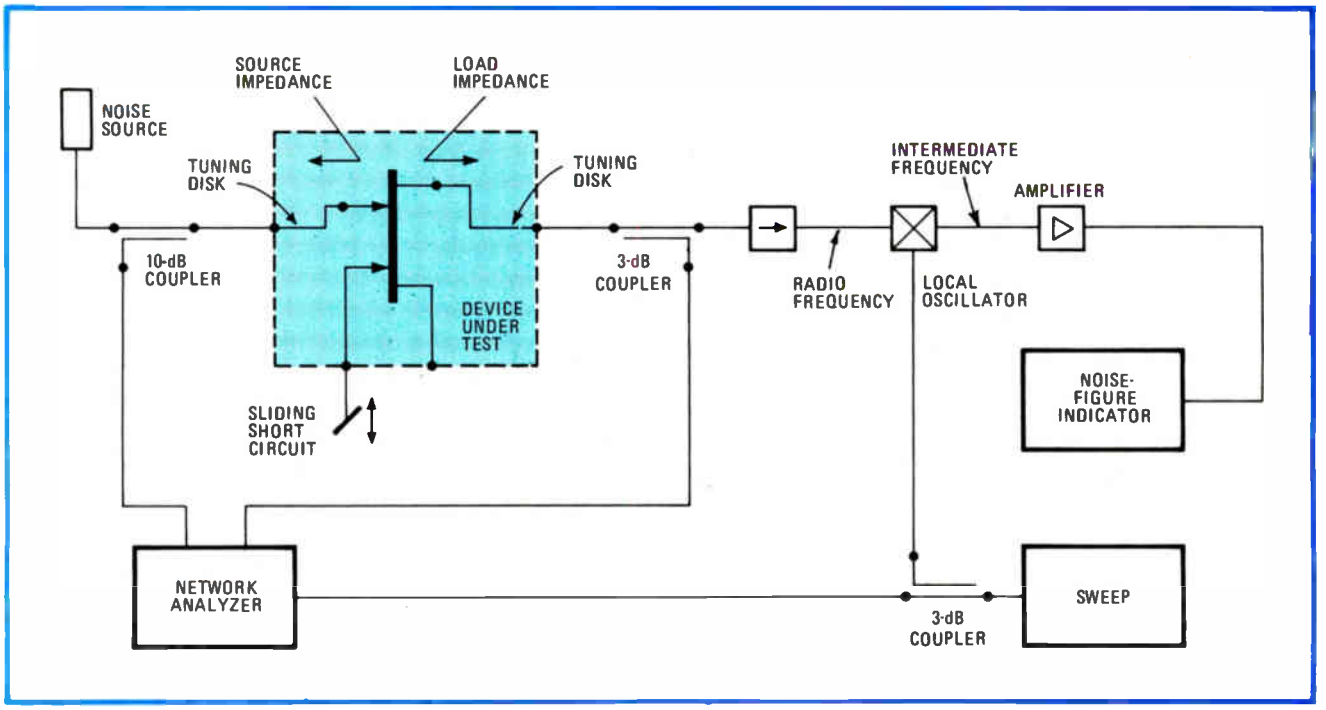
The modem filter requires just one 12-V supply and is implemented in standard n-channel double-polysilicon-gate MOS technology. It needs a 2.37-MHz master clock, the stability of which determines the stability of the filter's center frequency. The die size for a chip with two filters and clock generation and bias circuitry is a modest 130 by 157 mils (3.3 by 4.0 mm).

A Siemens group consisting of much the same people has developed another CCD filter for FDM modems. In this case, the monolithic device has a classic Chebyshev filter response characteristic centered at 50 kHz, with a bandwidth of 4.2%. It achieves the same stop-band attenuation as Siemens' other filter—60 decibels.

However, there is some disagreement over whether CCD filters are the best way to go for solid-state frequency filters. In fact, for a team led by John Mavor of the University of Edinburgh and his colleagues at University College in Dublin, the switched capacitor approach is better (see p. 79). Furthermore, Mavor says, a C-MOS implementation of such a filter (it is done with n-MOS now) will have characteristics superior to those of any other switched-capacitor approach when bandpass designs are necessary.

Shift that phase

In microwave technology, gallium arsenide is the watchword at this year's ISSCC. This compound—for monolithic microwave chips what silicon is for lower-frequency devices—is the substrate material for such diverse devices as analog phase shifters, varactor-tuned oscillators, and a receiver front end. As is usual for the



3. Multipurpose. This measuring setup allows both characterization of the source and load impedances presented to the FET phase shifter and on-line observation of the circuit's scattering, or S, parameters, as well as its noise figure and bandwidth.

conference, these devices are preliminary in nature. But they indicate that, for microwave ICs, GaAs is the way to go for the 1980s.

The technique for constructing analog phase shifters has been known for some years. Dual-gate GaAs FETs are the key to a successful design because in phased-array radar systems, for example, they can make possible a degree of fine phase adjustment on each array element to improve the antenna array sidelobe levels. Moreover, a properly tuned GaAs FET amplifier can simultaneously provide gain, a low noise figure, and phase shifting.

Shifting phase

Achieving all these parameters is no easy feat, but engineers at LEP (Laboratories d'Electronique et de Physique Appliquée), Limeil-Brevannes, France, have made a one-stage phase shifter yield 10 dB of gain and 90° of continuous phase variation. They have also achieved a gain of up to 30 dB, 140° of phase shift, and a noise figure of less than 4 dB at 13 gigahertz (Fig. 3). In their approach, a dual-gate GaAs FET accomplishes both the phase shifting and amplification, with a single-gate FET providing additional amplification and also acting as a buffer stage.

But these results, as impressive as they are, are not indicative of any limitations on the technique. What can be realized is a function of the input and output matching to the GaAs FET stages and whether various forms of mechanical tuning like sliding short circuits are used. The bandwidth of the amplifier's input and output networks and the bias voltages on the FETs also determine what is possible.

Charts and graphs summarizing the complex interrelationships between all the parameters of the GaAs amplifier network and the phase shift that can be achieved—at least for their circuits—were presented by the Allan Clark Research Centre of Plessey Research Ltd. in Caswell, Northants., England. To vary the coupling of their amplifier input and output circuits, Plessey's researchers employ mechanical tuning disks. They conclude that, for the cases investigated, the most critical part of the circuit is the input matching network.

As is true of the French phase shifter, the English one has a ripple in both the gain and the phase characteristics under most conditions. Add to those the amplitude and phase variations as a function of temperature—enough to require compensation—and it is clear that the GaAs FET phase shifter has a long path to travel before anyone will be shipping it for use in phased arrays.

GaAs FETs can also be configured as electronically tunable voltage-controlled oscillators. In fact, theory says that tuning of greater than one octave is achievable in both the X and Ku bands using submicrometer-gate GaAs FETs, hyperabrupt GaAs varactors, and both lumped and distributed passive circuit elements. For Texas Instruments Inc.'s Central Research Laboratories in Dallas, the theory translates into a voltage-controlled oscillator tuning from 7.3 to 15.6 GHz with a tuning voltage varying from only 0 to 16 V. The oscillator generates 4 mW with a 4-V, 80-milliampere input. These characteristics represent the state of the art for such a device.

Tune that frequency

According to TI's researchers, classic small-signal scattering parameters were used to determine the GaAs source and gate-terminal impedances for optimum oscillator operation. Because adequate bandwidth was a potential problem, computer-aided design techniques

were called on to get the last drop of bandwidth out of the drain circuit.

TI fabricated both the GaAs FET and the GaAs varactor. For the former, what the investigators called a "proven combination" of gold, germanium, and nickel contacts; titanium, platinum, and gold gates; and silicon nitride passivation was chosen to make the inherently high-gain and broad-bandwidth 0.5-by-300-μm gate. For the latter, vapor-phase epitaxy and ion implantation were combined to achieve a wide capacitance swing, low bias-voltage requirements, and low series resistance.

Building microwave components on GaAs substrates is well and good, but these accomplishments are only preliminary to integrating entire subsystems or systems. One such subsystem has been put together by the Massachusetts Institute of Technology's Lincoln Laboratory in Lexington, Mass.

Researchers there have made a 31-GHz monolithic receiver prototype as part of an ongoing program to look into the feasibility of GaAs for both transmitters and receivers at millimeter frequencies. It is fabricated with a mixer-diode front end and a metal-semiconductor FET preamplifier, all on a GaAs substrate. It has a conversion gain of 4 dB and maintains a single-sideband noise figure of only 11.5 dB.

What's more, the device can be improved. Noise-circle analysis of the intermediate frequency amplifiers, say the researchers, shows that the receiver's noise figure can be brought below 10 dB. In fact, they add, with two amplifier stages the receiver chip can have its conversion gain go up 10 to 14 dB.

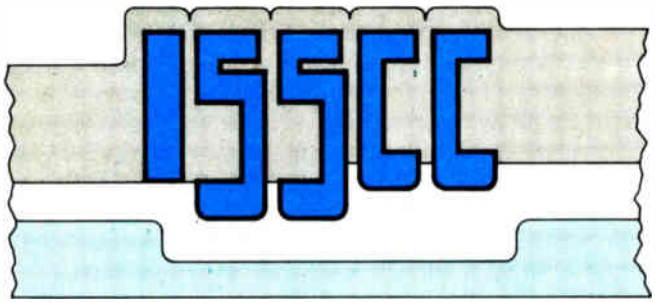
The problem they faced in their design was the integration of the Schottky-barrier mixer diode and the low-noise MES FET preamplifier. Because high-cutoff-frequency diodes and MES FETs demand different layer structures, different epitaxial requirements are imposed on the semi-insulating GaAs wafer. The engineers were able to develop a procedure for the deposition of these separate layers that was reproducible and that yielded acceptable receiver specifications.

Detect the light

For fiber-optics watchers, there is not much at this year's ISSCC except for a single-chip 200-megabit/second receiver from International Business Machines Corp.'s Thomas J. Watson Research Center in Yorktown Heights, N. Y.

The device is fast enough to keep up with computer data-transfer rates and generates logic outputs directly from a p-i-n photodiode [*Electronics*, Dec. 4, 1980, p. 40]. Key to its design is the use of what is known as current-mode amplification in place of the usual integrating or transimpedance amplifiers.

Current-mode amplifiers are not limited in speed by transistor base-spreading resistance as are conventional amplifiers using differential pairs. Furthermore, they are well suited to integration because they need few resistors and their gain and bandwidth do not depend on precisely fabricated electrical parameters. Based on master-slice technology of five years ago, the design may be extendible to 1 gigabit/s with the latest such chips, the IBM researchers say.



Linear ICs advance in drive, accuracy, frequency

by Roger Allan
Components Editor

Linear and discrete integrated circuits like monolithic data converters and operational amplifiers, power transistors, and control devices are confidently matching strides with digital integrated circuits. In fact, linear and discrete IC technologies have never been as varied as this year, with many papers coming from overseas.

As expected, data-conversion technology was well represented, with papers on the latest monolithic analog-to-digital and digital-to-analog converter designs. Japanese designers are showing surprising strengths in such parts, as evidenced by three interesting technical presentations. One of these, from Hitachi Ltd., describes a d-a converter with a linearity of 14 bits to within $\pm\frac{1}{2}$ least significant bit without the usual on-chip trimming of analog components. This accomplishment is yet another step up in linearity for untrimmed monolithic d-a units, the previous level having been 12 bits in a bipolar design manufactured by Advanced Micro Devices Inc., of Sunnyvale, Calif. [*Electronics*, Dec. 6, 1979, p. 152].

Intended for consumer high-fidelity audio systems, Hitachi's device packs 1,230 integrated-injection-logic gates and 470 linear devices on a chip that is 161 by 205 mils (4.1 by 5.2 millimeters). Fourteen-bit linearity without trimming is achieved by comparing a ramp-function output with the output of the main part of the d-a converter (Fig. 1). The comparator's output is then fed back through a flip-flop, a counter, and a random-access memory to a subcircuit of the d-a converter. The converter achieves a 1-microsecond settling time (to 1 LSB) and has an output of about 4 volts peak to peak. Its designers feel confident it can yield 16-bit linearity.

The 16-bit level is what Sony Corp. has reached in an a-d converter for pulse-code-modulation audio systems. Using a coarse-fine integration technique, it has produced a 50-kilohertz device that is completely monotonic and accepts input signals of up to 20 kHz. A combination

of I^2L and emitter-coupled-logic technology produces a linear-compatible 5-V device with a 50-megahertz clock frequency and a signal-to-noise ratio of 95 decibels.

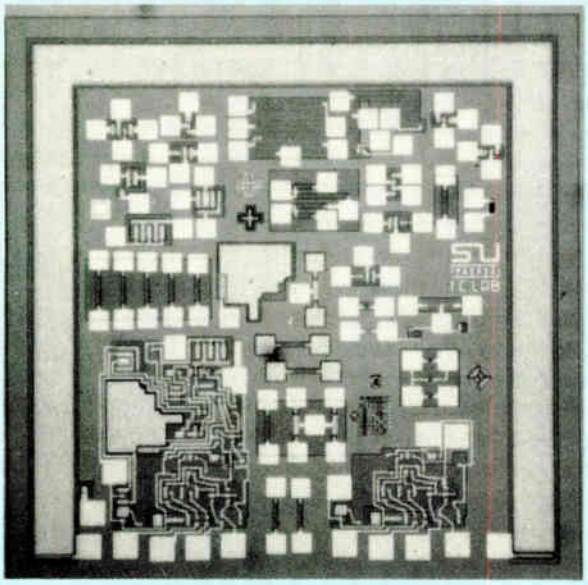
Error correction is the latest function to be added to an a-d converter. It appears in a 14-bit complementary-MOS unit from Intersil Inc., Cupertino, Calif. The converter's 161-by-165-mil (4.1-by-4.2-mm) chip houses a thin-film nonbinary 17-bit d-a converter similar to a conventional R-2R ladder network but using a radix of about 1.85 instead of the usual 2. It also contains an erasable programmable read-only memory for converter calibration. The part converts in 20 μs.

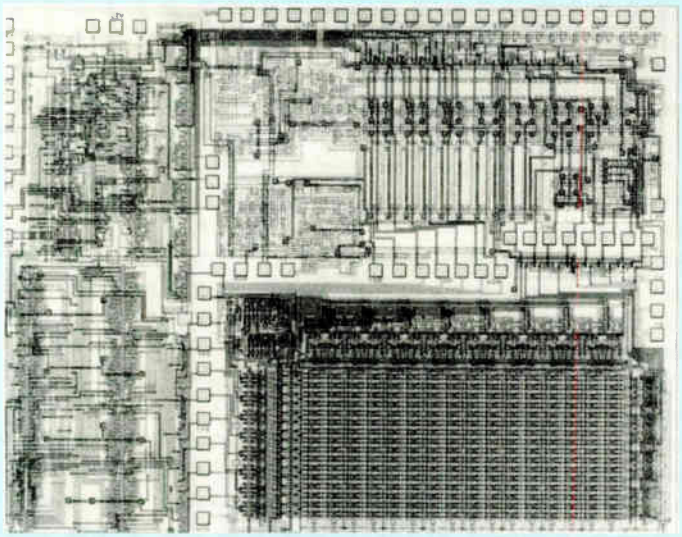
High voltage

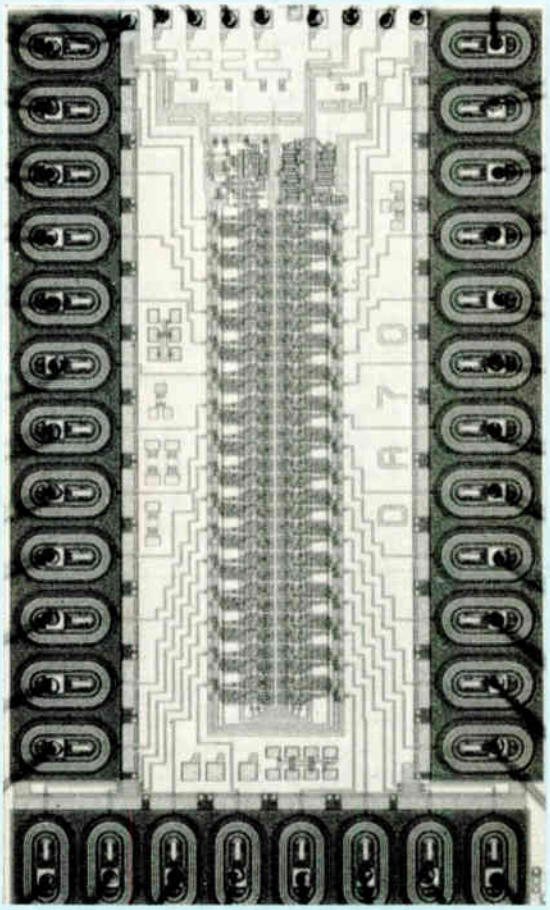
New performance plateaus are being reached, too, in designs for very low-level operational amplifiers and amplifiers capable of handling hundreds of volts. One high-voltage amplifier is a video device from Thomson-CSF, Saint-Egrève, France, for color TV applications. The monolithic amplifier includes a bipolar differential-input section and employs double-diffused MOS technology for the cascode-amplifier and current-driver sections. Its performance, which is said to be comparable to if not better than that of larger and more expensive hybrid designs, is exemplified by a 300-V maximum supply potential; a 150-V dynamic range (at a supply voltage of 220 V); and a 5-MHz, 3-dB bandwidth. The power dissipation is 3 watts maximum.

Signetics Corp., Sunnyvale, Calif., uses localized positive feedback in a programmable monolithic operational amplifier to achieve a 1-gigahertz maximum gain-bandwidth product. The op amp is configured as an open loop in which a voltage-to-current converter input is followed by a current amplifier and then a current-to-voltage converter. Constructed on a 56-by-78 mil (1.4-by-2.0-mm) chip, it features a total harmonic distortion of 0.1% over a programmable gain range of 0 to 100, for a 1-V peak-to-peak signal output. Depending on the gain level programmed, the device dissipates 60 to 100 milliwatts.

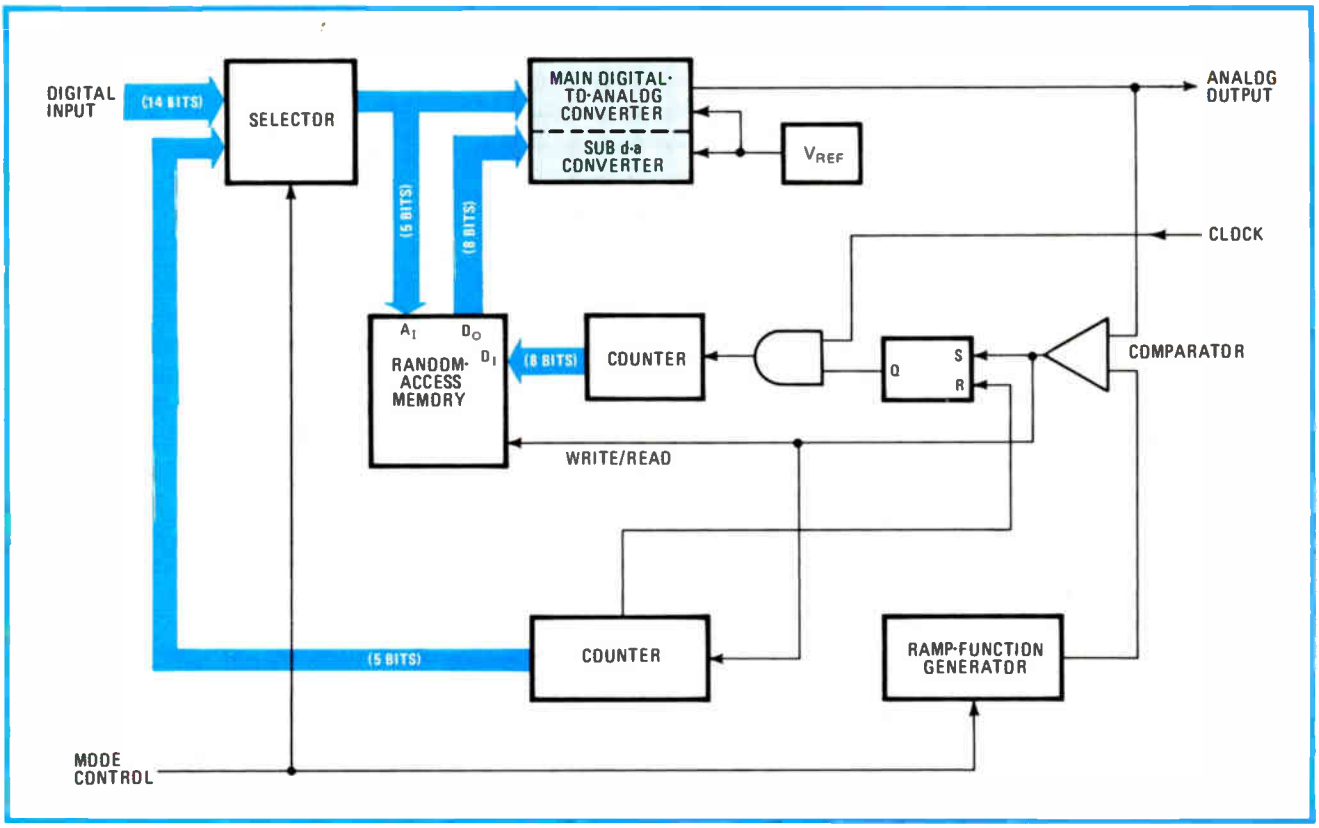
Of all the wideband monolithic amplifiers available on







Drive, detect, convert. Linear and data acquisition components introduced this year include an MOS integrated circuit from Sharp (above) that provides 400 volts to drive an electroluminescent display; a chip from Stanford University that finds the true mean frequency in a signal's power spectrum (above left); and a 14-bit digital-to-analog converter from Hitachi (left).



1. Untrimmed. Up to 14 bits of linearity (to within ±½ least significant bit) are possible from this digital-to-analog converter from Hitachi—without the usual trimming of analog components on the chip. The 161-by-205-mil chip is designed for hi-fi audio systems.

the market, few if any combine their wideband specification with low-noise performance. In addition, most come in large packages that not only require external components but also have large leads that contribute unwanted inductances, leading to poor performance at high frequencies. Signetics engineers, together with researchers at the University of California at Berkeley, have overcome these drawbacks with a wideband low-noise IC amplifier in a TO-46 can.

Sporting a 4.4-dB noise figure, the 725-MHz device has matched 50-ohm input and output impedances and requires only four connections to the external world: input, output, power supply, and ground. No external components are needed. The amplifier has a gain of 18 dB and a 1-dB gain-compression point of +3 dBm and dissipates 180 mW.

New sensor designs emerge

Sony has also produced a silicon magnetic sensor employing a saturation velocity principle that allows it to achieve high magnetic sensitivity independent of bias voltage and temperature. Made with a conventional planar process, the lateral device is built on a substrate whose 300-micrometer thickness does not influence sensor sensitivity, as conventional sensor substrates do.

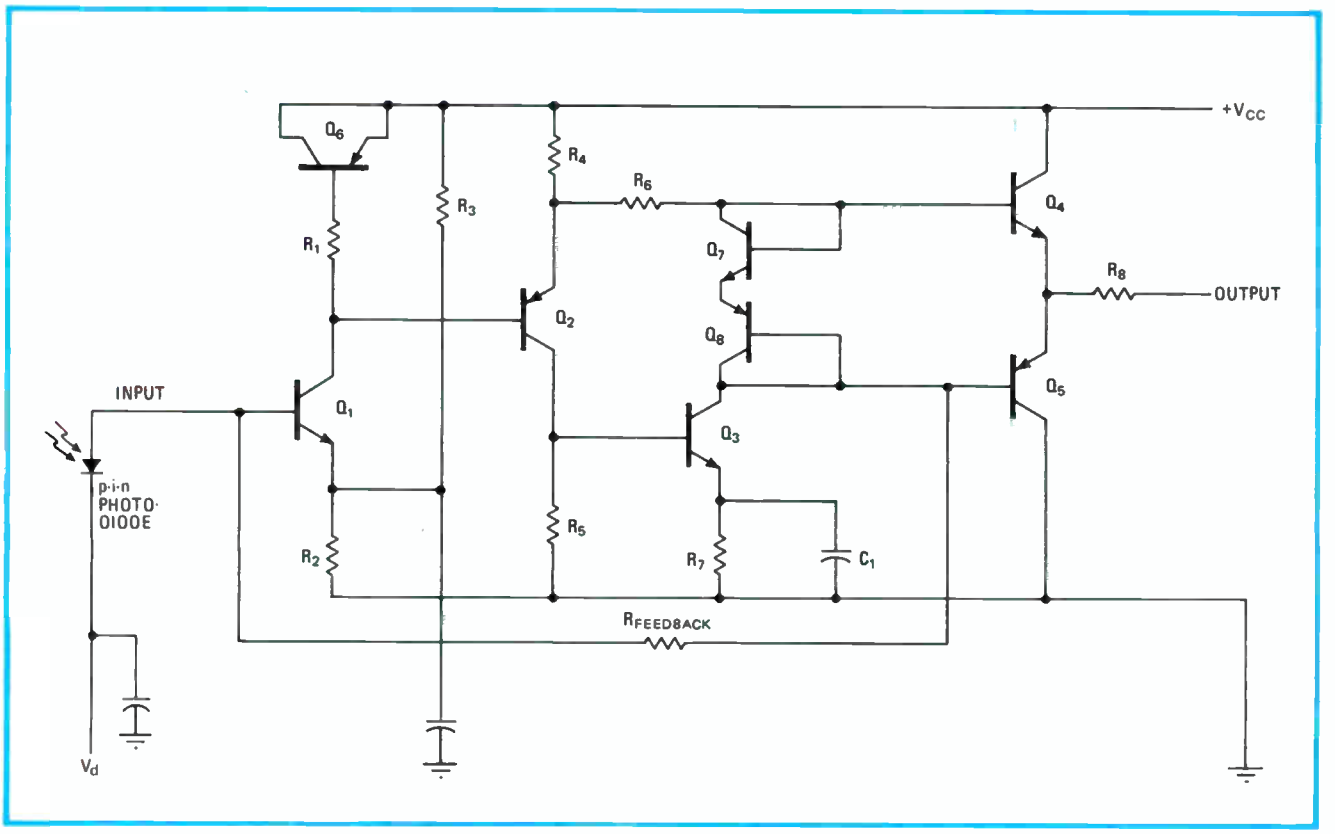
A different type of sensor is a monolithic power-spectrum centroid detector from the Electronics Laboratories of Stanford University in Palo Alto, Calif. The device estimates the centroid of a signal's power spectrum by defining its true mean frequency. It can be used in doppler sonar and radar applications, doppler ultrasonic blood-flow and velocity measurements, communications, and real-time signal spectral analysis and compression. Powered by ±7.5 V, the detector has an overall nonlinearity of 2% and a sensitivity of less than 0.1%/°C.

Stanford researchers have also produced a fully integrated rf-actuated battery controller for implantable telemetry systems. The 146-by-146-mil (3.7-by-3.7-mm) chip has 1-millivolt sensitivity at a standby current of 300 nanoamperes. An on-board I^2L ring-oscillator divider determines the on-time of the implanted package it is housed in, establishes acceptable input activation signals, and enables serial programming of the package's on-time. The device alleviates the problems of rf and magnetic interference common to conventional nonlatched continuous-rf devices and of accidental activation typical of conventional latched magnetic-reed switches.

Yet again from Sony comes a dual-channel audio IC for volume and tone control that has just 0.002% distortion and a 100-dB S/N ratio. Both figures are obtained with a 300-mV root-mean-square input signal and at a frequency of 1 kHz. The chip, 220 by 217 mils (5.6 by 5.5 mm), contains 110 MOS field-effect transistors as low-distortion switches, 1,000 MOS FETs as decoders, and 100 polysilicon resistors.

High-voltage devices for displays

Another consumer IC from Japan is a high-voltage driver IC from Fujitsu Laboratories Ltd. Designed for TV deflection coil, plasma-panel display, and electrostatic-printer circuits, it is made with an epitaxial spinel process that allows the integration of both low- and



2. Low noise. Using a single external p-i-n photodiode with a monolithic heterojunction preamplifier enables Sony researchers to achieve a broad bandwidth (30 megahertz) and notably high detectivity (1.53×10^{11} cm-Hz$^{1/2}$/W) in a photodetector.

high-voltage circuits on the same chip. Spinel, a magnesium aluminum oxide, is vapor-deposited onto shallow wells that are etched into a silicon substrate. Silicon is then grown epitaxially atop the spinel in order to fill the shallow wells.

Fujitsu achieved 450-V isolation between adjacent wells for spinel thicknesses of 1 μm and demonstrated that silicon-on-spinel structures have superior breakdown qualities to those of silicon-on-sapphire structures. At a potential of 5 V, for example, leakage current through a spinel layer was measured as less than 2×10^{-12} amperes/square centimeter.

Sharp Corp. has developed a 400-V diffused self-aligned MOS IC for driving electroluminescent displays. Housed in a 42-pin plastic dual in-line package, the 224-by-134-mil (5.7-by-3.4-mm) chip includes low-voltage logic and 32 high-voltage output transistors. The device improves its breakdown characteristics over those of previous MOS high-voltage ICs through the use of multilayer conductive and floating field plates that reduce its electric-field enhancement. It operates from a single 5-V supply, is TTL-compatible, and has an on drain current of 50 milliamperes. The drain-source on resistance is 500 Ω.

Stretching the microwave limits

Two complete microwave device sessions at this year's conference attest to the growing importance of this technology, as higher frequencies at yet higher power levels are reached.

An amplifier that operates over the K band (10.90 to 36.0 GHz), from Texas Instruments Inc., Dallas, relies on gallium arsenide power FETs to obtain an output of 675 mW, a gain of 5.8 dB, and an efficiency of 18% at 20.5 GHz. Even at frequencies as high as 25 GHz, gain is still an impressive 200 mW, with an efficiency of 6.3%. The 0.3-by-1.5-by-0.1-mm FETs have single, 1.35-mm gate stripes with multiple gate pads.

Researchers at Thomson-CSF in Orsay, France, put commercially available FETs to work in a three-stage single-ended amplifier to achieve 12 dB of flat gain and a voltage standing-wave ratio of less than 2.5 over a broad frequency range of 150 MHz to 16 GHz. The FETs, with 0.5-μm gates, are self-biased and yield an amplifier noise figure of 8.5 dB (from 1 to 12.4 GHz). The researchers employed computer-optimization techniques for second-order matching circuits without feedback to implement their design. No transformer or distributed circuit elements—components common to conventional broadband amplifier designs—are used.

To solve the problem of high S/N ratios in fast photodetectors, Sony researchers combine a p-i-n photodiode and a monolithic preamplifier. The result: a 30-MHz bandwidth and detectivity of 1.53×10^{11} cm-Hz$^{1/2}$/W at 10 MHz. According to the company, such detectivity is at least 12 dB better than that of the best photodetector at present on the market.

The preamplifier chip is configured with a common-emitter input (Fig. 2). The device exhibits an equivalent noise power (at a wavelength of 950 nanometers) of 5.35×10^{-12} W/Hz$^{1/2}$ at 30 MHz and 4.01×10^{-12} W/Hz$^{1/2}$ at 20 MHz. □

16-K EE-PROM keeps MNOS in the running

2-K-by-8-bit electrically erasable programmable read-only memory uses metal-nitride-oxide-semiconductor process to vie with floating-gate devices

by Kyotake Uchiumi and Tsugio Makimoto
Musashi Works, Hitachi Ltd., Kodaira, Tokyo, Japan

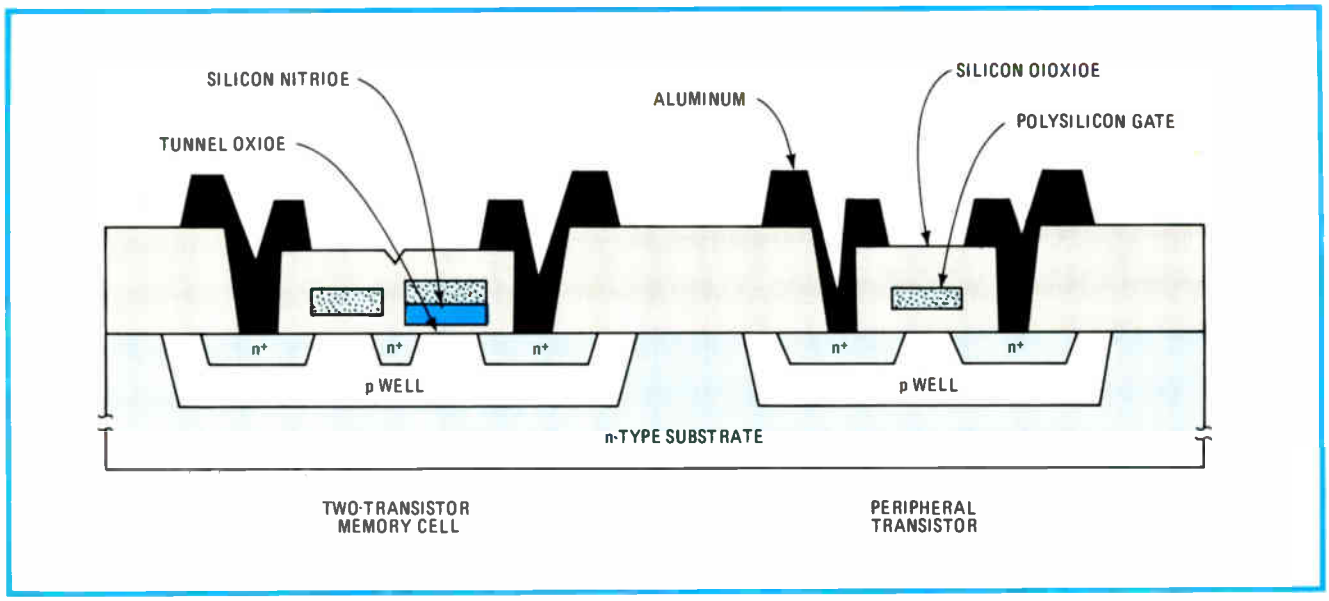
☐ Electrically erasable PROMs have come a long way in the last two years, from storing only hundreds of bits to storing tens of thousands. That puts them only a generation behind the less convenient E-PROMs, programmable read-only memories that are erasable by ultraviolet light. It also makes them strong candidates for use in microprocessor-based systems, with all that implies by way of an explosion of applications.

The newest EE-PROM updates the oldest EE-PROM technology—the metal-nitride-oxide-semiconductor, or MNOS, approach. Designated the HN48016, it achieves the same 16-K density as the more novel floating-gate type [*Electronics*, Feb. 28, 1980, p. 113]. Like other MNOS devices, it can be written into and erased 1,000 times. Yet with a typical access time of 250 nanoseconds, it no longer suffers from their moderate speed. Also unlike other MNOS EE-PROMs, it does not become harder to read the longer it is in use.

To enhance its performance, the 48016 substitutes polysilicon gates for the metal gates denoted by the M in MNOS. (Still, it is expedient to retain its MNOS classification.) Also for the sake of speed, the EE-PROM uses n-channel instead of p-channel MNOS storage devices. The third important change in the MNOS process is an adjustment to the threshold voltage of the memory cell that ends what is called the read-disturb problem.

As the memory can be read with a single 5-volt supply and as all its input/output pins are TTL-compatible, designers can put together boards and systems without having to incorporate other power sources or add level-shifting circuitry. The long list of the memory's potential applications includes:

- Controllers and microprocessor and microcomputer systems, for nonvolatile program and data storage.
- Cash registers and bank and point-of-sale terminals, for keeping track of running totals.
- Private telephone systems, for interpreting messages and mapping routes.
- Test and measurement instruments, for updating cali-



1. All n-MOS. The high-density electrically erasable programmable read-only memory gains speed by using an n-channel in place of the older p-MOS process. The compact memory cell, on the left, shares a source-drain implant between a selection device and a storage transistor.

bration data to keep pace with aging components.

- Systems that need to preserve hysteresis.

In any MNOS device, the application of a programming voltage alters the contents of the memory by forcing carriers to tunnel to or from the cells through an extremely thin layer of silicon dioxide. The n-channel version of such a memory behaves no differently.

Basic to it is an n-type (100) silicon wafer in which separate p-type wells are formed for the memory cells and peripheral transistors (Fig. 1). The first layer of polysilicon creates the gates of the non-MNOS transistors, including the switching device in the memory cell. A 500-angstrom-thick layer of silicon nitride topped by a second layer of polysilicon creates the gates of the MNOS storage devices. This polysilicon-nitride sandwich is separated from the substrate by a 20-Å-thick tunnel oxide.

Finally, the source and drain regions of all the transistors are implanted, with the gate serving to align the implantation. The implants are annealed at a relatively low temperature in a hydrogen atmosphere. High temperatures are avoided because they would degrade the MNOS gates. The hydrogen improves the memory's ability to retain data.

Do not disturb

The n-channel MNOS transistors in this design can be read a virtually unlimited number of times, unlike their p-channel predecessors. Figure 2 explains why. To distinguish logical 0 from 1 states in a p-type MNOS device, a gate voltage of about −7 V is required. This negative potential attracts positive carriers and ions, forming trapping centers in the gate region that eventually upset the device's threshold voltage. In contrast, the on and off states of the n-channel transistor have been deliberately shifted so that they can be distinguished by a gate voltage of 0 V. Consequently, the n-MNOS device is free from read-cycle limitations.

A schematic of a portion of the memory matrix is given in Fig. 3. Because the transistors employ silicon gates, the array can use low-resistance aluminum for its bit lines. During a read cycle, both the source and gate regions of the MNOS devices are grounded, so that the switching transistor gates are the sole contributors to word-line capacitance—in fact, word-line capacitance is about one quarter that of arrays using conventional aluminum-gate cells. The two factors translate into a significantly shorter access time.

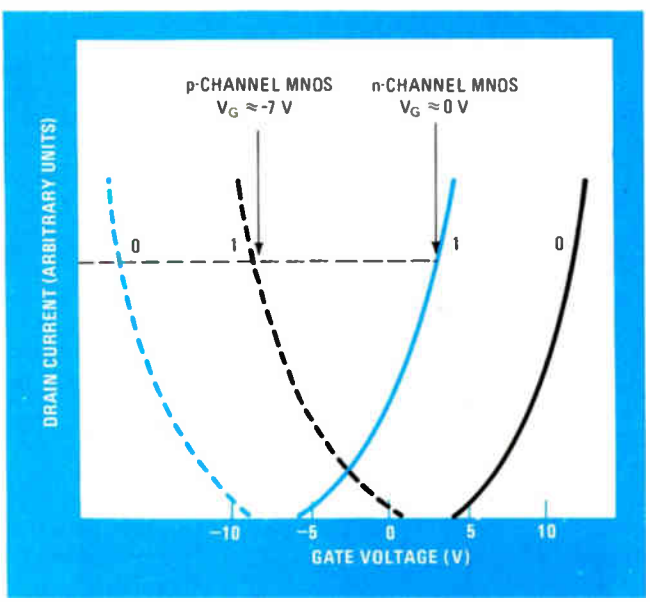
As Fig. 1 indicated, each memory cell consists of a conventional MOS switching transistor in series with an MNOS storage device. But because the two transistors share a p-well and a source-drain region, they occupy only 400 square micrometers, or less area than a comparable, double-device p-channel memory cell. As a result, the entire 16-K EE-PROM fits on a die measuring 4.46 by 4.16 millimeters, or 28,758 square mils. Some 16-K E-PROMs are larger, despite having only a single device in each of their cells.

Dual storage areas

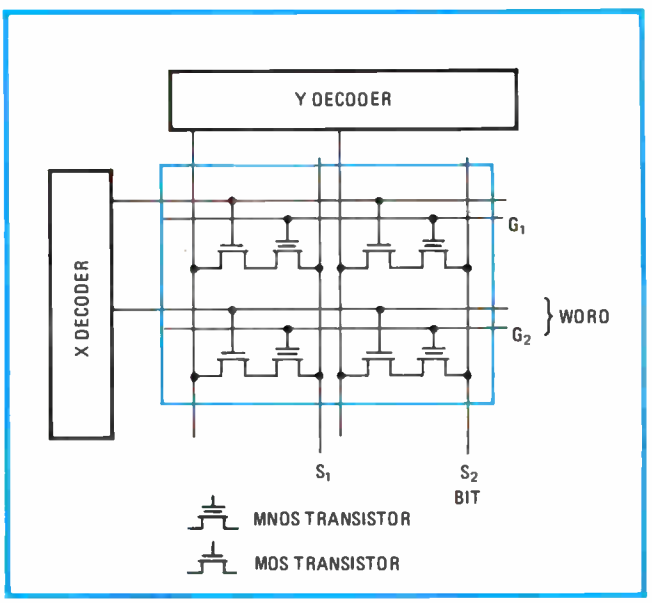
The die is organized into two 8-K storage areas, separated by the X, or word-line, decoder (Fig. 4). At one end of the two sectors lie the Y, or bit-line, decoder and gating circuits. Eight sense amplifiers and input/output buffers, 10 address buffers, and various bit-erasing elements make up the rest of the peripheral circuitry.

The chip is mounted in a 24-pin plastic dual in-line package for compatibility with standard 16-K E-PROMs. The only difference is that instead of a chip-enable ($\overline{CE}$) signal, pin 18 accepts a necessary programming pulse, PGM. And, of course, provision had to be made for electrical erasure in lieu of ultraviolet light. The table lists the various modes of the device, including erasure.

When being read, the 48016 becomes active only when both the chip-select ($\overline{CS}$) and PGM signals are low. In



2. Shifted shift. In older, p-channel metal-nitride-oxide-semiconductor devices, logical states are detected by high negative voltages that create positive trapping centers and thus give rise to the read-disturb problem, as it is called. N-type devices are free from this upset.



3. Mini matrix. Since the storage transistors have silicon gates, low-impedance aluminum can be used for bit lines. Word-line capacitance is also reduced because the source and gate regions are grounded during reading. The result: a shorter access time.

OPERATING MODES OF 16-K ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY

Memory mode \ Pin function and number	Programming pulse, PGM	Chip-select (CS) signal	Programming voltage, V_{PP} (V)	Supply voltage V_{CC} (V)	Output
Read	V_{IL}	V_{IL}	5	5	data out
Deselect	don't care	V_{IH}	5	5	high impedance
Program	pulsed V_{IL} to V_{IH}	V_{IH}	25	5	data in
Program verify	V_{IL}	V_{IL}	25	5	data out
Erase	pulsed V_{IL} to V_{IH}	V_{IL}	25	5	

Note: V_{IL} = input voltage, low; V_{IH} = input voltage, high

other words, it behaves like a fully static device, as do ultraviolet-light–erasable PROMs. Although it lacks the E-PROM's automatic power-down mode, it does dissipate less power than a standard 16-K E-PROM in the read mode—typically 180 milliwatts.

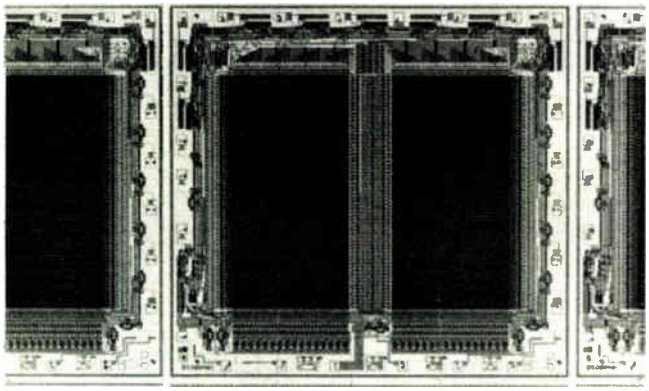
The chip has the same programming waveforms as an E-PROM and also allows the user to verify what has been written. The programmed data can be confirmed on the data pins by holding the address lines stable while bringing the $\overline{CE}$ and PGM signals low.

The 48016—like an E-PROM—cannot be erased a byte at a time. But the time it takes to write a byte of data is slashed to 10 milliseconds. The entire 2-K bytes of memory can be programmed in only 20 seconds, compared to the 100 seconds or more required for today's E-PROMs.

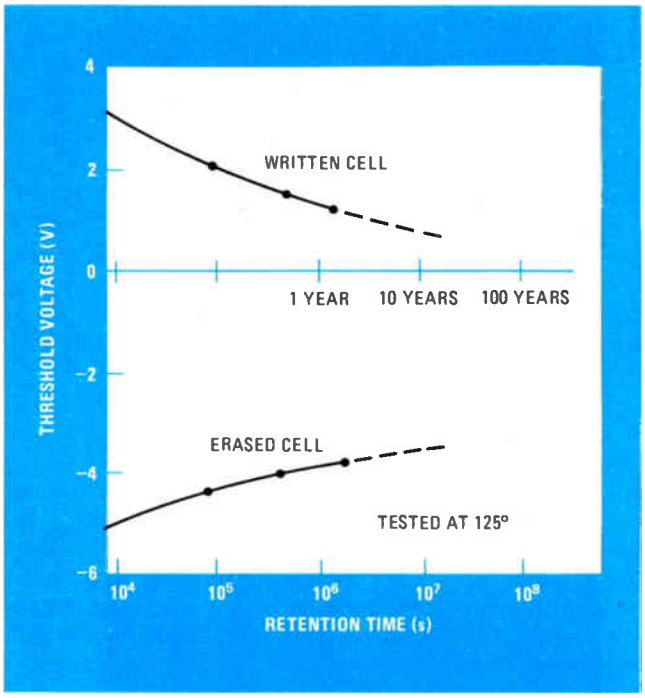
Erasure also takes less time than for a 16-K E-PROM. It is done in a way that deviates minimally from E-PROM operations. With $\overline{CS}$ low and PGM high, a single 1-s 25-V pulse on the V_{PP} pin clears all storage cells to a logical 1.

The typical access time of the 48016 is 250 ns, even if V_{CC} is lowered to 3.5 V at 25°C. An elevated ambient temperature degrades the memory's electrical characteristics, but at 70°C, the maximum access time is still only 300 ns. Even when wafer-processing variations cause, worst-case threshold voltages, polysilicon thicknesses, and so forth, the maximum access time of the device is 350 ns for V_{CC} = 5 V ±5% in the temperature range of 0° to 70°C.

All large-scale integrated MOS memories must be



4. Two times 8 K. The MNOS chip has two 8-K storage areas that are separated by the word-line decoders. The bit-line decoders are at one end of the chip, and the rest serves I/O functions.



5. Retention characteristics. With time, the threshold voltage of both written and erased cells nears the 0-volt sensing potential. However, these curves show that it will take more than 10 years for a written cell to fail and even longer for an unwritten cell.

tested for valid operation and data retention at high and low voltages and at high humidity, and they must also pass mechanical stress checks. In addition, MNOS memories must pass tests related specifically to their unique storage mechanism. Thus, their ability to endure repeated write and erase cycles must be verified. Also, any read cycle limitations must be observed—none, of course, in the case of the HN48016.

Long-lasting

As for endurance, the EE-PROM can be written and erased more than 1,000 times before those processes irreversibly alter the threshold voltage and channel conductance of its memory cells. There is a gradual buildup of carriers in the gate oxide very near the oxide-silicon interface, for each time the cell is programmed and discharged, slightly more carriers are trapped than released. Eventually, when the threshold voltage of an unwritten cell crosses the sensing level, the device fails.

The upper curve in Fig. 5 shows the threshold shift in a written cell, while the lower curve applies to an erased cell. When extrapolated, these curves indicate it will be more than 10 years before a written cell's potential crosses 0 V—the point at which it becomes impossible to read. The threshold voltage for an erased cell takes a much longer time to pass through 0 V, but this only means that worst-case data-retention characteristics must be inferred from a written cell.

Moreover, when 16,384 cells are integrated onto a single chip—as they are in the 48016—the poorest bit determines the reliability of the product. Owing to uniform processing, the 48016 should retain data longer than 10 years with junction temperatures of 85°C. □

Fast on-chip memory extends 16-bit family's reach

When stored on the same chip as the microprocessor, frequently used routines will execute faster

by David S. Laffitte and Karl M. Guttag, *Texas Instruments Inc., Houston, Texas*

☐ In the years ahead, advances in very large-scale integration will either sink the systems designed today around current microprocessors—or bear them triumphantly into new application areas. To succeed, today's systems must be capable of stretching to accommodate increasingly fast and powerful VLSI chips as and when they arrive.

A new generation of 16-bit microprocessors under development at Texas Instruments is being designed to form the core of such evolutionary VLSI systems. The TMS 99000 series will, in addition, carry forward already existing designs based on the TMS 9900 family of microprocessors, microcomputers, and support chips, updating the 9900 architecture while retaining software compatibility with their predecessors.

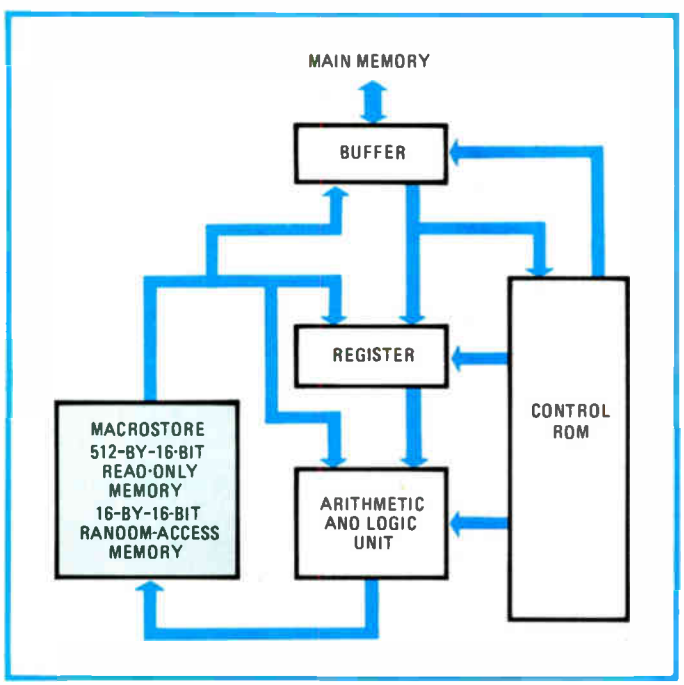
The microprocessors in the 99000 series will employ the strip chip architectural topology first used extensively for the TMS 7000 8-bit microcomputers [*Electronics*, Jan. 27, 1981, p. 107]. Also their greatly optimized microcode, as well as instruction prefetching, will speed program execution. But perhaps their most distinctive feature will be what TI calls the Macrostore.

The Macrostore is a high-speed memory that can be addressed independently of main memory. Once a function has been placed in the Macrostore, it can be executed much faster than when located in the main system memory. Macrostore functions will be coded in assembly language but derive the speed with which they are executed from the faster on-chip memory—as little as 167 nanoseconds will be needed for each memory cycle.

The Macrostore memory occupies 64-K bytes, some of them on chip and the rest located off chip in fast random-access or read-only memories. It is designed specifically for frequently used operating system functions and for real-time functions that can be stored in firmware. Initially, the on-chip part of the Macrostore will consist of a 1-K-byte read-only memory, plus a 32-byte random-access memory that will serve as a high-speed register set (Fig. 1).

It will also be possible to use the Macrostore as a waystation to even higher performance by implementing the same functions in what TI is calling attached processors. Several standard functions will be offered in both the Macrostore and attached processors.

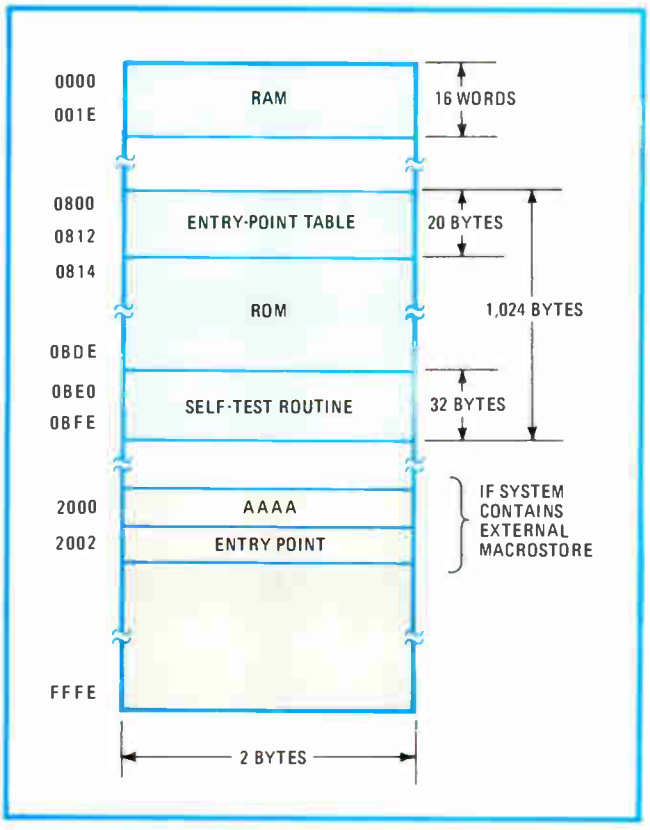
Users of the 99000 family will follow a design cycle in which the first step will be to emulate the desired function in normal memory. Once the program was debugged and verified, a production run could be scheduled to commit the program to the ROM portion of the Macrostore either on a 99000 processor itself or externally in a separate package. Alternatively, greater performance will be obtainable if the Macrostore is replaced by a dedicated attached processor.



1. The Macrostore. Standard 99000 microprocessors will contain a separate on-chip address space called the Macrostore. Often used or time-critical routines can be stored there and will execute up to twice as fast as the same routines when they are kept in main system memory.

TI plans to offer several standard solutions to common processing problems in specialized Macrostore ROMs. The 99110 will contain high-performance floating-point routines, and the 99120 will contain the kernel of TI's Real-time Executive, which supports the operating system of Microprocessor Pascal.

When operating in its standard mode, a 99000 processor will directly execute the op codes it has



2. Address map. The separate Macrostore address space uses the lowest 32 bytes as RAM locations that will ordinarily act as a high-speed register set. Programs may be kept in the ROM area with an entry point table indicating the starting address of each one.

in common with the 9900 series of devices as well as its new instructions. But when it recognizes an op code that is not defined, the Macrostore will become active. In this situation, the 99000 processor uses the same macroinstruction detection (MID) mechanism as the 9995 processor [*Electronics*, Dec. 18, 1980, p. 91].

Upon encountering an MID op code in the user's program in main memory, it will first interrogate its bus to determine if an attached processor is present to service the request. If none is present, it will check the on-chip Macrostore, and if that does not contain the routine, it will check the external Macrostore. If that search, too, should fail, it will trap to interrupt for conventional software emulation or illegal op-code error detection. Otherwise, it carries out a number of actions in the Macrostore.

Inside the Macrostore

First, the 99000 searches the entry point table in the on-chip Macrostore ROM to find the starting address of the appropriate routine. If found, it makes a context switch similar to a 9900's. The speed of this operation—a minimum of 14 machine states or 2.33 microseconds—has long been one of the hallmarks of TI microprocessors. Once the return address, or program counter (PC), the workspace pointer (WP), and the status register (ST) have been stored in the last three locations of the on-chip RAM, control is transferred to the Macrostore routine. Upon completion of the function, another context switch returns control to the calling program in main memory.

The 99000 complete Macrostore address space is shown in Fig. 2, with the off-chip portion located above 2000_{16}. The first 32 bytes are high-speed RAM and are normally used to hold the 16 general-purpose 16-bit registers. The work-space register set may alternatively be located in off chip RAM, which must be fast if the high-speed edge is not to be lost.

Next, starting at 800_{16}, come 1,024 bytes of on-chip ROM. The Macrostore routines in this ROM are entered via an entry-point table that stores the address of each.

Normally, accesses to the Macrostore, whether on or off chip, will take place within a single machine cycle (167 ns with a 6-megahertz four-phase clock). However, users will be able to add external memory with longer access times very simply, by using the ready line to insert wait states.

There is no need for the main memory to be homogeneous. Fast bipolar chips may be used for time-critical segments, and less exacting routines may be located in cheaper, slower memories. That memory partitioning will enable systems designers to trade off speed for cost and the lower power consumption of MOS memories.

It is unnecessary to have large amounts of high-speed memory in order to take advantage of the 990000's high throughput. If frequently used sections of code are stored in fast memory, the average execution time of programs can be significantly reduced. It should be noted that relatively small caches, on the order of 512 words, can have 90% or higher hit ratios—the percentage of memory requests for information located in the cache. (Of the microprocessors in Table 2, only the 99000 is designed to exploit fast cache memories.)

The prototyping mode

Before committing to the large production runs necessary to mask-program the Macrostore ROM, a user will be able to emulate and debug that operation in a special prototyping mode. In this mode, external RAM and/or ROM replaces the internal memory. The same mode may even be used to start low-volume production, giving way to the on-chip ROM only when the volume demand makes that option cost-effective.

The prototyping mode is a pin-programmable function that maps the lower Macrostore ROM locations into an off-chip memory of the user's choice. In this way users will be able to experiment inexpensively with the 99000 processor to evolve custom forms that are particularly suited to their applications by only adding ROM—since the high-speed on-chip RAM is still available.

Other improvements

Figure 3 is a block diagram of the microprocessors in the 99000 family. Strip chip architectural topology (SCAT) lines up all register and memory elements in strips and passes all control and data interconnections over them, saving silicon and shrinking die size. Such a design gives the 99000 series a radically different die layout from the 9900 series.

Still, the processors in the new series will use the same 69 instructions as those in the old series, adding several new ones to bring the total to 85. The 4 operations that

TABLE 1: STEPS IN MICROINSTRUCTION SEQUENCE

STEP NO.	OPERATION	STATE COUNT	MEMORY CYCLE	INTERNAL FUNCTION
1.	FETCH INSTRUCTION	4	FETCH INSTRUCTION	PROCESS PREVIOUS OPERANDS
2.	DECODE INSTRUCTION	1	WRITE RESULTS	DECODE INSTRUCTION
3.	FETCH SOURCE OPERAND	2	FETCH SOURCE	
4.	FETCH DESTINATION OPERAND	3	FETCH DESTINATION	
5.	PROCESS THE OPERANDS	4	FETCH NEXT INSTRUCTION	ADD OPERANDS
6.	STORE THE RESULTS	1	WRITE RESULTS	DECODE INSTRUCTION

were added to the 9995, including signed multiplication and division, are employed, but 12 others are completely new to the 99000.

Included in the 12 are 4 32-bit operations that can streamline floating-point routines: shift left, shift right, add, and subtract. There are also 3 new bit-manipulation instructions to set, clear, and test specified bits in the main memory space. Two stack manipulation instructions allow the 99000 to conveniently push and pop multiple stacks that can be located anywhere in memory. The remaining 3 new instructions are dedicated to communicating with the 74610 memory mapper, which expands the basic 64-K-byte address space to 16 megabytes using a segmentation methodology.

Besides the high speed of Macrostore accesses, a 99000 processor will use several other techniques for faster execution speeds. Whenever possible, op codes and operands are prefetched from memory while the processor is working internally.

Smarter pipelining

Unlike some other prefetching 16-bit processors, the 99000s will have some intelligence built into this pipelining process. For instance, branch instructions are often troublesome to a prefetching scheme since the next instruction need not come from the next location in physical memory. On 99000 processors, however, the microcode that executes all branch and jump instructions will inform the prefetching unit of the true next instruction location. In fact, only an interrupt will be able to cause the prefetcher to discard a prefetched item.

The prefetching scheme overlaps two successive bus cycles whenever possible, eliminating the time required to fetch an op code. For example, precessing an instruction to add involves the sequence of six steps outlined in Table 1. The prefetch mechanism recognizes that, while operands are being added (step 5), the memory bus is inactive and therefore can be used to prefetch the next instruction's op code. Then while the result of the current instruction is being stored, the prefetched op code is decoded. Thus all six steps are performed by the processor in only four machine cycles since in the first and fourth states both an internal operation and a memory bus transfer are made.

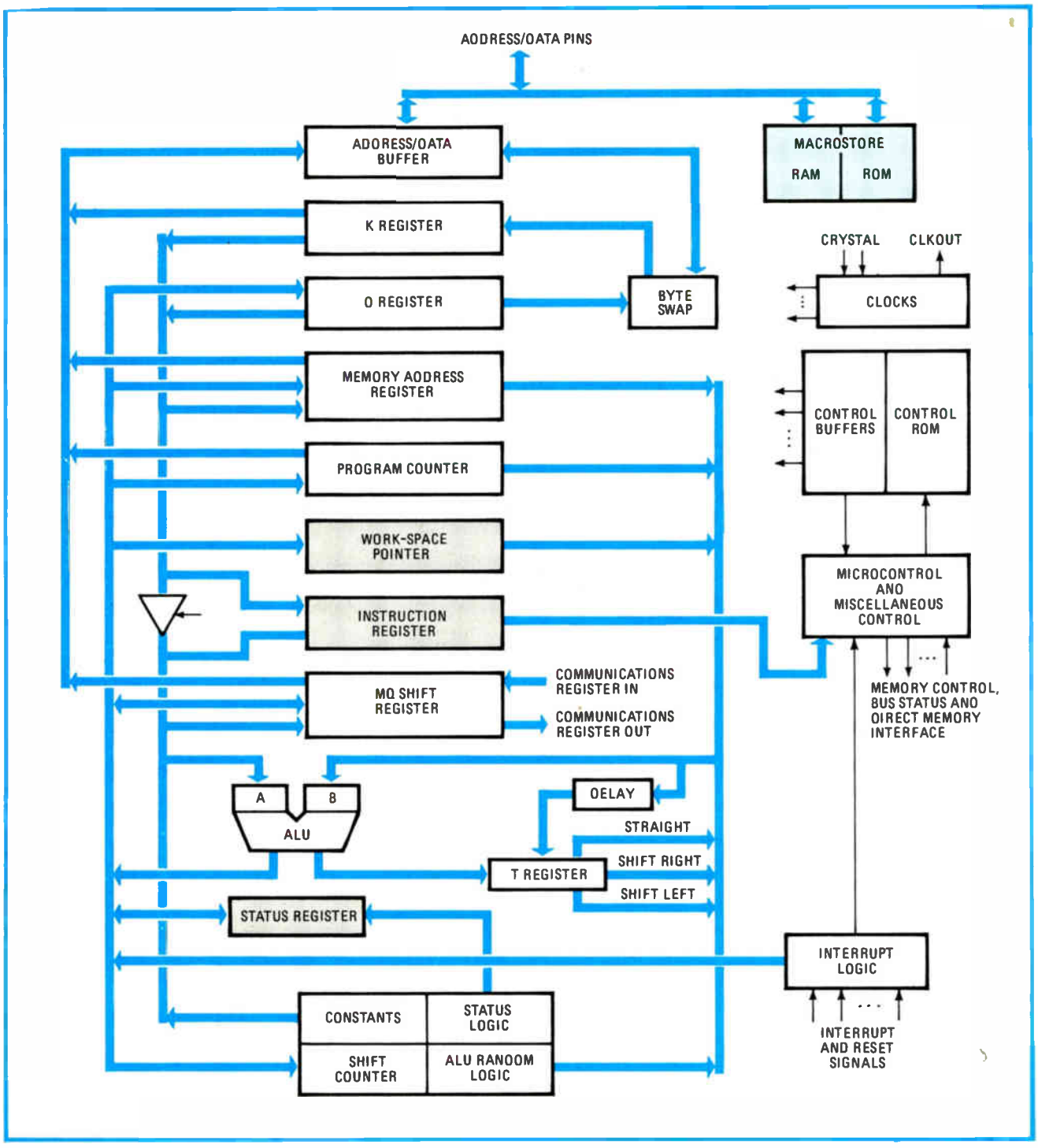
Microprogrammed

Microcode in a separate control ROM defines the operations that must be performed in order to execute each assembly-language instruction. The microinstructions specify the control signal states that manage the processor's arithmetic and logic unit, its internal registers, and its input/output operations. Each microinstruction is active for one machine cycle, or four cycles of the input clock. In fact, a microprogrammed processor is something like a computer within a computer. The smaller one consists of the microcode itself plus the mechanisms that apply a sequence of microinstructions to the control lines themselves. The length of time that a microinstruction remains active depends on the frequency of the processor's clock. For example, each microinstruction would last 167 ns for a 24-MHz input clock from which a four-phase, 6-MHz internal clock is derived.

Several microinstructions will be needed to execute a

TABLE 2: MACHINE CYCLES NEEDED BY 99000 AND OTHER MICROPROCESSORS TO EXECUTE TYPICAL INSTRUCTIONS

Instruction and addressing modes \ Microprocessor	99000	68000	8086	Z8000
Move register to register	3	2	2	3
Move memory to memory	5	10	29	20
Move register to register, indirectly autoincrementing each	9	6	18	20
Add register to register	4	2	3	4
Add memory to register	5	6	15	9
Jump relative	3	5	16	6
Signed multiply register to register	25	35	128 to 154	70
Signed divide register to register	34	79	165 to 184	95



3. Internal architecture. Like its predecessor, the 99000 does not rely on an internal register set, but allows access only to the program counter, status register, and workspace pointer. The last of these indicates where in main memory the 16 contiguous registers are located.

single assembly-language instruction, and TI will make available a table listing the number of machine cycles and memory accesses needed for each 99000 family instruction. The total execution time, T, for any instruction may be computed from:

$$T = t_c(C + WM)$$

where

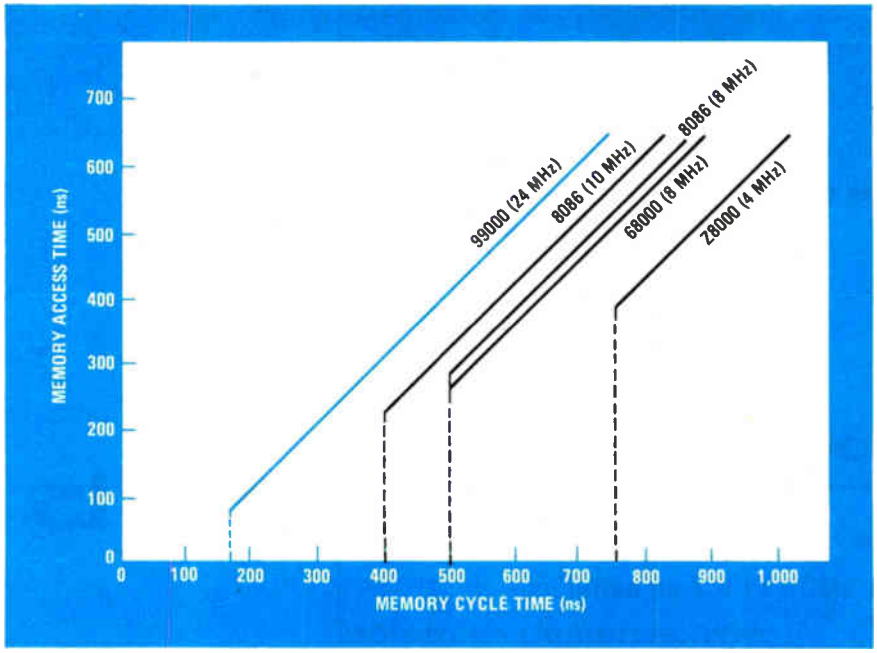
t_c = the machine cycle time

C = the number of machine states needed to execute the instruction and modify the associated addresses

W = the number of wait states per memory access

M = the number of memory accesses.

For example, when memory is accessed without wait states and both operands are in work-space registers, executing a move instruction (MOV) could take as little as 500 ns in a system operating at the maximum design clock frequency of 24 MHz. This would yield a 167-ns



4. Cycling efficiently. The 99000 will accommodate a range of memory speeds as determined by processor clock rate and number of wait states. Some values are projected in this graph.

machine cycle time with C = 3, W = 0 and M = 3 in the above equation. Working with a slower memory that requires two wait states will prolong the execution time to 9 t_c intervals (C = 3, W = 2, M = 3). Addressing the source operand symbolically, with the same two wait states required, raises the execution time by another 3 t_c (C = 3+1, W = 2, M = 3+1).

The control ROM itself uses the code-compression techniques developed for all new 16-bit TI processors. The result is a faster-acting, denser ROM that interprets assembly-language instructions using a microcoded control word of over 150 outputs. These microinstructions, which are among the widest in the industry, are largely responsible for the high efficiency of the device—very few machine cycles are needed for it to do the commonest assembly-language instructions. The reason is that more operations can be done in parallel when a wide microinstruction is used. Each separate internal bus can be transferring a different 16-bit word for each machine cycle. Architectures that use fewer internal buses and microinstructions that are not so wide will require significantly more machine cycles for each assembly-language instruction. Table 2 compares several microprocessors for their efficiency in this respect. The execution speeds depend upon the length of the machine cycle for each microprocessor listed.

Cycling efficiently

The relationship between the memory access time—the time needed to fetch data from a memory location—and the memory cycle time—the time from the start of one memory cycle to the start of the next—is the factor limiting efficient use of memory. Generally, the memory access time is determined by the memory subsystem itself, while the cycle time is adjusted to fit.

Two methods are used to extend a microprocessor's memory cycle: either wait states can be added to the access portion of the cycles or the clock frequency can be adjusted to the processor. The curves in Fig. 4 show the average relationship between access and cycle time for a range of wait states and clock frequency adjustment.

There are two important points to notice in Fig. 4. First, for a given memory access time, the memory cycle time can be shorter for the 99000 than for the other microprocessors. Secondly, the shortest 99000 cycle time will be over twice as fast as the other processors'. The first is due to an efficient memory interface, enabling the 99000 to operate faster with less expensive, slow memories. The second point indicates the 99000 will be able to make full use of fast memories.

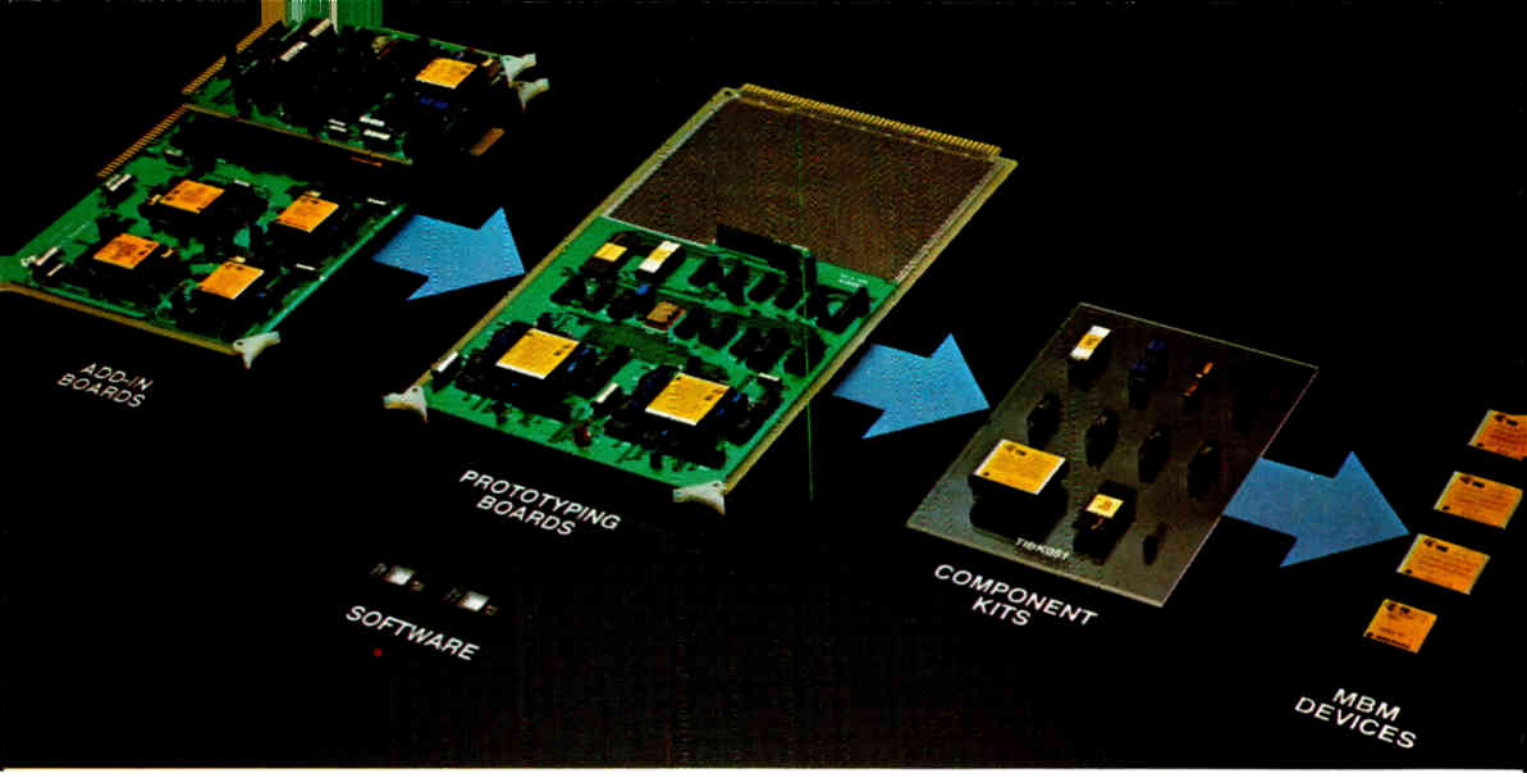
Future versions

Many specialized versions of the 99000 architecture will be built in the coming years. They will offer the system designer a totally modular solution to his microprocessor application.

Three processors will pioneer the series:

- The 99105 is a part that will bridge the gap between current 9995 applications and future 99000 ones. The instruction set of the 99105 will be identical to the 9995's, and the 99105 device will be pin-compatible with the other 99000 family members, but it will not contain a Macrostore.
- The 99110 will be the family's standard processor for number-intensive applications since it will have the ability to do a floating-point arithmetic in its on-chip Macrostore. This part will not only free the programmer from the need to write floating-point routines but will also reduce the time needed to the execute those functions.
- The 99120 will be the standard processor for applications requiring intensive use of TI's Micropascal system function. Its on-chip Macrostore will contain the kernel of TI's Real-time Executive.

All 99000 devices will initially employ the scaled n-channel MOS technology called SMOS and use 3-micrometer or less design rules. They will be supplied in 40-pin packages that multiplex the data and address lines and will operate off a single 5-V supply. □



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Mode scrambling can enhance fiber-optic system performance

To increase bandwidth and decrease attenuation, designers may use this little-known variation in light's electromagnetic field

by Steven L. Storozum, *McDonnell Aircraft Co. St. Louis, Mo.*

☐ The optical fiber phenomenon known as mode scrambling can be a real mischief maker in data transmission if systems designers choose to ignore it. But if the effect—which alters the electromagnetic fields through which light waves propagate—is understood, it can be controlled and even beneficial.

Scrambled transmission modes may account for increases in fiber-optic bandwidth and for unusual cable attenuation. If unrecognized and uncontrolled, such effects hinder repeatable results when low-loss, wideband, multimode optical fibers are configured into systems. They also have an impact on system performance after splicing of the fibers, where bandwidth increases with the number of splices per unit cable length. And they help explain how static and dynamic tension placed on the fibers during system installation affect bandwidth and attenuation.

Applying the research

The phenomenon, which has been exhaustively studied in laboratories, has received minimal attention from the fiber-optic user community. But a knowledge of its practical applications to system design and characterization can boost performance. In certain cases, for example, the increased bandwidth that is induced by mode scrambling can be used to advantage to expand system data rate beyond what the data sheet indicates for the fiber's normal bandwidth.

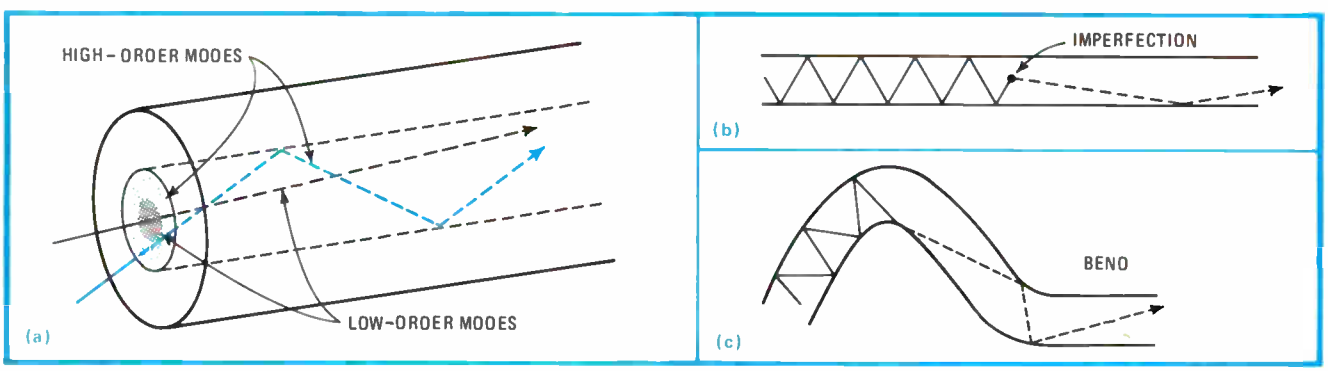
Also important for the designer, scrambler designs to enhance performance can be either installed initially or retrofitted into an existing system. In addition, attenuation and bandwidth measurements may be standardized by taking the effect into account.

A transmission mode is a way of characterizing propagating guided waves by a particular electromagnetic field pattern. In a high-order mode, light rays travel the length of the fiber as they ricochet around at a high angle in the fiber core on a per-unit-length basis. Rays in a low-order mode do the opposite, following a path close to the core's center.

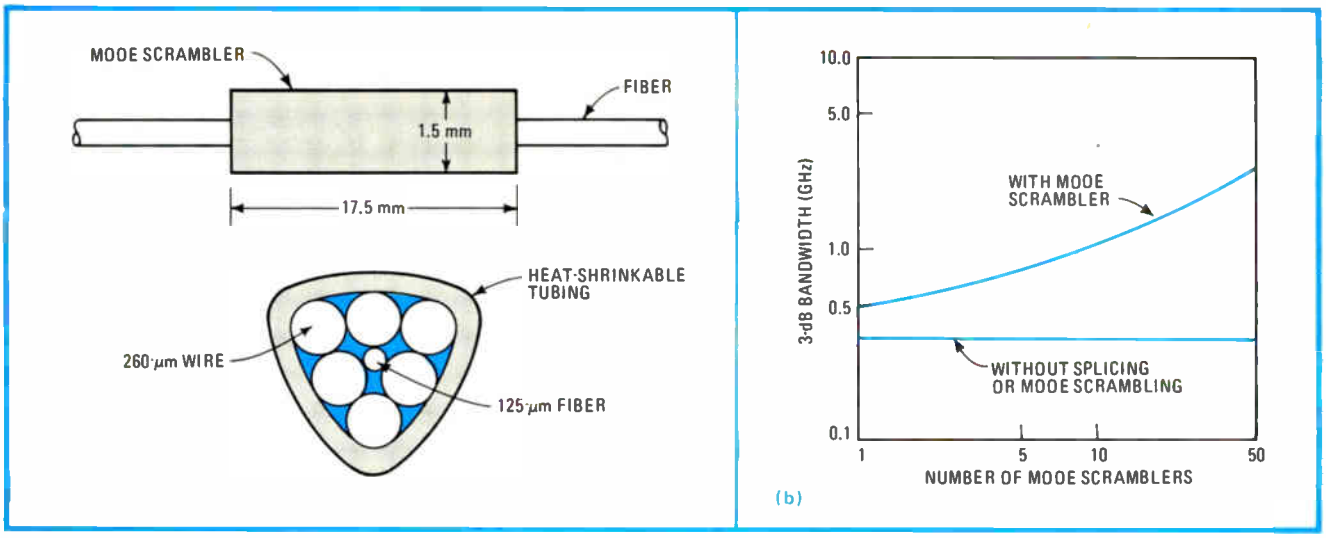
For example, in a typical optical fiber construction of cladding over core (Fig. 1a), high- and low-order transmission modes exist together. The difference in the times it takes light rays to traverse the fiber in high- and low-order modes is the primary cause of signal distortion in multimode optical fibers.

Graded-index fiber, which has denser glass at its core to slow down rays in the low-order modes, is used to correct that situation. This fiber is effective in equalizing signal transit times and alleviating intermodal distortion. But signal distortion is not the only problem; the mixing and switching of optical power between modes creates other performance difficulties.

Optical fibers are not flawlessly long and straight. Mode scrambling can take place whenever a light ray hits an imperfection in the core (Fig. 1b) or a curve at the core-cladding interface (Fig. 1c). These imperfections and bends are created during cable manufacture, splicing, and installation. The imperfections refract the light, shifting its angle or propagation mode. Bends in the fiber compress one edge of the core, slightly altering the light ray's propagation path. This change of direction



1. Lots of modes. The normal fiber-optic cable with core and cladding has both low- and high-order propagation modes (a). Scrambling of these modes can occur either at imperfections (b) or at bends (c). The fiber's attenuation then may vary in some unpredictable way.



2. Scrambler design. If 10-km fiber is squeezed by six wires in heat-shrinkable tubing of the proper length (a), its 3-dB bandwidth increases considerably (b) as a function of the number of scramblers used. Periodic scramblers thus change information-carrying capability.

transfers power between modes, which has an impact—good or bad—on system performance.

In fact, in terms of the pulse-broadening that occurs as pulses propagate, real fibers exhibiting mode scrambling have better characteristics—or less broadening—than those computed for an ideal step-index fiber. The computed pulse broadening for an ideal step-index fiber can be expressed as $T_i = (n_1 - n_2)L/c$, where n_1 is the core refractive index, n_2 is the cladding index, L is the fiber length, c is the velocity of light in free space, and T_i is measured in seconds.

Coupled modes

A real fiber's pulse broadening can be given as $\tau_r = (n_1 - n_2)(Ll)^{1/2}/c$ where l is the mode-coupling length. This characteristic length is inversely proportional to the mode-to-mode coupling coefficient.

The mode-coupling length has been computed theoretically for certain optical fibers and has been found to be on the order of 1 to 4 km. But in reality it is generally less than this, though normally more than 150 meters.

Because pulse broadening for actual fibers is less than that computed for the ideal fiber, fiber bandwidth can be improved with mode scrambling.

One design objective in an actual fiber-optic cable is to minimize sharp microscopic bending of the fiber during fabrication. This microbending, as it is called, causes mode scrambling that can even couple light out of the fiber under certain circumstances, increasing attenuation. Manufacturers have developed special techniques to reduce microbending. In fact, these efforts have resulted in one of the more heated debates among fiber-optics users to date—over the loose tube versus tight buffer method.

With loose tube cables, lacquer-coated optical fibers are threaded inside hard plastic tubes, with only one fiber per tube. The fiber's bend radius is thus constrained by the tube's bend radius, and microbending is therefore averted.

Tight buffer fibers are coated first with soft rubber (usually room-temperature vulcanizing silicone rubber, a substance similar to rubber cement) and then with a harder plastic such as DuPont Hytrel. Thus, the fiber floats in a bath of soft rubber that buffers it from any sharp bending of the outer plastic coating during cable manufacture or cable installation. Both types of jacketing alleviate microbending and mode-scrambling losses.

These buffers work so well that some systems have even seen cable losses begin to decrease after a cable has been in place for a few months. This happens because residual microbends induced during insertion of the fiber into the cable and cable installation iron themselves out as a fiber gradually moves within its buffering to a spot where it is under minimal mechanical tension. As microbending goes down, low-order modes are not scrambled as severely into high-order modes and the fiber's loss decreases. One example is an experiment at ITT's Electro-Optical Products division in Roanoke, Va., where a multifiber optical cable suspended between telephone poles decreased in loss by 0.25 decibel during the nine-month recording period. This was independent of temperature variation from 20° to 80° F.

Small but significant

One quarter of a decibel may not seem to be much, but with ever-decreasing cable losses, even small amounts of fiber loss that are not accounted for may downgrade system performance. Even with commercial fibers having losses as low as 3 dB per kilometer at 850 nanometers, a 0.25-dB variation over 1 km would amount to an 8% fluctuation in received optical power. Such a fluctuation would have an impact on the operation of certain optical data buses. Additionally, with optical connector losses decreasing to the 0.25-to-0.5-dB level and splice losses shrinking to 0.1 dB, a 0.25-dB decrease may let an extra connector or couple of splices be accommodated in an optical system with a tight power budget. The system designer must carefully determine when he must be concerned with these effects. They are small but in the aggregate can cause trouble.

There is no comprehensive theory available to quantify the microbending effect, but unless a fiber-optic sys-

tem has been designed in which the optical receiver is so near saturation that a decrease in fiber loss will saturate it, a detailed analysis is not needed for most system designs. Only a decibel or so need be allowed for in the designer's power budget for cable "annealing" after installation. If the cable is very long, the power budget should be adjusted accordingly.

Bandwidth effects

Mode scrambling can be exploited in several ways to boost fiber-optic system bandwidth as well as to decrease attenuation. One method of improving bandwidth is to employ low-order modes. Since the launched modal structure is partially preserved over short (less than 100-meter) lengths, launching low-order modes in short systems will lead to primarily low-order modes arriving at the far end. If all modes are launched, the high-order modes slow down relative to low-order modes, causing greater signal distortion. Therefore, avoiding high-order modes can widen a short system's equivalent electrical bandwidth.

There are three ways to launch low-order modes: by modifying the fiber; by modifying the light source; or by modifying the coupling between the two. Modifying the fiber's physical parameters is not practical because of size considerations. To modify the light source, which is the simplest method, the existing source is removed and replaced with a device having a smaller emitting area: the smaller the area, the more preferentially the low-order modes in the fiber are filled. Finally, the coupling of the source and the fiber can be modified by inserting a jumper fiber whose numerical aperture and/or core diameter is much smaller than the main channel fiber. If the system power budget can accommodate the associated loss increase, this technique is convenient for launching low-order modes.

Scrambling with splices

Another method of enhancing fiber bandwidth merely involves applying an in-line fiber splice. Splices cause mode-to-mode power transfer—even if the fiber is free of bends or imperfections—because of microscopic differences in glass density, fiber-to-fiber misalignments, or tiny fiber core bulges at a thermally fused splice. Since mode scrambling tends to equalize the power distribution among propagating modes, the splices in a fiber reduce pulse spreading, increasing the effective electrical bandwidth. This effect is most pronounced over long fiber runs where imperfect splices have been made.

Splicing may not fully equalize modal power distribu-

Using math to make models

The usual explanation of how light moves along optical fiber is based on simple geometric optics and does not take into account the electromagnetic-wave characteristic of light. Cylindrical optical fibers confine light within their diameter and guide it along their length by what is known as total internal reflection. To accomplish these two tasks, fibers have a center region of optically dense material surrounded by optically less dense material. Light rays incident at the interface of these two materials at an angle less than the total reflection angle are trapped by the fiber and guided by it.

But, in fact, not all the light rays within the total reflection limits of a given structure propagate down it. Because light is propagated by means of an electromagnetic wave that has its own physical requirements, only a given number of rays with discrete reflection angles propagate as guided light waves. These are called modes.

These propagating rays, or modes, travel along the fiber because, after successive reflections at the side walls, they repeat in phase, so that they are spatially and temporally synchronous. Thus they interfere constructively when they superimpose upon each other. Rays not repeating in phase will interfere destructively, canceling each other out before they propagate very far along the fiber.

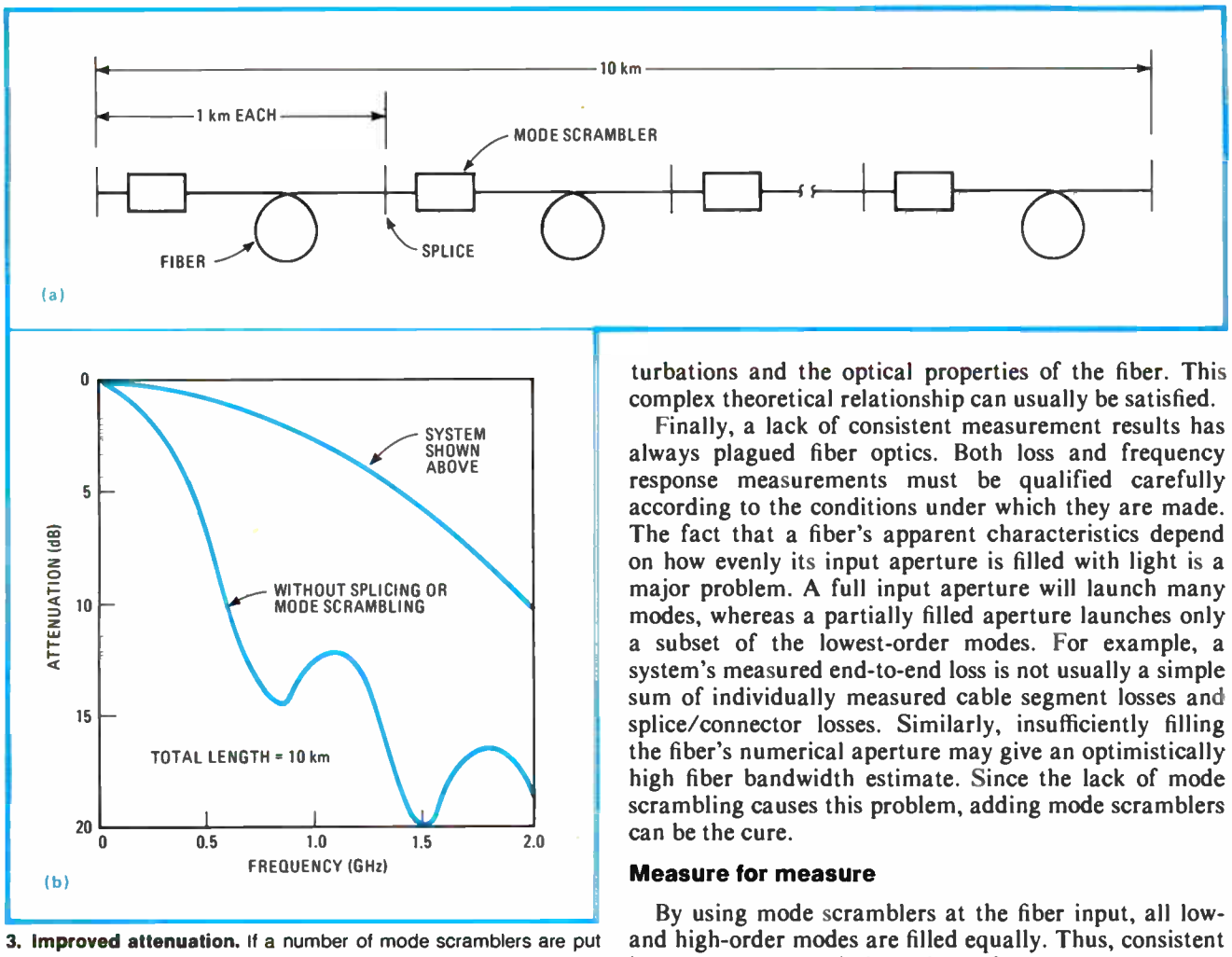
The quantization of waves into a discrete set of modes is required for the solution of the equations that model the fiber's behavior. These were derived by the physicist James Clerk Maxwell in the 19th century. Each cylindrical fiber, with its own peculiar geometry, has a unique set of solutions. Each member of the set of solutions corresponds to a mode.

Usually the optical density of the fiber's inner core has either an abruptly changing or a gradually changing refractive index. The laws of geometric optics that govern ray deflection may be used in either case. As long as the fiber is uniform and of perfect geometry, the wave propagation characteristics relevant to practical optical communication may usually be derived from the ray optics approach.

More importantly, to use the geometric optic approach as a valid approximation of Maxwell's equations, both the step-index fiber and the graded-index fiber must have diameters that are large in relation to the wavelength of the energy propagating through them. But if, on the other hand, it is necessary to propagate only a few modes—to keep attenuation at a low level, to design a device that can couple modes from one fiber to another, or to scramble modes—more rigorous solutions of Maxwell's equations must be found.

Ultimately, the so-called single-mode fiber will be used for optical communications—at least for long-distance, high-bandwidth systems. These fibers have small diameters in relation to the optical wavelength. Here, Maxwell's equations must be solved for each geometry in question—a difficult chore even for simple, idealized fibers with perfect geometry and no imperfections. These numerical analyses, which almost always involve computer assistance, are beginning to involve more and more fiber-optics systems designers as single-mode fiber becomes more important.

As difficult as such analysis may be, it has some advantages. Only one mode propagates in these fibers, and once its characteristics are fully understood, it is easier to design fiber-optic components to process and control the energy. The chore is more easily done, for example, for microwave devices that propagate only one mode, with its single electromagnetic field pattern. In fact, analysis of the operation of multimode microwave waveguides is so difficult that these transmission lines are rarely, if ever, used for practical components. **-Harvey J. Hindin**



3. Improved attenuation. If a number of mode scramblers are put into a 10-km graded index fiber system with splices (a), the system attenuation decreases as its bandwidth increases (b). The simultaneous occurrence of these effects is welcome to the designer.

tion. Additionally, splicing a cable for the sake of equalization may not be desirable from a loss standpoint (if the system power budget is tight) or from reliability or cost-effectiveness standpoints. Mode scrambling may be achieved under these circumstances far more simply by applying enough pressure to the fiber near its connectors, to bend the core. An efficient scrambler to accomplish this can be made of wire kept in tight contact with the fiber by heat-shrinkable tubing (Fig. 2a). The 3-dB fiber bandwidth of such a structure increases approximately as the square root of the number of equidistant mode scramblers that are used (Fig. 2b). System bandwidth can be broadened by a factor of 3 by using such a scrambler (Fig. 3).

Light that leaks

The price to be paid for bandwidth enhancement by scrambling is that scrambling can throw light into leaky or nonpropagating modes that is then lost into the fiber cladding. To minimize this loss, mode scramblers must be designed to scatter light primarily into guided modes. To do this there must be a relationship between the spatial periodicity of scrambler-induced mechanical perturbations and the optical properties of the fiber. This complex theoretical relationship can usually be satisfied.

Finally, a lack of consistent measurement results has always plagued fiber optics. Both loss and frequency response measurements must be qualified carefully according to the conditions under which they are made. The fact that a fiber's apparent characteristics depend on how evenly its input aperture is filled with light is a major problem. A full input aperture will launch many modes, whereas a partially filled aperture launches only a subset of the lowest-order modes. For example, a system's measured end-to-end loss is not usually a simple sum of individually measured cable segment losses and splice/connector losses. Similarly, insufficiently filling the fiber's numerical aperture may give an optimistically high fiber bandwidth estimate. Since the lack of mode scrambling causes this problem, adding mode scramblers can be the cure.

Measure for measure

By using mode scramblers at the fiber input, all low- and high-order modes are filled equally. Thus, consistent loss measurements independent of source type, source-fiber misalignments, or the fiber's inherent mode coupling length can be made. Such a stable distribution of modes at launch (one that simulates the modal distribution beyond the mode-coupling length) can be ensured for lateral source-fiber misalignment as well as for both light-emitting-diode and laser sources.

Additionally, cables with splices or connectors can be measured accurately by inserting mode scramblers after each continuity break. This technique guarantees that all propagating modes are refilled after each break. It also provides loss measurements that can be correlated with measurements made on a single length of standard cable, if the baseline cable is also measured using an input mode scrambler.

More repeatable bandwidth measurements can also be made with mode scramblers. Because all modes are equally excited spatially at launch when an input scrambler is used, the fiber's actual long-length bandwidth can be estimated from measurements made over fiber lengths shorter than the mode-coupling length. This standardization method can decrease some of the confusion surrounding bandwidth testing. □

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2. S. E. Miller and A. G. Chynoweth ed.; "Optical Fiber Telecommunications," Academic Press, New York, 1979, p. 31.

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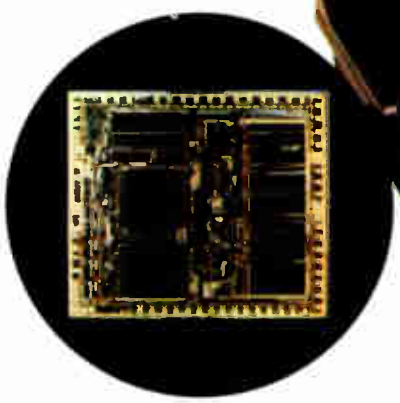

A full ¼" chip can be viewed at the lowest magnification (22.5X).

Chip photo courtesy of Motorola Corp

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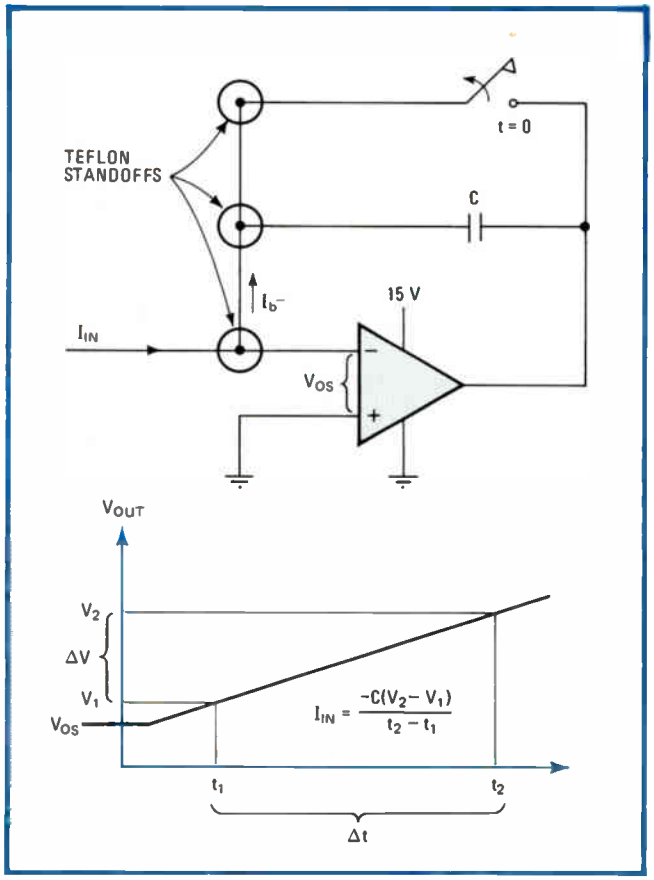
Charge integrator measures low-level currents

by Philip R. Gantt
Precision Monolithics Inc., Santa Clara, Calif.

Current cannot be measured accurately at picoampere levels by conventional measurement techniques. Yet in many cases, such small leakage currents can have a considerable effect on system performance. Measuring current at picoampere, and even femtoampere, levels is possible, however, using the method of charge integration. As shown here, a charge integrator can be easily used in conjunction with sample-and-hold amplifiers or analog-to-digital converters, or both, for such wide-ranging tasks as determining the leakage current at the gate of a field-effect transistor or measuring and recording small currents with the aid of an automated (microprocessor-based) test system.



1. Current climb. Bi-FET integrator can measure femtoampere leakage currents. Particular attention is paid to reducing shunting errors by mounting feedback-to-input connections on Teflon standoffs and using a polystyrene or Teflon capacitor. With a 100-pF capacitor, 100-pA input current produces an easily measured ramp of 1 V/s.

The integrator, shown in Fig. 1, is one of the simplest circuits that can be configured with an operational amplifier. Its relative immunity to 60-hertz interference is due to the negative feedback provided through a capacitor (C). The accuracy of the basic circuit is limited mainly by two factors—the input bias current of the op amp and the user's ability to measure voltage with respect to time.

The output voltage of the integrator is given by:

$$V_o = -\frac{1}{C}\int_{t_1}^{t_2} I_{in}dt - \frac{1}{C}\int_{t_1}^{t_2} I_{b^-}\,dt + V_{os}$$

where I_{in} is the driving current to the op amp, I_{b^-} is the inverting input's bias current, and V_{os} is the amp's offset voltage. Thus, if $I_{in} = 0$, it is in principle possible for the circuit to measure the bias current I_{b^-} or to accurately measure the leakage current, I_{in}, of an external device if $I_{in} >> I_{b^-}$.

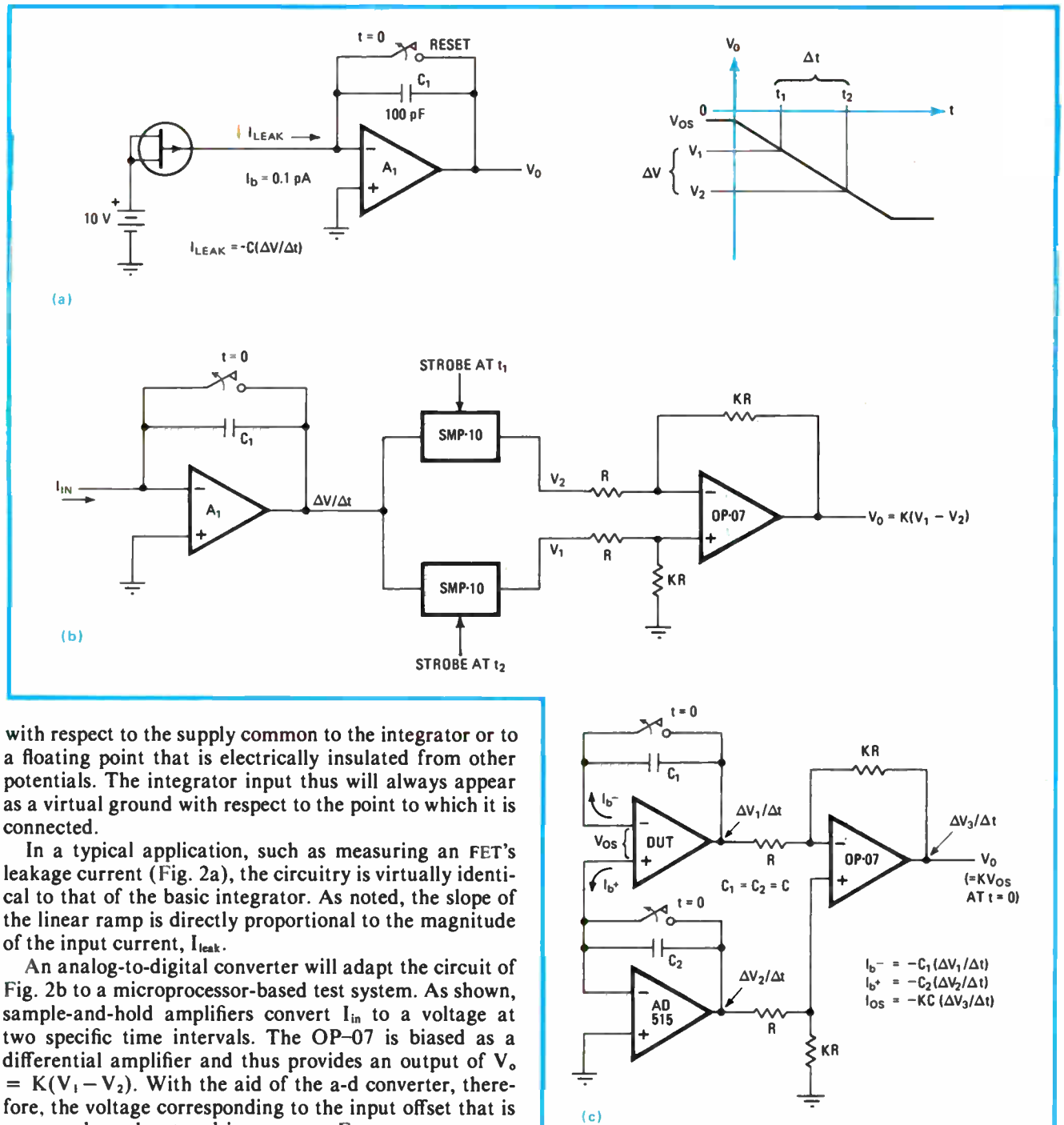
The integrator can be made practical for these low-level measurements by minimizing the leakage current of the entire circuit itself and by using an appropriate op amp. Installing Teflon standoffs at the op amp's inputs is recommended, and a low-leakage capacitor of the polystyrene type or, in high-temperature applications, a Teflon capacitor is necessary. Where printed-circuit boards are used, a high-surface-resistivity laminate such as Triazene is recommended to prevent leakage currents from flowing. The relay used to reset the integrator should be a high-impedance device of the glass reed type.

For measurements at several hundred picoamperes, a bipolar field-effect-transistor op amp should be used in conjunction with a 100-pF capacitor. Should measurements at lower levels be required, an electrometer amplifier with an input bias current of less than 0.1 pA is needed. Measurements down to 1 fA are possible using a discrete integrated-gate FET with the input biased at $V_{gs} = 0$ for low leakage.

Ideally, the input voltage as a function of time for a given input current will be a ramp. Since the V_{os} of the op amp is a constant and the terms relating to current are a change in voltage with respect to time, the offset voltage of the op amp is insignificant. Because the value of C will be known, $\Delta V/\Delta t$ can easily be observed on a storage scope or measured with the aid of a voltmeter and a stopwatch.

The anticipated current flow determines the capacitor value selected. A high-impedance reed relay placed across the integrating capacitor can be used to discharge it and reset the integrator for sequential measurements. For a 100-pA input current, a 100-pF capacitor would produce a voltage ramp of 1 volt/second, an easily measured value.

Because the noninverting input of the integrator is tied to ground, a potential at the input will normally cause the integrator to rail. To ensure against this, the input should be connected either to a point of zero potential



2. Applications. Charge integrator is ideal for measuring FET gate leakage (a). It is adapted to use with a microprocessor-based test system with sample-and-hold and differential amplifiers (b), which convert current into voltage so that measured values can be stored. More than one op amp offset parameter can be determined during a measurement (c). The circuit, which eliminates resistive-type errors, is well suited for measuring low currents.

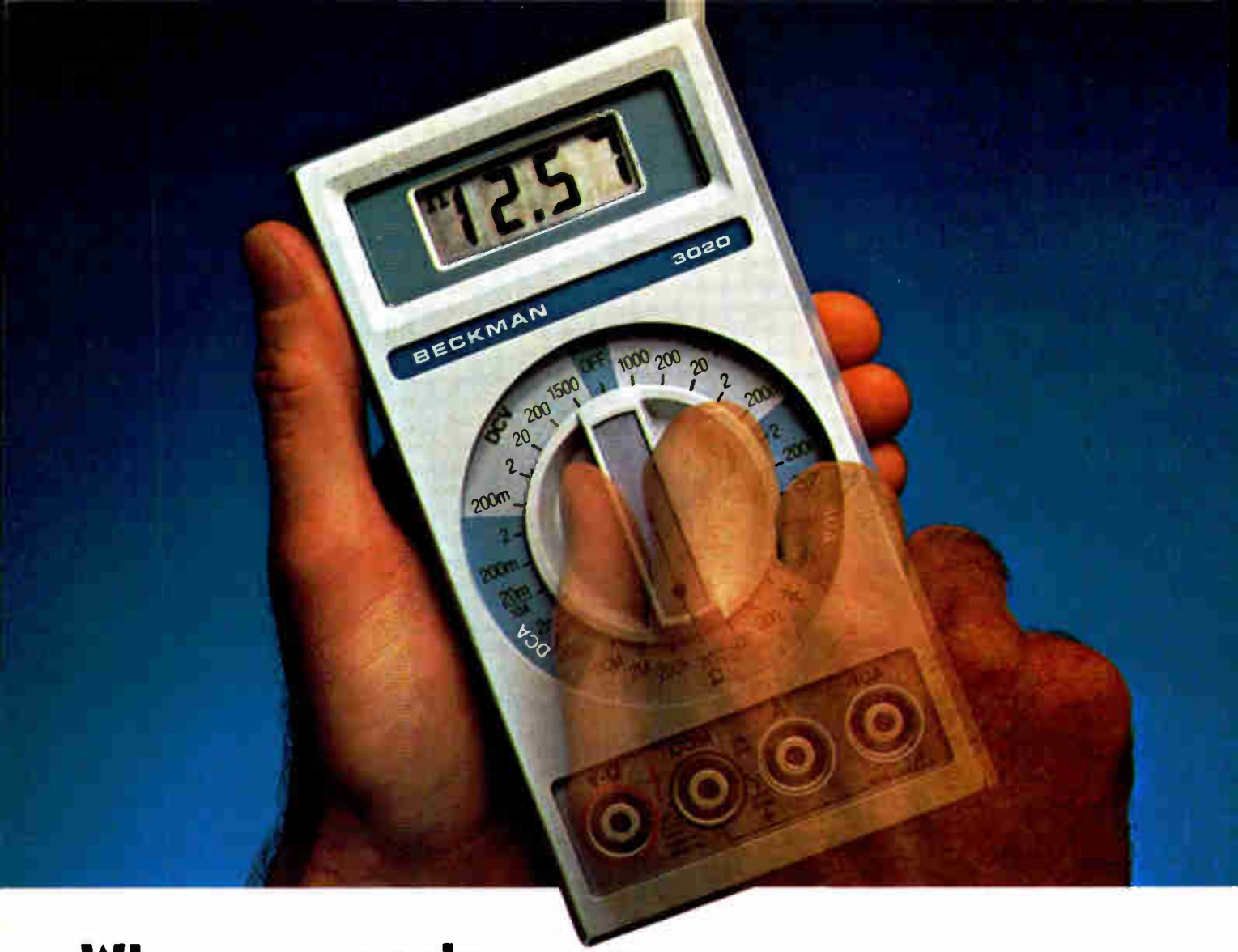
with respect to the supply common to the integrator or to a floating point that is electrically insulated from other potentials. The integrator input thus will always appear as a virtual ground with respect to the point to which it is connected.

In a typical application, such as measuring an FET's leakage current (Fig. 2a), the circuitry is virtually identical to that of the basic integrator. As noted, the slope of the linear ramp is directly proportional to the magnitude of the input current, I_{leak}.

An analog-to-digital converter will adapt the circuit of Fig. 2b to a microprocessor-based test system. As shown, sample-and-hold amplifiers convert I_{in} to a voltage at two specific time intervals. The OP–07 is biased as a differential amplifier and thus provides an output of $V_o = K(V_1 - V_2)$. With the aid of the a-d converter, therefore, the voltage corresponding to the input offset that is measured can be stored in memory. For greater accuracy, leakage error currents and droop errors can be calculated and then subtracted from measurements of device current. For measurements amid high noise, the integration period $(t_2 - t_1)$ should be a multiple of 60 Hz.

In Fig. 2c, three op-amp parameters are measured during one integrating time period. This circuit is especially suitable for measuring low I_b and low I_{os} values, as it avoids the resistive-type errors inherent in conventional measurements.

With the integrator in a voltage-follower configuration, the input offset voltage of the device under test can be measured by shorting the relays across the integrating capacitors. The V_{os} of the AD515 must be nulled to zero, or a relay having a low temperature-to-offset voltage dependence must be placed across the input of the device under test, in order to measure and subtract the errors on an automated basis. □



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Circle 172 on reader service card

Adapter equips HP analyzer for general ROM tracing

by Israel Gal
Liad Electronics, Moshav Yaad, Israel

A two-socket adapter turns the popular Hewlett-Packard family of HP1611A logic analyzers—which can normally be configured for debugging one specific microcomputer—into a general-purpose read-only-memory tracer. Thus, as this example shows, it can be used with the Z-80 Personality Module as a developmental tool for Intel machines, without the need for Intel's ICE series of in-circuit emulators.

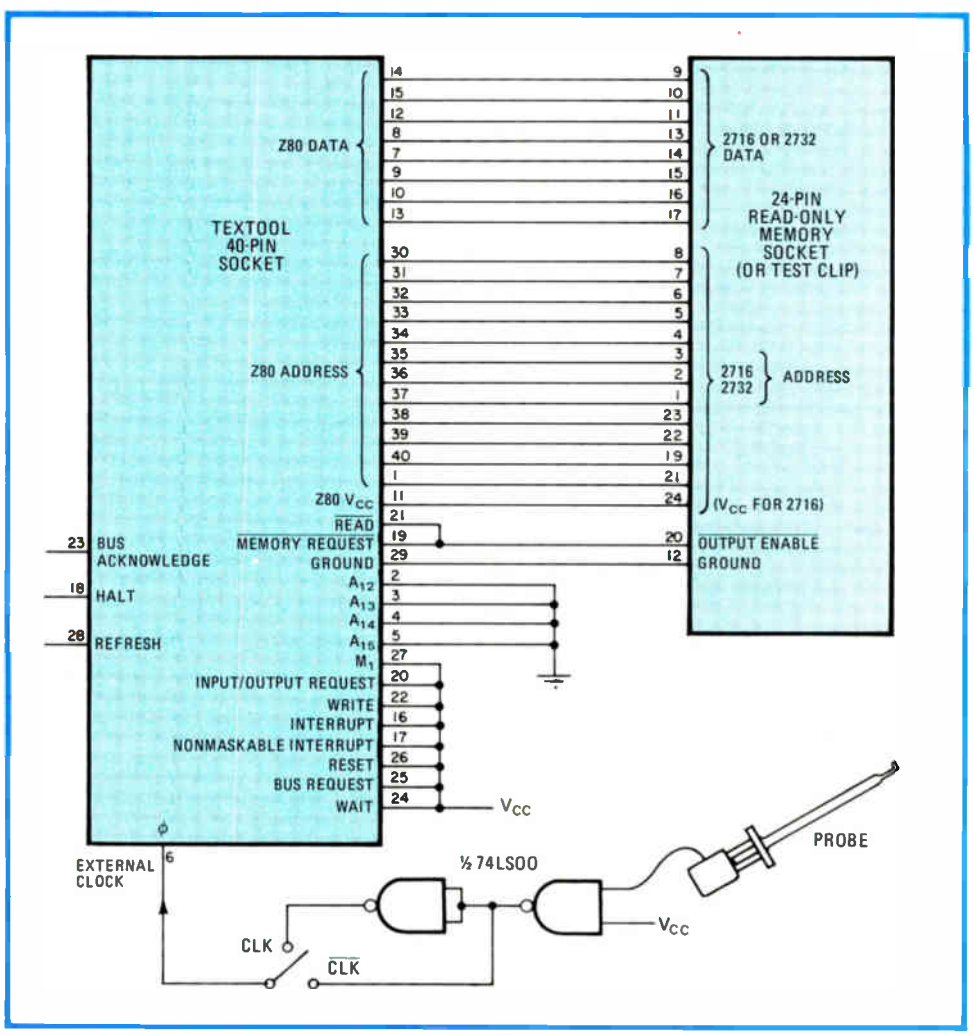
Tracing is simply achieved by placing the microprocessor's address and data lines directly in parallel with those of the external program memory and disabling all other input lines to the Z-80. Placing a low-insertion-force socket, such as those produced by Textool Inc., at the Z-80 end enables fast connection to the conversion circuit. At the memory end, use of a hardwired 24-pin spring clip adds increased flexibility for in-field testing. Also recommended is a scope probe for latching onto the appropriate circuit point of the desired clock signal. The clock and its inverse signal are available, so that the user can synchronize the timing to each particular processor.

In operation, the logic analyzer will be synchronized as usual to accept address, data, and external information in every possible combination. Thus, most of the additional options of the analyzer, such as pretriggering, post-triggering, trace and count triggering, and trigger enable and disable can be utilized. The single-step and trace-then-halt options of the Intel 8031-8051 machines cannot be used here, although they will be functional on every other processor that has a wait line.

Using the HP1611A this way has several drawbacks, among them the fact that there is no disassembly—information is displayed in hexadecimal or octal format. And the information shifted onto available on-chip RAM or registers is not itself displayed, only the representation of the transfer as an operating code. Also, as a result of the clocking arrangement, there can be situations where the directive will be displayed twice (although the address is always correct). However, where low cost, convenience, and efficiency are important, this circuit is satisfactory. □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $75 for each item published.

Translator. Parallel connection of data and address lines of external memory with HP1611A logic analyzer through appropriate interface eases debugging of any microprocessor-based system by a dedicated analyzer. Scheme has drawbacks—lack of disassembler, the fact that shifted information cannot be actually displayed, and occasional multiple display of op code directives—but is cheap, convenient, and efficient.



Engineer's newsletter

How to check that Basic programs meet ANSI standard

Software designers who use Basic and need to ensure that their programs meet the American National Standards Institute's new minimal guidelines for routines written in that language will want the National Bureau of Standard's new two-volume publication. It describes a set of programs for testing whether various implementations of Basic comply with the Federal Information Processing Standard 68 and ANSI standard X3.60-1978, which are virtually identical.

The 556-page manual is titled "NBS Minimal Basic Test Programs—Version 2, User's Manual." Volume 1, on documentation, describes the nature of the ANSI standard and how the tests support it. Volume 2, on source listings and sample output, supplements the information in the first volume, enabling the user **to examine various source codes in their original form.** In addition, it familiarizes the user with the form of the standard implementation at the output.

The two volumes sell for $4 and $9.50, respectively. They are available from the Superintendent of Documents, U. S. Government Printing Office, Washington, D. C. 20402. Order by stock number, 003-003-02262-4 for the first volume and 003-003-02263-2 for the second.

Vhf conference is receiving professional hams

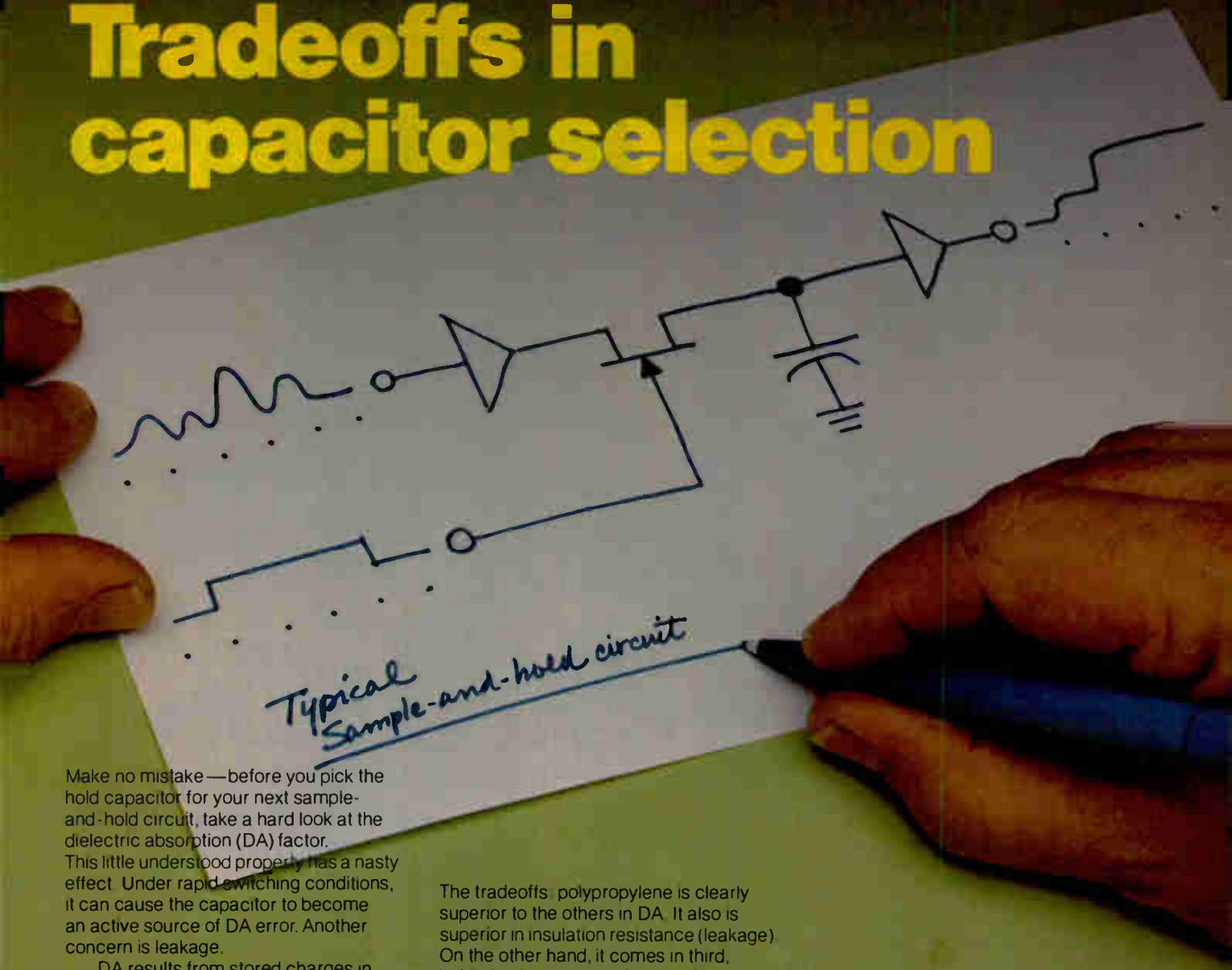
Calling out to the professional radio-engineering community, Western Michigan University is asking for papers for presentation in its 27th Annual vhf Conference, which will be held on campus the afternoon of Saturday, Oct. 17. The conference, long respected by technically minded radio amateurs, has in recent years attracted a growing number of engineers and speakers from industry and the universities. Chairman Glade Wilcox is now attempting to raise the level of quality even further. Papers are being solicited on a wide range of subjects, including **picture transmission and reception, satellites, antennas and transmission lines,** measurement and test equipment and mobile operation, in addition to other topics of traditional interest to amateurs.

The deadline for submission of synopses is June 30. Speakers will be notified of their acceptance by Oct. 1. Final drafts may be given to the chairman on the day of the conference. Contact Prof. Wilcox at the Department of Electrical Engineering, Western Michigan University, Kalamazoo, Mich. 49008, for more information.

Watch how you wash that capacitor

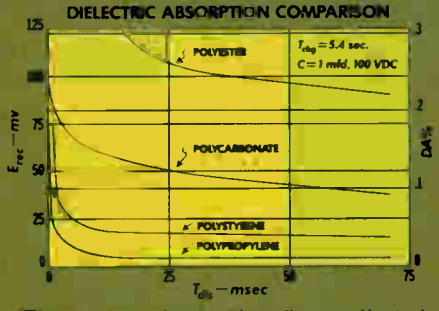
The halogenated hydrocarbon solvents used for cleaning and defluxing printed-circuit boards will attack unprotected aluminum electrolytic capacitors and cause their eventual failure, according to a recent application note released by the Sprague Electric Co., North Adams, Mass. The results of tests performed by Sprague support the cautionary statements made in the military specification MIL-C-39018 and the Electronic Industries Association's RS-395. They indicate that **among the generic substances that may or may not contain solvents, the safe ones** are acetone, butyl-, ethyl-, methyl-, and propyl-alcohol, lacquer thinner, butyl cellosolve, toluol-hexane-ethyl-acetate, xylene, and mineral spirits. Among the brand-named, acceptable substances are Alpha 2001, Aquaflux Strap 1000, FC78, Kenco 190 and 2240, Loncoterge 444-N, and the popular detergents Calgonite, Oakite, and Turco. All other agents should be avoided, unless the capacitor is so constructed that it contains an epoxy barrier. Even then, its exposure to any of the undesired solvents should last no more than 2 minutes. **-Vincent Biancomano**

Tradeoffs in capacitor selection



Make no mistake—before you pick the hold capacitor for your next sample-and-hold circuit, take a hard look at the dielectric absorption (DA) factor. This little understood property has a nasty effect. Under rapid-switching conditions, it can cause the capacitor to become an active source of DA error. Another concern is leakage.

DA results from stored charges in the dielectric which behave as parasitic RC components. These subversive elements serve to aggravate output voltage error, which obviously means a loss of accuracy. How much loss of accuracy depends primarily on the dielectric material. Typical DA percent values (i.e., voltage error), measuring accumulated charge after a controlled discharge, are:



(These values also, incidentally, are affected by capacitor value, size and configuration.)

The tradeoffs: polypropylene is clearly superior to the others in DA. It also is superior in insulation resistance (leakage). On the other hand, it comes in third, behind polystyrene and polycarbonate but ahead of polyester, in temperature coefficient.

Upshot: if high accuracy in your sample-and-hold circuit is a must, polypropylene is a must, too.

Next decision: source. TRW researched, developed and introduced polypropylene for use in miniaturized precision capacitors. We made it work in the real world. We suggest, therefore, that you test our Type X363UW for your next sample-and-hold design. It can save you a lot of design time.

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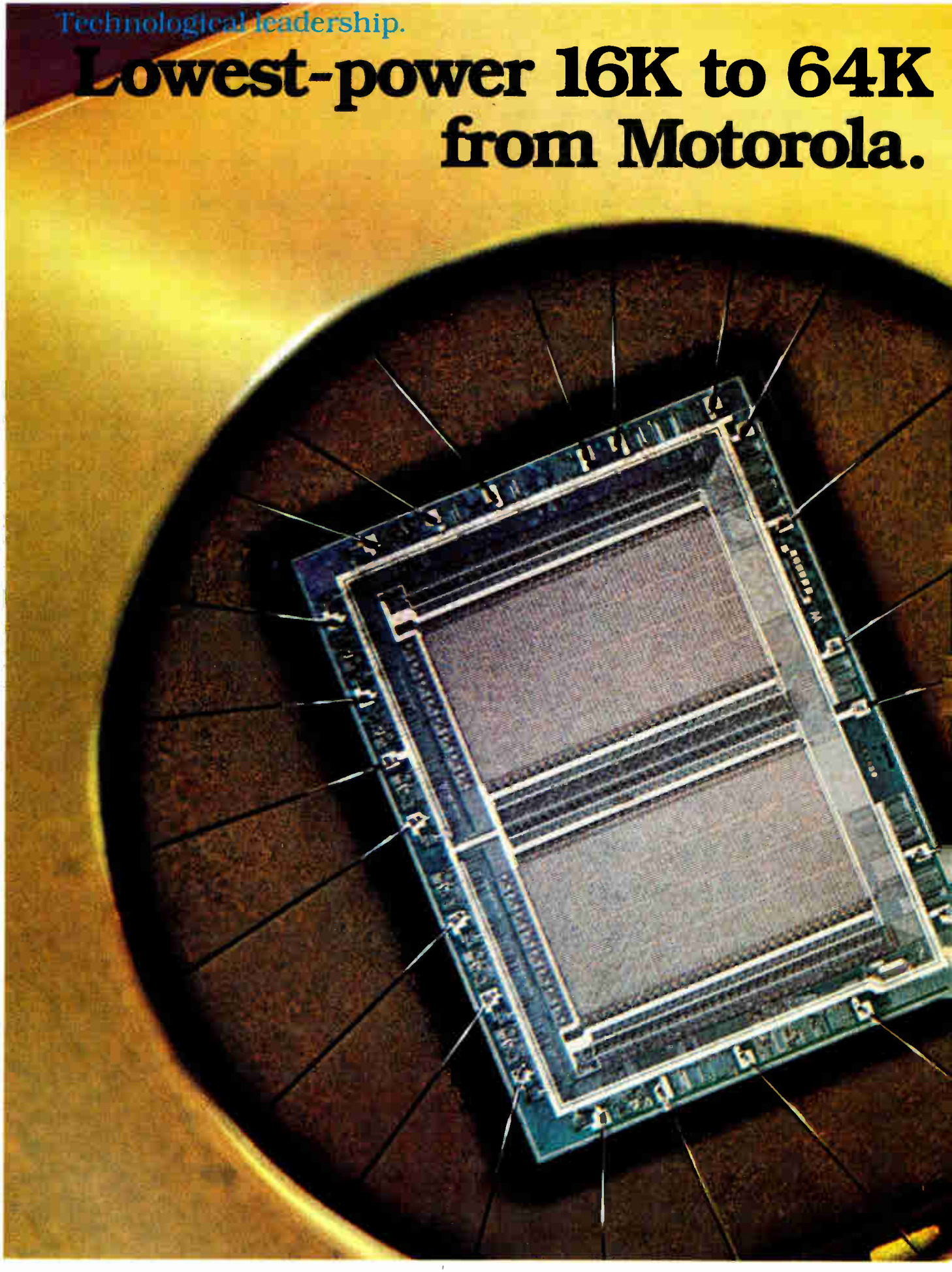

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Order Motorola 5 V EPROMs now from your local Motorola sales office or authorized distributor. For additional information, use the coupon or write to Motorola Semiconductor Products Inc., Technical Information Center, P.O. Box 20912, Phoenix, AZ 85036.

Motorola's Comprehensive 5 V EPROM Family

Motorola Part Number	Access Time – ns	Max Active Current – mA	Max Standby Current – mA	5 V Supply Tolerance – %
16K EPROMs				
MCM2716	450	100	25	± 5
MCM27L16*	450	50	10	± 5
MCM2716-35	350	100	25	±10
MCM27L16-35*	350	50	10	±10
32K EPROMs				
MCM2532	450	100	25	± 5
MCM25L32*	450	50	10	± 5
MCM2532-35*	350	100	25	±10
MCM25L32-35*	350	50	10	±10
64K EPROMs				
MCM68764*	450	120	25	± 5
MCM68L764*	450	60	15	± 5
MCM68766	450/150‡	100	–	± 5
MCM68766-35	350/150‡	100	–	±10

*Lowest power in the industry. ‡Access time from output enable

Industry-standard ROMs, 64K dynamic RAMs, fast static RAMs, and these leading 5 V EPROMs all point to one thing. Motorola has the MOS memories you need for

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TO: Motorola Semiconductor Products

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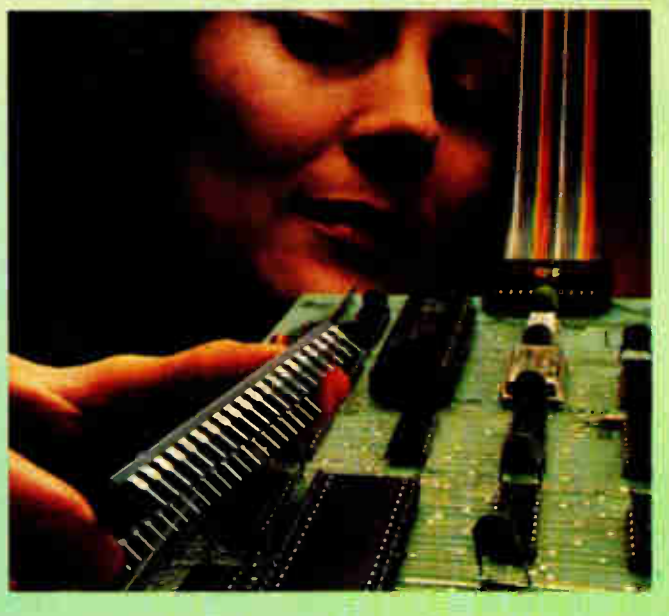

That's because AMP DIPLOMATE sockets' anti-overstress design prevents the major cause of socket failure. And at a cost-effective price.

DIPLOMATE sockets are available with the widest choice of features in the industry today. You can choose between .175" and .160" in profiles and solid or ladder housing construction. Our designs feature large contact target area for machine insertion, closed bottom to prevent solder contamination, and leg retaining detents to help increase productivity to meet your design needs. There are even MIL-S-83734 approved types.

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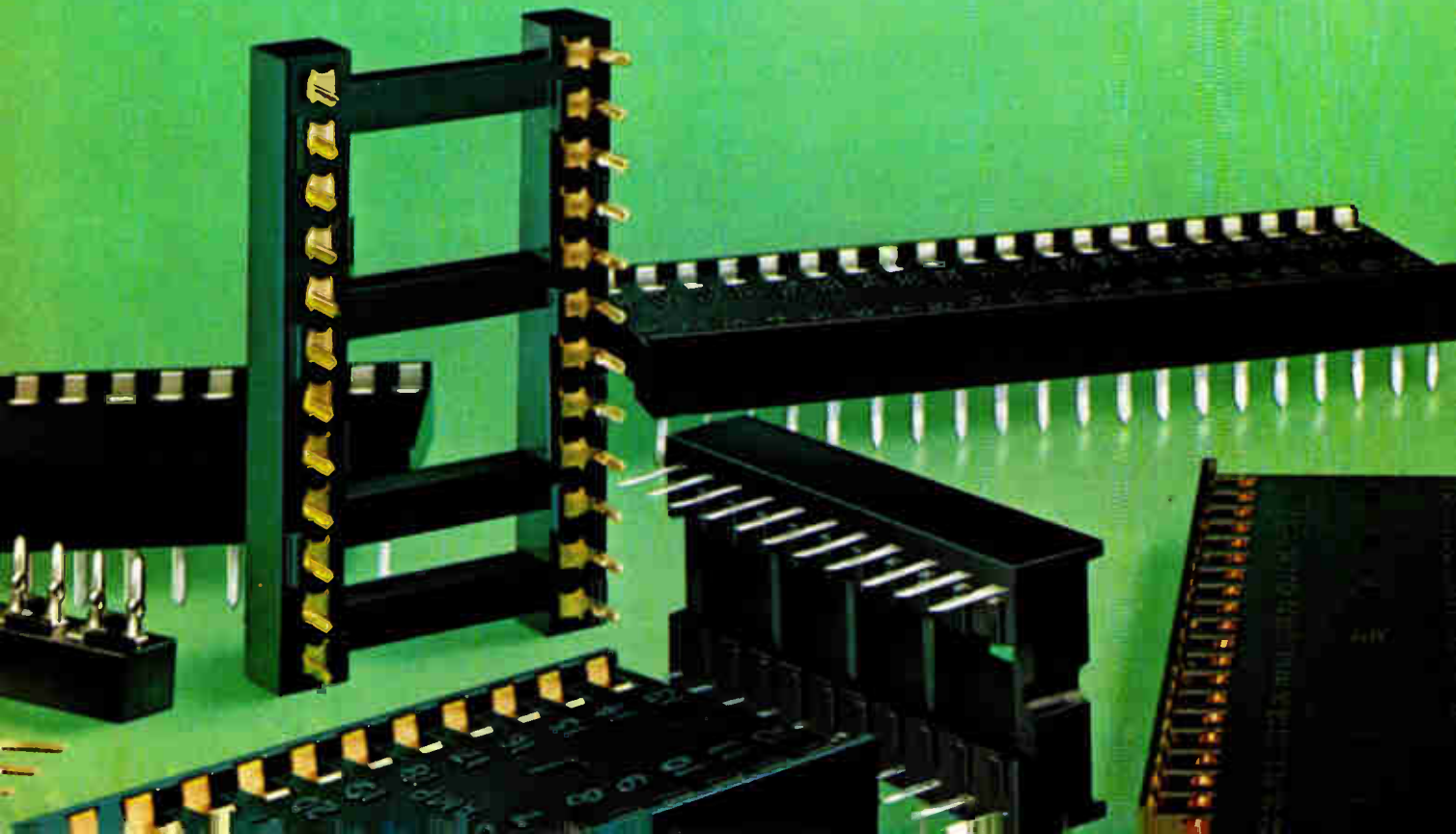


AMP Facts

for DIPLOMATE Sockets .175" Profile

Performance Characteristics

Physical

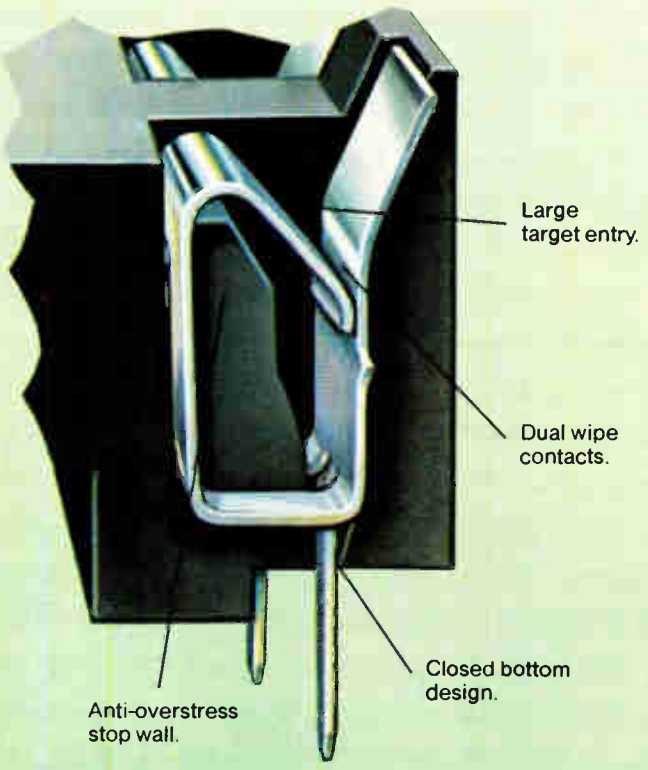
Engaging force: 340 grams max. (0.13) [0.33] pin)
Separating force: 14 grams min. (.008 [0.20] pin)

Electrical

Rating: 250 VAC
Contact resistance: 20 milliohms max. initial, 30 milliohms max. after test
Dielectric withstanding voltage: 1000 VRMS min.
Insulation resistance: 5000 megohms min.
Capacitance: 1 picofarad max.

Environmental

Operating temperature: −55°C to +105°C (tin plate)
Vibration: 10-2000-10 Hz in 20 minutes at .06 [1.52] or 15G's for 3 sweeps in each of 3 axes.
Shock: 100 G's, sawtooth waveform, total 6 shocks.



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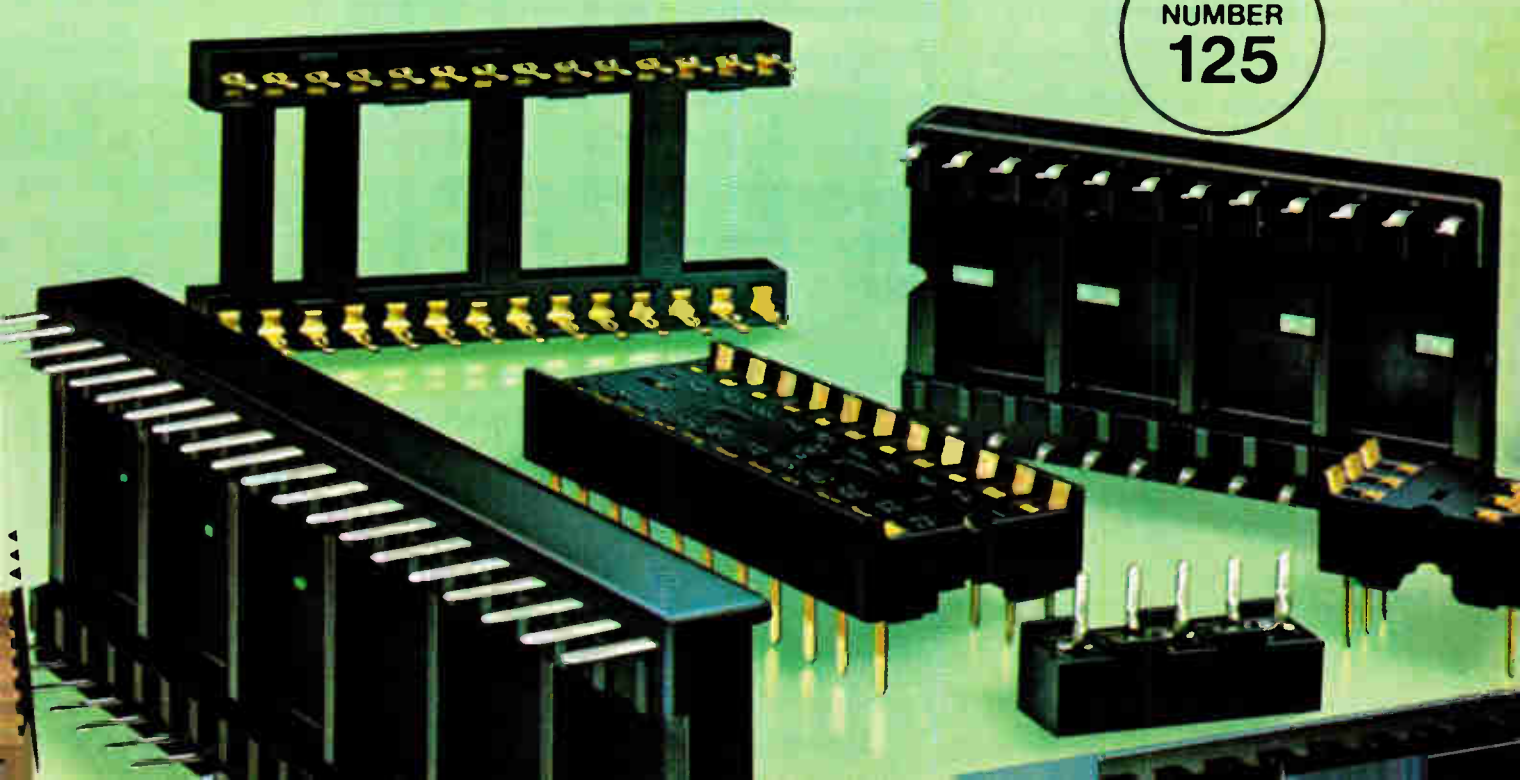

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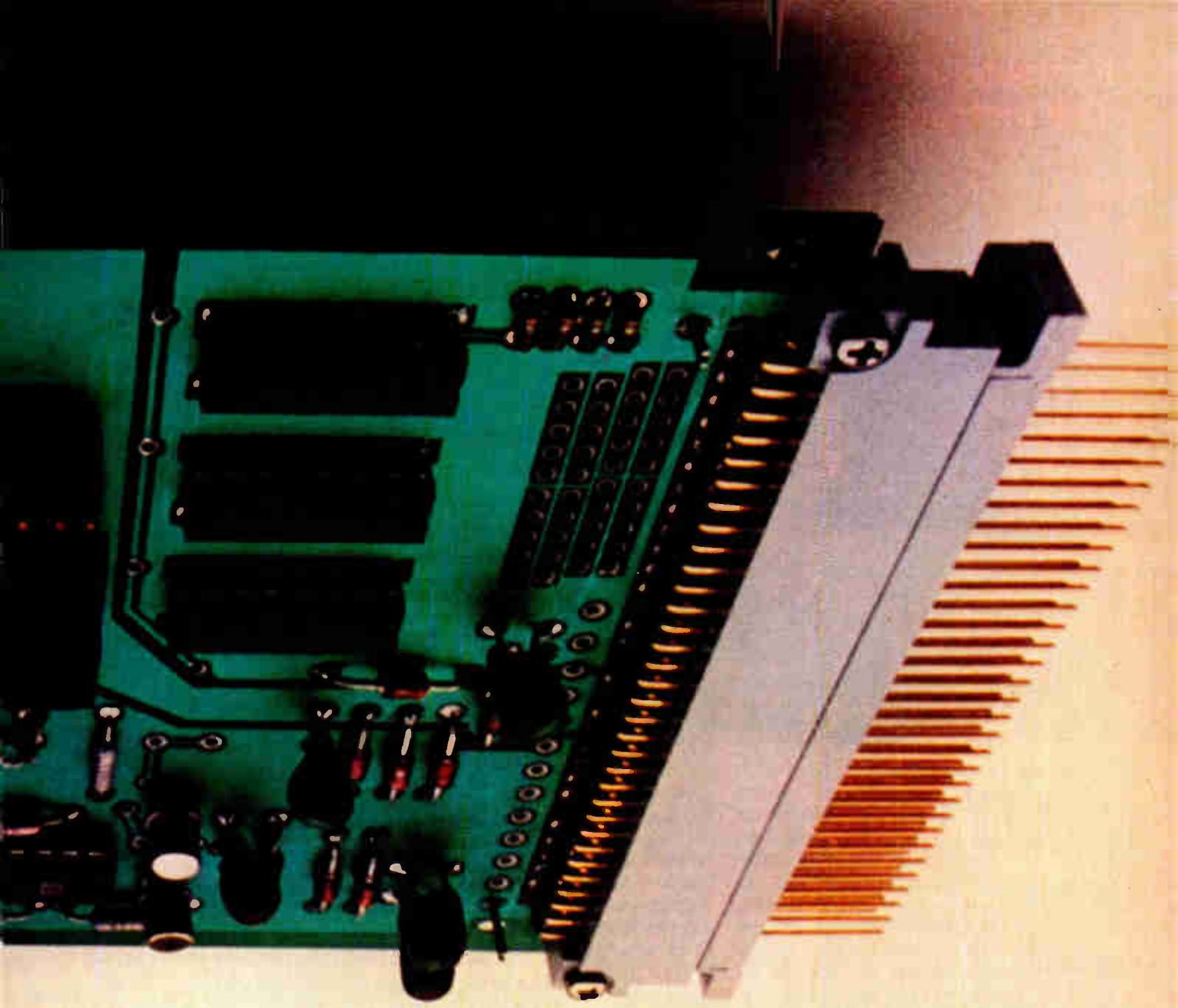

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process moves the wafers into and out of the reactor.

Most of the 480's processing functions are software-controlled, making the system's Z80 microprocessor more than just a sequencer, notes company president David K. Lam. He adds that this approach gives engineers greater flexibility and control in setting process parameters and minimizes the need for operator intervention during processing. An RS-232 port and standard software interface make the system compatible with remote host systems.

The 480 includes a cathode-ray-tube console for system monitoring and program development. Taking up 10.5 square feet of floor space, the machine will have throughputs of 30 to 60 wafers per hour; an expanded version of the 480 planned for later this year will double that rate while requiring only 35% to 40% more floor space, Lam says. The Autotech 480 will cost $165,000. Shipments begin in mid-1981, and delivery takes four to six months.

High throughput. Bowing at Semicon West this May will be Anelva Corp.'s 4001 reactive-ion etching system, which guarantees throughputs of 56 to 72 wafers per hour. A U.S. version of Anelva's Japanese model 504, the 4001 uses a simplified, ruggedized shuttle mechanism for wafer transport. It also employs two load locks, each able to handle two vertically stacked wafer cassettes. The reactor chamber processes 10 wafers at a time.

The 4001 includes a keyboard, CRT display, and two floppy disks. A Sord DA223 microprocessor runs the system and communicates with a host computer via an RS-232 port. Prices will be between $200,000 and $250,000; first shipments will take place in August or September.

R&D etching. Whereas the Anelva machine is production-oriented, Materials Research Corp.'s RIE-51 reactive-ion etching system is intended primarily for research and development. MRC says, however, that the RIE-51 can be operated on small production lines and can achieve throughputs of 10 to 40 wafers per hour. The system can etch materials like gold, aluminum, and gallium arsenide; product applications include processing magnetic-bubble memories, surface-acoustic-wave devices, and optical integrated circuits.

The RIE contains eight ports for diagnostic and control instrumentation. Its modular design enables customized configuration, so its price ranges from $23,000 to $60,000; delivery takes 120 to 150 days.

Independent channels. The Plasma Inline 701 from Tegal Corp. in Novato, Calif., costs $76,000 domestically. The single-wafer system automatically transports wafers from cassettes into a reaction chamber. Logic circuitry controls gas composition and flow, power, chamber pressure, and the like. Two independently variable process channels let users run combined or different etching processes without halting production to reset the whole machine.

The 701 has two automatic end-point detection modes and three automatic impedance-matching settings. It can operate fully automatically or be stepped through a process sequence with a push-button switch mounted on the inside control panel. Delivery of the 701 takes 90 to 120 days. Tegal also expects to announce its Plasma Inline 702, designed for etching aluminum and other metals and priced around $130,000, at Semicon West. Although technical details are not yet firm, the 702 will incorporate a 68000-type microprocessor and most system functions will be under software control.

Anelva Corp., 536 Weddell Drive, Suite 4, Sunnyvale, Calif. 94086. Phone (408) 744-1780 [401]

Drytek Inc., 220 Ballardvale Street, Wilmington, Mass. 01887. [402]

Lam Research Corp., 3350 Scott Blvd., Building 31, Santa Clara, Calif. 95051. Phone (408) 496-6999 [403]

Materials Research Corp./Plasma Etching Division, 35 Jefferson Ave., Pearl River, N.Y. 10965. Phone (914) 735-4900 [404]

Plasma Systems Inc., Linscott Road, Woburn, Mass. 01811. Phone (617) 933-9170 [405]

Tegal Corp., 1 Commercial Blvd., Novato, Calif. 94947. Phone (415) 472-7500 [406]

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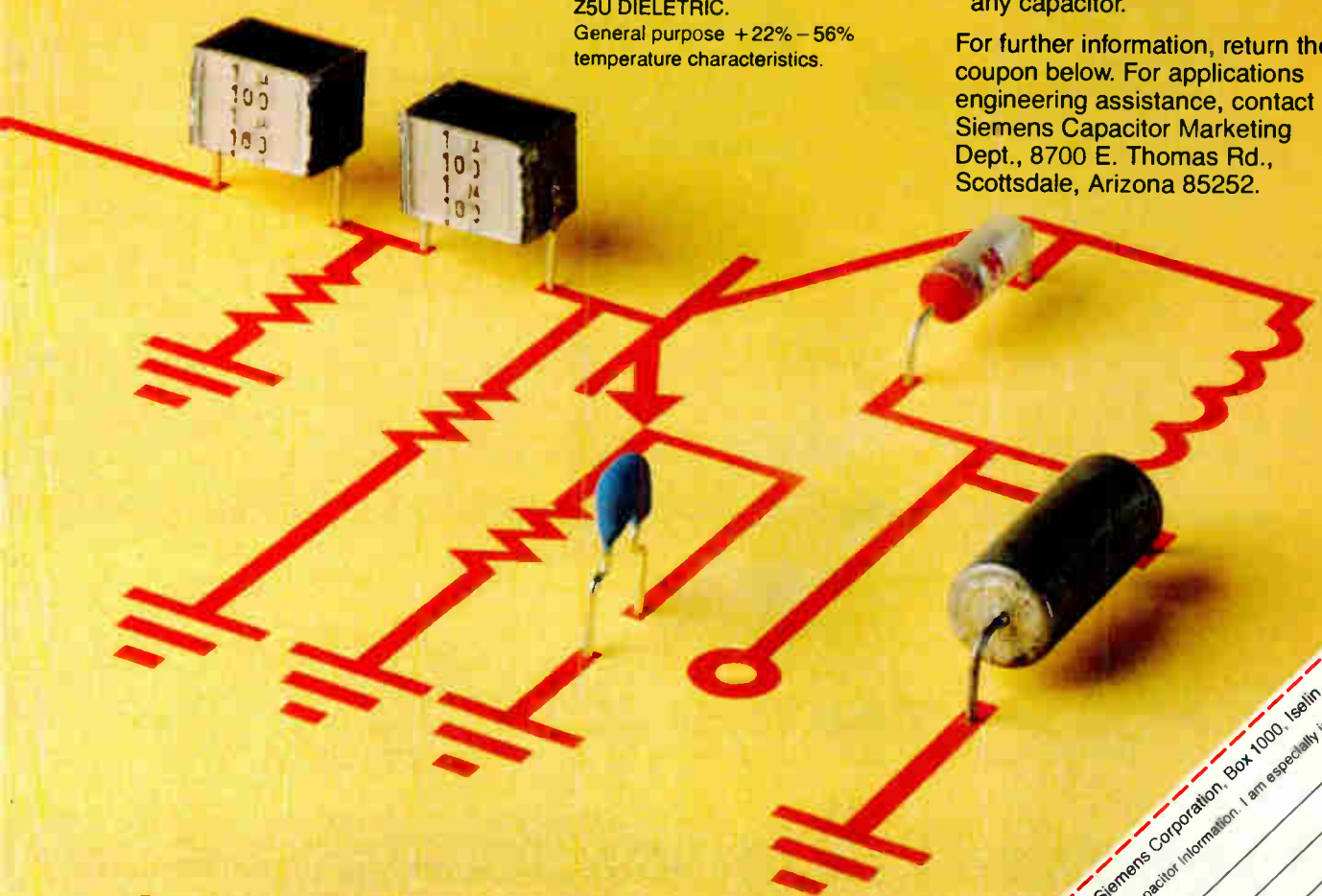

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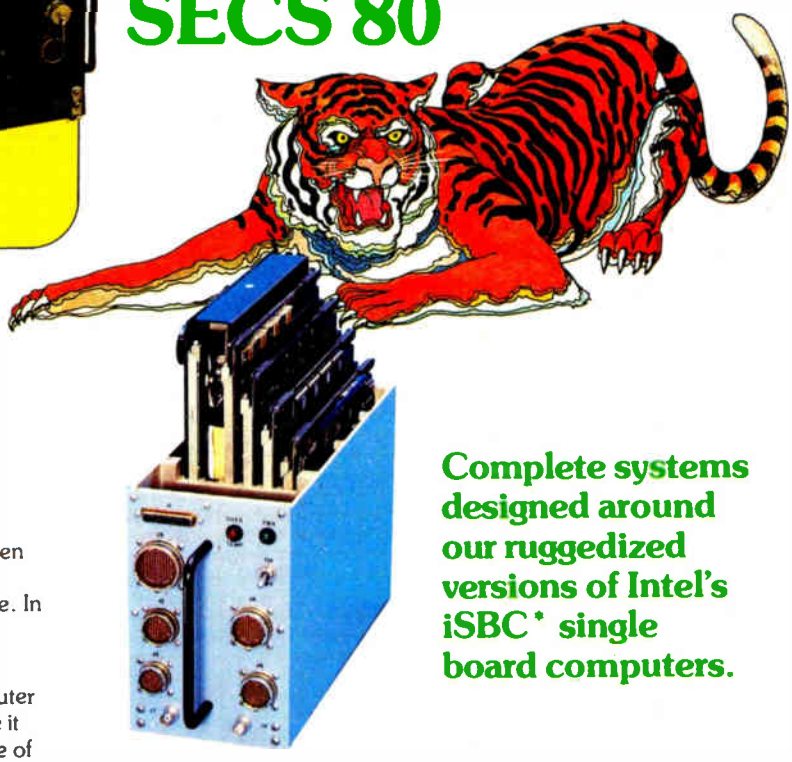
SECS 80



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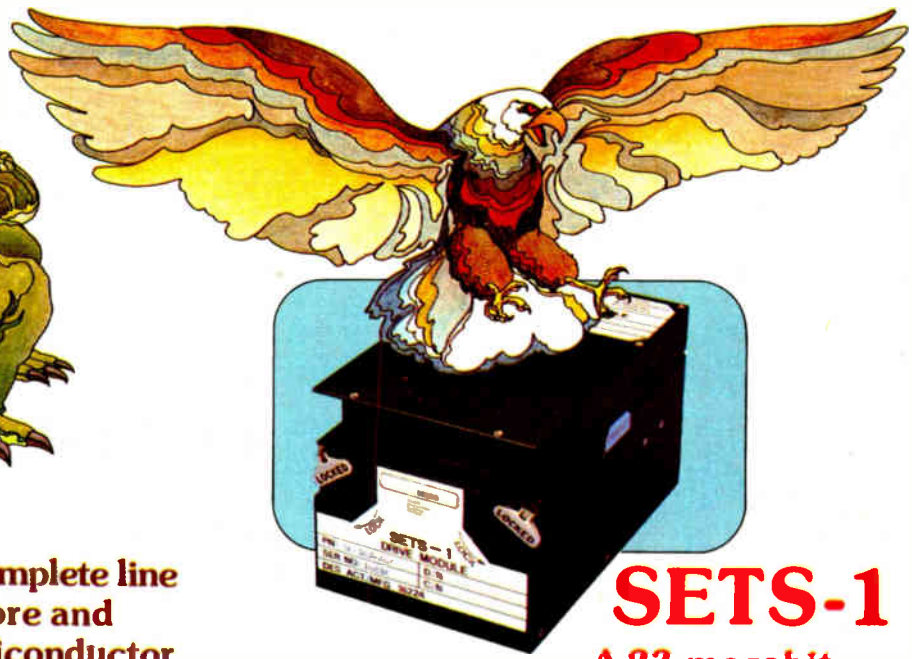

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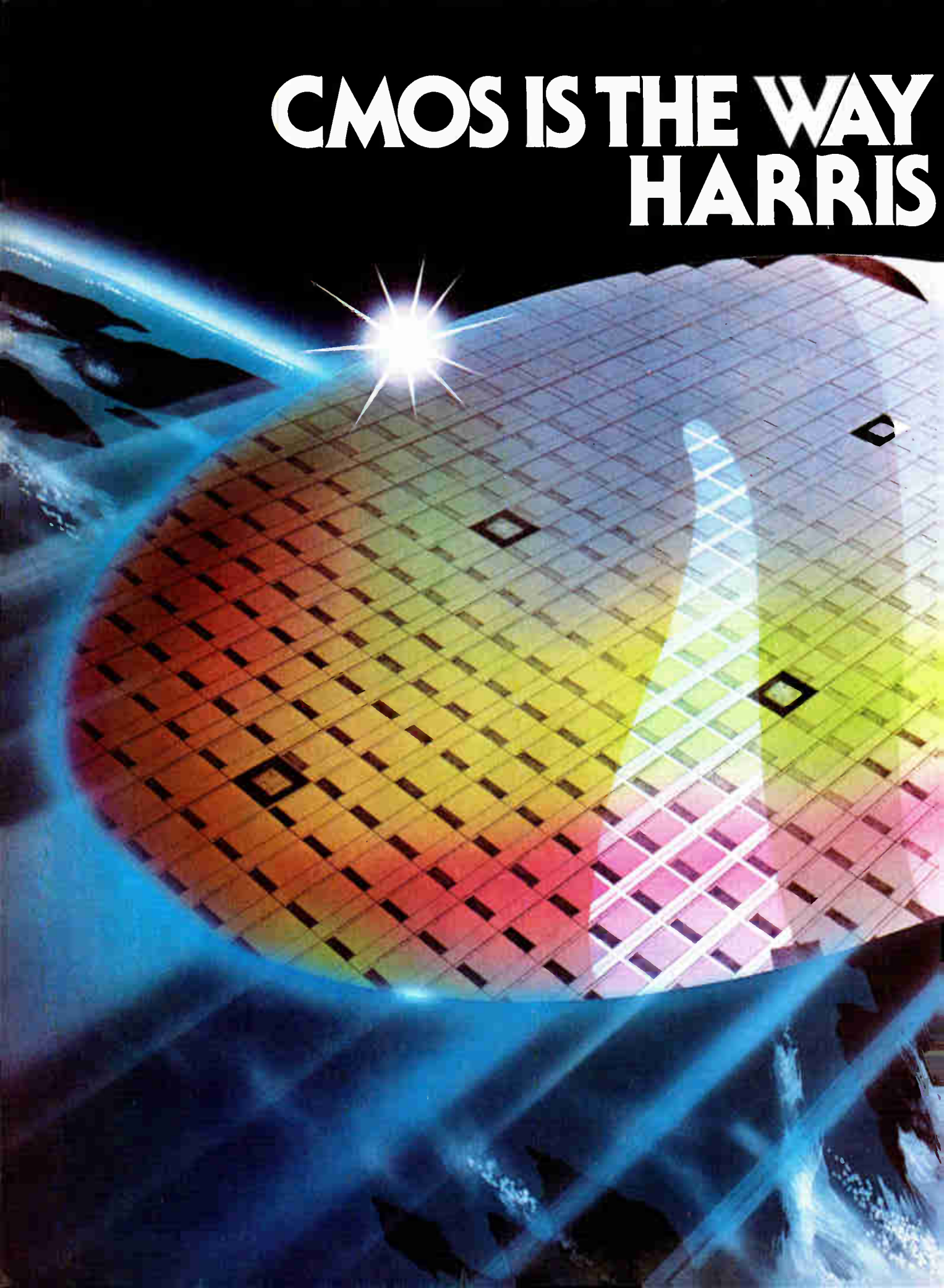

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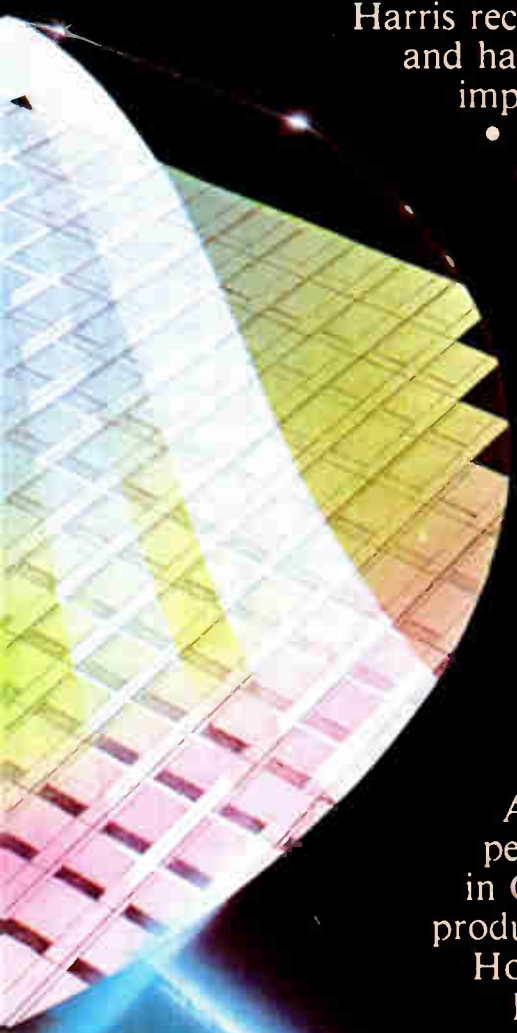

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Pulse generator speeds logic tests

100-MHz microprocessor-controlled pulse generator produces clean, fast pulses with rise times variable from 1.3 ns to 900 μs

by John Gosch, Frankfurt bureau manager

A 100-MHz repetition rate, a variable rise time as short as 1.3 ns, and setting accuracies of better than 2% are the key features of a fully programmable microprocessor-controlled pulse generator from Hewlett-Packard GmbH, the Böblingen, West Germany–based arm of the California company.

Intended for bench and system applications and suitable for jobs in research and development, production, and incoming inspection, the HP 8161A automates pulse parameter tests of fast logic circuits such as emitter-coupled logic and advanced Schottky TTL—tests that "for lack of effective instruments so far had to be done with manually controlled gear or expensive dedicated IC test setups," says Jürgen Brettel, product manager at the German HP facility.

The most significant features are the instrument's fast variable rise times ranging from 1.3 ns to 900 μs, measured between 10% and 90% of amplitude. That, Bettel notes, is important in production for evaluating integrated circuits under worst-case conditions and for testing high-speed ECL or TTL for propagation delay, as well as for testing setup and hold times—that is, where fast clean pulses are needed. Rise time can be varied to meet different ICs' specific requirements: 1.5 ± 0.2 ns, for instance, or 2.0 ± 0.2 ns.

The 020 option gives the 8161A an independent second channel. It is possible to use one or both channels in the double-plus mode, adding both channels or complementing them individually. With such flexibility, complex staircase-shaped waveforms with up to four voltage levels can be generated.

Also, through the "A plus B" channel mode, the option permits glitch and noise simulation, which should come in handy in testing high-frequency components. Since the two channels operate independently of each other, a glitch can be located anywhere within the base period. The glitch width can be set to as little as 4 ns.

Resolution. The 8161A, which has a variable output voltage of up to 5 V into a 50-Ω load, boasts a high timing resolution: 100 ps for all timing parameters like pulse delay, period, width, and double-pulse spacing as well as rise times.

Further enhancing the instrument's versatility are counted burst and synchronous gate capabilities as well as a 125-MHz repetition rate in the double-pulse mode. In addition to normal triggering, there are external triggering modes.

Versatility is combined with flexibility: the repetition rate can be set

New products

to within 2% and both the pulse delay and pulse width to within 1% ± 1 ns of the desired values—a characteristic especially handy for work with high-speed logic, Brettel points out. A high measured-value reproducibility is ensured because of the instrument's good repeatability. The latter is twice as good as the accuracy, or to within between 0.5% and 1% for all timing parameters.

Not to be overlooked is the instrument's wide operating temperature range. Extending from 0° to 50°C, it guarantees reliable and accurate operation in system or rack applications, where one instrument tends to heat up another.

The 8161A includes the popular IEEE-488 interface bus for precise and speedy programming in automatic testing and provides easy keyboard entry in manual operation. "Users can quickly familiarize themselves with the instrument because program instructions closely follow the procedures for manual operation," Brettel explains. Threshold and other critical values can be set with vernier controls for rapid manual adjustments. The learning mode makes for error-free transfer of critical values to the computer and the automated test system.

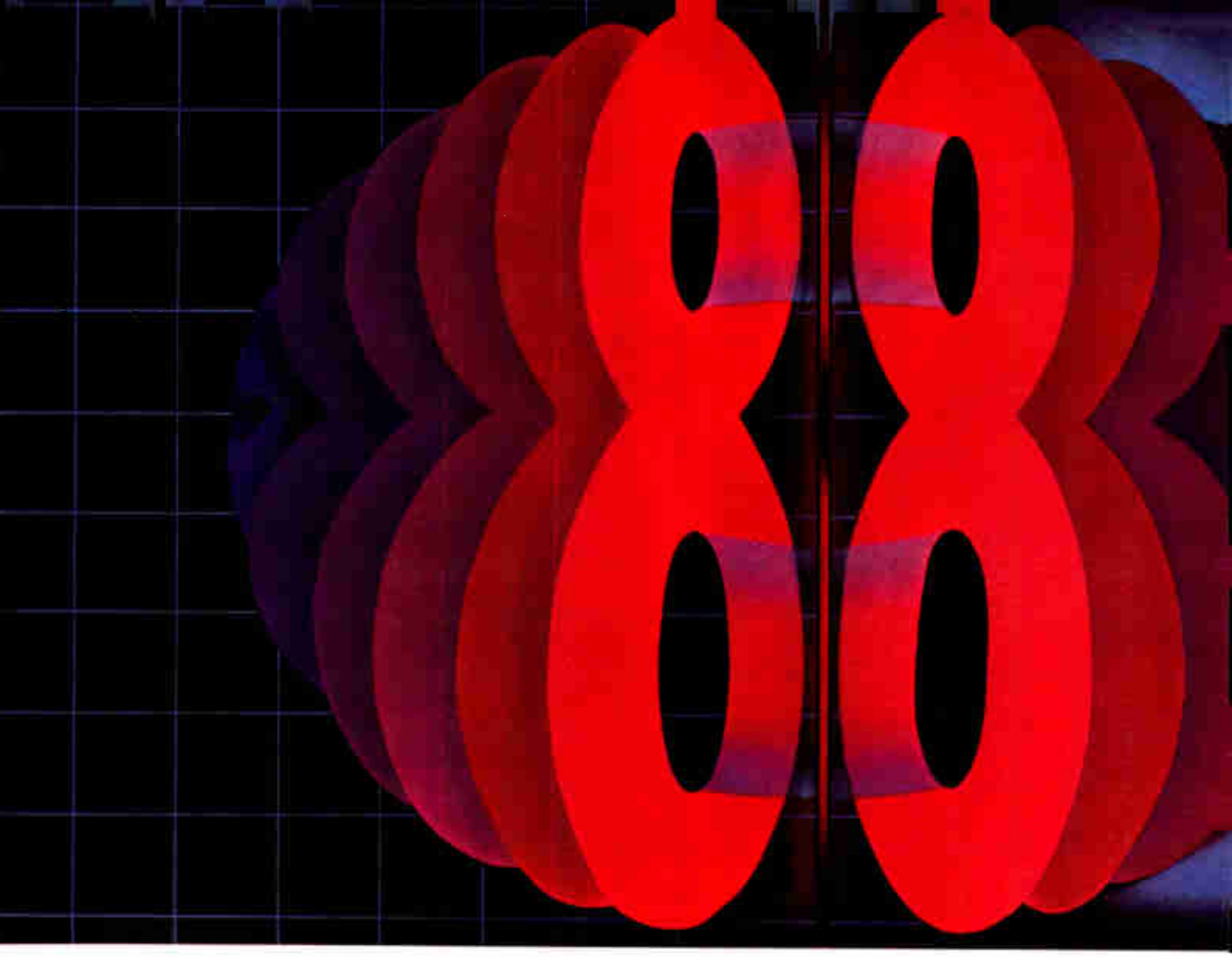
A nonvolatile memory in the 8161A stores nine complete sets of programmable parameter and mode setups, ensuring repeatable results. A hardwired set of parameters provides a handy starting waveform.

Error catcher. When a parameter is entered into it, the instrument checks the parameter's compatibility with other settings or checks if its values exceed specified limits. In case of an error or incompatibility, a front-panel display shows whether the cause is improper slope, level, or timing or if an inappropriate parameter has been set.

The basic 8161A carries a price tag of $14,940 in the U. S. The 020 option, the integrated second channel, adds $6,590 to the basic price. Delivery time is 12 weeks.

Hewlett-Packard Co., 1501 Page Mill Road, Palo Alto, Calif. 94304 [338]

Hewlett-Packard SA, P. O. Box, CH 1217 Meyrin 2, Geneva, Switzerland [339]



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Intel's latest HMOS processor and peripheral introductions plus extensive development and software support now expand the universe of 8-bit applications.

Ever since Intel introduced the first 8-bit microprocessor in 1972, we've been the industry leader. We've always been committed to staying on the leading edge of 8-bit technology. That's what enabled Intel to be first in introducing a wide range of components, most of which are now industry standards. Today, we're continuing to apply this innovative technology both to develop new 8-bit products and to reduce costs and improve performance of existing ones.

Even more importantly, Intel always designs 8-bit parts to be members of a family of products, so they evolve in an orderly progression, as the technology evolves. By *planning* for technological change, we've been able not only to improve product performance, but to extend product life-cycles and thus protect our customers' investments. That's the real reason why today Intel is the leading manufacturer of 8-bit microprocessors.

Expanding the 8-bit universe

For microprocessors, the greatest cost reductions and performance improvements have resulted from breakthroughs in *technology*—not volume production techniques and automation. That means breakthroughs such as Intel's advanced HMOS.*

This technology enables us to put more power and more functions on a smaller chip, and offer a range of devices that do more, while shrinking the price-performance ratio.

At the high-performance end of the 8-bit spectrum, for example, consider the new 8-bit champion: the iAPX 88. This state-of-the-art HMOS microprocessor outperforms its closest competitors in memory efficiency, ease of programming, and throughput—by as much as 4 to 1. It's also the only 8-bit microprocessor that addresses up to 1 million bytes of memory—without external memory management. And since the 8088 is the only 8-bit microprocessor whose instruction set is compatible with a 16-bit device, it's the only way you can move up to 16-bit power—such as the iAPX 86's—without sacrificing your software investment.

Or consider Intel's latest, highly integrated solution to design problems that previously required multiple chips: our new microcomputer hero, the 8051. This single-chip device contains twice as much program and data memory as

competitive parts; provides up to 10 times as much speed as the 8048; and offers a unique Boolean processor — particularly important in controller applications.

iAPX 88 Performance Comparisons

	iAPX 88	Z-80	MC6809	8085A
Relative performance	1 (5MHz)	3.4 (4MHz)	0.6 (2MHz)	0.3 (3MHz)
16-bit object code compatible	8086	NONE	NONE	NONE
Relative assembly language code required	1	1.5	1.4	1.5
Memory/IO address space	1 Megabyte/ 64K	64K/256	64K/NONE	64K/256
Multi & co-processing	YES (with 8087, 8089)	NO	NO	NO
PASCAL, PL/M & FORTRAN	YES	NO	NO	YES
ICE symbolic debugging	YES	NO	NO	YES

Shrinking the 8-bit world

As part of a long-range plan to apply advanced HMOS technology to our existing products, we've developed versions of numerous parts that deliver greatly enhanced price-performance. Take our industry-standard 8048, for example. The new 8048H versions of this single-chip microcontroller now offer up to 80% more speed, at 67% less power. Other established Intel® 8-bit parts — like the 8085A — show similar price-performance improvements.

The key to these breakthroughs is our second-generation HMOS technology. That, combined with our pioneering computer-aided design techniques, allows transparent process conversions. Since our strategic design program allows us to plan for die-size reductions at the time of original design, we can make subsequent process conversions via CAD software, rather than having to re-design. Thus we can produce faster, lower power, less expensive devices — like the 8048H and 8085AH — while keeping identical circuitry and layouts.

The net result of these improvements is that your existing products can now evolve as Intel's technology evolves. Right now, you can improve your existing designs while lowering costs, thus extending the life cycles of your products and boosting profit margins.

Intel's Built-in Die Shrinkage Steps

Technology Impact on 8-bit Products (The 8049)

Technology	NMOS	HMOS	Advanced HMOS
Introduction	1977	1980	1982
Relative Area	1.00	0.67	0.42
Relative Cost	1.00	0.55	0.40

Improved HMOS processors, however, constitute only a few points on the Intel 8-bit horizon. We've also used HMOS technology to enable our peripherals to cover a wide range of applications, from the 8274 multi-protocol serial controller, through the 8272 double-density floppy disk controller, to the 8741A universal peripheral interface, with on-chip EPROM memory. By doing more, these devices off-load your CPU, and increase system throughput.

HMOS also lets us build memories with a wide range of density and speed characteristics — from 16K statics through 64K dynamic RAMs, to a family of EPROMs ranging from our 2732A to our new E²PROM, the 2816. HMOS gives you the same flexibility in memory design that you have in designing other parts of your system.

Turning the competitive world around

When you want to make immediate use of the latest 8-bit VLSI technology at the board level, Intel has the solution. Our iSBC 88/25™ and iSBC 88/40 single board microcomputers, for example, will let you prototype systems or fill low- to medium-volume production requirements rapidly. And they're only two out of eight single board microcomputers for you to choose from.

Then too, when you'd rather concentrate on your product than on re-inventing the wheel, Intel offers two 8-bit real-time operating systems: the iRMX/80™ and iRMX/88. These operating systems are ideal for 8-bit designs, where memory space and response time are often critical. They require only 2K to 4K bytes of memory, and the iRMX/88 operating system is capable of providing up to 6000 samples per second in your real-time application.

Finally, to speed development time, we offer a full complement of development support tools. Such as the latest development system technology, the new Intellec® Series III. With its dual processor architecture, the Series III is ideal for 8088 development work. Then there's the Series II, and the new, low-cost Model 120 — the choice for entry level 8085 or 8048/8049 microcontroller designs. As part of a planned path to protect your investment, both the Series II and the Model 120 are upgradable to the Series III, and further to the NDS-1 development network. And, by applying the same computer-aided design techniques we use to shrink our chips, we're also able to build bond-out chips for use in our ICE™ in-circuit emulators. So our ICE modules perform exactly the same way in your circuit as the original chip. Plus they're ready to go, as soon as a new chip is available.

To further reduce development time and enhance programmer productivity, Intel supports these hardware systems with the broadest range of development software available today. Up to five language translators, including Pascal, PL/M, FORTRAN, COBOL, and BASIC. Four different macro-assemblers. An extensive set of programmer utility routines. So you can always match the right language or program to the job — and offer your customers a way of further developing your products if they wish.

All of which means that now it's easy, convenient and cost-effective to get the most out of Intel's 8-bit world of advanced technology. And make your product design possibilities almost infinite. With these technology advantages, this degree of commitment to 8-bit users, this breadth of product line, and this level of development support, it's no wonder the 8-bit world is turning to Intel's HMOS.

Our new brochure gives further details on Intel's 8-bit world. You can get your copy by circling the reader response number, or contacting your Intel sales office/distributor. Or writing Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Telephone (408) 987-8080.

*HMOS is a patented Intel process.

Europe: Intel International, Brussels, Belgium
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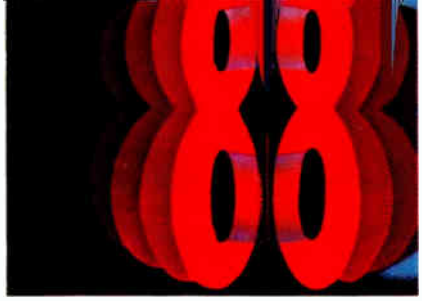


The New World of Intel's 8-Bit HMOS

Intel's 8-Bit Microprocessors and Support

Microprocessor	Replaces	Description	Evaluation Kits	In-Circuit Emulators
8048H/8748 8048L	8048	**Microcontroller** New 11 MHz and 8 MHz CPU speeds; up to 70% lower power; on-chip EPROM at new lower price	PROMPT-48	ICE-49™
8049H/8749 8049L	8049	**Microcontroller** Same speed selections as 8048H; now available with 2K byte on-chip EPROM		ICE-49™
8051/8751	NEW	**Microcontroller** Intel's newest high integration micro with on-chip serial port; Boolean processor; 12 MHz CPU and 4K byte on-chip EPROM	SDK-51™	ICE-51™
8080A		**Microprocessor** Intel's original 8-bit processor, recently upgraded	SDK-85™	ICE-80™
8085AH	8085A	**Microprocessor** 30% lower power; 10% voltage margins; new high performance 6 MHz version	SDK-85™	ICE-85™
8088	NEW	**Microprocessor** Highest performance 8-bit CPU; 1 Mbyte address range; 16-bit instruction set; multi-processor support	SDK-86™	ICE-88™
iSBC 88/25	NEW	**Single Board Computer** 8088-based, with Multibus™ expansion, coming mid '81		
iSBC 88/40	NEW	**Single Board Computer** 8088-based measurement and control computer		

Intel's 8-Bit Peripheral Controllers

Model	Replaces	Description
8202A		**Dynamic RAM Refresh Controller** Makes dynamic RAM look static, handles refresh, address multiplexing and arbitration
8272	NEW	**Double/Single Density Floppy Disk Controller** Interfaces 8- or 16-bit CPU to four floppy disk drives; IBM-compatible formats
8274	NEW	**Multiple Protocol Serial Controller** Speeds up to 1M baud; protocols can be async, bisync or synchronous (HDLC/SDLC)
8276	NEW	**Small System CRT Controller** Allows complete CRT system implementation with less than 20 devices
8041AH/ 8741A	8041A	**Universal Peripheral Interface** Controllers with new 12 MHz and 8 MHz CPU versions; slave processor interface
8232	NEW	**Floating Point Math Processor** Four function 64-bit floating point operation; IEEE compatible; 4 MHz clock
8291, 8292		**IEEE-488 GPIB Controller** Talker/listener and controller functions for 500K bytes/sec data transfer

Intel's Hardware/Software Support

Support		Description
Intellec® Model 120	NEW	**Development System** New price/performance breakthrough; gives small program development capabilities including ICE™ support at lowest cost for 8-bit microcomputers; also acts as editing station for NDS-1
Intellec® Series II		**Development System** Versatile; provides support for Intel's entire 8- and 16-bit product lines, including high-level languages and ICE in-circuit emulators
Intellec® Series III	NEW	**Development System** High performance; two host processors to support Intel's entire 8-and 16-bit microprocessor family; resident 8088 Pascal, FORTRAN, PL/M, and assembler; compatible with hard disk
Intellec® NDS-1	NEW	**Network Development System** Provides distributed support for multiple 8- or 16-bit projects; offers shared file access, high-speed compilation, and low-cost debugging; coming mid '81
ICE™ Emulators		**In-Circuit Emulators** Detect design flaws; perform real-time hardware/software symbolic debugging, even in the most complex systems; versions available for all 8-bit processors
ASM™		**Macroassemblers** Available for every Intel 8-bit processor
PL/M Pascal		**System Implementation Languages** Available for system software development
Pascal FORTRAN COBOL BASIC	NEW	**Application Languages** All four languages for 8085AH application programming; Pascal and FORTRAN for the 8088; all available now
iRMX/88™ iRMX/80™	NEW	**Real-Time Operating Systems** User configurable, for 8088 and 8080A/8085AH; major facilities include: priority-based resource allocation; real-time clock; interrupt handling; task dispatching

Europe: Intel International, Brussels, Belgium.
Japan: Intel Japan, Tokyo. United States and Canadian distributors: Alliance, Almac/Stroum, Arrow Electronics, Avnet Electronics, Component Specialties, Hamilton/Avnet, Hamilton/Electro Sales, Harvey, Industrial Components, Pioneer, L.A. Varah, Wyle Distribution Group, Zentronics.

intel delivers solutions

Circle 199 on reader service card

Components

Laser-trimmed ICs sense temperature

Chips need be calibrated only at the factory, have two reference outputs

Monolithic temperature sensors cost less than conventional electrical sensors but for high accuracy must generally add components and other resources to calibrate zero and full-scale end points. A family of single-chip temperature transducers from Intersil are "simpler, yet highly accurate, digital thermometers," claim its developers.

Designated the ICL8073 and −8074, the new bipolar temperature transducers include all the necessary offset and reference voltages, thus "eliminating the need for potentiometers and other external components typically employed when calibrating currently available temperature sensors," states Larry Goff, design engineer for analog research and development at Intersil. The temperature-sensing devices can be plugged directly into any number of available analog-to-digital converters, he adds, for a factory-calibrated direct temperature readout in any of the normal scales—Kelvin, Fahrenheit, or Celsius.

According to Goff, "the days of laborious calibration requiring equipment and manpower are gone forever. Digital temperature control, differential temperature measurement, analog temperature control, and more can be accomplished with no external components and absolutely no calibration."

Each of the new devices has three outputs. The first is proportional to absolute temperature in kelvins, similar to other monolithic temperature sensors, such as those offered by National Semiconductor, Motorola, Analog Devices, and Intersil, among others. However, a second output in the devices is a constant, the offset voltage: it is exploited to convert to the Celsius scale (in the case of the ICL8073) or to the Fahrenheit scale (ICL8074). The third output is a reference voltage for a-d conversion.

Using an ICL8073 or -8074 with Intersil's ICL7126 single-chip 3½-digit integrating a-d converter, for example, and a standard 9-v transistor radio battery "forms a temperature measurement system with a battery life in excess of six months," Goff says. He notes that each of the calibrated temperature transducers consumes 50 μA typically (200 μA maximum), about one sixth the power of the popular AD590 temperature transducer made by Analog Devices and Intersil.

Gradations. The 8073 and 8074 are laser-trimmed for accuracy and interchangeability. The absolute accuracy, which covers the offset voltage (V_{os}), reference voltage (V_{ref}), and voltage proportional to absolute temperature (V_{ptat}), is different for each of three grades of parts (I, J, and K) in each of three classes (commercial, industrial, and military). In the case of the ICL8073, the levels of absolute accuracy are ±5.0°, ±3.0°, and ±1.5°C, respectively. For the ICL8074, those accuracy specifications are ±9.0°, ±5.4° and ±2.7°F, for the I, J, and K grades, respectively. The worse-case interchangeability error equals the worst-case guaranteed error, which can be as little as ±1.5°C or ±1.8°F.

Both the 8073 and 8074 are available in a TO-71 package with six leads for full-function operation, as for a digital thermometer capable of 0.1°C resolution. The two types of temperature transducers also are available in plastic TO-92 or hermetic TO-52 packages, each of which has only three leads. The lower-cost, three-leaded devices have only one output voltage (V_{ptat}). "They are intended for those applications, such as temperature controllers, where it isn't necessary to know the temperature relative to absolute temperature (kelvins), but only the ratio with respect to degrees Celsius or Fahrenheit," Goff states.

The temperature-sensing ICs operate from a wide power-supply range, 2.7 to 30 v. Both the operating and storage temperature ranges of the two device types are −100° to +150°C. Nonlinearity is rated at a maximumn 0.5 K, and long-term stability is 20 parts per million per month.

At the 100-piece level, the commercial, full-function ICL8073 and -8074 are $3.10 each. The controller versions are priced at $2.45 each in like quantities. The premium for upgrading from the commercial to the industrial grade and from the industrial to the military is approximately 25% to 30% in each instance. Availability is 30 days after receipt of order.

Intersil Inc., 10710 N. Tantau Ave., Cupertino, Calif. 95014. Phone (408) 996-5000 [341]

58-key keyboard has low, 0.400-in. profile

A keyboard panel that meets European safety requirements, the model MK 058-001, is only 0.400 in. high—a low profile that should be useful in portable and desktop equipment like home computers, desk-top terminals, telephones, and portable and laboratory instruments.

The MK 058 gives the operator a tactile feedback and has a 0.060-in. travel for a faster throughput. It can be mounted from the front of an enclosure or flat panel via eight male-mounting studs. All of its 58 keys are enclosed and protected from the environment to extend its life. Legends, which are graphically applied, may be placed on the bezel for advanced styling or added to the buttons for more than one operating mode. The keyboard has a 2-Ω contact resistance, an eight-by-eight

array of switches for easy scanning by a microprocessor, and keys requiring a 2.8-oz force for actuation.

The keyboard panel is priced at $37.00 in quantities of 1,000 in off-the-shelf designs. Delivery is from stock. Custom-made keyboards are readily available. Matching numeric and hexadecimal keyboards will soon be available for the MK 058 family.
Advanced Input Devices, P. O. Box 1818, Coeur d'Alene, Idaho 83814. [343]

Monolithic op amp has high speed and low noise

An integrated circuit operational amplifier offers a peak-to-peak noise of only 80 nV in low-frequency instrumentation applications and 3 $nV/Hz^{1/2}$ in audio-frequency stages, an offset voltage of 10 μV, a slew rate of 3.2 V/μs, a bandwidth of 8 MHz, and a long-term drift of 0.2 V per month. These characteristics combine to make this device unique in the industry, says the manufacturer. At 10 Hz the OP-27/37 exhibits a typical input noise density of 3.6 $nV/Hz^{1/2}$ which drops off to 3.1 at 30 Hz and 3 at 1 kHz. It has a typical power consumption of 90 to 100 mW, and input noise current density of 1.7 $pA/Hz^{1/2}$ typically, and 4 $pA/Hz^{1/2}$ maximum at 10 Hz and 0.4 $pA/Hz^{1/2}$ (typical) and (maximum) 0.6 $pA/Hz^{1/2}$ at 1 kHz.

Available in eight-lead, dual in-line packages and eight-pin TO-99 cans, the OP-27/37 has a −55° to +125°C or 0° to 70°C temperature range. In quantities of 100 and up, the op amps range in prices from $5.00 to $50.
Precision Monolithics Inc., 1500 Space Park Dr., Santa Clara, Calif. 95050. Phone (408) 246-9222 [344]

Power-MOS-FET 'relays' need only 500 μA for control

A series of ultrasensitive, optically isolated, power MOS field-effect-transistor solid-state relays, the

Light-torque rotary switches make the LM-3.5A DMM as easy to operate as it is to carry.

On a benchtop or a belt, over a shoulder or in a tool kit, the LM 3.5A DMM, and its LCD counterpart, the LM-350, are ready to go when you are.

Convenience. That's the key to Non-Linear Systems' best-selling LM-3.5A. A high-performance, competitively-priced, all-purpose mini DMM. Convenience from light-torque rotary switches. So operation's a cinch. Convenience from bold, bright LEDs. For instant, accurate, numeric answers. Unlike some competitive meters, the LM-3.5A features both vertical and horizontal readings. And an optional leather carrying case with belt loops and shoulder strap assures hands-free operation.

At 9.2 oz., the LM-3.5A is portability at its best. There's more. The LM-3.5A is a 3½-digit DMM. Features 2,000 counts per range—100% over-ranging. Result? Increased accuracy and resolution between readings of 999-2,000. It also reduces the amount of range shifting when measuring near 1,000.

Troubleshooters swear by it. Repairmen find the LM-3.5A works wonders on tvs, business machines, even cameras. Checks all quiescent AC and DC voltage values. Spots current drains. Measures the resistance of suspect components. Quickly and precisely.

Other DMMs to match your needs. The LM-3.5A is just one in a full series of 3 to 4-digit DMMs. If you need LCD convenience for measurements outdoors, we market the LM-350, among others. You don't pay for true RMS capabilities you don't need. But if you do need true RMS readings, Non-Linear Systems can oblige.

FM-7. The bantam frequency meter. Portability teams with performance in the FM-7. The smallest, 7-digit, 60-MHz, battery or AC line-operated instrument available.

Operator convenience is the key to our line of frequency and temperature meters, too. Pictured left to right, SC-5 prescaler, FM-7 frequency meter, LED format LT-3 digital temp meter, and its LCD cousin, the LT-31. Top, the MLB-1 digital logic probe.

Hobbyists, radio and tv studios, phone companies and the military all depend on the versatile FM-7. Whether the job calls for calibrating fixed, variable frequency or voltage-controlled oscillators, checking flowmeters, high-speed photocell counters, or setting the IF or heterodyne frequency in communications equipment, the FM-7 is a standout performer.

SC-5 Prescaler. Top range booster. This 512-MHz, battery or AC line-operated prescaler was developed to extend the frequency range of the FM-7 from 60 to 512 MHz. Adapts to most other frequency meters, too.

LM-3.5A at a glance.

DC Volts	1 to 1,000, 4 ranges
AC Volts	1 to 750, 4 ranges
Kilohms	1 to 10000, 5 ranges
AC/DC Current	1 mA to 1A, 4 ranges
Polarity Selection	Automatic
Readout	0.3" Red LED
Size	1.9" H x 2.7" W x 4.0" D
Weight	9.2 oz (batteries installed)
Power	3 type AA rechargeable Nicad batteries and charger
Price	$165.85

LT-3 Digital Temp Meter. Featuring 0.1° resolution and high accuracy, the 3½-digit, 2,000 count full scale LT-3 is indispensable for home or industry. Checks everything from thermostats to appliances. Even monitors critical operations like photoprocessing and electroplating.

The LT-3 can be supplied with any of eight thermistor and RTD temp sensors to read ranges of 0-100°C, 32-199.9°F, or 0-199°C or F.

Work outdoors? Then the LT-31 (LCD format) is the ticket.

Get the word on us. We offer a full lineup of convenient, competitively-priced products. From DMMs, frequency and temp meters to miniscopes and DPMs.

For further technical information or the names of your nearest distributors, contact Non-Linear Systems Inc., 533 Stevens Ave., Solana Beach, CA 92705. Telephone (714) 755-1134. TWX 910-322-1132.

Non-Linear Systems, Inc.
Specialists in the science of staying ahead.

Circle 203 on reader service card 203

New products

OFM-21, -22, -23, and -24 series, operate on a dc input control current of less than 500 μA for complementary-MOS drivers or low-level battery circuits. They can switch ac or dc voltages at levels up to 300 V and currents to 750 mA. Because of the units' FET output, they do not exhibit a voltage or thermal offset. As a result, voltages as low as 10 μV can be switched at currents from nanoampere levels up to full rating.

Housed in either miniature six-pin dual in-line or single in-line packages, the units can be used in telecommunications and computer applications and to replace reed relays. In quantities of 1,000, the ac and dc solid-state relays range in price from $5 to $5.95 depending on rating. Delivery is two to four weeks after receipt of order.

Theta-J. Corp., 208 West Cummings Park, Woburn, Mass. 01801. Phone (617) 935-7600 [345]

0.1- to 3.3-F capacitors are rated at 5.5 WV dc

Rated at 5.5 WV dc with capacitance ratings of 0.1, 0.33, 1.0, and 3.3 F, a new series of miniature electrolytic capacitors measure only 1⅝ by 1⅝ by ⅝ in. They are designed to be used in solid-state memory backup driven by a 5-V (±10%) power supply or in long-time-constant circuitry, driving relays, solenoids, and other pulsed actuators. They come in rectangular packages instead of the cylindrical ones of the original Gold Capacitor series, which are rated at a lower 1.6 and 5.0 WV dc.

They have an operating temperature of −25° to +70°C, a capacitance tolerance of −20% to 40%, an internal resistance (impedance) of 1 Ω maximum at 1 kHz at 20°C, and a maximum leakage current of 1 mA after operating for one hour at rated voltage at 20°C. The failure rate is just 1% after 50,000 hours at a rated voltage at +40°C.

Deliveries of Gold Capacitors are from stock to 12 weeks.

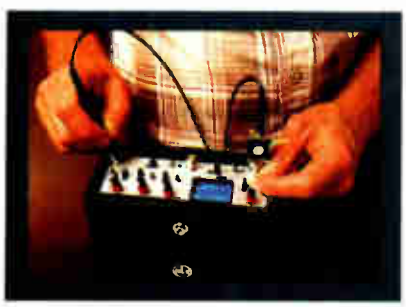
Panasonic, One Panasonic Way, Secaucus, N. J. 07094 [346]

Problem:
Build an oscilloscope light enough to carry in the field, yet sophisticated enough to use in the repair shop. And bring it in at under $650.

Solution:
Non-Linear Systems' MS-230. A 3 lb. 10 oz. miniscope.

At 3 lbs. 10 oz., the MS-230 is the lightest miniscope around. Now you can take the scope to the problem. Or bring the problem to the scope.

It's easy to get carried away with the MS-230. Our remarkable 30-megahertz, battery-operated, dual-trace miniscope. At 3 lbs. 10 oz., it's the smallest, lightest miniscope in the field today. Suddenly, portability's not a problem anymore.



On a benchtop or a belt, over a shoulder or in a tool kit, the MS-230's ready to go.

Sets up shop. Makes housecalls. The state-of-the-art MS-230 is at home anywhere there's a need to accurately test or measure electronics equipment.

TV repairmen find it works wonders in the field. Tuck it in the tool kit, sling it over a shoulder or slip it on a belt, and it's ready to make a quick on-site diagnosis.

It's a great benchmate in the shop, too. Checks distortion, compares circuit inputs and outputs, finds faulty components. All with equal ease. And the MS-230 is so compact it doesn't clutter up the work area.

What's more, the versatile MS-230 is perfect for servicing microcomputer systems, maintaining avionics equipment and diagnosing sophisticated medical equipment.

A trio to pick from. If your work demands an oscilloscope that handles virtually all normal applications with unblinking accuracy, we've got your number. The MS-230. A superb value at $649.00.

We also make miniscopes to match other budgets and needs. Take the MS-215, for example. It's a 15 MHz, dual-trace scope priced at $497.00. Or the MS-15, 15 MHz, single-trace at $389.00.

And each model is available with optional accessories to help you get the job done. Like a 10:1, 10 megohm probe and leather carrying case with shoulder strap and belt loop.

When it comes to portable, affordable, accurate miniscopes Non-Linear Systems leads the way.

MS-230 at a glance

Vertical Bandwidth:	30 MHz
Deflection Factor:	10 mV/div to 50 V/div, 12 calibrated ranges
Input Impedance:	1 megohm in parallel with 50 pF
Time Base:	0.05 nSec/div to 0.2 Sec/div, 21 calibrated ranges
Horizontal Bandwidth:	200 kHz
Trigger Modes:	Automatic, Internal, External and Line
Power Sources:	
Internal:	Rechargeable lead acid batteries
External:	115 VAC or 230 VAC, 50-60 Hz via plug-in transformer
Size:	2.9" H x 6.4" W x 8.6" D (74 mm x 163 mm x 218 mm)
Weight:	3 lbs. 10 oz. (1.65 Kg)

Get the word on us. Non-Linear Systems has been intelligently innovating in the digital testing industry for nearly three decades. From the introduction of the first digital voltmeter to breakthrough products like the MS-230.

Today we offer a full line of competitively-priced, state-of-the-art equipment. From miniscopes, digital voltmeters, digital panel meters and counters, to frequency meters, logic probes, line-frequency meters and pre-scalers.

Our entire lineup is available now from top electronic distributors throughout the world. Contact your local distributor today.

For further technical information, or the location of your nearest distributors, contact Non-Linear Systems, Inc., 533 Stevens Ave., Solana Beach, CA 92705. Telephone (714) 755-1134. TWX 910-322-1132.

Non-Linear Systems, Inc.
Specialists in the science of staying ahead.

Circle 205 on reader service card

THE NEWEST COMPUTER EQUIPMENT BY INVITATION ONLY.

In one day...in your city...in England, Germany, The Netherlands, France and Italy...You can get a close-up view of the latest in computer and peripheral equipment from 30 of the world's leading manufacturers. It's all there at the Invitational Computer Conference, the only international seminar/display designed specifically to meet the requirements of the quantity user.

The unique Invitational Computer Conference one-day seminar/displays have proven extremely effective and popular with OEMs for the past eight years in the United States. Now, the series is extended to promote the exchange of technological advances between the computer communities of the world.

Attendance at the ICCs is by invitation only. So, if you are a manufacturer of computer equipment, integrator of computer equipment into systems for resale, or volume user, the Invitational Computer Conference is for you. Don't miss the opportunity to attend when the ICC is in your region. Invitations are available from participating companies or the ICC sponsor.

The schedule for the 1981 International Series is:

London, England	**March 17, 1981**
Munich, W. Germany	**March 24, 1981**
Frankfurt, W. Germany	**March 26, 1981**
Amsterdam, The Netherlands	**November 5, 1981**
Paris, France	**November 12, 1981**
Milan, Italy	**November 17, 1981**

Some of the companies which will be participating in the International Series will be: Century Data Systems, Charles River Data Systems, Cipher Data Products, Control Data Corp., Dataram, Genisco Computers, International Memories, Inc., Lear Siegler, MDB Systems, MFE Corp., Monolithic Systems, Perkin-Elmer, Priam Corporation, Printronix, Remex, Rianda Electronics, Tektronix.

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The Invitational Computer Conference International Series

Here's an inexpensive way to give your existing products a face lift.

Our new snap-in pushbuttons fit standard rocker switch mounting holes. And they're available now, so you can use them to enhance your panel design *without costly restamping or re-cutting of the face panel.*

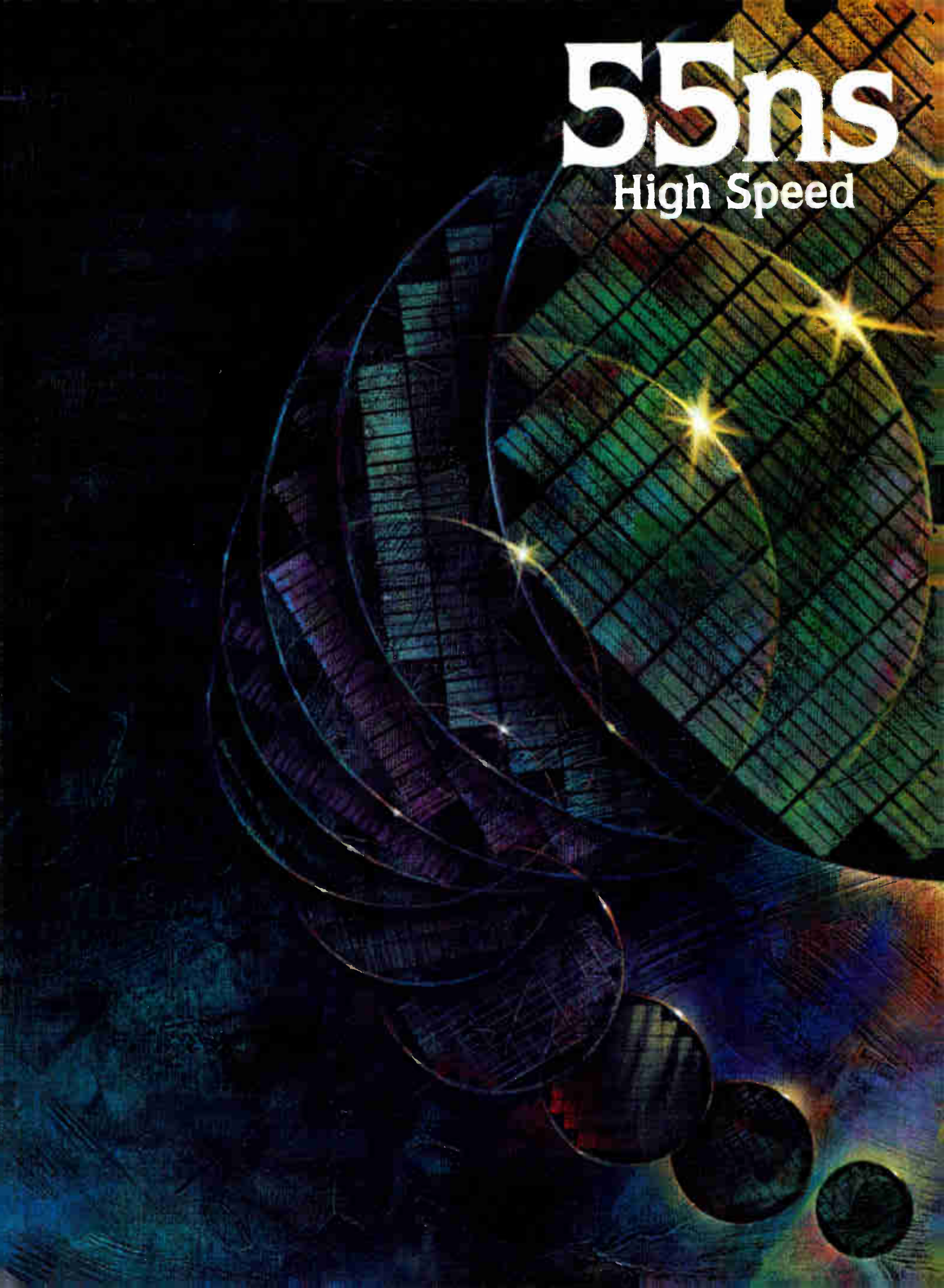
These new pushbuttons are available with all the circuits, terminations and ratings found in our standard rocker switch line. Actuators can be hot-stamped, illuminated or color-coded to meet every need.

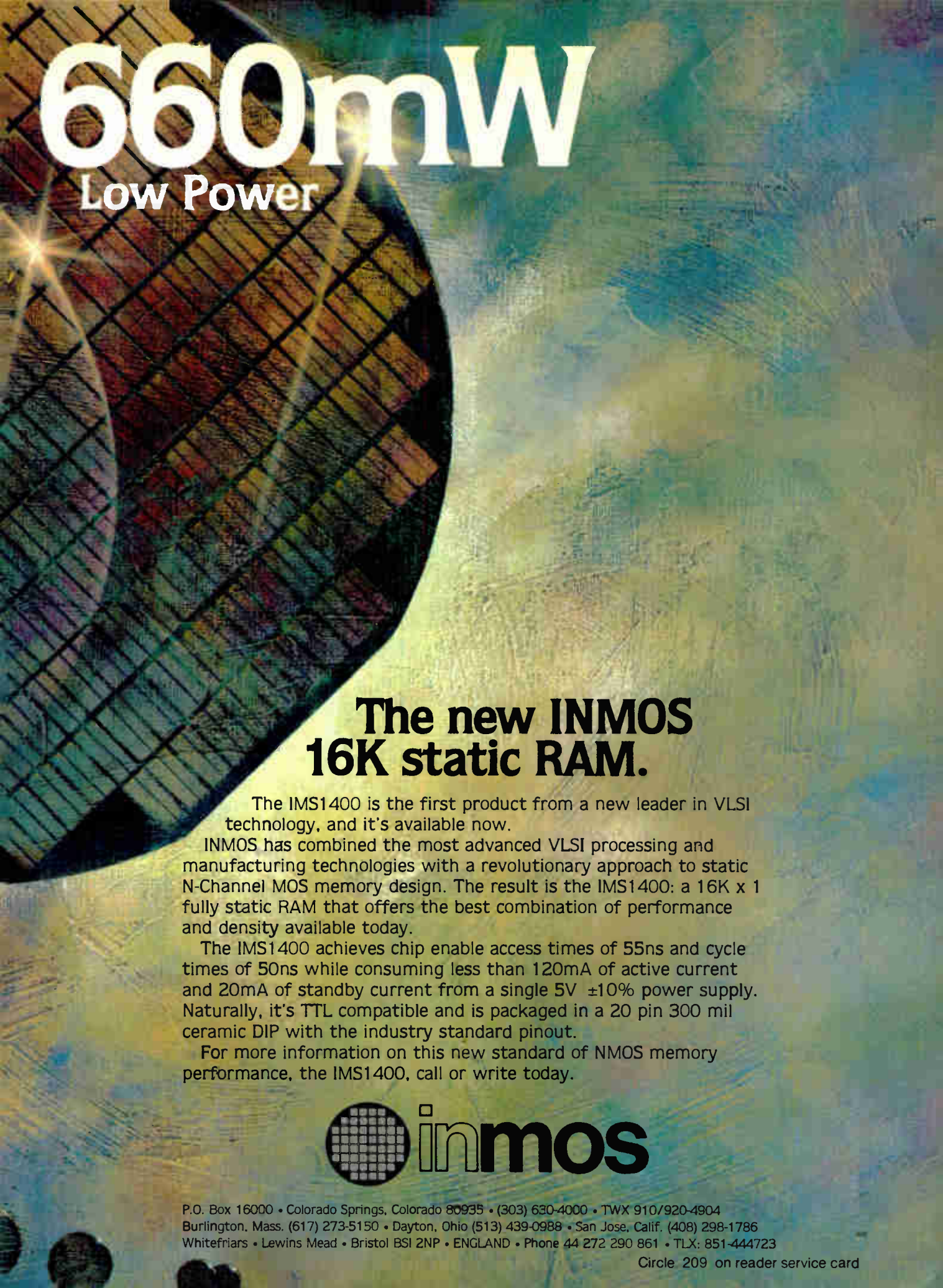
For more information, contact your Cutler-Hammer salesman or switch distributor. Or write for our new catalog of commercial switches. Eaton Corporation, Commercial Controls Division, 4201 N. 27th St., Milwaukee, WI 53216.

Snap our new Cutler-Hammer pushbutton into your plans. The switch is easy.

EATON
Electrical/Electronic Control

Circle 207 on reader service card


55ns
High Speed



The new INMOS 16K static RAM.

The IMS1400 is the first product from a new leader in VLSI technology, and it's available now.

INMOS has combined the most advanced VLSI processing and manufacturing technologies with a revolutionary approach to static N-Channel MOS memory design. The result is the IMS1400: a 16K x 1 fully static RAM that offers the best combination of performance and density available today.

The IMS1400 achieves chip enable access times of 55ns and cycle times of 50ns while consuming less than 120mA of active current and 20mA of standby current from a single 5V ±10% power supply. Naturally, it's TTL compatible and is packaged in a 20 pin 300 mil ceramic DIP with the industry standard pinout.

For more information on this new standard of NMOS memory performance, the IMS1400, call or write today.

inmos

P.O. Box 16000 • Colorado Springs, Colorado 80935 • (303) 630-4000 • TWX 910/920-4904
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Circle 209 on reader service card

SYSTEMS FLEXIBILITY

Because you want it.

Measurement, Source and Multiplexing Solutions for Your Systems Requirements

Not all systems requirements are the same. That's why Data Precision offers you a choice of instruments encompassing a wide selection of features, options and specifications. All accomplished without those burdensome customizing costs you're so familiar with.

Measurement requirements can be met with a choice of 4½ and 5½ digit multimeters with basic accuracies of .007% and conversion speeds from 2½ measurements/sec. up to 1000/sec. with full 5½ digit resolution. You can choose a dedicated DVM or full function instruments with multiple ratio measurement. Programming can be accomplished through BCD, IEEE-488 or RS232 and resistance measured with either 2 or 4 wire. You can purchase only what you need now and extend your instrument's capability with field installable options later.

Source requirements, both voltage and current, can be met with our programmable calibrator which will generate a different voltage or current level every millisecond (including settling time). Accuracy is 10ppm for voltage and 100ppm for current with outputs of ±100nV to ±100V and ±1μA to ±100mA. Capability can be extended with optional GPIB and ±1000V amplifier.

Multiplexing requirements can be addressed with our 8/16 channel analog multiplexer with automatic, remote, manual and slave scanning modes at rates up to 10 channels/sec. Range is 1μV to 250V.

For additional information or a demonstration contact Data Precision:
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Data Precision Division of Analogic Corporation, Electronics Avenue, Danvers, MA 01923, (617) 246-1600, TELEX (0650) 921819.

Circle #210 for additonal information

Circle #211 for demonstration

Computers & peripherals

Terminal divides screen two ways

Low-cost video terminal separates independent regions vertically and horizontally

A smart video display terminal from Texas Instruments is capable of handling a dozen independent scrolling regions at a time. Its ability to partition the screen into two vertical and six horizontal sections allows operators to compare data easily and will improve data-entry productivity, the firm says.

The first in TI's Opti 900 family, the 940 carries a single-unit price tag of $1,895 in the U. S. This, TI believes, puts the company in a price-performance leadership role in this area of the market. End users, original-equipment manufacturers, and distributors all figure in TI's marketing plans; quantity discounts are available. Hewlett-Packard Co. offers similar features in its 2626A display station, but the price is $3,950 and the display can be split into only four scrolling regions.

The 940, which has 16 programmable function keys, uses a 12-in.-diagonal cathode-ray tube designed with "state-of-the-art ergonomic features to reduce the operator fatigue normally associated with video terminals," says a company spokesman. A combination of double-height and/or double-width characters is standard, to reduce eyestrain. The full 128-character ASCII set is displayed using a 7-by-9-dot-matrix font in a 9-by-11-dot cell to make room for character descenders and underlines.

Separate fields may be defined within each displayed region, a useful feature for data verification work. Fields may be defined to accept only numbers, only letters, or both; a mandatory entry command requires the operator to complete the field before proceeding. Fields may be further defined to automatically tab and send data and also may be protected to prevent the operator from altering data from the host.

The 940 has an RS-232-C interface for asynchronous full- or half-duplex communications at rates from 110 to 19,200 b/s. It also has an output for a printer—it is compatible with the firm's dot-matrix Omni 800 impact printers and Silent 700 thermal printers. Two 256-character buffers are standard to prevent data overflow.

Painless growth. There is room in the 940 chassis for two more boards for options such as extra memory; 1,920- and 5,760-character memory cards are available. The 940's design and its message-based operating system make it possible for new options to be integrated easily, a key to the development of the terminal family, says Rod Canion, manager of terminal systems at TI. Other available options are a tiltable display mechanism, detachable nonglare filters (neutral, amber, and green), an international character set, and a graphic character set for both the keyboard and display.

Custom integrated circuits and the use of gate arrays have reduced the parts count on the chassis and therefore the power and heat dissipated. Power is also conserved by an automatic circuit that turns off the screen if no key is pressed for 15 minutes. The display is reactivated if a key is pressed or if the host sends data to the terminal.

Deliveries of the 940 are scheduled for April.

Texas Instruments Inc., P. O. Box 202145, Dallas, Texas 75220. Phone (713) 373-1050 [361]

Panel-mounted thermal printer includes control, interface

Unlike many stand-alone printers used with microprocessor-based instrumentation systems, most of their panel-mountable counterparts lack built-in interface and control electronics and are only about 20 columns wide so as to save space. But Datel Intersil has designed a low-cost 48-column panel-mounting thermal printer that sits in an 8.4-by-2.92 in. cutout and includes all the necessary electronics.

The model APP-48 5-by-7-dot-matrix printer is compatible with most microcomputers or serial ports that support RS-232-C or 20-

mA current-loop outputs. Only two wires are needed to connect it with the optoisolated current-loop input, and the data rate may be set at 110 to 9,600 b/s.

The APP-48 prints the full 96-character upper- and lower-case ASCII alphanumeric set and stores a second 96-character set of special figures and symbols in internal memory. Both sets are accessed by software control. The built-in microprocessor permits inverted-line printing so that the hard copy reads like a page from a standard typewriter, in addition to the standard instrumentation readout, wherein the first data recorded by the instrument appears at the bottom of the page.

The 6-lb printer includes a dual-voltage 115- and 230-V ac (47- and 440-Hz) power supply. It consumes a maximum of 40 W while printing at a rate of up to 72 lines per minute and 12 W when idling. A 12-V dc power supply can be substituted for the ac unit at no extra cost.

The single-quantity price of the APP-48 is $1,095; discounts for original-equipment manufacturers are available. Delivery takes two to six weeks.

Datel Intersil, 11 Cabot Blvd., Mansfield, Mass. 02048. Phone (617) 339-9341 [362]

Bubble memory cassette stores 256-K of data

A 256-K magnetic-bubble memory cassette from Fujitsu will be available off the shelf by the end of this month for $462.50 per single unit. The system consists of the detachable bubble memory cassette itself (FBM-43CA), a cassette holder (FBM-4002) that includes a linear circuit and sells for $212.50, and an 8-bit parallel controller board (FBC-404C38) that sells for $331.25 and interfaces the memory with the host system's 8-bit bus. Alternatively, for $358.75, the user can buy an RS-232 interface (FBC-404C3S).

Fujitsu America Inc., Component Sales Division, 910 Sherwood Drive-23, Lake Bluff, Ill. 60044. Phone George Neenox at (312) 295-2610 [367]

8-in. Winchester disk drive stores 136 megabytes

Because of a totally new idea for head positioning, the Ontrax Series 8 Winchester disk drive can locate 960 tracks per inch. The density gives it the highest storage capacity available among mini-Winchesters: 136 megabytes. The leader was Fujitsu's 2312 at 84 megabytes.

The new positioner is a digital actuator composed of nine concentric sleeves. These slide within each other and can place a read/write head in 512 discrete locations each 1 mil apart across the disk. By applying current to selected sleeves, any one of the 512 positions can be addressed with a binary number between 1 and 512. For example, to move the actuator to position 11, current is applied to the first, second, and fourth sleeves—the binary number 1011. When the current is removed, a spring returns the sleeve to its rest position.

Three models are included in the new Ontrax Series 8 family: the model 136, which uses two positioners, five platters, and 16 read/write heads to achieve 136-megabyte capacity in 9,600 data tracks; the model 68, which uses two positioners, three platters, and eight read/write heads for a 68-megabyte capacity in 4,800 tracks; and the model 34, which uses one positioner, two platters, and four read/write heads for a 34-megabyte capacity in 2,400 data tracks. Data rate is more than 9.2 Mb/s and data is recorded in an mfm format at 7,158 b/in. Each data formatter in the drive incorporates a 68000 microprocessor, a memory card containing data buffering and processor instructions, a storage port interface, and a communications port interface.

Final prices have not been set, but in original-equipment quantities of 250, the model 136 will be priced at about $4,000. A complete disk subsystem of the same model will go for around $5,500.

Ontrax Corp., 611 Vaqueros Ave., Sunnyvale, Calif. 94086 [363]

GOLD CONTACTS no surcharge

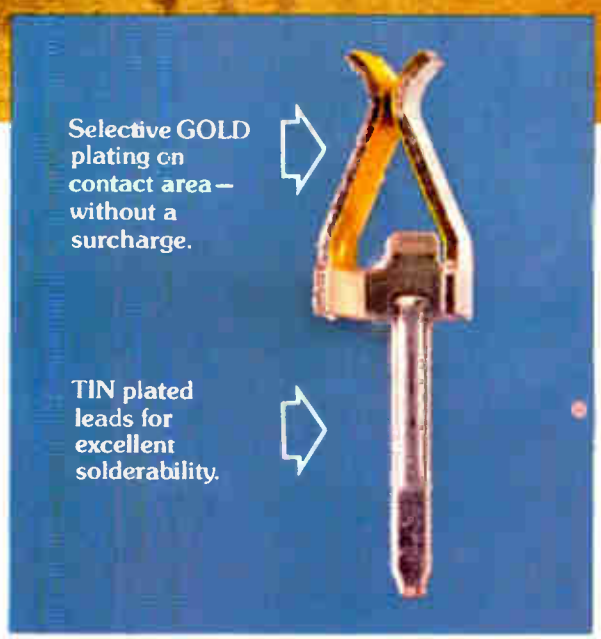
RN "hybrid" DIP sockets give you GOLD where it counts...TIN where you solder.

These RN solder tail DIP sockets are selectively gold plated in the contact area for highest reliability and low contact resistance. And the tin plated leads give you excellent solderability without solder bath contamination.

RN offers what smart engineers want—GOLD PLATED reliability—without the gold surcharge.

RN "side-wipe" contact design assures high reliability for the life of the socket. The gold cannot be degraded in use by the rough edges of the IC lead. Only the flat, smooth side of the IC lead meets the gold contact surface.

These cost-cutting GOLD "hybrid" contacts are available for ALL regular RN DIP sockets—**at very competitive prices—without a gold surcharge.**



Write Today for complete specifications on these "Gold-without-cost" DIP sockets.

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800 East Eighth Street, New Albany, Indiana 47150 Phone: (812) 945-0211 TWX: 810-540-4082

Circle 213 on reader service card

PMI Serves Up A New Data Conversion Plum Cake

The King of DACs Introduces DAC-206, 208, and 210

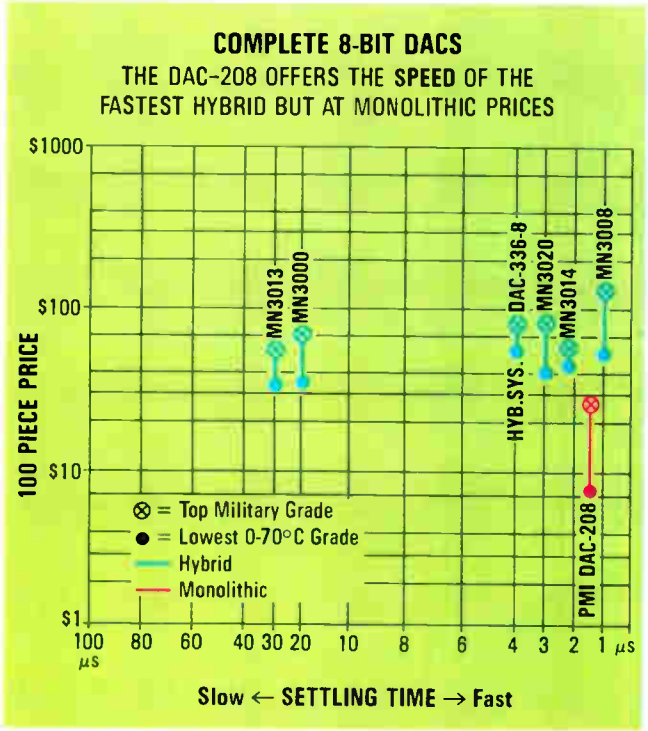
"The Lion and the Unicorn were fighting for the crown:
The Lion beat the Unicorn all around the town.
Some gave them white bread, some gave them brown:
Some gave them plum-cake and drummed them out of town."

Linear Wonderland has been a bloody battle—with everyone fighting for the DAC Crown, ev PMI introduced the *first* monolithic Digital-to- Converter back in 1969. The battlefield has been crowded, like the one Alice observed in *Through the Looking Glass,* and the challengers have often been just as ineffective.

> "She thought that in all her life she had never seen soldiers so uncertain on their feet: they were always tripping over something or other and whenever one went down, several more always fell over him."

What they are fighting for in Linear Wonderland is PMI's DAC crown. Now—just when the Lion and the Unicorn thought one of them was about to win it away—PMI gives them something new to trip over: from the original source of the world-famous DAC-08 comes the complete 8-bit DAC-208, plus two more—the 6-bit DAC-206 and the 10-bit DAC-210—to create a *truly monolithic* new DAC family, with all components on a single chip, including an internal reference and output Amp.

Just look what's in our new Data Conversion Plum-Cake: the DAC-206 (a complete 6-bit D/A system); the DAC-208 (8 bits plus Sign); and the DAC-210 (10 bits plus Sign). All are the fastest in their class, with a maximum of μs settling time and a typical of 1.5μs, and after all, what most DAC users want is *speed.* All have guaranteed monotonicity. And all are priced lower than comparable hybrids and have no monolithic counterparts. And they offer the greater convenience and reliability of PMI's famous monolithic construction, plus our exclusive Sign-Magnitude Coding format, and Triple Passivation, of course.



For any data conversion application you have in mind, there's now a PMI DAC to fit the bill at prices ranging from $55 at the top of the line to $9.50 at the lower end. They also come at all commercial and military temperature ranges, including 883B versions.

The chart shows comparisons and what we've been talking about—nobody else's are really *truly* monolithic like the DAC-206, 208 and 210—which are monolithicly *complete* with Op Amp and reference on the chip.

When Alice told the King she'd never seen such fighting just for a crown, he told her, "The best of the joke is, It's *my* crown all the while!" So the next time the Lion and the Unicorn stop fighting long enough to try serving you their plain brown data conversion bread, tell them you prefer the King's DAC Plum-Cake from PMI. Which DAC Plum-Cake would you prefer? Take your choice on the coupon.

If someone beat you to the coupon, write to us. Or circle #200 for literature.

Precision Monolithics, Incorporated
1500 Space Park Drive
Santa Clara, California 95050
(408) 246-9222 TWX: 910-338-0528 Cable: MONO

In Europe contact:
Precision Monolithics, Incorporated
c/o BOURNS AG
ZUGERSTRASSE 74, 6340 Baar, Switzerland
Phone: 042/33 33 33 Telex 78722

SAMPLE PMI's DAC PLUM CAKE

Just fill in the coupon for the DAC of your choice and we'll send you a free *sample. How do we know you'll like it enough to give them away? It's a piece of cake!*

☐ DAC-206 ☐ DAC-208 ☐ DAC-210

Mail to: **Precision Monolithics, Inc.,** 1525 Comstock Avenue, Santa Clara, CA 95050

or **Precision Monolithics, Inc.,** c/o BOURNS AG Zugerstrasse 74, 6340 Baar, Switzerland

My name_____

Title_____

Company_____

Dept._____

Address_____

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Phone (_____) _____

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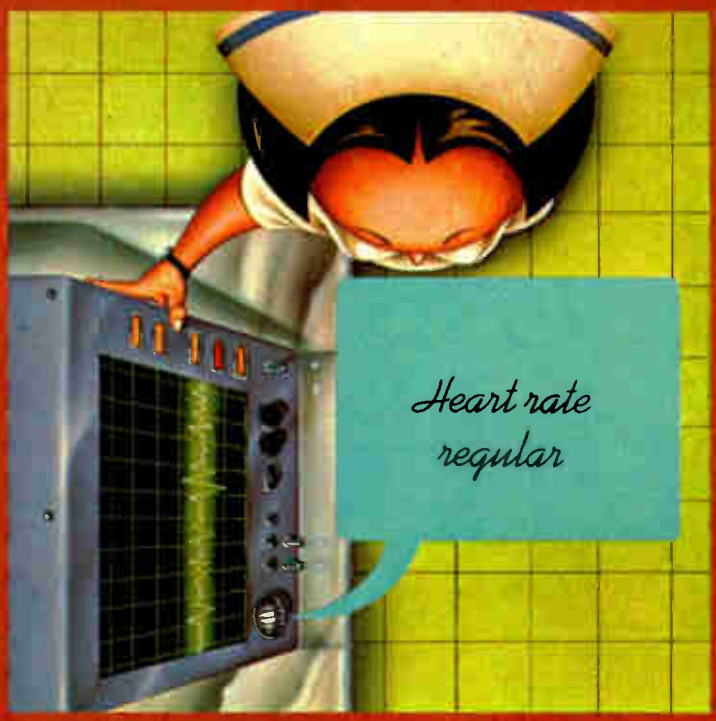
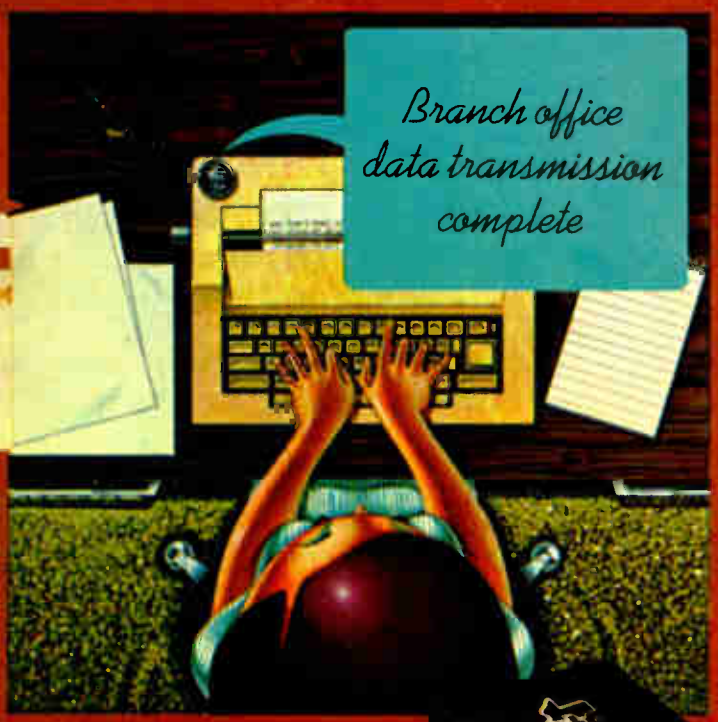




Products that talk.
The man-machine interface will never be the same.

Let's talk about speech capability. Voice synthesis products. From Texas Instruments.

The bright promise of products that think came closer to fulfillment in the 70s. The trend for the 80s is clear: Products that "talk."

Whether it's appliances, automotive consoles, transaction terminals, office systems, telecommunications, robotics or electronic toys and games, no other area of technology will have more impact during this decade.

Speech synthesis technology — pioneered by TI — portends a whole new generation of voice-prompting products. Products that will change the way you live and learn and work.

So, if you're designing new products with speech applications, talk to TI — the *only* total capability supplier with the experience and production-proven know-how to assure you of reliable speech products and services.

Let's talk technology

TI offers several methods of vocabulary analysis, dependent on your volume, versatility of application and voice quality desired. TI's Linear Predictive Coding (LPC) technique provides the highest quality speech reproduction because it's the only technique devised that models itself after the human vocal tract.

Define your vocabulary, consider your volume requirements, cost and development time, then talk to TI about your application.

Let's talk products

Choose from the industry's broadest, most cost-effective line of speech products. A growing line of integrated circuits, evaluation kits, OEM boards and a capability for the design and development of complete custom modules incorporating microprocessors, display and interface functions. A good example of our commitment to this technology: ROMs made especially for speech applications.

TI's LSI Voice Synthesis processors (VSP) and Voice Synthesis memories (VSM) are in volume production, now.

The TMS5200 single chip VSP produces high quality speech at a very low data rate (1200 bps), easily interfacing with 8 and 16-bit microprocessors. The on-chip FIFO buffer allows speech data to be stored in either the host microprocessor system, or off-line on bubble memory or floppy disk. Also, speech data may be stored in a custom ROM, such as the 128K-bit TMS6100. You can use TI VSPs with TMS6100 Series VSMs for storage of up to 3,000 words of speech.

The TMS5100 single chip VSP produces high-quality speech at data rates of 1200 bps and interfaces with 4-bit microprocessors. TMS5100 VSP directly addresses up to 16 TMS6100 VS memories for up to 30 minutes of speech.

For evaluation of TI's voice synthesis capabilities for 4, 8 and 16-bit microprocessors, complete speech evaluation kits are available for TMS5100 and TMS5200.

So, what are we talking about? We're talking about quality, flexibility, cost/performance effectiveness and right now delivery — only from the voice synthesis leader — only from Texas Instruments.

There's more. We're also talking about custom modules and boards. Like the TM990/306 speech module without standard vocabulary for applications using customer-specified words and shipped without EPROMs, allowing users to install Solid State Speech* vocabularies developed specifically for their own applications.

For high-volume applications, user-developed vocabularies can be implemented on mask-programmed ROMs.

The benefits of the custom module approach are both time and cost related. TI's experience in the design and production of electronic modules means quick cycle times, substantial savings, and, of course, getting your product to market faster.

Let's talk support

Like the development of production vocabularies at any of TI's Regional Technology Centers. Custom vocabularies can be synthesized at the RTCs at low cost with quick turnaround (so quick in some cases that you can walk out the door with your program) and delivered on EPROMs for use with either TI's TM990/306 speech board or TMS5000 Series VS processors.

And like tapping the resources of TI's word library where natural sounding speech is pre-recorded and readily available for specialized vocabularies.

And like an intensive one-day RTC seminar covering TI's Solid State Speech technology and its applications, including acoustics, phonetics, waveform analysis and LPC. Systems architectures as well as hardware and software design techniques and a demonstration of several speech products round out the day.

And like the Design Service assistance rendered by the RTCs for the application of cost-effective, state-of-the-art technologies to your specific product and program needs.

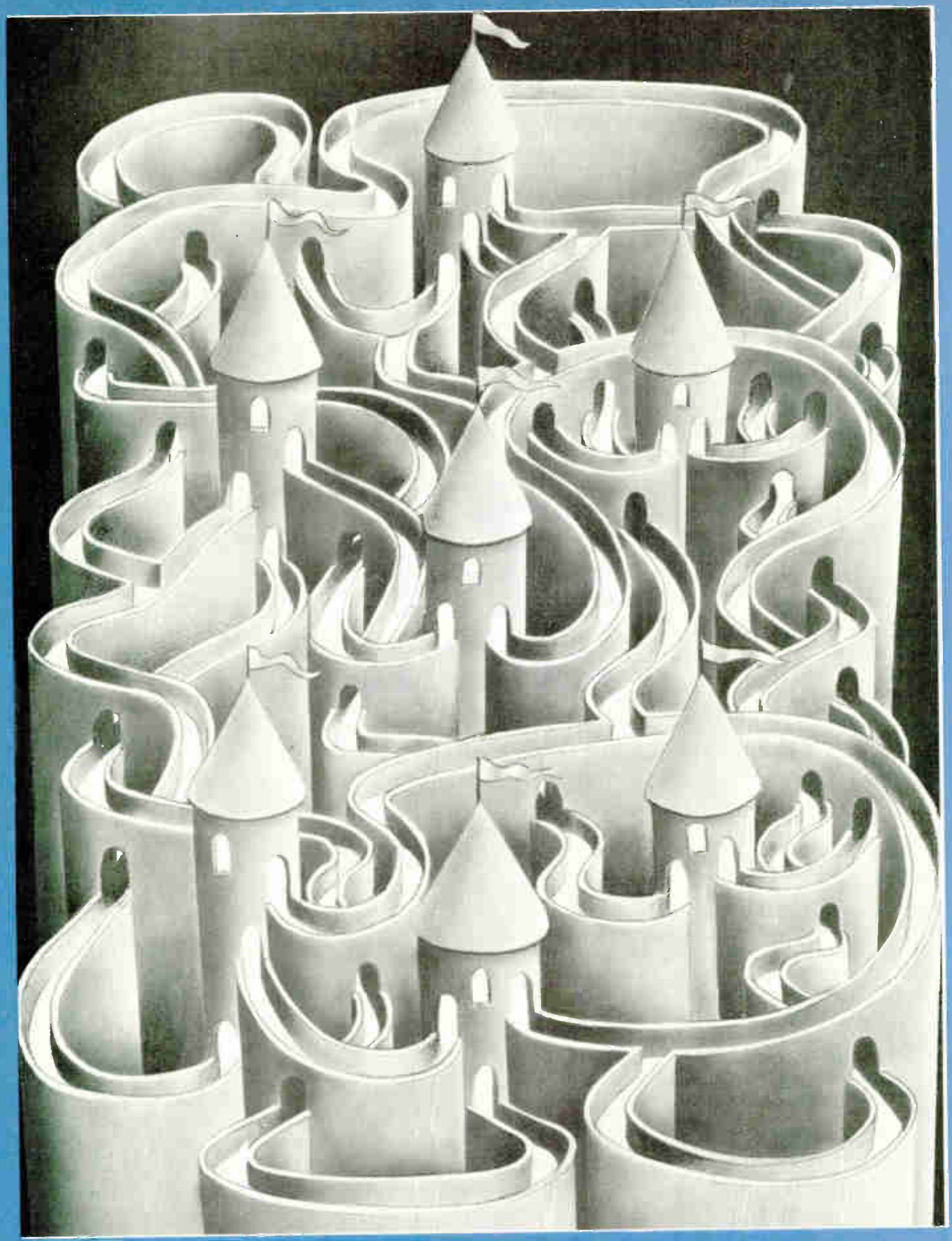
Let's talk now

About a total systems solution capability for voice synthesis technology. About low-cost, high-quality, quick turnaround Solid State Speech applications for your products.

Talk to your nearest TI field sales office, or write to Texas Instruments Incorporated, P.O. Box 225012, M/S 308, Dallas, Texas 75265.

TEXAS INSTRUMENTS
INCORPORATED

*Solid State Speech is a trademark of Texas Instruments Incorporated.



Test #1: You are a guard in this maze fortress and have the duty of visiting all seven towers starting with the middle tower. You may leave the tower by either doorway and return through the other. If you visit all seven towers only once, never using the same path twice, what is the only course you can take?

WE'D LIKE TO TEST YOUR CIRCUITS.

We devised a fiendish little labyrinth to test your mental circuits. If it points out a better way to test your printed circuits, so much the better.

It occurred to us that choosing an automatic test system is a lot like working your way through a labyrinth.

One system looks pretty much like any other, in the same way one path looks just like another. And, unless you know the difference between products, you don't know which way to go.

Some major differences between a GenRad system and all others.

At GenRad we genuinely believe our systems can test your printed circuit boards more efficiently than any other system. The reason? A GenRad system is significantly different from other systems.

Take software, for example. We made sure ours was well defined and well integrated with the hardware from day one. And we continue to update it. (Nine major enhancements in as many years, actually). The result? Systems we sold nine years ago are still testing today's board designs. Can anybody else say that?

Another key difference is programming support. We have 8 Regional System Centers worldwide, where you'll find as many as 10 complete GenRad test systems in operation—with 20 or more of our people ready to develop test programs for you. No one else can provide you with programming support like that.

And consider our credentials. GenRad has been a leader in testing for 65 years. And our sales are now over $150 million. But perhaps the best testimony to our commitment to our customers is the fact that we have more board testers in use worldwide than anybody else.

Some specific product differences to get you moving in the right direction.

GenRad makes both functional and in-circuit testers. A lot of our customers use both advantageously. No matter which you choose, what's important is how long it takes to do a test program. And how much help the system gives you automatically.

The advantages of a GenRad functional system.

When it comes to functional testers our systems give you plenty of help. A good-sized library of functionally modelled IC's, for example, can save a lot of time in developing a test program. We just happen to have the largest library in the business. Over 2000 SSI and MSI devices and over 100 LSI devices.

Also an accurate simulator can keep you from going down a lot of blind alleys while working on a test program. So does the ability to prepare programs incrementally and do nodal verification. You'll find all of these things on a GenRad functional tester. But not on anybody else's.

The GenRad 1795 Functional Test System

The GenRad 2270 In-Circuit Test System

When it comes to troubleshooting, isolating faults directly to a single IC can be a tremendous timesaver. Our special beyond-the-node software linked to a diagnostic resolution module lets you do just that.

The advantages of a GenRad in-circuit system.

You want pretty much the same things in an in-circuit system that you want from a functional system—simple program prep and comprehensive diagnostics to maximize throughput. Look for a test system that does more than dump out a rough first pass of a test program.

Look for one with software so automatic you get a program that's almost ready to run as is.

In that regard, you're going to be interested in these exclusive GenRad features: Automatic Bus Disable which frees the programmer from having to manually write a lot of extra tests in order to isolate the IC under test from the effects of other ICs on the bus; feedback squelch to automatically deal with troublesome spikes; and memory behind each pin to allow patterns to be applied and sensed in parallel. Go ahead and check out other systems, but you won't find these exclusive features on any of them.

One final thing to keep in mind. If you're going to design with two kinds of logic (and who isn't today?) your tester ought to be capable of testing two logic families simultaneously, right? Both our in-circuit and functional testers can.

The logical conclusion. And an offer that's hard to pass up.

If you've followed us this far, it ought to be pretty clear whose system can do the best job of testing your printed circuits. Now how about a wall-size version of our labyrinth to show the world your mental circuits check out okay, too? We'll send you a giant poster if you drop us a note on your letterhead. And, by the way, if you'd like to know more about a GenRad System, the best course of action is to call us.

How about right now?

You can reach us at 300 Baker Avenue, Concord, Massachusetts 01742. Telephone: (617) 369-4400.

GenRad

THE BEST IN TEST.

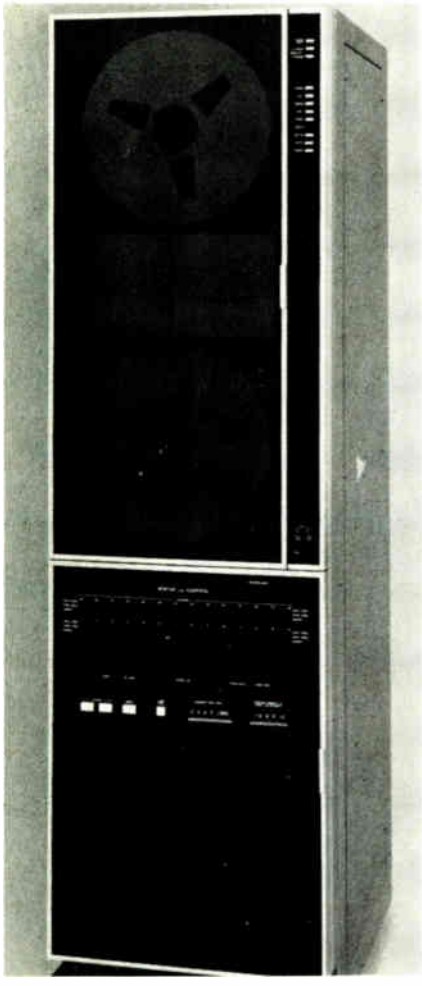
Circle 219 on reader service card

Instruments

Data recorder sets own speed

Data rate and tape speed of high-density instrumentation recorder adapt to application

The trend toward digital instrumentation systems is exciting a need for temporary or archival storage in the form of high-density digital tape recorders. These recorders are finding their way into a wide variety of applications, each of which may require different data rates and, consequently, additional expense in tailoring the recording system to suit the application. To satisfy these widely varying needs, engineers at Honeywell Inc.'s Test Instruments division in Denver have developed a high-density digital magnetic-tape recorder that can be readily programmed to match different data rates and packing densities without system recalibration.



To date, "manufacturers have designed high-density digital recorders to the unique requirements of a particular application," states Charles A. Castle, senior specialist at the Honeywell division. If an application is changed, "the recorder must be changed also, and it usually takes a minimum of hours—even days—to recalibrate and reconfigure. Redesign is often necessary."

Time saver. The HD-96 has built-in electronics that computes and sets optimum tape speed. This "eliminates the set-up time and cost usually required to handle the different data rates" of, for example, satellite image signals and radar signal analysis, Castle states.

In essence, the standard HD-96 is fully automatic (without recalibration) over a 128:1 speed range, or 1.875 to 240 in./s. It has a total serial throughput rate of 26 kb/s to 160 Mb/s and parallel data rates to 186 Mb/s. Higher rates are available in custom configurations. Specially designed pulse-code-modulation electronics are included for either serial or parallel input/output operation. Modular construction permits the number of active channels to be adjusted, from 4 to 28 tracks, to meet the aggregate bit rate needed for a particular application.

To reinitialize the HD-96 for new requirements, the operator manipulates the front panel and associated clock-frequency synthesizer to program bit rate and packing density in a matter of seconds. The recorder then computes, displays, and runs at the optimum tape speed for the new conditions.

The technical breakthrough in this proprietary design is the "automatic equalization" of the reproduction electronics after initial setup, Castle says. It is done by a "unique" digital reproduction amplifier and bit synchronizer, which replace the traditional binary equalizer and phase-locked-loop bit synchronizer. The design avoids the constraints of the binary tape speed steps in traditional instrumentation recorders by providing not just the discrete IRIG speeds but any in-between speeds to within 0.1%. Thus the HD-96 can run at the ideal tape speed for recording or reproduction.

Of equal significance is the HD-96's use of a recently developed, yet proven, multitrack error-detection and -correction system [*Electronics*, June 19, 1980, p. 46]. According to Castle, the system "offers bit error rate improvements over raw uncorrected performance by two to three orders of magnitude." The system minimizes the effects of signal dropouts that are the result of flaws in the magnetic tape and other error sources. The data quality is monitored by a bank of three light-emitting diodes for each active digital channel. These indicate a possible error in the reproduced data (data loss), the loss of frame synchronization (sync loss), or a parity error (error).

Among other features of the HD-96 is remote control of the tape transport, the digital data rate, and per-track density—there is a standard remote-control connector on the I/O panel. Additionally, up to four auxiliary analog channels are available for recording time codes, voice, low-rate pulse-code-modulated data, or similar editing or processing functions.

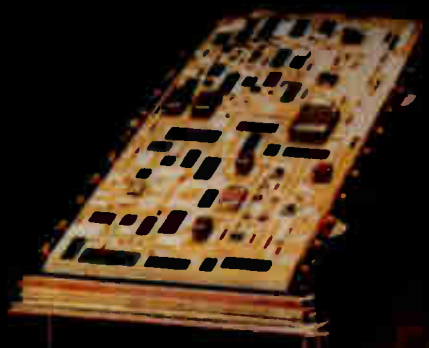
Prices for the HD-96 range from about $65,000 for a minimum-configuration 14-channel system with error detection and correction. Availability is immediate.

Honeywell Test Instruments Division, P. O. Box 5227, Denver, Colo., 80217. [351]

3½-digit panel meter consumes only 17.5 mW

Although the DM-LX3 3½-digit, single-board panel meter has an extra-large, 0.75-in.-high liquid-crystal display, it consumes only 17.5 mW (+5 V at 3.5 mA) because it uses low-power complementary-

MIL-STD-1553



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MANCHESTER II CONVERTER

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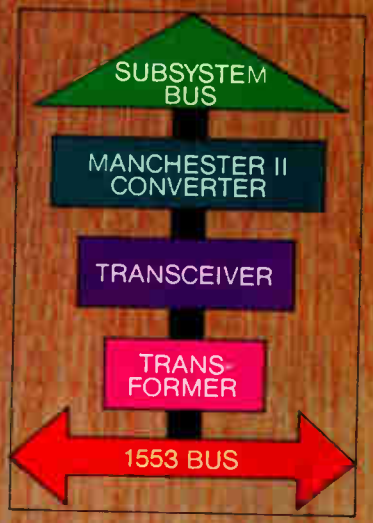
DDC TAKES YOU FROM BUS TO BUS

DDC's MIL-STD-1553 Transformer, Transceiver and Manchester II Converter hybrid circuits provide unique design solutions to the vital link between the 1553 Serial Data Bus and the Subsystem Parallel Bus. Model BUS-8553 Transceiver features very low power dissipation and improved filtering on the receiver to enhance bit error rate of the system. DDC's Model BUS-8937 Manchester II Converter offers encoding/decoding, serial/parallel and parallel/serial conversion, address decoding and recognition plus tri-state double buffered output latches. For complete details on how DDC can take you from bus to bus call or write today.

1553 Data Bus to Subsystem Bus



DDC

ILC DATA DEVICE CORPORATION

EXECUTIVE OFFICES: ILC Data Device Corporation, Dept. K-7, 105 Wilbur Place, Bohemia, NY 11716, (516) 567-5600, TWX: 510-228-7324
LOS ANGELES: ILC Data Device Corporation, Dept. K-7, 7337 Greenbush Avenue, No. Hollywood, CA 91605, (213) 982-6454, TWX: 910-499-2674
DALLAS: ILC Data Device Corporation Dept. K-7, 415 East Airport Freeway, Suite 490, Irving, TX 75062, (214) 252-7624, TWX: 910-860-5902
LONDON: DDC United Kingdom Ltd., Dept K-7, 128 High Street, Hungerford, Berkshire, RG17 ODL, England 04886-2141/2142, TLX: 851-848826
PARIS: DDC Electronique, Dept. K-7, 4 Rue de l'Abreuvoir, 92400 Courbevoie, France, (1) 333-5888, TLX: 842-630609

Circle 221 on reader service card

New products

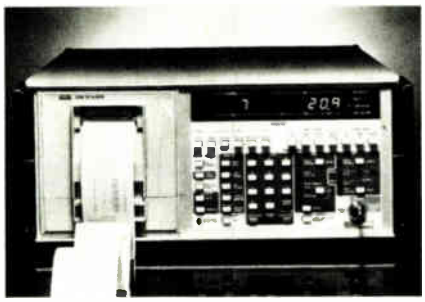
MOS circuitry. The meter can operate continuously for several months on a single set of four AA alkaline batteries. The DM-LX3 has a narrow profile, being only 0.56 in. deep, so it can be mounted in control panels or instruments with little available space.

The meter displays the 3½ digits (±1.999 v dc. nominal input range) with an accuracy of ±1 least significant digit. It requires an external +5-v power supply, but the −5 v that is required to run the meter's input circuitry is generated by its own dc-dc converter. The instrument sells for $57.50 in single quantities but substantial discounts are available to original-equipment manufacturers. Delivery is from stock to three weeks.

Datel Intersil, 11 Cabot Blvd., Mansfield, Mass. 02048. Phone (617) 339-9341 [353]

Data logger lets user set own engineering units

Any physical parameter that can be represented by a proportional voltage or current may be measured by the Fluke model 2240C data logger,



for it has 30 mx+b functions with which the user can convert transducer input scales into their proper engineering units. Moreover, the two-color printer can provide a wide variety of engineering-unit notations. The user has a choice of 11 thermocouple or resistance-temperature-detector linearizations, and a high-performance analog-to-digital converter ensures long-term accuracy. The control panel clearly differentiates the programming area from the operational area, and, once programmed, all front-panel functions can be locked out to prevent unauthorized alterations.

The instrument can scan up to 15 channels per second with a 0.1° resolution. It is remotely programmable via RS-232-C or IEEE-488 interfaces. Prices start at $5,790 for a typical system.

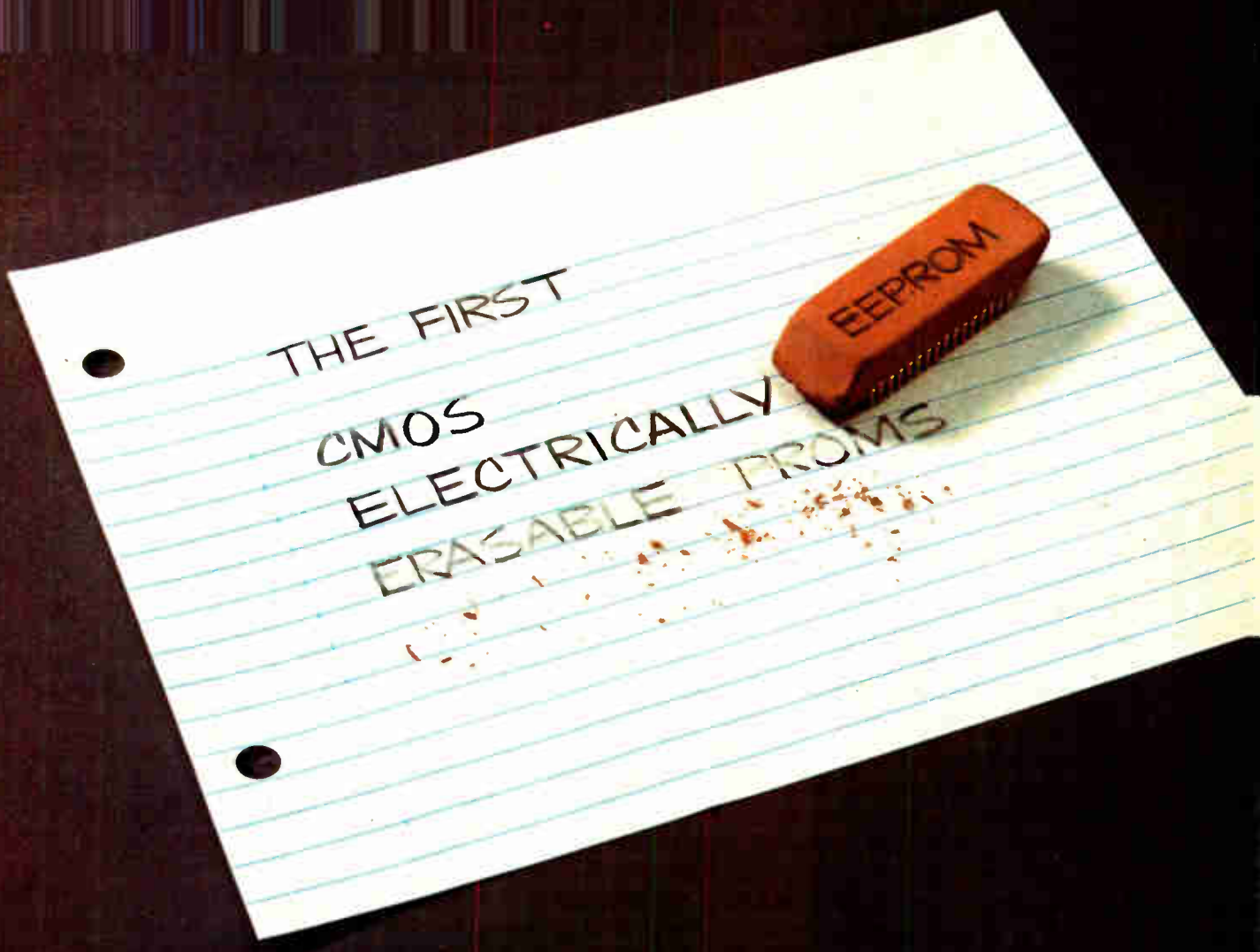
John Fluke Manufacturing Co., P. O. Box 43210, Mountlake Terrace, Wash. 98043. Phone (206) 774-2211 [354]

Fm radio test set for vhf/uhf range weighs 26 lb

Although one of the lightest portable fm radio test sets, the CE-31A contains all the test instruments needed to check the operation of an fm radio transmitter or receiver in the very and ultrahigh-frequency range of 25 to 999.9999 MHz. The radio-frequency signal generator section can check receiver sensitivity from 0.1 μv to 10 mv. The frequency-modulation measurement section can check a transmitter output frequency for accuracy and determine the output modulation's deviation or phase angle. The unit has a demodulated signal output that can be used to drive an oscilloscope and thus to visually check modulation waveforms for distortion and accuracy.

The 26-lb instrument sells for $4,995. Available options include a subaudible tone generator to open receiver squelch circuits and the capability of using an internal battery and external +12-v dc power.

Cushman Electronics Inc., 2450 N. First St., San Jose, Calif. 95131. [356]



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Clive House
12–18 Queens Road
Weybridge, Surrey KT 139XD
England
Telephone 932-47262

The HNVM 3008 EEPROM Offers the Advantages of:

- Non-Volatile Data Retention (10 years without power)
- High Number of Reprogramming Cycles (100,000 times)
- Fast Electrical Programming
- Low Power CMOS Performance

The HNVM 3008 is an 8,192 bit Electrically Erasable and Electrically Programmable Read Only Memory (EEPROM) organized in a 1024x8 configuration. It has the unique combination of low power, good access time, multiple erase and reprogram cycles and long retention time.

In addition, it operates in a wide temperature range and erases electrically in a very short time (no waiting for factory mask turnaround or ultra-violet light erasure).

The HNVM 3008 operates as a regular ROM with the power supply at 5V. Erasing and programming is accomplished in or out of the circuit when the input supply voltage is 17 volts. This characteristic allows the EEPROM to replace ROM or EPROM and provides non-volatile data updating and retention for a multitude of new applications.

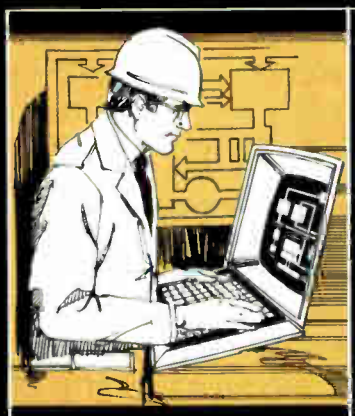
Also available now is the HNVM 3004, a 4,096 bit EEPROM (512x8) for those requiring smaller devices. These exciting new products are part of a planned family of high technology non-volatile devices.

For the HNVM 3008 or HNVM 3004 Data Sheets call or write: Hughes Solid State Products.

Size:	8,192 Bits
Type:	ELECTRICALLY ERASABLE Electrically Programmable
Voltages:	Read...+5V only Erase, Program...+17V only
Power Dissipation:	5mW Operating –0.5μW Standby
Operating Range:	–55°C to +125°C
Access Time:	500 nsec
Endurance (No. of Erase/Reprogram Cycles):	100,000
Data Retention:	10 years at 100°C
Data Erase Time:	100 μsec
Entire ROM Program Time:	0.1 sec

Circle 223 on reader service card

Gordos industrial controls the way they are applied



If one of our industrial controls products can pass the tests we put it through before it leaves the plant, you can count on it to perform in the field. In fact, across our entire SSR line, the average field return rate is less than 0.5% — well below the industry average. Here's why.

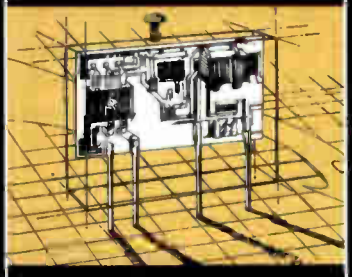
Gordos experience in industrial controls: I/O Systems, SSRs and Reed Relays

Gordos I/O Systems provide the mechanical and electrical interface to minimize your efforts in assembling an efficient, workable control system. With a company-wide emphasis on industrial controls, Gordos product development engineers know precisely where problems arise in actual field use. We've learned how to design in safeguards and what to test for.

Two of the toughest tests in the industry

We were one of the first manufacturers to offer 100% testing for immunity to electromagnetic interference (EMI), a problem frequently encountered in electromechanical environments. This test insures products which are highly immune to false triggering by EMI.

Perhaps the toughest test in field use comes when a relay is required to switch a highly inductive load. To meet this challenge, each Gordos relay is individually tested to insure maximum field reliability.

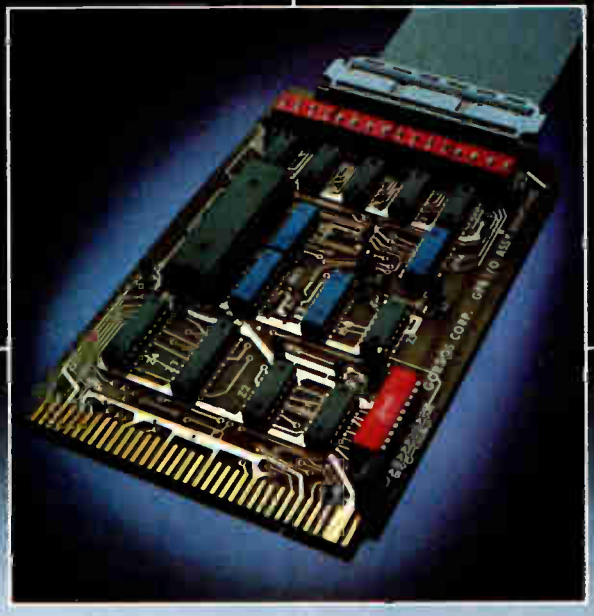


Other tests

Depending on your application, you may decide that additional testing is advisable on a 100% or partial basis. High temperature leakage tests, thermal shock tests, full environmental simulation, and life test data are all available.

Unbiased applications assistance

Gordos manufactures both reed and optically coupled industrial controls devices. Since we supply a full line, our primary interest is to provide you with the right product — on time and at the right price. For instance, if EMI presents a problem in your application, a reed coupled device may be the



products are tested in-house in the field.

best solution. If switching speed is of the essence, optical coupling may be required.

Thick film construction for harsh environments

Gordos was the first SSR manufacturer to offer certain models with the high reliability and cost/performance advantages of thick film hybrid construction. In industrial environments, thick film affords superior thermal properties, noise immunity, and superior resistance to shock and vibration.

VDE compliance

To assist you in building and marketing industrial controls systems for Europe, Gordos was the first manufacturer to produce SSRs and I/O s which conform to VDE specifications.

Distributor network

When one of our standard models will suffice, take advantage of immediate availability from your nearby Gordos Distributor.

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MY APPLICATION IS _____

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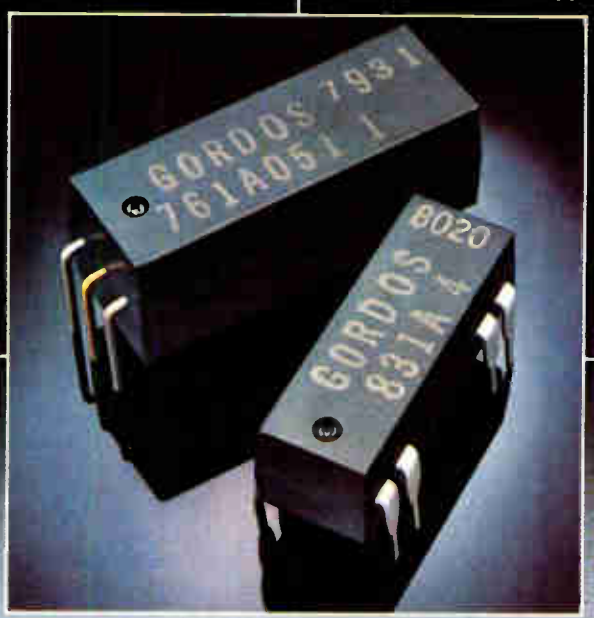
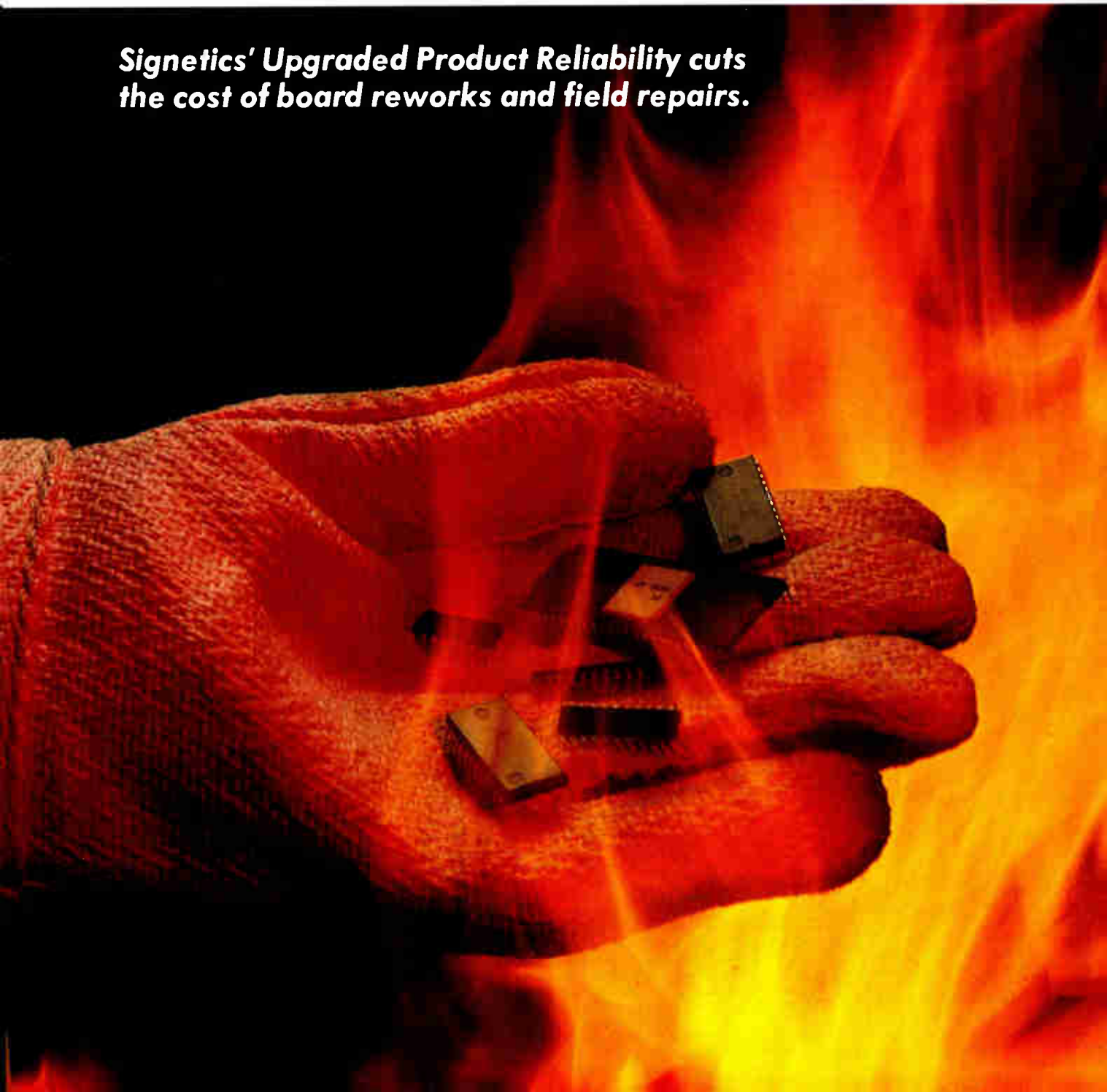


Interface with Intelligence GORDOS

SUPR IIB bu
heat on high

Signetics' Upgraded Product Reliability cuts the cost of board reworks and field repairs.



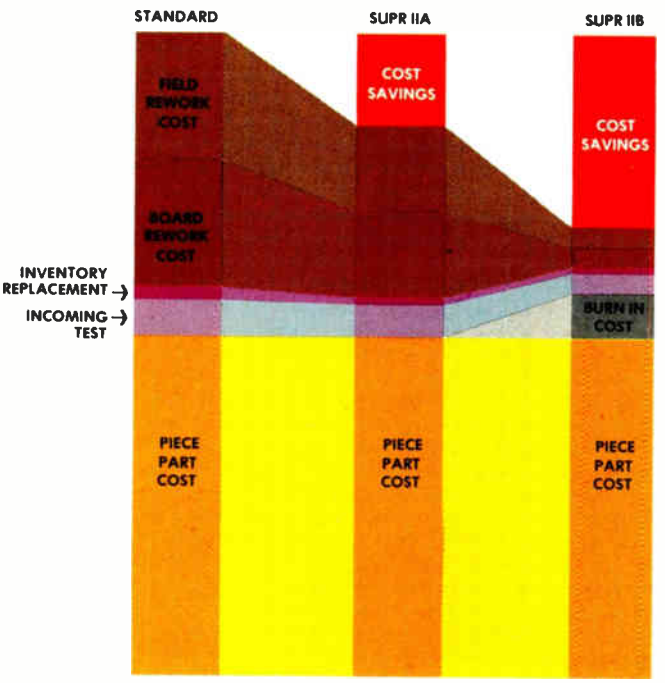
n-in puts the board costs.

The difference between a faulty IC and a good one is more than just the cost of the part. Board reworks, field failures, and inventory floats make up the hidden penalty OEMs often pay for unproven devices.

Signetics changes all that with SUPR IIB. It's our exclusive burn-in/test process. And we do it right on our manufacturing line. By pushing ICs to their limits, we accelerate failures without degrading device quality.

Your reward is tighter AQLs. Fewer incoming tests—and infrequent service calls. So you'll save money and enhance your reputation for reliable systems. The bottom line is more profits for you.

SUPR IIB is available to you with a wide variety of Signetics products in addition to our standard quality assurance test methods.



As a leading supplier to the Military/Aerospace market, we're well acquainted with the importance of tight specs and high reliability. Even our off-the-shelf logic ICs pack lower AQLs than the industry standard.

Count on fast delivery, too. Since SUPR IIB is part of the process flow, we beat independent test lab turnaround. Handily. To top it off, *we don't charge for those ICs that fail burn-in. You pay only for the winners.*

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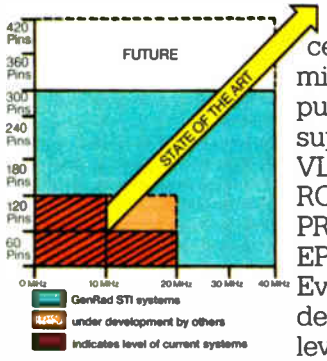
GENRAD ANNOUNC

This is the VLSI test system designers and test engineers have been anxiously awaiting. The VLSI test system that makes every other product on the market today look antiquated by comparison. The VLSI test system that's going to change forever the way VLSI testing is done.

This is the GenRad GR16.

A VLSI device tester that will define the state-of-the-art for years to come.

The GR16 starts out where other testers leave off. It can test VLSI



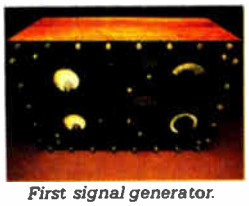
microprocessors, micro-computers and support chips. VLSI RAM's, ROM's, PROM's and EPROM's. Even VLSI devices with level sensitive scan. And a wide variety of custom devices.

It's as productive in production tests as it is in engineering characterization. And, here's the amazing news: the GR16 can routinely take on devices up to 144 pins at test rates of up to 40 MHz. With a level resolution of 14 bits and timing accuracy of less than a nanosecond.

The GR16 has parallel test capability. It has honest-to-goodness *auto* cal. It uses PASCAL. And there's host computer networking capability, too.

A company that's been a leader in testing for 65 years.

Before we go any further, though, you may be interested to know the character of the company behind this new machine. This is GenRad we're talking about. The people who pioneered the first standard signal generator. The first megohm bridge. The first electronic stroboscope. The first commercial computer-based logic board test system. A world-wide company with sales of over $150 million and with more levels of support (even regional centers) than anyone else in the industry. A company that is the acknowledged technology leader in printed circuit board testing with more functional test systems installed than any other company.



First signal generator.

The GR16. A product so new it's years ahead of its time.

An elite design group.

Who designed the GR16? An elite group of ATE experts with a carte blanche to explore the very limits of VLSI testing. A team that is, today, the very best in VLSI testing and, who are, according to the degree of your interest and your ability to buy, available to you for advanced planning and analysis of your VLSI device testing requirements as they apply to automatic test systems. Perhaps you should make a note to call them.

A "start-from-scratch" attitude yields a totally new design.

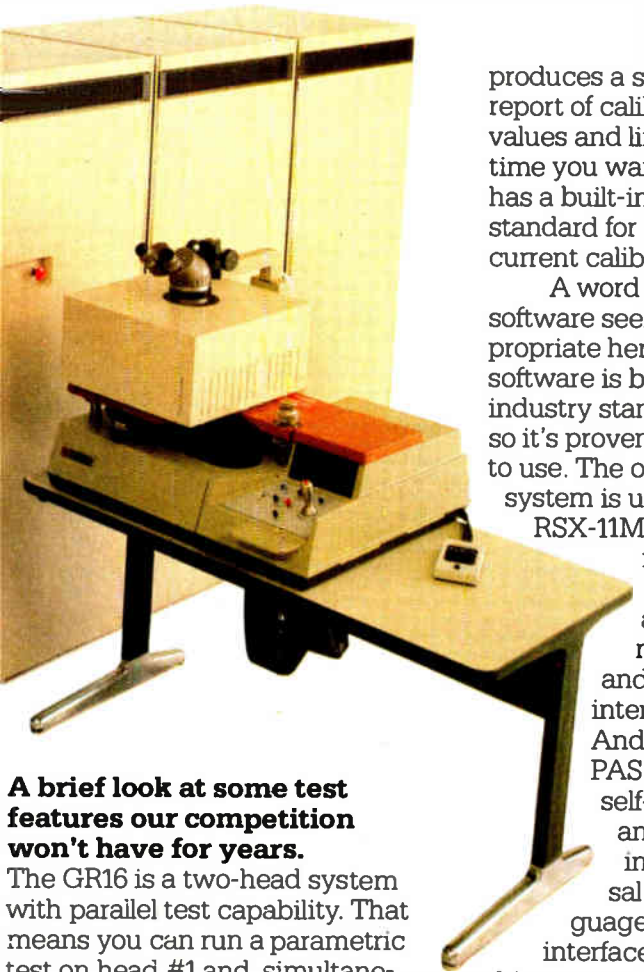
"The design," you're saying. "Get to the design."

O.K. The GR16 is a totally new design based on dual bus architecture. The advantages? There are several. Like a test rate of 40 MHz, which, combined with a 2 MHz instruction rate, means incredibly high throughput. Plus field-expandable pin count to help make sure the GR16 meets your needs for the future.

As you might expect, with all these features the GR16 has an

extraordinary capacity for speeding up your time to market and cutting your cost to test VLSI devices.

FS: VLSI TESTING.



A brief look at some test features our competition won't have for years.

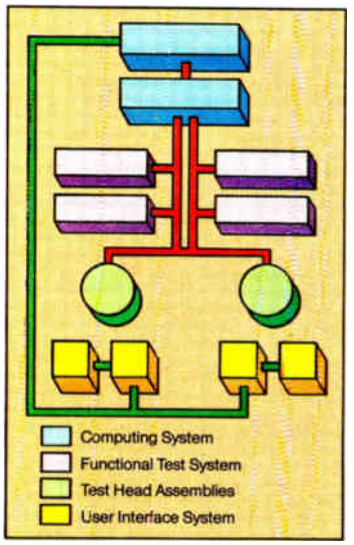
The GR16 is a two-head system with parallel test capability. That means you can run a parametric test on head #1 and, simultaneously, run either a parametric or functional test on head #2. As you can imagine, dual heads operating in parallel can increase throughput by up to 100%.

The timing control unit has 16 phase generators, each of which has 16 values, selectable in real time. 125 ps resolution, high stability, and autocalibration provide sub-nanosecond timing precision. And the GR16 allows you to switch, on-the-fly, between algorithmic and functional test patterns and all input, output pin states. In addition, all pins are truly universal with complete access to timing and test pattern resources which lets you test the most complex VLSI components.

And the GR16 has true *auto* cal. With a program that automatically calibrates the system and produces a summary report of calibration values and limits. Any time you want. It also has a built-in transfer standard for voltage/current calibration.

A word about software seems appropriate here. The software is based on industry standards, so it's proven and easy to use. The operating system is unmodified RSX-11M from DEC including file management, memory management and utilities. There's a user interface operating system. And our test language is PASCAL; highly-structured, self-documenting and becoming a universal test language. The user interface is menu driven so you get direction and guidance all along the way.

And, for people who want networking, there's GRnet,™ which uses very high speed data links to GenRad's host computers, to distribute the computing tasks and maximize throughput.



GR16's four main hardware segments.

A measure of our acceptance.

We should also mention in passing that the response to our first VLSI test system has been fantastic. It even surprised us.

Some very large companies, here and abroad, have been inquiring about our product (despite the fact we've tried to keep it as quiet as possible). And we're pleased to say we've already sold our very first system.

A chance for you to see for yourself.

By now you're probably wishing you could see the revolutionary GR16 in action. You can. We've created a special videotape presentation of the GR16 to show to prime prospects. If you'd like your own private screening, just ask.

After all, isn't that just the kind of advanced idea you'd expect from the company that's the best in test?

GenRad
THE BEST IN TEST.

If you're really eager for a screening or more information, give us a call at (408) 946-6960. Ask for Jim Healy. Or send this coupon to: GenRad STI, 510 Cottonwood Drive, Milpitas, CA 95035.

☐ I'd like a "private screening" of your videotape.
☐ Send me more information.
☐ Send a sales representative.

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Data acquisition

Hybrid is linear over temperature

12-bit a-d converter holds linearity error to ±1 LSB from −55° to +125°C

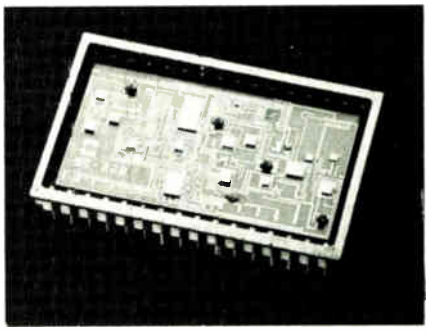
Of the many 12-bit hybrid analog-to-digital converters specified as military grade, few if any are in fact specified to operate over the entire military operating-temperature range of −55 to +125°C. For those that do operate over the full range, maximum linearity error may not be clearly specified for that full range, and external adjustments may be required to maintain rated linearity error levels at widely different temperatures.

The MNADC87-H successive-approximation hybrid a-d converter is specified to operate with a ±1 least-significant-bit maximum linearity error from −55° to +125°C, with no external adjustment. Guaranteed to have no missing codes over the entire range, it is rated at ±½ LSB maximum linearity error at 25°C. Its maximum unadjusted absolute accuracy error of ±0.3% of full scale makes it one of the most accurate 12-bit units for the military temperature range. Maximum offset drift is a mere ±5 ppm/°C, and maximum gain drift is 20 ppm/°C.

Housed in a 32-pin hermetically sealed case with dual in-line dimensions (pin rows are 0.9 in. apart), it is pin-compatible with the industry-standard ADC85 a-d converter. It has a 10-μs maximum conversion time and an internal clock and is available with serial and parallel outputs. Its five user-selectable input ranges (0 to 5, 0 to 10, ±2.5, ±5, and ±10 v) make it truly versatile.

Other specifications at 25°C include maximum unipolar and bipolar zero offset error of ±0.5% of full scale and maximum gain error of ±0.1%. Power consumption during operation from ±15 and +5-v supplies is 1,400 milliwatts.

Available with a short-cycle pin and optional high-impedance-input buffer and offset and gain adjustments, the a-d converter can be purchased fully screened to MIL-STD-883 method 5008. An industrial grade model MNADC87 is also available to operate over the −25° to +85°C temperature range. The TTL-compatible converter features complementary straight binary unipolar and complementary offset binary and 2's complement bipolar output codings. Input impedance levels are 1, 2, and 4 kΩ for the 5-, 10-, and 20-v full-scale ranges.



In lots of 100 units, the MNADC87-H is priced at $187. The industrial-grade MNADC87 is priced at $99. Both are available from stock.

Micro Networks, a division of Unitrode Corp., 324 Clark St., Worcester, Mass. 01606. (617) 852-5400 [381]

System module pipelines chores

Data acquisition module has overlapped functions to keep multiplexed operation fast

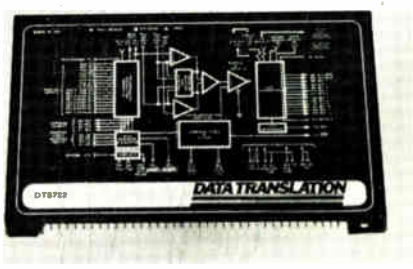
High-speed simulation and industrial-control applications often run up against the limits of their data-acquisition systems, especially when the number of parameters being monitored is large. The DT5722 high-speed data-acquisition module can access up to 8 differential or 16 single-ended inputs, performing 12-bit analog-to-digital conversion at an accuracy within ±0.03% at throughputs of up to 250 kHz in its multichannel mode and as rapidly as 300 kHz when locked to a single channel.

The DT5722 module grew out of a requirement of an array-processor firm, Floating Point Systems Inc., whose systems could handle large amounts of data rapidly, but which had found too few data-acquisition systems capable of supplying enough input to keep them busy.

The block diagram of the 5722 is standard enough. At its input is a multiplexer. This is followed by an instrumentation amplifier (with programmable gain an option), a high-speed sample-and-hold network, a fast 12-bit analog-to-digital converter, logic for timing and control, and three-state buffers at the module's output.

Data Translation engineers assembled the blocks so as to achieve maximum speed and designed the control logic so that the operation of the successive blocks in the 5722 could overlap in time—in other words, be pipelined.

The multiplexer needs 2.5 μs to acquire a channel (4 μs in the programmed-gain version), and this is the gating specification affecting throughput. Pipelining allows the output buffers to dump data onto a computer bus while the converter is digitizing a sample and while the sample-and-hold net is acquiring more data for the next round. Thus, while the unit's single-channel throughput is 300 kHz, it drops only to 250 kHz in multiplexed operation. Adding digitally programmable gain



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Long the recognized leader in quality open-frame linears, Power-One is now setting the pace in switching power supplies.

Our fast growing line of efficient high-performance switchers offer a combination of features not found in others at these low prices. Features such as fully regulated outputs, 115/230 VAC input capabilities, superior hold-up time, and totally enclosed packaging for enhanced safety. Additionally, these models incorporate many other innovative ideas that set our switchers apart... while reflecting the same simplicity of design that has kept our open-frame linears the most cost-effective in the industry.

Best of all, Power-One switchers are 100% American built by Power-One personnel, at Power-One facilities, and under tough Power-One quality control standards. Adding up to total dependability at typical Power-One low prices.

So check us out. See why we're leading the way again. This time in switchers.

Send for our new '81 Catalog. Better yet, contact your local Power-One representative for immediate action.

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5V	40A	SK5-40
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15V	13.4A	SK15-13.4
24V	8.4A	SK24-8.4
28V	7.2A	SK28-7 2
SIZE: 2"H X 4.88" W X 13"L		

$250
200 WATTS

OUTPUT	VOLTS	AMPS
#1	5V	20A
#2	12V	5A
#3	−12V	3A
#4	5V, 12V, 15V, or 24V. USER SELECTABLE	3.5A
SIZE: 2"H X 4.88"W X 14"L		
MAX OUTPUT POWER: 150 WATTS CONTINUOUS, SUM OF ALL OUTPUTS		
150 WATTS - 4 OUTPUTS THE UNIVERSAL SHQ-150W		

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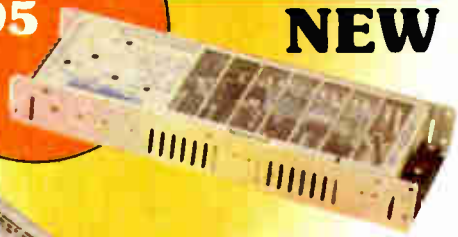

$115
50 WATTS

VOLTS	AMPS	MODEL
5V	10A	SD5-10
12V	4.2A	SD12-4.2
15V	3.4A	SD15-3.4
24V	2.1A	SD24-2.1
28V	1.8A	SD28-1.8
SIZE: 2"H X 4.88"W X 6.25"L		

$170
100 WATTS

VOLTS	AMPS	MODEL
5V	20A	SF5-20
12V	8.4A	SF12-8.4
15V	6.7A	SF15-6.7
24V	4.2A	SF24-4.2
28V	3.6A	SF28-3.6
SIZE: 2"H X 4.88"W X 10"L		

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Circle 231 on reader service card

also costs some time, but again, relatively little, with throughput falling only to 200 kHz.

The access time of the sample-and-hold net is 1 μs and its aperture delay only 20 ns; analog-to-digital conversion time is 2.5 μs, and the three-state buffers are said to be fast enough to use almost the full data-carrying capacity of Q-bus—itself capable of handling about 500 kilowords per second.

The 5722 is intended for high-level inputs: 0 to +10, ±10, or ±5 V. Differential linearity and quantization error both are ±½ least significant bit. Channel-to-channel input voltage error is ±100 μV. Input bias current is a maximum of 20 mA. Sample-and-hold feedthrough, interchannel crosstalk, and common-mode rejection ratio all are rated at −80 dB. Linearity changes with temperature at only ±3 ppm/°C.

The mechanical and electrical requirements of the 5722 closely parallel those of earlier Data Translation modules. Its external dimensions, metal-shielded packaging, and pinout configuration are exactly the same as in earlier modules. Length and width are 4.6 and 3.0 in., and thickness is 0.375 in. maximum.

The DT5722 requires positive and negative 15-V supplies at a maximum of 140 mA and a +5-V supply at 300 mA, all ±5%. Input impedance of the device is 100 MΩ shunted by 10 pF in the off mode and by 50 pF in the on mode.

Expander. Company spokesmen expect the DT5722's most popular option to be a multiplexing expander module that would bring the total number of channels accessed to 32 differential or 64 single-ended inputs. No price or model number has been designated for this option, but the firm says it is coming soon.

Though introduced as a module, the 5722 will probably find its way into the company's line of board-level products soon. The module systems must be ordered with the desired type of input specified (single-ended or differential), in contrast with some other Data Translation systems for which such features are user controllable.

The DT5722 costs $1,495 in quantities of 1 to 9. Programmable gain—gains of 1, 2, 4, or 8 are offered—adds $175 to this price. Original-equipment manufacturer discounts are available; delivery takes five days.

Data Translation Inc., 100 Locke Dr., Marlboro, Mass. 01752. Phone (617) 481-3700 [382]

8-bit d-a converter with 285-V amp has 500-ns settling time

An 8-bit digital-to-analog converter mounted in front of a small modular amplifier, the model ZDA 1200, features outputs to +285 V with a settling time of 500 ns and a slew rate of 800 V/μs. A second version, the ZDA 1201, offers an output of −285 V. Both converters are designed for applications that require high-voltage conversion. Current limiting on the devices provides short-circuit protection. Digital bias control can reduce idling power by 50%, with a 10-μs turn-on time, says the manufacturer.

The units have TTL-level inputs, and their linearity error falls within ½ a least significant bit. The ZDA 1200 requires a +300-V external reference to supply a typical output current of 5 mA; the 1201 requires −300 V. Each also requires a standard ±15-V dual analog supply.

The module is enclosed in a 2-by-4-by-0.88-in. housing. Its ambient operating temperature range is 15° to 45°C. Each module sells for $170 in quantities of 100 pieces. Delivery is from stock but may take up to eight weeks.

Zeltex Inc., 940 Detroit Ave., Concord, Calif. 94518. Phone (415) 686-6660 [383]

13-bit sample-and-hold amp has 700-ns acquisition time

For high-speed 13- and 14-bit applications, the MN375 13-bit sample-and-hold amplifier acquires a full-scale signal to ±0.005% in 700 ns (1 μs maximum) or to ±0.01% of full-scale range in 500 ns (700 ns maximum). Called a track-and-hold amplifier by the manufacturer because it stays in the sample mode almost continuously until made to hold, the device has a sample-to-hold settling time of 150 ns to ±0.005% of the full-scale range. A maximum aperture uncertainty of 100 ps allows signals as fast as 190 kHz to be accurately captured to the 13-bit level, and the unit's low, 5-mV/ms maximum droop rate allows these signals to be accurately held for over 120 μs.

The MN375's linearity error is guaranteed to be better than ±0.005% of full scale over its entire −25° to +85°C ambient operating temperature range. Gain accuracy is guaranteed to within better than ±0.05% over the same range. Offset error is a low ±1 mV (±3 mV maximum).

Commercial versions of the MN375 are priced at $120 each for 100 units. Units screened to the requirements of MIL-STD-883 are priced at $149 apiece in 100s. The MN375 is packaged in a standard, 24-pin, ceramic dual in-line package. Delivery is from stock.

Micro Networks Co., 324 Clark St., Worcester, Mass. 01606. Phone (617) 852-5400 [385]

40- and 100-MHz 8-bit d-a converters settle in 7.5 ns

The VDAC-8308 series of 8-bit digital-to-analog video signal converters offers settling times of 7.5 ns for a full-scale transition. The TTL version of the converters features a 40-MHz updating rate, and the emitter-coupled-logic version has a 100-MHz update rate. The series is pin-for-pin compatible with the Analogic MP-8308 devices.

In small quantities, the VDAC-8308 TTL d-a converter is priced at $125 and the VDAC-8308 ECL version is priced at $119. Units are available from stock but may take up to eight weeks for delivery.

Intech Inc., 282 Brokaw Rd., Santa Clara, Calif. 95050. Phone (408) 727-0500 [384]

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Or contact RCA Solid State headquarters in Somerville, New Jersey. Brussels, Belgium. Sao Paulo, Brazil. Hong Kong.

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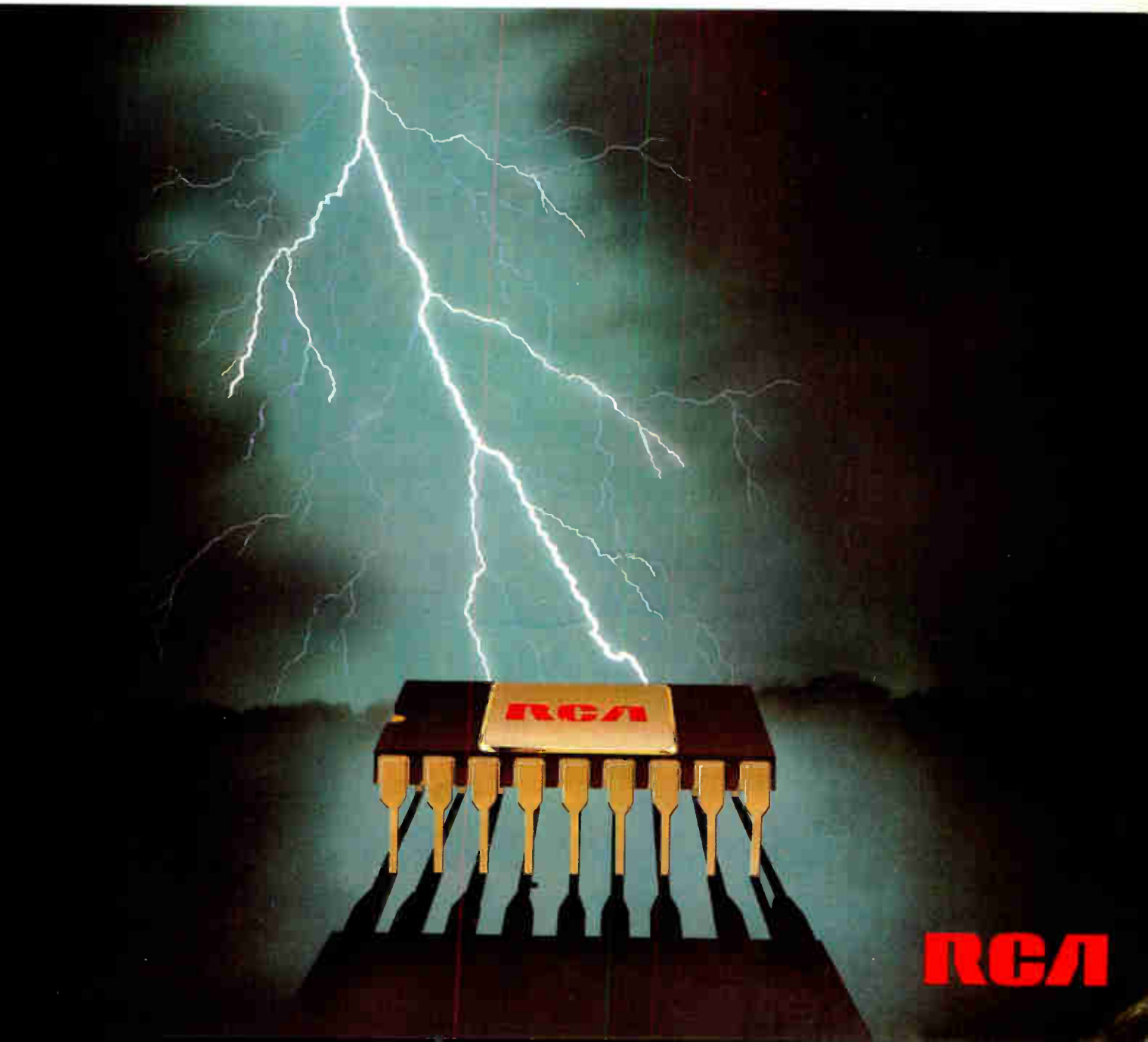

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Industrial

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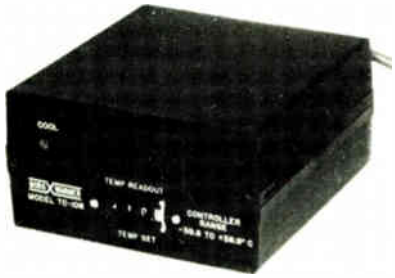
Digital temperature controllers use solid-state relays to switch heat-pump power

A digital temperature controller may cycle so fast that if it is using relays, it can run through their expected lifetime number of operations very rapidly. Solid-state relays not only add to reliability, but also let the device cycle faster, shortening the time between detection of the set temperature and the moment the power is switched.

The TC-106 and -107 from Borg-Warner use solid-state relays to control the solid-state coolers and heat pumps made by the firm. A thumbwheel switch sets and displays the desired temperature, and light-emitting diodes show the actual temperature as read by an external sensor, making the $265 controllers easy to use. The power line of the cooler or heater to be controlled is plugged into the controller, which is plugged in turn into a 110-V ac power outlet. The TC-106 is intended to control a cooler; the TC-107 is for heating.

The standard TC-106 has a temperature range of −39.9° to +39.9°C, a resolution of 0.1°C, and 0.1° hysteresis. The TC-107 has a −50°-to-+150°C range and the same resolution and hysteresis specifications. The temperature range of each is offered as an option on the other; some other options are hysteresis of 2°, 4°, or 8° for use where slower cycling is desired. The controllers include a power cord and one integrated-circuit temperature sensor. Additional sensors are available at a cost of $20 each. The line from the sensor plugs into the back of the controller.



The $265 price is for single units. Delivery is from stock.

Borg-Warner Thermoelectrics, 3570 N. Avondale Ave., Chicago, Ill. 60618. Phone (312) 588-5120 [391]

Programmable controller for small machines costs $400

Costing less to install than control panels that require four relays and a timer, the Model 510 programmable controller, a member of the 500 PC family, measures 12 by 13 by 3 in. It has been designed for small, single-purpose equipment such as punch and brake presses, drilling machines, small conveyors, and packaging equipment that are controlled by as few as four to six relays. It can also control 20 or more relays. The controller has 12 inputs to detect 120-V at 60-Hz or 24-V dc and 8 triac outputs rated at 2 A root mean square, 120 V ac. Inputs and outputs are contained on a single board that can be disconnected from the unit for maintenance. By using a hand-held read/write programmer, sequencing logic can be entered into the controller. Programming is via conventional relay ladder logic. Complex control logic can be entered via a sequence matrix chart that appears on the programmer's display. The Model 510 has 256 words of memory and 64 control relays and uses a combination of 16 timers that operate from 0.1 seconds to 30 minutes and/or counters with a maximum of 32,000 counts, as well as four drum timers with 16 steps each.

The Model 510 sells for under $400 in original-equipment-manufacturer volume. The typical electromechanical drum timers cost $600 each; the hand-held programmer sells for less than $300.

Texas Instruments Inc., Materials and Electrical Products Group, P. O. Drawer 1255, Johnson City, Tenn. 37601 [393]

Microcomputer gives timer high immunity to noise

The Series 365 Long-Ranger industrial timer has a transformer, power supply, full-wave bridges, buffered logic, and a built-in microcomputer capable of discriminating between the presence of noise and signals. According to the company, this latter feature provides the timer with a high immunity to noise not yet offered by any other industrial timer.

The microcomputer digitally clocks the timer making its reset time consistently the same duration regardless of line voltage, power supply, or time cycle. The Series 365 can be adjusted between 0.01 seconds and 999 hours in nine switch-selected ranges of 0 to 9.99, 99.9, or 999 seconds, minutes, or hours and can be easily programmed to time up to or down from the set point. Repeat accuracy is to within ±10 ms at all settings. After the time runs out, it will either stop or go. A built-in diagnostic program lets the user check whether the timer is operating properly without test instruments. Instructions for this program are printed on a flip card contained in the unit to help determine whether there is a problem in the timer or in external circuits or relays.

In a 72-mm dual in-line housing, the timer occupies 40% less space than conventional timers. Its electronic components have no moving parts and are assembled from computer-tested circuit boards. It is gasketed and O-ring sealed to prevent water and dust from entering. The Series 365 Long-Ranger is priced at $95 with display—$15.00 less without. There are additional costs for different voltage and frequency and extra features.

Automatic Timing & Controls Co., King of Prussia, Pa. 19406. Phone (215) 265-0200 [394]

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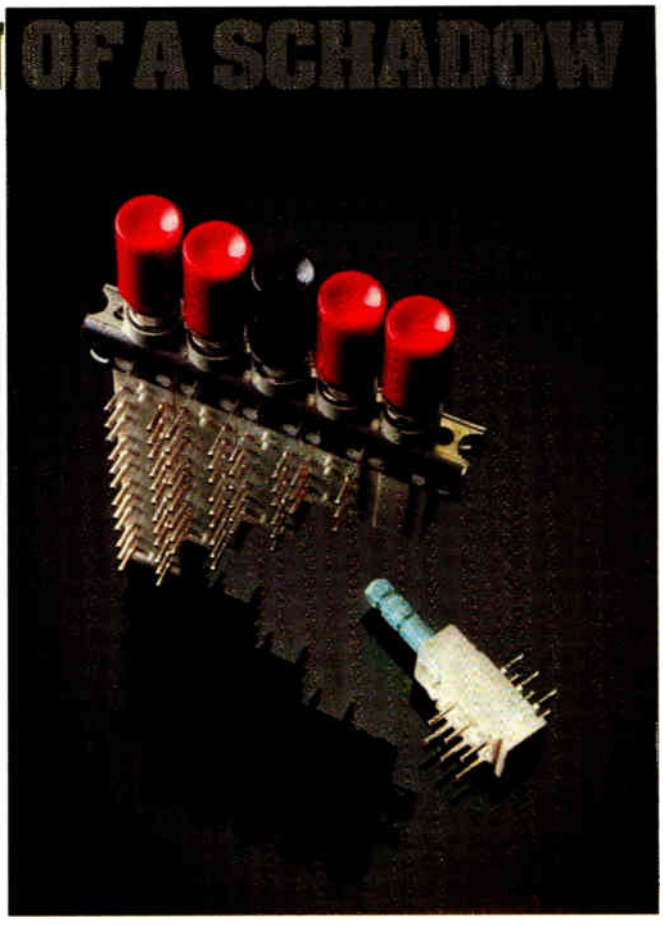

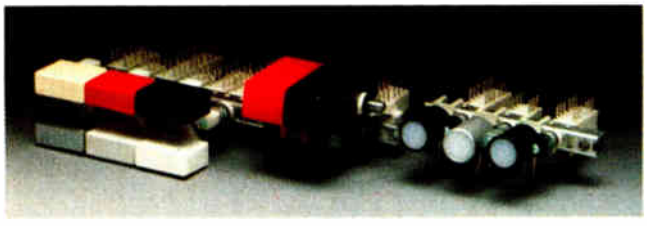

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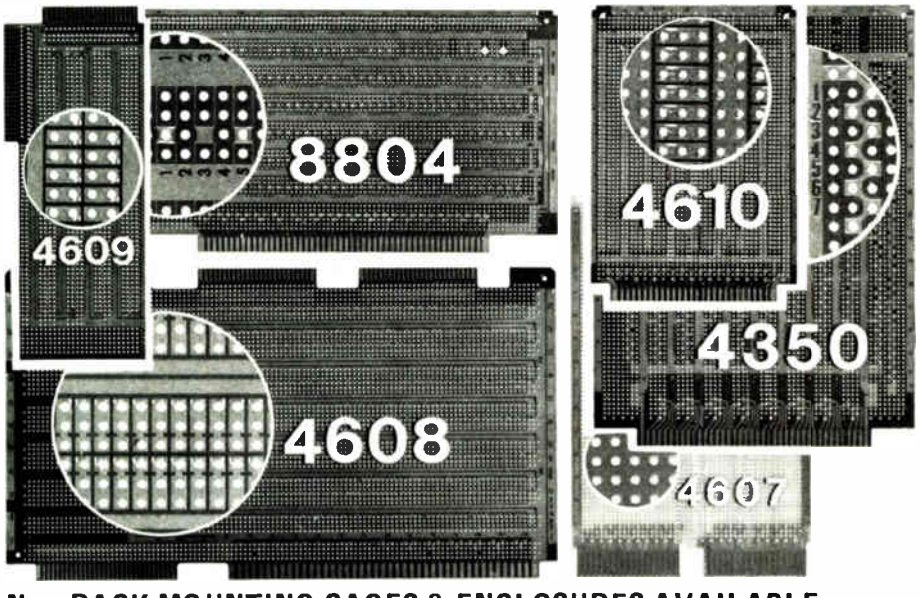

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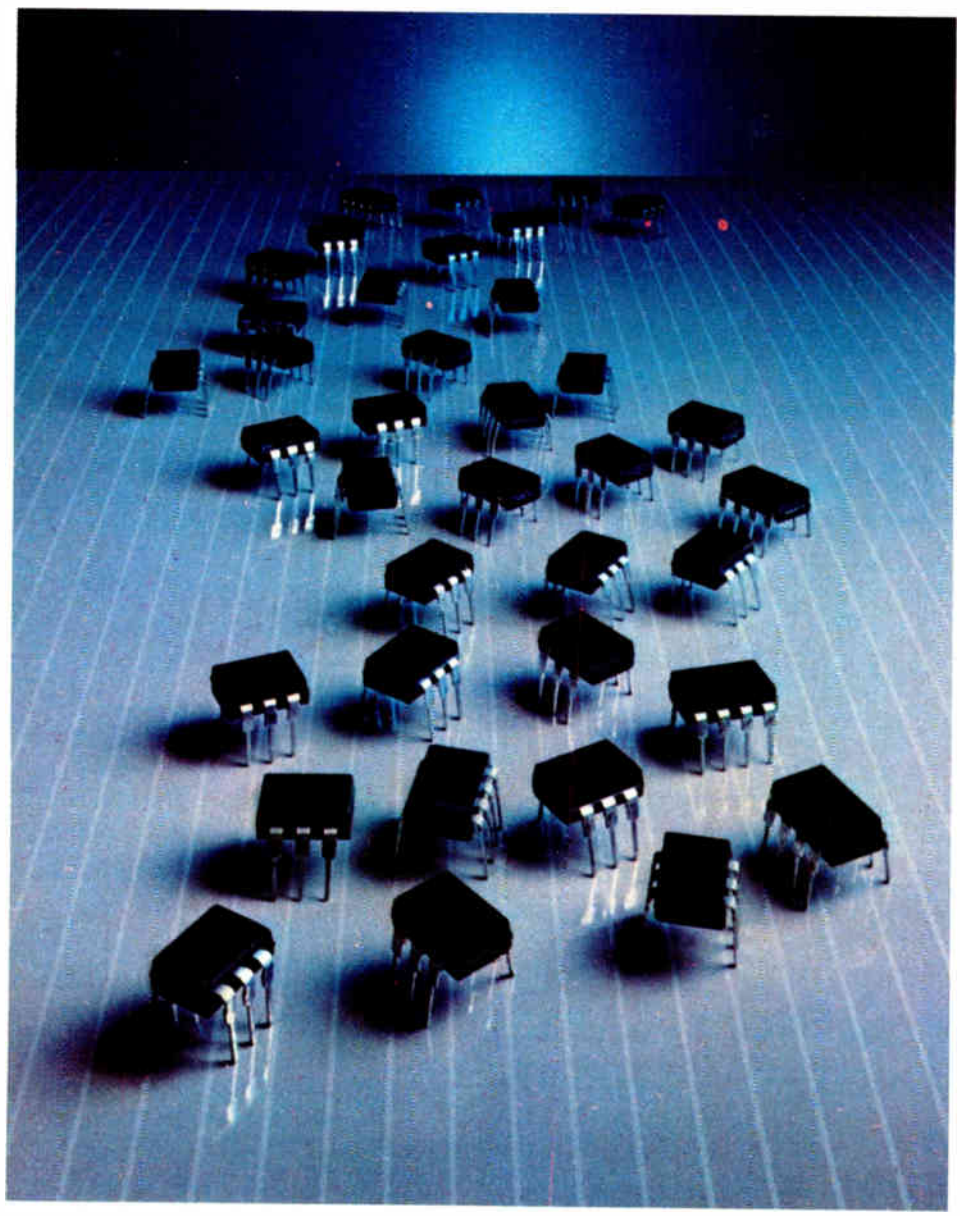

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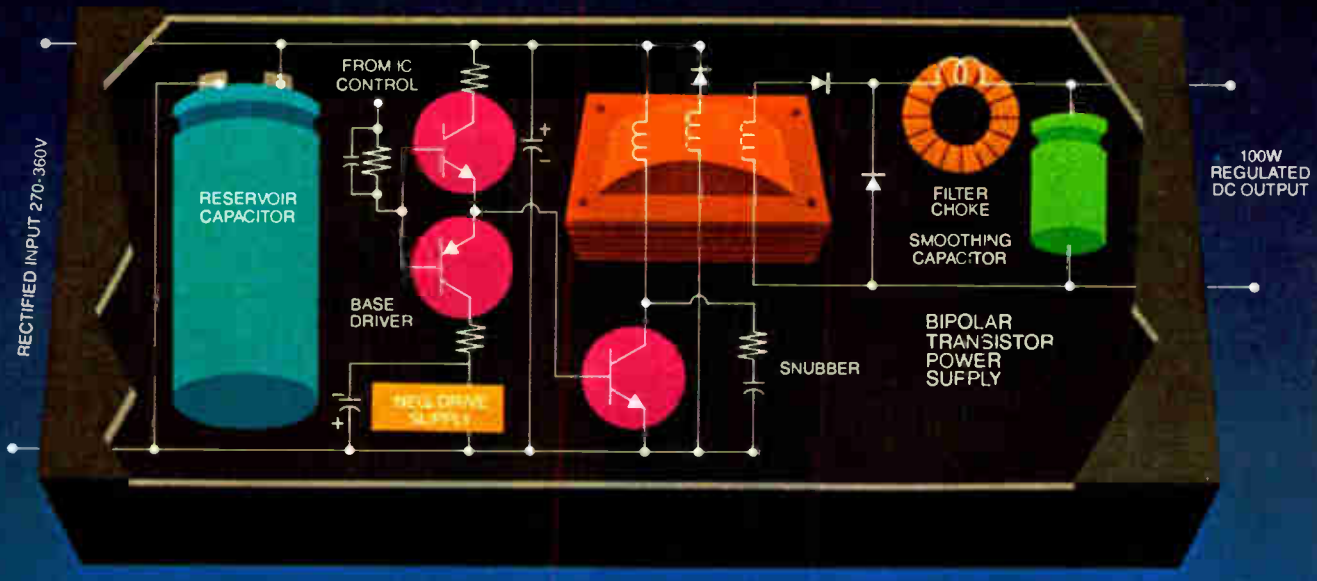

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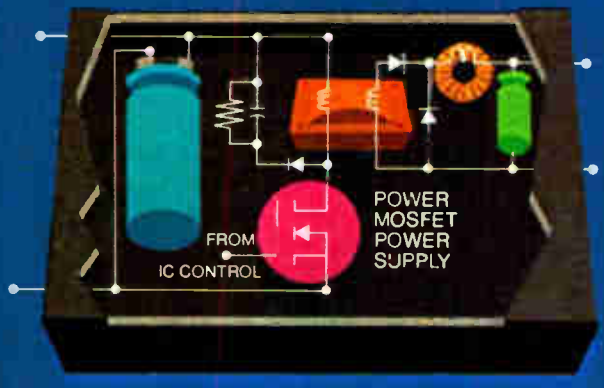

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Circle 241 on reader service card

Microcomputers & systems

Z8000 runs under Unix superset

Development system handles 16 users working with C; Pascal will be supported

Like the Z-Lab 80 announced last year, the Z-Lab 8000 uses the Z-scan module for hardware debugging chores such as in-circuit emulation, and it services Zilog's existing microcomputer products. There the similarity ends. The combination of a 16-bit Z8001 microprocessor used as a central processing unit and the adoption of Western Electric Co.'s Unix version 7 operating system makes the Z-Lab 8000 a far more powerful software development tool.

The Z-Lab 8000 extends the user community to as many as 16 terminals. It has approximately the power of a PDP-11/44 from Digital Equipment Corp., to service so many users. It offers a choice of either one or two 8-in. Winchester disk drives, as well as a tape drive. The Winchesters each have 24-megabyte capacities, and when the deliveries begin in November, a 40-megabyte drive should also be available. The tape drive is a nonstreaming type with 17-megabyte capacity. The system also has three peripheral controllers, including a serial input/output controller and intelligent ones for the Winchester disk and cartridge tape drives. Later Zilog will offer an intelligent serial I/O controller.

The system's CPU can address up to 16 megabytes in 128-K-byte segments (64-K bytes of data and 64-K bytes of instructions), and it uses up to six random-access memory cards in the CPU cage. Dynamic memory allocation is provided for: when a user's program takes up its allocated space, the system automatically finds more for it in another portion of memory. Each card has a 256-K-byte capacity using 16-K RAMs and has error-checking and -correction circuitry. Seven extra RAMs on each card provide 7 error-correction bits, giving the system the ability to correct single-bit errors and to flag multiple-bit errors. Because its 32-bit Z-bus has an 8-megabyte/second bandwidth, the system can grow into Zilog's forthcoming series of high-speed 32-bit processors [*Electronics*, Jan. 13, p. 97].

Software punch. The real advances of the Z-Lab 8000, however, are in the software. In addition to targeting the Unix operating system for use with the Z8000 instruction set, Zilog has enhanced it to include access-privilege refinements. In standard Unix there is nothing to keep two users, both of whom may have read/write access to any file, from simultaneously modifying a file, one user invalidating the other's changes. Zilog's enhancement, called Zeus, provides three access-control modes: one is the same as the standard Unix control mode; a read-only mode allows other users to read from a file

but not write into it; and an exclusive mode allows only one user to open a given file at one time.

Two other extensions written into Zeus make system reconfiguration easier. One program, Sysgen, automatically reconfigures the software to accommodate the addition of disk and tape drives to the controller. Another program, Patch, permits the distribution of operating system and utility patches either on cartridge tape or over the phone.

Zilog will support the C programming language on the Z-Lab 8000, as well as PL/Z SYS and PL/Z ASM. Zilog says it will also support Pascal by the third quarter of this year. Added utilities include a screen editor, containing numerous word-processing functions, and a spelling-error–detection program.

Single-unit pricing for the Z-Lab 8000, without terminals or printers, is $27,000 for the model 20 (with one Winchester drive) and $33,950 for model 30 (with two drives). Software costs $2,000 for a single-user version and $4,250 for a four-user version. Deliveries will be on allocation in 1981, with quantity production in the first quarter of 1982.

Zilog Inc., 10411 Bubb Rd., Cupertino, Calif., 95014. Phone (408) 446-4666 [410]

Master, slave develop systems

Development system gives user 60-K-byte space, is faster than its predecessor

A new microcomputer development system from National Semiconductor Corp. exploits the power of two microprocessors in a master-slave configuration and new high-level language support. Designated Starplex II, the system is primarily aimed at microcomputer systems designers using high-level languages, as well as those requiring support for future 16-bit processors.

Unlike its predecessor, Starplex, which had one central processing unit, the Starplex II is based on two Z80A processors. "The operating system and user programs are segregated into their respective processors, giving Starplex II a system integrity not offered in other development systems," claims Gary Mullinix, product marketing manager for development systems at National's Microcomputer Systems Group.

The master Z80A CPU in Starplex II is dedicated to the operating system and has 64-K bytes of random-access memory. The slave processor, a second Z80A, has 60-K of its own 64-K bytes of on-board RAM dedicated to user programs, compared with 34.5-K bytes of RAM in the

The Software Bus DVM

Introducing the Model 1065...a remarkable new DVM that combines outstanding hardware features with a unique and totally new software bus concept for systems operation.

A premium 5½ digit instrument, the Model 1065 features sophisticated noise rejection, unmatched long term stability, multifunction measurement capability, a superfast read mode, and excellent accuracy. It also includes Datron's exclusive error read-out, complete auto-calibration from the front panel (or on the bus) and self-test. And, it's fully IEEE-488 bus compatible.

Unique Software Bus For Quick and Easy System Programming

The 1065 goes one step further than simply offering hardware bus compatibility. It provides a software bus capability, too. The software bus is a unique series of program packages that provides simple "call-up" instructions for programming the 1065. Simple and easy to follow, it actually walks you through the programming routine in plain English. As a result, programs can be written in a matter of minutes or hours rather than the days or weeks it would take to perform the same chore in machine language.

Software bus packages are available for HP, TEK, Commodore and other popular controllers. Each package includes complete DVM and system control instructions plus a wide range of data acquisition and data processing functions. These functions include math, statistics, ratio, linearization, conversion, dB, scaling and offsetting, all performed quickly and efficiently by the controller under the direction of the Datron Software Bus Control Package.

Add to this unique software capability the five trigger modes, five SRQ modes, parallel and serial polling, binary program dump and the ability to operate every front and rear panel facility on the bus and you can see why we call the 1065 a remarkable systems machine.

Best For Bench Use, Too

One of the basic design concepts of the 1065 was simplicity. A quick look at the front panel confirms how effectively that has been achieved. No confusing multi-colors or arrows. All keys grouped logically. A clear, bright display with full annunciation. Simple to operate plus a "time-guard" feature that eliminates fat-finger errors. A remarkable bench instrument, too.

For additional information on this bus or bench instrument write: Datron Instruments, Inc., Laguna Hills Business Park, 23011 Moulton Parkway, Laguna Hills, CA 92653. (714) 830-8860.

datron
INSTRUMENTS, INC.

Circle 243 on reader service card

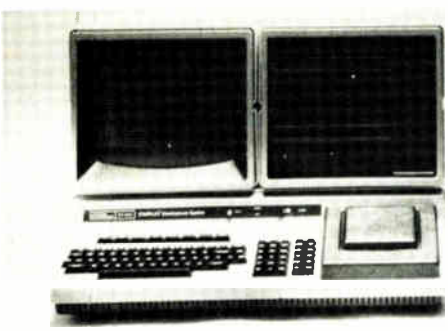
earlier Starplex system.

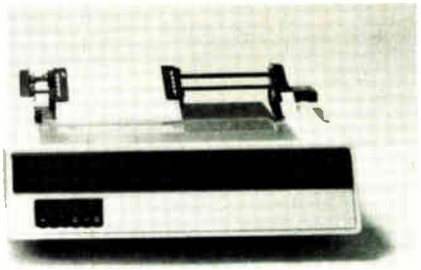
In contrast to the initial Starplex system, where a bug in the user program "could cause the entire operating system to die by overwriting or jumping into the middle of a system routine," notes Robert W. Freund, engineering manager, the Starplex II user "cannot accidentally destroy the operating system."

Optional high-level support for Starplex II includes PL/M and Pascal. Code generators for the 8080/8085 and Z80/NSC800 8-bit processors are available for the PL/M and Pascal compilers. Also available is the CP/M interface option offered on Starplex. With this high-level language support and the additional RAM, Mullinix notes, "Starplex II offers a performance increase of up to three times that of Starplex."

An input/output-spooled printer capability lets the Starplex II user print at the same time he is editing, compiling, assembling, or doing any other development-system work. "This makes better use of engineering resources," Mullinix says. "Other microprocessor development systems become very expensive printers" when used in a print-only mode.

A programmed-function keyboard with eight upper- and lower-case keys accesses a total of 16 user-definable programs. When the system is in the command mode and prompts the user to do so, these software function keys can be used to load and execute any 16 programs previously entered. When an application program is running, these 8 keys will be passed to that program and can be used for any function.





Starplex II also has a resident debugging utility. The program does not occupy any user memory space and can be called up by a simple keystroke at any time during program execution. Previously, the debugger in Starplex had to be specified prior to program execution, and used the top 4-K bytes of memory.

With the new development system, the user can also open six files besides the keyboard and cathode-ray-tube display, for a total of eight. Other enhancements in Starplex II are its two RS-232-C serial input-output ports and its dual floppy-disk subsystem with double-density, single-sided (1-megabyte) or double-sided (2-megabyte) drives.

The universal programmer personality module for programmable read-only memories that was optional on Starplex is standard on Starplex II, and it "is being extended to support programmable array logic devices and, eventually, most, if not all, other programmable devices from National," Mullinix says.

A typical Starplex II configuration consists of: two Z80A-based CPUs; 128-K bytes of RAM; 1 megabyte of floppy-disk storage (two drives); video monitor and keyboard; disk-based operating system; debugger, text editor, assembler, linker, Fortran, Basic, utilities, and diagnostics; and the universal programmed interface and software for PROMs and PALs. Designated SPX-90/51, this configuration costs $15,950. The 2-megabyte floppy-disk configuration, SPX-90/61, costs $18,600. The Pascal and PL/M code generators are $2,000 each. All can be delivered in 30 days.

Current users of Starplex will be able to upgrade their system's performance to Starplex II capability by purchasing a special upgrading kit, the AEE-A61, that will cost $2,000 during the first 90 days of availability and $3,000 thereafter. The kit will consist of the two Z80A CPU boards, a new keyboard, and new operating system software. During the first three months, any two high-level–language code generators bought with the kit cost $1,000.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone (408) 737-5000 [411]

Chassis holds 32 megabytes

One board in cage has all control circuitry; array cards carry 288 64-K RAMs

Motorola's first general-purpose memory system uses array cards mounting 288 64-K dynamic random-access memory chips and can accommodate up to 32 megabytes of memory at $8,800 per megabyte (in larger configurations).

The first members of the Systems 3000 family will be the 3268, compatible with the EXORmacs development system for the 68000, and the 3200, offered to customers with custom applications. With a single 2-megabyte array card, the basic 3200 and 3268 systems cost $30,700 and $32,500, respectively.

Included in the standard packages are: card cage, power-supply module, motherboard, two terminator boards, address-control card, error-correction card, cables, interface card, and one card of 64-K RAMs. The standard 3268 unit also includes interface features for compatibility with EXORmacs products.

With the basic 3200 system (one array card), a user has an average memory cost of $15,300 per megabyte. But additional 2-megabyte cards cost $16,800 each, so adding cards causes the cost per megabyte

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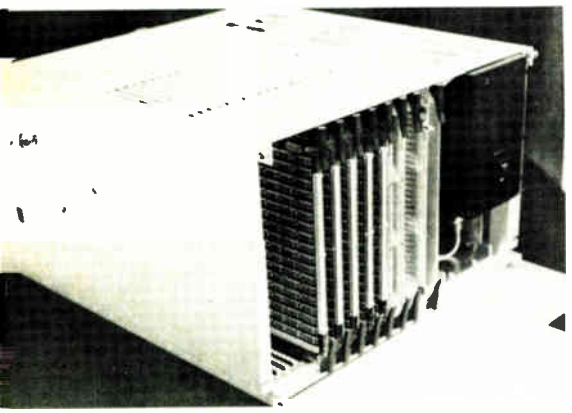
Circle 245 on reader service card



to drop quickly. The chassis has room for 16 array cards and three user slots. Motorola has condensed timing control to a single card, which enabled designers to put the maximum amount of RAM on the add-on cards.

Blocking the array circuitry this way makes the system easier to test and debug, the firm says, and it provides a cost advantage when the unit exceeds 4 megabytes. Users will not have to pay for the additional control circuitry as more array cards are added.

Big words. Depending upon the user's requirements, the system can operate on words up to 72 bits wide—64 bits for data and the rest for check bits. An optional error logger can be located on the front panel of the 12.5-by-17.5-by-21.2-in.-deep chassis.

Data-transfer rates depend on other user hardware. "Byte reads are multiplexed on the user interface card to give an effective data rate of 16 megabytes per second," Motorola explains. "Through the use of parallel read, with sequential addressing, an effective transfer rate of 64 megabytes per second can be established."

At the memory bus level, the system can have an access time of 350 ns with error correction, or 275 ns without. It can also operate on an average cycle time of 500 ns with ECC, or 400 ns without.

Interfacing with the system is simplified by the use of a large (11.4-by-18-in.) user card. Applications include additions to main memory, disk replacement, and disk cache. An intelligent controller on the user card enables the system to handle any type of custom requirement, the company says. In addition to the standard 64-K RAM cards, Motorola indicates the product could be loaded with 32-K RAMs.

Motorola says it is delivering prototypes of the system, and availability of production units is set for June. The company, which until now has offered only custom-made memory systems, is also planning to introduce a mini-chassis made for the 3000 series that will be available in the third quarter. The same cards can be used in either chassis.

Motorola Inc., Memory Systems, 3501 Ed Bluestein Blvd., Austin, Texas 78721. Phone (512) 928-6776 or (800) 531-5118 [412]

4-bit C-MOS microcomputer chip connects to 8-bit system

OKI Semiconductor is entering the U. S. microcomputer market by introducing its series 40 complementary-MOS single-chip 4-bit devices—five microcomputers, plus a full set of program development tools. Three of the five circuits, the MSM5840, the MSM5842, and the MSM5845, are available now. Two more, the MSM58421 and the MSM58423, will be available by the second quarter of this year.

The 5840 is a peripheral unit containing a 2-K-by-8-bit read-only memory, a 128-by-4-bit random-access memory, a programmable timer-counter, and 30 input/output lines. Featuring an 8-bit parallel I/O port and 4-bit-wide data paths, the 5840 can easily connect to an 8-bit system. The 2-K-by-8-bit ROM can be externally expanded with a multiplexed bus structure.

Prices for the series 40 devices in quantities of 100,000 or more are $6.00 each for the 5840 and $2.85 each for the 5842. Program-development packages offered include the MPSP-I, based on Intel's ISIS software and priced at $1,942.50; the MPSP-C, based on Digital Research's CP/M operating software and also priced at $1,942.50; and the MPSP-S, designed for those who do not own a development system and priced at $1,485.50.

Oki Semiconductor, 1333 Lawrence Expressway, Santa Clara, Calif. 95051. Phone (408) 948-4842 [413]

All-C-MOS microcomputer requires only 5 V to run

What may be the industry's first completely complementary-MOS microcomputer system, the model PPS-12, requires only 5 V for operation, and most system configurations will require less than half a watt of power. The compact system, designed to fit into any standard Multibus card cage, employs a 12-bit IM6100 C-MOS microprocessor and has been specifically designed for data acquisition and control in remote locations where only battery or solar power is available.

The central processing module includes three parallel input/output ports, one optically isolated 20-mA and one RS-232 serial I/O port, a programmable real-time clock, 4-K words of C-MOS random-access and erasable programmable read-only memory, a memory-expansion controller, and an on-board transparent monitor and debugger. The PPS-12 is also supported by a dozen system-expansion modules.

Software development can be carried out on any PDP-8 or VT-78 DECstation minicomputer because the 6100 microprocessor used in the PPS-12 employs a binary instruction set identical to that of these two machines. The company's Omega microcomputer is also available in a configuration that is fully integrated with the PPS-12 to facilitate development. Furthermore, the firm's model 660 C-MOS E-PROM programmer is also available for programming the 6653 C-MOS E-PROMs used in the system. Single-quantity price for the PPS-1201 CPU module is $990. Delivery takes 30 days after receipt of order.

Pacific Ciber/Metrix Inc., 6800 Sierra Court, Dublin, Calif. 94566. Phone (415) 829-8700 [415]

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Circle 247 on reader service card

Software

Portable language is full-featured

A commercialization of SAIL, Mainsail is independent of machine and operating system

Born in the artificial intelligence community, the Mainsail language is an attempt to realize the programmer's dream of obtaining maximum flexibility, simplicity, and power while retaining absolute portability. Minsail was designed to be machine–and operating-system–independent. Its character set is restricted to maintain portability, its data typing is portable, and it has a common strategy for all of its code generators. Much of Mainsail's development was funded by its preannouncement customers, and Intel Corp. has already used it to write software for its in-house computer-aided design systems.

Mainsail is an extension, formalization, and commercialization of the Stanford Artificial Intelligence Language (SAIL) developed by the Sumex computer project at Stanford University. It was developed primarily by Clark R. Wilcox, who is now president of Xidak Inc., a company formed to market the language to commercial users.

Although one of Mainsail's goals was to achieve complete portability, the approximately 300-K bytes of memory needed for the run-time program requires at least a powerful minicomputer to implement the language. To date, Xidak has developed working versions of Mainsail for Digital Equipment Corp.'s PDP-11, PDP-10, PDP-20, and VAX computer families.

On the PDP-11, it will run under RT-11 and RSX-11 operating systems. On the PDP-10, it will run under TOPS 10, TOPS 20, and Tenex, whereas on the VAX it will run under VMS, Unix, and a Unix emulator called Eunice developed by SRI International. The PDP-11 versions run slowly, however, because the machine's limited address space forces continual use of the disks.

In the second quarter, IBM systems running under VM/CMS will be added to Mainsail's repertoire, and in the third quarter a Motorola 6800-based system running under VERSA-DOS will also appear.

Task-easing features. What makes Mainsail a desirable language, compared with other languages like Pascal and C, is an impressive list of programmer-oriented features, only a few of which are included in the other two languages. Mainsail features include variable string lengths, manipulation at the bit level, dynamic array allocation, a "garbage collection" routine that methodically recycles unused program space, compile-time libraries, position-independent code, dynamic linking and loading, random file accessing, conditional compilations, embedded assembly language, recursive procedures, low-level memory access, and a few other twists that make a programmer's life easier.

Mainsail does not include a linkage editor, because intermodule linkage is specified within the language definition. Its compile-time features, including macros and conditional compilation, make it easier for groups of programmers to work together on large portable programs consisting of hundreds of modules. Cross-compilation of code between systems is a useful by-product of Mainsail's structure.

To the features of the language's development-system package, which includes a compiler and comes in the form of tape and hard copy documentation, Xidak has added a symbolic debugger that is now at the beta test-site stage. The symbolic debugger places source text on screen and indicates the position and nature of an error. Deliveries of the DEC-oriented versions of Mainsail are in 30 days, with pricing dependent upon the power of the target processor. The one-time licensing fee for a VAX-780 development-system package, for example, is $8,000. The symbolic debugger will be priced separately at under $4,000.

Xidak Inc., 885 N. San Antonio Rd., Los Altos, Calif. 94022. Phone (415) 948-4387 [371]

C language is available for Z80-A–based S-100 systems

The C programming language, originally developed and implemented on the Unix operating system, is available for use on Cromemco Z80-A–based, S-100–bus microcomputer systems. It combines the features provided by assembly languages with the structured programming techniques available in higher-level languages. This version operates under Cromemco's multiuser, multitasking Cromix operating system, producing relocatable code that can be linked with Fortran, Cobol, and assembly language or can be called from Basic. The language is available on 5-in. diskettes (model CCC-S) or 8-in. diskettes (model CCC-L), including extensive documentation, for $595.

Cromemco Inc., 280 Bernardo Ave., Mountain View, Calif. 94043 [373]

C compiler generates object code for Motorola 68000

The C68 compiler system generates object code for the Motorola 68000, executing on any PDP-11 processor that runs the Unix operating system. The compiler system consists of a preprocessor, a compiler, a relocatable assembler, a linking loader, support library, and utilities. Programs generated by the system will execute alone or under operating-system control on the 68000.

The compiler in the system produces assembly language, which is then assembled into relocatable object code by the assembler. The linking loader then combines the relocatable object files with the referenced library functions to produce an executable object file that includes a symbol table. A utility program transmits the executable object code

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Alcyon Corp., 8474 Commerce Ave., San Diego, Calif. 92121. Phone (714) 578-0860 [374]

Interactive proofreading is available for microcomputers

Thanks to a fast interactive program called MicroSpell, a microcomputer can proofread as well as a large computer. The software package includes a dictionary of about 20,000 common English words to which 14,000 more may be added.

MicroSpell looks up each word of the text file in its dictionary, searching for potential misspellings, guessing at the correct spelling, and then allowing the user to replace the misspelled word with one of the guesses pulled from its dictionary. It is also possible to just probe the dictionary for the correct spelling of words without a text.

To the program can be added an auxiliary dictionary of specialized or technical terminology and a spelling-correction dictionary that looks for common misspellings and automatically replaces them with the correct spelling, expanding to include every new pair of misspelled and corrected words in its listing.

On a system with a 2-MHz clock and a double-density floppy, MicroSpell takes about 12 min. to check and fully correct a page of text. The program plus complete documentation is $249; documentation alone is $20.

Lifeboat Associates, 1651 Third Ave., New York, N. Y. 10028. Phone (212) 860-0300 [377]

8086, 8088 cross assemblers offer enhancements

The Millennium 8086/8088 cross assemblers for generating programs for the Intel 8086 and 8088 family improve on the features offered by Intel's MCS-86 assembler by enhancing the instruction mnemonics, assembler directives, macroinstruction implementation, conditional assembly, and relocatable output capabilities. It includes a macro assembler, a linking loader, and a formatter and downloader to transmit the program to a MicroSystem Designer for execution and debugging.

The cross assembler will run on Digital Equipment PDP-11 and LSI-11 minicomputers under either RT-11 or RSX-11; Data General Nova 1200 or Eclipse minicomputers under either RDOS or AOS; HP 1000 or HP 3000 machines; or the TI 99/10. The cross assembler costs $1,500 and is available in 30 days.

Millennium Systems Inc., 19050 Pruneridge Ave., Cupertino, Calif. 95014. [375]

RDS Pascal is ready for two DG operating systems

The RDS Pascal language is available for use with Data General's latest operating systems: the MP/OS for the microNova and Nova/4 computers and the AOS/VS for the 32-bit MV-8000. It was already available for the company's other disk-based operating systems: AOS, RDOS, and DOS. All the compilers of RDS Pascal generate pseudo-code, which can be used across the Data General product line yet still permit the features of each system, such as a floating-point processor, to be used.

RDS Pascal is closer to the proposed International Standards Organization's standard for Pascal than any other implementation available for Data General systems, says the creator of the language. The license fees (plus a one-year update) are $2,500 for RDS Pascal for the MP/OS operating system and $3,500 for the language for the AOS/VS. Update renewal is $300 and $400, respectively. For $50, a user can get a programmer's manual and a 60-day license for the software.

Rational Data Systems, 245 W. 55th St., New York, N. Y. 10019 [376]

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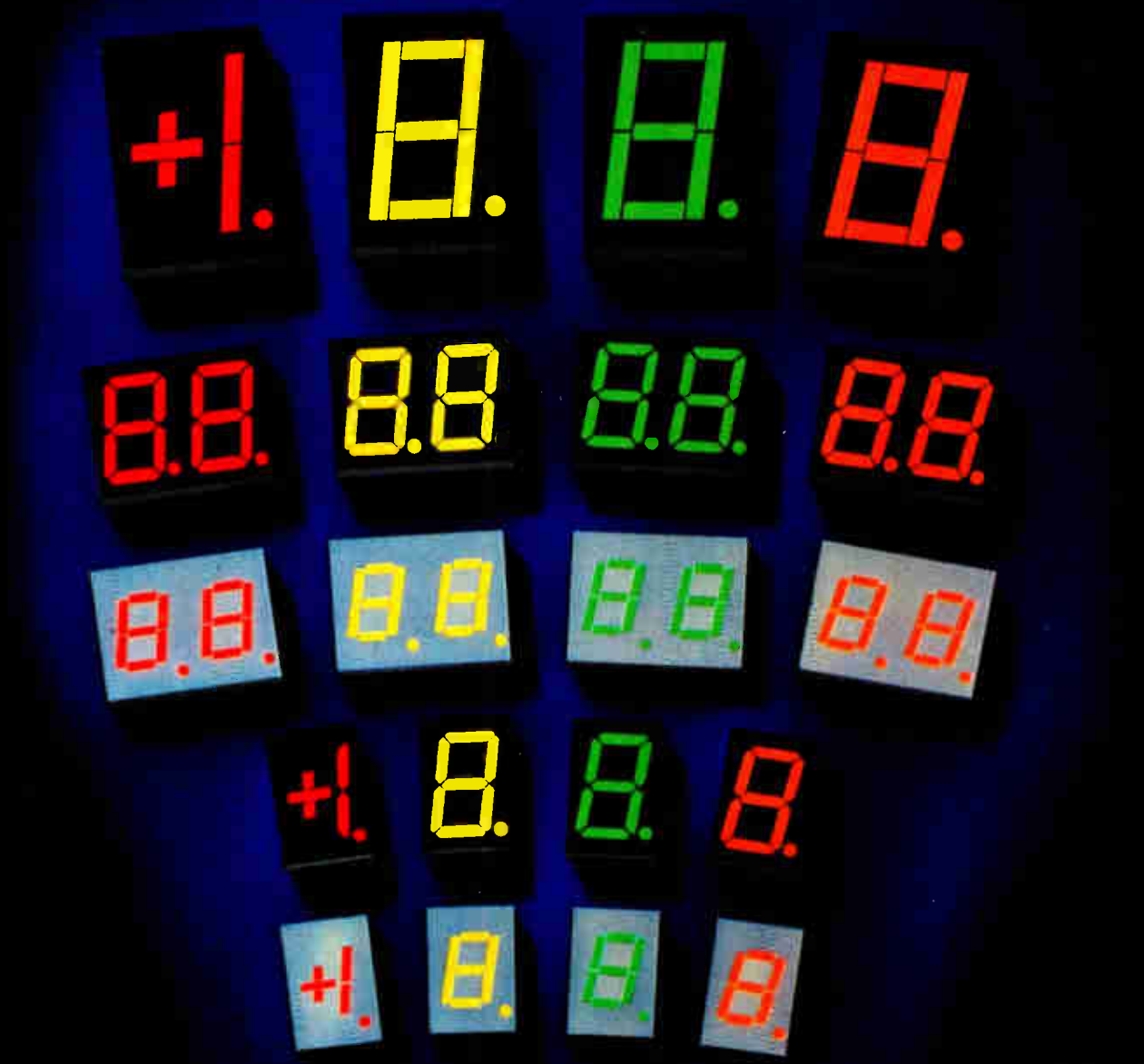

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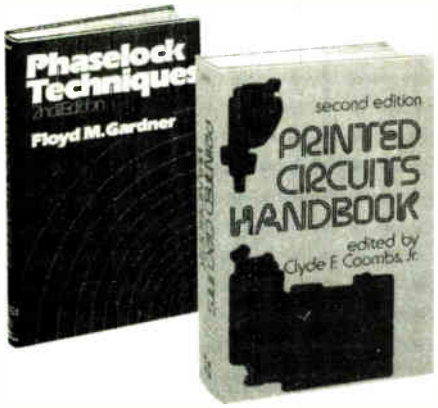

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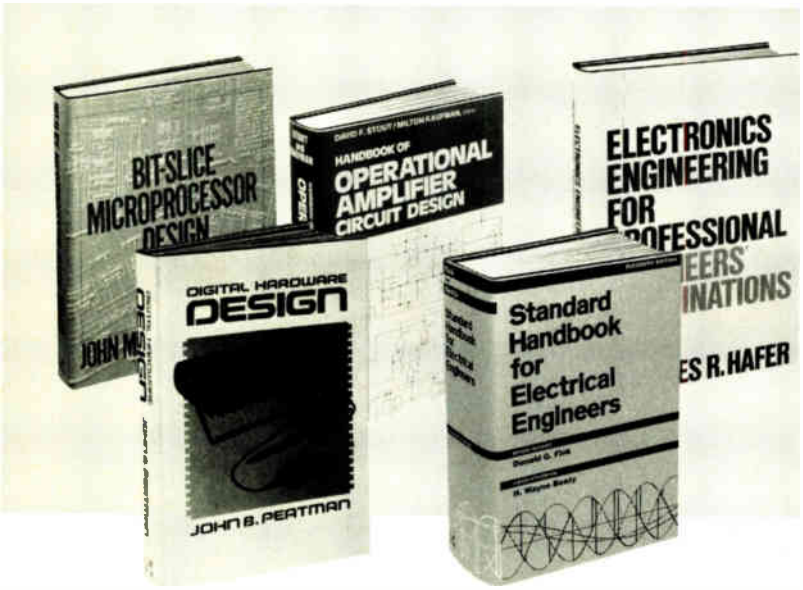

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New literature

Optoelectronic devices. "The 1980 Product Selection Guide" contains detailed information on a line of light-emitting-diode lamps, displays, and optoisolators. The 20-page brochure lists device identification numbers, suggests applications, and discusses color options for the products, including green, orange, red, and high-efficiency red. It lists specifications on the MAN series of LED displays and shows their actual digit size. Information on brightness or luminous intensity, types of pin connectors, and 13 different display package styles with complete sizes and configurations are provided. For the MV series of LED lamps, actual package size is also shown and specifications such as luminous intensity at forward current, maximum power, and typical viewing angle are given along with diagrams for package styles. Data for the optoisolator line covers actual size, output configurations, emitter voltage, the minimum output voltage of the detector, and so on. Three package styles for this line of transistors, Darlingtons, silicon controlled rectifiers, logic gates, and ac-line monitors are included. For a copy, contact the Marketing Communications Department, Optoelectronics Division, General Instrument Corp., 3400 Hillview Ave., Palo Alto, Calif. 94304. Circle reader service number 421.

Reed switches. An eight-page catalog describes a complete line of reed switches and gives specifications and dimensional drawings on dry reed switches in miniature (forms A and C) and standard size and on mercury-wetted reed switches in miniature forms A and C. The technical data in the guide simplifies the selection of reed switches requiring breakdown voltages to 15,000 V dc and switching characteristics of dry circuits to 100 W. A cross reference and applications guide and a stocking range chart not found in previous catalogs are featured. For a copy of Catalog 00001A, write to Walter Bruenger, Customer Service Manager, Hamlin Inc., Lake and Grove Streets, Lake Mills, Wis. 53551. [422]

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Burst-multiplexer channel helps Eclipse speed up

Operating at its highest transfer rate—20 Mb/s—a Data General Corp. 16-bit Eclipse S/140 computer equipped with a burst-multiplexer channel (BMC) can outdo any competing computer, claims the Westboro, Mass. firm. The BMC multiplexes data between disk and main memory on the bus linking the central processing unit and the main memory, **achieving data-transfer rates of 3.3 to 20 Mb/s.** It supports up to four disk stores or device controllers, and each controller can manage up to four disk drives itself—all of which makes for very large data bases that can be manipulated at much greater speeds than before. Priced at $2,500 and offered as an option on the S/140's error-detection and -correction board, the BMC takes no additional internal space and is deliverable in 90 days.

J-FET–input dual op amp is ready for military

The OP-215 precision dual operational amplifier with junction field-effect-transistor input introduced last spring by Precision Monolithics Inc., Santa Clara, Calif., is now also available in three military grades. Similar to the commercial part (E suffix), **the top military device (A suffix) has an input offset voltage of 1 mV at room temperature** (25°C), but is rated for 2 mV at full temperature (125°C), compared with 1.5 mV for the commercial unit at full temperature (70°C). In contrast, the more relaxed military grades (B and C suffixes) have offset voltages of 2 and 4 mV, respectively, at 25°C and 3 and 6 mV, respectively, at 125°C. In TO-99 packages, the A, B, and C versions are priced at $30, $21, and $10 each, in 100-piece lots. They also are available with MIL-STD-883 class B processing for a 20% premium and in an eight-pin mini-Cerdip for 20% less.

153 versions of dc-dc converters are 72% efficient

The DCS series of dc-to-dc power converters from Intronics Inc. comes in 153 different flavors. Available in 30-, 50-, and 100-W versions, the converters accept input ranges of 9 to 18 V dc, 18 to 36 V dc, or 36 to 72 V dc and deliver 17 possible single-, dual-, or triple-voltage outputs. The line's **high-efficiency rating of 72% varies less than 3% over the full input range,** says the Newton, Mass.–based company. Input-to-output isolation is 1,500 V dc, and operating temperature is −25° to +70°C. Prices start at $219 each in lots of one to nine, and delivery takes four to six weeks.

Features abound in thermocouple transmitter

There's a thermocouple-transmitter module coming from Analog Devices Inc. that **combines isolation (to 1,500 V) and cold-junction compensation in a single package.** The Norwood, Mass., firm's 2B50 is said to have no competition in its combination of features—and there is a laundry list of them: 0.01% nonlinearity, filtering, transient-voltage protection, 160-dB common-mode rejection, 70-dB normal-mode rejection, 1-μV offset, and an adjustable input span of ±5 to ±200 mV. Analog Devices expects to announce the module almost immediately.

V-f converters retain performance at lower cost

The 3800-series line of hybrid voltage-to-frequency converters due soon from Dynamic Measurements Corp. **have output frequencies ranging from 2 to 10 MHz.** Having reviewed the market—mostly analytical instruments and industrial control equipment—the Winchester, Mass., company found that by relaxing some input and power-supply requirements, it could cut the going price for such performance about in half without sacrificing either linearity or performance over temperature.

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Career outlook

Professional group aids women

■ With engineering and technical manpower shortages reaching critical proportions, companies are tapping nontraditional pools of talent within their firms. Among those being beckoned along these unfamiliar career paths are women, many of whom are technically ill-prepared and have few places to turn to for technical training.

Women in Electronics is a professional association and information center now being organized at the local level on the West Coast in Orange County and the San Fernando Valley, in Denver, Boston, Florida, and New Jersey, and on Long Island. It hopes to provide a meeting ground and source of career and technical information for these women and their current or prospective employers.

"One of our objectives is to share problems and information. Men seem to have this type of network going informally, and if something happens in the industry, they seem to know about it," notes Phoebe M. Blinder, president of the Long Island chapter. "Many women must hold down two jobs—career and family—and many are also going to school. They just don't have the time or opportunity to meet with their peers in this technical industry." She notes that up to 60 women have come to each meeting so far.

Blinder, who is vice president of QPL Components Inc. and president of Phoebe Electronics Inc., both distributors of high-reliability components in Ronkonkoma, N. Y., wants to help women increase their professionalism through technical education. To that end, the Long Island chapter is sponsoring a two-day technical seminar entitled "From Ohm's Law to Microprocessors" on April 13 and 14. The Long Island group is also planning to be quite visible at this year's Electro activities in New York. It will be cosponsoring the preceding Purchasing Day seminar and will have a table in the main lobby of the Coliseum throughout Electro to answer questions and disseminate literature.

"We're looking at a potential audience we haven't tapped before," confirms Harry Fallon, chairman of the Purchasing Day committee. His company, Federated Purchaser Inc. of Springfield, N. J., employs 40 people, most of them women. "Finding enough competent people in this industry is difficult. It's like a blood transfusion—you don't care where the blood comes from if you need it," he notes.

"The whole concept of our professional people meeting other professionals and sharing ideas can only aid our company," observes Joseph Friedman, group director of human resources at General Instrument Corp.'s Hicksville, N. Y.-based Microelectronics division. GI is supporting its professional women in their Women in Electronics memberships because, as Friedman points out, "we're in an industry that needs its people resources and whatever we can do to enhance these resources we will." **-Pamela Hamilton**

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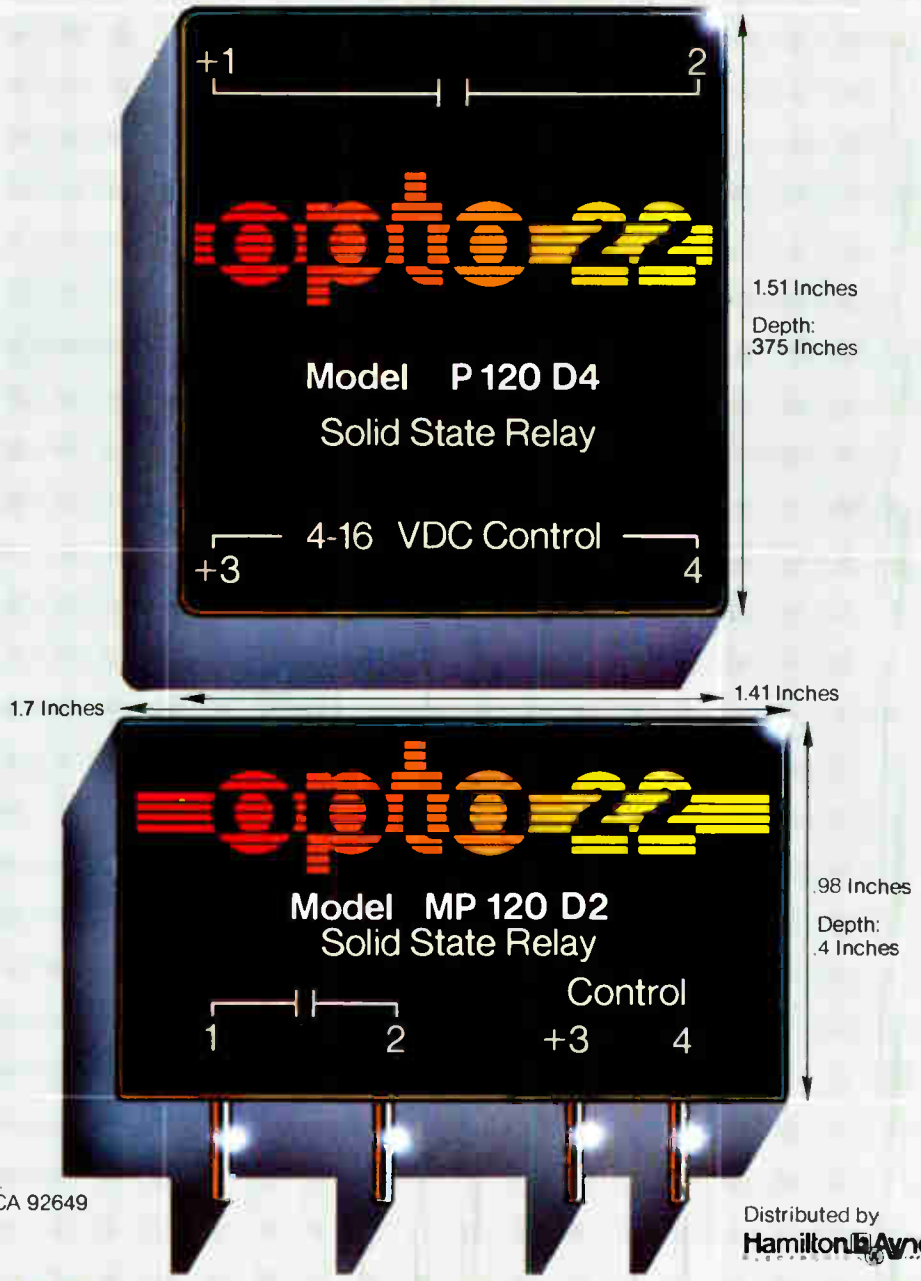

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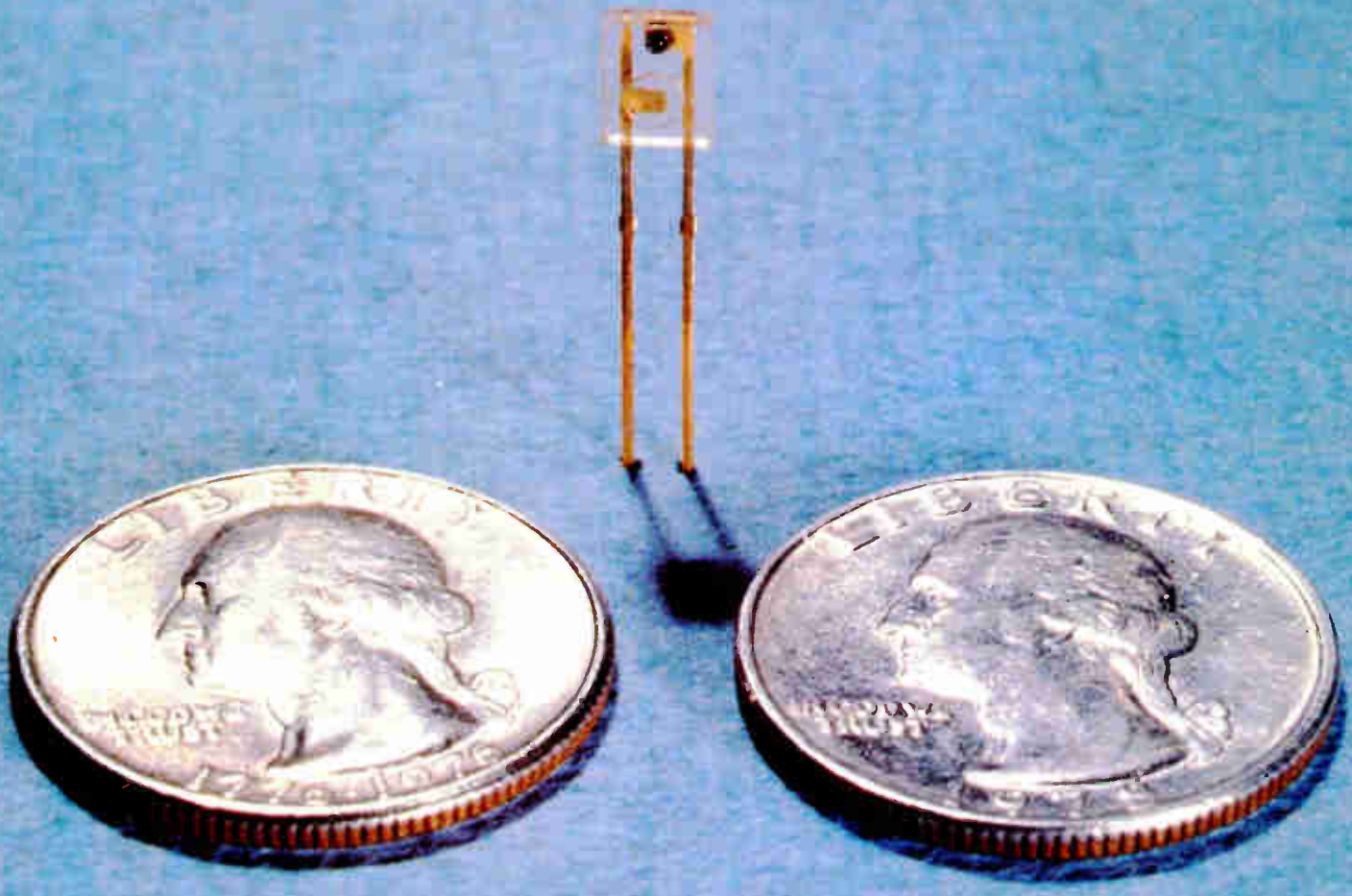

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