FEBRUARY 10, 1981

SPECIAL REPORT: HOW ADA EXCELS OTHER COMPUTER LANGUAGES/127

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GIVING VOICE TO TEXT

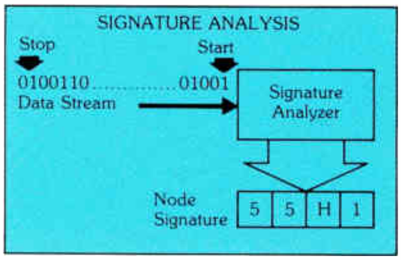
7. **Circuit Board Testing Update/No. 7 in a series from Hewlett-Packard.**

SIGNATURE ANALYSIS: A NEW AND EFFECTIVE METHOD OF TESTING MICROPROCESSOR-BASED BOARDS AT SPEED

If you're producing microprocessor-based products, you've probably found that board level testing is no trivial problem. That's because the complexity of the microprocessor (MPU) has introduced a number of new testing problems, especially when the boards must be tested at operating speeds.

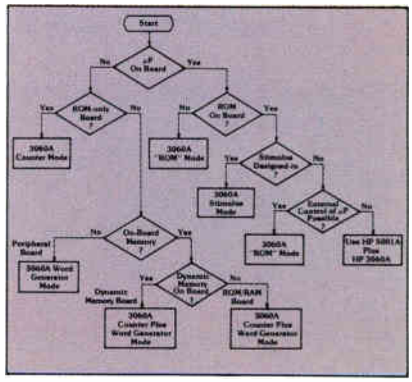
What are the new testing problems?
At-speed testing of dynamic devices creates five major problems: 1) Synchronizing most test systems with the MPU's fast on-board clock isn't possible; 2) The MPU's bi-directional bus makes fault isolation difficult; 3) Existing test systems often aren't fast enough to test today's dynamic memory devices thoroughly; 4) Most test systems cannot exercise the MPU's software — a must, and 5) Functional test development costs are increasing with device complexity. To solve these problems, Hewlett-Packard created new testing techniques.

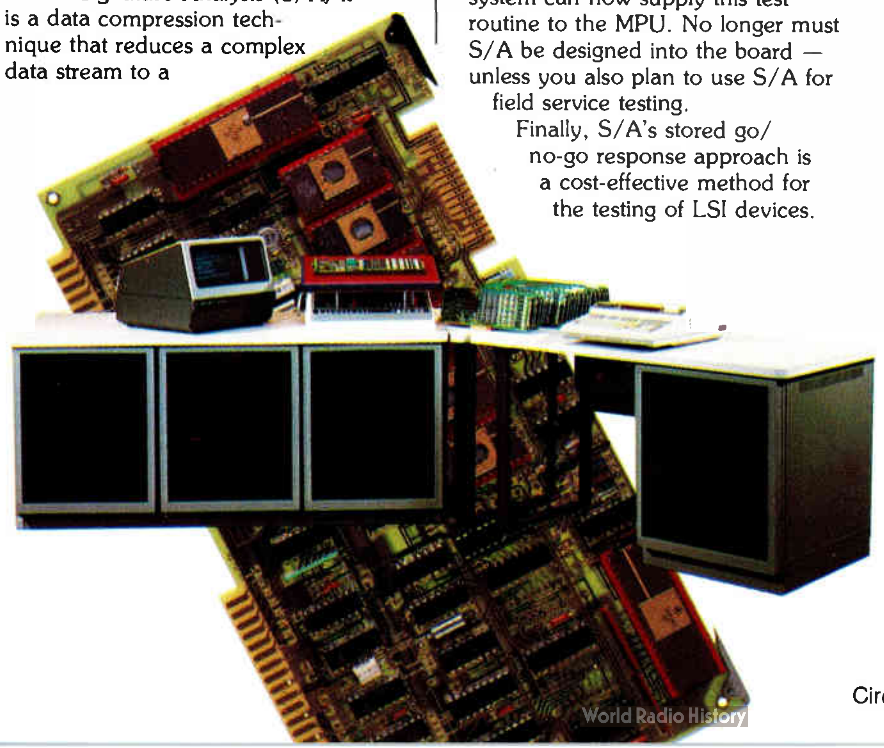
How HP developed Signature Analysis.
In 1977, as a means of reducing field service costs, HP developed a new method of testing dynamic devices. Called Signature Analysis (S/A) it is a data compression technique that reduces a complex data stream to a series of unique four-digit hexadecimal signatures. Under test, the signature of each circuit node is compared to a stored value, making it easy to locate faulty nodes.



Solving the five major problems.
Signature Analysis has made MPU board testing manageable by solving the testing problems outlined above. First, S/A can be synchronized with the MPU's on-board clock at rates up to 10 MHz. Second, interacting with the board under test, S/A can verify the data stream from a specific device on bi-directional buses. Third, the S/A technique is fast. It can locate speed-related faults in dynamic devices. Fourth, with S/A, the board under test is stimulated with a software test routine executed by the on-board MPU. With HP's 3060A, the test system can now supply this test routine to the MPU. No longer must S/A be designed into the board — unless you also plan to use S/A for field service testing.

Finally, S/A's stored go/no-go response approach is a cost-effective method for the testing of LSI devices.





You can put this new tool to work for you now.
Signature Analysis is part of the High Speed Digital Functional Test option to the proven HP 3060A Board Test System. This option is priced at $12,000* and can be added to 3060A's currently in service. The technique is complemented by the 3060A's programmable drivers, in-circuit program generator, and bed-of-nails visibility for automatic backtracing. Note, in the flow chart above, how the 3060A with this option provides flexibility in the selection of dynamic stimulus for board test applications.

For additional information.
To receive complete details on the HP 3060A Board Test System and the High Speed Digital Functional Test option, write: Hewlett-Packard, 1507 Page Mill Road, Palo Alto, CA 94304. Or call the HP regional office nearest you: East (201) 264-5000, West (213) 970-7500, Midwest (312) 255-9800, South (404) 955-1500, Canada (416) 678-9430.

*Domestic U.S.A. price only.

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Electronics

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Electronics

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Highlights

Cover: ICs read and speak, 117

The speech capability of integrated circuits and their associated software is growing to the extent that some of them are now vocalizing text. The first two articles of an ongoing series on speech synthesis discuss two examples of how that is accomplished. The first is a synthesizer chip that can speak any English word or text typed on the keyboard of its accompanying development system, with its software translating the keyed-in letters into basic word sounds (p. 118). The second is also a synthesizer chip; it is backed up by a library of 128 basic sounds and an algorithm for putting them together to speak messages appearing on a personal computer's display (p. 122).

The cover illustration is by Sean Daly.

Why some MOS memory makers are turning to epitaxy, 93

Are the benefits of building a dynamic random-access memory on an epitaxial layer—low noise, less leakage current, and operation at higher temperatures—worth the added cost of the layer? That is what is being debated by semiconductor firms that make MOS memories, following Texas Instruments' announcement that it is using epitaxy for its 64-K dynamic RAM. This Probing the News story considers the pros and cons.

Is Ada the last word in programming languages? 127

This special report presents a detailed portrait of Ada. Designed to meet the needs of the U. S. Department of Defense for a reliable, readable, and easily maintained high-level programming language, it may be so successful in meeting those goals that it will become, as its designer, Jean Ichbiah, believes, the last computer language. The key concept is software components, which would be standardized like hardware modules and joined by a common "bus."

Putting magnetic-bubble memories to work, 138

Bubble memories may be an appealing form of mass storage for computer systems, but the necessary control circuitry has been anything but attractive. So ways are emerging to help bubble devices realize their potential, and two are the subjects of separate articles. One is a controller chip that manages anything from a large memory system down to a single bubble device (p. 138). The other is a driver program that presents a bubble memory to an operating system—CP/M—in the guise of a disk, minimizing the application software changes for any system that now uses disks (p. 143).

And in the next issue . . .

The International Solid State Circuits Conference: a four-part article . . . next-generation microprocessors . . . a 16-K electrically erasable programmable read-only memory made using metal-nitride-oxide-semiconductor technology . . . applying signature analysis to a display terminal.

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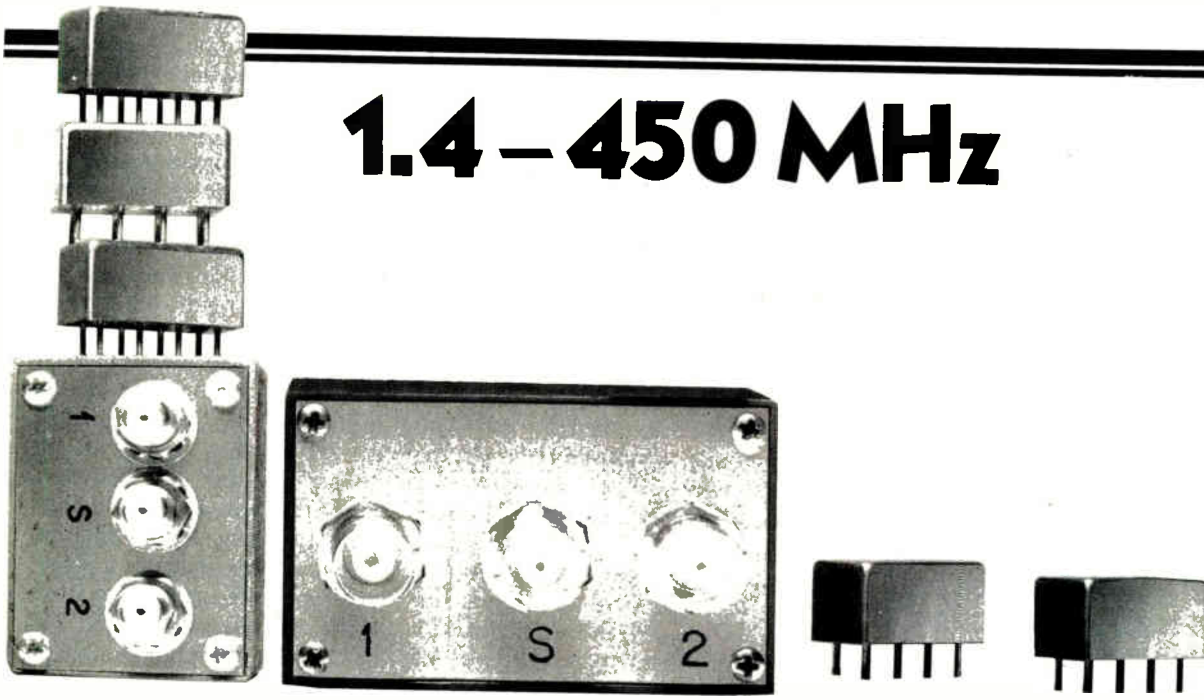

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Publisher's letter

Speech synthesis, the subject of the two articles featured on the cover, has only just begun to appear in consumer and industrial products. Work goes on to extend the capabilities of the various speech-producing systems, as these articles underscore.

The first, from the Votrax division of Federal Screw Works, Troy, Mich., describes a phoneme-based voice synthesizer chip that reads text (p. 118). It also goes into the development system that can be used to program the chip easily and simply. The second article, from Texas Instruments' Consumer group, Lubbuck, Texas, deals with a text-to-speech system that mixes linear predictive coding and phoneme-based techniques (p. 122).

The authors represent the kinds of people involved in speech synthesis. From Votrax there are Kathryn Fons, a speech scientist, and Tim Gargagliano, a computer and electrical engineer. At TI, Gene Frantz specializes in communications theory, Kun-Shan Lin in digital signal processing, and Kathy Goudie in linguistics. As Gargagliano, senior engineer in the research and development department, points out speech is a complex design problem requiring a multidisciplinary approach.

For Gene Frantz, manager of speech technology component design, TI's speech project, which began with the popular Speak & Spell, offered a chance to use his specialty, communications theory. "I started seven years ago designing calculators, but when the opportunity opened up with this new project, I grabbed it." Like the original speech synthesis development program, the work on the text-to-speech system described in the article was funded through TI's Ideas program, a plan for supporting projects proposed by employees.

The development of Ada goes back some six years when the Department of Defense recognized the need for a computer programming language that would serve all of its programming purposes. Later, by calling the language Ada instead of DOD-1, the department was aiming to set a standard for everyone.

Yet the DOD could not have foreseen Ada's immediate acceptance by industry. As the special report starting on page 127 points out, Ada's time has come. Prepared by microsystems and software editor Colin Johnson, the report describes the virtues of this universal language. "With Ada, the Defense Department was trying to specify a language more reliable, maintainable, and readable than any current language," he observes. "It borrows the best features from various languages, but mostly from Pascal."

According to Jean Ichbiah, who developed the language while at CII-Honeywell Bull in France, Ada will be the last computer language. The next step will have computers write programs to meet individual needs based on plain-language inputs.

"When that day comes," remarks Colin, "there will be no more programmers as we know them today. Everyone will be a programmer."

Wanted: an EE who wants to be an editor

We have a challenging position available for an electronics engineer who can combine writing ability and technical know-how into a rewarding career as an editor on *Electronics* magazine in New York. Candidates should have a BSEE and some linear design experience. We offer excellent salary and fringe benefits. If you are interested, send your résumé to Raymond P. Capece, Managing Editor, Technical, *Electronics*, 1221 Avenue of the Americas, New York, N. Y. 10020.

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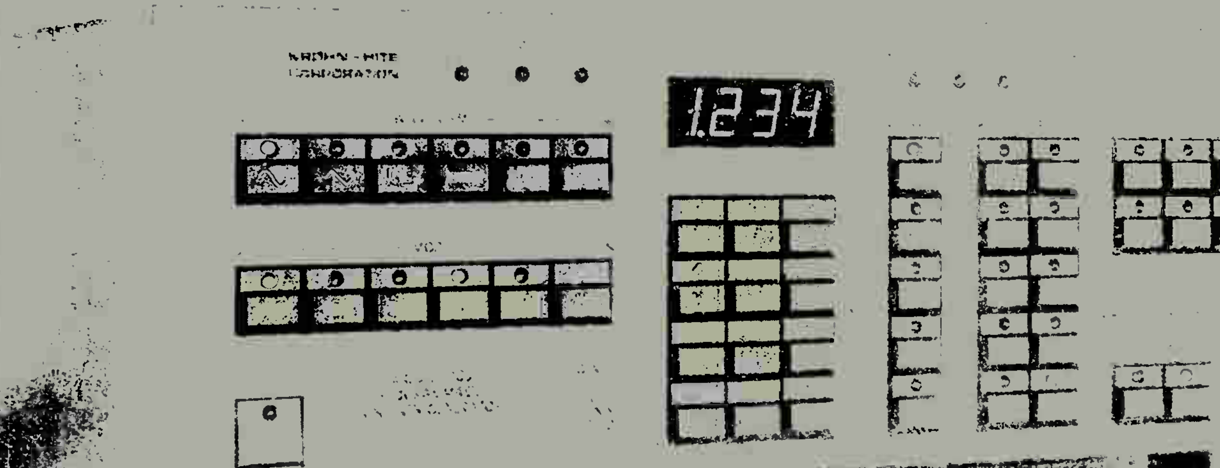

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Readers' comments

IEEE controversy: the full story

To the Editor: May I comment frankly on the Jan. 13 editorial [p. 24] in which you so aptly quote Juvenal's famous question, *Quis custodiet ipsos custodes?* The piece was written without a great deal of knowledge of what really goes on during and before board meetings, but that is not your fault. It is the job of us here at the Institute of Electrical and Electronics Engineers to inform you properly, and apparently we have failed. Let me try to make up for this failure.

I was out of the country when an announcement of the election results went out from IEEE headquarters. Upon my return 10 days later, I was immediately drawn into the controversy that had erupted around the referendum outcome. The last meeting of the 1980 board of directors was only about two weeks away, and one of the items on the prepared agenda was the tellers committee report. Before that board meeting I was almost constantly on the phone to the chairman of the tellers committee, to the general manager, to legal counsel, and to other interested parties, and I even insisted on a face-to-face meeting between the tellers committee and legal counsel in an effort to reconcile the opposing views. If we lacked legal sophistication, as you allege, it was not for want of trying.

The tellers committee report is usually noncontroversial, but anticipating a full-blown discussion, I made sure that all parties affected by the dispute were represented at the board meeting. In particular, the chairman of the tellers committee and the chairman of the credentials committee, as well as IEEE legal counsel, were invited and present during the entire discussion.

The board listened carefully to both sides and acted on legal advice. It made a decision not on the merits of the amendment but on the meaning of the vote. You are absolutely correct in stating that "it is unlikely that the IEEE board tried to slip its amendment past the membership by counting votes in a certain way." The board acted promptly and responsibly in this matter.

With 20-20 hindsight, I see two culprits. One is that the relevant bylaws, although approved by legal counsel years ago, were deficient with respect to this unusual situation; we are now working to clarify them. The other culprit is a practice that has been allowed to develop and has remained unchecked over the years, whereby the general manager and not the chairman of the tellers committee announces the election results. This practice is normally innocuous, but this year proved to be not in the best interests of the IEEE.

So what next? A petition has gone to the credentials committee, as reported in the same issue of *Electronics* [p. 332]. It would be inappropriate for me to comment at this time on what the credentials committee might recommend.

There are no villains in this drama. If there are any heroes, however, they are surely the members of the tellers committee who insisted on their rights and reasserted that the IEEE belongs to its members. The answer to Juvenal's question is *Ipsi custodes sunt.*

Leo Young, 1980 president
IEEE
Washington, D. C.

CML clarification

To the Editor: In response to your newsletter item "CII-Honeywell Bull to drop CML" [Jan. 13, p. 67], we would like to clarify our position on current-mode logic. CML technology is used in the new systems we will start shipping in 1981 and will also be used in systems that will be shipped after 1981. We see no limit, at this stage, to the use of this technology in any future generations of our products.

Michel Nico
CII-Honeywell Bull
Paris, France

Correction

On page 125 of the World Markets Forecast (Jan. 13), the source for the chart should have been given as Kessler Marketing Intelligence.

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News update

■ The 14-month-old international reallocation of radio frequencies has had little effect on communications services—so far. Not one piece of equipment has had to be shut down because of the decisions made at the 1979 World Administrative Radio Conference, say those who attended the WARC issues and impact meeting last month in New York.

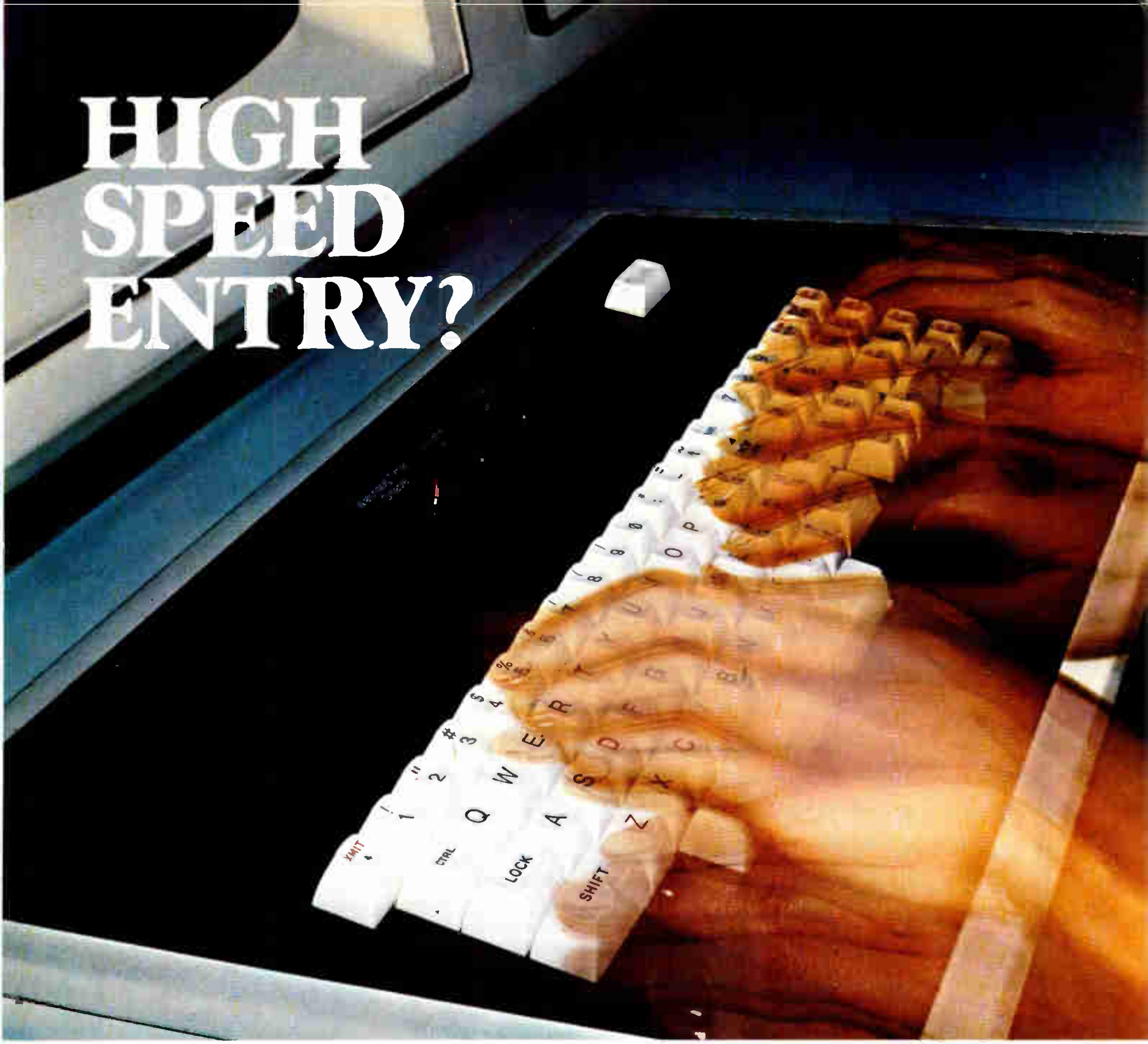
For example, the regulations for sharing the 2.5-to-2.65-gigahertz band between fixed-service and direct-broadcasting satellites have yet to be put into effect—the band has been reserved for the broadcasting birds. Also, the rules that were agreed upon have so many disclaimers and exceptions that no country has had to compromise any of its communications plans.

The main problem faced by WARC—the first held in 20 years—was the ever-increasing demand for a finite number of frequency allocations. The conferees avoided an anticipated impasse by deferring decisions on some critical bands [*Electronics*, Dec. 20, 1979, p. 76].

Conflict. One of the problems ahead concerns U. S. military communications in Western Europe. Department of Defense consultant Capt. Jack Weatherford, USN (ret.), explains that the transmission frequencies of U. S. military communications equipment are tailored to the allocations made within American territory.

But in Europe, some of these frequencies are assigned to civilian uses, and the geographic and spectrum congestion there only adds to the interference. Whenever possible, European communications authorities and U. S. forces there must cooperate closely, he says.

Conferees also noted that preparations must begin soon for the round of conferences on the deferred issues. Among them is a 1983 Western Hemisphere conference on the allocation of the 11.7-to-12.7-GHz satellite broadcast band. Also, 1984 and 1986 conferences are scheduled on international allocations for future satellites—the key issue that threatened to derail the 1979 WARC in Geneva. **-Harvey J. Hindin**



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People

Opdendyk sees opportunity for Personal Software's growth

New challenge. Terry Opdendyk brings his management skills to Personal Software.

No one abandons a high-level position at Intel Corp. without a good reason, and for Terry Opdendyk the reason was simply: "I was made an offer I couldn't refuse." The offer that he accepted late last year was to become president of Personal Software Inc. of Sunnyvale, Calif., a publisher of programming for personal computers.

"This is exactly the kind of opportunity that people had when they started Intel and National," he asserts. "It is the right time, and this is the right company."

If the projections hold up, Opdendyk, 33, may be a key figure in one of the decade's leading growth areas. Personal Software itself has grown over 200% yearly for the past two years, and company chairman Daniel Fylstra projects that the industry's current sales of about $90 million will exceed $1 billion per year by mid-decade. Fylstra, the former editor of Byte magazine, a monthly for users of small systems, chose Opdendyk because, "I needed someone with experience in managing a rapidly growing organization."

Opdendyk's career has been spent in high-growth areas. He joined Intel in 1973 when it was a mere $20 million-a-year company and saw it grow to close to $1 billion last year. After being manager of software for the Santa Clara, Calif., semiconductor maker's microcomputer operations, Opdendyk spent 1980 on the corporate staff as the manager of human resources.

Before joining Intel, he helped develop the first timeshared minicomputer at Hewlett-Packard Co. "I was on the tail end of the HP 2000 and the initial work on the HP 3000," he recalls.

Opdendyk plans to apply the lessons of Hewlett-Packard and Intel to the organization he is building at Personal Software. "At HP I learned the value of quality," he recalls, "and at Intel I learned the art of business management. All managers from the middle level up at Intel have to be business managers."

Managing a personal software house should tax Opdendyk's skills fully; because the nature of its business does not fit into any classic mold. Instead of mounting large research and development efforts in house, the company relies on some 50 independent software-writing companies, usually consisting of only two or three persons each.

The market served by such Personal Software products as VisiCalc also breaks the mold and is its reason for such dynamic growth. "In Personal Software's early days, the company focused on games," notes Opdendyk. "Now we are headed directly into the office automation field, and we expect that our products will change the way the white-collar workers do business."

Laconti sees big 1980s market for millimeter-waveguide gear

For Anthony Laconti, Thomson-CSF's attempt to penetrate the U. S. millimeter-waveguide components market is a golden opportunity. The French firm expects to gain a foothold in a business based on military and government sales—an area that will explode in the 1980s, according to his market studies. The fact that it is a long way from Paris to the U. S. does not bother him a bit.

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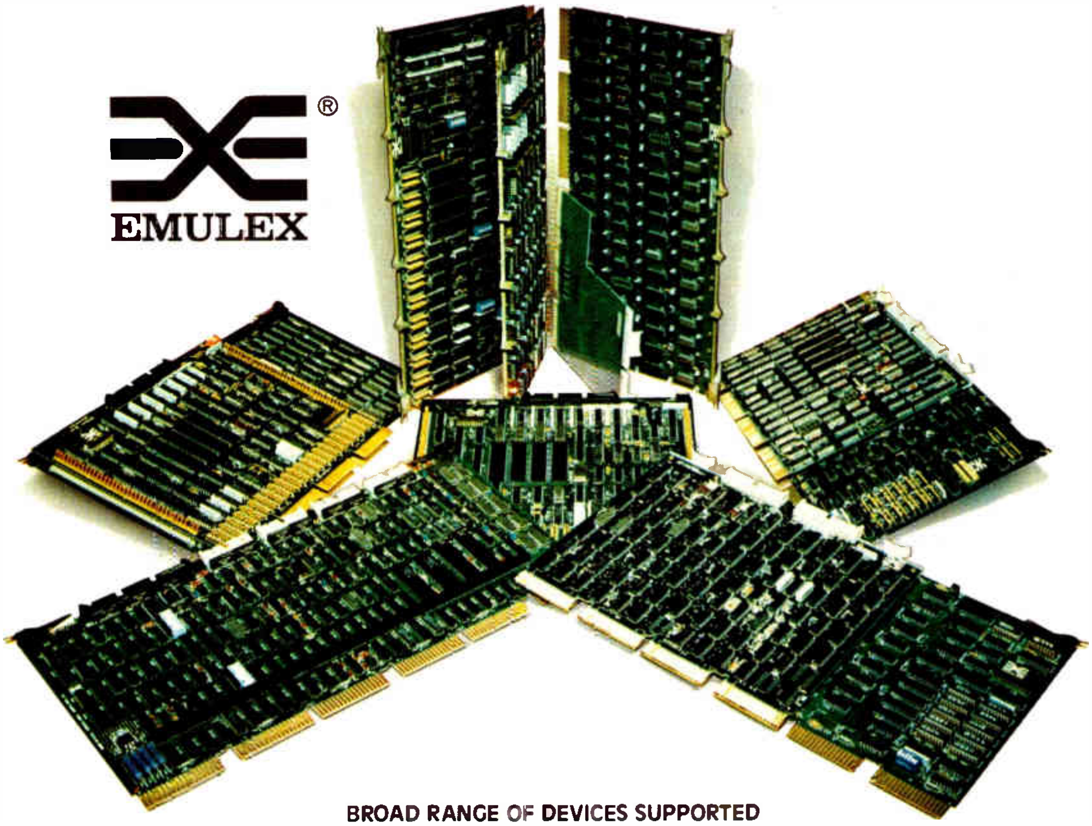

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Circle 15 on reader service card

People

Alpha are major factors in the standard waveguide market for millimeter technology," he says. "Our technology is as good or better and is based on years of sales in Europe. But, more importantly, we intend to beat them on price and delivery."

To handle the delivery problem, Laconti is setting up a distribution point in Clifton, N. J., where Thomson's Components division has its U. S. home and where he is sales manager for millimeter products and electron tubes.

"Some of the delivery times for millimeter-wave components from the other suppliers are six months to one year—a sure sign that there is a lot of business out there," Laconti says. To tap it, he is already writing a supplement to a new 40-page bilingual catalog while also working on data sheets for carcinotrons (voltage-tuned backward-wave oscillators). These millimeter-wave tubes can operate at up to 400 gigahertz with power to 50 milliwatts.

In addition to the need for standard line devices in the conventional millimeter-wave bands, the 51-year-old electrical engineer, a graduate of the University of Connecticut, predicts a lot of action in the 94-GHz band. Millimeter-wave transmission at this frequency requires the least amount of power because of an atmospheric "window" that minimizes attenuation.

Military role. "For the military, the resolution of millimeter waves is unsurpassed," Laconti says, because millimeter-wave radars and rangefinders have better specifications than anything at lower frequencies. Laconti concedes that the technology has been around for most of the years he has been in engineering and marketing and has never yet achieved practical application. But he insists that the military, who alone can afford to work with the expensive devices, will make them a reality in the 1980s. The reason, says Laconti, is that the improved generators, detectors, and components such as directional couplers, attenuators, and phase shifters now make the expense worthwhile. But, most important, there is a need for them. □

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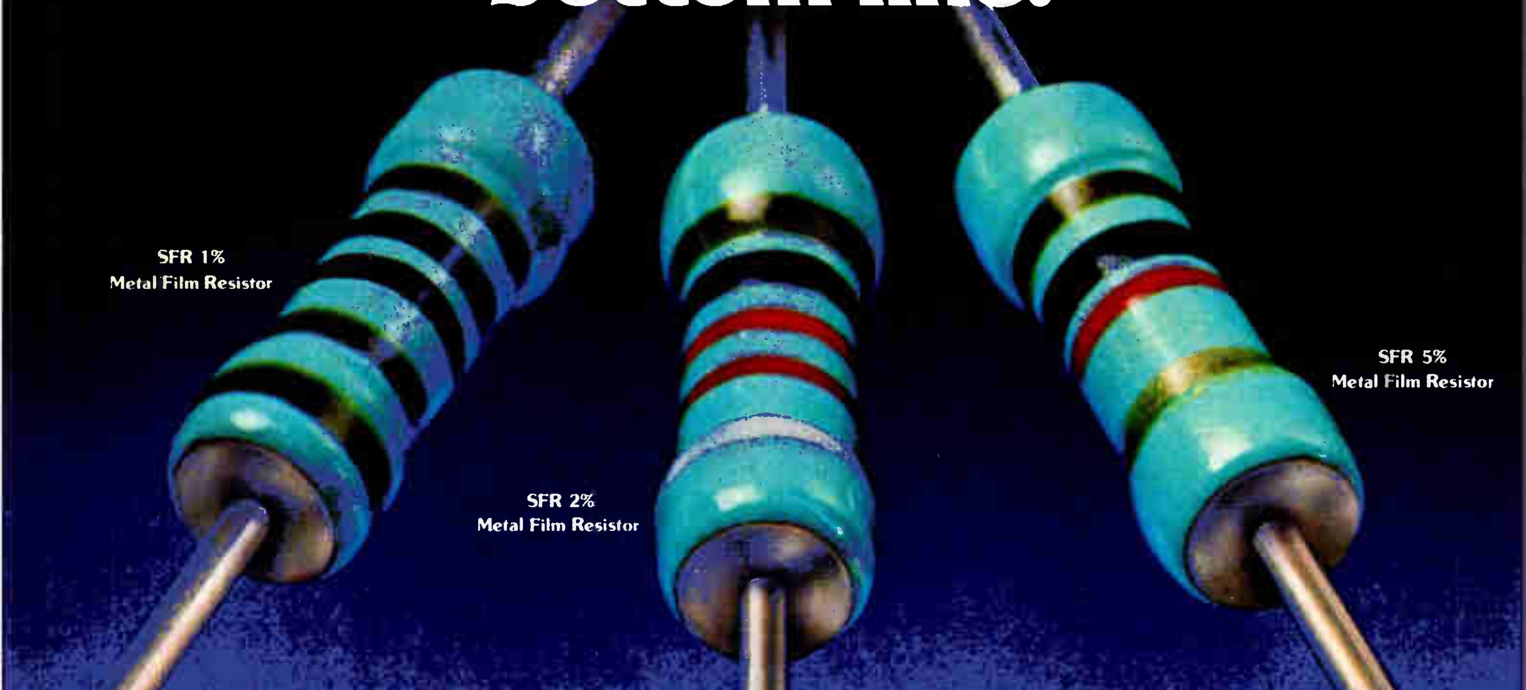

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Set your sites on Intel's new

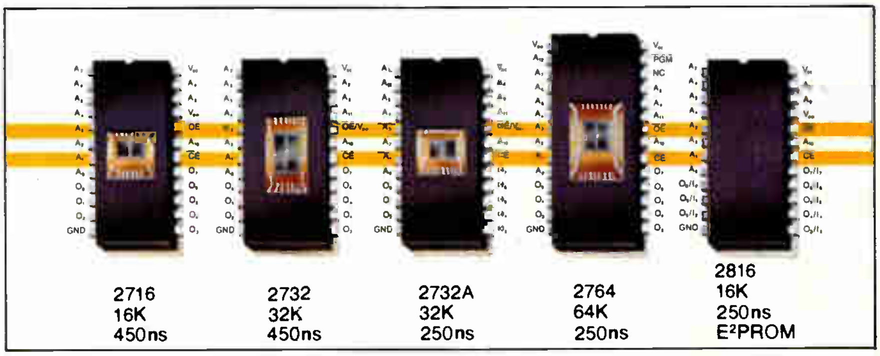
Introducing Intel's 2764 EPROM. The only 28-pin JEDEC-approved EPROM in volume production today.

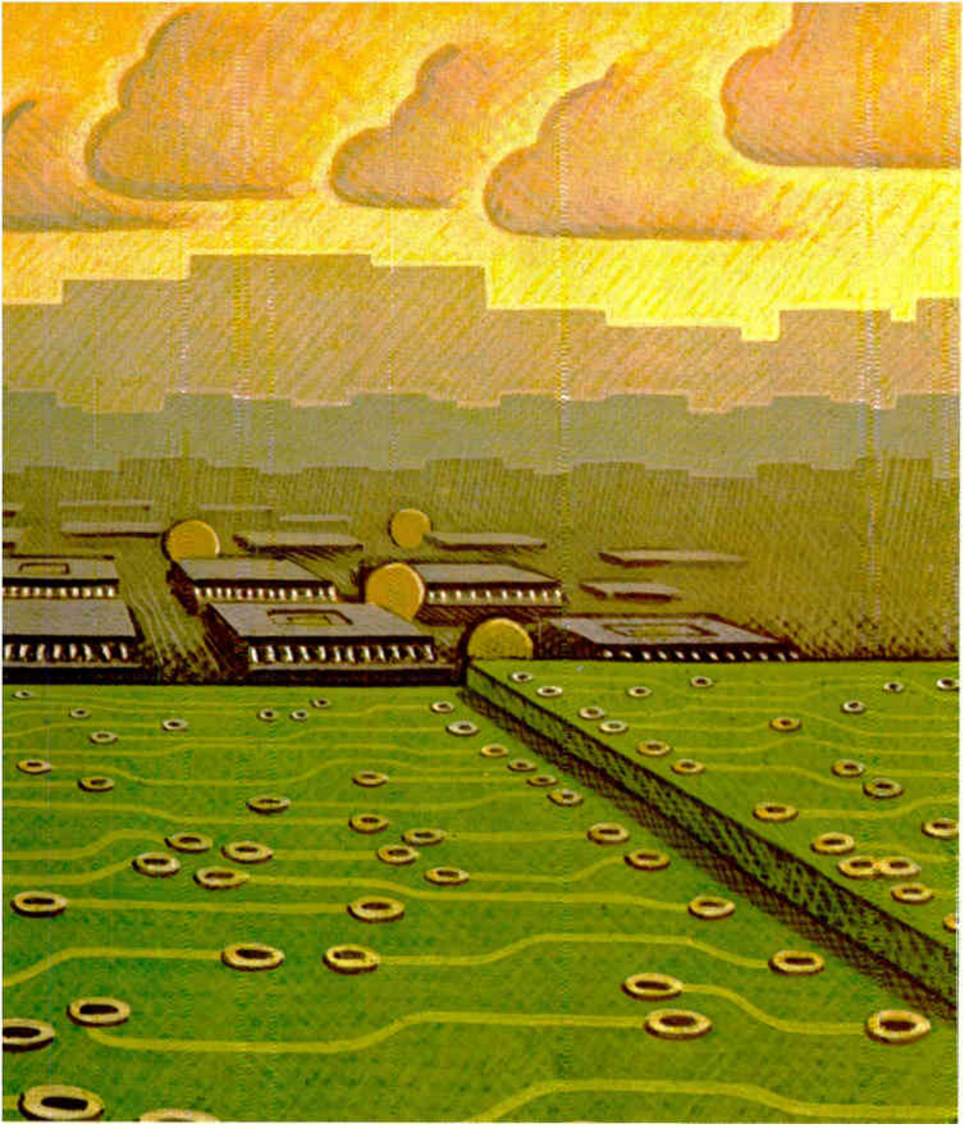
If you survey the field, you'll discover it's been hard to find high density and high speed in an EPROM. Until Intel introduced its new 2764—the one that has both. Plus Intel's complete family of EPROMs—including the 2764—allows you to get control of tomorrow's memory costs today.

The EPROM standard of tomorrow

Like its predecessor, the 2732A, our new 2764 is fabricated by Intel's proven fourth-generation EPROM technology, HMOS*-E. This technology allows us to shrink 2764 die sizes down dramatically, making this the smallest 64K EPROM chip in production. And HMOS-E makes possible the 2764's standard access time of 250ns. Which means you now have an alternative when you need high speeds and high densities—in applications such as controller systems for automated milling machines, vector color graphics displays, and over-the-horizon terrain radar.

In addition to high performance, the 2764 brings flexibility and cost control to your system designs. Like all of Intel's EPROMs, the





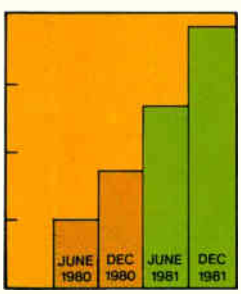
64K EPROM. Now.

2764's pinout conforms to the 28-pin JEDEC standard for Byte-Wide memories from 16K to 256K bytes. So when you design with 28-pin sites now, you can choose the EPROM that meets your needs today. Then upgrade your memory performance or density later — without any jumpers or expensive engineering changes.

Intel's universal EPROM solution

The 2764 represents the latest addition to our complete EPROM family — the only one that offers you a *universal* EPROM solution that begins with our industry standard 2716 and 2732 EPROMs.

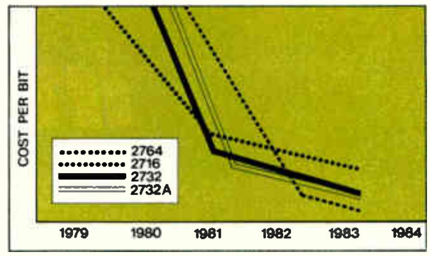
With this solution, your EPROM cost-per-bit will continue to drop. That means that by mid-1982, high-speed, high-density EPROMs will cost no more per bit than the EPROMs you presently buy. That also means that when it's right for you to upgrade, you'll save valuable board space *and* get increased performance — at no cost penalty.



Intel's EPROM Production Ramp-up

Getting all of the EPROMs you need will be easier, too. We'll more than triple our production capability by the end of 1981. Plus, more than ten ROM and EPROM manufacturers have already committed to the JEDEC Byte-Wide memory pinout standard, further increasing your design choices.

Our Byte-Wide memory family also includes the revolutionary 2816 E²PROM. It shares the identical pinout and 2K-byte data capacity as our 2716 EPROM. But the 2816's E² technology is the starting point for the next revolutionary step in non-volatile memories: in-system reprogrammability. Imagine the possibilities. Reconfigurable aircraft systems. Automatically adjusting machine tool controllers. Self-calibrating measurement equipment. Until the 2816, these designs have been impossible.



Cost-Per-Bit Decline for Intel EPROMs

Measuring the EPROM field

Only Intel offers you an EPROM solution with the widest range of speeds, densities, and performance. We back up this choice with the proven reliability that comes from HMOS technology and ten years of EPROM manufacturing experience. Plus we offer field support and technical documentation that leads the industry all the way.

For further information about Intel's EPROM family, including the new 2764 and 2816 E²PROM, contact your local Intel distributor or sales office. Ask for the "Intel EPROM Applications Manual." Or write directly to Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051. Telephone (408) 987-8080.

*HMOS is a patented Intel process.

Europe: Intel International, Brussels, Belgium. Japan: Intel Japan, Tokyo. United States and Canadian distributors: Alliance, Almac/Stroum, Arrow Electronics, Avnet Electronics, Component Specialties, Hamilton/Avnet, Hamilton/Electro Sales, Harvey, Industrial Components, Pioneer, L.A. Varah, Wyle Distribution Group, Zentronics.

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THE PRODUCER lets you spend less time programming and more time testing boards in production. That means you get your product to market faster and within budget.

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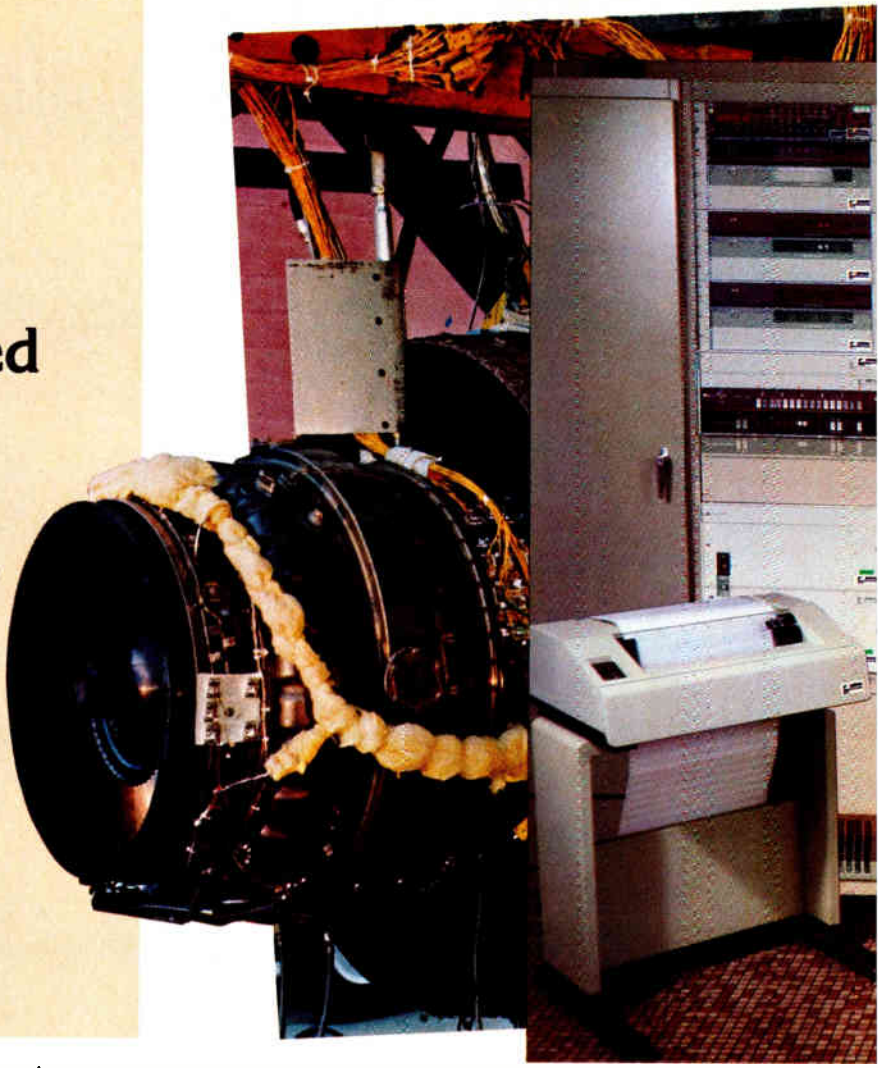
How HP-IB helped AVCO/Lycoming slash engine test time 50%...



AVCO's Lycoming Division, in Stratford, Connecticut, has long been known for the production of tough, dependable gas turbine engines for commercial aircraft and the military. Given the nature of its prime customers, this reliability must not only be designed in; it must be tested and proved at every stage of development. Thus, real time test data acquisition and analysis are critical to the company.

Edward Twarog, Lycoming's Manager of Electronics and Instrumentation, recommended the use of an HP-IB (Hewlett-Packard Interface Bus) system for developmental testing, because "this system is twice as fast as our previous data acquisition system, yet can be handled by a single engineer and one technician vs. the engineer and two technicians previously required. Just as important, the combination of HP 1000 computers and HP-IB instruments not only gives us the performance data we need; it gives it to us in engineering units that allow instant reaction, and, therefore, real time decision-making."

408 variables in 20 seconds.

Lycoming's HP-IB system is a closed-loop configuration. An HP 1000E is used to start the engine under test and operate it at various predetermined speeds. A total of 408 different variables can be monitored by HP instruments, which then feed this data back to the 1000 for data reduction and analysis. All told, these 408 variables — including pneumatic pressure, hydraulic pressure, temperature, speed, flow, position, vibration and torque/thrust — are acquired in 20 seconds.

"This system," Twarog reports, "not only gives us the accuracy we need but improves measurement sensitivity, and provides complete repeatability, since all engine and test parameters can be stored on tape or disc. This system will even give us an audible warning if something goes wrong with the test, or the test will be automatically shut down before any damage occurs."

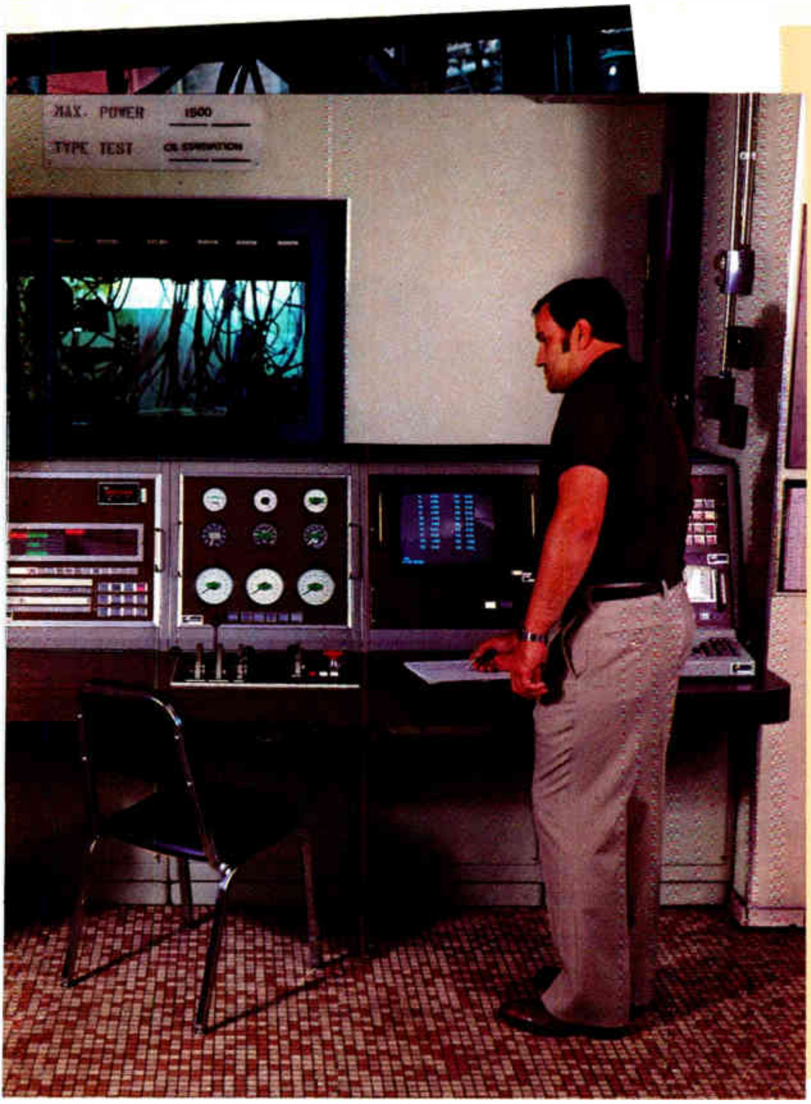
Serving many masters.

Twarog also reports that Lycoming's HP-IB system must be flexible enough to serve many engineers. In any given week, engineers from Lycoming's Design, Performance, Dynamics, Stress and Heat Transfer Groups may all be using the system working in any of AVCO's seven engine test cells on this distributed system. "We like the fact that a test engineer can perform his initialization on magnetic cassettes, load this data to the host HP 1000E, then download it to a satellite 1000E and suddenly, the system is doing exactly what he wants it to do — with no starting from scratch each time. This provides us with a very cost-effective solution to our needs."

One-stop shopping.

Lycoming chose the HP 1000Es to drive this automatic data acquisition system for two other important reasons. "We went to HP," Twarog explains, "because it's an instrumentation house. We felt they understood our needs and objectives better than any mainframe manufacturer. This also permitted us to enjoy 'one-stop shopping,' with a single manufacturer supplying both the computers and the test instruments.

"Second, in our case, we found the HP products just connected and worked. In addition to the two HP Satellite 1000Es and 1000E Host and two HP 5 Megabyte hard discs,



with no sacrifice in configuration flexibility or start-up time.

our data acquisition system also includes an HP 3455A Digital Voltmeter, three 3495A Multiplex Scanners, and two HP 2240A Measurement and Control Processors. HP-IB makes these instruments so easy to configure, we've just never had a problem."

What to look for in system design.

When you design and build instrument systems, make sure you get more than plug compatibility. HP, as a manufacturer of instruments and computers, offers you much more to help you achieve a working measurement solution in a minimum of time. That includes comprehensive documentation, training courses, applications information, systems engineering support, and on-site service.

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Editorial

Who's ready to pay for quality?

No doubt about it, quality is occupying center stage these days, especially in the semiconductor industry. In part because Japanese competition has raised the issue, U. S. companies are now motivated to set the record straight. But in reviewing quality-assurance programs, a couple of points emerge that have not received enough attention. For one, if quality has become a matter of direct concern to the top managers of semiconductor makers, are these concerns also granted the same high priority by the top management of their customers?

Yes, quality is akin to motherhood, but purchasing managers, who are highly motivated to cut prices, too often receive little or no backing to push for quality. In short, if quality pays—as the Japanese claim and most everyone else agrees—who is willing to pay the price?

Underlying this touchy equation is good, old-fashioned vendor-customer relations. Traditional barriers between buyer and seller involving secrecy about product plans and critical specifications often impede the open communication so important in quality programs. Some users, in fact, contribute to the U. S.'s quality problem in three ways. First, they do not make it a top priority; second, they fail to recognize that quality is a performance specification worth paying for; and third, they hinder smooth solutions to quality problems.

The quality circles touted by the Japanese have gained considerable notice and some backing in the U. S. [*Electronics*, Dec. 4, p. 95]. Important as this concept has become, however, little has been said about the Japanese firms' unique vendor-customer relationships. The fact is that often both parties belong to larger, vertically organized companies, and the spirit of cooperation between buyer and seller within a company spills over to outside dealings.

Semiconductor companies may well ask their customers, to paraphrase a famous line of a previous decade, "Are you part of the problem or part of the solution?"

Those daring young men in their flying machines

In what seems to be a new entrepreneurial wave, Silicon Valley is making 1981 the year of the startup. At last count, 12 new semiconductor makers have sprouted in the fertile soil south of San Francisco, and there is no reason to believe that we have seen the end of the wave. In fact, now that the venture capital pipeline is once again unclogged, what we are seeing is probably just the beginning.

There is a basic difference, however, between the new companies of the 1980s and those, now the well-established chip manufacturers, that mushroomed in the first great technology wave some 15 years ago. Then they were broad-based producers seemingly intent on becoming No. 1 in every aspect of the industry. Now they are companies that have set out to fill a special niche in the semiconductor product spectrum. For example, one is a manufacturer of arrays, another has set itself up as a silicon foundry.

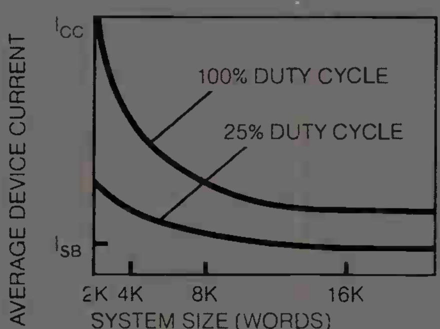
Still, a set of constants links the two generations of innovators. Companies that seek to exploit new technologies are still one of the best means of providing new jobs, keeping cash moving through the economy, and ensuring a steadily improving life for the population at large.

Still using bipolar PROMs? Catch on to the Fast Cat™ ROM. It purrs when it has to.

Keep your eye on this one — the SY3316A Fast Cat™ ROM from Synertek. Because we're adding features to this cat that translate into significant cost saving benefits for you.

The latest is automatic power down. At 20mA standby, the SY3316A puts the clamps on heat build-up. And as system size grows, power consumption slows. Dramatically.

And it's fast — 80nsec. It all combines to make the SY3316A the perfect solution wherever high performance, large bit storage and low power are important design considerations. Not to mention cost.

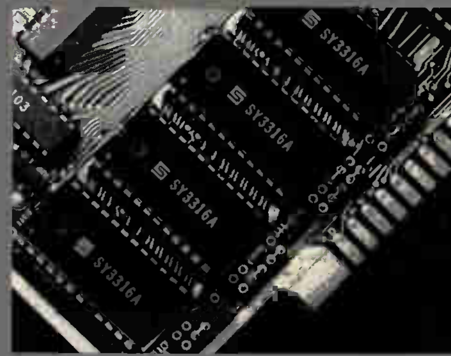


Now you can make a quick, cost-effective move from bipolar PROM prototyping right into volume production — without costly PC board redesign. The SY3316A can do it because it's directly pin compatible with 16K bipolar PROMs.

There's even more. Like a single +5V power supply, full input/output TTL compatibility, fully static circuitry, asynchronous operation, 2048x8 organization, two mask programmable chip selects and three-state outputs to facilitate system expansion.

Using 8K bipolar PROMs? Then set your sights on the SY3308 8K ROM, another fast number — at 70nsec — in the Fast Cat™ ROM family. And it's fully compatible with 1Kx8 bipolar PROMs.

Our family of Fast Cat™ ROMs is getting bigger. And better. When you consider the alternative — expensive bipolar PROMs — the logical way to go is with the SY3316 Fast Cat™ ROM. From Synertek, the company that built its name in ROMs. Call your area Synertek representative now.



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Meetings

Fourth Electromagnetic Compatibility Symposium and Technical Exhibition, Institute for Communications Technology (Tomas Dvorak, The Federal Institute of Technology, CH-8092 Zurich, Switzerland), Federal Institute of Technology, March 10–12.

Semicon/Europa '81 and Second SEMI European Symposium on Materials and Processing, Semiconductor Equipment and Materials Institute Inc. (625 Ellis St., Suite 212, Mountain View, Calif. 94043), Züspa Convention Center, Zurich, Switzerland, March 10–12.

Sixth Annual Spring Financial Conference, American Electronics Association (2600 El Camino Real, Palo Alto, Calif. 94306), Del Monte Hyatt House, Monterey, Calif., March 11–13.

Monaco Financial Conference, American Electronics Association (2600 El Camino Real, Palo Alto, Calif. 94306), Loews Monte-Carlo Hotel, Monte Carlo, Monaco, March 15–18.

Leipzig International Spring Fair, Leipziger Messeamt (P.O. Box 720, DDR-701 Leipzig, East Germany), Leipzig Fairgrounds, March 15–21.

SCTE Spring Engineering Conference, Society of Cable Television Engineers Inc. (1900 L St. N. W., Suite 614, Washington, D. C. 20036), Opryland Hotel, Nashville, Tenn., March 16–17.

LSI Technology Conference: Circuit Design, Systems and Applications, Verband Deutscher Elektrotechniker (6000 Frankfurt 70, Stresemannallee, West Germany), Congress Hall, Baden-Baden, West Germany, March 16–18.

14th Annual Simulation Symposium, IEEE, Association for Computing Machinery, *et al.*, Holiday Inn Resort, Tampa, Fla., March 16–20.

Third Annual Microelectronics Measurement Technology Seminar, Benwill Publishing Corp. (1050 Commonwealth Ave., Boston, Mass. 02215), San Jose Hyatt, San Jose, Calif., March 17–18.

28th International Electronics, Nuclear, and Aerospace Exhibition with conferences on computer communications and energy from space, RIENA (9 Via Cresenzio, Rome, Italy), Palazzo dei Congressi, EUR, Rome, March 20–29.

1981 Office Automation Conference, American Federation of Information Processing Societies (P. O. Box 9659, 1815 N. Lynn St., Arlington, Va. 22209), Albert Thomas Convention Center, Houston, March 23–25.

Automatic Testing Conference and Exhibition, Network GmbH (3050 Wunsdorf 2, Steinhunde, An der Friedenseiche 10, West Germany), Rhein-Main Hall, Wiesbaden, West Germany, March 23–26.

Fifth International Conference on Digital Satellite Communications, IEEE, Intelsat, and Telespazio SpA, Fairgrounds Conference Building, Genoa, Italy, March 23–26.

Digital Communications Techniques Seminar, IEEE and Princeton University Department of Electrical Engineering, Princeton University, Princeton, N. J., March 24.

FOC 81 East—International Fiber Optics and Communications Exposition, Information Gatekeepers Inc. (167 Corey Rd., Suite 111, Brookline, Mass. 02146), Hyatt Regency, Boston, March 24–26.

High-Temperature Electronics Conference, IEEE Solid State Circuits Society, Department of Energy, and University of Arizona, Ramada Inn, Tucson, March 25–27.

Seminars

Manufacturing Management: The Japanese Formula, American Electronics Association (2600 El Camino Real, Palo Alto, Calif. 94306), Hyatt Rickey's Palo Alto, March 6.

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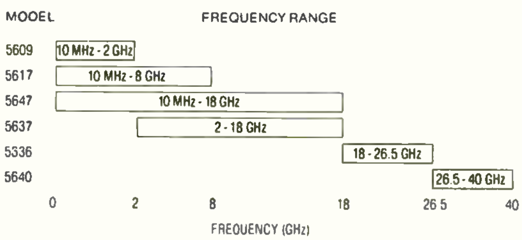
Each system consists of the Model 560 Scalar Network Analyzer, a 6600 Series Programmable Sweep Generator and the Model 85 Controller. Connect the SWR Autotester and Detector supplied, plug-in the factory preprogrammed cartridge and the system is ready to go.

40 dB Directivity

Wiltron's 5600 Series offers 40 dB directivity over a 10 MHz to 18 GHz continuous sweep range. Dynamic range is 66 dB with −50 dBM sensitivity. The system offers 82 dB programmable attenuation in 0.1 dB steps. ROM-corrected frequencies are accurate to ±10 MHz from 10 MHz to 18 GHz. Six models span the 10 MHz to 40 GHz range.



A key part of the system is the new Series 6600 Programmable Sweep Generator. This sweeper uses fundamental oscillators to avoid substantial errors generated by the harmonic products of multiplier type oscillators. The result, broadband coverage with the lowest harmonic content (−40 dBc, 2-18.6 GHz), low residual FM and greater stability.

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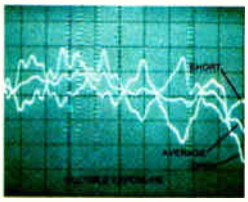
Simply plug-in the preprogrammed cartridge and enter a few simple inputs.

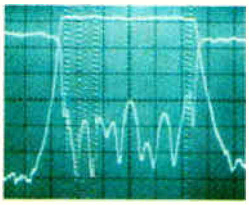
It's as Simple as A, B, C, D, E, F!

A. System Setup
Enter 1) Date.
2) Type of measurement to be made.

B. Frequency Selection
Enter 1) Frequency range limits.
2) Frequency step size or number of test points.

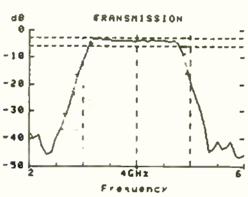


C. Calibration
Enter 1) DUT identification.
Select 1) Averaging of open/short residuals.
2) Storing of normalized residuals.



D. CRT display of DUT characteristics
1) Select marker frequencies and amplitude limits.
2) If necessary, adjust DUT.
3) If not, continue.

E. Measurement
1) Press key to start automatic measurement sequence.



F. Hard-copy output
Select 1) Plotted curves.
2) Tabular data.

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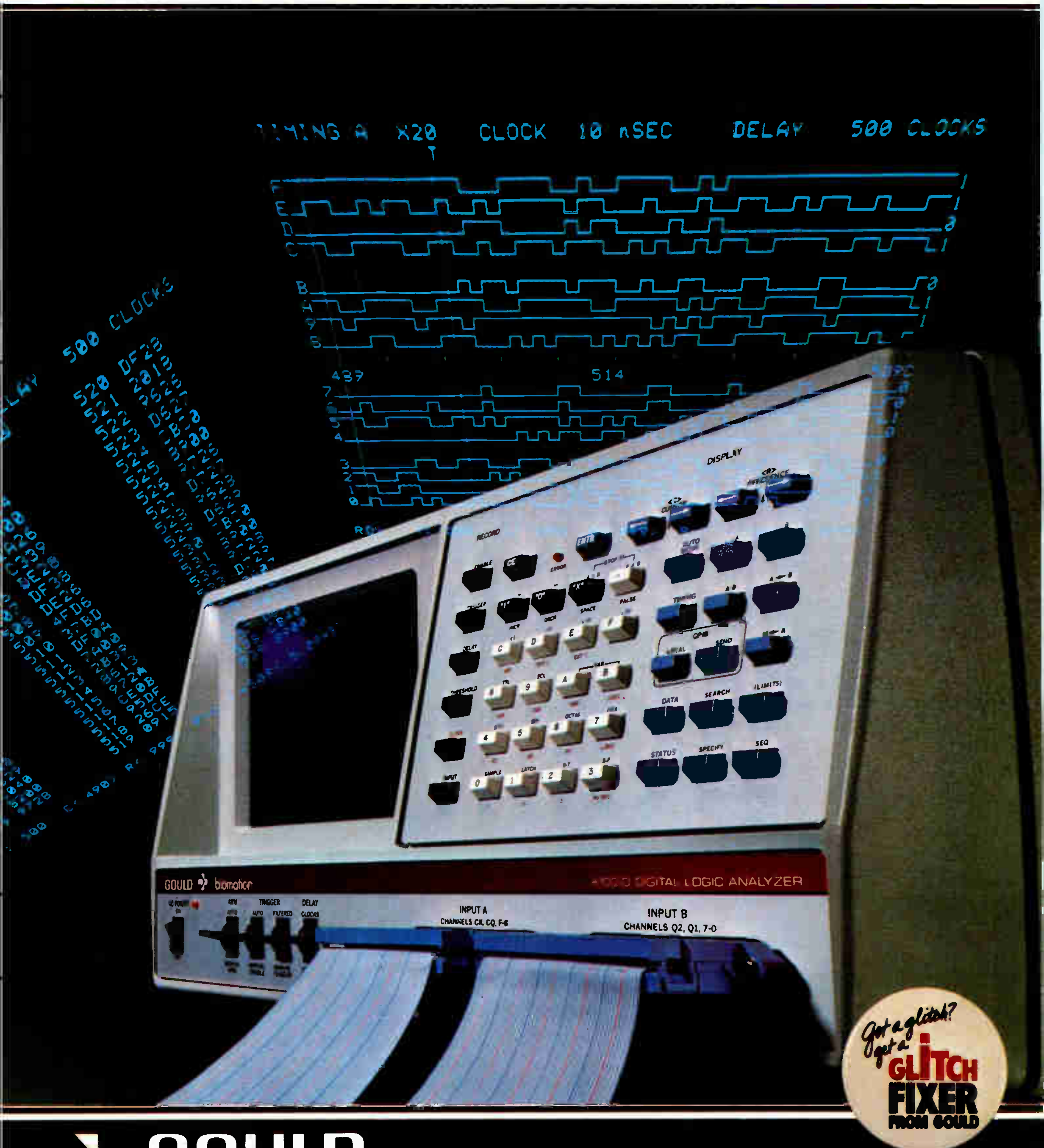

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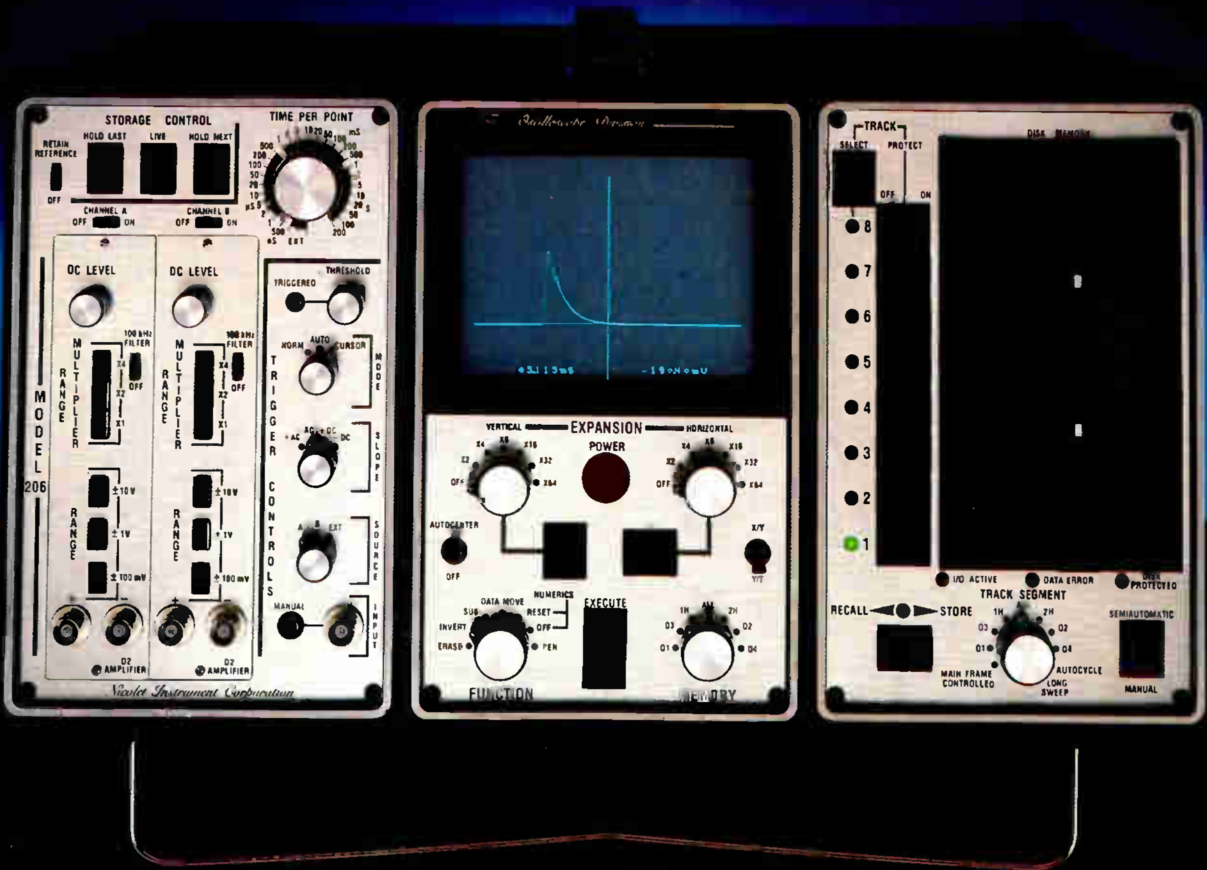

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Electronics newsletter

Fluke readies microsystem analyzer

With company president John W. Zevenbergen saying he expects them to be "our biggest dollar volume product ever," John Fluke Manufacturing Co. of Mountlake Terrace, Wash., has quietly been showing models in its 9000 series to several dozen favored customers. Dubbed the Microsystem Troubleshooter, **the service-oriented series performs signature analysis, triggers scopes, determines logic states with a separate probe, and counts transitions.** Moreover, the initial, under-$4,000 instrument contains sophisticated canned software routines with which it can learn the contents of an undocumented printed-circuit board, including determining the locations of random-access and read-only memories and input/output ports. Although the family, which contains IEEE-488 interface and Philips minicassette options, is not to be introduced until June, more than 80% of the customers shown samples have said they will buy the unit.

Zilog to offer Z8000-based development unit

Look for Zilog Inc. of Cupertino, Calif., to introduce a new development system later this month. Based on the company's Z8001 16-bit microprocessor, the Z-Lab 8000 will accommodate up to 16 users. In keeping with Zilog's commitment to Bell Laboratories' Unix operating system, the Z-Lab 8000 will operate under Zeus, a superset of Unix version 7 that is targeted to the Z8000 instruction set. **It can contain up to 1.5 megabytes of random-access memory in 256-K-byte increments, as well as up to four 8-in. Winchester disk drives handling 24 megabytes each, and a 17-megabyte tape cassette drive.** In addition to the C language in which Unix is written, it will also support Zilog's other languages, but the first units, to be delivered in November, will add only Pascal.

Production equipment makers are warned of economic jolt

There's a 50% chance that the U. S. will experience a severe slump in the first half of 1981, causing capital spending to lag and creating a ripple effect in the semiconductor-manufacturing equipment market. For the second year in a row, New York economist A. Gary Shilling has warned members of the Semiconductor Equipment Manufacturers Institute (SEMI), who were meeting in Newport Beach, Calif., last week, to prepare for a slowdown. **This one will be much worse than the one that stifled the economy last year, he adds.** Though operating in a high-technology growth market will help the semiconductor-equipment producers weather the worst effects, an overall decline in capital spending of 3% to 5% in 1981 will cut into growth rates and profits, according to Shilling.

32-bit supermini called most powerful

What may be the most powerful 32-bit superminicomputer yet announced is due this spring from Systems Engineering Laboratories Inc. of Fort Lauderdale, Fla., a Gould Inc. subsidiary. Code-named Thunderbird during development, the Concept 32/87 is termed a "third-generation supermini" by insiders. Oriented to real-time and science applications, the multiple-bus multiprocessor uses 64-bit-wide data paths and is said to perform more than 4 million operations per second. **That puts it in a league with IBM's 3033 and makes it two to four times faster than any supermini competitor.** Built with emitter-coupled logic, the 32/87 cycles in 75 ns and uses a four-stage, parallel-pipelined processor. Though about three times faster than the company's former best, the 32/7780, the new computer's software and peripheral equipment are compatible with existing products.

Electronics newsletter

Image processor to help automate IC houses, users

A general-purpose, programmable wafer- and chip-inspection system should emerge soon from Contrex Inc., Burlington, Mass. Based on high-speed, digital image analysis, **the automatic inspection and control system aims at markets like incoming inspection**—for example, at manufacturers of hybrid integrated circuits, especially those with automatic assembly facilities—where the system would rapidly spot such defects as chips and cracks in IC dice, physical contamination, damaged metalization, and dice delivered face down in their waffle packs. Tailored systems already are being built for two major semiconductor houses and delivery of general-purpose versions may be as little as four months away. A typical chip-inspection system would cost about $80,000 and pay for itself in less than a year, Contrex says.

Sharp gain in 5-in. wafer starts predicted

Some 20 million in.^{2} of silicon wafers—equivalent to 1 million wafer starts—will be produced worldwide in 5-in. form during 1981, according to market analyst Daniel Rose, head of Rose Associates, Los Altos, Calif. In 1980, he estimates, just 2 million in.^{2}, or 100,000 5-in. wafer starts, were made. **Though 3-in. wafers are still way ahead, Rose sees production leveling.** In 1980, there were 142 million in.^{2} produced, but he predicts a decline to 126 million in.^{2} this year and then a slight gain to 128 million in.^{2} in 1982.

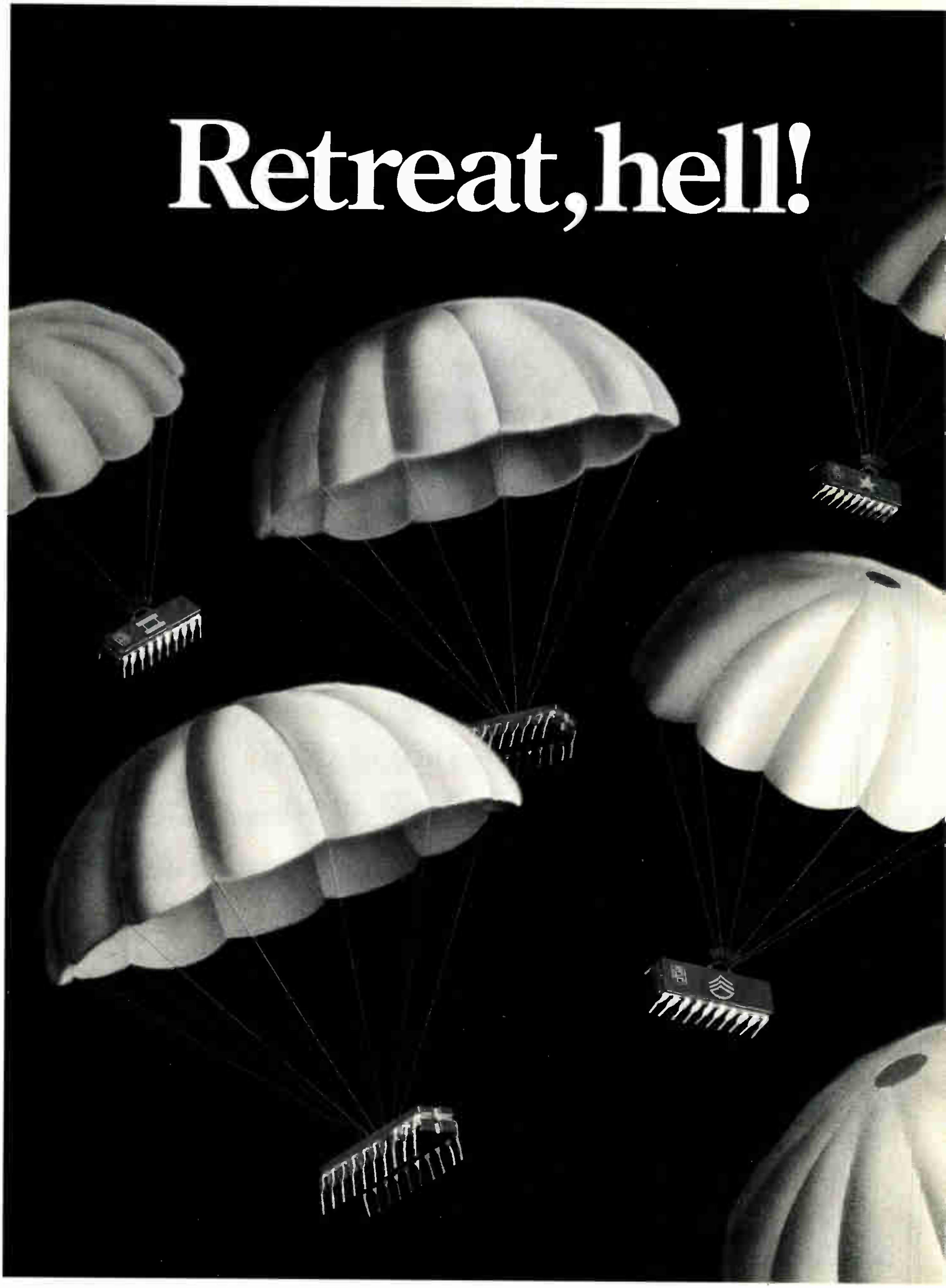
Intel plans 4-Mb bubbles

Now that support components are becoming available for 1-Mb magnetic bubble-memory devices, the manufacturers are starting to drop hints about their 4-Mb chips. One of them, Intel Corp.'s Intel Magnetics Inc. of Santa Clara, Calif., **expects to have working 4-Mb memories and an accompanying kit of components by the middle of next year.** Though it once believed that contiguous-disk technology would be ready for the 4-Mb level, the firm is going to stick with conventional Permalloy processing and field coils. The company says it can stuff 3 million bits more onto a chip about the same size as its 4-cm^2 1-Mb device [*Electronics*, April 26, 1979, p. 105]. Its access time may also be close to the 1-Mb device's, but the data rate will be about four times higher, indicating that four 1-Mb chips may be scaled down and combined onto one die. The 4-Mb chip's package will also keep the same number of pins, but possibly defined differently.

Meanwhile, later this year Intel Magnetics will offer a removable bubble cartridge, and so will National Semiconductor Corp., also of Santa Clara. National will disclose data about its 4-Mb bubble memory at the Intermag conference, to be held this summer in Grenoble, France.

Burroughs text writer challenges IBM machine

Taking on IBM, Burroughs Corp. is coming out with a low-priced, stand-alone word processor. The RIII system 315 text writer will compete with IBM's Displaywriter, as well as with Wang Laboratories' Wangwriter and Sony's series 35 [*Electronics*, Jan. 13, p. 46]. The Burroughs machine, available now with a 55-character/second printer at $8,395, including software, will be available July 1 with a 35-c/s printer for $7,795. It is a desktop model featuring a half-page display and a single floppy disk. The 315 is being marketed by Burroughs' new Office Systems group, **the first step by the Detroit company to integrate recently acquired Systems Development Corp. into the parent company.**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Circle 38 on reader service card

Over a million devices make up 32-bit CPU and support chips

by Bruce LeBoss, Senior Editor

1.5-μm n-MOS process, two levels of tungsten, build 5-chip set suited for desktop computer

A glimmer of the achievements possible with very large-scale integration can be seen at Hewlett-Packard Co.'s Desktop Computer division, where engineers are fabricating a 32-bit processor chip with a new high-density, high-speed n-channel MOS process. With 450,000 transistors and an 18-megahertz clock rate, the central processing unit is part of a set of integrated circuits that is likely to be the heart of an advanced desktop computer.

To fabricate the CPU and support ICs, the Fort Collins, Colo., division has implemented a silicon-gate n-MOS process with a minimum size of 1.5 micrometers for line widths and 1 μm for spaces. The support chips are an input/output processor, a memory controller, a 128-K random-access memory, and a 528-K read-only memory with over 600,000 devices so that it can include parity bits.

Fabrication. The eight-mask process, called N-MOS 3, resembles other n-MOS structures for VLSI. Self-alignment is used for ion implants and for interconnections to save area and to trim speed-limiting parasitic capacitances. As the figure shows, two levels of pure tungsten metalization for signal and power busing also contribute to a compact layout and high speed.

To further increase packing density, HP is able, through careful processing, to make contact with the polysilicon gates by placing the first layer of metal directly over transistor channel regions. This is in contrast to other processes, where metal-to-polysilicon vias are placed away from active regions so they do not damage delicate areas such as thin gate oxides.

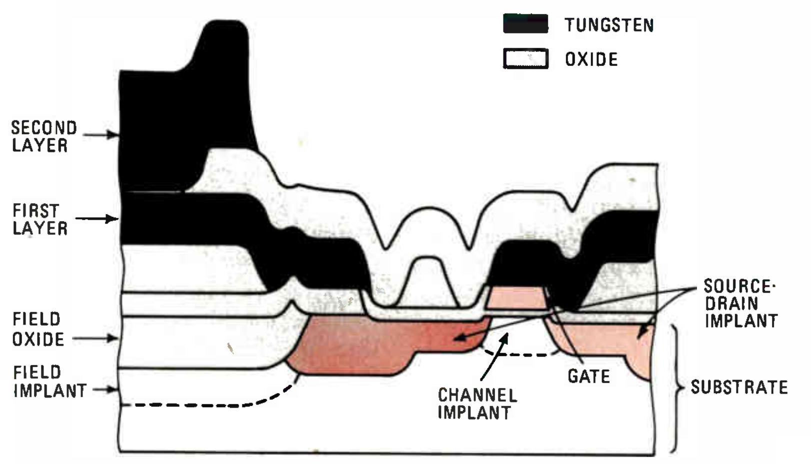
HP engineers are laying down the patterns with optical projection, using a GCA 4800 wafer-stepping lithography system and dry-etching technology in both tungsten layers. They developed low-pressure chemical vapor deposition to produce the second metal level, thereby providing low-resistance interconnections.

Devices are constructed on a high-resistivity substrate that minimizes the substrate-bias effect on threshold voltage. A field oxide fully recessed into the substrate allows minimum spacing between diffusions. This recessing technique also improves surface planarity.

The CPU contains 32-bit data paths and 9,000 38-bit words of microprogrammed control store that implement an extensive 32-bit instruction set. It has a sequencing stack with a set of 13-bit registers that fetch the microinstructions.

PLA decoding. These instructions are decoded by the chip's programmable logic array, which drives the appropriate control lines to perform specified operations. Most of the operations are executed in three clock cycles.

Special logic on the CPU performs a 32-by-32-bit multiplication in 1.8 microseconds and a 64-by-32-bit division in 3.5 μs. Much of the high speed comes from pipelining instructions, overlapping three of them so



Fast MOS. Double-level tungsten metalization and a fully recessed field oxide are among the steps in HP's new n-channel MOS process for high-density, high-speed integrated circuits.

that the net execution rate of sequential microinstructions is one per clock cycle (55 nanoseconds) instead of per three clock cycles.

An HP spokesman says the N-MOS 3 technology looks promising but disclaims any plans to use it or the CPU chip. One possibility for the process and the chip set, however, is HP's planned Vision family of 32-bit computers [*Electronics*, Oct. 23, 1980, p. 35]. The division is to be responsible for the low end members of that line.

Test equipment

ATE makers mounting software push to help users generate test programs

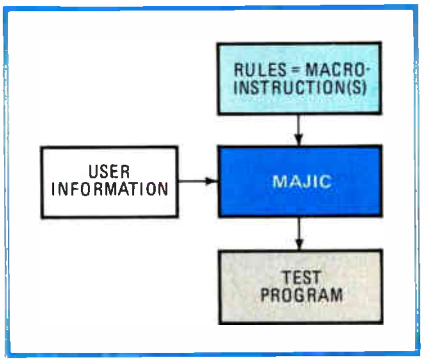
The automated test equipment industry is starting to make it easier for its customers to generate test programs. Macroinstructions written in high-level languages, menu-driven program-generation modules, and programs that can handle analog test procedures are among the software options now becoming available from ATE companies.

For example, the Majic test language developed by Computer Automation Inc. for its board testers includes a set of macroinstructions for automatically generating low-level code in a test program. Users can also write new macroinstructions and link the data base created by their computer-aided design system to that of the logic simulation program and to the tester.

Macros. The language also is flexible enough to let users write program statements that resemble English sentences in their structure. Thus the user statement "Ripple 1 to the left on the data bus" is read by the program as "Ripple data bus."

The "ripple" is a macroinstruction used to generate an entire sequence of input vectors that will ripple a 1 or a 0 through a field of complementary data bus lines. Such macros will in turn generate several lines of lower-level object code that the programmer previously had to generate one at a time.

"This can reduce the time involved in working out a new test program by a factor of 10," says Douglas Cutsforth, vice president and general manager of Computer Automation's Industrial Products division in Irvine, Calif. Majic will run on the recently introduced Sprint test system [*Electronics*, Jan. 13, p. 276] and on the company's Capable series of board testers.



ATE aid. Computer Automation has designed its Majic test language to act as a compiler, translating high-level-language inputs into test programs.

Even more impressive are the menu-driven programs developed by Eaton Corp. and by Plantronics/Zehntel Inc. for systems introduced at the Philadelphia test conference [*Electronics*, Nov. 6, p. 89]. Eaton calls the software for its integrated-circuit tester the Interactive On-line Program Generator. Its board tester is served by the Interactive Program Generator.

"The menus are much easier," asserts Ron Thomas, manager of technical marketing for the IC tester line at Eaton's Semiconductor Equipment operations in Woodland Hills, Calif. "Before, an engineer would pass a design to maybe four people before he saw a working test program. Now he can do it himself—or even have a secretary fill in the information."

The type of information requested by the programs includes the number of pins, the size of the device, and functions and labels for each pin. In the dc portion, voltages and clock states are requested, as well as expected output values. In the ac portion, the user specifies the timing exercises required and voltage groups in the patterns.

"We also allow the user to run what he has at each step of the program creation process," Thomas notes. "That way, he can see if he likes what he is creating as he goes along." The Eaton program also lets the user call up macros.

At Plantronics/Zehntel in Walnut Creek, Calif., its Producer software also uses a menu-driven approach. Like the Eaton packages, the key element is a binder module that links the user-supplied information with program modules.

The board-oriented software also executes network analysis routines on an element-by-element basis. In automating important testing tasks, the software performs the analog calculations necessary to derive parameters for circuitry up to three levels away from the point of test in order to determine where ground guards should be placed and which paths will conduct stray current.

Each of these three systems uses approaches that will become virtually mandatory on this decade's test systems. The link to simulation programs demonstrated by Computer Automation, the menu-driven programs of the Eaton systems, and the analog network calculations of the Plantronics/Zehntel system all help streamline the software for writing test programs. **-Martin Marshall**

Memories

Game plan at Intel includes multiplexing

In an ambitious effort to maintain its role as pacesetter in solid-state memories, Intel Corp. is lifting the veil part way on its blueprint for chips organized into bytes and wider. The Santa Clara, Calif., company plans a multiplexed 28-pin package to accommodate at least 4-megabit densities and so will remain a viable pinout for 20 years or more.

Redundancy bits and Intel's aborning high-performance complementary-MOS (C-H-MOS) process also will play roles in static and pseudostatic random-access memories and programmable read-only memories, both ultraviolet-light and electrically erasable. All will come in two packages, with multiplexed or nonmultiplexed buses.

Family trees. The master plan involves introducing a myriad of different memory parts in both n-channel MOS and C-MOS and in both packages. In effect, there will be a number of family trees like the one shown below outlining the development of pseudostatic RAMs over the next few years. The company will describe its first pseudostatic part, a 32-K multiplexed memory, at next week's International Solid State Circuits Conference in New York and will introduce an 8-K-by-8-bit nonmultiplexed part by year's end.

Intel's nonmultiplexed 28-pin configuration, intended primarily for byte-wide data, has already been accepted as a standard by the JC-42 subcommittee of the Joint Electron Device Council. The multiplexed package, however, is a new idea—but it, too, has been presented to the JC-42 committee and is supported by a later proposal from memory maker Mostek Corp. [*Electronics*, Dec. 18, p. 36].

Existing multiplexed memories include Intel's peripheral parts for its 8085 microprocessor and similar chips from National Semiconductor for its C-MOS NSC800 8-bit microprocessor. Motorola, too, recently introduced a multiplexed C-MOS 16-K ROM [*Electronics*, Sept. 25, p. 127].

But Intel's game plan for multiplexed chips extends to 9- and 16-bit-wide organizations. Accommodating 9-bit data will yield byte-wide data with parity, and a bus 2 bytes wide will give direct compatibility with the latest microprocessors. The multiplexed package will have 16 address and data lines, giving 256-K locations that, together with a 16-bit-wide bus, will permit a memory capacity of 4 megabits.

All parts will be built with Intel's H-MOS, or high-performance n-MOS, process with scale-downs for high speed in the cards. For lower power consumption, chips like the static RAMs will also use C-H-MOS.

Redundancy is getting increasing attention for high-density solid-state memories because of the dramatic improvements it promises for yield [*Electronics*, Dec. 4, p. 108]. Intel was not the first memory maker to embrace the idea, but it has done so enthusiastically—"All of these [planned] chips will have redundancy," says Kirk F. MacKenzie, strategic marketing manager for Intel's Memory Components division in Aloha, Ore. **-John G. Posa**

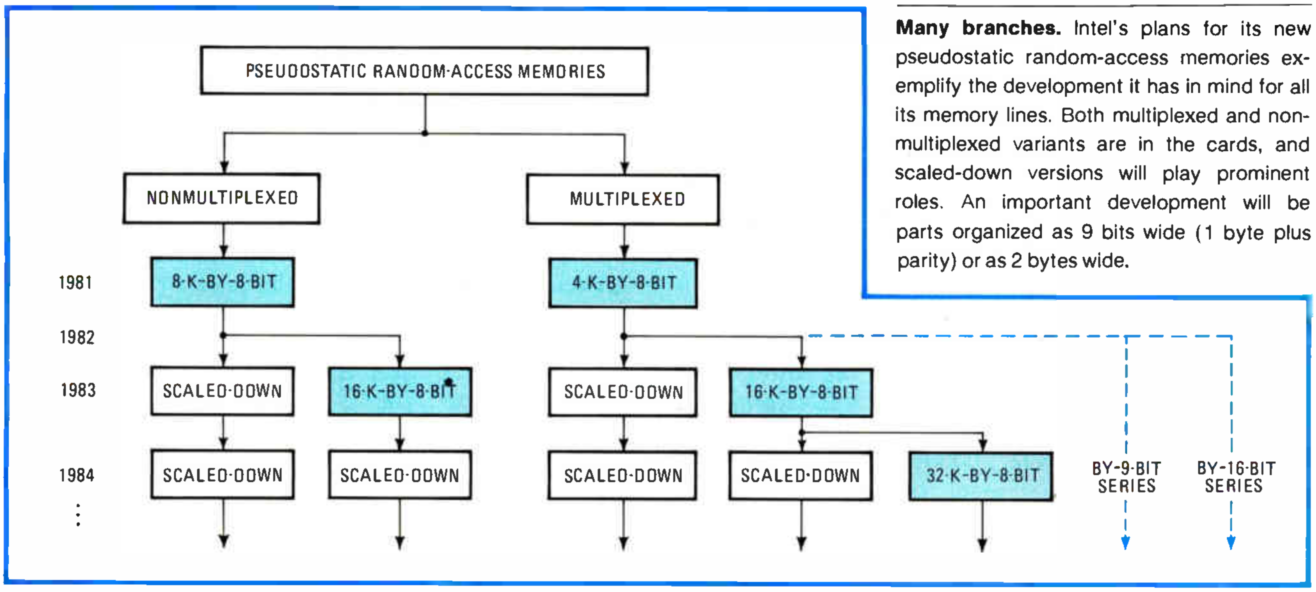
Communications

Add-on converts PBX for data, voice net

A new voice- and data-handling private branch exchange from Rolm Corp. is a forerunner of PBX systems that one day will handle electronic mail, store-and-forward voice switching, and other office-of-the-future tasks. It is a simple solution to the local-network question.

The voice- and data-handling capability is an add-on feature to the 12-year-old Santa Clara, Calif., company's CBX line of private branch exchanges that were originally designed to handle voice traffic within a user's complex. To get both voice and data on a local network, the user has had to add hardware and software to an existing system.

But when the data-communications feature is added to the all-digital CBX system, both voice and asynchronous data can be transmitted over standard telephone twisted-pair wiring. All that is needed, says company vice president of engineer-



Many branches. Intel's plans for its new pseudostatic random-access memories exemplify the development it has in mind for all its memory lines. Both multiplexed and nonmultiplexed variants are in the cards, and scaled-down versions will play prominent roles. An important development will be parts organized as 9 bits wide (1 byte plus parity) or as 2 bytes wide.

Modemless. Rolm's data-communications add-on to its digital private-branch exchange uses an data terminal interface unit (shown), a data-line interface at the controller, and a TDM control card for modem-free, on-site voice and data transmission.

ing James M. Kasson, are a data-communications software package, a special interface unit at each terminal to be hooked into the system, and interface cards plugged into the CBX controller.

As automated systems with computers, terminals, and word processors begin to fill offices and factories, the question of how to interconnect them in local networks has become increasingly important. Other ways of approaching that question include AT&T's much-discussed Advanced Communications Service, which uses the in-place telephone network; Xerox's coaxial-cable-based Ethernet; and IBM's Systems Network Architecture.

Underneath. Rolm's data terminal interface (DTI) is a desktop module shown in the photograph that sits under a phone and transmits asynchronous data at rates of from 110 to 19,200 bits/second. It can do this chore at distances of up to 5,000 feet from the CBX controller. Each DTI has a standard RS-232-C interface and may be used to originate or answer a data call. According to Kasson, it may "connect to almost any asynchronous terminal, computer port, modem, or multiplexer port" by emulating a full duplex standard Bell 102/212 line-signaling protocol to the equipment connected.

A data-line interface is mounted in the CBX controller cabinet. These two printed-circuit boards support up to 16 separate data channels, with each operating at its own data rate. They handle interface and control functions for full duplex data communications to the controller's time-division-multiplex bus.

The TDM bus needs a third board, called the time-division-multiplexing control card. It prepares the system for what the company refers to as data submultiplexing; this scheme allows data channels to be set up using fundamental voice channels. With the basic voice system, a voice connection is assigned two time slots for the duration of a call. Each of these slots can carry up to 192,000 b/s, far more than a typical data connection needs.

Rolm uses the new software and hardware in the CBX communication package to break up a pair of time slots into parts that can accommodate as many as 40 data connections at 2,400 b/s. Thus, either high-quality voice or data can be maintained and used as network requirements change. **-Harvey J. Hindin**

Business systems

Distributed system takes on IBM's 8100

As if to emphasize its commitment to office automation, the Electronics Office Systems Group of Northern Telecom Inc. is introducing a new model for its family of distributed-data-processing systems with twice the power of the previous top-of-the-line offering. The model 585 is one of a series of business-oriented introductions slated for this year from the group, the former Northern Telecom Systems Corp.

The new DDP system competes with IBM Corp.'s 8100 series, though it maintains compatibility with the Minneapolis group's smaller systems. Other competitors in this performance range include the mid-range systems from Datapoint Corp., the Hewlett-Packard Co.'s 3000 series, and Texas Instruments Inc.'s 990 series.

Stacking up. Though all these systems have similar capabilities, NTI claims better price-performance figures, especially with configurations of 7 to 11 terminals. A typical model 585 system with 11 megabytes of disk storage, 15 megabytes of tape storage, a 256-K main memory, four terminals, and a letter-quality printer will cost $46,900 and will be available by May.

The model 585 in its 7-to-11-terminal configuration does offer higher throughput at a lower price than a similarly configured IBM 8130. At its maximum of 16 terminals, however, the 585's system performance is about equal to that of the 8130 and other similarly configured competitive systems.

Based on an 8085 microprocessor, NTI's new system is one of the first of its type to offer mass storage on an 8-inch Winchester-technology disk drive with integrated backup on tape cartridges. The company decided to build its own disk and tape drives because no single source had both available at the time it was developing the 585—a situation it feared might compromise reliability.

The group's engineers chose the 8-in. format for its low cost per byte, market acceptance, and expansion capabilities. The disk drive comes with 11- or 22-megabyte capacities, and the tape cartridge drive can store 15 megabytes.

The disk uses a microprocessor-controlled embedded-servo positioner for the read/write head, with the track-reference information for the servo mechanism stored between sectors of data on both surfaces of the platter. This approach leaves more room for data, since it eliminates the need for an entire platter surface for storing the positioning information.

The 585 and related announcements indicate that the group is back

A few of our customers say Abbott MIL Spec power supplies are 99% perfect.

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on the track of product development needed to remain competitive. Formed when Canadian-controlled NTI bought the former Sycor and Data 100 computer companies, the group had difficulties integrating these acquisitions.

But the assimilation appears to have taken place. The group recently announced word-processing software and new printers for its systems [*Electronics*, Dec. 18, p. 45], following these with the 585.

Next will come software allowing NTI's remote batch terminals to use its DDP capabilities. Also planned are hardware and software enhancements to the DDP line and a system integrating voice and data capabilities in one terminal. -Tom Manuel

Packaging

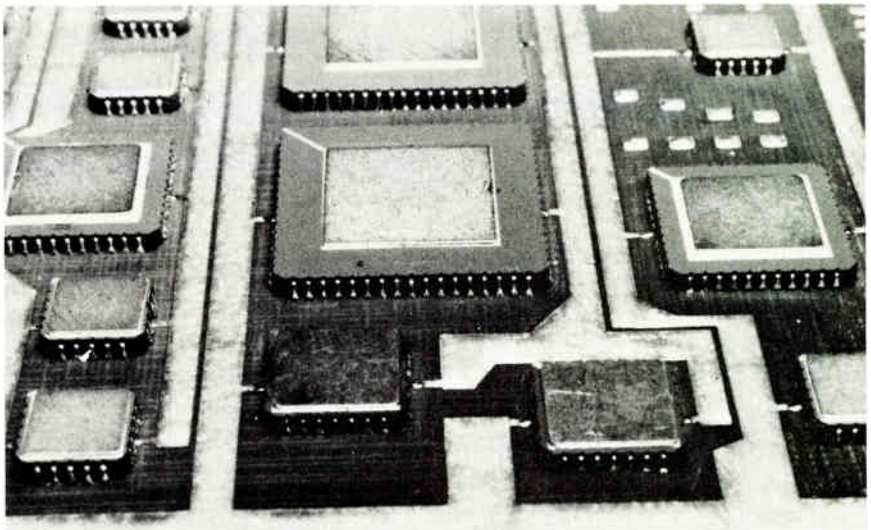
Multiwire's maker eyes metal-backed board for thermal match to leadless chip-carriers

Another investigation is under way of metal-backed circuit boards to which ceramic leadless chip-carriers can be directly soldered—potentially a convenient means of packaging very large-scale integrated circuits. Researchers at the PCK Technology division of Kollmorgen Corp. are developing a metal-backed board that will use a variant of the firm's Multiwire discrete wiring technique.

Structurally, the Melville, N. Y., division's board will resemble the Lampac printed-circuit board under development at Bell Laboratories in Denver [*Electronics*, Jan. 13, p. 48]. The key to both is the metal support, which matches the thermal coefficient of expansion of the chip-carriers' alumina much more closely than does the epoxy glass of the typical circuit board.

Charles L. Lassen, product manager of advanced interconnection technology at PCK Technology, reports excellent test results for a board that uses a 30-mil-thick nickel-iron support for an epoxy-glass sandwich. Chip carriers of many sizes were reflow-soldered on top of the sandwich, which had encapsulated wiring as the filling between its two 5-mil-thick layers. The board survived 400 thermal shock cycles over the military temperature range of $-65°$ to $125°$ without a single failure to its 692 solder joints.

The test used six boards of four substrate materials: the Alloy 42 nickel-iron material, steel, Kevlar



Partners. Solder joints between leadless chip carriers and a circuit board with a nickel-iron support survived 400 thermal shock cycles over the $-65°$-to-$+125°$C temperature range.

plastic, and standard epoxy glass. All the boards used etched copper interconnecting pads and identical complements of reflow-soldered chip-carrier packages (see photograph). But they varied in structure.

The epoxy-glass and Kevlar boards used typical printed-circuit interconnections, and one sample each of the steel and Alloy 42 metal boards used a thin epoxy-glass overlay layer with typical pc interconnects, much like Lampac. The other two metal boards had adhesive-encapsulated wiring (which PCK Technology is calling Microwire) sandwiched between epoxy-glass layers, with the top 5-mil-thick layer having copper footprints for the leadless chip-carriers.

At the Nepcon West conference in Anaheim, Calif., later this month, Lassen will report that, as expected, the joints on the epoxy-glass board failed first and most often, with 300 open joints after 400 cycles. The steel pc board, however, had 150 open joints, and the steel Microwire board had only 50 open joints.

No failures. Lassen says no joints failed on the two Alloy 42 boards or on the Kevlar board. However, the plastic costs \$7.50 a square foot (compared to \$4.60 for Alloy 42, \$2.30 for epoxy glass, and 70¢ for steel). It also has a thermal conductivity little better than epoxy glass and 67 times worse than Alloy 42.

Even though Alloy 42 costs twice as much as epoxy glass, PCK Technology prefers it to the much cheaper steel because of the higher thermal reliability of its solder bonds. The Lampac board from Bell Labs uses a steel support plane, but a copper-clad nickel-iron alloy is under consideration for high-performance applications.

Bell Labs has done some testing over a more limited temperature range with small chip-carriers and plans a 1,000-cycle test over the military temperature range with all sizes of packages. The bigger chip-carriers have high pinout counts, which makes them useful for VLSI chips but also makes them more prone to joint failure.

Both Microwire and Lampac are

High current transistors in TO-3.

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	V_{CEO} (V)	$V_{CE\ (sat)}$ typ. (V)	$t_{fall\ (typ)}$ (µs)	I_C/I_B		V_{CEO} (V)	$V_{CE\ (sat)}$ typ. (V)	$t_{fall\ (typ)}$ (µs)	@ I_C/I_B
BUR 50	125	0.8	0.1	70/7	BUX 10	125	0.7	0.15	20/2
BUR 51	200	0.9	0.24	50/5	BUX 11	200	0.6	0.24	12/1.5
BUR 52	250	0.7	0.2	40/4	BUX 12	250	0.5	0.23	10/1.25
BUR 20	125	1.15	0.12	50/5	BUX 40	125	0.6	0.14	10/1
BUR 21	200	0.7	0.2	25/3	BUX 41	200	0.6	0.25	8/1
BUR 22	250	0.5	0.18	20/2.5	BUX 42	250	0.45	0.2	6/0.75
BUX 20	125	0.55	0.1	50/5					
BUX 21	200	0.4	0.18	25/5	BDY 57	80	0.5	0.15	10/1
BUX 22	250	0.32	0.17	20/2.5	BDY 58	125			

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in the early developmental phases. An important incentive is the increased packaging density they offer—Microwire's planar interconnections are the equivalent of four layers of a multilayer board, and Lampac's two-sided interconnection board is equivalent to eight layers. Since leadless chip-carriers themselves greatly improve board densities [*Electronics*, July 3, 1980, p. 45], combining them with metal-backed boards may be the answer to packaging complex VLSI chips as compactly and simply as possible. **-Jerry Lyman**

Software

Financial model runs on desktop units

Making sophisticated financial modeling a routine task on desktop computers is the goal of a fledgling Van Nuys, Calif., software firm. C4P Inc.'s Financial Planning Language program requires only 64-K bytes of memory in a microprocessor-based computer, compared with the 80-K bytes or more needed on mainframes to run such programs as Capex Corp.'s popular Autotab II.

Although FPL may not have all the resources of the mainframe programs, its attractive price should appeal broadly to new users. A single-user license costs $695, whereas Autotab II is licensed for $21,000 or leased for $950 a month. Also, most buyers of the mainframe models use a timesharing service for their computing power.

Thus C4P and its marketing house, Lifeboat Associates, New York, think that financial analysts, bankers and stockbrokers, corporate planners, and the like, will welcome FPL, especially if they already own desktop computers that use the CP/M operating system. With the modeling language, they will be able to tackle a wide range of jobs like profit-and-loss forecasting, cash-flow management, commercial loan evaluation, acquisition and merger analysis, product-line planning, material and labor requirements, and real-estate development analysis.

Like Autotab II, FPL is written in Basic; in fact, it uses the same syn-

Money management. A variety of financial planning tasks are possible with the FPL modeling software designed to run on desktop computers rather than on mainframes.

News briefs

Sears plans computer stores

Sears, Roebuck & Co. has joined the growing list of companies hoping to capitalize on the business machines market with freestanding retail specialty stores. The giant Chicago-based retailer plans to open five test stores this fall in three unspecified cities in the East, Midwest, and South that will sell electronic equipment under Sears and other brand names. Computers, typewriters, word processors, printers, copiers, calculators, and dictating machines will be offered. Other firms that have opened similar retail outlets include Xerox, IBM, Tandy, and Control Data.

Thin-film disk-drive heads in the spotlight at CDC

Control Data Corp., Minneapolis, entered the market for very large disk drives late last month. The new CDC 38800 drives use thin-film heads to store 2.52 billion bytes per unit at a transfer rate of 3 million bytes per second—more than twice the speed of the CDC 33502. With the companion disk controller, these drives are IBM-compatible and match the basic specifications of the IBM 3880. They are priced at $66,000 to $120,000, whereas the IBM 3380 model A was announced with prices ranging from $97,650 to $142,200 [*Electronics*, June 19, 1980, p. 35]. First deliveries of the 38800 are scheduled for the second quarter of 1982.

Also last month, CDC and Memorex Corp. of Santa Clara, Calif. announced a technology-transfer agreement covering thin-film heads. The pact includes an exchange of information of the two companies' prototype head-arm assemblies and some peripheral circuitry but not the disks. Both firms are major IBM competitors in the disk-drive marketplace, but the agreement may be as much directed against potential Japanese competition as against IBM.

Southcon exhibitors call Atlanta show a success

Though its prospects as a first-time show were uncertain, last month's Southcon was generally considered a hit among the 284 exhibitors who occupied 482 booths at Atlanta's World Convention Center. Attendance totaled almost 12,000. Next year the show moves to Orlando, Fla., at the Orange County Convention Center, Jan. 19–21.

Boom year behind, TI sees troubles ahead

Sales crossed the $4 billion mark at Texas Instruments Inc. last year, but top TI officials warn that the industry may be in a steeper 1981 slump than predicted earlier. Net sales in 1980 rose 26% for the Dallas firm—$4.07 billion, compared with $3.22 billion in 1979. The company lists 1980 net income at $212.2 million, or $9.22 per share, up from $172.9 million, or $7.58 per share. Despite TI's performance, chairman Mark Shepherd Jr. and president J. Fred Bucy see a difficult first half for 1981. The company quotes them as saying: "Despite the fourth quarter 1980 growth in the U. S. economy, continuation of the recovery is doubtful in view of the persistent inflation and the monetary discipline necessary to curb it."

RCA's chief bows out

In a surprising move, Edgar H. Griffiths, resigned as chairman and chief executive officer of RCA Corp. late last month. Thornton F. Bradshaw, 63, president of Atlantic Richfield Co. and an RCA director, will assume the chairmanship July 1, when the resignation becomes effective. Griffiths will continue as a consultant to RCA and a director, and will become the chairman of the finance committee.

tax. Dennis Brown, C4P's president and FPL's author, boasts it has the same capability as Autotab, a point disputed by the houses offering mainframe-based financial modeling on a timeshared basis.

For example, Capex cites Autotab II's unlimited matrix size, whereas FPL's matrix has been limited to 2,000 cells. But, Brown says, "I find

NO. 21

NATIONAL ANTHEM®

SEMICONDUCTOR NEWS FROM THE PRACTICAL WIZARDS OF SILICON VALLEY.

New COPS™ microcontrollers double their memory capacity.

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P^2CMOS unveiled

New filter for digital switching systems

New μP-compatible clocks

The family approach to display drivers

Microcomputers correct themselves

Low pressure absolute transducers

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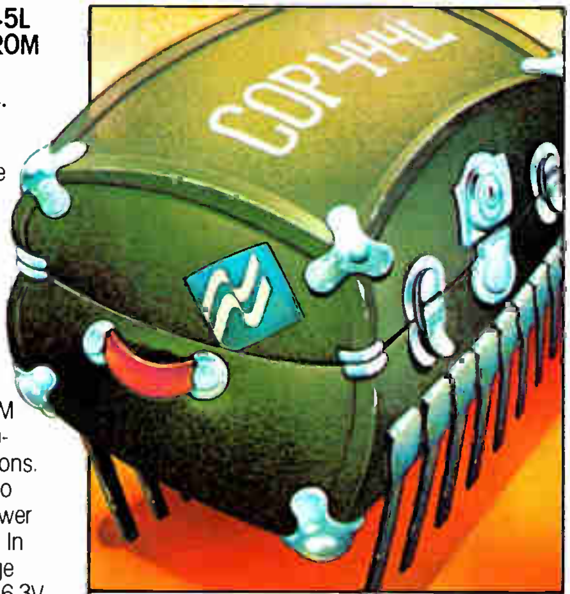
National announces two powerful new microcontrollers.

The new COP444L and COP445L microcontrollers pack 2K x 8 ROM and 128 x 4 RAM into the family's standard packages.



Two new high-end COPS™ Family microcontrollers, the COP444L and the COP445L, offer twice the on-chip memory as any other family member.

Both devices are compatible with the rest of the family in all respects – the architecture, instruction set, packages and options. But the COP444L (27 I/O lines; 28-pin DIP) and COP445L (19 I/O lines; 24-pin DIP) each carry 2K x 8 ROM and 128 x 4 RAM for the most advanced single-chip solutions for large microcontroller applications.

Another clear advantage of the two new COPS is their amazingly low power requirements: 55mW at 5V operation. In addition, they're available in two voltage range options, 4.5V to 9.5V or 4.5V to 6.3V.

The distribution of intelligence. The COPS Family represents a unique approach to microcontroller applications.

Every COPS peripheral device has enough intelligence designed into it to execute several instructions on its own. By distributing the processing workload to each device on the MICROWIRE™ every COPS system is optimized for efficiency.

And because the COPS instruction set consists of simple task-oriented operations, they not only take up less memory space, they also accomplish each task in less time than other single-chip microcontrollers.

The benefits of this family approach are felt throughout the development phase as well. The entire family is supported by a single development system (the COP400-PDS). Real-time emulation of the COP444L and COP445L is performed by the COP-E04L board. The COP400-T01 functional tester is a development system option useful in testing any COPS device.

Freedom of choice. So now the design engineer can pick and choose from a wide variety of key specs: CPU size, fabrication technology (CMOS, low-power NMOS, high-speed NMOS), the temperature range, the voltage range, the speed, the I/O options and the package size and type.

In short, the COPS Family offers the freedom to choose from a broad range of compatible microcontrollers and peripherals to closely match the requirements of each design.

And now that the high-end COP444L and COP445L are readily available, there's all the more reason to exercise that freedom.

For more information on these devices and the entire COPS Family, check box number 044 on this issue's National Archives coupon.

COPS and MICROWIRE are trademarks of National Semiconductor Corporation

Superior PCM filter gets digital switching systems off hold.

National Semiconductor advances digital telecom technology with their new low power P²CMOS TP3040 filter.

National is taking the leadership role in telecom with the addition of their new TP3040 PCM filter.

Its unique monolithic design incorporates both transmit and receive filters for 8kHz PCM codec filtering applications.

The TP3040 offers clear performance advantages over its pin-compatible counterparts, particularly in terms of power consumption. The TP3040 uses up to 85% less power than the competition.

Other performance enhancements include a lower noise level (1-2 dBrnCo), reduced crosstalk (−80dB typical) and better rejection of frequencies below 200Hz.

This kind of performance is a direct result of NSC's innovative double-poly, silicon-gate P²CMOS technology (see the article at right).

The Practical Wizards are already turning TP3040s out in high volume. And they'll be second-sourced within six months.

So now telecom design engineers can get their switching systems off hold with a truly superior PCM filter from National Semiconductor.

For complete details on the TP3040, check box number 054 on this issue's National Archives coupon.

P²CMOS yields higher performance.

The Practical Wizards at National Semiconductor have taken a major step toward advancing digital switching technology.

Their new double-poly, silicon-gate CMOS process, P²CMOS, dissipates much less power than competitive technologies. It also allows for more efficient op amp configurations with lower noise and improved power supply rejection ratio.

National brought together the most advanced fabrication techniques to perfect P²CMOS. Ion implantation, dry plasma processing, selective field oxidation and non-contact printing combine to yield the low power of CMOS plus the high speed of NMOS.

P²CMOS. A perfect example of what Practical Wizardry is doing for telecom.

Low pressure absolute transducers. High performance inside and out.

Ion Implantation and new die sealing technology combine to yield six new high-stability transducers.

National has just introduced two all-new series of low pressure absolute IC transducers in the LX1600 and the LX1800 Families.

By combining a state-of-the-art Ion Implantation process with a new die-sealing technology adapted especially for transducers, the new low pressure (10-20 psia to 0-30 psia) LX1600s and LX1800s meet guaranteed offset stability specs as low as 1.7% FS.

In addition, new cavity etching and low temperature processes assure high yield ICs. And that means consistent volume availability at very attractive prices.

The LX1601/02/03-A and LX1801/02/03-A transducers are fully signal-conditioned and feature built-in temperature compensation and full voltage regulation.

And both are available in the industry's widest variety of nylon, zinc or compact ceramic housings. As a result, these versatile new devices are just as much at home in rugged plumbing fixtures as they are in delicate PC boards.

Low pressure absolute transducers from National. Proving once again that practicality comes in all kinds of packages.

For more information, check number 041 on this issue's National Archives coupon.

It's about time – new μP-compatible clocks.

Two new low-power real-time clocks keep track of everything from tenths of seconds to leap years.

The Practical Wizards have developed two new MICROBUS™ compatible CMOS/LSI chips that perform all time- and date-keeping functions for microprocessor and microcomputer applications.

Both the 8-bit (24-pin) MM58167 and the 4-bit (16-pin) MM58174 real-time clocks are based on 32.768kHz crystal oscillators. So these clocks keep a precise accounting of time increments ranging all the way from thousandths of seconds to leap years.

They also feature a power-down mode for extremely efficient operation. The MM58167 takes voltages as low as 2.0V and the MM58174 as little as 2.2V.

Their mask-programmable interrupt timers can be set to provide a variety of interrupt signals ranging from 0.1 sec to 1 month. The MM58167 also includes alarm-type latches and a standby interrupt for μP wake-up during power-down mode.

Finally someone is offering multi-functional yet practical clocks for μP-based designs.

Check number 044 on the National Archives coupon for complete information.

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LED, LCD and VF drivers display family unity.

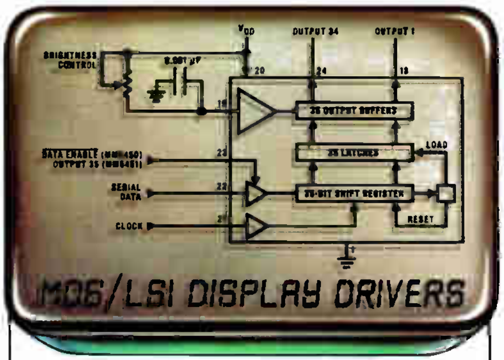
The Practical Wizards offer a complete family of software compatible MOS/LSI display drivers that use a simple serial interface to a μP bus.

National Semiconductor presents the industry's only true family of LED, LCD and VF display drivers.

Their broad line of compatible drivers is designed to meet all typical display driving needs in software controlled applications. So whether the design calls for LED, LCD or VF displays, the microprocessor, COPS™ Family or other microcontroller needs only one software routine to make the interface to any of the 40-pin drivers.

The practical approach. To make these devices even more practical and easy to use, they utilize a simple serial data input channel. In addition, the LED and VF drivers feature a continuous brightness control pin that respectively requires a current or voltage source.

As shown in the product summary table below, the Practical Wizards are offering four PMOS vacuum fluorescent display drivers. These parts, the MM5445/46/47/48, respectively drive 32, 33, 34 and 35 segment displays.



The NMOS MM5450/51 LED drivers can handle 34 and 35 segments, respectively. The CMOS MM5452/53 LCD devices drive 32 and 33 segments, respectively.

The remaining two family members, the MM5480/81, are lower cost LED drivers designed for smaller scale application needs. The 28-pin MM5480 drives 20 segments and the 20-pin MM5481 drives 14 segments. These parts are therefore not software compatible with the rest of the family.

The DATA ENABLE feature on the MM5445/46/52/81 allows these devices to be cascaded.

Once again, National Semiconductor comes through with a broad line of practical and reliable components.

For more detailed information, check boxes 044 and 053 on this issue's National Archives coupon.

DISPLAY DRIVER SUMMARY TABLE

PART NUMBER	DISPLAY TYPE	SEGMENTS DRIVEN
MM5445	VF	32
MM5446	VF	33
MM5447	VF	34
MM5448	VF	35
MM5450	LED	34
MM5451	LED	35
MM5452	LCD	32
MM5453	LCD	33
MM5480	LED	20
MM5481	LED	14

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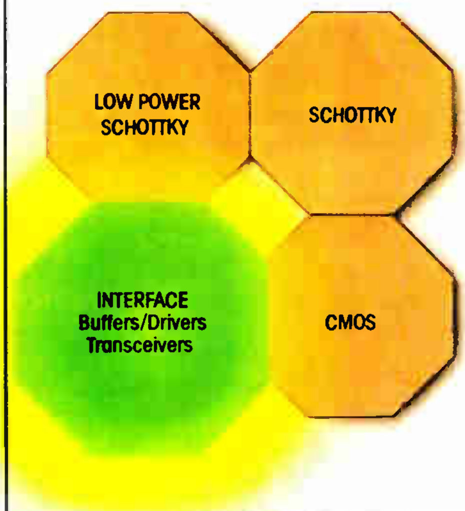
TRI-STATE® octals in 28 varieties.



National Semiconductor carries the industry's broadest line of 20-pin LS, Schottky, CMOS and Interface octals.

National Semiconductor is doing more for 8-bit designs than anyone else. In fact, they're currently offering no less than 28 different TRI-STATE octal devices.

So now the designer can select his 8-bit building blocks from the industry's largest assortment of 20-pin Low Power Schottky, Schottky, CMOS and Interface products. Everything from buffers/drivers, latches and D flip-flops to I/O registers and bidirectional transceivers.

National is currently offering no less than seven different Interface octals, all in both commercial and military versions. See the product table below for specifics.

The Practical Wizards are doing more for TRI-STATE octal designs than anyone in the industry.

For more information, check box number 045 on the National Archives coupon.

INTERFACE OCTALS

Device Type	PART NUMBER Commercial	Military
Buffers/Drivers	DS3628	DS1628
	DP8310*	DP7310*
	DP8311*	DP7311*
Transceivers	DP8303	DP7303
	DP8304B	DP7304B
	DP8307	DP7307
	DP8308	DP7308

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*These devices are open collectors.

Now microcomputers know when they're making a mistake.

Parity and Error Checking and Correction make NSC's BLC-8064 Family more reliable than conventional microcomputer memories.

Until now, microcomputers had to make do with conventional memory and the consequences of undetected error.

But now, National Semiconductor provides Error Checking and Correction (ECC) or parity for their BLC-8064 Family of board level computer products: the BLC-8016 A&B (16K RAM), the BLC-8032 A&B (32K RAM), the BLC-8048 A&B (48K RAM), and the BLC-8064 A&B (64K RAM). The A versions feature parity and the B versions feature ECC.

A logical approach to system design. With ECC, all single-bit errors are detected and corrected so efficiently that the processor never misses a beat. If a double-bit error occurs, the board simply notifies the processor.

BLC-8064 Family boards with parity notify the processor when they detect any odd number of bit errors.

ECC and parity open up vast new microcomputer applications that were previously too sensitive to fluctuation and error to trust to conventional memory systems.

Leave it to the Practical Wizards to bring this kind of reliability to microcomputer applications.

For more information on the BLC-8064 Family, check box 049 on this issue's National Archives coupon.

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041 ☐ Pressure Transducer Data Packet
044 ☐ 1980 MOS Data Book ($4.00)
045 ☐ TRI-STATE Octal Data Packet
049 ☐ BLC-8064 Family Data Sheets
053 ☐ MOS/LSI Display Driver Family Data Sheets
054 ☐ TP3040 Filter Data Packet

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National Semiconductor
The Practical Wizards of Silicon Valley

NA 21

that this size is more than adequate to handle about 80% of the tasks users want to perform."

In contrast to small modeling programs already available like VisiCalc, Brown says, FPL offers such advantages as IF...THEN...ELSE computing capability. It also documents the rules used to create data, he says: "Instead of getting a + b = c on a spread sheet, you get a spelled-out explanation of each of the elements being processed."

At the other end of the scale are financial modeling programs that are vastly more complicated than FPL. For example, Express, a model offered by Tymshare, requires a minimum system memory of from 512-K bytes to 1 megabyte, and FPL "is not in the same league," says Robert L. Schwartz, vice president of the Information Services division in Cupertino, Calif.

Upward mobility. He does agree, however, with Russell E. Edwards, senior vice president at Capex Corp. in Phoenix, Ariz., that offerings like FPL can attract users who will trade up. "It will likely be a good tool, and instead of taking away from our market base, it will open up more markets," says Edwards.

In recognition of these new markets, Capex has developed Autotab 300. "It is a step down in size and capacity from Autotab II," Edwards says. The program uses about 60-K bytes of the 256-K-byte virtual memory in a minimally configured Hewlett-Packard HP 300 business minicomputer.

-Ana Bishop

Industrial

Process controllers get new competition

The steady advance of programmable controllers into minicomputer process-control territory continues with Allen-Bradley Co.'s new PLC-3. It boasts a greatly expanded instruction set with floating point math and data storage for as much as 96,000 16-bit words.

Microprocessors and associated solid-state circuitry have been adding computer sophistication to programmable controllers for some time [*Electronics*, Feb. 28, 1980, p 171]. But the increased processing power and a data memory 12 times greater than the firm's PLC-2/20 will further enhance speed and precision, making possible use in process control. The new machine will also perform considerably more data processing in generating reports, says the Highland Heights, Ohio, Systems division.

Performance. Nominal execution time is specified at 1 millisecond per 1,000 instructions, three to four times faster than the PLC-2/20, says Ronald J. Toke, programmable controller product marketing manager. The precision possible with the floating-point math will be useful in process-control applications where analog inputs require multibit representations, he says.

Part of the power boost for Allen-Bradley's PLC-3 is the central processing unit of four AMD2903-type 16-bit-slice bipolar microprocessors. The unit also uses two 16-bit Z8002 microprocessors, each controlling up to four channels addressing 1,024 input/output points each. The CPU takes up two of the unit's maximum of six boards. Overall measurements of the controller are 19 by 20 by 14.5 inches.

Users can choose from three types of data memory. The complementary-MOS random-access memories are available in 8-, 16-, and 32-K increments, and RAM boards can include error-correction logic for single-bit errors. Also available is core memory in 16- or 32-K increments.

With availability scheduled for the fourth quarter, systems might cost from $30,000 to $60,000, a healthy hike over the $4,500-to-$12,000 range of the PLC-2/20. However, the new model is not intended as a replacement for the PLC-2/20; rather it is a move towards the level of process-control computers.

The new unit's 8,192 I/O points, compared with the PLC-2/20's 512, also permits increased control over a process. Such an I/O capability is not new to programmable controllers—it

is a feature on the year-old model 584 from Gould Inc.'s Modicon division, the other major competitor in the market.

The two firms are in strong competition, controlling between 60% and 80% of the U.S. domestic programmable controller market, by various estimates, with Modicon's share at least as large as Allen-Bradley's. The market is expected to grow about 30% to some $270 million this year.

Although the PLC-3 represents a jump ahead of its competition in computing capability, it will not be alone for long. Modicon, for one, plans enhancements for its 584.

Ladder logic. Despite the increased computing sophistication of their offering, the controller makers are continuing efforts to make their machines friendly to factory personnel, who are most comfortable working with languages that mimic the traditional ladder diagrams used with the relays that the programmable units replaced. "We're going in the direction of computer instructions, but they're presented in the format of ladder logic," says Allen-Bradley's Toke.

Like the PLC-2/20, the PLC-3 can function in a distributed network, sharing control with its counterparts. Modicon's 584 currently requires a hierarchical network with a central computer as controller, but an enhancement later this year will let a 584 act as a master controller, says Thomas M. Duff, product marketing manager at the Andover, Mass., division headquarters.

With that enhancement, the company's Modbus network will support as many as 250 slaves, running at 19.2 kilobits per second, he says. Allen-Bradley's 57.6-K/s Data Highway network will support up to 64 units, including programmable controllers, terminals, and printers.

Modicon also plans to expand the 584's RAM, from 32-K to 128-K 16-bit words, by late in the third quarter. Floating point instruction capabilities for the controller are also under development, but the company is not ready to make an announcement of them. **-Wesley R. Iversen**

SCIENCE/SCOPE

A prototype of the system that will serve as radar and radio for NASA's Space Shuttle has met its scheduled completion date and is undergoing tests. As a radar, the system will allow astronauts to rendezvous with orbiting satellites in order to repair or retrieve them. It also can track any payloads released from the Shuttle. As a radio, the system will link with the Tracking and Data Relay Satellite System to let astronauts communicate with stations on earth. Hughes delivered the Ku-band integrated radar and communications system, as it is called, to Rockwell International, builder of the Space Shuttle.

Laser designators, devices used by the military to pinpoint targets for laser-homing weapons, can now be tested automatically by a new computerized system. The laser is fired into a collimator to test laser energy output, beam divergence, pulse width, and boresight. Video imagery taken through the eyepiece, along with energy output data, is fed into a computer for analysis. The system, called the Automatic Laser Inspection Measurement System (ALIMS), was designed by the U.S. Army Missile Command to support production of Army laser designators. Hughes converted the design into a working system that is faster and more accurate than performing laser quality tests manually.

A device that scans the sky with heat sensors to detect, track, and identify aircraft and missiles is being developed by Hughes for the U.S. Air Force. The device, an electro-optical threat sensor, could be used with ground, ship, or airborne fire control systems. The sensor holds several advantages over conventional radar. It emits no telltale radiation of its own, it is small, and it can search a wide area rapidly. A signal processor extracts the target signal from the background radiation and feeds this data to a computer, along with the target's relative bearing. An interrogation unit then uses additional sensors to classify targets further. The computer processes the information to classify each target by type and lists them in order of priority.

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Smart weapons of tomorrow will rely on sophisticated algorithms to pick out their own targets and aim for the most vulnerable spots. The new weapons, like the Wasp anti-armor missile that Hughes is developing for the U.S. Air Force, will incorporate densely packaged electronic components and new low-cost, compact signal processors. The Wasp's automatic target selection will free pilots from time-consuming target detection tasks, thereby increasing weapon delivery rates. Also, the "fire-and-forget" capability reduces the need for close approaches to the target, thereby decreasing pilot exposure to enemy defenses.

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Weapons too complex, says GAO report . . .

Increasing weapons system spending will not improve U. S. readiness unless the Defense Department and its design contractors place more emphasis on quality assurance and field logistics support. What's more, while lowering the cost, schedule, and performance criteria now used, they must take into account the relatively low-skilled servicemen who use and maintain the weapons. That is the conclusion being drawn in a new report to Congress from its investigative arm, the General Accounting Office. Weapons systems are becoming too complex, incorporating too much **"unproven state-of-the-art technology in individual systems, and relying on too much automatic test equipment, inadequate training, and reduced numbers of personnel,"** concludes a panel of industry and academic experts consulted by the GAO. Issued at the end of January under the title "Effectiveness of U. S. Forces Can Be Increased through Improved Weapons System Design" (PSAD-81-17), the report was described as excellent and well balanced by Walter B. LaBerge, principal deputy to the under secretary of defense during the Carter Administration.

. . . with electronics linked to 9 of 21 'undependable' systems

Nine of the GAO's 21 examples of equipment reported by the services to be "undependable and difficult to support and operate" involve electronics. These include the Air Force F-15 fighter's avionics automatic test equipment, which has "low reliability [and] some software incompatibility" and suffers from a lack of trained, experienced personnel. One Air Force source confirmed that **the plane's avionics ATE system was down half the time and was unable to identify problems 40% of the time when working.**

High failure rates, low reliability when operating, replacement parts shortages, and inadequately trained technicians were also cited as problems on such Navy surface ship radars as the AN/SPG-55B for guided-missile control and the AN/SPS-40 for air search and on the BQQ-5 sonar for SSN-688-class attack submarines. The Navy's S-3A antisubmarine warfare plane suffers from poor operational availability because of the "low reliability of many key electronic components." The "significantly large number of random failures among the 40,000-plus parts" of the Navy's surface ship MK-86 gun fire-control systems was cited as an example of overcomplex designs. Two Army antitank missiles regularly miss targets: the Dragon system's, because of component failure plus the shock it delivers to the user on firing, and the TOW system's, because unreliable batteries make firings unreliable or cause loss of guidance in flight.

Comsat General buys second software firm

Comsat General Corp., the domestic satellite subsidiary of Communications Satellite Corp., has acquired another developer of computer software for integrated-circuit simulation and testing **to strengthen its new organization for computer-aided design, manufacturing, and testing** [*Electronics*, Nov. 6, p. 55]. The latest takeover by Comsat General Integrated Systems Inc.—the CAD-CAM-CAT subsidiary formed last fall in Palo Alto, Calif., with the acquisition of Compact Engineering—is Comprehensive Computing Systems and Services Inc. of Austin, Texas. The firm, whose CC-Texas software is used to simulate and test complex digital ICs, will be operated as the CGIS Digital division by its founder, Stephen A. Szygenda, who becomes a senior vice president.

Washington commentary

Telecommunications issues for the 1980s

With most analysts in the capital apparently agreed that the issue of competition between communications giant American Telephone & Telegraph Co. and everyone else will be resolved this year, the dominant new telecommunications issues of the 1980s fall into two technical categories: spectrum management and standards for new services.

By March 4, Federal Judge Harold H. Greene will receive the proposed settlement between the Justice Department and AT&T of the Government's six-year-old antitrust suit. And it will be some months later before the court decides to accept or reject the settlement, as the law now requires affected outside parties to be given an opportunity to study and comment on the plan.

Nevertheless, five leading telecommunications experts in Washington were unanimous in their opinion that the AT&T suit will soon be settled and that the telephone company will emerge relatively unscathed to move strongly into new, deregulated markets. In agreement were Robert R. Bruce, general counsel for the Federal Communications Commission; Herbert N. Jasper, executive vice president of the Ad Hoc Committee for Competitive Telecommunications; Ward H. White, minority counsel for the Senate communications subcommittee; Bernard J. Wunder, House communications subcommittee chief counsel; and Thomas R. Phillips, an AT&T assistant vice president. Their opinions came in response to a question from former FCC chairman Richard E. Wiley, now a Washington lawyer, at the conclusion of a panel he moderated during the Infotel conference held at the end of January in Washington.

The question then is where the U. S. telecommunications industry goes from here. Like the data-processing industry dominated by IBM Corp., telecommunications seems assured of continued expansion and growth despite the continued domination by AT&T in wired systems and, probably to a lesser extent, in microwave and satellite technologies.

Spectrum and standards

With that market scenario apparently set, U. S. telecommunications equipment makers and their designers will move on in the coming decade to the two critical issues of spectrum allocation and technical standards. Richard Neustadt, associate director of the White House Domestic Policy staff under Jimmy Carter, put it best with his observation that "if competition was the central issue of the 1970s, spectrum management will dominate in the 1980s."

To avoid future congestion, the FCC must continue its recent demonstrations of flexibility in both spectrum allocation (deciding how to use each band of frequencies) and assignments (deciding who gets an individual frequency within each band), Neustadt points out. If the FCC continues to permit several services to share a spectrum block and then to let the marketplace determine which services need larger assignment, the former White House staff member believes that the old problem of assigning narrow portions of spectrum to narrowly defined services can be left behind.

The teletext dilemma

Technical standards for new services presents a much trickier issue, however. "When the FCC picked a system for color television in the early 1950s," Neustadt recalls, "it had to switch horses after three years. The commission may be in the midst of a similar experience with its a-m stereo standard. In contrast, unregulated battles over video cassette and video disk formats—while messy—are not stifling development but are spurring innovation in directions consumers like."

In the broadcast marketplace, though, "standard setting is a chicken-and-egg dilemma," he points out, noting that setting them too early in technology development can retard innovation and wreck a new market. But without standards, software development can be slowed as producers wait to see which product consumers choose. "Hardware and software interests dance a subtle tango," Neustadt believes, while consumers either hold back or take a chance on an incompatible system.

Developing an American standard for teletext is a case in point. Whereas France has conducted tests on its Antiope system for some five years, the U. S. industry is still divided on the issue. Whether or not the FCC can resolve it by acting on the recent move by CBS to get Antiope adopted as teletext standard in this country is still an open question. Yet, if the FCC is to continue down the deregulation path and get Government off the nation's back, as President Reagan has so often promised, then the issue of standards for teletext and a host of other new and promising growth markets will require the same kinds of realism and creativity from the FCC that it is beginning to show in spectrum management. Otherwise, the U. S. may find it has fallen behind in the world competition for a major new market. **-Ray Connolly**

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32DR COMPULYTIC®	1.375 x 2.125 to 3.000 x 8.625	—40°C to +85°C	7.5 to 100	410 to 310,000	3441E
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622D EXTRALYTIC®	1.375 x 2.125 to 1.375 x 5.625	—55°C to +85°C	5 to 55	2,800 to 67,000	3459
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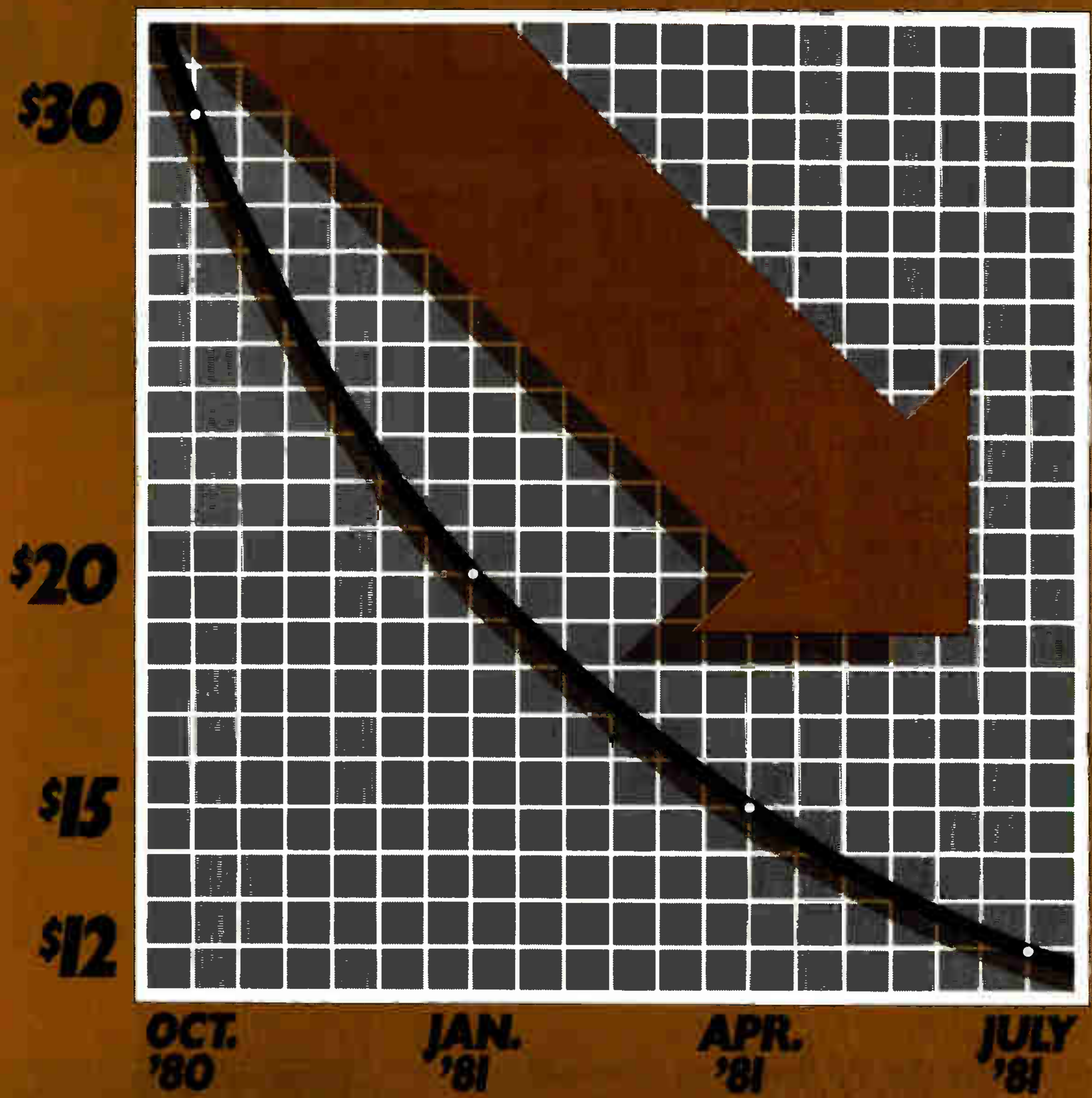

Prices shown are for 100-piece quantities. Lower prices are applicable for volume requirements.

Feb. 10, 1981

Electronics International

Low-cost wattmeter evolves from UK standard: page 77

Marking Philips' entry into the facsimile market are three units that meet CCITT standards and can send photographs to each other: page 82

ers. **Industry sources believe the main customer will be Sears, Roebuck,** though until now Sears has only handled Beta-format VCRs.

Meanwhile, NV Philips Gloeilampenfabrieken had a pleasant surprise for the West European consumer electronics community, under heavy pressure from Japan. In its drive to capture half the West European VCR market, the Dutch firm has picked up enough momentum that it plans to add a new supply center to the one in Vienna by converting a black and white TV plant in Krefeld, West Germany, to VCR production.

French packet-switching net to switch to Z80-based switches

The new generation of switches for France's public packet-switching network, Transpac, will be furnished by SESA, the systems and software house responsible for the existing switches. But in contrast to that expensive and bulky minicomputer-controlled hardware [*Electronics*, April 12, 1979, p. 70], the new Transpac switches will be built with modules controlled by Z80 microprocessors. SESA (Société d'Etudes des Systèmes d'Automation), based in the Paris suburb of Puteaux, **has already sold its new packet-switching system, the DPS 25, to the International Railways Association for its Hermes network and to the European Space Agency for its rocket-launch tracking network.**

NEC to market smaller, lower-cost speech-recognition unit

The DP-200 speaker-dependent speech-recognition system from Nippon Electric Co. is half the price and one tenth the size of NEC's present DP-100 system [*Electronics*, April 13, 1978, p. 69]. Priced at $24,000 in Japan, the new system is expected to sell much better, being intended for computer-input and other data-processing applications, whereas the DP-100 is used mainly in routing and classifying parcels in transportation firms and warehouses. The basic DP-200 can **recognize up to 50 words linked in phrases of up to 5 words, a figure that can be expanded to 150 similarly linked words or 500 discrete words.** Deliveries will start in Japan in May, exports several months later.

Stop-start system saves fuel in new VW

Volkswagenwerk AG of West Germany is equipping its new Passat E passenger car with an electronic system that helps save up to 15% of fuel in city driving. Called the stop-start system, it shuts down the engine when the driver is waiting at a red light or is stuck in traffic jam. The driver triggers it with a push of a button mounted on the windshield wiper lever, thus blocking the fuel supply. Then by stepping on the gas pedal (with the clutch disengaged), he or she starts the engine up again. This stop-start operation, during which electrical loads such as the headlights, radio, and air blowers remain on, **is possible only when the engine is warm and the car is going at less than 2 km/h** (about 1.2 mph).

Addenda

Targeting a total world market for semicustom circuits of $100 million in 1981, Marconi Electronic Devices Ltd., General Electric Co. Ltd.'s newly reorganized semiconductor activity, is teaming its three-year-old Cellmos automatic cell placement and routing software with the high-density, low-power Iso-C-MOS process it recently licensed from Mitel of Canada.
. . . Sharp Corp. of Japan says that it will start shipping **4-K or 16-K samples or both of its amorphous silicon electrically erasable memories** in April or May and begin full-scale production before the end of the year.

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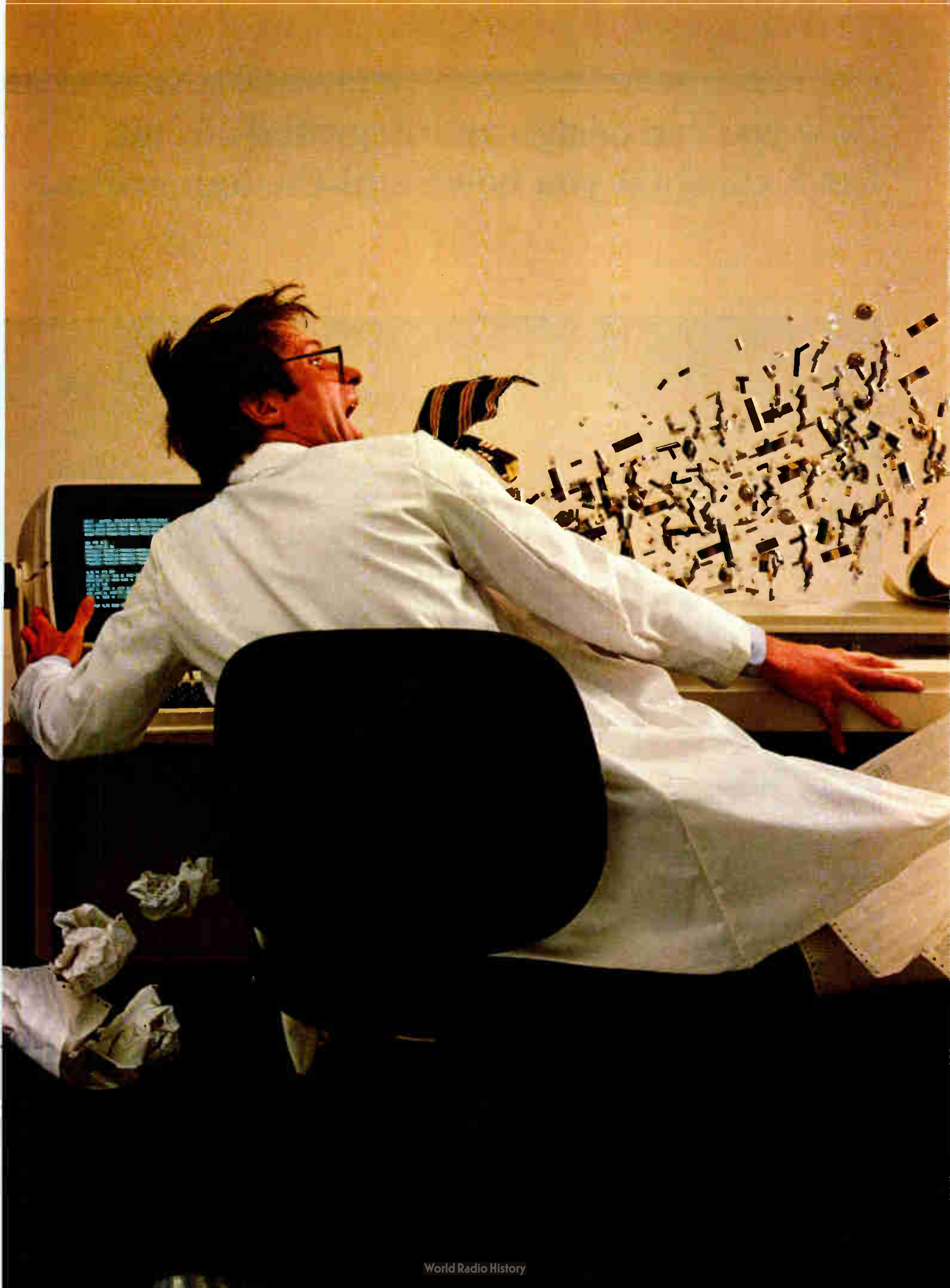

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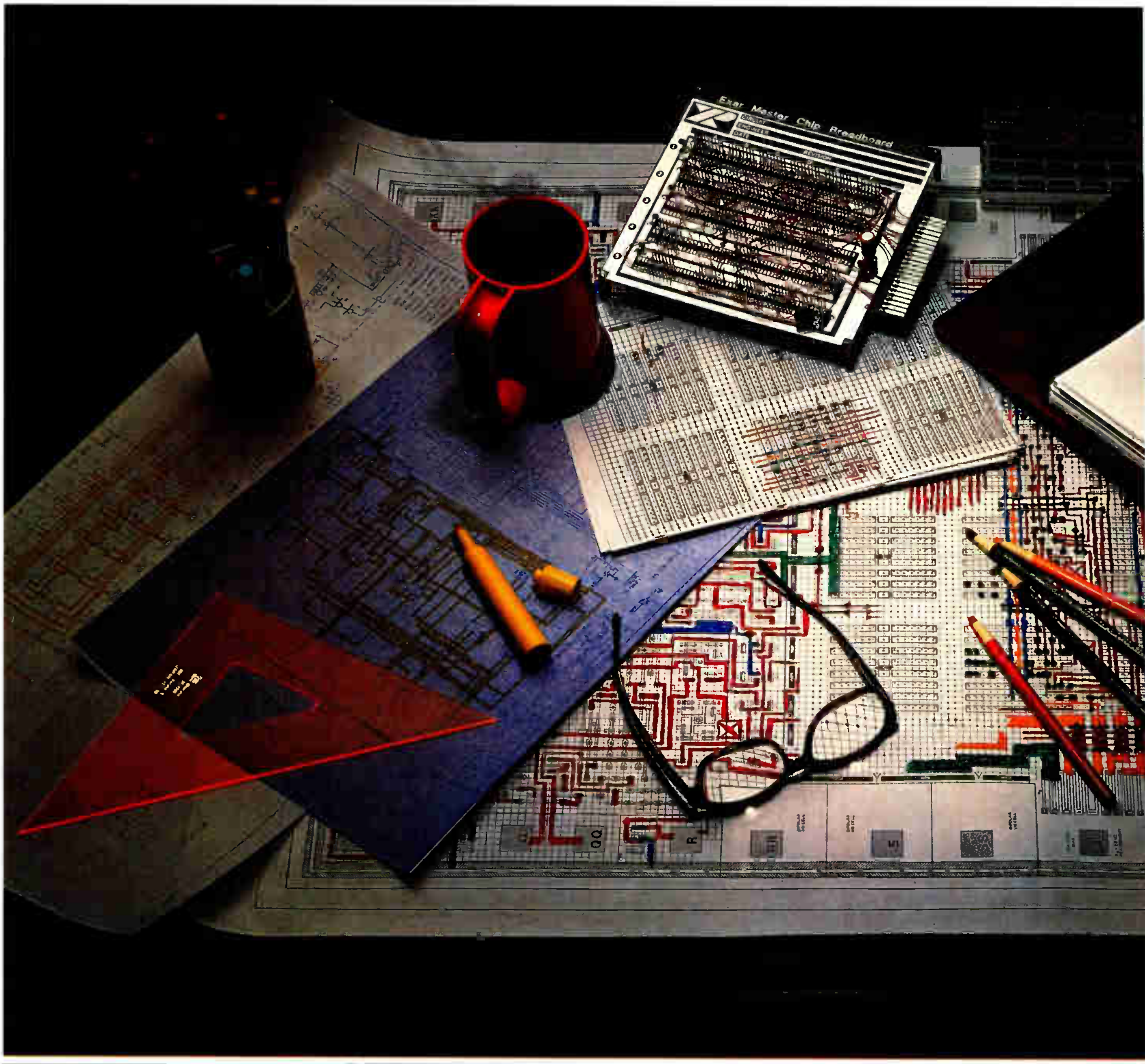

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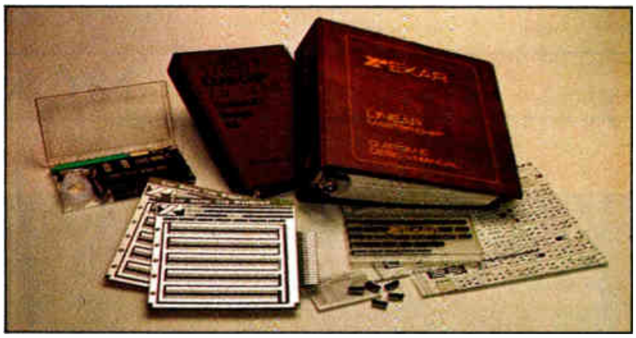

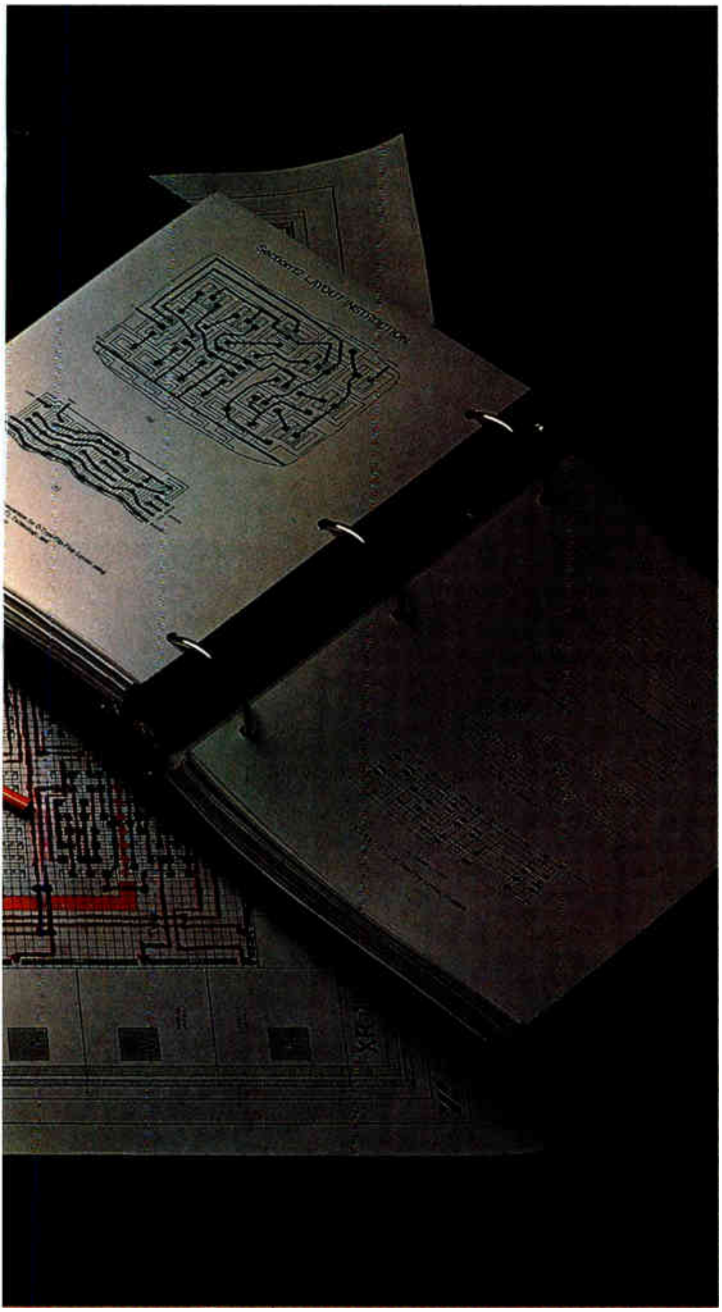

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NEC recently unveiled an ultra-large general purpose computer called the SYSTEM1000. At present, it is the largest commercially available computer in the world. The SYSTEM1000 was developed to meet increasing needs for large-scale processing in on-line data base systems, engineering calculations and communications networks.

NEC SYSTEM1000 has a 64MB main memory, and a 128KB cache memory. No other commercial computer can match these figures for main memory, cache memory and processing speed.

To develop the SYSTEM1000, NEC made full use of its advanced LSI technology. The SYSTEM1000 incorporates high-speed logic LSIs, 64-kilobit/chip high-density MOS LSI memories, and LSI high-density packages with up to 60 chips mounted directly on a multilayered substrate.

A special feature of the SYSTEM1000 is a very large data array address function which gives direct access to a volume of data as large as 1 gigabytes by using a virtual memory. The execution processing unit incorporates an integrated array processor which can work out large-scale vector and matrix calculations very quickly.

* As of December 24, 1980

SWEDEN TESTS 140MB DIGITAL MICROWAVE SYSTEM

The Swedish Telecommunications Administration is conducting field tests on an NEC-supplied two-hop 6.8GHz 8-phase 140MB digital microwave system. NEC is currently the world's only supplier of this type of system which features the highest bit rate recommended by the CCIR.

The system transmits CEPT hierarchy 140Mbps digital signals, using an 8-phase PSK modulation system, over the radio frequency band ranging from 6,430MHz to 7,110MHz.

The digital capacity is equivalent to 1,920 PCM telephone channels.

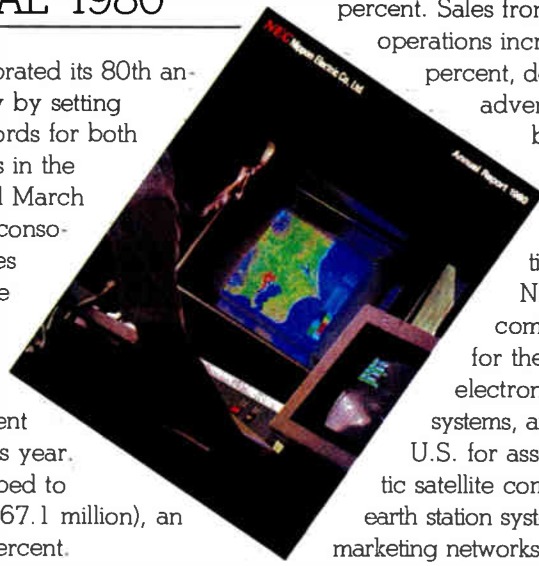
The transmitter-receiver may also be used in analogue service with a capacity equivalent to 2,700 FDM telephone channels.

The system will be put into commercial use in the public telephone network next year after testing is completed.

NEC has also received orders for the system from Denmark and Switzerland. Many other European countries are taking great interest in the 6.8GHz 8-PSK 140Mbps digital system.

RECORD INCOME AND SALES IN FISCAL 1980

NEC celebrated its 80th anniversary by setting new records for both income and sales in the fiscal year ended March 31, 1980. On a consolidated basis, sales and other income for 1980 rose to ¥879.31 billion ($4.03 billion), a gain of 9 percent over the previous year. Net income climbed to ¥14.62 billion ($67.1 million), an increase of 85 percent.



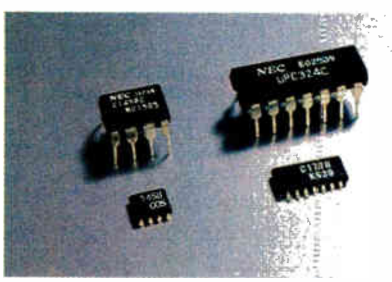
All four of NEC's major product lines recorded impressive growth in sales, with Telecommunications up 9 percent, Electronic Data Processing and Industrial Electronic Systems up 19 percent, Electron Devices up 35 percent and Consumer Electronics up 26 percent. Sales from international operations increased by 24 percent, despite a generally adverse international business environment.

To strengthen its international operations, NEC set up a new company in Brazil for the production of electronic switching systems, and a plant in the U.S. for assembly of domestic satellite communications earth station systems. In addition, marketing networks were expanded in both the U.K. and the U.S.

(In this article, ¥218=US$1.)

NEW FAMILY OF MINI ICs

To meet the need for smaller, more highly-integrated package ICs, NEC has begun marketing a new mini IC which is only 1/8 the size of standard package products.



The new package IC family is called the "Mini Flat Package Linear Series". It is offered in two types—one with 8 pins, the other with 14 pins.

Dimensions with the pins not included are 4.4 x 5.0mm for the 8-pin devices, and 4.4 x 10.0mm for the 14-pin products. Both types are a mere 1.5mm thick; pin pitch is 1.27mm, just half that of standard products.

The new ICs will be used in communications equipment, household appliances and consumer products. They will act as general purpose operational amplifiers or circuit modules in hybrid ICs.

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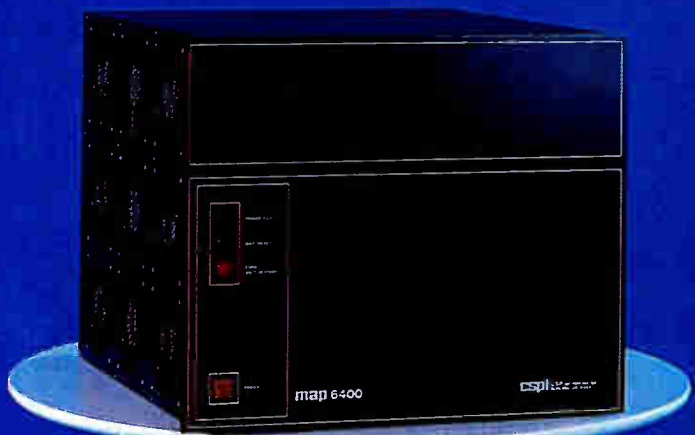

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Circle 76 on reader service card

Industrial wattmeter uses same principle as new national standard

by Kevin Smith, London bureau manager

Prototype replaces logic with dual-ramp converter pair to measure and multiply voltage and current values

A high-precision digital wattmeter for measuring alternating current power may serve as both a national standard for the UK and—with some modifications—as a low-cost industrial instrument. The meter was developed at Britain's National Physical Laboratory, the equivalent of the U.S. National Bureau of Standards.

The Teddington, Middlesex–based group first built a general-purpose computer-driven instrument to which the calibration of all watt and energy meters in the country will ultimately be traceable. From that it has developed a prototype industrial version employing the same measurement principle—simultaneous sampling of the voltage and current waveforms.

The prototype fits into an adapted digital voltmeter case just 20 centimeters wide, has a five-digit liquid-crystal display, and uses standard large-scale integrated circuits to cut the component count. Several British companies are interested in its manufacture, though the market is relatively specialized.

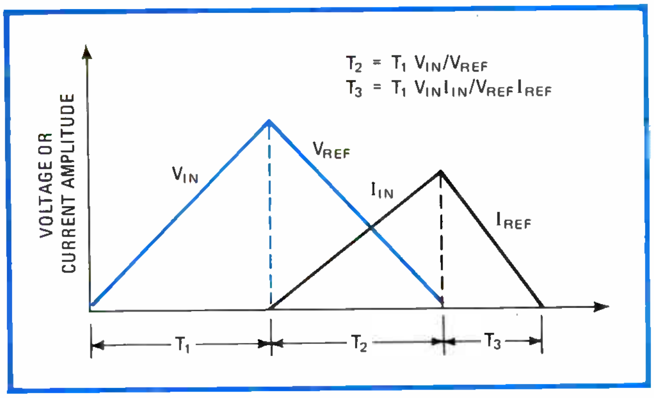
Ten times better. The new calibration standard is the outcome of a five-year investigation into electronic techniques of measuring ac power. Although a final assessment of its accuracy has yet to be completed, the NPL team hopes it will in the longer term improve at least an order of magnitude on the present standard, reaching perhaps 1 part in 10^5. More significantly, the system, incorporating a Digital Equipment Corp. LSI 11, two floppy-disk drives and cathode-ray display, will be far easier to use.

The multiplication of voltage and current variables to determine power is done mechanically in the electrostatic or electrodynamic instruments used by the National Bureau of Standards, for instance. To achieve a similar or improved accuracy electronically, the British researchers settled on a digital multiplication principle. In their technique, voltage and current waveforms are simultaneously sampled at regular intervals over an exact number of cycles at a rate that will accurately represent the highest harmonic present.

The resulting values are digitized and multiplied together to yield the instantaneous power. Subsequently, blocks of samples are averaged and scaled by frequency division to give the average power. The sample timing is controlled by a phase-locked loop, running at a large multiple of the input frequency whose output is divided down to a suitable sampling rate. In a first implementation, NPL researcher John R. Stockton used industry-standard 15-bit converters to feed 30 bits of data in 4 bytes to a SC/MP 1 microprocessor from National Semiconductor Corp., which itself was teamed with an 8-bit single-chip multiplier from GEC Semiconductors Ltd. This has since been superseded by the LSI 11–based system with 16-bit converters in a system built for the laboratory by Micro Consultants Ltd. and programmed in a high-level language.

Paired. A dedicated digital implementation of this technique, even when a microprocessor is used, requires a large chunk of electronic logic and so would be too expensive for industrial use. But by replacing the digital multiplier with an analog multiplier, the component count and hence the cost can be greatly reduced. The technique involves pairing two standard dual-ramp converter chips to perform the multiplication.

In a prototype five-digit instrument, for example, the British researchers use two Intersil 8052 analog-signal conditioners and two 7101 digital processors. In operation, the sample-and-hold circuits acquire



V times I. An inexpensive yet highly precise wattmeter applies dual-slope integration separately to simultaneously sampled current and voltage waveforms. Multiplying the results yields power.

signals proportional to the instantaneous voltage and current waveforms. The acquired voltage is sent to one of the two dual-slope analog circuits and integrated for a fixed number of fast clock cycles. Then it is replaced by a reference value of opposite sign that is integrated down to zero again.

Countdown. The clock count during this interval normally determines the input voltage, but in the NPL technique, this countdown period is used to start integrating the acquired current value in the second converter chip. This in effect multiplies current and voltage variables, so that the clock count of the current converter chip, once ramped down to zero, represents the instantaneous power. The average power is determined by accumulating a block of samples in the output register. Additional circuitry takes the sign of the two variables into account.

The resulting instrument has a resolution of 0.01% and an accuracy of 0.03% at lower power frequencies, deteriorating to about 0.1% at 5 kilohertz. Even so, it represents strong competition for established digital power instruments using pulse-width–height multipliers, of the kind developed by Yokogawa Electric Works. It matches them in accuracy, yet its potential price is far lower.

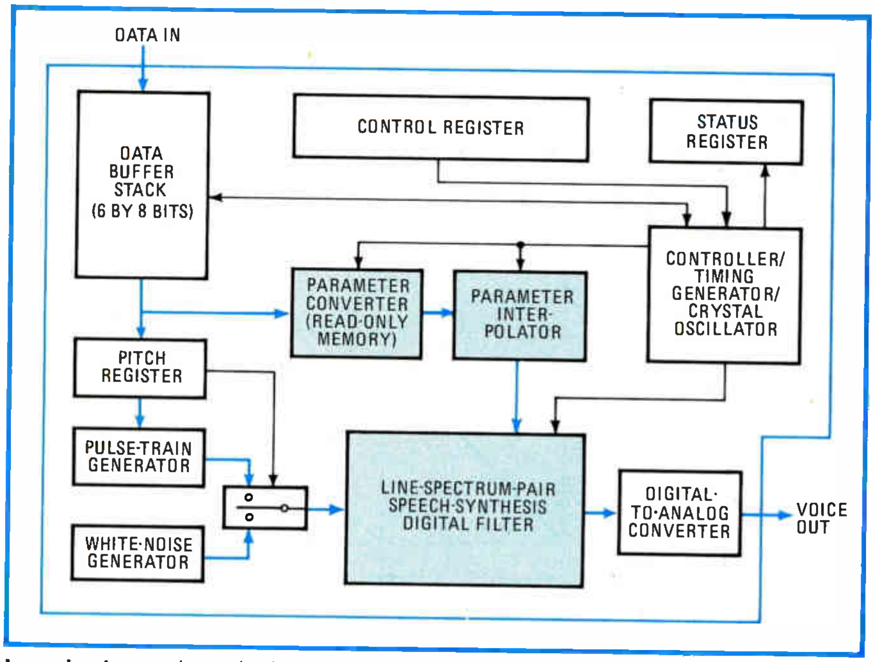
Impetus for the work at the National Physical Laboratory came originally from the need to develop a new ac-power–measuring standard more in tune with the electronic age. The present standard is a masterpiece of the 19th century instrument makers' art, an electrostatic wattmeter in which the attractive force acting on a fiber-suspended vane is detected by the movement of a light beam over a 6-meter scale sited on the far side of the room from the galvanometer. But, according to Brian R. Knight, a principal scientific officer at the NPL, the technicians who built and maintain these instruments are no longer available.

Japan

Frequency analysis of speech shrinks speech synthesizer by 40%

A new method of speech synthesis achieves the same speech quality as today's parcor approach at 60% the data rate—2,400 bits per second as against 4,000 b/s. So only 60% as much read-only memory is needed for the same vocabulary, say its developers at the Musashino Electrical Communication Laboratory of the Nippon Telegraph & Telephone Public Corp.

The method is based on a new way of analyzing speech, in terms of line-spectrum pairs (LSP). With a sampling frequency of 6.4 kilohertz, an experimental LSP system yields a maximum speech frequency of 3 kHz—about the same as on intercontinental telephone circuits.



Laconic. A speech synthesizer using line-spectrum pair instead of parcor analysis needs fewer bits to define parameters and less refreshing because of better interpolation.

The group that evolved the LSP method was led by Fumitada Itakura, who in 1969 developed the partial autocorrelation coefficient (parcor) theory. (It is theoretically the same as Texas Instrument's linear predictive coding.) In his new approach, Itakura views the vocal tract as a resonant cavity with two extremes of resonant frequency—one when the glottis is open and a second when the glottis is closed. These two frequencies as a pair express the transfer function of the vocal tract.

Resonances. If the extreme frequencies are known, the resonances for other conditions can be reproduced by analysis. Since the LSP parameters are frequency parameters, coding is performed by frequency. In contrast, parcor constants are in the time domain.

In one current Japanese implementation, 10 parcor constants are used for synthesizing voice: 7 bits are required for the first constant, 6 for the second, 5 for the third, 4 for the fourth through sixth, and 3 for the seventh through tenth. For LSP only 8 parameters are usually needed, and 4 bits are sufficient for each. Furthermore, LSP has better interpolation characteristics, so that the refresh rate can be slower. Thus in a typical implementation the data for each LSP sample is only 32 bits, compared with 42 for parcor. Also, the refresh rate for LSP is only three

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quarters that for parcor. This gives 34 divided by 42 times 0.75, or an LSP data rate only 0.6 that of parcor.

The experimental LSP synthesizer fabricated by Fujitsu Ltd. for the laboratory uses polysilicon-gate complementary-MOS technology with a 3.6-micrometer gate length. It holds about 25,000 transistors for logic and 1,500 bits of internal ROM.

Choices. Being experimental, the device includes many options. Its digital output is 16 bits, but depending on the speech quality desired, the internal 8-bit digital-to-analog converter may be replaced by an external 12-bit converter. The supply voltage is 3 to 6 volts, and typical current is as low as 3 milliamperes at 3 V for operation at less than 10 milliwatts. However, the internal d-a converter can provide a drive of up to 50 mA when moderate power output is sufficient. Also, for ease in interfacing with a microprocessor, a parallel 8-bit data bus is provided, although a serial bus would be sufficient in many dedicated applications.

The computer-aided chip design was not hand-optimized, making for a rather large 315-by-315-mil (8-by-8-millimeter) die. The chip is housed in a rectangular 64-pin package, because it is readily available and has a large enough cavity. Even with the parallel bus, only 33 pins are required—although additional pins are used for testing.

Few parts. When the chip is used with an 8-bit microprocessor, the only other components needed are a 2732 programmable ROM for data storage and a color TV subcarrier burst crystal if the microprocessor clock is not the correct frequency. A minimum configuration requires a quartz crystal for a clock, a 2732 programmable ROM for data storage, and a counter and a 4017 controller. **-Charles Cohen**

West Germany

Code accompanying TV program turns on video cassette recorder in proposed scheme

A television program triggers a video cassette recorder to record it in a new technique developed by West Germany's Blaupunkt-Werke GmbH. Such a system will be simpler to build and to operate than one that must be preprogrammed with the date and hour of day of a broadcast, says the Hildesheim-based member of the Robert Bosch group.

More than just consumer appeal is at stake here, however. "In the face of growing Japanese competition, we must come up with new ideas" to help the country's ailing entertainment electronics industry, declares Hans-Eckhard Krüger, head of the company's communication systems predevelopment. West Germany's Ministry for Research and Technology supports the storage TV project financially, and Blaupunkt must make the results available to all the country's TV set producers.

A two-year $0.5 million development phase has by now produced a demonstrable ZPS digital identification system, also called the Storage Television System. It could be in practical use within two years, Krüger says, if broadcasters decide to favor it and agree to code the individual programs.

To implement the concept, a decoder in the TV set and of course a video recorder are required. A conventional TV set could be equipped with an external decoder, whose cost of around $100 would be offset by the reduced cost of the recorder.

Identification. Crucial to the technique is a digital code that will be transmitted together with each program and identify it as, say, a newscast, commentary, western, or cultural show. At the receiver, a decoder will separate the code from the video signal and compare it with the contents of a memory in which the viewer has previously entered the codes for the desired programs. When the two match, a video recorder will automatically turn on.

Because the program itself triggers the recorder in the Blaupunkt ZPS system, there is no problem over a delayed or altered schedule. Even unscheduled broadcasts can be taped: viewers could be alerted to or kept up to date on emergencies like forest fires or floods, provided they had previously stored the special code attached to such warnings in the TV set's memory.

Program-triggered recording also relieves the viewer of the rather complicated job of operating the recorder. What's more, because it needs no radio-frequency portion or timing circuits and fewer controls, the recorder can be simpler and therefore less expensive.

The code. In practice, the ZPS code is part of the videotex code, which is now in limited use by West German TV stations and accompanies programs in a till now unused line in the vertical field-blanking interval. Made up of 16 bytes of data, the code denotes the date a broadcast takes place, its country and station of origin, and the type of program. The last named is identified by three digits, of which the first stands for the general class (say, a sports show) and the latter two narrows that down (for instance, the kind of sports involved).

Picked up at the TV receiver and fed to its ZPS decoder, the code is separated from the video signal, undergoes the serial-to-parallel conversion and the comparison processes, and turns on the recorder if the code is the same as that stored in the memory. The 256-byte random-access memory is part of the Intel 8035 microcomputer that monitors the program codes. Its 1-K-byte read-only memory contains the operating control programs for the receiver and recorder setup.

The decoder ignores spurious signals. The recorder turns on only when the decoder has recognized a code three times in a row. It turns off when the code is absent from eight consecutive blanking intervals.

In a typical application, the viewer would pick his daily TV fare from a TV guide in which each program is

identified by its code. He or she would then enter the code on a keyboard of the kind found on infrared remote-control units. Code entry could be done well in advance—theoretically up to a year—of the program's broadcasting time, Krüger says.

Light pen. For simpler code entry, Krüger envisions TV guides that would give the code in the form of a bar code similar to that used in marking merchandise in retail stores. With the aid of a light pen the viewer would simply scan the bar code, feeding the data into the remote-control unit. The latter, in turn, would feed the data to the memory of the microcomputer in the ZPS decoder. After that, the decoder would take over to watch for the proper code and to initiate recording.

The line in the vertical field-blanking interval has enough room for an additional 29 bytes of information. These, Blaupunkt says, could be used for clear-text information—for example, to give the actual title or name of a TV show. A miniature printer hooked to the receiver could then be made to print up a label that the viewer could use for marking the video tapes in the cassette library. **-John Gosch**

Belgium

Small fax unit switches between digital and analog modes as defined by CCITT

A desktop facsimile machine from MBLE SA of Brussels can send or receive one page every 3 minutes in CCITT's Group 2 analog mode or every minute in the Group 3 digital mode. It is probably the first and certainly the smallest facsimile unit to do both, say engineers at the Belgian affiliate of the Netherlands' Philips group.

Together with a Group 2 and a Group 3 machine, it is the start of the microprocessor-based P-FAX 2000 desktop series with which Philips has just entered the facsimile market [*Electronics*, Jan. 27, p. 67]. All three units meet the international standards established late last year by the International Consultative Committee for Telegraphy and Telephony.

High hopes. MBLE is aiming at the market held by Japanese and other producers in bulkier, stand-alone $30,000 machines. The P-FAX units will sell for $9,000 to $12,000 in small orders and for much less in the large orders that the company hopes will be placed by the Belgian and other national postal and telecommunications authorities.

Outside Europe, the machines have been demonstrated in Taiwan and South Korea, where oriental ideograms and characters limit the usefulness of typewriters and make facsimile machines very attractive.

The MBLE machine that can switch between Group 2 and Group 3 roles does so through an elaboration of its microprocessor's software. It should have a special appeal in the next few years, as the newer, digital mode gradually replaces the older, analog approach, says Marc De Block, division manager for telecommunications.

Handshake. When the interface with another facsimile machine begins, the unit will first attempt to establish a connection in the Group 3 mode. If the other unit does not respond to the questions in this first program, the machine will begin asking a second set of questions in order to establish a connection under the Group 2 mode. All of this takes 6 or 7 seconds.

Group 2 analog transmission, under CCITT standards [*Electronics*, Nov. 8, 1979, p. 85], enables the facsimile machine to read six lines a second. Group 3 digital transmission enables either 2,400 or 4,800 bits to be read a second. The digital interface, or handshake, is carried out by the units at a rate of 300 b/s.

The Group 2 mode uses duobinary

transmission, coding two input signal levels (say, 0 and 1) into three (−1, 0, and +1, for example) to halve bandwidth. But Group 3 is fully digital, generally using a microprocessor to control all synchronous modulation, demodulation, and equalization. The modem interfaces both with the facsimile machine's microprocessor when transmitting and with the analog-line access unit when receiving.

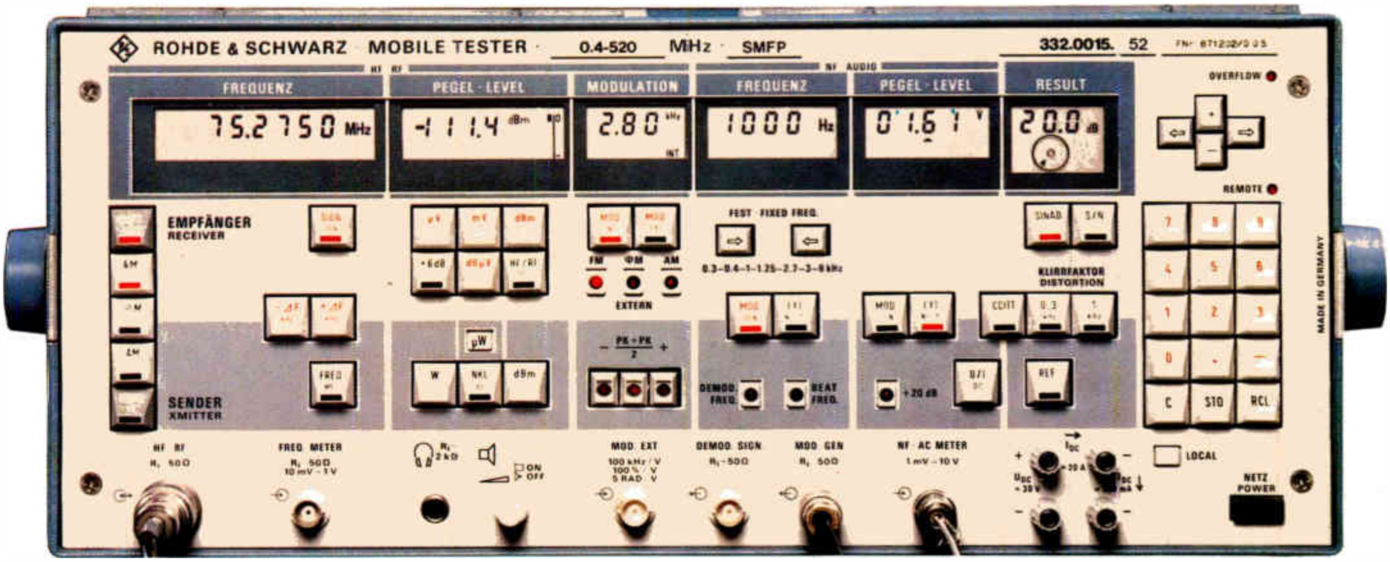
The 4,800- or 2,400-b/s modulation is based on phase modulation of a 1,800-hertz carrier. At 4,800 b/s, the data stream is divided into groups of 3 consecutive bits representing eight possible phase changes. At 2,400 b/s, groups of 2 bits represent four possible phase jumps. Whether the document is transmitted at 4,800 or 2,400 b/s depends on the quality of the telephone line, which is determined by the two communicating facsimile machines during the handshake.

The MBLE units print electrostatically on dielectrically coated paper. For the time being, they will scan documents using an integrated circuit with 1,728 photodiodes. The output signal from each scan of the 1,728 elements is a continuum of 1,728 charged pulses.

Switch to fiber. But in two years, when MBLE officials hope to be receiving 10,000 orders a year, a scanning system based on optical fibers will be adopted. The method employs a linear array of optical fibers at the full width of the paper. Unlike the current technique, it will not need bulky mirrors and lenses to reduce the page's image and will enable MBLE to reduce the size of the machines somewhat as well. They are currently 48 by 57 by 21 centimeters and weigh 28 kilograms.

An unusual feature of the Philips facsimile units are their ability to send or receive photographs, but only to each other, since other facsimile machines lack a compatible photo mode. By modulating the number of square dots it produces per square millimeter, the machine is capable of producing a pseudo gray scale. **-Douglas Glucroft, McGraw-Hill World News**

Testing transceivers in service and production



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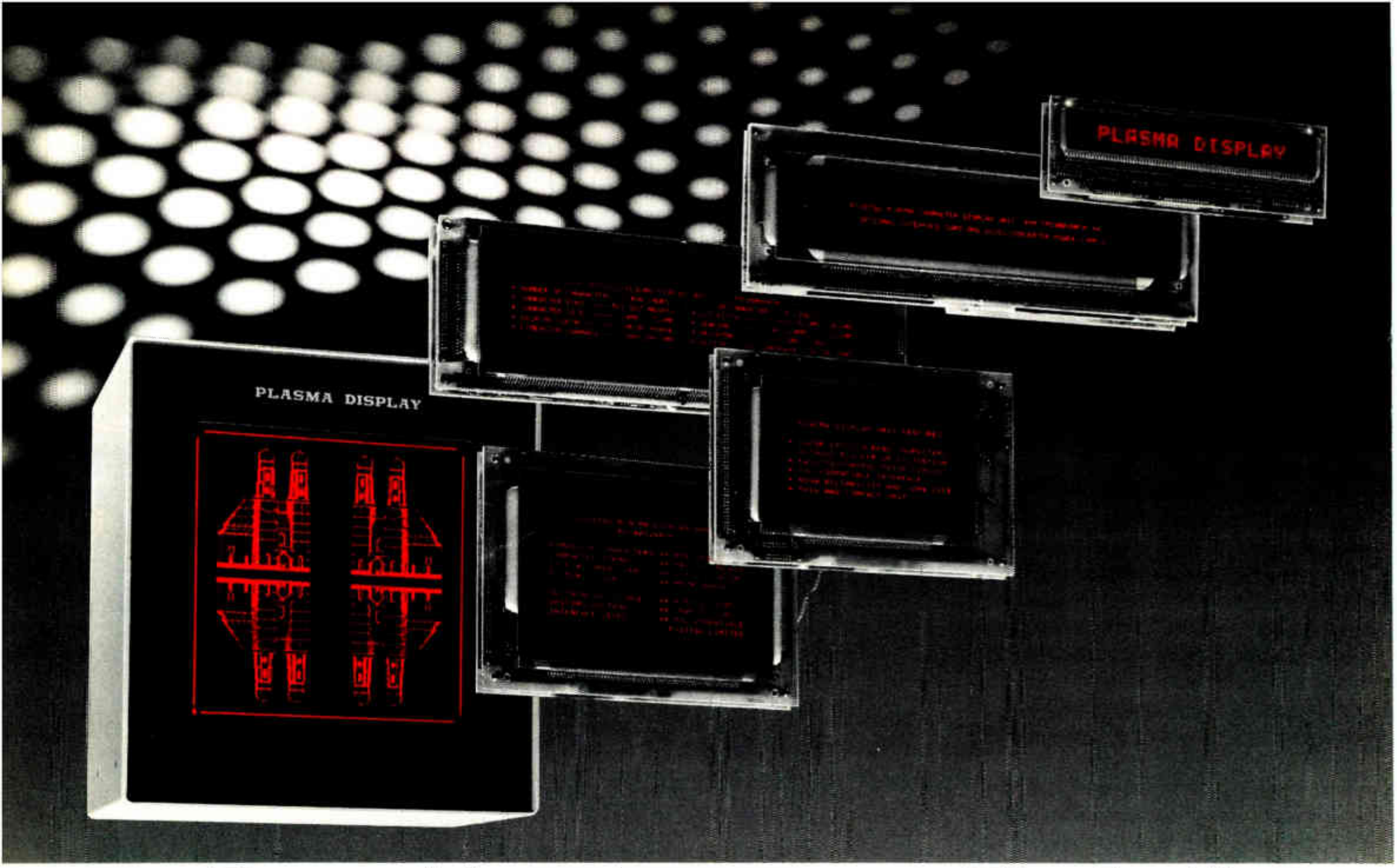

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FPC3201NRCK	32 (32 chars. x 1 row)		4.0 x 5.6	
FPC4002NRCK	80 (40 chars. x 2 rows)		3.1 x 4.4	
FPC3208NRCK	256 (32 chars. x 8 rows)		3.0 x 4.2	
FPC4012NRCK	480 (40 chars. x 12 rows)		3.0 x 4.2	
FPC8001NRCK	80 (80 chars. x 1 row)		3.0 x 4.2	
FPC8002NRCK	160 (80 chars. x 2 rows)		3.0 x 4.2	
FPC8006NRCK	480 (80 chars. x 6 rows)		3.0 x 4.2	
FPC8012NRCK	960 (80 chars. x 12 rows)		3.0 x 4.2	

* Also includes V_{sub} = −5V

GRAPHIC UNITS (For units with graphic generator control)

Model	Effective Display Area		No. of Effective Lines		Dot Pitch (mm)	Power Source
	D(mm)	W(mm)	D	W		
FPG0707NRUC	78	78	128	128	0.6	V_{CC} = +5V V_S = +80V ~ +110V V_W = +140V ~ +160V
FPG0805NRUA	18.6	153	32	256	0.6	
FPG0909HFUA	217	217	512	512	0.423	V_{CC} = +5V V_S = +85V ~ +105V V_W = −55V ~ −75V

Character and graphic color: neon orange

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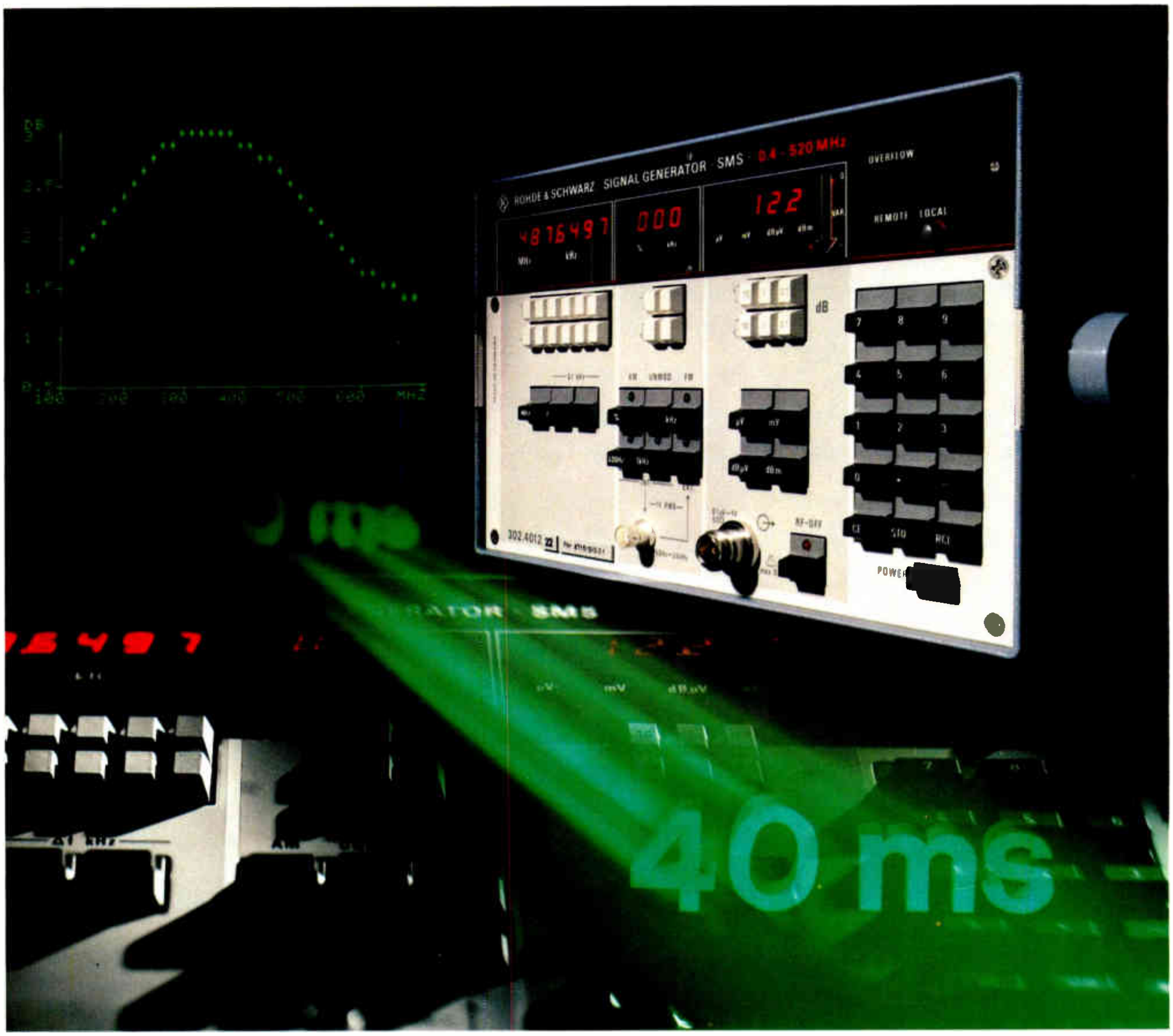

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Motor-control chip cuts times for power switching

by Kenneth Dreyfack, Paris bureau

Circuit monitors charge on power device's collector to prevent hard saturation and apply timely reverse current

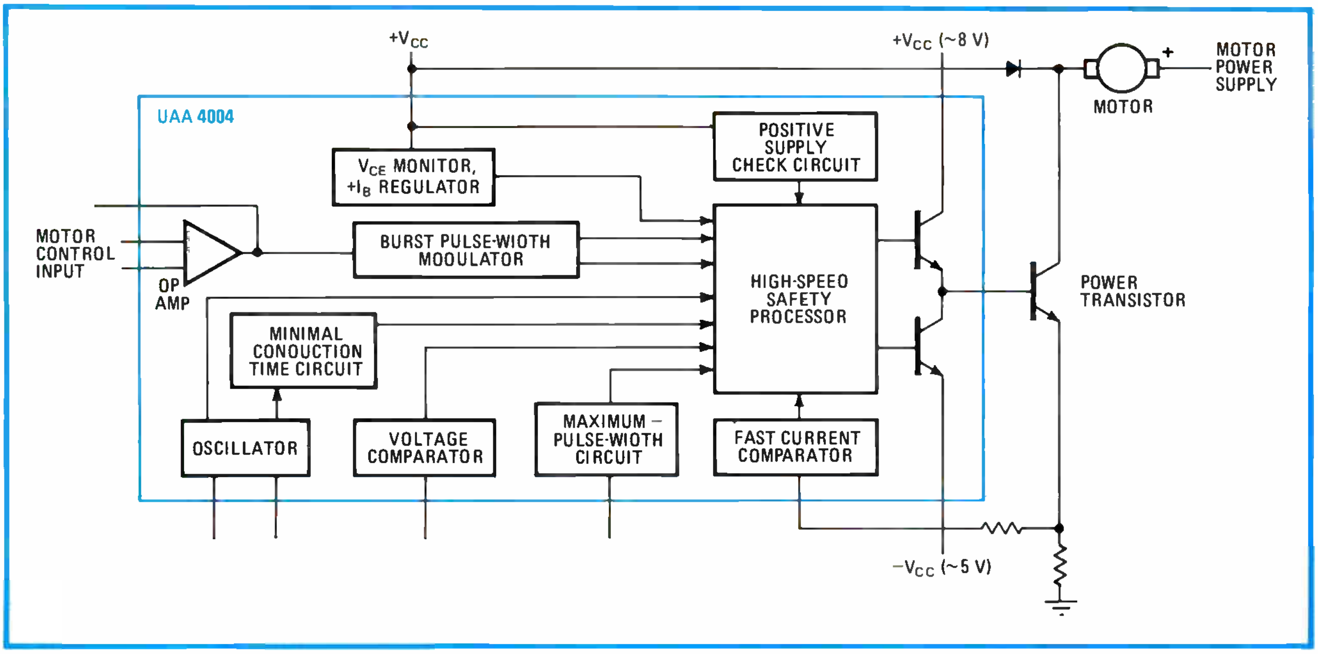
The Semiconductor division of Thomson-CSF is offering driving lessons for electric motorists. The company's bipolar switched-mode motor-control circuit, designed to control large appliance-sized motors like those in washing machines and machine tools, includes a self-optimizing driver to ensure efficient use of the power transistor.

Until now, driver circuits for switching-mode transistors and Darlingtons in the 100-W-to-100-kW range have been optimized for each application, explains Klaus Rischmueller, director of the Semiconductor division's power applications laboratory in Aix-en-Provence, France. What this means in practice is that for a given power transistor, say one rated at 400 V and 10 A, performance can range anywhere from 6 to 22 kW, depending on the efficiency of the driver circuit. Even with an efficient driver, switching time is rarely brought below about 0.8 μs. The switching time is the key factor for accurate control of the power transistor.

Thanks to the self-regulating, self-adjusting driver in the UAA 4004, designers no longer need worry about optimizing the driver for their particular application. Switching time can be cut by a factor of 10—in the example above, to 80 ns. "Yes," grins Rischmueller, "that is the switching time of a power MOS field-effect transistor."

Sensing saturation. The key to the circuit's adaptive operation is a system for monitoring the charge and thus the level of saturation of the driven power transistor's collector. The storage and fall times—the time it takes to drain the collector charge at turn-off so it can react to changes in the base current—largely determine switching speed.

The collector charge is monitored via a fast-recovery diode (see diagram). The base current can then be regulated by the 4004 so that the collector remains in a state of quasi-saturation; hard saturation, which



Fast driver. The UAA 4004 motor-control integrated circuit senses the collector charge and current drop of the power transistor it drives and thus is able to provide bias current to the base and timed reverse current that improve the power device's switching speed.

results in a relatively long storage time, is prevented.

But avoiding hard saturation is only half of Thomson's driving lesson. In order to ensure quick switching, relatively high reverse current—up to 3 A, depending on the power transistor being used—is applied to the collector. But it must not be applied until the collector saturation charge has already begun to decline, lest a minority-carrier charge extend the fall time.

Timed I_{REV}. To ensure that the reverse current is applied at just the right time, the driver circuit monitors the current drop between the power transistor's emitter and collector. Because of collector charge resistance, the collector-emitter voltage (V_{CE}) rises as the collector current decreases.

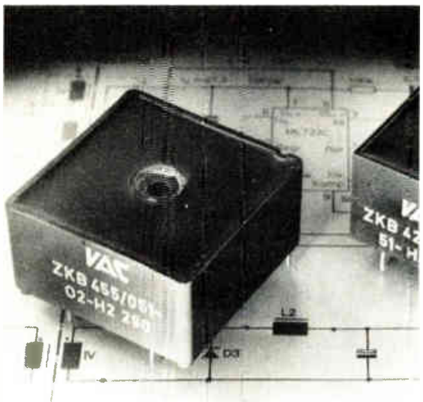
For example, the collector-emitter voltage might read about 0.7 V before turn-off but would immediately start to rise at the turn-off moment. When the voltage increases to 4 V, the collector saturation level is low enough to permit applying the reverse current without a minority carrier charge. The result is a dramatic drop in storage time—typically from 3 down to 1.5 μs.

The 4004 includes circuit elements normally found in chopper circuits for switching-mode motor control. An oscillator, programmed by an outboard RC circuit, can operate at from 100 Hz up to 50 kHz. A pulse-width modulator is also included, as is an operational amplifier. Normally supplying open-loop gain, the on-chip op amp can also be used as a voltage follower with unity gain.

Minimal-conduction-time and maximum-pulse-width circuits ensure complete discharge of all inductance in the motor drive circuit after each switching operation. A fast current comparator responds in less than 1 μs to ensure protection against base-current overloads.

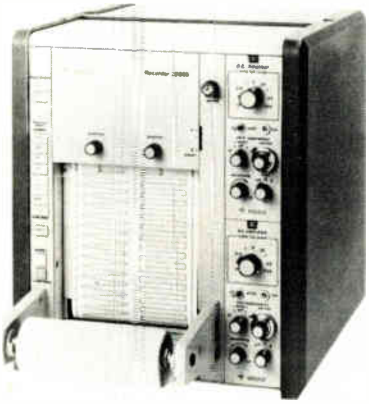
The UAA 4004, in a 16-pin dual in-line package, is available throughout Europe in sample quantities. The price is about $5 in lots of 100.

Thomson-CSF, Semiconductor Division, 50 Rue Jean-Pierre Timbaud, B. P. 5, 92403 Courbevoie, France [441]

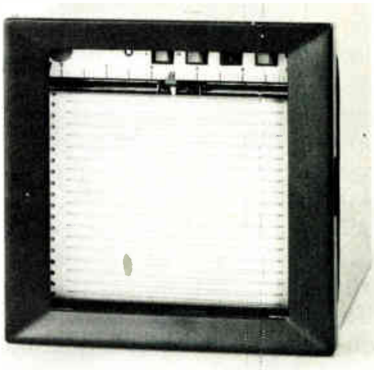


Compared with its predecessors, the ZKB choke for control circuits and switched-mode power supplies is 50% lighter. It is only 3.2 by 3.2 cm, with current ratings of from 4 to 16 A and inductance values of 1,000 to 60 μH. VAC GmbH, 6450 Hanau, P. O. Box 2253, West Germany [442]

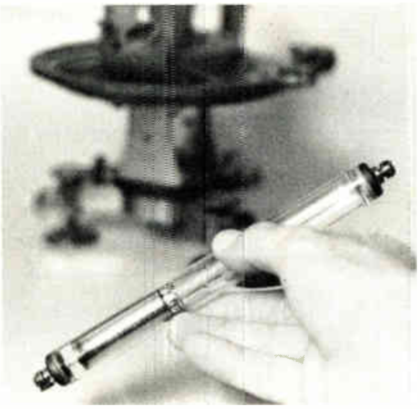
CP1600 and 1700 potentiometers can handle a large wiper current thanks to a specially designed element and wiper that combine to reduce the risk of damage during field service and testing. Their resistance range is 1 to 10 kΩ. Colvern Ltd., Spring Gardens, Romford, Essex RM7 9LP, England [445]



The Gould 2200S direct-writing recorder's chart paper is driven by a line-frequency-independent stepper motor system that increments by approximately 80.2 steps per mm. Gould Instruments Division, Roebuck Road, Hainault, Essex 1G6 3UE, England [443]



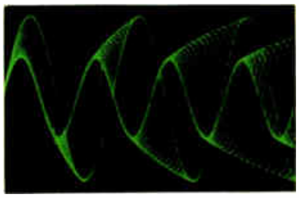
Model 8A41 is a miniature servo recorder that uses a single thermal pen to write on a black-trace, heat-sensitive recording paper that is driven by a quartz-controlled stepping motor mechanism. San-Ei Instruments Co., 1-12-1 Okubo, Shinjuku-ku, Tokyo 160, Japan [446]



The LGR 7632 laser tube is only 209 mm long and 19 mm wide and is thus suitable for portable, battery-operated equipment. With an output of 1.5 mW and an operating current of 3.5 mA, only a small power supply unit is required. Siemens AG, 8000 Munich 1, P. O. Box 103, West Germany [444]

The PM 2528 multimeter measures dc and true root-mean-square ac voltages, dc and ac currents, two- and four-wire resistance, and temperature. NV Philips Gloeilampenfabrieken, Science and Industry Division, P. O. Box 523, 5600 AM Eindhoven, The Netherlands [447]

Modulation Analyzer FAM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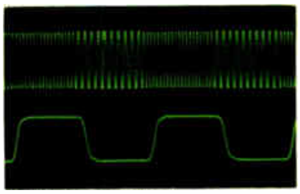
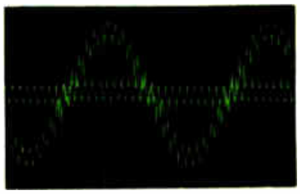

FSK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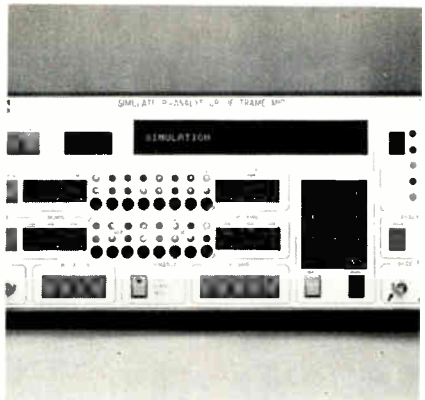
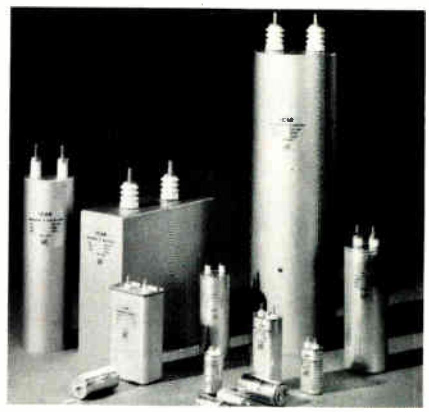
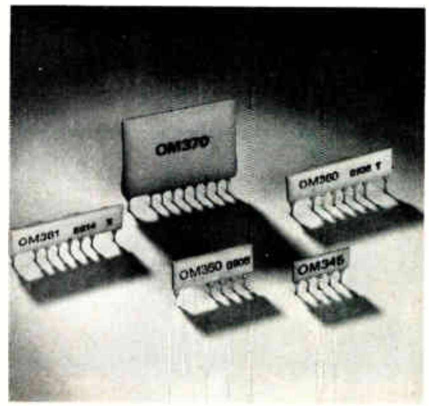


The TE 820 is a microprocessor-based simulation and analysis test set for frame-structured pulse-code-modulated serial data at 2,048 kb/s. It can be controlled remotely via an IEEE-488 bus. Tekelec-Airtronic SA, Cité des Bruyères, Rue Carle Vernet, B. P. N 2, 92310 Sèvres, France [448]



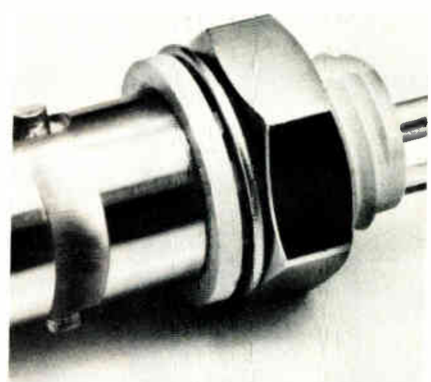
The Bioenergy series of capacitors have been designed for power electronic equipment. They are intended for use at high frequencies and high peak currents. Industria Condensatori Applicazioni Elettroelettroniche SpA, Via Felice Casati, 44 20124 Milan, Italy [450]

Philips' PM 3264 is a portable four-channel 100-MHz oscilloscope designed to cut digital measuring times. It features a dual time base, a 17-kV display tube, an 8-by-10-cm screen, and state-of-the-art circuitry. Pye Unicam Ltd., York Street, Cambridge CB1 2PX, England [449]



A family of 12-V very high-frequency and ultrahigh-frequency wideband amplifiers includes the OM345 single-stage amplifier and the OM370 three-stage amplifier. NV Philips Gloeilampenfabrieken, Elcoma Division, P. O. Box 523, 5600 AM Eindhoven, The Netherlands [454]

Model H402A Hotmarker, for tube and wire identification, has an input voltage of 100 V, 100 W maximum. On the front panel are a marking timer, a temperature controller, a digital counter, and a foot-pedal connector. Chuo Tsusho Kaisha Ltd., 1-6 Kanda Izumicho, Chiyoda-ku, Tokyo 101, Japan [451]



The Greenpar 35246BN insulated connector, designed for use in the computing, video, and office machinery fields, features an integrally molded mounting thread and a flame-retardant molding material. Greenpar Connectors Ltd., P. O. Box 15, Station Works, Harlow, Essex CM20 2ER, England [453]

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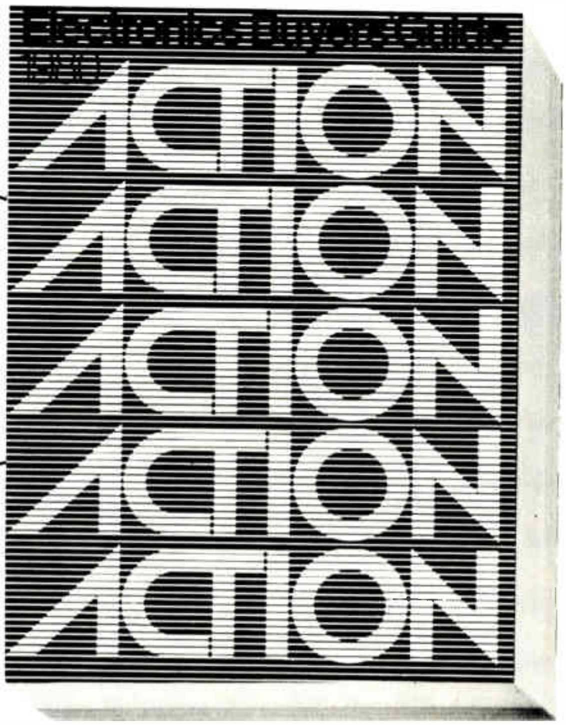

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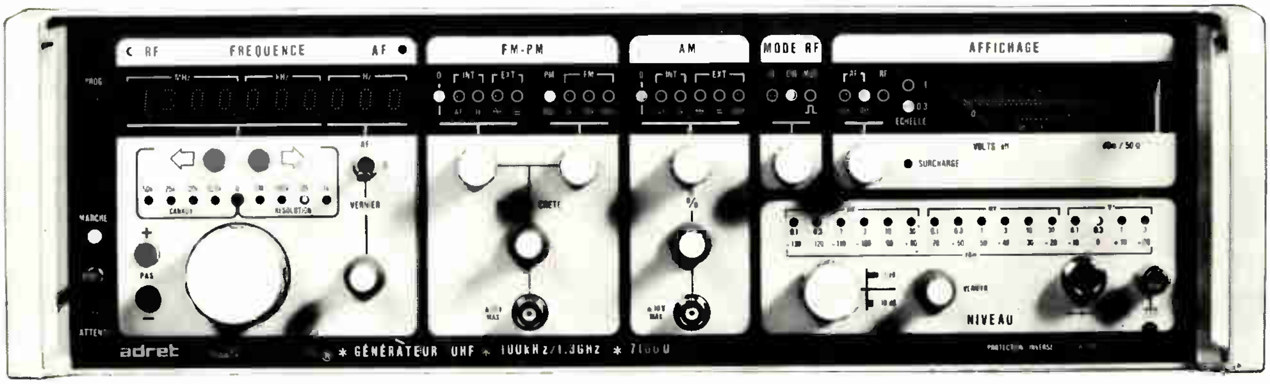

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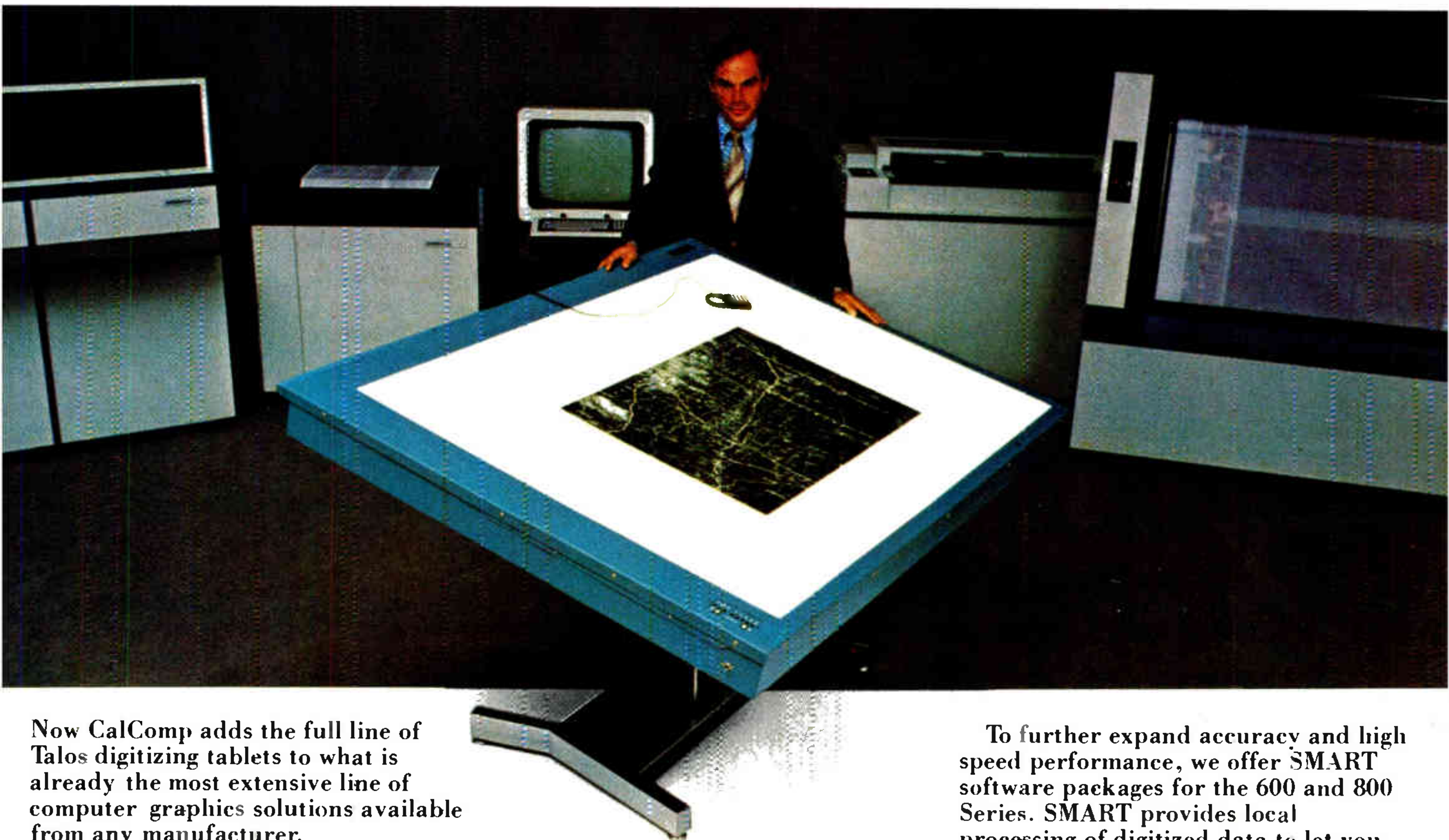

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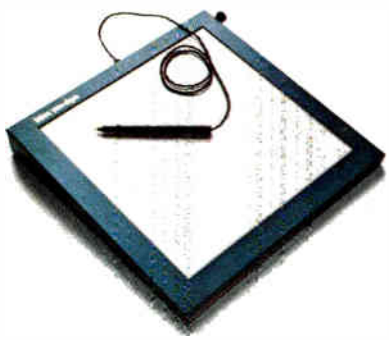

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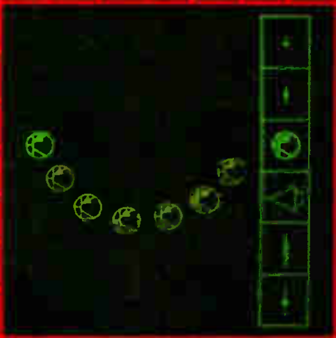

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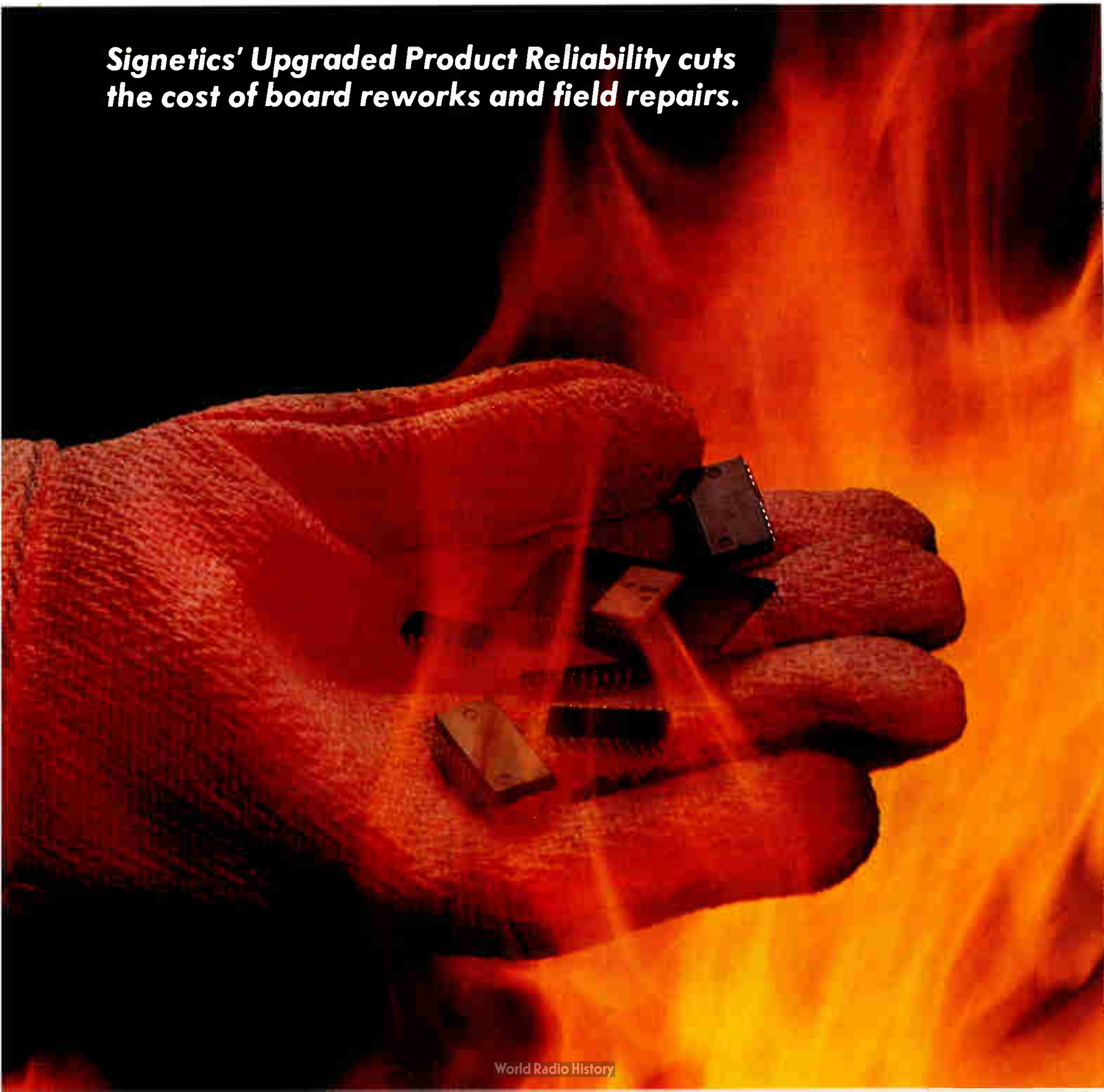

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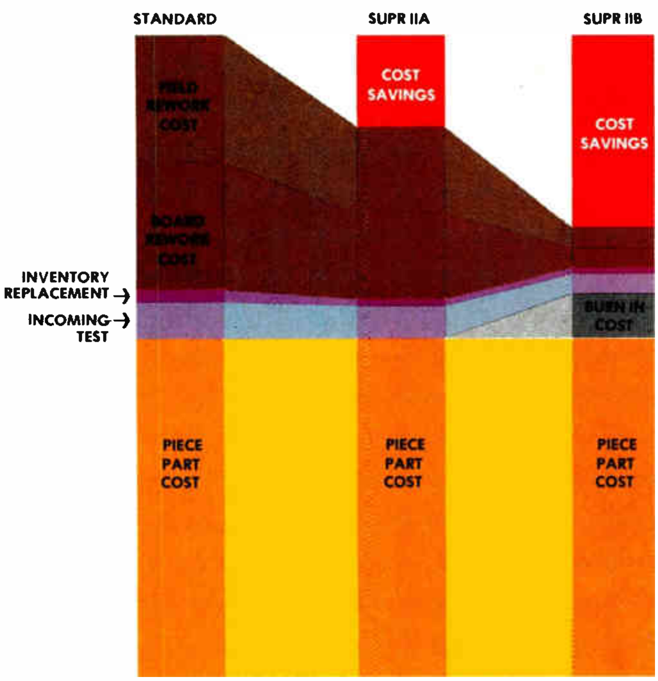

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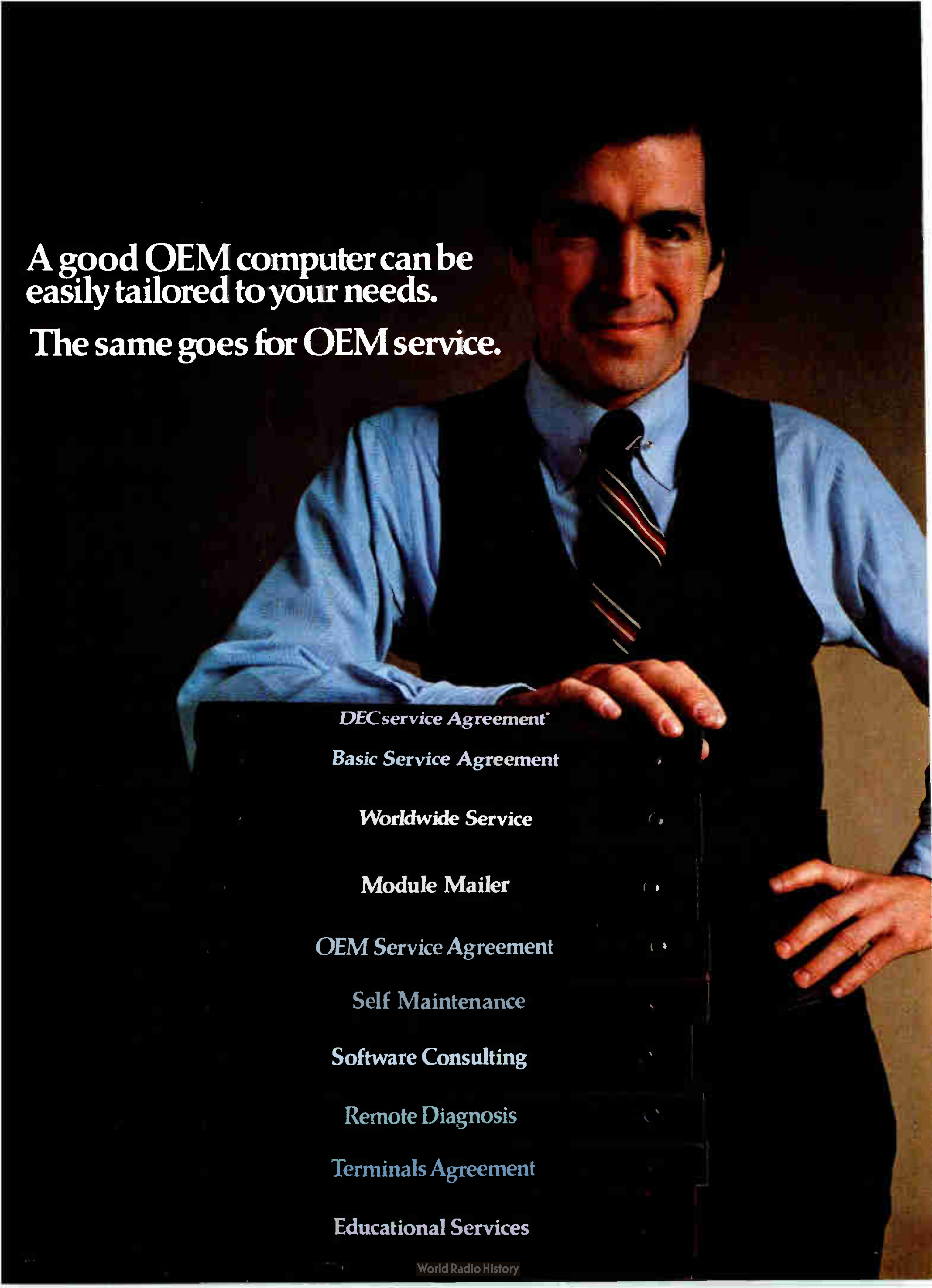
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Is epitaxy right for MOS?

TI thinks epitaxial layer for 64-K dynamic RAM is worth added cost; Bell Labs agrees, and other manufacturers eye the move

by John G. Posa, Solid State Editor

Most MOS devices are built on single-crystal silicon substrates, but now Texas Instruments Inc. is taking the lead in using an epitaxial layer for its 64-K random-access memory. This decision is controversial because epitaxy inflates the cost of each die somewhat, and it is becoming painfully obvious that the 64-K RAM is the most cost-sensitive solid-state device yet produced.

Nevertheless, Western Electric also is building a 64-K RAM, designed by Bell Laboratories, on epitaxial material; and Mitsubishi has published papers intimating that it may build future RAMs the same way. Other makers of MOS chips are weighing the switch. Indeed, a technology manager at Intel Corp. predicts that "one day all MOS circuits will be built on epi" and TI's MOS memory development manager, Richard Gossen, calls the move "the most important departure in the evolution of the dynamic RAM since the 1-T [single-transistor] cell."

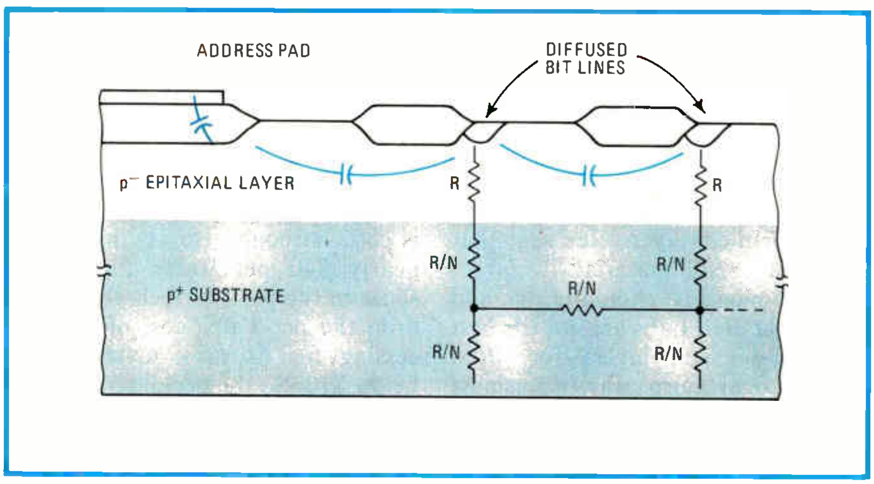
Why would high-volume memory manufacturers switch to a more expensive process? The answer: better-quality parts with less noise. With a high-resistance epitaxial layer, the substrate can be heavily doped and hence made highly conductive; the heavy concentration of acceptor ions limits the lifetime of the minority carriers—electrons, in this case, in both the starting material and the epi layer are p-type—dramatically reducing leakage currents to and from memory circuits.

In other words, superfluous electrons, which can be created by input-signal spikes, alpha particles, and other mechanisms, are not allowed to travel far to flip storage nodes or upset bit lines and foul up sensing. The resulting part is less sensitive to input test patterns and alpha particles and better able to meet long refreshing requirements. Producers of complementary-MOS memories are also investigating the use of epitaxial silicon as a cure for latch-up.

All 16-K RAMs exhibit some problems due to long minority-carrier lifetime in the substrate, with symptoms that become acute when the column-address strobe, $\overline{\text{CAS}}$, is allowed to fall about 40 nanoseconds after the row-address strobe, or $\overline{\text{RAS}}$, was lowered. Although the timing is within specification, it is during this period that sense amplifiers in the chip are latching data. So, when the addresses are strobed in, the pads on the die capacitatively bump the substrate, creating noise spikes that can unbalance bit lines. This effect, sometimes called address-pad bumping, can cause a memory to fail, especially at low supply voltages.

As for a more robust refresh, an epi layer "reduces substrate leakage, which is the key ingredient of holding-time degradation," according to Bruce Darnall, director of Bell Laboratories' MOS Technology and Memory lab in Allentown, Pa. TI's 64-K RAM, for instance, features a 4-millisecond refreshing requirement, which is twice as long as that for most other 64-K chips. More impressive, some of the Dallas company's parts will store data as long as 128 ms before leakage takes its toll.

More leakage. All commercial 64-K dynamic RAMs have on-chip negative-bias-voltage generators that pull the substrate down to about −2 to −3 volts. The biasing keeps the junctions between diffused n-type regions and the substrate in a stable, reverse-biased state, even with negative overshoots on input pins, because forward biasing will inject minority carriers. However, the increased overall voltage differential also widens the depletion regions



Noise sink. The highly conductive substrate allowed by a lightly doped epitaxial layer serves to dampen input noise spikes. The resistivity difference, N, is greater than 100.

sandwiching the junctions, thereby uncovering more generation-recombination centers—or G-R centers, as they are called—which contribute to leakage.

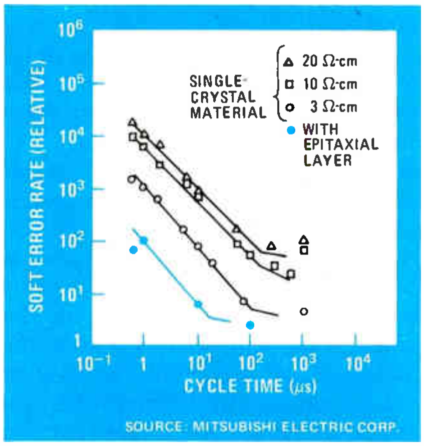
Some concern. Before TI announced its use of an epi layer, it disclosed that the substrates in its 64-K RAMs are grounded—that is, they are at zero potential. Grounding raises several concerns, to say the least, about the part's ability to cope with minority-carrier injection. Gossen admits that the epitaxial layer was added a full year after the device was introduced way back in the fall of 1978 [*Electronics*, Sept. 28, 1978, p. 109].

TI's initial 64-K RAM simulations assumed a stable threshold voltage, but fabricated chips proved that assumption unfortunate. As demanding as epitaxy is, "we concluded that going to a substrate supply generator is a difficult and tricky thing to do," Gossen says. Adds G. R. Mohan Rao, TI's manager for dynamic RAMs, "By September of 1979 we saw a clear distinction in favor of epi." Now the officials believe that the rest of the pack will be drawn to epitaxy with higher-density chips like the 256-K RAM.

A cross section of TI's 64-K RAM is shown in the figure on page 93. Although nowadays bipolar wafers invariably include epitaxial layers, substrate and epitaxial polarities do not usually match; that is, an n-type layer might be put on a p substrate. As mentioned, at least for n-channel MOS chips, the epitaxial layer has the same polarity as the substrate, but resistivity changes significantly from the bottom to the top of the wafer. In TI's wafers, resistivity changes by several orders of magnitude, from a highly conductive substrate to an epi-layer value near that for single-crystal material.

Some pioneers. Actually, TI and others like Bell Labs are not the first to suggest such layers for MOS. When Cogar Corp. was in business in the late 1960s, it brought out a line of MOS memories built with epi, but it soon ran into significant yield problems. Fairchild Camera & Instrument Corp. also experimented with such layers to protect MOS devices against electrostatic charge. More recent was American Microsystems Inc.'s V-groove MOS, which employed an intrinsic epitaxial layer as part of a vertical channel. But that technology, too, fell by the wayside for memory applications because of production problems indirectly related to the layer [*Electronics*, Dec. 20, 1979, p. 40].

TI is sure its epitaxial process will succeed where others have failed. Besides being of the same polarity as the substrate, the layer is relatively thick—about 10 micrometers—and does not determine any critical device parameters like gain. In contrast, AMI's layer was only 2 to 3 μm thick, which left it more prone to shorting spikes. In addition, TI does a lot of bipolar processing, so that it is familiar with epitaxial growth.



Alpha barrier? An epitaxial layer may help to prevent alpha radiation, but probably not when it arrives on a slight angle.

"Most of TI's bipolar lines have the epi reactor right at the front end," says Gossen. Although the particulars of its 64-K RAM's epi process are still proprietary, Gossen hints that "it could be done in a standard reactor."

But, as mentioned, the bottom line is cost. Although epitaxy has added nearly $40 per wafer for bipolar slices in the past, TI feels that it can drop the per-wafer cost of epi processing for its 64-K RAM to well below $10. So the per-die increment, as usual, depends on yield. As Bell Labs' Darnall puts it, "If it costs $10 per wafer and you're only getting 10 chips per wafer, you're incurring a considerable expense."

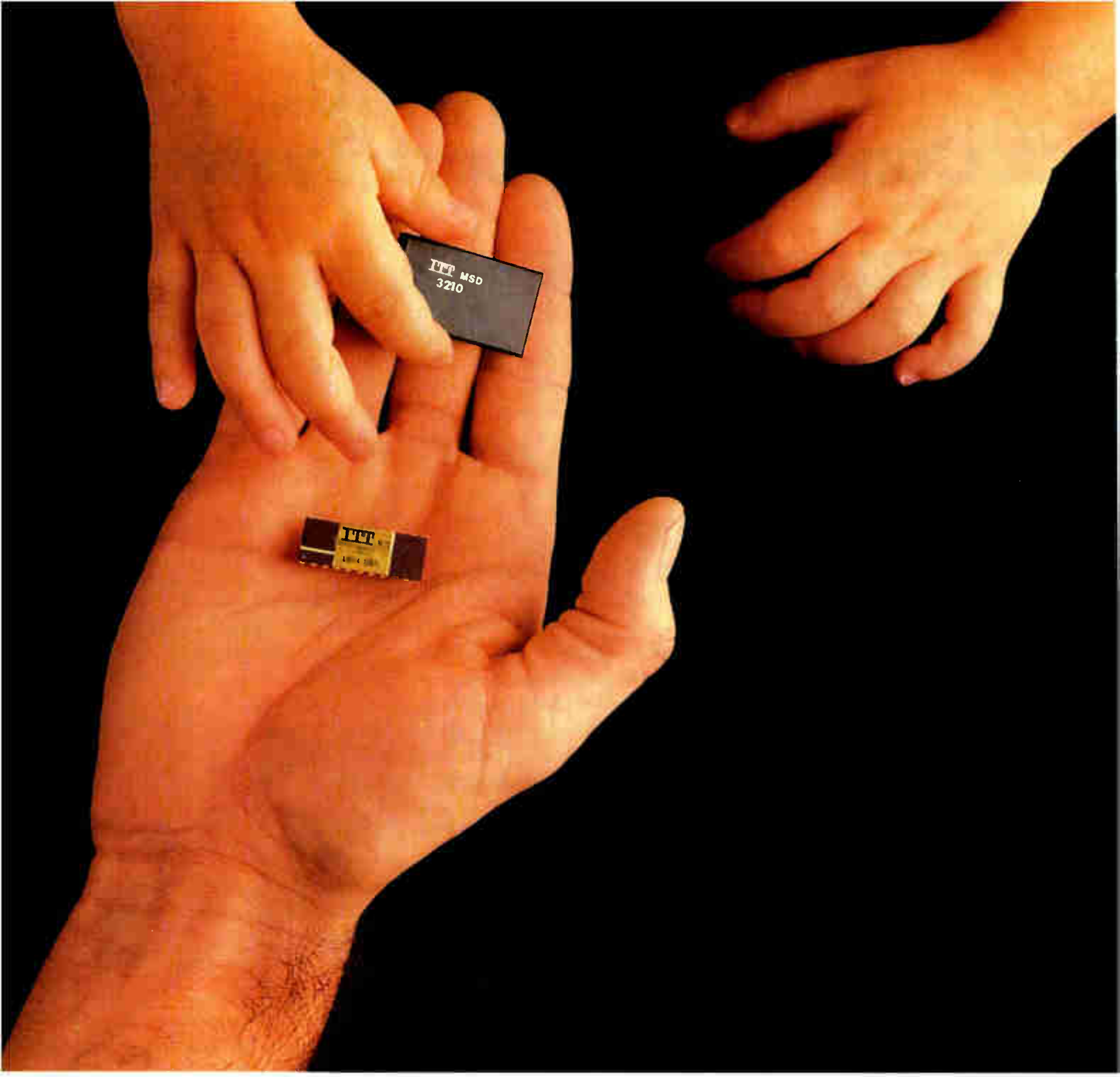
But TI must be doing better than that, since Gossen avers that "We're at a cost advantage right now. We will compete in 1981." He points out that the epitaxy adds nothing to the firm's already very small, 33,000-square-mil die and that the cost of the epi processing translates into an effective die area "in the mid-40s" for a chip with comparable performance and reliability but without the layer.

Besides, the dynamic RAM competition is buying immunity to external noise in other ways—for example, with larger, more forgiving cells and dice. Other companies are adding a mask step or ion implants to the storage capacitor to bolster its ability to keep charge. Finally, practically all producers have had to coat their chips with polyimide liquid or tapes to help fight off alpha radiation.

Handy. In addition to resisting external noise, the layer helps out in other ways. Heavy metal ions get snagged in the distorted lattice that surrounds the epi-to-substrate interface. These kinds of impurities tend to degrade high-temperature operation. But TI's layer, relatively free of such particles, supports proper memory operation at well past 70°C. Also, the now highly conductive substrate makes a much better ohmic contact when it is mounted.

The claim that the epitaxial layer reduces the sensitivity to alpha radiation is itself controversial. Mitsubishi Electric Corp. states that soft error rates with epi material can be 10 to 100 times smaller than with uniformly doped substrates exhibiting resistivities of 3 to 20 Ω-cm (see diagram). However, if the alpha particles come in on a slight angle—which is usually the case—instead of straight down, the epi-to-substrate interface may actually be a detriment, reflecting generated carriers back at the storage nodes.

"I wouldn't argue that it's a panacea to alpha sensitivity," says Bell Labs' Darnall. In fact, "I wouldn't conclude that they [the epitaxial layers] will become pervasive in the industry," he surmises, because so many are concerned about the added cost. "It depends on your sensitivity to reliability. It's not expensive, and it's money well spent." □



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Information processing

Small Winchesters rolling in volume

Mass-storage systems, in 8- and 5.25-inch versions, prepare to fulfill promise after year's delay

by Larry Waller, Los Angeles bureau manager

Finally, by most accounts many months late, significant numbers of perhaps the most heavily promoted computer peripheral device yet are starting to come down the production pike. It is the small Winchester fixed-medium (hard) disk drive, mostly in the 8-inch-diameter but also in a 5.25-in. version, issuing from a list of both established and newly formed suppliers that seems to grow each week.

Taking an early lead last year, when sources say only about 24,000 small Winchester drives were shipped to the noncaptive market for these mass-storage systems, were volume leader Shugart Associates (a Xerox Corp. subsidiary), with some 15,000 units, and International Memories Inc., both of Sunnyvale, Calif. (IMI, in fact, announced the first 8-in. Winchester drive in 1978 after IBM Corp. pioneered with its model 2230 in 1973. But the Sunnyvale firm could not even deliver samples until a year later.)

Benefits. In the meantime, however, the interest of eager suppliers as well as original-equipment manufacturers kept growing due to the marked advantages of the small drives. Overall, they fit well into small-computer systems: they are the same size as floppy disks, their capacity is from 5 to the recently announced 136 megabytes, and they cost as little as $1,000 or less for low-performance models.

Such high mutual interest caused users to clamor for quick deliveries and manufacturers to strain to keep to promised schedules—a situation that began in late 1979 and then stretched into late 1980. But ticklish design, vendor, and production problems combined to cause frustrating delays and mounting costs, so much so that some supporters began to examine alternatives. But just in time, midway in the year many of the bottlenecks were apparently removed—with crash programs in many cases, major participants indicate—and prospects are again high.

A typical experience is reported by Micropolis Corp. of Chatsworth, Calif., whose founder and president Stuart P. Mabon enjoys an industry reputation for candor. "All of us had the same troubles," says Mabon. He points out that these were made all the worse because they came along when development programs were several years old and supposedly nearly complete.

The basic difficulty in squeezing traditional 14-in. Winchester technology down to an 8-in. diameter is that tolerances have to be much tighter to get the dramatic increases in bit density. One example is read/write heads that must track the disk surface more closely, at a height of about 19 microinches, less than the height of most contaminants. Also, head load pressure is reduced to only about 10 grams from 350 g in traditional drives.

Squeaky clean. Not only were environmentally sealed enclosures to prevent contamination required, but superstringent clean-room assembly, something new to most disk manufacturers, was also needed. And most firms underestimated the difficulty and time needed to get vendors up to speed in supplying more advanced components, including heads, positioning systems, and even improved disk media themselves.

Add to this startup costs. These are estimated at a minimum $2 million to $3 million to design and produce the drive in an existing clean-room facility and upwards of $5 mil-

CATEGORIES OF SMALL WINCHESTER DRIVES

	8-inch very-high performance	8-in. high-performance	8-in. low-performance	5.25 in.
Typical capacities (megabytes)	40 and up	12–40	5–20	3–12
Positioning systems	closed loop (binary actuation)	closed loop (servo)	open loop (stepper-driven)	open loop (stepper-driven)
Interface	storage-module—driven; bus-oriented; ANSI*	storage-module—driven; bus-oriented; ANSI*	floppy disk	floppy disk
Approximate price (in large volume)	$3,000 and up	$2,000	$1,000 to $2,000	$1,000 and less
Available in volume	late 1981	early 1981	late 1980	late 1980

*Proposed ANSI X379.3/143 Rev. 5 interface standard lion for an entirely fresh start. Laying out those sums, among others, are Priam, San Jose, Calif., which is adding an 8-in. model 3450 35-megabyte drive to its Winchester line, and Quantum Corp., in the same city, which is adding a 40-megabyte member to its smaller versions introduced in November. In the Midwest, Irwin International Inc. of Ann Arbor, Mich., came up with $2 million when it decided a year ago to add a 5.25-in. version.

But Mabon and others downplay the technology problems themselves. "What took us, the industry, by surprise was something else: it is a management—not an engineering—problem." Mabon explains that the usual approach is to assign a design engineer and enough support people to a development project to push it successfully through, but by early 1980 this was not working. "It's a tough problem; that is, a complex of technologies that needs a multidisciplinary approach," says Mabon.

Several roads. Once management orientation was changed to attack development in multidiscipline fashion, the barriers fell rapidly. However, though many of Mabon's disk drive counterparts agree generally with his analysis, some point out that firms addressing the small-Winchester business with a 14-in. Winchester background generally had a smoother ride than floppy-disk companies jumping into drives for the first time.

Control Data Corp., for one, considered by some the major supplier of rigid disk drives, says production of its new Lark CDC9455, a combined fixed-and-removable disk unit, is only a few months behind schedule and has encountered no unseen problems. A spokesman at Fujitsu America Inc., Santa Clara, Calif., also points out that many delays in early production of Winchester drives were experienced by companies that entered the market as startups. Fujitsu has been making drives for 15 years.

In any event, makers of small Winchesters look for clear sailing through 1981. Already much clearer now are the niches being filled by Winchester disks, with the lines increasingly well-defined between high-performance models, as replacements for 14-in. drives, and low-end models, displacing floppy disks. The low side is where competition likely will heat up first, as 5.25-in. drives make inroads into the 8-in. drive market.

Industry consultant Dataquest Inc. predicts sales of 146,800 units for North America in 1981. This includes both those made by independents and by captive heavyweights like IBM and Control Data for their own systems. The comparable figure for 1980 was about 61,500, with captives taking some 38,000, says James Moore, manager of disk market research for the Cupertino, Calif., firm.

Micropolis already has grabbed off what might be the biggest Winchester drive contract yet, a three-year deal worth $20 million with Britain's International Computers Ltd. for deliveries of about 100 units per month of the Microdisk, with up to a 35-megabyte capacity, until spring, when the rate is slated to jump. And Seagate Technology Inc. of Scotts Valley, Calif., has just licensed Texas Instruments Inc. in the U. S. and CII-Honeywell Bull in the rest of the world to make and market its micro-Winchester drive.

A likely early tipoff to the competitive scuffling ahead for small Winchester drives is the model 510 5.25-in. micro-Winchester disk announced in September by Irwin International. It is loaded with a number of features so far found only on high-performance 8-in. units: voice coil actuation and a closed-loop servo system for head positioning instead of stepper motors and a 25-millisecond average access time. Furthermore, it has an integrated 0.5-in. cartridge tape for backup and 10-megabyte single-platter formatted capacity, all for $1,500 in OEM quantities. Volume shipments are planned for later in the year, but the firm admits it has not yet actually manufactured in large quantities. □

Bull's-eye

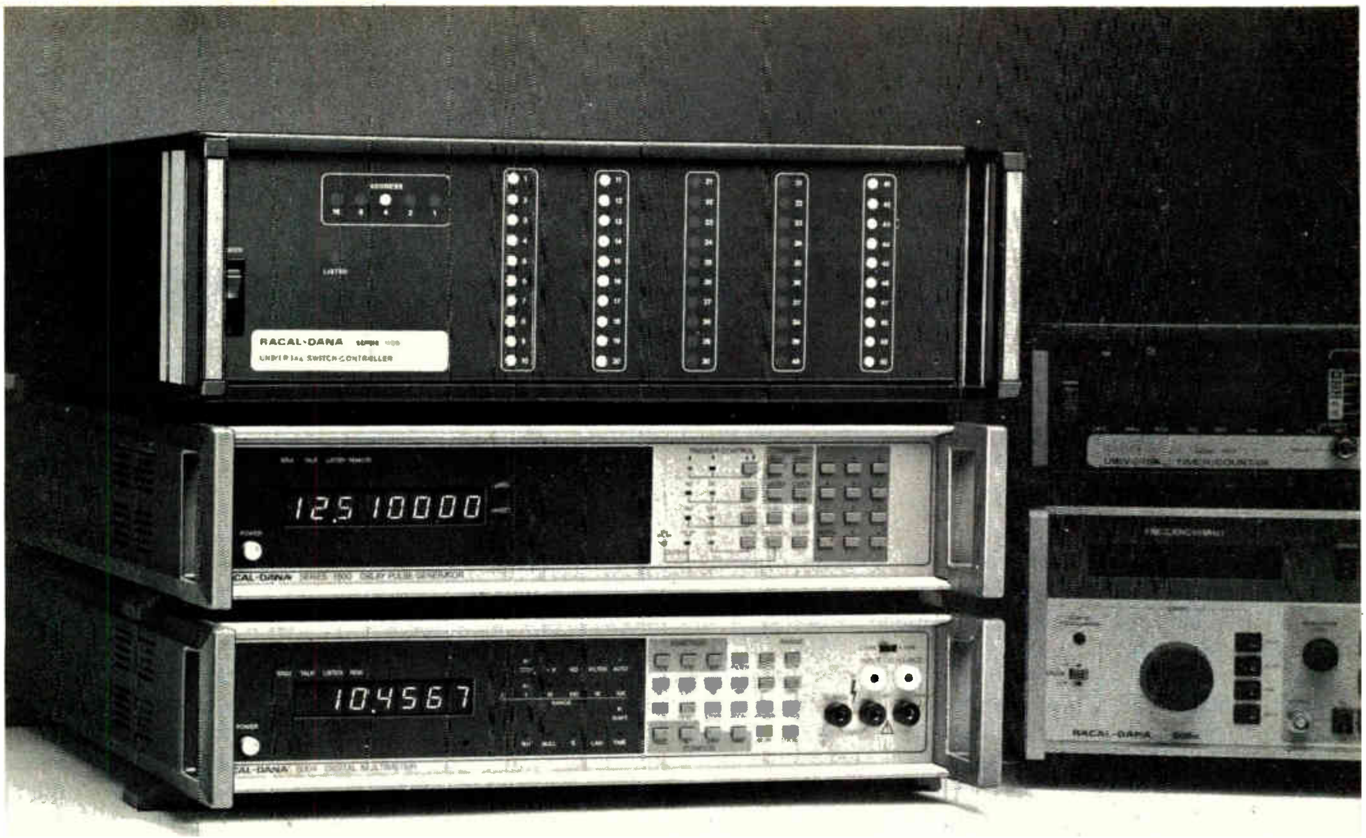
The Winchester nickname for rigid drives comes, as does much of the technology, from the trailblazing International Business Machines Corp., which in 1973 brought out its model 3340. It was a dual drive with planned twin storage capacity of 30 megabytes each. The 30-30 configuration reminded some of the famous rifle; though IBM soon upped the capacity to 35 and then to 70 megabytes, the name stuck. **-L. W.**

Streaming-tape drives also run into problems

Much like the Winchester disk drives they are designed to back up, streaming-tape drives were loudly trumpeted but mostly failed to materialize during 1980. Volume shipments are planned for 1981, but the impact on systems is not expected until 1982. Typical are two San Diego firms, Data Electronics Inc. and Cipher Data Products Inc., that now offer evaluation units. They and most companies with announced products expect to reach the 1,000-drive-per-month level this year. Problems that delayed the drives vary, as with most startups, ranging from head design to interface decisions.

Once production starts, the importance of streamers will not be realized until problems of integration into systems are overcome. A typical difficulty is that to fully utilize the top speeds of 90 to 100 inches per second offered by most of them, a buffer must be added to avoid starting and stopping. Furthermore, a lack of streamers last year forced original-equipment manufacturers to use floppy disks and start/stop drives, creating inroads into the backup market that will remain for some time, according to Sam Thompson, marketing vice president for Data Electronics.

Also, looming competition between half-inch and cartridge drives may create yet another backup question. Most cartridge units have focused on capacities below 30 megabytes, with half-inch devices taking the higher end. But 3M's 67-megabyte cartridge and a 25-megabyte half-inch drive with a relatively slow speed of 30 inches per second, recently introduced by Data General Corp., portend infighting. **-Terry Costlow**



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Computer-aided design

CHAS seeks title of global CAD system

Originally meant for very large-scale integrated circuits, it also handles data bases and enfolds other computer-aided design tools

by James B. Brinton, Boston bureau manager

A possible prototype for the global computer-aided design systems of the 1980s has emerged, not from the semiconductor industry or academe, but from an end user. The new system, labeled the Chip Assembler, comes from Digital Equipment Corp.'s Hudson, Mass., semiconductor facility; its eventual role will be to speed the design of very large-scale integrated circuits for DEC's future products.

Called CHAS by its developers in DEC's VLSI Advanced Development group, the system is variously described as an approach to structured very large-scale integration design; as an umbrellalike, multiuser design aid that enfolds other CAD tools; and sometimes simply as a large, interactive data-base management system. All of these definitions are correct, but not even all three tell the whole story, according to J. Craig Mudge, who was manager and technical director of the group. He has since returned to his native Australia to head the nation's VLSI effort.

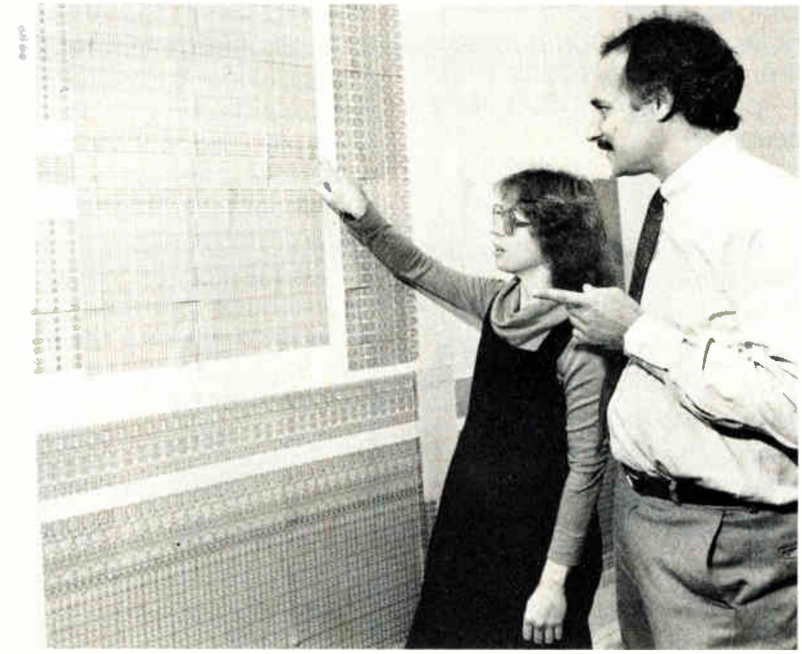
CHAS is as much philosophy as hard- and soft-ware; Mudge and his associates believe in a rigorous design approach and CHAS helps fulfill this. And unlike most other approaches, it tends toward synthesis, drawing on a wide variety of CAD tools. Indeed, it is capable of using almost any digitized input.

Mudge says that, to a degree, the philosophy behind CHAS draws on and extends the approach developed by Carver Mead of Xerox Corp. of the California Institute of Technology the bristle-blocks approach of David Johannson, also of Caltech; and Caltech's silicon structures program. It also takes a page from the Massachusetts Institute of Technology's CAD effort.

CHAS umbrella. According to Carol Peters, DEC's principal software engineer and CHAS project leader, a partial list of the CAD tools now in the prototype Chip Assembler would include: MIT's Mossim logic simulator; the subscriber line interface circuit simulator; a design-rule checker; a pattern generator; translational routines for getting data into and out of Calma equipment; a programmable logic array generator; the Smash mask-generation aid; and a large number of home-grown tools.

A variant of the Caltech Intermediate Form, or CIF, machine-readable language is used as CHAS's internal data format, simplifying the addition of new CAD tools. Such additions have been stumbling blocks to earlier attempts at integrated CAD systems, according to academic sources.

But using the CIF variant, says Peters, it took only about a week to add Mossim and a commercially available design-rule checker. "Additions can take place rapidly," says Peters, "if the data formats of CHAS and the new tool are compatible." In fact, Peters terms the task of adding new capabilities almost trivial under the right conditions; "all that's needed, basically, is a translational mechanism for the data, and a mechanism allowing the user, through CHAS, to invoke the new tool—a little input language. And since it includes ASCII text-editing capabilities, generation of the input language is simplified too"—but



Pretty picture. J. Craig Mudge, technical director, and Carol Peters, principal software engineer of CHAS design group, check mask of floating-point processor.

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Peters would be the last one to suggest that CHAS is a complete production too. "It will require several major additions before we can call it that," she says. But she does consider it a more than adequate proof of principle behind the approach.

The system speeds the design process itself by offering whatever CAD tools engineers need and dividing the design task among an arbitrary number of engineers at interactive work stations, thus cutting design time. It imposes controls on the design process so that the work of the various engineers can be evaluated in the context of the whole design; and it acts as prompter, information clearinghouse, data-base manager, and communications channel between designers. Regardless of the CAD tools used in the design trenches, all results from individual design exercises, refinements, iterations, and interconnections are under CHAS supervision.

The design system yields up about a dozen programmable logic arrays per second, with or without microcode—each of which can be customized by the engineer. It also establishes and monitors interfacing ground rules, performs consistency checks and geometrical editing, and carries out truth table verification. Some of this checking is done in a background mode with CHAS intervening in the process to correct engineers' errors by prompting at every level, says Mudge.

As implemented at DEC, the system is supported by two DECsystem 2020 mainframe computers with 180 megabytes of disk storage. About 5 megabytes are required for the floating-point-processor design. Other data, like design software, takes further disk space, but there is still enough space left for several parallel chip-design efforts.

Good ratio. CHAS encourages regularity of design, highly desirable in VLSI devices, according to Mudge. "Regularity," a term coined by William Lattin of Intel Corp., is the ratio of transistors in a VLSI design to the number individually designed. A high regularity factor means a healthy dose of CAD and thus faster

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Regularity factors are relatively low today, reaching about 5, according to Mudge. For example, the 8080 has a published regularity of about 1. The 8085's is about 3.5 and that of the 8086 about 4.4. With CHAS, Mudge's group hoped for a regularity factor of 50 to 75 in the first, proof-of-principle design—a highly complex floating-point processor chip. They topped 74, a tenfold improvement over today's best commercial designs.

As the high regularity factor hints, the design effort was swift, taking, at most, eight calendar months. And since the average number of engineers in the design group was only seven or eight, total design time was minimal by today's standards—and a good part of that time was also spent wringing out CHAS.

Data-base plan. With CHAS, evolution of a design corresponds to growth of a data base. All parametric data on a chip design is entered in memory, from the first crude "floor plan" to the final check plot and simulated performance figures. Thus, notes Mudge, it is possible to keep a one-to-one correspondence between successive layers in a design, "from the schematic to the silicon," he says.

Engineers enter data using whatever is available or convenient. At DEC, the medium is usually a Calma work station or custom, interactive work stations developed by the group as part of the CHAS effort and modeled on work stations designed at Caltech.

The CHAS prototype station is built around a 19-inch color display driven by a PDP-11/04 computer with 128-K bytes of frame storage. Direct input is via either a Talos Systems X-Y tablet or the keyboard of a DECscope alphanumeric display terminal. A Hewlett-Packard 7221 color plotter provides hard copy.

The whole station was assembled for less than $25,000, a price low enough, in Mudge's estimation, to make it attractive to VLSI design firms. "The trick is to make it possible for them to be able to buy a fair number of them," he says. □

Information processing

Europeans tighten data flow

Move is hailed as safeguarding human right to privacy, but Americans criticize agreement as protectionist

by Kenneth Dreyfack, Paris bureau

Watchdogs over the rights of individual citizens in Europe are quietly rejoicing about efforts to control transborder data flows, but some U. S. businessmen are concerned that European governments will use those controls as a smoke screen for protectionism.

The issue is hardly academic: seven countries agreed on Jan. 28 to abide by the Council of Europe's data-protection convention. The convention, a binding treatylike document designed to restrict the traffic in personal information across national borders, should be ratified and operating within the next 18 months. The seven are Sweden, West Germany, Austria, Denmark, Luxembourg, France, and Turkey. Another, Norway, is expected to sign soon.

The conflict is sometimes stated, in rather simplistic terms, as one between European concern over protecting individuals from abuse arising from dissemination of confidential data and U. S. insistence on the free flow of information as a basic right. "American multinationals are wired to the hilt, and any impediment hurts the transparency, speed, and cost benefit of their data communications," says G. Russell Pipe, former consultant to the Organization for Economic Cooperation and Development and president of Transnational Data Reporting Service in Amsterdam.

Power grab seen. Further complicating the situation, Pipe and other U. S. observers believe European governments are using the data-protection issue to ensure themselves a firm economic grip over new digital communications techniques. "What is really going on is competition between European PTTs [national postal and telecommunications authorities] and the American telecommunications industry—and the whole issue is clouded by the transborder data-flow issue," says Willis H. Ware, head of the Computer Sciences department of the Rand Corp., Santa Monica, Calif., and chairman of the National Security Agency's scientific advisory board.

In any case, European telecommunications authorities have no intention of letting data communications fall into private hands. Private networks such as Tymnet and Telenet are unknown in Europe, and a privately owned satellite service like that of Satellite Business Systems is unthinkable. Without competition from the private sector, the Europeans are under little pressure to lower their rates. So for Americans accustomed to cheap, unregulated data communications, the European scene is a headache.

"These laws are not intended as a method of economic protection," insists Hans Peter Bull, West German federal commissioner for data protection. "Other methods of protecting industry would be much more efficient." The Europeans also insist that they favor a free flow of information despite their concern with keeping it out of the wrong hands—and that U. S. and European interests in protecting privacy are similar.

"We passed the convention in the

Making it official. Swedish Foreign Minister Ola Ullsten signs data-protection convention as officials of the Council of Europe look on. Sweden was the first of seven original signatories.

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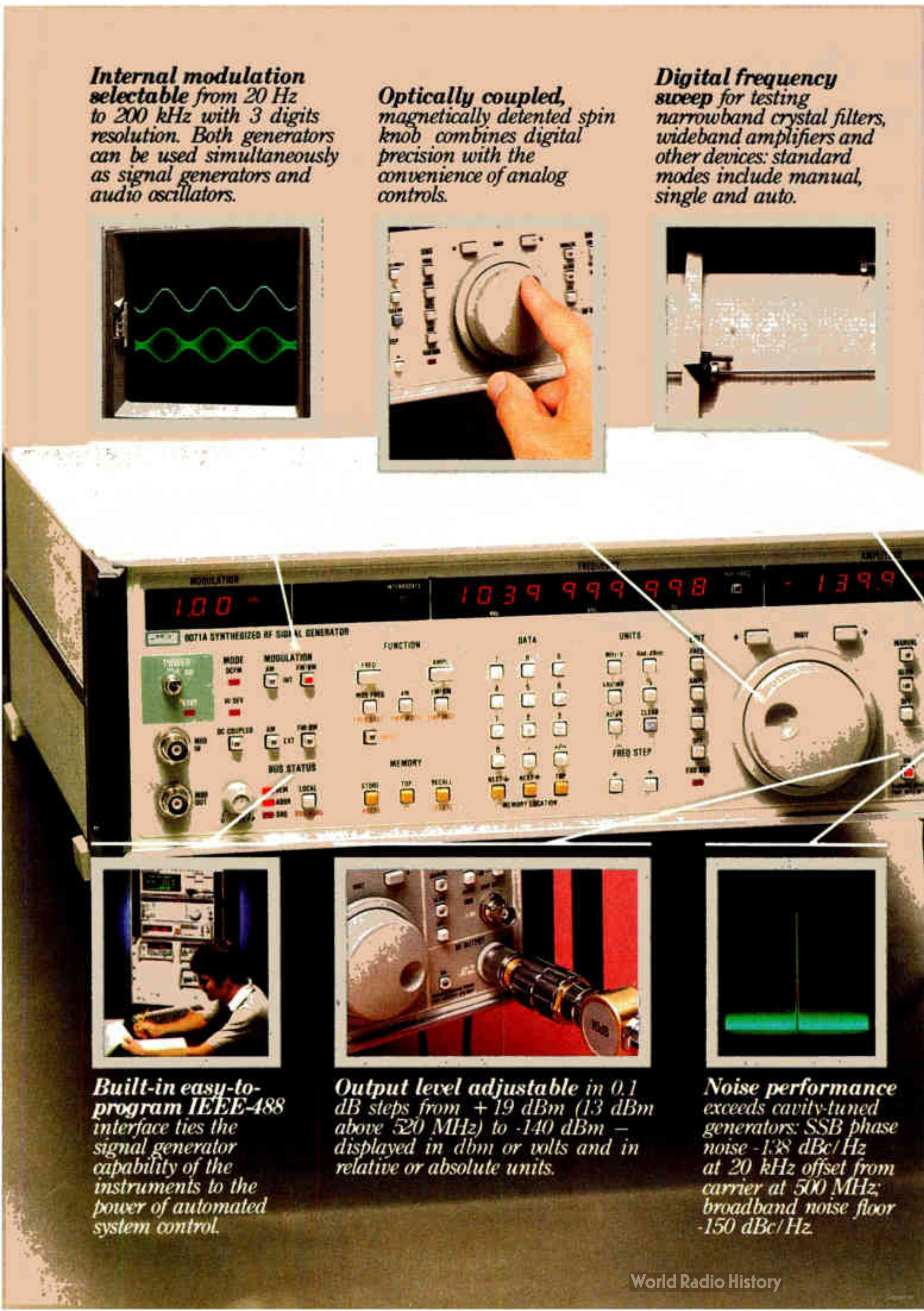

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interest of the free flow of information, because without international legal action national laws were putting heavy restrictions on transborder data flows," explains Fredrik Hondius, the international jurist who as head of the public law division in the 21-member Council of Europe was the driving force behind the group's data-protection convention.

Hondius and others who have been working toward data-protection measures emphasize that the prime motivation behind national laws in Europe is to protect citizens' right to privacy—especially from government abuse. Officials in countries occupied by Nazi Germany during World War II shudder at the idea of what would have happened if the Nazis had had access to computerized personal data files.

Some Europeans find the U. S. use of "free flow of information" a meaningless catch phrase. "We are exercising [information] control every day, with an overwhelming support from public opinion in democratic societies," says Knut S. Selmer, professor of law at the University of Oslo and chairman of the Norwegian Research Center for Computers and Law. As examples, he cites laws on slander, libel, and pornography, which prohibit the communication of information that threatens the interests of others or the common good. Military information is another area where restrictions are tight and penalties severe.

U. S. invited. Though both public and private officials in the U. S. have so far shown little sympathy for the European approach, the Council of Europe has invited the U. S. Government to adopt some provisions of its convention if it is not interested in the complete document. And Hondius is optimistic about U. S. adoption of a Council of Europe measure, developed as an adjunct to the convention, to control personal medical records. Hondius also feels cooperation in the area of credit information is likely.

With data-protection laws already on the books in seven European countries, and with most others now heading the same way, it is safe to predict that virtually all Western European countries, and perhaps Canada and Australia, should sign the Council of Europe convention over the coming five years. Within that time, they should be able to resolve a key outstanding legal problem—that of place or jurisdiction.

The growing popularity of distributed data-processing systems complicates the problem. Imagine a personal data bank in West Germany listing credit information on Belgians, accessed from a terminal in Italy, and transmitted via France's packet-switching network. If there is a suspected data-law violation, where should the trial be held? □

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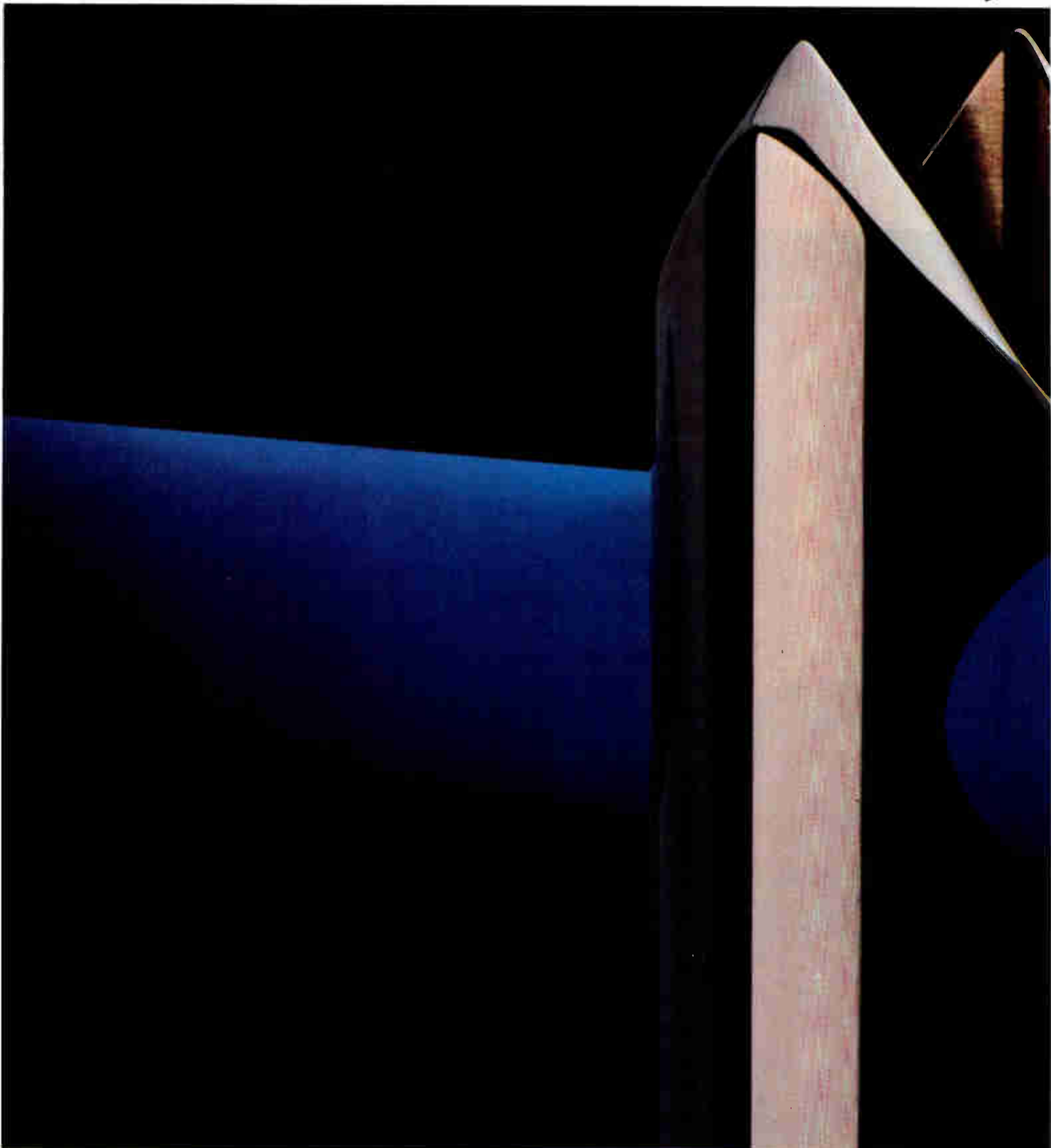

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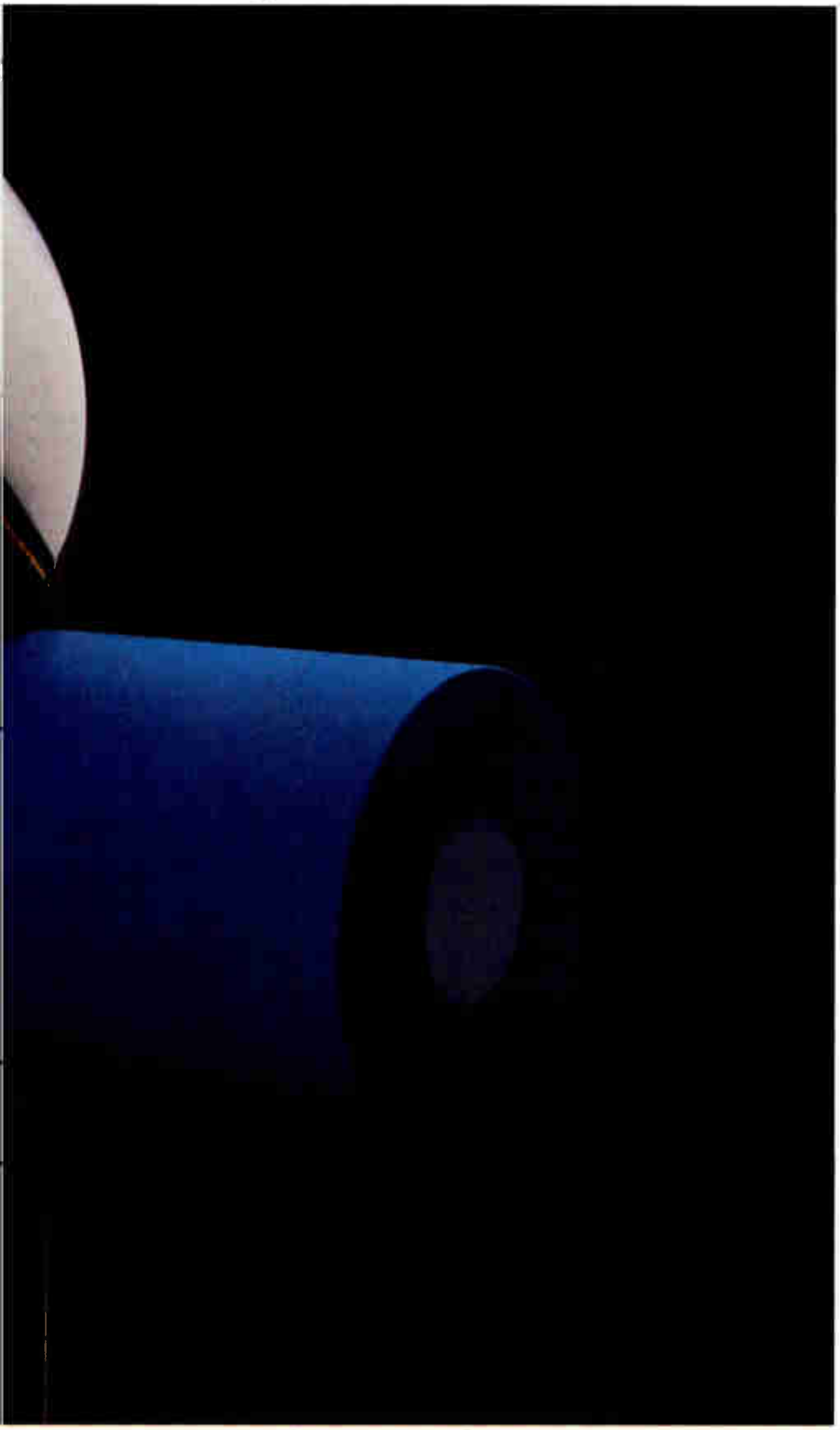

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M6805 Family MCUs all have at least 64 bytes of RAM, plus clock, timer and bidirectional I/O on-board with the MPU. The 28-pin HMOS MC6805P2 has 1100 bytes of user ROM on-chip, and the 40-pin MC6805U2 has 2048 bytes of ROM and 32 I/O lines. The 40-pin MC6805R2 also adds a 4-channel, 8-bit A/D converter. The MC68705P3, with 112 bytes of RAM, has 1804 bytes of user EPROM in place of ROM, and the CMOS MC146805E2 is a ROMless version available for low-power requirements.

Facts say it's a better MCU family.

Most inexpensive MCUs have no interrupts. Each M6805 Family MCU has a minimum of three: external, timer, and software.

Most MCUs are locked into a single configuration. M6805 Family MCUs are designed for versatility, for use in varied configurations, in either HMOS or CMOS.

Some day most MCUs will be able to "test themselves". Only the M6805 Family has on-chip self-check capability today. This means simpler and less expensive testing for users, resulting in lower overall costs.

And there's more. I/O lines are organized into three flexible ports, with one able to drive the widely-used common-cathode LEDs. The 8-bit timer is software programmable with a mask-programmed prescaler.

The MC68705 EPROM MCU contains a bootstrap program in ROM to simplify user-programming of the EPROM.

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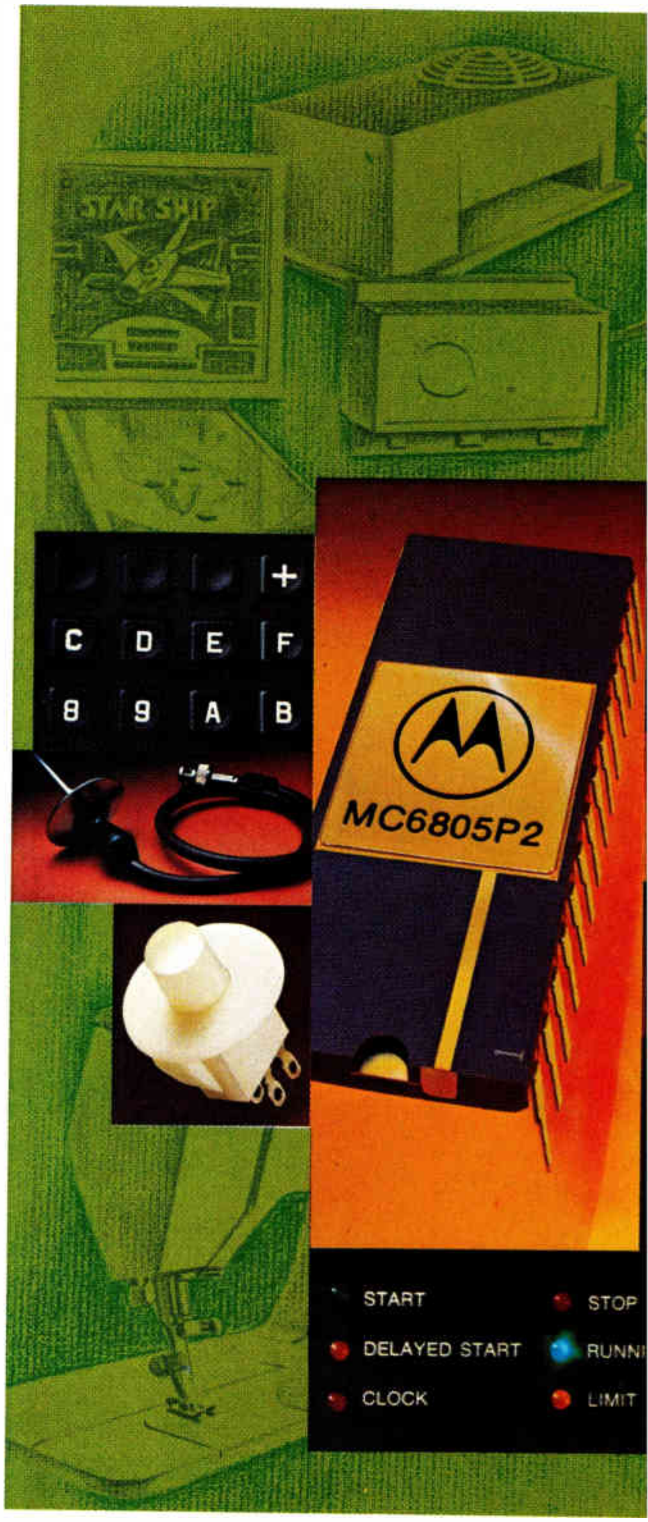
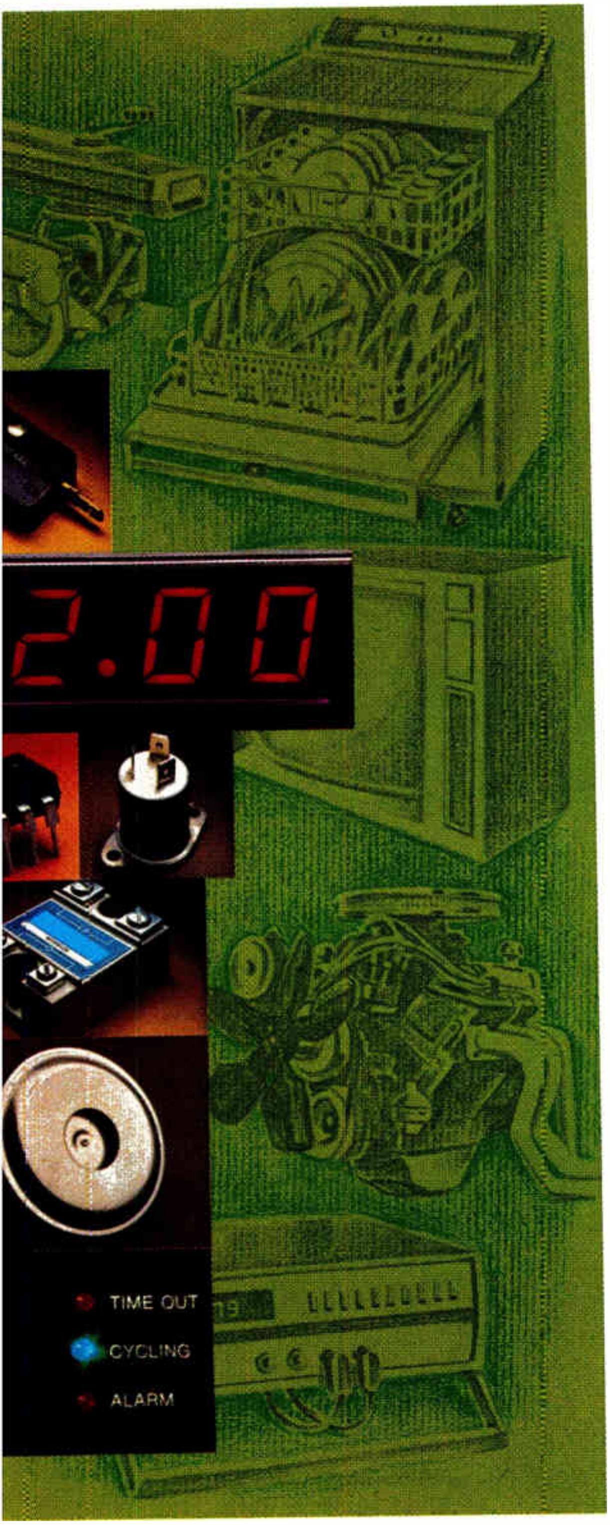
M6800 users find it an easy transition to programming M6805 Family MCUs, and the switch



these single-chip 8-bit so many, for so little.



from M6805 Family to M6800 processors is equally simple. Most programmers will agree: M6805 Family MCUs are programmed more easily and quickly, and at lower cost, than competing MCUs.

Complete development support.

Hardware and software (assembler) development support is provided for the MC6805P2 by the MEX6805 system. A simple adapter is available for converting this system to support of the other M6805 Family MCUs.

Each of these systems is fully compatible with both MC6800- and MC6809-based EXORciser® and EXORterm™ development systems. Each also provides a complete memory map, selectable via software, using RAM, EPROM, ROM or external memory.

Real-time emulation capability is a major MEX6805 feature. Debugging features include trace, display of registers and memory, single-step capability, plus halt on address and break points.

Evaluation units are available now.

An HMOS evaluation unit, the MC6805P2L1, is available with a terminal-interface program. It contains sample routines, demonstrates the "self-check" feature and performs standard monitor functions.

The MC6805R2L1 provides the same functions plus a stand-alone program mode for evaluating the A/D converter. The MC6805U2P2 has a 64-key keyboard encoder with parallel ASCII output in place of the A/D converter evaluation function.

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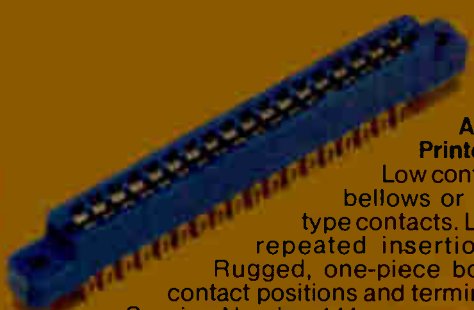

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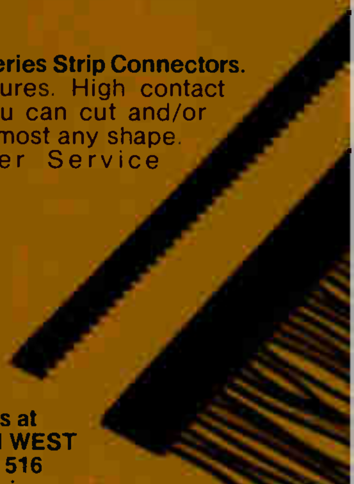

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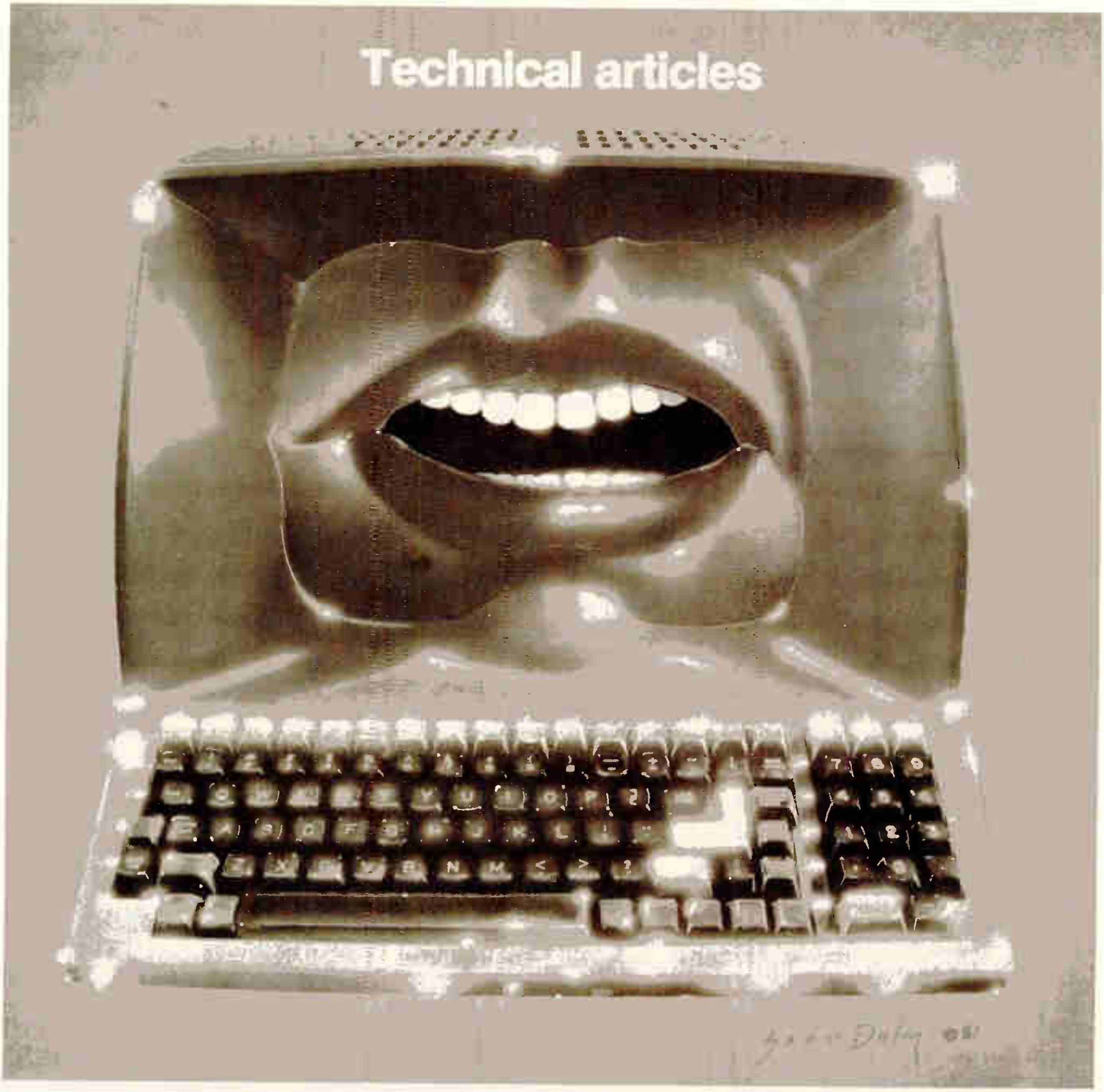


GIVING VOICE TO TEXT

The science of translating the printed word into synthetic speech is not new. But recent breakthroughs in integrated circuit technology have made text-to-speech techniques and speech-synthesizing circuits themselves so much less expensive that they can now be applied more readily, especially in the consumer market. The following two articles describe different approaches to designing systems for converting typed-in text into speech.

The first system, from Votrax, a division of Federal Screw Works in Troy, Mich., builds a vocabulary using a keyboard terminal that resembles a microprocessor development system. The data developed at the terminal is then fed to another Votrax innovation—the most comprehensive chip so far for developing synthetic speech, which features a low data rate and the capacity for unlimited vocabulary.

Texas Instruments Inc. in Dallas has developed its text-to-speech capability as an adjunct to its 99/4 home computer. Like the Votrax terminal, TI's computer relies on proprietary text-analyzing software. The resultant data is fed to a voice synthesizer similar to that used in its Speak & Spell learning aid for children.

Votrax will market its speech chip and development aids as widely as possible. TI intends its system to be used initially to speak aloud information sent by videotex information utilities. New applications for the system and for the synthesizer chip will undoubtedly develop. **-Gil Bassak**

Text translator builds vocabulary for speech chip

Voice synthesis chip and development system ease design of speech into consumer products

by Tim A. Gargagliano and Kathryn Fons
Votrax Division, Federal Screw Works, Troy, Mich.

☐ Computer manufacturers planning to use speech synthesis devices in new products can now develop their own vocabulary in house, without the usual vendor assistance. Votrax has introduced a chip-level voice synthesizer and a companion development system, which employs text-to-speech software to help the user arrive at a repertoire of words for synthesis.

The speech synthesis process typically begins with recording a human voice and analyzing it to extract important frequency and amplitude data. This data is then stored in memory and accessed by the synthesizer chip to re-create speech.

However, with the Votrax CDS II text-to-speech development system and SC-01 speech chip, the words to be synthesized are simply typed on a keyboard. No human voice is involved.

The CDS II development system (Fig. 1) generates data used by the SC-01 speech chip. The development system is based on a 6808 Motorola microprocessor. A text-to-speech algorithm plus the CDS operating system is stored in 24-K bytes of read-only memory and a work space in 2-K bytes of random-access memory.

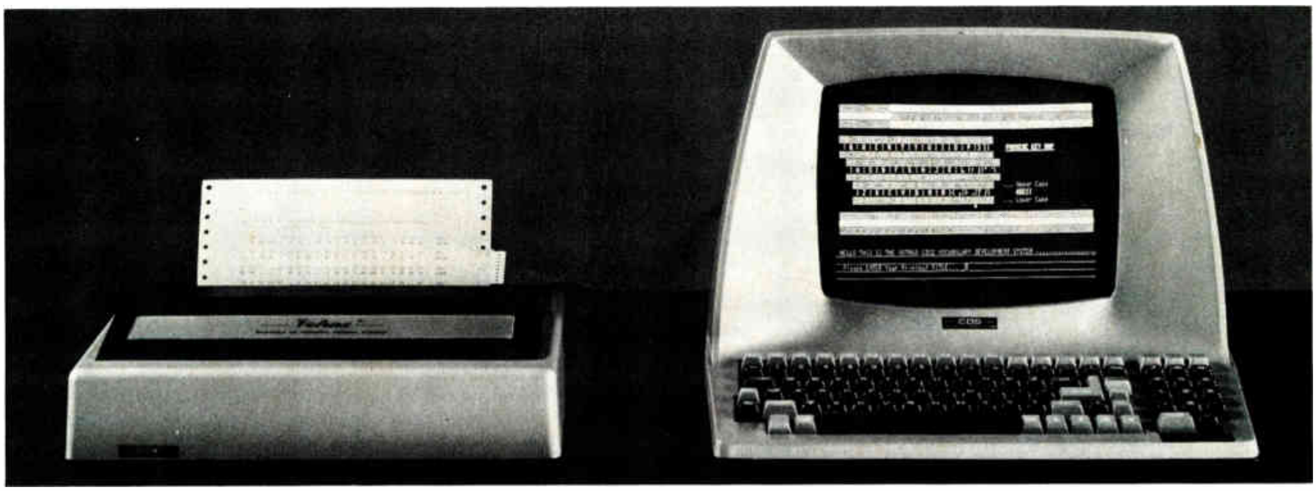
Data from the development system programs a memory, usually an erasable programmable ROM that stores data for the chip. In order to program the PROM, the development system uses an RS-232 interface to transfer the data serially to a host computer, a paper-tape punch, or some other mechanism for eventually burning in a PROM.

Since the development system has a Centronics 730 printer, the speech data can also be printed out in hexadecimal code and then entered manually into a PROM programmer. Whatever the programming mechanism, once memory is loaded with words a user wants, speech is produced by the SC-01 chip when it accesses the data from it.

Those preferring not to spend $15,000 for the development system may opt for a versatile speech module (Fig. 2) that has no text-to-speech capability. Instead, the VSM, a single-board device that requires a video terminal and must be plugged into an external power supply, stores 1,300 words and 25 suffixes and prefixes in a memory. There are also 12 instructions for generating sound effects.

The VSM sells for about $1,200 and is intended to assist those with limited resources in developing a word vocabulary for the SC-01 speech chip. Like the CDS II development system, it is also based on a 6808 microprocessor. It contains the SC-01 chip plus an operating system in 2-K bytes of ROM, a word table in 8-K bytes of E-PROM, and 1-K byte of RAM work space.

The operating system has exit and entry points for passing control of the module to an external system. This allows an external processor or host computer to control the module, easing the development task. For example,



1. Well-developed. With this CDS-II development system, a designer types a word or phrase into a keyboard and gets back a phonetic breakdown of the text. Each phoneme, or component sound, is assigned a hexadecimal code, which a synthesizer chip converts into speech.

Some ways of synthesizing speech

With new consumer markets in sight, companies in the U. S. and abroad have now introduced—or soon will introduce—their versions of a talking chip.

These chips differ in speech quality, bit rates, memory requirements, interfacing schemes, and the level of support needed to develop a vocabulary. But they all draw on two fundamental speech synthesis approaches.

The first reconstructs a digitized time-domain signal using a digital-to-analog converter. This straightforward method varies widely according to the digitization and encoding scheme used. It is closest to human speech, but at the cost of very high bit rates and large memory storage requirements since each word to be spoken must be stored separately.

The more common approach is to synthesize, or reconstruct, the time-varying spectral parameters of speech—that is, the frequency and energy content of a speech signal. Lower bit rates are achieved because of the relatively slow change of the spectral parameters in speech and hence the low rate at which they need to be updated.

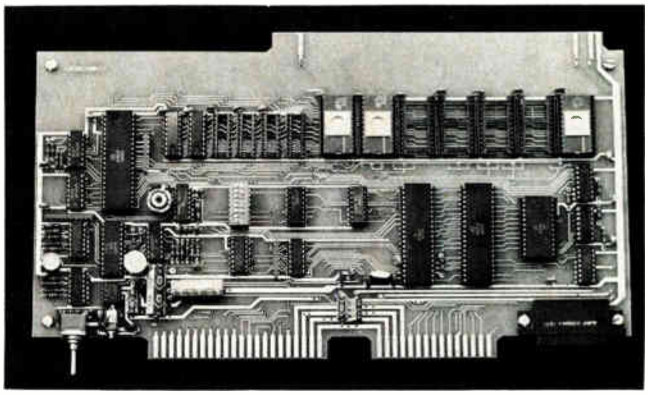
Several methods are used to extract and encode spectral parameters. The bands of frequencies that these parameters define are called formants, which are the major resonant frequencies of speech. In electronic speech synthesis, formants are produced by either analog or digital filters. The excitation signals driving these filters are both periodic and random waveforms that emulate vocal pitch and the sounds of turbulant air generated during speech.

Formant synthesis requires a moderate bit rate and offers good reproduction of speech characteristics. The ultimate in low-bit-rate speech synthesis is a formant approach called phoneme synthesis, in which the spectral parameters are derived from basic word sounds. A key element in phoneme synthesis is a phoneme code-to-parameter translator. This translator makes it unnecessary to analyze speech to derive the parameters. Votrax's SC-01 speech chip, which uses phoneme synthesis, performs phoneme-to-parameter translation in its phoneme controller circuit.

Speech can also be synthesized directly from text, without first translating it into phonemes, by storing whole words or phrases. But the resulting bit rate is no lower than with phonemes, and since a phoneme synthesizer generates its own parametric data instead of having it done on a separate computer, it has unlimited vocabulary.

an engineer might use any text-editing program in the host computer to ease the process of programming.

With the VSM, the user may generate words not stored in the word table and adjust the pitch and the transitions between words with a terminal or a host computer, to improve the synthesized speech. With the VSM the user can fully exercise the speech chip and develop a set of data matched for his or her application. It is also possible to use the VSM as a self-contained speech module in an end product. The on-board processor can be programmed to control the module's operation and its interface with the outside world.



2. Bare bones. Based on a 6808 microprocessor and with a speech synthesizer on board, the Votrax VSM (versatile speech module) is a low-cost alternative for developing speech data for the SC-01 synthesizer. It has a 2-K-byte operating system and a table of 1,300 words.

Expanding applications

The synthesizer chip itself, which costs about $12 in large quantities, is aimed at consumer products, computer and information systems, timesharing systems, training simulators, and other electronic speech applications. It works with an external memory, not shown in the chip's block diagram in Fig. 3. The memory size depends on how large a vocabulary of words is needed for a given application. The memory stores a sequence of 6-bit codes, each of them representing a basic word sound, or phoneme.

The SC-01 is in two functional parts. The first part translates the digital code taken from memory and generates an array of spectral parameters for adjusting the second part of the chip, which is an electronic model of the human vocal tract.

The vocal tract model itself, shown inside the dashed area of Fig. 3, has three main parts. First is a pair of signal sources—a variable-frequency oscillator for simulating the vocal chords and a pseudorandom-signal generator that simulates the sound of rushing air that is common in speech.

The outputs of these sources are shaped by the second main part of the vocal tract model—a bank of four analog bandpass filters that simulate the vocal cavities. Finally, the output of the filters is fed to the audio preamplifier, which in turn drives an external amplifier. The external amplifier, supplied by the user, can be a class A type. However, to reduce overall power consumption, the synthesizer chip has a current sink for implementing a class B amplifier. In either case the external amplifier in turn drives a speaker in the last stage of the speech synthesis process.

Sound spectrum

The heart of the SC-01 is the proprietary phoneme controller, which translates the phoneme code into a matrix of spectral parameters, which in turn adjust the vocal tract model to synthesize the phonemes.

Sixty-four possible speech sounds or phonemes, from which all English words are formed, are processed by the controller. The controller not only translates phoneme codes into parametric data but also adjusts their inflection by introducing subtle variations in pitch. Pitch variation prevents the synthesized voice from sounding monotonous or robotlike.

A clock circuit on the chip drives the synthesizer. Its frequency is adjusted by changing the time constant of an external resistor-capacitor network. Two pitch control lines labeled 1 and 2 produce gross changes in the frequency of the signal source so the chip can emulate more than one voice if the state of either line is changed.

A phoneme is generated by latching a 6-bit phoneme code from data lines P_0 through P_5 into register Q_1 using the strobe input line. The phoneme is processed by the phoneme controller, which tailors the vocal tract model to generate the phoneme sound. Finally the speech-output signal is available at the audio output pin, A_0.

Each phoneme is internally timed, with a duration of between 50 and 250 milliseconds, depending on the phoneme. When the phoneme is complete, the acknowledge/request line goes high to request the next phoneme and then goes low when the next phoneme is strobed in.

The chip is a complementary-MOS device in a 22-pin dual in-line package. It draws only 7 milliamperes over a 7- to 14-volt dc supply range. The filter network used to model the vocal tract is designed using switched-capacitance networks. These allow the low-frequency bandpass filters to be integrated without using space-consuming resistors [*Electronics*, Feb. 15, 1979, p. 105], resulting in a comparatively small chip.

The phoneme data processed by the SC-01 is developed by the text-to-speech algorithm executed in the development system. The proprietary text-to-speech software analyzes the character string stored in memory. The string represents the text typed in using the system keyboard or downloaded from a host computer. The text words are broken down into phonemes by the software according to a stored set of rules regarding English pronunciation.

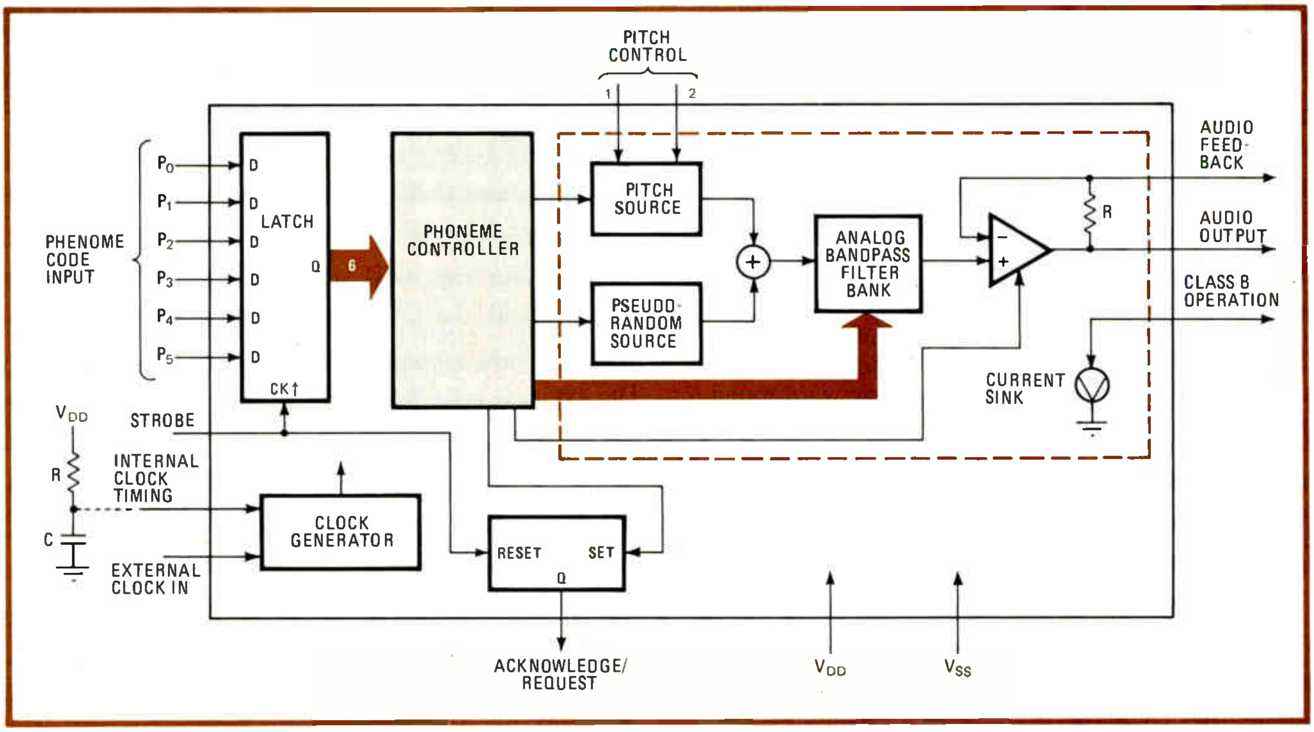
The program scans the words, searching for the most appropriate rules for replacing each word with a phoneme equivalent—that is, a string of component sounds making up the word.

The text-to-speech algorithm, based on a set of rules developed by Votrax's research and development laboratory, includes a list of two- and three-letter acronyms whose letters are spelled out by the software (that is, IBM is not pronounced as "ibm" but given instead as "eye-bee-em"). It also looks for nonsense words—character strings that are excessively long or contain no vowels. A sample output from the development system is shown in Fig. 4, where the typed-in phrase at the top is processed by the algorithm and the phonemes and their hexadecimal representations appear below the phrase. A partial list of phonemes, with their hexadecimal codes and pronunciation guides, is given in the table.

Stress determines duration

Several of the phonetic symbols use a number as a part of the code. These numbers indicate that the sound has a shorter duration than the core sound, which has no number. For example, the core sound /EH/ has three components of shorter duration, /EH3/ being shortest. In actual time, as listed in the table, /EH3/ is only 59 milliseconds. This is 126 ms shorter than /EH/ at 185 ms.

How the words are pronounced dictates the phonemes necessary for a sequence, but the stress pattern determines the duration of the phoneme to use in that



3. C-MOS synthesizer. Phonetic codes are latched and used by the phonetic controller, which generates signals used by the vocal tract model (shown inside dashed lines). The model, which is made up of a filter bank and signal sources, emulates the sounds of human speech.

```
>> THE SC01  IS THE WORLDS FIRST  PHONEME SYNTHESIZER ON A SINGLE
   CHIP
   - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   ..  38  32  23  ..  02  01  1F  1F  3C  21  29  ..  12  21  0B  2B  35  37  2D     Hex
   ... THV UH1 UH3 ... EH1 EH2 S   S   E1  AY  Y   ... Z   AY  I1  R   01  U1  W      Votrax

   32  31  0D  ..  3E  ..  0B  09  12  ..  38  32  23  ..  2D  3A  2B  18  1E  12     Hex
   UH1 UH2 N   ... PA1 ... I1  I3  Z   ... THV UH1 UH3 ... W   ER  R   L   D   Z      Votrax

   ..  1D  3A  2B  1F  2A  ..  3E  ..  1D  35  37  0D  3C  29  0C  ..  1F  0B  0D     Hex
   ... F   ER  R   S   T   ... PA1 ... F   01  U1  N   E1  Y   M   ... S   I1  N      Votrax

   39  02  00  12  15  00  29  12  3A  ..  15  23  0D  ..  06  21  29  ..  1F  0B     Hex
   TH  EH1 EH3 Z   AH1 EH3 Y   Z   ER  ... AH1 UH3 N   ... A1  AY  Y   ... S   I1     Votrax

   09  14  1C  23  18  ..  3E  ..  2A  10  0B  09  25      Hex
   I3  NG  G   UH3 L   ... PA1 ... T   CH  I1  I3  P       Votrax
   *77 Phonemes- - - - - - - - - - - - - - - - - - - - - - - - - - -
```

4. Component sounds. The sentence above is shown in terms of its phonetic components, and their hexadecimal codes, as determined by rules in the development system. The designer modifies the code so that the resulting sounds very closely mimic the human voice.

sequence. The table lists several words with the phonetic sequences for correct pronunciation and demonstrates the relationship between stress and duration.

For example, in pronouncing the words "warning" and "system" from the list, the first syllable in each word is the accented syllable, shown in the translation of the phonetic symbol sequences for each word. "Warning" requires a medium- and a short-duration /O/ phoneme to achieve the appropriate stress (duration) for pronunciation. Likewise, "system" requires two shorter /I/ phonemes to achieve the appropriate stress. In both cases, the final syllables are unaccented and utilize that component of the basic phoneme with the shortest duration.

Phonetic programming—resolving words into phonemes—is not difficult once the user becomes familiar with the phonetic symbols. Doing it manually can be time-consuming but is cost-effective if only a few words must be synthesized.

A powerful feature of phoneme synthesis is that vocabulary development can be done by users at their own facilities with the aid of a system like the CDSII. There are no turnaround delays as there are for those who depend on outside programmers. Vocabulary changes are easily accommodated right up to the time of final assembly of the product.

Also advantageous is the very small storage vocabulary requirement. Each phoneme needs only 6 bits of memory, and trial vocabularies can be quickly assembled without special memory chips. For instance, a 16-K programmable read-only memory such as a 2716 can store as many as 300 words.

A third feature of phoneme synthesis is that product security is maintained throughout the development procedure since no outside development support is necessary. An RS-232 port is provided on the development system to connect it to a host computer. In this way, speech data can be dumped into the host, or the host can take control of the development system to facilitate a high-speed translation of words into phonemes.

Votrax has been developing and selling its line of commercial speech products for about 10 years. It has been known for its highly successful VS line of rack-mounted voice synthesizers as well as its multi-lingual ML line of synthesizers, both of which produce very authentic sounding speech but at much higher costs than the chip. It has also sold board-level synthesizers, that are smaller and use less power than the VS and ML series, to a wide customer base, including personal computer manufacturers offering the system as an option for experimenting with electronic speech synthesis. □

PARTIAL LIST OF PHONETIC SYMBOLS

Phoneme hexadecimal code	Phoneme symbol	Duration (ms)	Example word
00	EH3	59	jacket
01	EH2	71	enlist
02	EH1	121	heavy
03	PA0	47	no sound
04	DT	47	butter
05	A2	71	made
06	A1	103	made
07	ZH	90	azure
08	AH2	71	honest
09	I3	55	inhibit
0A	I2	80	inhibit
0B	I1	121	inhibit
0C	M	103	mat
0D	N	80	sun

Examples:

Hello	H–EH1–UH3–L–UH3–01–U1
Good-bye	G–001–001–D–PA0–B–AH1–EH3–Y
Warning	W–01–02–R–N–I3–NG
System	S–I1–I3–S–T–EH3–M

Software rules give personal computer real word power

Speech IC and algorithm for pronunciation let computer 'read' aloud words on its own display

by Kun-Shan Lin, Gene A. Frantz, and Kathy Goudie
Texas Instruments Inc., Dallas, Texas

☐ The field of electronic speech synthesis is widening. A new text-to-speech translator from Texas Instruments can "read" aloud messages typed into a computer terminal. The system's software analyzes the text into elements that are pronounced by a TMS 5200 speech synthesizer chip.

The translator will be first used in the TI 99/4 personal computer, where it will read aloud information displayed on the computer screen. Such data might include news or weather information received from a videotex or electronic mail service.

Unlike the company's Speak & Spell learning aid, the text-to-speech system does not use "canned" words and phrases stored in a read-only memory. Instead, it generates words from a stored library of 128 sounds, called allophones, which it concatenates, or connects to form speech. Text-to-allophone software chooses the allophones and determines their stressing and intonation. It then transfers this information to the speech-generating hardware, which translates it into speech sounds using a linear predictive coding technique.

At the core of this hardware is the TMS 5200 speech synthesizer and a central processing unit that delivers the data to the synthesizer in an orderly way—keeping track, for example, of times when the synthesizer buffer is almost empty. The CPU then takes fresh data and loads the synthesizer's internal buffer. The synthesizer, in turn, takes the data and produces the time-varying speech signals that are amplified to drive a speaker.

In addition, a TMS 6100 128-K read-only memory chip can store common words or sounds the designer may wish to include in the system.

The speech synthesizer can work with any standard 8-bit microprocessor, since it has been designed with a first-in, first-out buffer on board to store chunks of data, freeing the CPU for other tasks.

A typical text-to-speech system (Fig. 1) generates speech in two major steps—speech construction and speech synthesis. Speech construction is done in two stages. The first is the translation of the letters of the text into a digital representation of component sounds. The second is the concatenation, or stringing together, of these digitally coded sounds. These component sounds can be complete words or phrases or simply the elements of words (see "Speech construction tradeoffs", p. 123). Speech synthesis then converts the digital data into audible, synthetic speech. TI's approach constructs speech for later synthesis out of elemental component sounds.

A little linguistics

Deciding which components to use requires a closer look at speech sounds. When speech is pronounced, there may be hundreds of minor variations between sounds that are roughly categorized as the same. For example, the /P/ sound in pin is aspirated (followed by a puff of air), whereas the /P/ in spin is not. Sounds that are slightly different but generally perceived as the same in a language are called phonemes of that language. Subsets of phonemes that change slightly depending on the context or environment in which they appear are called allophones. Thus the unaspirated /P/ sound of spin and

Some speech-construction tradeoffs

In speech construction, a written sentence or phrase is analyzed to identify logically connected groups of sounds. Such groups may be speech components that are smaller than words, or they may be words themselves or groups of words such as phrases.

Speech construction is a subtle and complex procedure, since similar words have different stressing and intonation in different contexts. How well the task is accomplished depends not only on how well the rules of pronunciation can be modeled in software, but also on such factors as the amounts of memory available in the system and the size of a vocabulary it needs.

The three speech construction methods are phrase, word, and component-sound concatenation. Each technique has tradeoffs between speech quality, vocabulary size, and memory required. The larger the vocabulary allowed by a given construction technique, for example, the less the memory cost but the less natural-sounding the speech. Better-quality sound demands more memory and cuts into the vocabulary size.

In phrase concatenation, complete phrases are stored in memory and played back through a synthesizer. This method is sometimes referred to as analysis synthesis, since entire spoken phrases are analyzed to produce synthetic speech. The speech sounds natural since whole phrases at a time are recorded and the prosody—or rhythm—and subtle variations in pitch and loudness are preserved throughout the passage. However, storage and flexibility are problems because the phrases must be stored together and kept intact. Since only a finite number of phrases can be stored in a reasonable amount of memory, the vocabulary is limited.

Word concatenation offers more flexibility than phrase concatenation but at the expense of prosody and other qualities. As these are lost, the words tend to sound artificial when strung together as phrases. But the range of phrases that may be formed is greater for a given memory space, since words may be accessed and connected in any order.

TI chose a third technique called component-sound concatenation because it is the most versatile of all in generating words and sentences. Here a library of fundamental speech sounds, giving the virtually unlimited vocabulary needed for translating any typed passage into speech, is used. Because the sounds stored are basic to speech, almost any English word or phrase can be generated by concatenating the appropriate sound units from the library. The memory cost of creating a library and accessing it to create a word or phrase is almost insignificant. But a major difficulty lies in developing a method for connecting the components of speech sounds without sacrificing variations in rhythm, pitch, and loudness.

the aspirated /P/ sound of pin are different allophones of the same phoneme, /P/, and represent the sound more accurately than the phoneme. For this reason, the text-to-speech system here uses allophone stringing to form words and phrases.

In this system, an allophone varies from 50 to 250 milliseconds in duration and is coded according to the parameters needed for a speech synthesizer that uses linear predictive coding. There are 128 allophones in the library, including long and short pauses, which are coded for energy and filter coefficients, the parameters for setting the filter characteristics in the LPC synthesizer. The entire library takes up 3 kilobytes of storage.

Once the allophone library is established, a set of rules is needed for translating the ASCII text into an allophone string. TI used a set of rules based on one developed by the Naval Research Laboratory in Washington, D. C.

However, the NRL rules deal with phonemes only and have been altered in several ways to give the allophonic version of a phoneme in a particular environment. For instance, rules have been added specifying that certain allophones be used only at the ends of words.

In addition, rules have been included for better pronunciation of words often mispronounced with the NRL rules, like "create," "increase," "lost," and "human." The resulting set of about 650 rules chooses 97% of the phonemes correctly and 92% of the allophones correctly for a typical benchmark test. These rules use 7 kilobytes of storage.

The speech construction program strings the allophones and smooths the transitions between them. Energy levels between allophones are matched to obtain a smooth contour, and filter coefficients are smoothed to make transitions from sound to sound less abrupt.

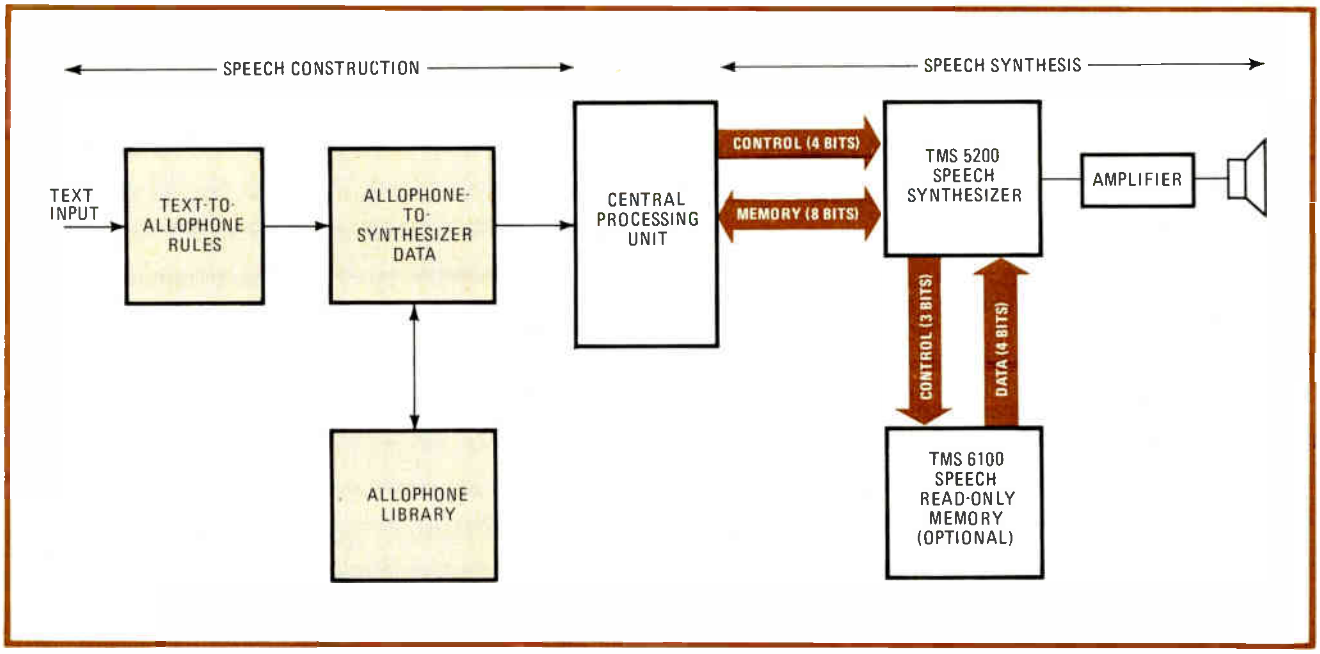
Once the allophones are concatenated, the quality of the speech depends on the stress and intonation patterns applied to the string. Since randomly stressed English sounds unnatural, both stress and intonation must be precisely applied. The pitch assignment is made by a speech-construction algorithm with only the stressed syllables being indicated by the user, who adds the needed pitch pattern to particular points in the sentence.

The control of inflection is based on gradient pitch control of the stressed syllables—that is, stressed syllables of a sentence can be thought of as lying along a line of pitch values tangent to the line of pitch values of the unstressed syllables. In a neutral intonation, the unstressed syllables would lie on a mid-level line of pitch while the stressed syllables would lie on a downward slanting line somewhat higher in pitch than the base line. The slope is constructed in software and the user need only mark the stressed syllables.

Delivering the speech

The speech construction data is used with one of several speech synthesis techniques that generate actual voice sounds. There are two speech synthesis approaches, waveform encoding and parameter encoding (See "Synthesis: another way to go," p. 124)

One of the parameter-encoding—or frequency-based—speech synthesis techniques is the channel vocoder method, which divides a speech signal into narrow frequency bands using a bank of bandpass filters and then stores the amplitude at each center frequency. These amplitudes, along with a variable-frequency source, control a bank of narrowband frequency resona-



1. Spoken aloud. There are two major steps in turning written text into speech—speech construction and speech synthesis. Construction, done in software, resolves the text input into electrical signals that the hardware-based synthesizer converts into "speech."

Synthesis: another way to go

Waveform encoding attempts to reproduce the amplitude-varying signal of natural speech by generating a similar waveform, in contrast to parameter encoding, which represents a speech signal in terms of frequency, or the spectral components of natural speech rather than its amplitude characteristics. Several such techniques are pulse-code modulation, delta modulation, and an amalgam of techniques called Forest Mozer's technique, after its inventor at the University of California at Berkeley.

The simplest waveform-encoding technique is uncompressed digital data recording, referred to as pulse-code modulation. Here the analog speech waveform is sampled and converted into digital information by an analog-to-digital converter. Once in a digital format, the speech signal is stored in memory and played back through a digital-to-analog converter and a low-pass filter. The problem with using PCM alone is that memory requirements quickly become excessive. The average data rate is 96,000 bits for 1 second of speech.

An alternative to PCM, delta modulation, compresses the amount of data needed to record speech digitally. As in PCM, the analog speech waveform is sampled, but this time only the changes in amplitude between samples are stored in memory. Since these changes are usually smaller than the absolute values of amplitude, the overall data rate is less than that of PCM. Thus delta modulation reduces the amount of memory required to store a library of words or phrases.

A simple delta modulation system uses a fixed step of change, or delta, in tracking the original speech waveform—the delta from the previous analog value is always some multiple of a fixed step size. The drawback is that for small changes in amplitude, errors in the form of quantizing noise are introduced.

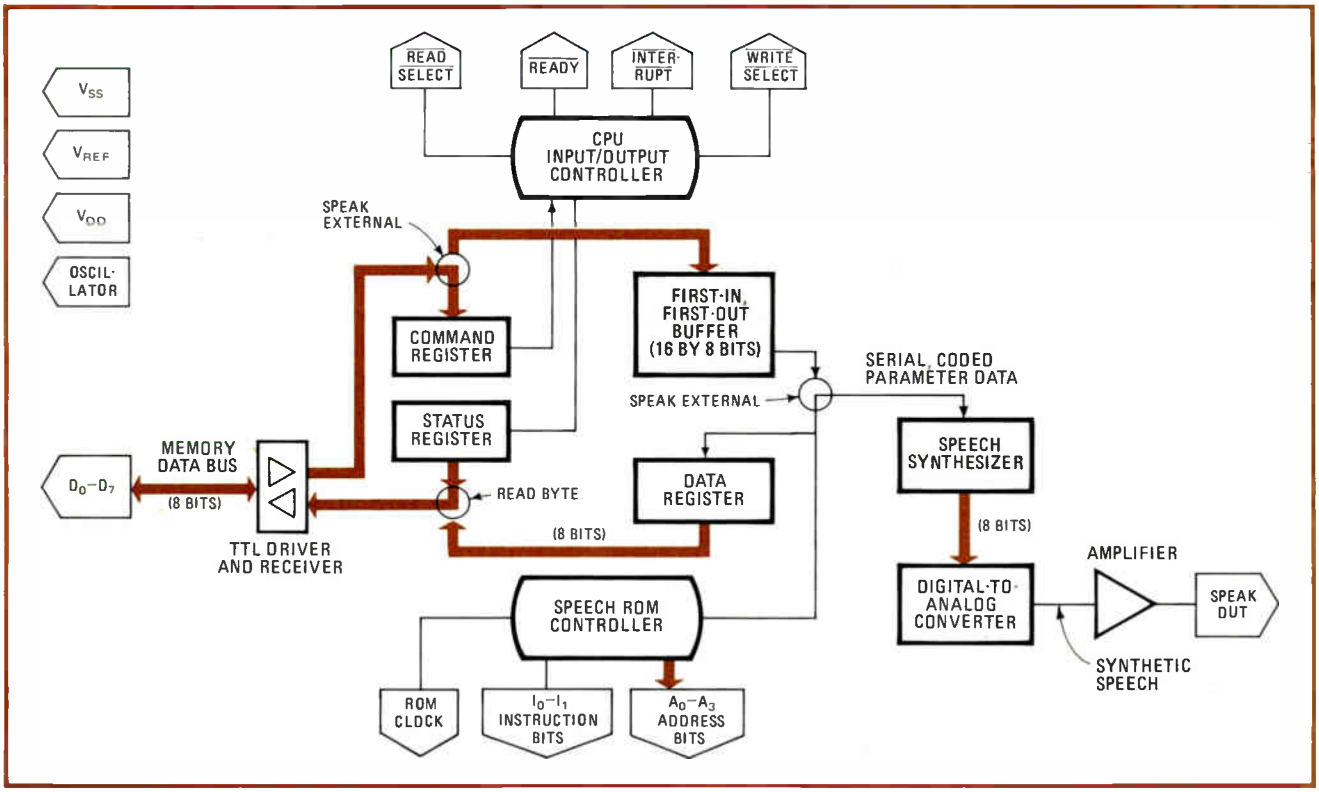
Delta modulation synthesis is improved by making the step size variable and proportional to the difference between the successive samples. Thus, smaller successive changes in amplitude are accurately tracked, using smaller quantizing steps when necessary and so reducing quantizing error or noise. This technique, dubbed continuously variable slope-delta modulation, produces data rates of 16,000 to 32,000 bits per second.

Finally, Forest Mozer's technique uses waveform compression extensively, and its data rate is about 2,400 b/s. The approach combines several techniques, taking advantage of two speech-perception characteristics. First, voiced speech is periodic, containing redundant information, and, secondly, listeners are insensitive to both phase and low-amplitude information. Thus the designer can strip all redundant information from the speech waveform [*Electronics*, April 10, 1980, p. 113], leaving only the most fundamental data for storage in memory.

tors corresponding to the vocoder's own bandpass filters. The data rate of a channel vocoder is typically 2,400 b/s.

Formant synthesis, the second parameter-encoding scheme, emulates the frequency response of voiced speech by generating sharp energy peaks at specific frequencies called formants. The amplitudes and bandwidths of these formants are recorded and used as inputs to excite a formant-based synthesizer. Formant synthesis typically has a data rate of approximately 500 b/s.

A third technique, linear predictive coding [*Electronics*, Aug. 31, 1978, p. 109], was chosen for this text-to-speech system. LPC is essentially a mathematical model of the human vocal tract, implemented as a filter network. The coefficients of the linear equations of the filter used in the model are calculated in the analysis of the original speech and used in the model to control the



2. Enhanced. Control circuits around the synthesizer simplify its interface with an 8-bit microprocessor. The synthesizer exchanges data and commands with the microprocessor along an 8-bit bus and four control lines. External 128-K ROM can also store word data.

"shape" of the vocal tract in speech reproduction. The parameters stored are the filter coefficients, the filter gain, and the frequency of the excitation source used to drive the filter. Good-quality speech is achieved using LPC at data rates from 1,200 to 2,400 b/s.

The 28-pin p-channel MOS TMS 5200, the main hardware component of the text-to-speech system, is a second-generation version of the TMS 5100 speech synthesizer. Several features (Fig. 2) have been added, including a 16-by-8-bit first-in, first-out buffer, to increase its flexibility when it is used with the system central processing unit.

The CPU interface shown in the figure consists of an 8-bit bidirectional data bus (D_0–D_7), read and write select line ($\overline{RS}$ and $\overline{WS}$), a ready line for synchronization (READY), and an interrupt line ($\overline{INT}$).

Activity on the memory data bus is controlled by the read and write select lines. When data is stable on the memory data bus, the ready line will go low to indicate that the CPU may complete a data transfer to or from the synthesizer.

What causes interruptions

The interrupt line indicates a change in the TMS 5200 status that may require the attention of the CPU. For example, the interrupt line, which is normally high, goes low to indicate either the end of speech or that the FIFO buffer is low.

The CPU interface consists of two input-holding registers (the command register and FIFO buffer) and two output-holding registers (the data and status registers).

The command register receives an instruction from the CPU and holds it for the TMS 5200 to interpret and execute. The 128-bit FIFO buffer, organized in a 16-byte parallel-in, serial-out format, holds the speech data used when executing the speak-external command. The buffer is low (BL status) when the FIFO is more than half empty, and the BE status means it is completely empty. When the BE is set, speech is terminated to prevent the synthesizer from processing invalid data.

The data register is an 8-bit serial-in, parallel-out holding register. It is used when speech data is transferred from an external ROM, such as TI's TMS 6100, to the CPU.

The 3 bits of the status register send information about the synthesizer to the CPU to indicate talk, BL, and BE conditions. They can be queried any time except during a memory read command. The CPU passes commands to the TMS 5200 by way of the memory data bus.

For the text-to-speech application, the only significant command is SPEAK EXTERNAL, which lets the CPU, rather than an external ROM, supply speech data to the synthesizer. Upon receipt of this command, the TMS 5200 loads the FIFO buffer with data from the CPU. The synthesizer remains idle until BL becomes false, at which time speech begins and the talk status is set. Data will continue to be taken from the FIFO until a stop code is encountered or the buffer becomes empty. During the execution of a SPEAK EXTERNAL command, no other commands are recognized by the TMS 5200.

The audio output of the TMS 5200 8-bit digital-to-analog converter delivers up to 1.5 milliamperes with a 1.8-kilohm resistor to ground. This signal can then be filtered and amplified to drive a speaker. □

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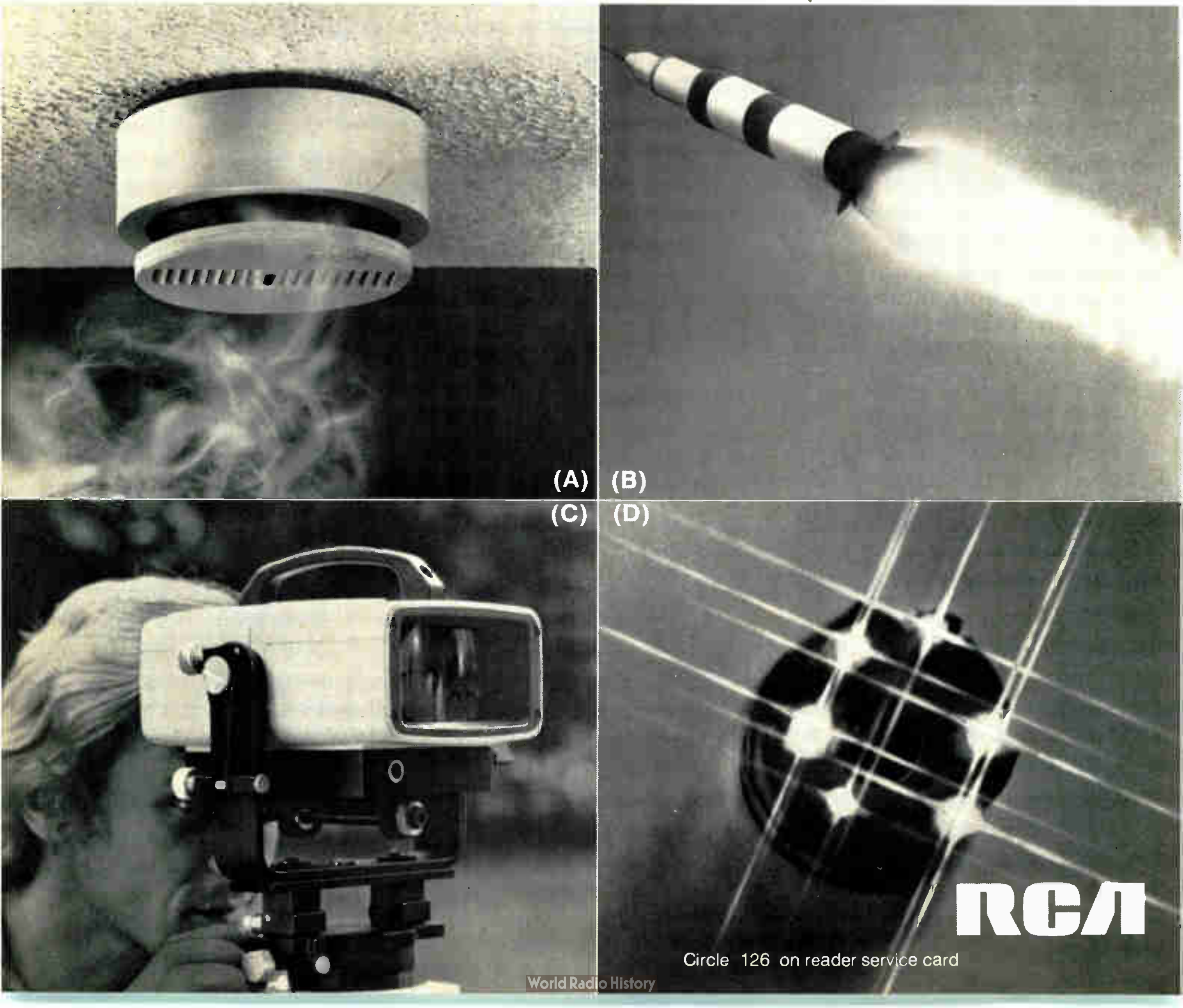


Special report: Ada, the ultimate language?

Software components, so portable that they would be bought like hardware modules, can customize Ada for any task

by R. Colin Johnson, *Microsystems & Software Editor*

☐ Augusta Ada Byron, Countess of Lovelace (1816–1852) and the daughter of the poet Lord George Byron, is credited with being the first programmer because of her work on Charles Babbage's Difference Engine. The forefather of the computer, the machine was designed to calculate entries in logarithm tables. It is a special tribute that the high-level language Ada was named for the first programmer, since its principal designer, Jean Ichbiah, sees Ada as the last computer language. In fact, he holds that Ada will "become the predominant language of the 1980s" and will maintain that position until it is replaced by "automatic program generators by the year 2000."

The concept that guided Ichbiah in achieving Ada's design goals as laid down by the United States Department of Defense is that of the software component [*Electronics*, Dec. 18, 1980, p. 39]. Analogous to hardware components, the software components envisioned by Ichbiah would be selected from a catalog and joined in any combination by virtue of their compatibility with a common bus. Actually, the bus is realized by an Ada compiler itself, which allows the various software components to be "plugged" into it. The place they are plugged into is the program library; any program becomes the bus controller and hence may use the facilities that an installed component provides—just as any module plugged into a hardware bus is available for use by any bus controller.

Ichbiah picked up the concept of software components from M. Douglas McIlroy, head of the Computing Techniques Research department of Bell Laboratories' Computing Research Center in Murray Hill, N. J. He is fond of quoting MacIlroy's statement: "I would like to see components become a dignified branch of software engineering. I would like to see standard catalogs of routines classified by precision, robustness, time-space requirements, and binding time of parameters."

Eponym. The programming language Ada is named after the first programmer, Augusta Ada Byron (1816 –1852), who worked with Charles Babbage.

Meeting the goal

The design goal laid out by the Department of Defense was to produce a language that not only could be used in all programming environments—business, scientific, and so forth—but that also would set new standards in reliability, maintainability, and readability [*Electronics*, Sept. 25, 1980, p. 56]. What has emerged from this charter is a language that contains the best features of Pascal, Algol, and PL/1 while adding real-time multitasking—all under the guiding influence of the software component.

Software components enable Ada to be customized for a specific application without making the extended version incompatible—extensibility without incompatibility was, in fact, a key goal. Most other languages are quite different. Pascal, for instance, exists in many different versions that include unique, incompatible extensions. Ada's designers have taken great pains to maximize Ada's extensibility without sacrificing portability—the ability to run on many different

LIBRARY PACKAGES CATALOG: PAGE 201

Name	Special data types	Overloaded operators +	−	*	÷	Other packages called	Details
Vectors	vector, direction, velocity	✓	✓	✓	✓	math_for_physics matrix_operations	
Matrix_ operations	n_tuple, index	✓	✓	✓		multidimensions	"–" stands fo inversion
Weather	temperature wind_velocity humidity	✓	✓			vectors statistics	
Business_ manager	dollars, cents, territory, salesman	✓	✓			gen_ledger, inventory, accts_payable, accts_receivable	helps manager as keep track o salesmen's com whereabouts
Statistics	variance, mean, std_dev	✓	✓	✓	✓	recursive_functions matrix_operations	basic stati or multiva
Calendar	time, data, week, day, month	✓	✓			temporal_math	supersedes by adding re

1. Hypothetical software catalog. Library components, called packages, extend the capabilities of Ada. Special data types, like vectors, and the valid operations on those types, like vector addition, can be overloaded into the normal operators (+, −, *, /).

machines. The software component permits the extensions themselves to be moved easily to new machines. Thus software components could very well revolutionize the industry, bringing the art of computer programming one step closer to a science.

Ada is also the first computer language to be fully standardized before commercial compilers were written for it. Most languages were designed for a specific purpose, like scientific calculations, where standardization was not an issue. Ada, however, was designed to be universal and standardized from the very beginning. In fact, the standardization committees of both the American National Standards Institute and Europe's International Standards Organization are now reviewing Ada's final specification document (see "The DOD moves for standardization"), which became available in July 1980. What's more, the Defense Department intends to enforce standardization by vigorously defending the use of the Ada name only for compilers that have passed its rigorous validation procedure. Thus, as with the qualification of a hardware part, each Ada compiler will be tested for correctness, as well as for complete compatibility with the original specification; if it does not pass, the DOD will not allow use of the name Ada.

With a validated compiler, users of different computers will be able to run the very same programs—not just similar, but identical. And as noted earlier, this ideal portability does not limit the language, since extensions may be added to any of those same programs—without introducing incompatibility—by plugging software components into the Ada bus.

The language

Ada has inherited much of its structured design from Pascal but with the addition of many constructs that expand its applications domain. It has the basic control statements and strong typing of Pascal, the block structure of Algol, and the exception handling of PL/1, to which it adds extensive real-time control facilities, as well as the concept of a software component.

An integral part of the Ada language is the program library that acts as the repository of those software components. The usefulness of the program library is that it allows programmers to concentrate on writing the main programs rather than on debugging their internal subroutines—thereby promising increased productivity for programmers. Placing components in the program library connects them to the software bus—that is, an Ada compiler.

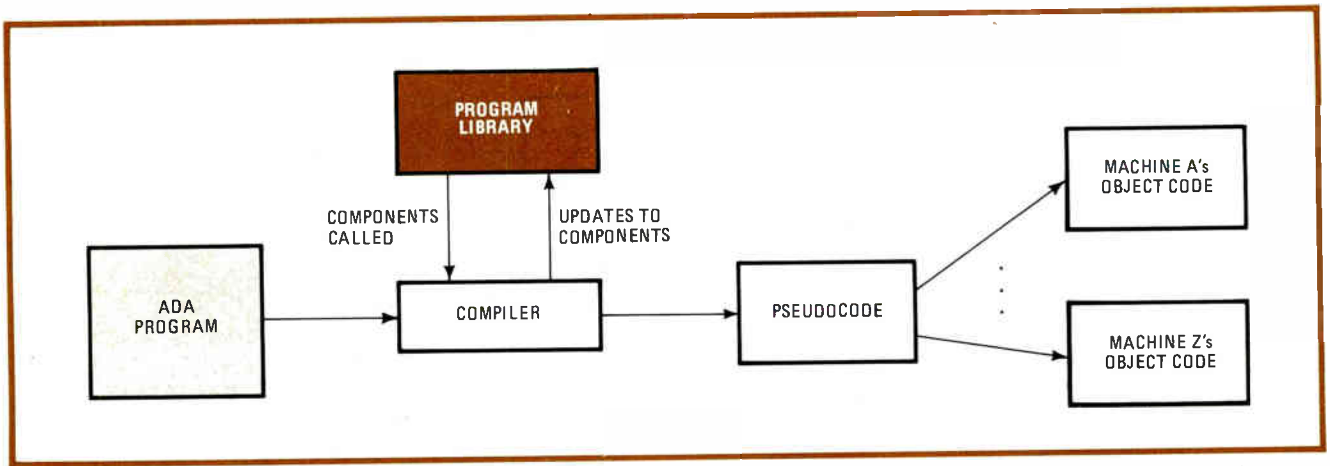
Ada is customized for the application at hand by including in the library those software components that define the data types and valid operations that are needed to solve a specific problem. On any given system, these components will be cataloged in the program library, which resides in a mass-storage device. The components consist of separately compiled modules that can be used by any authorized program to perform

The DOD moves for standardization

Ada's adoption as a U. S. and international standard is at least two and probably three or more years away. That is the consensus of officials at the American National Standards Institute (ANSI) and the International Standards Organization (ISO), both of which are still awaiting the Department of Defense to submit the list of computer language users it will canvas for comments on the new, inch-thick reference manual for Ada. After obtaining comments and developing responses to each, the DOD must formally submit these and its standardization proposal to both ANSI and the ISO, each of which will go through the process once again before a final vote.

"All told, it could mean that Ada's evolution will have taken a decade," says one DOD official, harking back to the beginnings of the high-order language program in 1975. That is when the military saw that it desperately needed a single, portable, easy-to-read language for multiple applications if software costs were to be kept under control. "Without exaggeration, the savings should run to several hundreds of millions of dollars annually," says one program specialist, "perhaps more with the reduced training and maintenance that Ada will make possible."

But what about the blessings of ANSI and the ISO? "We want them, of course, and will need them both if Ada is to find the widespread use that we would like to see among computer users generally," he says. "Yet we cannot forget that Ada was developed for military users first, and it *will* be implemented. Interest thus far has been so strong that it could well become a *de facto* standard regardless of what other actions are taken." **-Ray Connolly**



2. Separate but not independent. Components called by a user's program are linked to it at compilation time, and any updates to the library are done then. Most Ada compilers use an intermediate psuedocode that can be translated into the object code of any computer.

operations that would otherwise require separate subroutines. They are more than just subroutines, however, since they extend the capabilities of the language into specific application areas (Fig. 1). For instance, a vector package would define a one-dimensional-array data type that enables the normal plus and minus signs to add and subtract vectors.

In the library

The library is a collection of compiled units that are separate and largely independent of each other. The library file is submitted each time a program is compiled (Figs. 2 and 3); it is consulted and possibly updated by the compiler. Components that are called in by a program are linked to it at this time; also, new components or alterations to old ones are added to the library. Some library units will need periodic updating, like the system calendar that gives users access to the time and date. Most compiler projects are opting for compilation into a pseudocode that can be predefined for some imaginary machine. It is then a relatively simple step to translate this code into the native tongue of the target computer.

The library modules may be linked to a program by use of the "with" clause. For instance:

```
with VECTORS;
```

allows the program to use the vector data types and functions that are defined in that module. The programmer is free to use any of the modules that have been contributed to the library, and with a validated compiler users can acquire additional units from outside software houses, several of which are already gearing up to offer components. The vision of a software catalog for the Ada language that is continuously being expanded raises the hope that the science of software has truly come of age.

Inside the packages

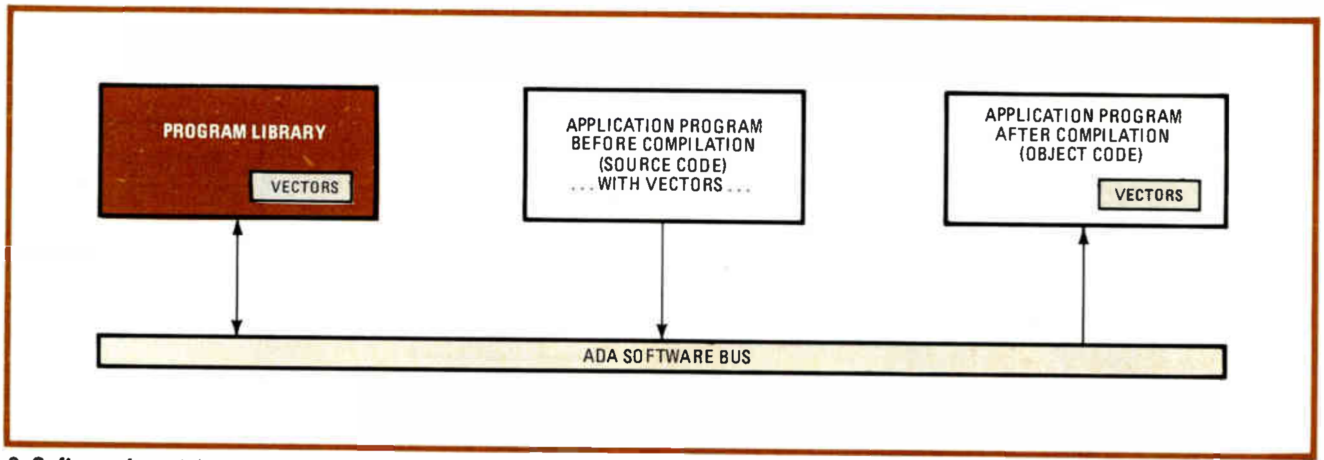
Within the primary software component, called the package, resides Ada's universality. Subroutines, called procedures, as well as several other program fragments, may be stored in the library as well, but the advantages of the package will cause it to become the basic type of component. A package encapsulates a group of related subroutines and data types into an isolated environment and thus can extend the capabilities of the language while maintaining tight control over its proper use. To that end, a separate interface portion of the package (Fig. 4) includes a specification of all the subprograms, functions, and variables that are accessible to the user.

The implementation, called the body, which contains the algorithms that perform the actual operation, can be hidden from the user of the package. Hiding is accomplished with the "body separate" clause, a feature that will enable software houses to supply the implementation portion in object-code form only, so as to protect their products. The hidden portion may use its own private data types and need not be the same from installation to installation so long as the interface portion is identical. This variability allows easy updating of software components without making past investments obsolete, since both the original and the updated version will perform properly. Presumably, however, the new package will execute the program faster, use less memory, or be optimized in some other way—perhaps by taking advantage of new hardware that has recently been added to the system. In this way, software components can be created by software houses and sold with the same kind of reliability assurances as hardware products. With a validated compiler serving as the system bus, the interface specifying its proper use, and the implementation hidden, software packages will likely be offered with guarantees of correctness—a most welcome advance in software engineering.

Overloading operators

Ada is unique in that a single operation can be expanded, or overloaded, so that it takes on different meanings depending on its context. For instance, the multiplication operator can be overloaded by adding a definition for vector multiplication. Then, whenever it is placed between two variables that are vectors, the compiler will ascertain from the context that vector multiplication is desired and will perform it. This process can be extended to subroutines as well, allowing several different procedures to have the same name. Each procedure is then invoked whenever the name is called with arguments of that procedure's respective type.

With generic procedures, on the other hand, variables



3. Software bus. Ada acts as a software bus into which both the user's programs and the software components contained in the library are plugged. Application programs that use "with" statements inherit new data types and operations during compilation.

of different types can make use of the same subprograms. These procedures may be stored in the library with their attendant variables left untyped. Then, at compilation time the variables that will access the procedure are specified and the generic procedure is appropriately recompiled.

Subprograms themselves can be either functions (that is, those returning one value only) or procedures. For procedures, the separate declaration part specifies the variables to be passed, designating them as inputs to the procedure, outputs from it, or both (Fig. 5). Furthermore, Ada also contains the statements that have become the familiar hallmarks of structured programming: BEGIN . . . END, IF . . . THEN . . . ELSE, LOOP, and CASE.

Real-time capabilities

A significant amount of the Ada compiler is devoted to the real-time concurrent programming environment. Task units are defined separately for each asynchronous process that is to be controlled, but execution is concurrent. Several mechanisms are provided by which tasks may communicate as well as keep track of external-world events like time.

Like packages, a task uses an interface portion that is separate from its implementation, or body. The interface portion of a task enumerates the entry declarations indicating how the task is activated. The task body includes the sequence of statements that perform the task at hand.

A rendezvous mechanism allows tasks to communicate with each other; one task acts as the server by containing an entry statement, and the other acts as the caller by using the name of the task's entry point. For instance, a task to write a line to a printer might contain in its interface the declaration:

```
entry PUT;
```

This declaration indicates that using PUT causes entry to this routine and is then followed by a task body that contains the statement:

```
accept PUT (L : in LINE);
```

This statement says that the code following it will put a line on the printer after accepting and storing it in local variable L of type LINE. The calling task will have a corresponding line like:

```
PUT ("HI THERE")
```

which will transfer the character string "HI THERE" to the task at the point where the accept statement occurs.

When execution reaches the accept statement, the server waits till the calling task reaches its PUT statement. Conversely, if the caller reaches its PUT statement before the server reaches its accept, then the caller will wait. In this way, a rendezvous is accomplished, either server or caller waiting for the other until both reach their respective lines referring to PUT.

Since many tasks may be operating in parallel and many of them may contain identical PUT statements, each entry declaration has a corresponding queue that stores the order in which the respective routines called the server task. They are processed first in, first out so that no callers will be locked out. The statement:

```
N := PUT'COUNT
```

will assign the number of waiting callers on the PUT task to the variable N, enabling a caller to determine what its position is in the queue.

Data types

Ada's strong typing is inherited from Pascal as a means of increasing the reliability of programs. At both compilation and execution times, extensive checking of types is done to ensure that no invalid assignments are made. For instance, the variables HEIGHT and WIDTH can be declared to be of type INCHES, whereas variable AREA is declared to be of type SQUARE INCHES. Then:

```
function "*"(HEIGHT : INCHES; WIDTH : INCHES)
  return SQUARE INCHES;
```

requires that all multiplication of inches times inches have results in square inches, and the compiler will check to make sure that this rule is adhered to. This is in strong contrast to most languages, which do not allow user-defined data types, so that no such checking is even possible. All variables that are used in a program must have their types declared, along with any operations on

```
package CALENDAR is
  type TIME is
  --define a data type called TIME
    record
      YEAR : INTEGER range 1901 .. 2099;
      MONTH : MONTHS_NAMES;
      DAY : INTEGER range 1 .. 31;
      SECOND : DURATION;
    end record;
  --define an enumeration data type called MONTHS_NAMES
  type MONTHS_NAMES is (JAN, FEB, MAR, APR, MAY,
      JUN, JUL, AUG, SEP, OCT, NOV, DEC);
  function CLOCK return TIME;
  --overload the "+" and "–" operators
  function "+" (A : TIME; B : DURATION) return TIME;
  function "–" (A : DURATION; B : TIME) return TIME;
  function "–" (A : TIME; B : TIME) return DURATION;
end CALENDAR;
--end of interface portion
package body CALENDAR is separate;
```

4. A predefined package. One package that will be supplied with all validated compilers is a calendar that works with a real-time clock. The plus and minus signs must be redefined for temporal calculations so that, for instance, a time minus a time yields a duration.

them that do not result in the same type (like inches times inches yielding square inches).

A type, then, is not only a set of values, but also a set of valid operations on those values. If a violation of these rules occurs, it will always be detected: incorrect type assignments at compilation time, and incorrect value assignments at execution time. It should be noted, too, that types are not the same just because their values can be; for two variables to be of the same type they must be explicitly declared as such.

Several types are predefined: integer, real, floating-point, character, boolean, array, string, enumeration, record, and access. Others may be defined explicitly by the user or may be built up from the predefined ones.

With the enumeration type, the specific values of a variable can be listed—for example:

```
type DAYS_OF_WEEK is
  (SUN,MON,TUE,WED,THU,FRI,SAT);
```

This enumeration restricts variables of the type DAYS_OF_WEEK to the seven strings specified. A subtype may be derived from this one by limiting its range—for instance, by:

```
type WEEK_DAY is DAYS_OF_WEEK
  range (MON .. FRI)
```

which restricts WEEK_DAY data types to the normal weekday range.

Record types allow different but related values to be grouped together and called by a common name. For example:

```
type DATE is
  record MONTH : MONTH_NAME
         DAY : INTEGER range 1 .. 31
         YEAR : INTEGER range 0 .. 2000
  end record;
```

```
procedure QUADRATIC_EQUATION (A, B, C, : in REAL;
                              ROOT_1, ROOT_2 : out REAL);
--enter the equation's coefficients and return its roots
  RADICAL : REAL
--now find the equation's roots
begin
  RADICAL : = (B**2) – (4.0*A*C);
  ROOT_1 : = (–B + SQRT(D))/(2.0*A);
  ROOT_2 : = (–B – SQRT(D))/(2.0*A);
end QUADRATIC_EQUATION;
```

5. Typical subroutine. The procedure subroutine lets any number of arguments pass between it and the calling program. The quadratic equation solver shown requires three coefficients (Ax^2+Bx+C) as inputs and two outputs corresponding to the roots.

permits variables of type DATE to be assigned values like WWII := (SEP, 1, 1939). If any attempt is made to assign values outside the specified range (like the thirty-second day of the month) a constraint error will be raised at execution time. In addition, elements of a record type can be accessed by dot notation, so that, say, WWII.MONTH picks out SEP as the month in which World War II started.

Imposing restrictions

A type may have its proper values and operations restricted in any way defined by the user by including what are called discriminants. These impose certain conditions to be checked by the compiler at both compilation and execution time. The example:

```
type SQUARE_MATRIX(I : INTEGER) is
  array (I,I) of REAL;
```

restricts the values of type SQUARE_MATRIX variables to ones that are really square by using the single discriminant I for both its dimensions. Even more complex data structures, called composition types, can be built up as well. For example, two square matrixes can be combined in a single record if they are assigned thus:

```
type DUAL_SQ_MATRIX (I : INTEGER) is
  record
    LEFT : SQUARE(I);
    RIGHT : SQUARE(I);
  end record;
```

That defines a DUAL_SQ_MATRIX to consist of a left and right portion, each of which is a square matrix as previously defined.

Once a type has been defined, objects (variables) may be declared using the notation:

```
MAT_2 : SQUARE_MATRIX
```

which now restricts the values that variable MAT_2 can take on to be square matrixes.

Exception handling

Ada has the ability to recover from execution time errors in a manner similar to PL/1. Whenever an error is encountered, an exception is raised, several of which are predefined, like CONSTRAINT_ERROR and NUMERIC_ERROR. To prevent execution from stopping when the exception is raised, a handler may be added by the user.

```
task DISK_HANDLER is
--define two entry points for data to and from the disk
  entry READ_DISK (A : out TRACK);
  entry WRITE_DISK (B : in TRACK);
end;
--end of interface portion
task body DISK_HANDLER is
begin
  loop
    select
    --either read or write
      accept READ_DISK (A : out TRACK) do
        GET_FROM_DISK (A);
      end;
      --external subroutines perform the reads and writes
    or
      accept WRITE (B : in TRACK)
        SEND_TO_DISK (B);
      end;
    else null;
    --if no reads or writes are waiting,then continue
    end select;
  end loop;
  --repeat
end;
```

6. Multitasking. The disk handler lets any program write or read a track of the disk, but not both simultaneously. "Select" and "or" statements allow only one alternative at a time. The "else null" clause causes exit from the select segment.

For example, to prevent a numerical error from being raised when a division by zero is performed, the following function may be used:

```
function "÷" (U,V : REAL) return REAL is
  begin
  return U/V;
  exception
    when NUMERIC_ERROR = >
         return REAL'LARGEST
  end;
```

Now, whenever two real numbers are divided with an out-of-bounds result, rather than causing the program to crash, the exception handler returns the largest value representable on the machine.

Current projects

Already, the race to produce Ada compilers is on. Many universities have experimental versions, but they are not intended for industrial users. At a conference held by the Association for Computing Machinery in Boston in December 1980, many companies said that they have programs in Ada ready to go as soon as compilers become available. General Electric, for instance, has Ada programs in hand that control one of its microwave ovens. Many are also working to ready test and validation programs for these compilers.

The first commercial compilers to appear will be for microprocessors. TeleSoftware Inc., a new company in San Diego, Calif., headed by Ken Bowles, the creator of UCSD Pascal, is working on a first quarter 1981 release of a compiler for a subset of Ada that runs on the Microengine from Western Digital Corp., Newport Beach, Calif. [*Electronics*, Jan. 13, 1981, p. 39]. It also plans to be the first clearinghouse for software components and undertook the compiler project to get started. In fact, Western Digital, part owner of TeleSoftware, is producing an Ada Microengine employing special microcode optimized for Ada. This compiler will also work with systems based on the S-100 bus now that the WD chip set is available for the bus [*Electronics*, Jan. 13, 1981, p. 290]. Others are reportedly working on implementations for the 68000 and the Z8000 microprocessors, though these are certainly a good way off.

Intel Corp., Santa Clara, Calif., will be offering an Ada-based microprocessor chip set in the near future, called the iAPX-432, that mirrors the structure of the language in its hardware. The iAPX-432 has been designed from the ground up with Ada in mind. In fact, Ada is its system implementation language, and the first validated compiler may well be from Intel, which appears to have a head start here, too.

The first Department of Defense contract for a compiler was granted by the Army to SofTech Inc. The Waltham, Mass., company has been asked to produce a full Ada compiler for Digital Equipment Corp's VAX-11/780. Preliminary versions of the compiler should be ready in 1981, though the validation process will probably hold up final delivery till 1982.

The other major DOD effort comes from the Air Force, which has granted three preliminary contracts to Texas Instruments, Intermetrics Inc., and Computer Science Corp. It will choose one of these companies to develop a full Ada compiler for IBM computers next year.

The designer of the language, Jean Ichbiah has formed his own company, named ALSYS, in Paris, which is currently working on a front-end compiler for CII-Honeywell Bull's and Siemen's computers.

Many implementations will compile Ada source statements into an intermediate code that can then be translated into the machine code of the target computer. Several manufacturers will be looking at these compilers as possible front ends for their own implementations. Joseph Rowe, vice president of research and development at the Harris Semiconductor Group's Minicomputer division, believes that "Ada will replace Fortran," and consequently the Melbourne, Fla., company is one of those already working on test programs to help evaluate compilers as they become available. Another minicomputer effort, for Data General's machines, is being undertaken by Application Software of Johannesburg, South Africa. And Westinghouse Electric Corp.'s Defense and Electronic Systems Center in Baltimore is working on an Ada-to-Fortran-77 translator for Sperry Univac, Burroughs, IBM, Honeywell, DEC, and Control Data computers.

However, most of the major minicomputer and mainframe manufacturers appear to be holding back from full-fledged compiler projects. Those with major defense contracts are training programmers, but they are not committing the funds necessary to write a full Ada compiler and validate it. Says Mary Van Duesen, editor of the Ada Implementor's Newsletter, "All of them will eventually go to Ada, it's just a matter of whether they take the first or second wave of customers." □

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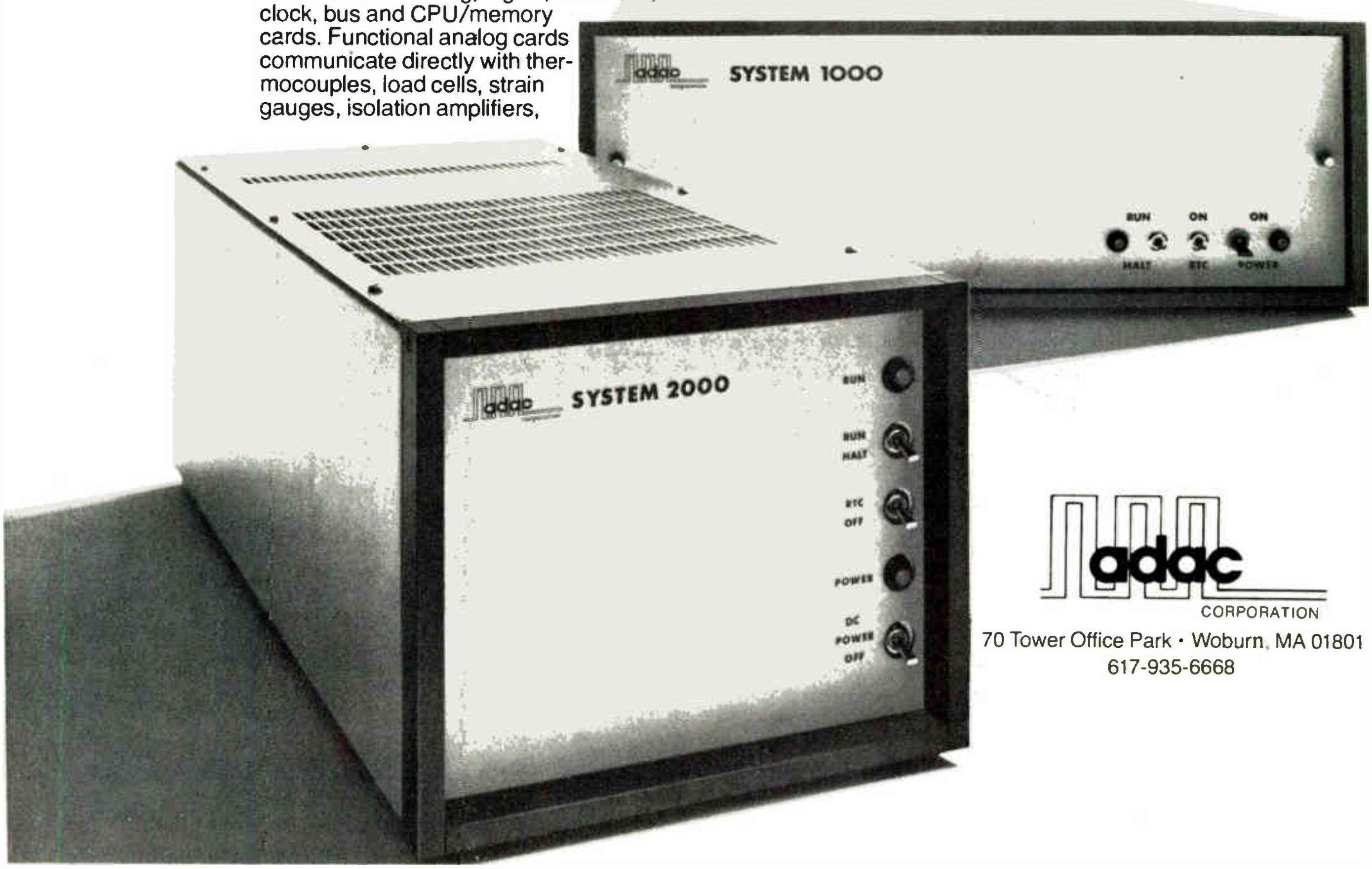

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On-chip transistors add versatility to op amp

by Jim Williams
National Semiconductor Corp., Santa Clara, Calif.

Low-cost audio-amplifier chips containing uncommitted transistor arrays are widely applicable, as discussed in part 1 of this article [*Electronics*, Jan. 27, 1981, p. 118]. Besides uses in nonaudio applications such as dc-dc converters, touch switches, and stabilized frequency standards, array amplifiers like National's LM 389 are especially suited for general service in portable oscilloscope calibrators, low-distortion oscillators, and logarithmic amplifiers.

For example, the circuit in Fig. 1 allows a quick check of an oscilloscope's time base and vertical calibration. It can be built into a small hand-held enclosure and may be powered by a 12.5-volt battery.

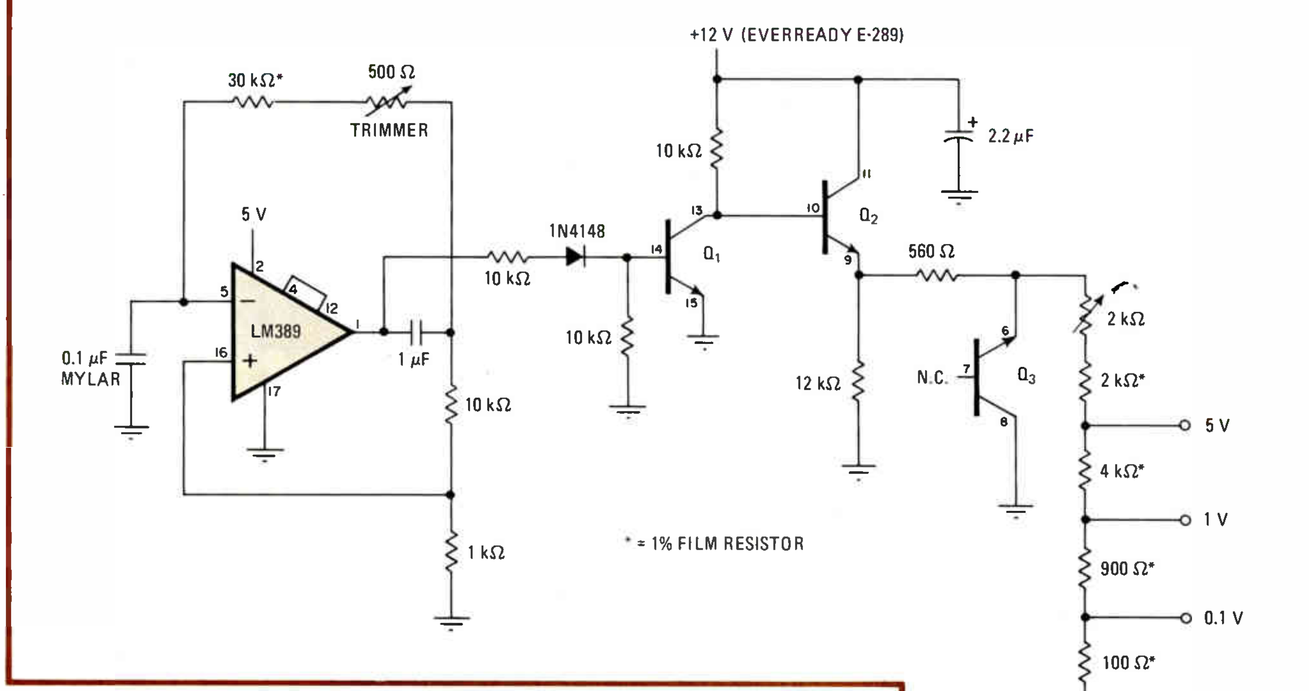
When suitably trimmed, the amplifier will oscillate at 1 kilohertz ± 5 hertz. Transistor Q_1 serves as a switch to provide fast, sharp edges to Q_2's base. This transistor drives Q_3, which functions as a zener diode so that a relatively constant 10-V square wave is applied across the resistive divider at the output. Q_3's breakdown potential is scaled by the 2-kilohm potentiometer to provide a 5-, a 1-, and a 0.1-V square wave at the appropriate output taps. Loading of the circuit by a 1-megohm oscilloscope impedance will not introduce any appreciable error.

In Fig. 2, the LM389 is called on to provide a low-distortion sine wave and a synchronous in-phase square wave. The circuit's 0.25-watt output capability enables it to drive such loads as a transducer bridge. In such an application, the in-phase square-wave output can be used to drive a set of synchronous demodulation switches.

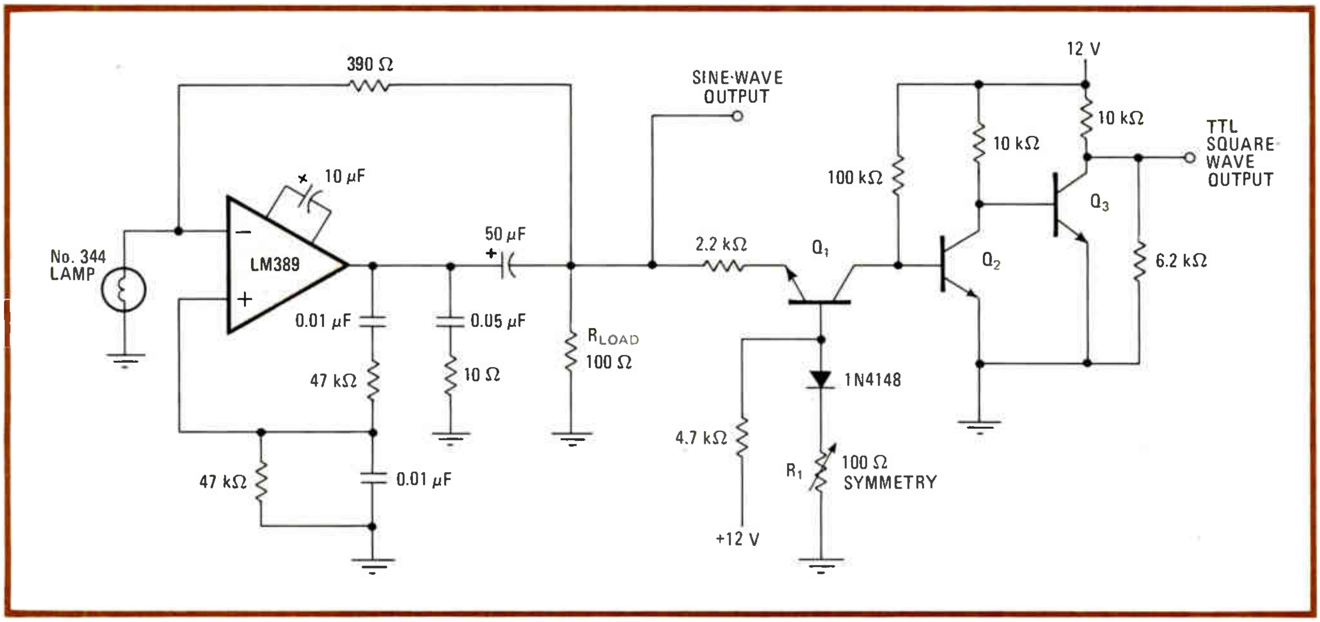
The oscillator's low distortion (0.2%) is directly traceable to the use of a light bulb that provides smooth amplitude-limiting for the Wien-bridge network of the amplifier. The oscillation frequency is 1 kHz. The in-phase square-wave output is ensured by Q_1–Q_3 and the potentiometer R_1, with Q_2 and Q_3 speeding up the waveform's edges. Calibration for synchronism is simply performed by adjusting R_1 so that the edges of the square wave line up precisely with the zero-crossings of the sine-wave output.

As shown in Fig. 3, the LM389 is used in an unorthodox fashion to build a logarithmic amplifier that eliminates the complex and expensive means by which temperature compensation is usually achieved. Thus, the cost of the log amp is reduced by some 90% compared with that of conventional approaches.

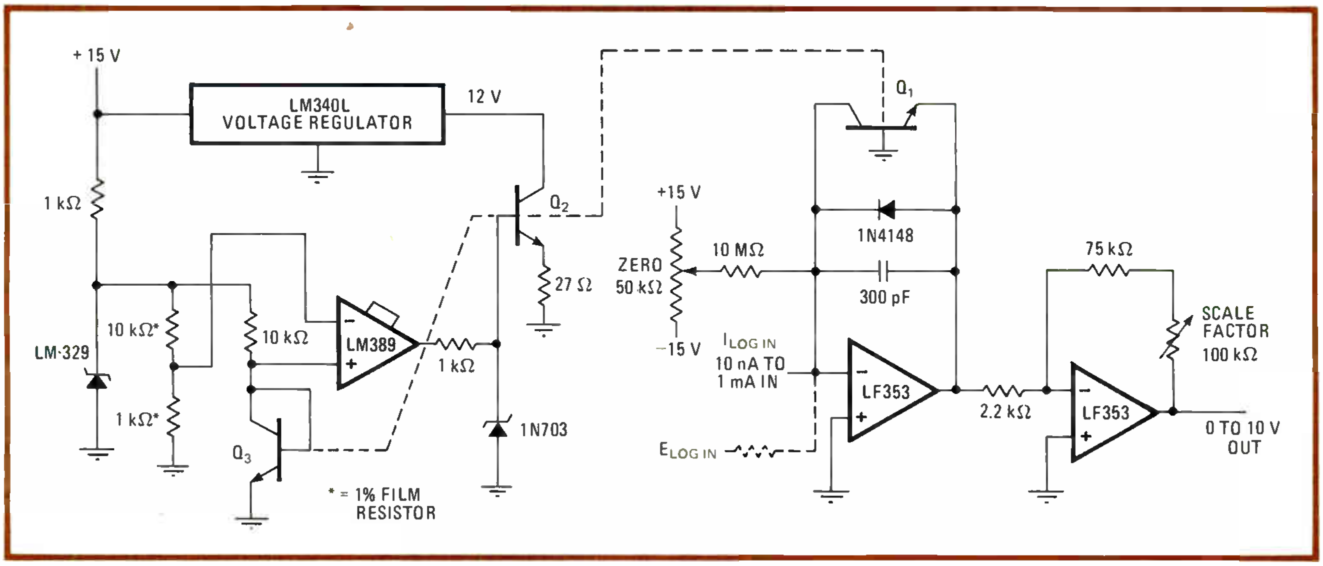
Q_2–Q_3 operate in a heat-generating and -sensing feedback network, with Q_2 serving as the heater and Q_3 the temperature sensor. This combination keeps the temper-



1. Calibration. The LM 389 array audio amplifier supplies 1-kHz markers at 0.1, 1, and 5 V for an oscilloscope. Loading caused by connecting scope is minimal. The unit can be comfortably powered by a 12-V battery for field applications.



2. Sines and squares. This oscillator provides a 1-kHz sine-wave output and synchronous in-phase square waves. The amplitude-limited Wien bridge contributes to low distortion (0.2%). Single-knob calibration for synchronization is provided by potentiometer R_1.



3. Holding heat. The LM389's servo loop, Q_2–Q_3, performs low-cost temperature compensation for the LF353 op amp, which is configured as a logarithmic amplifier. The chip temperature, initially determined by current through Q_2, is set with the 1-kΩ-to-10-kΩ resistive divider.

ature virtually constant, so that the LF353 op amp's transfer function, as determined solely by logging transistor Q_1 and the 1N4148 diode, will be independent of any variation in temperature.

When power is first applied, Q_2's emitter voltage rises to about 3.3 V and a current of 120 milliamperes flows. This current forces Q_2 to dissipate about 1.5 W, which raises the chip to operating temperature very rapidly because of its small size. At this time, the thermal servo Q_2–Q_3 takes over, because the LM389 senses the dependence of Q_3's base-to-emitter voltage drop on temperature and drives Q_2 to a temperature (50°C) corresponding to the setting of the 10-kΩ-to-1-kΩ divider string. Since the LM340 never has a voltage of more than 3 V across it, the power dissipation never exceeds 0.3 W. Note that the zener diode at the base of Q_2 will prevent servo lock-up when the circuit is initialized.

To calibrate the temperature servo, the base of Q_2 must first be grounded. The collector potential of Q_3 must then be measured at a known room temperature. Calculate what Q_3's potential should be at 50°C, assuming a temperature coefficient of −2.2 millivolts/°C. Next, trim the 1-kΩ resistor in the resistive divider so that the voltage at the LM389's inverting port approximates the calculated potential. Finally, unground Q_2's base. The Q_2–Q_3 servo loop should then be functional. As a check, note Q_3's collector voltage stability (within 100 mV) and temperature change (0.05°C maximum) as cool air is applied to the LM389. □

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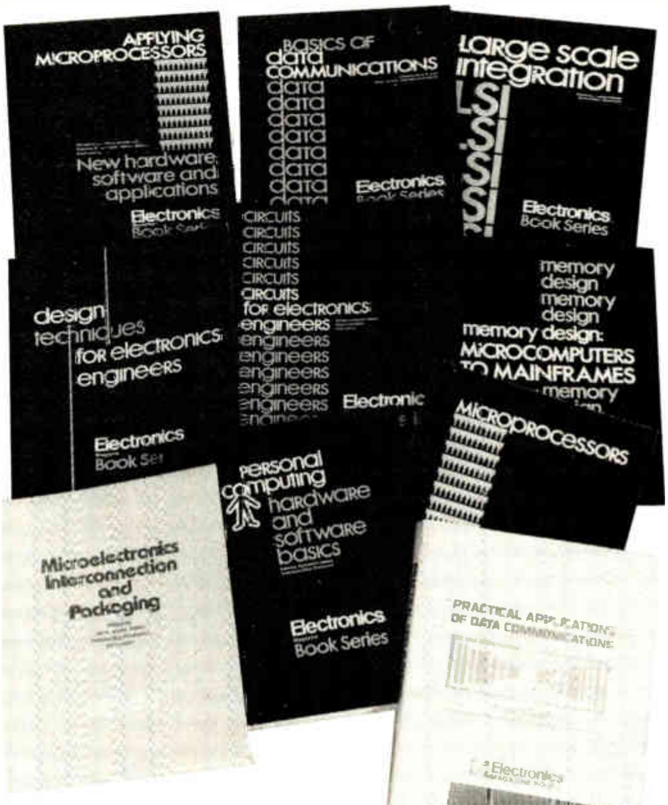

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Serial-data interface eases remote use of terminal keyboard

by Robert Nixon
Nixon Engineering Co., San Jose, Calif.

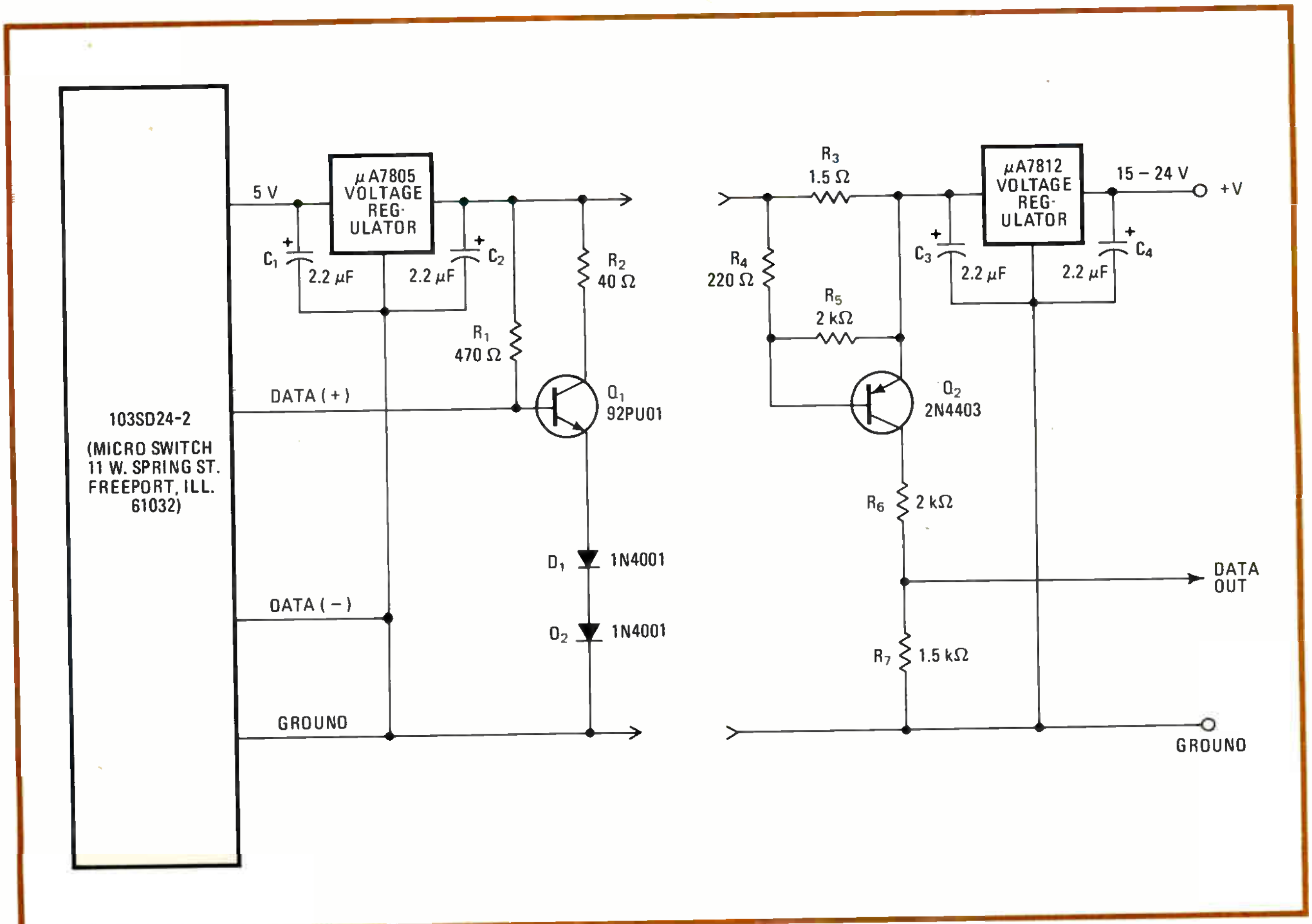
A keyboard that can be detached and operated at a distance from its terminal is often desirable in a computer-based system, but the job of developing the proper cable and connector can be hard and time-consuming. The interconnecting wire count can be reduced to just two leads, however. The trick is to choose a keyboard that generates a serial output for each keystroke and use it with the current-modulating interface shown. A minor modification will adapt the circuit to the RS-232 bus.

Here, the microprocessor-based keyboard is the Micro Switch 103SD24-2, which delivers the serial ASCII data at 110 bits per second. Power to the keyboard, which requires only 5 volts, is provided by the μA7812 voltage regulator. This device also serves as a current limiter, protecting the interface against damage caused by shorts in the connecting cable. A second regulator, the μA7805, smoothes out the small variations in voltage generated by the current modulator.

During the mark states of the data stream, transistor Q_1 is held off because the keyboard output is active—the total current through R_1 and the keyboard is 360 milliamperes, which represents the difference between the supply voltage and the keyboard's optocoupler output stage. During the space interval of the serial data stream, the keyboard output is inactive, and Q_1 is turned on. The total supply current then becomes 610 mA. Diodes D_1 and D_2 allow for the small voltage drop between the Darlington-coupled output of the keyboard, ensuring that Q_1 is switched properly. Capacitors C_1 and C_2 aid in stabilizing the μA7805 regulator during modulation.

The two-state current variation is detected on the receiver side by Q_2, and associated resistors R_3–R_5. During the mark state, the drop across R_3 is about 550 millivolts, which is not enough to turn on the transistor. During the space state, however, the additional current produced will switch on Q_2 and generate a positive voltage level at the output. Note that R_4 and R_5 prevent the transistor from being damaged by a short circuit.

For TTL compatibility, the output signal should be introduced to a Schmitt trigger to eliminate hash and ill-defined switching levels. To interface with the RS-232 bus, it is only necessary to increase R_7's value to 3 kilohms and connect its lower end to −12 V instead of ground. □



Interim link. Two-wire serial interface makes it simple to remove keyboard from computer terminal for remote use. ASCII output from keyboard is current-modulated by Q_1. Two-state output is recovered by Q_2. Minor modification makes board compatible with RS-232 bus.

BUBBLE MEMORY SYSTEMS

Control chip and driver program unlock magnetic-bubble potential

Controller runs 5-chip systems as well as disk replacements

by Ravi Luthra and George Reyling Jr.
National Semiconductor Corp., Santa Clara, Calif.

Magnetic-bubble memories must interface easily with bus-level signals if they are to win wide acceptance among designers. The first of these two articles describes a controller chip that does just that: links the bubble chip to the system bus in hand-held and large systems alike.

Perhaps more significant, however, is the second article, which tells how a software-assisted bubble memory can be made to look just like floppy-disk mass storage to a host microcomputer system. Eventually the garnet-based devices will go head to head against disks for high-density nonvolatile storage and turn up, surrounded by control circuits, in cartridge form. **-Raymond P. Capece**

☐ Though readily available, magnetic-bubble memories have met with a cool reception. The circuitry needed to control them is very complex—anywhere from 40 to 100 standard integrated circuits may be needed to manipulate a 256-K or 1-megabit bubble device.

That component count is reduced by an order of magnitude by a set of special-purpose support circuits that make it easier to exploit the technology's unique combination of nonvolatility, solid-state reliability, and high density. A well-designed controller IC is the key element. National Semiconductor Corp.'s INS82851/3, for instance, is powerful enough to run large, high-performance memory systems yet versatile enough to drive a single bubble memory with as few as five chips.

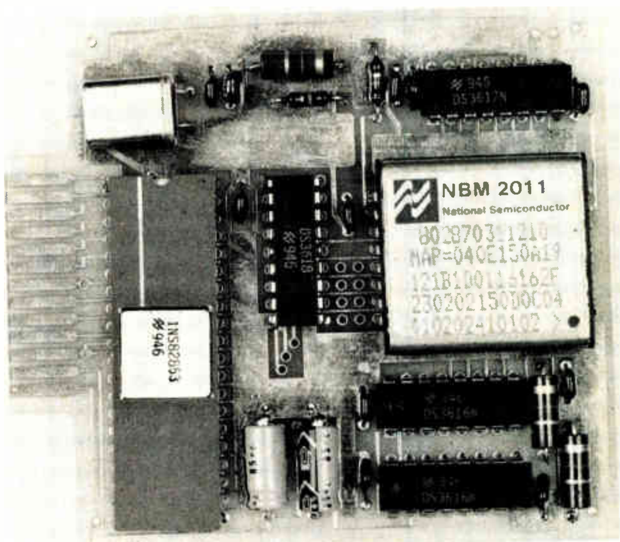
The problem with a bubble memory chip is that addresses are not inherent in its structure and the existence of redundant loops of magnetic bubbles has to be taken into account. In many respects it resembles a head-per-track disk or drum memory with serial input and output. The bubble chip's contents must be shifted during initialization until the synchronizing pattern is found that marks the starting address. Also required is a redundancy map, which must be read out to determine the usable data loops: every read or write operation sequences the bubble memory contents through several hundred or more clock cycles, using the map to avoid redundant loops.

In addition to those tasks, the control subsystem must take charge of the interface with the host system bus and must buffer parallel data on the way into the bubble memory and serial data on the way out. It should also detect and correct errors, sequence power-up and power-down operations, and time the various signals.

Finally, all these functions should be partitioned among the controller and other support chips in such a way as to create a versatile subsystem, capable of use in applications as diverse as a hand-held order-entry system, an industrial data logger, or a high-performance disk replacement in a large computer system.

The controller

In partitioning the control functions, a good starting point is to note that drive and sense circuits must accompany each bubble memory device, whereas the controller can be shared among many bubble devices. If all the



Packed. The power of the large-scale integrated controller chip (at left) is evidenced by the smallness of this minimum-configuration magnetic-bubble memory subsystem. Though it is only 9 square inches in area, the board can store either 256 K or 1 megabit.

complex logic needed for a minimum control system is put into a single n-channel MOS large-scale IC, then the drive and sense chips can be designed to be simple and therefore low-cost.

This approach produces the support circuitry shown in Fig. 1. The design of such a minimum configuration uses the least number of components consistent with keeping their individual cost low.

The controller, for instance, stores maps of redundant loops for one magnetic-bubble memory module but does not go to the expense of doing so for the eight modules of a full system. It is much more cost-effective to use a standard random-access-memory package and counter in large systems, where the extra packages have little impact on circuit-board size.

Also economical is a microprogrammed architecture that provides the INS82851 with the logic needed to run a 256-K bubble memory and the INS82853 with the logic for a 1-Mb memory. Microcoding at the time of manufacture characterizes the controller. A hardwired approach providing both would have been more costly and more complex and would in addition have produced a die larger than the 82851/3's 40,000 square mils.

Controller functions

Figure 2 is a block diagram of the 82851/3. The Microbus control circuitry and the input/output buffers employ address, data, and control signals at the user interface that are compatible with most microprocessors' requirements. The source and destination registers are accessible by the user, who writes into them or reads from them to operate the controller. First-in, first-out memory is a 16-byte buffer for data flowing between the user and the magnetic-bubble memory; the FIFO compensates for the difference in the data rates between the controller's interface with the user and its interface with the bubble memory. Then, during writing, the parallel-to-serial register converts the user's byte-parallel data into a serial bit stream. Conversely, during reading, the serial-to-parallel register converts the serial stream of bubble data into bytes for the user.

The circuitry for detecting and correcting errors employs a 12-bit Fire code. This code can correct single bits or pairs of adjacent bits it has found to be in error. It is also capable of detecting up to three random errors or a burst error up to 12 bits long.

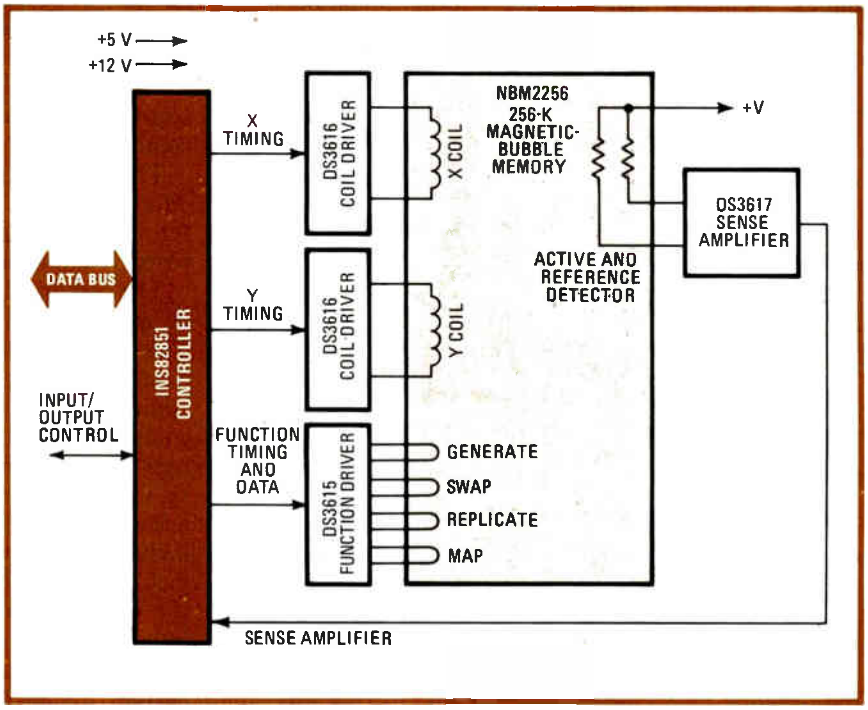
Redundant loops

National's NBM2256 256-K bubble memory contains 282 data loops of which 20 may be redundant. The NBM2011 1-Mb bubble contains 584 data loops of which 60 may be redundant. Each loop contains 1,000 bits. When writing, the output-mapper circuitry in the controller stores user data only in known-good loops; then when reading, the input mapper automatically ignores the data coming from redundant loops. The mask-programmable timing generator supplies all the signals necessary to operate the support circuitry. The microcoded control section contains the microcode for executing the user commands.

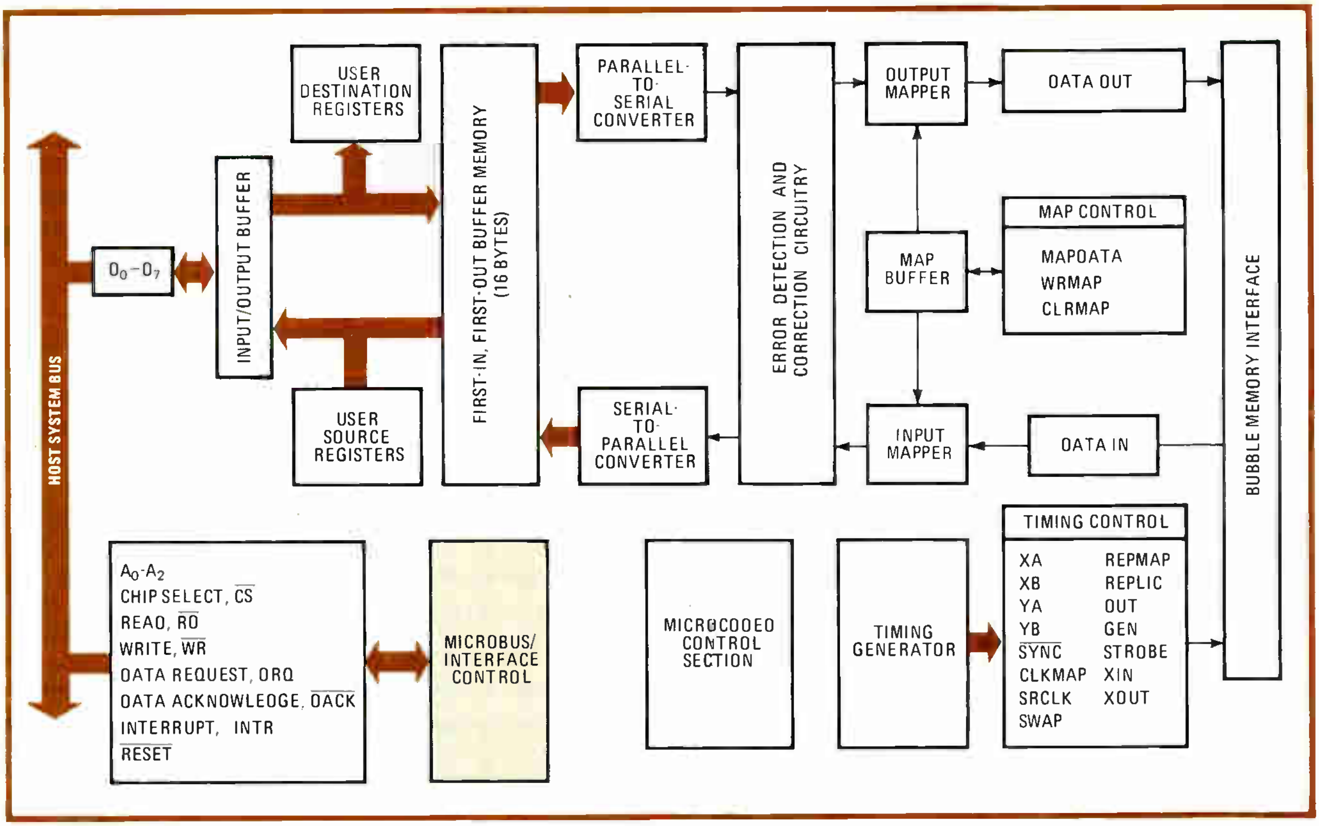
The user operates the controller by writing into or reading from the registers shown in Table 1. The user issues a command to the controller by writing into the command register (CMDR). The status of the controller is determined by reading the status register (STR), whose bits indicate if it is busy and reveal its data-transfer status as well as a variety of error conditions.

Various options can be written into the residual control register (RCR). They include:

- Write protection, which inhibits all write operations.
- Sector addressing, which keeps the sector size constant regardless of the number of bubble memories.
- Interrupt enabling, for requesting data when the FIFO is half full or has 1 byte empty, for stopping when the



1. Six chips only. The design of the INS82851 bubble-memory controller keeps costs low for minimum systems, since only it and four linear integrated circuits are needed to provide bubble–to–microprocessor-bus interfacing. Also, the controller supports either 256-K or 1-Mb bubble chips.



2. High density. The chores of the controller, which accepts user programming, oversees error detection and correction, and has bus interfacing as well as bubble timing functions, are so complex that the 40,000-mil² chip is denser than many microprocessors.

command is complete, or for stopping when an error is detected.

■ Read-FIFO enabling, which gives access to the FIFO when a command is not being executed.

The control system is configured by loading the system features register (SFR). This specifies the number of bubble memories and whether a programmable read-only memory for mapping redundant loops is to be used. It also includes a fast-access bit to indicate that data should be held in the bubble memory's output track for immediate access.

Next, the sector-address register (SAR) holds the logical address of the sector or page being accessed. Finally, when the user wants to read or write more than one sector (or page) of data at a time, the contents of the multiple-sector register (MSR) specify the number of sectors (pages) to be read or written.

Versatile commands

The 82851/3 controller provides a comprehensive set of user-oriented commands with options that further increase their power. Table 2 contains the format of the command code and a summary of the status register's formats for each of the commands.

The commands to read sector(s) allow the user to read one or more sectors. The user may either read all the data from the bubble memory or skip the data in the redundant loops. Alternatively, the controller may read data from the bubble memory using the redundancy map information but not send it to the user—that is, the data-request line (DRQ) is not raised. In this way, the integrity of the data may be verified without using the system bus, since the controller corrects erroneous data whether or not it is sent to the user.

The user may write data into one or more sectors by using write-sector(s) commands, through which he can write data either into all the loops in the sector(s) or into all except the redundant ones. Further, data present in the FIFO may be written repeatedly until the specified number of sectors have been written. A data error detected during the execution of a command to read sector(s) may be corrected by issuing a read-corrected command.

The position command aligns the bubble memory's output track with the controller's counter in preparation for reading or its input track with the counter in order to write. It can thus reduce latency to zero.

The command to read the map acquires the redundancy map information (RMPI) from the bubble memory. This gives the user an option to examine the map-loop data in its entirety and to make a hard copy of it. In addition, he can check the integrity of the RMPI by comparing it with the information in the map RAM. The user may also write his own RMPI into the bubble memory, using the command to write the map and storing it in either the odd or even map loop. (The 2256 and 2011 include a redundant map loop to further increase their yield and reliability.) Alternatively, the RMPI read from the bubble memory's redundancy map may be loaded into the map RAM.

Issuing a command to terminate halts the command currently being executed by the controller. The user may

TABLE 1: USER REGISTERS OF THE INS82851 BUBBLE-MEMORY CONTROLLER					
Name of register	Symbol	Address			Source or destination
		A_2	A_1	A_0	
Command register	CMDR	0	0	0	D
Status register (read only)	STR	1	1	0	S
Residual control register	RCR	1	0	0	S/D
System features register	SFR	1	0	1	S/D
First-in, first-out memory	FIFO	1	1	1	S/D
Sector address register, bits 0-7	SAR 0-7	0	1	0	S/D
Sector address register, bits 8-15	SAR 8-15	0	1	1	S/D
Multiple sector register	MSR	0	0	1	S/D

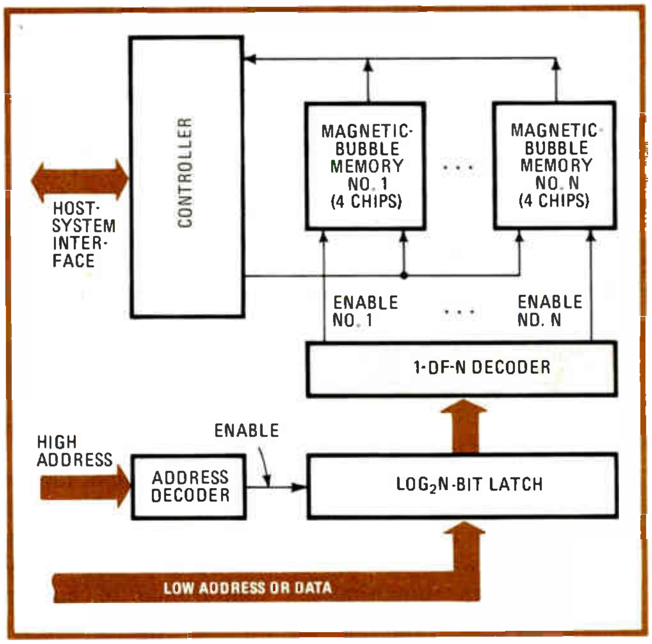
specify whether the command currently being executed should be terminated immediately or at the end of the current page.

All the bubble memories in a bank are initialized on power-up, and the controller also contains a command that lets the user initialize them under program control. All the memories in a currently active bank are rotated simultaneously so that the controller's internal counters can be synchronized with each of their page 0s.

The smallest system

The controller and other support circuits may easily be configured for hand-held or portable applications. Though packed on a board of only 9 square inches, the subsystem (shown in the opening photograph) stores either 256 K or 1 Mb, can detect and correct errors, has a FIFO buffer, and uses an 8-bit-wide parallel data interface with all the control signals required to transfer data under program, interrupt-driven, or direct-memory-access control. The subsystem requires +5-V and +12-V supplies and dissipates approximately 4 watts when operating and 1.5 W during standby.

When used as a removable cassette, the board has a standard bus interface, which plugs into a variety of host systems regardless of the electrical characteristics of the particular bubble memory being used. That is a simpler approach to system design than one that uses only the bubble memory as a removable cassette. Because the 256-K and 1-Mb systems are pin-for-pin-compatible with each other, cassettes of either capacity can be used interchangeably, provided that system software reads the size information from the bubble memory.



3. System expansion. With a multiplexing approach, one controller may handle as many bubbles as signal-loading limitations allow it to. Multiplexing saves power, since the bubble and support circuits dissipate only one fifth of the power they consume when active.

To expand such a system, extra bubble memories may be multiplexed or linked in parallel to each other with the controller.

In the multiplexed approach (Fig. 3), each bubble memory and its four drive/sense circuits are individually enabled by a decoder from a few bits of latched data, which may be sent over either the address or the data bus. The host system selects a particular bubble module and the controller executes an initialize command before transferring data. It typically takes about 10 millisec-

TABLE 2: COMMAND AND STATUS REGISTER SUMMARY																
Command name	Command register								Status register							
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
Read sector (s)	0	0	0	MS	RDM	SSD	0	0	0	0	out of range	0	error detected	data overrun	data request	controller not busy
Write sector (s)	0	1	0	MS	WRM	SAD	0	0	0	write protect	out of range	0	0	data overrun	data request	controller not busy
Position	0	W	1	0	1	0	0	0	0	0	0	0	0	0	0	controller not busy
Initialize	1	1	1	1	LM	1	0	0	0	0	initialization error	0	map data error	0	0	controller not busy
Terminate	0	0	0	0	0	0	1	I	same as the status of the terminated command							
Read map	1	0	0	0	C	0	0	0	0	0	map compare error	0	map data error	data overrun	data request	controller not busy
Write map	1	1	0	0	M	0	0	0	0	write protect	0	0	0	data overrun	data request	controller not busy
Read corrected	0	0	0	0	1	1	0	0	soft errors present	0	0	error not correctable	additional error detected	data overrun	data request	controller not busy

Note: MS = multiple sector; RDM = read with masking; SSD = skip sending data; SAD = skip requesting data; WRM = write with masking, W = position for a write operation; LM = load map into RAM; C = compare with map RAM; M = write into odd map; I = terminate immediately.

Number of packages / Capacity (K-bytes)	Magnetic-bubble memory	Controller	Magnetic-bubble memory interface	Map	Bus interface	Total	Ave. kb/pkg.
32(128)	1	1	4	0	0-12	6-8	36(146)
64(256)	2	1	8	0(4)	0-5	11-20	36(136)
128(512)	4	1	16	4	5-8	30-33	32(128)
256(1 megabyte)	8	1	32	4	5-12	50-57	39(151)

TABLE 3: NUMBER OF PACKAGES REQUIRED BY SYSTEMS USING PARALLEL 256-K (1-MEGABIT) MAGNETIC-BUBBLE MEMORIES

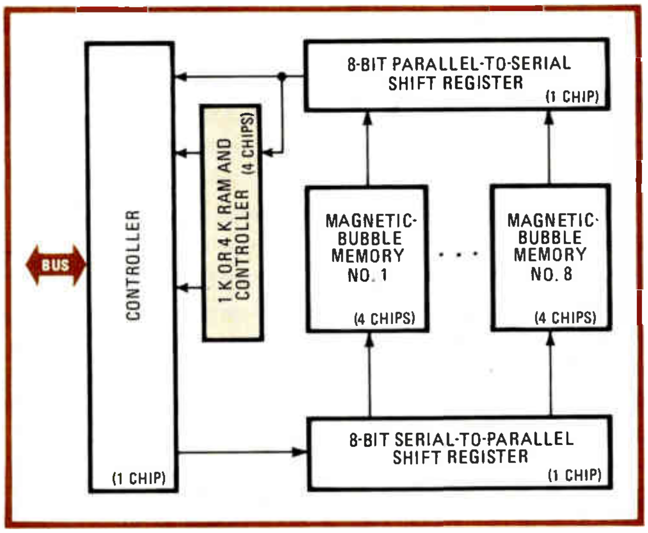
onds to initialize a new bubble module, so that the worst-case access time, for a system in which an inactive module is accessed, increases by 10 ms. However, the average access time increases very little, since most accesses will be to the currently active module.

The multiplexed approach has the advantage of lowest power dissipation, since inactive modules and drive/sense circuits need about 80% less power when inactive than when active. It also allows an arbitrary number (within signal-loading limitations) of bubble modules to be controlled by a single controller.

In parallel

The second way of expanding a system is to operate two, four, or eight bubble memories in parallel (Fig. 4). This is done by using a pair of 8-bit shift registers to convert the serial data from the controller into parallel inputs for the parallel bubble modules. Redundancy is easily handled by the controller, since the redundancy map storage can be expanded off chip onto a 1-K or 4-K RAM by means of three 4-bit counters. This scheme has only minor impact on total chip count, board area, and cost of a multimodule system; in fact, overall components cost is less than if the features had been provided directly in the controller.

Package counts for various system sizes using the parallel approach for 256-K and 1-Mb bubble modules are given in Table 3. The 1-megabyte system has a typical bit density of 151 K per package, including all overhead packages—a vast improvement on 16-K or even 64-K dynamic RAMs. A complete 1-megabyte system fits on a standard Series 80 6.75-by-12-in. microcomputer card. Its typical active power dissipation is less than 4 microwatts per bit, or 30 W overall (dropping to 10 W during standby).



4. Parallel view. Bubble systems can also be expanded in parallel to boost data rates. Then all bubble and support circuits are continuously active during data transfers. Shift registers produce parallel data and external memory stores the redundancy map.

The number of components in the eight-module system could be reduced by using discrete, high-current drivers to run all eight modules from the one controller. However, such an approach is questionable because it complicates signal routing, generates a lot of noise, and creates heat-sinking problems. Furthermore, the standard drivers have built-in power-up and -down sequencing to keep data safe when power is lost. Supplying discrete drivers with these functions may increase component count to the point where not much is saved.

Systems using eight modules, each operating at 100 kilohertz, have a peak data rate of 100 kilobytes per second. That rate would keep the host processor busy all the time. As a result, it will be desirable in most systems to add a DMA controller for the data transfer. Therefore, signals to interface with an LSI DMA controller have been provided on the bubble-memory controller (the DMA part is included in the package count given for the eight-module system).

The two methods of expansion may also be combined for systems where multiplexed banks of eight parallel bubble modules are used with a single controller, yielding multimegabyte capacity.

The big time

In larger systems the 100 K-byte/s of an eight-module system is not adequate. A bubble memory that replaces a head-per-track disk must handle data rates of 1 to 4 megabytes/s. Such an application will be best served by the 4-Mb bubbles currently in design [*Electronics*, Aug. 2, 1979, p. 99]. But the required performance can, in fact, be achieved with 256-K and 1-Mb parts if more than one controller is used. Therefore, control signals allow parallel operation of controllers to be synchronized over 16-, 24-, 32-bit and wider buses. In operation, the same commands are sent simultaneously to all controllers and data-request signals are used in a wired-AND mode while interrupt requests are used in a wired-OR mode. The FIFO buffer's temporary storage compensates for the differences in data rates due to the unique redundancy map patterns in each controller's map RAM (these maps should, however, be balanced to minimize the depth of FIFO storage for this purpose).

In addition, the data rate for each group of eight lines on the data bus can be increased from 100 kilobytes/s to 1 megabyte/s by time-multiplexing 10 controllers to the same set of lines (Fig. 5). Here, a microprocessor or specialized I/O processor interfaces the 10 controllers with the host system bus or I/O channel and adds considerable intelligence to the subsystem.

For a data rate of 2 megabytes/s, 20 controllers each running eight bubble modules in parallel would be required. For 256-K bubbles, each data block must be at least 20 times 256 or 5-K bytes, and the system must hold at least 5 megabytes. Average access time is 7 ms

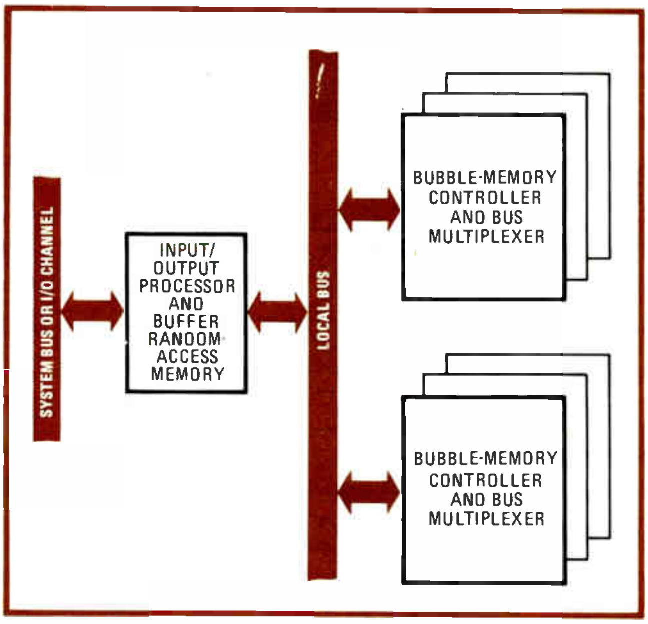
(12 ms maximum). For the 1-megabyte bubble the respective figures are 10-K bytes, 20 megabytes, and 11 ms (21 ms maximum).

In a system as large as this, the use of the controller's error-correcting feature becomes very important. In the smaller systems, it is usually enough just to detect errors and reread the data affected by soft (transient) errors. Assuming 10^{-9} soft errors per bit read and 10^{-11} hard errors (stored data loss) per coil cycle, then a single-module system running at a 5% duty cycle will produce only about one error a year requiring correction and one every few days requiring reread. With a frequency as low as this, the correction capabilities need not be very extensive. Indeed in noncritical applications, a simple detect-and-reread cycle to correct the most frequent soft errors would suffice.

Significant errors

On the other hand, the large system serving as fast-access mass storage has 160 bubble modules running in parallel, giving a correspondingly higher hard-error rate—and in this application, data integrity is very important. To address this need effectively, a 12-bit modified Fire code in the controller checks the data in the bubble memory a sector at a time, or every 512 bits. As noted, this code is capable of detecting up to three random errors or any burst error up to 12 bits long with 100% accuracy. Other error patterns have a high probability of detection.

As for error correction, the most frequent hard error—by several orders of magnitude—is a single-bit error; the next most frequent is a pair of adjacent bit errors, and both these can be corrected by the code. Other error patterns will in most cases be indicated as impossible to correct by the error-not-correctable status bit. Since this capability is itself imperfect, it seems best always to correct soft errors by rereading the data to avoid the chance of an erroneous correction. The presence of soft errors is indicated by a status bit at the end of the read-corrected command, which can be used to determine whether a reread should be performed. An additional-error-detected bit indicates when more than one 512-bit data block is in error in systems having more than 512 bits per page of bubble memory data. ☐



5. Disk replacement. Bubble data rates can be boosted to 4 megabytes/second with parallel and multiplexed expansion, where controllers, each handling parallel bubbles, are time-multiplexed. Ten controllers, for example, increase the 100-kb/s rate tenfold.

Software driver lets CP/M address bubbles as a disk

by Chris E. Le Tocq
National Semiconductor Corp., Santa Clara, Calif.

☐ Magnetic-bubble memory boards need not be hard to use for high-performance mass storage. With minor software changes, any system that currently relies on disks may replace them with bubbles. A storage driver program can make the bubble device look like a disk, so that the superior performance of bubbles can be exploited in compilers, word processors, data-logging packages, and so on, without changing the application programs.

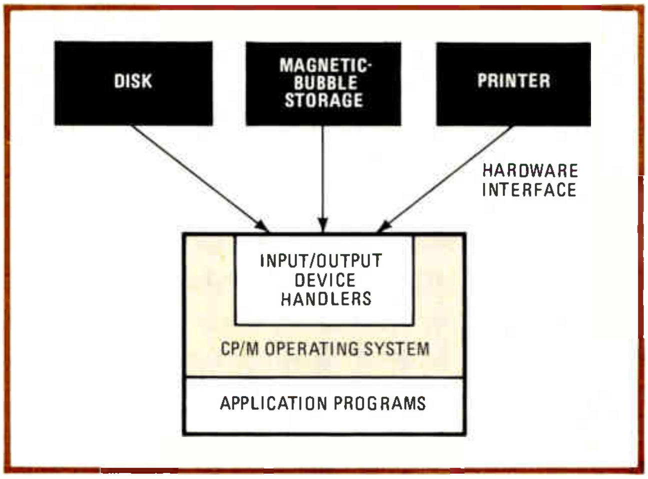
To see just how easy it would be to use a bubble device as if it were a disk drive, it was decided to interface the National Semiconductor 32-K-byte BLC9250 bubble memory board with a microcomputer running the widely used CP/M operating system (CP/M is a trademark of Digital Research Corp.).

The interrelationships of the CP/M-based system are shown in Fig. 1. The only important interface to consider here is the software one between the input/output device handlers and the operating system. For existing application programs to use the bubble board, National supplies a software I/O driver that makes the bubble storage look like a disk device to CP/M. The interface between the operating system and the application program is unaffected by the addition of the bubble memory.

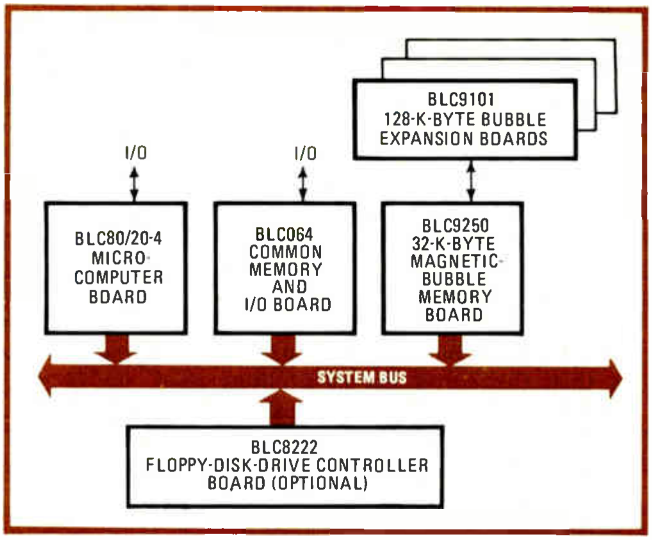
Figure 2 diagrams a microcomputer system using a bubble memory in place of a floppy disk. In addition to the BLC9250 bubble board, the system consists of a BLC80/20-4 microcomputer board with external I/O, a common memory, a Multibus-compatible system bus, and an optional floppy-disk drive and controller.

The BLC9250 (Fig. 3) has a 256-K NBM2256 chip, an Intel 8039 single-chip microcomputer, control circuits, and a system bus interface. Up to eight BLC9101 expansion boards, each containing 128-K bytes of storage, can be added to the system, bringing memory capacity to slightly over 1 megabyte.

In the simplest terms, a bubble device is a magnetic chip manufactured by processes similar to those used to make semiconductor devices. The magnetic bubbles themselves are small magnetic domains formed when an external magnetic field is applied perpendicularly to the surface of the device. In the presence of a magnetic field



1. Isolation. The I/O device handler can make a magnetic-bubble device look like a disk so that neither the operating system nor the user's programs have to be changed. The software accepts other hardware, which also is isolated from the user's programs.



2. Bubble microcomputer. Block diagram shows how a typical microcomputer system can use magnetic-bubble memory for mass storage. A floppy disk may still be used as an optional feature for memory backup or data and program loading.

gradient, these domains become mobile and their direction of motion can be controlled. Permalloy patterns deposited on the chip define the path along which the bubbles will travel.

Data bubbles stored in the device are arranged in loops of predetermined length, usually with two access points—one for reading and one for writing. The controls for generating bubble bits and governing their movement are implemented in metal layers on the chip.

Swapping bits

The 256-K chip has 282 loops of 1,024 bits. Less are needed, but redundant loops have been built into the design to increase manufacturing yields. A pattern contained on two map loops enables the controller to select 262 good loops out of the 282. From each of these loops, 1 bit at a time can be swapped or replicated for write or read operations, respectively (see "Inside a magnetic-bubble storage device," p. 146).

Data on the bubble is handled in blocks of 128 bytes because that is the standard disk-sector size for the CP/M operating system. In actual bubble configuration, 1 bit from each of the 262 loops—256 bits of data plus 6 bits for error correction—is called a page. A page is 32 bytes, and four successive pages is equivalent to a 128-byte disk sector. A track is defined as containing 32 sectors, or 4-K bytes. (This logical track is not to be confused with the physical input and output tracks on the device itself.) Eight tracks can be defined on the NBM2256 chip for a total storage capacity of 32-K bytes.

The operating system expects to be addressing a disk device. A disk address consists of two numbers—the track number and the sector number. In contrast, bubble data is addressed by a sequential string of page numbers. Thus, the bubble handler software translates a track and sector address from CP/M into the bubble page address for the first page of each four-page sector.

For example, track zero, sector zero, becomes page zero; track zero, sector one, is translated into page eight; and track four, sector zero (the logical middle of the device), starts at page four. The bubble address is large enough to handle data on expansion modules. If the page address is for a nonexistent module, an error is returned to the operating system.

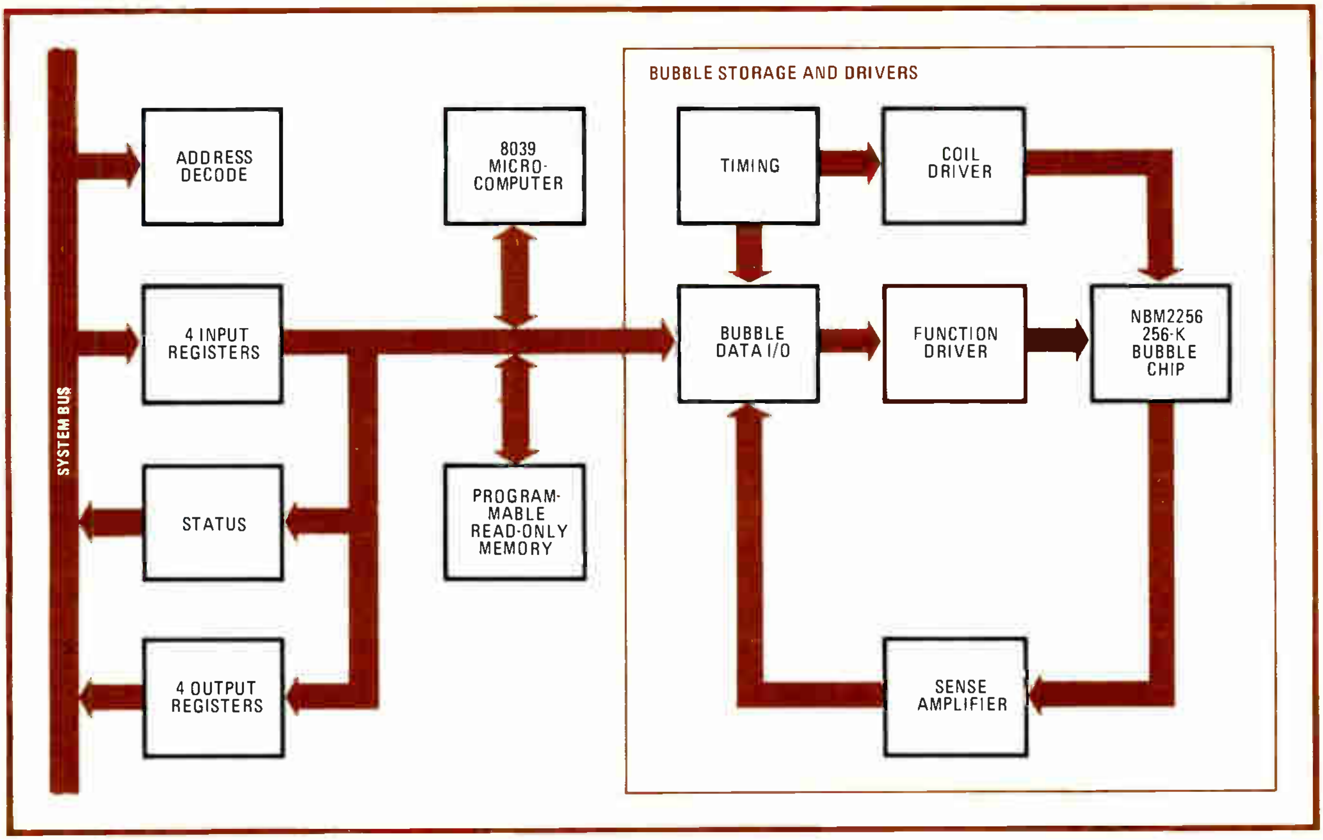
The CP/M operating system is stored on the first two tracks (the first 256 pages). The file directory for the data on the 2256 device itself, and on any expansion board, is stored in the first kilobyte of the third track (the next 32 pages). That leaves 23-K bytes of user space (the remaining 736 pages). It is possible to store CP/M on a read-only memory, freeing another 8-K bytes of user space, but the directory has to remain on the device to be updated as the file structure changes.

With the BLC9250 bubble storage board, neither the user nor the user's application program has to know the data configuration on the bubble chip. The design of the software handler makes the device look exactly like a disk. As with a disk memory, CP/M knows about the bubble storage in terms of track and sector numbers. The program running under CP/M gains access to data on a disk or the bubble storage by the name of the file in which that data is stored and the number of the record within that file.

Handler design

The flow chart of the bubble-storage handler logic is shown in Fig. 4. Its job is to convert the disk address into a bubble address (the third block), issue the appropriate bubble commands with the right timing, and check for errors. As the handler returns to the user program, the controller on the memory board positions the bubble storage at the next sector in anticipation that the same command will be repeated for the sector—which is what happens in most file-storage access operations.

The basic I/O handler can also drive a floppy-disk drive with a National BLC8222 double- or single-density diskette controller. Files may be transferred freely between standard floppy disks and the bubble storage, and the disk can be disconnected from the system when it is no longer needed.



3. Details. The components of the BLC9250 32-K-byte magnetic-bubble memory storage board are shown in this layout. A single-chip microcomputer without read-only memory, the 8039, takes care of all the complex control functions of the bubble device.

The remaining logic in the handler determines whether control passes to the bubble handler or to the floppy controller. All the bubble handler needs to know is the location of the three fields—track, sector, and DMAAD, the direct-memory-access address in system memory—with which the transfer is to take place.

How fast?

The two commonest ways of measuring the performance of storage devices are average access time and data-transfer rate. Bubbles have much faster access times than disks but slower transfer rates.

Access to data on bubble storage is fast because of two basic physical advantages. First, the data does not need formatting as on disk storage—usable data does not have to be surrounded with an unusable block of identifying data. Secondly, though bubbles are in essence a rotating storage device—the data rotates within the medium, but the medium does not move—the data does not continuously rotate and has no inertia.

A bubble device thus can be started and stopped instantly and can be rotated quickly to the right position. This eliminates the need for positioning algorithms that calculate when the next item of data will be needed and place this data where it can be retrieved quickly.

The access time of the magnetic-bubble storage device is the time it takes to move the bubbles of a desired page to the position in the loop opposite either the swap gates for writing or the replicate gates for reading. The average access time will be half the length of the data loop, or 512 cycles. The current version of the 2256 bubble device is driven by a 100-kilohertz clock, which moves each bubble one memory space in 10 microseconds.

After a sector has been accessed, the next logical sector is 198 cycles forward around the loop because of logical positioning. The time to position the device to the next sector is therefore 2 milliseconds.

The data rate is determined by the number of cycles it takes to transfer a four-page sector. It takes a total of 463 cycles to read out one page—282 cycles to move all the bits from the data loops plus 181 cycles to clear the last bit through the detector (see again the diagram in "Inside a magnetic-bubble storage device," p. 146).

When reading pages in succession, it is not necessary to wait until all the bits have cleared the detector before the next page is replicated. An additional 14 cycles are added to the basic 282 cycles to allow for the 14 bits of the leader on the input track that keeps the pages synchronized for writing. Another 41 cycles are needed by the 8039 processor to perform its control functions between each page, bringing the page transfer interval to 337 cycles.

Reading a full four-page sector then takes 337 cycles times three for the first three pages, plus 463 cycles for the last page, for a total of 1,474 cycles. This works out to a data rate of 70 kilobits per second—128 bytes (a sector) in 14.74 ms. That figure compares with a typical formatted data rate of an 8-inch floppy disk like Shugart Associates' SA800-1 of 160 kb/s (see Table 1).

Though the data rate for unformatted media is the standard method of quoting the transfer rate for disk drives, it is not valid for comparing disks with magnetic-

Inside a magnetic-bubble storage device

Magnetic-bubble memories store data on moving magnetic domains that travel along paths determined by metal patterns deposited on the chip.

On the NBM2256 256-K magnetic-bubble storage device, magnetic bubbles each representing 1 bit are stored on 282 data loops, each 1,024 bits long. The device consists of 1,024 physical pages, where a page consists of 1 bit from each loop. There are 282 bits per page, of which 262 are guaranteed to be from good loops. The redundant loops are incorporated to increase chip yields and thus reduce cost.

Information about which loops are good and which are not is contained in two map loops. Of the 262 bits from good loops, 6 bits are used for error checking and the remaining 256 bits are passed to the user program. Thus, each page contains 32 bytes of data.

For every 10-microsecond cycle of the rotating magnetic field applied to the memory chips, the data loops move one position forward. At the same time, the map loops, the input track, and the output track are each rotated one position forward. The redundancy map loops also contain a synchronization pattern, used for initialization. The data is rotated until this pattern is detected, and then the page opposite the output track is defined as page zero.

Each page is assigned a physical address, starting with zero, in a sequential, ascending order. By the time 282 bits have been shifted (to yield 256 bits of good data), the page that is aligned with respect to the output track is displaced by 282 physical positions from the page that has just been used.

In order to improve the data-transfer rate, the controller superimposes a logical page address on the physical address structure. The logical pages in the 2256 chip on the BLC9250 board are displaced from the physical ones by 337—that is, each logical page is separated by 337 bits on each loop. The 55 extra pages over 282 derive from the 410 μs (41 cycles) that the 8039 processor needs to perform its control function and the distance along the input track (140 μs, or 14 magnetic cycles) from the generator to the first data loop.

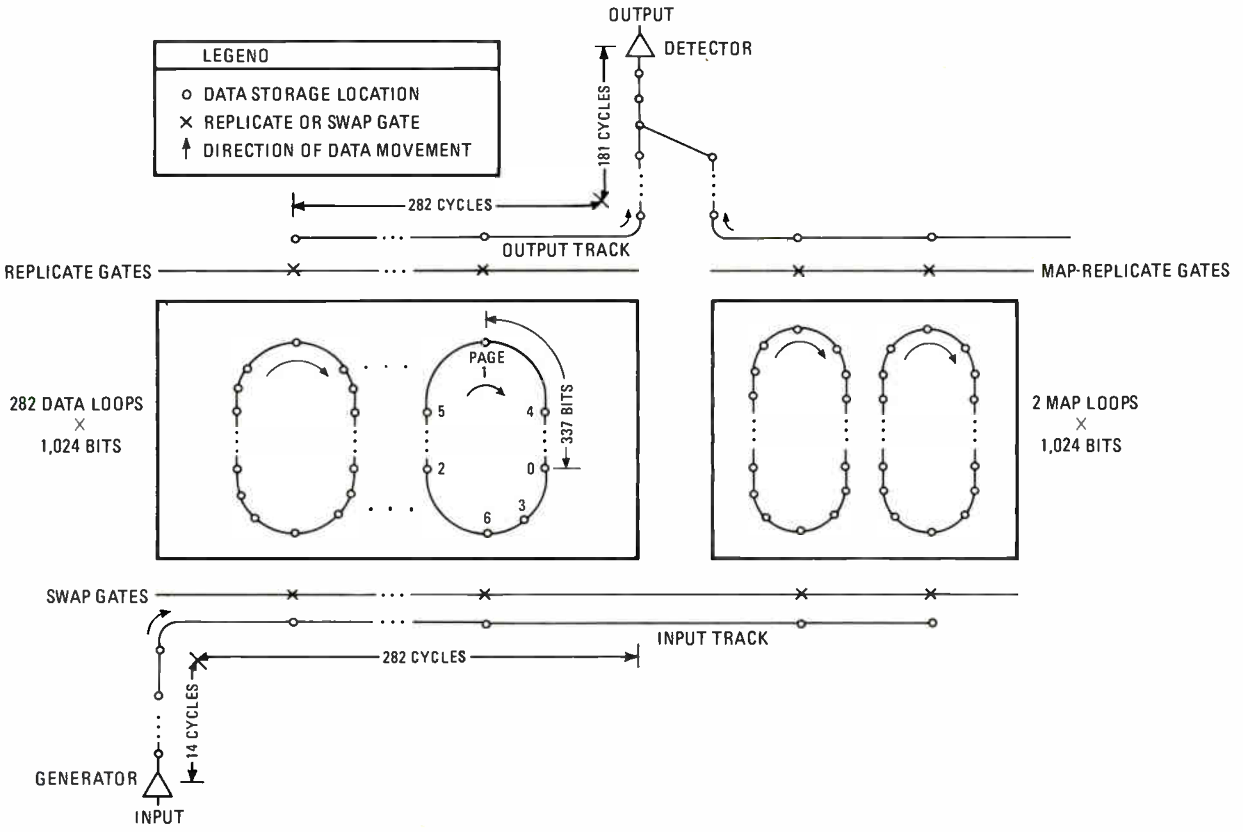
If the program needs more than one consecutive logical page at a time, then it is important to specify that to the controller so that the next page can be replicated when it is in position opposite the output track. If a single page is read, then by the time the controller has finished reading, the next logical page will have passed the output track because of the 181 cycles required to move the last replicated bit through the detector. Almost a complete rotation of the storage will be required to reach it.

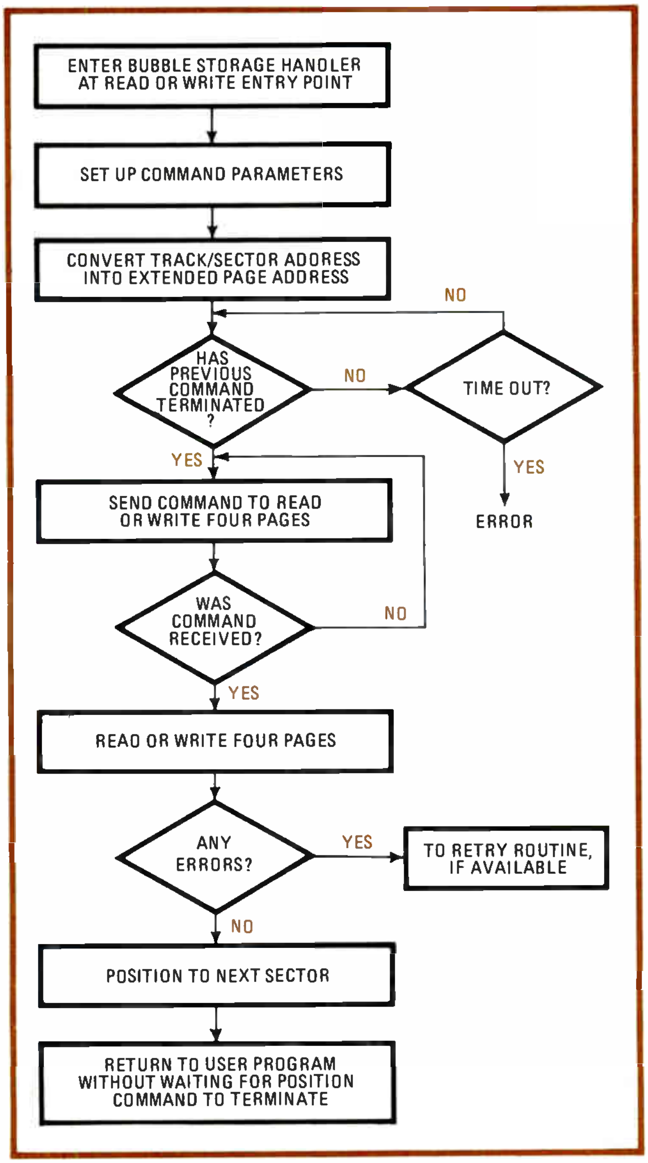
To read a page, it is necessary to:

- ☐ Rotate the data loops until the appropriate page is aligned with respect to the output track.
- ☐ Replicate the bits from the loops into the output track.
- ☐ Rotate the output track until these bits have passed the detector point, 181 cycles from the track.

The process of writing is functionally similar to that of reading. It is necessary to:

- ☐ Rotate the data loops until the appropriate page is offset back from the input track by the required amount.
- ☐ Read the data into the input track, rotating it and the data loops as the bubbles are generated.
- ☐ When all the data is read in and the required page is aligned with the input track, swap the current contents of the page with the input track.





4. Translation. Part of the magnetic-bubble storage I/O handler program translates the track and sector address used for a sector of data on a disk device into a page address of the first page of a four-page sector on the bubble device.

bubble systems. Before data is stored on a disk, it must be formatted into sectors with identification headers and formatting gaps for timing. The resulting overhead reduces the disk's usable data-bit capacity and also the effective transfer rate; the bubble device, as noted, does not need formatting.

Bubbles versus floppies

In an environment where files are frequently updated and manipulated, access time is often the most important parameter. Because the bubble storage actually has slower transfer rates, however, the average quantity of data transferred in each operation should be considered in comparing the performance of bubble devices and disk drives for inclusion in a system.

If the bubble storage and the floppy disk must both randomly seek and then read data, on average, the bubble will have read 2.5-K bytes before the disk has read anything. After another 1-K byte, the double-density disk will have caught up with the bubble device, and after an additional 0.9-K byte, the single-density unit will have caught up. Thereafter, the disk's greater transfer rate overcomes its slow access time.

CP/M's dynamic allocation of files spreads data blocks over the disk (or bubble) as files are deleted and added. The blocks belonging to one file may not all be on the same track, so that the access time also becomes the most significant factor in a multifile system.

Performance also depends on the type of programs that use the device. Programs manipulating files or single sectors need a device with a fast access time, as they will continually be moving between tracks. Examples of this type of program are record-update packages, editors, and data-base management systems. In contrast, programs that load large amounts of data onto and off the device at one time will benefit from the high transfer rate of a disk.

To demonstrate the effect of access time and data rate on the relative performance of bubble and disk devices, experimental comparison of the BLC9250 and the SA800-1 was carried out for three different tasks—loading a 14-sector file, loading a 164-sector file, and loading a Basic program into an interpreter that converted it into intermediate code as each sector was loaded.

This last task is a good example of a realistic environment because it shows a file being processed sector by sector. To provide a known environment on the floppy disk, there were no other files on the device and the initial file was positioned next to the directory.

The first two tests were mainly comparisons of data rates. The two files are good examples of the size file that a small system loads into memory. Although the head-loading time and the latency of the floppy disk will slow it down, the greatest difference, the seek time, is minimized.

The third test also minimizes seek time for the floppy disk, since the files will be close together. But because of the individual sector accesses, the bubble device can be expected to have an advantage. Positioning the files immediately after the directory offset this advantage somewhat. Yet, in a one-shot test with a moderately full disk, the times were still 10% to 40% longer on the floppy than on the bubble device.

In general operation, most sector accesses are sequential and the device is positioned at the end of the logical

TABLE 1: COMPARING THE BLC9250 BUBBLE WITH THE SA 800-1 FLOPPY DISK

Performance parameter	SA800-1 (unformatted)	SA800-1 (formatted)	BLC9250
Average access time, including latency (ms)	294	294	5
Data rate (kb/s): single-density double-density	250 500	160 246	70
Time to next sector (ms)	–	32/21 (single/double)	2
Number of tracks	77	77	8
Rotation	360 rpm	360 rpm	10 µs/b

TABLE 2: TEST COMPARISON OF THE BLC9250 BUBBLE DEVICE AND THE SA800-1 DISK MEMORY	Test 1: load 14 sectors	Test 2: load 164 sectors	Test 3: load Basic program
SA800-1			
Single-density			
interleaved-by-6 (s)	1.3	8.5	11.6
interleaved-by-3 (s)	1.2	5.3	12.0
Double-density			
interleaved-by-6 (s)	0.9	5.8	12.1
interleaved-by-4 (s)	0.8	4.4	11.7
BLC9250 (s)	0.7	4.5	4.0

sector just read to wait for the next request. For rotating devices such as disk storage, the effect of the disk's motion on access time to the sector can be minimized by physically interleaving the sectors to bring the head relatively close to the next logical sector.

Sectors may be interleaved in integral amounts and a good interleave will bring the head within one physical sector of its next access. The least time for a sequential access will be half the time it takes to transfer a sector. In order to compensate for the time interval required to process each sector, the disk device was tested at a number of interleavings.

The SA800-1 was tested at double density, interleaving the sectors by four and six, and at single density, interleaving by three and six. The interleaved-by-four double-density and interleaved-by-three single-density disks had the fastest file-load capability. The results, rounded to the nearest tenth of a second, are shown in Table 2.

The interleaved-by-four double-density floppy disk is faster for bulk file loading, with no seeks, but much slower with a Basic loader that is doing processing before loading each sector. The differences in performance stem from the fact that the bubble device positions itself at the next sector and waits, whereas the disk keeps rotating and the sector must be sought after each processing operation in the test is completed.

On a pure comparison of data rates, the disk should theoretically outperform the bubble device, but the system throughput in this example is three times as fast with the bubble storage. As these results show, the access time and the average latency of the disk device are what make the difference in actual performance.

Although throughput is generally considered to be inversely proportional to the average access time for a sector, a device's performance also depends on the type of access that takes place. A random access requires more time on both bubble and disk devices than a sequential access.

In order to determine the effect the ratio between

TABLE 3: COMPARISON OF AVERAGE ACCESS TIME FOR BUBBLE MEMORY WITH FLOPPY AND WINCHESTER DISKS	NBM 2256	SA800-1	ST506
Transfer times (ms)	15	4	.03
Sequential access time (ms)	0	2	.015
Random access time (ms)	5	294	193
Average access time (as a function of the probability of random access)	5p + 15	292p + 6	193p

TABLE 4: COMPARISON OF A 1-MEGABYTE BUBBLE MEMORY WITH TWO WINCHESTER DISKS	Average access time (ms)	Data rate (kb/s)
1 M byte bubble memory board	10	684
SA1000 8 in. Winchester	80	3,413 (formatted)
ST506 5-¼-in. Winchester	193	3,932 (formatted)

random and sequential access has on throughput, a comparison was made between the BLC9250, the Seagate Technology ST506 5¼-in. micro-Winchester disk drive, and the SA800-1. The average time to access a sector (T) was calculated, using the formula

$$T = (1-p)c + pr + t$$

where

p = the probability of random access
r = the average random access time
c = the average sequential access time
t = the time to transfer a sector between memory and device, once it has been accessed

Based on the figures in Table 3, the throughput of a system using the ST506 will be greater than that of one based on the BLC9250, if fewer than 8% of the systems accesses are random. The throughput for a system based on the SA800-1 will exceed that of the bubble device, if the figure is below 3%.

Bubbles vs Winchesters—the shootout

The advantages in throughput of such bubble devices as the BLC9250 in certain applications can be applied to mass storage with devices that can hold up to 1 megabyte of memory. The access time and data rate for National's upcoming 1-megabyte bubble memory board, using its INS82853 controller and eight NBM2011 1-megabit bubble chips, are compared with the Shugart Associates SA1000 8-in. Winchester and the ST506 drive in Table 4.

The bubble system will, on the average, read 5.8-K bytes before the Winchester drives have read anything. But anything over 7.3-K bytes will be loaded faster by the SA1000. The equivalent breakpoint size for the micro-Winchester is 18.5-K bytes. Thus, a Winchester drive is preferred in applications that generally process large blocks of data. However, in a typical systems environment, where small blocks are handled, the bubble system will have higher throughput.

The bubble memory handler outlined here provides a way for existing programs to take advantage of the higher performance and reliability that magnetic-bubble memory offers. These memories are supplied on boards meeting standard form factors and, when interfaced with a widely available operating system, are now well within the designer's reach. With such handlers as that for the CP/M operating system, bubble storage can therefore become a common component in microcomputer and larger scale systems alike.

Still, bubble storage is a new technology. It will undergo the orders of magnitude improvements in performance, capacity, and price that widespread production brings. □

Local network enlists Z80s for distributed processing

Coaxial-cable–based system handles 255 stations without the need for a central controller

by Judy Estrin* and Bill Carrico, *Zilog Inc., Cupertino, Calif.*

☐ "Talk to me," a recent song, could well be the refrain of personal computers and peripheral devices scattered throughout a company or institution's premises. Indeed with the proliferation of this equipment, made by a host of firms, it could turn into a wail. Manufacturers, lured as well by the budding market, are responding with local data-communications networks that, when programmed appropriately, work with most makes of gear.

Joining this competition is the Z-Net system from Zilog, based on the well-accepted Z80 microprocessor. Although best suited to connect the company's data-processing, -storage, and printing stations, it can work with other vendors' equipment. By integrating data-processing, electronic mail, and office automation traffic, it aims to bring computing out of specialized rooms so that the notion of a computer on every desk will no longer be unrealistic (Fig. 1).

The basic Z-Net terminal is a stand-alone computer built around a 4-megahertz, Z80A microprocessor. The terminal also comes with a network interface for placing data packets through a transceiver onto a coaxial cable at a rate of 800 kilobits per second.

*Judy Estrin is no longer with the company.

Through the addition of options such as a keyboard, a cathode-ray-tube display, disk drives (Fig. 2), and printers, each MCZ-2 series unit, as the terminals are designated (see "What are the pieces?" p. 151), can be built up into a complex and independent microcomputer-based system. A total of 255 such systems can be linked by means of a coaxial cable up to 2 kilometers (1.2 miles) long.

'Robust' system

Of course, providing a communications path between desktop personal computers, supplying a means to share line printers and disks, and furnishing links by which intelligent devices can communicate with or take direction from other, remote processing systems is not enough. These feats must be accomplished by a local network that is "robust"—that is, one that cannot be

1. Network station. A local-network work station in the Z-Net system is truly a desktop installation. The MCZ 2/50 user's station shown has a display terminal and printer, both controlled by a Z80 microprocessor. More than one of these peripheral devices can be used if desired.

brought down by hardware failures or software bugs, but degrades gracefully. Because all processing is distributed in the Z-Net approach rather than concentrated in one central processing unit, robustness is inherent.

As important as robustness, the modularity of both hardware and software in the Z-Net system allows the local-network user to upgrade his capabilities without making the initial investment obsolete. For example, a user might begin his network with two microcomputers and a shared hard- or floppy-disk data station. These 8-bit data-generating and -receiving stations are adequate for many applications. Only later might a user encounter the need for a 16-bit processor.

Adding 16-bitters

With Z-Net, a company or institution can add a 16-bit machine to the network and use its initial 8-bit hardware for other tasks, such as word processing. Similarly, connections to public global telecommunications networks, to high-performance graphics devices, and to additional Z-Nets all are straightforward.

Also, Z-Net will eventually be able to work with the recently announced Ethernet local network. For example, a hierarchy of networks might have the faster but more-expensive 10-megabit/s Ethernet as a trunk, with branches consisting of the 800-kb/s Z-Net. Combining the two yields a networking system that can deal with many of the anticipated future requirements for computer communications and resource sharing.

Three kinds of station

A typical network arrangement is made up of three types of station linked via a single coaxial cable (Fig. 3). One type, the user's station, generates or receives data; a second type, called a shared resource station, allows expensive disk drivers or printers to be shared by several user's stations; the third is a universal controller that handles dissimilar host-to-host communications or industrial process control.

At the heart of all three types are a microprocessor board and a memory board. The former contains a Z80A CPU, an RS-232-C interface, a parallel interface, and a Z-Net interface; the latter, 6-K bytes of read-only memory and 64-K bytes of random-access memory. A display terminal, a printer, or both can be added to any of the three station types with no additional interface hardware. If local storage is added, any station can also function as a standalone microcomputer. For local floppy-disk storage, a programmable floppy-disk controller board is available that has its own Z80A, plus 6-K bytes of programmable ROM and 4-K bytes of RAM; it can control up to four double-sided, double-density, soft-sectored 8-inch floppy-disk drives.

2. Many stations. Z-Net links as many as 255 of the various versions of the MCZ-2 series microcomputer systems with up to 7,000 feet of coaxial cable. The Z80A-based SDS 2/01 disk-drive unit shown lets data files on the system be shared without a central controller.

In the universal controller station, the Z80A and memory boards provide one serial interface and one parallel interface to connect devices to the network. Up to two additional pairs of these boards can be added for more interfaces.

The network interface circuit on the Z80A board permits each station—regardless of type—to be linked to Z-Net without the need for a central control. The interface also implements the data-communications link-level protocols, which include address detection, packet framing, and cyclic-redundancy error checking. The data packet containing these bits leaves the network interface via a standard RS-422 connection to the transceiver board.

The transceiver implements the physical-link functions—primarily data transmission and reception, carrier sensing, collision detection, and clock extraction. It connects to the coaxial cable by means of a passive BNC T-connector.

For flexibility in a diversity of

What are the pieces?

A variety of hardware and software is available to operate with the Z-Net system. Three basic terminals are available. These include the table-top MCZ-2/20, which is a bare-bones system with no peripherals or software. It is modular and can be upgraded with various options such as 2.4 megabytes of floppy-disk storage. As a computer, it is as powerful as any Z80-based machine. The MCZ-2/25 is a 19-inch rack-mountable version of the 2/20. The MCZ-2/50 is a ready-to-run package with 2.4 megabytes of hard-disk storage, a 1,920-character cathode-ray-tube display, a multitasking operating system, and single- or multiple-terminal Cobol. It also has printer options.

The MCZ-2/19 is another entry-level bare-bones desktop computer and is known as the 2/49-1 when it comes with a CRT display, an operating system, and Cobol or Basic software. This equipment is geared to systems that do not yet need local networking or remote communications but will eventually be upgraded. They are usable only as nonnetwork desktop machines in their basic forms.

Other products include the SDS 2/01 network station transceiver for hooking everything up to coaxial cable, and a variety of network protocol software that runs on any MCZ-2 or SDS 2/01.

There also are word-processing, American National Standards Institute level 2 Cobol, and standard applications packages so that the user can concentrate his software efforts on his own special needs. To do this there is the Z-Lab software development station. Finally, an emulator package permits data transfer between Zilog machines and those of other vendors. **-Harvey J. Hindin**

applications, the hardware is controlled by software, and to increase the flexibility, the software is divided into layers. The basic layer, the heart of the system, is the multitasking kernel. It is the minimal piece of software needed to control a station's CPU. Each station has its own independent multitasking kernel to eliminate the need for an overall master unit for the system software.

Another layer incorporates the operating system and the network protocols. These are broken down into asynchronous software tasks that run in the environment provided by the kernel.

Positive division

The division of complex software into smaller, simpler pieces reduces software development and maintenance time for both designer and user. In addition, software layering gives flexibility to those users who do not require the services of the most-sophisticated portions of the operating system like user and device programs.

The system software requires 22-K bytes of operating system memory space per user's station. Thus 42-K bytes of the 64-K-byte system total is available to the user. In addition, there is a 4-K-byte bootstrap program, which is mapped out after system initialization. Another 6-K bytes, located on the floppy-disk controller board, is for the file system needed to address any data stored in the station. The network software—needed to communicate with other stations—occupies 8-K bytes and can either replace the file system or be loaded into the system as well. There is also a shared data-manager file system to operate the hard-disk–based shared-resource station; it resides in its own 64-K bytes at that station.

The multitasking kernel manages all stations operations. For example, it schedules the tasks running in its environment. Furthermore, it has routines for task management chores, like the creation and deletion of files, task synchronization, and intertask communications. In order for the kernel to fulfill these responsibilities, each task is assigned a priority and a time slice. When the priorities are equal, the kernel uses a round-robin scheduling method.

Synchronization of tasks or events on the same processor is achieved with BLOCK and WAKE commands. With the former, a task can suspend execution of another task or itself until an event occurs. The latter is simply the mechanism used to signal the occurrence of the event.

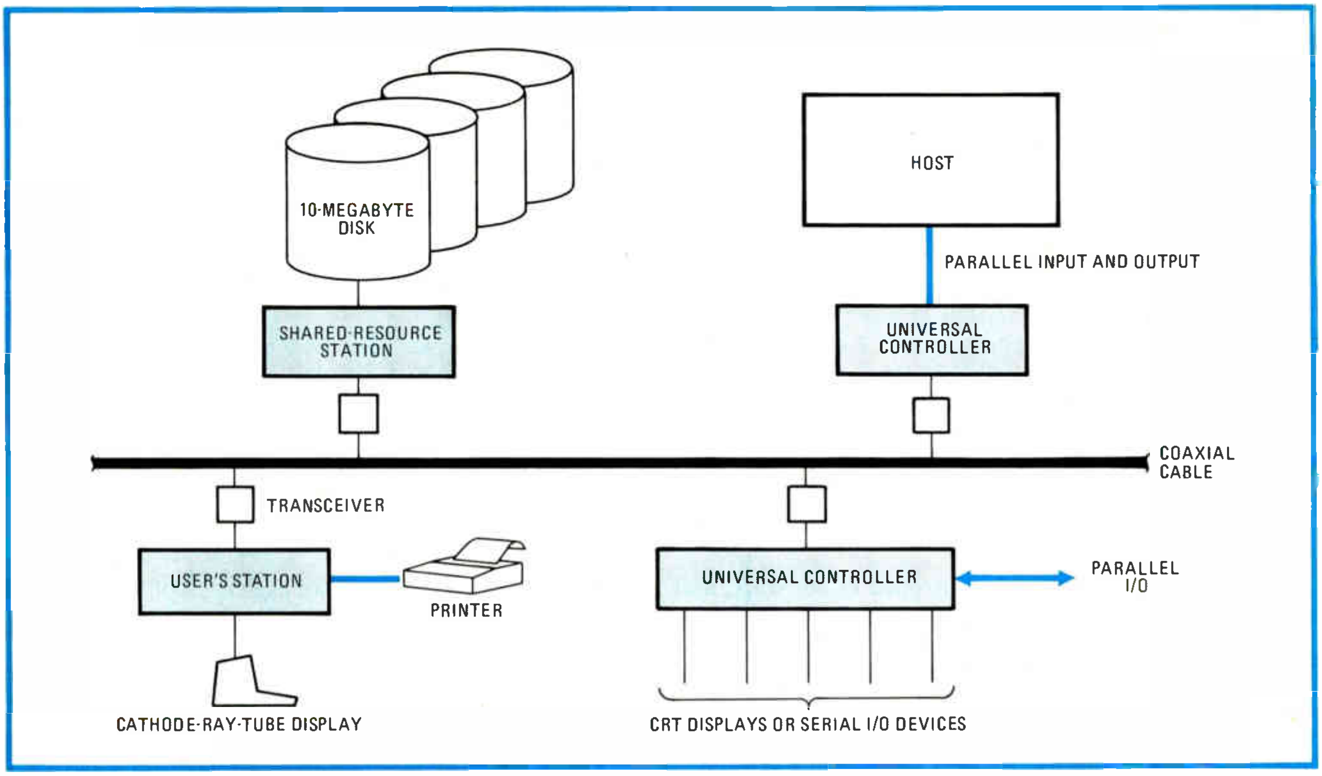
All intertask communication is performed by the kernel by means of conventional message passing rather than by memory sharing. This approach was chosen so that communications would be extendable to a network environment. With message passing, each task is identified by a unique identification number that is built up from a network, a station, and a task identification number. Names can be mapped onto these numbers, eliminating the need for a user's programs to keep track of the task locations.

Another advantage of message passing is that communication between local and remote tasks appears transparent to the tasks involved. A task simply issues the same kernel calls to send and receive messages regardless of the location of the destination task. Any differences in processing are internal and are handled by the kernels on the two stations. This extension of simple intertask communication across machines is an efficient way to synchronize remote tasks. The combination of a local network and transparent intertask communication helps maintain a cost-effective system that is easy to work with, since the user need not change his operating procedures as he changes his station use.

Keeping busy

While the kernel layer is doing its basic management job, the operating system and protocol-controlling layers perform a multiplicity of chores. The operating system manages memory, interprets and executes commands, and maps the I/O devices with logical numbers. Included with the operating system are a console driver, a single-user floppy-disk file system, and a multiuser hard-disk file system that runs on a shared resource station. The operating system also has a program interface that makes it compatible with Zilog's standard operating system for stand-alone Z80-based devices. As a result, a simple system call is sufficient to access such equipment.

Using the I/O mapping feature, device-independent software can be developed, because all I/O drivers have a standard interface. Consequently, new devices can be



3. Applications-oriented. With Z-Net, diverse data equipment, for applications ranging from electronic mail to office automation, can be connected, as shown. Each station can support up to five asynchronous lines, as well as parallel input/output.

incorporated without difficult, new system-generating procedures or changes to the user's programs.

The two file systems that come with the operating system have the same user interface, except that the hard-disk file system has added mechanisms for security (password authorization) and data integrity (record and file locking), safeguards needed in a multiuser environment. They also have a record interface that supports both sequential and random access, although their internal structure is optimized for the latter. Also, the hard-disk file system has hierarchical directories to make management easy when using large amounts of storage. As an added benefit, a program called STREAM is available that links to a user's programs and provides a byte stream interface to the disk. All these chores can be accomplished in a user-transparent manner because the operating system contains all the mechanisms needed to communicate with remote devices.

Software writing made easy

The operating system–user interface is optimized to facilitate software development, which can be done in Cobol, Basic, PLZ/SYS (a Pascal-like language), and Z80 assembly language. These are specific commands to manipulate files, control I/O devices and drives, and manage memory. New commands are added to the system simply by creating a procedure file. The multitasking kernel allows these commands to be run concurrently as long as they can coexist in memory.

These languages and commands interact with the modular software to make Z-Net easy to use for system software development. In turn, the flexible software and modular hardware combine to provide a ready scheme for hardware expansion. For example, each of the 255 available nodes can function as a user's station, a universal controller, or a shared resource. This flexibility allows splitting of tasks on demand as the overall workload increases. It also permits two stations to run the same task, should that be needed to guarantee maximum reliability. Furthermore, the addition of users does not degrade any existing user's processing performance. Since the network communications occur on an interleaved-packet basis, only a slight decrease in network performance may be experienced as a result of the addition of more stations.

To exchange data from one user's station to another, each station on the network has a set of two software-based high-level network protocols that, like the operating system software, are built around the software kernel. One is the interprocess communication, or IPC, protocol, which handles station-to-station data communications. The other, the data transfer protocol, or DTP, is designed to transfer data to and from a shared disk or printer.

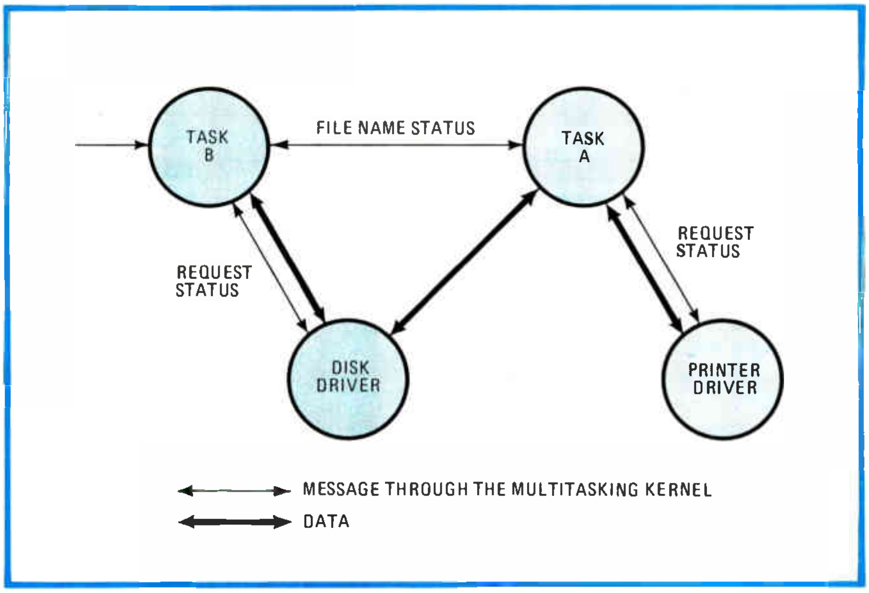
Each protocol uses lower-level protocols: the data-link layer drives the network hardware, and the network-control layer takes care of host-to-host reliability and data-flow control. The ability to communicate between local and remote tasks in the same manner makes possible some unique jobs that are best explained by example.

Split up

Suppose the job to be done is to enter data that is to be both stored in a file and sent to a printer. These tasks can run simultaneously on the same station. The creation of files to be printed and storage of them on the disk can be considered as task A and a printer spooler that reads a file from the disk and prints it on the printer as task B (Fig. 4).

Whenever task A wants a file printed, it sends a message to task B, passing the name of the file. When task B completes the job, it sends a message back to A and waits for the next request. Dividing this job into two tasks makes efficient use of the CPU resources. There is no problem with synchronization, as the tasks can synchronize themselves by sending messages to one another.

Job splitting is extendible to a multiuser environment. Here, to expand the example, multiple data-entry stations are sharing a disk and a printer. Driving the disk and the printer are tasks that run on their respective machines. Data is entered (task A) at each user's station and the spooler (task B) runs on the printer station. Tasks A and B communicate in exactly the same way as in the example above, using different routes for the messages and data.



4. Two at a time. With software designed in layers, it is easy to operate a disk (task A) and drive a printer (task B), at the same time. Depending on the data volume, this feat can be accomplished with a multiplicity of disks and printers simultaneously.

Tieing together independent microcomputers that can communicate among themselves or share resources opens up new ways to perform many existing applications and makes possible some completely new applications. For example, in a typical shared logic (timesharing computer) application, three users on the computer might be performing three different tasks. One, say, runs an accounts payable program, one runs an accounts receivable program, and one generates the payroll. In each case, the CPU is switched between the tasks on a time-sliced basis. All three use the same data base.

The Z-Net system solves this problem by dedicating one MCZ-2 to each application program, with all stations sharing the same data base over the network. The advantages of this approach are increased reliability due to independent machines, faster response time because each program has its own CPU, and ease in adding accounting programs.

When physical distribution is important, as on the factory floor, in inventory management, or in a network of point-of-sale terminals, Z-Net provides on-location processing power, with message passing between the physically separate sites. Timesharing just cannot handle such a setup. Office automation, which until now has yielded only intelligent stand-alone typewriters, word processors, and the like, can also benefit from the communication, data storage, and resource sharing possible with Z-Net.

Delivering the mail

The Z-Net system also is applicable to interoffice electronic mail because of the kernel's intermachine communication and task synchronization capabilities. Until now, distributed solutions have implemented electronic mail by storing a message or messages in a data base that must be routinely polled by the receiving machine looking for its mail. But with intertask synchronization across machines, the receiving machine can be flagged by the sender whenever mail is ready. Thus no processing time is lost in polling.

Industrial process control systems, which must gather data from and control devices at different locations, are obvious candidates for Z-Net. Process control applications often require on-site processing power for real-time responses. In addition, results obtained from computations at one site influence what should be going on at other sites. Intertask synchronization and a CPU at each site meet those needs.

Host to host

This wealth of applications, however, is not the whole story, and users of local networks are limited only by the creativity of the designer. As another example, consider host-to-host communication when the equipment is from different manufacturers in such applications as computer-based test equipment. This may be accomplished by interfacing the host with an appropriate MCZ-2. Interfacing can be as simple as writing a software driver that sends host data through the parallel port.

High process reliability is often the issue in a manufacturing environment—for instance, the monitoring of a chemical reaction where computer failure leads to grave consequences. Three MCZ-2 machines connected by Z-Net form a simple implementation of a highly reliable computer by using the intertask communication mechanisms. In this approach, two of the MCZ-2s are interfaced with the same sensors. They periodically pass information to the third machine, which compares the data for consistency. This machine also runs diagnostics on the two controllers. Should errors occur, the third machine transfers controls to the operating machine. The MCZ-2 operating system makes programming of this application straightforward. ❑

Universal E-PROM controller eases computer linkup

by Ralph Tenny
George Goode & Associates Inc., Dallas, Texas

A software-based controller lets an erasable programmable read-only memory programmer serve many different microprocessor systems, regardless of the individual microprocessors used. Programming the E-PROMs to meet any system format increases the system's capability, especially in transferring code between machines, in control of one computer by another, and in the direct transfer of data between an on-line computer and a word-processing system.

Here, TI's popular TM 990/189 University board is converted into a terminal that can receive an ASCII data stream, store it in memory, and then produce it on a cassette tape with a format acceptable to a TI loader. The tape input thus becomes the entree to any computer in the 990 family. With such a controller driving any of the many E-PROM programmers of standard design,[1,2] the memories can be programmed for any system.

The basic premise of this program is that almost any microprocessor's debugging routine contains a utility sequence that generates a memory dump. In the case of ASCII characters (figure), the program produces a continuous data stream that contains no control codes (CR and LF would be the most common extra characters). With this modification, the data stream becomes a serial version of the program data and can be recorded in consecutive memory locations. This serial data, when placed on a tape cassette, is then transferred to the machine through the E-PROM programmer.

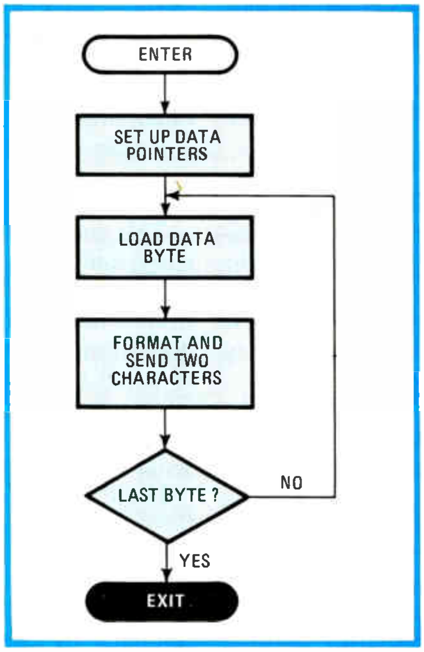
The board is especially suited to communication between systems. It is one of the few computers with an on-board terminal that, under software control, supports full resource sharing between on-board and external terminals. In contrast, many systems derive both control and interaction from an external terminal and may not support two terminals simultaneously without additional interfacing.

A buffer at location 36_{16}, which identifies the terminal in use—on-board or external—makes dual-terminal operation possible. Thus, at line 170 of the program, the clear command is initially used to order external-terminal operation. Similarly, at line 640, the INV statement writes in a nonzero value, and the on-board terminal and keyboard resumes control.

With this control feature, the utility bus can either be used in a passive mode (as in the listing) or serve as a terminal for another computer. Here, the bus sends a series of commands that initialize the slave computer for data reception. Of course, the slave must have the right program to accept both data and commands, but such a program is usually easy to implement.

Program operation is straightforward. Once the system is initialized (up through line 250), the command XOP R4, 11 puts the utility bus in a wait loop until a string of serial data is transmitted. Note that the communications port of most computer systems is configured as a transmitter. That is, data in RS-232 format is put out on pin 3 of the port and incoming data is received on pin 2, so it is best to install a cable that lets these two lines be interchanged by a switch.

An incoming character, assumed to be hexadecimal ASCII, is then tested to see if it is numeric or alphabetic. After suitable adjustment, the program then deposits it in one of four buffers in read/write memory (figure), which shows the buffer configuration after four characters have been received and stripped to a hexadecimal nibble.



Bit forms. Flow chart outlines method for maintaining a continuous stream of ASCII characters, which represents a memory image from the transmitting computer. Technique described in text permits TI's TM 990 University board to reconfigure memory image for the purpose of programming an E-PROM to meet almost any system format.

After the fourth character arrives, the routine beginning at line 380 recombines the four original data nibbles. The SOC @BUFR(R1), R5 command is a classical OR function that accesses the four memory locations via indexed addressing, with the result being placed in register R_4. Finally, at line 420, the data word (which may be two characters, one 16-bit data word, or one word of 9900 machine code) is stored in the memory buffer using auto-increment addressing, and the buffer is tested to see if it is full. In normal operation, only 1 kilobyte of code will be transferred, and the utility routine will be terminated manually by the operator. However, if the memory buffer overflows, the routine terminates reception and returns to on-board terminal operation, issuing an audible warning and relighting the on-board display.

Larger quantities of data may be transferred and then installed immediately in the E-PROM if a Memory

TM 990 LISTING: UNIVERSAL PROGRAMMER FOR ERASABLE PROGRAMMABLE READ-ONLY MEMORIES

```
0000              *This program makes the TM 990/189 University Board a smart terminal which
0000              *receives an incoming RS-232 data stream, converts each character into an
0000              *equivalent hexadecimal digit, then combines each successive group of four
0000              *characters into 16-bit words stored in memory. Data is stored in a four-word
0000              *buffer; each word contains one of the original nibbles sent. Each nibble has
0000              *been shifted to a position in the buffer which corresponds to that nibble's
0000              *position in the original word. The word is reassembled by OR'ing together these
0000              *four words; the assembled word is then stored.
0000
0000
0000
                         IDT    'DATAIN'
0890                     AORG   >890             Program location
0890                     DREG                    Assembler directive
      01C0      BUFR     EQU    >1C0             Define work buffer
0890  02E0      STRT     LWPI   >1A0             Initialize work space
0892  01A0
0894  04E0               CLR    @>36             Switch to external terminal
0896  0036
0898  0206               LI     R6, >900        Load alpha adjustment factor
089A  0900
089C  0203               LI     R3, >200        Define data buffer start
089E  0200
08A0  0201      ST2      LI     R1, 2           Load work buffer
08A2  0002
08A4  C081               MOV    R1, R2          Index values
08A6  06A0               BL     @CLR             Clear work buffers
08A8  08F2
08AA  C202      GET      MOV    R2, R8          Save multiplicand
08AC  3A01               MPY    R1, R8          Complete shift count
08AE  C009               MOV    R9, R0           and load it into register R0
08B0  2EC4               XOP    R4, 11          Enter ASCII character
08B2  0284               CI     R4, >3900       Test to see if character is numeric
08B4  3900
08B6  151B               JGT    LPHA             Make adjustment if necessary
08B8  0244      MASK     ANDI   R4, >0F00       Strip character to 4 bits
08BA  0F00
08BC  06C4               SWPB   R4               Move data to least significant nibble
08BE  0B04               SRC    R4, 0           Shift by count in R0
08C0  C844               MOV    R4, @BUFR(R1)    and store in buffer
08C2  01C0
08C4  05C1               INCT   R1               Bump the pointer
08C6  0281               CI     R1, 8           Test for last character
08C8  0008
08CA  12EF               JLE    GET              Not done. Continue
08CC  0641               DECT   R1               Adjust index pointer
08CE  04C5               CLR    R5               Done, combine hexadecimal characters
08D0  E161      ORIN     SOC    @BUFR(R1), R5     using successive OR operations
08D2  01C0
08D4  0641               DECT   R1               Count down index
08D6  0281               CI     R1, 2           Test for end of loop
08D8  0002
08DA  14FA               JHE    ORIN             and repeat as needed
08DC  CCC5               MOV    R5, *R3+        and then store data words
08DE  0283               CI     R3, >7F0        Check for end of buffer
08E0  07F0
08E2  1301               JEQ    EXIT              and quit if out of memory
08E4  10DD      NEXT     JMP    ST2              Continue in an endless loop
08E6  0560      EXIT     INV    @>36             Go back to on-board terminal
08E8  0036
08EA  06A0               BL     @>3000           Then go home
08EC  3000
08EE  A106      LPHA     A      R6, R4          Adjust for alpha
08F0  10E3               JMP    MASK             Return to data stream
08F2  0207      CLR      LI     R7, 8           Set up counter and index
08F4  0008
08F6  04E7      CL2      CLR    @BUFR(R7)        Clear a work buffer
08F8  01C0
08FA  0647               DECT   R7               Count down
08FC  1BFC               JH     CL2               and repeat as needed
08FE  045B               RT                      Then return
      0890               END    STRT
```

Expansion Module[3] is used. This module allows nearly automatic operation, with only 14 keystrokes needed to initiate the 90-second (1 kilobyte) programming cycle. As for control tasks, this scheme has worked well for students attending courses in 9900 assembly language, where the word processor of TI's 990/302 software development system is the system log that generates assembly listings. In transfer tasks, in-house development systems serving as extra text-entry stations are both flexible and inexpensive. This scheme will allow the addition of at least five such systems for the price of the original two included with the word processor. □

References

1. James Nicholson, "Upgrade your EPROM programmer," EDN, Nov. 5, 1980, p. 90.
2. H. S. Mazumdar, "Build a simple PROM programmer," EDN, June 20, 1980, p. 100.
3. Memory and I/O Expansion Module—User's Guide, George Goode & Associates Inc., 1st edition, Jan. 1980.

Calculator notes

HP-41 solves widest range of microstrip design problems

by L. Mar and M. W. Gunn, *University of Queensland, Department of Electrical Engineering, Brisbane, Australia*

Previous programs for finding the electrical characteristics of a microstrip transmission line of given physical dimensions have been based on a set of approximation equations that are valid only over a limited range. This program, however, uses the equations recently proposed by Wheeler[1], which have proved to be by far the most accurate to date. It therefore agrees to within 3% with the published table for striplines operating in the transverse electromagnetic mode[2], so enabling all line variables to be accurately found. They are: impedance, Z_c; effective dielectric constant, $e_{r_{eff}}$; operating wavelength, λ_g; conduction loss, α_c; and dielectric loss, α_d.

The program is partitioned into nine sections, A–I, of which input and output sections A and I are required by all the others. Thus, one or more variables of the microstrip element may be found as desired (see subtable).

Given the line's dielectric constant, ϵ_r, and its thickness-to-height and width-to-height ratios, t/h and w/h (see figure), the program finds the characteristic impedance from:

$$Z_c = (42.4/(\epsilon_r+1)^{1/2}) \ln [1+A^2B+(A^3B^2+A^2C)^{1/2}]$$

where

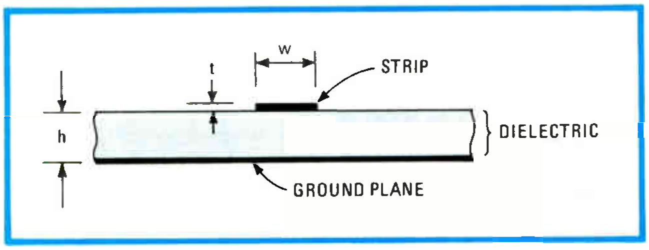
$A = 4h/w'$

$B = (14+8/\epsilon_r)/11$

$C = (1+1/\epsilon_r)/2$

and:

$$w'/h = D+(Ct/h\pi)\ln\frac{10.87}{E+E/[\pi(D+1.10E)^2]}$$



Strip section. Program finds impedance, wavelength, and loss of microstrip transmission line when given the thickness-to-height and thickness-to-width ratios, as depicted in cross-sectional view.

where D = w/h and E = t/h.

Following this, the effective dielectric constant and the microstrip wavelength are determined from the normalized characteristic impedance:

$$\epsilon_{r_{eff}} = (Z_{C\,\epsilon_r=1}/Z_{C\,\epsilon_r})^{1/2}$$

and:

$$\lambda_q = 2.998(10^8)/f(\epsilon_{r_{eff}})^{1/2}$$

where f is the specified frequency. Conductor loss is then calculated from:

$$\alpha_c = 27.288\left(1-\frac{Z_1}{Z_\delta}\right)\frac{(\epsilon_{r_{eff}})^{1/2}f}{2.998(10^8)}$$

where

$Z_1 = Z_{C\,\epsilon_r=1,\,t/h,w/h}$

$Z_\delta = Z_{C\,\epsilon_r=1,\,t\text{-}\delta,\,w\text{-}\delta,\,h+d}$

δ = skin depth of the metalization = $(2/\omega\,\mu_o\sigma)^{1/2}$

in which

ω = the radian frequency

μ_o = the permeability of free space

σ = the conductivity

Finally, dielectric loss is given by:

$$\alpha_d = 27.288\,q\epsilon_r \tan\delta/(\epsilon_{r_{eff}}\lambda_g)$$

where $q = (\epsilon_{r_{eff}}-1)/(\epsilon_r-1)$.

As an example of the program's usefulness, consider the case where ϵ_r = 9.6, t/h = 0.01, w/h = 0.8, f = 10 gigahertz, h = 635 micrometers, σ = 5.8(10^7) siemens/m and tan δ = 1(10^{-3}). Placing the constants into the program as instructed yields Z_c = 55.024 Ω, $\epsilon_{r_{eff}}$ = 6.245, λ_g = 1.196 cm, α_c = 4.512 decibels per meter, and α_d = 2.132 dB/m. A synthesis example for finding the width-to-height ratio, which uses block D of the program, where Z_c = 60 Ω, t/h = 0.01, and ϵ_r = 9.6, yields w/h = 0.647.

Comparing these results with Gunston's table shows that a program based on Wheeler's equations is the preferred solution to the approximation calculations on a microstrip line. This program achieves an effective compromise between complexity and accuracy. Although it is written for the HP-41C, it can be easily adapted to other calculators, with only minor modification.

References

1. H. A. Wheeler, "Transmission-Line Properties of a Strip on a Dielectric Sheet on a Plane," IEEE Transactions on Microwave Theory and Technique, MTT-25, No. 8, pp. 631–647, 1977.
2. M. A. R. Gunston, "Microwave Transmission-Line Impedance Data," Chapter 3.6, Van Nostrand Reinhold Co., 1972.

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $75 for each item published.

HP-41C PROGRAM LISTING FOR MICROSTRIP DESIGN

Location	Key
001	LBL^{T}MICSTR
	CF01
	CF27
	^{T}DIE?
	PROMPT
	STO 00
	XEQ^{T}K
	CF 00
	^{T}T/H?
010	PROMPT
	STO 01
	X=0?
	SF00
	SF27
	STOP
	LBL A
	XEQ^{T}W
	XEQ^{T}Z
	^{T}ZC=
020	GTO^{T}L
	LBL^{T}Z
	RCL 02
	FS? 00
	GTO 02
	RCL 01
	/
	1.1
	+
	PI
030	*
	1/X
	X↑2
	RCL 01
	X↑2
	+
	SQRT
	4
	X><Y
	/
040	1
	E↑X
	*
	LN
	RCL 01
	*
	PI
	/
	XEQ^{T}K
	*
050	RCL 02
	+
	LBL 02
	1/X
	4
	*
	STO 04
	8
	RCL 00
	/
060	14
	+
	11
	/
	*
	STO 03
	X↑2
	PI
	X↑2
	XEQ^{T}K
070	*
	+
	SQRT
	RCL 03
	+
	RCL 04
	*
	1
	+
	LN
080	42.4
	*
	RCL 00
	1
	+
	SQRT
	/
	RTN
	LBL E
	CF27
090	^{T}Zc?
	PROMPT
	42.4
	/
	RCL 00
	1
	+
	SQRT
	*
	E↑X
100	1
	−
	STO 03
	11
	/
	4
	RCL 00
	/
	7
	+
110	*
	RCL 00
	1/X
	1
	+
	.81
	/
	+
	SQRT
	RCL 03
120	/
	8
	*
	STO 04
	^{T}We/H=
	ARCL X
	AVIEW
	PSE
	FS? 00
	GTO 03
130	RCL 01
	/
	.26
	−
	PI
	*
	1/X
	X↑2
	RCL 01
	X↑2
140	+
	SQRT
	4
	X><Y
	/
	1
	E↑X
	*
	LN
	RCL 01
150	*
	PI
	/
	XEQ^{T}K
	*
	RCL 04
	X><Y
	−
	LBL 03
	^{T}W/H=
160	GTO^{T}L
	LBL B
	RCL 00
	STO 05
	1
	STO 00
	FC? 01
	XEQ^{T}W
	XEQ^{T}Z
	X><05
170	STO 00
	XEQ^{T}Z
	RCL 05
	/
	1/X
	X↑2
	FS? 01
	RTN
	^{T}EREFF=
	GTO^{T}L
180	LBL C
	SF 01
	XEQ^{T}W
	XEQ^{T}B
	SQRT
	2.998E8
	^{T}HZ?
	PROMPT
	/
	X><Y
190	/
	^{T}GWL=
	GTO^{T}L
	LBL D
	XEQ^{T}W
	SF 01
	XEQ B
	SQRT
	2.998E8
	/
200	STO 08
	RCL 00
	STO 07
	1
	STO 00
	XEQ^{T}Z
	STO 06
	RCL 01
	STO 05
	^{T}H?
210	PROMPT
	STO 04
	ST* 02
	ST* 01
	^{T}S, HZ?
	PROMPT
	ST* 08
	*
	SQRT
	1/X
220	5.033 E2
	*
	ST+ 04
	CHS
	ST+ 02
	ST+ 01
	RCL 04
	ST/ 01
	ST/ 02
	XEQ^{T}Z
230	ST/ 06
	1
	RCL 06
	−
	27.288
	*
	RCL 08
	*
	RCL 05
	STO 01
240	RCL 07
	STO 00
	RDN
	RDN
	^{T}ATT=
	GTO^{T}L
	LBL d
	XEQ^{T}W
	SF 01
	XEQ B
250	−1
	X><Y
	+
	LAST X
	SQRT
	/
	RCL 00
	*
	LAST X
	1
260	−
	/
	27.288
	*
	^{T}LOSS T?
	PROMPT
	*
	2.998E8
	/
	^{T}Hz?
270	PROMPT
	*
	^{T}Ad=
	LBL^{T}L
	CF 01
	ARCL X
	PROMPT
	SF 27
	RTN
	LBL^{T}W
280	CF 27
	^{T}W/H?
	PROMPT
	STO 02
	RTN
	LBL^{T}K
	RCL 00
	1/X
	1
	+
290	2
	/
	RTN
	END

Instructions

- Key in program and initialize MICSTR
- Enter microstrip's dielectric constant and thickness-to-height ratio:
  (ϵ_r), R/S, (t/h), R/S
- To find Z_c, go to LBL A (016), specify width-to-height ratio:
  (w/h), R/S
- To find $\epsilon_{r_{eff}}$, go to LBL B (161), specify width-to-height ratio:
  (w/h), R/S
- To find λ_g, go to LBL C (180), specify width-to-height ratio, frequency:
  (w/h), R/S, (f), R/S
- To find α_c, go to LBL D (193), specify width-to-height ratio, height, conductivity, frequency:
  (w/h), R/S, (h), R/S, (σ), ENTER, (f), R/S
- To find α_d, go to LBL d (246), specify width-to-height ratio, tangent of metalization, frequency:
  (w/h), R/S, (tan δ), R/S, (f), R/S
- To find width-to-height ratio for previously entered dielectric constant and thickness-to-height ratio, go to LBL E (88), specify characteristic impedance by keying in (Z_c), R/S:
  Program displays w'/h momentarily, then displays w/h

Program partitioning

Block	Find	Location
A	(input)	001
B	Z_c	016
C	"	021
D	w/h	088
E	$\epsilon_{r_{eff}}$	161
F	λ_g	180
G	α_c	193
H	α_d	246
I	(output)	273

Registers 00 to 08 are in use

Engineer's newsletter

Tracking the sun with solar cells

A novel tracking device that locates the sun and controls drive motors to keep a solar collector facing it has been invented by Burrel E. Hammons of Sandia National Laboratories, Albuquerque, N. M. The device's shape partially shades four of eight small solar cells mounted on the sides and the base of a small, square pedestal when the solar collector is properly oriented to the sun. Until this position is reached, unequal voltages from the cells cause the drive motors to move the solar collector until the voltages are equalized. A ninth cell, mounted atop the pedestal, deactivates the tracking mechanism when the sun is obscured.

The simple and inexpensive device boasts **unmatched tracking accuracy on a clear day—to better than ±0.1°**—and the ability to find the sun even when the collector is facing away from it.

Card carries 6502's software information

Since the 6502 is the heart of the popular Apple, Atari, Pet, and Kim home computers, as well as numerous other products, any programming aid for this processor is certainly welcome. Micro Logic has come up with a plastic, three-color instant microprocessor reference card to save programmers and engineers time and effort in their 6502 applications. The 8½-by-11-in. two-sided card gives such information on the 6502 as the **instruction set, hexadecimal-to-instruction conversion, the ASCII character set, hexadecimal-to-decimal conversion,** the interrupts, the pinout, the instructions that affect flags, and much more. It costs $4.95 each for up to nine cards, plus $1 for postage and handling. Write to Micro Logic Corp., Department CE, P. O. Box 174, Hackensack, N. J. 07602.

Watch that solder sucker

Removing integrated circuits soldered directly to a printed-circuit board usually requires sucking away the solder from a reheated pad or plated through-hole. That is fine for bipolar circuitry, but it can be extremely dangerous for MOS devices. Dan Anderson, president of Anderson Effects, points out that **standard plastic solder suckers have been found to produce a static surge of 5,000 to 10,000 V at the tip.** This tip is invariably in direct contact with a device's lead when the surge occurs, resulting in a damaged or destroyed device. Anderson Effects and other firms now offer static-free metalized plastic models that produce no static charge. For more information, contact Anderson Effects Inc., P. O. Box 657, Mentone, Calif. 92359; (714) 794-3792.

Video tapes educate the pc industry

The Institute for Interconnecting and Packaging Electronics Circuits (IPC) has become active in producing and distributing video tapes for its industry. **Of more than 25 tapes now available, 5 are new releases,** including "Processes and Controls for Production Soldering," "Automation of PWB Production," and "Raw Materials Production: Challenges and Developments in the 1980s." Write to the IPC, 3541 Church St., Evanston, Ill. 60203, for price and ordering information.

How big a seller are chip-carriers?

The leadless ceramic chip-carrier is now for real. But just how big is the U. S. chip-carrier market? James D. Welterlen, a technical consultant, who looked at this field in a June 1979 report, has an idea, as he **recently finished his 1980 update.** For details, contact him at 7460 Girard Ave., Suite 8, La Jolla, Calif. 92037.

-Jerry Lyman

THE MOST POWERFUL BENCHTOP TEST SYSTEM IN THE WORLD.

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The LTS-2000 is a lot more than a simple tester. It's a powerful instrument you can use anywhere in your plant for almost any kind of test from basic go/no-go to full-blown Discrepant Material Reports. And it can not only test DAC's and ADC's but a wide variety of linear components, including Op Amps, regulators, comparators, bifets, etc. Test results are immediately displayed and printed, and full reports including statistical analysis, data log and summary sheets are available through the integral 20 column printer.

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The LTS-2000 gives you true "big system" performance, like system measurement accuracy to greater than 16 bits, ±1LSB; self-calibration and diagnostics, 16 bit microcomputer with 64K bytes of memory and more – all at ¼ the "big system" price.

EASY-TO-PROGRAM, EASY-TO-USE.

The unique design also allows for easy use. You can set up a program in minutes either with a program from the device library or with the complete test menu of fill-in-the-blanks software. Just snap in the appropriate family board module and socket module, plug in the device and press "GO" – the LTS-2000 does the rest. There's even a full-edit capability, so test parameters can be changed quickly and easily.

IT'S THE MOST VERSATILE BENCHTOP YOU CAN BUY.

You can not only use the LTS-2000 for incoming inspection, but component selection and grading, engineering analysis, quality control, final test, qualification test, and even as a diagnostic tool for component evaluation.

Never before has a compact benchtop linear test system offered so much versatility for so little. For more information on the LTS-2000, or the LTS-2010 which lets you program in BASIC, contact Greg LaBonte at (617) 273-4780, Analog Devices, P.O. Box 280, Norwood, MA 02062.

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Circle 159 on reader service card


16K
32K
64K
NC/Vcc CS2 Vcc/NC A8 A9 A12 PD/PGM A10 A11 Q8 Q7 Q6
VPP CS1 A7 A6 A5 A4 A3 A2 A1 A0 Q1 Q2 Q3 VSS
NC/Vcc CS Vcc/NC A8 A9 A12
VPP A13 A7 A6 A5 A4
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All devices in TI's TMS2500 EPROM Family are plug-compatible with each other. And will be with all the ones that are on the way. Pinouts are derived from popular industry standard ROMs for maximum compatibility.

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Plug-in compatibility means easy upgradability. From 8K to 64K. For upgrading from 16Ks to 32Ks, for example, just include the signal to PD in the address decoder. No jumpering. Minimal modification for upgrade to 64K. And beyond.

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All TI EPROMs facilitate rapid program changes in high-density fixed-memory applications.

A single TTL-level pulse allows simple in-system programming. In any order. Individually. In blocks. At random. Programming time is reduced to a minimum. And, you can use widely available PROM programmers. Erasing? Simple ultraviolet.

Family portrait.

Check the chart and choose the member of TI's growing EPROM Family for your application. From the world's fastest 8K to a high-performance 16K to a fast new version of the industry's first standard 32K to the industry's first 64K.

Availability.

Right now delivery on all devices from your local TI field sales office or authorized distributor.

For more information about the industry's first EPROM Family, and other Texas Instruments EPROM products, write to Texas Instruments Incorporated, P.O. Box 1443, M/S 6965, Houston, Texas 77001.

TI's Growing TMS2500 EPROM Family

Device	Description	Power Dissipation*	Access Time*
TMS2564-45	64K	840 mW	450 ns
TMS2532-45	32K	840 mW	450 ns
TMS2532-35	32K	840 mW	350 ns
TMS25L32-45	32K	500 mW	450 ns
TMS2516-45	16K	525 mW	450 ns
TMS2516-35	16K	525 mW	350 ns
TMS2508-30	8K	446 mW	300 ns
TMS2508-25	8K	446 mW	250 ns

*Worst case over operating temperature range

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Circle 211 on reader service card

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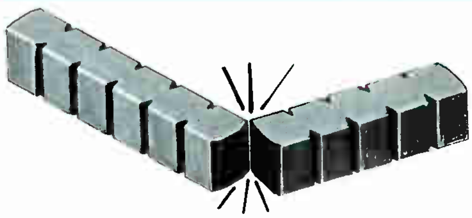

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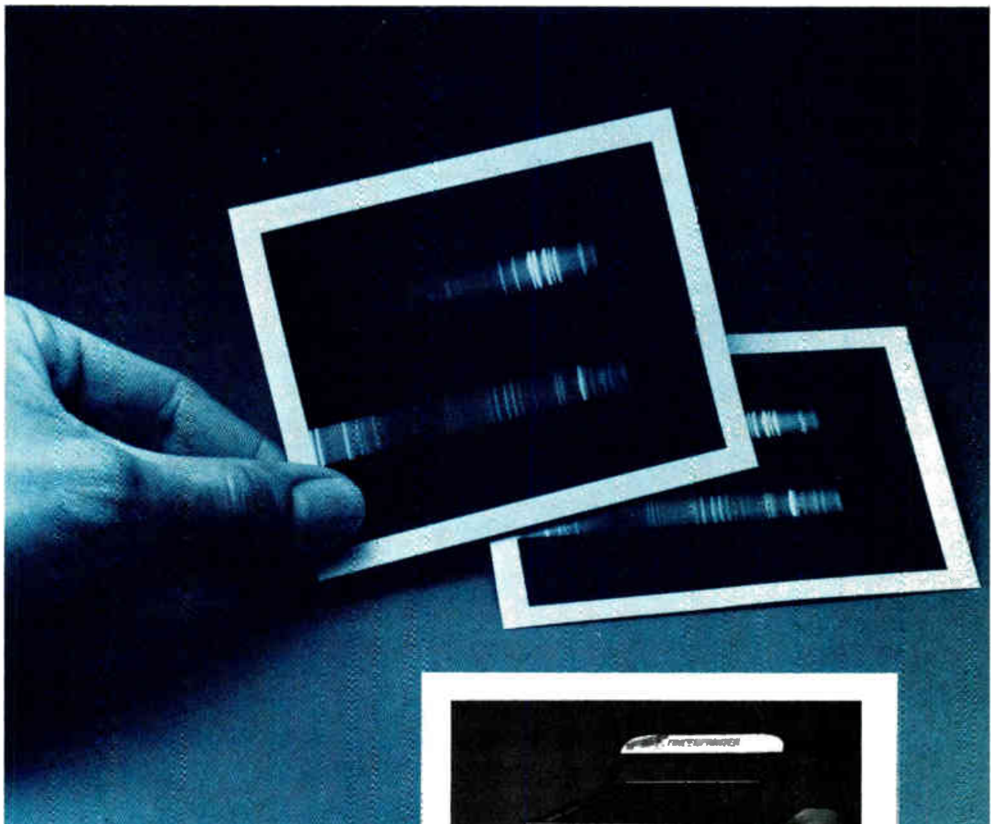
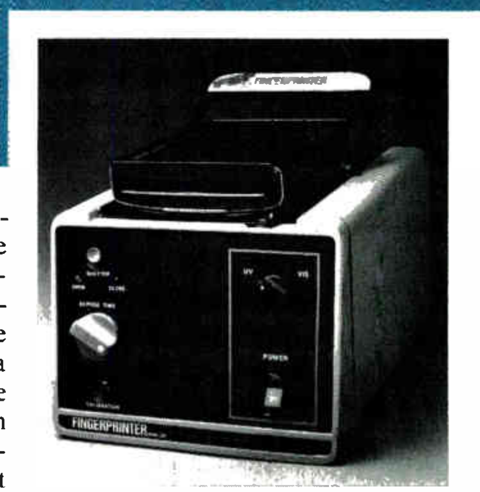
Circle 162 on reader service card

Spectrograph checks plasma process

Instrument takes photo of plasma operation's spectrum through viewport or optical fibers, adds reference

by Ana Bishop, Assistant New Products Editor





With so many plasma operations running on faith and good intentions, news of a fast and inexpensive way to detect contaminants, check vacuum operation, and analyze residual processing gases is welcome indeed. The Fingerprinter, the first product of a new Texas firm, Front End Processes Inc., promises to simplify on-line analysis of plasma-processing operations. The portable instrument uses gas spectrography, recording the data emitted by glowing plasma gases on Polaroid film. The resultant print becomes a unique fingerprint of the process at the time it was taken.

Comparisons. A glow tube of a standard processing plasma, such as argon, is built into the Fingerprinter. The tube supplies a spectrum reference that is printed alongside the spectrum of the process being checked. A technician can compare the spectra of the standard process and the tested processes to detemine whether all gases are present and check to see whether any contaminants have been introduced. The company suggests that each 3¼-by-3¼-in. print be used for immediate interpretation of the process and either stored for permanent record or attached to a batch of wafers to document a process's degree of perfection.

According to the company, the Fingerprinter is the first spectrograph designed specifically to aid in process control. It can be used for semiconductor manufacturing, in plasma and sputtering processes, and in determining the reliability of vacuum systems. It can be added to almost any process line, says the company, via a nonintrusive, noncontaminating viewport or an optical-fiber–bundle connection. Unlike quadrupole gas analyzers or scanning monochromators, the Fingerprinter does not require separate vacuum pumps or recorders. It is a compact 7.3 in. high by 7.1 in. wide by 11 in. deep, and the ease with which it may be connected to a vacuum line enhances that portability. It requires a 20-V, 60-Hz power supply.

The basic Fingerprinter is available for $7,500. Deliveries start in June. Though the Polaroid film can be obtained from any retailer, the maker will also stock it for the convenience of its customers. It will also make available later a high-speed Polaroid film for special applications. The instrument will be demonstrated at Semicon West.

Front End Processes Inc., 2912 Blystone, Dallas, Texas 75220 [391]

Card is smart node in industrial net

Communications controllers use serial links to form measurement and control network that offloads host computer

by James B. Brinton, Boston bureau manager

Industries are striving for increased productivity. The resulting growth in automation is being translated into countless sensors and actuators on factory floors, and the need for high-quality communication between these devices and central computers is expanding in due proportion.

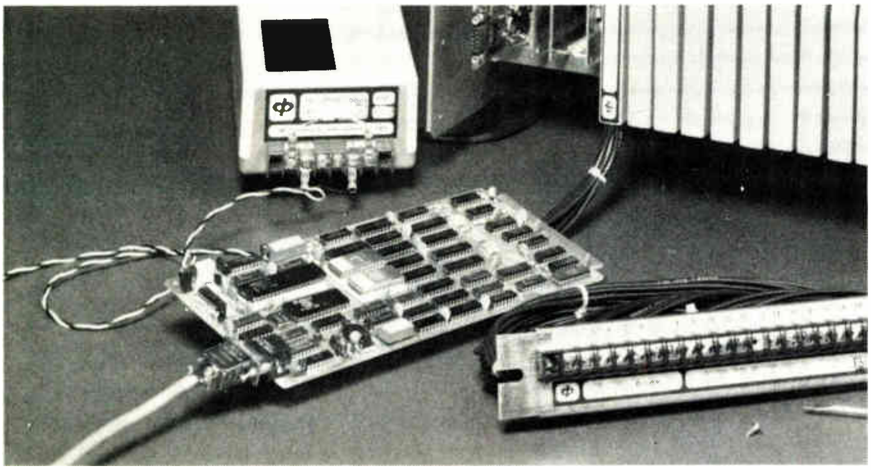
So far, the electronics industry has done its best to give users almost any form of communication an application requires, from digital formats to current loops. But as is so often the case, the diversity is itself a drawback for users, who need some form of standardization. Some relief from the large amounts of host processor overhead such communications imply is also called for. The vulnerability of some links to noise and error is another concern.

An intelligent communications control card from Computer Products Inc. called DIOC, for distributed input/output controller, addresses these problems. Representing a new method for designing distributed measurement and control networks, the controller is compatible with any existing computer and is specifically designed to work with the firm's RTP7400 series analog-digital input/output systems [*Electronics*, Sept. 11, p. 208].

The DIOC allows remote distribution of I/O functions, offloading from its host computer many communications functions formerly under time-consuming software control. It uses a single standard format—RS-232, at user-selectable rates of up to 19.2 kb/s. The system, which provides transmission-link security, offers error detection and correction as well.

The 9-oz, 9.45-by-4.53-in. DIOC card contains an Intel 8085 microprocessor, 4-K bytes each of random-access and read-only memory, a Usart (universal synchronous/asynchronous receiver/transmitter), and logic to interface with the RTP subsystem it serves. In ROM are power-up, self-test, and power-outage–sensing routines; the last two both trigger failure messages to the host, which can either reprogram the DIOC or call for repairs.

The system has simplicity going for it. A DIOC can be installed in the No. 1 card slot of an RTP7400-series subsystem—typically a comprehensive data-acquisition and -control system—and as many as seven other equally complex subsystems can be daisy-chained to the host via the one DIOC.

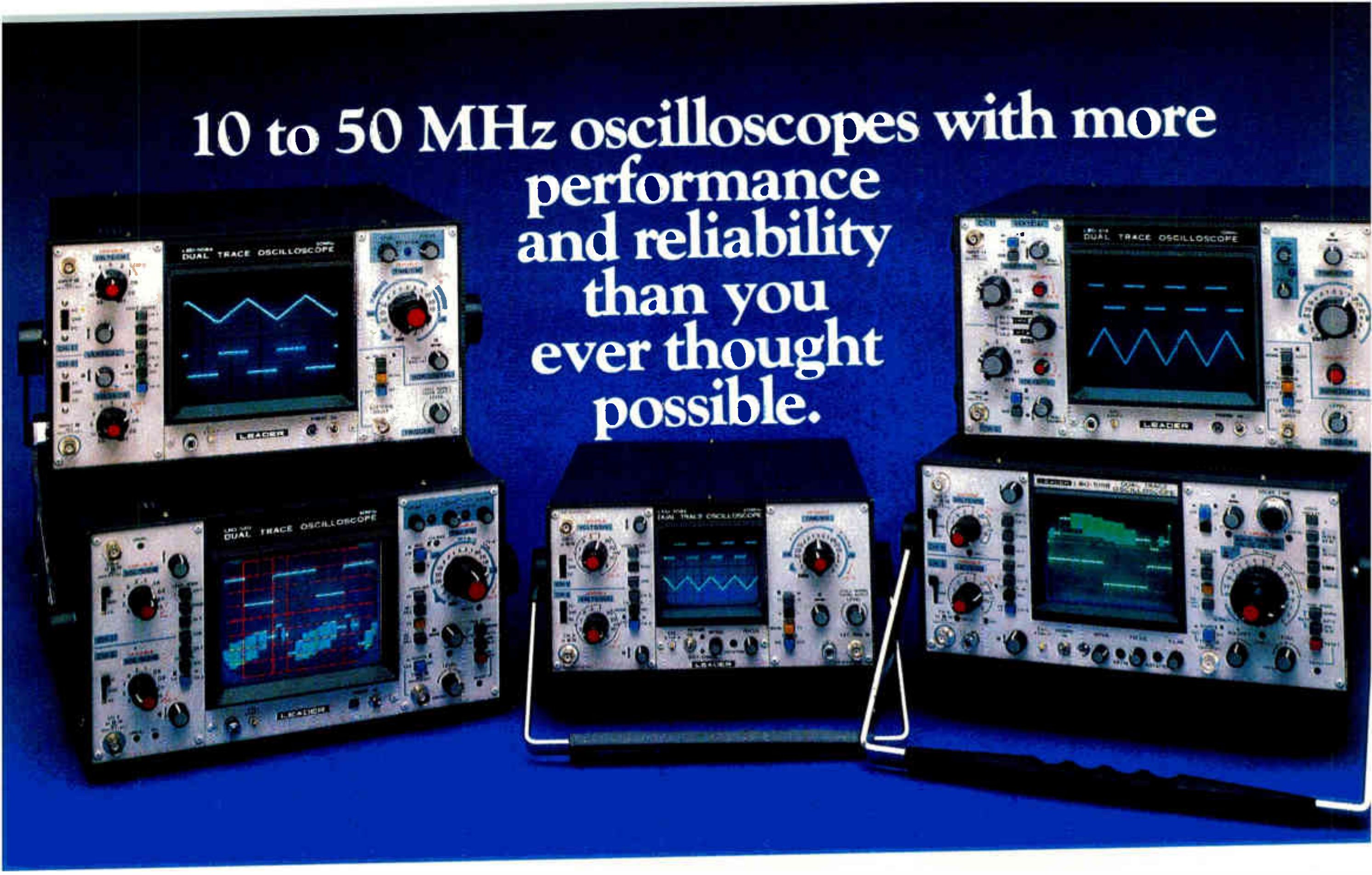


Net options. A network using 16 DIOCs in a multidrop configuration allows a host to monitor and control up to 65,536 analog or 32,768 digital points or combinations of either type. It is in applications like these that DIOC's assumption of communications tasks normally performed by the host becomes important. Without what the firm calls DIOC's block scan feature, each point would have to be addressed individually by the host. With DIOC they can be addressed in large blocks. Only a single host command is needed to acquire large amounts of data from subsystems.

In local applications, where sensors and actuators are close to the computer site, DIOC can be connected directly to one of its host's asynchronous serial input ports. Where long-distance transmission is needed, the DIOC communications are fed either to a Computer Products limited-distance multidrop modem or to a type-103 or -202 Bell System or equivalent modem.

Thus a host can be miles from the processes it monitors and controls or as near as the next equipment rack. In either case, the leads from sensors and controllers to the local RTP7400 subsystem are as short as possible.

All DIOC communications and I/O activities are controlled by the host, with a single host command sometimes triggering a cascade of DIOC



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LEADER's oscilloscope line includes 12 models, single and dual trace versions, for bench or field use. All models offer comprehensive triggering controls, TTL compatible Z-axis modulation, front panel trace alignment control and convenient, color-keyed front panel layout. Probes are furnished with every oscilloscope and options include probe pouches, carrying cases and front panel covers.

50 MHz alternate time base.

LBO-517 gives you complex analysis capability with alternate/composite triggering and simultaneous main/delayed time base display on its dome-mesh CRT with 20 kV accelerating potential. Has 7 ns rise time, 5 mV/cm sensitivity with X5 multiplier for 1 mV/cm up to 10 MHz, 5 ns sweep speed with X10 magnifier, and two trigger view channels.

The LEADER LBO-517 with dome-mesh CRT displays bright, clearly defined traces at all sweep speeds and repetition rates.

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LBO-515B is a dual trace oscilloscope with 4-inch CRT and parallax-free internal graticule, 5 mV sensitivity, 120 ns signal delay, trigger hold-off, delayed sweep and x-y operation at full sensitivity.

35 MHz with signal delay.

The dual trace LBO-520A combines 10 ns rise time with 5 mV sensitivity and 120 ns signal delay lines. Has 5.6 kV PDA CRT with internal graticule.

20 MHz dual and single trace.

LBO-508A and LBO-507A have 17.5 ns rise time with 1 M ohm input impedance. Automatic or external triggering, X5 sweep magnifier, 10 mV/cm sensitivity and add/subtract modes.

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LBO-514 has vertical and horizontal X5 magnifers, 1 mV/cm sensitivity and sweep speeds to 0.1 µs/cm. Auto or normal triggering. Z-axis modulation. (Single trace version, LBO-513.)

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LBO-308S gives lab performance and high reliability in field service. Sensitivity is 2 mV with complete triggering controls and 18 sweep ranges to 0.1 µs/div. with X5 magnifier. Dual trace, compact, lightweight with 3-inch, internal graticule CRT. Optional internal, rechargeable battery pack available.

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Circle 213 on reader service card

responses. For example, DIOC's block-scan feature allows the host to downline load scan tables (sequences of I/O operations) into about 3-K bytes of DIOC RAM. The DIOC can then be instructed to perform scans individually on demand or continually. In either case, the most recent data will be held in RAM, available on host request.

Single words. Company spokesmen feel that block scan will be DIOC's most used mode, though a programmed I/O capability has been retained—that is, the capability for single-word data transfers. Though costly in terms of host overhead, these small transfers are occasionally necessary.

Up to 16 scan lists can be assigned and maintained in DIOC RAM at one time. All 16 can run concurrently in the continuous mode, suspended when incoming messages require service. All housekeeping—such as RAM-address allocations, interrupt recognition, and error detection—is performed by the DIOC's 8085.

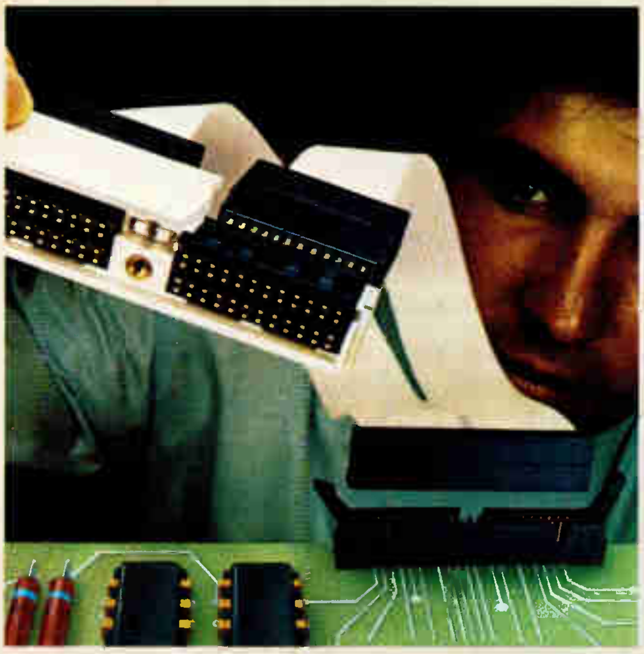
Predefined message formats (messages can be from 4 to 264 characters long) and cyclic-redundancy-check error detection help keep transmissions pure; there is parity checking on a per-character basis. There is also a check-before-operate mode that allows a host to verify a data transfer before altering data stored in RTP output cards. The proper control signal is almost always sent and commands that might be destructive are avoided.

The DIOC supplies so-called ACK and NAK message-status reports to its host, acknowledging or not the receipt of error-free data. When NAK is sent, retransmission takes place until the data arrives error-free and an ACK report is returned. The communications firmware in the DIOC includes a link time-out sensor that detects incomplete messages due to link failures. A NAK message is the response.

One DIOC costs $975 with discounts of up to 25% available depending on the size of the order; delivery is in 120 days.

Computer Products Inc., 1400 N.W. 70th St., Fort Lauderdale, Fla. 22207. [339]

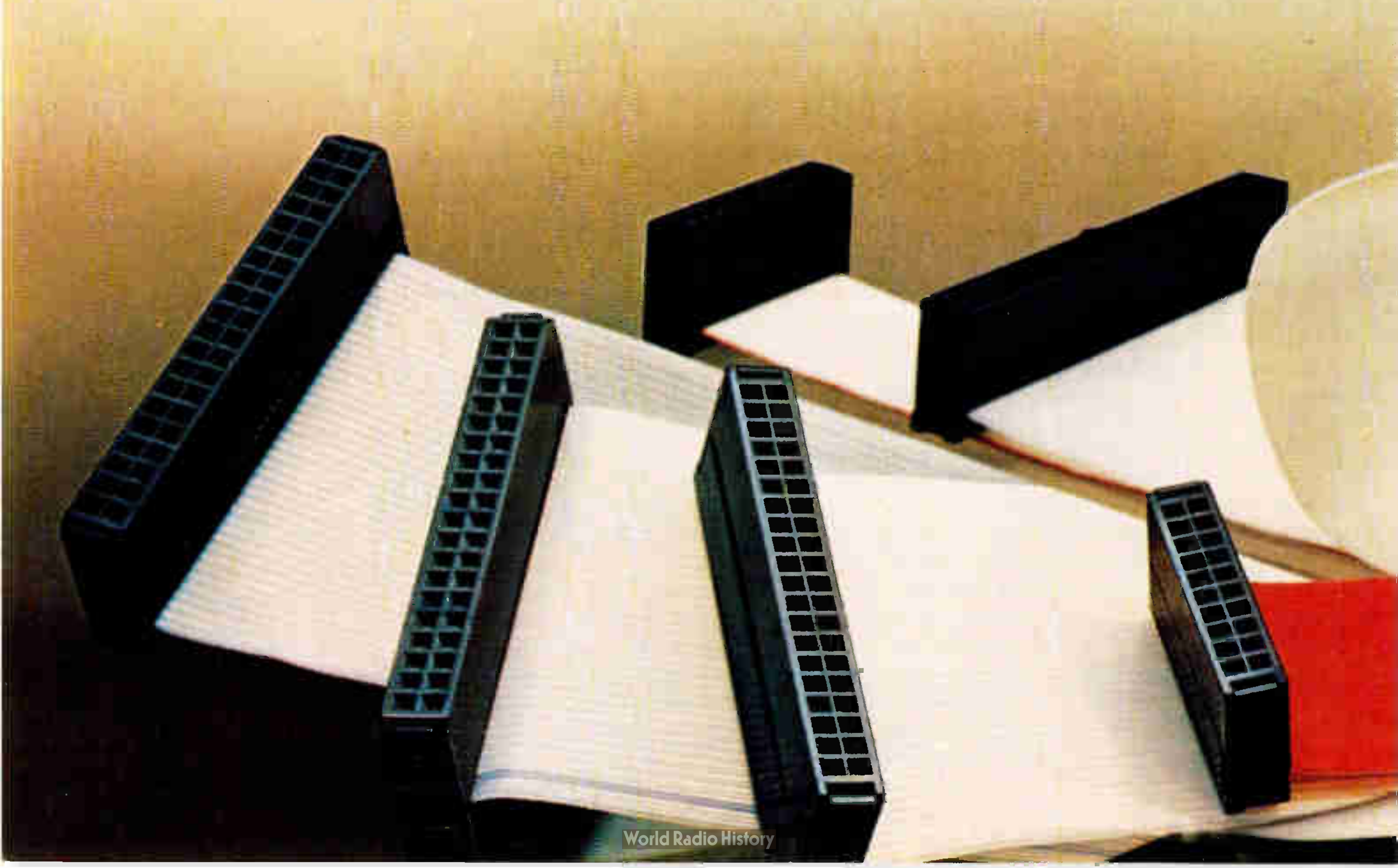
The first solderless transmission cable assembly protects your signals, and your costs.



The unique AMP connector mass terminates transmission cable far faster than soldering—and solderless design means you eliminate high cost, high-temperature cable. You can even forget tooling costs because we supply the assembly to your specifications.

The receptacle connector handles 100, 95, 75 and 50 ohm cables with signal conductors on .050″ centers. It automatically commons the grounds to your specified pin out. It physically separates and electrically isolates grounds from signal conductors. What's more, pinfield and SLT types are available, and all come in your specified length, and with your specified cable.

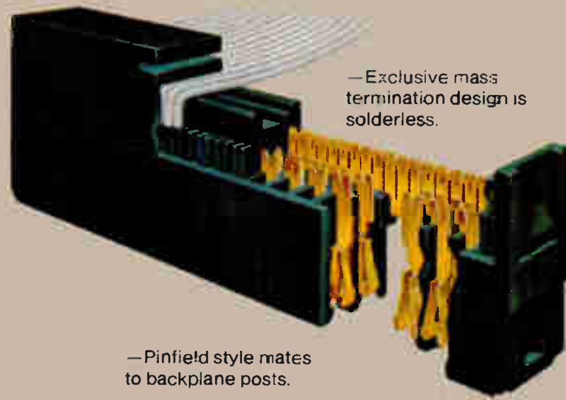
To get the crosstalk—and the cost—out, specify AMP transmission assemblies.



AMP Facts

Typical Mechanical/Electrical/ Environmental Properties

Mechanical	
Mating Force	8 oz. max./contact
Unmating Force	1½ oz. min./contact
Mating and Unmating	200 cycles
Vibration	15 G's, 10-2000 Hz
Physical Shock	100 G's, 6 millisec.
Electrical	
Current	1.0 ampere max./contact
Contact Resistance	25 milliohms max.
Insulation Resistance	5000 megohms min.
Dielectric Withstanding Voltage	500 volts RMS (sea level)
Environmental	
Temperature	−65°C to 105°C
Thermal Shock	5 cycles: −65°C to 105°C
Moisture Resistance	10 days, 25°C to 65°C, 80-98% R.H.
Salt Spray	5% solution, 48 hours
Industrial Gas	10% SO_2, 24 hours



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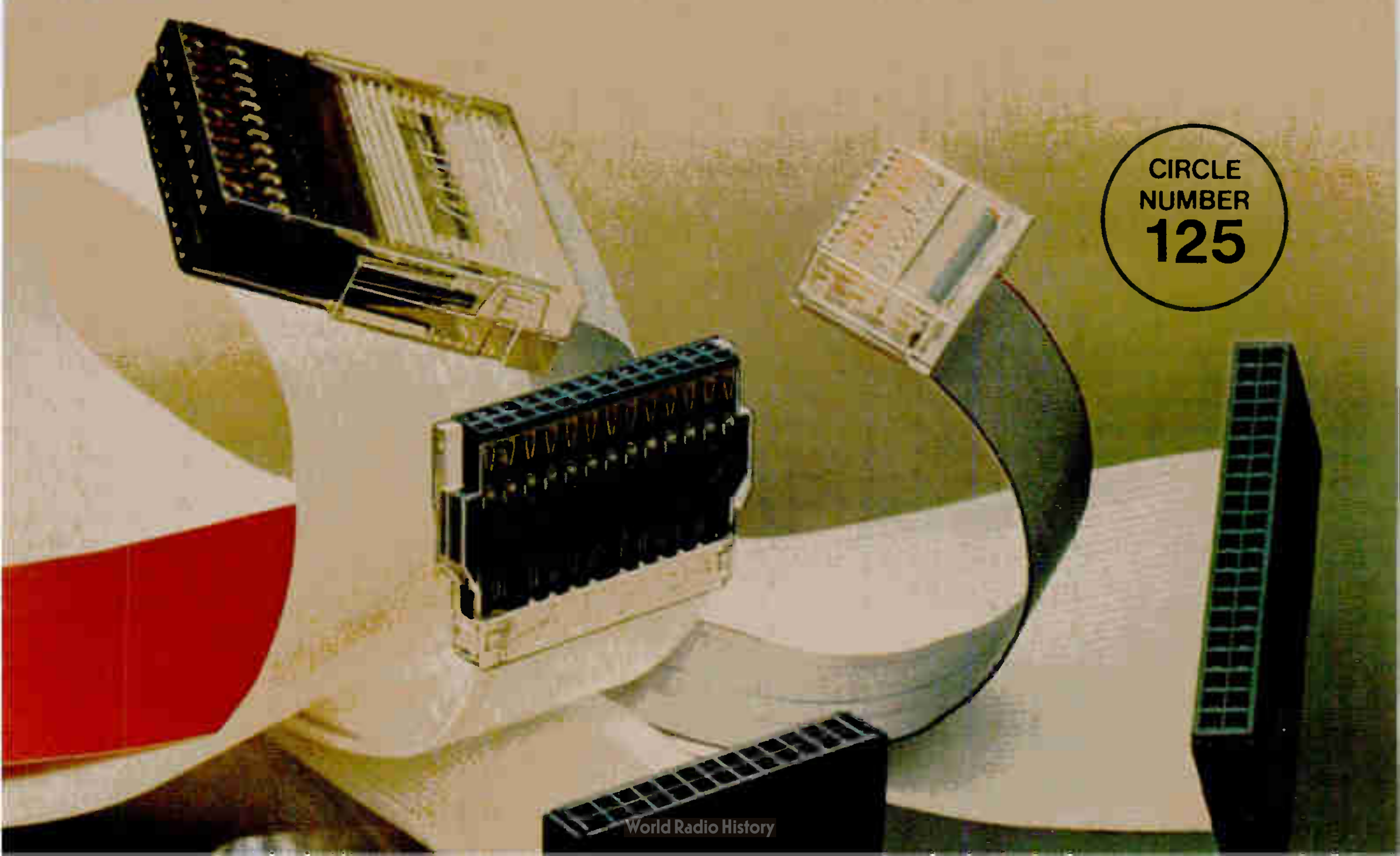


Op amp pair is tightly matched

Instrumentation amp's bipolar pair achieves 90-μV maximum offset voltage match; input bias cancelation shrinks error

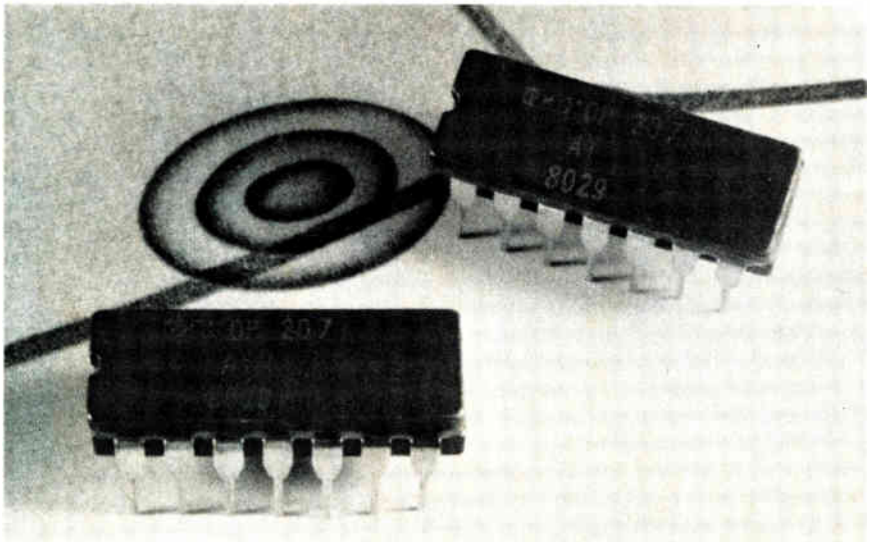
by Bruce LeBoss, San Francisco regional bureau manager

Matched pairs of operational amplifiers have in recent years given design engineers a powerful tool for solving design problems of the kind encountered in true instrumentation amplifiers. A pioneer in this field, Precision Monolithics has a new series of dual-matched instrumentation op amps with exceptionally low offset voltage and extremely tight matching of critical parameters.

Designated the OP-207, the bipolar devices consist of two independent high-performance op amps in a single 14-pin dual in-line package. Its offset-voltage match of 90 μV maximum (30 μV typical) at 25°C makes the OP-207 about twice as good as earlier dual-matched instrumentation op amps, says Tom J. Schwartz, a PMI product marketing engineer. PMI's OP-10, with an offset voltage match of 180 μV, was previously the lowest offset match available, he adds.

The amplifier characteristics of the matched device are more impressive than those of the individual amplifiers it contains because the output offset error of dual matched op amps is a function of the difference, or degree of matching, between the amplifiers' offset voltages. Nonetheless, the maximum 100-μV (35 μV typical) offset voltage of the individual amplifiers, Schwartz notes, "is at least a fivefold improvement" on the parameters of the individual op amps in the OP-10. Tracking over temperature has been pushed from an offset voltage match of 1.3 μV/°C maximum in the OP-10 to 1.0 μV/°C.

In a typical configuration employing two or three such devices, "users previously had to tweak the op amps to match the offset," says Schwartz. The OP-207 makes it possible to eliminate the trimming and, in numerous cases, the trimmer potentiometers themselves. Tight matching and close tracking make the OP-207 "particularly suited for building dual tracking power supplies and voltage regulators," Schwartz claims.



Low I_{BIAS}. In addition to improved offset-voltage parameters, the OP-207 features significantly lower input offset current (I_{os}) and input bias current (I_b). The I_b of the individual amplifiers is a maximum 3.0 nA at 25°C, 1.0 nA typical, while I_{os} is 2.8 nA maximum and 0.9 nA typical. For the matched pair, the average noninverting I_b is 3.5 nA maximum and 1.5 nA typical, while both inverting and noninverting I_{os} are a maximum of 3.5 nA, 0.7 nA typical.

Such low input bias current is achieved with an input-bias cancelation technique developed by PMI several years ago and employed on several earlier op amps. "It is a particularly important feature with high source impedances," states Schwartz. High impedances cause error to grow rapidly in the absence of an active input bias circuit.

Among other key specifications of the OP-207 are: a 100-dB minimum common-mode rejection match, 90-dB maximum power-supply rejection match, a maximum of 0.6 μV peak-to-peak noise, and long-term drift of 1.5 μV/month. Operation is from a $\pm$22-V power supply, and internal power dissipation is 500 mW. The operating temperature range is 0° to 70°C for commercial-grade parts. Devices covering military temperature ranges (−55° to +125°C) also are available, as are devices in 14-pin ceramic DIPs.

Prices start at $19 each, in quantities of 100. Availability is from stock to 30 days after receipt of order.

Precision Monolithics Inc., 1500 Space Park Dr., Santa Clara, Calif. 95050. [340]

it. Similarly, the 7234 can drive one more 18-segment alphanumeric character than can the 7233, a total of five. In both cases, however, this is done at the cost of ease in interfacing and requires that data and address information be entered in a serial format.

The input levels of the display decoder-drivers are TTL-compatible, and the "data accepted" output of the serial-input devices will drive one low-power Schottky TTL load. All members of the family use an internal string of three equal-value resistors to generate the intermediate voltage necessary to drive the display. One end of the string is connected to the power-supply voltage, and the user-input end is available at the display-voltage pin. "This allows the display voltage input to be optimized for the particular liquid-crystal material," Wells notes.

The display voltage of each device is independent of the power supply. As a result, the user can control the display operating voltage and LCD temperature compensation. What's more, a totally self-contained on-chip oscillator generates all display timing. No other components are needed. According to Wells, the single-chip drivers perform the functions of two to five devices that might otherwise be used.

Fewer pins. Perhaps equally important to display manufacturers, the chips significantly reduce pin count. "Previously, annunciators would have been driven separately from the display," Wells says. Thus, to drive 10 digits and 20 annunciators, as the 7232 does, "would have required about 75 to 80 pins to drive directly. By triplexing, pin count is nearly halved, and we can get more functions in the display."

Fabricated using Intersil's proprietary MaxC-MOS process, the devices have a total power consumption of 200 μW typically, 500 μW maximum, when operated at 5 V. A low-power shutdown mode retains data with a typical power consumption of 5 μW at 5 V and 1 μW at 2 V. The decoder-drivers dissipate 0.5 W at 70°C and operate at from −20° to +85°C.

Housed in a 40-pin plastic dual in-line package the drivers are priced at $16.20 each in lots of 24 or less and at $10.77 apiece for 100 or more. They can be delivered in 30 days.

Intersil Inc., 10710 N. Tantau Ave., Cupertino, Calif. 95014. Phone (408) 996-5000 [342]

Optoisolator's 8-V output drives logic directly

Dionics has entered the optoisolator business with the Iso-Gate, a device combining an 8-V, 16-diode array chip with a light-emitting-diode chip in a package that has an optical-coupling coating. Most photovoltaic devices produce only about 0.5 V and need external circuitry, including resistor networks, to produce enough voltage to drive MOS field-effect transistors in solid-state relays and switches. In contrast, the new hybrid circuit's LED triggers its own light-sensitive diodes to generate sufficient voltage.

The device is available in TO-5, TO-18, and miniature dual in-line packages with output ratings of up to 8 V at 3 μA, 8 V at 6 μA, and 16 V at 3 μA. Iso-Gate can be used as a gate drive for MOS devices, an interface between logic circuits and external loads, and as a digital voltage signal source.

Based on initial tests with the LED drive at 25 mA, the manufacturer says that Iso-Gate has a typical response time of 5 to 10 μs, a typical open circuit voltage of 6 V, and a typical short-circuit output current of 3 μA. In quantities of 100, prices begin at $5.00. Delivery is from stock to six weeks.

Dionics Inc., 65 Rushmore St., Westbury, N. Y. 11590. Phone (516) 997-7474 [343]

Analog divider is accurate to within 0.25%

A precision two-quadrant analog divider, DIV100 has an accuracy of within 0.25% over a 40:1 denominator range without external adjustments, even when the voltage is as low as 250 mV. The DIV100, which uses dedicated log-antilog techniques, consists of four operational amplifiers and logging transistors integrated into a single integrated circuit with a laser-trimmed thin-film resistor network. Housed in a 14-pin dual in-line package, it has input limits of 0 to +10 V on the denominator and ±10 V on the numerator, an output voltage of ±10 V minimum, and an output current of ±5 mA and uses power-supply voltages of ±12 to ±20 V (±15 V nominal).

In quantities of 100, the DIV100HP model, accurate to within 1%, sells for $17.25, the DIV100JP (to 0.5%) for $26.45, and the DIV100KP (to 0.05%) for $40.25. Delivery is from stock to four weeks.

Burr-Brown, Box 11400, Tucson, Ariz. 85734. Phone (602) 746-1111 [344]

10-A, 30-to-45-V rectifiers come in TO-220 packages

A series of single Schottky rectifiers rated to operate at 30 to 45 V with a continuous dc output of 10 A can be used for 5-V switching power supplies in the 10-to-50-W range. The 10TQ series has the low maximum peak forward voltage characteristics of Schottky devices that result in energy-efficient circuits. In addition, the rectifiers' low inductance permits faster switching for operation at frequencies of 100 kHz and above.

The TO-220 plastic packaging on the units simplifies mounting on printed-circuit boards and heat sinking. Although the rectifiers, produced by the company's own 830 process, allow nonrepetitive operation to junction temperatures of 170°C, the plastic package limits repetitive operation to 150°C. No voltage derating is required over the devices' full temperature range.

Prices range from $6 each for quantities of under 24 units to 90¢ in large volumes.

International Rectifier, 233 Kansas St., El Segundo, Calif. 90245 [345]

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Circle 215 on reader service card

Instruments

Scope gains third channel

100-MHz unit's extra channel adds flexibility in observing multiple digital signals

Entering the low-cost 100-MHz portion of the U. S. scope business now dominated by Tektronix' workhorse, the 465B, is the COS-6100 oscilloscope from Kikusui International. It has a feature that contributes to its usefulness in logic analysis: a third vertical channel.

The third channel makes it possible "to look at five channels of digital data in real time," says William B. White, the firm's vice president of marketing. In addition, the 6100 has two trigger-viewing channels (which display events triggering the sweep signals) and an extra mode that permits the scope, via the alternate sweep feature, to display a total of 12 traces. A television synchronization circuit for viewing video signals is also standard.

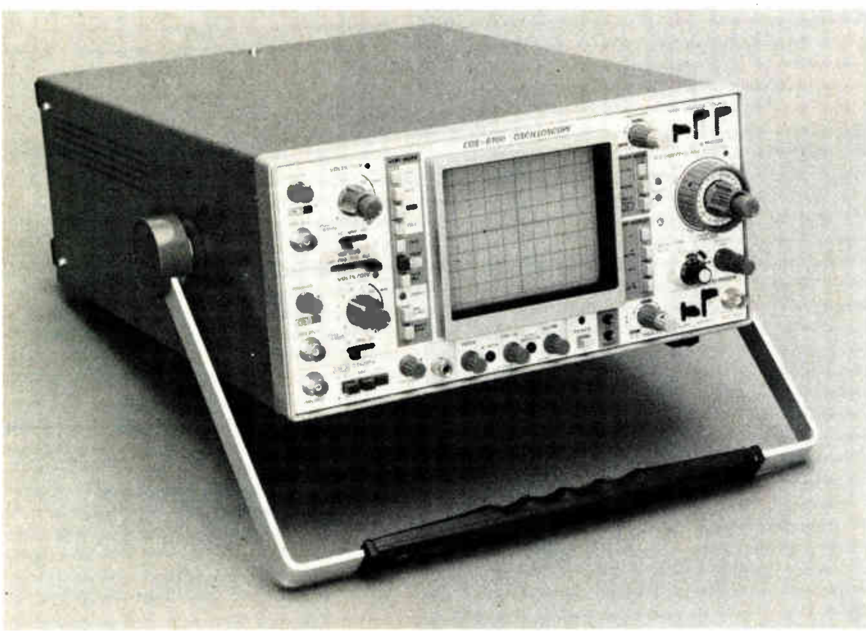
The added features position the $2,695 scope for the midpoint of a market stimulated by a growing number of users who need a logic-analysis capability but balk at the stiff price tags of dedicated systems.

At the crest. A Tektronix marketing executive confirms that logic analyzers are not finding their way into service as rapidly as predicted and that his firm also sees 100 MHz "in the center of the curve." Both Tektronix and Kikusui believe pricing is important, with scopes having an edge of approximately 50% over analyzers.

With a 100-MHz scope, most fast bipolar logic signals can be examined in real time. Kikusui's unit has a rise time of approximately 3.5 ns and sweep rates of 20 ns to 0.5 ms per division. At 10× magnification, the sweep rate is 2 ns to 50 ms per division, accurate to within ±2%.

Three vertical input channels give flexibility in comparing numerous signals. "You can punch up one channel at a time, or all three," allowing the user to sum, alternate, and chop the total of 12 signals—the most available in the low-price range, White says. Any two of the three channels may be used to form an X-Y display.

For channels 1 and 2, the sensitivity is 5 mV to 5 V per division or 1 mV to 1 V per division with a 5× magnifier; accuracy is to within ±2% or to within ±4% with 5× magnifier. The −3-dB frequency response for dc coupling is dc to 100 MHz, and for ac coupling it is 10 Hz to 100 MHz. The upper frequency limit drops to 10 MHz with the 5× magnifier. Channel 3 has a sensitivity of 0.1 to 1 V per division, accurate to within ±3%. The chop frequency is approximately 500 kHz.



For horizontal display, there are four sweep modes: A, A intensified, alternate time base, and B delayed. In the A mode, hold-off time may be varied from (made wider than) the sweep length by a factor of two or more. In the B mode, sweep time is 20 ns per division to 0.5 s per division with a 10× magnifier. The cathode-ray tube itself has an acceleration voltage of approximately 15.5 kV and a display area of 8 by 10 1-cm divisions.

The Japanese-made scope consumes approximately 50 W, weighs about 22 lb, and is 7.5 by 14.6 by 18.9 in. deep. It will be available in sample quantities late this month and in quantity by May.

A subsidiary of Kikusui Electronics Corp., a leading Japanese test equipment manufacturer, Kikusui International is expanding its scope line. The most recent additions till now were 50- and 35-MHz units.

The 1600 is the first but not last 100-MHz member of the line, says White, and in his view, could well set off competitive upgrading, "which to me smacks of a horsepower race." A Tektronix official, however, thinks "merely adding more bells and whistles will not make any difference to field users."

Kikusui International Corp., 17121 South Central Ave., Unit 2M, Carson, Calif. 90746. Phone (213) 638-6107 [351]

6½-digit DMMs offer high performance for under $3,000

In the 9574 series of 6½-digit multimeters from Guildline Instruments [*Electronics*, Jan. 20, p. 34], even the most fully configured model—with ac and dc current-measuring capability, a feature seldom seen in DMMs—sells for just $2,995. All of the members of the family come

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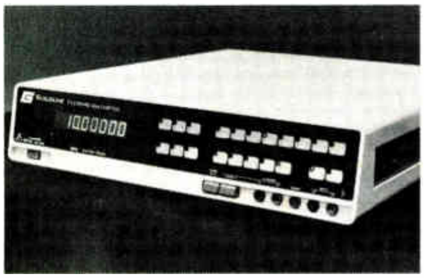
Circle 179 on reader service card



with IEEE-488 interfaces and not only perform complete self-checks at startup, but refuse to function when they do not meet their own specifications for accuracy of calibration or when they cannot be nulled.

The meters all have identical front panels, but function selectors will, when pressed, indicate whether the function requested is or is not included in the particular model. Autoranging is included in the instruments' repertoire, being performed before measurement to save time.

The 24-hour accuracy specification for dc voltage in the DMMs is ±(0.002% of reading + 6 digits) or better in its five (100 mV to 1,000 V) ranges. A ratio function is provided in addition to resistance, true-rms, average ac, and current functions. Using a proprietary digitizing technique, 9574 meters can put out 3½-digit readings at a 300/s rate.

A blank-faced version of the DMMs for use in dedicated systems has a dc voltage function and bus interface and is the lowest-priced of the family at $2,495. All versions are available within 30 days.

Guildline Instruments Inc., 2 Westchester Plaza, Elmsford, N. Y. 10523. Phone (914) 592-9101 [353]

Low-cost benchtop IC tester does job of $100,000 system

The Spectrum Series I benchtop integrated-circuit test system has been specifically designed to provide the same test results as a large, $100,000 system in incoming inspection applications, but to do so at half the cost. The unit's test head will test devices with up to 48 pins, and the basic system is priced between $41,000 and $84,000, depending on the number of pins requested.

The basic Spectrum Series I consists of a main chassis containing a minifloppy-disk drive, plus a test-head containing the pin-drive cards for each pin. The two are connected by a flexible cable. The tester is able to test all types of digital devices, all currently popular technology, says the manufacturer. It contains programmable phase clocks, high-speed data buffers, and an optional pattern generator for high-speed testing of microprocessor and memory devices. Through an RS-232 port, it automatically tests and controls such optional peripherals as a line printer, a strip printer, a cathode-ray tube with a keyboard, and a terminal. An optional IEEE-488 bus interface will enable the Spectrum to be connected to an existing host computer for multiple test-station applications. The tester can also be interfaced with manual and automatic device handlers for greater throughput.

The Spectrum Series I will be available for delivery in March.

Datatron Inc., 2942 Dow Ave., Tustin, Calif. 92680. Phone (714) 544-9970 [354]

Unit tests impedance, gain, phase delay at low frequency

Designed for making low-frequency (5 Hz to 13 MHz) evaluations of one- and two-part components, devices, and circuits, the model HP 4192A impedance and network analyzer measures 11 impedance parameters as well as gain, phase, and group delay. The instrument tests either floating or grounded devices, offering 4½-digit readings with a basic measurement accuracy of 0.3%. Impedance parameters measured by the HP 4192A include L, C, R, Z, Y, phase angle, X, G, B, D, and Q. The unit, says the manufacturer, is suitable for use in such applications as testing of materials, evaluation of capacitive and inductive devices mounted on printed-circuit boards, evaluation of semiconductors, and testing of crystals.

The U. S. price of the low-frequency impedance analyzer is $11,550. Deliveries begin in March.

Hewlett-Packard Co., 1507 Page Mill Rd., Palo Alto, Calif. 94304 [355]

Benchtop linear test system is programmable in Basic

Virtually any linear device can be tested to its own specified parameters on the first benchtop test system that can be programmed in the Basic language. Not only does the LTS-2010 system offer fill-in-the-blanks programming, it also yields production throughput that is comparable to that of mainframe testers. For example, typical test times are 800 ns for operational amplifiers and 5 s for digital-to-analog converters. The instrument will test d-a converters with up to 16 bits of resolution and ±0.01% accuracy.

The basic LTS-2010 includes a 5¼-in. double-sided dual-floppy disk drive, a 16-bit central processing unit, 64-K bytes of random-access memory, Basic software, two operating-system disks, a printer, a display, and a keypad for $29,000. IEEE-488 and RS-232 interfaces are standard. Family boards with all the circuitry needed to measure a general class of components sell for $3,000 apiece.

Analog Devices Inc., Component Test Systems Division, 10 Corporate Place, Burlington, Mass. 01803 [356]

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TIP 31A/B/C	NPN		5A	40W
TIP 32A/B/C	PNP		5A	40W
TIP 41A/B/C	NPN			
		40-100V	10A	65W
TIP 42A/B/C	PNP			

2N 6121/2/3	NPN	45-80V		
2N 6124/5/6	PNP	45-80V		
			7A	40W
2N 6288/90/92	NPN	30-70V		
2N 6107/9/11	PNP	30-70V		
2N 6486/7/8	NPN	40-80V	15A	75W
2N 6489/90/91	PNP	40-80V	15A	75W

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Microcomputers & systems

Board controls five serial ports

Communications controller supports expanding Multibus systems with versatile I/O

The BP-0575 serial communications controller from NEC Microcomputers Inc. sports five independent, individually configurable communications channels and full Multibus compatibility—a design intended for a wide range of applications.

"Original-equipment manufacturers are designing more complex systems, or want to build in the potential for more complexity down the road, so we're giving them more I/O capability per board," comments senior vice president George W. Muller. Most other boards of this type offer only three or four channels, he says.

At $550 in hundred-unit orders, the BP-0575 also is an attractively priced alternative for process control, medical instrumentation, or small-business data-base systems, Muller asserts. "A lot of folks make similar boards, but for flexibility and per-channel pricing, I think we're ahead of the game."

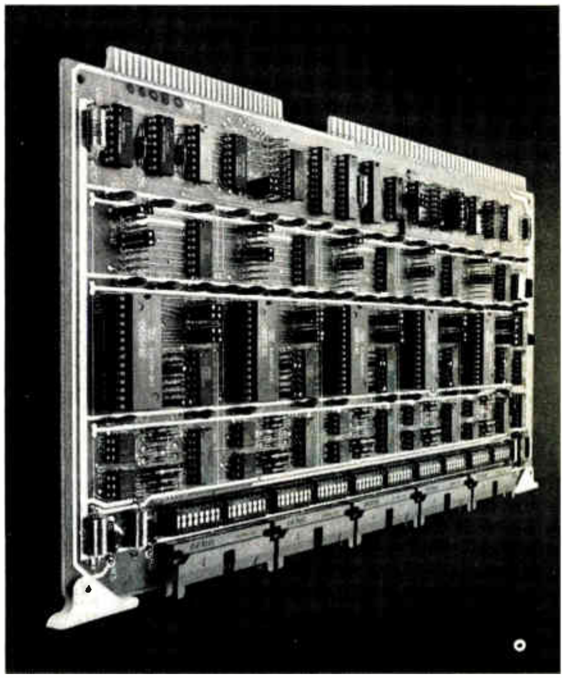
The BP-0575 communicates in parallel format on the Multibus with 8- and 16-bit host microprocessors and in serial with terminals, modems, and printers through RS-232-C or optically isolated 20-mA current-loop interfaces. The controller board also allows bidirectional serial communication between microprocessors. A single-cable network can be put together using the added I/O ports; nodes may be added simply by inserting drops along the line.

Backing each of the BP-0575's simplex or duplex communication channels is NEC's μPD8251A, an industry-standard programmable communications interface integrated circuit, and associated circuitry that supports all standard RS-232-C and modem control signals.

Jumper-selectable features let users configure the communication channels individually in a number of ways, points out Richard J. Weiner, engineering manager for board products. Data-transfer rates can be set from 75 to 19,200 b/s on the RS-232-C interface or from 75 to 2,400 b/s on the control-loop interface. Users may also put together an on-board interrupt scheme, grouping any desired combination of transmit- and receive-interrupt lines for the five ports, and so decrease the number of bus interrupts used by the board.

Addressing. The 16-byte block register of the BP-0575 can be placed on any 16-byte boundary within the input/output space of the host microprocessor, and 12 jumper-selectable I/O ports within the 16-byte block can access the board. Users may address the board's five serial channels and the two interrupt status registers in any order or priority in the addressed block.

The BP-0575 requires a single 5-V power supply, typically at 0.9 A. Operating temperature ranges from 0° to +55°C. Full production of the BP-0575 controller gets under way in March, although limited quantities are available currently, says



Muller. Delivery takes four weeks after receipt of order.

NEC Microcomputers Inc., 173 Worcester St., Wellesley, Mass. 02181. Phone (617) 237-1910 [371]

$995 S-100 computer uses ROM-based programs

The System Zero Computer executes programs based on random-access memories on the S-100 bus. It has a basic price of $995.

The computer comes with a Z80A-based single-card microcomputer, 1-K byte of RAM, and 3-K bytes of Control Basic in read-only memory. An additional three slots on the S-100 bus are available for extra memory and input/output cards.

A special version, System Zero/D is available for use with floppy disks. This $2,995 machine includes the Z80A card, 64-K bytes of fast RAM, and a floppy-disk controller card for use with disk drives that can store 390-K bytes on each 5-in. diskette. Also included are the RDOS-2 disk-operating system and system diagnostics.

The Zero/D sells for $1,295 and can be used with the model DDF dual-disk drive with single- or double-sided and single- or double-density diskettes. Currently available software for the System Zero is available in RPG II, Fortran, Cobol, 32K Structured Basic, 16K Basic, and Lisp languages and includes word processing, data-base management, and business application programs, as well as sophisticated disk-operating systems.

Cromemco Inc., 280 Bernardo Ave., Mountain View, Calif. 94043. Phone (415) 964-7400 [374]

64-, 256-K-byte RAM cards interface with EXORcisor bus

Novex Inc., a young Maryland firm with its sights trained on the EXORcisor-compatible board market, is offering battery-backable 64- and 256-K-by-9-bit random-access memory cards for the Motorola development systems. The 9.75-by-6-in. memory cards are priced substantially lower (more than 60% lower at the 64-K-byte level) than comparable Motorola memory cards.

The 2-MHz boards enable use of a hidden-refresh system called Cycle Salvaging that speeds up critical input/output operations by avoiding interruptions for refreshing. The methods suggested improve I/O speed over other 2-MHz memories, says the firm, a frequency at which conventional hidden refresh is not feasible.

A programmable read-only memory permits fixed memory mapping in 2-K-byte increments for the lower 64-K bytes on the board. Small on-board switching regulators allow 5- or 12-V battery operation.

The 256-K-byte card, not intended to withstand high vibration, uses stacks of four 16-K dynamic RAMs with pins soldered directly to the pins on the chip below (except for one pin each wired to the board for chip selection). It is priced at $2,475 in single units and $1,510 in lots of 100. The 64-K board is priced at $975, $595 in 100s; both are available in 30 days.

Novex Inc., P. O. Box 3006, Gaithersburg, Md. 20760 [376]

ROM emulator traces program execution in real time

A stand-alone read-only-memory emulator simulates, reads, and programs 2708, 2716, and 2732 erasable programmable ROMs, tracing program execution in real time by emulating the ROM instead of the microprocessor. Called the Micro Memory Tracer, the emulator has an alphanumeric keyboard and a cathode-ray tube for displaying the simulated ROM's access map and the memory's contents.

The unit is used independently of both the host system and the microprocessor under test. Object programs are downloaded from the host development system or timeshared computer to high-speed random-

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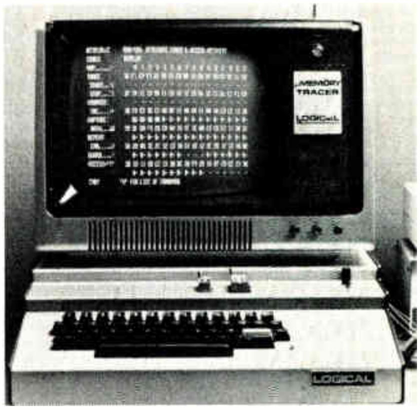
Circle 185 on reader service card

New products



access memory within the tracer via an RS-232 port. The tracer displays 256 data-bus samples from the trace operation, counts accesses to specified locations during a trace, and sends outputs to a line printer.

With operator's manual and the choice of E-PROM emulator cable, the model 800 Micro Memory Tracer sells for $3,995. Extra cables conforming to the other two E-PROM pinouts cost $45 apiece.

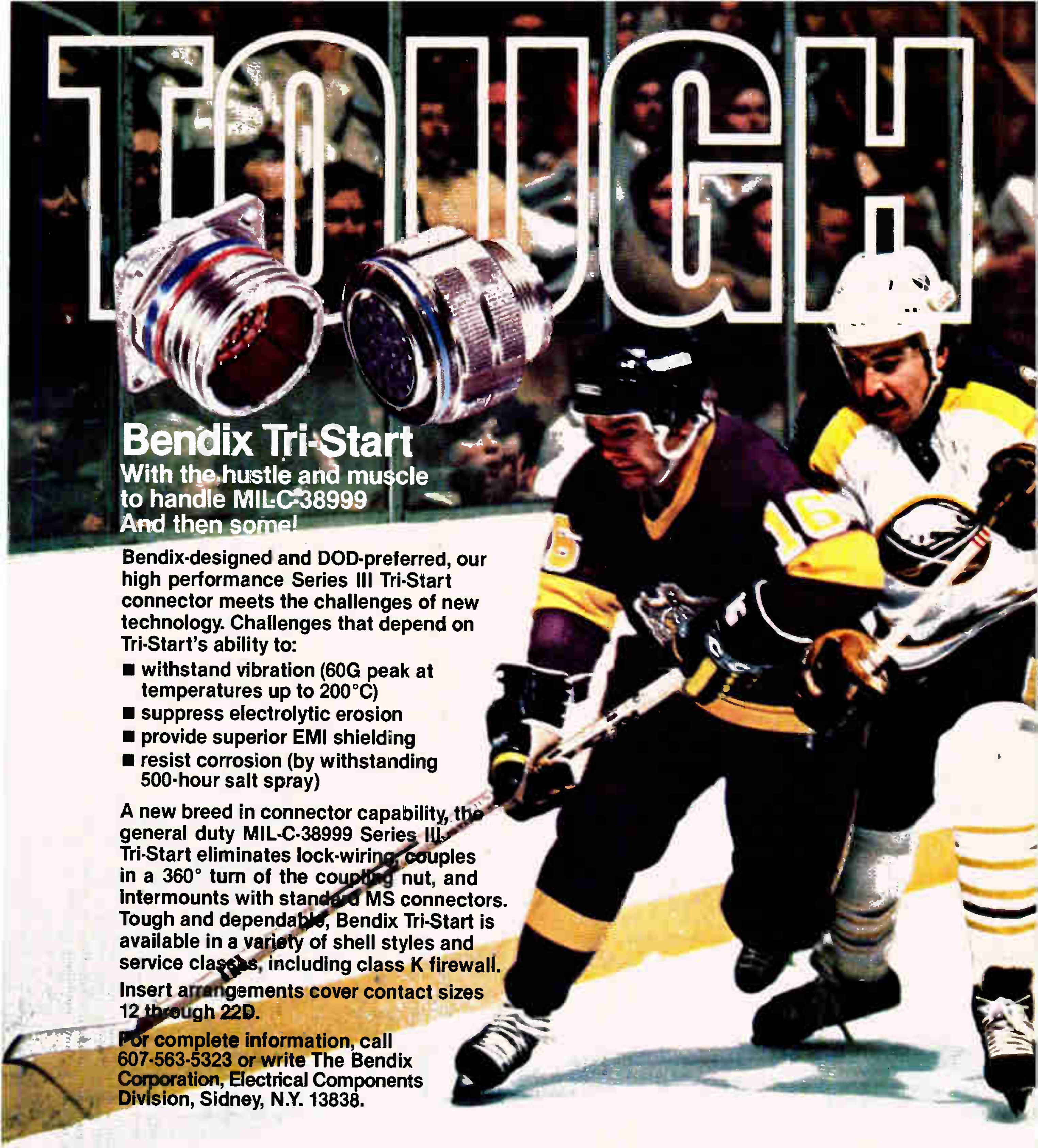
Logical Services Inc., 2340A Walsh Ave., Santa Clara, Calif. 95051. Phone (408) 727-1470 [375]

Development system for 8048s costs under $600

For those designers who have hesitated to use the 8048 family of single-chip microcomputers because of the high cost of development tools, an S-100 card can aid in developing and prototyping products using the 8048 at a low cost. The EPR-48 card will program the 8748 microcomputer with code from an external source or from a CP/M-compatible cross-assembler (XASM-48) that handles the 8021, 8022, 8041, and 8049.

The EPR-48 programmer card sells for $449, and the XASM-48 cross-assembler sells for $200; together, they sell for $574. Also available are read-only memory simulator boards (PSB-100) with 1-K or 8-K static random-access memories. They are priced at $395 and $565, respectively.

Avocet Systems Inc., 804 South State St., Dover, Del. 19901. [377]



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Bendix

Circle 187 on reader service card

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Synchro amp saves power

Design eliminates large transformers, synchronizes pulsating supply to signal

With few parts, high efficiencies, and built-in power supplies, ILC Data Device Corp.'s SBA series of synchro booster amplifiers offers 25-VA synchro outputs for direct drive of 90-V motors. Used in conjunction with digital-to-synchro or digital-to-resolver converters, or simply to boost synchro signals, the SBA units come in 60- and 400-Hz versions, each requiring either a 90-V synchro or 6.81-V resolver input.

Unlike previous converter modules that contained all the amplification circuitry needed to work in a system, today's hybrid circuits need an external amplifier, according to Seymour Lanton, research and development manager for synchro conversion products. "The modular synchro converters used power amplifiers that ran on external 15-V power supplies," he notes. "That meant the output transformer worked with amplified inputs and had to maintain high accuracies. Therefore, the transformers had to be very large."

Pulsating. Lanton has reversed that circuit design in the SBA series by putting small, isolating Scott-T transformers before the triple power amplifiers, thus eliminating the need for large transformers and significantly lowering the power required by the unit. The internal pulsating power supply, which produces two unfiltered, full-wave rectified positive and negative voltages synchronized so that they are in phase with the amplifier output voltage, also increases efficiency. Because the supply "follows the maximum envelope of the amplifier," notes Lanton, power dissipation is approximately halved for reactive loads.

The units have an accuracy of ± 3 minutes of arc for passive loads and ± 10 minutes for active loads, such as torque receivers. They also have current limiting to prevent damage from overloading and short circuits. A thermal cutout disables the output at 125°C. An automatic kick circuit shifts the synchro output by 120° for 0.5 s to free the rotor in a torque receiver if it is stuck.

Applicable wherever direct high-power synchro drive is required, the SBA units will find use in training simulators, remote indicators, gunfire control, and Navy retransmission systems. Digital outputs from the units can be monitored by a remote computer.

The 90-V synchro input model will sell for $850 in single quantities, and the 6.81-V resolver input model for $915. Delivery is within six weeks.

ILC Data Device Corp., 105 Wilbur Place, Bohemia, N. Y. 11716. Phone Hans Schloss at (516) 567-5600 [381]

3-by-6-by-4-in. programmable controller may be smallest

A miniature programmable controller, measuring approximately 3 by 6 by 4 in., is believed by its manufacturer to be the world's smallest industrial-process controller. The Sysmac-MO has been designed to handle fewer than 50 input/output functions, meeting the requirements for smaller system control applications. It has a keyboard for entering programs, a display, and a programmable-read-only-memory loader. Either logic or ladder-diagram programming instructions can be entered over the 23-button keyboard. A user's program can be stored in either random-access memory or ultraviolet-light-erasable PROM.

The Sysmac-MO contains shift registers, 48 counters, 16 timers, and 48 temporary storage points. Functional modules can be added to increase its flexibility. One version uses a 256-word RAM or 1,024-word E-PROM with programmer and downloader; another uses only a RAM with the program keyboard; a third is an E-PROM controller without the programmer.

The three versions range in price from $350 to $1,200, depending on type and number of extra modules requested.

Omron Electronics Inc., 650 Woodfield, Schaumburg, Ill. 60195. Phone (312) 843-7900 [403]

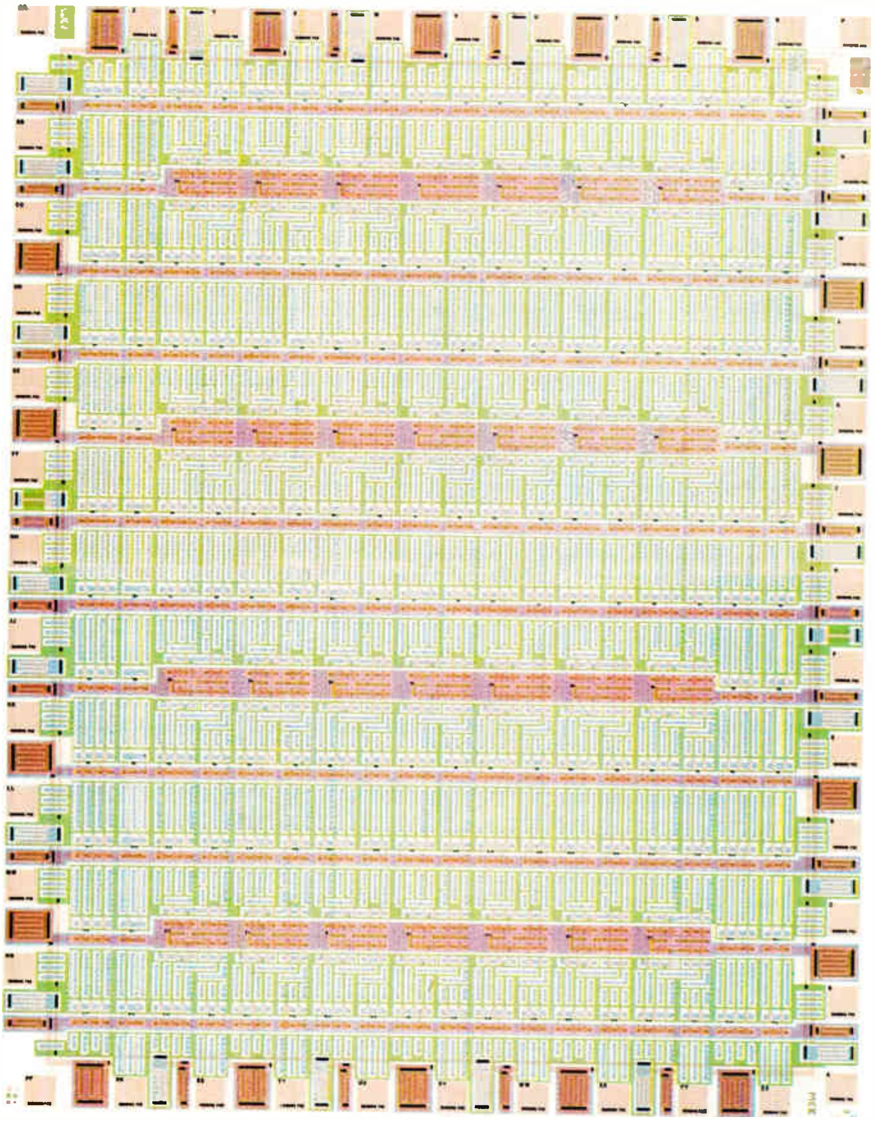
$2,255 system monitors machine performance

Priced at $2,255, the TRAC (for time, rate, and count) System is a microprocessor-based instrument that monitors and reports production activity and downtime in the manufacturing, processing, and packaging industries. The unit continuously updates 13 production statistics and 10 downtime categories, displaying them digitally or printing a permanent record.

The front panel of the instrument has on it the digital display, light-emitting-diode status indicators, a keypad, and function-selection as well as control switches. Since the instrument contains two independent counters, it can count both good and rejected parts, or machine cycles and units produced, or inputs and outputs. Counts may be displayed unaltered or can be scaled to permit accumulation in units of measure. For example, shaft rotations can be linearized. An internal battery powers the unit's memory and prevents loss of data when power is interrupted. The TRAC monitor has a standard RS-232-C serial interface port. The standard model can be delivered in 30 days.

Xytec Corp., 8104 S. W. Nimbus, Beaverton, Ore. 97005. Phone (503) 644-3633 [404]

For maximum cost-efficiency, design with the new MCE CMOS Monochip.™



MCE Monochip™ is the most cost-effective member of our CMOS digital gate array family. It's the same size as our MCC Monochip (23,500 square mils), but has 28 flip flops more—giving you the equivalent of 444 gates and boosting silicon usage efficiency by 37%. That means greater cost savings for you.

MCE Monochip™ is ideal for applications such as counters or dividers, data latches, or shift registers where numerous flip flops are required. Plus MCE Monochip has many new features to make chip layouts simpler for you, including 22 buffers and 18 drivers evenly distributed on the chip's periphery, internal contacts for easier accommodation of bus structures, and underpasses for easy access to the four corner bonding pads.

Start designing your own MCE gate array today. Our CMOS Design Manual gives you all the materials and information you need for just $25.

Because MCE Monochip's components are already in place, all you do is tell us how to connect them for the circuit you need. Working from your layout, we make your circuit and deliver 20 prototypes in 12 to 14 weeks for $4,650. Once you've approved them, we'll produce 1,000 to 500,000 parts for you.

Start saving money on your designs today—with the MCE Monochip. To order your kit—or for more information—call or write us. Interdesign, 1255 Reamwood Avenue, Sunnyvale, CA 94086. (408) 734-8666.

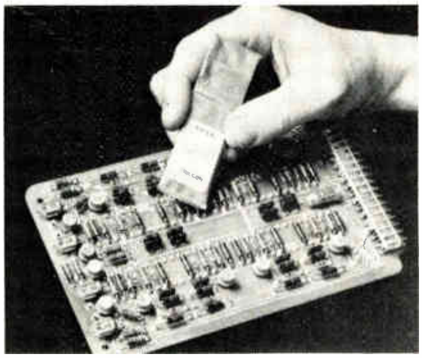
Description	Specification at 25°C (5 volts)
444 equivalent gates	3 to 5 volts supply
28 dedicated D-type flip flops arranged in 4 rows of 7 each	Average propagation delay of 13ns (FO = 2)
160 array cells arranged in 8 rows of 18 each and 4 rows of 4 each	Toggle frequency up to 5 megahertz
40 I/O/cells, 22 of which can be connected as three-state outputs	Storage temperature range: -55 to +150°C
136 x 174 mils	Operating temperature range: -55 to +125°C
44 pins max.	Proven metal gate CMOS technology

Interdesign

Monochip:™ the semi-custom IC.

Interdesign is a Ferranti Company.

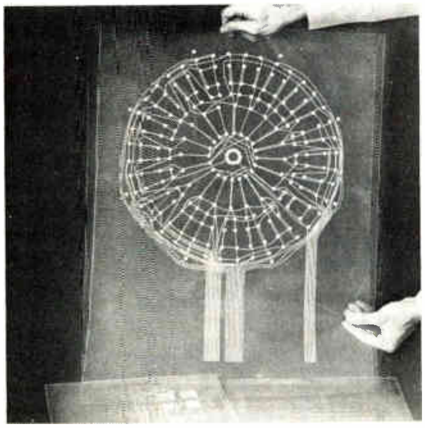
An electrically conductive adhesive, TRA-DUCT 2902 is designed for electronic bonding and sealing applications. It is a smooth paste of refined pure silver epoxy, free of solvents and copper or carbon additives. It can bond and coat dissimilar materials such as metals, ceramics, glass, and plastic laminates. TRA-DUCT 2902 cures at room temperature and can be used as a cold solder for heat-sensitive components and for the assembly and repair of electrical modules, printed circuits, waveguides, flat cables, and high-frequency shields.



The adhesive is available for immediate shipment from stock in predispensed Bipax packages. The Bipax package makes the epoxy easier to mix, convenient to store, and safe to use.

TRA-CON Inc., 55 North St., Medford, Mass. 02155. Phone (617) 391-5550 [476]

A polymer thick-film paste is designed to withstand the bending and flexure forces encountered in membrane switches and keyboards. Type G29B, part of a line of PTF conductive, resistive, and crossover insulation pastes, offers considerable cost savings on dense silk-screened membrane keyboards used in many consumer, commercial, and industrial electronic devices, according to the manufacturer.



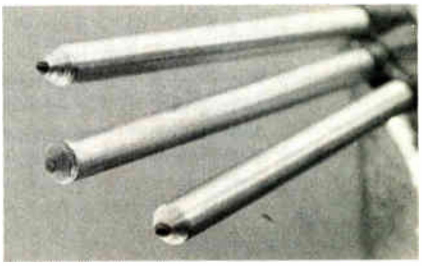
Methode Development Company, 7447 West Wilson Ave., Chicago, Ill. 60656. Phone (312) 867-9600 [477]

An engineering polymer, Mindel B-322 is designed for electrical connector applications and has properties such as high dielectric strength, arc resistance, and low loss factor. Made of polybutylene terephthalate and nylon, Mindel B-322 resists warping due to its amorphousness, can be molded to precise dimensions, and will hold its shape within close tolerances. The Mindel B series is characterized by high heat-distortion temperatures, excellent chemical resistance, high stiffness, ease of fabrication, and reinforcement with glass or mineral fillers.

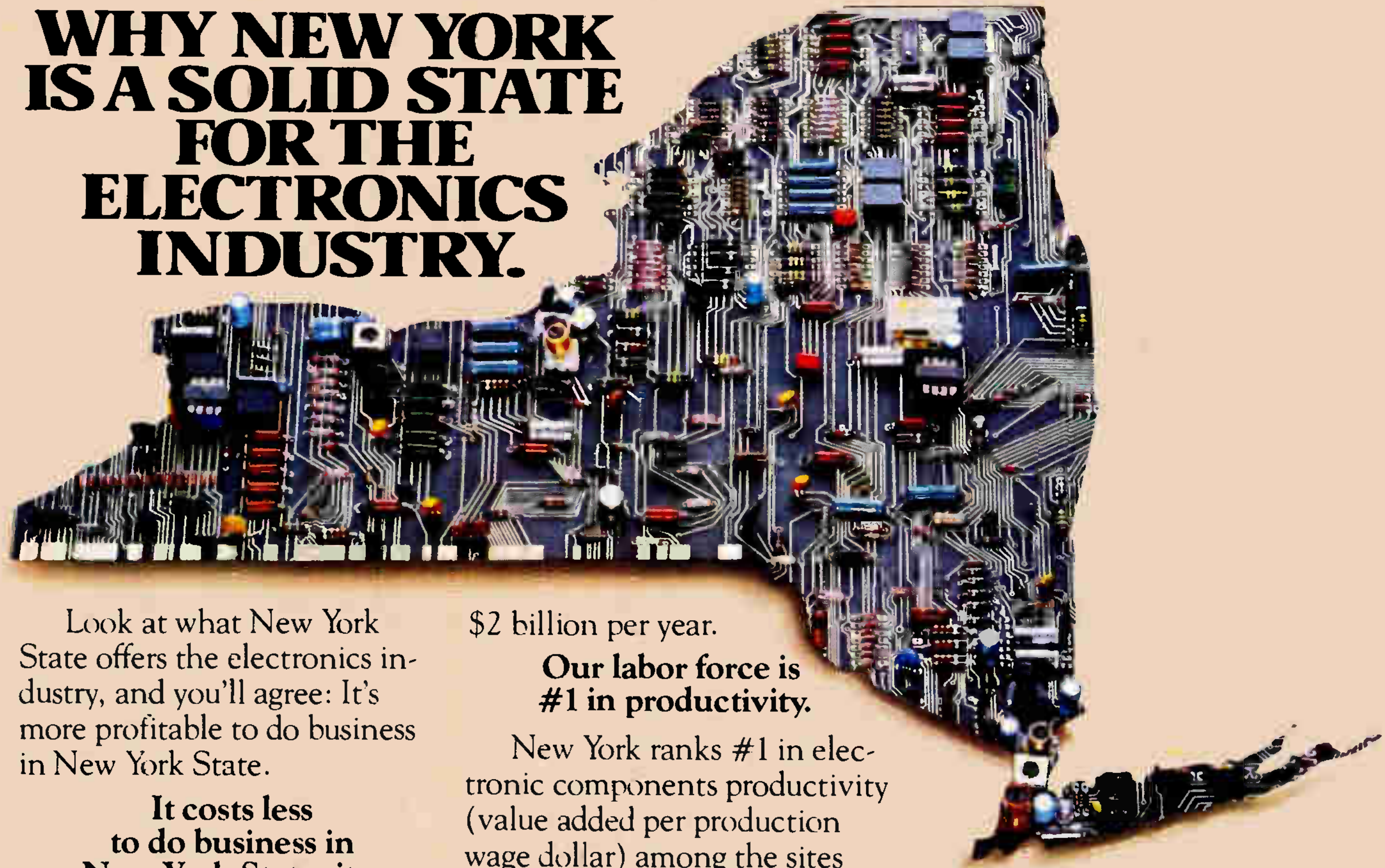
Union Carbide Corp., Old Ridgebury Road, Danbury, Conn. 06817 [478]

An alumina-based castable ceramic seals and insulates high-temperature devices such as thermocouple probes, connectors, and feedthroughs. Ceramacast 505 comes in a powder form that, when mixed with water, forms a slurry that is then poured into the device being insulated. It will cure at 200°F after setting for a few hours and can be used at up to 3,200°F. The material has a dielectric strength of 50 V/mil, a volume resistivity of 10^9 Ω-cm, and a dielectric constant of 4.0. It is available from stock at $35.00 per quart and $60.00 per gallon. In large quantities, it sells for $30.00 per gallon.

Aremco Products Inc., P. O. Box 429, Ossining, N. Y. 10562 [479]



WHY NEW YORK IS A SOLID STATE FOR THE ELECTRONICS INDUSTRY.



Look at what New York State offers the electronics industry, and you'll agree: It's more profitable to do business in New York State.

It costs less to do business in New York State sites than in San Jose, California. And we can prove it.

An independent study analyzed the four critical costs of taxes, wages, power and construction for a model new electronics firm. It showed that New York State offers sites where these costs are less than they are for choice electronics industry sites around the country.

For example, these costs would total $7.6 million annually in San Jose, versus only $6.4 million in, say, Brookhaven, New York.

New York has the best business advantages in America.

Our costs are lower because we have the best tax incentives and credits. We have on-the-job training and job incentive programs. Long-term, low-cost financing. And, we've cut personal and business taxes by $2 billion per year.

Our labor force is #1 in productivity.

New York ranks #1 in electronic components productivity (value added per production wage dollar) among the sites analyzed. And in the past five years, New York's number of idle man-days due to work stoppages was half that of the national average.

We graduate more electronics engineers than any other state.

Thanks to universities like RPI and Cornell—and dozens of other fine colleges—more electronics engineers are graduated each year in New York State than any other state including California or Massachusetts. And since many of the largest electronics firms are already doing business here—GE, IBM, to name only a couple—our graduates are quickly turned into seasoned professionals.

When you look into New York, you'll love New York.

We have an abundance of electric power. Lots of affordable housing for your employees. And our 30 million acres include thousands of available plant sites. Not to mention some of the most magnificent outdoors and year-round recreation on the American continent.

Tell me more about why New York is a solid state for business. I am particularly interested in information on:

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Computers & peripherals

Unit prints CRT dumps rapidly

$1,195 matrix printer makes hard copy of video graphics at 32 720-dot rows/s

Original-equipment manufacturers offering the ability to transpose high-quality graphics rapidly from cathode-ray-tube terminals to paper have had difficulty doing so at a low cost. But with a new graphics printer from Computer Printers International, OEMs will be able to offer rapid dumps from dumb CRT terminals and high print quality at a reasonable price.

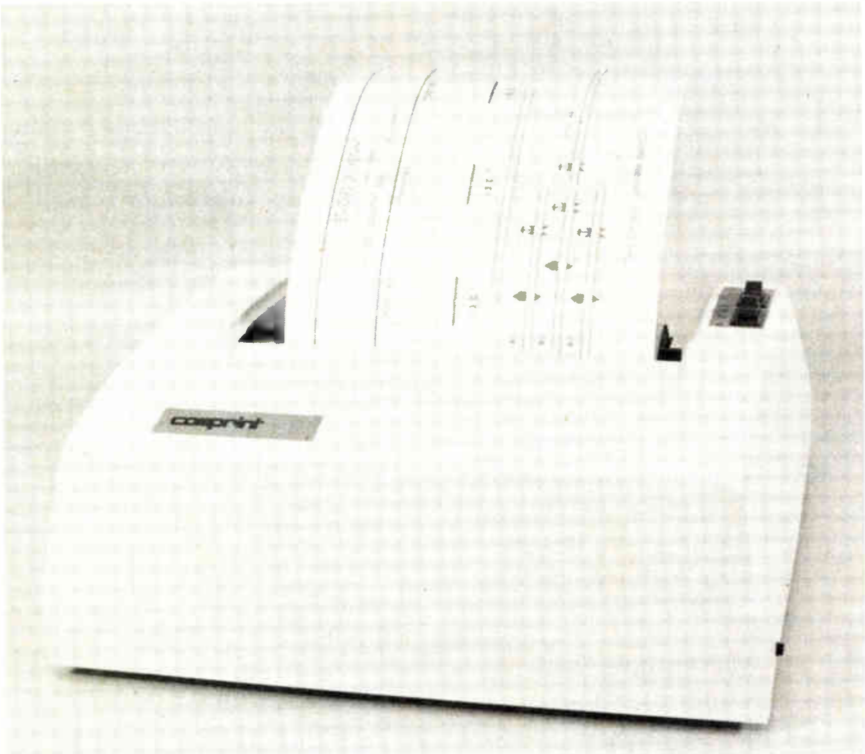
The 912-GO electrosensitive matrix printer prints at a speed of 0.32 in./s vertically. Producing 720 dots per row and 32 rows per second, the unit has a positional accuracy of ±0.25 dots at a 100-dot/in. resolution. "We believe that the price-performance characteristics of the 912-GO are such that it is less than half the cost of alternative devices having comparable speed and print quality," says Comprint president Michael J. Long. In fact, the printer's single-unit price of $1,195 and its compactness should make it attractive for integrating into a system. The stand-alone 912-GO weighs 15 lb and measures 5.75 by 15.23 by 13.5 in.

The printer comes with a standard parallel port, but the company is offering as options RS-232 serial and Centronics parallel interfaces. Graphics sent from the CRT must be in a binary vertical format since the unit prints vertically. Although the printing time to dump an entire CRT image "is generally a function of the speed with which data is provided by the host device," says Long, the time "can be as short as 10 seconds or so."

The 912-GO prints on aluminum-coated electrosensitive paper 8½ in. wide. It operates from a line voltage of 120 V ac (−5%, +10%), but a 220-V version is also available. It consumes a maximum of 55 W while printing and 10 W on standby.

Large-quantity discounts are available, and the printers can be delivered in one to four weeks, depending on the quantity ordered.

Computer Printers International Inc., 340 E. Middlefield Rd., Mountain View, Calif. 94043. Phone (415) 969-6161 [361]



Interactive color graphics system costs $17,500

For those users who have not been able to justify the cost of sophisticated computer-aided design and manufacturing systems, the Whizzard 6250 interactive graphics terminal from Megatek includes dynamic line-drawing capability for only $17,500.

The system consists of a 13-in. color raster monitor packaged with a keyboard and joystick control in a desktop cabinet. Its 14-slot chassis includes boards for a graphics processor, 64-K bytes of vector memory, and an RS-232-C serial asynchronous interface. Optional modules include additional vector memory (to 128-K bytes), a hard-copy output interface, and a data-tablet input interface.

Because the size and expandability of the 6250 have been intentionally limited to keep costs low, the unit resolves only eight colors, has no color look-up table, and cannot be expanded to use hardware modules for clip, rotate, or scale transformations.

The 6250 has an average picture-element writing time of 160 ns and can update and manipulate complex pictures 20 to 30 times per second. A long-persistence phosphor virtually eliminates screen flicker, says the manufacturer. The entire 4,096-by-4,096-pixel area can be displayed on the screen. A smaller view-port can zoom areas down to 512 by 512 pixels, with true scaling rather than pixel replication. Real-time data can be displayed simultaneously with static overlays.

Communications traffic with the host computer can be reduced when the 6250 uses its powerful bit-slice-architecture microprocessor in conjunction with an optional Wand

6200 software package. Wand 6200 is written entirely in Fortran, so all programs written for larger Megatek systems, including both vector refresh and color raster types, can be run on the new graphics terminal. Deliveries of the 6250 are scheduled to begin next month.

Megatek Corp., 3931 Sorrento Valley Blvd., San Diego, Calif. 92121 [363]

Floppy-disk drive uses linear stepper motor

Fully compatible with Shugart's 851R 8-in. floppy-disk drive, Decitek's 8302S drive uses a linear stepper motor, reducing the number of parts in the drive mechanism and positioner by 37%. A lower component count results in greater reliability, quieter operation, and a slightly lower price, according to Dennis Brown, sales manager for disk products at Decitek.

The linear stepper motor eliminates rotary-to-linear motion conversion and increases the specified mean time between failures from 8,000 to 12,000 h. The positioner mechanism may be replaced by removing a single screw, making field service easy. In 100-unit lots, the drives are $670 each.

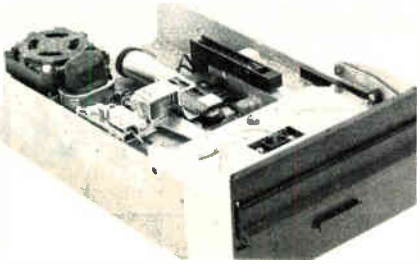
Built around an Intel 8035 microcomputer, the drive has a data-transfer rate of 250 kb/s (unformatted) and an average access time of 254 ms. The unformatted single-density version has a capacity of 0.8 megabyte and the formatted single-density unit 0.5 megabyte, with a recording density of 3,268 b/in. on the inside track and 1,836 b/in. on the outside track. An unformatted double-density version of the drive stores 1.6 megabytes. Head loading time is 35 ms; the diskette turns at 360 rpm ± 2%.

The 8035 can perform on-board diagnostics that completely exercise the drive's positioner mechanism. If a fault is found, a front-panel light-emitting diode so indicates. If there is a power failure, the microprocessor prevents the head from writing erroneous data.

Circle 194 on reader service card

Circle 222 on reader service card

New products



The 8302S comes with a one-year warranty on parts, 90 days on labor. The company can schedule immediate delivery of small orders.

Decitek Corp., 129 Flanders Rd., Westboro, Mass. 01581. Phone Dennis Brown at (617) 366-8334 [364]

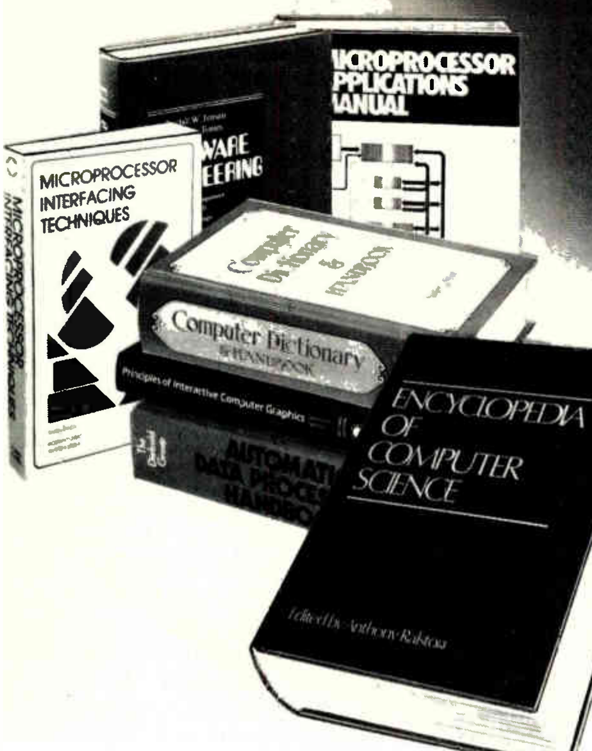
TI adds three computers to DS990 minicomputer family

Texas Instruments, expanding its line of DS990 minicomputers, has added two mid-range computer systems and a high-end system.

The model 7 uses TI's 990/10 minicomputer and a new cartridge-and-fixed-disk system mounted on a pedestal. The disk combination offers a total capacity of 32 megabytes of mass storage: 16 megabytes in fixed disk and 16 megabytes in removable cartridge disk. The model 9 uses the same minicomputer and another version of the new disk system that offers 80 megabytes in fixed disk and 16 megabytes in removable media for a total of 96 megabytes. The largest of the new systems, the model 29, uses TI's 990/12 minicomputer with cache memory. Mass storage is provided by the same cartridge-disk system used in the model 9. All three models provide space for expansion options.

The models 7 and 9 with disk controller, 128-K bytes of memory, and video display terminal sell for $39,150 and $46,150, respectively. The model 29 with controller, 256-K bytes of memory, and two displays is priced at $67,500. Deliveries are scheduled for May.

Texas Instruments Inc., Digital Systems Group, P. O. Box 1444, Houston, Texas 77001 [365]



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AUTOMATIC DATA PROCESSING HANDBOOK Edited by The Diebold Group, Inc
168/075 Pub. Pr., $44.95 Club Pr., $31.50

PROGRAMMING LANGUAGES BY A B Tucker, Jr.
654/158 Pub. Pr., $23.95 Club Pr., $16.95

MICROPROCESSOR APPLICATIONS MANUAL By Motorola, Inc.
435/278 Pub. Pr., $42.50 Club Pr., $29.50

DATA BASE DESIGN By G Wiederhold
701/30X Pub. Pr., $25 95 Club Pr., $19.95

PRINCIPLES OF INTERACTIVE COMPUTER GRAPHICS, 2nd Ed. By W M Newman & R. F Sproull
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P39494

New literature

Global estimates. Global estimates of West European markets for electronics equipment and components are discussed in the 1981 edition of the annual Mackintosh Electronics Yearbook. This book tallies 1980 markets for equipment and components at $92 billion. Last year's book forecast markets at $64 billion. Mackintosh postulates that this growth will push West European markets to $103 billion this year—$84 billion for equipment and $19 billion for components—and that these markets will soar over the next four years to top $140 billion in 1984. The 184-page volume contains chapters on economic prospects for the year in the United States, Japan, and Western Europe and production data for electronics and for production in end-user industries like automobiles. A list of statistical sources and the exchange rates used for conversion to dollars are explained in 30 pages. The yearbook, which sells for $325, can be obtained from Mackintosh Publications Ltd., Mackintosh House, Napier Rd., Luton LU1 1RG, England. Circle reader service number 421.

Capacitors. A 32-page catalog discusses a complete array of capacitors, including miniature, monolithic, low-voltage subminiature, bypass, temperature-compensating, temperature-stable, frequency-stable, high- and low-voltage, unleaded, and Underwriters Laboratories-recognized types. Complete specifications with line drawings and dimensions are given in decimal and metric equivalents, including sizes, ratings, tolerances, and temperature-characteristic curves. A ceramic-capacitor applications guide gives a breakdown of those available. To receive a copy of the catalog, write to RMC-Radio Materials Corp., 4242 West Bryn Mawr Ave., Chicago, Ill. 60646. [422]

Integrated circuits. An 884-page catalog describes 86 integrated-circuit families. The catalog includes 174 pages of application information and data for Precision Monolithics' line of operational amplifiers, buffers (voltage followers), comparators, matched transistors, multiplexers and analog switches, and sample-and-hold amplifiers. A cross-reference guide lists competitive IC manufacturers and shows either a direct pin-for-pin PMI chip replacement or the firm's nearest functional equivalent. There is also a chapter on linear IC terminology, a description of IC manufacturing and testing procedures, and a supplementary section on packaging. A copy of the catalog can be obtained by writing to Product Literature Department, Precision Monolithics Inc., 1500 Space Park Dr., Santa Clara, Calif. 95050. [423]

Test instruments. "Test Instruments for Industry" covers test instruments for engineering, production line, and other industrial applications. Catalog BK-181 provides a product specification section, applications information, and key features on each test instrument. New products such as a 100-MHz quadruple-trace scope; a portable dual-trace miniscope; an autoranging microcomputer-controlled digital multimeter; autoranging capacitance meters; a benchtop DMM; and new 30-MHz scopes are featured. Additional instruments covered are frequency counters, analog multimeters, function and radio-frequency-signal generators, digital and pulser probes, semiconductor testers, power supplies, and instrument probes. B&K-Precision, Dynascan Corp., 6460 W. Cortland St., Chicago, Ill. 60635. Phone (800) 621-4627 [424]

Products Newsletter

TI's 9995 16-bit one-chip computer is ready

Although the ink is not yet dry on the announcement that a version of the first single-chip 16-bit microcomputer—the TMS 9940—**can address up to 64-K bytes of off-chip memory** [*Electronics*, Dec. 18, p. 91], Texas Instruments Inc., Houston, says that samples of the new microcomputer, the TMS 9995, are ready to go and that production quantities of the device will be ready for shipment in the spring. Although the chip will be available in other packages, prices are available so far only for the plastic-packaged version, the 9995NL, which will cost $40 apiece in 100-unit quantities. An evaluation board sells for $800.

Boschert's 200-W open-frame switcher gets Europe's nod

Almost as if to mark its recent acquisition by Britain's electrical equipment builder BICC Ltd. [*Electronics*, Jan. 13, p. 34], Boschert Inc. of Sunnyvale, Calif., has become **the first American manufacturer of open-frame switching power supplies to gain approval under the stringent safety specifications** (VDE0730) required by West Germany's Verband Deutscher Elektroniker. Once mandatory only in that country, compliance with VDE specs is rapidly becoming necessary throughout the European Economic Community and is influencing the designs of most large U. S. systems manufacturers. Boschert's XL200-3501 200-W unit is the first U. S.-made, "Europe-oriented" general-purpose switching supply for medium-power data- and word-processing systems.

S-100 card offers serial, parallel I/O, vectored interrupts

Computer systems using the S-100 bus move a step closer to the minicomputer competition with the introduction of a **multifunction input/output board** by Digicomp Research Inc., Ithaca, N. Y. The MIFO follows hard on the heels of Digicomp's own 8- and 16-bit S-100–based dual-processor system, said to be the first central-processing-unit board set to combine a Z80 and Western Digital's Pascal Microengine [*Electronics*, Jan. 13, p. 290]. It combines, on a single board, almost all the features needed to control a multiuser computer system: four RS-232-C serial I/O ports with independent transfer rates as high as 19,200 b/s, a 24-bit-wide parallel I/O system configurable into up to four independent ports of varying widths, five independent multifunction timer-counters, 16 levels of vectored interrupt control, and an optional battery-powered real-time clock and calendar that includes 50 bytes of MOS random-access memory.

Price changes

■ **Memorex Corp., Santa Clara, Calif.,** has increased the prices of its end-user disk and tape subsystems 7% to 10%. Lease and rental prices on the disk subsystems have been raised by 7% but remain unchanged for the tape subsystems, though the latter's maintenance prices will go up 10% in April. Hourly service rates were also raised by 10% for all products of the Storage Systems group.

■ **Spectronics Inc., a division of Honeywell Inc. in Dallas,** has chopped about 30% off the price of its new SD 5600 and SDP 8600 Opto Schmitt component line. The Schmitt-triggered optodetectors are now $1.77 apiece (SDP 8600) and $2.67 each (SD 5600) for 1,000 units.

■ **Okidata Corp., Mount Laurel, N. J.,** has rolled back prices on two of its serial matrix printers. The Microline 80 goes from $800 to $600 retail and from $455 to $356 in 500-unit quantities. The retail price of the 82 was cut from $960 to $799 and the price for original-equipment manufacturers dropped to $499 from $540.

Career outlook

Wanted: communications EEs

■ Electrical engineering schools have been turning out graduates for whom such basics of analog technology as microwave theory, circuit design, and hands-on maintenance skills are lost arts. With so much emphasis currently placed on digital technology and the application of microprocessors, these traditional aspects of electronics are now all but untaught except in an occasional elective course. Yet these disciplines figure heavily in the design of billions of dollars' worth of communications gear produced each year.

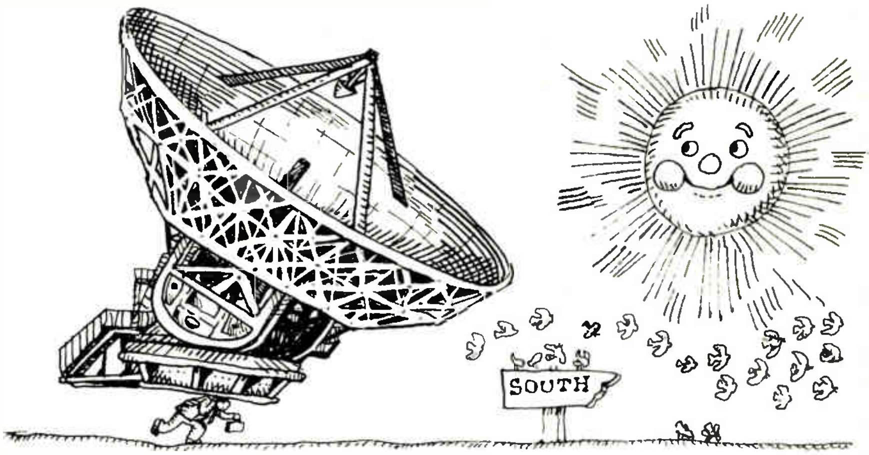
This situation has made it difficult for the communications industry to obtain the people it needs to design equipment for telecommunications networks. In fact, the need is so great, says the "Twelfth Annual Telecommunications Salary Survey," that employment in this area was less affected by the 1980 recession than any of the recessions that have hit the U.S. in recent years. Personnel Resources International Inc. of New York, the telecommunications specialty placement firm that published the survey, also reports that the demand for skilled people is expected to continue and salaries will grow accordingly.

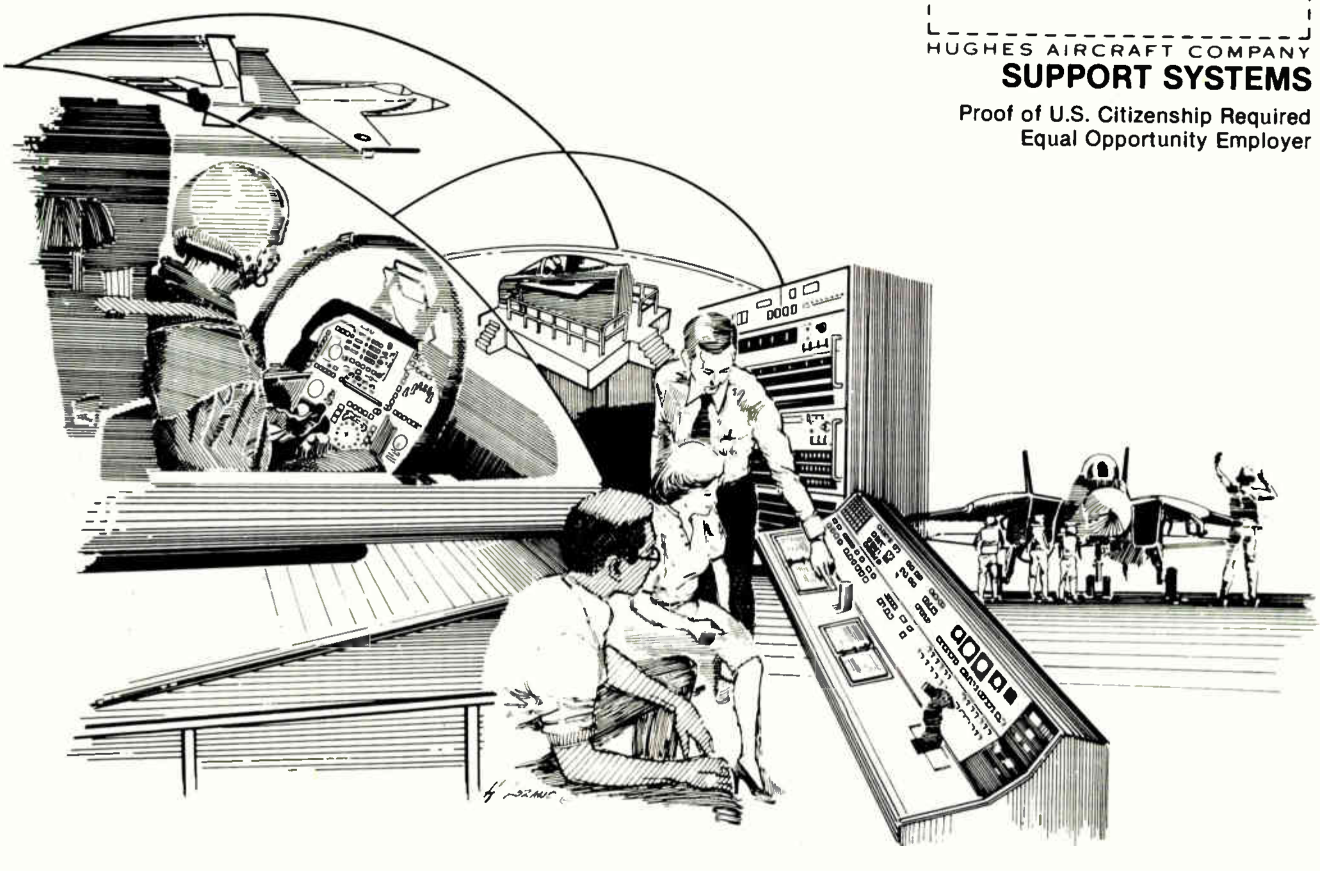
"Some needed personnel are almost impossible to find," observes company president Jay Jacobson. These include circuit and hardware designers and switching software engineers. If they are engineering managers, such people can expect to earn $34,000 to $37,000 per year. In fact, the demand is so great that, according to the U.S. Bureau of Labor Statistics, telecommunications engineers with little or no experience can earn $19,000.

Southern opportunities. To earn a salary at the high end of these figures, Personnel Resources recommends a simple strategy—go south. Telecommunications employment increased most rapidly in the South, especially in Texas. Another hot spot is Washington, D.C., where many large firms are headquartered or have established offices to keep abreast of the constant developments in telecommunications regulations.

Regardless of the location, however, the skills in demand still vary with the company specialty. Telecommunications interconnection firms, for example, need project engineers and field coordinators experienced with electronic switching systems. Transmission equipment manufacturers seek design engineers with backgrounds in mobile radio, fiber optics, and modulation techniques. But if the candidate is a product planner who can design systems that have marketing potential, he can practically write his own ticket.

Anyone aiming for a slot in these job categories should keep in mind that the telecommunications industry is moving toward software-controlled hardware. The Institute for Electrical and Electronics Engineers has recognized this trend and formed a software group in its Communication Society to help EEs keep current with developments in telecommunications technology.—**Harvey J. Hindin**





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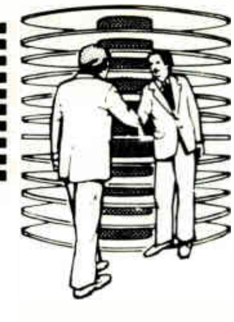

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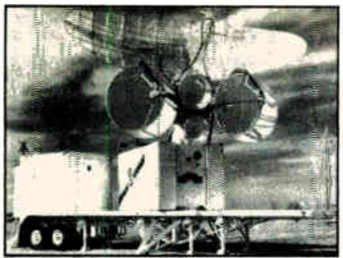
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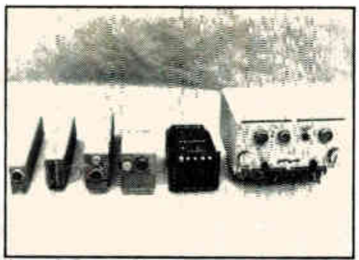
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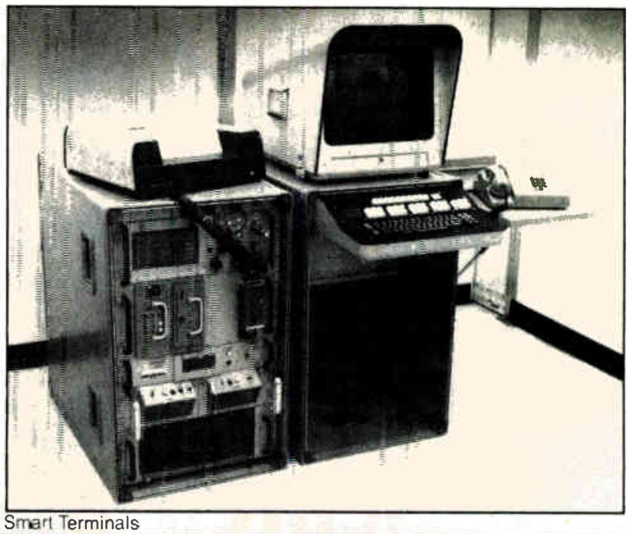
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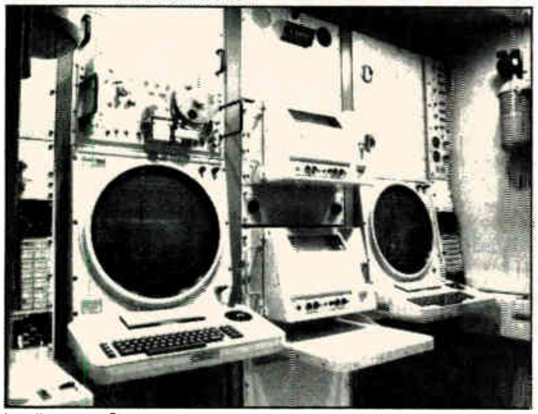
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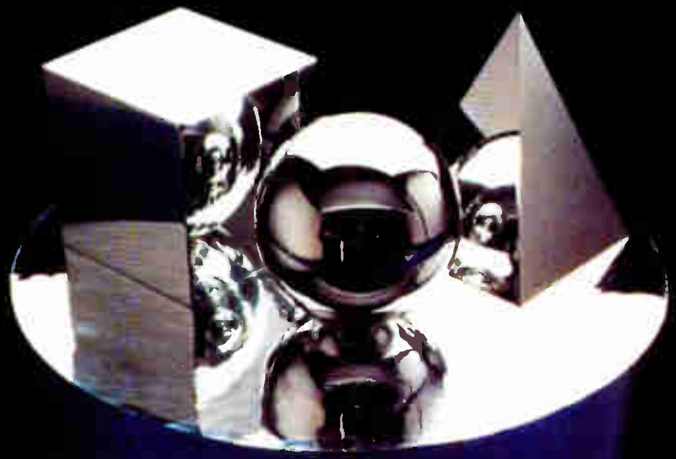

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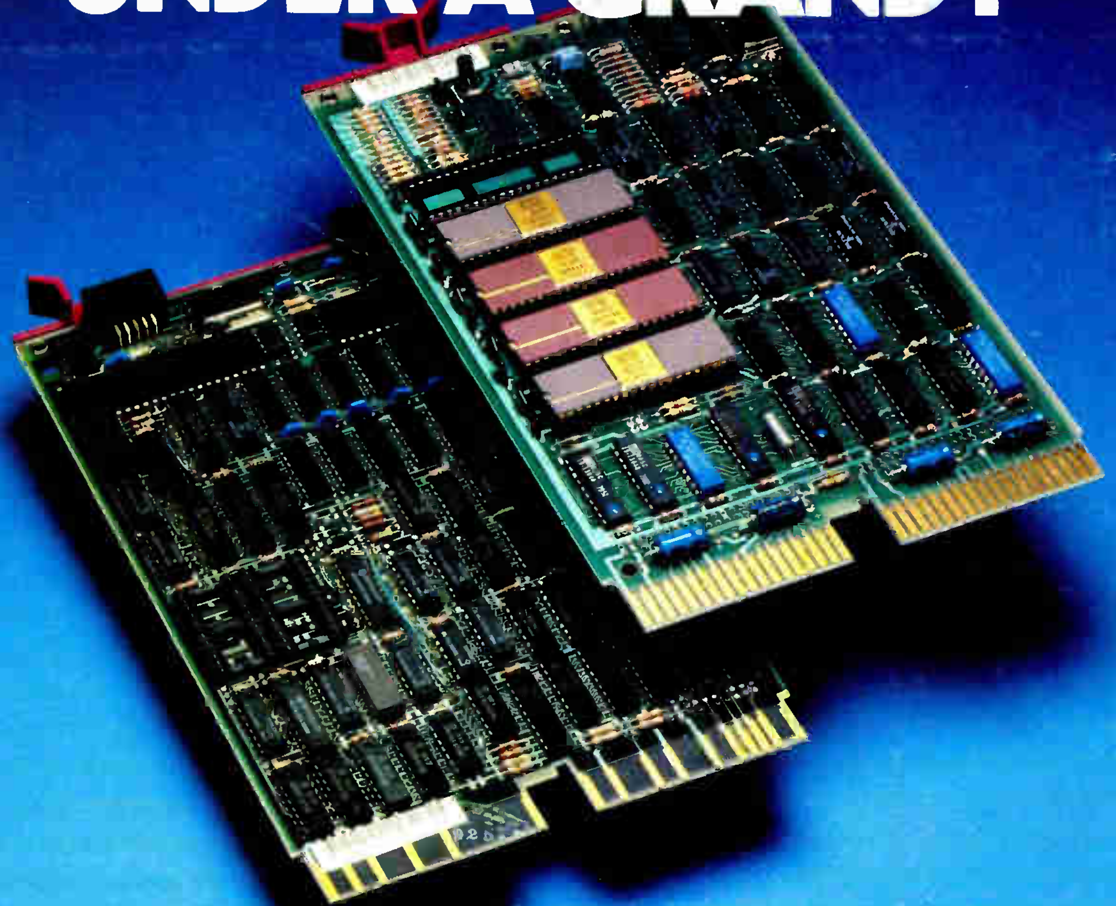

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