AUGUST 2, 1979

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Electronics
The International Magazine of Electronics Technology
Vol. 52, No. 16 • August 2, 1979

Highlights

Cover: Maturing bubbles take diverse forms, 99

The architectural options for magnetic bubble memory devices represent compromises in access speeds, voltage requirements, control-circuit complexities, and packaging. As memory makers prepare to bring out 4-megabit and larger chips, they must meet these problems head on.

Cover photograph is by Don Carroll.

Changes likely in Communications Act, 88

Rep. Lionel Van Deerlin (D., Calif.) has watered down his legislative proposals—from complete replacement of the 1934 Communications Act to less ambitious amendments. As a result, chances for enactment by this Congress have improved.

Multilayer packaging meets LSI challenge, 109

Nine chips in single 23-layer carrier mounted on cards and boards with 7 to 16 layers increase chip density of IBM mainframe computers more than 15 times.

LSI lets ECL show its speed, 120

Emitter-coupled logic is faster than TTL at the gate level, but limited density has diminished this advantage with interconnect delays. Fairchild's new 8-bit-slice mainframe parts give ECL its head.

. . . and in the next issue

A special report on peripheral integrated circuits . . . a direct-step-on-wafer reducing photolithographic technique

Electronics

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Publisher's letter

A tantalizing glimpse of the future of new bubble memory technology was provided at the recent Second Joint Intermag—Magnetism and Magnetic Materials Conference in New York (p. 44), where one technical spectacular followed another. It is a future that promises severe challenges—for example, how to organize chips designed to contain 16 million bits of memory. But even as researchers unveil their startling innovations, users in the real world are just beginning to step over the threshold of applications.

The cover article in this issue (p. 99) provides a good overview of the bubble memory devices that are now moving into the marketplace. As co-author George Reyling, manager of bubble memory subsystems for National Semiconductor Corp., Santa Clara, Calif., points out, the truly high-volume applications of bubble memories are not yet known.

"The first uses appear to be as replacements for disk storage, but this application may be a false lead," he says. "I think that, as with microprocessors, the volume sales will be for products not anticipated today."

Reyling, with seven years of experience in microprocessors, represents the user's view in National's bubble memory program. Co-author Peter George, as manager of bubble-memory design, concentrates on the physical details.

Involved in bubble-chip design since 1971, George observes, "In the next four years we will see 16-megabit bubble-memory chips using the contiguous-disk technique."

As more companies get into bubble memory design and production, growth of the market may very well be slowed by the lack of enough experienced engineers. In fact, the shortage is already apparent, the authors concede.

Once again Great Britain is turning to electronics technology to help the country compete in the international marketplace. Having begun to make itself heard in semiconductors with the formation of Inmos, the British lion is now roaring after digital telecommunications.

London bureau manager Kevin Smith's story on System X (p. 83) underscores the UK's vital interest in exporting the digital telephone system that is being installed now in its domestic exchanges. One of the interesting sidelights of the British conversion to digital technology is the change in procurement procedures dictated by the magnitude of the undertaking. Instead of competing, the equipment suppliers had to make cooperative efforts, each supplying a module for the total system.

"Competitive development programs were ruled out," Kevin reports, "a procedure that may be repeated in other European countries faced with the same problems."

To help export System X, the Post Office has formed a consortium called British Telecommunications Systems Ltd. Its first test will be how much interest System X attracts at the telecommunications exhibition in Geneva next month.

August 2, 1979 Volume 52, Number 16 100,841 copies of this issue printed

Electronics (ISSN 0013-5070) Published every other Thursday by McGraw-Hill, Inc Founder James H McGraw 1860-1948 Publication office 1221 Avenue of the Americas, N.Y., N.Y. 10020; second class postage paid at New York, N.Y. and additional mailing offices

Executive, editorial, circulation and advertising addresses Electronics, McGraw-Hill Building, 1221 Avenue of the Americas, New York, N.Y. 10020. Telephone (212) 997-1221. Teletype 12-7960 TWX 710-581-4879. Cable address. M C G R A W H I L L N E W Y O R K

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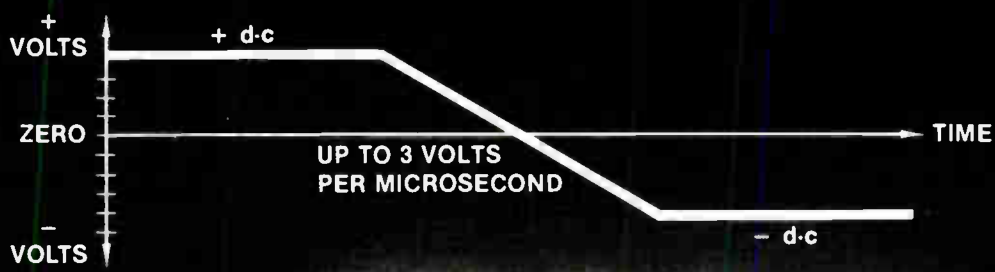

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Circle 5 on reader service card

Readers' comments

Spreading the word

To the Editor: On behalf of 6800 users, I would like to make the following widely known.

The 6800 instruction CLR (memory) performs a read memory before storing zero. This can lead—indeed has led for me—to serious debugging headaches if the memory in question is the output register of a peripheral-interface adapter and the interrupt flags of the control register are therefore inadvertently reset.

I imagine other users, too, implement special-purpose interfaces that perform separate operations on reading out of and writing into particular memory locations. CLR seems on the surface to be a useful way of generating a write into memory without disturbing the accumulators, but it becomes a trap if the "phantom" read is undesirable.

M. J. Randall
Wellington, New Zealand

More than meets the eye

To the Editor: The letter from J. W. Pehoushek in the April 26 issue on revamping plan-view displays ["Waste as savings?" p. 6] was good but not the complete story. It could be another "Big Brother strikes again," but not this time. The power savings is indeed 450 watts; however, there are about 47 PVDs per center, rather than the 20 he estimates.

First, what kills solid-state circuits more than heat? Less heat means more reliability, which means fewer parts used over time, less maintenance, and less downtime per PVD.

Second, what do you do with this extra 450 watts of heat times 47 PVDs? Remove it by air conditioning—what else?

The power savings alone of 450 watts for each PVD with a $1 million expenditure looks out of reason, but we are working with a complete system. Making it better at an overall cost savings is the end result.

Frank J. Ammel
Lenexa, Kansas

Righting the record

To the Editor: Several errors were introduced in my article "Reducing PLL's even-order harmonics" [April

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For additional information 4 For a demonstration 7

Readers' comments

12, p. 150], and I wish to point out the major ones.

In paragraph 2, it is the output of the divider and not the output of the voltage-controlled oscillator that is compared with the input frequency at the loop's phase detector. In paragraph 3, the modulation index cannot be calculated directly from the equation given, although reducing $\theta_0(s)$ does reduce the sideband noise.

In paragraph 4, the addition of capacitor C′ makes the filter a second-order type, not a third-order one. The bandwidth and damping are not, as stated in paragraph 7, filter characteristics, but loop parameters. Further, a reduction in harmonic output does not necessarily decrease the range over which the phase-locked loop will operate.

Finally, in order to make sense of the curves in (d), the following explanation is required. If a PLL frequency multiplier having a damping factor of 1.2 and a bandwidth of 100 Hz is needed, a standard second-order loop must be designed to meet the specifications. But it will be found that the loop's output contains excessive phase jitter. Therefore the loop must be redesigned with a damping factor of 2.2.

To determine N, and thus C′, we first calculate $R = \delta(\tau_1, \tau_2, \tau_3)/\delta(\tau_1, \tau_2)$. Given a required damping of 1.2 and a designed damping of 2.2, R = 0.55. From (d) then, N = 21.2. Thus $\tau_3 = \tau_2/N$ and $C' = \tau_3 R_2$.

R. P. Leck
Holmdel, N. J.

Lower

To the Editor: The article about low-voltage operational amplifiers in the May 10 issue ["C-MOS touch given micros, op amps," p. 44] says that the Intersil amplifiers can run on supplies "as low as ±0.5 volt—significantly less than the ±1-V bipolar op-amp design touted by National Semiconductor Corp." Actually, as indicated on the data sheet, the LM10 runs on ±0.6 V at 25°C and on ±0.65 V over the full military temperature range.

Robert Pease
National Semiconductor Corp.
Santa Clara, Calif.

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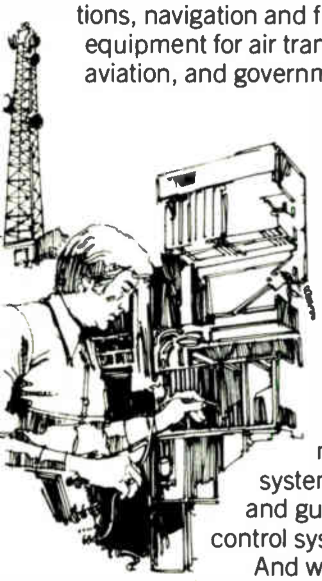

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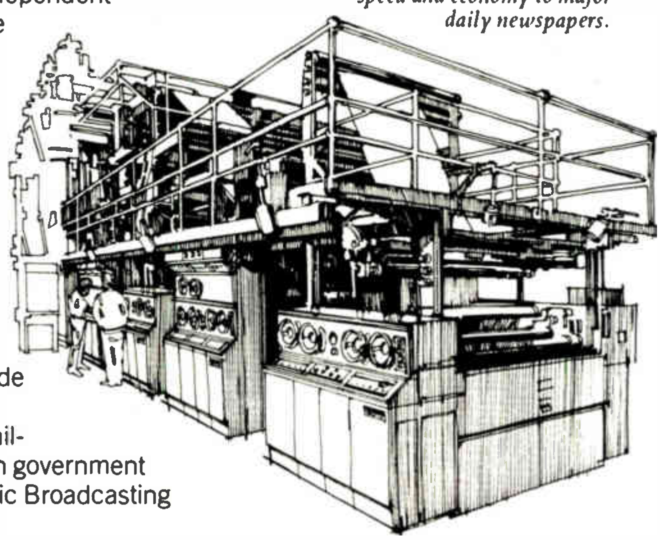

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The IEEE talks, but who listens?

Why is it that hardly anyone in Washington listens when the Institute of Electrical and Electronics Engineers addresses issues of law and economics? It is because the IEEE is widely regarded as politically naive. And that assessment, unfortunately, is a valid one.

The IEEE Committee on Telecommunications Policy demonstrated its naivete late last month when it urged the House and Senate not to tinker with the existing structure of Bell Telephone Laboratories on the grounds that it is "a major and irreplaceable national resource." It asked that American Telephone & Telegraph Co. and other telecommunications companies be exempt from antitrust laws so that they might perform "the coordination necessary to continue effective planning, technological improvement, and management of the telecommunications network."

"Adolescent rubbish" is the term used by one congressional committee staffer to characterize the IEEE presentation. Other legislative sources now immersed in the revision of the 1934 Communications Act are expressing similar judgments, albeit in softer language. "It is too hysterical to merit serious consideration," contends one Senate staffer. "I am surprised that a professional society like the IEEE is coming on like this. In one breath they say they recognize that the law needs to be changed, and in the next that they want to retain an economic status quo. What's worse, they want to turn back the clock and grant antitrust exceptions in the name of protecting 'the network'."

Certainly Bell Labs is a phenomenon of electronics technology that would be difficult to replace. But it is not irreplaceable. Nor is the Bell telephone network the "fragile and complex entity" that the IEEE's committee would have the Congress believe.

The leadership of the IEEE should move quickly to dissociate itself from the naive claims of the Committee on Telecommunications Policy. For in a national capital where hundreds of position papers on as many issues pour in daily, it is an unfortunate fact of life that the misguided views of that committee are being viewed as the position of the IEEE as a whole.

A timely idea deserving consideration

The four-day, 40-hour week is an idea whose time has come now that the seemingly perpetual gasoline shortage has moved in. That's the message from the American Electronics Association, which is trying to persuade President Carter to intervene.

Why involve the President? Well, it seems that the Walsh-Healey Public Contracts Act in effect bars Government contractors from switching to the four-day week. Actually, a section of the law mandates overtime pay for any hours over eight worked each day; AEA chairman Noel Fenton, president of Acurex Corp., Mountain View, Calif., has wired the President asking for a waiver of that clause.

While the shorter week makes marvelous good sense in lopping 20% off the amount of commuting that must be done—and President Carter has made conservation one of the cornerstones of his energy policy—it appears that the Pentagon has no intention of taking any waivers lying down. The attitude at the Department of Defense is that the AEA's suggestion is not to be taken seriously because its implementation would open a can of worms at the Pentagon—clamor for a four-day week by civilian employees.

The attitude of the military is a shame, particularly in light of the commander in chief's adjuration to use less gasoline. The AEA's request is one that deserves to be given a serious hearing.

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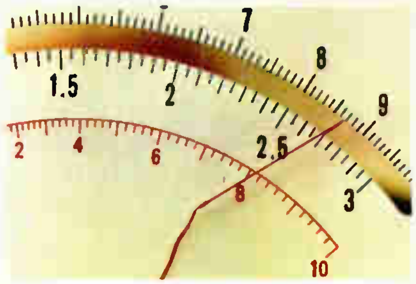

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People

Mark Shavit to direct Lambda's subsidiary in Israel

As general manager of Lambda Electronics Inc.'s new power supply development and manufacturing facility in Israel, Mark Shavit is out to make it big in Europe. "Our mandate is to meet European requirements, whether in production or engineering," he says, "and we hope to come up with original and cost-effective designs."

Currently getting to know the parent company at its headquarters in Melville, N. Y., Shavit will fly back to Israel in September, a month before opening a modest 17,000-square-foot facility in Carmiel, about a 50-minute drive northeast of Haifa. Five years or so off for the new Lambda Electronics (1979) Ltd. is growth to 100,000 ft² of space and a $20 million-to-$25 million business, mostly for export to Europe. Shavit has several reasons for believing such growth possible.

No tariffs. "We Israeli engineers have an advantage over American engineers in dealing with Europe," he explains. "We are more accustomed to meeting the diversity of requirements among the countries there. We have been fighting to get a foothold in this market for years." Another plus is that his exports from Israel, an associate member of the Common Market, will be admitted to Europe tariff-free.

Shavit's youthful look belies both his 50 years and his extensive experience, which he gained in the U. S. as well as Israel, his birthplace. His bachelor's and master's degrees in electrical engineering came from the Massachusetts Institute of Technology, Cambridge, Mass. In 1961, at age 32, he was one of the founders of Signetics Corp.—as he points out, the first company to specialize in integrated circuits. (He was known then as Mark Weissenstern, a name he changed to Shavit upon returning to Israel in 1965.) For the last eight years he has worked at the level of managing director and vice president for subsidiaries of American electronics firms making minicomputers and test and measurement equipment in Israel.

Home grown. Shavit is high on Lambda's manufacturing capabilities, and its ability to respond quickly to market needs. Perhaps even more important, he is confident about the quality of the engineering and manufacturing team that he will draw from Israel's engineering community. "My country's experience in power supply techniques comes primarily from military electronics activity—you can be sure it's very highly developed here," he says in his slightly accented English. "We have had to meet very Draconian specs with respect to heat dissipation and environmental requirements."

But will he be able to apply this to the standard off-the-shelf products that are Lambda's forte? "We will use our brains," he says quietly. "The combination of our smarts and Lambda's marketing and manufacturing system should do very well."

Zilog's systems approach will be broadened by Sweet

Zilog Inc.'s new director of marketing, Bill Sweet, is deliberately biased. He and the team he has put together are out to bring a heavier systems orientation to what he regards as the largely component-biased view of the microprocessor and microcomputer maker based in Cupertino, Calif.

Sweet feels that a better balance between systems and components is necessary. "As the microprocessor market matures, things like software and documentation are what influence the sale," he says. Hardware, readily available, will become less of a factor. In Sweet's view the customer will soon be saying, "Don't tell me about your hardware. You have to tell me about your Fortran, your Cobol compiler."

The 36-year-old Sweet comes by his systems orientation from close to 12 years in sales and marketing positions. He was marketing director for National's microcomputer systems operations for two years and held

The RAM with the non-volatile memory.

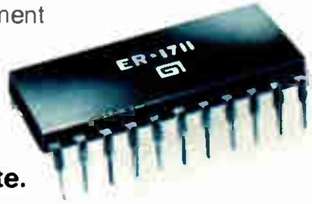
GI offers the advantages of RAM and EAROM in a single chip.

Now there's a RAM that retains its data in a power-down situation without the need for a backup battery. The mating of a RAM with an EAROM in a single low-cost chip — the ER1711 — has created a whole new world of design possibilities.

In normal operation, the ER1711 is a 256 x 4-bit static RAM with a fast 900ns read or write time. At power on/power off/power fail occurrences, single pulse programming controls the data flow to and from the RAM and EAROM cells. Data can be stored and recalled in the EAROM cells up to 10^4 times.

With fast read and write times coupled with a non-volatile memory, the ER1711 opens new application options. Examples: business machines and instruments where constantly changing data must be retained in a power off status; and any microprocessor based system where a portion of the memory must be retained to insure its operating functions.

If you have specific application questions, or would like complete specifications on the ER1711 RAM/EAROM write or call General Instrument Microelectronics, 600 West John Street, Hicksville, N.Y. 11802, 516-733-3192.



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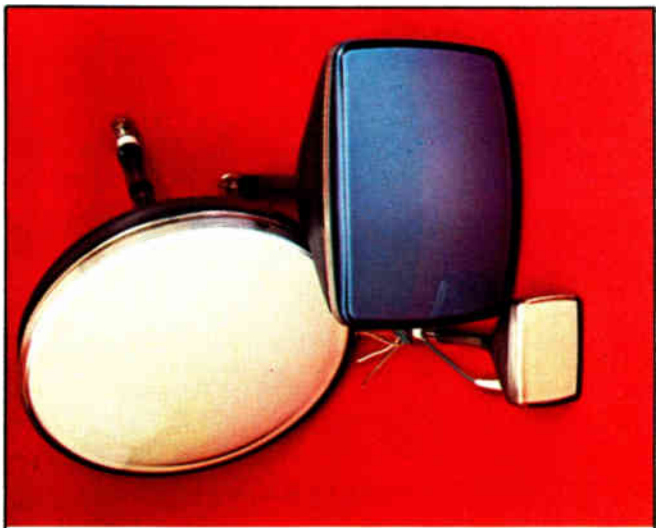
MICROELECTRONICS



People

Systematic. With minimakers as competitors, Zilog needs software clout, says Sweet.

sales and marketing posts at Perkin-Elmer's Data Systems division (then called Interdata) and at General Electric Co.'s process-control computer and nuclear energy divisions.

Sweet is also at the center of a \$5 million lawsuit brought by National over trade secrets, alleging he and five other former employees took specifications for its upcoming 16-bit microcomputer with them when they joined Zilog [*Electronics*, June 21, p. 34]. Sweet denies any wrongdoing, but otherwise declines to discuss the suit.

New competitors. Chip makers will have to be concerned with systems software as they compete with minicomputer makers, Sweet says, moving on to what is now probably his favorite subject. Digital Equipment Corp., for example, has years of experience with software behind it, "built not only by DEC but by its customers also," he continues. In comparison, a chip maker's software experience amounts to "virtually zero."

Zilog's sales will grow this year to \$40 million, up from last year's \$18 million (see p. 92). In maintaining the firm's growth, software—and Sweet's overall systems approach—will undoubtedly play an ever-increasing role. □

MEASUREMENT COMPUTATION news
product advances from Hewlett-Packard

AUGUST 1979

New plotter developments: automatic paper advance, interfaces for OEMs, and simple operation

HP-IB

Convert your present 7221A or 9872A to include paper advance capability. Although paper advance is an integral part of the plotter and not available as an accessory, HP will convert your existing 9872A or 7221A to include the chart advance capability if it was purchased prior to July 1, 1979. This offer is effective until April 1, 1980.

Recent developments in Hewlett-Packard plotters bring some new capabilities to plotter users.

- Automatic paper advance for unattended plotting with HP's three multicolor plotters—7220S, 7221S, and 9872S.
- Simple, abbreviated, English-like, plotter commands in an RS-232-C /CCITT V.24 interfaced plotter.
- A new RS-232-C/CCITT V.24 interface module to make the low-cost HP 7225A plotter available for many new OEM and end-user applications.

In addition to these new capabilities, HP's existing line of plotters provides a selection to meet your exact graphic needs.

Multicolor Plotters with Paper Advance

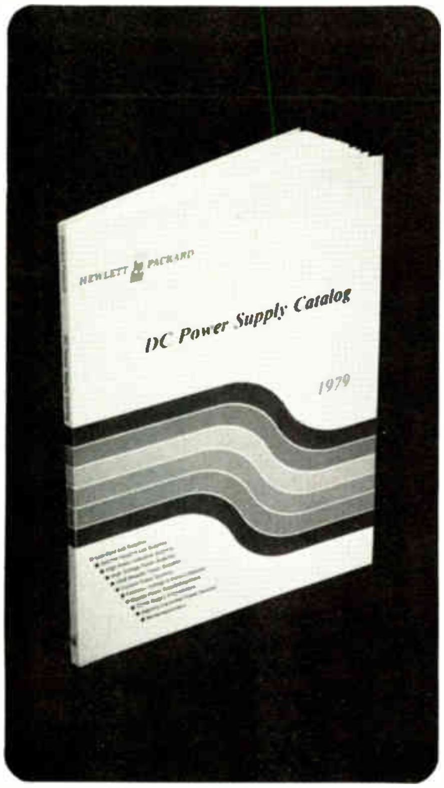
If your plotting needs include:

1) Repetitive or sequential graphics from automated production and engineering test systems
2) Unattended graph generation at a central computer site
3) Frequent multiple copies of quality multicolor graphs for presentations or reports

HP now offers you three choices—the easy-to-program 9872S for HP-IB control-

(continued on third page)

New DC power supply catalog from HP



Choosing the right power supply for your application is easy with HP's new *DC Power Supply Catalog*. This 128-page catalog contains product descriptions, photographs, outline drawings, specifications, and prices for HP's complete line of power supplies covering the range from 10 W to 11 kW. Products include:

- Low-cost lab supplies
- General purpose lab and system power supplies
- Precision voltage and current sources
- High power industrial supplies
- OEM modular power supplies
- Digitally programmable power sources
- Multiprogrammers

Included is a section detailing several methods to control DC power supplies using the HP Interface Bus. In addition, another section covers power supply ac and load connections.

*For your free copy, check **A** on the HP Reply Card.*

New 26.5 GHz pulsed RF counter simplifies radar measurements

This new Automatic Frequency Converter, called the Model 5355A, not only measures the average frequency in rf bursts as narrow as 60 ns, but also uses the time interval capability of the 5345A to measure pulse repetition interval, pulse width, and pulse-to-pulse timing.

The 5355A covers the frequency range of 0.4 - 1.6 GHz. For frequency extension, two frequency converter heads, similar in concept to the familiar power meter heads, are available. These rf heads are called the 5356A 18 GHz Frequency Converter Head and the 5356B 26.5 GHz Frequency Converter Head. For frequency measurements on pulse modulated signals, simply connect the Frequency Converter Head to the source, press PULSE mode on the 5355 keyboard, and read the frequency on the 5345 display. Select the 5345A GATE TIME for the resolution required—as high as 10 kHz, 1 kHz, 100 Hz, or better. Measurements are now completely automatic and require no auxiliary equipment. This means that measurements which used to take highly skilled operators and loads of equipment (e.g. transfer oscillator techniques, cavity wave meters, or spectrum analyzers) can be made easily and quickly. The 5345/55/56 opens up a whole new world of design improvement possibilities by making measurements which simply couldn't be performed previously.

Specific radar measurements made by the 5345/55/56 are:

- Average carrier frequency in pulse.
- Frequency profile of pulse (using a delaying gate from an HP 5359A Time Synthesizer). Measure frequency linearity in pulse compression radars and frequency variation in doppler radar.
- CW microwave and submicrowave frequency from dc - 26.5 GHz. Measure STALO, COHO, or magnetron frequencies to 1 Hz resolution in 1 second.
- Pulse width, pulse repetition interval with 2 ns single shot resolution.
- Pulse repetition frequency with resolution of 2×10^{-9} per second.

The 5345/55/56 is far more than a pulsed microwave counter. It is also a high performance CW microwave counter. High sensitivity of −20 dBm, high FM tolerance of 60 MHz p-p and high resolution suit it for all your CW frequency measurements. Simply push the CW pushbutton on the 5355 and select the 5345A GATE TIME for the desired resolution.

In summary, the 5345/55/56 is the industry's highest performance microwave counter, combining the best performance characteristics of three different instruments into one. You now get the economy and convenience of pulsed, CW and time interval measurements in a single counter.

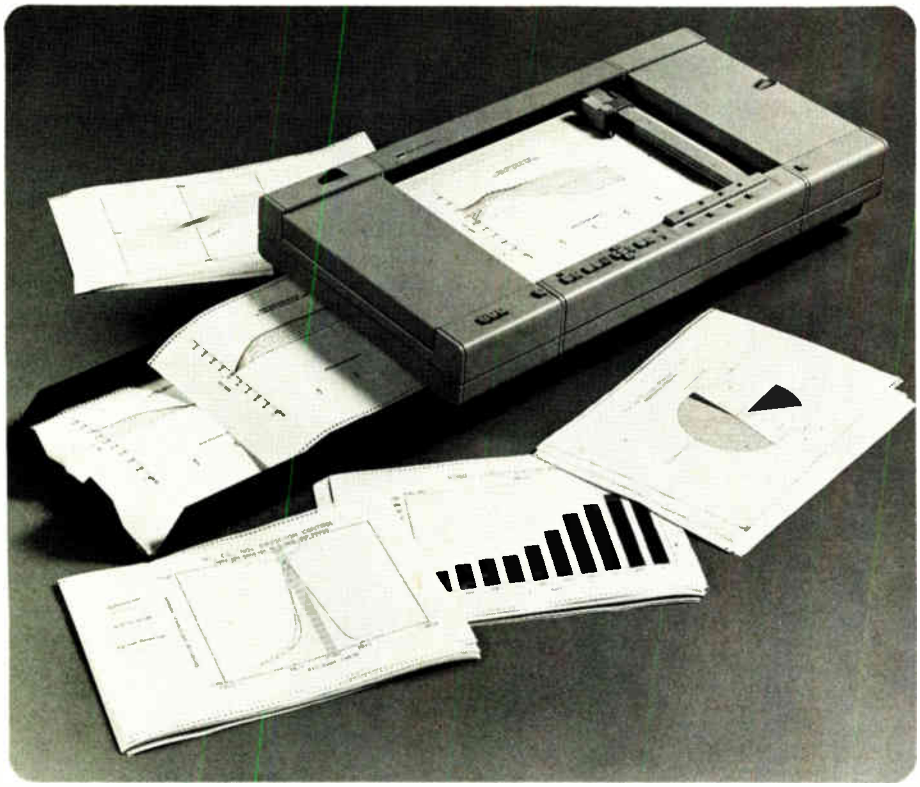
*Get more information by checking **B** on the HP Reply Card.*

With a new automatic frequency converter plug-in for the HP 5345A Frequency Counter, you can now measure pulsed frequencies as well as CW frequencies to 26.5 GHz with greater resolution and accuracy than previously possible.

Automatic paper advance plotters produce up to 280 graphs—unattended

(continued from first page)

HP-IB



In addition to the convenience and economy of unattended plotting, HP's three automatic paper advance plotters also feature an impressive number of other capabilities including: six character sets, 36 pen speeds, and over 40 different graphic instructions.

lers, or the easy-to-use RS-232-C/CCITT V.24 interfaced 7220S, or the optimized for timeshare 7221S. All three of these multicolor plotters feature automatic paper advance which can plot, cut and stack up to 140 A3 (11 × 17 in.) graphs or 280 A4 (8½ × 11 in.) graphs without operator attendance.

The integrated paper advance capability for these plotters consists of two electromechanical modules on the sides of the plotter to hold and pull the 61 m (200 ft.) roll of sprocket-punched paper across the platen. For convenience, the sprocket holes are carried on perforated strips bordering the graph area, allowing you to tear away the sprocket holes for standard size paper output.

In addition, all three of these plotters have all the capabilities and features of their multicolor, single-sheet counterparts, the HP 7220A, the 7221B, and the 9872B. For example:

- Six resident character sets including three European and three Latin sets, and miscellaneous mathematical and centered symbols.
- Programmable character size, slant and direction.
- Over 40 different graphic instructions including automatic pen selection.
- Point digitizing, labeling, character sizing, programmable graph limits, rotation, windowing.
- Excellent line quality and repeatability at all 36 pen speeds, from 10 to 360 mm/s.

24-Hours-a-Day Operation

Paper advance plotters enable you to carry on your plotting 24-hours a day—unattended. Both repetitive graphics for report and meeting presentations, and sequential graphs plotted against changing parameters can be programmed in advance to run through the night.

Shared Graphics Resource

Depending on your interface requirements, either the HP-IB or RS-232-C/CCITT V.24 paper advance plotters, should prove useful to you as a central computer or system resource. Programs can be initiated by a number of users in different locations on your mini or mainframe computer and the output produced on a "shared", unattended paper advance plotter.

HP-IB Systems

Both production test and engineering test procedures using HP-IB systems will benefit from the paper advance plotter's repetitive or sequential graphic reports. Many applications in these areas hitherto impractical for single sheet, operator attended plotting will find paper advance graphics to be a practical and desirable addition to their system.

HP-GL—The Easy Graphics Language

Another new development in HP plotters is the utilization of HP-GL with an RS-232-C/CCITT V.24 interface plotter. A simplified graphics language, HP-GL uses an abbreviated form of English words that are easy to remember and thus easy-to-use.

Several HP plotters, including HP's 7220A, general purpose and OEM plotter have over 40 different, built-in HP-GL instructions to simplify programming.

Low Cost Plotter with Versatile Interfaces

A third new development, the hardwire RS-232-C/CCITT V.24 interface module, now makes the low-cost, high-quality HP 7225A plotter available for many new OEM and end user applications. In addition to its low initial price, the 7225A owner can also expect low-cost-of-ownership thanks to HP's rugged, new linear stepper mechanism that eliminates many moving parts.

This plotter also uses HP-GL language, making graphics instructions and plotter commands easy to remember and easy to use. Its plotting speed between points is 250 mm (10 in.) per second and text is drawn at up to three characters per second.

Three additional personality modules for the 7225A provide HP-IB, GP-10, and 8-bit parallel interfacing to meet various OEM requirements.

*For full information, check **C** on the HP Reply Card.*

Generate high-quality, low-cost overhead transparencies in minutes with enhanced HP 45B and graphics terminal

Creating high-quality overhead transparencies that enhance and reinforce spoken presentations usually entails considerable lead time, expense and inflexibility. One must assemble the data, decide what the format should be and then "rough sketch" what the slide should look like. Then the whole thing is turned over to a graphic artist for production.

A Fast Alternative

To solve this visual data bottleneck, Hewlett-Packard has expanded the capabilities of one of its newest desktop computers and one of its versatile computer terminals. HP's new System 45B or 2647A Intelligent Graphics Terminal, together with the HP 9872A Four-Color Plotter, now enable you to produce professional quality overhead transparencies in minutes and at a fraction of the cost of traditional methods.

Versatile Performance

The System 45B/Plotter or Intelligent Terminal/Plotter system plus HP's new graphics presentation software allows you to generate even the most complete overhead transparencies: graphs, charts, x-y relationships, charts with variable letter sizes, shadings and colors. Plus much more.

No Expertise Needed

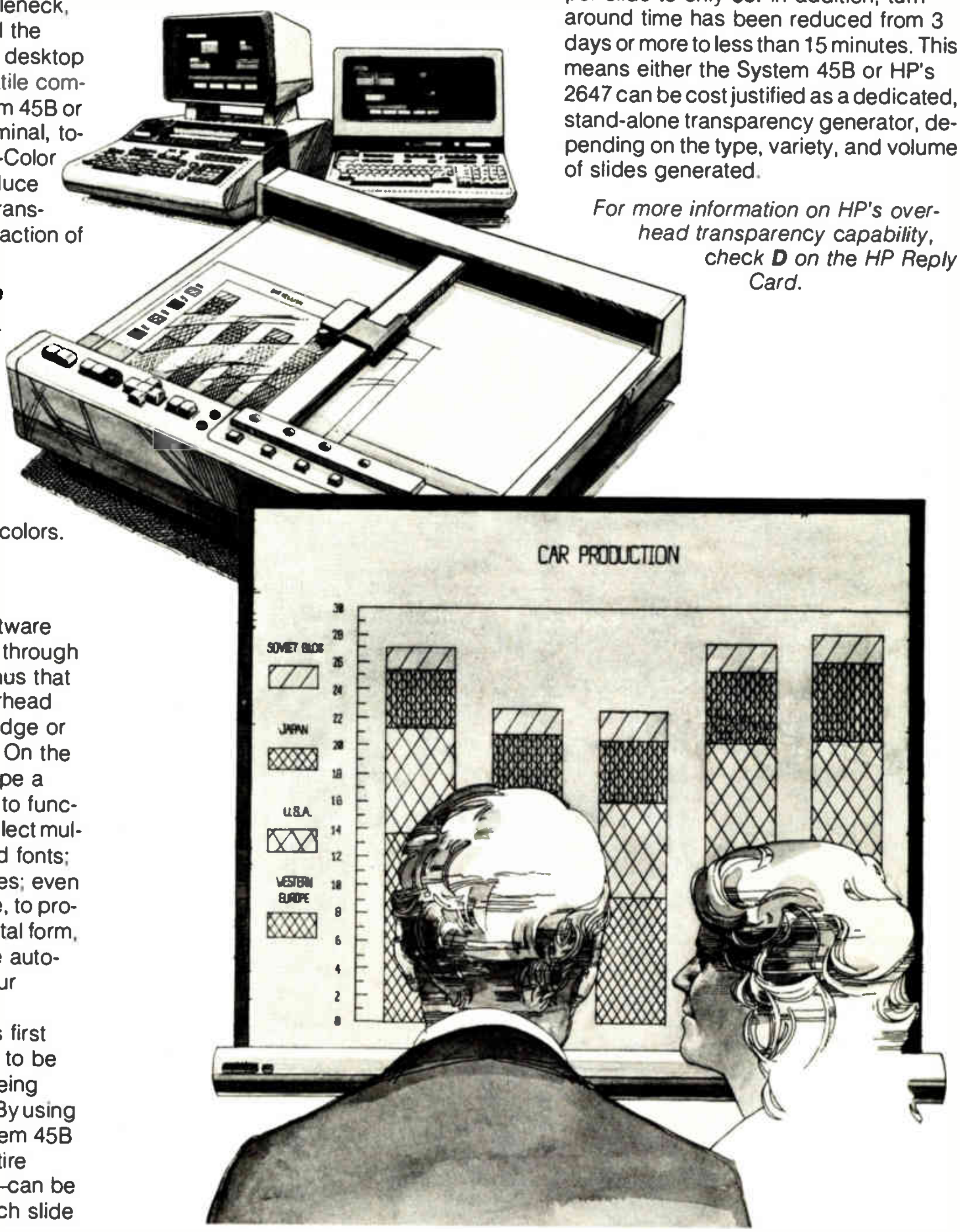
HP graphics presentation software helps you design transparencies through easy-to-use CRT-displayed menus that enable anyone to generate overhead slides. No programming knowledge or computer expertise is required. On the System 45B keyboard simply type a number or letter corresponding to functions displayed on the menu to select multiple colors, character sizes, and fonts; plot graphs and charts; draw lines; even edit transparencies. For example, to produce a slide in vertical or horizontal form, just type in V or H. The software automatically scales and formats your transparency.

To make editing easier, slides first appear on the System 45B CRT to be viewed and/or altered, before being drawn in final form on the plotter. By using tape cartridges on both the System 45B and HP 2647 for storage, an entire presentation—dozens of slides—can be stored on a single cartridge. Each slide can be easily recalled, updated, changed, or deleted as necessary.

Low Cost

The impetus to design such a system and software capability came from HP's realization that producing overhead transparencies was consuming large amounts of time and money. For example, HP's Desktop Computer Division uses about 400 overhead transparencies per month for new product introductions, management presentations and customer training. Producing these transparencies by traditional methods was costing over $140,000 per year. A System 45B Desktop Computer and its Graphics Presentations Software Pack, coupled with an HP 9872A Plotter has reduced this expediture to about $14,500 or from $30 per slide to only $3. In addition, turn around time has been reduced from 3 days or more to less than 15 minutes. This means either the System 45B or HP's 2647 can be cost justified as a dedicated, stand-alone transparency generator, depending on the type, variety, and volume of slides generated.

*For more information on HP's overhead transparency capability, check **D** on the HP Reply Card.*



HP offers "how to" newsletter for service technicians

Bench Briefs, a bimonthly publication, is your private line to Hewlett-Packard customer service. It is offered to technicians doing repair, calibration, incoming inspection, and system configuration of HP electronic instruments. It is particularly useful to service managers that want to plan future training programs for their personnel.

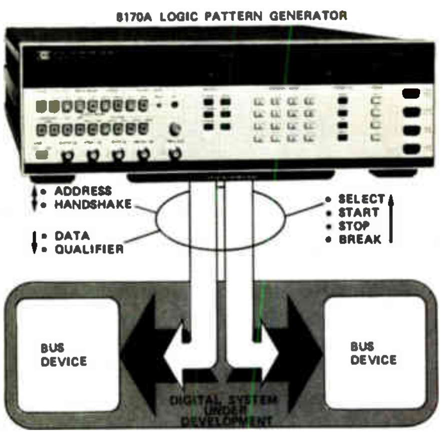
This attractive 8-page bulletin contains customer seminar training schedules, service tips, instrument modifications, new methods of testing, and new tools that simplify service and troubleshooting. Bench Briefs are full of practical information such as HP-IB programming hints for selected instruments, or Hewlett- Packard's IC and transistor part number to manufacturer number cross references, as well as factory recommendations for updating or modifying HP products.

*For a sample issue and a subscription qualification form, check **E** on the HP Reply Card.*

Bench Briefs: an HP service that improves your service.

Give your bus devices a better chance—simulate system conditions early in development

HP-IB



With many bus capabilities, the 8170A can stimulate practically any bus device.

Designing a digital system? Developing a hardware control circuit? Trying out a new D/A? For success at system level, each device must be developed and tested under the exact conditions it will later meet. This is scarcely possible with "homemade" switch boxes. Even data generators lacked the specialized bus capabilities. But now, with the HP 8170A Logic Pattern Generator, you can create true-to-life conditions right from the start. Device development becomes independent and you can make decisions before firmware and software are committed.

For hardware function tests, the 8170A's 8/16-bit bus provides an adequate data depth from the nonvolatile memory. Keyboard entry in the selected address and data codes facilitates rapid data loading. The handshake capability extends application to dynamic test of peripheral adaptors, duplex peripherals and remote I/Os. For memory-buffered peripherals such as alphanumeric displays, the 8170A emulates the R/W operation envisaged with the processor.

*For details, check **F** on the HP Reply Card.*

Microwave link analyzer offers dual IF capability

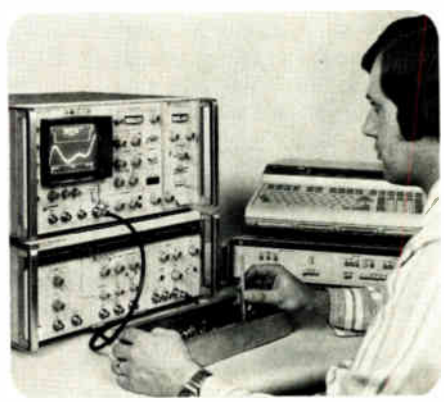
HP-IB

For microwave radio stations employing 70 and 140 MHz intermediate frequencies, the 3711A/3712A Microwave Link Analyzer (MLA) is an economical way of providing a complete range of dedicated measurements at both 70±25 MHz and 140±50 MHz. The back-to-back residual performance of this latest MLA has been improved substantially, making it the best currently available. Further improvements in measuring performance can be achieved with the addition of digital averaging and normalizing accessories.

In FM radio relay systems, IF flatness measurements with a resolution of 0.025 dB/cm are required frequently. At such sensitivities, the errors introduced by connecting cables may be significant. HP's MLA incorporates a slope control which can be adjusted to compensate for these errors. In contrast to FM systems, digital radio links require a larger dynamic display range for IF flatness measurements. For such applications, the new MLA provides 16 dB range.

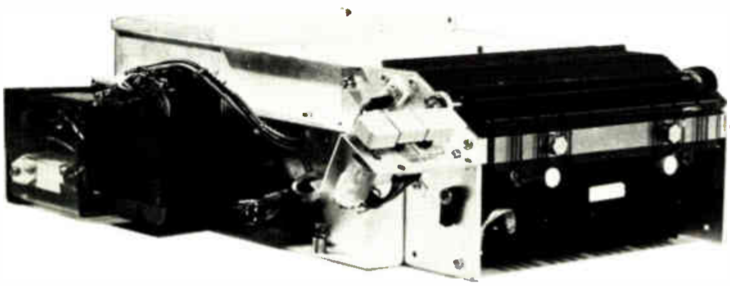
The MLA's new frequency identification system provides both fixed and variable markers. The variable marker may be adjusted over the whole measurement range while its frequency is continuously monitored on a 5-digit counter. The same counter can be used to measure the frequency of IF signals, providing a quick and easy method of checking and adjusting modulator center frequency.

*For more information, check **G** on the HP Reply Card.*



Measurement limit masks and adjustment instructions may be displayed on the screen when the new dual IF MLA is used with an 8501A Storage-Normalizer and desktop computer.

HP's high speed thermal graphics printer available to OEM's



The caseless version of HP's new thermal graphics printer, Model 11479A, facilitates integration into OEM systems.

HP-IB

- speeds of up to 480 lines-per-minute
- high resolution (77 dots per inch) characters
- sophisticated graphics capability and alphanumeric printing

The most versatile HP printer ever offered, the 9876A Thermal Graphics Printer, is now available to OEMs. Combined with design flexibility, the 9876's proven features of high-speed, quiet operation, superb print quality and reliable performance offer the OEM virtually unlimited marketing opportunities.

Design Flexibility

Two interfacing modes provide flexibility of use with a wide variety of large computers, desktop computers and terminals from HP, as well as from other manufacturers. The 9876's 7-bit or 8-bit parallel interface, with ASCII TTL level, features Strobe, Peripheral Acknowledge, and Busy lines, and readily adapts to most popular parallel printer interfaces on the market today. The 9876 also uses HP-IB (Hewlett-Packard's implementation of IEEE Standard 488-1975) interfacing.

An OEM can choose to purchase the 9876 with or without its outer shell. In either configuration, the printer is fully functional and ready to be connected to the system. Without its outer shell (Model 11479A), the unit can be incorporated in the OEM's cabinetry to better fit functional and product design requirements.

Printhead Technology

The heart of the 9876 is its monolithic printhead. A unique thin film technique, developed and proven by Hewlett-Packard, uniformly spaces 560 print resistors on .33 mm (.013 in.) centers. Because of their low thermal mass, these print resistors can be heated and cooled very rapidly so that speeds of up to 480 lines-per-minute can be attained. Microprocessor control insures reliability by monitoring and controlling all voltages as well as the printhead temperature. This protects the printhead from potential damage.

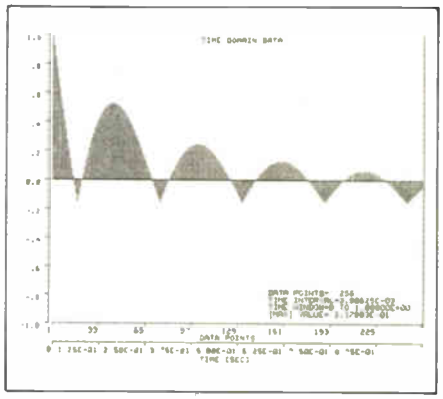
The 9876 prints characters in a 5×7 dot matrix. Its full character set contains 128 standard ASCII characters (upper and lower case) and control characters. Seven additional character sets, always in the printer, can be accessed through software: French, German, Katakana, British, Spanish, Danish/Norwegian and Swedish/Finnish. Also, users can create up to seven new characters at a time by defining special dot patterns which are then stored in the printer's memory.

High Contrast Paper

Another advantage of the 9876 is its thermal paper. The 9876's black-print paper sets a new standard for high-contrast and fade resistance. Its printouts provide excellent reproduction capability over an extended length of time. The blueprint paper provides excellent, high-contrast printouts, especially well suited for immediate work sources. Available in either 8½ in. or 21-cm widths, the 9876 thermal paper comes fanfolded, flat packaged, and perforated into 330 standard size sheets. And it's simple and quick to load.

The reliable performance of the 9876 is the result of continued technological advancements made by HP in thermal printing for its computer product line. The 9876 is further supported by HP's responsive service organization located in more than 170 locations throughout the world.

*To find out more about the OEM advantages of HP's 9876A, check **H** on the HP Reply Card.*



The HP thermal graphics printer is excellent for applications which require high-speed listings, frequent work reports or quick plotting and graphics.

```
60          DIM A$[180]              ! Dimension A$
70          PRINTER IS 7,1           ! Assign FLASH as system printer.
80    !     Re-define left bracket as double quote [ to "
90          PRINT USING "#,K";CHR$(27)&"&n91c20f20g20H"
100         PRINT CHR$(27)&"&k1S";TAB(35);"DEMO  INSTRUCTIONS  "&CHR$(27)
110         PRINT LIN(1)             ! Print first 3 lines manually
120   In:   READ A$                  ! Fetch line
130         IF A$="QUIT" THEN Done   ! Finished ?
```

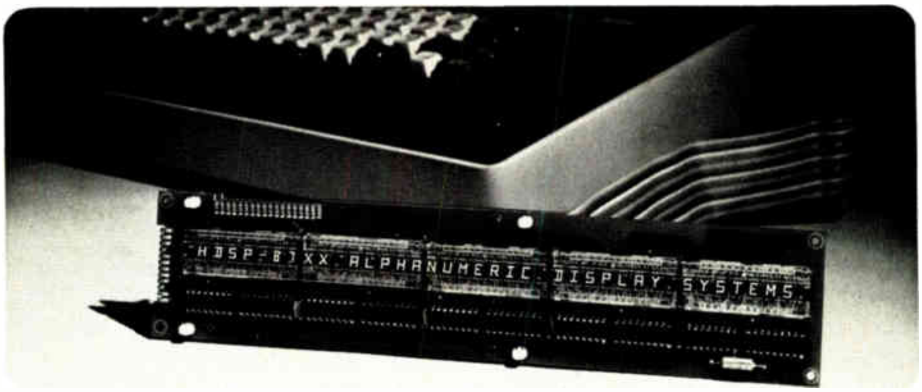
HEWLETT-PACKARD COMPONENT NEWS

18-segment display system is μP based and has low power requirements

A proven display with a microprocessor-based controller to provide an easy-to-read display, very low power requirements and easy interfacing has been introduced by Hewlett-Packard.

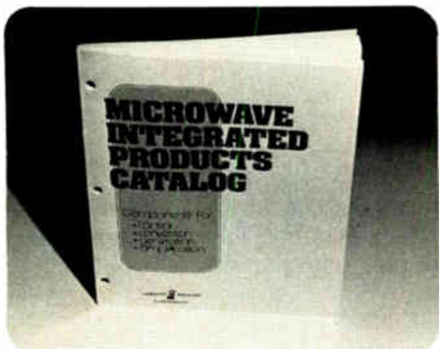
This new system, the HDSP-87XX Series, substantially reduces the engineering development costs and time previously required for an 18-segment display. Incorporated into the microprocessor controller are pre-programmed routines to accept, decode and display standard ASCII data. In addition, the 5.0 V operation, standard LSTTL compatible inputs and four separate display formatting modes, allow easy interface to the customer's keyboard or microprocessor-based system.

The low voltage, compact size and solid state features are great for applications in instrumentation, telephone equipment, data entry terminals and automatic banking terminals. Single line 16-, 24-, 32- or 40-character display lengths are available.



The new HDSP-87XX series is now available from all Hewlett-Packard component distributors.

*Check **I** on the HP Reply Card for more information.*



New designer's catalog available—free

A new designer's catalog describing HP's microwave integrated products is now available. The catalog contains listings of a broad line of components for the control, conversion, generation and amplification of RF and microwave systems.

Detailed, up-to-date specifications are provided for all products listed, including switches, attenuators, comb generators, limiters and detectors.

Amply illustrated with charts, graphs and photos, this 80-page catalog can be a valuable tool for designers of communications systems, instrumentation, measurement systems, EW, and radar systems.

*For your free copy, check **J** on the HP Reply Card.*

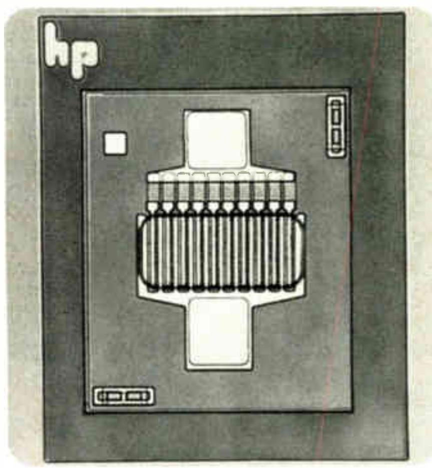
Hybrid designs made easier with new bipolar transistor chip

For economical hybrid designs with 100 mW linear power and gain to 5 GHz, consider HP's new, reliable HXTR-5001 Silicon Bipolar Transistor Chip.

This new transistor, the fourth in HP's family of bipolar chips, offers typical power output figures at 1 dB gain compression of 23 dBm at 2 GHz and 22 dBm at 4 GHz. Typical associated gain is 13.5 dB at 2 GHz and 8 dB at 4 GHz.

For high performance along with low cost, the HXTR-5001 is a designer's dream for wide dynamic range broadband applications. For immediate delivery, call your local franchised HP distributor.

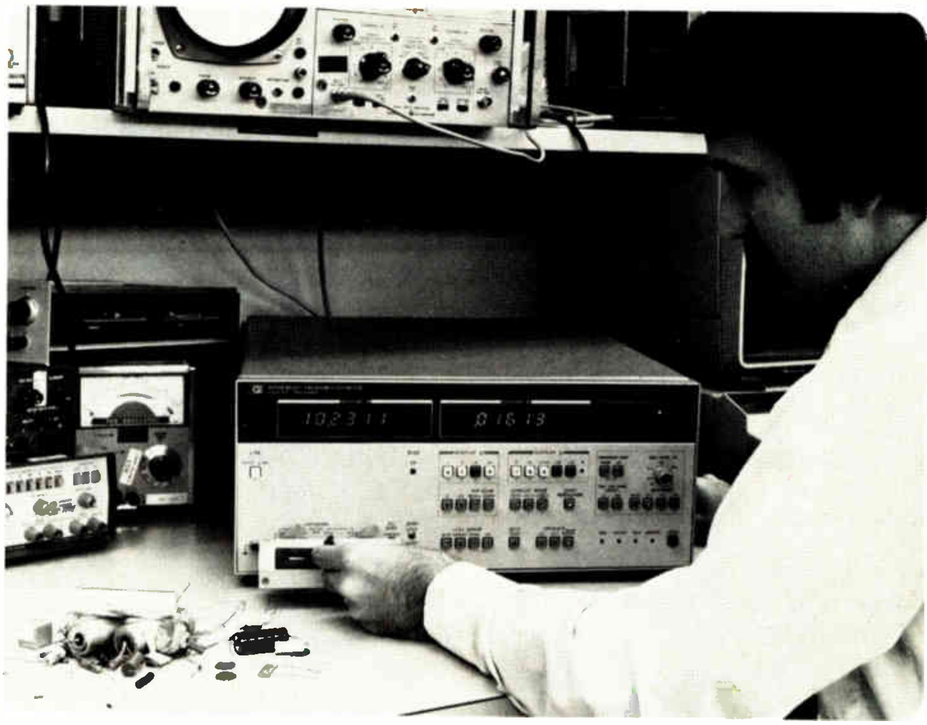
*Send for the complete technical data sheet, including S-parameters, bonding instructions, and design information. Check **K** on the HP Reply Card.*



New general-purpose linear power transistor chip is designed for high output power and gain to 5 GHz.

Test your components under conditions similar to actual circuit operation

HP-IB



New multi-frequency LCR meters for lab, production and quality control.

Discrete components, as well as semiconductor devices, can now be evaluated under conditions similar to those in which they operate. Hewlett-Packard's new microprocessor-controlled, multi-frequency LCR meters give you component and semi-conductor test capability in a laboratory, a production line and in quality control/inspection measurements.

Automatic Features

With a push of a button, HP's new 4274A and 4275A LCR meters are automatically set up to measure L,C,R, D, Q, G, ESR, X, B, /Z/ - Θ, delta or delta percent in either parallel or series modes and at or near operating signal level and frequency. Both instruments have automatic zero offset capability that automatically compensates for stray capacitance and residual inductance in test leads or fixtures at all spot frequencies.

For low to medium frequency (100 Hz to 100 kHz) applications, the 4274A offers measurements at 11 spot frequencies. This provides more accurate measurements when determining ESR frequency characteristics of electrolytic capacitors and testing of MIL and IEC specified components. For higher frequencies, choose HP's 4275A. Ten spot frequencies between 10 kHz and 10 MHz are standard, making high frequency *C-V* characteristics in semiconductors easier to do.

The 5½-digit, high-resolution mode and 0.1% basic accuracy greatly contribute to the quality and reliability of impedance measurements on electronic components and materials.

Standard Features

There are many other built-in, standard features in HP's 4274A and 4275A LCR meters, such as automatic/manual operation, self test, remote HP-IB operation and current/voltage monitoring.

*To find out all the details on these new multi-faceted LCR meters, please check **L** on the HP Reply Card.*

East-4 Choke Cherry Road, Rockville, MD 20850, Ph. (301) 258-2000
South-P.O. Box 10505, 450 Interstate North Pkwy., Atlanta, GA 30348, Ph. (404) 434-4000
Midwest-5201 Tollview Dr., Rolling Meadows, IL 60008, Ph. (312) 255-9800.
West-3939 Lankershim Blvd, North Hollywood, CA 91604, Ph. (213) 877-1282.
Europe-Central Mailing Depot., P.O. Box 529, Amstelveen-1134, Netherlands, Ph. (020) 47 20 21.
Japan-Yokogawa-Hewlett-Packard Ltd., Ohashi 29-21 Takaido-Higashi 3-chome Suginami-ku, Tokyo 168, Ph. 03-331-6111.

HEWLETT hp PACKARD

MEASUREMENT COMPUTATION news
product advances from Hewlett-Packard

July/August 1979

New product information from

HEWLETT-PACKARD

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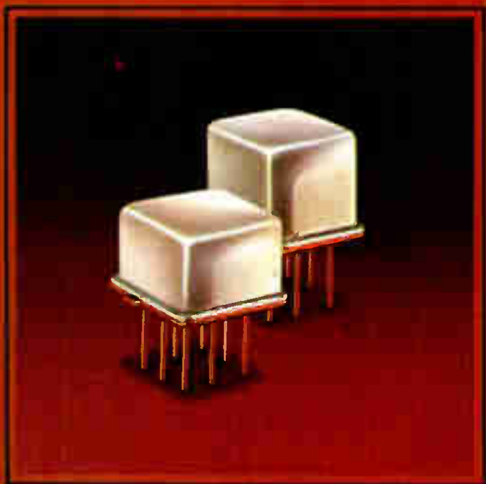
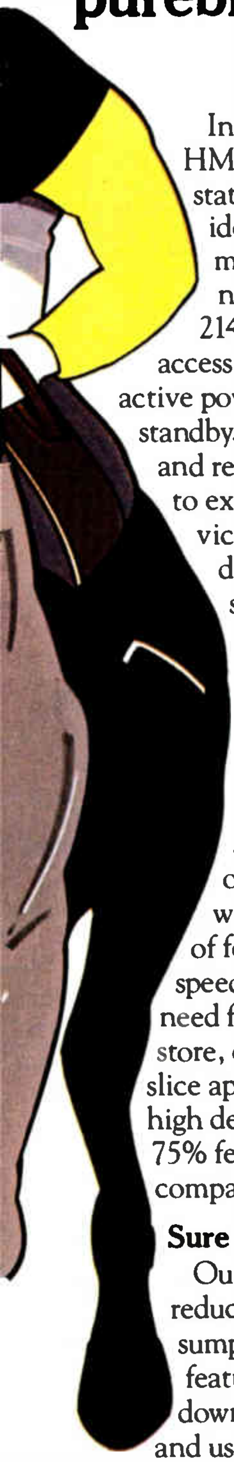


HMOS Goes 4-wide

Intel delivers the 1Kx4-bit 2148 fast static RAM, purebred descendent of our high performance 2147.



Introducing the first HMOS* high performance static RAM organized ideally for wide-word memory systems. Intel's new 1Kx4-bit HMOS 2148 gives designers access times to 55ns, low active power and automatic standby. Plus the economy and reliability you've come to expect from MOS devices. In fact, the 2148 delivers exactly the same advantages as our HMOS industry standard 4Kx1-bit 2147.

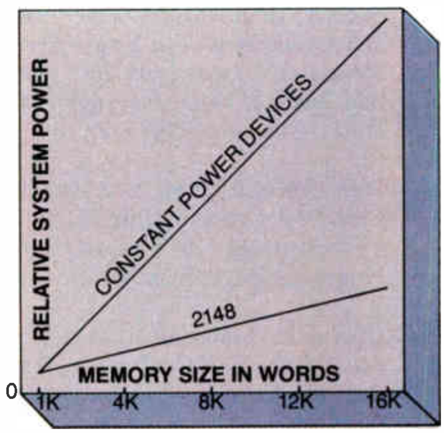
The 2148 is great news for anyone designing high speed, special purpose memories where word widths are in multiples of four. You'll get the speed and modularity you need for high speed control store, cache, buffer and bit-slice applications. Plus the high density that means 75% fewer components than comparable 1K designs.

Sure bet for lower power

Our 2148 will help you reduce system power consumption dramatically. It features automatic power down on deselection and uses standby current only a fraction that of constant current devices. And since most memory components in a system are normally deselected at any given time, the larger your system the lower your power dissipation per bit. (See chart.) It means simpler designs and lower costs for cooling and power supplies.

Our track record: 7 million reliable HMOS RAMs

We achieved the 2148's fast access and low power using HMOS. It's the patented high performance technology we pioneered in 1976 with our 2115A/2125A 1K fast static RAMs. And



it's the same process we use to produce our industry standard 16-bit microcomputer, the 8086.

Intel has already delivered over 7 million HMOS RAMs. This gives 2148 users a proven track record of reliability and volume availability. For more detailed information on HMOS dependability, request our comprehensive HMOS Reliability Report #18.

The 2148 is in the 18-pin 1Kx4 industry standard pinout. It is fully static, so you can use it in both

2148 Specifications			
	2148-3	2148	2148-6
Max. Access Time (ns)	55	70	85
Max. Active Current (mA)	125	125	125
Max. Standby Current (mA)	30	30	30

clocked and unclocked systems. All three 2148 versions are fully TTL compatible and operate from a single +5 volt supply.

Intel gives you a head start

We're delivering the 2148 today. To get a head start on the next generation of high performance memory designs, contact your local Intel sales office or distributor. Or write Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051.

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*HMOS is a patented Intel process.

Meetings

Conference on Simulation, Measurement and Modeling of Computer Systems, National Bureau of Standards *et al.*, University of Colorado, Boulder, Colo., Aug. 13–15.

Third Rocky Mountain Symposium on Microcomputers, IEEE *et al.*, Colorado State University, Pingree Park, Colo., Aug. 19–21.

International Conference on Parallel Processing, IEEE, Shanty Creek Lodge, Bellaire, Mich., Aug. 21–24.

23rd Annual International Technical Symposium and Exhibit, The Society of Photo-Optical Instrumentation Engineers (Bellingham, Wash.), Town and Country Hotel, San Diego, Calif., Aug. 27–30.

Compcon Fall '79—19th IEEE Computer Society International Conference, IEEE, Capital Hilton Hotel, Washington, D. C., Sept. 4–7.

Second International Fiber Optics and Communications Exposition, Information Gatekeepers Inc. (Brookline, Mass.), Hyatt Regency O'Hare Hotel, Chicago, Sept. 5–7.

25th Annual Holm Conference on Electrical Contacts, Illinois Institute of Technology (Chicago), Palmer House, Chicago, Sept. 10–12.

Dielectric Materials, Measurement and Applications Conference, Institution of Electrical Engineers (London), University of Aston, Birmingham, England, Sept. 10–13.

Fall Conference, USE Inc. (the organization for those who use Sperry Univac's series 1100 computers, Bladensburg, Md.), Diplomat Hotel, Miami, Fla., Sept. 10–14.

Optical Communication Conference, IEEE, RAI Conference Building, Amsterdam, Sept. 17–19.

Ninth European Microwave Conference, Institution of Electrical Engineers (London), The Brighton Centre, Brighton, Sussex, England, Sept. 17–21.

Impact of Improved Clocks and Oscillators on Communication and Navigation, National Bureau of Standards, NBS headquarters, Gaithersburg, Md., Sept. 18–20.

Wescon/79 Show and Convention, IEEE and Electronic Conventions Inc. (El Segundo, Calif.), Brooks Hall, San Francisco, Sept. 18–20.

Autotestcon—Automatic Support System for Advanced Maintainability Conference, IEEE, Radisson Hotel, Minneapolis, Sept. 19–21.

29th Annual Broadcast Symposium, IEEE, The Washington Hotel, Washington, D. C., Sept. 19–21.

Telecom '79—Third World Telecommunications Exhibition, International Telecommunications Union, Palais des Expositions, Geneva, Sept. 20–26.

IPC Fall Meeting, The Institute for Interconnecting and Packaging Electronic Circuits (Evanston, Ill.), Sheraton Palace Hotel, San Francisco, Sept. 23–27.

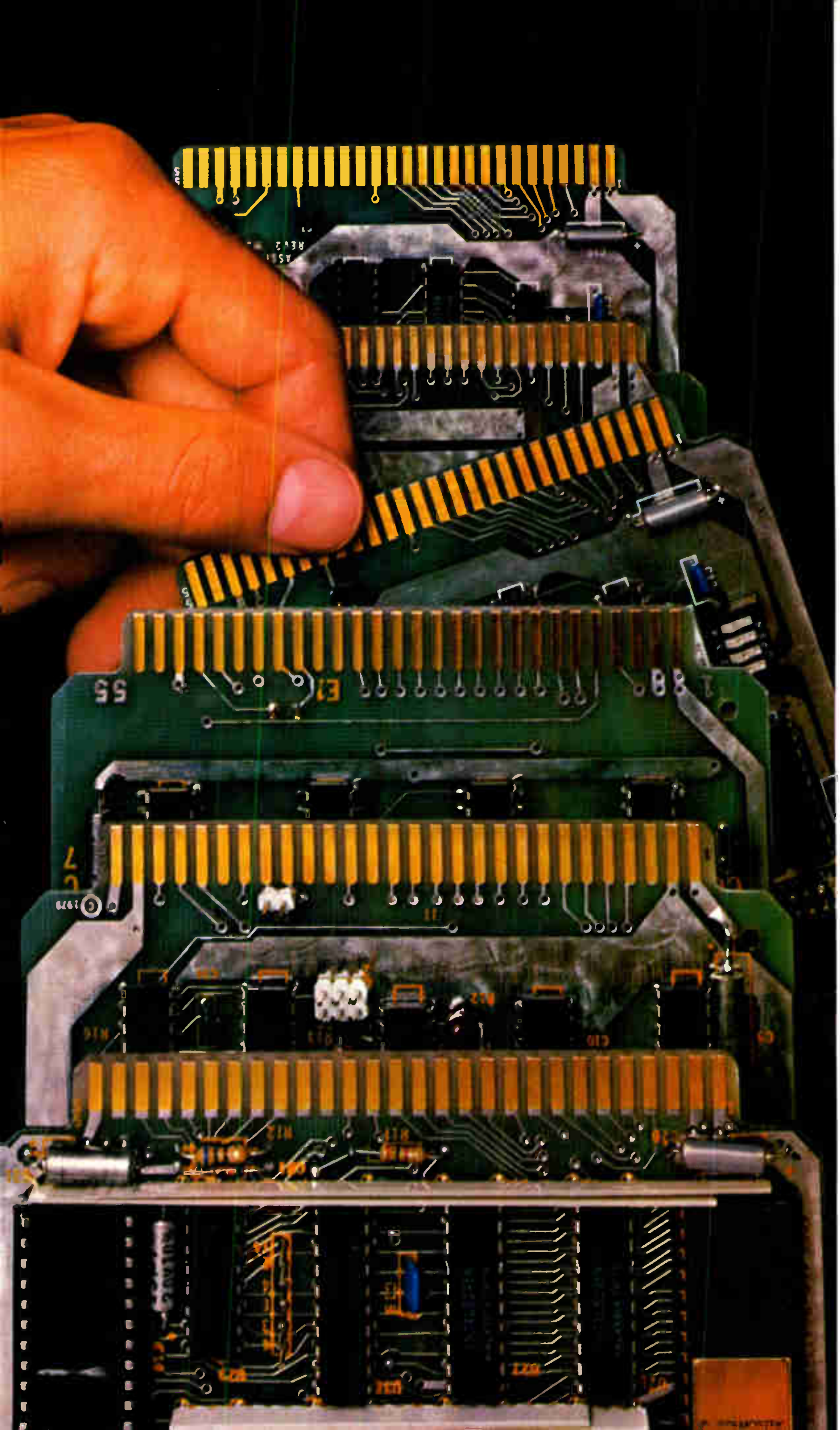
Mini/Micro Computer Conference and Exposition, sponsored by the organization of the same name (Anaheim, Calif.), Anaheim Convention Center, Anaheim, Sept. 25–27.

Second International Conference on Electrical Variable Speed Drives, Institution of Electrical Engineers, at the IEE headquarters, London, Sept. 25–27.

Ultrasonics Symposium, IEEE, Monteleone Hotel, New Orleans, Sept. 26–27.

Gallium Arsenide Integrated Circuit Symposium, IEEE, Sahara Tahoe Hotel, Lake Tahoe, Nev., Sept. 28–29.

Northeast Personal and Business Computer Show, Northeast Expositions (Brookline Village, Mass.), Hynes Auditorium, Boston, Sept. 28–30.



MDX-UMC

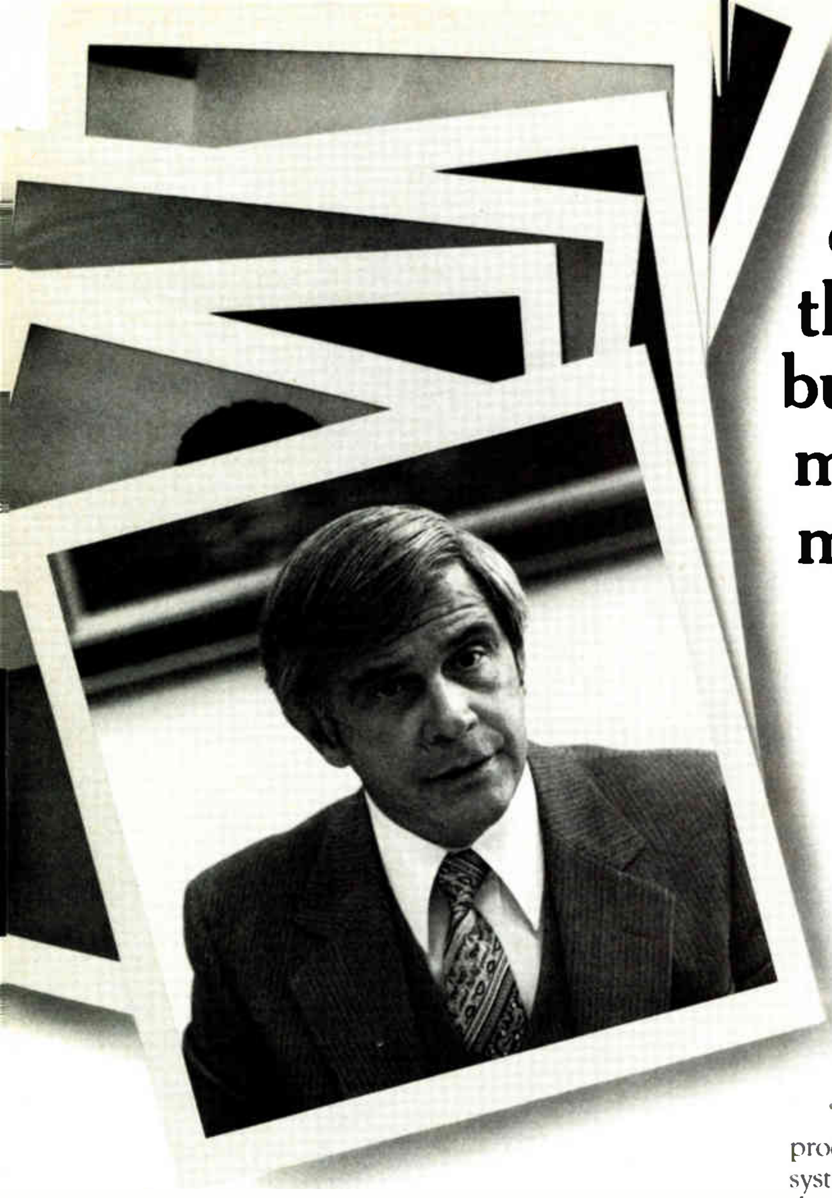
MDX-MATH

MDX-EPROM-4

MDX-SST

MDX-A/D 8

MDX-FLP



"The more competitive the video terminal business gets, the more Intel helps us maintain leadership."

Sal Nuzzo, President,
Hazeltine Corporation

Sal Nuzzo: "Intel's introduction of the microcomputer revolutionized the computer terminal industry. We were first to use a microcomputer in a terminal – Intel's 8008, years ago, and we've maintained a price/performance edge over the years by quickly taking advantage of Intel's breakthroughs.

"This is a tough, competitive industry. Getting a product to market first can make all the difference. Any company that doesn't move fast to take advantage of new technology will simply get left behind. So at Hazeltine, a key part of our strategy is to work closely with technology leaders – such as Intel. They introduced the microcomputer, and have continued to innovate with developments such as the 16-bit 8086 microcomputer. Taking advantage of their new products has enabled us to consistently give our customers higher performance and greater reliability.

"Intel makes it easy for us to apply their new products. An example is the Intellec® development system. Frankly, I don't see how any company can design a product that uses microcomputers without a system such as the Intellec system. The Intellec system features such as in-circuit emulation (ICE) and PL/M programming language are essential time-savers. With our Intellec systems we can convert our existing programs for the 8080 microcomputer to Intel's new 16-bit microcomputer, the 8086, quickly, and increase throughput ten times. That's flexibility."

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Circle No. 34 for information

Electronics newsletter

Mostek showing new 8-bit C-MOS a-d converter . . .

With its eye on the growing market for general-purpose data-conversion devices, Mostek Corp.'s Telecommunications department plans to begin shipping samples next month of a complementary-MOS analog-to-digital converter chip **that could be the first in a new line of components** from the Carrollton, Texas, company. The MK5160 will be a 16-channel-input 8-bit device designed as a pin-compatible alternative to the ADC0816 built by National Semiconductor Corp., Santa Clara, Calif.

. . . as well as CCD filter to use with codec

Mostek Corp.'s Telecommunications department has also been active with new circuits within its specialty area lately. In March, the group began quietly circulating limited quantities of samples of a **charge-coupled-device filter known as the MK5201 designed to work with Mostek's complementary-MOS codec parts.** The 5201 is housed in a 16-pin package with typical power dissipation specified as 100 mW. Though available only on a limited basis to select customers to date, samples of the part are scheduled to be shipped through normal sales channels in September.

Satellite antenna for urban sites coming from GTE

GTE plans to announce what may be the first satellite communications antenna aimed at the urban environment—**most now are placed far from electronically noisy cities, making necessary long ground links.** The antenna, to be unveiled next month by the GTE International Systems Corp., Waltham, Mass., at Telecom-79 in Geneva, Switzerland, uses unusual offset-feed geometry and strategically placed microwave absorber material to cut its sensitivity to terrestrial interference. Its sidelobes are as much as 10 dB lower than those of conventional designs while its beam is pencil thin—about half a degree wide.

Western Digital designs chip for X.25 packet switching

Specialty semiconductor house Western Digital Corp. appears to have the first entry into what is shaping up as another lucrative device business: **a single chip that supplants software for controlling a data interface with packet-switching networks.** Specifically, the Western Digital device, the WD2501, is designed for the X.25 packet-switching protocol, now the world standard. It implements the first two levels of X.25, physical and link controls that are administrative procedures allowing a user to get in and out of the network, in a complex chip of about 30,000 gates. The Newport Beach, Calif., firm already has discussed the device with many potential customers and specification sheets go out this month, to be followed in October by samples.

Feerst backs Schneider for IEEE president

Forced by a heart attack to withdraw from this year's IEEE election, perennial presidental candidate Irwin Feerst has thrown his support behind Burk Schneider, who was nominated by the board of directors. Feerst has decided on Schneider because of the candidate's views on professional activities, **especially on the issue of job security for EEs.** Feerst's move will confuse the voting in what is now a two-way race between Schneider and petition candidate Leo Young, who is presently the executive vice president of the Institute of Electrical and Electronics Engineers. In the last election Feerst pulled a little over 40% of the vote; however, his support among voters appears to be slipping. This year's balloting would have been his fifth try to become IEEE president.

Electronics newsletter

NEC's U.S. arm to build, sell Multibus boards

NEC Microcomputers Inc., the U. S. marketing and services outlet for some of Nippon Electric Corp.'s chips, has found a niche of its own. According to David Millett, marketing manager for the Wellesley, Mass., company, it will soon begin **building and marketing a family of Multibus-compatible board products.** The first will be a floppy-disk controller board that will use NEC's μPD765 dual-density chip.

National's NS16000 will be family of 8, 16, and 32 bits

Coming into the 16-bit microcomputer market behind Intel, Zilog, and Motorola, National Semiconductor Corp. plans to try to make up the lost ground and more when its NS16000 breaks from the gate next year. In a move to pass the field, the Santa Clara, Calif., firm is expected to announce the NS16000 as a family of 8-, 16-, **and 32-bit microcomputers that would let customers upgrade capabilities within the same family,** say industry insiders. The NS16000 series, made with National's new shrunken n-channel MOS process called X-MOS, may also include specialized coprocessors to handle high-level languages and other functions. The NS16000 is the subject of a suit by National against Zilog (p. 92).

Peripherals coming from TI for suport of 9900A

Look for Texas Instruments Inc. to begin shipping samples soon of several new general-purpose peripheral chips designed for use with the integrated-injection-logic version of the company's 16-bit 9900 microprocessor—the SBP9900A. To be fabricated on an I^2L gate array that the Dallas company has developed for internal use, **the new peripheral chips will be the first to support the 9900A,** which was introduced in its original version more than two years ago. Expected in sample quantities before year-end are the SBP9960, 61, 64, and 65. They will handle functions such as input/output control and timing.

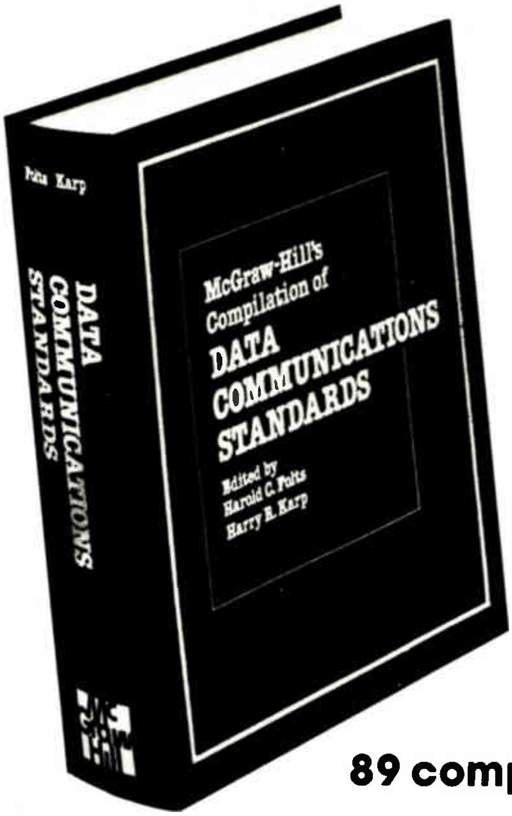
Executive salaries growing 8.6% this year, says AEA

Reflecting the booming marketplace, average salaries of electronics executives are up 8.6% from their base salaries a year ago, according to a survey of 610 companies covering 3,900 managers by the American Electronics Association. **But, as might be expected, chief executive officers are averaging 11%.** Excluding bonuses, average base salaries for CEOs in $5 million, $100 million, and $1 billion companies rose, respectively: $10,000 to $70,000; $20,000 to $120,000; and $20,000 to $195,000 over last year. In the same company categories, senior manufacturing executives average 10% raises to $38,000, $65,000, and $95,000, respectively. Senior marketing and engineering executives show similar percentage increases to, respectively, $40,000, $60,000, and $80,000 or more.

Addenda

Millennium Systems Inc. of Cupertino, Calif., will introduce at Wescon next month **a microprocessor evaluation and troubleshooting instrument** that will sell for less than $1,000. It is called the Micro System Designer. . . . Fairchild Camera and Instrument Corp. is soon to embark on an ambitious program **to let customers design their own 3870-like microcomputers.** The company has divided the basic chip into four sections—central processor, memory, input/output, and analog—and will let the user mix and match functions. . . . **George Schlageter has been named director of manufacturing operations** at the new Mahwah, N. J., oscilloscope plant of Philips Test and Measuring Instruments Inc.

Circle #37 for information



Instant American Data Comm

Edited by
HAROLD C. FOLTS, data communications standards consultant; and HARRY R. KARP, Editor-in-Chief, *Data Communications*, McGraw-Hill Publications Company.
1133 pages.

89 complete and unabridged standards

Consultative Committee for International Telephone and Telegraph
43 standards, including...

V.2	Power levels for data transmission over telephone lines
V.15	Use of acoustic coupling for data transmission
V.54	Loop test devices for modems (and provisional amendments, May 1977)
X.25	Interface for terminals operating in the packet mode on public data networks
X.28	Interface for a start/stop mode on a public data network situated in the same country
X.29	Procedures for exchange of control information and user data between a packet mode DTE and a packet assembly/disassembly facility (PAD)
X.95	Network parameters in public data networks

Electronic Industries Association
13 standards, including...

RS-232C	Interface between data terminal equipment and data communication equipment employing serial binary data interchange
RS-269B	Synchronous signaling rates for data transmission
RS-363	Standards for specifying signal quality for transmitting and receiving data processing terminal equipments using serial data transmission at the interface with non-synchronous data communication equipment
RS-449	General purpose 37-position and 9-position interface for data terminal equipment and data circuit-terminating equipment employing serial-binary data interchange

International Organization for Standardization
11 standards, including...

ISO 646-1973	7-bit coded character set for information processing interchange
ISO 1745-1975	Information processing—basic mode control procedures for data communications systems
ISO 3309-1976	Data communication—high-level data link control procedures—frame structure

American National Standards Institute
11 standards, including...

X3.4	Code of information interchange
X3.24	Signal quality at interface between data processing technical equipment for synchronous data transmission
X3.36	Synchronous high-speed data signaling rates between data terminal equipment and data communications equipment
X3.44	Determination of performance of data communication systems

Federal Standards
11 standards, including...

FED-STD-1003	Bit oriented data link control procedures
FED-STD-1010	ASCII bit sequencing for serial-by-bit transmission
FED-STD-1011	Character structure for serial-by-bit ASCII transmission
FED-STD-1012	Character structure for parallel-by-bit ASCII transmission

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NPN	PNP	Package	BV_{CEO} Volts	f_T MHz	Prices (100-up) NPN	PNP
8 A Drivers						
MJ3247	MJ3237	TO-66	120	20	$1.20	$1.30
MJ3248	MJ3238	TO-66	150	20	1.35	1.45
MJ4247	MJ4237	TO-3	120	20	1.65	1.80
MJ4248	MJ4238	TO-3	150	20	1.75	1.90
MJE15028	MJE15029	TO-220	120	30	1.15	1.22
MJE15030	MJE15031	TO-220	150	30	1.30	1.40
18 A Outputs						
MJ15022	MJ15023	TO-3	200	4	3.00	3.20
MJ15024	MJ15025	TO-3	250	4	3.50	3.70

All are complements. Gain linearity is typically a flat 2:1 for any given unit, gain matching 3:1 for any pair over a 100 mA to 3 A range. Min gain is 40, reducing to 20 at 4 A. No other drivers sound off like that.

With 20 MHz min f_T plus 0.1 μs typ t_f they make excellent switches and there's no chance they'll slow down your output devices one bit.

Speak loudly and carry a big load.

To get distortion-free performance while driving high inductive loads such as speakers, you need output units with high SOA and f_T. In the past all you could expect was about 1 MHz f_T with a 100 V, 1 A SOA. Now our MJ15022/23 family offers unprecedented 4 MHz response at this power level.

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Design them into your new audio systems. See your authorized Motorola distributor, or contact Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036 for your data sheets and free Power Leader Selector Guide. And, for our new Power Data Book . . . just $5.00. Get SuperPower sonics for your

Innovative systems through silicon.

MOTOROLA INC.

Echo-canceling chip opens way to increased use of satellite channels

by Harvey J. Hindin, Communications & Microwave Editor

Bell Labs' n-channel MOS chip, in production at Western Electric, will be installed in fourth quarter

By the end of the year, telephone communications via satellite will begin undergoing a drastic technical change. The voice-garbling echoes that occur over the 45,000-mile-long paths will be eliminated by an n-channel MOS chip developed by Bell Laboratories, and already in full production at Western Electric, the Bell System's manufacturing arm. By the fourth quarter, the relatively cheap chip will start being installed in Bell's digital switches that feed the satellite ground stations.

The development of the digital echo-canceling chip could by itself double the number of satellite circuits now being used by American Telephone & Telegraph Corp. in its telephone network. (AT&T uses 5,500 circuits out of 36,000 available in three Comstar satellites.) This is because of the way the phone company now deals with the echo problem. So severe is the garbling that transcontinental telephone calls are not sent by satellite both ways.

Rather, AT&T uses what it calls composite circuits: one end of the conversation goes by satellite, the other end via ground links. The echoes would be far too severe if the complete conversation went via the long satellite path; echoes are not as severe via the shorter ground path.

The new chip could also be used on standard terrestrial links. It could replace old-fashioned echo suppressors which break the echo path by effectively opening the transmission line when the echo's amplitude becomes too high. Another candidate for replacement is the method which adds attenuation to reduce the amplitude of the echo. The circuitry for implementing this method is expensive.

But perhaps even more important than its echo-canceling properties is the implication for the future of all-digital satellite links. (Right now, the links to the satellite are analog, rather than digital.) Digital technology will enable system designers to apply the benefits of large-scale integration to their circuits, as well as the myriad possibilities inherent in digital stored-program control. The ability to cancel echoes in such systems inexpensively is likely to encourage their introduction.

Few details. At this point, Bell engineers are not ready to release the technical details of their MOS chip. The chip is the work of engineer Don Duttweiler of the digital techniques section at Bell in Murray Hill, N. J. He did everything from the original MOS design through its computer simulation and final test. The chip includes about 35,000 transistors, which puts it in the LSI class. It dissipates about 0.75 watt and operates from a 5-volt power supply. It is a stand-alone device, doing its job without the help of a microprocessor or peripheral memory.

Bob Aaron, the head of Duttweiler's section describes how the chip works as a voice signal, converted to digital at the satellite receiving terminal, is received through Bell's ESS-4 digital switch.

"It looks at the digital speech signal and then compares the actual echo with an estimate of the echo signal that it generates. As a result, it generates what amounts to an error signal.

"The chip then adapts and gets an even better estimate of what the actual echo is and this is repeated many times. Then the chip takes the replica of the echo that it has generated and subtracts it from the real echo while not disturbing the normal speech transmission."

Two of these chips—one at each

Crammed full. Engineer Don Duttweiler holds the echo-canceling chip he designed that does the job of the seven printed-circuit boards on the table that cost much more. That's Bob Aaron, head of Duttweiler's design group at Bell Labs, in background.

The problem of echoes

The echo problem was recognized back in the 1960s when satellite telephony began. Echoes occur in all telephone networks. They stem from signal reflections at network connection points. Most often, this occurs where the standard four-wire lines used for long-distance connections are connected to the local two-wire lines via transformers called hybrids. These hybrids cause slight but unavoidable electrical impedance differences that result in signal reflections that are perceived as echoes.

For calls over a distance of up to about 1,800 miles, echoes are handled by purposely introducing loss in the network to keep the echo amplitude down to acceptable levels. Over more than 1,800 miles, echoes are controlled in terrestrial lines by devices called suppressors, which are activated by the speaker's voice and stop the echoes by interrupting their path of travel. However, sometimes this causes bits of the conversation to be clipped off. This happens, for example, when one speaker interrupts the other.

This clipping is not very pleasant and research had been going on to find a better way to suppress echoes—especially for the long distances of satellite circuits. By the mid-1970s these efforts had borne fruit but the echo cancelers that became available were small electronic systems in themselves, used valuable power, and were expensive. In fact, they were so cumbersome that they are not really being considered as a viable solution to the problem.

For example, the voice common carrier, Comsat Laboratories, has experimented with a piece of analog gear designed to cancel echoes. It is made up of several circuit boards that consume about 20 watts. It is under test in Canada and not in operational use. **H.J.H.**

end of the long haul four-wire line—can provide for full two-way echo-free communications. What is more, the estimating and correction process does not result in any noticeable additional delay in transmission because the chip does the job in milliseconds. The 0.3 second it takes to make a 45,000-mile trip to the satellite and back to earth remains, but this is too small to be a factor in a conversation.

Research

National Research Council calls for university R&D in electronic materials

U. S. world leadership in microelectronic devices may be jeopardized unless more university centers are established for high-risk research on the microstructure of materials and for training more engineers and scientists in this work.

That is the judgment of a National Research Council panel. Its recommendation: establish new regional centers along the lines of Cornell University's Submicron Facility to do research in such areas as the very large-scale integration of electronic and magnetic devices, the submicrometer lithography necessary to produce the patterns for such circuits, and exploratory fabrication of the circuits themselves. The limited research efforts at universities now, says the NRC report, show a "disappointing tendency to emulate industrial efforts, rather than to explore in new, high-risk directions."

Citing microstructure R&D programs in other countries, notably Japan, the NRC study says U. S. university researchers "should not concentrate on just the problems of extrapolation of current technology; industry expects to solve those problems. They should rather anticipate the needs of at least 10 to 20 years ahead, especially studying the inherent device physics."

The NRC panel, chaired by the University of Miami's Norman G. Einspruch, was made up largely of people from universities and from the semiconductor and computer industries. Their 305-page report, which assesses current U. S. semiconductor electronics, is titled "Microstructure Science, Engineering, and Technology," and is available from the Solid State Sciences Committee of the council at the National Academy of Sciences in Washington, D. C.

Limits. While memory chips are now pushing toward 1 million bits of storage in a complex circuit with structural features less than a micrometer wide, the panel believes that such achievements are approaching the "fundamental limits of available materials." Submicrometer circuit dimensions, the panel points out, fall "within a range for which there is a peculiar gap in the understanding of condensed matter—solids, liquids, and amorphous substances—since one is not able with confidence to extrapolate upward from the atomic scale nor downward from bulk solid-state."

For instance, there are problems with identification of both natural and implanted material impurities in very small circuits. Also, the chemical and electronic effects at edges, surfaces, and interfaces of thin films are poorly understood.

Accordingly, the panel's report spells out national research needs in microstructure science and engineering. To improve the fabrication of microelectronic devices it calls for more research in the formation and etching of thin films; on the interactions of electrons, photons, and ions with materials; and on improved instrumentation for analysis of very small devices. The panel also calls for greater collaboration between university and semiconductor industry laboratories, as well as an increase in programs of nonproprietary research and development on the part of industry.

"Our main conclusion," the panel

says, "is that a high level of long-range research activity closely related to integrated-circuit technology is essential" to continuing national success. **-Ray Connolly**

Automotive

Ford dashes get electronic look

Detroit automakers will be battling in a new arena this fall, this one defined by the dashboard features they can offer using solid-state electronics. The result—as evident from the instrument cluster to be introduced by Ford Motor Co. in its top-of-the-line Lincoln Continentals—will be an entirely new look. Not only will displays new to the automobile be used, but they will also present information that has never before been offered to the driver.

Ford calls its array of electronic goodies a message center. It flashes messages regarding the auto's performance on two lines of a greenish-blue 20-character alphanumeric vacuum fluorescent display. The center also cycles through a checkout procedure that determines whether 11 systems, such as lights, oil pressure, engine temperature, and alternator, are within their operating limits. And it has a chronographic function to keep track of the month, day, and time.

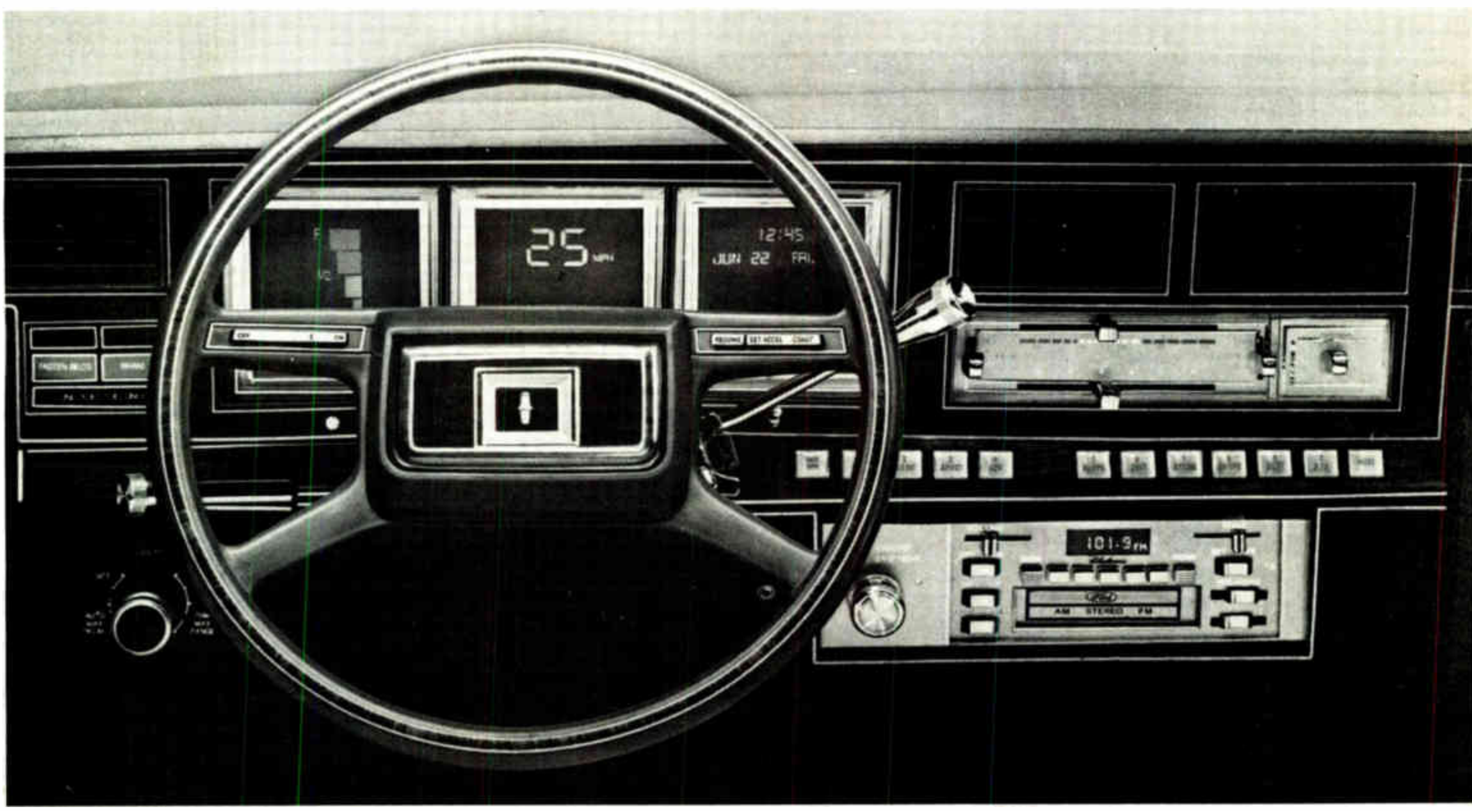
Actually, the instrument panel uses a trio of vacuum fluorescent displays, as shown in the photo below. The familiar fuel gage needle has been replaced by an analog bar chart that shows remaining fuel as a proportion of gas tank capacity. And the conventional speedometer has been replaced by 0.8-inch-high numbers that indicate speed in kilometers or miles per hour.

Space limits. The electronic bells and whistles do not come cheap. Detroit engineers note that the cost of the all-electronic cluster is about five times that of its electromechanical counterpart. But limited space behind the instrument panel of the downsized autos of the 1980s force the consolidation of numerous discrete gages into a compact display. Also, explains one engineer, since cars already have an array of new sensors dictated by fuel economy and emissions regulations, it is relatively easy to recycle the data as input for an instrument display. Of course, "electronics will be used to give us a marketing edge," he adds.

Larry Lopez, manager for electronic instrumentation and features engineering at Ford's Electrical and Electronics division, Dearborn, Mich., explains that two microprocessors and a programmable logic array are part of a package that uses 23 integrated circuits to drive the new cluster. The fuel gage is driven by an American Microsystems S2000A microprocessor plus an analog-to-digital chip that converts the fuel level sensor's electrical resistance into a digital equivalent.

The speedometer is driven by a programmable logic array from In-

Message center. Electronic instrument panel uses trio of vacuum fluorescent displays. Fuel gage is at left, speedometer (with electromechanical odometer not visible) at center. Derived information such as distance to destination is called up via row of push-buttons to show up on two-line display, right.



terdesign, while the message center for system checkout and timing has a Motorola 6800 with a 64-K read-only memory that stores 77 words, such as the days of the week and the months of the year. If fuel supply or system operating conditions drop below safe levels, an automatic visual and audible warning is produced by the message center.

The Ford unit, which also performs trip log calculations such as estimated time of arrival and distance to empty, comes 18 months after General Motors' Cadillac division first offered a trip computer using a gas-discharge numeric readout as an $1000 option for its Seville [*Electronics*, March 2, 1978, p. 40]. Buick will offer it this year for about $800. Cadillac has dropped that unit for its 1980 models, but a spokesman says that it will be replaced by a more advanced package this fall. As for the price of the Ford panel, the company will say only that it will be less than for General Motors' trip computer. **-Larry Marion**

Bubble memories

Bell Laboratories shows off chip with a capacity of 11.5 megabits

The record for the largest-capacity bubble-memory chip belongs to two researchers, Terry Nelson and Raymond Wolfe, at Bell Laboratories, Murray Hill, N. J. Their experimental chip, using the dense so-called contiguous-disk approach, could theoretically store 11,542,272 bits—roughly 11.5 megabits—and measures a hefty 28 by 30 millimeters, or more than 1 inch on a side. The chip was described by Nelson of Bell's magnetics department at the Second Joint Intermag-Magnetism and Magnetic Materials Conference held last month in New York. It contains the read and write elements required of a fully functional memory. These include generators, read-write lines, and a detector.

Contiguous disks are a relatively new way to pack large numbers of bubbles into a chip of magnetic garnet. Dense chips are possible because the technique permits no gaps in the propagating pattern needed to move bubbles around the chip for reading and writing. Current conventional patterns are chevron-shaped; on contiguous-disk devices the pattern resembles overlapping circles or disks.

By comparison with the new Bell chip, the largest bubble memories in production use the chevron patterns and contain roughly 1 megabit of storage. The possibility of fabricating a chip with as much memory as Bell's indicates that the future of the memories may lie with contiguous disks rather than the conventional kind.

Minimum features. The 11.5 megabit chip, which has 1,792 minor loops with 6,441 bits each, has an eight-micrometer period—the size of the propagating pattern before it begins to repeat itself—and was made with minimum features of 2

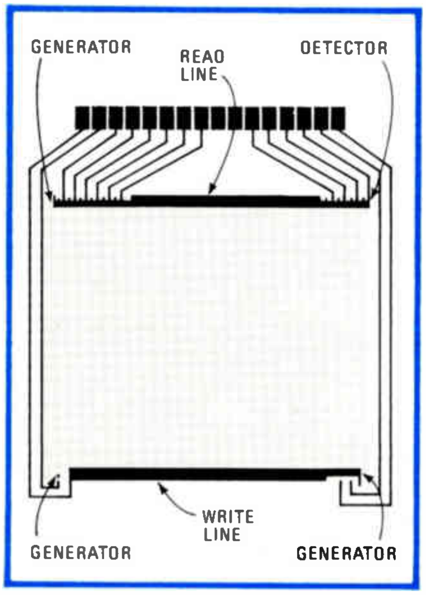
Memory disk doesn't spin

BASF Aktiengesellschaft, Rhein, West Germany, has taken an older memory technology and given it a modern twist. The technology first surfaced in the early 1960s before magnetic bubbles were discovered. Like bubbles, it relies on magnetic domains. But these domains are stored in metallic layers, rather than in the bubbles' garnet, and the domain shapes are flat, rather than cylindrical. At the New York magnetism conference, BASF described the memory approach applied to a flat magnetic disk that is perhaps the first removable, nonvolatile magnetic memory with no moving parts.

To make the 0.2-in. thick module, a thin iron-nickel-cobalt layer with circular magnetic anisotrophy is vacuum-deposited onto a 2-by-2-in. glass substrate and subsequently etched into four long parallel spirals. All magnetic fields necessary for domain nucleation, propagation, and inductive sensing are generated by a copper conductor pattern on a Mylar layer. The metallic and conductor layers are registered and attached to a 3-by-3-in. printed circuit board that has 32 edge connectors. The ensemble is finally potted in a square-shaped epoxy resin.

Each spiral acts as a 12,288-bit shift register, so the system has a total capacity of 49,152 bits. Data can be written at any rate up to 125 kilobits/sec, and the maximum access time at this rate is 98.3 milliseconds. At the maximum data rate, 500 kilobits/sec, the device consumes 17.3 watts. Thus, the module is not terribly fast nor power sparing.

It does, however, offer "low cost per function," according to Herbert Henkler, co-author of BASF's paper. "The whole feature, along with the electronics necessary for control, driving, and sensing, will be [available] in the $100-to-$150 range," he says.



Disk fever. Drawing shows layout of ion-implanted contiguous disks that guide magnetic bubbles through the 1 in.²-plus garnet chip developed at Bell Laboratories.

mm. Because of the chevron pattern, a conventional chip would need 1 μm minimum features to yield an 8-μm period. This feature size approaches the state of the art for optical lithography. Contiguous disk chips made with such resolution could be at least four times as dense as conventional chips.

Bell defines the contiguous disks by implanting helium and neon ions in the garnet substrate in which the bubbles reside. IBM, which has in the past championed a bubble-lattice structure for achieving higher densities, is also working with contiguous disks using ion implantation to fabricate them. But it first grows an extra garnet layer to receive the ions [*Electronics*, July 19, p. 39]. According to Emerson Pugh, manager of exploratory magnetics at IBM's Thomas J. Watson Research Center, Yorktown Heights, N. Y., "We are seeing ten times the density [of conventional designs]."

Not the same. Unlike semiconductor doping where impurities are introduced in precise quantities to alter conductivity, bubble implants are intended solely to impart damage to the crystal lattice. This forces short magnetic vectors to act along the cusps and curves of the disks, attracting bubbles and pulling them along under the influence of a rotating magnetic field provided by criss-crossed coils of wire. To get workable operating margins on the Bell device, only 1,350 of the 1,792 loops were used, "which works out to 8.7 megabits," says Nelson. This number is "significant, being slightly over one megabyte," he adds. The next step for Bell is to try to use the implants at shorter periods—ultimately producing periods of 4 μm, for four times the present chip's density.

However, it should be noted that ion implantation is not the only way to make contiguous disks. Two other papers at the conference, one from IBM's Watson Research Center and one from Rockwell International's Electronics Research Center in Anaheim, Calif., both described devices with two levels of complementary-permalloy contiguous patterns. In past attempts using a single permalloy layer, bubbles had problems getting by the cusps of the disks. To avoid these problems, when the bubble nears the cusp, one layer is shut off and the other activated. Though showing potential, "both papers presented only preliminary results," says Pugh. "They showed simple propagation, but they didn't have switches, nucleators, or sensing." **-John G. Posa**

Management

RCA Solid State adds the dash of Pepper

On Aug. 6, Robert S. Pepper, 44, will become general manager of the Solid State division of RCA Corp., Somerville, N. J. Like every job of his professional career, the position was unsought; Pepper was recruited while vice president of Analog Devices Inc. and general manager of its Semiconductor division in Wilmington, Mass.

Pepper takes over divisional responsibility for an organization grossing about three times as much as his old employer. But he is not

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worried: "I have had no second thoughts. I simply do not plan to fail—I hate to lose. I expect to have a steady pair of hands when I walk into the office on the sixth."

That's probably how it will be. Pepper is no stranger to the pressure of fast tracks, either the corporate or racing variety. A fierce business and sports competitor, he used to enter motorcycle races without the factory backing that other racers enjoyed. "A lot of the time I beat those guys," he says, and he has a room full of trophies to prove it. After a serious accident made him stop racing, he helped prepare the machine that now holds the motorcycle land-speed record. Pepper's Hall-effect electronic ignition was the cycle's only part that gave no trouble.

Pepper looks forward to the challenge of the RCA job. "The Solid State division is the only IC maker I used to play war games with in my mind," he says. "I tried to place myself in its management's shoes in a way I never did with firms like Intel. I guess it was because I have always been impressed by the division's capabilities and with the work done at RCA's Princeton [research] laboratories. I see no reason why the division can't contribute far more to RCA. I have been assured by [RCA executive vice president Roy H.] Pollock and [RCA president Edgar H.] Griffiths that money and backing will be there if needed. You can forget any doubts you may have had about the division's future within the corporation."

Past achievement. RCA was no doubt impressed with Pepper's track record. Since he obtained his doctorate in electrical engineering in 1964, his fortunes have risen steadily. He agreed to a year's leave of absence from his appointment to the faculty at the University of California, Berkeley, to set up a linear IC facility for the Sprague Electric Co., North Adams, Mass. The one-year leave stretched into an 11-year full-time job as Pepper was promoted to become technical assistant to the chairman of the board.

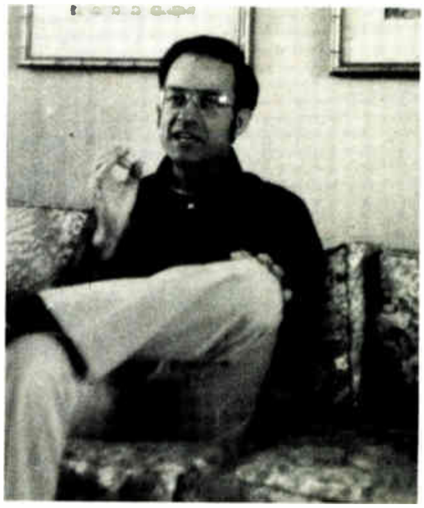
Insiders say Pepper made it possible for Sprague to enter the integrated-circuit business, citing a list of its achievements in that area—the development of the first practical IC television sound channel, the first successful high-voltage power ICs, and the first practical application of ion implantation, among others.

He left Sprague in 1975 for Raytheon Co.'s Missile Systems division, Bedford, Mass., where, he says, "I learned the systems engineers' side of the problem—they want circuits that fit their block diagrams, not lectures about sophisticated technology."

In April 1976, he moved to Analog Devices as director of R&D and four months later became general manager of the Semiconductor division. In less than 18 months, he was named a corporate vice president. Making the announcement, Ray Stata, Analog's president, noted that under Pepper the division's sales had grown by 50% in the prior 12 months and that profits had reached record highs. Analog insiders say that this compounded yearly growth rate will be a major factor in Analog's achievement of $100 million in gross receipts a full year ahead of expectations.

Pepper downplays the praise, stressing that he wanted to streamline new product introductions and to give the division greater focus in

Well-regarded. General manager Robert S. Pepper looks for the division he is taking over to be making long strides in the right direction within the next two years.



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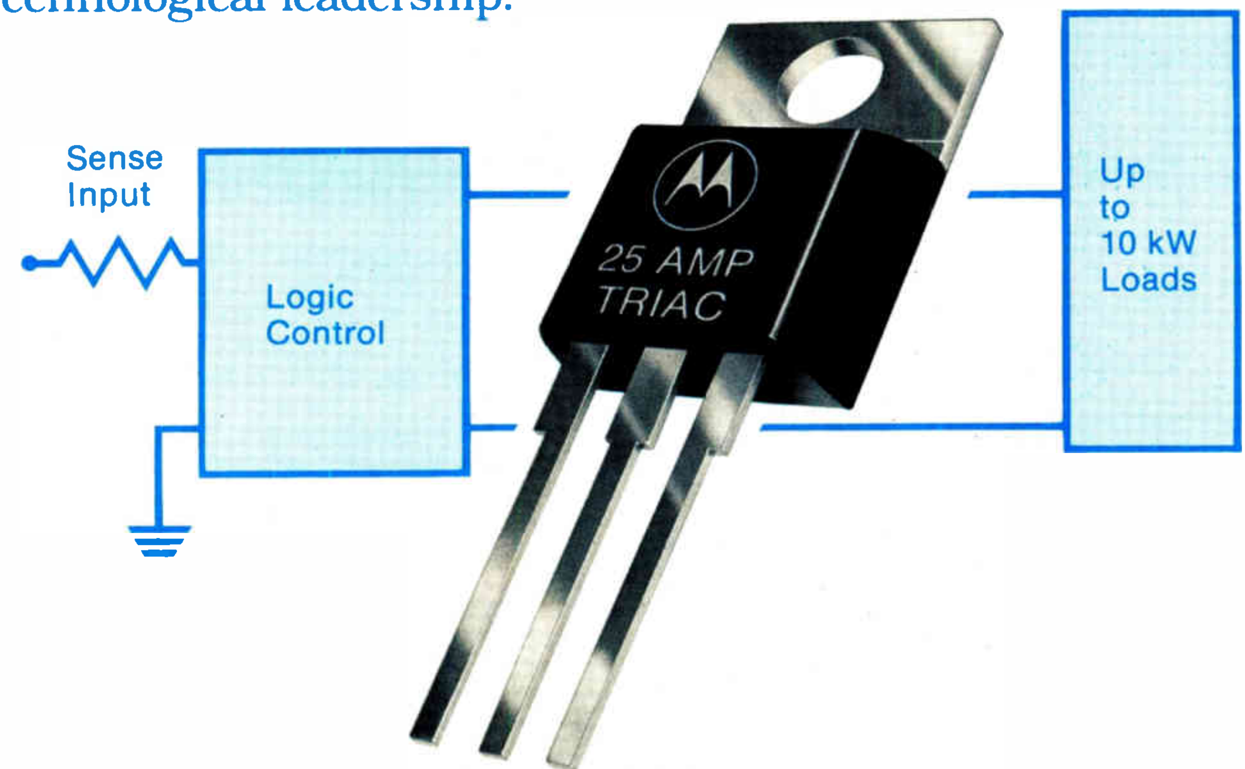

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key markets. Perhaps most importantly, though, he "emphasized pragmatic engineering solutions rather than the existing science-oriented approach to design."

Associates say that "he trims fat, admits mistakes, solicits ideas, puts the right people in the right jobs, gives 200% of himself, and gets at least 150% from those around him—and meanwhile, everybody has one hell of a good time."

An acquaintance from his days at Sprague says that Pepper "respects people who admit mistakes, but God help you if you try to cover one up and he finds out."

RCA Solid State, bigger than either Sprague or Analog's IC operations, should have more inertia. "I don't see massive changes in the next six months," Pepper says, "but in the next two years, I expect the division to be making long strides in the right directions." **-James B. Brinton**

Satellites

AT&T has chance at new services

The people at American Telephone & Telegraph Co. should be happy about the Federal Communications Commission's July 18 decision—or really, nondecision—to let a moratorium expire on the leasing of channels on the Comstar domestic satellites to non-government private-line users. This means that AT&T is now free to offer services it had been barred from providing specifically via satellite. These include cable television and various point-to-point and multipoint distribution services.

Competition. When it adopted its satellite policies in the early 1970s, the FCC prohibited AT&T from selling these services so as to enable

News briefs

Hand-held calculator accesses peripherals

Hewlett-Packard Co.'s new HP-41C hand-held calculator [*Electronics*, July 19, p. 33] turns out to be an exceptionally powerful system: the $295 unit can be connected through its four ports to such peripherals as a thermal printer, a magnetic card reader, an optical character-reading wand, and a memory. It can execute 130 preprogrammed functions and will accept plug-in application software supplied by the Palo Alto, Calif., company or written by users.

Up to four random-access-memory modules ($45 each) can be plugged in to store as many as 2,000 lines of data, equivalent to 319 registers. HP developed the peripherals especially for the calculator. The card reader costs $195; the thermal printer, $350. The wand, available early next year, will read standard bar code. The Corvallis, Ore., division of HP's Calculator Products group developed and builds the HP-41C, as well as the 11 complementary-MOS chips around which it is designed.

Northern Telecom to add more acquisitions

Though it has spent $276 million in cash and stock to acquire four makers of data-processing and telecommunications gear in the United States last year, Canada's Northern Telecom Ltd. is still not through. More acquisitions are planned, perhaps including a software developer along with more hardware vendors. Several new distributed data processing products are coming from a subsidiary, Northern Telecom Systems Corp. of suburban Minneapolis. This fall, it will follow up with hardware and software for word processing, joining the bandwagon of manufacturers of distributed data-processing equipment.

Adding word processing to their product lines [*Electronics*, July 19, p. 81], Northern Telecom Systems' salesmen are also packaging "Office of the Future" proposals using telecommunications gear from a sister corporation, Northern Telecom Inc., of Nashville, Tenn. Company sources, however, say a merger of the two subsidiaries of Northern Telecom is not imminent and that the joint sales efforts are part of an experiment to see how the two companies work together in the marketplace.

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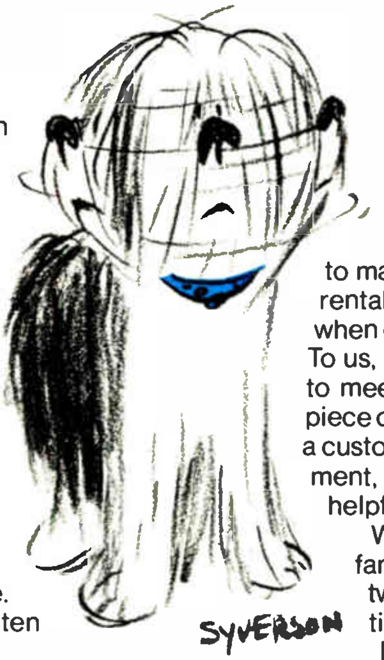

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Test and Measurement Instruments

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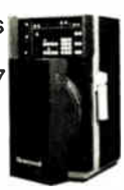
Biomation K 100 D Logic Analyzer. 16 channels; 1024 word memory; clock rates up to 100 MHz; signal timing resolution to 10ns; built-in display and keyboard control.



Honeywell 101 Recording System. 7 or 14 tracks depending on head assembly; ½ in. (7 tracks) or 1 in. (14 tracks) tape; 8 tape speeds from 0.937 ips to 120 ips; direct bandwidth to 2 MHz (wide band) and to 600 kHz (intermediate band); FM bandwidth to 80 kHz (wide band) and to 40 kHz (intermediate band); reel size 10½ to 15 in., coaxially mounted.

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competition to get started and grow. Thus the Bell System has been using Comstar—a satellite launched jointly by AT&T and General Telephone and Electronics Corp.—only for long-distance phone calls. (See related story on p. 41.)

Companies who filed objections with the FCC to letting AT&T in on the private-line action included RCA, Western Union, American Satellite, Xerox, and Satellite Business Systems. The last two are still getting organized to provide service. They feared competition from AT&T and voiced the oft-expressed worry that it would subsidize the new services from other revenues.

The ball is now very decidedly in AT&T's court. It says it is still deciding whether even to file tariffs describing any additional services it might offer. However, it could go into business almost overnight. Three Comstar satellites in orbit have 85% of their capacity unused.

The IBM-backed Satellite Business Systems may be most affected by what AT&T does. It will have no satellites in place before 1981, and potential customers may look to AT&T instead of the newcomer. However, competition may lead to cheaper, more innovative services.

As for the others, RCA and Western Union say their channels are fully booked, and so are new craft to be launched in 1980. American Satellite rents channels; so will Xerox. **-H. J. Hindin, R. Connolly**

Integrated circuits

Bipolar TRW chip has 1-μm line widths

Late in July, researchers at TRW Inc. completed an experimental test chip, employing bipolar semiconductor technology, that has minimum line widths of 1 micrometer. "It might be the first very large-scale integrated bipolar device," says Barry Dunbridge, manager of the TRW Microelectronic Center in Redondo Beach, Calif., where the work was done. Moreover, it comes at a time when a

TRW-led team is in the midst of putting together its proposal for the Department of Defense's very high-speed integrated circuits (VHSIC) program.

The fabrication of other test chips in the 1-μm range has been reported in semiconductor industry circles, but these chips use MOS technology. Dunbridge says, "I know of no other bipolar examples." Firms that have bipolar capabilities at this level include IBM Corp., Bell Laboratories, and Texas Instruments, he points out.

Bidding. All four firms are taking part in VHSIC bidding, Bell through its Western Electric equipment-making subsidiary. With phase 1A of VHSIC calling for construction of brassboard electronic subsystems with devices having 1.25-μm minimum feature size, an early demonstration gives a bidding firm "a nice leg up," says Dunbridge [*Electronics*, Sept. 14, 1978, p. 81].

Along with the small geometries, the request for VHSIC proposals also establishes a new criterion for device performance. It replaces the standard speed-power product with a "gate–clock-frequency product." Circuits with a 1.25-μm minimum linewidth must have an equivalent gate–clock-frequency product exceeding 5×10^{11} gate-hertz per square centimeter.

This assumes a maximum power dissipation of about 3 watts/cm^2 and a minimum clock speed of 25 megahertz. The inherently faster bipolar approach to fabricating circuits could have advantages over MOS in reaching these goals.

The TRW test chip is about 270 mils on a side, and has 10,000 1-μm gates, clustered on a small part of the chip. The connecting pads are 4 mils square and 8 mils apart, center to center.

The TRW researchers made their device with conventional photolithographic production equipment, but Dunbridge thinks the 1-μm level is its limit. He is convinced that direct writing electron-beam techniques are the answer to pushing down to submicrometer ranges, based on studies to date. *-Larry Waller*

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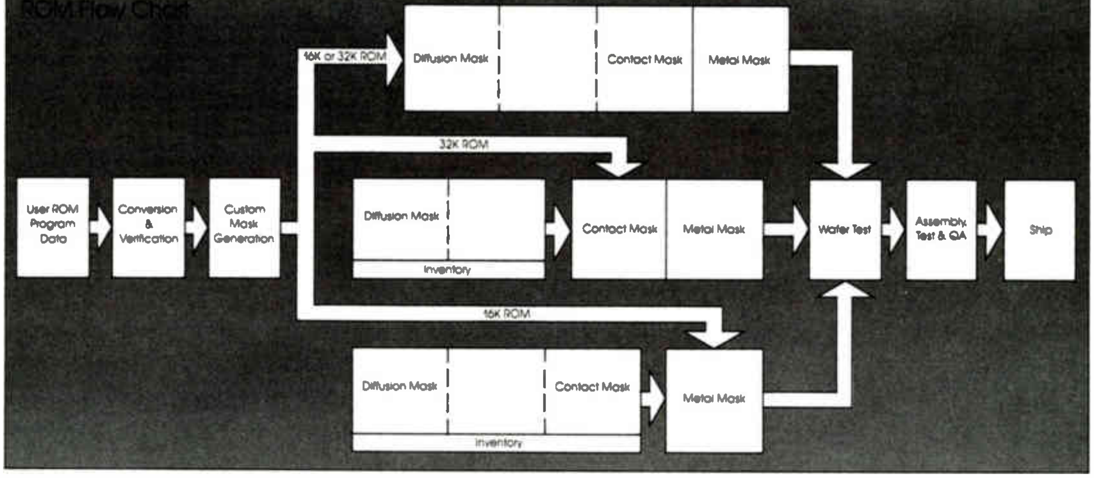

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Washington newsletter

Congress to toughen weak Carter plan to revamp trade

Watch for the Senate Governmental Affairs committee to make "its own meaningful reorganization" of U. S. foreign trade administration with relatively little regard to President Carter's proposal last month. That was made clear when the White House plan's chief sponsor, Ambassador Robert S. Strauss of the Office of the Special Trade Representative, **conceded to chairman Abraham Ribicoff (D., Conn.) in hearings that the Carter plan "is flawed."**

The Carter plan calls for the special trade office to become the office of the U. S. Trade Representative, with Cabinet rank and trade policy and negotiating responsibility acquired from the State Department, while the Commerce Department would be renamed the Department of Trade and Commerce, with an additional undersecretary for trade, along with a 300-person staff now in the Treasury Department to enforce antidumping and countervailing duties statutes.

Senate weighs granting contractors exclusive patent use

Federal research and development policies, which prohibit granting contractors the exclusive commercialization rights to Government-funded inventions, are being reviewed in the Senate, along with the adequacy of Patent Law protection of inventors. Hearings began before the August recess on S. 1215, a bill that would encourage more industrial competition for R&D funds **by granting inventors exclusive rights to commercialization in non-Government markets.**

$39.8 billion outlay for antisub weapons foreseen through '83

Navy antisubmarine warfare (ASW) funding of $39.8 billion over the five fiscal years from 1979 through 1983 will experience steady annual growth during the first three years before dropping in fiscal 1982 and then rising sharply again. That is the estimate of New York market research firm Frost & Sullivan Inc., which forecasts growth over the five-year period for electronic sensors, as well as weapons and targets, countermeasures, and research and exploratory development. **The estimate attributes the 1982 dip in electronics spending to outlays for ASW platforms**—aircraft, submarines, and surface ships, which account for about 60% of the total market—and for command, control, communications, and intelligence technical support and facilities. The five-year market for sensors, including sonar, sonobuoys, and ASW avionics improvements, is pegged at just under $5.5 billion, plus $4.8 billion for weapons and targets, $1 billion for countermeasures, and nearly $2 billion for R&D.

Bigger budget is FCC answer to GAO criticisms

Strong criticism of the Federal Communications Commission's operations and management are set for fall publication by congressional investigators in the General Accounting Office. But the FCC, which already has a draft of the GAO report, is countering the criticism of its weaknesses by drawing up a fiscal 1981 budget request asking for $81 million, about 12% more than it expects to get for fiscal 1980, which begins Oct. 1. FCC officials say **more money is needed for 156 more staffers and other resources to improve its performance in areas criticized by the GAO**, even though the increase runs counter to a White House inflation-fighting directive urging all agencies to hold budgets to existing levels.

The flaw in Carter's ointment for electronic mail

When the White House finally put out the President's policy statement on the U. S. Postal Service's future role in electronic mail, most of the public was too absorbed in the Cabinet purge to notice. But within the House and Senate, Carter's limited endorsement of the service's entry into the business is already being criticized as unrealistic and unworkable; for his plan and some of its more appealing aspects are totally flawed by one of its eight conditions.

The President would have electronic mail pricing subject to regulation by two Federal agencies—the Federal Communications Commission for electronic transmission charges and the Postal Rate Commission for pricing of mail delivery. "My God," exclaimed one Senate committee staffer, "I can't believe it! Having to deal with one [commission] can be bad enough. Two would be impossible. Disputes would inevitably wind up in the courts. The idea is unworkable." Similar exclamations could be heard from almost every corner of the Government, as well as industry.

The good points

That jurisdictional botch more than offset the desirability of the Carter policy's seven other conditions for USPS participation in electronic mail. They would mandate an open and competitive market by refusing extension of the postal service's private express statutes beyond letter mail to cover electronic transmission, as well as require that postal electronic operations be set up as a separate entity to prevent their subsidy by regular mail services or tax money.

Other conditions would require the postal service to: buy transmission services from carriers, rather than build its own network; make its delivery services available to all carriers at the same rates it charges itself; and ensure that interconnection with the mail delivery system be available to all companies by developing technical interconnection standards through a cooperative effort with the American National Standards Institute, the private carriers, and an impartial arbiter, if needed.

Postmaster General William Bolger says he is pleased with the Carter policy, calling it fair to both the postal and private sectors. He also sought to soothe continuing industry concern by noting that "no one should jump to the conclusion that an electronic mail system of any large scale is just around the corner. It is not, because it remains to be seen how ready the public is to accept and use such a system." The postal service will proceed with caution, Bolger adds.

The added fact that the service would be precluded from ever developing an end-to-end message system with electronic display and optional hard-copy printouts at the recipient's home or office provides little solace to potential privately owned competitors. "Limiting the postal service to physical delivery of hard copy like facsimiles still gives it a distinct advantage. It starts out with 40,000 post offices that could be converted into message terminals," notes one electronic message service competitor.

Opposition on the Hill

The Carter policy's proposal to divide jurisdiction over electronic mail between the FCC and the PRC and then see how that works for five years is providing congressional opponents to USPS market entry with a ready-made reason for rewriting the plan altogether. And the opposition has some legislative heavyweights on its team. Among them are South Carolina's Ernest F. Hollings, chairman of the Senate communications subcommittee; Nevada's Howard W. Cannon, Chairman of the parent Commerce Committee; and the first- and second-ranking minority members of the Hollings subcommittee, Arizona's Barry Goldwater and New Mexico's Harrison H. Schmitt, a former astronaut. All four have written to the President to the effect that the postal service should leave electronic communications to the private sector to develop, and Hollings and Schmitt are moving to bar postal service appropriations altogether if it "develops or procures its own electronic message system."

The White House view is that the U. S. Postal Service's use of electronic communications to speed transmission and printout of messages and physical delivery would improve both productivity and efficiency in providing nationwide coverage in 1985 and beyond. Moreover, it points to Carter's mandated conditions as protecting the interests of private competitors.

Some sort of electronic message service statute will emerge eventually, of course, but it may bear little resemblance to President Carter's plan because of the plan's faulty jurisdictional proposal. That is regrettable, for the plan has more good points than bad ones. Yet the White House seems to be losing the initiative on this issue already, now that President Carter has let his staff do the spadework for Congress and dig a legislative grave for another of his proposals. **-Ray Connolly**

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NEC Newscope

ASTRA Computers Introduced To N. American Market

NEC and NEC Information Systems, Inc., an NEC subsidiary in Lexington, Mass., recently introduced a series of powerful small business computers in the North American market.

The new ASTRA (trade mark) series makes extensive use of NEC-developed processors, circuitry and systems architecture to provide extraordinary power in the four compatible systems – Models 210, 230, 250 and 270.

The systems accommodate from one to 32 operator stations. Each can operate at peak efficiency in a transaction processing mode because of the unique NEC technology embodied in the products.

The ASTRA series has three important features that ensure its high-performance capabilities. One is a new 16-bit microprocessor, with a set of 114 business EDP-oriented instructions, which is two to three times more powerful than the most popular 16-bit microcomputers in use today. The second is a DMA controller channel that permits data transfer between an operator station and the central processor at a data rate of one million bits per second. The third is an LSI and microprocessor-based integral disk controller with a data transfer rate of 1.2 megabytes.

Supporting the new hardware is a complete structure of programming languages, operating systems and application packages. Advanced "BASIC" and ANSI 74 COBOL compilers are available with each model. An executive system which supports multi-user, multi-job environment is provided. Also available is an advanced data management system that supports formatted data entry and update, file management, report generation and English-language inquiry functions.

Plus integrated application software systems that simplify initial user start-up operations. These include sales order processing, sales analysis, inventory control, accounts receivable, accounts payable, general ledger and payroll packages.

Circle 61 on reader service card

Fiber Optics System Commissioned In Brazil

The NEC-equipped optical fiber cable communications system has been successfully commissioned for telephone use in Brazil.

The fiber optics system, commissioned by Companhia Estadual de Telefones (CETEL), links its two telephone offices over a distance of 5 - kilometers in Rio de Janeiro. It can transmit information at a bit rate of 34 megabits, or provide 480 telephone circuits.

CETEL's system is the second such installation provided by NEC outside Japan, the first being the 45 megabit system engineered for Vista-Florida Telephone System in Walt Disney World, Florida.

Circle 60 on reader service card

ISSCC Award

Three NEC engineers won the 1978 best paper award for their paper "A High-speed 1600-Gate Bipolar LSI Processor" which was co-authored by three engineers of Nippon Telegraph and Telephone Public Corporation (NTT). The award was presented to the six Japanese engineers at the official opening ceremony of the 1979 ISSCC in Philadelphia earlier this year.

The three NEC engineers winning the award are Kodo Kimura, Toshio Nakamura and Toru Takahashi of IC Design Engineering Department, IC Division.

The award winning paper described a high speed 8 bit slice processor fabricated by a new advanced bipolar process technique named the PSA (poly-silicon self-aligned) combined with three-layer metallization and 120 pin gang local bonding, affording large integration (1,600 gates), low power dissipation (1.5 watts) and high speed operation. By using the LSI chip, byte data can be handled within 40 nanoseconds in the read-modifying-write mode.

Iraq Irrigation Control System Contract For NEC

Iraqi Government has awarded NEC a contract for the design, manufacture and installation of a telecontrol and supervisory system for agricultural irrigation.

The irrigation telecontrol and telemetering system will incorporate NEC's most sophisticated computer and communications technology as well as its control know-how. It will have more than 20 remote stations to monitor water level in the canal at 80 locations and remotely control water gates and pumps. The data monitored at these check points will be sent over radio links to the central control station which, in turn, will control the water gates and the pumps.

The computer-controlled system will be powered partly with solar cells to operate telecontrol and telemetering equipment so as to economize on the cost of power supply and to permit easy maintenance.

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NEC At INTELCOM 79

NEC, as one of the largest exhibitors at INTELCOM 79 (International Telecommunications Exposition) held in Dallas, Texas, received unanimous praise for its entire exhibit from customers and other exhibitors alike.

Of special interest at the NEC booth was the DP-100 Connected Speech Recognition System. It was successfully demonstrated as the world's first commercially available data entry system that recognizes fluid, connected speech.

A new attraction at NEC's booth this year was the Intra-company Electronic Mail System, a highly advanced facsimile system designed for full duplex facsimile communications that is integrated with real-time voice communications.

Another first for NEC at the show was the NEC 45 M/b Fiber Optics Transmission System which uses laser beams to send thousands of calls simultaneously over thin glass fiber cables.

NEC's new digital switching system, NEAX 61 (also called Time Machine), was shown to be an impressive system for the central office market.

DP-100 Connected Speech Recognition System

High-Speed Facsimile Unveiled

NEC recently introduced a high-speed digital facsimile transceiver with new encoding system — the M.H. (Modified Huffmann) system for 1-dimensional coding and the READ (Relative Element Address Designation) encoding system for 2-dimensional coding. The encoding systems are automatically selected depending on the type of distant machine.

NEFAX-6200K high-speed facsimile

The new high-speed facsimile transceiver, NEFAX-6200K, can transmit a standard A4 size document at a rate of 20 to 40 seconds (9,600 BPS, 3.85 lines/mm) or 40 to 80 seconds (4,800 BPS, 3.85 lines/mm). In addition to high-speed transmission, the new facsimile equipment incorporates many man-hour saving and other features. These include multi-page transmission, automatic paper cutting, automatic transmission initiated from receiving side, automatic reception initiated from transmitting side, automatic speed selection, duplicating capability, override communication capability and many others.

Circle 169 on reader service card

NEC

Nippon Electric Co., Ltd.

P.O. Box 1, Takanawa, Tokyo, Japan

Japan's Mitsubishi grows round GaAs wafers

Mitsubishi Metal Corp. claims it is the first company in the world to grow 100-lattice-orientation gallium-arsenide single crystals in semi-insulating grades by the Czochralski method. **The ingot diameter is now 2 inches but will be increased to 3 inches in the near future.** Potential customers have started to receive wafer samples on which to grow epitaxial layers and then fabricate test devices like field-effect transistors and integrated circuits. If the substrates prove suitable, their conventional, circular shape and larger area than the presently available roughly triangular Bridgeman wafers will be a big step toward the mass production of fine-pattern devices. Mitsubishi says that it will initially offer the 2-inch wafers for about $93 each.

Bubbles store instructions for German CNC system

Siemens AG is about to unveil a computerized numerically controlled (CNC) system for machine tools built around a 256-kilobit bubble memory working in conjunction with a 16-bit microprocessor. These devices are part of the Sprint 8T CNC system that the Munich company will introduce at the Third European Machine Tool Exhibition, to be held Oct. 10–18 in Milan, Italy. **The bubble memory is equivalent to some 600 meters of punched tape** and stores the parts-machining programs; the microprocessor performs the necessary calculations and communicates with the system's peripheral devices.

France's LEP builds low-noise and power GaAs MES FETs

Scientists at France's Laboratoires d'Electronique et de Physique Appliquée (LEP) believe they are up with the leaders in gallium-arsenide metalized-semiconductor field-effect-transistor technology. A research arm of RTC-La Radiotechnique Compélec and other French companies in the Philips group, the LEP will have prototypes for both low-noise and power GaAs MES FETs within the next year or so. In low-noise devices, the lab, located outside Paris in Limeil Brévannes, is aiming for **a transistor with 5-dB gain and a low 5-dB noise factor at 20 GHz.** Also, by using vapor-phase epitaxy and putting the aluminum gate on the substrate before the source and drain, it hopes to bring the device's gate length down to 0.3 μm from the present 0.5 μm. In power GaAs MES FETs, the goal is a 5-W transistor delivering 5-dB gain between 6 and 12 GHz. Gold "pillars" will run from the source electrode through the substrate to the underside of the device, replacing overlays.

Fm dipole antenna combines efficiency with small size

Matsushita Electric Industrial Co. has developed a prototype of a high-performance, frequency-modulation-band dipole antenna that could **provide consumers with an efficient indoor antenna.** Distributed loading keeps it small, and varactor tuning optimizes its performance across the band. The dc voltage used for station selection in an fm receiver's varactor tuner is also fed via coaxial cable to the varactor diodes in tuned circuits at the center of the antenna for automatic tracking.

The antenna, which is only about 30% as long as a folded dipole, is built around a 7-by-43-cm printed-circuit board. It consists of two zigzag dipole legs, which resonate somewhat above the fm band, and coil-varactor lumped-loading circuits, which bring down the resonant frequency to that of the station to which the receiver is tuned. Matsushita also contemplates making another model with a built-in power supply and tuning knob.

International newsletter

Toshiba flat-panel LED display glows red, orange, green

Toshiba Corp. has announced Japan's first multicolor light-emitting-diode flat-panel display, a matrix of 64 by 64 picture elements that measures 81 by 81 mm. Each element consists of adjacent red and green gallium-phosphide LEDs and can emit red, green, or orange light. Diode drive voltage is 2 V from a single 5-V supply. Brightness is 90 ft-L: **the relatively high efficiency of 3% to 4% for the red diodes and 0.3% and 0.4% for the green ones eliminates any need for reflectors,** say Toshiba engineers. Since the color of each dot can be controlled independently, the display can handle both alphanumeric and graphic data, including bar graphs. Applications in microprocessor systems as well as industrial controls are foreseen. The firm expects to have samples available next year for $470. Somewhat earlier and for a much lower price, it plans to introduce matrixes 100 elements high by several dots wide for such industrial applications as its new one-loop controllers (see p. 72).

Reading machine translates books into braille

Extending their work on optical character recognition, engineers at AEG-Telefunken's research laboratories in Ulm, West Germany, have developed a reading system for the blind that reads the characters in a book and prints them in braille on paper tape. The reader uses some of the same principles as the mail-sorting equipment the company recently installed in a post office for reading typed addresses [*Electronics*, Dec. 21, 1978, p. 60]. A prototype of the reader will be ready this year. By **1981 AEG-Telefunken plans to have ready a system incorporating a speech output device and capable of reading a book aloud.**

NEB survives with wings clipped in a Conservative Britain

Britain's National Enterprise Board has been granted a stay of execution by the new Conservative government and will retain a role in encouraging high-technology projects—particularly computer software and microelectronics and its applications—as well as supporting the growth of small companies. But **its activities will be restricted by a requirement to make investments in partnership with the private sector and most likely by a smaller budget.** It will also have to sell assets worth $200 million by the year-end with stakes in such companies as Ferranti Ltd., ICL Ltd., and Brown Boveri Kent Ltd. as likely candidates. The NEB's commitment to the new microcircuit company, Inmos, continues.

Addenda

Encouraged by the success of its first wafer-fabrication plant in Greenock, Scotland, and by the prospect of a government investment grant of about $26 million, National Semiconductor Corp. of Santa Clara, Calif., is planning a five-year $100 million investment in another plant there. **Eventual overall capacity will be 100 million chips per month,** making the facility one of the largest in Europe. . . . Against heavy international competition, the German ITT subsidiary, Standard Elektrik Lorenz AG, has won **a $250,000 million contract to supply ground-based navigational equipment to air traffic control authorities in Mexico.** The order follows a similar one placed by the Mexicans with SEL last year. . . . The Japanese cabinet has approved an increase of 10.2% in military spending to a total of 2.094 trillion yen for 1979. It includes **construction of a defense microwave communications network.**

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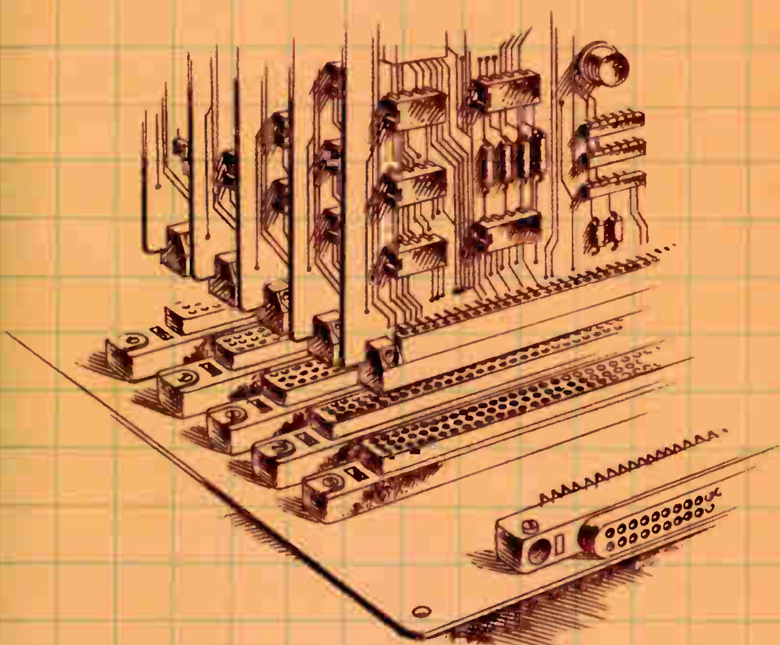

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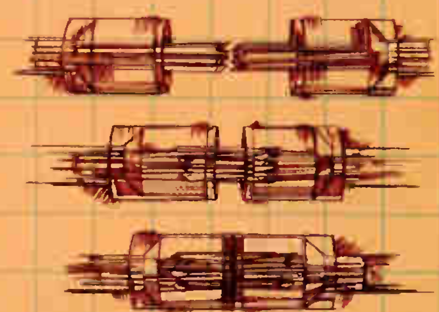

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Electronic system optimizes ignition and fuel injection

by John Gosch, Frankfurt bureau manager

Microcomputer unit provides accurate, constant control of both variables, thereby saving gas

Some top-of-the-line car models slated to come off the production lines at Bayrische Motoren Werke AG (BMW) in Munich this fall will have something new under their hood and dashboard: a digital electronic system that integrates the circuitry for controlling both the fuel injection and the ignition. A development of Robert Bosch GmbH of Stuttgart, the system will "contribute considerably toward fuel economy and a cleaner exhaust."

The heart of the so-called Motronic system is a multichip microcomputer consisting of a Cosmac 1802 microprocessor from RCA's Solid State division; a data and program read-only memory, also from RCA; and an input/output circuit, a joint RCA-Bosch design. These parts are contained in an electronic control unit (see photo) mounted under or near the dashboard.

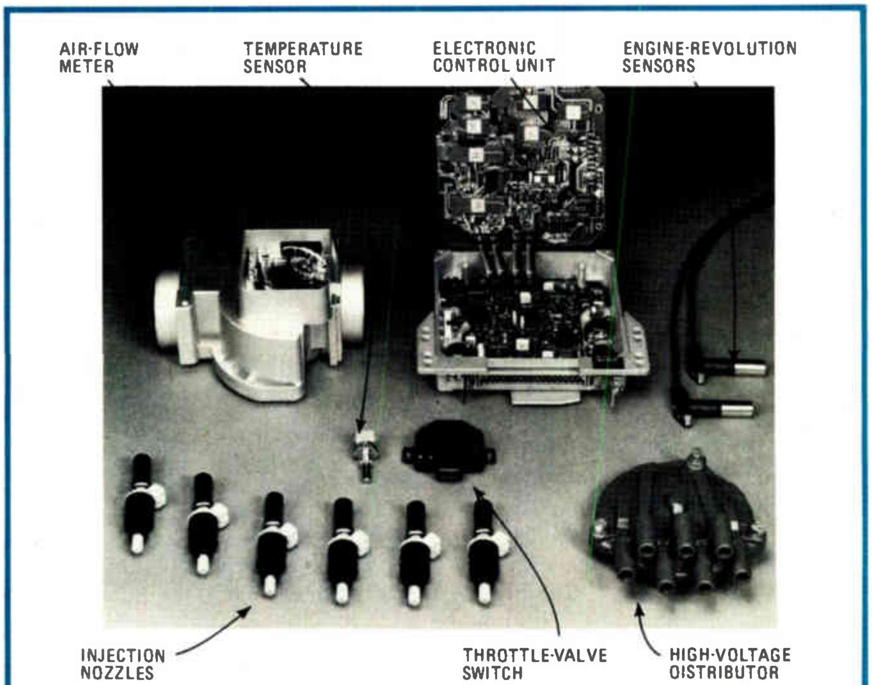
In operation, sensors under the hood pick up information on engine speed, crankshaft position, intake-air flow, and engine and intake-air temperature. Inductive pickups on the engine's flywheel, for example, provide data on engine speed and the crankshaft's position. The amount of intake air is derived from the air flowmeter, and regular temperature sensors determine the engine and air temperature.

The data on engine revolutions and gas pedal position—the latter derived from a switch on the throttle valve—are stored in the microcomputer's memory. Each memory location contains a certain data combination for these two parameters, and each combination in turn corresponds to a particular fuel injection and ignition time.

Deductions. Using the data it thus obtains, the computer calculates the injection and ignition timing and the amount of fuel to be injected for a certain engine revolution value and gas pedal position. It then feeds its outputs in the form of command signals to the transistorized ignition system and to the fuel injection nozzles.

Comparison tests, Bosch says, show a substantial savings in fuel. For example, a Motronic-equipped engine burns up to 5% less gas than the same engine using fuel injection in combination with conventional ignition. The savings is up to 20% for the same engine using a carburetor and conventional ignition. BMW figures that on the average its new 732i models to be fitted with the Motronic system will consume as much as 7% less fuel than its fleet of comparable cars without the system.

Constant control. The prime reason for the greater fuel economy is that the integrated system makes possible highly accurate and stable



Thrifty. Some 1980 BMW cars will come with this integrated electronic system from Robert Bosch GmbH. Dubbed Motronic, it determines the optimum fuel injection and ignition values at least once per engine revolution, thus improving fuel consumption.

control of both injection and ignition. With the combination of sensor outputs representing a particular operating condition like idling or acceleration, the computer constantly determines the optimum, or most economical, amount of fuel to be injected and the optimum ignition and injection timing for a specific condition. Because of its high speed, the computer can go through its calculations and come up with optimum results at least once during each engine revolution.

Quick off the mark. The Motronic system also enhances performance, Bosch says. For example, it facilitates starting the engine in cold weather. Furthermore, right after being started, the engine runs smoothly, responding without jerks to changing gas pedal positions.

The system is said to require virtually no maintenance. The permanently stored data on engine revolutions and gas pedal position in the microcomputer's memory will not change during the engine's lifetime, Bosch points out; neither temperature nor car voltage variations will alter that data. Also, the system's various components are built to last as long as the engine itself. The only parts that need occasionally be replaced are the spark plugs.

The Motronic system, Bosch says, can easily be adapted to suit changed requirements as may be demanded by new types of fuel or by new exhaust gas regulations that government authorities may choose to impose in the future.

Europe

Munich's Laser '79 exhibit points to growing laser, optoelectronics markets

About as good a place as any to spot the trends in Western Europe's optoelectronics markets is the biennial laser exhibition held on the sprawling Munich fairgrounds. This year, the 5,200 specialists from around the world—including a delegation from the People's Republic of China—who turned out for Laser '79/Opto-Elektronik early last month generally indicated a slowing pace for technology but strong growth for business.

The market for laser equipment, of course, is not quite transparent. For one thing, it is difficult to assess the role of lasers and related electronic parts in complete systems. For another, it is well-nigh impossible to obtain accurate figures on laser consumption for military purposes.

Figures. The general consensus, however, is that Western Europe consumed between $220 million and $250 million worth of nonmilitary laser-based and optoelectronic systems and subsystems last year. West Germany alone accounted for about $80 million worth. Adding between 70% and 100% to those figures, the experts say, would take military consumption into account. As for growth rates, they see annual rises of roughly 20% for the years ahead.

Easier to assess is the market for optoelectronic devices. Günther Hatzinger, sales and marketing manager for optical components at Siemens AG in Munich, pegs the 1978 world market for semiconductor-type optical devices (excluding solar cells) at about $430 million. Of that amount, Western Europe consumed roughly one third, or $146 million. One third of that, or some $50 million, he says, is West Germany's consumption. Other analysts come surprisingly close to those figures.

Hatzinger says sales of such devices will continue to rise unabated during the years ahead—at an estimated 30% annually. Giving a breakdown for the market, he notes that visible-light-emitting diodes account for two fifths of the total. Another two fifths is claimed by infrared LEDs, and the remaining one fifth by optocouplers, reflectors, and related items.

Ready for work. As for technology, the laser market has reached the stage of "backbreaking and down-to-earth applications-oriented design work," according to Hans Rottenkolber, head of Rottenkolber GmbH, a Munich holographic equipment maker. Adds Gerd vom Hövel, general manager of the Munich Fair

Voice on beam. The RLK-2 laser transceiver, developed by the Yugoslav firm Iskra, is a hand-held unit whose laser beam serves as the medium for voice communications.

and Exhibition Co., which served as host to Laser '79, "The show is turning more and more into a forum for practical and marketable systems that are based on a relatively young technology."

One example is Rottenkolber's PHK-1 "holo-double-pulse" camera that uses two laser beams to literally make the noise of, say, an engine, visible by way of a hologram. Another is a laser granulometer from the Compagnie Industrielle des Lasers (Cilas), part of the French Compagnie Générale d'Electricité (CGE). The $25,000 instrument distinguishes 16 powder-particle diameters between 1 and 192 micrometers and analyzes their distribution using an Intel 8080-based microcomputer.

Yet another example is a portable laser transceiver, model RLK-2, from the Yugoslav firm Iskra, priced at about $16,000 a pair. A gallium-arsenide infrared laser transmitter with a peak pulse power of 5 watts and a p-i-n photodiode receiver give the set a range of up to 7 kilometers. Because the laser beam does not scatter, the company notes, there is no way to eavesdrop on this walkie-talkie. -John Gosch

Japan

Benefits of digital process control come to one-loop systems

Direct digital control for industrial processes is now available in increments as small as one loop. Such controllers have long been desirable, but they have remained too costly.

Now, the TOSDIC-211 one-loop digital controller from Toshiba Corp. provides in one unit all the functions supplied by a complete line of analog controllers and auxiliary components. It also makes possible some applications—like adaptive, pH, and internal reflux control—that would not usually be attempted with analog controllers because they are insufficiently precise over the wide operating ranges involved.

The one-loop controller is equally applicable to the critical loops in large systems to distribute the risk and eliminate the possibility that failure of a single processor could affect more than one loop. The base load of control in such a system could still be handled by a digital system in which each processor controlled a larger number of loops. The new unit can also be mixed with analog controllers.

In control. Toshiba's one-loop digital controller performs more than 60 functions, including some that can be done by an analog unit only by adding extra hardware.

Built into Toshiba's controller is a repertoire of more than 60 functions, including subroutines for control, linearization, arithmetic computation, logic and comparison, and output. The number of subroutines—including repetitions—in the program of one controller can total up to 50, although far fewer would be used in a typical installation.

These functions are written in the 12 kilobytes of read-only memory on board. Four kilobytes of programmable ROM are included to allow the user to configure his particular system, including calling subroutines and setting parameter values. Thus the PROM selects the input-signal processing, control algorithm, and linkage information and sets initial values for the program.

Loading up. Toshiba prefers customers to do their own programming, rather than have the company do it. Therefore, it has also developed a PROM writer with a specially designed keyboard and display, which it calls a system loader. A hard-copy printer is provided for permanent records, as is a PROM eraser for correction and updating.

Since some users will have little occasion to change the system once it is running, Toshiba will rent as well as sell the loader. To encourage users to load their own systems, Toshiba sells an unprogrammed controller for some $2,200 but charges $2,500 for a programmed one.

Actual processing is implemented by Toshiba's 8085 microprocessor. Working memory, including storage of operator inputs, is a 2-kilobyte complementary-MOS random-access memory, which has a lithium battery backup in case of power failure. Front-panel controls and readouts similar to those on an analog con-

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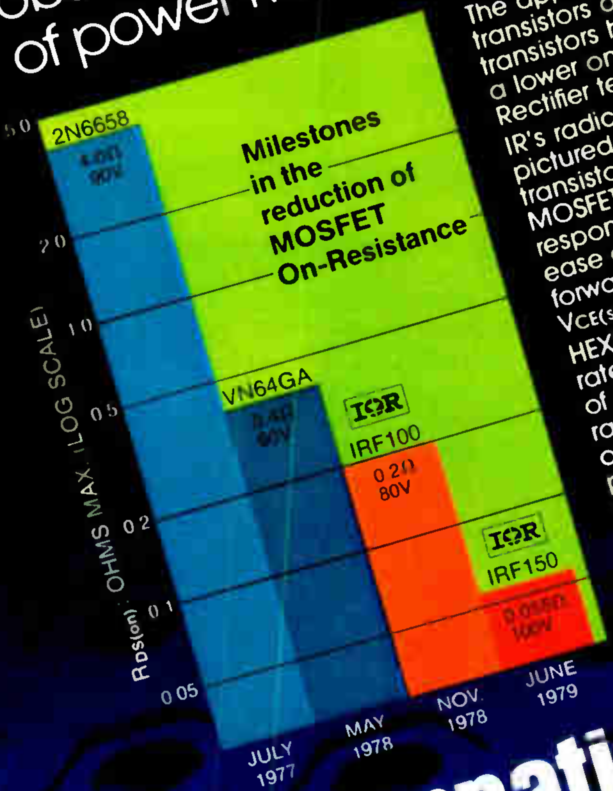

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troller, as well as a calculatorlike keyboard and display on the side of the controller, allow adjustments by the operator and readout of values stored in the RAM.

Parameters are processed in the form of a 4-byte floating-point word. Separate 12-bit analog-to-digital and digital-to-analog converters are used for inputs and outputs.

Since all controllers are identical except for their PROMs, which are highly reliable, a defective controller can be replaced by inserting its PROM into a good controller and then substituting the new unit.

Extras. Although the TOSDIC-211 costs perhaps $700 more than an analog unit, it has auxiliary functions built in that usually can be performed by an analog controller only by adding extra hardware. For example, the simple control of the flow of a gas requires four auxiliary functions. The output of the sensor that measures flow must be linearized by taking the square root of its output. Compensation for temperature and pressure is required, but before the former is made, the output of the thermocouple used to sense temperature must be linearized. Toshiba's one-loop digital controller performs all these and the control without extra hardware.

Furthermore, a cascade loop, which usually requires two analog controllers, can be implemented by the new unit at a significant savings. It would typically include the PID (proportional, integral, derivative) control function used twice and five auxiliary functions. **-Charles Cohen**

Great Britain

BPO moves into fiber optics

Fiber optics is making the big jump from engineering evaluation to operational status on the British telecommunications network. The British Post Office is awarding contracts for 450 kilometers of optical links at a total cost of some $13 million. Data rates will be 140, 34, and 8 megabits per second—three of the four digital transmission speeds on which European postal and telecommunications authorities have standardized.

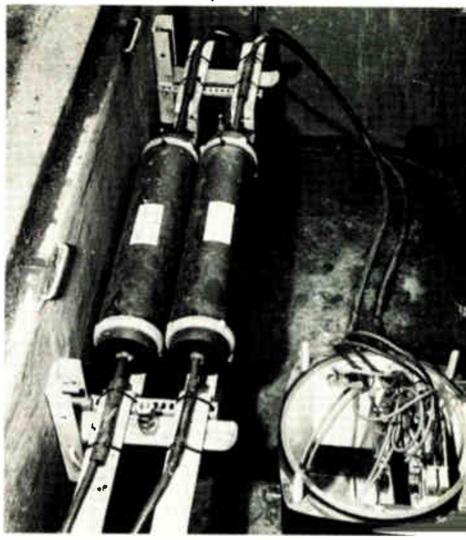
The first such contract, worth $3 million, has been placed with Plessey Telecommunications Ltd., Beeston, Nottingham, for the optical cable systems on one 34-Mb/s and four 8-Mb/s routes totaling 110 km; BICC Telecommunications Cables Ltd. will serve as subcontractor. Last month, General Electric Co. Ltd. (GEC), London, received the second, worth $5.72 million, for one 140-, one 34-, and two 8-Mb/s links totaling 172 km.

A third contract, to complete the post office's present plans, is expected to go shortly to Standard Telephones & Cables Ltd. (STC), London, an ITT subsidiary. Worth some $4 million, it will call for two 140- and four 8-Mb/s systems.

Though the systems may be marginally more expensive, as fiber costs fall the payoff will come. Furthermore, the attractions of these first-generation fiber-optic links are considerable. The 8.448-Mb/s 120-channel telephone system developed by Plessey, for example, can operate at distances up to 15 km without repeaters, compared with 3.5 km for conventional systems. Thus repeaters could be eliminated from well over 80% of the BPO's junction networks, which link neighboring exchanges, according to J. E. Midwinter, head of the Optical Communications Systems division at the post office's Martlesham Research Centre.

However, for its field trial system from Maidenhead to Slough, Plessey developed a repeater technology that it hopes to be able to exploit in overseas markets, according to F. A. Onians, the firm's director of marketing and planning. "The targets are urban and low-density trunk networks," he says.

For all the systems in the present round, the suppliers will use graded-index fiber with attenuations of about 2 to 3 decibels/km. BICC buys its from Corning Glass Works in the U. S., with whom it has a manufacturing option, and then forms the cable at its Prescott, Merseyside



Optical link. Repeater station (right) is part of Plessey's 8-Mb/s trial system.

plant. Rather than buy, both GEC and STC have invested in pilot production plants to make graded-index fibers, which they supply to their own in-house cable manufacturers. Their cables will be used on the post office's 140-Mb/s trunk-route systems.

The electronics in the systems involves high-radiance light-emitting diodes from Plessey Optoelectronics & Microwave Ltd. [*Electronics*, Dec. 23, 1976, p. 47 or 5E] in low-bit-rate systems and gallium-aluminum-arsenide lasers from STL Laboratories Ltd. in the trunk systems from GEC and STC. The receiver equipment uses avalance photodiodes from RCA. The LEDs operate at 850 nanometers, and the lasers at 900 nm.

The repeater requirement. The laser-photodiode combination used by both STC and GEC will be sufficient to meet a post office requirement of 8 to 9 km between repeaters on trunk routes.

The basic technology so far developed can meet the BPO's requirements for several years to come. The 140-Mb/s system, for example, can readily be run in tandem, by picking up the second cable fiber, to achieve a 278-Mb/s data rate. The use of hybrid techniques will allow repeaters to be packed in the same space, the post office says. Second-generation systems, according to one BPO expert, could be the first to operate in a single mode and will work at the longer wavelengths of 1.3 to 1.5 micrometers. Wavelength fiber attenuations of 0.2 dB have already been reported. **-Kevin Smith**

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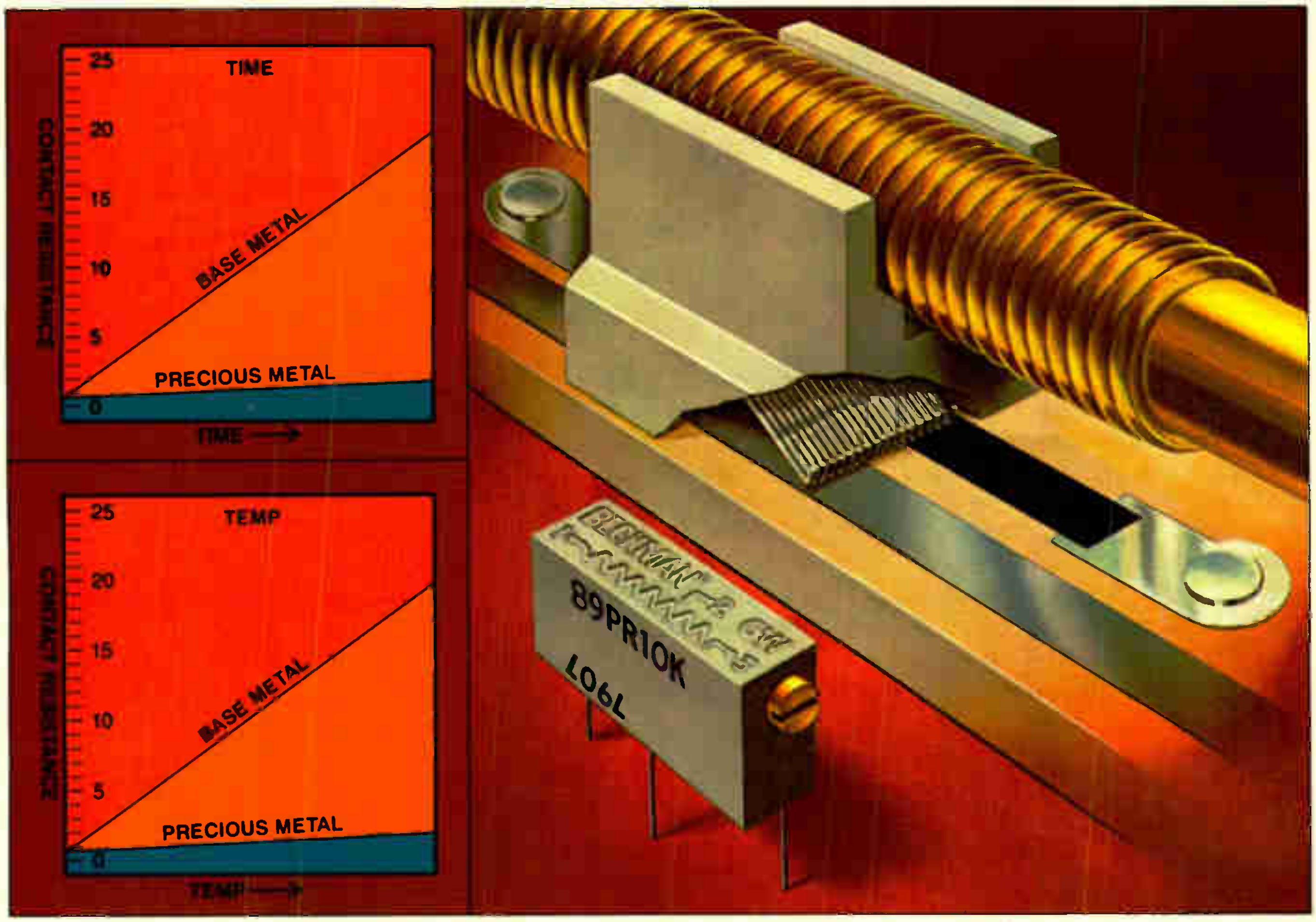

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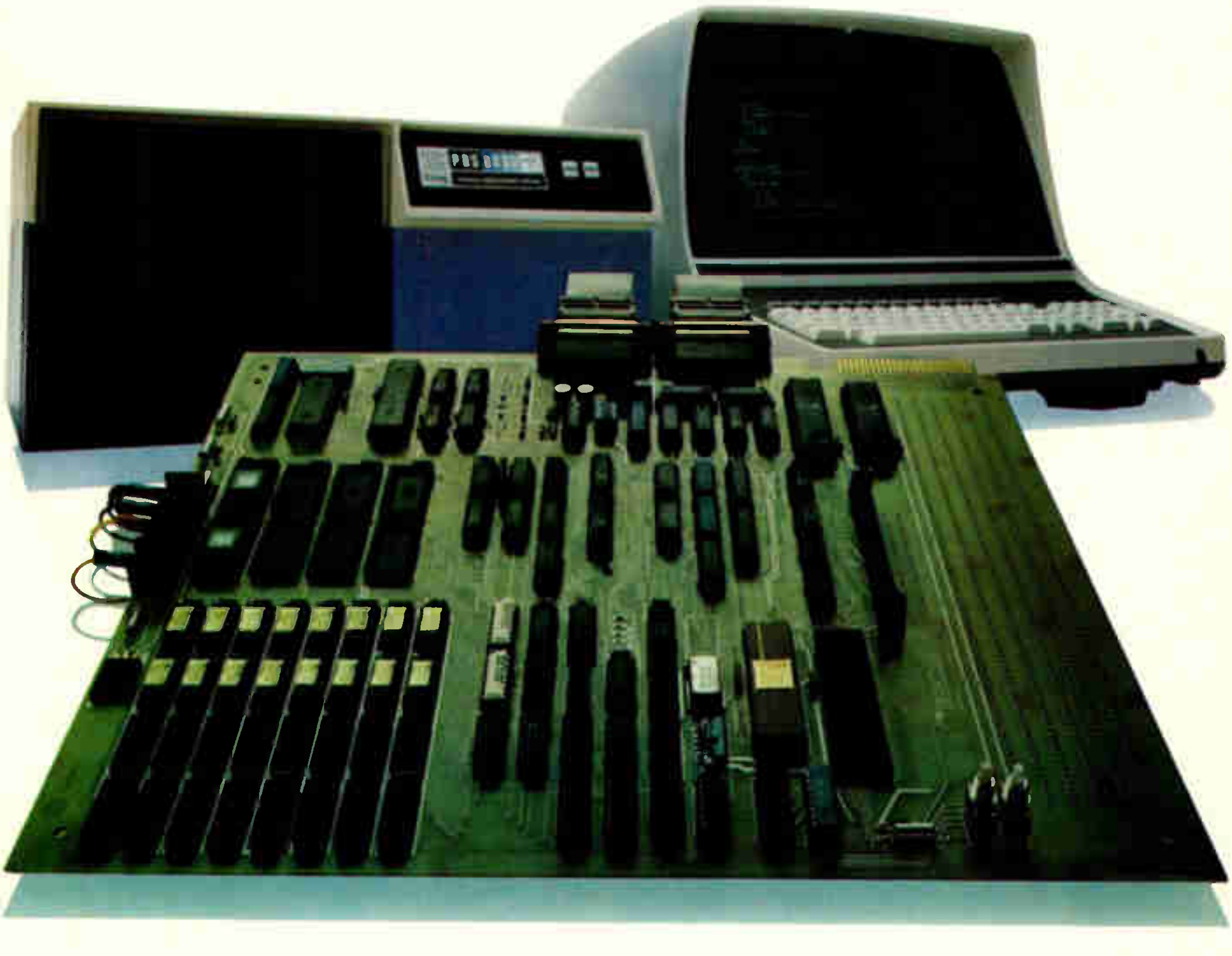

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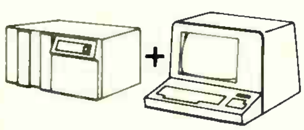

software development: a 64K byte microcomputer, CRT, dual floppys, interfaces, 9-slot card cage, power supplies, a Z8000 software development package, operating system, editor, linker and utilities. $10,500.*

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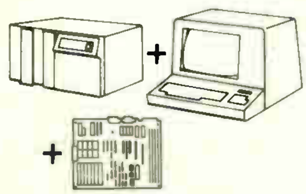

of EPROM (expandable to 8K words), 16 K words of dynamic RAM (expandable to 32K words), dual serial interface, 32 programmable I/O lines, four 8-bit programmable counter-timers and a generous wire wrap area. $11,995.*

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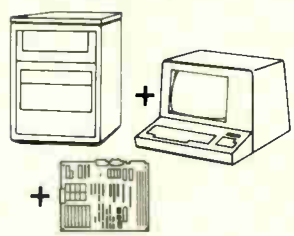

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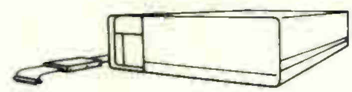

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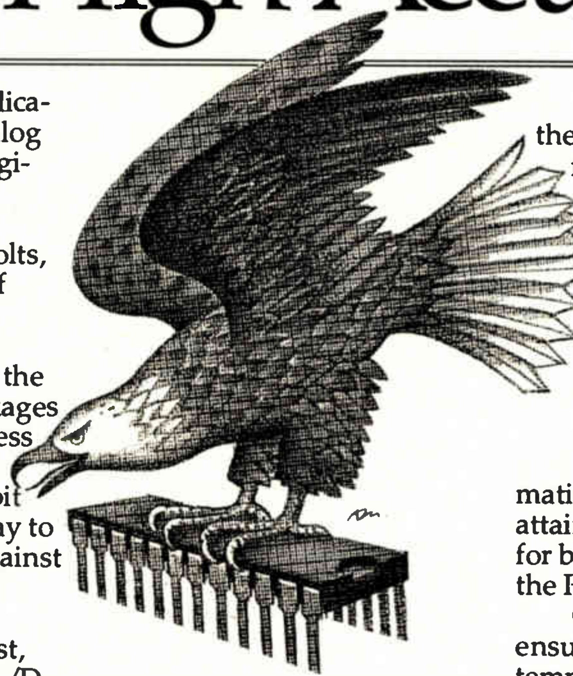


In automatic-testing applications, new high-accuracy analog LSI devices are giving test engineers fits. And this is just the beginning.

Specifications in microvolts, picoamps, and hundredths of a decibel are fast becoming commonplace.

Pin counts are already in the 18-28 range, with 40-pin packages on the horizon and 60 doubtless to follow.

A/D converters with 12-bit resolution are soon to give way to 14 bits, and no one will bet against 16 before too awfully long.

So, what engineers need right now is a really stable, fast, analog test system for 12-bit A/D and D/A devices and beyond. A system that can handle the mixed technology of present devices, with a comfortable reserve of speed, accuracy, and flexibility. For whatever the future holds.

In its new A300 family of analog LSI test systems, Teradyne has effected a marriage of high accuracy and high speed that is unique in the industry.

Our standard dc system allows measurements to be made within .05 percent of reading. Considering both gain error and tag error, this means that measurements can be made to plus or minus 6 millivolts at 10 volts. And measurement time is a mere 100 microseconds.

But for those who need truly high accuracy, the A300 offers an optional Precision DC Module, which allows voltage measurements to .005 percent of reading, with a tag error as low as 10μV.

An order of magnitude more accurate than any other system in the marketplace today, the measurement technique is a proprietary combination of successive approximation and triple-slope integration schemes, which makes measurement times beyond 600 microseconds rarely necessary.

A valuable supplement to the conventional dc voltage readout is called Device Normalized Scaling. Readout is provided in the form $\frac{V-V_0}{V_1}$, where V_0 and V_1 are programmable. In many applications this can greatly simplify test plans.

Several levels of automatic calibration are provided to attain the accuracies specified for both the standard system and the Precision DC Module.

Calibration accuracies are ensured by an ultra-stable, temperature-compensated, zener-diode reference assembly, offering NBS reference. It provides full calibration accuracy when inserted into any A300 system. And a replacement assembly can take over whenever factory recalibration is necessary.

Moreover, the Precision DC Module is now available for the hundreds of J273 Linear Test Systems presently in the field.

For more information on the A300 analog LSI test systems and the Precision DC Module, write Teradyne, 183 Essex Street, Boston, MA 02111.

TERADYNE

Britain gambles on System X

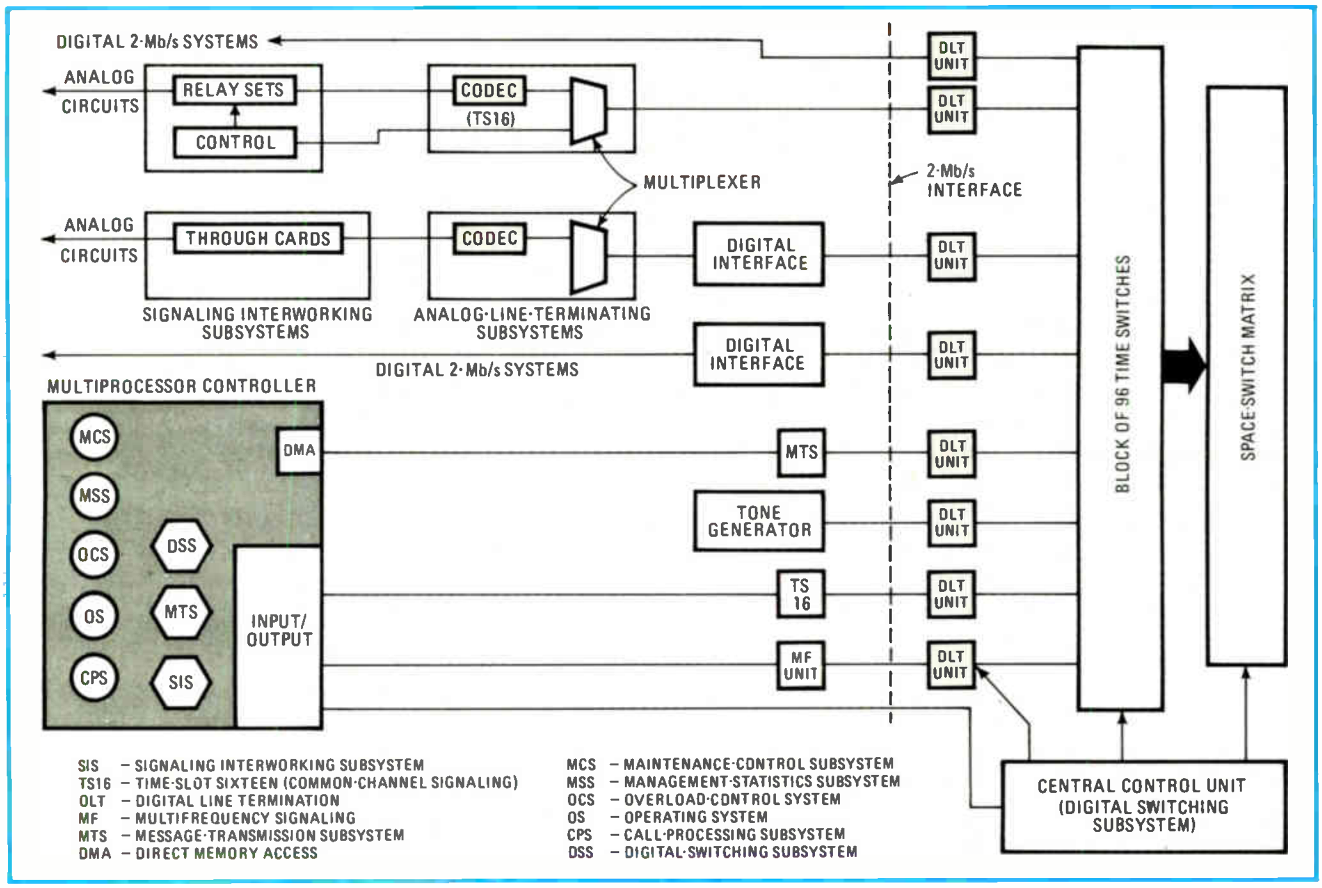
New digital switching system, to be shown first time at Geneva, is also designed to get nation back into export market

by Kevin Smith, London bureau manager

Few telecommunications projects have caused more controversy than the British Post Office's aptly named System X, which will be shown next month for the first time at the quadrennial telecommunications exhibition in Geneva. The project is intended to move Britain's telephone network, the third largest in the world, from analog to digital operation during the 1980s, as well as make the nation a major telecommunications exporter. The largest single operation ever undertaken by the British telecommunications industry, it has employed 600 Post Office and industry engineers; the full cost will be around $300 million.

Yet the secrecy surrounding System X has made for bad publicity, with reports that committee procedures involving the Post Office and its three suppliers were slowing design and that hardware would be outdated even before the wrappings were removed. This triggered a covert attempt by the government's National Enterprise Board, an agency set up to help technology companies, to merge two of the suppliers—Plessey Telecommunications Ltd. and Standard Telephones and Cables Ltd. That, in turn, caused a long dispute over how to sell System X overseas, for Britain wants to get back into the export market.

But, despite the dissension, when Post Office and industry executives finally decided to talk they were



Getting the call. British Post Office's System X will get its first showing at next month's Geneva telecommunications show. It is a digital network whose integrated services will be able to cover everything from small rural exchanges to computer-based record-keeping centers. In the diagram above, circles in multiprocessor indicate software; the hexagons are the software handlers.

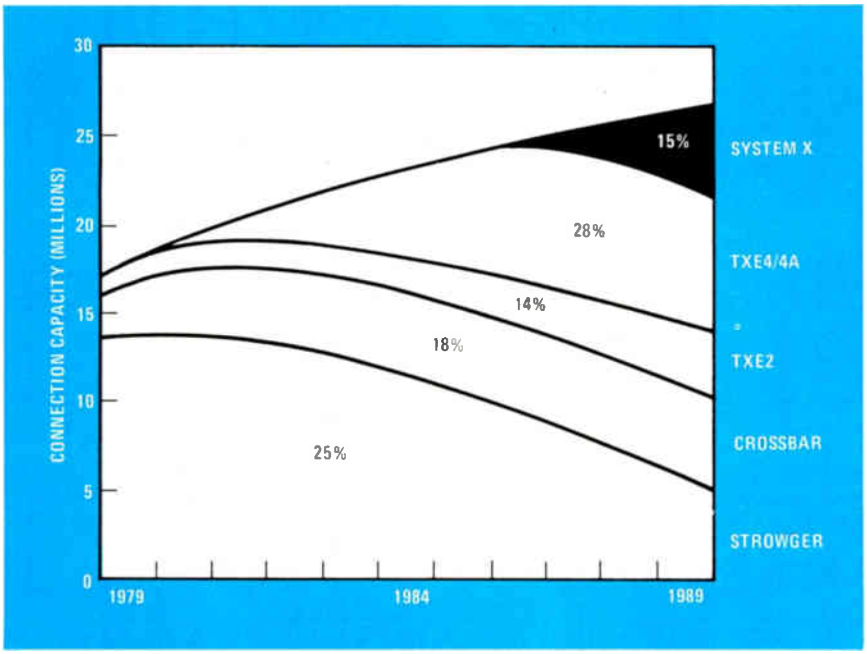
unanimously bullish on the prospects for System X. The hardware, described for the first time at an international switching symposium in May [*Electronics*, May 24, p. 76] has all the ingredients expected in a modern exchange: a digital central switch, stored program control, and four-wire common channel signaling. There is a high degree of modularity in hardware and software, from which exchanges of all sizes can be assembled. The hardware is stuffed full of microprocessors: the next-generation control processor will use a microprocessor array.

End of an era. The birth of System X marked the end of an era in the Post Office. Because of the huge cost of developing the new exchange systems, competitive development programs by all three suppliers were ruled out.

The UK's solution combines sound engineering practice and political expediency in the adoption of a highly modular design, with all three manufacturers developing separate system modules. GEC Telecommunications Ltd. took the contract for the stored program control processor, Plessey Telecommunications for the digital switch modules, and Standard Telephones and Cables for the signal interworking system used for internal communication and communication with older exchanges. The group is also developing a remotely controlled digital data concentrator for use in sparsely populated and fringe urban areas. Modularity also will ease assimilation of new technologies as they evolve.

The core of the program is a single data base that must capture design data once only, eliminating manual transcription and interpretation of engineering information with big gains in accuracy. Computer-aided design and manufacturing invades every stage of the manufacturing process: artwork generation, through printed-circuit-board manufacture, to tape preparation for numerically controlled drilling machines, to preparation of programs for insertion equipment and for automatic test equipment.

Too many paths. At the early stage, says Roy L. Harris, the Post Office's director of telecommunications strategy, the System X strategy team "was faced with serious problems arising from divergent approaches, standards, and strategies." In November 1977 an outsider, Sir William Barlow, took over as chairman of the Post Office and forced through recommendations of Sir William Ryland, managing director for telecommunications, advancing



Coming and going. The British Post Office predicts that System X all-digital exchanges will begin replacing TXE semielectronic types as well as crossbar versions in the 1980s.

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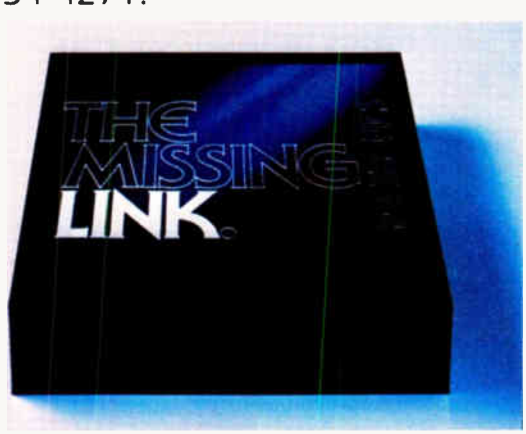

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the target by one year. "He concentrated our minds on one objective—Geneva '79," says one manufacturer. And he succeeded: the first exchanges went live in April, says Sir William, with one to be up and running in Geneva.

The ultimate test of the concept came when the first factory exchanges were put together. But, says John Tippler, deputy to the director of the System X development department, "the modules have been going together very nicely." More reservedly, one manufacturer agrees there are bound to be some problems, but he is confident they can be overcome. In fact, the Post Office has kicked off its System X program with orders for one trunk, two junction, and five local exchanges worth about $16 million and due to come into service by the end of 1982. The changeover should be very rapid after that.

But how exportable is the end product? Post Office engineers stress that it represents a total systems approach to a smooth transition from an analog to an all-digital network. In effect, System X was designed from the top down, a digital system superimposed on the existing analog system. Consequently, the Post Office is rushing through exchanges needed to create a skeleton digital data network to provide a variety of computer-based services for the business community. Such a complete package, the Post Office believes, could have attractions for developing countries.

Sales company. To help sell System X, the Post Office is offering its systems know-how in a newly formed consortium, called British Telecommunications Systems Ltd., with its three suppliers. Headed by managing director John Sharpely, formerly marketing director of Plessey Telecommunications, the company will promote System X overseas to the final tender stage. And when a contract is won, a consortium member will be chosen as lead contractor either because it has available factory space and can offer delivery, or because of historic links in a particular country. □

Communications

Bell bill takes a different tack

Amendments to Communications Act of 1934, not new law, would require separate AT&T subsidiaries for new businesses

by Ray Connolly, Washington bureau manager

Whatever revisions to telecommunications regulation emerge from the 96th Congress will come in the form of amendments to the 1934 Communications Act rather than its replacement by a sweeping new law that embraces broadcasting issues as well. Moreover, telecommunications leaders in the House, Senate, and White House now seem to agree that if American Telephone & Telegraph Co. and its Western Electric Co. manufacturing arm get into new competitive markets, it must be done through separate subsidiaries operating at a distance from the parent.

Thus the legislative controversy over how best to control evolving competition in U.S. markets dominated by the Bell System moved closer to resolution during July. The breakthrough came on action by Rep. Lionel Van Deerlin, chairman of the House Interstate and Foreign Commerce Committee's communications subcommittee. The California Democrat, sponsor of H.R. 3333, which would restructure the Federal Communications Commission and largely deregulate broadcasting, drastically altered his proposal after the bill became mired in his own subcommittee.

Bill revised. Rep. Lionel Van Deerlin has altered his Communications Act reform bill.

Widely criticized at the time of its initial introduction [*Electronics*, June 22, 1978, p. 58], the Van Deerlin proposal is being redrafted to drop broadcasting issues and concentrate solely on telecommunications regulation. And, like S. 611, its Senate counterpart sponsored by South Carolina Democrat Ernest Hollings [*Electronics*, March 29, p. 58], the new Van Deerlin proposals will be introduced as amendments to the existing law, rather than as replacements for it. The Hollings bill has already cleared the committee.

Not far enough. While most advocates of competitive telecommunications praised Van Deerlin's change in style as making passage of legislation much more likely before next year's adjournment, most claim his proposals do not go far enough in separating AT&T's components. The Ad Hoc Committee for Competitive Telecommunications (ACCT), for one, wants all Bell System interexchange services, not just competitive services, in a separate subsidiary. Similarly, the North American Telephone Association (NATA), comprising interconnection and service companies, believes "that the creation of totally separate subsidiaries for direct carrier entry into competitive markets is the 'fairest' solution for all parties."

Van Deerlin proposes separating AT&T subsidiaries for competitive services and products while permitting "the current partnership between the Long Lines company, the Bell operating companies, and the independent telephone companies to continue for purposes of providing Message Telephone Service [MTS]." At the same time, Van Deerlin would drop his earlier plan to end regulation of the MTS network by the Federal Communications Commission after 10 years and would require that MTS could be resold by any customer—a service now prohibited by FCC rules.

AT&T competitors see a loophole in Van Deerlin's observation that "while MTS is the only service that could be provided directly by the network, the network would be able to own facilities for other services, including private line, foreign exchange, CCSA, and enhanced data

Bill progressing. A reform bill by Sen. Ernest Hollings is out of committee.

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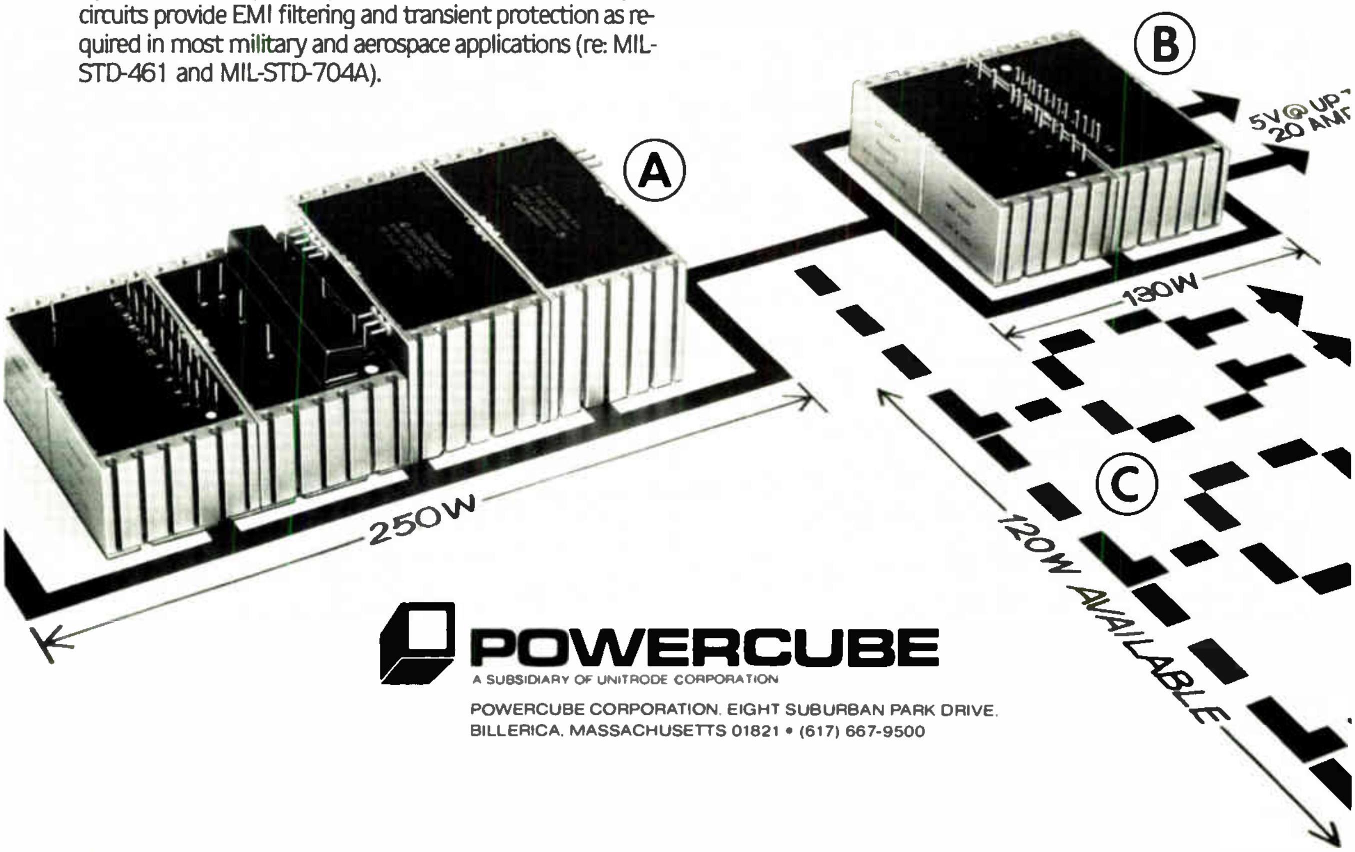

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services such as the proposed Advanced Communications System." The FCC would decide what is a permissible "enhancement," a power that competitors see as potentially troublesome.

There is concern, too, that Western Electric Co. would not have to be operated as a subsidiary, much less spun off as originally proposed. Van Deerlin now proposes that "Western Electric be required to establish separate divisions—an accounting separation of functions—for sales in the regulated (sales to Long Lines and operating companies) and unregulated markets. To the extent that Western Electric desires to participate in unregulated markets—terminal equipment, data processing, computers, etc.—it would be required to make products available through a separate subsidiary, which may or may not be the same as the subsidiary providing services." Only those subsidiaries would be free of the 1956 consent decree preventing AT&T from entering unregulated markets, but Van Deerlin's earlier proposal requiring Western to sell outside Bell would be dropped.

Finally, the FCC would be required to oversee the mechanics of transition "to preserve the availability of the system engineering services provided private line users today."

Timetable. Van Deerlin's revised proposals will not be put into appropriate legislative language until Congress returns from its August adjournment. Then AT&T and a variety of competitive industry groups are likely to call on the House subcommittee chairman to incorporate other multiple revisions into his measure.

AT&T indicates it is still studying the Van Deerlin changes, but initial indications are that the company finds it much preferable to the earlier bill. On the other hand, International Telephone and Telegraph Corp. and the specialized common carriers represented by ACCT, the ad hoc committee, want Van Deerlin to specify that legislative revisions will not exempt any Bell System segments from future antitrust action, as well as a need to define in detail equal access and access charges to local exchange facilities by carriers competing with AT&T.

ACCT's Herbert Jasper, executive vice president, was most sharply critical of the Van Deerlin proposals in a letter to the subcommittee chairman, calling his MTS plan "wholly unwarranted." Jasper argues that "no credible evidence—indeed nothing but unsupported claims—has been offered to show that either competition or concepts in the pending legislation pose any threat—technical or economic—to 'the network.' Thus, there is no reason to assume that TO 11 service, or MTS, requires a special statutory status to ensure universal service or to ensure a dial tone."

ACCT's alternative, Jasper wrote, "would take nothing away from AT&T or from 'the network.' It would merely organize all Bell's interexchange services in a separate subsidiary parallel to, rather than superior to, the operating companies. The competitors must have a more nearly equal status if competition is to be enhanced."

IEEE's view. A substantially different position more favorable to AT&T was advanced by the Committee on Telecommunications Policy of the Institute of Electrical and Electronics Engineers. While acknowledging the need for revisions to communications law brought about by technological advancements, the IEEE unit warned that Congress should seek to acquire more technological expertise before rewriting the present laws in a manner that threatens to "diminish the utility and future capabilities of the telecommunications network while increasing consumer costs."

The IEEE committee warned that "the network is a fragile and complex entity which is generally taken for granted; it can be severely degraded at greatly increased cost if the present mechanisms, standards, and state-of-the-art conditions are not clearly understood."

Bell Telephone Laboratories—which Van Deerlin would leave largely unchanged except for the creation of separate accounting systems for regulated and unregulated segments of AT&T—"should be recognized as a major and irreplaceable national resource," the IEEE committee declared. □

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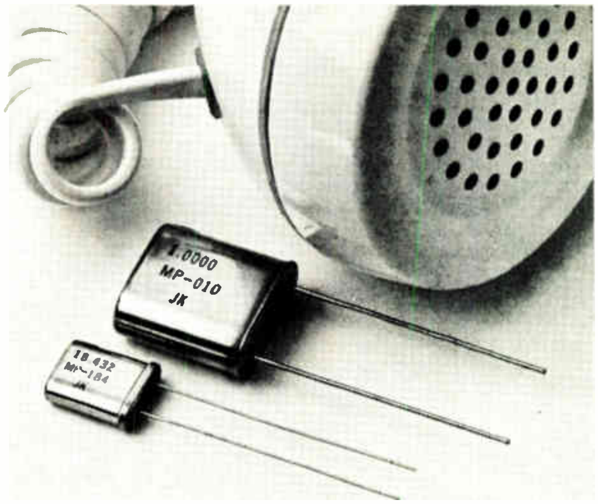

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Companies

Growing pains for Zilog

Rivals talk about personnel, production, and product woes, but president Faggin says four-year-old company is on right track

by William F. Arnold, San Francisco regional bureau manager

Cash is the lifeblood of any new company, but it's no foolproof cure for all headaches. The reason is that it is not so easy these days to start up and grow a high-technology company, no matter how much money is available initially. The technology is so dynamic and the start-up costs are so high that the payoff in products and profits can be a long time coming.

A case in point is four-year-old Zilog Inc. Backed by the mighty Exxon Corp. and originator of the world-class 8-bit Z80 microprocessor, it comes close to having had the best possible start. With the Z80 under its wing, tiny Zilog soared into wide visibility, pushed along by the potential of two other chips, the 16-bit Z8000 and the single-chip 8-bit Z8 microcomputer.

But as Zilog begins its fifth year, the stresses and strains of rapid technological growth have produced the following scenario. First, a dispute between two founders was resolved only when one left the company. Then other key management personnel left, to be replaced with new blood as the Cupertino, Calif., company reorganized. Products, some made with different processes, competed for space in the company's one wafer-fabrication area. The Z8000 (Zilog's top gun against Intel Corp.'s 8086 and Motorola Semiconductor Group's upcoming 68000 systems) and Z8 are coming into the marketplace later than announced, although this delay is not unusual among chipmakers. And the high-flying company got its image clipped a little when it lost the first round in a $5 million damage suit by National Semiconductor Corp., which alleges that Zilog stole trade secrets on a new 16-bit microcomputer.

National's suit rankles Zilog president Federico Faggin. It alleges that five former employees—headed by Bill Sweet, who became Zilog's marketing director (see p. 14)—took with them confidential papers on the design and marketing plans of National's own upcoming NS16000 when they left for Zilog. Zilog denies that the papers are either confidential or important and maintains that with its own 16-bit device it has no interest in National's.

All the commotion has industry observers saying what they think is wrong. Here is a selection:

- Organization is poor. Says an industry analyst, "They haven't pulled together, there's a lot of turmoil. And they're losing money."
- Zilog is having process problems as well. "They tried to do four processes at once instead of perfecting them one at a time," points out a competing marketing executive.
- Zilog has too narrow a product line and the wrong mix of products.
- Choices of second sources—Mostek for the Z80 and Advanced Micro Devices Inc. for the Z8000—are questionable because both will end up taking business away from Zilog.

Called unfair. "I don't think these accusations are just," replies Faggin. "I don't take them seriously." He sees such talk as common sniping by people who forget what their own companies have been through. About products, he says, "After all, we're only four years old. Clearly, we can't have the product line of a company that has been in business 10 years." Even so, Faggin says that young Zilog already has developed three advanced microcomputers.

Faggin also puts management problems behind him. "The company is stronger than it ever was," he declares. "It had problems; the problems were fundamentally management problems," he continues. "We've solved them." But there have been some recent defections. For example, Charlie Bass, system division general manager [*Electronics*, Jan. 4, p. 14], and Masatoshi Shima, designer of the Z80 and Z8000 and instrumental in the design of the industry-standard 8080, left to return to Intel [*Electronics*, April 12, p. 34].

It is hard to measure the cost of such turmoil on a new company. But the cost can be roughly measured by parent Exxon Enterprises, which owns more than 80%. So far Zilog's accumulated losses are less than $10

Thoughtful president. Zilog's Federico Faggin says company is stronger than ever.

million, including losses last year of less than $6 million on sales of about $18 million, depending on the accounting system used. This year, Zilog expects to become profitable in the fourth quarter, with projected annual sales of about $40 million. These figures would depend on how Exxon capitalizes expansion, including the new manufacturing plant in Boise, Ida., due to open this year.

More capacity. Faggin is optimistic. He sees the Boise plant, for example, giving Zilog a "substantial increase" in capacity so that it can grow further. At the same time, although microcomputer and peripheral logic parts represent a large portion of business, Zilog is expanding its microcomputer-compatible memories, with such devices as the 6132, a 4,096-by-8-bit pseudo-static RAM. Some Z8000 peripherals also are due out toward the end of the year. And the agreement is still on that National will second-source the 6132 and the two companies will codevelop 2-K-by-8-bit and 8-K-by-8-bit companions that will work with the Z8000 and the NSC16000 [*Electronics*, April 26, p. 33].

As for his choice of second sources for the Z80 and Z8000 and the risk that they will take the business away from Zilog, Faggin says, "The choice of a strong partner was intentionally made to create a strong market. The key in microcomputers is to get them designed in. The stronger the partner, the more that will happen."

How does Exxon see it? "Probably there's a basis for many of the rumors" critical of Zilog, according to Donald L. Spalinger, Exxon's contact executive with Zilog. He generally attributes problems to those typical of a high-technology company in a fast start-up mode.

Spalinger says that Exxon has no performance goals for Zilog except the general one that it is "going to be a microcomputer systems company. It will be both a components and a systems house." Marketing director Sweet agrees when he says that chipmakers have to be concerned with systems software. He expects that as the market matures, customers will be less concerned with hardware and more interested in such matters as Fortran and Cobol. □

Consumer electronics

Tape plays a growth tune

Worldwide sales of audio and video versions to amateurs will rise as much as 22% a year in near future, study says

by John Gosch, Frankfurt bureau manager

The world has become wrapped up in magnetic recording tape. So indicates a new study of international demand for all types of tape by Agfa-Gevaert, one of Europe's top tape producers. It says that not only have sales increased 15% annually during the past few years, but they will increase even more rapidly—22% in some years.

Analysts at Agfa, a West German-Belgian concern that also makes photographic accessories, say that the 15% rate has pushed the world market from about \$1.9 billion in 1974 to roughly \$2.27 billion in 1978, with the U.S. accounting for some 50% and Western Europe and Japan for about 30% and 12%, respectively.

Singling out audio and video tape for amateur use only, the Agfa researchers come up with a worldwide consumption of \$1.59 billion for 1978. That figure represents about 70% of last year's total tape sales. Magnetic tape for commercial applications, mainly in the computer sector, accounts for the remaining 30%, some \$680 million.

Video vital. Video tape occupies a relatively strong position in the equation, and it should grow stronger. The world consumption of audio tape by amateurs last year amounted to some 670 million square meters, eight times more than video tape. But in value the ratio works out to only 3.2 to 1, or \$1.216 billion for audio and \$38 million for video.

The study predicts the video tape market will increase considerably during 1980–83 relative to that for audio, until the volume of audio tape consumed will be only four times that of video tape—1.003 billion versus 252 million square meters. In terms of market value, however, video will grow much more rapidly.

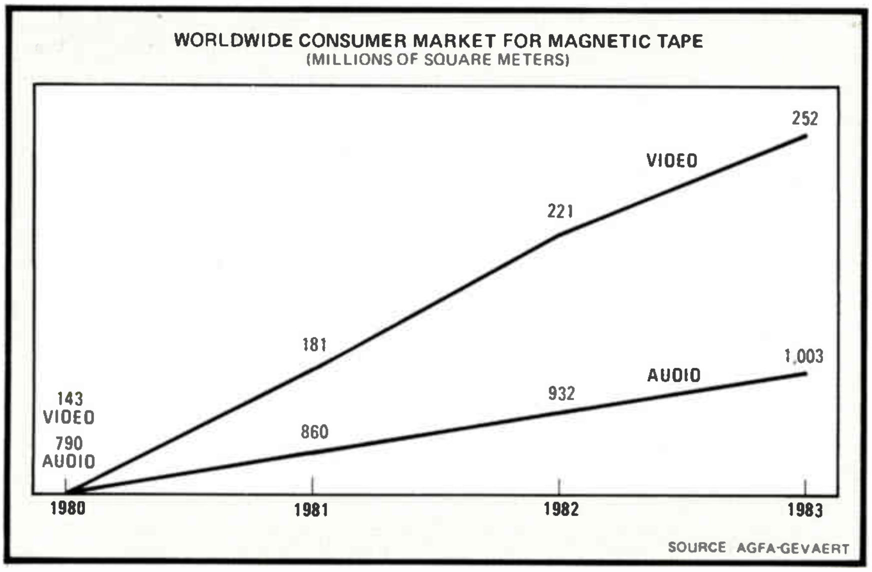
Since the introduction in the 1950s of the home reel-to-reel recorder, and in the 1960s of the eight-track cartridge and cassette, the amateur audio tape market has increased by leaps and bounds, as is seen in by the rapid penetration of cassette recorders into the home. In Europe, recorder saturation on a per-household basis shot up from 10% in 1970 to 91% last year, Agfa says. The corresponding figures for Japan are 26% and 118%, which means that a considerable number of Japanese households have more than one recorder. In the U.S., penetration went from 46% to 170%.

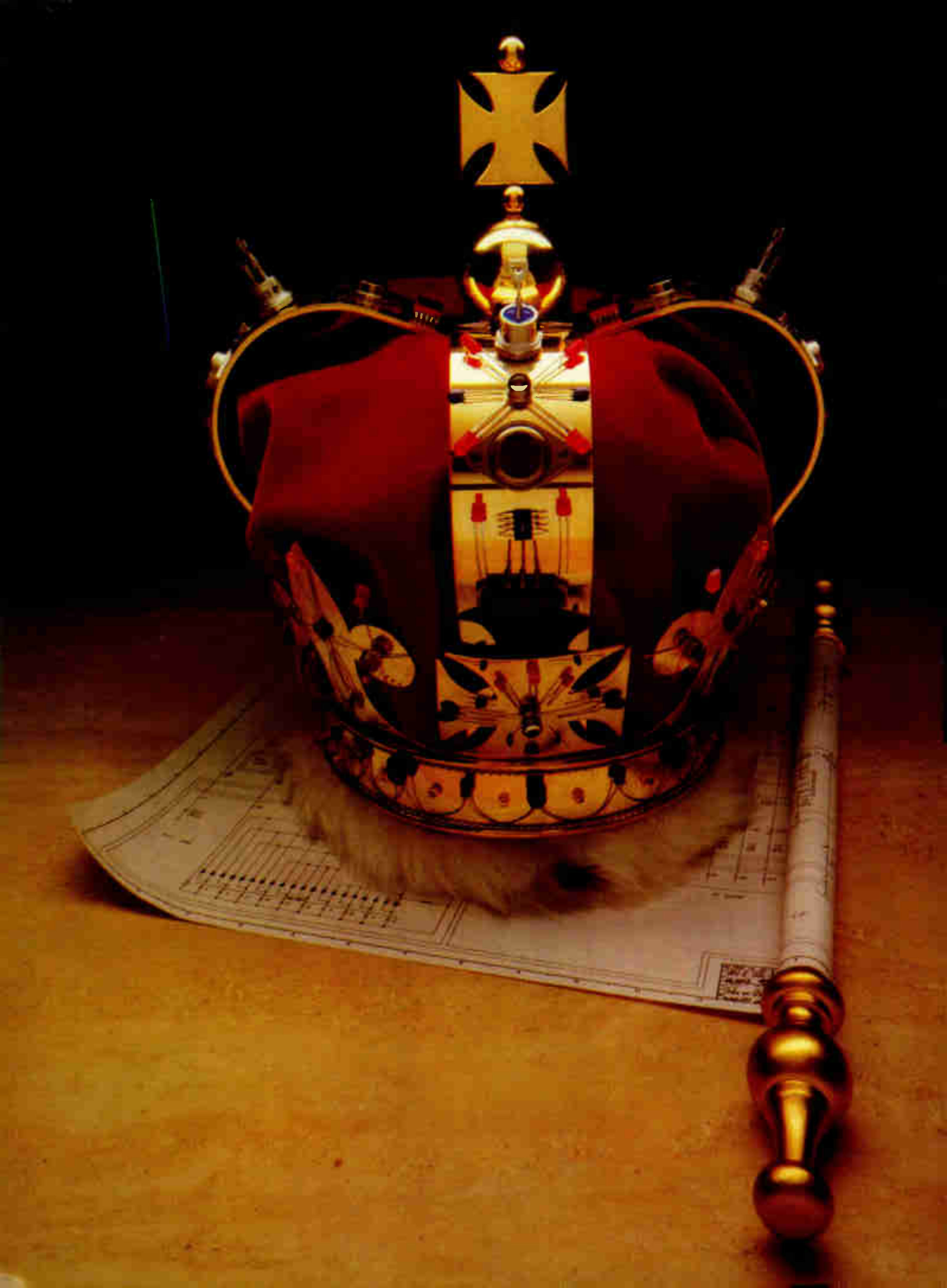
Like the audio market, that for video tapes was originally the domain of professional users. For the hobbyist, the video tape age did not start until 1971, when Philips entered the market with its video cassette recorder (VCR).

Despite the lack of standardization among VCRs, Agfa says, the entertainment electronics industry is certain that video recorder sales will increase rapidly. The reason: the high level of color TV saturation—94%, 95%, and 44% in the U.S., Japan, and Western Europe, respectively—will do a lot to push VCR.

Giving an estimate, the company puts the number of video recorders that will be in use worldwide this year at about 3.6 million. The number should climb to some 12.2 million by 1981 and to a whopping 32 million by 1983.

Tape sales will be stimulated not only by users' desire to record TV programs but also by their wish to arrange their own programs. Agfa has already made a start with its so-called Video Transfer Service, enabling amateurs to have their own 8-millimeter films and 35-mm slides recorded on video tape. □





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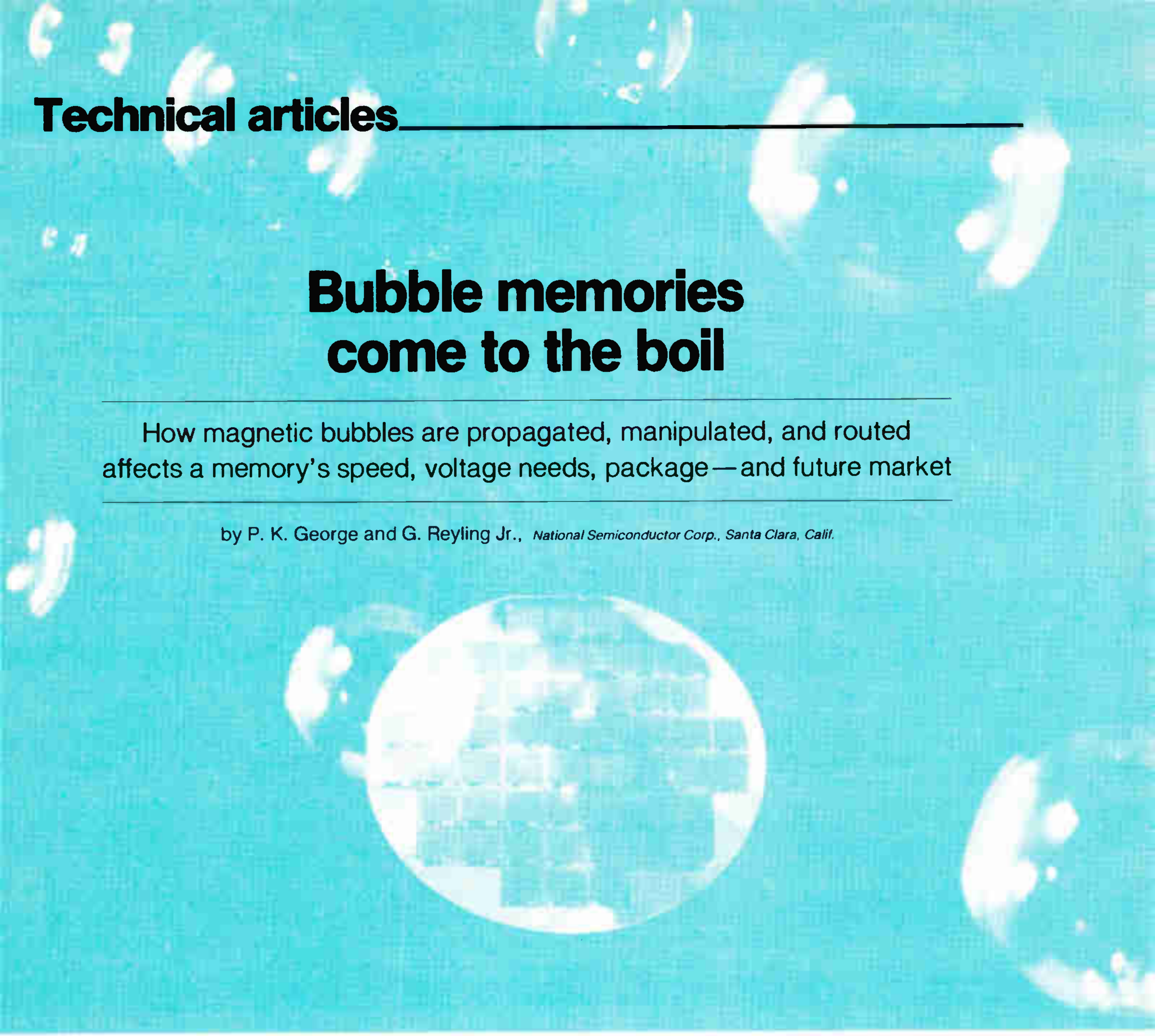


Bubble memories come to the boil

How magnetic bubbles are propagated, manipulated, and routed affects a memory's speed, voltage needs, package—and future market

by P. K. George and G. Reyling Jr., *National Semiconductor Corp., Santa Clara, Calif.*

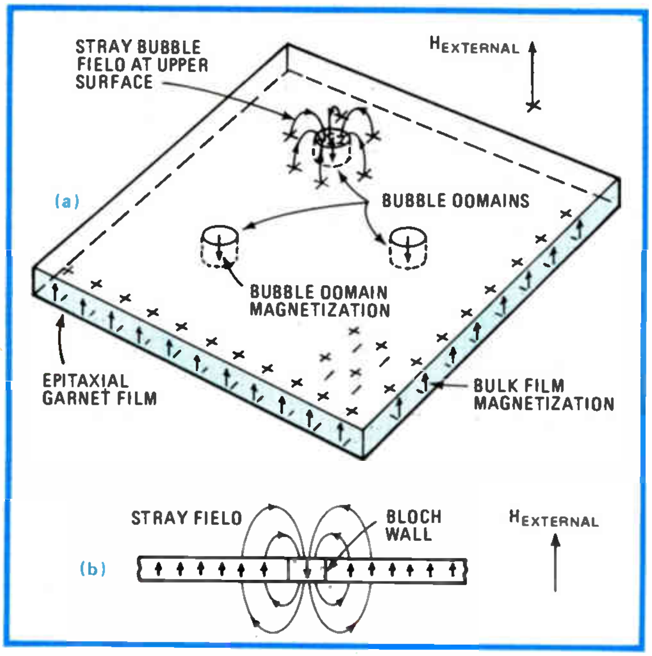
☐ With the announcement of devices by a number of companies, magnetic-bubble memories have at long last arrived. Already several major semiconductor firms are positioning themselves to do battle for the component and subsystem markets that will undoubtedly emerge in the early 1980s and grow throughout the decade.

The 256-K and 1-megabit chips will employ the coil-driven, field-access technology almost exclusively. But it is likely that for the next generation of 4-megabit devices and possibly even 16-megabit parts, the bubble-chip propagating pattern will change from the conventional asymmetric-chevron array to the contiguous-disk pattern. On the horizon is a current-access technology recently introduced by Bell Telephone Laboratories. It could solve the power supply and performance problems associated with field-access technology, though at a price—it departs vastly from the cost-reduction strategy of the past. But because it brings bubble memories into the 5-volt power supply regime and in addition eliminates drive coils, it will be attractive to semiconductor and microprocessor manufacturers.

However, as the capacity of a chip goes up, so typically do its average access time and voltage requirements—unless its organization is changed so as to counter those undesirable side-effects to some degree. The tradeoffs become quite complicated, but a look at them will aid the designer in assessing the various chips and their implications for different memory systems. Such an organizational perspective also helps in anticipating the future 1-megabit and 4-megabit chip designs.

Today's product

In most existing and proposed bubble memory chips, the bubbles travel along major and minor loops. Because a surplus of minor loops is always included, this kind of organization provides the built-in redundancy that is



1. Domains. Common to all bubble-memory chips is the formation of stable bubble domains with a magnetization opposite in polarity to that of the epitaxial garnet film (a). Stray magnetic field of reverse domains is indicated by lines of flux (b).

vital if decent yields are to be obtained with high-capacity chips. The loops can be arranged in various ways, but what is organizationally possible with them is to a large extent dictated by the other chip components—the bubble generators, replicators, and detectors, plus the gates for transferring or swapping bubbles between the major and minor loops. These components in turn will be affected by the increased chip capacity and decreased bubble size that future memory designers will be bound to employ.

A magnetic-bubble memory sandwiches a thin film of magnetic material between two permanent bias magnets. All the contending technologies represent logical 1s and 0s by the presence and absence of a reverse domain of magnetization in this thin film. (Other schemes in which different states of the domain wall represent data have fallen into disfavor, partly because of difficulties over incorporating the necessary redundancy.)

Figure 1a shows some cylindrical magnetic domains in an epitaxial garnet film that have been stabilized by the presence of an external bias field. The magnetization of each of these domains has a direction opposite to that of the remainder of the film, from which it separated by a transition region known as a Bloch wall. It also produces a stray magnetic field above the film surface like that of a magnetic dipole (Fig. 1b).

Moving bubbles

It is by means of this field (or equivalently the magnetic surface charge) that the bubble can be moved in the plane of the film. Conventional bubble memories make use of field-access propagation. The layer in which the bubbles occur has on it a thin-film permalloy pattern that lies in the plane of a rotating magnetic field generated by two coils. The changing poles thus induced in the permalloy pattern attract the bubbles beneath and drag them along from one pattern element to another, as shown in Fig. 2. The asymmetric-chevron pattern in the figure is currently regarded as the most desirable propagation element: however, it works well for propagation in one direction only. A more severe drawback of this technology is the degree of lithographic resolution needed to create the gap between the chevrons, which is typically only one half to two thirds of the bubble diameter. Given a 2-micrometer bubble and spacing between bubbles that is usually four times their diameter (or six to eight times the gap), asymmetric-chevron patterning is restricted to a 1-megabit chip capacity for most manufacturable chip sizes. Indeed as early as 1975, the feasibility of making a 1-megabit chip was demonstrated by Rockwell International Corp. and volume

2. Conventional. Most field-access magnetic-bubble memories use asymmetrical-chevron patterns. Their drawbacks: propagation is good in one direction only, and the critical lithographic dimension—the spacing between two neighboring chevrons—is at best two thirds the bubble diameter.

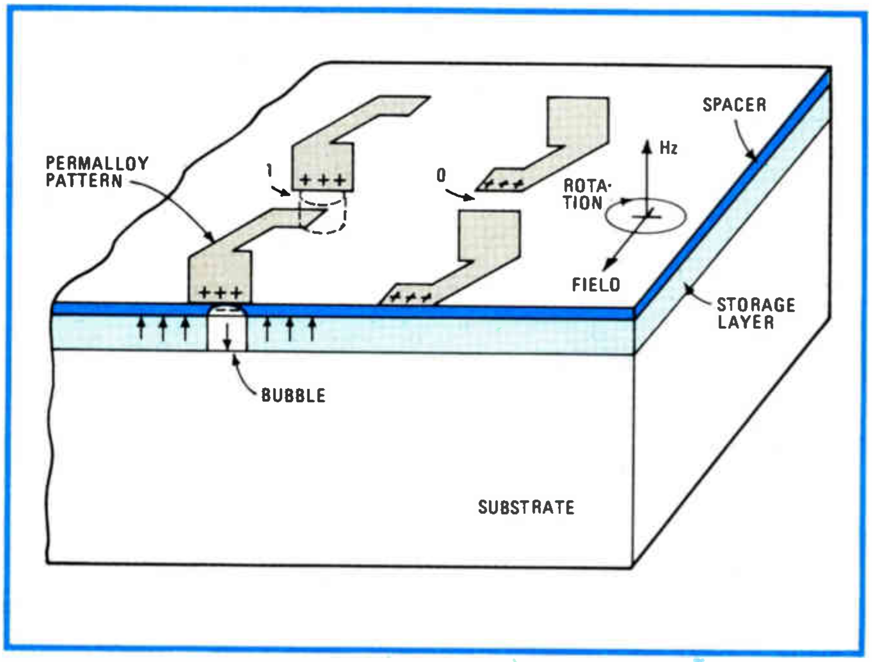


TABLE 1: ORGANIZATIONAL FEATURES OF MAJOR-MINOR LOOP CONFIGURATIONS		
Organization	Advantages	Disadvantages
Serial register	few pins, low voltage, simple design	low yield, long access time
Major-minor loop	few pins, low voltage, short access time, redundancy	complicated power-down, long cycle time
Block-replicate	short access and cycle time, simple power-down with swap, relatively few pins, redundancy	relatively high voltage
Bonyhard	short access and cycle time, low-voltage power-down possible, few pins, redundancy	complicated gates and controller
Multi-block	same advantages as block replicate plus higher data rate	many pins, redundancy compromised by peripheral area
G loop	unidirectional transfer gates, operation in continuous readout mode possible, low voltage, few pins, redundancy	long cycle time, complex controller

production of such chips is expected in the early 1980s.

The emerging candidate for larger-capacity chips is contiguous-disk technology, which can to some extent be regarded as a refinement of conventional field-access technology. The permalloy patterns are replaced by a thin drive layer of in-plane magnetization produced by ion-implanting the surface of the garnet film with a pattern of contiguous disks. Proper selection of the implanted geometry combines with a rotating magnetic field to produce attractive and repulsive charge walls that circulate around each disk and drag the bubbles with them, passing the bubbles on from one disk to the next (Fig. 3). This technology improves on permalloy technology in three important respects: the lithography requirements are relaxed; the rotating drive field can generally be less intense; and bidirectional propagation can be achieved with no performance loss.

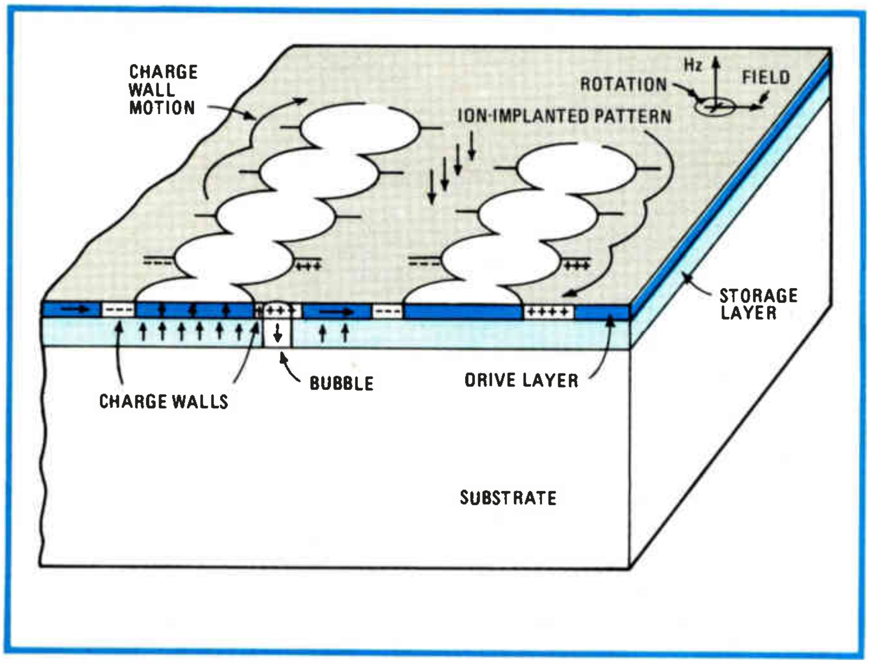
The reason contiguous-disk technology yields greater densities is that empirically the lithography resolution required is one and a half to two times the bubble diameter. That means 1-μm bubbles could be propagated in a structure using current lithographic minimum feature sizes. Thus contiguous disks open the door to a 4-megabit chip, provided that the problems associated with 1-μm-bubble materials can be solved and also provided that the required chip components can be demonstrated for 1-μm bubbles, as most of them have for 2-μm bubbles. It is also possible that contiguous disks will yield a shrunken, alternative version of the 1-megabit asymmetric-chevron chip, depending upon how fast the technology progresses. At least one manufacturer appears to be planning contiguous-disk 256-K and 1-megabit parts.

Problems with coils

A disadvantage of field-access technology—whether chevron or contiguous-disk—is its requirement for a high-frequency rotating field. Though it has been demonstrated that the bubbles themselves are capable of 500-kilohertz operation, a practical upper limit is probably 200 kHz. This limit is set by the power dissipation due to both skin-effect losses in the coil windings and eddy-current losses in the metal package components.

TABLE 2: HOW BUBBLE MEMORY CHIPS ARE ORGANIZED			
Company	Chip capacity	Chip organization	Detection scheme
Texas Instruments Inc.	92 K	144 by 64 bits, major-minor/swap	alternate bit
	256 K	256 bits by 1 K, block replicate/swap	consecutive bit
Rockwell International Corp.	256 K	256 bits by 1 K, block replicate/transfer	alternate bit, dual detectors
Hitachi Ltd.	256 K	256 bits by 1 K, block replicate/transfer	consecutive bit
Fujitsu Ltd.	256 K	256 bits by 1 K, major-minor/transfer	alternate bit
National Semiconductor Corp.	256 K	256 bits by 1 K, block replicate/swap	consecutive bit
Intel Corp.	1 megabit	256 bits by 4 K, multi-block replicate/swap	consecutive bit

That problem has been recognized for some time and various current-access approaches that would eliminate the coils have been proposed. The most recent of those, announced by Andrew Bobeck of Bell Laboratories, is illustrated in Fig. 4. The design relies on two conductive sheets punctured with rows of elongated holes. Every hole on one sheet overlaps with the ends of two holes on the other sheet. Current flowing in the sheets transversely to the axis of the holes produces fields (or poles) that attract bubbles underneath to (or repel them from) the ends of these holes. (The polarity of the poles at any instant can be deduced from the right-hand rule.) By driving both sheets with alternating current, bubbles can be advanced from one hole to the next—and in either direction. Moreover, the lithography requirements are about one quarter to one half of the propagation period (or one to two times the bubble diameter), making current-access technology comparable in density to contiguous-disk technology. But what may be more important is its potential for operating at a 1-megahertz intrinsic data rate with a 5-V supply—clearly out of the question for field-access technology. Hypothetical 256-K



3. Next pattern. Next-generation bubbles will use contiguous-disk technology. In place of a permalloy overlay, patterns of in-plane magnetization are ion-implanted directly into garnet. Advantages include bidirectional propagation and a bubble size that halves the lithographic resolution.

current-access chips with these characteristics have been proposed that dissipate less than 0.5 watt, which is comparable to the power dissipation levels of existing bubble technology.

Thus far the net performance benefit of the technology is somewhat obscure. For example, because the conductor resistance is so low, the page size—that is, the major-loop length—must be made large, which compromises performance. Furthermore, driver losses may be much higher than for field-access devices because of the high current and low voltage required from their function driver chips (to be discussed later). What is clear, however, is that elimination of the coils would considerably simplify the packaging of bubble memories and reduce its relatively high cost by perhaps 20%.

The final package

Figure 5 shows the construction of a typical field-access bubble memory package. The chip-carrier has the shape of an E to facilitate coil assembly and is made either from filled epoxy board (as shown) or from polyimide tape beam-lead–bonded to the chip and with a coil-support structure molded round it (not shown). For most commercial applications an open-ended Mumetal shield provides a return path for the magnetic flux produced by the permanent-magnet bias plates, at the same time shielding the chip from stray external fields. The chip-carrier and lead-frame assembly is inserted into the shield and magnet assembly and potted in place. (Since potting does not lend itself to volume production, several companies are instead injection-molding a plastic package around the E frame and inserting the magnets into pockets in it before sliding the assembly into the mu-metal tube.) The final product, which takes the form shown in Fig. 5, can be expected to be used for contiguous-disk chips in the future, since the device packaging requirements will remain essentially unchanged from existing technology.

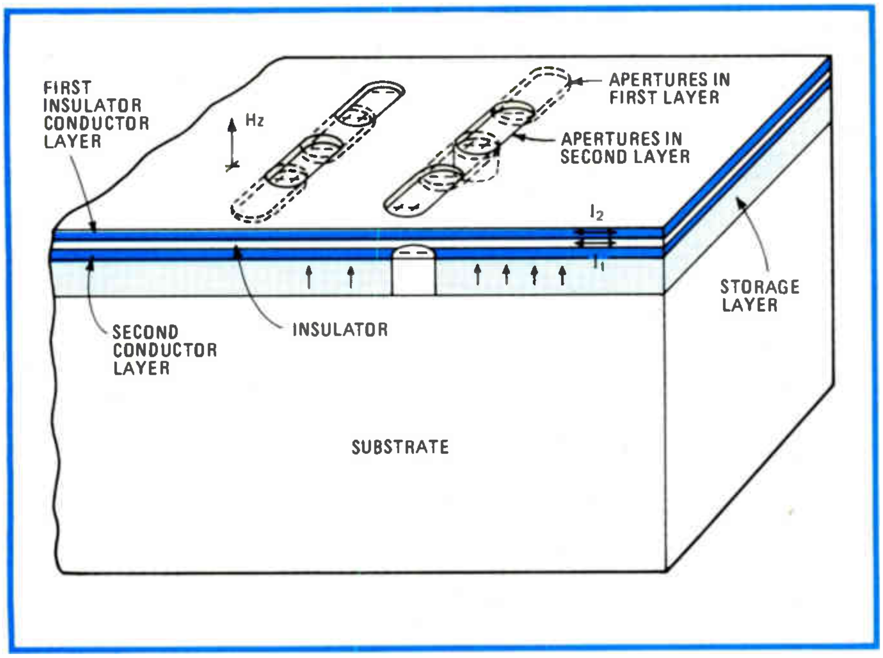
Although requiring no coils, the proposed current-access bubble memory would be packaged in a similar (albeit smaller) Mumetal shield; but the chip-carrier would likely be multilayered to provide a return current path to compensate for the bias-field variations produced by the on-chip currents. Also, the die's higher power dissipation might require special heat sinking to the package substrate, and the high currents might also require special bonding consideration.

Support circuits

Regardless of technology type, a common bubble-memory system will place one or more packages on a card along with the necessary support circuits to form a complete memory system. For a manufacturer to be competitive in bubble-memory systems, he must equip the bubble chip with specialized large-scale integrated support circuits. These LSI chips are indispensable, for by replacing the 20 to 50 conventional semiconductor packages required to realize the memory system, they reduce the required board area by about a factor of eight at the very least—not to mention the cost savings.

The functional building blocks of such a system, which will fit on a board of 9 to 16 square inches, are shown in Fig. 6. Central to the system is the controller, which serves as the interface between the bubble chip and system bus. It generates all of the system timing and control functions and supervises the handshaking operations required to access and transfer data between the system bus and the bubble memory module. The controller currently available for Texas Instruments Inc.'s 92-K bubble interfaces with one bubble device only; more recently designed controllers, such as Intel Corp.'s 7220 controller for its 1-megabit bubble chip, will operate up to eight of these devices in parallel.

The function driver chip produces the control currents required to generate and replicate the bubbles, as well as to transfer or swap them between storage loops and input or output tracks on the chip. In the past, the driver chip current levels have been made to track the temperature



4. No coils. Eliminating the coils of field-access bubbles, the current-access technology proposed by Bell Laboratories relies on conductive sheets to produce drive fields. Pluses include high data rate, bidirectional propagation, and a density similar to that of contiguous-disk memories.

of the bubble package so as to improve performance. While no longer absolutely necessary for recently designed bubble chips, that strategy is likely to be continued as it will extend the operating temperature range of the memory.

The sense amplifier converts the analog output signals produced by the magnetic bubbles into a TTL-compatible data stream, which is transmitted by a serial data bus to the controller. The controller partitions the addressed page into 8-bit bytes and transfers them to a first-in, first-out buffer in readiness for future accessing over the system data bus.

For low-power memory systems, the circuits that drive the X and Y coils can also be integrated; larger systems will require discrete power transistors to drive the coils. In most cases, out-of-phase triangular wave signals in the coils produce the rotating field. For a current-access system, high-current conductor drivers will be needed.

Component considerations

Several basic component functions are required within the bubble memory chip itself. Basically, they include generation, transfer (or swap), replication, and detection. Those components place various constraints on system requirements and hence affect the chip organization indirectly. By and large, generation has the least influence because it uses low voltage and few generators are required on a chip. It is normally achieved by nucleation—creating a bubble domain—under a current conductor. With proper design that technique appears usable for bubbles as small as 1 μm. Nucleation of 1-μm bubbles has been demonstrated in connection with contiguous-disk devices at current densities of less than 10^7 amperes/cm^2.

All remaining components play a more important role in determining what organization is feasible and also optimal. The reason is that the organization must minimize the high system supply voltage needed by a large chip, and that voltage is directly determined by component currents, bubble size, and the number of series-interconnected components.

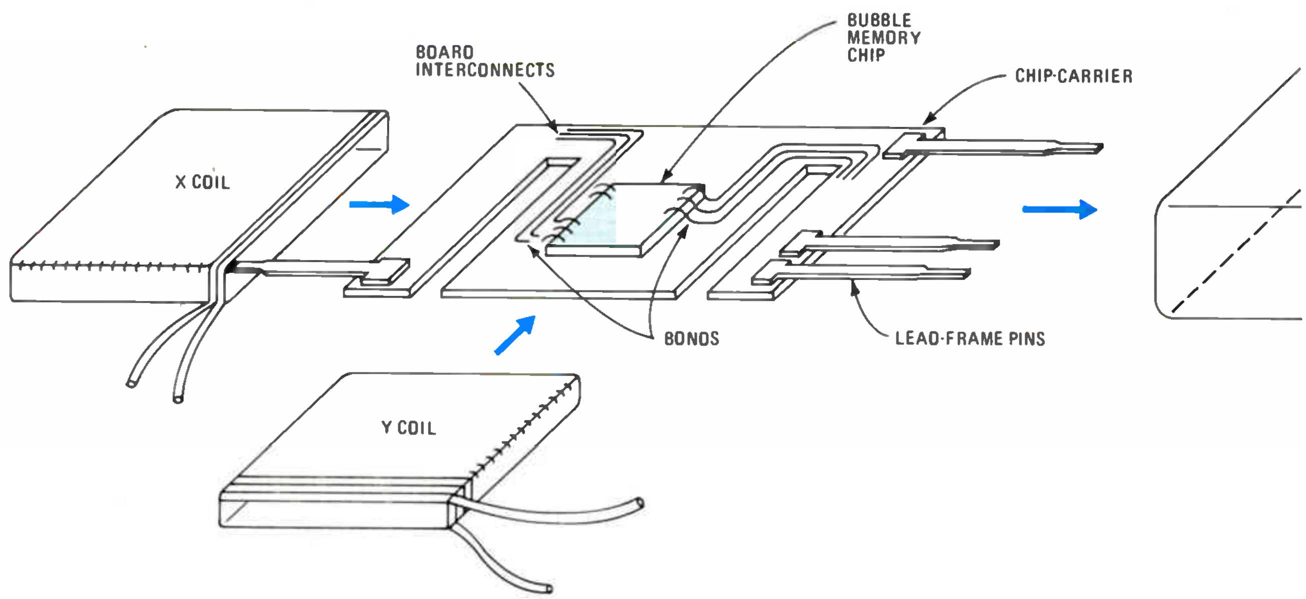
Replication—the splitting of bubbles to produce two for each one—generally requires three to four times the current needed to transfer (or swap) them from major loop to minor loop, making it more difficult to deal with as the number of minor loops—and hence the number of gates in series—increases with chip capacity.

Figure 7 shows the voltages required for a 400-mil-square conventional field-access chip. For a given capacity N, the number of minor loops is assumed to be $(N/2)^{1/2}$ and the length of each 2 $(N)^{1/2}$. Capacity N is 256 K for 3.3-μm bubbles and 1 megabit for 1.8-μm bubbles, as indicated on the figure. Since N is of course proportional to the square of the bubble diameter, intermediate values of the capacity can be inferred. Assuming each loop contains a series-connected gate of 10 squares of equivalent resistance, the results indicate that a 35-V supply is required for replication for 256-K or larger capacities. However, because the duty cycle of that component is less than 1/256 of the time, it is possible to use voltage-boosting techniques to render the power supply requirements less severe.

Minimizing voltage needs

Rockwell employs such techniques in its RMB256 bubble memory, relying on ±12-V supplies to produce the necessary replicating pulses. Texas Instruments has instead divided the replicate line in half and uses a 16- or 20-V supply. Since +5 and +12 V are standard in a microprocessor-based system, those devices may both be less desirable than others. A third possible solution for a 256-K chip is to pair higher-conductivity conductor metal with voltage-boosting techniques to reduce the supply voltage to ±12 V, thus avoiding altogether the complexity of having to split the replicate line.

The supply problem becomes even worse in relation to the 1-megabit chip. In that case, even the transfer (or swap) gate voltage is difficult to produce with a +12-V



supply. One way to circumvent the problem is to organize the chip as a 256-by-4-K device instead of a 512-by-2-K part. That is just what Intel has done for its 1-megabit 7110 part. The main disadvantages of that approach lie in the lengthened access time and longer testing required, due to the increased minor-loop length.

A parallel solution

Another strategy would use a higher-conductivity conductor and divide the replicate conductor in half. Because the current margin for replication is typically ±20%, it is feasible to connect the two sections in parallel without sharply reducing yield as a result of resistance mismatch. Moreover, with a multilayer chip-carrier (like the one Intel uses), the extra interconnections necessitated by the split conductors can be made easily without adding any pins to the package. Several companies are now exploring various alternatives to aluminum-copper-alloy conductors to make feasible a 512-by-2-K loop scheme. Rockwell recently reported on results with silver and Plessey Ltd. its with gold.

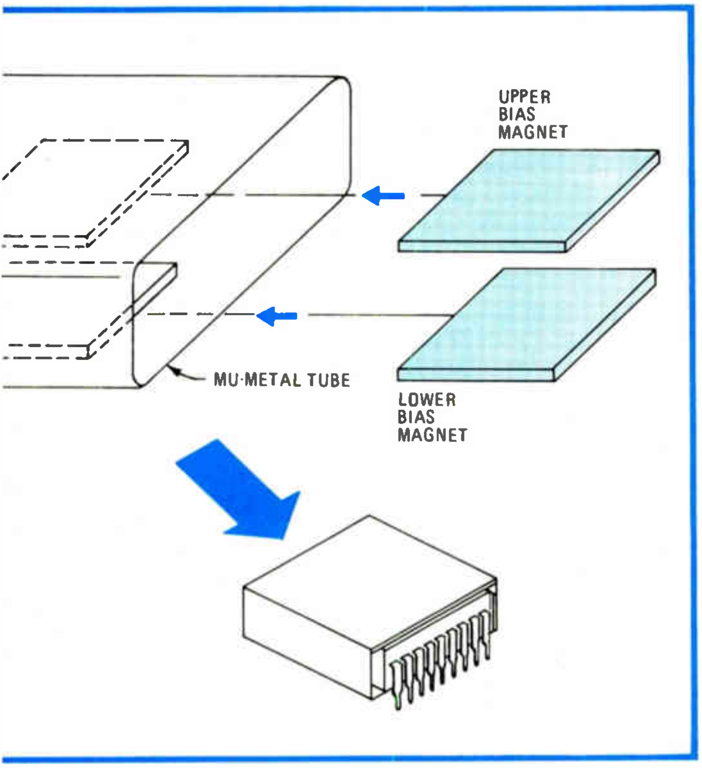
The component availability for contiguous-disk devices is much less certain than for conventional devices because of the relative newness of the technology. Still, for 2-μm bubbles, all the required functions have been demonstrated except for replication. Replication is more difficult in contiguous-disk devices because in them, unlike conventional structures, the propagation elements have very localized poles, which do not stretch the bubbles to ease the task of dividing them in half. Hence, a separate current conductor is needed to stretch the bubbles, complicating the design. It is likely, therefore, that if a replicator is developed for contiguous disks, it will take up considerable real estate, so that it will probably appear not in minor loops but rather in the major loop, where real estate is less restricted.

Several different transfer (or swap) gates have been demonstrated for 2-μm bubbles, some with resistances as low as 2 to 4 squares and with typical operating currents of 40 mA. This places a 1,000-loop-by-4-K contiguous-disk major–minor-loop chip with a 12-V supply well within grasp, assuming that scaling does not increase the component current. Early 1-μm work by IBM Corp. with a slightly different switch design seems to indicate that about 4 squares of resistance and a current of 70 mA would be required, which would still be compatible with a 12-V system that uses voltage doubling.

A 4-K loop has such a long access time, however, that a pair of 2-megabit chips might more advantageously be placed on a die to realize the 4-megabit chip. An alternative that decreases the access time is bidirectional bubble propagation, which is well within the capabilities of contiguous-disk devices. Bidirectional bubble motion would halve the access time of a large-capacity chip.

Detector demands

Detection of bubbles also plays a role in determining what organization is feasible or desirable—particularly for conventional field-access technology, where the less sensitive magnetoresistive thick-film detector is employed. Detector problems stem from several sources. As a rule, sensitivity decreases with bubble size and this, again, begins to boost power supply requirements, especially when it is coupled with the generally large resistances required for voltage drops great enough to yield a satisfactory output. Also, the threshold range appears to be better for detection of alternate bits than for consecutive bits because the overlap of bubble signals is reduced. However, in this case the reproducibility of the threshold setting depends upon matching active and dummy detec-



5. Packaging. Conventional field-access bubble memories all share a similar packaging scheme. E-shaped chip-carrier is surrounded by coils and slipped into Mumetal tube with bias magnets. Package will be employed for future contiguous-disk devices as well.

tors geometrically as well as in permalloy properties: the closer together the two detector elements are, the better.

The above observations have led to several different approaches to chip design. Probably the most conservative and most expensive scheme is reflected in Rockwell's RBM256 part, where alternate bits are detected with side-by-side active and dummy elements. The disadvantage of that approach is that three more pins are required, along with additional sense electronics. Texas Instruments, on the other hand, uses one consecutive-bit detector in its 256-K part. It puts a guard rail between the active and dummy detectors, which are several propagation periods apart. The latter approach is preferable to the alternate bit approach since it doubles the data rate, but it is more difficult to design and process and therefore will affect yields.

For the thin-film detectors used in contiguous-disk devices, consecutive-bit detection should be straightforward, provided the stretching process does not narrow the margins (that is, reduce the bubble's stability range) too much. By elongating the propagation period in the neighborhood of the current loop used for stretching, the problem of detection should be less organizationally restrictive with a thin-film element than with its conventional thick-film counterpart.

Loop organizations

Their organization into major and minor loops is a key ingredient in the success of bubble memories both because it yields a shorter access time than a simple serial organization (such as that used in the 64-K Fujitsu part) and because it provides a framework for introducing redundancy.

A schematic diagram of a major–minor-loop organization like that used in TI's 92-K chip is shown in Fig. 8a. It consists of a storage area formed by the minor loops and an input-output area provided by the major loop. Redundancy is added to the storage area simply by designing in additional loops so that after final testing a prescribed number of minor loops are good. Generally, about 10% redundancy is required.

A page—the data intended for the minor-loop storage area—is written serially into the major loop via the generator (G) and transferred (or swapped) by a gate (S) in parallel into the minor loops, where it resides until needed. Reading the page involves transferring it to the major loop, replicating it into the detector, and returning it to the minor loops. It is the last step that creates the bottleneck in a conventional major–minor-loop organization. Because data must be cleared from the major loop before another operation can be performed, cycle times tend to be long.

If the chip is designed to retain data in the major loop, then proper address selection can eliminate lengthy access by overlapping page-access and -restore operations for sequential reads, but at a penalty in controller complexity. Also, because the major loop is oriented at 90° to the minor loops, data in the major loop may suffer margin degradation; therefore TI elects to return data to the minor loops before powering the coils down.

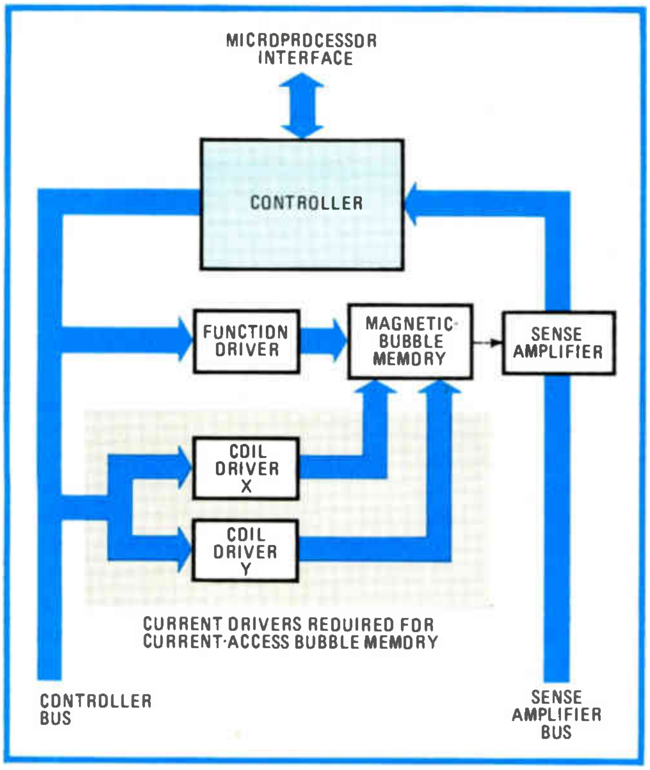
The attractive features of the simple major–minor-loop organization are the low voltage it requires for transfer (or swap) and its ability to be matrix-selected, which reduces the number of system components. If double-period propagation elements are used in the major loop along with consecutive bit detection, the peak data rate for this organization can match the rotating-field frequency.

First variation

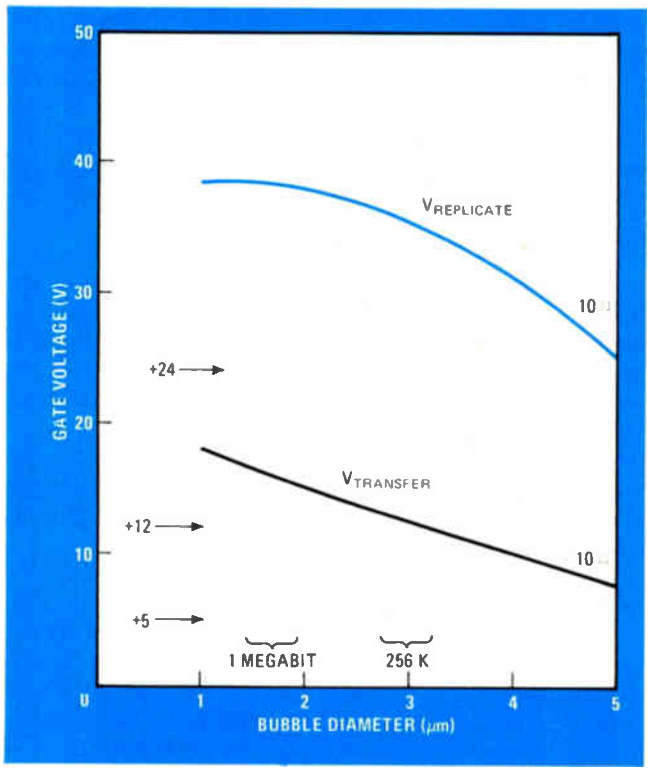
The block-replicate organization of Fig. 8b eliminates the power-down and data-transfer bottleneck of the conventional major–minor-loop organization. In this organization the major loop of Fig. 8a is split into input and output tracks, which are placed at oppposite ends of the minor loops. Because pages are replicated directly into the output track, data is not removed from the minor loops during a read operation. Nor, if a swap input is provided, is data removed for a write operation, and hence the device can power down immediately.

Another important feature results from the elimination of the closed major loop. A read or write operation can be performed as soon as the input and output tracks have cleared, so that the read and write cycle times are short. Also possible are sequential reading and writing of addresses that are physically displaced by these track lengths. The main disadvantage of this organization is the relatively high replicate-line voltage. But as has been pointed out, the problem can be circumvented for 256-K and 1-megabit parts by subdividing the replicate line.

Figure 8c shows a multiple-block-replicate organization comprising two side-by-side block-replicate chips



6. Memory system. Several manufacturers have built large-scale integrated circuits for controlling and interfacing bubble memories. A minimum system comprising bubble chips, controller, function driver, coil drivers, and sense amplifiers fits on a board as small as 9 in.²



7. Voltage requirements. Supply voltages have a strong effect on bubble chip organization. Swap (S) or transfer (T) gate and replicate voltages must be increased as smaller bubbles are used. Voltage-boosting can allow compatibility with microcomputers. Chart applies to a 400-mil-square conventional field-access chip.

having swap lines in common. Some of the generator and detector lines could also be combined and the replicate lines connected in parallel to reduce the number of pins (see below). The features of this organization are essentially the same as that for a single block-replicate chip except that the read and write cycle times (excluding latency) are halved and the data rate therefore doubled.

That is basically the organization Intel has selected for its 1-megabit 7710 part, except that it uses four blocks instead of two and has doubled and folded the length of the minor loops to reduce the number of gates. The two main disadvantages of the multiple-block-replicate are that it requires more pins than the standard block-replicate organization and that the peripheral area is increased, making the chip more susceptible to defects.

Attractive alternative

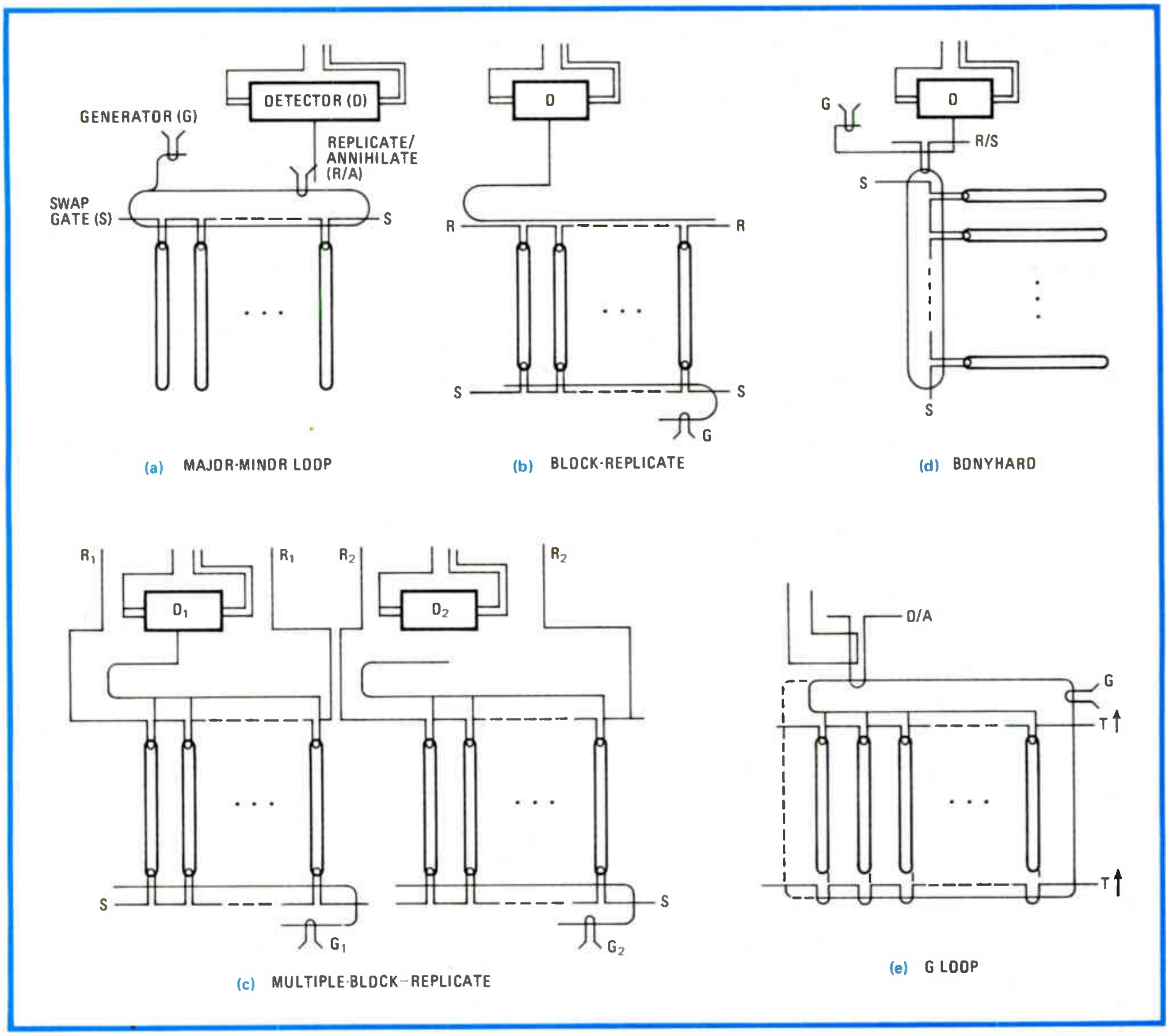
An attractive alternative to the block-replicate structure for large-capacity chips has been suggested by P. I. Bonyhard of Bell Telephone Laboratories. Shown in Fig. 8d, it is basically an improved major–minor-loop organization without the power-down problems of the earlier design. Upon loss of power an address is written into the track that can be subsequently read, allowing the page stranded in the major loop to be returned to its minor-loop location.

As an alternative, Bonyhard proposed that if the minor loops were split in half to form two sets and two major loops were employed, the performance of this organization could be very good. In this high-performance version, sequential page addressing is possible without a break in the data stream, and the access time is halved. However, because there are twice as many minor loops, data-block length doubles and the write cycle time is increased. Connecting the I/O track to the major loops also allows partial rewriting of pages without the necessity of an external buffer.

Because only one replicate switch is employed, the voltage requirements for the Bonyhard organization are low. As originally proposed, the swap lines for the high-performance version were connected in parallel, which would probably diminish yields due to resistance mismatch and the narrow current margins of the swap component. Nevertheless, it is an attractive organization for a conventional 1-megabit field-access device, even though it appears to be losing ground to the block-replicate organization. Still, it may yet gain appeal for contiguous-disk designs if swapping becomes possible, since it requires only a single replicate switch, and even that could be eliminated by employing a nondestructive detector design.

The G loop

As already noted, a replicator does not yet exist for a contiguous-disk device. However, if the major loop of a conventional major–minor-loop organization is cut and returned to the opposite end of the minor loop, an attractive solution to that problem is obtained. Figure 8e presents what, for obvious reasons, is called a G-loop organization. For a read operation, data is transferred out of the minor loops into the G loop where it can be read destructively or nondestructively by a thin-film



8. Organizations. Conventional major-minor loop (a), used in TI's 92-K chip, suffers data bottlenecks and can lose data with power-down. Block-replicate architecture (b) in today's 256-K chips duplicates data into I/O tracks, stores it in loops. Multiple-block-replicate (c) in Intel's chip uses four blocks to reduce cycle times and boost data rate, but a simpler alternative proposed by Bell Labs' Bonyhard (d) is similar to conventional major–minor-loop structure, can return any page stranded in the major loop on power-down to the minor loops upon restart.

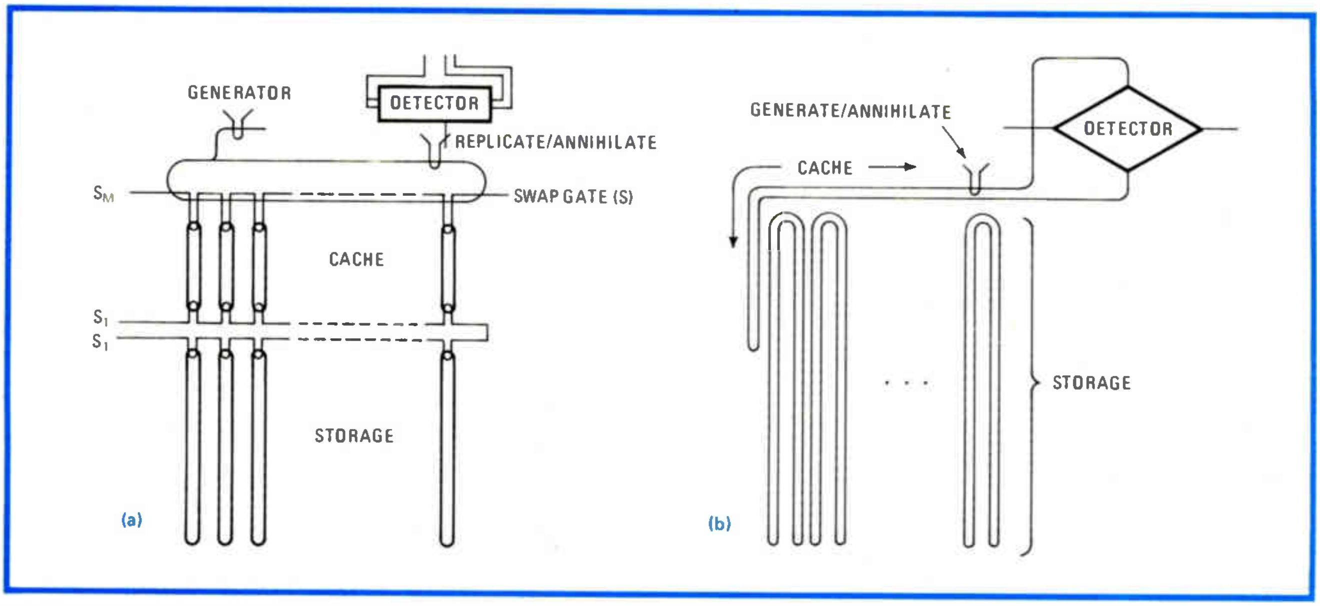
detector employing current-loop stretching and then (if appropriate) returned to the minor loop through the transfer-in port.

The advantage that this organization has over the conventional major–minor-loop organization is that returning data does not interfere with the next read operation. Also, the placement of write after read automatically implies that read-modify-write operations can easily be performed.

The power-down problem can be eliminated by closing the G loop with a return path, shown as the broken line in the figure. Upon powering up, properly tagged data can be returned to its rightful location in the minor loops. A similar organization can be constructed with two-way transfer gates to accommodate bidirectional propagation. The virtues of the G loop are its use of simple components and the low voltage required for the transfer function. On the other hand, its controller design is complex and performance is somewhat low. On balance, it would appear to be an attractive candidate for a 4-megabit contiguous-disk chip. Table 1 summarizes the key features of all organizations discussed.

Synchronizing systems

Since addresses are not normally stored with the data in bubble memories, a power failure will leave the memory address and the controller address register unsynchronized. An initialization procedure is therefore necessary to bring the memory up. One way is by using a dedicated bit or bits in each page of data as a marker; however, the entire memory contents might then have to be read to locate the marker—a process that would take a megabit memory with a 100-K/s data rate all of 10 seconds. A much shorter initialization time is obtained



9. Multilevel. Multilevel architectures can reduce access times. In two-level approach of (a), frequently accessed data is stored in smaller cache loops; the number of levels could be greater. Organization of (b) uses expanded major loop to hold several pages.

by the more conventional practice of providing a dedicated loop that is accessed directly. In fact, most bubble memory manufacturers add an extra loop to their products for addressing purposes. This loop also stores a map of the bad storage loops on the chip, which are masked out. During system initialization, the map data is written into an external buffer memory, which is used later to ensure reading from and writing into only the good storage loops.

Table 2 presents a survey by company of the bubble memory organizations that each of them either is using or has discussed at engineering levels. The rapid development of the technology is illustrated by 1-megabit parts soon available. A 4-megabit chip will probably be announced as early as two years from now.

Multilevel organizations

As chip capacities increase in the future, it is likely that bubble technology will be pushed to maintain or even decrease present access times. The high-performance version of the Bonyhard organization attacks the problem of speed by, in essence, placing two major–minor-loop chips on the same die, each with half the loop length of the equivalent original organization. Another approach employs the equivalent of an on-chip cache. The basis for a cache approach is the observation that accesses to memory are generally localized during the execution of a program. Hence an overall improvement in performance can be obtained if the pages that contain the most recently accessed information are positioned near the read port.

Figure 9 shows two organizations that employ this strategy. In Fig. 9a the storage area of a conventional major–minor-loop organization has been split in two, one part a cache with rapidly accessible pages and the other a longer-loop storage area. The interchange of pages between the two is established by a true swap gate. The most recently used pages are maintained in the cache for easy accessing through the major loop, and any request for a page not in the cache causes an algorithm to be executed that exchanges an inactive page in the cache for the requested page in storage.

In a field-access device this replacement algorithm is complicated by the need for synchronization between the cache and the storage area. However, introduction of an intermediate idling position eliminates the problem. For the newer current-access device the cache and the storage area can be controlled separately, making the cache organization that much more appealing. Bidirectional bubble propagation will, in either case, improve performance but much more so when the storage area can be controlled independently of the cache area.

The two-level organization of Fig. 9a can be generalized to an arbitrary number of levels; it has been done in literature where the organization is sometimes referred to as a bubble ladder. Numerous theoretical studies of its properties have been made in connection with dynamic reordering of data.

Figure 9b shows a diagram of alternative multilevel organization in which the major loop is expanded to hold several pages. Again, this organization is more suited to the case where the major loop and the storage area can be controlled separately and it would therefore be most useful in a current-access scheme with bidirectional propagation.

In both multilevel designs, quite a large number of storage pages must overlie the same cache page to ensure a significant improvement in performance. That limits flexibility in choosing the replacement algorithm and increases controller complexity. In general, reducing access time is an expensive proposition. Given the potentially high data rate of current-access bubble devices, it is likely that a scheme will be found to reduce existing access times for large-capacity chips. Users will then be able to select between expensive, high-performance and inexpensive, low-performance bubble memory chips much as system designers now choose between bipolar and MOS circuits for memory applications. □

Making 100,000 chips fit where at most 6,000 fit before

Multilayer, multichip packages mount on multilayer circuit cards plugged into multilayer boards in IBM 4331/4341 computers

by G. G. Werbizsky, P. Winkler, and F. W. Haining, *International Business Machines Corp., System Products Division, Endicott, N. Y.*

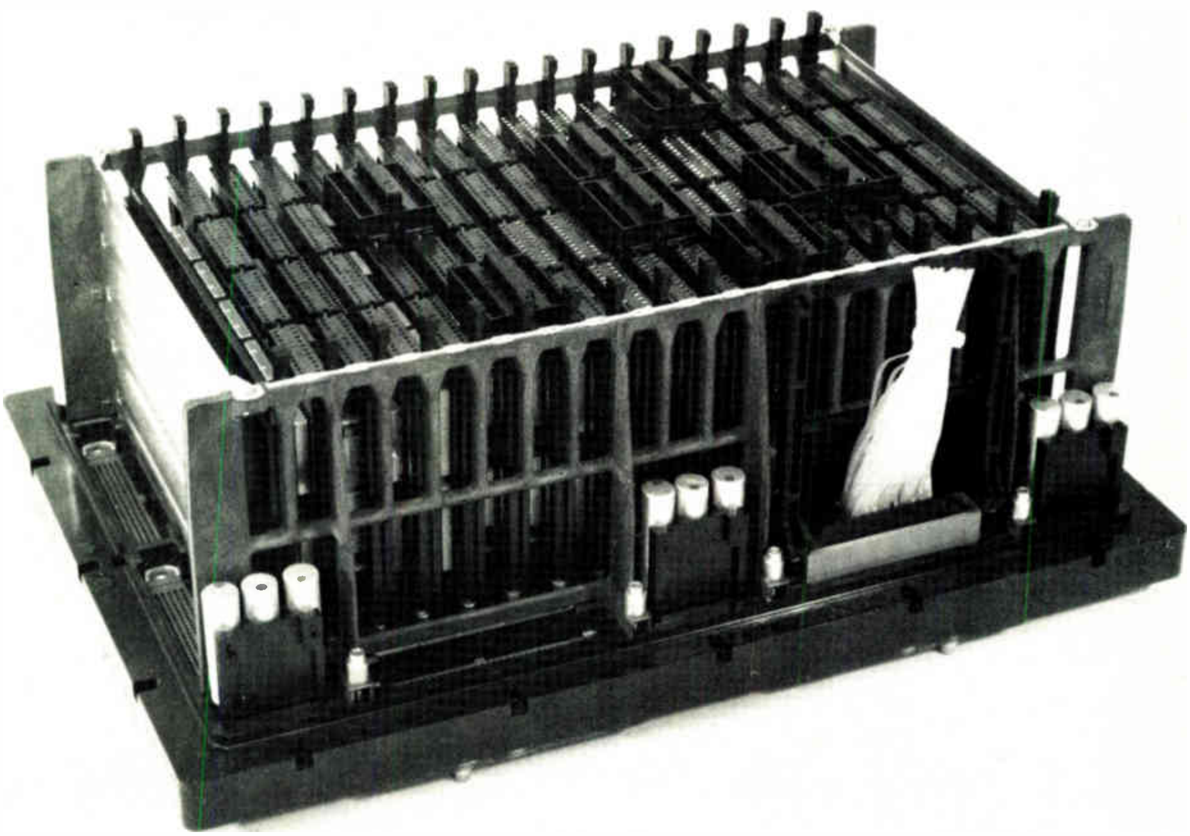
□ Some of today's most advanced packaging technologies are contributing to the success of the new IBM 4331 and 4341 processors. The techniques support the electrical performance required by the new large-scale integrated chip developments, allowing faster machine cycle times; they facilitate servicing; and they also shrink the size of the mainframe cube.

The new 4331 and 4341 systems replace the low end of IBM Corp.'s System/370 mainframe family. The 4331 can hold up to 1 megabyte of main memory and has up to four times the instruction rate of the 370/115. The 4341, with up to 4 megabytes of memory, is 3.5 times faster than the 370/115. The price/performance ratio of the two models is three to five times better than that of the older units.

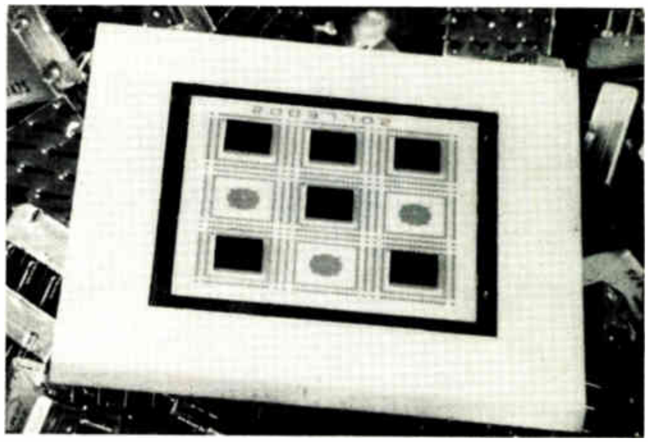
As Fig. 1 indicates, the complete 4331/4341 chip packaging structure houses LSI circuits in:

- Multilayer ceramic modules, which are mounted on
- Multilayer, high-density printed-circuit cards using mil measurements, which plug into
- Multilayer printed-circuit boards using millimeter dimensions and employing
- Special connectors.

By "multilayer" is meant more than just a half dozen



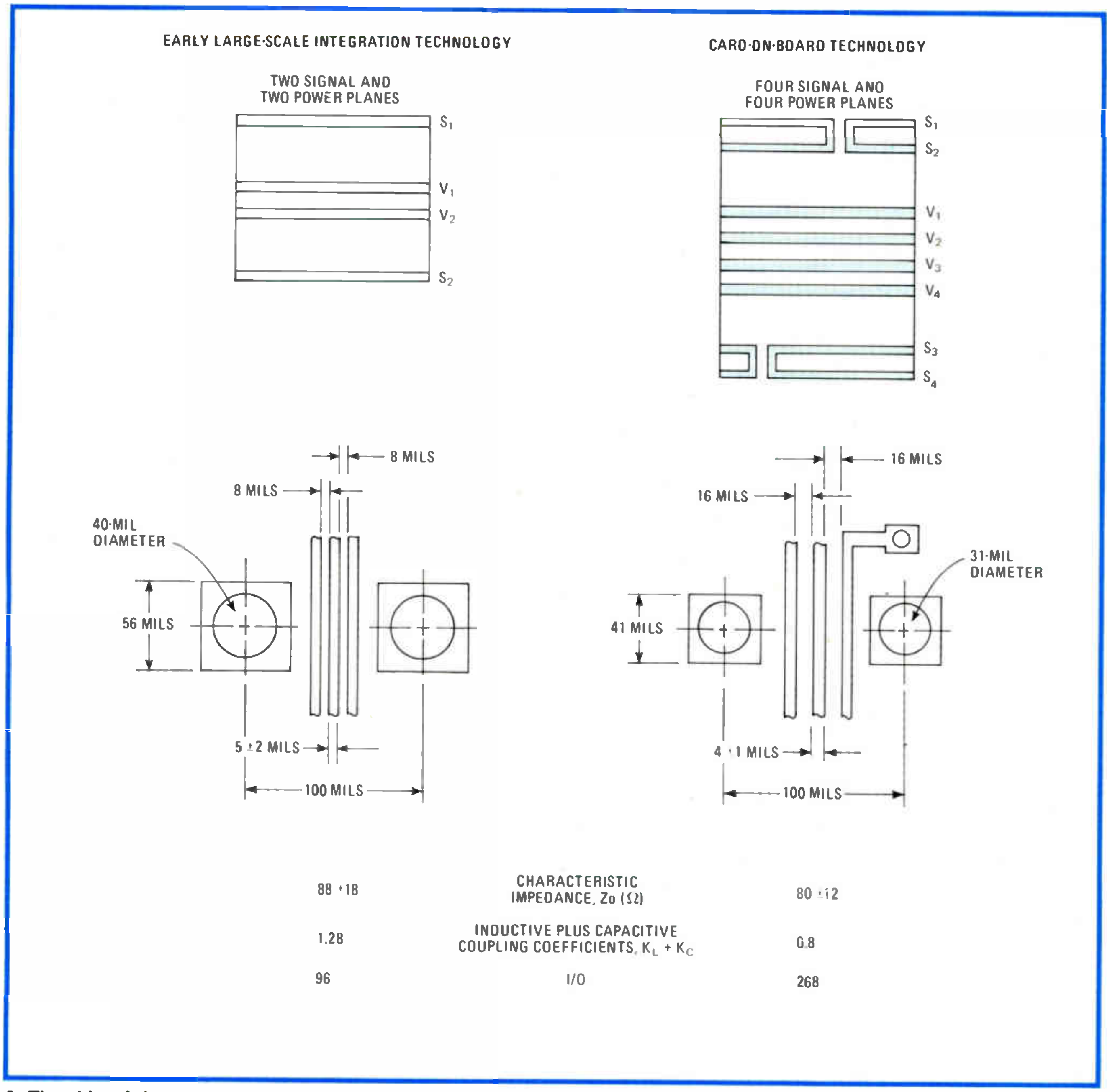
1. Module-on-board. The 100,000 circuits inside IBM's 4331 and 4341 computers employ three levels of interconnection: LSI chips in multilayer ceramic modules are soldered to subsidiary multilayer printed-circuit cards that in turn plug into a large multilayer pc board.



2. Multum in parvo. Typical multilayer ceramic module from a 4331 or 4341 IBM processor can hold as many as nine chips. Measuring 2 inches (50 millimeters) square, it has 361 pins on 100-mil grid and conceals the equivalent of nearly 33 feet of wiring.

layers. The ceramic module has up to 23, the subsidiary pc card 7 or 8, and the main pc board 10 or 16.

The card-on-board package in the new system holds over 100,000 circuits. In the System/370s (which admittedly have the components and performance of their time, the early 1970s), the same size of package has a capacity of between 3,000 and 6,000 circuits. In other words, one complete board in the new processors is comparable to between 15 and 17 boards in the System/370s. This increase in circuit capacity reduces



3. The old and the new. IBM's newer cards (right) have more layers, finer lines, and smaller plated through-holes than their predecessors (left). They also have vias between signal layers. This structure has greater circuit density, lower noise, and a low characteristic impedance.

the mainframe space requirements by eliminating extra input/output gates and the associated interconnecting cables. Moreover, the number of actual wired connections has been reduced to a new minimum.

A multilayer module

The greatest contribution to the 4331 and 4341's high circuit density is made by the multilayer, multichip ceramic modules. These units have up to 23 layers and can carry up to nine interconnected LSI chips. They are approximately 4 millimeters thick and either 35 or 50 mm square.

Each layer of a module begins as part of a continuous cast sheet of ceramic material, which is cut into pieces 175 millimeters (about 7 inches) square, then punched at high speed with holes so that electrical connections can later be made between the layers.

Conductive paste is then extruded onto some pieces through metal masks, forming a wiring pattern unique to a given layer. Stacks of pieces with the required configurations of conducting-line and insulation layers, layer-to-layer connections, and reference and power planes are laminated together and trimmed to form individual modules, which are then fired in a furnace to harden the ceramic. Finally, the upper surface of the module is plated with LSI chip sites.

After electrical testing of the ceramic modules and the attachment of their input/output pins, a number of chips—at most nine but more typically six—are joined to their plated sites using IBM's "flip-flop" solder-reflow interconnection technique. Finally, to protect the chips, a cap filled with inert gas is welded atop the module.

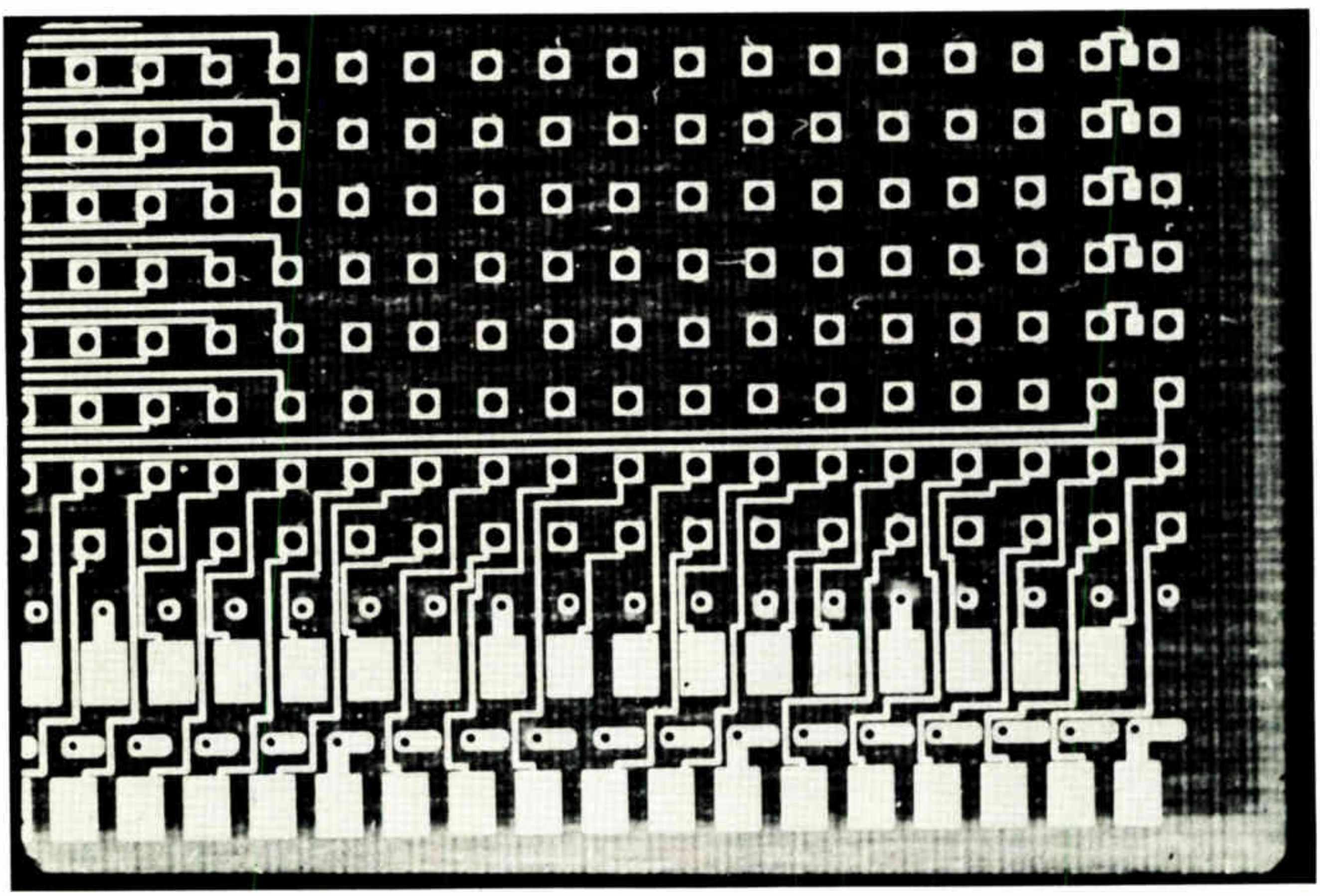
Up to 10 meters (nearly 33 feet) of wiring is concealed within these 4-mm-thick multilayer modules, which can therefore interconnect more high-density logic chips than any earlier IBM circuit modules.

Two module sizes—35 and 50 mm square—are used to meet differing input/output pin needs. The larger has 361 I/O pins, and the smaller, 196. These pins form a grid pattern on standard 100-mil centers, and they also are narrower in diameter than their predecessors in previous module designs. Besides affording high density, the modules do not degrade circuit performance and increase reliability, maintainability and interchangeability. A typical ceramic module is shown in Fig. 2.

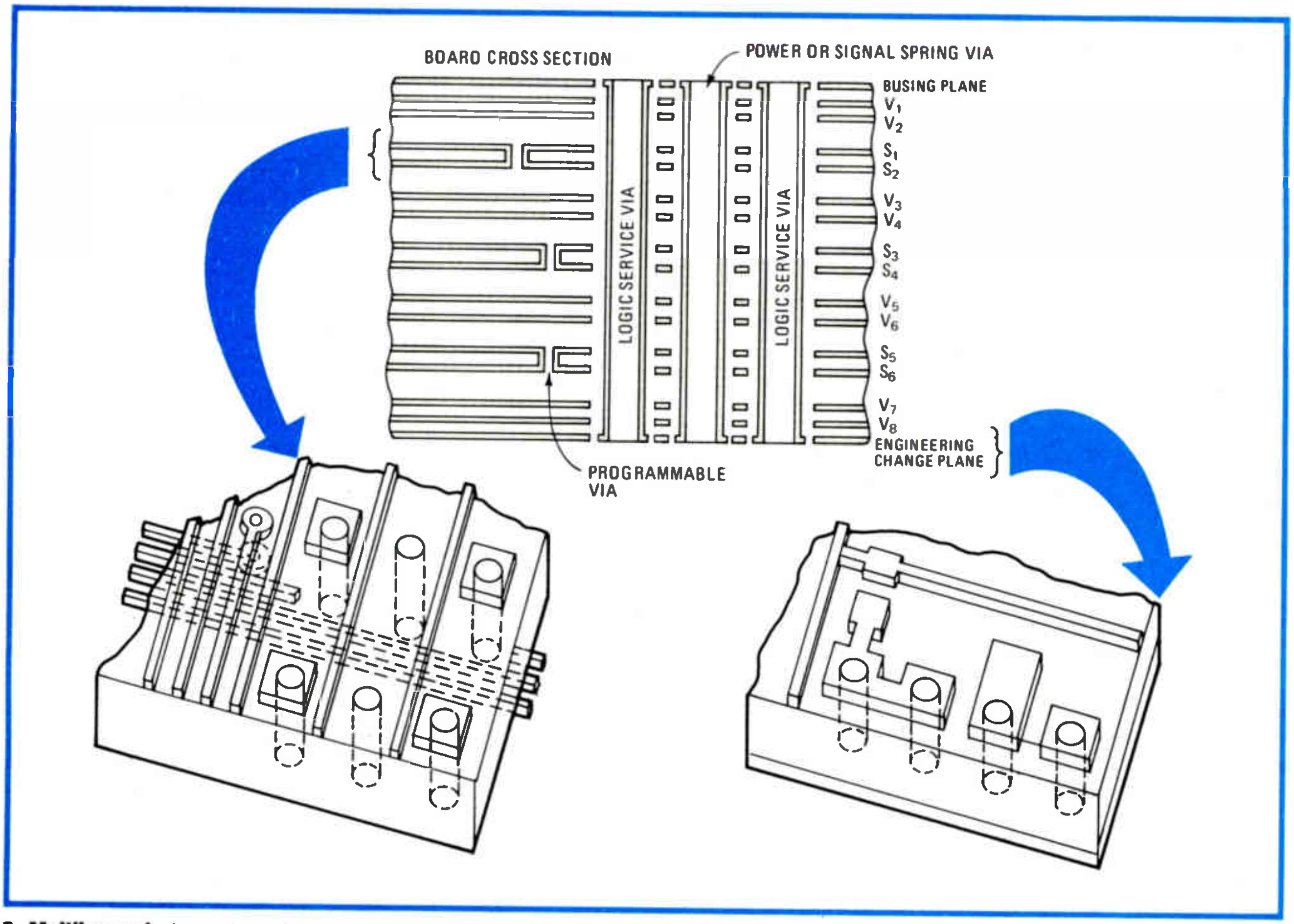
Take a card

The ceramic modules are wave-soldered into plated through-holes in the subsidiary printed-circuit cards—the next level of interconnection. These 3-by-5-inch seven- or eight-layer cards have a grid of plated through-holes also on 100-mil centers.

Figure 3 shows how they compare with earlier IBM circuit cards. Their three or four voltage planes are mostly composed of copper and are subtractively etched. But the four signal layers (two internal and two external) are made by an additive copper plating, since the tolerances of the circuit lines had to be held to ±1 mil to



4. Crowded real estate. A closeup of circuit card shows that three circuit lines can run through the channel between two plated through-holes. The larger holes on 100-mil centers accommodate ceramic modules. Smaller holes are vias between adjacent signal layers.



5. Multilayered. A section of the processor's main board reveals a complex structure. Six inner signal planes, interconnected with programmable vias, and eight power planes are combined with outer special busing and change and rework planes.

reduce coupled noise and impedance to the levels specified. As a result, cards for the 4331 and 4341 have approximately half the crosstalk of System/370 cards, and their signal circuits are maintained at a characteristic impedance (Z_0) of 80 ohms ±12 ohms.

As for the layout of the copper pc lines, three of them may pass through the channel between the copper lands surrounding the plated-through holes in the signal planes (Fig. 4). (Industry practice is two pc lines per channel.) In part, this is because the holes and hence the lands around them are smaller than in earlier IBM cards, a reduction in size made possible by the reduced diameter of the ceramic module's I/O pins.

Some of these plated through-holes lack the lands necessary for attaching modules and serve as program vias, linking signal layers. They provide sites for more than 10,500 signal-line connections per card, as against the 2,747 plated through-hole vias in the System/370s.

The four signal and three or four power planes of the new cards give the designer more flexibility in routing and distributing of signals and power. This flexibility is further increased by the large number of I/O points per card—up to 268 on its connector edge, as against 96 in the /370 packaging structure.

On this connector edge, the cards also feature a unique and disciplined line-to-land wiring distribution system that aids in connecting its signal and power planes to the board and in mating the card's English grid to the board's metric grid. The three lines per wiring channel here permits various combinations of wire routing in order to assure minimal circuit noise.

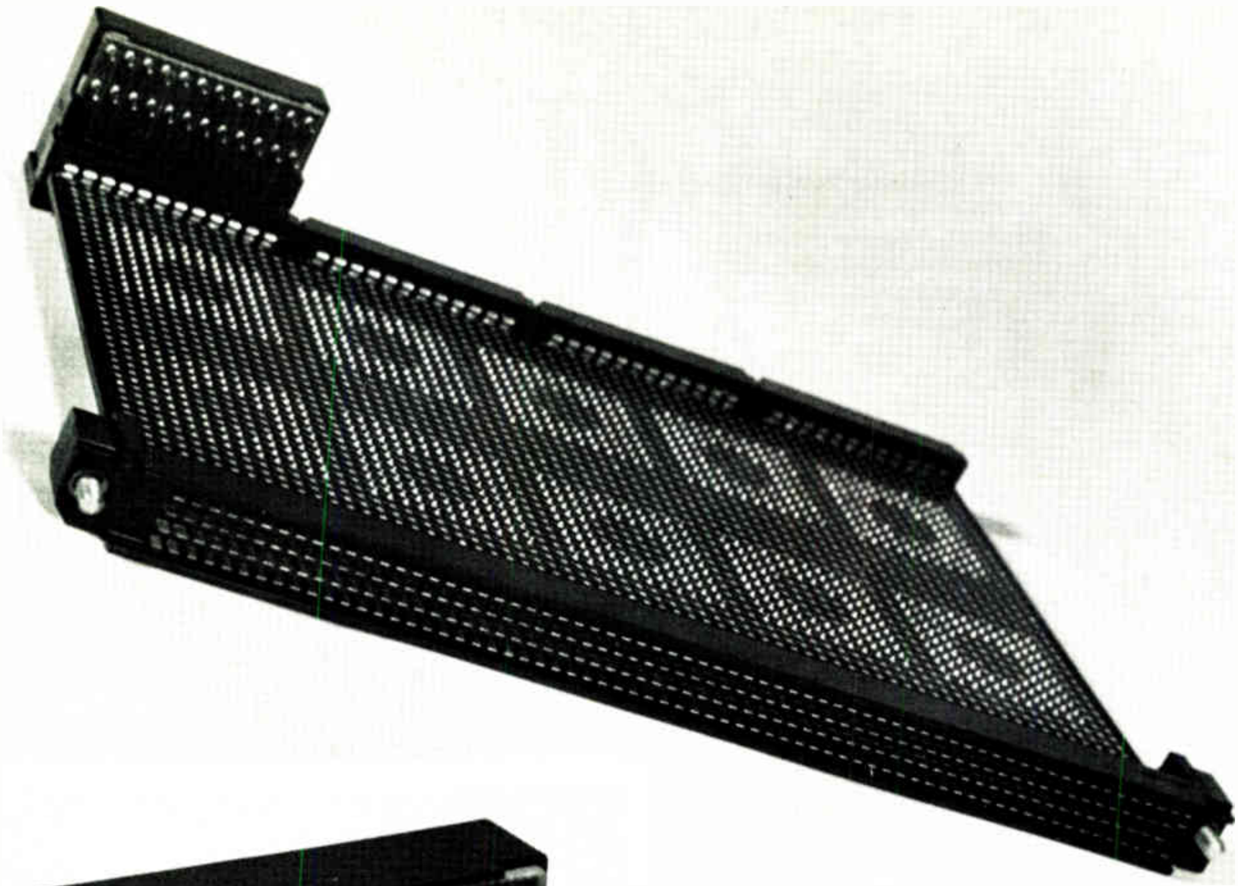
The connection to the main board is made by means of an unusual connector system. Besides including 268 I/O points per card socket, it mates the card's 0.100-inch pitch to the board's 2.5-mm grid; a two-part spring makes the connector more reliable than current IBM designs. Altogether, then, a complete 18-card-position board for the new processors has 4,824 I/O points or 150% more than the 1,920 I/O points in a complete 20-card-position board for System/370.

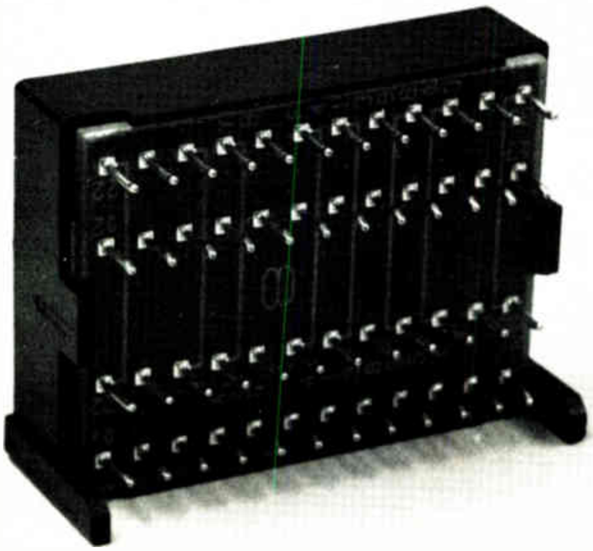
Crossovers between cards

The package also uses card-to-card crossover connectors. They allow circuitry that cannot be fitted on one card to be combined on two cards without tying up interconnections in the card-to-board interface. They were designed specifically for a 17.5-mm metric card spacing (Fig. 6) and are unique in that they provide impedance and noise control with two internal ground reference planes and with ground ties specifically designated for different first-level technologies. The design of these connectors is such as to prevent reverse plugging.

The backbone of the processor package is the main printed-circuit board. It holds 18 subsidiary pc cards and 8 I/O connectors to external equipment.

The pc boards are the first in an IBM processor to use





6. Hole card. This card is plugged into both a bottom-edge connector, which has 268 input/output contacts, and a topcard crossover connector. Shown in detail in the inset, the crossover connector bridges adjacent cards so as not to tie up board connections.

the metric system. Their metric dimensions are in accordance with the recommended industry standard dimensions. There are two board types. One has 10 printed-circuit planes, the other 16—4 or 8 internal power, a plane for engineering changes and rework on the bottom surface, and a special busing plane on the top surface (Fig. 5). The board with six signal planes also uses programmed through-holes to interconnect pairs of signal planes and increase the available wiring. The matrix of plated through-holes on both boards is on 2.5-mm centers. Between the holes on the signal planes up to four printed-circuit lines may run. Consequently, the number of wirable connections that can be made is fully a match for LSI requirements.

The bottom surface of the board accommodates all engineering changes and other overflow wires. Besides redundant vias, it includes pc lines that may be deleted as necessary. This last feature reduces repair time and error during rework (Fig. 7). The engineering changes themselves are made with twisted pairs of 0.0035-inch-diameter wires reflow-soldered to pads on the board's bottom surface. These twisted pairs lower signal noise and have tighter impedance control than do single wires.

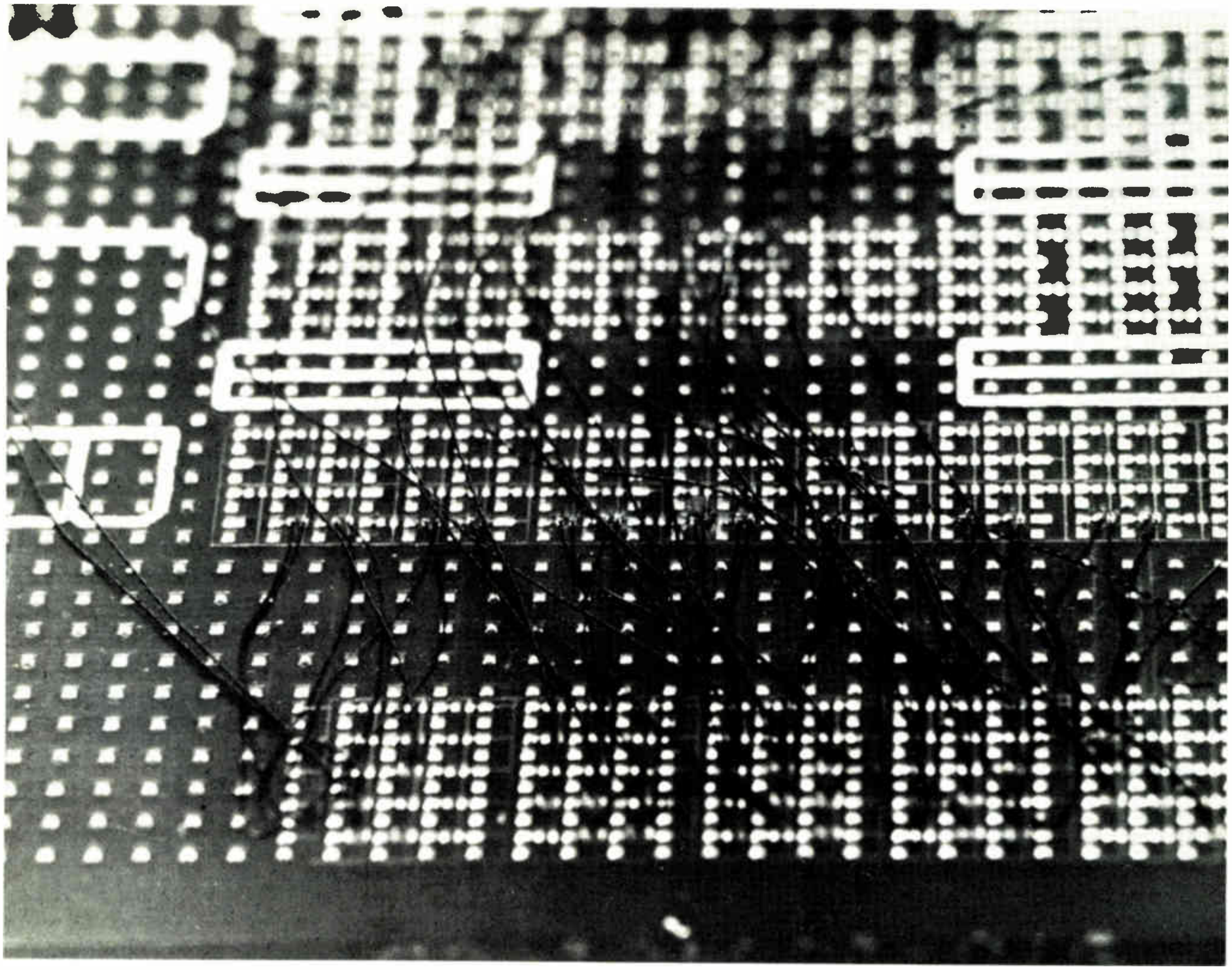
The top surface of the board is a special voltage distribution plane. It is supplied by six special voltage connectors containing three voltage inputs with a total of 18 possible special voltage points.

The board is a field-replaceable unit (FRU)—the first of its kind in an IBM system. It can be replaced in the field in less than one hour.

Tying it all together

A density of 1,000 I/O connections per board is handled by a connector using grouped trilead cable, a flat cable with alternating signal and ground lines. There are 125 I/O connections per five-cable grouping and eight groupings per board (Fig. 1). In comparison, current IBM products have individual 24-contact connectors in 12 positions providing only 288 I/O connections per board.

The new I/O connector uses a split or bifurcated spring contact mounted in the board. A small printed-circuit card with gold-plated tabs along one edge mates with these springs. Trilead cables with 18 signal and 7 ground connections are connected to the other end of the small circuit cards. Each small card has 25 I/O connections



7. Quick change. On this engineering change plane, all changes use twisted pairs of 0.0035-in.-diameter wire that are reflow-soldered to pads on the board. Modifications and repairs to the board can be made rapidly, and complete dismantling is unnecessary.

and five are packaged in one grouping in a molded housing. The cable groupings permit orderly wiring from board to board or from board to I/O connection.

With such a wiring system, the cables can be routed in the mainframe raceways where there is an optium flow of cooling air. Each cable grouping is also equipped with a handle, to ease extraction and reinsertion during service and field testing of the interior of the machine frame. Clamps mounted on a platform hold the grouped trilead cables fast. The platform lets the cable move but prevents it from interfering with board replacement.

In this new packaging system, including the carriers, there are many multifunction molded parts, including carriers for the connector pins mounted on the edge of the subsidiary cards and the housing on the main board for the cable groupings. The housing also holds two captive screws that lock into a metal retainer bar mounted on a board stiffener. When engaged with the retainer bar, the screws actuate the connector with a scissors-like action. Thus contact is made with up to 268 I/O connections using a minimal force that is less than the stresses incurred with a conventional straight plug connector.

The board stiffener is a plastic frame epoxied onto the circuit board. Besides adding structural strength, it has marked on it the location points needed for precise alignment of card sockets and precise mounting of boards, decoupling capacitors, power distribution cables, and probe masks. (The probe mask is a transparent plastic overlay perforated with a grid of holes that helps a service technician to locate any node on the main board.) The stiffener is molded to precise tolerances and enables all of these functions to interact without interference or error during assembly and servicing.

A combination molded card-holder, actuation tool guide, and wire retainer in one molded part permits rapid and precise location and the engagement of each card to the proper position on the board.

Mixing metric and nonmetric

Intermixing metric and nonmetric versious of cards is done with an adapter. IBM system/370 technology cards with 96 edge I/O connections may be plugged into the metric board by using a 96-edge-connection adapter that converts the nonmetric grid pattern into a metric grid pattern. In addition to the latest level of advanced-technology components, the machines use compatible modular cards and boards from current technology. □

Floating current source drives automatized test fixture

by Richard M. Fisher
ADT Security Systems, Clifton, N. J.

This generator provides a programmable current to drive any load, making the unit ideal for production-line testing. Because the constant-current source floats—that is, is not connected to ground—it can drive loads energized either by positive or by negative potentials of as much as 90 volts.

The output current is resolved to 50 microamperes by the 10-bit input to a digital-to-analog converter (a). The maximum current that can be delivered to the load is slightly more than 50 milliamperes.

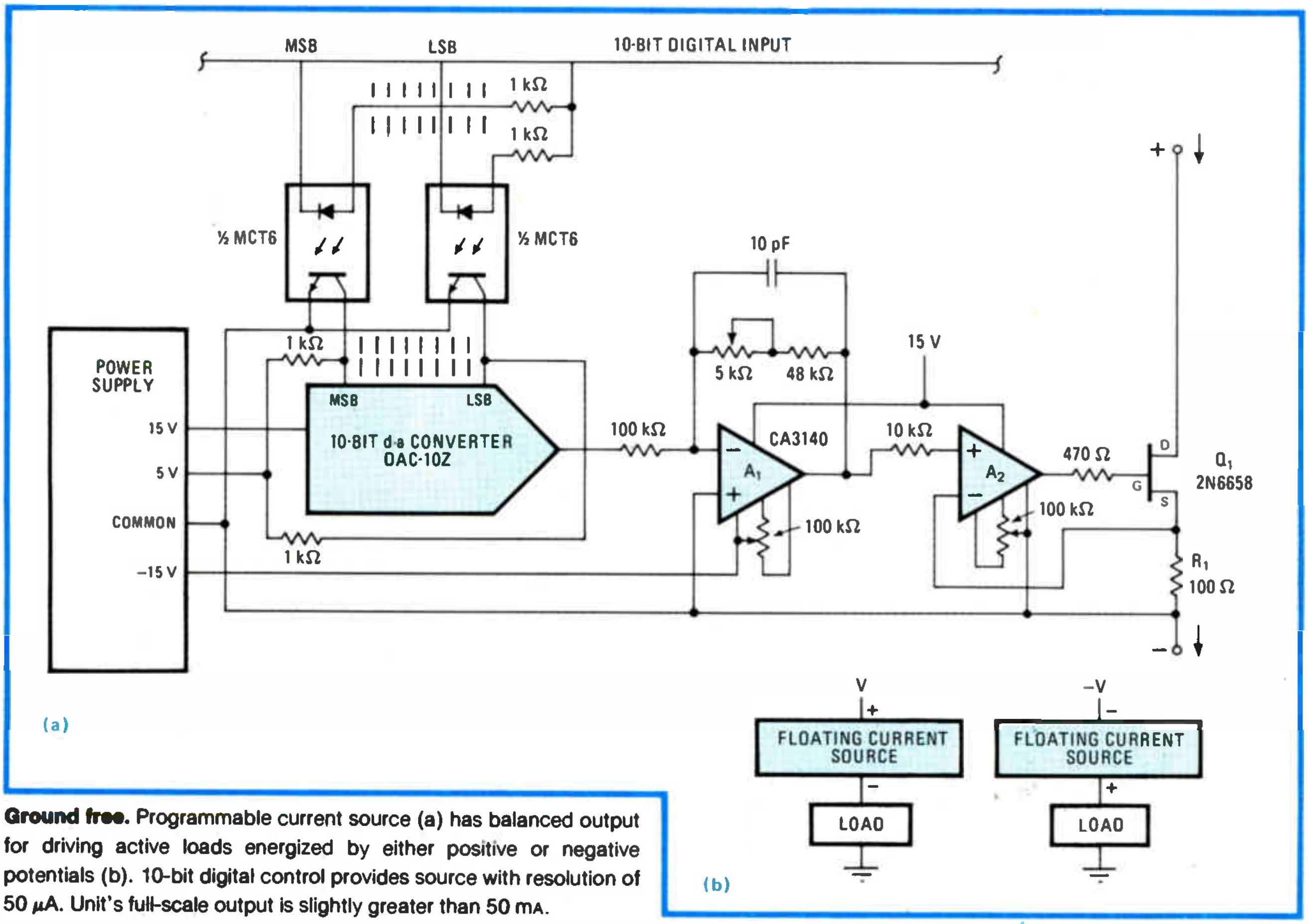
As shown, the 10-bit command input is transferred to the d-a device through optocouplers, thus isolating the DAC-10Z from ground paths under virtually all conditions. Note the 5-, +15-, and −15-V potentials for the generator are obtained from circuitry associated with the isolated secondary winding of the transformer in the power supply.

Operational amplifier A_1 inverts and scales the output of the d-a converter. The maximum output voltage from the converter is −9.99 volts and results in a full-scale output voltage of 5.115 V from A_1. A_2, in conjunction with R_1 (= 100 ohms), thus provides a full-scale output current of 51.150 mA.

The V-groove MOS field-effect transistor, Q_1, serves as a voltage-to-current converter. Q_1 performs the conversion at high accuracy, because the V-MOS device requires no gate current.

As for using the current source, implementation is easy with any energizing potential. If the device—the load—under test is driven by a positive voltage (b), it is necessary to connect the generator's positive output to the supply voltage. The negative port of the generator is brought to the load.

For negative potentials, the situation is similar, with source's positive terminal being connected to the load as shown. The negative port is connected to the supply voltage. □



Ground free. Programmable current source (a) has balanced output for driving active loads energized by either positive or negative potentials (b). 10-bit digital control provides source with resolution of 50 μA. Unit's full-scale output is slightly greater than 50 mA.

Counter banks stagger radar's pulse rate

by Prakash Dandekar
Tata Electric Companies, Bombay, India

In many radar applications, the instantaneous pulse-repetition frequency must be varied in an orderly fashion to improve the read-out accuracy of the system's moving-target indicator. Considerable circuitry is usually required to achieve the so-called staggered operation, but as shown here, two sets of synchronous counters can be easily connected to control the prf over any range, while providing superior MTI performance.

Normally, designers resort to transmitting pulses at each of three selected periods only, in order to simplify circuitry. Specifically, a popular technique is to transmit a group of three 1-microsecond pulses spaced at 1, 1.1, and 1.2 milliseconds repeatedly. When this is done, however, the filtered output of the MTI is not uniform and so—aside from causing discontinuities in the curve of MTI filter output versus target velocity—this method creates blind velocity points, or ranges over which velocity cannot be determined accurately.

With this circuit, a perfectly smoothed response is achieved by increasing the number of staggered pulses per given time. Thus in this case, a group of 200 pulses, each having a time between pulses of (1,201 − M) micro-seconds, where M denotes the Mth pulse of 200, are generated.

As shown, 12-bit counters A_1–A_3, comprising the main counter chain, advance at a 1-megahertz rate. When the counter reaches its maximum, the carry output of A_3, serving as the synchronous output, is generated.

The same signal is used to preset the main counter to a 12-bit binary number, N, which is determined by the state of the offset counter A_4–A_6. Because A_4–A_6 is also clocked, this unit is incremented with every sync pulse, so during each cycle the main counter is initialized at a higher value than it was previously. Thus the repetition time is reduced by 1 μs on each pass.

Note that the offset counter is initialized at a minimum value of $B51_{16}$ (see A–D inputs of A_4–A_6) and advances to a maximum of $C18_{16}$ (= 2^{12}) before it is reset by logic gates G_1–G_3. Thus, the difference between the counter's maximum and minimum is 200 counts, meaning the instantaneous pulse-repetition rate will vary from 1,200 to 1,001 microseconds. The maximum and minimum values may be easily changed, however, so that any pulse-repetition frequency range can be set.

When the counter reaches 3,096, corresponding to a rate of 1,001 μs, A_4–A_6 is loaded with $B51_{16}$. The rate becomes 1,200 μs once more, and the cycle is repeated.□

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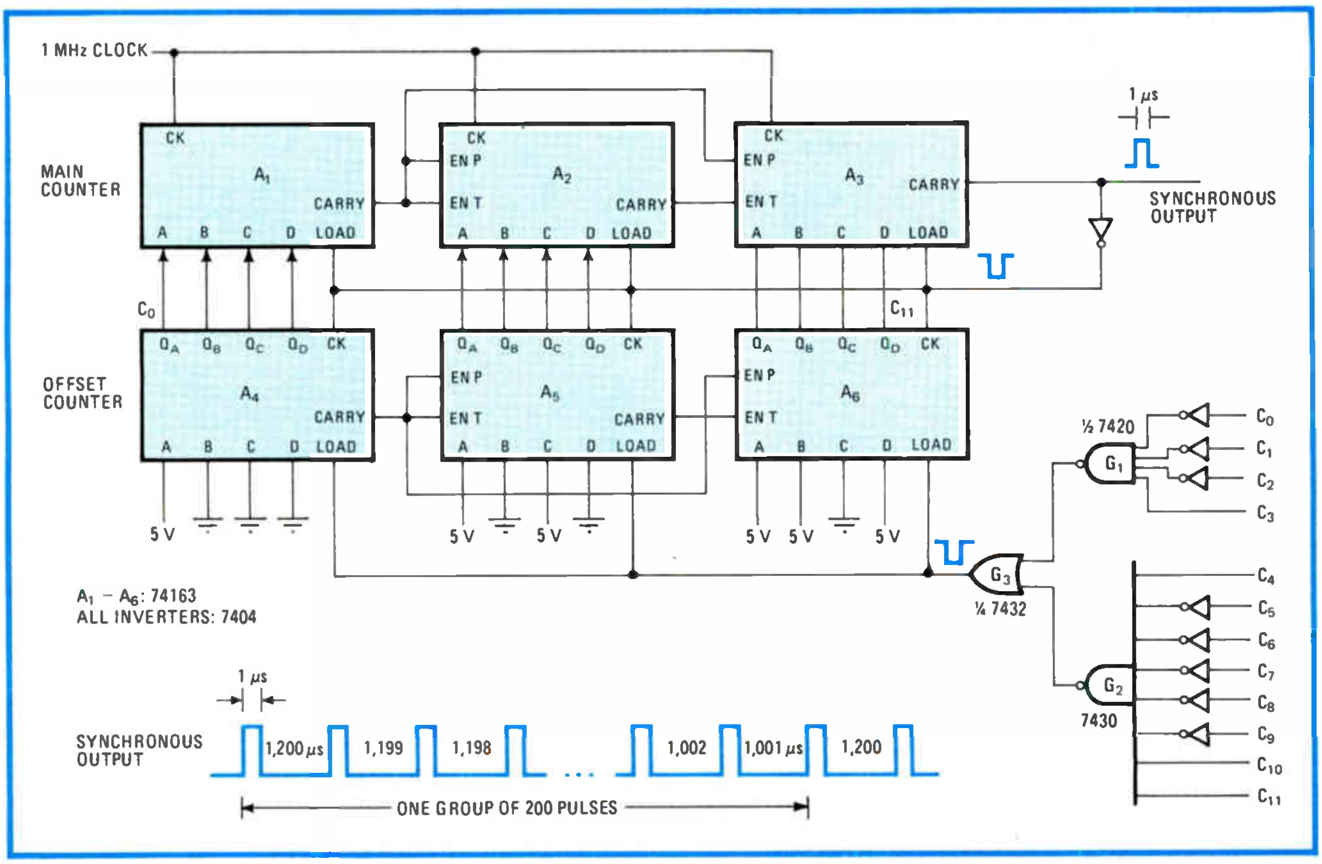

Smooth staggering. Two 12-bit counter chains generate a group of repeating N pulses spaced at (1,201 − M) μs, where M denotes the Mth pulse of N. for incremental staggering of the radar-pulse rate. Master clock sets absolute value of maximum pulse-repetition frequency.

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035214	OE-1		$16.35			
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Modulating the flyback inverter reduces supply's bulk

by Vladimir Brunstein
Nova Electric Manufacturing Co., Nutley, N. J.

The cost, size, and weight of an inverter will be reduced if a flyback transformer, modulated by a high-frequency carrier, is configured in the inverter's output stage. Modulating the flyback transformer is more efficient than attempting to modulate push-pull or bridge circuits, as is sometimes done.

The two subassemblies that are most difficult to miniaturize in the standard inverter are the output filter and transformer. But while the output filter can easily be simplified in a number of ways, the dimensions of the power transformer are determined mainly by the operating frequency.

The obvious solution to reducing the volume and weight of the transformer and the number of filter components, then, is to convert the dc input to a high frequency, such as 20 kilohertz. Here the harmonics of the output signal will be significantly higher than the demodulated frequency, and so a simple low-pass filter can be used to recover the desired 60-Hz waveform.

Using the flyback scheme brings an additional simplification, compared to a push-pull or bridge configuration. The recovered voltage on the secondary of the transformer will be amplitude-modulated, and only a capacitor will be required to obtain the low-frequency component.

As shown, a 60-Hz sinewave voltage is required to drive the flyback transformer via an error amplifier and pulse modulator and also through a power-driver connected to Q_2. Details of these blocks vary with individual requirements and so are not shown in detail here. Picking the right ferrite core is a subject in itself and has been discussed in various papers.

In general, coils T_{2a} and T_{2b} charge during the time interval t_1, and discharge through the load resistance R_L during t_2. Note that an inexpensive optical coupler may be used to replace T_{2b}. The voltage on the transformer secondary will be:

$$V_L = \eta \frac{n_s}{n_p} \frac{\tau}{1-\tau} E \qquad (1)$$

where:

η = efficiency of the power stage
$\tau = t_1/T$
t_1 = turn-on time for transistor Q_1
T = commutation period $t_1 + t_2$
E = dc input voltage

It is seen that the equation lends itself to achieving the end solution, for if the duty cycle is varied by the sine wave while keeping the turn-off time of Q_1 constant, then the peak value of the secondary will follow the sinewave reference as shown in the timing diagram.

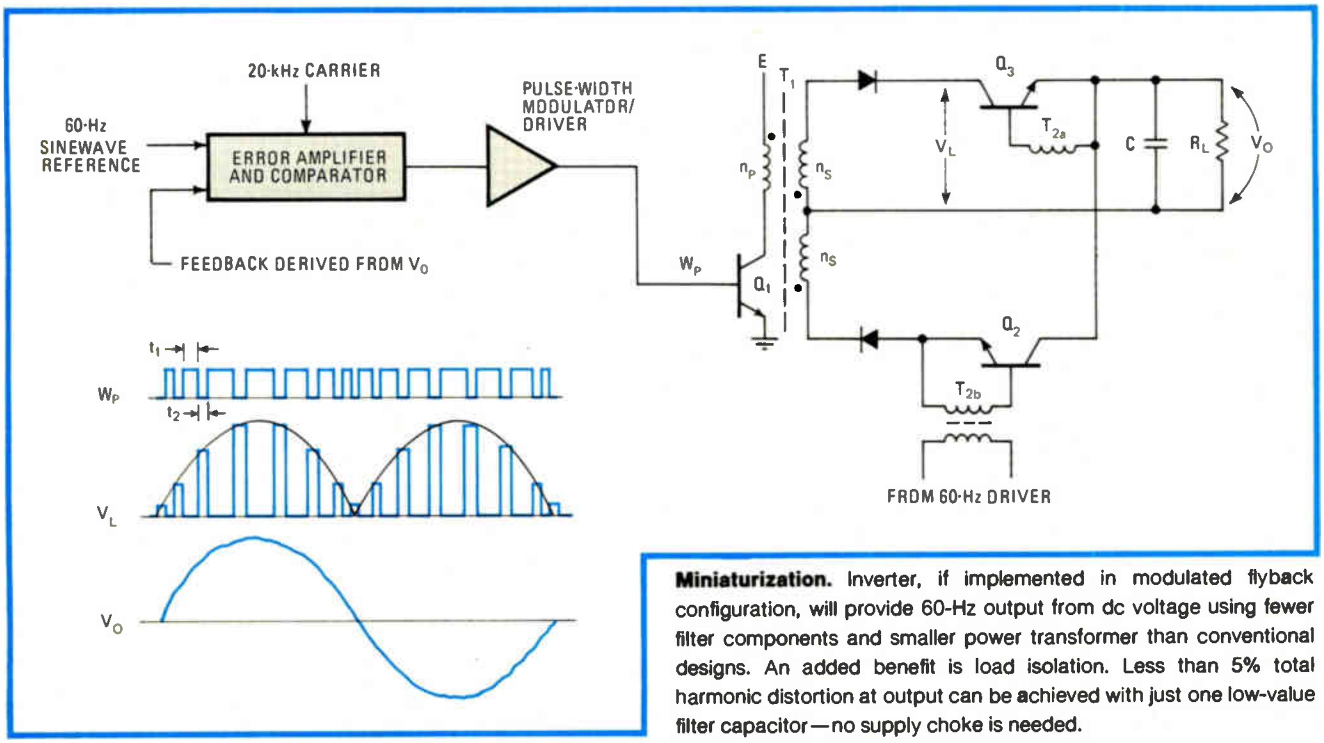
This action results if $t_1 = k_1 \sin \omega t$, for in that case Eq. 1 becomes:

$$V_L = K_2 \sin \omega t \qquad (2)$$

where K_1 and K_2 are constants.

In reality, one half of the sine wave would normally be inverted, as shown for V_L. Q_2 and Q_3 act as 60-Hz synchronous commutators serving to restore the original wave shape.

Note that only a relatively small output capacitor, C, is required for filtering—no choke is necessary. Total harmonic distortion at the output is less than 5%. □



Miniaturization. Inverter, if implemented in modulated flyback configuration, will provide 60-Hz output from dc voltage using fewer filter components and smaller power transformer than conventional designs. An added benefit is load isolation. Less than 5% total harmonic distortion at output can be achieved with just one low-value filter capacitor—no supply choke is needed.

ECL accelerates to new system speeds with high-density byte-slice parts

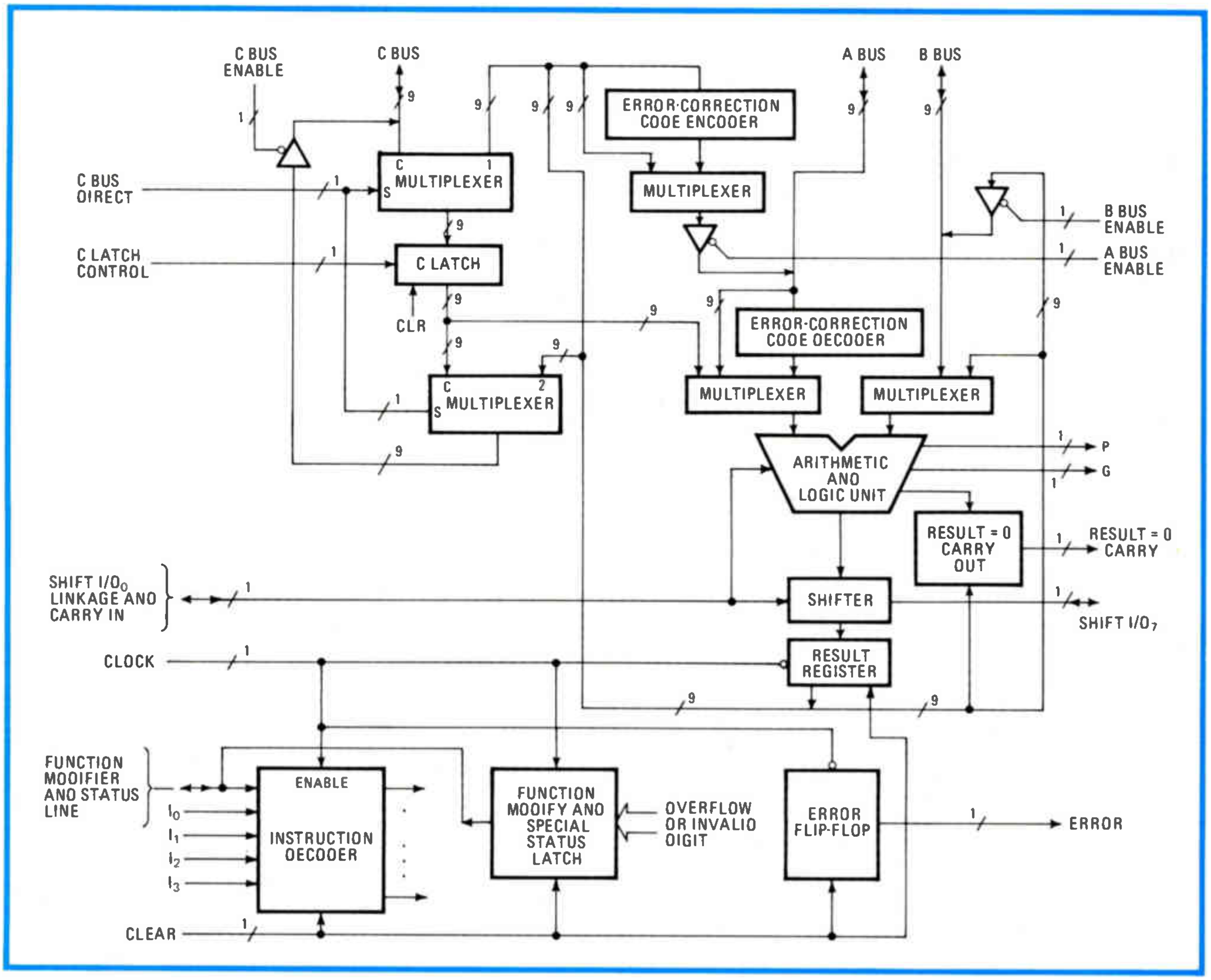
LSI reduces interconnect delays that have throttled ECL, allowing it to overtake available mainframe TTL

by Paul Chu, *Fairchild Camera and Instrument Corp., Mountain View, Calif.*

☐ For the drag racer, torque came first, and tire technology has been struggling to connect more and more of it with the drag strip pavement ever since. For those who race logic, the analogy is short gate delays and the need to develop integrated circuits dense enough to avoid losing the speed in interconnections and package delays.

Emitter-coupled logic (ECL) offers subnanosecond switching times, but at small- and medium-scale levels of integration, it cannot fully realize the edge it holds over the next-fastest bipolar technology, TTL. Widely available large-scale TTL integrated circuits have dominated the fast logic field.

Fairchild Camera and Instrument Corp. has been pushing back the limits of ECL density, however. At this



1. Byte slice. The heart of a new family of 8-bit-slice devices, the F100220 address and data interface unit (ADIU) operates on 8 bits of data plus a ninth parity bit. Its set of 27 instructions includes binary and packed and unpacked binary-coded-decimal arithmetic.

year's International Solid State Circuits Conference, the Mountain View, Calif., company announced the availability of a family of LSI ECL bit-slice parts designed for use in mainframe computers [*Electronics*, Feb. 15, 1979, p. 125]. These four chips, with their 8-bit slices and thorough error-catching facilities, threaten to take the lead in the high-performance logic chase. No commercially available bit-slice parts can touch them.

Bit-slice microprocessors are becoming increasingly attractive to computer engineers as basic logic building blocks. They offer flexibility in instruction set, data-path width, and system architecture while providing the designer with the economic benefits inherent in multiple-use, and therefore high-volume, LSI circuits. In addition, the microprogrammed design required by bit-slice microprocessors aids the engineer: the design method tends to be more structured and easier to follow than that of hard-wired logic.

A growing family

The four members of the Fairchild F100220 family are designed for use in highly bus-oriented systems. They are partitioned to perform functions useful in a variety of applications. By integrating more functions onto a chip and operating on a slice of data 8 bits wide in one chip, interconnections are shortened and interchip signal delays are reduced below those of a 4-bit–slice parts at present on the market. In addition, bidirectional buses are used whenever possible to reduce the number of interconnection paths, hold back the number of pins needed for each device, and save circuit-board space.

For the sake of reliability and data integrity, the new Fairchild devices automatically generate, store, and check parity bits, one of which is attached to each byte of data. This consistent parity checking is unusual among current bit-slice microprocessor products. But it is an important feature that makes possible diagnostic programs for isolating a problem to the device level.

Fairchild's F100K family of small- and medium-scale integrated ECL circuits are already used in systems needing high speed and low noise. ECL produces slow edge rates that allow noise coupling to be reduced in high-speed circuits. Complementary outputs, constant supply current, and wired-OR capability also ease design of ECL circuits generally. The F100K family of circuits, in particular, adds voltage and temperature compensation to provide constant output voltage levels, input thresholds, and propagation delays over a temperature range of 0° to 85°C and operation from a supply voltage ranging from −4.2 to −5.7 volts. Direct-current noise margins are increased and the specifications of switching characteristics are tightened significantly, permitting higher operating frequencies.

The internal gate delays of these circuits are so short that the interconnection and packaging delays represent a much larger portion of the system's total logic state delay. To take full advantage of this speed, it is necessary to rely on more LSI parts.

One approach now available is the gate array. The F200 gate array, for example, consists of a master diffusion of 168 discrete ECL switches. The interconnection of these switches can be customized by varying the two layers of metalization on the chip, providing a hook-up flexibility capable of implementing the functions of up to 300 equivalent discrete gates.

But a bit-slice microprocessor, specifically the F100220 family, offers a more cost-effective alternative, in the form of general-purpose building blocks that span a variety of architectural partitioning requirements and computer applications. The four new parts are:

- The F100220 address and data interface unit (ADIU), which has extensive binary and decimal arithmetic as well as logic, shift, and data-manipulation capabilities. It can function as an arithmetic and logic unit (ALU) in the data path and concurrently as a memory interface buffer through allocation of one of its three ports.
- The F100221 multiple-function network (MFN), which contains latches accessible by several bidirectional buses. It performs diverse tasks such as data multiplexing/demultiplexing, register-stack addressing, assisting with error-checking code, or serving as a multiport file.
- The F100222 dual-access stack (DAS), a 32-word-by-9-bit register file with two independent ports for data, address, and read/write control.
- The F100223 programmable interface unit (PIU), a general-purpose TTL-compatible input/output device for adapting a central processing unit or peripheral controller to a system I/O bus.

These four devices can be used in various parts of the data path in a microprogrammed machine. The cycle time of a system using them is on the order of 40 nanoseconds for a 64-bit data path.

Three-bus slice

The F100220 address and data interface unit (ADIU) is a 9-bit microprocessor slice that can be cascaded to handle wider data paths. It has a three-bus structure and a high-speed binary/decimal ALU (Fig. 1). All three buses (A, B, and C), which allow communications to the various system data paths and register files, are bidirectional and 9 bits wide—for 8 data bits and a parity bit.

Four instruction bits (I_3, I_2, I_1, I_0) and a multiplexed control line called the function modifier and status line (FMS) define the ADIU's commands. The 27 commands in the instruction set include a variety of binary arithmetic, packed and unpacked binary-coded-decimal arithmetic, single-bit shifts, data transfers, logic operations, and error-correction code operations.

The high (or 1) state of the clock input (CP) causes the ADIU to decode and execute the command. Operands can come to the ALU from any of three buses, the internal C latch, or the result register. The ALU result is always strobed into the result register at the trailing edge of the clock pulse and is available to all three bus drivers using the appropriate bus-enable controls.

Status flags such as overflow, zero, or carry, and error indications like parity or invalid digit are also available for convenient conditional branching by the microprogram sequencer. Carry-propagate ($\overline{P}$) and carry-generate ($\overline{G}$) signals for high-speed expansion are also provided. When these signals are used with a carry-look-ahead unit such as the F100179, a 64-bit ALU with an add time of less than 35 ns can be built.

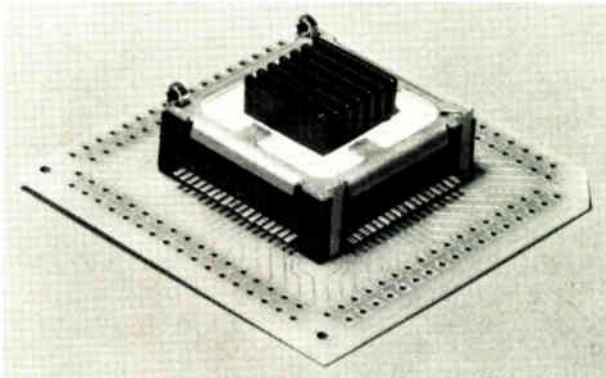
Although diversified, the four functions performed by

Physical characteristics

The four devices in the new 8-bit-slice family are built with Isoplanar technology developed by Fairchild some eight years ago [*Electronics*, March 1, 1971, p. 52]. The new parts have about 1,000 gates per chip and internal gate delays of 700 picoseconds. The ADIU has die size of 203 by 230 mils. The MFN measures 264 by 254 mils, the DAS is 180 by 220 mils, and the PIU occupies a chip of about 52,900 square mils.

The circuits are supplied in a 68-pin LSI package compatible with the standard footprint developed by the Joint Electron Device Engineering Council. The chips are mounted on ceramic bases about 1 inch square with the 68 signal and power paths routed from the die to the package edge through gold-plated metal on the base piece. A ceramic cover is placed over the wire-bonded chip to provide a hermetic seal.

The package has excellent electrical and thermal characteristics. The junction-to-ambient thermal resistance is 15°C/watt with a heat sink and air flow of 500 linear feet per minute, allowing the ECL circuits, which dissipate about 4 watts, to operate safely with air-cooling. Metal clips can be used to solder the leaded package to a circuit board, or the leadless version may be mounted on a carrier such as that manufactured by AMP Inc. (shown).



the F100221 multiple-function network (MFN) have enough in common to be incorporated in one LSI circuit. It contains six 5-bit latches that are loaded and accessed by five 5-bit bidirectional buses, a 10-bit bidirectional function bus that operates in various ways depending on the mode of operation, two additional function inputs, and two enable signals for drivers and receivers.

Multifaceted 4-bit member

Although the MFN is designed to work with the 8-bit slice, the limited number of pins on the package (see "Physical characteristics," p. 122) forced a change to 5 bits for the MFN buses. As mentioned, all data carried by these chips has a parity bit added automatically; for each 8-bit slice of data, a 9th bit is carried for parity. The pin limitation would not allow five 9-bit buses for the MFN, so it works on 4 bits of data plus a parity bit. Hooking two MFN chips in parallel with an exclusive-OR gate connecting the parity bits gives a 9-bit data path.

When operating as a bus multiplexer/demultiplexer, function lines F_1 to F_3 control the routing of data from four 5-bit-wide bidirectional buses (A, B, C, and D) to a fifth bidirectional 5-bit bus (E), with no internal storage and minimal propagation delay. Conversely, the E bus may be routed to any one of the A, B, C, or D buses. If desired, single-bit inversion of the data being multiplexed onto the E bus may also be done, with a compensating inversion of the parity bit to assure correct parity in all cases.

In the error-correction–code assist mode, the MFN performs exclusive-OR operations over either a 4-byte or an 8-byte field to generate the necessary Hamming check code and its related syndrome vector.

The Hamming code is generated by the MFN on outgoing data, such as data being written into memory, while the syndrome vector is calculated to check the correctness of received data, such as that read from memory. The MFN can then decode the syndrome vector to determine if the data in the field is correct or if a single-bit or multiple-bit error has occurred.

Should a single-bit error be found, the byte containing the error is decoded and the ADIU handling that 8-bit slice of data is signaled to correct the error through function lines F_9 to F_{12}. It is told which bit is in error over the A, B, C, and D buses, which are interconnected according to the Hamming parity-bit matrix. When a double-bit error is discovered, a special signal is generated that system designers can use to initiate other recovery procedures.

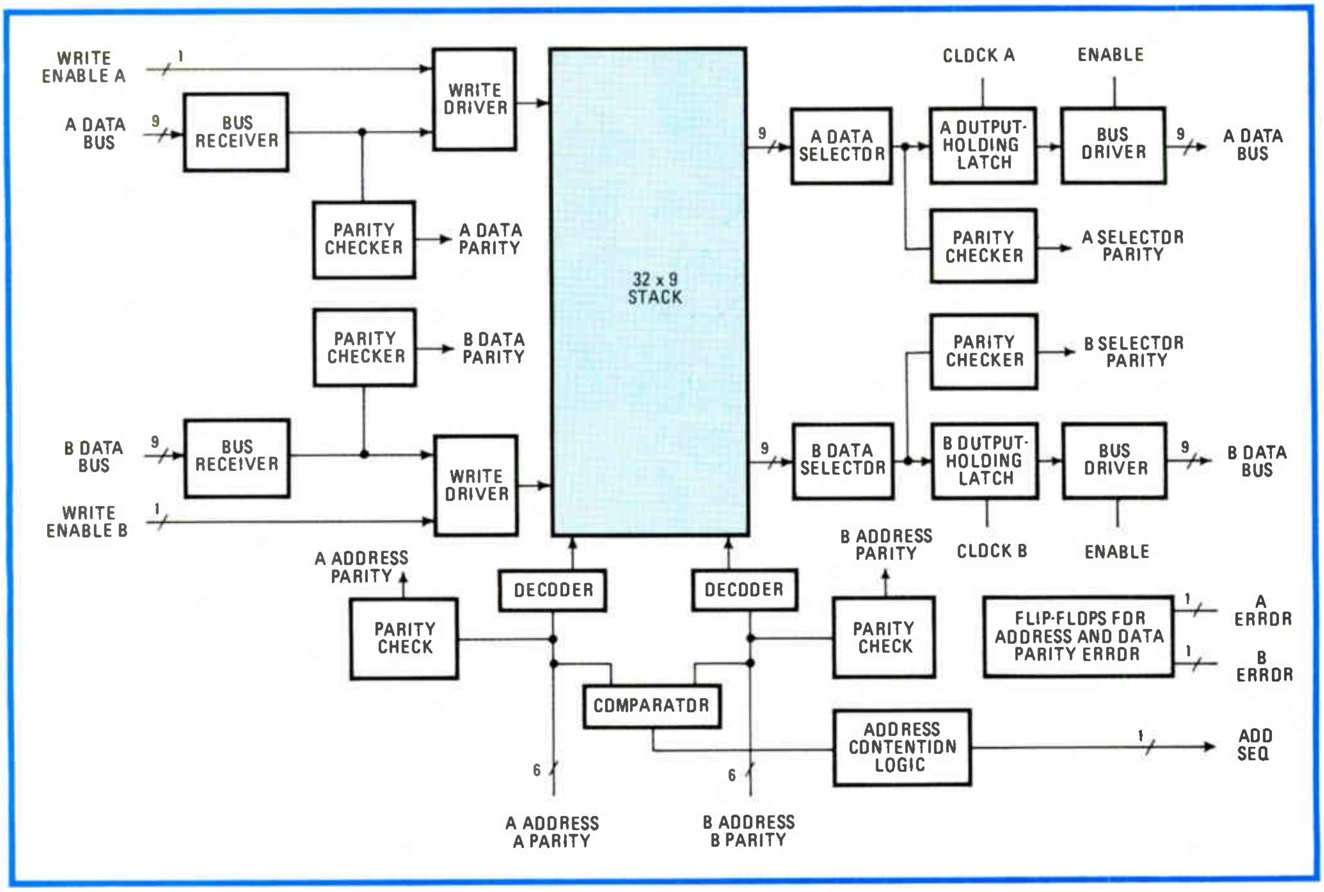
When the MFN is in the register-stack addressing mode, two 4-bit fields, each with a parity bit, are combined to generate one 8-bit field with a single parity bit. This resulting field is the stack address and is stored in an output latch called the stack-address register.

The MFN's six latches are accessible by the A and B buses and are used as four index registers and two page registers. In the indirect addressing scheme, the high-order bits of the address are selected from one of the page registers and the low-order bits are selected independently from one of the index registers.

Alternatively, the contents of the page-zero latch can be combined with an external constant supplied via the C or E buses to form a direct address. All transfers, again, check and maintain odd parity.

Finally, when it is operated as a multiport file, the MFN's five bidirectional 5-bit buses are used as data paths to access four internal latches. Each latch is loaded or accessed by either a dedicated bus (B, C, D, and E) or a common bus (A), depending on the signals placed on function lines F_1 to F_{12}.

A register file of 32 9-bit words is available in the F100222 dual-access stack (DAS). As its name implies, the register file has two independent read/write ports, each with its own data and address lines and separate read/write control signals (Fig. 2). Data parity is checked and stored; optionally, address parity may also be checked. Since this is a true two-port memory, the situation of address contention can occur when the writ-



2. Stacked. The A and B buses can independently access the 32 9-bit registers contained in the F100222 dual-access stack (DAS). Address-contention logic prevents the writing into an address location by one port while the other is reading or also writing into that location.

ing of data to a memory location through one port is overlapped with the reading or writing of information to the same location through the other port. An address-equal flag detects such contention and provides a signal that may be used by external logic for error recovery. The DAS has a maximum access time of 10 ns, making it ideally suited for use as high-speed arithmetic or control registers in a microprogrammed processor or in data-buffering applications.

TTL-compatible interface

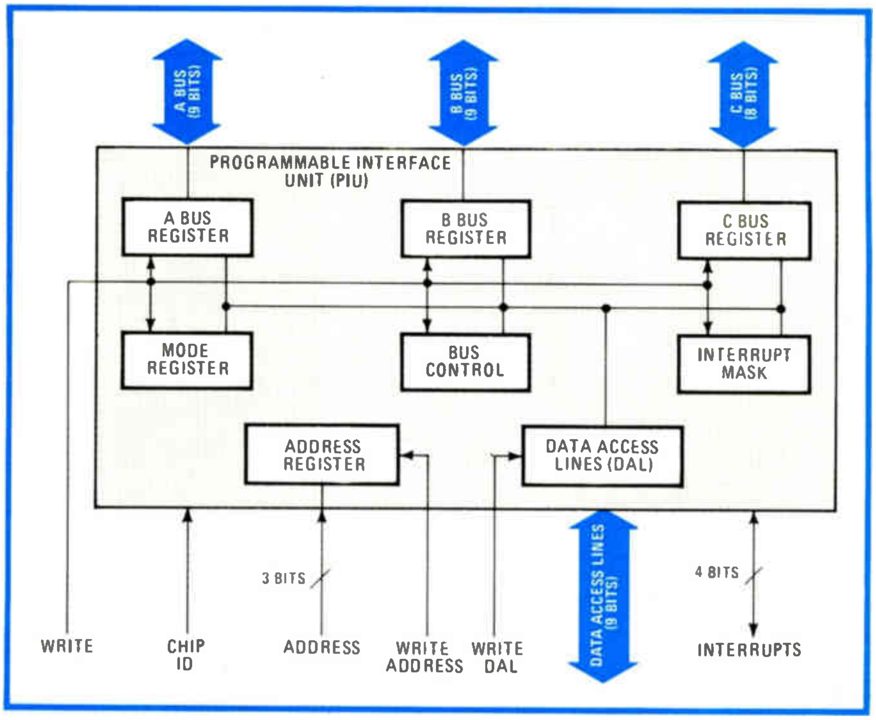
The F100223 programmable interface unit (PIU) is designed to handle input/output communications between central processing unit, channels, and I/O peripherals. Since most I/O interfaces use TTL circuits, the PIU has TTL-compatible I/O. Figure 3 shows the internal registers of the device. The A, B, and C buses provide a total of 26 lines that can be programmed to be unidirectional or bidirectional, with or without automatic handshaking. If automatic handshaking is desired, four lines of the C bus are used for data service and acknowledge signals (two lines each for the A and B buses), providing interlocked data transfer for the other two ports. All three ports have high current-sinking capability (48 milliamperes) with open-collector outputs and Schmitt-triggered receivers with built-in hysteresis for greater noise rejection.

Data communication with the device being interfaced is handled by nine three-state data access lines (DAL), which are compatible with the three-state bus design common among TTL circuits. In addition, the PIU has a powerful interrupt structure, with both inherent and user-defined interrupting conditions that can be inhibited or masked. An identification-comparison feature facilitates unit-to-unit data transfer on a multidrop bus.

For greater throughput, or for parallel transfer of address, command, or status information between I/O nodes, the three bidirectional buses may be expanded to provide another byte path and an independent set of four handshake and control signals.

Using the A and B ports together, a data transfer rate on the order of 3 megabytes per second can be achieved. Once again, the generation and checking of parity on all data transfers assure data integrity. Buffers in the PIU permit immediate retransmission of data received improperly, for quick correction of transmission line faults. Furthermore, interlocking data transfers by acknowledging on a byte-by-byte basis prevents loss of data that could occur in a "blind" transmission environment. A variety of transmission protocols can be built around these provisions to suit specific applications.

To illustrate the multiple functions of these devices, examine a generalized 32-bit computer implemented with them. The microprogrammed CPU is made up of four ADIUs, and uses multiple DAS and MFN chips in its data paths (Fig. 4). The combination of the ADIU and DAS yields a powerful structure with binary or decimal arithmetic and logic manipulation capabilities and a



3. Communicating. The F100223 programmable interface unit (PIU) has three buses that interface the central processing unit and nine TTL-compatible three-state data-access lines for communicating with the attached channel or peripheral device.

read/write scratchpad memory for bus-to-bus data or address transfer and modification.

The input source operands and output results of the A and B ports of the ADIU are provided by the A and B buses, respectively. The A and B buses are then connected to the bidirectional A ports of the DAS chips, but other connections to the A and B buses can be made if the application requires.

The DAS chips are physically grouped in fours, but logically organized as 8 banks of 16 register files. Addressing is provided by two MFNs operating in the register-stack addressing mode. If desired, the 9-bit address outputs of the MFN can address up to 16 banks of 16 registers. This organization facilitates the context switching required in applications such as interrupt servicing or multiprogramming. Instead of spending time to save and restore working registers during and after interrupts, this organization lets the system just swap to a new bank of working registers.

Because of its dual-port capability, the DAS can present two inputs to the ADIU and receive and store the result during the same cycle. Moreover, its simultaneous read/write ability allows it to store a previous ALU result while fetching a new value for another arithmetic operation or the continuation of a double-precision arithmetic operation.

Microprogrammed

Controlling this arithmetic and logic portion of the CPU is the microprogrammed controller. This portion of the machine gets the macroinstruction from memory, decodes it, and through the microprogram sequencer fetches the next microinstruction from the control memory. The DAS can be applied here as a macroinstruction register to buffer the macroinstructions coming from main memory. Because of its 10-ns access time, the DAS can access instructions along either sequential or conditional branch paths while the previous instruction is being executed. Address pointers select current instructions for decoding and a simple algorithm can increment the pointer for either a branch or no-branch decision.

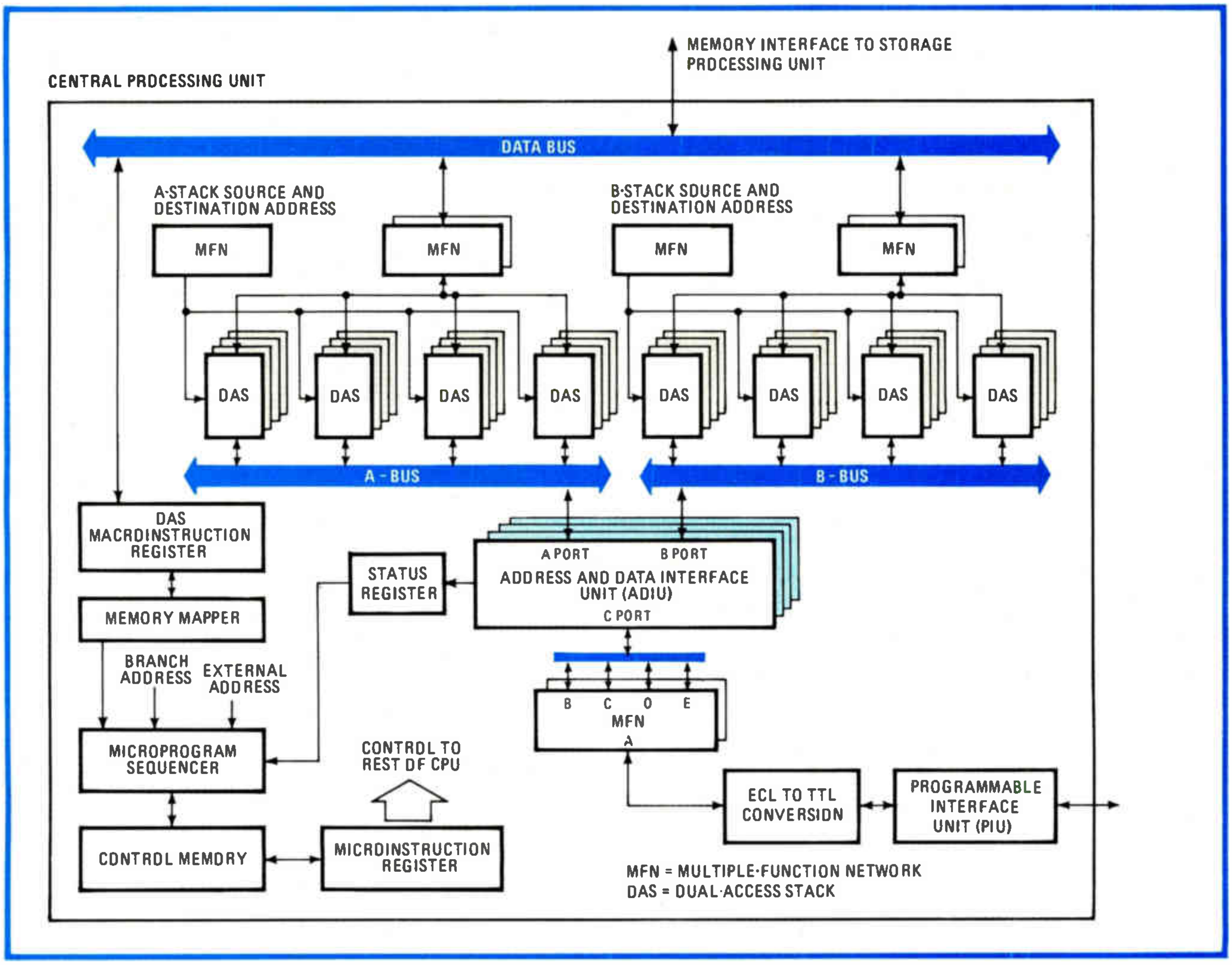
A microprogram sequencer chip designated the F100224 is now under development for use in this microprogram controller section; a variety of F1004XX memory devices are already available to complete the control store portion of the machine. A microinstruction register is used to hold the microinstruction currently being executed. This allows the execution of the instruction to be overlapped with the fetching of the next microinstruction in a pipelined fashion.

Another set of MFNs completes the CPU. Their bidirectional-bus multiplexer/demultiplexer abilities let them be used to handle data-alignment operations such as byte swapping or barrel shifting on information moving between the ADIUs and DASs and the data bus.

In the main storage processor, the ADIU and MFN are combined to handle address-field and data processing between main storage, CPU, and I/O channels. They also do data validity checking, address comparison, and limit checking. The storage processor performs single-bit–error correction and double-bit–error detection for 32- or 64-bit–wide data paths.

The DAS stores key information for access protection and effective memory partition. In addition, the dual-port design of the DAS facilitates its use as a cache interface to main storage, in cases where a wide data path operating at lower speed controls one port while a narrow data path accesses the second port at higher speed in an arbitrary sequence. Incidental conflict of addresses is detected for contingent action.

Communications between the CPU and channels, between two channels, or between channels and input/output controllers are handled by PIUs. The ADIUs are connected to the PIUs through their C ports via two



4. Illustrative. One possible 32-bit computer design using the bit-slice devices has four ADIUs forming the arithmetic and logic unit and two banks of DAS chips—one for each of the ADIU data buses—providing multiple register files. The third ADIU bus is used for input/output.

MFNs working in the multiport file mode. The four internal I/O ports serve as byte-wide bus interface registers. Each port can be selected to communicate to outside TTL circuitry through use of level translators (F100124, F100125). The PIU links the system to other TTL interfaces externally. Its flexible I/O bus structure allows a powerful storage hierarchy to be set up for transfer of command, status, and address sequences.

Obviously, with a microprogrammed computer such as this, some consideration must be given to the design of the microinstructions themselves. Typically, the sequencer instruction and the branch-address fields control the microinstruction flow of the microprogram. During branching operations, the microprogram can alter its execution sequence in response to the status of external test inputs and condition codes from the data path. The other fields of the microcontrol word contain instructions and addresses for the ADIUs, MFNs, DASs, and other miscellaneous logic in the system.

This is a highly horizontal microinstruction word format, which means there is a dedicated field for each control function. A designer may decide to trade in some performance to reduce costs by going to what is called a more vertical scheme. By sharing control fields, for example, he can shrink the microinstruction-word width and bring costs down.

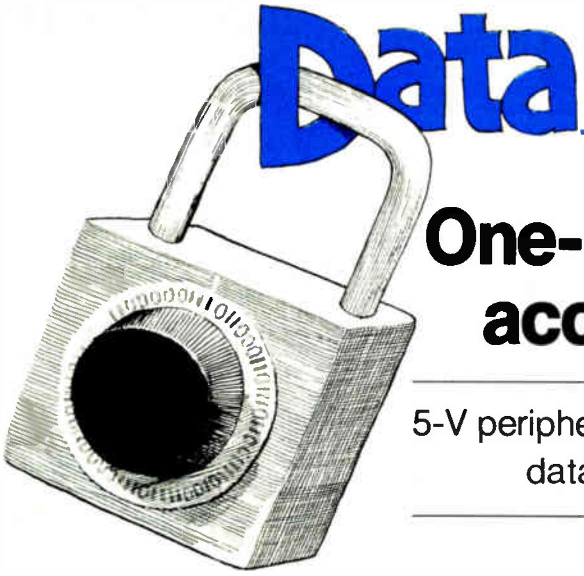
This new 8-bit slice family complements and supplements the F100K subnanosecond SSI/MSI family and the F200 gate array to offer a sophisticated tool for high-speed system designs. It is the fastest and widest bit-slice family on the market today with a bidirectional bus architecture and built-in parity generation, storage, and detection.

Future ECL LSI products

New circuits are being identified and developed to expand the family. As mentioned, a high-speed microprogram sequencer is on the list of products to come. Future development efforts in F100K ECL are aimed toward denser circuits of about 5,000-gate complexity, rather than toward shorter internal gate delays. At subnanosecond speed, system performance can only be enhanced by more on-chip integration and by optimizing packaging techniques. Circuit and packaging innovations are the keys to future ECL LSI products. □

Acknowledgements

The author wishes to thank William K. Owen, Daniel Wong, Cheuk Chu, and Patrick Yin of the ECL engineering group for their technical contributions.



One-chip data-encryption unit accesses memory directly

5-V peripheral circuit implements National Bureau of Standards' data-encryption algorithm at 640 bits per second

by John Beaston, *Intel Corp., Santa Clara, Calif.*

☐ Data-encryption devices—the latest products of large-scale integration—are the hot new rookies of the communications and computer industries. Developed as a result of the U. S. Government's establishment of a data encryption standard (DES) for the safe transmission of sensitive but not classified data, the devices, which can be purchased as chips, plug-in boards, or stand-alone boxes, promise to break into the lineup of any system whose data is not to be compromised.

Data-encryption and -decryption units (DEUs) implement an algorithm developed by the National Bureau of Standards [*Electronics*, June 21, 1978, p. 107]. This algorithm, experts generally agree, is secure enough for most practical purposes. That means that for commercial data manipulation or digital voice handling such as occurs in the computer, banking, or telephone industries, the codes generated cannot be cracked in a "reasonable" amount of time without an inordinate amount of effort.

Many of the major semiconductor houses have entered the burgeoning DEU market—Western Digital and Fairchild Camera and Instrument are two examples. Another is Texas Instruments, which has recently introduced a dedicated peripheral-microcomputer chip to perform the necessary encryption and decryption [*Electronics*, July 19, 1979, p. 140].

Intel's entry is a low-cost single-chip implementation. Already certified by the NBS, the 8294 (Fig. 1) is the only single-chip device also offering direct memory access (DMA) and compatibility with Intel's full line of microprocessor devices. In terms of applications, the 8294 is particularly suited for nonvoice data security when high speed is not required.

Turning it on

The 5-volt 40-pin 8294 converts data at the rate of 640 bits per second using 64-bit blocks of data and a 64-bit encryption key (including 8 parity bits). It has three interrupt outputs to aid in loading and unloading data and operates in the encryption or the decryption mode, or both. The 8294 is driven by an external processor through a series of control- and interrupt-logic circuits (Fig. 2). For convenience in exercising the required control, seven auxiliary output lines are provided for functions defined by the user.

Conversion of data from plain text to encrypted (cipher) text with the 8294 is particularly simple and requires three steps. First, a set-mode command is issued, enabling the desired interrupt outputs or DMA interface if needed. Then an enter-new-key command is issued, followed by the 64-bit key. The key is entered in 8-bit bytes. Each of these bytes must have odd parity as represented by the least significant bit. Finally, an encrypt-data or decrypt-data command is issued to set the chip into the desired mode.

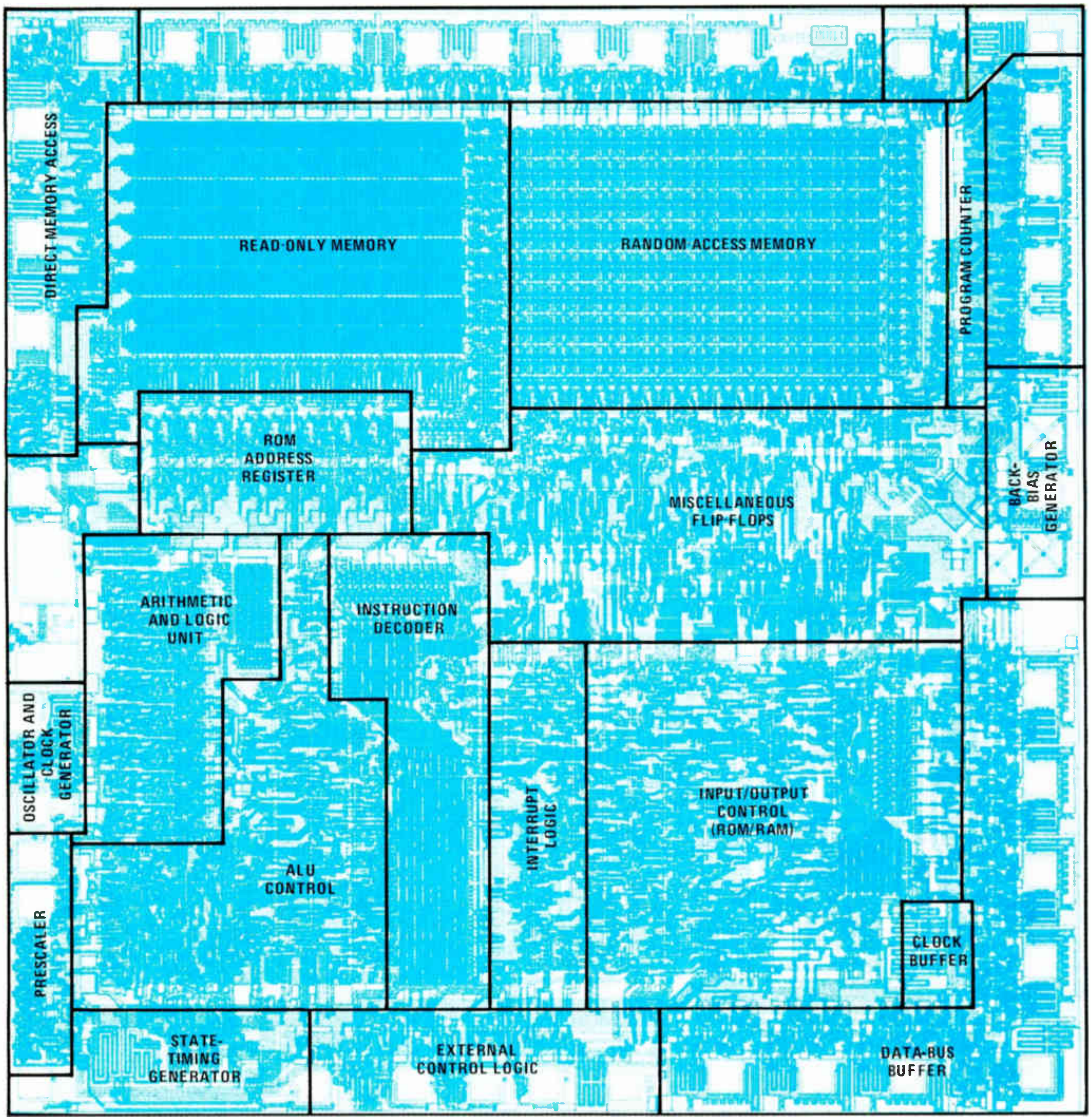
Once these procedures have been completed, data is encrypted or decrypted by simply writing 8 data bytes and reading back 8 converted data bytes. Clearly, all the commands used during data conversion must be "legal." For example, they must effect a change from encryption to decryption without affecting the key by which interrupt outputs are activated. So that the change may be done properly, the mode that the chip is operating in is stored in the status output buffer register and may be read out at any time.

The three steps to turn the chip on are carried out under software control from the central processing unit (CPU) with which the DEU is interfaced. For example, the set-mode command is issued with the appropriate command to activate the desired interrupts. If the user wants to enter a new key, the device's status must be checked before the enter-new-key command is issued. Failure to check properly may result in the 8294's ceasing to operate, and it would then have to be restarted. The key-entry procedure itself is straightforward.

After the enter-new-key command is issued, the 8 data bytes representing the new key are written into the data-bus input buffer 1 byte at a time, beginning with the most significant. The input-buffer-full (IBF) flag is set when a new byte is written and reset when the 8294 accepts the byte.

Before writing new data, the CPU must wait until IBF = 0. After the eighth byte is accepted by the DEU, the completion-flag (CF) bit goes high (CF = 1). At this

This is the second article in a series on integrated-circuit implementations of the National Bureau of Standards' data encryption standard. The first article appeared in the July 19 issue, page 140.



1. Compatible. The Intel 8294 data-encryption chip is perfectly willing to work with any microprocessor or peripheral in its family. It is designed for low-speed applications—up to 640 bits per second—although this figure can be multiplied by n by connecting n chips in parallel.

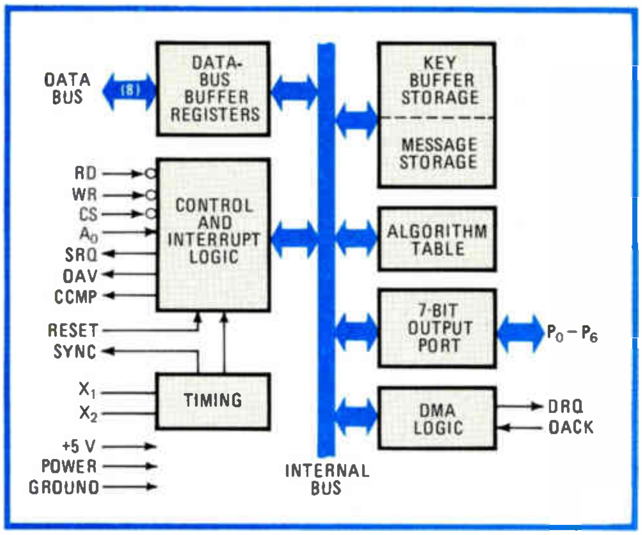
point, the 8294 tests the validity of the key and resets CF. Resetting CF enables the CPU to check the key-point-error (KPE) bit to determine that the key has been entered, stored, and validated before the data bytes themselves are entered.

The use of the CF bit to indicate the validity of the KPE flag makes it impossible to use CF = 1 to flag the end of the 8-byte entry. A counter must therefore be used. CF can then be reserved to validate the KPE flag.

For CPU-based data transfers, the processor writes 8 data bytes into the DEU's data-input buffer to be encrypted or decrypted. When the eighth byte has been received, CF goes high to indicate acceptance of the data block. This last step enables the CPU to check that IBF = 0 and CF = 1 to terminate the input mode.

When encryption or decryption is complete, the conversion-complete (CCMP) and output-available (OAV) interrupts are activated and the output-buffer-full (OBF) flag is set true (OBF = 1). OAV and OBF are reset to false again after each of the converted data bytes is read by the CPU. The CCMP interrupt goes false on the first reading by the CPU and stays false.

After all 8 bytes have been read by the central processing unit, CF goes false, allowing the CPU to test for this value in order to end the read mode. The CCMP interrupt also may be used to initiate a service routine to



2. Easy encryption. The 5-volt, 40-pin 8294 must be controlled by an external microprocessor. Convenient features include seven definable output lines and a DMA interface. Data is encrypted and decrypted according to the NBS's data encryption standard.

perform the next series of data reads and writes.

As an alternative, the DEU-CPU data transfers may be done using direct memory access (DMA). In this case, an external DMA controller, rather than the CPU, supervises the actual data transfers. The only CPU involvement is loading buffer addresses into the DMA controller and telling the 8294 how many 64-bit blocks are to be encrypted or decrypted.

Once loaded with this initializing data, the CPU is free to resume other tasks while all DEU data is being transfered transparently. The CPU is interrupted only after all data transfers and conversions are complete.

An inside peek

All of the 8294's functions are handled internally by microcode stored in the device's programmable read-only memory. The use of microcode results in a slower data throughput rate than that achieved by other devices—for example, IBM's 2845 and 3846 and Motorola's Infoguard systems—through hardware implementation of the DES algorithm. However, the 8294 has the advantage of low cost. Furthermore, it requires no extra integrated circuits for support if used in CPU-controlled operations and only DMA-support hardware if used with that feature.

Although most of the 40 pins of the 8294 have readily understood functions, several require an explanation. For example, pin 9 (A_0) is used to select the register to be accessed for the next operation. The data buffer is selected by a 0 on this line, and the command/status register is chosen by a 1. In conjunction with the not-read ($\overline{RD}$) and not-write ($\overline{WR}$) lines (pins 8 and 10, respectively), this signal chooses the proper register. If the triplet $\overline{RD}$, $\overline{WR}$, and A_0 is 100, 010, 101, or 011, the registers chosen are, respectively, the data-input buffer, the data-output buffer, the command-input buffer, or the status-output buffer. The not-DMA-acknowledgment ($\overline{DACK}$) and DMA-request (DRQ) connections are used to implement direct memory access—the former for an acknowledgment signal from the DMA controller (an Intel 8257 or the equivalent) that the requested DMA cycle has been granted, the latter for the signal used to request a DMA cycle.

Lines P_0–P_6 are definable by the user as a 7-bit port that may be employed, for example, to pass additional information between the CPU and the 8294. They have nothing to do with the encryption function.

Applications

In a breadboard application developed by Intel during the design of the 8294, the chip encrypts and decrypts a text file stored on the Intellec microcomputer development system diskette. Extension of this design may readily be made to allow the chip to be used in more sophisticated applications. In this case, the chip is mounted on a plug-in printed-circuit board (Fig. 3), along with its support circuitry.

The system requires one 8294 with DMA capability, including address generation for 16-bit addresses (handled by the 8212), buffering to the Intellec system's bus (the function of the 8226s), and chip-select logic.

The dual in-line switch is used to give the configuration an interrupt mode. The CPU can then query the 8294 and drive it directly for each data transfer. Whether in a CPU-monitored mode or with DMA, the system uses the CCMP signal from pin 24 of the 8294 to notify the CPU when the DEU has completed a transfer.

To start the system, the board is inserted into a card slot in the Intellec system. The user then types a command consisting of a file name, a D or an E symbol, and a sequence of eight ASCII characters. The file name is the name of the ISIS-II file to be encrypted or decrypted, and the D or E indicates whether decryption or encryption is to be performed. The eight ASCII characters are the key used by the 8294 in encoding or decoding data or text in the file.

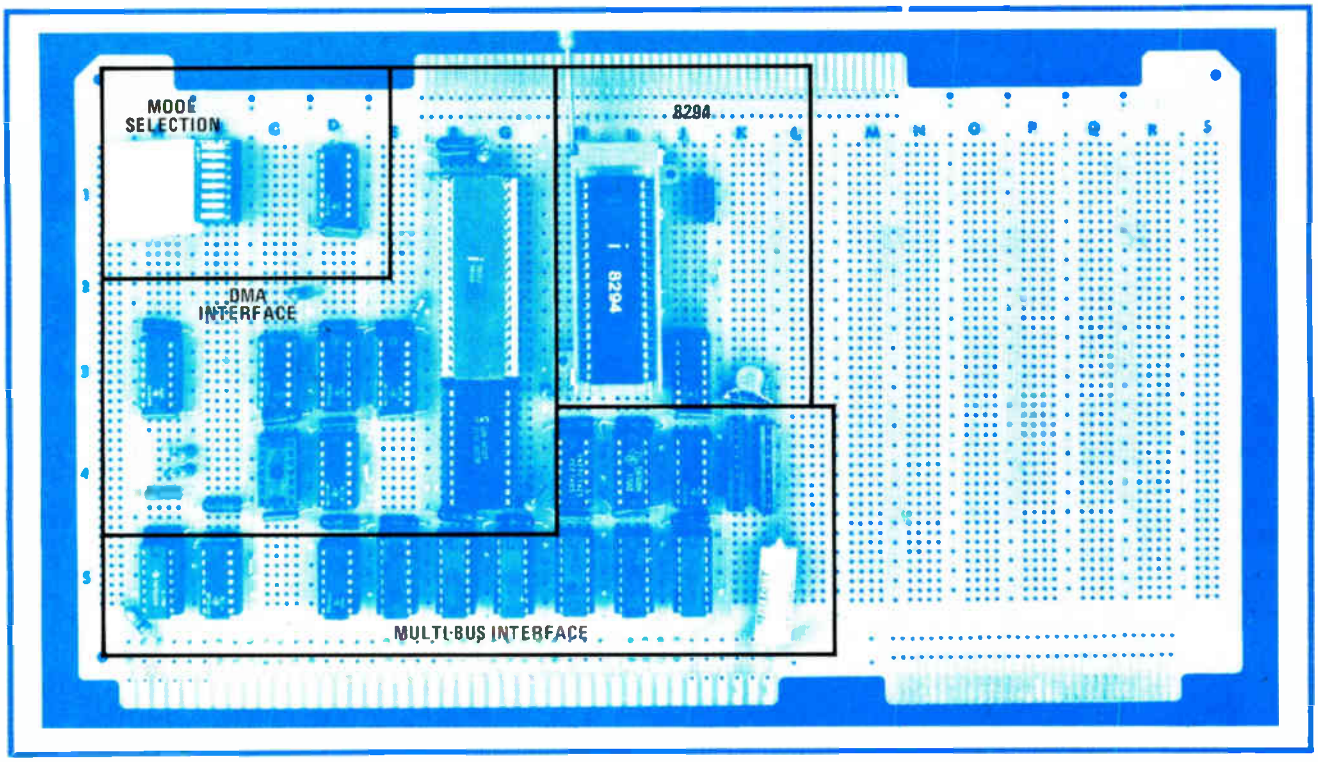
When encryption or decryption has been completed, the new file (containing either plain or encrypted text, respectively) replaces the old file on the diskette. If any errors—such as input/output problems with the diskette—arise during translation, the original file is left undisturbed, as the system uses a temporary holding file during both encryption and decryption.

Note that this system encrypts everything on the file. Therefore headers and other special symbols used by other software to recognize and manipulate the file are no longer recognizable. In an actual implementation, total encryption could seriously affect the file's usability and would have to be corrected in software.

In this application, support logic was added for direct memory access so that the CPU could complete other processing during encryption and decryption. Most of the circuitry on the pc board would be unnecessary in a minimum application (without DMA).

The other additional hardware required if DMA is implemented is a chip-selection or decoding module. This logic is used to determine whether or not the CPU is addressing the 8294 during initialization and processing.

The use of DMA has the dual effect of accelerating the throughput rate of the 8294 somewhat and of off-loading the monitoring of the DEU from the CPU. However, since



3. Breadboard. When mounted with its auxillary and support chips on a printed-circuit board, the 8294 functions as an encryption plug-in for a computer development system disk. In this application, memory is accessed directly, although that is not always necessary.

the CPU's involvement with data encryption and decryption is limited to reading 8 bytes from the data-output buffer and putting 8 more into the data-input buffer, the amount of time the CPU is occupied monitoring and handling the 8294 is fairly limited.

On the other hand, the availability of DMA implementation on the 8294 makes it possible to parallel several of the devices, along with the DMA controllers associated with each. Such parallel processing greatly increases the throughput of the encryption and decryption process. It can probably be useful up to a data-transfer rate of about 19,200 bits per second. Above this rate, a hardware-based implementation is preferable.

Obviously, far more sophisticated applications could be developed using other operating-system software and handling different-sized blocks of data. The principles of operation, however, remain the same. All that is required is to set the DEU to the proper mode, write the key into it, and convert 8 bytes of data at a time, either under DMA or CPU control. How the files are handled and what disposition is made of the decoded text are individual design decisions.

Software

Since the 8294 operates under microprocessor software control, the processor must, at a minimum, initialize the chip, set up the DMA controller to handle the block of memory to be encrypted or decrypted, and respond to an interrupt when the processing is over. In a minimum configuration (again, without DMA), the processor must also read the 8 bytes into the 8294's data-input buffer. There is a 100-millisecond delay between the time the 8 bytes are placed in the data-input buffer and the time they will typically be encoded or decoded and available at the data-output buffer; during this period, the CPU can perform other functions.

The software used in the development-system circuit described earlier is relatively simple. Note, though, that a loop is established after the input and output file names have been established. This loop is necessary so that the program can ensure that the command being given to the DEU has been accepted (detected by the presence of a 1 in bit 0 of the command-input buffer).

There are a few software subtleties to be aware of. For example, since the 8294 is designed to code 8 bytes at a time and since the file may not be an even multiple of 8 bytes, the last block of data read must be filled with 0s until it is 8 bytes long.

Also, remember that after the DEU's mode has been set, the output-data buffer is cleared by reading it and discarding the contents. This operation is necessary because the 8294 will hold the data valid in the output-data buffer indefinitely (assuming no power-down occurs). If the last conversion attempt was unsuccessful, not completed, or otherwise aborted or abandoned, this buffer could have 1 byte of encoded or decoded data present at the beginning of the new processing cycle.

When all the software setup work is out of the way, the data conversion proceeds in a straightforward manner. In the application program discussed earlier, data is read from the diskette file in blocks of 1,024 bytes converted and written into the temporary file in the same block size. Upon completion of the data conversion, assuming it was successful (that is, no I/O errors or disk errors were encountered), the new file replaces the old file, which is first closed and then deleted. □

Circle 130 on reader service card

 Circle 174 on reader service card Circle 175 on reader service card

D-a converter's low-glitch design lowers parts count in graphic displays

15 small matched current sources reduce size of fast transients produced by asynchronous switching

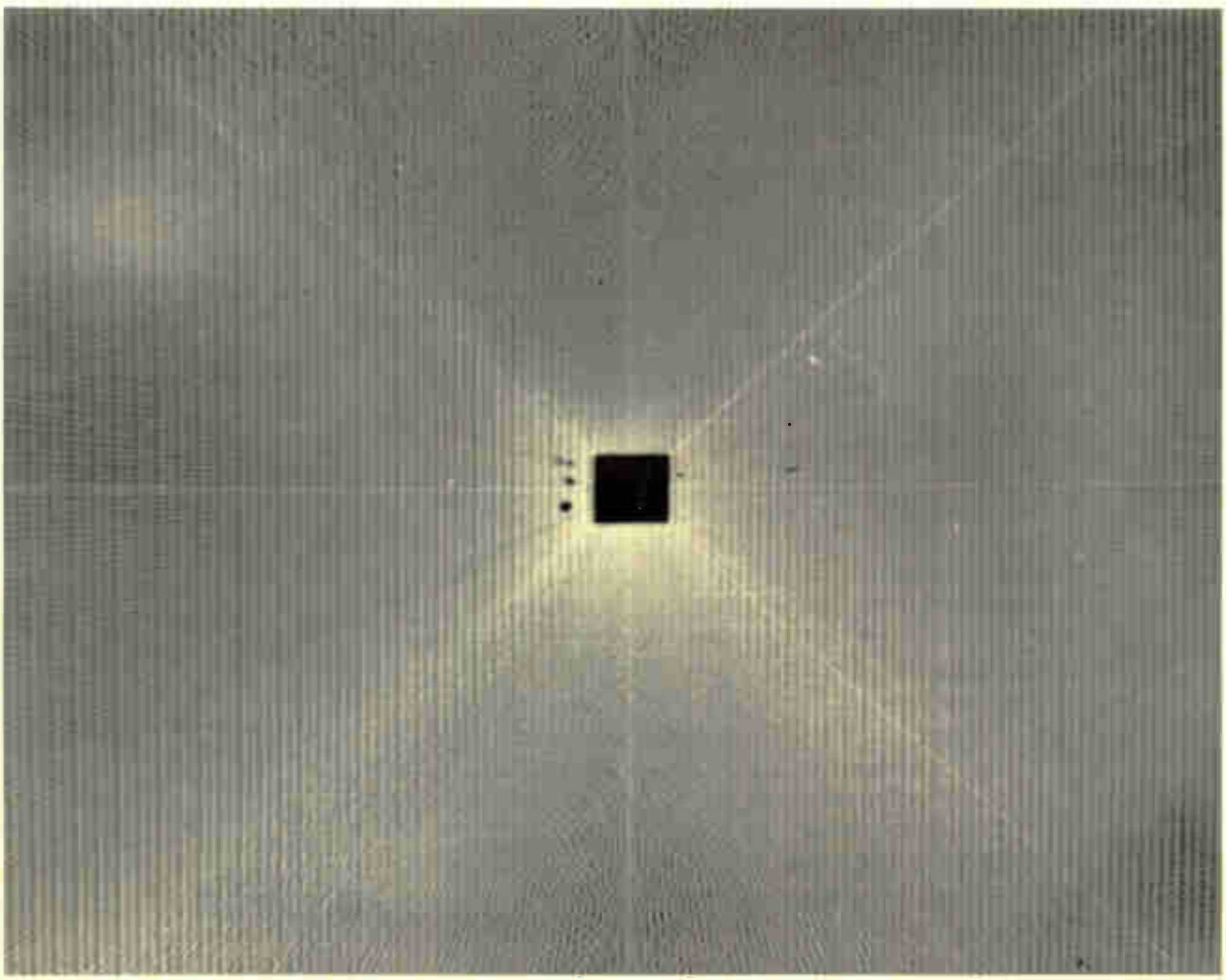
by Michael Yuen
Hybrid Systems Corp., Bedford, Mass.

☐ No designer of a digital-to-analog converter intends his device to produce spurious fast transients; the very name given these transients—glitches—bespeaks their undesirability. But the problem has plagued d-a converters since their inception.

Some applications can forgive this shortcoming. But when d-a converters are used to drive the beam-deflection circuits of a cathode-ray-tube graphic display system, distortion caused by glitches is easy to see and more than just annoying. Converters used for this purpose must have short settling times and high current drive capability in addition to a low glitch level. Rapid settling is vital to flicker-free display of complex patterns: the converter must be able to update at about 10 megahertz or faster. High current output makes possible the high slew rates required for good pulse transmission over coaxial cable.

Many current state-of-the-art d-a converters can provide the fast settling and high current output needed to drive CRTs. But until now, with the introduction of the Hybrid Systems 394 12-bit current-output d-a converter, the low glitch level has remained elusive. A number of

1. Display effects. A cathode-ray-tube display with its X-axis deflection circuit driven by a conventional digital-to-analog converter and its Y-axis one by a new low-glitch converter shows how a radial spoke pattern is distorted by glitches into a series of vertical lines.



deglitching techniques have therefore been called upon to compensate for the effect.

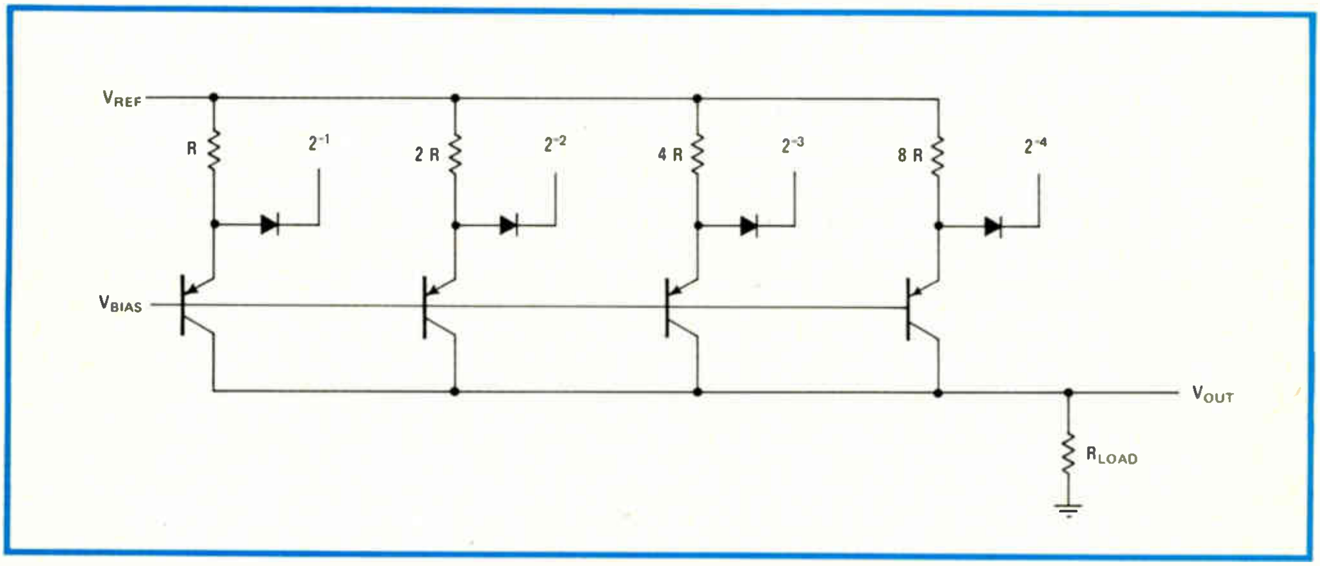
The effects of glitches on a CRT are easily demonstrated. Since the position of the electron beam is determined by the voltages (outputs from the d-a converters) at the X and Y inputs, any spikes or transients that appear at these inputs will displace the beam momentarily from its course or position. The direction of displacement is dependent upon the origin (X or Y input) and polarity of the glitch.

Graphic effects

If the X input of a CRT is driven by a conventional converter and the Y input is driven by a low-glitch converter, as in Fig. 1, the effect of glitches becomes clear. The digital inputs to the d-a converters are generated by a computer programmed to produce a spoke pattern. If neither converter produced any glitches, the display would consist of straight lines radiating from the center. Glitches in the output of the X-axis converter displace the beam momentarily to the left. The result is a series of vertical lines with each line representing a major transition, the point where a glitch occurs. In an alphanumeric display, the glitches cause distortion in the shape of the characters.

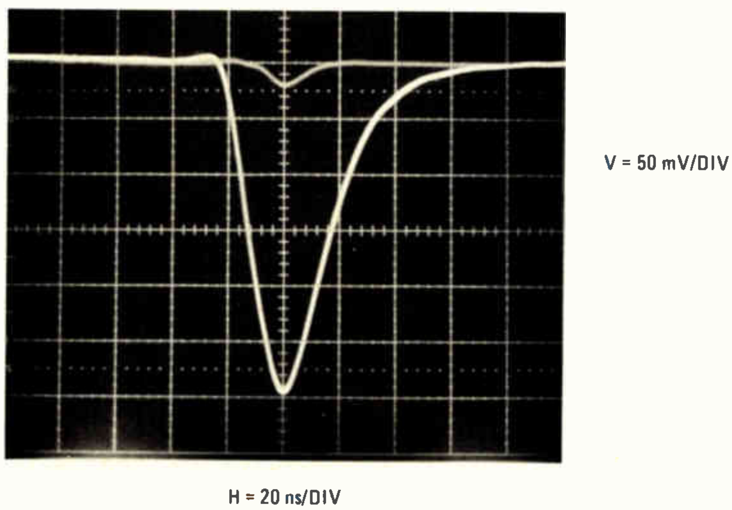
To understand the techniques used to build the above-mentioned low-glitch d-a converter, the source of these long-troublesome voltage spikes must be examined in some detail. The asynchronously switched transistors that control the analog outputs of modern d-a converters are the main culprits.

A simplified diagram (Fig. 2) shows how bipolar transistors are used in a 4-bit d-a converter. Depending on the input logic levels, the diodes steer current either through the transistors, turning them on, or through themselves, turning the transistors off. In high-speed



2. Glitch maker. Four-bit converter uses solid-state switches to control its analog output. Glitches are produced by digital feedthrough of high-speed TTL signals by way of the steering diodes, and by the current ladder during asynchronous switching of the transistors.

3. Spike shrinkage. Glitches produced at major transitions by a conventional d-a converter (the large spike) and a new Hybrid Systems 394 12-bit converter are compared on an oscilloscope. The large excursion is nearly half the full 1-V output. The other's amplitude is smaller by a factor of 16; as a result, the settling time is much shorter.



Conventional deglitching techniques

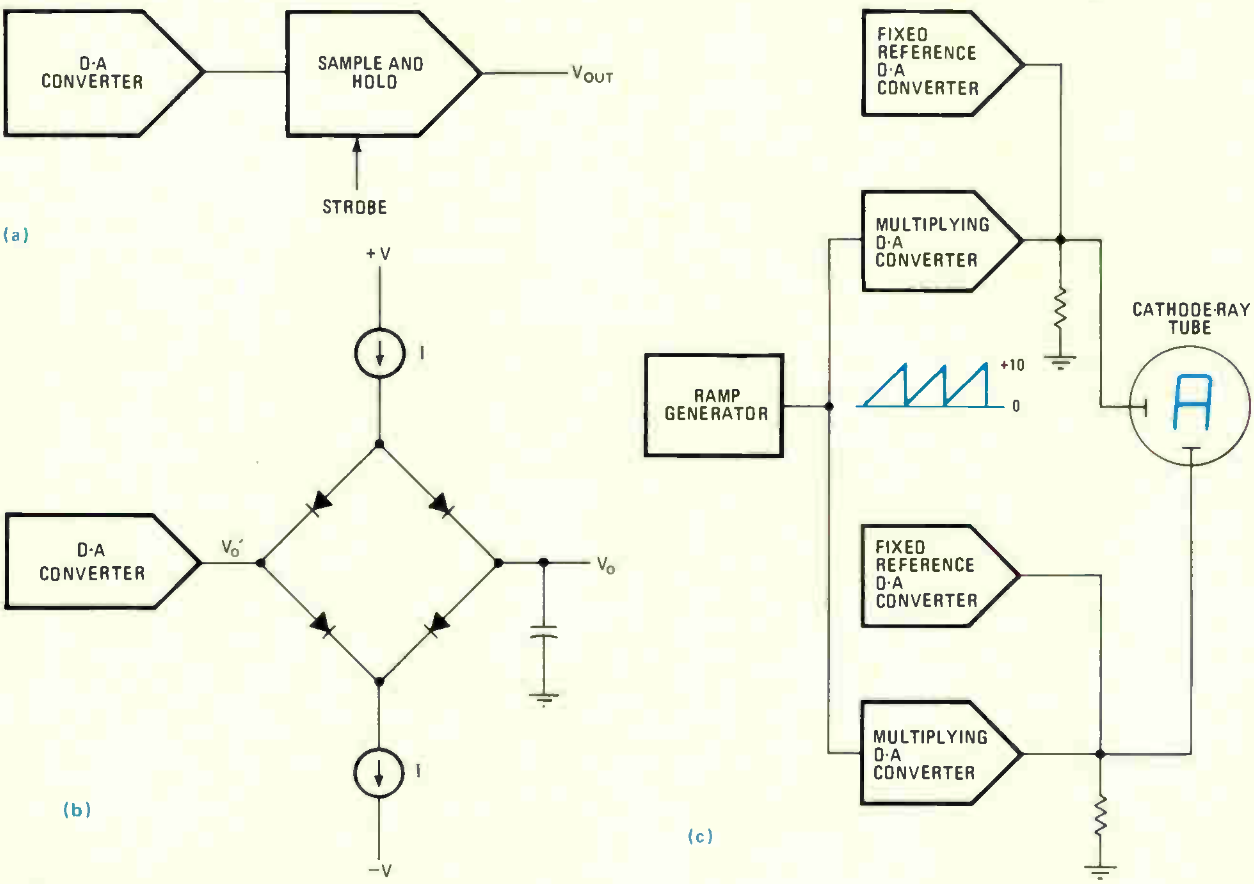
A number of deglitching techniques are in wide use, despite their drawbacks. The most common method is to use a fast sample-and-hold at the d-a converter's output (a). The sample-and-hold is normally operated in the track mode and is switched to the hold mode just before the converter is updated. When the converter has settled to the new value, the sample-and-hold is switched back to the track mode. Thus the glitch period is effectively isolated from the output.

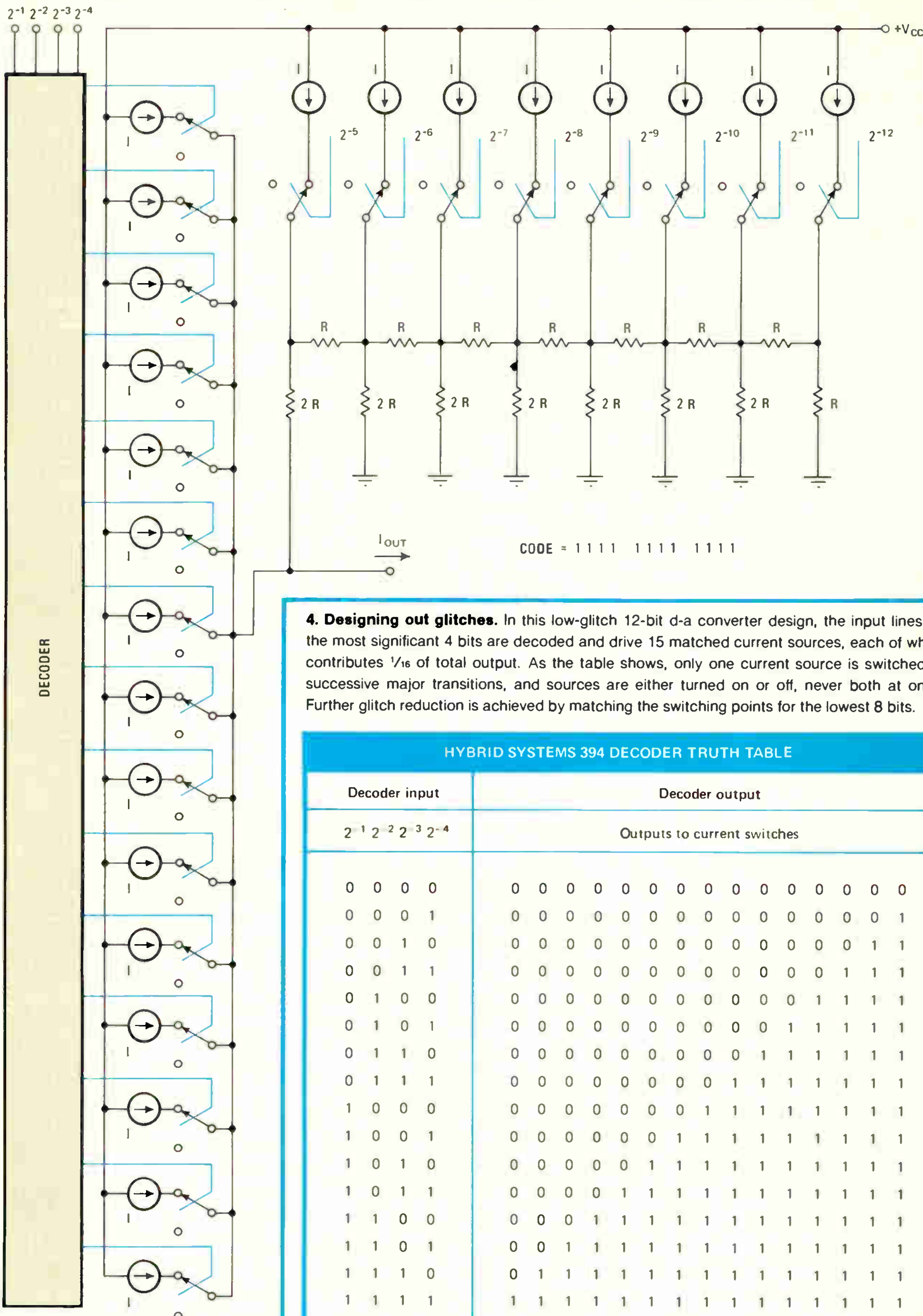
Of course, to be effective, the sample-and-hold itself should not introduce significant voltage spikes at the output. In addition to the cost of the sample-and-hold, which can be as high as that of a converter of comparable speed and resolution, this technique introduces extra delay due to the sample-and-hold acquisition time. This usually limits the update rate to 2 megahertz or less. Additional error from sample-and-hold offset and droop can be expected.

For graphic display systems that can tolerate a lower converter-update rate, a bandwidth- or slew-rate-limited circuit is sometimes used for deglitching (b). At equilibrium, the balanced diode bridge forces V_0 to be equal to V_0'. V_0 will follow V_0' as long as $V_0'/t \leq I/C$. Therefore, any fast-changing signals like glitches are filtered out. Unfortunately, this reduces the converter's overall response time. This compromise may be justified, however, in applications where reduced bandwidth without glitches can be tolerated.

Multiplying converters are sometimes used to circumvent glitch problems in CRT graphic display systems. A multiplying converter's analog output is proportional to the product of a variable reference and the input code. In the typical setup shown (c), a pair of current-output converters drive each CRT input (X deflection and Y deflection). The two fixed-reference converters determine the position of the starting point (X_0, Y_0) of the display line. Their outputs are summed with the external variable-reference (multiplying) d-a converters, which are driven by a 0-to-10.0-volt ramp reference. The ratio and magnitude of the multiplying units' digital codes determine the slope and length respectively of the line being generated on the display. Complex display characters are made up of a series of these straight lines. Since glitches occur only when the converter input codes are changing, this setup minimizes the code updating as the beam is essentially being driven by the ramp. In addition, the input codes can be changed during the retrace of the beam when the screen is usually blanked.

This method offers an attractive solution to the glitch problem in a CRT graphic display system, but is not without its limitations. The most obvious is the cost of the two extra converters. Moreover, the updating logic is more complex, as four converters must be updated instead of two. Finally, only one straight-line segment may be drawn per sweep, so that in a complex character-generation system, where many such segments are required, the devices must have a very fast settling time, 100 nanoseconds or less.

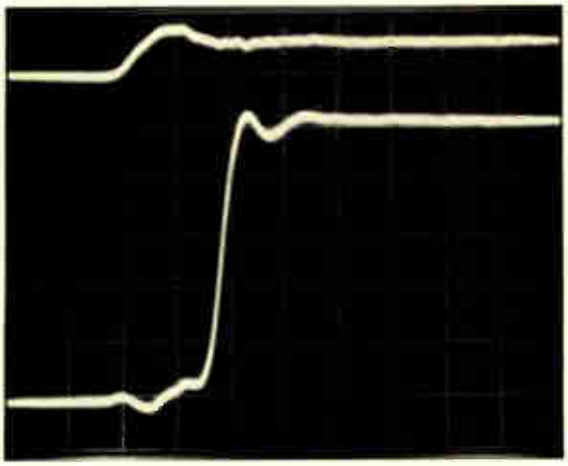




4. Designing out glitches. In this low-glitch 12-bit d-a converter design, the input lines for the most significant 4 bits are decoded and drive 15 matched current sources, each of which contributes 1/16 of total output. As the table shows, only one current source is switched in successive major transitions, and sources are either turned on or off, never both at once. Further glitch reduction is achieved by matching the switching points for the lowest 8 bits.

HYBRID SYSTEMS 394 DECODER TRUTH TABLE

Decoder input				Decoder output														
2^{-1}	2^{-2}	2^{-3}	2^{-4}	Outputs to current switches														
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
1	0	0	1	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	1	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1



5. Settle down. Nonsaturating current switches and input storage registers included in the design contribute to the high-speed performance of the 394. This output waveform shows settling to within 0.05% in about 50 nanoseconds after full-scale switching.

applications, these switches are often driven by TTL signals with very short rise and fall times; therefore, some digital feedthrough at the output of the converter is unavoidable. However, this feedthrough is usually much smaller than the glitches commonly produced by the asynchronous switching of the converter's transistors. The instant after the digital input code changes, these current switches briefly assume a temporary state that produces a transient output.

For example, if the time it takes to turn the switching transistor on exceeds the time to turn it off, the 0-to-1 transitions take longer than 1-to-0 transitions. Thus when a transition in the input occurs from a value of 7 (0111) to 8 (1000), instead of a smooth change in the output of the converter, it momentarily swings toward 0000 before returning to 1000. The worst case usually occurs at the half-scale transition (that is, from a value of 011 . . . 1 to 100 . . . 0) where all of the switches must change state. In this case, the excursion can have a half-scale magnitude.

The traces of two glitches are shown on an oscilloscope in Fig. 3. The greater of the two was produced by a conventional high-speed 12-bit d-a converter during a half-scale transition. The excursion is almost half scale for a full-scale output of 1 volt. Because of the large excursion, the settling time is increased. The smaller of the two glitches was produced by the 12-bit Hybrid Systems 394 d-a converter during a major transition. The magnitude of this spike is but a sixteenth that of the larger one; the settling time is also much improved.

Low-glitch design

None of the conventional deglitching techniques (see p. 133) such as added sample-and-hold circuitry are used to achieve this reduction. Its new design approach reduces glitches while cutting the number of components needed for a CRT display.

The 2-by-4-inch module has a full-scale current output capability of 21 mA that allows it to drive 50-Ω-terminated coaxial cable, and it delivers a full-scale output of 1 volt. Monotonicity and differential linearity of ±½ least significant bit are maintained over the commercial temperature range.

To achieve these performance specifications, the decoding technique illustrated in Fig. 4 is used. The converter is essentially divided into two sections. The lower-order 8 bits that together contribute 6.22% (225/4095) of the total output current is a conventional d-a converter using a R-2R current ladder. Instead of the usual scheme, which has the upper 4 bits drive four current sources with a binary weight of ½, ¼, ⅛, and 1/16, the input lines are decoded and drive 15 matched current sources. Each matched current source has a weight of 1/16 of the total output. Hence by switching on the correct number of current sources, any combination of the binary weights ½, ¼, ⅛, and 1/16 can be achieved.

As seen in the truth table, the decoder has been designed to switch only one current source for each successive major transition. Also, the coding is such that switching between any of the 16 major transitions involves either turning current sources on or turning them off—never both in the same step. In this way glitches produced by the asymmetrical switching times are practically eliminated. Since no current source has a weight of more than 1/16 of the total output, the glitch level is greatly reduced. To obtain a further glitch reduction, the switching points for the lower 8 bits of the converter are optimized and matched.

Nonsaturating current switches, together with input storage registers, produce the high speed characteristic of the new current-output d-a converter. As shown in Fig. 5, the unit settles from full-scale switching to ±0.05% in about 50 nanoseconds.

To achieve 12-bit accuracy, all 15 current sources are precisely matched. All 15 sources must be scanned to pick out the largest source; the remaining 14 are then matched to that value. Fortunately, this entire task is accomplished with the aid of an automated system programmed to trim the entire unit, including gain and offset, in less than 8 seconds. □

Separating data from addresses on the 488 bus

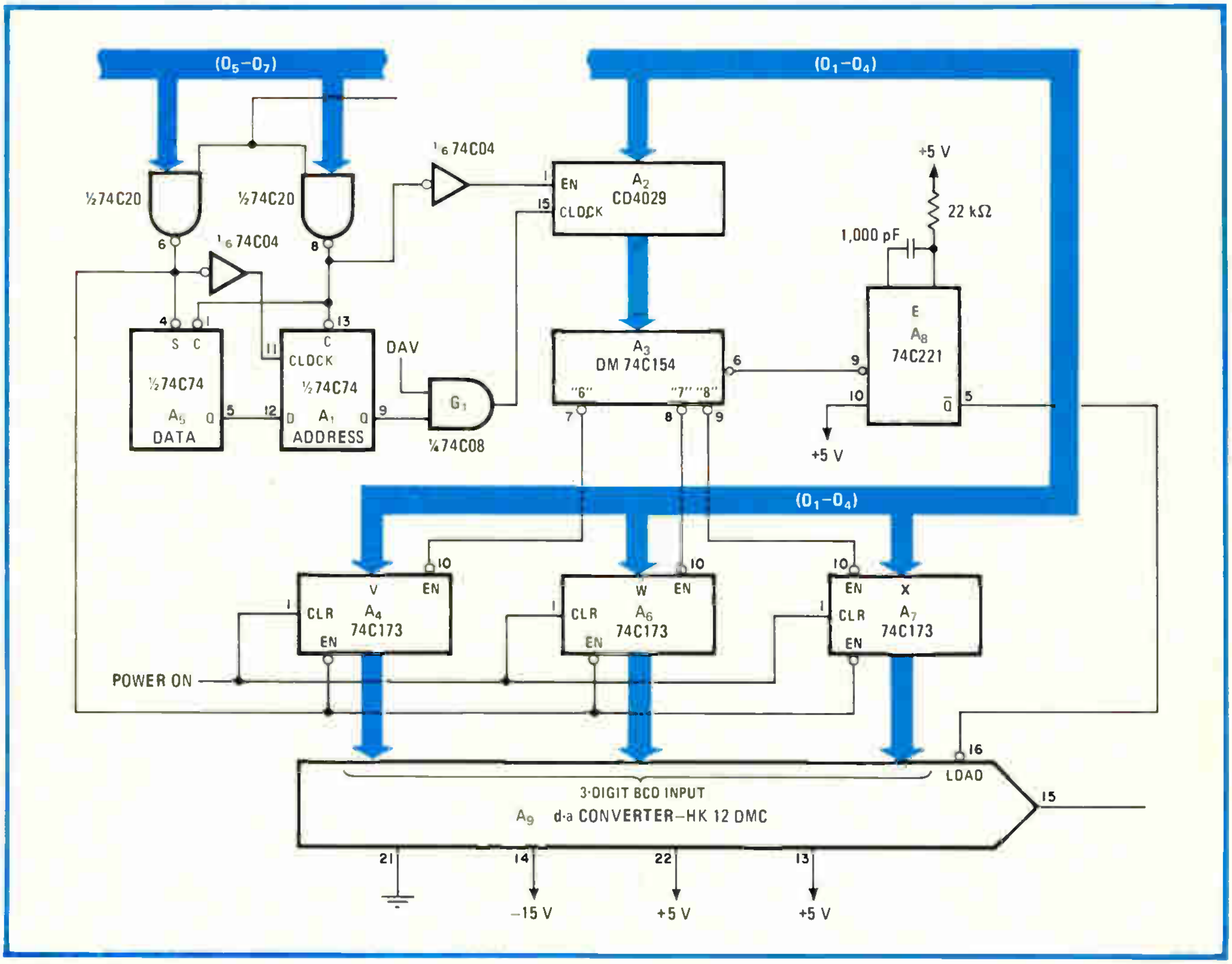
by Trung Nguyen
Systron-Donner Corp., Van Nuys, Calif.

This relatively simple interface offers a convenient way of detecting and differentiating between addressing information and data words on the industry-standard 488 instrumentation bus. It uses standard parts, is inexpensive, needs no complex clocking circuitry, and eliminates the need for software interaction.

Information on the bus is transmitted as a series of 8-bit bytes associated with a hexadecimal code. Normally a 7-bit ASCII character is sent, with the eighth bit appended for synchronizing the bit stream, so that 00110111, for example, is the equivalent of 37 hex, and 01001010 is 4A hex. The coding of bits 5 to 7 (as counted from right to left) identifies the information on bits 1 through 4 as representing data, if bits 5 to 7 = 3, or address locations, if bits 5 to 7 = 4 or 5. This interface easily determines under which category the bit stream will be identified, so that addressing information will be recognized as preceding the data, ensuring that the appropriate circuitry will display only data.

Address flip-flop A_1 is reset when the hexadecimal value of input bits D_5–D_7 equals 4 or 5, so disabling counter A_2 (through gate G_1) after bits D_1–D_4 are stored in it. Thus, if ASCII character V (56 hex) is sent, 0110 (6) is loaded in the counter and decoded by A_3 so that only address register V (A_4) is enabled.

On the other hand, data flip-flop A_5 is set when the hexadecimal value of input bits 5 through 7 equals 3,



Differentiation. 488-bus interface distinguishes address information from data bits, so that data alone may be displayed without using excessive software. Address bits detected are stored in register V, to be utilized in system as required. Data bits then fill V, W, and X. ASCII "E" command at end of data stream fires A_8, forces registers' contents to be dumped into d-a converter.

and so data is loaded into the V register. If there is more than 1 data byte in the stream following the address byte, A_1 is clocked by the new data and the contents of A_5 are transferred to A_1. A_1's output is combined with the data valid (DAV) pulse at G_1 so that A_2 will be advanced by one count.

The address decoder, A_3, thus activates register W (A_6). Register X (A_7) is brought into operation if a third data byte is sent in a given group.

After all data bytes are loaded into A_4, A_6, and A_7, an execute command represented by ASCII "E" triggers one-shot A_8, thus permitting data to be transferred to the digital-to-analog converter, A_9. The stream required to generate an output of 5.48 volts at A_9 would thus be V548E. The numeral 5 is loaded into V, and 4 and 8 are loaded in registers W and X, respectively, by advancing A_2. This operation eliminates the need to address each register for each data byte—that is, V5W4X8E. □

8080 program counter makes relative jumps

by Prakash Dandekar
Tata Electric Companies, Bombay, India

Although the conditional and unconditional jump commands found in the 8080's instruction set allow programs to be positioned anywhere in memory, all jumps are absolute and require specification of a 16-bit absolute address. The short routine of six instructions presented here, however, makes it easy for the program counter (PC) to make relative jumps either ahead of or behind its own starting point, adding greatly to the 8080's versatility.

By passing the desired relative displacement of the PC as a parameter through the D-E register pair, relative jumping of the PC can be effected virtually anywhere within the 64 kilobytes of available memory. The routine simply adds the contents of D-E to the current PC location stored in register pair H-L in order to bring the PC to its new location. This location is then stored in the H-L register.

The desired displacement should be expressed in 2's complement form. A positive displacement of X will cause the program to jump forward X locations from the initial PC location; a negative displacement will have the opposite effect.

When an unconditional jump is desired, the CALL instruction should be used to summon the relative-jump subroutine PCRJMP, as shown. A conditional jump (i.e. JZ, JZN, JP) can be ordered by the corresponding call instruction CZ, CNZ, or CP. □

8080 RELATIVE-JUMP SUBROUTINE

Source statement	Comments
:	
LXI D, DISP	; displacement in (DE)
CALL PCRJMP	; call PC relative jump routine
	; current (PC) on stack
:	
PCRJUMP : XTHL	; current (PC) in (HL)
DAD D	; displacement added to (HL)
	; result in (HL)
XTHL	; modified (PC) on stack
RET	; modified (PC) in (PC)
	; program control transferred
	; to new area

HP-25 program makes fast cost estimates

by Joe Barocio
Teledyne Lewisburg, Lewisburg, Tenn.

The learning curve, also known as the experience or improvement curve, is a well-known tool for predicting the total manufacturing cost of a product from the established cost of the first unit. Given any learning curve factor, this program uses its tabulated values to find unit, cumulative average, and total costs in a fraction of the time it would take to calculate those costs by hand.

The formula based on the learning curve factor, L, is $v = ax^y$, where v is the manufacturing cost of unit x, a is the cost of the first unit and y is the log of L divided by log 2. L *per se* represents an index of the cost of manufacturing a series of units, and it is affected by a personal-fatigue/delay allowance (PFDA). Determined empirically, L depends heavily on the manufacturing processes used in a given company but is relatively independent of the particular product manufactured.

Having v, the program determines the cumulative average cost of the first through the xth unit from $z = v/(1+y)$. The program then finds total cost, C, by multiplying z and x.

Consider the example where 1,276 electronic relays (x) are to be produced; the cost of one electronic relay (a) is $1.65; the learning curve factor (L) is 0.83; and the PFDA is 0.166. Introducing these constants into the program as instructed yields v = $0.2413, z = $0.3300 and C = $491.02.

This value compares favorably with the longhand solution of $490.67. Note the error between these two values will be considerably greater when x is equal to a small value (less than 10), or when a step learning curve (a factor of less than 0.50) is used □

Engineer's notebook is a regular feature in Electronics. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $50 for each item published.

HP-25 PROGRAM FOR ESTIMATING PRODUCTION COSTS

Line	Code	Key
01	31	ENTER
02	74	R/S
03	23 00	STO 0
04	74	R/S
05	14 08	f log
06	02	2
07	14 08	f log
08	71	÷
09	23 01	STO 1
10	14 03	f y^x
11	61	×
12	74	R/S
13	24 01	RCL 1
14	01	1
15	51	+
16	15 22	g 1/x
17	61	×
18	74	R/S
19	24 00	RCL 0
20	61	×
21	01	1
22	24 02	RCL 2
23	51	+
24	61	×
25	13 00	GTO 00

Registers	
R_0	x
R_1	(log L)/log 2
R_2	1+ PFDA

Instructions

- Key in program
- Enter RUN mode and initialize
- Key in the cost to produce the first unit, total number of units desired, learning-curve factor, and personal fatigue/delay allowance factor:

  (a), R/S, (x), R/S, (L), R/S, (PFDA), R/S

  The cost of the xth unit (i.e. v) is displayed
- Press R/S to display the cumulative-average cost, z.
- Press R/S to display the total cost for x units, x · z.

"How a Zehntel in-circuit test system made me a hero with my sales reps."

Tom McShane, VP of Marketing, Racal-Vadic.

"Last year, Racal-Vadic introduced a revolutionary new product — a triple modem — and sales took off like a skyrocket.

Production, however, lagged behind, much to the chagrin of sales reps — and customers.

There were logical reasons. This PC board had three times the component complexity (including a microprocessor) of anything we'd built before.

Our yield of good boards was less than 60%. And since our functional tester didn't indicate the type and location of failures, it was taking our techs forever to rework boards. A real bottleneck had developed.

Then we installed a Zehntel Model 800 TROUBLESHOOTER In-Circuit Test System.

Within six weeks we were shipping TEN TIMES as many triple modems as before!

In seconds, our Zehntel in-circuit inspector was finding the common assembly errors — wrong value, out of tolerance, mismarked or dead analog and digital components, solder bridges, open circuits. And since precise rework instructions on ALL failures is printed out in simple English, our techs could repair the boards much faster.

Today, board yield is well over 90%. Production is keeping pace with sales, and once again I'm a hero with my sales reps — and my customers.

Why did we choose Zehntel? For one thing, they're pioneers in in-circuit testing, with hundreds of satisfied users throughout the world. Also, they're specialists. In-circuit testing is their ONLY business. Because of this, they provide outstanding service and engineering backup every step of the way.

As far as I'm concerned, whether it's modems or in-circuit test systems, you just can't beat experience.

By the way, Zehntel just sent me an informative booklet entitled "How to Beat Murphy's Law with an In-Circuit Test System." It's worth sending for."

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Circle 139 on reader service card

Engineer's newsletter

Get hands-on experience with your thick-film prototypes

Traditionally, users of thick-film hybrid have two sources of prototypes. One is the independent hybrid house, and the other is in-house development. Now they have a third choice: Cermalloy has opened **a lab to provide thick-film users with up-to-date production and test facilities to determine the feasibility of new circuit designs.** Circuit prototyping and limited production facilities will also be available in the new lab. In most cases Cermalloy will be able to provide a customer with a prototype within two weeks after receiving the circuit design or artwork. In addition, a customer's engineers will be permitted to work alongside Cermalloy staff members in the new lab to gain first-hand production experience. For additional details about the laboratory, contact Cermalloy, Cermet Division of Bala Electronics Corp., Union Hill Industrial Park, West Conshohocken, Pa. 19428.

Program aids network design

If you would like to take some of the black art out of network design, a new low-cost, interactive program from Security Research Laboratories will demystify you for a mere $550. It computes transfer functions, gains, stability, and so on for two-port networks at any frequency. Available in Fortran IV and Basic, the ND-1 software uses **simple instructions to handle complex networks while plotting all items over any selected range.** It even permits the engineer to use measured parameter data as well as design data in predicting the response of a network. For further information, write to Security Research Laboratories, P. O. Box 49, Dept. ED1, Medfield, Mass. 02052.

A square hole for tritium

Considering tritium gas as a source of back-up lighting? Corning Glass Works had this use in mind when it developed precision glass tubing with a rectangular instead of circular cross section. **In a square tube, the tritium light-source—gas plus phosphor coating—can lie flat and thus save display space.** This type of tubing made it possible to use tritium lighting in extremely slim liquid-crystal-display watches. Available in borosilicate glasses, it comes in widths of 0.100 to 0.150 inch and heights of 0.030 to 0.040 inch. Additional information may be obtained from the Electronic Materials Department of Corning Glass Works, Corning, N. Y. 14830.

A reliable way to learn about reliability

Every engineer today needs a good basic knowledge of the principles of design reliability. To meet this need, the Reliability Analysis Center at Griffiss Air Force Base, N. Y., has prepared a course specifically for circuit designers who have had little or no previous reliability training. Major elements in the course are: part selection, specification and control; part derating, plus derating guidelines; reliability allocation and prediction; reliability analysis, testing, and program management; reliability design techniques such as redundancy, environmental protection, and design simplification and analysis; **and life-cycle-cost and design-to-cost philosophies.** The four-day course will be given for $400 in Seattle, Aug. 27–30, and Orlando, Fla., Dec. 10–13. For further information call Mrs. L. Mack at the Reliability Analysis Center, (315) 330-4151. **-Jerry Lyman**

Capacitance meter spans nine ranges

3½-digit instrument uses dual-threshold technique to minimize errors caused by dielectric absorption, measures up to 199.9 mF, sells for $190

by Richard W. Comerford, Test, Measurement & Control Editor

The 3001 is a 3½-digit meter that measures capacitance in nine ranges, the lowest resolving 1 pF and the highest able to measure values to 199.9 mF. At 23°C, the $190 unit's basic measurement uncertainty is ±0.1% of reading ±1 count on the seven lowest ranges and ±0.5% of reading ±1 count on the two highest. Temperature variation affects the accuracy of all ranges by only ±0.01% of reading at maximum over the instrument's 5°-to-45°C operating range.

In the design of the meter's front end, Continental Specialties Corp. engineers managed to overcome what marketing director Marty Weinstein refers to as "the biggest bugaboo"—dielectric absorption. The 3001 measures capacitance indirectly, noting, as do other meters, the time it takes to charge an unknown capacitor through a known resistance to a fixed voltage threshold. Typically, an unknown capacitor is charged and discharged several times a second during a test, with the display updated after each cycle.

Dielectrics, however, tend to retain charge; after discharge, a residual voltage can appear on their terminals. If not dealt with, this voltage would shorten the charge time and thus shift the reading to a value below the actual capacitance.

A refinement of the technique devised by design engineer Larry Fischer does away with this problem. Called dual-threshold slope integration, it uses two voltage thresholds: the first, at a value well above any possible residual voltage, starts a charge-time measurement and the second ends it. The difference in threshold is fixed for each range, as is the resistance, so capacitance is directly proportional to the measurement time. Each complete charge-discharge cycle takes only 0.3 s on all but the highest range, where it takes 3.5 s.

According to Fischer, the choice of line operation rather than battery power for the 3001 was dictated by practical considerations. He found that, with few exceptions, such meters are used "within easy reach of a 120-V or 240-V main." With batteries, he says, it easy for power to fall below useable levels without the user knowing it, thus invalidating all readings. "On a production line, this could mean big trouble."

Locating the 100-pF zero-calibration knob in the center of the panel, away from the input terminals, lets a user zero the instrument without his hand introducing stray capacitance. Overall calibration is accomplished by adjusting a single potentiometer from the back. The adjustment is also far from the power source; together with internal shielding, this minimizes line-induced capacitance errors.

The 3001 will be available starting in September along with a test jig for production line testing. Clock and gate signals provided at the rear permit the unit to be used with a remote display or limit comparator, which is planned for introduction later this year.

Continental Specialties Corp., 70 Fulton Terrace, New Haven, Conn. 06509. Phone (203) 624-3103 [338]

GE
Quick-rental®
instruments

Data acquisition

4-bit converter runs at 30 MHz

Monolithic device consumes only 250 mW, sells for $29 each in hundreds

The excitement in analog-to-digital converters—and there is plenty of late—has been mainly in three areas: high speed, high resolution, and low cost with low speed and modest resolution. Common to all three areas has been design for compatibility with microcomputers. Meanwhile, somewhat in the background, are ballooning video applications that require high speed and low price but can tolerate low resolution. TRW LSI Products is drawing a bead on this market segment with its TDC1021J—a 4-bit monolithic device with a conversion rate of 30 megasamples per second.

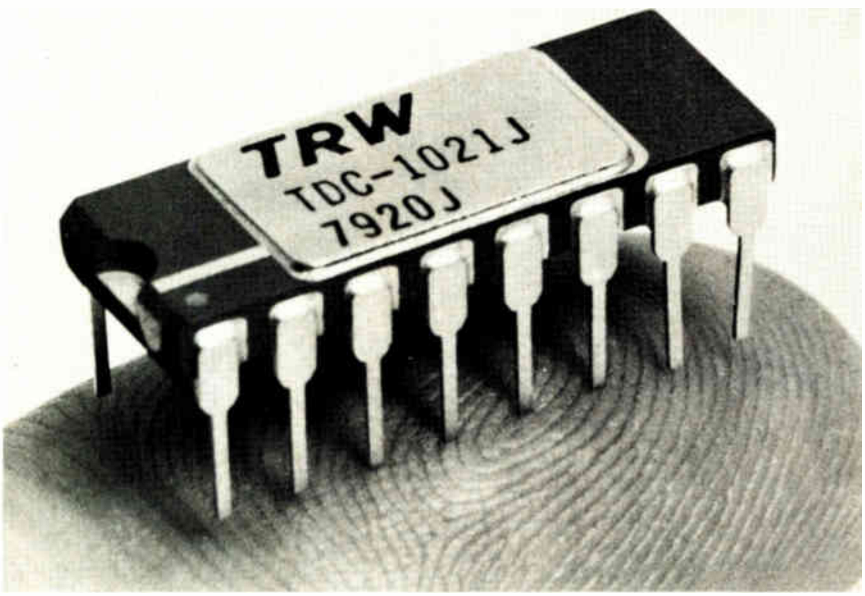
"The TDC1021J fills in the last little converter gap," says Willard K. Bucklen, applications engineer at the TRW Electronics division, which has up to now concentrated largely on such upper-end items as 12-, 16-, and 24-bit multipliers and converters. The new 4-bit unit is a fully parallel (flash) converter that can operate at any conversion rate from dc up to its 30-MHz maximum. "Furthermore, it works without an external sample-and-hold circuit," Bucklen points out.

Other features calculated to win users, in his opinion, are a total power consumption of 250 mW from two supplies (+5- and −6-V), housing in a standard 16-pin ceramic dual in-line package, and a 100-piece price of $29. The converter has a maximum nonlinearity of ±⅛ of a least significant bit, an aperture jitter of ±30 ps, and recovery time from a full-scale step of no more than 20 ns. Controls are provided for selecting straight binary or offset 2's complement output coding in either a true or inverted sense.

TRW LSI Products believes its 4-bit converter is the first such monolithic unit to reach production, although Advanced Micro Devices, Sunnyvale, Calif., announced a version in 1977. So far AMD has built 30-MHz engineering samples for internal evaluation, says a spokesman, but has no set production schedule. "But we will be in this market," he says.

Among applications TRW sees for the 4-bit converter are video and radar data conversion, high-speed multiplexed data acquisition, X-ray and ultrasound imaging, image processing, and facsimile.

TRW LSI Products, division of TRW Inc.'s Electronics Components Group, P. O. Box 1125, Redondo Beach, Calif. 90278. Phone (213) 535-1831 [381]



MOS device converts 8 bits using capacitance network

By using a capacitance network in its new MOS analog-to-digital converter, West Germany's Siemens AG has obtained what it believes are remarkable performance characteristics for such a device. Intended as a link between sensors and microprocessors, the 8-bit SAB3060P a-d converter sports a maximum nonlinearity of ±½ least significant bit.

The device, based on n-channel silicon-gate technology, uses successive approximation to convert analog voltages into 8-bit digital words. Measuring ranges of 0 V to between 1 and 8 V are selectable. The conversion accuracy checks in at ±1 LSB. At a clock rate of 2 MHz, conversion time is 40 μs, whereas at 3 MHz it becomes 25 μs.

The SAB3060P generates its selectable reference voltages—1 to 8 V—by charge distribution in the binary-weighted capacitance network. With this method, says Karl Hirschel, product manager for microcomputers at Siemens in Munich, a higher input impedance and a higher linearity can be obtained than with MOS converters using integrated resistance networks. Furthermore, since the reference and measuring voltage sources are only capacitively loaded, driver amplifiers are not needed. Internal resistance of these sources is less than 3 kΩ each.

Now available in sample quantities, the SAB3060P carries a price tag of about $11 in 100-piece lots. Larger-quantity lots can be had later this year, with delivery time for 1,000 pieces about four to six weeks.

Siemens Corp., 186 Wood Avenue South, Iselin, N. J. 08830, or Siemens AG, 8000 Munich 1, P. O. Box 103, West Germany [383]

Yes it's true —

There is a completely new kind of FFT-based Spectrum Analyzer

Yes, it does give you an extra dimension in high-speed, high-resolution spectrum analysis, DC—100KHz.

Yes, it plugs into any Tektronix® Series 7000.

Yes, it has the same "1-2-3-READ" Three-Knob simplicity of conventional tuned analyzers.

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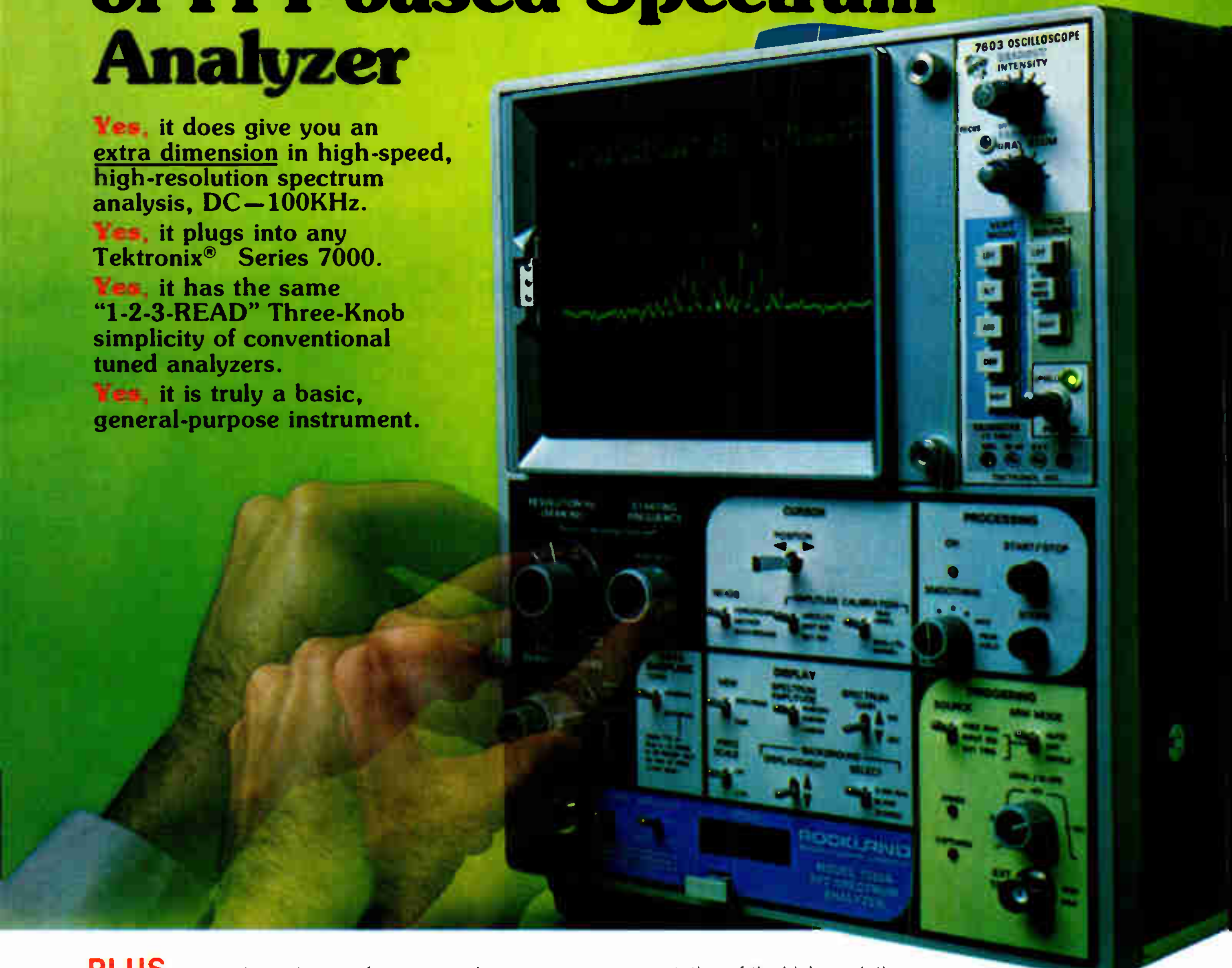

PLUS many other unique performance and convenience features... extra dimensions of value, only in the Rockland Model 7530A.

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ROCKLAND

Rockland Systems Corporation, Rockleigh Industrial Park, Rockleigh, N.J. 07647, (201) 767-7900, TWX 710-991-9852

Components

Zinc oxide makes varistors better

Units withstand 4,000-A surges and boast speedy response times

Taking the plunge into a new market area, Victory Engineering Corp. has begun producing metal-oxide varistors. For over 20 years the company has manufactured both silicon and silicon-carbide varistors, but it now believes the time is right to enter the market long dominated by General Electric. VECO's new metal-oxide varistors protect against high-voltage transients, as its other varistors do, and in addition sport high transient current capabilities and fast response times.

"Metal-oxide varistors aren't that simple to make," notes C. S. Molee, vice president for engineering. "But there are distinct advantages to using them." Among those advantages are: a high transient current capability of up to 4,000 A at 85°C; a response time of less than 35 ns; and the ability to withstand up to 2,000 pulses with only a 10% derating of the nominal voltage value.

The VECO line of Zorbguard varistors includes three different kinds: the R series, a disk type with radial leads and nominal voltage ratings from 117 V to 1,400 V; the A series, a cylindrical device with axial leads and nominal voltage ratings between 27 V and 430 V; and for low-voltage applications, the Z series, a disk type with radial leads and voltage ratings from 27 V to 120 V. Both the R and Z series have nominal voltage temperature coefficients of less than 0.05%/°C, and the A series is rated at less than 0.03%/°C. The R series has a response time of 35 ns, while the A and Z both respond within no more than 40 ns.

These varistors are nonlinear, voltage-dependent resistors made primarily from grains of zinc oxide.

Sintered at a high temperature, the devices exhibit sharp, symmetrical breakdowns. "What you're really looking at is a back-to-back zener diode," observes Molee. The units use solder-clad copper leads, which are placed across the entire body of the device, reducing formation of local hot spots under pulsing conditions. No compensating components are needed with these varistors; they may be inserted directly into the circuit across the power lines.

Affording protection against transient surges that occur when transformers switch, motors start, or there is high-current interruption, the varistors may be used to isolate solid-state circuitry and related components from relay coils and solenoids, for example.

Priced at $0.49 each in 1,000-piece quantities, the varistors may replace devices such as selenium surge suppressors, silicon power zeners, gas-discharge tubes, and carbon spark gaps. Delivery is from stock to six weeks.

Victory Engineering Corp., Victory Road, Springfield, N. J. 07081. Phone Bud Molee at (201) 379-5900 [341]

Rf amplifiers cover 1-GHz range

Additions to the MWA series of wideband radio-frequency amplifiers extend its upper frequency limit from 400 MHz to 1 GHz. The new amplifiers should prove useful as broadband linear amplifiers in military, commercial, and consumer equipment and, more specifically, in rf, intermediate-frequency, and automatic-gain-control amplifiers and as line drivers and isolation stages.

Like their 110, 120, and 130 predecessors in the series, the new single-stage devices have 50-Ω input and output impedances and are fully cascadable for any gain. Also like the earlier models, they are thin-film hybrid circuits hermetically sealed in metal TO-39 cans. As such they afford more consistent performance than discrete designs, not to mention greater reliability and greater temperature stability.

The MWA210, 220, and 230 have a frequency range of 0.1 to 600 MHz, a typical gain of 10 dB, and 1-dB compression output levels of +1.5, +10.5, and +18.5 dBm, respectively. Comparable figures for the 310, 320, and 330 amplifiers are 0.1 MHz to 1 GHz; 8-, 8-, and 6.2-dB gains, respectively; and +3.5, +11.5, and +15.2 dBm, respectively. Noise figures range from 4 to 9 dB, depending on type. High-reliability versions can be made to MIL-S-883, Method 5004.4, Class B.

Prices range from $5.50 to $7.00 in lots of 100; units are currently available from stock.

Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Ariz. 85036. Phone Alan Wagstaff at (602) 244-6394 [345]

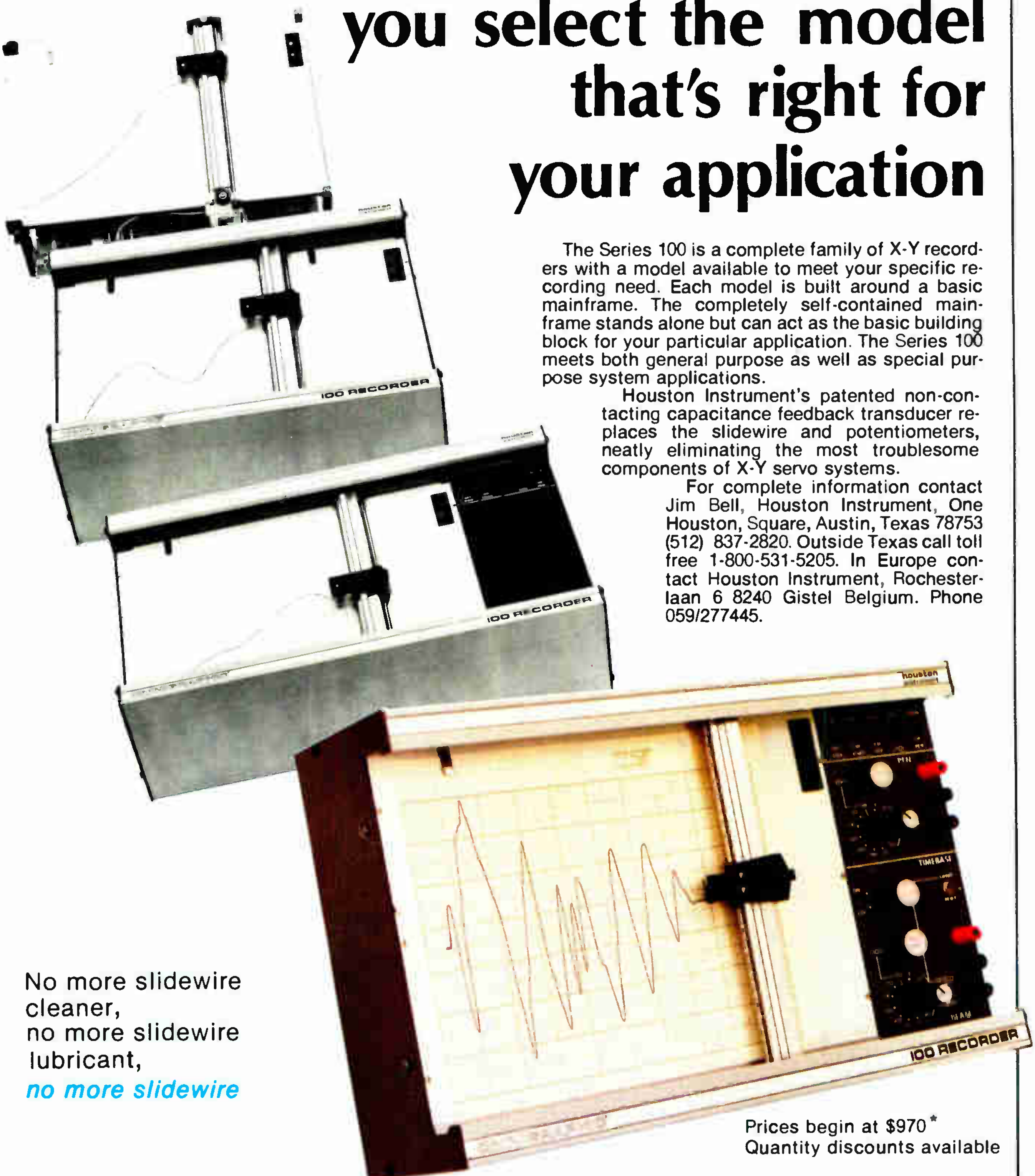
Low-cost ceramic chip capacitors handle 15 kV

Working voltages up to 15 kV are achieved by a line of high-voltage ceramic capacitors with a single dielectric layer. They supplement a standard line of multilayer devices rated to 4 kV. Proprietary glass- and silver-free noble-metal contacts make them easy to mount and provide high adhesion contact with excellent resistance to solder leaching. Available values range from 10 to 5,000 pF in NPO and X7R dielectrics. In quantities of 1,000, they sell for 95 cents to $3.85 each. Delivery takes four to eight weeks.

Johanson Dielectrics Inc., 2220 Screenland Dr., Burbank, Calif. 91505. Phone William Jensen at (213) 848-4465 [346]

Lab or field, production or process, OEM or general purpose...

The Omnigraphic® Series 100 lets you select the model that's right for your application



The Series 100 is a complete family of X-Y recorders with a model available to meet your specific recording need. Each model is built around a basic mainframe. The completely self-contained mainframe stands alone but can act as the basic building block for your particular application. The Series 100 meets both general purpose as well as special purpose system applications.

Houston Instrument's patented non-contacting capacitance feedback transducer replaces the slidewire and potentiometers, neatly eliminating the most troublesome components of X-Y servo systems.

For complete information contact Jim Bell, Houston Instrument, One Houston, Square, Austin, Texas 78753 (512) 837-2820. Outside Texas call toll free 1-800-531-5205. In Europe contact Houston Instrument, Rochesterlaan 6 8240 Gistel Belgium. Phone 059/277445.

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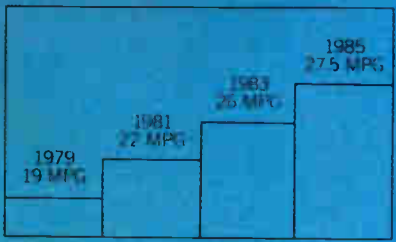
MOTOROLA HELPS STRETCH GAS MILEAGE

Automotive manufacturers are caught between a rock and a hard place. They are obliged not only to reduce fuel consumption, but also, at the same



Government mandated Corporate Average Fuel Economy (CAFE) standards. Source: NHTSA

time, to reduce harmful exhaust gas emissions. And these objectives seem to be mutually exclusive.

An engine whose carburetor and spark timing are adjusted to give high mileage tends to produce unacceptable levels of pollution. The same engine, adjusted for low pollution levels, uses more gas and gives disappointing performance.

The trick is to burn exactly the right amount of fuel at exactly the right moment. But what is "right" depends on a whole complex of constantly changing factors, including terrain, engine and air temperature, barometric pressure, and the load and speed of the car.

It would take a genius to juggle all those factors. Fortunately, Motorola has been working on the problem for some time, and has in fact produced just such a genius.

ELECTRONIC ENGINE MANAGER.

It's an electronic engine-management system, controlled by a microcomputer that thinks like a first-rate automobile mechanic. It lives inside the car, and because it can make a million calculations each second, it can automatically regulate carburetion, spark timing, and the recirculation of exhaust gases through the engine. It makes all these adjustments continuously, so you get as much performance with as little pollution as possible, whatever the driving conditions are at that particular moment.

It's a real computer in

BY MAKING ENGINES THINK.

miniature, with a memory and the ability to manipulate what it learns in terms of what it already knows. It works so well that car and heavy-duty-equipment manufacturers in America and Europe plan to use it, some as early as the 1980 model year.

IMPOSSIBLE WITHOUT ELECTRONICS.

Such precise, continuous engine management would be impossible without the integrated circuit, an electronic microcosm that contains the equivalent of twelve thousand transistors and measures about 5mm square. These small miracles are the central nervous system of Motorola's electronic engine-management system, and they're a remarkable but not unique demonstration of the kinds of things Motorola is doing with microelectronics today.

A microcomputer, shown larger than life

IMAGINATIVE ELECTRONICS.

Motorola is not only one of the world's largest manufacturers dedicated exclusively to electronics, but also one of its foremost designers of custom and standard semiconductors.

We've come a long way from the time when we put radios into cars fifty years ago, and TV sets into America's living rooms. Now we make hundreds of models of two-way radios, and we no longer make home TV sets here at all.

We make microelectronics carry telephone services to places where there are no phone lines. Transmit electrocardiograms and voice messages simultaneously from the scene of an accident to a nearby hospital. Help the energy industries develop the resources of the earth, the sea and the sun.

And we help make automobile engines think about how they use precious fuel.

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Circle 149 on reader service card

For further information, write Public Affairs Office, Corporate Offices, Motorola, Inc., 1303 E. Algonquin Road, Schaumburg, Illinois 60196.

Communications

CCD camera has high resolution

Unit with 248,832 pixels resolves 350 lines vertically and 360 lines horizontally

Using an image-sensing charge-coupled device with 248,832 picture elements (which it believes is the largest number so far reached by such a device), Matsushita Electronics Corp. has developed a monochrome video camera that combines high resolution with low weight, power consumption, and size. Capable of resolving 360 lines horizontally and 350 lines vertically, the completely solid-state camera measures 64 mm wide by 84 mm high by 149 mm deep and weighs only 540 g (without a lens). It draws a total of 4.7 W from three power supplies: +15 V, +8 V, and −12 V.

Because of the high reliability made possible by its all-solid-state design, the CCD camera is especially well suited to remote surveillance and measurement applications. Its size and weight should make it attractive for portable TV and video tape recorder applications, as well.

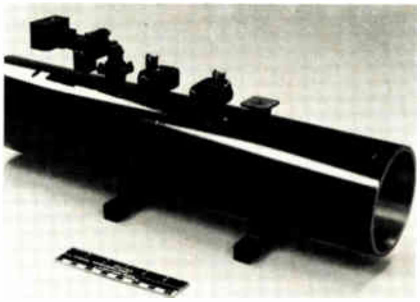
The camera will operate with a minimum light intensity of 10 lux and features a signal-to-noise ratio of 50 dB. Its 75-Ω video output delivers a standard peak-to-peak voltage of 1 V. The delivery schedule and price of the camera have not yet been determined.

Panasonic Electronic Components, One Panasonic Way, Secaucus, N. J. 07094. Phone (201) 348-7276 [401]

Traveling wave tube supplies 700-W cw power for Ku-band

The model 876H is a Ku-band traveling-wave tube that can supply 700 W of continuous-wave power from 14.0 to 14.5 GHz. A two-stage collector allows the tube to operate at efficiencies greater than 41% by lowering the total beam power when the drive level to the tube is reduced. This makes the tube desirable for pulsed operation and lessens the primary power drain when the TWT operates in its small-signal region.

By using a patented termination technique that has been successfully applied for several years in Hughes' coupled-cavity TWTs, the designers of the 876H were able to minimize



its phase distortion while keeping gain variation down to 1.2 dB across the 500-MHz band both at saturation and under small-signal conditions.

The 876H utilizes periodic-permanent-magnet focusing and forced-air cooling. It can be modified for power levels up to about 1,500 W. Measuring 22 in. long by 5 in. in diameter, the TWT weighs 28 lb. Priced at about $22,000, the TWT can be delivered in 9 to 11 months.

Hughes Aircraft Co., Electron Dynamics Divsion, 3100 West Lomita Blvd., Torrance, Calif. 90509. Phone Chuck Zilm at (213) 534-2121 [403]

TV transceiver communicates video data over phone lines

Designed to provide narrow-band video communications over standard voice-grade telephone circuits, the model 280 combines both transmission and reception modes to furnish video teleconferencing. The transceiver offers three functions: a frame freeze capability that captures a single image; conversion of this frozen picture into a slow-scan television signal suitable for transmission over audio channels; and reception and conversion of these TV signals into an immobile image on a normal TV monitor. The unit will operate in a moving environment.

When acting as a transmitter, the 280 receives a conventional CCTV input signal that is digitized and then fed into a solid-state memory. Once a transmit command is given, the memory is read out from left to right, with a cursor on the TV screen showing how much of the picture is left. Two sending speeds are available: 35 seconds for a single field picture with 240 by 256 picture elements, and 74 seconds for a full frame picture using 240 by 512 dot-interlaced pixels.

In the receiving mode, the 280 accepts the formatted, slow-scan TV input, and reconstructs the static picture, using the same solid-state memory provided for the frame freeze during transmission. The unit uses 6 bits to show 64 gray levels.

The transceiver sells for $8,000 if the lower resolution is selected, or for $10,000 if higher resolution is desired. Delivery time is within 60 to 90 days.

Colorado Video Inc., P. O. Box 928, Boulder, Colo. 80306. Phone Glen Southworth at (303) 444-3972 [404]

Microwave FET puts out 10 dBm at 10 GHz

A gallium-arsenide field-effect transistor intended for use in the frequency range from 2 to 12 GHz, the LND832 is a dual-gate device that typically offers a power output of 10 dBm at 10 GHz with a drain bias of 4 V. It will operate with drain biases as high as 10 V. The transistor is available as a chip with dimensions of 23 by 17 by 5 mils; it can also be mounted on carriers.

The multilayer devices use recessed gates and n^+ contract layers for resistance to burnout and breakdown. The chips, which are available from stock, sell for $150 each in quantities of one through nine.

Raytheon Co., Special Microwave Devices Operation, 130 Second Ave., Waltham, Mass. 02154 [405]

Instruments

Analyser has three clocks

Logic-state instrument aimed at multiplexed buses offers extra modes

Based on the pioneering model 1610A, Hewlett-Packard's latest keyboard-controlled logic state analyzer adds three-phase qualified clocks, a sequence protect function, and a memory retrieval mode for quicker and easier analysis of microcomputer and random-logic systems. Designated the model 1610B, the new instrument, which is especially well suited for analyzing multiplexed buses, can collect data on either or both edges of each of its three clocks. Altogether up to four OR-ed minterms may be used as qualifiers on each clock phase.

Three data-capture modes are possible with the 1610B: 32-bit, 16/16-bit, and 16/8/8-bit. The 32-bit mode is similar to that of the 1610A; the three clocks are OR-ed, and data is collected on each selected edge. In the other two modes, one clock is designated the "master" and the other two are "slaves." The master is the last to occur in sequence. As the clock pulses occur in sequence, the slaves strobe data into holding registers, and, at the end of each sequence, the master strobes all of the data into the analyzer memory.

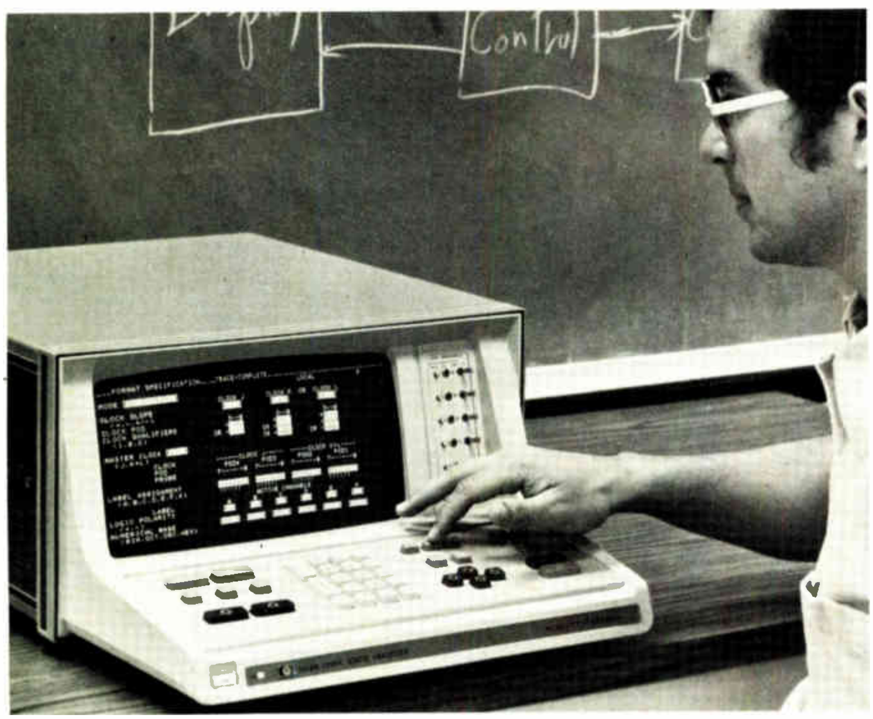
The 16/16-bit mode collects 16 data bits with one clock and the OR-ed combination of the other two clocks for the remaining 16 bits. In the 16/8/8-bit mode, the three clocks operate separately.

Emulator. The 1610B has a sequence protect function that, when activated, causes the analyzer to collect data in the same manner as the 1610A. Data storage begins after the last sequence term preceding the trigger point, and all sequence terms are displayed complete with labels. When the function is inactive, data storage is initiated immediately, and all of the 64 states relative to the trace point are captured. Sequence terms are neither labeled nor listed separately.

The new analyzer has a memory retrieval mode that allows the user to examine the contents of the analyzer memory even when a trace point is not generated—should the trigger sequence not be found, for example. In this mode the data listing is labeled HISTORY AT STOP or NO HISTORY AVAILABLE.

Options are available for connecting the 1610B to a thermal printer or to the IEEE-488 general-purpose interface bus. The basic analyzer sells in the U. S. for $12,500.

Hewlett-Packard Co., 1507 Page Mill Rd., Palo Alto, Calif. 94304 [351]



20-MHz pulse generator can deliver 2 A at ± 100 V

The model PG-13D high-power pulse generator is a versatile instrument that may be set to deliver pulses of up to ±100 V at ±2 A. It can put out its full power at frequencies from 1 Hz to 3 MHz. Its output amplitude drops with increasing frequency; at its top pulse repetition rate of 20 MHz, the output may be varied between 2.5 and 25 V at 0.5 A.

Both current- and voltage-output modes are provided. In the latter, the source impedance is approximately 50 Ω. In the former, the compliance voltage is specified in the region of 100 V.

Like most lower-power pulsers, but unlike many high-power units, the PG-13D provides variable rise and fall times, adjustable pulse widths and delays, and dc offsets. It sells for $2,980 and has a delivery time of 60 days.

Velonex, a division of Varian Associates, 560 Robert Ave., Santa Clara, Calif. 95050. Phone Perry McCown at (408) 244-7370 [355]

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REAL TIME...Yes, Real Time!

When the theme is fast changing and sweeping across the band, only real time interpretation gives full appreciation. If that's your scene, Surface Acoustic Wave chirp transform spectral analysis has got it taped . . . .

The W1748 Spectrum Analyser is based on real time chirp transform signal processing using SAW techniques. Basically the unit provides within an analysis time of 40μs, a 500 point resolution of analogue or digital signals in a 25 MHz bandwidth.

Designed for use in military airborne equipment as a fast spectral processor, the unit outputs the spectral content of input signals at a rate of 1 MHz/μs.

Frequency scaling techniques permit the analyser to operate at kHz bandwidths with the same resolution and intrinsic speed.

Specification

Bandwidth (1 dB)	25 MHz
Resolution (3 dB)	50 kHz
Spectral ripple	1 dB pk to pk
Max. input signal level	− 16 dBm pp (100 mV pp)
Dynamic Range (sidelobe limited)	30 dB
Dynamic Range (noise limited)	60 dB
Maximum output signal	1.28 volts pk
Processing time	40μs
Output data rate	1 MHz/μs
Duty cycle	50%
Power supplies	± 17V to ± 40V 1A + 7V to + 40V 1A
Internal Power	
Supply regulation	± 15V, + 5V
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Case	½ ATR short

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Lochend Industrial Estate, Newbridge, Midlothian, EH28 8LP, Scotland. Telephone: 031-333 2000. Telex: 72384.

RACAL

Circle 152 on reader service card

Products newsletter

TI expands ROM range for TMS1000 microcomputer

Later this summer, Texas Instruments Inc., Dallas, Texas, plans to offer two additional versions of the TMS1000 4-bit microcomputer, with different amounts of on-board read-only memory. **The TMS1400, with 4 kilobytes of on-board ROM, is expected to sell in the $3.00 to $3.50 range, and the TMS1700, a half-kilobyte version, will be priced between $1.30 and $1.50.** The original TMS1000 with 1 kilobyte of ROM is currently selling, in high-volume quantities, for about $1.75, while the 2-kilobyte TMS1100 goes for about $2.10.

Users may opt for varied instruments in single counter

Systron-Donner Corp.'s Instruments division in Concord, Calif., is poised to introduce a new family of universal counters that will allow users to specify exactly what they want in their instruments. **The UC1100 series will consist of a microprocessor-based mainframe that provides two identical channels, each equipped with controls and a display, to measure frequency, period, period averaging, time-interval averaging, and ratio, as well as complex-mixed simultaneous measurements.** The IEEE-488-compatible mainframe has a space for four instrument modules that initially will include: a 100-MHz input amplifier; a 3½-digit voltmeter to measure trigger levels and external voltages; and 512-MHz and 1.25-GHz prescalar inputs. Base price is about $2,000.

Graphics option adds adaptability to line printers

New graphics capabilities are sprucing up Okidata Corp.'s Slimline series of line printers. **With four different dot densities available—100 by 100, 70 by 72, 60 by 72, and 60 by 60—the microprocessor-controlled matrix printers can reproduce anything displayed on a cathode-ray tube.** This includes areas of solid black, maps, bar codes, charts, and labels, as well as character sets such as Arabic, Chinese, and Farsi, which require large matrices of dots. Priced at $95, the graphics option is available with the 125- and 250-line-per-minute printers from the Mount Laurel, N. J.-based firm.

Fiber-optic modems become more versatile

The asynchronous CRS-100 and synchronous CSY-100 fiber-optic modems from Canoga Data Systems used to be compatible only with the RS-232-C data-communications interface. **Now, at no increase in price, the Canoga Park, Calif., company is offering compatibility with MIL-STD-188, RS-422, RS-423, and CCITT standard V.35.** The move was a response to user requests, the company says.

Switches meet U. S. standards for Qualified Parts List

Analog switches have recently been added as a category to the U. S. Government's Qualified Parts List (QPL), **and Siliconix Inc.'s DG180 series of switches was among the first to receive this approval.** The QPL is part of MIL-M-38510—a Government standard covering semiconductor devices. QPL numbers for the analog switch category are 11101 through 11108, corresponding to the Santa Clara, Calif., firm's part numbers DG181, 182, 184, 185, 187, 188, 190, and 191. These switches are used in such equipment as military aircraft, missiles, spacecraft, navigational electronics, and detection systems.

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Engineer

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For designers working with microprocessor systems or battery backups, this regulator is ideal. (See specs left) If needed, DC voltage can be distributed to various 3T submodules throughout a system to eliminate voltage drop problems. And since hybrid power supplies have built-in isolation and low leakage, the 3T regulator is perfect for medical equipment, too.

At Boschert, we've been building off-line switching power supplies for nearly a decade. Over 100,000 of our multiple output power systems are now in operation. For any power requirement between 25-400 watts, at any volume level between 1 and 1000 a month, Boschert sticks with you. Today Boschert also sticks with OEMs who want to produce their own.

For more information on how our new 3T Switching Regulator takes the guesswork out of hybrid switching power supplies, contact your local Boschert representative. Or write Boschert, Inc., 384 Santa Trinita Avenue, Sunnyvale, CA 94086. Or call (408) 732-2440.

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