FEBRUARY 15, 1979

CC STILL WOWING THEM IN PHILADELPHIA/122

New IBM series bows to mixed reviews/ 85

64-K RAM features automatic- and self-refresh modes/ 141

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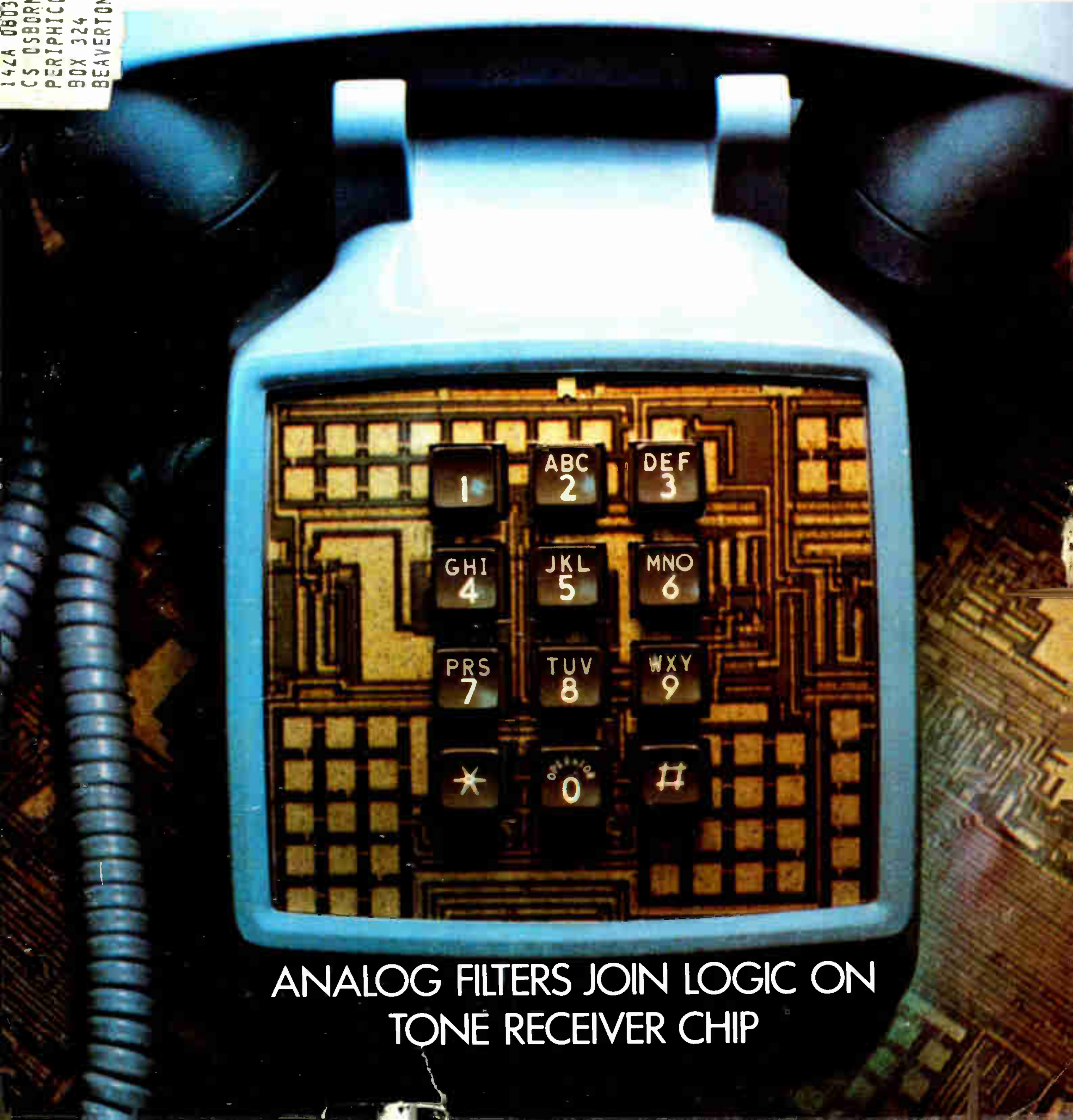

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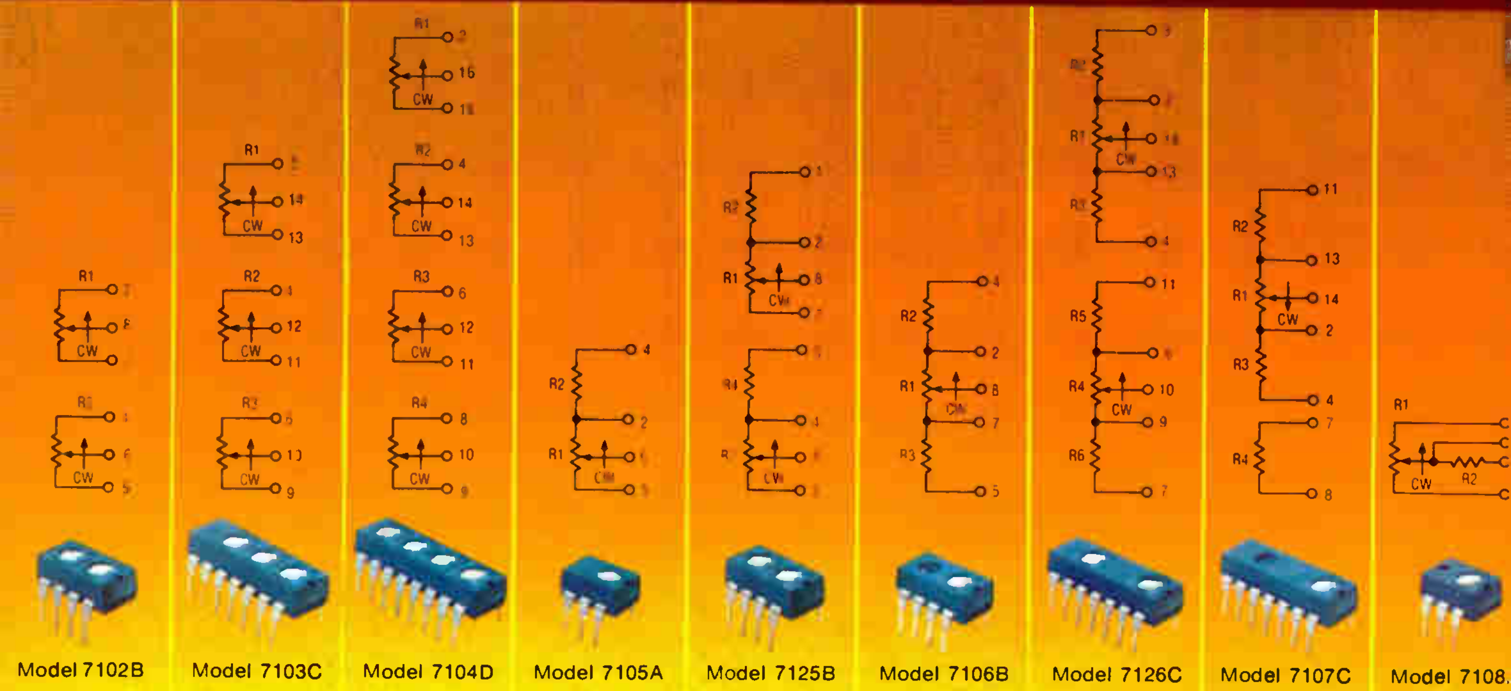

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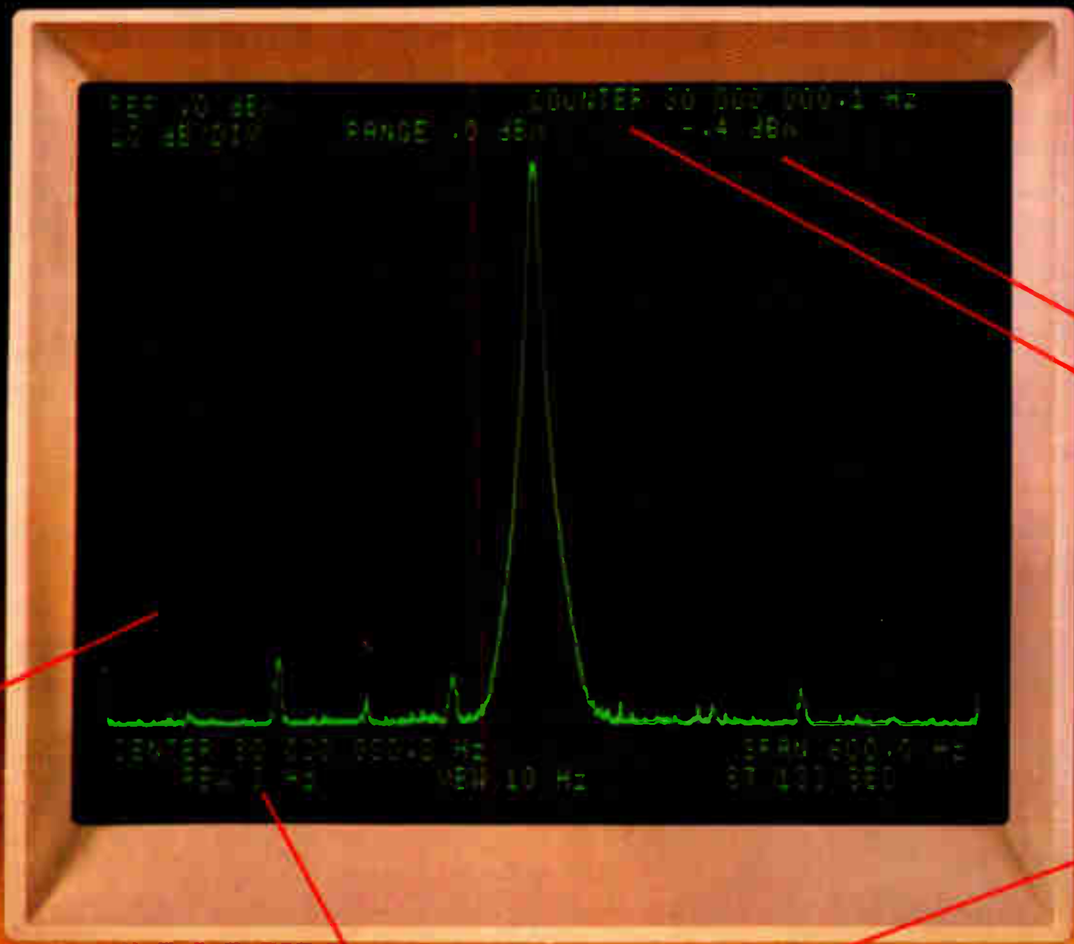

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098/45

Electronics

The International Magazine of Electronics Technology

Vol. 52, No. 4 • February 15, 1979

Highlights

Cover: Decoder chip merges analog, digital, 105
Switched-capacitor filters extend metal-oxide-semiconductor technologies into analog signal-processing systems. One result is a decoder that is the first single-chip telecommunications part to combine analog and digital blocks.

Cover photograph is by Art Director Fred Sklenar.

Chip testing faces greater challenges, 88
As manufacturers of test systems, chip makers, and chip users continue to argue about how to solve the problems of testing large-scale integrated circuits, very large-scale integration is making initial appearances. VLSI calls for the creation of entirely new approaches and increased communication among the three groups involved, says this commentary.

ISSCC: a hit once again, 122
The International Solid State Circuits Conference continues its role as *the* place to announce major technical advances in semiconductors. Two trends, especially, are growing: putting analog and digital functions on one chip, and using digital techniques for real-time signal processing.

64-K RAM refreshes itself, 141
Motorola's 64-kilobit 5-volt-only dynamic random-access memory takes a new route with its use of a single pin to control self-refreshing for both active and idle states.

And in the next issue . . .
A faster low-power family of Schottky transistor-transistor logic . . . how to design serviceability into microprocessors . . . sewing machines with electronic controls and touch switches.

Electronics

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Publisher's letter

There was a time when design engineers raised on analog technology had to learn painfully about digital technology. Well, the pendulum has swung, forcing many digital experts to cope with the mysteries of analog design. That is one reason why the team of George Lansberg, Bert White, and Gordon Jacobs of the technical staff for Silicon Systems Inc., Irvine, Calif., is unique.

This group was brought together about a year ago to design the switched-capacitor filter system described in detail on pages 105 through 112. Gordon, 23, did his masters degree research on switched-capacitor filter design at the University of California, Berkeley. There are not too many young engineers today who are knowledgeable on this subject.

Bert, 28, became involved in converter systems while designing with charge-coupled devices at Hughes. He was the systems man on the team. George, 34, brought to the group his experience with metal-oxide-semiconductor and analog integrated circuits, with special emphasis on codecs and converters.

"This is a unique team" George comments. "In fact, this system probably could not have been done by one designer in the time it took."

The group will probably continue to work together on other similar projects. "We still get along with each other after a year," Bert quips.

Taper-isolated cells . . . H-MOS II . . . analog microprocessor . . . multiprocessed linears. When words like these begin filling the air, it must be ISSCC time again.

As usual this year's conference is brimming with papers on the latest advances in memories, microprocessors, and linear devices.

The high points of the meeting are reviewed by solid state editor Ray Capece and components editor Nick Mokhoff in the article that starts on page 122. Higher performance is the keynote, according to Ray and Nick. Or, as Ray puts it, "chip manufacturers are not suffering from a shortage of sometimes startlingly innovative designs for boosting memory speed and density."

"Some of the more dedicated LSI circuit designs at ISSCC are quite intriguing, especially those that mix analog circuits with logic in what can only be the start of a trend towards analog-digital LSI," he adds.

As for the linears, Nick points out, "Active filters are this year what the codecs were a year ago, because the design problems that the codecs addressed were only the tip of the iceberg." In essence, interfacing the analog world with today's sophisticated processors has become a major undertaking that has led to the development of a variety of high-performance as well as linear circuits to use with them.

The annual index of *Electronics* articles, a handy compilation that can help you find anything we printed last year, will be available shortly. For a free copy, circle 340 on the reader service card.

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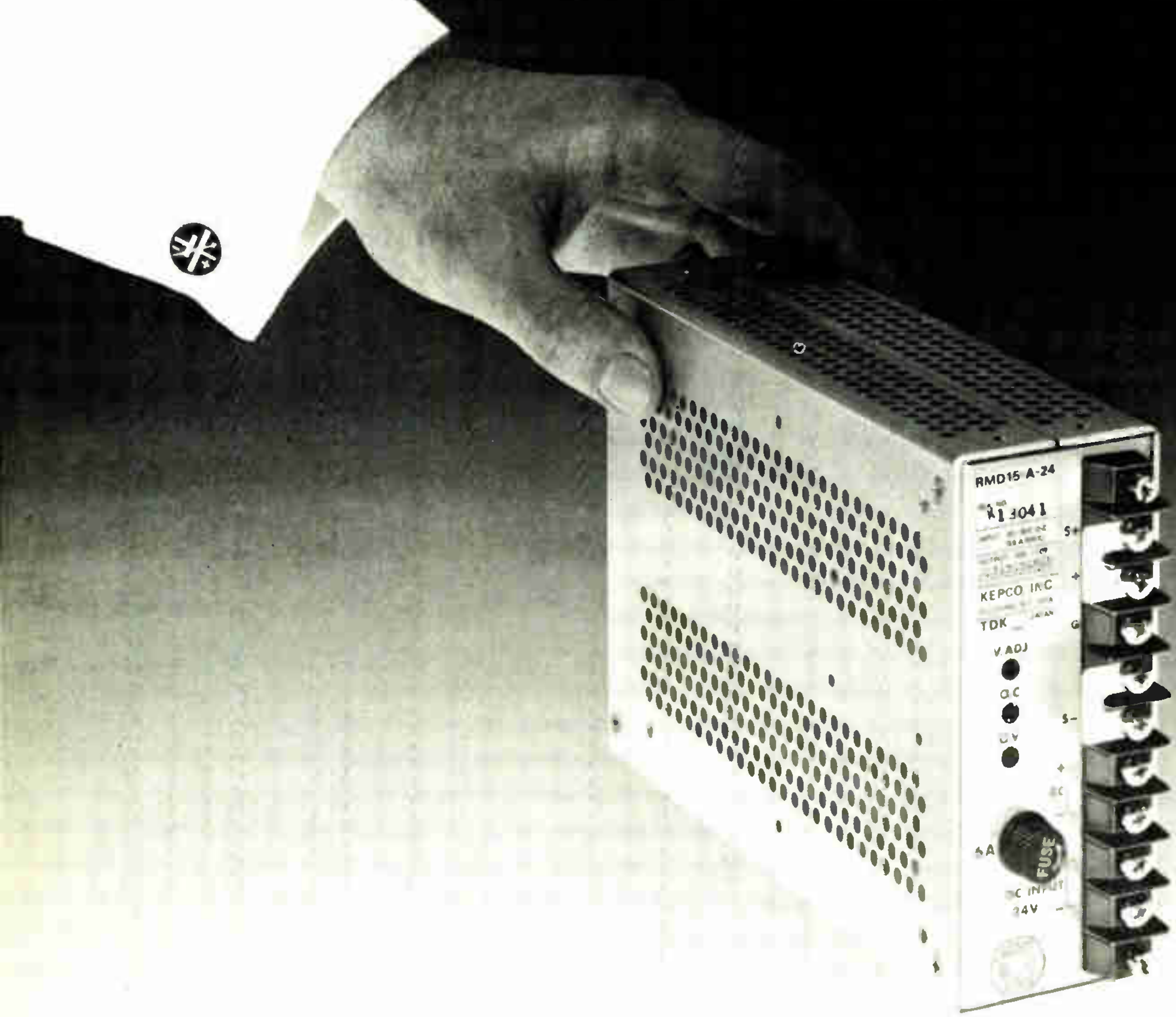

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Readers' comments

Missing

To the Editor: Your special report, "New networks tie down distributed processing concepts" [Dec. 7, p. 107], states: "In the United States the only public packet-switched network currently running is offered by Telenet Communications Corp."

Not only is there another public packet network, but it is older, larger, and financially more successful than Telenet. I'm referring to Tymnet, which is operated as a common carrier regulated by the Federal Communications Commission.

The Tymnet network has been fully operational since 1971, though it only began operations as a common carrier on April 1, 1977.

Ronald A. Bamberg
Tymnet Inc.
Cupertino, Calif.

Explaining the condition

To the Editor: I would like to correct a misstatement and eliminate possible confusion concerning the dc response capability of HP's fiber-optic links ["What designers should know about off-the-shelf fiber-optic links," Dec. 21, p. 89]. Operated normally in the internally coded mode, our link provides true dc response and thus has no restrictions on the data format whatsoever.

We do provide an option at the transmitter to disable our three-level optical internally coded mode (which gives us our dc response) so that our transmitter can be used with other fiber-optic receivers or for testing. With the transmitter in this mode, our receiver requires a 50% duty-cycle signal and a symbol rate above 2 megabauds. This is totally unrelated to the user's desire to encode clock and data together or the use of Manchester coding as claimed.

Lee Rhodes
Optoelectronics Division
Hewlett-Packard Co.
Palo Alto, Calif.

Correction

In "Hot time for ICs" (Jan. 18, p. 81), the figure shows the results of tests by General Electric Co.'s Electronics Laboratory, Syracuse, N. Y.

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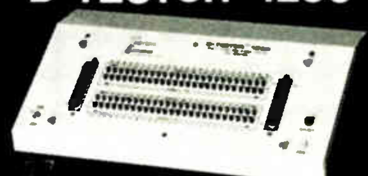

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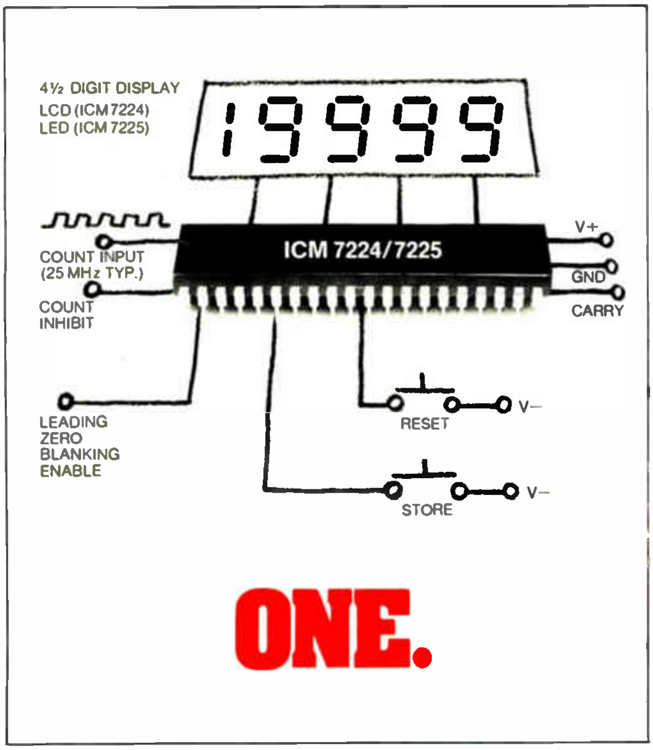

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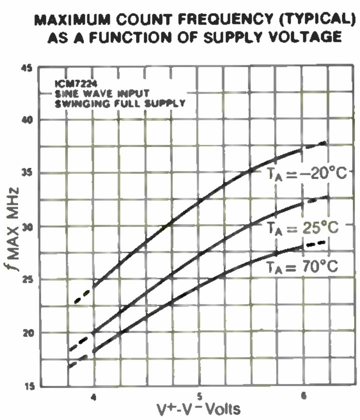

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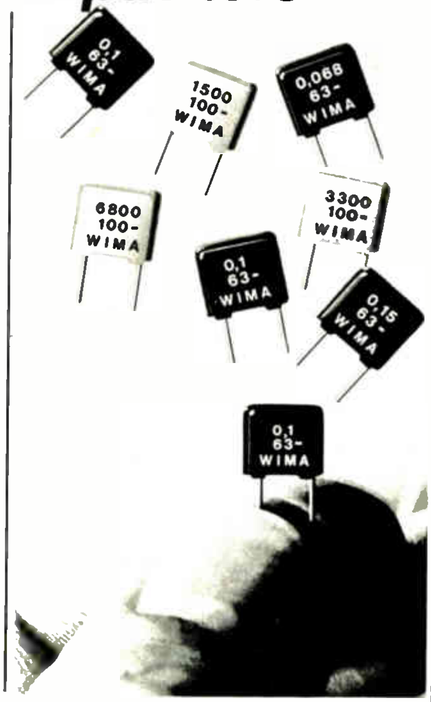

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News update

■ The makers of minicomputer systems that are plug-compatible with the machines making up IBM's System/370 may be headed for the edge of a cliff now that the giant has brought out its 4300 series [*Electronics*, Sept. 14, 1978, p. 88, and this issue, p. 85], but their attitudes and sales to date indicate otherwise.

For example, Two Pi Co., the Santa Clara, Calif., affiliate of Philips Industries of the Netherlands that started the trend, also leads the pack in deliveries—15 so far. Most have gone to National CSS Corp., Wilton, Conn., says Two Pi president Jared Anderson. During 1979, Two Pi will concentrate on furnishing large volumes of small integrated controllers that will allow users to tie their systems to minicomputer peripherals, he adds.

At National Semiconductor Corp., also in Santa Clara, the System 400 marketing group is "on a high" because of interest in the machine, says Ed McCurtain, manager of System 400 marketing. Despite industry reports of problems, "we've got one delivered so far that is still in [customer's] beta test, and we expect to begin production shipments by mid-February," he says. The focus has been on original-equipment manufacturers.

As for Cambridge Memories Inc. in Waltham, Mass., the first of its CM 1600 series went to National CSS last month. Kent E. Crombie, director of computer systems marketing, says, "The order rate is good and we have a substantial backlog." Peak production is set for April.

Another plug-compatible–system maker, Magnuson Systems Inc., delivered its first M80 series to Boston-based Mitrol, a systems house that offers manufacturing-information–management system software. "It all went well and they paid cash six days later," says L. James Beckman, Magnuson's vice president of marketing. A few more systems are in customers' beta testing, Beckman says; and the Santa Clara company has agreed to supply at least 10 systems to Scientific Time Sharing of Bethesda, Md.

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Standard 11/03-L systems are available as 1 Megabyte Double Density Floppy Disk based or 10 Megabyte Hard Disk Cartridge based RT-11® systems. These systems are available with choice of LA36, VT52 or VT100 as consoles.

	11V03-L		11T03-L	
Order Number	SRVXSSA	SRVXSSB	SRVXLLA	SRVXLLB
Backplane	KD11-H CPU	KD11-HA CPU	KD11-H CPU	KD11-HA CPU
	MSV11-CD, 16KW Memory	MSV11-DD 32KW Memory	MSV11-CD 16 KW Memory	MSV11-DD 32KW Memory
	Floppy Interface	Floppy Interface	MSV11-CD 16KW Memory	RL01 Controller
	DLV11-F Serial	DLV11-J Serial (4)	RL01 Controller	RL01 Controller
	BDV11 Bootstrap	BDV11 Bootstrap	RL01 Controller	DLV11-J Serial (4)
	Open	Open	DLV11-F Serial	BDV11 Bootstrap
	Open	Open	BDV11 Bootstrap	Open
	Open	Open	Open	Open
	Open	Open	Open	Open
Price	$9,475.00	$10,325.00	$16,265.00	$17,075.00
Delivery	30 Days	60-90 Days	30 Days	60-90 Days
Installation And 90 Day On-site Warranty	Included	Included	Included	Included
	By Digital Equipment Corporation			
Operating System	RT-11* V3B Plus Enhancements			
MOS Memory	16KW	32KW	32KW	32KW
Mass Media Storage	Dual RX02 Double Density Floppy	Dual RX02 Double Density Floppy	Dual RL01 5 Megabyte Cartridge Disk	

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First computer corporation

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"With microprocesso why take chances on

We keep hearing that microprocessors are all things to all people. Yet, at AMI, orders for custom-designed circuits continue to grow. And, when you take a realistic look at standard microcomputer systems versus made-to-order circuits, it isn't hard to see why.

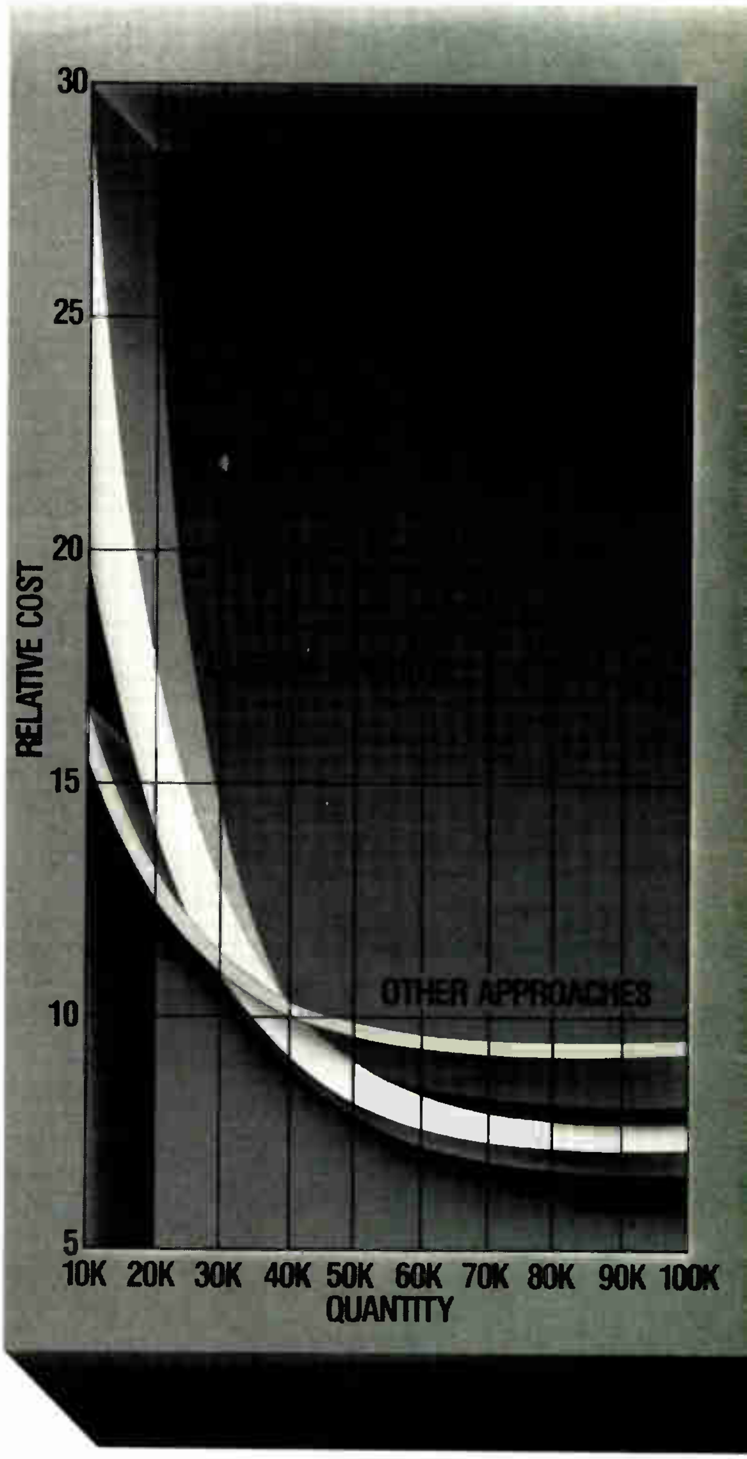
First, consider capabilities. While it's true that many products using custom circuits could be controlled by microprocessor systems, there are some that clearly couldn't.

For instance, we just produced a custom MPU for a commercial avionics system. It required a series of interrupts that the architecture of a standard microprocessor wouldn't provide. Special display drives, A/D conversion on inputs and specialized high-speed calculations are other areas where off-the-shelf products are clearly outclassed in this application.

Second, look at the real costs of both systems. On the one hand, custom assures the minimum number of circuits. And, although there is some start-up expense, this is easily amortized over the life of the product. On the other hand, standard microcomputer configurations usually require a number of components, taking up more board space, assembly effort and testing time. These costs can run you at least 50% of each part's price. So a multi-circuit microprocessor system often represents as much in indirect costs as in the price of the circuits themselves. These factors alone can make a standard system less cost-effective than a custom job. And that doesn't even include the time and expense involved in programming. You can spend as long getting your software written as we would building the custom hardware.

Standard and custom should be partners, not competitors.

In many cases, a 'mixed solution' works

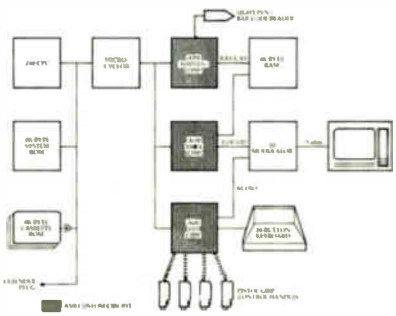


Is custom expensive? The chart shows that it can actually be more cost-effective than standard devices as the unit volume approaches 30,000 and when assembly, programming and test are taken into consideration.

rs a dime a dozen, custom LSI?"

best—a combination of standard microprocessor and custom peripherals. For instance, we designed a special circuit for a consumer entertainment company to expand the I/O capabilities of a standard 8048 MPU. And for a manufacturer of business equipment, we're working on plans to customize an S2400 (our 4-bit microcomputer) to provide ROM and RAM variations, adding a custom interface chip and clock. To help them get the product to market while we're developing this more cost-effective solution, we're providing them with our standard S6802 8-bit microprocessor.

An advanced home computer provides another example of standard and custom compatability. A Z-80 microprocessor is supported by three AMI custom circuits—address, I/O and data chips. This trio contains the equivalent of 600 standard SSI and MSI integrated circuits. And, having a fast MPU to work with, our circuits were designed to run at seven MHz. Most important, they perform the intricate graphics functions, lowering the cost to the point where the computer does more for the money than competitive products.



A triple option: this home computer uses a standard microprocessor, three AMI custom peripherals, plus standard ROMs and RAMs to achieve more performance for the money than any competitive system.

It's apparent that microprocessors, far from shrinking the need for custom, have actually opened up vast new areas of application. In fact, you now have three ways to go—full custom, standard microprocessor or a mixture of both. Since we're the leading custom LSI company *and* a major supplier of microprocessors (the 4-bit S2000, 8-bit 6800 and 16-bit 9900) and memories, we're in the best position to supply your complete microprocessor system needs.

Want to know more? It's in the book.

Titled "Six Steps to Success with Custom LSI," our new brochure should answer many of your questions. Such topics as timing, options, processes, test and manufacturing are thoroughly covered, along with a variety of case histories.

It also explains the flexibility that AMI offers. Since we work in 25 variations of four MOS processes, we don't have to reduce your product's capabilities to fit design or production limitations.

Unlike smaller companies, we're also organized to work with you in any of three different ways. We'll design and produce your circuit from scratch. Or you can handle the design in-house or through a third party, then we'll manufacture it. Or we can arrange a joint venture, where a team from your company and a team from ours work together to create a succession of new products.

Whichever way you decide to go, you'll have the satisfaction of working with the company that wrote the book on custom MOS. Since 1966, we've created more than 1200 different circuits. We're continually finding new ways to get more onto a chip (up to 67,000 transistors at last count) in less time. As a result, we average seven months from firm specifications to fully tested circuits—the fastest turnaround in the industry.

Why don't you explore all these opportunities with us? To start with, ask for a copy of our book. Write or call AMI Custom III Marketing, 3800 Homestead Road, Santa Clara CA 95051. Phone (408) 246-0330. Or contact one of these AMI sales offices: California, (213) 595-4768; Florida, (305) 830-8889; Illinois, (312) 437-6496; Indiana, (317) 478-9339; New York, (914) 352-5333; Pennsylvania, (215) 643-0217; Texas, (214) 231-5721; Washington, (206) 687-3101.

And, if you'd like your questions answered in person, we'll make a half-hour presentation right in your office. We think it will help convince you that getting into custom isn't chancey at all.

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HAVE IT

Chances are you're already familiar with Teradyne's L529. This in-circuit test system is well-known as a reliable, economical way to expand board-test capacity.

Now take a good look at the new L527, an equally productive in-circuit tester.

The difference is that the L529 comes with our innovative Pressure Rod Handler, and the L527 is designed to interface with whatever fixturing system you're using now.

How our innovative thinking boosts your productivity.

The L529 and L527 excel at prescreening the faults that occur most frequently: errors in manufacturing and workmanship. Both systems quickly detect a high percentage of such faults as shorts, opens, and missing, backward, or wrong-value components.

Our superior test electronics and diagnostic capabilities make these systems highly cost-effective ways to test analog, digital, and hybrid boards.

Our systems save you time and money.

Both our systems contain pre-planned test routines and the capacity to self-learn test limits from good boards.

A junior technician can program a board in hours, freeing your engineers for more productive work.

What's more, both the L529 and the new L527 deliver clear, concise error messages in your own product language. Non-technical repair people

Teradyne's L529 Assembly Inspection System

YOUR WAY.

can pinpoint faults quickly and easily.

More ways we save you time and money.

The L529 with its Pressure Rod Handler solves a lot of problems. It eliminates vacuums and precision tooling while giving you positive, dependable contact. You'll find our Pressure Rod Handler an elegant solution to a difficult problem.

And here's another advantage. With Teradyne's Fixturing Kit you can build your own bed-of-nails fixtures in-house and in just a few days. When ECO's pop up you can handle them immediately, and that means less downtime and more productivity.

The New L527 is a significant opportunity.

We realize that some of you are satisfied with your current fixturing system. To you we offer the new L527. It adapts easily to the handler you're using now, giving you increased board-test capacity without requiring any additional investment or start-up effort.

Teradyne means productivity and reliability.

The L529 and new L527 are obviously productive, but be assured they're reliable, too. All Teradyne systems are built for hard use and backed up by the best support program in the business.

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TERADYNE

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Teradyne's L527 Assembly Inspector

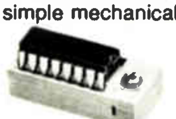
NEW TEXTOOL ECONO ZIP PRODUCTION SOCKETS

New TEXTOOL inexpensive ECONO ZIP socket series features easy, safe zero insertion and extraction pressure for "end-user" production requirements.

TEXTOOL's new low cost ECONO ZIP series of production sockets are especially designed for those applications where initial loading and field replacement of expensive IC's are a necessity and socketry is an absolute requirement.

ECONO ZIP sockets are available in 16, 24 and 40 pin models. They are designed for mounting on standard .100" centers on either axis.

The ECONO ZIP socket is designed for the most simple mechanical action. A device can literally be dropped into the socket. Rotation of the cam to a built-in stop firmly retains the device with exceptionally good electrical contact. Counter rotation of the cam releases the device, thus providing zero pressure during both insertion and extraction.



These economical (U.L. approved plastic) production sockets offer additional device protection features including wide entry holes to accept bent or distorted leads that don't have to be reformed prior to insertion, a screw driver operated plastic cam for easy operation and prevention of accidental unloading, and extremely long life (hundreds of actuations).

Detailed technical information on new low cost ECONO ZIP production sockets is available from your nearest TEXTOOL sales representative or the factory direct.

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Circle 14 on reader service card

People

IEEE's Herz to balance demands of members

As Eric Herz talks about his new job—general manager of the Institute of Electrical and Electronics Engineers—his listener envisions a juggler earnestly working to keep a clutch of tenpins aloft. For he talks about the challenge he faces as the IEEE's top administrator in terms of balancing demands, and he chooses his words carefully in discussing those demands.

Turning pro. Long-time volunteer Eric Herz takes over as IEEE general manager.

Roughly half of the institute's 300-odd employees are in editing and publishing activities, with the rest ranging across a spectrum from Washington lobbying to standards setting. Add to this the numerous volunteers and the rest of the 191,000 members, and the sum is many, and sometimes conflicting, voices to which Herz must attend. So he speaks cautiously in outlining his responses to what he hears.

Herz, 51, took over his position on Jan. 1, moving to the IEEE's New York City headquarters from San Diego, where he was a senior project engineer for the Convair division of General Dynamics Corp. Long active in the institute's affairs, he knew what he was plunging into.

A key task, he says, is to make the staff more responsive to members' needs. "I lead myself to believe I have some warm feeling for what people are looking for in the institute," he claims, pointing to his 20 years of volunteer work in section and region operations and in the IEEE's technical activities, where he capped his service by becoming the 1978 vice president for technical activities.

Herz will not directly criticize the mode of operations he inherited, but ideas for its improvement pervade his conversation. "If I can translate the [membership's] needs accurately, I think the staff will do a good job in responding," he summarizes.

Differing interests. Herz is circumspect when asked about the IEEE's socioeconomic activities. "We are not a society of common interests, but one of a diversity of interests," he observes. The members are working engineers, managers, entrepreneurs, government employees, teachers, and students, "and we need all for a good organization."

Still, he sees a board of directors' mandate for a broad spectrum of activities, including some socioeconomic activities. "The challenge is how to balance demands for more services with the institute's income," he says.

Linear designers pursuing higher speeds, says PMI's Erdi

Where speed and power are of paramount importance, scaling down geometries will not be as simple for future analog chips as for digital ones. Designers will be constrained by larger voltages that limit shrinkage, as well as by the need to preserve or even improve accuracy. That is what George Erdi sees in his crystal ball.

Erdi, 40, a veteran analog designer at Precision Monolithics Inc., has just been named staff vice president for design. The prize for being first with quality high-speed devices will be a larger share of the linear business, which Erdi says continues to grow faster than the overall market.

"There's plenty of room for improvement in monolithic a-d [analog-to-digital] converters," he says. "We've barely scratched the surface." Higher speeds, greater accuracy, and wider temperature com-

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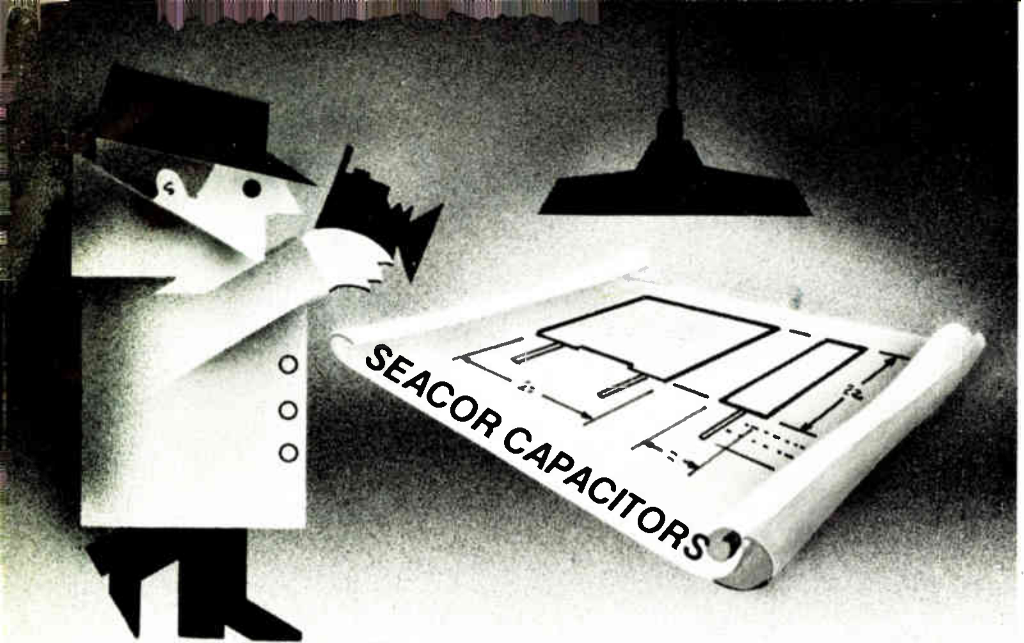

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And, even if brands X, Y and Z aren't so meticulously made, it is hard for you to be sure of that. The bottom line, therefore, is that our prices and deliveries have to be at least as good and when possible better.

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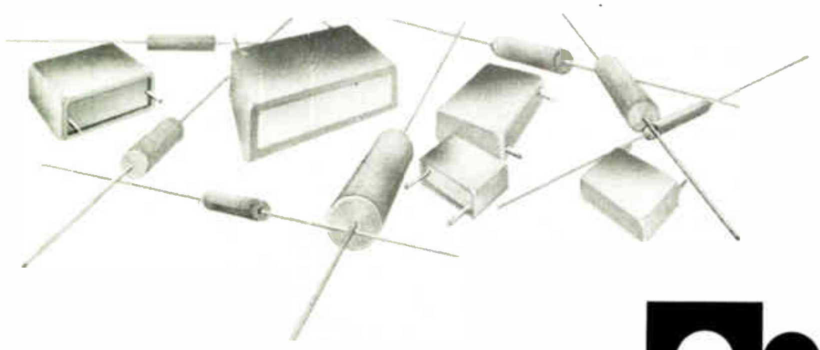

Everything in Film Capacitors

Circle 16 on reader service card

People

Limited. Too many technologies may spread a company too thin, says Erdi.

pensation are just some of the parameters to be improved, he continues. Higher slew rates for operational amplifiers and more precise control of on-resistance in bipolar analog switches will also be designer targets, he predicts.

However, Erdi sees a danger in designing with multiple technologies to achieve particular parameters. It is unlikely that any designer will be expert in several technologies, so several designers may work on the design. The end result of this "design-by-committee" may be "spoiled-broth-on-silicon," Erdi says.

Hungarian-born, Erdi came to Canada after the 1956 revolution and earned his BSEE in 1965 at McGill University in Montreal. He got an MSEE at the University of California at Berkeley the following year and joined Fairchild Camera and Instrument Corp.'s Palo Alto, Calif., research and development laboratory. There he designed the UA 722 digital-to-analog converter and the UA 725 monolithic precision operational amplifier.

Since moving to PMI in May 1969, Erdi has had a hand in designing some 17 products that account for more than half of the Santa Clara, Calif., company's $15 million in annual revenue. He's glad, he says, that, despite his promotion, he can still keep doing what he loves best—designing linear circuits. □

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just show me a way to
reduce connector hardware
costs without cutting down
the reliability as well."

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When you switch to the AMP Metrimate Connector line be ready to save as much as $3.50 per connector. In your product and assembly costs. And in your inventory costs. Because Metrimate gets rid of separate pin hoods, mounting hardware and connecting parts. It molds all of them into a housing designed to true metric dimensions.

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Look into the savings. Call the AMP Metrimate Information Desk at (717) 564-0100, Ext. 8400. Or write AMP Incorporated, Harrisburg, PA 17105.

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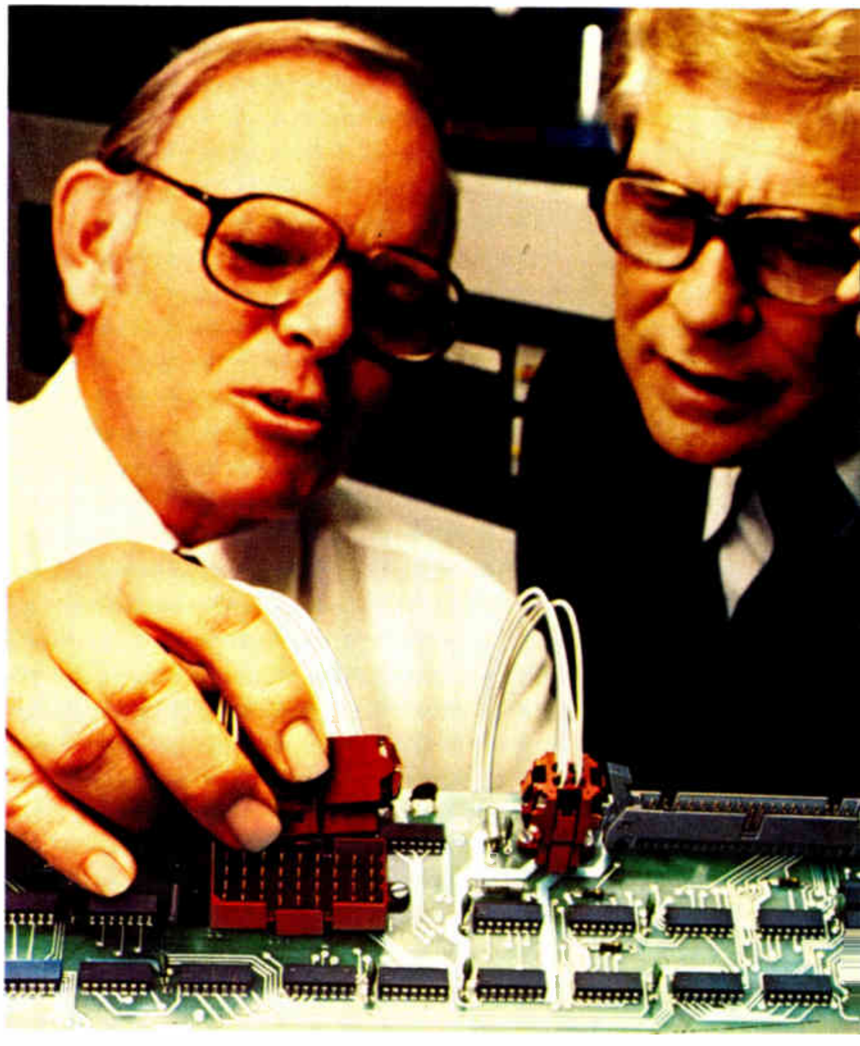
AMP has a better way.



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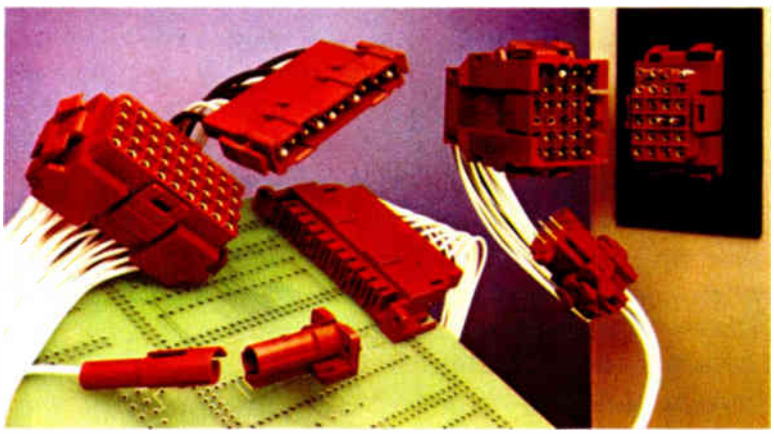

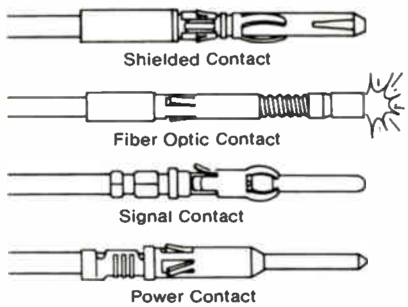

Some facts worth knowing about AMP Metrimate Connectors

Description: Part of AMP's exclusive Multimate Family that accommodates common contacts in a variety of connector housing styles and saves on both tooling and inventory costs.
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Dielectric strength: 1500 volts rms at sea level
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Insulation resistance: 5000 megohms, min.
Contact resistance: 5.5 milliohms, max.
Durability: 250 cycles, tin-plated contacts
550 cycles, gold-plated contacts
Where to telephone: Call the Metrimate Information Desk (717) 564-0100, Ext. 8400.
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AMP

Circle 19 on reader service card

The Mostek 16K

5 volt systems, the easy way.

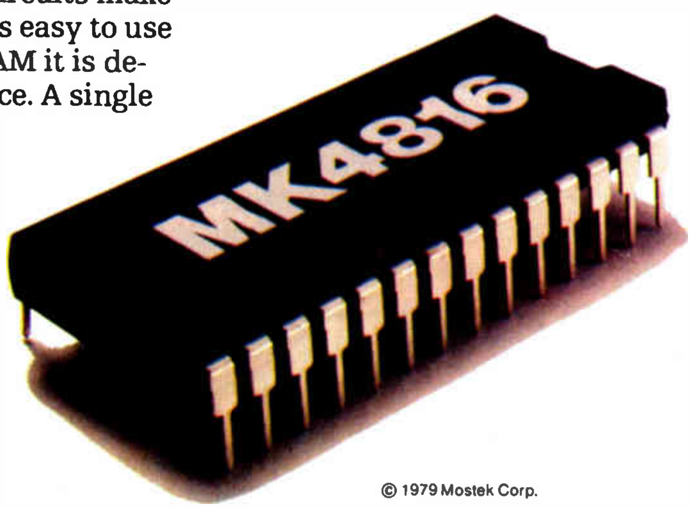
Now there's a total solution to 5 volt microcomputer systems. Mostek's new 4816 makes it easy. It's 5 volt only. It's 2K x 8. It's a compatible Micro Memory™ from Mostek.

Easy as static.

The 4816 is as easy to use as static RAMs, but offers all the performance and cost advantages of dynamic RAMs. The 4816 uses a dynamic cell and dynamic periphery to reduce die size to just 31,000 mils² as well as power dissipation to only 25 mW standby and 150 mW active. Access time of 150ns and cycle time of 270ns meet the needs of all microprocessor sockets.

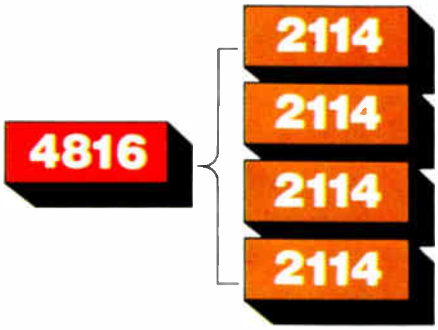
Easy to refresh.

On-chip logic, refresh and interface circuits make the 16K RAM as easy to use as the static RAM it is designed to replace. A single refresh pin allows flexible control of refresh, or automatic refresh in battery back-up mode. The timing of the refresh pulse is so flexible that it can occur during an active cycle or standby mode. In most 8-bit microprocessor systems as well as the new generation 16-bit microprocessors, the refresh pulse may be conveniently generated from the processor's output controls. In the Mostek system solution, our Z80 provides a refresh output signal that connects directly to the refresh input of the 4816. The 4816 appears totally static to the system.



Easy to upgrade.

Upgrading your system is as easy as replacing four 2114s or two newer generation 8K static RAMs with a single MK4816 to improve speed and density while reducing power and costs.



The 4816 is totally compatible with standard ROMs, PROMS, and EPROMs as well as next generation Micro Memories from Mostek.

The 4816 is available now for your system. Just call 214-245-0266 for more information. Mostek Corporation, 1215 West Crosby Road, Carrollton, Texas 75006. In Europe, contact Mostek Brussels; phone (32)02/660.25.68.

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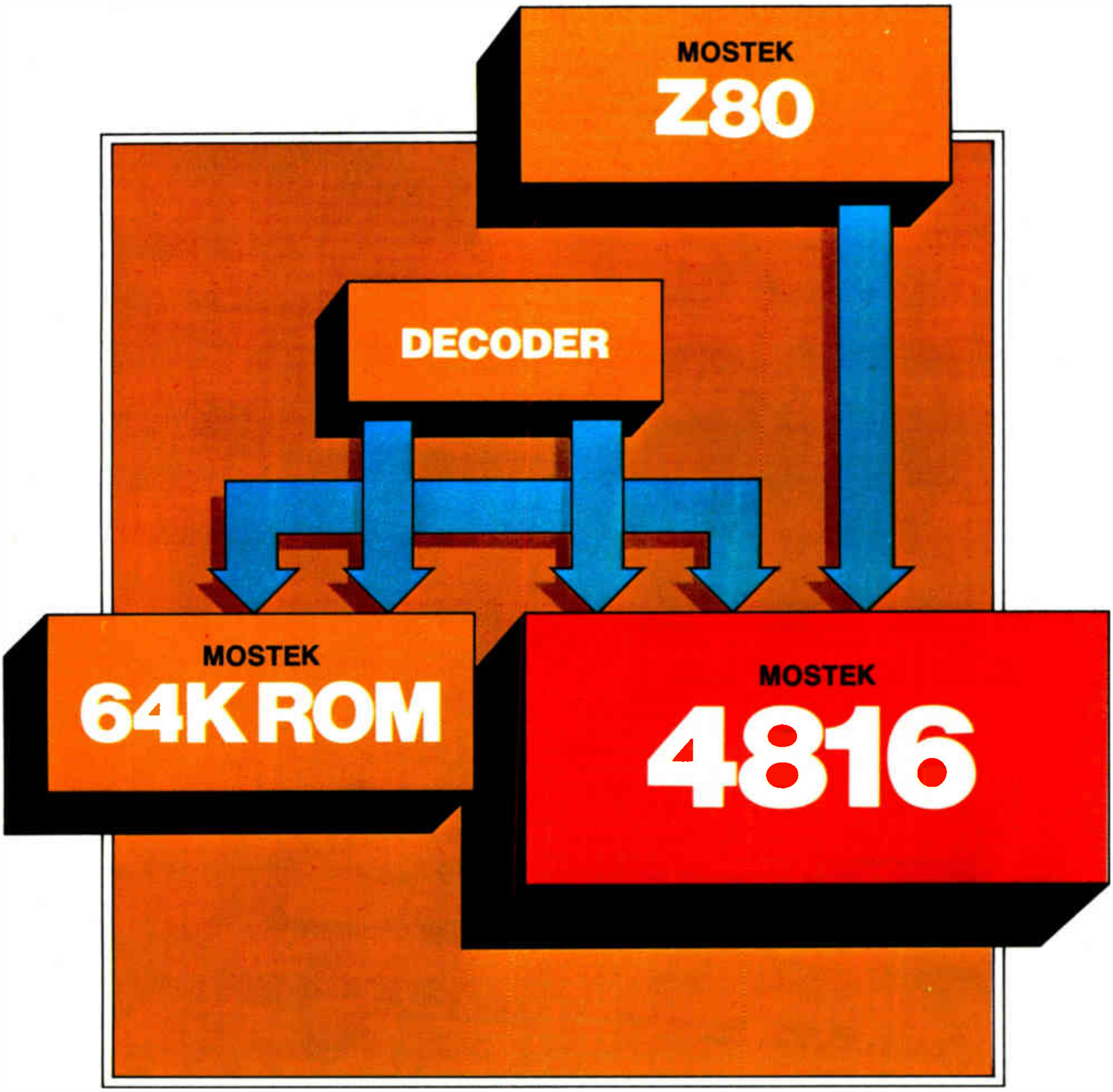
Micro Memory



Mostek's 5 volt System Solution

Circle 21 on reader service card

Introducing HP's System 35.

Under its friendly exterior lurks the power of a minicomputer.

The new System 35 delivers minicomputer performance while retaining those friendly characteristics of a desktop computer. Consider these features:

Big Memory—you choose from 64K to 256K bytes of internal read/write memory, of which all but 12K bytes are available for your programs and data. With 256K bytes, System 35 can manage an array of over 30,000 12-digit floating-point numbers. That's big problem-solving capacity.

Enhanced BASIC Language possesses some powerful, convenient features you'd normally find only in FORTRAN or APL. It's the same HP enhanced BASIC used with System 45 so you can step up to a bigger system without having to rewrite your programs.

Assembly Language is an option for those who are skilled assembly programmers to provide increased power and speed for data acquisition and control applications.

Real-time I/O performance makes System 35 an extremely powerful desktop controller. With direct memory access, buffered I/O, 15 levels of priority interrupt, built-in I/O drivers and standard interface options, System 35 handles data acquisition and control tasks with ease.

Yet with all its built-in performance, System 35 remains a friendly, easy-to-use computer. It integrates essential functions such as alphanumeric display—your choice of 24-line CRT or single line LED—typewriter-like keyboard, and a 217K byte magnetic tape drive in one trim, portable package. If needed, you can easily plug in external HP peripherals such as printers, plotters and floppy discs which, for convenience, use the same mass-storage commands as the built-in tape.

For immediate information on System 35, call your local HP desktop computer representative. For literature, send us the coupon, which will expedite its return, or circle our reader service number.

HEWLETT PACKARD

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408/3

Editorial

Speaking the same language . . .

Designers of systems have enough troubles, so those normally gentle souls must be forgiven the dark thoughts they sometimes harbor about software. To the electronics engineer, the arcane art of software writing is a time-consuming and sometimes frustrating experience that seems calculated to cause pain, though it is a vital task that is becoming more so every day.

That's why the experiences of the folks trying to bring us a standard form of that nifty and lately very popular language, Pascal, must bring a bitter and knowing smile to the lips of the average workaday EE. There seem to be enough groups and subgroups, each with its own perfectly good reasons for doing things its own perfectly good way, to mobilize several alphabets. We have ANSI, BSI, and ISO for the standards institutes of America, Britain, and the world; then we have PUG and, for good measure, the IEEE, for the Pascal Users Group and the engineers. The basic division is between the academicians, who seem to want the language to stay "pure" insofar as it hews to the word laid down by Pascal's author, Niklaus Wirth, and the industrial users, who appear to be intent on including modifications and extensions to Pascal right in the standard. And there is even a third group, one that feels there is no need to write a standard at all, that every computer maker should be free to incorporate its own form of Pascal programming.

As the article on page 96 describes it, a meeting to talk about standards last December got so involved with intergroup wrangling that the participants did not even get around to electing a chairman; all they managed to accomplish was to schedule another meeting for this month. With Pascal's popularity growing as it is, and with the digital world so dependent on software, now would be a good time for each side to see the merits of the other's view and give a little.

. . . even if it's a secret

While on the subject of languages and standards, the brouhaha in Washington over encryption is worth examining. It seems the National Bureau of Standards has come up with a Data Encryption Standard (DES) that has become the center of a storm. The standard was written because of the growing use in the commercial world of codes and ciphers, a practice that just a few short years ago was limited to the world of diplomacy, spies, and similar activities that most of us know only from novels, movies, and television shows. The problem here, however, is the super hush-hush National Security Agency, whose charter is to become involved in and safeguard the nation's communications where they involve national security. But the agency is specifically prohibited from involving itself in commercial or nonsecure Government communications, and there's the rub. Some commercial communications people say the NBS, while it says its DES was put together in consultation with the NSA, fell too much under the influence of the super spooks and the result is an inferior standard. On the other hand, the NSA now says it must have first censorship rights on governmental encryption contracts, so that it can safeguard America's security, a form of supervision that seems almost impossible in a democratic system.

The NSA cannot win everything it wants, and its stand is only holding up promulgation of a good standard, whether DES or any other. Despite the fact that its director, Vice Admiral Bobby Inman, took an unheard-of step when he went public at a meeting to plead his case, the NSA would be well advised to negotiate on this matter.

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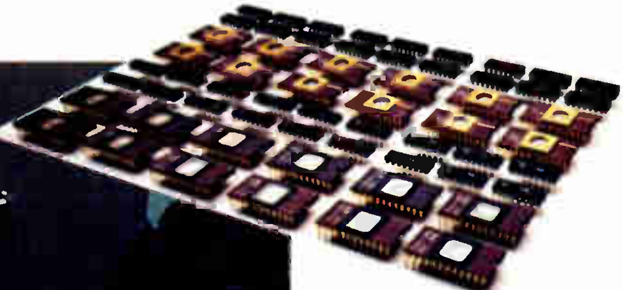

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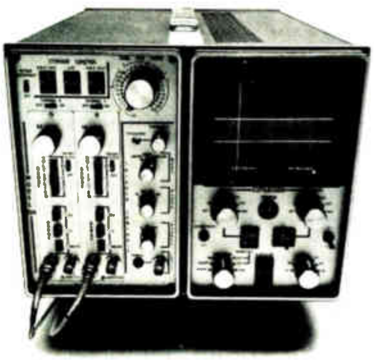

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Meetings

Recent Advances in High-Frequency Communications, Institute of Electrical Engineers (London), Savoy Place, London, Feb. 26–28.

Sixth Energy Technology Conference and Exposition, Electric Power Research Institute (Palo Alto, Calif.), Sheraton Park Hotel, Washington, D. C., Feb. 26–28.

Compcon Spring '79 — 18th IEEE Computer Society International Conference, IEEE, Jack Tar Hotel, San Francisco, Feb. 26–March 1.

Intelcom 79 — International Telecommunication Exposition, Horizon House International (Dedham, Mass.), Dallas Convention Center, Dallas, Texas, Feb. 26–March 2.

Digital Microwave Transmission Seminar, IEEE and Princeton University, at Princeton University, Princeton, N. J., Feb. 27.

Digital Encoding and Processing of Voice and Video Seminar, George Washington University, Washington, D. C., Feb. 27–March 1.

Nepcon West '79, Industrial and Scientific Conference Management Inc. (Chicago), Anaheim Convention Center, Anaheim, Calif., Feb. 27–March 1.

ICE '79 — International Computer Exposition, Marcom International Inc. (Tokyo) and Golden Gate Enterprises Inc. (Sunnyvale, Calif.), Tokyo Harumi Fairgrounds, Tokyo, Feb. 28–March 2.

Optical Fiber Communication Meeting, the IEEE and the Optical Society of America, Shoreham Americana Hotel, Washington, D. C., March 6–8.

Conference on the Electronic Printer Industry, Dataquest Inc. (Menlo Park, Calif.), Orlando Hyatt House, Orlando, Fla., March 7–9.

Mid-Atlantic Computer Exposition, The Caravan Group (Newton, Mass.), New York Coliseum, New York, N. Y., March 13–15.

12th Annual Simulation Symposium, IEEE, Causeway Inn, Tampa, Fla., March 14–16.

Fifth Annual Conference and Exhibit on Industrial and Control Applications of Microprocessors, Information Gatekeepers Inc. (Brookline, Mass.), Sheraton Hotel, Philadelphia, March 19–21.

IECI '79 — Industrial and Control Applications of Microprocessors, IEEE, Sheraton Hotel, Philadelphia, March 19–21.

Automatic Testing Deutschland and Test and Measurement Exhibition '79, Network/Watts Steadman Ltd. (London), and Gene Selven & Associates (Cupertino, Calif.), Rhein-Main-Halle, Wiesbaden, West Germany, March 20–22.

Eighth Annual Programmable Controllers Conference and Equipment Display, Engineering Society of Detroit, to be held at the society's headquarters, March 20–22.

Corporate-Wide Packet-Switched Data Networks Seminar, Data Communications Magazine/McGraw-Hill Publishing Co. (New York), Capital Hilton Hotel, Washington, D. C., March 26–27.

Trends in On-Line Computer Control Systems, Institute of Electrical Engineers (London), University of Sheffield, Sheffield, UK, March 27–29.

International Standard X.25 Interface Protocol for Packet Nets and Related Protocols Seminar, Data Communications Magazine/McGraw-Hill Publishing Co. (New York), Capital Hilton Hotel, Washington, D. C., March 28–29.

Southeastcon — 1979 Southeastern Conference, IEEE, Hotel Roanoke, Roanoke, Va., April 1–4.

Spring Conference, EIA, Shoreham Americana Hotel, Washington, D. C., April 2–5.

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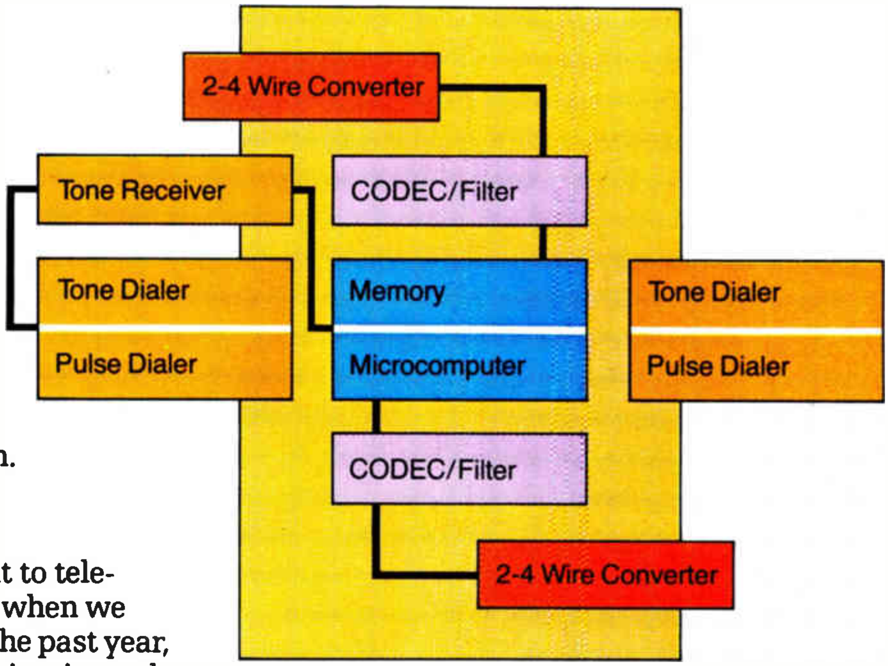

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The outcome was actually two models. The HP 2621A, which sells for $1450. And the HP 2621P, which has a built-in printer, costs $2550. You obviously want the sharpest display made. So we used the 9x15 character cell you see on every HP CRT terminal, including the top-of-the-line. And, to help you look back at the data you've entered, we provided two full pages of continuously scrolling memory.

We designed the keyboard like the familiar typewriter, so you don't have to waste time relearning it. We built in eight function keys, too. These control the cursor, rolling and scrolling. And, to make life easier, they're labeled on the screen for self-test, configuration, display and editing.

Editing? On a simple terminal? Certainly. We included character and line insert and delete, clear line and clear display. And, since the 2621 keeps your input separate from your CPU's, you can edit data before sending it to the computer. All without writing a line of system software.

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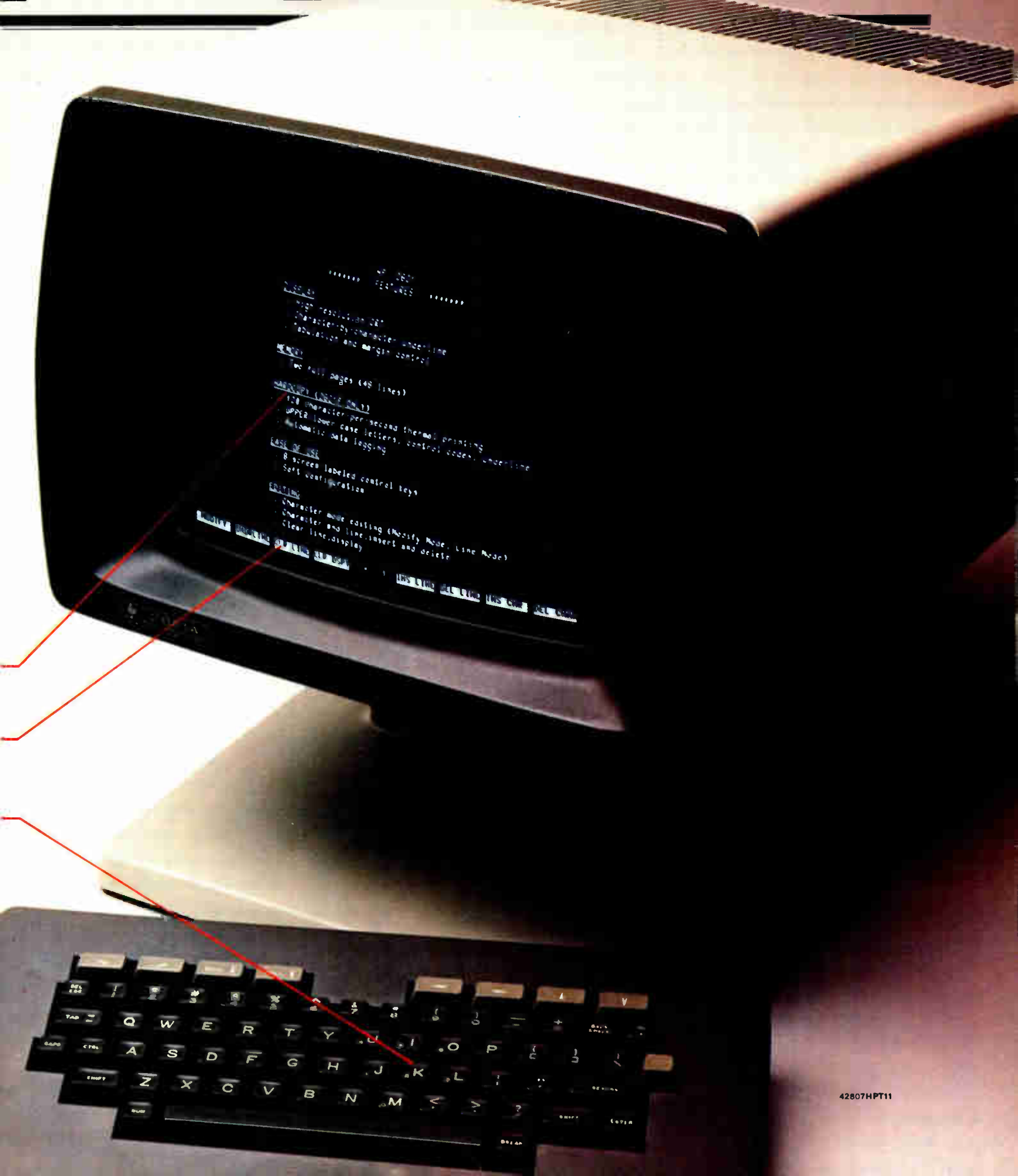

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Zilog rockets out in front again to launch a new generation.

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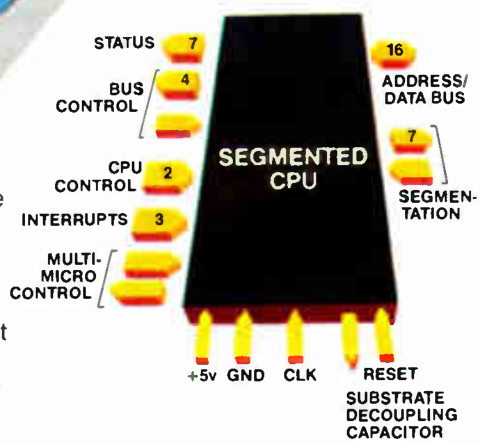
A revolution in sophistication.

The Z8000 has been designed from the ground up with options to fit your application needs exactly. For the full 8 MB addressing capability, choose the 48 Pin DIP version. Its companion device, the Memory Management Unit, opens the way to dynamic relocation, memory protection and multi-tasking applications.

Flexibility soars to new heights.

The Z8000 allows you to directly address up to 8 MB of memory. All 16 registers are a full 16 bits wide and are completely general purpose. The powerful, problem-solving instruction set supports 7 different data types from bits to 32 bit words, has 8 addressing modes and 418 usable opcode combinations.

The general register architecture helps avoid the well-known bottlenecks inherent in dedicated register designs. When this architecture is combined with the powerful instruction set, the Z8000 system throughput is an explosive 50% greater than any other 16 bit microprocessor available today.



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Cermet	100 ohms to 5 megs	±10%	Linear (U)	2.0 Watts at 70°C	1.0 Watt at 70°C	2.0 Watts at 70°C
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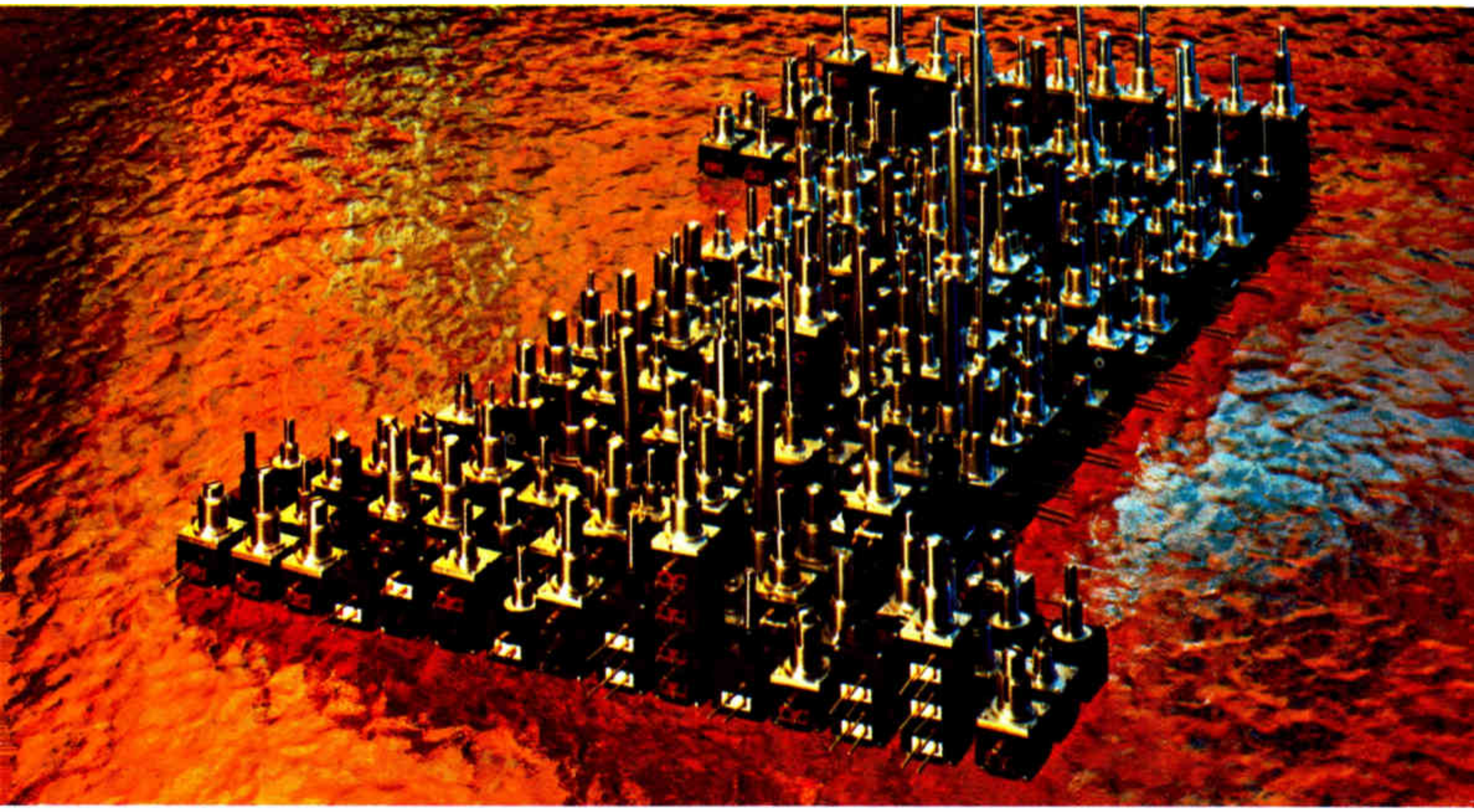

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Electronics newsletter

Zilog readying 16-K static RAM for partitioning

Watch for Zilog Inc. to try to get a jump on its memory competitors in the next few months with samples of a 16-K static random-access memory. **The byte-wide 6166, pin-compatible with the industry-standard 2716 erasable-programmable read-only memory,** is aimed at simplifying the partitioning of microprocessor system memory. The company's clocked single-5-V part features a power-down function that lets the chip operate off supplies as low as 2.5 V, cutting 50-mA active current drain to 10 mA standby. Although the part is much the same as the 4016 announced last year by Texas Instruments [*Electronics*, July 20, 1978, p. 39], its more conservative process, says the Cupertino, Calif., firm, will yield a larger but more easily manufactured die size.

Medtronics tests pacemaker run by microprocessor

Although company officials refuse to discuss it, sources close to Medtronics Inc. say the Minneapolis manufacturer of medical electronics equipment is now testing a heart pacemaker containing a custom microprocessor. In addition to generating a pulse to stimulate the heart muscle to pump blood, the device in Medtronics' unit also **transmits external signals about patient and pacemaker condition and can automatically change the unit's pulse width and rate to override a heart malfunction.** A few patients already have the pacer installed, but the large-scale and lengthy clinical investigation that is necessary before commercial introduction of the system is not yet under way.

Motorola schedules real-time clock for microprocessors

As a spin-off from its complementary-MOS watch crystal technology, Motorola Semiconductor Group is planning third-quarter introduction of a bus-oriented real-time clock part with battery backup for use in microcomputer systems. It will combine an outboard crystal with on-chip memory. With 52 of its 64 bytes of on-board random-access memory devoted to user data storage, **the new peripheral will be useful for, among other things, maintaining exact time-sampling data, even in power-down situations.** Officials at Motorola's Austin, Texas, facility plan to offer the device in two versions, the MC146818 in a 22-pin package and the MC14819 in a 28-pin package. The parts are designed to work with various n-MOS machines such as the 8080 and 3870 families, as well as with Motorola C-MOS and n-MOS microcomputer systems.

Mostek widens range with $300 development tool

Taking aim at a broader spectrum of customers for its MK3870 microcomputer development system, Mostek Corp., Carrollton, Texas, is planning a $300-range self-contained evaluation and development tool for introduction later this year. With a 3870 debug package in firmware, the new unit will fill out the low-cost end of the market, where Mostek hopes to attract low-volume 3870 users who can't afford the company's $1,295 SDB-50/70 support board and associated equipment. **At the other end of the price scale, Mostek has already taken steps aimed at more support for the 3870.** Late last month, the company began shipping an optional plug-in board that enables its $5,995 Z80 development system—the AID-80F—to support the 3870 as well. The new board, known as the AIM-72, brings the AID-80F in line with an industry trend toward development systems supporting more than one family of parts.

Electronics newsletter

ROMs getting bigger, faster at Signetics

A strong supplier of both bipolar and n-channel MOS read-only memories, Signetics is about to widen its charter with two new byte-wide ROMs that address two ends of the market. Due out first from the Sunnyvale, Calif., company is a high-speed 2,048-by-8-bit MOS device designed to complement—and help alleviate shortages in—16-K bipolar counterparts. First versions of the 24-pin part will feature 150-to-250-ns access times, but a redesign planned with Signetics' short-channel Minimos process is expected to lower that to below 100 ns. For larger microcomputer applications, the Philips subsidiary, which is recognized as the largest shipper of 64-K ROMs, will follow this fall **with a 28-pin 131,072-bit ROM—a full 16 kilobytes—having an initial access time of 450 ns.**

GE joins two others in supplying porcelainized steel

The importance of porcelainized steel as a substrate has been underlined by the entry of giant General Electric Co. into the business. GE's East Cleveland, Ohio, photo lamp department business group is supplying samples of electronic-grade (low-sodium-frit) porcelainized steel. L. Carl Krotine, OEM specialist at GE, says, **"Products are six months to a year away."** The only other manufacturers of the material are Erie Ceramic Arts in Erie, Pa., and Alpha Advanced Technology of Newark, N. J.

Parts pair works with IEEE-488 bus

While everyone else working on transceiver chips for the IEEE-488 general-purpose interface bus is handling the 16-line bus with four four-part devices, Motorola in Phoenix has already begun providing samples of an octal bipolar version. **Not only does the MC3447 get the job done with two chips, but it features a fast channel and some of the logic usually needed in external circuits to control the direction of data.** What's more, the chip, in a 24-pin, 600-mil dual in-line package, dissipates less power than anything else on the market—95 mW with all drivers on.

Addenda

GenRad Inc. has gone west to find a manufacturer of universal microcomputer development systems. As of Feb. 28, Futuredata Computer Corp., Los Angeles, will be merged with the Concord, Mass., test equipment manufacturer. **The price: 240,000 shares of GenRad common stock.** . . . A 34-megabyte quarter-inch tape drive being readied by Data Electronics Inc. of Pasadena, Calif., gets its density of 7,200 bits per in. through a seven-track design. **This capacity is double that of the largest reel-to-reel digital tape cartridge drive now available,** the firm says. The recording pattern is serpentine, with adjacent tracks recorded in opposite directions, eliminating rewind time. Called the Microtape, it is priced at $1,500, with deliveries starting in the third quarter. . . . **Intel Corp. is dropping the prices on its high-performance 8086 16-bit microprocessors 21% and 23%.** The move is viewed as an offensive thrust by Mostek, which will have samples of its second-source version later this year, and as defensive by arch-competitor Zilog, which is about to ship samples of its Z8000 16-bitter. Calling the cut orderly, Dick Konrad, Mostek's national sales manager, says that it should stimulate sales so "we'll have a bigger pie to go after." . . . Motorola and AMP Inc. will introduce **a jointly developed fiber-optic connector system at Nepcon West** in Anaheim, Calif., later this month. . . . The Electronic Industries Association of Japan purchased two-page ads in the New York Times and Washington Post **to outline its side of the TV-dumping controversy.**

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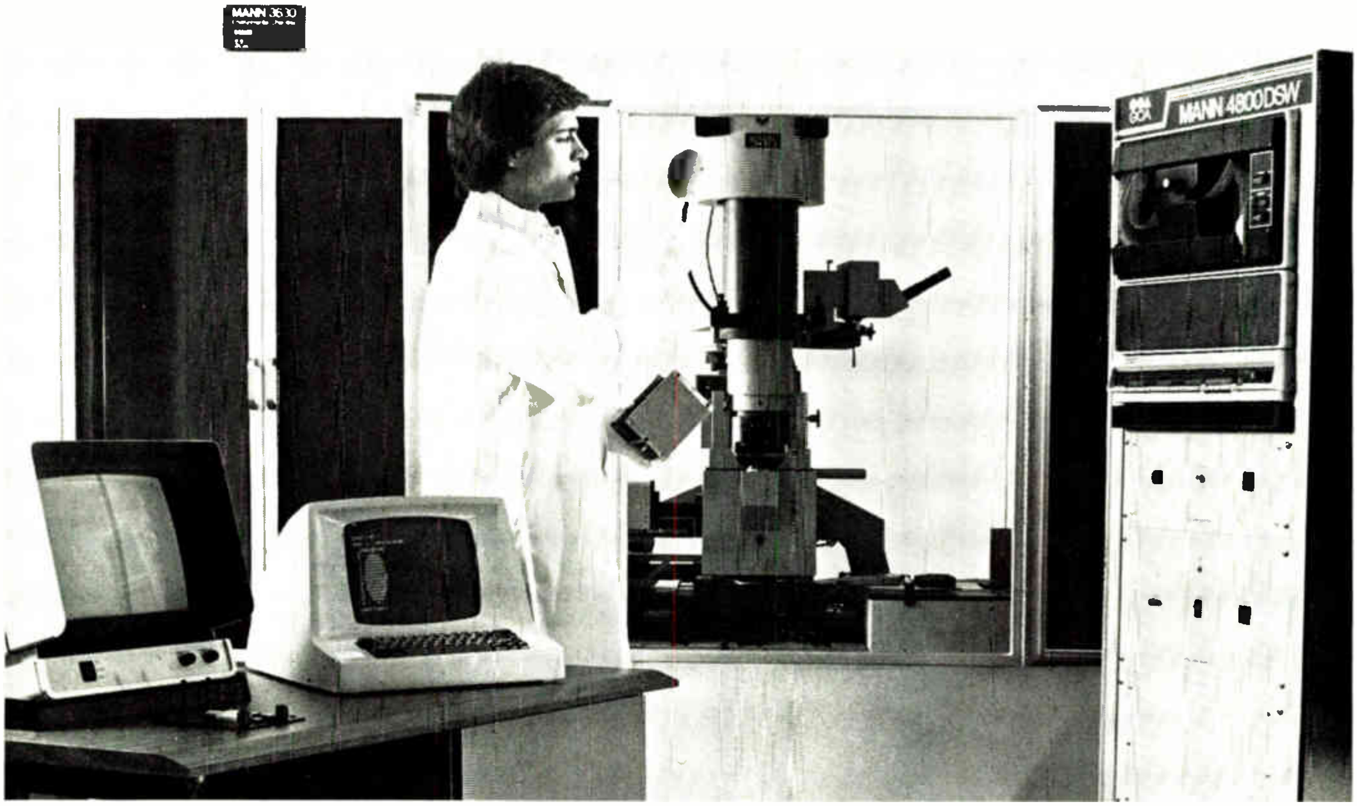

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Programming eased by replacement for ultraviolet E-PROM

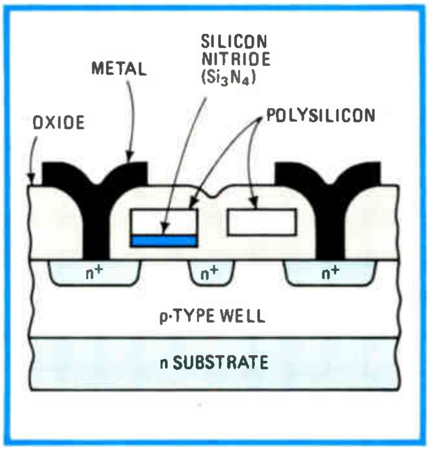
Hitachi researchers ready plug-in for industry standard 2716 that erases electrically; units due during fourth quarter

The 2716 programmable read-only memory is a hot part. The 16-K device is in such demand that major semiconductor manufacturers, like Intel, Texas Instruments, National, and Japan's Nippon Electric, sell all of the ultraviolet-erasable integrated circuits they can make.

However, workers at Hitachi's Musashi Works and Central Research Labs, both in Tokyo, have come up with a 16-K electrically erasable ROM that is not only plug-compatible with the industry-standard 2716 but, if the Japanese figures are correct, outperforms it in every respect as well. And the Japanese part overcomes the big bugaboo of EE-PROMs: speed. Previous EE-PROMs, too slow for most microprocessors, have trouble keeping up with the top performers.

Easy erasure. Although UV devices continue to improve in terms of speed and storage capacity, EE-PROMs offer advantages that cannot be matched. Their big plus, of course, is that they can be erased with an electrical signal instead of the UV light and reprogrammed without being removed from a board. Moreover, E-PROMs require a ceramic package with a quartz window to let the light in. EE-PROMS do not need it, so they lean towards lower production costs.

Hitachi's device, which it says it will deliver in sample quantities during the fourth quarter, is described in a paper at this week's International Solid State Circuits Conference in Philadelphia. It is organized like the 2716, as 2-K by 8 bits, and uses n-channel silicon-gate metal-nitride-oxide-semiconductor (MNOS) technologies. Its maximum access time is only 250 ns, little more than half that of the 2716's 450 ns. Its maximum power dissipation is 330 milliwatts, and it can be programmed in 2 seconds and erased in a tenth of a second. In contrast, the 2716 consumes more than 0.5 watt and takes 100 seconds to program, and requires a half hour to erase.



So long, UV. Cross section depicts an MNOS storage cell and series addressing transistor in Hitachi's 16-K EE-PROM replacement for the 2716. Data is stored as charge at the nitride-oxide interface.

Hitachi's part is also smaller. Even though the 2716 puts two transistors on top of each other to save space, Hitachi uses less area by having an addressing transistor in series with the MNOS storage device, as the cross section shows. Hitachi's part measures 23,300 mil² vs 30,600 for the 2716.

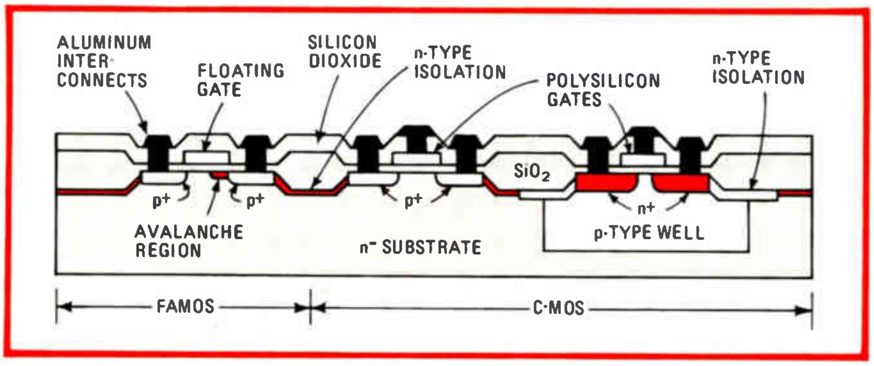
Although there are other nitride-type EE-PROMs in production—General Instrument Corp., Hicksville, N. Y., for example has parts as large as 8-K—the devices are cast as "read mostly." These are devices using nonstandard voltages whose data may be read constantly but are written over perhaps daily. Such parts find a home in cash registers and programmable television tuners. They do not address the market for microprocessor program storage. All semiconductor manufacturers with E-PROM capability, however, are aware of the obvious advantages of electrical erasability. Intel Corp., according to industry sources, is planning to announce a device before the year's end that will be based on the Famos cell it pioneered in 1970.

EE-PROMs are a bear to build consistently. Not only is oxide growth critical, but erasure is done by carefully controlling the discharge rate from the cells. Ultraviolet light does this very well, but the mechanisms of doing it electrically are not yet as well understood. ☐

Memories

8-K E-PROM gets a rival, too

While the 2716 faces stiff competition from a PROM that is erasable electrically, another Japanese company, Mitsubishi Electric Corp. in Hyogo, has found a better way to make the 2716's younger brother, the 8-K 2708. It has put complemen-



FA-CMOS. Mitsubishi combines C-MOS peripheral logic with Famos storage cell to achieve a low-power, programmable memory. It also succeeded in creating a complex structure, but one that requires only 11 mask steps, the same as standard C-MOS.

tary-metal-oxide semiconductors to work in the chip's periphery. This yields a device—another ultraviolet-light-erasable programmable read-only memory—that, the Japanese say, consumes one tenth the power of the 2708 and has negligible standby current. What's more, the part can be read with only +5 volts instead of the +5-V and +12-V power supplies required by the 2708.

Like the 2708 (and 2716), Mitsubishi's M58460S uses floating-gate avalanche MOS (Famos) technology to achieve nonvolatile storage. With Famos, developed by Intel Corp. in 1970, data is stored by charging a floating-gate insulator located above a channel region. The charge alters the memory cell threshold, and the presence or absence of conduction is the basis for readout.

Common problem. In fabricating its new memory, Mitsubishi had to overcome a problem common with PROMs: the unintentional application of programming voltages to sensitive peripheral devices. It therefore used arsenic instead of the more common boron to dope the Famos channel region, thus lowering the programming voltage to less than 20 V. Then it raised the threshold of the peripheral C-MOS transistors above this value by fabricating them with a double-diffusion process.

The figure above shows a cross section of the FA-CMOS structure. Mitsubishi says the device has a maximum power drain of 10 milliwatts, in contrast with the 800 mW of the 2708. Standby power is at most a mere 200 microwatts. Maximum access time for the two devices is the same, 450 ns.

Design rules for the memory cells are 8 micrometers and for the peripheral circuits, 6 μm. Mitsubishi engineers say that smaller design rules on future chips will allow them to build 16-K devices of a reasonable size. So far, Mitsubishi is applying the 8-K 2708 in a new telephone receiver it has designed [*Electronics*, Jan. 4, p. 67]. Other products using the device will follow, but the company has not yet decided to sell it as a component. □

Zilog previews its pseudostatic RAM

Born out of a need by microprocessor systems designers for low-cost, easy-to-use read/write memories, pseudostatic, or self-refreshing, dynamic devices are struggling for acceptance. Now Zilog Inc., in a late paper at the International Solid State Circuits Conference this week, has described its pseudostatic candidate: a 32-K chip, samples of which should be ready by summer, that offers a promising approach to making a dynamic memory as easy to use as a static.

The driving force behind the pseudostatic approach is economic: dynamic memory cells are smaller than static cells, so chip makers can get more cells per wafer, driving costs down. Static RAMs, on the other hand, are easier to hook up: no external refreshing logic is needed. In a pseudostatic RAM, refreshing circuits are included on the die itself. The result is a part with the small cell of a dynamic RAM and no external refreshing.

Zilog's 6132, organized as 4,096 by 8 bits, surrounds an array of one-transistor dynamic storage cells with an elaborate self-refreshing circuit scheme that makes sure every cell has its contents rewritten at least every 2 milliseconds. A strong point of the design, which uses a single 5-volt supply, is that the memory can refresh itself even while its data is being accessed. Thus the 6132 will not impede a system's throughput by requiring cycles of the central processing unit for refreshing.

Multiple refreshing. Zilog designed the chip to decide itself when refreshing is needed. To begin with, Zilog splits the chip into two independent 2-K-by-8-bit arrays, each with its own row-address buffers and decoders. The on-chip refresh circuits refresh one array while the other is being accessed. The split, says Zilog, takes advantage of the sequential nature of most memory-addressing schemes.

Self-refreshing also occurs when the device is idle: both arrays are automatically refreshed simultaneously. In a third mode, an on-chip counter determines if too many memory cycles have occurred since the last refreshing period. If so, the device signals the central processing unit to extend a cycle for a few nanoseconds so that it can refresh itself.

Zilog's approach, which yields a 200-nanosecond access time and 350-ns cycle time, differs subtly from the pseudostatic design used by Mostek Corp. [*Electronics*, Oct. 26, 1978, p. 128]. That, too, provides several levels of self-refreshing.

Both, however, mark a trend toward intelligent memories that support the low cost per bit of dynamic cells with on-chip peripheral circuits to simplify use and minimize power drain. Still, advances in fully static designs, coupled with industry ambivalence towards the various self-refresh schemes, leaves the fate of pseudostatic memories unsettled. □

Industrial

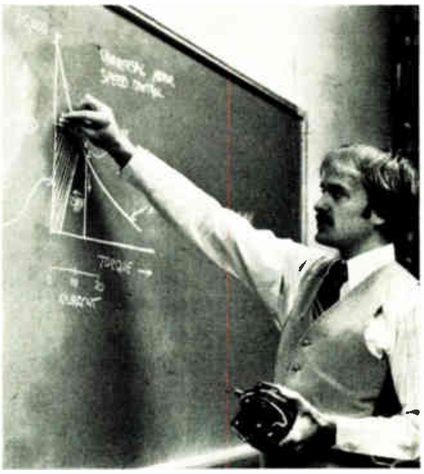
GI envisions smart motors

What do power tools, food processors, floppy-disk drives and radio-controlled cars have in common? The answer is motors, and engineers at General Instrument Corp.'s Microelectronics group in Hicksville, N. Y., see those products as perfect candidates for the benefits of microcomputer control. More specifically what the GI people have in mind is the PIC family of 8-bit microcomputers that GI has sold in great quantities for entertainment products like video games.

The number of motors used in this country is staggering. "Fifty million new universal motors are manufactured each year," says Tom Slade, GI's microprocessor applications engineering manager. He adds that universal motors, like those used in household appliances and tools, are not the only kind of motor that can profit from control by microcomputer. "The concept can be applied to any motor, regardless of size or speed. Right now, we're also working with permanent-magnet and ac motors."

Why do it? There are many reasons for using digital techniques to control a motor. One is cost: a $2 single-chip microcomputer can replace the $10 worth of analog feedback-loop circuitry needed for speed control. The configuration that GI proposes to use is the same—a closed-loop, negative-feedback scheme but with the microcomputer as controller, plus signal-conditioning electronics.

The microcomputer does more than simply adjust speed after comparing the motor's actual and desired values. It also checks motor current against a set of maximum-current values stored in a read-only-memory look-up table on the chip. Using a program nested in the same ROM, the microcomputer limits instantaneous and continuous surge and peak currents and allows a manufacturer to cut costs by using a smaller, and cheaper, motor.



Motor maven. General Instrument's Tom Slade converts theory into practice as he discusses programming a microcomputer with a motor's torque-speed characteristics.

But smaller motors may not always be what you want, Slade explains. "Take the vacuum cleaner. Here, what you'd like to use is a larger, more powerful motor, but large motors are subject to surge currents that may be too high for UL approval. The current-limiting program controls the surges nicely."

Higher efficiency is another fringe benefit, either of analog or digital control. Without a speed controller, a universal motor will speed along drawing maximum current regardless of load. Put a microcomputer in charge, however, and the speed will drop to match the load and current can be cut in half.

Ins and outs. Getting speed and control data into and out of the microprocessor is relatively easy. One speed-measurement technique compatible with microprocessors uses a Hall-effect switch and a 10-pole magnetic disk to sense the changes in the motor's rotating magnetic field and convert them into digital equivalents of speed. After computing the "error" in speed, the microprocessor converts it into a phase angle at which to drive a triac of the type generally used to speed up or slow down a motor. Speed and torque values are turned into the triac's firing angle through another look-up table in the on-board ROM.

Besides GI, National Semiconductor, Texas Instruments, and Rockwell International are pursuing motor-control programs of their own, using 4-bit parts. Slade defends General Instrument's use of an 8-bit part against charges of overkill in motor-control applications. "I'm not convinced that 4-bit machines have the processing power needed for closed-loop speed control. Our PIC-1655 microcomputer may cost 25 to 50 cents more in quantity, but that's a small price to pay for the current-limiting capabilities many of our customers seem to want."

At present, GI is working with several types of appliance and tool manufacturers, but he declines to reveal who they are. One of the first to introduce a microcomputer control—an open-loop design using a TMS1000 from TI—was Hamilton-Beach, Waterbury, Conn. However, it stressed features for the user rather than advantages to the manufacturer in its introduction [*Electronics*, Aug. 17, 1978, p. 43]. Other products are expected this year. □

Programming

C language befriends microprocessors

C is more than just the third letter of the alphabet—it is also the full name of a programing language that may one day liberate the microprocessor from its current dependence on tedious and error-prone assembly coding. C combines high-level statements with low-level machine control to deliver software that is both easy to use and highly efficient. Even Pascal, now so popular, may one day find itself in C's shadow.

A beginning. "I think Pascal is just a stepping-stone to C," says Bill Plauger. He was a member of Bell Labs' technical staff when the language was written in late 1971 by Dennis Ritchie, who is still there and remains a friend. "I've programmed 25 different computers, not for fun, but for a living, and C is the best way I've found to do business," says

C packs in a lot

The C language contains a number of features that make its code compact yet powerful. For example, C has an operation designated + + that in effect packs two program steps into one. If placed before a variable, it means increment the variable, then use it (in a computation, perhaps). When placed after, the variable is used first, then incremented.

This kind of powerful shorthand, which pervades the language, certainly helps to limit keystrokes. Peter Honeyman, a Princeton University doctoral candidate who sees a lot of C, also points out that C is succinct because assignment statements can be brought into expressions.

For example, to echo a character from a terminal's keyboard onto its screen might in another language require several statements. But in C, a single expression—while—suffices:

```
while ((c = getchar ()) != control)
    putchar (c);
```

The program fetches a character via the function: getchar. The character is set equal the variable c, then tested to see if it is a control code (!= means not equal to).

If the character is printable, putchar prints it on the screen and the process is ready to be repeated.

Plauger, "It lets you say what you want to do and there is no getting around that."

C grew out of a research project at Bell Laboratories aimed at developing an efficient system-programming language. System languages are a rare and special breed. Unlike so-called application languages like Fortran and Cobol, system languages must be intimate enough with the hardware to write the most demanding of programs: compilers, operating systems, and text editors.

Plauger left Bell in 1975 and has been busy spreading the word about C. After a three-year-plus stint at a New York City C house called Yourdon Inc., Plauger started his own company six months ago, calling it Whitesmiths Ltd., also in Manhattan. One of his first contracts, a C compiler for Zilog's Z80, came from a large process control company. He is now finished with a PDP-11 cross compiler which means the Digital Equipment Corp. machine accepts C and spits out Z80 assembly language. His next step is to compile the compiler, so he can make it resident in the microprocessor and able to accept C programs with no more help from the minicomputer. Plauger says it will be a few more months.

"The trouble with C is that it is a much bigger language than it looks," he says, "Everyone gets stuck on the code generator." The code generator is the back end of a compiler, the part that has to figure out how to make code for a computer.

Compilers coming. There are a number of compilers being geared toward microprocessors, and within the next year they will flourish. Like Plauger's, some will be for the Z80. Others will suit the 8080 and 6800, and still others are sure to be built for the coming 16 bitters. One company, however, Tiny-C Associates, Holmdel, N. J., has opted to design a C interpreter.

The Tiny-C interpreter, aimed at the part-time rather than the professional programmer, is a subset of Bell's (and Whitesmiths'). It runs on the PDP-11 as well as on the 8080 and Z80 microprocessors and is intended primarily for the education and hobbyist markets. Tiny-C is available on cassette or diskette for $20 to $60 to suit various personal computers. Unlike a compiler, which translates programs in big chunks, an interpreter translates on a statement-by-statement basis.

Tom Gibson, a Tiny-C partner, sees a tradeoff between Pascal and C. "Pascal is wordy, and current thinking is that languages should appear to be small and streamlined, and C is that." Gibson does give some credit to Pascal, however. "It helps the user avoid some programming errors that C does not," he says. "The better-equipped software houses in the future will probably stock both." □

Packaging & production

Mostek piggybacks its E-PROMs

As semiconductor manufacturers get better at fabricating erasable programmable read-only memories, an increasing number of single-chip microcomputers are beginning to appear with on-board E-PROM in place of ROM. Texas Instruments, Motorola, and Fairchild are among those either already offering them or about to do so for use in emulation and prototyping. And Intel Corp., which pioneered on-chip microcomputer E-PROM with its 8748 more than a year ago, is planning E-PROM versions of a number of other single-chip machines as well.

But amid this recent rush, Mostek Corp. is taking a much different approach. Instead of putting the E-PROM on the microcomputer die itself, the Carrollton, Texas, company has a new package that "piggybacks" a standard E-PROM part like the 16-K 2716 with a Mostek MK3870 microcomputer. Specifically, Mostek plans to mount a 3870 die in a 40-pin dual in-line "motherboard."

Plug at the top. Only slightly larger than a standard 40-pin DIP, this package will have a 24-pin DIP socket on top into which the E-PROM can be plugged. By replacing the ROM on the 3870 die with address and data buffers for the external device, the 3870 can access the external E-PROM as though it were resident on the chip itself.

Mostek plans to sell the entire assembled module, to be called the MK3874 P-PROM, for use in 3870 prototyping and for low-volume applications that don't justify the cost of masked ROM 3870 parts. The part will take no more board space than a 3870 ROM-resident device, thus

SCIENCE/SCOPE

The planet Jupiter will be scrutinized as never before by a spacecraft to be launched from the Space Shuttle in January 1982. NASA's Project Galileo will consist of an orbiter and a Hughes-built probe that will journey together for 42 months to the massive planet. Scientists hope the mission will provide new insight into the origin and evolution of the solar system, as well as reveal why Jupiter mysteriously emits more energy than it receives from the sun.

The probe, after separating from the orbiter, will plunge deeply into the hostile Jovian atmosphere. Its six instruments will take temperature and pressure readings, analyze cloud and atmospheric composition, detect for lightning, and glean other data. The probe will be designed to withstand the force of Jupiter's intense atmospheric pressure for about one hour. The orbiter will relay probe data to earth and will continue its mission and circle Jupiter for 20 months, taking pictures and analyzing the atmospheres of the red-eyed planet and its four largest moons.

Using signals transmitted in sequential bursts lasting 1/30,000th of a second, a Hughes multiplexing system designed for jet aircraft is able to control more than a dozen channels for passenger entertainment and service over a single coaxial cable. Because the signals are too rapid to be discerned separately by the human ear, the channels for high-fidelity stereo music, movie sound tracks, and passenger address announcements all seem to operate simultaneously. Other channels regulated by the system include reading lights and flight attendant call buttons.

By eliminating the need for separate wires to each channel, the system is able to save several hundred pounds of weight. It also offers better reliability, lower operating costs, and improved passenger services. Hughes systems have been installed on every McDonnell Douglas DC-10 in the world today, and now six international carriers have specified the equipment for their Boeing 747s.

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A contract to develop and build 100 satellite earth terminals has been awarded to Hughes by Satellite Business Systems. SBS, a partnership formed by Aetna Life & Casualty, Comsat General, and IBM, will receive the communications industry's first four-year warranty. The terminals will operate with the system's three satellites, also being built by Hughes to service U.S. businesses, government agencies, and public service organizations.

The unmanned terminals will be the first to use Ku-band frequencies (12 to 14 GHz) on a large scale in a U.S. domestic satellite. This makes possible small terminals located on customer premises, thus eliminating the need for a microwave link. With these highly-reliable redundant terminals, SBS data communications customers will benefit from a very high availability rate. The first engineering model is scheduled for delivery in nine months. All 100 terminals should be delivered by mid-1982.

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making for easy field prototyping, Mostek says. In contrast to E-PROM-resident microcomputers, the 3874's E-PROM can be removed, reprogrammed, and reinserted many times.

Including a Mostek-built 2716 E-PROM, the 3874 module is expected to sell initially in April in the $115-to-$120 range in small quantities, with 100-to-1,000-unit pricing around $73. The device may also be available without an E-PROM for around $75 in single units.

As additional 3870 family members become available, the 3874 type of package will be offered with the new dies as well, says Ron Baldridge, Mostek's strategic marketing manager for microcomputer products. The packages will accommodate other standard E-PROM parts besides the 2716, as well as various bipolar ROMs.

Some competitors snickeringly suggest that Mostek chose the 3874 piggyback packaging approach because it did not know how to integrate E-PROM on board a 3870 chip. Baldridge concedes that the difficulty of such a task was a consideration, since E-PROM processing is one of the trickiest technologies in the metal-oxide-semiconductor business today. But he contends that Mostek could have handled the on-chip E-PROM approach, had it chosen to do so. Rather, it prefers the piggyback's advantages.

Standard gear. For one thing, users of E-PROM-resident microcomputers have to buy specialized programming equipment, Baldridge says, whereas standard PROM programmers are good enough for E-PROM used with the 3874. And, he continues, users of the 3874 will have more E-PROMs to choose from than they would with a single-chip E-PROM-resident machine. The 3874 in its various configurations will also be able to support the 32-K 2732 and 2532 devices. To integrate that much E-PROM on a microcomputer chip would require circuits so large as to be unproducible today, Mostek says. For smaller program requirements, the 3874 will also handle 8-K 2758 and 82S2708 E-PROM devices.

From Mostek's own viewpoint, it

News briefs

TI reports sales of $2.5 billion

With its eyes on a $10 billion sales goal by the late 1980s, Texas Instruments Inc. reports a 25% sales gain for 1978, boosting its revenues to $2.546 billion. Earnings for the year were up 20% to $140.3 million, compared with 1977 profits of $116.6 million on sales of $2.046 billion, the Dallas-based company says. Other key figures just released in TI's 1978 annual report include: a record $1.4 billion year-end order backlog, some $486 million more than 1977's; capital and research and development expenditures of $311 million and $110 million respectively, up from $200 million and $96.2 million in 1977; and employment of 78,571 vs 68,521 a year earlier.

Makers slash predictions of microwave oven sales

Microwave oven manufacturers are scaling back their industry sales projections, as much because of overoptimistic predictions as because of economic uncertainty. Though Litton Industries' Microwave Cooking Products operation in Minneapolis last year predicted 1979 sales of 3.4 million units, its latest projection for the industry is 2.75 million units. Industry consensus for 1980 sales is only a 9% increase, to 3 million units.

Hughes, Raytheon named Amraam missile finalists

Development of the Air Force Advanced Medium-Range Air-to-Air Missile, Amraam, is in the hands of Hughes Aircraft Co. and Raytheon Co., under two contracts totaling $84.5 million. Losers in the competition for the 33-month prototype awards were Ford Aerospace & Communications, General Dynamics, and Northrop. Amraam will improve on its Sparrow predecessor's performance by permitting pilots to fire several missiles at separate targets simultaneously at longer range. Production awards could exceed $1 billion over 20 years for up to 10,000 missiles.

Forecast sees Army buys of satcom terminals doubling

Inflation, rather than real growth, will fuel the projected 30% increase over seven years in the military market for communications satellite systems, says Frost and Sullivan Inc. The New York-based market analysts put 1983 spending at $573 million. In that year the military will more than double its outlays for terminals from just under $118 million in 1977, the firm predicts. The leading terminal buyer will be the Army, spending a seven-year total of $883 million, the Navy $303.5 million, and the Air Force $245 million.

Computer Automation cuts mini prices—again

For the second time in three months, Computer Automation Inc., Irvine, Calif., is slashing the price of its low-end minicomputer on a board, the LSI 4/10, and of other models in its board-level Naked Mini line. With a 32-kilobyte memory, the 4/10 sells for $995, against the $1,235 price in effect since November, itself a 42% cut. The LSI 4/30 mid-sized mini and the larger LSI 4/90 will be 9% to 48% cheaper, depending on memory.

Worldwide fiber optics market to push $2 billion by 1990

Paced by growing telecommunications applications, worldwide demand for fiber-optic cable systems should reach $1.5 billion to $2 billion by 1990, says Gnostic Concepts Inc. The Menlo Park, Calif., research company's new survey pegs the North American market at $27 million for 1978, $390 million for 1985, and $974 million by 1990. It estimates the Japanese market at $2.1 million, $91 million, and $333 million, respectively. Outlays in Europe will be somewhere in between.

Ireland extends tax advantage

With the tax forgiveness feature of its aggressive program for attracting industry due to run out in 1980, the Republic of Ireland has come up with a successor: a tax of only 10% on export profits through 2000. However, allowances for plant expansion could, in effect, still mean a zero tax.

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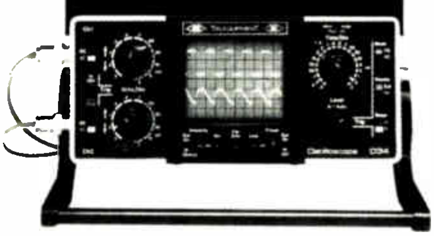

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will easily be able to provide E-PROM for its entire 3870 family with a single 3874 device. It will not have to redesign each chip specially to integrate E-PROM on board, Baldridge notes.

He also points out that the 3874 will be superior as an emulation tool to multichip emulator boards currently used for 3870 prototyping. This is because the 3874 will come much closer to being electrically identical to the part that is being emulated. □

Solid state

IBM logic adopts new gate arrays

Besides providing the basic building block for the latest computers from International Business Machines Corp. (see related story, p. 85), the new logic-gate arrays contained in the 4300 processor give an insight into the directions the computer industry giant is taking in implementing large-scale and very large-scale integrated circuits.

The new semiconductors are replacing the firm's so-called monolithic systems technology used in the nine-year-old System/370 line—a current-switched emitter-follower logic design that had gate delays ranging from 6 to 12 nanoseconds and, typically, contained six circuits on a chip.

IBM's future systems will apparently use LSI gate arrays customized by modifying their last layers of metalization. Computer-aided design systems for customizing chips are already installed at some 25 IBM design facilities worldwide.

Bipolar logic. The newest gate array uses current-switched bipolar logic. Each contains 1,496 gates, 88 receivers, and 64 high-powered driver circuits on a chip 224 mils square. In the 4300 processor, this bipolar array is used as a microprocessor for the 3880 disk-controller unit and is said to execute more than 5 million instructions per second.

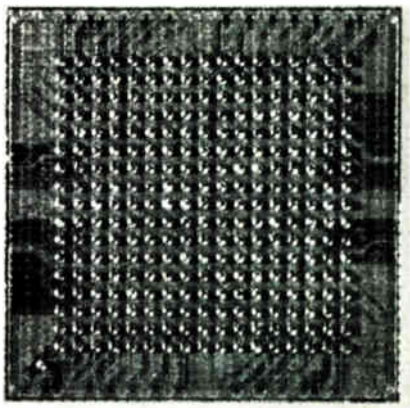
Powered by +5.0- and +1.7-volt supplies, the chip has typical gate delays of 1.5 ns and nominally dissipates 1.8 watts, according to designers Richard J. Blumberg and Stewart Brenner, who are describing the array at this week's International Solid State Circuits Conference in Philadelphia.

The receiver and driver circuits convert the levels associated with the Schottky transistor-transistor logic used in the rest of the 4300 to those needed by the current-switched logic of the new chip. An IBM spokesman describes this logic as similar to emitter-coupled logic but without the emitter-follower configuration. The higher of the two voltages is used for the receivers and drivers, and the lower is used for the logic gates, thus reducing the chip's overall power dissipation, Blumberg and Brenner say.

System/38 array. Also used in the 4300 is the same Schottky TTL gate array employed in the System/38 introduced by IBM's General Systems division [*Electronics*, Nov. 9, 1978, p. 81]. Measuring 179 mils on a side, the chip has 704 logic gates and 121 external connections, uses −1.5- and −4.25-V power supplies, and dissipates 1 W.

IBM's package is unusual. Rather than making all connections on the perimeter of the chip and using a dual in-line package, IBM relies on what it calls a "flip-chip" approach. In the final chip-fabricating step,

Dots. A 17-by-17 array of solder bumps marks the spots where connections can be made to the bipolar gate-array chip developed by IBM for a new disk controller.



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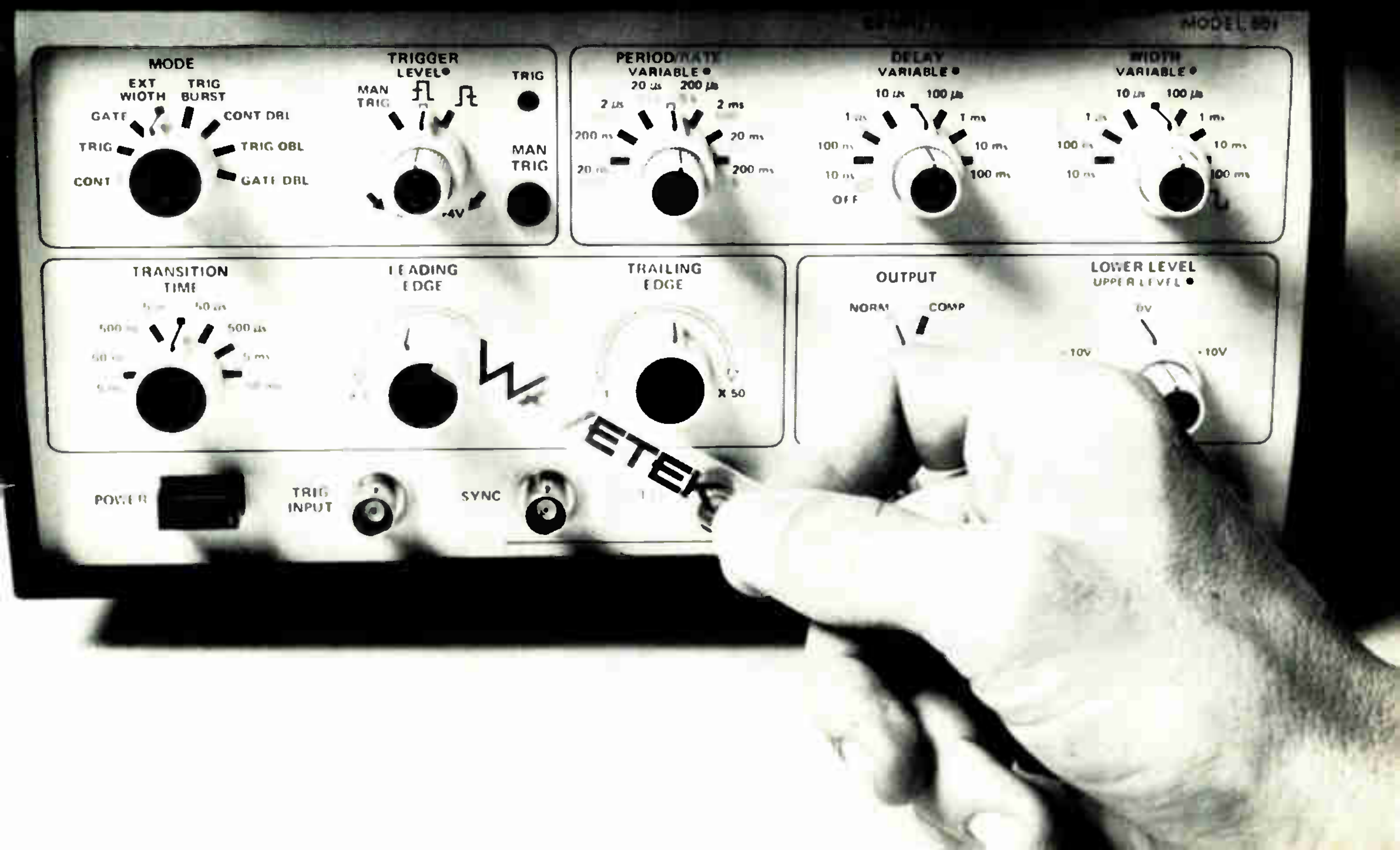

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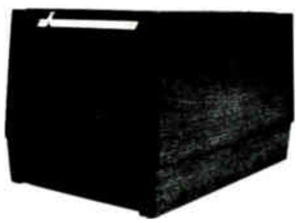

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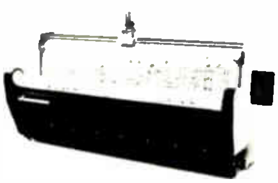

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solder dots, shown in the photograph on page 46, are placed on the chip. The chip is then inverted onto a ceramic carrier and heated so that the solder reflows, bonding the chip to the carrier and making the electrical connection.

This method allows the designer a larger mumber of external connections and permits connections to be made to the middle of the chip. The microprocessor chip for the 3880 has 249 solder dots arranged in a 17-by-17 grid, although only 94 are used. The Schottky TTL chip has an 11-by-11 grid of 121 solder dots, down from the 132 used on a similar chip in the System/38.

They are made at the Data Systems division, East Fishkill, N. Y. This division was dedicated to making large complex systems and high-performance computers when IBM split its mainframe manufacturing operations last August [*Electronics*, Aug. 17, 1978, p. 44]. This gives rise to speculation that the new chips are the harbingers of faster gate arrays designed for new high-end units. □

Distributors

Semiconductor pinch continues to hurt

While all the signs of continued high sales volume have semiconductor companies beaming and large-quantity users coping with stretched-out lead times, distributors are caught in the middle. Orders are indeed coming in from their small-quantity customers, but where's the supply?

Not only are distributors waiting at the end of the supply chain for the newer devices, such as low-power Schottky and 16-K random-access memories, but they report ever longer delays for the established, commodity products. A sampling of key distributors across the country last week indicates that there has been no shortening of lead times so far this year as had been anticipated.

Why the problem. The reasons for the supply problem—it's not exactly a panic situation at this point—are apparent high levels of real demand, double ordering, yield problems last year, and an overcommitment by some semiconductor producers to the as yet low-volume, high-technology products at the expense of the larger-volume established products. As usual, the vendors try to downplay the lead time stretch and make assurances that double ordering is not going to be a problem.

But this bravado does not sway the distributors who remember the boom-to-bust inventory disaster of 1974. For instance, Joseph Semmer, director of semiconductor business development for Hallmark Electronics Inc., a Dallas-based distributor, confirms that supplies of all digital logic parts "seem to have gone haywire in the last 30 days." He reports that in mid-January, Texas Instruments suddenly informed distributors that it would not take any more orders until Feb. 1. Shortly afterward, Motorola Semiconductor informed distributors that it would not take any orders in bipolar logic parts because it was booked up for the year.

"Recently, TI has said it will now take orders for deliveries on an allocation basis for July or August [which TI confirms]," Semmer relates. He expects TI to continue its allocation program on a month-to-month basis but says Motorola is now taking orders only on a "will advise" basis.

Memories, too. While distributors are worrying about getting bipolar logic, they are also experiencing problems with memories.. In Chicago, Advent Electronics Inc.'s president Abe Halegua reports shortages of 4-K RAMs and read-only memories, including the popular 2716 E-PROM. Another sign of tight supplies to Halegua is the number of out-of-state calls he gets.

"By this measure, supplies of semiconductors are stretched thin in California," he observes.

Distributors in the West confirm this impression. Michael H. Wolf, national product manager of Wyle-Elmar, Mountain View, Calif., reports that low-power Schottky is out

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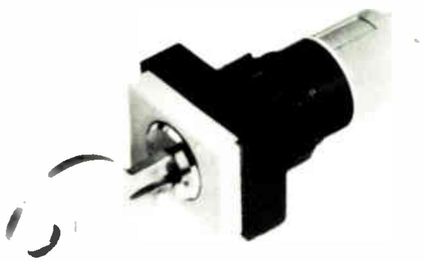

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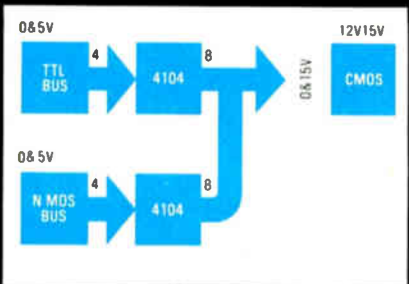

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anywhere from 20 to 50 weeks and standard Schottky is being affected, too. Bipolar PROMs are also stretched, Wolf adds.

Meanwhile on the East Coast, the story is the same with much more concern over double or even triple ordering. Seymour Schweber of Schweber Electronics, Westbury, N. Y., states, "Everybody knows that maybe 40% of their orders are going to disappear, but no one knows when." However, Donald A. Winans, vice president of marketing at Cramer in Boston, hopes that TI's allocation system will help prevent big double-order backlogs. □

IEEE

Suran to balance institute's goals

Members of the IEEE can look forward to a year that includes the promise from president Jerome J. Suran to try to strike a balance among the conflicting aims of the factions within the organization. At the same time, they can look to a fight to succeed Suran: executive vice president Leo Young is readying a petition campaign in the belief that the institute's board of directors will pass him over in designating its nominee for the 1980 presidency.

In announcing his program at a mid-January press conference in New York, Suran made it clear that he believes the Institute of Electrical and Electronics Engineers exists primarily to spread technical knowledge among its members. Yet he also voiced support for some of the socioeconomic goals promoted by the U. S. Activities Board.

The USAB is a focus of a basic dispute among members: should the IEEE concentrate on its technical activities to the exclusion of socioeconomic concerns, primarily that of employment. The debate has enlivened the annual campaign for election of officers in recent years. Young wants the IEEE to promote a stronger USAB. He fears USAB will take a back seat if the IEEE board, to meet this month, chooses as the "official" presidential candidate for 1980 either C. Lester Hogan of Fairchild or Burkhart H. Schneider of Detroit Edison—both selected by the IEEE nominating committee.

To defuse some of the controversy, Suran has promised to move towards board action on a bylaw change that would move the vice president for professional activities into an elected position [*Electronics*, Nov. 23, 1978, p. 44]. □

Commercial

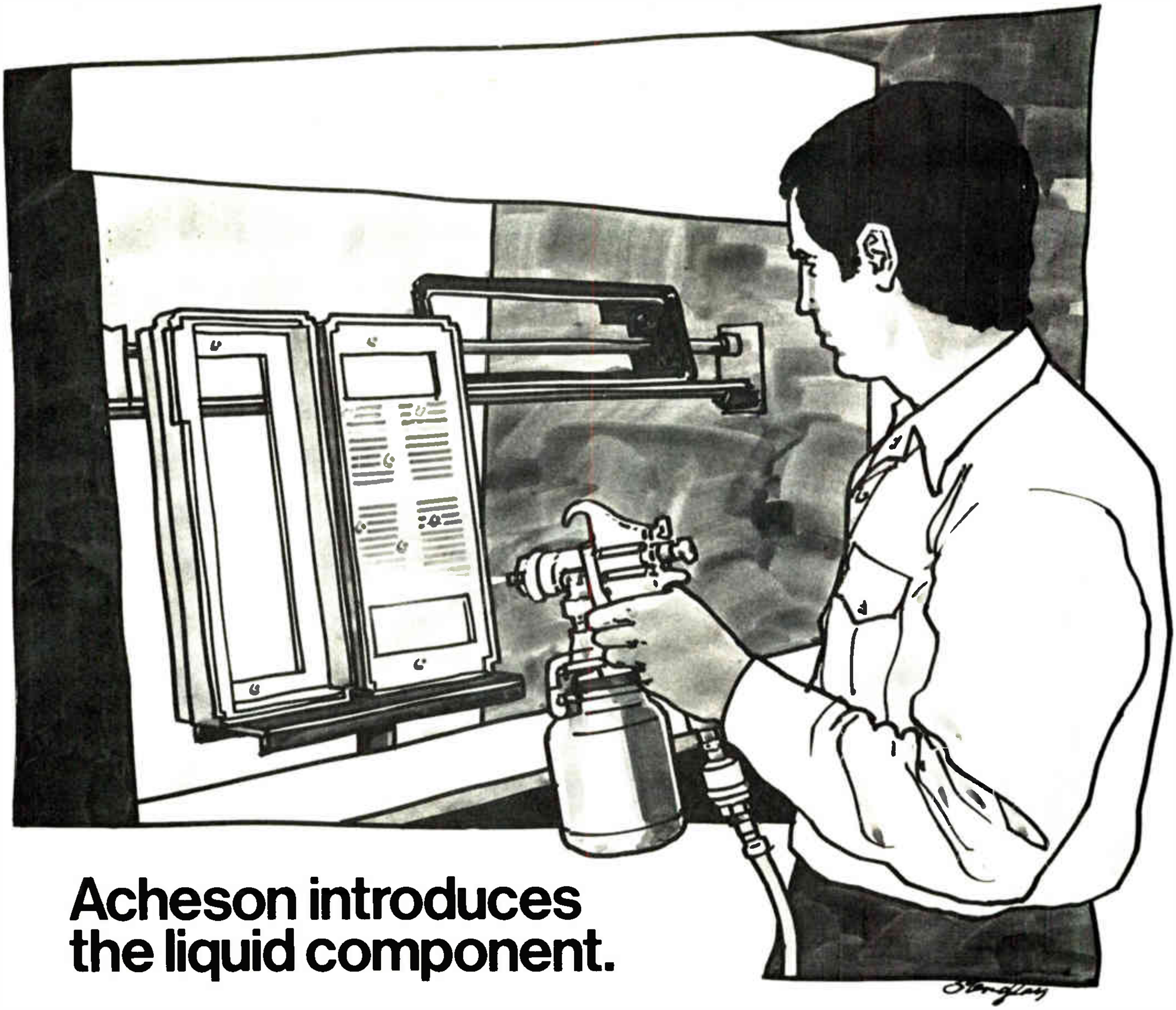
Five microprocessors raise typewriter's IQ

Microprocessors are making their way into office and business machines—but a typewriter with five of them? That's what Olivetti Corp. of America has put into its ET 221, now in production in its Harrisburg, Pa., plant.

"It's a Z80-based system using slave 8041s," says Charles Ericson, manager of product design and development in Harrisburg. The 8041 [*Electronics*, July 7, 1977, p. 109] is an 8-bit single-chip microcomputer called a universal peripheral interface by Intel. "There's one apiece to run the daisy-wheel printer, the carriage, the keyboard, and the display," Ericson says.

Capabilities. The under-$2,000 machine is a typewriter, he emphasizes, but it does boast capabilities associated with word processors. Among these are a 20-character, 5-by-12-dot vacuum fluorescent display for line-at-a-time editing, as well as storage of lines and page formats.

In the editing mode, each line goes into an 8,192-bit n-channel metal-oxide-semiconductor 2114. This static random-access memory stores two lines, as well as serving as a scratchpad for the Z80. The 2114 dumps its line data into an 8-K complementary-MOS dynamic RAM, which can store 829 characters of text—better than a page of an average business letter—as well as the line and page



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formats. It can be divided into 10 sectors, recallable independently.

Simultaneously Olivetti is introducing the ET 201, which has just a two-character, seven-segment light-emitting-diode display that indicates print position only. It cannot be used for line-by-line editing.

The new machines are top-of-the line typewriters, competing with products like the microprocessor-based $1,485 IBM 50 and 60, which do allow some data and format storage in a RAM. The ET 221/01 capabilities are roughly equivalent to those of the Qyx Level 1 from Exxon Enterprises Inc. [*Electronics*, March 2, 1978, p. 46]. However, the $1,650 Qyx is a low- or entry-level word processor, and the processing capabilities expand considerably up to the $7,750 Level 5.

Like the new Olivetti typewriters, the Qyx machines replace almost all electromechanical parts with electronics. But the Qyx word processors stick to Z80s—two in the Level 1 and three in Levels 2 through 5—which also happen to be a product of its fellow Exxon subsidiary, Zilog Inc., Cupertino, Calif.

Low-cost controllers. Still, the ET 221/01 is unusual in its lavish use of microprocessor technology. The reason is simple, says Ericson. "Extremely low-cost controllers with a medium-price microcomputer give a tremendous amount of power without appreciably changing the cost." A single processor "can drive the peripherals but will have no time to do anything else." Ericson will not disclose exact cost figures, but he does say the electronics parts are about half the cost of the electromechanical parts they replace.

The program memory is four 32,768-bit 2332 read-only memories. Also used with the 8041s that drive the printer and the carriage are simplified analog-to-digital and d-a converter chips made to Olivetti's design by the Italian semiconductor house, SGS-Ates SpA. Initial production is limited to Harrisburg, but the Italian parent company, Ing C. Olivetti & Co. SpA, also plans to make the machines in one of its European plants. ☐

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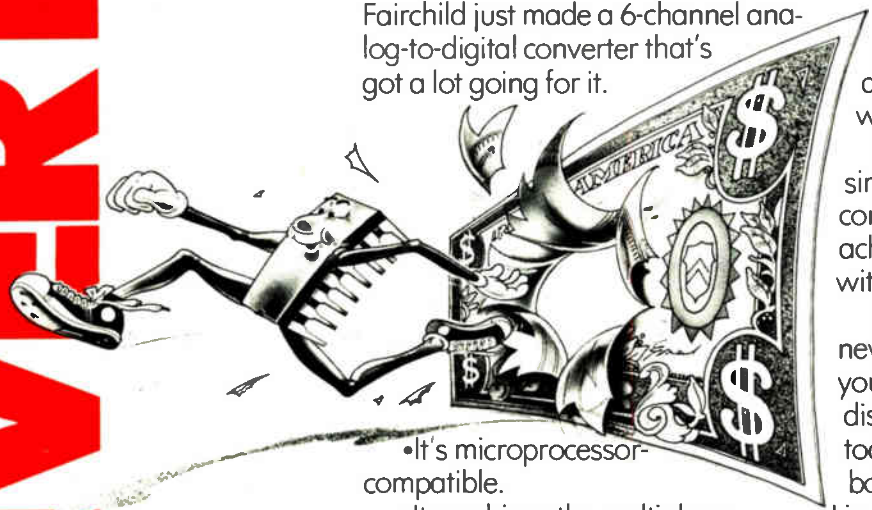

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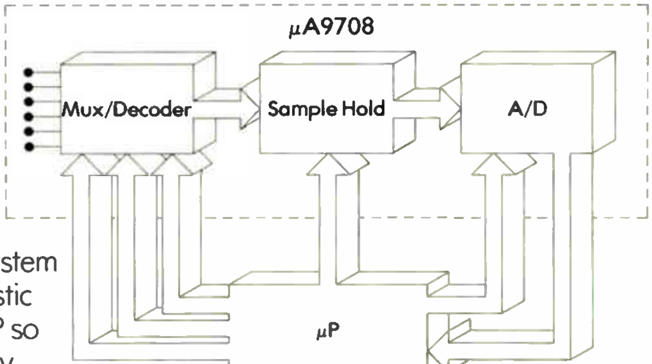

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NEC To Supply 100 RF Terminals For U.S. Digital Satellite Services

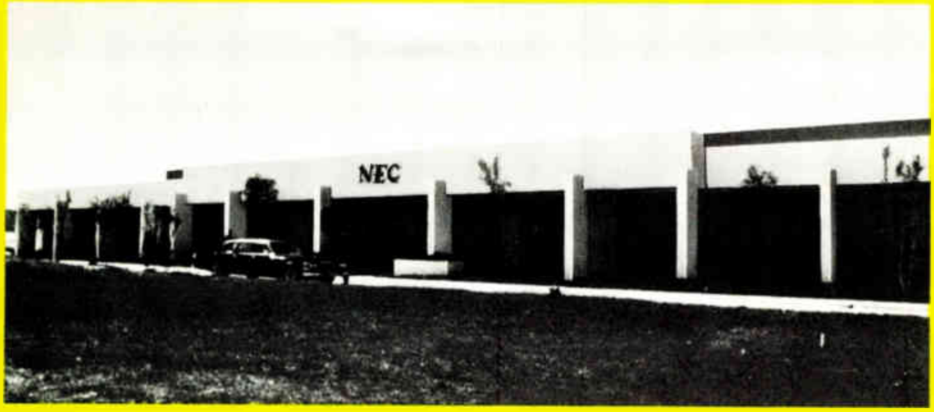
The Satellite Business Systems, Inc. (SBS) of the United States recently awarded NEC a contract for the provision of 100 RF terminals for its digital domestic satellite communications network.

The RF terminals will have a 5-meter or 7-meter diameter antenna — 14 GHz for transmission and 12 GHz for reception — and communications equipment including a high-power amplifier, low-noise amplifier and frequency converter.

These earth stations, intended for unmanned operation, will be installed at subscribing private and government organizations, as one of the SBS network facilities for such domestic satellite services as speech, data, facsimile and television/telephone conference communications.

The 100 RF terminals will be delivered between February 1980 and August 1982.

NEC America Dallas Plant In Full Swing



NEC America's Dallas plant has begun the full-scale manufacture of electronic private branch exchanges and electronic key telephones to meet increasing demands for these NEC products in the North American market.

The new plant, with floor space of about 5,600 square meters on a 48,000 square meter site, manufactures medium-capacity NEAX-12 electronic private branch exchanges and large-capacity popular Electra-100 electronic key telephones. It will start production of digital telephone switching systems for central office use next year.

USSR Orders NEC Equipment In Readiness For Olympics

NEC recently announced a total of nineteen NEC System 100 office computers and eighty-four work station terminals will be delivered to the V/O Electronorg-Technica, and put into operation by April 1980.

These computers and terminals will be installed in eight hotels now under construction in Moscow for booking, check-in and check-out operations.

The communications facilities awarded by the V/O Mashpriborintorg consist of an Intelsat standard A earth station, a line-of-sight microwave communications system and studio-to-transmitter links.

The earth station will have access to the Intelsat IV-A communications satellite above the Atlantic Ocean for the transmission of color television, telegram and telephone signals.

It will be capable of transmitting four video programs at the same time via the Intelsat satellite so that receiving countries can select any of the four Olympic programs. In past Olympic Games, only one video program could be transmitted internationally through a communications satellite.

NEC System 100 office computer

Cassegrain 13-meter diameter antenna at MARISAT shore station in Yamaguchi, Japan.

Japan's MARISAT Shore Station Is Officially Commissioned

Japan's shore station, the third in the world, was officially commissioned recently for maritime communications via MARISAT satellite above the Indian Ocean.

The shore station, completed by NEC for Kokusai Denshin Denwa Co., Ltd. (KDD), Japan's international communication carrier, is located at Yamaguchi in the westernmost part of the main island where KDD's Intelsat standard A earth station is also located.

The station features a complete duplex configuration except for its 13-meter diameter Cassegrain antenna commonly used both for C- and L-bands. The main facilities include 4 GHz 55K uncooled parametric low-noise amplifiers, 6 GHz 2.7kW air-cooled klystron high power amplifiers, C- and L-band transmitter/receivers, power supply units, and network control processors.

The new shore station is capable of providing 22 high-grade instant telegraph and two telephone lines between land subscribers and ships in the Indian Ocean and the waters off Japan, Southeast Asian countries, etc. via the MARISAT satellite above the Indian Ocean.

With the completion of the Yamaguchi shore station, the MARISAT System can now cover almost all the waters of the world.

In addition to shore station systems, NEC also manufactures a ship terminal which can handle the complete range of MARISAT services.

NEC Delivers Its Largest Multi-Processor System To Osaka University

NEC System 900 Model 2 computer.

NEC recently delivered an ultra-large multi-processor system composed of two NEC System 900 Model 2 computers, the first two of the newly-unveiled top end model of the NEC System general-purpose computers, to Osaka University, Japan.

The NEC System 900 Model 2 has the world's largest instructions processing capability of 6.5 MIPS (million instructions per second), and the multi-processor system is capable of processing 11.2 MIPS.

An ultra-large host computer of NEC's new information processing network architecture "DINA", it was designed on the basis of NEC's "C & C" — communications and computers — technology, and incorporates high-density LSIs with up to 200 gates per chip and LSI packages with up to 110 chips per package.

In addition, the system is intended for distributed multi-processing applications for the first time in the world. It is especially suited for a large-scale communications network and highly-comprehensive on-line data base system.

First Micro-optic Devices For Optical Fiber Systems

NEC recently announced development of the world's first micro-optic components for optical fiber communications systems.

The new devices are "optical multiplexer", "optical branching filter", "optical directional coupler", "star coupler", "optical isolator" and "optical switch".

Newly developed "optical directional coupler" compared with conventional device.

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Washington newsletter

Anti-inflation rules in NASA contract called illegal

Corporate confusion over President Carter's pay and price guidelines is expanding following a Government attempt to incorporate them into a space shuttle contract congressional investigators say is illegal. At issue is the National Aeronautics and Space Administration's early February award of another $2 billion to Rockwell International Corp., Downey, Calif., for three more shuttle vehicles. **The contract is the first to make the pay and price guidelines a part of the agreement.** The White House Office of Management and Budget (OMB) has issued regulations requiring compliance with anti-inflation guidelines in all Federal contracts over $5 million issued after Feb. 15, a ruling that would cover 62% of the Government's $85 billion annual procurement. Yet Congress's General Accounting Office says the guidelines were issued on a voluntary basis and have no effect in law, and it is urging Congress to act unless OMB cancels its contract requirement.

Inquiry set into electronic mail plans of post office

Competitive private development of electronic message services got a boost late last month when the Federal Communications Commission inaugurated an investigation into the legal and policy issues of the U. S. Postal Service's proposal for electronic computer-originated mail [*Electronics*, Dec. 21, 1978, p. 36]. The new inquiry under Docket No. 79-6 **should forestall Postal Service plans to begin ECOM, as it is known, next month** and thus save the National Telecommunications and Information Administration (NTIA) the embarrassment of not having a policy recommendation ready for the White House on the post office market entry before the service begins. Leaders at the NTIA and the Justice Department oppose the Postal Service plan. But the FCC action came at the urging of another opponent—Graphnet Systems Inc., a small facsimile-message transmission and delivery carrier.

FAA names Boeing to study simpler cockpit warning aids

Now that there are 150 visual and aural warning systems in the cockpit of some modern jetliners, the Federal Aviation Administration wants to simplify and standardize the technology. **Boeing Co. of Seattle is getting a $917,000 two-year contract to produce and test at least three prototype systems** that the FAA can use in developing guidelines for aircraft and avionics manufacturers. Lockheed and McDonnell Douglas will serve as subcontractors. The agency says multiple alert systems could be replaced, for example, with a single tone that would either draw the pilot's attention to a cathode-ray tube display spelling out the problem or indicate he should push a button to call up a checklist for display.

SBS wraps up earth station awards

Satellite Business Systems Inc., McLean, Va., has completed its initial contracts for components of customer ground stations with an award to Tokyo's Nippon Electric Co. for design, development, and production of 100 port adapter systems. Deliveries will begin next January after SBS tests of three prototype systems, which interconnect the voice and digital ports of the satellite communications controller. **The award, the value of which was withheld, is NEC's third** for major components of the domestic satellite system. Last month NEC won a contract for five terminals to be used in the 12-to-14-gigahertz tracking, telemetry, and command system [*Electronics*, Jan. 18, p. 57]; last year it won a contract for 100 rf terminals for earth stations on customers' premises.

Washington commentary

DOD's opportunities and NATO's threat for 1980

For the second straight year, the Department of Defense's spending plan holds out significant increases in contract dollars for the electronics industries. That money, coupled with the uncertainties developing in other segments of the economy, guarantees greater competitive interest in the Pentagon's programs for the fiscal 1980 year that begins next October.

Money for electronics in the two categories that count—procurement and research, development, test, and engineering—totals more than $15.5 billion, roughly 40% of the total. The figure represents a 13.3% gain on the current year's spending level and more than offsets inflation, now pegged at just under 7%.

Congress must still act on this good news, of course. Yet conversations with staffers on the House Appropriations and Senate Budget Committees indicate that DOD's bigger budget for electronics procurement and R&D faces few threats and none whatsoever from embittered sponsors of social programs who believe they have been shortchanged by the White House. "Sacred cows like Social Security probably won't be cut the way the White House wants," observes one analyst. "But when that extra money is budgeted, it won't be at the expense of the Pentagon; it will be at the expense of the Federal deficit" that President Carter wants to reduce to $29 billion.

New stress on technology

One reason for DOD's budgetary strength this year is Defense Secretary Harold Brown. In his annual report to Congress at the end of January, Brown spelled out policies and programs with remarkable candor, clarity, and precision. It took him nearly 350 pages to do so, and congressional opponents of increased military outlays will find it difficult to find flaws in Brown's spending plans. Rather than attempt to match the Soviet Union and its Warsaw Pact allies on a weapon-for-weapon basis, Brown insists that the U. S. and its NATO allies should strive "for balanced forces: nuclear and nonnuclear; ready as well as modern."

To achieve that modernization, Brown's science and technology segment of the budget is designed to revitalize the interest of the nation's semiconductor companies in military R&D. Dollars for basic technology of all types exceed $2.3 billion, up from the current $2 billion level and making it the second straight year in which spending will rise by 14%.

New to the 1980 R&D budget is the program to develop very high-speed integrated circuits [*Electronics*, Sept. 14, 1978, p. 81]. Brown puts VHSI at the top of his list of nine basic research priorities. With $32 million to initiate the six-year R&D effort, Brown hopes it will "achieve major advances in IC technology, including an order of magnitude reduction in size, weight, power consumption, and failure rates and a hundredfold increase in processing capacity." Circuits with these capabilities, he says, "will allow important and significant advancements in cruise missiles, satellites, avionics, radar, undersea surveillance, electronic warfare signal intelligence, and systems for command, control, and communications."

Ranked right behind VHSI is Brown's program for increased R&D on precision-guided munitions technology, which he says will "capitalize on increases in microelectronics and signal processing."

Sharing with NATO

Despite such R&D initiatives and a host of procurement programs heavy with electronics subsystems, U. S. defense contractors still have problems with Harold Brown's programs for the North Atlantic Treaty Organization. Even though strengthening the NATO alliance is a principal reason for the fiscal 1980 increases, U. S. contractors are uneasy about the prospect of sharing technology and contract dollars with their European counterparts within NATO.

In response to Europe's call for "more of a 'two-way street' in defense buying," Brown says the U. S. will increase competition throughout the alliance for new weapons. Moreover, says the defense secretary, "we are making major efforts to buy already developed European equipment for U. S. use where it meets our needs at a competitive price. Finally, we are working on a dual production program in which we will make our latest existing defense developments available for production in Europe."

While Brown believes these programs will produce "a major improvement in the efficiency of defense R&D and procurement for the NATO alliance as a whole," some electronics suppliers see such efforts as threatening more than their military market share. "A lot of companies," says one congressional budget staffer, "suspect they might lose their leverage in related industrial and commercial markets as well if they are obliged to share their technology." The prospect of constituent companies losing dollars and jobs to Europe does not sit well with many members of Congress, and DOD would like to head off industry from raising the issue. **Ray Connolly**

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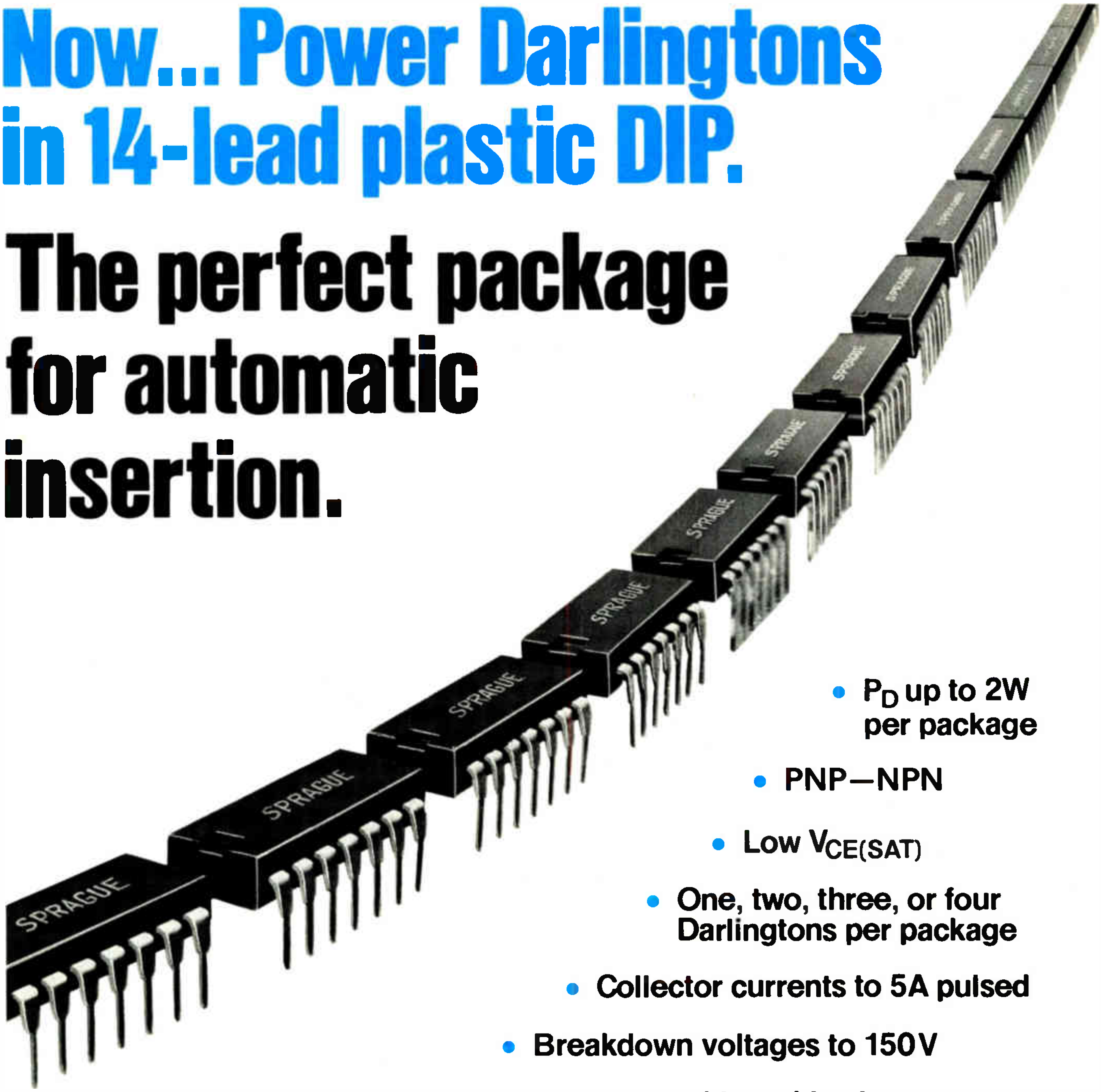

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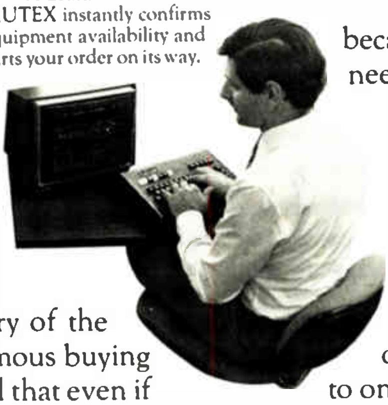

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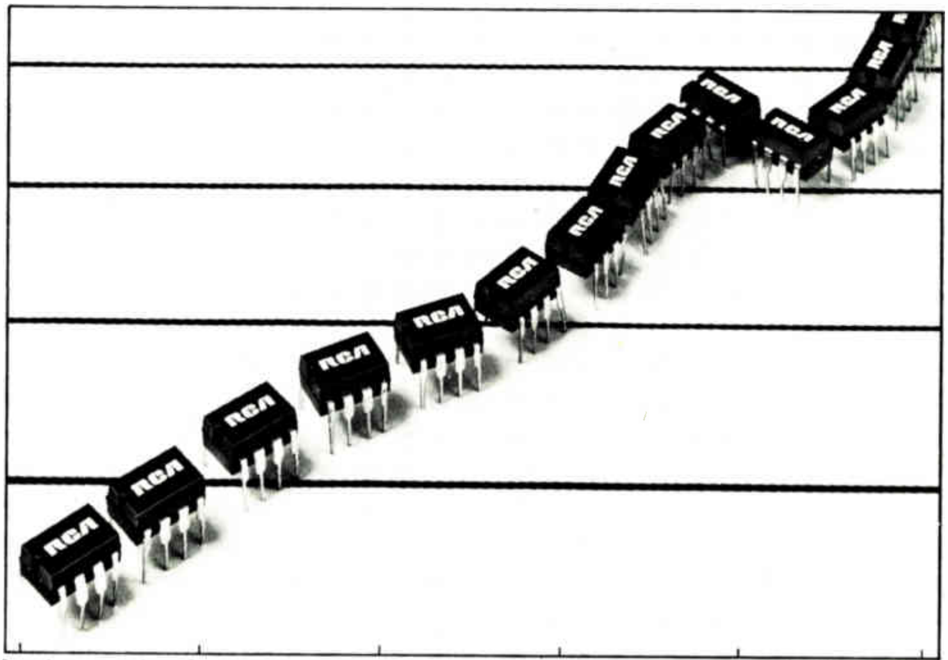

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NEC and NEC Toshiba expand power of low-end mainframes . . .

Nippon Electric Co. and NEC Toshiba Information Systems Co. have just increased the power of the bottom end of their mainframe line with their ACOS System 250 models 40 and 60, which they say **include features formerly found only on the largest computers.** Both are designed for a combination of multiple-workstation, batch, and on-line processing. Much of the operating system is built as firmware or hardware for faster speed; this design also makes the entire read/write memory available to users. Throughput is said to be 0.1 million instructions per second for the model 40, 0.2 million instructions per second for the model 60. The main memory capacity of the model 40 is from 256 kilobytes to 1 megabyte in 256-kilobyte steps, and the model 60s's capacity extends to 2 megabytes. The two will compete in the same market range as IBM's new System/38 and its just-announced 4300 series (see p. 85).

. . . and Siemens extends its low end downward

Spurred by the market success of its desk-sized computers 7.708 and 7.718, West Germany's Siemens AG will soon come out with its 7.706, another low-cost machine that extends the company's line downward. The new model, which Siemens considers "our answer to IBM's System/38," will rent from upwards of about $3,700 a month, depending on configuration. Like the 7.708 and 7.718, the 7.706 uses a simplified version of Siemens' virtual, dialog-oriented operating software BS2000. The new model's central processing unit **performs some 90,000 operations per second.** Its main memory has a capacity of 384 kilobytes, extendable to 1,024 kilobytes.

Philips developing 3-Gb/s ECL multiplexer for fiber-optic links

With an eye to future long-haul fiber-optic telecommunications links, the Philips Research Laboratories in Redhill, Surrey, has come up with a superfast monolithic multiplexer capable of interleaving four 250-megabit/second bit streams into a single 1-gigabit/s data stream and of demultiplexing it at the receiver. **Key to the emitter-coupled-logic multiplexer is a current-steering ring circuit that controls a bit serializer and halves the clock rate for a given multiplexed data rate.** The experimental integrated circuit can thus be clocked at up to 1.5 GHz to give a 3-Gb/s maximum data rate. That's at least 10 times faster than production ECL multiplexers. This speed will be needed if the broad bandwidth of fiber-optic links is to be exploited. One-of-eight-line and higher-order multiplexers can be built from combinations of the ICs. Circuit design yields transistors with a 5-GHz cutoff frequency. The part consumes 500 mW.

French town gets network that ties bank to POS terminals

A cashless society of sorts has begun to emerge in Bourg-en-Bresse, an agricultural town some 40 miles northeast of Lyons. Early this month, the Banque Régionale de l'Ain put into service a network of 13 IBM 3614 automatic teller stations and a batch of IBM 3608 point-of-sale-terminals in more than 50 stores and service stations in the town, all tied to the bank's central computer, an IBM 370/138. In addition to the usual card-controlled transactions at the teller stations, card holders can also pay for purchases at the point-of-sale terminals, which both debit the buyer's account and credit the store's account immediately. IBM says this is the first network of its kind in Europe and **the first anywhere that debits and credits accounts in real time through a point-of-sale terminal.**

International newsletter

ITT Semiconductors gears up for 64-K RAM production

For its British-designed 64-K random-access memory, scheduled for the second half of 1979, ITT Semiconductors will back Mostek Corp.'s refresh specification of 128 refresh cycles per 2 ms, rather than Texas Instruments Inc.'s 256 cycles, 4 ms, but has not yet decided on automatic refreshing. With production of 4-K and 16-K RAMs now running at 150,000 parts per month, ITT is the largest memory maker in Europe. It is investing **$20 million, partly supplied by the British government, in 4-inch wafer facilities, project aligners for 3-μm line-width electron-beam masks, and an automatic chip-bonding production line** at its Footscray, Kent, facility. As the assembly line phases in, ITT plans to bring Far East assembly operations back to the United Kingdom.

Fixed-head VCR uses old idea to get reel without end

A fixed-head video tape recorder being developed by Toshiba Corp. features a cassette with a single reel of endless tape—the planar magnetic video equivalent of Thomas Edison's cylindrical phonograph records. The tape has 220 tracks across its width. Toshiba's scheme allows the 100-meter loop, which runs at 6 m per second, to give one hour of playing time. The relative speed between the head and the tape is similar to that of the currently popular helical-scan VHS and Betamax VCRs (which use a slow-moving tape and rapidly moving heads), permitting the use of the same types of heads and tapes. **The microprocessor included in the prototype permits random access of individual tracks;** track access time is 20 ms to traverse one track pitch. Toshiba says the recorder is suitable for both consumer and professional use.

BBC codes composite video color signal to pack in 34 Mb/s

Hastening the day when European nations will interchange broadcasts over high-quality digital, instead of analog, links, British Broadcasting Corp. engineers have demonstrated a composite PAL signal-coding technique that packs a complete television signal with all its ancillary services into a standard 34-megabit/second data link. In contrast, digitization of the video signal using conventional pulse-code-modulation techniques takes up at least 100 Mb/s. The BBC system cuts the bit rate by **coding the composite video signal, rather than its constituent colors, by removing the line and field blanking intervals,** and by the use of a differential PCM. Britain's Independent Broadcasting Authority is also adopting a similar approach. However, this approach contrasts with West German and French systems using constituent color coding.

Hitachi to sell color TVs to China . . .

Japan's Hitachi Ltd. says it has a contract with the People's Republic of China to supply 20-inch color TVs for reception of PAL telecasts. **The firm will ship 100,000 units,** at the rate of 1,000 a month, starting in March. It will also ship 10,000 air conditioners for nonresidential installations—probably offices.

. . . while Sharp will ship LCD capability to East Germany

The Japanese and East German governments have given the go-ahead for Sharp Corp. to export the plant, technology, and materials to make liquid-crystal displays for calculators and digital watches to the Foreign Trade Enterprise of the GDR Elektronik Export/Import. The plant will be located in East Berlin. Sharp expects to ship equipment in July. **It says that the value of the deal is roughly $7.5 million.**

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(1) Gnostic Concepts, Inc., *VLSI Technological Market Forecast*, 1978, Palo Alto, California.
(2) Anderson/Bogart, *Vertical Dis-Integration* 1978, Los Altos, California.
(3) Linear Corp., Bill Schanbacher, President, Inglewood California.
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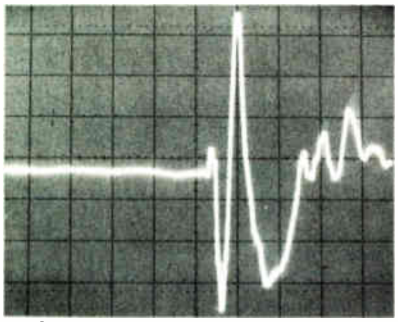

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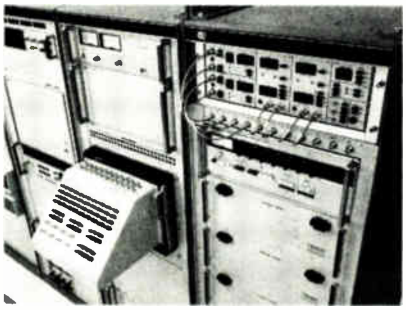

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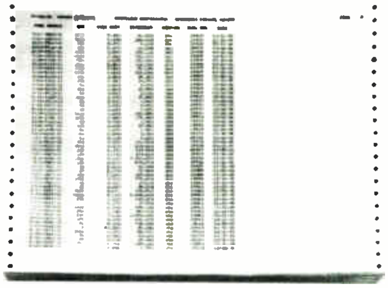

Digital storage gives you maximum analysis flexibility. You can transfer the data, already digitized, to mag tape, disc or other permanent storage. Or you can read the data out directly to a programmable calculator or computer system.

The 8100 features an 8 bit, 100 mHz ADC with 2048 word memory to help you capture and analyze analog signals. Other Biomation products also enable you to convert your scope to a "super scope" by adding digital storage. For more information, or to arrange a demonstration in your lab, call S. Reynolds (408) 988-6800. Or write us: Gould Inc., Biomation Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050.

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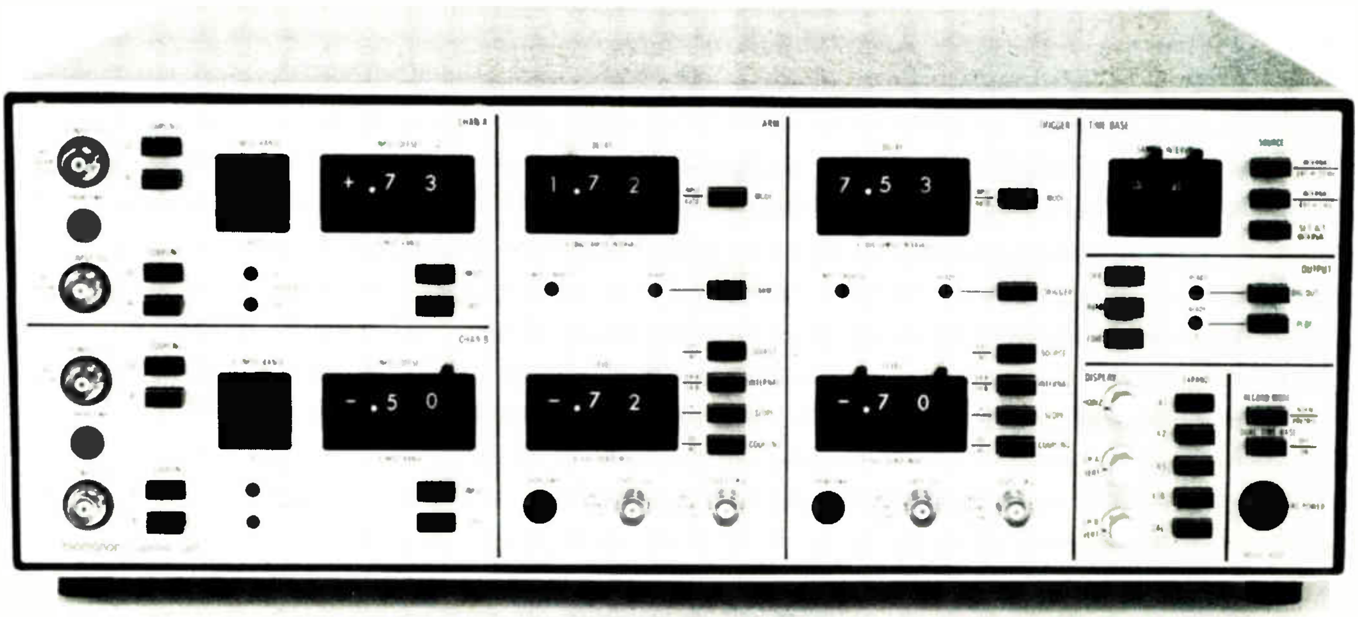


Multiple-channel codec uses CCD filters for eight subscriber lines

Plessey eschews both usual single-channel approach and switched-capacitor filters in developing a five-chip set

Though most coder-decoders built so far are single-channel devices, some designers argue that multichannel codecs could lower overall system costs by reducing chip count. Opting for the latter approach is Plessey Ltd., with a five-chip set for eight subscriber lines.

Developed by engineers at the firm's Allen Clark Research Centre, Caswell, in collaboration with colleagues at Plessey's Telecommunications Research Centre near Maidenhead, the part uses speedy emitter-coupled logic and high-density integrated injection logic for the single-chip codec. The other four chips use charge-coupled devices to implement the filters needed for the eight transmitting and eight receiving channels.

Furthermore, Peter John Schwartz, a development engineer at the Clark center, who delivered a paper on the set at this week's International Solid State Circuits Conference, is confident that they will soon be able to pack eight filters on a chip instead of four, yielding a three-chip set.

Feasible. Samples of the five-chip set are scheduled for the end of 1979, but Plessey has already proved the feasibility of its multichannel concepts with a two-chip successive-approximation codec announced in November [*Electronics*, Nov. 23, 1978, p. 69] that contains no filters. It comprises an ECL chip to perform the analog function and an n-channel ion-implanted metal-oxide-semiconductor chip for the control logic.

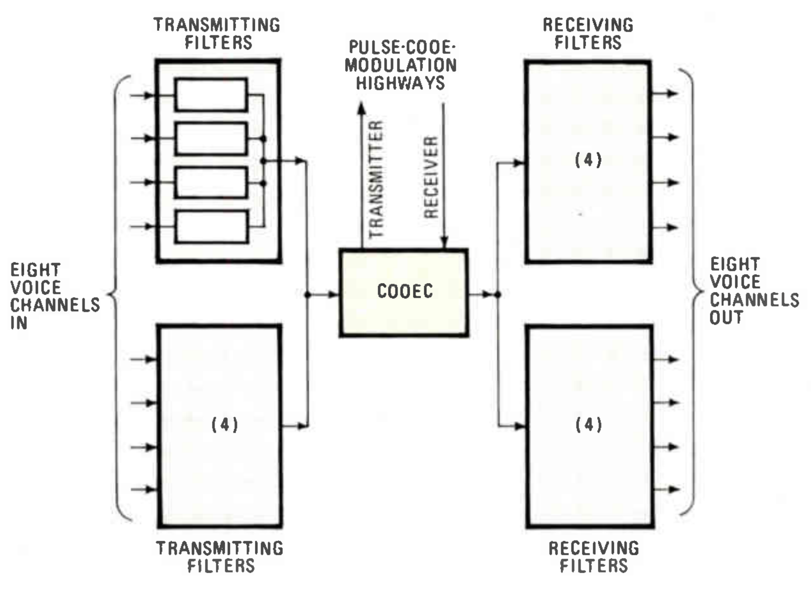
The two are being combined for the new set, and filters are being added.

The two-chip codec operates at 2.048 megahertz, producing a sample every eight clock pulses, or 3.9 seconds. It can decode the full 32 channels of the European CCITT pulse-code-modulation system.

Encoding, though, is slower, because guard bits must be inserted before samples to ensure that the first signed sample bit is accurate and after samples to allow the sampling amplifier to settle. Without these precautions, crosstalk and adjacent channel sampling can occur. Therefore the codec encodes 16 channels. In duplex operation it handles 8 channels—that is to say, 8 subscriber lines.

The 104-by-76-mil bipolar chip contains a fast digital-to-analog converter, band-gap voltage reference, comparator, and two-channel multiplexer. It consumes 350 milliwatts from a 5-volt supply. The 112-by-88-mil control chip contains three registers and the channel-selection logic. It requires 150 mW, also from a 5-V supply.

For the new set, the analog section remains the same, but the control logic will be shoehorned onto the bipolar chip with the aid of a high-density I²L layout. This 250-gate logic system will fit into the area now used for the interface buffers and level shifters. Thus the chip size



Five for eight. Plessey uses five chips to realize a codec (one chip), plus filters (four chips), to service eight subscriber lines. The filters are implemented with CCD technology.

will remain about the same.

To restrict the transmitted signal bandwidth to the 300-Hz-to-3.4-kHz level specified by the CCITT, a channel filter is required. Intel, for one, uses switched capacitors for this function [*Electronics*, Nov. 23, 1978, p. 220], but Plessey has chosen a CCD sampled-data filter. Already realized is a 100-tap transversal filter that consumes 30 mW.

Says Schwartz, "We went for CCD because of the higher circuit densities and lower power consumption achievable. There have been reports that CCD filters are noisy, but we have not found that to be the case." Target consumption for the quad filter is 25 mW per filter.

There are other advantages to a CCD solution. The CCD input and output sample-and-hold circuits fulfill the normal signal-holding requirement of a sampled-data system, and they can also be clocked sequentially to perform the analog multiplexing function, thus switching each channel in turn onto the codec. In effect, "you get the multiplexer free," Schwartz comments.

Though he will not say what the set has been developed for, a good bet would be System X, the British Post Office's all-solid-state digital exchange system due to be unveiled in Geneva this year. □

France

Thomson-CSF getting ready for VLSI with fast optical wafer stepper

One essential for France's plans for very large-scale integration in the early 1980s will be a fast wafer-stepping device. To help realize those goals, Thomson-CSF has come up with a fast photorepetition unit that uses a new alignment method.

Though current forecasts for electron-beam methods suggest a maximum throughput of 10 wafers per hour within the next few years, Thomson-CSF's Corbeville laboratories' unit looks capable of processing 50 3-inch wafers per hour. And with a resolution of 1 micrometer and an alignment tolerance of 0.1 μm, it promises to outperform other direct-step-and-repeat-on-wafer machines.

Thomson uses a 5- or 10-to-1 projection ratio and thus dispenses with a contact mask. The machine has an automatic search field of 20 by 20 μm, and alignment time is less than 200 milliseconds per mark per axis when initial misalignment is only 1 μm. For a 3-in. wafer having 100-square-millimeter circuits, total alignment time is about 10 seconds, with reindexing at each chip.

To achieve this performance, Thomson aligns successive exposure zones on the wafer with a reticle in the exposure optics. The positions of the reticle and of the zone are each defined by an L-shaped mark. When the two marks are correctly aligned, they form a cross.

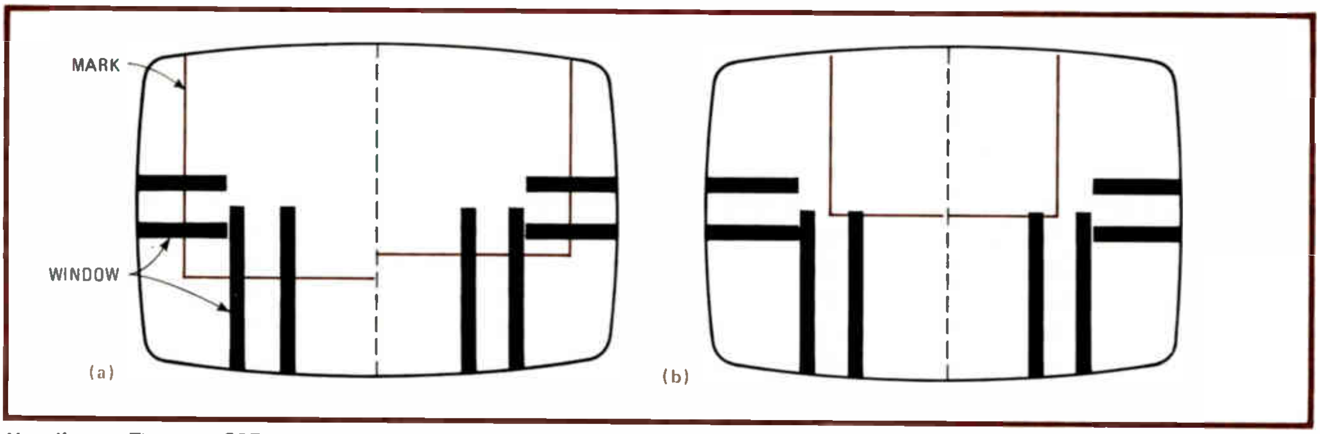
Analysis. The images of the zone and reticle marks are projected by separate optical systems onto two areas of a vidicon target. The areas, each have two windows (see figure).

Each window is analyzed successively by a scanning electron beam. Comparison with window-position data yields a video signal from each that is proportional to the extent that the mark image is off from the center of each window.

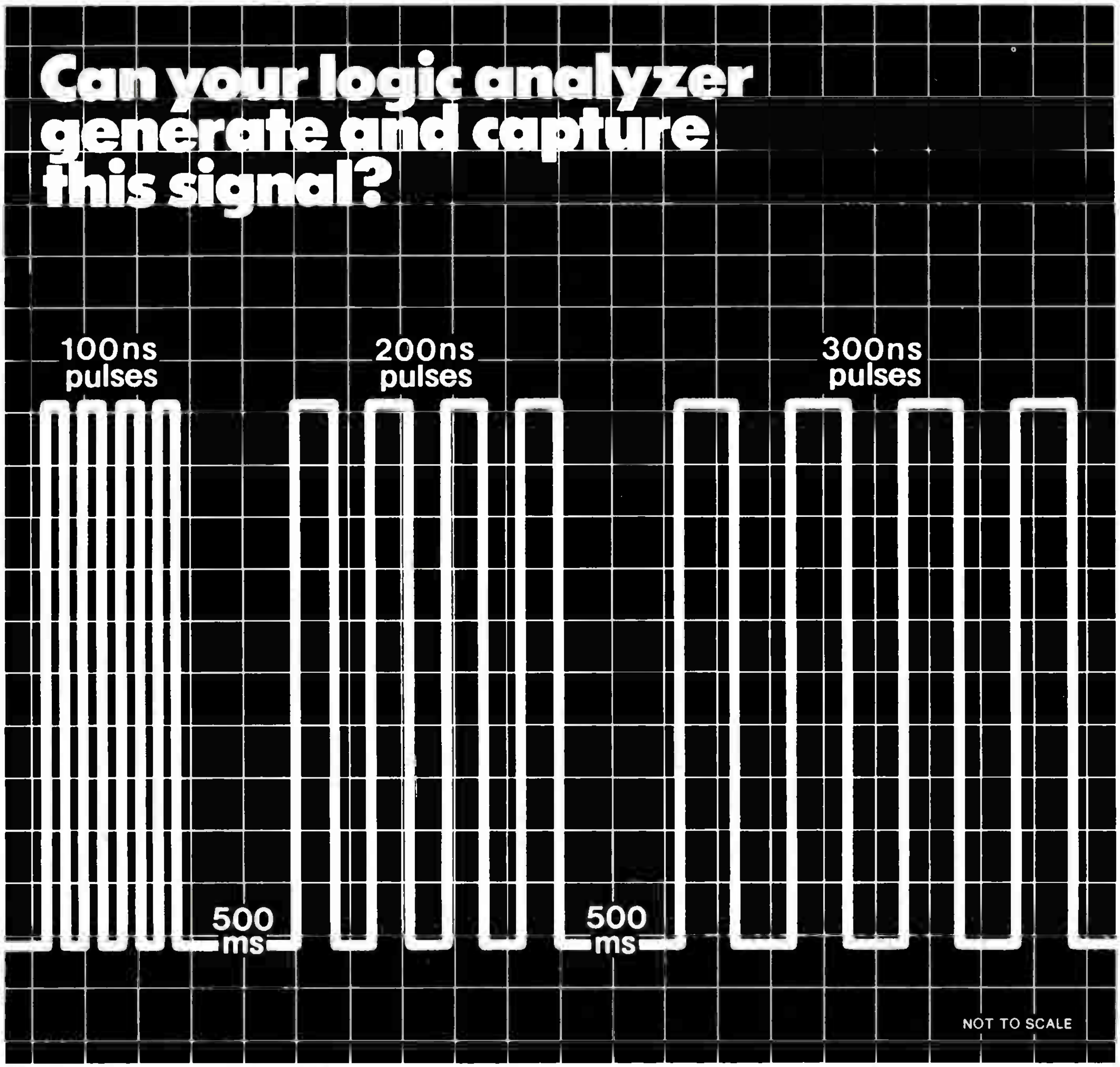
Actually, Thomson uses the third harmonic of the scanning signals as alignment signals. This, the developers say, is the best compromise for a signal that can handle the search field with adequate accuracy.

The misalignment can be corrected by automatically aligning the reticle and then manually aligning the wafer or vice versa. Thomson used the latter method with its experimental unit because the positioning of the reticle need be only one tenth as accurate as mechanical displacement of the wafer. But it believes the other way around would be faster.

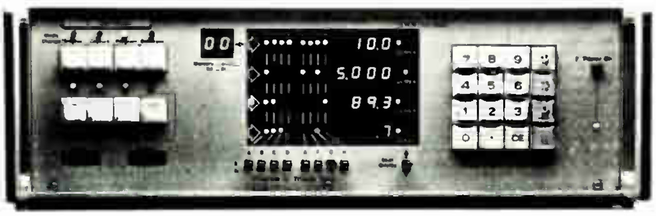
As Michel Lacombat, chief engineer for the project, points out, the firm is not alone in developing high-precision photorepeater techniques. GCA Corp. in the U.S. makes a



New lineup. Thomson-CSF's optical wafer stepper uses an L-shaped mark on the reticle and on the wafer zone for alignment. Images of the marks are projected separately onto two areas of a vidicon target each containing two windows, as shown in artist's rendering (a). The windows are analyzed to adjust both reticle and wafer. When they are aligned, the marks and windows each form a cross (b).



The Gould DSA 600 can.



The Gould DSA 600 digital synthesizer analyzer is the first instrument designed to generate and capture pulse trains with unusual values in a state linear display format.

With eight input channels plus qualifiers and 32 memory locations, the processor controlled DSA 600 allows logic waveforms, even unpredictable ones, to be captured, stored and analyzed. It even permits complex sequences of timing, drive or test signals to be readily synthesized or modified without specially constructed hardware.

The DSA 600 is simple to operate, fast and accurate with no ambiguity or drift because measurements are locked to a precise clock with a timing range of 100 n sec. to 100 sec. for each logic state.

For complete details on the DSA 600, call the toll free number now. Remember the DSA 600 also carries Gould's full two-year warranty covering all parts and labor (exclusive of fuses, calibration and minor maintenance). Or contact: Gould Inc., Instruments Systems Division, 3631 Perkins Avenue, Cleveland, Ohio 44114 for a demonstration.

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machine that accepts wafers up to 4 in. in diameter with an alignment tolerance of 0.1 μm and a throughput of 20 wafers/hour.

Thomson's approach, meanwhile, needs further development. For example, the machine would need new wafer-handling peripheral equipment to feed in wafers and take them away after the photorepetition.

But for the moment, work has stopped as Thomson looks for more government funds. The current level was achieved with the help of the government, and in theory more aid is available for the development of a wafer-stepping machine under the French components plan. So far, though, the government has not decided on a technique or a builder. □

West Germany

Audio compander squelches hiss and hum better than Dolby system

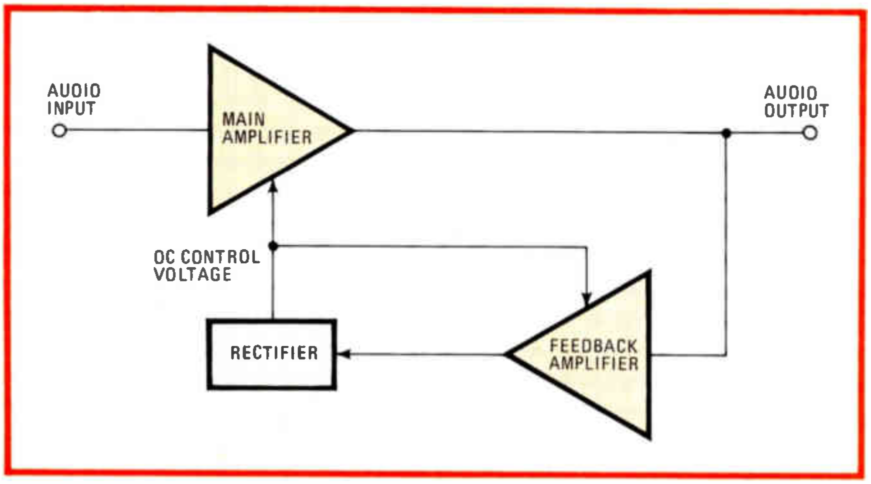
Mention "Dolby" and millions of audiophiles think of today's most popular system for suppressing noise in audio-tape equipment and fm stereo receivers. Proof of the excellence of the U. S.-developed system is its use in more than 22 million cassette tape recorders worldwide.

Now preparing to lock horns with Dolby is a noise-suppression system developed for consumer applications by Telefunken GmbH, the entertainment electronics arm of West Germany's AEG-Telefunken.

The new system, called High Com, outperforms Dolby in two important ways, Telefunken says: it removes 10 to 12 decibels more noise; and it does so over virtually the entire audio spectrum, typically 30 hertz to 20 kilohertz. This means that High Com suppresses annoying power-frequency hum at 50 or 60 Hz. Dolby, on the other hand, is effective only from 300 Hz up.

During compression, low-level signals are amplified so that any noise present in the transmission path or storage medium is swamped by the strengthened signal. The noise is then attenuated during expansion.

High Com—the name derives from high-fidelity compander—is based on Telefunken's three-year-old telcom c 4, a four-channel compander used in broadcast-studio equipment. It provides noise suppression "that is substantial for a system designed for consumer use," says Hans-Joachim Thuy, High Com product manager at the Hanover-based company. When used on an audio cassette tape recorder, noise is reduced by an average of 20 dB to 1% of its original power level.



Doubling up. Use of two identical wideband amplifiers in Telefunken's High Com compander yields an average noise-suppression figure of 20 dB from 30 Hz to 20 kHz.

Telefunken's compander is a bipolar integrated circuit that contains two identical wideband amplifiers and a rectifier (see figure). One amplifier handles the audio signal; the other picks off the output and feeds it to the rectifier. The dc output of the rectifier controls the gain of the main amp and also keeps the output of the feedback amp constant. Use of two amplifiers enhances noise suppression, and the resulting system has a compression-to-expansion ratio of 2:1.

In addition, High Com's feedback configuration makes it relatively insensitive to changes in component specifications because operation is influenced by the ratios of component values, rather than by their absolute values. It is also insensitive to differences in the transmission channel or storage medium—for example, cassette tapes with different recording sensitivities. With a Dolby system, an out-of-spec input to the expander would distort the output, but with High Com, the company says, frequency response is unchanged for signal-level deviations as great as ±6 dB.

The IC, in production at AEG-Telefunken's semiconductor facility in Heilbronn, comes in a 24-pin dual in-line plastic package. Designated U401B, it integrates some 450 devices including 200 transistors on a 3.1-by-2-millimeter chip.

Lots of interest. Given High Com's good performance, Telefunken officials are confident that it will be widely adopted. Already, some 20 electronics producers in Europe and 4 in Japan have expressed interest, Thuy says, adding that the company will supply the ICs to other firms or grant licenses for their production.

Initially, the system will turn up in cassette recorders, with Telefunken and a number of other companies in Europe to show their first High Com versions at the Radio and Television Exhibition in West Berlin this summer. The recorders will be designed to play back Dolby-encoded cassettes.

The system may also find use in radio receivers, the company says;

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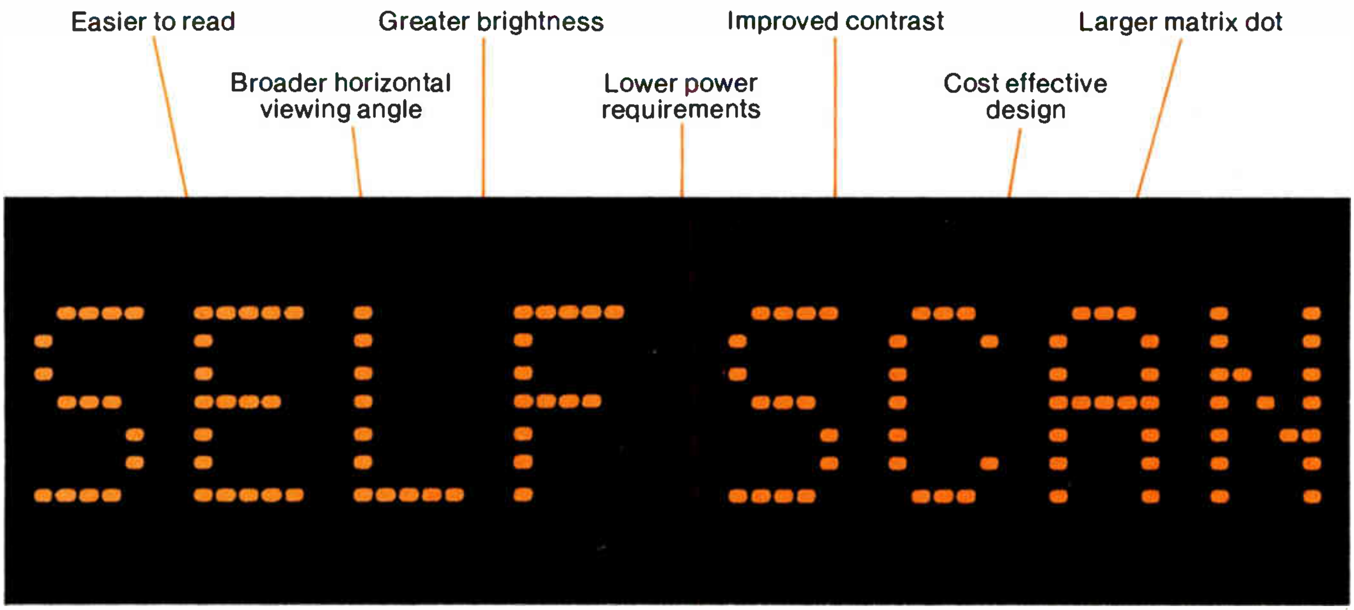

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Circle 71 on reader service card

however, that would require that broadcasting authorities and set makers agree to adopt the system on a wide basis, Thuy cautions.

Another application would be in television sets, where interference signals are encountered mainly at the low end of the radio spectrum. With the new compander built in, a TV receiver would deliver practically noise-free sound.

Currently a bit more expensive than its rival, High Com will come down to Dolby's price level as volume production gets under way, Thuy says. □

Great Britain

Dedicated traffic-information service to start trials in London area

Britain's motorists could look forward to reduced traffic delays and lower fuel bills if a dedicated-broadcast traffic-information service proposed by the British Broadcasting Corp. and shortly to go on trial in the London area is implemented nationally.

Motorists using the system, called Carfax, will be able to pick up detailed news of local traffic delays and road construction or repairs with the aid of a car radio attachment that mutes normal reception when receiving a traffic broadcast from a nearby transmitter.

In all, a chain of 20 low-power transmitters, each programmed to broadcast local news in sequential time slots on a common frequency, would be needed to reach 85% of UK motorists, and 70 transmitters would provide complete coverage. For the London-area trial 5 transmitters will serve a test population of some 500 motorists.

Backed up. The official go-ahead for the trial was expected several weeks ago, after a long period of committee evaluation [*Electronics*, March 2, 1978, p. 64], but it has been delayed because of the truck drivers' strike.

Other European countries have already turned to electronics to ease their traffic problems. Since 1974 a number of fm stations in West Germany, Austria, and Switzerland have preceded regular traffic news bulletins with a subcarrier identification tone that activates the car receiver. Called ARI for automobile-drivers' radio identification, the system was developed by Blaupunkt-Werke GmbH, a subsidiary of West Germany's Robert Bosch GmbH.

Carfax, conceived by BBC engineer R. S. Sandell six years ago, takes the traffic-information concept a stage further: it is a dedicated system, and it provides much more information tailored to a fairly small area.

Each Carfax transmitter relays messages relating only to its area and so spends most of its time switched off, even during rush hour conditions. The transmitters are time-division-multiplexed in a so-called ring mode, in which only one is broadcasting at any given time.

Capturing. To make sure that a motorist's radio responds only to the transmitter in its area, BBC engineers rely on the capture effect of fm broadcasts and enhance it with a high modulation index—that is, a wide deviation at low modulating frequency. Consequently, they chose the medium-frequency band.

In practice, frequency-modulated tones are sent by each transmitter at the start and finish of each message. All other transmitters radiate a low-power continuous-wave inhibiting tone simultaneously with the start tone. The strongest signal—either the start tone or one of the inhibiting tones—captures the car radio.

The message itself is carried by conventional amplitude modulation and has a telephone bandwidth of approximately 300 hertz to 3.5 kilohertz. Finally, the finish tone returns the car radio to normal reception.

This arrangement, says Sandell, allows all transmitters to operate at the same frequency, resulting in considerable spectrum economy and the possibility of a single international frequency for traffic information. However, ARI already has a head start as a candidate for a European standard system, as several million motorists already use it and it is well established in West Germany.

Three basic receivers have so far been developed for the trials: a completely separate receiver, an add-on unit to existing car radios, and an integrated unit. The motorist can operate his radio in any of three ways: switched to ordinary broadcasts without interruptions, ordinary listening with interruptions for traffic news, and tuned to traffic news only.

According to BBC engineers, a conversion unit for an existing radio might cost something like $20 in volume production. But others think that figure is optimistic.

Before the London-area trials can get under way, however, a clearing-house will have to be established to edit police information and schedule it under computer control so that each transmitter reports only messages of local interest.

For their part, Blaupunkt engineers say that their system could be set up immediately in the UK without a dedicated transmitter chain. Nonetheless they have come up with a proposal to harmonize both systems by changing Carfax from the medium- to the very high-frequency band, which ARI uses, and transmitting both ARI and Carfax alert tones.

The trouble with traffic broadcasts by regular stations, such as ARI provides, Sandell responds, "is that they can only give limited coverage. The police gather masses of information on road conditions which they cannot use because there is not enough air time. Another problem is that motorists only want to hear news that might affect them."

More importantly, BBC engineers argue that if Carfax moved to the vhf band, the capture effect it relies on would be less certain, since vhf wave propagation is affected by topological conditions. □

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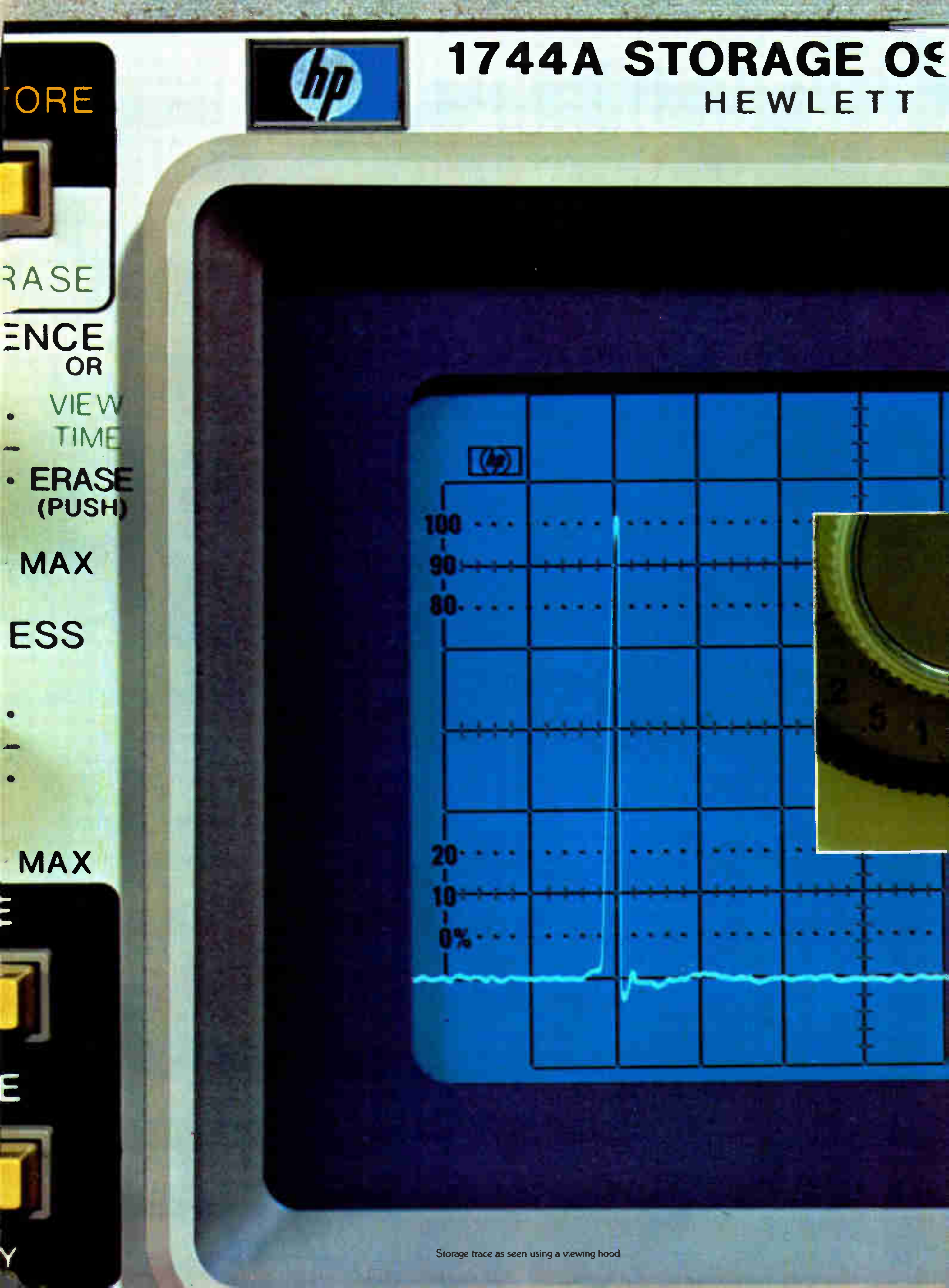
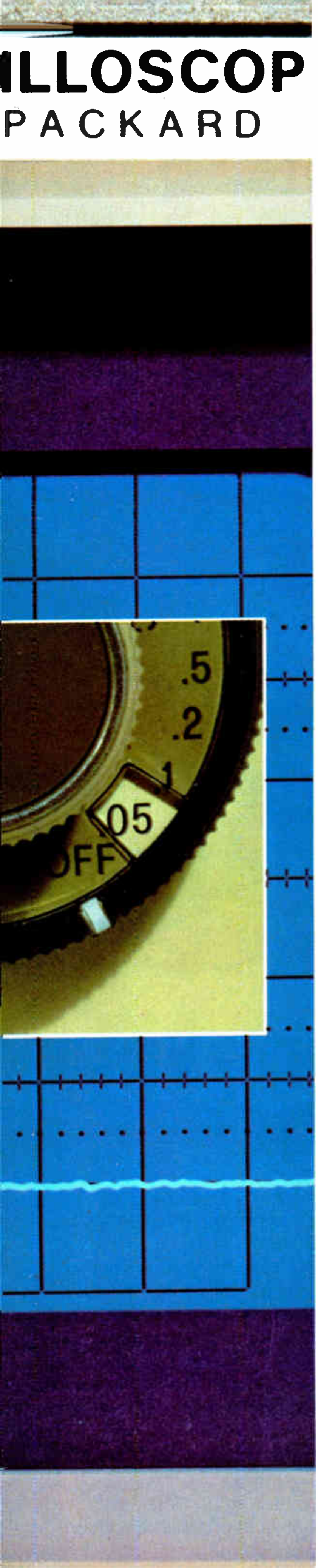


Storage trace as seen using a viewing hood



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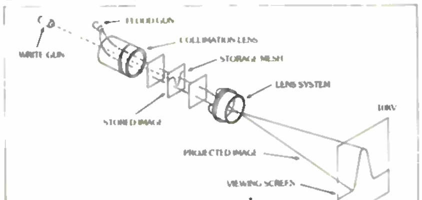

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Take a good, hard look. Any input signal within bandwidth specification will be displayed cleanly by the 1744A, even at the maximum writing speed of 1800 cm/μsec when using a viewing hood. That provides the sharpness you need for detailed evaluation of hard-to-catch waveforms. Our Auto Erase/Auto Store modes simplify your pursuit of these elusive signals. Auto Erase provides hands-off operation while Auto Store prepares the scope to snare the troublemaker the instant it occurs. Both are powerful tools for capturing the spurious spikes that disrupt your logic circuitry.

Catch that glitch. Expansion Storage technology combines a small storage mesh (about the size of a postage stamp) and an expansion lens system. This exclusive arrangement permits a writing speed of 1800 cm/μs and a fine spot size, which lets the 1744A write faster and further than any other 100 MHz storage scope. That gives you full-scan glitch capture capability over a broad range of sweep speeds and repetition rates.

A new view. Three channels are better than two. And with the 1744A you have pushbutton selection of a third-channel trigger view. Now you can view timing relationships between the trigger signal and the two vertical channels simultaneously.

Rounding out the 1744A's capabilities are these convenient measurement features: **Easy-IC Probes** to improve closely spaced probe connections and eliminate shorting hazards; a selectable input impedance (1 megohm/50 ohm) for general purpose probing or 50 ohm matching; and measurement sensitivity as low as 1 mv/div to 30 MHz on both channels without cascading. Priced at $5250*, the 1744A furnishes the state-of-the-art technology and performance needed today in digital design and trouble-shooting applications.

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Circle 75 on reader service card

Parallel testing keeps your memory traffic moving.

Your production line is probably spewing out a virtual river of memory devices: RAMs, ROMs, EPROMs up to 65K x 8 bits. Your test system can't be a bottleneck. It must pace the flow, not choke it.

Fairchild developed the Xincom 5581 Parallel Operation Memory Tester specifically to speed throughput and help reduce the cost of testing.

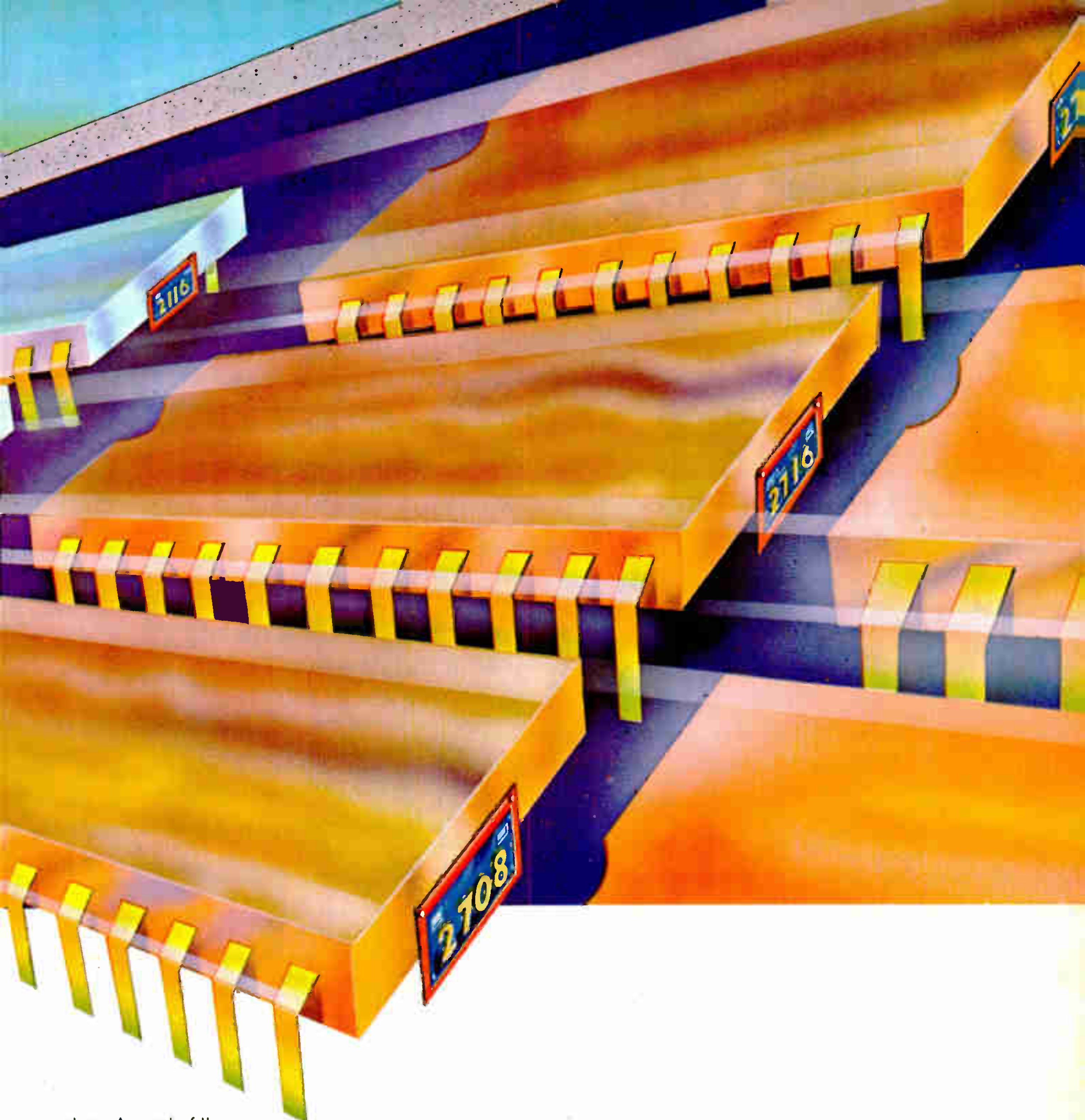
The 5581 is a high performance, functional and parametric memory tester. It can parallel test up to four 65K x 4 bit multiplexed address RAMs. And it's done with only two heads, each with two sockets or connectors for wafer probers or device handlers. Thus, the 5581 combines the throughput of a 4-head tester with the mechanical simplicity of a 2-head system.

In its maximum configuration the 5581 will handle:

- ☐ 65K x 4 bit RAMs with multiplexed addresses, four at a time with two at each test head:
- ☐ 65K x 8 bit RAMs and 4K x 8 bit ROMs two at a time, one in each test head:
- ☐ 65K x 8 bit RAMs or 4K x 8 bit ROMs time sequential with a different device at each head.

On-the-fly timing edge control provides test accuracy and reproducibility for production testing of dynamic MOS and bipolar memories.

The 5581 can be used as a stand-alone tester or as a satellite to the Xincom III distributed test



system. As part of the Xincom III test system, it can store, analyze and process vast amounts of test data or prepare schmoo plots, wafer maps, or trend graphs. You also get compiling and test program editing capabilities.

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Circle 77 on reader service card

VAX Program Capacity. Ask any user.

"VAX offered us almost three times the address space of our 370/168."

Bill Miller, Senior Systems Analyst
Chevron Geophysical Co., Houston, Texas

Chevron Geophysical is heavily engaged in seismic data processing involving matrix operations on large arrays.

As Senior Analyst Bill Miller states the problem: "Our IBM systems, running on TSS, give 24 bits of true address space—for a maximum program size of 16 megabytes. But only 10 to 12 megabytes of this can be used by the programmer—and our application had grown to the point that TSS was simply cramping us.

"With the VAX-11/780, we know we can have application programs that use a full 32 megabytes as we're configured now—and it could be more if we wanted."

But Chevron didn't buy their VAX without first benchmarking it against the far more expensive 168.

Miller comments: "We developed a number of benchmarks to test specific areas of performance. On the average, the VAX CPU appears to be about a third as fast as the 168, which is really quite impressive. And it's very possible that for certain applications, we may see a negligible loss of throughput over the 168, thanks to VAX's unique page clustering scheme."

And as far as system performance to date, Miller reports: "The VAX/VMS operating system has been remarkably reliable. The people at Digital have done a phenomenal job."

"VAX's true 32-bit addressing puts its potential capacity so far out, we don't have to worry about it."

Dr. Edwin Catmull, Director,
Computer Graphics Lab
New York Institute of Technology,
Old Westbury, New York

The Computer Graphics Lab at New York Institute of Technology is a leading research and production facility for computer animated commercial and educational films.

In Dr. Catmull's words, here's what brought NYIT to the VAX-11/780: "While spending years developing our capabilities with minicomputers, we

continually ran into the problem of small address space. Our work demands the large address space we can get with a 32-bit machine. We were dealing with extremely large, randomly accessed data bases, and memory mapping is not the answer."

Dr. Catmull continues, "The VAX UNIBUS lets us easily hook up a wide range of special video display equipment that had previously been on the minicomputers, and allows us to easily convert our algorithms."

According to Dr. Catmull, "VAX has fulfilled our expectations for speed, program size, ease of conversion, and ability to attach special graphics equipment."

"With a 22,000-point data base, we really needed VAX's huge memory capacity."

Peter Ackermans, Manager of Computer Systems Engineering
CAE, St. Laurent, Quebec, Canada

CAE Electronics Ltd., currently has thirteen VAX-11/780 systems under development for both flight simulation and supervisory power control.

Here again, VAX capacity was key. Systems Manager Peter Ackermans told us: "Our SCADA systems for the power market need to handle a 22,000-point data base. VAX's large memory capacity and the VAX/VMS virtual memory operating system made it a very attractive machine."

But speed was also important. "In flight simulators," Ackermans continues, "top FORTRAN performance is essential, and on that score, VAX measures up well. Our FORTRAN programmers have also been impressed with the machine's debug facility and file handling capabilities."

Digital's VAX-11/780, with its true 32-bit address space, has set a new standard for program capacity. This means that you can run large programs easily on VAX, with a potential for growth that's unmatched in the industry.

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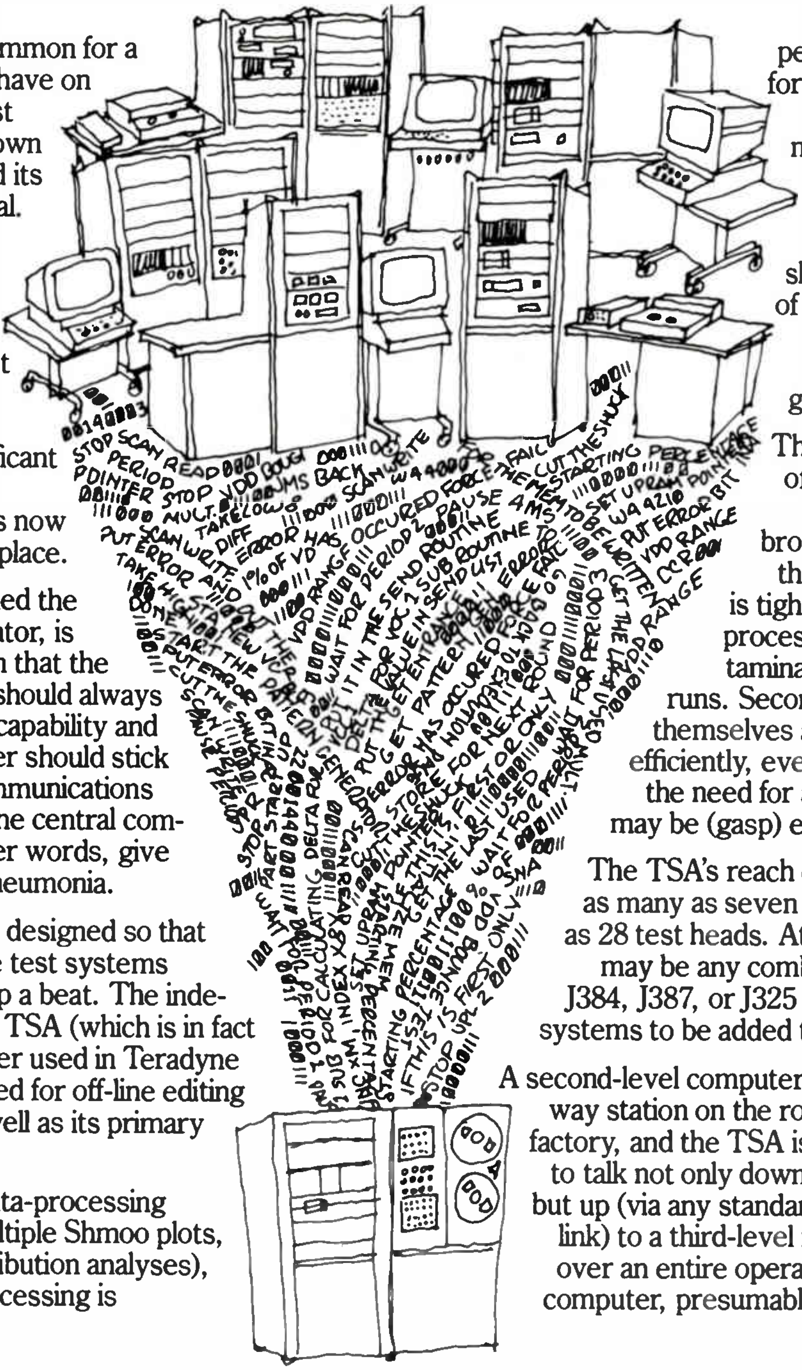


These days it isn't uncommon for a semiconductor plant to have on line a dozen or more test systems, each with its own test program library and its own data output terminal. The situation begs for a clustering of systems around a central computer that can store all the programs and collect all the data. Although the basic idea is simple enough, there are significant differences among the various implementations now appearing in the marketplace.

Teradyne's solution, called the Test System Administrator, is based on the proposition that the individual test systems should always be self sufficient in test capability and that the central computer should stick to management and communications functions. A sneeze at the central computer should not, in other words, give the whole test facility pneumonia.

The TSA was therefore designed so that when it is unplugged the test systems connected to it don't skip a beat. The independence is mutual: the TSA (which is in fact the same M365 computer used in Teradyne test systems) can be used for off-line editing and translating jobs as well as its primary management function.

The TSA has enough data-processing capability to develop multiple Shmoo plots, multiple ADARTs (distribution analyses), and the like, and the processing is performed in real time for fastest possible utilization. The unit is not only scorekeeper but timekeeper as well. One may direct it to pull summary sheets at a given time of day, for example, or to report the time at which the yield on a given system shifted.

The economic benefits of test system administration fall into two broad categories. First, the data feedback loop is tightened, so that minor processing flaws can't contaminate whole production runs. Second, the test systems themselves are used much more efficiently, even to the point where the need for an additional system may be (gasp) eliminated.

The TSA's reach currently extends to as many as seven systems or as many as 28 test heads. At the moment, these may be any combination of Teradyne J384, J387, or J325 systems, with other systems to be added to the list.

A second-level computer is, of course, only a way station on the road to the automated factory, and the TSA is therefore designed to talk not only down to the test systems but up (via any standard RS232 or Bell 103 link) to a third-level mainframe presiding over an entire operation. The third-level computer, presumably, talks only to God.

TERADYNE

Circle 80 on reader service card

Cipher-shifters fight it out

Data Encryption Standard put together by NBS called too easy to crack; critics also seek to keep NSA out of picture

by Harvey J. Hindin, Communications & Microwave Editor

When the National Bureau of Standards decided to write data-encryption standards in 1971, it had no idea how much controversy the move would generate. Charged by Public Law 89-306—the Brooks Act—with setting Federal standards for effective and efficient uses of computer systems, NBS went ahead and developed an algorithm that guaranteed that 2^{55} (70 quintillion) attempts and the use of the method of exhaustion—keep trying till you get it—would be required to crack any code. But by now it might be wondering if it should not instead have worked out a criticism algorithm.

Since most coding experience had been gained in the kind of hush-hush activities the military and other Government sectors engage in, the NBS went to the experts for assistance: the super-secret National Security Agency (NSA). The two agencies were able to cooperate in the development of the standard, known as the Data Encryption Standard, or DES, since the constituency for the efforts would be Federal agencies and the general buyer, with neither group operating under national security directives and procedures. National security cryptography is the NSA's area under the 1947 National Security Act and no conflicts were anticipated.

But this was not to be. In fact, the DES has come under severe criticism in some quarters. According to Martin E. Hellman of Stanford University in Palo Alto, Calif., the DES, which is the kind of algorithm that uses the same "key" or coding base at both the transmit and receive ends, can be cracked. "A $20 million machine can search all the keys of the DES in one day at a cost of $10,000." Worse yet, he says, under certain circumstances, the cost for each cracking run on a DES-coded information signal is between $1 and $100. In fact, of course, any code can be cracked if enough time and money are spent on the job.

Hellman advocates the public-key encryption system, one the NSA had no hand in. In this algorithm, knowledge of the encoding transformation does not automatically imply knowledge of the decoding transformation. Secure data communication in the public system is made possible by

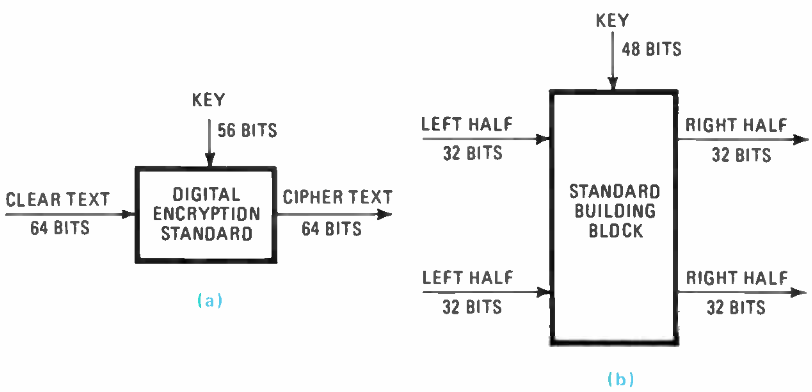
How DES works

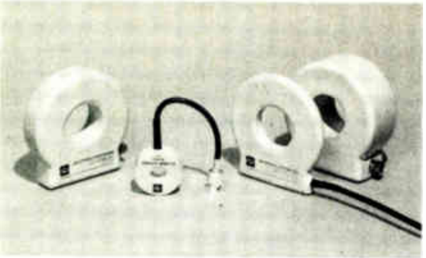
The DES encryption/decryption algorithm is public information and has been published, although individual privacy is insured with a private key. This user-chosen key is 56 bits long and allows 2^{55} possible choices (a). Both the sender and the receiver must have a copy, since the same key is required for both coding and decoding.

Each 64-bit block of data entered into a DES communication system is first transformed through a simple initial permutation that provides two 32-bit channels. Next, all of these bits are reordered according to a defined scheme. Then each 32-bit block is manipulated through 16 iterations with what is called a standard building block (b). Each of these building blocks further permutates the data with the aid of a specific 48-bit key. Each key is different for each of the 16 building blocks and is derived from the 56-bit main key. There is a further simple transposition at the final output, which is similar to the initial transposition. Neither of these transpositions is controlled by an external key.

All of the various scramblings that take place are based on either fixed look-up tables or some permutation procedures. Parts of these were designed by the NSA, and although the transformations themselves have been printed in the Federal Register, the design procedures have been classified, arousing suspicions of "easy-to-decode if you know how."

Decryption is very similar to encryption. The same algorithm is used, but the standard building block keys are used in the reverse order.





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simply using a "telephone book" of the codes for encoding wherein the decoding procedures are associated but secret. With the DES system, encoding is the reverse of decoding and the same key is used. Further complicating the issue, patented work on the key system has been done by Ronald L. Rivest and his associates at the Massachusetts Institute of Technology in Cambridge, Mass.

Hellman not alone. Other critics have been wondering aloud whether some DES coding design procedures were classified by the NSA so that it could break the code if it had to. Others feel the system is too simple to have more than a 10-year life in practical use. What's more, they ask, why is the code not 128 bits long, the much more secure procedure believed to be in the IBM system that NBS chose as a design model?

However, DES is not so bad, maintains Robert Morris, a computer software researcher at Bell Laboratories. "Doubtless, anyone with sufficient time and money can read messages encrypted with it," he says, "but the time and money required are well beyond the means of the local burglar or even the most skilled embezzler." Multimillion-dollar investments in special-purpose hardware would be needed, he maintains.

He thinks the greatest security problem for DES users will be proper selection, custody, and distribution of the key. He sees "no particular reason to believe there was any subterfuge" involved in the design of some of the scrambling boxes (see "How DES works").

Coding and encryption problems have existed since the earliest days of electrical communication. In fact, telegram security was an issue for Western Union back in 1870. Today, with the use of data banks, there is worry about unauthorized transfer of information, electronic crime, electronic sabotage, and other such security problems in the civilian and commercial sector. While work is starting—Dennis Bransted, NBS project leader for computer security, says, for example, that seven commercial LSI chips have been validated to perform the DES algorithm—there is still a lot to do.

As procedures are at present, however, the vast store of expertise available in the diplomatic and military organizations can hardly be tapped, if at all. The way the National Security Agency sees it, its mission is to protect the security of United States communications.

This has been variously interpreted as including not only direct defense information, but also economic data and other potentially sensitive material. For example, the encryption community was shaken by Jeremy Stone of the Federation of American Scientists when he said that code cracking can be used to wage economic warfare.

Denial. Last month, NSA head Vice Admiral Bobby Inman, addressing the Armed Forces Communications and Electronics Association at the State Department in Washington, declared that his agency has not, as some critics claim, exerted an undue influence on scientific research into encryption theory or the development of commercial products. What's more, he says, it turns out that "the legal resources of the Federal government to control potentially harmful non-Government cryptologic activity are sparse."

The "potentially harmful" issue is the bone of contention. Clearly the NSA approach will be conservative in defining the words, while those interested in better algorithms or encryption equipment will feel just the opposite pressure.

In a clear indication that the NSA does not intend to be liberal in its definition of what is vital to the national security, Inman called for rules that would allow him and his agency to prohibit domestic or foreign dissemination of cryptology research when security is involved. Needless to say, the budding cryptology industry in the U. S. is unhappy about this prospect, for it is still small, despite rapid growth in the last five years. However, most of the suppliers of what encryption equipment is available are foreign concerns. According to Ruth M. Davis, deputy under secretary of defense for research and advanced technology, they accounted for more than 75% of 1977 U. S. sales. □

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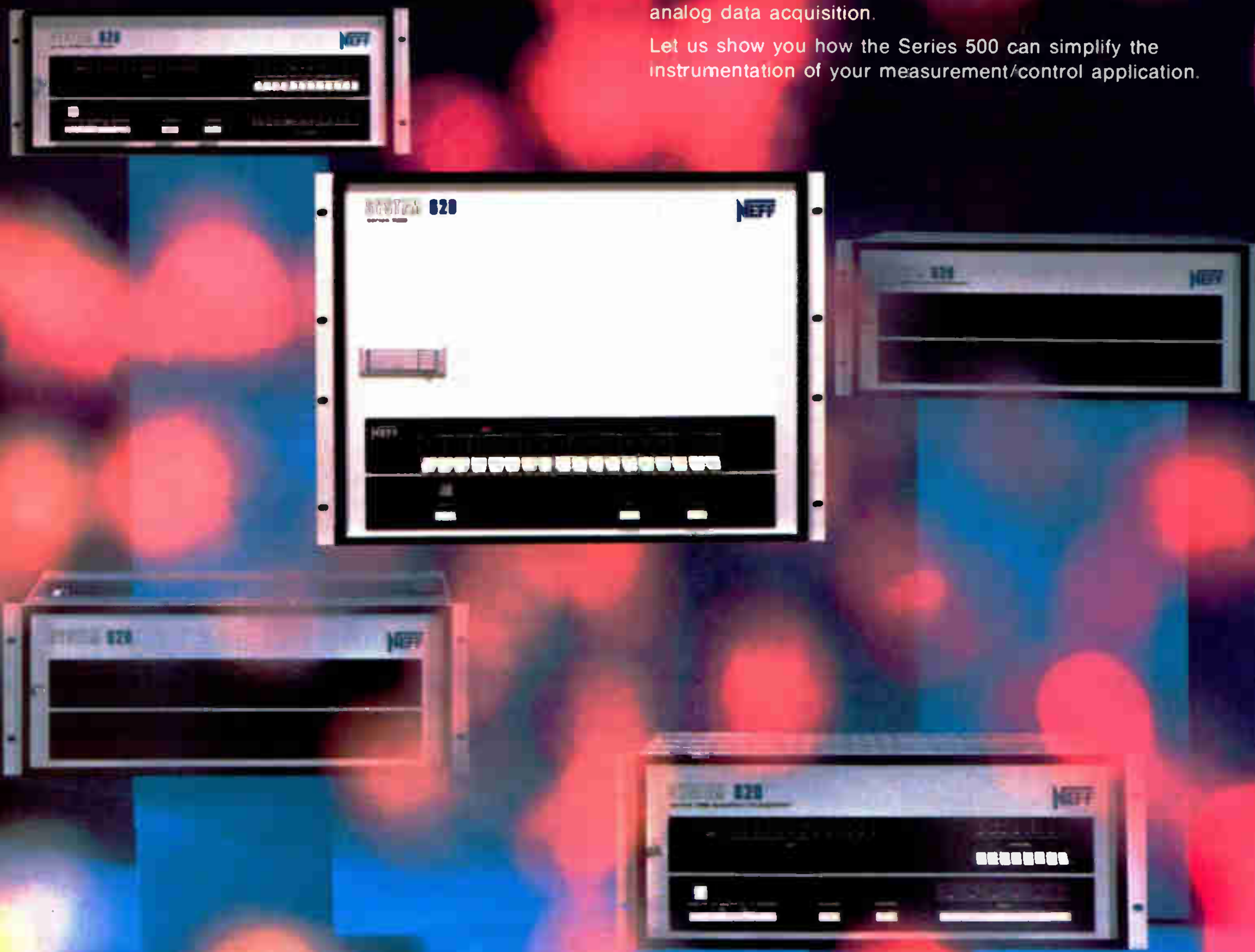

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Computers

IBM has a message: the 4300

New series shows determination of the industry leader to use new technology to offer more for less money

by Anthony Durniak, Computers Editor

IBM is sprucing up its computer line with a fresh coat of high technology. Although the company has consistently dominated the computer market, many competitors have charged IBM with resting on its technological laurels by leaving the nine-year-old System/370 mainframe computers essentially unchanged in the face of rapid developments in almost every area of electronics.

But now the industry leader is polishing its tarnished reputation and using a new generation of chips, peripherals, systems software, and architecture to revamp its line of computers. It is promising improved performance and greater ease of use and maintenance, all at reduced prices, and it has put the rest of the industry, especially the growing legion of IBM-compatible computer makers, on notice that it will use this new technology to lower the quasi-standard price/performance ceiling.

The latest evidence of this, and the third IBM computer to be unveiled in the last four months, is the Data Processing division's long-awaited 4300 series, introduced at the end of January. Discussed in industry circles for the past several months under the code name E-Series, the new computers are seen by industry analysts as only the first wave of new mainframes [*Electronics*, Feb. 1, 1979, p. 36].

Replacing the low end of the System/370 mainframe family, the new 4331 can hold up to 1 megabyte of main memory and has up to four times the instruction execution rate of the 370/115. The 4341, with up to 4 megabytes of memory, is 3.5 times faster than the 370/138. With the price of the 4331 starting at $65,000 and the basic 4341 tagged at $245,000, the estimated price/performance ratio is some three to five times better than that of the older units.

Most vendors of IBM-compatible computers say they were expecting the new machines and, even though their analyses are not complete, claim they can continue to compete effectively even with the narrowing of the margin between them and the industry giant. Key to their continued competition, however, will be their emulation of functions IBM has added to the 4300 and its systems software, much of which is in microcode. Because of this, most analysts feel these functions will not be clear until the first 4331 is delivered in the second quarter and the first 4341 is shipped in the fourth quarter.

One segment of the industry less confident about its ability to continue to compete against IBM's more aggressive pricing is the makers of add-on memories. Already, Intel Corp. says it will not pursue the 4300 add-on market.

H-Series still coming. Robert Fertig, vice president of Advanced Computer Techniques Corp., New York consultants, adds that these are only the first of the new machines the plug-compatible vendors will have to contend with. "Our technology analysis group expects two more E-Series machines later this year, the biggest of which will offer performance of a 3031 mainframe at about half the price. And of course, we expect IBM to unveil the top-end H-Series early next year."

IBM has been very vague about the inner workings of the 4300s. Though a spokesman says the 4331 has a memory read cycle time of 900 nanoseconds for 4 bytes and a write time of 1,300 ns, no processor cycle time was available. On the other hand, the spokesman says the 4341 has a processor cycle time of 150 to 300 ns, but he could not give a memory cycle time.

Up to 16 megabytes of virtual memory space is available, the same as the System/370, but the address translation scheme has changed—a

Stacking the deck. Card containing logic modules is inserted into processor motherboard. Card has four rows containing 67 edge connectors each, for a total of 268.

spokesman says the 4300 uses a "one-level addressing facility," which sounds like that used in the System/38.

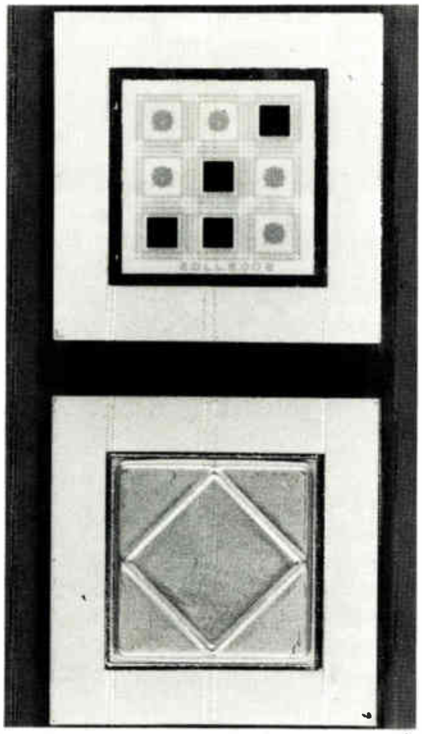
The 4300 processors are heavily microprogrammed and use a novel storage approach that places the microcode in both reloadable control store and in the processor's main memory, thus reducing the processor storage available for user programming. The 4331 has up to 128 kilobytes of control store, yet still needs 16 kilobytes of processor storage for microcode. IBM is keeping the amount of control store on the 4341 a secret, but says that model needs an additional 110 kilobytes of processor storage for microcode.

Diagnostics. One feature IBM did reveal was a separate support processor contained in the 4300s. Using its own microcode, this dedicated processor performs diagnostic routines, monitors environmental factors such as power-line conditions and temperature, and is used to provide remote diagnostic capability.

A major contributor to the price/performance improvement is new semiconductor technology such as the 64-K random-access memories introduced earlier [*Electronics*, Nov. 9, 1978, p. 39] and the new bipolar logic gate arrays (see p. 46). Although the semiconductor industry considers the IBM-developed memory and logic chips large, slow, and power-hungry, these chips offer what appear to be interesting, if not unique, solutions to the problems of designing and packaging large-scale integrated circuits and incorporating them into system designs.

For example, when the 64-K RAMs were introduced, they were thought too slow for use in mainframes, and it was pointed out that only 30% of the 1/4-inch-square chip's surface was used for memory. The 4300 reveals the kind of functions contained on the rest of the chip.

Cache is included. Two on-chip 8-bit buffers allow data to be read out at 100-ns data rates, three times faster than the typical chip access time of 300 ns. The memory increments using these chips are priced at a startling $15,000 a megabyte, a fifth of what IBM charges for memory for the rest of its mainframe line, even after the recent 30% price cut [*Electronics*, Dec. 21, 1978, p. 39].



Layers. Ceramic modules of 23 layers can interconnect nine chips for the 4331 and 4341. Modules come in two sizes, with the larger (2-in.) holding 19 by 19 pins.

The 4300 also features a new modular packaging scheme. Central to this is a 23-layer ceramic carrier that holds up to nine of the Schottky transistor-transistor-logic chips and comes in two sizes: 1 3/8 inches square with 196 pinouts or 2 inches square with a staggering 361 pins. Obviously, inserting such a package into a circuit board is tricky, so IBM first solders the logic modules to a 4 7/8-by-7 1/2-inch 8-layer circuit card, which has 268 edge connectors and is later attached to a 16-layer motherboard measuring 11 by 16 in. The resulting assembly is 6 1/2 in. high, but IBM says its modularity provides easier servicing.

Less power-hungry. Another advantage of the new components and packaging is the reduction in overall size, so that the new processors are about half as big as the older mainframes and use up to 70% less power and cooling.

In addition to the computer's circuitry, IBM has also improved its peripherals, introducing its largest disk drive—the 3370. The new drive stores 571 megabytes, twice that of the current top-of-the-line 3350 drive, and has a data transfer rate of 1.859 megabytes per second, a 55% increase over the 3350's rate. Although it is close-mouthed on its details until it ships the first one, the company does admit that the 3370 uses a read/write head "manufactured by a semiconductor process," apparently a reference to thin-film head technology. Priced with controller at $35,100, the 3370 is about half the price of the dual-spindle 3350 with equal capacity.

Piccolo calls the tune. The much discussed "piccolo" disk drive, first delivered in the General System division's System/34 last month [*Electronics*, Feb. 1, p. 36], is also included with the 4300 as the model 3310. The new drive uses an 8-in. disk medium as expected and Winchester technology heads recording at densities of 450 tracks per inch and 8,350 bits per inch. The 3310 stores a total of 64.5 megabytes on six platters and costs $12,960.

Key to getting the most performance out this hardware, however, is new software. The 4300 has two modes of operation, one to support programs from the existing System/370 computers and a so-called "native" mode that uses the new Disk Operating System/Virtual Storage Extended (DOS/VSE) software. Although IBM has continued its practice of including the basic operating system software in the price of the hardware, many of the advanced features offered under DOS/VSE require additional—and separately priced—program products. The most important of these is the VSE advanced functions package, priced at $130 a month plus $44 for maintenance, which supports up to 208 tasks and 12 partitions in a multiprogramming environment and offers what IBM calls improved "performance, usability, installation, and maintenance."

Indicative of the importance software plays in computers today, IBM has established a software support facility and is separately pricing maintenance on all its new software. It will extend the practice next year to the rest of its software, including the bundled systems software. □

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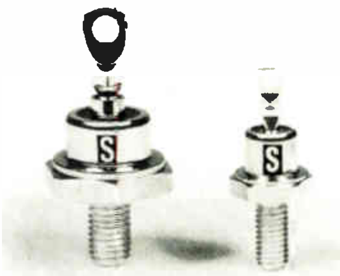

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Commentary

Testing debate enters new phase

Problems with VLSI devices require new solutions, with some compromise already beginning to take shape

by Albert F. Shackil, Instrumentation Editor

That the difficulties of testing large-scale integrated circuits has become a three-sided and seemingly unending conflict is well documented: the finger-pointing and blame-shifting of the people who make test systems, those who make circuits, and those who use the circuits has accelerated from conference to symposium to meeting.

But with very large-scale integration just down the road, testing now requires what amounts to the invention of a new art form and even more communication among three factions that have not been known for their willingness to sit down and swap information.

Fundamental to the obstacles to quick, inexpensive, and efficient tests is the nature of VLSI. Up to now, increases in density—going, say, from 7- to 5-micrometer line widths—have required merely mechanical reductions, very much like manufacturing a size 34 man's suit from a size 40 model. However, getting down to the 1- and 2-μm line widths demanded for VLSI means basic changes in design parameters; hence it also means basic changes in thinking.

There are those who think that the industry's attitude toward device testing should change from a component orientation to a system attitude. In other words, LSI and VLSI devices should not be considered components, but rather as systems that must fit in with the construction, testing, debugging, and reliability parameters associated with systems.

Walt Luciw, principal engineer for research and development of advanced circuits at Sperry Univac, Blue Bell, Pa., agrees with this approach. In fact, he goes on to suggest that chip designers implement such system-testing features as breakpoints in the routine. This, he maintains, "would permit the probing of the microinstruction logic array, arithmetic-and-logic unit, and register banks. It would certainly reduce test times."

The mention of test times brings up a major concern. In fact, it is generally accepted that the testing concept of the industry has been altered by semiconductor management philosophy that anything in a dual in-line package is a component and therefore should take no longer than 12 to 15 seconds to test. This includes the LSI and VLSI devices whose comparable off-chip systems sometimes took as long as 30 days to test, even with the numerous test points accessible to those systems.

Data wanted. Complicating the picture is the insistence of the test engineer that he should receive more

State of the art. At left is one of the newer testers for microprocessors, microcomputers, and other LSI devices, the Tektronix S-3270 automated test system.

Remembering. Shown at the right is an engineer using Teradyne's J387 memory system. It offers a feature called real-time bit mapping that displays the memory layout.

information about device design than he has been getting. But there is no reason to suspect that the device makers will supply any more design information about upcoming VLSI circuits than was sent along with LSI devices.

In general, the communication between chip designer and test engineer has been limited to the designer's giving a functional description of the part along with the critical timing specifications, leaving the test expert, as it were, to his own devices.

This disclosure debate often became the fulcrum of the early disagreements, with the testers insisting that they needed more information and the chip makers equally insistent that they were not going to disclose to the world what they considered proprietary data.

Also a factor is the belief by some device tester firms that going from LSI to VLSI will merely be another step upward, much like the one to LSI from medium-scale integration. As Gary Gillette, an engineering manager at Teradyne Inc.'s Semiconductor Test division, Woodland Hills, Calif., explains it, "Tester manufacturers have seen a continuous rise in chip density over the past 10 years, at a 60% increase in bits per year, and some prefer to think of VLSI as just another name for the latest devices with lithography in the 1-to-2-μm region."

That view, naturally, is not shared

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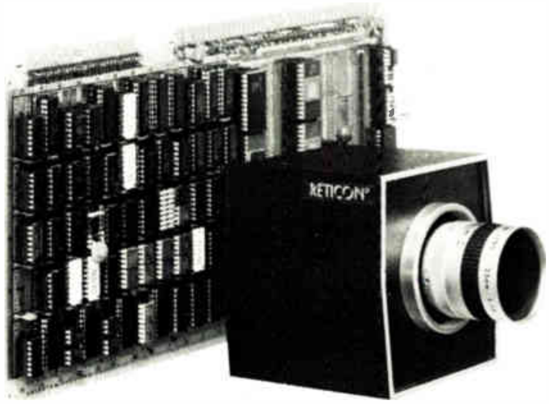

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by the chip makers. They point out that a typical LSI gate is 5 μm wide with 2-μm design rules. The figures get much smaller for VLSI, with geometries shrinking to the 2-μm stage and approaching the processing limit. Newer manufacturing processes such as electron-beam lithography are capable of forming channels in the 1-μm range with 0.1-μm design rules. This leads to the dangerous notion that VLSI testing problems will be similar to those associated with past increases in chip density.

Just what are the new problems unique to VLSI? "There are problems of device physics," says Wayne Murakami, manager of computer-aided manufacturing at National Semiconductor Corp., Santa Clara, Calif., "with the second- and third-order effects that were ignored in the past becoming very important. Device-physics problems like punch-through and trapping of holes become more evident in them."

Some changes. Clearly the attitude regarding testability at the design stage, along with feelings about supplying more data, is going to have to change. Also, attendance is increasing at special device-testing seminars such as the Institute of Electrical and Electronics Engineers' workshop on design testability coming up on April 25–26 in Boulder, Colo.

In addition to the matters of communicating chip design data and designing in testability is the economic consideration: someone will have to pay for all this.

Worth it. Here, as in the other areas, compromise is called for, one that satisifies the device maker while reducing the overall testing costs of the user. It is probably the job of the chip and system salesman to point out to their customers that, though they may be paying more for devices, they certainly stand to save time and effort on testing.

In addition, says Tom Williams, chairman of the IEEE's subcommittee on designing in testability, "it's to semiconductor houses' advantage to build it in, since an easier-testing component can sell for more."

Such a solution is not impossible—there are already several methods for providing VLSI testability without using up too much silicon, adding more pinouts to the package, or occupying too many of the existing pins. The most popular ones have parallel-in–serial-out shift registers located within feedback loops upon the chip; they enable subsections of the circuit to be accessed through the common bus and test data to be retrieved. IBM calls its version LSSD, for level-sensitive scan design; Sperry's is called scan/set, and Nippon Electric's scan/path.

Thus, progress is being made. Perhaps the best view of all the fuss comes from a computer company official who concludes that device testing is simply an evolution of know-how and that there is nothing to indicate that it will stop evolving when confronted with VLSI. □

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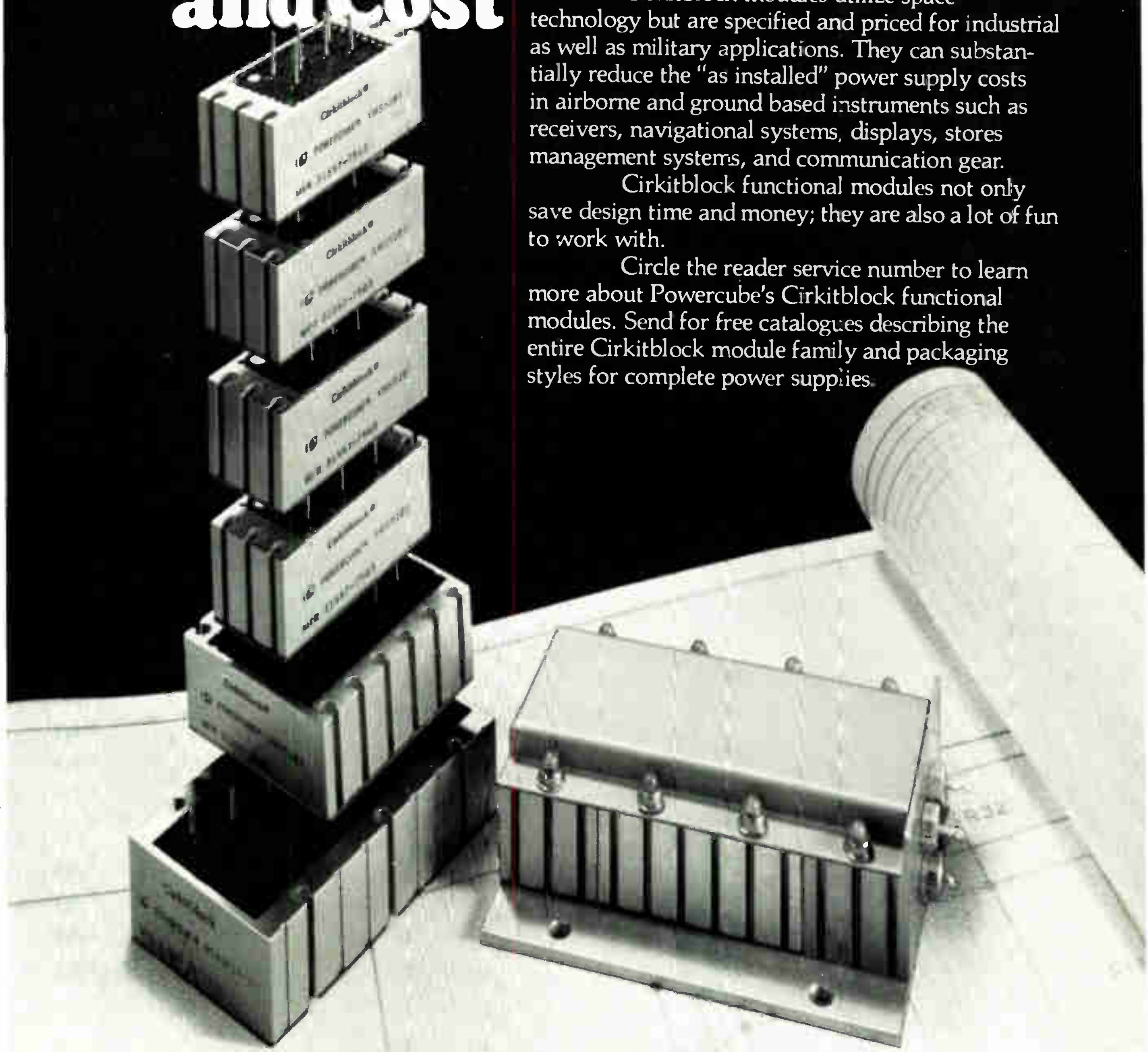

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Electronics abroad

Scandinavian markets back to normal

Sweden making a 1979 comeback to once again set the pace, while Norway, last year's leader, has an austerity program

by Arthur Erikson, Managing Editor International

There are no upstarts in view this year to upset the economic pecking order in Scandinavia.

Sweden, always at the top of the list for sheer size, has edged out of the doldrums and will set the pace for growth among the Nordic countries and perhaps for all of Western Europe as well. Denmark, the No. 2 Nordic economy, also seems set for a spurt in growth after several lackluster years. But Norway, whose North Sea oil boom kept it the pacesetter until the economy overheated last year, will fall back in line this year with a campaign for austerity and thus moderate growth.

With the dominating Swedish economy on a strong uptick, the totals for electronics markets in Scandinavia obviously figure to grow faster this year than they did last. But do not expect anything dramatic. The outlook for consumer electronics is as bleak as the landscape in Lapland and consumer electronics still is a market mainstay. So despite the respectable gains for computers and for communications equipment that turned up in *Electronics'* survey of the three countries last fall, the forecast for equipment markets in 1979 is $2.352 billion, a 7.9% gain over the 1978 total, estimated at $2.180 billion. Since the survey figures markets in current money, the nominal rise has to be looked at, because of inflation, through the wrong end of a telescope. Even so, it is a solid improvement over the gain turned in last year, when equipment markets edged up 6% from $2.056 billion for 1977.

Components markets, in contrast, will rise much the same as they did in 1978. They will hit $556 million, up 3.5% over the estimated $537 million for last year. The only sector anything close to comfortable is integrated circuits, pegged to climb from $67 million last year to $73 million this year. That works out to a near-9% increase, not enough to excite anyone in the IC business.

Sweden. After two years in the doldrums, the Swedish economy now has brisk winds blowing behind it. The country's economy watchers, almost to a man, expect 1979 will be one of the best years of the decade as far as growth goes. In the draft budget for the upcoming fiscal year, for example, the government has postulated a growth of 5.4%. If that is right, Sweden will have the highest growth rate in all Western Europe.

The brisker economy will buoy equipment markets—entertainment electronics excepted. The forecast puts 1979 markets at $1.205 billion. That means a 9% rise, if the forecast is close to the mark, from the estimated $1.105 billion for 1978.

Swedish communications-equipment makers presumably can count on a solid home market during the next 12 months. The markets chart posts the sector at $209 million, a full 15% over the $181 million estimated for 1978. Spending for defense equipment will stay on its plateau, a fairly high one. But there is a lift in store from Televerket, the state communications agency. Televerket this year will get its first substantial deliveries of AXE stored-program-control exchange equipment from L M Ericsson Telephone Co., for one thing. Other ambitious projects under way that will link subscribers in Stockholm, Copenhagen, Oslo, and Helsinki, and the

SCANDINAVIAN ELECTRONICS MARKETS FORECAST
(IN MILLIONS OF DOLLARS)

	1977	1978	1979
Total assembled equipment	2,056	2,180	2,352
Consumer electronics	815	802	818
Communications equipment	391	435	484
Computers and related hardware	554	626	703
Industrial electronics	147	156	175
Medical electronics	72	75	78
Test and measurement equipment	51	57	62
Power supplies	26	29	32
Total components	518	537	556
Passive and electromechanical	309	321	331
Discrete semiconductors	61	60	60
Integrated circuits	59	67	73
Tubes	89	89	92

(Exchange rates: Denmark, $1 = 5.3 kroner; Norway, $1 = 5.1 kroner; Sweden, $1 = 4.4 krona)

Note: Estimates in this chart are consensus estimates of consumption of electronic equipment obtained from an *Electronics* survey made in September and October 1978. Domestic hardware is valued at factory sales, prices and imports at landed costs.

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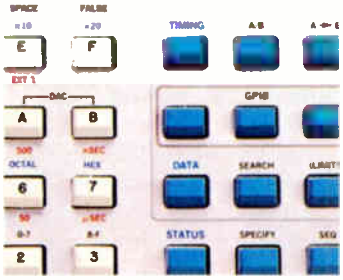

It starts with the microprocessor-controlled keyboard and interactive video display. To give you fast, precise control, the display serves as a comprehensive control status menu, with all selectable parameters in reverse video. There's a single, labelled key for each function, corresponding directly to status display choices. So guesswork is eliminated.

For example, in the data domain, you can direct the display to read in hexadecimal, octal, binary or ASCII, or any combination, by selecting one of four control buttons. There's also a unique "sequence" key that enables you to rearrange the order in which channels are displayed, to aid in data decoding, to simplify side-by-side comparison of timing signals and to enable you to cancel any channels you're not interested in seeing. A separate key controls horizontal expansion.

That gives you an idea of the K100-D's display versatility. Here's a picture of its astounding capture capability.

By providing timing analysis of signals as fast as 100 MHz, you can capture logic signals with resolution to 10ns. And the 100 MHz clock rate protects against obsolescence as the speed of your systems gets faster and faster. The K100-D also has a latch mode that can capture glitches as narrow as 5ns.

With the 32-channel input adapter, the K100-D is ideal for exploring the new world of 16-bit microprocessors. To give you unprecedented analysis capability, there's a built-in Auto Stop capability you can use to detect, record and display any match (or mismatch) between incoming data and previously recorded data held in a reference memory. Or using Search Mode you can key in a specific word and the K100-D will find it in memory.

To get the full impact of the K100-D, you really do need to have it at your fingertips. That's why we would like to arrange a demonstration. Call us at (408) 988-6800. Or, for more information, write: Gould Inc., Biomation Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050.

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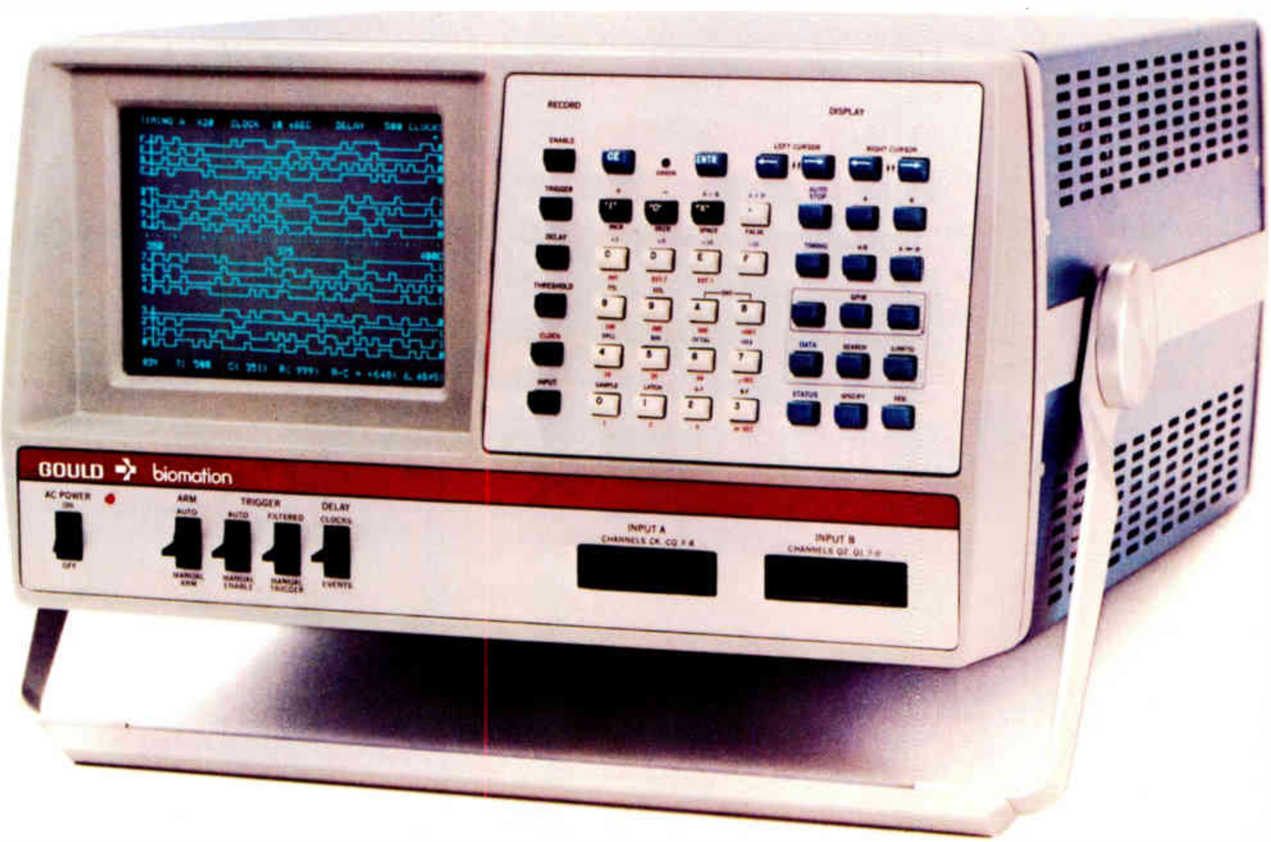

nationwide paging network that started up late last year [*Electronics*, Jan. 4, p. 67].

Computer makers should do all right, too. The forecast for the sector—data-processing equipment and electronic office equipment—puts the market at just under $380 million, up 12% from the 1978 figure of $338 million.

Meanwhile, the country's TV set-makers face immediate and more pressing problems. There is no growth in sight for color-TV sales and nothing yet in sight to spark the market as color-TV once did. So consumer electronics sales will edge up only to $437 million this year from 1978's $421 million.

The two major set makers—Svenska Philips AB, a unit of the Dutch-based Philips' Gloeilampenfabrieken group, and family-owned Luxor Industri AB—are both feeling the pinch. But Luxor has been hit particularly hard. The company, whose sales last year ran about $110 million, tried to cope with the slope in the home market by emphasizing exports. But sales did not match the high costs involved and Luxor lost last year some $20 million and recently recast top management.

And as go the set makers, so to a large extent go most component suppliers. The survey suggests only a modest rise in sales this year to $340 million from last year's $329 million. The 1979 figure may turn out low; the Swedish industry association, noting "definite optimism" among its 120 member companies, says component sales are up sharply over last year, which was poor. Microprocessor sales certainly will bulge. Products designed around them during the slow years of 1977 and 1978—from hi-fi receivers to forestry machines—will spill into the marketplace this year.

Denmark. Like their neighbors on the far side of the Kattegat, the Danes foresee better business ahead. After a nearly invisible expansion of 1% last year, the country's Gross Domestic Product (GDP) could grow something like a perceptible 2.5% this year. Anyway, that is the reading by economists at the Organization for Economic Cooperation and Development (GECD), the Paris-based international organization.

Just as important, the Danes hope to whittle down their foreign trade deficit, which has been the traditional bane of their economy. They managed to cut it back by nearly 17% to $3 billion last year and could do even better in 1979. How much better depends mainly on what kind of wage rise the unions will settle for in upcoming negotiations with employers. Another plus for the year ahead is a rise of 3% in investments.

Unfortunately, these improved prospects for the economy overall will do little to stimulate consumer spending. What is more, the satura-

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tion level for color-TV sets is approaching 60% and sales of sets—figured in money or in units—are slipping. The survey forecasts consumer electronics markets this year will run slightly below the $245 million estimated for 1978. And when there is no lift in consumer electronics, there is no chance for a substantial rise for equipment markets as a whole. Despite a strong gain for computers, the No. 2 sector, the forecast is $648 million, a hike of 6% over 1978.

As always, Danish electronics hardware producers count more on exports than their home market. The country's 200-odd firms prospered last year and generally see more of the same as they peddle their specialties around the world [*Electronics*, Nov. 9, p. 86].

Norway. Although they did not take to wearing 10-gallon hats, the men who govern Norway did let their North Sea oil bonanza go to their heads. To keep their economy headed up despite the general slowdown around the world, the Norwegians spent oil revenues before they came in and thus acquired a dangerous payments deficit along with an overheated economy. Not only did the forced prosperity suck in imports, it also pushed wages to levels where Norwegian workers were the highest paid anywhere, making many Norwegian products uncompetitive in world markets.

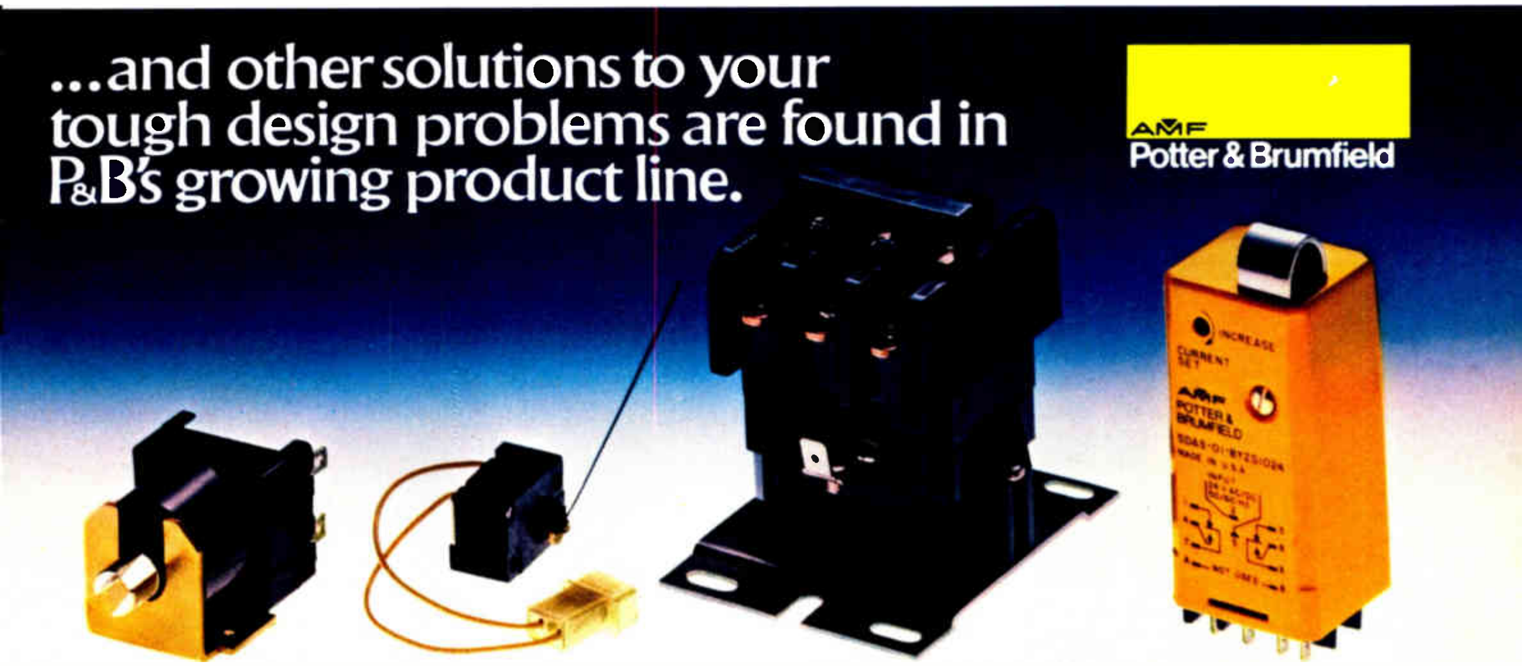
The government slammed on the brakes late last summer with a freeze on prices and wages that is going to last through 1979. So it is not particularly surprising to learn that the growth in GDP will fall sharply—from a rise of 3.75% in 1978 to only 2.5% this year in the view of OECD's forecasters.

It is no surprise, either, that this year Norway's electronic equipment markets won't outpace the others in Scandinavia as they did in 1978. They grew some 9% then to reach $464 million. This year they will move up about 7% to just under $500 million. As in Sweden and Denmark, consumer electronics is no-growth and the gain comes mainly from computers and from communications equipment.

As for components suppliers, their prospects have been lowered several notches by the bankruptcy of Tandbergs Radiofabrikk A/S. Taken over by the government last year, it will stay in the computer terminal business [*Electronics*, Jan. 4, p. 63], but it won't consume components the way it did when it was the sole Norwegian producer of TV sets.

When *Electronics* surveyed the market last fall there was a chance that Tandberg would carry on, and the forecast was $71 million in components sales. With Tandberg out of the television production picture, the figure this year will fall well below that. □

Last in a series examining European markets. Robert Skole in Sweden, Alfred Petersen in Denmark, and Ottar Odland in Norway reported for this article.



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Software

Pascal people unhappy over standard

ANSI, BSI, ISO, and even IEEE are in the act as attempts to settle differences between academicians and industrial users are unavailing

by John G. Posa, Microsystems and Software Editor

When the American National Standards Institute sponsored an organizational gathering in Washington, D. C., late in December of its X3J9 subcommittee to standardize the programming language Pascal, it probably expected to make some headway. But, as with some other recent Pascal gatherings, progress at the ANSI meeting was minimal. "We agreed only to have another meeting on Feb. 20," says Joe Cointment, Texas Instruments' representative, "We didn't even elect a chairman."

As that meeting nears, a number of issues are turning attempts to arrive at a Pascal standard into a real headache, one that would bring tears to the eyes of Blaise Pascal, for whom the language is named. One problem is that a number of groups claim to be working on a standard already. Worse still, academic factions maintain that the standard should incorporate only the ideas presented by the language's author, Niklaus Wirth, in his revised Pascal Report—without any major alterations. Industrial users contend that modifications and extensions to the language are so essential that they should be embodied in the standard from the outset.

Finally, there is the question of whether language standards make sense at all. While the proponents maintain that it is necessary and would be fruitful for all Pascal machines and users to be able to communicate, particularly since the language has enjoyed a phenomenal growth in the last few years [*Electronics*, Oct. 12, 1978, p. 81], opponents of the idea would just as soon go their own proprietary ways.

In Europe, progress toward standards has been made for almost two years. A subcommittee of the British Standards Institute called DPS/13/4 first met in Southampton in the spring of 1977. Headed by Tony Addyman of the University of Manchester, this group is still going strong and is backed in the U. S. by the Pascal Users' Group (PUG), based at the University of Minnesota. In the spring of 1978, a working draft for a Pascal standard was given to the International Standards Organization (ISO).

"There was a choice whether to go to ANSI or ISO," says Richard Cichelli, a founder of PUG. "It was decided at Southampton, and every group since has concurred, that ANSI presents significant problems. We wanted only to standardize the language in the report. We don't want to design a new language."

Parallel to the European standards effort, PUG established a working group in June 1976 to consider extensions to Pascal. Now coordinated by Andy Mickel, who also edits PUG's Pascal News quarterly, this group comprises virtually every major implementer around the world, including Wirth himself. PUG was satisfied. There was a group for a standard and a group for extensions. The standard, which the ISO will most likely still adopt, is very close to the language in Wirth's revised report.

But since then, Pascal has become enormously popular, and it seems everybody wants a piece of the action. Kenneth Bowles, a professor at the University of California at San Diego, put together a Pascal system to run on a wide variety of microprocessors. He began quietly to blanket the country with his system, in the hope that it would become a *de facto* standard, and in July 1978 held a workshop to discuss extensions to Pascal. "But it was all about standards," says TI's Cointment.

Some believe that ANSI wants to undermine the British effort—to change Pascal to make sure it is not compatible with ISO's standard. But that's not so, says Justin Walker, a National Bureau of Standards mathematician who convened the ANSI meeting. "There's a good chance we will vote in the British standard," he says. "We first have to get all the groups and interests together and start going in the same direction."

One of those groups is the IEEE. It decided at the ANSI meeting that it should draft a standard of its own, so it met in San Francisco in January to do that. Says ANSI's Walker, "We're trying to set an agreement whereby ANSI and the IEEE can work together, even though we're starting out differently." □

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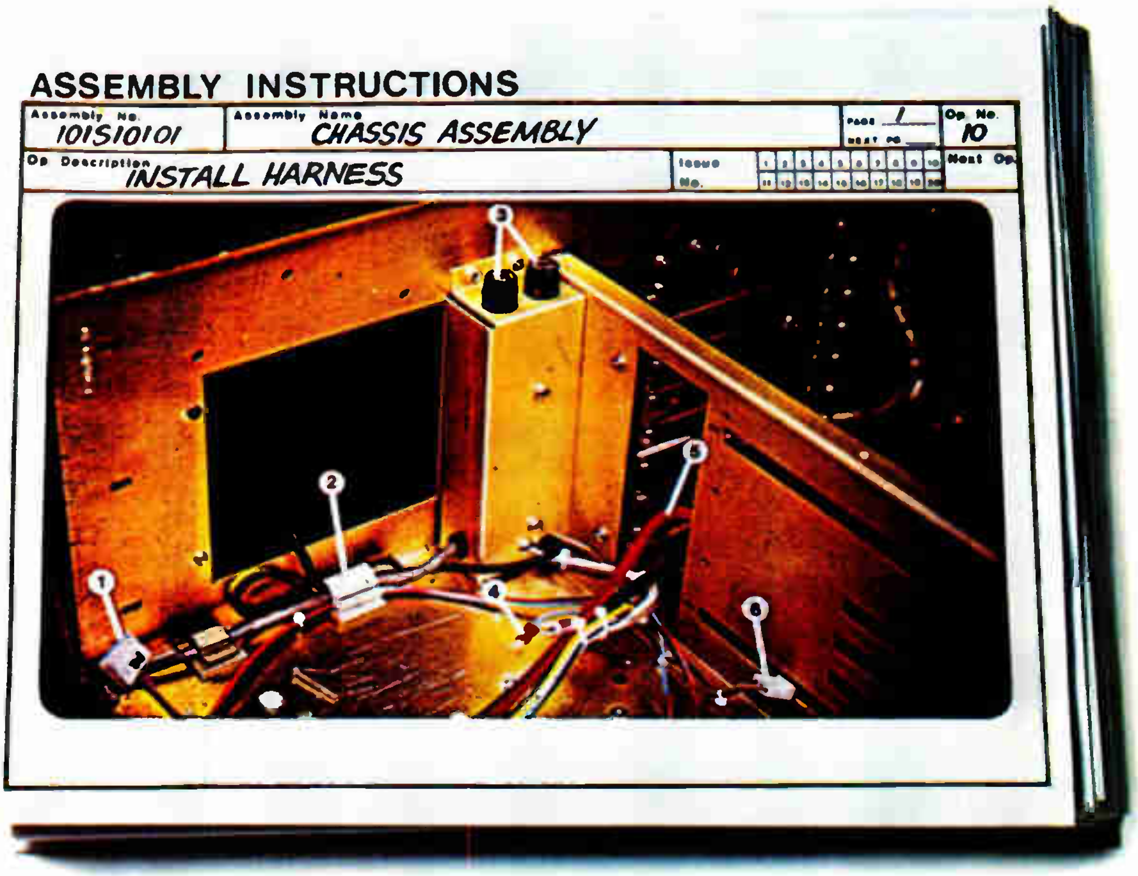

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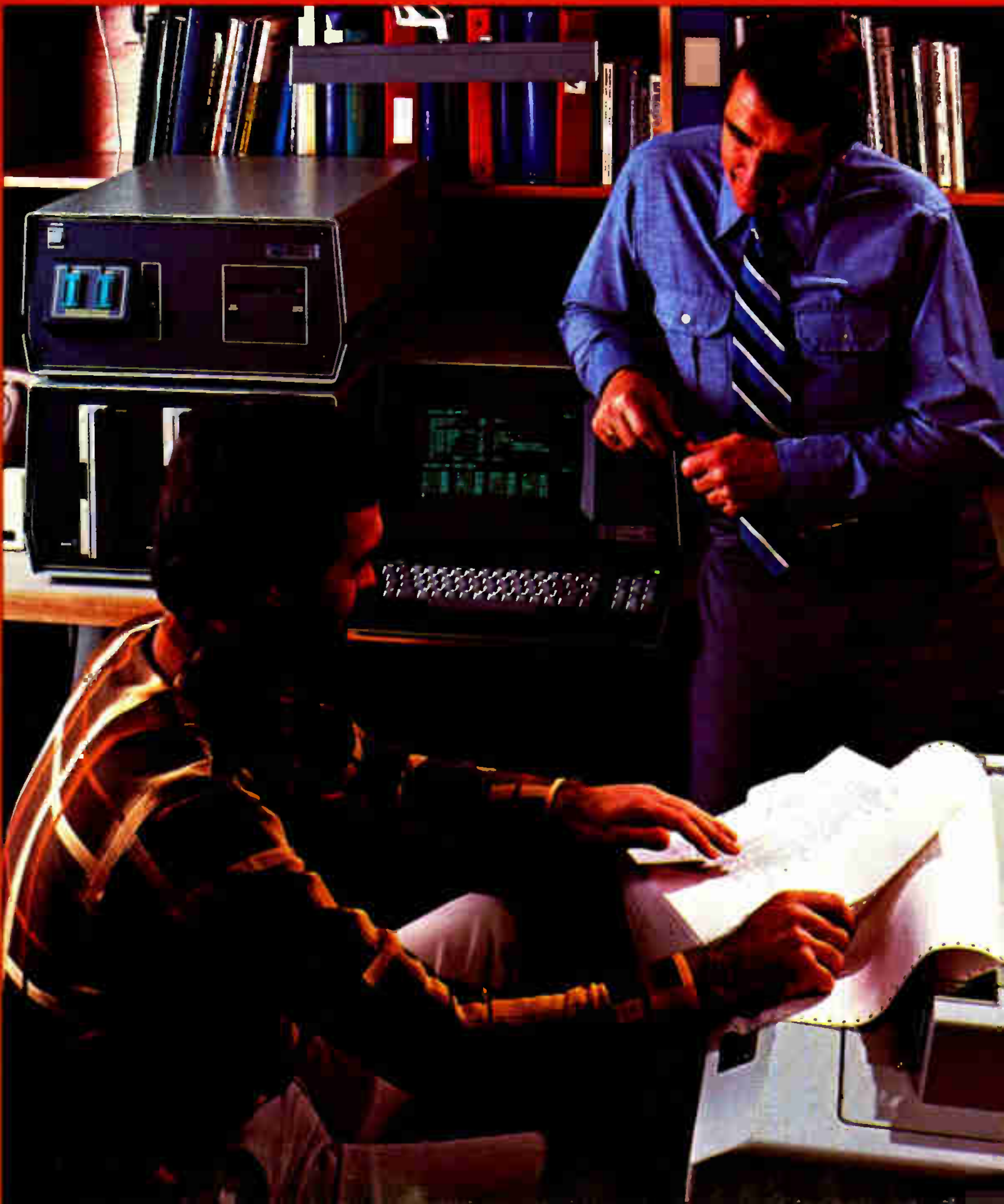

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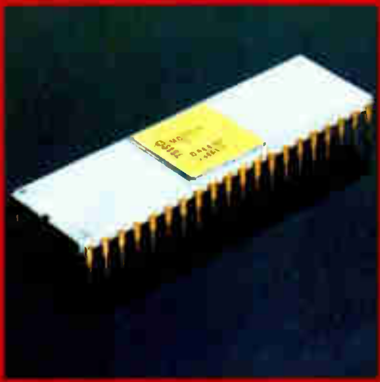

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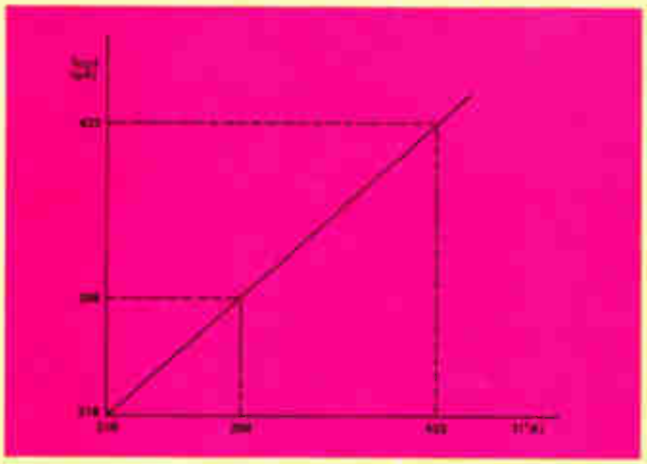

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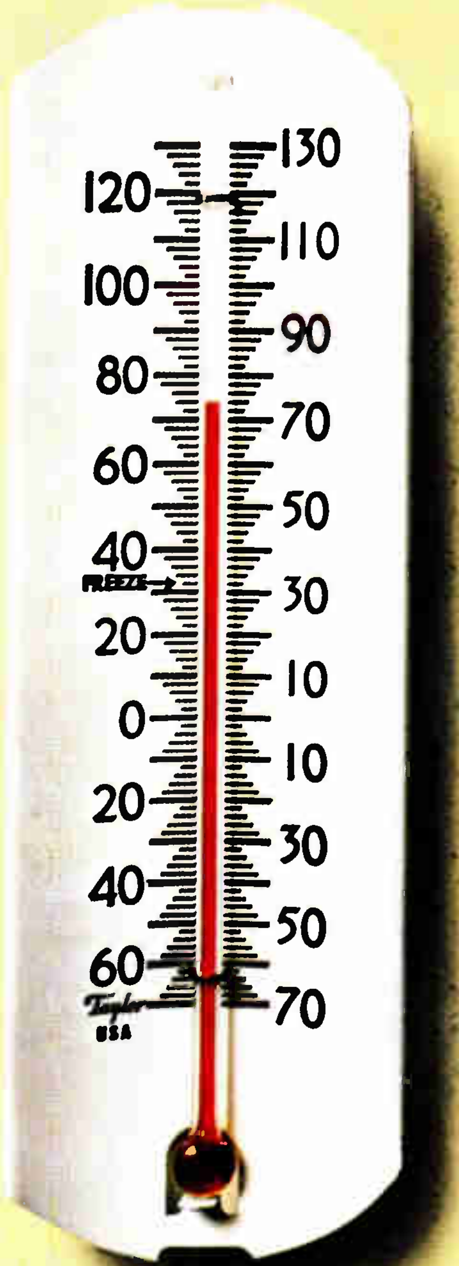

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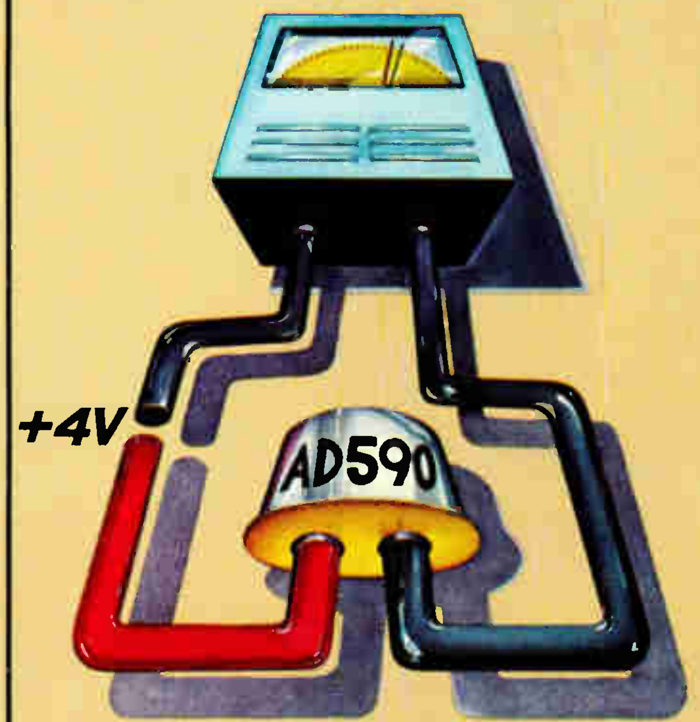

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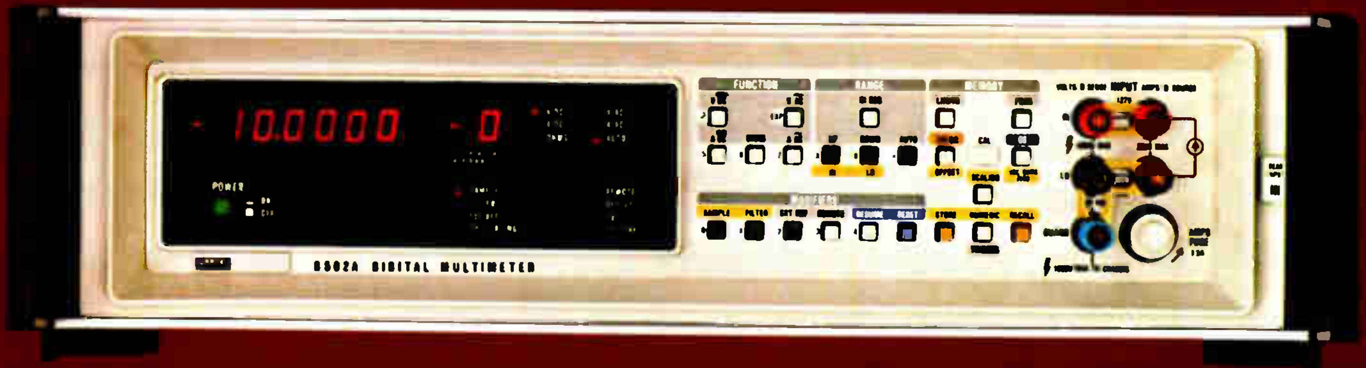

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Circle 105 for demonstration

Touch-tone decoder chip mates analog filters with digital logic

Switched-capacitor filter design builds 40 poles of bandpass, bandstop, and bandsplit filtering with TTL-compatible outputs on complementary-MOS chip

by G.M. Jacobs, G.F. Landsburg, and B.J. White,
Silicon Systems Inc., Irvine, Calif.
and D.A. Hodges,
University of California, Berkeley, Department of Electrical Engineering

☐ Analog-digital large-scale integration is coming to life with the aid of the switched-capacitor filter—a monolithic precision active filter that can be fabricated with any of several standard metal-oxide-semiconductor processes. The addition of this component to the MOS arsenal, which already includes analog-to-digital and d-a converters, stable voltage references, and high-resolution offset-nulled comparators, gives the IC designer virtually all elements of analog signal-processing systems in the same high-density, high-performance technologies that have captured digital large-scale integration.

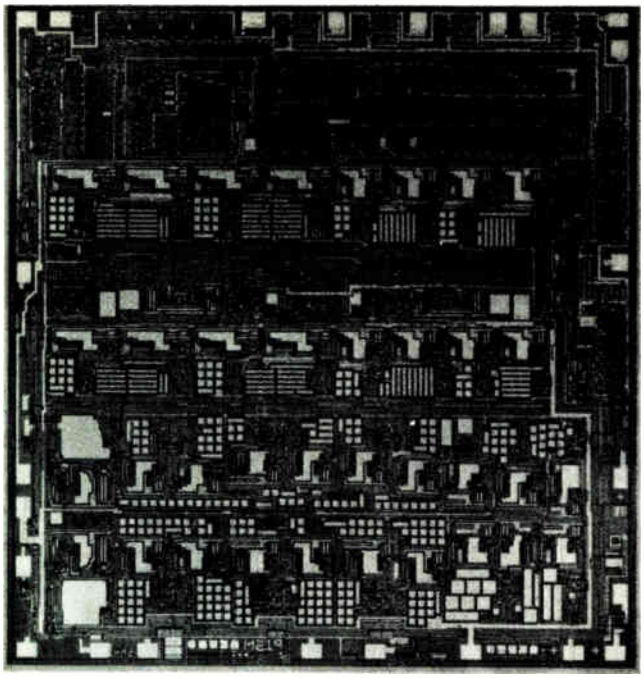
Demonstrating the power of the switched-capacitor technique in realizing analog-digital LSI is Silicon System's 201 dual-tone multifrequency (DTMF) receiver for decoding Touch-tone telephone numbers (see "The DTMF receiver chip," p. 109). For the first time, one 40,000-square-mil complementary-MOS chip combines a variety of analog and digital functional blocks to efficiently perform a historically cumbersome telecommunications operation. Included are high-Q bandpass filters, sixth-order bandstop filters, comparators, and special-purpose analog circuits, as well as extensive digital logic (Fig. 1). The only outboard components needed are two noncritical capacitors and a 3.58-megahertz crystal—the type found in all color-television receivers.

Filter approaches

The DTMF receiver, like many other analog systems, requires precision filters—and that usually means precision components. Passive filters could be built with discrete inductors and capacitors, or precision resistors and capacitors combined with operational amplifiers for active designs—but in either case dozens of precision devices are required. More easily manufactured approaches have evolved, one of the first of which was hybrid circuits.

Hybrid active RC filters are built by depositing thin- or thick-film resistors on a ceramic or glass substrate and attaching chip capacitors and integrated-circuit amplifier chips. For a DTMF receiver, dozens of connections must be made between all the R, C, and amplifier elements. Finally, to achieve exact frequency response each filter stage is anodized or laser-trimmed. But little can be done to trim the cost of hybrids; their fate is usually replacement with lower-cost monolithic circuits when technology permits.

Charge-coupled-device (CCD) filters can often meet tight specifications for frequency response, but have certain limitations that have delayed their development in commercial form. Aside from the fact that advanced fabrication processes like double-polysilicon-gate MOS structures are required for building CCDs with good



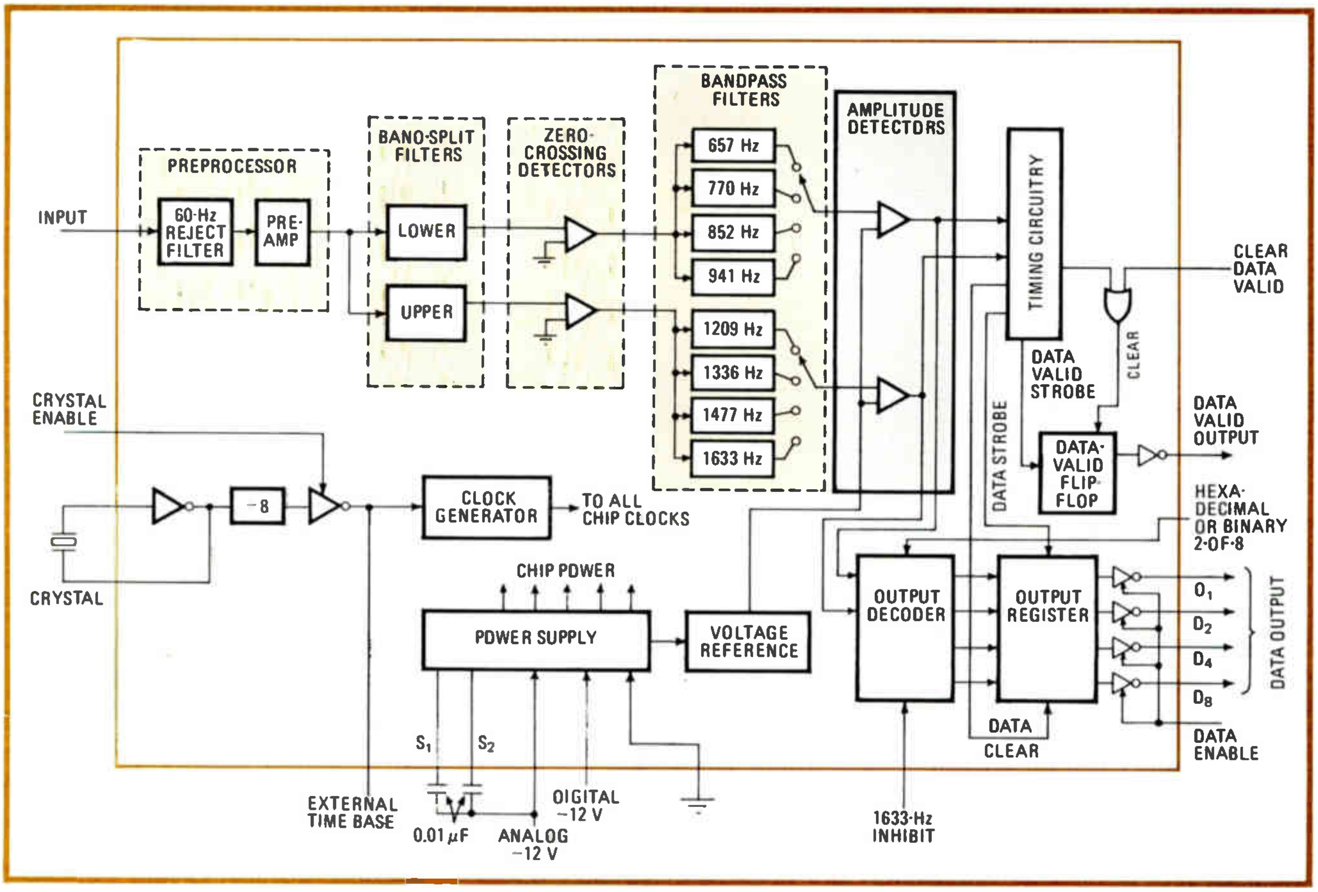
Analog meets digital. Integrated on a C-MOS chip is a complete dual-tone multifrequency receiver that performs central-office quality Touch-tone decoding. Twenty percent of the 210-by-220-mil device is digital logic, while the other 80% comprises 40 poles of precision analog filters that need no trimming. Power dissipation is typically 350 milliwatts from a 12-volt supply.

characteristics, thermally generated leakage currents and the excessive areas of silicon required limit CCD filters to a lowest center frequency of about 1 kHz. Moreover, minimizing distortion by raising the sampling rate can drive the number of CCD stages excessively high. Finally, the split-electrode transversal filter configuration usually used with CCDs yields a filter with substantial insertion loss even for frequencies in the pass band, making a good signal-to-noise ratio difficult to achieve with CCD filters. Only in certain applications—time-domain matched filters, for example—are CCD approaches attractive.

Wholly digital filtering techniques that employ only logic and memory elements might be preferable to analog methods in many applications—especially where programmability of the response is desirable. The fact is, however, that both chip area and power consumption for digital filters are still prohibitively large. For functions like the DTMF receiver, which requires fixed precision filters and which is slated for high-volume production, the driving forces are minimal chip size and easy integration that requires no trimming or special processing.

Enter switched-capacitor filters

Since inductors cannot be integrated practically, active filters built around RC networks seemed the best approach. But the longest RC time constant possible with the usual on-chip resistors and capacitors is 10 microseconds at best—too brief for filters in the audio



1. One-chip DTMF receiver. All the circuits for a dual-tone multifrequency receiver, which requires high-pass, high-Q bandpass, and bandsplit filters, in addition to extensive digital logic, are integrated with second- and third-order switched-capacitor filters on one chip.

The DTMF receiver chip

The analog circuits in Silicon Systems Inc.'s 201 dual-tone multifrequency receiver occupy approximately 80% of chip area, the digital circuits 20%. The die, packaged in a 22-pin DIP, measures 210 by 220 mils and uses very conservative design rules: minimum metal width is 7.5 micrometers in the standard metal-gate C-MOS process used. Power dissipation is typically 350 milliwatts from a 12-volt supply. Digital outputs and inputs are transistor-transistor-logic–compatible; outputs are either binary-coded 2-out-of-8 or hexadecimal; and handshake capabilities simplify interfacing with the external system.

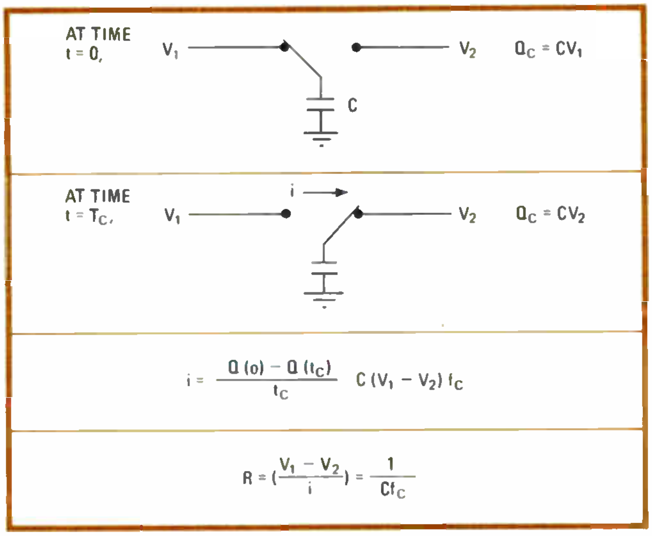
In addition to the 40 poles of switched-capacitor filtering, several other circuit functions are required to form the complete DTMF receiver. Digital functions are realized with standard C-MOS circuits. Zero-crossing detector/limiter circuits are ac-coupled comparators that supply square-wave outputs to the bandpass filters. The purity and frequency of an incoming tone is measured by comparing the peak signals at the detector/limiter outputs with the peak signals at the filter outputs. If there is interference or if the incoming signal is not a valid frequency, no bandpass filter will have an output that exceeds the threshold established by the peak detectors and thus no valid tone will be detected.

SPECIFICATIONS FOR DUAL-TONE MULTIFREQUENCY RECEIVER

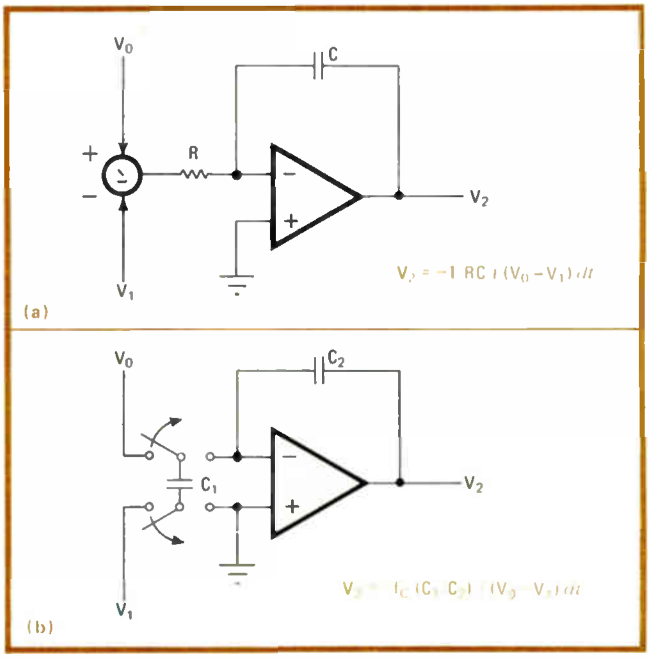
Supply voltage	10 to 13 volts
Operating temperature	0 to 70°C
System clock	Internal: 3.58-MHz crystal External: 448-kHz input

Receiver performance

Specification	Must accept	Must reject
Low-frequency bandwidth (697, 770, 852, 941 Hz)	± (1.5% + 2 Hz)	± 3%
High-frequency bandwidth (1209, 1336, 1477, 1633 Hz)	± (1.5% + 2 Hz)	± 3%
Minimum amplitude (each frequency)	−24 dBm at 600 Ω (53 mV rms)	–
Maximum amplitude (each frequency)	+ 6 dBm at 600 Ω (1.3 V rms)	–
Twist (high ÷ low)	+ 4 dB to − 8 dB	–
Tone-valid time	⩾ 40 ms	⩽ 12 ms
Pause time	⩾ 40 ms	⩽ 12 ms
Talk-off performance	⩽ 2 hits on Mitel test tape (CM7290) (typical)	
60-Hz tolerance	2 V rms	
Outputs	three-state, binary 2 of 8, or hexadecimal	



2. R from C. Switching a capacitor between two nodes simulates a resistor whose value depends only on the capacitor value and the switching frequency. This switched-capacitor technique allows the integration of precision filters on the DTMF chip.



3. Integrator. In a modification of standard integrator (a), C_1 of the differential switched-capacitor integrator (b) first charges to the difference between the two input voltages, then transfers the charge to C_2. The periodic transfer of charge appears as a current flow.

band, which require time constants as long as 100 milliseconds. In standard IC technologies, the readily attainable capacitance ranges from about 1 picofarad to 100 pF, and the smaller values obviously are preferable since they take up less chip area. To achieve the desired time constant, resistors of from 10 to 10,000 megohms are needed; but none can be diffused, implanted, or deposited with the kind of accuracy and stability required.

In 1976, at about the same time, researchers at the University of California at Berkeley and at Bell-Northern Research in Ottawa recognized that a small capacitor switched rapidly could simulate a high-value resistor.[1,2] The basic scheme and design equations are given in Fig. 2; as shown, the resulting derivation yields a simulated resistor whose value depends only on the capacitance and the switching frequency.

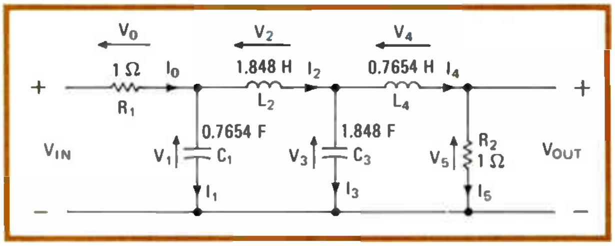
The scheme lends itself well to integrated circuits: switches are easily implemented with small MOS transistors; signal voltages can be sensed with FET-input amplifiers; and operational amplifiers in n-channel MOS and

Designing a switched-capacitor filter

With a little active filter theory and some classical LC design tables, the task of designing a switched capacitor filter becomes quite simple. The most popular designs implemented with switched-capacitor filters are the classical LC ladders, which are not only well documented,[1,2,3] but are inherently insensitive to variations in component values. Thus, LC ladder filters yield a highly accurate frequency response despite wide tolerances on capacitors. In this section, the design of a low-pass ladder will be presented in detail.

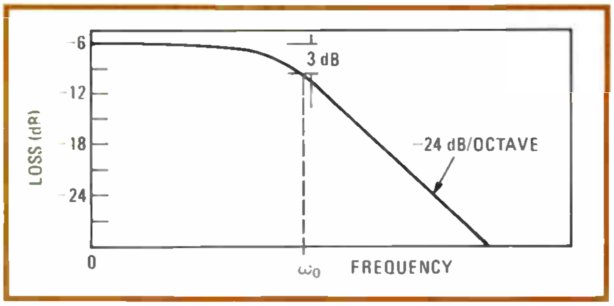
The active simulation of an LC ladder filter is done with state-variable techniques. The active-ladder (or "leapfrog") configuration was first presented by Girling and Good ("The Leapfrog or Active Ladder Synthesis," Wireless World, July 1970). This configuration models the state variables of the LC ladder exactly, and thus maintains the same sensitivity characteristics as the passive LC prototype.[4] Consider as an example the doubly terminated four-pole LC ladder below:

(a)



The Butterworth approximation is chosen. The normalized component values given in the table are taken from a catalog of standard filter approximations of which many are in print. The response will be flat in the passband starting at dc and will roll off to 3 dB down at the cutoff frequency ω_0. The loss through the filter increases at 24 dB/octave after yielding the low-pass characteristic as shown below. The dc gain is −6 dB due to the R_2–R_1 divider.

(b)

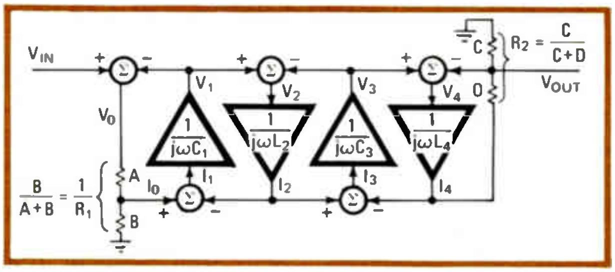


Referring back to (a), a set of equations can be generated using Kirchoff's voltage and current laws:

$$V_0 = V_{IN} - V_1 \qquad V_3 = I_3(1/j\omega C_3)$$
$$I_0 = (V_{IN} - V_1)/R_1 \qquad V_4 = V_3 - V_5$$
$$I_1 = I_0 - I_2 \qquad I_4 = V_4(1/j\omega L_4)$$
$$V_1 = I_1(1/j\omega C_1) \qquad I_5 = I_4$$
$$V_2 = V_1 - V_3 \qquad V_5 = I_5 R_2$$
$$I_2 = V_2(1/j\omega L_2) \qquad V_{OUT} = V_5$$
$$I_3 = I_2 - I_4$$

These equations completely describe the operation of the passive LC ladder and are all written describing the relationship between voltage and current of any energy-storing element as an integration. The symbolic representation of the equations shows integrators as triangles and summers as circles.

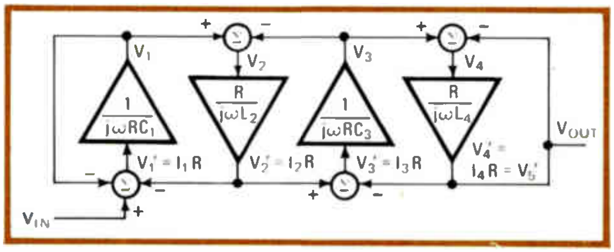
(c)



The symbolic representation of the LC prototype is now taking form as a circuit schematic. The integrators can be implemented with switched-capacitors as explained earlier.

Several scaling procedures are still necessary to make the circuit practical for building. Since the operational amplifiers used for integrators respond to voltages, the currents must be converted to voltages by scaling with an arbitrary resistance, R. For simplicity, the termination resistors R_1 and R_2 are each set to 1. The scaled version is thus:

(d)

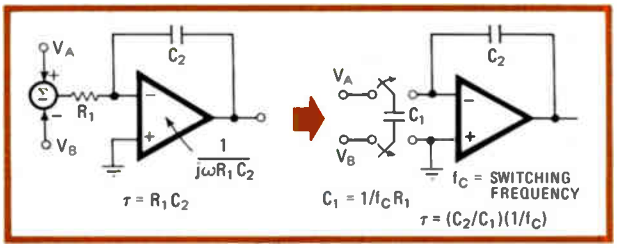


The integrators now have traditional RC or R/L time constants. A differential switched-capacitor integrator has the advantage of easily implementing the integrator and

C-MOS technologies have already been demonstrated. For the first time, RC filters with a wide range of center frequencies can be built on a chip that replaces the resistors with switched capacitors. But perhaps the biggest advantage of the switched-capacitor approach is that the accuracy and stability of equivalent RC products are determined only by capacitance ratios and switching frequency—and overall accuracy of within a few tenths of one percent can be achieved without trimming or adjustments.

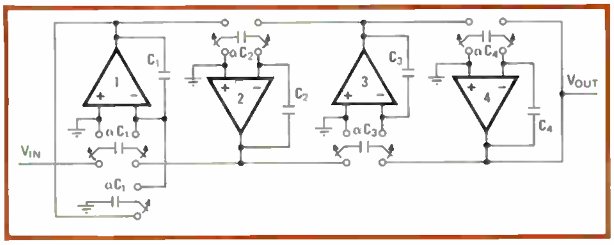
The simple equivalence between a switched capacitor and a resistor holds true only for switching frequencies summing function at each stage shown above. The analogy is shown below:

(e)



The complete ladder implemented with switched-capacitor integrators looks like:

(f)



Although the switched capacitors are being clocked at a much higher frequency than the signals passing through the filter, they have a significant time delay. The delay through a switched-capacitor integrator translates into an unwanted phase component or loss in each integrator. Therefore, for proper operation of the ladder, the switches (MOS transistors in integrated form) on adjacent integrators must be clocked as shown by the arrows in the figure.

When the output of integrator 1 changes (switches up), for example, integrator 2 is picking up that change on C_2, thus minimizing the delay. When clocked that way, the effects of switching are negligible as long as the clock is at a sufficiently high frequency to avoid anti-aliasing or foldover distortion common to any sampled data system.

To complete the example design, actual capacitance values must be calculated for a specific frequency response. For the same Butterworth prototype, a cutoff frequency is assumed of, say, 1 kHz (ω = 6,283.2 radians/second) and a clock frequency of 40 kHz. (Input signals are thus bandlimited to 20 kHz.) For a 1-kHz f_o, the prototype in (b) must be scaled down by 2π (1 kHz). In addition, the arbitrary scaling resistance is given the value of 1 Ω. The time constants of the switched-capacitor integrators are then simply the L and C values from the prototype ladder. Each time constant is $C_2/C_1\ f_c$ as shown in the figure. Therefore, the capacitor ratios necessary to implement the Butterworth filter at 1 kHz are calculated to be:

Integrator 1 (C_1)	$\frac{0.7654}{2\pi(1\text{ kHz})} = \frac{C_1}{\alpha C_1}\,\frac{1}{40\text{ kHz}} \Rightarrow \frac{C_1}{\alpha C_1} = 4.87$
Integrator 2 (L_2)	$\frac{1.848}{2\pi(1\text{ kHz})} = \frac{C_2}{\alpha C_2}\,\frac{1}{40\text{ kHz}} \Rightarrow \frac{C_2}{\alpha C_2} = 11.76$
Integrator 3 (C_3)	$\frac{1.848}{2\pi(1\text{ kHz})} = \frac{C_3}{\alpha C_3}\,\frac{1}{40\text{ kHz}} \Rightarrow \frac{C_3}{\alpha C_3} = 11.76$
Integrator 4 (L_4)	$\frac{0.7654}{2\pi(1\text{ kHz})} = \frac{C_4}{\alpha C_4}\,\frac{1}{40\text{ kHz}} \Rightarrow \frac{C_4}{\alpha C_4} = 4.87$

The ratios completely define the frequency response for a given clock frequency. (Also, for given ratios, the response will shift directly with f_c.) In integrated form, for a ratio of 10, the two capacitors might be chosen at 1 pF and 10 pF to keep the area small. For a discrete version, the same frequency response would be realized using 100 pF and 1,000 pF. Since the only variables are the clock frequencies and capacitance ratios, extremely high accuracy is achievable as well as insensitivity to aging, temperature, and other environmental effects. In most applications requiring a fixed frequency response, a crystal-controlled clock generates the frequency reference.

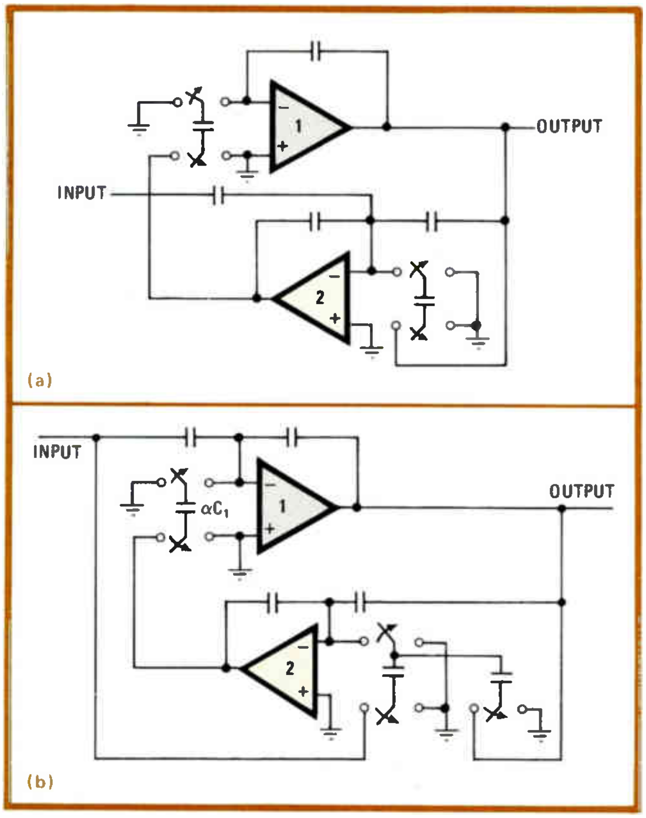
References

1. D. J. Allstot, R. W. Brodersen, and P. R. Gray, "Fully integrable high order NMOS Sampled Data Ladder Filters," ISSCC, San Francisco, Feb. 1978.
2. G. M. Jacobs, D. J. Allstot, R. W. Brodersen, and P. R. Gray, "Design techniques for MOS switched capacitor ladder filters," IEEE Trans. on Circuit and Systems, Dec. 1978.
3. D. J. Allstot, R. W. Brodersen and, P. R. Gray, "MOS switched capacitor ladder filters," IEEE Journal of Solid-State Circuits, Dec. 1978.
4. H. J. Orchard, "Inductorless Filters," Electronic Letters, Vol. 2, June 1976, pp. 224-225.

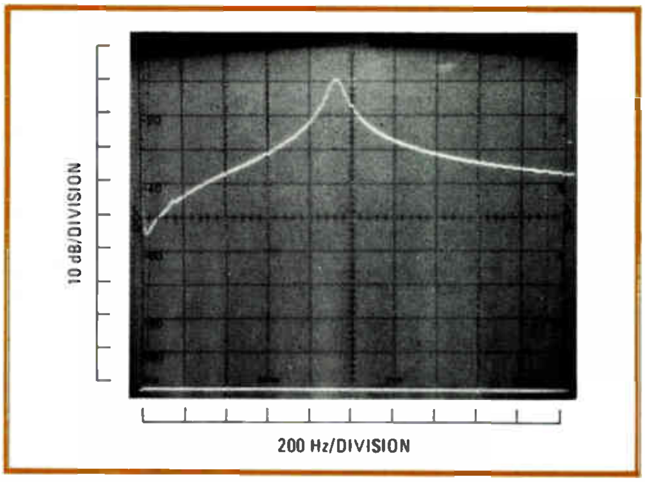
that are higher than the highest frequency being filtered. Since practical clock frequencies for audio-frequency filters are in the range of 50 to 500 kHz, exact design of switched-capacitor filters requires Z-transform analysis, as is true of all sampled-data circuits. Fortunately, digital filter computer programs such as Dinap (developed by Steven Bass and colleagues at Purdue University) can be used for simulating switched-capacitor filters operating at any sampling frequency. One concern worth mentioning here, however, is that input-signal frequency must not exceed half the sampling frequency to avoid fold-over or aliasing distortion, as predicted by the Nyquist theorem.

The equivalent RC active filters can take several forms. But unavoidable parasitic capacitances, many of which are nonlinear, eliminate many of the classical passive and active RC filter circuits from integrated-circuit realization. Filters based upon active integrators eliminate the effects of most parasitics, because inputs are at virtual ground and outputs are voltage-driven. A widely useful building block is the differential integrator, shown in both classical RC form and switched-capacitor form in Fig. 3. For the complete development of an IC filter (see "Designing a switched-capacitor filter," p. 108), a classical LC prototype is first transformed into a state-variable filter, where integrator voltages are the state variables, and then, after scaling, is transformed into the switched-capacitor circuit.

A simplified schematic and the IC implementation of a second-order bandpass filter in switched-capacitor form are shown in Fig. 4a. Eight bandpass filters of this type are used in the DTMF receiver. Bandpass filters of a



4. Bandpass, band reject. Biquadratic switched-capacitor filters are used throughout the DTMF receiver chip. Both bandpass filter (a) and band-reject filter (b) minimize circuit complexity by using operational amplifier 2 as both an integrator and gain block.



5. Second-order bandpass. The frequency response of the 941-Hz bandpass filter in the DTMF receiver chip displays a sharp rolloff. The Q of the filter is 15. Statistical data on filters from several wafers has shown standard deviations of 0.4% for both center frequency and Q.

higher order can be made by cascading second-order sections or by using a ladder configuration that reduces sensitivity to variations in parameters. The measured frequency response for one such second-order bandpass filter in the DTMF receiver is shown in Fig. 5.

Statistical data on filters from several wafers has shown that the center frequencies have a standard deviation of 0.4% from desired values, and the filters' quality factor, Q, has a standard deviation of 0.4% from the design value of 15. That level of control, obtained without trimming or adjustments, is ample for the DTMF receiver application.

Both of the bandstop filters in the DTMF receiver are made up of three cascaded second-order sections of the form in Fig. 4b; Fig. 6 gives the measured frequency response of one such section. A 60-Hz-rejection filter is built with a third-order high-pass filter, which provides 60 dB attenuation at 60 Hz, but less than 1 dB at 600 Hz. There is no difficulty in designing and building stopband attenuations up to 60 dB with switched-capacitor circuits.

Limitations

Since all factors regarding the accuracy of a switched-capacitor filter—gain, Q, center frequency, bandwidth, and so on—are set by capacitor ratios, the designs are as good as the best-trimmed active RC and LC filters. Furthermore, the stability with time and temperature of switched-capacitor filters is excellent—drifts are so small as to be virtually unmeasurable. The limitations are imposed by the elements of these filters themselves: capacitors, analog switches, and op amps.

Accuracy in capacitor ratios is limited only by the ability to define related capacitor areas through the various masking and processing steps, and several rather obvious techniques can minimize ratio error. Placing ratioed capacitors physically close together heightens the probability that they will experience similar mask and process variations. (The gate oxide that determines capacitance may, for example, undergo some variation in thickness across a chip.) Hence, the proximity of crucial capacitors is important.

Another rule of thumb is to maintain the same periphery-to-area ratio for ratioed capacitors, thereby minimizing any processing shrinkage effects. If these rules are followed, the capacitors become a model of stability: absolute voltage and temperature coefficients are 20 parts per million per volt and 20 ppm/°C, respectively—ratio variations are infinitesimal.

Analog switches

The MOS transistor is an excellent analog switch. It has up to a 90-dB on-off ratio, depending on layout, and no inherent offset voltage. Depending on the signal range involved, single-channel switches may suffice; C-MOS switches permit the fullest use of the system supply voltage range.

Gate-overlap capacitance gives rise to voltage offsets due to gate drive feedthrough to sources and drains, but it has no distorting effect. However, it must be considered, since voltage offsets can greatly reduce the linear range available. One caution regarding on-resistance: since minimally sized switches may have on-resistances of tens of kilohms, complete charge transfer may take as long as several hundred nanoseconds, depending on the capacitive load.

Since switched-capacitor filters are sampled-data filters, all nodes must settle between samples. Thus the useful frequency of such filters is limited by the settling time of the operational amplifier integrators. Settling to

Process considerations for switched-capacitor filters

To minimize costs and risks in the development of the dual-tone multifrequency receiver chip, only proven, standard process technologies were considered for the part. For one, switched-capacitor filters require high-quality analog switches with near-zero control current for precise conservation of charge. That calls for metal-oxide-semiconductor or junction field-effect transistors. Also, the switches must have low parasitic capacitance to minimize charge errors in coupling from clock to signal paths. Parasitic capacitances of MOSFETs are, in general, smaller than those of JFETs in monolithic circuits.

In addition to being precisely ratioed, the capacitors must have a very low voltage coefficient of capacitance to minimize harmonic distortion of the overall filter. Inversion-layer capacitors are ruled out—the capacitors must be formed between two highly conductive layers. Suitable capacitor plates are metal, heavily doped bulk silicon, and heavily doped polycrystalline silicon. The capacitor dielectric must be of high quality with no dielectric relaxation (hysteresis), which could introduce distortion. In this respect, deposited oxides are of questionable quality. Thermally deposited silicon dioxide is strongly preferred as the capacitor dielectric. Finally, the process technology must provide high-density, low-power digital logic.

Of the bipolar transistor processes, candidates for switched-capacitor filters are the bi-FET and the bi-MOS processes. In the former, JFETs are incorporated into a standard analog bipolar IC process by adding two process steps. The drawbacks of the bi-FET process, besides its complexity, are the high parasitic capacitances and relatively large area of the JFETs obtained. Moreover, the integrated-injection-logic circuits achievable are marginal in performance and low in density.

In the bi-MOS process, complementary-MOS devices are added to a standard analog bipolar process by means of two process steps. The availability of the bipolar analog devices is not a significant advantage; in relation to the switched-capacitor filter application a conventional C-MOS process is a substantially less complex alternative. Nonetheless, both bi-FET and bi-MOS can provide the necessary capacitors with the same bulk-silicon MOS structure used for compensation capacitors in standard bipolar operational amplifiers.

Among the MOS processes, metal-gate p-channel MOS, n-MOS, and C-MOS standard processes provide all of the needed elements. Capacitors are formed between metal and heavily doped source-drain diffusion regions with gate oxide as the dielectric in all of the processes. In addition, the MOS transistor is nearly ideal analog switch, with zero offset and zero control current.

P-MOS is not recommended if only because its use in new designs is on the decline. Similarly, metal-gate n-MOS is not a common process. But metal-gate C-MOS is widely available and provides all the needed features; hence, it was selected for use in the DTMF receiver.

Silicon-gate MOS processes generally provide higher circuit density and smaller parasitic capacitances than the metal-gate processes. The self-alignment of polysilicon gates with source-drain diffusions, however, makes it impossible to obtain a capacitor with low voltage coefficient between polysilicon and bulk silicon. Worse yet, the dielectric between polysilicon and metal is normally a deposited oxide with substantial hysteresis effects. Hence, good capacitors are simply not available in standard silicon-gate n-MOS and p-MOS processes.

Excellent capacitors are available, however, between the two layers of polysilicon in a double-polysilicon n-MOS process. The process used for erasable programmable read-only memories normally employs thermal silicon dioxide between the layers of polysilicon. The only drawback to the process is that it is relatively new and as yet difficult; only the large companies specializing in memories have the expertise. In the future, though, it may fare as an excellent choice for switched-capacitor filters.

A final possibility in the spectrum of large-scale integrated processes is C-MOS built on sapphire substrates, which has often been viewed as attractive for analog ICs. But few versions of this new process appear to offer satisfactory capacitors with low voltage coefficients. Further, leakage currents in SOS transistors are some 100 times greater than in MOS transistors on bulk silicon. Since the signals in switched-capacitor filters are conveyed as charges on capacitors of a few picofarads, larger leakage currents can cause undesirable dc offsets—and that could be troublesome when building low-frequency filters such as the much-used 60-Hz reject filter. In sum, C-MOS on sapphire is not particularly attractive for switched-capacitor filters.

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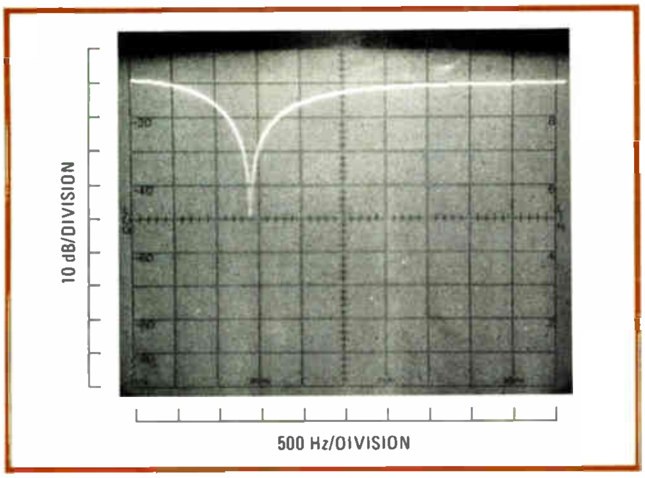
within 0.1% in 1 microsecond is readily achievable and implies a maximum clock frequency of about 1 MHz. In actuality, practical filters have an upper limit of about 200 kHz, limited by the Nyquist criterion. Evolution of fabrication technologies will raise this limit eventually.

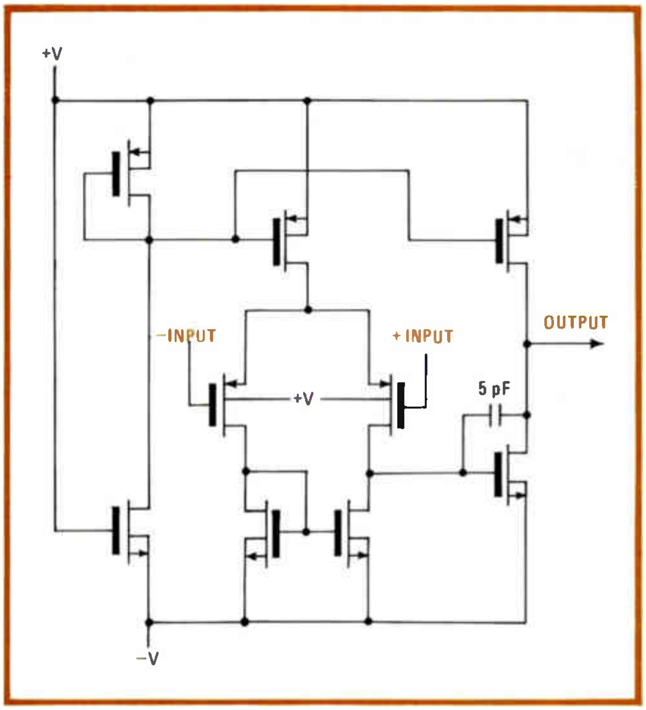
The op amps

MOS transistor amplifiers generate substantially more electrical noise than the best bipolar transistor amplifiers. The total rms noise voltage, integrated over the audio band and referred to the input of a MOS op amp, is in the range of 10 to 50 microvolts. When operating from 10-to-12-volt supplies, the rms maximum signal is about 2.5 V without overloading. Thus the maximum signal-to-noise ratio possible for a one-amplifier system is about 100 dB. Filters employing multiple amplifiers typically show an overall signal-to-noise ratio of 80 to 90 dB. While adequate for data communications, tone signaling, and telephone voice channels, that ratio is not acceptable for highest-quality sound and music systems.

The basic C-MOS operational amplifier, of which 40 are used in the DTMF receiver, is shown in Fig. 7. Because of the large number of amplifiers required, emphasis has been placed on minimizing circuit area and power consumption. Since the amplifier loads are small on-chip capacitors, a low output impedance, which requires large output transistors, is unnecessary. Although in the DTMF receiver any dc offset voltage at amplifier inputs is of little consequence (since response below 697 Hz is not desired), offsets for such amplifiers typically range from 5 mV to 50 mV—and filter output offsets may be greater due to the contribution of switch feedthrough. In other applications, where such offsets are unacceptable, auto-zero techniques have been



6. Second-order band reject. The measured frequency response of a second-order band-reject filter shows a Q of 0.8 and a 40-dB rejection at 1,404 Hz. Three cascaded sections of this type, illustrated in Fig. 4b, make up the two bandstop filters in the DTMF chip.



7. Op amp. The basic complementary-MOS operational amplifier is duplicated 40 times in the DTMF receiver chip. Its design emphasizes minimal chip area and power consumption. Each op amp dissipates only 5 milliwatts and occupies a mere 200 square mils.

successfully employed to reduce the effective dc input offset of an MOS amplifier to 1 mV or less.

The amplifiers shown in Fig. 7 have an open-loop gain of 3,000, a unity-gain bandwidth of 2 megahertz, power consumption of 5 milliwatts, and 0.1% integrator settling time of 3 microseconds. Die area per amplifier is a mere 200 square mils—only a quarter that of a typical bipolar-transistor IC operational amplifier.

Other applications

The melding of analog and digital functions on a single chip with LSI densities brings many additional applications to mind. A fifth-order, sharp-cutoff lowpass elliptic filter, for example, is required prior to sampling voice signals for PCM telephony. Switched-capacitor filters for this application are being introduced by two or more semiconductor firms. Those filters require pass-band ripple of less than ±0.125 dB and an overall signal-to-noise ratio on the order of 85 dB, so the application is a challenging test of the achievable characteristics of a filter technology. Although CCD filters for that function have been demonstrated, switched-capacitor filters alone can incorporate the 60-Hz-reject function and appear to have an advantage in signal-to-noise performance. Within two years, codecs and low-pass filters will likely be realized on a single chip.

Modulator-demodulators for data transmission can also be realized in fully integrated form. For instance, frequency-shift-keyed transmission that is normally used for data rates ranging from 100 to 600 bits per second can be realized. A frequency synthesizer develops digital versions of the signals to be transmitted from a precise crystal oscillator frequency, and a d-a converter forms the transmitted analog sine-wave signals keyed between 1,070 and 1,270 Hz for an originating terminal, or between 2,025 and 2,225 Hz for an answering terminal; both circuits serve the modulator function. A sixth-order bandpass filter defines one of two receiving bands, approximately 1,000 to 1,350 Hz, or 1,950 to 2,300 Hz, depending on whether the terminal is in the answering or originating role. A zero-crossing detector and timer perform the demodulator function. Additional digital circuits provide terminal-control logic, automatic answer and disconnect logic, and clock and timer functions. Single-chip modems incorporating all of those elements and built with switched-capacitor filters will, in fact, be feasible within the year.

Another important new applications area is in voice processing and voice input and output to computers. Speech synthesis using wholly digital techniques has been described recently [*Electronics*, Aug. 31, 1978, p. 109] that produces high-quality speech signals from a serial data stream of 2,400 bits per second or less.

While sophisticated linear predictive coding (LPC) techniques achieve that result, an alternative approach to encoding and synthesizing speech relies on formant analysis, an analog approach that offers certain advantages. First, the technique is well suited to a vocoder (voice encoder-decoder) system. Whereas LPC requires more complex analysis for encoding, formant analysis encodes voice signals using only a spectrum analyzer and pitch extractor. Moreover, formant analysis can produce the same quality speech at a lower bit rate than LPC.

The elements of vocoder systems lend themselves very well to combined analog-digital LSI techniques. The appeal of this approach compared to LPC techniques is that total silicon area may be considerably smaller. □

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Functional array eases custom ECL design

Macrocell array uses more than 100 logic, interface, and output cells to achieve the equivalent of over 1,000 gates

by Jerry Prioste, Ramu Rao,* and William R. Blood Jr., *Motorola Inc., Integrated Circuits Division, Mesa, Ariz.*

☐ Though emitter-coupled logic is the fastest commercial semiconductor technology, it, too, is being pushed by demanding applications to ever higher speeds, as well as greater densities. And increasingly complex applications mean increasingly complex custom designs.

One approach is to use bit-slice parts like those in the M10800 family [*Electronics*, Feb. 1, 1979, p. 99]. But when a standard family is insufficient, one can opt for Motorola's functional array, the Macrocell, which consolidates dozens of logic elements like flip-flops, adders, and registers into a single integrated circuit. This approach simplifies design, reduces power consumption, and saves board space. What's more, an engineer designing with the Macrocell array need not be an expert in the various ECL logic circuits, since that information is in the computer-aided design library that is an integral part of this approach.

With discrete components, one simply picks the needed functions out of a manual, interconnects them on a circuit board, and writes programs to test the product. With the Macrocell array, however, a single chip replaces a circuit board of approximately 50 IC packages.

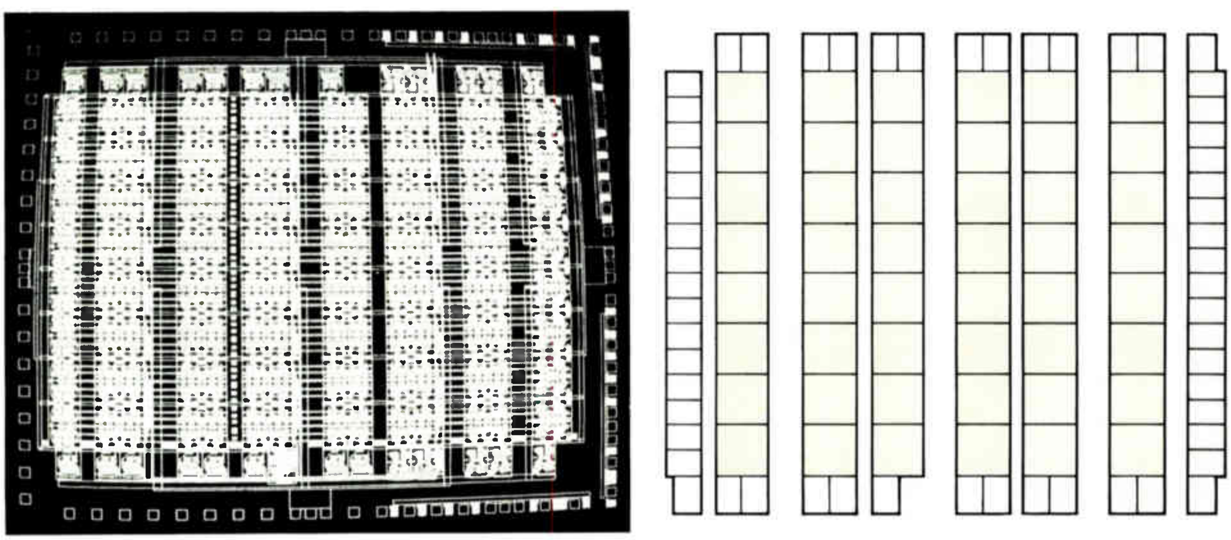
*Now with Sperry Univac, St. Paul, Minn.

The Macrocell concept is an extension of gate arrays currently used in mainframe computers. These arrays consist of 100 to 200 high-speed gates on a chip, interconnected by custom metal patterns to form various complex logic functions. The Macrocell array differs from a gate array in that it is subdivided into functional blocks instead of individual gates. Each Macrocell is itself roughly equivalent to a small- or medium-scale IC.

The array is composed of three cell types (Fig. 1). There are 48 large blocks, called major cells, that hold most of the actual logic circuitry. Arranged in a 6-by-8 array, these cells are identical to each other. Each has about 50 transistors and 50 resistors.

A Macrocell is created when internal metal patterns interconnect a major cell's transistors and resistors to form a logic element. At present, 54 different Macrocell functions have been defined and interconnected in major-cell blocks. These will be described later.

The Macrocell array also employs 32 interface cells at the chip's periphery. These cells do not have the logic power of a major cell. Fourteen functions have been defined thus far, including simple gates, inverters, clock buffers, latches, and so on. Interface cells are used when



1. Building blocks. Macrocell array functions are selected from a CAD library. A designer refers to a CRT display like the one on the left. Diagram on the right shows the relative positions of the 48 major cells (color), 32 interface cells, and 26 output cells (gray).

TABLE 1: PRIMARY FUNCTIONS OF MACROCELL TYPES
Major cells
Dual D flip-flop
Single flip-flop with multiplexed inputs
Quad latch
Dual latch with multiplexed inputs
4-to-1-line multiplexer
Quad 2-to-1-line multiplexer
1-of-4-line decoder
Priority encoder
Priority expander
Full adder
Dual half-adder
Various OR or NOR gates (up to 12 inputs)
Various AND or NAND gates (up to 8 inputs)
Various exclusive-OR or -NOR gates (up to 4 inputs)
Various OR-AND, OR-and-exclusive-OR gate combinations
Interface cells
2-to-1-line multiplexer
D input latch
Dual OR, NOR, AND, NAND gate
Various OR or NOR, AND or NAND, OR or AND gates
Output cells
2-to-1-line multiplexer
D input latch
25-Ω drive bus transceiver
Various OR, NOR, AND, NAND, exclusive-OR, exclusive-NOR gates

it is inefficient to tie up a major cell.

Although major and interface cells operate with standard 10,000 ECL levels, the relatively low internal current sources (1 milliampere) do not yield full output drive. Thus, though inputs can go directly to any cell of the chip, circuit outputs must first be routed through an output cell. Twenty-six such cells give the array the ability to drive a 50-ohm transmission line, making it compatible with the 10,000 ECL family. A set of 17 functions gives these cells logic power as well.

Fixed positions

All Macrocell-circuit options are built with a standard process, from diffusion to metal-mask making. This is key to the Macrocell concept. The positions of transistors, resistors, power buses, bias drivers, bonding pads, and so on, are fixed and only have to be engineered once. Development costs are thus reduced for both standard and custom parts.

Currently available bipolar LSI circuits, such as the 2900 transistor-transistor-logic family or the M10800 ECL family, are designed around bit-slice architectures. These function well in many processor applications, but often there are other high-speed logic needs that standard families cannot provide. With the Macrocell array, a custom chip can be defined to meet such needs. Possibilities include high-speed disk controllers, fiber-optic or radio-frequency communications systems, high-speed test equipment, and mainframe computer systems. Moreover, parts developed for a specific product are difficult to duplicate, so a product can remain proprietary. All three Macrocell types are configured into predefined logic functions (Table 1).

Table 2 lists the major array circuit features. There is actually no fixed number of Macrocell array gates because gate density depends on the functions selected. However, many options can be put together with a set of major, interface, and output cells that exceeds 800 equivalent gates out of the 1,192 possible.

Fewer watts

When 90% of the cells are used, the chip's power consumption is about 4 watts. Since unused cells are not connected to power buses, actual package power depends on the function performed. Dividing 4 W by 800 gates yields an average gate power dissipation of 5 milliwatts. Output cells capable of driving 25- or 50-ohm transmission lines need more power, and internal gates require somewhat less.

The Macrocell array has 60 logic I/O pins. Of the 60, 34 function only as inputs. The remaining 26 may be used for input, output, or bidirectional I/O bus ports. This flexibility increases the range of part types available to the user.

The bidirectional I/O ports are built with bus-transiceiver output-cell functions (see Table 1 again). Through these ports the Macrocell array interfaces directly with system bus lines, thus eliminating the need for external bus-driver circuits. A transceiver's 25-Ω output drive is used to handle bus-line impedances as low as 50 Ω when terminating resistors are at each end of the line.

Macrocells use series-gated structures to perform complex functions with maximum gate speeds. Some of the functions would require at least three delay stages if implemented without series gating. However, it is difficult to determine actual gate speed in the array. Cells connected as simple gates would typically have a 0.9-nanosecond propagation delay (1.3 ns maximum). However, total Macrocell speed is a more meaningful parameter. The slowest major or interface functions listed in Table 1 have a typical propagation time of 1.3 ns (1.8 ns maximum).

Output cells are slightly slower because of the transmission line drive. They have a typical propagation delay time of 1.5 ns and a maximum of 2.2 ns.

The Macrocell array's compatibility with the 10,000 ECL family is a large bonus. Over 100 part types are available that directly interface with the array, including random-access memories, programmable read-only memories, TTL and metal-oxide-semiconductor interfaces, and the M10800 bit-slice processor family. Compatibility means that all parts operate off the same power supplies and match all input, output, and noise-margin specifications.

Custom development

Custom arrays are designed with a Motorola computer-aided design system (Fig. 2). After deciding on the number of parts, the production volumes for each, and development costs and schedules, the customer receives a design handbook and a password to the CAD system. The CAD system is accessed over phone lines through a leased or purchased graphics terminal and optional plotter located at the customer's facility.

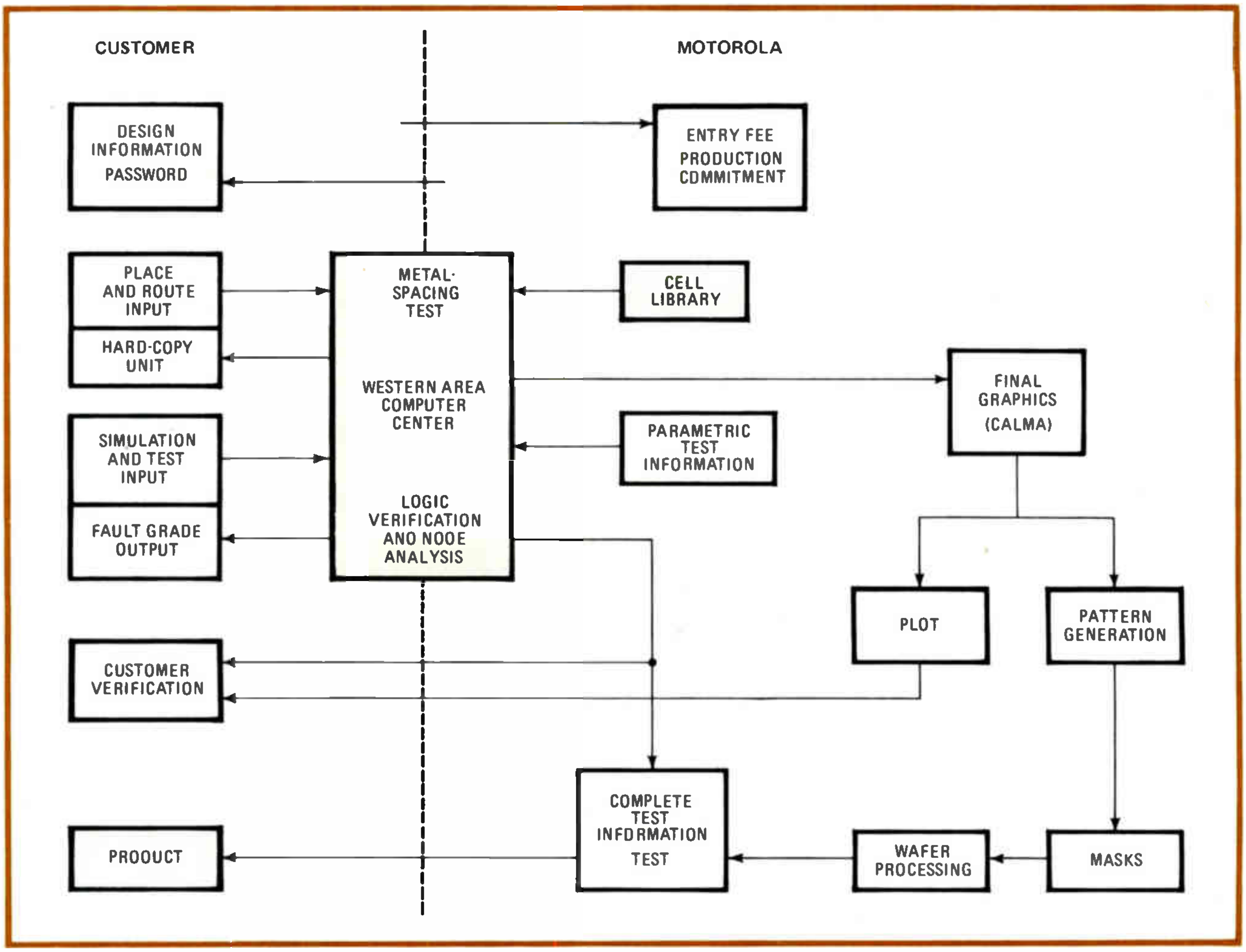
The CAD system contains the Macrocell library, plus a number of programs to help design and check the circuit. A chip layout shown in Fig. 1 is displayed on the terminal's screen. The designer selects cell functions from the CAD library and places them in the desired cell locations. Using the terminal, he then defines I/O points and specifies point-to-point data-routing information. Additional CAD programs perform logic simulation to verify design accuracy, and others check for violations of interconnection wiring rules.

Cell-to-cell wiring is an important part of option design. The array has 12 channels alongside each Macrocell for cell interconnection. These are in addition to the power buses, as well as the bias-reference voltages and metal interconnections in the cells themselves. With respect to the 6-by-8 array of major cells, there are 100-by-130 metal channels reserved for cell-to-cell and cell-to-I/O-pin routing.

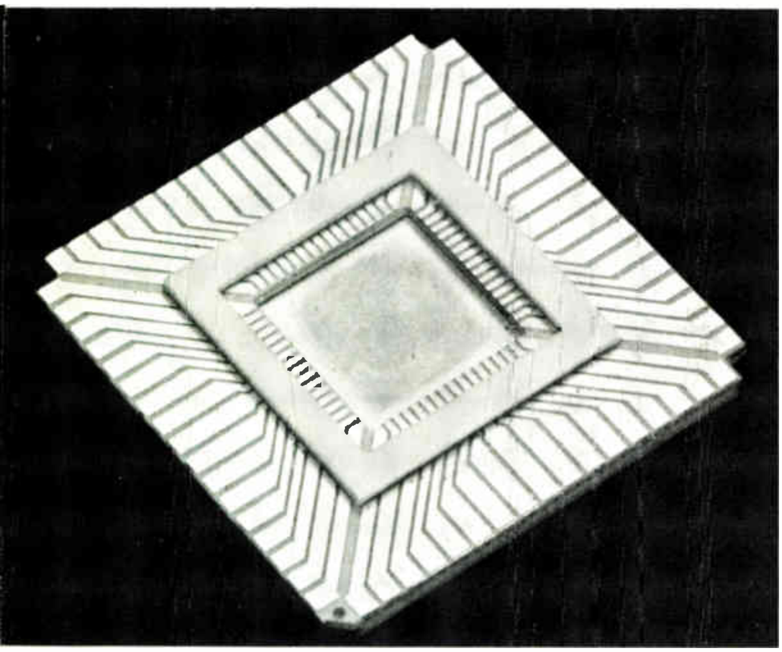
Customers must also generate final test sequences. Here, again, the CAD system is extremely helpful because programs are available to check for paths not covered by the user's test sequence. The CAD programs also yield a test format compatible with Motorola's final-test equipment.

Upon completion of a custom design, information in the CAD system is fed through Motorola's Calma graphics system to a plotter. Drawings of the cell selections and routing patterns are sent back to the designer for final verification. When approved, the Calma data is used for pattern generation and mask making. Custom metal patterns are added to wafers, completing the processing sequence for the ICs. Final test information in

TABLE 2: MAJOR FEATURES OF THE MACROCELL ARRAY
1,192 equivalent gates (approximate)
5-mW average gate power
4-W typical power dissipation (all cells used)
34 input ports, 26 input/output ports
25-Ω drive on up to 8 outputs
Macrocell delay: 0.9 – 1.3 ns typical, 1.3 – 1.8 ns max
Compatible with the 10,000 ECL family



2. Exchange. Motorola's computer-aided design system is essential to developing a Macrocell option. A graphics terminal links the customer to the system via a telephone line. Design inputs are converted into a format that is compatible with final-test equipment.



3. No leads. The Macrocell's 68-pin leadless package features small physical size, high I/O-pin density, and good thermal characteristics. Support hardware under development will hasten its acceptance as an LSI packaging standard. A 68-pin DIP just wouldn't do.

the CAD system is converted into test programs that are used to test the circuit before shipping the final products.

The popular dual in-line package has serious limitations when pin numbers increase. The 68-pin Macrocell array would require a DIP over 3 inches long. Such a package would take up too much circuit-board area, and impedance of the long leads on the substrate are not suitable for the high speed of ECL signal lines. This package would also be difficult to handle in terms of maintenance or replacement.

Fortunately, system manufacturers, especially mainframe computer companies, realize the need for a standard LSI package and have worked to develop the Joint Electron Device Engineering Council's LSI package standard for devices with 0.05-in. centers. This housing contains 68 pins, is leadless, and has 17 terminals per side (Fig. 3). The IC mounts on a ceramic base slightly smaller than 1 in.^{2} Gold-plated metal on the base piece routes signals and power from the package edge to the chip. A ceramic cover over the wire-bonded chip provides a hermetic seal.

The package is mounted upside down in terms of conventional IC practices. The base of the chip is on the top side, away from the pc board. A heat sink is bonded to the package on the same ceramic piece as the chip for efficient heat transfer. The package and heat-sink combination have a thermal resistance of 15°C/w, allowing the relatively high-power circuit (4 W) to operate safely in an air-flow environment.

Two techniques can be employed to mount the package on a pc board. The first uses rows of metal clips that solder to both the IC package and the board. The clips hold the package off the board, yet provide solid mounting and good electrical connection.

The second method uses the package and connector arrangement illustrated in Fig. 4. The connector (manufactured by AMP Inc.) can be either soldered to the pc board or held in place with a mounting bolt. The leadless IC package fits into the connector and is held in place with a spring clip. Sixty-eight metal tabs near the connector base facilitate testing and troubleshooting by giving access to all 68 package pins.

Practical?

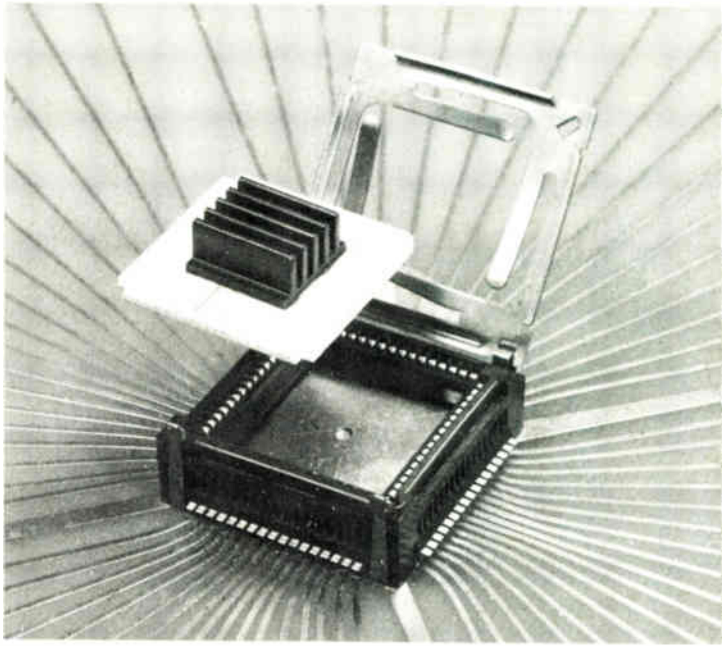
Consider an 8-bit binary/binary-coded-decimal arithmetic and logic unit made with the Macrocell array (Fig. 5). The circuit features four 8-bit data ports—three for input and one for output. Independently controlled latches can be used to hold data on any input. Five function-select lines determine 32 ALU operations to be performed on the A, B, and C inputs. All commonly used ALU functions are incorporated, including add, subtract, shift left, shift right, increment, decrement, and transfer plus other logic operations.

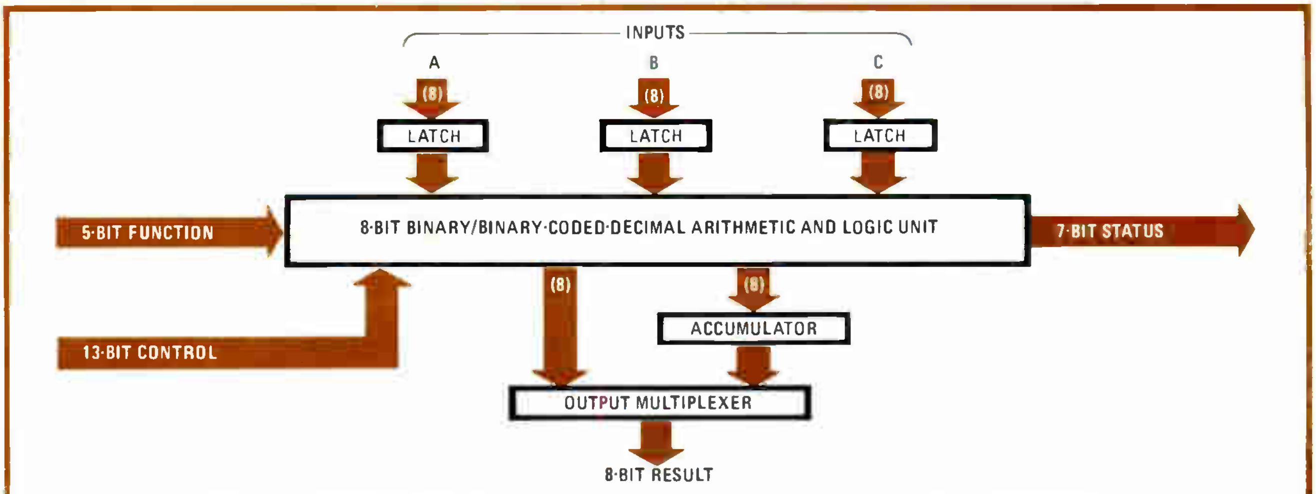
The propagation delay from input through the ALU to the results output is estimated at 13 ns maximum. Using ripple-carry propagation increases the delay 2.2 ns for each 8-bit increment in the width of the input. Above 32 bits, carry–look-ahead circuits built as part of another Macrocell array option can minimize the delay.

A 16-by-4-bit, triple-port register-file circuit built from the array would have a maximum address access time of 6.5 ns. Four register-file circuits and two ALUs would build a 16-bit system ALU with microinstruction cycle times under 25 ns. This is six to eight times faster than existing speeds for LSI TTL.

The 8-by-8-bit expandable array multiplier in Fig. 6 further illustrates the performance of the Macrocell array. The circuit accepts 8 multiplier and multiplicand

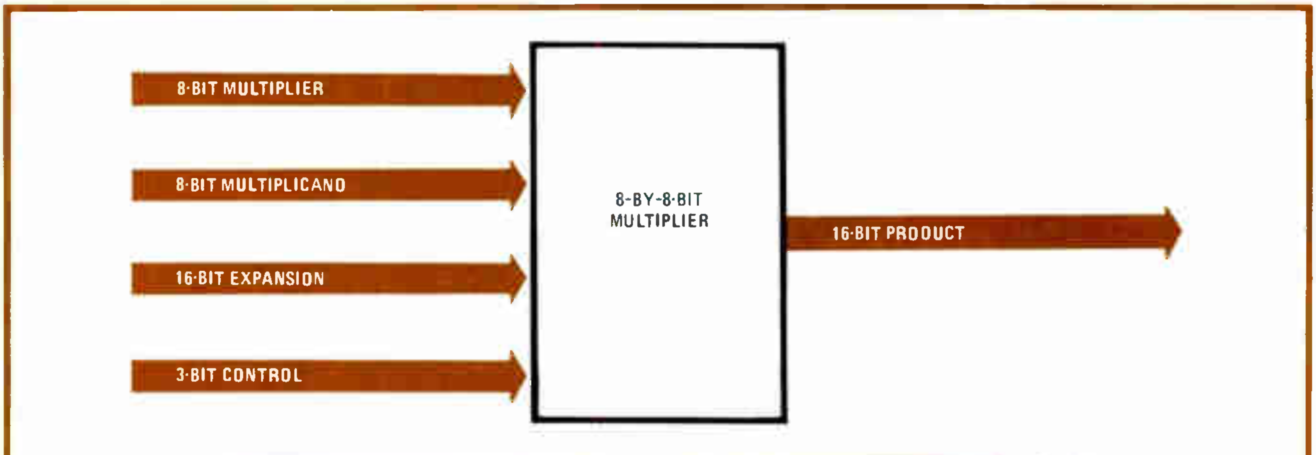
4. Box. Metal clips can be used to solder the leadless package of Fig. 3 to a pc board, or the connector shown below can be used. It permits easy replacement without damaging to the circuit board or the package, and the cover provides a hermetic seal.





Size (bits)	8	16	24	32
Add delays (max,ns)	13	15.2	17.4	19.6

5. Fast math and logic. A high-speed 8-bit binary/BCD ALU illustrates the functions and performance of the Macrocell array. This circuit, featuring four 8-bit data ports, requires 57 of the 60 available signal pins and performs all of the common CPU functions.



Size (bits)	8 by 8	16 by 16	24 by 24	32 by 32
Package count	1	4	9	16
Delay (max,ns)	23	48	74	100

6. Multiplier. The 8-by-8-bit multiplier is a good benchmark circuit, since it is widely used. Though the Macrocell design is more complex than most, it is faster and smaller. What's more, it is easily expandable and allows asymmetrical combinations like 16 by 8 bits.

bits and generates a 16-bit product. Control inputs select between 2's complement and sign-magnitude formats, and the expansion inputs allow the array to be expanded without additional part types.

As indicated, four packages are needed for a 16-by-16-bit multiplier, 16 for a 32-by-32, and so on. Asymmetrical combinations such as 16 by 8 or 24 by 8 bits also can be built for specialized applications. Compared with existing LSI products, a multiplier built from the Macrocell array would be many times faster and easier to expand. The 48-ns multiplication time of the 16-by-16-bit configuration should meet the requirements of future high-speed signal-processing systems.

Process developments promise faster logic for other technologies, like n-channel and complementary MOS, C-MOS-on-sapphire, and integrated injection logic. However, they are many years way from the speeds of today's ECL. Moreover, Macrocell arrays are four to eight times faster than existing bipolar LSI, because of processing improvements and innovative circuit design. Even more important, LSI emitter-coupled logic is an open-ended technology, and processing developments under way could lead to arrays with 1,000 or more subnanosecond equivalent gates in the next few years. ☐

This is the second of two articles on high-density ECL. The first, which appeared in the Feb. 1 issue, pages 99–105, discussed the M10800 family of bit-slice parts.

Voltage-controlled amplifier phase-adjusts wave generator

by G. B. Clayton
Liverpool Polytechnic, Liverpool, England

When added to a generator that produces two triangular and two square waves in quadrature, a voltage-controlled, gain-switching amplifier makes it easy to adjust the phase difference of each pair of signals. The entire circuit—that is, the generator and the controller—requires only two chips and one field-effect transistor for providing phase differences from 0° to 180°.

In the arrangement shown, a quad operational amplifier (A_1–A_4) serves as the quadrature oscillator, and a dual op amp (A_5–A_6) is the control section. Amps A_1 and A_2 form an integrator and comparator, needed for generating the triangular and square waves. A_3 is a zero-crossing detector, used to produce a square wave from the triangular input of A_1. A_4 produces a second triangular wave from A_3's output. Note that the feedback resistor R_3 in the A_1–A_4 loop will prevent A_4 from drifting into saturation, even if offset voltages from the op amps are high.

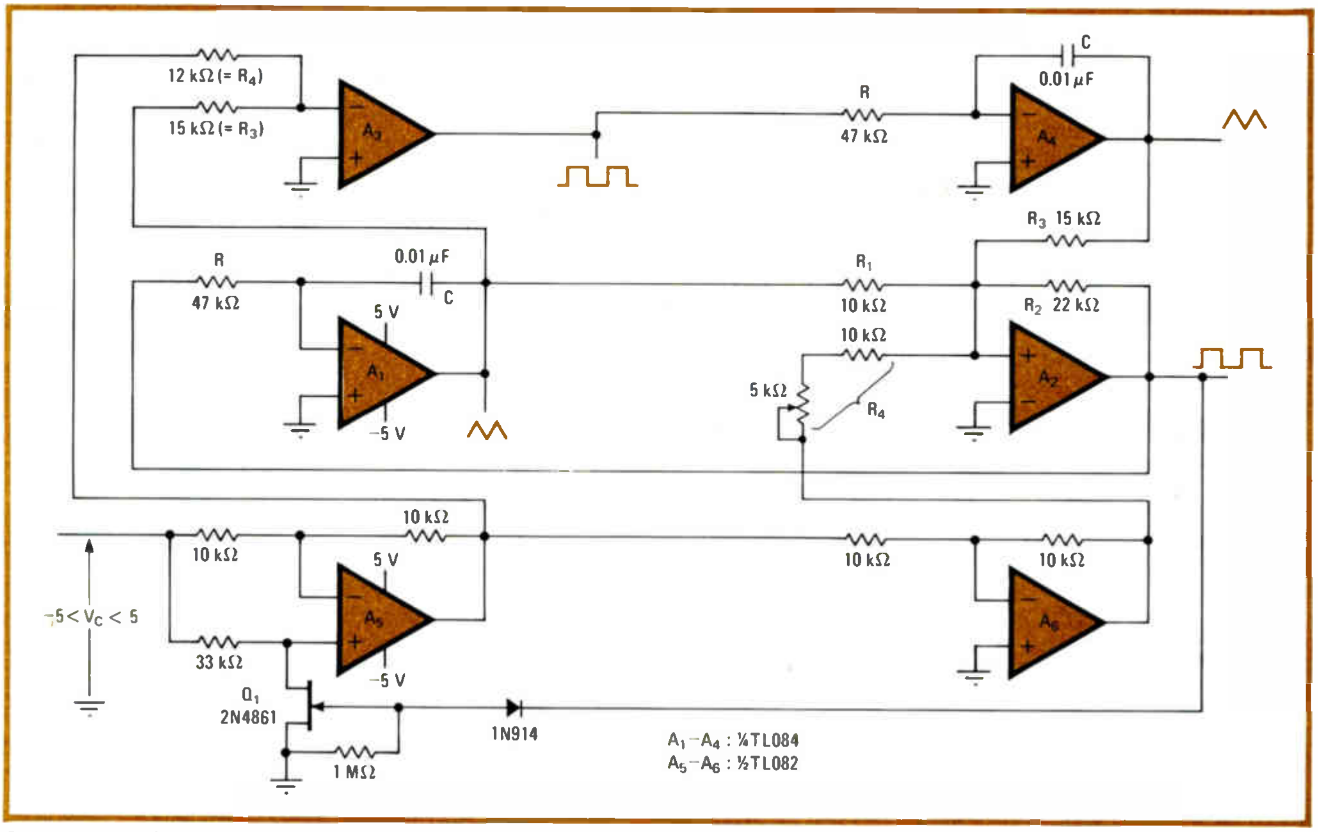
In the phase-control section, A_5 acts as the switched-gain element. A_2 and Q_1 control the gain of A_5. When Q_1 turns on, A_5 has a gain of -1; otherwise, its gain is $+1$. This element, appropriately biased at its input with a control voltage, V_c, thus turns on and off sooner or later than usual, depending on the magnitude of the control voltage. This acts to advance or retard A_3's on-off transitions on both the rising and the falling edge of A_2's square-wave signal. As a result, the signals from A_3 and A_4 lead their respective counterparts at A_2 and A_1 by a value almost linearly proportional to V_c.

A_5's output is inverted by A_6, which is in turn connected to potentiometer R_4 and A_2. R_4, included to overcome the effects of component mismatch, is placed strategically, so that it will not interfere with the generation of waves produced by A_1 and A_2.

If the components and amplifiers are matched, the frequency of oscillation for all waveforms will be $f = R_2/4R_1CR$. The relation between control voltage, resistor R_4's value, and phase shift is given by:

$$\theta = 90°[(V_cR_2R_3/V_{osat}R_1R_4) - 1]$$

where V_{osat} is 0.7 v below the supply voltage. □



Quadrature variance. Waveform generator that normally produces in-quadrature (90° departure) triangular or square waves is converted into variable phase-delay circuit when gain-switching amps A_5–A_6 are added. A_5–A_6 act to advance A_3's turn-on transition, so that signals at A_3 and A_4 lead those at A_1 and A_2. Phase shift between both sets of waves is controlled by V_c.

Synchronous counters provide programmable pulse delays

by R. E. S. Abdel-Aal
Sunderland Polytechnic, Sunderland, England

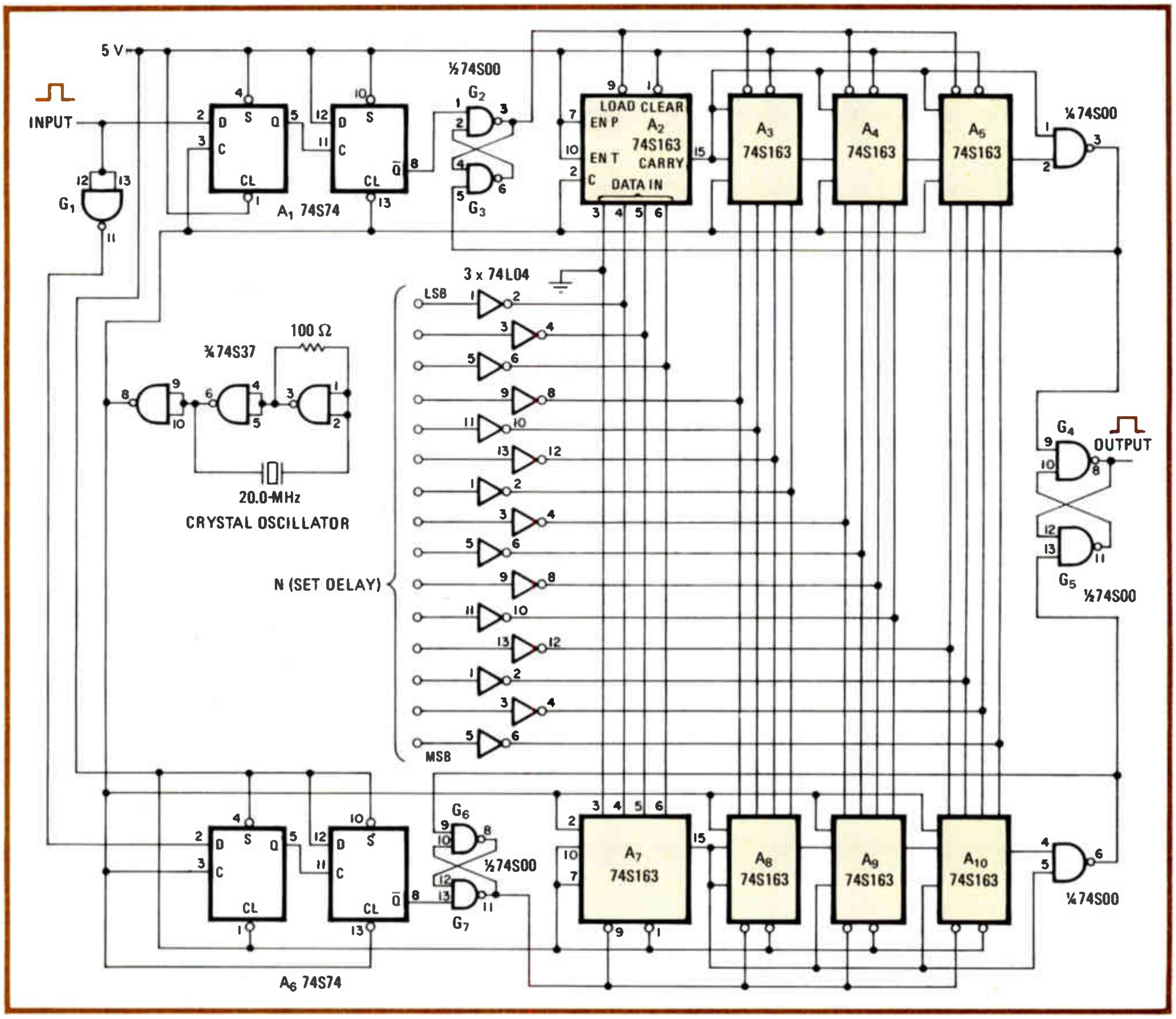
In this circuit, cascade counters are digitally programmed to provide pulse delays of 50 nanoseconds to 3.25 milliseconds, accurate to within 50 ns. Selected by a 15-bit binary number, N, the delays can be ordered in 100-ns steps.

Two chains of synchronous counters, driven by a 20-megahertz clock, delay the input pulse's leading and trailing edge separately. Input pulses, which are asynchronous, are first applied to a dual D flip-flop, A_1, as shown. A_1 generates a single negative-going clock pulse when triggered by the 20-MHz clock. The pulse is used to set the bistable latch, G_2–G_3, thus enabling counters A_2–A_5 to delay its leading edge.

A_2–A_5 are wired to perform a fast look-ahead operation for the high-speed multistage counting required. To eliminate glitches that might upset the counter, the carry outputs of both A_1 and A_5 are brought to a NAND gate and then to G_2–G_3. This ensures the latch will be reset and the desired N value loaded into the counter only after the previous delay period is ended, despite the differential delays that exist in the signal path.

The input pulse is inverted by G_1 and applied to flip-flop A_6 for the counters that provide delay on the trailing edge of the pulse, A_7–A_{10}. G_6–G_7 and A_7–A_{10} perform the function identical to G_2–G_3 and A_2–A_5.

In actual operation, both counter chains are programmed by the set-delay lines, which are connected to their data-in ports. The delay time is given by $T = 50(1 + 2N)$ ns. At the end of the delay period, N is



Two-edge retardation. Counter chains, of which one starts counting on arrival of the positive edge of an input pulse, the other on its negative edge, use a 20-MHz clock to provide repeatable delays of 50 ns to 3.25 ms on both edges of signal. Delays produced are accurate to within 50 ns. Amount of delay is selected with 15-bit word (M). Width of input signal to be processed must be at least 60 ns.

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loaded into both counter chains. Note that the circuit is wired such that the N inputs must be active high, ensuring that maximum delay will correspond to a value of N that, when read as a number in standard binary form, is maximum.

Upon the arrival of the leading edge of the input pulse, A_2–A_5 count up, starting from the number loaded. Similarly, A_7–A_{10} count up on the trailing edge of the pulse. The carry pulse generated by A_5 signifies the end of the delay period. This signal is united with the carry pulse generated by the trailing-edge counter A_{10}, at flip-flop G_4–G_5. The signal at the output of G_4–G_5 thus has the same width as the input pulse, but is delayed by a period of time proportional to the number N. □

Counter delivers data in signed or complemented form

by N. Bhaskara Rao
U.V.C.E., Department of Electrical Engineering, Bangalore, India

Adding one chip to the basic digital-averaging circuit proposed by Frazier [*Electronics*, Nov. 9, 1978, p. 114] forms a data counter whose outputs express a negative number not only by its magnitude and sign, but by its 2's complement as well. Expressing numbers in the latter form enhances the circuit's usefulness by allowing direct interfacing with computer circuits.

The circuit shown works differently from Frazier's, which generates a sign bit and reverses the direction of the count when the counter is about to move down through zero. Instead, the 74193 is allowed to go below zero, where its R output becomes 15 and the state of its borrow output changes, thereby clocking the 7470 flip-flop. The 7470's Q output, which is the sign bit, S, then moves high.

The sign bit and the R bits are applied to the 7483 4-bit full adder (not part of the original circuit) through the 7486 exclusive-OR gates. The 7483 and 7486 together form an add-or-subtract unit. As a result, the output of the adder, M, will be equal to R if the 74193 indicates it holds a positive count ($S = 0$), and will be equal to $16 - R$ if the 74193 has gone negative ($S = 1$).

If $S = 0$, the R bits, as seen at the output of the 74193, will represent the binary equivalent of the number. Any negative number will be represented by its 2's complement value and an enabled borrow bit. □

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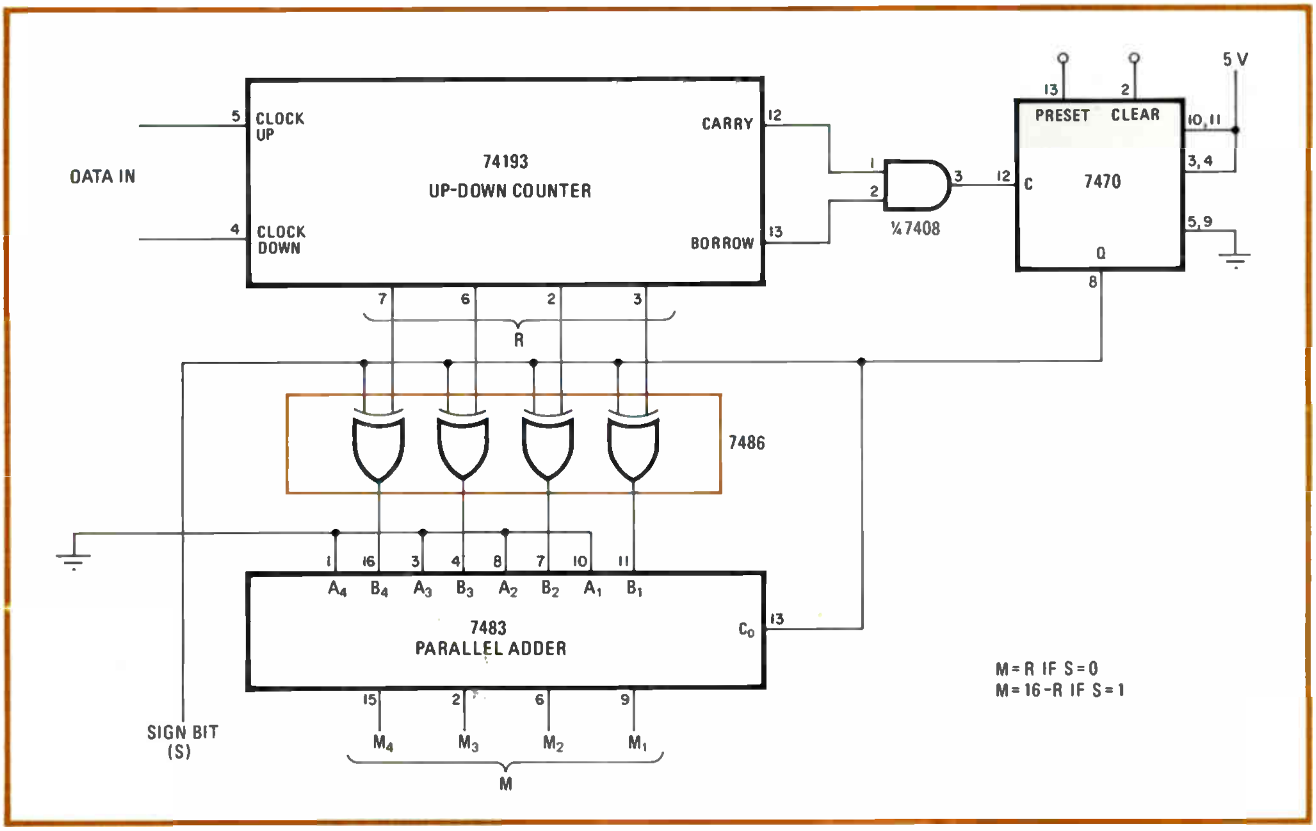
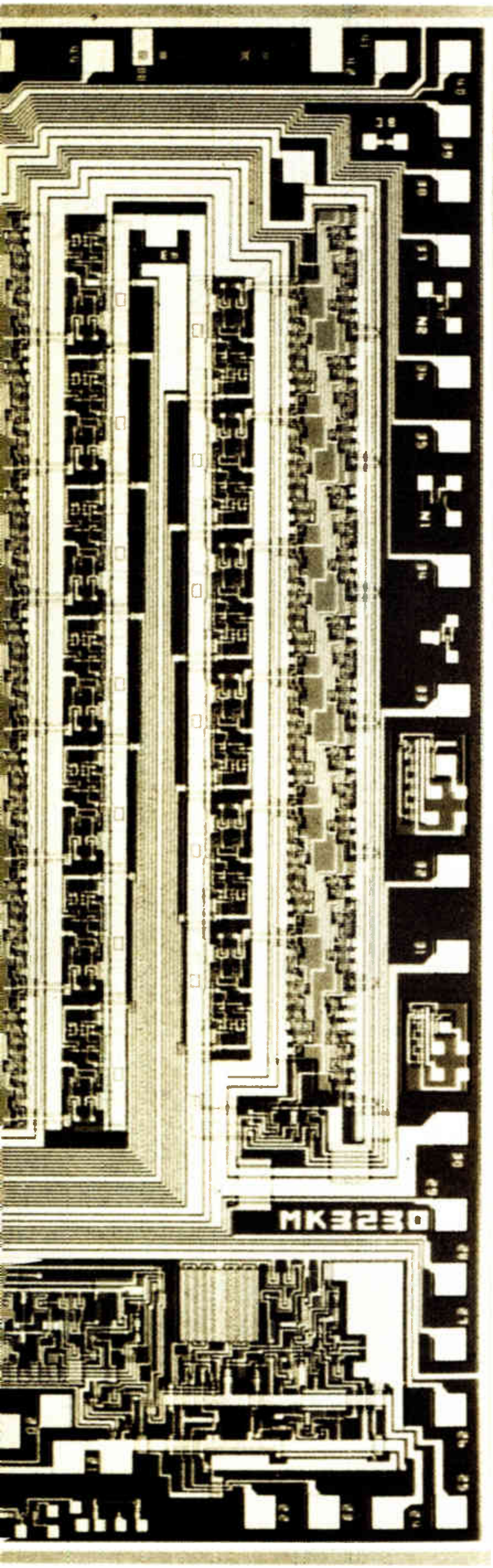


Number forms. Availability of any number in both binary equivalent or magnitude-sign forms enhance circuit's interfacing capability. Data generated by 74193, expressed as binary number (R bits), is converted into magnitude-sign form by add-or-subtract unit 7483–7486. R represents the 2's complement of any negative number when counter steps down through zero.



ISSCC

A coming-out party for the important new devices

Now in its 26th year, the International Solid State Circuits Conference continues to enhance its reputation as the premier forum for announcements of significant advances in semiconductor technology. One major reason for the stature of ISSCC, which returns to Philadelphia from last year's sojourn in San Francisco, is its unrelentingly high standards for selecting papers from the hundreds of submissions. Another is the conference's traditional role as a precursor of important products.

This year is no exception. In the memory area, for example, attendees will be given their first glimpses of superfast static random-access memories from Intel and 64-K RAMs from National, Siemens, and Bell Laboratories. The innovative Japanese are weighing in with some impressively large-capacity devices, presumably fallout from their VLSI program. Even a partial list of the chips would have to include a huge 128-K read-only memory, a 1-megabit wafer-size RAM, and a 5,000-gate logic array. Also in logic, look for the debut of a new high-speed bit-slice family from Fairchild, with slices that are all of 8 bits wide.

But linear technology is also an important feature of ISSCC. This year, high-performance conversion devices are spearheading the host of important developments in this area. Speed and accuracy are benefiting from new techniques, as evident in TRW's 35-MHz fully parallel a-d converter, 12-bit a-d or d-a devices from the University of California, Berkeley, Advanced Micro Devices, and Nippon Electric, and a 13-bit unit from Matsushita.

Another important trend at this year's meeting is the impact that large-scale integration is beginning to make on linear functions. This can be seen in two major innovative approaches: the combination of analog and digital techniques on the same chip, and the use of digital techniques to do real-time signal processing. The first is exemplified by Silicon Systems Inc.'s tone decoder chip (see p. 105), the second by Intel's new analog microprocessor. These and the growing use of switched-capacitor filter techniques will open a whole new analog world to LSI.

Design, process innovations expand memory, logic frontiers

by Raymond P. Capece
Solid State Editor

☐ That chip manufacturers are suffering from no shortage of innovative designs is evident from their memory circuits, which adopt new and sometimes startling ways of boosting speed and density. Microprocessors, too, are taking on new challenges, and a trend toward analog-digital large-scale integration is fast developing.

Likely the most unusual entry in the dynamic memory area is Texas Instruments Inc.'s taper-isolated cell for a dynamic-gain random-access memory. First introduced at the International Electron Devices Meeting in December of last year, the taper cell is conservatively posted by the Dallas company as capable of yielding RAMs with read-only-memory densities; in actuality, its theoretical cell size of 6 F^2, where F is the interconnect line width, makes it a viable candidate for a superior 64-K RAM—or even a 256-K device.

Whereas the IEDM presentation covered the physics of the device's operation [*Electronics*, Dec. 21, 1978, p. 31], the ISSCC paper describes its optimization for a large memory array. Shown in Fig. 1, the cell indicates a 1 or a 0 by the presence or absence of a hole packet in the channel region and hence uses a single transistor but no capacitor. The cell area accordingly is only a third that of a conventional dynamic RAM's one-transistor cell.

Other pluses could also accord the taper cell superior performance to conventional RAM designs. First, unlike stratified-charge approaches to eliminating the capacitor, which require a constant-charge signal to be read, the device supplies a constant-current signal. That signal not only provides roughly five times the drive capability of conventional RAMs, according to one TI benchmark, but can actually be designed into the cell to meet a given access-time requirement. Second, diffusion currents, which arise especially at high temperatures, are collected by the taper cell's drain and, as such, contribute minimally to leakage, even at 100°C. Also, the activation energy of that leakage, being much lower than in conventional RAMs, leads TI to believe its cell will be far less susceptible to soft errors caused by alpha particles.

However, generating the negative pulse needed to write a 1 into the cell remains a problem, since the normal n-channel process does not lend itself well to negative swings. TI counters that by adjusting the shallow p-type implant, so that a zero gate-oxide surface potential occurs at a positive gate voltage and the cell can be operated with three-level positive clocks.

A somewhat more conventional approach to the 64-K RAM is taken by National Semiconductor Corp., Santa Clara, Calif. Its triple-polysilicon process (Fig. 2) yields a 195-square-micrometer cell size and hence a 38,000-mil-square chip (pin 1, incidentally, is left unconnected).

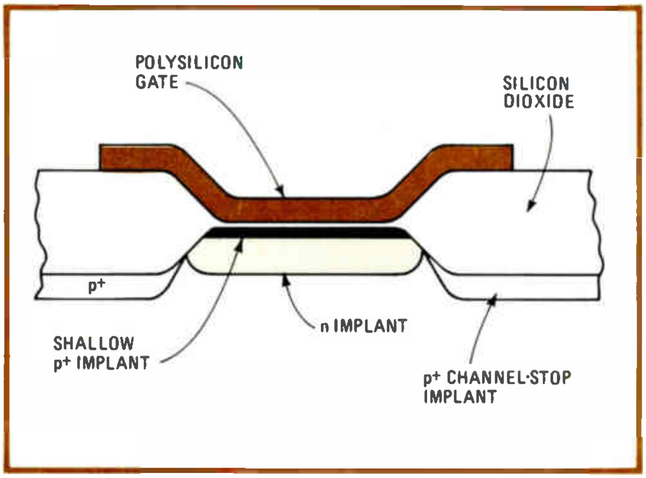
The cell is the usual one-transistor, one-capacitor type. But the capacitor, being formed between two of the three layers of polysilicon, is a high-quality one, says National, unlike the inversion-layer capacitor of 16-K dynamic RAMs. A mere fifth of the total area of improved capacitor's storage node is subject to substrate leakage, and the device has a higher immunity to alpha particles.

National has also improved the sense amplifier, giving it a symmetrical design and two bit lines. Thus the number of memory cells attached to each bit line is halved, increasing the signal level that is sensed, while the symmetry eases the layout and improves the matching of dummy and memory capacitors. The final 5-volt-only chip, arranged into four 16-K arrays, requires 256 refresh cycles at 4-millisecond intervals and provides an access time of 120 nanoseconds.

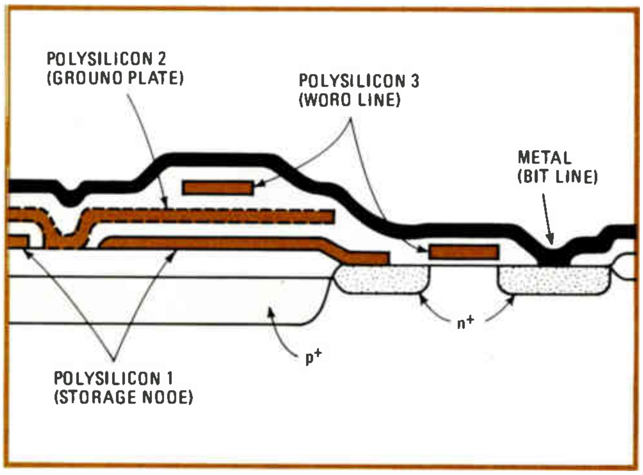
Redundancy to the rescue

At Bell Telephone Laboratories Inc., Allentown, Pa., the needs are different and so is the 64-K RAM. To ensure immediate high yields, Bell designs redundancy bits into its n-channel, two-polysilicon-level device. As Fig. 3 shows, each of the chip's two 32-K arrays contains spare rows or columns, which are substituted for defective ones by laser pulsing. An yttrium-aluminum-garnet (YAG) laser with a 1.06-μm wavelength burns open polysilicon lines that are buried under phosphorus-doped glass. No special processing is needed, says Bell, because the laser repairs are done during wafer probing.

Aside from its redundancy and unusual power supplies of +8 and −5 V, Bell's 64-K RAM maintains compatibility with industry-standard 16-K dynamics, since it requires 128 refresh cycles every 4 ms and has an access time of 100 ns. In addition, Bell has made special efforts to reduce power dissipation: there is full selection of only



1. New cell. One-transistor RAM cell with no capacitor stores 1s and 0s at different thresholds. TI, which calls the device a taper-oxide dynamic-gain cell, says the device looks good for large memory arrays where it could be driven with three-level positive clocking.



2. Triple-poly approach. National Semiconductor is using a three-level polysilicon process to build its 64-K RAM. Advantages of the more complex process, says National, are a better capability and a lessened susceptibility to soft errors caused by alpha particles.

one 32-K array at a time, and the sense-amplifier/column-buffer circuits partially decouple the heavily capacitive column line from the sense amplifier during latching, thus achieving fast access time without the usual high-current spikes.

N-channel MOS static RAMs are forever on the descent in access time, and, as usual, Intel Corp. is leading the parade. In two separate papers, the Santa Clara chipmaker describes its second generation of high-performance MOS, which it calls H-MOS II. By pushing the limits of silicon technology to 2-μm channel lengths and 400-angstrom oxide thicknesses, Intel has driven gate delays way into bipolar territory—400 picoseconds—and produced working 1-K- and 4-K-by-1-bit RAMs with the barely credible access times of 15 and 25 ns, respectively. Of course, even with n-channel MOS, speed isn't free—it comes at a cost of increased power dissipation. But with maximum power ratings of about half a watt, n-MOS still has any bipolar competitor beat, and it easily excels in a memory system where chips can be deselected.

Applying the same scaled-down process to a 16-K-by-1-bit static memory, Intel has produced a 45-ns device—faster than current 4-K chips—yet one that dissipates little more than half a watt. The key to its density is a second level of polysilicon interconnect, which will assuredly be adopted by other semiconductor manufacturers as they gain the necessary expertise.

A big ROM and the electron beam

Nippon Telegraph and Telephone Public Corp.'s Musashino Electrical Communication Laboratory in Tokyo offers a viable approach to the next generation of read-only memories with its 128-kilobit electron-beam-written ROM. In one go, NTT solves several of the problems of huge ROM arrays: it minimizes die size, holds back power dissipation, and adds flexibility to programming with a scanning electron-beam exposure system.

The 16,384-by-8-bit ROM is arranged in four 32-K arrays, as shown in Fig. 3. Its cell size is a scant 62 μm^2, due to a design in which each pair of bits requires only one contact hole. The resulting die is only 20.6 square millimeters in area.

The power dissipation of the single-5-V device is a low 65 milliwatts, thanks to a dynamic-inverter approach and some clever circuit design. Yet the access and cycle time are more than respectable, at 200 ns and 400 ns, respectively.

Perhaps the most significant feature of the big ROM, however, is its electron-beam programmability. Although at the 1.3-megahertz beam stepping rate used it takes two minutes to program each die, the flexibility of the approach cannot be denied. Each die on a wafer can have different data written into it, since the electron beam operates under software control. The beam modifies the threshold voltage of each MOS device in the array; thus, the data writing is done halfway through the chip fabrication process. The ROM's initial application will be as a character generator for Chinese ideographs, each of which requires 288 bits to define.

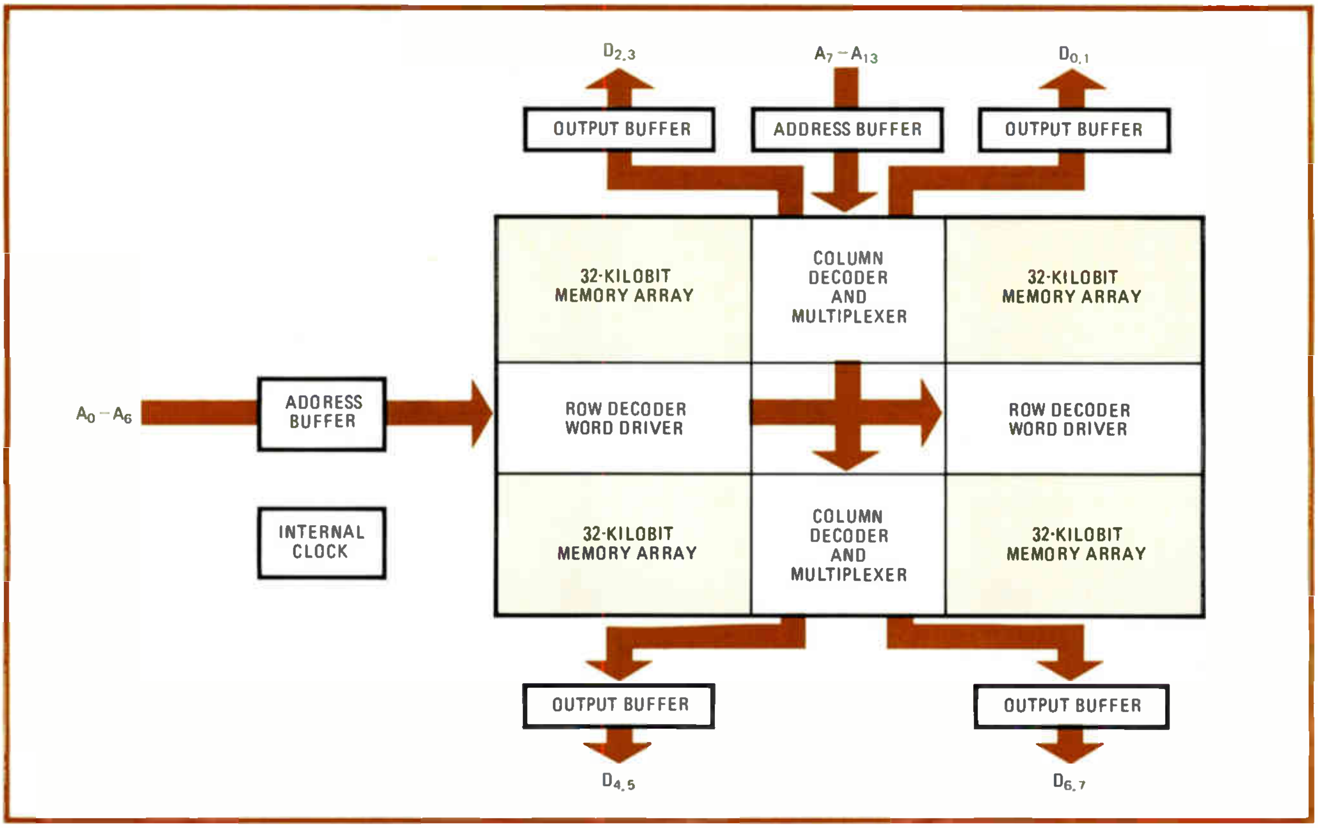
At the VLSI Cooperative Laboratories in Kawasaki, Japan, the emphasis is indeed on electron-beam lithography. A paper presented by the laboratory—one of the few entries on process technology—describes some methods of correcting the scattering of the beam's electrons that exposes unwanted areas during direct-wafer writing. The resultant interconnection of adjacent patterns is called the interproximity effect, while the intraproximity effect describes the rounding of a pattern's corners. To combat both, the intensity of the electron beam is modulated by calculations done in real time. At the VLSI lab, new approaches vastly reduce the extent of the calculations necessary.

For interproximity effects, representative points midway between a given pattern and all adjacent patterns are located. Then whenever the beam crosses those points, its intensity is lowered. Such an approach has the advantage of low computation time, since only at those points need high-speed, real-time arithmetic be performed.

Corner-rounding, or intraproximity effects, can be rectified by varying the dose and beam centers in accordance with the pattern size, says the VLSI lab: for pattern geometries of less than 0.5 μm the beam must be moved outside each corner and the beam intensity lowered; for 0.5- to 2.0-μm geometries the exposure can be right on the corner, but dosage must still be reduced; for geometries of more than 2 μm the exposure at the corners can be a constant full dose.

Logic and memory for the computer

Gaining popularity as replacements for lots of small- and medium-scale integrated logic circuits, master-slice logic arrays are taking many shapes. A paper from Hitachi describes one of the biggest yet: a 5,122-gate device built with integrated injection logic (I^2L). To



3. Big ROM. NTT'S 128-K read-only memory, split into four arrays that provide access to 16,384 bytes, has 65-square-micrometer cells. Writing directly on the wafer, an electron beam programs each device in mid-fabrication by altering its nanosecond thresholds.

reduce voltage drops in injector lines, ground lines are added to keep gate delays on the large (25.4-mm²) chip to 10 ns for an injection current of 100 microamperes.

The chip comprises 124 basic block cells placed around two programmable logic arrays (PLAs). Each block cell consists of a D-type flip-flop, 22 I²L device-islands for random-logic, and four wiring channels. The PLAs each have 35 inputs and 15 outputs, and product terms can be linked between the two. A line-control unit for computer terminals has been built with the chip, says Hitachi, that replaces 59 transistor-transistor-logic packages with one 42-pin dual in-line package. Using both PLAs and 107 of the 124 basic blocks, the design draws only 300 milliwatts at an 8-MHz operating frequency.

Another paper by Hitachi describes a pair of very high-speed bipolar memory chips used by the Japanese manufacturer in its new M-200H mainframe computer. The two chips are designed to work together to boost the speed of table-lookup and address buffers, and hence the speed of processor execution.

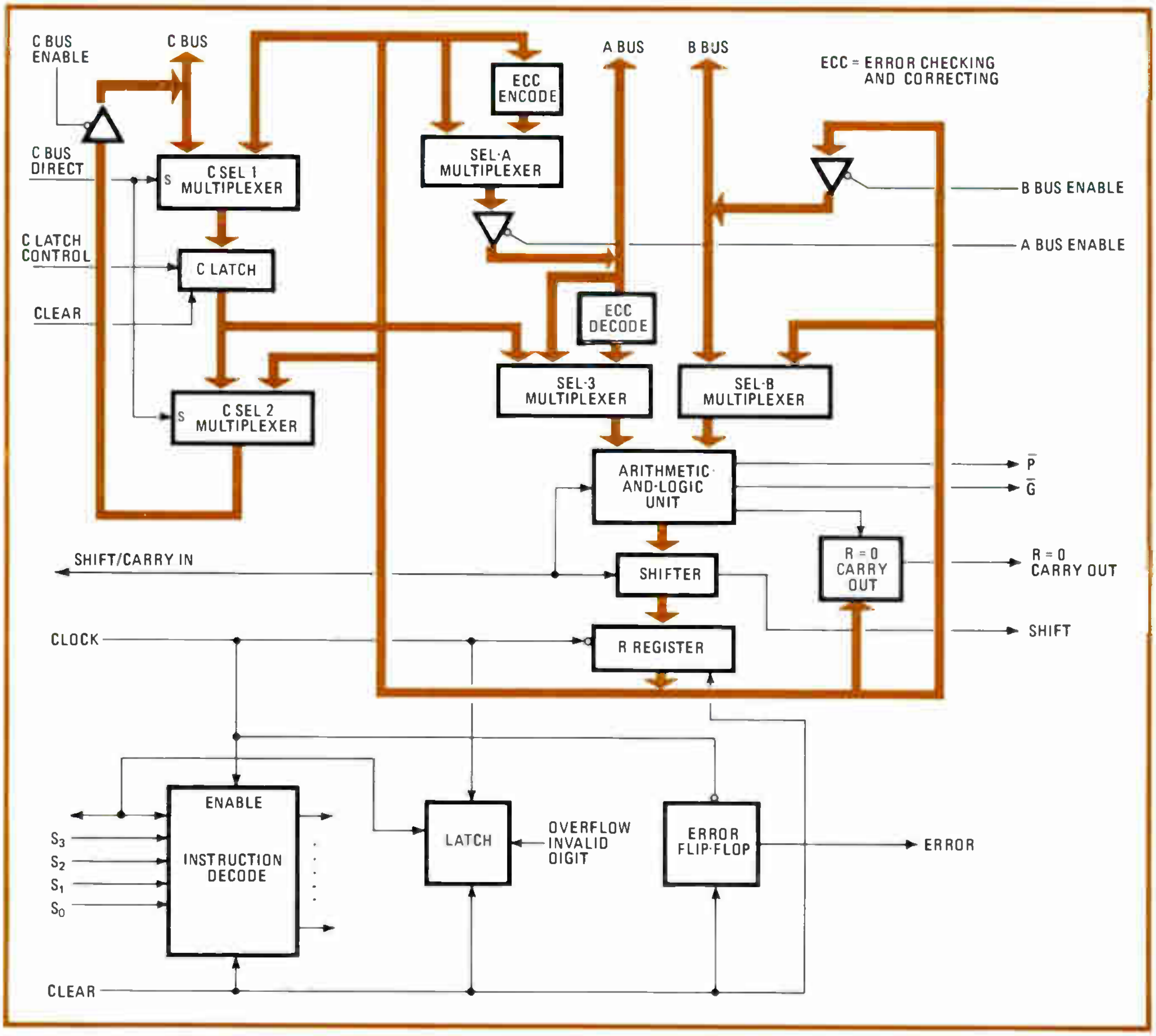
The pair consists of an index-array chip, which mixes 3,072 bits of RAM with 470 logic gates, and a super-fast 1,024-by-1-bit RAM. The mixed chip has an access time of 6.7 ns and typical power dissipation of 3.9 W. The straight RAM has a typical access time of 5.5 ns—the fastest ever recorded, according to Hitachi—yet dissipates only 800 mW.

The index-address chip represents a completely new bipolar memory approach for mainframes. It includes not only the usual peripheral circuits for its memory array, but additional logic for compare functions, which are usually done off chip and thus add propagation delays. The new approach can achieve fast dynamic address translation and cache control.

Basically, the index-array chip is arranged into two sections, each with four 64-by-6-bit RAMs. Although it can function normally as a 256-by-6-bit RAM, it provides in addition parity-checking outputs and a compare output, which indicates whether the word addressed in its memory is the same as one present at its inputs. The combination of logic and RAM boosts the throughput of mainframe buffer memories so much that the idea of such "smart" memories will probably catch on and percolate down even to the microcomputer level. Both the index array chip and the 1-K RAM use the same bipolar process: an oxide-isolated technology with two layers of metalization.

Enter the 8-bit slice

Also oriented towards mainframes is a new bit-slice family from Fairchild Camera and Instrument Corp., Mountain View, Calif. Built with Fairchild's Isoplanar emitter-coupled logic and compatible with the 100K subnanosecond logic family, four new 8-bit slice parts



4. Byte slice. The start of the 8-bit microprocessor slice family, Fairchild's address- and data-interface unit boasts the densest emitter-coupled-logic design yet. The part has an 18-nanosecond cycle time and is compatible with the 100K logic family.

are succeeding in pushing the limits of ECL density.

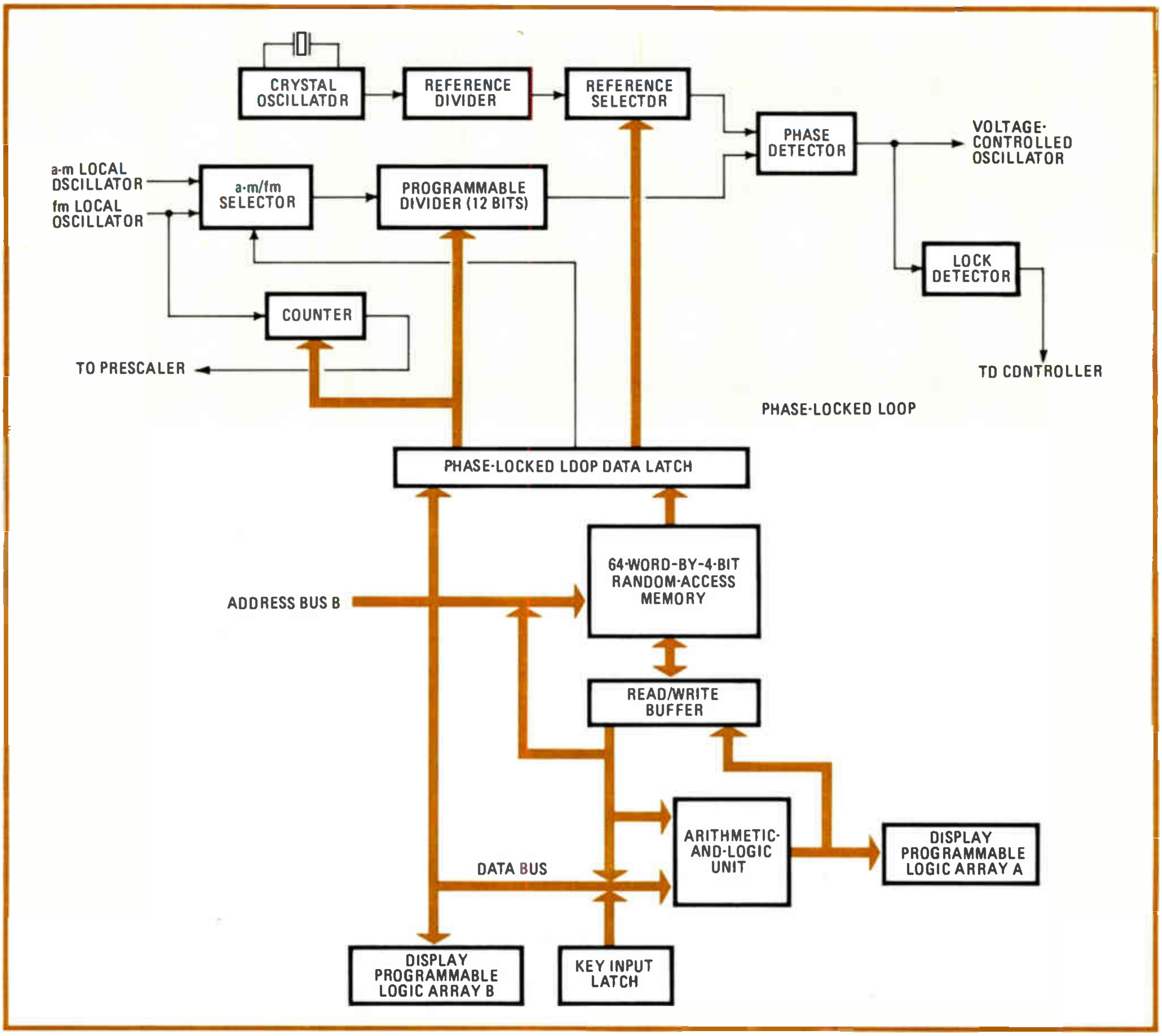
The reasoning behind the development is simple, says Fairchild: what good are internal gate delays of 600 ps if interconnect and package delays are the culprits slowing the system? None whatsoever, says Fairchild—only LSI and a bigger slice can improve the performance.

The first part is the address and data-interface unit, shown in Fig. 4, that handles bus-to-bus data and address transfers, data manipulation, and temporary storage. With three bidirectional data buses of 9 bits each (8 bits plus a parity bit) and a healthy 27-instruction set, the chip can add two 64-bit words typically in 25 ns, with the aid of a carry-lookahead chip. The large (47,000-mil²) chip dissipates a hefty 4.1 w when operating from an 18-ns clock.

The other 8-bit slices include: a multiple-function network containing six 5-bit latches that assists in error checking and correction and register-stack addressing; a dual-address stack of 32 9-bit words; and a programmable interface unit that makes efficient use of a common, time-shared bus through handshaking, parity generation and checking, and three-state interfacing.

Rapprochement on chip

Some of the more dedicated LSI circuit designs at ISSCC are quite intriguing, especially those that mix analog circuits with logic in what can only be the start of a trend towards analog-digital LSI. Consider, for example, a one-chip microcomputer from NEC that has a built-in phase-locked loop (PLL). The circuit has been



5. Microprocessor for radios. NEC digital-tuner chip combines a microcomputer with two phase-locked loops for use in digitally tuned a-m/fm radios. Few other components are needed for a complete radio, as the chip interfaces directly to keyboard and display.

expressly designed for digital a-m/fm radios and packs 15,000 transistors into a 27-mm² aluminum-gate complementary-MOS chip.

Figure 5 shows the chip's organization (the PLL section is the tinted area). Not only does the microcomputer portion have programmable logic arrays that eliminate decoding for the digital display of the station frequency, but its 64-by-4-bit RAM can be programmed with up to 14 preset stations. The chip even contains circuits for a time-of-day clock.

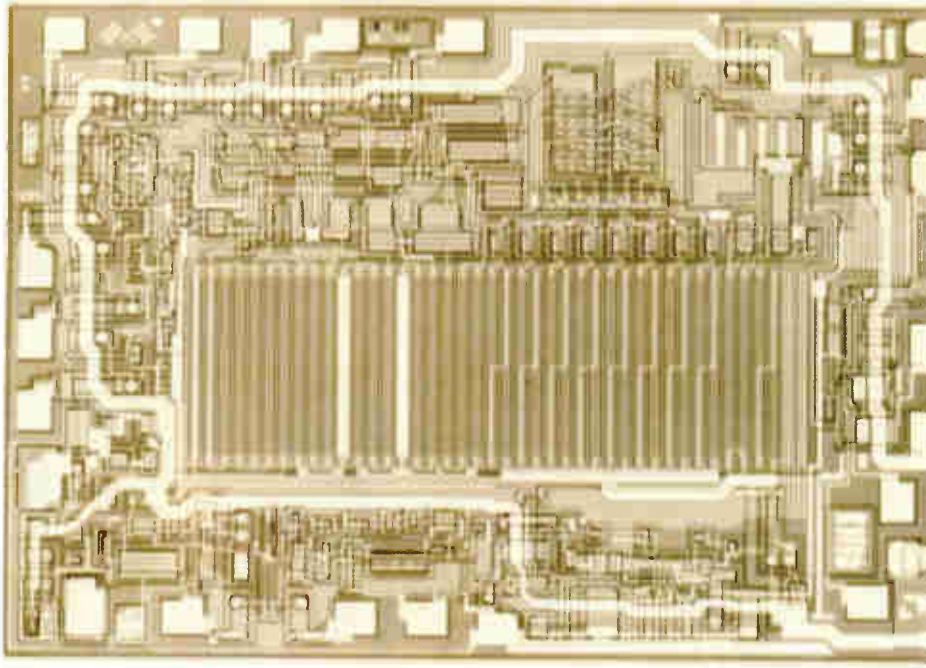
The PLL, driven by a crystal, uses the 12-bit programmable divider in its feedback loop to multiply the frequency of the crystal oscillator. To operate in the frequency-modulated band, a prescaler is needed because the PLL locks on a frequency that is a fraction of the actual rf signal. Few outboard components are needed to complete the digital receiver unit: voltage-controlled oscillators, amplifiers and mixers for the radio-frequency and intermediate-frequency signals, and an audio amplifier and speaker, in addition to the keyboard matrix and display.

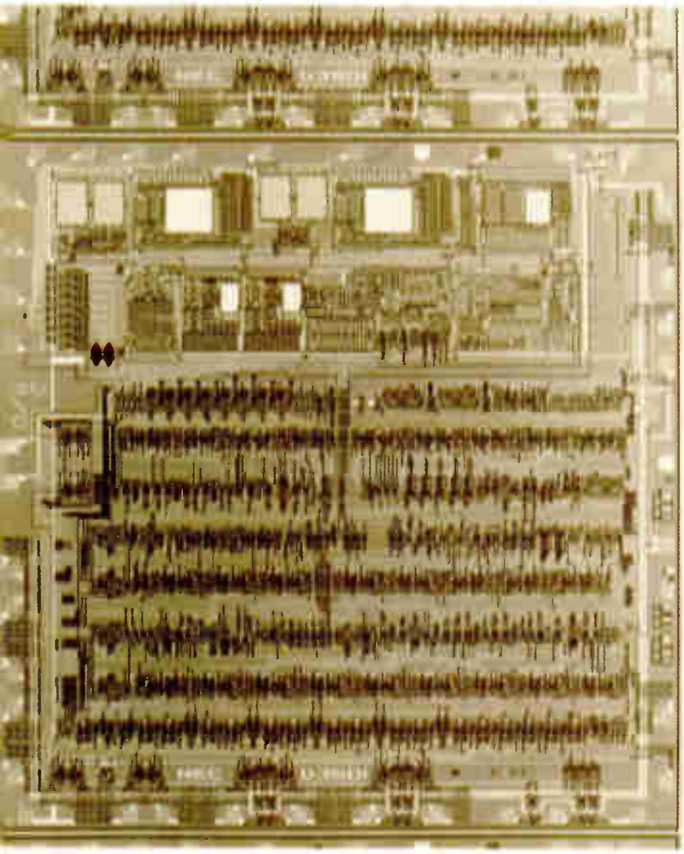
And now an analog microprocessor

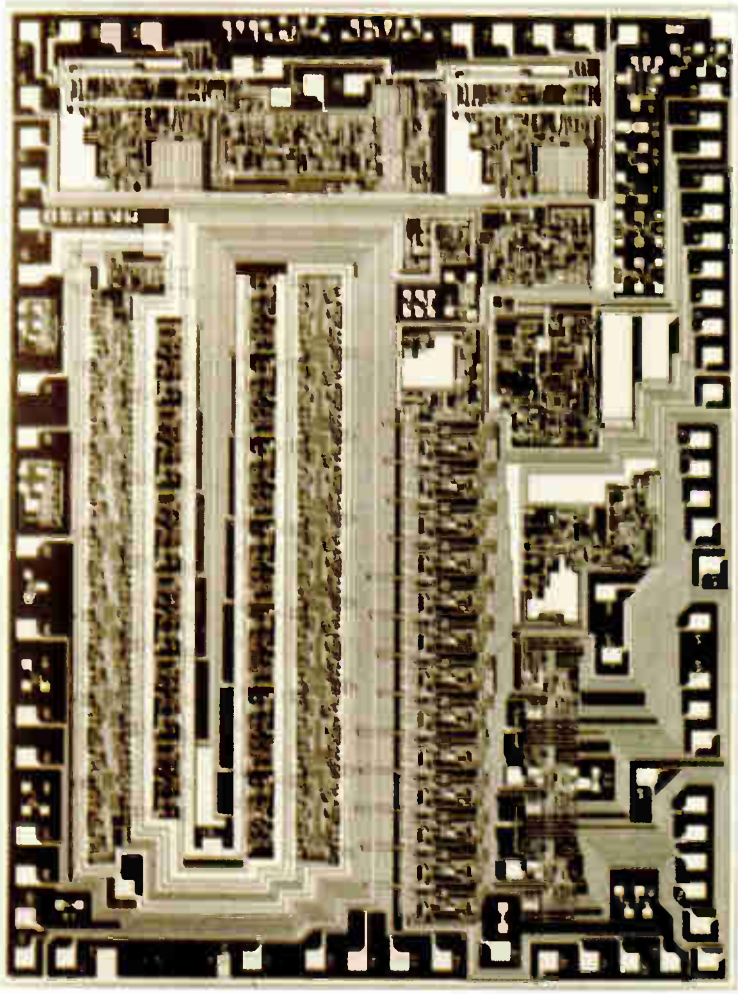
A paper presented by Intel Corp.'s Ted Hoff, one of the digital microprocessor's founding fathers, describes the first analog microprocessor. A breakthrough in signal processing, the chip can serve as the building block for filters, modems, speech synthesizers, and many audio and telecommunications applications. It will be described in detail in the March 1 issue of *Electronics*.

High resolution

Twelve-bit precision converters have made the grade. Going clockwise from top right, Advanced Micro Devices' fast digital-to-analog converter has resistors diffused into the same substrate as the active components, guaranteeing monotonicity to 13 bits and a settling time of 250 ns. Next, Matsushita Electrical Industrial Co.'s 12-bit analog-to-digital converter mixes three technologies: an integrated-injection-logic network is made with the same diffusion steps as high-frequency bipolar transistors and a p-channel metal-oxide-semiconductor sample-and-hold circuit. Finally, Nippon Electric Co.'s 12-bit complementary-MOS simultaneous-integration converter integrates the input signal over eight intervals, improving the signal-to-noise ratio by an order of magnitude, reducing the internal integrating capacitor value, and attaining the high operating bandwidth of 2 MHz.







Performance barriers fall to unique linear designs

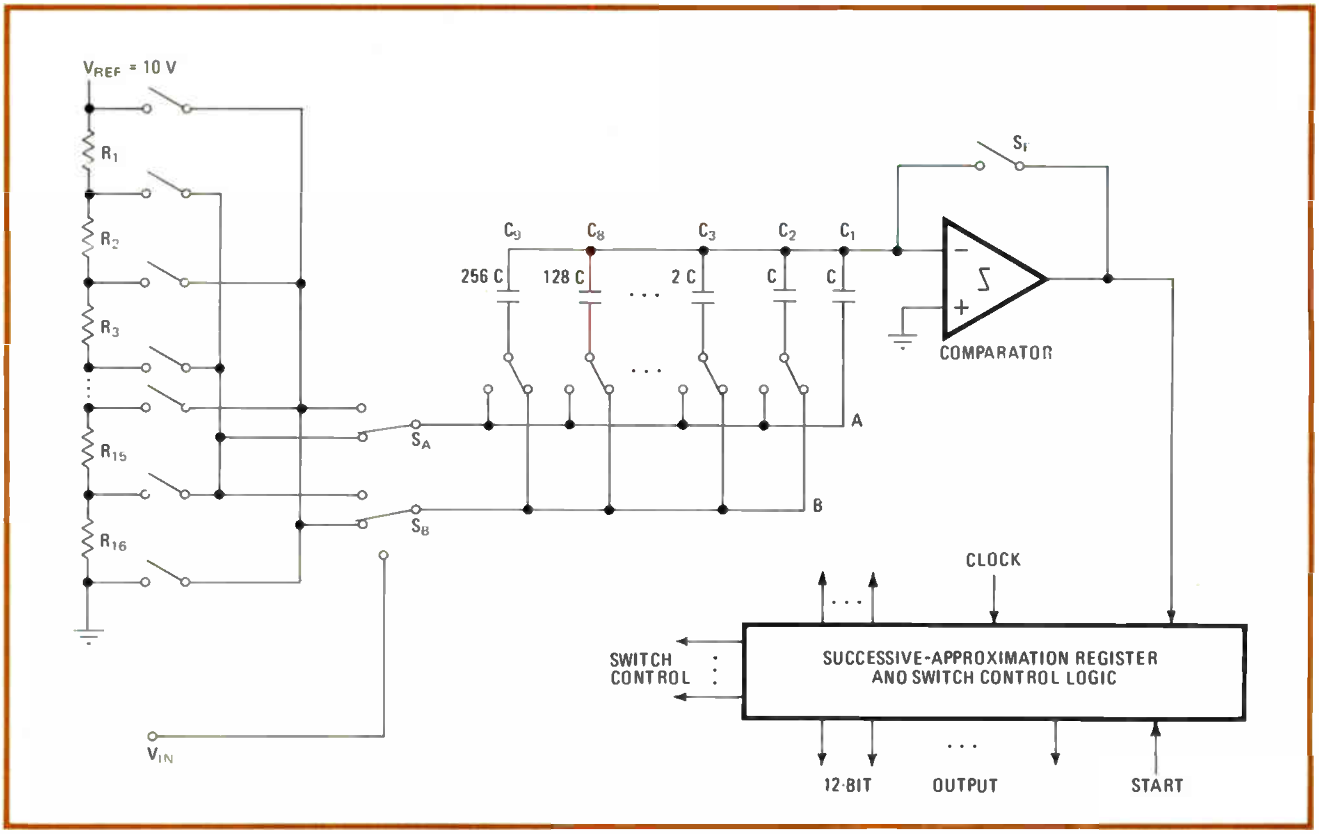
by Nicolas Mokhoff
Components Editor

☐ Interfacing the analog world with today's sophisticated processors demands a matching sophistication, and the importance attached to the area is reflected at this year's conference in four complete sessions and numerous scattered papers. At the two data-acquisition sessions, for instance, it is possible to hear about a variety of high-performance analog-to-digital and digital-to-analog converters as well as a couple of interesting linear circuits for use with converters. Other analog chips tackle jobs in electronic organs and communications—filters are especially active.

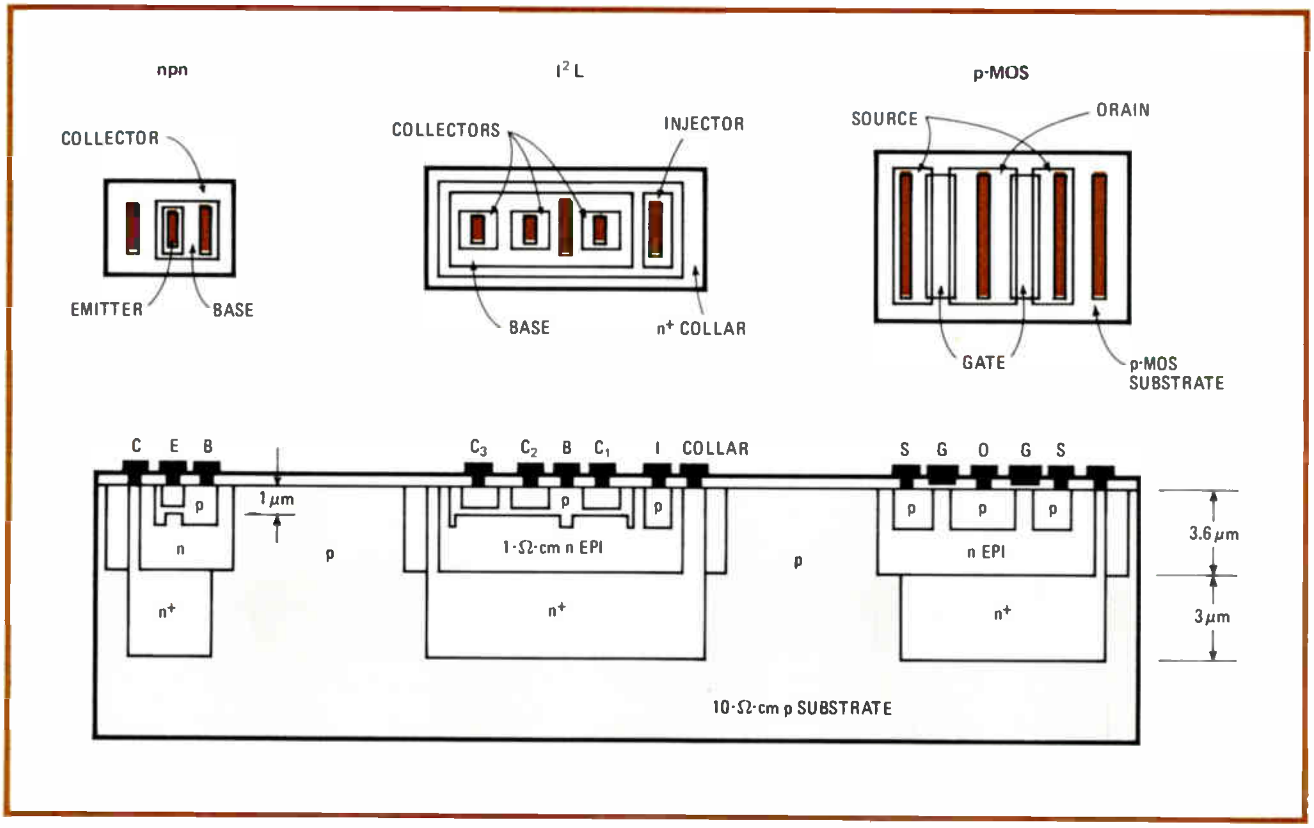
The TRW Defense and Space Systems Group of Redondo Beach, Calif., is working on a fully parallel 8-bit a-d converter that can sample at rates up to 35 megahertz. The traditional sample-and-hold circuit has been eliminated, and that function is implemented instead by 255 sophisticated strobed comparators and associated logic circuitry. Each comparator accepts a different dc reference voltage simultaneously with the input voltage. When the device switches from the sample to the hold mode, all comparators display the results of their comparison independently. Peripheral logic gates develop a 1-out-of-256 code and express it as an 8-bit word. Responsible for the high 35-MHz speed is the use throughout of current-mode logic in combination with TRW's unique triple-diffused bipolar technology, which also boosts yields. The 6.5-by-6.7-millimeter chip contains 17,000 active elements.

Bits by the dozen

In contrast, a 12-bit successive-approximation a-d converter from researchers at the University of California in Berkeley uses only conventional processing to realize its novel circuitry. Implemented in a standard metal-gate n-channel metal-oxide-semiconductor process, the device employs a resistor string to provide a monotonic division of the reference voltage, plus a MOS weighted-capacitor array to subdivide any one of these voltage segments into 256 levels (Fig. 1). The input voltage is sampled and held on the capacitor array by keeping the MOS transistor switch across the comparator closed. Then a search is made among the resistor string taps for the stored sample, and a successive approximation is performed on it once found. By driving the arrays through MOS transistor switches, the researchers claim



1. Weighted-capacitor array. Resistor string divides input voltage into segments, each of which is subdivided by capacitor array into 256 levels. Successive comparison of the stored sample nulls comparator input voltage—array in effect eliminates any comparator offset voltage.



2. Three in one. Novel process produces high-speed npn transistors on same p substrate as an I²L logic network and a sample-and-hold circuit made up of p-MOS transistors. The 6-by-4.6-mm chip contains 1,200 active devices; another chip contains the resistor network.

they have succeeded in eliminating offset errors.

As for fabrication, the 9,000-ohm resistor string is formed in the normal source-drain diffusion of the n-MOS integrated circuit, while the 50-picofarad capacitor array is formed between metal and source-drain diffusion with the thin oxide mask defining capacitor areas. To give the RC charging transients adequate time to settle, a full 25 microseconds are allowed for the 12-bit conversion.

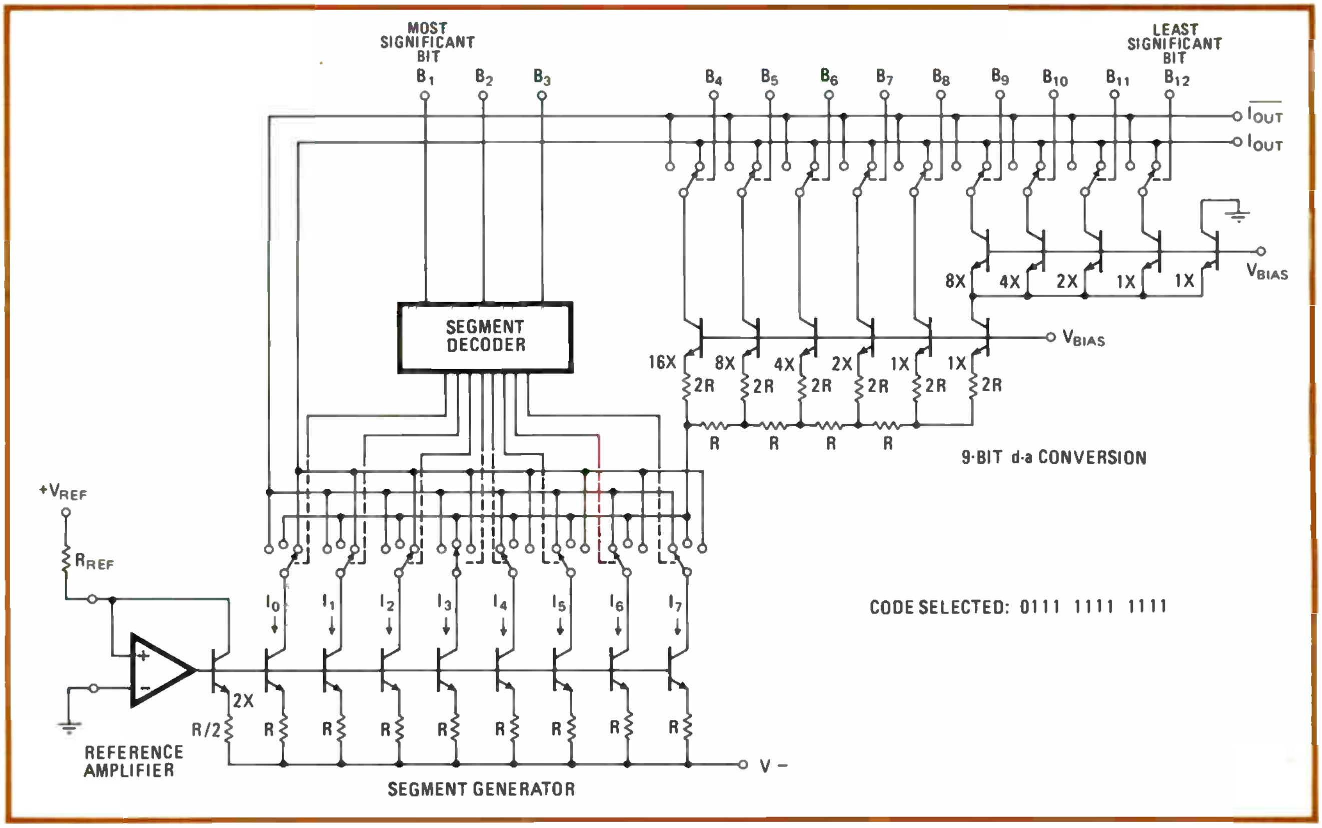
With PCM in mind

A couple of Japanese papers go into detail on a 13-bit converter designed for pulse-code modulation applications and on a 12-bit simultaneous-integration complementary-MOS a-d device. To load a chip with all the elements needed to perform a true 13-bit a-d conversion (Fig. 2), Matsushita Electric Industrial Co. employs a new process that combines three technologies: p-channel MOS for the sample-and-hold circuit, integrated injection logic (I²L) for the comparator and control logic network, and an ion-implanted bipolar process for the high-frequency npn transistors used as output logic buffers. In fact, the p-MOS circuit is also ion-implanted for minimum effect on the bipolar transistor characteristics, and the I²L network is fabricated by the same diffusion steps as the bipolar transistors.

The device actually consists of two chips interconnected in a 40-pin dual in-line package. One chip has a nickel-chromium resistor network vacuum-deposited on it to ensure the 13 bits of accuracy. The other contains 1,200 active devices making up the a-d converter. The combination yields a conversion time of 16 μs, while consuming a mere 1.05 watts.

The 12-bit C-MOS device from Nippon Electric Co. is a monolithic a-d converter employing current-mode analog circuitry. Instead of the conventional dual-slope technique, it uses a simultaneous integration technique, in which the output of the comparator at the end of each preassigned time interval determines either the simultaneous integration of the input current and the reference current or the simple integration of the input current to be performed for each of the subsequent integrating intervals (Fig. 3). Among the significant improvements thus achieved are a much larger equivalent output-voltage range of the integrator, reduction of the external integrating capacitor value, and an order of magnitude increase in the signal-to-noise ratio. The circuit configuration also loads to a relatively fast conversion speed of 500 μs, while dissipating a mere 15 mW of power. The NEC part is a +5-V-only device made from a standard silicon-gate C-MOS structure and claims the same linearity as that of its internal amplifiers—a low 0.02%.

Meeting the challenges posed by the conversion of the output of digital systems is Advanced Micro Devices's



3. No trimming. This 12-bit d-a converter is monotonic because diffused resistors on same chip ensure ±0.01% nonlinearity without trimming. Each of the eight segment resistors carries a current equal to an eighth of full scale and tolerates a ±0.2% mismatch.

entry into the 12-bit d-a conversion field. Enhancing its reputation for making high-speed converters, the Sunnyvale, Calif., company has fabricated a part that it calls inherently monotonic, on the grounds that its diffused resistors need no trimming yet guarantee differential nonlinearity to ±.01% for 13 bits.

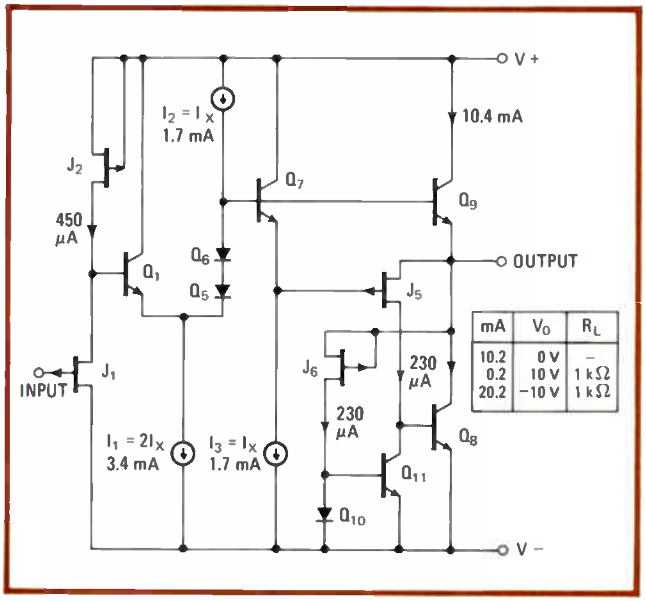
Using conventional bipolar processing, the new design technique combines the advantages of both the R-2R and 2^nR approaches to come up with the monotonic characteristic; but instead of the 37 ladder resistors that would be needed by an R-2R network for 12-bit d-a conversion, or the string of 4,096 resistors needed for a 2^nR network, this part requires only 24 resistors. Eight of these resistors are used as current sources for the 3 most significant input bits, thereby generating eight current segments, each of which is divided into 512 current steps and summed to yield the analog output. As can be seen from Fig. 4, no single resistor determines more than one eighth of the full-scale current, since the slope of each segment is determined by one of eight precision matched current sources. Therefore, full monotonicity is preserved within the tolerance of the diffused resistors, here a ±0.2% mismatch between them. Integrated on a 93-by-134-mil chip, the part is packaged in a 20-pin DIP and consumes 230 to 290 mW, depending on the power supplies.

As for other precision analog devices, one of the most innovative is a 5-A adjustable regulator from National Semiconductor Corp., Santa Clara, Calif. It exhibits good regulation, even when dissipating 100-W transients, by taking thermal gradients into account. This gradient sensing is accomplished by a couple of transistors that increase the available power output without sacrificing overload protection. Load regulation is to 0.05% at 5 A, and the device can be used for output voltage swings of 1.2 to 33 V.

Dealing with heat

These characteristics are achieved by having the power transistor made up of individually ballasted emitter stripes in a base section. The base sections of seven emitters are in turn also ballasted with one of the resistors used for current sensing. This and deep n^+ diffused collector contacts assure the transistor of a breakdown voltage of typically 50 V. The output current sensors are diffused n^+ resistors with a positive temperature coefficient of 0.2%/C°, matched to the gradient sense voltage of the current limit transistors, thereby ensuring a fast current limit cutoff.

Another device that uses a clever design to cancel thermal gradients is a voltage-follower IC from Precision Monolithics Inc. of Santa Clara, Calif. A quasi-quad field-effect-transistor layout minimizes mode capacitances to such an extent that a slew rate exceeding



4. Quasi-quad. Open-loop design has a quasi-quad configuration in which a pair of eight-channel FETs are separated into two four-channel segments. This retains the advantage of common centroids while limiting capacitance and yielding a 300-V/μs slew rate.

400 V/μs is achievable. In effect, instead of two sets of four separate channel segments for current distribution, the device is split into two sets of four four-channel segments. This configuration retains the benefit of common centroids, yet it holds capacitance well below that of a pure quad layout, since the capacitance generated does not lie in the signal path and therefore is considered negligible. The upshot is a monolithic voltage follower specified for a 90-MHz bandwidth, a slew rate of 300 V/μs, and an offset voltage of 1.5 millivolts.

Also from Precision Monolithics is an example of how a mixed technology can greatly enhance device characteristics. It is a temperature-compensated quad analog switch IC fabricated with a bipolar and field-effect-transistor process. Unlike the on-resistances of its C-MOS and junction-FET counterparts, which fluctuate extensively with variations in applied voltage and/or in temperature, the 85-ohm on-resistance of this IC remains virtually constant when it is operated at low currents: its drift is on the order of 400 ppm/C° at 125°C. A protection circuit guards the device against loss of power and against voltage excursions of 20 V beyond the specified input voltage limits.

Sound distinctions

Several exotic linear integrated circuits have been designed for special applications. Japan's Matsushita Electric Industrial Co. has developed an analog LSI chip that generates tone signals with even and odd harmonics and exhibits the hyperbolic decay envelope of conventional musical instruments. The MOS analog LSI chip comprises resistive-source MOS devices and sawtooth dividers using modified R-2R networks. The resistive-source MOS device acts as a variable nonlinear impedance element that enlarges the decay time control from 25 milliseconds to the 2 seconds needed for applications in electronic organs.

Sawtooth wave dividers generate the even and odd harmonics that color the signal source and mellow the musical tone. The IC has five- and six-octave tone-generator circuits of three independent musical notes. Combining four LSI chips would be enough to cover the full 61-key keyboard of an electronic organ.

Cheaper tuning

Another consumer-oriented IC comes from Toshiba Corp.'s Research and Development Center, which has developed a monolithic device for wideband frequency converter applications in a very high-frequency television tuner. Using a silicon-nitride passivation self-aligned (NSA) bipolar process, the Toshiba engineers were able to put a mixer plus an oscillator plus an intermediate-frequency amplifier on one piece of silicon. The NSA process enables high-frequency bipolar transistors to have a 2-micrometer emitter width, a cut-off frequency of 5 gigahertz, and a collector-to-emitter on-voltage of 20 V. In effect, linking this 34-decibel-gain chip to a MOSFET radio-frequency amplifier chip would satisfy the specification for a solid-state tuner and thereby both miniaturize and cut the cost of a conventional TV tuner.

Also in the consumer area, General Instrument Corp.'s Microelectronics division in Hicksville, N.Y., has come up with an LSI version of a versatile programmable sound generator. The n-channel metal-gate chip measures 144 by 159 mm and comes in a 40-pin DIP. Compatible with most microprocessors, it requires no external timing components to generate sound, this data being stored in program ROM and on occasion in data RAM. The completely software-controlled device consists of an unlikely quantity of registers, data converters, and buffers, as well as peripheral logic circuitry, all under one roof.

Included in this year's linear circuit techniques session is a paper on an IC that has been available for some time as a standard off-the-shelf item but that has some unique features. The 4200 analog multiplier from Raytheon Co.'s Semiconductor division in Mountain View, Calif., marries a well-known analog multiplier/divider concept to a novel on-chip nonlinearity cancellation technique. Since virtually all the nonlinearity caused by the emitter resistance of the transistors is eliminated, the chip's nonlinearity errors are less than 0.03% over a signal bandwidth in excess of 3 MHz.

Current-mode operation is set up by three high-speed differential input amplifiers so configured as to multiply two input currents, divide the result by a third input current, and output the result as a signal current. This design embodies the log-antilog principle that utilizes the logarithmic current-voltage transfer characteristic of the bipolar transistor.

Telecommunications has made its presence felt sharply in the device world this year, in the form of monolithic active filters, intended mainly for use with last year's ISSCC stars—codecs. In fact, integrated filters for telecommunications are the subject of a panel discussion chaired by P. R. Gray of the University of California at Berkeley. In addition, a number of people are turning a fairly well-known concept—the switched-capacitor filter—into a reality. A small capacitor when switched rapidly resembles a high-value resistor, allowing just capacitance ratios themselves and a check frequency to simulate very stable RC networks. The required switches can now be easily implemented with small MOS transistors, and signal voltages can be sensed with readily available FET input amplifiers fabricated in either n-MOS or C-MOS. All that remains is to put the ingredients on a single chip.

A switched-capacitor filter is at present a part of a two-chip pulse-code-modulated voice coder made by American Microsystems Inc. of Santa Clara, Calif. The circuit consists of a low-pass section of a fifth-order-elliptic ladder-simulation filter type, a novel high-pass state-variable section, and a low-pass elliptic type constructed from two third-order sections connected in tandem. The innovative high-pass section has a design based on the bilinear Z transformation, which unlike designs using analog modeling, does not distort the filter frequency response.

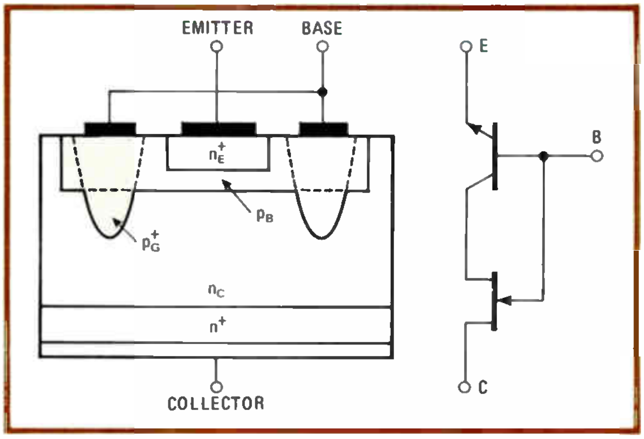
The chip is a combination of n-channel and C-MOS processing with thin-oxide polysilicon-to-metal capacitors fabricated in both. Operating off ±5 V, the device can sample at a maximum rate of 128 kilohertz.

Another application for switched-capacitor filters is being tried by a newcomer to the field of telecommunications—Silicon Systems Inc. in Irvine, Calif. This custom house has fabricated a C-MOS LSI version of a dual-tone multifrequency (DTMF) receiver for Touch-tone telephones (see p. 105). As today's DTMF receivers carry too large a price tag to be used anywhere except in shared private branch exchanges and switching centers, this novel monolithic chip now affords the chance for service on a telephone-by-telephone basis.

A color-TV imager

Some of the more exotic single-chip implementations of complex functions are to be found at the session on solid-state imaging and biomedical applications. Out of Hitachi's Central Research Laboratory comes a 484-by-384-element MOS imager intended for use in a color camera and exhibiting television-like resolution. The 484 rows are on 20-μm centers and the 284 colums are on 34-μm centers, yielding a horizontal resolution of 260 TV lines and a vertical resolution of 350 TV lines. The peripheral circuits consist of a vertical scanner with the interface circuit and a low-noise horizontal scanner using bootstrap capacitors. The device employs a 7.2-MHz horizontal clock rate.

In an effort to build a close-to-ideal transistor exhibiting both high emitter-to-collector breakdown voltages



5. Gate-associated transistor (GAT). When the gate of a field-effect transistor is grafted onto the base of a standard bipolar device, it is possible to build a high-breakdown-voltage transistor with the narrow base essential for high-frequency performance.

and high cut-off frequencies, researchers at Mitsubishi Electric Corp.'s Semiconductor Laboratory in Japan have come up with a literally hybrid device—a field-effect transistor grafted onto the base of a standard bipolar transistor. The base region of the new device is divided so that part of it operates as an ordinary base and part is doped with a higher impurity concentration and projects into a collector region (Fig. 5). This latter part acts as the gate of a JFET in the off condition, giving the device its name—gate-associated transistor, or GAT.

The gates in the collector region punch through at a lower voltage than the base does. As in a triode vacuum tube, the base region is electrostatically shielded from the collector, but the lower electric field strength near the base-collector junction results in no appreciable charge between breakdown voltage and h_{fe}. The new structure clearly is useful for fabricating breakdown voltage transistors with a thin base, a necessity for high-frequency devices. GATs therefore succeed in combining cutoff frequencies of 380 MHz with breakdown voltages of 250 V, useful characteristics for high-power applications.

Impatt diodes are solid-state replacements for such bulky microwave power sources as traveling-wave tubes and magnetrons, but till now they have not succeeded in exhibiting pulsed peak powers of more than 20 W. Nippon Electric Co.'s Semiconductor division, however, has fabricated a diode capable of 50-W peak power output at a 10-GHz band. The device operates at an efficiency of 13% under excitation conditions of a 1-μs pulse width with a 10% duty factor.

The diode is a ring of silicon with a p^+-pn-n^+ vapor-epitaxially-grown double-drift region. The 20-μm-thick wafer has titanium/platinum/gold film evaporated on both sides, is mounted on a diamond heat sink, and is hermetically sealed in a 3-mm-diameter ceramic package—quite a difference in size from the bulky magnetrons of the past. □

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C-MOS a-d converter surges to bipolar speed on sapphire substrate

by Daryl T. Butcher, *Electronics Research Center, Rockwell International Corp., Anaheim, Calif.*

☐ When monolithic analog-to-digital converters make use of conventional complementary-metal-oxide-semiconductor technology, they can resolve 12 bits—but only at the slow speed characteristic of C-MOS. Silicon on sapphire, though, is one form of MOS technology that equals or exceeds the high performance of bipolar large-scale integration.

The C-MOS-on-sapphire a-d converter shown in Fig. 1 promises to outdo converters processed in integrated injection logic and other advanced bipolar linear and digital circuits. Yet it retains the low power consumption and excellent analog switching capability of C-MOS. For a 12-bit conversion at 5-megahertz speed, it consumes only 15 milliwatts.

Basic to such a fast successive-approximation a-d converter is a fast comparator. To build a comparator that would extract all the speed and power advantages possible from using a sapphire substrate, it was first necessary to characterize and develop MOS transistors on sapphire that performed comparably with bipolar devices. This and the rest of the work on the converter were carried out at Rockwell International Corp.'s Electronics Research Center under a program funded by the military since 1975.

The pros and cons of sapphire

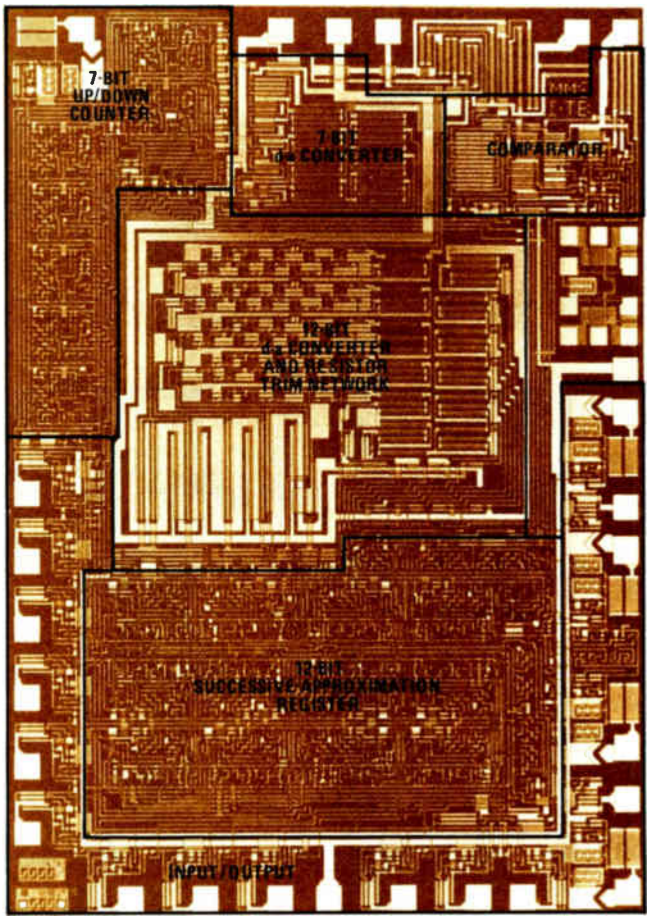
From the outset, it was clear that the construction of MOS transistors on an insulating sapphire substrate results in mixed blessings.

On the one hand, parasitic capacitances are greatly reduced, so that the devices attain very high switching speeds. Also, the complete device isolation eliminates body effects and simplifies the design and construction of circuits that require transistor sources to operate at potentials other than the power supply voltages. On the other hand, the dielectric isolation not only creates island edge effects and adds a second insulator interface at the back of the transistor, but it also introduces the "kink" phenomenon (Fig. 2).

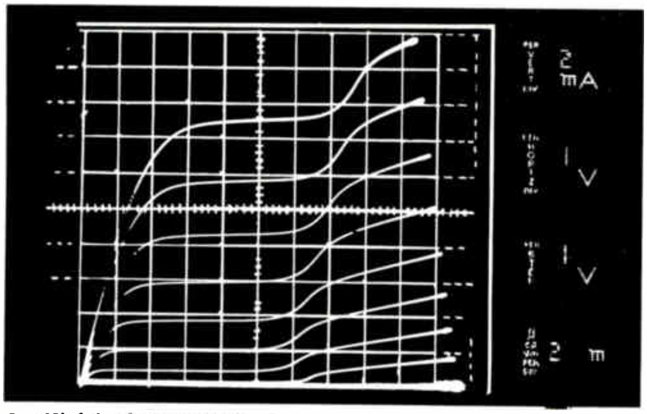
This phenomenon is a nonlinear transfer characteristic caused by leakage and drain-to-body avalanche currents. When the leakage and/or currents modulate the body voltage in an SOS n-channel device, they cause a rapid increase in output conductance for drain voltages between 4 and 8 volts. The high drain conductance results in a low voltage gain for the device. The voltage gain factor for typical devices (μ in vacuum tube terminology) is limited to less than 50.

Another drawback of SOS devices is that extremely large chip areas are required to achieve even moderate transconductances—hundreds of micromhos. Simple resistive-loaded gain stages are therefore limited to gains of less than 100 (for usable bandwidths). Active-load gain stages also appear useless because of the unfavorable output impedances for both n and p devices.

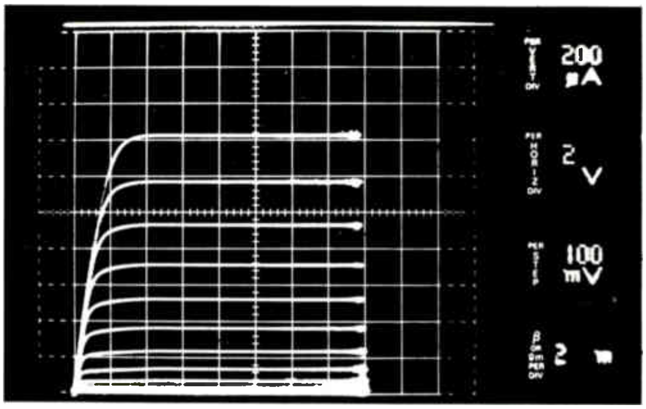
Finally, when manufactured with MOS technology, the



1. High density. C-MOS-on-sapphire 12-bit a-d converter occupies 115-by-150 mil chip. The on-chip comparator, the offset voltage correction circuit, and the precision chrome-silicon resistor network between them ensure the device's 12-bit performance.



2. "Kink" phenomenon. Caused by leakage and drain-to-body avalanche circuits (I_{DB}) that modulate the body voltage in SOS n-channel devices, the kink is a highly nonlinear transfer characteristic. Output conductance increases rapidly between 4 and 8 V.



4. Negligible kinks. The kink phenomenon is defeated by using a composite amplifier stage whose transconductance is determined by an enhancement-mode device with a relatively short channel length. The stage can achieve a μ of > 10,000.

matched differential amplifier pairs that are fundamental to comparator functioning have in general poor noise characteristics and also high offset voltages, in the region of tens of millivolts. In both respects they are much inferior both to junction field-effect and to bipolar transistors and become still worse when they are fabricated on a sapphire substrate.

Revival of the tetrode

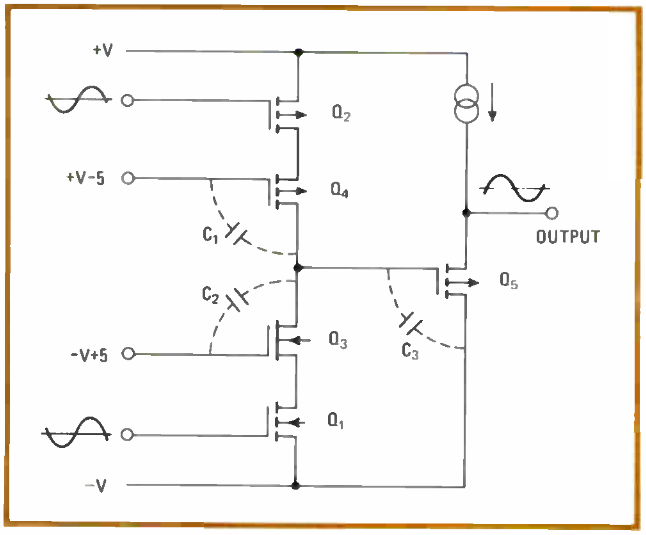
To develop a useful MOS-on-sapphire amplifier and hence comparator, a circuit concept from vacuum-tube days was revived. This structure (Fig. 3) defeats the kink phenomenon and produces an amplifier with very high output impedance (Fig. 4). When complementary tetrode devices are used as the double-to-single-ended stage of a differential operational amplifier, a node impedance of greater than 10^8 ohms and a voltage gain in excess of 80 decibels are obtained. Also, a single-pole amplifier built in this way achieves the exceptional gain-bandwidth performance indicated in Fig. 5.

The amplifier's bandwidth is determined by gate overlap capacitances C_1, C_2, and C_3. (No separate outside capacitor is needed to stabilize the device.) A metal-gate process yields a high-performance amplifier but, to minimize the overlap capacitance and thus maximize gain-bandwidth performance, a self-aligned silicon-gate construction was preferred. The level of performance thus achieved requires a power dissipation of 5 to 10 mw, which turns out to be the greater part of the converter's power consumption.

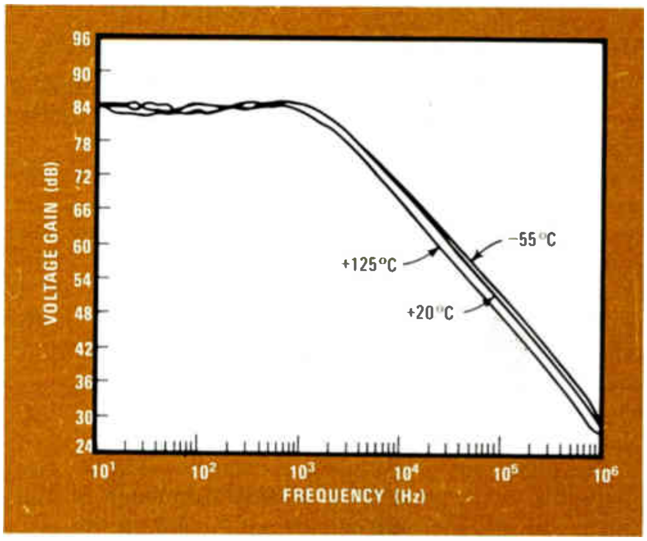
A high slew rate

The amplifier slew rate is also outstanding: 50 volts per microsecond is achieved when source-follower transistors with a relatively large (high-capacitance) output are used. When the amplifier design is modified for implementation with silicon-gate devices and smaller output devices are used, a maximum slew rate of approximately 5,000 V/μs is theoretically possible.

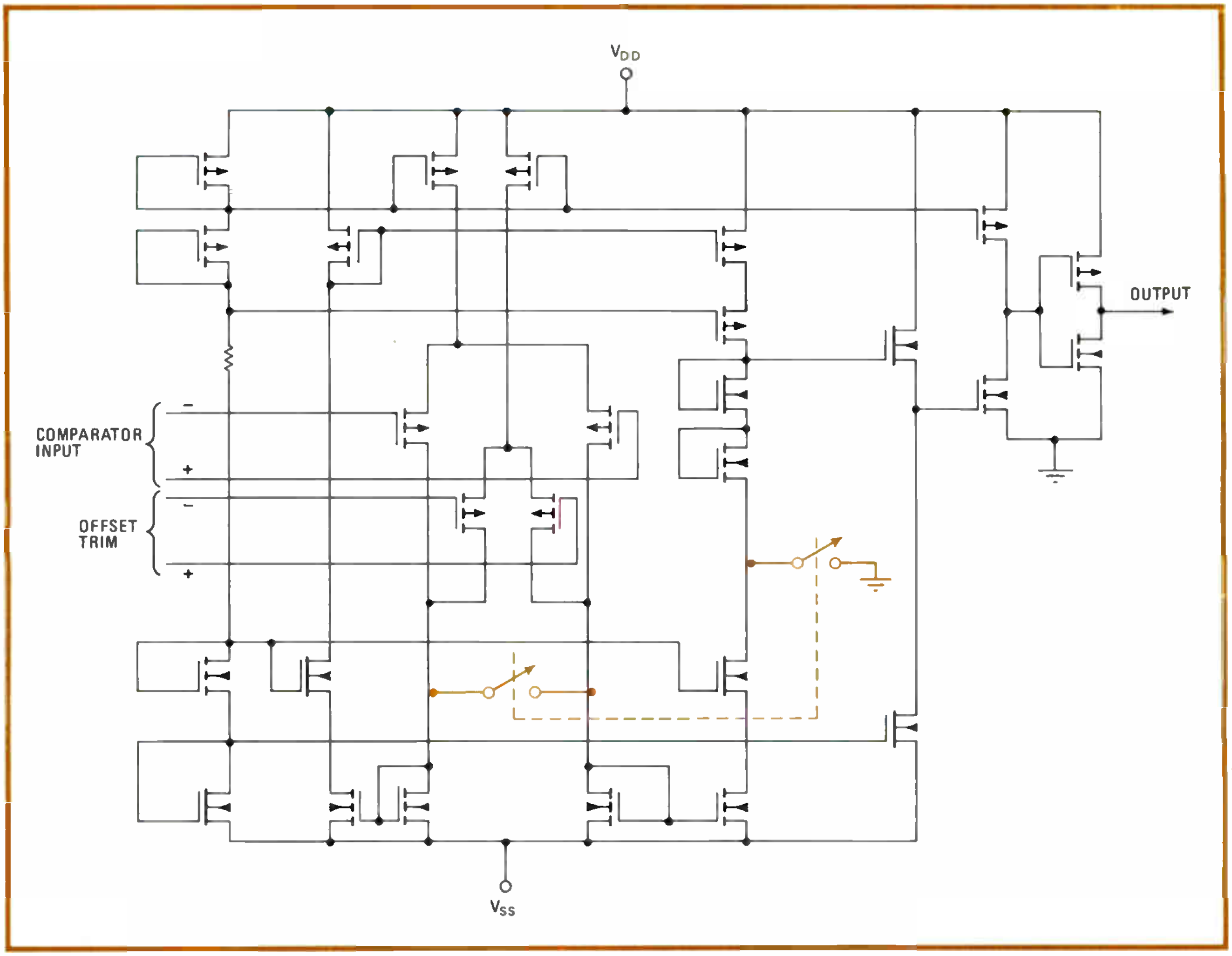
In an actual a-d converter, the slow rate has to be very



3. Complementary tetrode amplifier. The high-gain SOS amplifier converts in-phase voltage signals into push-pull currents in the Q_1, Q_3 and Q_2, Q_4 stages. A 10^8-ohm impedance at the Q_2 and Q_4 drains yields an 80-dB-plus voltage gain. Q_5 is used as an output buffer.



5. High gain-bandwidth. The complementary tetrode amplifier structure makes possible a single-pole amplifier, which achieves the unusually good gain-bandwidth product shown here. The bandwidth is determined by the overlap capacitances shown in Fig. 3.



6. Operating details. Comparator uses dual-differential input stage and current mirrors to supply input signals to a complementary output stage. Critical nodes shorted to their nominal operating points allow excessive voltage excursions only when a comparator decision occurs.

responsive under small-signal conditions. This design resolves a 1-mv input differential in 50 nanoseconds—amply fast enough for a very high-performance a-d converter. In combination with the low power dissipation of 5 to 10 mW, this speed gives the device speed-power performance much superior to any previously available.

Also to be considered

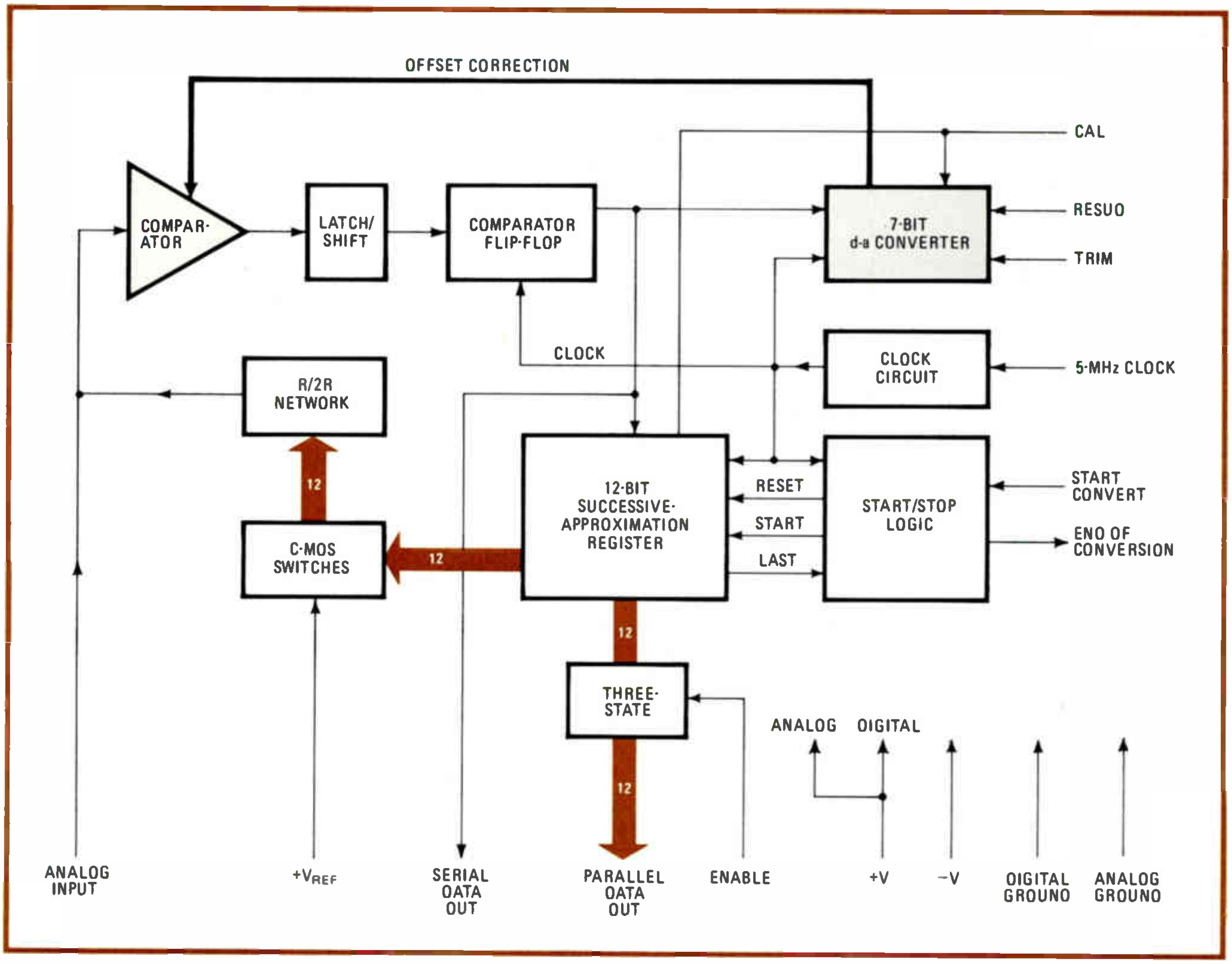
But unusually good bandwidth and slew rate are not sufficient for superior comparator performance. Overload recovery must also be minimized. In the silicon-on-sapphire technology, junction storage is not a problem, since the isolated majority-carrier transistors have negligibly small charge-storage times; however, electrical voltage excursions must be limited to minimize charge/discharge recovery periods. In the comparator used for the 12-bit converter, these effects are eliminated altogether by shorting critical nodes to their nominal operating points during the major portion of each clock cycle, thus allowing excursions from these conditions only during the brief period when a comparator decision is required (Fig. 6).

The a-d design problem, then, becomes tolerable when a high-speed comparator is available. However, several other obstacles must be overcome. The comparator offset voltage must be reduced to a fraction of the signal weight of the least significant bit. In addition, a method must be established for generating successive-approximation signals.

Several advances have recently been made in weighted-capacitor or charge-equalization conversion. But SOS technology, suffering as it does from relatively high device leakage, is not readily adaptable to this approach. So it seemed preferable to use a conventional Kelvin resistor network to add up the binary-weighted voltages of successive approximation.

The resistor network

This decision nevertheless created new design challenges. Resistors are more difficult to produce with high relative accuracy than capacitors. Further, resistor as well as transistor temperature coefficients must be accommodated by the design. Since diffused silicon resistors typically exhibit poor temperature stability for a full 12-bit conversion, a chrome-silicon resistor process was chosen that has a typical temperature coefficient of resistance of 30 parts per million per °C. The resistors are trimmed employing laser burnout of metal links.



7. The system. The complete 12-bit a-d converter is organized conventionally, except for the incorporation of a 7-bit d-a converter for on-line offset voltage correction. The only functions not supplied on chip are clock input, reference voltage, and certain control signals.

Micropads incorporated in the resistor network enable the trimming to be performed during fabrication.

The a-d converter clock diagram is shown in Fig. 7. The organization is conventional, except for the use of a 7-bit d-a converter for offset voltage correction.

Offsetting offset

Offset voltage adjustment had to be effective over the military temperature range (−55° to 125°C) and even over radiation environments, so that an initial trim is not sufficient. Since the on-chip 7-bit d-a converter tracks continous changes in offset voltage, the 12-bit converter's offset voltage can undergo dynamic correction over a range wide enough to cope with such offset-voltage–varying environments as boost-ballistic, reentry or satellite radiation.

Furthermore, an additional system benefit is afforded by the offset-correction circuitry because it rids the comparator of 1/f noise (which may be viewed as an instantaneous offset voltage). The offset-correction d-a converter can be set to midrange, allowed to track the offset voltage continuously, or allowed to update the offset correction following each conversion period (the modes are controlled through the CAL, RESUD and TRIM inputs of Fig. 7). The last mode of operation requires one additional clock cycle per conversion.

The device requires a clock input, control signals for conversion and data output, and a reference voltage. These functions were not supplied on chip because initial systems applications required synchronous and ratiometric operation using several converters and a common clock and reference. Here, also, the use of a common reference is helpful in keeping system power requirements to a minimum.

The results

Initial devices have demonstrated performance levels very near the converter design objectives. These included a conversion speed of 2.5 μs for a 12-bit precision conversion, observed from the very first process wafer. The 15-mW average power dissipation was maintained despite the use of on-board offset voltage correction and other logic circuits. The converter operates off ±10 V and accepts input signals of a 0-to-10-V range.

The initial design is slated for use in a high-performance developmental satellite system. Commercial realization of C-MOS-on-sapphire a-d converters is not planned by Rockwell at this time. □

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64-K dynamic RAM has pin that refreshes

Single signal controls automatic- and self-refresh modes; design simplifies peripheral circuitry, needs only +5 V

by David C. Ford, Dick Brunner, and Jerry Moench, *Motorola Semiconductor Products Division, Austin, Texas*

□ A tough competitor is joining what promises to be a crowded field for the 64-K dynamic random-access-memory race: the MCM6664. Besides storing 65,536 bits of information in a standard 16-pin package, this RAM's strengths include a fast access time and low power consumption from a single +5-volt supply (Table 1). What will really make this part stand out in a crowd is the refresh control function available on pin 1. This feature provides automatic- and self-refresh modes in addition to the $\overline{\text{RAS}}$-only mode found in other dynamic memories, in which the row-address strobe (RAS) and refresh addresses must be applied to the chip.

Putting the row-address counter and associated logic circuitry on chip means that fewer peripheral chips are required in MCM6664-based systems. A single signal will initiate either of the new refresh modes, depending on the length of time it is applied.

Advances in integrated-circuit design have gotten rid of the need for the −5- and +12-V potential. One of these spare pins is dedicated to the extra address line that the 64-K RAM needs over 16-K parts, and the other is used for the refresh control signal.

This concept makes system design with cost-effective dynamic RAMs almost as easy as with static parts. Now high-density dynamic memories can be designed into systems without the worry of tracking memory locations to be refreshed, generating the correct addresses, or supplying row-address strobes for refresh operations.

The MCM6664 is fabricated with n-channel silicon-gate technology using Motorola's H-MOS, a high-performance, metal-oxide-semiconductor process under development since late 1975. H-MOS is largely responsible for the move to single-supply operation by virtue of the reduced operating voltages required by its high-gain, short-channel-length transistors. The smaller transistors also are responsible for a reduction in capacitance and a subsequent increase in speed, which further gives rise to an enhanced speed-power product.

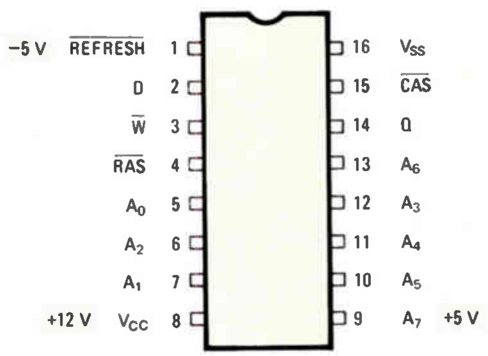
Better bias

The chip also contains a special substrate-bias generator. Traditional substrate-bias generators are free-running; the voltage generated varies in accordance with read/write operations. The MCM6664 has a regulated bias generator using noise-equalization capacitors to produce a more consistent negative potential.

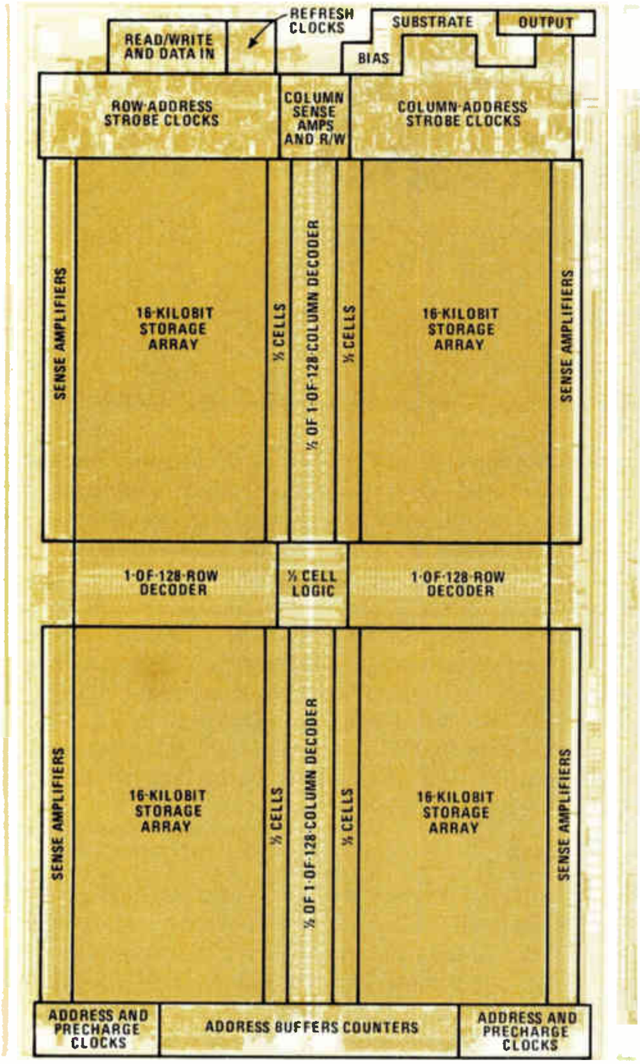
Although substrate bias is not required in a RAM design, it does prevent negative system transients of up to −1.5 V from destroying information stored in the memory. The negative bias also decreases the junction

TABLE 1: THE MCM6664 64-K RAM AT A GLANCE

- industry-standard pinout:



- single +5-V operation
- 150-ns operation
- low power drain (< 300 mW)
- fully compatibility with transistor-transistor logic
- three-state output
- internal latches for address and data input
- early-write output capability (for common input/output)
- 128-cycle, 2-ms refresh
- control on pin 1 for automatic refresh and self-refresh
- $\overline{\text{RAS}}$-only refresh mode
- pin-compatible with the 16-K RAM (MCM4116 pin designations in gray)



1. Die. The MCM6664, Motorola's 64-K dynamic RAM, has four memory arrays, each 128 bits square, with a resulting 128-cycle, 2-ms refresh period. The chip uses high-performance MOS technology, which is largely responsible for its +5-V-only operation.

capacitance, and since much of the device's power dissipation is the product of capacitance and voltage, the overall active power consumption drops when a substrate-bias generator is used.

Layout

Figure 1 shows the functional sections of the MCM6664 and represents their approximate position on the die. The RAM was designed with conservative dimensions to enhance producibility. The die, which measures 145 by 260 mils, uses 3-to-4-micrometer geometries and projection printing on all levels to reduce defect densities and improve uniformity.

A total of 512 sense amplifiers are on the chip for a 128-cycle, 2-millisecond refresh period. The sense amps are precisely matched, both topographically and electrically, to allow for variations in alignment and device characteristics.

An easier approach would have been to halve the number of sense amplifiers, potentially reducing the power dissipation, and perform a 256-cycle, 4-ms refresh. This would yield the same refresh overhead. However, 128 cycles is the same refresh scheme that 16-K RAMs use, which makes substitution easier. Moreover, the MCM6664's approach provides better noise immunity. The signal-to-noise ratio is greater because of the higher-level signals allowed by the shorter refresh time and because each 16-kilobit block of memory has its own bank of sense amplifiers.

Improved noise immunity also stems from the electrical isolation of the sense amplifiers from the bit-sense lines before signals present on the lines are detected. This isolation yields better sensitivity, or noise immunity, because charge is not stolen from the bit lines (see "Folded bit-sense lines reduce alpha errors," p. 143).

Another bonus is that no active dc restoration is needed in the refreshing process. By eliminating the current required to restore the dc levels, the power dissipation by the 512 sense amps is less than required in designs using 256 sense amps with dc-restore schemes. In short, the MCM6664 has all the benefits of 128-cycle refresh without an increase in power consumption.

The net effect of all these techniques is that the maximum active power of the part is roughly half that of 16-K chips. Power dissipation heightens junction temperatures, and this accelerates failure rates. Therefore a reduction in power requirements results in improved reliability for the 64-K RAM.

A refreshing idea

The increase in silicon area required to implement the two additional refresh modes is just 3 mils on the long side. Thus the 145-by-260-mil chip is only 1.5% larger than it would be without refresh control. What's more, the current consumption of the new refresh circuitry is only 0.8 milliamperes, representing a power increase of less than 5 milliwatts.

Automatic refresh is used during standard operation just like $\overline{RAS}$-only refresh, except that sequential row addresses from an external counter are no longer necessary. In fact, the MCM6664's refresh control circuitry also supplants the need for row- or column-address strobes, address counters, or any critically timed pulse during automatic operation.

The automatic refresh cycle is initiated by bringing refresh low after $\overline{RAS}$ has precharged (Fig. 2). The time between the two edges is $t_{d(RAS)}$. Shortly after the refresh cycle begins, an internal row-address strobe fires an on-chip row-address counter that presents the next set of 128 row addresses to the memory matrix. For maximum reliability, this counter is refreshed during every memory cycle. The refresh signal can be inactivated (pulled high) after a time period $t_{w(REF)}$.

Self-refresh is primarily intended for trouble-free power-down operation. For example, when battery backup is used to maintain data integrity in the memory, pin 1 may be used to place the device in the self-refresh mode with no external timing signals necessary to keep the information alive.

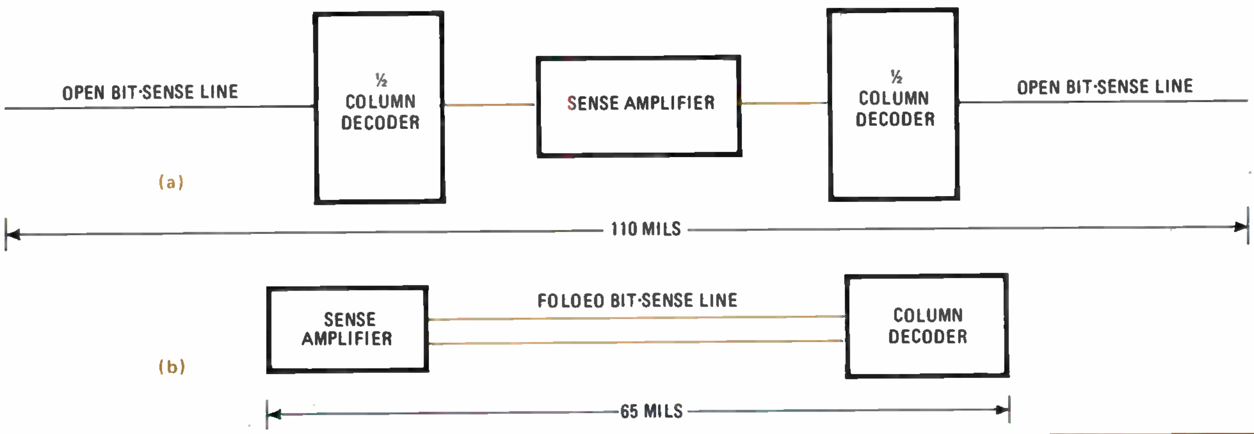
Timing for self-refresh is quite similar to that for automatic refresh (Fig. 2b). The $\overline{RAS}$ line is brought

Folded bit-sense lines reduce alpha errors

The MCM6664 uses a folded bit-sense line to subdue a problem common with open bit-line approaches: noise. With an open bit-line scheme (part a of the figure), noise injected on either of the open nodes is not balanced, which may lead to an error in charge detection. Folded bit lines are only 9 micrometers apart (part b), so that the common-mode noise cancels itself. The configuration also eliminates conductor patterns atop the column decoders, which cuts the capacitance of the bit-sense lines.

The folded bit-sense lines also play a key role in minimizing errors induced by alpha radiation [*Electronics*, June 8, 1978, p. 42]. Maintaining relatively high levels of stored charge in memory cells and improving the sensitivity of the sense amplifiers is one way that the MCM6664 reduces the effect of alpha radiation. However, storage-well filling is only one alpha radiation phenomenon. A diffused bit-sense line can sustain an alpha hit with the same result as when a storage well is hit. In fact, an n^+ (highly doped) bit line appears to be even a better collector of alpha-generated charge carriers than are storage cells.

Since the area of the bit-sense line is greater than the area of a storage cell, a good design must consider methods to reduce these effects. The MCM6664 substantially reduces its susceptibility to alpha radiation by using a metal overlay sense line, which dramatically reduces the exposed n^+ area of the bit line. An alpha hit on a metal line will not cause the collection of charge from electron-hole pairs as it will in a diffused bit-sense line.



high (or left high), and after the regular precharge time, t_d(RAS), the refresh control line can be brought low. Once again, this starts an internal refresh interval, and the MCM6664 provides its own row-address, strobe and refresh-location count.

As long as $\overline{\text{RAS}}$ remains high and refresh remains low, the RAM will refresh itself. This internal sequence repeats asynchronously every 12 to 16 µs. After 2 ms, the on-chip refresh-location counter has advanced through all the row addresses and refreshed the entire memory. This can continue until a regular memory cycle is desired. Since it is possible that a self-refresh cycle just started, a delay of one cycle time is necessary to guarantee valid data in the next memory cycle.

The MCM6664 offers complete compatibility with systems designed for $\overline{\text{RAS}}$-only refresh, which became the industry standard with 4-K and 16-K dynamic RAMs. That is, it allows 128-cycle, $\overline{\text{RAS}}$-only refresh exactly as it is performed in the 4116 16-K dynamic RAM. As with the 4116, A_0-A_6 are used during refresh. The new address line, A_7, is not employed for refresh, so no modification to refresh circuitry is necessary to drop the 64-K chip into existing systems. Figure 2c shows the timing for $\overline{\text{RAS}}$-only refresh.

The MCM6664's design allows the $\overline{\text{CAS}}$, data-in, write, and address lines to change without affecting the refresh cycle. Thus one portion of the system memory may be refreshed while typical read/write operations are occurring elsewhere. Moreover, internal lock-out circuits guarantee fail-safe operation. The refresh control and the row- and column-address strobes (CAS) work together to provide the internal refreshing and a three-state output control (Fig. 3).

After a refresh request, the RAM responds immediately, thus avoiding the problem of having to look ahead an additional cycle, common with other schemes. Moreover, output data remains valid for use by the central processing unit because of the three-state output control. The $\overline{\text{CAS}}$ signal controls the output during refresh or regular memory cycles regardless of other inputs. If $\overline{\text{CAS}}$ is low, the output remains valid. As soon as a floating output is desired (even during the middle of refresh), $\overline{\text{CAS}}$ goes high and the output goes to its high-impedance state.

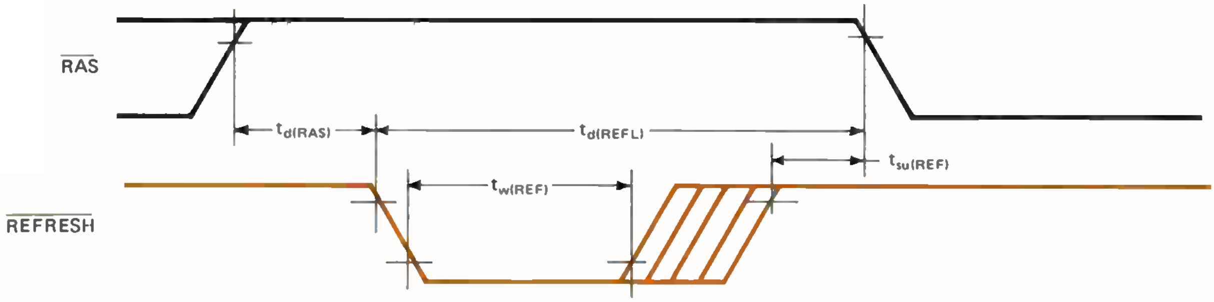
Output control

The three-state control circuitry can place the output in the high-impedance state during an early write cycle. In such a cycle, the write line ($\overline{\text{W}}$) is pulled low before $\overline{\text{CAS}}$ to facilitate common input/output operation.

But the key to the MCM6664's output flexibility is in the independent $\overline{\text{CAS}}$ control. If $\overline{\text{CAS}}$ is high, the output goes to the high-impedance state regardless of other input conditions or what memory cycle the memory is in at the time. For example, if previous output data needs to be cleared to prepare for a read operation or if a write operation needs to be set up in a system with common I/O, $\overline{\text{CAS}}$ is simply brought high and the output floats.

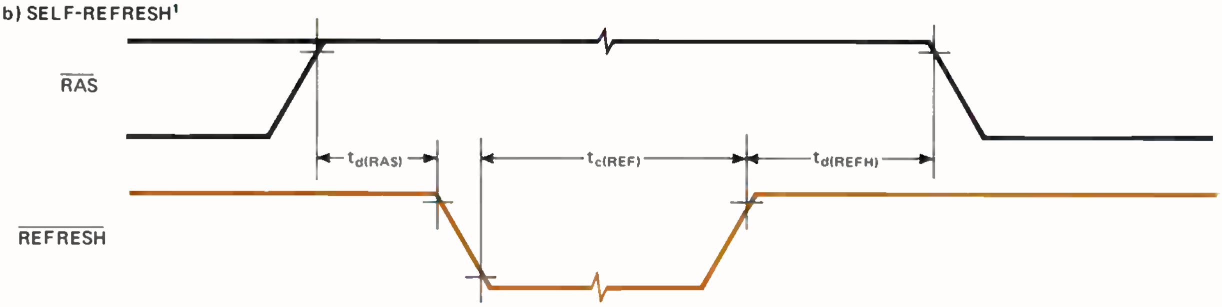
The internal CAS line of Fig. 3 always takes the

(a) AUTOMATIC REFRESH[1]



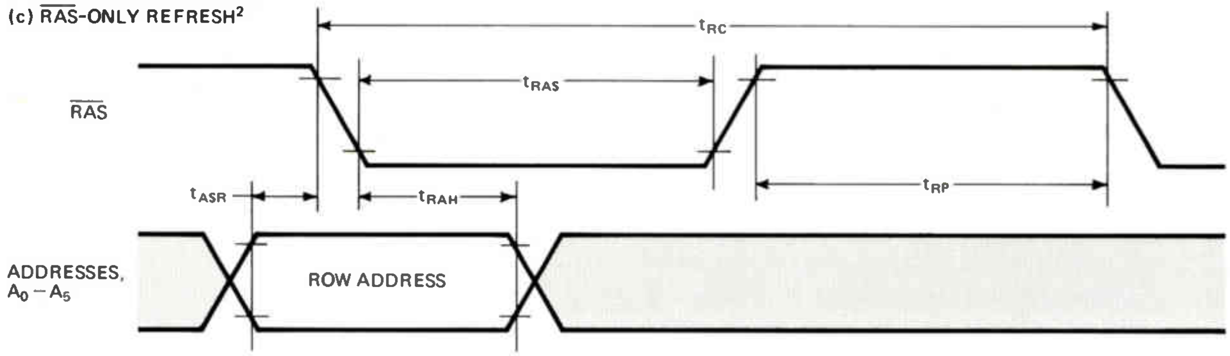
Parameter	Symbol	Minimum	Maximum
Refresh-low delay time before beginning of next cycle	$t_{d(REFL)}$	290 ns	–
Refresh-low duration time	$t_{w(REF)}$	60 ns	8 μs
Refresh-high setup time before next memory cycle	$t_{su(REF)}$	20 ns	–
$\overline{\text{RAS}}$-high-to-refresh-low delay ($\overline{\text{RAS}}$ precharge time)	$t_{d(RAS)}$	60 ns	–

(b) SELF-REFRESH[1]



Parameter	Symbol	Minimum	Maximum
Self-refresh cycle time (entire memory refreshed every 2 ms)	$t_{c(REF)}$	16 μs	–
Refresh-high delay time before a new memory cycle may begin	$t_{d(REFH)}$	250 ns	–
$\overline{\text{RAS}}$-high-to-refresh-low delay ($\overline{\text{RAS}}$ precharge time)	$t_{d(RAS)}$	60 ns	–

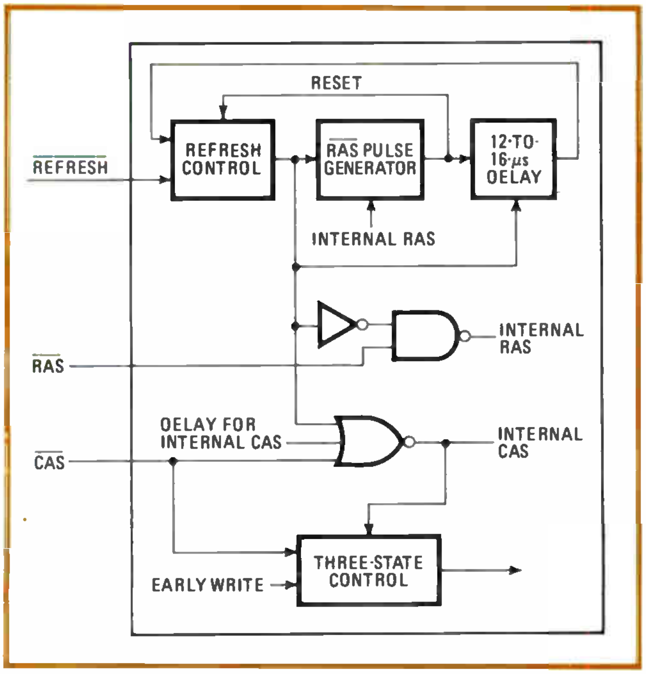
(c) $\overline{\text{RAS}}$-ONLY REFRESH[2]



Parameter	Symbol	Minimum	Maximum
Random read or write cycle time	t_{RC}	250 ns	–
Row-address-strobe pulse width	t_{RAS}	150 ns	–
Row-address-strobe precharge time	t_{RP}	60 ns	–
Row-address setup time	t_{ASR}	0 ns	–
Row-address hold time	t_{RAH}	15 ns	–

1. Addresses, data in, and write ($\overline{\text{W}}$) are "don't care". $\overline{\text{CAS}}$ controls the output data. If it remains low, the previous output will remain valid. If it is brought high, the output will assume a high-impedance state.
2. Data in and write are "don't care", $\overline{\text{CAS}}$ is high.

2. Refresh timing. The MCM6664 has two new refresh modes: automatic (a) and self refresh (b) in addition to $\overline{\text{RAS}}$-only (c). Automatic refresh removes the need for critically timed signals during typical operation. The self-refresh mode makes power-down a snap.



3. Control. The refresh control and the row- and column-address strobes work together for refreshing and output control. If CAS is high, the output goes into the high-impedance state regardless of other input conditions or memory-cycle type.

TABLE 2: OUTPUT BUFFER TRUTH TABLE				
Early write	CAS	Refresh control (internal CAS)		Output buffer
high	–	–	(–)	high impedance
–	high	–	(–)	high impedance
low	low	low	(high)	maintains previous data
low	low	high	(low)	active

opposite state of the refresh control (Table 2). During a refresh cycle, the output maintains the previous data as long as the external CAS line is held low. When that line is brought high, the data is cleared and the output is returned to the high-impedance state.

During a regular memory cycle, the data at the addressed location becomes the output level. This is the case when all inputs to the three-input NOR gate in Fig. 3 are low.

System refresh

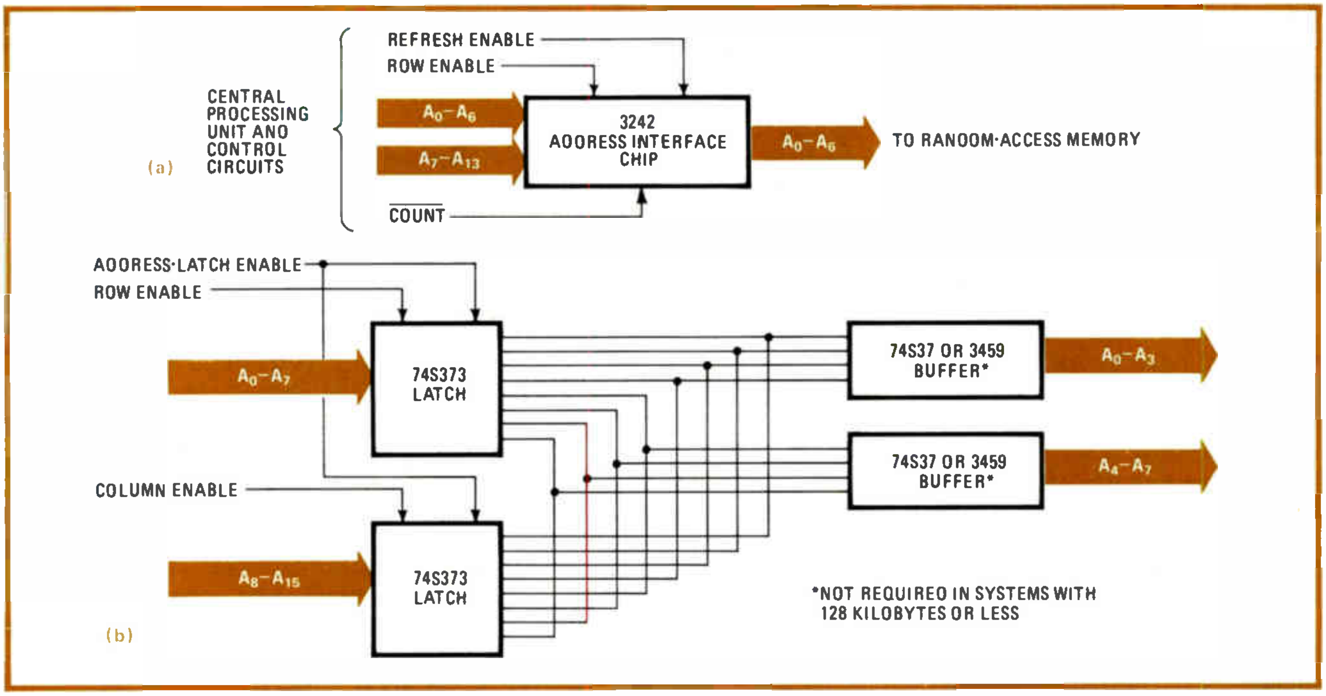
When it comes to putting the MCM6664 into systems, the chip's design eliminates the need for much peripheral circuitry, such as a row-address counter. It also radically simplifies the refresh role of the memory controller.

To meet interface requirements, 16-K dynamic RAMs may use a special address-interface circuit, like the 3242, that contains an address multiplexer and refresh address counter (Fig. 4a). At present, there is no similar interface part for 64-K RAMs.

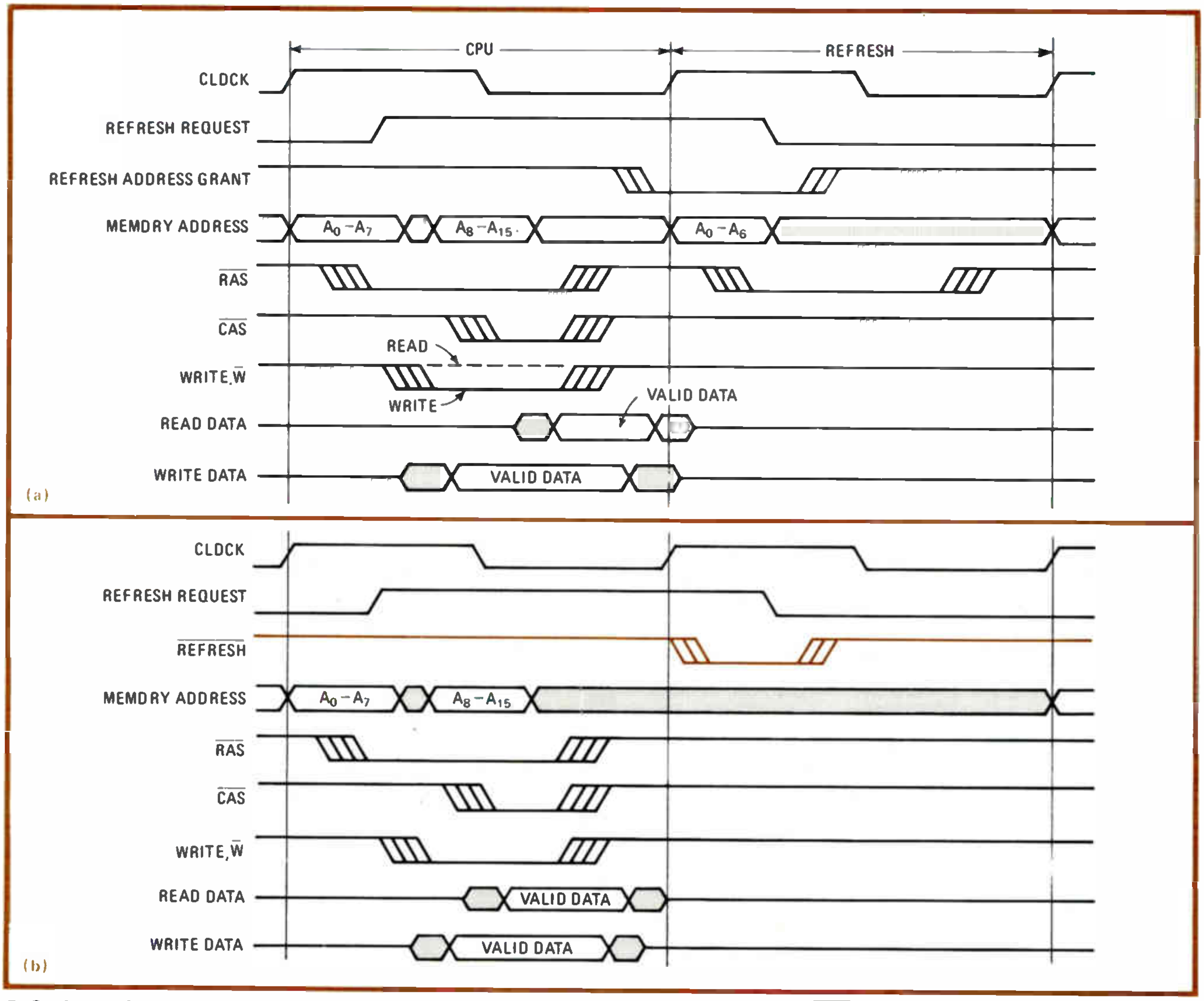
Although these special interface parts simplify memory controller design, they have two fundamental disadvantages. First, they are not universally available (unlike standard transistor-transistor-logic components); second, they are relatively expensive.

Fortunately, the MCM6664 does not require special address interfaces. In fact, for systems with 128 kilobytes or less, all that is required are two standard TTL 8-bit latches (the 74S373s in Fig. 4b).

In systems where the refresh- and CPU-cycle requests are asynchronous, the memory controller requires a settling time. In other words, it needs time to determine which type of cycle to execute when both a refresh and CPU cycle are requested concurrently. If the controller finds that a refresh cycle is to be executed, additional settling time is required with conventionally refreshed



4. Interface. A 16-K RAM can use a special chip, like the 3243, which has a multiplexer and counter (a). Such parts do not yet exist for 64-K parts, but their savings are questionable anyway. For systems with 128 kilobytes or less, the MCM6664 needs only two TTL latches (b).



5. Cycle steal. With conventional RAMs, dispersed refresh gets complicated. After disabling $\overline{\text{CAS}}$, an address grant is generated and the refresh address is set up and strobed (a). However, when the MCM6664's $\overline{\text{REFRESH}}$ line is lowered, no strobes or addresses are needed (b).

RAMs because the refresh address first needs to stabilize. With the MCM6664, however, this skew time can be eliminated since the refresh address is generated on chip.

With conventional dispersed refresh, as it is called, the logic flags the memory controller to indicate that the next cycle to be executed will be a refresh. The refresh-request signal is generated by a counter set to a frequency determined by the system's cycle time and the number of refresh cycles required by the memory devices during a specified time period.

When the refresh-request signal is generated, the memory controller switches to the refresh mode and a refresh cycle begins after the current memory cycle is terminated. First, the memory controller must disable the row-address-strobe decoder so that all memory chips receive a $\overline{\text{RAS}}$ signal. Next it must disable the $\overline{\text{CAS}}$ signal and generate a signal that tells the refresh logic to send its refresh address to the address logic block. Then a refresh-control signal disables the CPU address from the memories and enables the refresh address.

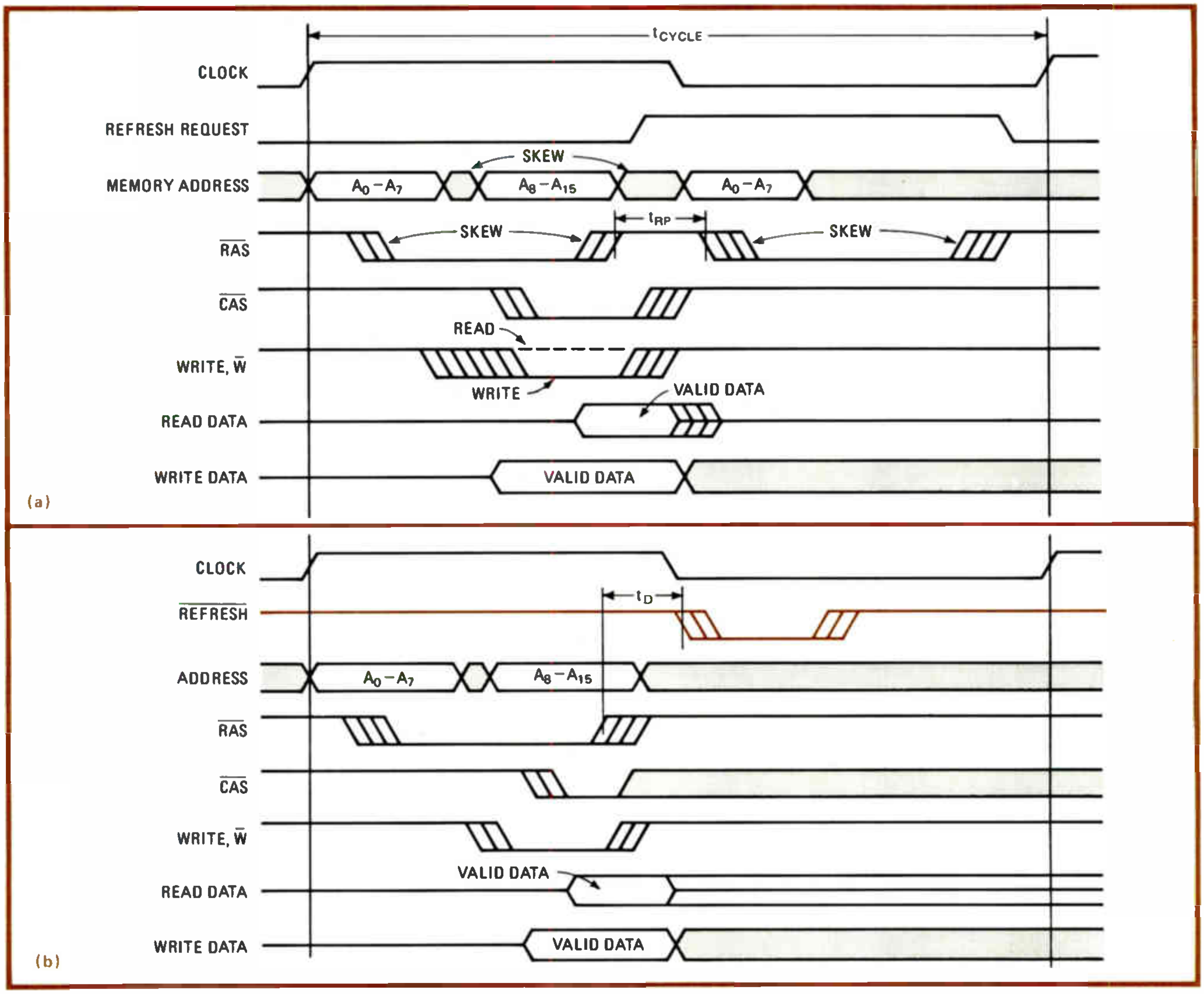
With these conditions set up, the controller executes the refresh cycle with an operation time the same as that for a read or write cycle. At the end of this cycle, the memory controller switches back to a CPU operational mode. Timing for a dispersed-refresh system using RAMs without refresh control is shown in Fig. 5a.

If the refresh address and timing logic are on the memory chip as with the MCM6664, then this sequence becomes much simpler. After the memory controller has determined that a refresh cycle is required, it disables the normal timing sequence, generates a $\overline{\text{REFRESH}}$ signal with noncritical timing and enables the normal timing sequence at the end of the refresh cycle. Figure 5b shows the timing in a MCM6664-based system.

Hidden refresh

There are a variety of data-processing systems that cannot steal an occasional cycle to perform the refresh. For these systems, the refresh must appear transparent: the memory system must look as if it is composed of static RAMs.

One way of performing a transparent or hidden refresh is to integrate the refresh cycle into selected CPU cycles. To minimize the cycle time, the refresh cycle



6. Hidden refresh. For systems that cannot steal it, an occasional refresh cycle can be integrated into selected CPU cycles. With the MCM6664, the refresh control signal, $\overline{\text{REFRESH}}$, can be timed off the trailing edge of $\overline{\text{RAS}}$. Timing skew and cycle time are both reduced.

must begin as soon as data transfer to the CPU can be terminated. However, there are limiting factors.

Before a refresh cycle can be initiated, the row-address-strobe signal must return to a high state for the minimum $\overline{\text{RAS}}$ precharge time, t_{RP} (Fig. 6a). To minimize the amount of control logic, the CPU timing sequence repeats as a refresh-cycle sequence.

However, the digital control path to initialize the refresh cycle is not necessarily the path used by the central processing unit. Consequently, to ensure minimum t_{RP}, additional delay between the CPU cycle and the refresh cycle must be added to overcome the timing variations. The timing skew at the trailing edge of the refresh cycle also tends to increase the cycle time, since a new CPU cycle cannot start before t_{RP}.

With the MCM6664, the timing of the refresh control sequence does not have to be the same as for a CPU cycle. In fact, the control signal, $\overline{\text{REFRESH}}$, can be timed off the trailing edge of $\overline{\text{RAS}}$. Thus, timing skew is minimized and the cycle time is reduced (Fig. 6b).

The MCM6664 also simplifies the design and enhances the performance of those systems requiring battery backup. With the exception of the logic that detects the power-fail mode, the $\overline{\text{REFRESH}}$ signal, and the $\overline{\text{RAS}}$ buffers, all of the hardware can be turned off.

Battery backup

When a power failure is detected, the power-fail logic forces the $\overline{\text{REFRESH}}$ output low. After this, the power to the rest of the controller can be removed, except to the $\overline{\text{RAS}}$-output gates which must remain high. If the $\overline{\text{REFRESH}}$ signal stays at a low level for more than 16 μs, internal logic on the memory chip takes over and automatically generates all of the required refresh cycles. The memory chips remain in this mode until the $\overline{\text{REFRESH}}$ line goes high, ending the self-refresh mode.

With the MCM6664's battery-backup refresh, overall power consumption will be far less than with conventional dynamic RAMs, because less control logic must remain powered up. Since the memory chips do not require any signals during the battery mode, no high-current buffers have to remain active except $\overline{\text{RAS}}$. The absence of the external $\overline{\text{RAS}}$ signal and refresh address eliminates the ac power required to charge and discharge these lines. ☐

Digital multiplexer derives six-variable logic function

by A. Mageswaran
Tata Institute of Fundamental Research, Ootacamund, India

The chip-optimization method introduced by Siebert ("Digital multiplexers reduce chip count in logic design," *Electronics*, April 28, 1977, p. 120) can be extended, so that logic functions containing six variables can be easily implemented. Using a single 1-of-16-line multiplexer and several gates, most functions can be generated with much less effort than stated by Siebert.

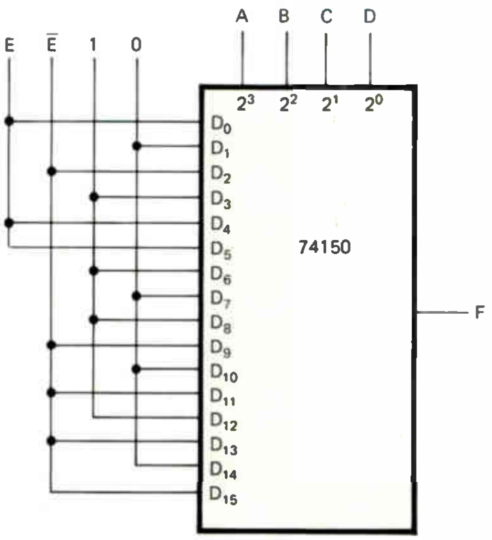
In order to understand how chip count is reduced, consider the implementation of any five-variable function with a 1-of-16-line multiplexer, as was discussed in the aforementioned article. Part (a) of the figure shows a typical truth table and the required setup. Although it is customary to see a logic equation corresponding to the truth table, in reality the advantages of using multiplexers for chip reduction is that explicit writing and minimization of the logic equation are not required.

Here, the multiplexer's data-select inputs are driven by four of the input variables (A–D) and the 16 data lines (D_0–D_{15}) are driven by two functions of the remaining variable, E, and logic 1 and logic 0 signals. The function to which a particular data line is to be connected is easily determined by inspection of the truth table. For example, if variables A–D are all at logic 0, then line D_0 will be selected. Under these conditions, the output F should be 0 when E is 0, and F should be 1 when E is 1. Therefore, line D_0 should be connected to E. Likewise, when inputs A–D address line D_1 (see entries 3 and 4 of the truth table), it is seen that D_1 should be connected to logic 0, and so on.

If this scheme is directly extended to six variables, it will be found that a 1-of-32-line multiplexer or equivalent will be needed. Alternatively, however, a 1-of-16-line device can be used, provided the data lines of the multiplexer are connected to the corresponding functions of both of the remaining variables (E and F) and the logic 0 and logic 1 states. Such a case is shown for the function, again displayed in truth table form, given as an example in (b).

As in the five-variable case, A–D address the data-selected lines. From the first two entries in the truth table, it will be evident after some thought that the exclusive-OR function, E ⊕ F, must be applied to the D_0 line. Similarly, it becomes apparent from the next four entries that data line D_1 must be connected directly to E, and so on. Several gates are required for implementing the E–F functions, but the cost should be below that of the additional multiplexers Siebert's scheme would require to generate the six variables. □

Engineer's notebook is a regular feature in Electronics. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $50 for each item published.

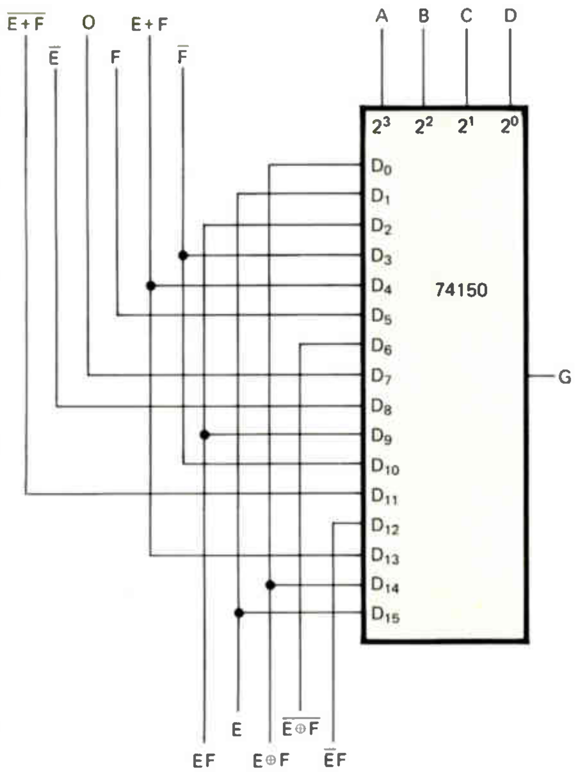


A	B	C	D	E	F
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	0
0	0	0	1	1	0
0	0	1	0	0	1
0	0	1	0	1	0
0	0	1	1	0	1
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	0	1	1
0	1	0	1	0	0
0	1	0	1	1	1
0	1	1	0	0	1
0	1	1	0	1	1
0	1	1	1	0	0
0	1	1	1	1	0

A	B	C	D	E	F
1	0	0	0	0	1
1	0	0	0	1	1
1	0	0	1	0	1
1	0	0	1	1	0
1	0	1	0	0	0
1	0	1	0	1	0
1	0	1	1	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	1
1	1	0	1	0	1
1	1	0	1	1	0
1	1	1	0	0	0
1	1	1	0	1	0
1	1	1	1	0	1
1	1	1	1	1	0

(a)

Variable placement. General method for implementing any five-variable logic function with multiplexer requires inspection of truth table in order to determine where variable E and logic values 0 and 1 should be placed on data lines (a). Six-variable function can also be implemented with a single multiplexer if variables E and F are united (b). In either case variables A–D drive the multiplexer's data-select inputs.



A	B	C	D	E	F	G
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	1
0	0	0	0	1	1	0
0	0	0	1	0	0	0
0	0	0	1	0	1	0
0	0	0	1	1	0	1
0	0	0	1	1	1	1
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0	1	1	0	1	0	0
0	1	1	0	1	1	1
0	1	1	1	0	0	0
0	1	1	1	0	1	0
0	1	1	1	1	0	0
0	1	1	1	1	1	0

A	B	C	D	E	F	G
1	0	0	0	0	0	1
1	0	0	0	0	1	1
1	0	0	0	1	0	0
1	0	0	0	1	1	0
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1	1	1	0	1	0	1
1	1	1	0	1	1	0
1	1	1	1	0	0	0
1	1	1	1	0	1	0
1	1	1	1	1	0	1
1	1	1	1	1	1	1

(b)

Calculator notes

HP-67 finds op amp's gain and common-mode rejection

by Michael R. Hyman
Gamma Scientific Inc., San Diego, Calif.

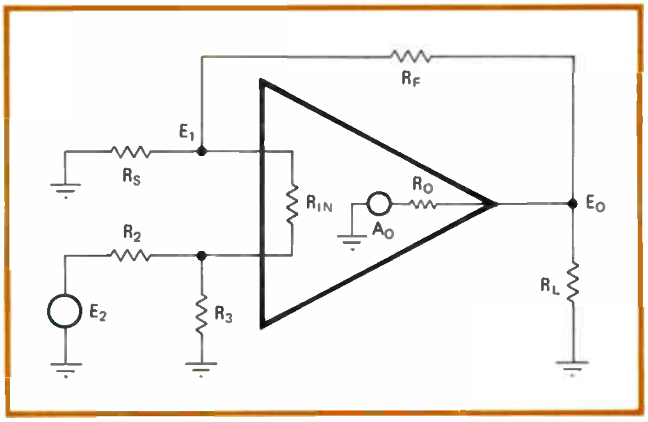
Analyzing circuits built around operational amplifiers is often complex and almost always time-consuming, even when the configuration is relatively simple. This HP-67/97 program can cut the calculation time from hours to seconds for the general circuit shown in the figure. Both the exact inverting and noninverting closed-loop gain are found, as are the true common-mode rejection ratio (CMRR) and the value of the input matching resistance required to optimize that ratio.

The program finds the inverting closed-loop gain from:

$$\frac{E_O}{E_2} = A^- = \frac{R_O[1+(R_2/R_3)+(R_2/R_{IN})]-[R_F A_O][1+(R_2/R_3)]}{D}$$

where D is a complex 27-term function of A_O and all circuit resistances. The noninverting closed-loop gain is found from:

$$A^+ = \frac{(R_O R_S/R_{IN}) + A_O(R_F + R_3)}{D}$$



Time saver. Complex nodal equations for this standard op-amp circuit are solved in seconds by the HP-67/97. Exact inverting and noninverting closed-loop gain, true common-mode rejection ratio, and the value of R_2 required for infinite CMRR are quickly determined.

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where, in general, the difference between A^+ and A^- is small but may be significant in some cases.

Having determined both loop gains, and given the circuit's element values and the op amps' specified CMRR ($CMRR_o$), the calculator finds the true common-mode rejection ratio in decibels:

$$CMRR_{true} = \frac{A^-}{A^- + A^+[(CMRR_o + 1)/CMRR_o]}$$

When A^- and A^+ are expressed in terms of circuit resistances, the optimum value of the input-matching resistor, R_2, required for maximum $CMRR_{true}$ is determined from:

$$R_2 \approx \frac{R_3[(R_F + R_S)/R_S][(CMRR_o + 1)/CMRR_o]}{(-R_F/R_S)/CMRR_{true} + R_F/R_S} - R_3$$

To illustrate an example of the program's usefulness, take as an example the following circuit:

R_{IN} = 10 megohms	$R_S = R_2$ = 1 kΩ
R_O = 2 kilohms	R_3 = 325 kΩ
R_F = 325 kΩ	A_o = 50,000
R_L = 1.5 kΩ	$CMRR_o$ = 1778.28 (65dB)

Keying in the data as instructed reveals that A^+ = 316.08, A^- = −316.08, $CMRR_{true}$ = 1,778.81, CMRR = 65.0 dB, and R_2 = 1 kΩ. R_2 (optimum) is then found to be 1,180 Ω, and the new CMRR is 136.48 dB. □

HP-97 PRINTER LISTING: OP-AMP STAGE ANALYSIS

001	LBLC	037	1	073	1	109	1	145	×	181	×
002	SF2	038	+	074	+	110	+	146	CHS	182	STOD
003	RTN	039	RCL0	075	RCL4	111	RCL2	147	RCL5	183	PSE
004	R/S	040	1/X	076	RCL2	112	RCL4	148	RCL0	184	RCL5
005	LBLA	041	×	077	×	113	+	149	÷	185	RTN
006	STO0	042	RCL4	078	×	114	×	150	RCL5	186	R/S
007	GSB1	043	×	079	RCL0	115	+	151	RCL6	187	LBLE
008	STO1	044	RCL2	080	÷	116	RCL8	152	÷	188	RCL2
009	GSB1	045	RCL3	081	+	117	+	153	+	189	RCL4
010	STO2	046	÷	082	RCL1	118	STO8	154	1	190	+
011	GSB1	047	+	083	RCL3	119	F2?	155	+	191	RCL4
012	STO3	048	RCL2	084	÷	120	GTO2	156	RCL1	192	÷
013	GSB1	049	RCL0	085	×	121	RCL2	157	×	193	RCL6
014	STO4	050	÷	086	RCL8	122	RCL4	158	+	194	×
015	GSB1	051	+	087	+	123	+	159	RCL8	195	RCLE
016	STO5	052	1	088	STO8	124	RCL7	160	÷	196	1
017	GSB1	053	+	089	RCL5	125	×	161	STOB	197	+
018	STO6	054	RCL1	090	RCL6	126	RCL1	162	RTN	198	RCLE
019	GSB1	055	×	091	÷	127	RCL4	163	LBLD	199	÷
020	STO7	056	STO8	092	1	128	×	164	RCLE	200	×
021	GSB1	057	RCL2	093	+	129	RCL0	165	1	201	RCL2
022	STOE	058	RCL4	094	RCL2	130	÷	166	+	202	RCL4
023	GTOB	059	+	095	RCL0	131	+	167	RCLE	203	÷
024	LBL1	060	RCL5	096	÷	132	RCL8	168	÷	204	÷
025	RCLA	061	RCL6	097	RCL7	133	÷	169	RCLA	205	RCL6
026	STOI	062	÷	098	+	134	STOA	170	×	206	−
027	ISZI	063	RCL5	099	×	135	RTN	171	RCLB	207	STO5
028	RCLi	064	RCL0	100	RCL4	136	LBL2	172	+	208	PSE
029	X⇄I	065	÷	101	×	137	RCL5	173	1/X	209	RCL5
030	STOA	066	+	102	RCL5	138	RCL6	174	RCLB	210	GSBB
031	R/S	067	1	103	RCL6	139	÷	175	×	211	GSBC
032	RTN	068	+	104	÷	140	1	176	ABS	212	GSBB
033	LBLB	069	×	105	RCL5	141	+	177	PSE	213	GSBD
034	RCL5	070	RCL5	106	RCL0	142	RCL7	178	LOG	214	R/S
035	RCL6	071	RCL6	107	÷	143	×	179	2		
036	÷	072	÷	108	+	144	RCL2	180	0		

Instructions

- Key in program
- Enter circuit parameters

  (R_{IN}), A, (R_O), R/S, (R_F), R/S, (R_L), R/S, (R_S), R/S, (R_2), R/S, (R_3), R/S, (A_O), R/S, (CMRR), R/S

  Specify R_{IN} in megohms, all other resistances in kilohms. The noninverting closed-loop gain is displayed.
- Press C to set an internal flag, preparing the calculator for finding the inverting closed-loop gain

  When B is pressed, the gain will be computed and displayed.
- Press D to find the common-mode rejection ratio (CMRR)

  The CMRR value in dB will also be displayed, followed by the value of R_2.
- Press E to find the optimum value of R_2 required to effect a corresponding change in the CMRR

  The new value of R_2 will be momentarily displayed, followed by the new value of CMRR both as a ratio and in decibels. R_2 will then be displayed again.
- To find the change in the noninverting closed-loop gain caused by the change in R_2, press RCL A. Follow this step by pressing RCL B to find the inverting closed-loop gain.

Engineer's newsletter

Resistor trimming optimizes generator's sine wave

Intersil's 8038 function generator produces a sine wave by shaping a triangle wave with a ladder network, two rungs of which are accessible. The potentials imposed on these pins (1 and 12) by external sources determine both waveform symmetry and distortion. But independent adjustment of those potentials to optimize the waveform, as proposed in the application notes, may be **very difficult in practice because both parameters are functions of both potentials,** says Pete Pomeroy of United Electronics Corp., South Africa. Instead of using potentials, Pomeroy proposes placing one potentiometer that varies from 60 to 100 kΩ between pin 12 and ground of the device to control symmetry and another that varies from 10 to 20 kΩ between pins 1 and 12 and ground to control distortion. Because of the low resistance values used in the ladder, the pots have little effect on the voltage distribution within, so that adjustments can be made more easily. Once the sine wave's symmetry is optimized with the first pot, it is a simple matter to reduce distortion by a factor of two or three with the second pot. No retrimming is necessary.

EIA announces standards for resistors, other passive components

The Electronics Industries Association has issued RS-452 and RS-186-E, two documents that recommend the standardization of the physical and electrical properties of high-voltage, high-resistance fixed film resistors and set methods for testing passive components. RS-452 describes axial and radial resistors having values of up to 499 megohms, working voltages to 20 kV, and power ratings to 5 W. RS-186-E is a revised version of an earlier report that discusses the testing of components under varying degrees of severity. The base document includes an index of 13 test methods, which are available individually, **for checking the effects of humidity, corrosion from salt spray, vibration, thermal shock, and heat on component life.** RS-452 costs $7.80. RS-186-E is $3.00, as are each of the 13 test method descriptions. All may be ordered from EIA, 2001 Eye St., N. W., Washington, D. C. 20006.

Voltage-controlled video amp makes wide-ranging AGC

Video amplifiers having differential inputs lend themselves to applications where their peak output can be easily set by a control voltage—a property that makes them excellent as automatic gain controls, observes Yishay Netzer of Haifa, Israel. In contrast with amplifiers whose output is controlled by varying their transconductance (current control), the differential devices **have wider bandwidth and are much simpler to implement in AGC stages.**

Netzer uses the Fairchild μA733, plus a field-effect transistor as a voltage-controlled resistor. Either an n- or a p-channel FET may be chosen, depending on whether the control voltage, V_c, is negative or positive. The FET's source and its drain (operating without supply voltage) are connected between the emitters of the differential-input transistors of the μA733, pins 9 and 4 respectively. The control voltage is applied to the gate of the FET through a 20-kΩ resistor. To linearize the response further for large signal swings, a 20-kΩ resistor in series with a 0.1-μF capacitor can be placed between the gate of the FET and pin 4 of the μA733. The gain of the amplifier is inversely proportional to the FET's resistance and is given by $A = A_o(1 - V_c/V_p) + A_p$, where A_o is the FET's nominal gain, V_p is its pinch-off voltage, and A_p is the gain at pinch-off and beyond.

Vincent Biancomano

Why is the DigiTec Datalogger 3000 already the most popular logger in the world?

most powerful & easiest to use

The Datalogger 3000 puts more power in your hands than any other datalogger.

MORE DATA ACQUISITION. The 3000 handles the widest variety of inputs: ac and dc voltages, ac and dc currents, resistances, *all* thermocouples, RTD's, thermistors, digital and contact closures – *all standard.*

MORE COMPUTATION. The 3000 opens up the power of mathematical computation. It can determine an Average, Difference, Deviation from a Mean; extract Square Roots and more. You can easily convert to engineering units with 30 programmable offset and scale factors. That's 900 different mx + b equations. Two unique tables feature the exclusive "U-PLOT" function (User Programmable Linearization Tables). This powerful feature provides linearization for any transducer or transmitter.

MORE DECISIONS. The 3000 offers 100 programmable set-points for alarm detection. You can assign up to 4 different limits, with priority levels, to each channel for "High," "Low," or "Equal to" decisions. You can Alarm on rate of change or alarm transition. Ten standard Alarm Relays provide outputs for annunciation and control. And, only DigiTec Dataloggers visually spell out alarm messages on a built-in CRT.

Behind all these standard features is 32K of memory. That's enough power to support a system of up to 1000 points.

The Datalogger 3000 ... more powerful than any other datalogger.

The Datalogger 3000 is as easy to use as it is powerful. All communication is in everyday English. We spent man-years developing programming innovations so you can program your system in minutes.

PROGRAM PROMPTING. A built-in CRT display provides prompting to guide you through each step of your program. The Datalogger asks you simple questions in plain English and supplies multiple-choice answers. This interactive prompting assures quick and accurate program entry. Programming is further simplified by utilization of conventional data acquisition terms, no need for complex, computer languages.

CASSETTE LIBRARY. Once your program requirements have been defined, they can be saved on the built-in cassette. This lets you create a library of application tapes. Simply drop in a cassette and the Datalogger will completely program itself. Changing programs, therefore, is as easy as changing cassettes. The same cassette deck can be used to record measured data for future reference.

COMPLETE COMMUNICATION. The built-in CRT provides more information than possible with conventional datalogger displays. You can see 10 channels of system information at a single glance. For hard copy, a standard built-in alphanumeric printer quietly records data. To communicate with peripheral devices, the 3000 offers the widest variety of interfaces. ASCII outputs, both serial and parallel, relay outputs, external condition input, and composite video output are all standard.

The Datalogger 3000 ... easier to use than any other datalogger.

For a free brochure or "hands-on" demonstration, just call Daryl Barnaby collect. (513) 254-6251

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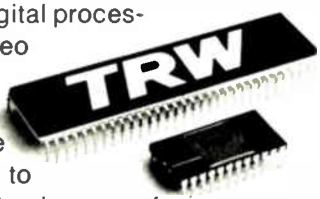
Digital signal processing is here.

TRW takes another step in digital signal processing

PRESENTING OUR 33-NSEC, ONE-CHIP ANALOG/DIGITAL CONVERTERS

We've developed a family of single chip, 30MHz A/D converters with VLSI technology. They're TTL devices that bring all the advantages of digital signal processing to high-speed, wide-bandwidth signals like those used in radar, broadcast video and closed-circuit TV systems. We've designated the 8-bit converter TDC-1007J and the 6-bit device, TDC-1014J.

With digital processing of video signals, you can use simple algorithms to control video images of all kinds. You can freeze, store, and replay the action; compress and expand time; fade in, fade out, wipe, and superimpose—all under non-critical digital control.



Our inexpensive A/D converters make the connection to all this flexibility.

Because we invented TTL and refined it to the level of VLSI, our converters enjoy the luxury of operating as *flash converters*, rather than depending on tedious, successive-approximation techniques.

Our TDC-1007J features full eight-bit resolution. It is a single chip with 255 comparators and a resistive voltage divider. Activating a single device pin strobes the comparators, encodes all their binary outputs into an eight-bit word, and stores the word in an output latch. All this can happen 30 million times a second—now *that's* video-speed data conversion!

The TDC-1007J provides four output data formats and does not require a sample-and-hold circuit at the front end; it is unsurpassed for both NTSC and PAL color video systems.

Our six-bit converter chip, the TDC-1014J, is no falloff from the larger device—it is made with its own 63-comparator mask set and features all the speed, linearity, and utility of its big brother. Use it for applications that call for reduced resolution and cost—like ultrasound, X-ray, radar, and CCTV.

Both the eight-bit A/D and the six-bit A/D are packaged in industry standard DIPs. The larger -1007J has 64 pins; the smaller -1014J has 24. They are both powered by +5V and -6V supplies; the -1007J uses 2W and the -1014J needs only 750mW. Both are radiation hard.

The TDC-1007J (in 100s) is priced at $485. The TDC-1014J (in 100s) is priced at $186. (And these are only our introductory prices—they will go lower like all monolithic devices.)

Like all TRW LSI products, the TDC-1007J and -1014J are available from stock at Hamilton/Avnet. For more information, send in the coupon or talk to one of our digital signal processing experts at 213/535-1831.

TRW LSI Products
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P.O. Box 1125
Redondo Beach, CA 90278

Please send data sheets on the new **TDC-1007J**, 8-bit and **TDC-1014J**, 6-bit A/D converters.

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E-2

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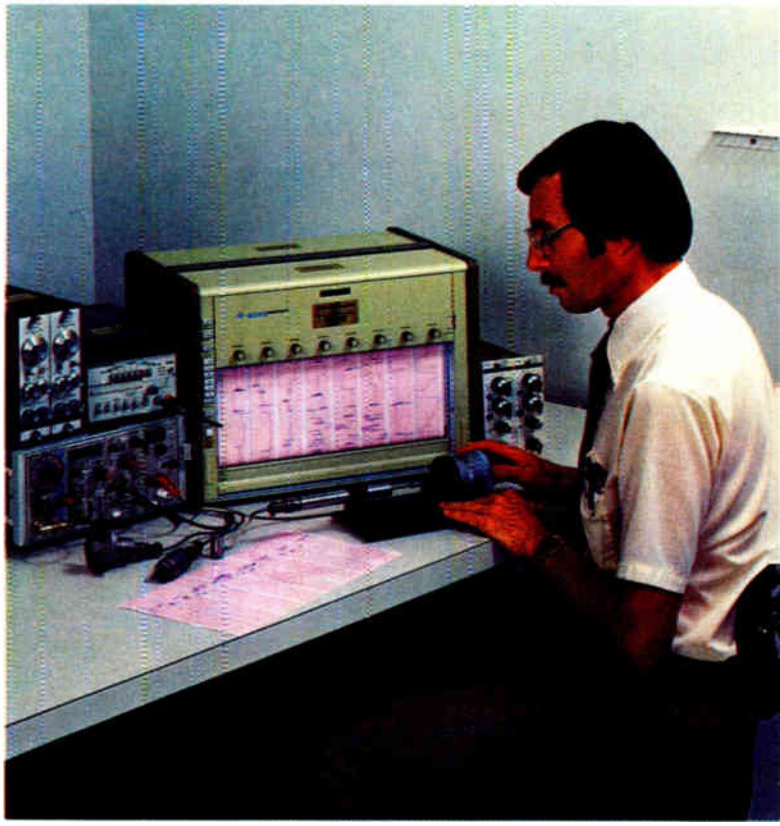

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GENERAL ELECTRIC

LED modules beat space crunch

By rearranging the C-MOS chip that drives light-emitting diodes Litronix realizes space savings of 33% and 46% in intelligent display

by Robert Brownstein, San Francisco regional bureau

Small microprocessor-based systems such as hand-held controllers and instruments, as well as data terminals, generally have been unable to keep up with the rush to market of their larger cousins, in part because of the lack of effective small displays. The bigger systems can use cathode-ray tubes, but the smaller versions have had to get by with less capable light-emitting-diodes and liquid crystals.

Essentially, the problem has been a space crunch—trying to fit 20 alphanumeric characters, plus their decoders, drivers, buffer memory, and random-logic control circuits, in a 3.5-inch-wide package. With the introduction this month of its DL1414 intelligent display modules, Litronix has come up with an answer. In fact, the first full-production units, like earlier samples, are slated to go into the new Lexicon hand-held language translator [*Electronics*, Dec. 7, 1978, p. 50]. Moreover, David M. Barton, Litronix product marketing manager, claims that the translator could not have met its size and cost targets without the display module.

Direct hookup. These modules hook up directly to a microprocessor's address bus and data bus, making hardware design relatively easy. Behind the module's four-digit LED display is a complementary-metal-oxide-semiconductor large-scale integrated circuit that contains all the functional logic needed to translate 7-bit ASCII data into any of 64 alphanumeric characters.

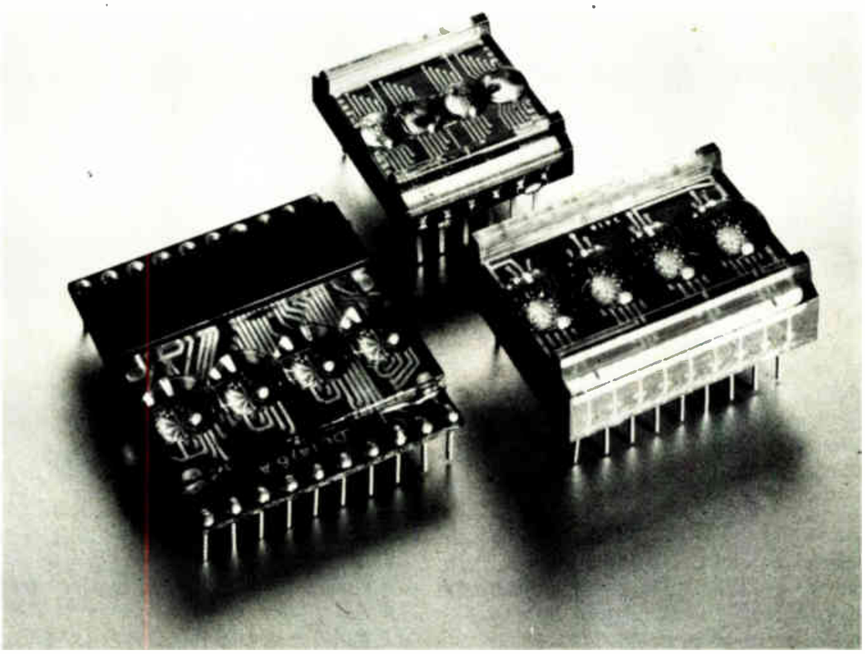
The microprocessor simply treats the module as if it were a random-access memory, writes in an ASCII "word," and moves on to other tasks as the module decodes and displays the characters it has stored, Barton explains.

The DL1414 and a larger module, the DL2416, due out in March, make both electrical and physical design easy, as well, Barton says. Litronix' first intelligent module, the DL1416, has the C-MOS chip side by side with the displays (left in photo), but the new packages move it behind the displays, so their sizes shrink by 33% for the DL2416 (lower right) and 46% for the DL1414 (upper right). What's more, the modules' shape makes it possible to align them horizontally or vertically, thus facilitating the design of displays needing more than a single line of characters.

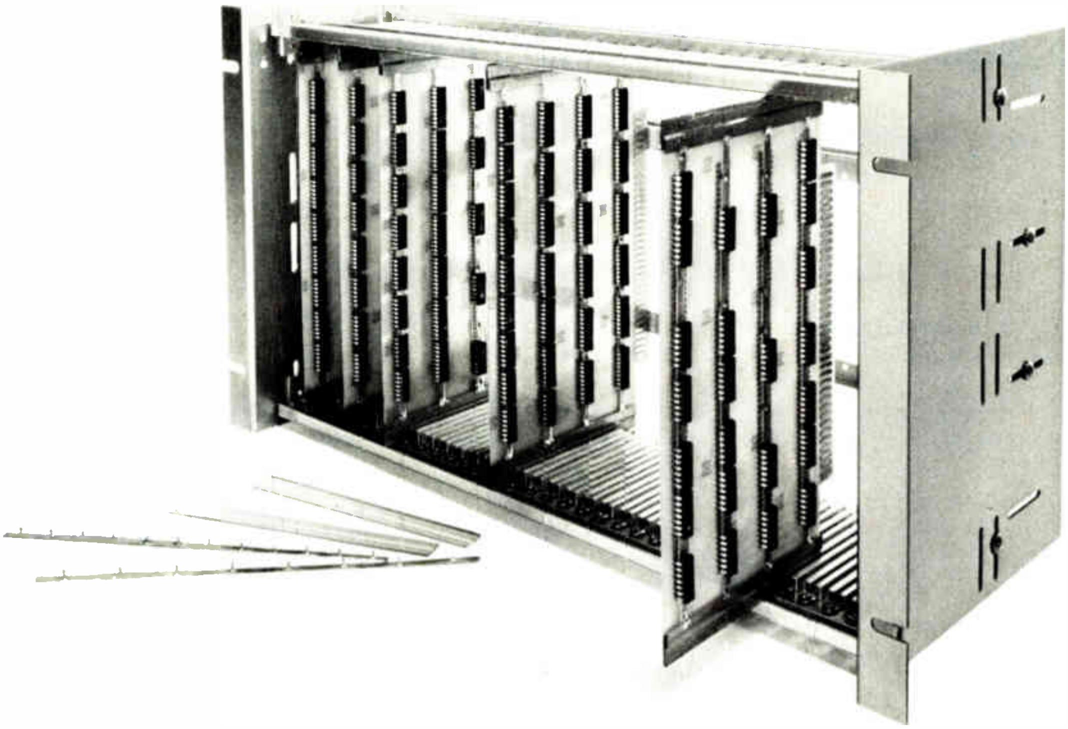
Wide view. A plastic immersion lens, an integral part of the package, magnifies the LED digits, making them appear 160 mils high (the DL2416) or 112 mils high (the DL1414). The maximum viewing angle, a function of actual LED size and lens optics, has been increased from 25° for the older 1416 to 40° for the new 1414 and 50° for the 2416.

The two new intelligent display modules operate from a single 5-V supply, with the larger unit drawing approximately 100 mA and the smaller 50 mA. Price for each in 1,000-piece quantities is $26 and $13 respectively. The higher cost of the DL2416 compared with that of the DL1416 ($18.75 apiece for 1,000) is due to using larger diodes (which have lower production yields) to obtain the greater viewing angle.

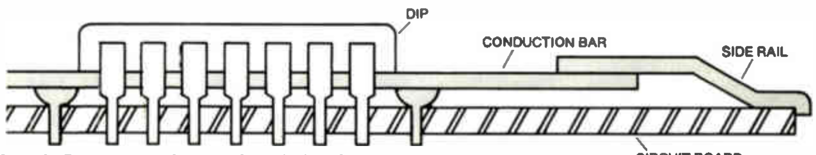
Litronix Inc., 19000 Homestead Rd, Cupertino, Calif. 95014. Phone (408) 257-7910 [338]



Why IERC's new heat dissipation system for .300" DIPs is more efficient, simpler and costs less than alternate technologies.



The IERC system provides significant thermal transfer for better thermal balance as well as an efficient thermal interface from DIPs to card holder.



Standoffs raise conduction bar .020" above circuit board to accommodate metal traces between the standoffs, and to permit removal of solder residue.

The Problem

The thermal management of large numbers of dual-inline packages on a single PC board can be a problem, particularly in telecommunications and logic networks. Single DIPs rarely dissipate as much as one watt, but a board full of them can add up to 15-25 watts. IERC's system of conduction bars and side rails provides a simple, inexpensive, off-the-shelf solution to the problem.

Some Expensive Solutions

Ladder networks will do the job. Of course there is the cost of fabrication, and the difficulty of epoxying the networks to the boards, which makes assembly and repairs a nightmare.

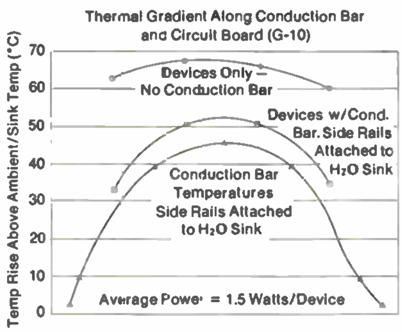
Another approach is to plate heat-dissipation strips directly onto the board. A good idea for some applications, except the cross-sectional dimensions of plated strips (and hence their dissipating efficiency) is limited by the plating process. Also, plated strips require valuable board space and often introduce capacitance and induction problems into your design.

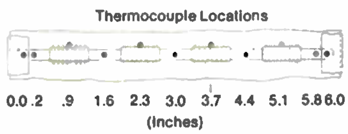
Boards with heat-dissipating metal cores require extremely careful engineering, and are costly and very difficult to make.

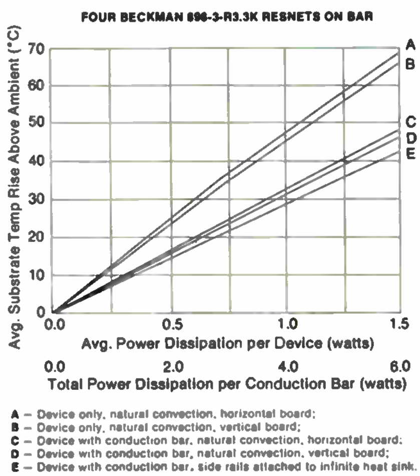
IERC's Better Solution

IERC's heat dissipation system consists of conduction bars and side rails, both of which are made from high-thermal-conductivity copper (solder plated) and are available in practically any length. The conduction bars can be wave-soldered into place along with other board components. The IERC system permits quick fabrication of a custom heat-dissipating network for .300" DIP systems, with no restrictions on the distance between DIPs or rows of DIPs. Call or write today for more information.

IERC's conduction bar system lowers substrate temperatures 30% — 40%.







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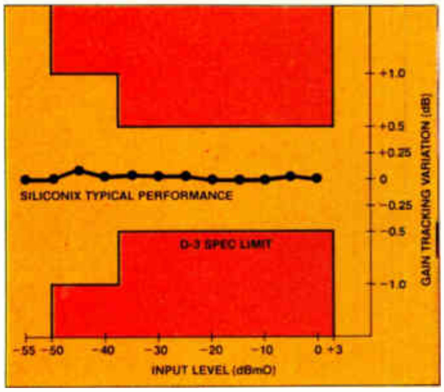
Circle 158 on reader service card

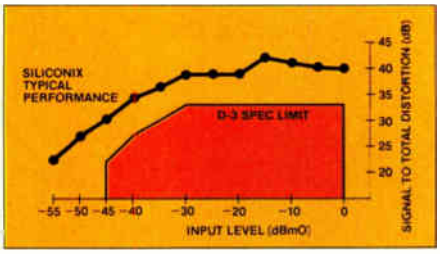
A lot of people are talking CODEC.

We're delivering now. At Siliconix, CODEC is more than just talk. Our DF331/DF332 per channel system is now in volume production to support volume requirements. Prices are low and going even lower as more and more systems commit to Siliconix' format. Since ours is the only CODEC with a licensed second source, we've got everything it takes to be the first industry standard. And you're assured of designing PCM or PABX systems with parts that are here today and a supply that will be going strong when you move into production.



Gain Tracking DF331/DF332 Pair

Volume availability, alternate sourcing and good economics — they're all excellent reasons to call Siliconix first. Perhaps the best reasons, though, are the unique features and performance of our CODEC.



Signal to Total Distortion DF331/DF332 Pair

Low Power. Siliconix' two-chip CODEC gives designers low active power and even lower standby dissipation. Typical active requirement for the chip pair is only 80 mW. In standby, power is reduced to 11 mW.

Superb specs. Backed by Siliconix' 17 year experience in high performance analog circuitry and CMOS technology, our CODEC coder/decoder pair is designed to perform to ATT D-3 channel bank system specs and CCITT specs shown.

Asynchronous operation. Since encoder and decoder are separate parts in Siliconix CODEC, you don't have to depend on local clocks for timing. Independent timing means simpler circuit requirements and more efficient signal processing.

Flexible designing. Siliconix' CODEC gives designers three additional advantages that can make the switch to digital even easier. In D-3 channel banks, our *A/B signaling* capability eliminates external circuitry and further simplifies timing requirements. An *internal auto zero* feature holds input offset voltage to a minimum. And designers working on conference calling PABX applications will like our decoder's *fast conversion rate.* Since it operates four times faster than the encoder, you can design with multiple time slots to a single decoder.

Get us on the line: (408) 988-8000. Talk to our CODEC marketing manager, Barry Boulton. He's ready to help you get Siliconix CODEC into your design — and into your hands. He'll give you details, data sheets and delivery schedules. Or write Barry at Siliconix, Inc., 2201 Laurelwood Road, Santa Clara, CA 95054.

Siliconix

Siliconix puts it on the line.

Circle 159 on reader service card

PMI'S PCM Shared CODEC

It'll leave you grinning like a Cheshire Cat

© PMI 1979

"Would you tell me please, which way I ought to go from here?" Alice asked the Cheshire Cat.

"That depends a good deal on where you want to get to," said the Cat.

"I don't care where, so long as I get *somewhere*," said Alice.

"Then it doesn't matter which way you go," said the Cat.

With that passage from *Alice in Wonderland*, written more than 100 years ago, Lewis Carroll brilliantly summed up the attitude of many people today.

Telephone switching equipment designers right now all want to convert their products to PCM, and they don't care which way they have to go as long as they know they'll get there, and at the lowest cost per line. They know that to get there requires coder/decoder (CODEC) but the device manufacturers have hit them with so many claims and false promises that, like Alice, they aren't sure which way to turn.

PMI's PCM Carrier, CO and PABX customers don't have to ask which way to go because they're already there. They got there with multichannel shared CODECs designed with PMI COMDAC® companding digital-to-analog converters, which PMI has been delivering to them *off the shelf* since 1975. In fact, our COMDAC® μ-Law and A-Law converters (the DAC-86, and DAC-87), are actually in service carrying telephone traffic today. Some have been in operation for over two years in carrier systems, PABX's and remote terminals, with performance that meets or exceeds telephone system specifications.

Of course, some people argue in favor of a single-channel CODEC approach, especially those *Digital* Dreamland houses which can't offer you the *linear* components you need for shared CODEC. Certainly you can get where you want to go with single channel CODECs. Eventually! And if you can afford the price, board space, and believe in price *projections* and *eventual* second sources.

To understand why you'll get there faster and cheaper by going our way, just think in terms of *IC packages* per line rather than CODECs per line.

You see, to provide one *single-line* CODEC per line for 24-line channel bank, takes a minimum of 24 CODECs. In fact, some of the announced single line CODECs are two-package sets. So a 24-line system takes 48 of these "Tweedle Dee-Tweedle Dum" sets.

"But all single-line, single chip CODECs are in huge 24 pin packages!" exclaimed Alice. "That's 576 total pins!"

"Right," said the Cheshire Cat, "and these take up a lot of board space. Even the 2-package CODECs are in 16 or 18 pin packages which aren't small either."

"A PMI 24-line shared CODEC takes about 32 packages—about the same! However most of them are in 8 lead or 14 lead packages. Total pin count is only 424! That's a 26% 'hole saving'!"

The Cheshire Cat told Alice, "You can't take less than nothing." However, when you make PC boards, holes are nothing but they cost something. With the PMI shared CODEC approach, *you* can save lots of board space and hole drilling. That's something!

These are today's PUBLISHED 100 piece prices for off the shelf parts, many with second sources. Of course, you can buy them for much less in larger quantities, TODAY as well as in the future. (50% off for 100K.)

ENCODER FOR 24 LINES	TOTAL COST AT PUBLISHED 100 PIECE PRICES	TOTAL NUMBER OF PINS
3 COMDACs® Converter (DAC-86μ-Law or DAC-87 A-Law)	$ 27.00	54
3 Comparators (CMP-01)	9.00	24
3 SAR's (2502-PC)	9.90	48
3 S/H AMPS (SMP-81)	28.50	42
3 8-Channel Multiplexers (MUX-88)	22.50	48
1 Voltage Reference (REF01 = 10V or REF02 = 5V)	2.95	8
9 Gates (TTL)	3.00	126
DECODER FOR 24 LINES		
1 COMDAC® CONVERTER	9.00	18
1 OP AMP (OP-16)	2.50	8
3 8-Channel Multiplexers (MUX-88)	22.50	48
21 TOTAL LSI/MSI IC PACKAGES	**$136.85**	**424**
PER LINE	**$5.70**	**18**

"Why go to all this trouble just to save a few bucks?," one might ask. The Cheshire Cat knows! Why do you think he's grinning? He knows that CODECs are a major cost item in PCM systems, and less expensive CODECs mean more competitive systems. Is there any telephone equipment manufacturer who doesn't have to worry about competition? (Well, maybe ONE!)

Furthermore, the Cheshire Cat is grinning because he knows that if you don't try to put so many different functions on one chip, the process can be optimized for each function. This not only means lower cost per line due to higher yields, but also lower noise, better performance and better reliability. System signaling and supervision are flexible with the shared CODEC approach, too.

A COMDAC® Converter is not a CODEC

"If you're not a CODEC, what are you, then," said the circuit designer.

"I'm a D/A converter," said the COMDAC® CONVERTER ("CC").

"A likely story indeed. You have no reference, no op amp. You're 'incomplete'."

"Ah, but I'm optimized," said "CC," grinning like the Cheshire Cat. "I conform precisely to the μ-Law or A-Law, whichever you prefer. I do both the conversion and companding and need no special ion implant or thin film processes. So I work inexpensively and reliably."

"I have thin film resistors," interrupted the Voltage Reference.

"Sure, but you're a small chip," chortled the "CC." "Furthermore, we only need one of you for lots of channels, so your cost is negligible."

"What about my ion implant?" asked OP-16.

"You're a small chip, too," replied "CC." "You need the fancy processes to get your speed and input accuracy. But I'm not about to let you on the same chip with me! Otherwise, I'd have to get the ion implant, too, and my friend Circuit Designer doesn't want to pay for it where it's not needed. Besides, I only need you to decode. For encoding, I can do nicely without you, thank you."

"But you need me for encoding and I get ion implant, too," said SMP-81.

"Yes, but for a different reason," said "CC." "You don't have FETs like OP-16. You use ion implant for Super Beta, so you can work in the heat or in the cold, and still do the job. I do need you for encoding, but not for decoding. Sorry, no economic advantage to having you on my chip. Oh, and before *you* ask, Comparator, I don't need you to decode either. So you stay off my chip, too."

"What about me?" asked MUX-88. "I'm new. I have low cross-talk, low on-resistance, super off-isolation, meet all system specs and cost less than any analog MUX on the market!"

"RIGHT!" said "CC." "What's your question?" "I guess I just answered it," said MUX.

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You already know how easy it is to get lost in Linear Wonderland, so let PMI be your guide. If you can tell us where you want to be, we can tell you how to get there. Then we'll *both* be grinning like the Cheshire Cat while everyone else is still trying to find the road.

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- ☐ SMP-81—S/H AMPLIFIER
- ☐ CMP-01—COMPARATOR
- ☐ MUX-88—8-CHANNEL BIFET MULTIPLEXER
- ☐ OP-16—BIFET OP AMP
- ☐ REF01—10 VOLT REFERENCE
- ☐ REF02—5 VOLT REFERENCE
- ☐ I don't need samples, but data sheets will make me grin too.

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2E5020

Packaging & production

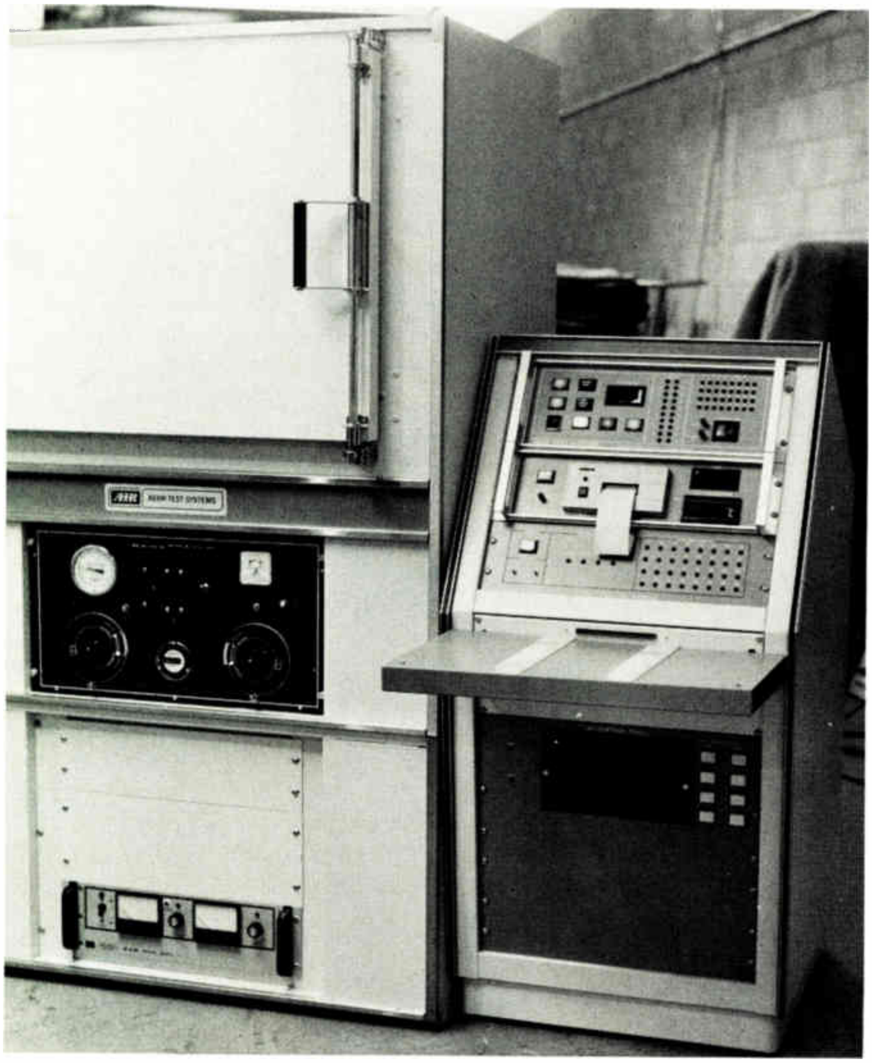
System tests while RAM burns

Unit simultaneously handles 64-K dynamic and 4-K static read/write memories

As 65,536-bit read/write random-access memories begin to appear on the market, users as well as chip makers will want to put the new devices through environmental tests. Unfortunately, such testing usually takes many steps and much time. To help out, Aehr Test Systems is introducing a burn-in system with a difference it makes functional tests on memories while it burns them in.

Called the MBT-100, the system can perform functional tests on 64-K dynamic and 4-K static memories with no need for the user to make any hardware changes, according to Aehr president Rhea Posedel. He believes his system can save time in reliability testing, where the procedure now is to "cook them, take them out, and test them, and then put them back in and cook them." Furthermore, he points out, "then you only pick up the gross errors; you don't pick up the soft errors."

Test parameters, including clock rates and power-supply voltage levels, are stored in an electrically erasable programmable read-only memory. Thus, during a 12-hour burn-in, the memory parts could be subjected, for example, to a data-retention test, a voltage stress test, and a logic pattern to which they are particularly susceptible. Failures are logged on a printer that lists the precise test conditions under which the part failed as well as the nature of the test and the time.



The MBT-100 can test up to 832 chips at a time and has two zones—one for 64-K dynamic memories; the other for 4-K statics. Typical testing speed is 2 MHz (500-ns cycle time), although static memories can be tested with cycle times as low as 300 ns.

An 8080 microprocessor controls system timing and interfacing, but proprietary circuitry of the 7400 series, mostly low-power Schottky, energizes the driver boards, handling clock drives and error monitoring, Posedel says. There is one driver board for each burn-in position. The tester, whose main chamber measures approximately 3 by 4 by 5 feet, sells for about $60,000.

Aehr Test Systems, 440 Hurlingame Ave., Redwood City, Calif. 94063. Phone (415) 366-3831 [391]

Meter tests components between 10 kHz and 10 MHz

Most LCR meters test components at a single frequency—not necessarily the one at which the component will be operating. But the 4275A LCR meter, a microprocessor-controlled instrument, can test a component at any of 10 frequencies between 10 kHz and 10 MHz. Also, the amplitude of the test signal can be varied from 1 mV to 1 V rms.

The meter can completely characterize a device's impedance or admittance. It can measure the inductance and Q of magnetic components such as ferrite cores and filter coils, as well as the capacitance, equivalent series resistance, and dissipation factor of various types of capacitors. It also provides direct readout of resistance, inductance, conductance, reactance, susceptance, and the magnitude and angle of admittance and conductance. Full-scale measurements range from 100 nH to 1 H, 1 pF to 100 μF, and 1Ω to 10 MΩ—all accurate to within 0.1% of reading. The instrument can measure and display two parameters simultaneously with 4½- or 5½-digit resolution.

The 4275A can be integrated into a system with either an isolated or a nonisolated interface-bus option, both of which offer total automation of complex measurements. Two dc bias options, covering the range from 0 to $\pm$100 V dc, eliminate the need for external dc supplies.

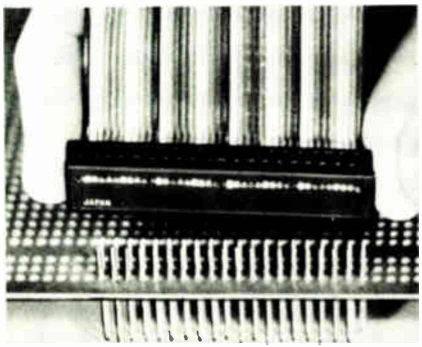
The instrument operates from an input of 100, 120, or 220 V ac $\pm$10% or 240 V ac +5%/−10%, at 48 to 66 Hz. Selling for $8,720, the unit measures 177 by 425.5 by 574 mm and weighs 18 kg. Delivery time is 60 days.

Hewlett-Packard Co., 1507 Page Mill Rd., Palo Alto, Calif. 94304 [394]

Wrapped-wire posts do double duty

T46-5-9 posts can function individually as terminals for wrapped-wire interconnections or side by side to mate to a ribbon-wire connector. Each 0.025-in.-square post extends 0.24 in. above the board and 0.64 in. below. These lengths allow the post to be wrapped with two and three wires, respectively. The posts are also offered with top lengths of 0.32 or 0.42 in. and bottom lengths of 0.36 or 0.42 in. A stop bar ensures consistent insertion depth.

The tin-plated T46-5-9 sells for $3.58 for a package of 100, and $28.93 for 1,000. The gold-plated



T46-5A-9 sells for $5.97 for 100 and $51.93 for 1,000.

Vector Electronic Co., 12460 Gladstone Ave., Sylmar, Calif. 91342. Phone (213) 365-9661 [395]

Rotary table speeds substrate exposure

The 8422 rotary table has dual alignment fixtures that let it expose one substrate while the operator is still unloading a previously exposed one. The system can be used for contact or proximity printing and will accept masks and substrates of various sizes. Masks may range from 2 by 2 in. to 5.5 by 5.5 in., substrates from 1 by 1 in. to 6 by 6 in. in size. The table can be positioned precisely in the X, Y, and Z directions.

Depending on the table style, the price ranges from $2,000 to $10,000. Delivery time is 10 to 12 weeks.

Oriel Corp., 15 Market St., Stamford, Conn. 06902. Phone (203) 357-1600 [396]

Etcher combines dry-plasma and reactive-ion techniques

The DEA-503 reactive-ion etching or dry etching system is designed to meet the fine-resolution requirements of extremely high-density integrated circuits. The unit produces patterns to within 0.2 μm and etches aluminum at 2,000 Å per minute with selectivity to silicon dioxide of 30:1. The use of planar electrodes keeps etching uniform, with a deviation of only $\pm$5% from lot to lot. Having an idle time of less than 15 seconds, the system processes 30 2-in., 14 3-in., or 7 4-in. wafers per cycle. According to the manufacturer, etching can be done with extremely low power, resulting in minimal semiconductor damage. An end-point detection monitor, which measures luminous spectra in the plasma, is optional. The system sells for from $70,000 to $100,000. Delivery time is four months.

Roberts' Associates, 536 Weddle Dr., Sunnyvale, Calif. 94086 [397]

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	MN1404	16 Pin DIP/Plastic	512 x 8 bits	16 x 4 bits
	MN1405	40 Pin DIP/Plastic	2048 x 8 bits	128 x 4 bits
	MN1498	40 Pin DIP/Plastic	External	64 x 4 bits
P-MOS	MN1430	40 Pin DIP/Plastic	1024 x 8 bits	64 x 4 bits
	MN1432	28 Pin DIP/Plastic	768 x 8 bits	2048 x 8 bits
	MN1435	40 Pin DIP/Plastic	32 x 4 bits	16 x 4 bits
C-MOS	MN1450	40 Pin DIP/Plastic	1024 x 8 bits	64 x 4 bits
	MN1453	18 Pin DIP/Plastic	512 x 8 bits	16 x 4 bits
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	MN1455	40 Pin DIP/Plastic	2048 x 8 bits	128 x 4 bits

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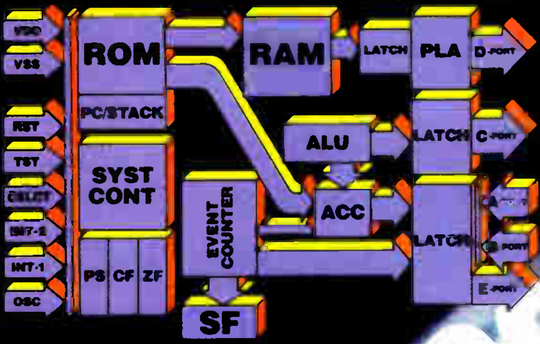

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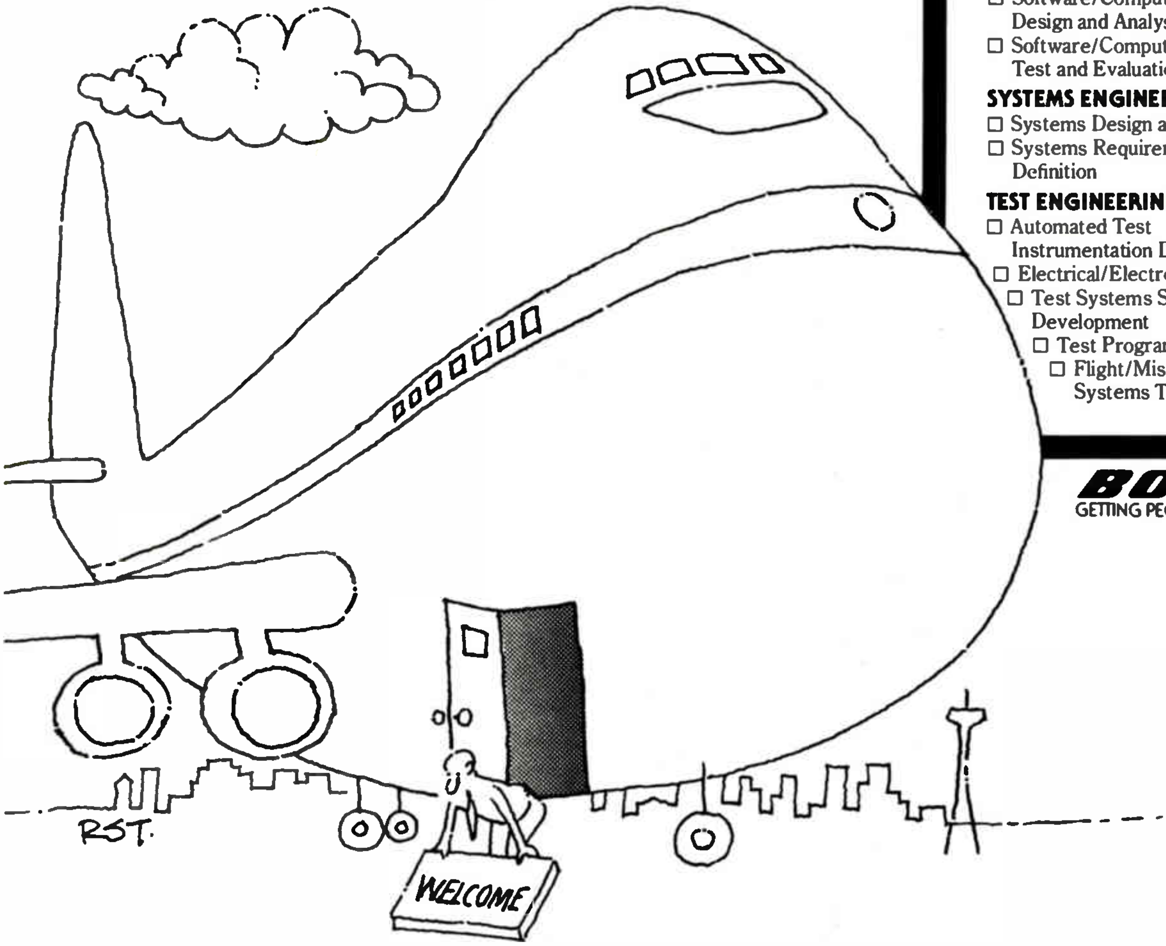

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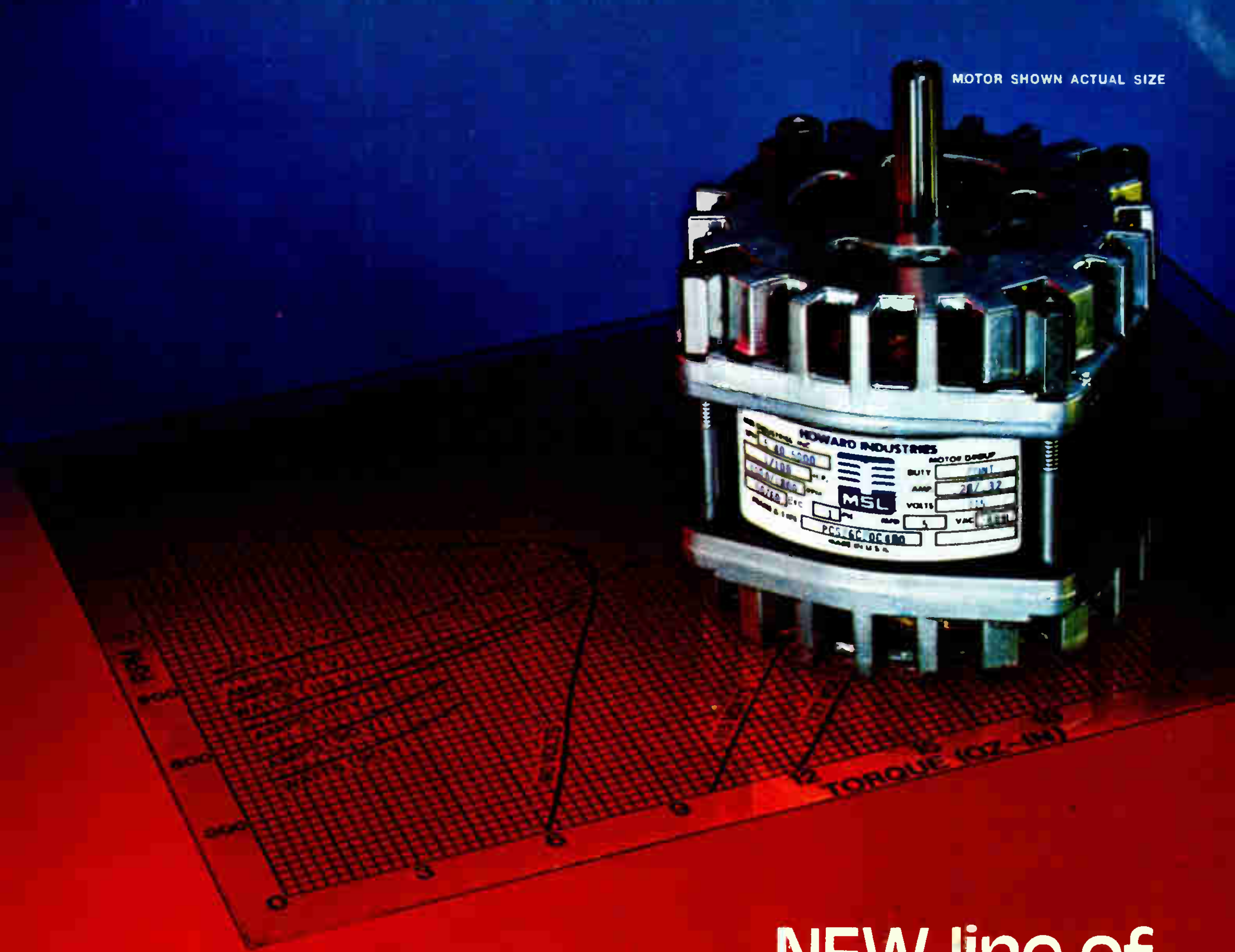

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Microcomputers & systems

Adac offers two Q-bus boards

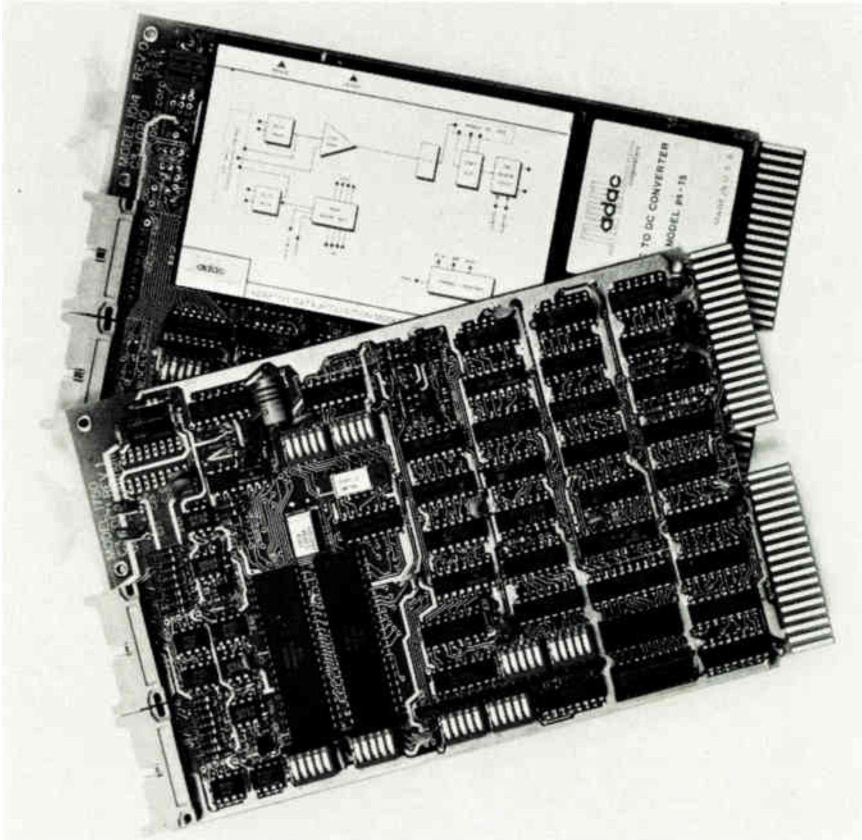
Data-acquisition card has 14-bit resolution; dual-port board saves computer space

With input/output boards for the LSI-11 and LSI-11/2 popping up like mushrooms after a spring shower, a board has to offer something special to create interest in potential users. For Adac's model 1014 data-acquisition system, that something special is 14-bit resolution and accuracy. For the model 1750 dual-port asynchronous serial line I/O card, the key feature is its small-quantity price of $395. Both new boards are dual-width units—8.5 by 5 inches—and are compatible with the Digital Equipment Corp. Q bus.

The model 1014 data-acquisition system has a relatively high throughput rate of 10 kHz. It requires 15 μs to settle and 85 μs to perform a 14-bit analog-to-digital conversion. The system provides 16 single-ended or 8 fully differential channels, which can be expanded up to 64 single-ended or 32 differential using an expander board. Full-scale ranges are selected by means of jumpers, whereas register and vector addressing is done by means of on-board DIP switches.

The temperature coefficient of nonlinearity of the 1014 is less than 1 part per million of full-scale range per °C. The unit's operating temperature range of 0° to 55°C suits it well for conditions in a computer environment. Extensive shielding over the analog circuitry ensures that the computer circuitry will not interfere with the reliable acquisition of input signals.

The 1014 can gain access to the computer in one of three ways: by program control, by program interrupt, or by direct memory access. With either program control or



How do you see fiber optics?

Fiber optics is getting so much publicity from its use in telephone communications that you may see that as its only important application.
It's not.

Optical communication cables are being used in computers, process instruments and control applications. They weigh less and take less space. They eliminate electrical and electronic interference as well as ground loops. They can be more economical. And every day, they're making the old standard interconnect systems obsolete, one by one.

So when you spend time and money on an interconnect system, you should consider fiber optics. And that's where we can help you.

We can help you make the right choices for your system. Choices in line attenuation, mechanical strength, environmental isolation, light coupling efficiency. Choices in every element you need.

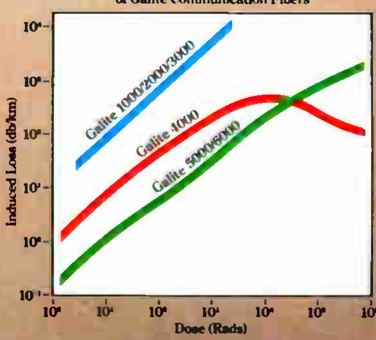
Ours is the broadest line of optical communication cables in the industry. We've been working with fiber optics for 20 years. And engineers have already put more than 2,000,000,000 feet of our fiber optic products in use. Since we make our cables from raw materials to finished product, we can fill your needs exactly. And at the least expense.

Galileo Electro-Optics Corp.
Galileo Park, Sturbridge, Massachusetts 01518

Progress made practical.

As a matter of fact, we can fill your needs more quickly, because all of our standard cables, including Galileo's highly versatile Galite® 3000, are in stock. We even stock complete lines of connectors and electronic components for you.

Radiation Hardness of Galite Communication Fibers

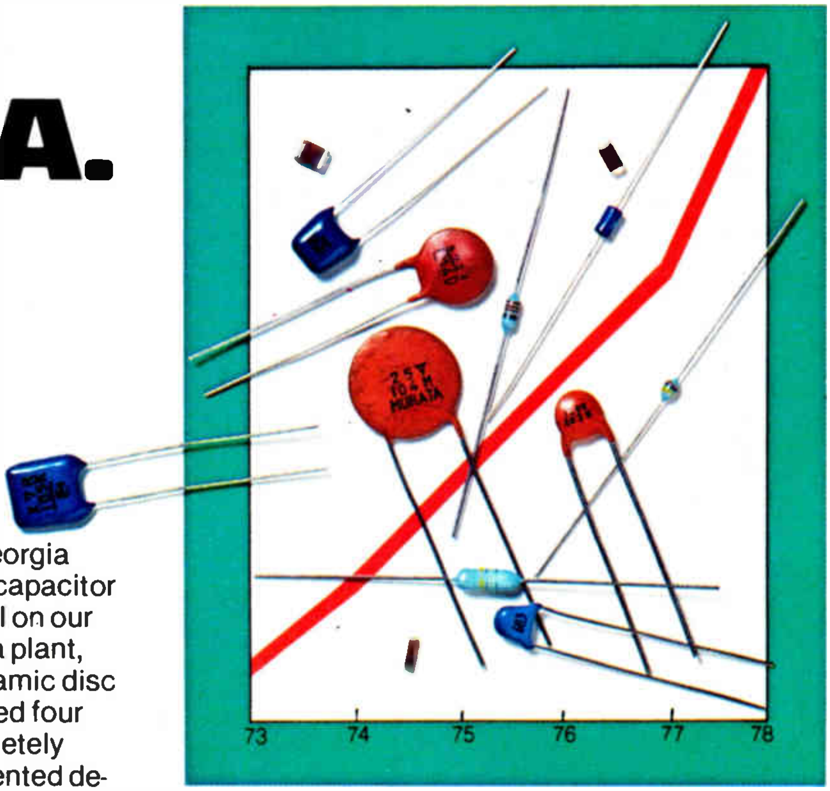


You can write to Galileo for a detailed information package that will give you a good idea of what fiber optics can do for you today. Or you can call Galileo's application engineers at (617) 347-9191 for specific personal help on how... and where fiber optics could fit into what you're doing today.

You will find we offer more than fiber optics. We also offer know-how.

Circle 171 on reader service card

It's no coincidence that Murata-Georgia is the fastest growing ceramic capacitor manufacturer in the U.S.A.



In 1973, we made a decision: Murata-Georgia would create an unsurpassed ceramic capacitor capability and we'd do it fast. We're well on our way. Since 1974, our Rockmart, Georgia plant, already one of the most automated ceramic disc facilities in the world, has been expanded four times. We're presently building a completely automated plant to meet the unprecedented demand for monolithic glass, epoxy and chip capacitors in Douglasville, Georgia. Our corporate headquarters in Marietta, Georgia ties it all together with one of the most sophisticated data processing systems in the industry for inventory control and customer service.

Combine Murata-Georgia's rapidly expanding production capability with a line of ceramic discs, monolithics and high voltage units based on over 30 years of ceramic capacitor experience, and it's easy to understand why Murata-Georgia is the fastest growing manufacturer in the field.

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MURATA CORPORATION OF AMERICA

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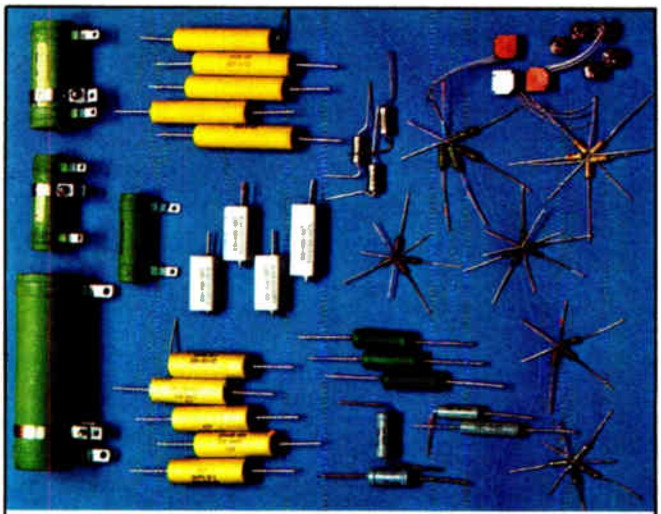
ceramic capacitors, subminiature potentiometers, piezoelectric ceramic filters, resonators and transducers, resistor networks, Posistor® PTC thermistors program interrupt, the 1014 operates as an independent unit. With DMA it can transfer data into the computer memory at its top speed of 10 kHz, according to A. L. Grant, vice president for marketing and sales. Grant expects the 1014 to be used mainly in scientific research and development, although he maintains that some applications also exist in process control and other industrial areas. "The biggest area will be R&D," he says, "but it will sell in all three marketplaces." In quantities of one to four, the system is priced at $1,195.

Compact. Adac's second new Q-bus product, the model 1750 has more going for it than just its $395 price, also in quantities of up to four. The board saves a lot of space by providing two independent serial I/O ports on a single card. Each I/O channel will perform serial-to-parallel and parallel-to-serial data conversions using universal asynchronous receiver/transmitters (UARTs). Transmission may be carried out at switch-selectable rates from 50 to 19,200 bauds. The transmitter will also perform parallel-to-serial conversion of data provided by the LSI-11 bus with a 5-, 6-, 7-, or 8-bit data format; the length of the code is switch-selectable. The receiver does serial-to-parallel conversion with the same format.

Each channel can operate with the following interfaces: RS-232-C, RS-423, RS-422, an optically isolated active 20-mA channel loop, or an optically isolated passive current loop. Jumpers allow each channel to be set up independently for a particular line discipline.

The 1750 contains sockets for a 512-word-by-16-bit programmable read-only memory, which may be used for program storage of bootstraps, down-line loading, or other functions. Alternatively, two 512-byte-by-8-bit fusible-link PROMs can be used to store two 256-by-16-bit arrays. Addressing of one or both arrays is automatically available using wire-wrapped jumper-selectable DEC REV11-compatible addresses.

There will be two major areas in



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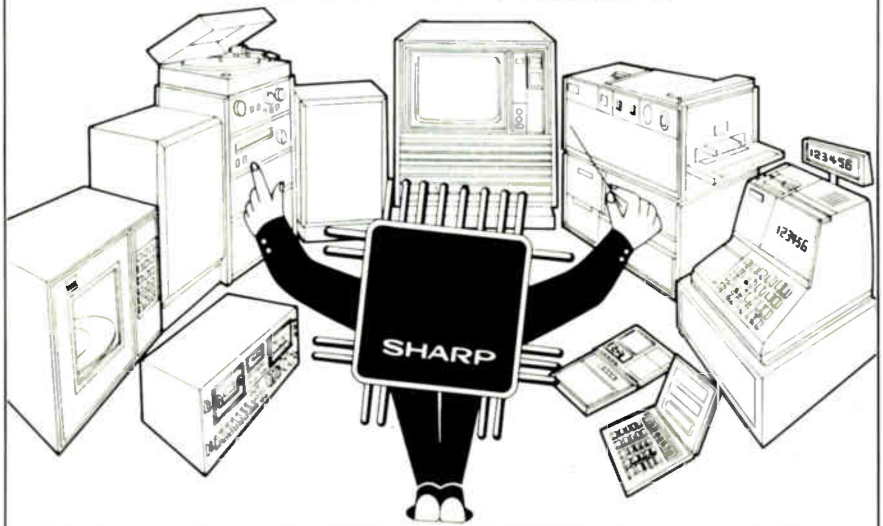
Circle 173 on reader service card

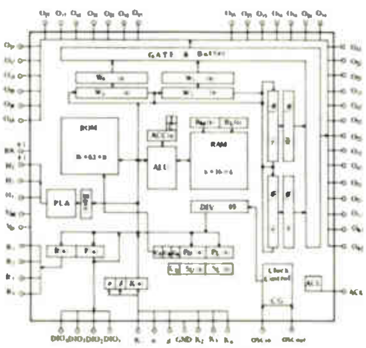
You get a much better performance when the maestro is a SHARP SM-4.



Low power consuming 4-bit one chip C-MOS microcomputer for direct interface with Liquid Crystal Displays (accurate time control with crystal oscillator)

Our little SM-4 delivers a perfectly-orchestrated performance from all kinds of instruments—from calculators to vending machines. And it's not only versatile, it consumes very little energy. Since it contains high RAM/ROM capacities, static shift register, 15-stage divider and other peripheral circuits on one chip, it can be mass produced at a substantial reduction in cost. So at Sharp, we've already put our little semiconductor to work directing the operation of such products as our electronic tape processor and clock-calculators. So look over the numbers behind the SM-4 performance. We think you'll like this little maestro so much you'll end up asking for encores.

ROM capacity	2268 bytes x 8 bits
RAM capacity	96 words x 4 bits
Instructions	54
Subroutine level	1 level
Input port	6 bits
Output port	41 bits
Input/output port	4 bits
Divider	15-stage divider with reset
Drive circuit	LCD internal drive circuit (external RAM drive)
Others	Internal crystal oscillation circuit, internal low voltage detection circuit, single power supply (−3V Typ.) 60-pin quad package



System Construction

Applications
- Clock-calculators
- Programmable remote controls
- Programmable digital timers
- Programmable timing systems
- Multi-function telephone sets
- Cameras, etc

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SHARP ELECTRONICS CORPORATION
10 Keystone Place
Paramus, New Jersey 07652

SHARP

which this card will be used extensively, according to chief engineer Richard B. Plummer. The first is a laboratory situation in which the user has his own computer terminal and there are also floppy disks and line printers—a host-satellite situation. The second is an application in which a large number of peripherals at remote data-gathering locations must be controlled. Current applications for similar serial I/O cards call for up to three full-size cards—two DEC DLV11s and one REV11.

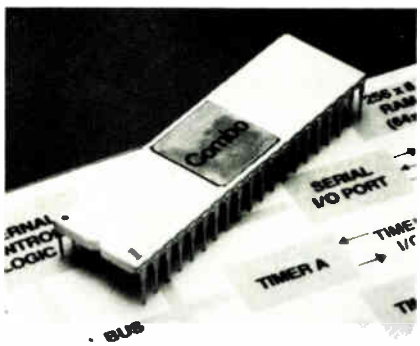
Delivery time for both the 1014 and the 1750 is 30 days after receipt of order.

Adac Corp., 70 Tower Office Park, Woburn, Mass. 01810. Phone Al Grant at (617) 935-6668 [371]

Chip combines extras needed for small system operation

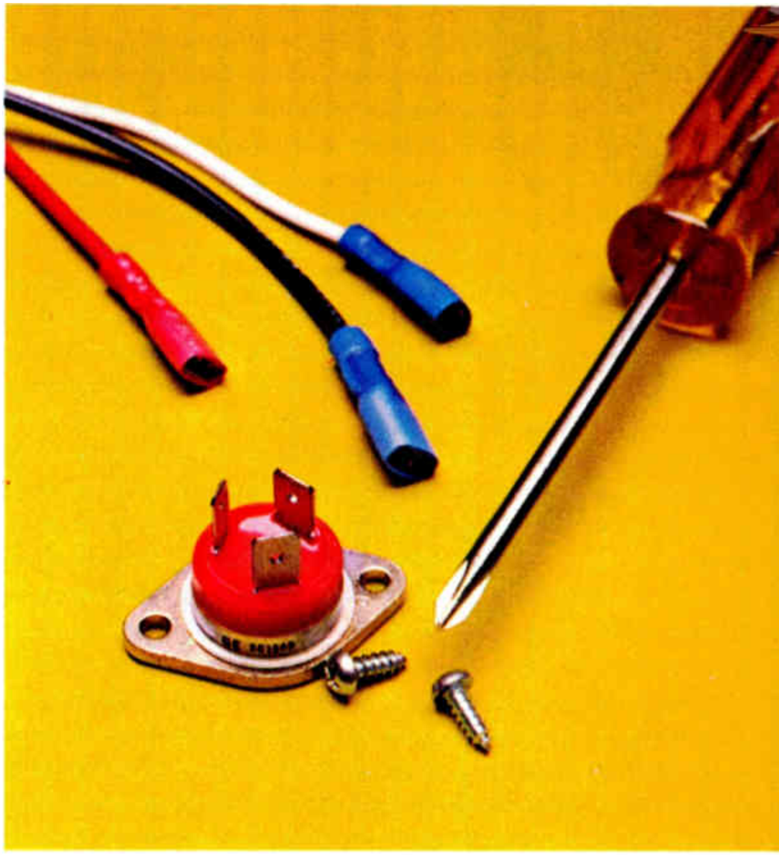
With 256 bytes of static random-access memory (RAM), two timers, a serial input/output (I/O) port and three external interrupts all on a single chip, the MK 3886 "Combo" can form a small control system with a minimal number of additional chips. All that is needed is a central processing unit (such as a Z80), an oscillator circuit, a programmable read-only memory, and a single 5-V power source.

To preserve volatile data, the unit has a low-power standby mode for its lower 64 bytes of RAM, which are also write-protected. The two on-chip timers are software-programmable. In addition to the zero-count output on both timers, timer A has an external-interrupt input linked directly to its control circuitry that



How do GE Econopower™ Triacs cut production costs?

Packaging.



General Electric introduces the SC160 Econopower™ Triac as a direct response to your industrial and appliance needs. You asked us for a low cost, isolated Triac package with FASTON terminals to speed up production and cut assembly costs. So, we've developed the Econopower package that combines these features to meet your needs.

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The new SC160 Econopower Triac has a rating of 25 amperes (RMS), up to 600V. This new user-oriented Triac, attractively priced starting at $2.78 in 10 K lot quantities, is another indication of our Triac leadership. We invented the Triac. We wrote the book on them. And we'll continue to offer new Triac types to meet your needs.

For a free SC160 sample kit, write to General Electric Company, West Genesee St., Auburn, N.Y. 13021; call George Sawchuck (315) 253-7321, Ext. 368, or contact your authorized distributor.

In Europe, contact International General Electric of New York, Dundalk, Ireland, (042) 32371, TELEX: 6500.

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provides two additional timer modes, for pulse width measurement and event counting. Timer B is designed to toggle its output on each cycle, thus generating a square wave that can be tied to the chip's serial I/O port for transmission timing.

The serial I/O port is basically a 16-bit shift register that operates synchronously or asynchronously in a half-duplex mode at an external clock rate, with end-of-word interrupts. The 3886's three interrupt lines allow independently vectored, maskable, priority interrupts from external sources.

Housed in a 40-pin dual in-line package, the 3886 will sell initially for $35.30 in single quantities and will be priced at $17.65 at the 1,000-piece level.

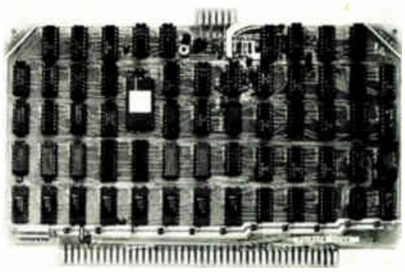
Mostek Corp., Microprocessor Marketing Department, 1215 West Crosby Road, Carrollton, Texas 75006. Phone (214) 242-0444 [373]

Control board gives glitch-free displays

Compatible with Motorola's EXORciser system, the NES002A is a cathode-ray-tube control board that provides glitch-free operation at full processor speed. Display formats of 24 lines of 80 or 84 characters or 25 lines of 80 characters can be chosen. Characters are generated in a seven-by-nine-dot matrix.

The board, which provides either composite or separate sync outputs, is priced at $495 in single quantities. Delivery time is about two to three weeks.

Nixon Engineering Co., 578 Menker Ave., San Jose, Calif. 95128. Phone Robert Nixon at (408) 287-2816 [376]



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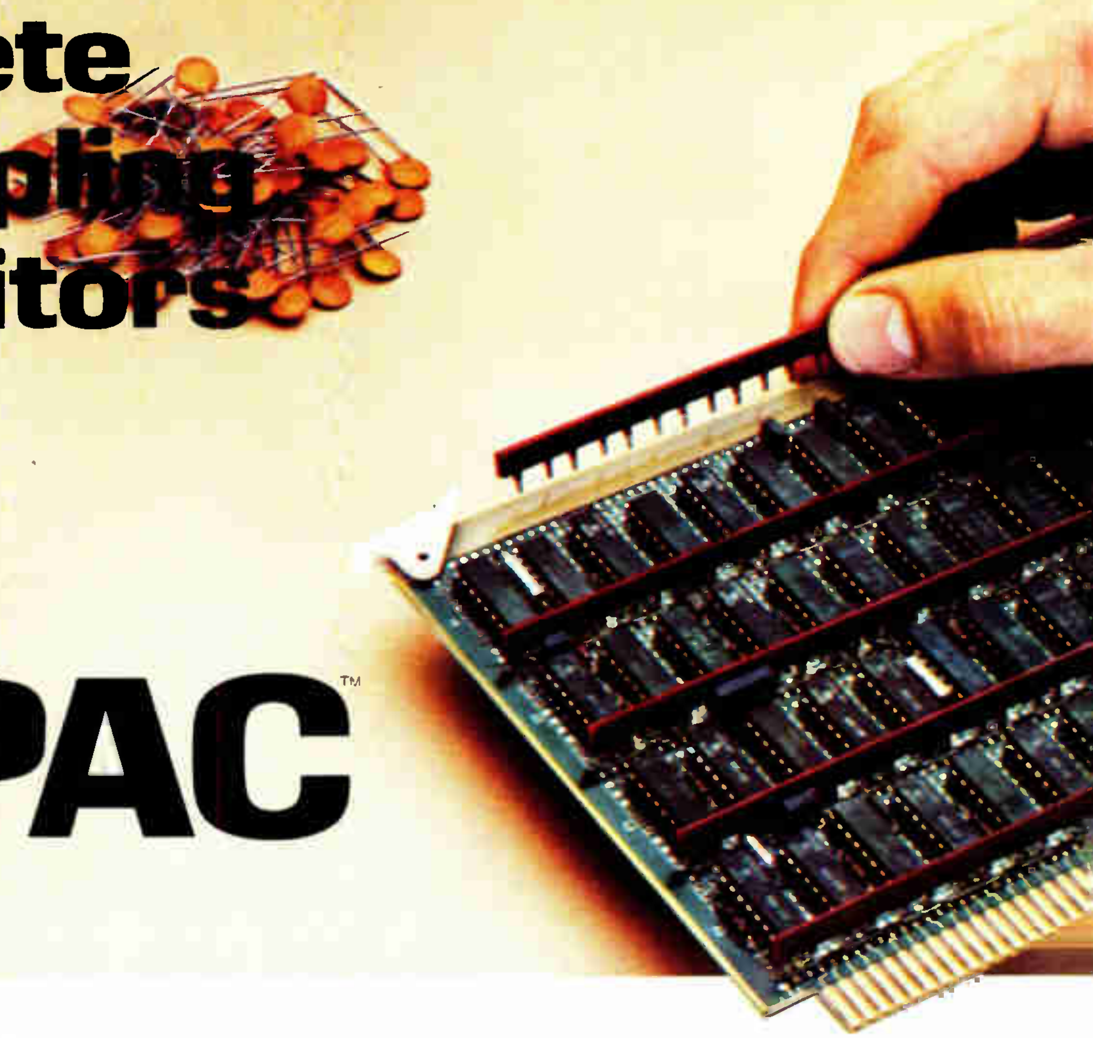

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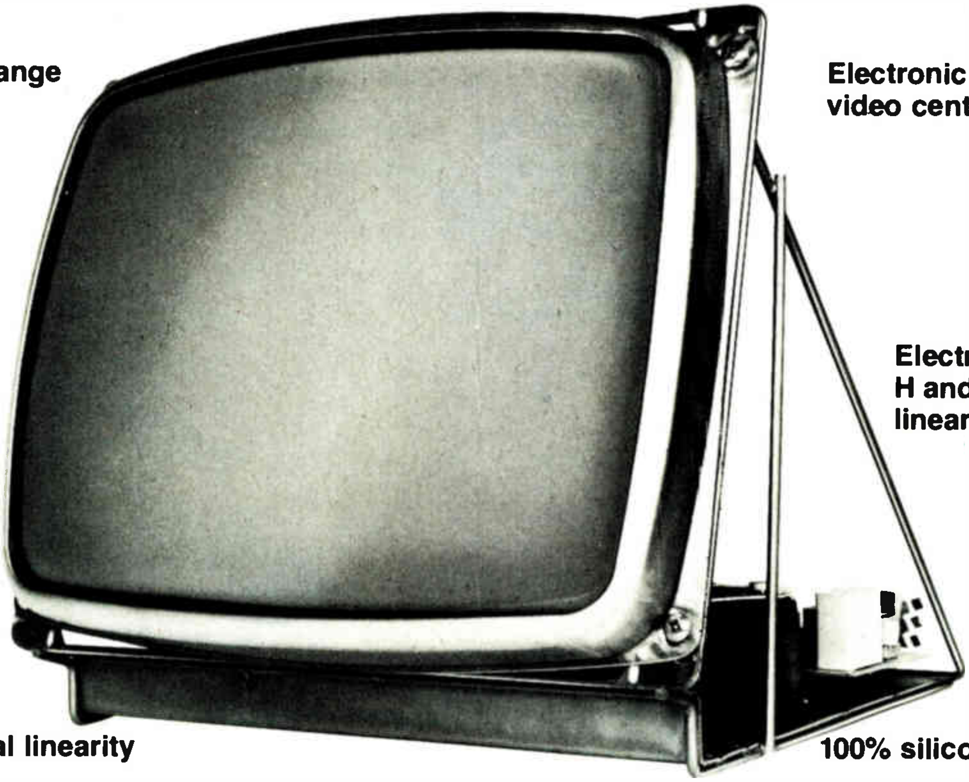

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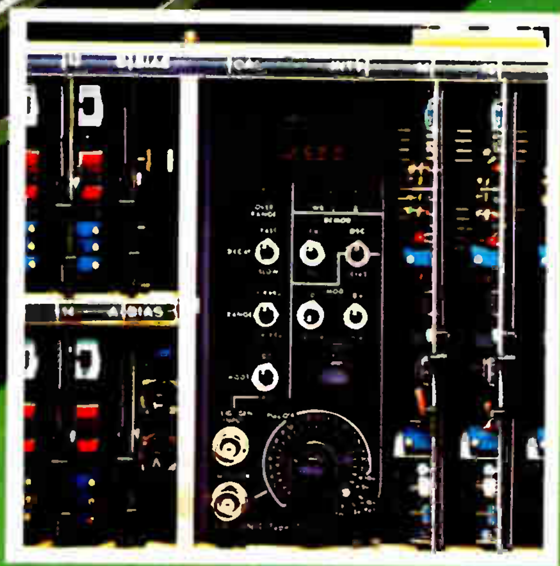

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New products

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Chip implements GPIB interface

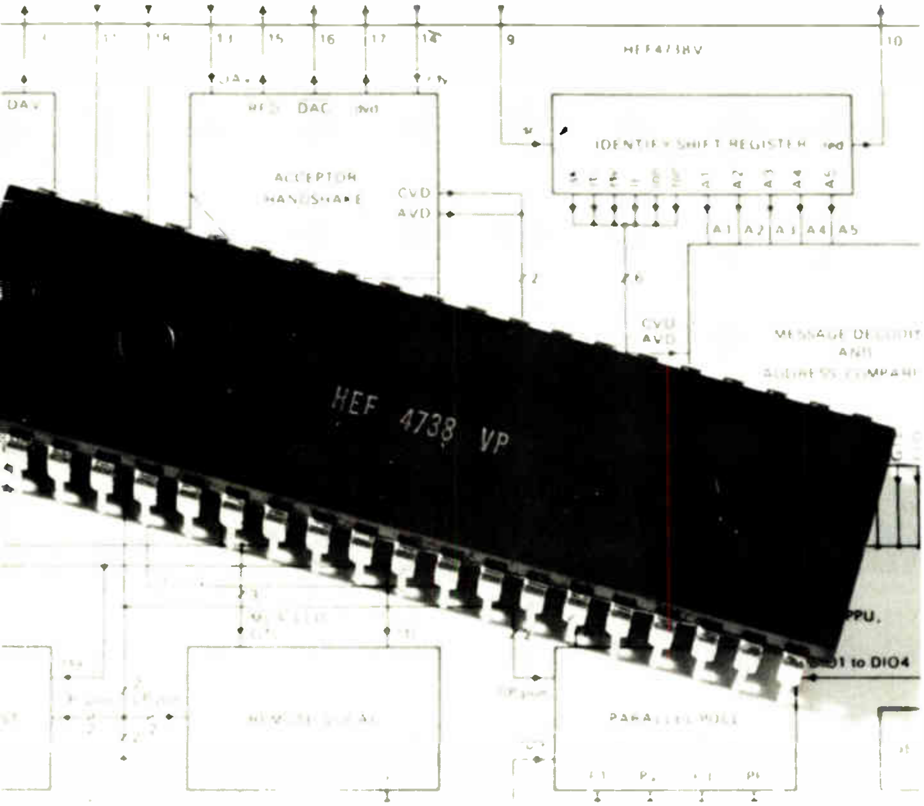
Fabricated in Locmos, device provides complete source and acceptor handshake capability

A monolithic circuit that provides all the functions required to connect a programmable instrument to the IEC/IEEE-488 general-purpose interface bus (GPIB) features both talk and listen modes and fits in a standard 40-pin dual in-line package. Designated the HEF-4738, the chip is fabricated with Locmos (local-oxidation complementary-metal-oxide-semiconductor) technology—a high-density process, which makes it possible to put the circuit on just one chip. Locmos has all of the advantages of C-MOS plus faster operation (comparable to that of transistor-transistor logic) and improved noise immunity. Also, the HEF-4738's inputs may be driven by C-MOS, TTL, and low-power TTL levels, while its outputs are capable of driving TTL buffers.

The chip affords complete source and acceptor handshake capability. It can also be used with instruments that are talkers, listeners, or talker/listeners. It provides complete service-request capability, remote/local operation selection, parallel-poll capability, and device-clear and device-trigger capabilities.

The HEF-4738 can operate from supply voltages between −0.5 and +18 V, but the recommended range is 4.5 to 12.5 V. The maximum current into any input or output is 10 mA, and the power-dissipation rating for the entire package is 400 mW. The device may be operated in ambients between −40° and +85°C and is offered in a choice of plastic or metal-ceramic packages.

The HEF-4738 has been available in Europe from NV Philips Gloeilampenfabrieken, Eindhoven, the Netherlands, developer of both the circuit and the Locmos process. Philips is also the parent company of Signetics, which is marketing the chip in



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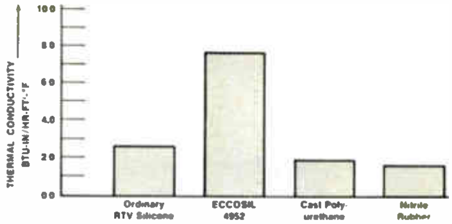

Comparative thermal conductivity graph shows the superior heat dissipation properties of ECCOSIL® 4952 over other various elastomers. ECCOSIL 4952 cures at room or elevated temperature to a flexible silicone rubber capable of withstanding 500°F (260°C). Recommended for potting and encapsulating components from which heat is to be dissipated.

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PLASTIC AND CERAMIC FOAMS

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the U.S. The U.S. price for the plastic-packaged version, in quantities of 25 to 99, is $26.25. Delivery is from stock.

Signetics, P. O. Box 9052, 811 East Arques Ave., Sunnyvale, Calif. 94086. Phone (408) 739-7700 [411]

Decoder-driver family does standard and custom jobs

The MN1205 series is not just another family of decoder-drivers: one member drives four-by-eight matrixes of light-emitting diodes (the MN1205A), others turn on seven-segment LED displays of two digits (the MN1205D and E), and still another handles custom applications. The heart of these units is a programmable logic array (PLA) that, in the last case, can be masked according to a customer's wishes.

Inputs to the complementary-metal-oxide-semiconductor part are in 4-bit nibbles, with two nibbles required to format the 14-line output. Each nibble is latched into either the upper or lower data latch, depending on whether the input signal on the data-select pin has a positive- or negative-going edge. Both nibbles are then fed to the PLA for conversion.

An MN1205 device comes in a plastic, 22-pin, dual in-line package and operates from a single 5-v supply. Standard units are priced at $4.75 each in 1,000s and are deliverable from stock or in up to eight weeks. Custom devices will be supplied in minimum quantities of 5,000.

Electronic Components Division, Panasonic Co., One Panasonic Way, Secaucus, N. J. 07094. Phone Bill Bottari at (201) 348-7276 [413]

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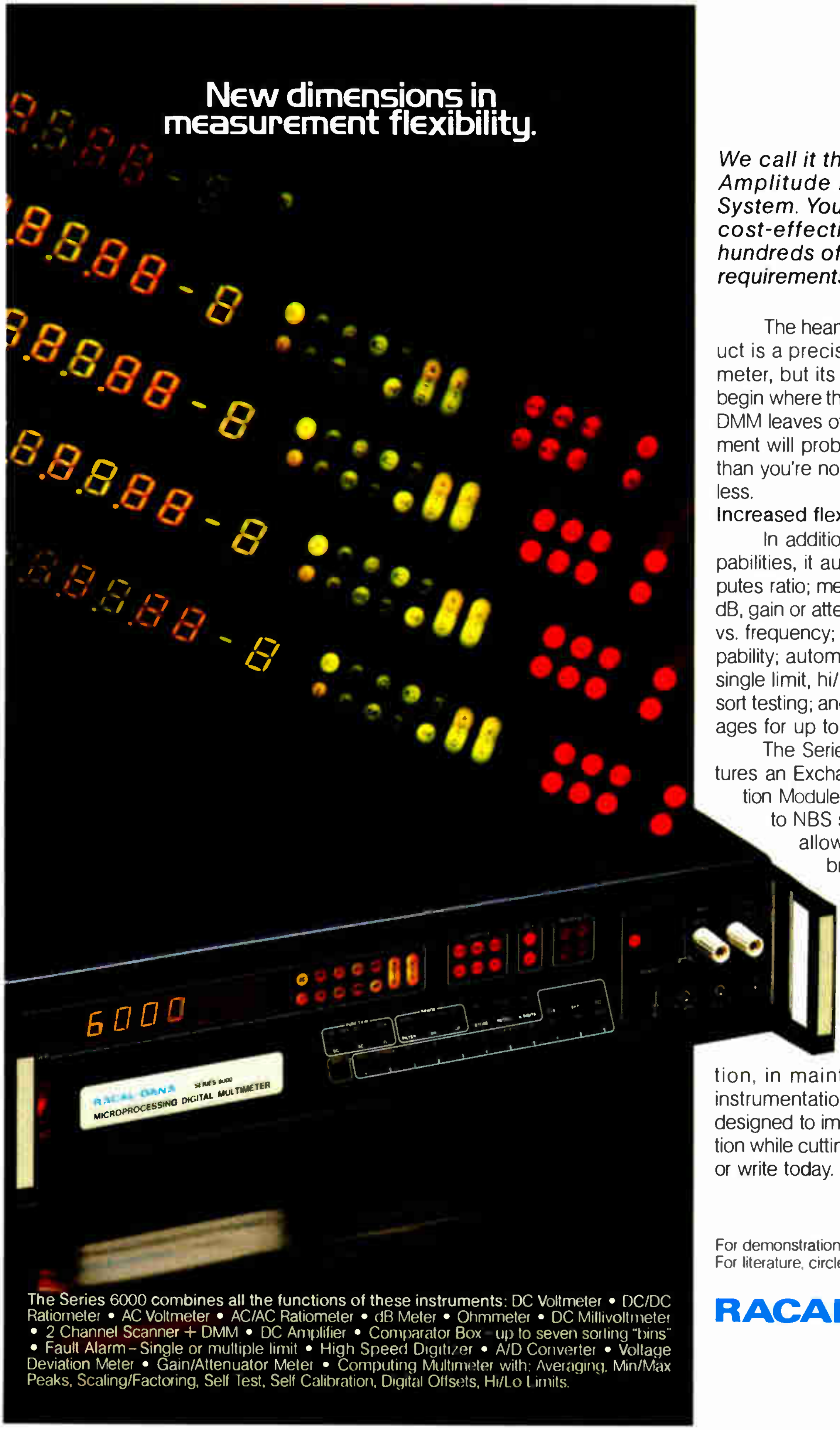

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The heart of this new product is a precision digital multimeter, but its capabilities only begin where the most advanced DMM leaves off. Yet your investment will probably be no more than you're now paying for a lot less.

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Circle 184 for Product Demonstration

Circle 251 for Literature Only

mable read-only memories introduced last spring [*Electronics*, May 25, 1979, p. 224] provide 1,024 by 8

bits of storage. Plug-compatible with earlier 1-K-by-4-bit PROMs, the units are particularly attractive for microcomputer applications.

Like the earlier members, the byte-wide SN74S memories are available in two versions: three-state (478) and open-collector (479) output. They feature maximum access times of 70 ns and maximum enable times of 40 ns and consume 630 mW typically—about the same amount as a 4-K unit.

In 100-piece lots, the PROMs are priced at $21.60 in ceramic packages and $19.35 in plastic. Deliveries will begin this quarter.

Texas Instruments Inc., Inquiry Answering Service, P. O. Box 225012, M/S 308 (Attn: 74S478-479), Dallas, Texas 75265 [414]

Darlington devices drive fluorescent digits or segments

Designed to interface low-level digital logic and vacuum fluorescent displays, the UDN-6116A and 26A consist of six npn Darlington output stages and associated common-emitter input stages. The units may be used either as segment or digit drivers and all outputs can be activated simultaneously.

Pull-down resistors are incorporated in each output stage so that, in most instances, additional components are not needed for a complete interface. The UDN-6116A is compatible with transistor-transistor-logic and 5-V complementary-metal-

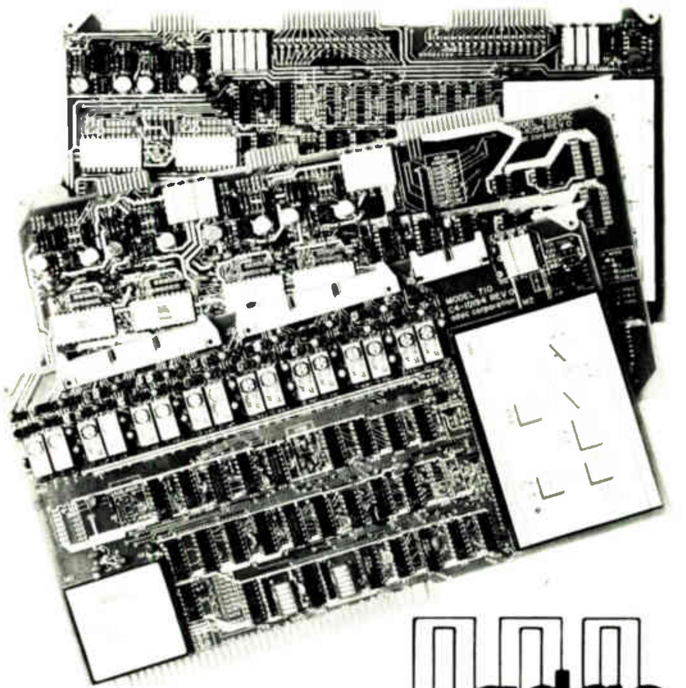
MULTIBUS compatible data acquisition and control systems.

The ADAC 700 Series of data acquisition systems plug directly into the MULTIBUS of single board computers from Intel and National. The 710 Series is the first low level analog to digital system available that includes such unique features as the capability to withstand common mode voltages of up to 250V while digitizing low level outputs from bridges, thermocouples and other low level transducers. A software programmable gain amplifier with optional cold junction compensation circuit can be programmed on a channel to channel basis. The low level analog to digital card and low level multiplexer expander card can be supplied with either 8 or 16 differential inputs per card. Resolution is 12 bits.

The 735 A/D high level analog to digital series is supplied with 16 to 64 single ended or pseudo differential inputs. It also is jumper selectable for 8, 16, or 32 differential analog inputs. The inputs can be either voltage or current loop. The 735 A/D features a 12 bit high speed analog to digital converter with throughput rates of 35 KHz basic and 100 KHz optional. The series include bus interfacing with a software selection of program control/program interrupt and a jumper selection of memory mapped I/O or isolated I/O. Up to 2 channels of 12 bit digital to analog converters can be supplied.

The extensive series of MULTIBUS compatible analog I/O boards is further complemented by the 735 DAC Series. They are supplied with up to 4 channels of 12 bit digital to analog converters, MULTIBUS interfacing, 2 scope/recorder pen control circuits, 8 discrete digital outputs with 8 high current sinks, 8 discrete digital inputs, and memory mapped or isolated I/O interfacing. Optionally available are third wire sense for ground noise rejection and 4 to 20 ma current loop outputs.

Send for full technical data:



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Circle 185 on reader service card

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Division of Valcor Engineering Corp.

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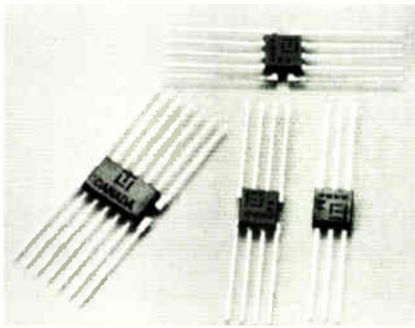
oxide-semiconductor devices; the UDN-6126A works with 6-to-15-V MOS logic.

With either device, the output is activated when the input is pulled toward the positive supply. The drivers work with 5-to-85-V supplies, so they can provide a maximum output voltage of 85 V. Operating from 0° to 70°C, they are priced at $1.17 in lots of 1,000. Delivery is from stock.

Sprague Electric Co., 35 Marshall St., North Adams, Mass. 01247 [415]

Low-voltage amplifiers consume little power

In audio applications where the power budget is tight, series 500 low-voltage linear amplifiers may fit the bill. Available in packages as small as 3.56 millimeters square, the units can operate from battery voltages in the 1-to-2-V range. They consume about 1 mW in the active state and



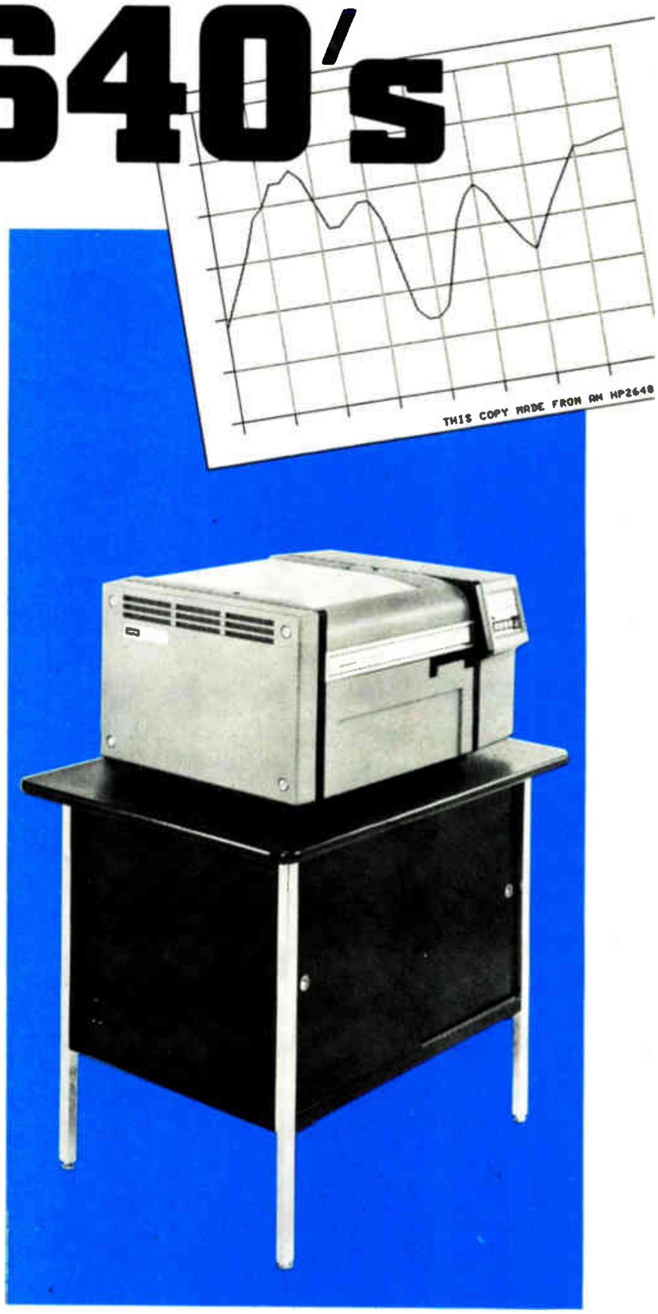
as little as 100 μW when quiescent.

Models can provide gains of up to 70 dB and put out as much as 10 mW, keeping distortion to less than 1%. Some models, intended primarily for portable communications applications, permit automatic gain control. The parts might also be used in cassette recorders.

In 1,000-piece lots, the amplifiers range in price from $3 to $6 each. Sample quantities are in stock and delivery of production quantities takes six to eight weeks.

Linear Technology Inc., 3435 Landmark Rd., Burlington, Ontario L7M 1T4, Canada. Phone Bob Simpson at (416) 335-2996 [416]

CRT COPIER for 2640's



The new Model 8640 CRT copier provides hard copies from HP 2640 Series terminals

in less than 10 seconds

The Houston Instrument 8640 CRT copier, at $4495, provides you with permanent high quality hard copies from any HP 2640 Series terminal equipped with HP's video interface. Utilizing HI's electrostatic technologies, the Model 8640 produces permanent non-fading copies at about one third of the cost of comparable dry silver copies. The Model 8640 is the choice hard copy adjunct to your terminal.

- No warm up time
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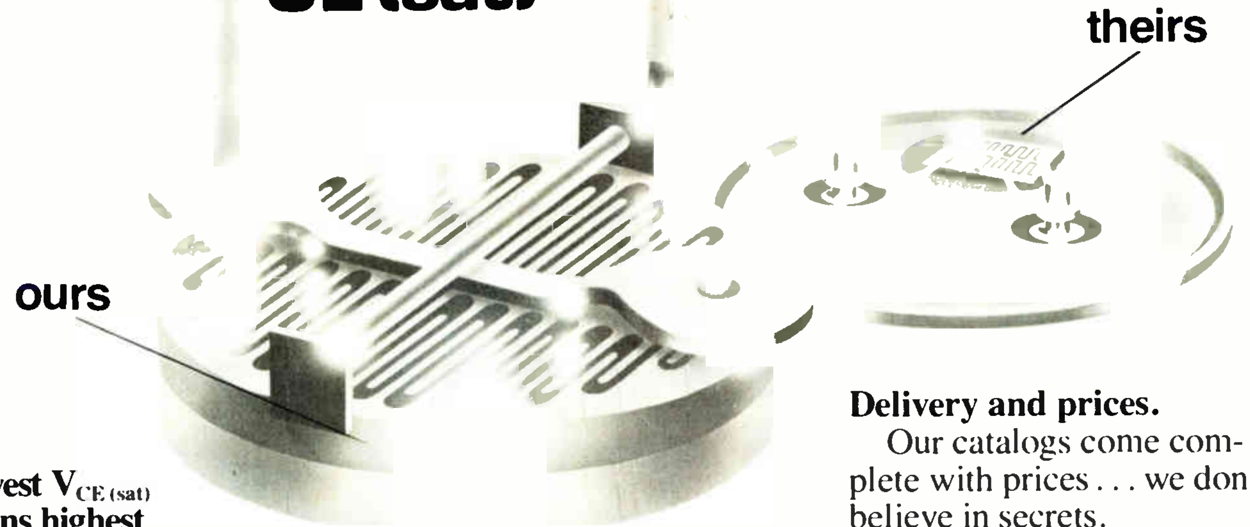
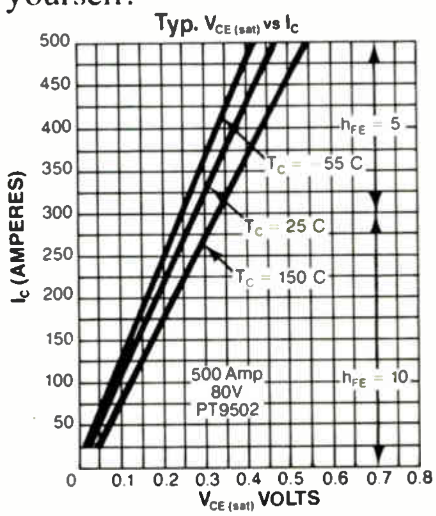


Lowest $V_{CE\,(sat)}$ means highest efficiency

efficiency—this is especially important with transistor operation above 30 Amps. As you know, at high currents most transistors also have $V_{CE\,(sat)}$ in excess of 1.5 Volts. Such high $V_{CE\,(sat)}$ causes loss of efficiency, excess heating and heat-induced reliability problems. PowerTech transistors have a *maximum* $V_{CE\,(sat)}$ rating of *less than* 0.75 Volts at anywhere from 50 to 300 Amps. Compare these ratings to others and judge for yourself.



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$V_{CE\,(sat)}$ Max.	V_{CE}	PART NO.
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0.35V @ 200A	120V	PT-9503
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Exclusively licensed by Intel, our SECS (Severe Environment Computer System) is a functional counterpart of the standard iSBC 80/10A board. Even uses the same development system software.

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Our SECS 80/10A, which uses rugged Intel 883B chips, is mounted on a 9″ by 6″ shock and vibration resistant, full ATR compatible board. Conduction cooled, it operates from −55°C to +85°C. Add our numerous support modules and you end up with a versatile severe environment microcomputer system at a fraction of the development cost.

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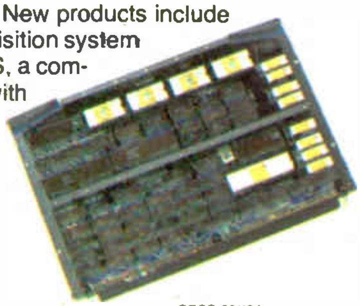

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Data acquisition

I/O boards access memory directly

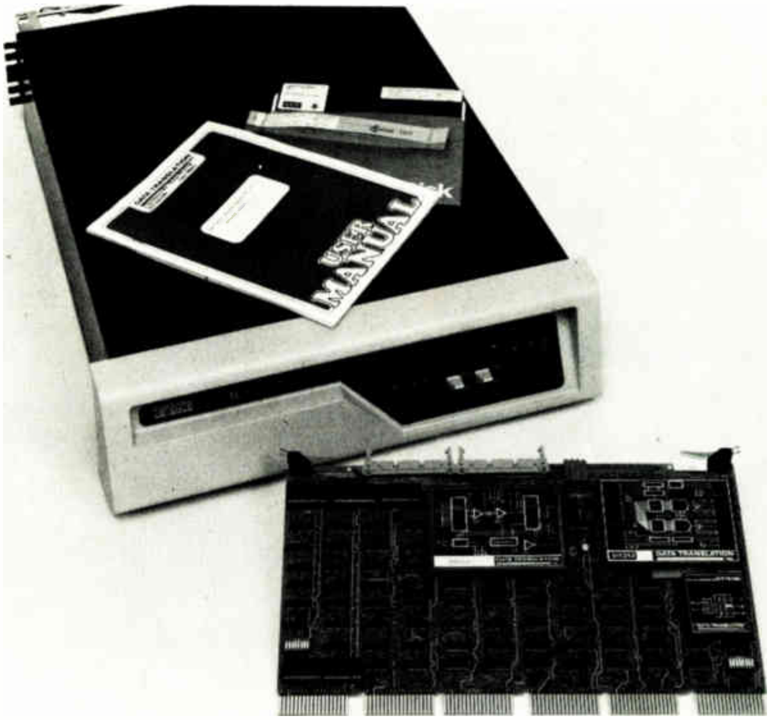
Units for Unibus computers also offer programmable gain and Z-axis point plotting

Users of Digital Equipment Corp.'s PDP-11 Unibus minicomputers, particularly the PDP-11/34, now have another family of analog input/output subsystems that allow the computer to easily handle analog data in laboratory and industrial applications. It's the DT1711 series from Data Translation Inc., which probably packs more capability on the individual hex-size boards than previously available boards.

There are six boards in the series offering various features, but Paul Severino, vice president for engineering, believes the on-board direct-memory-access option of the DT1711 analog I/O board and DT1712 input-only board will be the series' most popular feature, "especially in labs with PDP-11/34s." He adds that he knows of no similar board that offers on-board DMA on both input and output. Fred Molinari, Data Translation's president, points out that when a computer user buys a fast system, such as a PDP-11/34, he wants to get data into and out of memory fast. "When you buy a wizard for a lot of money, you don't want to hobble it, so direct memory access will be attractive," Molinari observes.

The basic 1711 offers 16 single-ended or 8 differential 12-bit input channels, a throughput rate of 35 kHz, and two channels of 12-bit digital-to-analog output with a power amplifier, and Z-axis point-plotting capability for $1,800. The basic 1712 input board provides the 16 single-ended or 8 differential 12-bit channels and the 35-kHz throughput rate for $1,240. The DMA option for both of these adds $500 to the price, and there are two other options for both: a programmable-gain amplifier ($175) and a 100-kHz throughput ($300). The DT1712 is expandable to 64 single-ended channels at additional cost.

The DT1714 is a low-level analog-input board for full-scale signal



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Tektronix Logic Analyzers are versatile. In the synchronous mode, examine software flow using the clock of the system under test—up to 20 ns sampling rate. Switch to asynchronous and sample with the Logic Analyzer's own clock—up to 10 ns sampling rate. Pulse anomalies and timing problems are out in the open, where you can see them. With *one* logic analyzer.

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Contact Tektronix Inc., P.O. Box 500, Beaverton, OR 97077. In Europe, Tektronix, Ltd. P.O. Box 36, St. Peter Port Guernsey, Channel Islands.

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MDB interface products always equal or exceed the host manufacturer's specifications and performance for a similar interface. MDB interfaces are completely software transparent to the host computer. MDB products are competitively priced, delivery is 14 days ARO or sooner.

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MDB also supplies interface modules for LSI-11*, IBM Series/1, Data General and Interdata computers. Product literature kits are complete with pricing.

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*TM Digital Equipment Corp.

Circle 192 for PDP; 253 for LSI; 254 for IBM; 255 for DG; 256 for INTERDATA

ranges from 10 mV to 10 V. It sells for $1,340 with 16 single-ended (8 differential) channels, and otherwise offers the same capability as the 1712. There is also a low-level version of the 1711, the DT1715 I/O board for input ranges from 10 mV to 10 V, which is priced at $1,800.

Completing the family are the DT1718 and 1719. The former is an isolated low-level 12-channel analog-input board, priced at $1,990. It has a 12-bit integrating a-d converter, and programmable or fixed full-scale input ranges from 10 mV to 10 V and provides 250 V of isolation. It and the 1719 are both well suited to industrial applications, where isolation is required.

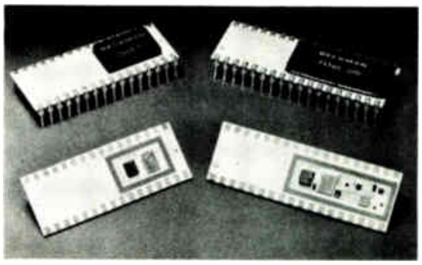
The latter has four channels of analog input, with isolation to 250 V, two channels of nonisolated analog outputs, the same programmable or fixed full-scale input ranges as the 1718, power amplifier output, and Z-axis point-plotting capability.

The 1719 also sells for $1,990. Delivery of all the boards is 30 days after receipt of order.

Data Translation Inc., 4 Strathmore Rd., Natick, Mass. 01760. Phone (617) 655-5300 [381]

C-MOS a-d converters give 12-bit accuracy in 2 bytes

Compatibility with microprocessors, a much touted capability in today's market, is of little value if unaccompanied by the accuracy needed for optimum system performance. Two series of hybrid analog-to-digital converters, however, are now claiming both attributes. Moreover, the complementary-metal-oxide-semiconductor units complement series 7545 and 7546 d-a converters [*Elec-*



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Let's talk business.

Circle 193 on reader service card

tronics, Nov. 24, 1977, p. 141] and are offered at relatively low prices.

The 7555 and 7556 series use successive-approximation techniques to derive outputs with guaranteed 12-bit accuracy. For compatibility with typical 8-bit busing schemes, the converters have three output states (high impedance and logic high and low).

Outputs are available either from the serial output register or in parallel form after the end-of-conversion pin goes high. The parallel output is separated into 2 bytes: one containing the 4 most significant bits (MSB) and the other containing the 8 least significant bits (LSB). A separate inhibit line for each byte controls when it drives the data bus.

Members of both series are linear to within ½ LSB and are available in commercial and military temperature versions. The 7555 converters are made up of a successive-approximation register, a switch-and-clock chip, a thin-film ladder network, and an input scaling resistor; users can add an external comparator and a reference of −10 to +10 V to form a complete conversion system. The commercial version of these units is priced at $26.60 in 100s.

The 7556 units include the 7555 circuitry plus a high-speed comparator and precision −10-V reference. They can perform a 12-bit conversion in 50 μs, typically consume only 200 mW, and sell for $54.80 in hundreds. Both series are available from stock.

Beckman Instruments Inc., Technical Information Section, Advanced Electro-Products Division, 2500 Harbor Blvd., P. O. Box 3100, Fullerton, Calif. 92634 [383]

System acquires data with easy-to-program computer

Where data gathering and system control are subject to variation and refinement, the 7252C data-acquisition system allows operators unfamiliar with sophisticated programming techniques to reprogram quickly with simple keystrokes. The system's computer can be addressed

Our New Spectrum Analyzer MS62C/D does only what it's told.

Some spectrum analyzers give you a pretty picture of their own noise and internally generated spurious signals. Not ours. With a dynamic range of 70 dB and noise of less than −122 dBm, our new MS62C and MS62D come pretty close to showing you only what you put into it. Even with a −30 dBm input signal, spurious components are kept to −100 dBm or less. A wide frequency range from 50 Hz all the way to 1.7 GHz means this is one spectrum analyzer you can use for a wide range of applications: base band, video, radio, or mobile. Controls have been simplified for quick pushbutton operation, and overall size and weight have been reduced for ease in carrying. Operates on a.c., d.c., or battery power. MS62C comes with a normal persistence-type CRT (P7 phosphor), while MS62D comes with a storage-type (P31 phosphor) display screen.

For comprehensive literature on Anritsu's Spectrum Analyzer, contact—

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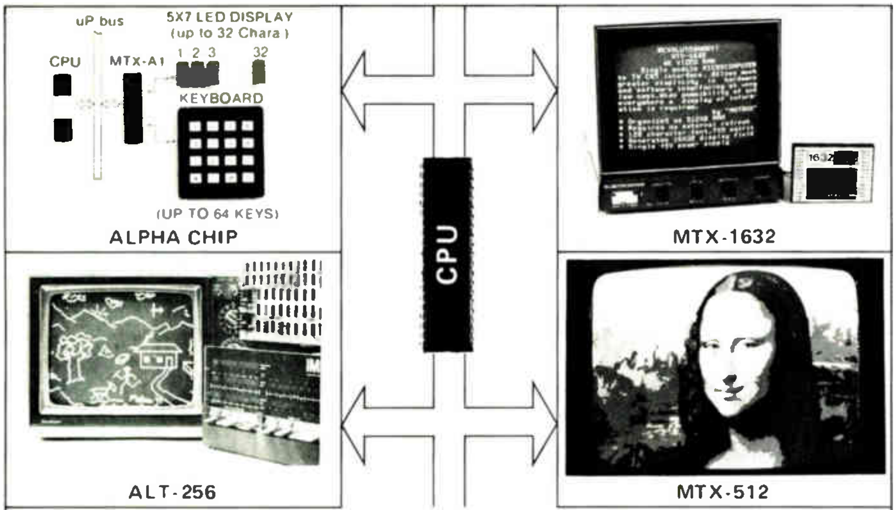
Circle 195 on reader service card



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Circle 196 on reader service card

using a standard ASCII keyboard plus 43 special function keys that provide most Basic instructions.

In addition to performing standard arithmetic operations and mathematical functions, the computer makes transcendental and matrix manipulations of input data. The basic 7252C accepts 10 low-level inputs from such sensors as thermocouples and strain gages, displays readings on a 5½-digit multimeter at a rate of 12 samples per second or in graphic form on its 9-in. cathode-ray tube, and creates reports with its 80-column, 320-character/s printer.

Priced at $15,200, the system comes with 8 kilobytes of read/write semiconductor memory, 89 kilobytes of minifloppy storage (both of which are expandable), and a 42-kilobyte Basic interpreter. Optional input/output expanders are available. Delivery time is 45 days.

FI Electronics, 968 Piner Rd., Santa Rosa, Calif. 95401. Phone Edward Bollet at (707) 527-0410 [384]

D-a converters multiply 20-MHz reference inputs

Engineers who want to provide digital gain control for systems operating at up to 20 MHz can now get a hybrid 10-bit multiplying digital-to-analog converter to do the job. Called the DAC-HA10B, the d-a converter accepts a reference that varies from as much as −12 to +12 V in that frequency band.

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Circle 257 on reader service card

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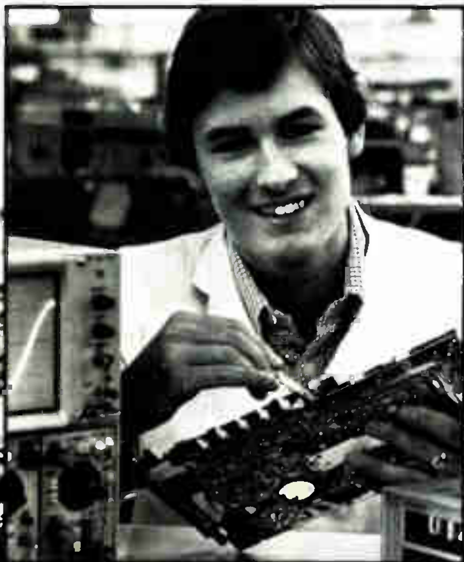
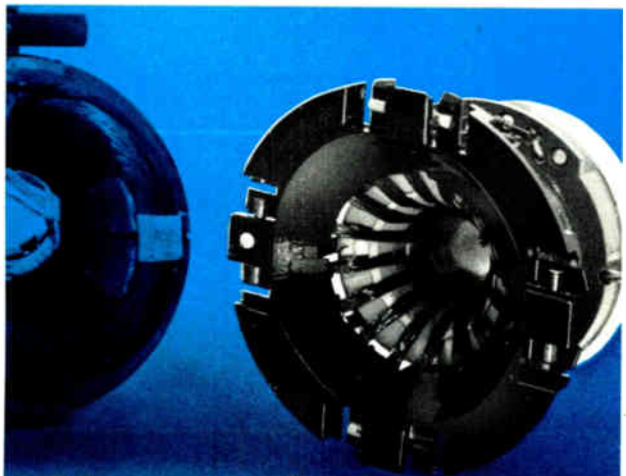
Find out how the people and the province can work for you. Get the facts from Reg Browne or George McLaren at the Northern Ireland Industrial Development Office in New York. They can quickly tailor an offer of assistance to suit your plans. Call (212) 593-2258. Or write: NIIDO, British Consulate-General, 150 E. 58th Street, New York, NY 10022.



Kieran Fitzpatrick works. An apprentice for the past year, he's building a career in electronics with Grundig.

Northern Ireland works.

Circle 197 on reader service card



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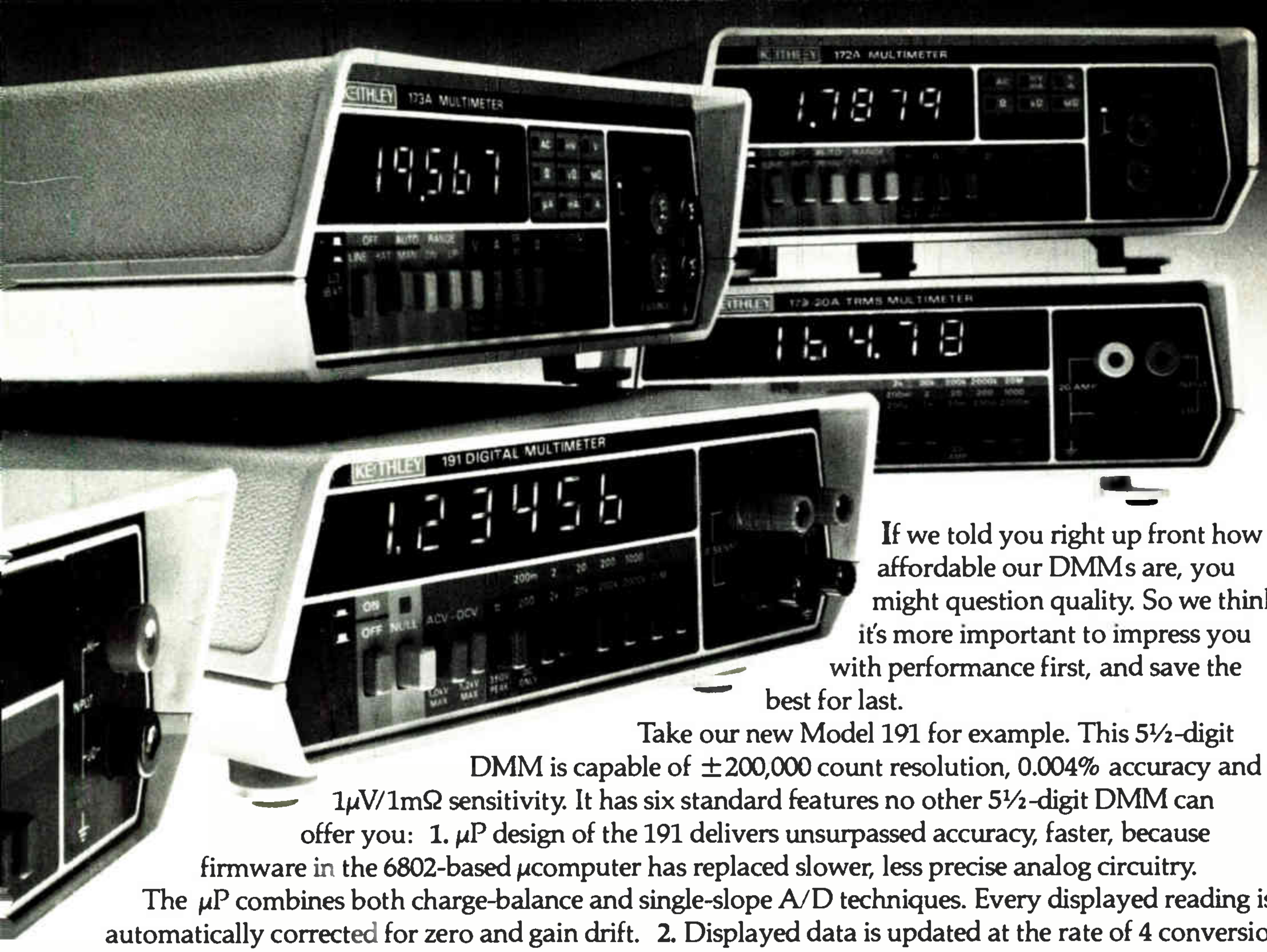

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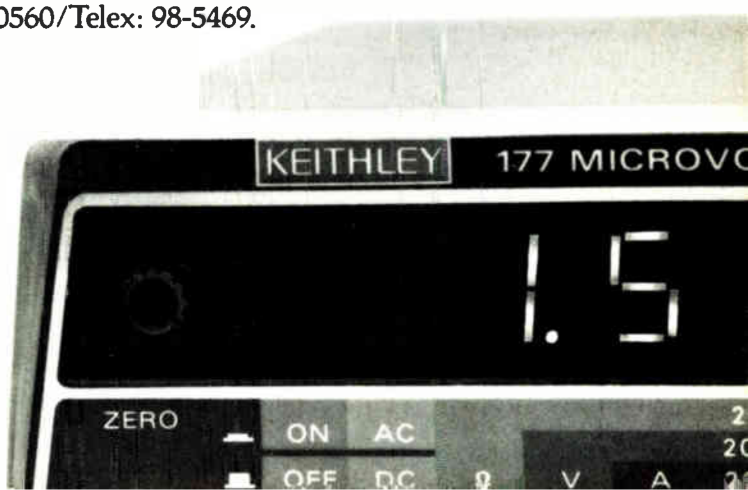
Circle 258 for demonstration
Circle 199 for literature



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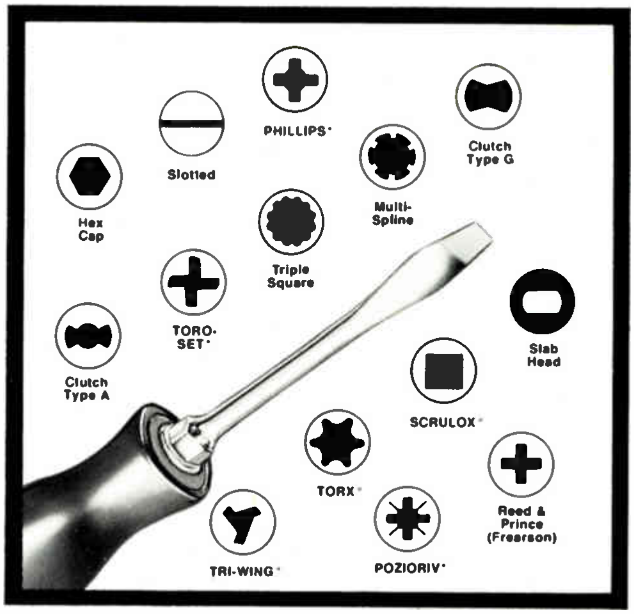

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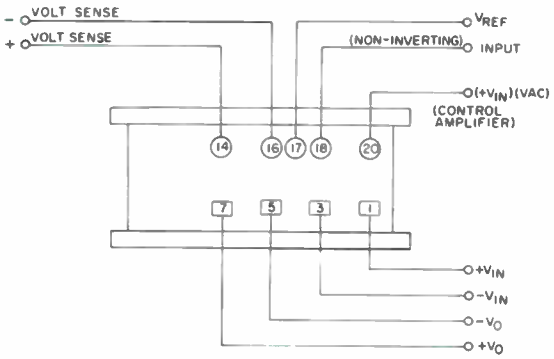
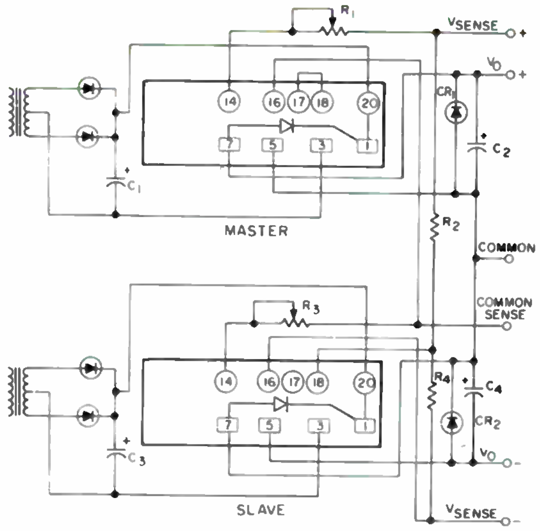
LAS 5000 SERIES

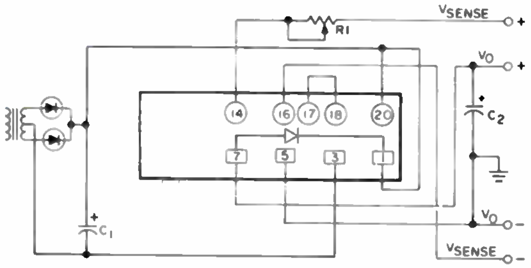
Connection Diagrams



9-PIN POWER HYBRID VOLTAGE REGULATOR



DUAL TRACKING POWER HYBRID VOLTAGE REGULATOR CIRCUIT



POSITIVE POWER HYBRID VOLTAGE REGULATOR CIRCUIT

NOTES

1. Minimum value of input filter capacitors C1 and C3 is determined by: C1, C3 = I_O x (1000 mfd/amp recommended
2. Minimum value of output capacitors C2 and C4 is determined by: C2, C4 = I_O x (100 mfd/amp):
3. Minimum value of output voltage adjust resistors R1 and R3 is determined by: R1, R3 = (0.25V_O x 1000Ω/V) ohms wirewound. Use next highest standard value.
4. Values of tracking reference voltage divider resistors R2 and R4 for all models are determined by:
   a) R2 = (2000V_O – 2490) ohms, ± 1%, ½W film
   b) R4 = 2.49K ohms, ± 1%, ½W film
5. Rectifiers CR1 and CR2 should be rated at peak inverse voltage of 50V and forward current equal at least to maximum rated I_O.

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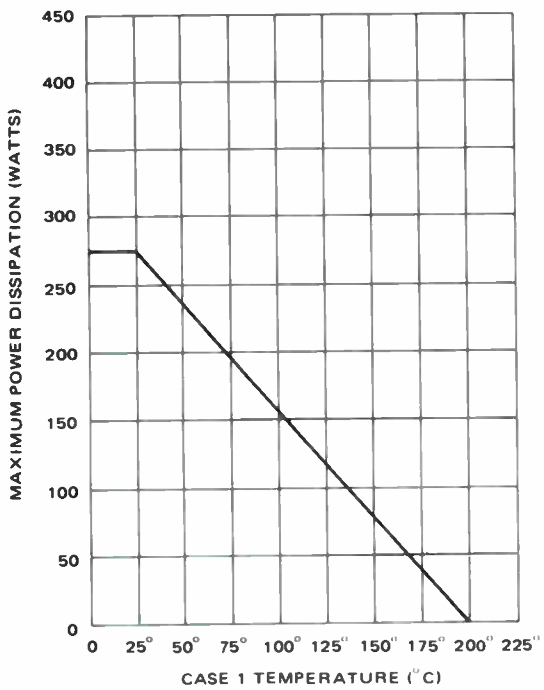
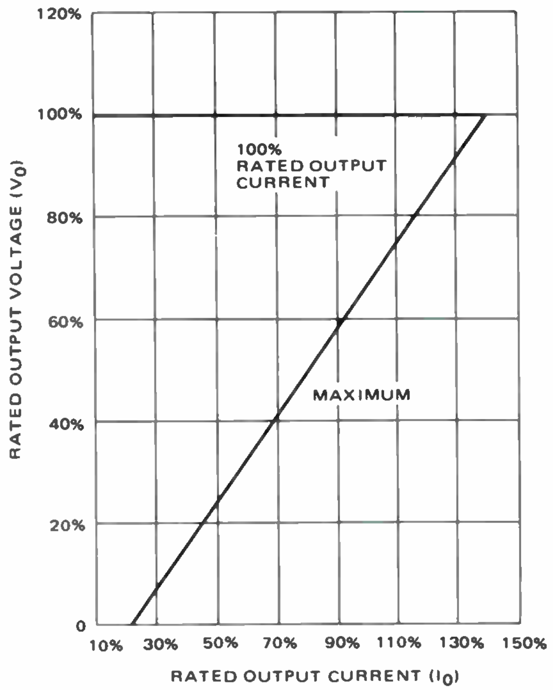
LAMBDA ELECTRONICS

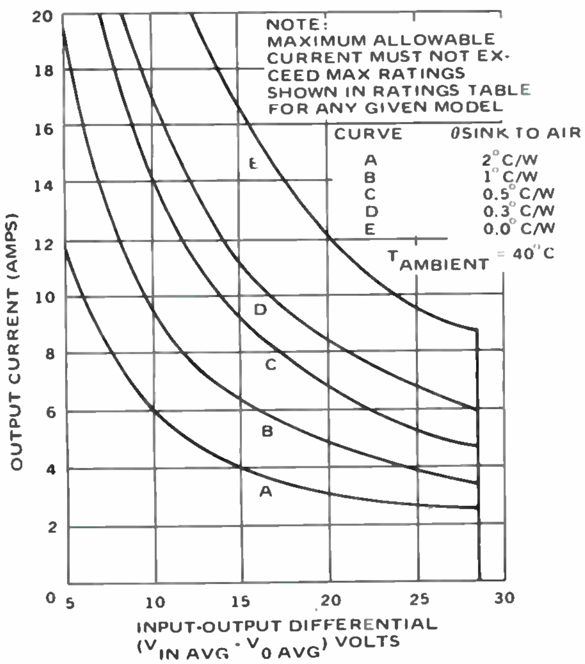
Operational Data

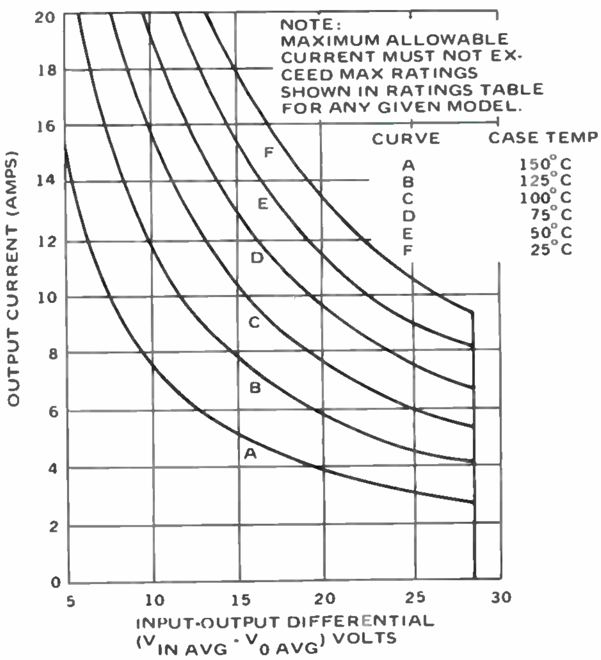


POWER DERATING CURVE AS A FUNCTION OF CASE 1 TEMPERATURE



SHORT CIRCUIT PROTECTION CHARACTERISTIC, LAS 5000 SERIES





DC SAFE OPERATING AREA AS A FUNCTION OF HEATSINK THERMAL RESISTANCE TO AIR AT 40° AMBIENT TEMPERATURE FOR LAS 5000 SERIES

DC SAFE OPERATING AREA AS A FUNCTION OF MODULE CASE TEMPERATURE FOR LAS 5000 SERIES

LAS 5000 SERIES

Regulator Performance Specifications

20 amp, 270 watt positive regulator

General Description

The LAS 5200 Series of Power Hybrid Voltage Regulators is designed for applications requiring a well regulated output voltage for load current variations up to 20 amperes. A key feature of the LAS series of Power Hybrid Voltage Regulators is its construction. A high degree of thermal isolation between the heat generating power elements and the heat sensitive control and reference elements is achieved by the placing of the power section on the heat-dissipating base of the unit, and the control stage on the heat-dissipating upper surface. This thermal isolation results in extremely low thermal drift characteristics for changes in power levels.

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Input voltage to pin (1) [A] [H]	V_{IN} (1)		7.25	40.0	volts
Input voltage to pin (20) [A][G]	V_{IN} (20)		11.9	40.0	volts
Output voltage	V_O		4.75	29.4	volts
Input-output differential [A][F]	V_{IN} (1) − V_O		2.5	28.6	volts
Input-output differential [B][F]	V_{IN} (20) − V_O		7.20	28.6	volts
Output current	I_O			20.0	amps
Standby current	I_Q (1)			30.0	mA
Standby Current	I_Q (20)			7.0	mA
Power dissipation	P_D	Plate #1 @25°C		270.	watts
Power dissipation	P_D	Free Air @25°C Amb		11	watts
Thermal resistance junction–Case #1	θ_j – C1			0.65	°C/watt
Thermal resistance junction–free air	θ_j – FA			12.0	°C/watt
Storage temperature	T_s		−55	+125	°C
Power transistor junction temperature	T_j			+200	°C
Regulation line [C]				0.014	%/ΔV_{IN}
Regulation load [D]				0.2	%
Programming resistance				1000nominal	ohm/volt
Programming voltage				one/one	volt/volt
Temperature coefficient				0.015	%/°C
Ripple attenuation [E]		V_{IN} (1) minimum I_O maximum	60		dB

NOTES:

A Separate DC input voltages for power circuit (pin 1) and control circuit pin (20).

B. Common input voltages for power circuit (pin 1) and control pin (20).

C. Io constant for entire input voltage range from [V_{IN}(1) & V_{IN}(20) min.] to [V_{IN}(1) (20) max.]

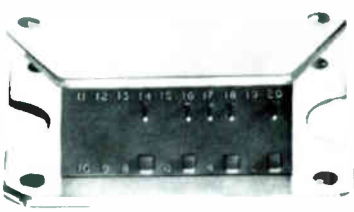
D. V_{IN} constant for entire range from 0 to full load.

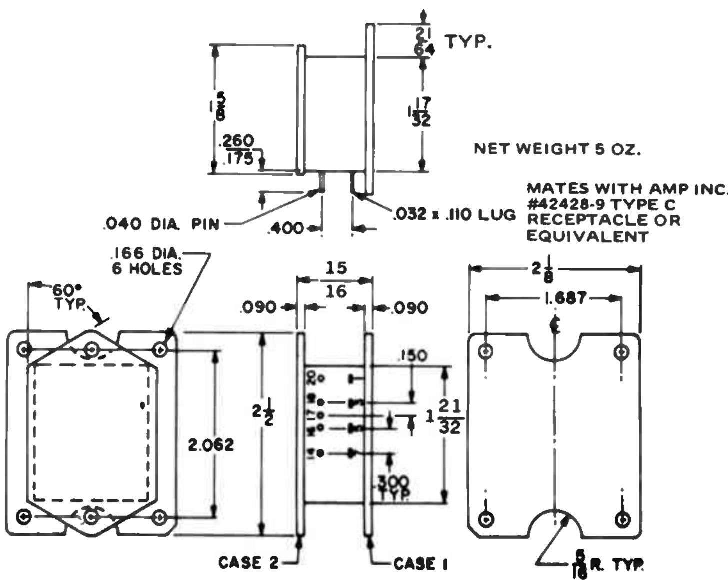
E. Ripple attenuation is 54 dB min. for 24V and 28V models.

F. Minimum input-output differential based on T_j > 25°C.

G. For AC source to Pin 20 with source resistance less than 10 ohms, minimum VAC = 12V rms. For other conditions consult factory.

H. Maximum input voltage is 30V for LAS 5205 and 5206.

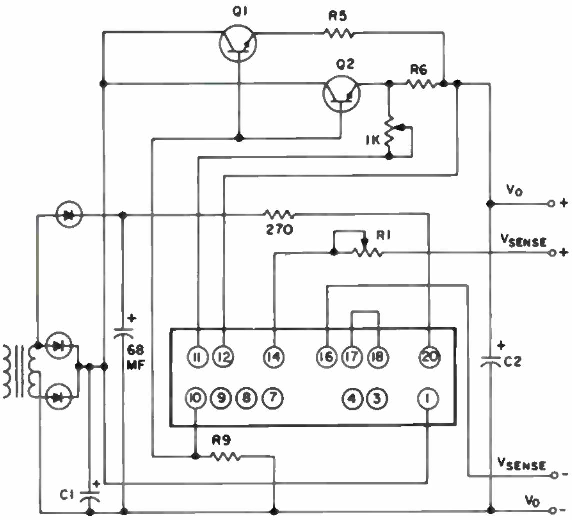




OUTLINE DRAWING, POWER HYBRID VOLTAGE REGULATOR, LAS 5000 SERIES

V_O VOLTS	MODEL	I_O AMPS	PRICE QTY 1-24	25-49	50-99	100-249	250-499	500-999	1000
5±5%	LAS 5205	20	$80	$65	$55	$46	$46	$42	$38
6±5%	LAS 5206	20	80	65	55	46	46	42	38
12±5%	LAS 5212	15	80	65	55	46	46	42	38
15±5%	LAS 5215	15	80	65	55	46	46	42	38
24±5%	LAS 5224	14	80	65	55	46	46	42	38
28±5%	LAS 5228	13	80	65	55	46	46	42	38

Connection Diagrams



POWER HYBRID VOLTAGE REGULATOR USED AS A DRIVER FOR HIGHER CURRENT OUTPUTS USING PEAK DETECTOR FOR CONTROL AMPLIFIER INPUT VOLTAGE

NOTES

1. Minimum value of input filter capacitors C1 and C3 is determined by: C1, C3 = I_O x (1000 mfd/amp) recommended.
2. Minimum value of output capacitors C2 and C4 is determined by: C2, C4 = I_O x (100 mfd/amp).
3. Minimum value of output voltage adjust resistors R1 and R3 for LAS 3205 is 3K ohms. See note 4 to determine value for all other models.
4. Minimum value of output voltage adjust resistors R1 and R3 is determined by: R1, R3 = (0.25V_O x 1000Ω/V) ohms
5. Values of tracking reference voltage divider resistors R2 and R4 for all models are determined by:
   a) R2 = (2000V_O – 2490 ohms ± 1%, ½W film
   b) R4 = 2.49K ohms, ± 1%, ½W film
6. Values of current sharing resistors R5 and R6 are determined by: R5, R6 = (N x 0.5V)/MAX Io ohms ± 3% wirewound where N = number of emitter current sharing resistors required.
7. Nominal value of the current sharing resistor R10 determined from table below:

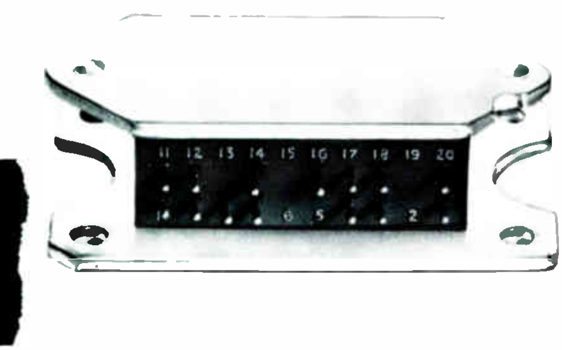
R10	Model
.05Ω	LAS 3205, 3206
.064Ω	LAS 3212, 3215, 3224
.075Ω	LAS 3228

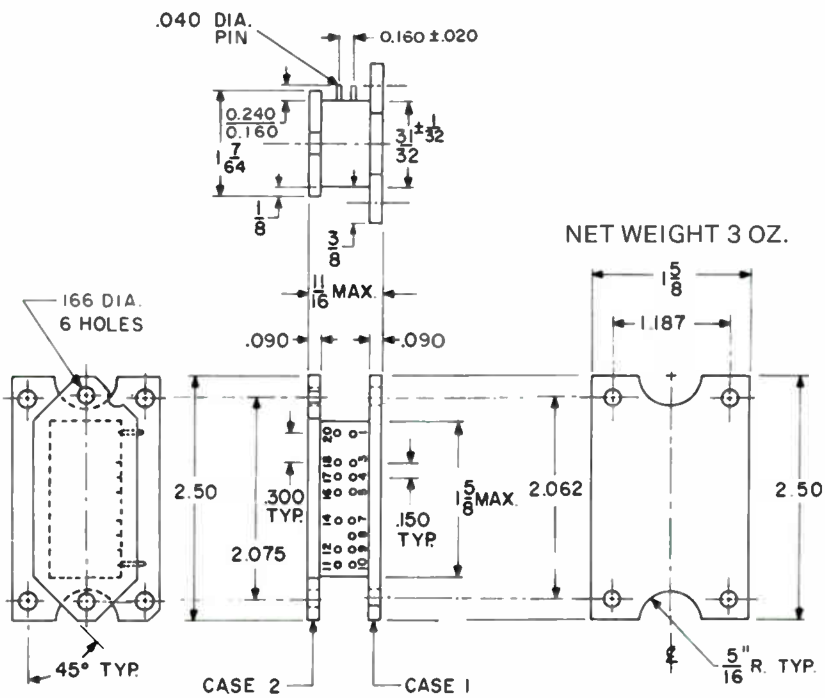
8. Value of current sensing resistor R7 is determined by R7 = 2.5V/I_O ohms, nominal, wirewound.
9. Rectifiers CR1 and CR2 should be rated at peak inverse voltage of 50V and forward current equal at least to maximum rated Io.
10. Value of I_{cbo} drain resistor R9, is determined by R9 = (V_O)/(N x MAX I_{cbo}) ohms, ±5% composition where N = number of external series pass transistors.
11. All fixed resistors shown on diagrams with given values in ohms are ¼W composition.
12. Temperature rise of Case 2, Δ TC_2, is given by the following:
    a) For no external heat sink on case 2.
       $\Delta TC_2 = 0.25 P_D \theta_{J1-A}$
    b) For an external heat sink on case 2 with thermal resistance θ

$$\Delta TC_2 = \frac{\theta \cdot HS_2}{50^\circ \text{ C/W} + \theta HS_2} \times P_D\, \theta_{J1\text{-}A}$$

LAS 3000 SERIES

Outline Drawing

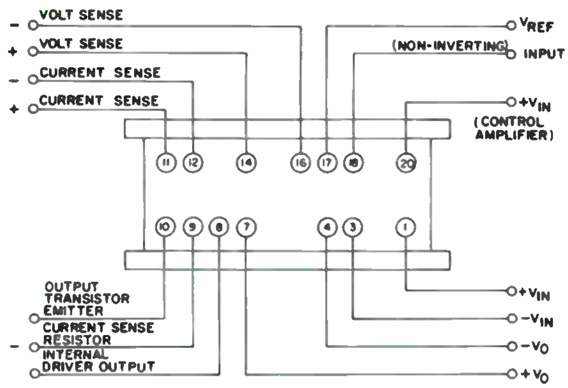




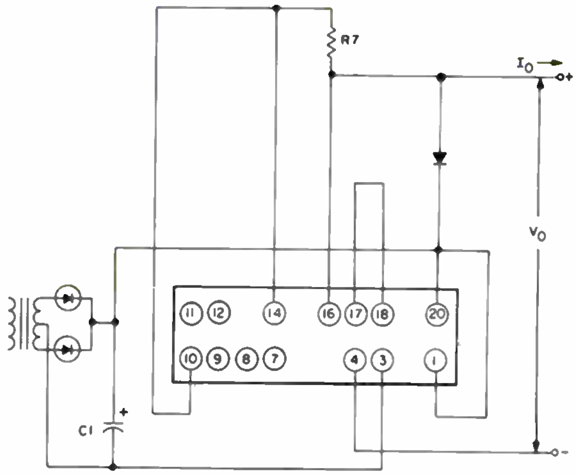
OUTLINE DRAWING, POWER HYBRID REGULATOR, LAS 3000 SERIES

LAS 3000 SERIES

Connection Diagrams

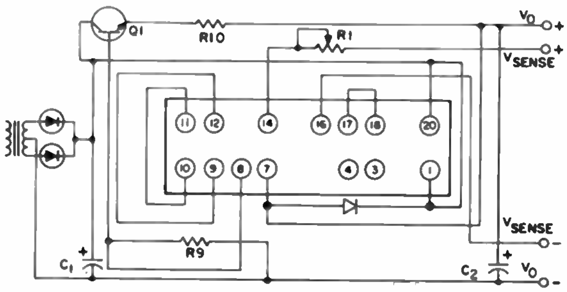


14 PIN POWER HYBRID VOLTAGE REGULATOR

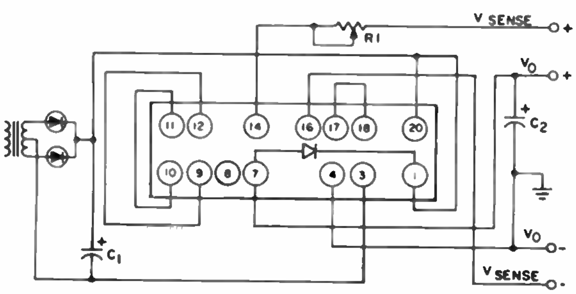


NOTE: V_{IN} MIN = 7.9 + V_0

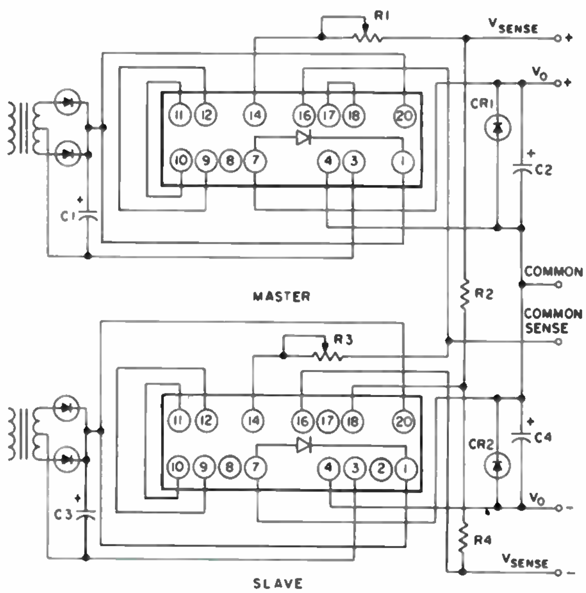
POWER HYBRID CURRENT REGULATOR CIRCUIT FOR LAS 3205 ONLY



POWER HYBRID VOLTAGE REGULATOR USED WITH PARALLEL PASS TRANSISTOR FOR HIGHER OUTPUT CURRENT

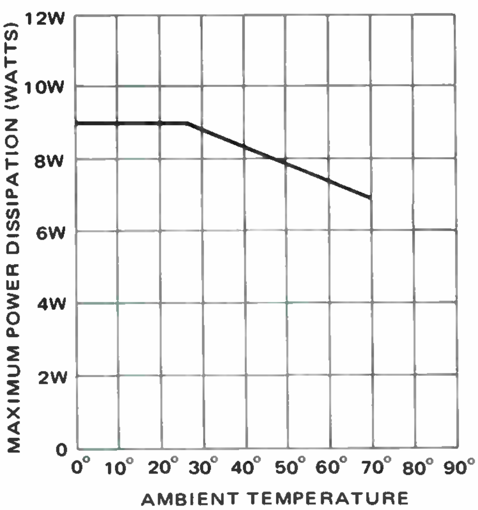


POSITIVE POWER HYBRID VOLTAGE REGULATOR CIRCUIT

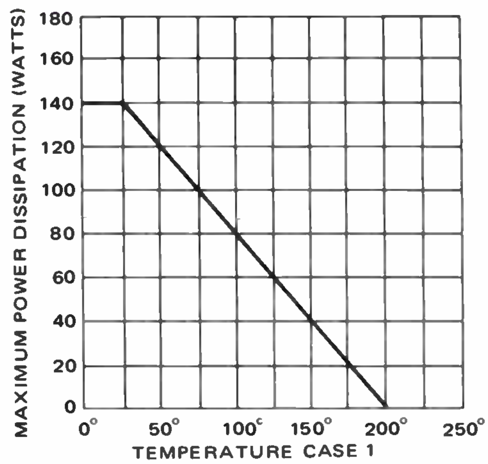


DUAL TRACKING POWER HYBRID VOLTAGE REGULATOR CIRCUIT

Operational Data

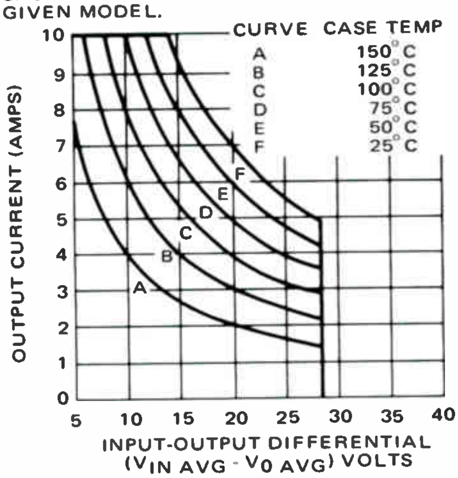


FREE AIR DERATING CURVE



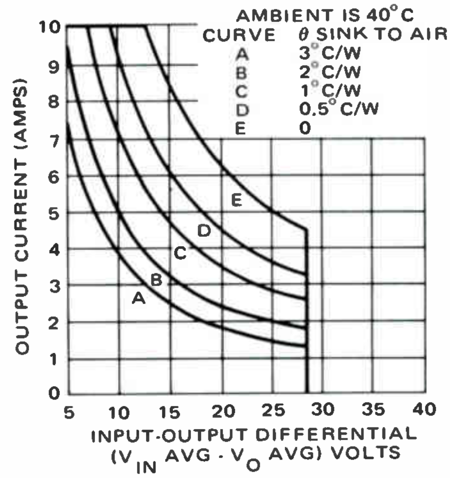
POWER DERATING CURVE AS A FUNCTION OF CASE 1 TEMPERATURE

NOTE: MAXIMUM ALLOWABLE CURRENT MUST NOT EXCEED MAX. RATINGS SHOWN IN RATINGS TABLE FOR ANY GIVEN MODEL.

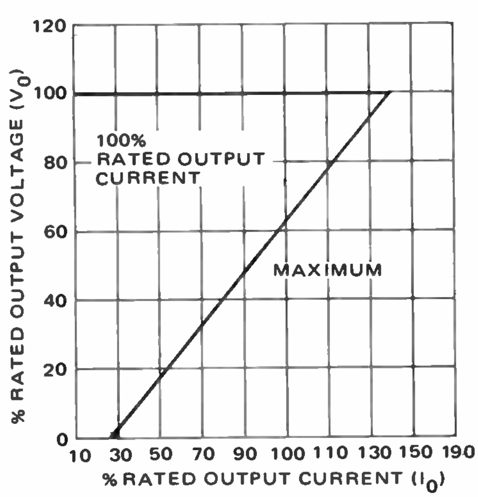


DC SAFE OPERATING AREA AS A FUNCTION OF MODULE CASE TEMPERATURE, FOR LAS 3000 SERIES

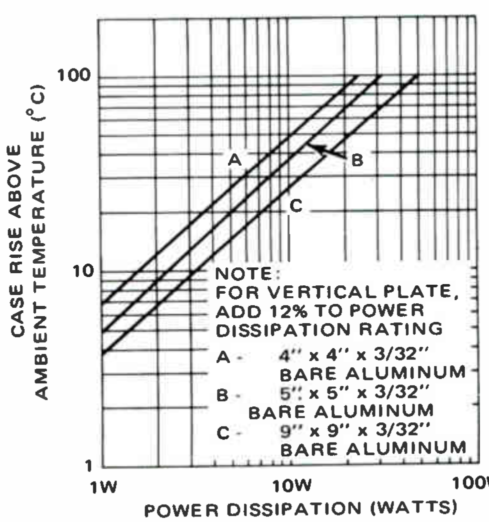
NOTE: MAXIMUM ALLOWABLE CURRENT MUST NOT EXCEED MAX. RATINGS SHOWN IN RATINGS TABLE FOR ANY GIVEN MODEL.



DC SAFE OPERATING AREA AS A FUNCTION OF HEATSINK THERMAL RESISTANCE TO AIR AT 40°C AMBIENT TEMPERATURE FOR LAS 3000 SERIES



SHORT CIRCUIT PROTECTION CHARACTERISTIC



TYPICAL HEAT SINKING DATA FOR HORIZONTAL PLATE

LAS 3000 SERIES

Regulator Performance Specifications

10 amp, 140 watt positive regulator

General Description

The LAS 3200 Series of Power Hybrid Voltage Regulators is designed for applications requiring a well regulated output voltage for load current variations up to 10 amperes. A key feature of the LAS series of Power Hybrid Voltage Regulators is its construction. A high degree of thermal isolation between the heat generating power elements and the heat sensitive control and reference elements is achieved by the placing of the power section on the heat-dissipating base of the unit, and the control stage on the heat-dissipating upper surface. This thermal isolation results in extremely low thermal drift characteristics for changes in power levels.

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Input voltage to pin(1) (A)(G)	$V_{IN}(1)$		5.2	40.0	volts
Input voltage to pin(20) (A)	$V_{IN}(20)$		7.9	40.0	volts
Output voltage	V_O		2.7	29.4	volts
Input-output differential (A)(F)	$(V_{IN}(1) - V_O)$		2.5	28.6	volts
Input-output differential (B)(F)	$(V_{IN}(20) - V_O)$		5.2	28.6	volts
Output current	I_o			10.0	amps
Standby current	$I_Q(1)$			20.0	mA
Standby current	$I_Q(20)$			7.0	mA
Power dissipation	P_D	Plate #1 @25°C		140	watts
Power dissipation	P_D	Free Air @25°C Amb		9	watts
Thermal resistance junction—Case 1	θ_j - C1			1.25	°C/watt
Thermal resistance junction—Free Air	θ_j - FA			15	°C/watt
Storage temperature	T_s		-55	+150	°C
Power transistor junction temperature	T_j			+200	°C
Regulation line (C)				0.01	%/ΔV_{IN}
Regulation load (D)				0.2	%
Programming resistance				1000 nominal	ohms/volt
Programming voltage				one/one	volt/volt
Temperature coefficient				0.015	%/°C
Ripple attenuation (E)		$V_{IN}(1)$ Minimum 60 I_o Maximum			dB

NOTES:

A. Separate DC input voltages for power circuit (pin 1) and control circuit pin (20).
B. Common input voltages for power circuit (pin 1) and control pin (20).
C. Io constant for entire input voltage range from [$V_{IN}(1)$ & V_{IN} (20) min.] to [$V_{IN}(1)$, (20) max.]
D. V_{IN} constant for entire range from 0 to full load.
E. Ripple attenuation is 54 dB min for 24V and 28V models.
F. Minimum input-output differential based on T_j, > 25°C.
G. Maximum input voltage is 30V for LAS 3205 and LAS 3206

V_o VOLTS	MODEL	I_o AMPS	PRICE QTY. 1-24	25-49	50-99	100-249	250-499	500-999	1000
5V ± 5%	LAS 3205	10	$38	$34	$29	$25	$25	$21	$20
6V ± 5%	LAS 3206	10	38	34	29	25	25	21	20
12V ± 5%	LAS 3212	8.5	38	34	29	25	25	21	20
15V ± 5%	LAS 3215	8	38	34	29	25	25	21	20
24V ± 5%	LAS 3224	7.5	38	34	29	25	25	21	20
28V ± 5%	LAS 3228	7	38	34	29	25	25	21	20

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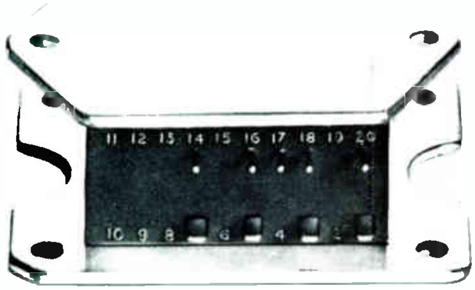

ACTUAL SIZE

THIS HYBRID REPLACES... ALL THESE PARTS

Up to 28V, up to 20A—0.01% line reg. 0.2% load reg.
built-in short circuit and overload protection

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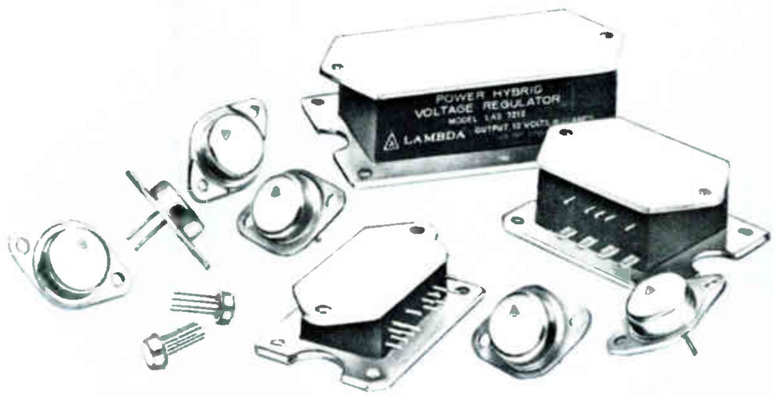


LAMBDA SEMICONDUCTORS

Components

52¢ beeper stands only 0.79 in. high, is clearly audible

Beepers, small transducers that emit tones of approximately 2.1 kHz, are turning up in everything from microprocessor-based toys and pocket pagers to remote-control units for telephone answering systems. The QMB series promises to make these chirpers even more nearly ubiquitous, for the small devices—they measure only 0.63 in. in diameter by 0.79 in. high, including pins—are priced at just 52¢ in quantities of 1,000 or more.

The series consists of three models that differ by dc voltage rating: 1.5, 6, and 12 V. Each consists of a coil and a metal cone with a rare-earth magnet. The resistance of the coil varies directly with the voltage ratings, and for the three models the coils are 165, 260, and 430 Ω.

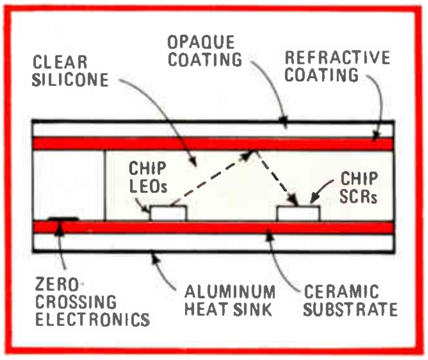
With an input signal of 2.1 kHz, the low-voltage model requires only a 15-mA driving current and the higher-voltage models need 30 mA. At 8 in. from the unit, the clearly audible signal has a minimum sound-pressure level of 70 dB.

Unlike other beepers, the QMB operates at frequencies as low as 1 kHz and voltage levels as low as 1 V, but, like audio speakers, the unit functions best in matched-impedance circuits. It is housed in a polyacetal resin package and has pins spaced on 0.3-in. centers. Delivery is from stock to five weeks.

Star Micronics Inc., 200 Park Ave., Suite 2308, New York, N. Y. 10017. Phone Arnie Peters at (212) 986-6770 [341]

Solid-state relay refracts light

There's a new kind of solid-state relay in town—one that couples the output from light-emitting diodes to the gates of silicon controlled rectifiers through a light path of clear silicone epoxy. The result is a device, called the OptoFilm solid-state relay, that can switch up to 2A with a 50-mA input.



Moreover, its price is attractive: $3.90 each in 10,000-piece quantities, with the promise of dropping significantly under $3 in the near future. Also, a 5-A device is just a couple of months away.

"We tried to ignore everything that had been done before and to attempt completely different things," says Ed Rodriguez, president of the manufacturer, Theta-J Corp., and its main idea man.

OptoFilm is indeed unusual. Truly a semiconductor device, it can be fabricated using hybrid technology. It uses the refractive properties of materials to reflect light from a pair of LED chips onto a pair of SCR chips, as shown in the figure. One LED-SCR pair switches the ac load voltage on; the other switches it off.

The relay can isolate up to 3,750 V ac from input to ouput and also maintains a maximum peak repetitive off-state voltage of ±400 V dc. It has switching times of 8 ms and a leakage current of 100 μA.

Theta-J Corp., 208 Cummings Park, Woburn, Mass. 01801 [342]

Optocoupler outputs linearly while isolating to 7,500 V

To isolate a measurement system from an analog signal sensed by, say, a thermistor or medical electrode, designers have resorted to building their own circuits. Usually, such circuits contain an optocoupler, sometimes called an optoisolator, as well as an op amp and discrete transistor to linearize the coupler's output. Now, however, designers can purchase an optocoupler whose output is linear up to 250 kHz, typically, and whose isolation capability is 7,500 V, peak.

Designated MOC5010, the component consists of a gallium-arsenide infrared-emitting diode (IRED) optically coupled to a bipolar monolithic amplifier. Input currents are amplified at a gain of 200 mV/mA to provide outputs of up to 4 V, peak to peak. The emitter-follower output impedance is typically less than 200 Ω.

The UL-recognized device comes in a six-pin, plastic, dual in-line package and works from a 12-V supply. It is available from stock and is priced at $3.25 in lots of 100 or more.

Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Ariz. 85036. Phone (602) 244-4556 [343]

Power inductors come in pigmy packages

Though quite small, type LL series inductors are very much at home with relatively large currents. The 0.49-in.-long, 0.365-in.-diameter elements are available in six inductance and current values ranging from 120 μH and 1.6 A to 5,000 μH and 0.25 A.

Hermetically sealed to meet the requirements of MIL-T-27, the units

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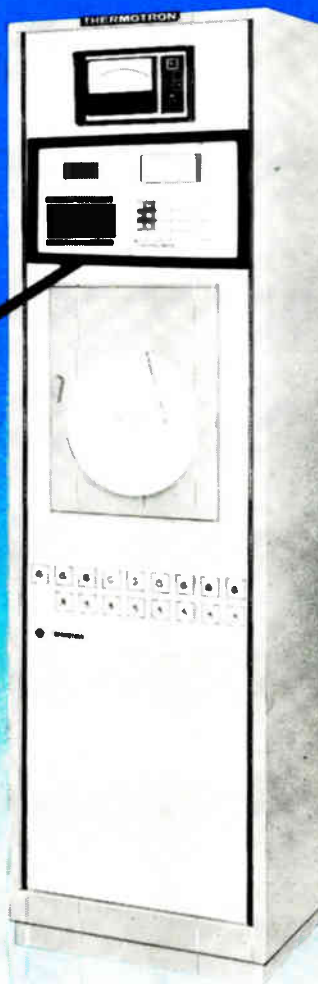

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Circle 210 on reader service card

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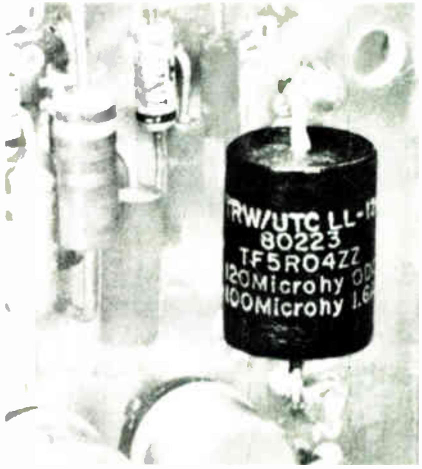


are specified at 1 V and 20 kHz. At rated dc current values, the inductors experience a rise in temperature of approximately 40°C and a drop in inductance not in excess of 20%. In production quantities, type LL inductors sell for less than $5.50 each and delivery of the units is from stock to eight weeks.

TRW/UTC Transformers, 150 Varick St., New York, N. Y. 10013. Phone Austin Profeta at (212) 255-3500 [345]

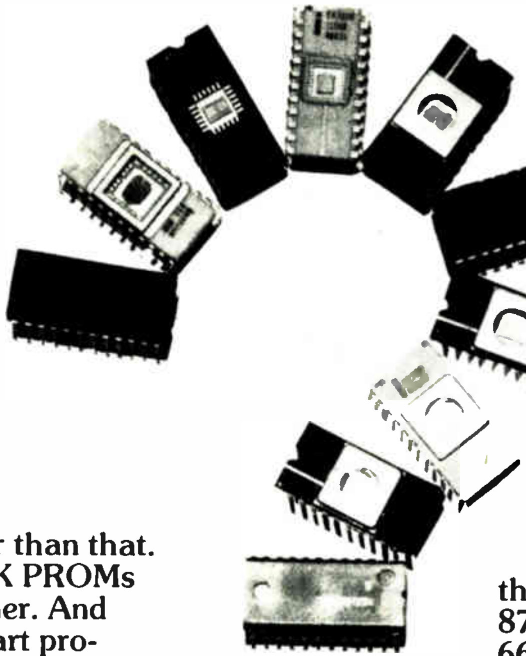
Low-noise isolation amplifier drives guards and shields

Intended for biomedical applications, the IA294 not only offers low input noise (typically 5 μV from 10 Hz to 1 kHz) but also provides drivers for active guards and shields, thus further ensuring low-noise performance in circuit.

For a balanced source impedance, common-mode rejection, input to

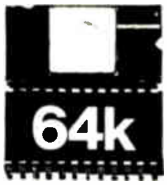
In 1979, you are going to ask the 64k question.

International Microsystems will have the answer.



It may come sooner than that. But the point is,that 64K PROMs are just around the corner. And when you're ready to start programming them, you'll want to know which programmer company can do the job.

International Microsystems will have the answer. We don't have it yet, of course. But we will. And long before your need arises. Because when you're ready for us, we'll be ready for you.



Today, we have modules for the most advanced PROMs—Intel 8748 and 8755, Intersil 6603 and 6604, Signetics 82S191, TI 2532 and the Harris 76161. And if you're anywhere in the U.S., we have a representative ready to serve you. So give them a call, and be sure to ask for your trial demonstration.

International Microsystems means state-of-the-art PROM programming. We don't have all the answers, yet. But that's because no one has all the questions.

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Even ten feet away, the new Series X-70 Solid State Piezo Audio Indicator demands attention with its strong, strident tone. Only 1.2" (31 mm) deep and 2.1" (53 mm) wide, the X-70 can be specified with PC pins or wire leads. Get all the details on the X-70, and our entire line of Audio Indicators. Write or call Projects Unlimited, Inc., 3680 Wyse Road, Dayton, Ohio 45414, Tel. (513) 890-1918, TWX 810-450-2523.

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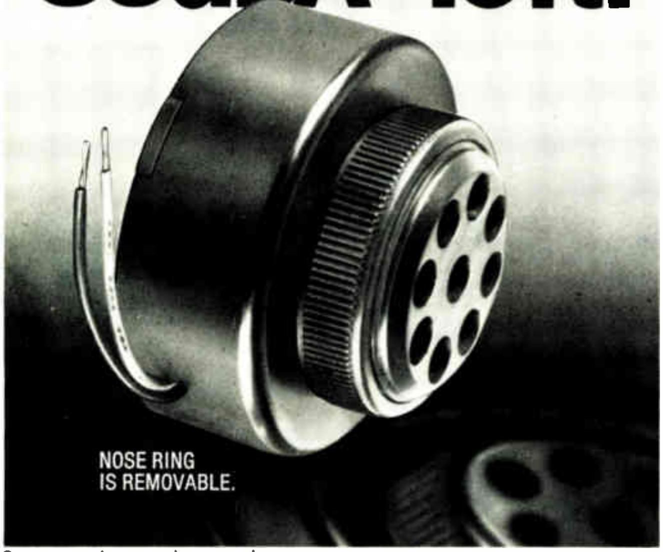

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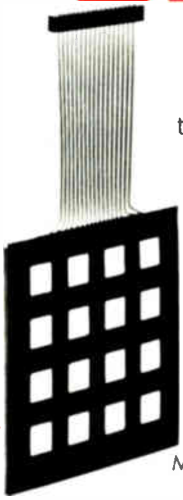

With scissors, modify this .030 thick, non-tactile panel into a 2-16 key, water and dust-resistant switching module. Prototype kit includes: design guidelines, complete instructions, a Sheldahl FLEXSWITCH®, flexcircuit connector, press-on nomenclature and RFQ check-sheet. Available in production quantities at reduced prices. Pressure sensitive back.

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output, is typically 126 dB; with a 5-kΩ source imbalance it is 120 dB, as is the CMR input to input. Isolation is 6,500 V peak for a 10-ms pulse and 5,000 V dc continuous.

The IA294 is priced at just $99 each and delivery is from stock to four weeks.

Intronics Inc., 57 Chapel St., Newton, Mass. 02158. Phone (617) 322-7350 [346]

Side-stackable LED matrix measures 1.16 in. high

Members of the LRT1057 series of 5-by-7-dot matrixes measure 1.16 in. from first dot to last. When these large, light-emitting-diode units are placed side by side, the horizontal spacing between dots is uniform, so characters can be made to "walk" across the face of the display.

The gray-faced units are available with red, yellow, green, or orange LEDs. Depending on color, the units range in price from $4.08 to $6.80 each in lots of 100 or more. Delivery is from stock.

Industrial Electronic Engineers (IEE) Inc., 7740 Lemona Ave., Van Nuys, Calif. 91405 [347]

Programmable wideband unit drives high-speed ECL

The PM-501M can drive a 50-Ω terminated cable at rates in excess 500 MHz with a minimum pulse width of 1 ns. Thus, the ultra-wideband programmable driver can be used in the testing of emitter-coupled-logic devices and other high-speed parts.

Rise and fall times are typically 500 ps with a 1-V output and propagation delay is 900 ps. Output offset is programmable continuously from +0.5 to −2.0 V, as is output amplitude from 0.5 to 1.5 V, peak to peak.

Specified for operation from 0° to 50°C, the PM-501M is priced at $250. Delivery is from stock to four weeks.

Tau-tron Inc., 11 Esquire Rd., North Billerica, Mass. 01862. Phone (617) 667-3874 [348]

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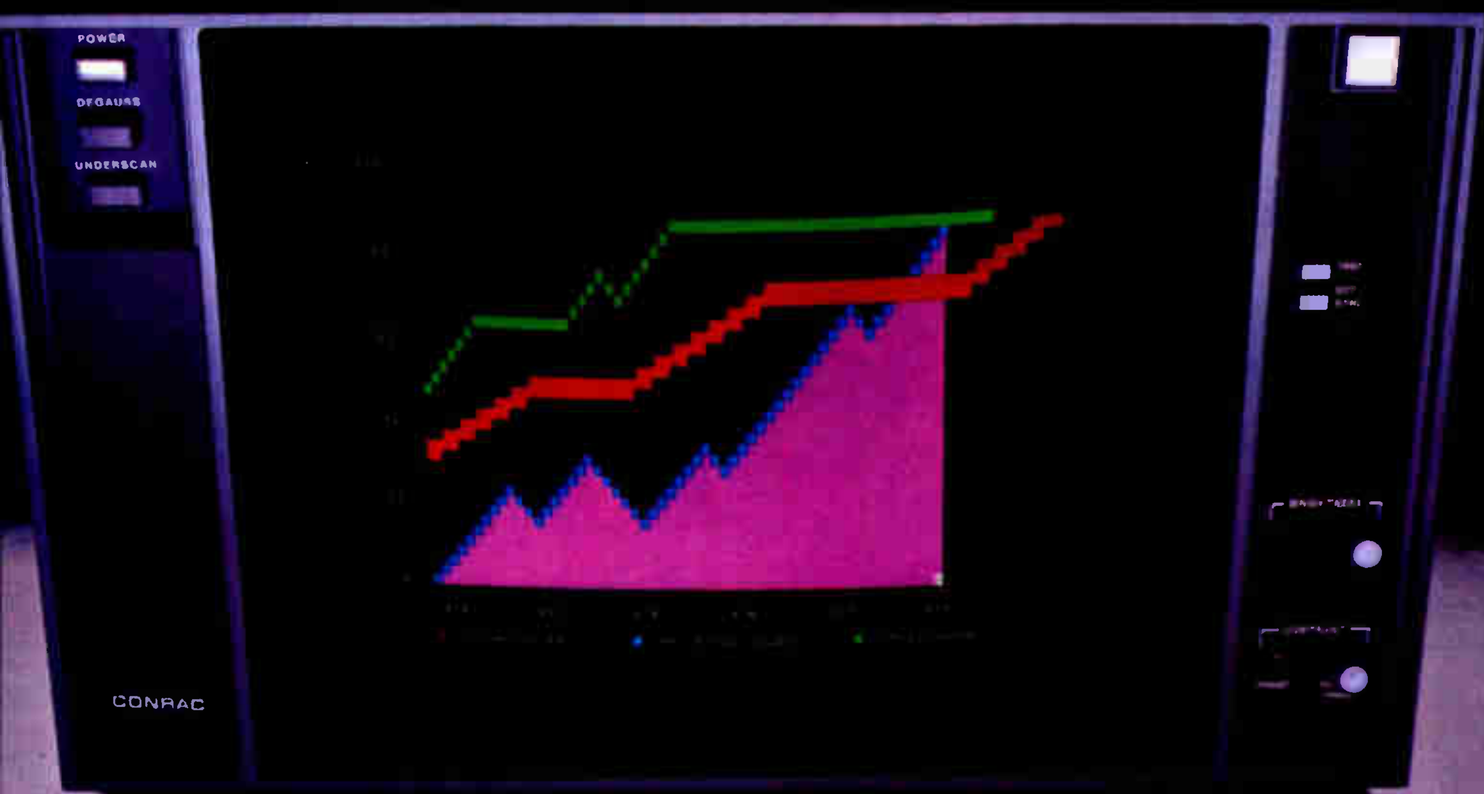

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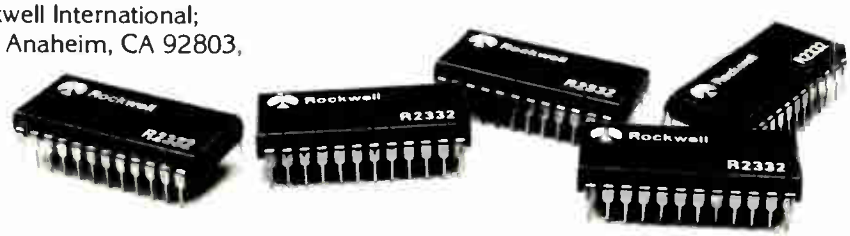

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D-a unit converts 12 bits in 50 ns

Datel Systems Inc., Mansfield, Mass., has unveiled the fastest 12-bit digital-to-analog converter on the market today. **The current-output device will settle to within 1 least significant bit in 50 ns.** Part of Datel's DAC-HF series, the converter is packaged in a 24-pin dual in-line package. It consumes 780 mW and will sell for between $139 and $219, depending on temperature range.

Chip includes 4½-digit counter, decoder, and driver

Intersil Inc., Cupertino, Calif., has the distinction of being the first company to integrate a 4½-digit counter, a decoder, and a display driver on a single silicon chip. Two versions of the device are being offered: **the 7224 for liquid-crystal displays and the 7225 for light-emitting-diode displays.** Both complementary-metal-oxide-semiconductor devices can handle input rates of 15 MHz and require only a single 5-V dc supply. In hundreds, the LCD version, which contains an oscillator for generating the backplane signal, sells for $7, whereas the LED version is priced at $5.30. The units are available now.

3-μs a-d converter expected from Analog Devices

Look for Analog Devices Inc.'s Semiconductor division, Wilmington, Mass., to come up with a 12-bit analog-to-digital converter with a conversion time of 3 μs. The part, which should be out within the next three months, will be housed in the company's unique slam pack package and **will sell for a low $100 each in large quantities.**

Interface chip gets more flexible

Signetics Corp., Sunnyvale, Calif., is upgrading its popular 2651 programmable communications interface chip with an "extended" version that fits the same sockets but offers more flexibility in the selection of transmission rates. **The new chip will be offered in three versions, each of which has a choice of 16 selectable rates up to a maximum of 38.4 kilobits per second.** Available now in sample quantities, the new chips will sell for $13.05 in plastic and $15.05 each in ceramic for quantities of 100 or more.

Two companies cut prices for DEC-compatible gear

To strengthen its position in the market for computer peripherals compatible with Digital Equipment Corp. computers, Xebec Systems Inc., Santa Clara, Calif., **is dropping prices for its cartridge disk controller from $2,800 to $1,975.** At this price the Xebec quad will be more competitive with the bottom of the growing DEC-compatible market, according to Bob Sigal, marketing manager.

Another company lowering prices on equipment made to work with computers from DEC is Data Translation Inc., Natick, Mass. **The company is making price cuts on its line of dual-height boards for the LSI-11/2.** Affected are the DT2762 high-level data-acquisition system, which is being reduced from $695 to $545; the optional programmable-gain amplifier for the system, which has been cut from $175 to $100; the DT2764 low-level data-acquisition system, whose price is being slashed from $795 to $545; the DT2766 four-channel, 12-bit analog-input board, which has been cut from $695 to $545; and the DT2767 four-channel, 8-bit analog-input board, whose price has dropped from $495 to $445.

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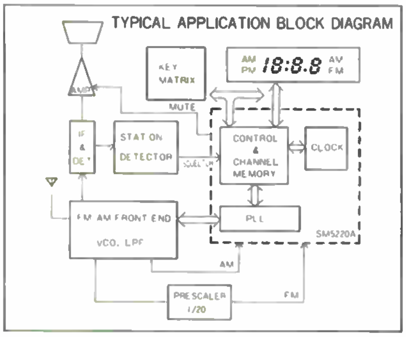

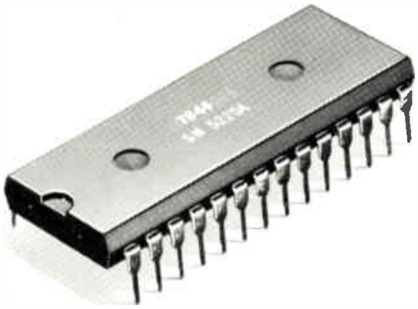

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and board ejectors. Dimensional drawings and ordering information are provided on all products. Richco Plastics Co., 5825 North Tripp Ave., Chicago, Ill. 60646. Circle reader service number 421.

Power supplies. Detailed information on power supplies capable of providing 60 amperes at 1 to 200 volts is contained in a 52-page catalog. Comprehensive lines of miniaturized (in both printed-circuit-board and chassis-mounting versions), plug-in, premium-performance, general-purpose, narrow-profile, laboratory benchtop, and unregulated power supplies are included. Many models have dual and triple outputs. Acopian Corp., Easton, Pa. 18042 [422]

Rf and i-f signal-processing hybrids. High-reliability hybrid circuits for radio- and intermediate-frequency signal-processing applications are illustrated and described in an eight-page brochure. It gives application information and specifications for a wide variety of hybrids, among them two- and three-way power dividers, double-balanced mixers, rf switches, phase modulators, 180° and quadrature hybrids, bidirectional couplers, and amplifiers. Composite hybrids

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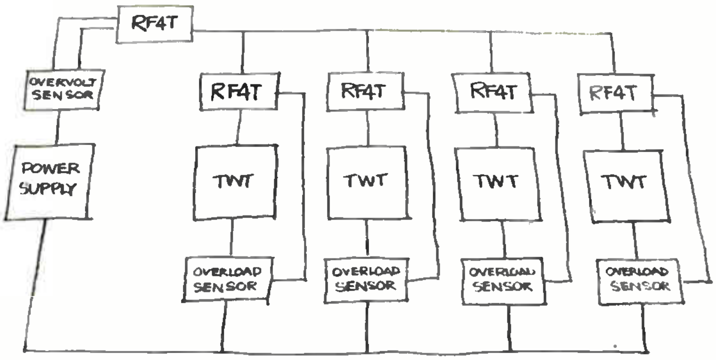

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that incorporate two or more functions on a single substrate are described in a separate section. Raytheon Co., Industrial Components Operation, 465 Centre St., Quincy, Mass. 02169 [423]

Accelerometers. Written for the user and designer of systems that measure shock, vibration, and acceleration, Technical Information Bulletin No. 781 gives a detailed description of the construction, performance, and advantages of eight types of accelerometers. The eight-page bulletin includes information on strain-gage and servo-type accelerometers,

along with schematics and block diagrams that will clarify how they operate and where they can be most effectively applied. Self-induced cable noise due to shock and vibration is explained and methods of determining various types of measurement-system deficiencies are discussed. Gulton S-C Division, 1644 Whittier Ave., Costa Mesa, Calif. 92627 [424]

Data-conversion design. The 80-page "Data Conversion Design Manual" covers the 8700 series analog-to-digital and the 9400 voltage-to-frequency and frequency-to-voltage converters, made using complementary-metal-oxide-semiconductor technology. It is available from Teledyne Semiconductor, 1300 Terra Bella Ave., Mountain View, Calif. 94043 [425]

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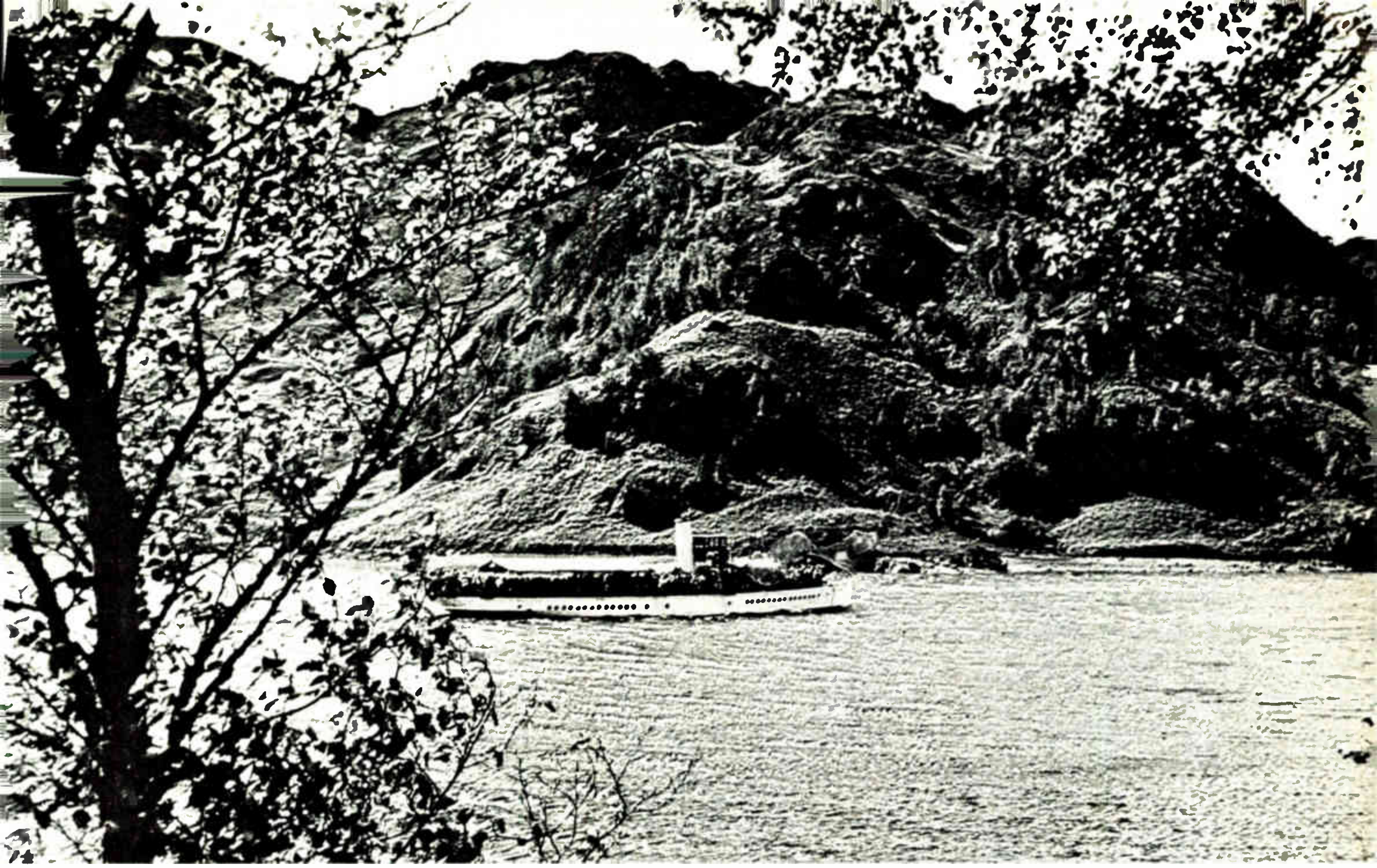

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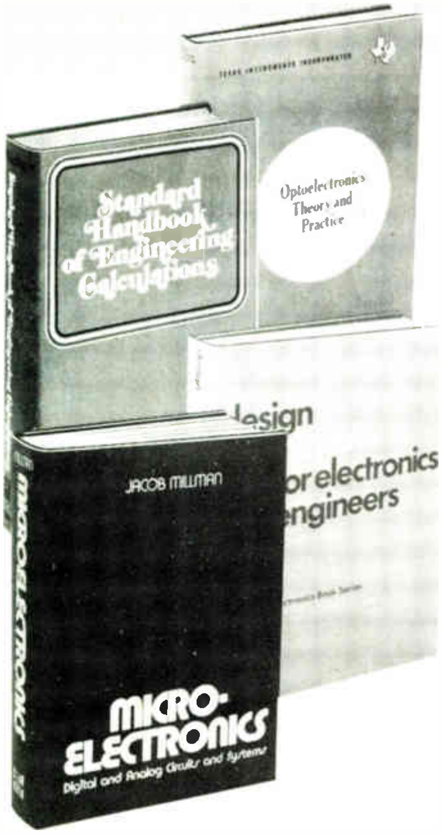

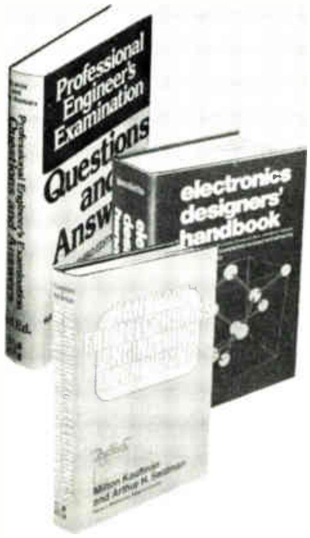

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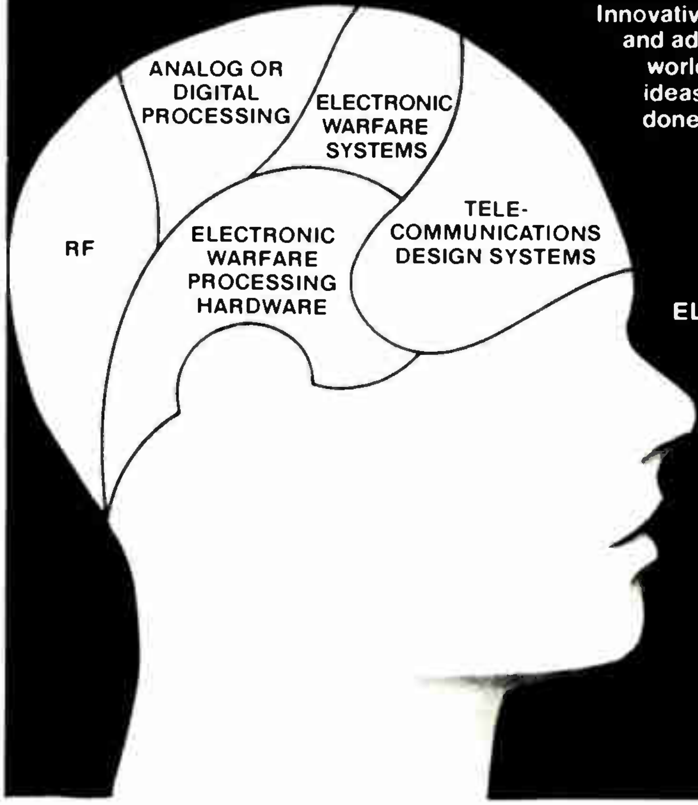

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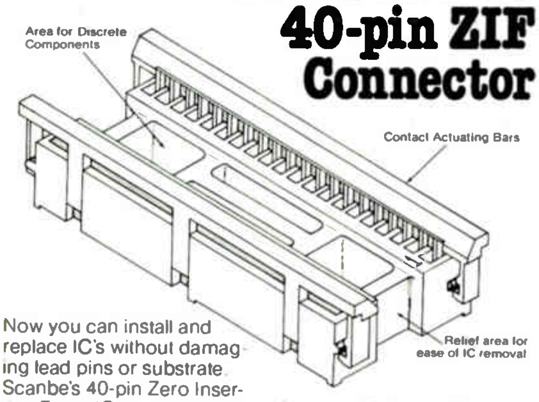

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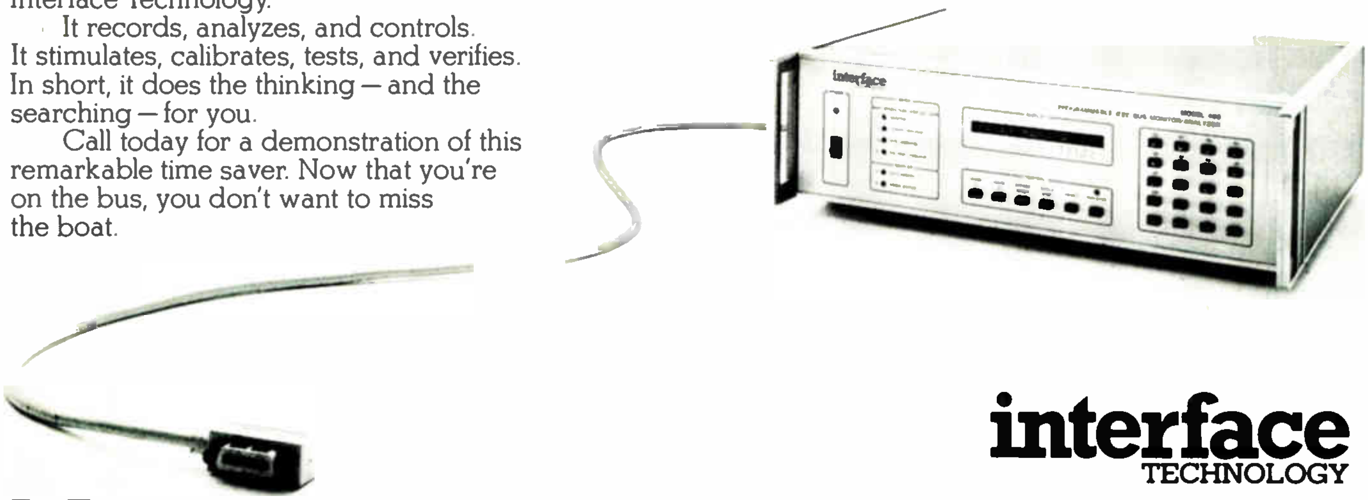

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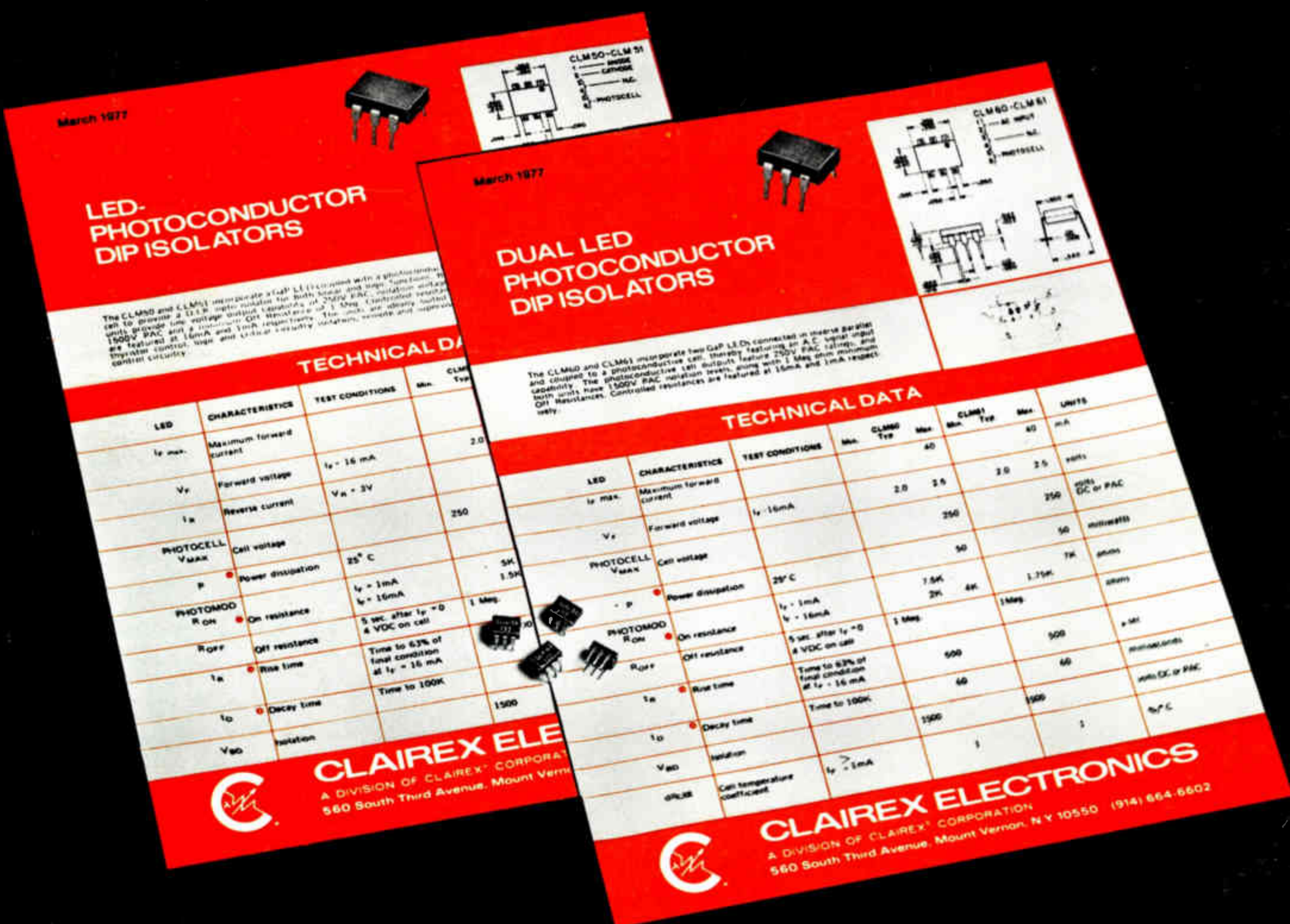

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