JANUARY 18, 1979

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Electronics
The International Magazine of Electronics Technology
Vol. 52, No. 2 • January 18, 1979

Highlights

Cover: Off to language school, 105
High-level languages are growing in importance for microcomputer systems as programs become longer and more complex, says this special report. It is the first article in a series on using adaptations of these languages to program microcomputers.

Cover is by Art Director Fred Sklenar.

Software protection gets thornier, 88
After more than a decade, the problem of protecting software is becoming even harder. One complicating factor is the increased use of "soft architecture"—hardware-software mixes that employ much microcode. A spate of lawsuits is likely to be another.

How to ease microcomputer-board testing, 113
Testing microcomputer-based systems can be made much simpler by using the microcomputer's self-test capabilities, adopting new diagnostic algorithms, and designing the system for testability.

Interfacing video-game processors with TVs, 124
Large-scale integration is eliminating the nightmare of designing an interface for a video game or personal computer's microprocessor with a home TV set. A single video-display generator can supply all the brightness and color information necessary, replacing hundreds of small- to medium-scale integrated circuits.

And in the next issue . . .
A family of ECL bit-slice parts . . . optimizing high-level languages for microprocessor-based system development: part 2 of a series . . . a small computer that uses C-MOS-on-sapphire.

Electronics

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Publisher's letter

That programming microcomputers has become a No. 1 engineering task is by now well known. And the situation is getting tougher as the more complex systems built around 16-bit microprocessors emerge.

But high-level languages have come to the engineer's rescue, although there are also disadvantages in using them. To sort out the many complexities of this important subject, we have begun a series of articles. It starts with this issue's cover story (p. 105), in which microsystems and software editor John Posa has prepared an overview of these languages.

The main advantage of a high-level language over assembly language is that it makes better use of the programmer's time, John remarks. On the other hand, the various types of high-level languages are slow-running and use up a lot of memory.

Another point he makes is that there is a bewildering variety of high-level languages available today. In addition, many users are torn between the need to use a new language like Pascal and the desire to preserve their libraries coded in older Basic and Fortran.

"In some respects the microcomputer programming situation today is like that of the mainframes some 15 years ago—there's a language problem," John observes. "If everyone agreed on, say, one version of Pascal, it would be fine. But it's impossible to throw out the past and no one is sure yet which version of Pascal will work for the future. That's why Pascal standardization is such a charged issue."

Nevertheless, structured programming like that possible with Pascal seems to be the way to go because it is easy to use.

Future parts of this series will concentrate on the high-level languages discussed in the overview. The next installment will cover optimizing high-level languages with assembly code to tighten up a program for critical time or space requirements.

A good example of how on-the-job training works is William Meronek, senior circuit design engineer for Western Digital Corp., who designed the SD1933 communications controller chip described on page 137. Originally an expert in logic design, 27-year-old Meronek was hired by the Newport Beach, Calif., firm with no direct experience in the idiosyncracies of large-scale integration. And though he knew what had to be done from a circuit standpoint, he had to pick up a lot of know-how to make a cost-effective product.

"My boss had to spend a fair amount of time with me," Bill recalls. "First I had to learn how to read all those drawings. Then I had to learn about processing, FETs, bipolar integrated circuits, and device physics—a lot of material I did not study at school."

He learned well enough to design the SD1933, which is capable of handling any of the new, bit-oriented data-communications protocols.

January 18, 1979 Volume 52, Number 2 99,099 copies of this issue printed

Published every other Thursday by McGraw-Hill, Inc Founder: James H. McGraw 1860-1948. Publication office 1221 Avenue of the Americas, N.Y., N.Y 10020; second class postage paid at New York, N.Y. and additional mailing offices. ID# 172400.

Executive, editorial, circulation and advertising addresses. Electronics, McGraw-Hill Building, 1221 Avenue of the Americas, New York, N.Y. 10020. Telephone (212) 997-1221. Teletype 12-7960 TWX 710-581-4879. Cable address: M C G R A W H I L L N E W Y O R K.

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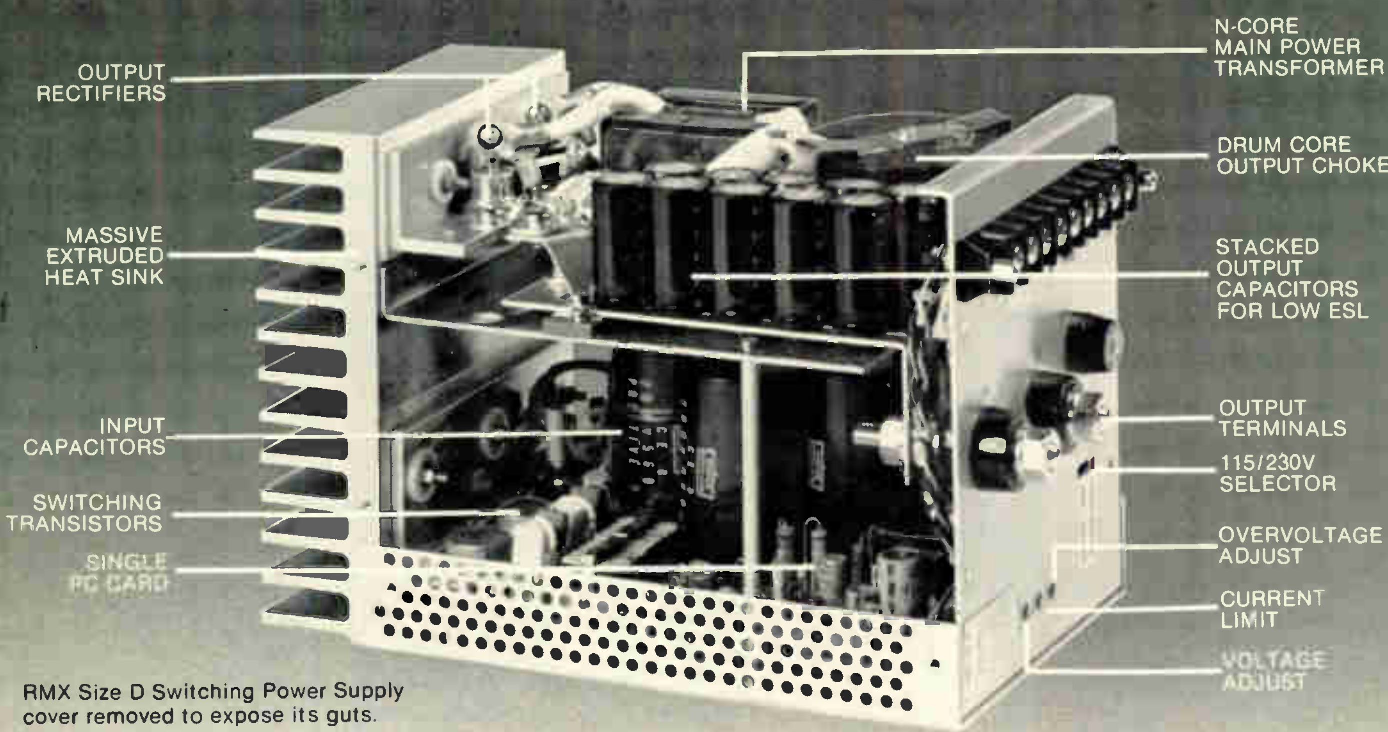

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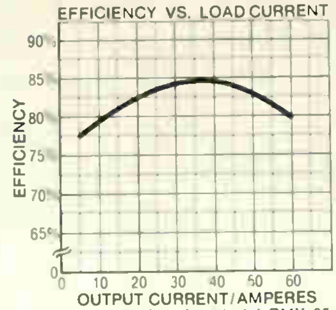

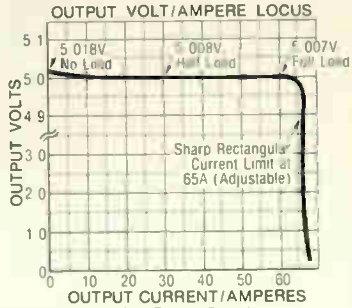

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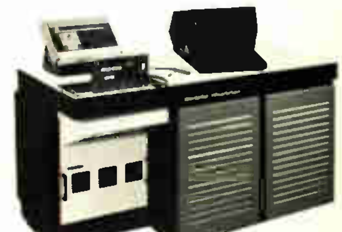

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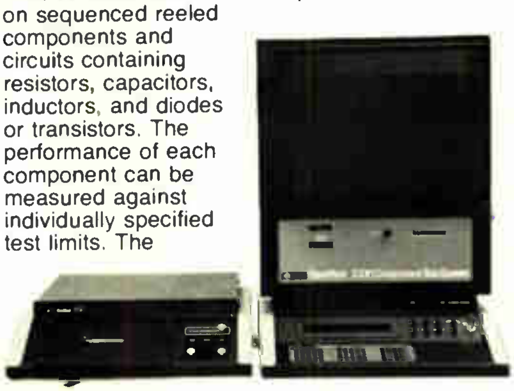

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GenRad

News update

■ Neutrinos—those elusive, high-energy, zero-mass particles, which have been in the private domain of the particle physicist—are generating a lot of action and controversy for the communications specialist. They have been proposed for such uses as television carriers, interplanetary communications, and straight-through-the-earth links with submerged submarines, because no known material stops or even attenuates them [*Electronics*, Aug. 17, 1978, p. 73].

However, the question of their practicality in terms of real-system cost, modulation capabilities and the like, are matters of dispute. The latest round started when an outspoken proponent of neutrino communications, Peter Kotzer of Western Washington University in Bellingham, Wash., took his neutrino detection gear to the Fermi National Accelerator Laboratory in Batavia, Ill., and detected neutrinos 5 kilometers from their high-energy beam.

Kotzer's work won front page coverage in the New York Times, thus widening a rift between those members of the high-energy-physics community who support his theories (or at least believe they should be tried out) and those who believe his proposals to be totally impractical.

The test was done without Fermi's blessing and was conducted off the lab's property. But Kotzer says it was successful, and he "intends to go on with my work with or without the support of the Fermi lab" because it is important for his long-range goals in studying neutrino communications. The lab, for its part, considers his work not important enough for it to expend funds on.

The lab may not be able to stop Kotzer's work, since he is off its property and its neutrinos are just flying around freely. However, its new director, Joshua Lederman, says "accelerator-generated neutrinos have been used to communicate with detectors since 1960 over ever-increasing distances filled with steel or earth. . . . The results reported in the New York Times teach us nothing." **Harvey Hindin**

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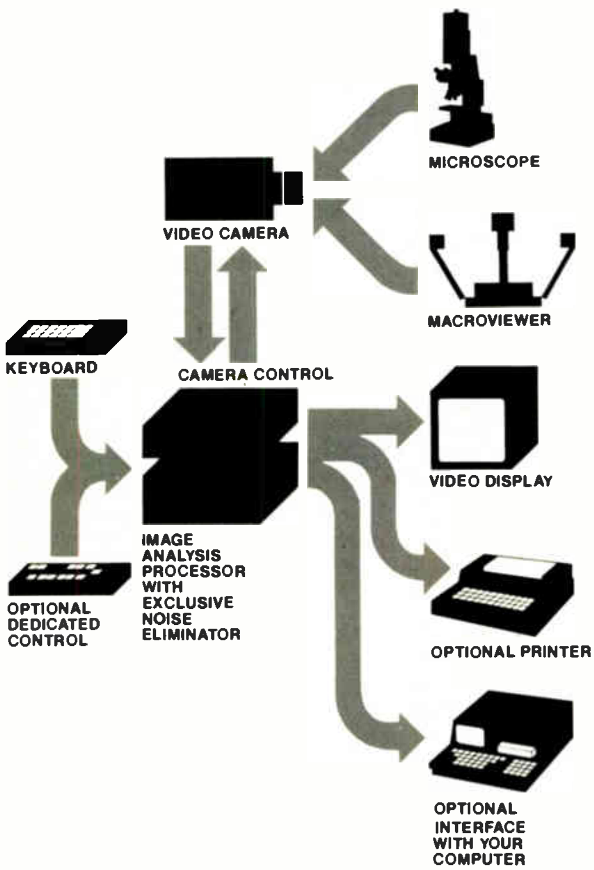

Processed video image without calibrations. The field is not uniform. The image center has considerable noise, while objects at the corners are lost.

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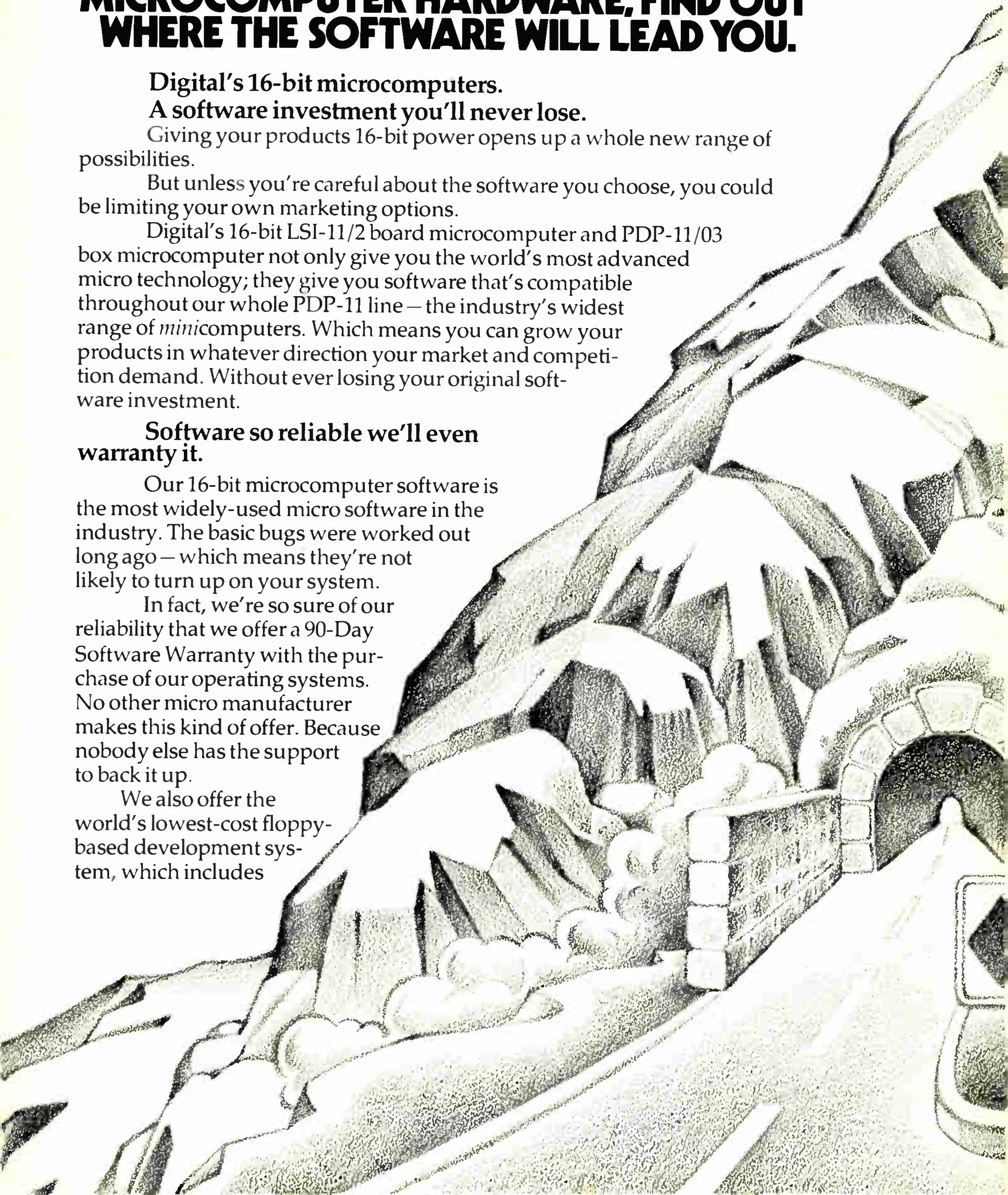

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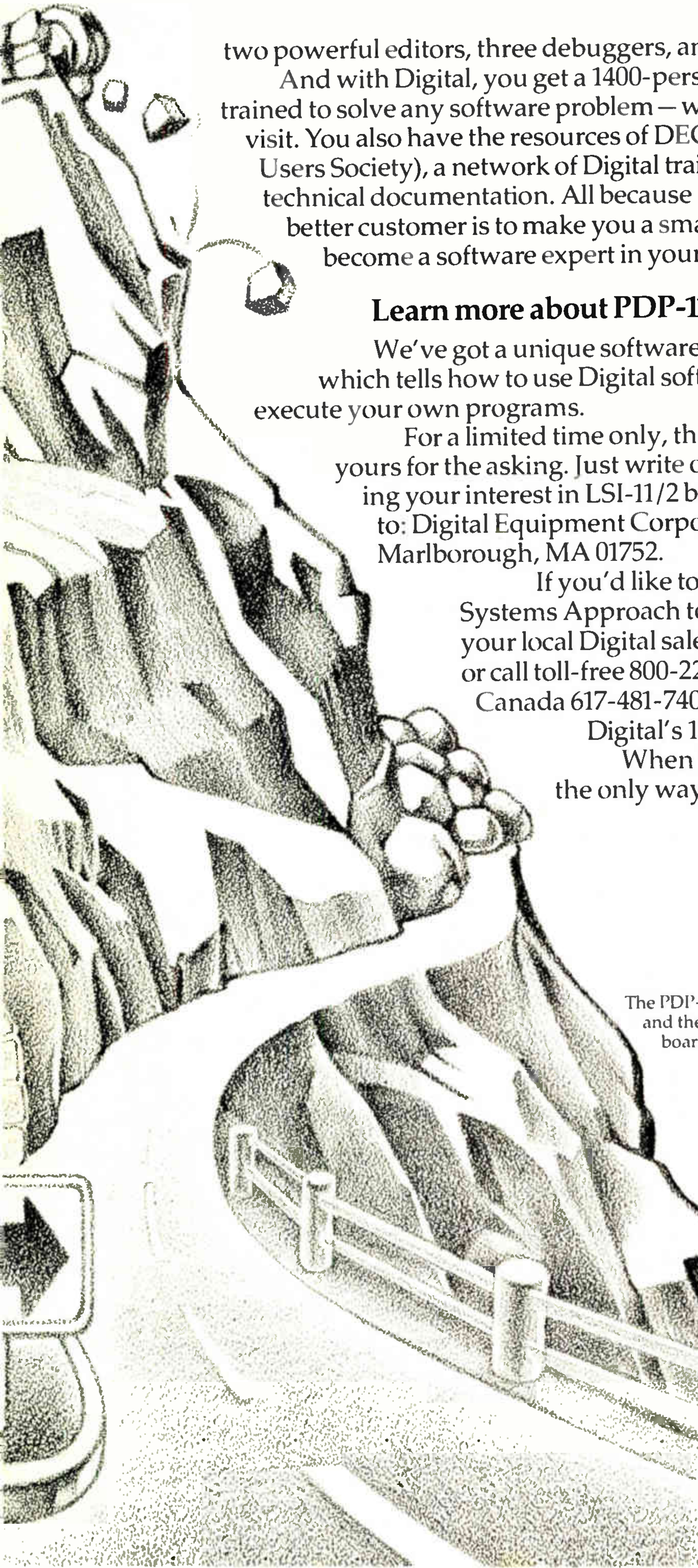

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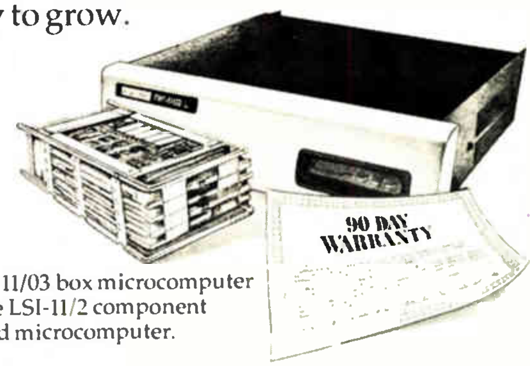

The PDP-11/03 box microcomputer and the LSI-11/2 component board microcomputer.

digital

Circle 13 on reader service card

People

West and Nichols count on servicing microprocessors

Though the market is still small, David G. West and A. J. Nichols believe the need for instruments designed exclusively for troubleshooting microprocessor-based products will grow rapidly in the 1980s. They believe it enough to have recently gone to work for Millennium Systems Inc., Cupertino, Calif., the only company now making the service instruments. West is director of marketing; Nichols is vice president of engineering.

Prospects. "From nothing in 1977 to between $3 and $4 million in 1978, the market for this kind of instrument is definitely not a sleeper," says West, 32 years old and with a Ph.D. in electrical engineering from Stanford University. He should know: he has just spent about a year and a half managing efforts in microprocessor development systems and microcomputer systems and board products at Zilog Inc.

"Right now, most engineers are grappling with designing microprocessors into their new systems. The aftershock of keeping the systems working hasn't hit them yet, but it will," he says.

Four-year-old Millennium hit the jackpot last year when it won a contract to build a microprocessor development system of its own design exclusively for Tektronix Inc., the giant instrument maker. Now it is the only company making the new service instruments, because Intel Corp. stopped producing its Microscope 820 in December.

Millennium is in a good position to pick up Intel's customers. Indeed, next month, it is introducing a 5-megahertz emulator for the Intel 8085 microprocessor that works with its troubleshooting Micro System Analyzer.

"Intel simply could not wait," says "Nick" Nichols, 43, also holder of a Stanford Ph.D. in electrical engineering. Like West, he should know whereof he speaks: he was manager of Intel's instruments and test systems engineering before joining

Upturn. Millenium's A. J. Nichols, left, and David G. West, expect sales of instruments for servicing microprocessors to rise.

Millennium. His group was disbanded when Intel dropped the 820, and, he says, "I could have stayed, but I believe in this market."

West predicts the market will total between $6 million and $7 million in 1979—too small for a giant like Intel, Nichols points out. But for Millennium, those numbers have appeal. Both men expect that by 1982 as much as 75% of electronic products in development will be built around microprocessors; today that figure is only 25%.

Yockey ready to roll at Rockwell Electronics

The rationale for the changes that in two years have swept away most of its top executives and largely restructured Rockwell International Corp.'s Electronics Operations might not be apparent to outside observers, its new president concedes. But management was too busy making the changes work to do much explaining, says Donald R. Yockey, named last month to head the $1.3 billion operation.

The new organization pulls together similar product lines from formerly independent divisions. In the process, such familiar industry names as Autonetics and Collins were downgraded in favor of the Rockwell name.

Previously president of one of its major groups, Electronic Systems, the 57-year-old Yockey played a key

People

Chief. Donald Yockey is spearheading Rockwell's realigned Electronics Operations.

role in helping plan and carry out the changes for his predecessor, Donald R. Beall, now Rockwell International president and chief operating officer. Yockey is now ready to roll.

"Things are about where they should be in products, organization, and people," he observes. Especially promising, he feels, is the Rockwell Commercial Telecommunications group, based in Dallas, as is he. Essentially the former Collins Radio Co., acquired in 1972–73, it holds a strong position in computer-based switching communications.

Electronics Operations includes two other groups, Rockwell Electronic Systems and Rockwell Avionics and Missiles, and a division, Rockwell Electronic Devices.

Sharing. The Collins side of the Rockwell business had such a good record that spreading its people and expertise throughout Electronics Operations was a paramount objective of the reorganization, says Yockey. "In particular, we wanted to use successful commercial telecommunications products from Collins to strengthen the Rockwell Government-business side."

Accordingly, two former Collins divisions selling to Government and military customers are now part of the Electronics Systems group, based in Anaheim, Calif., which is itself largely made up of the old Autonetics division.

Yockey also is high on his Electronic Devices division, which has emerged as a prime manufacturer of n-channel integrated circuits. Also, he shares the Rockwell enthusiasm for the bubble memory's future.

The fireworks have just begun!

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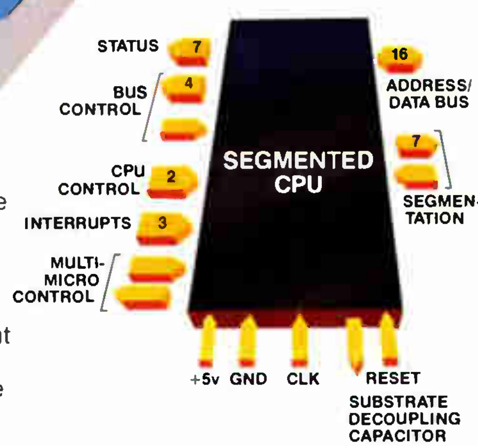

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Prefer to use it as a fully expandable microprocessor? In that role the Z8 can address up to 62KB of external program memory and 62KB of data memory. Plus, an almost unlimited amount of I/O is available to you by using a memory-mapped technique.

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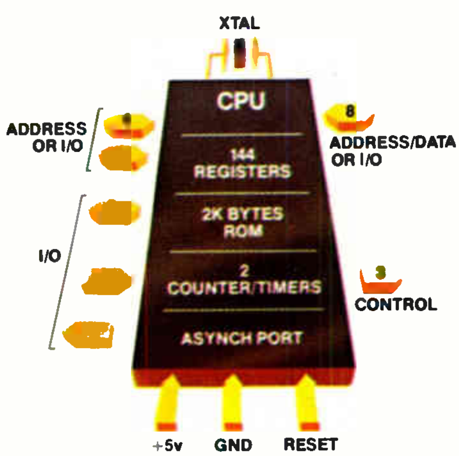
You'll be delighted with the Z8 instruction set. It contains the same type of power as found in advanced microprocessors such as Zilog's Z80 and Z8000. As a result, the Z8 can manipulate bits, bytes and words (16-bit) with ease. Combined with 9 powerful addressing modes, it can provide your programmers with a problem-solving tool of near-unlimited flexibility.

IMAGINE

A SINGLE CHIP MICROCOMPUTER THAT EXPANDS WITH YOUR NEEDS–ZILOG'S Z8.

Explosive Performance.

The Zilog Z8 makes no compromises with speed. It is specified to operate off its own internal clock generator circuit at 4MHz. That's the same



speed as the famous Zilog Z80A! Instruction execution times typically range from 1.5 to 2.5 microseconds —fast enough for even your toughest application requirements!

Imagine how your products can sparkle with new ideas.

With the Z8 problem-solving instruction set, high-speed, and almost limitless expandability your products could easily become incredible not just excellent.

To help develop and debug these exciting ideas, Zilog has a complete set of tools for you. The software development package contains a Z8 Assembler and Simulator that runs on Zilogs' Z80-based MCZ or ZDS Systems.

In addition there's also a special 64 Pin version of the Z8 that uses external PROM for hardware simulation to permit thorough debugging and testing prior to committing to mask-programmed ROM 40 pin Z8's.

Additional development tools soon to come include a prototyping board and a sophisticated systems analyzer.

Zilog introduces the next generation with a bang!

The revolution in microprocessor technology that began with the Z80 and its supporting family of products, blazes on. Now its a soaring jump in architectural sophistication to the unprecedented Z8 and the incredibly powerful Z8000. And, there's a whole family of support products to come. It's what you expected from Zilog, the company that's pledged to stay "a generation ahead."

Get your own fireworks going today.

Join the excitement. Place your order today with your nearest Zilog distributor.

In the meanwhile, give your development staff a headstart by ordering the Z8 product manual set; order directly from Zilog in the U.S. Elsewhere contact your Zilog distributor.

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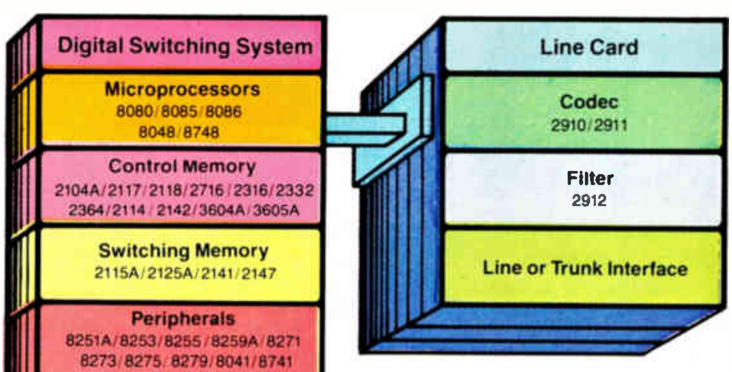
The fireworks have just begun!

How Intel's codec cut PCM

The switchover to an all digital telephone network just took a great leap forward. Introducing Intel's 2912 transmit/receive filter. It's the first and only one-chip LSI filter. And it's the only filter with a companion one-chip codec, our 2910 (μ Law) and 2911 (A Law).

Since we introduced the 2910/2911, line card designers have had the capability to code and decode digital signals with a single, reliable component. Now our 2912 goes a step further. Like our codec, the 2912 replaces multiple devices with a monolithic solution. And it meets the stringent digital Class 5 Central Office requirements for both D3/D4 and CCITT Transmission Standards, with necessary voiceband flatness and stop band rejection. The 2912 also has a 50-60 Hz notch to filter AC line noise, and permits gain adjustments of voice signals.

We designed our codec and filter to work together. And neither one requires precision external components. The 2912 provides a direct interface to line or trunk circuits that use either transformers or electronic hybrids.



Meeting in the middle of the digital highway

For the first time, line card design can dramatically reduce PCM switching costs in most TDM systems. That's because our codec has a built-in microcomputer interface that allows switching directly on the PCM highway, eliminating or greatly reducing the size of the time-slot interchange memory and allowing greater flexibility in the level of blocking selected for the system.

So when line card designers select Intel's filter and codec, the systems savings and design simplicity extend beyond the entrance to the digital highway. System

new filter and system costs.

engineers benefit, too, with important economies in hardware and common control overhead.

How Intel gives you a head start in digital technology

We've long been a supplier to the telecommunications industry, at the forefront of each new step in the evolving digital network. Today we supply microprocessors, memory components and peripheral support circuits, as well as our codec and filter.

All our telecommunications products use the same NMOS process we use to manufacture tens of millions of semiconductor components each year. And every Intel telecommunications product undergoes extensive testing before it's shipped.

Best of all, the 2912 filter, as well as our codec, is in volume production and available for delivery now. To order, or to obtain additional information, contact: Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051, or telephone (408) 987-6475.

Europe: Intel International, Rue du Moulin a Papier, 51 Boite 1, B-1160, Brussels, Belgium. Tel: (32-2) 660 30 10

intel® delivers.

Circle No. 23 for information

The trial in the marketplace

Software is devouring more and more development dollars at the same time that computers are becoming less and less dissimilar in their physical characteristics. Some manufacturers estimate that programing accounts for 75% to 80% of their development cost, and they hint that they would not be surprised to see that figure reach 90% before too long. It is against this background that a pair of lawsuits filed by semiconductor makers against producers of minicomputers is drawing a great deal of attention and causing not a little bit of worry in both camps.

The suits were filed by Fairchild Camera and Instrument Corp., the semiconductor house, against Data General Corp. and by National Semiconductor Corp. against Digital Equipment Corp. Fairchild claims that Data General's software licenses violate the antitrust laws, and National maintains that four of DEC's PDP-11 patents are invalid. The two suits have this in common: they are designed to free software developed by the computer makers, so that the semiconductor houses can use the programs in the machines they have built.

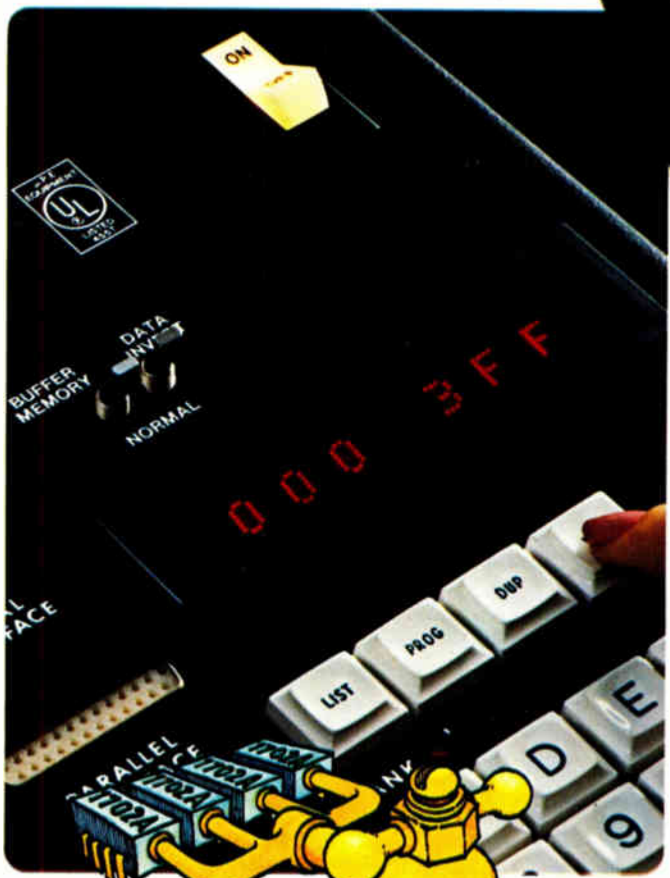
The question is a highly complex one that could spend the next few years grinding its way through the courts. The semiconductor people make the point that their rivals have wrongly sought to head off competition by surrounding software with a protective thicket of legalities and "threats" to customers. The computer makers, on the other hand, maintain that they have put many years and many dollars into development of their programs and that the courts should protect them and their investment from what they see as a predatory attempt by others to enjoy a free ride. Complicating the whole matter is the fact that the manufacture of hardware that emulates another company's computer is becoming an increasingly popular method of diversifying into other markets.

Meanwhile, in the real world, users must continue to function no matter how long the legal disputes drag on. That's why, for the time being, at least, the most important trial is going to take place in the marketplace with the customer as judge and jury. Only the difference here is that the issue will be cost/performance, with the user selecting the machine that runs longest between breakdowns, does the fastest job, demands the least power, and carries the most attractive price tag. In short, disputes involving technology may in fact be settled first in the market place, and not in the courts.

The courts should be keenly aware of that winnowing-out process, one that could mean the death of companies even as the litigation proceeds with all deliberate speed. A little judicious haste would be welcome here, in order to avoid the irony of a company expiring before legal help arrives in the form of a favorable ruling.

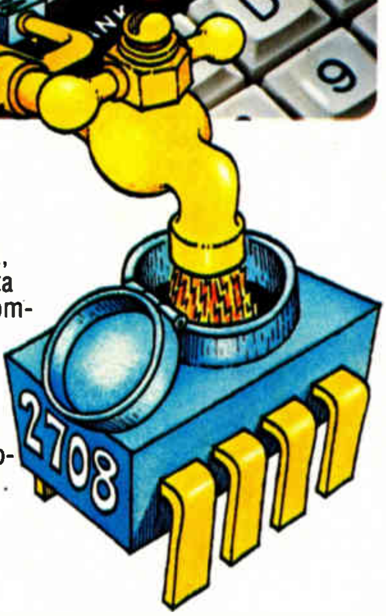
Ooops-free PROM programming with the CMOS buffered programmer.

Avoid lost or altered data, misprogrammed PROMs, ruined master PROMs with the M900B, the only programmer with built-in CMOS buffer.
Our new M900B has a buffer of 2048 8-bit words with capacity to 4096 words. It's CMOS with power-backup so you can shut off or lose AC power for up to 60 seconds and not lose data. That's plenty of time to replace one PROM personality module with another. Thus you can transfer data from one PROM type to an entirely different PROM type (UV eraseable to bipolar, for instance) or transfer from several small PROMs to a single large one. A Data-Shift feature lets you change data locations when transferring data between PROM and memory.



Helps prevent misprogramming.
The M900B lets you check, correct and verify your data in the buffer before you commit it to a PROM.

CMOS technology with power-backup guards against transients that can alter data stored in a cheaper but volatile bipolar RAM.



Use it with or without the buffer. Two-socket personality modules guard your master PROMs.
With the buffer switched out, the M900B gives you direct PROM to PROM copying. We use two sockets, one for the master PROM, one for the copy PROM. Operator error can't alter a PROM in our master socket because that socket contains no programming voltages.

The M900B, like all our control units and PROM personality modules, comes U.L. listed, designed and built to U.L. electrical safety standards.

The M900B with standard 2K buffer costs only $2,100. With full 4K buffer, it costs only $2,400.

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Meetings

Communication Networks Conference and Exposition, The Conference Co. (Newton, Mass.), Sheraton Park Hotel, Washington, D. C., Jan. 30–Feb. 1.

Second Annual Defense Market Forecast Conference, American Institute of Aeronautics and Astronautics (Los Angeles section), Hyatt-L. A. International Hotel, Los Angeles, Feb. 5–6.

Microelectronics Measurement Technology Seminar and Exhibit, Benwill Publishing Corp. (Boston), Hyatt House, San Jose, Calif., Feb. 6–7.

Wincon—Aerospace and Electronic Systems Winter Conference, IEEE, Sheraton Universal Hotel, Los Angeles, Feb. 6–8.

Phase-Locked Loops Seminar, George Washington University, Washington, D. C., Feb. 12–13.

International Solid-State Circuits Conference, IEEE, Sheraton Hotel, Philadelphia, Feb. 14–16.

1979 SAE Congress and Exposition, Society of Automotive Engineers (Warrendale, Pa.), Cobo Hall, Detroit, Feb. 25–March 2.

Sixth Energy Technology Conference and Exposition, Electric Power Research Institute (Palo Alto, Calif.), Sheraton Park Hotel, Washington, D. C., Feb. 26–28.

Recent Advances in High-Frequency Communications, Institute of Electrical Engineers (London), Savoy Place, London, Feb. 26–28.

Compcon Spring '79—18th IEEE Computer Society International Conference, IEEE, Jack Tar Hotel, San Francisco, Feb. 26–March 1.

Digital Microwave Transmission Seminar, IEEE and Princeton University, at Princeton University, Princeton, N. J., Feb. 27.

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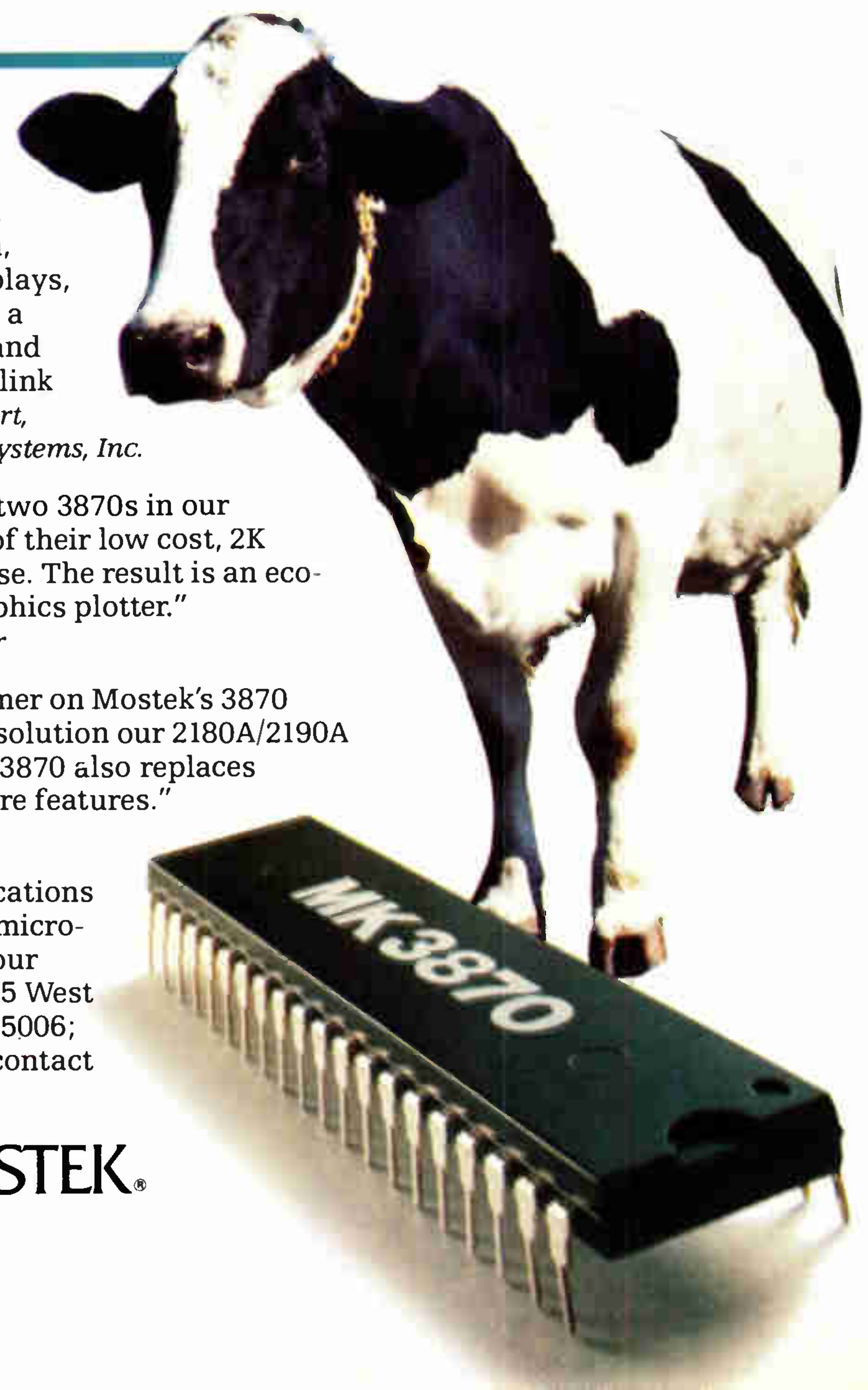
Because it takes 32 I/O lines to keep her contented.



"Dairy management is becoming more and more scientific. In our automated milking system, Mostek's 3870 controls three displays, numerous solenoids, a keyboard, a switchbank, valves and motors, and also provides a communications link to a larger computer." *Mike Wingert, Vice-President Engineering, Dairy Systems, Inc.*

Hewlett-Packard: "We use two 3870s in our 7225A Graphics Plotter because of their low cost, 2K ROM memory and interfacing ease. The result is an economical and highly versatile graphics plotter." *John Fenoglio, R&D Project Manager*

John Fluke: "The unique timer on Mostek's 3870 provides the one microsecond resolution our 2180A/2190A Digital Thermometer needs. The 3870 also replaces all digital IC's while allowing more features." *John Lund, Senior Design Engineer*

There are hundreds of applications using Mostek's 3870 single-chip microcomputer. Get information for your design by contacting Mostek, 1215 West Crosby Road, Carrollton, Texas 75006; phone 214/242-0444. In Europe, contact Mostek Brussels; phone (32)02/660.25.68.

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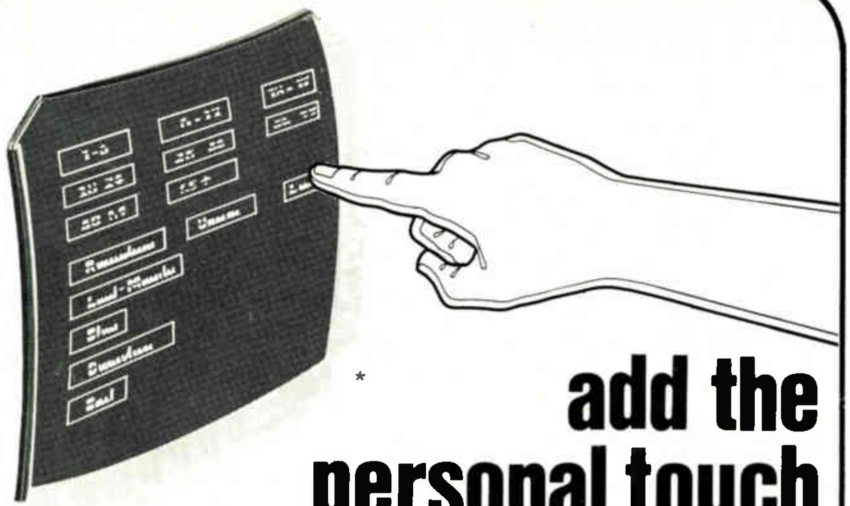

Meetings

Voice and Video Seminar, George Washington University, Washington, D. C., Feb. 27–March 1.

Nepcon West '79, Industrial and Scientific Conference Management Inc. (Chicago), Anaheim Convention Center, Anaheim, Calif., Feb. 27–March 1.

ICE '79—International Computer Exposition, Marcom International Inc. (Tokyo) and Golden Gate Enterprises Inc. (Sunnyvale, Calif.), Tokyo Harumi Fairgrounds, Tokyo, Feb. 28–March 2.

Optical Fiber Communication Meeting, IEEE and Optical Society of America, Shoreham Americana Hotel, Washington, D. C., March 6–8.

Mid-Atlantic Computer Exposition, The Caravan Group (Newton, Mass.), New York Coliseum, New York, March 13–15.

12th Annual Simulation Symposium, IEEE, Causeway Inn, Tampa, Fla., March 14–16.

Fifth Annual Conference and Exhibit on Industrial and Control Applications of Microprocessors, Information Gatekeepers Inc. (Brookline, Mass.), Sheraton Hotel, Philadelphia, March 19–21.

IECI '79—Industrial and Control Applications of Microprocessors, IEEE, Sheraton Hotel, Philadelphia, March 19–21.

Eighth Annual Programmable Controllers Conference and Equipment Display, Engineering Society of Detroit, to be held at the society's headquarters, March 20–22.

Trends in On-Line Computer Control Systems, Institute of Electrical Engineers (London), University of Sheffield, UK, March 27–29.

Technical Symposium East '79, Society of Photo-Optical Instrumentation Engineers (Bellingham, Wash.), Hyatt Regency Hotel, Washington, D. C., April 2–5.

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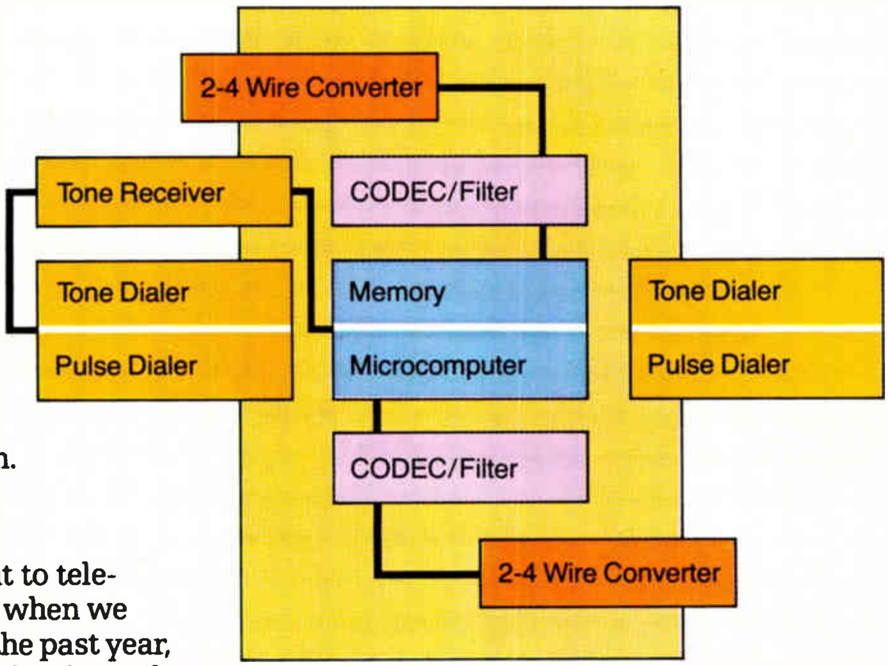
The Mostek System Solution

Only Mostek offers a complete system for your telecommunication applications. Innovative design techniques give Mostek the edge in telecommunication product features. High density RAMs, ROMs, PROMs and versatile microcomputers complete the picture. Total compatibility from a single source—that's why we call it the system solution.



Designed by the leader

Mostek made its commitment to telecommunication products in 1974 when we built our first tone dialer. During the past year, we've shipped over three million circuits and earned a reputation as industry's most dependable source for reliable products. Products like tone receivers, tone dialers, pulse dialers, repertory dialers and CODECs are available in volume now. Monolithic filters are coming soon, followed by 2-4 wire converters.

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The Mostek System Solution will meet your toughest specifications. Whether you're designing central office switching systems, key telephone systems, PABX, remote concentrators, channel banks, or automatic call distributors, contact Mostek for the solution, 1215 West Crosby Road, Carrollton, Texas 75006; phone 214/242-0444. In Europe, contact Mostek Brussels; phone (32)02/660.25.68.

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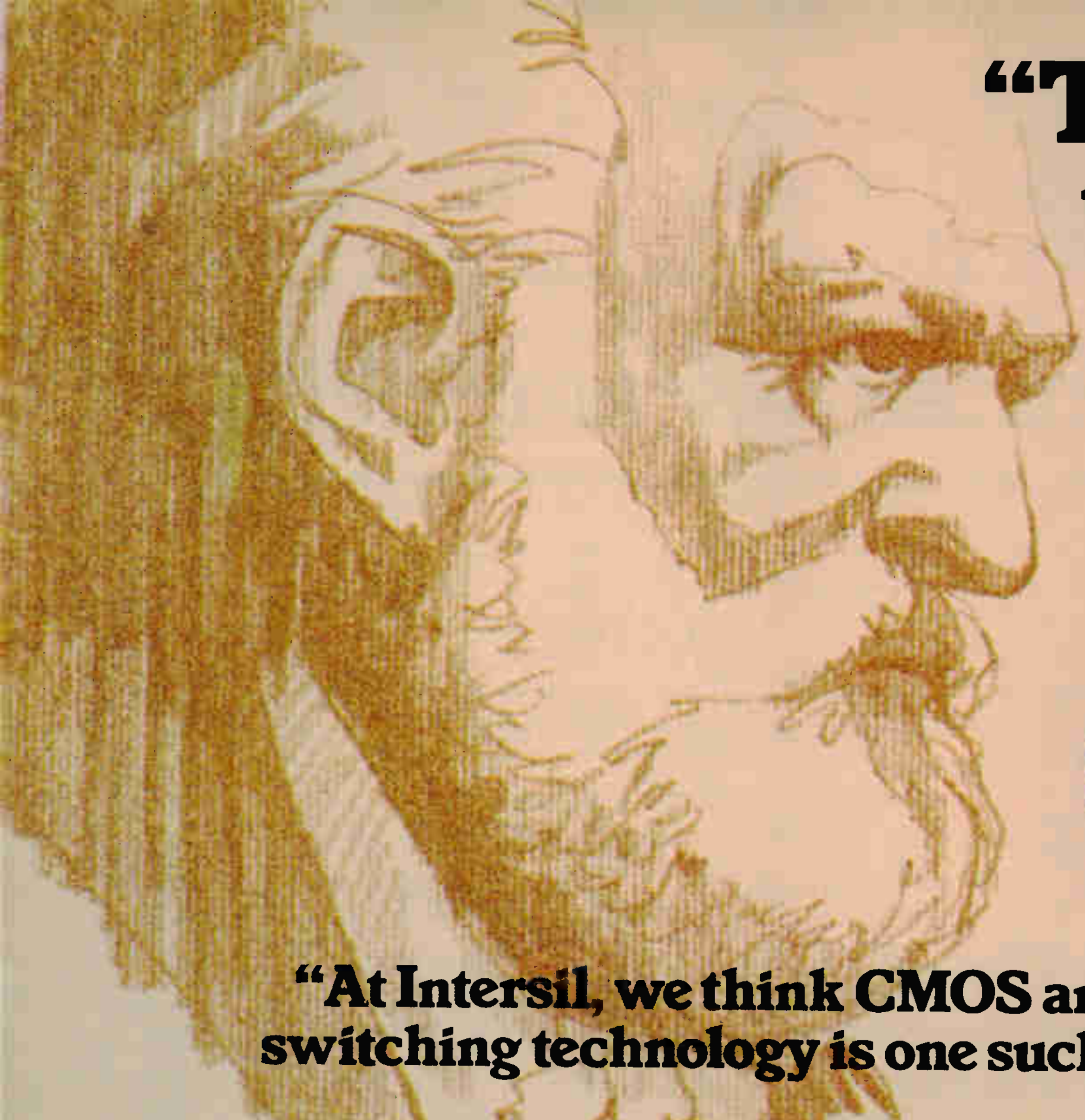
“There is
than a



“At Intersil, we think CMOS analog switching technology is one such idea.”

Intersil 1967-

LEADERSHIP IN ANALOG SWITCHING.

Intersil has offered a number of "firsts" in analog switching:

- First, with virtual ground switches
- First, with ultra low power CMOS monolithic analog gate technology
- First, with monolithic CMOS latch proof technology
- First, with Varafet technology

Today we offer over 150 analog switching devices ...tomorrow, we'll be introducing new devices that reduce component count, reduce overall system cost and increase reliability. We think cost effective solutions to your design problems are an idea whose time has come.

VIRTUAL GROUND SWITCHES.

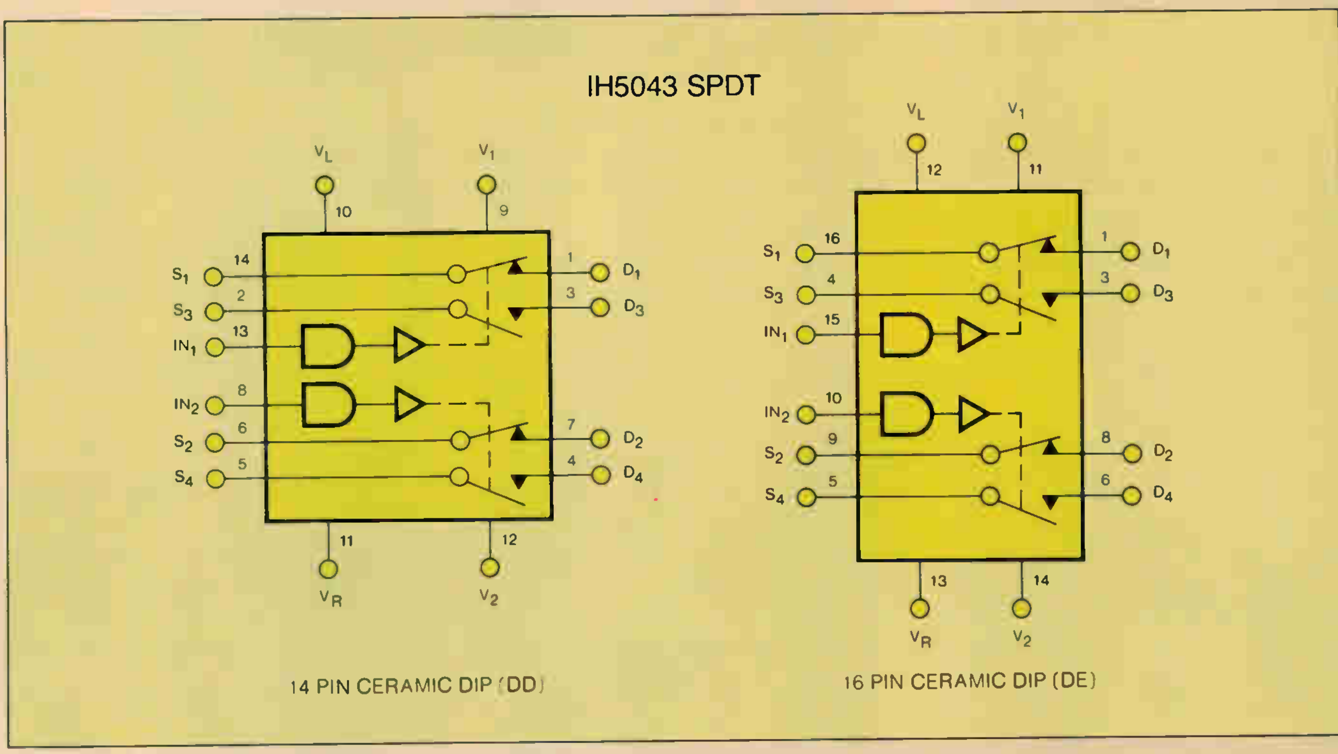
The IH5009 series of analog switches was designed to fill the need as an easy-to-use, inexpensive switch for virtual ground switching into operational amplifiers. This family is primarily intended for constant impedance switching multiplexing and interfaces with 5V or 15V logic. Switching accuracy is increased through a built in compensating FET for use in the gain feedback loop of the op amp.

ULTRA LOW POWER CMOS GATES.

The IH5040 family of monolithic analog gates was designed using an improved, high voltage CMOS technology. The advantages are T^2L, DTL, CMOS and DMOS compatibility...combined with ultra low power operation. The technology provides input overvoltage capability to ±25V. Diode protected inputs eliminate the need for special handling techniques associated with other CMOS analog gates. Destructive latchup has been totally eliminated. And, there is no need for external logic to prevent channel-to channel shorting. Power requirements of the IH5040 family of CMOS gates, up to 30 times lower than previously available state-of-art devices, open up new low power applications in

nothing more powerful
dea whose time has come."

Victor Hugo, 1802-1885



portable and battery operated equipment.

HIGH PERFORMANCE VARAFET CMOS GATES.

Intersil was first with a family of low power, high level Analog Gates: The IH181 Series. The Family incorporates two of our leading technologies: CMOS and VARAFET.

The result is a series of latch proof CMOS gates which draw extremely low quiescent current from power supplies...reducing system power dissipation from milliwatts to nanowatts with no sacrifice in switch performance. The IH181 family is pin for pin compatible with the DG181 family.

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The IH401 Quad J-FET Switch varactor diodes integrated into the gates of the FETS provides high speed, easy to use switches while eliminating the need for external capacitors, diodes and resistors. That means high performance analog switches at lowest possible cost.

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Four very small ways to improve on your PC design.

With four types of switches—rockers, pushbuttons, toggles and DIPs—Cutler-Hammer offers one of the industry's broadest and most unique selections of PC subminiatures.

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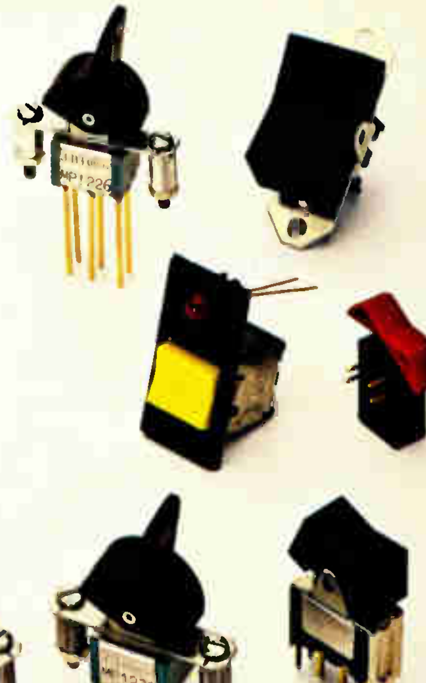
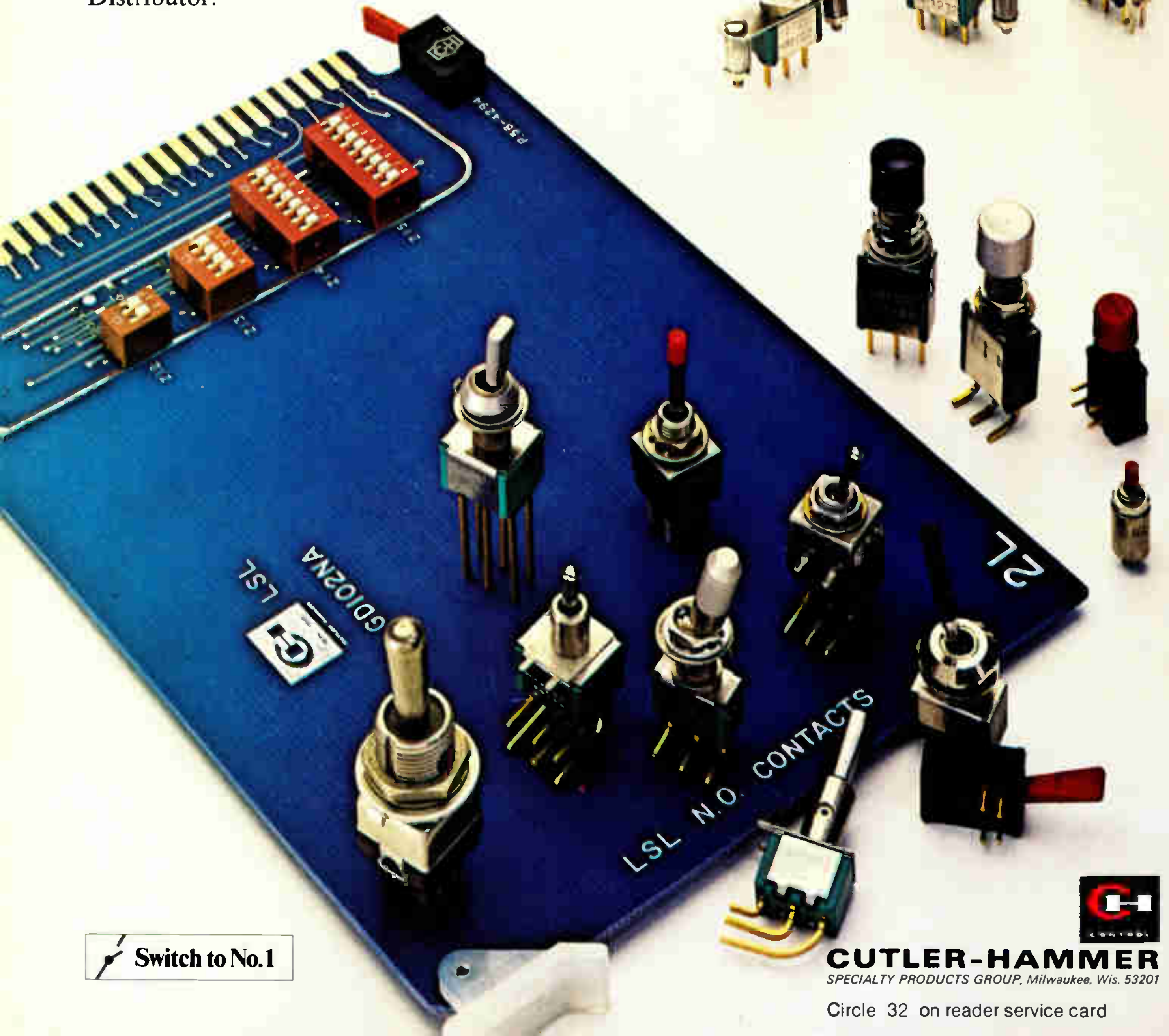
To improve your next design in any number of small ways, contact your Cutler-Hammer Sales Office or Switch Distributor.





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Circle 32 on reader service card

Electronics newsletter

GM robot sorts, places objects on moving conveyor

A robot equipped with camera "eyes" is being touted by General Motors Corp., its developer, as the first that can sort and place objects on a moving conveyor belt. Previous versions could work only on stationary surfaces. In the unit, called Consight, a charge-coupled-device camera from Reticon Inc. with a single line of 100 picture elements, is linked to a pair of Digital Equipment Corp. PDP-11s and a huge Cincinnati Milacron arm. **The result is a robot that can lift hundreds of pounds and can identify and track a variety of casting parts** for palletizing or other sorting tasks. A streamlined version, hardened to withstand a metal foundry environment, will be installed on a production line next year, says GM.

Motorola widens processor family with n-MOS, C-MOS

Samples will be out in a few months of Motorola's new single-chip microcomputer, the 6805. A scaled-down version of the 6801, the n-channel 6805 will be the core of a low-end microcontroller family that will eventually offer many on-chip features like analog-to-digital conversion. Housed in a 28-pin package, the chip will sport 1 kilobyte of read-only memory, 64 bytes of random-access memory, 20 input/output lines, clock, timer, and a central processing unit using 6800-family instructions.

Following shortly after the 6805 will be a sister part from another of Motorola's operational groups, **a complementary-MOS pin-for-pin-compatible version of the one-chipper.** First versions out will use 5-μm channel lengths to give the 14-6805 a 1-MHz clock frequency. But when the silicon-gate C-MOS process gets its first design-rule reduction to 3-μm, the part will speed up and have a density almost equivalent to that of Motorola's high-performance H-MOS n-channel devices.

Hughes prepares development system for C-MOS devices

Readying its entry into the microcomputer development systems business is Hughes Aircraft Co.'s Solid State Products division. The Hughes system is **intended as a design and software aid for Hughes' 1800 series of complementary-MOS devices,** manufactured under license from RCA's Solid State Products division. The full development system will be available within months, priced at about $10,000. It will also accommodate MOS processors having 8080-type architecture.

Swiss come up with smaller analog watch

Microminiaturization is the battle cry in the latest Swiss parry of the digital watch onslaught. Ebauches SA, Switzerland's leading producer of watch movements, is introducing in the U. S. a $4,400 analog wristwatch with what the firm says are the world's smallest quartz tuning fork, stepping motor, and battery for a total thickness of only 1.98 mm. The circuitry also includes a complementary-MOS integrated circuit for electronic timesetting, plus other microminiaturized components. **The technology is adaptable to less expensive models,** although the firm has not said when they will be along.

CBS to test French Antiope videotext system

Télédiffusion de France, the government agency that handles the broadcasting chores for the national radio and television networks, is pushing hard to have its Antiope teletext system adopted by the Federal Communications Commission as a U. S. standard. As part of its campaign, TDF's overseas sales unit, Sofratev, will supply hardware to the Columbia Broadcasting System for a trial scheduled to start in early April.

Panel to seek standards for bubble memories

As 256-K and 1-megabit magnetic-bubble memories begin to rise above the commercial horizon, a task force of the Joint Electronic Device Engineering Council's JC-42 committee will meet at next month's International Solid State Circuits Conference in Philadelphia to try and hammer out standards for such things as nomenclature, architecture, pin locations, and electrical characteristics. **But don't expect much progress, and even if there is some, it will be too late,** declares one insider. "There's much less cooperation [among companies] than there was in 4-K RAMs," he says, because some companies insist on their own designs.

New bipolar group at National plans ECL thrust

Looking for the bipolar memory market in high-end mainframe computers to take off by 1981, **National Semiconductor Corp.'s new bipolar memory operation plans to contest such leaders as Fairchild and Motorola** in the emitter-coupled-logic end of the business. On tap are 1,024-bit and 4,096-bit random-access memories with target access times from 10 to 25 ns to complement 1-K ECL RAMs coming out. National also will test-market the market in ECL programmable ROMs this summer with a 256-by-4-bit device expected to have an access time of under 10 ns. The director of the bipolar operation, formed this month, is Frank Barone.

Harris lists bi-FET innovations

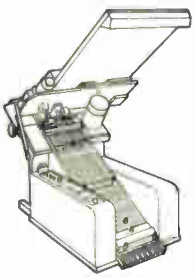
Harris Semiconductor in Melbourne, Fla., is about to introduce an innovative linear device: a bipolar-field-effect-transistor (bi-FET) operational amplifier with dielectric isolation in two models, **that exhibit gain-bandwidth products of 60 and 120 MHz.** The HA-5150 and -5160 are twofold improvements over the -5100 and -5110 introduced several months ago. The new devices exhibit 50-V/μs and 120-V/μs slew rates, respectively and are packaged in TO-99 cans. The next step is to halve the 9,000-mil^2 die size and to place an n-channel FET at the front end, thereby doubling or tripling the speed of the devices.

Addenda

Carm Santoro, who left American Microsystems Inc. to become vice president of Monolithic Memories Inc. for four months [*Electronics*, Jan. 4, p. 14], **has returned to AMI as group vice president for microprocessors and memory products.** . . . To help it meet orders expected to reach $1 billion for computational products alone, **Hewlett-Packard Co. will build plants in Vancouver, Wash., and Roseville, Calif.** . . . Even as RCA Corp. prepares to enter the video-disk player market (p. 50), it is pushing its video-cassette recorders with a **$2 million promotion campaign for the first quarter.**. . . Hitachi Ltd. is negotiating with General Motors to supply the 6800 microprocessor it produces under license from Motorola. **The deal would involve up to 1 million or 2 million chips a year.** . . . Texas Instruments is **increasing the speed of its 16-bit microprocessors to 4 MHz.** . . . Robert B. Heikes, who resigned his No. 2 slot at Motorola Semiconductor Group [*Electronics,* Nov. 9, 1978, p. 46], **is becoming National Semiconductor Corp.'s international vice president,** stationed in Munich. . . . Concerned that U. S. patent laws don't adequately shield their big investments in new chip designs from unauthorized copying, Silicon Valley semiconductor makers are pushing for a new law that would amend the Copyright Act of 1976 and **permit them to copyright chips.**

"At MCT, We Take The Sweat Out of Buying a Hot Handler…

…With Our Series 2608E"



Series 2608M
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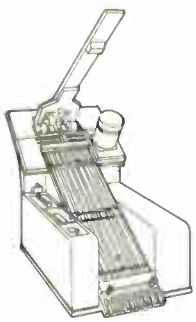
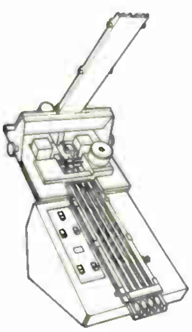


Series 2608
10,000 DPH
Ambient Temperature
Handler



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(1) Gnostic Concepts, Inc., *VLSI Technological Market Forecast*, 1978, Palo Alto, California.
(2) Anderson/Bogart, *Vertical Dis-Integration* 1978, Los Altos, California.
(3) Linear Corp., Bill Schanbacher, President, Inglewood California.
(4) National Radio Astronomy Observatory (NRAO), Ray Escoffier, Program Manager, Socorro, New Mexico.

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C-MOS op amp offsets errors with continuous sampling technique

Within frequency limits of dc to 10 Hz, new design has maximum input offset voltage of ±5 microvolts

Ideally, when the difference between the voltages on an operational amplifier's inverting and noninverting inputs is zero, the output voltage should be zero, too. In reality, however, circuit imperfections upset this balance and the degree of upset is described in terms of error voltages and currents. Intersil Inc., Cupertino, Calif., has come up with a technique called commutating autozero (CAZ) to markedly reduce these offset errors. What's more, it is a model of simplicity.

Working in complementary-metal-oxide-semiconductor technology, which is inherently noisy and prone to offset error, designer David Bingham devised a way to continuously sample these errors, store them on a capacitor, and then insert them, in reverse, in series with the input, thereby canceling the errors.

The key word is *continuously* because methods for doing the same thing *periodically* are used in most dual-slope-integration analog-to-digital converters. In contrast, Bingham's CAZ amplifier scheme, shown in the figure below, provides signal processing and autozeroing at all times except for a momentary switchover mode.

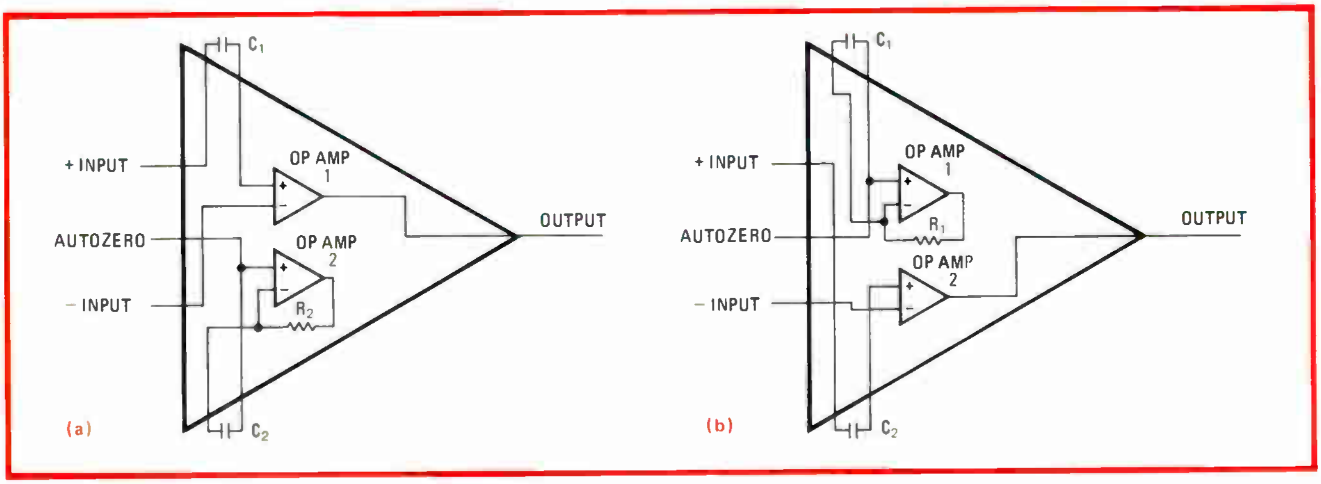
Without this technique, typical offset errors of a C-MOS op amp would render it useless for low-signal-level applications. But with it, the op amp becomes useful at the level of the low tens of microvolts. It dissipates only 20 milliwatts at most, operating from ±5-volt supplies.

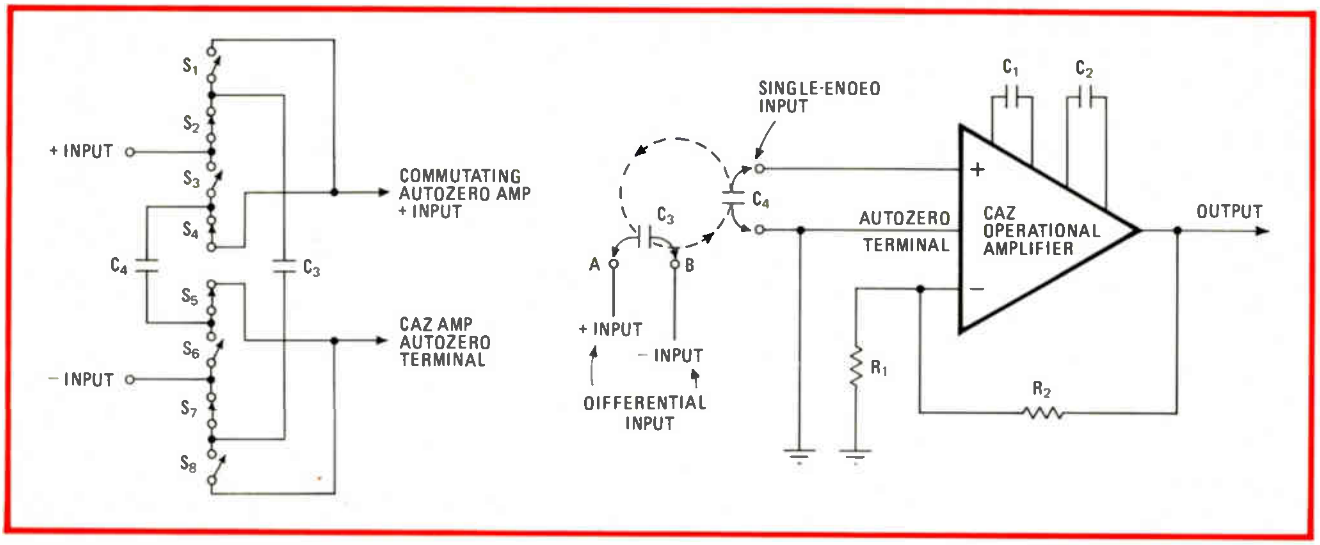
Two for one. "The method is so straightforward that I continue to marvel that it has not been done before," says Bingham. Instead of one op amp, he put two of them on the semiconductor substrate, along with a clock oscillator, a digital divider network, and a dozen analog switches—six on each op amp to switch among input and output pins, internal resistor, and external capacitor.

"While one op amp is sampling and storing its errors, the other is connected in series with its capacitor to the input signal to be processed," he explains. Then, after a nominal 6.25 milliseconds, a clock pulse toggles the analog switches and the op amps switch over and reverse roles. The external capacitors are about 1 microfarad each.

The CAZ amp's application is limited to frequencies 1/10 or less than the commutation rate because of noise introduced at the switching frequency and its harmonics. Consequently, the first Intersil product to use the new technique, the ICL 7600

Here it is. With op amps in the ICL 7600 (a), one processes an input signal (op amp 1), and the second stores the offset errors on an external capacitor (op amp 2). When the op amps change roles, the error on C_2 is in series with op amp 2's input (b), canceling offset errors.





More complex. By switching C_3 and C_4 between the differential input and the input of a CAZ operational amplifier (left), Intersil effectively converts the differential input in its ICL 7605 instrumentation amplifier into a single-ended kind (right) suitable for the CAZ amp.

CAZ operational amplifier, is optimized for applications with signal frequencies between dc and 10 hertz and gains of no more than 100, according to Skip Osgood, marketing manager for data-acquisition products. Its commutation frequency is a nominal 160 Hz, and he says it will compete for sockets with modular chopper amplifiers, as well as with precision bipolar op amps.

Within optimal frequency limits of dc to 10 Hz, the ICL 7600 has a maximum input offset voltage, V_{os}, of only ±5 microvolts. Even more impressive is the temperature coefficient of V_{os}, which is guaranteed to be less than 0.1 μV/°C. "We're measuring tempcos at 0.005 μV/°C, typically," Osgood claims. Long-term temperature stability is a low 0.2 μV per year and minimum open-loop gain is 90 decibels, he says.

The difference. For instrumentation applications, Intersil modifies the CAZ op-amp technique to function as a differential rather than an operational amplifier, as shown in the figure above. The differential signal is stored on a capacitor, which is then switched to a CAZ op amp's single-ended input. At the same time, a second capacitor is switched from the CAZ amp's input back to the differential input—a variation on the technique.

By combining a CAZ op amp with extra analog switches and two additional capacitors, Intersil created a second product, the ICL 7605 instrumentation amplifier. Its common-mode rejection ratio is 100 dB at 0.3 V above the positive supply and 0.3 V below the negative supply. Moreover, it shows a power-supply rejection ratio of 110 dB, according to Osgood. Also, it eliminates the need for precision-tracking resistors like those found in typical instrumentation-amplifier circuits, which use three op amps.

Intersil is providing samples of both the 14-pin ICL 7600 and 18-pin ICL 7605 now and expects to be in full production by late February. The 7600 costs $6.50 apiece and the 7605 $15 each for 100 units. □

Instruments

Dual-trace scope acts like dual beam

An $845 dual-trace oscilloscope that behaves almost as if its inputs come from two independent writing beams, rather than from one, is about to bow at Ballantine Laboratories Inc. The dc-to-20-megahertz scope is, in fact, aimed right at the job that the more expensive dual-beam instruments do so well: presenting a stable display simultaneously of two signals that are not quite synchronous.

What distinguishes the model 1032A portable scope is a clever twist in its circuitry, separating the triggering function from the dc-level-positioning function by providing an electronic switch for each circuit. Thus the dc-level signal no longer distorts the trigger signal as in other single-beam, dual-trace scopes. "The trigger sees the time-base signal exactly," says Fred L. Katzmann, president of the Boonton, N. J., firm.

The standard setup in single-beam dual-trace scopes (part a of the figure on p. 41) runs each of the two input channels through its own attenuator, preamplifier, and a position control, which adds the dc level set by the operator. Both channels then feed into one electronic switch, Katzmann explains.

Dual purpose. The switch performs two functions. It alternately feeds the two input signals with their position-determining dc offsets to the display circuitry. It also alternately feeds the channels' signals to what is called a composite trigger that contains a high-pass filter, as well as the Schmitt trigger that starts the beam's sweep when the incoming signal reaches the voltage level specified by the operator.

In Ballantine's 1032A, each channel's preamplifier has two outputs (part b of the diagram). One output feeds a dc-level position control and then goes to an electronic switch. The other output goes directly to a separate electronic switch that feeds the trigger.

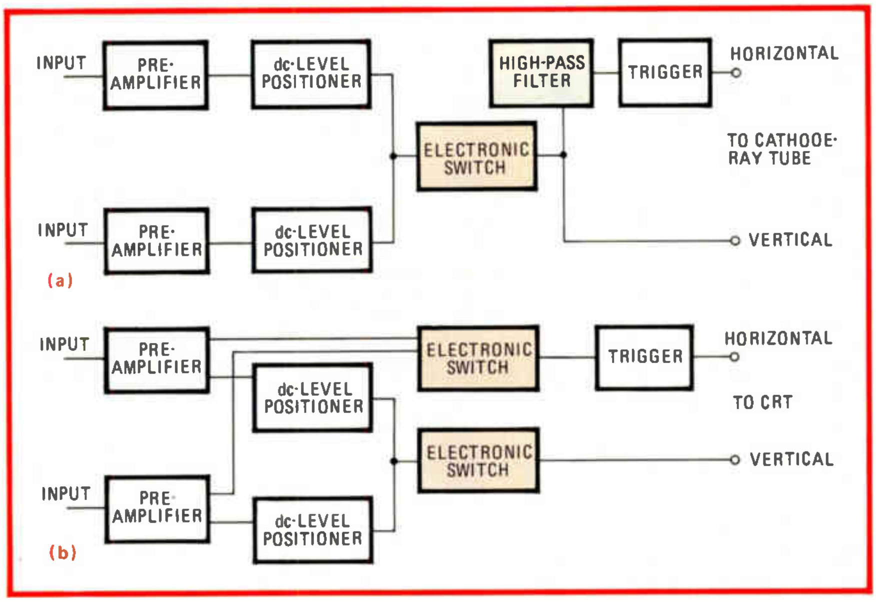
No high-pass filter is necessary, because there now is no vertical-position signal to remove from the trigger signal. In the composite trigger, the filter serves exactly that role, but this filter has problems of its own.

Problems. "The filter will only maintain a constant output so long as its input is constant," says Katzmann. A major problem occurs with such equipment as computers, where peripherals frequently have mechanically controlled time signals rather than crystal-controlled. Thus the signal is likely to be slightly asynchronous, and its constantly changing frequency means a constantly changing dc-level signal, and consequently a trigger signal with jitter.

Not only is the filter eliminated, but the second electronic switch can be optimized for the triggering function, Katzmann says. "You get a clear jump from channel to channel."

It is because of this clear jump that Ballantine calls its new trigger mode "independent dual triggering." "There is less interrelationship between the signals as the trigger sees them," says Katzmann. "There is less modulation of one by the other."

To be available beginning March 1, the 1032A features nine other trigger modes, a full 3-decibel passband of dc to 20 MHz, and a rise time of 17.5 nanoseconds. It offers calibrated vertical sensitivities of 5 millivolts per division to 20 volts/division and calibrated sweep speeds of 1 microsecond/division to 0.5 second/division. All calibrated vertical and horizontal range steps are accurate to within ±3%. □



Add a switch. Instead of one electronic switch (a), Ballantine's new scope has two (b), separating the circuits for triggering and for dc-level positioning.

Fiber optics

Bell Canada tests home fiber optics

In the world's first field trial of a fiber-optic system for home telephones, Bell Canada has started a two-year test of a voice, video, and data service to 35 homes in Toronto. "The purpose is to integrate all traffic, whether it be voice, video, or data, in a common mode and on a common base in an effort to maximize productivity," says Jack F. Stinson, Bell Canada's vice-president–operations staff. "This will make it possible to ease the per-capita burden of providing expensive, far-flung telecommunications service to a small population."

The $1.75 million installation has 1.2 kilometers of graded-index fiber-optic feeder cable, plus about 200 meters of graded-index entrance cable for each of the subscribers. Using light-emitting diodes, the beams of light that carry the information will pulse along on hair-thin strands of glass that run under the streets much like conventional cable. In addition, the fiber actually goes to the customer's telephone.

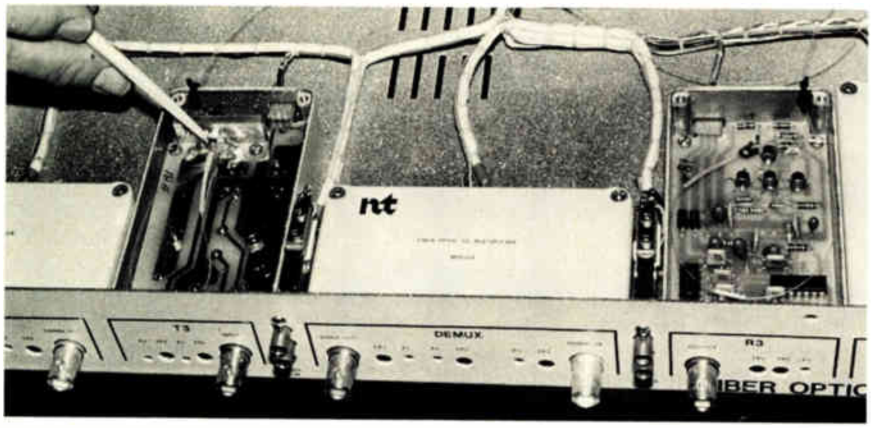
Not ideal. The system is incomplete in the sense that it is not fully digital. However, it was not difficult to provide telephony and data-signaling capabilities using available analog components and techniques, Stinson explains. Bell Canada found that single telephone-channel systems with an analog subscriber carrier could be interconnected with the optical system after only minor changes. These modifications included a slight shift in the carrier frequency and some changes in the signal level.

The optical system is made with off-the-shelf components. For example, the 840-nanometer LEDs for the transmitters are not perfect for this sort of system, but such LEDs are readily available and adequate for this first test.

In fact, Bell Canada did not want to wait for all aspects of an integrated fiber system to be available. The telephone company preferred to get information on the interaction of new techniques, on cable technology, and on the electro-optic and operational aspects of the setup as soon as possible.

The best subscriber installation would use fiber in the loop plant (the first switching center connection to the residence), employ digital transmission, and make use of integrated-circuit technology. This will come in 1985 or thereabouts. For now Bell is satisfied with having taken a giant step in gaining practical experience, according to Stinson.

Voice and video. Each individual connection is designed to carry one telephone channel, together with the capability of a centrally switched,



In the plant. A typical fiber-optic terminal at the switching plant has an optical transmitter (left) and an optical receiver (right). Bell Canada is using analog transmission technologies.

one-way video channel from the central office to the subscriber. It can also carry the associated low-speed data-signaling channel from the subscriber to the central office for video channel selection. This will enable cable television or other video services to be tapped as required. Four of the residences will operate on one fiber only in a duplex mode for both transmission and reception, and the rest will use unidirection transmission over two fibers.

In various phases of the tests not only will basic telephone service be demonstrated, but customers will be able to take advantage of such services as conference television, remote video surveillance, and a video library. Later trials will include interactive graphics such as videotext. ☐

Laser refines optical-fiber quality control

Corning Glass Works has developed a new way to keep close tabs on the characteristics of fiber-optic cable during manufacture. The company is concerned about the refractive index of the glass-fiber core, which must vary parabolically with radius for wideband, multimode propagation. This relationship ensures that light-propagating modes travel over the same optical lengths and experience identical time delays. If they do not, transmitted data suffers from pulse broadening or decreased bandwidth.

The technique, developed by staff member Robert Olshansky at the corporate research laboratories in Corning, N. Y., is called a differential-mode delay measurement. It uses a mode-locked krypton gas laser providing a spot 10 micrometers in diameter. The laser's pulsed output scans radially outward from the center of one end of a length of glass fiber. At the other end, an avalanche diode detects the emerging light, which is displayed on a sampling oscilloscope.

As the spot scans, measurements are made of the arrival times for each pulse peak, performance that can be predicted mathematically. The times are correlated with the refractive-index profile in the fiber. Thus the quality of the fiber is determined, and the manufacturing process can be adjusted accordingly.

Olshansky points out that positioning of the fiber and obtaining the data are computer-controlled and require less than five minutes. Moreover, the data is highly sensitive to very small profile changes, he says.

This technique is a more valuable aid to the manufacturing process than older profile-taking methods, he claims, because it represents an average over the length of the cable. Other profile measurements involve only small cable lengths.

"The Corning technique is quite suitable for a manufacturing environment," Olshansky concludes. "Ultimately a small injection laser will be used. It is no more difficult than other routine quality-control measurements."

Components

MESFETS and SAW improve uhf tuner

The Federal Communications Commission may soon grant Texas Instruments as much as $120,000 for further development of an unusual high-performance ultrahigh-frequency television receiver. This possibility arose when the FCC, persuaded by a TI prototype it received early last year [*Electronics*, March 16, 1978, p. 57], launched a major inquiry late last month aimed at improved uhf receiver design and transmission standards, as well as to expand the number of channels permitted in a geographic area.

"We haven't negotiated [the additional contract] with TI yet, but we're certainly looking toward that," reports Paul Fox, an engineer in the FCC's Office of Plans and Policies. The additional money would be available as part of a $750,000 surplus congressional appropriation that is being set aside for improving uhf reception.

TI's unusual approach uses a mixer and amplifiers made of Schottky metal-semiconductor field-effect transistors (MESFETs) to boost television frequencies up to 346 megahertz. This is some eight times higher than the 45-MHz intermediate frequency of conventional uhf tuners, which is usually converted down for signal processing.

Enter SAWs. At 346 MHz, TI brings into play a pair of highly selective surface acoustic-wave filters to reject unwanted interfering signals. These SAW filters can be made very small and with extremely narrow bandwidths. Moreover, since they are fabricated photolithographically, they can be made cheaply, the firm believes.

Though additional development work needed on the tuner has not been spelled out, the FCC has expressed an interest in possible design changes that would reduce both the receiver's noise figure and its cost. Possible cost-saving steps

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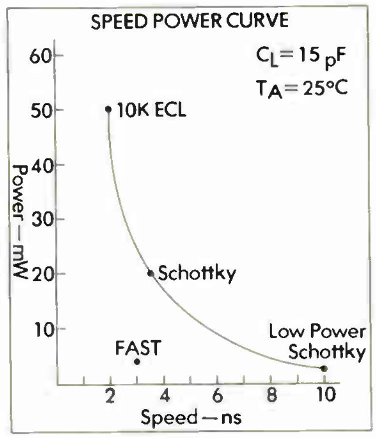

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include development of techniques for using only one SAW filter instead of the two in the present device, says Darrell Ash, senior communications engineer at TI's Central Research Laboratories.

Another possibility is development of an integrated circuit that could house up to 16 active components in the i-f portion of the receiver on a single chip. Such application of large-scale integration techniques could reduce the cost of the tuner even further than projected in TI's original report to the FCC, Ash says. According to that report, the first 1.5 million production-line units could be made for about $9 more apiece than conventional receivers, which the Dallas firm estimates would translate to an increase of $27 to $35 per unit in the retail price of a TV set.

More improvements. Since delivering the final prototype version to the FCC last January, TI has already made several improvements in the device, Ash says. Among other things, an IC has been developed that houses on a single chip all four MESFETs used in the receiver's balanced silicon MESFET mixer. This has reduced system noise from 14 decibels maximum in the prototype device to about 10 dB maximum in the redesigned version, Ash notes, thus exceeding the original FCC goal of 12 dB.

Since delivery of the prototype, TI has also reduced the unit to a single 5-by-11½-inch printed-circuit board, in contrast to the two 5-by-6-in. boards of the original design.

The prototype was developed under a $200,000 FCC contract awarded in August 1976. TI proposed its own set of performance goals for the contract after a request for proposals based on the FCC's own specifications attracted no bidders. As Fox notes, there has been little market incentive for TV manufacturers—already squeezed by tight industry profit margins—to spend money developing a tuner with the improved interference-rejection characteristics desired by the commission.

Though TI had been working on an improved TV tuner with its own funds for several years before the FCC contract, Ash says that work has now stopped pending additional FCC funding or increased interest from TV set manufacturers. An additional 18 months of work would be necessary to get the tuner ready for production, he says. □

Communications

ACS controversy flares at FCC over AT&T's computer services

Where does data communications end and data processing begin? The Federal Communications Commission may be obliged to make that Solomon-like judgment this year. The immediate issue forcing the FCC to take a definitive look is ACS—the Advanced Communications Service of the American Telephone & Telegraph Co., which wants a declaratory ruling in order to begin the service this year [*Electronics*, Aug. 3, 1978, p. 79].

Meanwhile, a host of comments to the FCC earlier this month by both the communications and computer industries heightened the developing controversy. Directly opposed conclusions were reflected in the comments, and at least one value-added common carrier threatens a court appeal unless the commission rejects the AT&T petition and instead investigates the communications company's "character" as part of further proceedings.

Of those companies and trade associations responding, 13 were opposed to the ACS petition, 3 were in favor, 2 straddled the fence, and 1 reserved the right to comment later.

The split. Reflecting the division within the computer industry, the Computer and Business Equipment Manufacturers Association (CBEMA) says ACS clearly involves data-processing functions like manipulation and retrieval, while minicomputer maker Digital Equipment Corp., Maynard, Mass., says that ACS "clearly is a communications service and not a data-processing service" and will enhance computer industry competition.

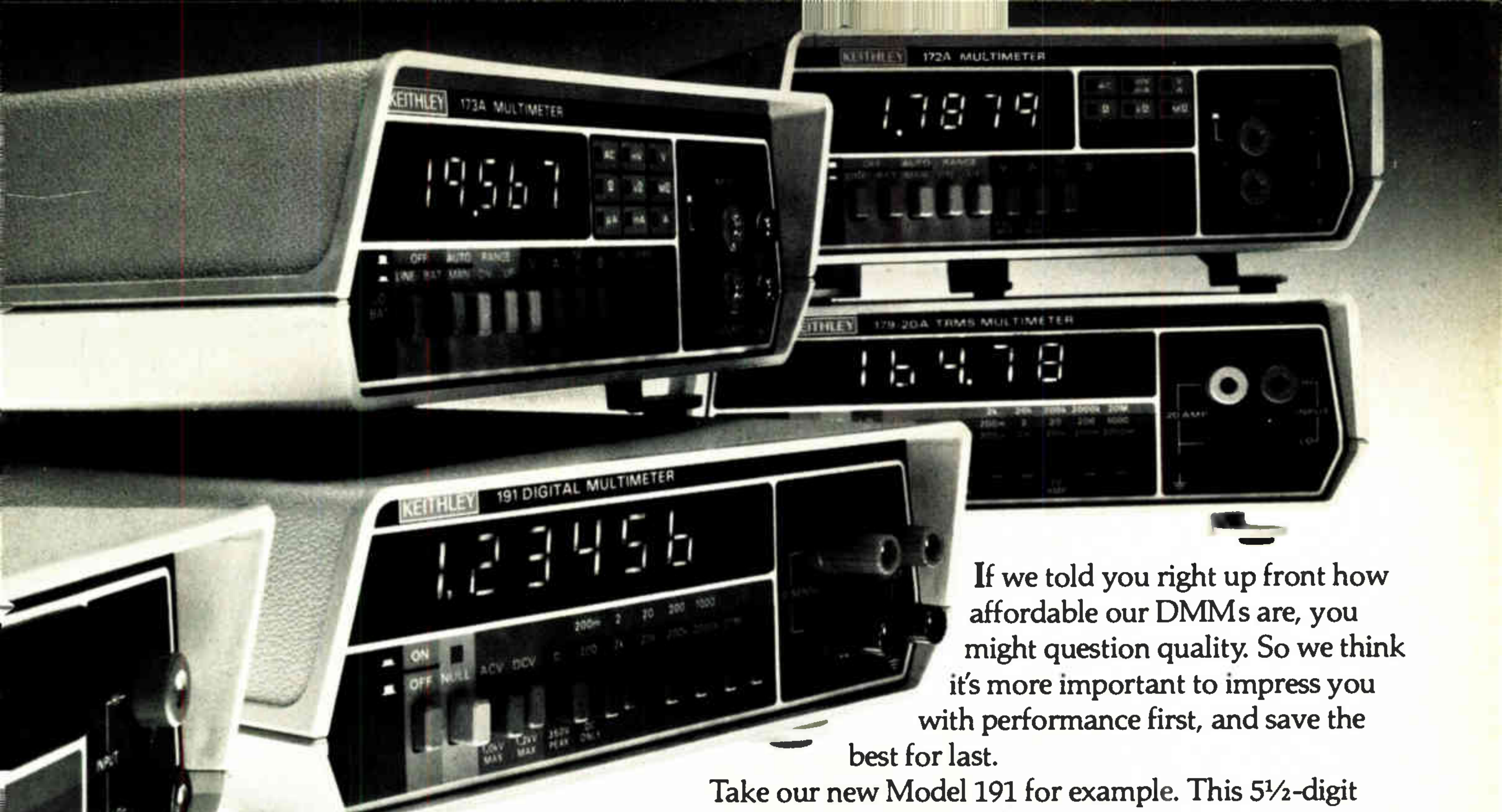
Tymnet Inc., the Cupertino, Calif., value-added carrier subsidiary of Tymshare Inc., comes down on CBEMA's side and for the first time injects the issue of AT&T's "character" into a common-carrier hearing. Tymnet argues that FCC rules "unequivocably require the commission to consider an applicant's character" in granting radio broadcast licenses and notes that AT&T has radio licenses for microwave channels.

Tymnet says it does not want the FCC to revoke AT&T's radio licenses, but is insistent that the commission's broadcast rules require it "to consider AT&T's past conduct in evaluating this application"—a conduct that Tymnet charges shows "a pattern of persistent and willful violations" of FCC rules by using Bell's "monopoly power in an unlawful attempt to restrict competition."

After extensive legal research on the question of restricting competition, costing in excess of $100,000, Tymnet president J. Robert Harcharik in an interview says he is "outraged" by AT&T's actions and will appeal in court if the present "defective and incomplete" ACS petition is approved.

Other charges. Two other questions are raised by Tymnet and other competitors of ACS regarding excessive delays in getting digital lines and local exchange facilities from AT&T. A decline in AT&T's ability to meet the 23-day timetable for installation of new lines—down to 60% to 65% today from 90% to 95% a year ago, Tymnet says—is attributed by AT&T to a shortage of skilled craftsmen that runs as high as 50% in some areas.

Tymnet asks the FCC: "Should AT&T be offering a new competitive service when it is unable to meet its current obligation? What priority



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will AT&T assign to requests for circuits when it has requests for circuits for ACS?"

On the other side of the coin, Digital Equipment Corp. told the commission that it favors ACS, since "users will be able to select computer equipment based upon the individual features of the equipment, rather than being forced to make decisions based primarily upon the need to assure compatibility with existing systems," an obvious reference to IBM's market position.

However, a key feature of DEC's pro-ACS stance, that the service will resolve the problem of computer equipment incompatibility, "is not a valid basis on which to base policy, even though it is a highly desirable goal," believes one FCC staff member. □

Business

SMC and SSS ink multiple agreement

Not long after Solid State Scientific Inc., Montgomeryville, Pa., approached SMC Corp. in Hauppauge, N. Y., to secure a second supplier for some of its custom parts, the two semiconductor manufacturers have struck a two-pronged agreement: they will exchange know-how and cross-license one another's patents in n-channel MOS processing, and they will second-source some of each other's current and future products.

For both, the pact, signed earlier this month, seems a natural one—it will broaden the technology base both of these specialized companies need to secure a niche amid the commodity business of major chip makers.

To SSS, a company whose $28 million in sales last year was obtained mainly from complementary-metal-oxide-semiconductor circuits, the deal gives a Berlitz course in n-channel technology. "We need n-channel to broaden our customer base," explains Leonard P. Kedson, president.

He regards the agreement as key to his firm's anticipated 40% to 50% growth in the current year. Apparently so, because in addition to royalties for SMC's patents, SSS has paid the company an undisclosed lump sum of cash in advance.

It expects immediate benefit from the first part of the agreement. According to Kedson, it will first put its newly gained knowledge to use to aid in the development of a new high-performance C-MOS process it calls HC-MOS, although he declined to say just how.

Other rewards. For SMC, a $12 million company specializing in controller chips for video displays and floppy-disk and tape drives, the deal is more than just another royalty check (see "Two small firms with international horizons"). "We've had lots of licensees before," explains Paul Richman, president of SMC, "but with SSS we're looking for a more intimate relationship." He adds that though it is not part of the agreement, his company is interested in obtaining a foothold in C-MOS technology.

The second part of the agreement is more clearly bilateral: each party can choose to second-source the n-channel parts of the other, paying due royalties. Solid State will first

Sitting pretty. SMC Corp.'s president, Paul Richman, looks for more than royalties from agreement with Solid State Scientific.

Growing. Solid State Scientific's president, Leonard P. Kedson, sees the acquisition of n-channel expertise as a key to growth.

Two small firms with international horizons

The agreement signed by SMC Corp. and Solid State Scientific Inc. further enhances what appears to be a bright future for the two firms, each of which has succeeded in attracting worldwide interest in its technology.

SMC is in the enviable position of owning basic patents in n-channel metal-oxide-semiconductor processing that have resulted in royalties from several large companies, including General Motors, Texas Instruments, and ITT, and a cross-licensing agreement with IBM Corp. Late last year the Hauppauge, N. Y., firm and EFCIS, the jointly owned subsidiary of Thomson-CSF and CEA, the French atomic energy agency, signed an agreement by which SMC second-sources the French firm's video controller chips. That agreement provides SMC with a full line of controllers and extends its reach into European markets for its own product line.

Solid State is active on the international scene as well—in fact, it does 40% of its business overseas. The Montgomeryville, Pa., company recently agreed to supply the Soviet Union with liquid-crystal-display technology. Though still subject to U. S. government approval, the agreement should net Solid State royalties within the year. SSS also has similar agreements with Italy and Yugoslavia.

Solid State's agreement with RCA Corp. to second-source the 1800 complementary-MOS microprocessor family gives it access to some of RCA's know-how and the option to make RCA's silicon-on-sapphire parts.

whip up its n-channel process by building three of SMC's standard products: the CRT5027 video timing and control chip, the COM5025 multiple-protocol universal synchronous receiver-transmitter, and the CRT8002 video-display-attributes controller.

It will also build floppy-disk and cassette-cartridge controller chips currently under development at SMC that the two firms hope to introduce jointly later this year. For its part, SMC can look at future n-channel products Solid State develops and expect to second-source as many as it gives SSS.

Where exactly Solid State will take n-MOS on its own is not yet clear. But Jay Litus, the firm's MOS marketing manager, alludes to one possibility: telecommunications. "We plan a definite entry into the telecom market, but we are waiting for the dust to settle," he says. "It's not clear which technology—n-, p-, or C-MOS—will be the best solution for those parts, but we'll feel a lot better having all three."

Since SSS already second-sources the 1800 family of C-MOS processors produced by RCA Corp. and Hughes Corp., will it pursue an n-channel microprocessor family? "It's a possibility," Litus says. □

1979: better forecast for semiconductors

While many sectors in the electronics marketplace are expecting a slowdown this year, that's not the case for the semiconductor companies. Buoyed by the strongest fourth quarter in their history, U. S. semiconductor companies are entering 1979 booked solid through the first quarter and most of the second, according to Thomas D. Hinkelman, executive director of the Semiconductor Industry Assocation.

"We look forward to a good 1979 based on a very strong first half, with the possibility of the year's growth being better than the 9% we previously forecast [*Electronics*, Oct. 12, 1978, p. 88], if the market remains strong through the third and fourth quarters this year," he says. Hinkelman explains that the SIA's 9% figure was made last fall when it assumed a softening in the middle two quarters, but "we now are looking at a softening, if it occurs, beginning sometime in the second half."

Preliminary 1978 tabulations show that total worldwide semiconductor sales of U. S. companies were $4.8 billion, up almost 25% over 1977. The total was paced by a $1.325 billion fourth quarter, up 29% over the same period in 1977. The U. S. market grew 20.4% to about $3.1 billion, and the international market by one third to $1.7 billion. Hinkelman notes, for example, that the Japanese market for U. S. stand-alone companies—those not selling to their own subsidiaries—grew 40%, but much of that was due to the dollar's decline against the yen.

Consumer

Bally computer uses plain language

Fearing that few people will actively want to program their home computers, the makers of these machines are turning to simpler software packages. But whereas many personal computers use some form of Basic, Bally Corp. is coming out with a custom language that uses words instead of letter-number combinations to make it seem friendlier.

Introduced at this month's Consumer Electronics Show in Las Vegas, the new language also has a more glamorous pedigree than most software, being an offshoot of the language used to create special computer effects in the movie "Star Wars." Called Grafix, the self-teaching, user-expandable language is to be a major feature of Bally's Level III home computer when it hits the market during the third quarter. The firm previously introduced a Level I computer that operates with read-only memory cartridges containing video games.

Creative. Basic's mnemonics and typical programming-like syntax, such as HLIN for horizontal line and VLIN for vertical line, could confuse potential users. Instead, the Level III program allows users to create graphics by using words like "circle" and "box," according to Robert Wiles, general manager of the Franklin Park, Ill., company's Consumer Products division.

When a user is uncertain how to specify a figure, its position, or its color, he or she can type in "help," and the computer will begin a sequence of directives that show the proper method.

Users add new words to the Grafix vocabulary simply by programming graphics subroutines and then naming them. In this way, the language can be expanded to the limits of available memory. At present, the system contains 32 kilobytes of read-only memory and 20 kilobytes of random-access memory, and provisions exist for adding memory accessories later, according to Wiles.

Grafix was developed by a team of programming engineers led by Tom DeFanti, professor of computer sciences at the University of Illinois, who created the software for "Star Wars." The language is loaded into Level III from a software cassette. Whereas Bally's Z80-based computer can interface to a black-and-white television set or monitor, it is best to attach it to a color set in order to make full use of its 256-color capability.

A Level III computer is built by adding the special programming keyboard and Grafix software to Bally's Level I video console. The $300 video console is available now, and the $650 keyboard and software cassettes will be ready during the summer, Wiles says. □

Computers

IBM introduces one-board computer

Although not unique in the marketplace, the new single-board Series/1 model 4952 computer unveiled ear-

Adac System 1000 handles a ton of I/O functions.

In its simplest form, the System 1000 functions as a low cost peripheral expander to minicomputers. When incorporating a DEC LSI-11 microcomputer, it acts as a stand-alone data acquisition and control system or as a remote intelligent terminal.

No other data acquisition system comes close to offering so many analog and digital input and output modules. Functional analog cards communicate directly with thermocouples, load cells, strain gauges, isolation amplifiers, transmitters and strip chart recorders to name a few. Discrete cards communicate with switch contacts, relays, thumb wheel switches, pumps, motors and many other devices.

A single System 1000 provides up to 700 high level analog input channels, or 128 analog low level input channels, or 700 digital I/O functions. For even greater capacity, a bus repeater card allows additional System 1000s to accommodate as many modules as desired.

System 1000 in the stand-alone configuration can be supplied with up to 32K of memory and DEC RT-11 software.

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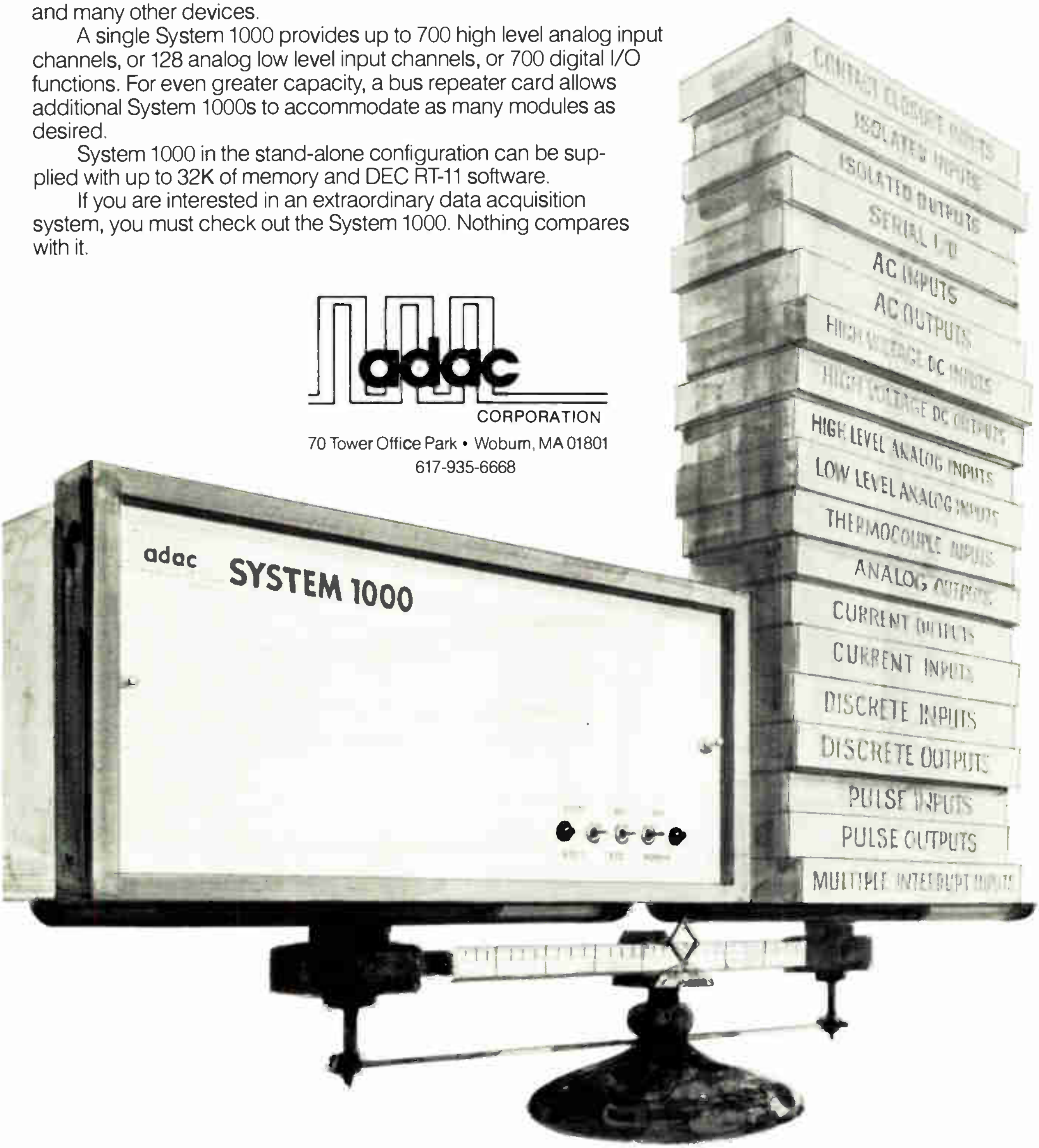

News briefs

Video disk players lining up

By the end of the year, consumers in some U. S. cities may have a choice of three video-disk players, now that RCA Corp. has announced it will enter the market and the U. S. Pioneer Electronics Corp. is readying its own player. They will join Magnavox Consumer Electronics Co., which began test marketing its Magnavision last month [*Electronics*, Dec. 21, 1978, p. 33]. Both firms should announce initial marketing plans around October. The simpler capacitive pickup technology involved means that RCA's Selectavision VideoDisc player will retail for around $400, some $300 less than Magnavision. Both Pioneer's and Magnavox's laser-pickup units are based on technology from Magnavox parent, Philips' Industries of Holland. As for selection, RCA says only that its initial catalog will contain 250 titles, ranging from feature movies to how-to shows. The entertainment conglomerate MCA Inc. is already out with an initial catalog of 200 Discovision titles that can be played on the Magnavision player and the forthcoming Pioneer unit. MCA has a Japanese joint venture with the Pioneer Electronics Corp. of Japan, which has just begun production of an industrial video-disk player [*Electronics*, Dec. 21, 1978, p. 55] that will be the basis of the U. S. Pioneer subsidiary's home player.

New products bow at winter consumer show

While the just-ended Winter Consumer Electronics Show in Las Vegas wasn't distinguished by exciting product announcements, some new devices were introduced. Texas Instruments Inc. showed the first vocabulary expansion of its speech-synthesizing learning aid, Speak & Spell. The $15 module, called Vowel Power, plugs into the rear of the unit. It stores 140 words in one 128-K read-only memory . . . Among microprocessor-based board games, Fidelity Electronics Ltd. showed a chess computer that narrates each move. Called the Model VCC Chess Challenger, it will retail for $325 upon availability in June and uses a multichip speech synthesizer . . . Also shown was an accessory for auto stereo receivers that transfers the music's vibrations to the lower back of the driver or passenger. Pioneer Electronics of America's Bodysonic is a cushion containing two proprietary moving coil transducers; it fits between one's back and the seat.

lier this month by IBM Corp.'s General Systems division is the latest sign that the industry giant is aggressively pursuing the minicomputer market.

It is also a continuation of the firm's recent memory price cutting [*Electronics*, Dec. 21, p. 38]: memory for the new unit has a dramatically low price of $450 per 32-kilobyte increment—equivalent to $14,400 per megabyte and although slower is about 89% less than the previous Series/1 memory price. That is much less than the $32,000 Hewlett-Packard charges per megabyte of minicomputer memory—the industry low till now—or the $2,200 Data General charges for 32-kilobyte increments for its new Nova 4 computer [*Electronics*, Jan. 4, 1979, p. 206].

Using new 36-K random-access metal-oxide-semiconductor memory chips made at the General Technology division, Burlington, Vt., IBM packs eight chips into a 1-inch-square module for a total of 32 kilobytes. With this density, the system's main memory of 128 kilobytes fits on the 4952's 7-by-9-in. board.

Fewer boards. The Atlanta, Ga., division's previous entry-level Series/1 model, the 4953, needs six boards and supports at most 64 kilobytes of main memory. The new 4952 processor with cabinet, power supply, and 32 kilobytes of memory sells for $4,600, some 14% less than a 4953 with comparable memory. But IBM notes that the 4952 offers only 80% the 4953's performance.

Although comparable in performance to the low end of competitive machines, IBM's Series/1 processor carries higher price tags—and no quantity discounts are offered. □

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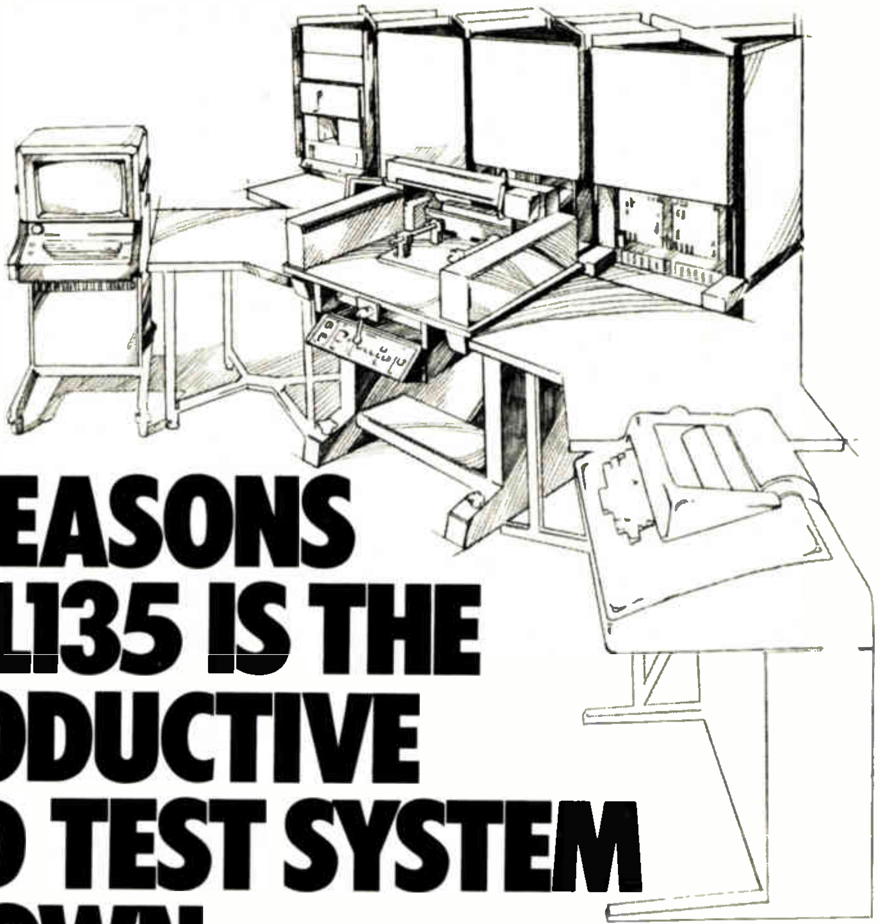

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2. The L135 makes fewer diagnostic probes – by an order of magnitude.

State-sensitive trace does it. Most LSI boards are loaded with multi-input LSI chips linked through "wired-and" bidirectional buses. These often require hundreds of diagnostic probes per fault. State-sensitive trace cuts the number dramatically.

3. The L135 produces immediate probe commands.

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4. The L135 mechanizes probing.

The M150 Automatic Prober does it. Seven to ten times faster than a human operator, the M150 speeds up board diagnosis even more because its operation is both error-free and fatigue-free.

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The L135 delivers the highest quality of testing, thereby slashing costs for diagnosis later at systems test and service out in the field.

5. The L135 emulates LSI-board operating environments.

5-MHz clock-rate testing does it. To ensure adequate board quality, you usually have to run LSI boards at clock rates as the last step in testing. Only the L135 provides test rates of up to 5-MHz, the speed of many microprocessors seen in today's products.

6. The L135 emulates and tests CPU sets.

Multiple drive/compare phase control does it. During clock-rate testing, the test system must first replace the CPU set and then test it at speed. The associated microprocessors usually receive multi-phase inputs and generate multi-phase outputs. The L135 provides the necessary, easy-to-program, precise phase controls over driver inputs and comparator strobing.

7. The L135 tests and diagnoses analog circuits.

Integrated ac-dc-parametric capability does it. The L135 offers many analog force-and-measure functions through matrix connections, all completely integrated into system hardware and software. If these capabilities aren't integrated into the test system, they must often be added to accommodate the increasing analog content of LSI boards. That prolongs test time and slows diagnosis considerably.

8. The L135 tests at dc and clock-rate on the same channel.

All-speed pin compatibility does it. In clock-rate testing, high-speed tests are usually applied on the same pins tested earlier with dc. The L135 allows you to apply both types of tests at the same system channel, eliminating the need for awkward switching or extra channel capacity.

9. The L135 has enough clock-rate channel capacity for the big jobs.

432 I/O pins does it. Big LSI boards have upwards of 250 edge-connector pins, all active. In addition, you need simultaneous access to dozens of internal test points and devices invisible to the edge connector. The L135 offers the highest clock-rate channel capacity, enough for all foreseeable LSI boards.

10. The L135 cuts total programming time.

The P400 Automatic Programming System does it.
The P400 automatically generates all the dc patterns and diagnostic data for the toughest part of most LSI boards: the jungle of random digital logic, as well as those portions containing modeled LSI devices. Total programming time is shorter. The best of the so-called "automated test generation" techniques offered by other systems still require manual pattern-writing. That takes longer and costs much more.

The L135 cuts the time needed to get products into the production line and out to the market place.

11. The L135 cuts system time for debugging.

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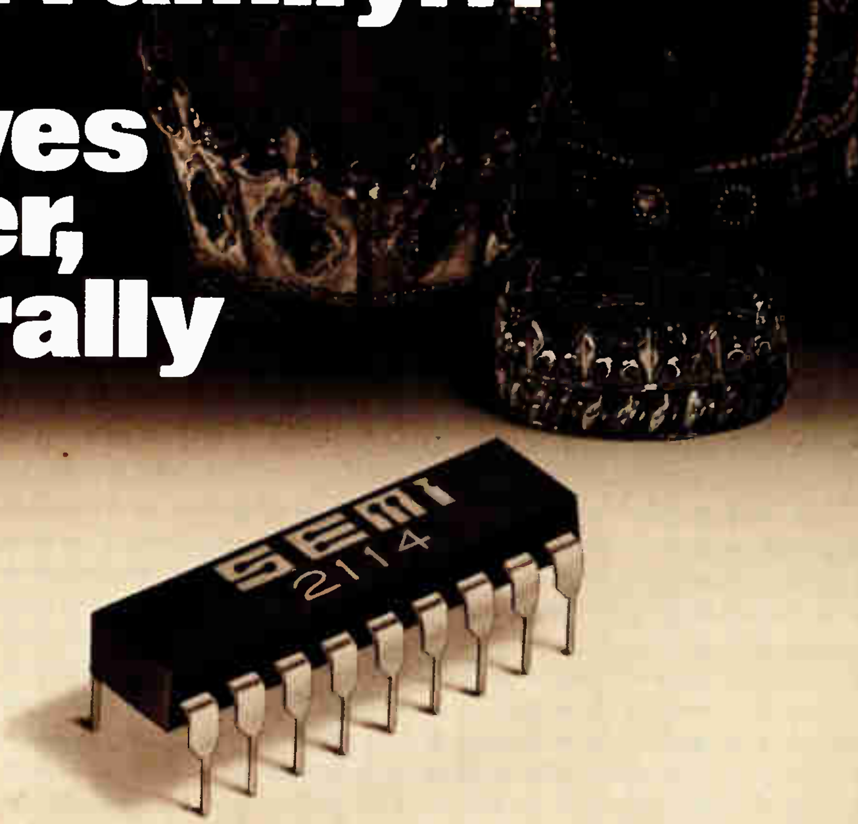

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Washington newsletter

Nippon Electric wins SBS award for five Domsat terminals

Japan's **Nippon Electric Co. has made a major advance into the U.S. domestic satellite earth station market** by winning a contract for five rf terminals to be used in the 12-to-14-GHz tracking, telemetry, and command network of Satellite Business Systems Inc. The dollar value of the award was not disclosed. SBS, the jointly owned venture of Comsat, IBM, and Aetna Casualty & Life, is scheduled to begin operations in 1981, with two digital satellites to be launched into geosynchronous orbit late next year. Two terminals, each with two 7.6-m, limited-motion antennas and a 12.5-m, fully steerable antenna, will be installed by NEC next year at the SBS's Castle Rock, Colo., beacon station. Two other terminals, with limited-motion antenna terminals only and associated electronics, will be used at a control station near SBS headquarters in McLean, Va., outside Washington, D. C.

Solar power satellites to cost $12 billion each . . .

The Department of Energy's first in-depth study of solar power satellites, to be issued before month's end, estimates it will cost up to $12 billion to build and orbit each system if two are launched per year. The study draws heavily on National Aeronautics and Space Administration data using satellite models capable of delivering 5-GW net power output on the ground, about four times the capacity of the average public utility power plant [*Electronics*, April 27, 1978, pp. 60, 96]. **However, that estimate "could move up or down by a considerable amount,"** says Jerry Grey, public administrator for the American Institute of Aeronautics and Astronautics. The AIAA, in a new position paper, says it favors a $30 million annual effort over five years in ground-based research before any development or demonstrations are undertaken.

. . . as NASA seeks frequency for the craft

The National Aeronautics and Space Administration is sparking a domestic and international controversy by asking that a solar power satellite transmission frequency be set aside for future use. For one, the Federal Communications Commission has not yet developed a position on the issue for the U.S. negotiating team for the World Administrative Radio Conference that convenes later this year in Geneva. For another, **Britain and a number of less developed nations reportedly oppose NASA strongly on the allocation** in view of the incomplete studies on possible ionospheric heating and related environmental concerns. The favored solar satellite frequency for microwave transmission of solar electric power to a large earth rectifying antenna **is 2.45 GHz, midpoint of the 100-MHz-wide band** used for industrial, scientific, and medical purposes.

Addenda

Equipment market potential for Message Toll and Wide Area Telephone Services, known as MTS and WATS, was significantly expanded early this month with the Federal Communications Commission's decision to let an International Telephone & Telegraph Co. subsidiary, ITT Corporate Communications Services, into the competitive fray. The firm is expected to provide stiff competition for AT&T. . . But AT&T won another battle when the FCC **refused to force it to make advance disclosure of its plans for use of the Comstar domestic satellite** that it shares with CTE Satellite Corp. A three-year moratorium on AT&T's offering of non-Government private-line service on Comstar expires July 23.

Washington commentary

AT&T throws the book at the Government

The American Telephone & Telegraph Co. has literally thrown a book at the Justice Department's antitrust charges against the communications giant. If you count the book's 38-page index, it is a hefty 552-page rebuttal of monopoly charges that comes on at least as strong as the Government's detailed charges late last year [*Electronics*, Nov. 23, 1978, p. 98]. Like International Business Machines Corp., AT&T is fighting mad and makes clear it intends to do battle with the Government in the courts with an army of lawyers equipped with an endless supply of documentation.

Bigness by itself is neither bad nor evidence of monopoly, says AT&T in its "defendants' first statement of contentions and proof" filed in mid-January with the District of Columbia's U. S. district court. Moreover, bigness is virtually mandated by telecommunications technology and its need for a large and "complex, interdependent switched network" to guarantee efficient operation and reliable parts. These are "fundamental industry principles" not considered by the Justice Department, AT&T adds.

Regulation precludes monopoly

Also ignored, in AT&T's view, is the fact that the Bell System is regulated by the Federal Communications Commission and its state counterparts who control market entry and set rates. Under the applicable regulatory statutes, "the Bell System cannot be held to have control over entry or prices in any market as a matter of law," AT&T asserts, although the Government must prove the opposite in order to show monopoly power.

AT&T's lawyers also call on economist Alfred Kahn, now chairman of the President's Council on Wage and Price Stability, to rebut the Government's demand that the corporation divest itself of equipment manufacturer Western Electric Co. Citing a 1976 FCC judgment opposing a Western Electric spinoff at that time, AT&T quotes a statement by the then-chairman of the New York Public Service Commission that divestment would be "a plunge into the unknown" that might prove economically unwise and undesirable. Such integration is critical to successful operation of its network, AT&T claims, adding "it cannot be maintained if the telecommunications industry is balkanized, as the Government insists it should be." That wording—indicating that the phrases "telecommunications industry" and "Bell System network" are interchangeable—is puzzling a number of industry executives who note that AT&T's filing elsewhere cites the existence of 1,600 U. S. telephone companies as evidence that it is not a monopolist.

One long-time AT&T competitor attributes such slips in the filing to "hysteria" on the company's part and in support of that claim cites the filing's final statement: "There is and can be no justification for such wanton destruction of a valuable national asset, and, for that reason alone, there is and can be no justification for the remedy sought by the Government here. The Government's request that the Bell System should be fragmented should, therefore, be rejected for reasons independent of the court's views with respect to the merit of the Government's charges." That is translated by the competitor to read that the Bell System "is above and beyond the reach of the law."

Unfair competition

What bugs AT&T at least as much is the issue of competition, which it refers to throughout as "cream-skimming" of its most profitable markets in a way that imposes "increased communications costs upon the American public." Increasingly pro-competitive regulatory rulings have put Bell in the "untenable position" of adjusting services and rates to respond to competition in selected fields, the company charges, "without in any way modifying Bell's common-carrier obligation to serve all classes of customers with all types of services." The Government, it says, has overlooked that issue, too. It is competitors, the defendants argue, who have manipulated the regulatory process "at the expense of Bell and the public."

On the hardware side, AT&T totally rejects charges that it foreclosed competition with Western Electric Co. by refusing to let operating companies buy technologically superior and sometimes cheaper products from industry. Citing the Government's charge that its first large electronic switching system, the No. 1 ESS, was "an expensive failure" and that IBM might have built it faster and better, AT&T angrily replies that it undertook electronic switching research and development in 1954, years before IBM approached it in 1961, and that the No. 1 ESS "is almost without exception recognized by the scientific and business communities as a monumental technological achievement." Moreover, all the Government's statements about IBM "are inaccurate," AT&T says, asserting that IBM at that time had "almost no know-how or experience in real-time data processing, which is essential in telephone switching," a fact IBM personnel are said to have acknowledged.

Ray Connolly

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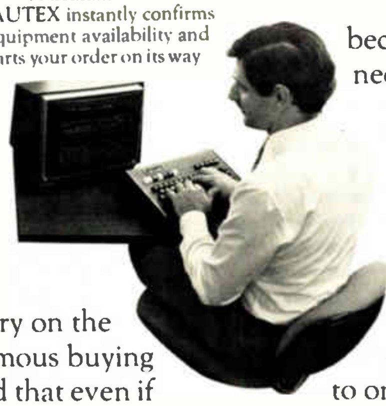

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International newsletter

Japanese tab $235 million for software, peripherals

With the government-supported VLSI program to begin its last fiscal year in April 1979, the Japanese cabinet is bringing its scheme for sharing the cost of research and development to a different sector of the electronics industries. It has approved a $235 million, five-year plan in which mainframe manufacturers would develop basic software for the next generation of computers and would also join with peripheral makers to develop new peripherals [*Electronics*, Oct. 26, 1978, p. 63]. The government would cover half the cost, the companies the other half. If approved by the Japanese parliament, the budget for the first year will be $17 million, with the government supplying half.

West German satellite would beam TV into homes

Under a $3 million contract from Bonn's Ministry for Research and Technology, a consortium of West German aerospace and electronics firms has worked out a detailed concept for a nationally operated television satellite that would beam TV programs directly to peoples' homes. According to consortium leader Messerschmitt-Bolkow-Blohm GmbH, **the satellite could be readied by the end of 1982 and operational a year later.** It would send out three TV programs initially, an additional two by 1986. Participating in the concept phase were aerospace firms Dornier System and Erno GmbH and electronics companies AEG-Telefunken and ITT subsidiary Standard Elektrik Lorenz AG.

Israel lands aircraft deal with Australia . . .

Israel Aircraft Industries, the government-owned conglomerate that includes seven electronics companies, has worked out agreements in principle worth tens of millions of dollars with Australia. The deal involves refitting and renovation of the Australian air force's 300 U. S.-made Skyhawk and French-made Mirage warplanes. **IAI will install sophisticated systems to make the planes flight-worthy well into the 1980s.** Also, IAI will sell technology to Australian firms as well as a Westind executive jet specially fitted for naval reconnaissance.

. . . and gets a shot at Pentagon deals

Israeli sources say that the Pentagon may soon cancel all limitations preventing Israeli firms from participating in its public tenders. If it does, and the Carter Administration gives final approval, Israeli firms will be allowed to bid on equal footing with American companies for Pentagon contracts. At present, **Israeli firms can be awarded contracts only if their proposals are at least 40% below those of American firms.** Also, a minimum percentage of U. S. parts must now be used. Most likely to benefit are the country's electronics firms, which comprise Israel's second largest export sector: Elta, subsidiary of government-owned Israel Aircraft Industries, Elbit Co., Tadiran Co., Astro Co., and AEL Electronics Co. Exports are expected to increase $50 million to $60 million the first year and thereafter by even more. The Department of Defense had no comment.

Ferranti, Sperry to build laser-gyro for UK aircraft

The UK Ministry of Defence has awarded two three-year contracts to develop a laser-gyro inertial navigation system for combat aircraft to Ferranti Ltd., Edinburgh, and Sperry Gyroscope, Bracknell, a division of Sperry Rand Ltd. Sperry says it delivered a British-designed and -built laser gyro to the Royal Aircraft Establishment, Farnborough, back in 1976. Both laser gyros have a three-legged triangular pathway, formed by drilling a temperature-stable vitreous ceramic block that accommodates the lasing helium gas-neon gas, reflecting mirrors, and interference fringe detectors. Last month, Boeing Commercial Airplane Co. awarded the first civil contract for such a system to Honeywell Inc. [*Electronics*, Dec. 21, 1978, p. 36].

Swedish cop cops fine for copping data on ex-cop

The first culprit to be prosecuted under Sweden's data law, which sets strict regulations on the use of data banks, is a policeman. The perpetrator used a terminal in his police station to access data about a former policeman from **the central data bank, which holds data on 400,000 individuals—5% of Sweden's population.** The ex-cop had been much in the news after publicly admitting having seen police beat up some youths, so the data thief posted personal information about him on the station bulletin board. The victim complained to the data inspection board, and a court fined the policeman 40 days' pay.

Automated information, please

The telecommunications directorate of the French post office plans to start trials of an automated telephone directory in early 1981. In the Ille-et-Vilaine department in northwest France, subscribers will get special handsets having an alphanumeric readout and keypad. **Dialing information will access a computer-based directory on which they will punch in their requests.** The PTT says that handset suppliers have projected that a directory terminal that would also serve as a telephone could be mass-produced for less than $100; a prototype will be on display at the audio-visual and communication exhibition in Paris, Jan. 22 to 27.

Philips coming up contracts all over

The way Philips Telecommunicatie Industrie BV in the Netherlands has been picking up contracts, they might be growing on trees. **The firm has received a $29 million order for the traffic control system of Mexico** City, including a central control system of several computers, 25 computerized substations, several thousand traffic detectors, and 1,000 electronic crossing controls. Philips is also working with SIRTI, a unit of the Italian telecommunications group STET, to upgrade a 1,400-km 12-MHz backbone trunk route in Saudi Arabia by adding a 60-MHz link. The $40 million link between Taif, in the southwest of the country, and Damman on the Arabian Gulf, will be the first 60-MHz trunk for combined telephone and color TV transmission, Philips claims. And in Norway, Philips will use 18-MHz hardware to upgrade an existing 4-MHz line.

Addenda

ITT's Semiconductors Group plans to have samples of its 64-K RAM by mid-1979 from its Footscray, Kent, plant. Footscray will be the subject of a $20 million development program with $4 million to come from the UK government. . . . French TV-makers' trade association SCART has worked out specifications for a **20-pin connector for linking household sets to external systems like videotext and TV games.** The connector, which provides stereo and monaural audio, composite and red-green-blue video, remote control, and clock functions, could turn up late this year on French-made sets. . . . **General Instrument Corp. is eyeing Plessey Ltd.'s semiconductor operations** with a view to purchase either outright or as a joint venture. GEC Ltd. has already made an offer of purchase.

Solid-state approach to electrochromic displays holds promise

Chemical reaction produces color change in new ceramic material; passive display can be read in bright sunlight

Most research into electrochromics has aimed at liquid displays, but this once-promising technology has "hit long-term chemical degradation problems that appear to have no solution," according to Mino Green, who heads up work on alternative, solid-state electrochromic displays at London's Imperial College. Now a solid-state technology looks set to steal the limelight, thanks to the development of a new class of ceramic compounds—called super-ionic conductors—and a broad, interdisciplinary attack on the subject.

Work with test cells has been encouraging, and, says Green, the first experimental solid-state electrochromic display, in which deep-blue seven-segment numeric characters will be chemically formed on a white ceramic background, could be working within twelve months at the Imperial College Department of Electrical Engineering.

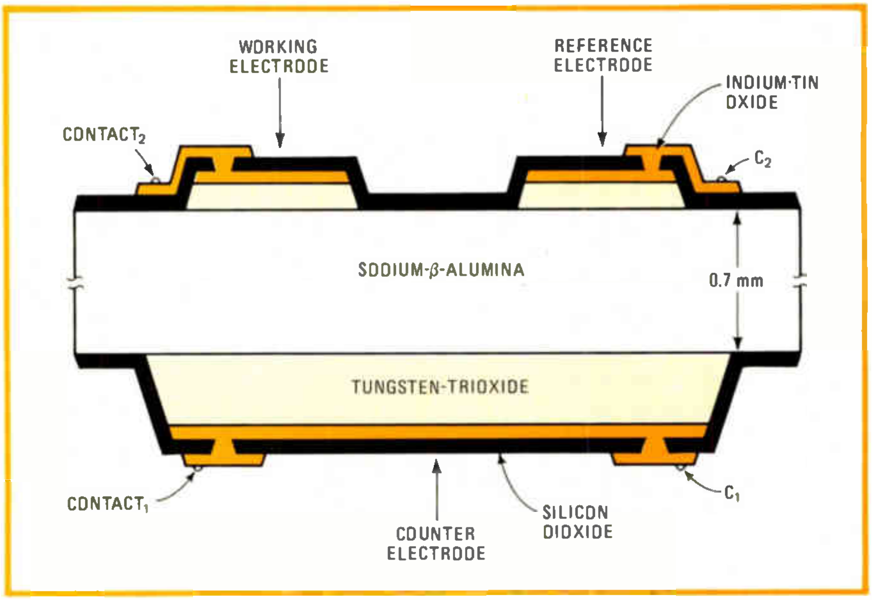
Unlike other technologies, the electrochromic display operates by producing a chemical color change. "We are shifting atoms around and not electrons," says Green. Consequently the displays are passive and cannot be washed out by bright sunlight, as are light-emitting diode displays. This factor, plus an "aesthetically pleasing appearance," may make them useful in such applications as car dashboards, he adds. In addition, they only consume power during read-write operations.

Starting point for the solid-state electrochromic display is a new class of ceramics developed initially for use in high-energy-density sodium-sulphur batteries. Called super-ionic conductors, these hot-pressed ceramics are used in batteries to separate the reactants while at the same time supporting a current flow between them by the motion of sodium ions through the separator wall. Ceramic is ideal in the battery because it is chemically inert, and that is what makes it so attractive for electrochromic displays.

Test cell. In his first-generation display, Green uses a sodium-alumina substrate in which sodium ions support an electric current. The chromic compound is tungsten trioxide. This normally colorless compound can absorb sodium ions, and as it does so, it turns a deepening blue. "A complete 'gray scale' is possible" says Green.

An electrochromic cell is formed by radio-frequency sputtering a 1-to-3-micrometer-thick tungsten trioxide layer onto the top and bottom surfaces of the ceramic substrate. Connection to the chromic surface electrode is made through an indium-tin-oxide layer sputtered onto the surface which yields a transparent conductive coating and assures uniform coloration.

The display is written into by applying a negative-bias voltage between the display-surface working electrode and the counterelectrode. The resulting current flow transfers sodium ions from the ceramic substrate into the tungsten trioxide layer, where they are chemically absorbed, causing a deepening color



Bright future. Test cell produces blue display on white background. Colorless tungsten trioxide darkens as it absorbs sodium ions from sodium-alumina substrate.

change as the charge flow continues. "It's a lovely contrast, dark blue against white" comments Green. The process is reversible, and there are no long-term degradation effects if the display is not overdriven.

Some like it hot. Work on first test cells has produced attractive display qualities, but has also pointed up problems common to many chemical reactions. In particular, the read/write time is extremely temperature-sensitive and can vary from 1 second at room temperature to 1/10 a second at 55°C. "One nice thing about these displays is that they like to be hot," comments Green. But like liquid-crystal displays, at 0°C "they will take a hell of a long time to operate."

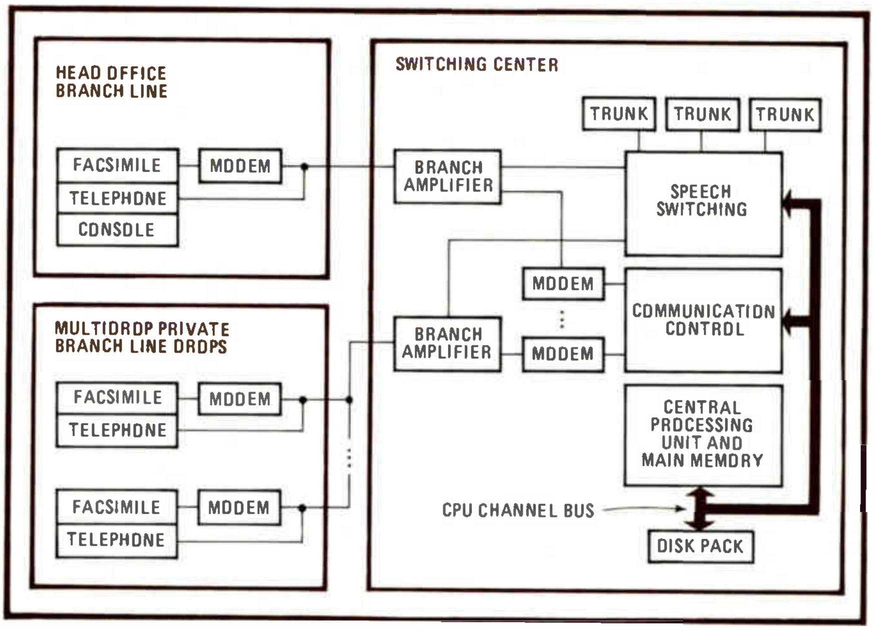
This problem can be overcome by keeping the display warm, which would require 0.1 watt per square centimeter, for a read/write time of 0.1 second, according to Green. Where power is scarce the display could be pulse-heated during the read/write cycle. In terms of power consumption, this puts the technology between the LCD and the LED display.

Improved materials could further reduce the temperature dependence. In particular, says Green, lithium fast-ion conductors are much less temperature-dependent. But to get a small display—rather than just a test cell—working within the next 12 months, Green has now frozen the technology to produce a fully characterized device. At the same time work will progress on second-generation technologies. □

Japan

Facsimile and voice system links offices

Electronic mail service may be only a gleam in U. S. Postmaster General Bill Bolger's eye, but in Japan one private system is already proving its economy. Installed by Nippon Electric Co. at the main headquarters and branch offices of Nikko Securities Co., one of Japan's Big Four securities firms, it links 130 digital facsimile terminals on leased telephone lines.



Send or save. Electronic mail system transmits messages instantly and carries phone service on idle circuits. If circuits are busy, disk pack at switching center can store up to a day's documents for later forwarding. Trunks generate dial tone and ring and busy signals.

Not only does the system transmit messages instantaneously at lower cost than mail or teletypewriter services, but it also can support telephone service on idle circuits and broadcast urgent messages through speakers at each office in the system by preempting normal service.

Heart of the system is a NEAX-51 integrated electronic exchange that switches both speech and data. Right now one exchange is being used in a star network because most messages originate at headquarters in Tokyo. More terminals will be added as needed; the system can support as many as 1,000.

Storage and forwarding. Four 100-megabyte disk packs enable the exchange to store all data messages sent during one day. Thus when circuits are busy, the operator at the system center can process low-priority documents for forwarding when circuits become free. The storage also allows repeats to be sent when needed.

Although the system has 130 terminals, there are only 22 multidrop branch lines. Since one terminal is connected to each drop, the branches are similar to party lines, but with the important difference that the system center can send documents to all terminals or any combination of terminals simultaneously or to any individual terminal. Also, cost is an order of magnitude lower than a previous system that had an individual circuit for each terminal.

Terminals. NEC's Nefax-6000 digital facsimile terminals have separate transmitters and receivers with a resolution of eight lines per millimeter. Redundancy reduction circuits enable the terminals to transmit a standard letter-size page of text with this high resolution in less than a minute at a data rate of 4,800 bits per second. However, oversize pages of closely spaced fine print giving stock prices take up to several minutes. An average page of text contains about 50,000 bytes of data, so that one 100-megabyte disk can store about 1,000 documents.

The transmitter uses a charge-coupled-device sensor with discrete photodiodes to scan the copy. Two adjacent scanning lines are stored in a 4-kilobit memory for the system's two-line batch-mode run-length coding.

This coding scheme processes the

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information for all points along two lines. It then transmits the type of transition from point to point (from black to white or vice versa), as well as the run length from one transition to the next. Because two adjacent lines on a page generally have a very high correlation, processing two lines together greatly reduces the redundancy of transmitted information.

At the receiver, the signal is decoded to give a replica of the pattern on each line and is electrostatically printed on coated paper by means of a multiwire stylus.

Both the transmitting and receiving terminals use 8085 microprocessors for input/output control and automatic self-diagnostic functions. The transmitter console includes a 10-key pad for selecting destinations, various function switches including selection of facsimile or phone, and a journal printer for confirming input information and certifying addresses. Among the microprocessor's functions in the receiver is generation of patterns for message serial number and time of reception.

Studies by NEC compare the cost of running the service with that of postage for special delivery, which is normalized as 100. On this basis, the facsimile system operating cost, including paper and power, is about 5, and the cost for direct labor is also 5. When more than 1,000 messages a day are sent, the sum of these two costs exceeds fixed costs, which are system depreciation and line charges, and total cost per message is less than 20, or less than a fifth the cost of sending a special delivery letter. □

West Germany

Technique screens resistors and conductors directly onto printed-circuit substrates

Efforts to build higher-density printed-circuit boards at lower cost have paid off in a new production technology at West Germany's Preh-Werke. By allowing direct silk-screening of resistors and conductors onto phenolic or epoxy laminates or heat-resistant thermoplastic, the technique yields higher component density than conventional pc boards, as well as a cost advantage over film circuits on ceramic or foil substrates.

Using the Seri-additive technique, which derives its name from serigraphy, or silk screening, multilayer arrangements and crossovers on both substrate sides can be produced as well as plated-through holes. Resistors can be made in a wide resistivity range—from 10 ohms to more than 2 megohms per square—and can be laser-trimmed to within ±1% of any chosen value. The temperature coefficient of these resistors depends on the resistance of the paste used. It ranges from 0 to −300 parts per million/per °C for values of less than 10 kilohms per square and from 0 to −800 ppm/°C for values greater than 10 kilohms per square.

Since the minimum line width is 0.3 millimeter, the main application will be in consumer electronics. Preh has made samples of Seri-additive circuits for customers in the entertainment electronics industry. Large-volume production will get under way this year, says Wolf-Erhard Steigerwald, senior vice president and inventor of the technology.

Benefits. The cost and density advantages over pc boards stem from silk-screening the fixed resistors right into the circuit, explains Steigerwald. Not only does this increase component density, but it also eliminates the need for manual or automatic component insertion and cuts labor and device costs. The cost benefits vary with the application, he notes. "But generally, a Seri-additive circuit with a number of fixed resistors screened into it costs no more than a pc board of the same size without fixed resistors."

Fabrication technologists the world over have been pursuing similar goals. Among the most noteworthy rival techniques devised so far is the U. S.-developed polymer thick-film (PTF) method [*Electronics*, April 27, 1978, p. 114]. It uses a polymer and carbon paste for resistors and a polymer and silver paste for the conductors.

PTF has some problems, though, not the least of which is that conductors made of the PTF paste do not readily take to solder. The new technique achieves good solderability by selectively coating the conductors with a metal layer, preferably copper, in a galvanic- or chemical-deposition process. Only conductors to be exposed to tin in the solder bath need be so coated.

PTF may also develop cracks at the interface between resistor and conductor, a result of the different expansion coefficients of the materials used. But the same polymer material is used for resistors and conductors in Seri-additive, so cracks and breaks will not form.

Another problem with PTF is that conductors often suffer from silver migration. This is prevented in the new technique by covering specific areas with a special resist layer and by using a special thermoplastic.

The proprietary thermoplastic substrate is nonflammable and resistant to temperatures well above 300°C. It does not warp or buckle even after several times through a solder bath. And Steigerwald claims a cost advantage over epoxy-laminate substrates as well.

Making conductors. There are three ways to fabricate conductors in the Seri-additive technique. The first is to screen on a polymer and silver paste. Conductors using this compound become conductive right after the curing process. Areas to be soldered are selectively covered with a copper or nickel layer, and all other areas are coated with a resist layer to prevent silver migration.

In the second method, both the conductors and resistors are screened on with a polymer paste. Areas that are to serve as resistors are masked with a galvanic resist, whereas the conducting areas have a layer of copper or nickel galvanically or chemically deposited on them;

masking with a solder-stop resist ensures that only the desired conductor areas accept tin on passing through the solder bath.

Conductors are made of a polymer and metal-oxide paste in the third method. After screening and curing, they undergo a galvanic or chemical process that deposits copper or nickel layers selectively on them. These layers make the conductors electrically conducting and at the same time solderable. In all three methods the curing process takes place at 220° to 250°C. □

Canada

Feed-forward amp stretches TV link

At 145 miles, the new coaxial cable television transmission system linking the capital of Canada's Manitoba province with four rural communities is the world's longest. What's more, the use of new low-distortion amplifiers yields a signal-to-noise ratio of more than 50 decibels—performance equal to that of present systems, which run to 30 miles.

The system is expandable to 225 miles and carries eight channels in the forward direction and four in the reverse. "It's all made possible by feed-forward distortion cancellation in the repeater amplifiers," says Jeffrey Rohne, a design specialist for Manitoba Telephone System, which installed the cable.

"Until now," he continues, "conventional cable TV was limited to about 30 miles by the buildup of noise and distortion in the cascaded amplifiers. We expect our amplitude-modulated vestigial-sideband transmission to be able to handle several hundred miles if we go to frequency modulation."

Not new. The amplifier, built by Century III Electronics of Vancouver, British Columbia, uses a phase-distortion cancellation principle that is actually older than the commonly used negative feedback idea. Though it has been tested for several years, it is only now coming into system use.

"It is just because negative feedback is so common that the feed-forward concept has been neglected," Rohne says. Moreover, it was not possible until recently to get the needed well-matched integrated-circuit amplifier chips. And, according to Ronald Solomon, engineering manager at Century III, the firm's delay lines use lumped inductance-capacitance circuits instead of coaxial delays—a far more practical approach for shaped delay.

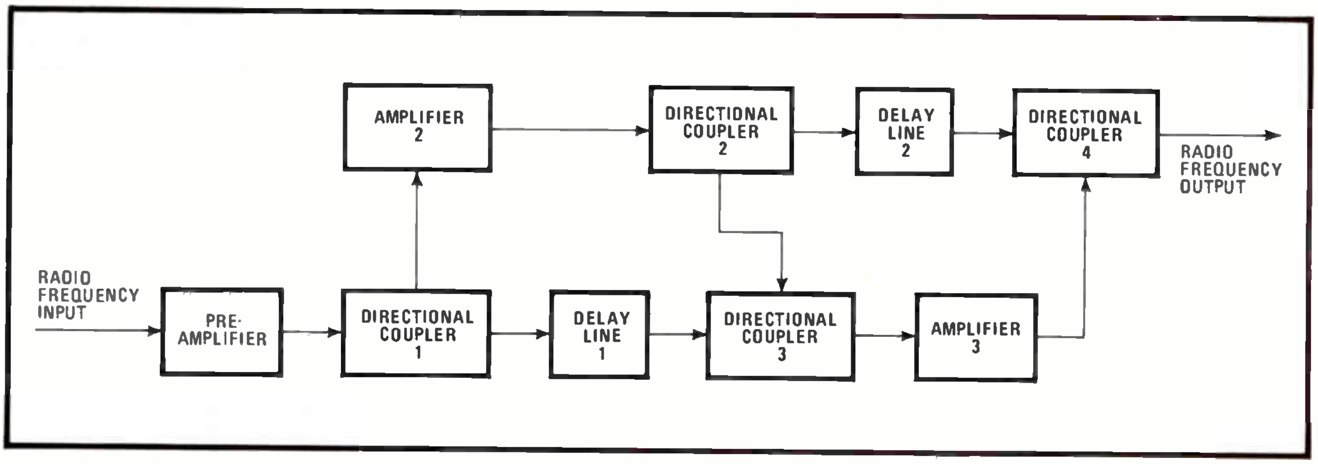
A typical feed-forward amplifier (see figure) consists of a preamplifier, two regular amplifiers, two delay lines, and four directional couplers. In operation, a small portion of the distortion is first extracted from the output of main amplifier 2 by subtracting the input signal after a suitable delay through delay line 1. The extracted error signal at the output of directional coupler 3 is then amplified by error amplifier 3 and combined through directional coupler 4 in opposite phase with the main amplifier output signal.

Cancellation of most of the main amplifier distortion results, allowing the user to run the amplifiers at high gain levels to go greater distances. And many amplifiers can be used before the quality of the signal falls below cable TV standards.

"The key to the feed-forward design is the recognition that the amplitudes and phases of the signals on the upper and lower paths of each stage need to be perfectly matched," Rohne says. If this is done successfully, from 20- to 30-dB improvement in distortion performance can be realized in comparison with conventional cable TV amplifiers.

Check on it. The operational status of each amplifier is monitored by a microprocessor that can be interrogated from a central control. Both failure and degradation as well as maintenance functions can be supervised from a central video-display circuit with hard-copy output and keyboard instruction entry.

Ultimately, the system will deliver high-speed data, teleconferencing, medical and educational television, and telephony. A fiber-optics system could also offer these services, but, Rohne notes, "our cable system is up and in service this year—meeting customer requirements which cannot wait for optical technology." □



Low distortion. To minimize phase distortion in a feed-forward amplifier, the delay lines and amplifier chips must be matched perfectly. Depending on configuration and system specification, the preamplifier can be made as a feed-forward amplifier to boost performance.

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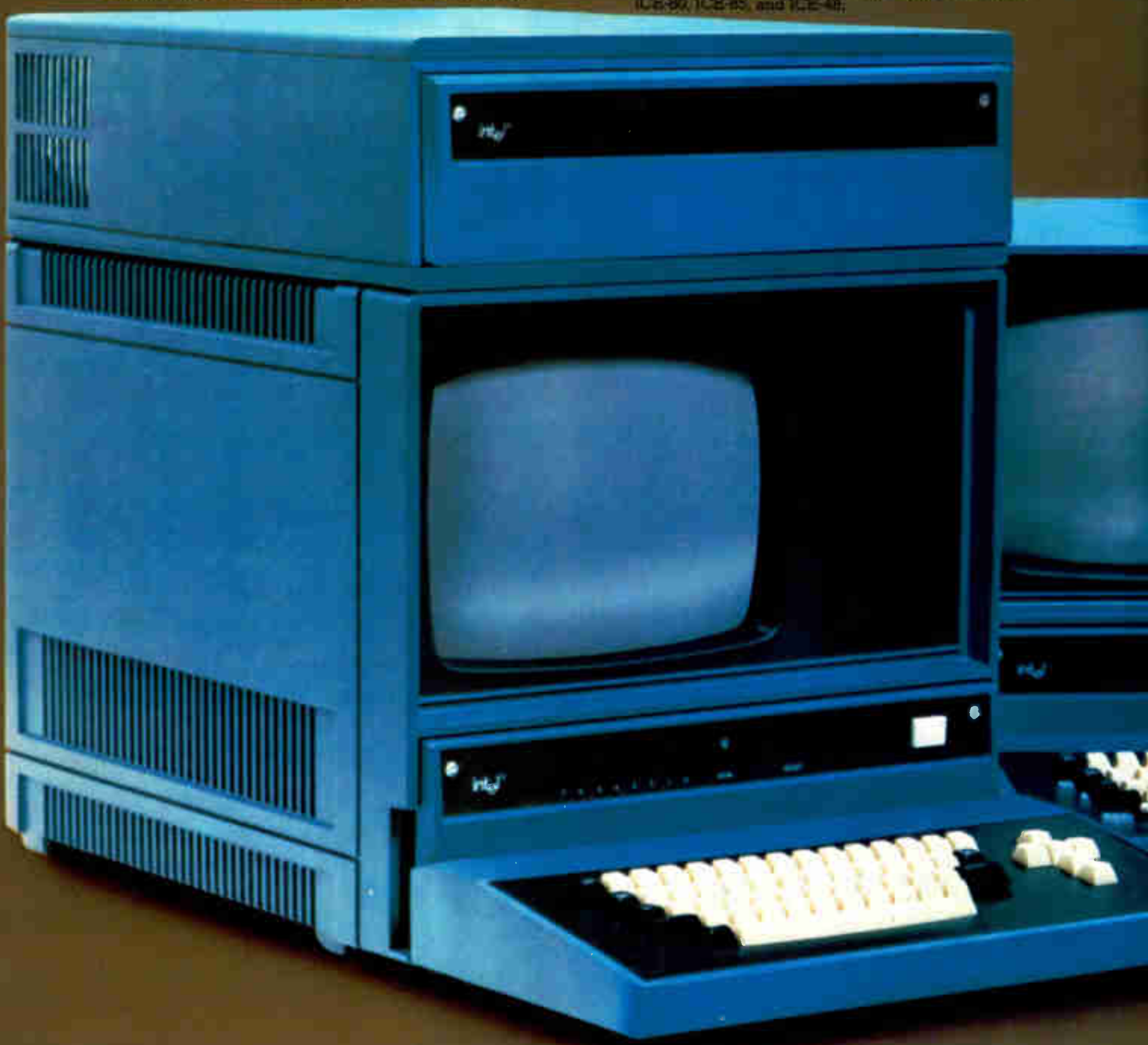

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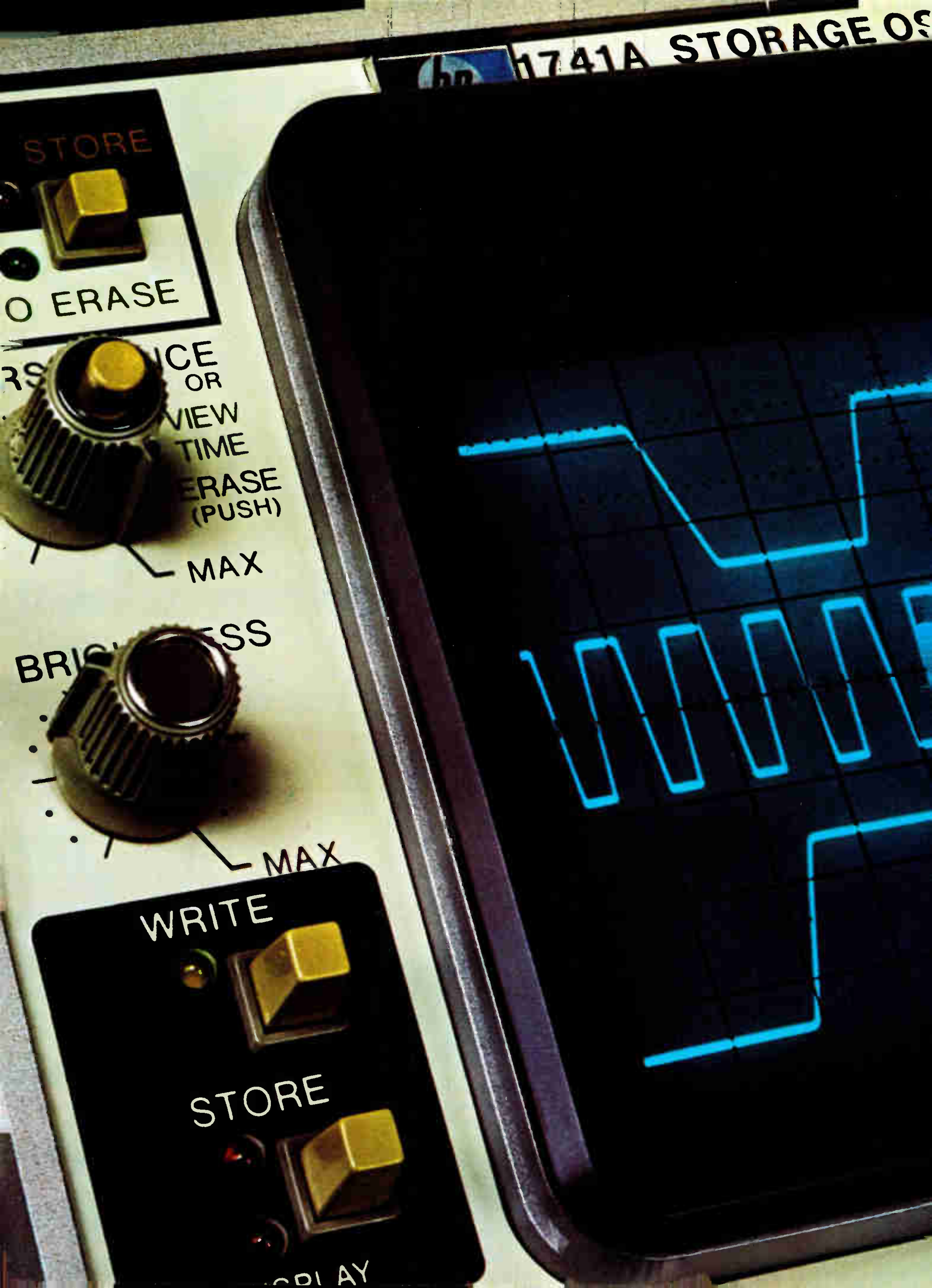
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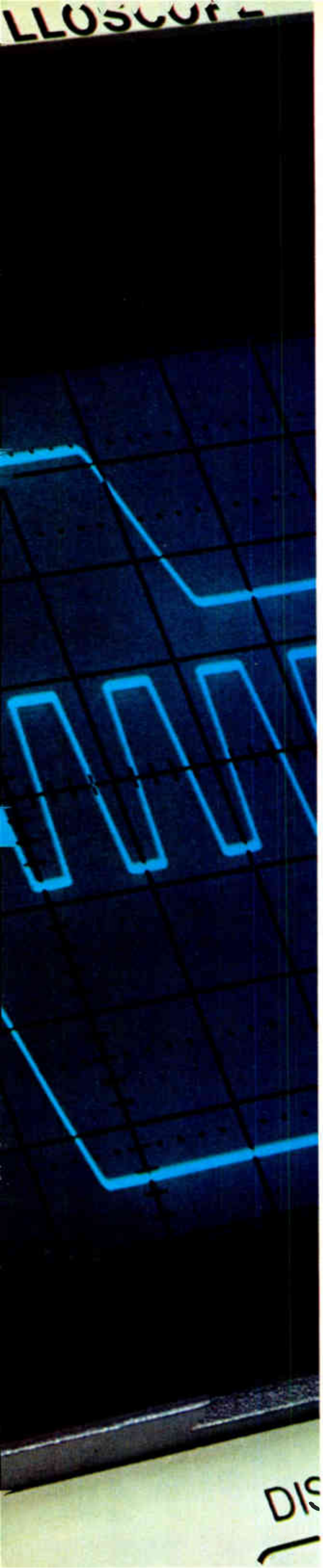

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Circle 77 on reader service card

Hot time in store for ICs

Demand for integrated circuits that can function at 250°C to 350°C in industrial and commercial applications spurs research

by Nicolas Mokhoff, Components Editor

Demand is rising in the industrial and commercial world for integrated circuits that can do their jobs in the 250°C to 350°C range, and researchers are working hard to supply them.

While it has been common practice for some time to design with ICs capable of functioning over the full military temperature range of −55°C to +125°C, those chips generally have been wrapped in protective subsystems or systems. But new applications go beyond that. For example, a designer might want to put an operational amplifier IC in a sensor package to be placed on an automobile's exhaust pipe to monitor exhaust fumes, or a microcomputer might have to live smack in the middle of an airplane jet engine to regulate engine speed, fuel flow, and actuators.

The state of the art has not yet arrived at that point, but judging from the progress being made it will not take much longer. "We're into our second year of a full-fledged program to develop and demonstrate a high-temperature electronic technology," says L. J. Palkuti of the Naval Research Laboratory in Washington, D. C. "Our primary aim is to satisfy the requirements of uncooled electronics mounted on aircraft engines."

At present, to maintain semiconductor devices at a safe 125°C ambient temperature, electronic packages are cooled by interfacing the engine fuel with the components' heat sinks. "Eliminating the cooling can save up to 20% in life-cycle costs as well as improve reliability and reduce system weight," says Palkuti.

He emphasizes that the program mandates the running of existing commercial ICs at the higher 200°C temperatures. Once this proves possible, it calls for minimum design changes and minor process modifications to extend their temperature range to 300°C.

"The program consists of six tasks, the first of which has just been awarded as a contract to General Electric Co. in Evendale, Ohio," he explains. "They are to identify present state-of-art feasibility for a high-temp technology and recommend the ICs and the minimum modifications needed to make them work. Whether high-speed bipolar, complementary-metal-oxide-semiconductor on sapphire, or even integrated injection logic will come up as a sure winner is hard to tell at this moment."

Following the completion, open bids will go out to commercial IC manufacturers, as well as system houses, to redesign large-scale ICs for operation at high temperatures. Some nine months away, this task will concentrate on devices like the 2901 4-bit slice microprocessor, 1-K and 4-K random-access and read-only memories, op amps, 12-bit analog-to-digital converters, power amplifiers and power supplies, as well as a slew of passive components.

Also, the Naval Research Laboratory is conducting an in-house investigation into possible contenders. So far, the only thing Palkuti is sure of is that aluminum-metalized devices will not do the job at 300°C.

While melting is not a problem, "you need refractory metalization systems using high-quality elements like titanium, tungsten, platinum, and gold," he says. "Our preliminary results for 300°C burn-in tests on diodes, MOS field-effect transistors, and junction FETs have shown that the best mean time between failures achievable with aluminum-metalized devices is between 10^3 and 10^4

HA-2600 OPERATIONAL-AMPLIFIER PERFORMANCE

	−55° to 125°C	25°C measured value	200°C measured value
Input offset voltage	6 mV	1.2 mV	1.9 mV
Input bias current	30 nA	6.5 nA	100 nA
Voltage gain	70 K	166 K	180 K
Common-mode rejection ratio	80 dB	92 dB	86 dB
Positive-power-supply rejection ratio	80 dB	100 dB	90 dB
Negative-power-supply rejection ratio	80 dB	102 dB	91 dB
Supply current	3.7 mA	2 mA	3.6 mA

SOURCE: HARRIS SEMICONDUCTOR

hours—and that falls short of our reliability goals of 300°C with an MTBF of 10^5 to 10^6 hours."

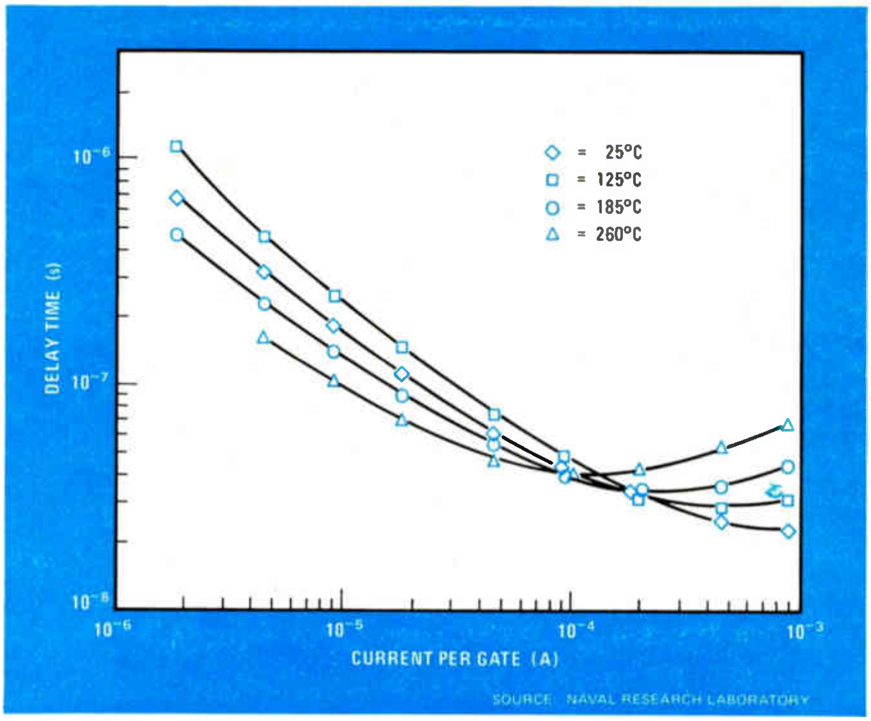
Pioneer. A pioneer of high-temperature electronics has been Sandia Laboratories in Albuquerque, N. M. There, researchers have tackled problems of components used in geothermal well-logging instruments for the last 2½ years. Their interest is not just in ICs, but in hybrid circuits operating from 25°C to 300°C for at least 100 hours [*Electronics*, Dec. 8, 1977, p. 36].

"It's a twofold problem area," says David W. Palmer, principal researcher. "You have to implement circuit designs that are forgiving at such temperatures; also, manufacturing processes must be adjusted for the devices to operate at high temperatures."

Palmer speaks from experience, since Sandia has designed, built, and field-tested hybrid microcircuits that operate from 25°C to 300°C. They are used in logging instruments for geothermal wells, a market that is the driving force behind exploration into high-temperature ICs. "Most people don't realize it, but half of San Francisco's electricity is generated by hot steam sources," Palmer points out. "And there are numerous other places that depend on geothermal energy."

The other major area for high-temperature electronics is the oil-well drilling industry, where the returns could prove lucrative. Palmer foresees an initial market of $20 million to $30 million a year, once a few commercial manufacturers start putting hot ICs on the shelf.

But how many semiconductor manufacturers are interested in such endeavors? Not many, according to Palkuti. Only three have expressed interest in the second task of the Naval Research Laboratory's program, building and testing high-temperature ICs: Harris Semiconductor, RCA Corp.'s Solid State division, and National Semiconductor. That could stem from the fact that there are a limited number of manufacturers that have military radiation-hardened capability, an easier stepping stone to hot ICs.



Gate delay. These figures are from an I^2L test device fabricated with a modified process developed for radiation-hardened applications. Tests were done at Naval Research Lab.

However, the Harris division, in Melbourne, Fla., is the only manufacturer taking the deep plunge by making standard-line devices specified to 200°C available off the shelf within the next six months. "Our dielectric isolation technology was the prime consideration in going ahead with the decision," says R. W. Randlett, product planner for analog devices.

Vital. "Dielectric isolation eliminates all the parasitic active devices inherent in the more common junction isolation, as a result of the extra junction required to perform the isolation function. This becomes increasingly important at high temperatures, where increased substrate resistance, increased H_{FE}, increased leakage current, and reduced V_{BE} combine to increase the sensitivity of junction-isolated circuits and cause a latch-up condition."

The results of tests on HA-2600 high-performance op amps confirm Randlett's assertions (see table). Future available devices contemplated by Harris are quad op amp and quad comparator packages. Simultaneously, work is progressing on an op amp for 300°C operation for the naval laboratory's program. Meanwhile, RCA is conducting an internal search, looking at its high-speed bipolar line, as well as possible C-MOS-on-sapphire candidates.

Not one process technology is being bypassed in this search. Even though dielectric isolation looks promising, C-MOS and I^2L are also heavy contenders. Bulk C-MOS, however, has been shown to be susceptible to electrical- and radiation-induced latch-up, with the result that standard C-MOS devices latch up at high temperatures. But this can be eliminated with minimum redesign, according to Palkuti.

GE, which will be surveying the industry's process technologies for the Naval Research Lab, seems to be leaning toward I^2L, a technology that can easily accommodate both analog and digital circuits and seems to hold up well at higher temperatures than those that are normally specified.

What about devices produced on gallium arsenide? With the majority of present GaAs circuits designed for microwave applications, there are no readily available LSI devices for use as general-function high-temperature ICs. But GaAs is known for its ability to withstand temperature excursions up to 450°C or 500°C. That quality should keep the material in the forefront of the race. □

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IL-5	50	2500	"	1
IL-15	6	1500	"	1
IL-74	12.5	1500	"	1
4N25	20	2500	"	1
4N26	20	1500	"	1
4N27	10	1500	"	1
4N28	10	500	"	1

Part Number	Current Transfer Ratio %	Voltage	Description	No. of Channels
4N32	500	2500	Photo Darlington	1
4N32A	500	2500	"	1
4N33	500	1500	"	1
IL-100	1000	2500	High Speed 75 nS	1
IL-101	1000	1500	High Speed 200 nS	1
ILCT6	20	1500	Photo Transistor	2
ILD74	12.5	1500	"	2
ILQ74	12.5	1500	"	4

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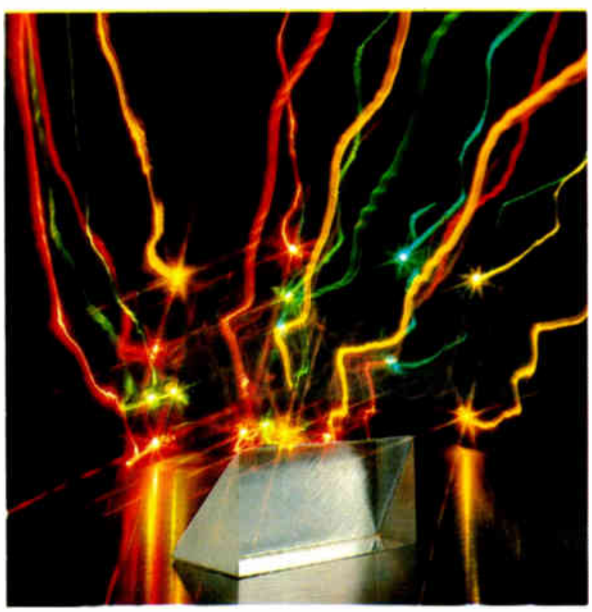


Circle 83 on reader service card

Electronics abroad

French paint a mixed picture

Despite uncertainties about the economy in general, the electronics industries should find 1979 a fairly good year

by Andrew Lloyd, McGraw-Hill World News

Forecasters in France have dubbed 1979 the year of the phony recovery. The phrase reflects uncertainty despite forecasts that the Gross National Product will expand between 3% and 3.5%, because alongside that modest growth figure are much larger percentages: for unemployment, which is at historic highs for the postwar period, and for inflation, which still threatens to run at double-digit levels.

"It is going to be a phony recovery for two reasons," says Alexis Westermann, marketing director for ITT Components, France. "People do not believe in a recovery, so confidence will be lacking, and there is no real sign of any significant increase in demand." Jacques Bouyer, chief executive officer of La Radiotechnique-Compelec, the major components producer in France for the Philips' Industries group, puts it another way: "If investments do take off again in 1979, it will only be a result of non-French factors."

There is one big plus in the outlook, however—political stability. The ruling establishment coalition, which a year ago seemed likely to lose its majority in the National Assembly, won out over the squabbling left-wing parties in the legislative elections. That ended fears among businessmen that a left-wing government would take control of industry and run it mostly for the short-term benefit of the workforce.

Despite pressure from the Left for government measures to combat unemployment, Premier Raymond Barre has refused so far to launch any large-scale package to stimulate the economy. France was one of the first countries to give its economy a boost after the 1974 crisis. This time things might be different. Edouard Guigonis, senior vice president of Thomson-CSF and president of the French professional electronics trade association, says it does not look to him as though the present government will step in to stimulate the economy—"at least not with Barre as prime minister."

What is more, Guigonis maintains that the benefits companies must pay when they lay off employees militates against a recovery in French investments. They are so high that he asks, "Will people be ready to invest in electronic automation equipment if it means getting rid of people?"

Two other uncertainties loom large on French planners horizons, both having to do with the U.S. First, there is the dollar. Guigonis, for one, does not mince his words. "If the U.S. plays the game of the weak dollar, it will be the ruin of Europe," he says.

The second worry is the prospect of a dull market in the U.S. later this year. The tougher it is for the Japanese and Americans themselves to sell in the U.S., the harder will be their attack on European markets, reason French executives.

Not all bad. All these worries integrate the frustrations built up over years of less-than-boom conditions. But when it comes to the electronics industries, things are not really so bad. Equipment markets, according to *Electronics'* survey, are set to rise some 13% to $8.07 billion. The only sector tagged for really poor performance is production and control equipment, forecast to rise only 4%. (Percentages are not adjusted for

FRENCH ELECTRONICS MARKETS FORECAST
(IN MILLIONS OF DOLLARS)

	1977	1978	1979
Total assembled equipment	6,249	7,121	8,070
Consumer electronics	1,846	2,068	2,261
Communications equipment	1,538	1,841	2,223
Computers and related hardware	2,260	2,564	2,885
Industrial electronics	202	222	242
Medical electronics	173	180	192
Test and measurement equipment	170	181	198
Power supplies	60	65	69
Total components	1,324	1,474	1,645
Passive and electromechanical	757	835	918
Discrete semiconductors	166	181	204
Integrated circuits	174	204	242
Tubes	227	254	281

Note: Estimates in this chart are the consensus estimates of consumption of electronic equipment obtained from a survey made by *Electronics* magazine in September and October 1978. Domestic hardware is valued at factory sales prices and imports at landed costs. Exchange rate: $1 equals 4.50 francs.

inflation.) The stagnation—or worse—comes mainly from the reluctance to invest and displace personnel.

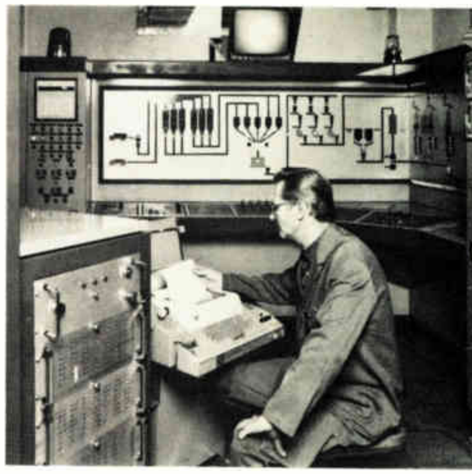
Consumer sales should rise some 9% to reach $2.26 billion. But that may not be so healthy. Says one industry statistician: "The French cannot afford to buy or save for a house, so they are spending more on consumer items."

The big-ticket item is color television. Sales of sets should bound up again this year to reach nearly $990 million. This is good news for receiver makers and their component suppliers, who half expected a falloff. Other fast-rising consumer items are video tape recorders, whose sales should more than double to $17 million, and video games, to rise better than 20%. Sales of black-and-white TV sets and phonographs are going down.

Computer systems and electronic office equipment will rise a strong 12.5% to $2.89 billion, according to the survey. Not surprisingly, smaller systems are pegged for the greatest growth among general-purpose machines. French computer and communications sales are likely to receive a boost from a new program of education and industry aid announced by the government [*Electronics*, Dec. 21, 1978, p. 61].

Getting the word. Word-processing equipment will make the most telling gain among electronic office equipment—better than 25% and maybe even 30%, according to one supplier. Even greater gains could be logged, says one expert, if traditional suppliers of office equipment in France knew better how to sell sophisticated equipment like distributed data-processing systems, facsimile machines, and telephone-related hardware.

The communications sector should be a pacesetter among French electronics markets this year. Sales are forecast to rise almost 20% to $2.22 billion, thanks largely to a 73% jump in deliveries of electronic and semi-electronic telephone central exchange equipment. Orders from the government-controlled telecommunications agency have peaked. So



Keeping track. This ferrite process-control center is maintained by La Radiotechnique-Compelec in its plant at Evreux.

French telephone-equipment companies will be pushing hard for export business.

Defense electronics figures to run strong, but there will be slowing home markets for items like broadcast equipment and air-traffic-control installations. For this kind of gear, luckily, French producers have hefty export backlogs.

In components, Thomson-CSF's Pierre-Leonard Mestre, who heads the company's components operations, is looking for a good first half and a less good second half. "Orders are in and stocks are low," he says. *Electronics* forecasts a nearly 12% rise for components overall, taking them to $1.65 billion. Passive components will pull down the average—their sales will rise less than 10%. Semiconductors will do much better, rising nearly 16% to $446 million.

Integrated circuits are still looking particularly healthy with a sales growth rate forecast at nearly 19%. But there will be a lot more than just market figures to watch this year: the government's moves to build an indigenous manufacturing capability will get under way.

Beneficiaries of government funds, totaling $146 million over five years, are Thomson-CSF and RTC for bipolar development, Thomson and its subsidiary EFCIS together with Motorola for metal-oxide-semiconductor production, and a joint venture between National Semiconductor and St. Gobain Pont à Mousson, also to produce MOS circuits. □

Third in a series examining European markets.

Commentary

Suits muddy software

Increased use of hardware-software mixes complicates question of how computer makers may protect their investment

by Anthony Durniak, Computers Editor, and William Arnold, San Francisco regional bureau manager

The question of how best to protect computer software is still unresolved after more than a decade of debate. The recent spate of lawsuits between minicomputer and semiconductor manufacturers may further cloud the software protection issue—and extend the confusion to protecting the more intangible aspects of computer architecture.

With the growing power of semiconductor devices making computers increasingly similar and less costly, it is the systems and applications software offered that separates the various vendors' machines and accounts for more than half of their development budgets.

Furthermore, the software investment inherent in the design and marketing of microprocessors and microcomputers has added the semiconductor makers to the list of those affected by the software protection issue.

Finally, increasing the importance of the software protection question is the trend to what is called soft architecture—a mixture of hardware and software—which uses much microcode. Such mixes may be the most difficult to protect.

As Calvert Crary, an attorney who studies legal matters for the investment firm of Bache Halsey Stuart Shields Inc., New York, notes, these recent cases "point up an interesting theoretical question of how to protect a data-processing company when a major portion of its investment goes into software."

Suit and countersuit. The most interesting is the suit filed last fall by Fairchild Camera and Instrument Corp., Mountain View, Calif., charging Data General Corp., Westboro, Mass., with violating the antitrust laws with its software licensing agreements. Fairchild was one of the first of a growing number of companies to market computers that emulate Data General's Nova computer [*Electronics*, June 22, 1978, p. 88] and was sued in 1977 by Data General for theft of trade secrets.

Fairchild's action charges (as do similar suits filed by SCI Systems Inc., Huntsville, Ala., and Digidyne Corp., San Diego, Calif.) that Data General is attempting "to stifle and prevent competition from Fairchild and other manufacturers and potential manufacturers of microprocessors and board-level processors which emulate any of the Nova line of computers" by "creating a scheme of legal entanglement and threats whereby any company which has acquired a Nova computer . . . will be deterred from purchasing any Nova-compatible processor manufactured by any other company."

Part of this scheme, the Fairchild suit contends, is the machine-specific software license Data General makes its customers sign. These licenses restrict the use of a given software package to a particular model machine.

The crux. Because software cannot be patented—the Supreme Court reaffirmed that decision last October—computer companies have been using a collection of other techniques (see "Modes of software protection"). Software can now be copyrighted, but this is not considered as absolute a form of protection as a patent because only the expression is protected—not the content of the program or the approach taken to solve the problem.

Software licenses have thus become the primary means of protection and are widely used often in addition to a copyright notice by

Modes of software protection

With software currently considered unpatentable, the popular means of protection, besides licensing agreements, are as trade secrets and by copyright. Although lawyers and companies interpret the rules differently, here are the basics:

Trade secrets are unpublished works with limited numbers of copies and distribution. Customers sign agreements not to divulge the secret information given to them and are liable for legal action if it can be proved they released the information to others. Sperry Univac, for example, uses this technique to protect all its software, and Intel uses it for source code of key software products. Since January 1978, software has been eligible for **copyrights,** and can be submitted to the Copyright Office on magnetic tape, punched cards, or even read-only memories, some legal experts say. A listing of the program and a truth table is usually also required.

Under either method of protection, the companies generally license customers to use the software on a specific model of a machine. Interestingly enough, IBM also offers licenses that cover entire installations (all computers in the same or contiguous rooms) and customer locations (entire groups of buildings at the same mailing address).

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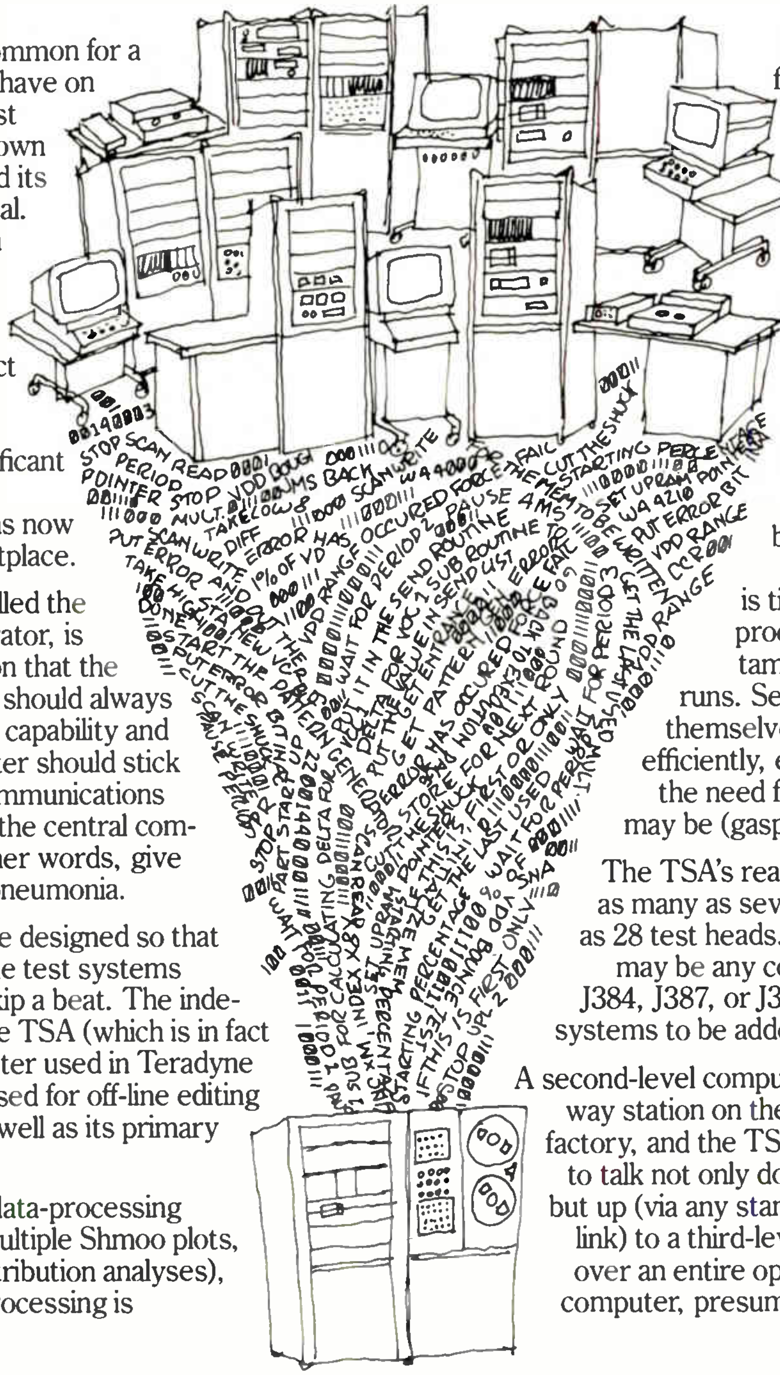
No. 9 in a series.

The test system administrator

A sensible way to manage multiple test systems.



These days it isn't uncommon for a semiconductor plant to have on line a dozen or more test systems, each with its own test program library and its own data output terminal. The situation begs for a clustering of systems around a central computer that can store all the programs and collect all the data. Although the basic idea is simple enough, there are significant differences among the various implementations now appearing in the marketplace.

Teradyne's solution, called the Test System Administrator, is based on the proposition that the individual test systems should always be self sufficient in test capability and that the central computer should stick to management and communications functions. A sneeze at the central computer should not, in other words, give the whole test facility pneumonia.

The TSA was therefore designed so that when it is unplugged the test systems connected to it don't skip a beat. The independence is mutual: the TSA (which is in fact the same M365 computer used in Teradyne test systems) can be used for off-line editing and translating jobs as well as its primary management function.

The TSA has enough data-processing capability to develop multiple Shmoo plots, multiple ADARTs (distribution analyses), and the like, and the processing is performed in real time for fastest possible utilization. The unit is not only scorekeeper but timekeeper as well. One may direct it to pull summary sheets at a given time of day, for example, or to report the time at which the yield on a given system shifted.

The economic benefits of test system administration fall into two broad categories. First, the data feedback loop is tightened, so that minor processing flaws can't contaminate whole production runs. Second, the test systems themselves are used much more efficiently, even to the point where the need for an additional system may be (gasp) eliminated.

The TSA's reach currently extends to as many as seven systems or as many as 28 test heads. At the moment, these may be any combination of Teradyne J384, J387, or J325 systems, with other systems to be added to the list.

A second-level computer is, of course, only a way station on the road to the automated factory, and the TSA is therefore designed to talk not only down to the test systems but up (via any standard RS232 or Bell 103 link) to a third-level mainframe presiding over an entire operation. The third-level computer, presumably, talks only to God.

TERADYNE

Circle 89 on reader service card

both minicomputer and mainframe manufacturers. This makes the antitrust charge the crux of the case. "It certainly would help to know whether a contract that limits the use of software to a specific machine is in violation of the antitrust laws or not," says Bache's Crary.

In its suit, Data General appears to be trying to extend the licensing protection beyond the actual software to the instruction set itself—that repertory of basic operations that the computer is capable of performing. Data General claims that Fairchild could not have designed a unit that runs the Nova instruction set without stealing trade secrets and violating the software contracts. Crary notes that the instruction set "has to be available; otherwise people can't program the computers." The protection of the instruction set could become especially crucial to microprocessor makers, since it is one of the primary basis of comparisons between versions.

In another case, National Semiconductor Corp., Santa Clara, Calif., is suing Digital Equipment Corp., Maynard, Mass., claiming that four of Digital Equipment's PDP-11 patents are invalid for a variety of reasons. This lawsuit is intended to clear the way for National's marketing of a DEC-compatible computer early this year.

Locking the bus. One of the patents covers the DEC Unibus; another covers the method used to connect additional memory and peripheral devices to the Unibus. Since bus structure in general incorporates both hardware and software, it represents one of the intangible aspects of a computer's architecture. As Crary notes, "Patents on software are on extremely difficult ground. The fact that hardware and software are often combined to get around the inability of patenting software doesn't help clear up the theoretical questions of software patentability."

DEC filed a countersuit last month charging National with "wilful and deliberate" infringement of its patents. In addition DEC points out in its

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court papers that two prior court challenges of the patents by California Data Products and Lockheed Electronics "terminated in consent decrees of validity and infringement with injunctive relief against further infringement."

What makes the protection issue involved in these cases more significant is the increasing number of companies marketing hardware that emulates another company's computers. Although applications programs can often be run on more than one vendor's machines—obviously calling for protection from piracy—the operating system software is written for a specific computer and up to now was worthless on another maker's model.

Yet this system software, which increasingly determines the characteristics and performance of a computer, can now be run on an emulating machine, thus making it, too, subject to piracy. Since this represents a growing portion of the computer and semiconductor company's development outlays, system software becomes as critical to protect as the schematics of the logic circuitry.

Although IBM Corp., Armonk, N. Y., also uses machine-specific licenses, it has never legally challenged a user of any of the many processors compatible with its System/370. But most agree that is only because the company, which is already charged with antitrust violations by the Justice Department, did not want to add fuel to the antitrust fire. As for its instruction set, IBM considers that to be in the public domain.

The recent suits provide more impetus for the courts or Congress to set the precedent for software protection. But John McManus, an analyst with investment bankers Shearson Hayden Stone Inc., New York, says the companies involved will find their futures determined in the marketplace. "They can't wait until the suits are settled in court. Both DEC and Data General will fight the emulators in the marketplace on price and performance grounds. ☐

Companies

AMC sees robust future

Advanced Micro Computers Inc. will take advantage of skills of its parents, AMD and Siemens, in single-board market

by William F. Arnold, San Francisco regional bureau manager

With the business in single-board microcomputers expected to highball toward a $500 million market by 1982, Advanced Micro Computers Inc. believes it is on the right track toward a market share of 10% or better. To meet that schedule, the year-old company plans to capitalize on what it considers a unique advantage: the products and marketing organizations of its parents, Siemens AG of West Germany and Advanced Micro Devices Inc. of the U. S.

The joint venture can offer boards based on bipolar 4-bit-slice chips, as well as on 8-bit and 16-bit n-channel metal-oxide-semiconductor devices, and incorporating major or proprietary parts from either side of the Atlantic. For example, this spring, the Santa Clara, Calif., firm expects to launch the first of its Z8000 products built around the 16-bit microprocessor that parent AMD is second-sourcing from Zilog Inc. [*Electronics*, Sept. 14, 1978, p. 52], according to Robert Sumbs, director of marketing, and James R. W. Clymer, managing director of U. S. operations. Z8000 products will include evaluation boards and development systems, they add.

But even with its powerful parentage, is AMC coming to the market with too little too late? For one thing, it has tough competition. Among chip makers, Intel Corp. virtually owns the board business; then there are the likes of Motorola Semiconductor Group, National Semiconductor, Texas Instruments, Mostek Corp., and Zilog. Nor does this list include other firms in the field that make only boards.

Another question is, has AMC had teething problems in getting the right people? "Only for one slot," Clymer responds, and that was for a departing marketing manager. "All I can really say is that we significantly beat our business plan," he adds.

However, a permanent general manager has yet to be found since Anthony Holbrook left in November to become AMD's vice president of bipolar operations. Leo Dwork, formerly manager of AMD's bipolar division, is acting as general manager to help take some of the load off AMD president W. J. (Jerry) Sanders III, who is also AMC's chief executive officer. Clymer, formerly AMD's applications engineering manager for linear and MOS products, has been on board from AMC's inception; Sumbs joined Aug. 1 from Zilog, where he was marketing director.

"The potential seems to be there," observes an industry analyst. "They have the 8080 line and they're getting the Z8000, so they should have some powerful products." But he cautions that starting up a profitable board business probably will take longer than AMC thinks.

Competitors generally refrain from commenting publicly about the new company. However, a source at one large East Coast board maker says, "AMD is a noted bipolar chip maker, so AMC has the proven 2900 microprocessor. Unlike most companies starting out in this field, they have experience and resources behind them. They won't fold over the short haul."

In any event, AMC estimates its volume at the end of its first year at $4 million to $5 million—30% of that outside the U. S. It should be several times better by the end of the second, executives predict.

"The biggest market right now is in process and industrial control, including in-house original-equipment manufacturers," Sumbs declares. On the other hand, part of the market also lies in selling to "labora-

An opportunity for Siemens

For Siemens AG, its partnership with Advanced Micro Devices Inc. in Advanced Micro Computers is more than just another money-making enterprise. Rather, the Munich-based electronics and industrial giant sees AMC as a means of not only strengthening its position at home in Europe but, with the 20% of AMD it also acquired, as a way of gaining a foothold in the technology-rich Silicon Valley. As far as marketing goes, the agreement with AMD gives Siemens worldwide rights to market AMC products except in the U. S., Canada, Japan, and Israel.

Siemens forecasters see the world market for single-board microcomputers as $280 million this year, with Western Europe accounting for 20% and West Germany making up 35% of the European figure. The company says that the annual rate of increase will amount to nearly 20% for the world market and 40% for the West European portion. It figures that by 1982 it will have 10% of the world market and a bit more than that of the West European segment. The prime customer targets for AMC's products are producers of measuring and control equipment with production runs of up to 500 pieces of one type of equipment, it believes. **John Gosch**

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tory environments that buy one or two boards each."

To get that business, the company created in its first year four Intel-bus-compatible boards, led by the 95/4000, which it calls the industry's most powerful single microcomputer board [*Electronics*, Oct. 12, 1978, p. 34]. In development is a 4005 version with less on-board read-only memory and more peripheral control functions.

Due this year is the floppy-disk controller board run by its own 8085A and designed to be a truly intelligent peripheral, Sumbs says. Three boards are already out: the $595 95/6011, which can be added to Intel boards to give them floating-point capability, the 95/1032 32-K random-access memory board, and the 95/5032 32-K erasable programmable read-only memory board.

For even more processing punch, AMC is considering a new 8085A-based board designed as a central processor board instead of a monoboard computer. It would have 20-bit addresses and 64 kilobytes of memory so that it could track more data. Another possibility is a super Z8000 board based on AMD's 2900 series of bit-slice parts.

However, as the 16-bit Z8000 boards come out, how important is all that 8-bit 8080 user base? "The 16-bit area is going to be interesting from a systems standpoint," Clymer answers. "The people using components are primarily updating the machines they have, but there's surprisingly little interest among 8-bit users to stay machine-language–compatible." But Clymer says that AMC is going to help bridge that gap by coming out with a compatible Z8000-8080 family board set in the next 12 to 16 months.

Sumbs and Clymer report that although AMD and Siemens are an ocean apart, they produce complementary parts for their joint venture's board business. For example, AMC markets a Siemens-developed board based on a 3-megahertz 8085 and featuring 22 input/output ports and on-board battery backup for its complementary-MOS memory. □

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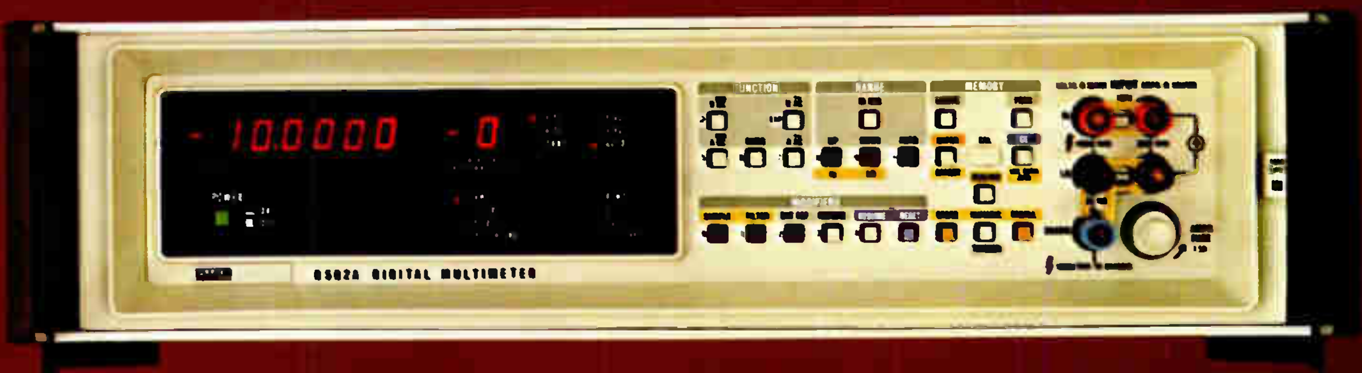

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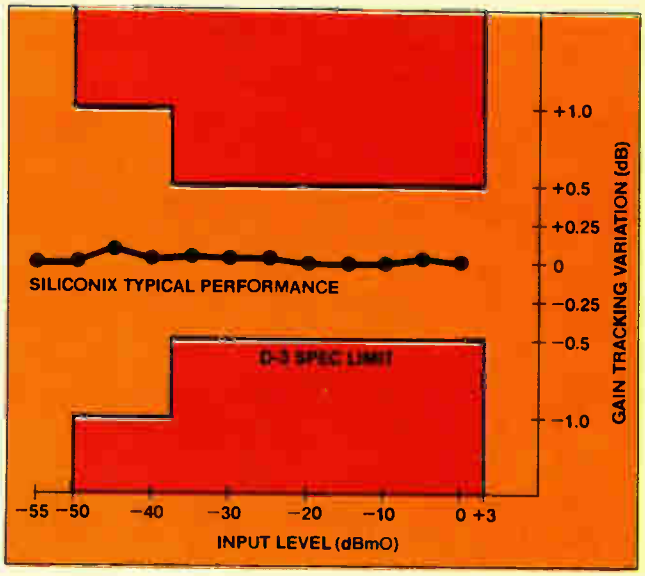

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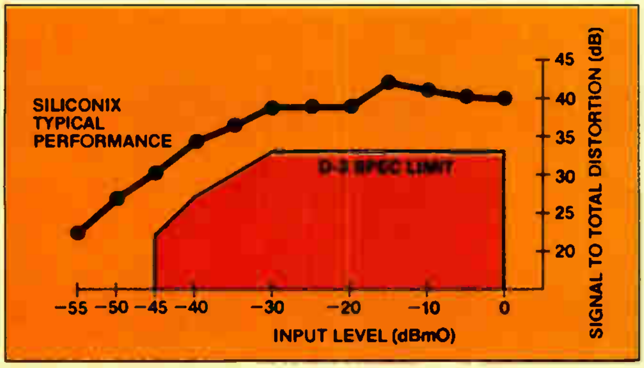

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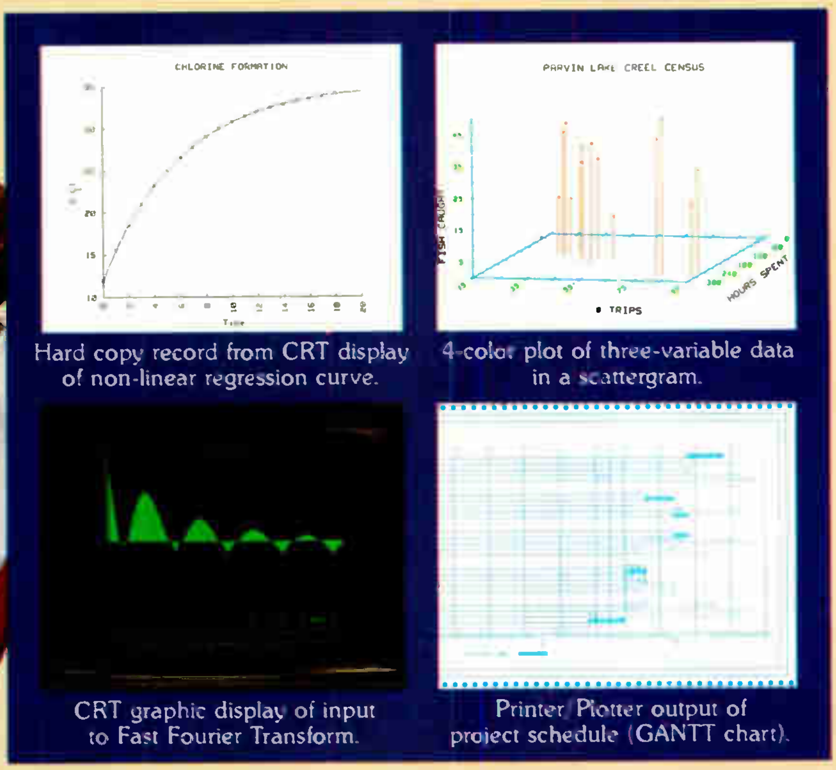

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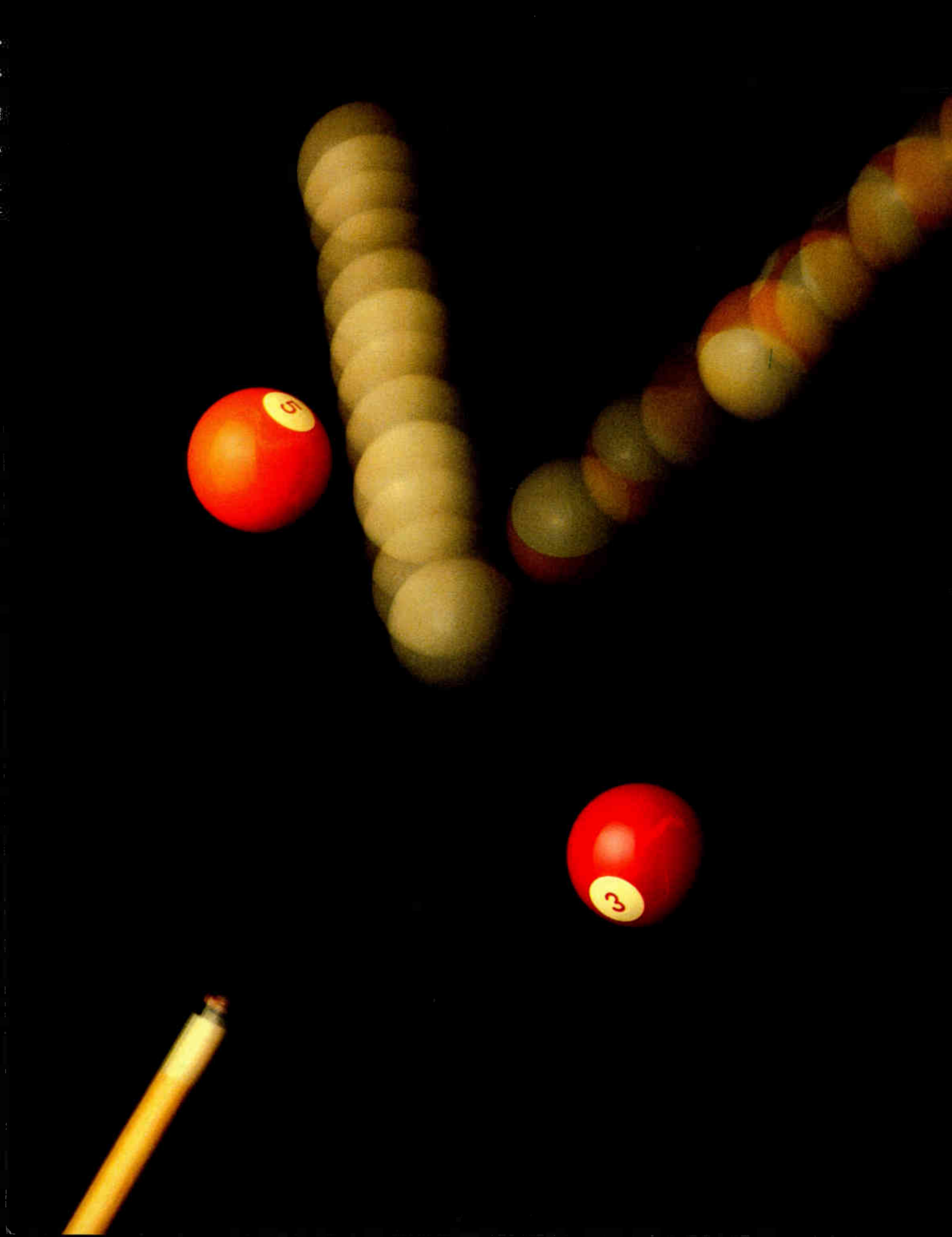

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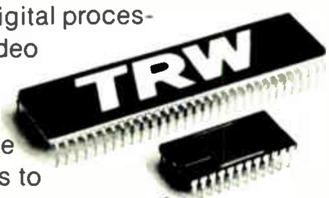

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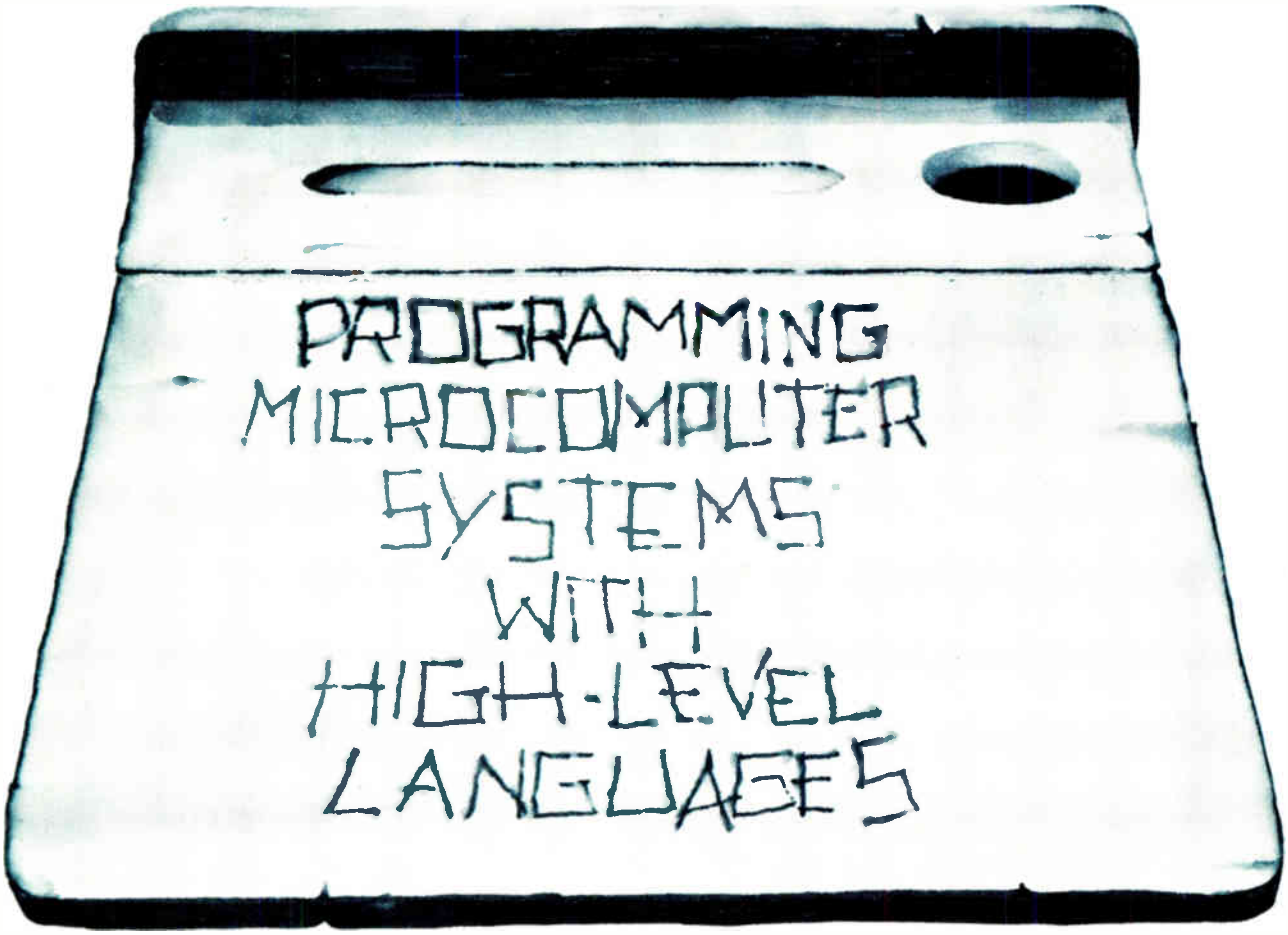


Industrial and other stand-alone applications require languages that are competitive with assembly-code programming

by John G. Posa, *Microsystems and Software Editor*

□ Microcomputer programs are starting to cost too much. The longer and more sophisticated they become, the more impractical it is to code them in assembly language and the more appealing becomes the use of higher-level languages.

Studies show that each line of a program costs about $10 to write, which is outrageous compared to the cost of the chip that will eventually execute it. Worse still, maintaining programs can cost up to three times as much. However, it is also said that programmers write the same number of lines a day, regardless of the language they use—and whereas assembly language generally produces one line of machine code per instruction, high-level languages generally produce several.

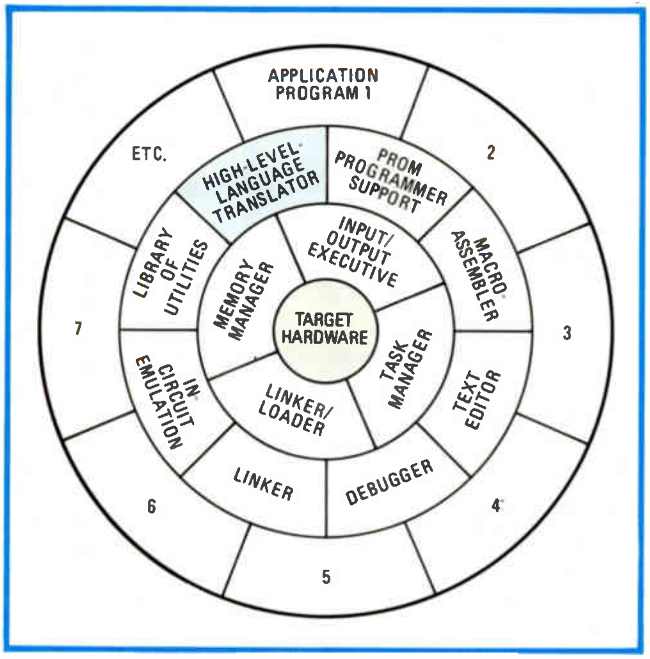
On the face of it, then, high-level languages should be the way to go, because they make more efficient use of the programmer. For one thing, they more directly represent the logical flow that the programmer has in mind once he has figured out an initial algorithm and made a flow chart of it. Also, their commands and keywords are more like English, which again helps with the writing of programs. More importantly, this similarity allows the code to be more easily read, whether by its author or by others, so that it is more painlessly modified, updated, and repaired. This program maintenance, as it is called, is easiest to do on structured programs, because their functional blocks or modules can be altered individually, without upsetting the overall effort.

This is the first article in a series on using high-level languages to program microcomputers.

On the other hand

However, compared with assembly language, high-level languages make less efficient use of the computer. In general, they require more time for execution and

PROCEDURE·BEGIN·REPEAT·FUNCTION·IF·THEN·CAS



1. Target. A well-equipped computer or development system uses a nested hierarchy of software tools. System hardware is surrounded by the operating system, which provides resource management. Translators reside in the next level out with other utility programs.

more memory space—both often critical factors in microcomputer systems. And although memory costs are falling and system clock speeds are on the upswing, space and time savings will remain important because another trend is toward single-chip microcomputers having built-in and hence limited read-only-memory (ROM) space. Moreover, microcomputers are tackling more real-time processing applications, where every microsecond counts.

Also, from the programmer's viewpoint, lengthy programs in a high-level language can take a long time, even an hour, to compile from source code into machine language. About the only way to speed up the process is to cross-compile on a more costly computer; but then users often have to wait for access to the larger machines, and during debugging that can be intolerable.

Evidently, then, an ideal high-level language for microcomputer system design would have to have some remarkable qualities. While producing compact, highly efficient machine code, it would be generalized enough to support good programming practices and be machine-independent—requirements that tend to negate each other. Moreover, if the language is to be compiled, the compiler should be resident. That is, it should execute on the same microcomputer that the software is being developed for, to avoid the cost and inconvenience of cross-compiling, or transferring programs from one machine to another (see "Two types of translator," p. 108). Compilation time should also be as short as possible, and this, too, is tough for a microcomputer.

One way of avoiding these problems is to opt for a macro-assembly language, which is at a higher level of organization than assembly language but at a lower one than high-level languages. Such a language assigns symbolic names to lists of or to individual assembly-language instruction statements, which are executed whenever the names are called. These macroinstructions are ideal for many applications because they yield programs that are almost as condensed and fast as those coded in assembly language but quicker and easier to write. For some projects, in fact, a library of well-defined macros may be more valuable than a high-level language (see "Ready made macros," opposite).

Optimize

Another approach is to doctor up the code generated by high-level language translators. The technique most accessible to the programmer is to hand-code the most critical program sections in assembly language. Development system manufacturers are aware that hand optimization is often essential, so the high-level languages they provide on their machines are either capable of mixing high- and low-level modules or else permit the embedding of assembly-language routines in their low-level object code. The next article in this series, to be published in the Feb. 1 issue, will be devoted to optimization with assembly language.

Such high-level system-development languages now come as integral parts of extensive software packages supplied with major development systems. In some cases, the software support available from chip makers now approaches that of the minicomputer manufacturers.

Figure 1 shows the hierarchical structure of the software tools available on a typically well-equipped development system. This type of diagram can be drawn for Intel's Intellec, National Semiconductor's Starplex, and Zilog's ZDS, among others. The concentric circles are not stationary. Rather, they can be rotated so that various paths can be assumed from the user environment to the target hardware. The bull's-eye represents the hardware of the development system: the central processing unit (CPU), the core and mass memories, and the various peripherals. The next level out, with memory, task, and input/output (I/O) control, is commonly called the operating system.

It is customary to classify high-level languages in terms of their suitability for either application or system programming. Application languages are used for scientific or business calculations, to manipulate mathematical or textual information, as Cobol does, for example. System languages handle more basic machine operations like tasking, memory management and allocation, and process prioritization.

It is worth noting, however, that with regard to microcomputers, the division between high-level application and high-level system languages breaks down. On microcomputers, languages like C and Pascal can be used successfully for both purposes. Also, Basic, though regarded as an application language, is being put into

F•END•UNTIL•DO•WHILE•END•ELSE•FOR•NEXT

Ready-made macros

A macroinstruction, or macro, is a collection of assembly-language mnemonics. At least two languages exist that supply the user with already defined macroinstructions. They are BSAL from Mupro Inc., Sunnyvale, Calif., and SMAL from Chromod Associates, New York. Both serve the 8080 and 8085 microprocessors. Each uses Algol-like control constructs, and each replaces most assembly-language mnemonics with easier-to-read statements.

BSAL stands for Block-Structured Assembly Language. It is part of a software system that contains a relocating/linking loader, a text editor, and a paper-tape or disk operating system, in addition to the BSAL assembler. To aid the human programmer, the language replaces most 8080 and 8085 mnemonics with statements that more obviously denote the respective operation. For example, to increment the accumulator, the 8080 uses the mnemonic INR A whereas BSAL would say A = A+1.

BSAL also allows the use of parametric macros where specific functions within the macro need not be defined until the macro is invoked. Four constants may be defined in BSAL (see table). Addresses of variables and program labels may also be preceded with the @ operator to indicate "address of": for example, HL+@BUFFER (5).

Finally, BSAL uses Algol's IF-THEN-ELSE constructs. When such structured control statements are used, they speed program writing because there is a less than one-to-one relationship between them and the assembly mnemonics, but there is little loss in efficiency because the resulting machine-code bytes are very close to an assembly-language version of the program.

SMAL, which stands for Structured Macro-Assembly Language, was developed at Bell Laboratories in 1974 by Charles Popper, now with Chromod. The newest version of the language, SMAL/80, was designed for the 8080 and 8085 microprocessors and, later in this quarter, will be offered for the Z80 also.

Unlike BSAL, SMAL is implemented as a resident compiler. At present, it can run on any 8080 or 8085 microcomputer having at least 8 kilobytes of memory. SMAL/80 programs can be written free form, in the sense that statements may be written anywhere on a line or across several lines because carriage returns, line feeds and comments are equivalent to blanks. As in BSAL, each statement is terminated with a semicolon.

SMAL/80 also replaces assembly-language mnemonics with easier-to-remember statements. To increment the accumulator, it supplants INR A with ++A. (This is reminiscent of the C language, also developed at Bell Labs).

When a register pair is used as a pointer in SMAL/80, its address is enclosed in parentheses and preceded by an M. For example, "load the accumulator from memory using the H-L register pair as the address" would be written A=M(HL) in SMAL/80, whereas it is MOV A, M in assembly language. SMAL/80 also contains structured control in the form of IF-THEN and IF-THEN-ELSE as well as LOOP-REPEAT-WHILE constructs.

CONSTANT DEFINITIONS IN BSAL AND SMAL MACRO-ASSEMBLY LANGUAGES

	BSAL-80/85	SMAL/80
Binary	%01000001	B'01000001
Octal	–	O'101'
Hexadecimal	#41	H'41' or X'41'
Decimal	65	D'65'
Character	"A"	C'A' or 'A'

ROM to direct the activity of microprocessors in intelligent products, thus functioning as a system language.

One high-level language that has been widely adapted for use on microcomputer systems is IBM Corp.'s PL/1. Intel Corp. of Santa Clara, Calif., Zilog Inc. of Cupertino, Calif., and Rockwell International Corp.'s Electronic Devices division in Anaheim, Calif., offer the microcomputer system programming languages PL/M, PLZ, and PL/65, respectively, to develop software for their chips. Being based on PL/1, these languages are similar, but they are not compatible. All three blend structured programming concepts from Algol and PL/1, support modular programming, and allow assembly-language routines to somehow be incorporated for optimization.

The PL/1-like languages

Intel's PL/M is currently available as a resident compiler for the 8080, 8085, and, most recently, the 8086 microprocessors. The original version of the language was developed by Gary Kildall in 1974 and first implemented as a two-pass cross-compiler that generated down-loadable code for the 8008 microprocessor [*Electronics*, June 27, 1974, p. 103]. The language is now resident on the Intellec Development Systems, including the new Series II.

PL/M-80, for the 8-bit CPUs, uses two data types: byte and address. The byte type takes on 8-bit unsigned values, the address type 16-bit unsigned values. PL/M-86 supports five data types: byte, word (16-bit unsigned), integer (16-bit signed), real (32-bit floating-point), and pointer (either a 16- or 32-bit memory-address pointer).

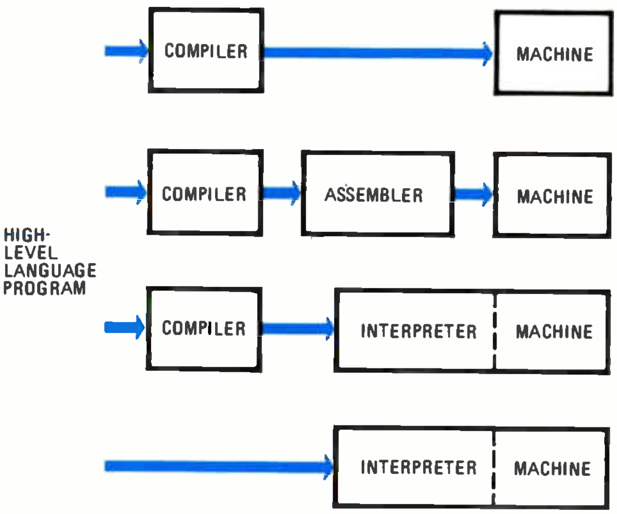
PL/M compiles the source code written by the programmer into relocatable object modules (Fig. 2). The source modules in PL/M contain data declarations and procedures (variable declarations and executable code) that can be given PUBLIC and EXTERNAL attributes to facilitate intermodule communication. That is, a module may employ an EXTERNAL data declaration to reference PUBLIC information in another module.

PL/M has been criticized for producing inefficient

Two types of translator

High-level languages must be translated into a particular computer's machine code before execution can take place. Two sophisticated programs are capable of doing this: compilers and interpreters.

A compiler translates a program written in a high-level language into machine code, assembly language, or an intermediate language. If the compiler generates assembly language, another program called an assembler is used for the final translation into machine language. If the output of a compiler generates machine code, it is said to produce real code—that is, a machine's native language.



Compilation may require as many as six passes to perform some or all of the following functions:

- Lexical analysis to identify keywords and operators.
- Syntactic analysis to identify each statement's type and correctness.
- Flow analysis to find relationships between statements to aid in error checking, register assignment, and optimization.
- Optimization to minimize the number of instructions.
- Code generation to produce assembly or machine language.
- Listing generation so that the programmer can read about what has happened.

Interpreters are very intimate with the machine that executes them. Indeed, they become part of a host and transform it into a new machine having as its native language their high-level language. Interpreters are very useful for fast, interactive programming and debugging, because each instruction is translated before the next, so that any errors show up immediately.

When an interpreter receives a high-level command, it references a predefined sequence of machine instructions to execute the statement. These sequences have to be stored in memory, either random-access or read-only. If all the sequences and the look-up rules are in RAM, the interpreter is said to be implemented in software. When interpreters are used in industrial products, they are often contained in ROM. Also in ROM are instructions, usually in an intermediate or tokenized form.

object code and the compiler is said to be slow. But the language and the ISIS-II operating system are also praised for having numerous helpful user features.

To develop software on its MCZ series of microcomputers and its ZDS series of development system, Zilog offers the PLZ family of two closely related languages. The high-level PLZ/SYS is a procedure-oriented language that blends elements of Pascal, Algol, PL/1, and C and is designed to be divorced from any particular machine architecture. It is implemented as a resident compiler. The low-level PLZ/ASM is actually a structured assembly language for the target machine but with some of PLZ/SYS's control features.

PLZ/ASM is available for Z80 and Z8 currently, and it will be available for the Z8000 this quarter. PLZ/SYS is offered for the Z80 and will be available for the Z8000 around midyear. No version of it exists for the Z8, which, as a one-chip microcomputer with internal ROM, almost always needs only the low-level PLZ/ASM.

PLZ meets many of the requirements of a good microcomputer system programming language. It is structured and produces efficient code quickly. Also PLZ/ASM, being very machine-dependent, can be optimized for speed and minimal memory.

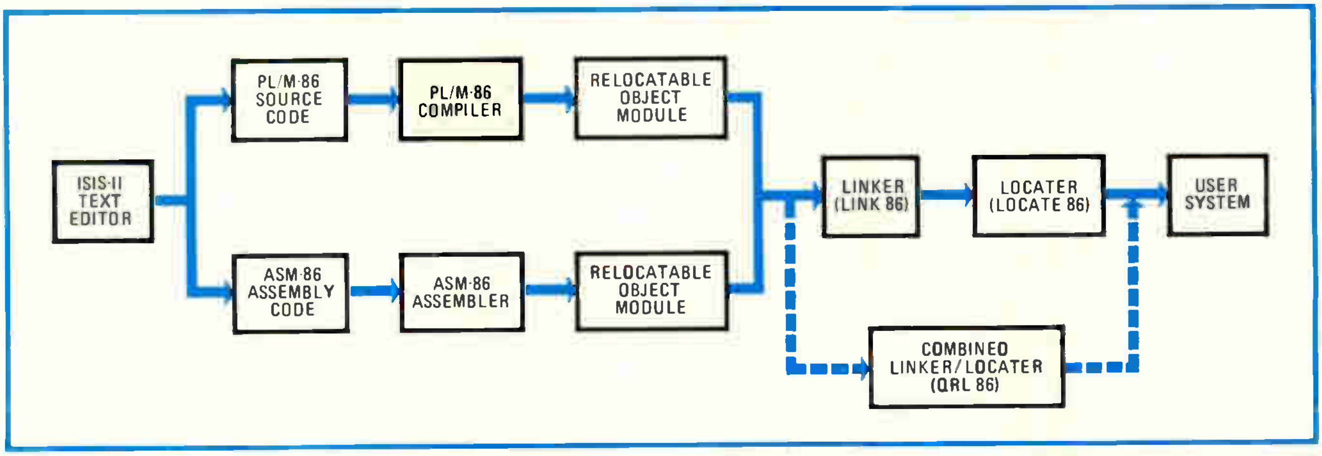
A PLZ program consists of modules that, as in PL/M, contain data declarations and procedures. Module symbols are either internal, external, or global. Intermodular communication is accomplished by declaring a particular symbol to be global in one module, then referring to it as external in another (again, as in PL/M). PLZ procedures contain local variable declarations and executable code.

Conditional statements in PLZ take the form of IF-THEN, which can also be used with a SELECT statement to provide selective execution of various statements, like the CASE statement in Pascal. PLZ provides for iteration with a DO statement. Statements within a DO-OD boundary are executed until an EXIT, REPEAT, or RETURN statement is reached. Figure 3 illustrates how PLZ/SYS and PLZ/ASM modules are linked to form an object module under Zilog's RIO operating system.

Summing up, "the major feature of PLZ is that it was designed as two languages to allow optimization on a modular basis rather than statement by statement," says Jim Gibbons, corporate marketing manager for Zilog. "By having two languages, PLZ/SYS can be truly high-level and machine-independent."

A compiler for the language PL/65 is available on diskette from Rockwell International to develop code for the 6500 family of microprocessors. The compiler is resident, and no additional random-access memory (RAM) is needed over the standard 16 kilobytes supplied

F • END • UNTIL • DO • WHILE • END • ELSE • FOR • NEXT



2. PL/M *et al.* High-level-language translaters for the 8086 produce relocatable object modules that are linked for execution. For the 8-bit 8080 and 8085, programs written in Intel's Fortran-80 will also generate modules in addition to those coded in PL/M and assembly language.

with the System 65. As a bonus, a PL/65 compiler and a 6500 cross-assembler are available to run on the PDP-11 minicomputer under the RT-11 operating system.

The PL/65 compiler produces assembly language for the System 65's assembler, making it possible to enhance or debug a program at the assembler level.

PL/65 also supports modular program design, since the language's conditional and iterative-looping control statements can be used in a structured manner. Other features of the language are integer arithmetic, conditional and collective execution, and array manipulation.

Besides PL/M, PLZ, and PL/65, some other compiled languages that resemble PL/M are available for other devices. Motorola Semiconductor offers MPL, also a descendant of PL/1. MPL is resident in Motorola's Exorciser development system for the 6800 CPU. Versions of the language will be available this year for the 6809 and 68000 CPUs as well. MPL produces assembly code for space and time enhancements as well as allowing embedded assembly-language statements at the source level. National Semiconductor has a language called SMPL to develop software for IMP-16 and Pace microprocessors. Signetics offers PLμS for the 2650 (also written by Kildall). Finally, there exist two versions of PL/M for the 6800 called PL/M 6800 and PL/W, which are available through Intermetrics of Cambridge, Mass., and Wintek Corp. of Lafayette, Ind., respectively. Intermetrics in fact may soon have a number of software products for microprocessors. "We're thinking about coming out with a family of compilers and really jumping on the microprocessor bandwagon," says Richard Weissberg, product manager for PL/M 6800, adding, "We don't know if we'll stick with PL/M or start using Pascal."

Pascal catches on

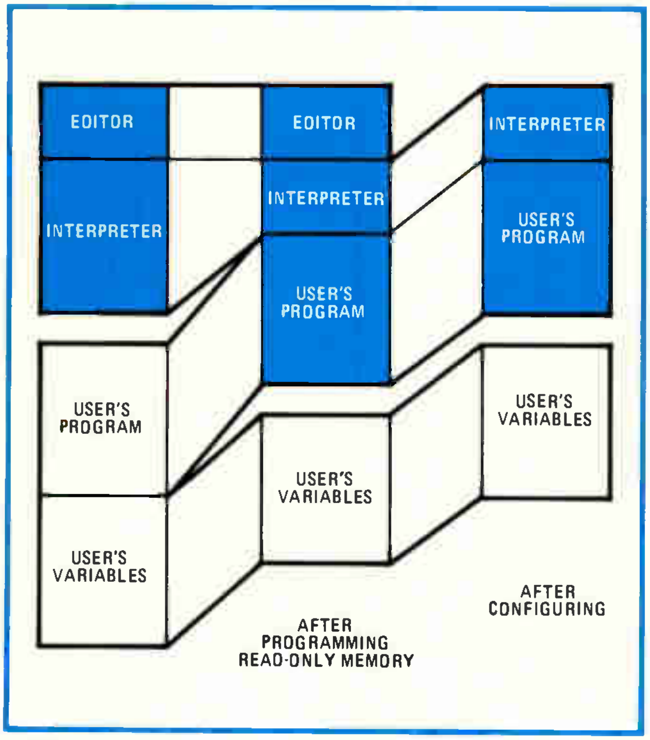
The language Pascal was deemed valuable by the academic world from its inception and is just now beginning to catch on in the industrial domain [*Electronics*, Oct. 12, 1978, p. 81]. Seemingly every corporation from American Microsystems to Zilog is eyeing it.

Pascal is popular for good reasons. First, it appears to be suitable for both system and application programming. Second, it is relatively new, having been written only 10 years ago, so that it incorporates many valuable features not found in older languages. Pascal's structured control features, for example, constitute one of the most comprehensive lists of any programming language.

A big problem with Pascal at present is that no usable standard exists for the industrial community, yet activity in it is high. The version proposed by its author, Niklaus Wirth, in his book, "Pascal User Manual and Report," evidently is unsuitable for industrial applications because every new user has to quickly add extensions or modifications. If this continues, Pascal could become a family of languages like Basic and the user would then be uncertain of their compatibility without an in-depth analysis. However, a committee sponsored by the American National Institute of Standards gathered for the first time last month to discuss Pascal, and other such activities are progressing in Europe.

Probably the two most active proponents of Pascal in this country are the University of California at San Diego and Texas Instruments Inc. of Dallas. UCSD's Pascal compiler generates an intermediate language (often called pseudo code or p-code) for interpretation by the target machine. This enhances the language's portability. Once the interpreter has been written in machine language, UCSD Pascal can be compiled to run on it. For this reason, the language has been adopted for a multitude of microprocessors.

Because the interpreter must somehow be included in the host machine, some say the overhead renders UCSD Pascal unattractive for industrial applications based on the use of read-only memory. All the same, some companies have been steering UCSD Pascal toward industrial environments by implementing the interpreter in hardware. Recently, for example, Control Systems Inc. of Kansas City, Kan., introduced its Universal Development System 470, which has the UCSD interpreter in ROM [*Electronics*, Dec. 21, 1978, p. 128]. After the user



5. Three sizes. Of the many versions of Basic, TI's is called Power Basic. Knowing full well that in ROM-based controller applications space savings are important, TI provides a configurator to whittle down the ROM requirements (shown in color).

gate packages in the most cost-effective way, there just isn't enough slop left over to warrant using a high-level language. It's like trying to replace a few gates with a fancy LSI package—you can't afford it, and so you keep the gates."

Bob Swartz, vice president of the Mark Williams Co., Chicago, Ill., would say that Russo and others like him are in a gap where high-level languages cannot be used effectively. "Almost all high-level languages are adaptations from data processing and not specifically designed for microcomputers. Therefore, they don't have the kind of control that the industrial application needs, like bit manipulation and interrupt-handling capabilities," says Swartz. And on the other end is assembly-language programming, which most industrial applications still use. "There's a big gap in between, and nobody seems to be asking the engineers what they need," he says.

He also feels that compilers are a mistake for many microcomputer users. "Compilers are really meant for large machines that get paid for by being used all the time. Intelligent interpreters are really the way to go. You can tinker around with them, add new devices, and debug and maintain programs in the field." The Mark Williams Co. currently markets a Basic interpreter called XYBasic that is geared to the industrial user [*Electronics*, Sept. 14, 1978, p. 224].

Whether to use an interpreter or a compiler for industrial software development is another controversial question. Many agree with Swartz that for small projects the interactive nature of an interpreter is invaluable. Bill Gates, president of Microsoft Co., Bellevue, Wash., feels that a compiler that is able to generate real machine code is best, at least for large, industrial projects. "For small systems, sometimes the interpreter itself will be as large as the user's program, and it's three to five times slower," he says.

Gates also sees lack of programming support in microcomputer software: "Industrial people need better real-time operating systems, better data-base management systems, and there's a lack of utility programs."

Next year, to help bridge that gap, Microsoft plans to add to its support of 8-bit machines with four new software products. It will introduce an APL interpreter [*Electronics*, Dec. 21, 1978, p. 68], a Basic compiler, a data-base management system, and a superset of Pascal, all aimed at the microcomputer user.

"Pascal is good for both system programming and application programming, but most versions of the language make use of pseudo-code, which renders them unsuitable for industrial programming," says Gates. Microsoft's Pascal will instead generate real code, and it will be heavily influenced by the language C, a Bell Labs creation. "C's notation is not only compact, it makes it easy to design the compiler as well," says Gates. "I hope to push it on the development system people—Zilog, Mostek, etc."

Gates is also interested in the new 16-bit machines and expects to do Cobol and Basic for the 8086 and Z8000. "The newer processors are so much faster and it will be easier to set up multi-user systems," he says. "Also, hard disks seem to be growing more popular for microcomputers. The microprocessor is so general-purpose that it's getting harder and harder to distinguish between a development system, a small-business system, and an intelligent terminal."

Kildall, now president of his own firm, Digital Research Inc. in Pacific Grove, Calif., maintains, "System languages in general are just a cut above assembly language. You really need access to the machine's facilities like interrupt control and the I/O ports. So you have to be able to generate machine code that's competitive with hand coding. With interpreters, you can get really dense code, but you pay for it in time. In systems based on ROM, you just can't run as fast as the machine itself. Interpreters have an overhead that you can't get rid of."

Adds Zilog's Gibbons: "When a person uses a ROM as opposed to a magnetic device for program storage, that person is obviously concerned with the size of his code. I'm not certain this person has ever been satisfied with high-level languages, and I don't know if he ever will. He's almost by definition interested in hand-tooling his programs. It's our goal and the goal of others to ultimately satisfy that person. But when you go through a list of people who need software, it's those people who will get it last, because their requirements are the most stringent." □

Design forethought promotes easier testing of microcomputer boards

Three key considerations are: using microcomputers' self-test capabilities, adopting new diagnostic algorithms, and designing the system for testability

by Michael D. Lippman and Edward S. Donn, *Fluke Trendar Corp., Mountain View, Calif.**

☐ In the course of changing system design radically, microprocessors are complicating testing procedures just as radically—yet these new chips can be as much a part of the solution as they are of the problem. The trick is to take advantage of the inherent intelligence of microcomputers, notably their ability to perform self-tests.

Traditional test schemes are designed to find stuck faults in largely combinatorial systems, which pyramid circuits to perform specific tasks and thus operate in ways that can be traced by following the dedicated circuitry. Such test methods cannot cope with the bidirectional buses and the soft failures that characterize microprocessor-based systems. What is required, then, is the use of new diagnostic algorithms developed for microcomputer testing.

Moreover, testing of systems can be significantly eased by taking testability into account during the design stage. Such designing for testability will simplify troubleshooting on the production line and in the field.

Self-test benefits

Self-tests can drastically reduce the costs of testing microcomputers and can have the same effect on microprocessor board testing. Written in the processor's own language instead of automatic-test-equipment languages, a resident test program will provide large volumes of stimulus data and accurate verification of the system's workability. It can be used universally for development, production testing, incoming testing, and field testing.

Such test programs can exploit the sequential operation of microcomputer systems. The assigned tasks are performed through step-by-step software connection of individual system functions. Thus it is easy to isolate the

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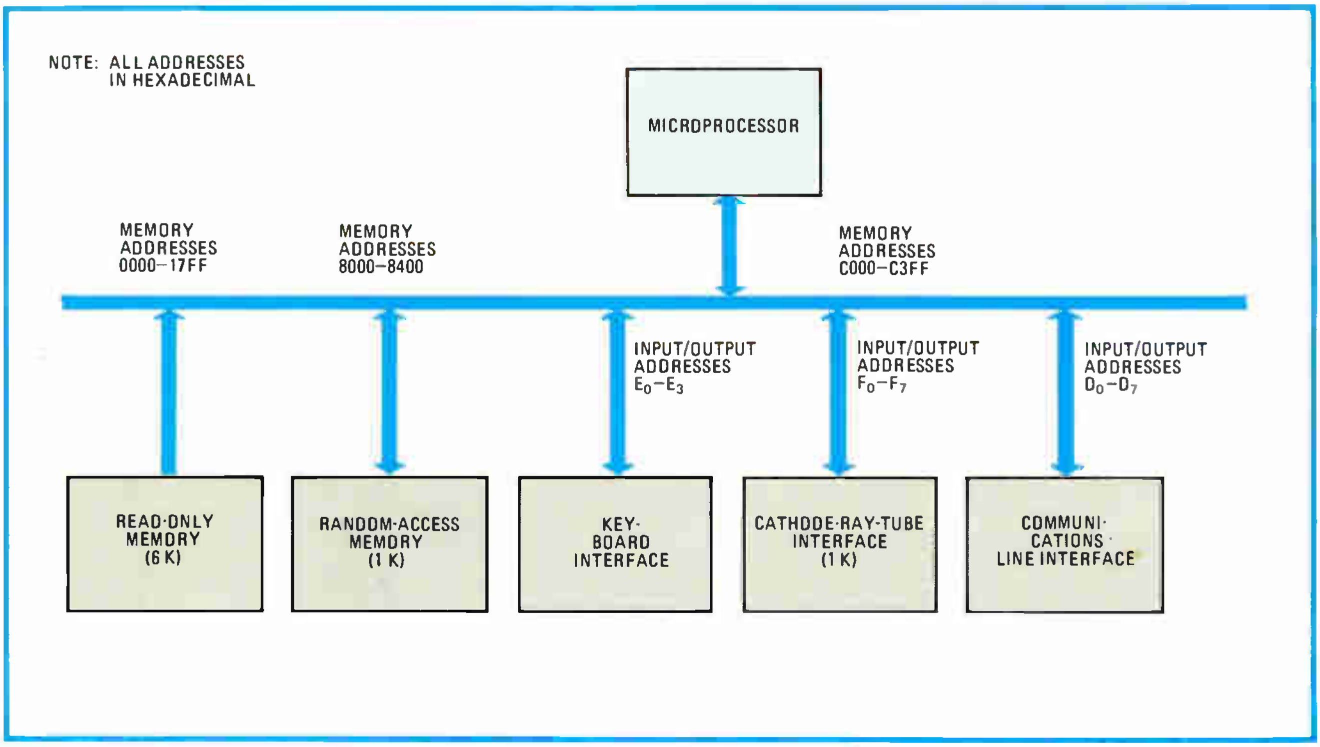


1. All aboard. The functional subsystems of a microcomputer board are partitioned physically and electrically, thanks to its inherent bus architecture. This common system bus provides access simply by addressing the desired memory or input/output section on the board.

causal failure, in contrast to the random-logic combinatorial systems where troubleshooting must work back through every bit of circuitry between the incorrect result and the cause.

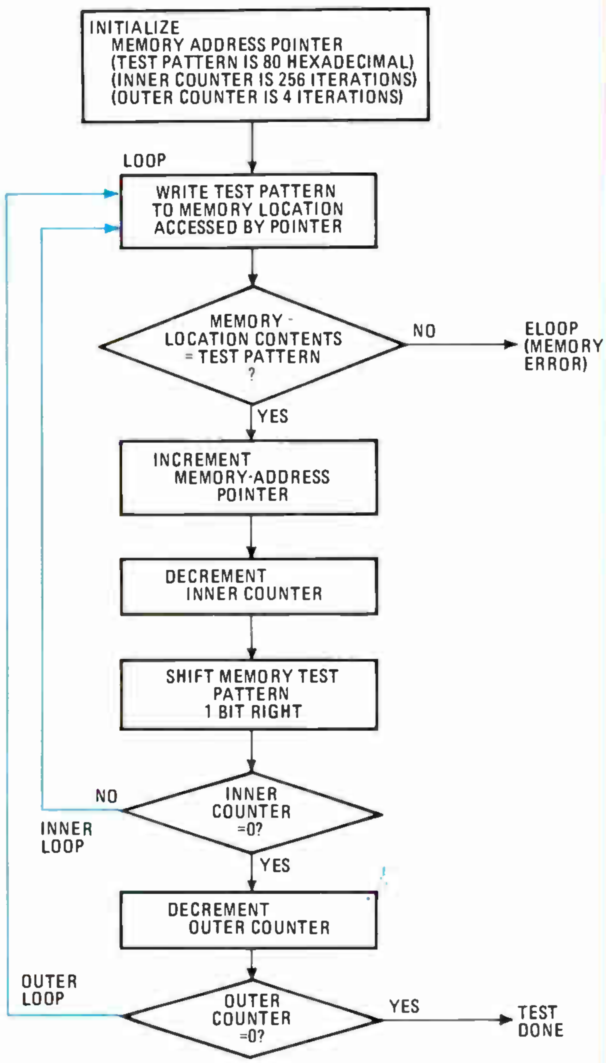
Another testing advantage inherent in microcomputer architectures is the partitioning of the boards by the memory and input/output address assigned to the different functional modules (Fig. 1). Such functional partitioning gives easily diagnosable modules and minimizes the switches, sockets, or gating dedicated to testing.

Easy testing access

The system bus solves the too common problem of insufficient test points, because it connects with almost every complex device on a microcomputer board. The tester can be connected to the bus for both monitoring and control of these devices. Frequently it is possible to eliminate the expensive bed-of-nails fixture required for access to individual devices on a board.

It is worth emphasizing again that testing microprocessor-based boards differs markedly from testing random-logic boards. The major problem with these combinatorial random-logic systems is supplying just the right stimulus to get a stuck fault to propagate out to one of the board's edge connectors, where the test engineer can find it and verify that the board was bad.

On the other hand, microcomputers easily generate their own stimulus and verification for go/no-go testing. A few instruction codes can control 1 to 2 kilobytes of program memory to generate on the order of 1 billion bits of stimulus on the system bus and possibly 10 billion bits throughout the board under test (Fig. 2).



2. RAM self-test. The 15 8080 instructions to test a 1-k random-access memory use only 30 bytes of program code to generate about 427 kilobits of stimulus data. The flow chart for this self-test procedure shows the simple repetitive pattern that is used.

8080 RAM TEST ROUTINE

Address/program code		Label	Instruction		Comments
0041	210010	1 BEGIN:	LXI	H, MEM	;LOAD MEMORY ADDR PTR (H, L)
0044	3E80	2	MVI	A, 80H	;INITIALIZE MEMORY TEST PATTERN
0046	0604	3	MVI	B, 04H	;INITIALIZE OUTER COUNTER = 4
0048	0E00	4	MVI	C, 00H	;INITIALIZE INNER COUNTER = 256
		5	;NOTE:1024 RAM LOCATIONS ARE COUNTED BY INNER X OUTER =		
		6			;256 X 4 = 1024
004A	77	7 LOOP:	MOV	M, A	;WRITE TEST PATTERN TO MEMORY
004B	BE	8	CMP	M	;CHECK MEMORY LOCATION WRITTEN
004C	C25C00	9	JNZ	ELOOP	;JUMP IF THEY'RE NOT THE SAME
004F	0F	10	RRC		;SHIFT PATTERN 1 BIT RIGHT
0050	23	11	INX	H	;INCR MEMORY ADDR PTR
0051	0D	12	DCR	C	;DECR INNER CTR
0052	C24A00	13	JNZ	LOOP	;LOOP IF INNER COUNTER NOT 0
0055	05	14	DCR	B	;DECR OUTER COUNTER
0056	C24A00	15	JNZ	LOOP	;LOOP IF OUTER COUNTER NOT 0
0059	C34100	16	JMP	BEGIN	;DO IT AGAIN (MAINTAIN INT ENA SETTING)
005C	C35C00	17 ELOOP:	JMP	ELOOP	;TRAP MEMORY ERROR
1000		18	ORG	1000H	
1000		19 MEM:	D5	1024	;BEGINNING MEMORY ADDRESS IS 1000H

Software initialization can be tricky

The basic rule in software initialization is to first write a test pattern into each memory element to ensure that its contents are known. However, the memory element must be initialized to a value that the tester can anticipate. For comparison testing, both the reference board and the board under test must be initialized to the same value.

As the following example shows, initializing a microprocessor system can require some programming subtleties.

In response to an interrupt, the 6800 microprocessor stores the current value of the program counter, the index register, both accumulators, and the condition-code register in the contiguous block of random-access memory called the stack. Should an interrupt occur soon after the initializing reset signal, then the contents of these registers will be pushed onto the stack.

The problem is that some registers will be holding unknown contents if the program had not yet used them or set its status bits. That is, what will go into the stack—and will come out again when the return-from-interrupt instruction is executed—is whatever was in these registers before the initializing reset signal occurred. Thus these registers have not been initialized, a problem that occurs with several processors besides the 6800.

Fortunately it is easy to avoid this problem by taking precautions when writing the software for the test program. Any processor register that can be pushed onto the stack can be initialized by a few register-load instructions. For example, the 6800's TAP instruction will initialize the condition-code register by storing the contents of accumulator A in it. For the 8080, an XRA A instruction exclusive-ORs accumulator A with itself, thus clearing all of the status bits.

A microcomputer can carry this vital self-test with it in an inexpensive read-only memory. The test program, written in assembly language on the microprocessor development system in about a month, can be used any time a go/no-go test is needed.

Furthermore, the test algorithms are portable between systems using the same microprocessor. For example, the memory test for an 8085 processor can be the same for every system except for the address parameters. Only new I/O features require any notable modification of the test program.

Self-testing can radically reduce the amount of automatic test equipment needed, because the go/no-go routine can quickly identify good boards that need not go on automatic testers. However, self-testing verifies faults; it does not diagnose them. So diagnostic algorithms come into play.

As well as being written in the unfamiliar languages that are used in automatic test equipment, test programs for random logic diagnose poorly on the board level. Sometimes they can find a bad board, sometimes only a bad set of boards; but seldom can they pinpoint a bad component on a board.

With random logic, diagnosis of board failures is a simple procedure, since the dominant failure mode in such systems is a stuck pin. To find this type of fault, it is necessary to start with a board's edge failure and work back to locate the device with good inputs and bad outputs. A spatial diagnostic algorithm is used, but it might have to wander all over the board to follow the path leading to the failure.

Uncovering system failures

Failure of microcomputer-based systems can be much more challenging, for three reasons. Failures are dynamic, which means they can propagate through the steps of a task, increasingly skewing the result. Moreover, the bus is bidirectional, and the response data is enormous, typically 10 billion bits per test.

Because microcomputer boards are in effect systems, often the parts will test good but the system will not work because of speed- and noise-induced failures. Such problems only show up when the whole circuit is operating at speed with realistic data. Moreover, they take far more time and data to uncover than do simple stuck-pin failures that can happen in random-logic systems only in predetermined sequences.

The bus that makes it so easy to monitor the working of microcomputer systems is bidirectional. This attribute defeats spatial diagnostic algorithms, which require that inputs and outputs at each point in a circuit go in only one direction. So the bidirectional bus dictates an algorithm that diagnoses sequentially rather than spatially.

A microcomputer needs a lot of stimuli to uncover dynamic faults, but fortunately they are easy to generate from program memory. Effective microcomputer tests require about 30 seconds to exercise the board. For a 32-bit bus (16 address bits and 8 each data and control bits), the amount of stimulus data for a test of this length typically is: Bus data = (32 bits) (30 s) (1 megahertz) = 0.96×10^9 bits.

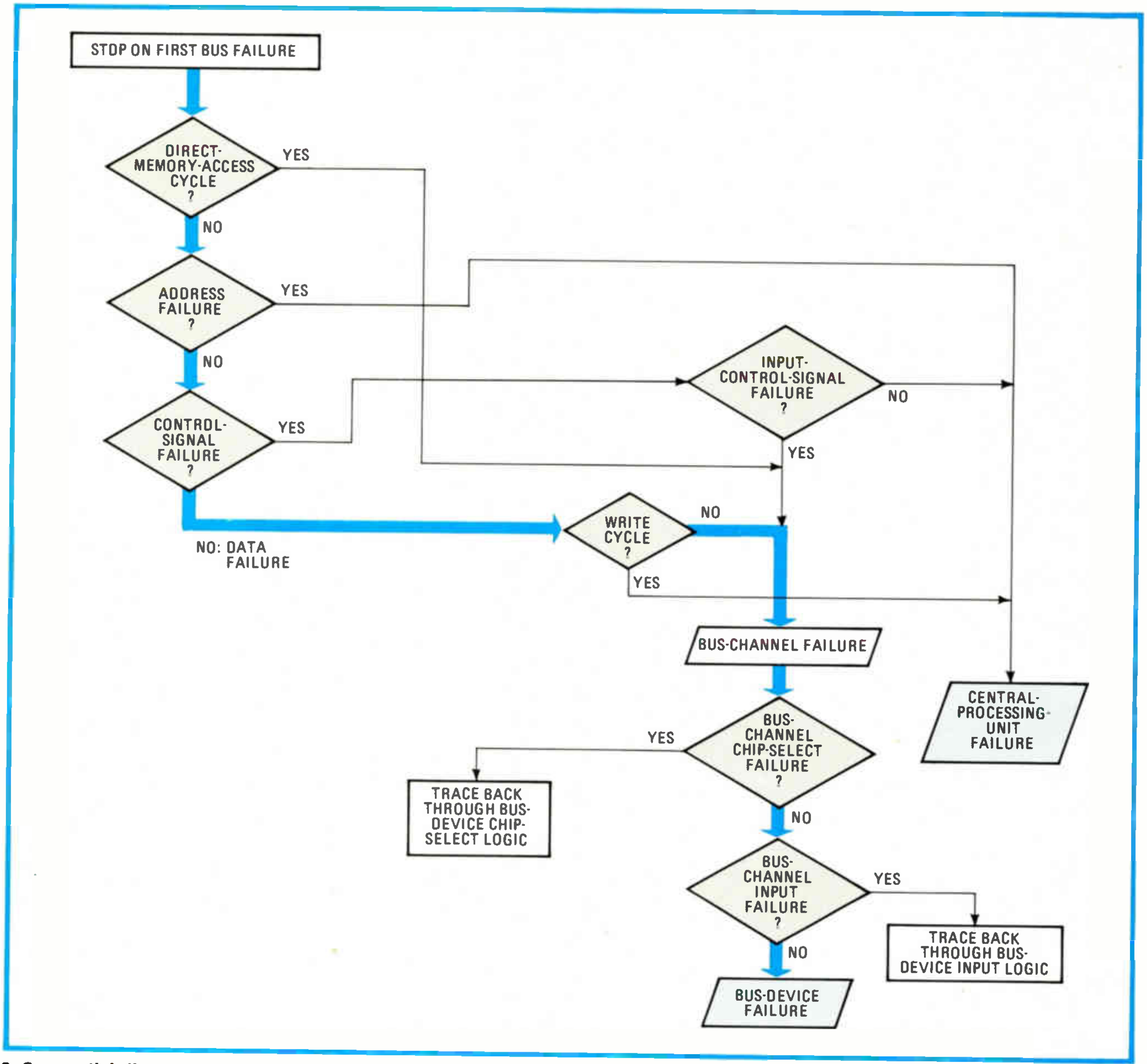
Storing this much data for diagnosis is practical only with a test system that relies on emulation tests of a known-good board. This approach is similar to the techniques recently evolved for testing large-scale integrated devices [*Electronics*, May 25, 1978, p.141].

The sequential diagnostic algorithm

Although self-test response data is a go/no-go indicator, it can be analyzed with a new sequential algorithm capable of real-time diagnosis on a three-state bus. Figure 3 shows the algorithm's flow chart. The tester, whether a logic-state analyzer or a production tester, begins by identifying the first, therefore causal, failure on the bus. The status of the microprocessor is stored and analyzed to find the failure channel.

If the microcomputer is not executing a read cycle, the failure comes from a direct-memory-access channel or from the central processing unit. Status information will, of course, identify which one.

If the failure occurs during a read cycle, any of the other bus-connected devices could be the source of the fault. The address and data information stored when the failure occurred will identify the channel harboring the



3. Sequential diagnosis. The sequential algorithm diagrammed diagnoses microcomputer bus-oriented problems in real time starting with the first bus failure. The address and data information stored when the failure occurred can be used to identify the fault.

fault. Then the test equipment may use conventional spatial algorithms in order to narrow the fault down to a bad node by probing for a device on the bus having the correct inputs and incorrect outputs.

However, there is more to designing for testability than taking into account the microcomputer's self-test capability and the need for sequential diagnostic algorithms. It is necessary to make the designs testable from the start, so that specific hardware and software requirements must figure in designing these boards.

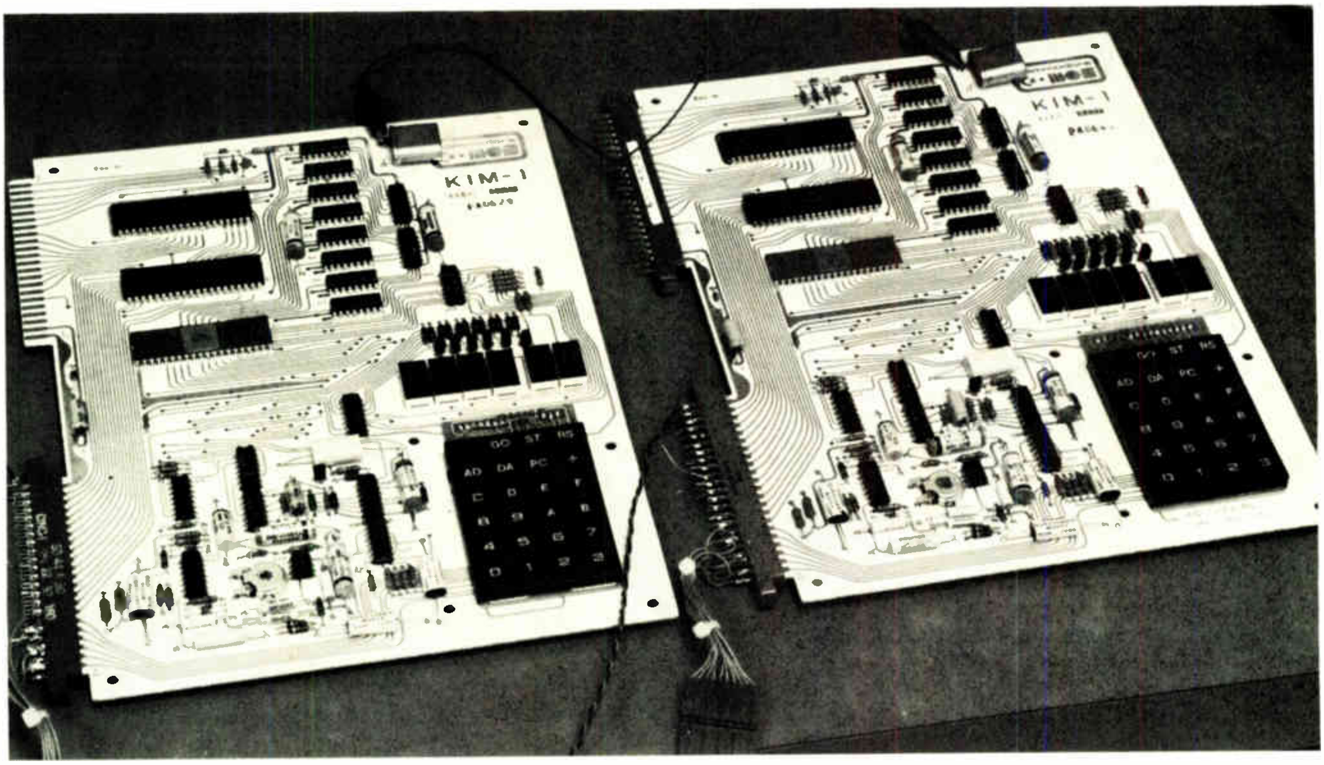
Design rules to follow

The design procedures exploiting the capabilities of the microprocessor for testing are simple ones. Some come from conventions established for random-logic boards; many are unique to microcomputer boards. These procedures can be grouped into five categories for discussion: access to the board under test, synchronization and control of the board by the tester, initialization of the devices on the board, self-testing, and some miscellaneous rules.

In providing access to the board, the first thing to remember is that the address, data, and control bus lines of the microprocessor form the central nervous system of the entire microcomputer. They must be accessible, preferably by being brought out to edge-connector pins.

If this setup is impossible, there should be enough room left around the microprocessor chip to fit a test clip. The penalty for using a test clip is simply some additional board-handling time.

Another point to remember is that what used to be an I/O module or board is often one component in a single-board system, such as the keyboard and display circuits in the lower right corner of the board in Fig. 4. In order



4. Packed on. The Commodore Kim microcomputer board exemplifies on-board input/output component design, containing both the keyboard and display circuits in the lower right hand corner. Earlier designs often featured separate boards for this circuitry.

for the tester to exercise the inputs and measure the response of the outputs, it must have access to all on-board switches and displays, via edge-connector pins, test sockets, or test points on the board.

To perform a real-time check, the tester must be synchronized to the board under test. Either it must clock the board, or the board must clock it.

A simple scheme for comparison testers and for boards with crystal oscillator clocks uses a clip lead connecting identical crystal sides in the known-good board and the board under test (Fig. 4). This forces the crystals to oscillate at the same frequency, so long as the two separate frequencies are reasonably close. It also can be used for some RC oscillators with low Q.

Other types of testers need a technique that disables the board's oscillator and feeds in a clock signal from the tester. These requirements may be met easily with an off-board jumper scheme, which also permits checking the oscillator independent of the rest of the circuit. Other alternatives include clock-gating circuits and socketed oscillator components.

Synchronized clock rates

Sometimes systems need several clock rates, as in a setup with a microprocessor and a universal asynchronous receiver-transmitter. If these clocks are unsynchronized, they will almost surely preclude testing the system as a whole. There is a way around this roadblock: generating the multiple frequencies by counting down from a common multiple oscillator.

Another essential signal that must be provided is a start-up synchronization so that the tester knows precisely when the microcomputer's self-test program begins execution. An easy way to obtain this synchronization is to let the tester generate a reset signal for the board. Thus the board should have an external input for this purpose, supplementing the usual system reset-signal input. For comparison testers, a single reset signal must go to both the reference board and the board under test.

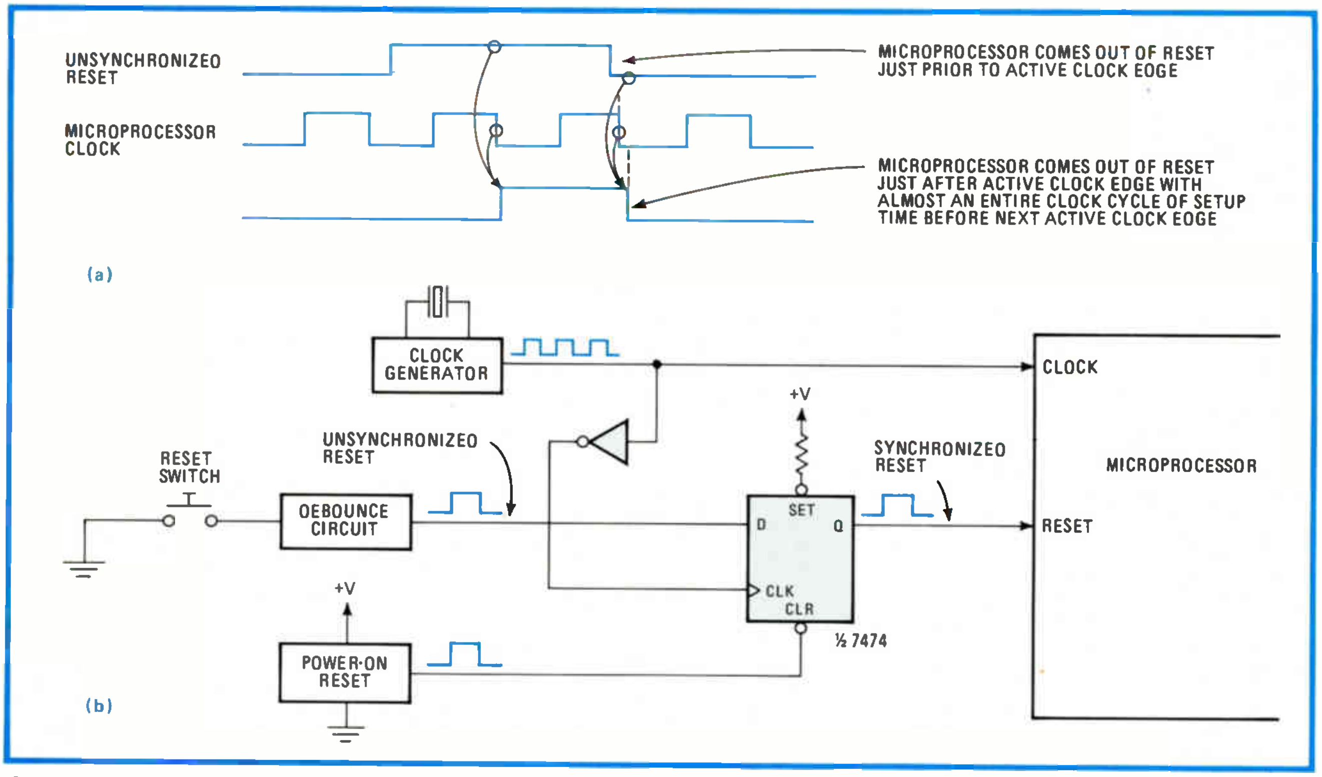
Since the reset signal reaches the microprocessor, it must be synchronized with the processor's machine cycle (Fig. 5a). Otherwise, the processor could come out of its reset state in the middle of the clock pulse near an active clock edge, possibly putting the board one full machine cycle out of synchronization with the tester or the known-good board.

Synchronization approaches

Some microprocessor clock-generator chips, like the Intel 8224, perform this reset synchronization. If such a chip is not in the system, the simple circuit in Fig. 5b will perform the synchronization.

An important test consideration is to permit the tester to supply microprocessor control signals, such as read and write strobes and status identifiers. The external control signals should be multiplexed onto the system control bus along with the processor's hold request. In this manner, the tester can replace the processor to emulate direct-memory-access or peripheral devices.

All memory elements in the system must be initialized: not only the hardware latches and counters, but also random-access-memory locations and all processor and peripheral-chip registers that will be read. To get to the RAM locations and these registers, it is possible to use software initialization, that is, to gain access through the system's program. However, using this relatively new



5. Reset sync. A tester's unsynchronized reset signal can cause a microcomputer board's processor to come out of reset just before or after the active edge of the board's clock (a). A simple circuit (color in b) provides synchronized reset signals, ensuring proper timing.

concept involves some subtleties, especially with regard to interrupts and stack operations (see "Software initialization can be tricky," p. 115).

If possible, there should be no uninitializable support components, such as memory-refresh counters with no reset. Even if there is no functional reason for initializing a memory element except for testing, it must be done to allow diagnostic analysis.

For easy access, the self-test code should be included with the application program. It usually will take up less than 1,024 bits of memory. Of course, the microprocessor must have some sort of ready access to the self-test program, such as an on-board switch or jumper. To enhance user confidence in the system, it is a good idea to program the execution of the self-test to occur at power-on reset.

Self-test considerations

If resident self-testing is not feasible, then the system should include an empty ROM socket and address decoding for access to it. Room for one 2-K-by-8-bit ROM should be ample.

If no socket can be left empty, then there must be allowance for a decode-disable signal from the tester. Such a signal can overlay the self-test program onto the application program. Unfortunately, any overlaid memory space cannot be tested, so the overlay should occupy the smallest possible block of memory.

Input/output ports should be designed so that outputs can be routed into inputs with a special test connector, permitting a highly effective I/O test. Many serial-communications peripheral chips, like the National 8250 asynchronous-communications part, have a programmable loop-back mode supporting this kind of test.

An important design aid to self-testing is functional partitioning of the microcomputer, which, in fact, is inherent in bus-oriented architectures and can be virtually an automatic design procedure when assigning various system components to memory or I/O addresses and connecting them to the bus.

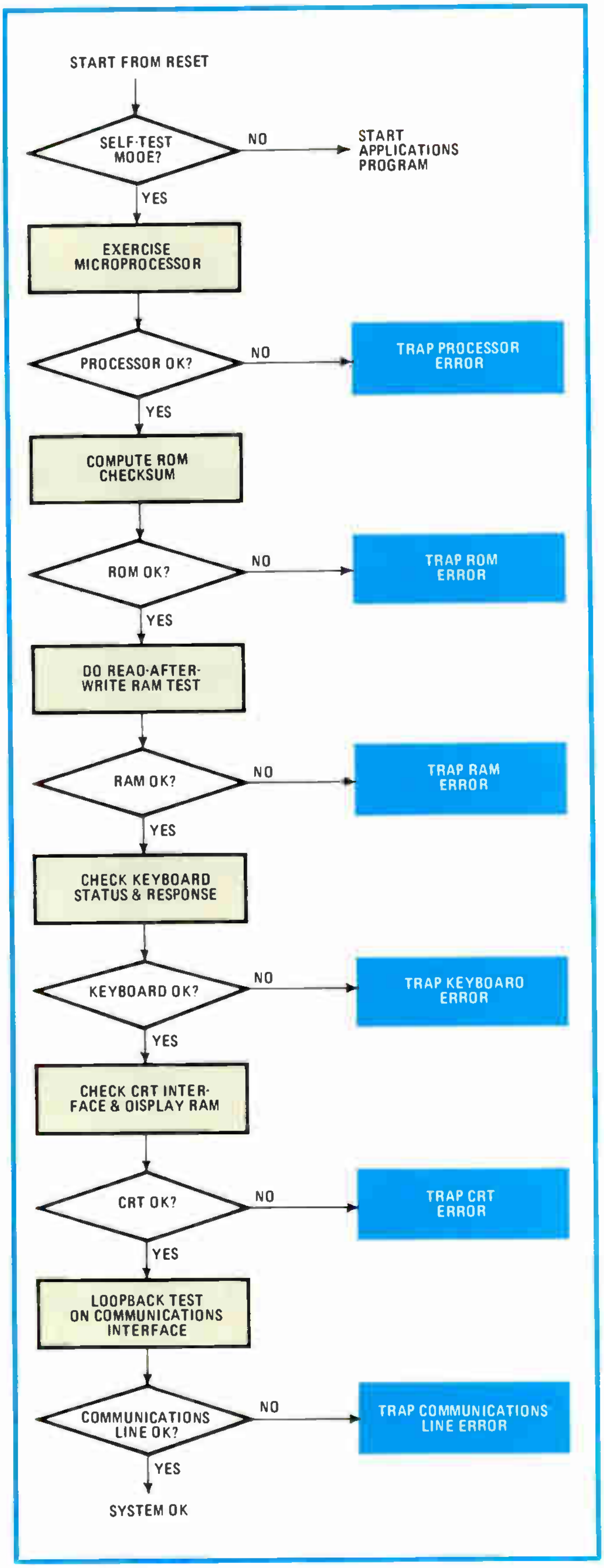
Then, the self-test program can be arranged in modules according to the functional partitioning (for example, separate test modules for a ROM test, a RAM test, a peripheral-interface-adapter test, and so on). These modules should run one at a time for system verification (Fig. 6), or else they should execute repetitively to provide continuous stimulus for fault diagnosis. Such looping test modules also are useful for finding intermittent faults.

Some test modules can be general-purpose, for use in many systems. The Intel diagnostic routines written to test the SBC 80/10 single-board computer are excellent examples of such modules. The routines include CPU, RAM, ROM, and I/O tests.

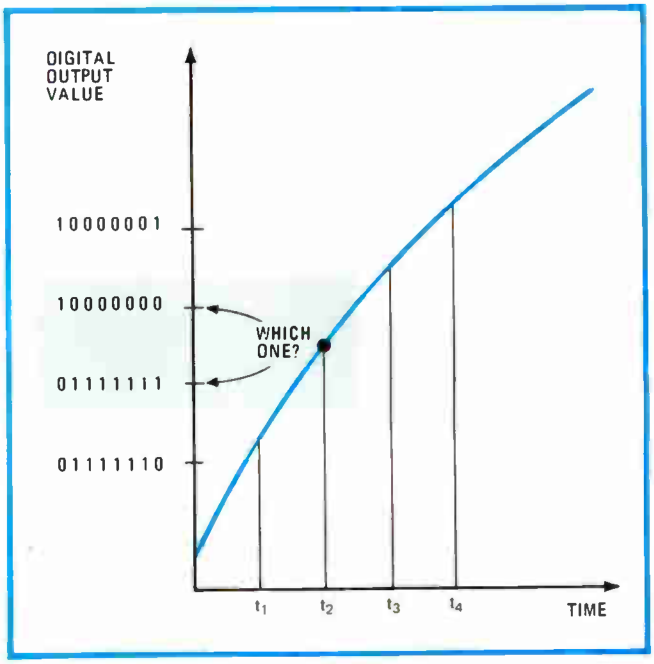
If modules in the application program are written as subroutines, they can be called by the self-test program, thereby saving code space. A good example is using the I/O driver routines from the main program.

Every system should have adequate timing margins that minimize soft failures. Soft failures come and go depending on temperature, noise, and other system parameters. They are among the most difficult and time-consuming faults to diagnose, and their appearance in any great number can virtually bring a production line to a halt.

More and more brand-new components are being



6. System self-test. A microcomputer's self-test program examines each functional module on the board. The diagnostic priorities of the self-test work to isolate the module in which the fault occurs by checking all modules in order and noting which are error-free.



7. Which one? Since analog-to-digital converters have an inherent uncertainty of ± 1 bit, analog inputs of the same voltage can produce different digital outputs. This characteristic will present special problems when doing the testing of microprocessor-based boards.

designed into products today. These new devices are often incompletely characterized when first available. Thus they should be used conservatively, especially with respect to timing specifications.

The boundaries between the exact digital world and the approximate analog world present special testing problems. Digital-to-analog conversion offers no problem, but analog-to-digital converters can have an inherent uncertainty. For the same input voltage, one converter could produce 01111111 and another one 10000000, although both are operating within analog specifications (Fig. 7). Although the possible output values will be close to nominal, it is very difficult to measure the difference in real time.

Alternative solutions

One solution to this problem is to test a-d converters separately from the system to see if they meet specifications. The design rule here is to provide access to the converter's output so that a known value can be inserted to test the digital part of the system. Another alternative is to underdrive and overdrive the analog input and look for all 0s and 1s respectively.

Microprocessors allow design of amazingly compact and aesthetic products, but when it comes to service, small is not always beautiful. It is important to avoid letting a package get so small or fancy that it becomes very difficult to service.

Also, it is wise to avoid using a collection of dissimilar microprocessors simply to obtain technical nuances. Families of microprocessors and microcomputers are designed to work together through common instruction sets, hardware, architectures, and timing requirements. A design built around similar processors will be much easier to test than a design involving different ones. □

Standard ICs provide raster scan interface

by Serge Poplavsky
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One master oscillator and a few counters, flip-flops, and gates make a baud-rate clock with a sync generator that produces horizontal and vertical pulses for noninterlaced raster scanning of a cathode-ray tube. In it, standard integrated circuits are used to generate rates up to 38.4 kilobauds (the upper limit of most generators is only 9,600 bauds) and sync pulses for producing 312 lines at a 50-hertz refreshing rate (or 260 lines for a 60-Hz rate). Thus the circuit is a low-cost solution to building an important part of any data terminal.

All clock rates are derived from one crystal-controlled oscillator, A_1, which uses the 7209 and a crystal cut for 7.9872 megahertz. The master clock frequency is then divided by 13 by A_2, the 74LS161 presettable counter. A_2 generates a frequency 16 times 38.4 kilobauds, suitable for interfacing with universal asynchronous receiver-transmitters or similar modems.

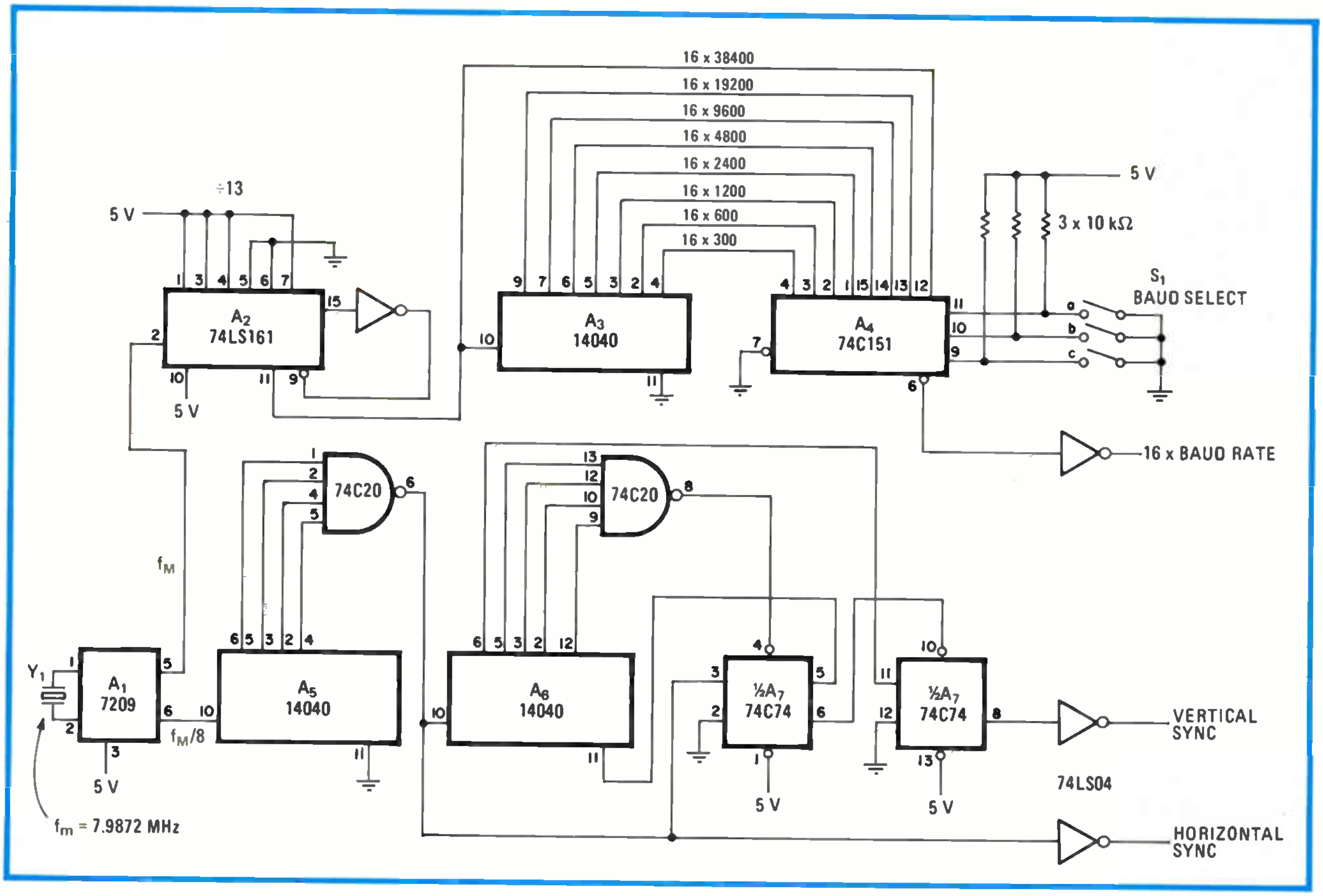
This frequency is further divided by A_3, the 14040 binary counter. Thus, rates extending from 16×300 bauds to 16×19.2 kilobauds will appear at its output.

S_1, which is used in A_4, the 74C151 one-of-eight-line multiplexer, selects the baud rate desired. When all switches are open, a rate of 300 bauds is selected. Closing switch a, the least significant bit (i.e., binary number 1), selects a baud rate of 600, and so on.

The horizontal sync pulses for the cathode-ray tube are derived from A_5 and a four-input NAND gate, which generates a frequency of 15,600 Hz, each pulse lasting 4 microseconds. The vertical sync frequency, either 50 or 60 Hz, is obtained from A_6–A_7 and a four-input NAND gate.

Dividing the horizontal sync pulses by 312 or 260 (for 50 or 60 Hz, respectively), the binary counter, A_6, which in this case is wired as a divide-by-312 device, drives two flip-flops (A_7). A_7 resets the counter and generates vertical sync pulses, each 256 μs long. □

Designer's casebook is a regular feature in Electronics. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published.



Versatile. Using standard integrated circuits, combination baud-rate generator and sync generator for CRT works up to 38.4 kilobauds and can be wired to generate sync pulses suitable for a 50- or 60-Hz refreshing rate. All frequencies are derived from one oscillator.

Gates replace PROM in Intellec-8 bootstrap loader

by Simon Gagné and Bernard Boulé
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In what may be the most cost-effective solution yet for implementing a bootstrap loader for Intel's popular Intellec-8 development system, logic gates are used to replace the jump-to-monitor routine stored in a programmable read-only memory (PROM).[1] This simple method of automatically accessing the system's monitor, or executive-control routines, is possible because the set of 8-bit logic signals required at the data bus to access the monitor on power-up can be easily generated.

In the Intellec-8, the monitor is located at address 3800 (hexadecimal). Therefore, a jump instruction is used to advance the program counter from location 0 to 3800H. To avoid the manual programming required after each power-up, the previous solution was to use a PROM programmed with the instruction (C3 00 38).

The logic signals required on data bus lines D_0–D_7 for achieving the three-byte jump instruction are shown in Fig. 1a. The output of each flip-flop in the three-stage 74175 shift register, previously used to enable the PROM, together with simple logic, can synthesize this sequence.

When the outputs of the shift register (Q_1, Q_2, and Q_3) alone are stepped with system clock $\overline{DBIN}$, they generate the signal pattern shown in Fig. 1b. Comparison of Fig. 1a and 1b reveals that the identical patterns of lines D_0–D_1 and D_6–D_7 can be generated by forming the logic function $\overline{Q}_1 + Q_3$. It is also seen that bits D_3, D_4, and D_5 are identical to the Q_2 output of the shift register and the D_2 bit is identical to the Q_3 output, so that the Q_2 and Q_3 signals can simply be connected to these corresponding data lines through noninverting buffers. To make the final circuit, which appears in Fig. 2, operational, switch S_1 need only be placed in the monitor position for automatic loading on power-up. □

References
1. "PROM adds bootstrap loader to Intellec-8 development system," *Electronics*, April 27, 1978, p. 126.

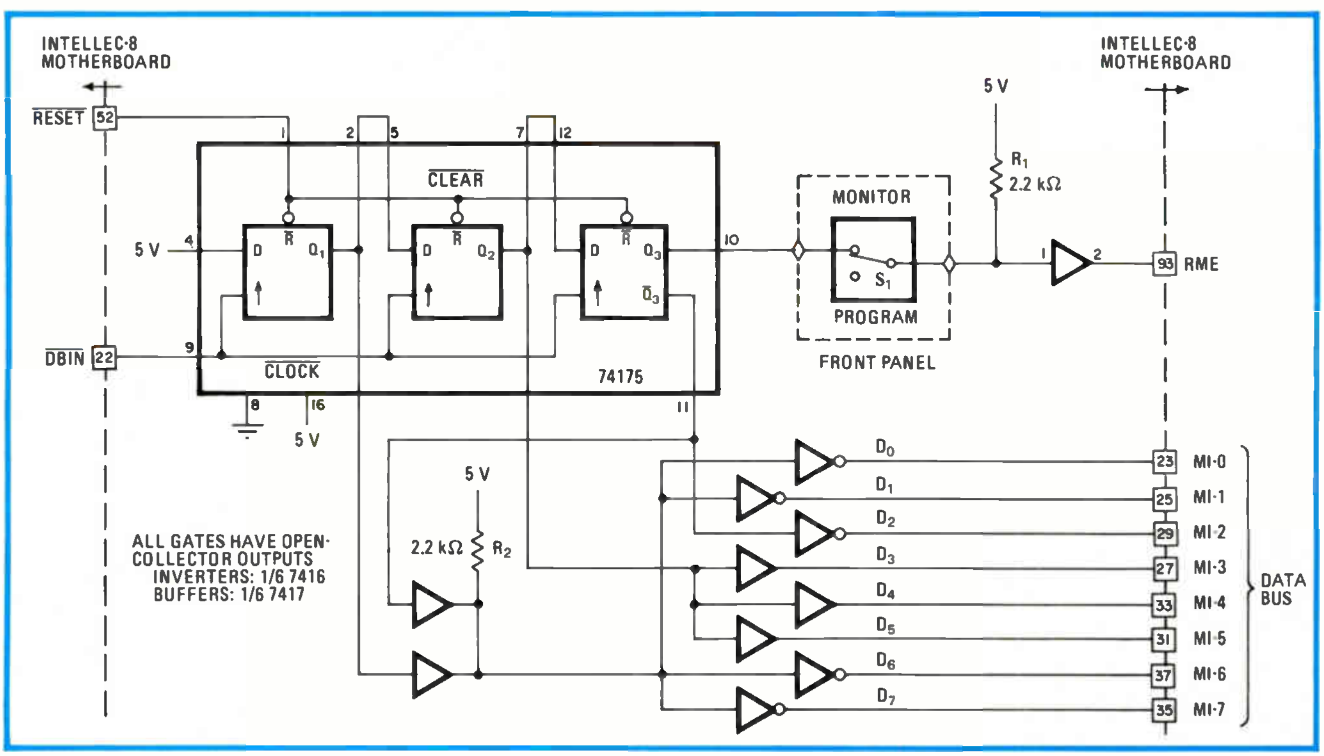
Instruction	Op code	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
JMP 3800H	C3	1	1	0	0	0	0	1	1
	00	0	0	0	0	0	0	0	0
	38	0	0	1	1	1	0	0	0
(AFTER JMP)	FF	1	1	1	1	1	1	1	1

(a)

Condition	Q_1	Q_2	Q_3
RESET	0	0	0
AFTER FIRST $\overline{DBIN}$	1	0	0
AFTER SECOND $\overline{DBIN}$	1	1	0
AFTER THIRD $\overline{DBIN}$	1	1	1

(b)

1. Synthesis. Table outlines logic sequence required on data bus for achieving jump operation in order to enter Intellec-8's executive program (a). Outputs of clocked three-stage shift register of basic circuit generate signals (b), which can be used to synthesize D_0–D_1 and D_6–D_7 signals if function $\overline{Q}_1 + Q_3$ is formed with logic gates. Q_2 output is by itself identical to D_3, D_4, and D_5. Q_3 output is identical to D_2.



2. Implementation. Circuit for accessing system's monitor uses open-collector logic gates, which replace programmable read-only memory in original configuration. Circuit is armed by placing front-panel switch S_1 in monitor position before each power-up of system.

Circuit phase-locks function generators over 360°

by Lawrence W. Shacklette
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This circuit locks a low-cost function generator without a voltage-controlled-oscillator (VCO) input to a second inexpensive generator having such a phase-reference feature. A J-K flip-flop, two one-shots, two comparators, and an operational amplifier are linked in a feedback arrangement that includes the programmable generator as the VCO in a phase-locked loop (PLL). The resultant circuit provides a selectable phase shift between generator outputs over the range of 0° to 360°.

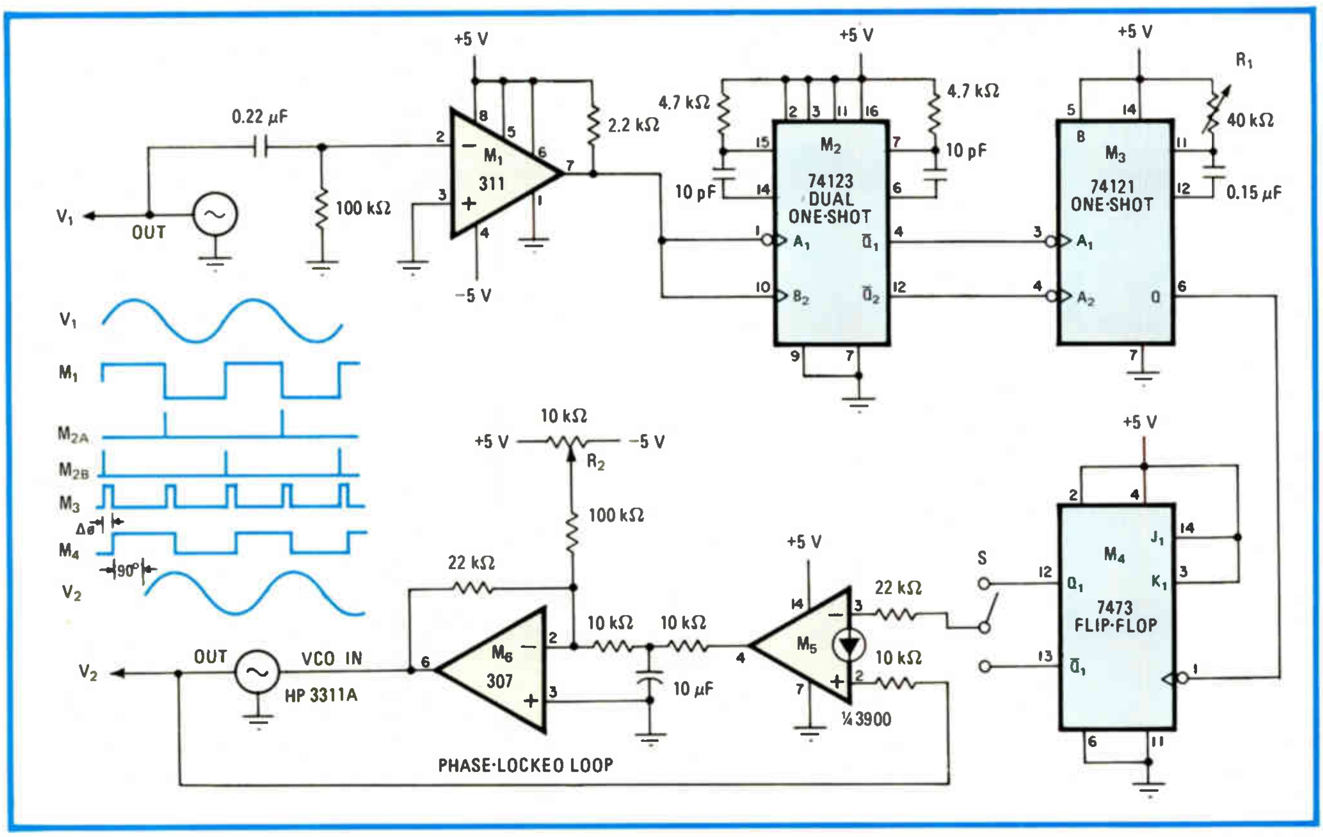
In operation, the output of the low-cost generator, v_1, passes through a high-pass filter to a zero-crossing detector that employs a 311 comparator (M_1), as shown. A dual monostable multivibrator and J-K flip-flop follow. Although these two devices can be eliminated, they enable the phase-locked loop to be operated at the center of its locking range for any phase shift. This arrangement ensures that two often desired phase angles, 0° and 180°, fall within the capture range of the PLL, so that if locking is lost, it will be automatically regained.

The outputs of the dual one-shot, M_2, wired so that each fires on opposite edges of the signal applied to its inputs (see timing diagram), are fed to the OR input of M_3, whose on time is selected by potentiometer R_1. Thus R_1 controls the amount of phase shift.

M_3 produces two pulses for each cycle of v_1 and triggers the J-K flip-flop, M_4, on each negative edge. The flip-flop thus produces a square wave with a frequency equal to v_1, but shifted in phase by up to 180°. An additional shift of 180° can be obtained by using switch S to connect the Q output of M_4 to the inverting input of the 3900 Norton amplifier.

The adjustable-phase square wave serves as a reference signal for the phase-locked loop, which is composed of the 3900, a low-pass filter, a buffer (307), and a VCO (the second function generator, a Hewlett-Packard 3311A). The input signal to the VCO is a negative dc voltage that is the inverted sum of the filtered output of the 3900 and the voltage selected by the offset control, R_2. By turning the generator's front-panel control or R_2, the free-running frequency of the loop can be adjusted.

Because the reference signal is a square wave, the PLL will lock onto either the fundamental of v_1 or its odd harmonics. Selection of a particular harmonic is made by adjusting the free-running frequency to the approximate value of the harmonic desired. Half-multiple harmonics ($\frac{1}{2}f_1$, $\frac{3}{2}f_1$, $\frac{5}{2}f_1$, etc.) can be produced at v_2 by breaking the $\overline{Q}_1$–A_1 connection between M_2 and M_3 and tying A_1 to +5 volts. Even harmonics can be obtained by using the remaining flip-flop in the 7473 as a divide-by-2 counter, and placing it between the output of the VCO and the 3900's noninverting input. □



Phase-locked. Comparators, one-shots, and flip-flop combine to provide stable locking of generators without phase-reference feature to those having a VCO input. R_1 and S are used to select phase of v_2 with respect to v_1; phase can be adjusted from 0° to 360°. M_2 and M_4 ensure that locking is regained if it is lost, and R_2 controls lock frequency, which may be set to integer or half-integer harmonics of v_1.

Converting digital data into color television graphics

Video-display generator chip simplifies the interface between microprocessors in computers or video games and a TV receiver

by Mitch Goozé* and James Farrell, *Motorola Inc., Semiconductor Group, Austin, Texas*

☐ By using the consumer's color TV set as a display, the most expensive component of video games and personal computers can be eliminated. Although this approach may be advantageous from a marketing standpoint, it can be a designer's nightmare, especially if the add-on device contains a microprocessor.

A typical interface between a TV set, which requires a radio-frequency analog input, and an intelligent game or home computer that uses digital logic could require as many as 25,000 transistors or 280 small- or medium-scale integrated circuits. In an effort to reduce the amount of hardware in the interface, several integrated-circuit manufacturers have condensed the digital-to-video function onto one large-scale integrated chip.

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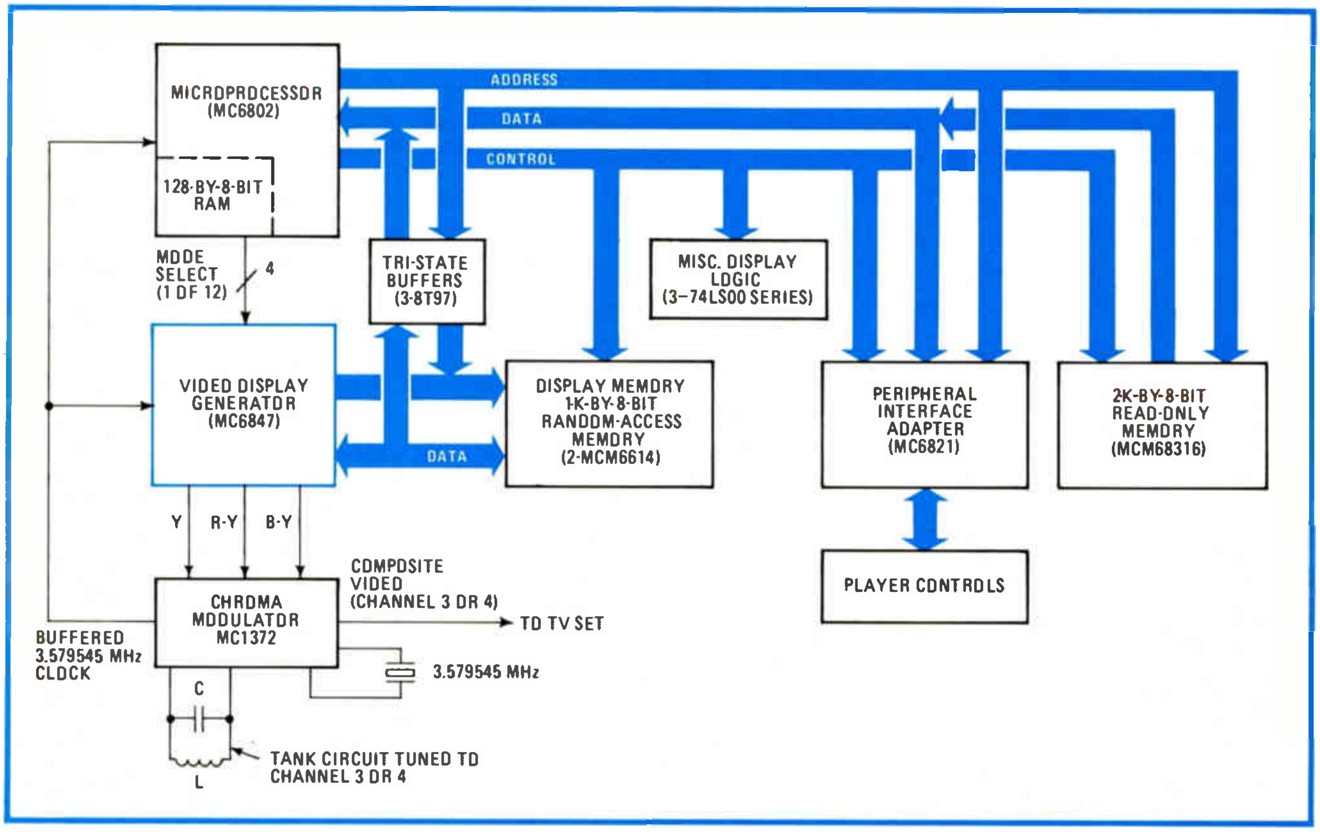
A video-display generator (VDG) reads digital data from a microprocessor-controlled random-access display memory (sometimes called a refresh memory) and converts it into analog video waveforms that contain brightness and color information. The waveforms are synchronized with the TV raster by adding timing pulses. These signals then go to a chroma modulator, which encodes them into a composite rf signal that replicates a TV transmission on Channel 3 or 4.

This article describes the operation of one such video-display-generator chip, Motorola's n-channel metal-oxide-semiconductor MC 6847, within a microprocessor-controlled video game. Operation of the chip within a game is governed by the National Television System Committee Standard; this standard defines the format



1. Video generator. In a "smart" video game, the microprocessor transfers data from the display memory to the video-display generator, which converts it to video waveforms. ROM stores object codes; the peripheral interface adapter links the electronics with the players.

Playing by the rules

In 1953, the National Television System Committee established the specifications of color television signals. The NTSC, in response to the need for compatible signals for color and black-and-white receivers, decided that color-defining signals should ride on a subcarrier that is 3.579545 MHz above the brightness-modulated carrier. This guarantees separation of brightness (luminance) and color (chrominance) information and, therefore, the separability of the two signals by detector(s) in any TV set. Black-and-white TVs detect the luminance signal and ignore the chrominance signal. Color TV sets look first at the luminance signal for how much light is at a certain point on the screen, then at the chrominance signal for how much of that light is red, blue and green.

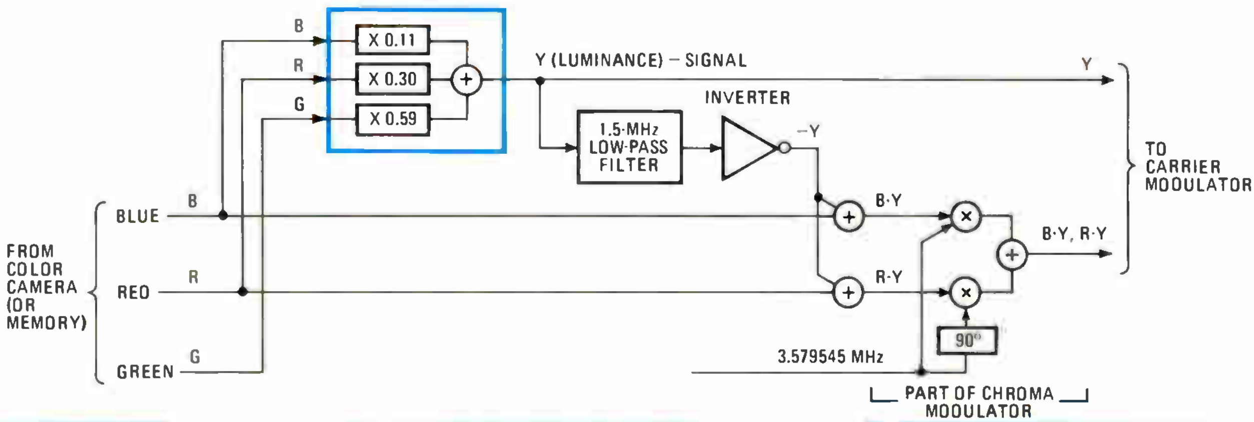
Having determined how TV signals would carry color information, the NTSC then examined how much resolution the color picture could have. The tradeoff here is resolution for bandwidth. To define a high-resolution pattern of rapidly changing colors requires a high-frequency signal, which in turn requires a wide-bandwidth transmission. But the bandwidth of each TV channel is only 6 MHz. Within this limited bandwidth, it would appear that, since fast color changes over small areas cannot be transmitted, tiny objects on the screen would appear colorless.

But during its research the NTSC studied the resolving characteristics of the human eye and found that the eye's ability to perceive color decreases as the viewed area becomes smaller. For small objects, the eye cannot detect color, but the brain "fills in" a color from the surrounding area. This is why the 6 MHz bandwidth provides adequate resolution for color TV graphics: for larger areas, a low-frequency signal defines color, while smaller areas are transmitted essentially in black and white.

The NTSC also studied the frequency response of the eye and found that the eye is sensitive to color in the following proportion: $Y = 0.59G + 0.11B + 0.30R$, where Y is the total brightness of the light, and G, B and R represent its green, blue and red components. Since brightness, as measured by the monochrome signal, is already part of a black-and-white transmission, the NTSC's finding meant that only two of the three color signals have to be sent. The remaining signal can be derived in the receiver by subtracting the other two signals from the monochrome signal in accordance with the above equation. In practice, the circuit in the diagram generates the color signals in a TV transmitter (or VDG chip).

The blue, red and green signals from a color camera (or display memory) are summed in proportion to produce the luminance signal Y. After it passes through a 1.5-MHz low-pass filter and an inverter, Y then is subtracted from the blue and red signals and sent off to frequency-modulate the carrier. The green signal is dropped, while the B-Y and R-Y signals each phase-modulate a 3.579545-MHz subcarrier at different angles, as shown. This puts the two signals in quadrature, which means that their phasor representations are 90° apart. Since the magnitude and phase of their resultant, or vector sum, changes as the relative amplitudes of the two signals vary, one composite video signal suffices to define two colors.

When the signal reaches the receiver, the luminance signal is detected and added to the demodulated R-Y and B-Y signals to recover the red and blue components of the light. The red and blue signals then are subtracted proportionately from Y to obtain green.



and bandwidth of television broadcast signals used in the U. S. (see "Playing by the rules," above). Since a video-game output must duplicate a TV transmission, the NTSC standard also determines the characteristics of the video waveforms and synchronization signals generated by the VDG chip, and the maximum display resolution possible within the channel bandwidth.

The price of versatility

There are two popular system architectures for video games that use microprocessors to generate and control graphic-character dot patterns or objects: object-oriented and random-access-memory–intensive. In an object-oriented system, a fixed set of graphics characters is stored in read-only memory. These objects are accessed by the microprocessor and transferred directly to the screen through the VDG and the chroma modulator. Object size and resolution depend on the system clock frequency, with faster systems yielding smaller objects and higher display resolution.

In this system, the microprocessor moves an object with two degrees of freedom by changing its coordinates in internal horizontal- and vertical-position registers. Complex movements like rotation require more sophisticated programming. For example, in a military game rotating the image of a tank would require storage of

SUMMARY OF OPERATING MODES OF THE 6847 VIDEODISPLAY GENERATOR					
MODE NAME	TV SCREEN FORMAT			VDG DATA BUS (MSB — LSB)	REQUIRED DISPLAY-RAM SIZE (BITS)
	NUMBER OF COLORS	DISPLAY-ELEMENT MATRIX	ELEMENTAL DETAIL, IN DOTS		
INTERNAL ALPHANUMERIC	2	32 WIDE BY 16 HIGH	8 wide, 12 high (5, 7)	SPARE, ASCII CODE	512 BY 8
EXTERNAL ALPHANUMERIC	2	32 WIDE BY 16 HIGH	8 wide, 12 high	(CUSTOM CHARACTERS)	512 BY 8
SEMIGRAPHIC-4	8	64 WIDE BY 32 HIGH	4 wide, 6 high: L_3 L_2 / L_1 L_0 (ONE ELEMENT)	$C_3\ C_2\ C_1\ C_0\ L_3\ L_2\ L_1\ L_0$	512 BY 8
SEMIGRAPHIC-6	8	64 WIDE BY 48 HIGH	4 wide, 4 high: L_5 L_4 / L_3 L_2 / L_1 L_0	$C_1\ C_0\ L_5\ L_4\ L_3\ L_2\ L_1\ L_0$	512 BY 8
64 BY 64 COLOR GRAPHIC	8	64 WIDE BY 64 HIGH	4 wide, 3 high: $E_3\ E_2\ E_1\ E_0$	$C_1\ C_0\ C_1\ C_0\ C_1\ C_0\ C_1\ C_0$	1024 BY 8
128 BY 64 GRAPHIC	2	128 WIDE BY 64 HIGH	2 wide, 3 high: $L_7\ L_6\ L_5\ L_4\ L_3\ L_2\ L_1\ L_0$	$L_7\ L_6\ L_5\ L_4\ L_3\ L_2\ L_1\ L_0$	1024 BY 8
128 BY 64 COLOR GRAPHIC	8	128 WIDE BY 64 HIGH	2 wide, 3 high: $E_3\ E_2\ E_1\ E_0$	$C_1\ C_0\ C_1\ C_0\ C_1\ C_0\ C_1\ C_0$	2048 BY 8
128 BY 96 GRAPHIC	2	128 WIDE BY 96 HIGH	2 wide, 2 high: $L_7\ L_6\ L_5\ L_4\ L_3\ L_2\ L_1\ L_0$	$L_7\ L_6\ L_5\ L_4\ L_3\ L_2\ L_1\ L_0$	1536 BY 8
128 BY 96 COLOR GRAPHIC	8	128 WIDE BY 96 HIGH	2 wide, 2 high: $E_3\ E_2\ E_1\ E_0$	$C_1\ C_0\ C_1\ C_0\ C_1\ C_0\ C_1\ C_0$	3072 BY 8
128 BY 192 GRAPHIC	2	128 WIDE BY 192 HIGH	2 wide, 1 high: $L_7\ L_6\ L_5\ L_4\ L_3\ L_2\ L_1\ L_0$	$L_7\ L_6\ L_5\ L_4\ L_3\ L_2\ L_1\ L_0$	3072 BY 8
128 BY 192 COLOR GRAPHIC	8	128 WIDE BY 192 HIGH	2 wide, 1 high: $E_3\ E_2\ E_1\ E_0$	$C_1\ C_0\ C_1\ C_0\ C_1\ C_0\ C_1\ C_0$	6144 BY 8
256 BY 192 GRAPHIC	2	256 WIDE BY 192 HIGH	1 wide, 1 high: $L_7\ L_6\ L_5\ L_4\ L_3\ L_2\ L_1\ L_0$	$L_7\ L_6\ L_5\ L_4\ L_3\ L_2\ L_1\ L_0$	6144 BY 8

several tank patterns at various angles.

Object-oriented systems allow more objects to be controlled more easily (by simply changing their position in registers) than RAM-intensive systems. They also require less RAM, so system cost is lower. However, RAM-intensive systems offer greater flexibility of what can be put on the screen.

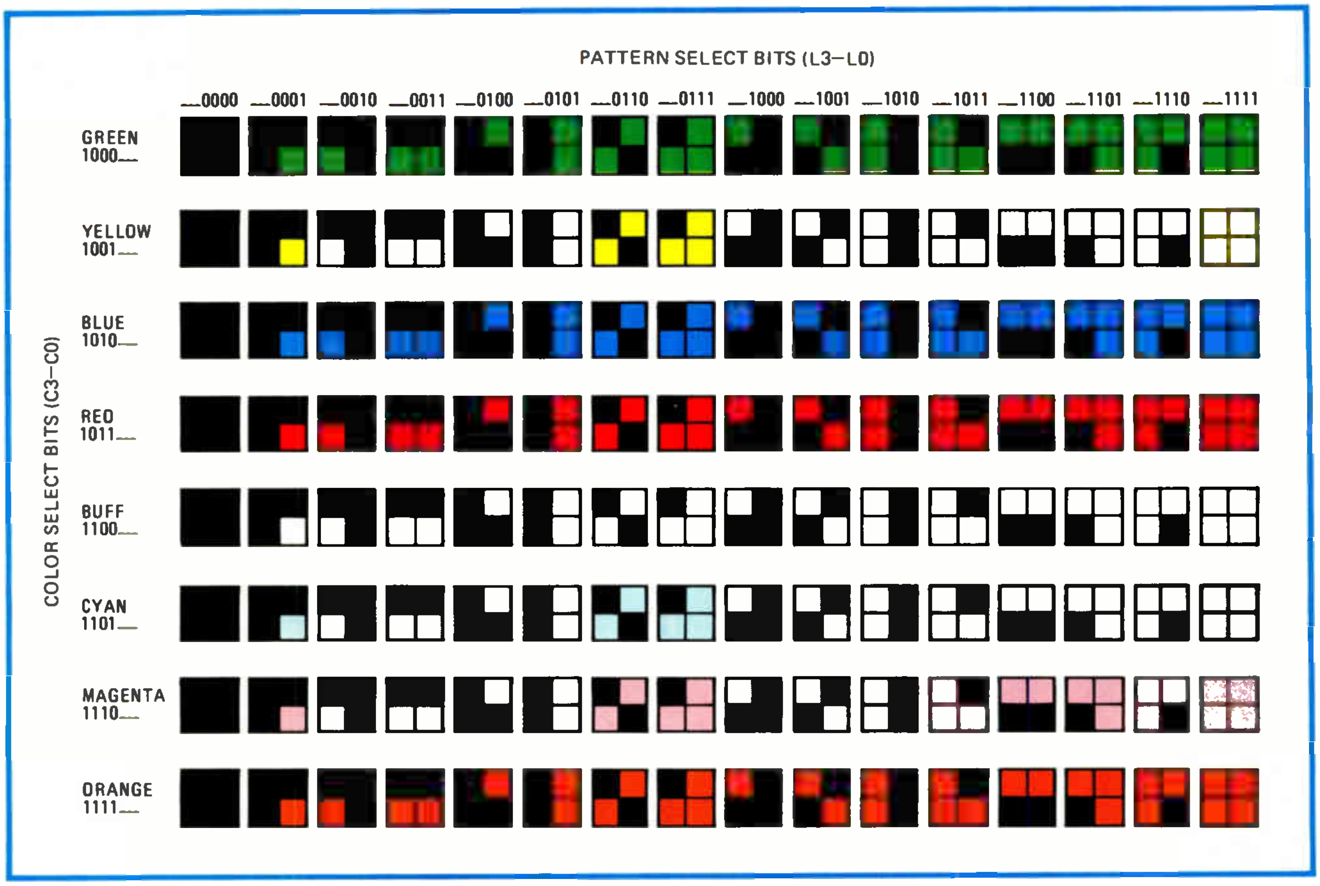
RAM-intensive systems use a technique called direct memory mapping. Here, as Fig. 1 shows, the VDG sequentially reads 8-bit bytes of data that represent strings of horizontal dots from the display memory, mapping its contents directly onto the screen. To change the picture, the microprocessor simply updates the appropriate lines in the display memory.

The ease of changing the display makes RAM-intensive systems attractive. But because display resolution is a function of display memory size, higher resolution translates into higher system cost. By combining the advantages of both the object-oriented and RAM-intensive methods, the MC 6847 reduces the game's memory requirements and cost with no loss of display resolution or control flexibility.

Subdividing the screen

The MC 6847 video-display generator can operate in 12 different display modes: two alphanumeric modes, two semigraphic modes, and eight full-graphic modes (see table). Each mode is selected by the microprocessor and arranges the display area, which is 256 dots wide and 192 dots high, into a matrix of boxes or elements. The contents of each box vary—from an 8-column, 12-row dot matrix in the least dense (alphanumeric) modes to a single dot in the highest-resolution graphic mode. Choice of color for all illuminated dots in each box also varies by mode, from one of two to one of eight.

A RAM-intensive game requires a display RAM large



2. Colorful. The VDG divides each 8-by-12-dot display element into four boxes in the semigraphic-4 mode. The four least significant bits of each incoming data word select one of sixteen possible patterns of illumination; the four most significant bits determine color.

enough to store all 49,152 dots of one 256-by-192-dot TV frame. Therefore, the amount and cost of RAM needed to implement a particular VDG mode are a function of how many dots a data word controls in that mode. In the least dense mode, each 8-bit byte controls 96 dots, so a 512-by-8-bit display RAM is required. In the highest-resolution mode, each byte controls 8 dots (one per bit), so the required RAM size goes up by a factor of 12 to 6144 by 8 bits.

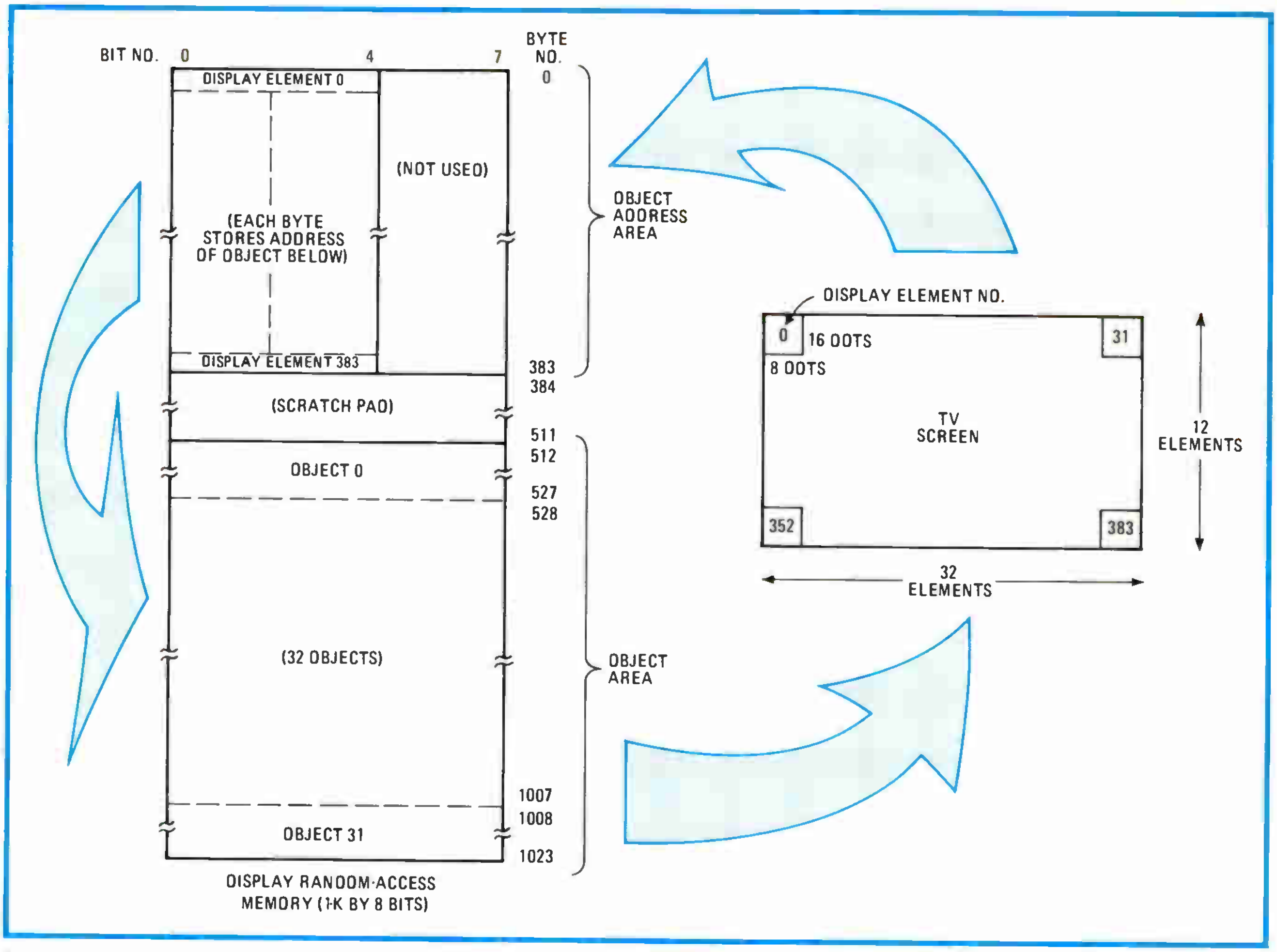
Both alphanumeric modes divide the screen into a 32-column, 16-row matrix of character boxes. Each box is 8 dots wide and 12 dots high and contains one character. In the internal alphanumeric mode, a read-only memory inside the VDG generates 1 of 64 characters in a 5-by-7-dot pattern that fits inside the 8-by-12-dot box. The 6 least significant bits of each data word contain the ASCII code for the character. The remaining two bits are spare; they could be used to select, for example, an orange or green character on a black background, or the inverse, by tying them to the color-set-select (CSS) and inverse-video (INV) pins of the VDG. Another possibility is to tie one of the spare-bit lines to the VDG's INT/EXT pin, thus allowing selection of an external character ROM.

In the external alphanumeric mode, an external ROM generates 1 of up to 256 custom characters in the 8-by-12-dot box. As in the internal alphanumeric mode, each data word defines 96 dots, so either alphanumeric mode requires 512 bytes of display RAM.

The two semigraphic modes are designated semigraphic-4 and -6. In the semigraphic-4 mode, each 8-by-12-dot character box is divided into four elements (Fig. 2). The four least significant bits (L3–L0) of the internally generated data word select 1 of 16 patterns of element illumination, while three of the four most significant bits (C2–C0) select one of eight colors for the illuminated dots. In this mode, the screen becomes a 64-by-32-element display, with each element 4 dots wide by 6 dots high. Each data word controls four of the 2,048 24-dot elements, so the mode requires a 512-byte RAM.

In the semigraphic-6 mode, each 8-by-12-bit box is divided into six elements. The 6 LSBs of the data word, which comes from an external ROM, select 1 of 64 patterns of element illumination. The two MSBs select one of four colors for the box. In addition, the CSS pin can be used to select either of two 4-color sets. Here, the screen becomes a 64-by-48-element matrix, with each element 4 dots wide by 4 dots high. Each data word controls six of the 3,072 16-dot elements, so a 512-byte RAM is needed. The INT/EXT pin is used to select the semigraphic-4 or -6 mode.

In addition to the alphanumeric and semigraphic modes, the MC 6847 also operates in eight full-graphic modes, whose element formats and memory requirements are summarized in the table. Note the increasing RAM requirements as resolution and control increase through the graphic modes. For example, the densest modes—the 128-by-192-element color graphic and 256-



3. Indexing. In indirect mapping, each display element is assigned a byte in the display memory. This byte points to an object below. Compared with direct mapping, this hybrid architecture requires memory that is twice as fast, but only one sixth the size.

by-192 graphic—require 6,144 by 8 bits of RAM. Also note the absence of a 256-by-192 color graphic mode, due to the NTSC's finding that the eye cannot distinguish colors of small objects like individual dots.

The best of both worlds

To reduce the amount of RAM required for its denser display modes, the MC 6847 operates in a hybrid system architecture. Called indexing, this approach offers the advantages of both object-oriented and RAM-intensive systems, while cutting RAM requirements for the high-density graphic modes from 6,144 by 8 bits in RAM-intensive systems to 1,024 by 8 bits. The hybrid architecture has a disadvantage, however: although it requires a sixth the memory, the memory must be twice as fast.

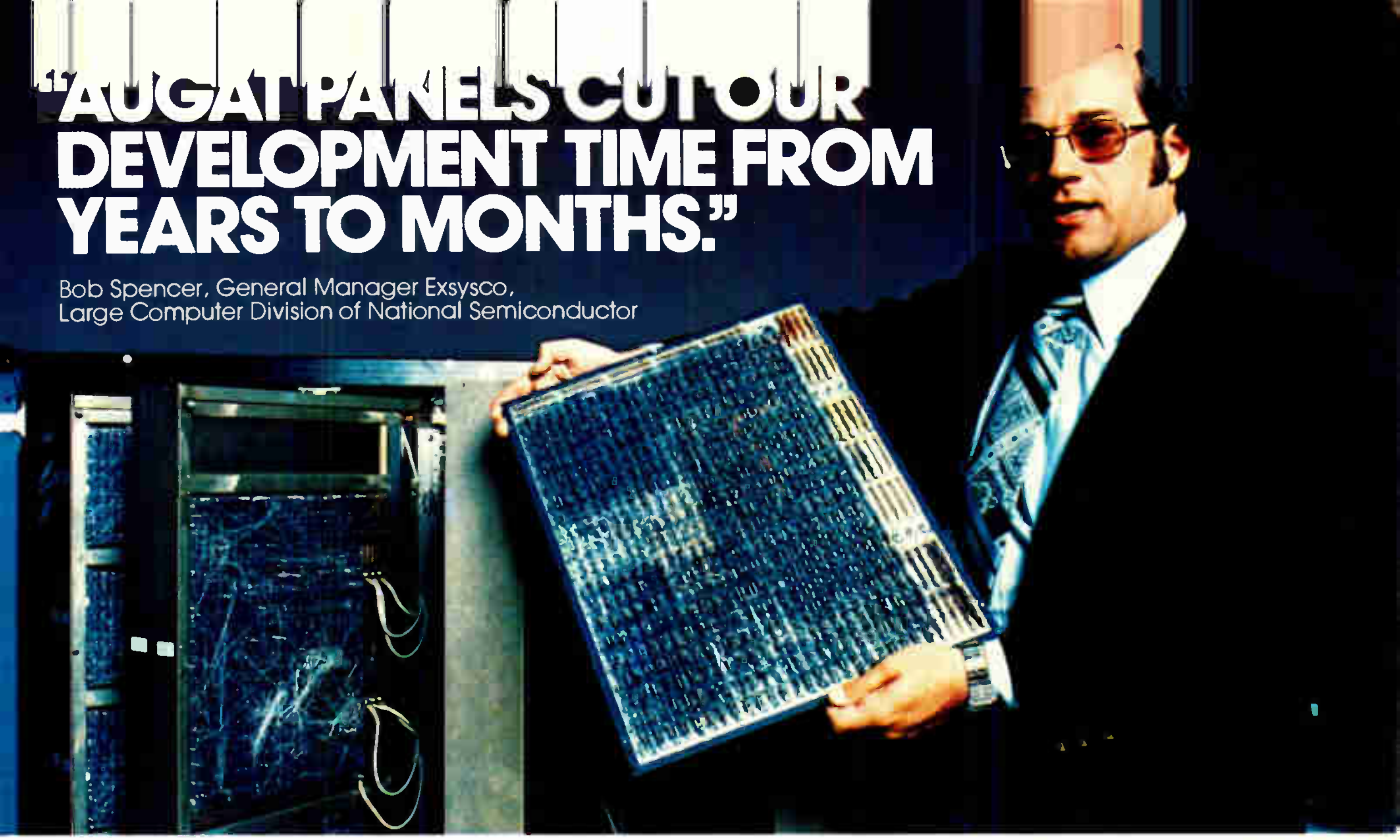
The indexing system uses a technique called indirect memory mapping. Here, the display area is arranged in a 32-by-12-element matrix, with each element an 8-by-16-dot box. Thus the screen contains 384 elements which are numbered from 0 in the upper left-hand corner to 383 at the lower right (Fig. 3). Each box is assigned a byte in the upper half of a 1,024-by-8-bit display RAM. The lower 512 bytes contain the codes for 32 objects; the remaining 128 bytes are used as a scratchpad during computations.

Accelerated timing is the key to the indexing approach. Normally, the system takes four cycles of the 3.58-megahertz clock to deliver one byte of data to the VDG. But by multiplexing the display memory's address lines, it can be accessed twice as often in what is called a double fetch.

During the first two cycles of the clock, the VDG addresses the RAM location assigned to the element being scanned by the electron beam. This location contains the address of the 16 bytes in RAM below, which define the object to be displayed in that screen element. The object's address is latched at the end of the first two cycles, then applied back to the RAM at the start of the next two, when the object code is sent to the video-display generator.

This procedure repeats until all 384 elements are scanned. To change the screen position of an object, the microprocessor changes its address pointer in the upper 384 bytes of display RAM. One of the objects is typically background (no object); the remaining ones are selectable in one of four colors.

Since the display memory is accessed twice as often in this system, RAM access-time requirements change from 450 nanoseconds for a RAM-intensive system to 200 ns using this approach. The cost of this doubling in memory speed is more than offset by the 6:1 reduction in size of memory required for high-resolution operation. □



"AUGAT PANELS CUT OUR DEVELOPMENT TIME FROM YEARS TO MONTHS."

Bob Spencer, General Manager Exsysco,
Large Computer Division of National Semiconductor

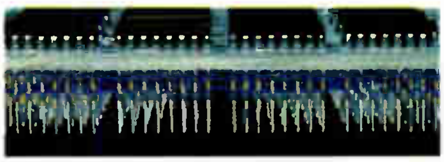
The dynamics of the computer industry demands that manufacturers capitalize on opportunities during the limited lifespan of the "current" technology. That's why initial development time is crucial. One sure way to cut that time is with Augat Wire-Wrap* panels. Bob Spencer explains: "Multi-layer boards meant a lead time of a year or more to design and prototype with another six months to get into production. With Augat boards, we reduced this cycle to a few months and started production the day we approved the prototype. Augat also gave us a flexibility to make circuit changes during the development cycle without causing delays."

Time isn't the only consideration—cost is also critical. "The expense to design and develop dozens of different, large multi-layer boards can easily run into the hundreds of thousands of dollars, not to mention staffing and equipment. The Augat approach drastically reduced these costs allowing us to concentrate our resources on other critical design elements."

Packaging density is also vital in evaluating interconnection alternatives. "The multi-layer approach, with boards of typically 475 IC's, would have required 15 layers to achieve the same density that Augat gave us."

National builds the Advanced Systems™ 4 and 5 computers for ITEL. These systems must offer high reliability. "As the temperature inside a computer goes up, the reliability goes down. Augat boards reduce the temperature problem because Wire-Wrap pins are excellent radiators."

The benefits also carry into the field. "Thanks to Augat boards, service engineers can make any required changes using simple tools. And because the boards are designed with sockets, we make repairs or upgrade systems quickly by pulling the old chips and plugging in new ones. We also eliminated the cost and logistics of stccking hundreds of different, completed PC boards. Now we simply stock IC's."



How would Bob Spencer rate the performance of Augat Wire-Wrap panels? "Excellent! Our system uses high speed ECL throughout. Augat's patented logic panel, combined with unique automatic wiring from Augat's Datatex subsidiary, performs with no noise or transmission problems."

Throughout the computer industry, you'll find Augat boards at work in all kinds of logic applications delivering high speed performance and system flexibility at dramatic cost and time savings.

For further information, call Len Doucet at 617-222-2202. Or write Augat, Inc., 33 Perry Avenue, Attleboro, Massachusetts 02703.

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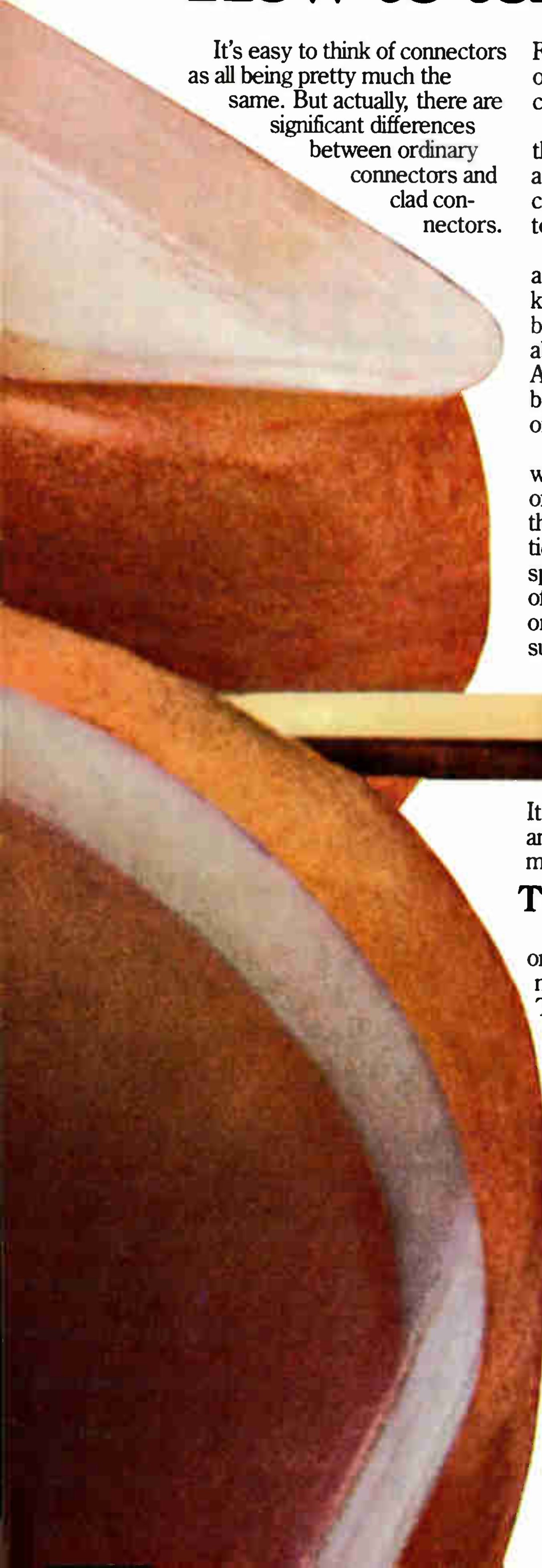
AUGAT®

Augat interconnection products, Isotronics microcircuit packaging, and Alco subminiature switches.

Circle 129 on reader service card

How to tell a clad connector



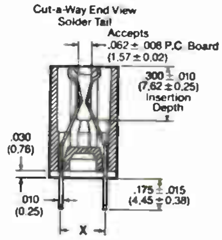
It's easy to think of connectors as all being pretty much the same. But actually, there are significant differences between ordinary connectors and clad connectors.

For example, the shortcomings of connectors with monometal contacts have long been known.

Alloys, though more versatile than monometals, haven't been able to provide the range of characteristics demanded by today's applications.

And most gold platings, such as flash gold, are too thin for any kind of durability. They tend to be porous and vulnerable to abrasion and intermittencies. And they're wasteful and costly, because you really need gold only at the point of contact.

The optimum solution, then, would be a combination of metals that provide the exact characteristics required for the specific application. As of today, there is only one way to produce such a combination.



It's a bonding process pioneered and developed by Texas Instruments. And it's called cladding.

The clad difference.

Basically, a clad metal is two or more metals bonded at the molecular level into a composite. There's no need for intermediate adhesives or brazing alloys. It's simple, it's clean and it's permanent.

In TI connectors, a strip of metal – the "contact" metal, usually gold – is bonded as a *50 to 75 micro-inch* inlay to a base "spring" metal.

When the connector is fabricated, the gold inlay appears at the point of contact, the only place it's needed. So even though it's non-porous, much thicker and far more reliable than gold plating, we can almost always offer our clad connectors for less than you'd pay for an ordinary connector.

Cross section of a 3-layer pressure-bonded composite metal.

And because we manufacture our connectors from start to finish at a single site, you not only get a *low priced* connector, but a *high quality* connector, too.

Our toughest customer.

The technique of bonding one metal to another is simple in concept but difficult to execute. This probably explains why there are so few manufacturers of clad metal. Of these manufacturers, TI is far and away the

Clad metal strip material

from an ordinary connector.

Clad metal strips are stamped into contacts by high speed presses.

largest in the world.

We are also the largest semiconductor manufacturer, which gives us an intimate knowledge of connectors and their electrical requirements. So as we developed our clad metal capability, we were able to apply it intelligently and immediately to our connectors.

And since we use our own connectors in many of the products we make, we get direct and rapid feedback from one of the most exacting manufacturers in the electronics industry.

In short, we're our own toughest customer. Which is why our connectors have to be the best.

Cross Section of H4 Series Edgeboard Connector

Custom features, standard prices.

TI's gold inlay is easy to spot. But there are other features, usually associated with customized connectors, that aren't so easily seen. These features come with all standard TI connectors and sockets, along with off-the-shelf availability. They include the following:

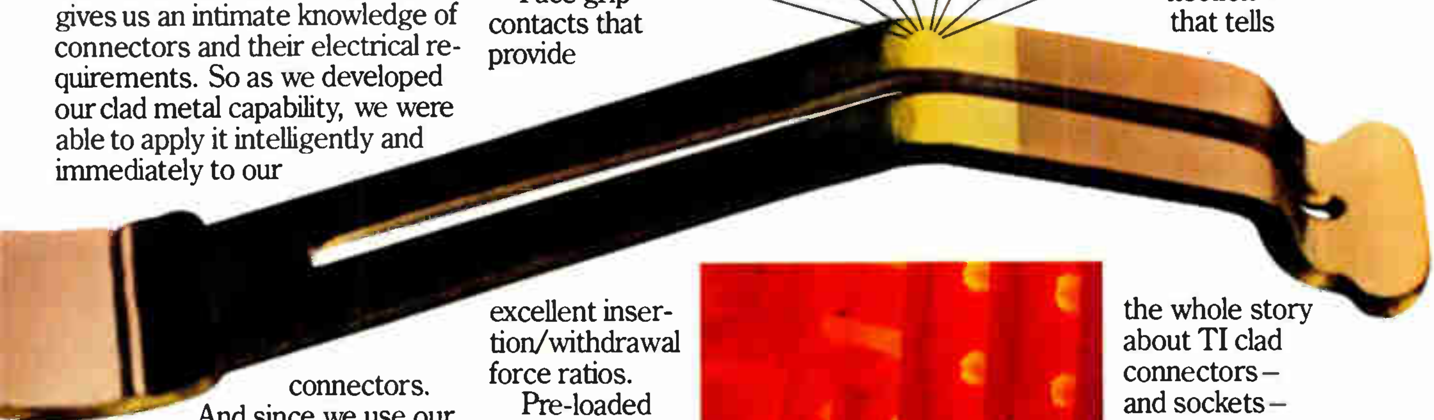
A special edge grip contact design that maximizes contact pressure and permits fast, positive insertion.

Face grip contacts that provide excellent insertion/withdrawal force ratios.

Pre-loaded contacts for faster, easier production insertion of IC's.

And individually replaceable contacts which can be changed without removing an entire socket from its mounting.

In most cases you'll be able to find the connector you need among our standard offerings. But if you have a complex or unusual application that calls for a custom-designed connector, tell us about it. We've helped hundreds of customers with such problems. And chances are, we can help you, too.



Ask for our catalog. It's beautiful and it's free.

Now that you know there's a big difference between clad connectors and ordinary connectors, you'll probably want to see what we have to offer. We have a fascinating catalog – "The Texas Connection" – that tells the whole story about TI clad connectors – and sockets – and presents the products in detail with accompanying descriptions, illustrations and specifications.

For a copy, just call or write Texas Instruments Incorporated, Connector Systems Department, Mail Station 2-16, Attleboro, Massachusetts 02703. Telephone (617) 222-2800, extension 268, 269 or 7327.

Fire assay helps Texas Instruments metallurgists determine precious metal purity, fundamental to achieving high reliability.

H4 Series Edgeboard Connector

TEXAS INSTRUMENTS
INCORPORATED

Boschert low-power switchers win OEMs' stamp of approval. Here's why.

Low cost. Only Boschert is delivering switching power supplies that are cost-competitive with linears in the 25 to 400 watt range. That's because Boschert is focusing exclusively on the design and production of low-power switchers. Our modular design techniques are lowering prices while maintaining quality and reliability.

Small, light and efficient. Boschert power supplies are perfect for microprocessor-based systems and other digital equipment because they're five times smaller than comparable linear supplies, and nine times lighter. Because little power is wasted as heat, they require no fans — only convection cooling. And Boschert switchers are well-suited for high pulse-load environments such as printers: when additional power is required, it is available instantaneously — at any output.

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Boschert experience and reliability. Boschert has assembled the finest switching power supply design and production team anywhere. Our facilities are prepared to meet expanded production schedules rapidly and reliably — with rigorous automatic burn-in, wave soldering and testing techniques. With over 50,000 of our power systems in operation today, we're the leading company for low-power, low-cost OEM switchers.

For information, contact a Boschert representative. Or write Boschert Incorporated, 384 Santa Trinita Ave., Sunnyvale, CA 94086. Phone (408) 732-2440. TWX 910-339-9241. The finest microprocessor-based systems are powered by Boschert. What about yours?

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Circle No. 132 for more Information

Planar stitch welding yields higher board density at lower cost

Low board profile is another benefit of interconnection technique that welds nickel wire to stainless steel pads

by Rene Lemaire and Ray Calvin, *Augat Interconnection Products Division, Augat Inc., Attleboro, Mass.*

☐ High wiring densities and low profiles are a combination often hard to beat when loading printed-circuit boards with components. When such a wiring method can lower costs over the established high-density low-profile techniques, then it is a strong contender for a myriad of electronics applications.

This advanced interconnection technique is planar stitch-wiring. It is based on welding nickel wire to stainless steel pads on special pc boards. Especially for lower production runs, it already is competitive with multilayer board techniques.

Welded wires

In planar stitch-wiring, point-to-point circuit interconnections are made by electrically welding lengths of Teflon-insulated solid nickel wire to stainless steel pads on the pc boards. On both sides of the board, the weld pads form a grid around the plated-through interconnections into which the components are inserted. Figure 1 shows an example of a finished board.

The interconnections may take the shortest distance between points, or they may be routed indirectly according to the designer's wiring map. Twisted-pair connections may be made; also, weld pads on the components side may serve as interconnects, so long as the wires are channeled around the components' locations.

Like the Multiwire technique, planar stitch-wiring can bond wire continuously [for a Technology Update on automatic wiring, see *Electronics*, May 25, 1978, p. 134]. The insulated wires used in both techniques can be layered, which provides the high density of interconnections. Multiwire achieves its low profile by bonding the wire to an adhesive substrate and terminating it to a plated-through hole. Planar stitch-wiring achieves its low profile with its stainless steel pads—in contrast to the similar stitch-wiring, which welds the wire to stainless steel pins, giving a higher profile and increased production costs due to the pin insertions required.

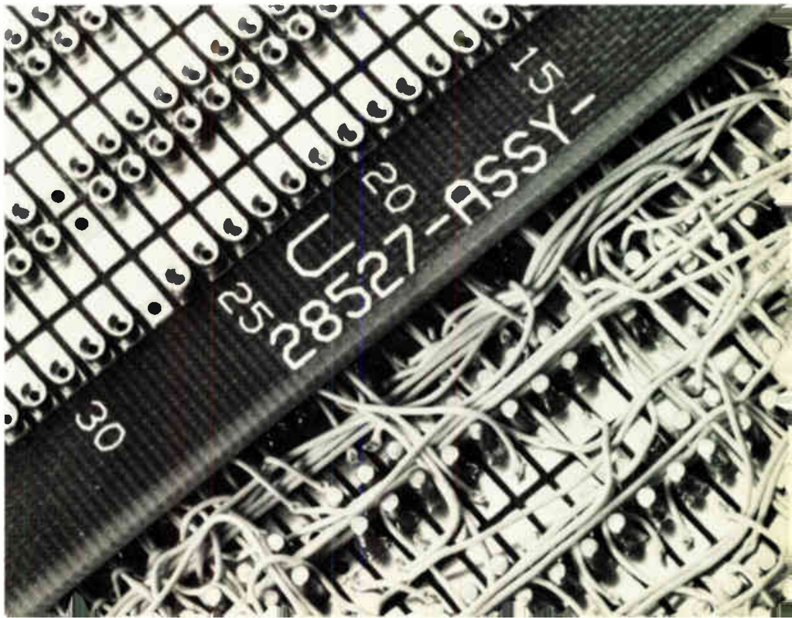
Another high-density low-profile alternative is the tried and true multilayer board, which may have as many as 30 internal conductive layers for the interconnection tasks. These complex boards generally are restricted to military, aerospace, and high-end computer applications, although a simplified method is beginning to make inroads into commercial uses [*Electronics*, May 25, 1978, p. 102].

The planar stitch-wired technique came from the APAC division of Varian Associates, aiming at military and aerospace applications. APAC became the Planar division of Augat in October 1977 and has been developing the method for use in commercial applications.

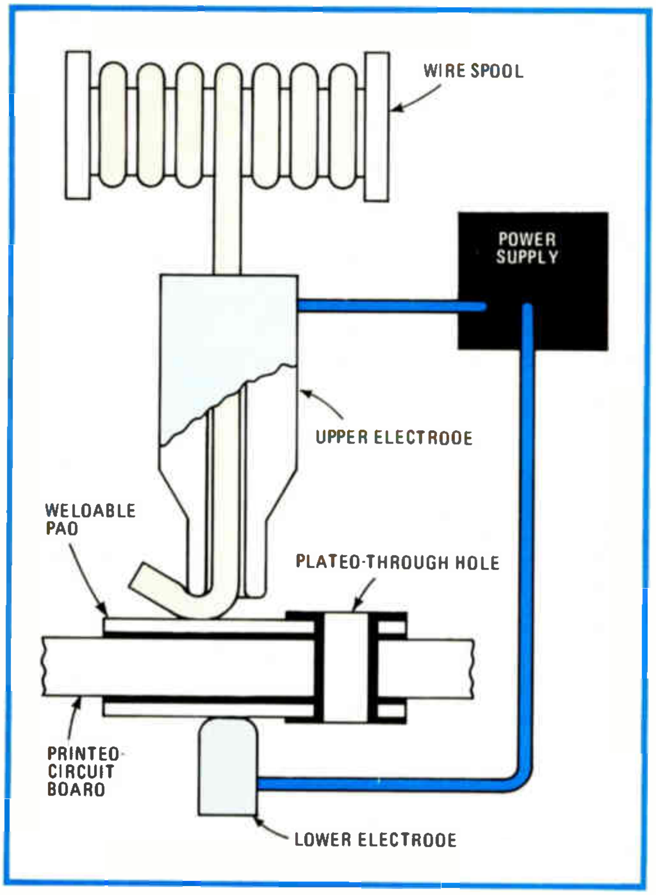
The solid, Teflon-coated nickel wire is 0.010 inch in diameter and has a minimum tensile strength of 45,000 pounds per square inch. Nickel wire and the stainless steel used for the weld pads have the bonding points and corrosion resistance necessary for electric welding, as well as the required differences in resistivity. The nickel provides a strong connection, resistant to shock and vibration, because it bonds without recrystallization or embrittlement.

The weld process

In the welding process (Fig. 2), the insulated wire automatically feeds through a hollow upper electrode and is pressed against the weld pad. The electrode is under pressure and mechanically displaces the Teflon insulation until a metal-to-metal contact is made to the weld pad—connected by the plated-through hole to a similar pad on the other side of the board, where the lower electrode is resting. The wire is slightly flattened



1. Stitch wiring. Combined are views of the wiring and component sides of a planar stitch-wired board. On the wiring side, insulated solid nickel wire is electrically welded to stainless steel pads. Wiring and component pads are connected by plated-through holes.



2. Electric bonding. In stitch-wiring, insulated wire is fed through an upper electrode and pressed against a board pad, displacing the insulation. A current pulse is then fed through the two electrodes, bonding the nickel wire to the stainless steel pad.

3. Semiautomatic. In Augat's System 78 planar stitch welder, the desired board pad is automatically positioned under the fixed welding head. The operator then actuates the head and cuts the wire, and the machine moves the board to its next position.

for a increased surface area, and a 2.5-millisecond high-current pulse from a capacitive-discharge power supply produces the bond.

Typically, the bond strength will be 85% of the ultimate tensile strength, varying only ±5%. Average heat generated during the bonding process is low, having no effect on the laminate or solder plating of the board. Underneath the steel pads is copper plating, which acts as a heat sink and minimizes the heating effect and changes in resistance caused by welding.

The welding may be either a manual or a semiautomatic process. In the manual approach, the operator follows a wire list in positioning the board for each weld. In the semiautomatic approach (Fig. 3), a punched-tape program positions the board on its X-Y axes, waiting until the operator has used the weld-activating foot pedal before moving on to the next interconnection. The difference in output is considerable: more than 100 wires an hour for the manual machine; more than 500 wires an hour for the semiautomatic machine.

A steel-clad board

Planar stitch wiring does require a special pc board, which begins with a core of FR-4 flame-retardant epoxy-glass. Laminated to both sides are sheets of 0.003-in. stainless steel, electroplated on their inner side with a thin layer of nickel and with a 0.0015-to-0.0020-in. layer made of copper.

After the stainless steel lamination, holes are drilled through the laminate to form the required pattern. Then the nickel film is plated to the stainless steel, and the epoxy-glass in the holes is chemically sensitized so that it, as well as the board surfaces, can be plated with the copper to a minimum thickness of 0.0015 in.

What follows are the basic steps to form a pc image: coating, exposure, and developing. Next are two etch cycles, one removing all metal layers where they are unnecessary, and the other selectively removing the copper from on top of what are then the weld pads.

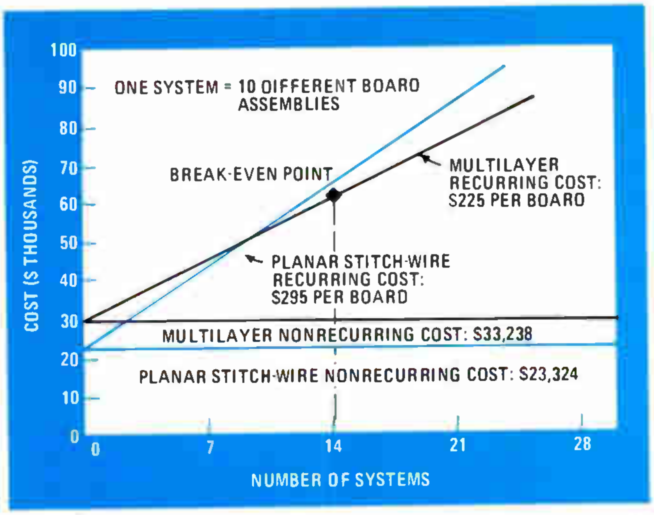
During the etching, the plated-through holes and the connecting terminals are protected by an applied mask. After removal of this mask, solder-coating the holes and the terminals completes the manufacture of the basic printed-circuit board.

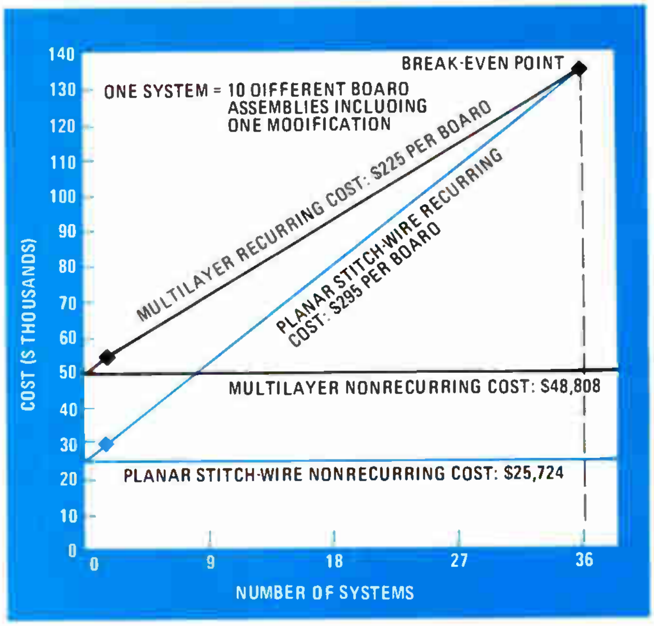
Myriad board designs

To connect integrated circuits (ICs) or discrete parts in dual in-line packages (DIPs) to a planar stitch-wired board, the patterns for the pads and plated-through holes may be custom designs or standard configurations. The off-the-shelf designs include patterns for 14-, 16-, and 24-lead DIPs, as well as universal layouts. The power and ground planes may be etched directly into the pc board to connect directly to the components, or they may be connected to separate weld pads at each IC position.

Pads formed outboard of the plated-through holes are standard. For even greater density, they may be inboard with the components mounted over them.

Computer-generated design means that the boards may be tailored to the most sophisticated custom circuitry that an engineer may require. Additional voltage and ground planes may be gained with inner layers tied





4. Getting even. The break-even analysis to the left shows that, for small quantities, stitch-wired boards are less costly than multilayer boards. One board modification to the same system can radically shift the break-even point upward (right).

through the plated-through holes to weld pads. Large aluminum heat sinks have been designed and bonded to component planes, as well.

A wide range of input/output interconnections are available, including standard nickel-gold edge connectors, two-piece right-angle connectors, and flat cable inter-connectors. Moreover, component mounting is available in a number of options: direct mounting, wave-soldered low-profile dual-in-line-package sockets, or machined socket pins.

A prime advantage of planar stitch-wired boards is the high wiring density—the ability to layer a large number of interconnections in a small amount of space. The density is comparable to that of a 15-layer pc board made by the multilayer method.

Other advantages

Even with this high density, the low profile of planar boards permits packaging in a standard cabinet with as little as 0.5 in. in between. By insuring compatibility with wire-wrapped boards, many systems using wire-wrapping can be expanded by selected board replacement using planar stitch-wiring. Since all wiring in the stitch-wired system is adjacent to the ground plane, the low profile also minimizes any delay of logic signals due to impedance variations, especially at emitter-coupled-logic speeds.

Another advantage of this wiring method is its flexibility, which makes it suitable for prototyping. Since it is easy to apply wires to the interconnection points or to change them, there is no need for breadboards when designing and debugging a new circuit or when expanding an existing one.

The planar boards also work well in full production runs. All connections are readily accessible, so if change is necessary, the wires being replaced are simply cut out and the new connections welded to the stainless steel pads. As many as four bonded wires may be accommodated on each pad. Even if a welding machine is not readily available, there is room for soldered connections at the terminal area of the plated-through holes.

Multilayer boards are the most widely used methods for obtaining high-density low-profile systems. However, they are cost-effective primarily in high-volume production of circuits that are past design change.

Planar stitch-wired boards have the flexibility and capability for being changed in production runs. Also start-up costs and turnaround times can be cut by a third to a half, compared to complex multilayer board designs.

Cutting costs

A cost study recently conducted compared the planar stitch-wiring and multilayer techniques. It found that the initial cost for a standard planar board is about half that for a multilayer board, while a custom stitch-wired board was about 65% of the cost of a multilayer unit. The study was fairly extensive, comparing nonrecurring and recurring costs for a typical small system with and without modifications.

The resulting computations, in the table and Fig. 4, are based upon doing most or all of the nonrecurring work in house, as well as the wiring. If Augat were to do the artwork, engineering, and programming, nonrecurring costs for stitch-wiring should be less than half the amount shown in the table.

For 10 board assemblies per system with no modifications, stitch-wiring has a $9,900 savings in nonrecurring costs. However, it has a higher recurring cost, resulting in a break-even point, for this example, of 14 systems, or 140 boards (left in Fig. 4).

With modifications

If just one modification per board is introduced into the sample system, the crossover point goes much higher. Nonrecurring costs for the first 10 boards are the same as before, but there is an additional $13,000 savings in nonrecurring costs for the stitch-wired board when making the modifications or changes. Also, production of the first system with the change results in another $1,840 savings with stitch-wiring raising the break-even

TYPICAL NONRECURRING COSTS

Multilayer boards	New board		Second board of same configuration		Modification	
	Hours	Material cost	Hours	Material cost	Hours	Material cost
Layout and artwork	90	$24.00	60	$24.00	45	$24.00
Board detailing and preparing numerical-coded drill tape	6	2.00	6	2.00	6	2.00
Assembly and parts list	24	1.00	8	1.00	2	1.00
Schematic	40	1.00	40	1.00	4	
Tooling	7					
Setup	6					
Drawing check	32		23		11	
Subtotal	205	$28.00	137	$28.00	68	$27.00
Labor cost at $22.50 an hour	$4,610		$3,080		$1,530	
TOTAL	$4,638		$3,108		$1,557	

Planar stitch-wire boards	Custom board		Standard board		Modification	
	Hours	Material cost	Hours	Material cost	Hours	Material cost
Layout and artwork	38	$ 8.00				
Board detailing and numerical-coded drill tape (computer-aided design)	6	2.00				
Cover detail	4	1.00				
Assembly master	24	1.00				
Assembly drawing and parts list	6	1.00	6	$ 1.00	2	
Schematic	40	1.00	40	1.00	4	
From-to wire list	24		24		1	
Keypunch and computer service	5	30.00	5	30.00	1	$15.00
Tooling	40	20.00				
Setup	5		5			
Drawing check	24		9		2	
Subtotal	216	$64.00	89	$32.00	10	$15.00
Labor cost at $22.50 an hour	$4,860		$2,010		$225	
TOTAL	$4,924		$2,042		$240	

point to 36 systems or 360 boards (right in Fig. 4).

Users of planar stitch-wiring are reporting excellent results in applications that have limited space or require rugged construction to resist the stresses of shock and vibration. For example, the Aerospace and Electronic Systems division of Westinghouse Electric Corp is using planar boards for satellite-launch vehicle control and integrated logistic support. Hughes Aircraft Co. is using them in an electronics package in an experimental military tank, which has a harsh shock and vibration environment. Cubic Corp. is flying a number of planar boards on an electronic package for a drone aircraft.

Commercial applications

Besides these aerospace and military uses, there are many commercial applications, including Itek Corp.'s use in imaging reproduction systems and very dense packaging for sophisticated aircraft instrumentation from the Avionics division of International Telephone and Telegraph Corp. Another aerospace firm used the planar method in a back panel.

To enhance the attractiveness of this wiring method, there is some down-to-earth research needed on equipment development. For instance, a study is being made of the feasibility of a relatively inexpensive field tool facilitating stitch-wiring changes at locations where a welding machine is unavailable. Such a tool will likely be comparable to the hand-held Gardner-Denver wiring gun now used with wire-wrapped boards.

Another development that may appear within the next few months is an economy line of single-sided stitch-wired boards, which promise to substantially cut production costs. It is based on a technique called parallel-gap welding, which will be designed for incorporation into both the microprocessor-controlled semiautomatic welding machine and the manual unit. □

Data-link control chip supports all three bit-oriented protocols

Ability to handle newer control procedures increases flexibility in designing data-communications systems

by Bill Meronek, *Western Digital Corp., Newport Beach, Calif.*

☐ As with any form of communication, rules, whether implicit or explicit, are necessary if messages are to be received and interpreted properly. In the case of data communications, the increasing capability and complexity of equipment and rapidly rising software costs have called forth the development of more efficient sets of rules, or protocols. The recent protocols for data-link control have therefore switched from a character- to a bit-oriented approach.

This approach uses position instead of control characters to define the various parts of a message, thereby boosting throughput and greatly simplifying implementation. In addition, the newer protocols provide advanced error-checking techniques, data transparency, and full-duplex capability.

Western Digital Corp.'s SD1933 (and the version soon to be produced as a second source by National Semiconductor Corp.) is the first data-link control chip to fully support all three bit-oriented protocols: IBM Corp.'s Synchronous Data Link Control (SDLC), the International Standards Organization's High-Level Data Link Control (HDLC), and the American National Standards Institute's Advanced Data Communications Control Procedure (ADCCP), which is almost identical to HDLC (see "Lots of protocols," p. 142, and "Data-link control chips: bringing order to data protocols," *Electronics*, June 8, p. 104).

The SD1933 generates modem-controlling signals for total link control. It interfaces a parallel digital system with a serial data-communications channel. To understand how this is done, the basic unit of information transfer for the three bit-oriented protocols—the frame—has to be examined.

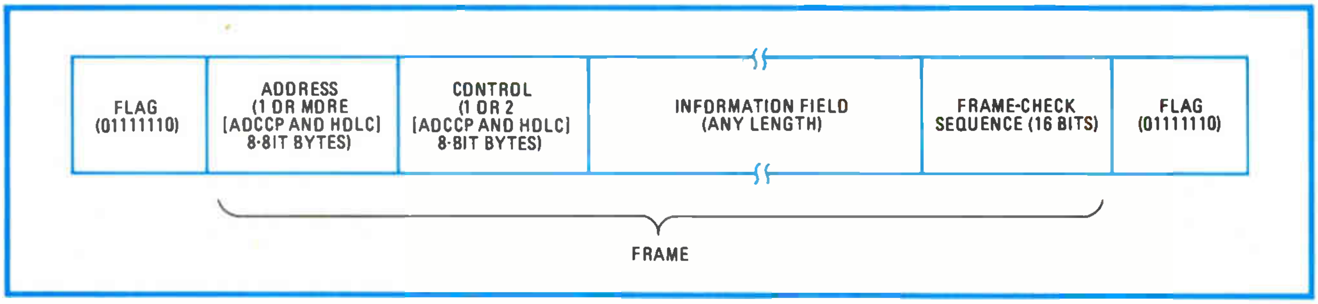
The frame consists of an address field, a control field, the information field, and a frame-check sequence (FCS) and is bounded at each end by a flag (Fig. 1). The flag sequence is 01111110.

Picturing the frame

There are two addressing modes: the basic address mode, which uses a single address byte (8 bits) and may be an individual, group, or global address; and the extended address mode (ADCCP and HDLC protocols only), in which the field is one or more bytes. In the latter, if the first (2^0) bit of an address byte is a 0, then the next byte is an extension of the address field. The field is terminated by putting a 1 in the first bit of the last byte. In this way, the address field may be extended to any number of bytes.

The control field, for encoding commands and responses required to control the data link, is one (all three protocols) or two (ADCCP and HDLC) bytes long. Three types exist. They are: supervisory, used to convey ready or busy conditions and possibly to report frame sequence errors; information transfer, used to send sequenced information frames; and nonsequenced (unnumbered), for data-link management, which includes initializing or activating secondary stations, controlling the response mode of secondary stations, and reporting procedural errors.

The frame-check sequence provides error detection. It uses the CCITT's 16-bit error-checking algorithm to perform a cyclic redundancy check on the address, control, and information fields. The transmitter first presets its 16-bit frame-check sequence to all 1s. Next, the binary value of the transmission to be sent is multi-



1. Information transfer. The frame is made up of groups, or fields, of bytes that contain all the required data control information, as well as the data itself. It is always bounded by flag sequences. The flags contain no information; they act as start and stop signals.

Data-link control: a glossary

Abort	a sequence of 7 to 14 consecutive binary 1s that terminates a frame and also the continuity of the data link
ADCCP	Advanced Data Communications Control Procedure: the American National Standards Institute's version (BSR X3.66) of SDLC
Address field	the field that defines the source or destination of a frame; it follows the opening flag of a frame
Asynch	any asynchronous data-communications protocol: transmission in which each character is individually synchronized by the use of start and stop bits; the length of the gap between characters is not necessarily fixed
Bisync	Binary Synchronous Communications: a character-oriented synchronous data-communications protocol developed by IBM; the predecessor of SDLC
Control field	a one- or two-byte (ADCCP and HDLC only) field that follows the address field and is used for sending commands and responses required to. control the data link
CRC	cyclic redundancy check: an error-checking technique that uses a sophisticated mathematical algorithm
Extended address	feature of ADCCP and HDLC that allows the address field to be more than one byte long
FCS field	frame-check sequence field: a 16-bit error-checking field to validate transmission accuracy; it uses CRC
Flag	a bit sequence (01111110) used to delimit frames
Full-duplex	simultaneous independent transmission of information in both directions
Global address	an address of all 1s, indicating that the frame is intended to be received by all stations
Go-ahead mode	a special SDLC mode in which the link is configured as a loop with one primary and n secondary stations
Go-ahead pattern	a bit pattern of one 0 followed by seven 1s, which is recognized by secondary stations as permission to transmit
HDLC	High-Level Data Link Control: the International Standards Organization's (ISO 3309) version of SDLC
Idle	a sequence of 15 or more consecutive 1s, indicating that the data link is to be idled
I-field	information field
NRZI	nonreturn-to-zero–inverted coding: a coding method in which the output remains in the same state to send a binary 1 and changes state to send a binary 0
SDLC	Synchronous Data Link Control: IBM's most recent synchronous data-communications protocol (GA27-3093)
STR	Synchronous Transmit and Receive: IBM's earliest synchronous data-communications protocol; predecessor of Bisync
Zero insertion and deletion	an encoding and decoding method used within a frame to guarantee that there are no more than five 1s in a row, thereby ensuring data transparency

plied and divided by appropriate polynominals. The integer quotient is then ignored and the complement of the remainder is transmitted. The receiver performs a similar computation on each incoming frame, including the frame-check sequence. If there are no errors, the receiver's FCS equals F0B8 (hexadecimal).

SYNCHRONOUS DATA-LINK CONTROL CHIP FUNCTIONS

Transmitter	Receiver
Zero insertion	Zero deletion
CRC generation	CRC check
Abort generation	Aborted frame detection
Residual byte transmission	Residual byte detection
Variable-byte-length transmission	Variable-byte-length reception
Go-ahead (loop) mode	Go-ahead (loop) mode
NRZI encoding	NRZI decoding
Flag generation	Idle detection
	Invalid frame detection
	Address comparison
	Address extension

The information field may be any length, including zero. Thus the minimum frame, not counting flags, is 32 bits long. In SDLC, the information field length must be a multiple of 8 bits; consequently, the SD1933 can generate and receive a residual byte of 1 to 7 bits.

Aborting the frame

Besides flags, two other bit sequences have meaning, and both are important features of the three bit-oriented protocols. A transmitting station may end a frame by sending an abort—a sequence of 7 to 14 1s. The receiving station will then ignore the frame, and it may not send another frame until it receives a command from the primary station.

The third bit sequence triggers the idle state provided for by the three protocols. The data link is idled when a station receives 15 or more 1s in a row. It remains idle until a 0 is detected.

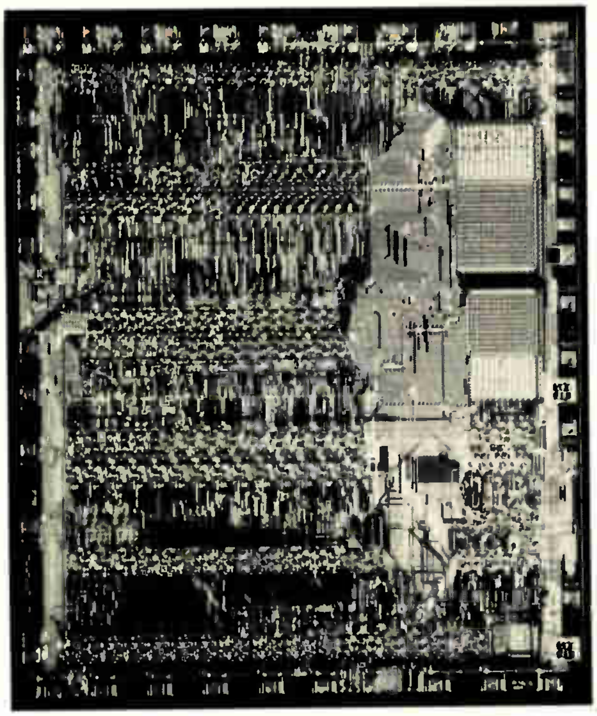
Another attribute of these protocols is zero insertion and deletion, which ensures data transparency. Within the two flags of a frame, a 0 is automatically inserted during transmission after five 1s and deleted on reception. Therefore no bit sequence in a frame can be misinterpreted as a flag, an idle, or an abort.

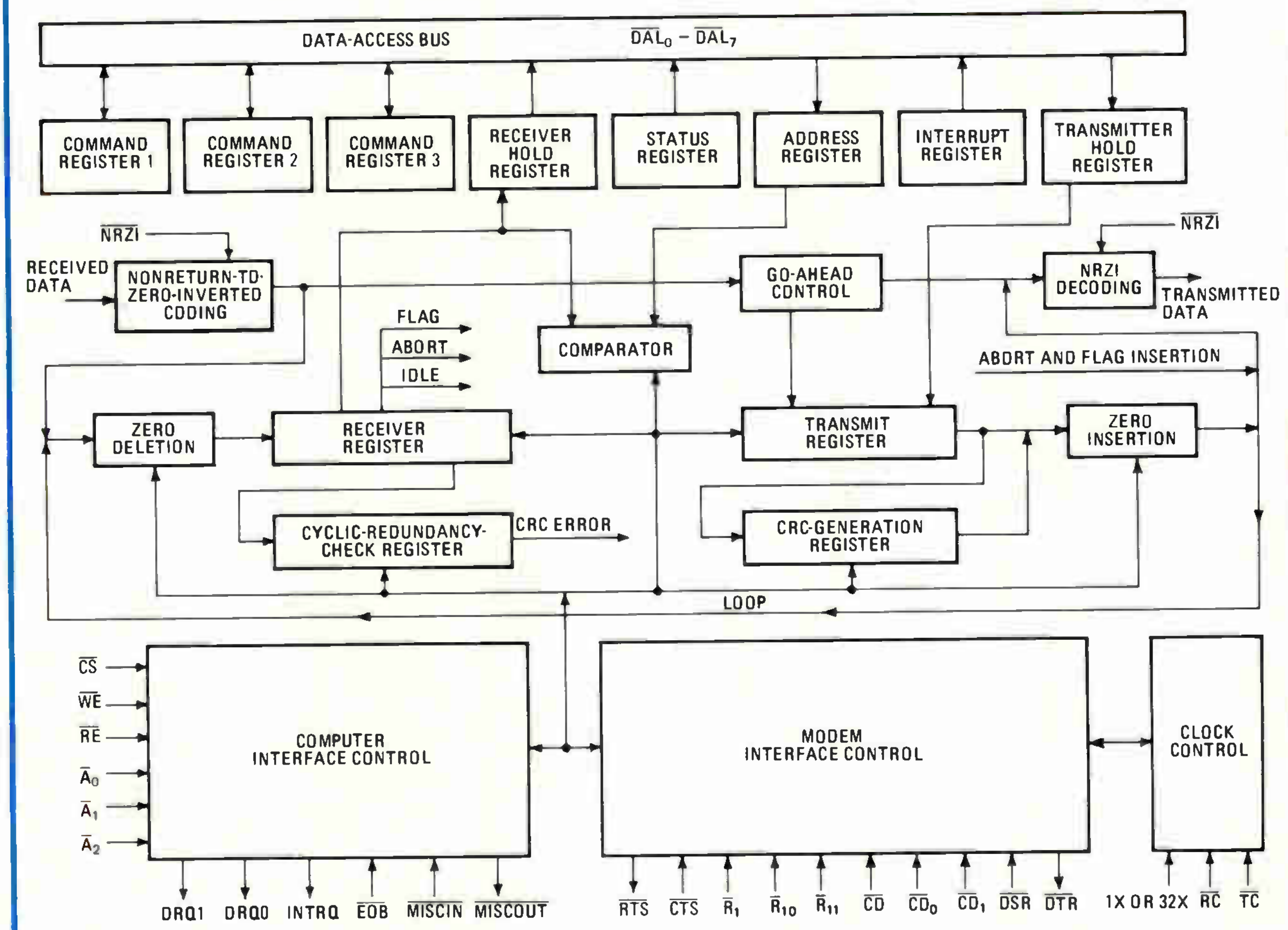
In addition, SDLC features a loop mode, called go-ahead. In this mode, each secondary station becomes a repeater. Transmissions from the primary are relayed from station to station and then back to the primary. Any secondary station finding its address in the address field of a frame captures that frame for action. All received frames are then relayed to the next station down the loop.

Whenever a secondary station receives the go-ahead pattern (a 0 followed by seven or more consecutive 1s), it may, at its option, suspend repeating and put its own transmission on the line. When it is finished, it sends a go-ahead pattern, deactivates its transmitter, and again becomes a repeater.

Performing the functions

The SD1933 performs all the functions required by the SDLC, ADCCP, and HDLC protocols (see the table). Built with n-channel metal-oxide-semiconductor technology, it uses a single 5-volt supply and is transistor-





2. Layout. The architecture of the SD1933 data-link control chip is fabricated on a chip 300 mils by 300 mils (top). Internal interconnections (bottom) use 40 external pins for interfacing a parallel digital system with a synchronous serial-data channel.

ters, and monitoring is accomplished by use of the status and interrupt registers (Fig. 3). The command registers dictate what the transmitter will send: the type of information (abort, flag, FCS, or data), the number of bits per byte, and the number of bits in the residual byte. Similarly, they tell the receiver the types of frames to look for, the number of bits per byte, whether to perform an address comparison, and whether to watch for an extended address.

Monitoring the signals

The status and interrupt registers perform monitoring. The status register indicates if an aborted or invalid frame has been received, whether an idle was received, and so on. The interrupt register indicates if end-of-message signals have been received and if frame transmission is complete. It also monitors the status of the interrupt signals.

Various modems are readily accommodated, as the SD1933 has a full complement of modem interface signals. These signals include data set ready (DSR), ring indicator (RI), carrier detect (CD), clear to send (CTS), request to send (RTS), and data terminal ready (DTR). An interrupt is generated if DSR, RI, or CD changes state (the latter two if so programmed). RI and CD may be programmed to interrupt on the rising edge, on the falling edge, or on both edges. The interrupt source is determined by reading the interrupt and status registers. The DTR output is set by a bit in the command register and RTS is set when the transmitter is activated.

Still more choices

When the nonreturn-to-zero–inverted code is chosen (a data transition when a 0 is sent and no transition when a 1 is sent), the transmitter encodes the transmitted data with the NRZI code before shifting it out. Similarly, the receiver expects NRZI-encoded data and will decode it before assembling data bytes.

In the 1X mode, the SD1933 requires the clock and data signals to be phase-synchronized in order to ensure link integrity. In the 32X mode, it uses a digital phase-locked loop to provide the synchronization, thus allowing connection to asynchronous modems as well. However, the loop requires data transitions to do this. Zero insertion and deletion guarantees transitions for long strings of 1s within a frame. To provide transitions for long strings of 0s, the nonreturn-to-zero–inverted option should be used.

The end-of-data-block (EOB) option allows easy transfer of blocks of memory by direct memory access. Activated at the end of the data block, it causes automatic transmission of the frame-check sequence and a flag.

Putting the chip to work

In a typical data-communications application (Fig. 4) such as might be found in a stock brokerage firm, the host and its peripherals are located at the main office. Terminals are also located in remote offices, with connection to the host via data-communications controllers. The terminals provide up-to-the-minute stock prices, entry of customers' buy and sell orders, and companies' financial statements, as well as the firm's accounting and billing information.

Such a system is general enough to be configured for a wide variety of applications. For example, the host processor and remote terminals could be located respectively in airline reservation offices and ticket counters, travel centers and travel agencies, central bank offices and branch banks, or department stores and individual cash registers.

The host processor performs high-level data-processing tasks such as accounting, bookkeeping, and input and output to the cathode-ray-tube terminal, line printer, card reader, or disk. Usually, a large portion of the data processing is dedicated to sending or accepting data to or from the data concentrator. Sending large blocks of data to the remote terminals via the data concentrator relieves the host of time-consuming I/O chores, freeing it for other processing tasks.

The data concentrator processes and formats data to allow for more orderly and efficient information transfer between the host and the data-communications controller. It is modified for each application to enable it to translate the data received from the controller into a format acceptable to the host, and vice versa. Other functions include setting priorities for the controller's channels, processing interrupts, and holding data until the host is ready to accept it.

The data-communications controllers interface remote terminals via modems (if necessary) with the data concentrator. Each controller uses a microprocessor to manage eight serial data-communications ports. Each port contains a printed-circuit board with a 40-pin socket filled with the chip appropriate for SDLC or Bisync communications. A DIP switch on each pc board programs it to expect the right one. □

Lots of protocols

Since the advent of synchronous data communications, a wide variety of protocols has been developed by various military agencies, universities, and companies. The most widely used have been those generated by IBM Corp.

The earliest were the Synchronous Transmit and Receive (STR) and Binary Synchronous Communications (Bisync) protocols. However, the increased sophistication of processing equipment called for more efficient procedures.

Synchronous Data Link Control (SDLC), announced in 1973, was developed to permit accurate full-duplex transmissions with a high throughput. Some of the advantages of SDLC over STR and Bisync are independence of code structure, full information transparency without the use of control characters, a single standard-frame format, and full-duplex operation.

After the introduction of SDLC, several national and international organizations issued their own versions. The International Standards Organization's High-Level Data Link Control (HDLC) is described in the ISO 3309 specification. The American National Standards Institute's version, called Advanced Data Communications Control Procedure (ADCCP), is described in ANSI BSR X3.66. The ISO and the ANSI specs are very similar and both are supersets of SDLC (except for its loop mode).

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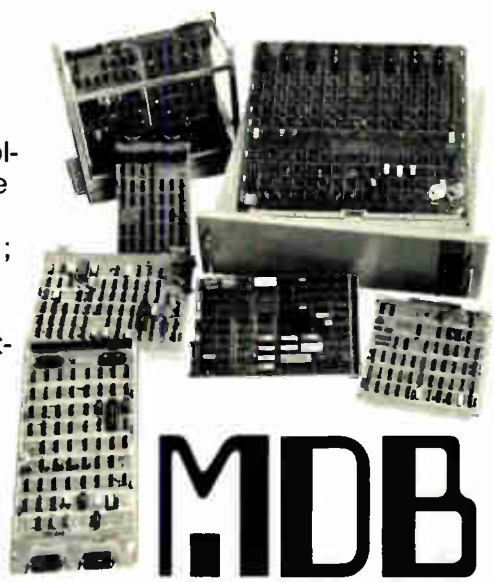

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Unspecified 8085 op codes enhance programming

by Wolfgang Dehnhardt and Villy M. Sorensen
GSI, Darmstadt, and Sorensen Software, Seeheim, West Germany

Ten operating codes and two flag bits previously unknown to most users of the 8085 microprocessor will enable programmers to write more efficient routines. The new members of the instruction set, which were stumbled upon during the testing of an assembler-disassembler module, include seven op codes that involve the processing of register pairs, two that involve jump operations with one new flag bit, and one that performs a conditional restart on the overflow indication of the other flag bit.

The seven register pair instructions (all with 16-bit operands) consist of a double subtraction, a rotate, a shift, indirect loading and storing of a word, and two offset operations. Either BC, DE, HL, or SP are the designated register pairs used in these op codes.

The mnemonic names of the instructions have been selected to be compatible with the 8085's existing mnemonics. In the double subtraction (DSUB), register pair BC is subtracted from HL. This instruction thus performs the opposite task of DAD B, a well-known instruction. The instruction RDEL rotates register pair DE left 1 bit through the carry. ARHL is an arithmetic shift to the right of HL. It serves to divide HL by 2, except in cases where HL is −1.

All 16 bits of register pair HL can be stored indirectly at the address contained in the DE pair by specifying instruction SHLX. To load HL, LHLX must be employed.

As an example of how this instruction can be used to cut instruction steps, consider the common sequence used for a routine table jump shown in part (a) of the figure. By assigning the register DE for HL and using the LHLX instruction, this sequence can be replaced by the much simpler arrangement shown at the bottom of part (a).

As for adding the contents of register pairs with an additional byte (offset), DE can be loaded with HL plus the byte by selecting the instruction LDHI, which simplifies array addressing. Usually, the architecture of 8080-type systems dictate the addressing of arrays in what are called pages of 256 bytes. This restriction means that the starting address of an array must be placed near the beginning of a page. A typical call is as shown in part (b) of the figure.

The page limitation is bypassed using the LDHI instruction code and constant indexes. The starting address of the array can now be placed anywhere, and addressing occurs as shown at the bottom of part b.

Any additional byte can be combined with register-pair SP in DE if instruction LDSI is specified. This instruction is designed for operating system routes that transfer arguments on the stack. An example sequence, shown in (c), stores HL into the 16-bit word located as the second item below the top of the stack.

The jump and restart instructions work in conjunction with the two discovered flag bits, X5 and V. Op codes JX5 and JNX5 jump depending on the state of the X5 flag. Op code RSTV makes a restart call to hexadecimal address 40 if the V flag is set; otherwise it functions as a no-operation instruction.

Flag bit V indicates a 2's complement overflow condition for 8- and 16-bit arithmetical operations. Flag bit X5 has been named for its position in the condition code byte and not for its function. It does not resemble any normal flag bit. The only use for this bit found thus far are as an unsigned overflow indicator resulting from a data change of FFFF to 0000 on executing the instruction of INX and as an unsigned underflow indicator from a data change of 0000 to FFFF on executing DCX.

The new 8085 instructions are outlined in the table. ☐

(a)

Source statement		Comments
MOV	E, M	;ROUTINE ADR LOW BYTE
INX	H	;HL = TABLE ADR
MOV	D, M	;ROUTINE ADR HIGH BYTE
XCHG		;DE = ROUTINE ADR
PCHL		;GO TO ROUTINE ADR

↓

Source statement		Comments
LHLX		;DE = TABLE ADR
PCHL		;HL = ROUTINE ADR

(b)

Source statement		Comments
LXI	H, ARRAY	;ARRAY BASE ADR
MVI	L, INDEX	;8-BIT INDEX, HL = ARRAY ADR

↓

Source statement		Comments
LXI	H, ARRAY	;ARRAY BASE ADR
LDHI	INDEX	;8-BIT INDEX, DE = ARRAY ADR

(c)

Source statement		Comments
LDSI	2	;DE = SP + 2
SHLX		;REPLACE 2. ITEM ON STACK

Options. Newly discovered operating codes for 8085 shown in table enables the writing of more efficient programs. Program for table jump (a, top) may be reduced significantly when new instruction (a, bottom) are implemented. Array routines (b, top) can be rewritten (b, bottom) so that arrays can be addressed across page boundaries. Data words can be entered at any point in a stack register (c).

NEW CONDITION CODES: V = bit 1 — 2's complement overflow

X5 = bit 5 — Underflow (DCX) or overflow (INX)

X5 = 01·02 + 01·R + 02·R, where 01 = sign of operand 1, 02 = sign of operand 2, R = sign of result. For subtraction and comparisons, replace 02 with $\overline{02}$.

Condition code format							
S	Z	X5	AC	0	P	V	C

DSUB (double subtraction)

(H) (L) = (H) (L) – (B) (C)

The contents of register pair B and C are subtracted from the contents of register pair H and L. The result is placed in register pair H and L. All condition flags are affected.

0 0 0 0 1 0 0 0	(08)

cycles: 3
states: 10
addressing: register
flags: Z, S, P, CY, AC, X5, V

ARHL (arithmetic shift of H and L to the right)

(H7=H7); (Hn–1) = (Hn)
(L7=Ho); (Ln–1) = (Ln); (CY) = (Lo)

The contents of register pair H and L are shifted right one bit. The uppermost bit is duplicated and the lowest bit is shifted into the carry bit. The result is placed in register pair H and L. Note: only the CY flag is affected.

0 0 0 1 0 0 0 0	(10)

cycles: 2
states: 7
addressing: register
flags: CY

RDEL (rotate D and E left through carry)

(Dn+1) = (Dn); (Do) = (E7)
(CY) = (D7); (En+1) = (En); (Eo) = (CY)

The contents of register pair D and E are rotated left one position through the carry flag. The low-order bit is set equal to the CY flag and the CY flag is set to the value shifted out of the high-order bit. Only the CY and the V flags are affected.

0 0 0 1 1 0 0 0	(18)

cycles: 3
states: 10
addressing: register
flags: CY, V

LDHI (load D and E with H and L plus immediate byte)

(D) (E) = (H) (L) + (byte 2)

The contents of register pair H and L are added to the immediate byte. The result is placed in register pair D and E. Note: no condition flags are affected.

0 0 1 0 1 0 0 0	(28)
data	

cycles: 3
states: 10
addressing: immediate register
flags: none

LDSI (load D and E with SP plus immediate byte)

(D) (E) = (SPH)(SPL) + (byte 2)

The contents of register pair SP are added to the immediate byte. The result is placed in register pair D and E. Note: no condition flags are affected.

0 0 1 1 1 0 0 0	(38)
data	

cycles: 3
states: 10
addressing: immediate register
flags: none

RSTV (restart on overflow)

If (V):
((SP)–1) = (PCH)
((SP)–2) = (PCL)
(SP) = (SP)–2
(PC) = 40 hex

If the overflow flag V is set, the actions specified above are performed; otherwise control continues sequentially.

1 1 0 0 1 0 1 1	(C8)

cycles: 1 or 3
states: 6 or 12
addressing: register indirect
flags: none

SHLX (store H and L indirect through D and E)

((D)(E)) = (L)
((D)(E)+1) = (H)

The contents of register L are moved to the memory location whose address is in register pair D and E. The contents of register H are moved to the succeeding memory location.

1 1 0 1 1 0 0 1	(D9)

cycles: 3
states: 10
addressing: register indirect
flags: none

JNX5 (jump on not X5)

If (not X5):
(PC) = (byte 3) (byte 2)

If the X5 flag is reset, control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction; otherwise control continues sequentially.

1 1 0 1 1 1 0 1	(DD)
low-order address	
high-order address	

cycles: 2 or 3
states: 7 or 10
addressing: immediate
flags: none

LHLX (load H and L indirect through D and E)

(L) = ((D)(E))
(H) = ((D)(E)+1)

The content of the memory location whose address is in D and E, are moved to register L. The contents of the succeeding memory location are moved to register H.

1 1 1 0 1 1 0 1	(ED)

cycles: 3
states: 10
addressing: register indirect
flags: none

JX5 (jump on X5)

If (X5):
(PC) = (byte 3) (byte 2)

If the X5 flag is reset, control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction; otherwise control continues sequentially.

1 1 1 1 1 1 0 1	(FD)
low-order address	
high-order address	

cycles: 2 or 3
states: 7 or 10
addressing: immediate
flags: none

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Selectors squeeze data into random-access memories

by Thinh V. Nhuyen
Technology Service Corp., Los Angeles, Calif.

In interfacing a random-access memory (RAM) with a computer or a central processing unit, it is hard to utilize the maximum space available in the RAM because its word and bit organization is incompatible with the structure of the data bus. For example, a RAM might be configured as a 16-word-by-8-bit device, whereas the data bus might be configured to accept data organized in 8 words by 16 bits. Worse yet, no standard-sized RAM may exist for a desired data-block organization. Although there is no hard-and-fast scheme for interfacing, the circuit shown in the figure, which in this case configures data in a 128-word-by-1-bit block although accepting the same data from an 8-word-by-16-bit bus, will yield insight on how to solve similar problems.

Since no 128-word-by-1-bit RAMs exist, two 7489 16-word-by-4-bit devices are used. One stores 64 even-addressed 1-bit words; the other stores the remaining odd-addressed words. Two two-to-one-line data selectors (74157s), driven by a 7-bit system counter, assign data on the bus to their corresponding RAMs.

The bus line is wired into the 74157s, so that their outputs map their corresponding RAMs as shown. During the write operation, bits 3 to 6 of the 7-bit counter are used for addressing. Bit 3 enables data to enter the correct RAM in blocks of 4 bits. Thus all available locations in both RAMs will be filled with data.

On readout, two four-to-one-line selectors (74153s) and a two-to-one selector (74157) extract the desired data in sequence from both RAMs. During the read operation, bits 3 to 6 are used for addressing the RAMs, as before. Bits 0 to 2 address the appropriate data selectors: bit 0 selects either odd- or even-location data (in order) from the 74157, and bits 1 and 2 direct the data from the 74153s to the input of the 74157. Thus 128 1-bit words appear at the output.

Because data from the bus is loaded into the RAMs 8 bits at a time, the clock rate of the RAMs' address counter should be twice that of the bus line's data rate. To say it another way, the 7-bit counter should run 16 times faster than the computer's clock.

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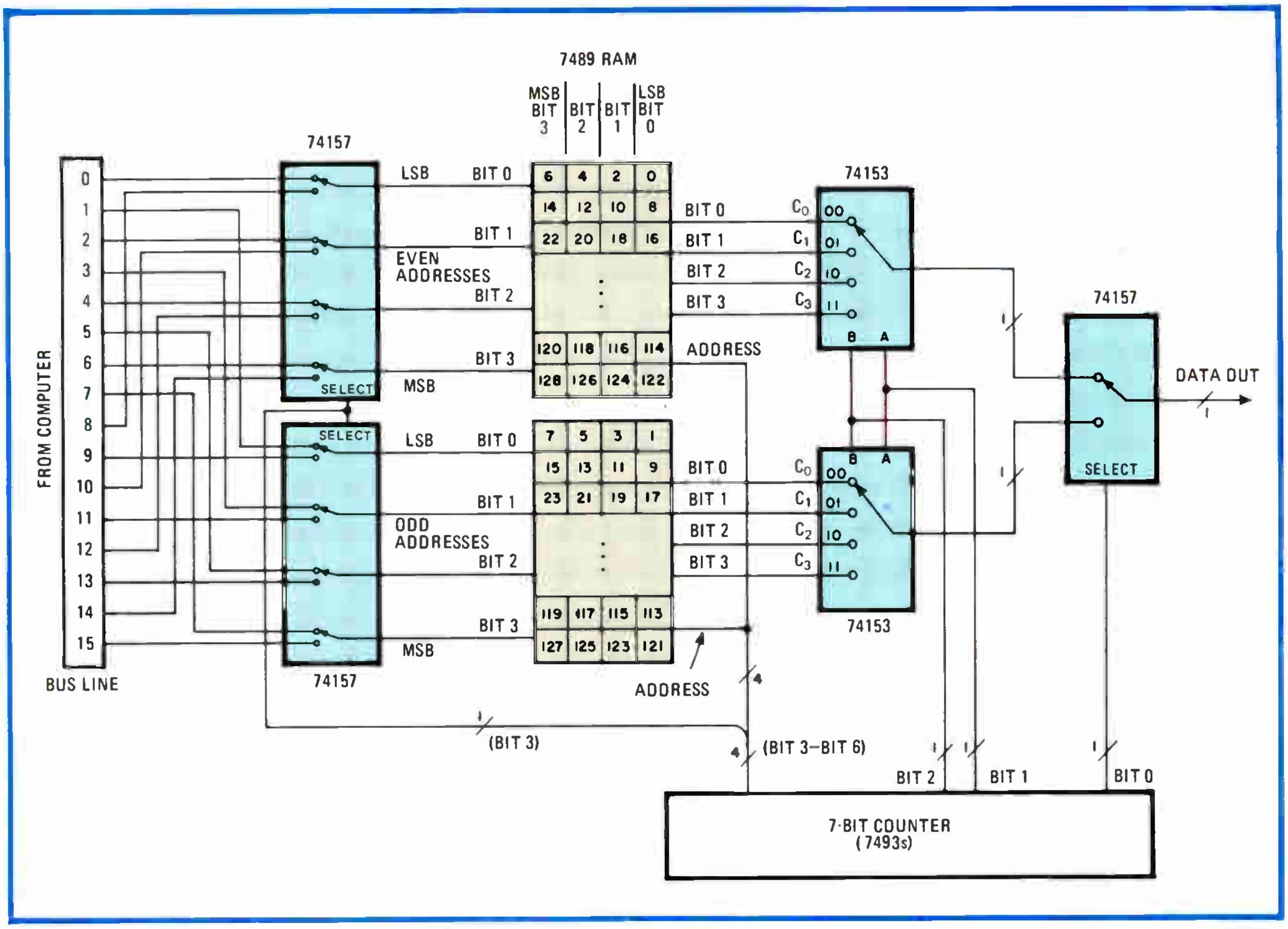

Selective addressing. Maximum number of RAM locations can be filled with data, despite incompatibility of RAM's word and bit organization with data-bus structure. General method for organizing large, nonstandard-sized m-word-by-n-bit data blocks from p-word-by-q-bit data bus uses selectors for mapping data into two RAMs, one of which contains the even-addressed data, the other the odd-addressed data.

Latch's metastability may generate synchronizer glitches

Simple circuits that synchronize a one-shot to a system clock independent of the input signal's arrival at the one-shot may generate glitches if flip-flops are used to do the job, says Roy C. Ogus of Xerox Corp., Palo Alto, Calif. He therefore disputes the effectiveness of a circuit (described in *Electronics*, July 21, 1977, p. 107) in which a flip-flop, driven at its D port by a differentiated high-level trigger signal, is latched by the system clock (C input). Because the amplitude of the signal at the D input is changing, setup times may not be observed, depending on when the system clock signal arrives. The author's suggestion that the signal fall below the threshold level of the D input halfway between clock pulses cannot be ensured with the tolerances of the RC components used in the differentiator, says Ogus. As a result, the flip-flop's outputs may show metastable behavior, failing to assume true logic states or even oscillating.

Ogus' solution for lowering the probability of glitches is to connect the D input of a second flip-flop to the output of the first and to latch both with the same clock. The output of the second flip-flop becomes the output of the circuit. The probability that the second device will assume any metastable state is drastically reduced, since **the transients from the first latch are likely to disappear by the time the next clock occurs.**

Where to get thermal properties measured

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Conducting the sessions will be interface products marketing manager Don Tarver, design manager Bill Fowler, and design section leader Charles Carinalli. The seminar, geared to design engineers and technicians, has yet to be presented in Boston (Feb. 5); Stamford, Conn. (Feb. 6); Westbury, N. Y. (Feb. 7); Pinebrook, N. J. (Feb. 8); Philadelphia (Feb. 9); Dallas (Feb. 26); Fort Lauderdale (Feb. 27) and Orlando (Feb. 28), Fla.; Phoenix (March 1); and Tucson (March 2). The seminar is free of charge. Those interested should contact their local National Semiconductor sales office for further information.

Vincent Biancomano

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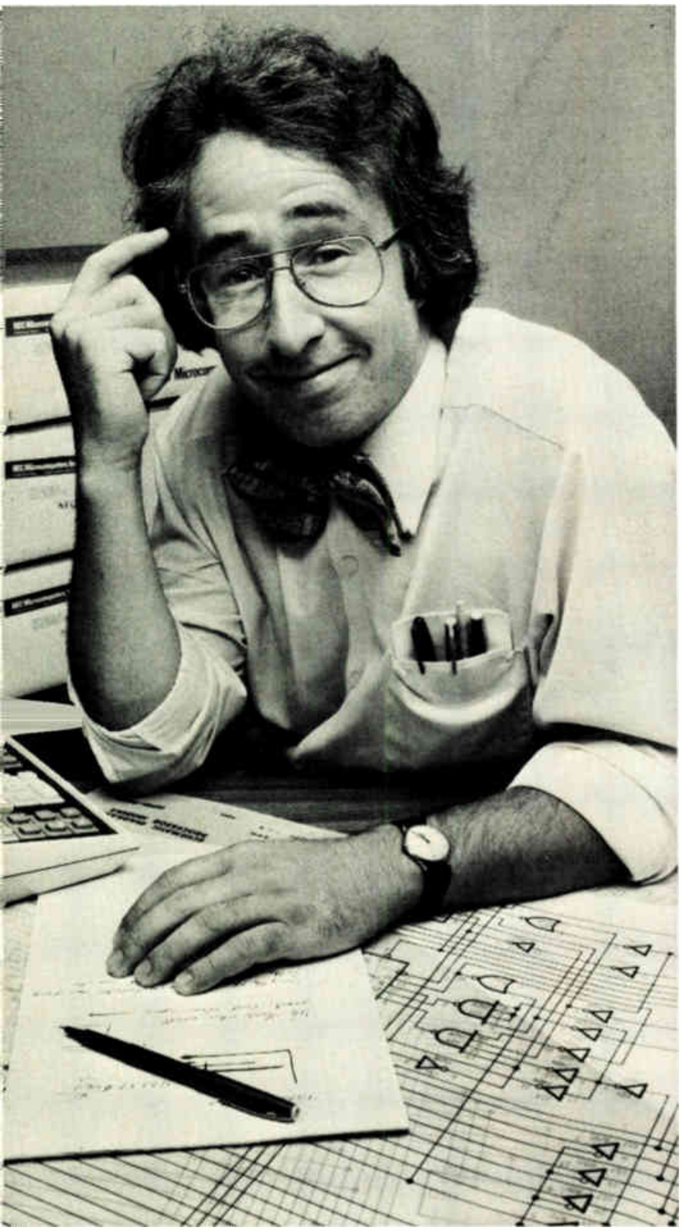

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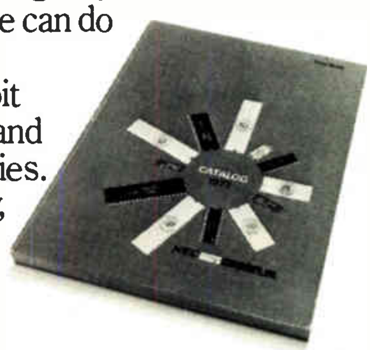

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E1-3

The monolithic filter has arrived

Family of switched-capacitor filters includes three bandpass and two low-pass devices, each of which fits into a standard 16-pin DIP

by Bill Arnold, San Francisco regional bureau manager

To perform the filtering required by telecommunications, acoustic analysis, and other medium- and low-frequency applications, engineers usually turn to active filters whose less than ideal RC networks often yield less than desirable results. Reticon Corp. claims a better solution: a line of monolithic bandpass and low-pass filters built using a switched-capacitor technique.

Not only does the filter family offer integrated circuits in 16-lead dual in-line packages, but it can cram up to 18 poles of filtering into that space. The family consists of three bandpass and two low-pass filters. The bandpass units have bandwidths of one-third, one-half, and one octave, with center frequencies variable from 5 Hz to 10 kHz. Because of the switched-capacitor design, the center frequency is determined by the frequency of an external clock: no precision external components are needed.

The low-pass devices are an equal-ripple six-pole Chebyshev filter and a five-pole Bessel (linear-phase) unit. They have corner frequencies that can be varied by an external clock from less than 1 Hz to 30 kHz. Broadband signal-to-noise ratio is typically 70 dB, and insertion loss is typically 6 dB.

Key specifications for the bandpass filters include a maximum in-band harmonic distortion of 1% and center-frequency and gain temperature coefficients of less than 0.001%/°C.

Space saver. Conventional active filters need resistors and capacitors, which take up a lot of room. To eliminate them, Reticon married n-channel metal-oxide-semiconductor polysilicon-gate technology and the switched-capacitor architecture. The critical frequencies of conventional active filters are determined by the absolute values of resistors and capacitors. With the switched-capacitor technique, what counts is the ratio of capacitances.

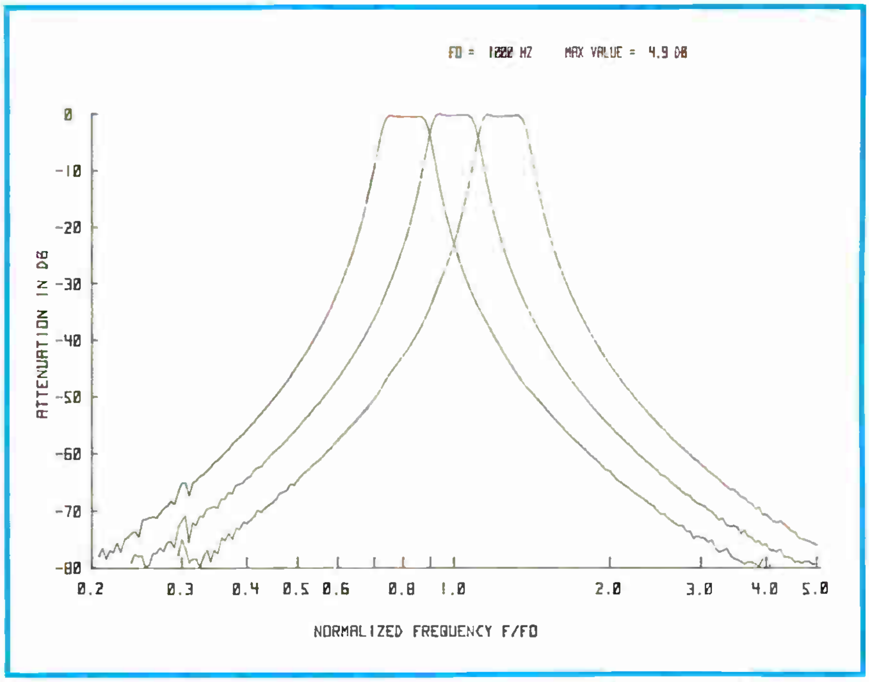
These capacitances can be realized in n-MOS technology by stacking two layers of polysilicon around a layer of silicon dioxide. Capacitors made in this way tend to be stable over time and temperature and can consistently be made with tolerances of 0.1%. The result: subaudio filters the size of standard ICs.

The R5604 one-third-octave, R5605 half-octave, and R5606 full-octave bandpass filters have a signal-to-noise ratio, in the pass band, of more than 80 dB. Insertion loss is 0 dB, and maximum peak-to-peak signal level is 10 V. The R5604 sells for $60 ($24 in hundreds), the R5605 goes for $50 ($20 in hundreds), and the R5606 is priced at $40 ($16 in hundreds).

The R5607 Chebyshev and R5608 Bessel filters sell for $13 each in thousands. They can handle peak-to-peak signals up to 4 V.

Besides these standard products, Reticon can also make a variety of semi-custom filters using the same combination of techniques, according to analog product marketing manager David D. Arnold.

Reticon Corp., 345 Potrero Ave., Sunnyvale, Calif. 94086 [338]



Curve. Computer-plotted graph shows frequency response of one-third-octave R5604 filter for a center frequency of 1 kHz and for two slightly offset center frequencies.

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IEEE-488 reaches beyond 20 meters

Bus extender allows operation at distances up to 1 kilometer using twisted pairs and over unlimited distances using modems and phone lines

by Robert Brownstein, San Francisco regional bureau

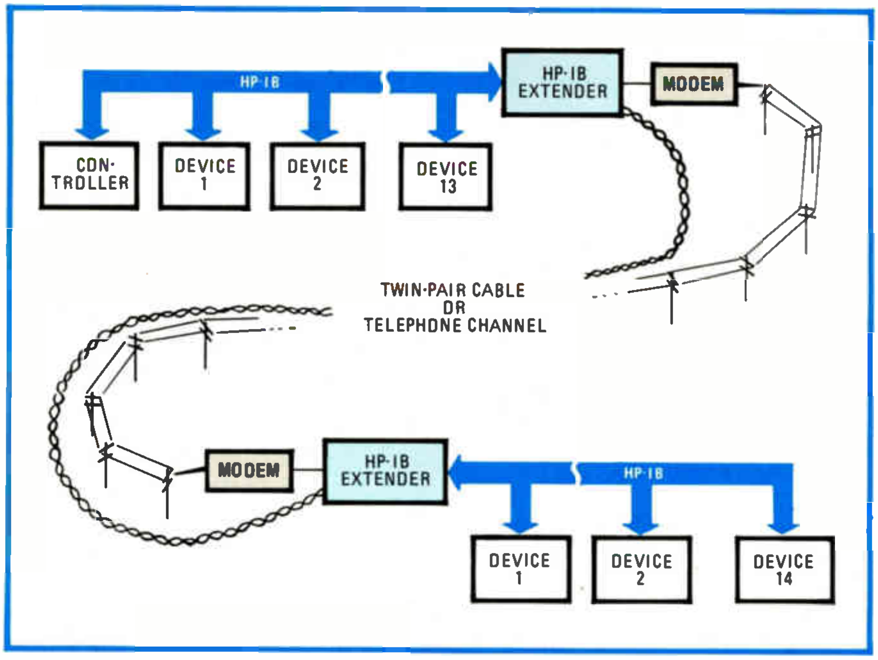
The 20-meter limit on cable length specified by IEEE-488—the standard for general-purpose interface buses—has prevented some potential users from adopting the scheme. Many of these possible users can now be accommodated by a transparent bus extender from Hewlett-Packard, which is designated the model 37201A.

"Without too much compromise, a user can link instruments up to 1,000 meters apart with the HP-IB [HP's name for the IEEE-488 bus] and dedicated twisted-pair cabling," says Donald C. Loughry, HP corporate interface engineer. The only penalty, he explains, is forfeiture of the ability to pass control from one site to another or to parallel-poll across instrument clusters separated from the controller by the extender.

Otherwise, the 37201A is virtually transparent to the instruments it connects and requires no software changes in the controller program nor any special protocols, he says.

For applications over long distances, the 37201A may be linked to a standard telephone modem to connect any points in the world that can be connected by telephone. If the points are connected by a four-wire leased line, a single controller can communicate one at a time with up to 32 instrument cluster sites in a multidrop arrangement.

The bus extender hooks on to the bus like any other instrument or controller. It accepts parallel bus characters and converts them into a serial bit stream, buffering and grouping them for transmission at rates up to 20 kilobits per second synchronously or 1,200 bits/s asynchronously. All communication between extenders is full-duplex and all data is checked for transmission errors; if errors are found, the data is retransmitted until it is error-free.



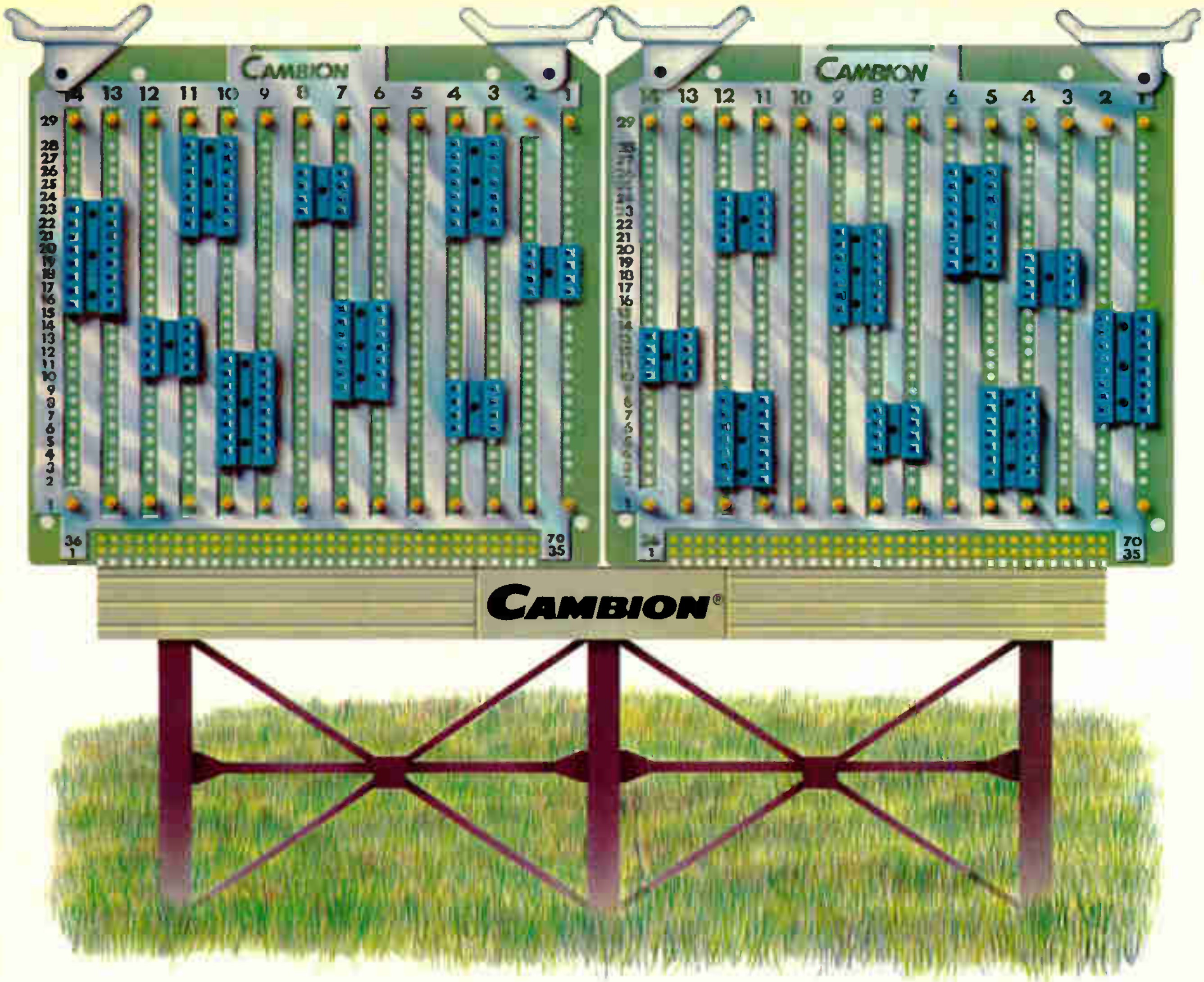
"Besides errors, another thing you don't want is for a telephone-linked system to lose control of the phone on the remote end," he points out. Otherwise, the remote phone might be left off the hook should something go wrong with the communications link after the call was established.

To prevent this sort of problem, the bus extender automatically hangs up the phone within a minute of detecting a communications malfunction. "The alternative is to send someone to the remote site to hang up the phone. If the instruments are measuring weather conditions in the Arctic, that can be a problem," Loughry quips.

In a twisted-pair setup, if the cable is inadvertently cut or disconnected, it can be reattached and the 37201A will quickly recover synchronization automatically. A remote site can be effectively disconnected by an idle command from a controller, Loughry says, allowing the remote system to be serviced without tampering with the interface hardware. Automatic dialing under program control is available through a standard RS-366/V.25 connector.

Deliveries of the 37201A will begin this month. The price is $1,600. Four-wire cable (two twisted pairs) can be ordered as an option for dedicated interconnections. Modems that are compatible with RS-232-C/V.24 are required for telephone links.

Inquiries Manager, Hewlett-Packard Co., 1507 Page Mill Rd., Palo Alto, Calif. 94304 [339]



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In less than three minutes, an ambulance with two paramedics arrived.

But as they began to work, arrhythmia—erratic, wildly uncontrolled heartbeat—set in.

Then his heart stopped altogether.

A MIRACLE OF ELECTRONICS.

Fortunately, the ambulance was equipped with a Motorola APCOR Coronary Observation unit.

It put the paramedics in immediate touch with an emergency physician at the hospital miles away.

Not just by voice communication; that doesn't give a doctor all the information he needs.

But at the very same instant, by Motorola telemetry, an electrocardiogram of the activity of the man's heart was being transmitted.

A miracle of electronics—microelectronics—was about to show what it could do.

TECHNOLOGY DOES THE TALKING.

A lot of things were happening at once.

The medical assistants at the scene were talking to the emergency room at the hospital.

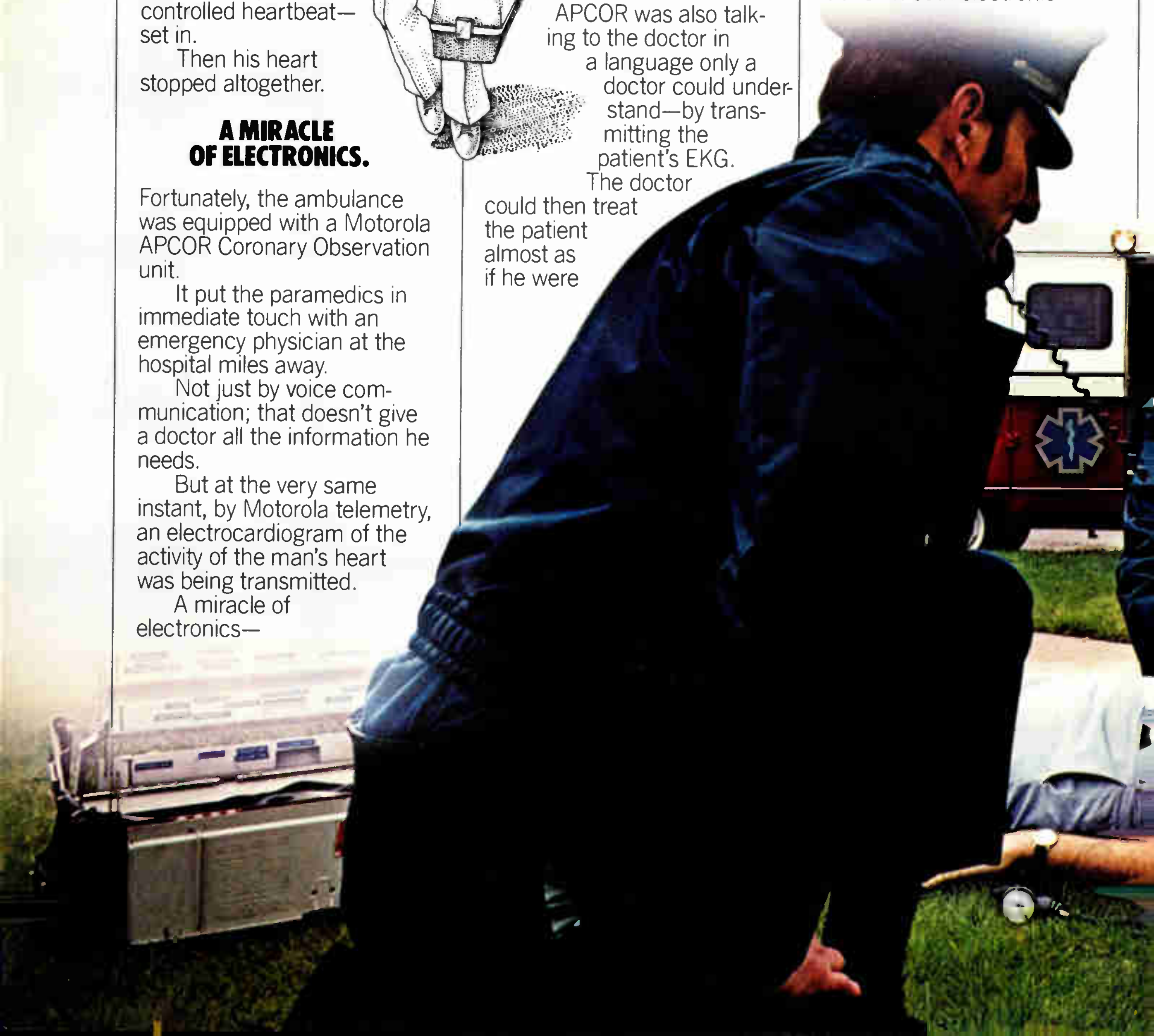
And the Motorola APCOR was also talking to the doctor in a language only a doctor could understand—by transmitting the patient's EKG.

The doctor could then treat the patient almost as if he were on the spot.

In a few minutes, the man's heart began to beat. He was once again on his way to being alive, in every sense of the word.

MICROCIRCUITS MAKE IT HAPPEN.

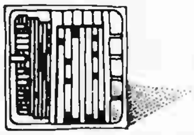
APCOR is made possible by Motorola microcircuits, tiny information processors that transmit both electronic



THIS MAN BACK TO LIFE.

signals and the human voice.

Microcircuitry is also at the heart of the many other kinds of two-way communications equipment we make.



A microcomputer, drawn larger than life.

But communications equipment is only part of what contributes to our nearly two billion dollars a year in sales.

MAKING ELECTRONICS HISTORY.

Thanks to Motorola microelectronics, we create all kinds of remarkable systems that would have been inconceivable not long ago.

A system to help power companies handle peak loads without danger of blackouts.

An electronic car-engine management system that can save gasoline.

Even a communications system to help probe Mars.

But then, we've come a long way from the time we first made history by putting radios into cars (we went on to put alternators and electronic ignitions into them) and later put popular-priced TV sets into homes (they're a product we don't make here at all anymore).

Today, Motorola is one of the world's largest manufacturers dedicated exclusively to electronics, as well as one of its foremost designers of custom and standard semiconductors.

Many of the things we make are changing people's lives.

Others are actually saving them.

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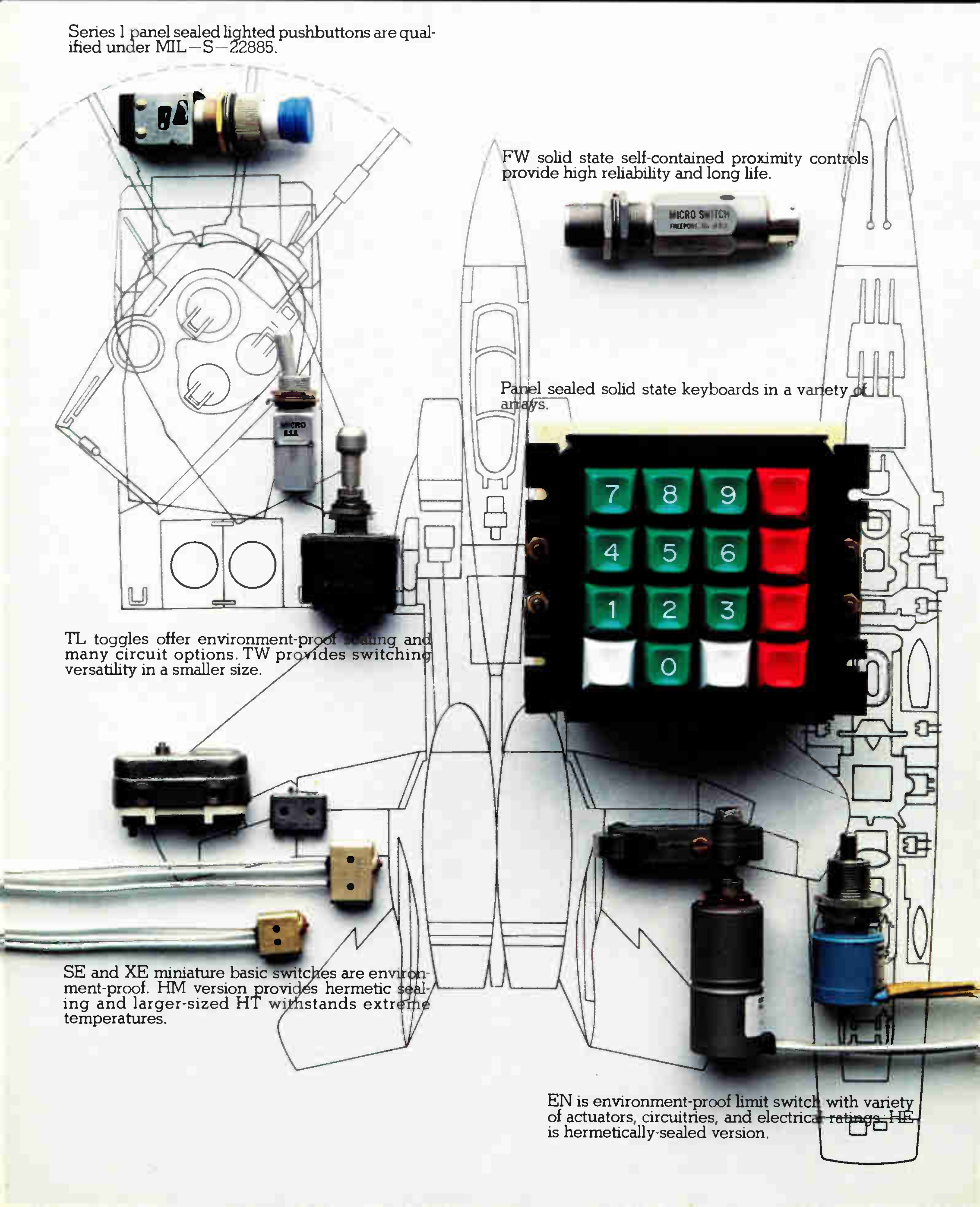


Microwaves

10-GHz transistor delivers 12 dBm

GaAs FET has 3.1-dB noise figure at 14 GHz, is housed in a microstrip package

A 10-GHz microwave chip transistor that can operate linearly while delivering 12 dBm is rare enough. Supply it in a microstrip package that meets the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883, and you have something unique.

Such a transistor is the HFET-2201 from Hewlett-Packard's Microwave Semiconductor division—a gallium-arsenide field-effect device housed in an HPAC-170 package. The package, an in-house design, is configured for easy circuit design in such applications as radar and communications. The transistor body, which is its source, measures 4.3 by 2.5 mm; the microstrip leads of the gate and drain extend out another 4 mm at each side.

The transistor is suitable for both narrow- and broad-band operation at frequencies from 2 to 18 GHz. Its noise figure is typically 2.4 dB at 10 GHz and 3.1 dB at 14 GHz. The saturated drain current is rated at 50 mA for a drain-to-source potential of 3.5 V.

Available from stock, the part is priced at $325 each in quantities of one to nine.

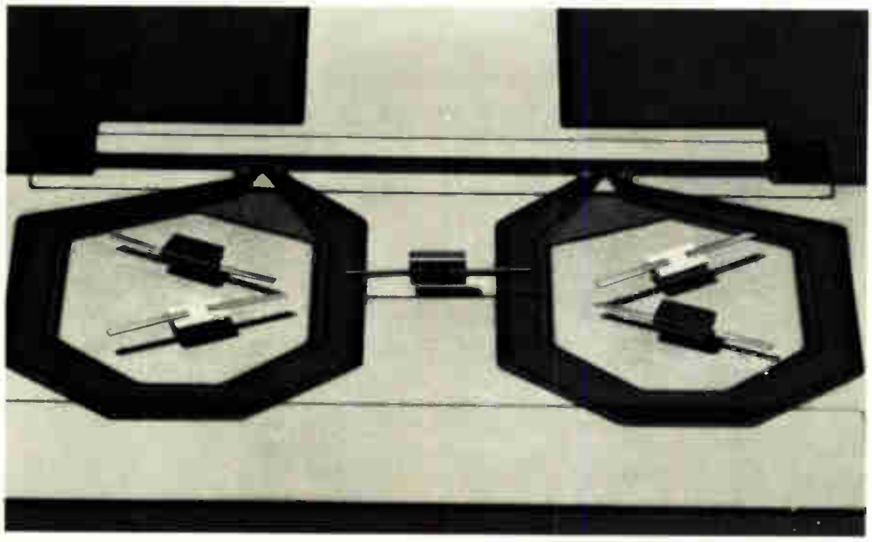
At the same time, the company is introducing an npn bipolar transistor chip that can deliver 29 dBm at 2 GHz. Called the HXTR-5002, the 480-by-380-mm device is designed for a 38% efficiency and third-order intermodulation distortion of −30 dB at 4 GHz. Maximum achievable gain is 7.5 dB at 4 GHz. The HXTR-5002 sells for $29 each in lots of one to nine. Availability is from stock.

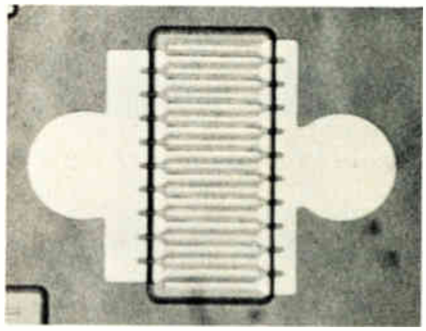
Hewlett-Packard Co., Inquiries Manager, 1507 Page Mill Rd., Palo Alto, Calif. 94304 [401]

Medium-power transistor offered in cost-reducing forms

Intended for low-to-medium-power amplification, a microwave transistor is available in five forms, so that the same device can be used cost-effectively in various applications. In quantities of 100, the transistors sell for as little as $1.40 in chip form and $7.50 in a hermetic strip-line package. At 500 MHz, they offer maximum gains as high as 15 dB and typical noise figures as low as 2 dB at 10 mA, depending on packaging.

The transistors are fabricated using ion implantation and gold top





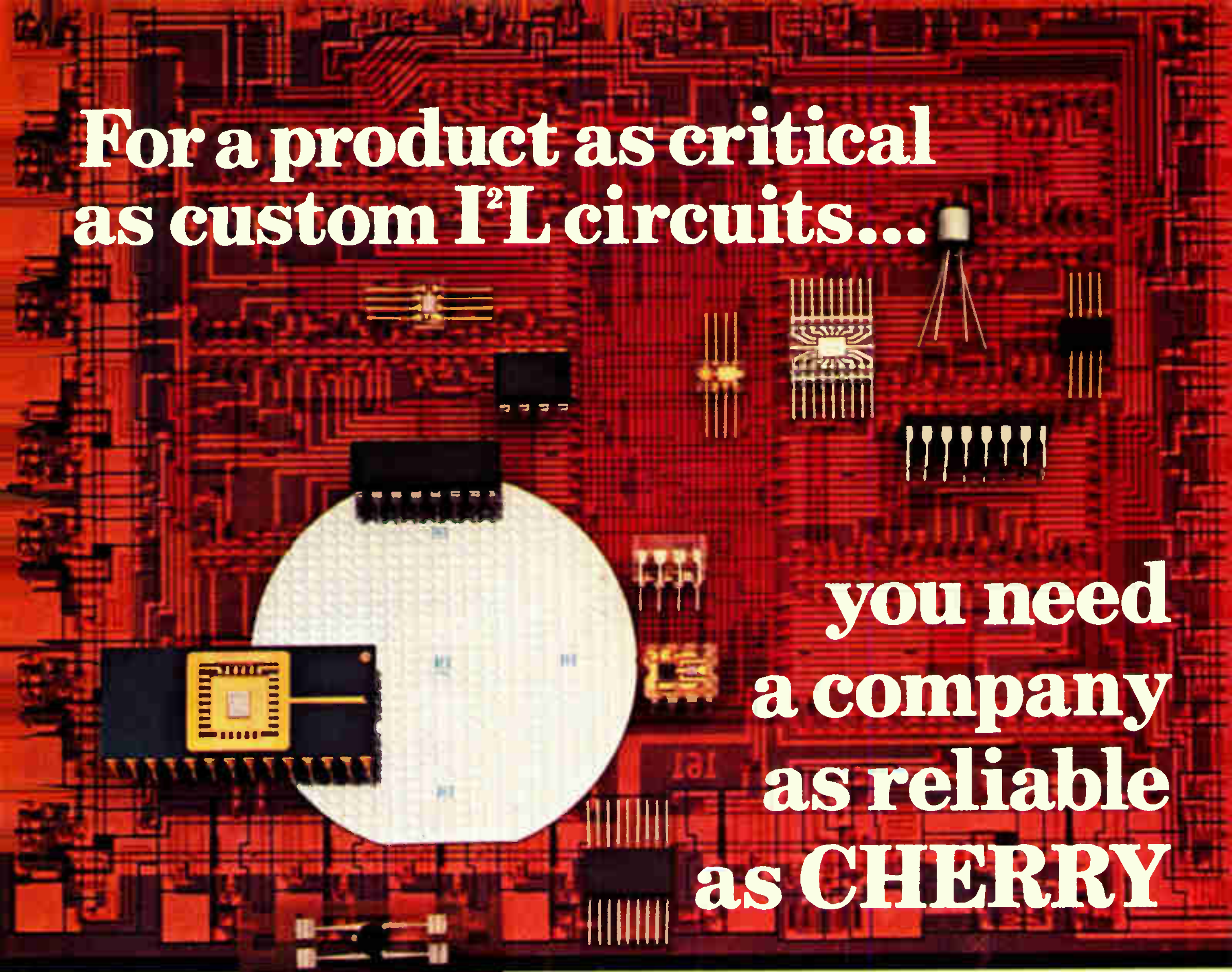
metalization. The former facilitates precise control of dopant densities and gradients and, by using arsenic ions, yields a high transition frequency—the frequency at which the small-signal forward-current transfer ratio (common-emitter) extrapolates to unity—and concomitant noise-figure improvements.

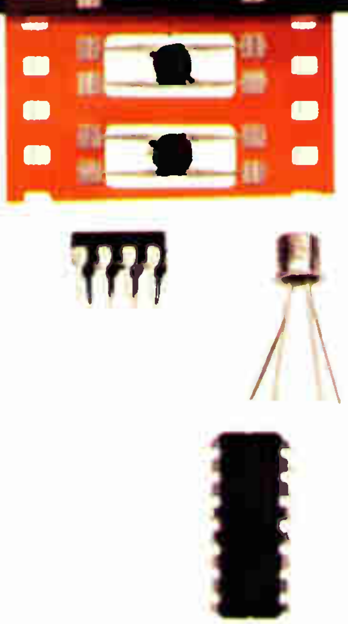
The gold top metalization prevents metal migration caused by high current densities in the fine metal lines required for microwave frequency operation. Unpackaged, the chips are designated BFRC96 and are intended for use in hybrid circuits destined for broadband oscillators and amplifiers.

Transistors are offered in two types of plastic packages: a three-lead MACRO-T, BFR96, and a four-lead MACRO-X, MRF961. Both are suited for use in microwave-transmission cable-television systems, with the MACRO-T offering a direct replacement in existing board designs and the MACRO-X providing 2.5-dB higher gain that results from its opposed-emitter design. In either package, units are priced at $1.75 in hundreds.

The device also comes in a metal or a metal-ceramic package. In a standard TO-46 can, the unit is designated MRF965 and can be used in high-gain Class C amplifier applications at output powers of up to 400 mW; it is priced at $2 in quantities of 100. The MRF962 sports a hermetically sealed stripline package that allows it to be specified for 2-GHz operation. Compared to the same die in a MACRO-T package, the MRF962's gain is typically 6 dB higher.

Motorola Semiconductors, P. O. Box 20912, Phoenix, Ariz. 85036 [403]





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VAX-"An implementor's dream."

—Dr. Brian Ford, Director, Numerical Algorithms Group
Oxford, England/Downers Grove, Illinois

For the Numerical Algorithms Group, the plain fact is this: "Software implementation was faster on the VAX-11/780 than on 25 other major machines."

Before VAX, Dr. Ford's staff had implemented NAG's complex FORTRAN Mark 6 Library on 25 major machines ranging from minis to mainframes, including the Burroughs 6700, CDC 7600, Univac 1100, and IBM 370. The average implementation time was 13 man-weeks.

VAX took five.

In Dr. Ford's words, "The NAG FORTRAN Mark 6 Library consists of 345 subroutines covering the major areas of numerical mathematics and statistics. It's used in applications such as structural design, nuclear physics, economic modeling, and academic research.

"A successful implementation requires the correct functioning of the 345 library routines to a prescribed accuracy and efficiency in execution of NAG's suite of 620 test programs. Whilst the activity is a significant examination of a machine's conformity to the ANSI standard of the FORTRAN compiler, its main technical features are file creation, file comparison, file manipulation and file maintenance."

And then there was the record of VAX reliability: "No problems were encountered in the VAX/VMS software even though approximately 3000 files were being handled. The operational availability time for the machine was close to 100%, an outstanding statistic for new hardware and a new operating system."

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Semiconductors

Chip mates drives and CPUs

Format-independent data handler works with cartridges and cassettes

Central processing units are bus-oriented. Cartridge and cassette drives, however, accept and supply data in a serial format. When hooking a CPU to a drive of this sort, a number of chips are needed to massage the data in both directions to ensure compatability between the inherently dissimilar devices. To make this task more manageable, Standard Microsystems Corp. has designed the CCC 3500 cartridge and cassette data handler.

During a write operation, this 40-pin metal-oxide-semiconductor integrated circuit receives data from the processor and shifts it out bit-serially to the data-encoding logic and on to the drive as shown in the figure. In a similar manner, the 3500 accepts serial streams of data from recovery circuitry during a read operation. The IC establishes byte synchronization by detecting the sync byte and transfers data on a byte-by-byte basis back to the CPU.

The 3500 also takes care of many control functions. For example, it detects data overrun and underrun error conditions and flags them through its status lines.

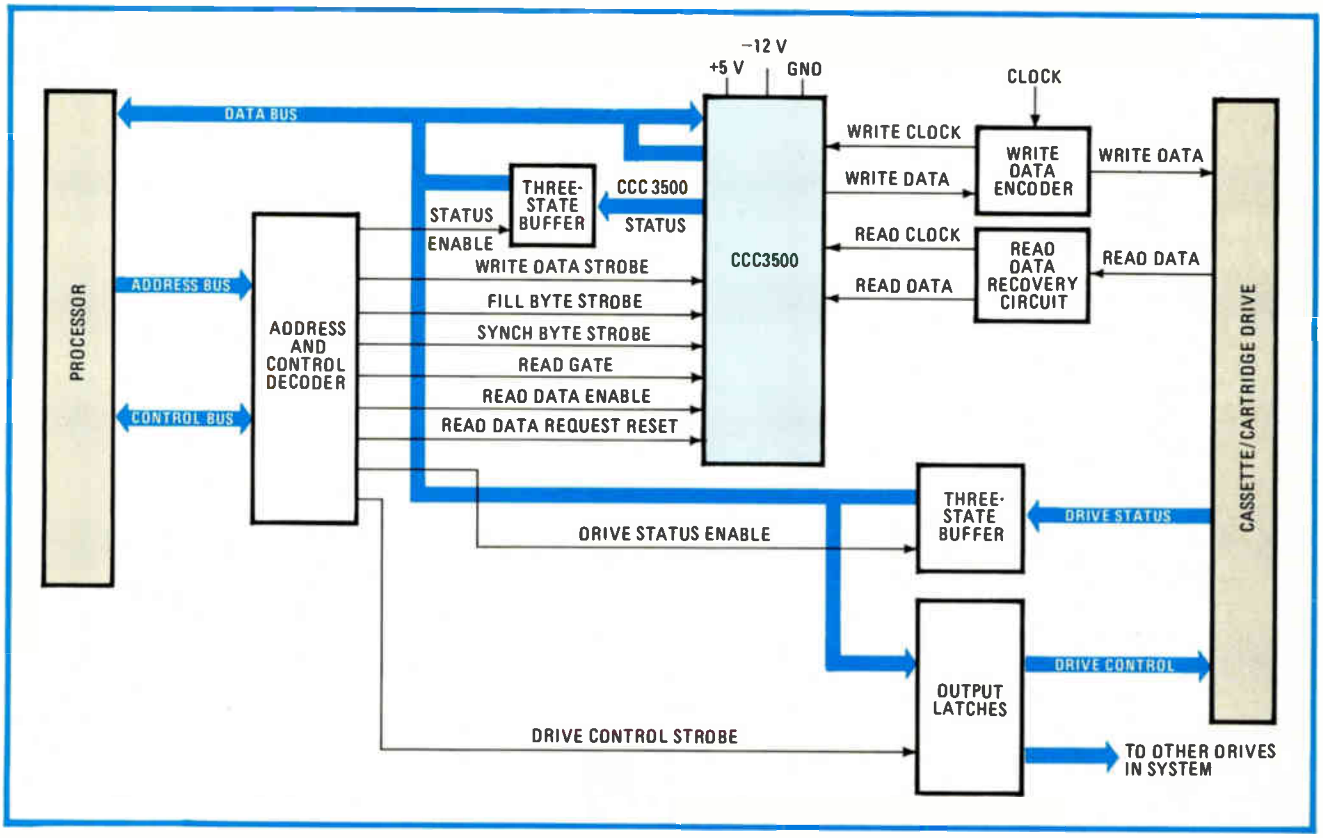
Another special feature of the chip is its separate read and write registers. Separate registers allow read and write operations to occur concurrently when dual-headed drives are used. Such drives may read and write simultaneously to verify data, thereby upping both throughput and reliability.

The 3500 is format-independent and can be interfaced with any existing drive for standard or mini cassettes and standard or mini 3M-type cartridges. According to John Tweedy, product planning manager for SMC, "Data coding and decoding are done external to the chip—the 3500 is capable of handling the data derived from these operations regardless of the format."

Moreover, the chip can operate with data rates of up to 250 kilobits/second. "The fastest I've seen for a 3M cartridge is 192 Kb/s," says Tweedy, "and a standard rate is about 48 Kb/s, making our chip capable of handling rates more than five times as fast."

The 3500 has a three-state output bus for processor compatability and transistor-transistor-logic inputs and outputs. The chip is available now and sells for $8.90 in quantities of from 100 to 499 and $7 in quantities of 1,000 or more.

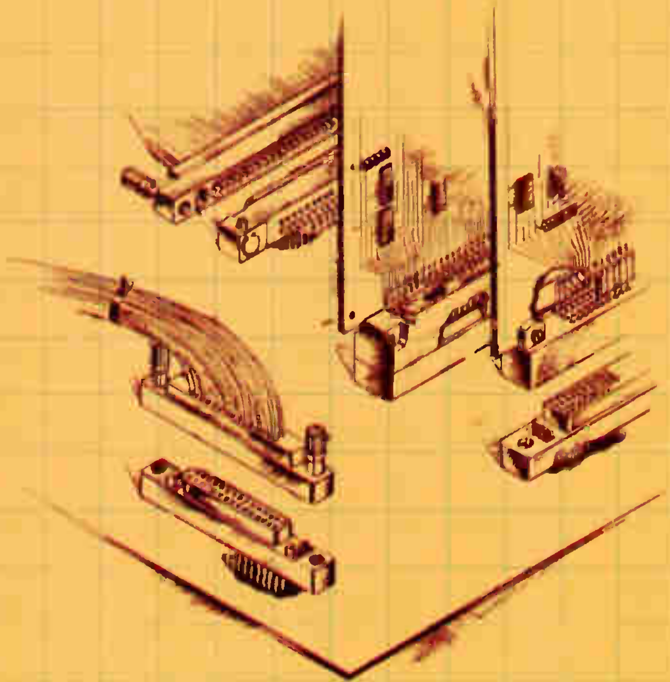
Standard Microsystems Corp., 35 Marcus Blvd., Hauppauge, N. Y. 11787. Phone (516) 273-3100 [411]



Static RAM crams 8 kilobytes into 18-pin DIP

How do you put a 1-K-by-8-bit static random-access memory into a dual

PCB Flexibility with Bendix Brush Connectors.



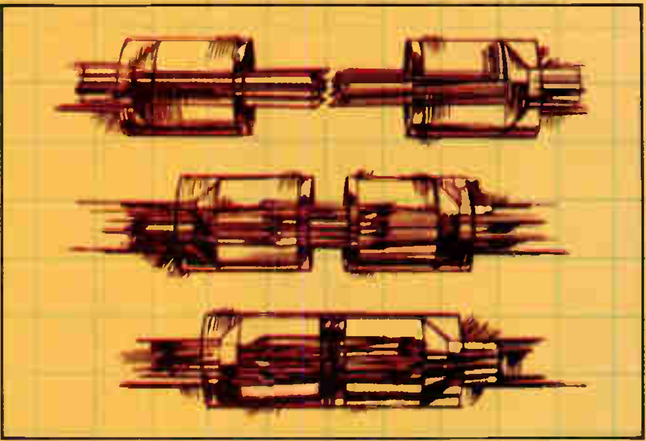
A low mating force connector with up to 400 contacts. 4 body styles. 3 contact variations with options. Superior electrical characteristics and long mechanical life. That's flexibility! And Bendix has one for your high-contact needs. The Brush Connector. Here's what you get.

Bendix Brush Connectors increase circuit count per board.
- Reduce number of boards by allowing more circuits per board.
- Greater board effectiveness by providing exact circuit counts up to 400 contacts in only one connector!

Bendix Brush Connectors reduce mating force 70% to 90%.
- Less complex board supports.
- Secondary actuators eliminated.
- Extended mechanical life. Up to 20,000 mates/unmates.
- Fewer damaged boards.
- Eliminates fixture mounting need of multiple smaller connectors.

Bendix Brush Connectors—a broad product line.
- Mother Board, Daughter Board, Input/Output, PC receptacle body styles.
- 2, 3 and 4 row configurations.
- 90° and straight PC, solderless wrap, crimp removable terminations with multiple lengths and plating options.

Bendix Brush contacts improve electrical characteristics.
- Highly redundant contact sites with multiple electrical paths and wiping action.
- Gold plated wire bristles mesh together intimately with gas-tight junctions.
- Stable contact resistance even after extreme mechanical durability abuse to 20,000 matings.



For full information, call (607) 563-5302, or write The Bendix Corporation, Electrical Components Division, Sidney, New York 13838.

Bendix

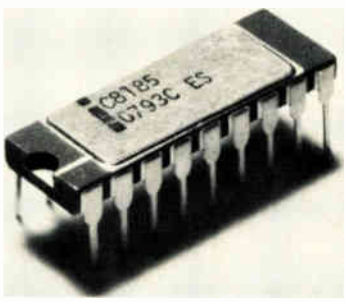
We speak connectors.

in-line plastic package with only 18 pins? The obvious answer for Intel, originators of the 8085, was to use the same technique used in designing that microprocessor to put address and data onto the same lines—multiplexing.

Without the need for separate address and data lines, a device can be configured with either a greater number of functions or fewer pins. For the 8185 RAM, the decision was made to concentrate first on package size, so the number of pins was reduced and package size shrank in accordance with industry standards for an 18-pin DIP.

Several of the excess pins, however, were retained to provide increased functional options for the user. For example, the 8185 has both an active-high and an active-low latched chip enable.

One of these latched chip enables can be used as a standard chip enable while the other serves to power down the chip during input/output or interrupt cycles. Thus power consumption—the unit draws a maximum of 500 mW when active and only 125 mW when quiescent—can be further minimized.



The RAM also has an unlatched chip select that holds the chip inactive even when the unit is powered up by the enable pins, and it provides separate pins for read and write control functions, too.

Two versions of the 8185 are being offered, one for the standard 8085A and a faster chip for the 5-MHz 8085A-2. Both types work from a single 5-V supply and are available in sample quantities now. The standard 8185 sells for $37.50 each in quantities of 100. Production deliveries will begin this quarter.

Intel Corp., 3065 Bowers Ave., Santa Clara, Calif. 95051. Phone Rob Walker at (408) 987-8080 [413]

Dc-motor speed control fits in 14-pin DIP

Intended primarily for applications involving ac tachometer signals, the model CS-175 dc-motor speed control is an inexpensive circuit that fits in a 14-pin dual in-line package. The units lists for $1.68. In lots of 1,000 pieces, it sells for 79¢, whereas in quantities of 10,000 pieces, the price drops to 65¢.

Cherry Electrical Products Corp., 3600 Sunset Ave., Waukegan, Ill. 60085 [417]

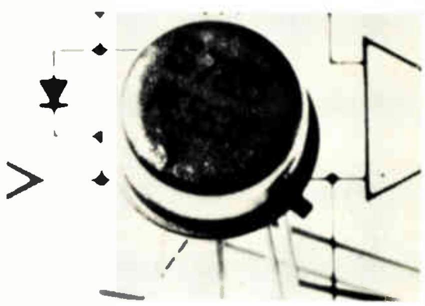
Sample-and-hold amplifier has short acquisition time

Designated the NE5537, a monolithic sample-and-hold amplifier circuit uses ion-implanted field-effect transistors in combination with bipolar devices to obtain an acquisition time of under 10 μs. The approach also improves accuracy and decreases the droop rate.

The device operates from ±5-V to ±18-V supplies. Logic inputs are fully differential with low input current (typically 10 nA), allowing direct connection to transistor-transistor-logic and complementary-metal-oxide-semiconductor devices. The output can drive a 2-kΩ load.

Housed in a TO-5 can, the 5537 is available from stock. In 100-piece quantities, they cost $3.50 each.

Signetics Corp., 811 E. Arques Ave., P. O. Box 9052, Sunnyvale, Calif. 94086. [415]



The Series 6000 combines all the functions of these instruments: DC Voltmeter • DC/DC Ratiometer • AC Voltmeter • AC/AC Ratiometer • dB Meter • Ohmmeter • DC Millivoltmeter • 2 Channel Scanner + DMM • DC Amplifier • Comparator Box – up to seven sorting "bins" • Fault Alarm – Single or multiple limit • High Speed Digitizer • A/D Converter • Voltage Deviation Meter • Gain/Attenuator Meter • Computing Multimeter with: Averaging, Min/Max Peaks, Scaling/Factoring, Self Test, Self Calibration, Digital Offsets, Hi/Lo Limits.

Over 34,000 readings per second, a 'third generation' IEEE-488 interface and built-in diagnostics combine to make the new Series 6000 the ultimate systems instrument.

The Racal-Dana 6000 is the culmination of ten years of benefits-oriented engineering, incorporating many measurement capabilities never before available... at a price that's less than a traditional systems DVM.

A **sample and hold** option, when used with the high speed digitizer, allows precise timing of measurements and extremely short sample times. **Full annunciation** of all programmed conditions assures easy software development.

Automatic timeouts during input setting, and inhibited output during autorange prevents erroneous readings. Five **programmable integration times**, six programmable trigger modes, and an auto-test/auto-cal routine provide the ultimate in flexibility.

See for yourself why the new Series 6000 Amplitude Measurement System is an instrument so unique that it even needed a new name. More important, find out how it can save you valuable systems dollars while cutting your systems design time. Call or write today.

RACAL-DANA

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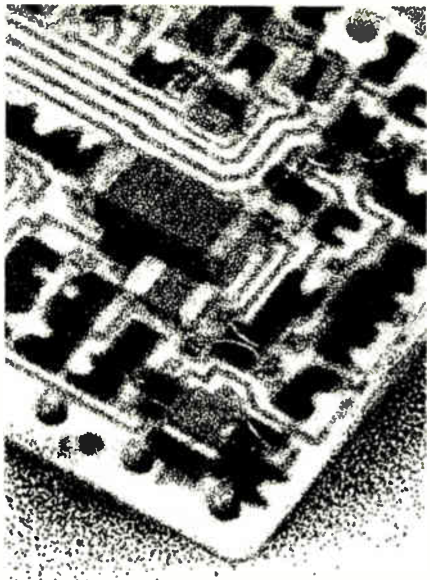
RACAL-DANA INSTRUMENTS, 18912 Von Karman Avenue, Irvine, CA 92715; Ph: 714/833-1234; Duke Street, Windsor, Berkshire SL4 1SB, England, Ph: (07535) 69811; 91 Route de Gardes, 92 Meudon-Bellevue, France, Ph: 027-7575.

Circle #173 for Literature only

Circle #228 for Product Demonstration



Computers & peripherals

Prime aims at IBM's midsection

Four 32-bit machines and enhanced software also compete with VAX 11/780

Four new 32-bit computers and enhanced distributed processing software from Prime Computer Inc., are said to offer users performance comparable to a mid-range IBM mainframe computer at traditional minicomputer savings. The new units bolster the competitive stance of rapidly growing Prime.

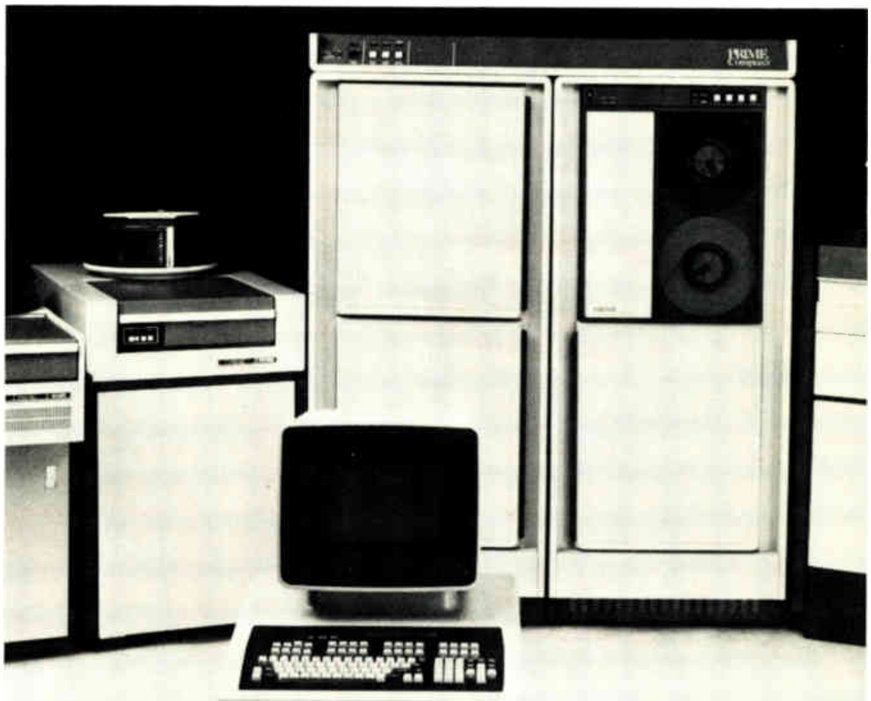
Indicative of this broadened stance is the new model 450. It is aimed at systems and software houses who will buy the unit in large quantities and remarket it to the less sophisticated end users Prime has up to now avoided.

The 450 and the other three units, the 550, 650, and 750 [*Electronics*, Dec. 21, 1978, p. 25], have similar processor characteristics, but differ in memory capacity, options, and hence processing speed. Based on Schottky transistor-transistor logic, the central processing unit has a cycle time of 200 ns, uses a bipolar cache memory with an 80-ns access time, and has main memory with an access time of 600 ns.

The three larger machines can support up to 63 simultaneous users, each addressing up to 32 megabytes of virtual memory, whereas the 450 supports up to 32 users. The top-of-the-line 750 has 16 kilobytes of cache memory, an instruction-prefetching unit, two-way interleaved memory, a burst input/output mode that permits data transfers at up to 8 megabytes per second, and a standard floating-point processor. According to Joseph d'Angelo, director of planning, it is competitive with DEC's VAX 11/780.

Less powerful without instruction prefetching is the 650, which has 2 kilobytes of cache memory and up to 4 megabytes of main memory. The 550 does not have the floating-point processor, but has 2 kilobytes of cache memory and up to 2 megabytes of main memory. The 450, similar to the 550, supports up to 1 megabyte of memory.

At the same time, Prime revamped its Primenet networking



Circle 176 on reader service card

software, increasing its distributed processing capabilities through three sets of programs. The Inter-Program Communications Facility, operating under the Primos operating system, lets programs establish full-duplex communication paths to other programs in the same or another Prime computer. Remote terminals attached to other Prime systems or to a packet-switching network can communicate with a Prime system and operate as if they were directly attached to that system by means of the Interactive Terminal Support Facility. Programs on one Prime system can use data files physically stored in another such system using the File Access Manager software.

Primenet software can be used to connect any mixture of Prime models 750, 650, 550, 500, 450, 400, and 350, as well as other vendors' computers, the company says. For local networks where no system is more than 750 feet from another, a Primenet Node Controller is placed on each computer and connects it to up to seven other systems in a ring network made up of coaxial cable.

The high-speed multiple-data-link controller is used to connect geographically dispersed units over synchronous communications lines or X.25 packet-switched networks. Primenet software costs $12,000 with X.25 compatibility, $7,000 without.

Available for delivery next summer, the Prime 750 ranges in price from $180,000 to $300,000; the 650 and 550, available now, run from $150,000 to $250,000 and from $95,000 to $175,000, respectively. First deliveries of the 450 are scheduled for April, with quantity prices starting at $35,000.

Prime Computer Inc., 40 Walnut Street, Wellesley Hills, Mass. 02181 [361]

Cobol on the way for VAX-11/780

Those waiting for a common-business-oriented language that would take full advantage of the VAX-11/780's 32-bit architecture need be patient only a little longer. Starting in March, copies of VAX-11 Cobol-74 will be available for a single license fee of $7,700.

Conforming to ANSI's 1974 standard, the language implements the nucleus, table-handling, and input/output modules for sequential, relative, and indexed-sequential file access. Also provided are interprogram communication and a library facility.

VAX-11 Cobol-74 will accept packed decimal data and can use the VAX-11 string manipulation instructions. Use of a 32-bit object code provides transparent access to the DECnet and the use of VAX virtual memory space. It also allows subroutine calls to and from other VAX-11 languages, as well as direct calls to the operating system.

To bow in March, too, are two facilities, which will be bundled with the operating system for new deliveries. The multikey, indexed-sequential-access-method (ISAM) facility provides a primary key and as many as 254 alternative keys for access to each record. The sort facility, as its name implies, sorts data—according to record, tag, address, and index. It is modular, with flexible memory requirements, and can be used in either a stand-alone mode or as a subroutine.

Digital Equipment Corp., Maynard, Mass. 01754 [363]

Graphics display is compatible with IBM 3277

The Tektronix 618 storage display monitor is fully compatible with the IBM RPQ 7H0284 graphics attachment for the IBM 3277 terminal. The addition of the 19-in. monitor makes up a dual display station: the 3277 dislays alphanumeric data while the 618 presents graphic information and special symbols. Priced at $8,700 with quantity discounts obtainable or available for lease at $348 a month for 36 months, the 618 will be available in March 1979.

Tektronix Inc., P. O. Box 500, Beaverton, Ore. 97077 [364]

Instruments

Signal generator spans 520 MHz

1,040-MHz range and IEEE-488 bus compatibility are options for low-noise unit

Already well known for its laboratory-quality signal generators, West Germany's Rohde & Schwarz is now aiming to meet the needs of personnel who must provide field service for modern high-performance receiving systems. The company's model SMS synthesized signal generator, which is also well suited for testing such components as sharp-cutoff surface-wave and crystal filters, is both versatile and easy to use, "something the on-site technician may value most," says Dieter Burkhart, who headed its design.

The SMS combines the latest synthesizer technology with microcomputer control in a fully programmable instrument—one that optionally can work with the IEEE-488 general-purpose interface bus. The basic unit covers the range from 400 kHz to 520 MHz with a resolution of 100 Hz; an optional doubler extends that range to 1,040 MHz. The generator's output level can be set in 0.1-dB steps from −137 dBm to +13 dBm. Maximum total amplitude error is 1.5 dB.

The standard generator drifts less than one part in 10^6/°C. An optional temperature-controlled reference oscillator improves this to one part in 10^7 from 0° to 50°C. The standard oscillator has an aging drift of one part per million per month; the high-stability option drifts only 1 ppm per year. At 20 kHz from the carrier, the instrument's phase noise is typically −120 dB/Hz.

A neat arrangement of front-panel controls, plus separate digital indicators for frequency, level, and modulation, makes the SMS easy to operate. The values for the displayed parameters may be entered directly from a single keyboard.

An eight-digit readout displays the frequency in megahertz. Level is shown on a four-digit display in microvolts, millivolts, dBmV, or dBm. Modulation is indicated on a three-digit readout that goes up to 90% for a-m and 125 kHz for fm.

Slated for delivery both in the U.S. and in Europe in March, the instrument carries an FOB price tag of 12,500 Deutschmarks, which is equivalent to about $6,830 at the current exchange rate. The frequency-doubling and IEEE-488 bus options add $1,040 and $245, respectively. The high-stability reference oscillator goes for $490, and $245 more buys overvoltage protection.

Rohde & Schwarz Sales Co., 14 Gloria Lane, Fairfield, N. J. 07006 [351]

Rohde & Schwarz, 8000 Munich 80, P. O. Box 801469, West Germany [352]

Scope has separate control and programming units

Suppose there were a number of different locations, on various production lines or in the field, for example, where having a programmable oscilloscope would be desirable. Would it not be advantageous to pay just once for the means to originate programs for the scopes, rather than each time a scope was purchased?

A series of instrument modules offers purchasers that option. Consisting of four individual units—the model 5810 oscilloscope, the 5812 programmer, the 5811 program-control unit, and the 5813 multiprobe controller—the series separates the functional aspects of a programmable scope so that only those required need be purchased.

The 5810 is a 20-MHz dual-channel scope with an effective display of 8 by 10 divisions. It has calibrated sensitivities of from 5 mV/div to 2 V/div and is accurate to within ±3% of full scale. Unlike other programmable scopes, the unit has front-panel controls only for setting the usual variety of continuously variable functions; six values can be preset for such functions as vertical trace position, vertical gain, sweep speed, and trigger level. Three values of the horizontal trace position may be set also.

The controls for the discrete scope functions are all on the 5812 programmer, which can remotely supply transistor-transistor-logic–level signals to the scope, by means of two 50-pin connectors, to set up those values. The 5812 may also be used to program the 5811 control unit, which can store a sequence of up to 32 sets of scope parameters. The control unit can run back and forth through that sequence and select a particular set for the scope without the use of the 5812.

The multiprobe controller accepts inputs from eight different probes, four for the X channel and four for the Y, and under the direction of the controller, selects one for display on the appropriate channel.

Prices for the 5810, 5811, 5812, and 5813 are $2,614, $741, $1,058, and $582, respectively.

Leader Instruments Corp., 151 Dupont St., Plainview, N. Y. 11803. Phone George Zachmann at (516) 822-9300 [353]

RELAX...it's amazing how an easy mind helps build a home.

We're the easy mind people. TRW Capacitors.

We can solve your problems connected with reliability in ultra-miniature capacitors. Our X463UW metallized polycarbonates are designed to do just that.

The X463UW gives you "Space Age" performance in circuits demanding the smallest possible size. Capacitances range from .001 to 10 mfd, at 50, 100, 200 and 400 vdc—with less than 1.5% capacitance change from −55°C through 125°C. IR is 60,000 megohm x mfd minimum at 25°C. DF is less than 0.3% at 25°C and 1 KHz. And stability? In humidity and shelf life tests the stability of the X463UW is actually two to three times better than polysulfone.

You get all that because we've applied the latest in component technology to combine the improved electrical performance of polycarbonate with dramatic size and weight reductions made possible by the use of our exceptionally reliable metallized dielectric.

We also put the same kind of effort into our engineering services and our field support. Try us. We can help reduce the tension. Give us a call, or write: TRW capacitors, An Electronic Components Division of TRW, Inc., 301 West "O" St., Ogallala, Nebraska 69153. Tel: (308) 284-3611.

TRW CAPACITORS

ANOTHER PRODUCT OF A COMPANY CALLED TRW

Circle 179 on reader service card

Data acquisition

LSI-11 board has 32 inputs

Other members of board family are an output-only unit and an I/O combination

The strategy at Analog Devices in its maturing microcomputer analog input/output subsystem business hasn't always got the company out first with boards that mate with a given system, but there has usually been a performance and price attraction. The story is no different with the latest series—the RTI-1250, intended for users of Digital Equipment Corp.'s LSI-11 and LSI-11/2 microcomputers.

There are three boards in the series, all with 12-bit resolution: the RTI-1250 input-only board, the RTI-1251 combination I/O board, and the RTI-1252 analog output subsystem. Each is on a single half-quad-sized board; each includes an on-board dc-to-dc converter as standard; and each appears to the microcomputer as a block of four memory-mapped address locations.

Whereas competitive input boards offer 16 single-ended input channels (8 differential), the RTI-1250 provides 32 single-ended inputs (16 differential). There are two versions—one with a resistor-programmable-gain instrumentation amplifier (RTI-1250-R), and one with a software-programmable-gain amplifier (RTI-1250-S). The latter allows the user to select gains of 1, 2, 4, or 8 and is priced at $645 in quantities of one to nine. The RTI-1250-R, at $560, may be used for input ranges from ±10 mv full scale to ±10 v full scale.

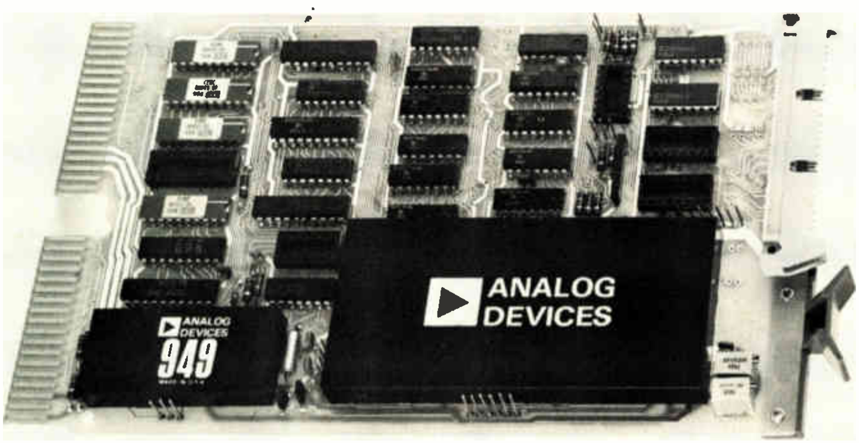
Barry Glasgow, marketing manager of microcomputer peripherals, says the RTI-1250 is the only input board for the LSI-11/2 that provides up to 32 channels and the choice of resistor- or software-programmable-gain amplifiers. He is especially enthusiastic about the RTI-1251 combination board, maintaining that it is the first I/O board that offers 16 channels of 12-bit input plus two 12-bit digital-to-analog voltage outputs. "We think this is the major contribution of the series," he says. There are two 12-bit multiplying d-a converters providing up to ±10 v of analog output in several ranges.

Finally, the RTI-1252 board provides up to four channels of output, using Analog Devices' own AD DAC-80 d-a converters. It also has four digital logic drivers for simple on/off applications.

"We've done something interesting," Glasgow says, "in that two of the DAC-80s are soldered and two are socketed, so that the user can expand in the field" if he wants to start off with two output channels.

A two-channel RTI-1252 will sell for $460, or the customer can get all four channels from the factory for $550. "But all he needs to expand to four from two himself is a digital voltmeter to trim the offset and gain" of the DAC-80s, Glasgow notes. "The digital circuitry is there to support all four outputs." Optional voltage-to-current converters are also available for 4-to-20-mA outputs. Delivery time for all units is three to four weeks.

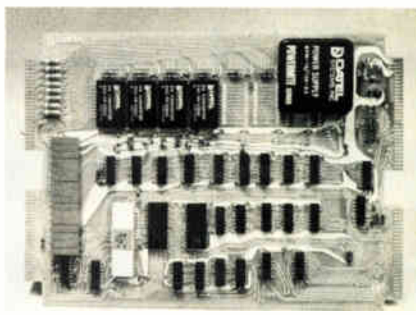
Analog Devices Inc., Route One Industrial Park, P. O. Box 280, Norwood, Mass. 02062. Phone Russ Vernooy at (617) 328-4700 [381]



4- and 8-channel d-a boards compatible with microNovas

Owners of microNova computers who would like to control real-world variables analogically can now turn to a series of digital-to-analog conversion boards designed for their particular machine. These boards slide directly into the microNova's card guides and are compatible with its input/output pinouts.

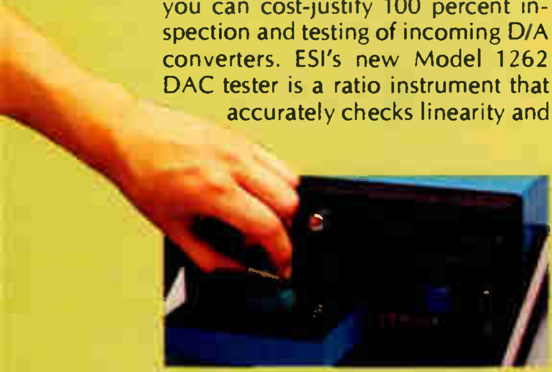
Three versions of the basic board are being offered: two four-channel units, the ST-MNOVA-DA4A and B, and an eight-channel model, the ST-MNOVA-DA8B. The four-channel boards differ in powering and price; the A model has an on-board ±15-v dc-to-dc converter and



Model 1262 accurately reads wide variety of DACs for linearity, montonicity. Price: $2960.

DAC linearity deserves a credible test.

Now — perhaps for the first time — you can cost-justify 100 percent inspection and testing of incoming D/A converters. ESI's new Model 1262 DAC tester is a ratio instrument that accurately checks linearity and



monotonicity. Under microprocessor control the 1262 readily supports:

...different input codes (BCD, inverted BCD, and several binary codes);

...different number of input bits (up to 12) and,

...different analog outputs (voltage or current) in either polarity.

And it handles both DACs which require full time data or those for which data must be latched through strobing signals (microprocessor compatible).

Test results are presented in 2 seconds plus selected warmup time via front panel LEDs showing absolute and differential linearity as fractions of one least significant bit, and any evidence of nonmonotonic behavior. Test fixture LEDs signal PASS, FAIL, and the presence of excessive superposition (bit addition) error.

Test fixtures the key

The instrument achieves its flexibility through a number of personalized test fixtures. You can be testing BCD current DACs one moment, and binary voltage DACs the next, simply by changing test fixtures according to the pin configuration of the test fixture. Each contains a zero insertion force test socket, the analog circuitry to process the output signal of the device under test, and switches and jumper wires on the fixture's PCB, used to select code formats, pretest warmup time, and the pass/fail specifications for the DAC type to be tested.

The user makes no adjustments within the instrument.

For complete information, call or write, Electro Scientific Industries, 13900 N.W. Science Park Drive, Portland, Oregon 97229, phone (503) 641-4141.

25 years

esi ELECTRO SCIENTIFIC

Circle 181 on reader service card

costs $630; the B model requires an external source of ±15-V, 160-mA dc power but costs $80 less. The eight-channel model also requires external ±15-V power, at twice the current rating, and is priced at just $785.

All the boards convert straight binary, offset binary, or 2's complement inputs into analog signals using 12-bit d-a converters whose outputs settle to within ±½ least significant bit within 4 μs. The slew rate is 20 V/μs.

Output ranges are jumper-selectable from among unipolar ranges of 0 to 5 V and 0 to 10 V and bipolar ranges of ±5 and ±10 V. Zero and offset temperature drift are 5 ppm of full-scale range/°C, gain temperature drift is 30 ppm (full scale)/°C, and maximum nonlinearity is within ±½ LSB.

With their output impedance of 50 mΩ, these boards can deliver up to 5 mA. They are specified for commercial temperatures and are optionally available with 16-bit digital ports, each of which replaces a d-a converter. Delivery time for all models is from four to six weeks.

Datel Systems Inc., 1020 Turnpike St., Canton, Mass. 02021. [383]

Intelligent converter works with Multibus or alone

Compatible with systems built around the Multibus, the MLZ-DAQ can be used as an intelligent analog-to-digital conversion board. But because of that intelligence, it can also be used as a stand-alone data-acquisition system.

Seat of the system's intelligence is the on-board Z80A microprocessor, which can converse with other external devices by means of two RS-232-C communications ports. The unit is supplied with 1 kilobyte of read/write memory and sockets for 4 and 8 kilobytes of erasable programmable read-only memory.

The MLZ-DAQ's conversion capabilities spring from the use of an ADAM-12 or an ADAM-12APG module, which can accept 16 or 32 channels of analog inputs in either the 0-to-5-V or the 0-to-10-V unipolar range or the ±5- or the ±10-V bipolar range. For differential monitoring, input lines can be paired, and with the ADAM-12APG module, software-programmable gains of 1, 2, 5, or 10 can be selected.

In single quantities, prices for the MLZ-DAQ start as low as $545.

Heurikon Corp., 700 W. Badger Rd., Madison, Wis. 53713. Phone Christopher Priebe at (608) 255-9075 [384]

Synchro-to-BCD converter lets user select scale factor

The SBC40 series of synchro-to-binary-coded-decimal (BCD) converters offers users a choice of scale factor so that the three- or four-digit output can be tailored to the tolerances of a particular application. Inputs, from a synchro or resolver of 11.8 or 90 V at 400 Hz, are converted into BCD outputs with errors that will not exceed ±6 or ±30 minutes

of arc, respectively.

Outputs can represent either unipolar or bipolar ranges and are transistor-transistor-logic-compatible. A reference input of either 26 or 115 V, 400 Hz, is required in addition to 15-V and 5-V power; synchro and reference inputs are isolated.

Units are available for the commercial and industrial operating temperature ranges and are priced at less than $375 in production quantities. Delivery time is four weeks.

Computer Conversions Corp., 6 Dunton Ct., East Northport, N.Y. 11731. Phone (516) 261-3300 [385]

The only 40 column printer with NCR reliability.

It's field proven and available in quantity now.

Compare this low cost, 40-column printer with others available. You'll get these *extra values*.

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- Produced in quantity with NCR quality control
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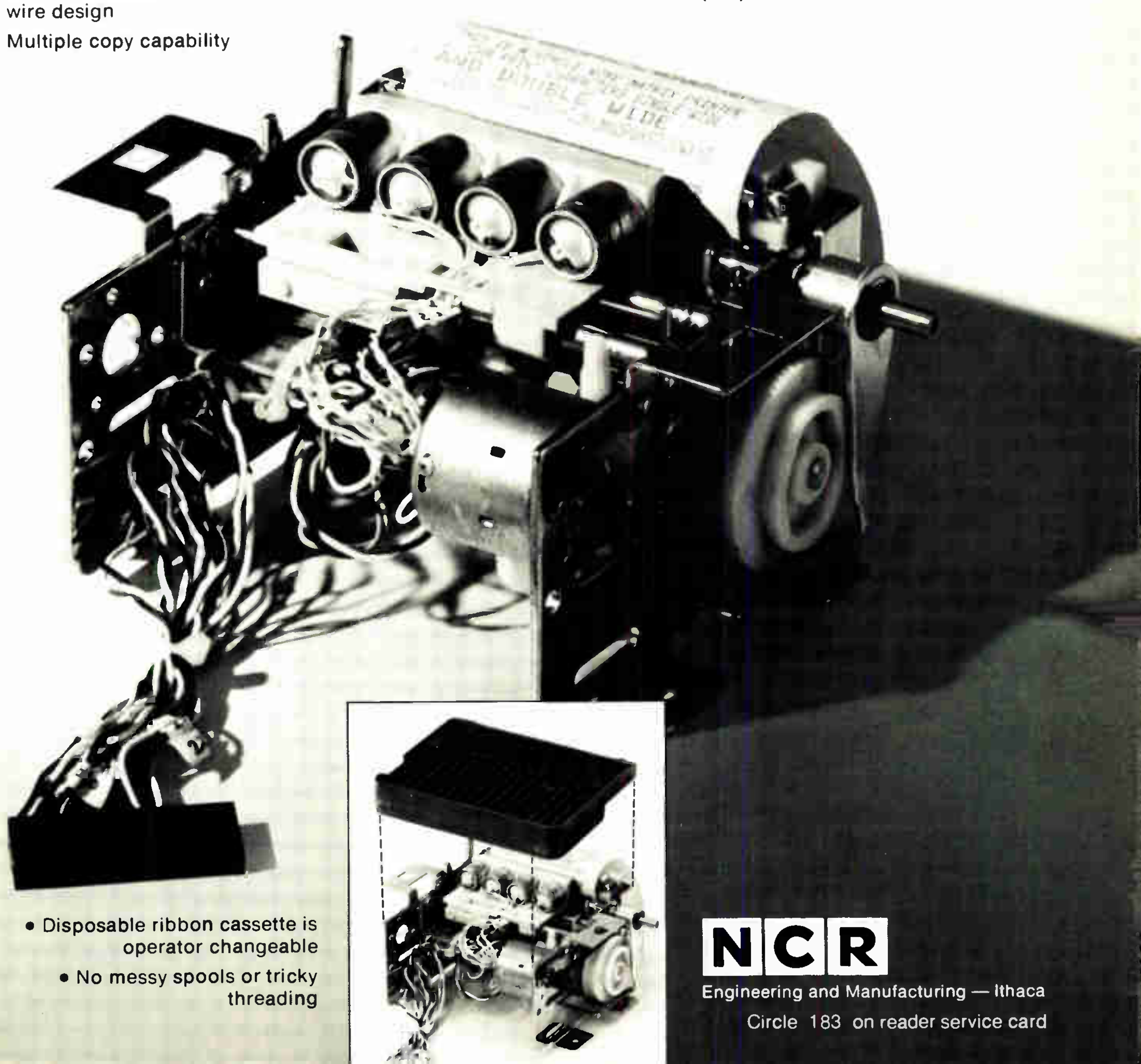
- Attractive quantity pricing

For delivery information, prices, or literature, please contact us at NCR Engineering and Manufacturing, OEM Marketing, P.O. Box 627, Ithaca, New York 14850 (607) 273-6066.



- Disposable ribbon cassette is operator changeable
- No messy spools or tricky threading

NCR

Engineering and Manufacturing — Ithaca

Circle 183 on reader service card

Components

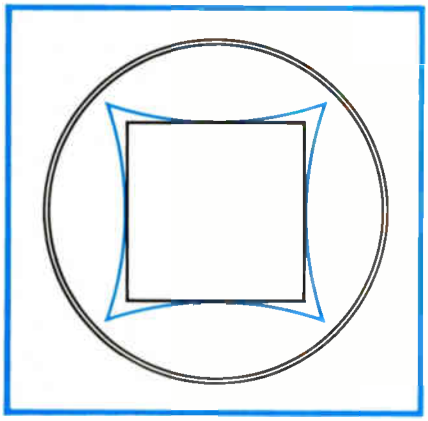
IC cuts CRT distortion

Pincushion eliminator comes in a 24-pin DIP, is priced starting at $75

Pincushion distortion has long plagued manufacturers of precision cathode-ray-tube displays. Existing solutions have been costly, cumbersome, or ineffective. Now, however, Intronics Inc. is offering a series of monolithic devices that are much less expensive as well as more accurate than anything that was available previously.

The C300 series will replace complicated and expensive diode breakpoint circuits or clumsy magnet-positioning schemes. "The C300 series will offer a continuous function, whereas diode breakpoint circuits have not," points out Herbert F. Wise, vice president for engineering. It will also replace an earlier, more expensive, C100 series of correction modules.

Hermetically sealed in 16-pin dual in-line packages, the C300 units will operate from 0° to 70°C. Moreover, military versions, the C400 series, come in a 24-pin DIP and work from −55° to +125°C.



Pincushion. When pincushion distortion occurs, the effect is to make squares appear as shown by the colored outline. This distortion appears in all flat-faced tubes because the distance from the center of deflection to the screen varies with deflection angle.

Members of each series differ in accuracy. At a deflection angle of 50°, the model C310 has a typical error of 2% of the full on-axis screen dimension. For the C311, the figure is 1%, and for the C312 it is 0.5%. For the C410 and C411, the figures are 1% and 0.5%, respectively.

Settling time to within 0.1% of full-screen dimension is typically 2 μs for all models, and typical 3-dB bandwidth for all models is 7 MHz. The maximum slew rate for all units is typically 200 V/μs.

Other typical specifications include an end-point temperature coefficient of 400 parts per million/°C for the C300 series and 350 ppm/°C for the C400. Offset temperature coefficient is 75 μV/°C for the C300 family and 50 μV/°C for the C400. The input voltage range for all models is ±5 V, and the no-load output voltage range is the same.

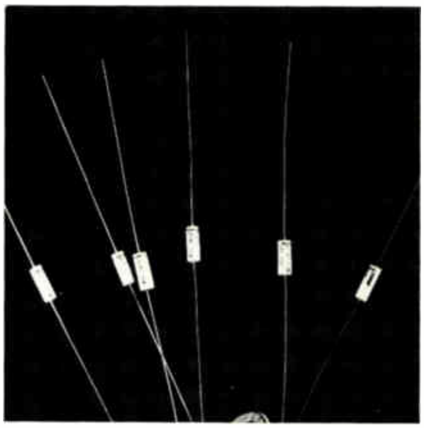
Peter de Hollan, sales engineer, expects the correction integrated circuits to find use in CRT displays involved in word processing, process control, and photo typesetting. "Color processing is a field that may use them, too," he says.

Prices for the C300 series, in lots of one to nine pieces, are $75 apiece for the C310, $99 for the C311, and $145 for the C312. For the same quantities, the C410 goes for $150 each and the C411 is priced at $225. Delivery for all units takes four to six weeks.

Intronics Inc., 57 Chapel St., Newton, Mass. 02158. Phone Peter de Hollan at (617) 332-7350 [341]

Small capacitors withstand 4½-lb pull on leads

Built to withstand a pull of greater than 4½ lb on its axial leads, the type 608 foil-wound capacitor is small enough to be used in high-density circuits and encapsulated military assemblies. The polyester-dielectric elements are available with 100-V ratings in values from 0.001 to 0.10 μF and with 50-V ratings from



0.012 to 2.0 μF. Tolerances range from ±1% to ±20%.

Prices vary according to capacitance, tolerance, and voltage rating. A 0.001-μF capacitor with ±20% tolerance and 100-V rating, for example, costs 63¢ in quantities of 1,000.

TRW Capacitors, 301 W. O St., Ogallala, Neb. 69153. Phone Al Tompkins at (308) 284-3611 [344]

8-character display is visible far and wide

Taskdata is an alphanumeric display unit consisting of eight five-by-seven-dot matrixes controlled by a microcomputer. The 1¾-in.-high, light-emitting-diode matrixes are visible from over 90 feet away at viewing angles over 110°. Therefore, they can be stacked or arranged vertically to form electronic bulletin boards.

The on-board microcomputer's memory can retain up to 32 charac-

ters, so four eight-character messages can be presented sequentially. Serial or parallel inputs in ASCII format are accepted by the display's RS-232 interface.

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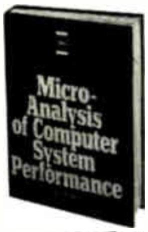

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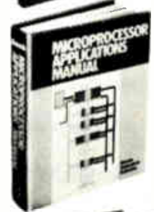

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Logic Electric, P. O. Box 5154, Kingwood, Texas 77339. Phone Curt Hamilton at (713) 446-1021 [345]

Tough automobile relay plays to the pits

Electromechanical relays of the type used in automotive electronics usually employ a design in which the contact arm is of a separate piece from the remainder of the relay, joined to it by a piece of copper braid and retained by flanges and a spring. Under the recurring influence of severe shocks like those induced by New York City potholes, the elements retaining the contact arm can be altered, thus producing failures that may be permanent or puzzlingly intermittent.

In addressing this kind of problem, Gulf and Western's Automotive operations developed a particularly rugged relay, one that can withstand vibrations and shocks in excess of 10 g. Available in both single-pole, single-throw and single-pole, double-throw versions mountable on printed-circuit boards, the relay employs a different design: its bobbin and the contact arm are cast as a single part.

Wrapped around the bobbin is a coil with a resistance of 130 Ω, so the unit consumes less power than competitive relays. It is rated for current switching of 30 A continuous at 12 V dc and 125°C, insulated to withstand 440 V ac, and operates from −40° to +125°C. At 25°C with a lamp load of 7 A and 2-s-on/2-s-off operating cycle, a single-pole, single-throw type has a lifetime of 750,000 operations.

In sample quantities of 1 to 10, units are priced at about $1.50, and sizeable discounts are available on large-volume orders. Deliveries from stock are scheduled to begin in mid-February.

Gulf and Western Manufacturing Co., Automotive Operations, 24114 Research Dr., Farmington Hills, Mich. 48024. Phone Ken Conrad at (313) 478-8140 [347]

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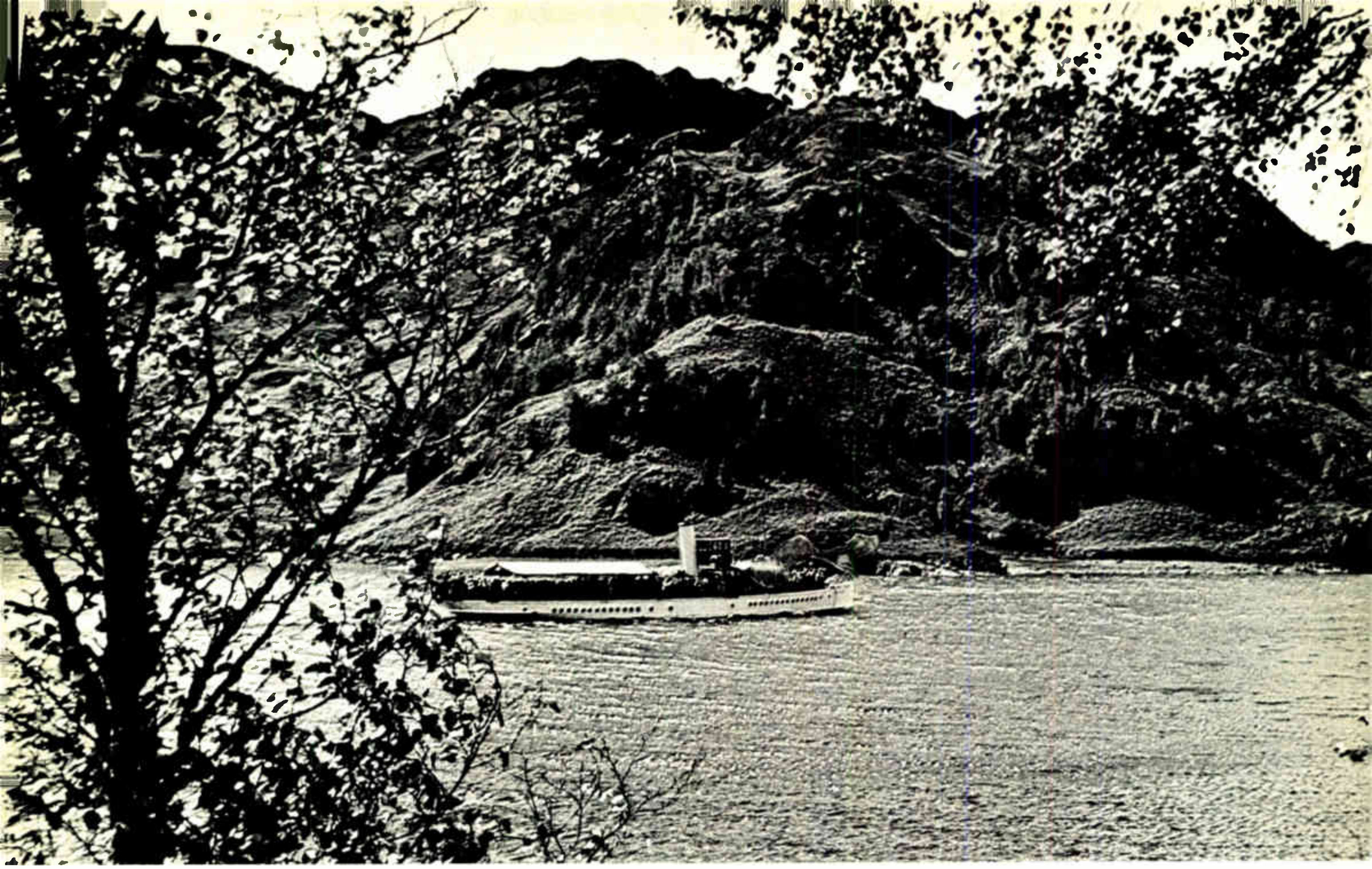

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But, for the full story, contact D. S. Logan, Industrial Development Officer, City of Glasgow District Council, Sun Life House, 116 West Regent Street, Glasgow G2 2RW. Telephone 041-332 9700.

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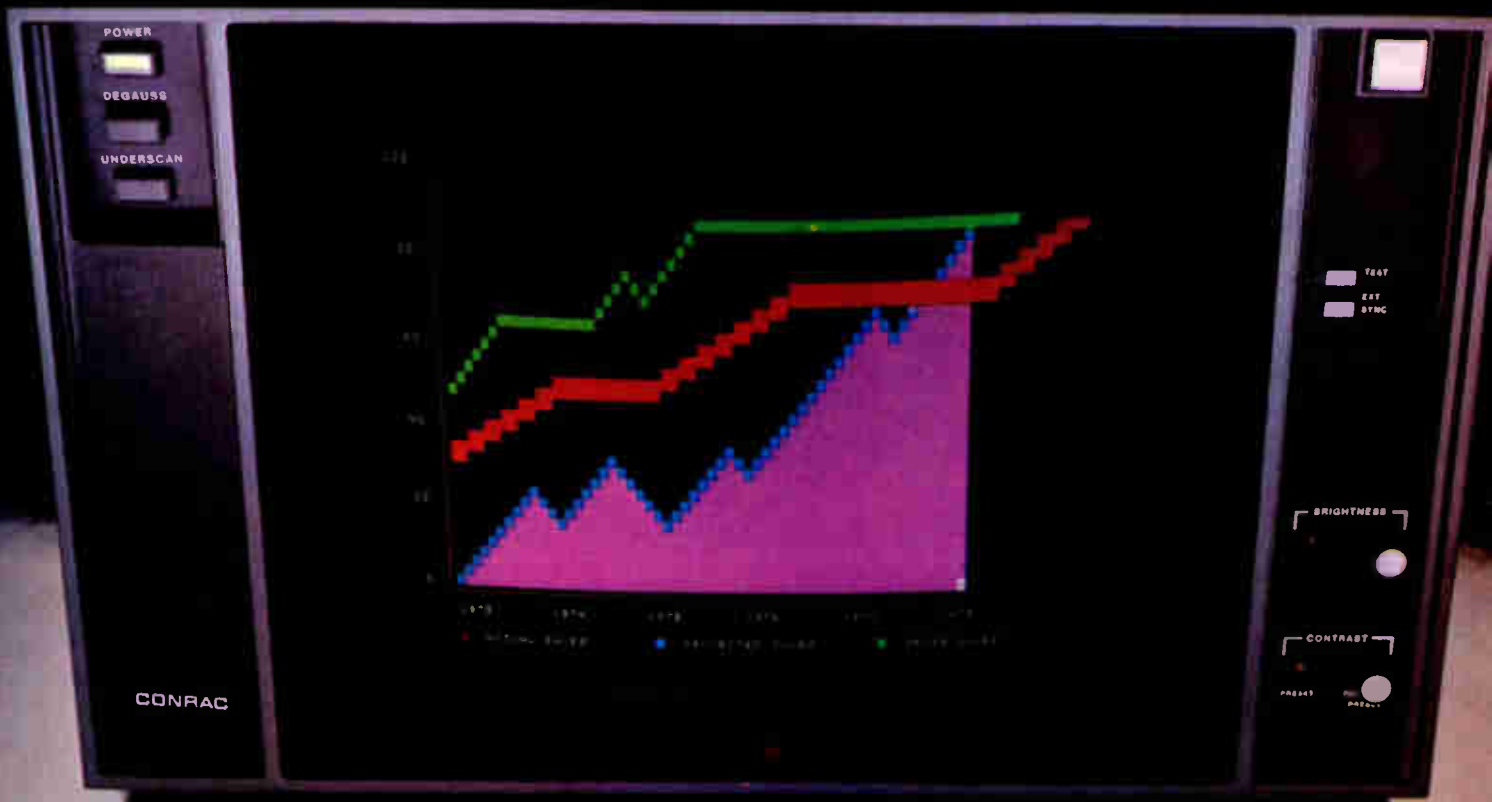

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Products newsletter

Fewer parts make analog function ICs cheaper and better

They won't change much on the outside, but Burr-Brown Research Corp.'s model 4213 multiplier-divider and its model 4291 divider are being redesigned on the inside to lower their parts counts, thereby cutting costs and raising reliability. **The multiplier-divider, which will de designated the MPY 100, will have one chip instead of two; the new model DIV 100 divider will have two chips instead of eight.** Both units will sell for about $10 each in large quantities, according to the Tucson, Ariz., company.

Cable lets programmer emulate PROMs

Instead of burning a number of programmable read-only memories in the course of developing their programs, users of E-H International Inc.'s model 4 programmer [*Electronics,* Sept. 14, 1978, p. 210] can make program changes on the model 4's internal 16,384-bit read-write memory and connect it directly to the system under development. Then, when the system is definitely working properly, a single PROM may be programmed. **What makes this possible is a $15 accessory for the model 4—the model PEC-24 emulation cable.** The 36-inch cable adds about 200 ns to the memory access time, but Jerry D. Rampelberg, program manager of the PROM programmer section, believes that it will not pose any problems in most cases. The cable is available from E-H's Sunnyvale, Calif., division.

40-W V-MOS FET sells for 50¢

Priced at 50¢ each in lots of 10,000, the second generation of V-groove power field-effect transistors from Siliconix Inc., Santa Clara, Calif., is going on the shelf this month. The first new device, designated the VN10KM, **is an 80-V, 0.5-A transistor with a source-to-drain on-state resistance of 6 Ω.** It is supplied in the TO-92 package, commonly used in solid-state entertainment equipment.

Signal conditioners make it easier to acquire data

A line of signal-conditioning products from Analog Devices Inc., Norwood, Mass., is designed to ease the problems of interfacing transducers with computers. Designed to work with strain gages, thermocouples, and resistance temperature detectors, the modules are intended to **eliminate problems caused by noise and high common-mode voltages and, where appropriate, to isolate, filter, and amplify signals and excite transducer bridges.** The line currently consists of amplifier-filters, both with and without transducer-excitation supplies (models 2B30 and 2B31) and a separate transducer-excitation supply (model 2B35). A voltage-to-current converter and an isolated V-I converter will be introduced soon.

Price cuts

The following price cuts have recently been announced:

- **The Du Pont Co., Wilmington, Del.,** has reduced prices on the products it makes for the manufacture of gas-discharge displays by about 22%. Reductions on 9530 and 9535 Nicyl air-fireable nickel compositions for display cathodes and on 9741 contrast dielectric have lowered the per-gram cost to 84¢ for the cathode materials and 39¢ for the dielectric.
- **Microm Systems Inc., Chatsworth, Calif.,** has cut the cost of its Micro800 series of data concentrators from 10% to 20%, depending upon the model. Prices now range from $1,150 for a two-channel unit to $4,600 for a 16-channel machine.

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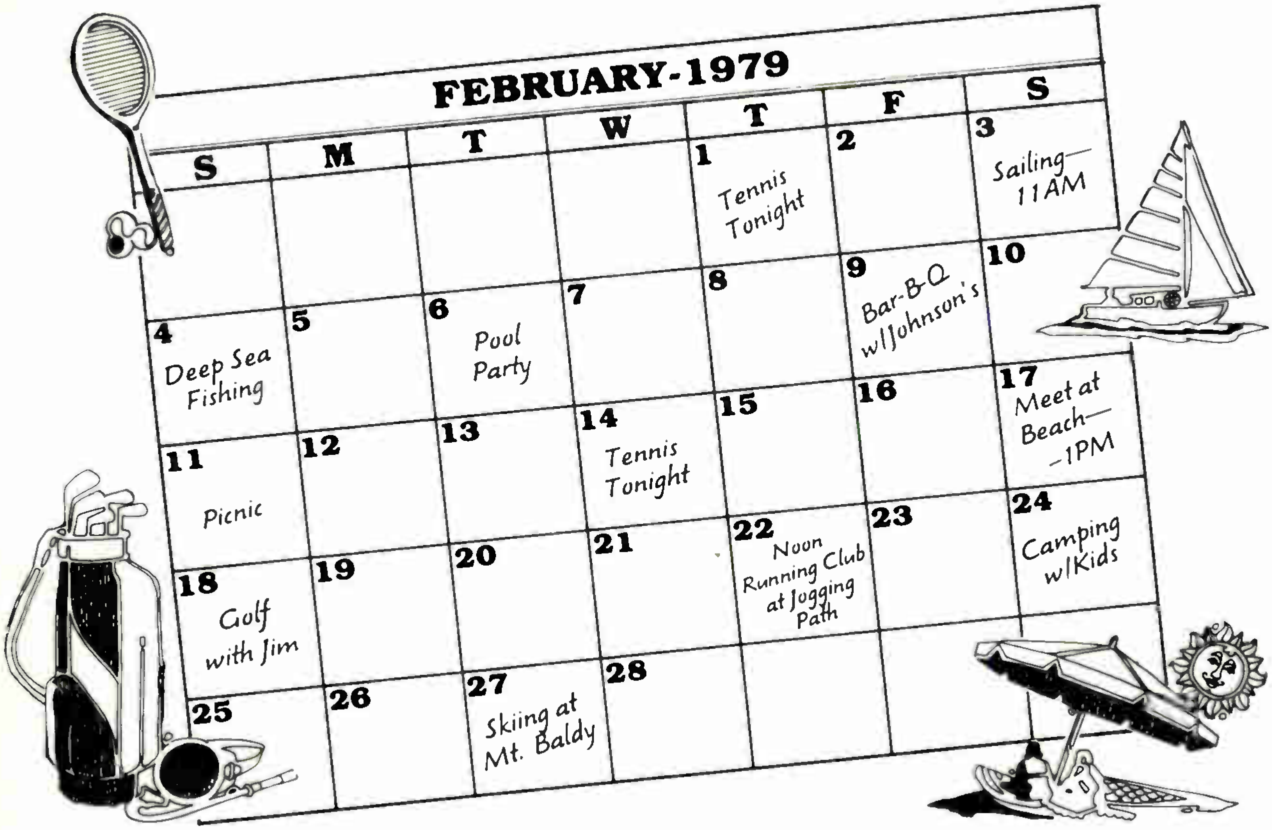

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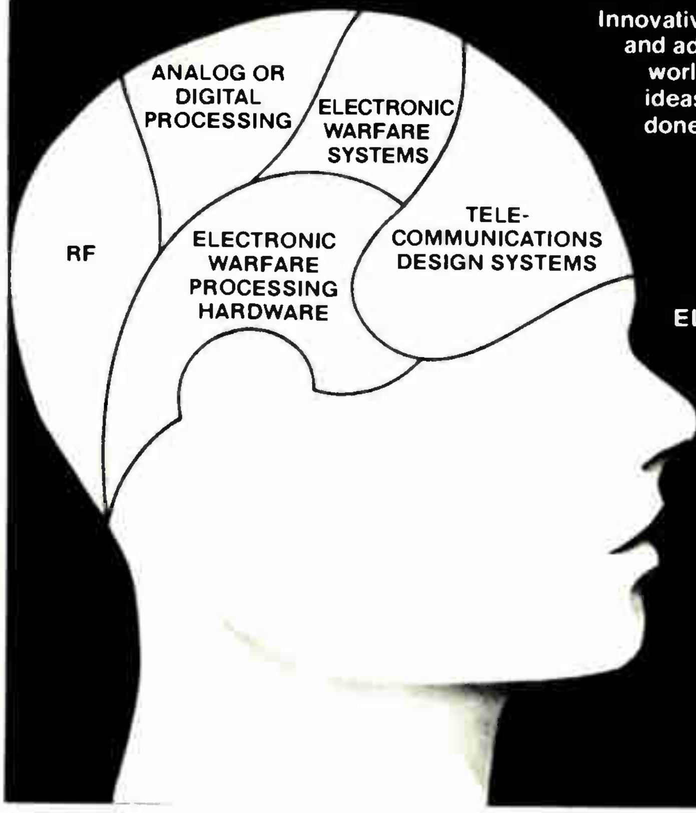

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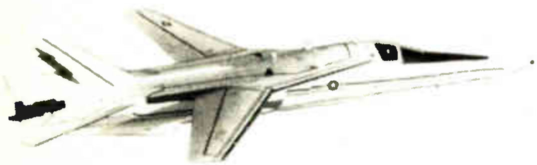

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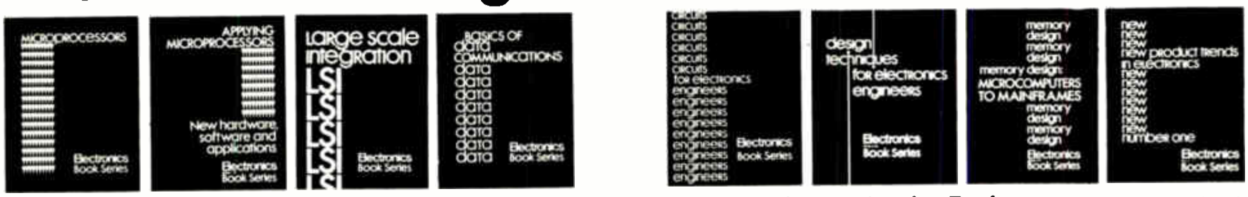

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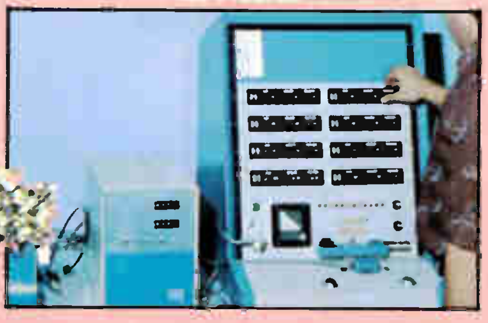

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