AUGUST 31, 1978

WESCON: A PREVIEW OF THE HOT SESSIONS AND PRODUCTS/156

New single-chip microcomputer has dual capability / 128

How plasma etching enhances LSI processing / 117

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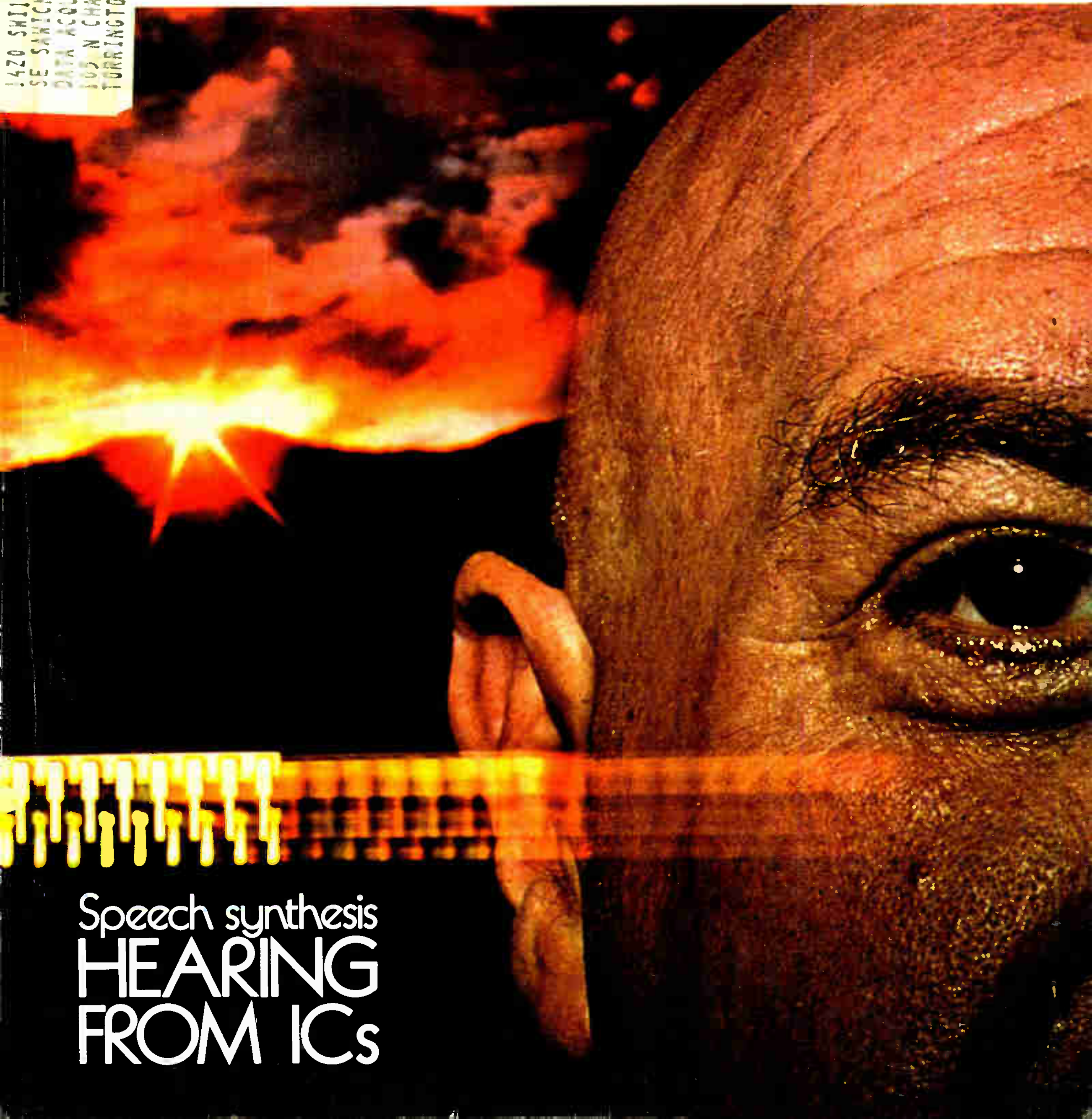

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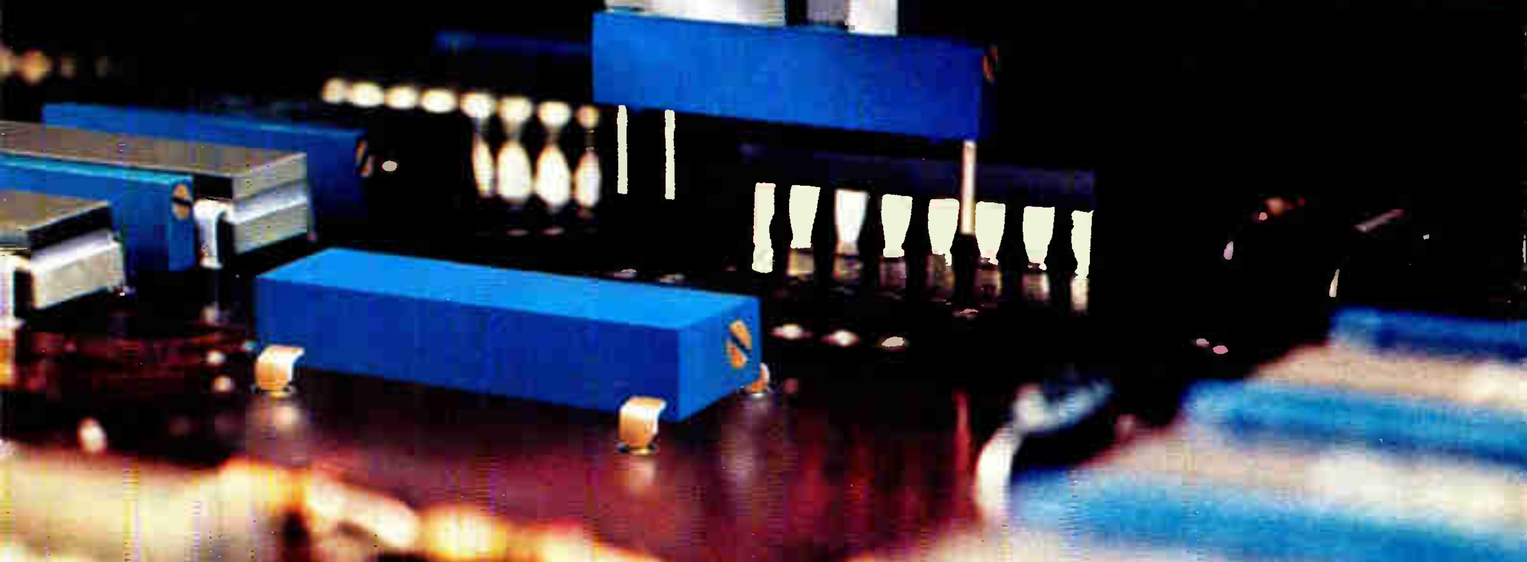

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098/45

Electronics
The International Magazine of Electronics Technology
Vol. 51, No. 18 • August 31, 1978

Highlights

The cover: Three chips 'speak,' 109

A synthesizer, a read-only memory, and a controller, all integrated circuits, are enough to synthesize human speech. By squeezing the equivalent of a multistage filter onto the synthesizer chip, the system can take advantage of linear predictive coding, a data compression technique.

Cover photographed by Don Carroll.

TI pushes minicomputers, 92

Few observers think of minicomputers as big business for Texas Instruments, and the semiconductor giant is out to change that. A product line designed for compatibility and a strongly supportive software effort are intended to turn the firm into a really beefy mini contender.

Z8 one-chipper boasts dual capability, 128

An input/output-intensive microcomputer or a memory-intensive microprocessor: the new Z8 can fill either role. Part 1 examines the architecture that makes this possible, and the immediately following Part 2 discusses the design's software.

Wescon/78 is near . . . 156

. . . and *Electronics* is ready. This overview of the microprocessor- and telecommunications-oriented program is followed on page 171 by a preview of significant new products to bow at the Los Angeles show. See also the Probing the News on the electronics associations in the West, page 85.

In the next issue . . .

All about codecs . . . new chips for the new data communications standards . . . measuring coherence.

Departments

Electronics

Publisher's letter

It was December 1976. In a meeting room at Texas Instruments Inc.'s Dallas headquarters, two men with widely divergent professional interests were getting together for the first time to design something that could have far-reaching effects—TI's speech synthesis system (see p. 109). The two were Larry Brantingham, a logic designer, and Richard Wiggins, a speech researcher.

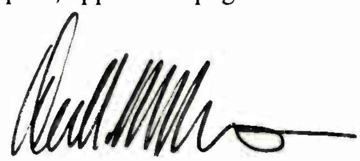
Brantingham is an electrical engineer; Wiggins, a mathematician. Brantingham has taken the more or less conventional EE's route: college, first job, laid off, then to TI as a hardware designer for the then calculator division, where he worked on I^2L designs. Wiggins had been at TI only a month when product engineer Paul Breedlove's idea—which turned out to be TI's Speak & Spell "talking" educational toy [*Electronics*, June 22, p. 30]—got him together with Brantingham. Whereas the engineer's bent was logic design, the mathematician was involved in analysis and simulation. After the initial get-together, the two had their speech synthesis project "idea-funded" until the middle of last year when TI decided to put big money into it. Wiggins and Brantingham then went their own ways—Brantingham to lay out the logic, Wiggins to work with his computer.

The fact that, as Brantingham says, the system is "good for any application from toys to vehicles to instrumentation" reflects the eclectic background of the designers and, indeed, the very way in which divergent technologies—and people—come together to spawn the many branches of electronics.

The history of American journalism is peppered with the accomplishments of farmboys from the Midwest who made their way to the big cities to make their names on metropolitan daily newspapers. Wesley Reed Iversen, *Electronics*' new Dallas bureau chief, is, at 30, an heir to that tradition.

Iversen grew up on a farm in southwest Iowa, went to college in Nebraska and at Iowa State, and then became business editor of the Sun newspapers in Omaha. He became a member of several award-winning investigative reporting teams. Then, in 1972, Iversen and some other Sun reporters started to look into Father Flanagan's Boys Town, Omaha, Neb. "It seems," says Iverson, "that the home routinely sent out two letters a year appealing for funds, whether it needed money or not. So the contributions would come rolling in, making Boys Town a cash-fat organization." The investigation brought some fiscal reforms to the institution and for Iversen and his fellow investigators a Pulitzer Prize—the most coveted award in journalism.

After becoming a senior editor at the Sun, Iversen moved to Dallas in December 1976 and the business news desk at the Times-Herald. This month he made his move into business-magazine journalism when he joined *Electronics* on Aug. 7. His first news story, about the Mostek-Inmos dispute, appears on page 42.



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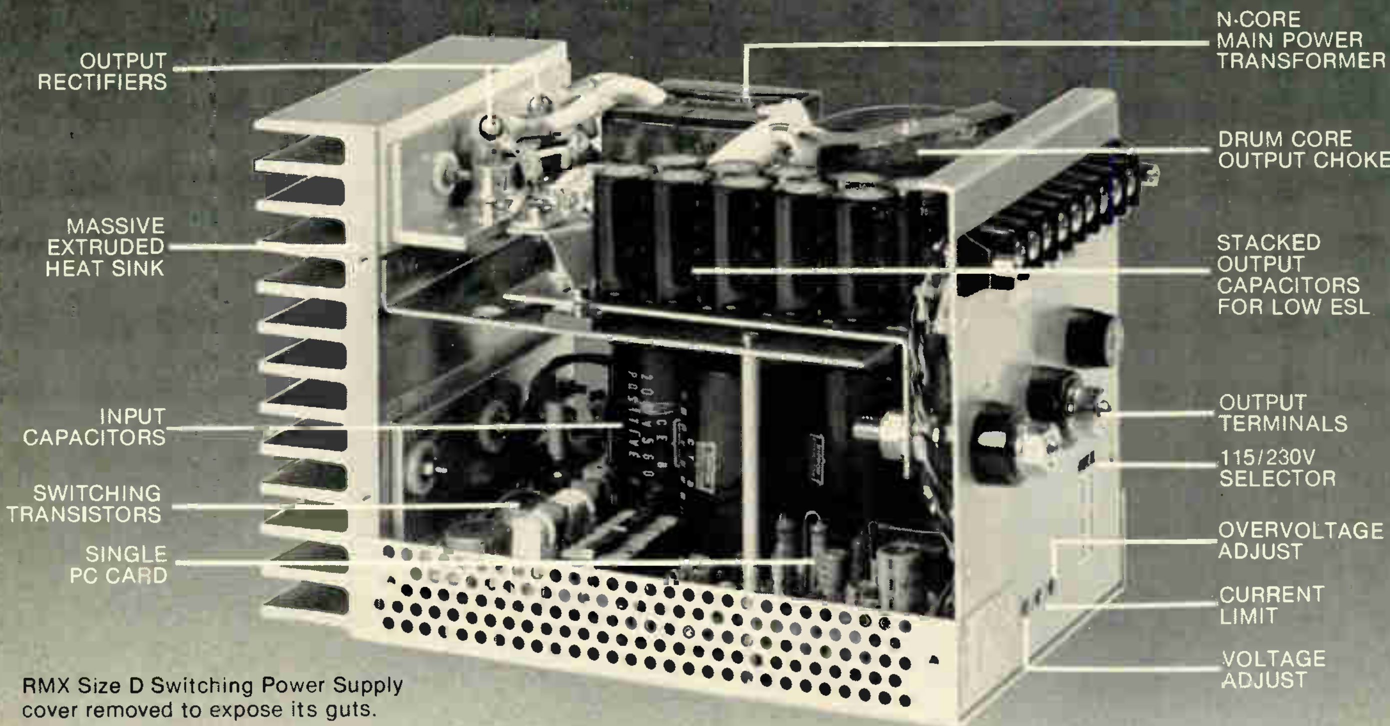

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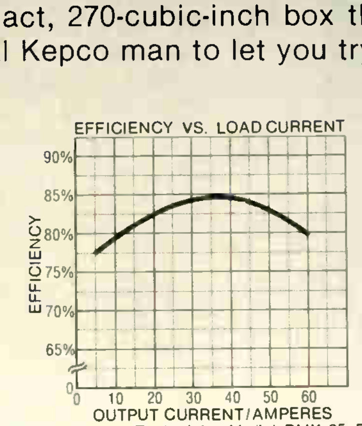
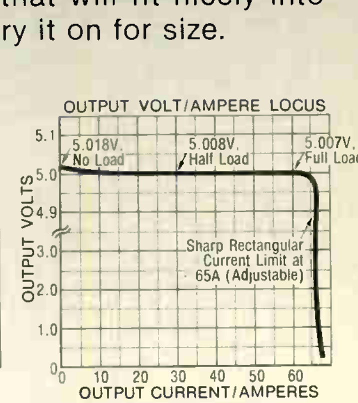
RMX 15–D	10.5–16.5	23A
RMX 24–D	16.8–26.4	16A
RMX 28–D	19.6–30.8	13.7A





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Readers' comments

Disputing signature analysis

To the Editor: The article "Logic-state and signature analysis combine for fast, easy testing" in your June 8 issue [p. 141] contains several points that in our view need correcting.

1. Building signature analysis into products or retrofitting them for signature analysis is not the problem it was originally thought to be. Engineers who have worked with signature analysis indicate that in most cases solutions are easily identified and cost-effectively implemented.

2. The 532 approach implies that a disadvantage of Hewlett-Packard's 5004A and similar instruments is that they require clock and gating signals. Obviously, the 532 also requires such synchronizing signals, and the captured data must be just as repeatable to detect errors using any signature technique.

3. The panel on page 143, "A look at two signature-analysis algorithms," strongly implies that Paratronics' software algorithm produces the same error-detecting capabilities as certain other approaches. The use of probability values and other figures could lead one to believe that the 532 detects bit-pattern errors and verifies good behavior to the same degree as a linear-feedback shift-register technique. In our view, this is just not so.

J. S. Grout
Phoenix Digital Corp.
Phoenix, Ariz.

■ **The author replies:** *1. I agree that signature analysis of the type Mr. Grout is concerned with can and should be integrated into a product during its early design phase. However, there are cases where signature analysis is not practical. That is why I stated in the introduction that "the product's design must include special hardware and software to support the test instrument: something that* may not *be feasible when board or program space is at a premium" (emphasis added).*

2. The difference between the model 532 and the 5004A (and similar instruments) is that the 532—like any other logic analyzer—uses clock and qualifier signals already present in the product: there is no need to design in the special control signals required by the 5004A. This allows the 532's signature analysis to be used with existing equipment.

Of course, captured data must be repeatable for the identifying signals to have any meaning. That's the whole point of signature analysis.

3. The actual algorithm in the 532 is considerably more complex than could be described in the panel, since the use of parallel channels makes the data-compression problem two-dimensional rather than one-dimensional. For example, one aspect of the algorithm incorporates the relative position of the data in the memory into the signature computation. Unfortunately, we cannot describe all the details of the algorithm, as it is proprietary.

Furthermore, I freely admit that bit patterns can be found that will defeat any algorithm, no matter how complex. In fact, all signature-analysis approaches are similar in one important respect that, interestingly, is never discussed: there can be an enormous number of bit patterns that will map to the same signature. However, the saving grace of signature analysis is that failures tend to be random and thus the probability that another bit pattern with the same signature will occur is extremely small.

Cause or effect?

To the Editor: I must take issue with your editorial of July 6 on a-m stereo [p. 24]. The main reasons for the current state of programming on a-m that you object to are the erosion of "good music" audiences by better-sounding fm and the lower quality of a-m receivers.

A-m stereo will allow manufacturers to produce receivers that will rival fm in quality of sound, and the existence of stereo will encourage a-m programmers to try many of the formats used successfully on fm. As chief engineer of an fm station and technical director of an a-m station that already programs good music and is eagerly awaiting a-m stereo, I think such a development will revitalize radio in general by improving sound quality and thereby increasing competition between a-m and fm.

James W. Davis
Durham, N. C.

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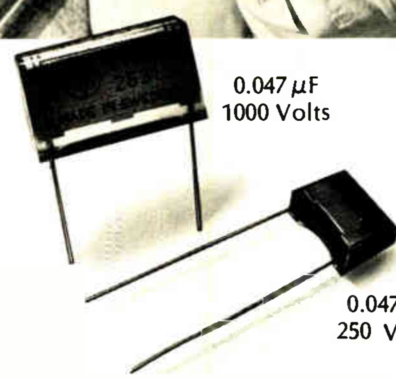

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News update

■ Westinghouse Electric Corp.'s Defense and Electronic Systems Center in Baltimore has delivered the first production radar for the U.S. Air Force F-16 multirole fighter to General Dynamics Corp. Delivery of the coherent, pulsed-doppler radar comes slightly more than two years after Westinghouse won a $36 million development contract [*Electronics*, July 8, 1976, p. 33].

The 300-pound radar is the lightest ever developed with its level of performance, according to a Westinghouse spokesman. "It has more operating modes than previous airborne fighter radars of its type:" an air-to-air down-look mode to distinguish aircraft from ground clutter found below the horizon, a dogfighter mode for close-in situations, and eight air-to-surface modes for weapon delivery and navigation.

Thus far, six full-scale developmental radar systems have been flown on F-16 aircraft. Another six are going through or have completed a program to increase reliability and qualification testing of their environmental and reliability parameters as well as their built-in test equipment. Westinghouse expects peak production of the system to reach about 20 to 40 per month.

■ The first commercial international digital facsimile service between the United States and Hong Kong, capable of transmitting high-resolution documents in 26 seconds, went into service this month. The facsimile machines used in the system employ the latest error-correcting technology and achieve a high degree of data compression by using relative-address coding techniques developed by Kokusai Denshin Denwa of Japan [*Electronics*, Feb. 17, 1977, p. 55].

Introduced jointly by RCA Global Communications Inc. of New York and Cable and Wireless of Hong Kong, the service operates at speeds ranging from 2,400 to 9,600 bits per second and costs $10 per 8½-by-11-inch page. It is an expansion of the first-ever high-speed, high-resolution digital facsimile service that started in Tokyo in March.

Bruce LeBoss

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Product Description	Special Features	Power Supply Voltages Req'd	Board & Doc. Part #	Board & Doc. Price	Assembled Product Part #	Assembled Product Price
CPU						
• Challenger II CPU BASIC-in-ROM 6502 based CPU with serial I/O 4K RAM machine code monitor	• Can use four 2716 EPROMS instead of BASIC or can be configured for disk	+ 5/ – 9	500	39.00	C2-0	298.00
• Challenger III CPU has 6502A, 6800 and Z80 micros. RS-232 serial port machine code monitor	• 1 megabyte memory manager. software programmable vectors	+ 5/ – 9	510	NA	C3-0	490.00
• 560Z multi-processing CPU expander runs PDP-8, Z80 and 8080 code	• Runs concurrently with another OSI CPU	+ 5/ – 9	560Z	125.00	NA	NA
RAM						
• 16K static RAM (Ultra low power)	• 215NS access time automatic power down standby mode	+ 5/ + 12/ – 9	520	35.00	CM-3	498.00
• 8K static RAM (low cost)	• Expandable to 16K	+ 5	—	—	CM-7	198.00
• 16K static RAM (low cost)	• Can be expanded to dual port operation	+ 5	525	35.00	CM-8	339.00
• 24K static RAM (high density)	• 20 address bits	+ 5	527	35.00	CM-9	NA
• 4K static RAM (2102 based)	• Can be populated for 4K by 12 bits	+ 5	420	35.00	CM-2	125.00
• 16K dynamic (ultra low cost)	• Uses 4027 RAMS	+ 5/ + 12/ – 9	530	NA	CM-4	249.00
• 32K dynamic	• 20 address bits	+ 5/ + 12/ – 9	530	NA	CM-5	698.00
• 48K dynamic (high density)	• 20 address bits	+ 5/ + 12/ – 9	530	NA	CM-6	990.00
EPROM Boards						
• 8K 6834 EPROM board	• 16 line parallel port and on board programmer	+ 5/ – 9	450	35.00	NA	NA
• 4K 1702A EPROM board	• 16 line parallel port	+ 5/ – 9	455	35.00	NA	NA
I/O Boards						
• Audio Cassette interface Kansas City standard 300 baud	• Expandable to CA-7C	+ 5/ – 9	430	35.00	CA-6C	99.00
• RS-232 port board	• Expandable to CA-7S	+ 5/ – 9	430	35.00	CA-6S	99.00
• Combination audio cassette two 8 bit DACs, one fast A/D and 8 channel input mux	• Also Features 8 parallel I/O lines	+ 5/ – 9	430	35.00	CA-7C	399.00
• Combination RS-232 two 8 bit DACs, one fast A/D and 8 channel input mux	• Also features 8 parallel I/O lines	+ 5/ – 9	430	35.00	CA-7S	399.00
• 32 by 32 character video display interface	• Keyboard input port	+ 5/ – 9	440	35.00	NA	NA
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• 16 port serial board RS-232 and/or high speed synchronous	• 75 to 19,200 baud and 250K and 500K bit rates individually strappable	+ 5/ – 9	550	35.00	CA-10X	200.00 to 900.00
• Parallel (Centronics) Line Printer Interface	• With cable	+ 5/ – 9	470	NA	CA-9	249.00
• 96 Line Remote Parallel Interface	• Interface "Front End" remotable via 16 pin ribbon cable	+ 5	—	—	CA-12	249.00
• Voice I/O board with Votrax* module	• Fully assembled voice output, experimental voice input	+ 5/ – 9	—	—	CA-14	525.00
DISKS						
• Single 8" floppy disk 250 Kbytes storage	• Complete with operating system software and disk BASIC	+ 5/ – 9	470	NA	CD-1P	790.00
• Dual 8" floppy disk, 500 Kbytes storage	• Complete with operating system software and disk BASIC	+ 5/ – 9	470	NA	CD-2P	1390.00
• 74 Million byte Winchester disk and interface	• Complete with OS-65U operating system	+ 5/ – 9	—	—	CD-74	6000.00
OTHER						
• 8 slot backplane board with connectors	• Can be daisy-chained to n-slots	—	580	39.00	NA	NA
• Prototyping board	• Handles over 40 16 pin IC's	—	495	29.00	—	—
• Card Extender	• With connectors	—	498	29.00	—	—

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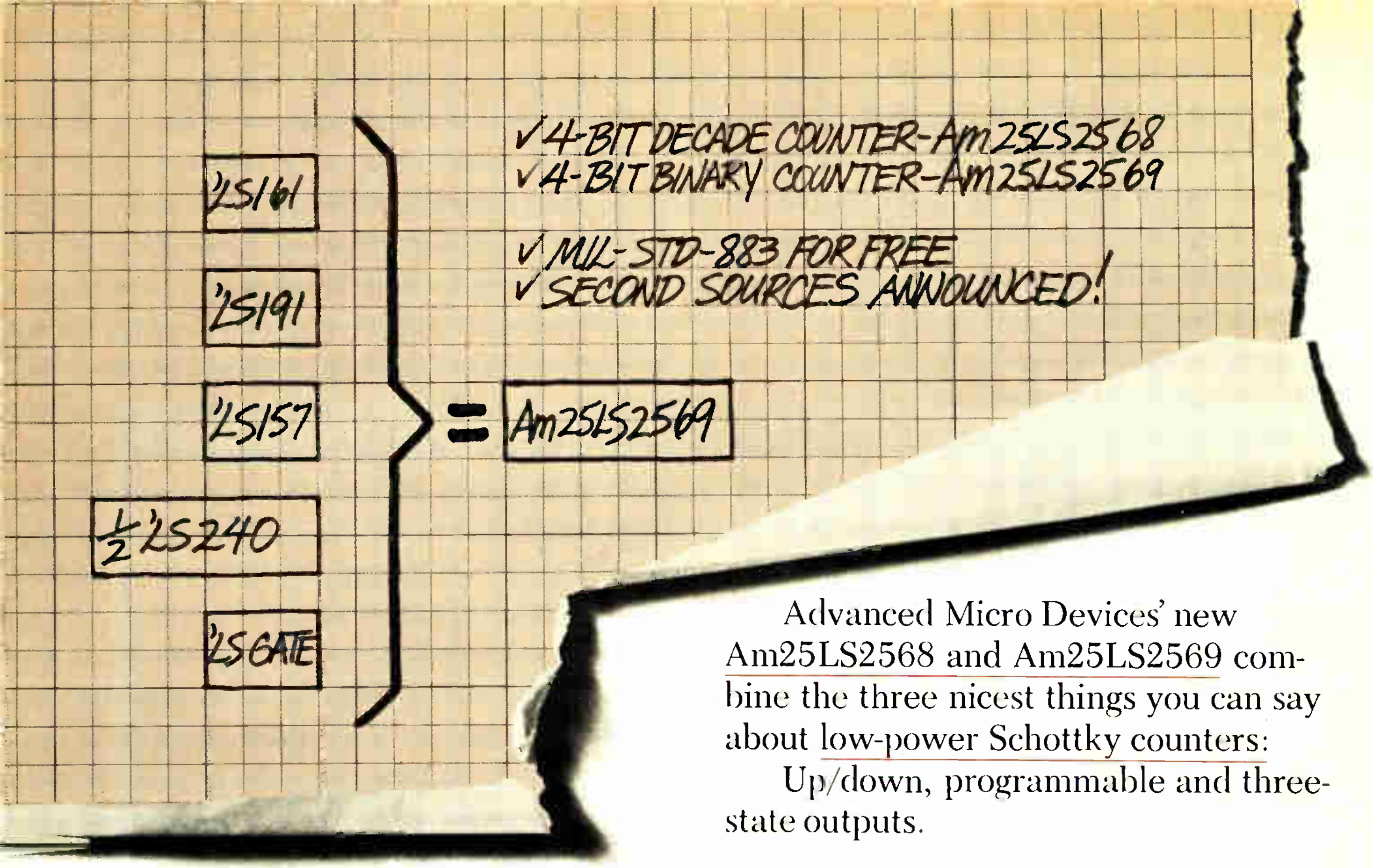

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Model 5345A: PLUG-IN VERSATILITY/optional front panel plug-in accessories expand measurement range to 18 GHz, make automatic narrow-pulse RF measurements to 4 GHz, or add a third 500 MHz channel. HIGH-SPEED LOGIC THROUGHOUT/for higher speed in systems use . . . over 50,000 four-digit readings per second in HP's 5391A Frequency and Time Data Acquisition System, for example.

The Super Counters offer many other features to help make your measurements much faster, simpler, more convenient and, of course, accurate. They're described in comprehensive data sheets that are yours for the asking. Prices: 5370A, $6500* including HP-IB. 5345A, $4400* plug-ins and HP-IB extra.

*Price domestic U.S.A.

Your broadest choice of counters from the industry's most experienced source.

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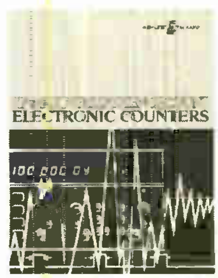

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People

McCook of Fluke Trendar asks designers to help out

The senior executive of a manufacturer of test systems for circuit boards promoting the idea of microprocessor-based boards testing themselves? Unusual, to say the least of it, for if the boards tested themselves, what would he be left to do?

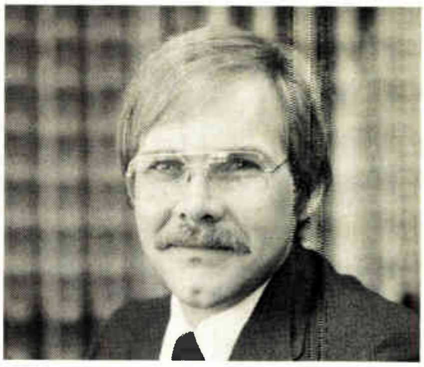
But Donald F. McCook, the new general manager for Fluke Trendar Corp., Mountain View, Calif., thinks it's a good idea.

"Designing a system to check itself is not a new concept," says the 32-year-old McCook. "But until the advent of microprocessors it was accomplished with considerably more hardware than was needed for the basic functional design alone. It's now easy for a designer to implement self-test routines in software, and we're seeing more and more of that technique being used in new instrumentation and systems."

But design engineers do not go far enough, McCook says. They typically use the self-test routines for pass-fail verification of a test plan governing checkout from board level to service in the field. "With a few design tricks, a self-test can act as a common link for all required tests—those for subassembly boards right through those used in field-service troubleshooting."

Complementary. McCook says that this concept would complement the usefulness of board testers, rather than render them unnecessary. "There are sections of the board best tested by the board tester without microprocessor interaction," he points out. "But a great many of the board's functions can be examined by exploiting the microprocessor's capabilities along with those of the test system.

"In a design using a microprocessor and 64-K random-access memory, for example, instead of having to program the tester with several thousand memory-test procedures, the tester could direct the microprocessor to a built-in test sequence. That would save both test program development time and money."



Tester. More built-in self tests offer big boost to board testers, says McCook.

McCook was president of Pacific Northwest Electronics Inc., a firm of sales representatives in Seattle, when Fluke Trendar's offer arrived. But he is familiar with his new employer. He began at the parent company, John Fluke Manufacturing Co. of Mountlake Terrace, Wash., in 1965 as a bench technician repairing meters. Eventually, he became marketing manager for Fluke's Precision Instruments division, before leaving in 1975.

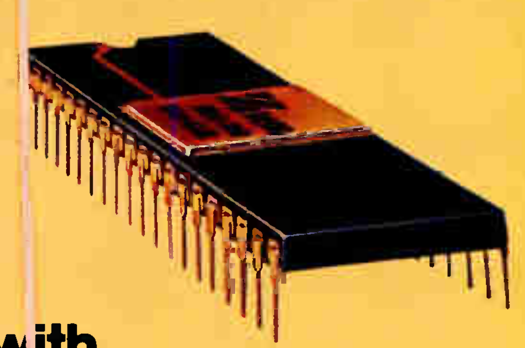
Distributors will survive by selling systems: Pond

The differences in style and background between Lauren L. Pond Jr., new executive vice president of Wyle Distribution Group, and most of his old-line counterparts at similar companies point up the changes sweeping the lively distribution business.

In the first place, the 41-year-old Pond is youthful for such a top job and represents a profit-oriented new management wave starting to replace the fast-talking, hard-selling industry pioneers. These veterans for the most part put "school of hard knocks" experience above education and worship ever-growing sales volume. In contrast, Pond, who is in effect the general manager of the $130 million company headquartered in El Segundo, Calif., holds an MBA in addition to his BSEE and knows that without "bottom-line results, larger sales by themself lead to big troubles."

In the second place, Pond says,

Now Zilog does double-duty.



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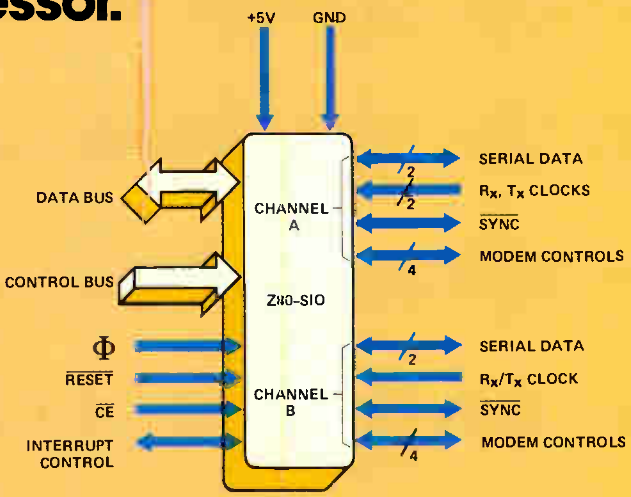

The Z80 Serial Input/Output: Here at last is a general-purpose device that can efficiently solve data communications problems for just about any microprocessor on the market.

The Z80-SIO is the world's first dual-channel, multi-protocol, serial communications interface circuit. It supports all serial data communications techniques with a single, N-channel (+5V) 40-pin device.

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Check out the Z80-SIO today. It's on your Zilog distributor's shelves right now in prototype or production quantities. Make double sure your next design delivers all the performance you're looking for.

CHANNELS:	Two independent, full-duplex with modem controls.					
DATA RATES:	0-550k bits/second (Z80-SIO); 0-880k bits/second (Z80A-SIO).					
OPERATING MODES:	Asynchronous; bisynchronous (with CRC generation and checking); SDLC/HDLC (with CRC generation and checking).					
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People

Overview. Pond says distributors will need more than parts to stay in business.

"the nature of the job we're doing is changing. We're being called on to sell mini- and microcomputer systems and peripherals. These are new high-technology products in the early part of their life cycle, just the opposite of components. A distributor's survival into the 1980s hinges on how well it can make money selling the systems."

Wyle has been a leader among distributors in moving strongly into what Pond says was "a marketing vacuum with semiconductor firms storming us to do something." The firm has been growing 30% a year and has all six of its locations in the western U.S. Pond, in fact, put together its initial systems marketing plan in 1974 after joining Wyle from Beckman Instruments, where he was director of marketing. Then, as now, he treated microprocessors as a long-haul proposition.

Rather than seeking instant results, Pond looks to growth with "heavy up-front investments in equipment, stock, and training costs for a better quality of sales person." He says that profits of Wyle's systems sales unit are "moving in the right direction, probably in the black two out of four years."

Whether Wyle succeeds in "getting as good in the systems business as we are in components" depends on one thing, Pond says. "People are the key, upgrading them to a broader, more educated type, bringing more of them in from suppliers." Better-prepared Wyle representatives will be more responsive to his customers, Pond says. ☐

"We eliminated LSI lead damage with AMP LIF-Lock connectors. And improved performance, too."

AMP LIF-Lock connectors are the economical way to prevent lead damage and excessive wear in frequently removed microprocessors, RAMs, PROMs and EAROMs. They also provide the greater reliability of high pressure contacts plus the extra economy of tin-plating.

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AMP LIF-Lock connectors can be used for both ceramic and plastic packages. And they are available in 24, 28, and 40 position configurations.

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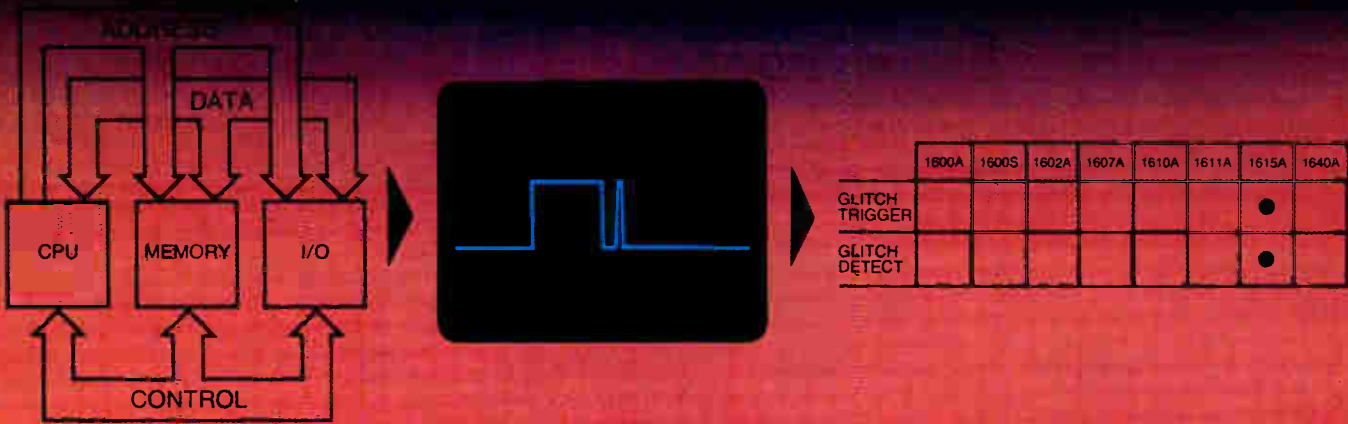
Here's the sensible way to select your next logic analyzer.



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We've developed a logical procedure to help you select the correct combination of features to solve your problems. Now, you can quickly make the transition from system to potential problems to features to a specific model. Here's how it works.

Suppose your system resembles the one shown in the above block diagram. A problem you're likely to encounter is glitches on a control line—leading to disruptive signals being generated within your system. That's where a logic analyzer comes in. But which one?

In this case, the two features you need which are central to glitch analysis are GLITCH DETECT and GLITCH TRIGGER. One look

at the Logic Analyzer Selection Chart and you'll find that both features are available in HP's 1615A Logic Analyzer. With a few simple keyboard entries you'll be able to trigger on the glitch and perform cross-bus analysis for rapid troubleshooting.

HP can show you a logical selection process for your design and troubleshooting problems. From system . . . to potential problems . . . to features . . . to a specific model.

Simply send for the **HP Logic Analyzer Selection Guide.** It will take you through the step-by-step sequence and help you discover which HP Logic Analyzer is best for your application. Or, for immediate assistance, give your local HP field engineer a call today.

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Circle 21 on reader service card

"Any bunch of hotshots can design a new microcomputer. It takes brains to improve an old one."

John Jones
Product Marketing Manager
Series/80 Microcomputer Systems

Series/80 Microcomputer Systems

"We're super aware that forcing a change in system architecture causes customers a lot of pain and agony. It costs a small fortune. And no amount of cross assemblers, translators or mode switches will make things easier.

If you want to hear real horror stories, ask the minicomputer guys. They've seen it.

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Like 'shadow ROM.' It lets ROM share the same memory address as RAM. And the ROM can be completely shut down and shut out when you don't need it.

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Don't get me wrong. The SBC 80/204—in fact, all the original SBC products are very good. But coming later lets us take customer reaction into account.

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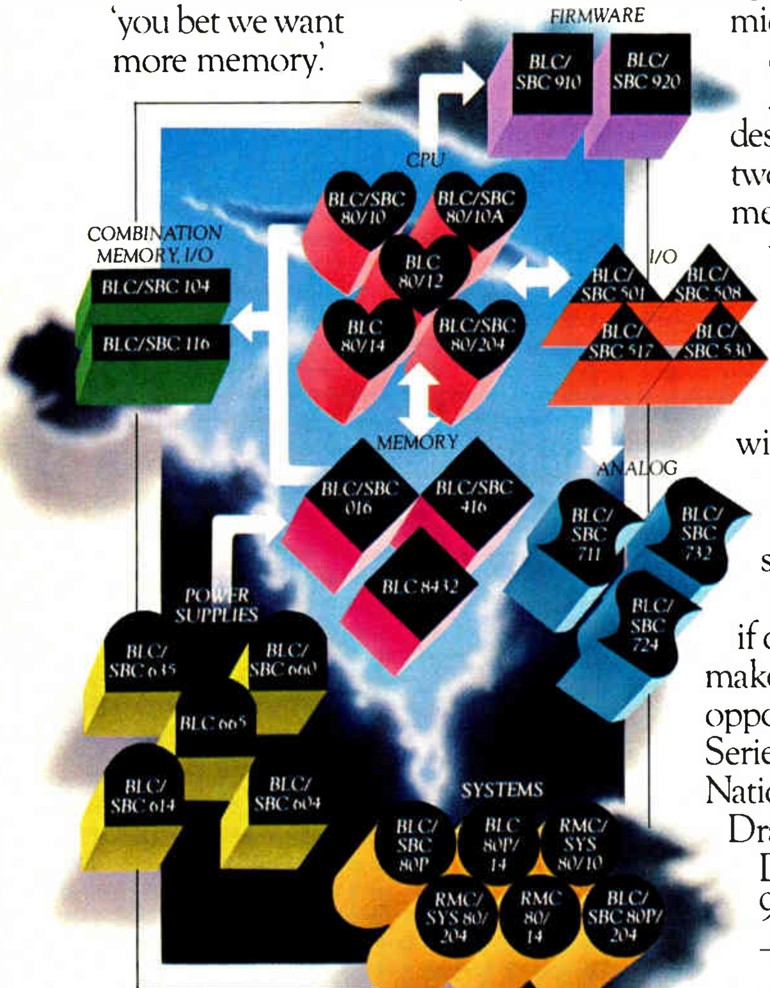

And that's what we gave them with the BLC 80/11, 80/12 and 80/14.

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We're dead serious about Series/80. Just last year we started with seven products. Now we're at 41 and still counting—every one designed from a top-down systems point of view.

For more on Series/80—or, if our market-driven philosophy makes sense and you'd like to talk job opportunities, write me: John Jones, Series/80 Product Marketing, National Semiconductor Corporation, Drawer 6, 2900 Semiconductor Drive, Santa Clara, California 95051. Or call 800-538-1866—800-672-1811 in California."

Computer Products Group
National Semiconductor Corporation

Editorial

Give the IEEE's members a break . . .

The Institute of Electrical and Electronics Engineers is a large and prestigious organization beset by problems of direction and execution. The debates that have heated its annual elections have gone a long way toward spurring some needed changes, and it is likely that the process will go on. But as the 1978 campaign for the presidency gets under way, the society's members are getting an earful of something rare in the usually sedate contests.

Both presidential candidates on the ballot—Irwin Feerst and Jerome J. Suran—have stooped into the ward-heeling politician's bag of tactics and emerged with fistfuls of names and accusations. One is called a "clone," the other is said to be encouraging "bigotry;" there are accusations of "treachery," "duplicity," and "harassment of members;" there is the charge of "advocating illegality."

Really, now. The contenders seem to be forgetting that many of their objectives are the same. They both oppose wage busting, age bias, and mandatory licensing. Their differences appear to revolve mostly around priorities and methods, important differences to be sure but certainly not extreme enough to force the candidates to call up the reserves of mud. Such tactics could have a serious side effect by widening the split among the IEEE's 180,000 members over the question of whether the society should put more of its muscle behind professional problems or behind matters of technology. What's more, such goings on also endanger one of the institute's greatest assets: its prestige.

The engineers in the society deserve a good, clear, sharp discussion of issues. Neither they nor the candidates are much served by a pointless name-calling contest.

. . . and how about one for the candidates?

Candidate Suran points out that as he goes about the country on his scheduled 20 election appearances, he is greeted typically by 20 or 25 members per appearance—although in one case about 100 turned out, but that was to see him receive an award, as well as discuss the election.

Such apathy possibly should be no surprise—after all, election turnouts in this country seem to have been declining steadily over the past few decades. Still, with the issues so immediate and personal, with the concerns so closely entwined with one's profession and lifestyle, it would seem that more engineers would show more concern about their society's stewardship.

It is a truism that one gets the kind of government one deserves. Apathy will serve only to drive out qualified candidates—if the members don't care, an aspiring contestant might reason, why should I? When a candidate for the presidency of the IEEE stands up before you and offers his ideas about your future and that of your society, you owe it to yourself to listen to him and ask some questions. Grumbling after the fact won't gain you much in the way of pension rights, job security, or professional standing.

Meetings

Wescon/78 Show and Convention, Electronic Conventions Inc. (El Segundo, Calif.), Los Angeles Convention Center, Sept. 12–14.

ECOC—**Fourth European Conference on Optical Communications,** IEEE Italian Section (for information, contact Istituto Internationale Comunicazioni, Genoa), Genoa, Italy, Sept. 12–15.

Conference on Information and Systems Theory Used in Digital Communications, IEEE German Section (for information contact VDE-Zentralstelle Tagungen, Frankfurt), Technical University, West Berlin, West Germany, Sept. 18–20.

ESSCIRC **78—Fourth European Solid State Circuits Conference,** IEEE Benelux Section (for information contact ESSCIRC 78, Delft University of Technology, Delft), Tropen Instituut, Amsterdam, the Netherlands, Sept. 18–21.

Sixth Computer-Aided Design and Computer-Aided Manufacturing Conference and Exhibition (CAD/CAM VI), Society of Manufacturing Engineers (Detroit), Hyatt House, Los Angeles, Sept. 19–21.

28th Annual Broadcast Symposium, IEEE, Washington Hotel, Washington, D. C., Sept. 21–22.

Eascon—Electronic and Aerospace Systems Convention, IEEE, Sheraton International Hotel, Arlington, Va., Sept. 24–27.

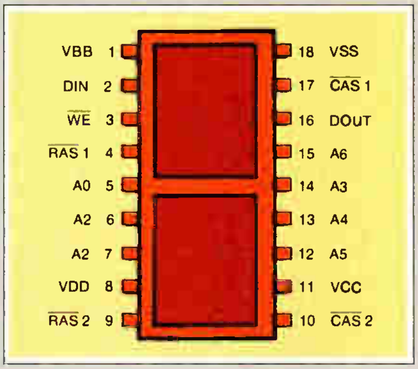
Distributed Data Processing, AIAA, Ramada Inn-Rosslyn, Washington, D. C., Sept. 25–26.

Convergence 78—International Conference on Automotive Electronics, Society of Automotive Engineers (Warrendale, Pa.), Hyatt Regency Hotel, Dearborn, Mich., Sept. 25–27.

ISHM **78,** International Society for Hybrid Microelectronics (Montgomery, Ala.), Radisson Hotel, Minneapolis, Sept. 25–27.

Mostek's 32K RAM. Double up for system density.

Mostek's 32K RAM doubles system density without increasing package count. By utilizing the industry standard 4116 in a dual device package configuration, Mostek now offers a 32K X 1 Random Access Memory module that's pin-compatible with 16-pin 4K, 16K and next-generation 64K dynamic RAMs.



The MK4332D is manufactured by mounting two MK4116 RAMs in leadless chip carriers onto a standard 18-pin DIP mother board. The assembled module has the same package dimensions as an 18-pin cerdip package, permitting the module to be used with standard automated handling and test equipment.

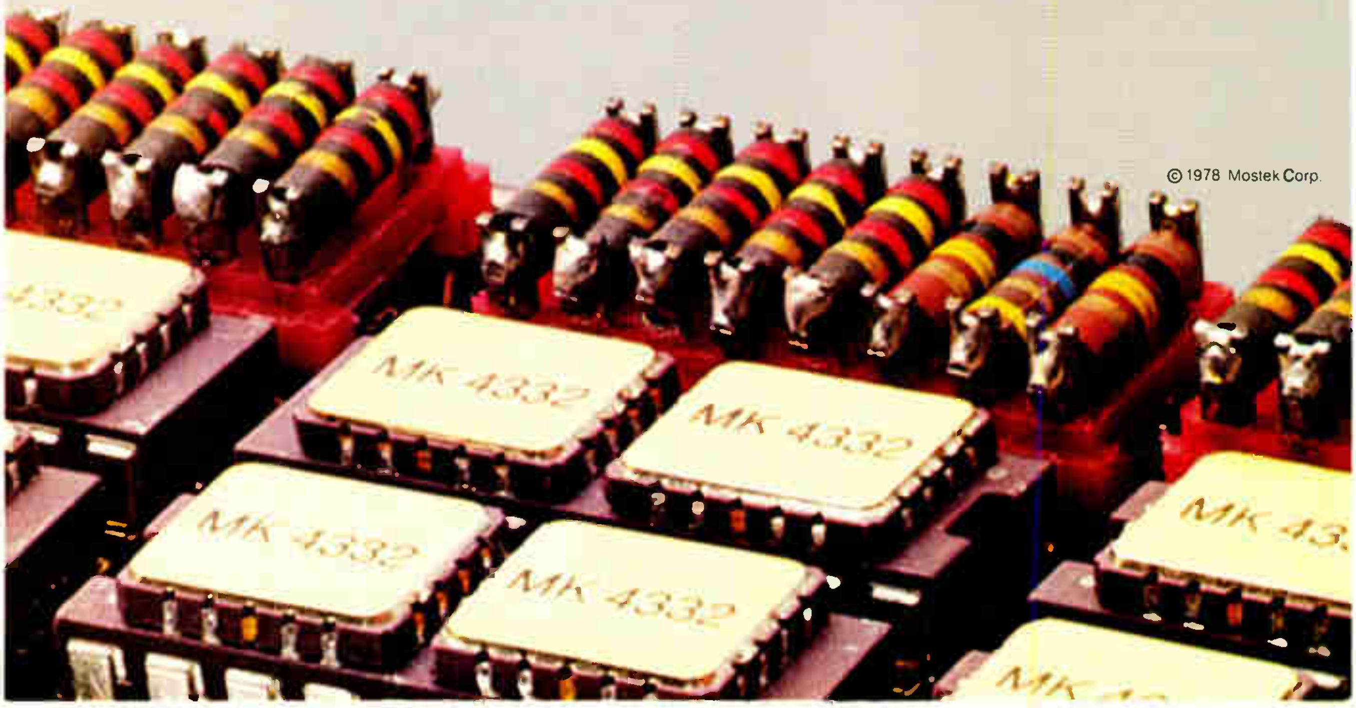
The two chips share common Address, Data In, Data Out, Write Enable, and Power pins. Separate $\overline{RAS}$ and $\overline{CAS}$ clocks for each MK4116 are provided for easy device selection and control.

The MK4332D-3 features an access time of 200ns with a cycle time of 375ns. And operating power is just 482 mW active and 40 mW standby (max). It requires a ±10% tolerance on all power supplies (+12V, ±5V).

The MK4332 offers 4116 performance and ease of use but allows greater memory density. Samples of the MK4332 are available now. Full production is scheduled for the 4th quarter, with optional pin configurations available.

For more information on Mostek's 32K RAM, contact Mostek, 1215 West Crosby Road, Carrollton, Texas 75006; Telephone 214/242-0444. In Europe, contact Mostek Brussels; Telephone (49) (0711) 701045.

MOSTEK.



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commodity in this unrealized potential."

Calvin Coolidge
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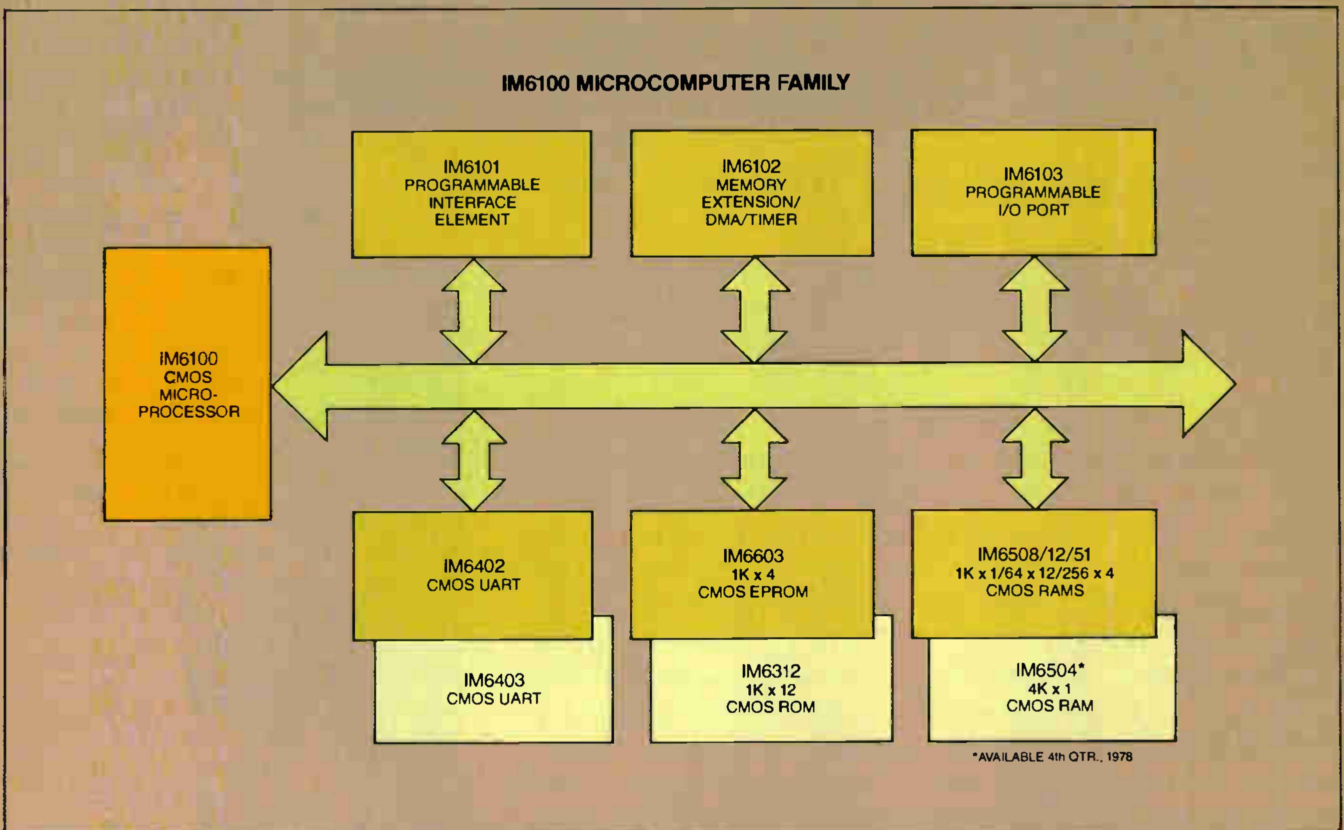

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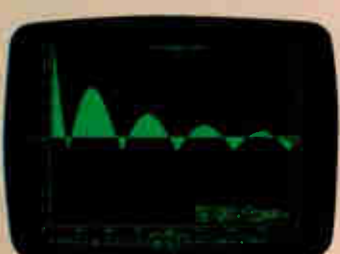

Waveform Analysis

Regression Analysis

Bar Chart


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National 2-chip codec set hits market . . .

The verdict is in as far as National Semiconductor's pulse-code-modulated coder-decoder chips are concerned. For the past two years, National has shipped samples of its monolithic single-channel two-chip set to some users and large quantities (1,000 to 10,000 a month) to two telephone manufacturers. Now the company is offering its TP 3000 complementary-MOS/bipolar field-effect-transistor series from stock for $10 per set in volume. Adhering to both μ- and A-law code standards, both versions have on-board 5-V references and feature a power-down capability. **National is claiming life expectancies of 20 to 40 years for the devices.** Moreover, look for National's second-generation ICs, such as single-chip codecs, by the second quarter of 1979.

. . . as Motorola prepares C-MOS part for market

Meanwhile, Motorola will soon be shipping samples of its MOS codec. **Its bid to the telecom market for switching jobs, central offices, and private automatic branch exchanges is a three-chip set:** codec and five-pole elliptic filter in C-MOS, and the subscriber loop interface circuit built with bipolar technology and a few outboard parts. Features include pin-switchable A- or μ-law encoding, full analog and digital loopback testing, and extremely low standby power: according to Motorola, the whole system will dissipate less than 10 mW when the phone is on the hook.

Canada to get phone-line video-text link

Look for Bell Canada to set up North America's first video-text information service using two-way transmission via existing phone lines. Scheduled for 1979, a pilot digital link will supply standard color home or business TV sets with news, entertainment, advertisements, and other special services at speeds up to 1,200 bits/second. Similar systems exist in England and France, but Bell Canada's pilot project, unlike the British Viewdata, is not a broadcast approach. **No regular television channel is needed, and the set functions only as a graphic terminal coupled to the phone lines.** As for the U. S., AT&T says that it plans no commercial test of such a system now.

RCA developing sapphire micros for Air Force

RCA Corp. has found yet another believer in its silicon-on-sapphire technology. The Air Force Materials Laboratory is funding RCA's Solid State Technology Center to develop a family of radiation-hardened complementary-MOS-on-sapphire devices based on a high-performance 8-bit slice microprocessor. **The family will be able to emulate existing microcomputers, such as 8080- and 2900-based systems,** and other widely used computers, among these the PDP-11 and AN/UYK-20, as well as custom designs. A spokesman at the Air Force lab at Wright-Patterson Air Force Base in Ohio says the service wants to be able to implement these computers with a minimum number of radiation-hardened chips and that C-MOS/SOS technology offers the needed speed and power performance.

British software for ATE gear in use at DEC

Chalk up a major software coup to the English software firm Warren Point Ltd.: its Atlas compiler for automatic test equipment will be used by Digital Equipment Corp. of Maynard, Mass. Called MICA (machine-independent compiler for Atlas), the package will be on equipment shown at Wescon (see p. 156). It is written in Coral high-level language; **thus routines in Atlas (the international ATE language) can be compiled readily to run on almost any computer-controlled automatic test system.** Further-

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Integrated device promises to perform optical-receiver functions

Experimental Bell Laboratories chip, fabricated on lithium niobate, should work as filter, coupler, switch, modulator

If electronic systems operating at microwave and millimeter-wave frequencies can be fabricated in minute pieces of silicon and gallium arsenide, then it seems likely something similar can be done at the much higher frequencies of light. Researchers looking into such integrated-optics devices have been dealing with this question for some years now. In one of the latest developments, it appears that Bell Laboratories may have an important part of the answer.

R. V. Schmidt and R. C. Alterness, researchers at Bell Labs' Holmdel, N. J., facility, have developed a device on a piece of lithium niobate that appears able to perform the four major functions found in a radio receiver—filtering, coupling, switching, and modulation. Unlike a radio, it operates at light wavelengths ranging in the red spectrum from 5,800 to 6,300 angstroms.

In integrated-optics devices, the four functions are usually performed separately. But Bell Labs, taking a basic coupled-line filter and carefully analyzing the mathematical equations governing its light-propagating characteristics, thinks it can obtain multiple functions.

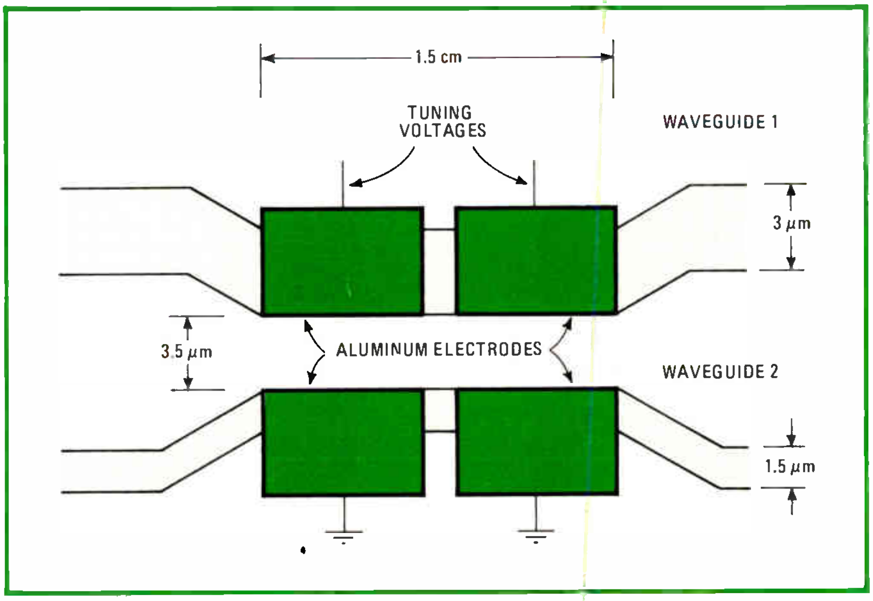
Tuning. "So far, we've only had time to work with tuning the filter, and we found we could tune it over several hundreds of angstroms," says Schmidt. "It had a tuning rate of 110 angstroms per volt and yielded a normalized 0.55 bandwidth per volt, decent enough figures for a bandpass filter in a fiber-optic system. Only about a ±2-v variable supply was needed for this.

"We'll be checking out more of the filtering, coupling, switching, and modulation characteristics over the next few months," he continues. "Right now, it all seems feasible. For example, the filter bandwidth can probably be lower than its present 200 angstroms. In fact, filters with bandwidths as narrow as 50 angstroms might be possible for lithium-niobate devices. If greater differences between the substrate and waveguide refractive indices are gotten, even narrower bandwidths might be obtainable."

In one 200-angstrom version of the filter, sidelobe levels of about 4% were achieved with a peak response of about 75%. No tuning voltage was applied, and examination of the frequency response was limited to the tunability of the dye laser used as a light generator.

Physically, the filter device is a very simple affair. It consists basically of a pair of closely coupled strip waveguides made of titanium diffused along one of the axes of the lithium niobate. This is a standard way to make such parts as an integrated optical filter or coupler. However, Schmidt and Alterness modified and adjusted the device on the basis of their mathematical analysis.

One titanium waveguide line is 1.5 micrometers wide, the other 3 μm. The interaction distance, or the length over which the coupled lines interact, is fixed at 1.5 centimeters. After these lines were deposited, the



Versatile. Bell Labs has added split electrodes to pair of closely coupled light waveguides. Voltages applied to the electrodes allow fine control over the device's optical properties.

Bell Labs researchers added a pair of split aluminum electrodes on top of the lines to afford fine control over the optical properties of the waveguides and the lithium-niobate substrate. The four receiver functions result from this structure.

Variable. For example, when light is introduced along waveguide 1 in the figure, the bandpass characteristic of the filter, caused by the coupling between the two guides, can be varied by varying the voltages on one or both sets of electrodes. The second function, coupling between line 1 and line 2, is basically set by the dimensions of the device but is finely adjustable by the electrode voltages.

The device acts as a switch or modulator when the electrode voltages are varied to alter the percentage of energy coupled from one line to another; adjusting the voltage at a particular rate means the energy in one of the lines is being modulated at that rate. It is also possible, by feeding energy at different wavelengths to both lines, to multiplex or demultiplex: energy from one line moves to the other. □

Microcomputers

Motorola system does well, quietly

Slipping almost unnoticed into the market for low-end stand-alone microcomputers for original-equipment manufacturers is a new entry, but one that carries an old-line name: Motorola Inc.'s Semiconductor Products Group. Despite the lack of fanfare, the Exor 68, referred to as a "multifunction display-oriented microcomputer system," seems to be doing very well. Motorola says it has sold 1,000 units since early this year and could have sold more except that first call on its components goes to other Motorola operations.

Also holding sales down is Motorola's reluctance to beat the drum for its new computer too loudly. Its top management is so touchy about selling systems competing with its semiconductor customers that company officials would not talk about the microcomputer until recently.

"We put together a pretty attractive little computer, all from standard parts, that we could make money with," says marketing manager L. C. Hevle. Buyers have flocked to Motorola's door, he says, mostly on the basis of word-of-mouth information.

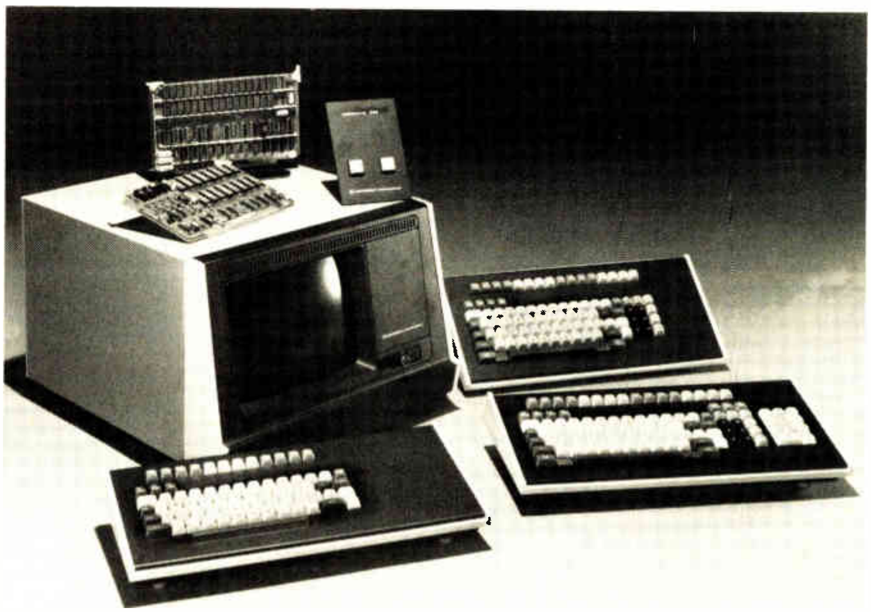
The machine is put together by Motorola's Microsystems operation in Phoenix from standard modules that go into various versions of the company's Exorciser microprocessor development system, and from Micromodule printed-circuit boards sold to OEM customers for expanding 6800 microprocessors. "It's part of our modular building-block concept, built entirely out of off-the-shelf components," explains Hevle.

A basic Exor 68, he says, includes a cathode-ray-tube terminal, keyboard, 6800-based central processing unit, and about 2 kilobytes of memory for display and 2 kilobytes for a minimum operating program. With a power supply, these parts are packaged in a card cage with room for eight plug-in boards for memory, input/output, or data communications. The system operates with high-level languages (including Basic, Fortran, and Cobol) and has such options as a disk operating system and printer.

Though these elements are hardly unique, the microcomputer's attraction is twofold: it is a complete system in a standard package, easing the customers' selection problems, and it is cheap. It sells for less than $4,000; in 100-unit quantities, at $1,700 to $1,800.

Motorola got into the small computers almost as an afterthought, admits Hevle, who was a founder of the Microsystems unit four years ago. The charter of this branch of the Integrated Circuits division is to furnish support equipment for users of Motorola semiconductor products.

But in the last year, Microsystems' management, largely computer people rather than semiconductor-oriented, came to recognize they had what it took to fill a void in the low-end OEM computer field. They could put together a flexible system, that was capable of expansion, microprogrammable, and priced below $5,000. Expanded facilities in Motorola's Mesa, Ariz., plant should



Off the shelf. Motorola assembles its Exor 68 microcomputer, shown with several keyboard possibilities, from modules being built for 6800 and other OEM customers.

boost production of the machine in several months, Hevle says.

A user. Confirming advantages of the Exor 68 from a user view is Thomas F. Fisher, chief engineer of Lordel Manufacturing Co., which employs the Motorola unit as clustered distributed-processing terminals in repair-service systems it builds for telephone-company central offices. "It's a very competent system and priced so that a small company can afford it," he says.

Fisher's company, located in Monrovia, Calif., is a division of Reliance Electric Co., Cleveland. In its $45,000 systems, Lordel beefs up the Exor 68 with up to 32 kilobytes of random-access memory and a mini-floppy disk, pushing the cost to almost $8,000 each. "But we talked to minicomputer companies, and for the minimum unit they started talking $10,000 and went up fast," Fisher says.

The question of Motorola's future in the small-computer business has yet to be answered. Motorola's reluctance to compete with customers could act as a brake on growth. In fact, an inquiry to Motorola corporate officials about plans for the Exor 68 program elicits the reply, "We're not going into the computer business." □

Two sources have new, smaller boards

Engineers who cannot use a prepackaged microcomputer system such as Motorola's can take one of two courses: buy preassembled and tested microcomputer boards that may have more power and hardware than they need; or spend lots of time and money custom-designing a microcomputer system.

Enter a new team of collaborators: Mostek Corp., perhaps the leader in semiconductor memory technology, and Pro-Log Corp., Monterey, Calif., which has been making a name for itself as a builder of microcomputer boards. At the Wescon show next month, they will be exhibiting a set of boards that offers a middle course: a family of physically the smallest microcomputer boards, yet one that can be expanded to meet the user's requirements. And it is available from two sources, hardly ever the case when board systems are announced.

The result could be much cheaper systems because the designer need not buy the bells and whistles that may be on the larger boards yet may not be needed, says Harold Webb, a systems product marketing engineer with Mostek in Carrollton, Texas. The boards in the STD (for standard) bus system measure 4½ by 6½ inches (current board families like the Intel SBC, measure 6¾ by 12 inches). Also, with only 56 signal lines, including 8 data and 16 address lines, each board needs only a single edge connector, as opposed to the pair that are often needed.

Besides the cost advantage of having only a single, smaller connector, Webb says that "the smaller modules making up the system will have less functions on board, allowing the designer to pick and choose from boards that are really needed—as for example, for a system that's all input/output or all memory."

At Wescon, Mostek will be unveiling a central processing unit board, three random-access memory cards, an erasable programmable read-only memory plus universal asynchronous receiver/transmitter board, a serial input/output board, and a parallel I/O board. Pro-Log will be showing similar equipment.

Mostek's CPU board, which is called the MDX CPU-1, contains the Z80 processor and will sell for $210 in quantities of 25. The three RAM boards come in sizes of 8, 16, and 32 kilobytes and are priced in 25-piece lots at $223, $275, and $506, respectively. Standard speed is 2.5 megahertz and, with the exception of the 8-K RAM card, all the boards will have a 4-MHz option.

An evaluation kit called the MDX-Proto will contain a CPU board, an 8-K RAM board, an erasable-PROM/UART board, plus a wire-wrap and extender card. It will cost $1,095 in single-unit quantities, without power supply.

For the computer to be successful, analog boards to interface with the real world are needed. Data Translation Inc., Natick, Mass., is at work to provide this missing link. It will be announcing eight different analog boards to mate with the STD bus "around the Wescon time frame," according to the firm's president, Fred Molinari.

The DT 2720 series will include two analog output boards, three analog input boards, and three expansion boards. One of each comes in an isolated version to reject 250 volts of noise—particularly important for industrial uses.

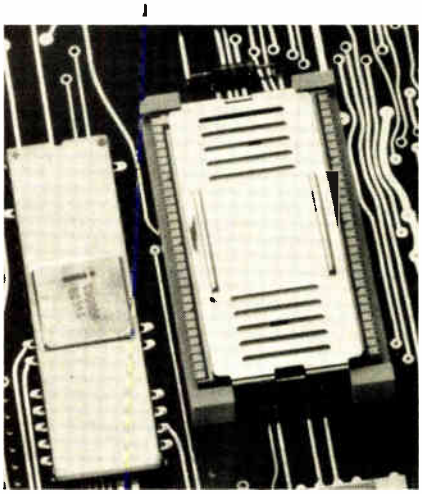
Molinari is convinced the new bus and boards will be a success. "A simple thing like size can stand in the way," he says. "And," he smiles, "there's that immediate cooperative second-source factor." □

Packaging & production

Intel, 3M develop new 64-pin carrier

Intel Corp. is going it alone again just as it did last year, when it struck out on its own with the pinouts for its 16-K read-only memory. This time, concerned with mounting large-scale-integrated microprocessor chips on printed-circuit boards, it

In place. Most visible on Intel's new 64-pin package is the shiny metal clip that holds chip carrier upside down in socket.



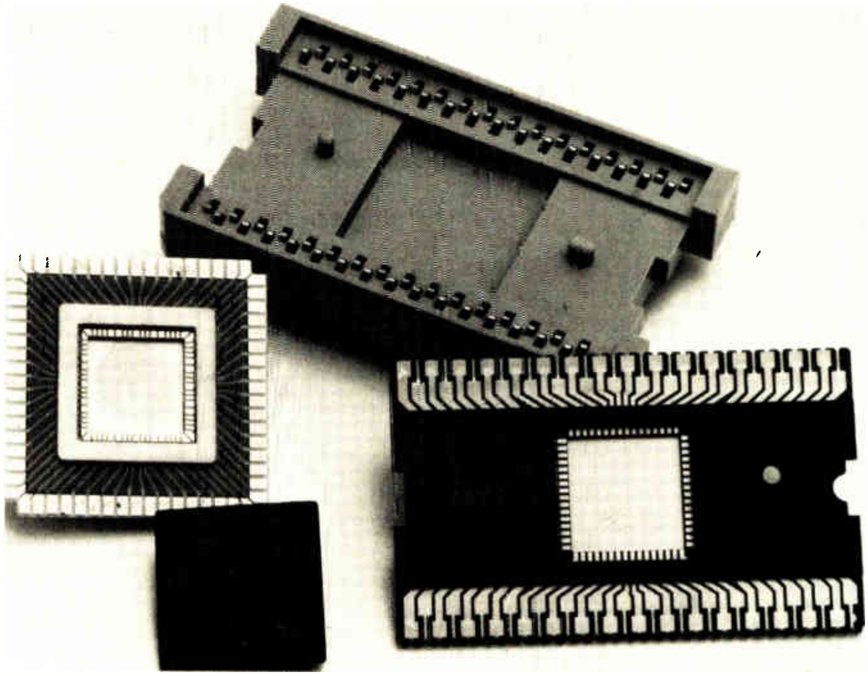
has come up with a 64-pin quad in-line package that is smaller and cheaper than a dual in-line package with the same number of pins.

With the new Quip package, as it is called, Intel and 3M Co., with whom it developed the unit, are going against the recommendations of the Joint Electron Device Engineering Council—in particular, those of Jedec's JC-11.3.1 committee on LSI package standards. The council meets this month to consider accepting these recommendations.

Five types. In March 1976, the committee proposed a family of five types of chip carriers, furnished with or without leads, and made of ceramic, epoxy glass, or plastic. The plan is for the carriers to have anywhere from 20 to 156 leads, and they all are to fit on a standard 50-mil-spaced printed-circuit-board footprint [*Electronics*, March 17, 1977, p. 81]. So far, the largest available chip carrier that is built to the Jedec specs is a four-sided design with 17 pins on a side. Besides having four more pins than the new Quip, this carrier is smaller, occupying only 1.4 square inches versus the Quip's 2.1 in.^{2} (The conventional 64-pin DIP measures 3.5 in.^{2})

But there are practical drawbacks to applying Jedec's 68-pin carrier that Intel and 3M are trying to overcome, according to William Lattin, engineering manager for Intel at its Aloha, Ore., design facility. For one thing, only two of the five Jedec types are available—leadless ceramic carriers made by 3M, Kyocera, and others. Of even more concern to Intel is that these carriers cannot now be readily mounted on a pc board. This is because they require either a separate socket or a set of substrate clips, and these are still not available. In fact, they are only in the developmental stage at AMP Inc. and in the prototype stage at Berg Electronics Inc.

The new Quip, on the other hand, will be in production at 3M in October and will solve any mounting problem because it will come with its own socket. Lattin says that Intel will be introducing a device using the new design this year, and 3M, which says a large unnamed systems house also will be employing the Quip, will try to sell it to other chipmakers, too. At an estimated 14.5¢ for package and socket, it is competitively priced with 64-pin DIPs which typically cost about 16.8¢ for package and socket.



Components. Square, 68-pin Jedec chip carrier (left) contrasts with Intel's 64-pin design. Intel's rectangular chip carrier, its lid (black square) covering the chip cavity, is meant to flip over into the socket (top). Device contacts at socket's sides remain exposed for test.

Quip has three main parts—a ceramic substrate with a chip-holding cavity, a keyed socket with four rows of pins in which the substrate is mounted cavity downward, and a metal clip that holds the substrate and socket together. (There is also a lid that fits over the cavity.)

"In our Quip we have made the packaged chip easier to test than with the Jedec design, because we run out extra contacts across the top of the substrate so it can be probed from the top, while it is still plugged into the circuit board," says Lattin. "This has not been available with any other IC package."

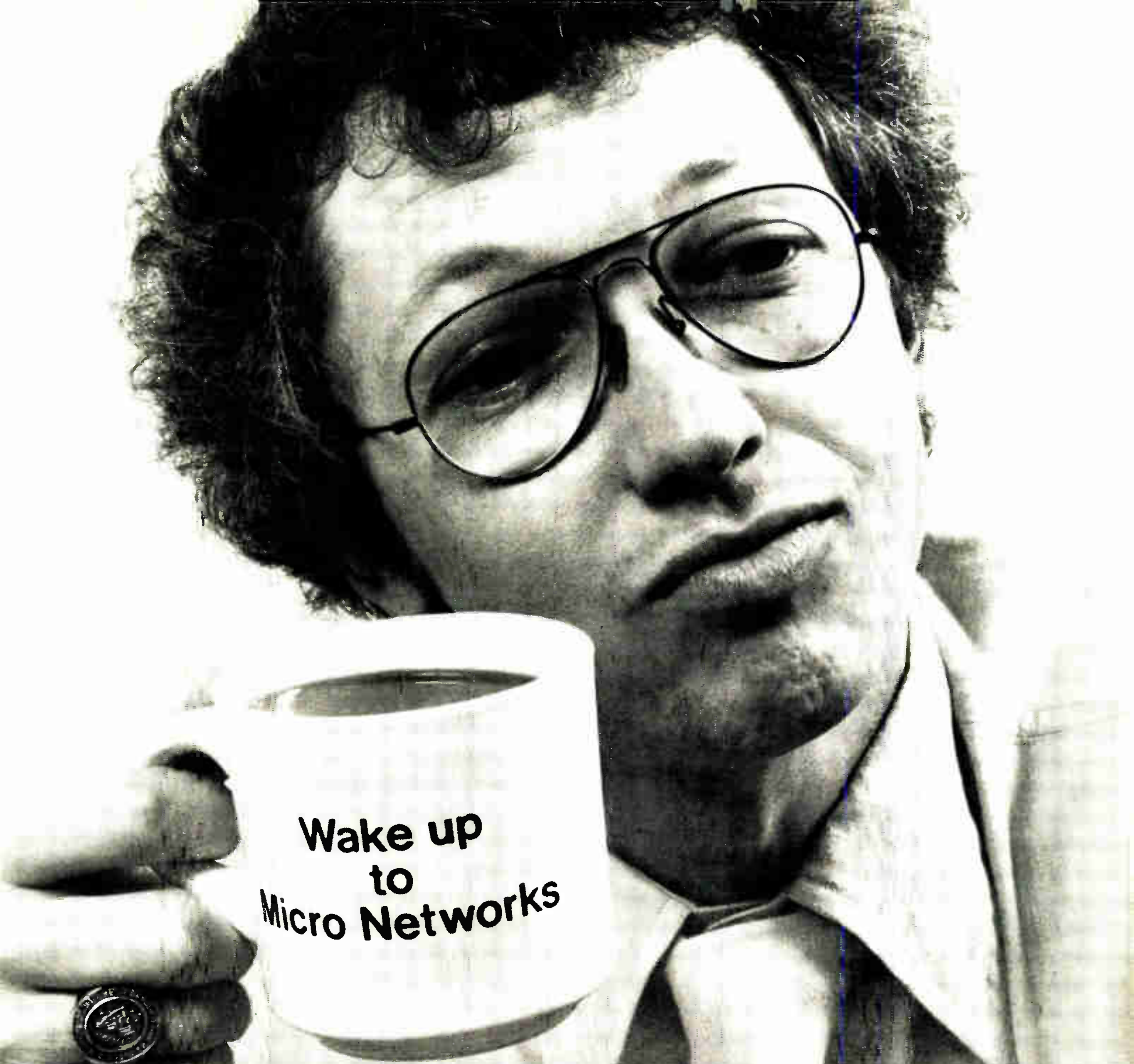
In addition, the new package is built so its chip-holding substrate can easily be removed and replaced by a new substrate for diagnostic purposes. And since this package is aimed directly at microprocessor applications, an emulator cable can be plugged into the socket in place of the substrate. Again, this is done while the socket remains soldered to the board.

Other features of the new Quip include a low 35°C-per-watt thermal resistance that allows it to dissipate more than 2 W in still air and not exceed the 170°C maximum permitted junction temperature within the chip. Its cavity is 0.4 in. on a side; the Jedec design however, can have a cavity measuring 0.6 in. on a side, according to Dan Amey of Sperry Univac, Blue Bell, Pa., who heads the Jedec committee. Lead resistance and capacitance are 0.3 ohm and 3 picofarads respectively, comparable to the Jedec specs. □

Companies

Surprised Mostek seeks Inmos halt

At about the same time this summer that Mostek Corp., Carrollton, Texas, was launching a new employee-recruiting campaign with tee shirts, posters, billboards, and even a brightly colored hot-air balloon,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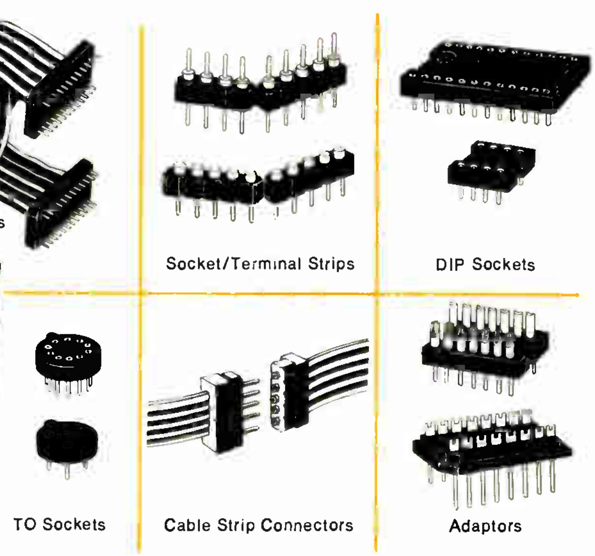

there was apparently some recruiting of another, quieter kind going on within the Mostek ranks.

"We were taken by surprise," said a stern-faced L. J. Sevin, Mostek board chairman and chief executive officer, following the successive resignations of five key Mostek employees to join Inmos Ltd., the newly formed British-backed semiconductor firm [*Electronics*, Aug. 3, p. 42].

The company wasted little time in responding, however. After three of the five took their leave on Aug. 9, Mostek was in Federal court next day filing a lawsuit charging Inmos, the five former employees, and Britain's National Enterprise Board with conspiring to misappropriate Mostek trade secrets. Richard L. Petritz, a one-time Mostek president who is a cofounder and president of the English firm, was also named a defendant.

Too familiar. According to the suit filed in U. S. District Court in Dallas, former Mostek employees Paul R. Schroeder, Ward Parkinson, Dennis Wilson, Dave Wooten, and Doug Pittman are intimately familiar with proprietary Mostek design, processing, and business information on, among other things, the company's 64-K random-access memory (planned for introduction next year) and a single-chip microcomputer on which Schroeder had been working. When formation of Inmos was anounced in July with more than $40 million in start-up funds, plans to develop and produce a 64-K RAM, as well as a microcomputer, were specifically mentioned.

At Mostek, Sevin says efforts are under way to "cover the gaps" in the memory group left by the departures. Introduction of the company's 64-K RAM, which had been planned as "a New Year's present for the world," may be delayed slightly, but "only a few weeks" at the most, he says. Some projects involving new Mostek static RAM products will be delayed several months.

Sevin charges: "There are strong indications that [the formation of Inmos] is a move to rip off Mostek, expropriate its technology, and deliver it over to the British government." Inmos plans to "make exactly the same products we're planning to make next year," he continues. "What else can you conclude? They took key people right out of the main product area of our company."

Tough talk. Mostek's L. J. Sevin says Inmos is out to rip off his technology and deliver it to the British government.

The unexpected resignation on June 9 of Schroeder, who was the first of the five employees to go, was the "first inkling we had that [the Inmos venture] would involve any of our people," Sevin says. Schroeder, considered a leading expert in memory design, had been with Mostek since 1974 and headed up the memory design group until April 10.

Secrets. The Texas firm also alleges that Pittman, on the day before he resigned, "approached the chief process-development engineer and elicited from him all of the details relating to Mostek's highly proprietary and confidential photomasking process." According to industry observers, a weakness in the Inmos plan has been a lack of top-notch personnel with processing background or expertise in electron-beam-system technology.

Mostek is seeking a permanent injunction, prohibiting the use or dissemination of proprietary Mostek information or the acceptance of such information by Inmos or the NEB. The company also wants to permanently enjoin Inmos from hiring away any present Mostek employees and is also asking for treble damages in an unspecified amount under Federal antitrust laws.

For their part, Inmos officials in Dallas remained mum shortly after the suit was filed. The company has said it hopes to have a U. S. pilot plant in operation within six months to a year and volume production under way in a plant in the United Kingdom by 1981. "We just don't want to make any comments at this stage on this whole matter," Schroeder says. "We feel as if anything we say at this stage would exacerbate the situation."

Likewise in London, a British official would say only that "the NEB can confirm that it would not be its policy to countenance the improper use by Inmos of trade secrets and proprietary information." □

Government

New law to ease customs hassles

Legislation creating a new customs law, expected to pass Congress soon and go into effect early next year, promises to make life easier for electronics companies importing equipment and material or bringing in their products from offshore assembly plants. Besides simplifying paperwork, H. R. 8149, the Customs Procedural Reform Act, would remove the threat of heavy penalties and expensive litigation for companies disputing the amount of duty they owe the U. S. Customs Service, especially on value-added offshore products.

Procedure. Under the present law, passed in 1930, the Customs Service feels compelled to assess fines equaling the full domestic retail value of shipments in dispute, even though the real issue is the duty owed, which is much less. This means, for example, that a disagreement over duty on an item worth only $100 on an invoice could lead to fines equaling the domestic retail value of the

Another problem

Wait before relaxing in relief about the softer customs bill, lawyers John Rode and Leonard Bernstein told an American Electronics Association briefing this month. A proposed criminal reform act now in Congress could have a chilling effect on any gains, said the pair from Rode and Qualey, a New York law firm.

Whereas current criminal law carries a maximum penalty of $5,000 and/or five years in jail for falsely entering goods, the proposed section 1411 on smuggling provides steeper penalties. For example, if the object's value or duty exceeds $500, a violator would be subject to a $100,000 fine and/or five years in prison, and an organization could get a $500,000 fine.

entire shipment, even if it is worth $100,000, explains an executive at Advanced Micro Devices Inc., Sunnyvale, Calif. And the penalty could be applied to all shipments where such disagreement arises.

If Customs suspects a discrepancy, its agents investigate a company's books to derive a "constructed value" of the shipments questioned and then levy a duty on that value. If a "significant difference" exists between the two duty figures, the service assesses a fine.

But, as the AMD executive relates, companies seldom know how the Customs Service derives "constructed value" and "significant difference." By being cooperative and pleading simple error, companies often get the fine knocked down to only a multiple of the lost duty. Failing that, they can appeal only the violation—but not the fine—in the courts, in a rare diversion from U. S. due-process laws. Hefty fines for negligence cannot now be appealed.

Changes. The new bill eases the strain in several ways. For the first time, it distinguishes between outright fraud and negligence and assesses penalties accordingly. Although outright fraud still carries the old penalty of full domestic retail value, simple negligence is penalized only with fines up to twice the loss of duty. A new category, gross negligence, carries a fine of only up to four times the loss of duty. Moreover, a company unhappy about its dealings with Customs can appeal both the alleged violation and the amount of the penalty.

"Customs is always a hassle," declares an executive with Signetics Inc., also in Sunnyvale, in a sentiment echoed by others. For one thing, the Customs Service does not tell how companies should calculate their offshore costs, and it often changes its mind on rules, the AMD executive says. He does admit that sometimes the importing companies do not always follow the accounting processes that the Customs Service has approved.

To underscore the hassles of the current law, one executive recounts the plight of a U. S. company whose Hong Kong plant substituted Far East gold wire for U. S. gold wire without declaring it in some of the 5 million devices brought in each month. Customs, in examining three devices in one shipment, discovered one with the overseas wire. The Government slapped a $16 million fine on the entire shipment.

Such import problems get complex when "a company's offshore plant is buying materials from three or four countries, assembling them, and bringing in products with 350 parts," says James Whittaker, associate manager of government operations, American Electronics Association, Palo Alto, Calif. The association has been fighting for customs reform for four years. "The whole point of the new act is to give the importer his day in court," says the AMD executive. "I'm optimistic." □

Solid state

Demand for LSI brings test crunch

The growing demand for reliable large-scale integrated circuits is starting to cause a crunch on the testing capabilities of both IC vendors and independent IC testing houses. Rather than play field-service roulette, most users are depending on the vendor and the independents to weed out the 30,000 out of every million ICs likely to fail within the first year.

At present, weeding them out involves a long burn-in that ages the ICs rapidly by operating them in a chamber at 70°C for four days and then testing them and throwing out the failures. "At present demand, vendors and testers are barely keeping up," says Gary Voget, president of Microtest Systems Inc. "Forecasts of future demand are forcing them to seek faster methods."

Surge coming. Fueling demand are the computer and instrument makers, but the needs of the telecommunications and automotive industries are expected to swell considerably within the next two years, he says. "Domestic automotive manufacturers are cranking out 10 million new cars a year, and it's no secret that they are designing in LSI electronics for many 1980 models."

Microtest, a Sunnyvale, Calif., independent testing house and manufacturer of burn-in systems, is already doing life tests on LSI circuitry for General Motors, Delco, Western Electric, and Bell Laboratories, Voget says.

To handle the expected flood, Microtest and other testing houses are developing faster burn-in and testing methods. One time-trimming technique tests the ICs functionally while they are still hot, instead of afterward in a separate operation. By combining a microcomputer-controlled combination oven and functional tester, Microtest has come up with a system to do that.

Commercial versions of these systems, two of which have been delivered, are the testing industry's first, Voget believes. They eliminate the extra time needed to unload the oven's trays, load the tester's device handlers, and test the chips.

To speed up functional testing itself both before and after aging, manufacturers of device testers are squeezing as much testing speed as

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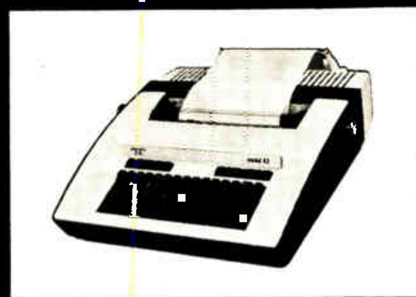

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they can from their testers and designing for simultaneous tests. Last year, for example, Fairchild Camera & Instrument Corp.'s Xincom Tester division introduced a quad test head handling four random-access-memory chips at a time.

Failure modes. Other methods for saving time are related to the causes of IC failures—problems with metalization, contamination, or oxides. A method Microtest uses to quickly flush out failures created by thin oxides—by far the greatest cause of the "infant mortality" in n-channel metal-oxide-semiconductor LSI chips, Voget explains—is to increase the differential voltage between V_{DD}, the drain supply voltage, and V_{BB}, the negative substrate bias supply voltage, from the nominal 17 volts to 25 V. Under these voltage conditions, the four-day burn-in can be reduced to a single day, he claims. The triple-supply n-MOS ICs are still the most widely used for memories and microprocessors.

"For now, we know we can reduce to one fourth the burn-in time and still expose the major contributory failure mechanism," he says. Before committing themselves to this procedure, Microtest's researchers ran tests against control lots and compared any shifts in device characteristic curves (called "schmoo" plots) between the control group with its nominal differential voltage and the voltage-stressed group. "Had there been differences, it would have indicated that we were overstressing those parts," Voget says, "but there were none of significance." □

News briefs

Mitsubishi announces IBM-compatible computers

In what may be seen as a pre-announcement to beat all pre-announcements, Sadakazu Shindo, president of Japan's Mitsubishi Electric Corp., says the company expects to complete development of a line of IBM-compatible computers in 1983.

The plans are not concrete enough for Shindo to say exactly what models in the IBM line the Mitsubishi machines will emulate or whether the line will extend to more powerful systems. The company does admit, however, that it will increase its efforts in the computer field.

When the new computers are ready, Mitsubishi will be joining two other Japanese companies in the increasingly competitive IBM-compatible marketplace. Fujitsu Ltd. currently makes the M-180-II computer, which is roughly equivalent to IBM's System/370 model 158, and is both a supplier to and an investor in Amdahl Corp. of Sunnyvale, Calif. An IBM 3031- and 3032-compatible computer is manufactured by Hitachi Ltd., which sells it to Itel, San Francisco for sale in the U. S. as the Advanced System/6.

The three companies are partners in Japan's Computer Development Laboratories Ltd. and participate in the VLSI Technology Research Association. Since the aim of both projects is closer hardware resemblance between software-compatible computers made by Fujitsu and Hitachi, it is very possible that Mitsubishi will also use similar semiconductor technology.

Color TV imports fall, exports soar

U. S. unit imports of color television receivers declined 2.4% to 660,699 in the second quarter and 5.4% to 1,212,522 in the first half of 1978, compared with the same periods a year ago, according to statistics from the Electronic Industries Association in Washington, D. C. In sharp contrast, unit exports of color TV sets increased 245.8% to 100,637 and 210.6% to 161,512 in the second quarter and first half of 1978, respectively.

U. S. hits Spectra-Physics with antitrust suit

The U. S. Justice Department has hit Spectra-Physics Inc. with an antitrust suit, charging that the Mountain View, Calif., company's 1976 acquisition of Laserplane Corp., Dayton, Ohio, gives it a 47% share of the emerging construction laser market. The suit seeks to force Spectra-Physics to divest itself of Laserplane, for which it paid $4.7 million. Worried that four companies have about 90% of the domestic construction and machine control markets, the U. S. says that Spectra-Physics was already the largest supplier of construction lasers with 24% of the market and Laserplane had about 23%. The company says the acquisition was lawful and will defend it.

Maritime

Mississippi to get new comm system

As America's weekend sailors continue to multiply, so does the congestion on the five radio channels they must now share with commercial shippers on inland waterways. They are finding the 50-kilohertz-wide very-high-frequency duplex channels busy one third of the time on the average, and even more so on summer weekends and holidays.

To relieve the communications congestion, the Commerce Department's Maritime Administration, which is responsible for inland waterways, is turning its attention first to the Mississippi River. Marad, as it is called, has a twofold plan. It wants to move commercial shippers from vhf maritime channels 24 through 28 to channels 84 through 87, which are currently unassigned there. Concurrently, it wants to implement a new automated communications system that would reduce congestion and also ensure the channels will conserve spectrum.

Marad is paying $500,000 to a new private agency that has been organized to operate the commercial system, much as Aeronautical Radio Inc. provides mobile aeronautical services to the nation's airlines. Formed by 16 Mississippi barge-towing companies, Watercom, for Waterways Communications Inc., will also contribute $500,000 to the cost of the initial system design and development.

Design study. Watercom is already paying about $100,000 to Ohio's Lorain Electronics Corp. for a study to be completed in October. The effort will identify shore-station sites for radio relays and intercon-

The Reward

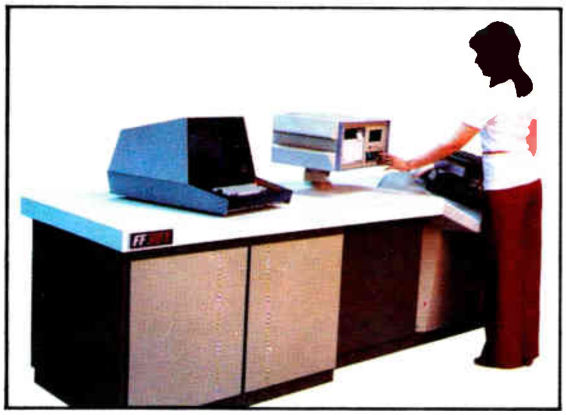
The top prize is a Model VCT200 RCA SelectaVision video cassette recorder with 4-hour continuous recording capability, remote pause control and tape counter with memory. The top ten winning entries will receive a Computime 2000 Digital Clock with six digit LED display and solid state circuitry. First 500 entrants will receive a desk model Digi-thermometer.

THE RULES: All entries must be completed on this entry form and each question must be answered in full. Only one entry per person will be accepted. Entries must be postmarked no later than October 15, 1978. Receipt of all entries will be acknowledged.

Contest is open to all U.S. residents over 21 years of age, except employees and their families of Faultfinders, Inc., its advertising agencies, and persons presently employed by manufacturers of in-circuit test equipment.

All prizes will be awarded and winners will be announced in an advertisement in this publication within 90 days of the prize awards. In case of ties, winners will be selected by drawing. Liability for taxes is the sole responsibility of individual winners.

Contest is void where prohibited or restricted by law.



Faultfinders ATE systems help you improve yield and reduce costs.

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COMPANY ______________________

ADDRESS ______________________

CITY ______________________ **STATE** ______________

ZIP ______________________ **TELEPHONE** ______________

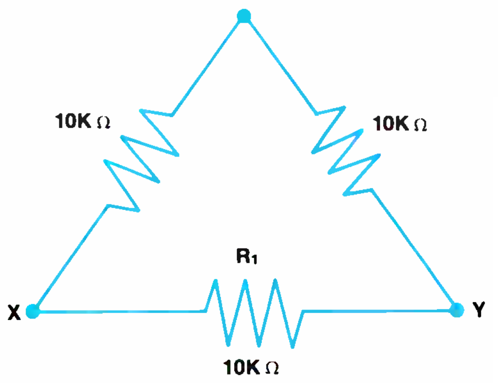
Number of PCBs you test each year: __________ **Number of employees at this location:** __________

Q. What are some advantages to using a high-level language such as BASIC for the in-circuit testing application? Check only those that are true.

- ☐ BASIC is an interpreter, which allows test code editing and easy program debug.
- ☐ Expansion of the BASIC syntax to incorporate in-circuit test program commands permits fault isolation tests to be written in a flexible programming environment.
- ☐ BASIC offers the advantages of branching and sub-routine implementation. Branching allows the test sequence to proceed according to test results, and subroutines are especially useful for implementing in-circuit digital tests.
- ☐ Arithmetic calculations may be performed on the test measurements.

Problem: Measure the resistance of R_1 with two other resistors in parallel. If an ohmmeter were connected to X and Y, what would the measured resistance be?

☐ 5K ☐ 6.6K ☐ 6.7K ☐ 15K



Q. ☐ T ☐ F

When an automatic in-circuit test system is installed, the PCB inspection and testing sequence typically follows this pattern:

Manual inspection (cosmetic repair), In-circuit fault isolation, Fault repair, Final test.

Q. "BASIC" refers to:

- ☐ An operating system.
- ☐ A task scheduler.
- ☐ A software assembler.
- ☐ A high-level application language.

Q. Automatic Program Generation for an in-circuit test system refers to:

- ☐ A diagnostic program library.
- ☐ A program to generate test statements using a circuit data set as input.
- ☐ Brute force programming.
- ☐ On-line program generation.

In-circuit test systems utilize a unique approach to digital testing. Each logic circuit or IC is tested independently of its PCB environment. The test sequence proceeds automatically (no operator interaction necessary).

- ☐ T ☐ F In-circuit systems can test for digital faults instead of simulating faults, which provides substantial fault isolation programming economy.
- ☐ T ☐ F Stuck at one, stuck at zero (at each node), adjacent pin shorts, adjacent trace shorts, loss of power or ground to an IC, incorrect one shot timing and mis-oriented ICs are faults that can be isolated by today's advanced in-circuit test systems.
- ☐ T ☐ F By controlling limited energy pulse voltage levels and timing, it is possible to safely force the input pins of an IC to appropriate levels and measure output states.

Q. "Visibility" in test parlance refers to:

- ☐ A test system fault diagnostic capability.
- ☐ The method used for electrical access to the PCB under test.
- ☐ The CRT readout of test results.
- ☐ A self-programming technique.

Circle 250 on reader service card.

The TEST

It's a real test and it demands skill and concentration. You need to know something about electronics, production and economics. And you have to use a bit of common sense.

Try the test. You'll enjoy the challenge and we guarantee you'll learn something of value about in-circuit testing. If your score is among the top ten, you'll win a Computime 2000 Digital Clock. If you have a perfect score you'll participate in the winners' drawing for an RCA Videotape Recording system and we may want to recruit you. The first 500 entries will receive a Digi-thermometer. Enter now and be a winner.

(See complete information on rewards and rules on Page 4)

Q. The term "bed-of-nails" refers to:

☐ Test system backplanes. ☐ UUT/test system interface.
☐ Test system software. ☐ Ranchipur test site.

Q. Practical in-circuit test systems were first operated in:

☐ 1952–53 ☐ 1958–59 ☐ 1962–63 ☐ 1969–70

Q. In-circuit testing is a unique approach to PCB production testing. Utilizing the guarding technique, an in-circuit test system can inspect an entire printed circuit assembly by checking each individual component against its specified values, by running functional device tests, and by checking the board itself for shorts and opens. On the production floor, how can this test approach most benefit the user.

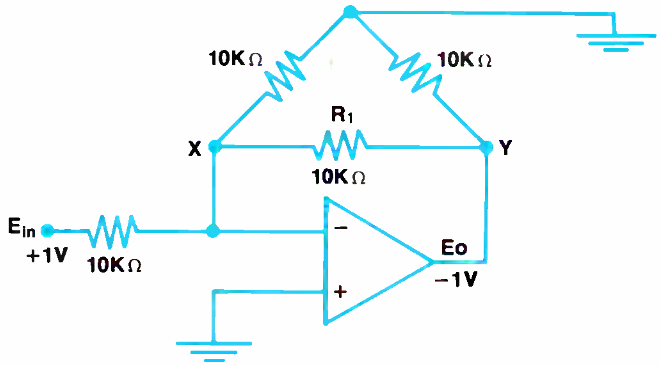
☐ Provide a go/no go test that quickly determines whether a PCB assembly is functional.
☐ Verify design faults that result from mis-matched circuit elements and race conditions.
☐ Isolate the workmanship errors and component failures that most frequently cause low PCB yield.
☐ None of the above.

Yield is the percentage of PCBs that pass a test. For example, if 10 boards are tested and 8 pass the test, yield is 80%. Once an in-circuit test system is installed, statistics show that yield is affected.

☐ T ☐ F The yield at the in-circuit test station is higher than the yield at the final test station.
☐ T ☐ F The number of boards passing final test (sometimes called throughput) will be higher than it was prior to the installation of the in-circuit test station.
☐ T ☐ F Troubleshooting time is now longer because of the added test station.
☐ T ☐ F Troubleshooting is significantly reduced because of the in-circuit test system's fast fault isolation.

Q. A guard circuit, such as the one below, would measure 10K ohms, providing that is the resistor's true value. In this op amp based circuit, the measured resistance R_1, is in the ______ position.

☐ Input ☐ Feedback ☐ Shunt ☐ None of the above



Q. What is the potential at X?

☐ +1V ☐ Virtual ground
☐ −1V ☐ None of the above.

Q. Since the in-circuit test sequence is a Fault isolation process, based on testing each component against specified tolerances, it follows that test programming is written on a component by component basis. Why does this create a cost savings for the system user?

☐ Test programming can be written by technician level personnel rather than test engineers.
☐ In-circuit Fault isolation tests are written by simply listing test parameters, rather than by developing algorithms; programming, therefore, is a straightforward task that proceeds quickly.
☐ Test programs may be easily changed in accordance with PCB design changes.
☐ All of the above.
☐ Only one and three are true.

Q. A recent development has been the introduction of mini-computer based in-circuit test systems. What advantages are offered by mini-computer control? Check only those that are true.

☐ High-level languages such as BASIC may be utilized for test programming.
☐ Development of the real time based software system enables the use of application programs such as automatic test program generation and data logging.
☐ Besides allowing peripheral device flexibility, a wide selection of programmable test instrumentation may be incorporated into the in-circuit system.
☐ Computer control helps each in-circuit test to run faster.

The in-circuit test test.

nection with telephone companies, as well as recommend the ship and shore hardware, including shipboard radios that Watercom's members may buy, according to Marad.

Watercom has also petitioned the Federal Communications Commission for use of channels 84 through 87. While the FCC has yet to approve Watercom, the system fits in neatly with its A-B-C approach to levels of maritime mobile service being proposed for the future [*Electronics*, Aug. 17, p. 40]. Level A relies on existing equipment, B uses "available technology" for more efficient spectrum use, and C applies "emerging new technology."

The degree of proposed automation for the Watercom system "will be new to shippers even though it may not be state-of-the-art," says one Marad official. Equipment will operate at the FCC's proposed new B service level. It will include automated channel selection, transmitter identification, message relay, and call setup and disconnect. The equipment will also be expected to be able to apply, at a later time, digital signals for automatic transmission of such administrative and housekeeping functions as checking and storing billing information, and ship berth reservations—operations the shippers now perform manually.

Concern. Despite the apparent advantages, the proposed division of the Mississippi's maritime channel assignments is producing uncertainties within the communications community. "Equipment manufacturers are worried about things like inventoried systems," says Raymond Wilmotte, coordinator of the FCC task force on uhf spectrum allocation. "They want to know if they are going to have to add channels to their lines, or perhaps make different kinds of radios." And maritime users have similar concerns, for which there are no firm answers yet. "Users want to know if they are going to have to carry two radios, and ask how much it will cost," Wilmotte points out. Some radio makers complain the cost of an automated shipboard system could run "out of sight—perhaps $7,000 to $8,000." □

Communications

AT&T's ACS plan is stirring queries

Apparently the hardest part about interpreting AT&T's proposal for its Advanced Communications Service still is gaging the information that *isn't* included.

American Telephone & Telegraph Co. last month asked the Federal Communications Commission for a declaratory ruling that it be allowed to file for a tariff for a switched data-communications service [*Electronics*, July 20, p. 41]. At that time, many observers and members of the data-processing and -communications industries declined to comment until they could study the filing [*Electronics*, Aug. 3, p. 79]. Now, even as the first industry comments are being filed with the FCC and the first of the consulting firms' seminars are being held, the technically vague document still raises more questions than it answers.

"There is conspicuously less detail as to the exact service features to be offered in ACS," points out the Computer and Business Equipment Manufacturers Association in its comment to the FCC. At the same time, the Washington, D. C.–based organization points out, the ACS proposal "describes at great length AT&T's conclusions that users need a service which can interconnect various data equipment and networks."

Questions. Many of the questions CBEMA and others have raised involve the proposed message-editing and -handling features of ACS and the regulatory issues of cross subsidization of the new service by the established monopoly voice service. They include:

- What is the programming language to be used with ACS and what functions will it provide?
- How will AT&T prevent customers from programming ACS to perform more than the message-formatting and -editing functions proposed?
- To what extent can a customer

format his input data and manipulate it according to his needs?

■ How will the costs already incurred for the research and development of ACS be reflected in the planned cost accounting system?

Because of these uncertainties the association urges the commission "to undertake a comprehensive investigation to determine the exact nature of ACS."

Such an investigation will probably take the form of an FCC demand for a more extensive AT&T filing, according to Howard Anderson, president of the Yankee Group, Cambridge, Mass. His consulting firm organized a seminar on ACS earlier this month in New York. Anderson says such a request for a more detailed filing could delay AT&T's planned implementation of ACS, and this date is still uncertain, by a year and a half.

Anderson also questions whether Bell will develop the marketing expertise he thinks is needed for the new service. "The sophisticated systems sell is something AT&T is not used to doing," he notes.

AT&T briefing. Apparently in response to the questions, AT&T has decided to hold briefings for equipment suppliers on Sept. 18, 20, and 21 in Bedminister, N. J., Chicago, and Los Angeles, respectively. Firms can get more information by calling (800) 526-0642 or (201) 540-6592 in New Jersey.

As the seminars and FCC filings continue, the number of questions and interpretations will undoubtedly increase. The New York securities firm of Oppenheimer & Co. has scheduled sessions for Oct. 4, 5, and 6 in New York, Chicago, and San Francisco, respectively, and Gideon Gartner, the seminar's organizer, says the interpretation may be more complete, since the FCC filings should be complete by then. Among other things, the Oppenheimer-sponsored sessions will feature comments by William Stritzler, an AT&T marketing director, who has been asked to address the questions of compatibility and functionality, as well as AT&T's best estimate for the availability of the service, Gartner adds. □

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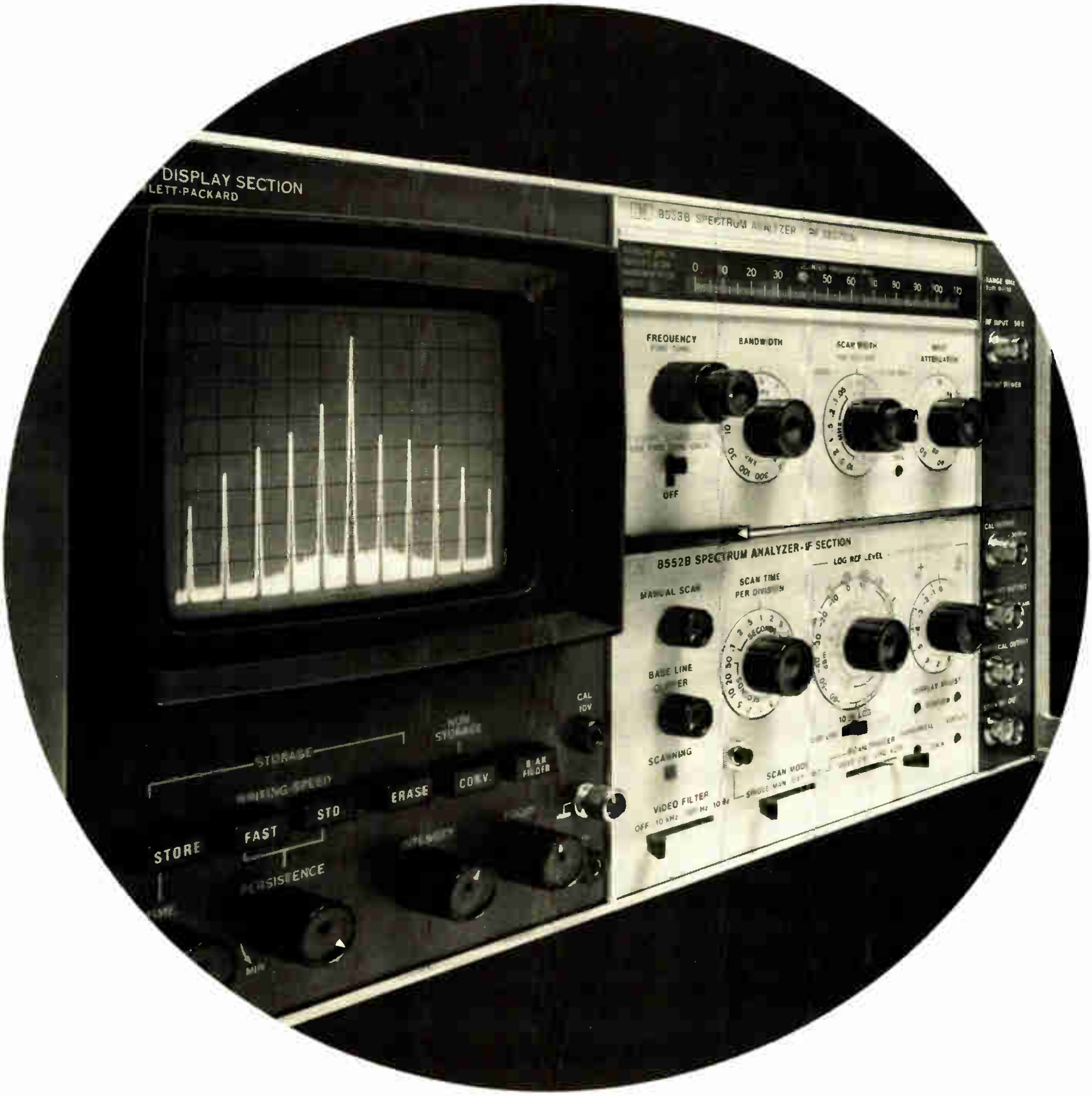

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8552B	High Resolution IF Section	$4025
8556A	20 Hz-300 KHz RF Section	$2525
8553B	1 kHz-110 MHz RF Section	$3350
8443A	Companion Tracking Generator/Counter	$5000
8554B	100 kHz-1250 MHz RF Section	$4975
8444A	Companion Tracking Generator	$3675
8555A	10 MHz-40 GHz RF Section	$8100
8445B	10 MHz-18GHz Automatic Preselector	$3180

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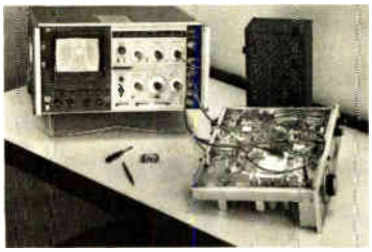
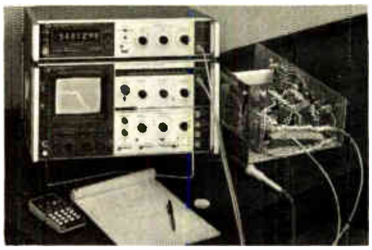
Circle 57 on reader service card

20 Hz to 300 kHz



The 8556A tuner covers 20 Hz to 300 kHz and comes with a built-in tracking generator. It's calibrated for measurements in both 50 and 600 ohm systems, with accuracies better than ±1 dB. Highest resolution is 10 Hz.

1 kHz to 110 MHz

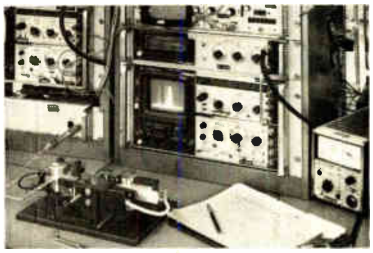


The 8553B takes you from 1 kHz to 110 MHz with −140 dBm sensitivity and resolution as high as 10 Hz. Signals can be measured with ±1¼ dB accuracy. Choose the companion HP 8443A Tracking Generator/Counter for wide dynamic range swept frequency measurements and precise frequency counting.

100 kHz to 1250 MHz

Use the 8554B tuning section to cover the 100 kHz to 1250 MHz range. Maximum resolution is 100 Hz. Measure with ±1¾ dB accuracy. Its companion HP 8444A Tracking Generator (500 kHz to 1300 MHz) also works with the 8555A tuning section.

10 MHz to 40 GHz



For 10 MHz to 40 GHz, choose the 8555A. Its internal mixer covers to 18 GHz, accessory mixer for 18-40 GHz. Maximum resolution is 100 Hz. Measure with ±1¾ dB accuracy to 6 GHz, ±2¾ dB to 18 GHz. For wide scans free from unwanted response between 10 MHz and 18 GHz, add the HP 8445B Automatic Preselector.

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Washington newsletter

Cost curbs on medical technology proposed by OTA

Legislation that could limit the market for medical electronic instruments is expected in Congress this fall, following a report to the Senate Committees on Finance and Human Resources that links rising medical costs with insufficient evaluation of new diagnostic technologies. **Too many instruments are bought prematurely and are used too much,** says Congress's Office of Technology Assessment; as a result, equipment and use charges—largely reimbursed by third parties such as medical insurance companies and Federal agencies—are soaring.

As an example, OTA's report traced the installation and use of the more than 1,000 computerized tomography scanners in the U. S. from their introduction in 1973 to the end of 1977. The scanners, invented in Britain, combine X-ray equipment with a computer and a cathode-ray-tube display to produce cross-sectional images of the body in three dimensions. For 1975–76, the annual operating cost of a scanner ranged from $259,000 to $379,000 according to the report. Moreover, the units cost about $500,000 apiece, yet scaled-down systems using solid-state technology will shortly drop instrument cost to $100,000 or less, estimates OTA.

Sanders, Raytheon to build color ATC radars

Four-color displays are coming to air traffic control radars with Sanders Associates Inc. and Raytheon Co. heading the competition for the developing market. The Naval Electronic Systems Command has picked **Sanders over Raytheon and others for a $4.9 million award to produce 36 displays,** each with its own 16-bit processor, for use at Navy air stations at Jacksonville, Fla., San Diego, and the Virginia Capes.

Raytheon must content itself with a $186,000 Federal Aviation Administration award to modify six monochromatic displays for four-color tests next year at the agency's Atlantic City, N. J., experimental test center and the Leesburg, Va., air route traffic control center. The FAA displays will add red for map lines and navigation aids and orange for weather, with yellow and existing green for aircraft identification data blocks.

Lockheed developing 12.5 kW solar array for space shuttle

Production of solar electric power in space is getting a major boost with a National Aeronautics and Space Administration award of $2.7 million to Lockheed Missiles and Space Co., for development of a massive solar-array wing for a November 1980 flight test aboard the space shuttle. **The retractable experimental wing will measure 105 by 13.5 feet when extended** and will contain 41 panels each carrying 3,060 silicon solar cells able to generate a total of 12.5 kilowatts. Only three panels will be active during the first flight test which will measure structural and dynamic characteristics as well as electrical performance.

FCC hears support for ACS concept from large users

The Federal Communications Commission is hearing strong support from large potential users of American Telephone & Telegraph Co.'s proposed Advanced Communications Service [*Electronics*, July 20, p. 41]. An *ad hoc* committee of 15 large-business users of telecommunications, all presently using data services provided at AT&T, told the FCC that **efficient and cost-effective data communications is increasingly essential to effective use of distributed data-processing nets, large-system time-sharing, and direct computer-to-computer links** by large companies. The users conclude: "Someone, be it the user or the carrier, must perform speed, protocol, and other conversions if users are to have maximum flexibility."

The solid-state revolution is only just beginning

Where is solid-state technology taking society, and what will be its impact on life styles for the long term? How should the community of electronics researchers, engineers, and managers direct these changes? Such questions are not asked often enough by those who rarely have time to step back from the work at hand. Yet they are issues that National Science Foundation director Richard C. Atkinson must evaluate regularly. His conclusions, excerpted here from remarks prepared for the Scripps Institute of Oceanography's 75th anniversary this summer, are stimulating. **Ray Connolly**

It is inevitable that the size and cost of microcircuits will continue to decrease while their processing power increases. The key to further advances lies in our ability to fabricate microcircuits smaller and more densely packed than the optically etched chips available today. By using X-ray lithography, or energetic electrons, we will achieve at least another tenfold reduction of component size and a corresponding increase of several orders of magnitude in processing speed. Today, a well-designed commercial chip can accommodate up to 16,000 functions, but in the near future this density will increase to 160,000 or more. Clearly the remarkable data-handling devices on the market today represent only the first steps toward almost universal access to sophisticated information-processing systems.

The new revolution

The invention of the computer some 30 years ago is comparable to Johannes Gutenberg's invention of the movable-type printing press in the 15th century. Some three centuries elapsed before the full potential of the press and its product, the printed book, were realized. Literacy had to be achieved on a wide scale before books became relevant for any but the elite. And there had to be an industrial revolution to put the cost of the book—and the means to buy it—within reach of a substantial market. With respect to the computer, the microprocessor—in conjunction with a spectrum of new telecommunication technologies—is compressing this time span into three decades.

For the most part, computers have taken over tasks previously handled by human beings. Now that is changing. Problems are being posted for the computer that do not just replace humans but do totally new things. As a society, we are entering unfamiliar terrain.

The task of scaling down microcircuitry itself involves basic research: research on semiconductors and polymeric materials; research on the chemistry of surfaces and etching; research into advanced electron and ion optics and into the effects of radiation on matter; and research on the mathematical properties of large data systems. Indeed, the list of scientific areas involved in microcircuitry development spans almost the entire spectrum of basic research.

NSF has moved to support research in this area by establishing a national submicron facility at Cornell University. This facility will provide both university and industrial users with the specialized resources to do advanced research in this field. The facility is just beginning to operate, but the prospects are exciting. Continued progress in reducing the size of data processors will carry us to frontiers far beyond those penetrated by the relatively straightforward computerization of traditional scientific instruments. There will be fundamental changes in the way research is done at the microstructure scale.

Coping with the future

Recent developments in artificial intelligence and cognitive psychology have given us a glimpse of the type of processes that may underlie truly intellectual behavior. But we are a long way from realizing a theory of human cognition that explains how the mind operates in making a scientific discovery or even in choosing between political candidates. The changes in information processing that I foresee may finally permit theory in the behavioral sciences to measure up to the complexity of the phenomena they are attempting to understand.

What is particularly important at this time is to avoid a marketeering mentality. Hardware and gadgets should not drive our decision-making in this area; rather, we should stress the exploration of new approaches and new ideas. I can vividly recall the derogatory remarks made by some visitors to the Stanford Computation Center about several young computer workers who were disheveled, unshaven, and literally spent every waking moment with their computer. But it was these very individuals who provided the creative thrust for a new programming language and an innovative system design. We must guarantee an environment—particularly in our universities—where scientists will be able to pursue ideas in this field in an open and free fashion. If the university meets its obligations in this regard, we will have gone a long way toward ensuring that the information revolution will strengthen and not undermine individual rights and freedoms.

There's one fully programmable LSI test system priced under $200,000

The MX-17, at $37,750

The MX-17 is an automatic, fully programmable LSI test system. At $37,750, base price, it is by far the most affordable software-programmable system on the market.

MX-17 performance is equally impressive. The MX-17, in fact, is the *only* small system that can deliver every one of these large-system capabilities:

A powerful production/engineering tool

A true general purpose system, the MX-17 permits completely valid electrical and logical testing of microprocessors, support chips, RAMs, ROMs, and custom LSI devices. It can be used for manual test or with automatic handling or probing equipment.

As an engineering tool, the MX-17 provides error diagnostics, full reporting capabilities, data logging of all test variables, and "joy-stick" slewing of parameters.

Software programmable

Unlike other low-cost testers, the MX-17 is fully programmable. Logic sequences, strobe placement, phase widths and relationships, and data and address formats are all under program control. Test variables can be changed as required, allowing the device under test to be stressed and margined for worst-case conditions.

Faster test times

No laggard, the MX-17. All pins are tested simultaneously for continuity. Rigorous tri-state testing is done at speed during functional testing. And DC parametric tests can be made on a pin-by-pin basis, or in parallel.

The result? Higher throughput than any other LSI test system, regardless of price.

Field expandable

The MX-17 is completely field-expandable by simple card plug-in. The expanded system can include 69 timing edges, 21 voltage levels, 56 drive/sense channels, a 32K controller memory, and storage for truth tables up to 65K.

Available now

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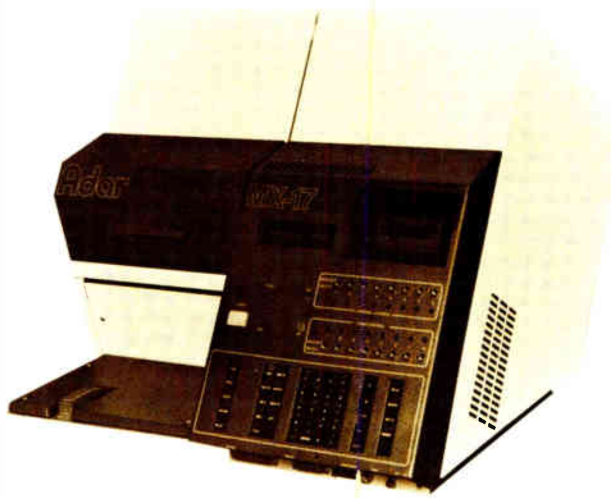

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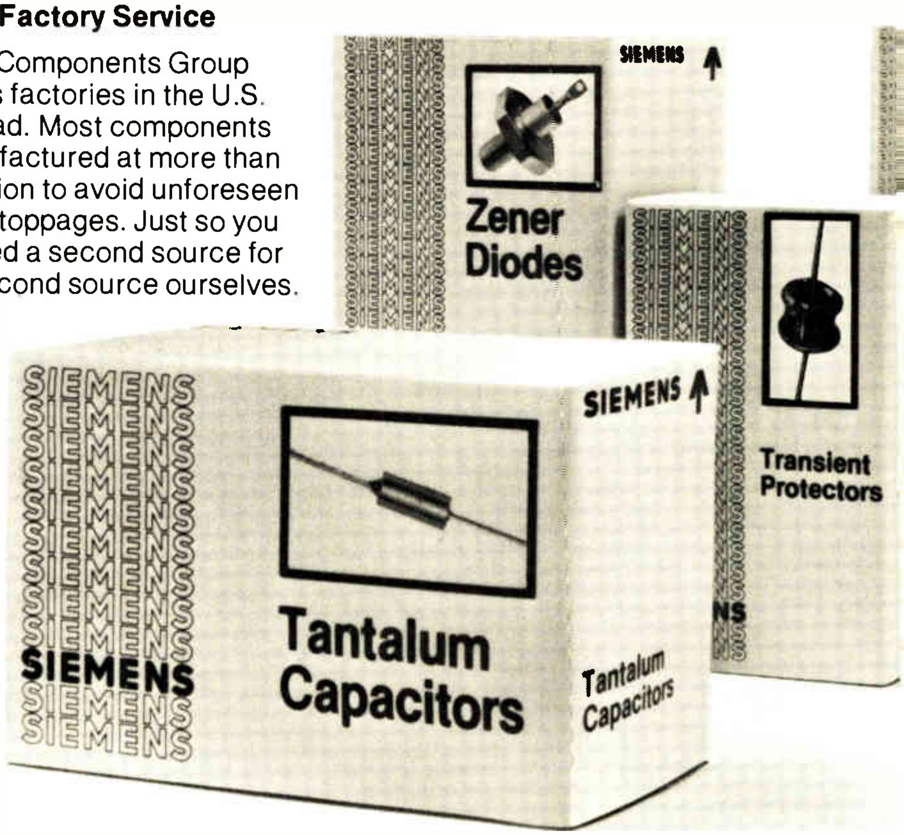

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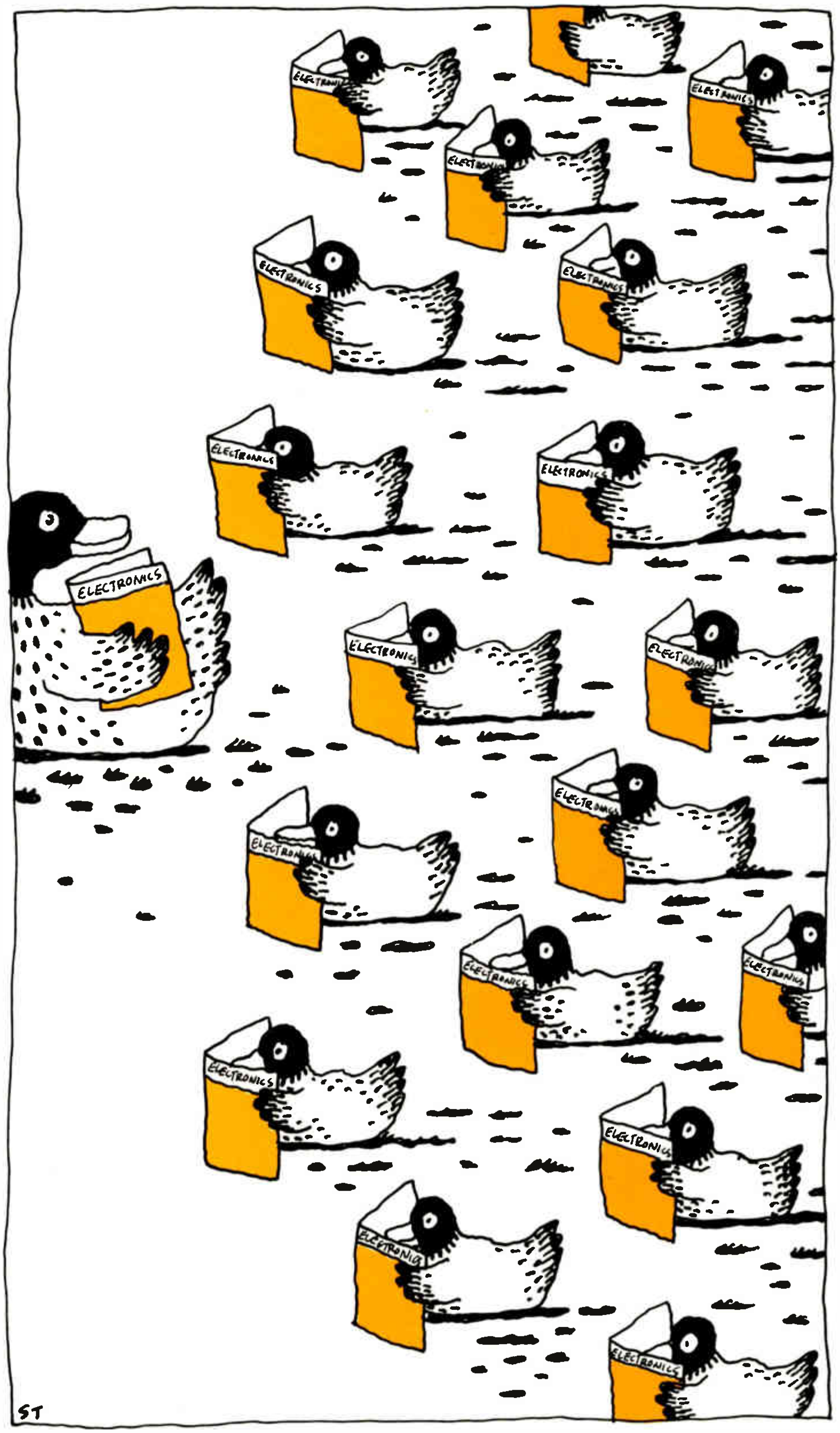

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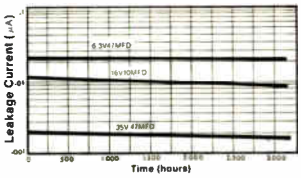

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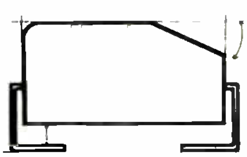

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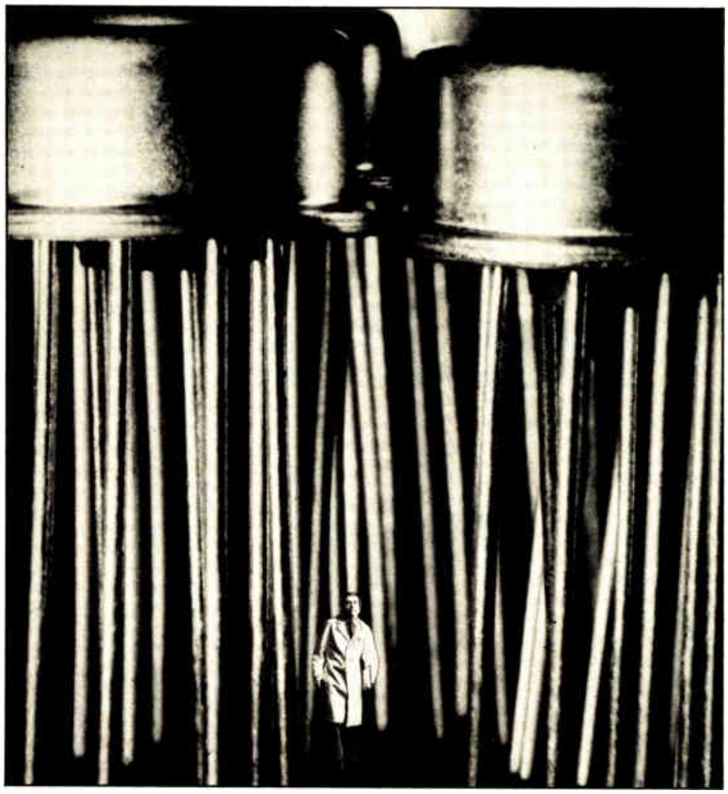

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CA3130	0V to $(V^+ - 10V)$	10mV to $(V^+ - 10mV)$ $R_L = \infty$ 10mV to $(V^+ - 3V)$ $R_L = 2K\Omega$	50pA	10V/μsec	Op Amp
CA3140	0V to $(V^+ - 3V)$	1V to $(V^- - 3V)$ $R_L = 2K\Omega$	50pA	9V/μsec	Op Amp
CA3160	0V to $(V^+ - 10V)$	10mV to $(V^+ - 10V)$ $R_L = \infty$ 10mV to $(V^+ - 3V)$ $R_L = 2K\Omega$	50pA	10V/μsec	CA3130 with internal compensation
CA3240	0V to $(V^+ - 3V)$	1V to $(V^+ - 3V)$ $R_L = 2K\Omega$	50pA	9V/μsec response time	Dual CA3140
		V_{IO}			
CA3290	0V to $(V^+ - 3.8V)$	20mV	50pA	100V/μsec	Dual Comparator

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International newsletter

Matsushita shows 16-K RAM no bigger than 4-K device

Matsushita is showing its prototype of a 16-K static random-access memory that is about the size of a 4-K RAM. The secret is a new configuration: the two polysilicon load resistors are fabricated in the second poly level overlying a silicon-dioxide insulating film on top of two of the four n-channel silicon-gate transistors. With minimum dimensions of 3 μm, cell area is 23 by 27 μm and chip area is 3.75 by 4.19 mm, or 15.7 mm^2. **Organized as 2,048 by 8 bits, the 16-K RAM has 100-ns access and cycle times** and operates from a single +5-V supply with TTL input/output levels. Operating current is 145 mA; standby current is 30 mA. It will be some time before the device appears, unlike the very similar 16-K static part from Texas Instruments.

West German PO to spend billions for expanded services

After years of keeping the lid on investments, West Germany's post office is in the spending mood again, which spells boom times of sorts for the country's 30-odd producers of communications and related equipment. For the next five years, **the agency has earmarked some $12.5 billion for telecommunications, primarily for telephone services.** The chief goal is to outfit all households with phones by the mid-1980s. Included in the planned expenditures is about $1.7 billion for phone network expansion and for increasing the capacity of existing links. The post office says billions have also been set aside for new services like Viewdata and cable television, although the exact amount has not been pinpointed.

Codec will dub TV programs with many languages

The Tesla Electronics Research Institute in Prague is working on an experimental coder-decoder for eight-language accompaniment to TV video signals. **The eight sounds are transmitted digitally and independently of each other and are decoded as desired at the receiver,** much as a codec mixes different telephone channels for transmission. Such a system would be particularly useful across Europe's many borders.

Switchable modem sends and receives low and high

Sescosem of Grenoble will be offering samples of a new low-speed modulator-demodulator chip in the fall. The complementary-MOS circuit has some functional similarities to Motorola's MC14412 but can send and receive in either high or low frequency. Modems are usually limited to sending in low frequency and receiving in high frequency. Like some other modems, the new SF.F 96501 from the Thomson-CSF division also can switch frequencies, enabling its terminals to call each other directly instead of via a central control. **With this combination of the two features, the chip will be a natural for the portable terminal market, Sescosem thinks.** Initially the modem will be limited to 300-baud European-standard transmission, whereas the Motorola chip offers U. S. and European standards and a 600-baud speed. Launch price for the SF.F 96501 is $40 to $50, though volume orders could bring the price down to nearer $10.

Siemens moving LED production to Malaysia

Customs barriers and high labor costs are prompting Siemens AG to shift the mass production of light-emitting diodes and related devices from its home plants to Malacca, in Malaysia, where the West German company is already manufacturing other semiconductor components like transistors. Remaining at its domestic optoelectronic facilities near Munich are only pilot lines for LEDs and for producing the gallium-phosphide base material used in optodevices. Production is slated to increase from the current rate of 80 million LEDs per year to between 120 million and 150 million annually during the early 1980s. Together with its recently acquired subsidiary Litronix Inc., Cupertino, Calif., Siemens says it has a share of the world's optoelectronics market of better than 6%, putting the twosome among the top five producers in the field.

Digital technique adjusts temperature in quartz oscillator

Coming up from Racal Electronics Ltd. is an LSI quartz-crystal oscillator that uses a new precision digital technique for temperature compensation to achieve a frequency accurate to within 5 parts in 10^8. University of Bath researchers developed the technique, which gives accuracy comparable to that of oven-controlled oscillators but at a fraction the cost and power consumption. Racal, which funded the work, will produce a one- or two-chip version. **Similar to an approach developed by Hewlett-Packard in the U. S., the technique employs two co-mounted crystals,** one of which is a conventional AT-cut crystal and is used as a reference in a frequency synthesizer. Temperature-induced frequency variations in the second, Y-cut crystal are translated by a counter and read-only memory into a synthesizer control signal. The frequency stability that results is needed for future single-sideband radios and can be used to advantage in present-day maritime and land-based communications systems.

Computer to monitor TV/radio signals right off the air

A computer-controlled system for wireless monitoring of radio and television stations is taking shape in Belgium. A development of the Belgian broadcasting organization BRT and West Germany's Rohde & Schwartz, **the system will cyclically check the signals from four fm radio transmitters and eight television stations.** To monitor sound and picture quality, the signals are picked off an antenna at a Brussels monitoring center and are measured with R&S equipment. Then a Philips P857 computer evaluates the signals. The system greatly simplifies signal monitoring because only one set of instrumentation is needed for all stations.

Addenda

Bowing at Technograph and Telegraphs Ltd. is **a British version of the Multiwire technique for making highly dense printed-circuit boards.** Produced under license from the Photocircuits division of the U. S. firm Kollmorgen Corp., the UK technique will be called Multiwire. . . . Olivetti will begin marketing its $2,400 ET 101 **electronic typewriter next month, with major exports planned to the U. S. in particular.** Included are memories that store each line of type while permitting corrections and that store recurring phrases, justification, and page and table layouts. . . . The hot competition in the exclusive, yet lucrative, market for advanced air-defense radar systems has a new contender: Marconi Space and Defence System Ltd.'s portable Martello system. **The new three-dimensional, L-band, 300-mile-range radar incorporates advanced techniques** such as phased-array technology, multibeam tracking, frequency agility, monopulse processing of signals in parallel beams, and parallel signal processing. . . . A highly sensitive perimeter alarm system using Standard Telecommunications Laboratories fiber-optic cable is coming from an English firm, Branglea Ltd. **All an intruder has to do is to stretch or cut the cable, thus disturbing the pulse-coded light signal in the fiber,** and an alarm will sound at the monitoring point.

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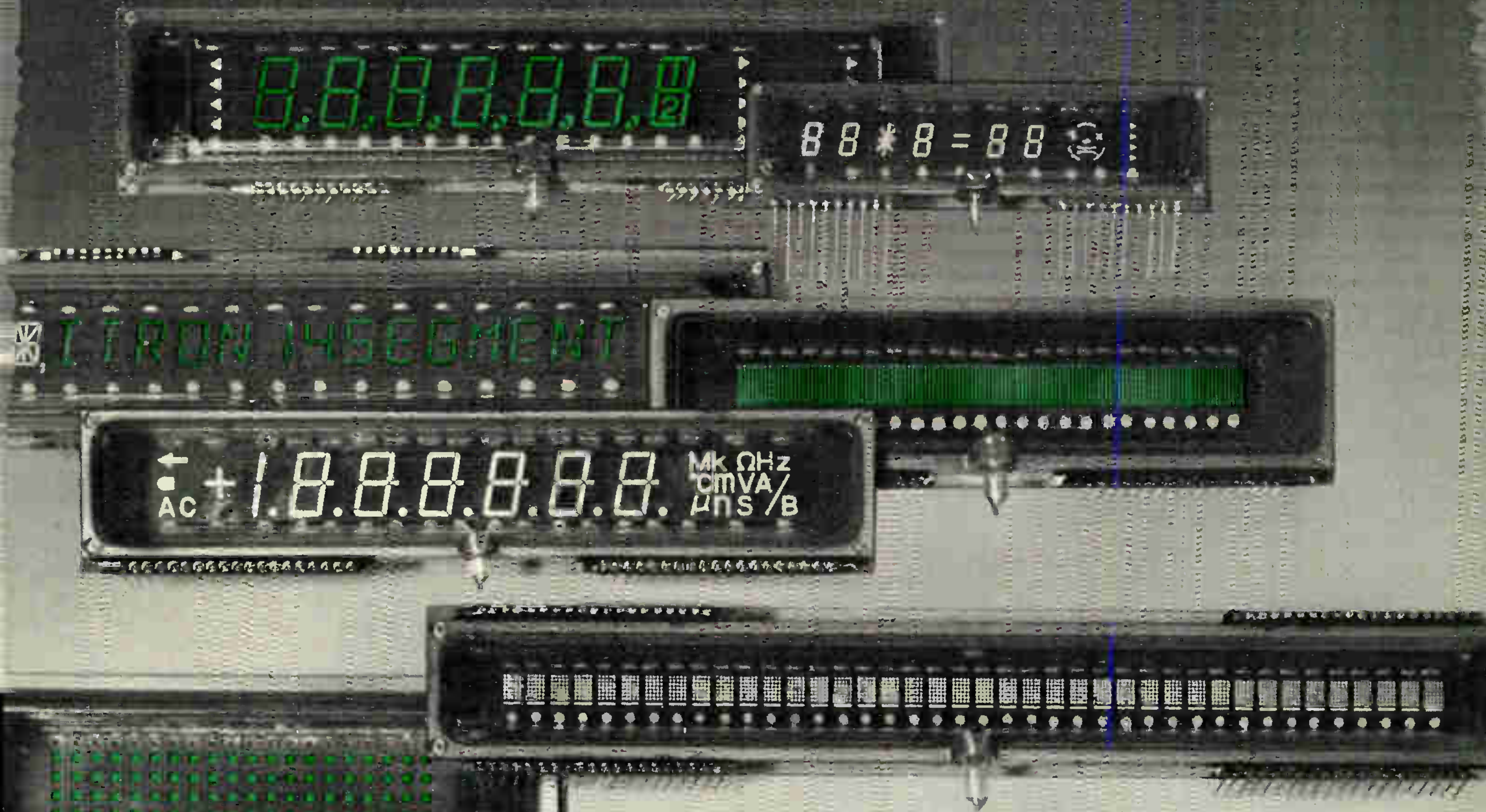

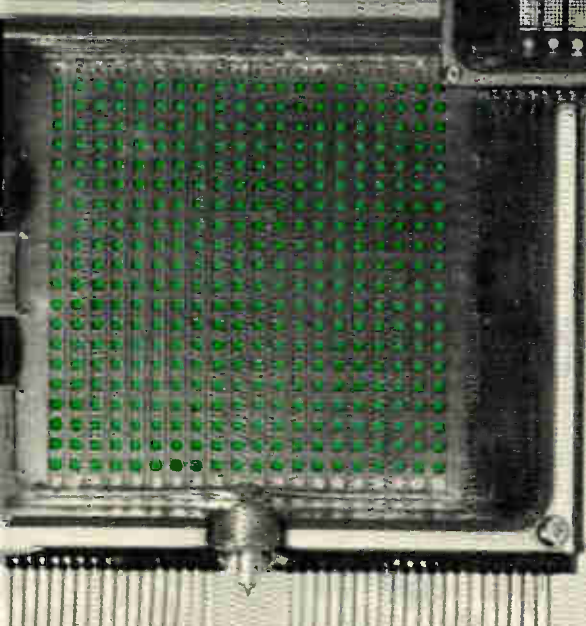

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re Radiometer Electronics ...... *Quality Beyond Measure*

Mini-based system synthesizes speech in real time

Wave-function synthesizer has a four-step program for high-quality speech, in effect from an unlimited vocabulary

Sit down at SARA's keyboard, type in a sentence, and right away a loudspeaker reproduces it. What's more, this speech synthesis system is based on a French minicomputer, not a mainframe, and gives high-quality speech in real time. SARA stands for Synthétiseur Automatique Rapide.

Under development by CEA, the French atomic energy agency, at its electronics laboratory in Saclay, the wave-function synthesizer uses a four-step program to produce speech. The simplicity of the calculations involved gives SARA its speed. The program also constructs a "voice" to sound much more human than that of other speech synthesis techniques.

"Traditional approaches to the speech synthesis problem have usually meant big expensive computer hardware or very slow response times to achieve an acceptable quality of speech synthesis," says Benoit Dupeyrat, a researcher at the Saclay lab. Built around a 32-kilobyte Intertechnique Multi 20, SARA can take an alphabetic data stream from a keyboard or other digital inputs.

In limbo. Such a system could serve a wide range of inquiry systems for which a voice response is desirable, such as inventory control or orders placed by telephone. However, commercial development is uncertain at this point, although there is an advanced version with even better voice fidelity under way.

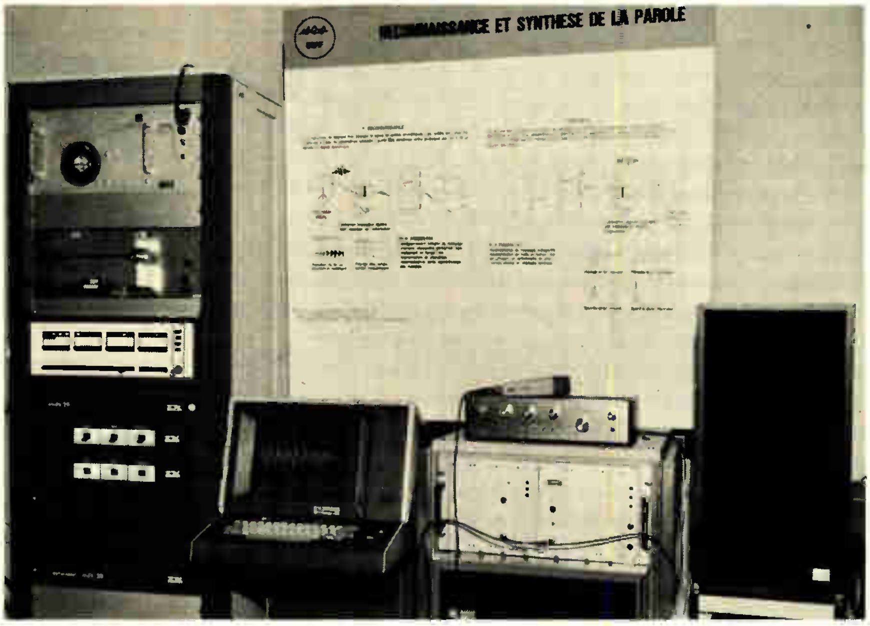
In effect, SARA has an unlimited vocabulary, because it synthesizes its words from syntactical and grammatical rules, rather than from a fixed vocabulary. The first software step converts the input into a phonetic stream. Basically this step uses a set of rules that give the pronunciation for each letter based on its context. A dictionary of the more common exceptions supplements these rules.

Another important part of speech synthesis is a satisfactory intonation. Without near-human stresses and rises and falls in the "voice," the speech at best will be the metallic science-fantasy robot voice and at worst barely intelligible. Thus the program breaks each sentence into what the Saclay researchers call "intonational clusters" by detecting "grammatical function words," the articles, pronouns, conjunctions, and so forth that signal different parts of the sentence. This second step can introduce pauses and impose a melodic pattern between the lengthier pauses, while superimposing other intonations as appropriate.

The next two steps are both calculation steps. The first works out the acoustic characteristics of the signal, including amplitude, from the constituents of the vowel-consonant-vowel chains. As in other speech synthesis approaches, this step is fairly complex number crunching.

However, the final step, which constructs the sound wave, is relatively simple, says Xavier Rodet, one of the originators of SARA and now a consultant working on the advanced

Speak to me. New speech synthesis system from France produces real-time responses of high-quality speecn with a 32-kilobyte Intertechnique Multi 20 minicomputer.



phones receive each three-frame signal, but only the phone called responds by latching its link-switch IC onto the designated speech path. The three-frame signal is composed of digital dc pulses; the voice signals are analog.

Since the originating number is transmitted, it is possible to show it on the display of the called phone, handy for paging, transfer of incoming calls, and the like.

The standard system is optimized for about 60 phones connected in daisy-chain fashion; capacity can be stretched to 100 simply by lengthening the chain. A single five-pair cable can provide three simultaneous voice circuits; an optional eight-pair cable can provide six. □

Great Britain

Frequency-synthesizer ICs ready assault on the mobile-radio communications market

Integrated-circuit frequency synthesizers are beginning to do to multiple-crystal frequency references what the transistor did to the vacuum tube: after supplanting crystals in U. S. citizens' band radios, the IC synthesizer is ready to move on to the commercial mobile radio field. Coming up later this year in the top-of-the line M206 set from Pye Telecommunications Ltd. of Cambridge is a two-chip set designed by fellow UK Philips affiliate, the Philips Research Laboratory.

The two-chip phase-locked-loop synthesizer (see figure) uses Philips' proprietary Locmos complementary-metal-oxide-semiconductor technology in 28-pin packages. One chip incorporates a 4½-decade programmable frequency divider that accepts a 9-megahertz input level at 10 volts. It is used with standard emitter-coupled-logic prescalers, giving the system a full 6½-decade division ratio and a 4.5-gigahertz maximum frequency.

Two comparators. A second chip includes two phase comparators and the frequency reference divider, used to step the 5-MHz reference oscillator down to the required channel-spacing frequency. The reference divider has a directly programmable range of 1 to 1,024 and a prescaler with division ratios of 1, 2, 10, and 100. It allows a high degree of flexibility in the choice of crystals and reference frequencies.

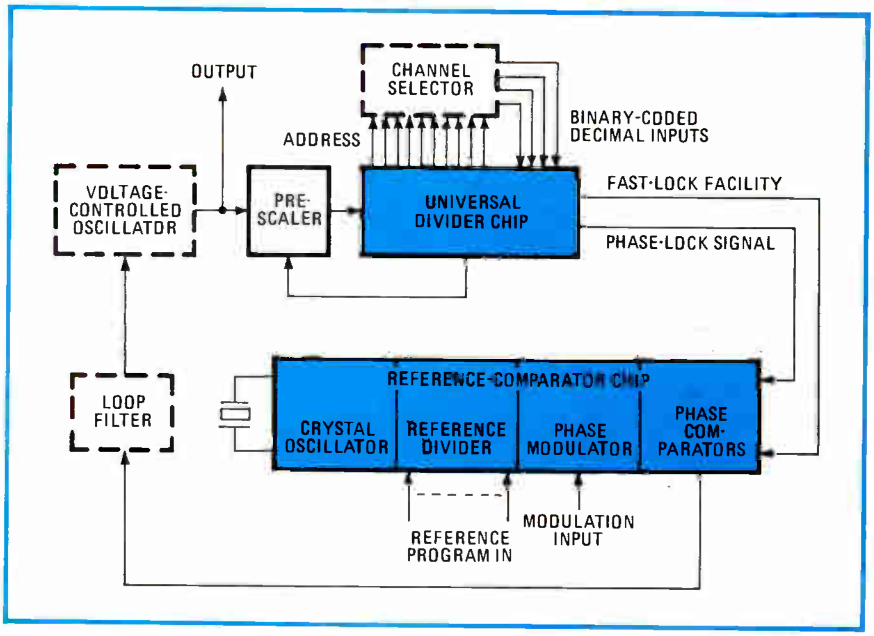
General availability of the chip set could follow next year, according to one company engineer, although officially Philips is not even committed to commercial production. Already, though, other manufacturers are jumping in.

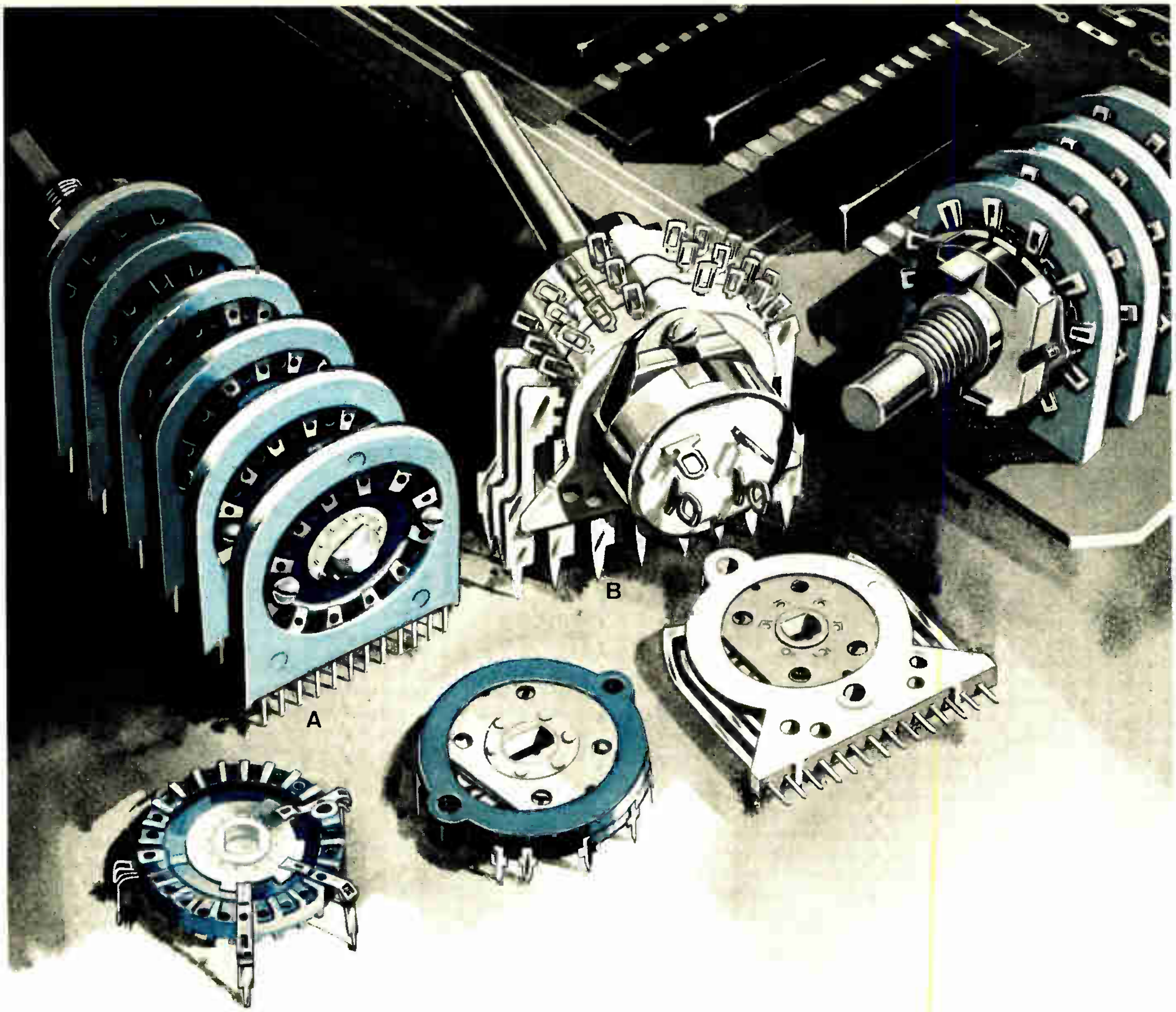
The U. S. Philips subsidiary Signetics Corp. will also offer the set. In the UK, Plessey Semiconductors Ltd. has in the works a 60-MHz-to-1-GHz two-chip universal synthesizer set in low-cost, 16-pin packages. One chip is a programmable high-speed ECL prescaler used as a four-modulus divider, and the other is an n-channel MOS programmable divider-comparator chip that is microprocessor-compatible and accepts data in 4-bit bytes. Both chip sets are for full-fledged mobile radios and are designed to outperform integrated synthesizers developed for the CB market [*Electronics*, April 28, 1977, p. 77].

Of the two chip sets, the first likely to get into equipment in a big way is the Philips chip set: Pye Telecommunications, the UK's largest mobile-radio manufacturer, plans over the next five years to design it into all its models. Initially, though, the synthesizer will be used in top-of-the-range models, since it adds $50 to the component cost of a mobile radio over present multicrystal synthesizers.

But there are compensating advantages in manufacturing a single standardized product instead of customizing each production batch for specific users, says Hugh Hamilton, Pye Telecommunications' development manager. In the future, he says, all of the firm's mobile radios will have a single 5-MHz bulk-purchased crystal, thus cutting crystal inventory and simplifying production. Channel requirements will be loaded into a programmable read-only memory, which controls the frequency-divider ratio and sets the

Quick reference. Two-chip frequency synthesizer from Philips is intended for mobile radios. It uses two comparators to overcome the noise problem inherent in building high frequencies.





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channel allocation as well.

Frequency synthesizers first made the grade in military systems like the UK Army's Clansman radio, because they allow the operator to switch over a wide range of channels to avoid enemy jamming. But performance barriers, as well as the high cost, prevented an easy jump to commercial markets. "The major problem with frequency synthesizers is the amount of division you can apply without running into sideband noise," says Hamilton.

"We use two comparators in the phase-locked loop, a digital type with three-state outputs that is frequency-sensitive and locks fast, and a high-performance analog phase comparator, which is the guts of our system," Jordan says. After the signal is captured, the digital lock switches out and loop control passes to this low-noise comparator. □

Austria

Cable-TV boom is giving an additional boost to electronics industries already doing well

Small, landlocked Austria, nestled in the highlands of Central Europe, is beginning to draw the attention of European television experts with its feverish activity in cable-television. Its rush into what some German observers call "das totale Fernsehalter" (the total TV age) is fueling the healthy local electronics industries.

All over the Maine-sized country of seven million, cable-TV companies are sprouting to give the population more program variety, particularly in entertainment shows. The craving for additional programs is particularly strong in areas where West German and Swiss broadcasts cannot be picked up because of the mountains or because of the distance. Eventually all major cities, such as Innsbruck in the west and Klagenfurt in the south, and many medium-sized towns will have cable service.

Vienna's plans. By far the biggest network is being laid in Vienna. In a project valued at nearly $150 million, some 450,000 households will be wired up during the next six to seven years. Since the city's population is 1.6 million, it will form one of Europe's most extensive and tightly knit cable-TV systems. The first 60,000 or so households should have service before the end of the year.

Handling the project is a company established by the Austrian subsidiary of Philips Gloeilampenfabrieken and Kabel-TV Wien. With its 95% share, Philips is shouldering most of the burden—and taking on most of the financial risk. Kabel-TV Wien, owned by the city, is handling the $4.6 million job of installing the microwave links that feed in the foreign TV programs.

The project's initial phase calls for feeding in one of West Germany's two national broadcast programs, with the other to follow next year. By 1980, German-language programs from Switzerland and an English program (mostly for workers at United Nations facilities and other international organizations in Vienna) will be added. Radio programs also will be coming in.

Although Vienna owns but 5% of the new cable-TV company, the city fathers are making sure that the project benefits local firms the most. At least 80% of the $150 million outlay to wire up the city will go to Austrian companies. Moreover, the city will see to it that small and medium-size firms will get their share: the $20-to-$30-million cost of connecting individual households to the system will go to them.

Boost to business. Austria's activities in cable TV spell an added boost to her electronics industries. Although the growth of the country's overall economy has slowed to a snail's pace—about 1.5% is forecast for this year—the electronics markets are not doing badly at all. Outpacing most other sectors is components: domestic sales of both passive and active devices are predicted to rise 33% during the 1976-to-1979 period, from $260 million to $340 million. Active devices account for roughly 45% of these totals.

Sizing up Austria's market for semiconductors, officials at Texas Instruments in West Germany see sales growing about 15% this year—from $30 million in 1977 to $34.5 million. There is an almost even split between discrete and monolithic integrated devices. With a share of about 60%, the entertainment electronics sector is by far the biggest components user.

Besides the Austrians' penchant for entertainment products, there are several other factors behind the upsurge in components. One is the business that Philips' big videocassette-recorder factory in Vienna is generating. (The Dutch company makes all its VCRs in Vienna.) Another is the huge components consumption by Grundig AG's TV-set plant, Europe's largest, that the German firm started up in Vienna last year. Still another factor is the production of quasi-electronic telephone exchange systems that Austria's communications industry began last year.

Consumer up. The consumer electronics market will rise about 8%, from $220 million last year to $238 million this year, according to ITT marketing experts in Germany. Color-TV sales are doing better than the average. About 270,000 color receivers are expected to be sold this year, 30,000 more than last year.

Less steep than the consumer-products sales curve is that for Austria's measuring-and-control-equipment sector. The increase from $53 million in 1975 to $60 million in 1979 translates into only a 13% rise for the total five-year period.

But the slack in some sectors is more than offset by the strength in the computer field. The number of computer installations rose by some 17%, from 12,157 at the beginning of 1977 to 14,327 at the start of this year, according to Diebold Deutschland GmbH statistics. The 1978 total represents a value of $1.27 billion. □

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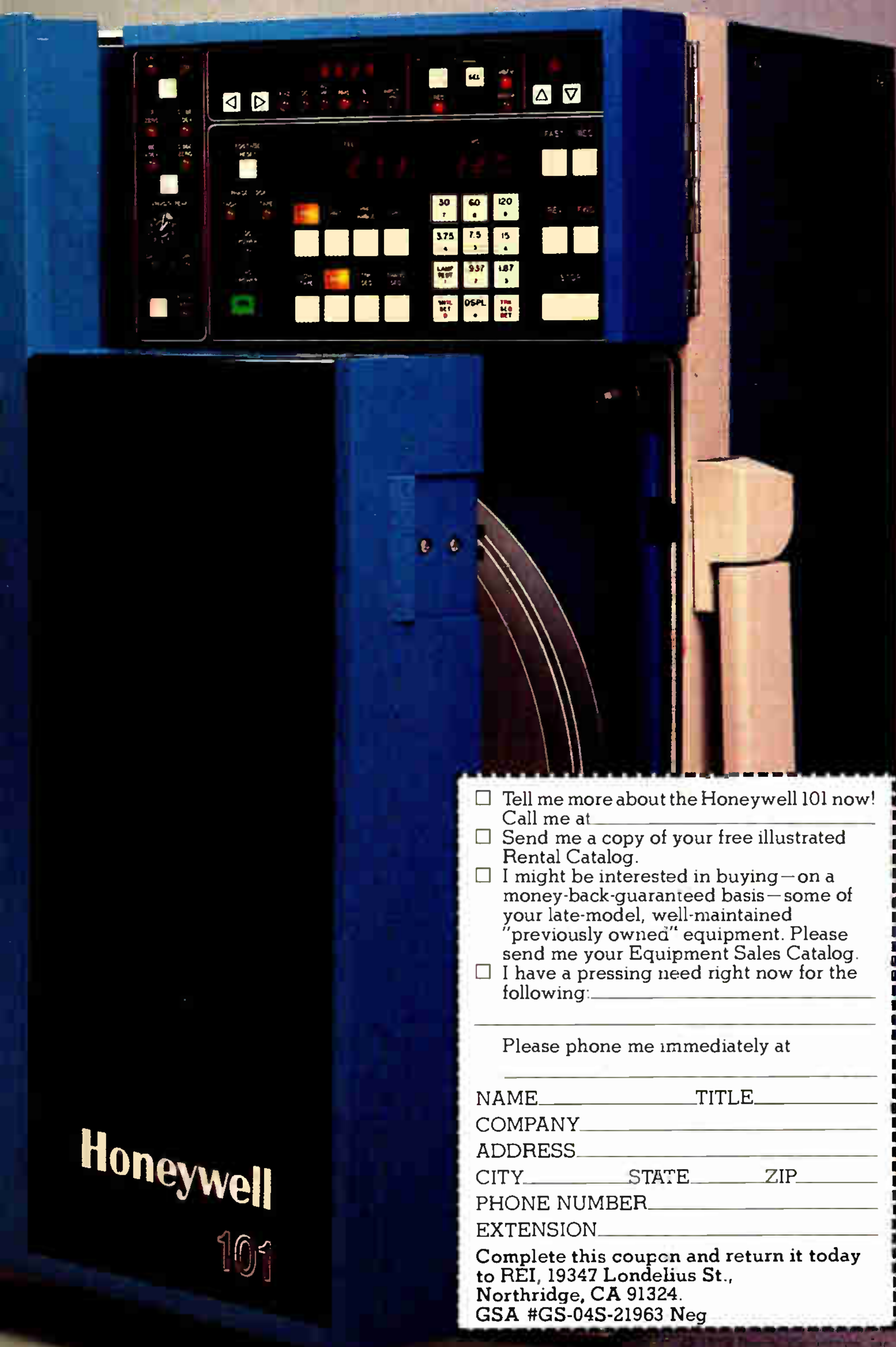

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Note rough, jagged edges always present.

Your IC lead frames look like this at 30X enlargement (unretouched). Because they are punched out of metal, the edges are rough, jagged and irregular. In contrast, the flat sides of the lead frame are smooth, even and perfectly plated.

Arrows indicate scars and abrasions made by rough edge of lead frame.

THEIRS

An ordinary edge-bearing socket contact after 5 insertions of DIP lead frame. Contact has been spread apart to show inside faces of contact. Notice how the contact has scars and abrasions from *rough, irregular edge of IC lead frame.* Electrical contact is degraded and resistance is increased. Reliability is obviously reduced.

Lead frame in place in an ordinary edge-bearing contact.

Arrows indicate contact surface still smooth, clean, free from abrasions.

OURS

ROBINSON-NUGENT "side-wipe" socket contact after 5 insertions of DIP lead frame. Contact has been spread apart to show inside faces of contact. See how the RN contact—because it mates with the *smooth, flat side of the IC lead frame*—retains its surface integrity. This 100% greater lead frame contact results in continued high reliability.

Lead frame in place in RN "side-wipe" contact.

expose 'junk' socket problems

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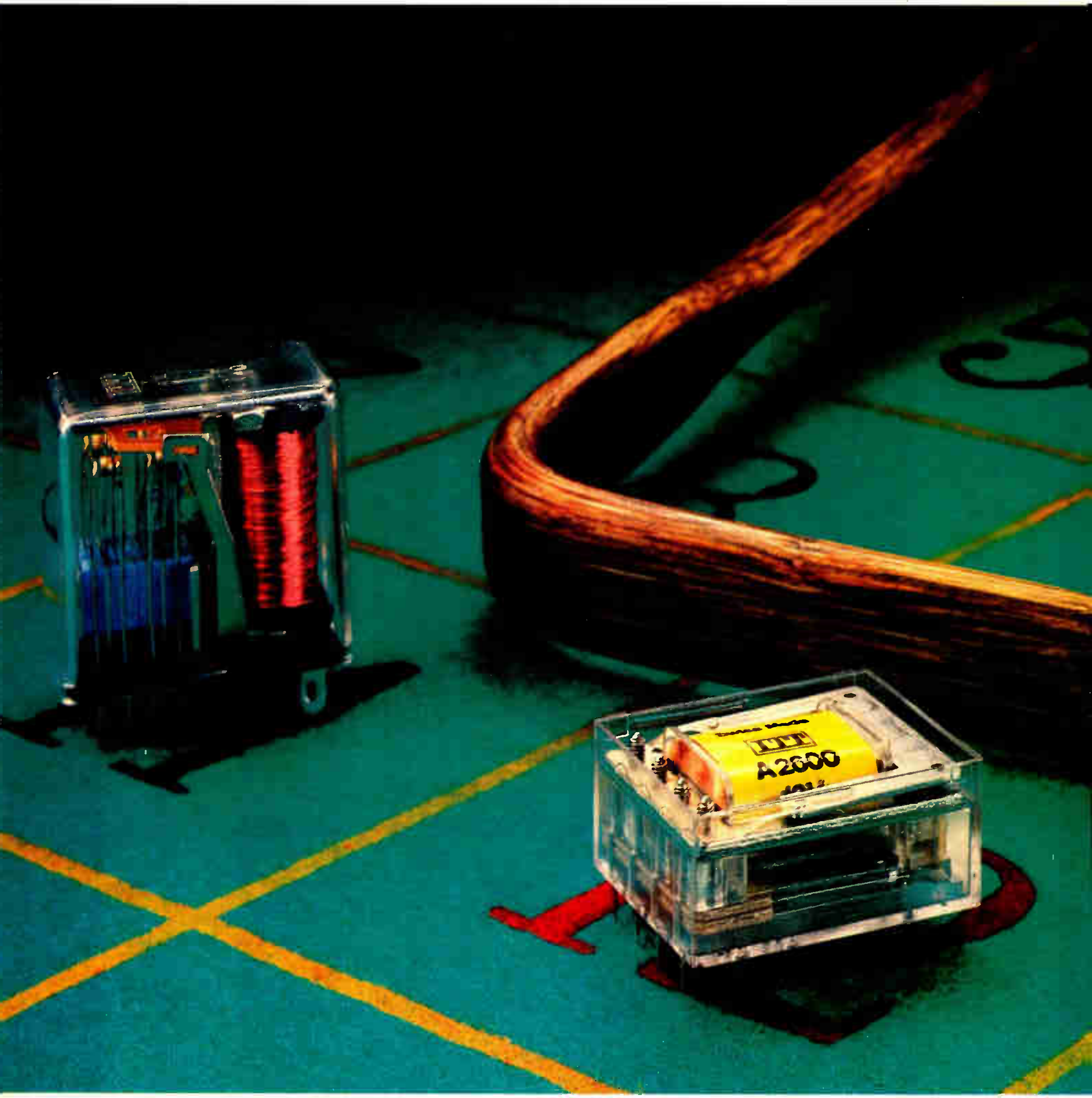

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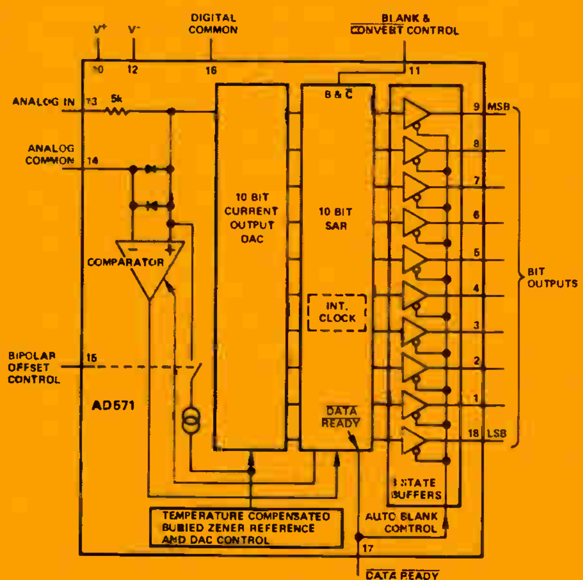

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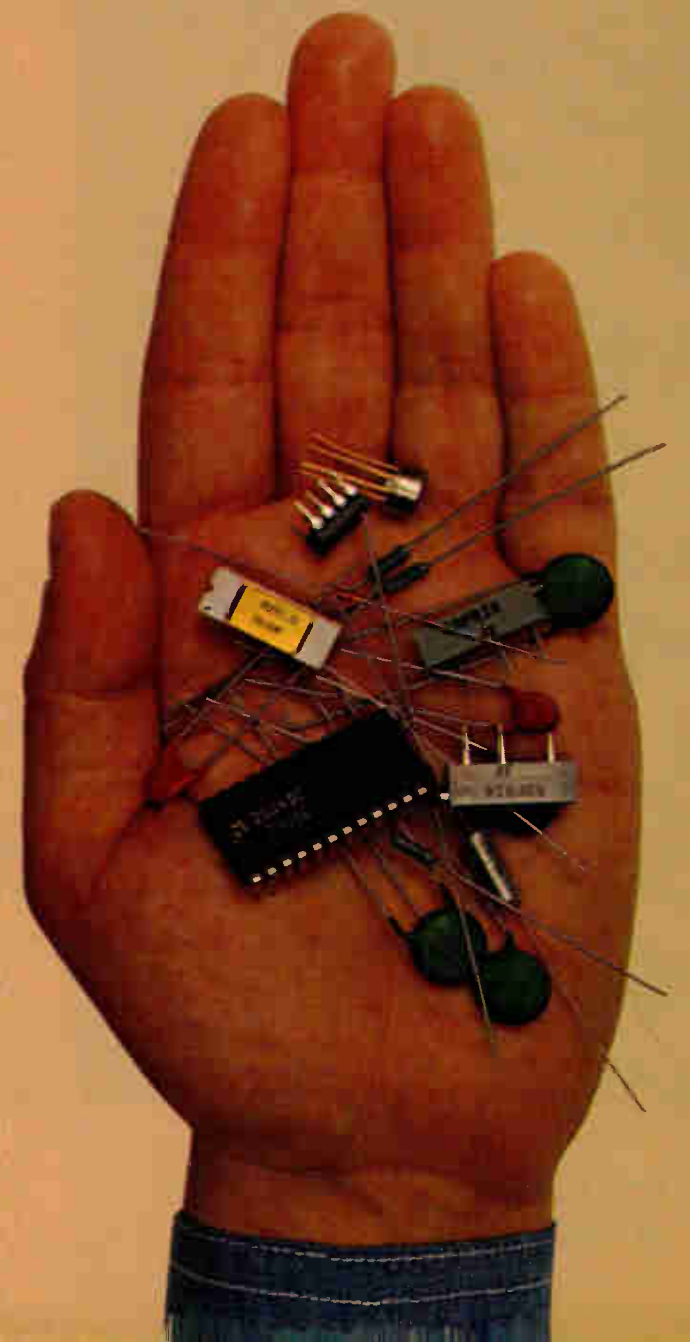
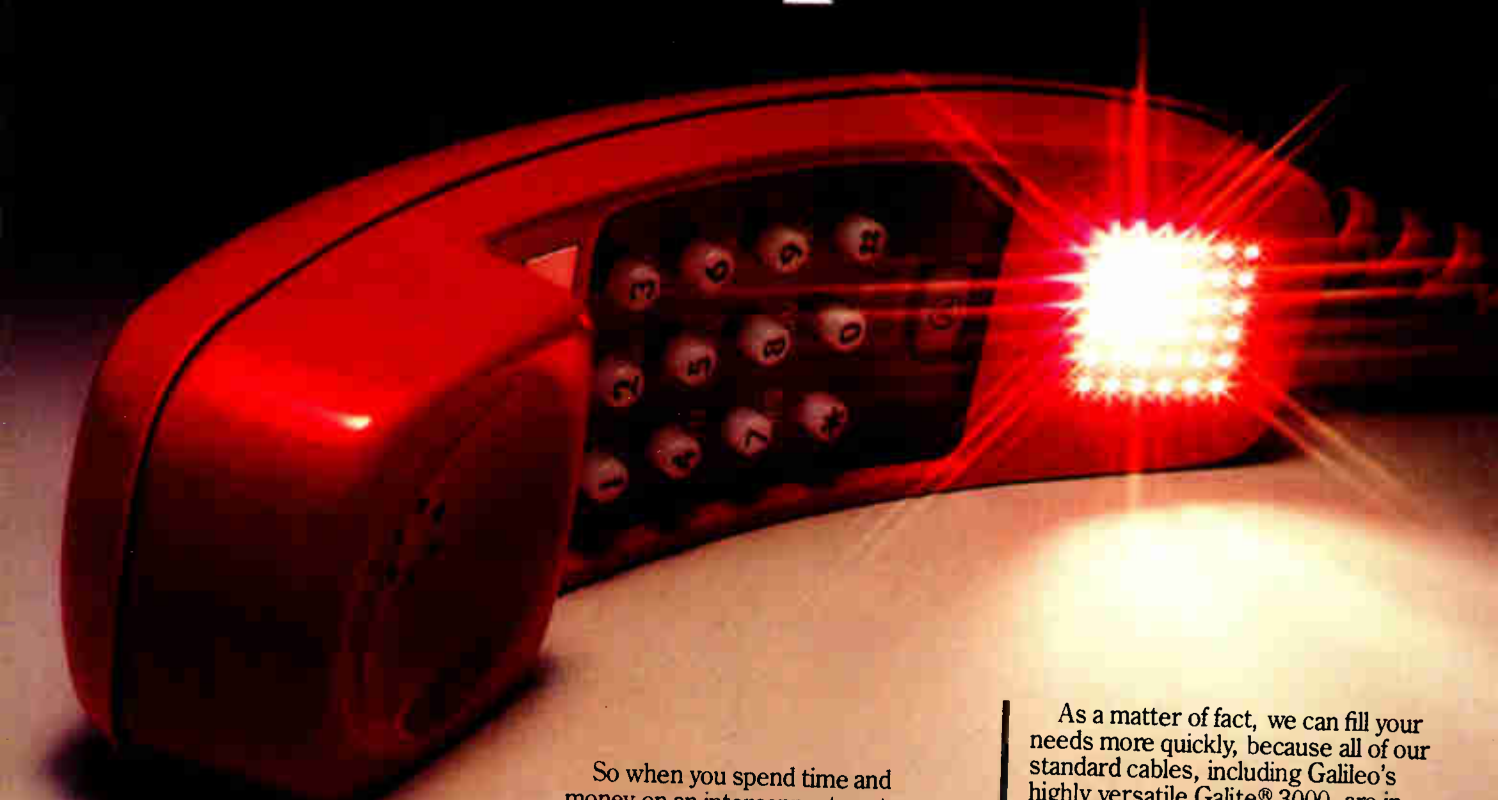


How do you see fiber optics?



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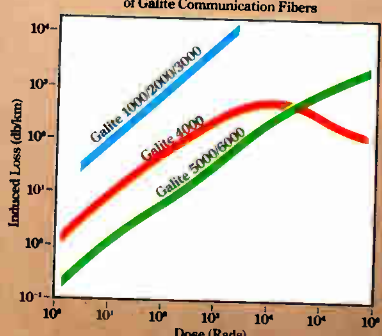

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Trade groups thrive in California

Four major associations have headquarters in Golden State providing services ranging from lobbying to credit union

by William F. Arnold, San Francisco regional bureau manager

Besides hosting the Wescon show, California helps the electronics industries present another important face to the world. The Golden State is home base for four major industry trade associations: the American Electronics Association, the Electronics Association of California, the Semiconductor Equipment and Materials Institute Inc., and the Semiconductor Industry Association.

Not surprisingly, these groups embrace companies as diverse as the state's electronics industries themselves. But together they perform such needed industry services as lobbying on Government policy and legislative matters, educating members about new trends, holding executive seminars, formulating standards, running trade shows, managing training courses for production-line supervisors, gathering statistics, and even providing a social milieu at dinner meetings so that members can informally discuss vital issues of the day. In other words, they provide industrywide services that many individual companies cannot provide for themselves.

Lobbying. For example, the AEA (originally the West Coast Electronic Manufacturers Association, then Wema until earlier this year) is generally credited with being a major force in the current drive in Congress to lower the capital gains tax so that more venture capital would be available to fledging high-technology companies [*Electronics*, March 30, p. 76]. The AEA also has been part of a four-year fight to bring efficiency into customs processing and fairness into adjudication of any disputes between companies and the Customs Service (see related story on p. 45).

Moreover, the AEA plans to carry its political activity a step further this year: it will actually support congressional candidates across the country. The group has formed an electoral political action committee that will contribute a total of $5,000 to candidates, irrespective of party, who support AEA policies.

Successful. The young EAC, on the other hand, provides three employee services that its members, mostly small companies, cannot offer but feel they must have in the highly competitive Silicon Valley labor market: a credit union, health insurance, and training classes for supervisory personnel. It is becoming so successful that the association plans to open offices in southern California in addition to its Sunnyvale headquarters and is getting inquiries

Executives. Directing day-to-day activities of three of the four electronics trade associations that are based in California are, left to right, James J. Conway of the EAC, Thomas D. Hinkelman of the SIA, and E. E. (Ed) Ferrey of the AEA.

from other states about setting up their own equivalents.

SEMI, a traditional vertical trade association, began by running trade shows so that its members might have a place to exhibit the products they sell to the semiconductor industry. Significantly, SEMI is now also busy writing standards for those products. And the SIA, as its name implies, is an association of chipmakers formed to influence Government trade policy with Japan that also collates statistics on the semiconductor market.

Counting its 1,000th company member this month, the AEA goes back to 1943, when 12 Los Angeles and 13 Bay Area companies formed the West Coast Electronic Manufacturers Association. The transistor had not been invented then, and what was to become Silicon Valley was hardly more than Hewlett-Packard Co. and Varian Associates nestled among the orchards around Stanford University in Palo Alto. Today, with headquarters in Palo Alto, the AEA has offices in Los Angeles, Boston, and, according to its energetic president, E. E. (Ed) Ferrey, is looking to open a full-time Washington, D. C., office.

As the largest trade association serving the electronics and information technology industries, the AEA has 40 out of the 50 biggest electronics companies as members, Ferrey says. But to criticism that it caters to big companies, Ferrey answers that 60% of the members have fewer than 200 employees. In fact, the 1,000th member is Tencor Instruments Inc., Mountain View, Calif., with only 30 employees, he says.

Education. Having severed its connection with Wescon in 1974 because only a small percentage of its members were participating, the AEA, besides lobbying, carries on "an extensive educational activity." This translates into seminars. The AEA holds many of them a year, from half-day briefings on new trends to two-week institutes at universities. Among its 60 to 80 "how-to" seminars are sessions on technology update, high-technology selling, mergers and acquisitions, and effective sales management.

For small companies, the association has luncheons, forums, and councils, where chief executive officers or other administrators can get together to discuss common concerns. It also provides training for first- and second-line supervisors.

There has been some criticism, however, that the AEA has been slow to respond to small companies' needs in such matters as credit unions and health plans. Ferrey says that the association is planning to offer a credit union and is investigating several options. A group health plan is coming up, too, in addition to the worker's compensation plan started late last year, he says.

Meanwhile, the Electronics Association of California has got off to a quick start by zeroing in on the needs of small- and medium-size companies. "We've targeted three main service areas," declares James J. Conway, president. First is "to provide fringe benefits compatible with those of larger companies"; second is to help small companies train employees, which is generally difficult for them; and third, to "collectively leverage the strength of their combined buying power." For example, in insurance, small companies pay from 20% to 25% higher rates than what they pay typically with EAC, he says.

Shows. SEMI was started because makers of semiconductor equipment felt the need for a place to display their handiwork. By 1980 it will be offering four shows a year: Semicon West, in San Mateo, Calif., Semicon East in Boston, Semicon Japan in Tokyo, and Semicon Europa in Zurich. In addition, senior vice president James E. Gallagher says, it has a large program on standards in which it works with users on such issues as wafer sizes, wafer thickness, and the like. It also has four dinner meetings a year to cover forecasts and trends, as well as an active export control committee.

Gallagher agrees that "there's

LOOKING AT THE WESTERN ASSOCIATIONS

	Founded	Member companies	Associate or individual members	Membership requirements	Annual company dues
American Electronics Association 2600 El Camino Real Palo Alto, Calif. 94306	1943	1,000	206	produce components, subassemblies equipment, or systems that employ principles of electronics or information technology in performing major functions, including software, R & D, and supplying parts or equipment for such production	$200 to $7,000, depending on previous year's income (increase will be proposed at September board meeting)
Electronics Association of California 795 Kifer Rd. Sunnyvale, Calif. 94086	1976	197	11	be in "electronics industry"	$350 to $2,000, depending on number of employees
Semiconductor Industry Association 20380 Town Center Lane, Suite 155 Cupertino, Calif. 95014	1977	33	18	be a semiconductor manufacturer	$1,000 for small company with under $10 million in sales
Semiconductor Equipment and Materials Institute Inc. 625 Ellis St. Mountain View, Calif. 94043	1970	250	250	supply or make equipment or materials for semiconductor industry	$350 the first year, then $200

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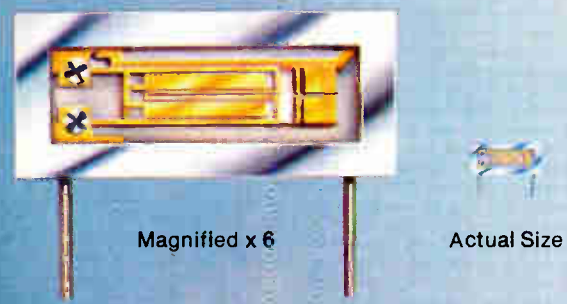

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Probing the news

Equipment makers. James E. Gallagher is senior vice president of SEMI.

overlap among SIA, AEA, and SEMI. All have night programs, for example, in which the audience and the speakers are similar. Some one of us has to start thinking about this." But unlike the other three, SEMI is an international association with more than 10% of its members from overseas. Overall, it would like to have 450 members within two years. 'We're looking at a quantum step upward in growth," he says.

Meeting a threat. SIA began in April 1977 "primarily due to a concern over a threat to the semiconductor industry by the Japanese and other foreign competitive concerns," declares Thomas D. Hinkelman, executive director. Mostek and RCA have since joined the original board of Advanced Micro Devices, Fairchild Camera & Instrument, Intel, Motorola Semiconductor, and National Semiconductor.

Besides the trade policy program, SIA collates a statistical service on shipments and bookings for its members. Subject to board approval, it also is about to start a series of educational seminars for semiconductor engineers on such topics as ion implantation. It plans to videotape the seminars and make the tapes available to member companies that cannot send employees. The association also holds four dinner meetings a year, Hinkelman says. Lastly, the organization is "getting involved with regulatory agencies on specific programs." ☐

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Avionics

Europe's watchword: together

Missiles, satellites, and warplanes on display at Britain's Farnborough air show illustrate success of consortium concept

by Kevin Smith, London bureau manager

Europe's fragmented national aerospace industries are welding themselves into units capable of competing evenly with dominating American rivals. Evidence of that will be thick on the ground and in the air above Farnborough as the International Aerospace Exhibition gets under way on Sept. 3 for its biennial one-week stand.

The swing-wing Tornado multirole combat aircraft, as it blasts spectators' eardrums and twists and gyrates in the sky, will provide the best demonstration yet that collaboration can work. It was developed jointly by West Germany, Great Britain, and Italy. Up there too will be the Anglo-French Jaguar tactical-strike fighter, the first collaborative project to enter military service.

In the civil field, the Franco-West German 250-seat A-300 Airbus now looks like a winner. The first American orders from Eastern Airlines are in and total orders are closing in on the 100 mark. Flushed with a financial success that eluded the ill-fated Anglo-French Concorde, the Airbus industry consortium is now planning to build a smaller sister to the A-300 B-2 and B-4 versions now in service. Designated the B-10, the new craft will be a 200-seat short-to-medium-haul liner.

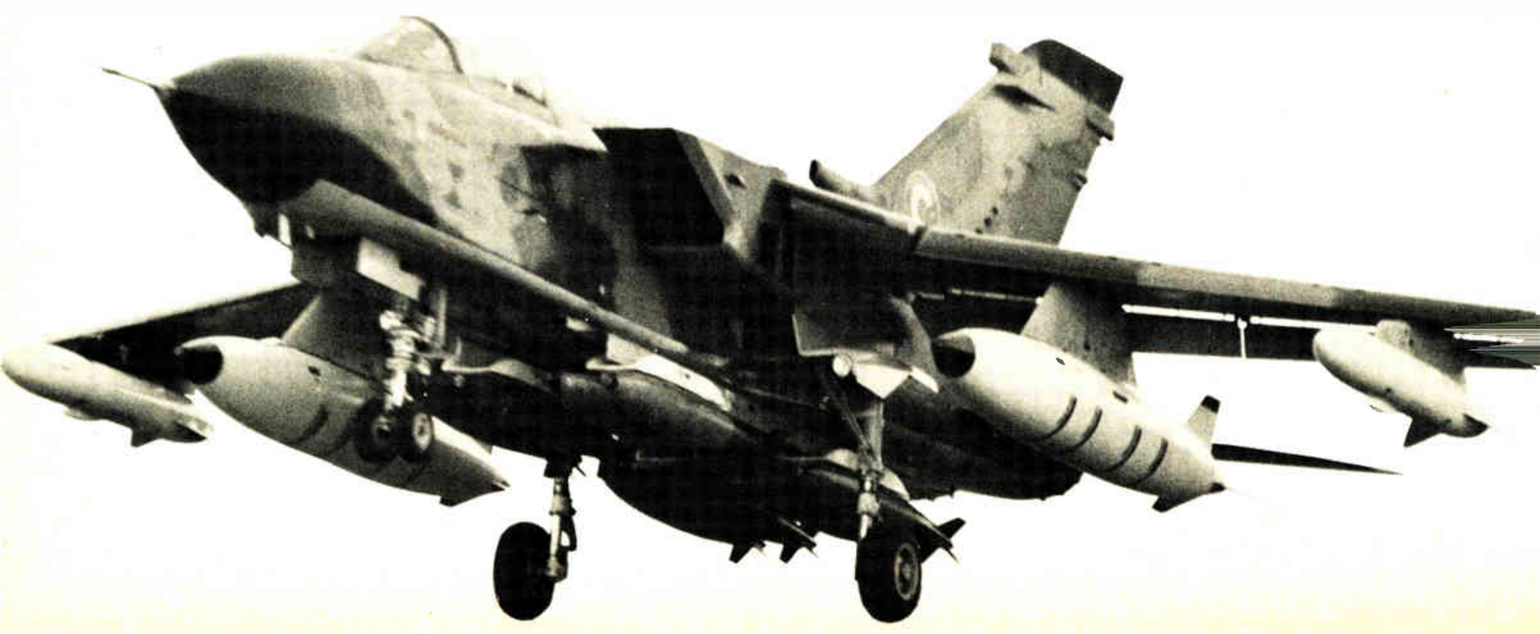
The list of collaborations in missile systems is also growing. There are the Franco-German HOT helicopter-borne antitank gun weapon, the European consortium to manufacture the U. S. AIM-9L sidewinder missile, and the new P3T antiship sea-skimming missile that is to be developed by Britain and France. Nor is space being neglected: two European consortiums put into space in 1978 the GEOS 2 scientific satellite and the OTS 2, Europe's first communications satellite.

Strains. But all is not blue skies. The tightly stretched pan-European image could soon be rent as Britain's Eric Varley, secretary of state for industry, agonizes over a choice of partner for British Aerospace and Rolls Royce Ltd., both nationalized companies. On the table before him is a proposal from Boeing Co., the world's largest plane maker, for collaboration on the 757A 160-to-180-seat short-to-medium-haul liner that would be a direct competitor to the new B-10 and would be powered by Rolls Royce engines.

Also, West Germany and France are pressing Britain to play the good European and rejoin the Airbus program that it left several years ago. In fact, the Hawker Siddeley Group, now part of British Aerospace, is already building the wing sets for the present version. But what additional sweeteners France and Germany are prepared to offer is none too clear.

Meanwhile, British avionics manufacturers standing on the sidelines fear they will be left out. "Unless you are in on a program, you don't get any improvement in the technology," comments Malcom Moulton of Marconi Avionics Ltd. That's why the Tornado has played such a big role for British and other European

All for one. Tornado multirole combat fighter is result of cooperative effort of British, West German, and Italian aircraft industries.



manufacturers of avionic gear.

"For the first time," says D. M. McCullum, director and general manager of Ferranti's Edinburgh Avionics Systems group, "we have had production runs comparable with U. S. production lines." It is supplying, among other systems for the Toronado, the cockpit display, a combined moving-map display with superimposed radar for the navigator, a moving-map display for the pilot, and the terrain-following radar that is being assembled under license from Texas Instruments Inc.

Another company, Marconi Avionics, will be supplying some 16 modules, among which will be a smart radar for the Royal Air Force's air-defense variant of the Tornado. With an eventual production run of 809 aircraft at $14 million apiece and with avionics systems accounting for one third of the cost, that is lucrative business.

Spin-offs. But possibly more important is the spin-off business. Ferranti, for example, picked up a $4.5 million contract to fit its advanced moving-map display system to the McDonnell Douglas A-18 strike fighter. Also, the company has closed an agreement with Honeywell Inc. to market its military laser systems jointly in the U. S.

Heads-up displays have also brought in fat export contracts for suppliers like Smiths Industries Ltd. and Marconi Avionics. Marconi is supplying the heads-up gunsight for the General Dynamics YF-16 lightweight fighter. This figured in the so-called sale-of-the-century contest against the French Mirage to re-equip the Norwegian, Dutch, Belgian, and Danish air forces.

The prevailing mood is indicated by Ferranti's McCullum, who feels "very bullish about the prospects." But whether or not this mood of optimism is reflected in improved earnings in the radio, radar, and electronic capital goods sector remains to be seen. For example, according to a recent National Economic Development Office report, there was a decline in the proportion of British exports from 90% in 1970 to 75% in 1975; during the corresponding period Britain's share of world trade fell from 12.6% to 9.7%. □

Minicomputers

It's a new ballgame in minis at TI

Semiconductor giant signals it's in minicomputers to stay with new compatible family, software, and upgraded systems group

by Anthony Durniak, Computers Editor

Texas Instruments Inc. is in the minicomputer business to stay. Although manufacturing minicomputers since 1968, the semiconductor leader has not generally been viewed as a serious contender with long-term prospects. It has had an incompatible product line and software support that lagged behind the rest of the industry.

Now, with its 990 family of compatible computers established, the first fruits of an extensive software-development effort on the market, and the elevation of its Digital Systems division to group status, TI is looked at more seriously.

The most recent evidence of the increased effort was the reduction of memory prices and the introduction of a data-base management system for the 990 family in June, along with the unveiling of five new models of its Series 700 intelligent terminal family. Moreover, as part of its more aggressive marketing stance, it last month improved the discount schedule and pass-through warranties it offered to original equipment manufacturers, systems houses, and large end users.

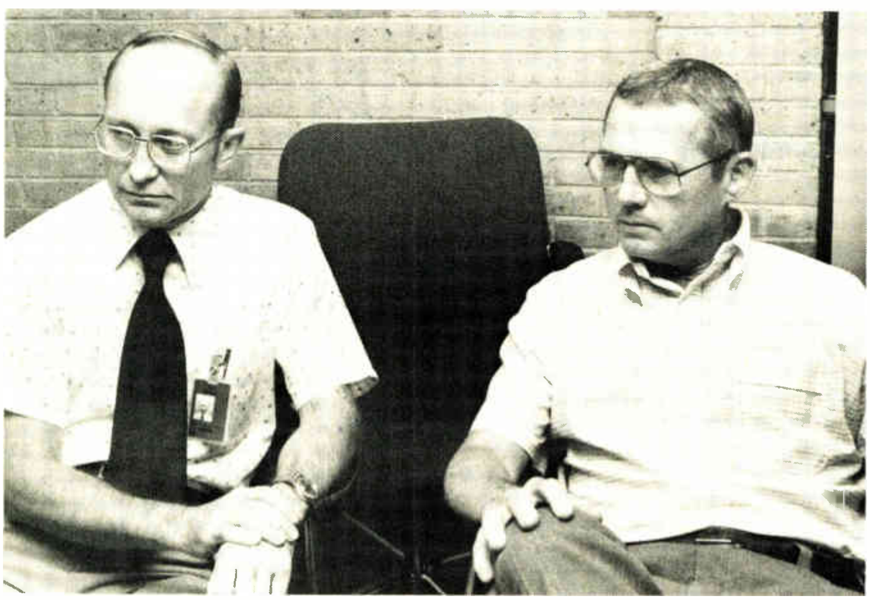
In fact, chairman Mark Shepherd Jr. and president J. Fred Bucy are saying that TI is counting on distributed-computing hardware, along with consumer and semiconductor products, to lead the Dallas corporation in its effort to reach $10 billion in revenue by 1980.

Ranks seventh. TI will not break out the numbers, but minicomputers are estimated to have contributed $80 million to the corporation's $2.046 billion in 1977 revenues, according to International Data Corp. of Waltham, Mass. Based on that estimate, the market-study firm ranks the Dallas-based company as the seventh largest U. S. minicomputer maker. Securities analyst Charles T. Casale, with Bache Halsey Stuart Shields Inc.'s Boston-based technology group, estimated TI sold another $70 million of its Silent 700 terminal products, bringing the Digital Systems group to about $150 million—enough to rank it as fourth largest.

"We've had good success in distributed processing and have grown faster than the market has," says Sam K. Smith, Digital Systems group vice-president and general manager. He will not specify, however, how much faster than the market's estimated 35% to 40% growth rate. Nor will he comment on the revenue estimates.

What puzzles industry observers is how TI achieved such volume in spite of the incompatibility of its 960 transaction-oriented Cobol processor and the 980 real-time-oriented computer aimed at scientific applications, plus the lack of software and a marketing effort aimed primarily at customized turnkey installations. TI officials themselves explain it only by saying its products are good.

Company insiders concede, in the words of one, that the company "didn't know what compatibility was" and realized a new product line was necessary if the computer effort was to grow. The result was the upwardly compatible 990 computer line, which ranges from the TMS9900 microprocessor and the 990/4 microcomputer based on it, to the 990/10, a Schottky transistor-transistor-logic minicomputer with a cycle time of 250 nanoseconds that



Compatible. TI's Digital Systems group marketing manager Doss Dunlop, left, and group manager Sam Smith say compatibility is the watchword in minicomputer efforts.

can address up to two megabytes of metal-oxide-semiconductor memory. From now on, Smith says, "our intention is to maintain compatibility." Eventually, compatibility will be brought to the older products, says Carl Jack, national marketing manager for computers. "A bridge is being built between the transaction-oriented 960 and the 990," he says.

As for software, John Hanne, manager of 990 product development, points with pride to the DX10 multitasking operating system he helped design. He notes that in addition to the Cobol and Fortran programming languages previously offered, TI now markets Basic, RPG II, and Pascal.

Onward. W. Joe Watson, manager of the Computer Systems division, the Austin operation that builds the minicomputers, agrees that many of the new products plug holes. Now, he says, "we've got a strong foundation in processors and key peripherals and we're putting the software in place. With our language offerings we don't have to stand in second place to anybody."

In addition to expanding its product line and software offerings, TI has targeted its marketing aims on standard systems packages to large end-users and OEMs with industrial and commercial data processing applications. "The commercial and industrial markets will be the two largest slices," says vice president and group marketing manager Doss D. Dunlop. "With the 990, our goal is to have less than 5% specializing on a system."

What's in store for the future? Dunlop says the company intends to draw on the distributed processing and network experience gained from its four-year-old internal international packet-switched data communications network. It ties together some 3,000 terminals and most of the 3,000 computers used within TI.

Although Dunlop will not say exactly when TI will unveil a network architecture for the distributed-processing marketplace, he reports "we'll do it." Smith adds that the company's semiconductor operations "should give us an advantage because we'll see the new technologies first and have an opportunity to plan products around them." □

Computers

Heat rises over interface standards

Hearing on I/O norms for computers purchased by U. S. highlights split between mainframers and peripheral makers

by Ray Connolly, Washington bureau manager

The heat is on at the National Bureau of Standards, and it will get hotter as the Commerce Department agency pushes for adoption of its first meaningful Federal Information Processing Standards, known as FIPS.

The heat is a product of friction between FIPS advocates and their activist opponents. The former include congressional leaders who mandated NBS standards development 13 years ago and are still waiting, as well as most Federal computer users and makers of plug-compatible peripherals who would benefit from adoption of the NBS standard. The standards would be derived from technology developed by International Business Machines Corp. Opposition to FIPS includes most mainframe manufacturers and their powerful lobby, the Computer and Business Equipment Manufacturers Association.

Compatibility. The FIPS at issue are three related channel-level input/output interfaces intended to achieve operational compatibility between large and medium mainframes and associated peripherals bought by the Government. Functionally, the interfaces determine the amount of data that can pass at any one time between a peripheral device such as a disk or tape drive and the data channel—the dedicated computer that handles I/O requests for the mainframe. Implicit in the interface are hardware constraints such as the width and speed of the data path, and hence the type of cabling and electronics needed. In addition, the operating system software of the mainframe must also conform to the interface's requirements for command and data formatting as well as timing.

The proposed interfaces are based on ones used by the IBM System/360 and 370 computers—and there lies the rub. The other mainframe manufacturers and CBEMA claim that the interface's hardware and software are too closely related to the machine's overall architecture to be standardized.

Honeywell Information Systems Inc., Minneapolis, adds that the standard—based on techniques devised in the 1960s—are technically obsolete. Specifically, Irma Wyman, Honeywell's director of central staff, says that "Honeywell's use of bidirectional data transmission paths reduces the number of components in its interface in comparison with the proposed standard."

Digital Equipment Corp.'s Patricia White, standards manager, stresses the inability of the FIPS to accommodate changing technology. The I/O standard channel, the Maynard, Mass., company believes, is "inadequate" for faster disks and nonrotating memories like solid-state and magnetic bubble hardware.

"The nature of a parallel interface, the timing, and the states at both the channel and controller are such that the total number of states is unworkably large," White argues.

Honeywell weighs court action

Honeywell Information Systems Inc. is preparing for the role of plaintiff against the National Bureau of Standards and its parent Commerce Department if push comes to shove over adoption of Federal Information Processing Standards for input/output interfaces on all computers purchased by the Federal Government.

But Honeywell will take court action, insiders say, only "if all other avenues are closed." Those avenues are expected to be crowded in coming months with lobbyists from Honeywell and other big computer systems houses beating their way to the doors of Commerce Secretary Juanita Kreps, who must sign any standards, a sensitive Congress standing for reelection, and even the President.

Honeywell, ranked fourth among Federal computer vendors and rising, has already threatened to withdraw from bidding on procurements if the proposed standards are invoked. The FIPS at issue use IBM technology that Honeywell and others claim is archaic. HIS vice president Stephen Jerritts speaks sharply of standards that would "require fundamental changes in our systems architecture and require massive changes in our software. And to what end? So that we may move backward to a technology bypassed years ago by innovative manufacturers? So that we may copy a prime competitor's older specifications?" The price of compliance "for our large-scale product lines only," says Honeywell standards chief Irma Wyman, would be $12.5 million in hardware costs alone and take two to four years. In that period, Wyman contends, evolving technology will make the standards obsolete, leaving Honeywell with what it characterizes as "zero return on investment" for compliance.

"It is hard to believe that any specification can cover them all adequately." The future for DEC and the computer industry, she says, lies in "serial message-oriented interconnections" that are "more reliable, are truly specifiable and provide more freedom in equipment location," citing fiber optics as a prime example.

Joining in the 6-to-3 testimony against plug compatibility in mid-August hearings were Burroughs Corp. and Control Data Corp. On the other hand, Hewlett-Packard Co., most of whose Federal computer sales would be exempt from the FIPS exclusion of systems priced under $400,000, took an essentially neutral stance. HP vice president Donald Loughry urged raising the minimum price of systems excluded from FIPS to $500,000 and postponement of any effective date.

On the other hand, manufacturers who already market IBM-plug–compatible equipment support the interface, since they are already using it.

Gene Amdahl, now chairman of IBM-compatible computer maker Amdahl Corp., Sunnyvale Calif., was the chief architect of the IBM 360 and its interface. He disagrees that the interface is obsolete or technologically limiting. Future architectures, he says, "are in no way impeded and in fact are simplified by the channel interface."

Also favoring FIPS was the Computer and Communications Industry Association and Norman J. Ream, who was director of the NBS computer institute when standards were first called for by Congress in 1965.

Remarkable by their absence from the hearings were IBM and Sperry Univac Corp., another major Federal contractor, whose spokesman later said that "the proposed standards don't pose any big problems for us. If FIPS is what the Government wants, that is what they'll get."

Univac's apparent indifference was in sharp contrast to the attitude of Honeywell, which threatened to "withdraw completely from the Federal marketplace" if the FIPS rules become mandatory.

Opening the gates? George Bardos, vice president for market development at Control Data Corp., Minneapolis, made the forceful claim that FIPS proposals are "a national standard in Japan" that would open the floodgates to Japanese computer exports to the U. S., an argument also advanced by CBEMA and other components. "We feel that some of these independent peripheral manufacturers have taken a short-sighted view and may be sowing the seeds of their own destruction," said Bardos of FIPS advocates.

DEC's Patricia White also sees the standards giving leading Japanese computer makers "a built-in cost advantage in competing with U. S. business," since they "have already adopted this architecture" to produce IBM-plug–compatible hardware. CBEMA president Vico E. Henriques, too, raises the specter of a Japanese invasion and possible takeover of the American computer market if channel-level interfaces become standard. "The potential impact of the FIPS on innovation, competition, foreign trade, and jobs is negative and contradictory to the Government's responsibility to the nation," he insists.

Estimate. The reason for FIPS in the first place is to increase competition for Federal data-processing procurement bids and also to save the Government the expense of maintaining incompatible equipment. The NBS Institute of Computer Sciences and Technology conservatively estimates that approval of the standards next year could cut Federal computer outlays by nearly $56 million over five years.

The 13-year-old battle may finally be reaching its conclusion. Pros and cons will continue to be heard until Sept. 30, when the record on written comments and rebuttal closes. NBS's analysis and recommendation should take a month to reach its parent Department of Commerce, which is expected to act on the proposal within 60 days.

Publication of a FIPS interface could thus become a reality by early next year, with its implementation occurring four months later. But lobbyists have never been known for agreeable attitudes and the sharp divisions on this issue suggest that it may be a long while before FIPS is anything more than a gleam in the Government's eye. □

You and your career

They're off and running at the IEEE

Major issues are repeats, but Feerst-Suran contest for top spot is generating an uncharacteristic gloves-off battle

by Bruce LeBoss, New York bureau manager

There are fewer candidates, but this year's election campaign for the leadership of the Institute of Electrical and Electronics Engineers is no less a slugfest than contests of recent years. In fact, as election ballots were being mailed this week, the battle for the IEEE's presidency has heated up to the point where the issues raised and charges traded might actually widen the gap in a membership that already is quite severely split.

That the presidential campaign bears a striking resemblance to those of recent years is not surprising: neither the issues nor the slate of candidates has changed all that much. Major issues continue to center around the priorities and management of the 180,000-member organization's technical and professional activities.

The contest pits perennial petition candidate Irwin Feerst, an independent consulting engineer making his fourth consecutive bid for the IEEE's top spot, against Jerome J. Suran, manager of General Electric Co.'s Electronics Laboratory in Syracuse, N. Y. and currently IEEE's vice president of educational activities. Suran was nominated by the institute's board of directors, as was Leo Young, staff consultant to the Electronics Technology division of the U. S. Naval Research Laboratory in Washington, D. C., who is running uncontested for the post of executive vice president.

In at least one sense, this year's campaign is unlike those of prior years when Feerst set the pattern of a tough campaign and the board's nominee chose either to ignore him or to maintain a decorous appearance. Suran, who Feerst calls "a clone" who "promulgates the policies of the existing board," now appears to be taking the gloves off and fighting back. He seems to feel the tactic is necessary if he is to keep Feerst from the IEEE presidency, a seat the reformer almost won last year when he received nearly 44% of the vote.

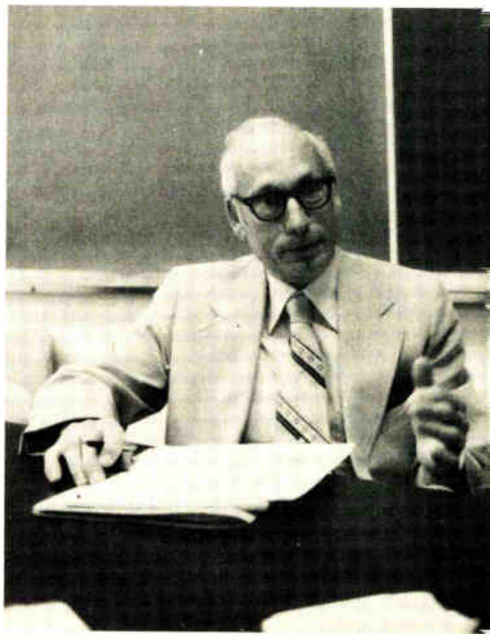
According to Feerst, a key issue "is the necessity to revive professional activities in accordance with the IEEE's constitution." He believes "there is a subtle push by the board to prevent involvement in professional activities and to divert the IEEE toward industrial lobby efforts." The United States Activities Board, Feerst says, is spending some of its limited resources to function as an industry lobby. By doing this, he says, the IEEE "denudes itself in other areas, such as pensions, anti-wage-busting, and the problems of age bias and alien engineers."

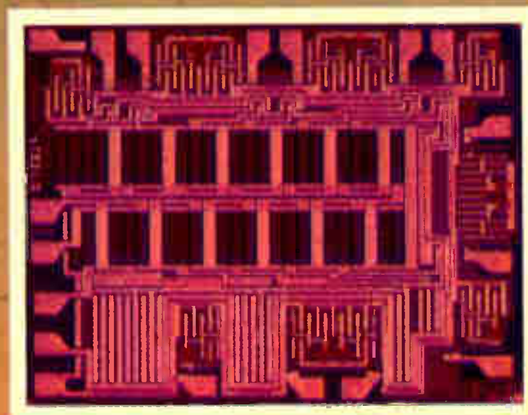
One of the key issues, as Suran sees it, is matters related to the individual status of IEEE members, basically job security both in keeping and seeking jobs. "The first prerequisite of job security is the existence of jobs themselves," he says. Thus, Suran believes the institute should "lobby very strongly with decision makers [the Congress and others involved in determining how national problems are to be handled] and opinion molders [the press and other media] to show how engineers can contribute toward solving the nation's problems." If they could be convinced about the utility of engineering, he adds "I think there would be a surplus of jobs and not a surplus of engineers."

Best known for his pioneering work in transistors and transistor circuits and for developing the first implantable cardiac pacemaker (a feat for which he received an honorary doctor of engineering degree

Challenger. Irwin Feerst, perennial petition candidate who last year won 44% of the vote, again seeks presidency of the IEEE.

Board nominee. Jerome J. Suran was nominated by the board to run for the IEEE's top spot. He manages GE's Electronics Lab.





from Syracuse University in 1976), Suran feels strongly about other issues related to job security for the working engineer. He believes USAB's decision to seek anti-wage-busting laws by pushing for them on two fronts—the legislative and the administrative—"probably is the most effective and fastest way of getting action in this area."

On the matter of pensions for those engineers in the aerospace business who are dependent upon Government contracts and who have not built up vested rights in their companies' pension plans, Suran says he will battle for IEEE action. He wants to take to Congress a proposal that engineers who work for companies that do have pension plans "be allowed to establish their own independent retirement accounts, until such time as they get vested in the plan." Then, the engineer's individual account would be transferred into the company plan with the firm making whatever payments it would have from time zero.

The 52-year-old Suran says that he feels equally strongly about age bias and that the IEEE must take a stand on this. He believes certain studies showing "it is a myth to correlate age with technical obsolescence" ought to be publicized to "overcome some of the attitudes that may exist in some parts of the industry." However, "it is also time to stop stereotyping all industry as being guilty of age discrimination."

Whatever happened to the GGG?

The Good Government Group, that blue-ribbon panel of top industry executives and academics that last year turned the election into a free-for-all as it sought to provide new direction to the IEEE's professional activities [*Electronics*, Aug. 4, 1977, p. 70], has been rather quiet in this year's election.

"The GGG is low-profiling it this year, because everything is going its way internally," says Robert A. Rivers, president of Aircom Inc. and leader of the IEEE's manpower task force. First, GGG-supported candidate C. Lester Hogan, vice chairman of Fairchild Camera and Instrument Corp., was elected the IEEE executive vice president last fall. Secondly, Bruno O. Weinschel, president of Weinschel Engineering Co., was appointed head of the United States Activities Board. A member of the committee that opposed the GGG, Rivers adds, "Bruno is doing a good job for it [the GGG], namely, molding all of USAB's activities to stress industry-oriented interests."

F. Karl Willenbrock, secretary of the GGG and dean of Southern Methodist University's School of Engineering, sees it a little differently. "We feel a lot of progress has been made as a result of last year's elections. Also, this year's nominations by the board are both good ones, and there is no need for a petition candidate. Those nominated this year have a good grasp of the IEEE's technical functions, as well as others, and are not apt to be overcompensating in one direction." □

The 50-year-old Feerst believes still stronger actions should be taken. "It is time for IEEE to serve as a public defender," he says, adding that when the "legitimate goals of a professional EE are impeded by the actions of an unethical employer, it is time for IEEE to do something about it." For example, Feerst accuses Emerson Electric Corp. of St. Louis, of "circumventing American law" by recruiting EEs in Great Britain for jobs in the U. S. and also of specifying an age bracket for applicants. Although Emerson officials responded to Feerst by saying they are also recruiting in the U. S., he says, "It should be a function of the IEEE to inform all of its members about Emerson's actions, with a view to suggesting that they might not want to work at that company."

But, says Suran, by making "aliens in engineering" an issue, Feerst has introduced "discrimination, if not bigotry," into the campaign. Citing fiscal 1977 figures showing the Labor Department granted 238 certifications of employment to alien electrical/electronic engineers in a population of about 200,000 EEs, Suran adds: "If we accept the hiring of aliens amounting to 0.12% of the population as a threat to our job security, then we have lost our sense of what the U. S. is all about."

Feerst counters that he is not making alien engineers an issue. Rather, he notes, it was a matter brought up in the 1977 U. S. Member Opinion Survey, which asked: "Should the IEEE support policies to eliminate abuses of immigration practices which affect engineers?" Some 61% said yes, says Feerst, who also cites National Science Foundation figures that there were 69,000 foreign engineers of all specialities that entered the U. S. work force during the 1966–1975 period.

The holder of three earned degrees, Feerst would like to make some sweeping changes in IEEE's educational activities. He says it is time for the institute to withdraw from the Engineers' Council for Professional Development. "It hasn't served us, and its standards are lower and looser than we would like to see," says Feerst, who wants the IEEE to become the accrediting agency for EE colleges. "I'm also against the fact that the Educational Activities Board has not seen fit to come out forcefully against use of the title 'doctor' by IEEE members who have received such titles from either non-accredited, open universities, or as honorary degrees."

Suran is also concerned with elevating standards. He has started a drive to eliminate the bachelor of engineering technology degree.

Both candidates, for different reasons, oppose the sole proposition for an IEEE constitutional amendment on this year's ballot. Made by Robert Bruce, senior past chairman of the Long Island Professional Activities Committee, the proposal calls for changes that would make the entire IEEE board of directors, as well as the entire Executive Committee and all corporate officers, elected by voting members. The board urges a vote against the proposition. Also at stake in this year's election are delegate/director posts in four regions and four divisions. □

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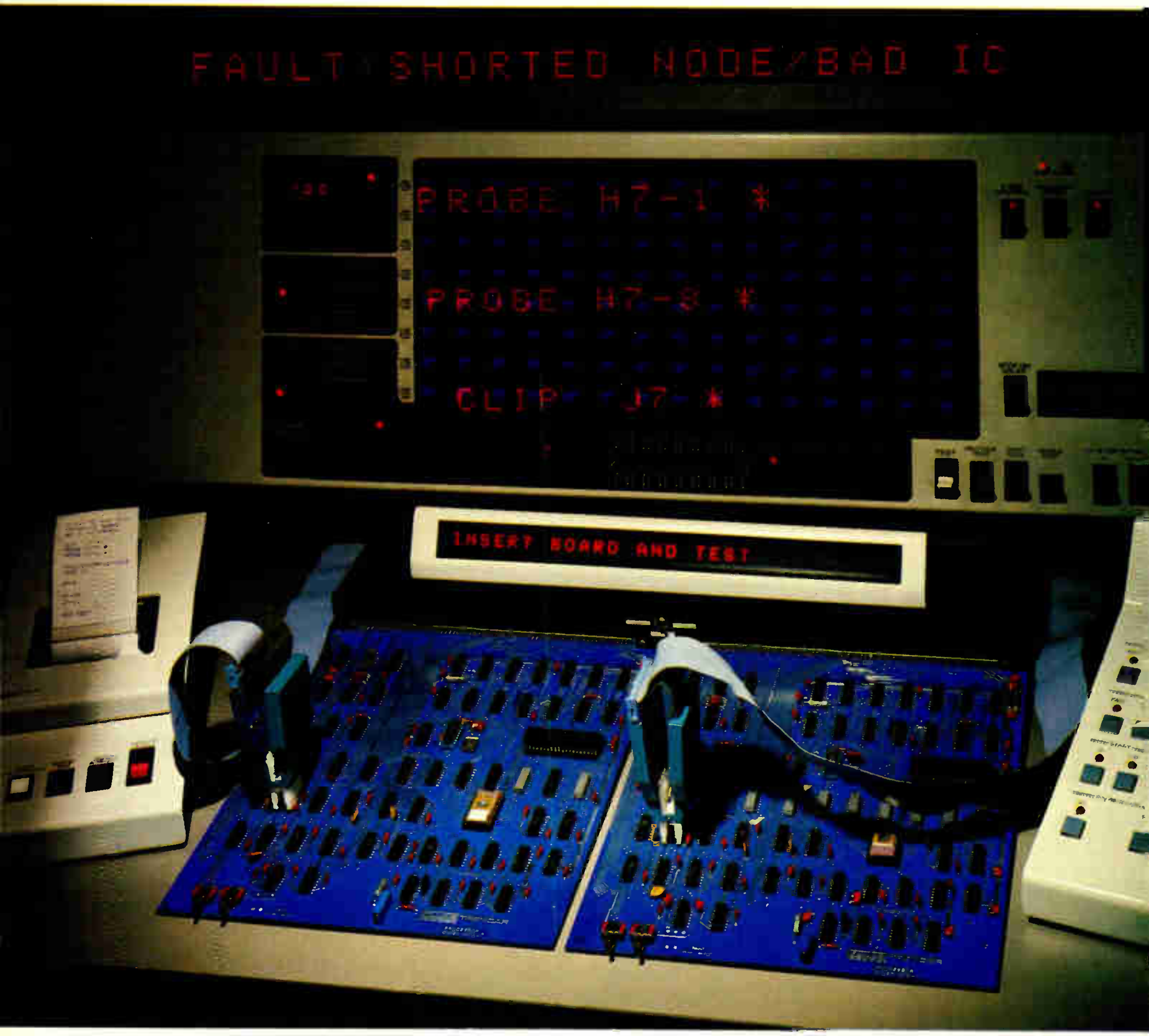

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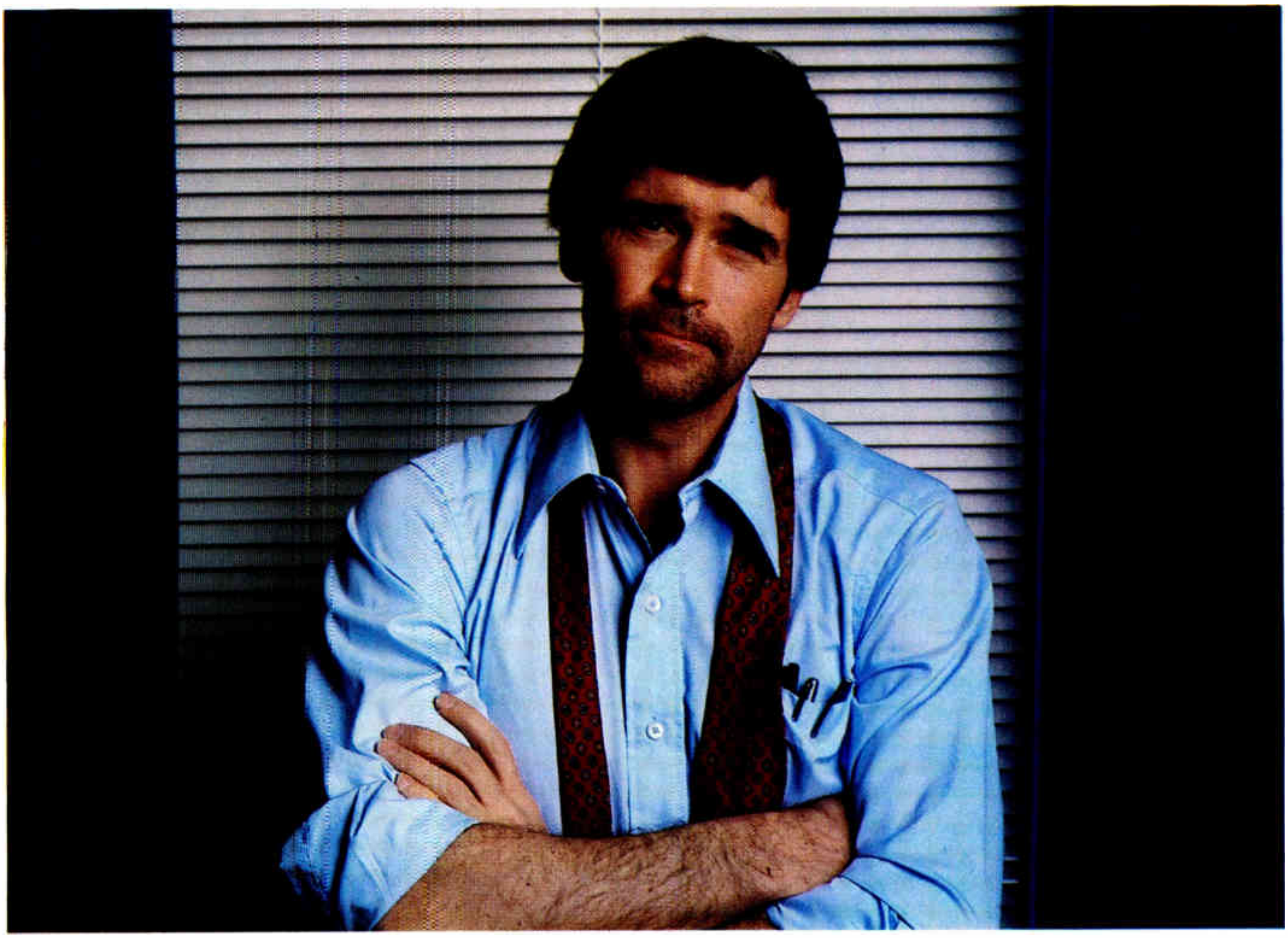

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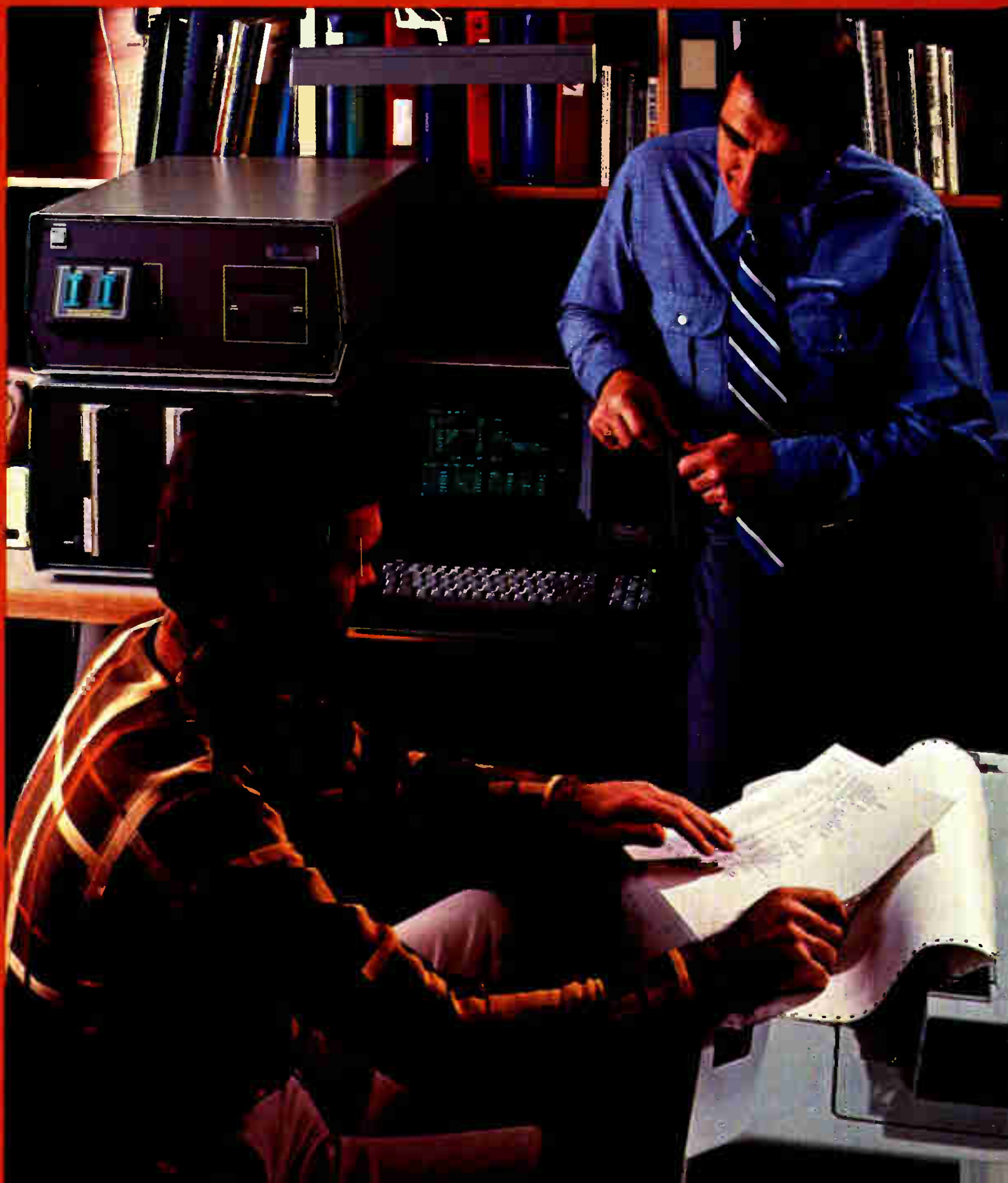

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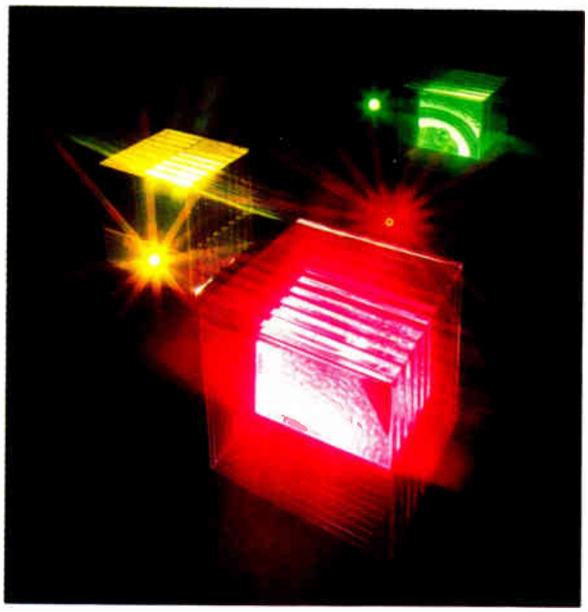


Three-chip system synthesizes human speech

Cost-effective technique called for novel circuit design to cope with complex number-crunching needs

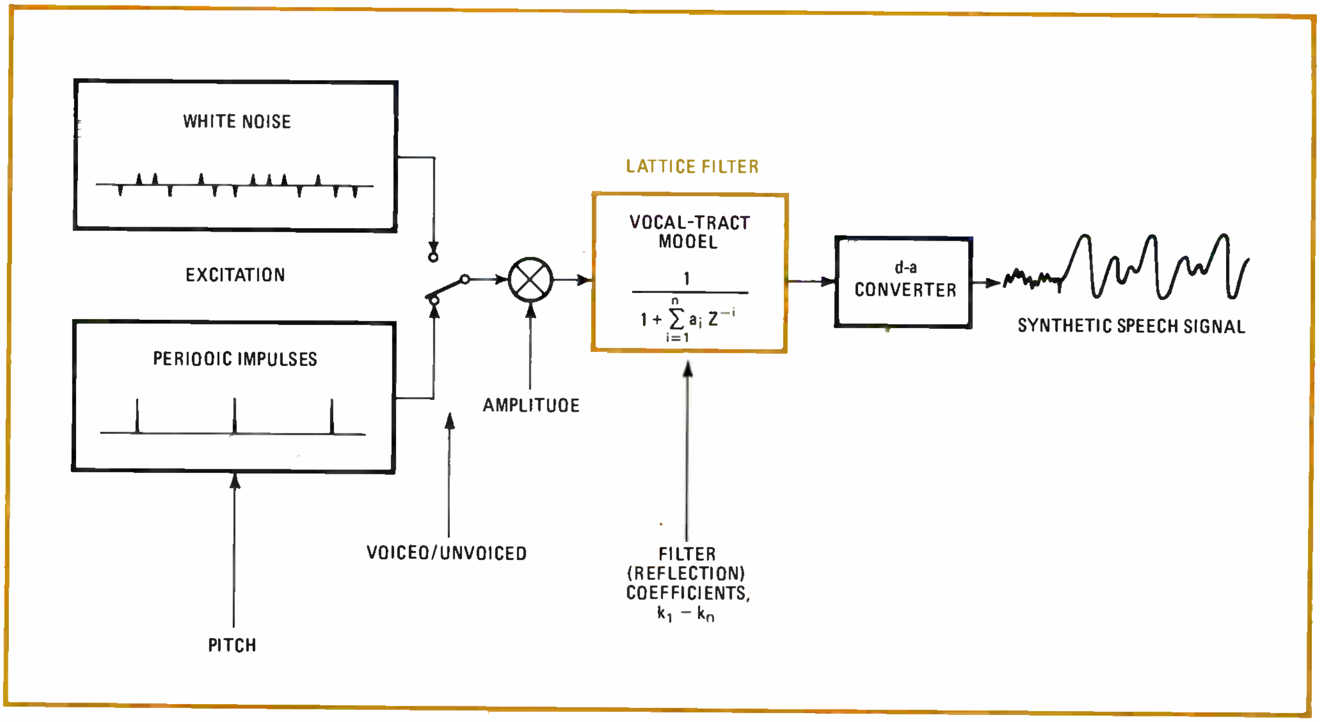
by Richard Wiggins and Larry Brantingham, *Texas Instruments Inc., Dallas*

☐ A three-chip system has finally reduced the synthesis of human speech to the integrated-circuit level. Consisting of a speech synthesizer, read-only memory, and controller, it opens up a new range of design possibilities that is limited only by one's imagination. Teaching aids, telecommunications equipment, and consumer products for home and business are all likely applications, especially as the size of the memory can easily be expanded and the synthesizer chip will work with most microprocessors.

The system is based on the recently developed voice-compression technique called linear predictive coding. LPC can generate speech of high quality from data rates of less than 2,400 bits per second. But the number crunching required is formidable, the more so if it is to be done within the confines of one chip. So the success of LPC in this application hinges on being able to squeeze a multistage filter, or rather its equivalent, onto the synthesizer chip. It is done by making one pipeline multiplier, one adder/substracter, and delay circuits do the work of 10 filter stages.

The resulting synthesizer chip is designated the TMC 0280. Together with the TMC 0350 ROM and the TMC 0270 controller, its first application is in Texas Instruments' new learning aid for spelling, called Speak & Spell.

When this three-chip system produces speech, the controller specifies to the synthesizer the starting point



1. Linear predictive coding. Either pseudo-random noise or a periodic sequence of impulses, representing unvoiced or voiced sounds, respectively, is amplified and fed through a lattice filter that models the resonances of the vocal tract during speech.

of a string of data stored in the ROM. The 131,072-bit ROM has room for approximately 165 words or 115 seconds of speech, depending on the data rate, which may range from approximately 600 to 2,400 b/s. The ROM output provides the pitch, amplitude, and filter parameters from which the synthesizer chip constructs the speech waveform.

To update the speech parameters, the synthesizer is made to transfer a new parameter string from the ROM every 20 milliseconds. But because of the redundancies in a typical speech pattern, a complete set of parameters is not always required. Therefore whole sections of the data stream may be replaced by a single repeat bit, cutting it from a maximum of 49 bits down to a minimum of 4 and thus saving ROM space. But what really shrinks the data to storable proportions is the use of linear predictive coding.

Linear predictive coding

LPC is used in vocoders, which is short for voice coders. It uses a digital filter to model human speech. The filter's input is either a periodic or random sequence of pulses, and its output resembles the waveform of speech. The process has certain similarities to the actual mechanisms of human speech, in which the vocal cords have air forced past them by the lungs and the rest of the vocal tract (tongue, teeth, lips, etc.) modifies the resulting sound.

Figure 1 is a block diagram of the basic elements of an LPC voice-synthesizer system. Shown modeling the vocal tract is a multistage lattice filter that uses coefficients k_1, to k_n to digitally filter an amplified excitation signal, finally passing its output to a digital-to-analog converter connected to a speaker.

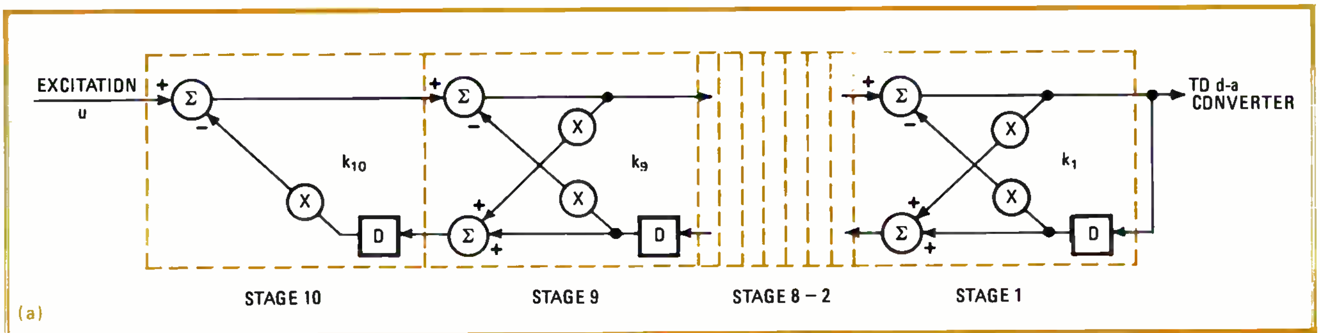
As the diagram shows, the excitation signal may be either a periodic sequence of pulses or pseudo-random noise. Periodic sequences generate voiced sounds, such as the sound of the letters *ee* in the word *speech*, which are created by vibration of the vocal cords; the rate at which the vocal cords open and close determines the pitch of the sound generated. Pseudo-random white noise generates unvoiced sounds, such as the *s* in *speech*, which are heard when the vocal cords are held open and air is forced past them.

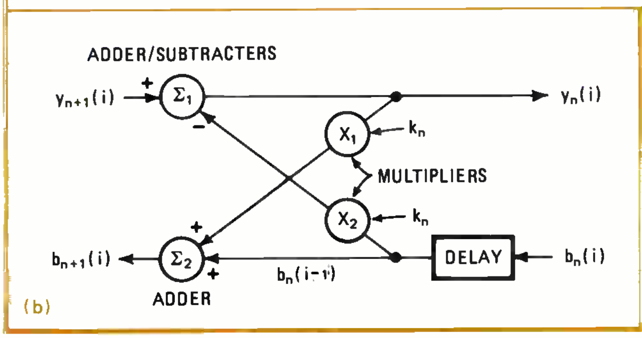
The coded digital data necessary to specify the type of excitation, degree of amplification, and filter coefficients is stored in ROM. Pitch bits either vary the frequency of the periodic sequence or, if all are zero, select random data as the lattice filter's excitation. Along with them is stored a multibit amplification factor, which adjusts the constant-amplitude signal from the excitation source to produce sounds of varying intensity. The filter coefficients are usually updated approximately every 20 milliseconds—a rate that results in speech of very high quality and reasonable ROM storage requirements. If the rate of updating is increased, the lattice filter will model the vocal tract dynamics more closely, but with a corresponding increase in the amount of data to be stored in the ROM.

The lattice filter

The TMC 0280's lattice filter has in effect 10 stages (called 10th-order LPC or LPC-10). Each stage (except stage 10) carries out two multiplications and two additions on its two digital inputs before passing the results backwards and forwards to its neighbors. The operations of the 10 stages are carried out sequentially, as are the 4 operations within each stage.

Careful timing of this sequence of 40 operations makes it possible for 1 adder and 1 multiplier to do the





2. Lattice filter. Diagrammed in (a) is a hypothetical 10-stage filter, of which one stage is shown in detail in (b). The coefficients k_1-k_{10} vary between +1 and −1, permitting fixed-point arithmetic, and are periodically updated to reflect vocal tract changes.

work of 20 adders and 20 multipliers. But to understand how the timing works, it is simplest to start by visualizing 10 stages carrying out these 40 operations one after the other. The block diagrams in Fig. 2 therefore model the occurrence of actual additions and multiplications with hypothetical adders and multipliers.

Figure 2a shows the excitation signal u entering stage 10 of the filter and the output from stage 1 being applied to the d-a converter and also being fed back through the filter. (Only three stages are shown in detail since the other seven are just like stage 1; stage 10, though, having only a single output, has no need for the second output adder or its associated multiplier. But the design does in fact use the multiplier for amplification purposes, as will be explained later.)

Figure 2b shows what happens in the filter's nth stage during the ith time cycle to the y data deriving directly from u and to the feedback b data. Note that the subscript of the y and b data defines the stage in which that data is used while the term in parenthesis indicates the cycle in which the data is generated.

At the start of cycle i, the input to this stage, $y_{n+1}(i)$, is applied to adder 1, whose other input is subtracted from it. This other input derives from the output of multiplier 2, which takes roughly half the cycle to compute the product of coefficient k_n and its input from the delay circuit, $b_n(i-1)$. The result of this subtraction then spends roughly the other half of the current (i) cycle being multiplied in multiplier 1 and added to the contents of adder 2—namely, $b_n(i-1)$ from the delay circuit—to yield $b_{n+1}(i)$. This $b_{n+1}(i)$ is the feedback data required by the preceding ($n+1$) filter stage for application to its delay circuit. (Note how the subtraction, multiplication, addition, and second multiplication are done one after the other.)

TABLE 1: LATTICE FILTER EQUATIONS	
Equation	Stage
$y_{10}(i) = y_{11}(i) - k_{10}b_{10}(i-1)$	10
$y_9(i) = y_{10}(i) - k_9b_9(i-1)$ $b_{10}(i) = b_9(i-1) + k_9y_9(i)$	9 9
$y_8(i) = y_9(i) - k_8b_8(i-1)$ $b_9(i) = b_8(i-1) + k_8y_8(i)$	8 8
$y_7(i) = y_8(i) - k_7b_7(i-1)$ $b_8(i) = b_7(i-1) + k_7y_7(i)$	7 7
$y_6(i) = y_7(i) - k_6b_6(i-1)$ $b_7(i) = b_6(i-1) + k_6y_6(i)$	6 6
$y_5(i) = y_6(i) - k_5b_5(i-1)$ $b_6(i) = b_5(i-1) + k_5y_5(i)$	5 5
$y_4(i) = y_5(i) - k_4b_4(i-1)$ $b_5(i) = b_4(i-1) + k_4y_4(i)$	4 4
$y_3(i) = y_4(i) - k_3b_3(i-1)$ $b_4(i) = b_3(i-1) + k_3y_3(i)$	3 3
$y_2(i) = y_3(i) - k_2b_2(i-1)$ $b_3(i) = b_2(i-1) + k_2y_2(i)$	2 2
$y_1(i) = y_2(i) - k_1b_1(i-1)$ $b_2(i) = b_1(i-1) + k_1y_1(i)$	1 1
$b_1(i) = y_1(i)$	

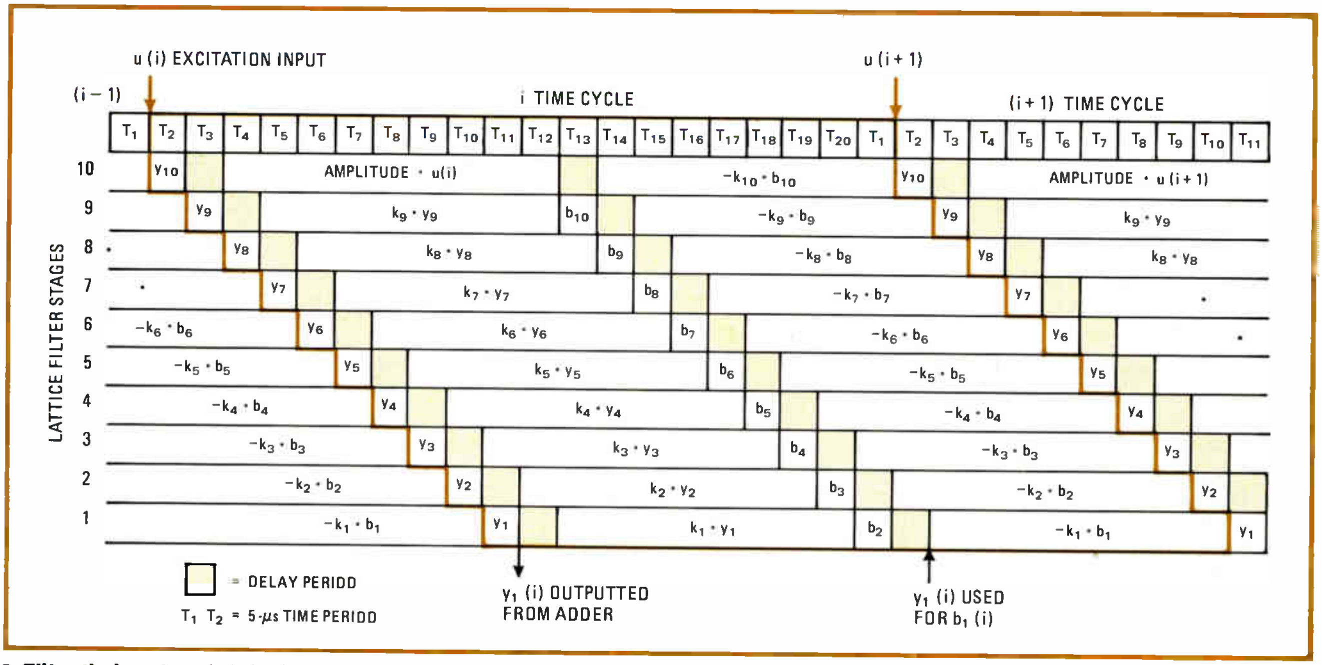
From this it follows that the 10 stages also operate sequentially, since during any time cycle y_{10} must be calculated before y_9, which must be calculated before y_8, and so on, while b_1 must similarly be calculated before b_2, and so on.

Equations expressing the relationship between the various y and b data are given in Table 1. In all of the calculations performed by the filter, the y and b data as well as the coefficients k_1–k_{10} are multibit numbers. The coefficients k_1–k_{10} may vary between a decimal equivalent of ±1 and are periodically updated.

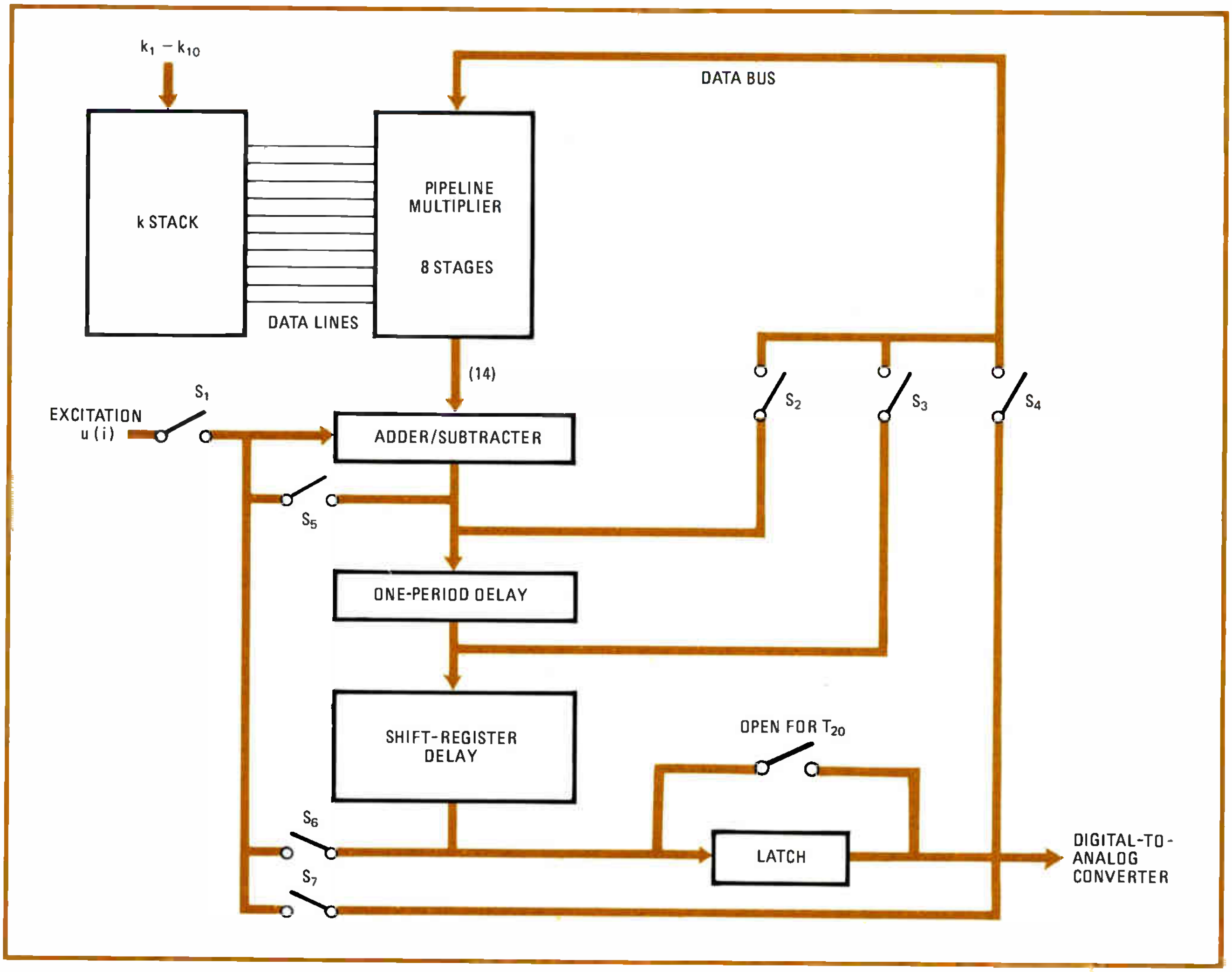
The digital multiplier

Figure 3 charts the flow of activity through all 10 stages of the lattice filter during the successive time periods of successive time cycles. Each of the 20 time periods, $T_1 - T_{20}$, lasts 5 microseconds. The time cycles are indicated as $i-1$, i, and $i+1$ for ease in comparing the availability of the intermediate results in the filter with the requirements set out by mathematical representation of the filter given in Table 1.

In the first time period, T_1, the excitation data $u(i)$ is applied as an input; the output of the filter, y_1, becomes available at time period T_{11}, half a time cycle or 50 μs



3. Filter timing. A cycle is broken down into twenty 5-microsecond time periods. An addition requires one period, while a multiplication needs eight. To ensure that only one of each kind of operation begins in each time period, a delay is added after each sum is calculated.



4. Data routing. The multiplier output is one input to the adder/subtracter. Depending on the status of switches S_1, S_5, S_6, and S_7, the other input may be the excitation input or the output from the adder, multiplier, or latch. Similar paths are created by S_2, S_3 and S_5.

TABLE 2: COEFFICIENTS FROM k STACK											
k-stack output		Time period									
Bit	Line	T_1 T_{11}	T_2 T_{12}	T_3 T_{13}	T_4 T_{14}	T_5 T_{15}	T_6 T_{16}	T_7 T_{17}	T_8 T_{18}	T_9 T_{19}	T_{10} T_{20}
LSB	1	k_2	k_1	k_{10}	k_9	k_8	k_7	k_6	k_5	k_4	k_3
	2	k_2	k_1	k_{10}	k_9	k_8	k_7	k_6	k_5	k_4	k_3
	3	k_3	k_2	k_1	k_{10}	k_9	k_8	k_7	k_6	k_5	k_4
	4	k_4	k_3	k_2	k_1	k_{10}	k_9	k_8	k_7	k_6	k_5
	5	k_5	k_4	k_3	k_2	k_1	k_{10}	k_9	k_8	k_7	k_6
	6	k_6	k_5	k_4	k_3	k_2	k_1	k_{10}	k_9	k_8	k_7
	7	k_7	k_6	k_5	k_4	k_3	k_2	k_1	k_{10}	k_9	k_8
	8	k_8	k_7	k_6	k_5	k_4	k_3	k_2	k_1	k_{10}	k_9
MSB	9	k_9	k_8	k_7	k_6	k_5	k_4	k_3	k_2	k_1	k_{10}
Sign bit	10	k_9	k_8	k_7	k_6	k_5	k_4	k_3	k_2	k_1	k_{10}

later. Now an add operation, which takes one time period, is initiated and completed every 5 μs in the cycle. A multiply operation is similarly initiated every 5 μs but is not completed for eight time periods or 40 μs; with the pipeline multiplier used for the speech-synthesizer chip, this means a result is available at the output of each stage every time period.

Altogether, however, the add and multiply operations use up only 45 μs of the 50-μs half cycle, requiring a delay period of 5 μs to be inserted between them if they are not to overlap. Otherwise, to initiate multiple add or multiply operations in any given time period, more than one adder and one multiplier will be needed. Equally important, the time cycles of successive filter stages start one time period after each other, yet each stage needs to be able to fall into step with its neighbors' operations at least once per cycle in order to hand on and accept b data. Thus the insertion of a 5-μs delay period after the add operation that produces, say, the b output from the 8th stage ensures that b_8 becomes available to it from the 7th stage, in time for the $-k_8 \cdot b_8$ multiply operation.

As shown in Fig. 3, the $k_{10} \cdot y_{10}$ and b_{11} intermediate results are obtained, though not required for a digital implementation of the lattice filter because there is no previous stage in need of the data. But in the actual circuitry, it is easier to generate them than to stop the filter from making the calculations.

Recall that the amplitude of the excitation signal for the production of voiced and unvoiced sounds is controlled by an amplification factor. The excitation data is actually multiplied by the amplification factor and this multiplication is done by multiplier in stage 10 during the time that $k_{10} \cdot y_{10}(i)$ would otherwise be generated.

Digital filter design

A block diagram of the actual digital 10-stage lattice filter is shown in Fig. 4. The filter includes a pipeline multiplier, an adder/subtracter circuit, a delay circuit, a shift register, and a latch memory.

The pipeline multiplier performs all 20 of the multiplications required by the lattice filter. It receives either y_n or b_n via the data bus and the coefficients k_1–k_{10} from the k stack of shift registers via the data lines.

It initiates a different multiplication operation every 5-μs interval. As already mentioned, one multiplication operation requires eight time periods, so the pipeline multiplier has eight stages. Thus there are eight multiplications in various stages of completion at any given time. The multiplier's 40-μs computation time can be determined from its inputs and outputs as shown in Table 2.

The k stack consists of 10 shift registers, each of which has 10 stages so that each of the 10 coefficients can be circulated for 10 time periods. The arrangement is shown in Table 2. The coefficients are stored as 9-bit numbers plus a sign bit. The decimal equivalents of these 10-bit numbers range from -1 to $+1$, which simplifies the structure of the pipeline multiplier since the intermediate results obtained in the multiplication operations will have a decreasing numerical value. Also, it can be shown that all values of k in the range $+1$ to -1 ensure filter stability.

The output of the multiplier is 14 parallel bits: 13 bits of data and 1 sign bit. These 14 bits form one input to the adder/subtracter circuit. The other input varies with the time period: it is the excitation signal at time period T_1, the multiplier output during time periods T_2 through T_{10}, the output of the shift register for time periods T_{11} through T_{19}, or the output of the latch memory at time period T_{20}. The particular input to the adder/subtracter circuit is controlled by digital switches illustrated as single-pole, single-throw switches S_1, S_5, S_6, and S_7.

The output of the adder/subtracter is also 14 parallel bits; it is delayed one time period before being stored in the shift register—actually 13 shift registers, each of which has eight stages. (Remember, the multiplication operation requires eight time periods.) The shift register is arranged to perform shift operations only during time periods T_{12} through T_2.

Table 3 is a list of the various intermediate results occurring in the circuit of Fig. 4 during time periods T_1 through T_{20}. One of the multiplier inputs comes from the k stack, while the other input varies according to which of the switches S_2, S_3, or S_4 is closed. At time period T_1 switch S_2 is closed so that the output of the adder/subtracter, in this case $b_2(i-1)$, is applied as a multiplier input. At the same time the other input to the multiplier is the excitation signal $u(i)$. At time period T_2, the other multiplier input is $b_1(i-1)$, which is from the output of

TABLE 3: INTERMEDIATE RESULTS AVAILABLE IN EACH TIME PERIOD

Time period	Multiplier inputs from k stack	Multiplier inputs from Data bus	Multiplier output and one adder input	Other adder input	Adder output	Period-delay output	Shift-register output	Latch output
T_1	$-k_2$	$b_2(i-1)$	$-k_{10} \cdot b_{10}(i-1)$	$u(i)$	$b_2(i-1)$	$b_3(i-1)$	$b_{11}(i-1)$	$y_1(i-1)$
T_2	$-k_1$	$b_1(i-1)$	$-k_9 \cdot b_9(i-1)$	$y_{10}(i)$	$y_{10}(i)$	$b_2(i-1)$	$b_{10}(i-1)$	↓
T_3	k_{10}	$y_{10}(i)$	$-k_8 \cdot b_8(i-1)$	$y_9(i)$	$y_9(i)$	$y_{10}(i)$	↓	↓
T_4	k_9	$y_9(i)$	$-k_7 \cdot b_7(i-1)$	$y_8(i)$	$y_8(i)$	$y_9(i)$	↓	↓
T_5	k_8	$y_8(i)$	$-k_6 \cdot b_6(i-1)$	$y_7(i)$	$y_7(i)$	$y_8(i)$	↓	↓
T_6	k_7	$y_7(i)$	$-k_5 \cdot b_5(i-1)$	$y_6(i)$	$y_6(i)$	$y_7(i)$	↓	↓
T_7	k_6	$y_6(i)$	$-k_4 \cdot b_4(i-1)$	$y_5(i)$	$y_5(i)$	$y_6(i)$	↓	↓
T_8	k_5	$y_5(i)$	$-k_3 \cdot b_3(i-1)$	$y_4(i)$	$y_4(i)$	$y_5(i)$	↓	↓
T_9	k_4	$y_4(i)$	$-k_2 \cdot b_2(i-1)$	$y_3(i)$	$y_3(i)$	$y_4(i)$	↓	↓
T_{10}	k_3	$y_3(i)$	$-k_1 \cdot b_1(i-1)$	$y_2(i)$	$y_2(i)$	$y_3(i)$	↓	↓
T_{11}	k_2	$y_2(i)$	$k_{10} \cdot y_{10}(i)$	$b_{10}(i-1)$	$y_1(i)$	$y_2(i)$	$b_{10}(i-1)$	↓
T_{12}	k_1	$y_1(i)$	$k_9 \cdot y_9(i)$	$b_9(i-1)$	$b_{11}(i)$	$y_1(i)$	$b_9(i-1)$	↓
T_{13}	$-k_{10}$	$b_{10}(i)$	$k_8 \cdot y_8(i)$	$b_8(i-1)$	$b_{10}(i)$	$b_{11}(i)$	$b_8(i-1)$	↓
T_{14}	$-k_9$	$b_9(i)$	$k_7 \cdot y_7(i)$	$b_7(i-1)$	$b_9(i)$	$b_{10}(i)$	$b_7(i-1)$	↓
T_{15}	$-k_8$	$b_8(i)$	$k_6 \cdot y_6(i)$	$b_6(i-1)$	$b_8(i)$	$b_9(i)$	$b_6(i-1)$	↓
T_{16}	$-k_7$	$b_7(i)$	$k_5 \cdot y_5(i)$	$b_5(i-1)$	$b_7(i)$	$b_8(i)$	$b_5(i-1)$	↓
T_{17}	$-k_6$	$b_6(i)$	$k_4 \cdot y_4(i)$	$b_4(i-1)$	$b_6(i)$	$b_7(i)$	$b_4(i-1)$	↓
T_{18}	$-k_5$	$b_5(i)$	$k_3 \cdot y_3(i)$	$b_3(i-1)$	$b_5(i)$	$b_6(i)$	$b_3(i-1)$	↓
T_{19}	$-k_4$	$b_4(i)$	$k_2 \cdot y_2(i)$	$b_2(i-1)$	$b_4(i)$	$b_5(i)$	$b_2(i-1)$	↓
T_{20}	$-k_3$	$b_3(i)$	$k_1 \cdot y_1(i)$	$b_1(i-1)$	$b_3(i)$	$b_4(i)$	$y_1(i)$	$y_1(i-1)$
T_1	$-k_2$	$b_2(i)$	$-k_{10} \cdot b_{10}(i)$	$u(i+1)$	$b_2(i)$	$b_3(i)$	$b_{11}(i)$	$y_1(i)$

the latch via switch S_4. Also at time period T_2, the other adder input is its own output, in this case $y_{10}(i)$. At time period T_3 the multiplier inputs are k_{10} and $y_{10}(i)$, which are the output of the one period delay circuit. The results of this multiplication will not be available until time period T_{11}, when they will be provided as one of the inputs to the adder/subtracter circuit. At time period T_{11} the other input to the adder/subtracter is taken from the output of the shift register. The first term loaded from the shift register is the $b_{10}(i-1)$ term, which was first output at time period T_2 and remained at the output until T_{11} since the shift register does not shift during this time.

At time period T_{13} the multiplier's input on the data bus comes from the output of the adder/subtracter circuit via switch S_2. At time period T_{20} the $y_1(i)$ term is sent to the latch memory from the shift register and the current output of the latch is applied to the other input of the adder/subtracter circuit through switch S_7. The latch stores the filter's output (y_1) for one cycle.

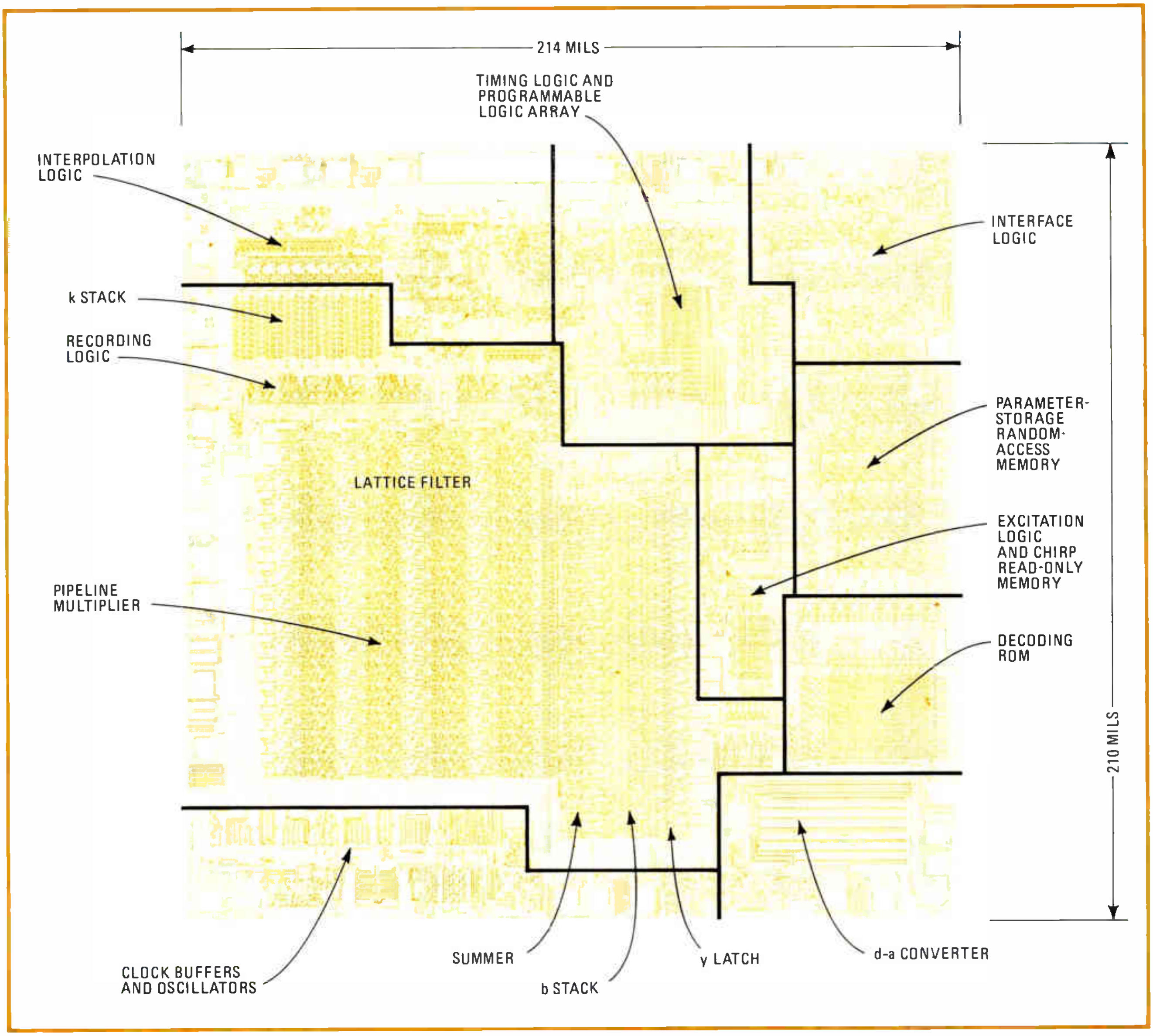
To sum up, the digital implementation of a 10-stage latice filter performs the filtering operation at reasonable data rates. Here, for example, the coded data is applied in short bursts every 20 ms. A 10-kilohertz output speech sample rate requires a time cycle of 100 μs, allowing the basic operations of the adder/subtracter, the multiplier, and shift registers to be accomplished in 5-μs time periods. Since such speeds are well within the capabilities of p-channel MOS technology, the speech synthesis chip can be produced at a very low cost.

The various functional sections of the TMC 0280 speech synthesizer chip are shown in Fig. 5. The converter section contains an 8-bit digital-to-analog converter with an accuracy of ½ least significant bit and the ability to drive a 200-milliwatt speaker. The sign of the output word (y_1) determines the direction of the current flow in the speaker that provides the d-a conversion for the most significant bit. Filtering is provided off chip by the speaker and an impedance-matching transformer to eliminate the effects of the 10-kHz sample rate.

The rest of the chip

The long rectangular area in this d-a section of the chip contains upper-level driver transistors yet occupies only about 1,200 square mils. To maintain this small an area yet produce enough output to drive a speaker, the 14-bit output of the y latch is digitally clipped to 8 bits via some truncation logic. In essence, this truncation logic increases the average level of the output signal by increasing the level of the lower-order bits—a scaling of the signal that has no noticeable effect on the output since the upper-level bits are used a very small percentage of the time.

In the excitation generation section of the synthesizer chip, two separate logic blocks provide voiced and unvoiced excitation in response to the signals from the 131-kilobit ROM. For voiced sounds, a 5-millisecond periodic chirp sequence is applied to the input of the lattice filter at a time interval corresponding to the pitch. The chirp signal sweeps across the frequency spectrum. It is of the form sin ωt^2 and is stored in digital form in on-chip ROM addressed by the pitch-period counter. Address inputs equal to 0 or greater than 50 produce a zero output. This section also contains a pitch counter, actual-



5. Talking chip. The lattice filter is the largest single element on the speech synthesizer chip. For voiced sounds, a chirp sequence enters the filter; for unvoiced sounds, the sequence has a random sign. Also on the chip are RAM, ROM, and timing and interface logic.

ly a serial binary counter that counts up from 0 until its value is greater than or equal to the value in the pitch register, whereupon it resets itself and starts over again. Special provisions zero the pitch counter at a voicing transition (from voice to unvoiced excitation and vice versa) and before the start of speech. For unvoiced sounds the excitation has a constant magnitude of 0.5 and pseudorandom sign. The sign bit is provided by a 13-bit shift counter with three exclusive-OR feedback circuits.

Decoding tables for the 12 speech synthesis parameters (10 reflection coefficients k_1–k_{10}, pitch and energy) are stored in the ROM in the section of the chip that loads, stores, and decodes parameters. Recall that these parameters are updated periodically. In most cases, it is desirable for the speech parameters to vary smoothly from one updating period (or frame) to the next. The TMC 0280 contains logic to do an approximately linear interpolation of all 12 parameters at eight points within the frame. When selected by the parameter counter, the parameters are interpolated one at a time. This serial operation minimizes the silicon area required, since parallel data lines are not needed. To further conserve area and eliminate error, the interpolation logic calculates a new parameter value from the present value and the next or target value stored in code in the parameter random-access memory.

ROM organization

The frame of data stored in the parameter RAM consists of 12 codes or pointers that select 10-bit parameter values from a 216-by-10-bit ROM. Each speech parameter is provided its own decoding table organized in ROMs of 2^n by 10 bits, where n is the number of code bits for a given parameter. The parameter counter's 4 MSBs supply the table select and the parameter RAM supplies the value address. The 10-bit parallel output of the parameter ROM is applied to the inputs of a parallel-

Other products that talk

A growing number of products now "talk." The speech chip described in this article is contained in an inexpensive learning aid for children called Speak & Spell [*Electronics*, June 22, p. 39].

Votrax of Troy, Mich., a division of Federal Screw Works, makes two portable speech synthesizers for the vocally impaired [*Electronics*, Nov. 10, 1977, p. 32]. It also manufactures a Business Communicator, which translates up to 64 telephone Touch-Tone inputs into an audio response, and a multilingual voice system, which electronically synthesizes English and German and is planned to do the same for Spanish, Japanese, French, and Persian. All Votrax products join phonemes.

Comutalker Consultants in Santa Monica, Calif., sells a speech synthesizer that connects to the hobbyist's S-100 bus. With this board, either the user manipulates nine control parameters directly or an optional software package automatically computes the parameters from phonically spelled ASCII (for example, *Hello* would be phonically spelled H—H—E—L—O—W).

Also producing S-100-compatible synthesis boards is Speech Technology of Santa Monica, Calif. It makes two such boards, the M-188 and M-250, which generate speech from stored vocabularies of words. Using LPC to generate formats, they achieve data rates as low as 1 kilobit per second.

Master Specialties Co. of Costa Mesa, Calif., manufactures a talking calculator and a variety of word-oriented announcement products.

Telesensory Systems Inc., Palo Alto, Calif., which also makes a talking calculator for the blind, has recently described a two-chip set of 40-pin integrated circuits for synthesized speech applications. Designed to function with standard memories and digital-to-analog converters, the new chips are fully programmable, offering a wide range of synthesized "voicings." The firm plans to introduce an advanced spoken-word output reading system for the blind in 1979.

John Posa

to-serial converter, which is loaded according to timing signals generated by the interpolation logic.

The timing for the TMC 0280 is based on a 50-hertz frame rate (the rate at which new speech data is obtained from the ROM) and a 10-kHz sample rate that corresponds to a maximum output frequency of 5 kHz. An 800-kHz oscillator is divided by four to produce two major phases, ϕ_1 and ϕ_2, with corresponding precharge clocks ϕ_3 and ϕ_4. Twenty 5-μs time periods, T_1 through T_{20}, are generated by a state-shift counter driving a programmable logic array. These state times are used for control and timing within the 100-μs sample period. A 25-state binary parameter counter provides the 2.5-millisecond parameter interpolation interval. The states of the counter serve as controls for the interpolation and parameter loading processes.

The other two chips

The coded speech data for the synthesizer chip is stored in the TMC 0350, organized as a 16,384-by-8-bit ROM and having an internal 18-bit address counter/register and two 8-bit output buffers. Fourteen bits of the address go directly to the ROM array, while the 4 MSBS are used as a 1-of-16 chip-select. Several means were used to achieve this large 131-kilobit capacity. First, the chip is a virtual-ground dynamic ROM fabricated on a very large bar of silicon. Next, there are no pads on half of the bar, so that interconnection lines are limited to one side and the array goes right up to the edge of the bar on most of three sides. Also, minimum-area design rules were used to achieve a cell size of only 0.225 square mil per bit.

The third chip in this three-chip speech-synthesis system is the TMC 0270 controller, which is a slightly modified calculator chip. It is a member of the TMS 1000 microprocessor family. The TMC 0270 shares the basic architecture of the TMS 1000, but has modifications that enhance its binary-coded-decimal arithmetic capabilities. It also has an expanded instruction set and output multiplexer to reduce the pinouts required in this application.

During speech, the TMC 0280 synthesizer accesses the phrase ROM directly but when it receives an end-of-phrase command, returns control to the controller. In periods of silence the controller has complete control over the ROM interface lines: it can transfer phase start addresses to the ROM or access address look-up tables or other auxiliary data from the ROM.

There are five special lines from the controller to the synthesizer that transfer data and commands within the system. One of these lines is the processor data clock, which is used to determine when the other four lines are valid.

The controller has several commands. In addition to the normal read command, there is the speak command, which tells the synthesizer to start accessing data and begin speaking, and a test/talk command, which allows the controller to determine whether or not the synthesizer is finished talking. The controller can tell the ROM to read 1 bit and the ROM will shift 1 bit into a 4-bit shift register. This sequence can be repeated three more times until 4 bits are ready for output onto the four control and data lines.

Although the controller was specifically designed to interface with the TMC 0280 speech synthesizer, the synthesizer chip was designed so that most microprocessors could be used as controllers. This feature can only add to the numbers of manufacturers of appliances and electronic controls attracted by the possibilities of low-cost speech synthesis.

Indeed, yet another phase of electronic wizardry seems about to begin. One can easily envision clocks that literally tell the time, appliances and machines that explain their operation, and computers that speak our language. This improvement in the man-machine interface will surely enhance the effectiveness of many devices used in daily life. However, the inverse operation, that of recognizing a wide range of human voices, complete with accents, slurring, and slang, continues to pose a genuine challenge to electronics technology. □

Plasma processes set to etch finer lines with less undercutting

Wet chemical etching is starting to give way to plasma-assisted techniques that now can etch selectively any level on a semiconductor device with greater dimensional control

by C. J. Mogab, *Bell Laboratories, Murray Hill, N. J.*
and W. R. Harshbarger, *Bell Laboratories, Allentown, Pa.*

☐ If there were a Rip van Winkle of semiconductors and if he were to fall asleep today, he would wake up to an industry as vastly changed in manufacturing technology as it will be in design advances. One important difference he would note right away would be plasma etching's displacement of wet etching.

Based on the use of reagent gases, plasma etching is safer and less expensive than wet etching, which is based on sulphuric, hydrofluoric, or phosphoric acid. Also, it provides finer resolution and less undercutting, so it is better suited to the era of very-large-scale integration.

As interest in plasma etching has grown over the past several years, new equipment and new processes have been developed that overcome certain drawbacks. For one thing, it is now possible to etch selectively any level on a metal-oxide-semiconductor or bipolar device. Furthermore, it is now possible to etch thin films of semiconductor material anisotropically (leaving a perpendicular edge), as well as isotropically (leaving a concave edge). This advance over wet etching greatly improves the dimensional control of integrated-circuit patterns, leading to ever-higher circuit density.

Physical and chemical phenomena

A plasma is an ionized gas, composed of nearly equal quantities of positive and negative charge (electrons and positive and negative ions) [*Electronics*, July 21, 1977, p. 81]. Plasma etching techniques employ weakly ionized gases produced by low-pressure electric discharges. Inelastic collisions between gas molecules and energetic electrons created by the electric field produce the ions and free radicals that can cause etching by physical and chemical interactions with surfaces.

An important characteristic of these discharges is that the gas temperature is much lower than the free-electron temperature. The low gas temperature means that it is possible to directly expose thermally sensitive materials, such as photoresists, to these plasmas.

Plasma-assisted etching had its beginning in the 19th-century work of Michael Faraday and Sir William Crookes on gas discharges in vacuums. W. R. Grove reported the erosion of matter by sputtering processes in a plasma more than 100 years ago.

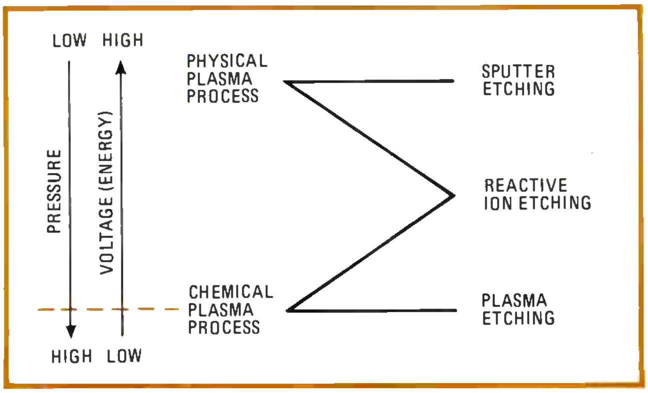
Sputtering is a wholly physical process, in which the plasma's ions are accelerated by an electric field and made to hit a solid's surface. They transfer their momentum to the surface, ultimately causing atoms of the solid to be ejected. The physical phenomenon of sputtering forms the basis of two plasma-assisted etching techniques: sputter etching and ion-beam milling, also called ion milling.

To achieve useful etch rates, that is, to direct many ions toward the solid, these processes require relatively low pressures (less than 0.1 torr), as well as high particle energies that make them prone to causing damage to semiconductor devices.

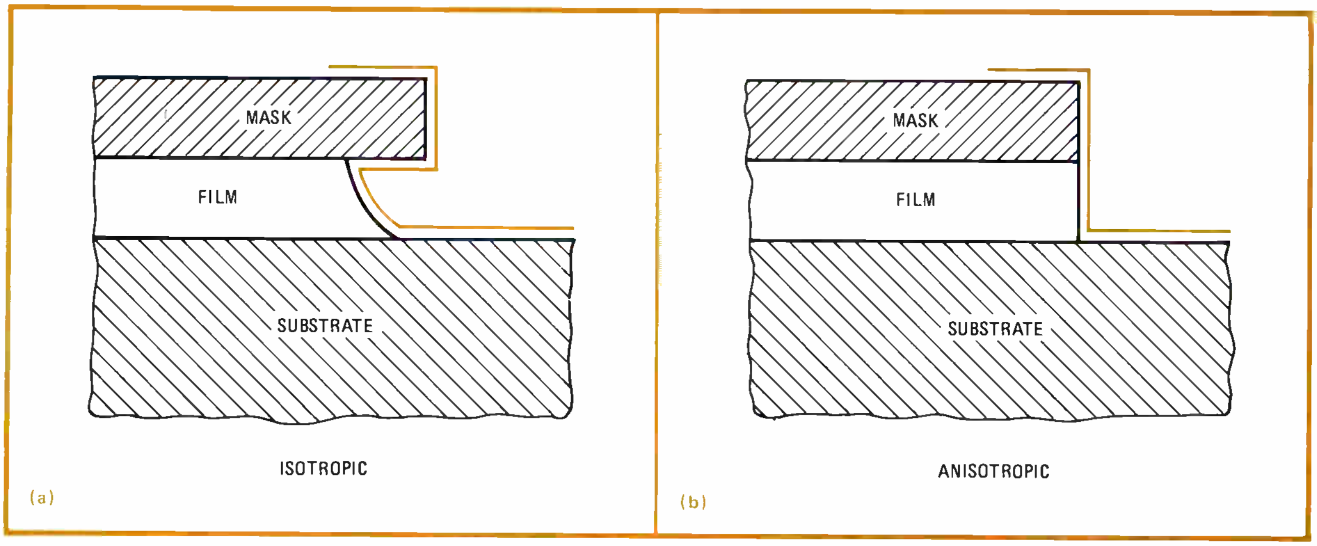
Even worse, these etching techniques provide very little selectivity in etch rates among the materials used in silicon IC fabrication. Selectivity is a key word in the delineation of patterns, signifying that the etching does not go below the layer for which it is intended.

However, there is also a chemical plasma-assisted technique, called simply plasma etching, in which an electrically induced gas discharge provides active free radicals that combine chemically with a solid to produce volatile products. Generally it is done at higher pressures than the physical etch techniques, and since it needs lower-energy particles, it is less damaging to the semiconductor solid.

In 1971, S. Irving, K. E. Lemons, and G. E. Bobes of Signetics Corp. reported that carbon tetrafluoride (CF_4) can be dissociated in a plasma to produce fluorine atoms and other reactive free radicals. Fluorine atoms react vigorously with silicon and its compounds to produce



1. Plasmas. Depending on pressure and energy available, the spectrum of plasma-assisted etching can go from chemical to physical. The techniques are becoming the processes of choice for LSI and VLSI manufacturing and are gradually displacing wet etching.



2. Along the edge. A fully isotropic edge profile film (a) undercuts the photoresist mask by an amount equal to the film thickness. An anisotropic edge (b), on the other hand, has no undercut. Anisotropic etching is an absolute must for the high-resolution patterns of VLSI.

SiF_4, which is a gas at room temperature. The reaction is close to a purely chemical process; indeed, if argon is simply substituted for CF_4, the etch rate of silicon is insignificant, indicating negligible sputtering.

Between the extremes of physical sputtering and plasma etching, there exists a broad spectrum of plasma conditions (Fig. 1). In 1974, N. Hosokawa and his co-workers at Nippon Electric Varian Ltd. discovered a way station between the two extremes: reactive sputter etching, also called reactive ion etching. Their experiments demonstrated that the etch rates and selectivity of physical plasma sputtering could be improved by substituting halocarbons for noble gases. As Fig. 1 shows, this substitution involves lower energy requirements than does straight sputter etching.

In fact, reactive sputter etching suggests that there is no sharp demarcation between physical and chemical techniques. In general, both may occur, perhaps synergistically, in plasma etching. Of course, there is more chemical etching and less physical etching as pressure increases or, more generally, as the average energy of the plasma decreases.

Still, at just what point, if ever, physical ion bombardment becomes unimportant is not known precisely. For instance, R. A. H. Heinecke of Standard Telecommunications Laboratories Ltd. in England has demonstrated that plasma etching under high-power conditions can improve selectivity and feature profiles in silicon dioxide.

Good performance

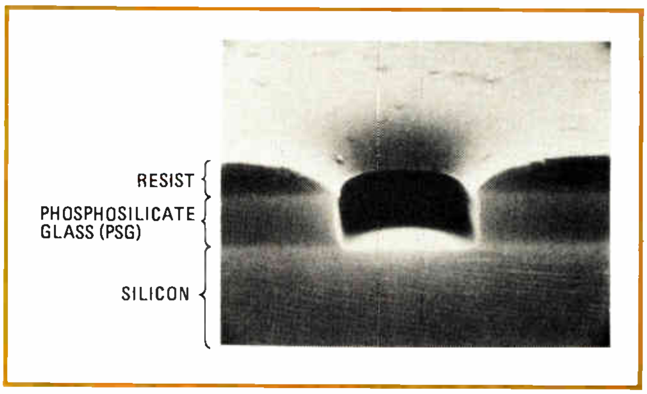
Wet chemical etching techniques would be expected to etch isotropically, giving rise to edge profiles of the kind shown in Fig. 2a. The concavity of the etched feature undercuts the mask (on top of the circuitry for illustration only; in actual production, it would have long since been removed). Thus the etching does not faithfully reproduce the dimensions of the mask.

This undercutting is not a serious problem until the ratio of feature width to layer thickness drops below about 5 : 1, as it inevitably must for VLSI. Imagine trying to produce 2-micrometer lines and spaces in a 1-μm-thick film with isotropic etching that would produce the edge profile of Fig. 2a.

However, the nature of the boundary layer between a plasma and a solid surface is such that the charged particles have trajectories perpendicular to the surface. With many semiconductor materials, such directional bombardment can lead to the edge profiles of Fig. 2b. Clearly, under conditions that permit such anisotropic etching, the resolution limits on pattern transfer depend only upon the lithographic technique used to generate the mask and not at all upon the plasma-assisted etching technique. This high-resolution capability, of course, is the single most compelling reason for development of such etching techniques.

The ever-increasing scale of integration on silicon chips has led to extensive development of techniques that can handle the handful of materials used in IC fabrication. Thus, single-crystal silicon, polycrystalline silicon, thermally grown and deposited silicon dioxide (doped and undoped), silicon nitride, and aluminum metalization all have been plasma-etched.

Moreover, these materials can be etched selectively in the presence of masking layers, such as organic photore-



3. Window making This contact window is etched anisotropically in a 1.7-μm thick phosphosilicate-glass layer on silicon. It has been opened in the glass dielectric to allow electrical contact between the polysilicon substrate and the aluminum conductor lines.

TABLE: PLASMA-ASSISTED ETCHING FOR IC FABRICATION

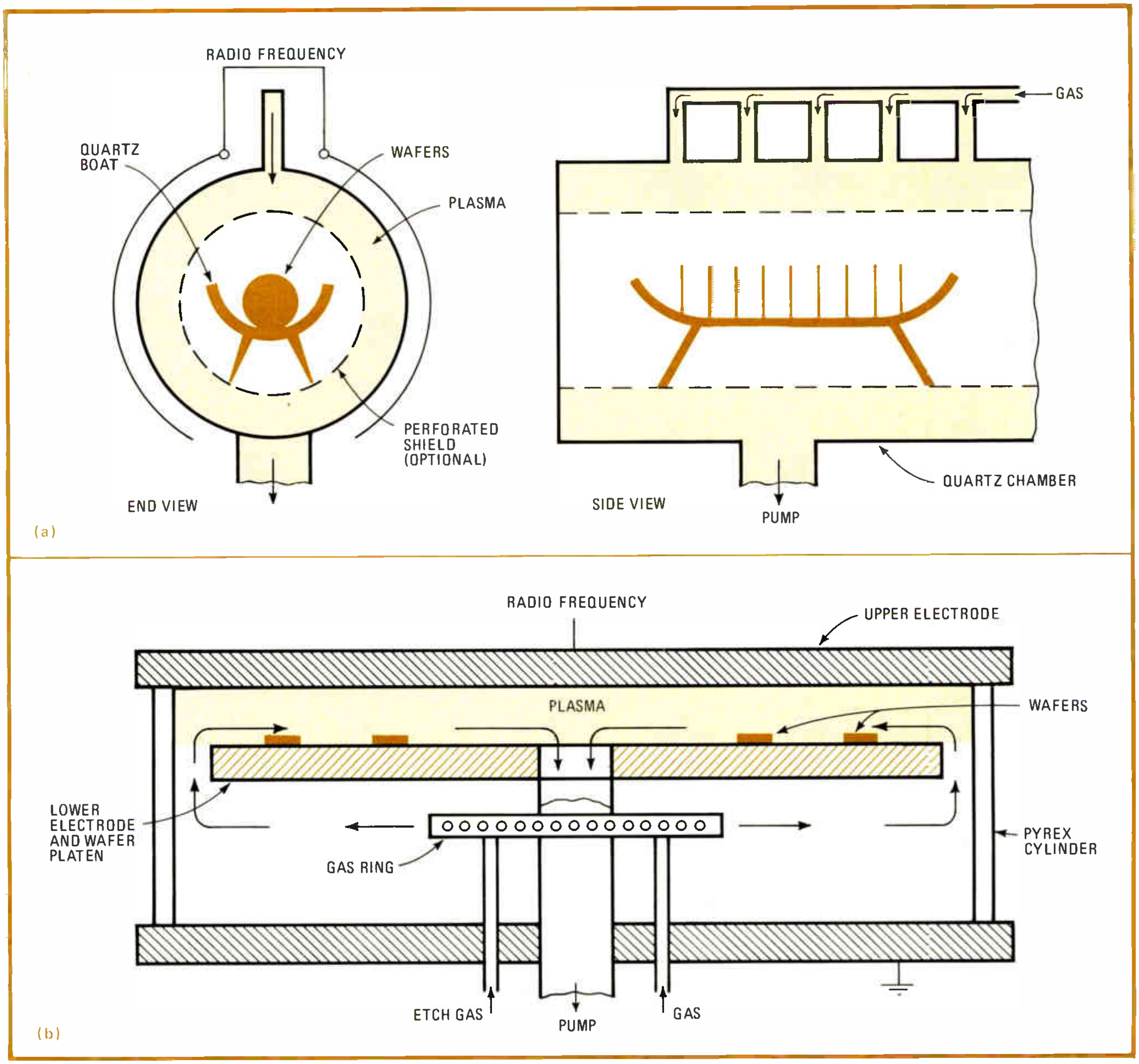
Film	Substrate	Film etch rate (Å/min)	Selectivity (etch rate ratio of film to substrate)	Resolution (edge profile)
Si_3N_4	SiO_2	300	4 : 1	isotropic
Si_3N_4	Si	700	7 : 1	anisotropic
Poly-Si	SiO_2	1,000	30 : 1	isotropic
Poly-Si	SiO_2	1,100	8 : 1	anisotropic
SiO_2 thermal	Si	600	6 : 1	anisotropic
PSG	Si	1,300	13 : 1	anisotropic
Al	SiO_2	1,000	6 : 1	anisotropic
Si N*	Al	2,000	∞	isotropic

* Plasma-deposited silicon nitride

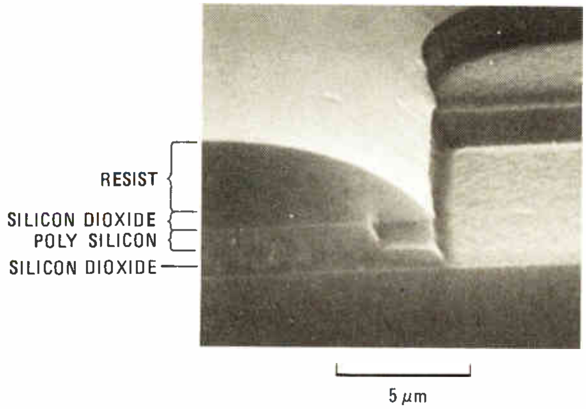
sists, and of underlying layers that are a permanent part of the multilevel IC. An important example of this selectivity is etching contact windows, typically the smallest feature to be defined in the production of an integrated circuit.

In the case of a polysilicon-gate MOS device, for instance, an intermediate phosphosilicate-glass dielectric insulates the polysilicon from the aluminum conductor lines deposited later. Windows must be opened in the dielectric to permit electrical contact to the polysilicon and to the underlying silicon substrate. Making such a window (Fig. 3) with dimensions at the resolution limit of the mask-making technique requires anisotropic etching of the phosphosilicate glass relative to the polysilicon and the silicon.

The selectivity required for the windows depends upon the thickness of the polysilicon layer and the depth of



4. Barrel vs. planar. The barrel reactor (a) is a high-throughput machine for plasma etching. However, it cannot etch either fine lines or aluminum. The parallel-plate reactor (b) overcomes these deficiencies but has a low throughput in the present models.



5. Anisotropic etching. The SiO_2 layer in this structure was intentionally undercut by overetching with a wet chemical etch in order to demonstrate the anisotropic character of plasma etching of the polysilicon layer in a Bell Systems production-line process.

junctions in the substrate. For very-large-scale integrated work, selectivity requirements naturally will be even more stringent.

The table summarizes some of the features in etching IC materials with plasma-assisted techniques. Actual etch rates depend on such system parameters as gas composition, pressure, power density, and type of plasma-assisted etching. They generally range from a few hundred to a few thousand angstroms per minute. Many materials not listed, including metals such as titanium, tantalum, tungsten, molybdenum, gold, and plantinum, and semiconductors and insulators such as germanium, gallium arsenide, carbides, nitrides, and oxides, also can be etched in plasmas.

Commercial reactors

Commercially available reactors for plasma-assisted etching are generally of two types, both generating plasma with radio-frequency power (usually 13.56 megahertz). The first type consists of a chamber with external electrodes into which wafers are stacked vertically in a suitable carrier (Fig. 4a). The chamber usually is cylindrical, accounting for the designation given this design: barrel reactor. The second type has internal electrodes and the wafers are loaded horizontally (Fig. 4b). The electrode arrangement usually is planar, accounting for this design's designation: parallel-plate reactor.

The large batch capacity of the barrel reactor is its most attractive feature and makes it ideal for such noncritical uses as photoresist stripping. However, such a reactor generally cannot be used for anisotropic etching, for etching aluminum, or for selective etching of silicon dioxide over silicon at practical rates. Thus this type cannot be used for most of VLSI's high-resolution, exacting etch operations.

Despite smaller batch capacities, parallel-plate reactors are finding increasing use in semiconductor production because they can perform high-resolution anistropic etching. Moreover, they allow greater selectivity and can do certain operations impossible with barrel reactors, such as etching contact windows and aluminum.

A particularly effective parallel-plate design is what is called the radial-flow reactor, shown in Fig. 4b. It was designed by A. R. Reinberg of Texas Instruments Inc. for uniform plasma deposition of insulator films over a large area. Its flow geometry tends to compensate automatically for the effects of gas-phase depletion and electron-density gradients.

The radial-flow principle will work equally well for etching. Parallel-plate reactors recently have become available from several commercial suppliers; however none employ the radial-flow principle exactly as developed by Reinberg.

Advantages and limitations

While plasma equipment is justly extolled by its manufacturers as dry, clean, and safe, some of the volatile reaction products are toxic and corrosive gases, which must be handled respectfully. On the other hand, the reaction products from stripping of photoresists in an oxygen plasma are primarily water, carbon dioxide, and carbon monoxide, which are much easier to handle than are the phenols or heavy-metal acids present in the commercially available wet chemical stripping agents.

Also, plasma-assisted etching is fully compatible with present photoresist technology, and resist adhesion is seldom the problem it can be with wet chemical etching. Thus it often is possible to eliminate intermediate masking layers that compensate for the lack of adhesion.

Another bonus with most commercial plasma reactors is their fully automated operation. The wet chemical processes usually are manual or semiautomatic.

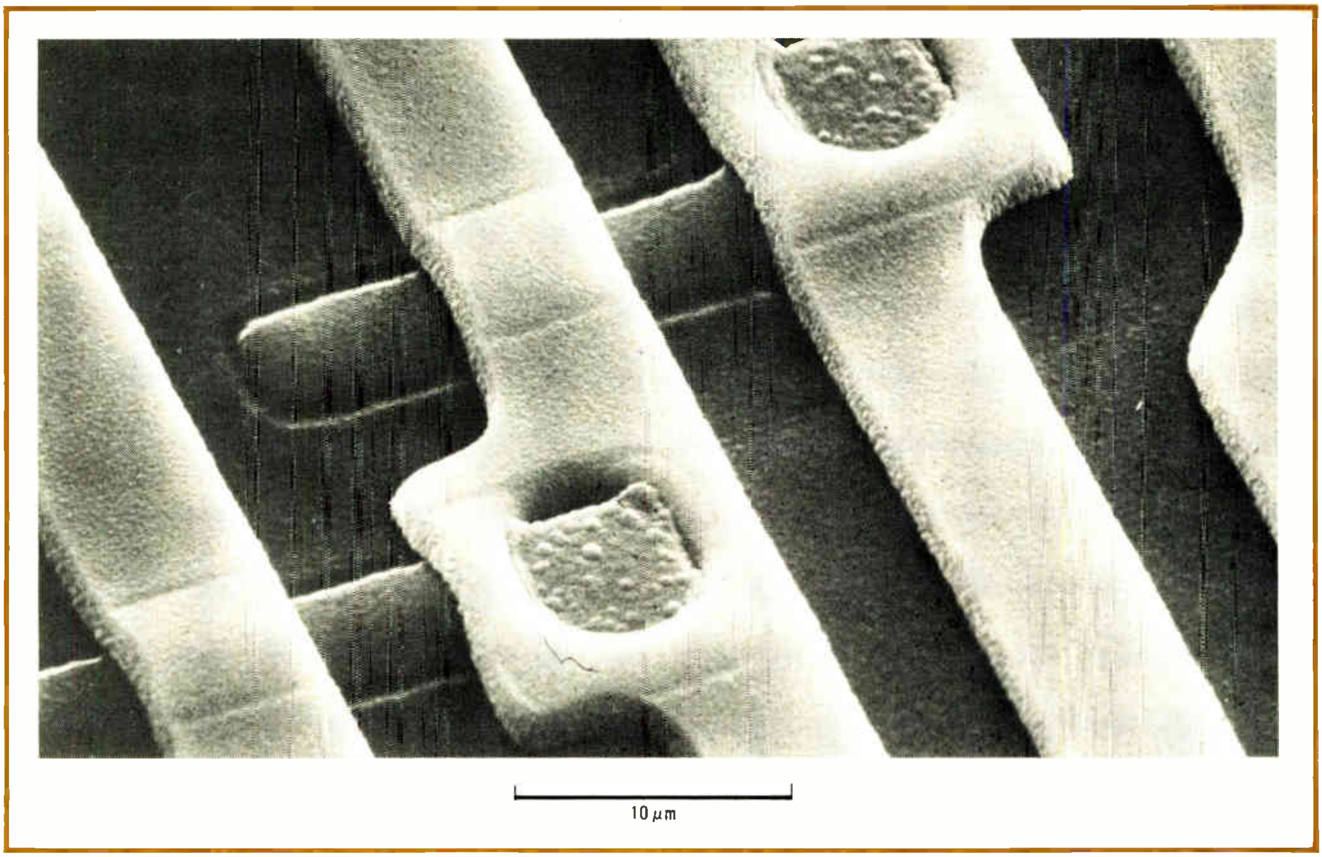
For the design and processing engineer, of course, the main advantage is the high resolution obtainable in pattern transfer. If 1-to-2-μm features can be reliably imaged in the resist, plasma-assisted etching can replicate them in silicon, polysilicon, silicon nitride, silicon dioxide, aluminum, and so on. The isotropic physical processes involved in wet chemical etching means there is now no way to obtain comparable results.

Plasma-assisted etching is not without its limitations, such as the restricted batch size in parallel-plate reactors. Moreover, with some IC materials, etch selectivity compares poorly with wet chemical etching. For example, plasma etching of silicon dioxide over silicon generally results in selectivities on the order of 12 : 1, depending on the doping levels of the constituent materials. In contrast, buffered hydrofluoric acid can give a nearly infinite etch-rate ratio.

Another problem with plasma-assisted etching can be the presence of unwanted particulates on the wafer. Wet chemical etching often is accompanied by some type of agitation, so it is less susceptible to such contamination.

Finally, plasma-assisted etching may result in damage to ICs through photon or charged-particle bombardment. This type of damage tends to vary from one level of the device to another and has not been fully characterized yet. Fortunately, it often can be annealed in the standard furnace operations found in production.

Plasma-assisted etching at Bell Laboratories and Western Electric Inc. generally reflects use throughout the electronics industries. G. K. Herb of Bell Labs has developed production processes for chip separation,



6. Etching aluminum. A recent development in plasma etching is the introduction of plasma reactors that can etch aluminum. These anisotropically plasma-etched aluminum conductors are on a 16-K MOS dynamic random-access memory used in Bell System equipment.

using commercially available barrel reactors. They also are used to strip photoresist and clean substrates during processing. Parallel-plate reactors have been used for several years to isotropically etch silicon nitride and polysilicon.

Anisotropic etching at Bell

More recently, Western Electric has begun anisotropic plasma etching in IC manufacture. For the past year, plasma etching has been used to define contact windows in PSG on a 16-K n-channel MOS random-access memory manufactured for Bell System applications.

Plasma-assisted etch technology also has been extended into new areas. R. A. Porter of Bell Labs has developed an anisotropic etching process for polysilicon (Fig. 5), now being introduced on production lines. D. B. Fraser of Bell Labs has developed anisotropic etching of aluminum films, also being introduced into manufacture (Fig. 6).

Evaluation of these new etching processes generally discloses that, for devices with large design rules of 6 to 8 μm, yields and reliability are not significantly different than with wet chemical etching. However with 2-to-5-μm design rules, with their tighter dimensions and tolerances, there is no comparison between the two. Devices and structures beyond the capabilities of wet chemical processes are routinely manufactured with plasma-assisted techniques.

Several developments may be expected in plasma-assisted etching for semiconductor processing. First of these are improvements in commercial equipment, such as scaled-up parallel-plate reactors for bigger batch sizes. Also coming are novel reactor designs with high throughput capability. In-line wafer handling with serial, rather than batch, wafer handling is the next step in this evolutionary process and should appear soon.

Improvements in the etching of some materials will be made to increase marginal selectivities. Control over resist erosion for particularly sensitive materials such as electron resists will improve, making plasma techniques fully compatible with the most advanced lithographies. Moreover, plasma-assisted etching will expand into technologies other than silicon: III-V-compound semiconductors, magnetic-bubble devices, integrated optics, etc.

Flexible edge profiles

Better understanding of the influence of charged particles on the development of edge profiles during etching in reactive gases may ultimately permit complete flexibility in controlling these profiles, producing variable tapers as well as straight walls.

Finally, as designers and process engineers become more familiar with plasma processing, they will evolve new sequences to exploit its advantages. To date, plasma etching has been used merely as a one-to-one replacement for wet chemical etching in the etching and stripping of thin films. However, the ability of plasma-assisted etching to produce anisotropic plus isotropic etch profiles should lead to the fabrication of device structures impossible with wet chemical etching. □

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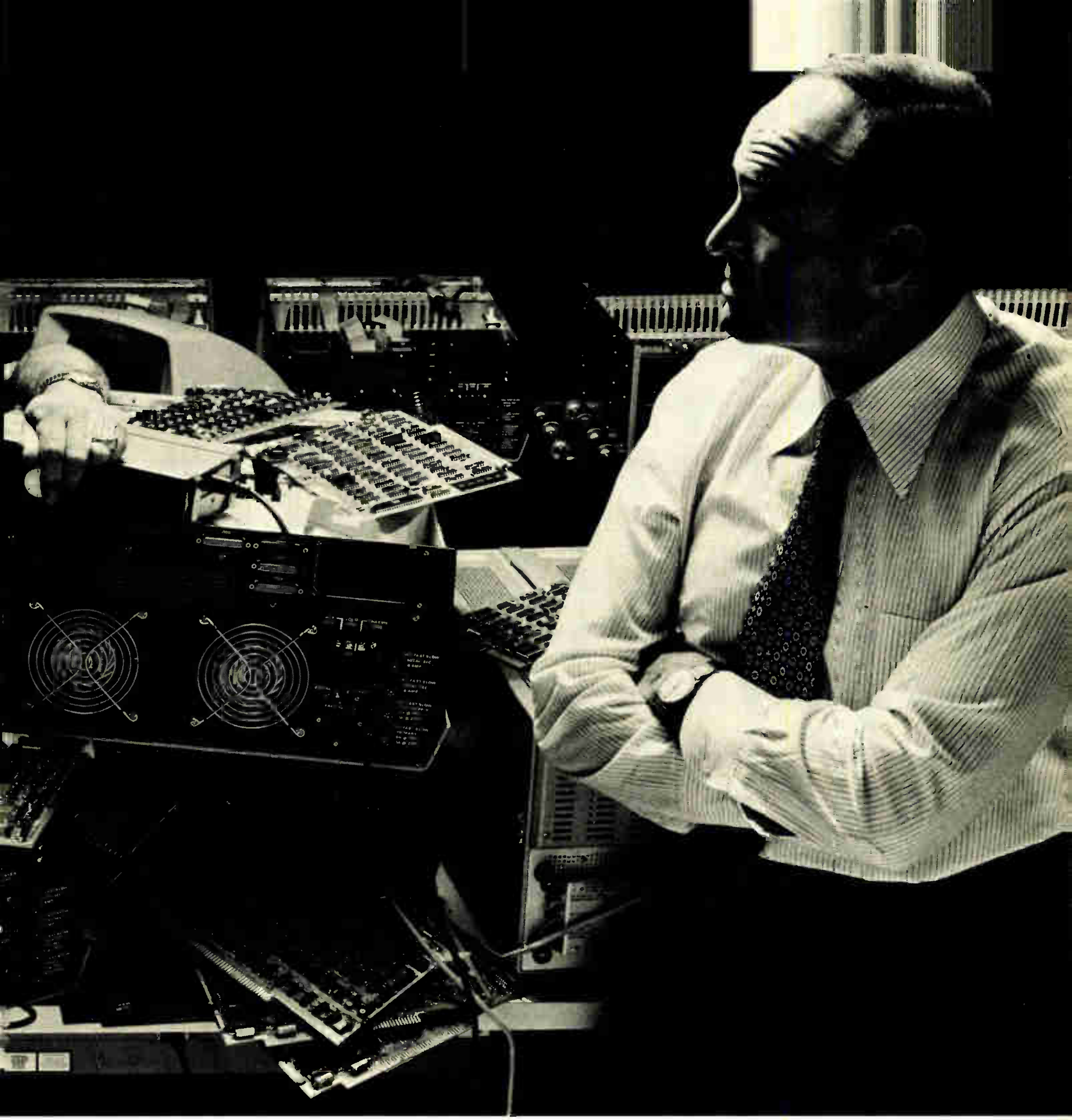

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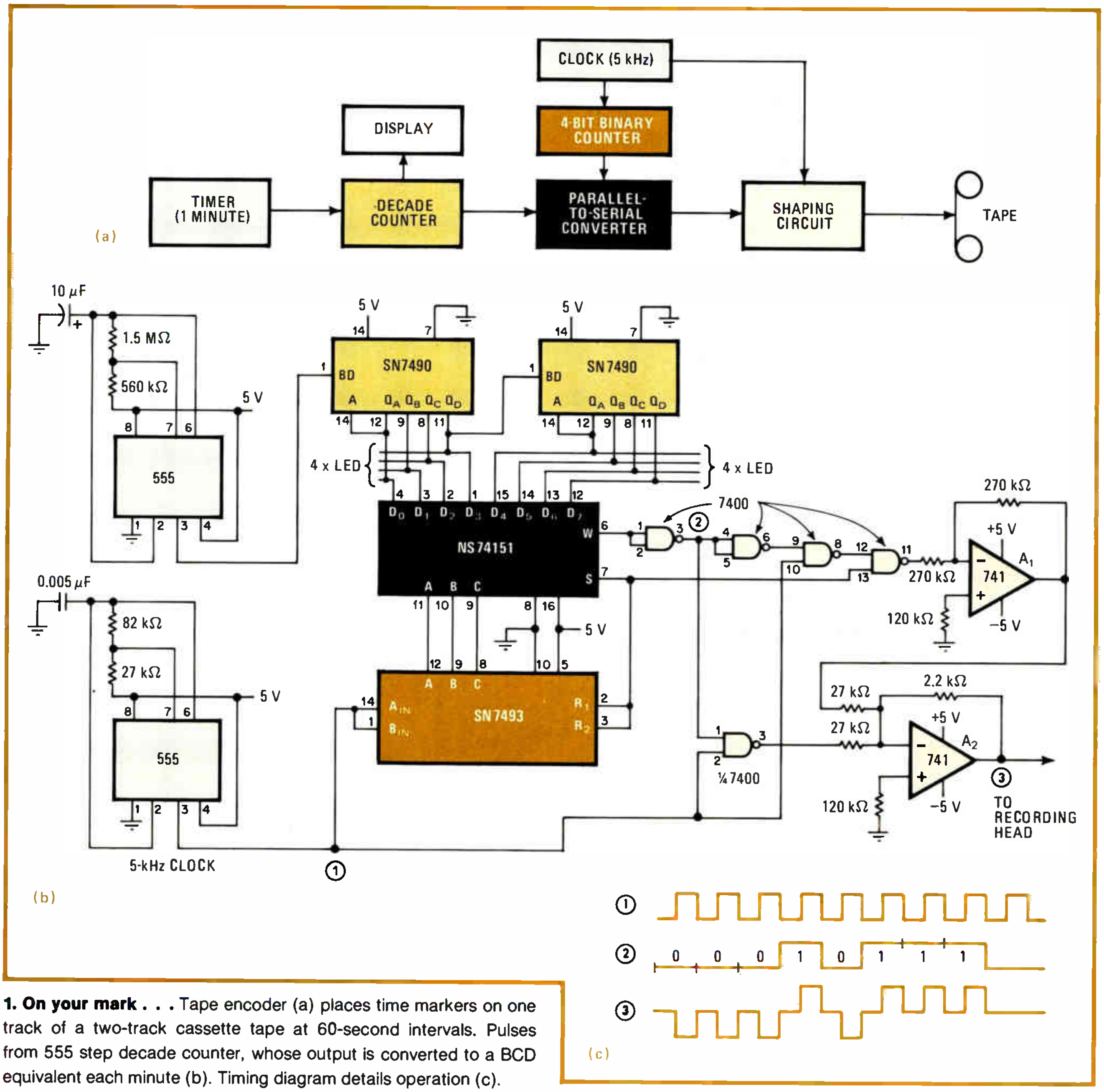
THE MICROSYSTEM ANALYZER

Time-encoding system formats cassette tapes

by Fathi Saleh and Benham Bavarian
Abadan Institute of Technology, Abadan, Iran

Using operational amplifiers and standard digital elements to place 1-minute markers on a stereo cassette tape, this formatter is extremely useful when implemented in simple data-recording and control systems. Also shown here is a rudimentary decoder circuit, and the information required to utilize the markers for controlling any cassette's stop, play, fast forward or rewind functions for more advanced systems.

Figure 1a gives the block diagram of the tape formatter, which was used with the JVC MC-1820R recorder. The timing signals are recorded at the expense of one track of the tape, leaving the other track for monaural sound or data recording. It might have been possible to add a thin head to the recorder in order to record marker signals and at the same time make possible two-channel



1. On your mark . . . Tape encoder (a) places time markers on one track of a two-track cassette tape at 60-second intervals. Pulses from 555 step decade counter, whose output is converted to a BCD equivalent each minute (b). Timing diagram details operation (c).

data recording, but this was not tried.

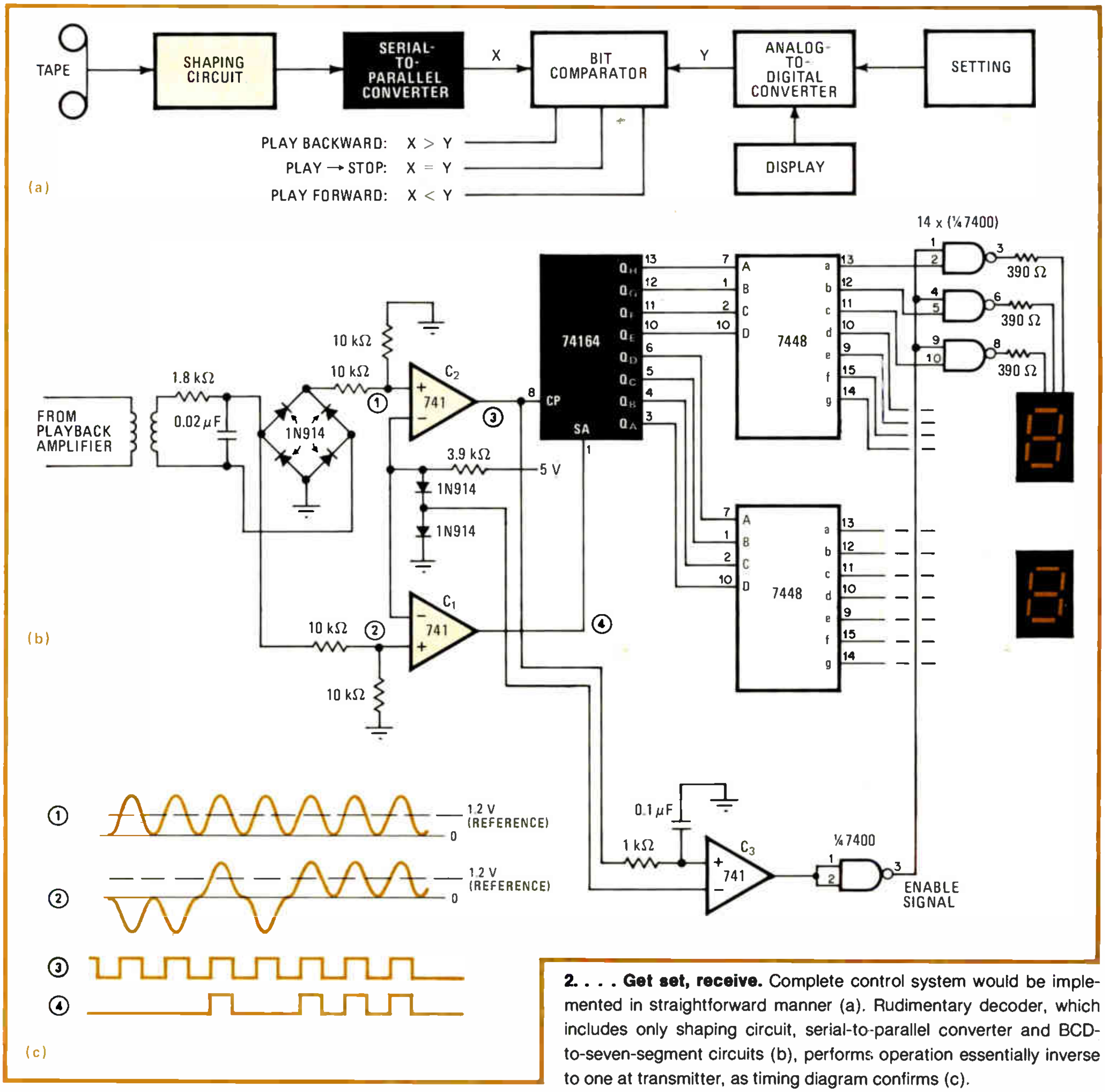
As shown in Fig. 1b, the recording system uses a 555 timer to generate a pulse every 60 seconds, two 7490 decade counters that are stepped by the timer to yield required 8-bit patterns, eight light-emitting diodes to monitor the number generated, a parallel-to-serial converter (74151) that is clocked at 5 kilohertz by a second timer, a 4-bit counter (7493), and shaping circuitry.

Pulses emanating from the 1-minute timer advance the 7490s. The output of these devices is introduced to the 74151, which is being clocked at a 5-kHz rate through the 7493. The output of the 74151, after passing through a NAND gate, appears as shown in the timing diagram (Fig. 1c).

Recombining the 5-kHz clock with other summing-circuit (A_1) signals yields an output at A_2 having a 50% duty cycle. This output returns to a logic 0 when the output from the 74151 is a logic 1 and moves high for a logic 0 output from the 74151. The signal is a two-digit binary-coded-decimal character which advances from 0 to 60 minutes. The return-to-zero format is used here so that one may differentiate between the zero-state and the no-signal levels. This format also simplifies the design of the decoding circuits.

The playback (decoder) circuit is shown in Fig. 2. The block diagram (Fig. 2a) shows a complete control system, but the system, although straightforward, encompass more circuitry than can be shown here.

The basic decoder is shown in Fig. 2b. Passing through the shaping circuit is the output from the tape recorder. This input signal is compared with a 1.2-volt reference at C_1, enabling the original bit pattern recorded to be recovered at its output. Meanwhile, the original clock



2. . . . Get set, receive. Complete control system would be implemented in straightforward manner (a). Rudimentary decoder, which includes only shaping circuit, serial-to-parallel converter and BCD-to-seven-segment circuits (b), performs operation essentially inverse to one at transmitter, as timing diagram confirms (c).

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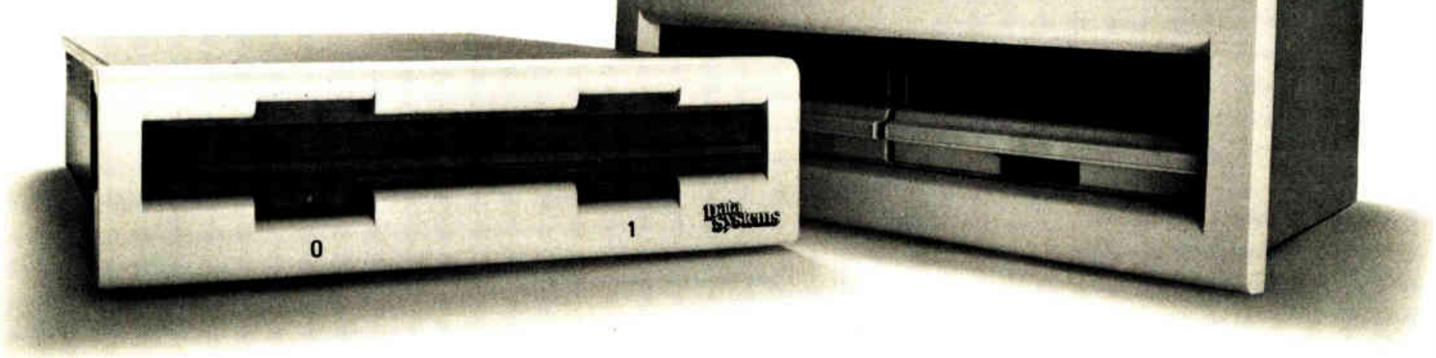

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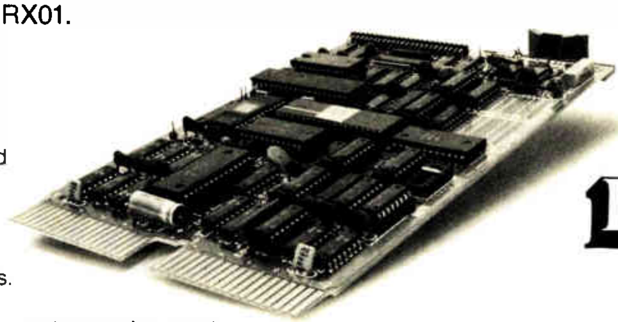

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pulses are regenerated at C_2 by comparing the rectified 1s and 0s of the bipolar return-to-zero input signal with the 1.2-v reference. The bit pattern output from C_1 is connected to the 74164 serial-to-parallel converter, which is stepped by the output of C_2.

Thus the output of the 74164 is a binary-coded-decimal equivalent of the marker-input's value. The seven-segment displays that follow indicate the time, in minutes, corresponding to the last marker detected. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published.

Digital logic multiplies pulse widths

by N. Bhaskara Rao
U.V.C.E., Department of Electrical Engineering, Bangalore, India

Using logic elements to multiply the width of incoming pulses by a value selected by the user, this circuit is simple to build and provides a higher accuracy-to-cost ratio than its analog counterpart. It should therefore find numerous uses in synchronous systems, and although its prime function is to provide a multiplication factor of greater than unity, it can generate smaller values as well.

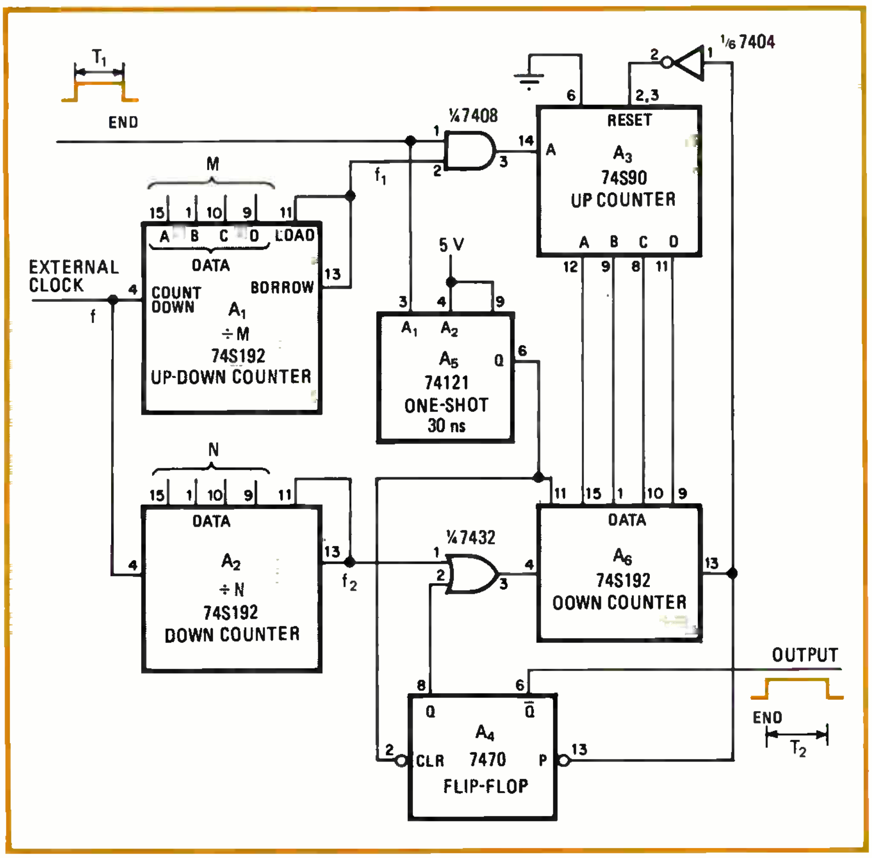
The figure will help make circuit operation clear. The multiplication factor is selected by presetting two 74S192 down counters, A_1 and A_2. Initially, counter A_1 is set to a value, M; A_2 is preset to a second value, N; A_3 is zero; and the Q output of flip-flop A_4 is high.

An incoming pulse of width T_1 (the signal to be multiplied) switches on the 7408 AND gate and enables A_3 to count to a number determined by f_1, which is derived from an external clock having input frequency f. Thus, at the end of the pulse, the counter contains the number f_1T_1. Note that $f_1 = f/M$.

When the trailing edge of the pulse arrives, A_5 is triggered and presets A_6 with the number contained in A_3. Meanwhile, A_4 is cleared (Q=0) by A_5, and the OR gate is thereby activated so that counter A_6 can initiate counting from its preset value. Note that A_6 is driven by A_2, the divide-by-N down counter, and that $f_2 = f/N$.

The time taken for A_6 to reach zero from its preset value is thus $T_2 = (f_1/f_2)T_1 = (N/M)T_1$. At this time, the output from A_6's borrow port clears A_3 and presets the flip-flop. Therefore the time between the flip-flop's move to logic 0 (at the trailing edge of the input pulse) and the time its Q output moves high again is T_2.

The output signal is not derived until the input pulse's trailing edge arrives. The multiplication factor, N/M, can thus be set to any value greater or less than unity because the conversion is carried out after a delay. Needless to say, f should be much greater than T_1 for accurate pulse-width multiplication. □



Width multiplier. Circuit has no analog elements. Multiplication factor is determined by ratio of N to M, set by user. A_6 is preset to f_1T_1; stepped to zero at f_2 rate, it signals flip-flop. Time between state changes of flip-flop is $T_2 = (N/M)T_1$.

Introducing the Z8, part 1:

One-chip microcomputer excels in I/O- and memory-intensive uses

Data/address lines are multiplexed with input/output lines to increase addressing capability and enhance throughput

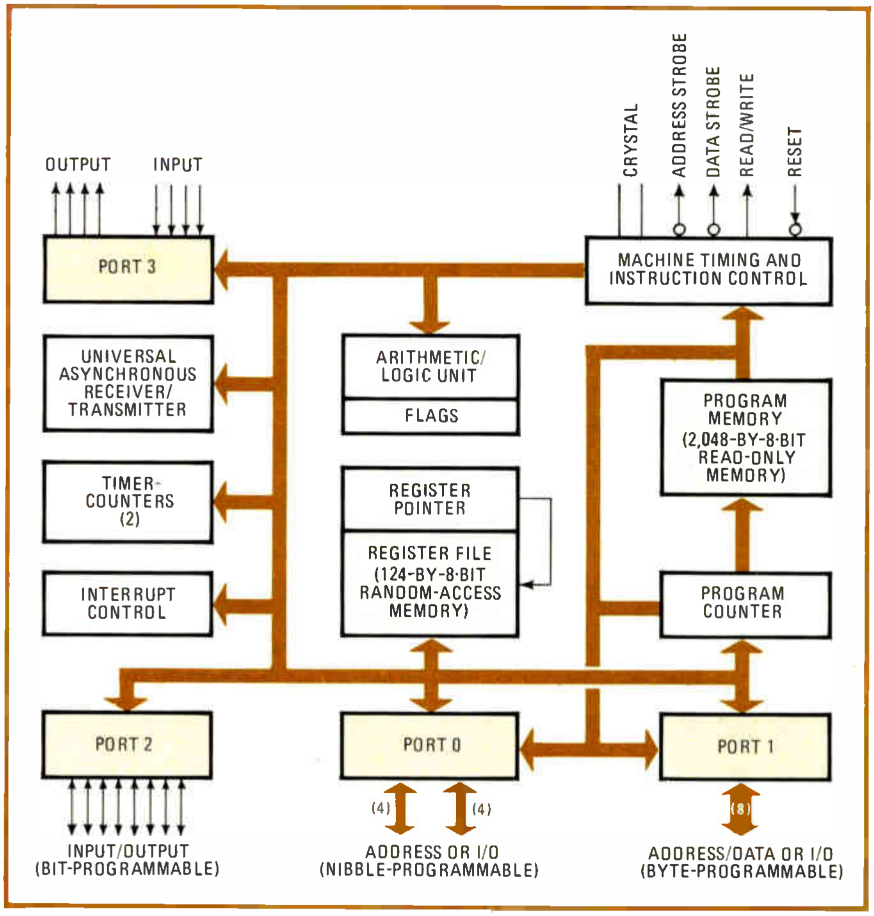
by Bernard L. Peuto and Gary J. Prosenko, *Zilog Inc., Cupertino, Calif.*

☐ Eight-bit microprocessors have increased in performance and sophistication, but they have taken one of two different paths in doing so. On the one hand, some have evolved into single-chip microcomputers that emphasize input and output efficiency to the extent that they often function as microcontrollers. Others, meanwhile, have improved as microprocessors—that is, memory-intensive machines for crunching numbers and manipulating data.

Although each type is suited for particular applications, it is desirable that, ultimately, one architecture serve both needs. Zilog Inc. has developed just such an architecture for its 8-bit single-chip microcomputer. The Z8, in fact, can serve as either an I/O-intensive microcomputer or as a memory-intensive microprocessor.

To achieve its dual capability, the Z8 addresses external memory while maintaining as many I/O lines as possible—its multiplexed address-data bus shares pins with I/O port lines. With half of its 32 lines also available under software control to address external memory, the Z8 can expand its address space to a maximum of 131,072 bytes while retaining 15 lines of I/O.

But to serve equally as an I/O-intensive microcomputer and a memory-intensive microprocessor, the Z8 must also support the many different addressing spaces required by both. This goal has been achieved by separating some spaces, such as external program memory and external data memory, and merging others, such as the I/O buffer storage and the register file.



1. Memory meets I/O. Zilog Inc.'s single-chip 8-bit microcomputer, the Z8, is both an input/output-intensive microcontroller and a memory-intensive microprocessor. Half of its 32 I/O lines can be programmed as multiplexed address/data lines for adding external memory.

Included on the Z8's 221-by-223-mil chip are an enhanced central processing unit that runs at an internal clock rate of 4 megahertz from an 8-MHz crystal (most instructions are executed in 1.5 to 2.5 microseconds), 2,048 bytes of read-only memory for program storage, 144 bytes of random-access memory forming the register file, a universal asynchronous receiver/transmitter, a pair of 8-bit timer-counters, and six vectored interrupts (Fig. 1).

The register file

The Z8's register file resembles that of a computer, and this architectural regularity is the key to several of the device's unique capabilities. The 144-byte file, shown in Fig. 2, comprises 4 I/O-port registers, 16 status and control registers, and 124 general-purpose registers.

The I/O-port and control registers are included in the register file to allow any Z8 instruction to process I/O data or control information, thus doing away with the need for special I/O or control instructions. Also, each of the general-purpose registers can serve as an accumulator, an address pointer, or an index register, thereby simplifying programming.

Instructions can access registers or register pairs either directly or indirectly with an 8-bit address field. What's more, the Z8 can designate registers using a 4-bit address field, which saves bytes and speeds program execution and task switching. In this mode, the register file is divided into nine groups of 16 working registers each. A register pointer, one of the status and control registers, determines the group being accessed; the 4-bit address field then specifies the register within the group.

The first and last group have special significance. The first includes the four I/O-port registers. Setting the register pointer to this group makes possible fast I/O processing. The last group includes all the status and control registers for I/O-port operation, timers, serial interfacing, and interrupt control. Again, the short format for addressing these registers can greatly simplify those sections of a program that establish or change system configuration.

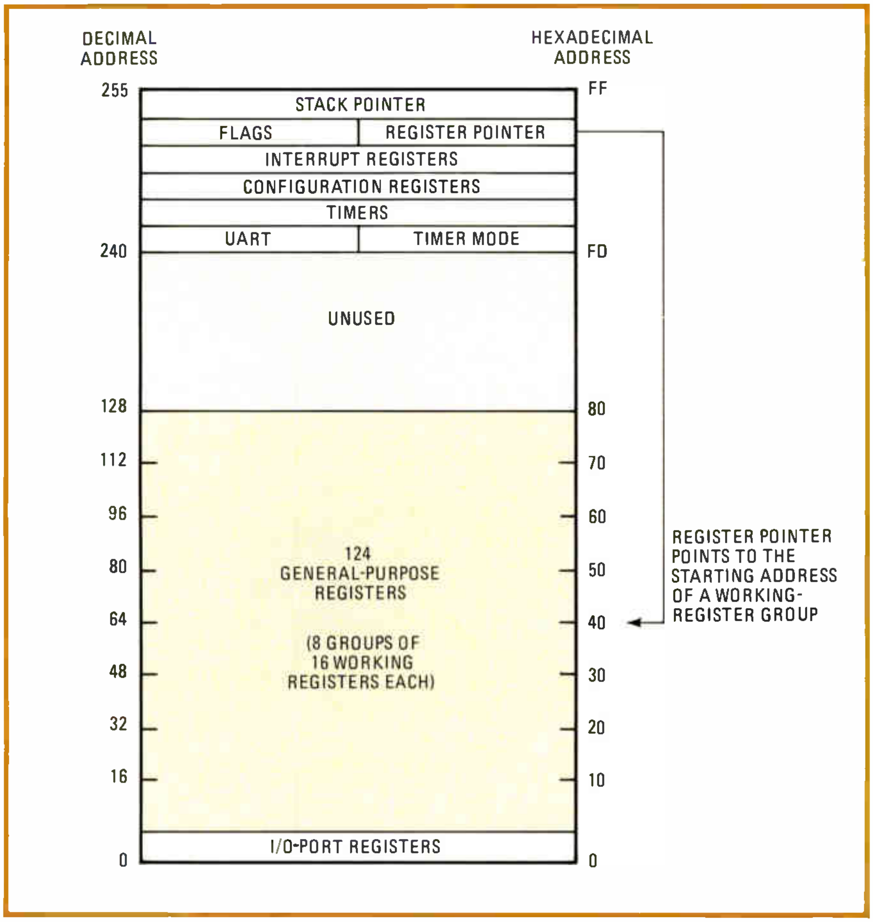
The Z8's 32 I/O lines are software-configurable for either input or output and have active pull-ups and pull-downs to make them compatible with transistor-transistor-logic loads. The lines are grouped into four 8-bit ports, two of which may be programmed to serve additionally as multiplexed address/data lines, as noted earlier.

Flexible I/O

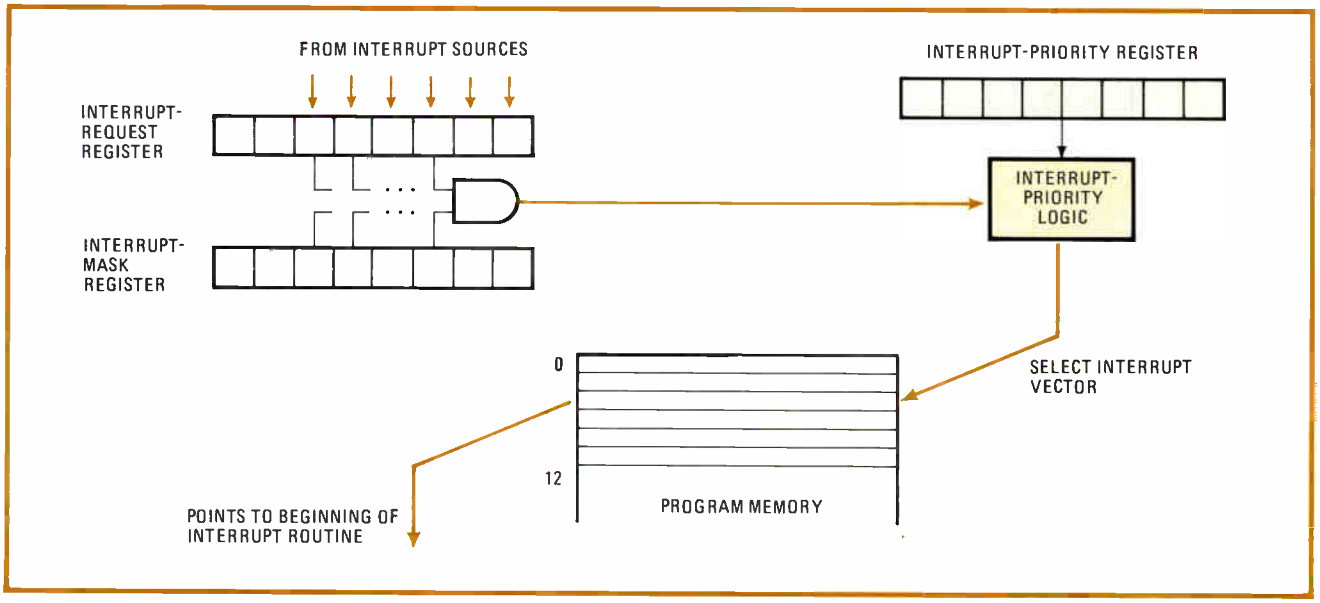
The I/O ports are treated internally as general-purpose registers mapped into the register file, allowing I/O data to be manipulated directly by any instruction. In I/O-intensive applications, this mapping ensures fast and efficient I/O transfers.

In order to manage both memory- and I/O-intensive applications, the ports are configurable in a variety of ways:

- Port 0 can be split into two 4-bit nibbles, either of



2. Merged storage. The Z8 has 124 general-purpose registers, 4 I/O-port registers, and 16 registers for status and control. Four-bit nibbles can also address registers, since the file is divided into nine groups of 16 locations each. The register pointer identifies the group to be accessed.



3. Interruptions. The Z8's six vectored interrupts are individually or globally maskable and can be assigned priorities by software. The output of the priority-determining logic points to a vector in program memory that corresponds to the interrupt request being serviced.

which can be programmed as input, output, or external-memory address.

■ Port 1 can be programmed as a byte-wide I/O port and as a multiplexed address/data port for interfacing external memory.

■ The eight lines of port 2 can be programmed bit by bit, either as inputs or outputs. The output buffers of this port can have their pull-ups disabled by software as an option to provide open-drain outputs for applications such as keyboard scanning.

■ Port 3, fixed to four inputs and four outputs, functions as either an I/O port or a control port. Two lines can also be programmed to function as a full-duplex UART. The control functions of port 3 are handshaking, interrupt request, timer in and out, and status out.

Communicating serially

The ability to communicate serially is important in a microprocessor, since a distributed control system in effect requires such communication between local control stations, as well as to a central controller. The Z8's UART provides a simple and efficient means of serial communication, unburdening the CPU from bit manipulation and therefore saving software. Data rates as high as 62.5 kilobits/second (crystal frequency ÷ 128) are controlled by an on-board timer, using two lines of port 3 for serial I/O.

The UART also provides programmable odd parity. Eight bits are always transmitted. If parity is selected, the eighth bit becomes the parity bit; when parity is on, the byte that is read contains a parity error flag instead of the original parity bit.

An interrupt request is generated whenever a character is transferred into the receiver buffer. Although the receiver is double-buffered, it is not protected from overwriting. A transmitted character also generates an interrupt request, and the transmitter buffer, too, is not protected from overwriting.

To free timing and counting functions—so often needed in real-time control applications—from software routines, the Z8 offers a pair of 8-bit counters, each with its own 6-bit prescaler. Each counter accepts a maximum input frequency of 1 MHz, derived internally from the clock or supplied externally. The dividing range of the prescaler (1 to 64), combined with that of the counter (1 to 256), allows a timing interval that ranges from 1 microsecond to 16,384 milliseconds. Of course, the two counters may be cascaded, which extends the timing range to more than 537 seconds.

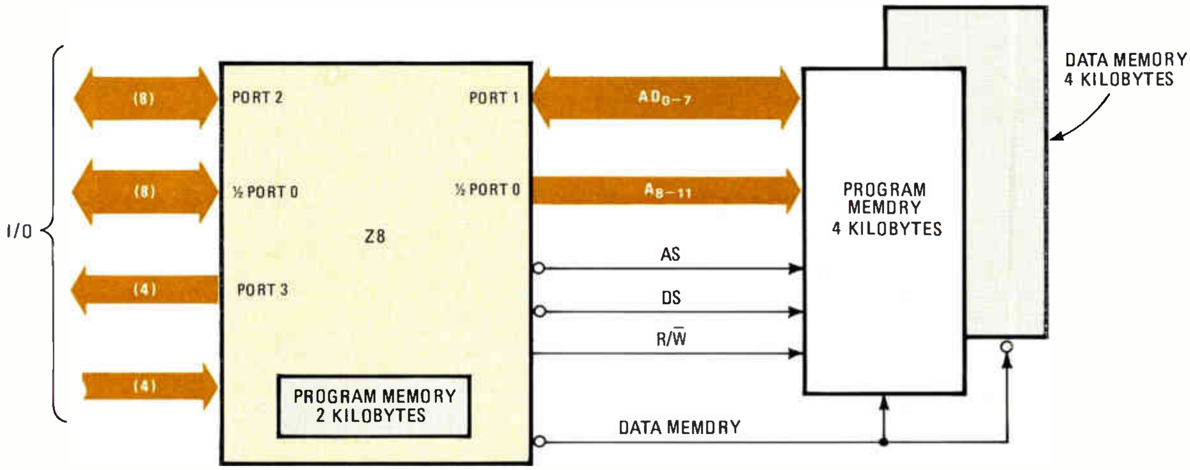
The counter-timers have several modes of operation: a regular clocked mode as described, a gated mode for period measurement, and both retriggerable and nonretriggerable modes.

There are two methods by which a controller receives a peripheral device's call for service—by polling or by getting interrupt requests—and the Z8 can do both. Its six vectored interrupts are assigned priorities and masked by software. There are three sources for interrupts: four input pins of port 3, one from each of the two timers, and one each from the UART's input and output. Interrupt requests are stored in an interrupt-request register that can also be used for polling.

Interrupts

Each of 6 bits in the interrupt-mask register corresponds to an interrupt, allowing them to be disabled individually. A seventh bit disables all the interrupts. When more than one interrupt is pending, a priority encoder, controlled by an interrupt-priority register, establishes the order of the requests. The output of the priority encoder is an address that points to a vector stored in program memory associated with the interrupt request being serviced. When an interrupt source is masked, the user can poll the source of the interrupt by testing the interrupt-request register.

When an interrupt request is granted, the Z8 enters an interrupt machine cycle that disables all other interrupts, pushes the program counter and flags onto the stack, and



4. Medium-memory microcomputer. Both the separation of address spaces and the instructions that access them are geared to medium-sized systems. This 10-kilobyte configuration—6 kilobytes for program and 4 for data—requires only 12 address and 4 control lines.

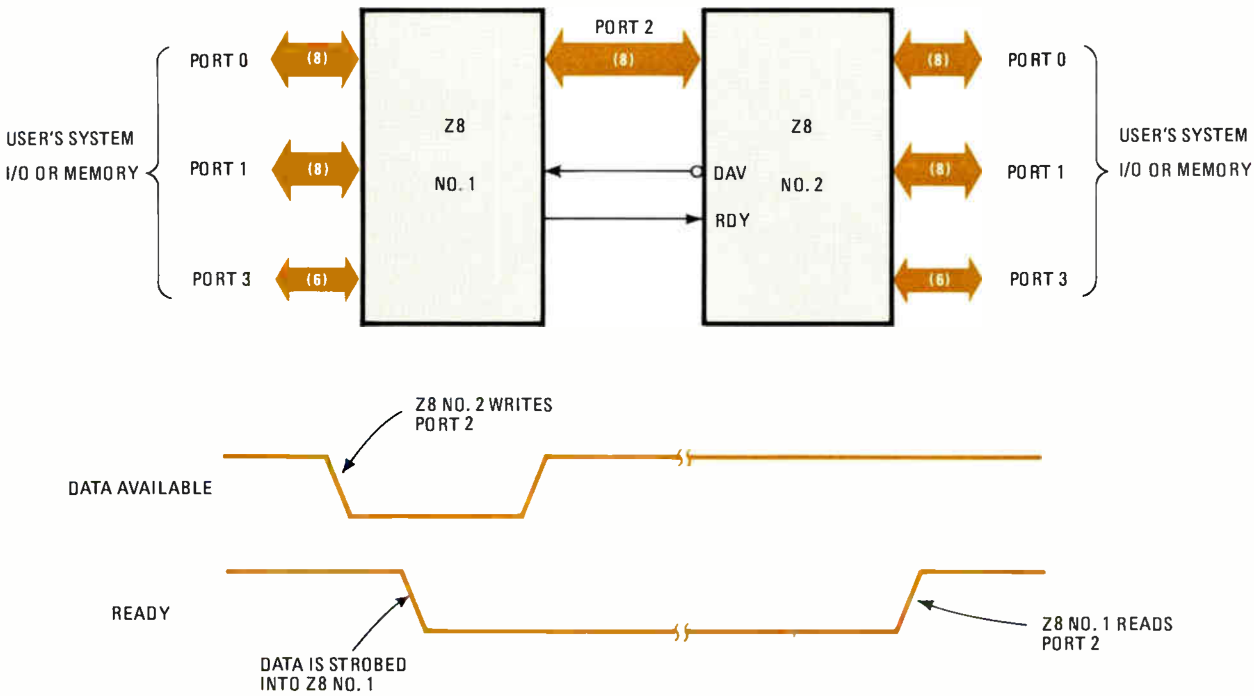
Handshaking with the Z8

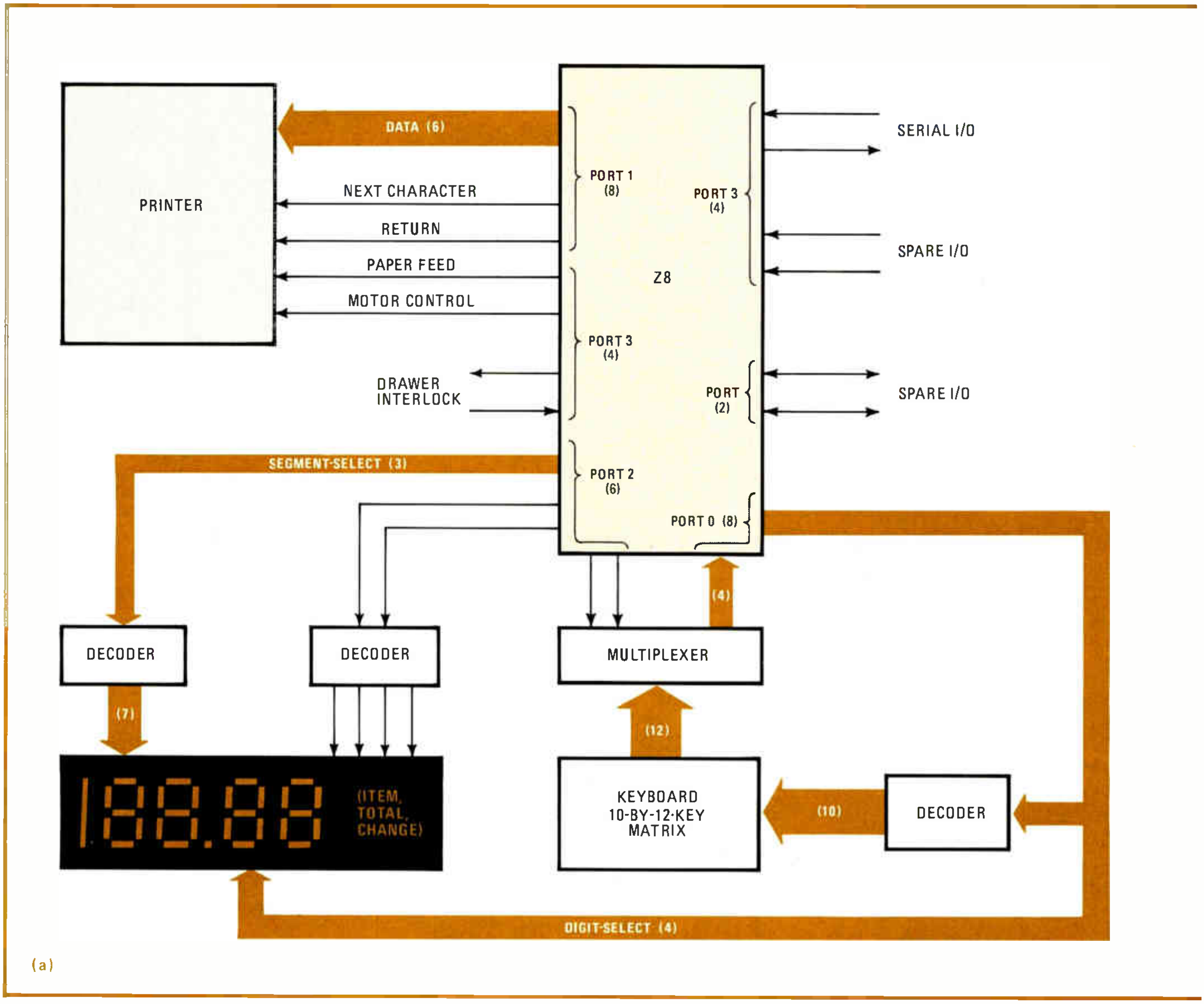
With the growing popularity of distributed systems, whether for interconnecting several pieces of equipment or for partitioning the chores within a given unit, the ability to connect processors in a fully interlocked handshake is extremely important. The Z8 lends itself well to such a hookup, with port 3 dedicated under program control as the handshake lines for the remaining ports, 0, 1, and 2 (see figure). The handshake allows complex communication between Z8s—that is, between computers or between a computer and its peripheral elements.

Referring to the figure, suppose the direction for half-duplex transfer is from Z8 No. 2 to Z8 No. 1. Z8 No. 2 writes data to its port, forcing the data-available line (D̄ĀV̄) low, and this condition strobes data into Z8 No. 1 and causes an interrupt request. When data is latched, Z8 No. 1's ready line (RDY) goes low. This transition in turn causes an interrupt request of Z8 No. 2 signifying that the transfer is complete.

As long as RDY is low, no further data can be strobed into Z8 No. 1. RDY's low state allows D̄ĀV̄ to go high on Z8 No. 2. When Z8 No. 1 reads its input port, RDY returns high if D̄ĀV̄ is high, completing the handshake.

The direction of communication can be reversed under software control.





5. POS system. This distributed point-of-sale system uses the Z8 as both local processor and host. Z8s in each terminal (a) control printers, display, and keyboard and perform calculations. They also communicate serially with the central Z8 (b), which interfaces with a floppy disk.

then branches to the location specified by the associated vector. It is only then that control is given to the user's interrupt-service routine, as shown in Fig. 3.

Interrupts may be re-enabled either by software during the interrupt-service routine to allow for nesting (interrupts within interrupts) or automatically at the end of the routine by executing an interrupt-return instruction, which also restores the program counter and the flag register.

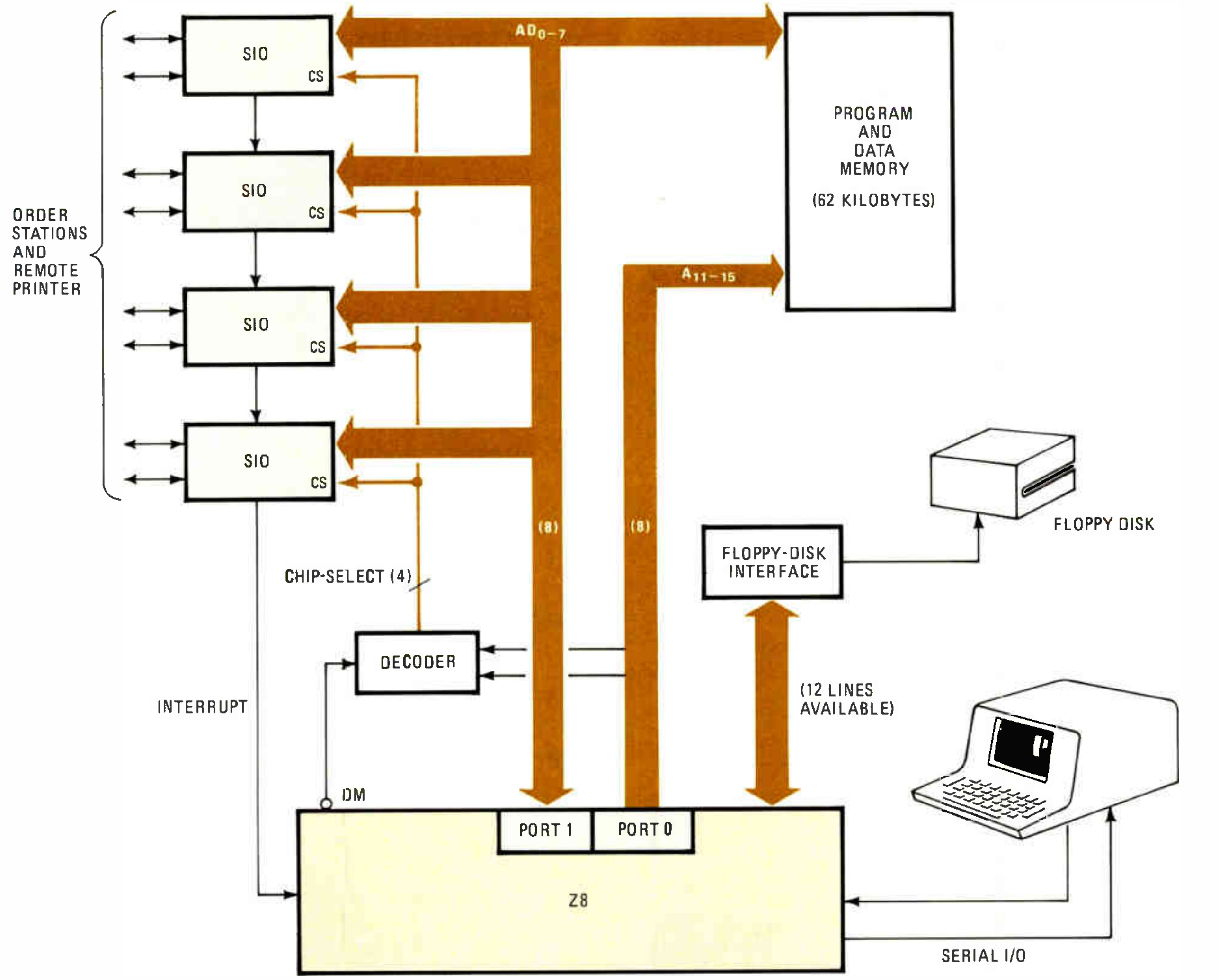
Need more memory?

When more than the 2 kilobytes of internal program memory are needed, the Z8 can address up to 63,488 bytes of external ROM. What's more, there is a separate space allotted for external data memory—up to 63,488 bytes of additional RAM can also be addressed.

The two external memory spaces can be addressed as a single space or as two individual 63-kilobyte spaces. The address-space separation and the instructions used to access them were designed to optimize the Z8 for medium-sized memory applications. As shown in Fig. 4, up to 10 kilobytes of memory—6 kilobytes for program and 4 for data—can be addressed with only 12 address lines and the control lines.

The logical addresses of external memory are from 2,048 to 6,143. Addresses always appear on the 12 external address lines, but when program references are made to the internal memory (0 to 2,047) the data-select ($\overline{DS}$) and read/write (R/$\overline{W}$) lines are inactive. References made to external memory between 2,048 and 6,143 put the 12 low-order bits on the 12 address lines and substitute $\overline{DS}$ and R/$\overline{W}$ (both active) for the 13th bit.

The data-memory line ($\overline{DM}$) separates external program and data memory. In the example in Fig. 4 (10 kilobytes of external memory) for instance, if this line is not used the two external memory spaces are merged into a 6-kilobyte program memory, with the upper 4 kilobytes also usable for data memory. For small memory applications (up to 512 bytes externally), 8 bits of address are used; for large memory applications (up to



(b)

124 kilobytes externally), 16 address bits are used.

The flexibility of the Z8 is demonstrated in a fast-food point-of-sale system in which several ordering stations feed a central accounting computer and order-logging devices (Fig. 5). Each ordering station uses a Z8 in an I/O-intensive mode to control a keyboard, a 4½ digit display, and a printer.

A point-of-sale system

Transactions are entered on the keyboard and the item's cost is displayed. The total cost, including taxes, and the change due are computed locally, displayed, and printed. The Z8's on-chip UART transfers the transaction to the central computer for processing.

The central computer is a memory-intensive application of the Z8, which acts as a small-business computer controlling several peripherals and up to 62 kilobytes of external memory. It supplies prices, tax rates, and inventory information to the ordering stations and performs inventory control and general accounting functions. Transactions are transferred to it through serial I/O controller chips (Zilog SIOs) and placed in external memory until processed and stored permanently on a floppy disk. Interaction with the central computer is through a standard serially connected terminal.

Development support

Program development for the Z8 can be carried out on Zilog's MCZ or ZDS development systems, for which a Z8 assembler and software simulator complement the standard editor, file system, and operating system.

Hardware support takes the form of an evaluation board and a system analyzer. The evaluation board is the inexpensive prototype kind, whereas the analyzer is a sophisticated self-contained unit that offers hardware and software development, measurement, and fault-diagnosis capabilities. Both can communicate with the MCZ system.

As an additional aid, the Z8 is also available in a 64-pin prototype package, which allows program development in external memory. In this version, the bus lines to the external ROM are brought out of the package, ensuring that mask-programmed parts will perform without error when delivered.

Introducing the Z8, part 2:

Rich instructions, nine addressing modes make coding easy

by Charles Bass, Judy Estrin, and Bernard L. Peuto, *Zilog Inc., Cupertino, Calif.*

□ The programmability of microprocessors has improved significantly over the last few years, and for good reason: with software development costs steadily rising, a rich, regular instruction set counts almost as much as basic chip cost in evaluating microprocessors. Furthermore, throughput most certainly depends on the kinds of instructions offered.

The speed and byte efficiency of Zilog Inc.'s Z8 single-chip microcomputer result largely from its powerful instruction set (Table 1). The Z8 processes bits, bytes, and 16-bit words using 129 instructions that combine 47 basic types with nine addressing modes. Most instructions are executed in 6 to 10 machine cycles, which, for the Z8's 4-megahertz internal clock, equals 1.5 to 2.5 microseconds. The longest instruction requires only 20 cycles, or 5 μs.

Three areas for program instruction and data storage are available in the Z8: an on-chip 2,048-byte read-only memory that can be expanded to 64 kilobytes externally, an internal 144-byte register file, and up to 62 kilobytes of external data memory. These separate address spaces, combined with the instruction repertoire and its various addressing modes, provide exceptionally dense program encoding, saving memory space, and increased data throughput, improving execution speed.

The PLZ/ASM language

The assembly language for the Z8, PLZ/ASM, is a blend of high-level data declarations and control structures from the PLZ high-level language with conventional assembly-language instructions. This mixture provides a balance between desirable programming practices (the result of high-level language) and machine-dependent operations (assembly language). The control statements available in PLZ primarily generate test and branch instructions that do not interfere with the programmer's control of register values or condition codes. An ideal use of PLZ/ASM avoids assembly-code versions of branches altogether.

The assembly notation outlined in Table 2 uses the

TABLE 1: AN OVERVIEW OF THE Z8 INSTRUCTION SET

- **Load.** Clear, load, load constant, load external, pop, push.
- **Arithmetic.** Add, add with carry, decimal adjust, increment byte and word, decrement byte and word, subtract, subtract with carry.
- **Logical.** AND, compare, complement, OR, exclusive OR.
- **Program control.** Call, decrement and jump on nonzero, interrupt return, jump conditional, jump relative conditional, return, set, reset and complement of carry flag.
- **Bit manipulation.** Test under mask, test complement under mask (plus logical operations listed above).
- **Rotate and shift.** Rotate left, rotate left through carry, rotate right, rotate right through carry, shift right arithmetic, swap nibbles.
- **Block transfer.** Load constant autoincrement, load external autoincrement.
- **CPU control.** Disable interrupts, enable interrupts, no operation, set register pointer.

generic name LABEL to signify that the content of a particular register file location and not its address should be used as the operand. For example, the instruction LD R0 LABEL loads the 8-bit working register R0 with the content of the location addressed by the label. An exception occurs when a program memory label is used. In that case, the operand specifies the address of the program memory location with the assigned label.

The symbol # is used to indicate that the following symbol is taken literally. For example, #0 represents the value zero, and #LABEL represents the value of the label's address, not its content. This symbol is generally used for immediate operands; that is, the operand appears within the instruction itself. The symbol @ is used to indicate that the following symbol be taken as an indirect address for the operand; that is, the specified symbol contains the address of the operand, not the operand itself. Hexadecimal constants are indicated by the symbol % followed by the appropriate hex digits, for example, %AF.

Addressing modes

The Z8 instruction set uses six main addressing modes: register, indirect register, immediate, indexed, direct, and relative (Table 3). The other addressing modes—autoincrement, register pair, and indirect register pair—are implied by certain instructions.

Z8 instructions can be grouped into three classes: instructions for which address modes are not applicable, such as no-operation (NOP) and return (RET); and one-operand and two-operand instructions, for which more than one addressing mode can be selected.

For the one-operand instructions, the register and indirect-register addressing modes are applicable to the source and destination operands. Increments, decrements, and rotates belong to this class. Three addressing modes are typically applicable to the source operand for the two-operand instructions—register, indirect register, and immediate. The destination addressing mode is register when the source is a register or indirect register; when the source is immediate, the destination addressing modes are register and indirect register. Add and subtract are examples of the two-operand class.

The indexed address mode is used with the load instruction (load and store), when the indexed and destination registers are both working registers. Relative address (RA) is used for jump relative, decrement, and jump on nonzero. Direct address (DA) is used for jumps and calls.

Several instructions (for example, load external and load constant) are available with an implied addressing mode, typically indirect register. These instructions can also be used in the autoincrement mode when the register value is incremented after being used. This mode allows very efficient block moves, described later.

As noted in Part 1, the Z8 contains a 144-byte random-access register file that is divided into nine groups, each occupying 16 contiguous locations. Eight of the working-register groups are general-purpose, and one is for control and input/output.

The full address of a working register is formed by combining a 4-bit working-register designator with the upper 4 bits of the register pointer. Thus the working-register group may be varied simply by changing the value of the register pointer.

Designating a register by a 4-bit working-register address, rather than an 8-bit register address, often reduces the length of an instruction and results in a shorter execution time. Changing the value of the register pointer is a convenient way to save the contents of the currently active working-register group, which is often necessary during interrupt processing.

TABLE 2: ASSEMBLY NOTATION FOR ADDRESSING MODES

Addressing mode	Assembly notation
Register	Rn for working registers (n is a number from 0 to 15), LABEL for registers
Register pair	RRn for working registers (n is an even number from 0 to 14), LABEL for registers
Indirect register	@Rn (n is a number from 0 to 15), @LABEL for registers
Indirect register pair	@RRn (n is an even number from 0 to 14), @LABEL for registers
Direct address	LABEL
Indexed	LABEL (Rn) (n is a number from 0 to 15)
Immediate	#VALUE
Relative address	LABEL

Bit manipulation

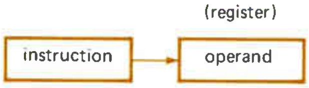
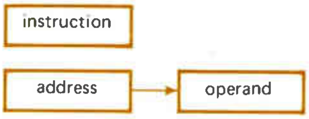
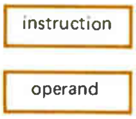
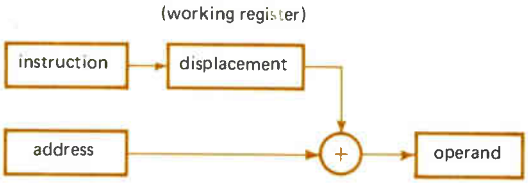
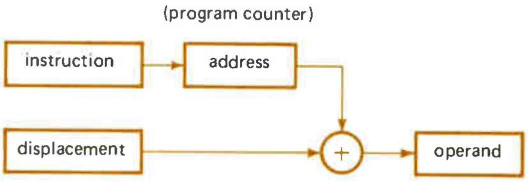
The Z8 can set, reset, or test any bit within any byte in the register file. This includes any I/O port, and most control registers. Combinations of 1 to 8 bits in any byte can be set, reset, or tested for 1s and 0s. In other words, any byte can become a flag byte that is set, reset, or tested by a single instruction. The following examples illustrate this feature.

Define the masks:	CONSTANT BIT3: = %08 BITS25: = %24
To set bit 3:	OR WAITFLG, #BIT3
To reset bit 3:	AND WAITFLG, #NOT BIT3
To test bit 3:	TM WAITFLG, #BIT3 JR Z, FLGZERO FLAGONE:
To test for bits 2 and 5 equal to one:	TM WAITFLG, #BITS25
To test for bits 2 and 5 equal to zero:	TCM WAITFLG, #BITS25

In all these examples the mask could be in a register.

The ability to test data and make decisions based on the results is especially important in single-chip microcomputers. The jump and jump-relative instructions of the Z8 have a repertoire of 21 conditional tests that use four of the six flags (carry, zero, sign, and overflow.) The jump-relative instruction, with its true range of

TABLE 3: ADDRESSING MODES OF THE Z8

Mode	Symbol	Diagram	Comments
Register	R		The operand value is the content of the register.
Indirect register	IR		The operand value is the content of the location whose address is in the register.
Direct address	DA		The destination address is the location whose address is in the instruction.(For program memory only.)
Immediate	IM		The operand value is in the instruction.
Index	X		The operand value is the content of the location whose address is the address in the instruction, offset by the content of the working register.
Relative address	RA		The operand value is the content of the location whose address is the content of the program counter offset by the displacement in the instruction.

+127 to −128, saves bytes and is easy to use.

Since the Z8 has a fully continuous program space, the user need not be concerned with pages or banks. The same instruction sequences are used no matter where the code resides, internal or external to the Z8, across a page boundary or not. This is possible because, when using the direct addressing mode, the 16-bit addresses for jumps and calls are contained in three-byte instructions. Jump indirect and call indirect are two-byte instructions that point to a register pair containing the 16-bit destination address. Long addresses are not inefficient in practice, because extra instructions are required for page or bank organization. In addition, the simplicity of the code greatly improves clarity and reduces software bugs.

Block transfers

Up to 62 kilobytes of external memory can be addressed using the load-external-autoincrement instruction. For sophisticated applications such as intelligent terminals, high-speed block transfer of data between external memory and the register file is extremely important. In the Z8, this type of transfer occurs at very high speed with the load-constant-autoincrement and load-external-autoincrement operations. These instructions autoincrement the source and destination automatically—much as is done in direct memory access.

To move a block of data from external data memory to the register file, the load-external-autoincrement instruction (LEDI) is used. The working register pair RR0 contains the 16-bit external address, the working register R2 contains the register address of the destination, and R3 contains the number of bytes to be moved.

			Bytes	Cycles
TRANSFER:				
	LDEI @R2	@RR0	2	8
	DJNZ	R3, TRANSFER	2	10/12*
			4	18/20* per byte transferred

*Jump taken/not taken.

```
INT1:         PUSH RP               !save RP and IMR!
              PUSH IMR
              SRP #RP1              !set RP!
              LD IMR #INT1MASK      !enable interrupts,
                                     of higher priority!
                 :
INTRETURN:    POP IMR               !restore RP and IMR!
              POP RP
              IRET

INT2:         PUSH RP               !save RP and IMR!
              PUSH IMR
              SRP #RP2              !set RP!
              LD IMR #INT2MASK      !enable interrupts,
                                     of higher priority!
                 :
RETURN2:      JP INTRETURN
```

1. Nesting interrupts. When entering an interrupt routine, the register pointer and interrupt-mask registers are saved in the stack. In the second level, the INT2MASK value will alow higher-priority interrupts to be processed, but will forbid lower-priority ones from occurring.

The load-constant-autoincrement instruction (LDCI) can be used to move data from the program space (either internal or external) to the register file. Data contained in the program space can be used for initialization and code conversion, as well as many other constant-value tables.

Interrupts

As was discussed briefly in Part 1, the Z8 has six levels of vectored interrupts—maskable and assigned priorities under software control—plus the ability to mix polling and interrupts. The register pointer mechanism can be used for fast context switching. In the simplest case, the program uses one set of registers for normal processing and another set for the interrupt-handling routine. In this instance, the following instructions would be needed when starting and completing the interrupt-handling routine:

```
INTHANDLER:         !flags are saved, and
                    disabled automatically!
    SRP #RPI        !RPI is a constant for
                    the interrupt RP!
       •
       •            !interrupt code!
       •
    SRP #RPN        !RPN is a constant
                    for the normal RP!
    IRET            !flags are restored and
                    interrupts enabled automatically!
```

Note that interrupts can be re-enabled either by software during the interrupt service routine to allow interrupts within interrupts (nesting) or automatically at the end of the interrupt service routine by executing the interrupt-return instruction (IRET) that also restores the program counter and flag register.

If nested interrupts must be processed, one of two courses may be chosen. For nonprioritized nesting, all the interrupts that were enabled can be re-enabled. For prioritized nesting, a new mask allows the user to re-enable chosen interrupts. The separate interrupt-request and interrupt-mask registers make it possible to use interrupts and polling together.

In the example presented above, interrupts were disabled for the entire routine. In order to allow other types of interrupts to occur, the interrupt-mask register can be changed so as to disable only the interrupt currently being processed.

```
BCD MODULE
CONSTANT
          PORTINIT: = %45                         !set up port 0
                                                  input port 1
          P01M: = 248                             output internal stack
INTERNAL
          STRING1  ARRAY [4 BYTES]
          STRING2  ARRAY [4 BYTES]
GLOBAL
          BCDADD PROCEDURE
                    ENTRY
                    SRP =0
                    LD P01M, =PORTINIT
                    LD R4, =8                     !read in two strings!
          INLOOP:
                    LD STRING1-1 (R4), R0         !input from port 0 store in
                                                   strings from bottom up!
                    DJNZ R4, INLOOP
                    LD R7, =4
                    RCF                           !clear carry!
                                                  !R4 = 0 from before!
          ADDLOOP:
                    LD R5, STRING1 (R4)
                    LD R6, STRING2 (R4)
                    ADC R5, R6                    !add digits!
                    DA R5                         !adjust!
                    LD R1, R5                     !output to port 1!
                    INC R4                        !next digit!
                    DJNZ R7, ADDLOOP              !loop!
                    RET
          END BCDADD
END BCD
```

2. BCD routine. The Z8 accepts two binary-coded-decimal digit strings, adds each pair of digits, and puts out the result. The strings which are (eight digits long) are read from port 0, upper digits first. The output is routed to port 2, lower digits first.

Stack

Under software control, the Z8 can use an internal or external stack, which is limited in size only by the available memory space. An 8- or 16-bit stack pointer occupies one of the registers or register pairs in the register file. Call instructions use the stack to store the 16-bit return value of the program counter. Interrupts automatically save the contents of the 16-bit program counter and of the 8-bit flag register on the stack. Moreover, the Z8 has push and pop instructions (see Table 1 again) that can save the contents of any register from the register file on the stack.

Figures 1 and 2 portray two programming examples. Fig. 1 illustrates the use of the stack for implementing a prioritized nesting scheme for handling interrupts. Upon the start of each of the handling routines, the register pointer is set to the appropriate register group and the interrupt-mask register is set to mask out interrupts of lower priority.

In Fig. 2, the Z8 takes two binary-coded-decimal digit strings, adds them, and puts out the result. The strings (each eight digits long) are read from an 8-bit port, upper digits first. The result is then transmitted, lower digits first, out another 8-bit port. □

Postscript on bit-slice families: microcontrollers serve many needs

by W. Thomas Adams and Scott M. Smith*

Applied Research Laboratories, University of Texas, Austin, Texas

ARCHITECTURAL FEATURES AND GENERAL CHARACTERISTICS OF MICROPROGRAM CONTROLLERS							
Bit-slice device	Manufacturer	Second sources	Technology	Unit/element[1]	Unit/element width (bits)	Pins and package	Power dissipation (mW)
SN74S482	TI	—	Schottky TTL	E	4	20 DIP	473
Am2909	AMD	Raytheon, Mot, Nat'l	Schottky TTL	E	4	28 DIP	420
Am2911	AMD	Raytheon, Mot, Nat'l	Schottky TTL	E	4	20 DIP	420
MC10801	Motorola	Fairchild	ECL	E	4	48 QUIL	1,738 (total)
67110	MMI	—	Schottky TTL	U	9	40 DIP	835
3001	Intel	Signetics	Schottky TTL	U	9	40 DIP	850
8X02	Signetics	SMS	Schottky TTL	U	10	28 DIP	682
9408	Fairchild	—	I^3L	U	10	40 DIP	650
Am2910	AMD	—	Schottky TTL	U	12	40 DIP	1,024

[1] Unit = one device controlling a memory space of 512 to 4,096 words, depending on the device.
Element = a bit-slice part, several being required to implement the sequencer for a reasonably sized control memory.

[2] Excluding resets, clocks, output bus enables, carry-in, etc.; intended to represent lines usually driven by the control memory.

[3] Control lines for instructions + status register input + I/O bus.

☐ The processor elements reviewed in part 1 of this series on bit-slice families [*Electronics*, Aug. 3, p. 91] mainly carry out data manipulation or arithmetic and are unlikely to be used alone. But the sequencers discussed in part 2 [*Electronics*, Aug. 17, p. 96] are controllers. When paired with a read-only-memory control store, they can be just what is needed in a high-speed application requiring more intelligence than it would be practical to provide with discrete transistor-transistor-logic circuits.

An example of a stand-alone use of the microcontroller might be as a high-speed intelligent front end for a minicomputer that is processing information gathered from a high-speed data-acquisition system. Digitized samples arriving every 150 nanoseconds would be too much for a metal-oxide-semiconductor microprocessor to handle, especially if it had to use its decision-making abilities on the fast stream of incoming data to, say, discriminate against false or aliased signals or to channel the stream to one of several signal-processing computers.

The best controller for the job would be a microprogrammed control unit. Unlike those microcontroller elements that must be cascaded and would require additional addressing components for control-store memory, such units have built-in memory-addressing capabilities of adequate size.

In fact, as the table indicates, a microcontroller is available to satisfy just about any need. Chips are available in a wide variety of technologies—emitter-coupled logic for the highest speed, standard TTL, and integrated injection logic for power-sensitive applications. While many functions are similar from microcontroller to microcontroller, the requirements for power dissipation, address widths, and package size will differ and in many cases dictate which device to use.

Untapped versatility

In conclusion, the limited popularity of bit-slice parts is largely attributable to an uninformed public of design engineers who labor under certain misapprehensions about their capabilities. In particular, the parts are in no way limited to general-purpose processing or standard computer architectures. Yet emphasis is almost always placed on a family approach—cascading a given manufacturer's processor elements into a desired word length and sequencing the result with a similar cascade of related microcontroller elements.

Such a construction is not the only legitimate use of the parts. It should by now be clear to potential users that the parts carry out basic functions (though some tack on a mix of additional useful features); that they can be interconnected in a myriad different ways; and finally, that many devices in bit-slice processor families can do very well on their own.

All the same, it is worth remembering that, although bit-slice parts may seem interesting in terms of both throughput and flexibility, they are also expensive. They should be used only in applications that cannot be built with a handful of low-cost TTL parts and that can afford the investment in software development required. ☐

* Both authors are now at IBM Corp., Office Products Division, Austin, Texas.

	Fundamental next-address mode	Subroutine levels	Internal looping capabilities	Internal storage for future branch	Ports I	O	I/O	Control lines required[2]
	Inc PC	4	none	none	1	1	0	6
	Inc PC	4	none	next-address field	3	1	0	5
	Inc PC	4	none	next-address field	1	1	0	5
	Inc PC	4	instruction, subroutine	status flags or next-address field	1	2	2	5 + 4 + 3[3]
	Inc PC pairwise branch	1	program	status flags	1	1	0	8 + 2[4]
	Branch	1[5]	none	status flags	1	1	0	7[6] + 4[4]
	Inc PC	4	none	none	1	1	0	3
	Inc PC	4	none	status flags	1,3	1	0	4 – 5
	Inc PC	5	program, instruction	next address	1	1	0	6

[4] Number of internal lines for controlling the carry/shift logic for the processor elements.

[5] Not inherent; device must be externally wired.

[6] The seven control lines are sufficient for all branching as well; separate branch address bus is used only for input of variable next addresses such as macroinstruction entry points.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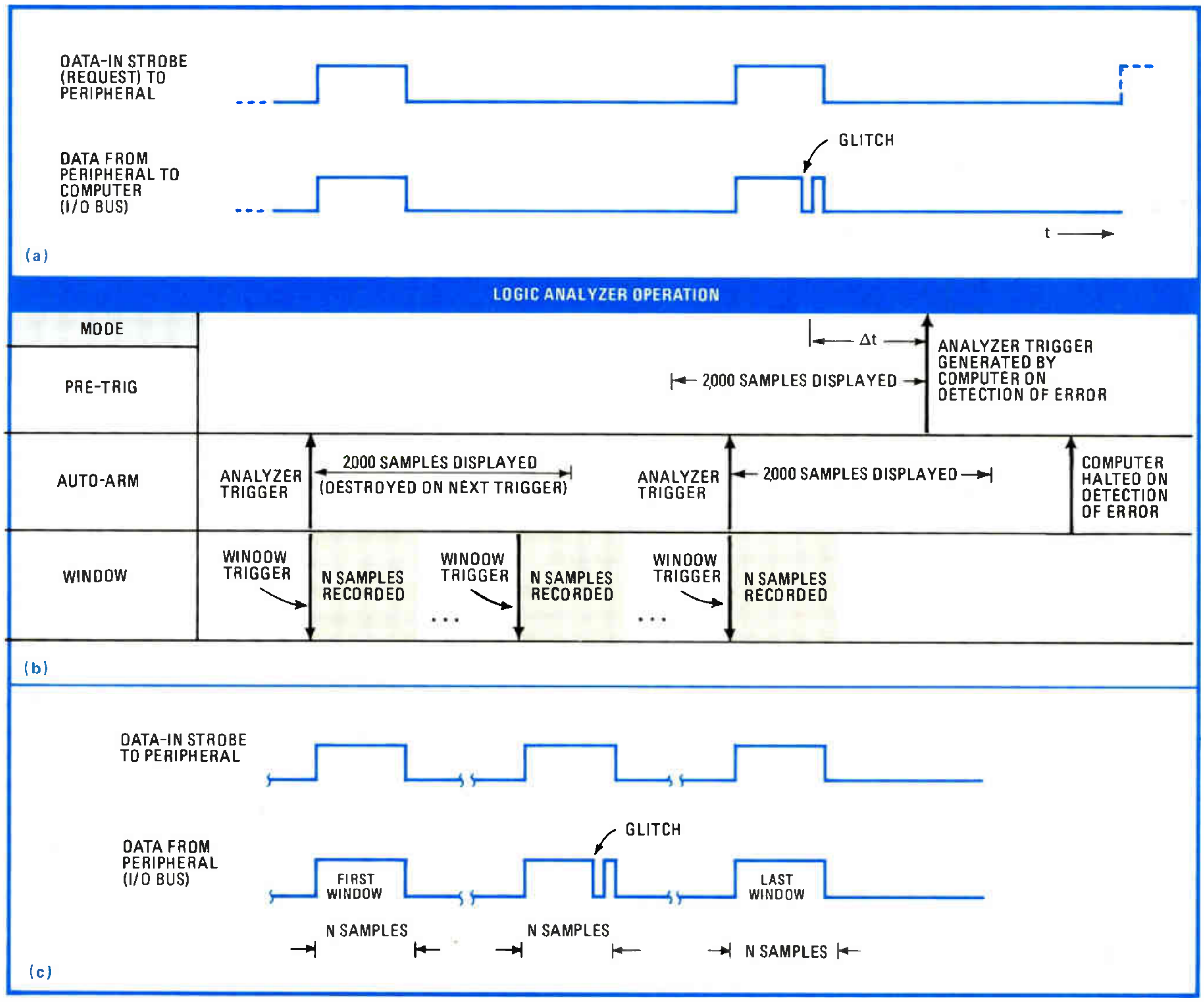
Window generator increases logic analyzer's capability

by Colin Gyles
Canadian Marconi Co., Montreal, Canada

Although the diagnostic power of the logic analyzer is unparalleled for troubleshooting digital systems, its ability to detect the type of errors that lead to intermittent circuit failures leaves something to be desired. For example, the analyzer would have difficulty in detecting a random error in a computer system that passed data in short bursts separated by longer periods containing no relevant information. In such instances, this circuit vastly increases the recording range of analyzers of the time-domain variety, such as the Biomation 8100D.

It is necessary to understand the operation of a stand-alone analyzer to appreciate the difficulties involved in the display of certain data errors. In the example shown in the timing diagram of Fig. 1a, a strobe or similar data-request signal is sent from a computer or other control unit to a peripheral device. The peripheral then sends the data requested to the computer through the latter's I/O port. Note that the data has a glitch, perhaps caused by noise, so that when checked by the computer it is found to contain an error.

There are two methods of recording the error with an analyzer. The first method makes use of the analyzer's pre-trigger mode. Input data is recorded continuously,



1. Analyzer overview. In typical example, stand-alone logic analyzer records glitch in the last word received on computer I/O bus only, because of limited record range (a, b). Record range is vastly extended with window generator, which produces bursts of clock pulses during data-strobe time, permitting many data words to be recorded. Errors occurring in other than the last word received can thus be detected (c).

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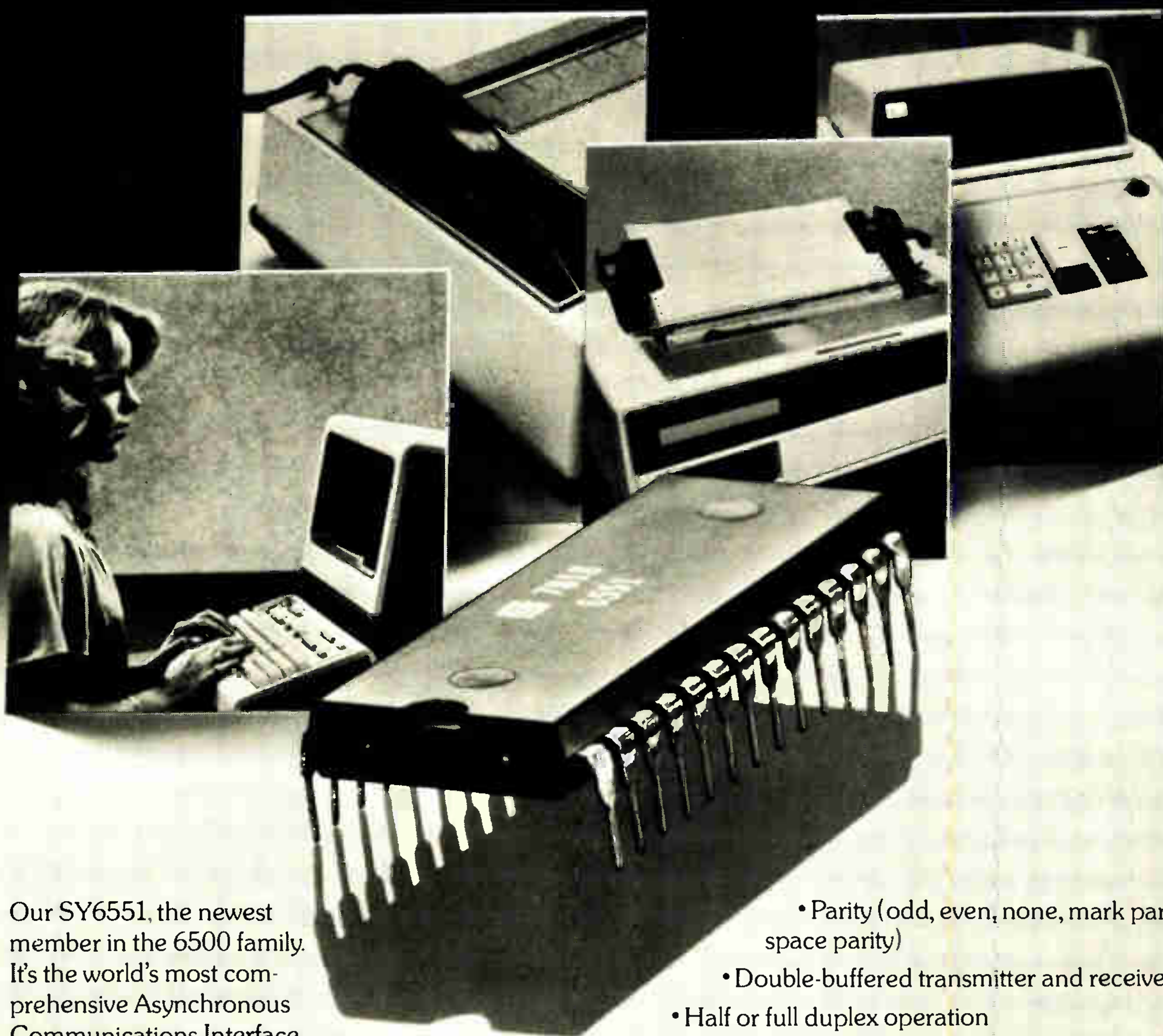

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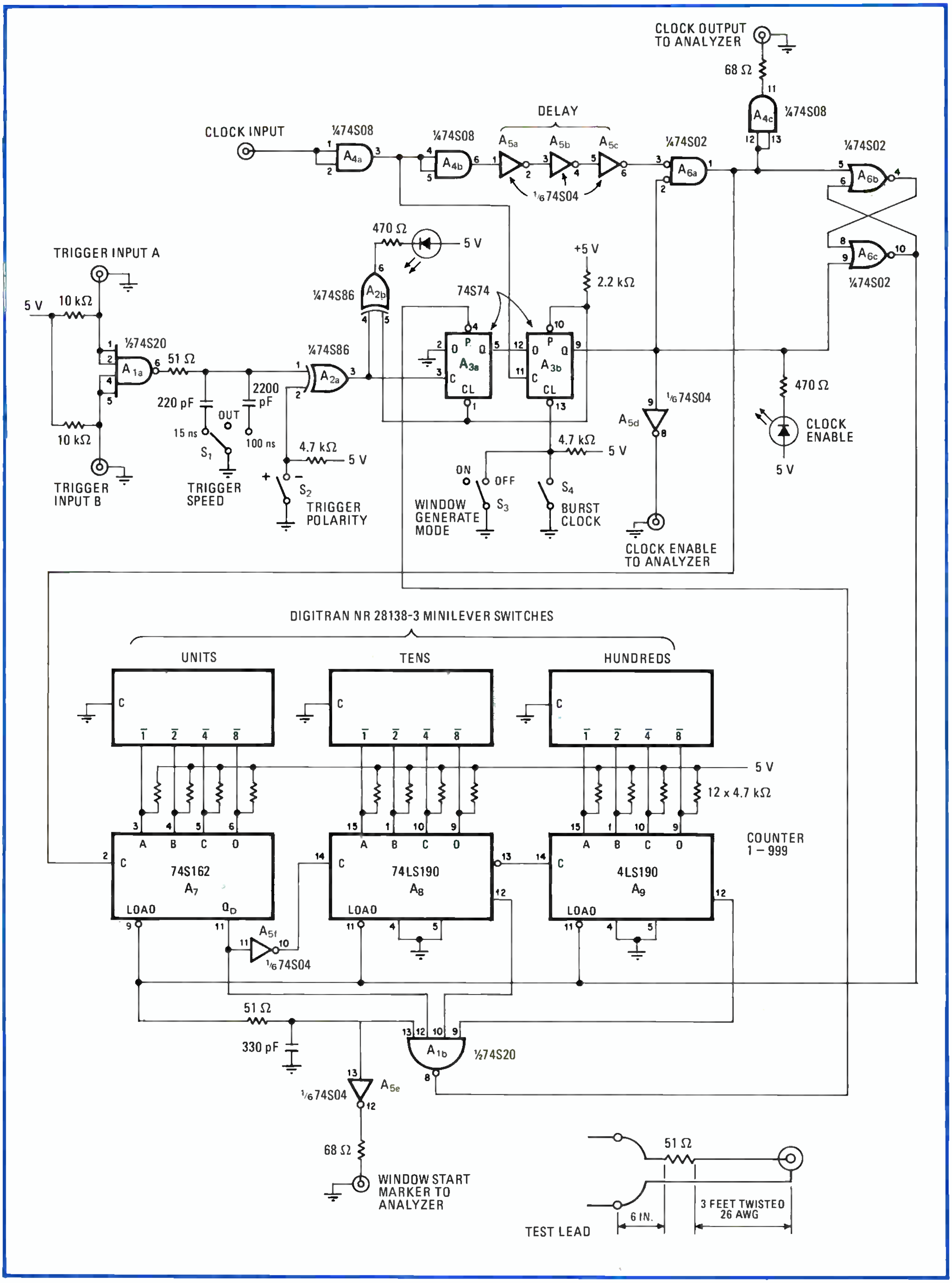

2. Window generator. Data-in strobe from control unit (computer) drives trigger inputs, initializing record period as circuit generates N clock periods, 1 microsecond wide, to analyzer through clock-output port. The value of N may be selected from 1 through 999.

and the analyzer is made to display the events causing the glitch. In the case of the 8100D, it displays the sequence of states that occurred in the interval, 2,000 sample units long, immediately preceding the trigger generated by the computer when the error was detected. Each sample unit corresponds to the period of the sampling rate of the analyzer's internal data clock. Thus, if the clock period is 20 ns, the events occurring up to 40 μs before the trigger can be displayed.

Needless to say, the larger the required recording range, the poorer the resolution and the harder it is to determine where an error occurs. And if the computer is so occupied with other duties that it cannot generate a trigger quickly enough after the error has occurred, the error will be missed altogether. Thus the time Δt, shown in Fig. 1b, must be minimized.

The second error-detection method uses the analyzer's auto-arm mode, which when triggered by an error records the following 2,000 samples. The circuitry is then rearmed. If a second trigger should occur, the analyzer destroys the previously recorded data and overwrites it with 2,000 new samples. The results of its operation are illustrated in Fig. 1b, with the trigger generated by the leading edge of the data-in strobe. With this method, the required range over which the analyzer records is small, so that the resolution will be high.

The error-detection problem cannot be solved satisfactorily by either method when the error is not contained within the last word received in a data stream (Fig. 1c). This condition might occur if the computer were making check-sum error determinations on a block of data from a paper-tape reader, where the results of the check would be revealed after the data word was read. In most instances, it would be impossible to display the error, since the time between strobes for a reader might be 100 milliseconds or so, but the strobe width might be only 1 microsecond.

Thus, to record a block of, say, 10 words, the record range would be 10(100 ms) = 1 second, but the resolution would be only 1/2,000 = 0.5 millisecond, and it is safe to conclude that an error lasting 1 μs would not be detected. Ideally it would be desirable to record the period in the vicinity of each strobe, where the error would occur, while holding the analyzer's internal clock off during the remaining time.

Therefore to detect the error, it is necessary to generate windows greater than 1 μs wide by a counter delivering N pulses to the external clock input of the analyzer after each window trigger, where N could be selected by the user. Then, on receipt of a trigger from the computer, due to detection of an error, the analyzer will stop recording (assuming pre-trigger mode) and display 2,000/N windows. The recording range would be equal to 4 seconds if N = 50 (that is, R = 100 ms [2,000]/50) for a resolution of 20 ns (equal to the analyzer's clock rate). This is an improvement of 100,000 times over the 40-μs recording range previously shown to exist for the same resolution.

The window-generator circuit for attaining the desired range magnification is shown in Fig. 2. The clock input is driven by a square-wave generator to provide the desired sampling interval. The logic analyzer is clocked by the signal emanating from the clock-output port. When a transition of the required polarity occurs at either of the trigger-input ports, the unit counts N clock pulses to the logic analyzer, N being set by the digital switch, which has a range of 1 to 999. During the time of the N-clock pulse burst, the trigger-input port is disabled.

The end result of the unit's operation is that N samples are clocked into the analyzer after each window-generator trigger. If the analyzer is set in the pre-trigger mode, then on receipt of an analyzer trigger from the computer, the recording will stop, displaying the last 2,000 samples, made up of 2,000/N windows side by side.

The window-start marker output may be fed to any one of the eight analyzer channels. This pulse is one clock period wide at the start of each window so that each frame may be identified at will. The clock-enable output can be recorded on a second logic analyzer to measure the time between window frames, if desired.

Note that the analyzer can be used in all trigger modes while using the window generator. In any of the post-trigger modes, the recording is complete when all 2,000 samples have been taken. If there are not a sufficient number of window triggers, the analyzer will hang up. The burst-clock switch is therefore included to enable the recording cycle to be completed manually whenever there are too few triggers to record the 2,000 samples.

The circuit relies mostly on sequential logic, as shown. S_1 and S_2 select the trigger speed and polarity, respectively. A positive transition at A_{3a}'s clock input brings its Q output low. At the next positive transition of the clock input, A_{3b} moves low. A_{4b} and A_{5a}–A_{5c} provide delay, in order that A_{6a} be enabled when the clock input is low. This is to prevent generation of a narrow clock-output pulse, which could upset the analyzer operation. The clock-output port now follows the clock-input signal. The circuit is designed to minimize the delay from the trigger-input pulse to the time the first clock-output pulse appears.

Just prior to the first clock at A_{6a}, the flip-flop A_{6b}–A_{6c} was set, which enables counters A_8 and A_9 to be loaded with the digital switches. A_7 is loaded during the first positive clock-input transition. This data is the 9's complement of what is displayed. A_{6c} is then set high, and the counters are free to advance from their set values up to 999, at which time the counters enable A_{1b} and preset A_{3a} to logic 1.

During the next clock input, A_{3b} moves high. The delay provided by A_{4b} and A_{5a}–A_{5c} disables A_{6a} before the clock-input transition arrives at its input, thus ensuring that no narrow glitches can be produced at clock output, as mentioned previously. The logic present at the output of A_{3b} then sets A_{6b}–A_{6c}, removing the preset signal from A_{3a} so that the trigger can be enabled for the next window.

Lead lengths should be minimized when building the circuit. The test lead for the trigger-input port should be built carefully also. It should not exceed 4 feet in length. A 51-ohm resistor on the hot side of the test lead will minimize ringing and reflections of energy from probed

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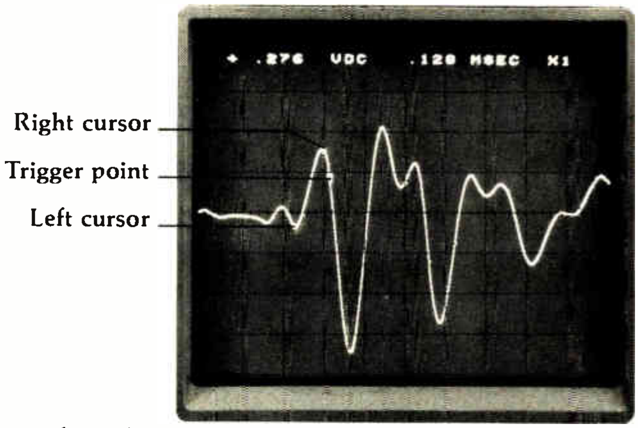

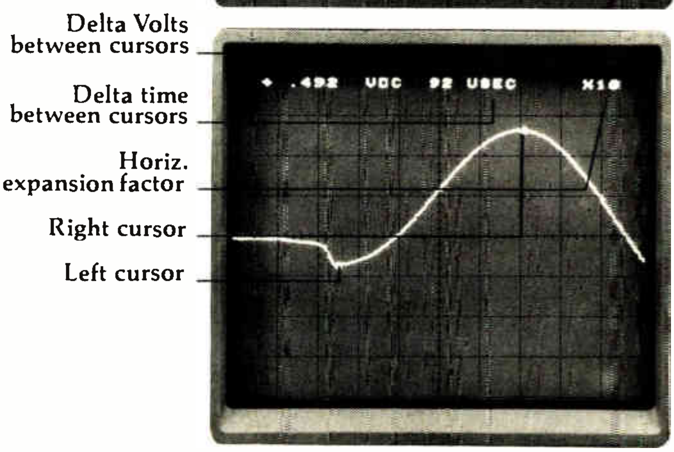

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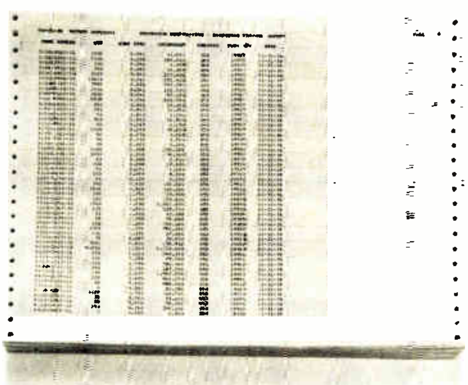

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circuits. Twisted-pair wires should be used to avoid undesirable coupling effects.

The circuit can work up to 60 MHz, with a one-count error between 33 and 60 MHz, which simply increases the window size by one. The size of the window does not substantially affect circuit accuracy. □

Synchronous pulsing cuts three-phase motor's dissipation

by D. J. Greenland
Cambridge, England

At very low clock rates, below 20 hertz, the windings of a three-phase motor dissipate excessive power. But this problem may be overcome if the motor is not heavily loaded—that is, the torque is less than 20 gram-centimeters. The circuit described here momentarily switches on the motor's supply line synchronously with the phase-generator clock pulse that activates each winding in sequence. Pulsing the windings at a low duty cycle and at the start of each phase increases circuit efficiency, yet enables the motor to develop sufficient torque.

Consider the savings in power. If each winding has a dc resistance of 15 ohms and is periodically energized from a 28-volt source, the power dissipated by each winding as the clock rate approaches zero is $P = (28)^2/15$, or 52.26, watts. Even when working at 20 hertz, or a 50-millisecond period, each winding would be energized for the same 50 ms or so and the power consumed per phase would be $P = (28^2/15)(50)(10^{-3}) = 2.61$ W. But if the energizing time can be reduced to 1 ms, say, the power consumed will be $P = (28^2/15)(1)(10^{-3}) = 52.26$ milliwatts.

The energizing time, T_c, is controlled by elements R and C of the 74121 monostable multivibrator, A_1, as shown in the figure. The one-shot is driven by the same phase generator clock, ϕ_{CK}, that also drives the three-phase switching circuit. (Since many well-known arrangements exist for deriving the required phase voltages for the windings, the actual schematic for the network is not shown here.)

A_1 fires on the positive edge of ϕ_{CK} and generates a 1-ms pulse that charges C_1, switches Q_1, and brings its collector to 28 V. Q_2 then turns on, driving the particular windings that happen to be activated at that instant by the switching network. The $\bar{Q}$ output of A_1 then moves back to 1 after the 1-ms interval and C_1 discharges through R_2 exponentially. C_1, R_1, and R_2 are selected once the frequency of ϕ_{CK}, R, and C are known.

It should be mentioned that at clock rates above 1 kilohertz, this circuit offers no power-saving advantage. This is because the period of 1-kHz waveform is 1 ms, comparable to the duty cycle required to reduce the dissipation for the 20-Hz clock previously discussed. □

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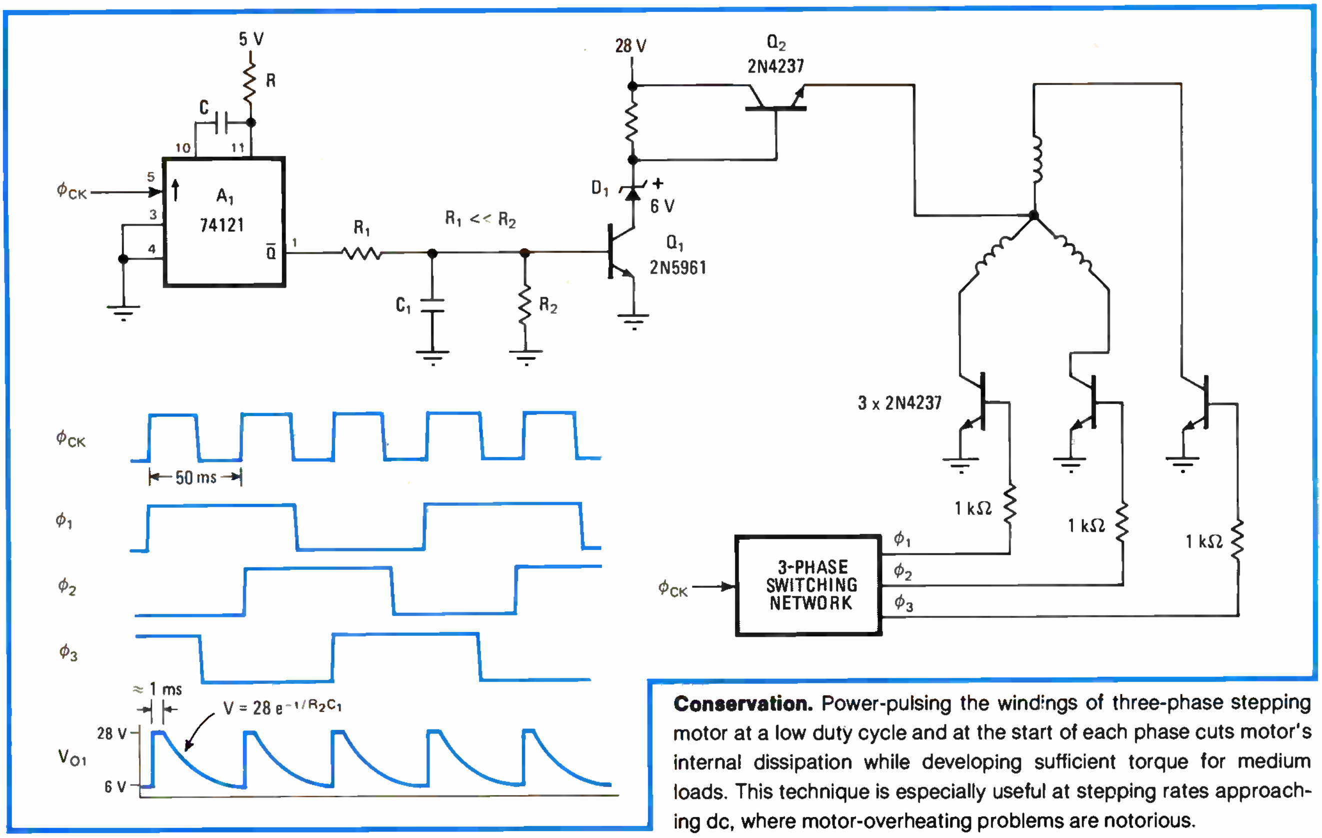


Conservation. Power-pulsing the windings of three-phase stepping motor at a low duty cycle and at the start of each phase cuts motor's internal dissipation while developing sufficient torque for medium loads. This technique is especially useful at stepping rates approaching dc, where motor-overheating problems are notorious.

Engineer's newsletter

Multiplier makes a better-balanced modem

One of the more popular balanced modulator-demodulator circuits is the Motorola MC 1596, according to Arthur Delagrange of the Navy Department's Naval Surface Weapons Center, Dahlgren, Va. But he notes that this circuit has a totem-pole arrangement of transistors, requiring that the two inputs and the output all be at different dc voltages. If the circuit is biased for unity gain and maximum dynamic range, only the carrier input is at ground. The signal input must be biased below ground, so that it picks up noise from the negative supply unless decoupling or regulating circuitry is added. The output must be biased above ground, so it picks up noise from the positive supply unless a differential amplifier is added.

The use of an MC 1594 multiplier can eliminate these problems. This device can be made into a balanced modulator simply by driving the Y input into saturation. **Then both inputs and outputs are all biased at ground,** but all have low power-supply sensitivity and full ±10-v dynamic range. The only disadvantage: the MC 1594 is slower and costs more.

Multiwire upstages multilayer

Are you considering the use of multilayer printed-circuit boards for a large system? A recent investigation at Rockwell's Autonetics Marine Systems division compared the cost of Kollmorgen Corp.'s automatic wiring technique called Multiwire against multilayer boards in the engineering phase of a large electronic military system. Aimed at improving the signal-to-noise ratio of sonar signal inputs, this system required 48 circuit boards of nine different types. The study showed that for this system there would be **an engineering cost saving of $17,586 if Multiwire were used.** During a future phase of this program, Multiwire boards will be evaluated for their adaptation to the manufacturing cycle

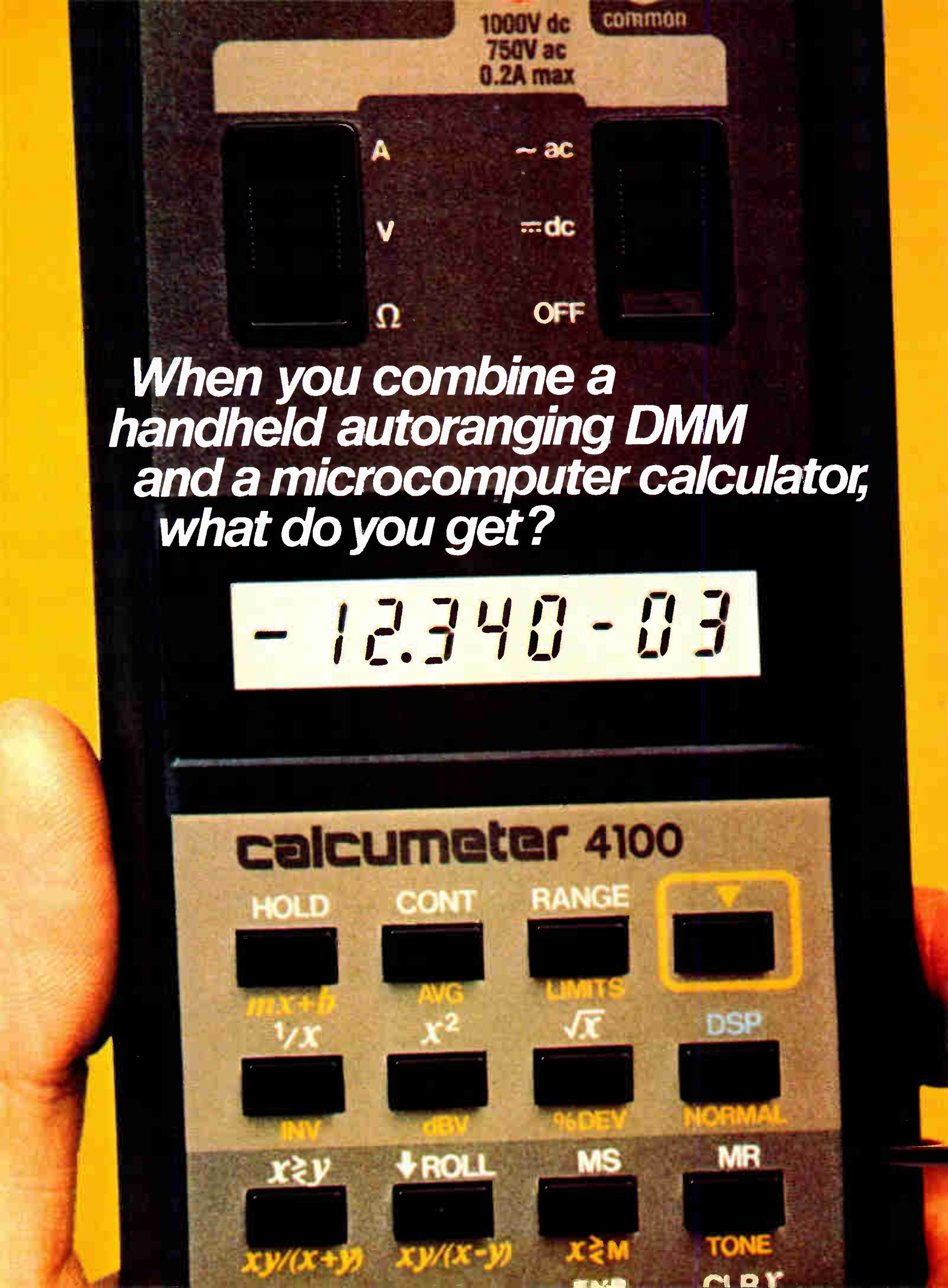
Stronger lens gets same-size image from smaller LEDs

Are you using acrylic for the bubble magnifying lens of your light-emitting-diode digital display? While acrylic is very clear, it has a much lower refractive index than other optical thermoplastics and therefore requires the design of more complex and costlier higher-magnification lens. U. S. Precision Lens has found a lens material as clear as acrylic but with greater magnifying power—Richardson's NAS **acrylic copolymer composed of 70% styrene and 30% acrylic.** This material, with a D-542 refractive index of 1.56 and 90% light transmission, allows smaller LED digits to be used and thus saves on the cost of their raw materials. For more information about NAS, write The Richardson Co., Polymeric Systems Division, 15 Meigs Ave., Madison, Conn. 06443.

Here comes the 3rd annual update on hybrid reliability

The third databook prepared by the Air Force's Reliability Center on the subject of reliability in hybrid circuits has just been released. Like its predecessors, the MDR-9 presents data collected from thousands of hybrid circuits used in many industry and Government programs and analyzed over the year preceding publication of the databook. The 300-page volume summarizes more than **200 million hours of field operation and 750 thousand hours of reliability tests,** plus burn-in and screening information, on more than 100,000 parts representing all types of IC technology. Also featured is a section dealing with failure rates of various resistors, capacitors, and other components for hybrids. A copy costs $50 from the Reliability Analysis Center, Rome Air Development Center, Griffiss Air Force Base, N. Y. 13441.

Jerry Lyman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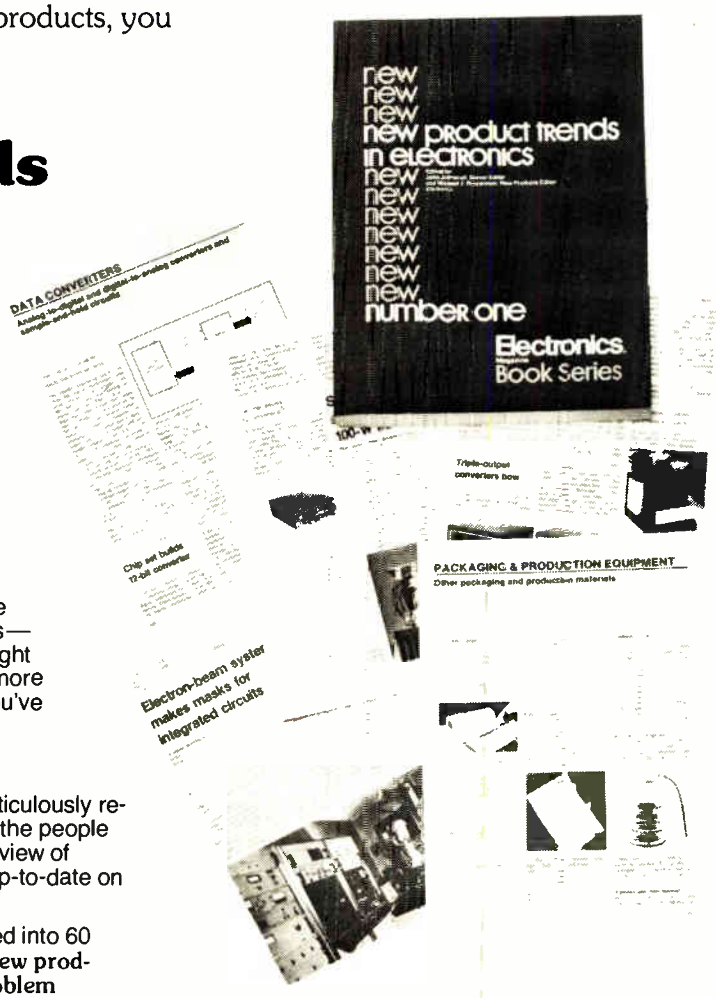

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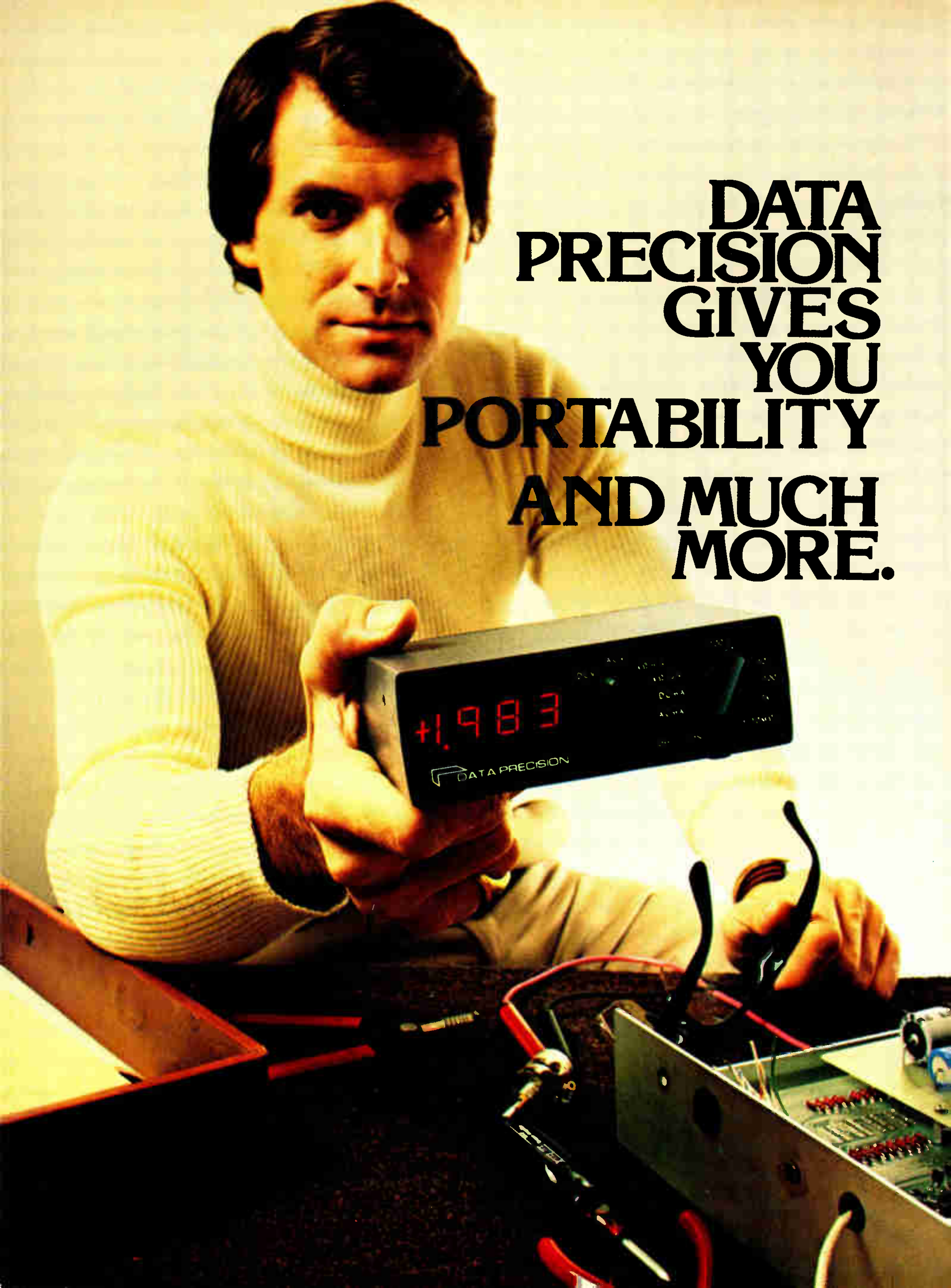
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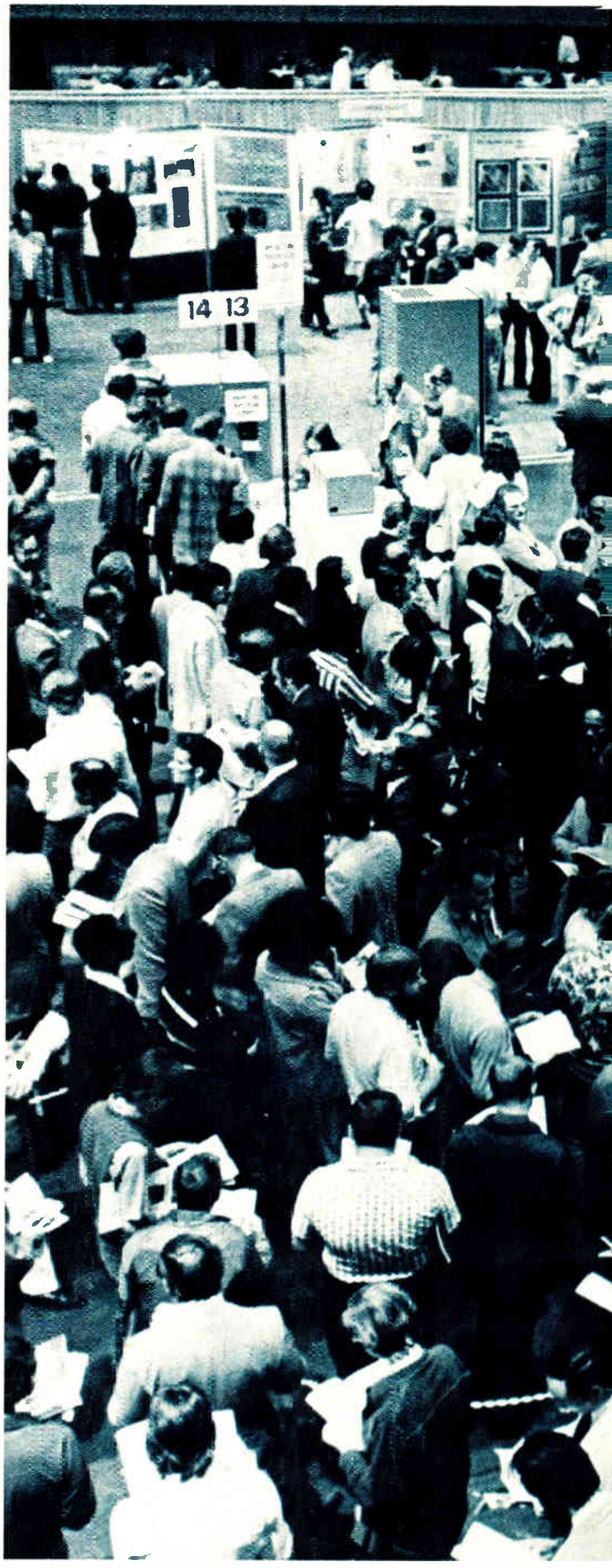
Telecommunications, microprocessors share star roles at sold-out Wescon



35,000 expected in Los Angeles to see wares of 500 exhibitors and attend 38 technical sessions

☐ The breezes of economic change are blowing through California's electronics industries. As evidence, the Los Angeles Convention Center and the city's year-old Bonaventure Hotel are being prepared to embrace the biggest Western Electronics Show and Convention of the decade Sept. 12–14. At the sold-out Wescon/78, exhibitors and conferees will spread their wares and words before an expected 35,000 engineers, executives, and technicians.

The other numbers for the 1978 show are equally impressive. Exhibit space was sold out in April, so the organizers added 19,000 square feet within the convention center. This permitted, in turn, the addition of 100 booths to the 862 already laid out, meaning accommodation for a total of about 500 exhibitors. Even the professional program has been expanded: it now numbers 38 sessions packed into the three days.

The Wescon/78 theme is "Micro/Evolution," and the show will give a good idea of the pervasiveness of microprocessors in electronic technology. But life is not all microprocessors. A look at the schedule of technical sessions indicates the growing importance of another sector: telecommunications. Fueled by Federal Communications Commission decisions encouraging competition, the industry is firing up for action. No less than nine sessions are devoted to telecommunications, foreshadowing a prime competitive arena of tomorrow.

Telecommunications components

The onrush of telecommunications technology is important to component makers. As a result of the rulings by the FCC and the courts encouraging competition, semiconductor firms are providing low-cost, small, durable devices in almost every area of telecommunications. Manufacturers have been able to take advantage of large-scale and very-large-scale integration to produce both digital and analog ICs. Two sessions, "A New Breed of Integrated Circuits Invades Telecommunications Systems" (session 38) and "Designing with Single Chip Multipliers" (session 25), offer insights into the latest applications of highly specialized ICs.

In his overview for session 38, Glen Myers of the electrical engineering department at the Naval Postgraduate School in Monterey, Calif., emphasizes the importance of the Carterfone decision of 1968, which cleared the way for non-Bell attachments to telephones, encouraging competition and prompting innovation.

The other papers in this session cover five specific devices, each with a unique communication function. Bruce Ballard of Rockwell International Corp. in Anaheim, Calif., discusses both the telephony and nontelephony applications of dual-tone multifrequency and push-button signaling techniques. Rockwell's DTMF receiver and binary-to-dial-pulse converter chips are offered as prime examples of LSI penetration of the telecommunications field. A related paper by Charles B. Johnson of Mostek Corp., Carrollton, Texas, discusses two complementary-metal-oxide-semiconductor pulse and tone dialers that allow telephone designers to utilize keyboard dialing and to signal the central office with either pulses or DTMF signals.

The hottest item in the communications industry—the encoder-decoder implemented as an IC—is the topic of two papers. Stephen Moore of Siliconix Inc., Santa Clara, Calif., reports on a two-chip design for a per-channel pulse-code-modulated codec. He emphasizes the advantages of the per-channel approach: flexibility for implementation in other systems besides the telephone, such as digital audio, speech synthesis, data acquisition, and telemetry. Steven Kelly of Motorola Semiconductor Products Inc. of Phoenix describes a dedicated solid-state subscriber set for telephone systems and private automated branch exchanges that uses four chips for delta-modulated communication. The ICs consist of two codecs for simple operation, a wideband, low-power quad operational amplifier for filtering, and a solid-state transformer for line conversion. Lastly, George K. Warren of National Semiconductor Corp., Santa Clara, Calif., discusses thick-film hybrid active filters for both PCM and DTMF telecommunication systems.

One-chip multipliers proliferate

In the session on single-chip multipliers, the emphasis turns to hardware implementation of digital signal-processing techniques. In a detailed look at the available chips and how sophisticated implementation of mathematical algorithms is possible with newer chips, Roy Levy of Advanced Micro Devices Inc., Sunnyvale, Calif., discusses their use in radar and sonar processing and in spectrum analysis. He compares today's 8-by-8-bit and 16-by-16-bit serial/parallel multipliers with the 2-by-4-bit arrays handled by less sophisticated chips in the past. In the second paper, Bill Koral, of TRW Inc.'s LSI Products division, Redondo Beach, Calif., presents an in-depth study of multipliers as they apply in digital signal processing. He describes a 24-by-24 parallel double-precision multiplier providing a 48-bit product in 200 nanoseconds—a feat necessary for complex recursive digital filtering, as well as for spectrum analysis using a fast Fourier transform. A 35-bit-wide multiplier-accumulator is also discussed as the heart of a circuit that can perform a 512-point FFT and produce the 8-bit-wide complex data in 4.2 milliseconds.

A high-speed 12-by-12 number cruncher in a 28-pin package is the subject of the third paper, by Dick Blasco of American Microsystems Inc., Santa Clara, Calif. Using V-groove MOS technology, the device is said to be compatible with the 6800 and 9900 microprocessor and able to perform a 128-complex-point FFT in 10.7 ms. In the last paper, Shlomo Wasser of Monolithic Memories Inc., Sunnyvale, Calif., discusses a bus-oriented 16-by-16-bit 2's-complement multiplier that interfaces with popular microprocessors. He points to the chip's 1-microsecond speed and 16-bit resolution as ideal for speech processor and instrumentation applications.

Microprocessors

Microprocessors have revolutionized logic design: chip counts have been slashed, power consumption is down, reliability is up. Furthermore, when a computer runs a system, alterations can be as easy as changing a few lines of code—hence the expression, "extra functions are free with software." Obviously, however, something must be done about the skyrocketing cost of software design. Session 30, "Reducing the Cost of Microprocessor Software Development," examines the subject from three perspectives: what a system designer should know to develop a microprocessor-based design, how high-level languages can cut time and expense, and how the microprocessor itself can be designed so as to be cost-effective through its architecture.

System design will be discussed by Burt Masnik of Hazeltine Inc., Greenlawn, N. Y. With seven years' experience integrating processors into systems, he concentrates on debugging techniques. For example, if the system does not function properly, is the malfunction hardware- or software-related? A good way to find out, he says, is to write small routines whose sole purpose is to exercise the hardware to ensure its credibility, after which software problems can be ironed out. He also discusses what can be done about changing product specifications, the need for more detailed information from IC manufacturers regarding their products, and the advantages of in-circuit emulators.

Software components are addressed in two papers, one from Joseph P. Harakal of Intel Corp., Santa Clara, Calif., and one from Stephen M. Hicks of Forth Inc., Manhattan Beach, Calif., which offers miniForth and microForth as software design tools. Both speakers will look at the pros and cons of high-level languages in developing software for microprocessors. The advantages are many: they are inherently more portable than assembly languages, they limit errors by accomplishing certain tasks automatically, and they are easier to read and write. However, they can be inefficient because they are further removed from machine code and therefore often produce too many object lines or run at less than optimal speeds. The Forth language is said to have solved some of these inefficiencies.

Finally, processor architectures themselves can make programming easier. To get this point across, William Huston from Motorola's Integrated Circuit division in

Austin, Texas, reports on the 6809 processor, which will be introduced this fall. It has a number of addressing modes that allow, among other things, the use of position-independent code at the assembly-language level. This means that high-level-language benefits like modularity and relocatability will be available through the use of relative addressing and pointer stacks, which in turn will increase efficiency and reduce cost.

16-bit processors

Before it ever made an appearance, the 16-bit microprocessor was thought to be the collision point, in terms of hardware, for minicomputer makers integrating downward and semiconductor manufacturers scaling upward. Now the collision is taking place, and two sessions consider the various products from just such bottom-up and top-down perspectives. Taking the bird's eye view is session 20, "Evolution to 16-Bit Microprocessors," organized by Thomas A. Longo of Fairchild Camera & Instrument Corp. in Palo Alto, Calif. Peter W. J. Verhofstadt, also from Fairchild, will discuss the Mountain View, Calif., company's 9440 central processing unit, which executes the same instruction set as Data General Corp.'s Nova series of general-purpose minicomputers. The 9440, built with integrated injection logic, uses a 16-bit multiplexed information bus to directly address 32,768 words of memory and up to 63 peripheral input/output devices.

Another descendant from a minicomputer past is Texas Instrument Inc.'s 9900 family of microprocessors, and the path downward from TI's 990 mini to the 9900 is presented by Deene Ogden, from the company's Houston facility, who takes up the issue of compatibility between the machines. He tells how the cost of integrating from mini to microcomputer can be minimized only if the software is saved—with machine-independent high-level programming languages and a software-compatible family of parts. TI carries register-to-register minicomputer architecture in the 990 on down through the board products like the 900/10 and 900/4 on to the 9900 CPU, 9940 one-chipper, and finally to the 8-bit–compatible 9985. The 9985, the most recently introduced, is a 40-pin high-performance device with no I/O that has 256 bytes of random-access memory (no read-only memory) and is oriented toward control applications.

Not to be left out is the contribution of the minicomputer leader, Digital Equipment Corp., Maynard, Mass. DEC's Michael Titelbaum offers his company's LSI-11 microcomputer as a contender for high-performance applications and describes the extended instruction sets available to the user in a microprogram ROM that supplements the standard four-chip set. With it a whole world of specialized high-performance applications like real-time signal processing and extensive number crunching, can be attacked.

Spicing up the session is a report on a proprietary microprocessor also from a minicomputer manufacturer—Hewlett-Packard Co.'s unique C-MOS-on-sapphire 16-bit device that goes into several of the company's instruments, including the new HP 2631 bidirectional intelligent printer. The control-oriented processor is a nonmultiplexed fully static part that runs from dc to 5 megahertz and is housed in a 48-pin leadless-substrate package. The paper's authors, David Burns, Matthew O'Brien, and Lance Mills, of HP's Data Terminals division, Cupertino, Calif., go into the circuits that shift from C-MOS to transistor-transistor-logic levels (the part runs on 12 volts), the 34 instructions, and the machine's regular register-to-register architecture.

The session with the worm's-eye view is number 14, "A Close Look at the 16-Bit Microcomputer: Past, Present, and Future." Represented is Intel's 8086 in a paper delivered by Dave Gellatly, who discusses the new chip's fit into the upwardly mobile 8-bit design world. The goals of the 8086 design were to extend 8080 features and add processing like 16-bit arithmetic, signed 8- and 16-bit multiplication and division, efficient byte-string operations, and improved bit manipulation.

Painting a family portrait are Motorola's Gary Daniels and Gary Summers, who relate the 6800 approach, from the first 8-bit CPU to the forthcoming 68000, or Macss, (for Motorola advanced computer system on silicon). Included in the picture are a pair of soon-to-appear parts. The first is the one-chip 6801, which comprises in a 40-pin package an enhanced 8-bit CPU, a 1-MHz clock, 2,048 bytes of ROM, 128 bytes of RAM, a 16-bit multipurpose timer, and 31 pins for I/O. The second is the high-performance 6809, Motorola's bridge between 8 and 16 bits. Basically a souped-up 6800, the 40-pin part has lots of stack and address flexibility (for example, over 20 addressing modes) and new registers, new instructions, and new hardware (like a built-in multiplier). Yet it is upwardly source-code–compatible with the 6800.

The authors also give a peek at the 16-bit 68000, which coincidentally contains over 68,000 transistors. They stress the regularity and cleanness of the part's architecture—much like that of a minicomputer. The 68000 supports six data types and a 24-bit address field for reaching 16 megabytes—big programs. Powerful new instructions have been added to the 68000 compared with earlier 6800 parts, Daniels and Summers point out, including fast signed or unsigned 16-bit multiplication and division, binary coded-decimal arithmetic, and a versatile MOVE instruction.

Family

Equally exciting is the forthcoming Z8000 from Zilog Inc., Cupertino, Calif. Peter Alfke will extol the merits of the 16-bit microprocessor and its proposed family of parts. He foresees use of the device in many high-performance distributed-processing applications, as a result of the family approach taken by Intel. Alfke says that coming are: a memory management unit that will take care of the memory segmenting, address translation, and memory protection; a parallel I/O interface with three counter-timers and a programmable interrupt controller; a dual-channel serial-I/O communications interface that handles multiple protocols; an intelligent peripheral controller; and some buffers to interface the Z8000 with I/O devices.

Michael Smolin wraps up with a survey of microprocessor trends that may hint at some of the developmental work at National Semiconductor. His area is advanced microprocessor products, and that includes 16-bit units, one-chip designs, and other devices that are still on the drawing board at Santa Clara.

Single-chip microcomputers

Mostek's James Vittera thinks that enough has been said about single-chip microcomputers in the mundane roles of oven and toy controllers, and so he put together a session devoted to the role of one-chippers in more sophisticated applications. The result is session 7, "Single Chip Microcomputers—Distributed and Multiprocessing Techniques."

Vittera thinks that designers should look at devices such as cash registers and terminals as systems best implemented with several microprocessors—especially one-chippers, since they have their own program and data memory. The trend, he adds, is toward loose coupling, that is, having the processors communicate over a serial bus.

Supporting loosely coupled networks are Intel, Motorola, Texas Instruments, and Mostek. Michael Wiles and Fuad Musa have written a paper on Motorola's forthcoming 6801, which has, in addition to a serial I/O port that permits its use in multiprocessor applications, an improved 6800 CPU, 2 kilobytes of ROM, 128 bytes of RAM, a 16-bit timer, and 31 parallel, programmable I/O lines for managing peripherals. The authors discuss a full-duplex distributed-communications system using a standard protocol that allows interconnection of either star or ring networks.

Intel's Don Phillips proposes a cash register built with multiple microprocessors, namely, the 8085, 8041, and 8049. The 8085 is Intel's enhanced 8080, running at 3 MHz; the 8041 is an intelligent peripheral controller with a CPU, 64 bytes of RAM, and 1,024 bytes of ROM. Together they perform all the calculations and internal operations. The 8049, a high-speed (11-MHz) version of the 8048, also has a CPU, 64 bytes of RAM, and 1 kilobyte of ROM; it is the stand-alone controller of the display in the cash register. The three chips communicate over a serial line, and Phillips describes a novel use of the 8085's MOV ACC instruction to create a universal asynchronous receiver/transmitter in software.

TI's John Bryant discusses the 16-bit 9940 microcomputer. He considers the advantages and disadvantages of both loosely and tightly coupled systems of multiple microprocessors. The problem with tightly coupled systems, he says, is that the software design for them is just too strenuous. In such systems, all parallel-interconnected processors share a global memory, and problems like conflicting requests and reliability must be resolved with extensive operating-system software. As a result, the lower-cost, serially interconnected approach better fits cost-sensitive microcomputer designs, and Bryant gives as examples several systems built around the 9940.

Mostek's Robert Burckle proposes the same approach (also using the example of a cash register) built around the 3870 and 3872. The 3870 has 64 bytes of RAM and 2,048 bytes of ROM; the 3872 doubles both those figures. In the cash register, the 3870 is dedicated to control of the printing mechanism, while the 3872 does everything else. Also mentioned in Burckle's paper are a pair of new chips in the 3870 family: the 3973, a 3972 with a serial port, which is heavily involved in Mostek's distributed-processing game plan; and the 3876, a 3870 with the doubled RAM capacity of a 3872.

Logic and memory

Large high-speed computers have only recently begun to enjoy the savings in cost and power offered by LSI, which has entered the highest-performance applications in the form of nanosecond and subnanosecond gate arrays. Session 3, "Programmable Bipolar Logic for High Performance Applications," takes a close look at the high-speed components offered by several manufacturers and their potential uses.

Proponents of the gate-array approach include Motorola and Fairchild Camera & Instrument. William Blood of Motorola's Integrated Circuits division, Mesa, Ariz., discusses the applications of his firm's new macrocell array, which, unlike the usual array of gates, is made up of a collection of cells each comprising many gates. Each cell is equivalent to a small- or medium-scale integrated device and is selected from Motorola's library of logic and arithmetic functions.

Fairchild's F200 subnanosecond emitter-coupled-logic gate array is the topic of a paper delivered by James W. Hively. The F200 array actually comprises 168 gates, 144 of which are internal low-level logic and the remaining 24 are high-level or buffer gates. Gate delays in the family are a miniscule 750 picoseconds, and the parts come in special 52- and 68-pin packages.

Bearing witness to the usefulness of this array, which can actually carry out 250 to 300 functions through the use of collector and emitter "dotting," or complements, is Control Data Corp.'s Richard E. Offerdahl. Offerdahl will discuss the efficacy of the F200 parts in a high-speed Cyber-76-type computer under development at the Minneapolis company.

As a replacement for all the power- and board-space–hungry 7400 family of random TTL parts that surround nearly every high-speed design, John Birkner of Monolithic Memories offers his company's PAL high-speed, low-cost fusible-link arrays. With PAL (for programmable array logic), not only can a user make tighter, more efficient designs, Birkner says, but he no longer has to keep a large inventory of 7400 parts. All that is needed at most is a stock of the 14 PAL parts, since the function of each is determined when its fusible links are blown to interconnect the logic paths.

Charles Mitchell and Phillip Holland of National Semiconductor describe the use of high-speed programmable ROMs to generate Boolean functions. Using the PROM as a truth table for the logical operation makes for great savings in random-logic chip count, and the new PROMs are getting fast enough to replace TTL parts.

"The Impact of New Memory Technologies on Computer Design" is the subject of session 16. Included are papers on MOS RAMs, bubble memory devices, charge-coupled devices, electron-beam addressable memories, and magnetic media.

Mostek's David Wooten discusses how the inherent refresh and power requirements and error-correcting capabilities of dynamic RAMs affect the application of these parts in computer systems. He notes that in older computer architecture, designed with asynchronous bus structures and slower cycle speeds, dynamic RAMs can generally be applied with no problem at all. In newer systems with synchronous bus structures, however, they are more difficult to use. But Wooten says that memory devices "will not force other changes in architecture. Memory devices don't change, they just get faster."

Bubbles offer options

The development of bubble memory devices is the subject of a paper by Gayle Lampson of Texas Instruments' Terminals and Peripherals division, Houston. He notes that these devices offer the computer terminal designer more tradeoffs among transfer rate, access time, cost, power, size, and weight when compared with existing memory technologies.

Don Smith of Control Data's Micro-Bit division, Lexington, Mass., explains the construction and application of an electron-beam addressable memory (EBAM). The memory system is based on a vacuum tube 6 inches in diameter and 2 feet long that contains a silicon-dioxide MOS capacitor target 1.6 in. square. Each target can store 128 million bits, and the system Smith describes uses 16 tubes to provide a total of 256 megabytes of storage. Since it costs some 10 to 20 times less than MOS memory, Smith believes that EBAM can be applied in a storage hierarchy between the disk drives and the CPU as a fast paging disk or I/O cache, instead of bubble or CCD memories. Although the technology has already been in development for nine years, he says, it will take until the early 1980s for the system to be commercially available.

Floppy disks and their future are explored in a paper by George Sollman of Shugart Associates, Sunnyvale, Calif. Calling floppies "the most explosive peripheral technology of this decade," Sollman explores the state of the floppy art and discusses future refinements that he says could bring the floppy disk to 5 to 10 megabytes of storage per diskette, up from the current limit of slightly more than 1 megabyte.

A more tutorial session on how these various technologies are applied to system design is session 22, "Memory Technologies: Systems Considerations and Applications." The session starts with a paper by Mike Chang and Brent Miller of Amdahl Corp., Sunnyvale, that discusses how the various technologies fit the different systems' performance requirements. Other papers discuss MOS and bipolar RAMs and CCD and bubble memories, with the emphasis on current developments and soon-to-be available products.

Instruments

With microprocessor-based products having taken the instrumentation industry to new levels, designers are aiming for digital fault isolation. Session 29, "Solutions for Product Testing," covers the various techniques used for fault isolation and their effectiveness in design debugging, production testing, and field service.

Hans Nadig of Hewlett-Packard Co., Santa Clara, Calif., discusses the basic technique of signature analysis and what design considerations are necessary to implement it in a microprocessor-based product. He also considers production and field service strategies based on signature analysis and gives a number of actual applications. Lawrence Badagliacca of Millenium Systems Inc., Cupertino, Calif., reviews a number of stimulus-and-response test methods, describing in particular the implementation and advantages of a new instrument combining in-circuit emulation and signature analysis.

Walter R. Kalin of Tektronix Inc., Beaverton, Ore., approaches system maintenance and troubleshooting from the viewpoint of a documented service procedure used with his company's 851 digital tester. The emphasis here is on fast evaluation of system performance or malfunctioning by providing a means of measuring the chip's power-supply voltages, clocking waveforms, temperature, and peripheral-circuit parameters. Finally, Bob Lorentzen of Gould Inc.'s Biomation division, Santa Clara, Calif., discusses the use of his company's digital testing oscilloscope in production testing and field service. It eliminates the need for software support when testing a microprocessor system.

Session 35, "Automated Test and Control Systems—The Building Block Approach," focuses on the IEEE-488 bus. It covers bus operation, hardware interfaces, troubleshooting, and applications to complete automated systems, both instrument- and component-based.

The leadoff paper, by Claude A. Wiatrowski of the University of Colorado, Colorado Springs, describes the bus's logical operation and electrical characteristics and then compares several commercially available bus monitor-testers. Mike Newman and Joe Hootman of Motorola, Austin, compare bus interfaces constructed with SSI components with their company's recent LSI interface chip, the MC 68/488, and Intel's newly announced 8291 talker-listener and 8292 controller chips. They give practical information on the use of these components and specific examples of their application.

Session organizer Robert L. Morrison of Burr-Brown

Research Corp., Tucson, Ariz. concentrates on interfacing the bus with data-conversion components rather than with instruments. He discusses interfacing digital-to-analog, analog-to-digital, and data-acquisition systems with the bus. Finally, Richard Zitzmann of John Fluke Manufacturing Co., Mountlake Terrace, Wash., examines the advantages the IEEE-488 bus affords the system design approach, emphasizing cost-effectiveness, especially for software and instruments.

Wescon coverage

In addition to this summary of important technical sessions, such as those on 16-bit processors, single-board computers, instruments, and communications, *Electronics'* Wescon coverage also features a section, previewing the significant new products to be introduced at the show, starting on page 171.

For a related story, see the Probing the News article (p. 85) dealing with the electronics associations in the West. This article is based on interviews with supporters and critics of these industry groups: American Electronics Association, Semiconductor Industry Association, Electronics Association of California, and the Semiconductor Equipment and Materials Institute.

Satellites and fiber optics

With the rush to digital communications technology accelerating [*Electronics*, July 20, p. 88]. Wescon is a good place to gain an overview of the state of that art. Three sessions are devoted to the burgeoning area, with an emphasis on satellite systems.

"Modern Communications: Techniques and Applications" is divided into two parts—sessions 15 and 21—both headed by Bernard Sklar of The Aerospace Corp., El Segundo, Calif. Sklar's paper reviews the basic signal processing performed in typical digital communications systems. It traces the complete signal path from the information source to the receiver, focusing on formatting, coding, multiplexing, modulation, and spreading.

L. Biederman of Lincom Corp., Los Angeles, considers the advantages and disadvantages of various coding schemes, gearing his discussion to practical examples of codes for both error detection and correction. He notes that "it's possible to use coding even in a bandwidth-limited environment. The implication that coding expands the required bandwidth doesn't always apply."

G. Huth of Axiomatix Inc., also in Los Angeles, describes the basic operating principles of spread-spectrum communications. His state-of-the-art tutorial addresses the jamming problem and presents a procedure for determining the best results obtainable in the face of a given worst-case jamming. F. S. Nakamoto of Rockwell International, Los Angeles, considers performance degradation due to synchronization errors between a transmitter and a receiver.

Session 21 continues the tutorial format of session 15 but stresses present-day applications as well as design principles. For example, L. M. Nirenberg of The Aerospace Corp. speaks on multiple-access system engineering for satellite communications, including time-domain and frequency-domain multiple access. He presents a useful curve showing the relationship between message delay and carrier power/noise density as a function of bit error for continuous-phase shift-key modulation.

Rockwell's J. C. Hoagland compares overall and component specifications for the space shuttle communications systems with actual results. Space shuttle communications are all digital, and many devices were especially developed for this application. These include a 200-watt continuous-wave S-band mechanical switch and a 200-w cw traveling-wave tube. Hoagland reveals what he calls a "major breakthrough" in his curves of system bit-error rate versus signal-to-noise ratio: his achieved data was very close to the theoretical limits for the system's bit-synchronous decoder.

Session 31, "Communications Satellites—New Technology, New Services," has been designed by chairman Ivan Bekey of The Aerospace Corp. to provide information on new trends in communications-satellite systems, techniques, and technology.

The all-digital communications for the SBS satellite is discussed by J. D. Barnla of Satellite Business Systems Corp., McLean, Va., in a paper co-written by F. R. Zitzmann. This system will provide private switched networks for integrated voice, data, and image services. Barnla's discussion concentrates on the overall system, and a companion paper by Lee Pressman of Hughes Aircraft Co., Los Angeles, examines the satellite's transponder and antenna hardware. Students of AT&T's proposed digital data service, called Advanced Communications System [*Electronics*, July 20, p. 41], for similar types of communication using telephone lines should find these papers very interesting.

Another hot topic, fiber-optic links, is the subject of two sessions. Session 34, "Fiberoptic Links Design and Installation Considerations," aims to give the technically diverse Wescon audience an overview of what problems will occur in real fiber-optic system operations. David R. Weller of Bell Laboratories, Murray Hill, N. J., is heading the session; his paper on an optical data bus system, co-authored with Kinichiro Ogawa, reviews a new low-cost fiber-optic data link that connects a PDP-11/45 minicomputer with peripheral terminals. The miniature circuit was designed to take advantage of the compatibility in dimensions of ICs and fiber cables. A computer-controlled fiber-optic test loop allows testing at different frequencies, temperatures, and cable lengths.

A paper by M. C. Hudson of Valtec Corp. in West Boylston, Mass., indicates the state of the art in the design and installation of fiber-optic cables, with examples taken from Valtec projects. The connector problem is examined by Peter Keeler of Augat Inc., Attleboro, Mass. He explores cable and fiber selection, connector loss, splicing methods, and component selection. ☐

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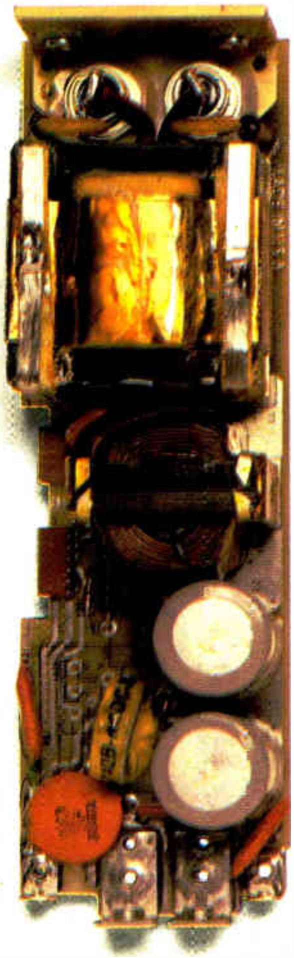

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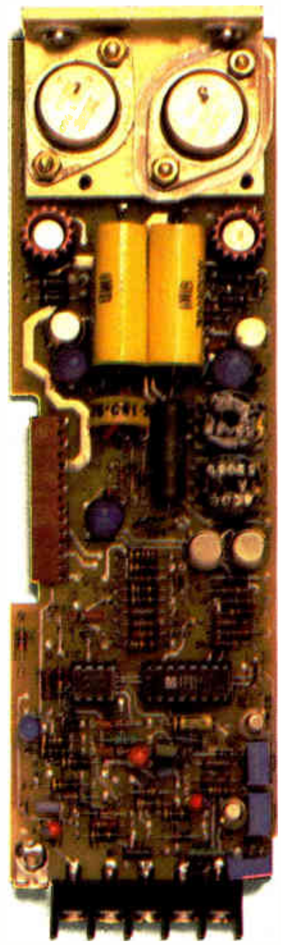

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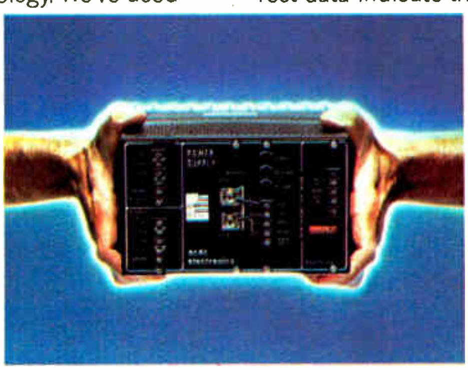

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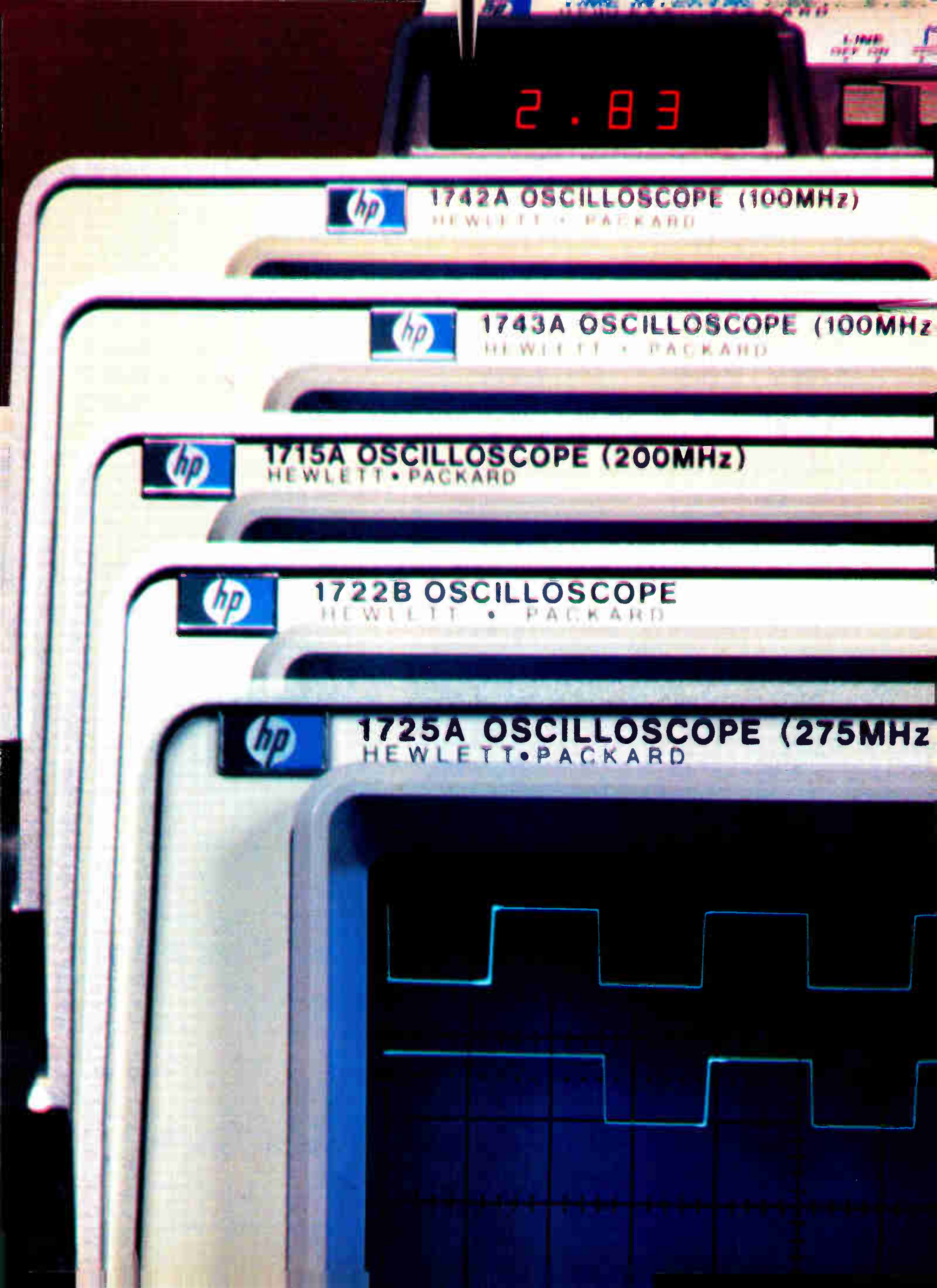
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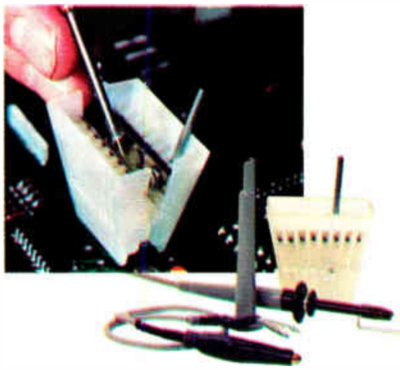

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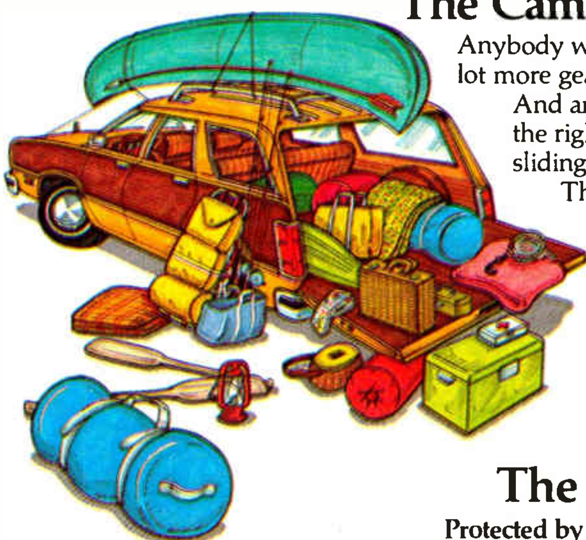

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The emphasis is on test instruments, especially digital equipment, at this year's show, Sept. 12-14, in Los Angeles

Generator is programmable and clean

Most signal generators fall into one of two categories: synthesizer-based units or tuned cavity oscillators with high spectral purity. Comstron/Adret of Freeport, N. Y., has introduced the model 7100, a programmable, low-cost signal generator with noise performance 10 dB better than that of most cavity generators. The model 7100 covers 300 kHz to 650 MHz (300 kHz to 1.3 GHz with an optional doubler) with 1-Hz resolution. It is a microprocessor-based synthesized signal generator featuring optional full programmability of frequency, modulation, and level, with better than −136 dB/Hz phase noise 20 kHz from the carrier and a noise floor of greater than 150 dBc.

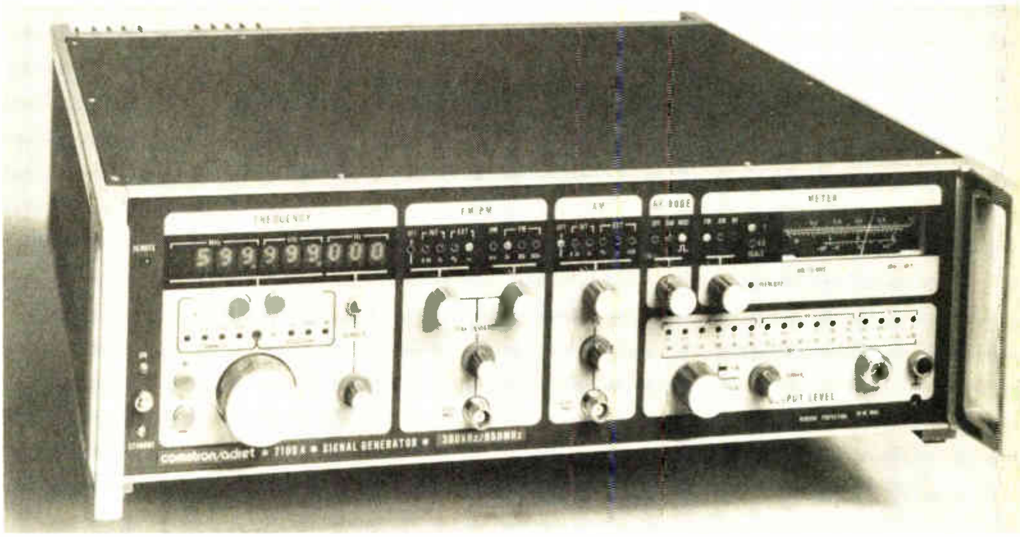
The frequency is continuously tunable and is displayed on a 9-digit light-emitting-diode readout (10 digits with optional frequency doubler). Decades of 1 kHz and greater are provided by a spin wheel, and a vernier provides 1-Hz resolution. All digits are programmable, and band switching is automatically directed by the microprocessor and is completely transparent to the user.

The unit's development was a joint venture, with the low-noise oscillator technology (patent pending) coming from the French codeveloper, Adret Electronique of Trappes. According to Joel Remy of Adret, "The development of the high-output, low-noise oscillator and low-spurious mixer required to produce this product was the result of an intense research effort over the past two years."

The 7100 is fully programmable through an IEEE-488 interface bus option. The microprocessor handles scaling and protocol and the entire unit can be programmed with one ASCII character string. Frequency switching time is 100 ms. Other specifications include a dynamic range of 160 dB, from +20 dBm to −140 dBm (2.24 V rms to 22.4 nV rms across 50 Ω). With the IEEE-488 option the attenuator is programmable in steps of 0.1 dB.

Nonharmonic signals are more than 100 dB down for frequencies beyond 10 kHz from the carrier, whereas harmonics are maintained more than 35 dB down across the band. Residual frequency modulation is less than 1 Hz in a 300-Hz-to-3-kHz band; residual amplitude modulation is less than −90 dB in the same band. Radio-frequency leakage is less than 1 μV using the standard two-loop method at 5 cm.

Available modulation modes include amplitude, frequency, phase, pulse, frequency-shift keying, and phase-shift keying. Provision is also made for a low-distortion VOR (very-



high-frequency omnidirectional radio ranging) modulation input—necessary for certain avionics applications. The unit permits simultaneous modulation, as well as optional programmability of all modulation functions. These functions include modulation type, percentage, and frequency.

The frequency stability of the 7100's internal time base is 5 parts in 10^9 per hour; for even better stability, the generator can be locked to an external 5-MHz reference standard.

The price of the basic 7100, which spans 300 kHz to 650 MHz, is $7,500. The frequency doubler needed to extend its range to 1.3 GHz adds $1,000. The IEEE-488 programmable-frequency and -level option and the programmable-modulation option add $1,800 and $700, respectively. A systems version with a blank front panel and frequency programmability sells for only $6,900. Delivery time is 12 weeks.

Comstron/Adret, 200 E. Sunrise Highway, Freeport, N. Y. 11520. Phone (516) 546-9700 [341]

V-MOS puts power into 50-MHz pulser

Systron-Donner's Instrument division has made what may be the first production pulse generator that uses V-groove metal-oxide-semiconductor field-effect transistors in its output stage. The model 101D is a $900, 50-MHz instrument that can provide an impressive 8 W of signal power, yet needs no fans or blowers.

The output transistor, a Siliconix MVP-4, "provides adequate current handling (400 mA) with no fear of secondary breakdown problems," according to Wayne R. Merryman, pulse-generator chief engineer. "If I had had to meet the price-performance design goals, but had been constrained to use bipolar transistors, I would most likely have scrapped the idea."

The new pulser differs from instruments in its price class in a second way: its output controls operate in two modes. A switch gives users a choice of upper-and-lower-voltage-level control or amplitude-and-baseline control. In the latter mode, the user may fix the baseline at zero, but retain control of the amplitude.

Heat, the eternal enemy of things electronic, could have been a problem, but Systron-Donner countered the threat by using a switching power supply in the 101D. It may seem to have been a risky design decision to employ a switcher in a signal source, but, as Merryman explains, "the switcher is isolated physically and electrically from critical areas of the pulse generator." The high efficiency of the switching supply keeps the overall heat dissipation down to a level that obviates the need for a cooling fan.

Against such formidable competition as Hewlett-Packard and Wavetek, Merryman sees the 101D as a potential "giant killer." "It's a 50-MHz box that can provide pulses up to 20 V at 400 mA under 50-Ω load conditions. In fact, it has almost every feature except burst." Its control flexibility makes the unit compatible with all logic technologies, although it is frequency-limited in its emitter-coupled logic uses.

The 101D has provisions for external triggering, manual triggering, and synchronous and asynchronous gate control. Repetition rate is continuously variable from 1 Hz to 50 MHz in eight ranges. Pulse delay is variable from 25 ns to 1 s, and pulse width is controllable from 10 ns to 1 s. The output amplitude can be adjusted from below 250 mV to 20 V, with a switch giving control of pulse polarity.

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power source of 100–125 or 200–240 V ac at a frequency of between 50 and 400 Hz. It draws approximately 40 W and may be operated at ambient temperatures from 0° to 50°C, according to the company.

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Systron-Donner Corp., 10 Systron Dr., Concord, Calif. 94518. Phone (415) 676-5000 [342]

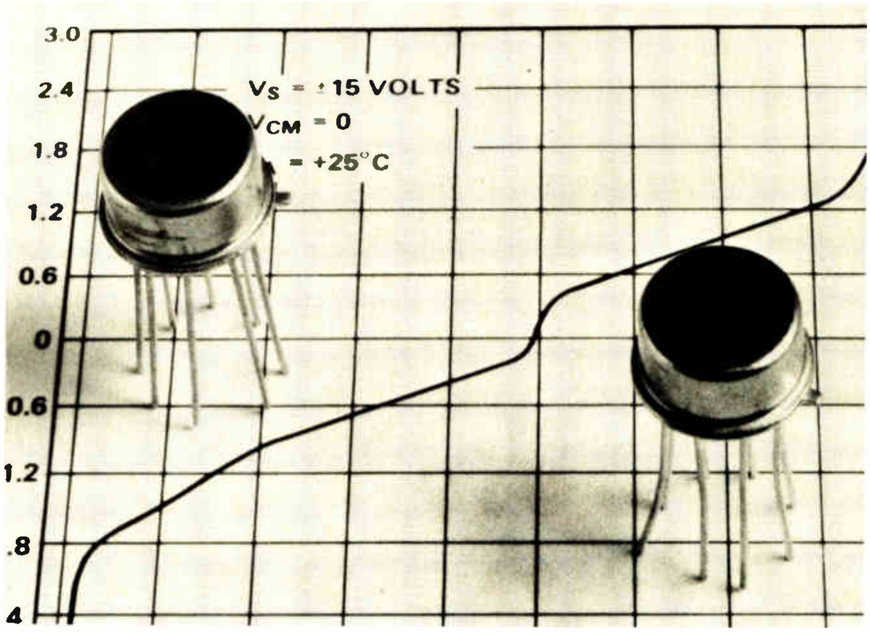
Op amp has low bias current and drift

"Very seldom are FET-input devices made with both low bias current and low offset-voltage drift," says Richard E. Frantz, products marketing engineer at Analog Devices' Semiconductor division. However, his company is offering just that in its model AD545 operational amplifier.

The two-chip hybrid also features high input impedance, low quiescent power consumption, and low noise. The input bias current is specified at 2 pA maximum for the bottom-of-the-line J version and 1 pA maximum for the K, L, and M versions. Differential input impedance is 10^{13} Ω in parallel with 0.8 pF.

By using laser trimming, low input-offset voltages are obtained: 1 mV maximum for the J and K units, 0.5 mV for the L, and 0.25 mV for the M. Input-offset voltage drift is 25 μV/°C for the J version, 15 μV/°C for the K, 5 μV/°C for the L, and 3 μV/°C for the M.

The quiescent current—1.5 mA maximum and 0.8 mA typical—is half that of most op amps, according to Frantz. The low power consumption means that the AD545 can be put into battery-operated portable instruments, where it can extend battery life or the interval between rechargings. Moreover, as Frantz explains, the low power consumption means a low temperature rise, which, in turn, means low drift. Bias current doubles every 10°C, he notes.



Low input noise current and voltage are also important features of the op amp. With 3.0 μV peak to peak for the J, K, and L versions, 5 μV for the M, and 0.01 pA across the board from 0.1 Hz to 10 kHz, the AD545 will be useful whenever low input noise is a requirement.

The device is designed for operation from ±15-V supplies, but can operate anywhere in the range from ±5 V to ±18 V. It is packaged in a TO-99 can and has an operating temperature range of 0° to 70°C.

Applications for the 545 include pH-sensitive electrodes, photocurrent detectors, and vacuum ion-gage meters. In quantities of 100 and up, prices for the J, K, L, and M versions are $5.95, $7.90, $10.75, and $18, respectively. Delivery of any of the various models offered is from stock.

Analog Devices Inc., Semiconductor Division, 829 Woburn St., Wilmington, Mass. 01887. Phone (617) 935-5565 [346]

Counter resolves 0.01 Hz in 1 s

When shopping for a small, portable electronic frequency counter, you would hardly expect to find one that combines a top frequency of 1.25 GHz with the capability of resolving audio-frequency signals to 0.01 Hz in 1 second. Yet that is what you will find in Ballantine Laboratories' model 5722A 8-digit counter—a $950 instrument that consumes a mere 8 W of power.

Intended for mobile communications, navigation, and other general-purpose field and laboratory applications, the 5722A may well be the smallest instrument of its kind. Measuring 2.375 by 8.3 by 9.03 in., it weighs less than 3 lb and uses 0.43-in. light-emitting-diode readouts to display its readings. Operation is from any 9-to-15-V dc source, such as an automobile or boat battery. Wall-mounted ac-to-dc power adapters for 115 V ac and 230 V ac are available as options.

A standard feature in the 5722A (but an extra-cost option in most, if

not all, competitive instruments) is the audio-tone multiplier circuit that permits signals up to 1 kHz to be resolved to 0.01 Hz and signals up to 10 kHz to be resolved to 0.1 Hz in 1 s. In its multiplier mode, the counter is "ideal for quickly setting selective audio tones in two-way communications systems," says Milton J. Lichtenstein, marketing vice president. What's more, "conventional counters in the field today require up to a hundred times longer measurement time and cost hundreds of dollars more," he claims.

A front-panel adjustment provides continuously variable input sensitivity to accommodate large-amplitude signals and to discriminate against noise. For sine waves, sensitivity is 15 mV rms from 10 Hz to 32 MHz and 50 mV rms from 32 MHz to 150 MHz. For fast-rise square waves, the counter has a peak-to-peak sensitivity of 40 mV from 1 Hz to 32 MHz and 140 mV from 32 MHz to 150 MHz. In the high-frequency mode, sensitivity is 15 mV rms from 25 to 500 MHz, 25 mV from 500 MHz to 1 GHz, and 40 mV above 1 GHz.

The 5722A's standard 10-MHz crystal-controlled clock has an aging rate of less than 2 parts per million per month and a maximum temperature sensitivity of 5 parts in 10^7/°C from 0° to 40°C. A temperature-compensated crystal-controlled clock with an aging rate of 1 part in 10^8 per day is available as an option.

Another important option is provision for external programming and parallel binary-coded decimal outputs for systems and remote applications, Lichtenstein points out. The programming feature allows command of remote or local (front-panel) manual operation as well as selection of either the direct 150-MHz or prescaled 1.25-GHz inputs and selection of gate time, he notes. The counter is available from stock to four weeks.

Ballantine Laboratories Inc., P. O. Box 97, Boonton, N. J. 07005. Phone (201) 335-0900 [350]

Language seeks the golden mean

Generally, most experts agree that while a good assembly language uses fewer bits and allows faster execution of instructions than do high-level languages, it also takes longer to prepare and to alter—factors that make it more expensive and, hence, cause it to lose favor with software management. So after looking over competing languages already at work in the software development field, applications engineers at Rockwell International's Microelectronic Devices division decided to seek a middle course, designing a language they believe combines the best of both approaches.

Intended to support the R6500 family of microprocessors, which now comprises 10 central processing units, the PL/65 language is implemented as a resident compiler on the firm's System 65 microcomputer development system. In general form it resembles such other high-level languages as PL/1 and Algol. It is supplied on a minifloppy diskette that can work on a microcomputer development system with a 16-K random-access memory.

"The PL/65 has the structuring potential and programming ease of a high-level language, but retains the power and flexibility of an assembler," claims Robert A. Stow of the Anaheim, Calif., division, who was instrumental in its development. "Its design encourages and supports a modular, structured utilization of processing and memory resources that simplifies writing programs."

Key to accommodating the assembly-language inputs to the high-level format are the "optimal code-generator techniques and interfaces that are employed," according to Rockwell staff members. These are particularly aimed at those points in the software development cycle where much more detailed programming instructions—that is, multiline codes—help ensure the integrity of final system control. A critical point in the development sequence typically is the output of the compiler where host high-level languages "spit out bit patterns that are already in a machine-executable object code," according to Stow and Rockwell staff members. But the Rockwell language instead causes the program compiler to produce a conventional language code that gives the programmer the option to further enhance it by writing assembly instructions and then embedding them directly into the program.

"This gives a programmer the flexibility to incorporate routines to meet such requirements as extremely stringent timing control," Stow continues. Prospective industrial process users particularly like this feature, Rockwell marketing personnel find, because they feel it gives them more

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control in directing precise production operations than does a high-level language alone.

One feature that Rockwell claims as unique to its language is installation without any additional memory modules. "Most other microprocessor high-level languages require expensive extra memory added to the host development system," according to Stow. PL/65 statements are written using resident read-only memory, with source program results of compilation directed to disk memory. These are loaded into resident random-access memory for editing. When programming, including in-circuit emulation, is completed, the final object code is loaded into programmable ROM for demonstration. For production systems the code is put on low-cost ROM.

In applying the Rockwell language to highly formatted programs, general control structures for conditional and iterative looping allow great flexibility. These language statements include: assignment, integer arithmetic, conditional looping (WHILE-DO), collective execution (BEGIN-END), conditional execution (IF-THEN), and setting up arrays. Also block structures, subscripts, and parenthetical expressions may be supported.

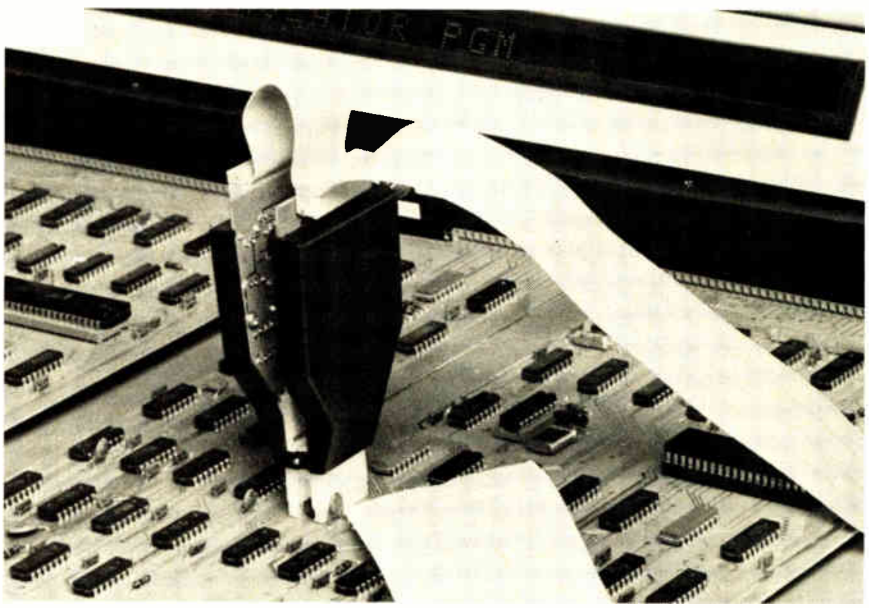
With minifloppy diskette and PL/65 users manual, the price of the language is $500. It is available immediately.

Rockwell International Microelectronic Devices, P. O. Box 3669, Anaheim, Calif. 92803. Phone (714) 632-3729 [363]

Fault emulator speeds checking of logic-test programs

As program-development and debugging costs displace the cost of capital equipment as the major factor in automatic test equipment budgets, Fluke Trendar has been putting much of its design effort into reducing software costs. Until now, however, the debugging of test programs for all testers geared to checking out printed-circuit boards depended heavily on feedback from the production area on board problems not picked up during testing.

The company's new AFE (automatic fault emulator), designed to be used with the 3040A Autotrack Logictester, lets the programmer simulate the simple and complex faults likely to occur on pc boards and thus determine how effectively



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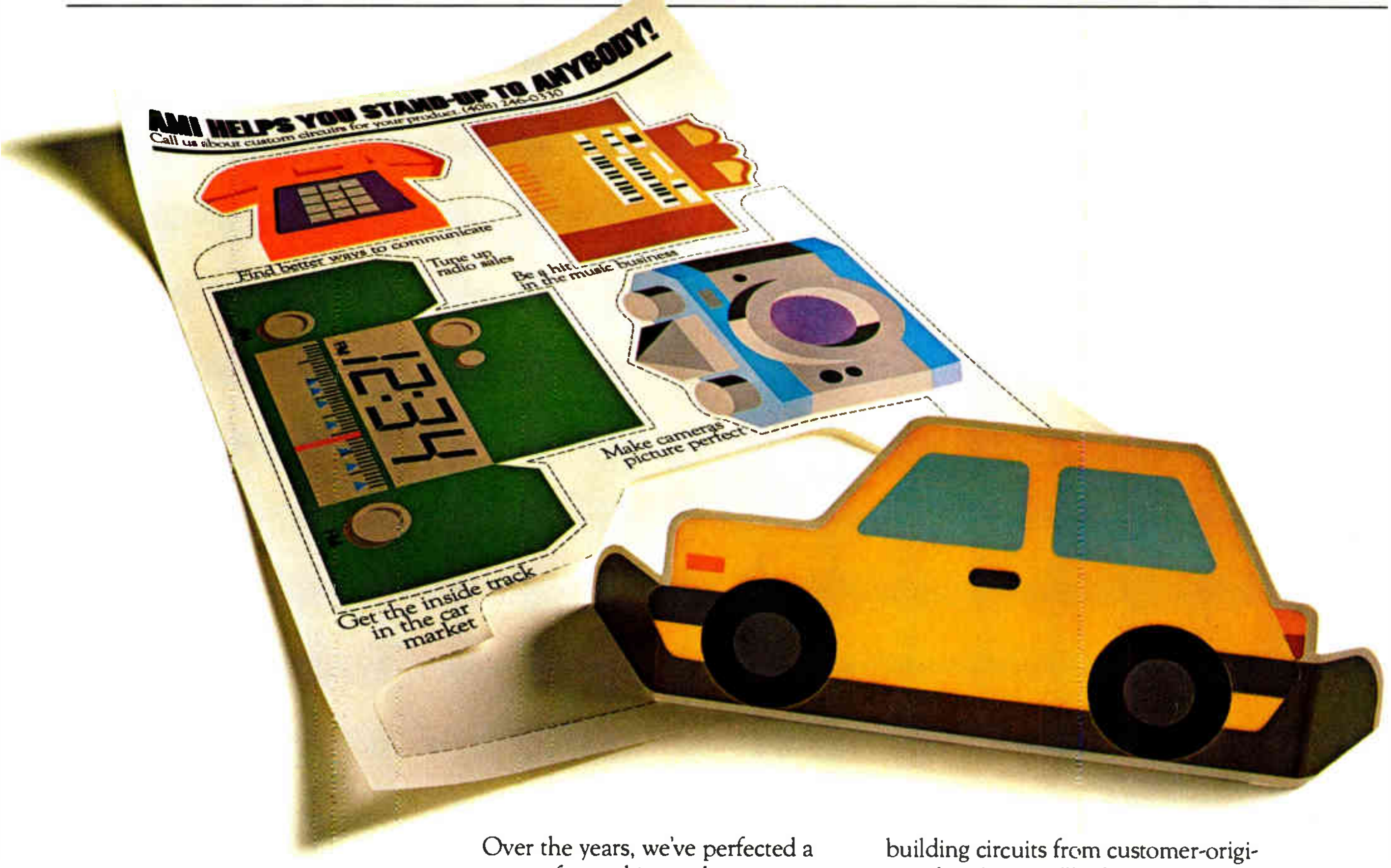

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his program uncovers them.

The AFE is a natural extension of the concepts that Fluke Trendar's engineers developed for testing boards loaded with large-scale integrated circuits. As the functions on the board expanded from system subsections to entire miniature computer systems, the effectiveness of bit-by-bit stored-sequence programming waned both in terms of the fraction of faults detected and the time required to write the programs.

The 3040A, therefore, while providing stored-sequence capability, also provides for the automatic generation of long, complex digital sequences. These can be programmed quickly, yet are effective in fully activating a complex digital-circuit board, according to Gary E. Miller, product manager.

The AFE works together with the 3040A's software to enable the programmer to apply any or all of six fault conditions to each node tested by the program. This will determine whether or not the faults ripple through the circuitry to the board's edge connector, where they can be detected. According to Miller, most testers have a means for simulating stuck pins, but the problems that have begun to haunt the programmers are of the intermittent, low-duty-cycle type that result from opens and shorts buried deep within LSI circuitry.

These faults only occur on a board node occasionally and may not be picked up by the tester, he says. By simulating these intermittent faults, the programmer can determine whether his test plan is efficient enough to detect them. Whereas the individual-node test may not pick up these failures, a well-done program should weed them out by producing a signature for the bad board that is not identical with that of a known-good board, Miller explains.

The six faults that the AFE can simulate are stuck high, stuck low, stuck high/low (an alternating of logic levels at the node), intermittent high, intermittent low, and intermittent high/low.

Pushing a button on the Autotrack printer console initiates the AFE, which then guides the programmer through a series of yes/no questions and tells him where to put the clip. As the programmer proceeds, the AFE keeps track of the results and later makes a printout with figures of merit both for how effectively his program activates the board (toggles each output) and how successfully it detects each of the six types of faults.

The AFE is priced at $4,500. It can be ordered with a new 3040A or retrofitted to an old one. Delivery time is 10 weeks after receipt of order.

Fluke Trendar Corp., 630 Clyde Ave., Mountain View, Calif. 94043. Phone (415) 965-0350 [344]

Low-cost multimeters reach new heights

There can't possibly be any more features available in a low-cost 3½-digit multimeter that you haven't seen before, can there? Wrong! Just take a look at Fluke's latest: the $239 8010A and the $299 8012A.

Both feature true-rms response on their ac voltage and current ranges. Both combine liquid-crystal displays with true-rms circuitry that automatically powers down when not in use to minimize power consumption. And both offer three conductance ranges (200 nanosiemens, 20 μS, and 2 mS) in addition to their six resistance ranges.

What differentiates the meters from each other is the 10-A current range of the 8010A and the 2-Ω and 20-Ω ranges of the 8012A. Otherwise the meters are identical. Their rms response extends to 50 kHz (typically 3 dB down at 200 kHz), their current ranges go from 200 μA full scale to 2 A, their voltage ranges extend from 200 mV F.S. to 1 kV dc and 750 V ac,

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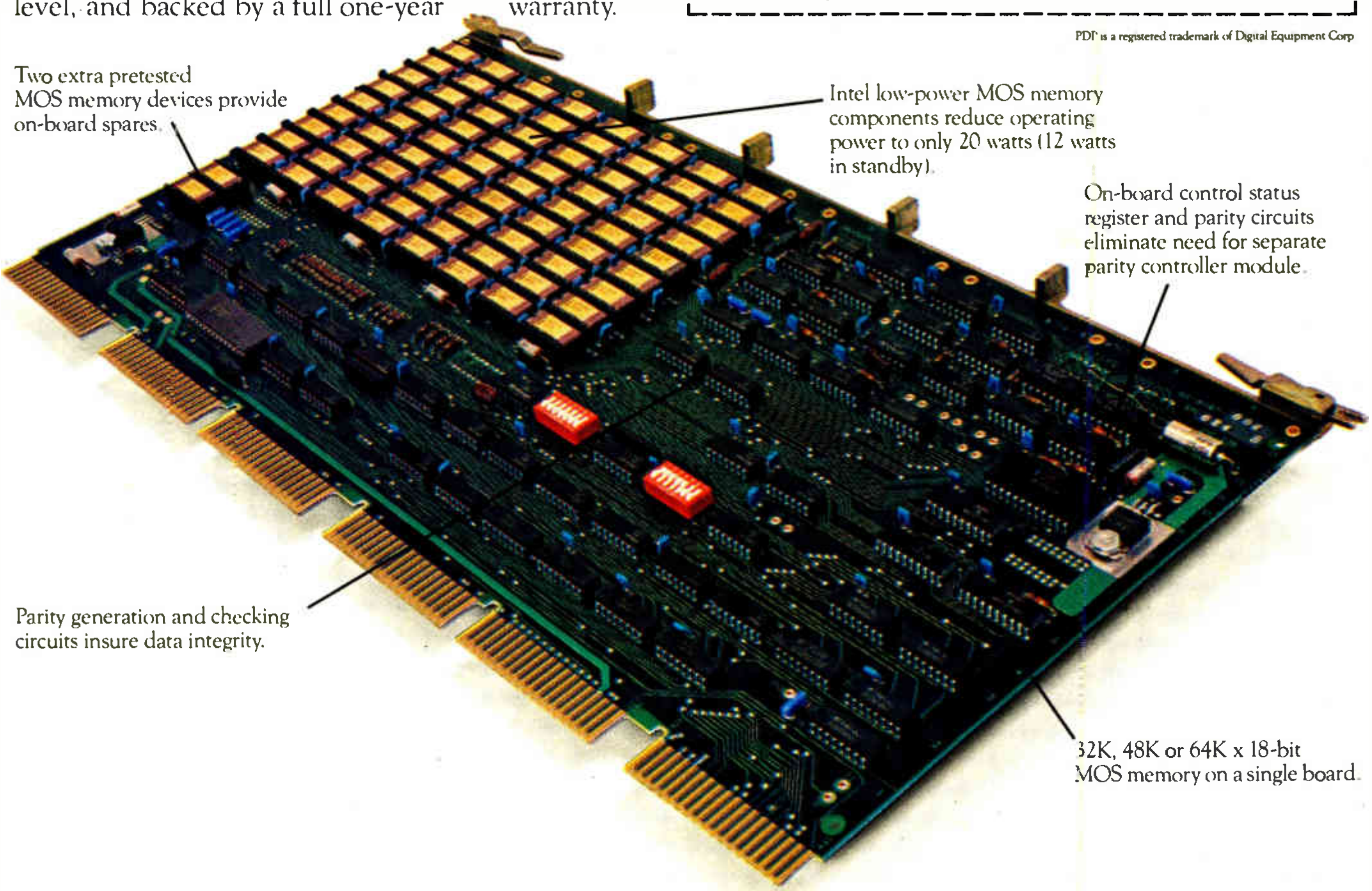
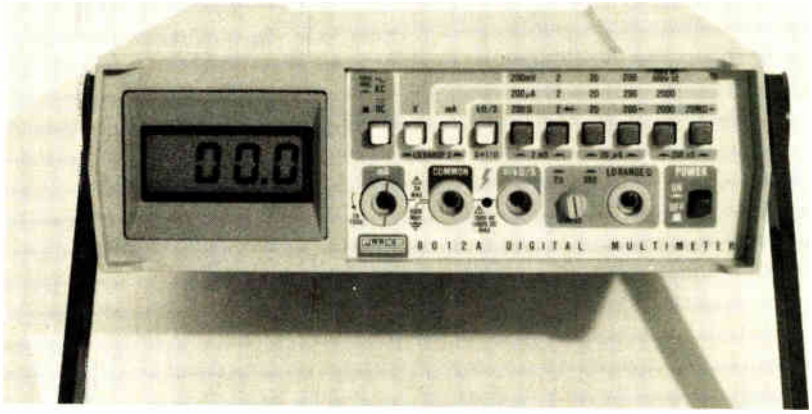




and their resistance ranges span 200 Ω F.S. to 20 MΩ.

Could there be more? How about a touch-and-hold feature for displaying voltage and resistance measurements until it is released? Or current input fuse protection up to 600 V in addition to the input overload and transient protection usually supplied? For those who want to use the new meters as battery-operated portables, a rechargeable battery pack and charger is available for $40. The instruments are available from stock, the company says.

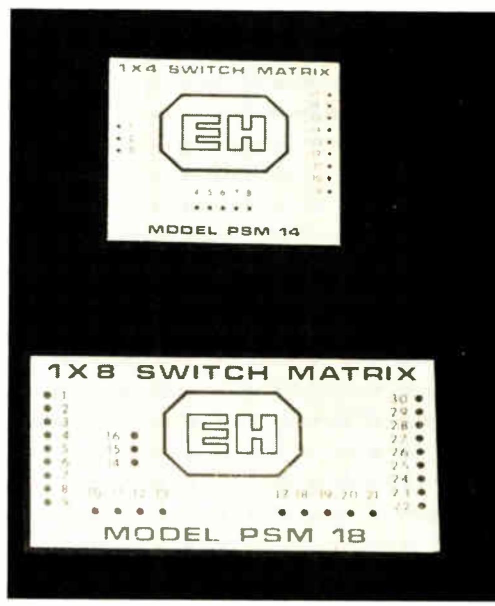
John Fluke Manufacturing Co., P. O. Box 43210, Mountlake Terrace, Wash. 98043 [343]

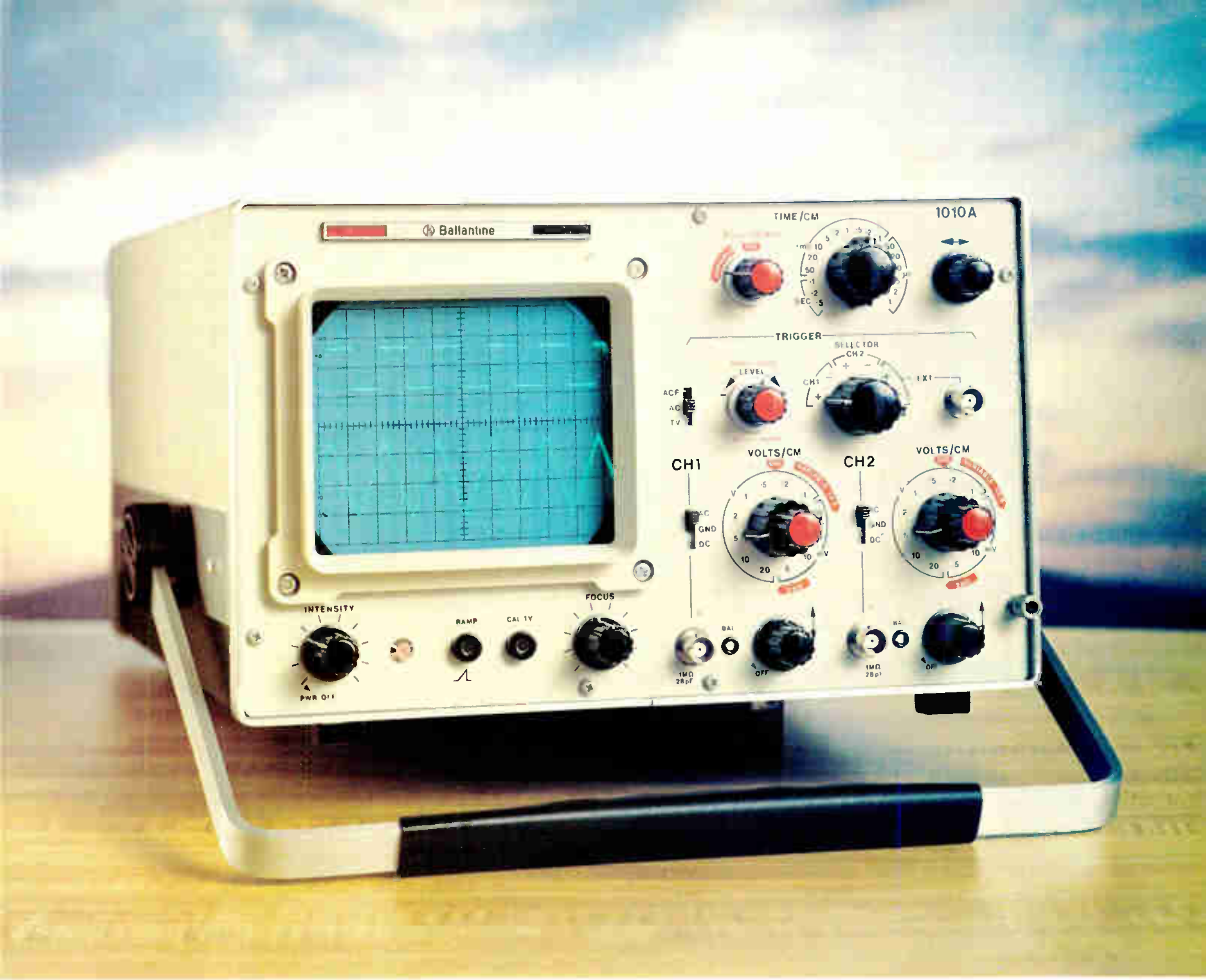
Switching modules have bandwidths up to 700 MHz

Whether designed to test integrated circuits or printed-circuit boards, a truly flexible automatic test system depends heavily on a complex network of signal switches to handle the distribution of inputs and outputs among the pins of the product under test. Conventionally, this switching is accomplished by pc boards loaded with individual reed relays—as many as 1,200 for a 40-pin tester. Now, to make the switching scheme more reliable and to ease the stringent layout requirements on high-speed signal sector boards, E-H International has developed a series of switching modules, with 1-by-2, 1-by-4, and 1-by-8 switch matrixes.

At first glance, it may seem a simple task to arrange some relays on a small circuit board, encapsulate it, and call it a module. However, according to Richard C. Nyder, product line manager at E-H, "achieving useful bandwidths within the module is not a trivial design problem." The bandwidths he refers to are impressive: 700 MHz for the 1-by-2 unit, 500 MHz for the 1-by-4, and 350 MHz for the 1-by-8—all at their 3-dB points.

With bandwidth specifications like these, it would seem that the





Ballantine
1010A
TIME/CM
TRIGGER
LEVEL
SELECTOR
EXT
CH1
CH2
VOLTS/CM
GND
DC
INTENSITY
RAMP
FOCUS

modules are designed especially for testing emitter-coupled logic. "Not so," Nyder says. "It's true that the switch modules are ideal for ECL applications, but they are not aimed at a strictly coaxial environment—they'll work well with transistor-transistor-logic circuits, too."

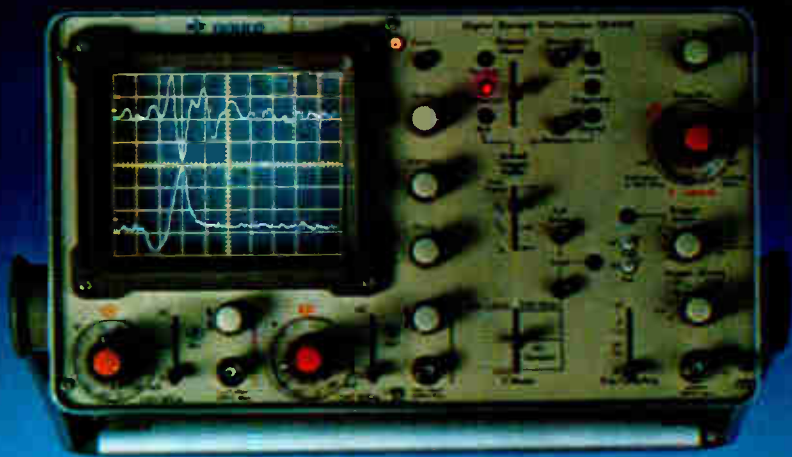
Nyder is not sure how large-volume test equipment manufacturers will accept the modules. "They may balk at paying two or three times more per relay," he explains. However, he believes that designers working on systems to be built in small numbers will save significant amounts of time and money if they use the programmable switching modules. The savings will come, he says, from shorter layout times and better impedance integrity. Ultimately, he says, "E-H would like to be the Heathkit of the automatic test equipment world," by providing products that no one else is offering.

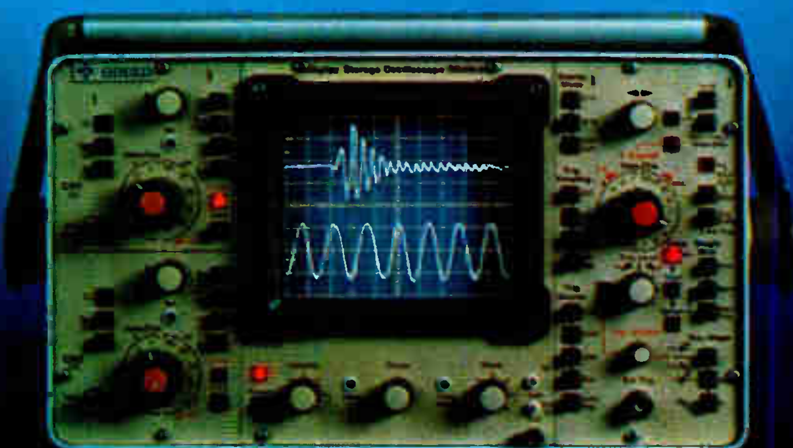
Production quantities of the modules will be available in October. Prices, for 20-piece quantities, are approximately $50 each for the 1-by-2 PSM 12, $80 each for the 1-by-4 PSM 14, and $125 each for the 1-by-8 PSM 18.

E-H International Inc., 515 11th St., Oakland, Calif. 94607. Phone (415) 834-3030 [347]

PROM programmer has C-MOS RAM buffer work space

The rapid growth of programmable read-only memories spawned the need for programmers that could handle all PROM families regardless of technology type or size. Pro-Log's answer was to use a 4-bit, microprocessor-based design so that any PROM family could be programmed with a simple change of the personality module. Now, the company's designers have added a two-kilobyte random-access-memory buffer, made with the latest complementary-metal-oxide-semiconductor tech-





nology and have given the new programmer, the M900B, several useful data-manipulation and programming capabilities.

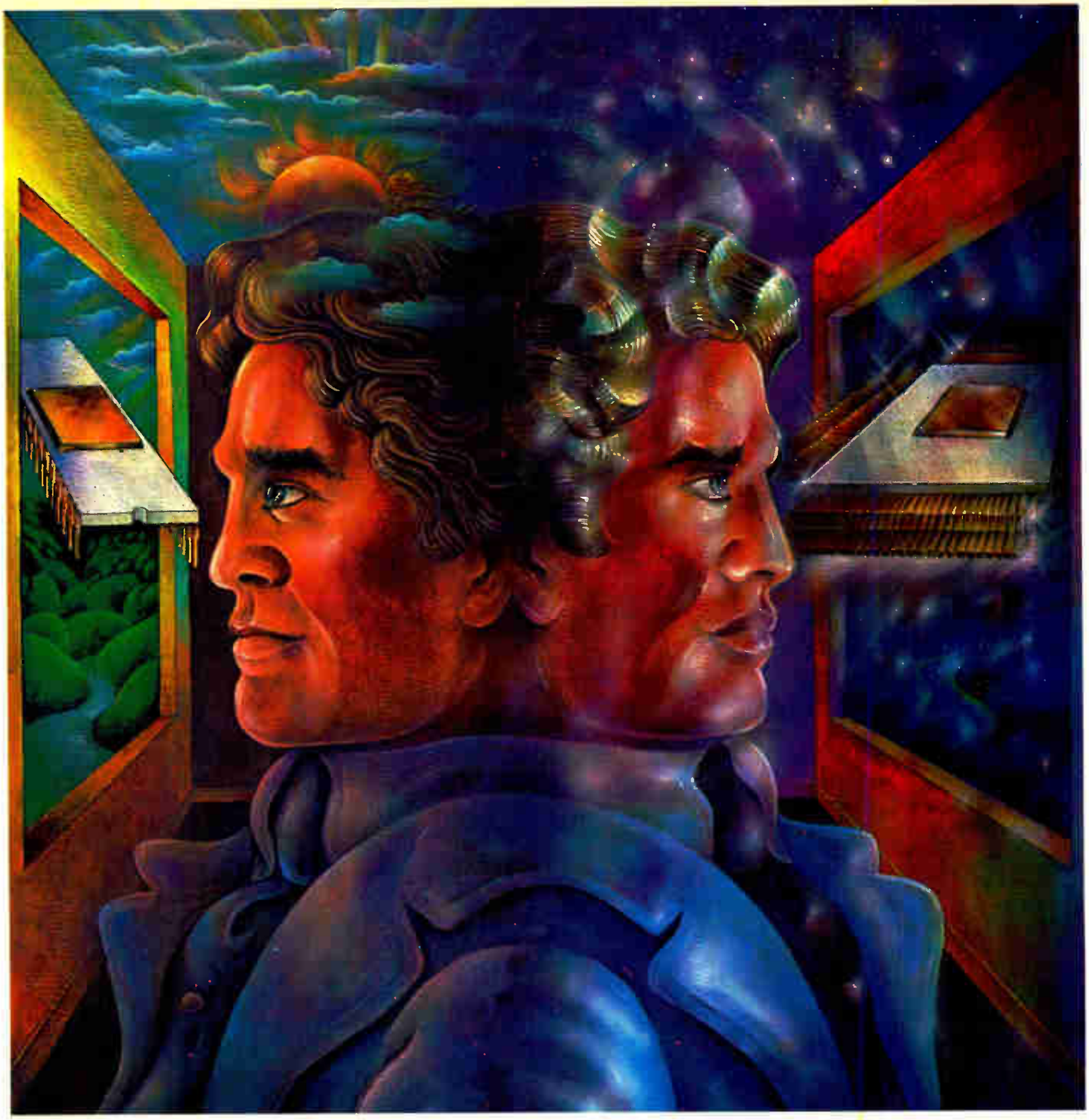
One new buffer-related feature, called data manipulation, allows the operator to transfer any section of the program stored in the buffer to any location in the PROM being programmed. The key to this capability is in "the way we set up our address definition," explains Shay Adams, international marketing manager. In the past, users had no such flexibility; they had to rewrite the program, he says.

The C-MOS RAM buffer offers the user a convenient, in-the-box, program work space: he can list buffer contents, change them, program a blank PROM, and immediately verify its program against the buffer's contents. Furthermore, when a development system's computer is down-loading a program into the M900B, the buffer serves to make the procedure more time-efficient by eliminating the pauses that are common to direct computer-to-programmer interfaces, Adams says.

A unique feature results from the combination of data displacement, C-MOS technology, and a stiff power supply. The C-MOS RAM buffer retains stored data for up to a minute after the power is switched off. "That's more than enough time to power down, change PROMs, switch personality modules, power up, and program a new PROM," Adams points out. Thus, a user can sequentially load programs from four small (256-by-8-bit) PROMs into the buffer, power down, swap modules, then load all the stored programs into a single, large (1,024-by-8-bit) PROM.

All the features of the original M900 are retained in the new programmer: it is portable, has a 16-key data-entry keyboard, a six-digit hexadecimal display, and automatic zero checking. The checking feature allows it to examine the PROM and indicate whether or not the defined address field is all 0s before attempting to program.

Like the rest of Pro-Log's instrument line, the M900B is listed with



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Still testing devices one at a time? By multiplexing the 120 fully programmable I/O pins on the Sentry VIII you can test two, even three, LSI devices simultaneously. Another 50% to 60% savings in test time.

And you can save even more. To provide lower operating costs, the Sentry VIII features multi-task (foreground/background) software for simultaneous compiling, editing and testing; a CPU that provides 50 to 200% faster throughput; a sequence processor to handle high complexity devices; and a pattern processor to tackle the largest memories.

Still don't think you're ready for a true 120-pin tester? Maybe you'd better think again.

Fairchild Test Systems Group, Fairchild Camera and Instrument Corp., 1725 Technology Dr., San Jose, CA 95110 (408) 998-0123

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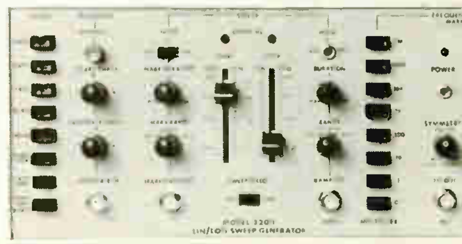
Underwriters Laboratories. Available now for $2,100, it comes with a carrying case. Options such as paper-tape reader, serial and parallel communications interfaces, a checksum board, and an additional 2,048 by 8 bits of add-on C-MOS RAM buffer are also available.

Pro-Log Corp., 2411 Garden Rd., Monterey, Calif. 93940. Phone (408) 372-4593 [345]

Generator works in many modes

A sweep/function generator that goes up to 30 MHz is certainly quite respectable. But Krohn-Hite's latest has more going for it than just a high top frequency. The model 2200 has eight modes of operation, including various gated, triggered, and burst variations on its basic continuous-wave and swept modes. "Quite a few generators have this (up to 30 MHz) frequency range," observes William C. Kulas, the company's vice president for engineering, "but it's the sweep capabilities of the 2200 that make it convenient."



Among those capabilities is a pause/mark feature, which is used in conjunction with the sweep modes. This feature makes the sweep pause for an adjustable length of time at a frequency set by the instrument's main frequency/marker dial. When the generator is used in conjunction with an oscilloscope, the pause creates an intensified region on the trace, making it easy to identify key points on a frequency-response plot.

The pause duration is variable from 0.1 ms to infinity. The marker is accurate to within 2% of full scale for each of the lower seven bands and to within

3.5% for the eighth band. The decade bands each span a 1,000:1 range: band 1 covers 0.003 Hz to 3 Hz, whereas band 8 spans 30 kHz to 30 MHz.

The 2200 can produce the following waveforms: sine, square, triangle, positive- and negative-pulse, and ramp. Its cw frequency accuracy is the same as its marker-frequency accuracy. Maximum peak-to-peak output voltage is 30 V into an open circuit or 15 V across 50 Ω.

Among the many operating modes are multiple-cycle burst using an external or front-panel gate, triggered-sweep burst, and continuous linear and logarithmic sweeping. Auxiliary outputs include a ramp generator output, a gate output, a log output, and a transistor-transistor-logic output.

Applications for the 2200 include swept video and communications testing, checking the noise immunity of complementary-metal-oxide-semiconductor logic, and frequency-response testing of amplifiers and filters. The generator sells for $1,295 and has a delivery time of 60 days.

Krohn-Hite Corp., Avon Industrial Park, Avon, Mass. 02322. Phone Ernie Lutfy at (617) 580-1660 [362]

Printer fits in tight places

A self-contained alphanumeric printer small enough to fit into those tight spaces on an instrument has always been a very desirable, albeit virtually unobtainable, commodity. But Datel Systems is going to change that with a microprocessor-based, panel-mounting printer dubbed the APP-20.

The printer, which uses a thermal print head and offers the full range of ASCII characters, differs from other printers in that "it's one of the only ones that has all of its electronics in one package—and it's an alphanumeric printer," explains Lawrence D. Copeland, product marketing manager. He also notes that "this is a small printer compared to most others."

And small it is. With dimensions of 4.44 by 2.70 by 8.75 inches, the

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position-sensors are paving Detroit's way to better performance & lower cost

Our EGR, TAS and TPS position-sensors perform smoothly, accurately and noise-free for up to 250 million cycles. They feature RESISTOFILM (U.S. Patent #3,457,537), a hard, smooth conductive plastic film which is bonded to a flexible high-temperature substrate.

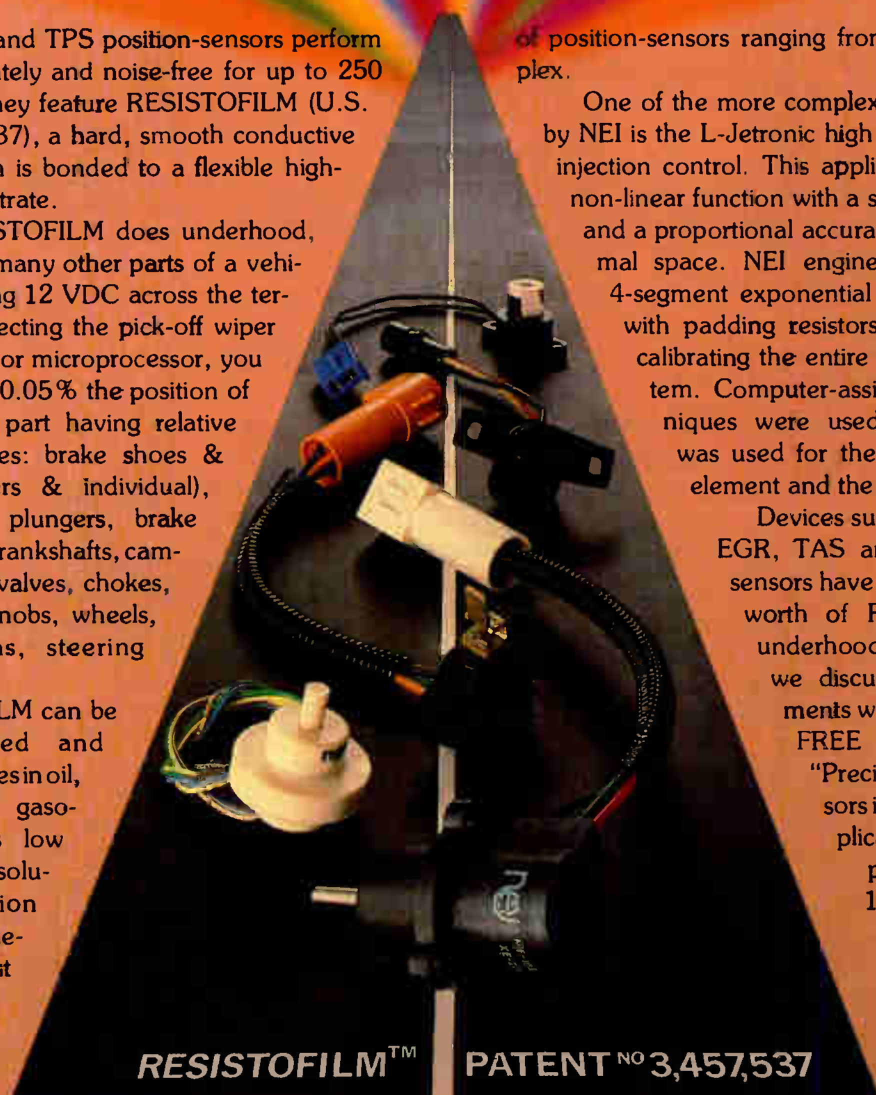
What RESISTOFILM does underhood, it can also do in many other parts of a vehicle. By connecting 12 VDC across the terminals and connecting the pick-off wiper to your indicator or microprocessor, you can sense within 0.05% the position of any automotive part having relative motion. Examples: brake shoes & cylinders (masters & individual), shock absorber plungers, brake pedals, pistons, crankshafts, camshafts, throttles, valves, chokes, floats, springs, knobs, wheels, gears, antennas, steering wheels..........

RESISTOFILM can be flexed, punched and bonded. It operates in oil, diesel fuel, and gasoline. It features low noise, infinite resolution, multi-million cycle life, tight linearity, and low cost in volume production. It can improve the performance of position-sensors ranging from simple to complex.

One of the more complex devices supplied by NEI is the L-Jetronic high performance fuel injection control. This application required a non-linear function with a slope ratio of 40:1 and a proportional accuracy of 1% in minimal space. NEI engineers developed a 4-segment exponential function element with padding resistors which allow for calibrating the entire fuel injection system. Computer-assisted design techniques were used. RESISTOFILM was used for the variable resistive element and the padding resistors.

Devices such as this and our EGR, TAS and TPS position-sensors have demonstrated the worth of RESISTOFILM in underhood applications. May we discuss other requirements with you?

FREE ON REQUEST: "Precision Position-Sensors in Automotive Applications," a paper presented at the 1978 SAE Congress & Exposition by William Wheeler, Laboratory Manager, NEI R&D Dept.



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Circle 191 on reader service card

New products

APP-20 occupies a mere 105 cubic inches of space and weighs under 5 pounds. Despite its size, it prints the full ASCII font in 20 column lines. The dot-line thermal print head forms characters at the rate of 1.5 lines per second using a five-by-seven-dot matrix. Characters twice the height of the regular ones are also a feature of the printer.

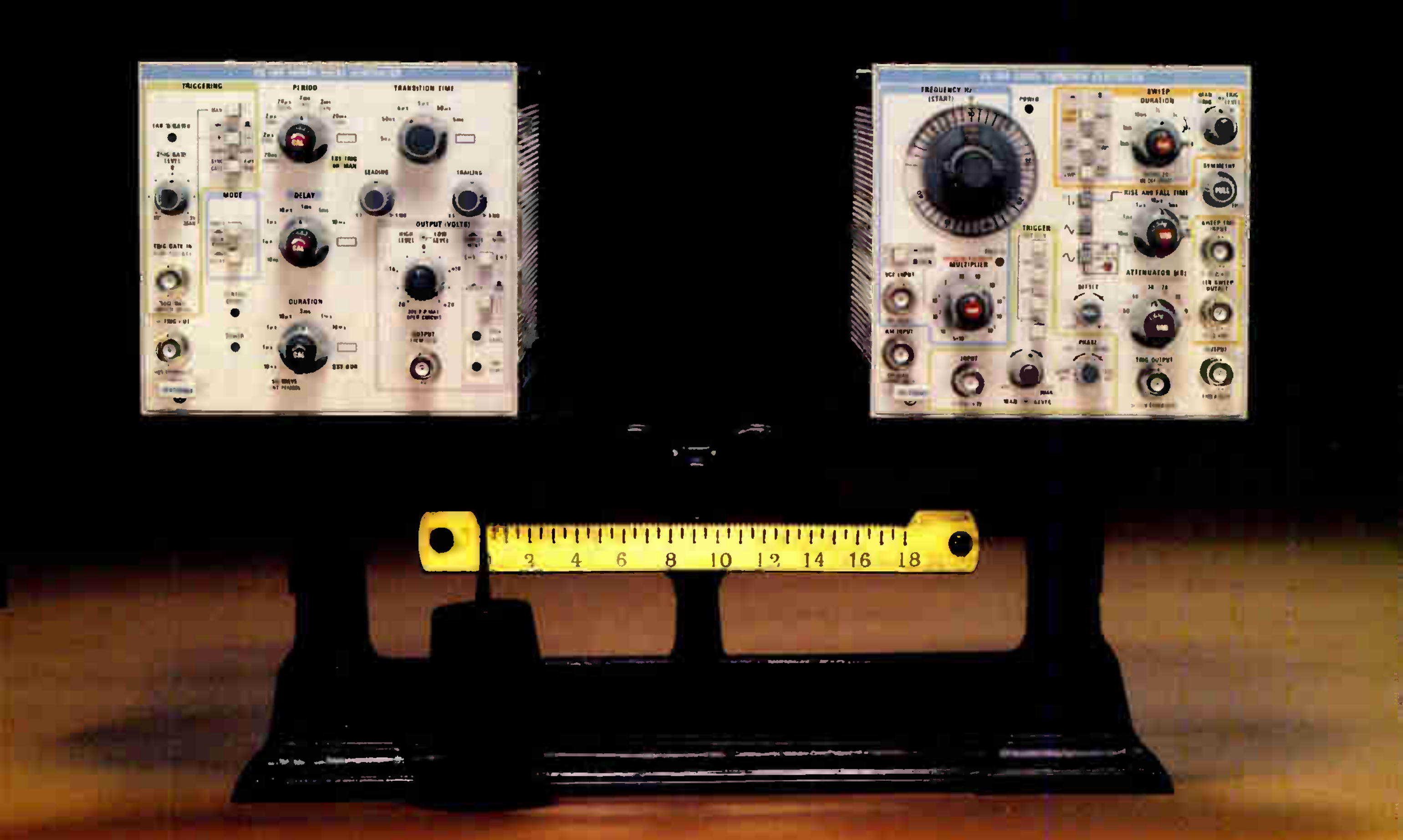
Working in a listing mode, the APP-20 can tabulate horizontally to positions 4, 9, and 15 automatically, as well as advance 11 lines if needed. In text format, the first line is printed upside down starting at the right margin, at the bottom of the printout. A single character mode is also available for keyboard echo.

All inputs may be selected as positive true or negative true, allowing direct connection with a variety of instruments and microprocessors. "The easiest hookup will be with microcomputers, because looking into the printer you see an 8-bit parallel port of a microprocessor: it's really one microprocessor looking at another," observes Copeland. Characters usually enter the unit's 20-character line buffer as 8-bit parallel asynchronous words. A handshake interface is implemented with a carriage return or print command.

The APP-20 has its own dual-voltage transformer, which accepts switch-selected input power at either 115 or 230 V ac ±10%. Power consumption is about 25 W, maximum, and 500 mA at 5 V may be diverted from the printer to power other external devices.

Primary uses for the unit will be in

Pulse Generator or Function Generator? Let Tektronix help you decide.



When you're considering a generator for your applications, think twice. Both pulse and function generators have special advantages and making a decision between them can be tough.

At Tektronix we build high performance pulse and function generators. We know the versatility of each instrument. We also know the individual characteristics of the two generators that make evaluation of both necessary.

We can help you make that evaluation. The following comparison chart is based on our 50 MHz Pulse Generator (PG 508) and our 40 MHz Function Generator (FG 504).

PG 508	FG 504
Similar Features	
50 MHz	40 MHz
20 V p-p from 50 Ω ± 20 V window	30 V p-p from 50 Ω ± 20 V window
20 V max unipolar output	15 V max unipolar output
Unique Features	
Constant pulse width w/changes in frequency	Constant duty cycle w/changes in frequency
Delay and double pulses	Phase lock to an external signal
High/Low voltage controls	Voltage and offset controls

And, there's more. We've prepared an in-depth evaluation of the capabilities of these two instruments, and we'd like to give you a copy. (Just circle reader service number below.)

For Technical Data circle #28 on Reader Service Card
For Demonstration circle #193 on Reader Service Card

These instruments are members of the TM 500 Family of Modular Test and Measurement Instrumentation from Tektronix. Both generators combine high performance capabilities with TM 500 compactness and portability. The 50 MHz PG 508 Pulse Generator features independent rise and fall controls, external control of output voltage and selectable 1 MΩ-50 Ω trigger/gate input impedance. The 40 MHz FG 504 Function Generator generates three basic waveforms plus a wide range of shaping with variable rise/fall and symmetry controls.

The PG 508 and FG 504 are fully compatible with five versions of our TM 500 Mainframes and over 40 TM 500 Plug-ins. The TM 500 Family of Instruments includes a wide range of counters, multimeters, generators, power supplies, amplifiers, logic analyzers, and oscilloscopes. Plug-ins can be configured to suit the performance needs of your measurement.

TM 500 Designed for Configurability.

For more information and your copy of an educational comparison of pulse and function generators, please circle the reader service number below or write to: Tektronix, Inc., P.O. Box 500, Beaverton, Oregon 97077. (503) 644-0161, Ext. 1505.

In Europe: Tektronix Limited, P.O. Box 36, St. Peter Port, Guernsey, Channel Islands.

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analytic equipment and instrumentation, says Copeland. This includes automotive, medical, and scientific applications. The APP-20 alphanumeric thermal printer is priced at $695 in single quantities, and deliveries should begin in November, the company says.

Datel Systems Inc., 1020 Turnpike St., Canton, Mass., 02021. Phone Ron Petrelli at (617) 828-8000 [364]

Unit generates digital data

Because checking out complex digital circuitry from the simplest chip to the most complex board needs precise test signals, it follows that the best instrument for generating and timing such signals is the one that can operate at the largest number of different levels. Aiming for this goal is a new microprocessor-controlled data and timing generator, "a tool that has been developed to fill several gaps in the digital circuitry test and checkout field," declares Stanley Kubota, marketing manager at Interface Technology.

More specifically, the model RST-432 is designed as a subsystem component for large automatic test systems, but "the inherent versatility of the programmable microprocessor-data-generator approach suits it for a broad range of applications," Kubota notes. These include general-purpose signal generation, memory and microprocessor testing, hybrid integrated-circuit and printed-circuit-board checkout, and as an add-on to high-speed computer-driven automatic testing systems.

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10 μV	1000V **TRMS ac**
10n A	2A **TRMS ac**

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Keithley Instruments, Inc., 28775 Aurora Road, Cleveland, Ohio 44139, (216) 248-0400. Heiglhofstrasse 5, D-8000 München 70, West Germany, (089) 7144065. *In Ohio: (216) 248-0400.

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Circle 195 on reader service card

inputs that are both known and fixed, device response can be predicted and verified with great precision," he says. Signals can be generated at dynamic data rates of up to 10 MHz.

What gives the RST-432 its functional flexibility is the range of choice a user has in supplying the appropriate data patterns for a specific test. The user creates the processor program that controls a set of input/output signals and data patterns selected according to the testing level. Programs can either be loaded manually through the unit's front-panel controls or automatically under external computer control via an IEEE 488-1975 interface bus. Test results can be monitored visually or by computer.

Key to its use as a component of larger systems, Kubota emphasizes, is the model RST-432's microprocessor section. Not only does it provide high-speed control of the entire word-generation section, but it also generates the handshake control and timing signals needed by the device being tested. A self-contained memory is capable of storing up to 256 instructions programmed by the user, with processor language consisting of a set of 16 instructions, each requiring 200 ns for execution. Each instruction controls the microprocessor or the word generator.

The IEEE-488 interface is, in Kubota's words, "a full listen/talk feature that allows the master controller computer to load and read back any of the internal RST-432 memories." A record-memory module lets the unit operate as a logic recorder. With it, 256 or (optionally) 1,024 32-bit words may be recorded, any of which can be recalled and analyzed by the master controller.

In the unit's special clock section, 16 signals may be generated. While interrelated, these signals are asynchronous to the microprocessor and word generator clocks. Timing intervals themselves can range from 100 ns to 8.192 s, in increments of 50 ns.

Other specifications include output patterns to 64 bits by 1,024 words as well as input and record data patterns to 32 bits by 1,024 words. Both input and output lines are compatible with transistor-transistor logic. The speed of the internal word generator clock can be set from 0.975 Hz to 10 MHz. If an

Model 1262 accurately reads wide variety of DACs for linearity, montonicity. Price: $2960.

DAC linearity deserves a credible test.

Now — perhaps for the first time — you can cost-justify 100 percent inspection and testing of incoming D/A converters. ESI's new Model 1262 DAC tester is a ratio instrument that accurately checks linearity and

monotonicity. Under microprocessor control the 1262 readily supports:

...different input codes (BCD, inverted BCD, and several binary codes);

...different number of input bits (up to 12) and,

...different analog outputs (voltage or current) in either polarity.

And it handles both DACs which require full time data or those for which data must be latched through strobing signals (microprocessor compatible).

Test results are presented in 2 seconds plus selected warmup time via front panel LEDs showing absolute and differential linearity as fractions of one least significant bit, and any evidence of nonmonotonic behavior. Test fixture LEDs signal PASS, FAIL, and the presence of excessive superposition (bit addition) error.

Test fixtures the key

The instrument achieves its flexibility through a number of personalized test fixtures. You can be testing BCD current DACs one moment, and binary voltage DACs the next, simply by changing test fixtures according to the pin configuration of

the test fixture. Each contains a zero insertion force test socket, the analog circuitry to process the output signal of the device under test, and switches and jumper wires on the fixture's PCB, used to select code formats, pretest warmup time, and the pass/fail specifications for the DAC type to be tested.

The user makes no adjustments within the instrument.

For complete information, call or write, Electro Scientific Industries, 13900 N.W. Science Park Drive, Portland, Oregon 97229, phone (503) 641-4141.

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Circle 197 on reader service card

external clock is used, it may run as fast as 14 MHz. The complete unit, with 256-word record memory, is priced at $19,995 and has a delivery time of five weeks.

Interface Technology, 852 Cummings Rd., Covina, Calif. 91724. Phone (213) 966-1718 [348]

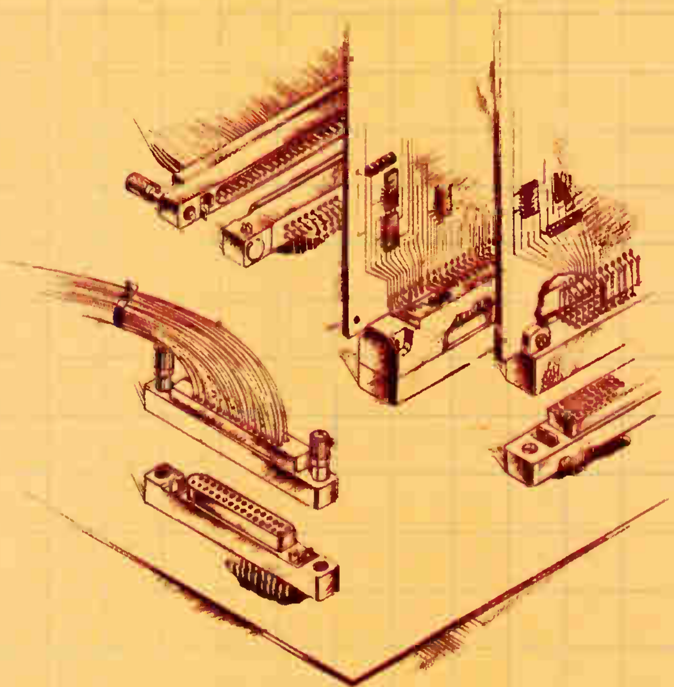
Small display speeds design

Designers of instruments or systems for mobile or aircraft applications now have a choice of designing their own display or dropping in a small, self-contained, intelligent alphanumeric display module. The 7-by-3-by-5-in. DE/320 is slated to be the first in a series of small display modules from Digital Electronics Corp.

The 20-character display module comes complete with built-in refresh, drive, and interface circuitry. An Intel 8041 (a microprocessor with resident read-only memory) manages character generation, display buffering, and refresh logic for this bus-oriented product. Instead of a large, single printed-circuit board containing all 20 chips and the display, the DE/300 series uses a smaller, multiple pc board arrangement so that it can be packaged in a more compact enclosure, explains Robert L. Christensen, the company's marketing manager.

Characters are formed on low-power, vacuum-fluorescent, dot-matrix displays and can be viewed from distances of up to 10 feet, Christensen says. He believes the display module will appeal to engineers who, in designing systems for

PCB Flexibility with Bendix Brush Connectors.



A low mating force connector with up to 400 contacts. 4 body styles. 3 contact variations with options. Superior electrical characteristics and long mechanical life. That's flexibility! And Bendix has one for your high-contact needs. The Brush Connector. Here's what you get.

Bendix Brush Connectors increase circuit count per board.

- Reduce number of boards by allowing more circuits per board.
- Greater board effectiveness by providing exact circuit counts up to 400 contacts in only one connector!

Bendix Brush Connectors reduce mating force 70% to 90%.

- Less complex board supports.
- Secondary actuators eliminated.
- Extended mechanical life. Up to 20,000 mates/unmates.
- Fewer damaged boards.
- Eliminates fixture mounting need of multiple smaller connectors.

Bendix Brush Connectors—a broad product line.

- Mother Board, Daughter Board, Input/Output, PC receptacle body styles.
- 2, 3 and 4 row configurations.
- 90° and straight PC, solderless wrap, crimp removable terminations with multiple lengths and plating options.

Bendix Brush contacts improve electrical characteristics.

- Highly redundant contact sites with multiple electrical paths and wiping action.
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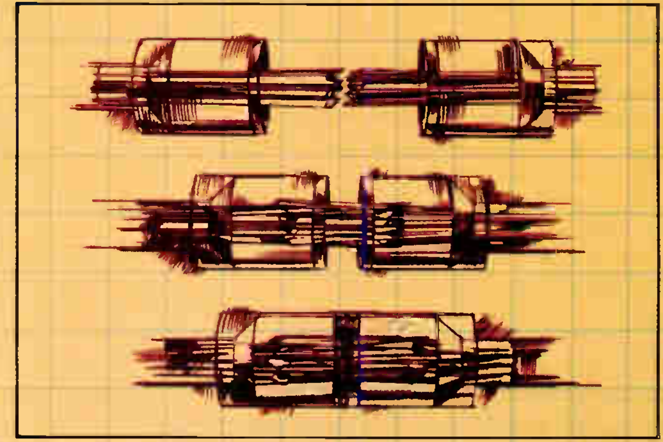

For full information, call (607) 563-5302, or write The Bendix Corporation, Electrical Components Division, Sidney, New York 13838.

Bendix

We speak connectors.

vehicles or aircraft, require clear, brightly displayed information or to those who need low-power readouts for portable instrument designs.

The cool green vacuum-fluorescent display, which is widely used in desk-top calculators, is generally believed to be easier on the eyes than are the red light-emitting diodes usually found in today's digital electronic equipment.

The DE/320 costs $350 in single quantities and includes enclosure and power supply. The module requires only a 5-V dc power input at less than 700 mA full load and can interface with any of the 8-bit parallel data busses of the popular metal-oxide-semiconductor microprocessors. "We've successfully interfaced it with Z80s, 8080s, 6800s, and the like," Roger W. Doering, division vice president adds.

The parallel interface scheme uses the 8-bit data bus signals in ASCII format, and controls are implemented via low-order address, chip-select, and read/write active-low inputs. Also, a 1,200-baud serial interface is supplied which requires transistor-transistor-logic level input signals formatted, for example, as for a standard ASCII printer.

Production quantity deliveries will begin by mid-October, according to Christensen, and there are discounts for large-volume, original-equipment-manufacturer orders, he says.

Digital Electronics Corp., 415 Peterson St., Oakland, Calif. 94601. Phone (415) 532-2920 [349]

Test unit works at a fast clip

Up to now, computer-controlled automatic test equipment for checking out logic circuitry on printed-circuit boards has, for the most part, been able to isolate faults down to the component level only in the case of static components. Existing probes have had problems performing fault isolation on the newer microprocessors and memories, which are both too sensitive and too fast for them to handle.

To update its line of Capable testers, Computer Automation Inc.'s Industrial

Boschert low-power switchers win OEMs' stamp of approval. Here's why.

Low cost. Only Boschert is delivering switching power supplies that are cost-competitive with linears in the 25 to 400 watt range. That's because Boschert is focusing exclusively on the design and production of low-power switchers. Our modular design techniques are lowering prices while maintaining quality and reliability.

Small, light and efficient. Boschert power supplies are perfect for microprocessor-based systems and other digital equipment because they're five times smaller than comparable linear supplies, and nine times lighter. Because little power is wasted as heat, they require no fans — only convection cooling. And Boschert switchers are well-suited for high pulse-load environments such as printers: when additional power is required, it is available instantaneously — at any output.

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For information, contact a Boschert representative. Or write Boschert Incorporated, 384 Santa Trinita Ave., Sunnyvale, CA 94086. Phone (408) 732-2440. TWX 910-339-9241. The finest microprocessor-based systems are powered by Boschert. What about yours?

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Circle 201 on reader service card

New products

Products division is bringing out a new high-speed probe-type clip that lets the testers check dynamic logic parts at functional speeds. The clip, to be demonstrated for the first time at Wescon, has real-time capability for exercising the devices with pulses down to 25 ns and at speeds up to 40 MHz. When hooked up to a Capable system running with guided fault-isolation software, the new clip will accommodate most of the dynamic devices now on the market, according to the company.

The clip itself is an assembly with cabling and connectors that a system operator attaches to an individual circuit when the system's test sequence signals a fault. Comparing the performance of the unit under test against a stored fault-signature file in memory, the system minicomputer, in effect, helps the operator determine where the fault is most likely to be located by means of step-by-step instructions displayed on a cathode-ray-tube terminal. Faults generally are identified immediately, the company says, or within one or two trys after test interruption.

A major improvement designed into the high-speed clip over earlier probes is a buffer circuit in the input end of the cable that connects the clip to the data management section. This circuit is essentially a bidirectional isolation amplifier that keeps the test sequences from influencing sensitive devices during real-time operation. The clip also has a fail-safe feature that alerts the operator of the Capable system to improper placement on the circuit or

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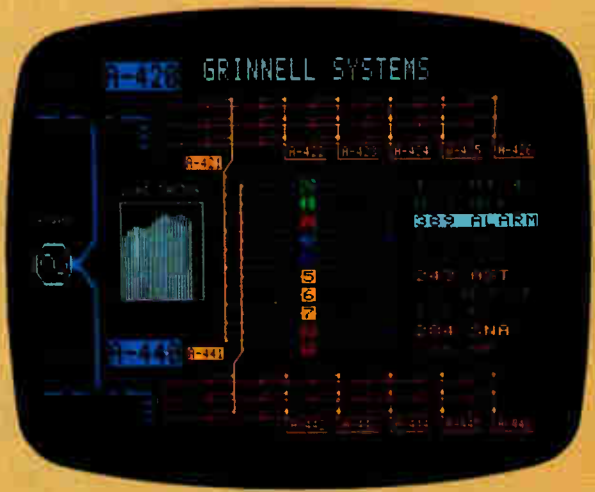

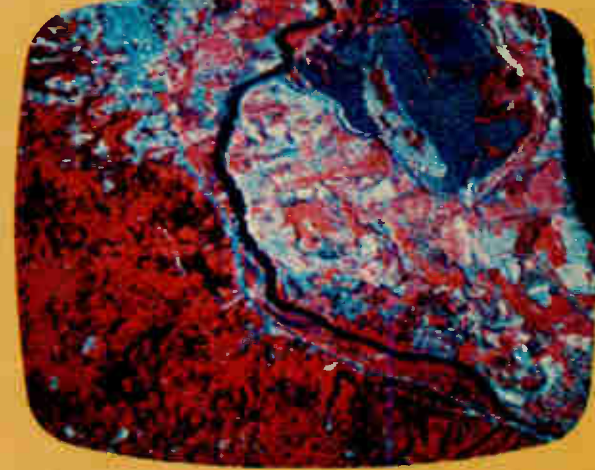

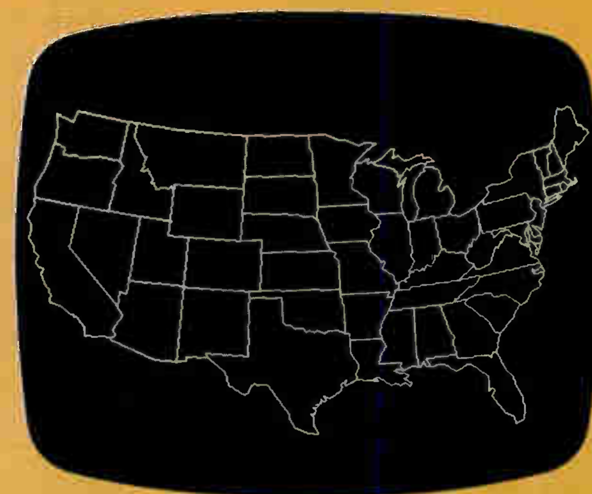

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Grinnell displays are already at work in tomography, ERTS imaging, process control, data plotting and many more applications.

So, before you decide on a display system, talk to our experts. Complete operating systems start at $5,450, and quantity discounts are available. For detailed specs and/or a quotation, call or write.

GRINNELL SYSTEMS

2986 Scott Boulevard, Santa Clara, California 95050 (408) 988-2100

Circle 203 on reader service card

errors in placement sequence.

For users of Capable systems with real-time capability, Computer Automation is offering the standard 16-pin clips as an updated feature at no extra charge. A 24-pin version is available as a $975 option. For users who do not have real-time systems, the 16-pin clip is $875. In this case, it would be of value in conducting static tests on low-power Schottky devices, which are susceptible to crosstalk. Narrow pulses in the 40-ns range are required. Delivery takes 30 to 50 days.

Computer Automation, Industrial Products Division, 2181 Dupont Dr., Irvine, Calif. 92713 [361]

System gives 8086 support

Adding to the illustrious line of 8-bit microprocessors that it already supports—the 6802, 6800, Z-80, 8080, and 8085—the Microsystem microprocessor development system is the first to support the 16-bit 8086 microprocessor. Software-compatible with both the 8080 and 8085 systems, the 8086 development systems deliver up to 10 times the processing power of those systems at a rate of 5 MHz.

A full range of disk-based 8086 systems are offered to allow the designer to select the level of performance he requires. Each includes microprocessor central processing unit with up to 256 kilobytes of memory, high-speed 960-character cathode-ray-tube display, ASCII keyboard, dual floppy-disk unit, and operating system software.

Optional accessories for the system include software logic analyzers, in-circuit emulators, line printers, Basic compilers, and a disk operating system with relocatable macro-assembler and linkage editor. Low-cost plug-in modules to convert the system for use with

With 32 kilobytes of memory and double-density 8-in. dual floppy-disk unit, the system is priced at $9,625. Delivery of the Microsystem/32 Mod 8086 is 120 days after receipt of order.

Futuredata Computer Corp., 11205 S. La Cienega Blvd., Los Angeles, Calif. 90045. Phone R. Schaaf at (213) 641-7700 [365]

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*Price for AC line version. AC/battery version available for $40 additional cost.

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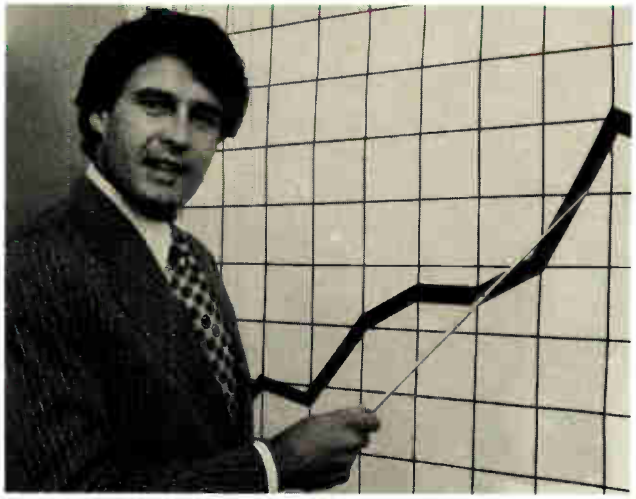

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Harris introduces a complete new line of Op Amps in 8 lead epoxy DIP packages...at low, low 100-up prices starting at an unbelievable $1.78 each. You could pay two or three times as much elsewhere and still not get the performance features you get with Harris. The new line is the epoxy version of our highly successful family of HA-25XX and 26XX amplifiers. The charts that follow tell the whole story.

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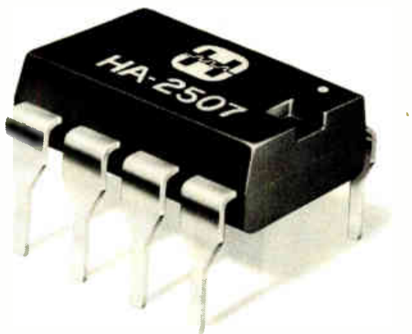

With operating temperatures from 0°C to +75°C, the new Harris op amps cover a wide range of industrial and commercial applications including: Laboratory-grade test equipment. Automatic electronic test systems. Medical patient monitoring systems. CRT displays. Process control systems...and many more.

Harris epoxy op amps provide the highest level of ac performance that is commercially available in a monolithic form. They give the designer a new degree of freedom without cost concern; give the customer a new measure of economy without forfeiting performance. And that should satisfy both you and your boss. Get the happy story today by calling the Harris Hot Line, or write: **Harris Semiconductor Products Division, Box 883, Melbourne, Florida 32901.**

HIGH SLEW RATE

	PRECISION				COMPENSATED				UNCOMPENSATED				
	−55 to 125°C	−55 to 125°C	0 to 70°C	EPOXY 0 to 75°C	−55 to 125°C	−55 to 125°C	0 to 70°C	EPOXY 0 to 75°C	−55 to 125°C	−55 to 125°C	0 to 70°C	EPOXY 0 to 75°C	
PARAMETER*	HA-2500	HA-2502	HA-2505	HA-2507	HA-2510	HA-2512	HA-2515	HA-2517	HA-2520	HA-2522	HA-2525	HA-2527	UNITS
OFFSET VOLTAGE	2	4	4	5	4	5	5	5	4	5	5	5	mV
BIAS CURRENT	100	125	125	125	100	125	125	125	100	125	125	125	nA
VOLTAGE GAIN	30K	25K	25K	25K	15K	15K	15K	15K	15K	15K	15K	15K	V/V
UNITY GAIN BANDWIDTH	12	12	12	12	12	12	12	12	20	20	20	20	MH
SLEW RATE	±30	±30	±30	±30	±65	±60	±60	±60	±120	±120	±120	±120	V/μs
RISE TIME	25	25	25	25	25	25	25	25	25	25	25	25	ns
	APPLICATIONS DATA ACQUISITION SYSTEMS SIGNAL GENERATORS				APPLICATIONS R.F. AMPLIFIERS PULSE AMPLIFIERS				APPLICATIONS VIDEO AMPLIFIERS SIGNAL CONDITIONING				

*VALUES GIVEN ARE TYPICAL AT 25°C

WIDE BAND WIDTH

	COMPENSATED				UNCOMPENSATED				
	−55 to +125°C	−55 to +125°C	0 to 75°C	EPOXY 0 to 75°C	−55 to 125°C	−55 to +125°C	0 to 70°C	EPOXY 0 to 75°C	
PARAMETER*	HA-2600	HA-2602	HA-2605	HA-2607	HA-2620	HA-2622	HA-2625	HA-2627	UNITS
OFFSET VALVE	0.5	3	3	4	0.5	3	3	4	mV
BIAS CURRENT	1	15	5	5	1	5	5	5	nA
VOLTAGE GAIN	150k	150k	150k	150k	150k	150k	150k	150k	V/V
UNITY GAIN BANDWIDTH	12	12	12	12	100	100	100	100	MHz
SLEW RATE	±7	±7	±7	±7	±35	±35	±35	±35	V/μs
RISE TIME	30	30	30	30	17	17	17	17	ns
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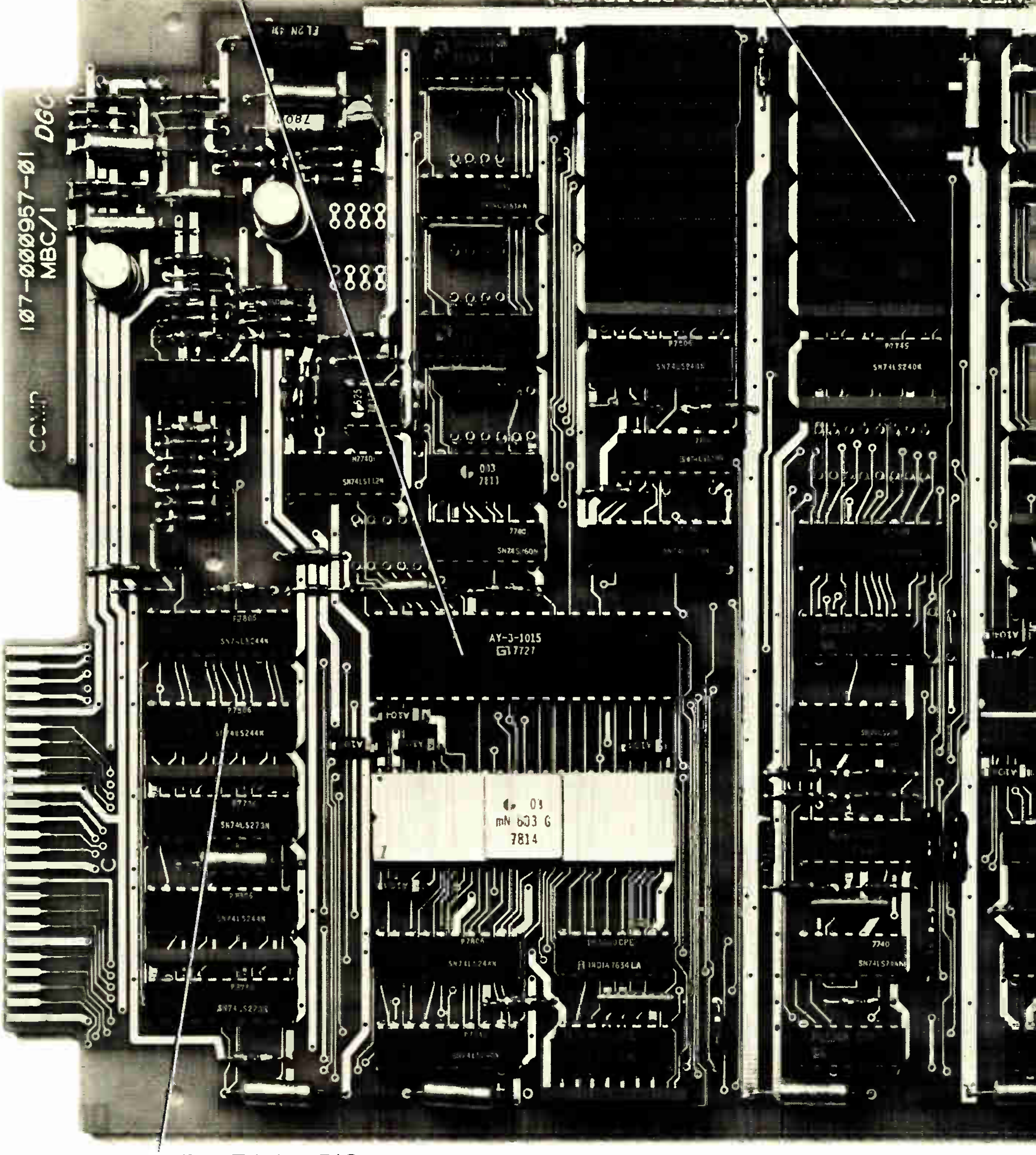

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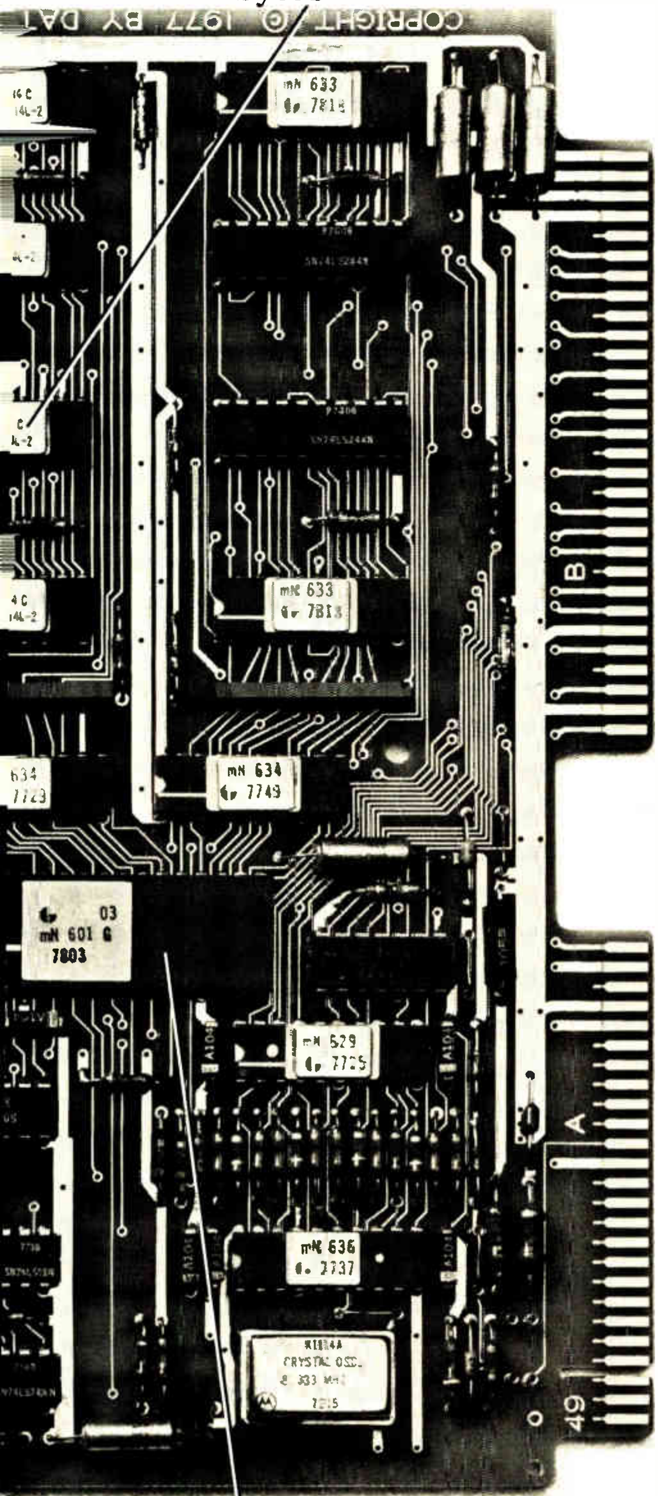

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Model 154-4 Automatic Pulse Generator
Model 7115 DVM with microprocessor control
Model DPSD-50 Dual 50 W Power Supply

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Circle 210 for literature
Circle 211 for demonstration

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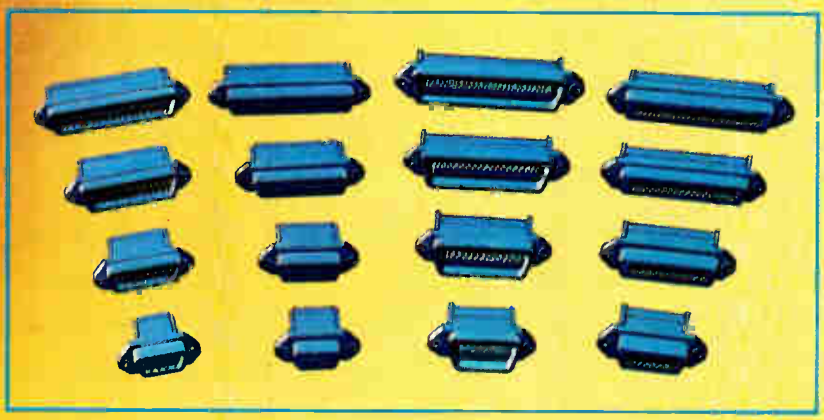

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Circle 212 on reader service card

LSI testers operate at 20 MHz

Full-blown unit for device characterization and medium-cost system for incoming inspection allow true time-sharing operation

by Al Shackil, Instrumentation Editor

Offering a full range of test options for large-scale integrated circuits are Tektronix' new S-3270 and S-3250 systems. The S-3270 (right in photo) provides state-of-the-art tester performance for device characterization required by LSI vendors and design engineers. The S-3250 (left) does production testing and incoming inspection.

Both testers feature 20-MHz operation, enabling devices with clocks of 10 MHz to be tested at full speed. The testers provide input signals, compare device outputs with expected values, generate functional test patterns, and perform dynamic error storage at the 20-MHz rate. A seven-phase clock is provided, with up to 14 phases available.

The systems' driver format choices include return to zero, nonreturn to zero, return to one, and return to complement. This means hardware restrictions can be overcome by proper driver formatting. Fast input/output bus testing is also possible with special return-to-inhibit driver formatting.

A dual-memory architecture is achievable by adding, for each tester pin, the optional 4-K random-access memory to each pin's standard 4-K shift-register local memory. This enables running of large, complex test patterns without test interruption to reload local memory. A high degree of test-pattern compression is also possible, which allows common test subroutines to be stored. It is necessary to define only their arguments for each test.

True foreground/background time-sharing operation is provided by the Tektest III operating software in both systems. This enables testing to continue without interruption in the foreground, while up to four users on the system program, edit, or reduce data in the background.

The two test systems can test LSI, RAMs, read-only memories, microprocessors, analog and digital hybrids, peripheral interface circuits and essentially all non-LSI devices. A fully integrated waveform digitizer performs linear and analog tests on the same device. Up to 64 pin-control cards, each with input and output capability, allow testing of a device with up to 128 pins. Complex test patterns can easily be generated with the aid of a pattern RAM with looping and subroutine capability, and a memory pattern generator providing a fast source of algorithmic patterns.

The major differences between the S-3270 and the S-3250 are related to the system architecture, which affects cost and performance. The S-3250 uses a DEC PDP-11/34 with cache memory and floating-point hardware as the controller. This provides the high-speed background data processing needed for device characterization. A disk operating system and Tektronix 4010 graphics terminal are also included.

The S-3250 production tester employs a lower-cost version of the DEC PDP-11/34 as its controller and the less expensive, lower-resolution, Tektronix 4006 terminal. The number of power supplies for pin-control cards is also reduced to a level consistent with the number of pins necessary for the device under test.

The price for the basic S-3250 production tester starts at $180,000 and the S-3270 device characterization system in its basic configuration is priced at approximately $250,000. Delivery time is 12 to 16 weeks.

Tektronix Inc., P. O. Box 500, Beaverton, Ore. 97077 [338]

Introducing the HP 1000 model 45.

A powerful number cruncher that won't break your budget.

Most engineers and scientists will find all the power they need in this new leader of the HP 1000 family. A new floating point processor handles big data arrays and cuts lengthy computational problems down to size. And the HP 1000 Model 45 also has the flexibility for complex measurement and control applications, for data base management and distributed networking.

And it isn't hard to get your hands on all this computational power. System prices start at just $46,500.*

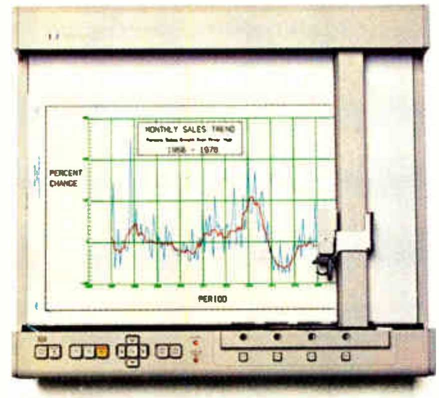
Our new F-Series processor is the hard-working heart of the system. It's extremely fast, completing load and store operations in 900 nanoseconds. The separate hardware processor does floating point calculations at high speeds, too—630 ns for add, 1.8 microseconds for multiply and 3 microseconds for divide.

A special scientific instruction set, standard in the system, also helps to improve execution speed, performing trig and log functions in less than 48 microseconds. And a fast FORTRAN processor, which handles commonly used FORTRAN operations in hardware, also gets things done in a hurry.

Our RTE-IV real-time operating system, the latest in an upward compatible family, lets you manipulate data arrays up to 1.8M bytes, using simple FORTRAN commands. As many as 64 partitions, with a program capacity of 54K bytes, can be resident in memory at the same time.

The HP 1000 Model 45 comes with a fast (25 msec seek time) 20M byte disc drive and an HP 2648A Graphics Terminal, as well as our new Graphics/1000 support software to help you write graphics programs. You can also team it up with other HP products like the HP 9872A four-color plotter and the HP 7245A printer/plotter.

Adding data base management is as simple and economical as adding peripherals. Our IMAGE/1000 software will consolidate your technical information into related and easily accessible files. And you can pool data from other HP 1000 systems (as well as linking to our powerful HP 3000 general purpose computers and IBM) with the help of DS/1000 networking software.



In addition to getting graphic displays on the 2648A terminal, you can get hard copy graphics on our new 9872A programmable four-color plotter, one of many options available with the HP 1000 Model 45. It has a built-in microprocessor and operates up to 360 mm/s (14 inches/s) on each axis. Ideal for vector analysis trace differentiations and window plotting.

So if you've got some big jobs to do, but don't have a big budget to match, the HP 1000 Model 45 can solve your problems fast. To find out all about it, call the HP office listed in the White Pages. Or send us the coupo . We'll prove once again that good things do come in small packages.

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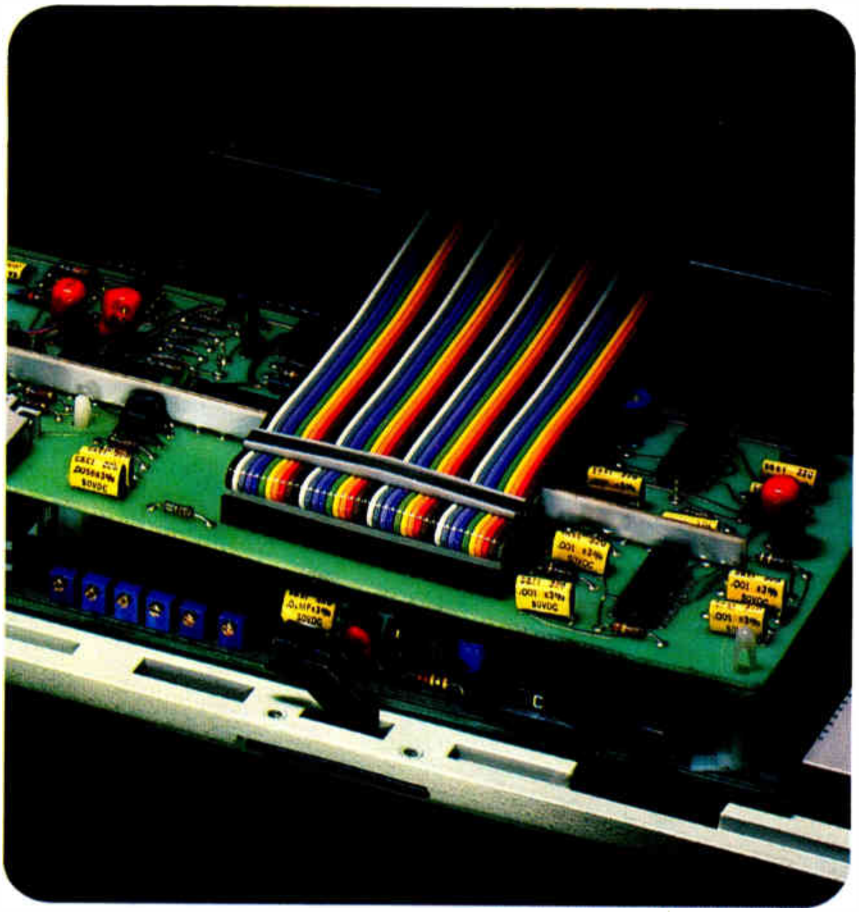

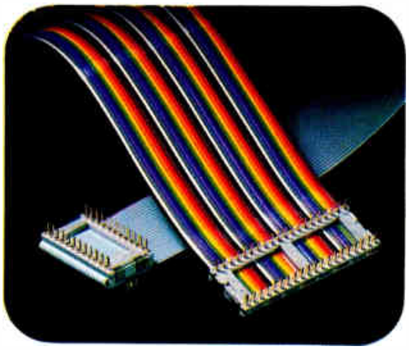

Need some more ways to simplify wiring and increase circuit density? 3M's Scotchflex line offers you the widest choice of mass terminating cable, connectors and system components to accommodate your design packages. Plus proven reliability. Off-the-shelf availability. And the unmatched experience of the people who pioneered the concept of electronic mass termination.

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Both connectors have .100″ x .600″ grid spacing and are available with either rectangular legs for use with standard I.C. sockets or round legs for use with high density packaging panels. They may be used with Scotchflex shielded, non-shielded or color-coded flat cable or with twisted pair or parallel lay woven cable.

Where frequent plugging and unplugging is necessary, strain relief bars and pull tabs are available for all Scotchflex D.I.P. connectors including 14 and 16-pin sizes.

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One-chip computer has serial I/O port

Latest member of 3870 family is aimed at distributed-processing applications, has controller to reduce communications burden on CPU

by Raymond P. Capece, Solid State Editor

Mostek Corp's next addition to the 3870 single-chip microprocessor family could turn out to be the new favorite, as it has all the features of the 3870 and one major addition, a serial input/output port. The 3873, which will be available in sample quantities next month, can play a role in distributed-processing applications, since it has the capability for serial data communication without tying up its central processing unit.

The port is a simple universal asynchronous receiver/transmitter that greatly enhances the microcomputer's appeal. Like the 3870, the 3873 has central-processing, oscillator, and clock circuits, 2,048 bytes of read-only memory for program storage, 64 bytes of scratch-pad random-access memory, and a general-purpose timer. But the 3873 sacrifices three of the 3870's 32 I/O lines for the serial port, which requires two pins for the serial data and a third as a shift-clock line. In addition, the 3873 adds two vectored interrupts and a timer for setting the serial data rate.

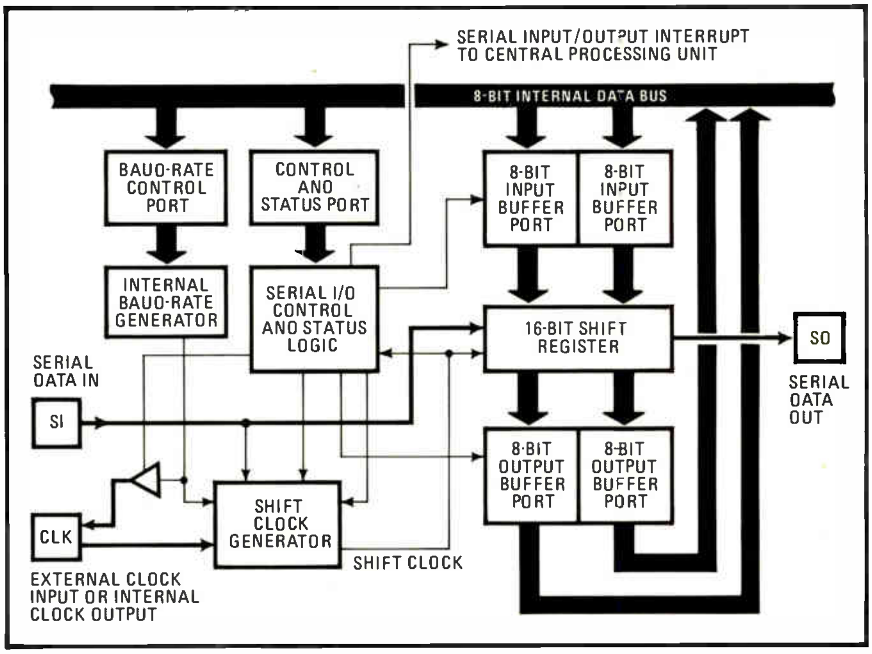
The serial port will be a must in future applications of one-chip microcomputers in distributed processing arrangements that lean towards "loosely coupled" networks. (The term refers to serial communication between processors, as opposed to tightly coupled, parallel, bus-sharing arrangements.)

Mostek is developing an ambitious network approach for remotely located equipment that will use a preprogrammed 3870 dedicated as the front-end receiver/transmitter at each location. Such a setup would have a 3873 as the host processor polling and commanding its peripheral devices. "Since the port is a simple UART, it doesn't, for example, do parity checking," says Harold Dozier, manager of microcomputer design at Mostek, "but that could be done in software." He adds, however, that the 3873 is capable of full-duplex synchronous communication which is much simpler since the data is always clocked in at known times.

The port itself has a maximum data rate of 9,600 bits per second. Although it is double-buffered for both receiving and transmitting data, it contains only one transfer register and therefore is not capable of full-duplex asynchronous two-way communication. According to Bob Schweitzer, microcomputer marketing manager at Mostek, that inadequacy does not bother the Carrollton, Texas, company, however. "Most systems are designed to operate in one direction," he explains.

Since it uses a single twisted pair of wires, a serial port may seem simple enough to be handled by the CPU with a small routine. It is simple, but for the processor, it is especially time-consuming. "Doing the UART in software can tie up the CPU entirely over just one pin," explains Dozier. He goes on to say that when receiving data, for example, the CPU has to watch and wait as the bit data words are loaded into a register one bit at a time. "Now, a serial I/O block is doing the watching till an entire byte is shifted into the register," he says. "The CPU is only interrupted when the register is full." The extra port requires no additional instructions.

Mostek Corp., 1215 West Crosby Rd., Carrollton, Texas. Phone (214) 242-0444 [339]



Instruments

Modulation unit measures all

Analyzer determines power, frequency, and modulation from 150 kHz to 1.3 GHz

Despite its deceptively simple front panel and the ease with which an operator can learn to use it, the 8901A modulation analyzer is one of the most complex, powerful instruments to come to market. It shows promise of becoming the standard for rf signal measurement.

Basically, the analyzer completely characterizes signals in the 150-kHz-to-1,300-MHz range. It measures frequency with a resolution of 10 Hz below and 100 Hz above 1,000 MHz. It measures peak envelope power in the range from 1 mW to 1 W with an accuracy within ±2 dB. It measures frequency modulation with an accuracy within ±1% of reading ±1 digit for rates between 30 Hz and 150 kHz; amplitude modulation within ±1% ±1 digit between 30 Hz and 50 kHz and depths greater than 5%; phase modulation within ±3% ±1 digit between 200 Hz and 20 kHz. And that is just the beginning of the analyzer's capabilities.

Microprocessor-based, the 8901A offers all major functions at the stroke of a single key without manual tuning or range selection. It automatically tunes to the input signal, adjusts for proper signal level, selects the appropriate measurement range, makes the measurement, and displays the result.

In the manual mode, the analyzer allows users to designate the frequency to which it is tuned. When more than one signal is present, entering the desired frequency via a front-panel keyboard causes an intermediate-frequency filter to eliminate all but extremely close signals. Thus, the unit can count signals other than the largest.

With a ratio key, users can also make measurements relative to either a measured value or a keyboard-entered one, and that measurement can be expressed in either percent or decibels, an extremely useful feature when testing for hum and noise in fm mobile transmitters and for fm broadcast applications.

The operator can also initiate various special functions using the coding given on a pull-out information card under the front panel. For example, by entering 4.1 and depressing the "special" key, the user can make the analyzer track a given input signal as it changes frequency, so that he can continuously measure the modulation accuracy of a signal generator while tuning across its entire frequency band.

High-pass and low-pass filter selectability; IEEE-488 (HP-IB) programmability; pre- or post-detection fm deemphasis capability; positive-peak, negative-peak, and average detection—the list of the unit's features is seemingly endless. But with the advantages it offers in mobile communications, avionics, commercial broadcast, and metrology applications, it shouldn't be long before those features are well known to most engineers.

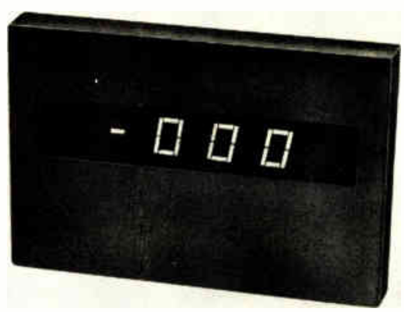
The 8901A is priced at $7,500 and deliveries will begin in November.

Hewlett-Packard Co. Inquiries Manager, 1507 Page Mill Rd., Palo Alto, Calif. 94304 [351]

3½-digit panel meter is a $38 stick-up

There are many advantages to economy of design, not the least of which is price. The F500 series of digital panel meters is a case in point. Each meter consists solely of a 3½-digit, light-emitting-diode display, one integrated circuit, and 16 passive components—so there are very few parts that can fail. And because of the dearth of components, the entire meter fits in a small package, one that measures only 3 by 2 by 0.4 in. All this contributes to the fact that prices for series members begin down at $38 in 100-up quantities.

Installation can be as simple as the instrument itself. The 2-oz DPM is shipped with high-strength (500-lb/in.^{2}), double-sided tape that allows users to attach the meter to the



front or back of any panel they wish. For front-panel use, all that is required is a ¼-in.-diameter hole through which to attach wiring.

One place where economy is fortunately not evident is in the unit's specifications. The meter is accurate and linear to within ±0.05% of the reading ±1 digit. Furthermore, the mass-produced units receive three 100% tests and 150-hour burn-in before they are separated from production-line carriers, and they also get a 100% test before being shipped.

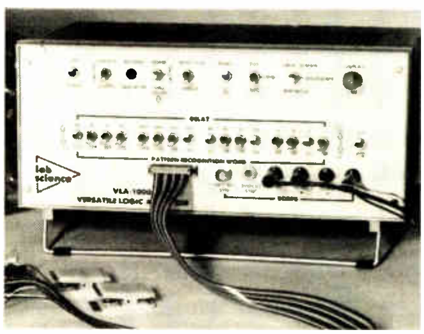
The meters are offered in both single-ended and differential models with full-scale voltage ranges from 50 mV to 500 V or full-scale current ranges from 200 μA, 11 ranges in all. Power requirements are 800 mW at 5 V dc. Delivery time is four weeks.

International Microtronics Corp., 4016 Tennessee St., Tucson, Ariz. 85714. Phone (602) 748-7900 [353]

Logic analyzer offers versatility at low cost

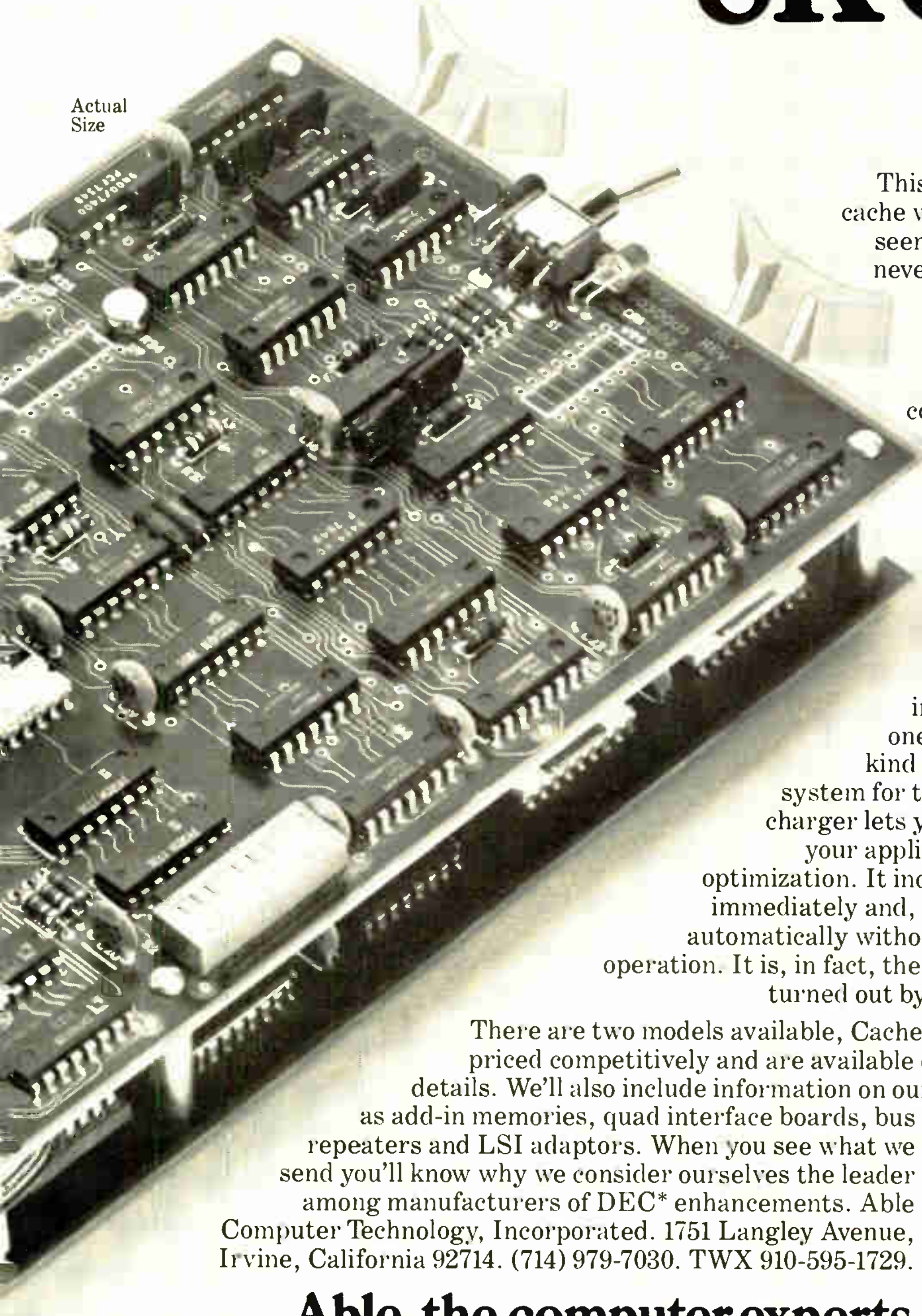
The VLA-1000 logic analyzer provides most of the features of second- and third-generation analyzers for only $575. For that price, the user gets an instrument with four output display modes: data domain, waveshape, map, and dual-byte digital-to-analog. The unit accepts 16-bit parallel input data, has a 16-bit-by-16-word memory, and plugs into any dual-trace oscilloscope provided with external synchronization.

In the data domain mode, the dc-to-10-MHz unit provides a hexadecimally grouped display of 256 1s or 0s; in waveshape mode, 16 traces



The Incredible 8K Cache

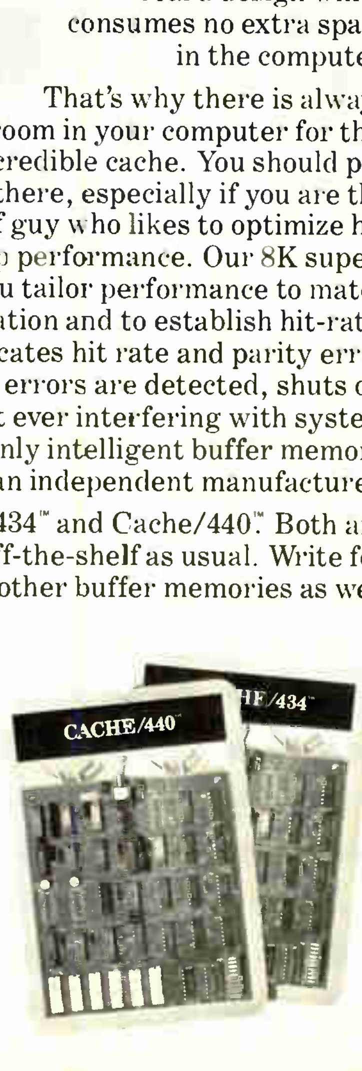
Actual Size



This is the ultimate version, the 8K cache with everything. You have never seen one like it before, and you may never see another. Designed for the 11/34, 11/35 and 11/40, it has byte and address parity, upper/lower limit switches, on-line/off-line manual switch control, activity indicator lights, 8K bytes of memory (4K words) providing a capacity four times that of competitive units and an interconnect board design which consumes no extra space in the computer.

That's why there is always room in your computer for this incredible cache. You should put one there, especially if you are the kind of guy who likes to optimize his system for top performance. Our 8K supercharger lets you tailor performance to match your application and to establish hit-ratio optimization. It indicates hit rate and parity error immediately and, if errors are detected, shuts off automatically without ever interfering with system operation. It is, in fact, the only intelligent buffer memory turned out by an independent manufacturer.

There are two models available, Cache/434™ and Cache/440™. Both are priced competitively and are available off-the-shelf as usual. Write for details. We'll also include information on our other buffer memories as well as add-in memories, quad interface boards, bus repeaters and LSI adaptors. When you see what we send you'll know why we consider ourselves the leader among manufacturers of DEC* enhancements. Able Computer Technology, Incorporated. 1751 Langley Avenue, Irvine, California 92714. (714) 979-7030. TWX 910-595-1729.



Able, the computer experts

*DEC is a registered trademark of Digital Equipment Corporation.

Circle 221 on reader service card

with clock-reference ticks. The map mode offers a display of 16 addresses on a field of 64-K locations, and the dual-byte d-a mode shows the most and least significant bytes resulting from conversion on separate traces. By diverting the display to the side of the screen when recording, no oscilloscope-blanking connection is needed.

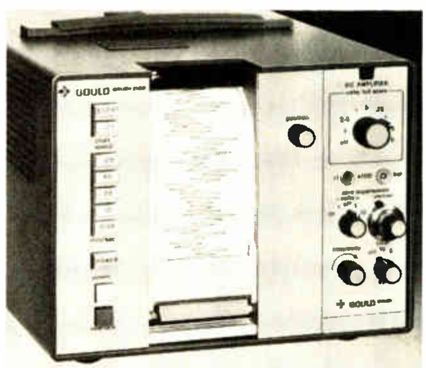
The 16 data-plus-clock input lines are fully buffered and compatible with all standard logic families. Other features include synchronous or asynchronous operation in repetitive or single-shot mode, a 0-to-9,999 event or clock delay, positive-, mid-, or negative-time display, end-for-end data-word inversion through connector reversal, and 10-ms-to-2-s variable display time in the repetitive mode. Future accessories will include cable interfaces for the S-100 and IEEE-488 buses. The instrument is available from stock.

Lab Science, P. O. Box 1972, Boulder, Colo. 80306 [354]

Rugged recorder gives choice of penmanship

The latest addition to the Gould 2000 series of chart recorders is the model 2100, a rugged, portable 22-lb unit that will be on view at Wescon/78. The recorder uses a single 50-mm channel and is fully compatible with the 4600 series of plug-in amplifiers, giving it a wide range of applications in such areas as industrial, scientific, and biomedical measurement.

Users can choose between two



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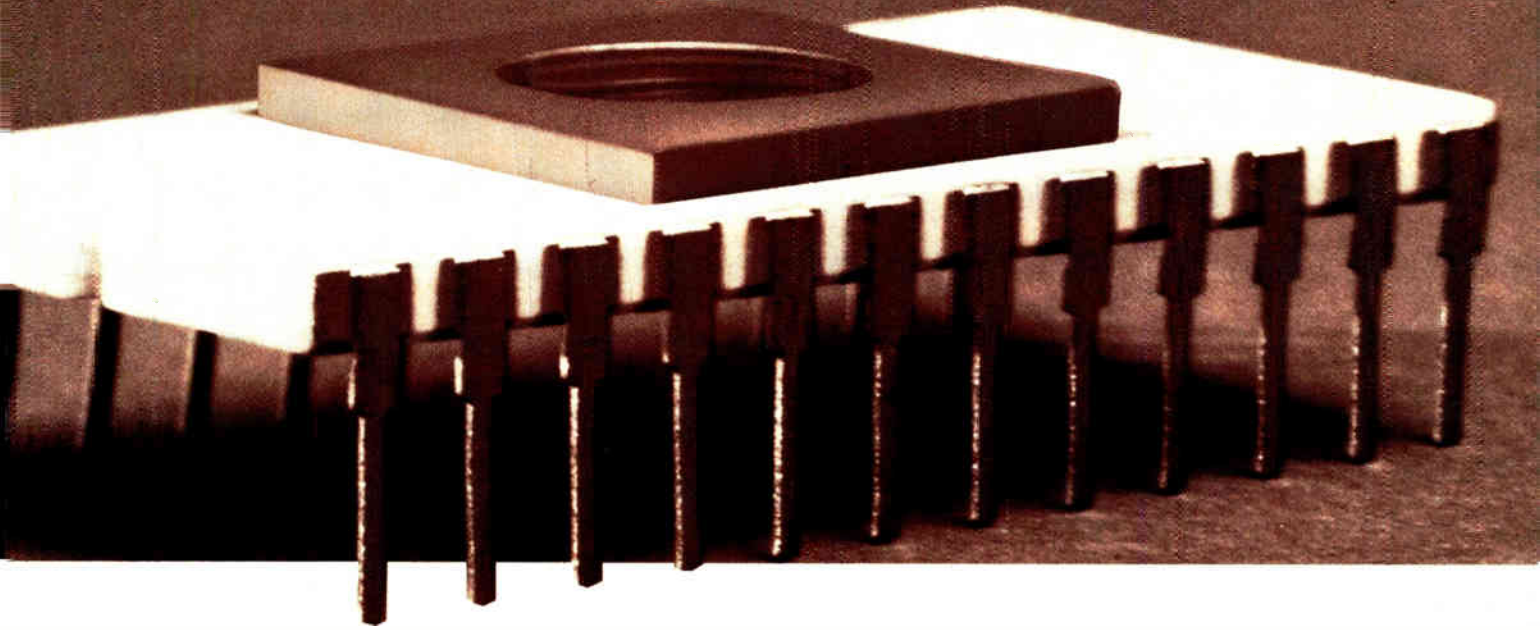

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Circle 223 on reader service card

New products

writing methods: fine-line thermal writing that uses thermal paper which does not smudge from pressure or handling, or pressurized fluid writing. Full-scale frequency response is 30 Hz, rise time is less than 8 ms, and overshooting is under 1% on square waves and transients. Any of eight chart speeds from 0.4 to 125 mm/s can be selected from the recorder's front panel.

The new recorder is the lowest priced in the 2000 series, costing just $1,495.

Gould Inc., Instruments Division, Marketing Services, 3631 Perkins Ave., Cleveland, Ohio 44144. Phone (216) 361-3315 [355]

Chip-based units count frequency up to 3 GHz

Based on an integrated-circuit chip that is itself almost an entire counter, the five 9910 series frequency counters are aimed at the needs of the communications industry.

At the low end of the line, in terms of both price ($395) and frequency (200 MHz) is the model 9913, an eight-digit benchtop counter with a sensitivity of 10 mV. One step up is the model 9915, which, for $650, offers the same sensitivity in a nine-digit, 520-MHz counter that can provide up to 15 hours of battery operation. Like the other ultrahigh-frequency members of the series, the 9915 has a specially designed uhf input that provides protection against signals that exceed 25 W.

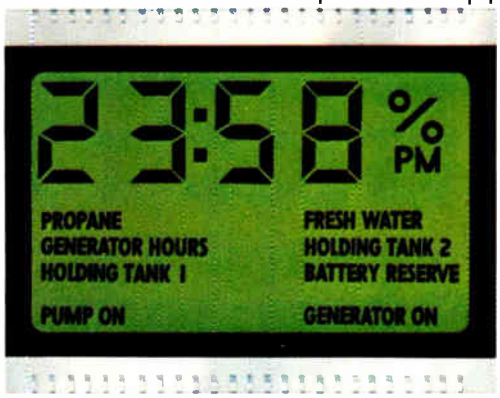
The model 9917 is a direct-gated, 560-MHz unit priced at $895 that includes a low-frequency multiplier to enable direct frequency measurements down to 10 Hz with resolutions of 0.01 Hz. The multiplier is optional for the four other models.

The 1.1-GHz 9919 and the 3-GHz 9921 are programmable and have IEEE-488 interfaces; they are priced at $1,095 and $1,995, respectively. Like the 9915, the 9919 is capable of battery operation. All units offer oscillator stability of 1 ppm/month, and higher stability options.

Racal-Dana Instruments Inc., 18912 Von Karman Ave., Irvine, Calif. 92714. [356]

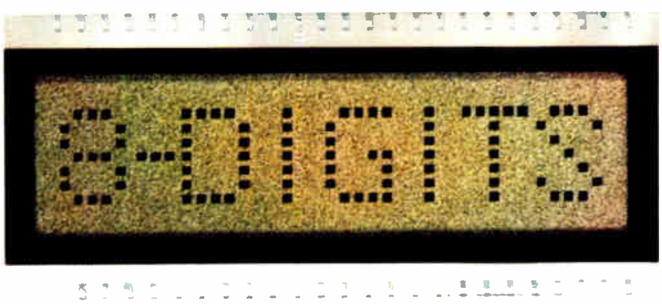
Being First Isn't Easy.

LXD. First with digital liquid crystal watch displays. LXD. First with D.I.L. pins. LXD. First with integral back-lighting. LXD. First with wide-range liquid crystal fluids.



And now LXD is first, again. First with high temperature/high humidity LCDs. First with bar graphs. First with dot matrix LCDs. Yes, being first isn't easy. It's really the combination of skill, expertise, and a pioneering development team that has made LXD Number 1 in LCDs. We'd like to be Number 1 with you, too, by developing and delivering the standard or custom LCDs you need, when you need them.

Applications of LXD LCDs are rapidly



expanding. For example, after exhaustive environmental testing, LXD LCDs are now approved for use in gasoline pumps and dispensing stations. LXD LCDs passed with flying colors!

Give us your toughest LCD application — high heat, high humidity, whatever. No matter how highly specialized your application, LXD will design the LCDs no one else can give you. After all, that's what it takes to be first.

And if you're interested in multiplexing displays, contact us first. LXD is shipping multiplexed LCDs to manufacturers who've designed the multiplexing circuitry for handling this type of display.

Being first takes a lot more than meets the eye. Want to hear more? Contact us.

Visit us at the LXD booth #677 at WESCON, in Los Angeles.

Liquid Xtal Displays INC.
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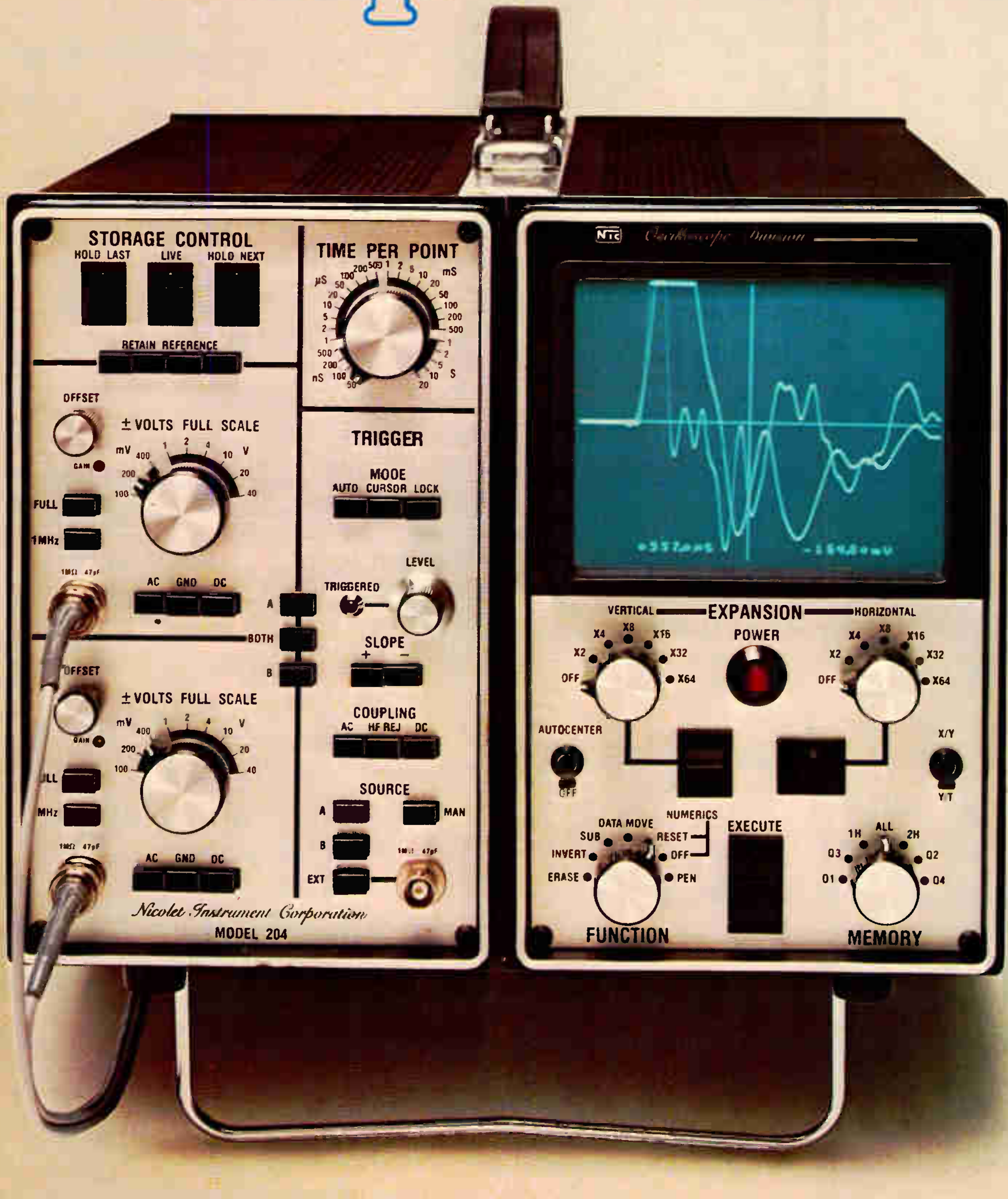
Nicolet's Explorer...



...begins a new oscilloscope era.

This is an oscilloscope that's *many* times more accurate than traditional oscilloscopes, and it has an order of magnitude better resolution. It is a great storage oscilloscope, too, storing literally hundreds of times more information, without adjustments, at the touch of a button, and it doesn't "forget" until you want it to. It can show live waveforms, or stored waveforms, or live waveforms superimposed on stored waveforms. It has x64 display scale expansion which allows you to see fine details. You can see signal changes as small as a hundredth of a percent, while observing superimposed signal waveforms.

EXPLORER has "retroactive sweep trigger" which means you can observe signals that precede your sweep trigger just as easily as you can observe those that follow. Therefore, you can see the causes of an event as easily as the consequences. This is truly a *general purpose oscilloscope*, for signals in the frequency range of millihertz to a few megahertz, and of course, dc. It provides the same functions as general purpose analog oscilloscopes. The improvement is simply that it performs these functions superbly, with less hassle, and under a greater range of conditions.

An optional internal magnetic disk memory, with removable disks, allows you to store waveforms permanently and recall them in seconds for comparison or inspection. It records at the touch of a button, or automatically in sequence if a series of signals is to be stored. Another option is digital I/O, in case you want to analyze the signals by calculator or computer. RS-232 and IEEE 488 busses are available.

EXPLORER has plug-in unit construction so that you can choose one or two channel operation. You can choose fast plug-ins, or plug-ins designed for measurements of very low frequency and high sensitivity.

Nicolet? Who's Nicolet?

If digital oscilloscopes mark the beginning of a new era in oscilloscopes, you might wonder why little, unknown, Nicolet was the one who pioneered them, rather than one of the traditional manufacturers of 'scopes. Well, we're not so little, and are well known in other instrumentation fields. We manufacture high technology instrumentation including Fourier transform infrared spectrometers, superconducting magnet NMR spectrometers, research and clinical medical instrument computers, real-time FFT spectrum analyzers, and signal averagers. In every one of these product areas we are leaders, or right near the top.

Nicolet has what was needed to conceive and produce general purpose digital oscilloscopes: A fresh viewpoint, imagination, a good knowledge of what an oscilloscope should be and exceptional expertise in the design of digital instrumentation.

There's much more you should know about the EXPLORER, and how it can help you. For complete details or a demonstration, send the reader service card or call Jim Bartosch at 608/271-3333.

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OSCILLOSCOPE DIVISION
5225 Verona Road, Madison, Wisconsin 53711
Telephone: 608/271-3333

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Circle 227 on reader service card

TEKTRONIX
Portable Oscilloscopes

22 high-performance models that go where you go.

Here's how to choose the TEKTRONIX Portable that's right for your application.

Tektronix offers an unmatched selection of 22 portable oscilloscopes, including six storage models, designed to meet the testing requirements of the electronics industry. These high-quality scopes are used for computer servicing, communication system maintenance, research, education, and production testing.

Your specific measurement needs should guide you in selecting the TEKTRONIX Portable that's best for you. First consider your performance, price and weight requirements. Then choose a model from one of our four oscilloscope lines. Each combines portability, reliability and ruggedness with unique features and capabilities.

400-Series Performance Leaders

Take lab quality into the field with TEKTRONIX 400-Series Portable Oscilloscopes. Choose from nine models including the 350-MHz 485, the widest bandwidth portable available today.

If you need to capture fast, nonrepetitive events, the TEKTRONIX 466 stores a single-shot waveform at its full 100-MHz bandwidth. For military system support, consider the 465M, also known as the U.S. Military's AN/USM 425 (v) 1. Fully provisioned and qualified to MIL-T-28800, Type II, class 4, style C the AN/USM 425 (v) 1 is the tri-service standard 100-MHz portable oscilloscope.

The factory-installed DM44 Delta Delayed-Sweep Option adds a direct numerical readout to five TEKTRONIX 400-Series Scopes. At $445*, it's the least expensive, most accurate way to make digital-voltage, current, temperature and differential-time measurements. In the photograph, the DM44 is shown with the high-performance 475A, our moderately priced 250-MHz oscilloscope.

Each TEKTRONIX 400-Series Portable weighs less than 26 pounds.

200-Series Miniscopes

These go-anywhere miniscopes are the perfect traveling companions. Powered by internal batteries or external ac, and weighing less than 3.7 pounds, 200-Series Portables fit easily into your briefcase or toolbox. Four models, with bandwidths to 5 MHz, are available. If you need to make numerical-voltage and current measurements, select the unique 1-MHz 213 DMM/Oscilloscope.

All 200-Series Miniscopes are ruggedized to withstand the high-shock conditions and extreme temperatures of remote locations.

300-Series Portables — Excellent Size/Weight/Performance Combinations

Four models from SONY/TEKTRONIX make up the 300-Series Family. All weigh less than 11 pounds, yet offer bandwidths to 35 MHz (the SONY/TEKTRONIX 335). Various oscilloscopes feature dual trace, delayed sweep, battery operation, and long-term storage.

Take SONY/TEKTRONIX 300-Series Portables with you for servicing industrial control systems, on-board ship equipment and remote computer terminals—wherever light-weight, medium-bandwidth scopes are required.

T900-Series Low-Cost Oscilloscopes

Priced from $695,* T900 Scopes are ideal for cost-sensitive education, servicing, and manufacturing applications. Choose from five bench-top models including four dual-trace and one delayed-sweep oscilloscope.

If your requirements call for a versatile, low-cost, 35-MHz scope, examine the two newest members of our T900 family—the T932A and the T935A. Both feature composite triggering and differential while retaining all the popular features of their predecessors (the T932 with variable trigger-holdoff and the T935 with delayed sweep).

All T900-Series Oscilloscopes are designed for ease-of-operation, simple maintenance, reliability and long life. They're the quality, low-cost scopes from Tektronix.

Service and Support Programs

Purchasing a TEKTRONIX Oscilloscope means more than buying an instrument from the industry leader. Applications assistance, training programs, worldwide service, and a large family of probes and accessories are available to help you get the most out of your TEKTRONIX Instrument. Classes in product theory and maintenance are also offered. The Long-Term Support Program insures continued parts availability. And your Tektronix Field Engineer will work with you to solve even the toughest servicing problems.

Here's How To Purchase a TEKTRONIX Portable.

To order a TEKTRONIX Portable Oscilloscope, contact your Tektronix Field Engineer. He can also arrange for a demonstration and provide complete specifications. Or for our latest Portable Oscilloscope Brochure, write: Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077. In Europe: Tektronix Limited, P.O. Box 36, St. Peter Port, Guernsey, Channel Islands.

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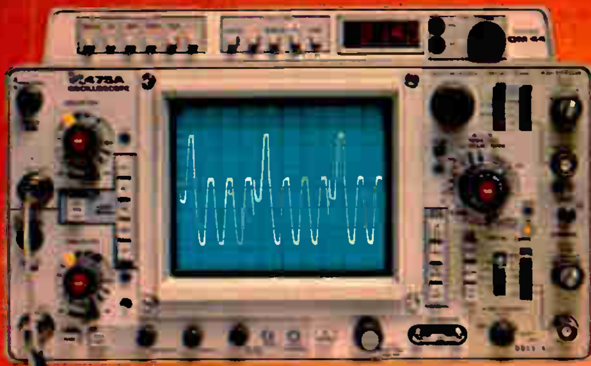
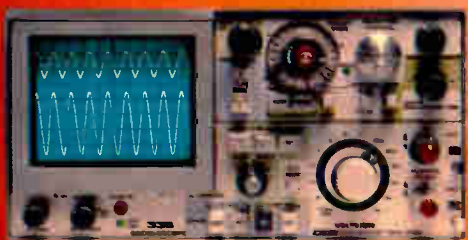
Circle 229 on reader service card



475A DM44

485



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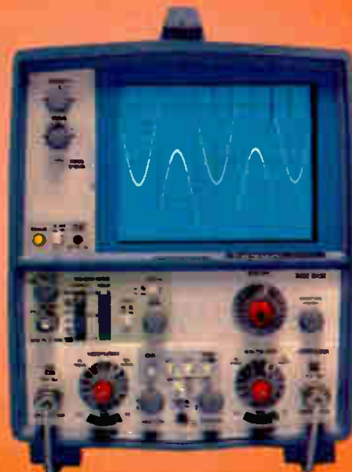
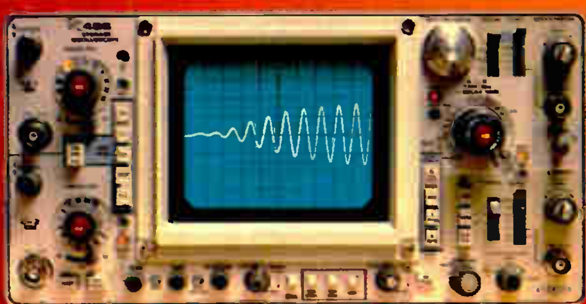


T935A



466

465M

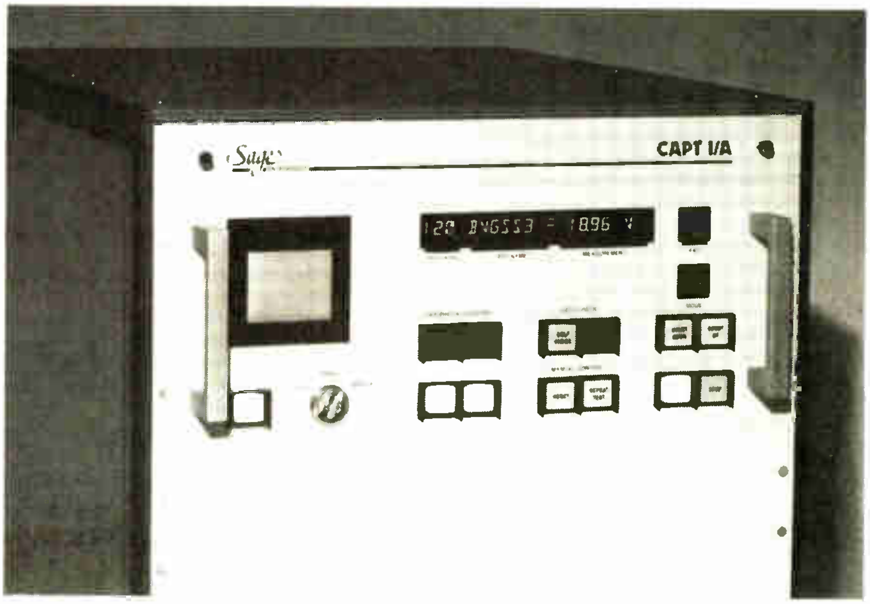
	Product	Bw	Dual Trace	Delayed Sweep	Fastest Sweep Rate	Other Special Features	Price*
Storage Models	466	100 MHz @ 5 mV/div	yes	yes	5 ns/div	3000 div/µs stored writing speed	$5050
	464	100 MHz @ 5 mV/div	yes	yes	5 ns/div	110 div/µs stored writing speed	4245
	434	25 MHz @ 10 mV/div	yes		20 ns/div	Split-screen storage	3350
	314	10 MHz @ 1 mV/div	yes		100 ns/div	Only 10.5 lbs (4.8 kg)	2475
	214	500 kHz @ 10mV/div	yes		1 µs/div	Only 3.5 lbs (1.6 kg)	1520
	T912	10 MHz @ 2 mV/div	yes		50 ns/div	Low-cost bistable storage	1350
Nonstorage Models	485	350 MHz @ 5 mV/div	yes	yes	1 ns/div	Widest bw in a portable	5400
	475A	250 MHz @ 5 mV/div	yes	yes	1 ns/div	High-performance 250-MHz portable	3665
	475	200 MHz @ 2 mV/div	yes	yes	1 ns/div	Highest gain-bw in a portable	3300
	465	100 MHz @ 5 mV/div	yes	yes	5 ns/div	Cost effective for 100-MHz bw	2375
	465M	100 MHz @ 5 mV/div	yes	yes	5 ns/div	AN/USM 425 (v) 1 Tri-service standard scope	2450
	455	50 MHz @ 5 mV/div	yes	yes	5 ns/div	Cost effective for 50-MHz bw	1925
	335	35 MHz @ 10 mV/div	yes	yes	20 ns/div	Only 10.5 lbs (4.8 kg)	1955
	326	10 MHz @ 10 mV/div	yes		100 ns/div	Internal battery	2180
	323	4 MHz @ 10 mV/div			500 ns/div	Only 7 lbs (3.2 kg)	1495
	221	5 MHz @ 5 mV/div			100 ns/div	Only 3.5 lbs (1.6 kg)	1025
	213	1 MHz @ 20 mV/div			400 ns/div	DMM Oscilloscope @ 3.7 lbs (1.7 kg)	1520
	212	500 kHz @ 10 mV/div	yes		1 µs/div	Low cost for dual trace & battery	1080
	T935A (New)	35 MHz @ 2 mV/div	yes	yes	10 ns/div	Variable trigger-holdoff and differential	1435
	T932A (New)	35 MHz @ 2 mV/div	yes		10 ns/div	Delayed sweep and differential	1155
	T922	15 MHz @ 2 mV/div	yes		20 ns/div	Low-cost dual-trace scope	885
	T922R	15 MHz @ 2 mV/div	yes		20 ns/div	Rackmount version of T922	1220
	T921	15 MHz @ 2 mV/div			20 ns/div	Lowest-cost TEKTRONIX Portable	695
Time Interval Readout	DM44	Optional, factory-installed, direct numerical readout of time intervals and DMM functions for the 464, 465, 466, 475, and 475A					445

*U.S. sales prices are F.O.B. [illegible]

Packaging & production

Testers are easy to program, run

13 versions of Sage's CAPT system permit user to write tests on mark-sense cards



Computer-based parametric testers generally require highly skilled programmers and maintenance technicians to get them started and keep them running. To help cut those labor costs, designers at Sage Enterprises set two major design goals for a line of 13 custom automatic parameter testers: operating simplicity and reduction of downtime.

To ease the pain of programming, Sage designed the testers so that a user may configure his own tests on simple, easy-to-use optical mark-sense data-entry cards. He then stores the string of tests on a small magnetic-tape cartridge that becomes the test program. The heart of what Sage has dubbed its CAPT system is a 16-bit Pace microprocessor from National Semiconductor.

CAPT is widely applicable; its 13 systems measure parameters of integrated-circuit wafers, bipolar transistors, high-power diodes, and a host of other devices, including

V-groove metal-oxide-semiconductor power field-effect transistors. All 13 are made with the same upper unit housing the Pace microprocessor and related boards, 20-character alphanumeric display, 2-character test results display, two-digit mode display, cartridge drive, panel switches, and panel lock-out switch. The bottom units are designed for the type of device to be tested and either a device handler or a wafer-prober test setup.

To program, specially prepared mark-sense cards contain test step, test name, test conditions and forcing functions, parameter maximum limit, parameter minimum limit, and branch addressing contingent upon test results. "The cards are just like those we've all used a million times," declares Bernard S. Siegal, one of Sage's founders, "and all the programmable items are described in English, not computerese."

After the user fills in the card with a No. 2 lead pencil, he feeds it into the card reader. When all the necessary test steps have been written and checked out, the card reader transfers the data onto a magnetic-tape cartridge inserted into the drive on the upper-left-hand corner of the system.

The same drive is used to load the special fault-identification and -location or calibration cassettes. Once loaded, the CAPT undertakes an extensive self-testing routine in which literally every function, switch, display, and subsystem circuit portion is examined and any failures are called out on the alphanumeric display and, if selected, the thermal paper-tape printer.

There is also a built-in diagnostic program that can be set to run after every n devices are tested. Thus, for example, if 100,000 transistors were to be tested, the user could ensure that no more than 1% of the devices could be erroneously tested by choosing n = 1,000.

Finding out why the system is down is of no real value if the problem cannot be quickly alleviated. Therefore, Sage will stock a supply of spare boards available to the user within 24 hours. Moreover, Sage will put together a suggested list of key components, subassemblies, and modules for a maintenance department to stock as a hedge against failures. "There is no way to eliminate downtime completely except with a redundant system," Siegal says, "but we have tried to reduce, as much as possible, the effects of a partial system failure."

Although the CAPT systems are capable of operating in a stand-alone fashion, they can be interfaced with a computer for data analysis via an RS-232-C data port. What's more, there are options available for adding a floppy-disk drive and a formatted-data line printer.

There are a lot of different ways to set up a multiple-CAPT system. All the testers could be working simultaneously, storing data in diskettes for later processing by a separate computer system, or they could be interfaced directly with a computer via their data ports. In any case, the throughput should be better than for a parametric tester that is really a minicomputer system with testing peripherals that must time-share the host.

The first CAPT system has just been shipped to Raytheon Co.'s Semiconductor division in Mountain View, Calif., Siegal says.

The prices for basic systems vary from approximately $23,000 to $28,000 depending on the degree of customizing required. The time from order to delivery ranges from three to six months, with a large part of it devoted to testing, burn-in, and retesting before shipping.

Sage Enterprises Inc., 1080 Linda Vista Ave., Mountain View, Calif. 94043. Phone (415) 969-5111 [391]

Prototyping boards boast iSBC 80 compatibility

Compatible with Intel's iSBC 80 in form and size, the 4608 and 4608-1 prototyping boards provide five edge-card connectors to simplify interfacing and are punched with 0.042-in. holes on 1-in. grids.

The 12-by-6.75-by-0.042-in. 4608 has power and ground buses, as well as pad arrays surrounding three-hole groups. It holds as many as 54 16-pin dual in-line packages in its patterned area and also has a 13-in.^{2} unclad area. The 4608-1 is the same size but has no etched patterns.

The five card-edge connectors on both models are compatible with Intel's Multibus and Microbus. The 86-terminal connector serves the system bus; two 50- and one 26-terminal connectors are provided for connection to flat-cable connectors; and a 60-terminal connector serves unassigned signals.

In quantities from one to four, the 4608 is priced at $45 and the 4608-1 at $34. Both epoxy-glass-composite boards are available from stock.

Vector Electronic Inc., 12460 Gladstone Ave., Sylmar, Calif. 91342 [396]

Data acquisition

I/O board reduces component count

SBC-series-compatible unit uses hybrid technology to optimize board layout

Realizing that there are already a number of other analog input/output subsystems that mate with Intel's popular SBC series of single-board computers, Micro Networks Corp. wanted its first entry into the I/O board market to offer something different. So it decided that by offering less it could offer more.

John Munn, manager of new market development, explains that the MN7300 has about one-third fewer components than a popular competitor. Although the board is still the same as those in the SBC series—for electrical and mechanical compatibility—the reduced package count allows the user more space on the board to optimize his layout or to reconstruct it. Further, Munn figures that the reduced package and pin counts offer more reliability than higher-density competitors.

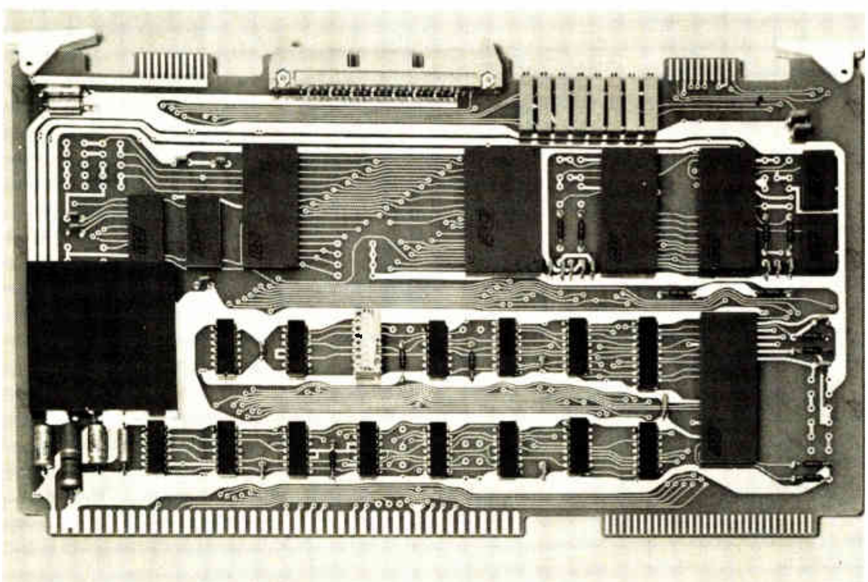
Key to the reduced package count is the use of thin-film hybrid microcircuitry, Micro Networks' forte. Most other designs use mixtures of integrated circuits in dual in-line packages and modules composed of discrete components, which naturally demand more room. The board's sample-and-hold module, for example, replaces four separate integrated circuits and associated resistors.

The MN7300 accepts analog inputs in any of five user-selectable ranges: 0 to 5 V, 0 to 10 V, ±2.5 V, ±5 V, or ±10 V. In its basic configuration with 16 single-ended channels, the board carries a multiplexing sample-and-hold amplifier, a 12-bit analog-to-digital converter, and a programmable-gain amplifier that lets the system's microprocessor pick any of eight gains (1, 2, 4, . . . , 128) with a 3-bit word. In this configuration, the converter sells for $612.

A multiplexer expander, which is an $83 option, doubles the input channels or lets the unit accept the same 16 inputs in differential mode. Two optional 12-bit d-a converters provide user-selectable voltage outputs in the same ranges as the inputs, while another two d-a converters provide outputs in the 4-to-20-mA range for current-loop applications. Each d-a converter is priced at $135.

The unit requires 5-V and ±15-V power, but with the dc-to-dc converter—a $55 option—it can operate from a single 5-V power supply. Delivery of the MN7300 is from stock to four weeks.

Micro Networks Corp., 324 Clark St., Worcester, Mass. 01606. Phone (617) 852-5400 [381]



Deglitching 12-bit d-a unit promises smooth, fast sailing

In a market swimming with modular, hybrid, and monolithic digital-to-analog converters, it takes some complex maneuvering to keep from getting swamped by the competition. Taking a new tack, Intech is running with a very stable, high-speed 12-bit d-a converter.

Designated the model A-866H-12, the modular device consists of selected components, Schottky diodes, and high-speed operational amplifiers used in a sample-and-hold-like scheme to keep switching glitches small and equal. It has a maximum settling time of 600 ns for a 10-V input step, and glitch amplitudes are specified never to exceed twice the value of the least significant bit. Nonlinearity stability is guaranteed to have a maximum temperature coefficient of ±3 ppm/°C. Pin-compatible with Datel's DAC-DG12B, the new module increases drive capability from that part's 10 mA to 40 mA.

John Dour, marketing vice president, believes that the unit will eventually carry his company into vast open waters. "We've already lost the low-end market to the monolithic d-a converters," he concedes, "but the market for 12-bit and higher precision devices, though small, is growing fast." Not only does he see a host of applications in the video display, sonar, and radar fields, but video and audio data reconstruction and recording should also add to the

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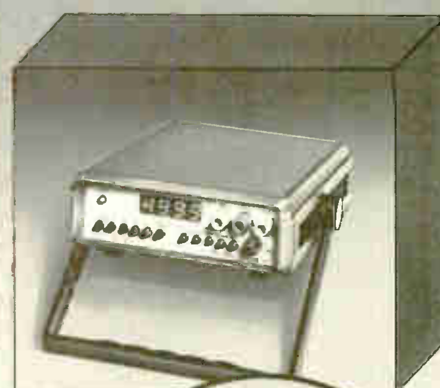

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Circle 236 on reader service card

number of market possibilities.

The A-866H-12 requires three supply voltages — ±15 and 5 v — and operates in the 0°-to-70°C temperature range. In addition to the tight nonlinearity temperature coefficients, the 2-by-4-by-0.5-in. module's gain and offset temperature coefficients are ±10 ppm/°C and ±p5 ppm/°C, respectively. In 100-and-up quantities, its price is $170.

Intech Inc., 282 Brokaw Rd., Santa Clara, Calif. 95050. Phone (408) 244-0500 [382]

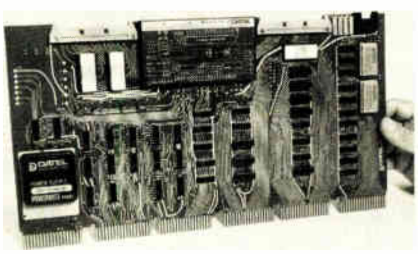
A-d converter card gives fast throughput

When plugged directly into the PDP-11's block connector and interfaced with its Unibus, the SineTrac analog-to-digital conversion board allows direct memory access to 64 single-ended or 32 differential channels. The 12-bit card, designated ST-PDP2D1C5, has a maximum conversion time of 20 μs, enabling it to handle data bursts of up to 45,000 samples per second.

Four input-voltage ranges are available: 0 to 5 v, 0 to 10 v, ± 5v and ±10 V. Input impedance is 100 MΩ minimum and 10 pF. At 25°C, SineTrac is accurate to within ±0.025% of full scale and linear to within ±½ least significant bit. Output coding is straight binary, offset binary, or 2's complement.

The 7.96-by-15.5-by-0.375-in. card takes up just six BB-11 connector-card slots on the Unibus. Included with the unit are a systems manual and a complete set of paper-tape diagnostic programs for accuracy and calibration checks and for troubleshooting. Two optional d-a channels are also available. The card may be purchased from stock singly for $2,750.

Datel Systems Inc., 1020 Turnpike St., Canton, Mass. 02021. Phone (617) 828-8000 [383]

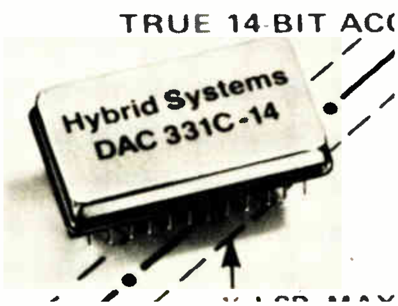


Multiplying d-a converter boasts true 14-bit accuracy

Claimed to be the first integrated-circuit multiplying digital-to-analog converter to offer true 14-bit accuracy, the DAC331-14 is capable of both two- and four-quadrant multiplication and offers maximum linearity error within ±½ least significant bit.

With the converter's proprietary 25/50-kΩ ladder network to produce the required accuracy, the effects of switch resistance are reduced by 60%. The thin-film resistor networks are trimmed to within ±1%.

The unit's temperature coefficients for linearity is ±2 ppm/°C for the full-scale range and for gain is ±3 ppm/°C. Power consumed is less than 30 mw, suggesting battery-powered equipment applications. Other possible uses include digital attenuation of ac and dc voltages, digital gain control, and stroke generators for cathode-ray-tube displays.



All models are compatible with transistor-transistor-logic devices and complementary-metal-oxide-semiconductor devices. In quantities of 1 to 24, an industrial-grade unit is priced at $69 and a MIL-STD-883B part costs $139. Delivery is from stock to four weeks.

Hybrid Systems Corp., Crosby Drive, Bedford, Mass. 01730 [384]

Microcomputers & systems

TI launches 8-bit processor

Unit is based on 16-bit 9900 design; features new input/output structure

While most microprocessor manufacturers are upgrading from 8-bit to 16-bit machines, Texas Instruments, is going the other way, from 16 to 8 bits. It is turning its popular 16-bit 9900 into a processor with byte-wide multiplexed buses and a new input/output structure. The thrust of TI's new 9985 is, predictably enough, toward the high-performance microprocessor market addressed by Intel with its 8085.

The 9985 uses a single 5-V supply and is housed in a 40-pin package, with built-in clock and timing circuits. The device has 256 bytes of random-access memory but no on-chip read-only memory. Its real pluses are carried over from the 9900 architecture: the same fast central processing unit and rich instruction set, which includes multiply and divide instructions; 16-bit address words for a capacity of 65,536 bytes of memory; 16 general-purpose registers, and five prioritized interrupts.

The 9985 emphasizes input/output capability and includes four types of channels: direct-memory-access, memory-mapped I/O, a bit-oriented interface for fields up to 16 bits that TI calls a communication register unit, and a serial port called a multiprocessing system interface.

The multiprocessing system interface is a two-wire interface that allows several 9985s to be hooked together and communicate with a serial bit stream. That way, 9985s acting as dedicated controllers in, say, a point-of-sale system can communicate over a twisted pair with a central computer.

Because the 9985 executes the same 16-bit instructions as the other processors in the 9900 family, including the 990 minicomputer, there is a wide software base available for it. For example, fully matured compilers are available for both Pascal and Fortran.

Samples of the 9985 will be available in September. The part is expected to be priced between $8 and $10 in 100-piece quantities.

Texas Instruments Inc., Inquiry Answering Service, M/S 308, P. O. Box 5012, Dallas, Texas 75222 [401]

Meta assembler eases bit-slice debugging

Debugging, emulating, and testing a bit-slice design can often be more demanding than the actual design of the controller or central processing unit itself. To ease this burden, Step Engineering has added a meta assembler compatible with most microcomputer-development systems to its line of bit-slice development products.

The meta assembler allows the user to define his own assembly language, as well as assemble the source code thus generated. When the assembler is used with Step 2, the company's stand-alone real-time development system, development is totally independent of the designer's architecture.

The program can be used on any single- or double-density development system that supports ISIS-II and has a 64-K random-access memory. Future expansion capability is provided by a Fortran version that can be installed on any 16-bit or larger computer.

Three separate subprograms make up the meta-assembler software: language definition, source assembly, and formatted object code. The definition segment lets the user define instruction mnemonics and their associated formats. It produces an output listing and disk file consisting of the defined items.

The source assembly subprogram operates like a traditional assembler and provides symbolic, relative, and page addressing, as well as conditional statements. The formatter program reads the object module file and translates it into microword format suitable for down-loading into a Step-2 system.

Accompanied by a detailed manual, test programs, and test output listings to verify proper operation, the meta assembler is priced from $800.

Step Engineering Inc., 714 Palomar Ave., Sunnyvale, Calif. 94086. Phone Steve Drucker at (408) 744-7837 [402]

can be removed and transported without adverse effects.

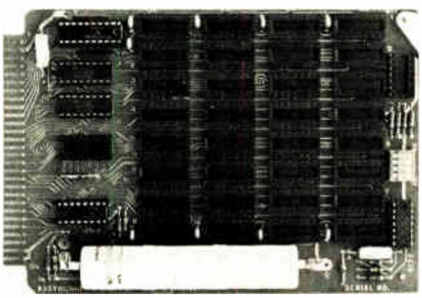
Two versions of the card are available, one for 6800-based systems and the other for 8080-based systems. Each may be specified without RAM or with RAM in 1-kilobyte increments. Prices range from $150 to $450 in single quantities, depending on memory specified, and delivery takes two to four weeks

Pro-Log Corp., 2411 Garden Rd., Monterey, Calif. 93940. Phone (408) 372-4593 [404]

Memory card has retention power

A 4-kilobyte random-access-memory card, the model 8122 can retain data stored in its complementary-metal-oxide-semiconductor RAM for up to 20 days without having to rely on an external power source.

The card accepts a maximum of 32 1,024-bit C-MOS RAMs in 1-kilo-



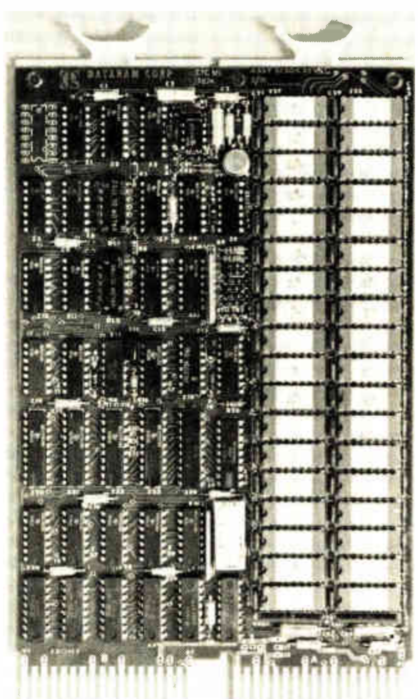
byte increments. Each kilobyte of memory has associated with it a write-inhibit switch that prevents inadvertent memory overwriting. In addition to full 16-bit address-word decoding capability, separate input and output data buses, and a jumper-selectable three-state input/output data bus option, the 8122 provides a battery backup that will keep the board powered from 5 to 20 days depending on the amount of on-board memory.

Upon detecting a power loss, the 8122 recharge circuitry automatically switches to battery power and immediately write-inhibits all memory. Although data retention will vary with the leakage characteristics of the C-MOS RAMS used, the 8122

Dual-board add-on memory takes to the Q-bus

Compatible with Digital Equipment Corp.'s Q-bus interface, the DR-115S is a dual-board memory that can be added to the LSI-11, LSI-11/2, or PDP-11/03 microcomputer systems. The memory is available in parity (18-bit) and nonparity (16-bit) versions, and a choice of 8, 16, or 32 kilobytes is offered. Cycle and access times are 500 and 325 ns, respectively.

The DR-115S has on-board refresh circuitry and provides the logic

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needed to add a backup battery. In single quantities, parity and non-parity versions of the 32 kilobyte memory are priced at $1,475 and $1,400, respectively. Delivery is 30 days after receipt of order.

Dataram Corp., Princeton-Hightstown Road, Cranbury, N. J. 08512. Phone (609) 799-0071 [407]

M6800s can take care of common business

Among likely markets for microcomputers, many original-equipment manufacturers look to small businesses, which is one reason why a Cobol compiler for use with M6800-based systems is now available to OEMS.

Named the M68COBOL010M resident ANS Cobol compiler, the program contains the entire Level 1 ANSI-standard Cobol, plus higher-level features that will speed up software development. It has been written for use on an Exorciser microprocessor development system equipped with an Exorterm 100 display console, an Exordisk II floppy-disk system, and 32 kilobytes of memory. Alternatively, it may be used with an Exorterm 200 development system configured with the same disk system and size of memory.

Providing both sequential and random disk addressing, the compiler has 11 input/output commands, including start and read next. It also has automatic page-mode formatting, expanded field editing, paragraph name trace, exhibit statement, and a compilation speed of 500 statements per minute. Features from higher-level Cobol include compute, search, and inspect commands, as well as complex logic conditions and nested IF statements. By taking advantage of the 6800's decimal arithmetic capability, the software offers the decimal mode preferred for business applications.

The compiler has a license fee of $1,195.

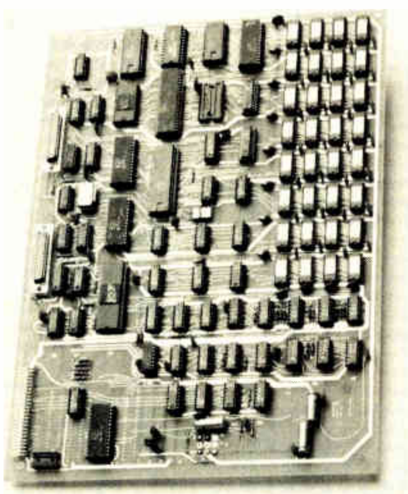
Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Ariz. 85036. Phone Gary Hughes at (602) 244-4035 [403]

Single-board unit supports disk operating system

The MicroStar/5 single-board computer is a complete microprocessor-based computing system that supports the CP/M disk operating system, including Basic, Fortran IV, and Cobol. The system will interface with a variety of IBM-compatible drives, such as the Shugart SA 800 and 850 and the Calcomp 142M and 143M.

Onboard the unit is an 8085 microprocessor, an 8271 floppy disk controller, 16 to 64 kilobytes of random-access memory, real-time clock, programmable interrupt controller and wo RS-232-C interfaces.

A MicroStar/5 with a 32-K RAM is priced at $1,270 in large quantities. Available software includes a macro-assembler, interactive debugger, interactive editor, and text processor. A bootstrap loader is an integral part of the system.



A complete CP/M application software development system, with 32-K RAM, dual floppy-disk drive, and interfaces for video display terminal and printer, is priced at $3,995.

Micro V, 17777 S. E. Main St., Irvine Calif. 92714. Phone (714) 957-1517 [406]

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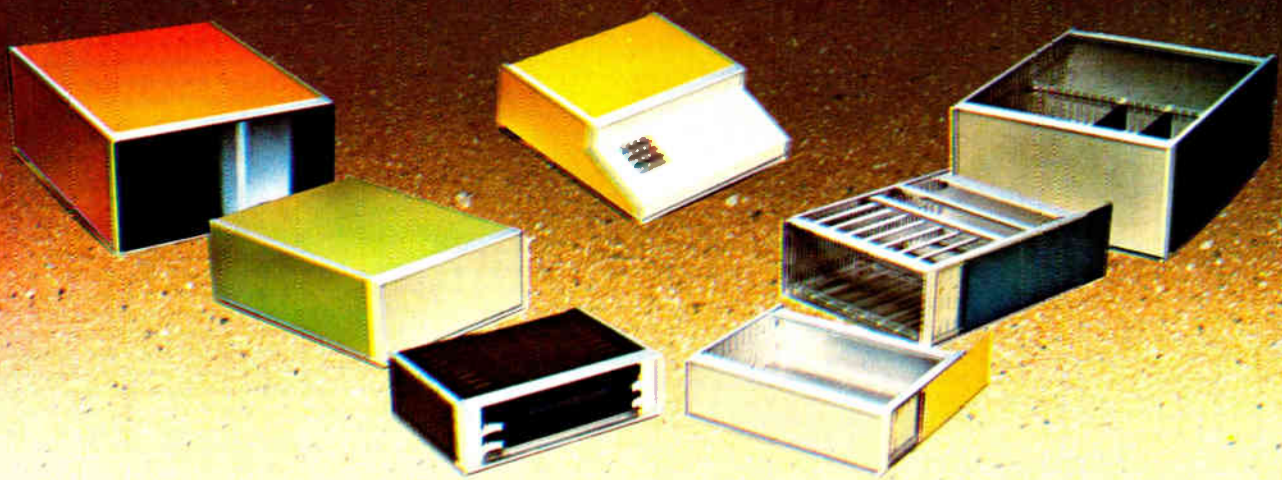

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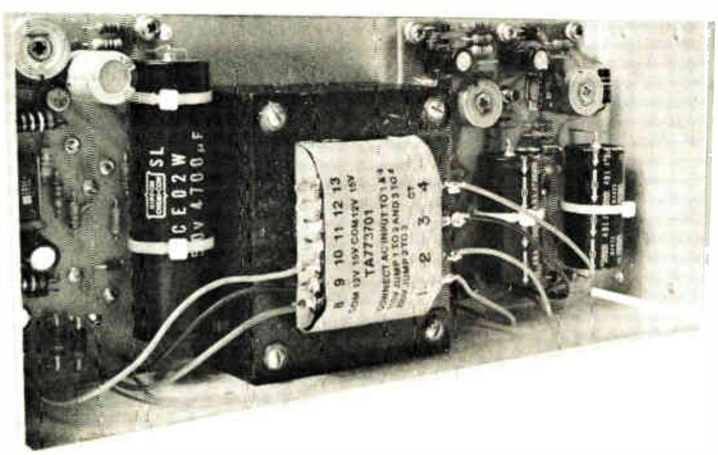

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Angle indicator sells for $495

Synchro/resolver panel meter is accurate to within 0.2°, operates from 50 to 1,200 Hz

Blending its ac instrumentation technology with the large-scale integrated circuitry and digital panel meter designs of outside suppliers, North Atlantic Industries Inc. has developed an indicating synchro-to-digital converter that satisfies an industry need for a small, universal, low-cost device for measuring synchro/resolver shaft position.

Designated the model 800, the synchro panel meter has a p-channel metal-oxide-semiconductor circuit containing approximately 500 gates and is housed in a 48-pin package. The LSI chip has all the logic functions and analog switches necessary for implementing the converter's unique math model. "This combination of math model and LSI processor permits a significant reduction in component count: about 50%," says sales manager Ken Salz.

Priced at $495 in small quantities, the 800 is unlike low-cost competitive designs, such as those that use peak sample-and-hold techniques, in that it has a full type II tracking converter. Hence, Salz claims, errors caused by velocity, noise, and harmonics are reduced to insignificant levels. However, he concedes, the 800's overall error of 0.2° is greater than that of some higher-priced synchro-to-digital converters. The unit can resolve 0.1°.

Deliverable from stock to six weeks, the 800 can be pin-programmed for synchro or resolver operation at 11.8, 26, or 90 V line to line. It accepts a reference of 50 to 1,200 Hz at 26 or 115 V and fits a standard DIN panel meter cutout of 1.75 by 3.625 in., thus allowing for complete installation flexibility in almost any system configuration. The ability to power the unit via the reference terminals, Salz says, is "a key and very novel" feature that makes the instrument "extremely versatile and saves the user the additional effort of making power connections."

Aside from the standard 0-to-359.9° readout that the unit's 0.3-in.-high light-emitting-diode readouts display, the 800 also is available with ±179.9° and 0-to-9,999° scaling. The latter, Salz notes, allows for precise monitoring of flow measurement, batch-weighing systems, nuclear rod positioning, and other industrial applications. An offset control allows a ±2° adjustment for final system zeroing without the

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Processor Technology

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sometimes difficult task of physically tweaking in a remote synchro.

Through use of an input Scott-T (isolation) transformer, the 800 attains a high input impedance of 100 kΩ and high common-mode rejection (on the order of 100 dB). Hence, Salz notes, "there is no need to consider instrument-loading effects in the measurement." Furthermore, the 800 provides a binary-coded-decimal three-state output (10 loads), tracks up to 1,500° per second, and measures 1.9 by 3.8 by 7.84 in., including connector.

North Atlantic Industries Inc., 60 Plant Ave., Hauppauge, N. Y. [371]

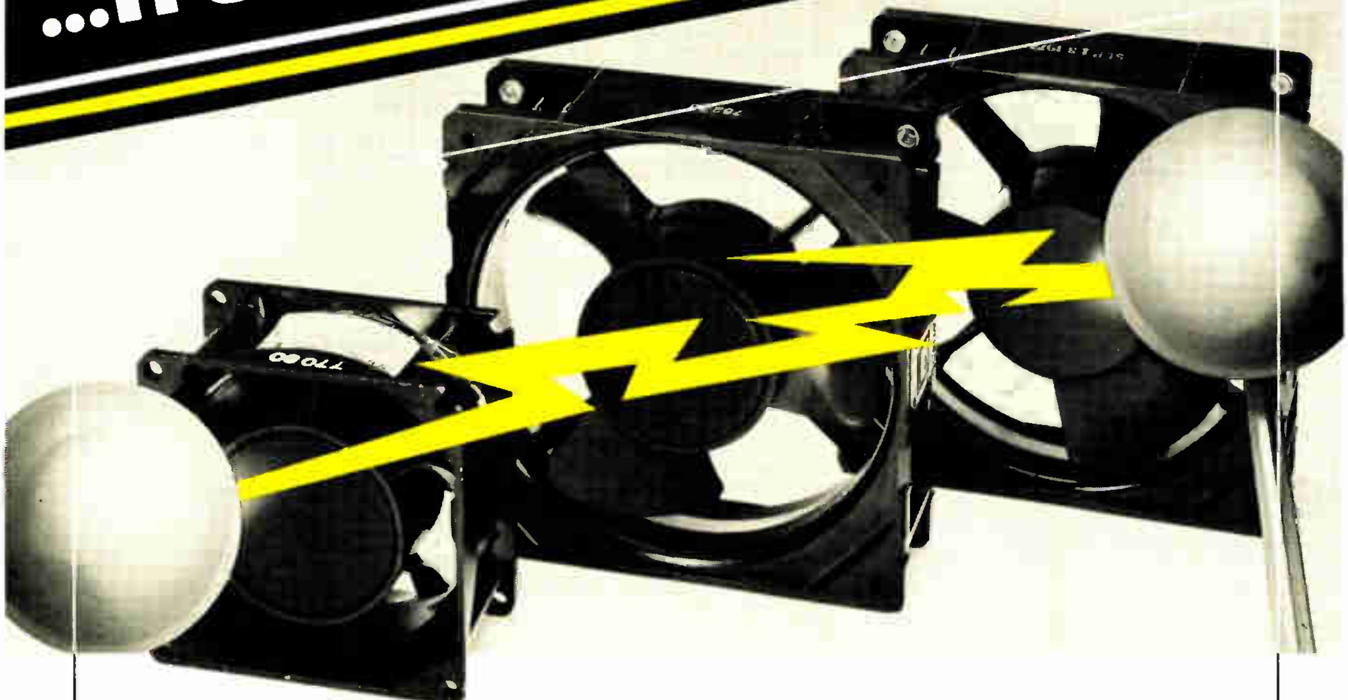
Pressure transducer fits wide variety of OEM needs

A likely candidate for consideration by original-equipment manufacturers is the model AB pressure transducer, a unit with various design features that suggest it for use in applications ranging from medical instrumentation to truck engine-performance monitoring.

Available in full-scale ranges of 6 to 20,000 psi, the units are constructed of 316 of 15-5 PH stainless steel in a single piece to ensure survival in harsh environments. Units are offered in both gage and absolute versions, with cable or integral connectors, and in waterproof and explosion-proof models. The standard model is rated as intrinsically safe. Low-range gage models respond to negative pressure.

The combined effects of nonlinearity, repeatability, and hysteresis result in inaccuracies of 1% or less

Revolting developments ...from Rotron



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for the standard model and 0.5% or less for the improved version. All units are compensated for temperature effects from 30° to 130°F.

The transducers may be either mounted in a variety of metal or plastic adapters or flush-mounted where requirements so dictate. In single quantities, units are priced beginning at $195; in larger quantities, discounts are available.

Data Instruments Inc., 4 Hartwell Place, Lexington, Mass. 02173. Phone R. Minard at (617) 861-7450 [374]

3½-digit temperature meter linearizes thermocouples

The ability to linearize signals from any one of seven standard types of thermocouples is just one of the attractive features of Hades' latest digital thermocouple indicator. In the field, its linearizing curves can be changed for different thermocouple types and the scale set for Celsius or Fahrenheit readings.

The meters have a maximum total error of 2° for a full-scale reading and can resolve 1°. They provide 1,400-V isolation between thermocouple input and power ground, a common-mode rejection ratio of 130 dB, and a normal-mode rejection ratio of 100 dB.

Indicators are offered with a buffered, linearized analog output of 1 mV/°C or/°F, as well as with a latched and buffered parallel binary-coded-decimal output. Status, control, and timing signals have been provided also.

The meters can be powered from 110 or 220 V ac, 5 V dc, or 8 to 28 V dc. Prices for the meters start at $179 each in quantities of one to nine and delivery is from stock.

Hades Manufacturing Corp., 151A Verdi St., Farmingdale, N. Y. 11735 [376]

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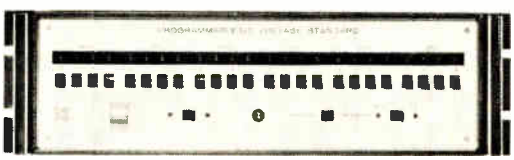

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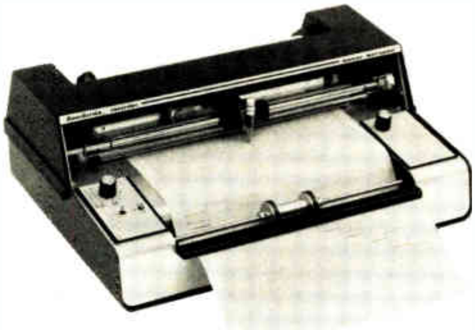

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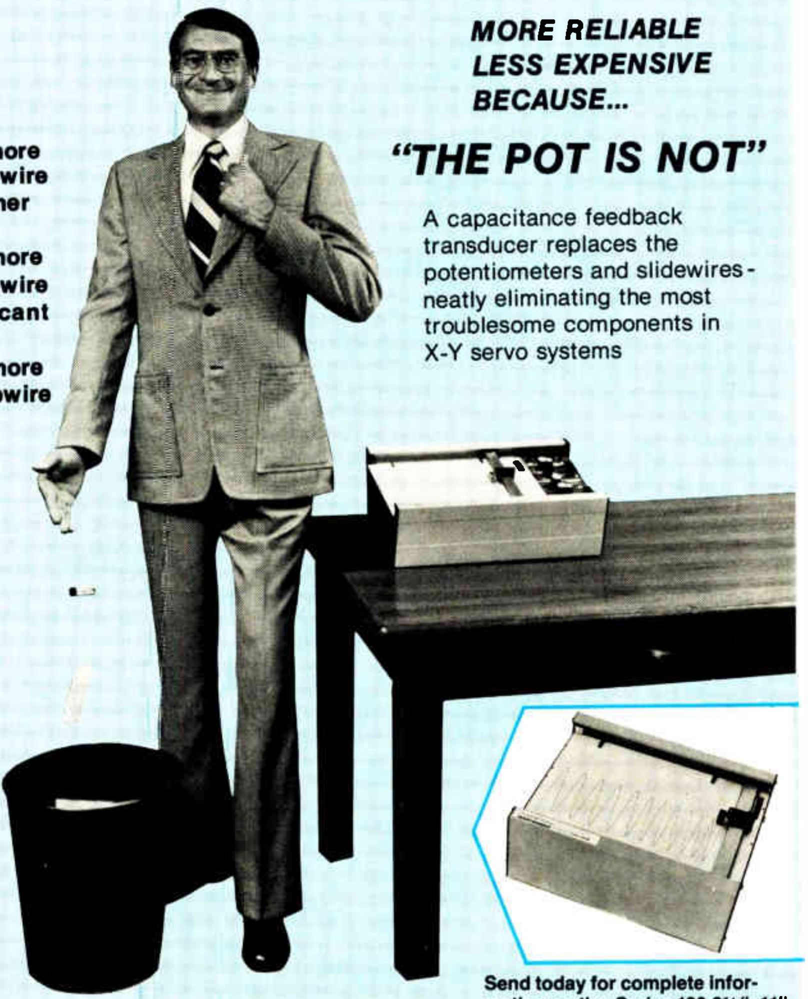

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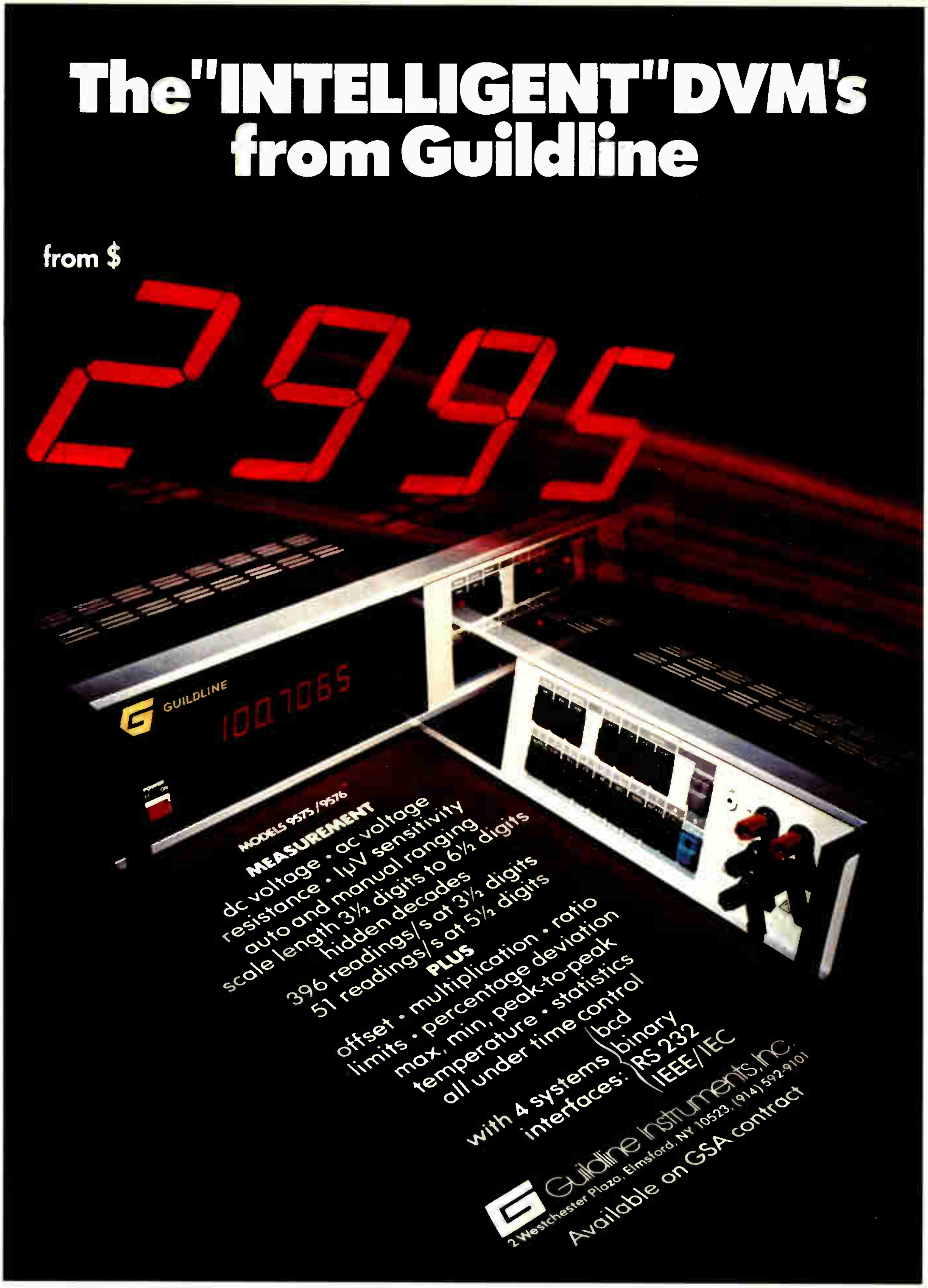

Wescon - Booths 939-941

Products newsletter

Boxed iSBC 80/30 has multiprocessor orientation

Intel Corp., Santa Clara, Calif., will package its iSBC 80/30 single-board computer one step further by combining it with a power supply and cooling fans in a standard 19-in. enclosure. Designed for both distributed computing and multiprocessing applications, **the 80/30 seems especially useful in the multiprocessor area because of its triple-bus architecture,** which provides multiple-processor bus-arbitration logic for sharing memory, peripherals, and input/output accessories. The system sells for $2,260.

Twisted pairs added to wiring service

Bondex Inc., a contract wiring firm in Waltham, Mass., specializing in automated routing and reflow soldering of heat-strippable wire to solder-coated pads on standard printed-circuit boards, has come up with a new wrinkle. **Now Bondex can add on twisted pairs for those circuit lines that are particularly sensitive to noise or that require a low characteristic impedance.** The impedance of the twisted pairs may be anywhere between 50 ohms and 90 ohms.

8085A family has a second source

The 8085A microprocessor and its principal support circuits are being second-sourced by NEC Microcomputers Inc., Wellesley, Mass. **Included in the family are the μPD8085A microprocessor,** which has a 1.3-μs cycle time and sells for $12 in hundreds; the μPD8155/56 2,048-bit static random-access memory with its 100-up price tag of $11; and the μPD8355 read-only memory, which goes for $8 in hundreds and has a delivery time of 10 to 12 weeks after data verification. Later in the fall, the μPD8755A erasable programmable ROM will be offered at $48 in hundreds.

Logic state analyzer gets remote control

A plug-in serial interface board from Paratronics Inc. allows its model 532 logic-state analyzer to be controlled remotely. According to the San Jose, Calif., firm, the control can be through a modem, **which opens the door to field servicing under the direct control of a factory computer.** The model 532 weighs less than 10 lb and sells for $1,800; the interface board adds $350 to its price.

System analyzer supports 4-MHz Z80A-based systems

The designers at Millenium Systems Inc., Cupertino, Calif., are putting the finishing touches on the new Z80A emulation adjunct to their universal microprocessor field-service tool—the Microsystem Analyzer. This will enable users **to apply the system's combination of signature analysis and in-circuit emulation to designs based on the 4-MHz Z80A.** The package will be available for $1,000 in October. A Microsystem Analyzer with both signature analysis and the Z80A emulation package sells for $3,750.

Price changes

Recently announced price reductions include:

- A drop of 25%, on the average, for optical waveguide fibers made by **Corning Glass Works,** Corning, N. Y.
- Reductions of $20 (from $195 to $175) for the HP-29C and $70 (from $345 to $275) for the HP-19C calculators from **Hewlett-Packard.**
- Cuts ranging up to 14% in half of the single-output power supplies made by **Deltron Inc.**

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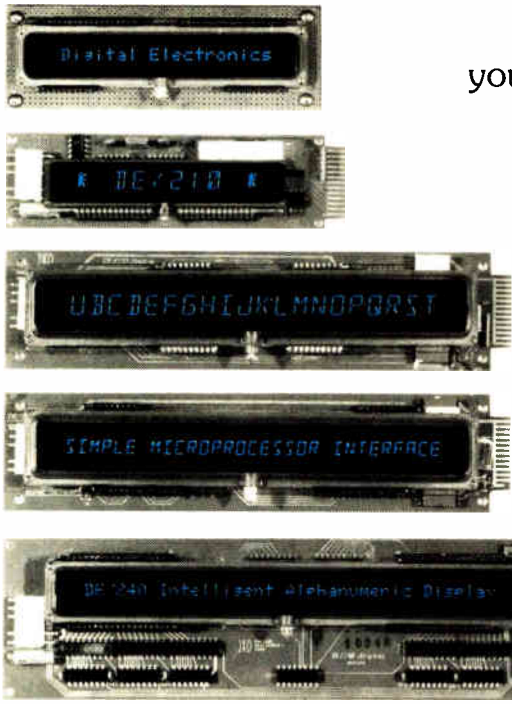

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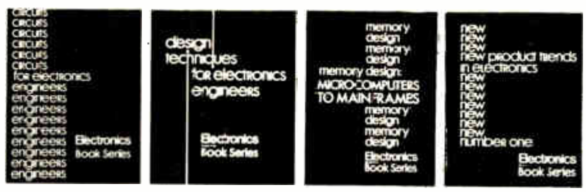

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Transene Co. Inc., Route One, Rowley, Mass. 01969 [476]

Polymer pastes for use in the manufacture of liquid-crystal displays are first cured, then sealed in a two-step heating process. Thermoplastic formula F-100 produces an adhesive bond generally stronger than the fracture strength of the glass substrates. An added pigment, which acts as a visual aid, will change color and eventually disappear if the material is overcured. The otherwise similar NF-100-1 also contains particle spacers of 8 to 10 μm that help control the distance between glass plates during the sealing cycle. Both NF-100 and NF-100-1 have viscosities of 350 poises when measured at a shear rate of 9.6 s^{-1}. NF-200 is a conductive paste that can be used for screen-printing interconnections to LCD numerical segments. The materials may be removed by a solvent wash. In production quantities, the seal pastes are $0.68 a gram and the conductor is $0.82 a gram.

Thick Film Systems Inc., 324 Palm Ave., Santa Barbara, Calif. 93101 [477]

An epoxy paste adhesive, Eccobond Solder 74C, has a volume resistivity of 0.02 ohm-cm. Similar in performance to silver-filled adhesives, this paste can be used for making electrical connections where hot soldering is impractical. It will not flow when applied and will give good bond strength to various metals, ceramics, and plastics. Curing temperatures can vary, but curing at 150°F (66°C) or above yields the lowest resistivity. Eccobond 74C has a tensile lap shear strength of 1,850 psi and a flexural strength of 11,200 psi. In 1-lb kits, it sells for $65 each.

Emerson & Cuming Inc., Dielectric Materials Division, Canton, Mass. 02021 [478]

A ceramic potting compound is intended for the encapsulation of conductive elements in devices such as crankcase heaters, power transformers, power rectifiers, and triacs. Cermacast 510 has a compressive strength of 7,500 psi, a modulus of rupture of 1,500 psi, and a dielectric strength of 50 v/mil. The material sells for $30 a quart, $50 a gallon, and as little as $15 a gallon in 50-gallon lots. Delivery is usually from stock.

Aremco Products Inc., P. O. Box 429, Ossining, N. Y. 10562 [474]

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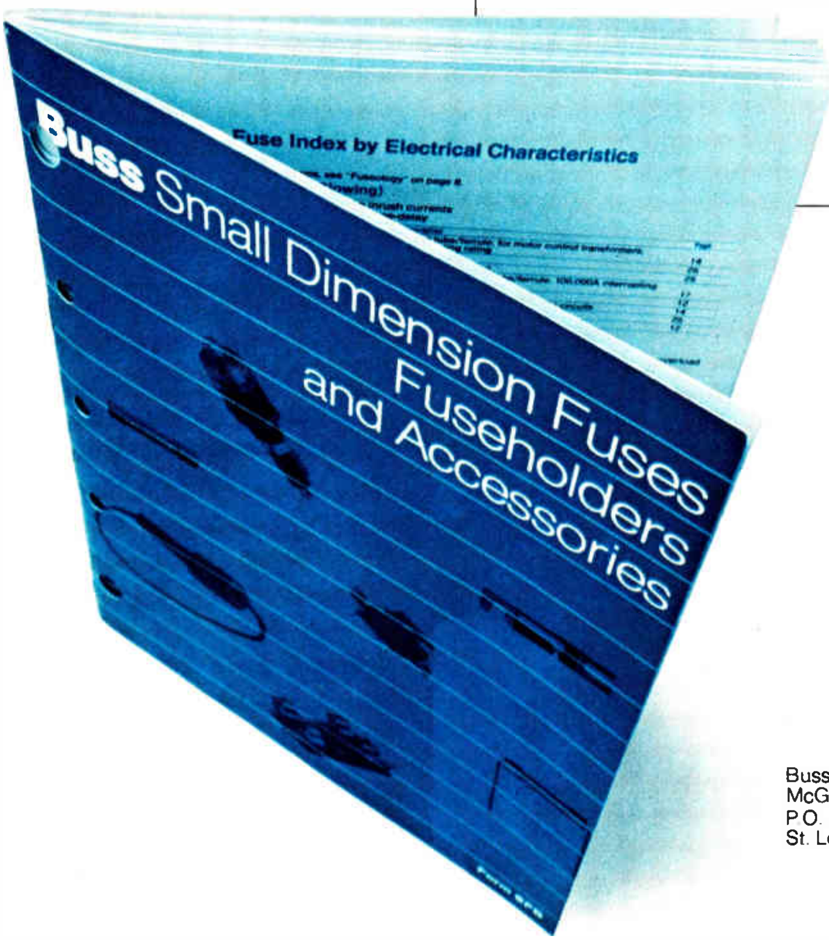

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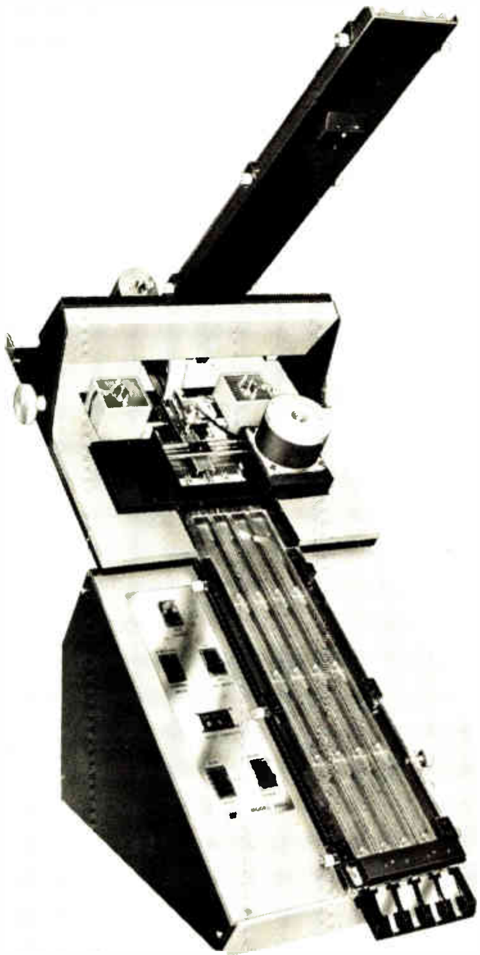
Statistics. Anyone who wants to know what the business statistics for the past 5 or 10 years in the West European electronics industries look like can now get a detailed report—"The Mackintosh Yearbook of European Electronics Companies 1978." The 104-page book lists the 50 largest firms that manufacture electronics products in Western Europe, all of which have sales of $100 million or more. Sales figures are broken down by major product groups. The book sells for $50. Mackintosh Publications Ltd., Napier Rd., Luton, LU1 1RG, England

Measurement services. The 1978 edition of "Calibration and Related Measurement Services of the National Bureau of Standards" revises the last edition, issued eight years ago. It presents detailed descriptions of the services mentioned in the title. Test methods and applicable industry standards are covered, and a bibliography of technical references is provided. The book will be updated every six months with an appendix containing price lists, changes in service, and a directory of NBS personnel to contact for further information. It sells for $3 each. Ask for SN-003-003-01916-0. Superintendent of Documents, U. S. Government Printing Office, Washington, D. C. 20402

Data acquisition. "Data Acquisition Products," a 600-page catalog, contains data specifications and prices for a line of precision data-acquisition components, data converters, signal-conditioning components, temperature transducers, digital panel meters, computer-interface equipment, and microcomputer-compatible analog input/output subsystems. Also included are tutorial sectors for each type of device. Analog Devices Inc., P. O. Box 280, Route 1 Industrial Park, Norwood, Mass. 02062. Circle reader service number 422.

Power supplies. Intended for the design engineer, the 1978 "Engineering Power Supply Handbook" details the electrical and mechanical parameters on more than 180 power supplies. The products include single-, dual-, and triple-output line-operated power modules; 1-, 3-, 4.5-, 5-, and 10-watt dc-dc converters; and a dc-dc converter module for use in microcomputers. In addition, it explains power-supply principles, practices, and terminology. Datel Systems Inc., 1020 Turnpike St., Canton, Mass. 02021 [423]

Lamps. "Precision Lamps," a 36-page catalog, gives details about subminiature, miniature, telephone slide-base, miniature fluorescent, and photographic lamps. It lists envelope shape and size, base type, filaments, support and lead-in wires, lamp dimensions, electrical and illu-



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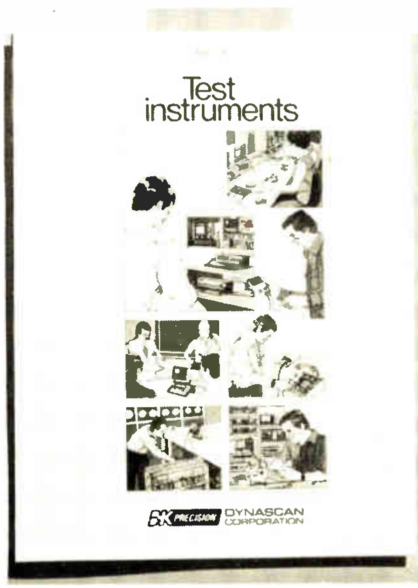
New literature

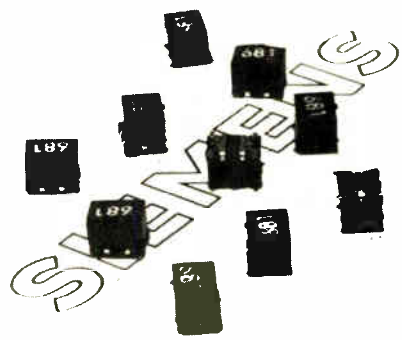
mination characteristics, and operating parameters. A review of lamp construction, characteristics, and specifications is also given. Precision Lamp, 950 N. Rengstorff Ave., Mountain View, Calif. 94043 [424]

Test instruments. A 48-page brochure gives information on a broad range of test instruments, including oscilloscopes and semiconductor testers. Detailed specifications are given and suggested applications are supplied for each instrument,



along with a discussion of what makes each unique. Precision B & K, Dynascan Corp., 6460 West Cortland St., Chicago, Ill. 60635 [425]

Alphanumeric display terminals. "All about Alphanumeric Display Terminals," a survey report, is based on responses of 742 users who rated 20,000 installed alphanumeric display terminals for overall performance, ease of operation, display clarity, hardware reliability, maintenance service, and software and technical support. The report compares specifications and prices for 261 display terminals from 88 vendors and provides guidelines for selecting the best terminal for buyers' needs. It sells for $12 each. Datapro Research Corp., 1805 Underwood Blvd., Delran, N. J. 08075



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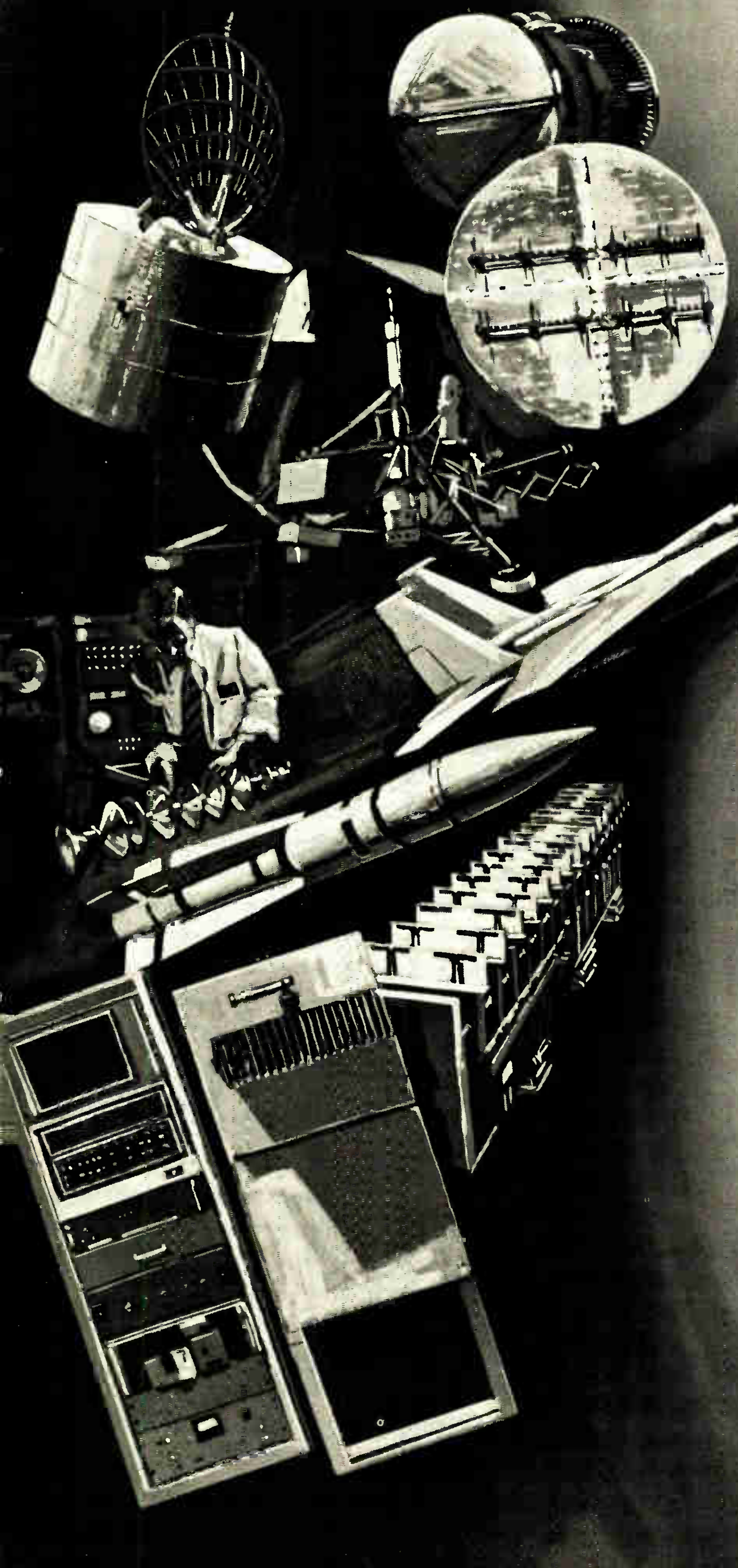

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The ideal experience for this position will include prior design exposure in a high technology engineering group working in a small team environment plus 5-7 years' related test experience, reviewing and improving basic product circuit and logic design, and a background in the design of test fixtures for digital and analog equipment. You must also have some microprocessor design and automatic test set design experience with emphasis on hardware design.

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To arrange for a confidential interview, please send your resume including present salary and requirement with indication of specific position in which you are interested to, or call: Patrick H. Augustine, Director, Personnel at (516) 231-5005 (no agency calls, please). Databit, Incorporated, 50 Davids Drive, Hauppauge, New York 11787. We are an equal opportunity employer m/f.

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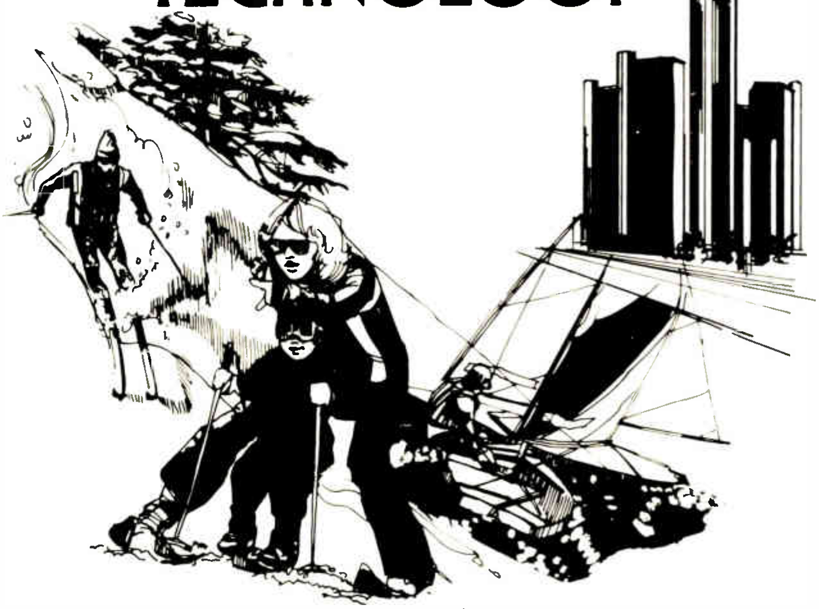

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Assume responsibility for the development of a 64K VMOS dynamic RAM. Scope includes product definition, circuit design, layout, product engineering and test engineering. You must have an MSEE, Ph.D. and 5 years memory design with recent 16K or large scale next generation dynamic RAM experience.

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SENIOR DESIGN ENGINEER

You will be responsible for circuit design, layout, debugging, test definition for the development of this next generation VMOS dynamic RAM. Project Management includes coordination with various organizations such as CAD and mask shop. Position requires MSEE, Ph.D. and 3 years in Memory Design with dynamic RAM experience.

ENGINEER

Responsibilities include development of a VMOS dynamic RAM process, including running experiments in fab, analysis and development and documentation of process steps. MS, Ph.D. and 1 year industry experience required or Graduate with solid state background and college lab experience.

SENIOR PRODUCT ENGINEER

Responsibilities will include dynamic RAM Product Engineering (checking design, debugging yield analysis product characterization, and coordinating with test, process and reliability groups). MSEE with 3 years experience in memory product engineering required.

SENIOR TEST ENGINEER

Your responsibilities will encompass dynamic RAM test program development, hardware design and product characterization. MSEE with 3 years experience in memory test program development with 1 year in dynamic RAMS required.

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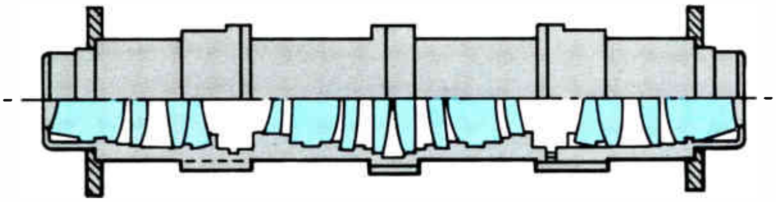
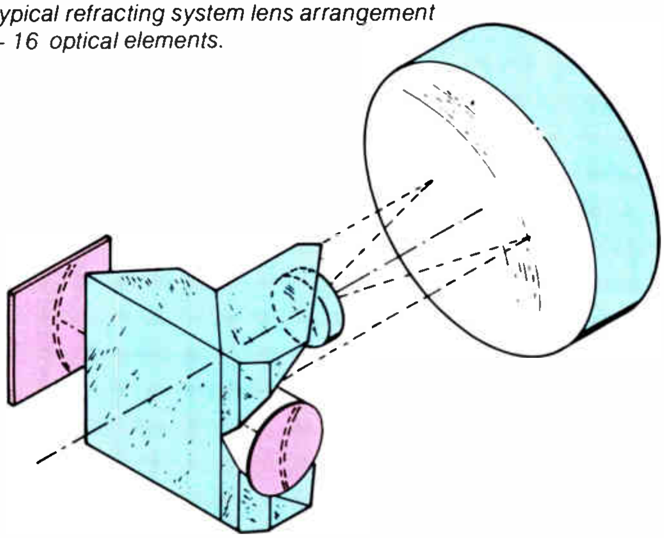


Typical refracting system lens arrangement — 16 optical elements.



The MICRALIGN all-reflecting folded projection system — three optical elements.

Compare these two lens systems. Until Perkin-Elmer introduced the Micralign Projection Mask Alignment System five years ago, all manufacturers of projection systems used refracting optics. Most still do.

Complex refracting optics

Refracting optics can involve as many as 16 separate lenses. Such complexity has several drawbacks. In spite of antireflection coatings, the individual lenses scatter light. Imperfections in the glass scatter light. And all this scattered light affects image quality. It limits the use of negative photoresist. In addition, standing wave effects make the system hard to use.

Simple reflecting optics

Note the contrast with the Micralign reflecting optical system. Its simple design employs only three reflective elements, no refracting lenses. Scattered light is near zero. Ghost images are eliminated, image quality is enhanced.

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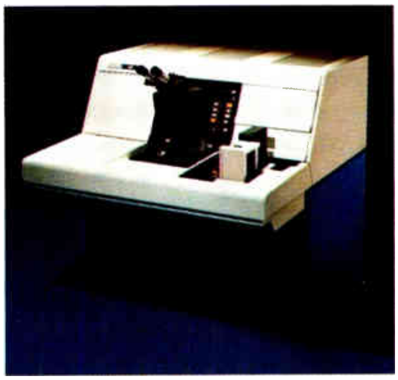

Model 140— the third-generation MICRALIGN instrument.

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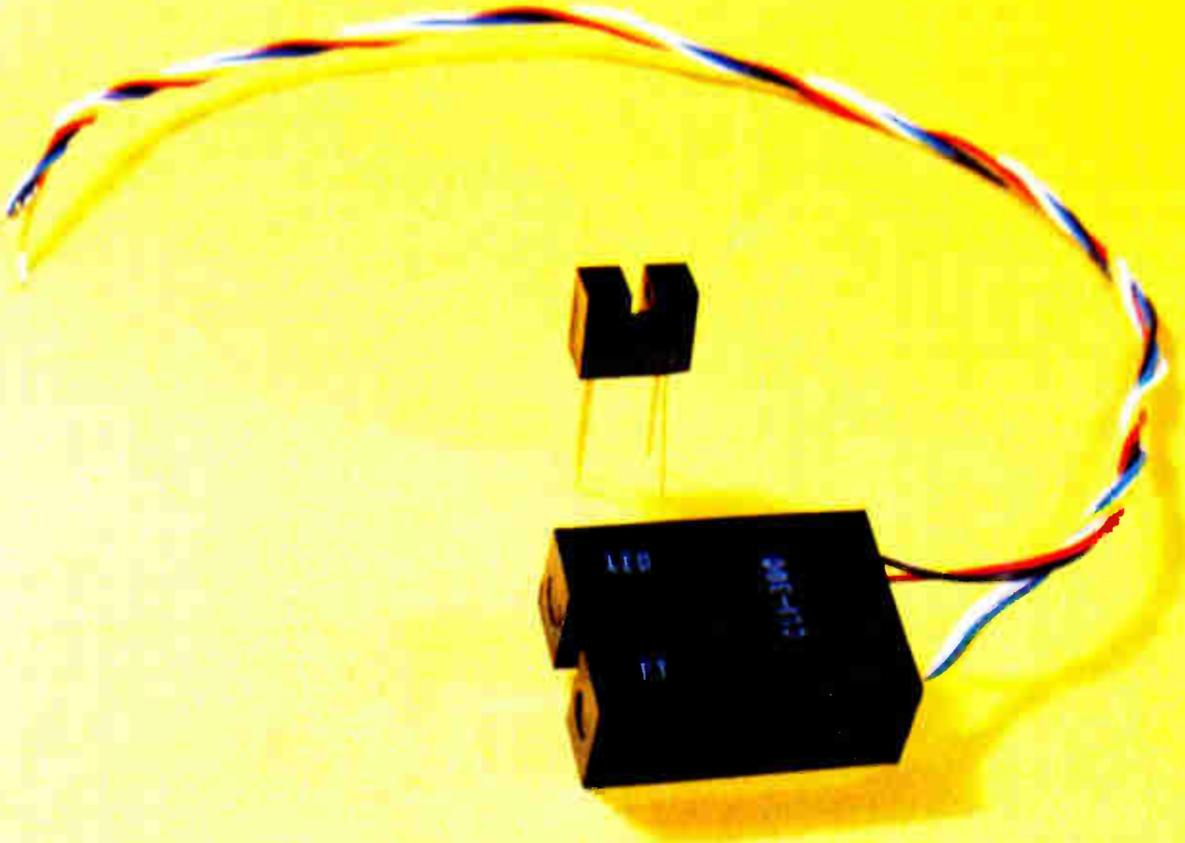

Clairex optical switches are made with hermetically sealed emitters and detectors for maximum reliability. Glass lenses align the light beam to improve target detection, to minimize false triggering from stray light, and to reduce dust pickup.

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