

APRIL 15, 1976

THE PRICE WAR IN HYBRID DATA CONVERTERS/35

Current tracer isolates digital-circuit faults/177

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Electronics[®]

MICROPROCESSORS

Roundup of available components

Learning to design systems

Evaluating software

Applications

Design aids

Testing



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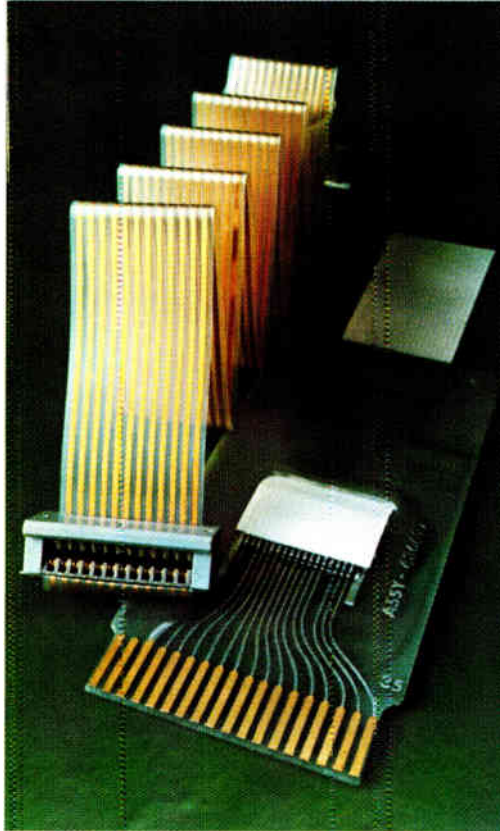
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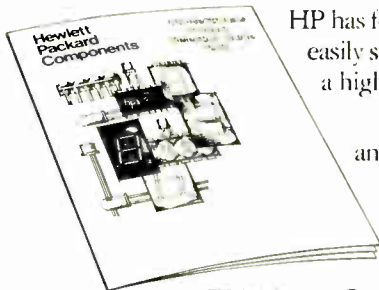
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Highlights

Cover: Making it with microprocessors, 74

Microcomputers on chips are not only revolutionizing and expanding the electronics universe—they're also turning circuit-design techniques upside down. Opening up ahead of the engineer is a myriad of opportunities requiring new disciplines. This special issue is a guide to both.

Cover device is a 6800 microprocessor from Motorola Semiconductor.

Introduction, 76

Chips and boards, 78: This roundup of the latest devices puts them in perspective, explaining where they fit best.

Software, 104: Effective programming depends on the right choice of language level and caution in using support software.

Design aids, 114: Some of the new development systems can emulate not-yet-built hardware and can handle more than one type of processor chip.

Testing, 125: Level of confidence is all-important in determining which chip-testing techniques are right for a given application.

Applications, 134: Designers of fourteen successful microprocessor-based systems outline what they did and why it worked.

And in the next issue . . .

Preview of Electro/76 . . . special report on industrial lasers . . . a guide to computer-aided-design programs.

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Microprocessors represent the closest thing to a revolution to hit digital circuit design in a long time. True, these potent little packages of computing power have been available for a couple of years. Yet the pace of progress in both applications and device development has built up so fast recently that "technological evolution" seems too slow-footed a term to describe the phenomenon.

To help all of our readers to understand what microprocessors are, how they work, and how they can be used, we are publishing this special issue of *Electronics*. In it, you'll find a 62-page package of microprocessor information, ranging from hardware to software, from circuit and device specifications to applications details.

The result of many months of planning and countless man-hours of preparation, reporting, and writing, this report should prove valuable to the newcomer to microprocessors as well as the designer who has been with microprocessors ever since they first came on the scene.

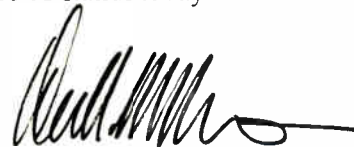
The team that put together the roundup, under the direction of executive editor Sam Weber, was headed by senior editors Larry Altman and Steve Scrupski, whose areas of specialty, solid state and computers, respectively, overlap in microcomputers. And, because the growth in microprocessor applications is having such an impact on so many other areas, the rest of the team represented a cross section of electronics. Contributing were Don Blattner, circuit design editor; Dick Gundlach, communications; Jerry

Lyman, packaging and production; Margaret Maas, industrial; Andy Santoni, instrumentation; and Jerry Walker, consumer.

The long-awaited expansion of citizens' band is going to have to be awaited a while longer yet. Presented with new evidence that the planned upping of allocations to about 50 channels from the present 23 will bring on an unwanted level of intermodulation interference between channels in the new range, the Federal Communications Commission has called for more studies of the proposed expansion.

In his Probing the News article on the new snag, Dick Gundlach, communications editor, says, "The crux of the problem, is this: any two channels operating in the proposed expansion, separated by either 450 or 460 kilohertz, would mix in the receiver front end. They would generate intermodulation products that would be passed by the extremely wide 455-kHz intermediate frequency section used on most CB sets. This signal would effectively blank out reception across the entire band."

So turn to page 37 for the details on this latest development in the citizens' radio saga and what it means to set makers and users alike. And, if you missed it, be sure to read the special report in the March 4 issue for all the background on where CB stands today.



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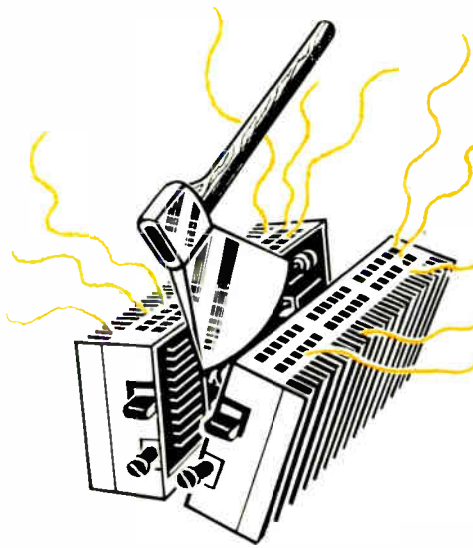
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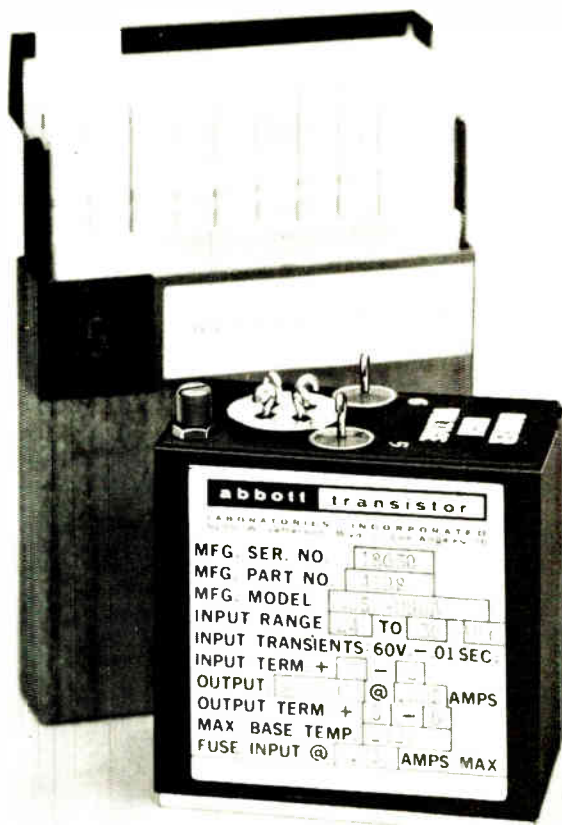


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Readers' comments

Shun big-brother tinkering

To the Editor: An editorial in the Feb. 5 issue [p. 13] says that the Federal budget priorities are out of balance. You end with a true statement concerning the strength of national security ultimately resting upon the health of the society that it protects. The rest of your argument is entirely specious, however.

The health of our society has been constantly undermined by the Federal Government's spending money that does not exist. You seem to advocate more of the big-brother tinkering with the market, wherein lies the gravest danger to the nation's health.

National defense happens to be one of the very few things that government can do better than any one else. It isn't necessarily done too well, but the Government's level of competence goes down precipitously when it moves into other areas.

H. W. Holland
Union Carbide Corp.
Greenville, S. C.

Get off that bandwagon

To the Editor: The proposal to control the number of engineers graduating from the nation's universities ["Professional activities split IEEE," Feb. 19, p. 86] is an example of a wheel-less bandwagon.

Colleges are now chartered, accredited, and, in most cases, aided by the state. The heads of engineering departments run them like little Roman empires and are trying to improve cash flow and keep cost per student reasonable by accepting the maximum number of students. Anyone who thinks politicians in the 50 states and hundreds of department heads are going to let the IEEE run their empires and control the number of graduates probably was born yesterday.

At the Federal level, there are people who constantly are saying that the Russians are going to get ahead of the U.S. because they graduate more engineers than we do. So the Feds would be against any reduction in the number of engineering graduates.

Finally, the antitrust people cer-

abbott transistor

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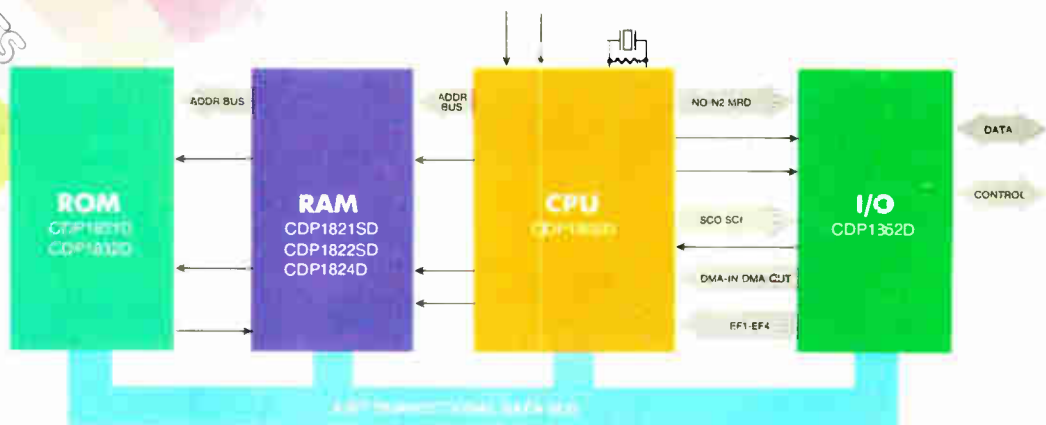
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Readers' comments

tainly will take a dim view of any attempt to control the number of engineers, since the professions no longer are exempt from the antitrust laws.

Willie Handzuik
Philadelphia, Pa.

But will it make an impact?

To the Editor: Milton Alpern has taken another step toward stable careers and professionalism for engineers ["Manpower predictions draw fire," March 4, p. 76]. It was heartening to see some hard data on the engineer-employment problem.

The fact that it took one professional engineering society a year and a half to comprehend such convincing data is evidence for the depth of establishment entrenchment on these matters.

Anthony M. Marqués
Cambridge, Mass.

Value received is the key

To the Editor: It is true that some middle-aged engineers earn high salaries for design work that can be performed equally well by junior engineers earning 50% to 60% as much. However, it also is true that some middle-aged engineers are able to perform the work in less than half the time expended by their juniors.

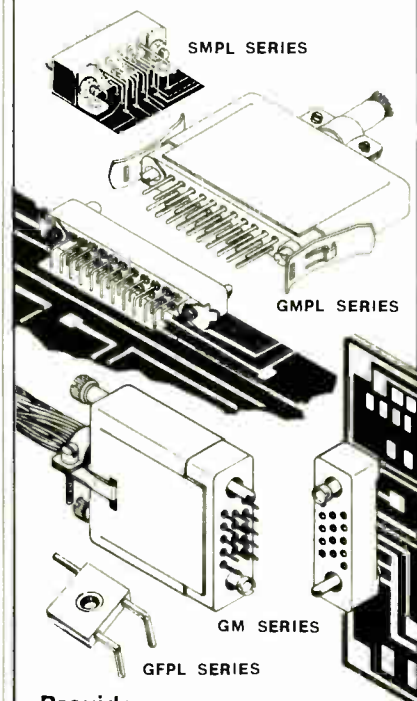
The greatest value that can be placed on the middle-aged engineer is his potential breadth of engineering skills, which so often goes unrecognized by management. A fundamentally sound systems approach can save hundreds of thousands of dollars in the overall cost of a program. It is more likely to come from the experienced engineer.

(Name withheld)

Correction

The description by Stephen W. Fields of National Semiconductor Corp. of the manner in which pseudo-color home video games create their color [March 4, p. 48] was given inadvertently as a description of the operation of National's new MM57100 chip that generates specific color signals for such games.

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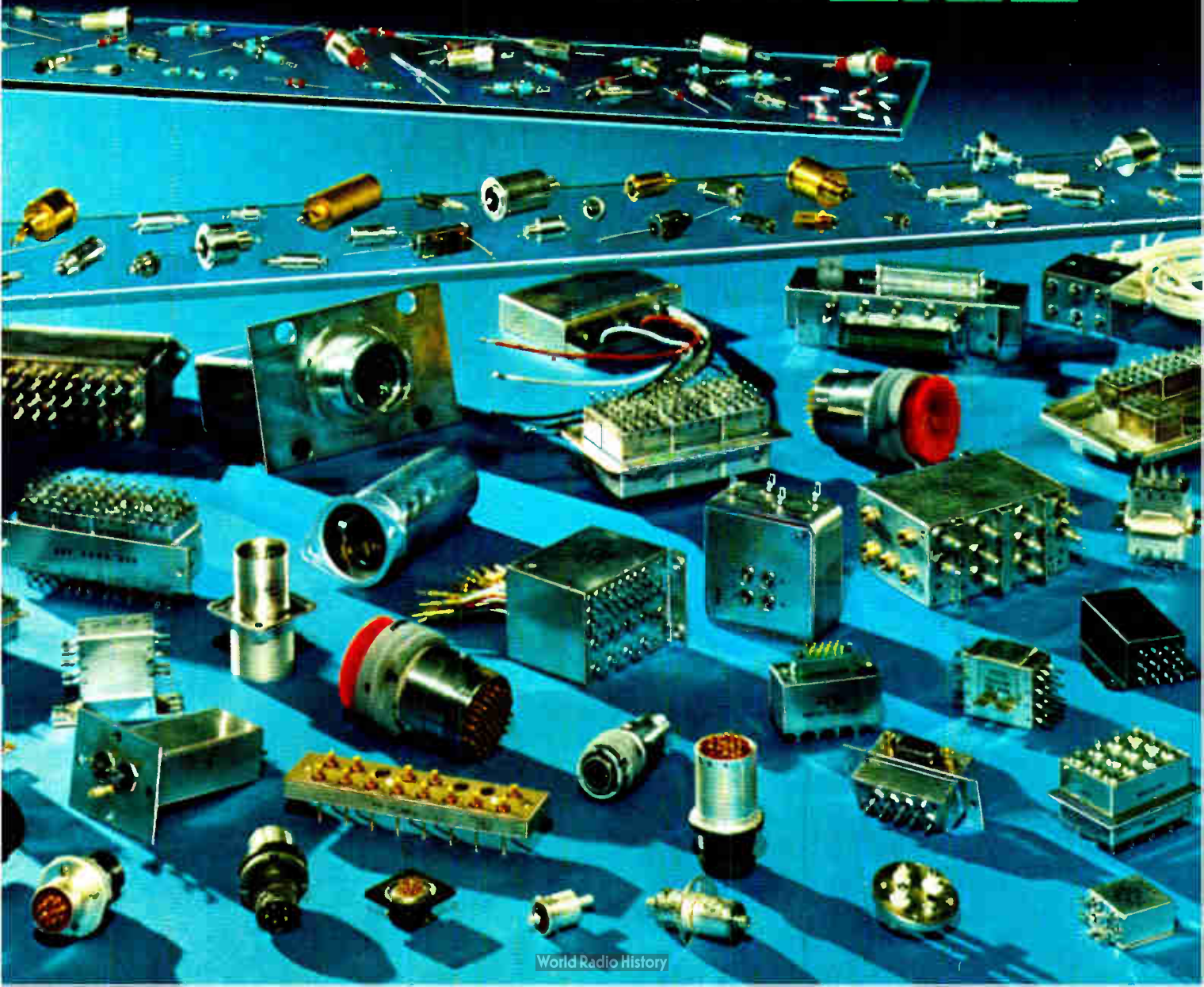
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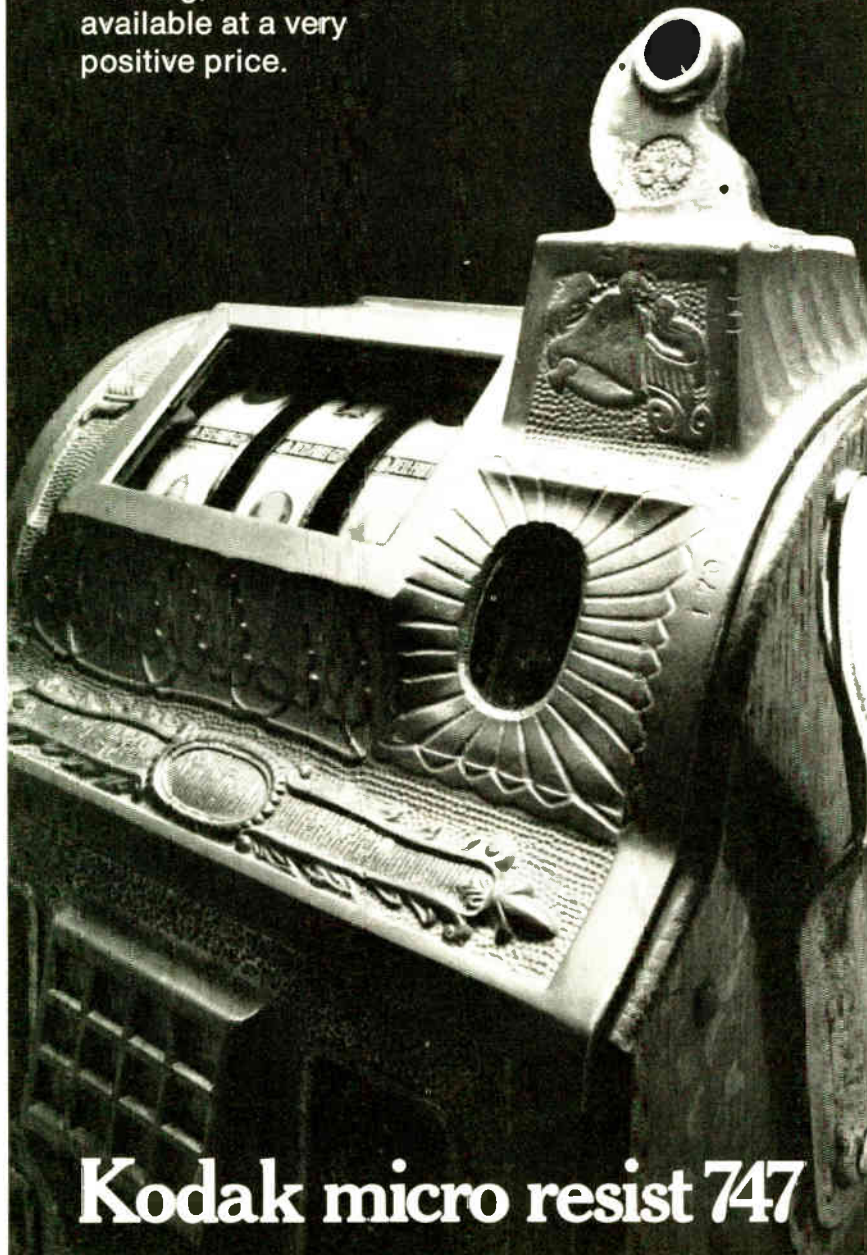
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RESULTS COUNT



Kodak micro resist 747

News update

■ While it is reluctant to name customers, Motorola Inc.'s Communications division says it's pleased with the market acceptance enjoyed by its Spectratrac [*Electronics*, May 15, 1975, p. 35]. A digital receiver system, Spectratrac is designed to help two-way mobile radio systems such as those used by city police cope with high-speed digital transmission. Basically, it's an upgraded total area coverage system. Spectratrac is now in use, for example, by the Fort Worth, Texas, police. There, the department has installed a 12-site, six-channel uhf system for county-wide coverage. Motorola has also added new features to Spectratrac. These include a secondary line driver for subcomparator applications, and line priority for console takeover of the transmitter in emergencies.

The system's key feature is a central station's selection of the strongest signal from several receivers scattered around the coverage area. A sort of analog voting system is used, but Spectratrac uses digital techniques to speed by a factor of 25 the selection of the receiver to be monitored.

■ When RCA Corp.'s Solid State division developed its tri-metal process to eliminate moisture-produced corrosion in integrated circuits packaged in plastic, the scheme had a limited application. It was used originally to create a hermetic-type seal on linear bipolar chips in low-cost plastic dual in-line packages [*Electronics*, May 1, 1975, p. 29]. But now RCA has received a \$1.4 million contract from the Naval Electronics Command to extend the technique to a wide range of IC types. Among them are transistor-transistor logic, complementary MOS, low-power Schottky TTL, and two bipolar devices. Under the contract terms, the failure-rate goal is specified as 0.005% per 1,000 hours of operation, one of the most stringent requirements yet proposed by the Defense Department for ICs in plastic DIPs. Another goal: create the new ICs at a minimal cost increase over tri-metal (gold-chip) devices.

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People

MCI's Wright says AT&T
doesn't own long distance

The case coming up next month before the Federal Communications Commission is a "make or break" situation for MCI Telecommunications Corp., contends V. Orville Wright, president and chief operating officer of the specialized common carrier. He joined the firm, the very first of the new breed of common carriers, a year ago, and has been struggling to keep the company alive ever since.

Service the question. At issue is whether MCI should be allowed to continue its year-old Execunet service, which provides businesses with long-distance communications over shared, rather than dedicated, lines in the firm's microwave net and local telephone-company loops. It wants to provide the voice-and-data service between 16 major U.S. cities.

Aim of the service is to broaden MCI's customer base by attracting the smaller company that can't afford its own dedicated lines. But American Telephone & Telegraph Co. maintains that is illegal. Oral arguments on May 10 are expected to be followed by an FCC decision by midsummer at the earliest.

Wright, with a 26-year career behind him at IBM Corp., RCA Corp., and Xerox Corp., disagrees with AT&T, of course. He argues emphatically that the commission has "never granted a message toll-service monopoly to Bell" like the one it holds over local-area telephone business. And he welcomes, albeit with some trepidation, a precise delineation from the FCC of where AT&T's monopoly service begins and ends.

Seeing red. His apprehension stems from MCI's financial condition: it's still in the red. Despite monthly revenues of \$4.5 million, it needs another \$500,000 a month to turn profitable. Execunet, at this point, brings in less than \$6,000 monthly, but Wright says the market for data switching—now a mere 7% compared to voice transmissions—is expanding rapidly.



Hopeful. A favorable FCC decision is just what Orville Wright of MCI is hoping for.

So for him, the service is critical. It will help the company break even in another four to six months, he says. Otherwise, the loss of Execunet could be the last straw, he concedes, eventually breaking the corporation's back.

Ex-Navy captain to direct
product coding in Europe

In an industry of experts, the new chairman of Pro Electron in Europe, says, "I am not an expert, and I don't need to be." In fact, Willem Goossens, who has 29 years of experience in the Dutch navy and five years with NATO, was brought to Pro Electron primarily because his work with communications and electronics has been independent of the industry. The former navy captain's first civilian job requires him to be as impartial as possible.

Headquartered in Brussels, Pro Electron is a nonprofit association of

Codifier. Uniform component codes is the goal of Pro Electron's Goossens.



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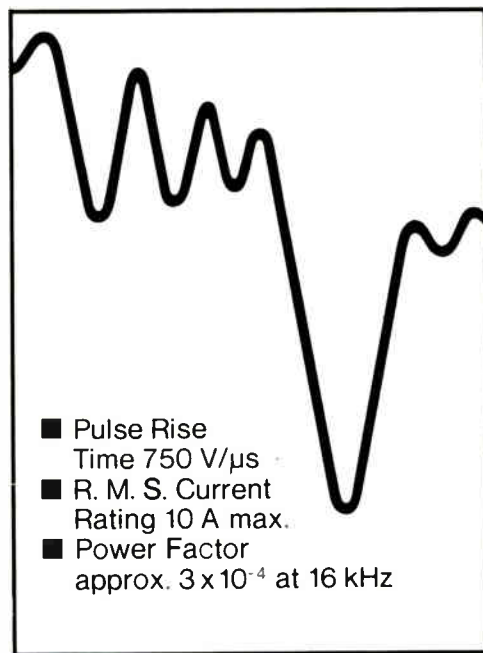
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People

33 components manufacturers in the Organisation for Economic Cooperation and Development. It categorizes active components.

Since it was organized in late 1966, Pro Electron has registered nearly 14,000 products. Goossens thinks that its strongest achievement is the codification of integrated circuits, started in 1967. The Joint Electron Device Engineering Council (Jedec) in the U.S. is currently adopting a product code for ICs based on the Pro Electron model. "We have experience, and our system works," Goossens boasts.

Full agenda. Assuming his post on April 1, Goossens already has a full slate of plans for the future. His next step will be to expand into microprocessors and liquid crystals. The codes are ready and have been waiting for some time for manufacturers' approval.

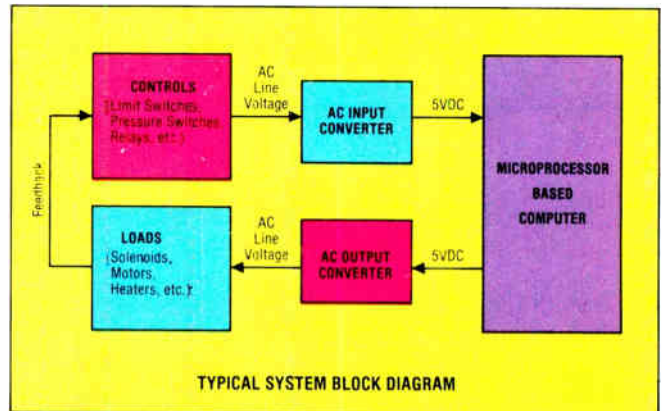
To ensure the effectiveness of a uniform European code, Goossens is pressing for approval before the new products in these rapidly developing sectors become known under individual manufacturers' numbers.

He emphasizes that Pro Electron will remain purely a type-designation agency. "Standardization is not a purpose of Pro Electron," he says, "It is a commercial consequence."

Because new codes are developed only for significant product changes or improvements, Goossens hopes that this system will prevent the proliferation of products which differ only in minor details. Another aim is to increase sales of the Pro Electron indexes. However, Goossens insists that sales are not his primary concern. "I am marketing an idea, not a product," he says.

Cooperation sought. Soft-spoken and unassuming, the 54-year-old Goossens does not view competition as a factor between Pro Electron and Jedec, with which, in the future, he hopes to exchange more information. Ideally, he would like to see one worldwide system. "Realistically, it would be difficult to fuse Pro Electron and Jedec," he says, "But we have in fact the same market. It is to everyone's advantage to have a unified codification system."

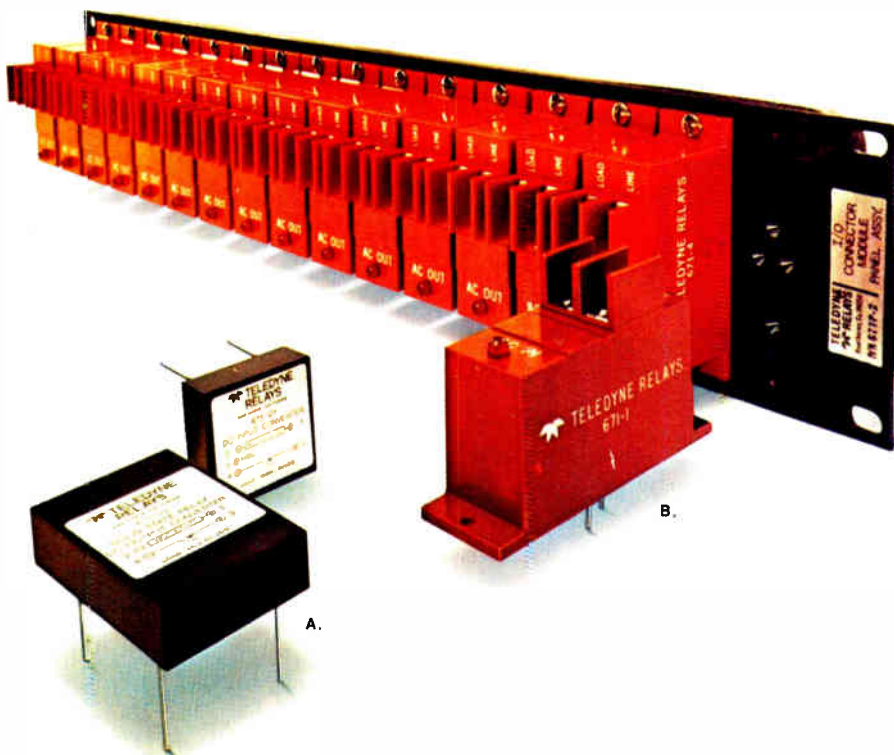
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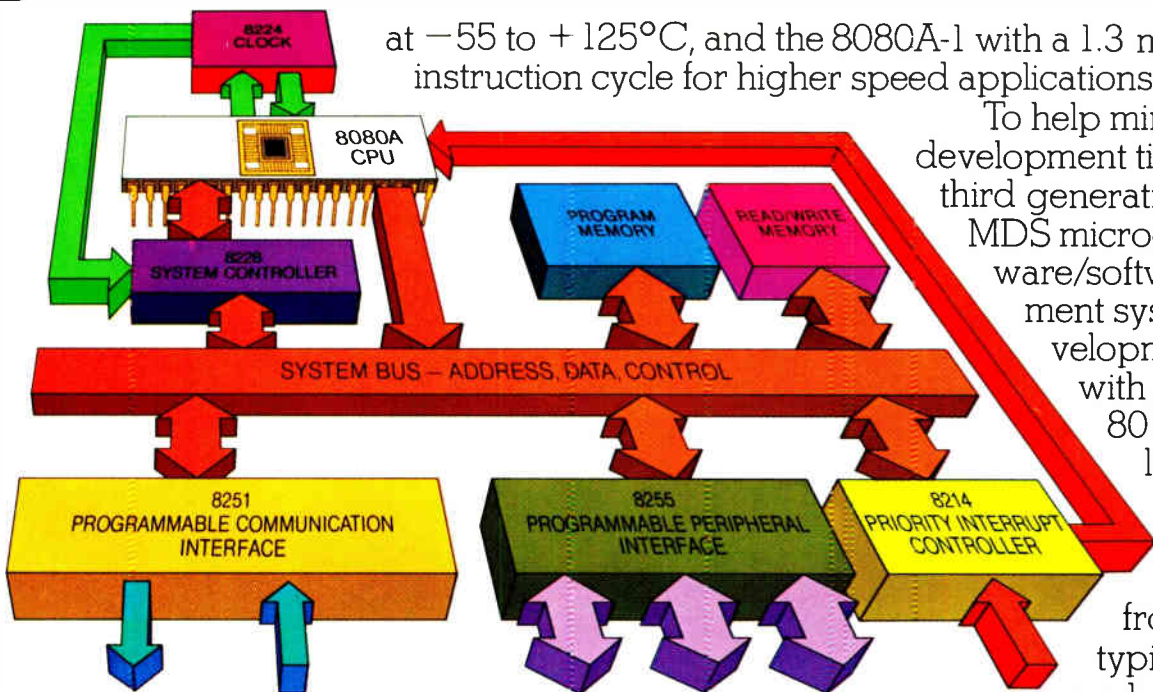
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	8228	System Controller
CPU OPTIONS	8080A-1	1.3μs cycle
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I/O	8212	8-bit I/O Port (15 mA drive)
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PERIPHERALS	8205	1 out of 8 Binary Decoder
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RAMs	5101	256 x 4 Static CMOS, 650 ns
	8101A-4	256 x 4 Static, 450 ns
	8102A-6	1K x 1 Static, 650 ns
	8102A-4	1K x 1 Static, 450 ns
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Electronic Components Conference, IEEE, Jack Tar Hotel, San Francisco, April 26-28.

Offshore Technology Conference, IEEE, Astrohall, Houston, Texas, May 3-6.

Carnahan Conference on Crime Countermeasures, IEEE, University of Kentucky, Lexington, May 5-7.

Industrial and Commercial Power Systems Conference, IEEE, Hyatt Regency Hotel, Los Angeles, May 10-13.

Electro 76—IEEE International Convention, IEEE, Hynes Auditorium and Sheraton-Boston Hotel, Boston, May 11-14.

National Workshop on Low-cost Polycrystalline Silicon Solar Cells, National Science Foundation and Energy Research & Development Administration, Southern Methodist University, Dallas, May 18-19.

Naecon Aerospace and Electronics Conference, IEEE, Dayton Convention Center, Dayton, Ohio, May 18-20.

Eighteenth Israel Annual Conference on Aviation and Astronautics, Technion—Israel Institute of Technology, Haifa, Israel, May 19-20.

Third International Euromation Exhibition—Instrumentation and Automation in Industry, Belgian Institute of Automatic Control, Brussels International Fair, May 22-26.

Conference on Lasers and Electro-Optical Systems, IEEE, Town and Country Hotel, San Diego, May 25-26.

Semicon West '76, Semiconductor Equipment & Materials Institute (c/o Golden Gate Enterprises, Santa Clara, Calif.), San Mateo County Fairgrounds, Calif. May 25-27.

International Symposium on Multi-valued Logic, IEEE, Utah State University, Logan, Utah, May 25-28.

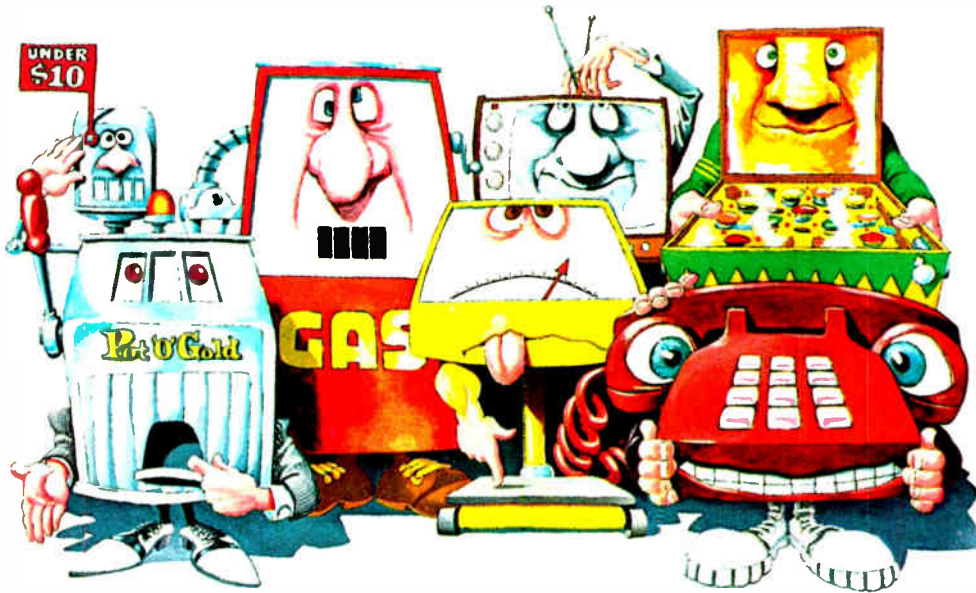
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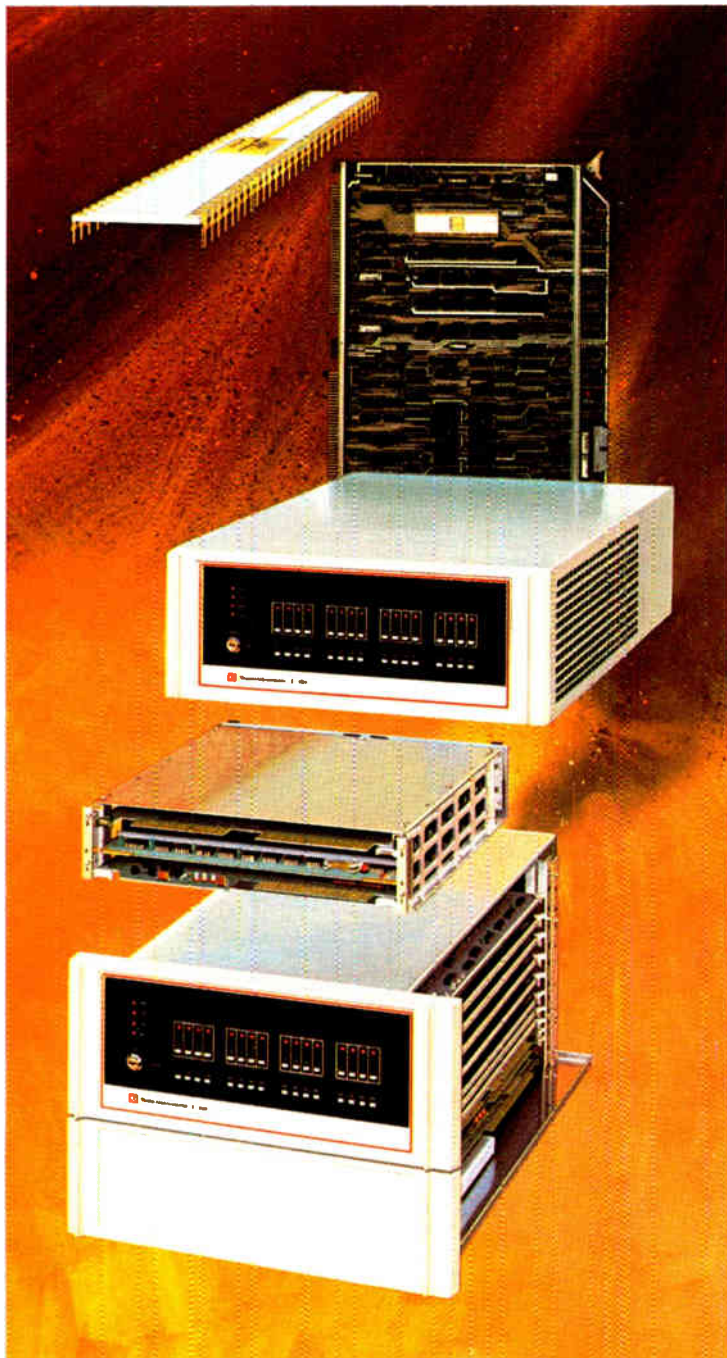
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The reign of the PMOS UART is over.

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Hughes Aircraft might find time ripe to go public

Along with other questions raised by the death of Howard Hughes, one concerns the future of Hughes Aircraft Co., whose \$1 billion yearly sales are almost wholly made up of electronic systems and equipment. Some observers think the timing could be right for the company, owned entirely by the Hughes Medical Foundation, to go public. The late billionaire was the sole director of the foundation.

In the past, rumors circulated from time to time that his representatives had talked with Wall Street investment bankers about a public stock offering. But nothing ever happened, largely because of Howard Hughes' other legal troubles or bad timing in the market. Some observers also think that **the company has all the elements to become glamour-type stock**, since interest has picked up lately in electronics shares.

There also may be tax implications working in favor of such a course, since the foundation might have to divest itself of the company, in much the way the Ford Foundation had to sell Ford Motor Co. stock in the 1950s.

Walkie-talkie frequencies get shifted upward

In an effort to reduce interference for the licensed citizens' band operator, **the FCC has shifted upward the operating frequencies of 100-milliwatt walkie-talkies**. These and some other low-power devices—all called "part 15" devices—will move to five frequencies from 49.82 to 49.90 megahertz. However, operation of non-voice equipment such as automatic vehicle locators and telemetry transceivers will still be permitted to continue in the 27-MHz citizens' band.

In essence, the new rules are: all manufacturing of part 15 devices for operation at 27 MHz must be stopped by March 18, 1977; a year later, dealers may no longer sell such devices; and after March 18, 1983, these devices may no longer be used. The mandated move to a higher frequency band will require re-engineering, which is bound to increase the price of the transceivers.

TI to unveil power linears

Texas Instruments' renewed efforts in analog control products (see p. 33) also are benefiting from work on power linear devices. By the end of April, the Dallas firm expects to announce **a monolithic switching voltage regulator in a 14-pin dual in-line package**, boasting efficiencies of 60% to 80%. The device contains all the necessary components on a single bipolar chip, including power switch, duty-cycle oscillator, commutating diode, error amplifiers, and short-circuit sense. To be priced at less than \$2 in large quantities, the part will offer 0.4% typical load regulation and 0.2% line regulation.

Signetics emulates 8080A in bipolar

Signetics Corp. has started production of a bipolar version of the popular 8080A microcomputer system. Using Intel's 3000 series of Schottky-TTL microprocessor-slice chips, which Signetics now second-sources, the company will offer its 80E emulator. **The 80E will be two to 12 times faster than equivalent 8080A systems**, claims Frank Brunot, in charge of marketing bipolar microprocessors.

Although the high end of the 8080 market isn't large—Brunot puts it

at 5% of the total 8-bit market—it nevertheless allows 8080 designers to use the same software in the 80E emulation to implement minicomputer-type data-processing equipment. As for costs, it takes 30 to 40 80E chips to emulate a typical 10-to-20-chip 8080A system.

Little study shows foreign advantage shrinking

A new forecast by Arthur D. Little Inc. recommends that U.S. electronics companies compare the costs of manufacturing their products in the U.S. with costs overseas. **Those costs will tend to merge by 1980, Little says.** The study covers 15 countries and 18 product categories. The multi-client study by the Cambridge, Mass., research firm shows, for example, that the cost of manufacturing a 19-inch portable color-television set in the U.S. in 1980 will be \$329 and \$324 in Japan, compared with \$265 and \$230, respectively, in 1975.

The same shrinking differential is apparent in a comparison for mini-computers made in the two countries. By 1980, Little estimates, it will cost \$2,085 to manufacture a small minicomputer in the U.S. that will cost \$1,905 to build in Japan. The 1975 figures are estimated at \$2,275 and \$1,875, respectively, for the two countries.

The study, entitled "The Worldwide Cost of Manufacturing Electronic Products, 1975-1980," was sponsored by 13 multinational corporations. Subscribers receive from ADL a computer program and data base that allows them to simulate the manufacturing costs for their own products.

Army seeks improved version of remote sensors

The Army Electronics Command at Fort Monmouth, N.J., has requested quotations to develop design plans for the basic remotely monitored battlefield sensor system (Rembass), a family of unattended ground-surveillance and target-acquisition sensors with associated data-communications equipment.

Portable collector of solar energy to be marketed

A hand-held solar-energy collector and converter **to power portable radios and calculators** will be marketed for about \$30 by late summer. The unit, built by M7 International of Arlington Heights, Va., will use a non-imaging solar-radiation collector, called a compound parabolic concentrator, developed by University of Chicago physicist Roland Winston. Use of the collector, which delivers 0.25 watt, will reduce by 70% the number of silicon cells needed, says M7.

Last \$1.5 million awarded for chart automation

The \$25 million program by the National Oceanic and Atmospheric Administration to automate production of U.S. nautical charts is **nearing reality with the mid-April award for the system's final link.** Information Science Corp., the McLean, Va., subsidiary of Planning Research Corp., got \$1,496,422 to prepare an automated digital-information process that will store and retrieve nautical-chart data. From that data, NOAA cartographers can photograph new charts from computer-generated graphics. The system, to become fully operational in 1980, will speed production of new chart negatives to four to six weeks, in contrast to the six to nine months now required.



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San Jose, CA	May 11, 12, 13
Minneapolis, MN	May 11, 12, 13
Pittsburgh, PA	May 18, 19, 20
Phoenix, AZ	May 17, 18, 19 (20/21)
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Phoenix, AZ	June 15, 16, 17
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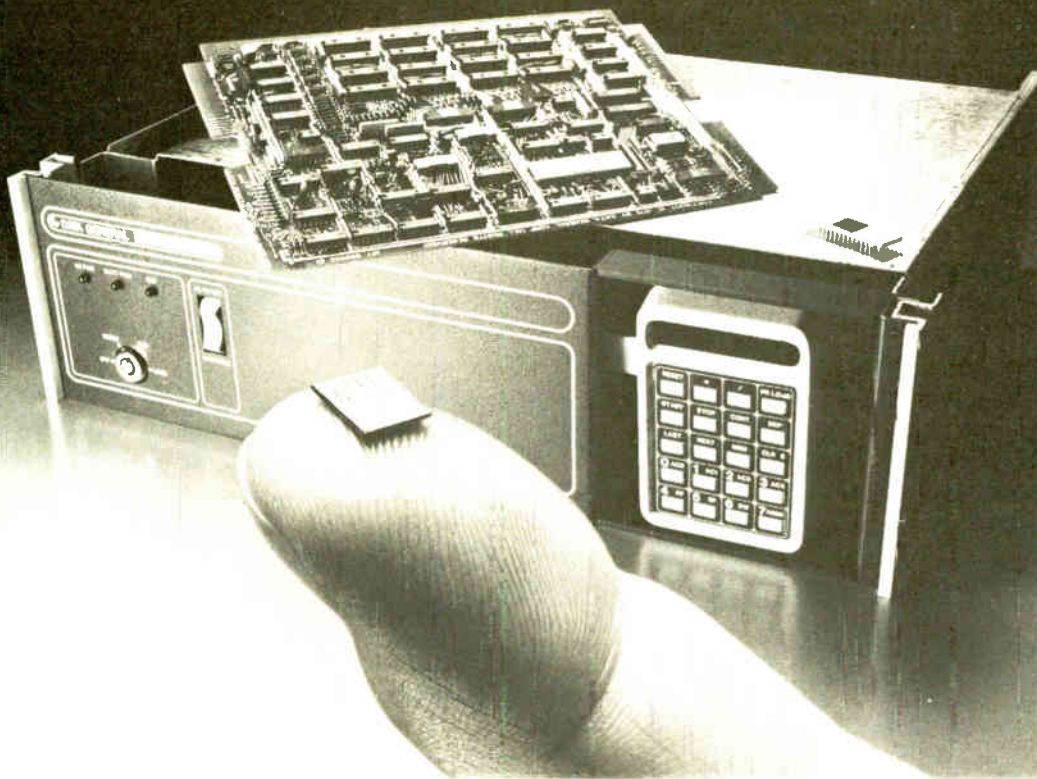
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Reels of film automate watch module assembly

Sprocketed film will carry everything but the battery in production scheme of International Micro Industries

Mounting integrated-circuit chips on reels of sprocketed film is a well established means of automating the assembly of electronic systems. But a company in Cherry Hill, N.J., is not stopping at simple chips. Rather, International Micro Industries Inc. is bonding a complete watch module that includes IC logic, discrete components, and a light-emitting-diode display on either side of each frame of a special 35-millimeter film tape.

The new process could save manufacturers \$1 to \$3 in material per watch module, claims company president Tom Angelucci. In addition, labor costs would be cut by as much as 75%. A line of 10 to 15 machines for the new process, capable of producing 500 modules per hour, would take up an area of 5,000 square feet and require 10 people, Angelucci continues. He contrasts this production to present methods using manual wire bonding and hand assembly that would require some 40 persons to turn out the same number of modules.

Angelucci's company is finishing the design of 12 automated-assembly machines that are designed for this process.

He intends to license the concept, and is currently negotiating, he says, with two major electronic-watch manufacturers. But although he has shown his development to

Electronics, he declines to make any photographs or drawings available for publication.

Film as substrate. Referring to the usual way of dealing with IC chips mounted on film carriers [*Electronics*, Dec. 25, 1975, p. 61], Angelucci points out that "the chips and their copper interconnect leads are cut out of the [film] tape and applied to either ceramic or printed-circuit substrates."

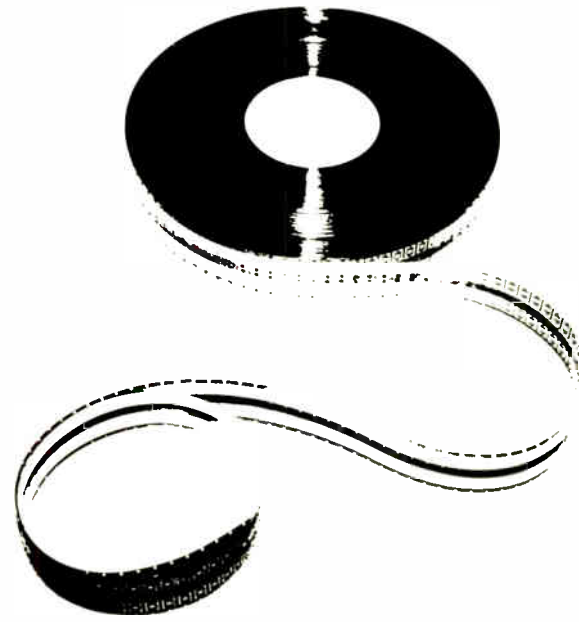
Angelucci, however, takes a short cut. "We omit the step of cutting the ICs from the film tape," he explains. "The film itself is the substrate. But to make it work, we had to come up with a multilayer tape."

Designers at International Micro, heretofore a manufacturer of the polyimide and polyester carrier tapes and custom-assembly equipment, decided that the component density of a typical digital-watch module required a tape with one conductive layer of copper on each side of the insulating film. This arrangement would avoid the complexity of a single-conductive-layer tape with conductive crossovers.

Also, rather than using plated-through holes between the two layers, the designers came up with what Angelucci describes only as a proprietary and novel method that doesn't involve plated-through holes or wire-bonding.

On a production line, the empty tape would move through machines to gang-bond the logic chip and attach the other circuit components (crystal, trimmer capacitor, resistors) to either one side or the other of each 1.4-in.-by-0.7-in. frame of the 35-mm tape.

Each digit of the seven-segment



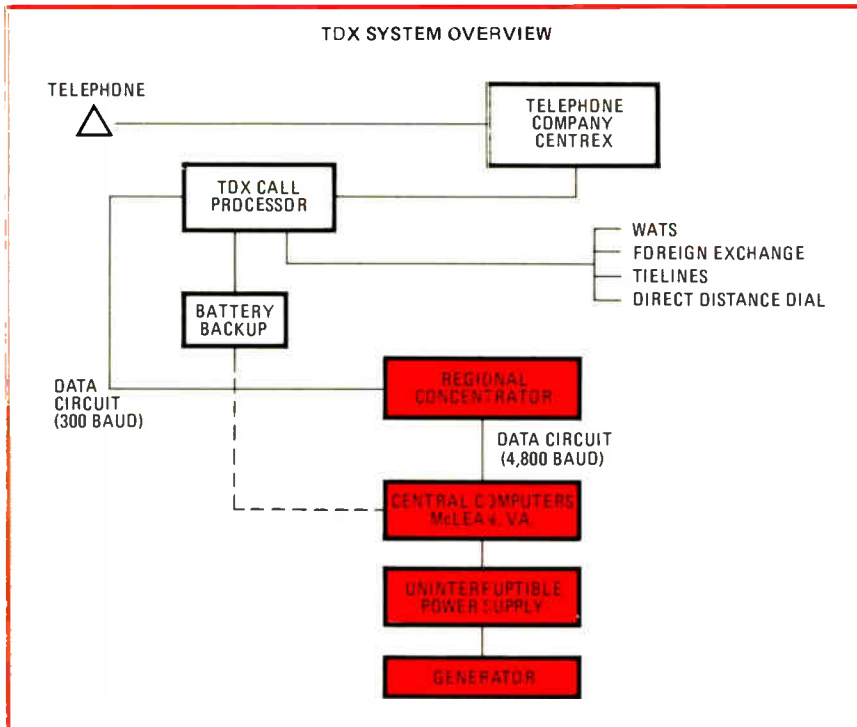
LED displays would be gang-bonded to a 0.3-by-0.2-in. frame of specially designed 8-mm tape. This tape also has conductive layers on both sides, but all LED pinouts are on one side. A multiframe strip of this LED tape is then pressed to conductive pads on the top of the main 35-mm film substrate. When the two-tape assembly is put into a watch case, the LED tape would be held by pressure against its "mother" tape, eliminating any bonding or soldering of the display to the watch tape. □

Communications

Small on-site unit manages phone lines

Computer-controlled telephone-management systems aren't new. But a new company, TDX Systems Inc., is offering the service by remote control. In doing so, it is cutting the customer's capital-equipment investment to zero.

"What we've done is broken off the 'big computer' part of the usual [telephone-management] installation, together with its disk and tape drives, and put it in our own offices in McLean, Va.," explains TDX president William von Meister. The customer is left with a relatively simple microcomputer-driven call proces-



Phone manager. Relatively low-cost microcomputer-driven call processor on the customer's premises controls data flow regarding calls to TDX Systems' shared central computers. Decision regarding the least-cost path over which to route phone calls is made in McLean, Va.

processor that controls the communications lines. This unit, in turn, is connected to the company's central computers via a single 300-baud phone line.

Sharing. "Our approach allows the high capital cost normally associated with stand-alone computer systems to be invested in central computers and, therefore, shared by many users," von Meister says. Without this approach, the investment at a customer's facility may range upward from \$250,000 to \$1 million. TDX's central site, built around a redundant pair of Interdata Inc. model 732 computers, can be shared among as many as 500 users, he says.

Reduction in telephone-company charges—from 10% to 40% for organizations with long-distance telephone bills of at least \$5,000 a month—is the big plus for using his telephone-management system, he points out. Long-distance charges are cut because the system automatically routes all calls over the least-cost path, taking into account the customer's mix of WATS, foreign

exchange, tie, and direct-distance-dial lines.

And besides cutting monthly phone bills, the system also does such things as simplify billing and accounting within the company, and reduce phone abuse by unauthorized callers, von Meister adds. Eight to 32 special-rate outside lines plus the phone company's direct-distance-dial lines can be accessed from a single five-to-six-foot-high rack of equipment that processes the calls.

The microcomputer-driven equipment consists of tone-key decoders, automatic dialers, and 8,000 words of random-access and programable read-only memory that attaches to a PBX or Centrex telephone system at the user's premises. It's built around an Intel Corp. 8080 8-bit microprocessor, with the programable ROMs storing the programs for such things as checking account numbers, and controlling the data flow.

The central computer is a 32-bit machine with 1 million bytes of core memory. Communicating through a concentrator at a 300-baud rate with

the customer's installation, as shown in the drawing, the central site keeps track of the phone lines at each customer location, always picking the cheapest line available.

A monthly charge of \$350 to \$900 covers rental of the call processor and data-circuit costs, as well as accounting and line-usage reports. Additional fees are incurred as a call goes out on the system.

Competition. Ed McAteer, president of Action Communications Systems Inc. of Dallas, which sells and leases stand-alone computer-controlled voice-communications control and monitoring systems, admits that TDX may cut into Action's and others' markets—but only with smaller users, those with long-distance telephone bills of \$12,000 a month or less.

McAteer also points out that because the price charged for the rival system is based on its use, his company's system will be competitive in many low-end situations. "But we don't see TDX making a dent in the bulk of our business, which is users with long-distance billing of about \$40,000 a month or more." □

Microprocessors

Intel 8080 proves highly reliable

Probably the first data on microprocessor reliability is coming from Intel Corp., Santa Clara, Calif., on the reliability of its model 8080 device, an early, widely popular microprocessor. And the findings are impressive, says Kenneth McKensie, microprocessor applications manager at Intel.

Fabricated with n-channel silicon-gate metal-oxide semiconductor technology, the 8080 is a general-purpose 8-bit parallel central processor for computer and control applications. Of the first approximately 100,000 devices shipped, McKensie says, about 32,100,000 hours of operation have been accumulated with only eight field failures. This works out to a failure rate

of 0.04% per 1,000 hours at the 90% confidence level.

In addition to monitoring field failures, Intel has been conducting its own reliability study of the 8080. And the results of the in-house system life tests correlate with the analysis of field failure, notes McKensie. At the 90% confidence level, the company's tests establish a failure rate of 0.064% per 1,000 hours when the devices are operated at 70°C.

Like all components, MOS microprocessors have some unique failure mechanisms, as well as ones in common with other semiconductors, points out McKensie. The report cites faulty diffusions and other causes such as oxide, metalization, and package defects for 8080 failures. Copies of Intel's reliability report will be available from the company, possibly this month. □

Consumer

Digitally compressed voice patters amiably

Most people can understand words faster than they can be spoken. To bring speech closer to the speed of thought—without adding the objectionable “Donald Duck” distortion—a Waltham, Mass., company, Lexicon Inc., has developed a “pitch-control microcomputer.”

The device, which changes the rate of speech without changing its pitch, is the first product on the market to use digital techniques, says president Ronald Noonan. Other playback controls for taped speech [*Electronics*, Aug. 22, 1974, p. 87] have been analog systems (“Analog approach is also viable,” p. 32).

Being sold to audio-equipment manufacturers as a \$100 circuit-board module (in quantities of 3,000 per year), the computer could be applied in playing back educational and training recordings and in sound-film editing.

But it can also slow speech down. Its 5:1 speed swing is between one-half and two-and-one-half times the original speed. So Lexicon thinks it

could also be used to help decipher the excited voices that make emergency phone calls to the police and turn up on crash recorders of downed aircraft.

Sampled waveform. Basically, the pitch-control microcomputer compresses or expands speech by sampling the waveform on the tape at a 16-kilohertz rate when the tape is running at normal speed. However,

the tape's speed is controllable by the user, and the sampling rate increases or decreases in step with the tape.

In addition, the microcomputer includes a special “intelligent-splicing” algorithm, which digitally reconstructs the analog voice waveform without any of the audio “pops” or splice noise found in other kinds of approaches to analog

RCA developing laser/disk recorder for broadcasters

RCA Corp. has demonstrated a high-density video-disk recording technique that uses a laser to store up to 10,000 television pictures or 20 minutes of viewing on a single coated 12-inch disk. The developmental system can store one frame in only 0.003 square inch, whereas today's standard broadcast video recorders require 300 times as much room—1 square inch of magnetic tape for each frame.

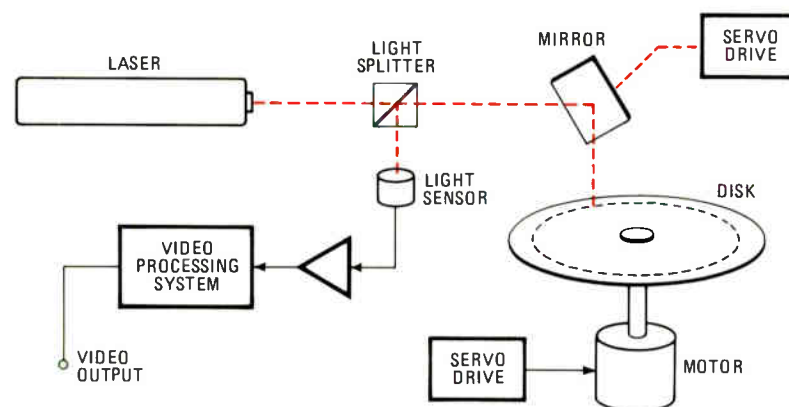
RCA only demonstrated its equipment's capability to record and play back still pictures. But the technology, the company says, could be used to record scenes from TV film chains, cameras, and video tape recorders.

The lasers emit less than 10 milliwatts. An electro-optic modulator focuses the beam on a tiny spot on the disk, which spins at 1,800 revolutions per minute. The disk has a proprietary thin-film coating, which,

when hit by the laser beam, permanently records a single TV frame in one revolution.

Arch Luther, chief engineer for RCA's Commercial Communications Systems division in Camden, N.J., says the system, shown recently to commercial broadcasters, is similar in concept to the videodisk player designed by Philips and MCA Inc., for consumer use. However, the RCA system, designed for professional broadcasting, both records and plays back. In the play-back mode, the RCA unit operates two lasers simultaneously; while one is decoding a picture for “on the air” playback, the other searches for the next.

Luther says RCA has no immediate plans for producing the unit. The company's own SelectaVision video-disk system for home use uses a capacitance-pickup technology rather than lasers.



Analog approach is also viable

Cambridge Research and Development Group, Westport, Conn., has developed its analog speech compression/expansion system, which it calls Variable Speech Control for applications similar to those at which Lexicon is aiming. Kenneth Sherman, a general partner at Cambridge Research, concedes that Lexicon's digital technique has the advantage that, once speech is digitized, it can be processed less expensively than analog signals. But without the analog-to-digital and digital-to-analog conversions required in a digital system, he says, his company can offer a less expensive solution that doesn't degrade speech quality, as he claims digitizing does.

To add compression and expansion to a tape recorder with the Cambridge Research approach adds only \$26 worth of components in addition to the recorder cost, Sherman asserts. To get compression only, which he says is what most users want, the added cost with the firm's technique is about \$15 in components. Cambridge Research does not manufacture systems as Lexicon does; rather, it licenses makers of audio and audio-visual equipment interested in speech control.

speech compression and expansion.

Sampled and digitized data is stored in a 4,096-bit random-access memory. But although the rate at which data enters memory is a function of tape speed, data always emerges at the basic 16-kHz center frequency, ensuring that the pitch stays unchanged. The tape neither quacks when speeded up nor growls when slowed down.

During compression, the RAM overflows when digitized data goes into it at faster than recorded speed, causing some data to be discarded. However, the splicing algorithm has been looking for likely splice points in the input data. And it's been storing the last-discerned splice point in a temporary address register in the microprocessor.

In addition, what vice president Charles L. Bagnaschi calls an "early-warning system" is also looking for likely splice points in real time during data output. This system warns the microprocessor when an overflow point is approaching, and the microprocessor responds by looking for the splice point stored in its temporary register. This point is pulled into an output register and is digitally spliced to the last data coming out of the RAM. In this way, Lexicon avoids splice noise in the voice output.

Similar techniques are used in speech expansion, with data pulled from the RAM faster than it is put in.

Lexicon first introduced the pitch-control system last December in its Varispeech II system, a stand-alone unit that includes a tape deck, amplifiers, and speakers. The microprocessor is a silicon-gate n-channel metal-oxide semiconductor from Standard Microsystems Inc., Hauppauge, N.Y.

The complete pitch-control microcomputer, including a 4-k RAM and 8-bit digital-to-analog converter, fits on the single printed-circuit board. □

Military

Tankers set fuze after shell is fired

Fuzing specialists at the Army's Picatinny Arsenal in Dover, N. J., are developing a technique for increasing the accuracy and speed of firing air-burst projectiles from a tank. By setting the fuze automatically—after the projectile has been fired—the system enables faster firing by transmitting ranging data after the round is in flight.

The new fuzing technique is in the advanced-development stage. "We're eliminating having to set the fuze before the projectile is loaded into a tank's gun," says Henry Hagedorn, project engineer at Picatinny's Ammunition Develop-

ment & Engineering Directorate. "Up to now, the tank commander would see a target, then determine the range. The crew would then have to set the range on the fuze manually, before loading the round."

Automatic range. With the new fuze system, which will be linked to the tank's laser rangefinder and on-board ballistic computer, Hagedorn says a tank commander can ride around with the round already in the gun and aim and fire as soon as a target is spotted.

The fuzing mechanism in the projectile includes an antenna, radio receiver, and low-power complementary metal-oxide-semiconductor timing circuits. Power is supplied, not by batteries, but by a simple generator—a coil of wire within a cylindrical magnet. Inside the coil of wire is a moveable core. When the projectile is fired, inertial forces move the core about one eighth of an inch with respect to the coil, breaking magnetic lines of flux and inducing a voltage in the coil. This voltage is used to charge a tantalum capacitor.

A transmitter and doppler receiver in the tank use the doppler shift caused by the motion of the projectile to start timing the interval until data can be sent to the fuze.

Hagedorn says the best time for transmission is when the projectile is less than 12 feet away from the tank. At that distance, signal attenuation from the hot propelling gases is not excessive, and the distance between the transmitter in the tank and projectile is not too great.

Help from industry. General Electric Co.'s Research and Development Center in Syracuse, N. Y., and GE's Armaments Development Branch in Burlington, Vt., worked with Picatinny on the project, but funding so far has been at a low level. Hagedorn says most of GE's contribution has been in the radio-frequency area. "A study is under way to determine optimum frequency," he says.

The concept has been successfully demonstrated in firings of artillery and rocket fuzes. □

DOD could save on test equipment

Electronic test equipment for the military could cost up to 17% a year less if the Defense Department bought more commercially available instruments instead of those designed to military specifications. That is the judgment of an 18-month study by a Government-industry task force led by instrument maker John M. Fluke, chairman of John Fluke Manufacturing Co.

Excluding automatic test equipment for weapons systems, costs of the test equipment could be cut by at least \$77.9 million annually by implementing the task force's 28 recommendations, says Fluke. Electronic test equipment outlays by DOD ran to \$467 million in fiscal 1975, 35-40% of total U.S. sales, the task force noted.

Breakouts. According to the Fluke report, made to DOD's Defense Science Board, the largest economy—\$17.5 million—could be achieved by using Army Preferred Item Lists in procurements. But the task force argued that use of the lists to limit inventory and support costs "should not . . . limit purchase to a single manufacturer's piece of equipment when similar off-the-shelf equipment is available."

But a recommendation by a minority of the task force, prepared by Ballantine Laboratories Inc. president Fred Katzmann, stressed strongly that the Army lists be used only when items are available from more than one manufacturer.

Further, simplification of procurement procedures would generate an annual Defense saving of \$6.2 million, the task force said. A majority encouraged maximum use of the General Services Administration's supply schedules for off-the-shelf instrument buys, including use of multiple awards. But a minority qualified that view with a call for controls to protect small manufacturers. It urged reduction of the \$250,000 maximum limit on orders placed without public notice to

\$25,000, and recommended that orders for one to five units for which there is more than one supplier be set aside for small business.

Management. The Fluke task force also split on the issue of placing both general-purpose and special-purpose electronic test equipment under a single manager in each service. A minority called this impractical because of the size of the responsibility and the reorganizations this would require. Instead, it urged a manager in each service for general-purpose test gear who would also coordinate special-purpose buys "to maximize use of off-the-shelf" equipment.

Other economies the task force said could be achieved include \$10.5 million by reduced writing of specifications; \$15 million from increased use of "fly-before-buy" testing; \$7 million from use of commercial-parts support; \$8.5 million by consolidating military calibration and repair facilities and more use of manufacturers' resources, and \$9 million by accelerating procedures for replacement of old test equipment. □

Solid state

TI begins drive on analog controls

Texas Instruments has been producing custom camera-control circuits with bipolar and metal-oxide-semiconductor structures on the same chip since last summer. But it's now using what it calls the Bi-MOS process to launch a major push into standard analog-control products.

In a few weeks it will announce a one-chip, chopper-stabilized operational amplifier and a line of analog switches. This summer will see a two-chip, dual-slope analog-to-digital converter, followed by a faster monolithic version. And with an extra ion-implant step putting junction field-effect transistors on the same chip, TI will also introduce a version of the National Semiconductor Corp.'s LF155-series high-

performance Bifet op amp [*Electronics*, Aug. 7, 1975, p. 143] later this month.

Junction isolation. Since conventional junction-isolated substrates are used, both the bipolar MOS and JFET processes lend themselves to the high-volume, low-cost manufacturing techniques at which TI excels. "We process bipolar slices as if we were building conventional op amps," says Tim Smith, manager of linear circuits in Dallas. "But at one point in the process, we open up the oxide between the base diffusions used as source and drain, and use an ion implanter to adjust the threshold of the MOS device."

Three JFET products will replace about 49 other single op amps in the industry, Smith says. By adding the JFET, input electrical characteristics are improved significantly: input bias currents of 30 to 40 picoamperes are typical, compared with earlier parts' 1,000 pA or more.

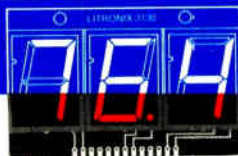
"But the biggest impact of the Bi-MOS process will be for LSI linear functions where we take advantage of bipolar performance in the linear section and the logic densities of p-channel MOS in the digital," Smith says. Initially, TI plans a one-chip successive-approximation converter for data acquisition in microprocessor-based systems and a more accurate two-chip converter for digital panel meters.

Planned for summer introduction, the two-chip 13-bit model will use the TL500 bipolar-MOS analog processor to do dual-slope functions, such as input control and sampling. An integrated-injection-logic and control chip, the TL502, will add such functions as auto zero and auto ranging, as well as display drivers.

Bi-MOS will also be used for a one-chip chopper op amp, the TL089, for high-gain dc applications.

Analog switches. TI has already announced four proprietary bipolar-MOS analog switches, and by May plans eight more monolithic versions, pin-for-pin compatible with Siliconix DG181-series hybrids. Prices in volume will be about 50 cents per switch, compared to \$10 to \$20 for comparable hybrids. □

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Converter price war stays hot



by Lucinda Mattera, Components Editor

Probably the most dreaded of all merchandising modes—the price war—is now raging among makers of thin-film hybrid data converters. And, as in most price wars, only the user will likely be the real winner when the dust settles.

Last September, National Semiconductor Corp., Santa Clara, Calif., started the battle by announcing its first hybrids, an array of low-cost data-conversion products. A couple of weeks later, picking up the gauntlet, Datel Systems Corp., Canton, Mass., launched its hybrid facility with three similarly priced, but higher-performance, devices. (Only this month, Datel has been forced to raise the prices—by 50% or more—of all its hybrid converters and to pull its initial devices off the market.)

In the meantime, Burr-Brown Research Corp., Tucson, Ariz., an established member of the hybrid community, took note of both National's and Datel's low prices—and retaliated, cutting its prices below those of Datel's for similar products. Now, two other "traditional" hybrid manufacturers—Beckman Instruments Corp. of Fullerton, Calif.,

and Micro Networks Corp. of Worcester, Mass.—have joined the lists, both coming out with economy devices meeting Burr-Brown's prices.

The action is swirling about 12-bit digital-to-analog and analog-to-digital converters, and the prices are so low that there is reasonable doubt about profitability. High-performance self-contained d-a units (those that include both a reference and an output amplifier) were costing over \$40 last fall but now sell for as little as \$20 each in 100-lot quantities. Complete a-d devices (those including a comparator, a clock, and a register) that went for more than \$120 are down to less than \$80 each in single-unit lots.

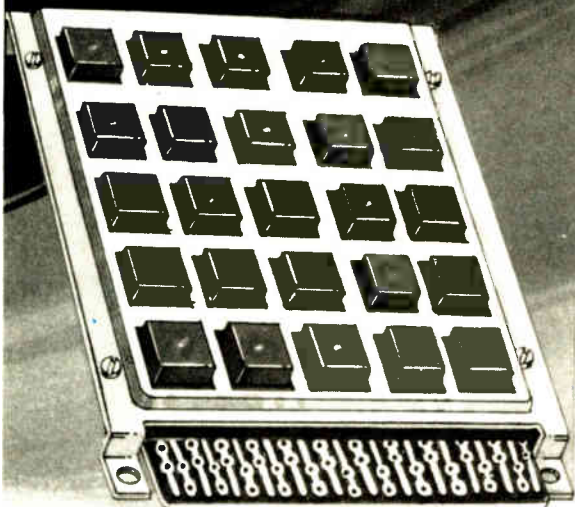
However, self-contained 12-bit converters are fairly complex devices. Usually they incorporate 10 or more semiconductor chips, in addition to thin-film resistor networks and several chip capacitors. The prices of these components, plus overhead expenses, labor, and yield factors, can bring the cost of manufacturing to around \$15 or so for a d-a hybrid and in the vicinity of \$50 to \$60 for an a-d device—leaving a very questionable profit margin.

National, which fired the first shot, is "unequivocally serious about staying in the business," asserts Dean Coleman, converter products marketing manager. The company made its move to get into the market heavily and to stir competition, he says.

More ahead. Coleman believes that prices have nearly bottomed out in hybrids, but further reductions will occur when most converters become monolithic within three years. Hybrids are a means to an end, he says. "Building a seven-chip d-a is crazy." As a result, he predicts, "The guys that are going to be out on top are Analog Devices, National, and Motorola, if they can get their act together," pointing out that all three have a semiconductor capability.

Looking back, Eugene Zuch, Datel's product marketing manager for data conversion products, notes, "We went too low, and I'm surprised at the current stampede at the low end of the price structure." At Burr-Brown, Gene Tobey, marketing manager, observes: "Datel tried to buy a part of the market with price cuts, so we protected our

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market share by doing the same thing."

What will happen to prices? Tobey says, "The tendency is for prices to hold firm and even start to rise a little. I doubt if we'll see any drastic cuts until the new generation of converters comes around, in the neighborhood of a year or so."

To Beckman, which is a major supplier of thick-film hybrids, Burr-Brown seems to be a more important factor than National. In fact, "We haven't seen the impact of National's product deliveries yet," observes Lyle Pitroff, product marketing manager. Over the next 12 to 18 months, he projects, the trend will be to redefine what converter needs really are, come up with simple designs using fewer parts, and plan how to manufacture them with the maximum use of automated production techniques.

Micro Networks has been in thin-film technology for about six years now, specializing in the high-reliability end of the converter market. But in the last few months, it has begun to commit itself heavily to the commercial arena. According to Robert R. Jay, president, the company was more than ready to enter the low-priced thin-film market because it had the technology, as well as the production capability, and its volume lines could achieve the necessary high yields to compete.

Waiting. Sitting on the sidelines for the time being is Analog Devices Inc., Norwood, Mass., which could become a significant factor in pricing. Analog is the only company fabricating some of its thin-film hybrid converters with its own custom-design chips, thereby minimizing parts count. Dubbed "compound monolithic integration," the approach puts the firm in a unique market position because it's not selling the custom chips outside. Jerry Fishman, marketing manager for the Semiconductor division, believes his company has the best competitive edge, but current orders are claiming all the custom chips the facility can produce. However, Fishman already has expansion in the works.

Communications

FCC delays CB expansion

Informed that interference in a 50-channel allocation could kill reception, agency will delay its decision until next January

by Richard Gundlach, Communications Editor

The long-awaited FCC decision to expand class D citizens' band to around 50 10-kilohertz channels from 23 has hit another snag. This has led the Federal Communications Commission to initiate a second inquiry and notice of proposed rule-making to study proposals for frequency reallocation.

The commission has been told that intermodulation interference between certain channel frequencies in the proposed expansion could make transmission on all CB channels useless. This threat heaps more confusion upon a situation already blessed with more than its share.

The crux of the problem is this: any two channels would generate intermodulation products that would be passed by the extremely wide 455-kHz intermediate-frequency section used on most CB sets. This signal would effectively blank out reception across the entire band.

So far, the FCC's three expansion plans are not as simple as merely adding channels to a total of 53. The first is for 105 voice channels using 53 shared a-m and single-sideband 10-kHz channels with 52 additional SSB-only channels interleaved. The second would use the five class C channels and wind up with 115 voice channels—but both these arrangements would be susceptible to intermodulation problems. The latest plan pushes expansion to the limit: add to the number of shared a-m and SSB channels by including the five from class C, then interleave 44 SSB-only channels among the 10-kHz a-m channels. This would theoretically provide 99 voice channels on class D citizens' band.

CB equipment makers ruefully re-

call the commission's March 1975 prediction that it would have a decision in the matter by January 1976; now, FCC chief engineer Raymond Spence forecasts a ruling by January 1977. Many CB makers view that new target with a jaundiced eye. "We need that rule-making this year," says R.E. Horner, president of E.F. Johnson Co. of Waseca, Minn., the largest U.S. CB-set maker. It was Johnson that informed the FCC about the threat of intermodulation interference between frequencies.

Not only are manufacturers and congressmen urging the commission to do something about the extreme

congestion on CB bands, but the White House is also getting into the act. A three-page special message, read to the Electronic Industries Association's first personal-communications conference late last month by John Eger, acting director of the White House Office of Telecommunications Policy, made clear the office's concern with providing for increasing communications needs of mobile America.

No help at 27 MHz. Spence is of the opinion that more 27-MHz channels won't be the answer to a long-term viable CB service, and certainly a mix of a-m and single-sideband channels in that band is equally useless [*Electronics*, March 18, p. 10]. Spence said at a conference session, "Stop thinking about 27 MHz. We have to go into part of the frequency spectrum that doesn't have skip problems [signals that travel over large distances due to reflections from the ionosphere], and that means going to a frequency band greater than 150 MHz. But since there is no spectrum between 27 MHz and almost 1 GHz available for CB use, it means taking spectrum away from other users."

As for use of the 900-MHz spectrum for citizens' band, most manufacturers agree that equipment would be costly and yet have many propagation problems. Steve Mieth, chief engineer of Communication Power Inc., says that "Operating up there would mean reprogramming our phase-locked-loop synthesizer and some circuit redesign, which is no real problem." But mismatch in the antennas would cause all kinds of problems for the CB user, Mieth warns. □

The CB traffic jam

Citizens' band proponents argue that frequency allocation is way out of balance. They point out that 250,000 amateurs use a 42-megahertz chunk of the spectrum up to 450 MHz; on the other hand, 10 million CB users are fighting to squeeze into a 0.25 MHz slice. A recent FCC study found complete congestion on all 23 channels in metropolitan areas such as Chicago, Los Angeles, and New York during peak-use periods. And according to FCC chief engineer Raymond Spence, more of the same channels isn't the answer. The quantum leap in users—the FCC has received over 500,000 license applications per month since January—coupled with increasing sun-spot activity, would compound interference problems, and, by 1979, this could well spell the demise of CB.

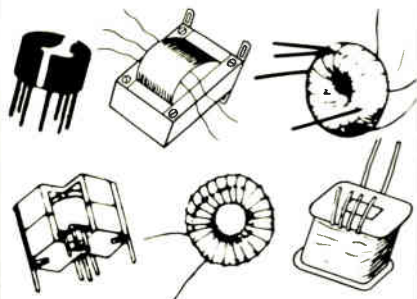


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Trade

Pentagon seeks more control

Asks new export guidelines after Bucy task force says DOD, not Commerce, should set the rules

by Ray Connolly, Washington bureau manager

The Pentagon is trying to expand its control over high-technology electronics exports. Defense officials are developing new guidelines that would virtually halt foreign sales of manufacturing knowledge. At the same time, they would loosen restrictions on exports of relatively unsophisticated commercial products and speed approval of export requests.

The call for new guidelines follows the warning of a Defense Science Board task force headed by Texas Instruments' president J. Fred Bucy that "control of design and

manufacturing knowhow is absolutely vital to the maintenance of U.S. technological superiority."

Although primary authority for export controls rests with the Commerce Department, Bucy says his group believes "the initiative for developing policy objectives and strategies for controlling specific technologies" should be the Defense Department's. But exporters are suspicious because the task force was dominated by representatives from the Pentagon and from defense contractors.

Beyond tighter limits on foreign

EFFECTIVENESS OF TECHNOLOGY TRANSFER						
Transfer effectiveness	Industry				Transfer mechanism	
	Instrumentation	Semiconductor	Jet engine	Airframe		
Highly effective (tight control)	H	H	H	H	Turnkey factories	Active
	H	H	H	H	Licenses with extensive teaching effort	
	H	H	H	H	Joint ventures	
	H	H	H	H	Technical exchange with ongoing contact	
	H	H	H	H	Training in high-technology areas	
Effective	MH	H	M	M	Processing equipment (with knowhow)	Donor activity
	M	H	MH	MH	Engineering documents and technical data	
	M	H	MH	MH	Consulting	
Moderately effective	M	MH	M	M	Licenses (with knowhow)	Passive
	L	L	M	M	Proposals (documented)	
	L	MH	L	L	Processing equipment (without knowhow)	
Low effectiveness (decontrol)	L	LM	L	L	Commercial visits	Passive
	L	L	L	L	Licenses (without knowhow)	
	L	L	L	L	Sale of products (without maintenance and operations data)	
	L	L	L	L	Proposals (undocumented)	
Low effectiveness (decontrol)	L	L	L	L	Commercial literature	Passive
	L	L	L	L	Trade exhibits	

L = Low effectiveness LM = Low to medium effectiveness
M = Medium effectiveness H = High effectiveness
MH = Medium to high effectiveness
Source: Defense Science Board

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sales of design and manufacturing knowledge, the Bucy task force is urging constraints on exports of key manufacturing, inspection, and test equipment, as well as products "accompanied by sophisticated operation, application, or maintenance knowhow."

While calling for faster Federal action on export applications for commercial products, the task force would appear to do the opposite by judging applications on the basis of the product's "intrinsic utility, rather than commercial specifications and statements of intended end-use." Yet the task force is defending that recommendation by noting that specifications and end-use statements on export applications are now assessed for potential military significance, requiring "a tedious case-by-case analysis."

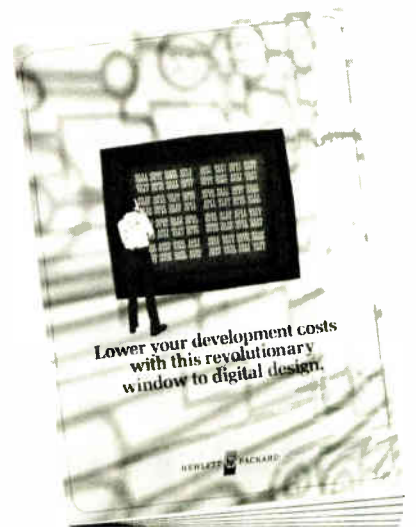
The task force has developed a chart ranking 17 typical technology-transfer mechanisms in descending order of effectiveness and degree of donor activity (see table). "Especially significant," the task force observed, "is the fact the four [technology] subcommittees agreed so closely."

Controversy. The Bucy group neatly sidestepped the controversial issue of high-technology transfer via weapons sales to neutrals or questionable U.S. allies, although it did call for strengthening the network of export controls exercised by Co-Com, the coordinating committee of NATO member countries plus Japan.

Nevertheless, the issue was brought up quickly in Senate hearings by the Computer and Business Equipment Manufacturers Association. CBEMA president Peter F. McCloskey called U.S. computer-export policies inconsistent "when we deny moderately advanced computers to the USSR, Eastern Europe, and the People's Republic of China, and at the same time, export weapons containing highly sophisticated computers to nations whose long-term allegiance to the U.S. is questionable, and where such technology is highly susceptible to uncontrolled leakage to what we term 'hostile nations.'"

Look at the opposite page...

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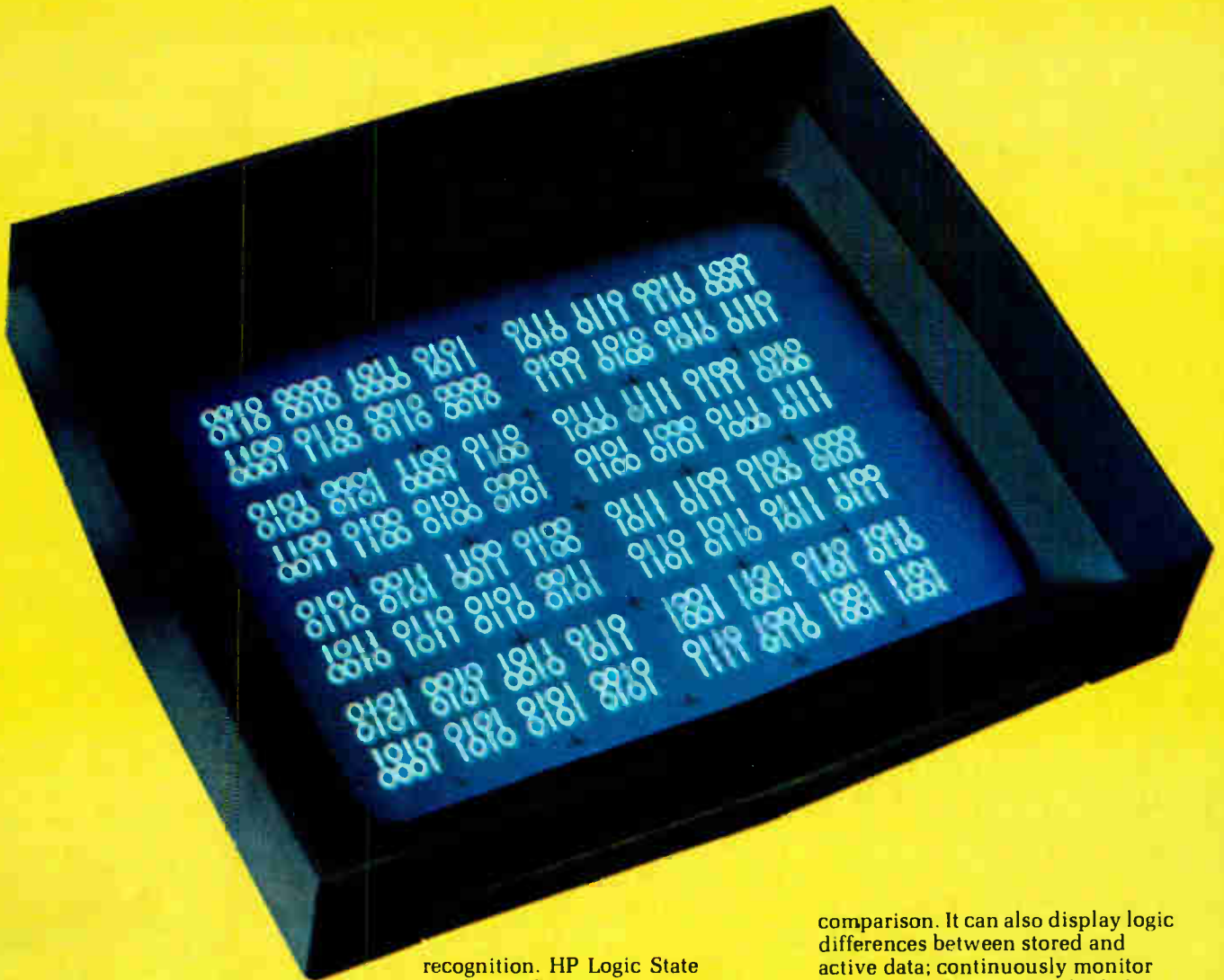
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If you rely primarily on we think you're



Now we're not advocating that you stop using your scope. You've always needed one and you always will. But if a scope is all you're using, you're probably wasting a lot of time. A couple of years of field experience with logic state analyzers has shown us that about 85% of digital troubleshooting problems can be solved faster with a logic state analyzer than with a scope.

Think about it. When you want to observe action on address or data buses, or on control lines, which instruments give you more meaningful data—a scope with four input channels or a logic state analyzer with 12, 16, or 32 channels?

You need a trigger that's related to program steps. Scopes by themselves simply don't have the capability of triggering on pattern

recognition. HP Logic State Analyzers do. Suppose you want to delay the data display to a specific point after the trigger word. The scope's analog time delay system has the inherent problem of display jitter. This is completely eliminated by the stable clock-pulse delay of a logic state analyzer. And when you're viewing data, would you rather mentally convert waveforms to digital words (1's and 0's) or have the instrument do the conversion for you?

Obviously, the scope is the logical choice for electrical measurements such as voltage level, rise time, and timing measurements. But when you're viewing state flow, there's no substitute for a logic state analyzer.

For example, one of HP's Logic State Analyzers can store one table of digital words and display it next to your active word display for

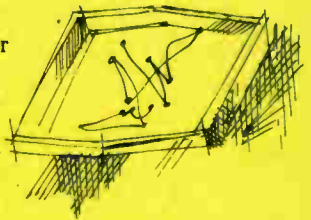
comparison. It can also display logic differences between stored and active data; continuously monitor data flow and automatically halt when the active data does not equal the stored data.

A new technique called mapping gives you an entirely new view of operating logic

circuits—over 65,000 data words can be displayed as discrete dots, each representing one input word.

You can easily recognize these dot patterns after some familiarization, thus providing a rapid way to spot system irregularities. And for locating "lost programs," the map provides unequal speed.

But these aren't just interesting measurement techniques, HP Logic State Analyzers provide more



a scope for digital design. making a mistake.



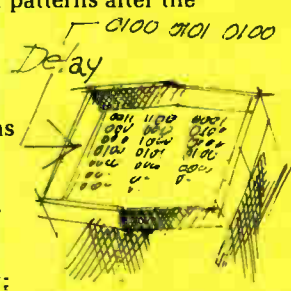
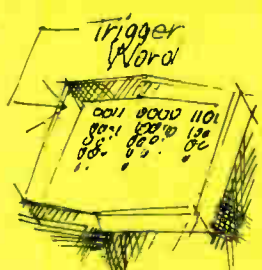
capability than any other digital troubleshooting instrument can deliver.

The Logic State Analyzer is the only economic alternative when it comes to digital system design.

Your digital system operates in the data domain. You know all about time domain and frequency domain measurements, but how do you define data domain measurements? Basically they are measurements of logic state as a function of discrete intervals of time — clock cycles, for example. The emphasis is on word parameters. While the scope gives you an analog display of amplitude vs. time (time-domain dimensions), the logic state analyzer gives you a display of digital words vs. clock cycles.

But what are the other requirements of a data domain instrument? Obviously you need sufficient channels to see what's happening

on address and data buses. With today's systems, that means 16 channels or more. You need data registration — the ability to trigger on a specific bit pattern and the ability to position the display window as a function of clock cycles (pattern recognition triggering and digital delay). Because you often encounter events that occur only once in a program, you need a method of internal storage. Obviously, you want the ability to look at bit patterns after the trigger point, but you also want to see what happens before that point... in other words, you want negative time display; and even the ability to look on both sides of the trigger word at



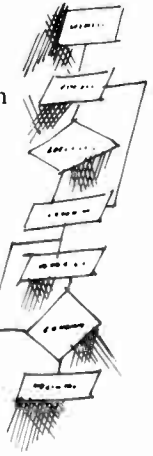
the same time. It's essential that you be able to qualify both the trigger point and the display so you won't trigger on, or display, unwanted data. You'll still need to observe time-domain waveforms on your scope for detailed electrical measurements such as rise times, logic levels, and for locating glitch-generating race conditions. Your data domain instrument should therefore be able to drive a time-domain instrument — providing a trigger upon pattern recognition. Finally, you want data displayed in a functional format (a display of states) to simplify analysis.

From the previous comparison with a scope, you can see that these are the requirements we've used at HP in developing our family of Logic State Analyzers. Obviously, some members of the family have more capability than others, and prices vary accordingly. But the point is, all have been designed specifically to help speed digital design and debugging by giving you a better view of your system's operation. A view in the data domain... where your program flow is happening.

HP's Logic State Analyzers

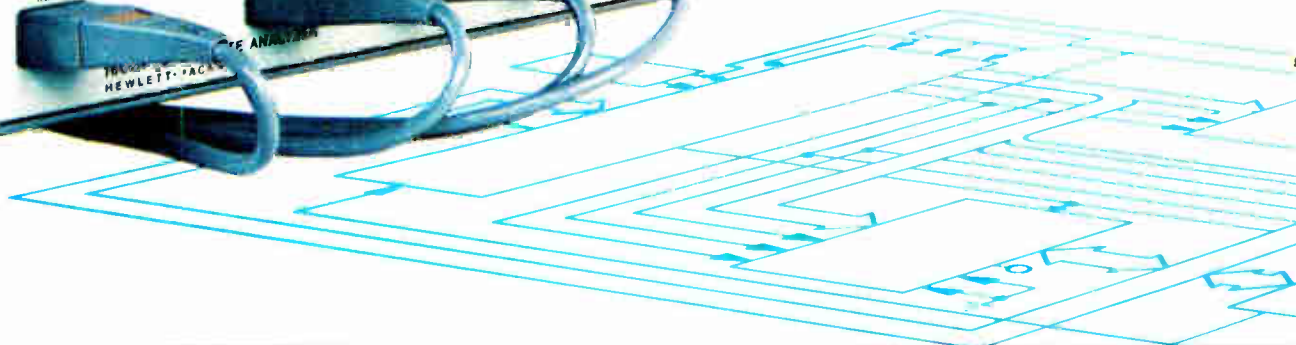
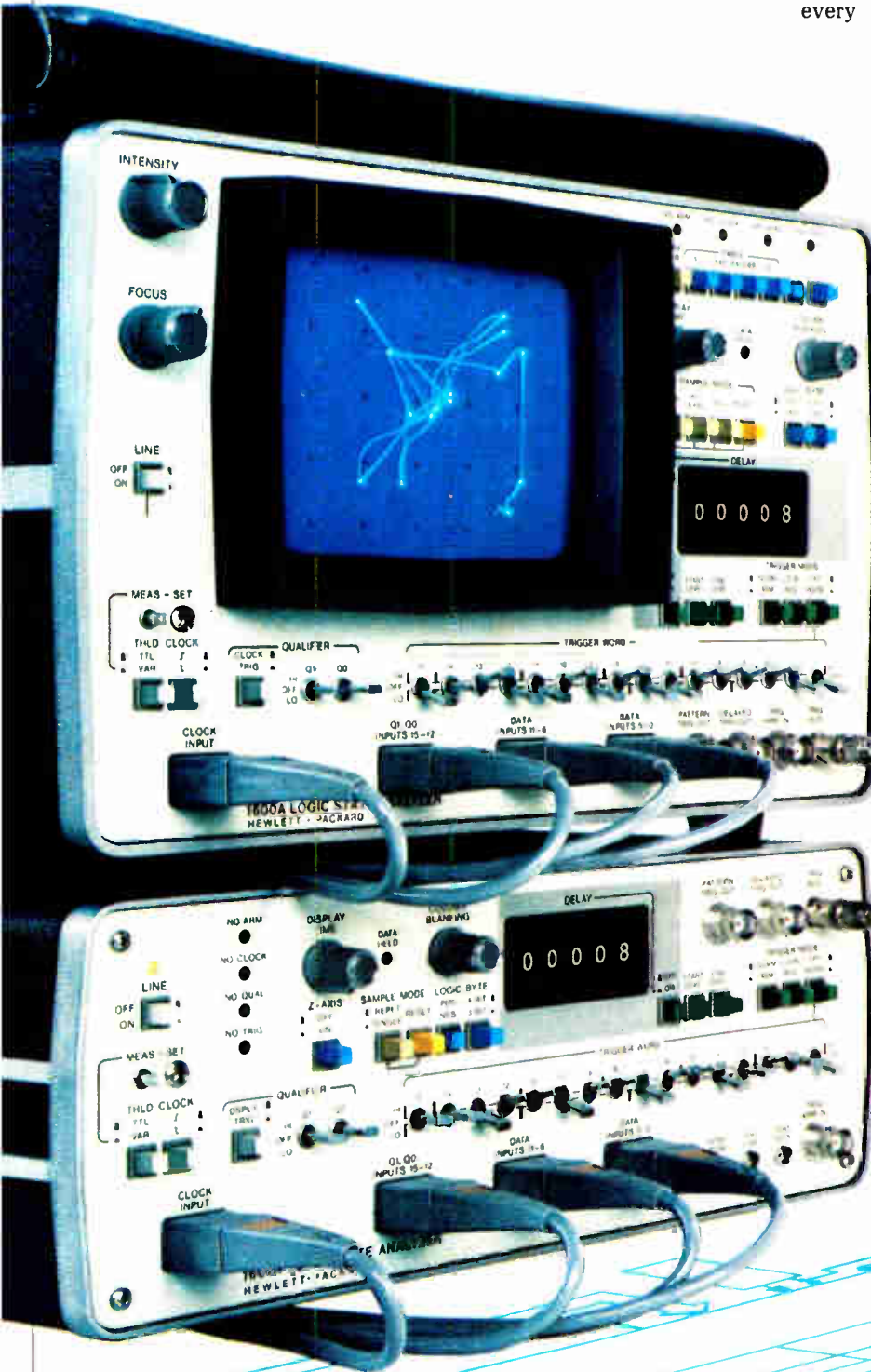
Software debugging. It's great if you write a program that works right the first time it's implemented in hardware. But you know that it doesn't happen every

time. And when you get into program debugging, it's usually a time consuming task. How can an HP Logic State Analyzer help? By putting a window right on the data and address buses and giving you a real-time view of your program in operation... so you can see the exact word flow while it's happening. What's more, HP Logic State Analyzers let you move the window around at will by triggering on any word you want, or delaying the display a specific number of words beyond the trigger word.



This lets you compare the actual addresses and data on the buses with the program instructions you entered. It becomes much easier to spot an erroneous data word, an erroneous jump in the program, or an unending loop. With the mapping capability of the HP Model 1600A Logic State Analyzer, it's a simple matter to compare an executing program pattern to a known good pattern, or spot unique points in the pattern that indicate problems in an executing program.

The 1600A also gives you the ability to locate any word on the map and trigger on that word so you can pinpoint a potential error source quickly. Then you can zero in by



speed digital design.

using the table display (1's and 0's) and digital delay to examine the program sequence in detail.

Watching your software in action ... it gives you a big edge in problem solving.

Hardware/software marriage.

In digital design, you often discover incompatibilities between hardware and software — particularly when separate design teams have responsibility for these two aspects of the system.

It's not uncommon for the software to command the hardware to look for a signal (such as a request for interrupt) that apparently never occurs. Failure to get the signal may be a timing problem — the signal may occur too early or too late. The signal may exist at the right time, but at the wrong place — on the wrong data line for example. Or perhaps the signal was omitted altogether in hardware implementation. With microprocessors, the

problem may be due to lack of understanding of CPU peculiarities.

Whatever the case, you could spend an inordinate amount of time looking for the answer with the channel and triggering limitations of time-domain instrumentation.

However, with an HP Logic State Analyzer, you can tie into both the address and data buses at the same time, plus flag or qualifiers (up to 32 channels can be displayed on one screen). You can then run a short test program, trigger on a specific word at the beginning of the program, and view the program implementation leading up to the problem.

With this detailed picture of software in action, it's a simple matter to observe the displayed program sequence and see what's happening to that signal at a specific point in time. Then it's usually easy to spot the problem and apply a software or hardware solution — whichever is more appropriate.

System interaction. Additional problems frequently show up when you start transferring information across an I/O port. And your troubleshooting problems are compounded because you have two sources of data to monitor at the same time. They may have independent clocks ... be asynchronous ... but require a common trigger signal.

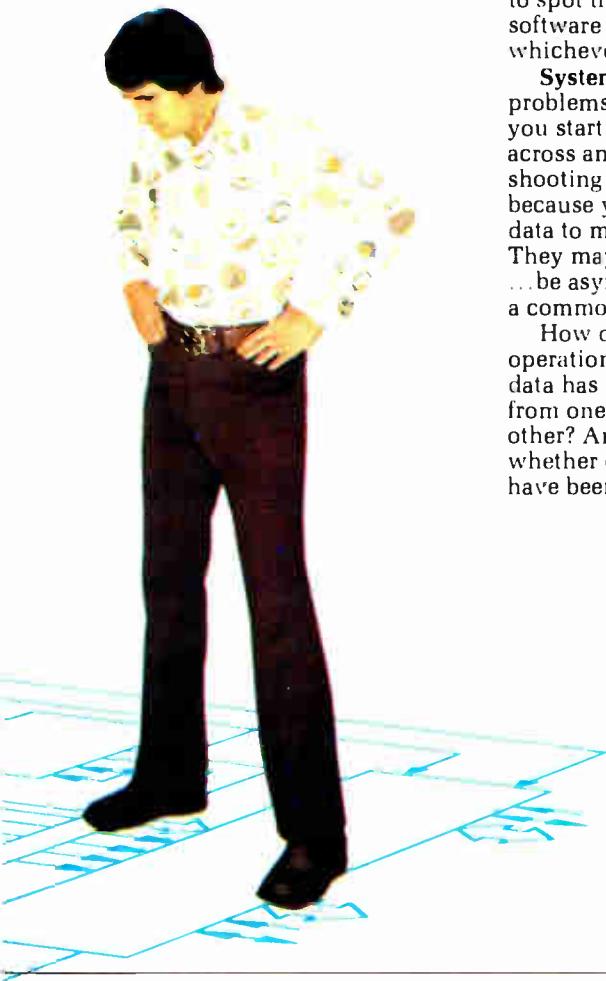
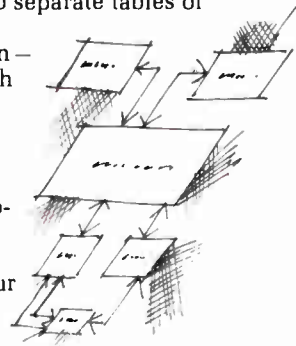
How do you verify overall system operation? How do you find out if data has been properly transferred from one part of the system to the other? And how do you determine whether or not the instructions have been executed properly?

Suppose, for example, you've designed a microcomputer-controlled test system for production. How do you know that the software is giving proper instructions to the instruments under test? Or that the instruments are inputting data correctly to the microcomputer? Unless you can verify the states in your program flow and look at digital inputs and outputs during the test cycle, your test could be meaningless. But with your microcomputer operating at one clock rate and the monitoring instrumentation at some other rate, how do you observe both and relate microcomputer software to hardware output.

The answer is HP's 1600S Logic State Analyzer. It lets you display two separate tables of data on the same screen —

even though clock rates are different or one system is asynchronous. One table can display your microcomputer software sequence while the other displays the hardware output and input resulting from that software. With program flow displayed alongside the input and output states of the instruments being controlled, there's no doubt about a correct testing sequence ... or about the information being fed back to the microcomputer. Furthermore, if there is a fault, you have adequate information to diagnose problems for correction.

In all of these phases of digital design — from the time you input software right through system checkout — an HP Logic State Analyzer can give you a clear view of program flow and hardware logic states to simplify design and debugging.



Pioneers in the data domain are convinced.

Our customers have been using HP Logic State Analyzers since 1973. And we've talked to quite a number of users to find out what designers need in data-domain instrumentation. We've also found out how these data-domain pioneers feel about the HP Logic State Analyzers.

Here's a sampling:

"With the 1600A analyzer, I can do in an hour what I couldn't do in 3 months otherwise, and that's a fact."

"I designed a buffer interface that allows us to make real time tests using a slower tester. With my \$20,000 interface, the \$100,000 tester and your \$4,000 logic analyzer, we can do the job of a \$400,000 real time tester."

Don Glancy,
Principal Engineer

"We encountered some severe software problems on a real time 4K system where we were at a loss as to how to approach the problem. Because it was a real time system we were unable to stop it to use the standard software debug techniques. By coincidence your salesman called on the same day to demonstrate the 1601 Logic Analyzer. We hooked the analyzer to the system under test and wound up solving the problem that same afternoon. We were so thoroughly convinced of the potential power of the 1601 as it applied to software debug that we ended up buying two of them."

"Even though we had limited experience with microprocessor design, there's no question the logic analyzer saved us valuable design time."

Ken Fiske,
Senior Design Engineer



"When a parity error does occur, our equipment re-reads the data block fifteen times. In order to initiate that search routine, many sequential logic events must occur. Problems occasionally arise in that logic flow and it's been very difficult to analyze using just a scope. The logic analyzer allows us to troubleshoot logic flow in parity error problems about twenty times faster than the scope does. In addition to being faster, it's also easier to interpret the 1's and 0's than it is to interpret waveforms."

Don Stewart
*Coordinator of
Service Planning*

You've just read actual testimonials from users who have achieved significant time savings with an HP Logic State Analyzer—savings ranging from a factor of 20 to well over 400 compared to other methods, (Don Glancy's comment, "I can do in an hour what I couldn't do in three months otherwise.") And equipment savings of a factor of 3 or more.

If you or your people spend significant numbers of hours in the development of bus-structured systems such as computers and microprocessor-based systems, consider what those time savings could mean to you:

Convince yourself.

Over and over again, the reports from the field say: time saving... greater productivity... reduced development time... products into production faster. Whether you're a digital designer or an engineering manager, this message is important to you.

As a circuit designer, you know the importance of sticking to development schedules and budgets. And that always means

solving the problems the fastest way you know how. Take a look and see what kind of savings you might realize with an HP Logic State Analyzer.

If you're an engineering manager, concerned with the productivity of your engineering department, consider how much further your engineering budget could go if your people had HP Logic State Analyzers.

(A) — Estimated man hours spent in evaluating and debugging hardware and software using conventional techniques.

= — Your estimated time-saving factor — using a logic state analyzer — based on these testimonials.

= (B) — Estimated time spent in evaluating and debugging hardware and software with a logic state analyzer.

(A)–(B)= — Potential time savings during the project.

× — Your hourly rate including overhead.

= — Potential direct cost savings.

Make your own analysis of what the time savings can mean in terms of getting products into production faster. The figures you come up with might easily exceed the cost of one of our Logic State Analyzers.

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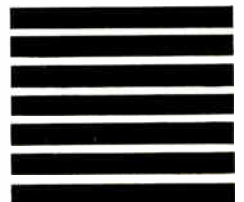
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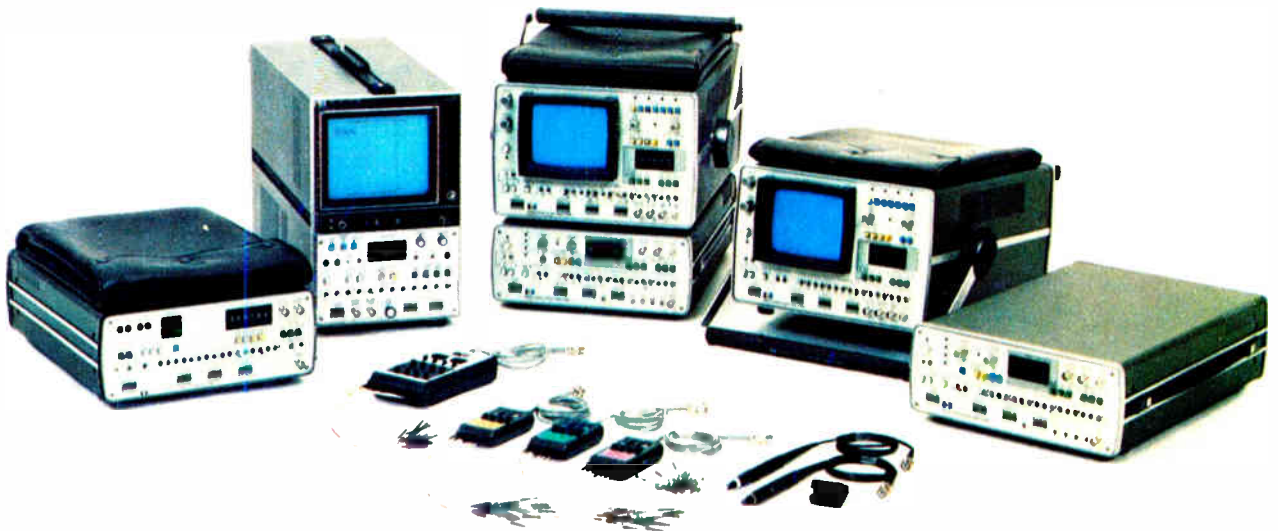
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We've just scratched the surface.

There's a lot more to know about the data domain and about HP's family of instruments. And there are several sources for more information.

Seminars. HP instructors are now conducting one-day seminars on logic state analyzers and their application, and will continue in 1976.

Technical Data Sheets. These publications give you details of operation and instrument specifications on each of the family members.

Application Notes. A number of notes cover the use of mapping, using logic state analyzers to troubleshoot mini computer systems, microprocessor systems, etc.

For more technical data, simply mail the attached reply card, indicating the data sheets you want. Or, for even faster action, contact your local HP field engineer and ask him for more details about the instruments or seminars. Give him a call today and join the data domain revolution.

086/4

I'd like more technical information about HP's family of data-domain instruments. Please send data sheets on:

- Logic State Analyzers
- Pattern Trigger Accessories
- Clips and Probes

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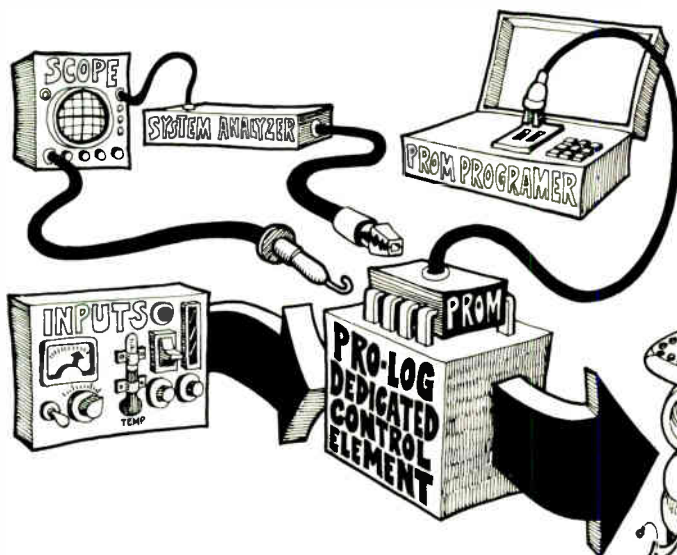
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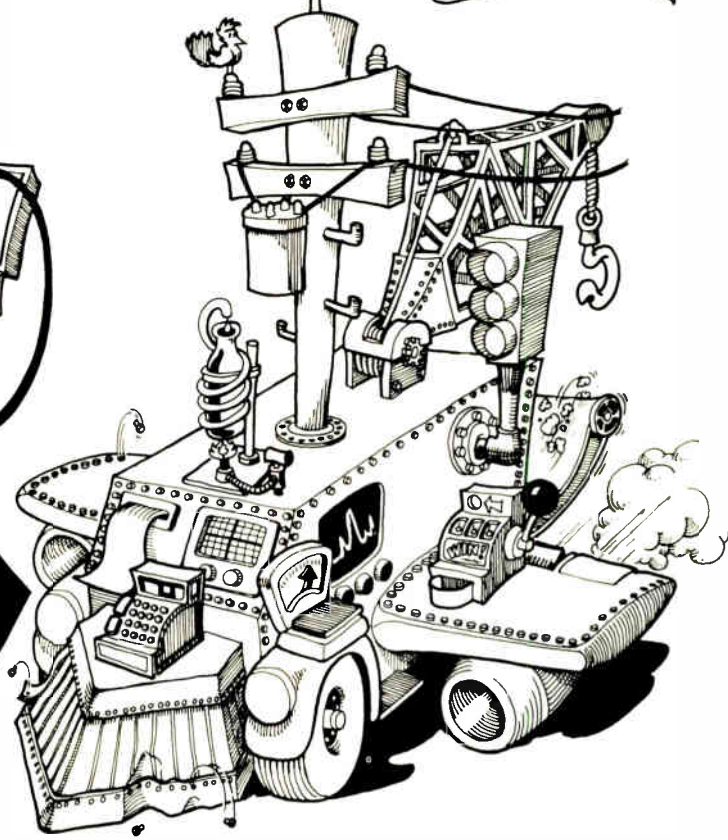
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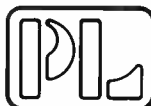
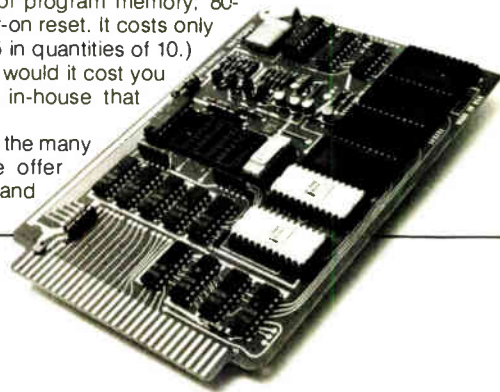
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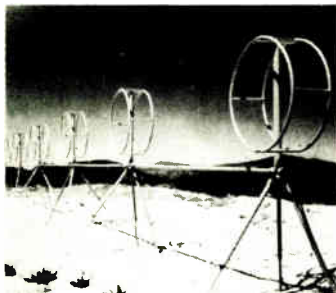
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Washington newsletter

Michigan site for Seafarer to get A for ecology

The National Academy of Sciences is **expected to report favorably on the ecological impact of the Navy's Seafarer** submarine-communications system on the Upper Michigan Peninsula, say sources familiar with the academy's study program. The study of the controversial extremely low-frequency grid, which would maintain worldwide communications with submerged submarines, was undertaken last year at the service's request and will be completed late this summer.

The Michigan site is atop the Laurentian Rock shield, which would minimize earth absorption of the elf signal. The Navy, at the request of the Worldwide Military Command and Control Council (WWMCC), is also considering sites at Nellis Air Force Base, Nev., and in the White Sands-Ft. Bliss, N.M., complex. However, the Navy considers those sites unsatisfactory because of the lack of a rock subsurface, their size, and the cost to locate Seafarer there [*Electronics*, April 1, p. 40].

GSA wants more competition in U.S. telecommunications buys

Suppliers of telecommunications equipment to interconnect with telephone lines and specialized common carriers **will get more opportunities to compete for Federal communications contracts**, says Theodore D. Puckorius, head of the General Services Administration's Automated Data & Telecommunications Service. Puckorius says his office is working on guidelines for competitive GSA telecommunications procurements that will be "practicable and realistic."

More than 15 Federal installations will buy private-branch-exchange hardware under competitive procurements already announced. Puckorius says. However, the scheduled April 19 major award to install "pilot" interconnect equipment for a government installation at Charleston, S. C., has been slipped to June. Puckorius promises equipment makes will be asked for "new and innovative products for specific needs," and that unsolicited proposals to Federal agencies will be evaluated.

Communications reform bills gain support but irk Macdonald . . .

Moves by the nation's telephone companies to get Congress to limit competition by legislation are gaining some support in the Senate and House, but have irked the influential chairman of the House Communications subcommittee, Torbert H. Macdonald (D., Mass.).

Following introduction of the Consumer Communications Reform Act as H.R. 12323 by Rep. Teno Roncalio (D., Wyo.) in March [*Electronics*, March 18, p. 60], two more versions have been introduced: H.R. 12844 by Samuel L. Devine (R., Ohio) and H.R. 12924 by Joe L. Evins (D., Tenn.). Another version of the bill, supported by AT&T, the U.S. Independent Telephone Association, and the Communications Workers of America, has been introduced in the Senate by Vance Hartke (D., Ind.). Wyoming's two senators, Democrat Gale W. McGee and Republican Clifford P. Hansen, will be cosponsors.

Chairman Macdonald sees the legislative plan as one by which the carriers could "legally prohibit anyone other than themselves from competing for the public's business." Nevertheless, the telephone companies were heartened by Macdonald's suggestion that the proposal will get a hearing. "Their proposal, as well as alternatives suggested by myself and others," he said, "will set the stage for a national debate on this important subject."

. . . as FCC's Hinchman sees no threat from competition

New numbers playing down the economic threat to the telephone industry from interconnection and specialized common carriers are being advanced by Walter R. Hinchman, chief of the Federal Communications Commission's Common Carrier Bureau and a long-time advocate of competition.

"Bell's annual increase in revenues for services subject to competition," Hinchman says, "is more than four times the total annual revenues of the specialized carriers and the interconnect industry combined. The fact is that in order to reach the penetration level forecast in one industry-sponsored study, the specialized carrier industry **would have to grow by a factor of 140 over the next decade**, which amounts to a rate of 70% annually, compounded."

Utah site readied for testing of remotely piloted craft . . .

The Air Force will begin operating its **first major technical installation for test and evaluation of remotely piloted vehicles** late this summer in western Utah. The new test range, which combines former facilities of the Army's Dugway Proving Grounds with those of Bill and Wendover Air Force Bases, will ultimately provide restricted air space of 60 by 120 nautical miles. The southern half of the range will begin initial use of the High Accuracy/Multiple Object Tracking System (Hamots) to simultaneously track up to 40 cooperative RPV targets with a maximum error of 5 meters in all three coordinates, the Air Force says.

Also beginning operation will be an improved-gain telemetry auto-track/reacquisition system with full-range coverage in the L and S bands; Loran C/D coverage; and an electromagnetic test system for technical verification and evaluation of airborne electronic countermeasures systems, electromagnetic compatibility and interference, and range frequency management and control. Also, there will be improved full-range C-band tracking-radar coverage, plus a permanent range and mission control center at Hill Air Force Base with 50 telemetry channels and real-time display of RPV space positioning by means of radar and Hamots. Tests are already scheduled at the range for the Teledyne Ryan AQM-34V and the multi-mission BGM-34C, the Tactical Expendable Drone System prototypes of Beech Aircraft and Northrop Corp., and the Compass Cope reconnaissance drones developed by Boeing and Teledyne Ryan.

. . . but high costs plague mini-versions for attack role

Use of miniature remotely piloted vehicles, like the twin-tailed Axillary built by F-Systems Inc.'s Melpar division for tactical harassment missions by the Air Force, is so far proving successful in virtually all areas but one. **"The fly-away unit cost is still a long way from the goal of \$1,000** sought by the Tactical Air Command, says a Defense Advanced Research Project Agency official tracking the effort.

Nevertheless, the Air Force is pushing the R&D effort to define its operational requirements for a small RPV as an all-weather weapon to automatically track and kill armored targets, defensive and missile radars, communications, and other tactical installations. Emphasis is being focused on developing new low-cost sensors for three RPV configurations scheduled to be tested this summer.

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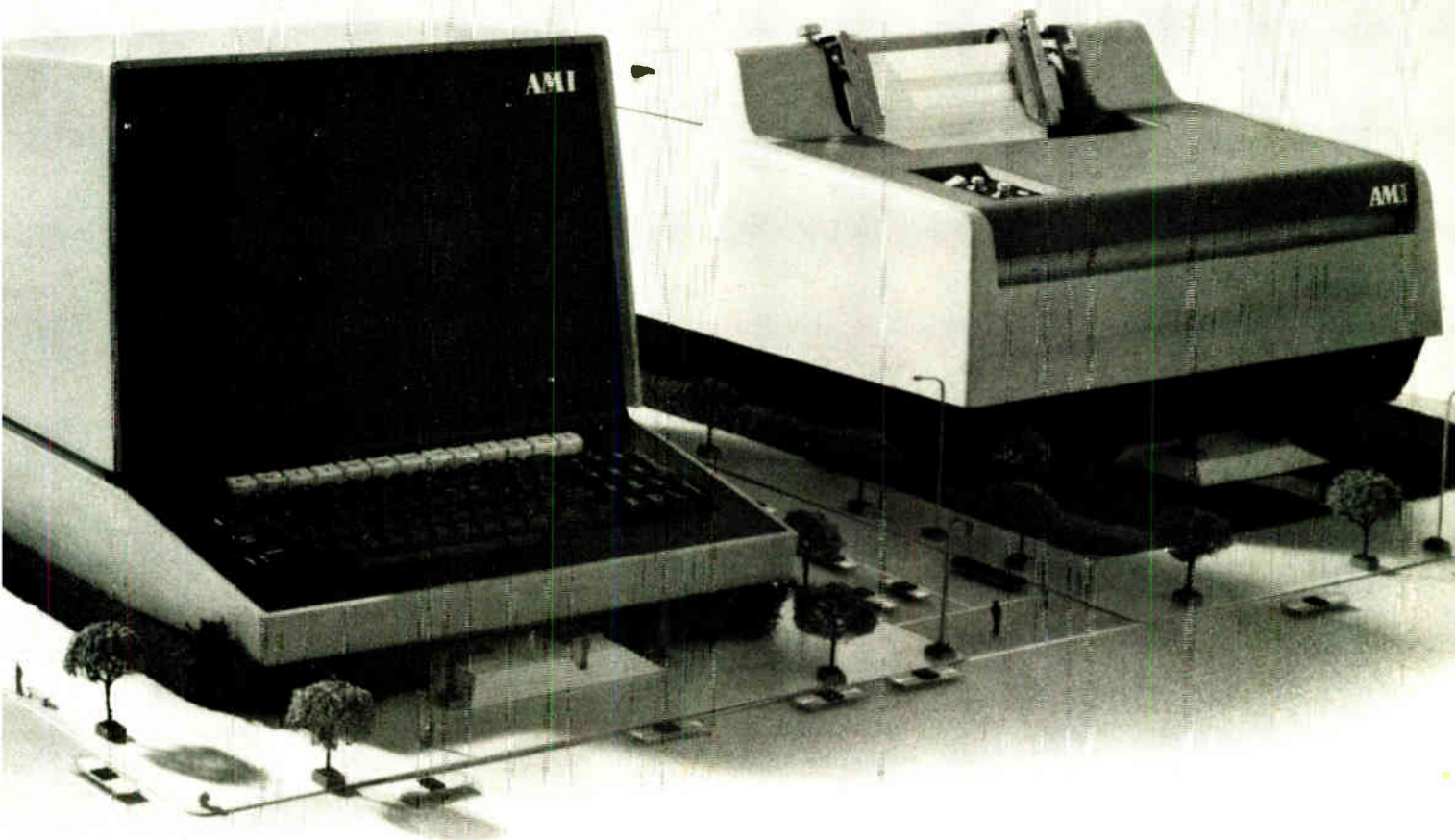
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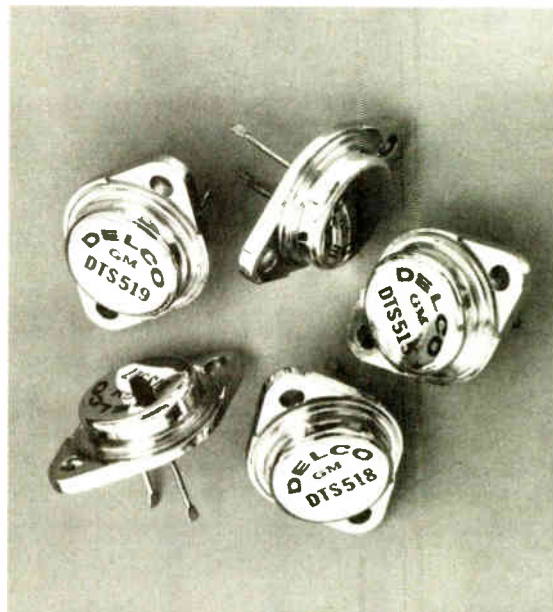
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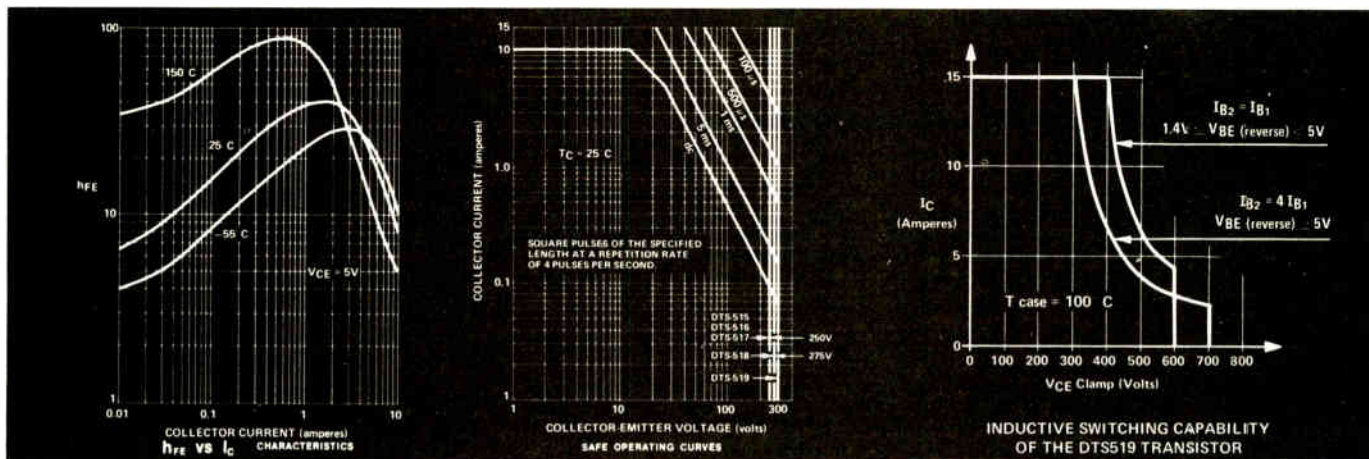
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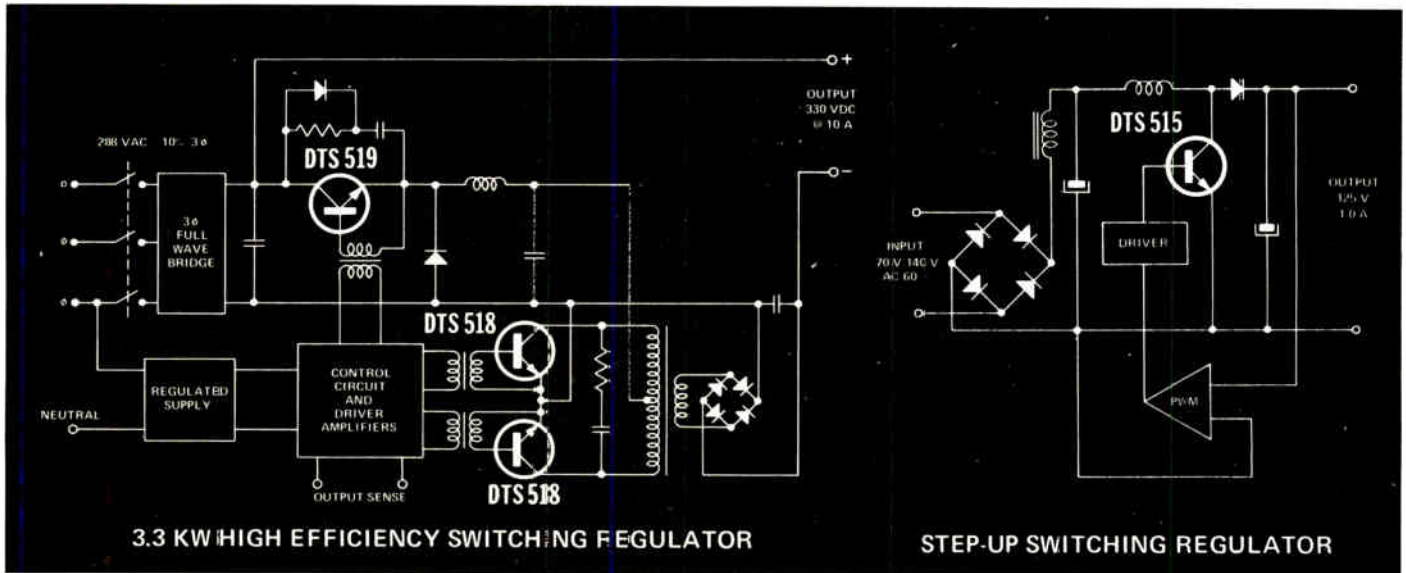
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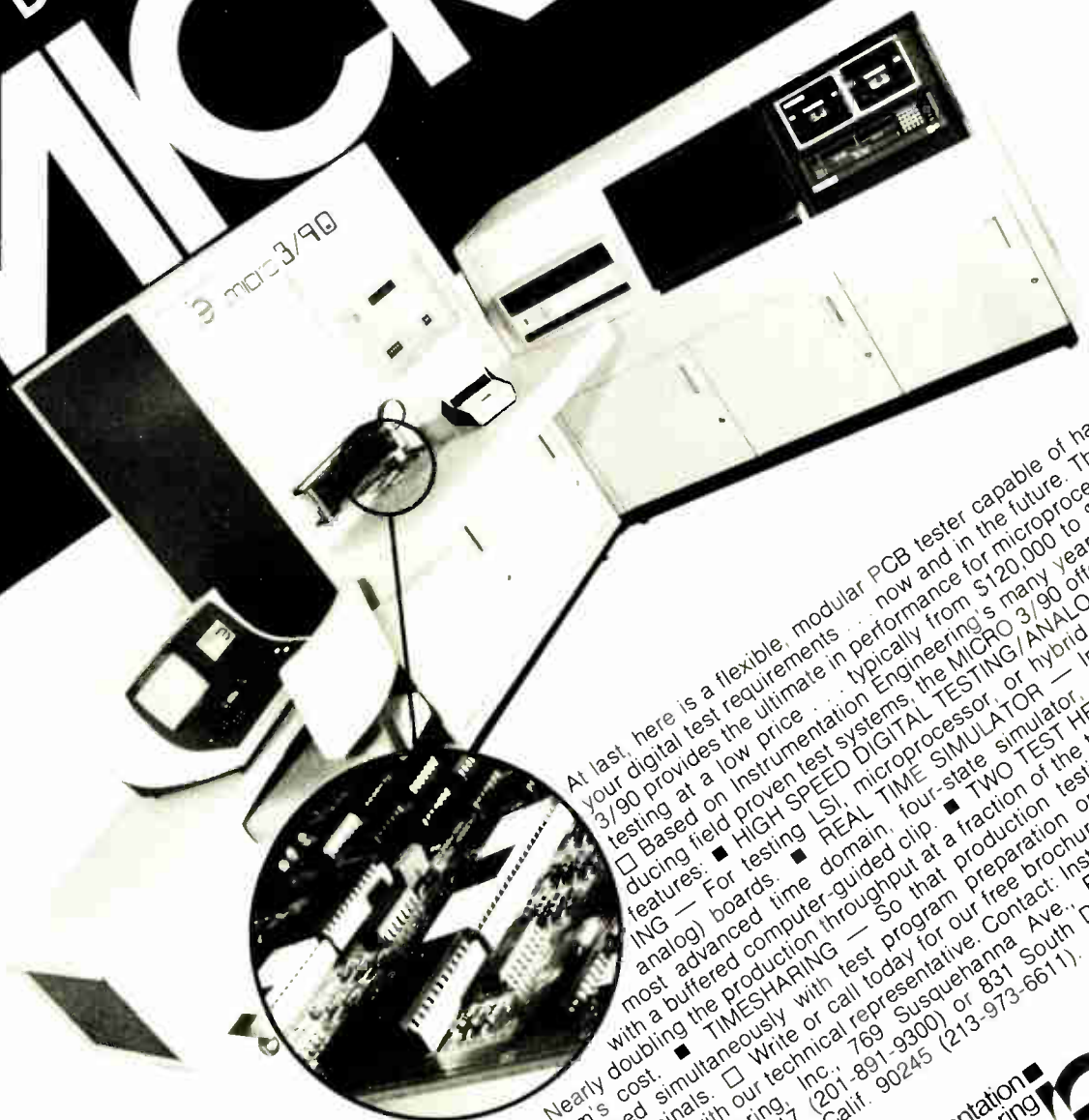
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Japanese space-TV gear aids treatment of U. S. Indians

The first all-electronic system for eventual transmission of still color-television films from the space shuttle is being installed this month in the U.S. by the National Aeronautics and Space Administration. The system, developed by Japan's Nippon Electric Co., is replacing a prototype system already being tested in a unique humanitarian application on earth.

One terminal, installed at a health facility on the Papago Indian Reservation at Sells, Ariz., transmits X rays and pictures of patients' infirmities to an Indian hospital in Phoenix for analysis by specialists there. The system, being tested in cooperation with the Indian Health Service, is called Starpahc.

Standard NTSC color cameras and monitors are used. Because Starpahc is built to commercial communications standards rather than space standards, the system is large and heavy. But at \$55,000, it is also cheaper than the space model will be. Starpahc enables still color-TV pictures to be transmitted by means of differential pulse-code modulation (DPCM) over bandwidths as small or even smaller than those of a standard telephone line. Important as bandwidth economy is on earth, it is even more critical in space.

Operation. Starpahc directly converts NTSC color-TV brightness and chroma signals to digital values, compresses the bandwidth, and stores the values. The analog color signal sample is converted initially to 8 bits. A DPCM encoder compresses the eight bits into a 4-bit signal sample, which is stored in a high-speed bipolar buffer memory and then is transferred to the main semiconductor memory in the form of 48-bit words.

The cycle time of the main memory is not short enough to store the 4-bit groups as they are formed.

Transmission makes use of higher-order prediction—the predicted value of a sample depends on the value of the three previous samples.

Transmission. Since the new terminals transmit one of the two NTSC TV fields that normally constitute a complete frame, the vertical resolution is only half the value of conventional television. However, it appears to be adequate for the

intended applications. The entire frame was not used because any motion of a subject between two successive fields in one frame would displace them and reduce, rather than enhance resolution of still pictures. In addition, the transmission of a single frame halves the memory capacity and time required for transmission. But four more memory cards can be plugged in to pro-

Around the world

British simplify formation of IC contacts

A simple way of forming the tiny metal contacts on semiconductors has been developed by Britain's Royal Signals and Radar Establishment (RSRE). The method, called selected-area electroplating, involves bombardment by a 5-kilovolt ion machine, a conventional plating solution, and illumination by an ordinary 60-watt bulb about 20 centimeters above the device. The RSRE has made in the laboratory n-type gallium-arsenide Schottky-barrier field-effect transistors it says perform as well as conventional FETs, and the process should work for all semiconductor devices. The agency says the process, which could be automated, would fit into semiconductor production lines after photomasking and photoresist.

Essentially, ohmic or rectifying contacts are deposited onto a photo-masked semiconductor slice by first damaging the required area with charged particles and then dipping the slice into the appropriate plating solution illuminated by electric light. Without any external connections, this process creates a cathode electrode in the damaged area and an anode electrode on the semiconductor surface. The plating current flows through the electrolyte, causing the metal to be deposited on the bombarded area.

Several metals can be deposited by selecting the correct electrolyte, and the rate of deposition can be controlled by the extent of the ion bombardment, the area ratio between the anode and cathode, and the amount of light. Multiple metal layers can be formed by sequentially dunking the slices into the proper plating solutions.

UK timer chip directly drives TV-clock display

General Instrument Microelectronics Ltd. of the UK is offering a timer it claims has more drive than its competitors. When the new AY-5-1230 is built into a television set, the chip not only drives time displays in conjunction with GIM's AY-5-8320 display circuit, but it can directly drive a seven-segment four-digit fluorescent display for clocks. A viewer can program it to turn the set on and off at preset times for days on end, but if he doesn't select a turn-off time along with the turn-on time, the device automatically shuts off the set within 10 minutes. GIM says the ion-implant nitride process for its p-channel metal-gate MOS chip saves 12 external resistors. Better yet, the timing output is a high 30 milliamperes, which can drive relays and triacs.

Although the company is aiming initially for the West German TV market, it also visualizes applications in cookers, heating controls, and video recorders. The price would be only \$2.50 each in quantities of 10,000. The chip runs off the standby power used for remote control.

vide full-frame operation if desired.

The terminals each contain 768 kilobits of semiconductor memory, composed of NEC's latest 4,096-bit n-channel MOS random-access-memory chips. The memory stores the entire image in the 1/60-second field interval at the originating end. Transmission-control circuits feed the digital signals to a modem at the rate appropriate to the transmission line. At the receiver end, the image

is stored in memory and is repetitively read out to refresh the monitors every 1/60 second.

At the rate of 2.4 kilobits per second through an inexpensive modem and over a standard telephone line, a single field requires 300 seconds for transmission. NASA uses a 4.8-kb/s modem to transmit in half that time. However, if a standard 24-channel PCM cable were used, each field would require 0.5 second. □

Austria

Security system responds to changes in power level and tension of fence

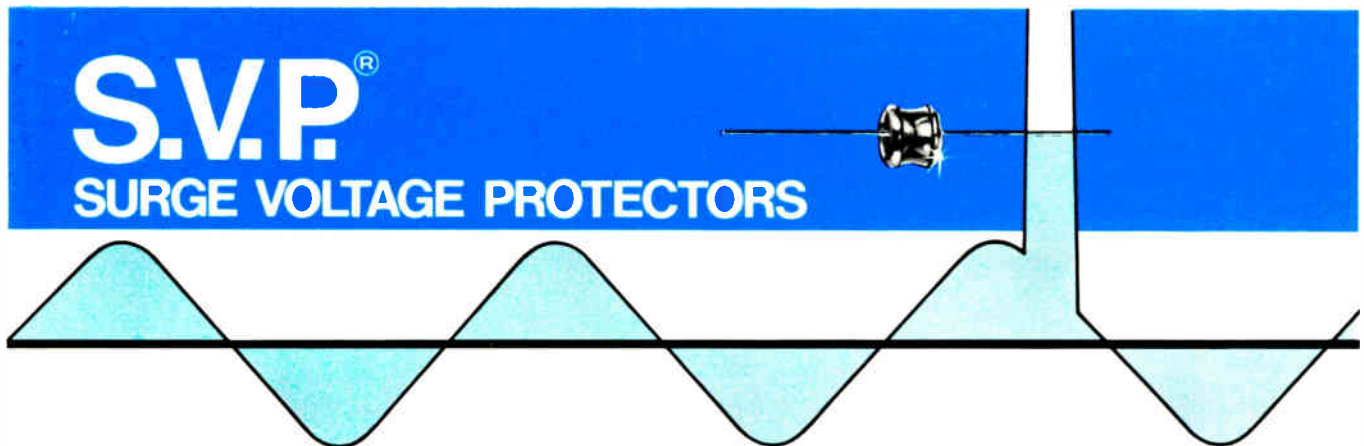
One system used to protect the 1,500 athletes during the Winter Olympics at Innsbruck, Austria, sounds an alarm when sensors de-

tect sabotage or tampering with a wire-mesh fence guarding a particular area. The small control computer is programmed to reject vibrations set

up by inadvertent contacts or weather conditions. Since the Winter Olympics in February, the Gama system has been installed at several industrial facilities, including atomic power plants in Europe and Israel.

Designed by the small Austrian firm Gama-Electronic, the so-called FSD 05 consists of a number of sensors and the single cable for signal transmission and power supply, in addition to the computer. The sensors, hidden inside certain fence posts, respond to vibrations and mechanical or electrical tampering and send corresponding signals to the computer, situated in a guard house or security office.

Discriminating. The computer, also designed by Gama, stores 16 different words, each representing an unusual physical condition of the fence posts and wire mesh. These



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conditions include overtaut wires, which could be caused by someone placing a ladder against the fence, or slackness in the wire mesh, which could result when wires are cut. The sensor-derived signals are compared with the words in the computer memory, and if the information jibes, an alarm is activated.

The computer can be programmed for several alarm stages. In a two-stage alarm configuration, the first stage would signal a condition when a wire is jerked, say, only once and then no more. During the second stage, an alarm might be sounded when wires are cut in rapid succession, indicating an attempt to penetrate the fence. The alarm is triggered when any kind of mechanical or electrical tampering is sensed.

The sensor is a piezoceramic vibration pickup that comes as a cylindrical body roughly 12 centime-

ters long and 4 cm in diameter, which fits into most commonly used fence posts. Part of the device is a high-impedance, highly linear amplifier for boosting vibration-induced signals.

Detecting sabotage. The so-called sabotage detector senses and signals all conditions that would render the system inoperative. These conditions may be an overvoltage, an excessive temperature, or a break in the sensor's ceramic body. This detector also senses any current variations in the supply cable that might result from cutting or wiring around certain cable sections. Sound waves send the fence wires into minute vibrations that are picked up by the vibration sensor. The system can distinguish vibrations set up by human speech from those produced by such weather disturbances as wind, rain, and hail.

In evaluating the signal coming from the sensors' vibration pickup, the computer first applies these signals to an amplitude discriminator and then to a frequency analyzer. The resulting histogram, which contains both amplitude and frequency information, is digitally compared with the stored words representing the unusual physical conditions of the wire mesh or fence posts.

When the comparison shows agreement, alarm pulses either sound an alarm, flash a light or activate television cameras. At the same time, a microphone is turned on so that the guard personnel can listen to any noises along the fence. A single coaxial cable supplies the power and transmits the signals derived from the sensors. Because of the sensor's low current drive—about 1.5 milliamperes—the cable can be 17 miles long. □

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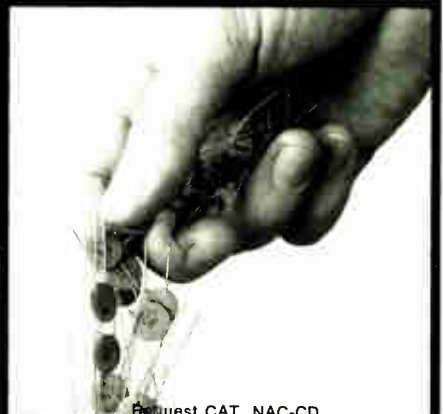
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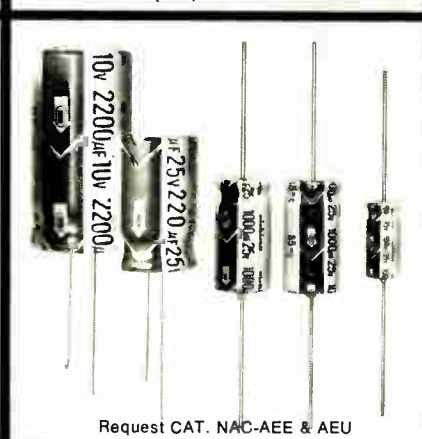
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Sony color set has 32-in. picture tube for mass viewing

A 32-inch color-television set, chiefly for mass viewing, will go on sale in Japan this summer at \$5,000. Sony Corp., the developer, will also sell the color monitor without a tuner for \$3,333. The units, equipped with output and input terminals for connection to video-tape recorders, is designed for large displays so that groups can view videotaped programs. On the theory that this application, in addition to sales for conventional TV viewing, will provide an adequate market for the large-screen sets, Sony plans to produce about 2,000 picture tubes a year.

The neck of the 32-inch tube, which has a deflection angle of 114°, is 36.5 millimeters in diameter, and the electron gun has a 19-mm bore, the largest gun Sony has ever used. The set draws 200 watts of power, which Sony compares with the 350 W dissipated by early RCA sets built with vacuum tubes. The bulb is made by Nippon Electric Glass Co. The largest previous set, 1,000 of which have been sold, was a 27-in. model, introduced last July. The picture tubes used in both of these sets have an image-modulated sweep to sharpen outlines. Sony disclosed this technique in 1974 at an IEEE conference in the U.S.

3-d gamma-ray gear to challenge X-ray body scanners

A three-dimensional semiconductor-based gamma-ray detector, which may become a competitor to computerized X-ray body scanners, is under development by the UK Medical Research Council's Institute for Medical Research. **To produce 3-d views, orthogonal Schottky-barrier junctions on n-type high-resistivity silicon slices are aligned within the camera tube to detect the direction of gamma rays emitted by radioactive fluids ingested by a patient.** A computer correlates the source and direction of the rays by matching ray strikes through matrixes on the slices.

A system made with two 5-centimeter-diameter cameras, each containing 50 slices each, is expected to operate in real time. It will show body functions, as well as provide higher resolution, be more sensitive, and subject the patient to lower doses than X rays, its developers claims.

Germany begins third program to promote EDP

West Germany's Ministry for Research and Technology has earmarked more than \$600 million for its third electronic-data-processing promotion program, to run through 1979. **Of the total, roughly 35% will be spent for EDP-related research and development and about the same percentage for system applications.** The rest is slated for computer training and special projects.

The government's third program focuses greater attention than its predecessors did on small computers and terminals. Before the end of this decade, the outlays for that type of hardware are expected to match those for large and medium-size EDP equipment. Previously, the ratio of expenditures was about 2:1 in favor of the larger systems.

France transfers to Thomson control of minicomputers

France has placed a reluctant Thomson group in charge of the minicomputer plant of the Compagnie Internationale pour l'Informatique in Toulouse and has directed Thomson to head a merger of CII minicomputer activities with those of Télémécanique Electrique. At the opening of the International Components Show last week, Michel d'Ornano, France's minister

of industry and research, called the arrangement the final phase in the restructuring of the country's computer industry. The French government will spend \$42.8 million to implement the transfer from CII to Thomson.

The government go-ahead on the move comes almost one year after the first announcement of the merger between the CII and Honeywell-Bull. In order to complete the negotiations, **Thomson had to accept the government's terms for the integration of the Toulouse plant into its own operations.**

MIT licenses X-ray mask-making gear to Japanese firm

Nippon Kogaku K.K. has been granted the exclusive right by the Massachusetts Institute of Technology to manufacture MIT's soft-X-ray lithography equipment for production of large-scale integrated circuits in Japan. **Nippon Kogaku, maker of the Nikon camera and LSI-production equipment, plans to start manufacturing the X-ray equipment in about three years.** The company already manufactures the proximity printer, which is a photographic printer for production of integrated circuits, as well as other photographic equipment for testing ICs and LSI, including the mask-alignment scope and mask comparator.

Plessey introduces synthesizers for CB radio, microwave

Britain's Plessey Semiconductors is introducing two high-density bipolar resistor-transistor-logic frequency synthesizers—one for citizens' band radio, and other for radar, microwave, and high-frequency applications up to 1.2 gigahertz. **Plessey says the synthesizers, made by the company's Process Three technology, are cheaper and simpler than complementary-MOS units, which need additional prescalers and mixers.** The two-chip 8923 CB channel synthesizer needs only an additional channel selector, voltage-controlled oscillator, and loop filter. A 50-channel version is expected soon for the U.S. market.

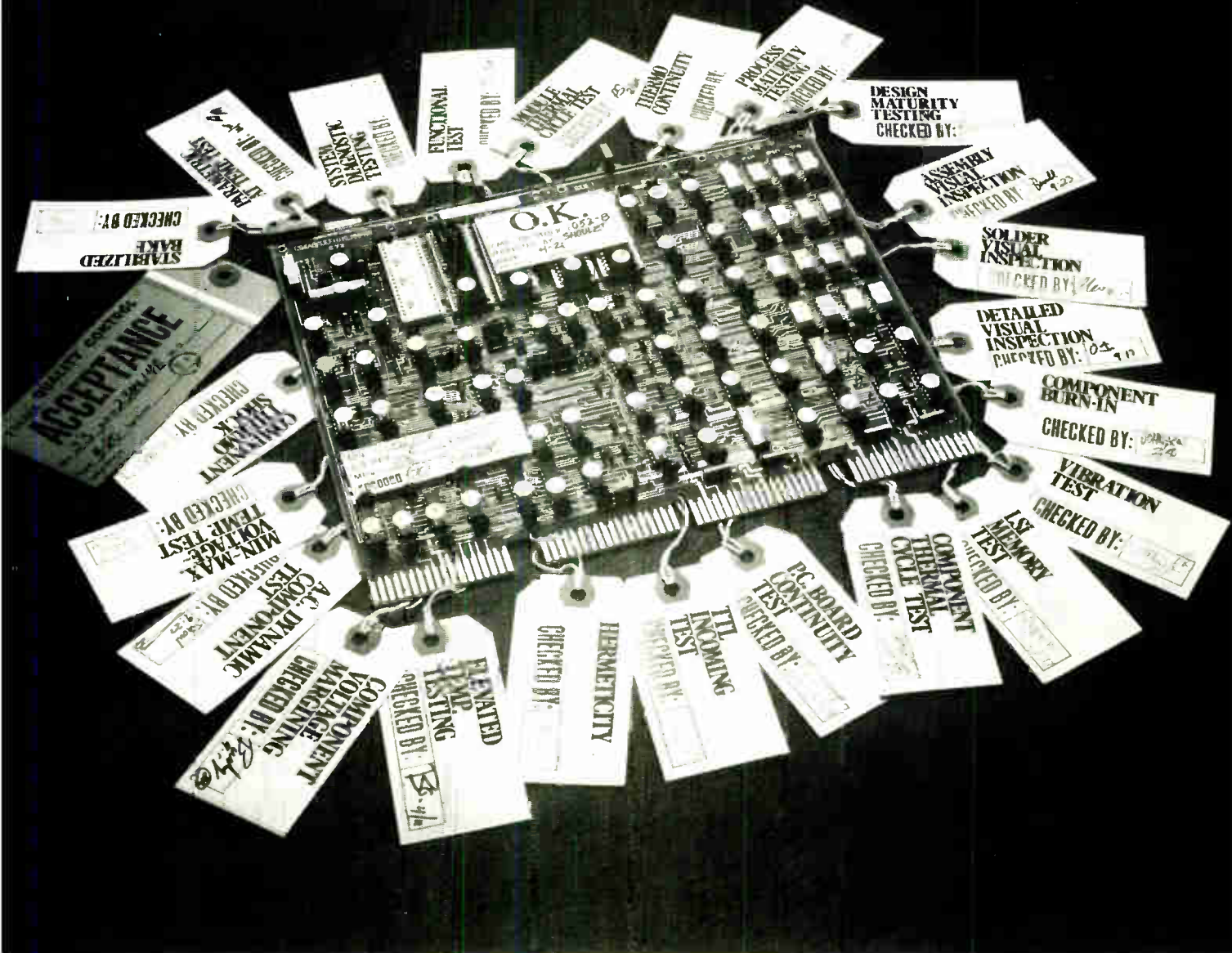
For other high-frequency applications, the modular 8760 synthesizer phase-locks a controlled oscillator to a fixed-frequency quartz oscillator by using a 1.2-GHz divide-by-64 circuit. The 8760 contains the necessary prescalers, comparators, and crystal-oscillator maintaining circuits.

Dialing cut to two digits by Siemens PBX processor

An abbreviated-dialing processor is being marketed by Siemens AG for private branch exchanges built for as few as two subscriber lines. Such processors have been available until now only for large PBX systems, the German company says. The processor, an MOS circuit, can store 100 telephone numbers, each with as many as 18 digits. **Dialing a two-digit code number is all that's needed to place a call—even an international one.** The memory content can easily be altered by plugging in a programming unit. Even if the power supply fails, programming remains intact for about 12 hours, Siemens says.

Two U.S. firms to buy color-video recorders in Japan

RCA and Ampex in the U.S. have agreed to have Victor Co. of Japan manufacture two types of lightweight ¾-inch color-video cassette recorders for electronic news gathering. **To be exported to the U.S. under the RCA and Ampex logos, the two machines are the CR-4400 portable recorder and the CR-8300 desk-type recorder.**



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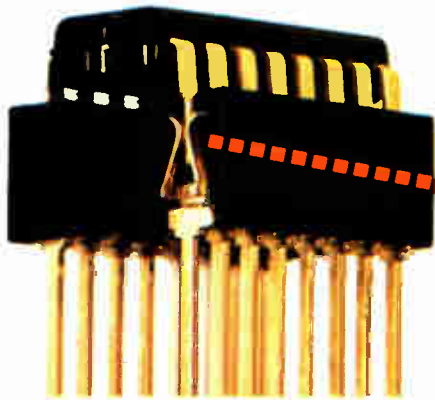
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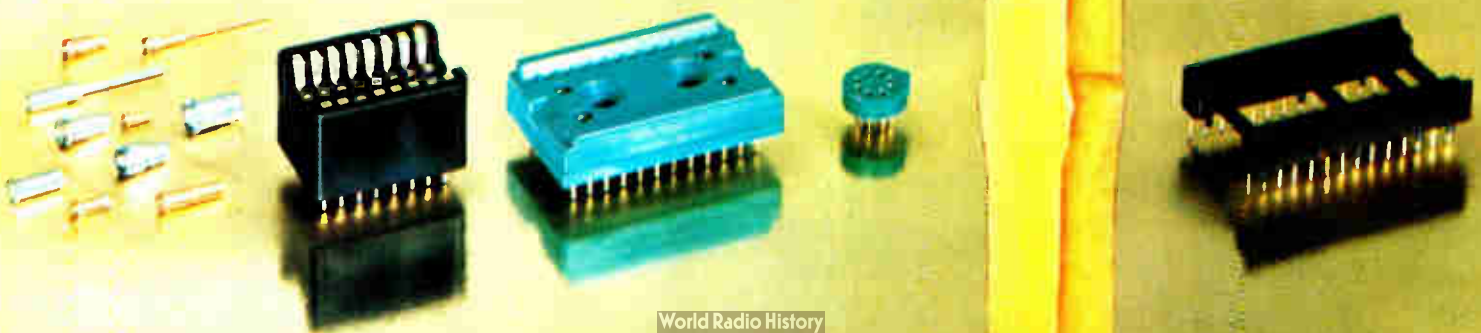
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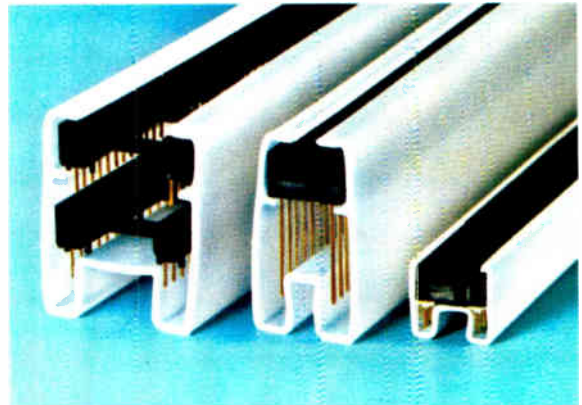


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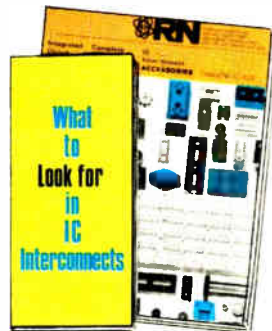
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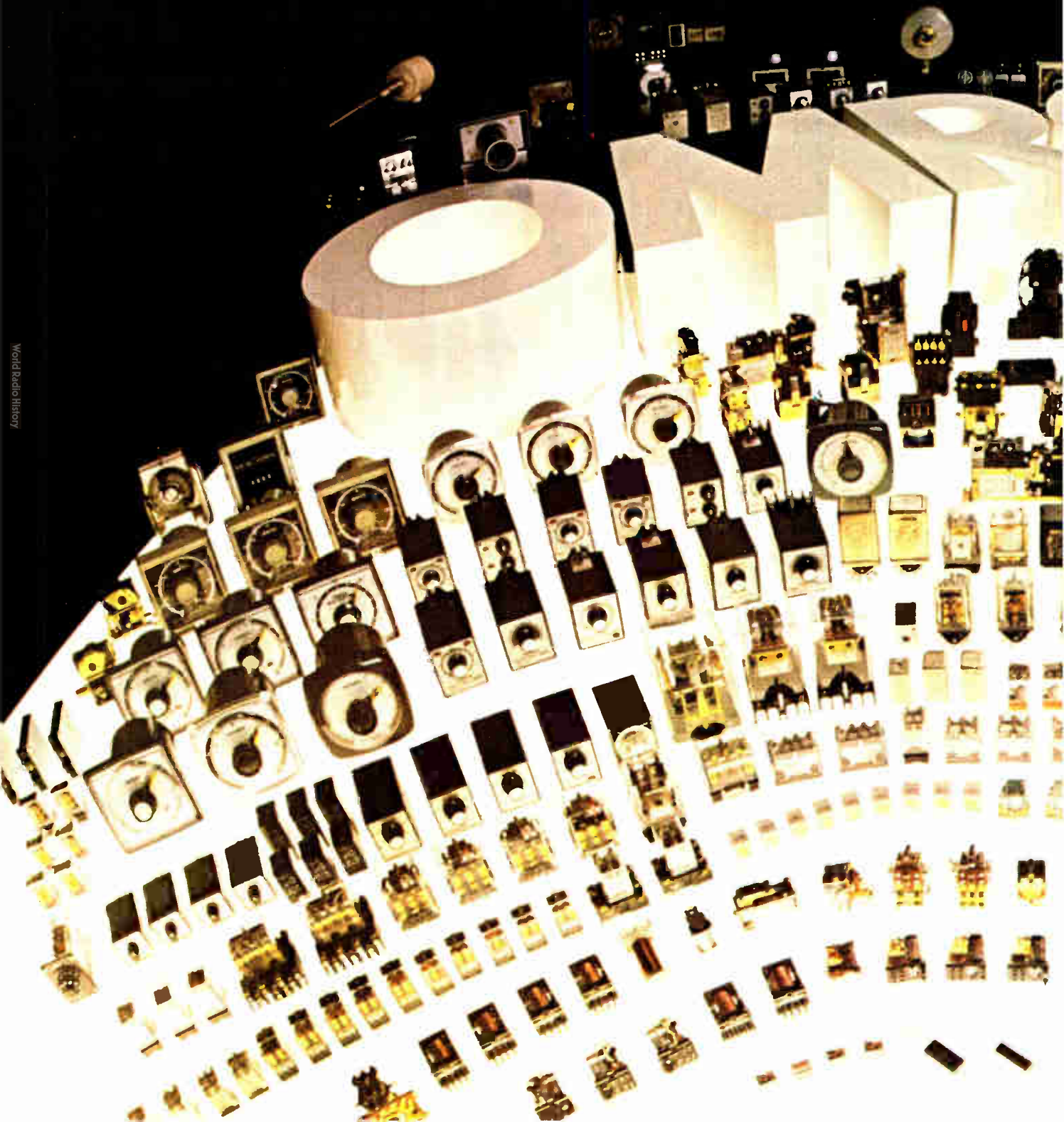
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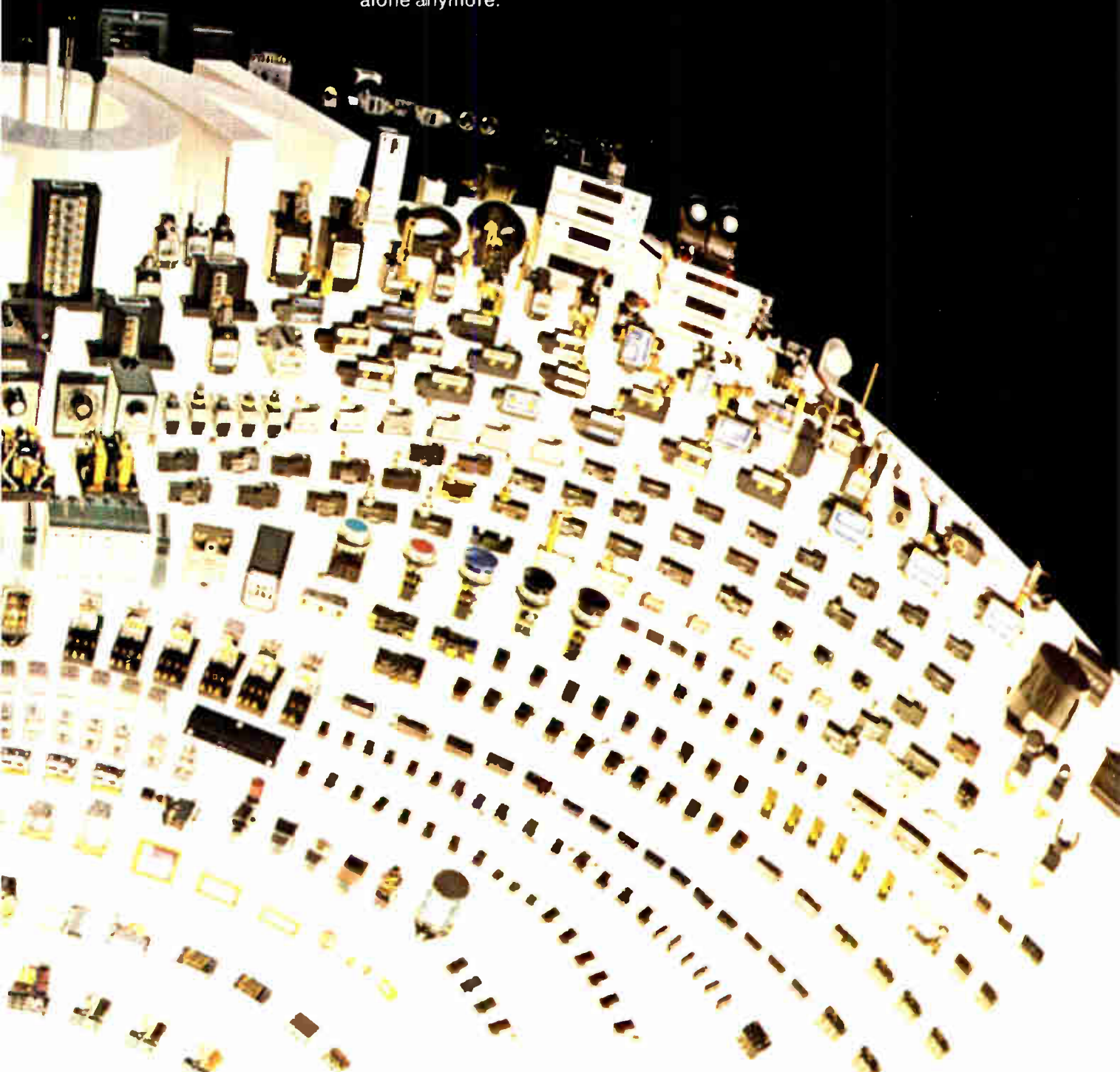
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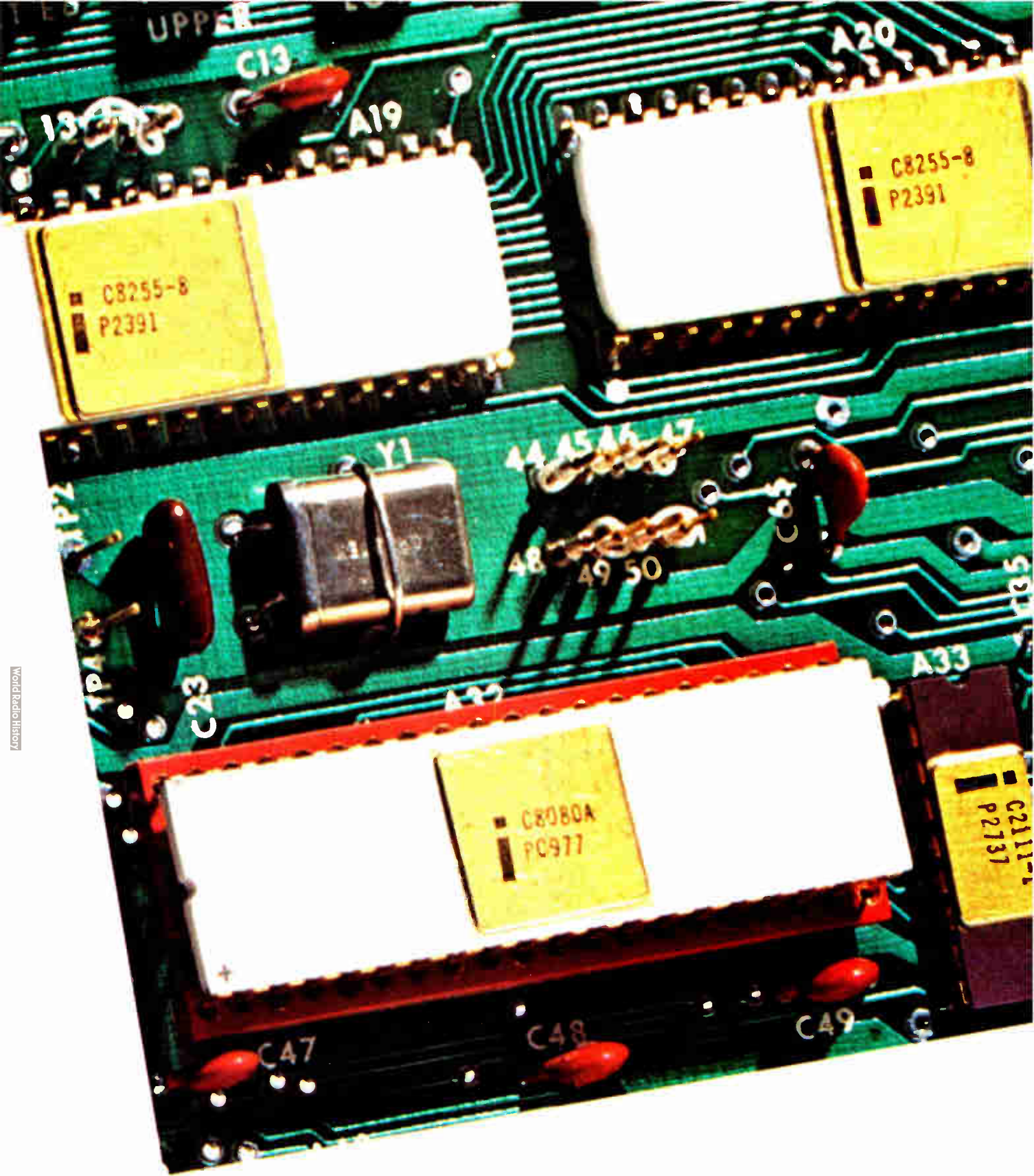
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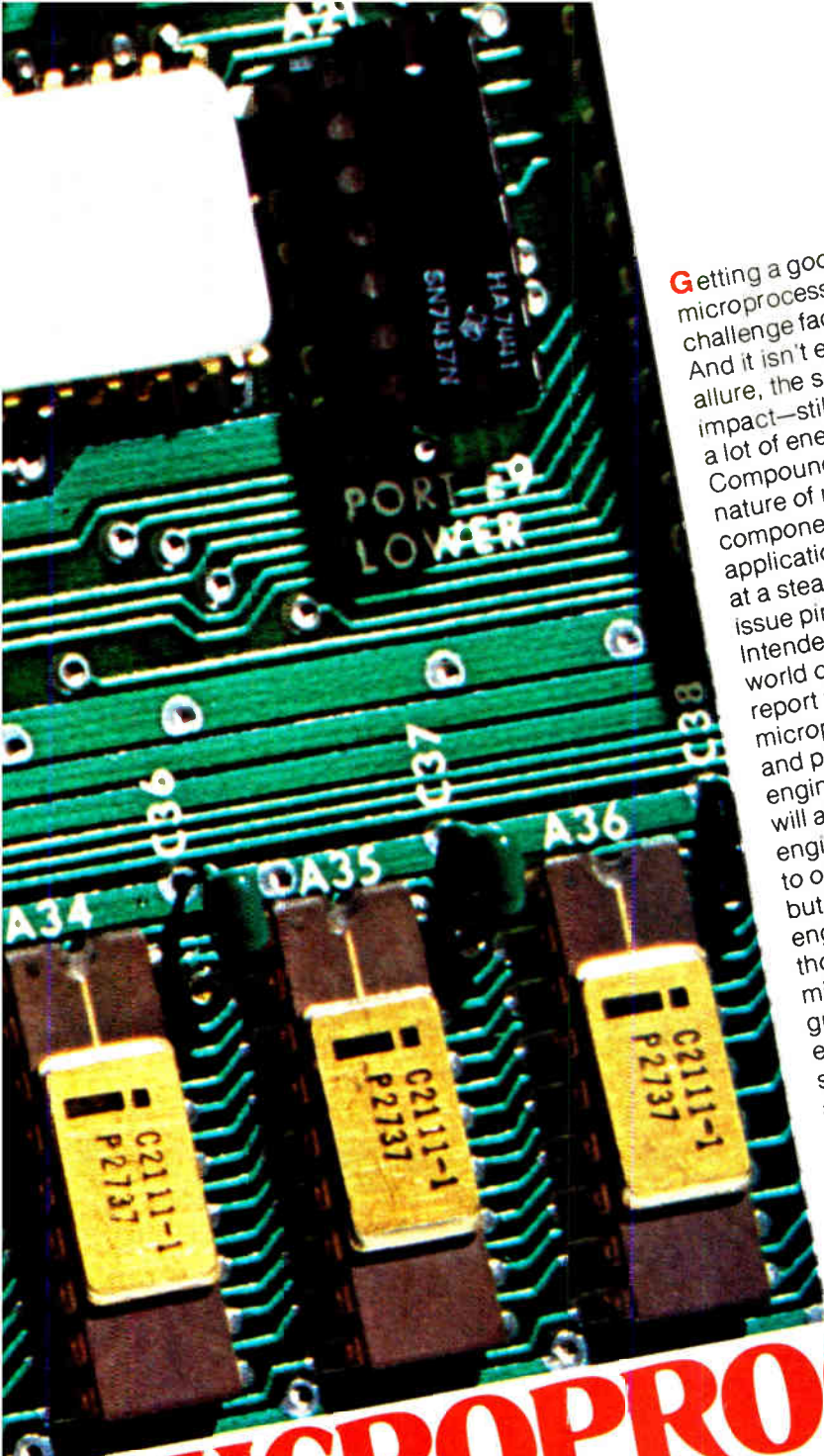


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Getting a good grip on the subject of microprocessors is the biggest and most exciting challenge facing electronics engineers today. And it isn't easy. For all its fascination and allure, the subject is so complex, and its impact—still not fully felt—so far-reaching that a lot of energy is needed to encompass it all. Compounding the problem is the dynamic nature of microprocessor developments. New components, new techniques, new applications—and new markets—are appearing at a steadily accelerating pace. This special issue pins down where things stand today intended to ease the transition to the new world of microprocessor engineering, the report will present the case for the microprocessor as a tool whose versatility and power exceed anything electronics engineers have ever had at their disposal. It will also demonstrate that microprocessor engineering isn't some mystic rite, accessible to only a small, privileged band of high priests, but a skill that can be readily mastered by any engineer who wants to make the effort. For those who are just getting on board microprocessors, this report will be a helpful guide to the realities of microprocessor engineering—ranging from the hardware and software, to the design aids, test equipment, and components you'll need to become intimate with. If you're already on board, there's a lot in the issue to help you sharpen and focus your newly won skills. And you can measure your progress against the amazing variety of real applications of microprocessor engineering that are detailed by their designers in the last third of this report.

MICROPROCESSORS

A SPECIAL ISSUE

INTRODUCTION

In plain, everyday engineering terms, the meaning of the microprocessor is three-fold:

1. Cheap, digital computing capability can be put anywhere a designer wants it.
2. For any digital system, microprocessors can greatly reduce the component count.
3. Engineering turnaround time is cut drastically.

These simple truths account for the current explosion in microprocessor activity. And explosion is just what it is. Practically all new data-processing systems at or below what one could call the minicomputer level of complexity are being designed with microprocessors. And the availability of cheap computing power enables designers to incorporate decision-making capability into applications never considered before.

It has been estimated that by 1980, microprocessor-based systems and equipment will exceed \$1 billion in sales. Entire new businesses are being spawned—in games, test equipment, communications gear, intelligent terminals, and in industrial controls of every imaginable variety.

The attributes of microprocessors that make them so attractive are almost paradoxical:

- They're complex devices, yet they can be adapted simply to many different tasks.
- They're mass-produced, but they make

custom large-scale integration economically feasible.

- They're low in cost themselves, but they add significant value to a product. It's no wonder that microprocessors are turning electronics technology on its ear. Part of their attraction is that they make the actual task of logic design easier, albeit radically different from in the past. Gone are the traditional logic diagrams, the old bench instruments for

troubleshooting, and the magnitude of the effort required to make an engineering change. Instead, the designer now works with compilers, assemblers, and editors, she makes engineering changes simply by altering a pattern that is stored in a programable read-only memory.

However, it is a radical transition from the world of gates and flip-flops to the world of programming and memory utilization, from circuit diagrams to flow charts. Compounding the difficulty is the dynamic nature of microprocessor development—an engineer can quickly be lost in the forest of new components, test equipment, design aids and all the literature that comes with it.

This special issue is intended to help you wend your way safely and efficiently through these technological thickets. It begins on the following pages with a comprehensive roundup of the

microprocessor families that are available or newly emerging. This section will provide valuable insight into the architecture and performance of each family, whether chip or board, and help you make the right selection for your application.

Perhaps the most perplexing task facing the designer taking on the microprocessor is becoming familiar with software and its uses. The next section in this special issue will lead you through the formerly arcane universe of assemblers, compilers, simulators, and high-level languages. It's important to be able to assess these, because each has its advantages and disadvantages in terms of cost, ease of use, and efficiency in memory utilization.

Out of the microprocessor ferment is rising a whole new class of instruments and exerciser equipment, accompanied by special software that simplifies the job of producing and debugging a prototype system. Right now, most of these developments are coming from the semiconductor manufacturers for their own microprocessor-chip families. How these aids fit into the design process is the subject of the next section of this issue, which also discusses a new class of universal development systems that is on the way. The systems are applicable to any type of processor.

The sheer complexity of the microprocessor imposes a difficult testing

problem at both device and board levels. Compared to the conventional hard-wired logic board, microprocessor failure modes are far more subtle and varied and therefore more difficult to detect. The testing report in this special issue sorts out the various techniques being employed. It shows that, at both levels, the choice of test method depends greatly on the degree of assurance—and therefore the cost—you are willing to accept.

If any part of this special issue testifies to the scope of the microprocessor explosion, it is the final section of this report, dedicated to applications. Here we have assembled 14 examples of successful designs of real products, described by the engineers who conceived them. They range from process control systems to cash registers, from blood analyzers to telephone automation, and encompass simple 4-bit, ubiquitous 8-bit, and sophisticated 16-bit systems. We asked all the contributors in this section to tell why they decided to use a microprocessor in the first place, and why they chose the one they used. And we asked that, whenever possible, they describe the major problems—in hardware as well as software—they ran into, and how they solved them. We believe that their collective experience will be a valuable guide to most digital design engineers, who inevitably will find themselves working with microprocessors.

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Designers gain new freedom as options multiply

Enhancements add lustre to the capabilities of established families, and new devices are extending the performance range in both directions. Low-cost microcomputer boards offer another alternative.

After 18 months of calm, in which microprocessor manufacturers have consolidated the designs of their first general-purpose families, a second big wave of activity has begun. This time, however, it reaches a more sophisticated level.

Urged on by savvy users, whose concern is with system design rather than chip architecture, the manufacturers are introducing second- and third-order refinements aimed at boosting microcomputer capacity while lowering system cost. At the same time, they are rushing new devices to market to extend the microprocessor performance range both at the low end, where existing chips present an overkill solution, and at the high end.

Four trends are emerging. First, established families are being enhanced. System throughput is being increased and instruction sets enlarged as manufacturers turn to new metal-oxide-semiconductor processing and improved central-processor architecture. Input/output power, too, is being increased with new sets of programmable I/O chips.

Second, the new 16-bit single-chip processing units are heading upwards. What they are aiming for is the high-performance end of the microprocessor market, where precision arithmetic and large memories must be accommodated.

Third, the one-chip controllers, as their name implies, contain enough computing power to handle many stand-alone controller functions on their own. On the same chip as the central processing unit sit control read-only memory for program storage, random-access memory for data storage, and input/output registers for system manipulation.

Finally, there's a host of single-board microcomputers, beguiling alternatives to the do-it-yourself approach of buying just the chips.

All these developments are changing the microprocessor universe. In order to graph this change, Fig. 1 charts the various family types against the applications spectrum.

Clearly, the 8-bit system covers the most ground, being used in many more different designs than either the 4- or 16-bit devices. Indeed, the 8-bit word seems just about right for most of today's microcomputer systems, in contrast to the 16-bit words that are the staple of minicomputers.

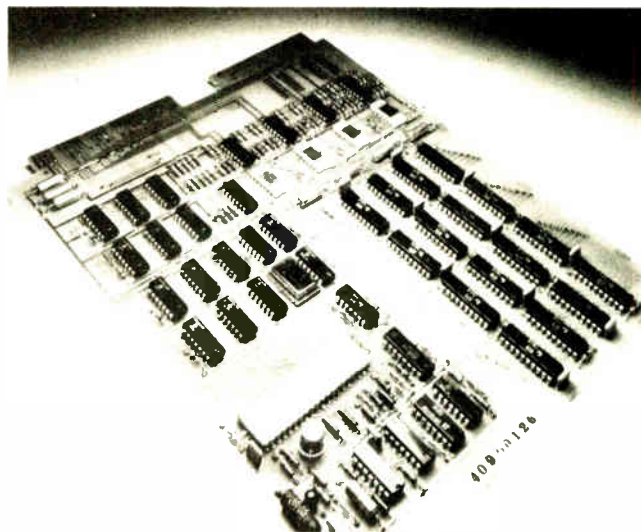
How much overlap there will be between powerful 8-bit general-purpose systems and the 16-bit high-performance systems is still to be determined, especially in large-memory process-control applications. The current

wisdom is that the 16-bit families will remain primarily on the high-performance end of the application spectrum for several years, since the 8-bit families are so well established.

Besides, enhanced 8-bit microprocessors are coming along that are faster and can handle 16-bit word data anyway, making it easy for a user to upgrade his 8-bit system to a 16-bit design without much additional investment in software. Moreover, the use of single-chip controllers in distributed processing systems boosts the performance of 8-bit designs by taking much of the burden off the central processing unit and, in many cases, by making it unnecessary to move up to a higher-capacity 16-bit CPU system.

Meanwhile the multichip 4-bit systems—the earliest microprocessors to appear—are feeling increasing pressure from the minimum-chip system designs. Rockwell's PPS-8/2 and PPS-4/2 two-chip systems, Fairchild Semiconductor's F-8, National Semiconductor's SC/MP, and Electronic Arrays' 9002 can all handle many of the jobs formerly done by the 4-bit Intel MCS-4 or Rockwell PPS-4 but often with fewer packages and at lower cost. Moreover, the single-chip 4- and 8-bit microcontrollers already mentioned will increasingly eliminate the need for multichip 4-bit designs.

Puts it all together. Activity in microprocessors is fast and furious, as manufacturers make available a wide range of products, from low-cost microcontroller chips to powerful, general-purpose families and boards. This 16-bit microcomputer is from Data General.



The 8-bit mainstream

In the 8-bit microprocessor applications spectrum, Intel Corp.'s 8080 family, with its enhanced 8080A CPU, Motorola Semiconductor's 6800 family, with its enhanced 6800D CPU, and Rockwell's PPS-8 family currently rank one, two, and three in popularity among users. The 8080 system is being used in a wide range of industrial process controls, games, intelligent data terminals, and so on. The 6800 has found its greatest penetration in data-communications terminals and instrumentation. The PPS-8 has found strong acceptance in skid-control automotive designs, as well as in other high-volume systems. All are second-sourced—the 8080 by AMD, TI, NEC, and Siemens, the 6800 by AMI, and the PPS-8 by National.

What makes these chip families so suitable for general-purpose applications is the centralization of their computing capabilities—an orientation borrowed from minicomputer architecture. Unlike many newer designs, such as the F-8, which distributes its computing power among its family of devices, the 8080, 6800, and PPS-8 concentrate that power all on a single chip. In effect, their central processing units act as their own peripheral controllers, using generalized bus lines to manipulate external memories, interface chips, and input/output chips.

These CPU chips are well equipped for their job. Both the 8080A and 6800D have a 16-bit address bus, an 8-bit bidirectional data bus, and fully TTL-compatible control outputs. Besides supporting up to 65 kilobytes of random-access memory, they can address a large num-

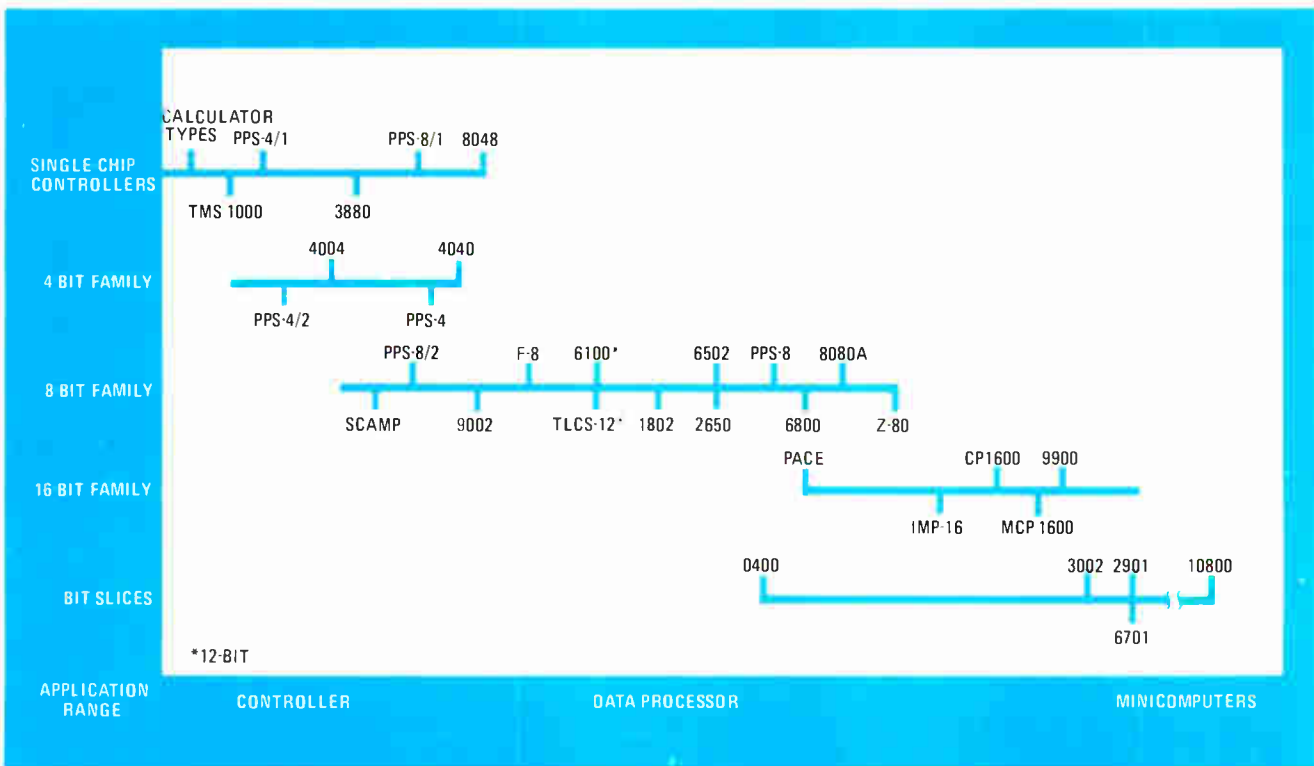
ber of peripheral devices, providing for practically unlimited system expansion.

Moreover, both CPUs show a considerable improvement in architecture over the preceding generation of 8-bit designs. The 8080, for example, contains a 16-bit stack pointer that controls the addressing of an external stack located in memory. The proper instructions can initialize this pointer to use any portion of external memory as a last-in/first-out stack, so that almost unlimited subroutine nesting becomes available. The stack pointer in addition allows the contents of the program counter, the accumulator, the condition flags, or any of the data registers to be stored in or retrieved from the external stack.

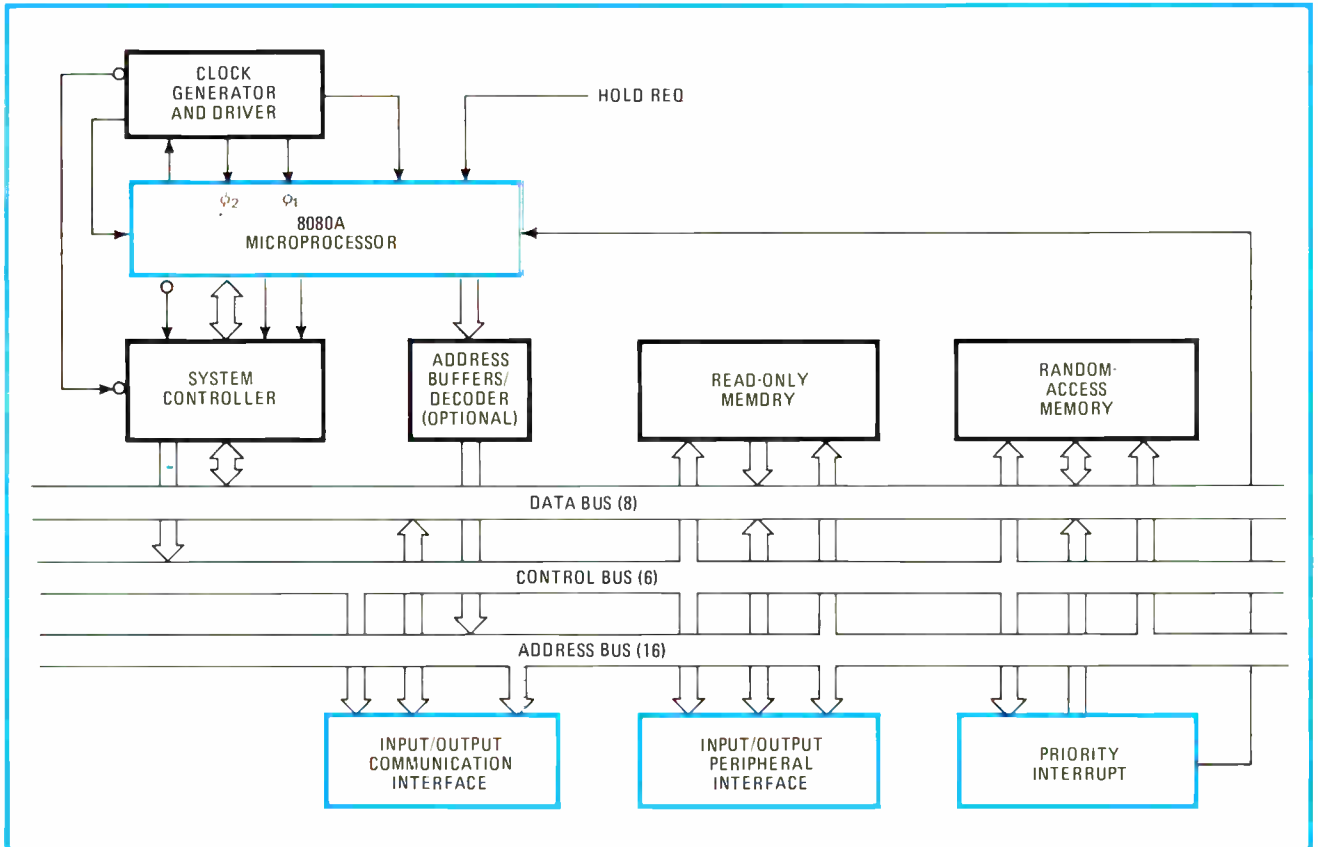
The 8080's stack control instructions also permit multilevel interrupts. The current program or "status" of the processor can be pushed onto the stack when an interrupt is accepted, then popped off the stack after the interrupt has been serviced, and this can be done even when the interrupt service routine is itself interrupted.

Where the two families differ is in several of the system requirements. The 6800's single 5-volt power supply contrasts with the 8080's ± 5 v and 12 v supplies. The 6800 timing is quite simple. All instructions are executed in two or three cycles, which are identical in length. Control outputs are real-time signals instead of look-ahead instructions. Moreover, in the 6800 system, separate I/O instructions are unnecessary since memory locations can house either I/O or memory data.

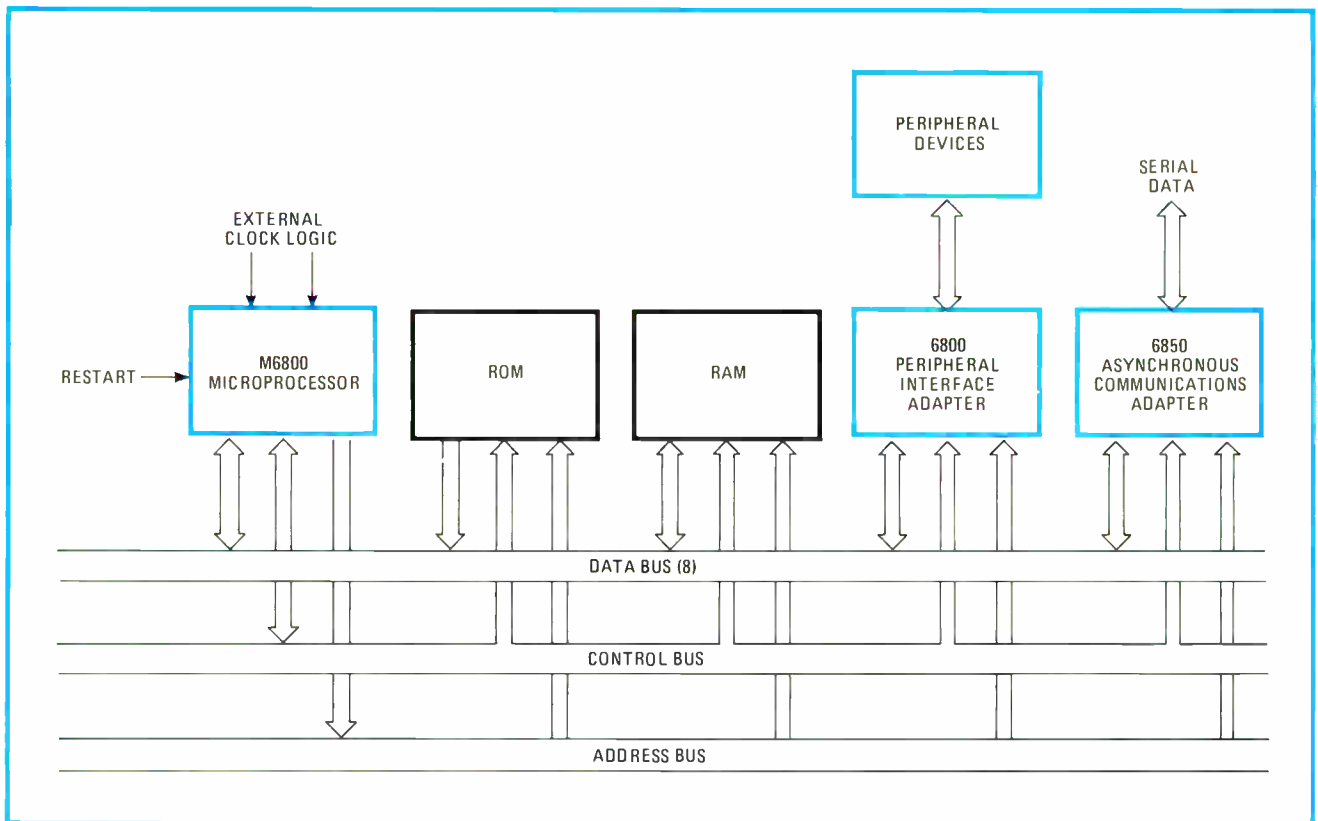
On the other hand, the 8080 has more powerful instructions, with stronger branch and interrupt capability. It can interface with a wide variety of peripheral devices. It has tremendous software support, such as an in-



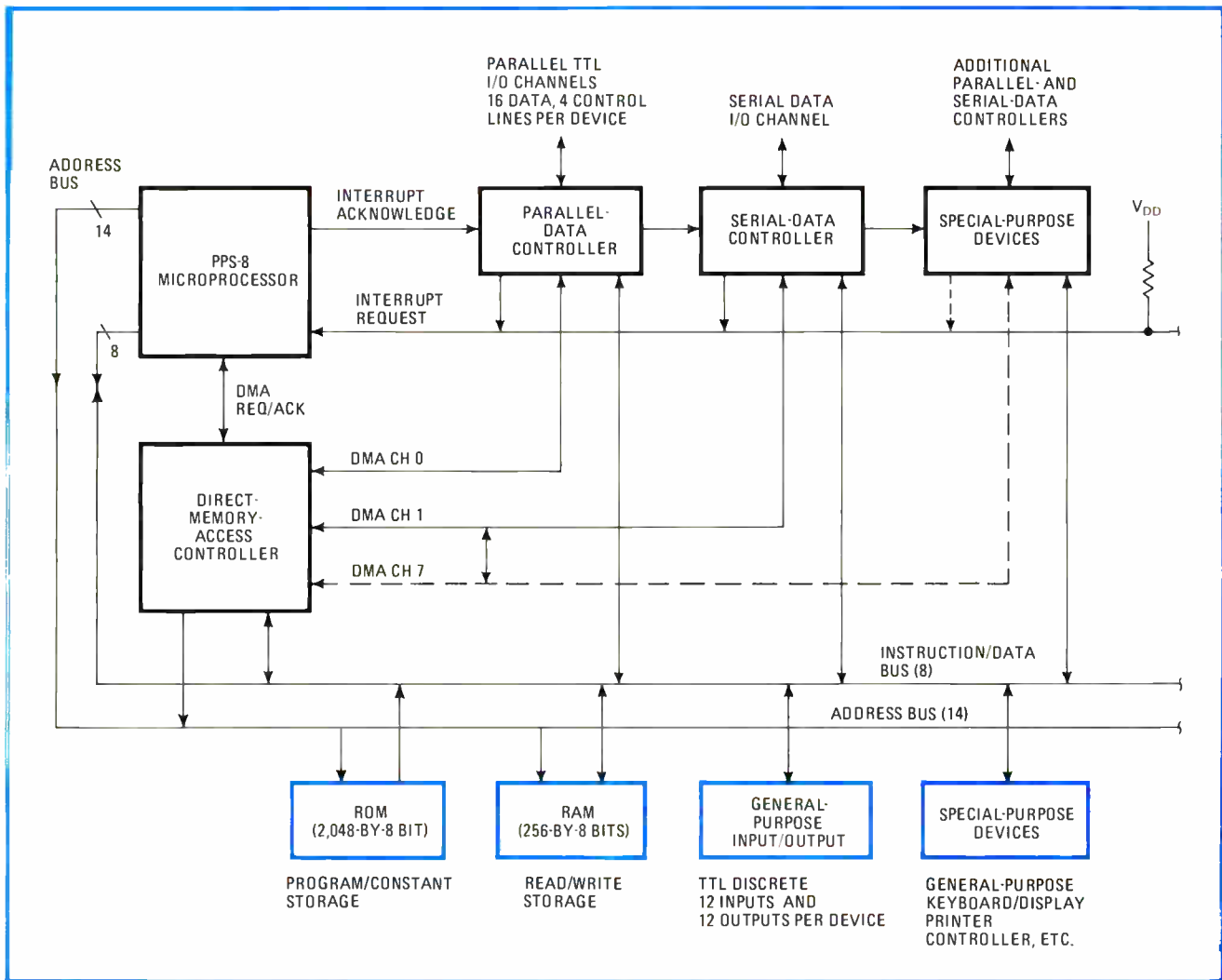
1. **The universe.** The 8-bit microprocessor families cover most ground, being found in everything from peripheral controllers to powerful data-processing systems. The 4-bit systems handle the smaller controller jobs, while the 16-bit chips and bit slices rise to minicomputer work.



2. The 8080. Intel's 8080 system can produce dozens of peripheral and I/O device configurations. Because all devices connect to a system bus, hooking up parts into complex configurations becomes quite straightforward once the instruction program has been developed.



3. The 6800. A Motorola 6800 system, also designed around a central bus, keeps the package count to a minimum by using powerful peripheral devices, such as the peripheral interface and communication adapters. System works off standard ROMs and RAMs.



4. **The PPS-8.** In Rockwell's PPS-8 microcomputers, general-purpose input/output, ROM, and RAM chips again hook up directly to address and instruction data buses. Family contains a direct-memory-access controller and parallel and serial I/O data channel modules.

circuit prototype developing system and a large library of user-generated instruction programs. All this accounts for the 8080 system's overwhelming success.

Rockwell's PPS-8 differs from both the 8080 and the 6800 in the basic architecture of its CPU. Its CPU chip has an arithmetic/logic unit, a control unit, accumulators, and address registers, laid out much as in the 8080 and 6800, but interlinked quite differently from either the 8080 and 6800 families (see Figs. 2, 3, and 4). For example, the program and data memories in a PPS-8 microcomputer system have completely separate and parallel address spaces, so that a memory address may legitimately identify two different memory locations—maybe a byte of program memory containing an instruction code and a byte of data memory containing binary data. This double-duty memory address accounts for the PPS-8's high throughput, even though it is built with p-channel MOS technology.

A unique feature of the PPS-8—its clock signals—adds to its flexibility. These signals serve for both synchronization and control. The four-phase clock generator transmits two clock signals to every device in a system, and every device contains logic to decode them, inter-

preting the contents of the data and address buses in different ways during different phases of a machine's cycle. As a result, the CPU can program a wide variety of peripheral devices—if the user is willing to learn his way around the clocking scheme.

While the CPU or microprocessor chip is the central controlling element in a microcomputer system, just as vital are the ROMs, RAMs, and various input, output, and interface circuits that make up the balance of the design. Figures 2, 3, and 4 illustrate typical system configurations for the 8080, 6800, and the PP-8: these, the most established general-purpose microcomputer systems, have highly-developed system components that hook up directly with the CPU on simple bidirectional bus lines.

The bus line configuration of the 8080 and 6800 families generally has become the model for most 8-bit systems. Its three bus lines—a data bus, a control bus, and an address bus—handle all elements of a system. Standard ROMs, which store the program data in the form of lookup tables, are hooked up by connecting the ROM's output lines to the data bus and input lines to the address bus. RAMs get their data written from CPU com-

AVAILABLE MICROPROCESSORS

Type No.	Technology	Address Capacity (bytes)	Manufacturers* and Comments**
4 bit			
4004	p-MOS	4-k	Intel
4040	p-MOS	4-k	Intel (National)
PPS-4	p-MOS	4-k	Rockwell (National): SV
PPS-4/2	p-MOS	8-k	Rockwell: CC, SV
PPS-4/1	p-MOS	—	Rockwell: CC, SV, RAM on chip
TMS 1000	p-MOS	8-k	Texas Instruments: SV, MP
8 bit			
EA 9002	n-MOS	65-k	Electronic Arrays: SV
F 8	n-MOS	65-k	Fairchild (Mostek): CC
8008-1	p-MOS	16-k	Intel
8080 A	n-MOS	65-k	Intel (AMD, TI, NEC, Siemens)
8048	n-MOS	2-k	Intel: 512-bit RAM on chip
6502	n-MOS	65-k	MOS Technology — other versions are available with lower address capacity
5065	p-MOS	32-k	Mostek
6800	n-MOS	65-k	Motorola (AMI): SV
SCAMP	p-MOS	65-k	National: CC, SV
1801	C-MOS	65-k	RCA: 2-chip CPU
1802	C-MOS	65-k	RCA
PPS-8	p-MOS	32-k	Rockwell (National): SV
PPS-8/2	p-MOS	32-k	Rockwell: CC, SV
2650	n-MOS	32-k	Signetics: CC, SV
300	TTL-S	8-k	Scientific Micro Systems
Z-80	n-MOS	65-k	Zilog: SV
12 bit			
6100	C-MOS	4-k	Intersil (Harris): SV, CC
TLCS-12	n-MOS	4-k	Toshiba: MP
16 bit			
CP1600	n-MOS	65-k	General Instruments: MP
MCP-1600	n-MOS	65-k	Western Digital: MP, MC
IMP-16	p-MOS	65-k	National: MP, MC
PACE	p-MOS	65-k	National: MP
PFL-1600A	n-MOS	65-k	PanaFacom: MC
TMS-9900	n-MOS	65-k	Texas Instruments: SV, general-purpose registers in memory
Bit slices			
2901	TTL	65-k	Advanced Micro Devices (Motorola, Raytheon): MP
9400	TTL	65-k	Fairchild: MP, SV
3002	TTL	512	Intel (Signetics): MP, 2 bit slice
6701	TTL	65-k	Monolithic Memories: MP
10800	ECL	65-k	Motorola: MP, CC, ECL
SBP0400	I ² L	65-k	Texas Instruments: CC, MP

NOTES

* Developing manufacturer listed first.

** Key: MP — microprogrammable SV — single voltage
 ECL — emitter coupled logic CC — clock on chip
 TTL — transistor transistor logic MC — multi chip central processing unit
 I²L — integrated injection logic

Assessing microprocessors

Making comparisons between the available microprocessors on the basis of data sheets is a very tricky business. Even a simple specification like cycle time can be highly misleading. In most cases cycle time by itself tells you practically nothing—you must know how many cycles are needed to execute what instruction. For example, some microprocessors boast cycle times as low as 1 microsecond but require multiple cycles to execute even the simplest instructions. Others list longer cycle times but require fewer cycles to do the same instruction.

Nor does it help too much to compare execution times of simple instructions. Often the time to do a fetch or a register-to-register ADD has little relation to the time required for executing more complex instructions, like calling in a subroutine on the basis of various bit settings.

Even more misleading is ranking CPU complexities in terms of numbers of registers, or I/O ports, or whether the chip has built-in direct memory access, and so on. Many powerful microprocessors, such as TI's 9900 expel all the general-purpose working registers from the CPU chip and locate them in external RAM. But the chip is more powerful than most CPUs with multiple general-purpose registers. Likewise, a minimum-chip system design, such as the F-8, has computation logic distributed over two or three matched chips, so just looking at the CPU doesn't begin to show the capability of the system.

The instruction set is another area that lends itself to vendor specmanship. Repertoire size alone has little meaning, unless you know how the supplier is counting instructions. Are multiple, closely related instructions counted as one or as many? What instructions are included? And the various types of instructions that differ only in their "if" conditions, how are they counted?

That's why this microprocessor chart is kept fairly simple. Breaking down the chips by word length gives an idea of a processor's range—but only a rough one, since the efficiency of doing anything certainly does not depend on word length alone. The technology is broken out only because knowledgeable users feel more comfortable knowing what's in the device, but it too has to be related to design—whether processing is done serially or in parallel, and so on. (All things being equal, devices built with n-channel MOS are faster, smaller, and easier to interface than those built with p-channel MOS, whereas devices built with bipolar technology are faster and can do more but are larger and cost more to build than MOS LSI devices.)

As for address capacity, obviously the more memory that a chip can access, the larger the system that can be implemented. But again, watch out. Some processors can access large amounts of memory directly. Others need external devices to reach large bytes of memory.

Another area that concerns users is alternate sourcing. In general, the alternate sources of microprocessors are proving well able to satisfy customers' demand for multiple-sourced devices. For instance, AMD's 9080A series claims speed and power specifications that in some respects exceed Intel's 8080A specifications, and AMI undertook considerable process development in building its version of Motorola's 6800 family. Mostek Corp. has done a nice job supplementing Fairchild's F-8 support and applications effort. Then too, there is the National/Rockwell technology exchange that made their respective microprocessor families available to each other.

mands that travel on the address bus, and their data is read out to the CPU on the data bus. Peripheral interface circuits receive their inputs on the control and address bus and return their data outputs on the data bus. Thus, this bidirectional bus system is the conduit serving all members of the microcomputer family. New interface and peripheral chips, regardless of their complexity, will use these bus lines, ensuring a user a simple and well-formulated method of upgrading his basic system with more powerful I/O and peripheral chips.

The dedicated 8-bit types

Unlike the general-purpose 8-bit systems, which generally use at least a dozen chips, Fairchild Semiconductor's F-8, also supplied by Mostek Corp., and National Semiconductor Corp.'s SC/MP families were designed to realize controller-type systems with the fewest possible chips at the lowest possible cost. Both families can dish up useful designs with just two chips, although the F-8 is a more powerful system, readily expandable into memory-rich designs.

The dissimilarities of these two devices stem from dissimilar design philosophies. The Fairchild F-8 designers chose a configuration that is quite unlike the CPU orientation of minicomputers. Instead they distribute process and memory control throughout the system. The F-8 therefore works best where two or three of its powerful family members can do the job standing alone, without a large number of external memory (although they can be added if necessary).

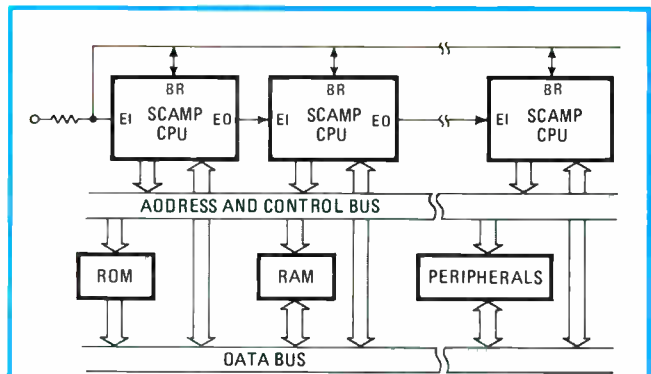
Because they interact so intimately, a designer must be familiar with the functions of the F-8 chips. Besides the CPU chip, there's a programmable storage unit, which provides read-only memory plus various logic functions—it combines with the CPU to form a complete microcomputer if so desired. A dynamic-memory interface

chip links the first two chips to either dynamic or static RAMs storing data, and a static-memory interface is for use with state RAMs only. Finally, a direct-memory-access chip implements the direct-memory-access logic in conjunction with the dynamic-memory interface chip.

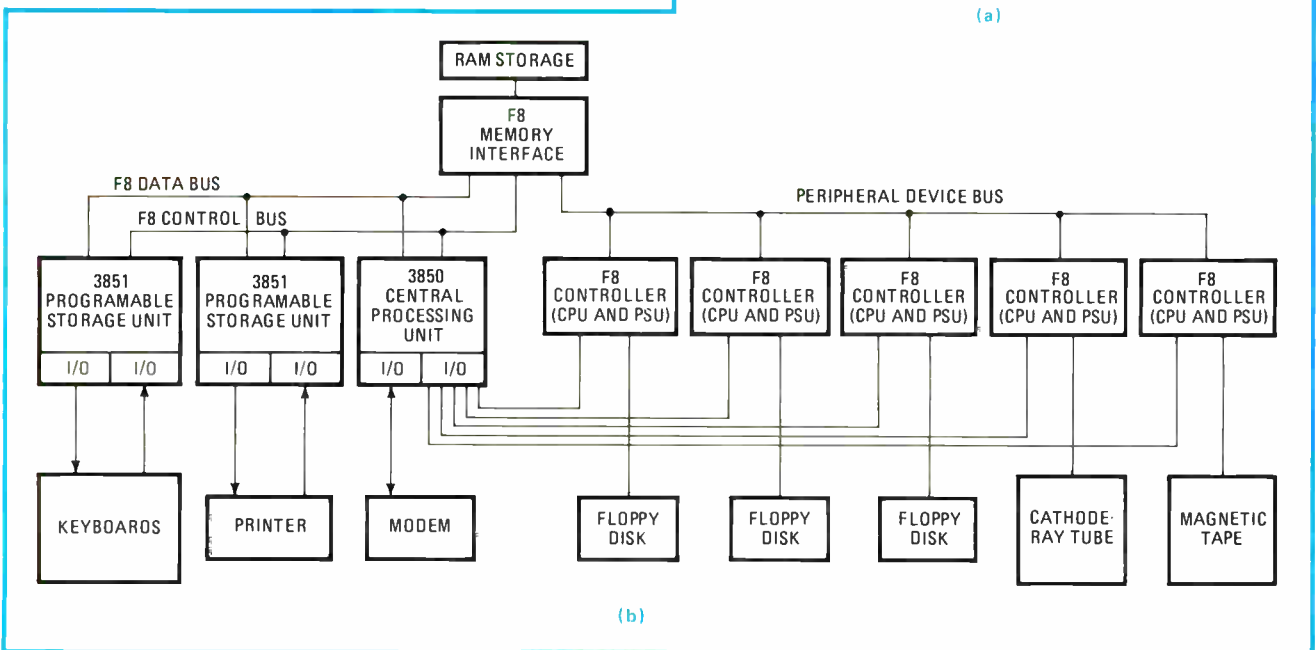
Because various logic functions are distributed among the four peripheral chips, the CPU contains only the arithmetic/logic unit, the control unit and instruction register, the logic associated with interfacing the system bus with the I/O control signal, and the accumulator register. It does not contain memory-addressing logic, memory-addressing registers, stack pointer, program counter, and data counter, all of which reside in the companion memory and memory interface chips.

This configuration has both advantages and disadvantages, the chief advantage being that fairly powerful systems can be implemented with remarkably few chips.

Moreover, the lack of memory-addressing logic on the CPU chip itself means that no address lines are needed on the system bus, and the 16 address signals, which CPU-oriented systems need to interface with the bus, can instead be used for two 8-bit I/O ports on each

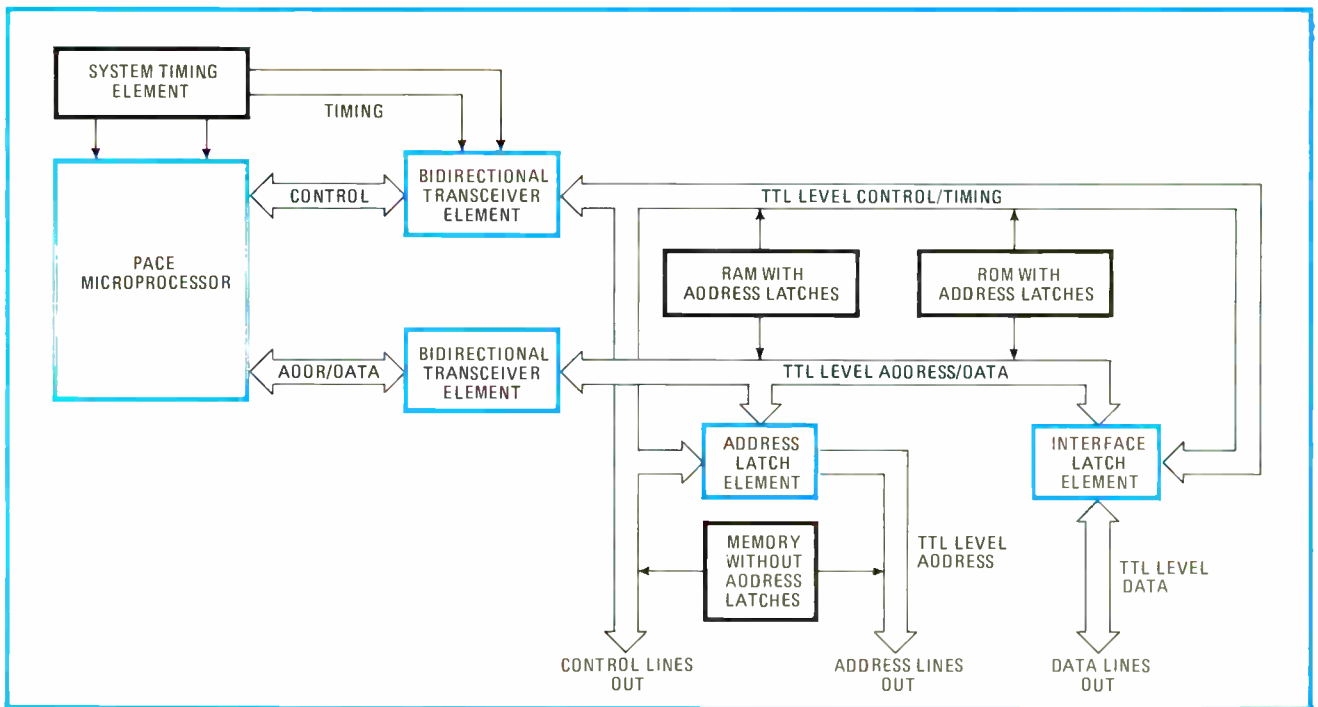


(a)



(b)

5. Efficiency experts. SC/MP and F-8 carry off the prize for minimum-chip multiprocessor systems. This SC/MP configuration (a) from National daisy-chains several microprocessors along one bus. The Fairchild F-8 disk controller has five F-8s operating as distributed processors. F-8 systems can readily be expanded to handle a wide variety of peripheral control and complex data communications applications.



6. Relating. National's 16-bit PACE system reaches the TTL world with transceivers that interface directly with any RAMs or ROMs designed with on-chip address latches. Standard memories can also be used if an 8-bit address latch element is included.

device. Better yet, the place on the CPU chip formerly occupied by address registers and memory-addressing logic can now accept 64 bytes of random-access memory. It is this on-chip RAM that makes an F-8 minimum two-chip configuration functionally useful.

Now for the disadvantages. Because of the removal of memory-addressing logic from the CPU chip, external memories can no longer be connected directly to the system bus, which no longer has address lines, and the family's other devices must be used. Of course, this is easily done with the memory-interface devices, but the extra packages do add to the cost of the design. Worse yet, this memory-addressing logic must be duplicated if more than one memory device is present.

On the other hand, SC/MP (pronounced Scamp) centralizes its computing capabilities in the CPU, just like the 8080 and 6800 families, so that systems can be configured with standard memories directly. The SC/MP chip can handle up to 4 kilobytes of memory with no additional logic or interface packages. Systems requiring more memory are also possible: a five-chip system, handling up to 65 kilobytes of RAM, would consist of the SC/MP, a two-chip bidirectional transceiver, an address latch, and a buffer.

Internally, SC/MP is a programmable 8-bit parallel processor. It contains one 8-bit accumulator, four 16-bit pointer registers (one of which is dedicated to the function of program counter), an 8-bit status register, and an 8-bit extension register. On-chip timing circuits eliminate the need for external clocks, and TTL compatibility allows easy interfacing with other system components.

Architecturally, SC/MP, again like the 8080 and 6800 families, employs a unified bus system, to which the central processing unit, memory, and peripheral devices are each connected. The common data bus enables

memory-reference instructions to reference peripheral devices. In addition, SC/MP architecture provides serial data and control streamlining under software control and has built-in programmable delay.

Both the SC/MP and F-8 families lend themselves to multiple processor systems. In SC/MP, the bus configuration is responsible, allowing many SC/MPs to be tied to the bus for daisy-chain operation (Fig. 5a). When one SC/MP stops transmitting or receiving, it notifies the next SC/MP in line that it may take over.

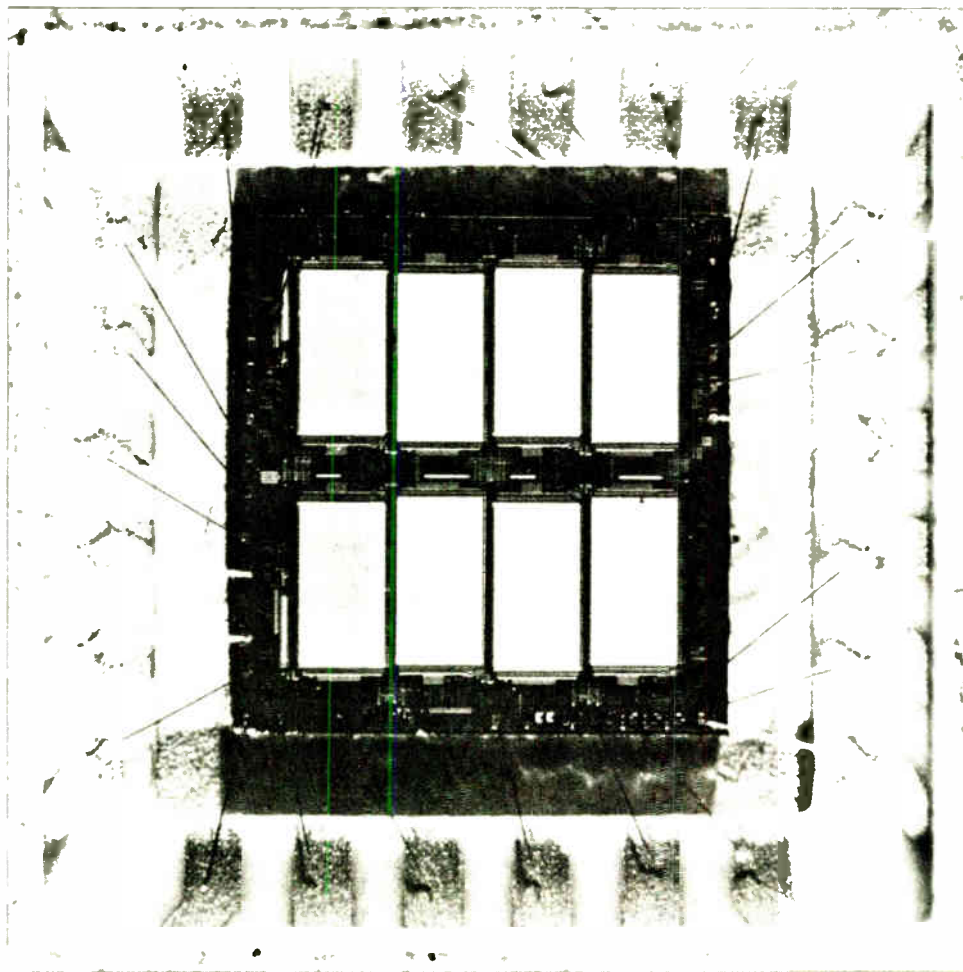
The F-8 CPU chips can serve either in a multiple processor system or in two-chip peripheral controllers subordinate to a multichip processor-based system, such as large point-of-sale terminals. The floppy-disk controller shown in Fig. 5b contains five F-8s working in conjunction with floppy disks, a magnetic-tape unit, a cathode-ray-tube display, a keyboard, printer, and modem. While the low-speed devices (the keyboard, printer, and modem) can be adequately handled by the programmed I/O structure, the other, high-speed devices require separate F-8 CPUs and programmable storage units.

The 8-bit newcomers

While established suppliers of microprocessors have recently come out with upgraded products—most notably the 8080A and 6800D—newcomers to the field are trying to gain entry with still higher-performance versions of the earlier devices. A good example is Zilog Inc.'s Z-80 chip. In a tribute to the success of the 8080, designers at the Los Altos, Calif., company have based their design on it, but have added more data-processing and instruction-handling capability. At the same time, they have tried to simplify the system configuration along the lines of the 6800.

For example, the Z-80 is heavily CPU-oriented, like

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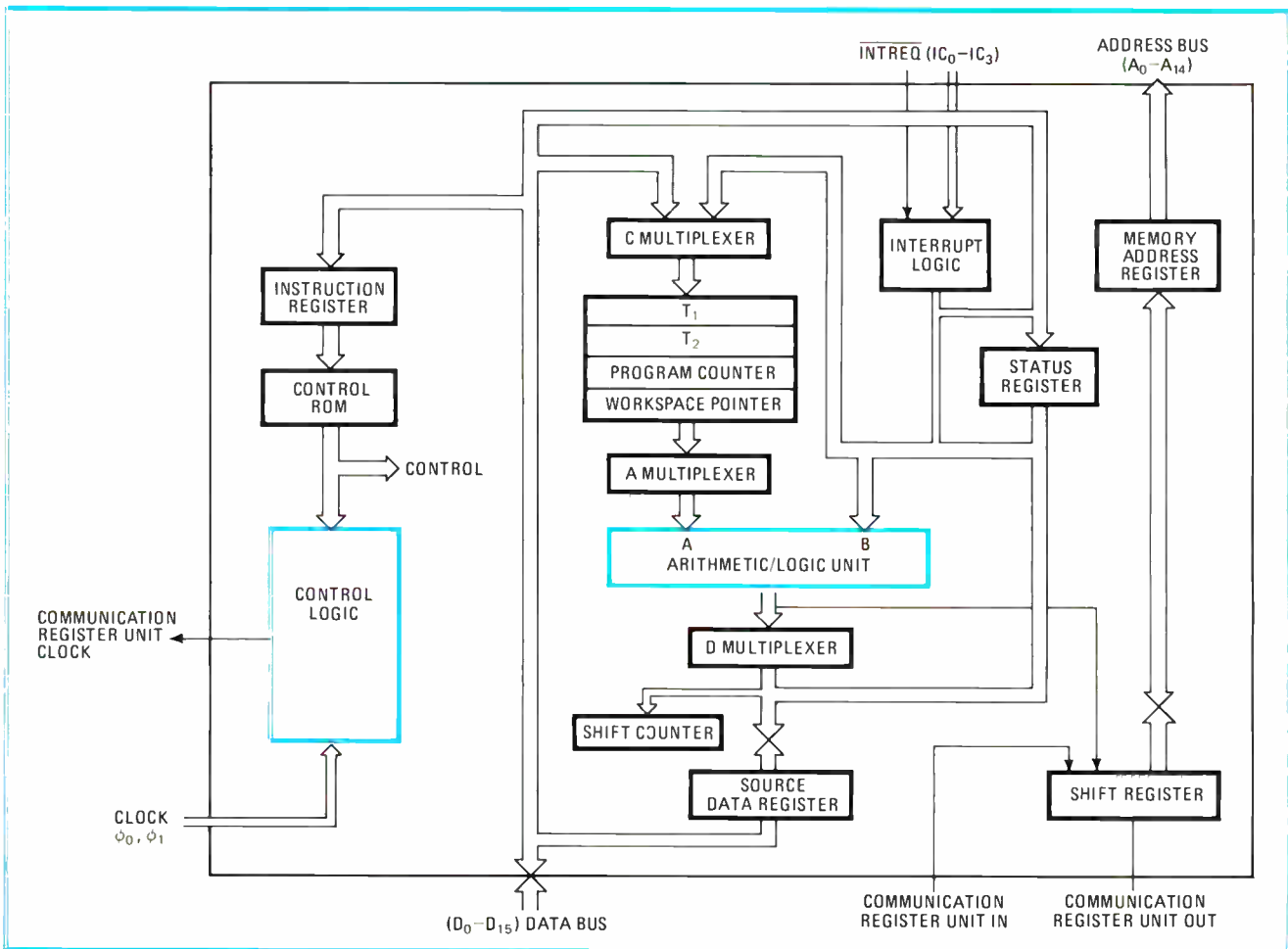
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7. Thinking big. Texas Instruments' 9900 16-bit microprocessor has full 16-bit data bus and 16-bit ALU on chip but exiles all general-purpose registers to external RAM locations. A wide range of interrupt capability is included, making the chip very flexible.

the 8080A, and is completely compatible with 8080A software. But thanks to depletion-mode technology, it, like the 6800, has a single-phase clock on the chip and requires only a single 5-v power supply.

The Z-80 can handle 158 different instructions and, like the 8080A and 6800D, has an internal 16-bit-wide data bus. Unlike them it contains both an 8-bit and 16-bit external address bus, so that it can process either 8- or 16-bit words in one cycle.

Architecturally, the Z-80's CPU chip resembles the 8080A, where general-purpose registers perform basic computation operations and special-purpose registers perform various program operations, such as program counting and stack pointing. Also as in the 8080A, the CPU contains the accumulator and flag registers.

The Z-80's block of general-purpose registers has a distinctive feature: it consists of two matched sets of six 8-bit registers. Now a programmer can use them individually, as 8-bit registers, or in tandem as 16-bit register pairs, depending on whether he is handling 8-bit or 16-bit words. Moreover, the programmer may select one set of registers for a single exchange command while using the other set for the rest of the sequence. This saves interrupt time—and is especially useful in systems that require a fast interrupt response—because there's no need to transfer the register contents to an external stack dur-

ing the fast-cycle interrupt or subroutine processing.

As for the Z-80's special-purpose registers, the program counter and stack pointer function much as they do on the 8080A. The program counter holds the entire 16-bit address of the current instruction just fetched from memory, and the stack pointer keeps track of the 16-bit address of the current instruction. An external stack memory, organized as a last-in/first-out file, allows simple implementation of multiple level interrupts, unlimited subroutine testing, and simplification of many types of data manipulations.

Like the Z-80, another recently introduced microprocessor that takes cognizance of established 8-bit general-purpose designs is the 9002 from Electronic Arrays Inc., Mountain View, Calif. But unlike the Z-80, which is being supplied with its own set of dedicated support devices, the 9002 has been conceived as a stand-alone digital process controller that can interface with standard peripheral chips through an 8-bit parallel TTL-compatible data bus.

The 9002 timing and control signals allow a user to bring the chip together with any bus-oriented peripheral devices he may choose. Examples are: Motorola's 6820 peripheral interface adapter for general-purpose controller applications; the asynchronous communications interface adapter and low-speed modem for

Learning about microprocessors

In approaching the design of microprocessor systems, the first requirement for the novice is to learn the specialized jargon. The basic terms defined below can help. They are followed by some advice on the next steps in an education in microprocessor theory and applications.

Central processing unit: a group of registers and logic that form the arithmetic/logic unit plus another group of registers with associated decoding logic that form the control unit. Most metal-oxide-semiconductor devices are single-chip CPUs, in that the registers hold as many bits as the word length of the unit (the 8080 and 6800, for example, are 8-bit devices and thus the basic registers are eight bits wide). With bit-slice devices, however, central processing units of any bit width can be assembled essentially by connecting the bit-slice parts in parallel. Externally, a bit-slice device will appear to be a coherent single CPU capable of handling words of the desired bit length.

Register: logic elements (gates, flip-flops, shift registers) that, taken together, store 4-, 8-, or 16-bit numbers. They are essentially for temporary storage, in that the contents usually change from one instruction cycle to the next. In fact, much of the microprocessor's operation can be learned by studying the registers, which take part in nearly all operations.

Accumulator: a register that adds an incoming binary number to its own contents and then substitutes the results for the contents.

Program counter: a register whose contents correspond to the memory address of the next instruction to be carried out. The count usually increases by one as each instruction is carried out, since instructions generally are stored in sequential locations.

Instruction register: storage for the binary code for the operation to be performed. Usually this instruction represents the contents of the address just designated by the program counter. However, the contents of the instruction register or the program counter may be changed by the computations. This, of course, represents one of the key ideas of a stored-program computer—instructions, as well as data, can be operated upon and subsequent operations will be determined by the results.

Index register: some memories are organized by index number (the contents of the index register). The address of the next instruction may be found by summing the contents of the program counter and the index register. Increasing the index register by one will cause the processor to go to a new section of memory.

Stack pointer: a register which comes into use when the microprocessor must service an interrupt—a high-priority call from an external device for the central processing unit to suspend temporarily its current operations and divert its attention to the interrupting task. A CPU must store the contents of its registers before it can move on to the interrupt operation. It does this in a stack, so named because information is added to its top, with the information already there being pushed further down. The stack thus is a last-in first-out type of memory. The stack-pointer register contains the address of the next unused location in the stack.

Flag: usually a flip-flop storing one bit that indicates some aspect of the status of the central processing unit. For

example, a carry flag is set to one when an arithmetic operation produces a carry. A zero flag is set when the result is zero. These flags aid in interpreting the results of certain calculations. Others are sometimes provided to permit access by interrupt request lines—for example, if a CPU is engaged in the highest priority of calculation, it may set all status flags to zero—which, loosely translated, means "don't bother me now." If only some of these flags are set, then only certain interrupt lines will be able to get through according to their priority.

Direct memory access: a technique that permits a peripheral device to enter or extract blocks of data from the microcomputer memory without involving the central processing unit. In some cases, a CPU can perform other functions while the transfer occurs.

In going beyond these definitions, an engineer will probably find that there's not an abundance of good basic information on microprocessors. However, the gap is filling.

Certainly, a first source on the details of a particular product is the manufacturer's product descriptions. Some of them are quite readable. Most provide easily understood introductions to the microprocessor, with just enough information to get started. Best known are Intel's "8080 Users Manual," Motorola's mammoth "Microprocessor Applications Manual" and 6800 System description, Fairchild's "F-8 Circuit Data Book," Signetics' 2650 manual, Rockwell's microprocessor family descriptions, and the descriptive literature National puts out on SC/MP, PACE, and IMP-16 families.

Independently produced sources also are available, but they're of varying quality. A useful one is a monthly publication on a variety of microprocessor subjects called "New Logic Notebook," edited by Jerry L. Ogden of Microcomputer Technique Inc., 1120 Reston International Center Office Bldg., Reston, Va. 22091. A monthly compilation of microprocessor news and product introductions is a newsletter called "Microcomputer Digest," P.O. Box 1167, Cupertino, Calif. 95014.

One of the best books is a paperback called "An Introduction to Microcomputers," from Adam Osborne and Associates, 2950 Seventh St., Berkeley, Calif. 94710. It has a compact tutorial section on basics, followed by good comparisons of key families.

Then there's "Microprocessors," first volume in the Electronics Book Series. It is a compilation of all the original articles on major microprocessor designs that appeared in this magazine—from the first 4004 to today's complex 8- and 16-bit designs. It also contains detailed design and application material. It's available for \$8.95 (see page 227).

A good source of basic information is the independent seminars that are becoming widely available. One of the most successful is Integrated Computer Systems' three-to-five-day courses held across the country. A schedule is available from David Collins at ICS, 4445 Overland Ave., Culver City, Calif. 90230.

An opportunity for hands-on experience is the suppliers' seminars. These are manned by applications specialists who travel around regularly, offering a good review of a particular microprocessor line. Finally, there are the courses offered by the IEEE and the universities.

communications-controller applications; or any of Intel's new programable interface devices, such as the programable peripheral or communications interfaces. This means that a system designer can use the 9002 as a powerful controller chip, managing the operation of any TTL-compatible peripheral device.

The 9002 designers also picked the best features of existing processor designs. The CPU combines the on-chip 64-byte scratch-pad RAM of the F-8, the push-pop subroutine stack of the Intel 4040, the simplified timing concepts of the PPS-4, the straightforward peripheral addressing techniques and single 5-V-supply requirement of the 6800, and the general-purpose registers of the 8080.

To these borrowed features the 9002 adds some purely its own. It contains a seven-level subroutine stack for multiple interrupt capability and eight 12-bit general-purpose data registers. With its 64-byte scratch-pad memory it can handle many stand-alone controller jobs without requiring additional RAM. Moreover, one of the 9002's internal flags allows the user to perform either 8-bit binary arithmetic or packed binary-coded-decimal arithmetic (dual 4-bit operands) with built-in, automatic decimal correction. To choose, he simply sets the flag in one state or another. This is useful for peripheral controllers where CRT displays need BCD data.

With all this computing power, ample control signaling, and on-chip RAM capability, the 9002 can realize many fairly powerful designs with only two or three packages. For example, a controller can be built with the 9002, a 1,024-by-8-bit ROM, such as the EA 4700, and two Intel 8212 peripheral interface chips, or else it can be built with the 9002, a 2,028-by-8-bit ROM, such as the EA 4600 and Motorola's 6820 PIA chip.

C-MOS: another choice

Another enhancement of an existing device is RCA Solid State division's single-chip version of its 8-bit C-MOS microprocessor. Designated the 1802, the chip is three times faster than the old two-chip design, has one third more instructions—a total repertoire of 91—and costs less. This came about thanks to RCA's new silicon-gate process that yields C-MOS devices almost half the size of metal-gate designs and also increases transistor switching speed. As a result, a C-MOS microprocessor becomes as fast, cost-effective and flexible as today's p- and n-MOS microprocessors.

To illustrate, the 1802 has a cycle time of 1.25 microseconds and takes only one or two cycles, plus a fetch cycle, to execute any instruction. This gives it an instruction time of either 2.5 or 3.75 microseconds that puts it well in the speed range of either the 8080 or 6800. Moreover, with its 91 instructions, it is as powerful and as flexible. Yet RCA designers were careful to retain the architecture of the two-chip design, so that the 1802 is software-compatible with its predecessor.

What distinguishes the 1802 CPU from other 8-bit designs is its separate instruction and address registers. The address data is placed in an array of sixteen 16-bit scratch-pad registers, each of which can point to either data or program. That means that a user is not forced to provide an address with each memory reference instruc-

What it costs

Like all semiconductor chips, microprocessor prices are coming down. Here's a rough guide to how much it costs to do some typical jobs at today's prices (in appropriate volumes):

Job	Number of packages	Cost
General-purpose		
minicomputer emulation	30 and up	\$1,000
Dedicated minicomputer	20-30	600
Process controllers	15-20	400
Smart terminal (i.e.		
communications, etc.)	10-15	300
Complex general controllers (i.e.		
traffic lights, medical, machine tool, etc.)	10-15	200
Complex peripheral controllers,		
industrial	10	150
Point-of-sale terminals	10	150
Games, instruments, etc.	5-10	75
Simple controllers, hobby gear,		
appliance control	1 or 2	10

tion—something he must do with other processors.

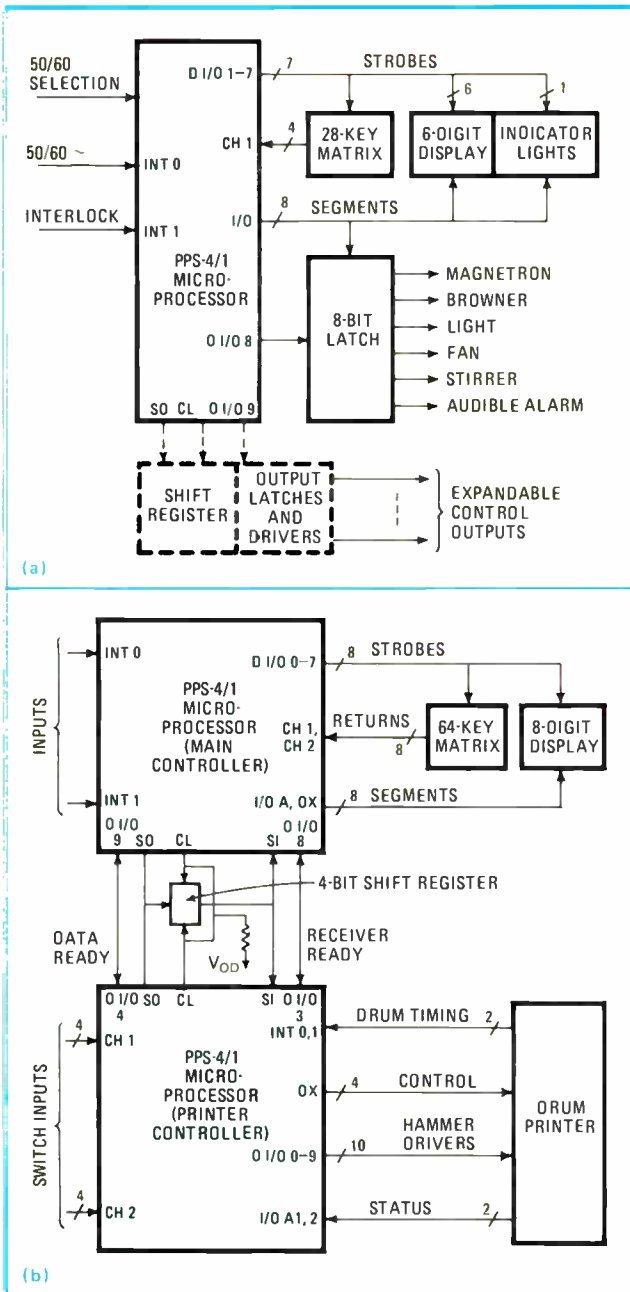
As address pointers, individual scratch-pad registers in the array are selected by any one of three 4-bit registers, so that the contents of any address can be directed to any one of three destinations. As data pointers, the 16 scratch-pad memories are equally flexible. They can be used either to indicate a location in memory or as pointers to support a built-in direct-memory-access function.

The only other C-MOS microprocessor is Intersil's 12-bit device. By using the same software as the PDP-8A, the device lets users of that popular computer implement their systems in low-power easy-to-use C-MOS technology. The 40-pin package has an instruction capacity of about 40, can access 32-k bytes of external memory, and can control 64 I/O parts. For the 1600, Intersil plans to supply a complete set of C-MOS peripheral devices, such as C-MOS ROMs, RAMs, and UARTs.

Two n-channel 8-bit microprocessors that have begun to make headway for general-purpose applications are the Signetics Corp. 2650 and the MOS Technology Inc. 6500 family of microprocessors. The Signetics part, available only in sample quantities about a year ago, lately gained momentum—especially in Europe, thanks in part to Philips' recent acquisition of Signetics.

The 2650 is a single 5-v parallel 8-bit binary processor capable of performing 75 instructions in a machine cycle time of 2.4 microseconds, which puts it in the same general class as the 8080 and 6800 families. The chip can address up to 32 kilobytes of external memory (compared to 65-k for the others). But its ability to execute variable-length instructions makes it somewhat more efficient, since a one- or two-byte instruction may often be used for memory addressing. Moreover, most instructions require only 6 of the first 8 bits, so the remaining bits can be used for the register field.

MOS Technology's family is unique in that it includes a number of software-compatible microprocessor chips differing primarily in the amount of memory they can address. The 40-pin 6502 can handle 65-k bytes of



8. Independence. Rockwell's PPS-4/1 handles many controller jobs almost by itself. Microwave oven controller (a) needs only an 8-bit latch to drive the high-current oven gear. Two PPS-4/1s (b) handle more complex systems like cash registers.

memory, as well as a large number of real-time interrupts, putting it in the class of the 8080 and 6800 families. For smaller systems, there's the 6503, a 28-pin device capable of addressing 4-k bytes while accommodating two interrupts. The 6504, also a 28-pin package, can address up to 8-k bytes of RAM and handle one interrupt, and the 6505, a 28-pin package, can address 4-k bytes with one interrupt.

All the chips are single 5-v depletion-load devices with on-chip clocks that operate with very fast 1-microsecond cycle times. Moreover, all can handle 55 instructions, have 13 addressing modes, contain true indexing capability, and come with direct memory access. And,

since all the parts use the same software, they allow a user to tailor his microprocessor selection to the size of his system.

Recently, MOS Technology has announced several peripheral chips that work directly with the processor chips. There's a combination RAM/ROM chip (6530)—the first to incorporate RAM, ROM, I/O, and an interval timer on a single chip. It contains 1-k byte of ROM, 64 bytes of RAM, and two 8-bit bidirectional peripheral interface ports. The timer is programmable from the CPU and has interrupt capability. Two other versions have no ROM but twice the RAM content.

The only single-chip 8-bit bipolar microprocessor on the market is the SMS 300, from Scientific Micro Systems Inc., Mountain View, Calif. A recently introduced version cuts the original cycle time by 20% to 250 ns, so that the device can now, for example, directly control double-density floppy-disk units.

More performance

The 8-bit microprocessor has undoubtedly caught on—it fits many of the controller and medium-sized data-handling jobs that formerly went by default to mini-computer designs. But the 8-bit word length can be a handicap for large systems, where big bytes of memory must be processed, or in high-performing data-acquisition systems where speed and high resolution are needed. This is where the 16-bit microprocessor comes in: its 16-bit words reach external memory locations two bytes at a time, while its long words can easily accommodate the 10-, 12-, and 14-bit converter resolution that's standard for most systems.

National Semiconductor Corp. was the first semiconductor manufacturer to recognize the value of the 16-bit systems. In fact, the industry's first microprocessor above the 4-bit level was National's IMP-16, introduced in 1973 and still a viable product today. (The company is redesigning the IMP-16 with bipolar technology for ten times faster performance.) Though among the most powerful and flexible, the IMP does, however, need rather a large number of chips to implement most systems—the CPU alone uses five. The company therefore began working on a single-chip version of IMP, producing another industry first—the one-chip 16-bit PACE.

The first 16-bit CPU on a chip

PACE is software-compatible with IMP and retains many of its features. Like IMP, PACE provides 16-bit instruction and address processing plus a choice of either 8-bit or 16-bit data processing. In addition, many CPU-related operations, for which IMP needed external TTL packages, are included in the 40-pin PACE chip—for instance, status and control registers, instruction branching, interrupt logic, and clock generation (although some clock logic is still needed). Thus, a six-chip PACE system, including a ROM for program control and four 1,024-bit RAMs with on-chip latches for data storage, can run a powerful data-processing terminal containing 16-kilobits of program storage and 4-kilobits of data RAM. Such a terminal would previously have needed either dozens of TTL packages or, in an 8-bit micro-

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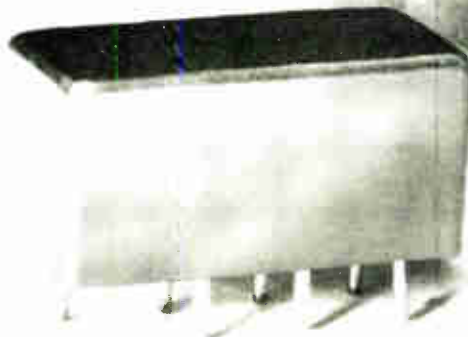
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One octave from band edge	5.5	7.5
Total range	6.5	8.5
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Lower band edge to one decade higher	LD-RF: 50	35
Mid range	LD-RF: 45	30
	LD-RF: 45	30
	LD-IF: 40	25
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Min. Electronic attenuation (20 mA) 3 dB

Signal, 1 dB compression level + 1 dBm

Impedance all ports 50 ohms



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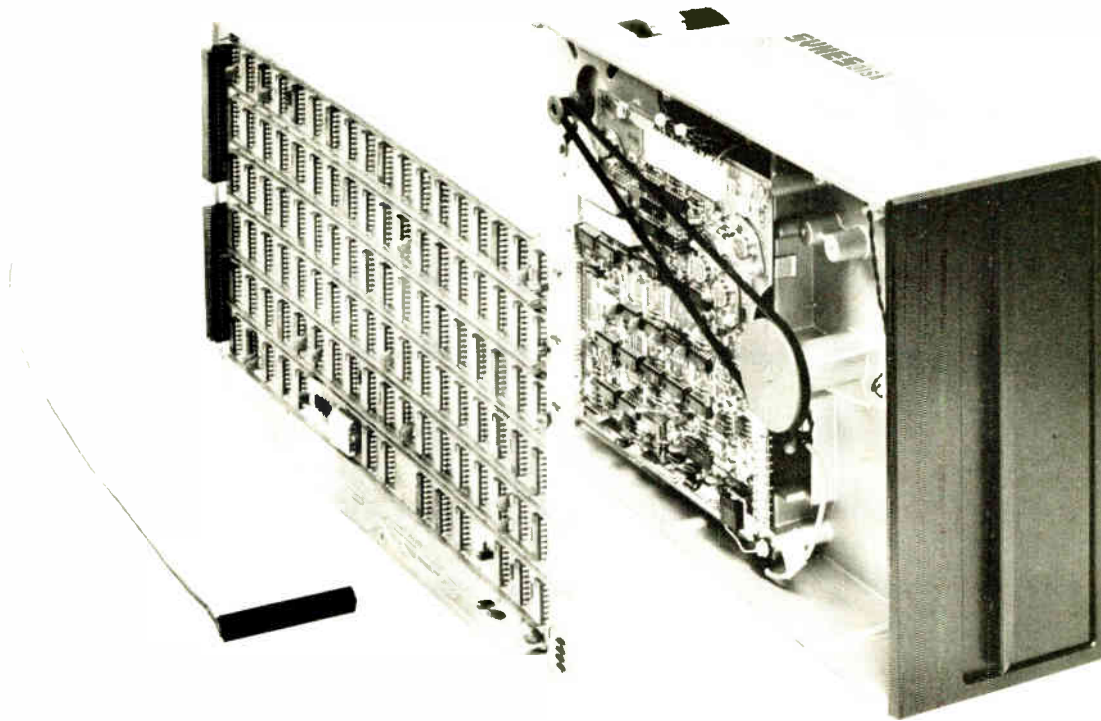
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processor-based design, longer programs, more memory and more interface chips.

Indeed, because its 16-bit capability can process two 8-bit words at a time, PACE can supply faster throughput to many designs now using 8-bit microprocessors. Moreover, a 16-bit system can work with shorter programs using less memory. Clearly, a user must analyze all system requirements—program length, memory, and peripheral functions—before he can be certain whether an 8- or a 16-bit design is better for his purposes.

For example, in complex, high-speed, data-processing terminals or in large point-of-sale and industrial process-control systems, an 8-bit CPU system may require double-precision arithmetic to attain the necessary data accuracy. Moreover, in 8-bit designs, multiple registers must be provided if 16-bit memory addresses and multiple accesses to memory are used to fetch multibyte instructions.

Besides PACE, National supplies a set of matched LSI chips that hook onto a TTL-compatible PACE bus system. A typical PACE system is shown in Fig. 6. Included in the family are a system timing element, for generating the clock signals, and a bidirectional transceiver element, for converting PACE's p-channel MOS signals to the TTL levels required by the TTL bus line. (These level converters will be eliminated in n-MOS versions of PACE that are in development.) Since the address and data lines are multiplexed on the PACE CPU, there are also an interface latch element, actually an 8-bit-wide demultiplexer that selects and retransmits data outputs, and an 8-bit address latch element, which does the same demultiplexing job for the address outputs. These system-matched components, together with external ROM and RAM, form the PACE 16-bit system. No TTL parts are needed for most system designs.

Designed for power

An even more powerful 16-bit microprocessor is Texas Instruments Inc.'s 9900, which was designed for TI's minicomputer division and is now available on a microcomputer board or as a lone chip. Its use of advanced n-channel processing results in very fast (3-megahertz) clock operation, and its minicomputer-like CPU design results in efficient register-to-register computation and direct memory-to-memory data transfer.

This method of handling data permitted the 9900 designers to remove from the chip all general-purpose registers, along with their associated 16-bit parallel buses (Fig. 7). Their functions are instead assigned to locations in external RAM, and room is made available for several powerful special-purpose registers—accumulators, pointers, index registers and the like.

This configuration has several advantages. For one, the incorporation of working registers in memory produces a memory-to-memory architecture that makes for very flexible programming. For another, the beefed-up special-purpose or housekeeping registers enable the CPU to handle up to 17 interrupts, 15 of them external plus two pre-defined ones. (Four bits in the status register store the priority of the interrupt currently being serviced.) Also, seven addressing modes are available.

Finally, the 9900 has separate address and data bus

lines, so that external demultiplexing devices are not needed, unlike in the PACE system. The chip operates efficiently with standard memories and many standard peripheral circuits, whether TTL-compatible MOS packages or standard TTL circuits.

Clearly the architecture of the 9900 is fundamentally different from most 8-bit general-purpose processors, including the 8080 and 6800. Whereas the 8080 employs conventional stack architecture, with the program and data spaces in external memory, the 9900 puts not only the program and data spaces but also the general-purpose registers in external memory. There are two basic advantages to such an architecture, especially for large systems. First, the number of workspace register files is not fixed, as it is on the 8080. Second, interrupt handling can be very fast, since all data used in program execution is contained in memory.

Another 16-bit microprocessor gaining in popularity is General Instrument Corp.'s CPI600. It's a more conventional general-purpose CPU that can handle instruction cycles about as fast as the 9900, but keeps its working registers on the CPU. These eight 16-bit registers operate either as accumulators or as memory stack pointers, in this respect behaving very much as in RCA's 1802 8-bit design.

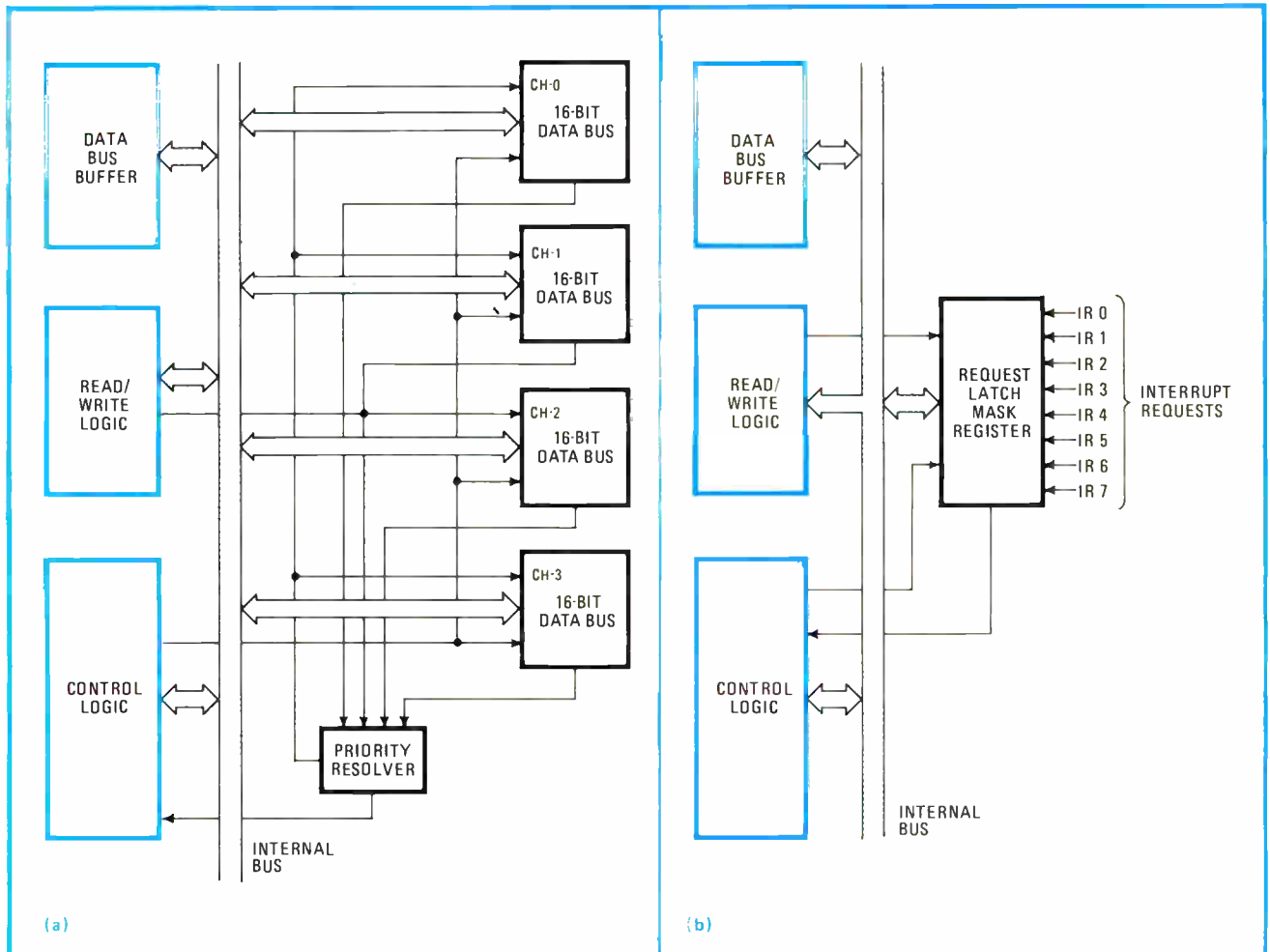
A strength of the CPI600 is its sophisticated interrupt system which yields fast service but has low hardware and programming overhead. Both interrupt servicing and priority programming within the CPU are handled by stack processing on command from the stack pointer.

Finally, in the 16-bit area, the Western Corp. MCP 1600 microprocessor, which originally was designed for DEC's LSI-11 microcomputer, is also available as an independent device. Like the other 16-bit chips, it is an n-channel MOS device that can be microprogrammed for control applications, or programmed to emulate most minicomputers. It differs from the other 16-bit designs by its use of three matched LSI chips to make up the processor: a data chip (1611B), a control chip (1612B), and a ROM program chip.

The three chips are interconnected by an 18-bit microinstruction bus that provides bidirectional communications between them for address and instructions. An additional data-access bus uses a 16-bit port for communicating with memory, input/output devices, and other system components.

The one-chip controller

Even while microprocessor manufacturers are moving up into the 16-bit minicomputer region, others are extending the technology in the other direction to the stand-alone controller. These new self-contained single-chip controllers provide the cheapest solution to a host of small control applications—in appliances, low-cost instruments, such as digital thermometers, and gear that requires a minimal amount of data processing, such as calculators, gas pumps, cash registers, and scales. Since the level of performance required is not too high, even a single low-cost chip can contain enough CPU, program ROM, data RAM, and I/O capability to handle most small-to-medium controller applications on its own. TI and Rockwell already have 4-bit controller chips on the



9. New talents. Programmable peripheral circuits are extending the capabilities of CPU-oriented microprocessor systems and at the same time simplifying them. The programmable interrupt controller (a) can handle up to eight vectored priority interrupts, while the programmable direct-memory controller (b) can access or deposit data directly from or into memory. Intel makes both for use with its 8080 family.

market, and other manufacturers are expected to announce 4- and 8-bit designs shortly.

But bear in mind, there is an overlap here. Clearly minimum-chip microprocessors, like the F-8, SC/MP, or the 9002, could be used to implement controller systems. But their processing power might be wasted in too small an application—they're better in configurations of at least two and usually three or more chips.

The first single-chip processor to have been designed specifically as a stand-alone controller is Rockwell's PPS-4/1. Several of these small microcomputers can also act as peripheral controllers in large systems, such as point-of-sale and communications terminals, to take the load off the central processors.

Each PPS-4/1 chip contains 10,752 bits of read-only memory, 384 bits of random-access memory, and 31 input/output ports. That's more on-chip I/O capability than is available on the single-chip 4-bit controllers originally developed for calculators. Also adding to the chip's versatility is a large set of 50 instructions and compatibility with Rockwell's older general-purpose PPS-4 and recent two-chip PPS-4/2 systems.

In more detail, the PPS-4/1's program memory is a 1,344-by-8-bit mask-programable ROM while a 96-by-4-

bit RAM provides data, parameter, and working storage. Data is processed by the chip's accumulator, functioning as the primary register, and five-register arithmetic/logic unit, which, together with a carry register, combine to perform either binary arithmetic or decimal arithmetic.

The efficiency with which such a chip can serve a controller is illustrated in Fig. 8. The microwave-oven controller (Fig. 8a) needs in addition to the PPS 4/1 only an 8-bit latch chip for the oven's mechanical controls—blowers, stirrers; and so on. A 28-key matrix supplies the controller inputs, while the strobe signals from seven of the chip's data output channels operate the 6-digit display and indicator lights. The eighth data output runs the latch. One interrupt line provides real-time clock inputs for accurately measuring cooking time, and the other interrupt provides an interlock input for turning off the oven when the door is open.

The cash-register design (Fig. 8b) shows how two or more controller chips work in one system. Here one PPS-4/1 operates as the main controller, the other operates as the printer controller, and the two communicate over any of the input/output lines, helped by a 4-bit serial shift register tied to the serial I/O lines of both chips.

A more ambitious (and more expensive) single-chip design is Intel's soon-to-be-available 8-bit microcontroller, the 8048. The Intel chip will contain all the elements of a microcomputer—CPU, program ROM, data RAM and I/O. But it will be both more powerful, because it contains an n-channel 8-bit ALU for handling over 80 instructions, and more flexible, because its on-chip control ROM is programable and alterable by the user. (Intel will also supply an unalterable version.)

The chip's PROM, a 1,024-by-8-bit configuration, is similar to the company's recently introduced 2708 erasable read-only memory, which the user can erase with ultraviolet light. Erasability has distinct advantages. Not only can a system designer program his ROM on the bench as his design progresses, but he may update or change that program at any time afterwards without exchanging one chip for another.

Besides the ALU, data registers, and PROM, the chip contains a 512-bit static RAM for scratch-pad data handling, a programable interval timer, and I/O channels. Moreover, it can address up to 2,048 bits of external RAM. Thus, a designer can use either the 8048's own 64 bytes of RAM in stand-alone controller applications or an external 256 bytes of RAM in more complex systems.

Besides being useful as a stand-alone controller, the 8048 works well as a peripheral controller in 8080 distributed processing systems. The powerful 8080 CPU chip acts as the main microprocessor, handling the central computation and providing the control signals needed to run the peripheral controllers and programable I/O and interface circuits. In point-of-sale systems, for example, several 8048s would provide the control logic for cash registers, credit-card validators, and inventory accounting, while the 8080 would handle the number crunching and central processing operations.

While Intel alone will offer a field-programable 8-bit controller, other suppliers are developing mask-programable devices. Rockwell, for example, will soon have a one-chip software-compatible controller (PPS-8/1) for its PPS-8 product line, and National is developing a single-chip SC/MP system. Fairchild will offer a one-chip 3860 controller for its F-8 line. Fairly typical of this class, the 3860 will have 2 kilobytes of ROM, 64 bytes of RAM, 32 I/O ports, interrupt capability, programable timer, clock circuit, and power reset.

The bottom line: calculator types

Texas Instruments led the way in making the TMS 1000—originally developed for its line of programable calculators—available as a stand-alone microcontroller. Now other calculator firms, such as Rockwell and National, are preparing calculator-type controller chips. Generally smaller and cheaper than the more powerful stand-alone 4- and 8-bit controllers, they work best in slow-input equipment, like keyboards or clocks.

But the TMS 1000 is still quite powerful. Introduced about 18 months ago, the p-MOS device is in heavy demand as a high-volume low-cost 4-bit serial controller. Several software-compatible versions are available: a 28-pin TMS 1000 with 1,024 bytes of ROM and 64 bytes of RAM; a 40-pin TMS 1200 with more I/O; the TMS 1070 and TMS 1270, which have high-voltage output

capability for directly driving displays, and the TMS 1100 and TMS 1300, which have twice the memory of the others. TI also plans enhanced n-channel versions.

National's line of 4-bit calculator-type controllers will start at the high performance end with the MM7581 and 5782 chip set. The first chip has 2-k bytes of ROM, ROM address and control logic, and some I/O; the second chip contains the ALU, a programable-logic-array instruction decoder, a 160-by-4-bit RAM, some RAM registers, and a serial I/O port. A lower-priced single-chip combination, the MM5799, will offer 1,536 bytes of ROM and 96 by 4 bits of RAM, and last in line will come a very low-priced MM5734, with less memory.

Rockwell's calculator-like controller line is aimed at applications below the capability of its single-chip PPS-4/1 controller. Coming soon is the A76XX, which will have about half the PPS-4/1's ROM and RAM capability and a slightly smaller instruction set. It is intended to sell in the \$5, high-volume range.

I/Os with intelligence

While microprocessor suppliers are answering the call for lower-cost controller chips on the one hand, they are also satisfying the demand for more I/O and peripheral flexibility in general-purpose systems. Rockwell, for example, has paid close attention to I/O and peripheral support. In its PPS-8 family, besides the CPU chip, clock generators, and memory modules, there are a general-purpose I/O chip, parallel-data, serial-data, direct-memory-access and printer controllers, a telecommunications data interface, as well as a general-purpose keyboard/display and floppy-disk controllers, the last compatible with IBM's floppy disks. Again, all work directly on CPU control at system clock and voltage levels.

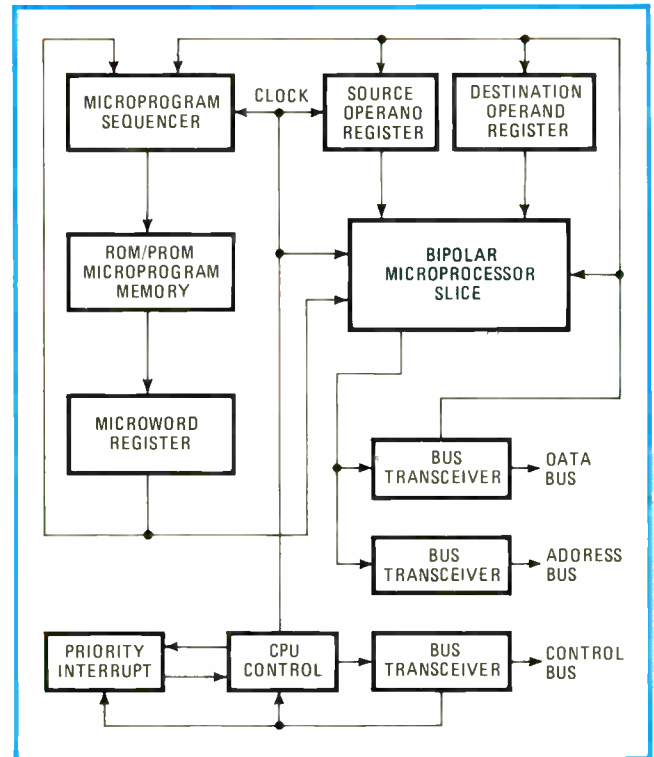
Motorola and Intel have been actively adding power and flexibility to their general-purpose I/O and peripheral devices. Since these chips can operate at TTL voltage levels, they will undoubtedly find markets outside of those of their families, especially with the new bus-oriented n-channel microprocessors.

The peripheral devices in Motorola's 6800 system have found wide acceptance in the industry. Included are the peripheral interface adapter, the asynchronous communications interface adapter, and the low-speed modem. Working with the CPU (or MPU, as Motorola calls it), ROM and RAMs, all on a single 5-v supply, these peripheral chips can implement many systems with a minimum of packages.

Intel's new 8080 peripheral devices have stirred interest because they are all software- or I/O-programable. These programable chips complement a large number of I/O devices, both TTL and MOS, that already are available, including an 8-bit I/O port, one-of-eight decoders, a priority interrupt control unit, and a 4-bit bidirectional bus driver.

Two of the programable chips are already available: a peripheral interface and a communications interface. Three others are coming: a programable interval timer, DMA controller, and interrupt controller (Fig. 9). The interrupt controller can handle eight levels of requests, and is expandable to configurations of up to 64 levels. The interval timer is actually a group of three independen-

BIPOLAR MICROPROCESSORS COMPARED				
Parameter	AMD Am2900	MMI MM6701	Intel 3002	TI SBP0400
Slice width	4 bits	4 bits	2 bits	4 bits
Functions of arithmetic logic unit	8	8	about 6	16
Number of microcode control inputs	9	8	7	9
Working registers	17	17	11	9
Two-address operation	Yes	Yes	No	No
Independent shift and arithmetic	Yes	Yes	No	Yes
Cycle time (register to register, read, modify, write)	100 ns	200 ns	150 ns	1,000 ns
Technology	Low power Schottky	Schottky	Schottky	I ² L
Power dissipation (4 bits)	0.92 W	1.12 W	1.45 W	0.13 W
Pin connections (4 bits)	40	40	56	40



10. However it's sliced. . . . In AMD's 2900 family of high-performance bipolar chips, the 4-bit processor slice is the key element in minicomputer configurations. The powerful 11-chip system can handle 16- or 32-bit-wide words for data-processing equipment.

dent 16-bit counters driven simply as I/O ports—instead of setting up timing loops in system software, a programmer can now satisfy his system timing requirements with a single chip.

Bit slices and microcomputer boards

While the MOS single-chip microprocessors are dominating control and data processing in small, medium-performance systems, the bipolar processor slices are taking on the tough process-control and high-speed controller jobs now handled by minicomputers.

Unlike MOS designs, a bipolar bit slice is only a section of a central processing unit. It is not intended to operate alone. A 16-bit computer design requires eight 2-bit slices or four 4-bit slices for the CPU, plus a host of peripheral input and output packages. These are usually standard TTL circuits, which are not available in low-cost LSI form and therefore add considerably to the cost of the system. Finally, bit-slice-processor designs generally require a lot of external memory—up to 64 kilobytes and more—and memory is expensive. In fact, a typical minicomputer CPU using the slice technique may need 15 packages costing about \$300.

Nevertheless, bit-slice activity is humming along, with several families already on the market:

- For stand-alone controls and minicomputers there's TI's integrated-injection-logic low-performance 4-bit processor slice. This chip, with 1,500 gates operating at delays of 25 nanoseconds, works with TI's existing family of TTL LSI processor parts. In addition, a 4-bit

Schottky TTL slice is to be introduced shortly, increasing speeds into the 1-to-10-nanosecond range.

- For high-speed processors and fast minicomputers there are the 2-bit and 4-bit Schottky TTL slices produced by a growing number of bipolar-circuit manufacturers (Fairchild, AMD, MMI, Raytheon, and Intel). These generally emulate existing minicomputers.

- Finally, there are the highest-performing emitter-coupled-logic processor slices for the control of big mainframe memories. Motorola has already announced a 4-bit ECL processor slice using its ECL 10K technology.

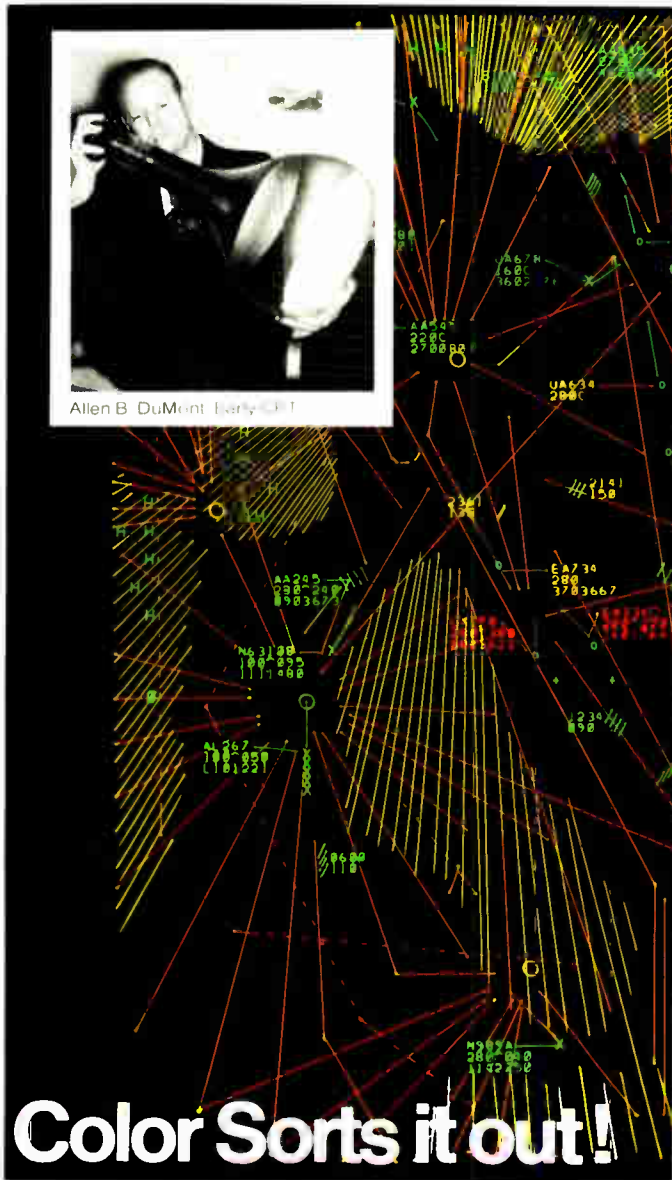
All this performance and flexibility do not come free. Bit-slice microprocessor designs are considerably more expensive than those built with MOS microprocessors.

The major asset of the bipolar LSI families is their processing power, which is far greater than that presently available from MOS microprocessors. By packing their processing power on several matched LSI chips, they are easily expandable to 16-bit or even 32-bit word lengths, and they can be microprogramed to handle the most powerful high-level instruction sets available.

No matter how different each new bit-slice system may appear, certain circuit blocks are common to them all. Besides the processor slice itself, there are the functions of control register, timing, slice-memory interface, and carry look-ahead. The control register always contains the logic necessary for microprogrammable control. It includes a 2- or 4-bit-wide data path, which can be expanded to larger words, plus enough storage and logic to address and control the memory circuits. It can also handle status, branching, and interrupt functions.



Allen B. DuMont, Early CRT



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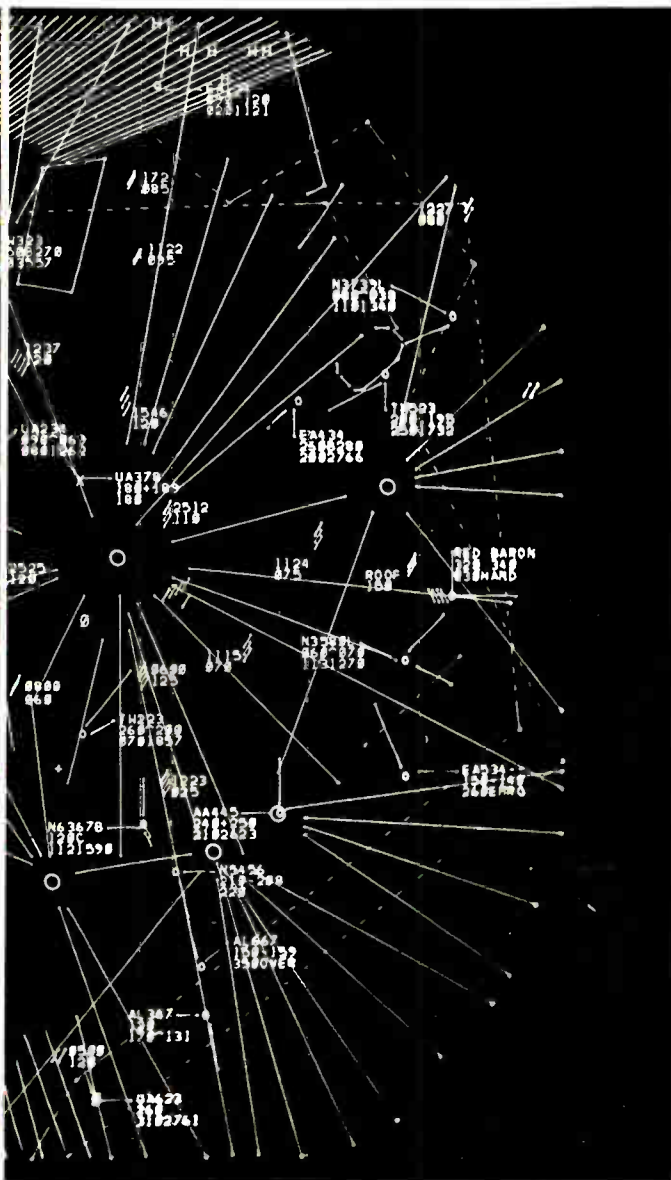


Figure 1: Air Traffic Control Presentation Courtesy CPS Inc.

For more than forty years, ever since DuMont introduced the commercially produced cathode ray tube (inset, above), professional users of high resolution CRTs have worked with only a part of their natural visual capacity. They have been limited by single-color phosphor screens. Multi-color screens have been available, but only in low resolution shadow mask and similar tubes.

Now, with the introduction of DuMont's proprietary P49 color penetration phosphor screen, professional users can have a vivid, four-color display AND high resolution—resolution comparable to that of high quality monochrome CRTs—with superior contrast and clarity.

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- Public utility power dispatching
- Nuclear reactor status

Electronics / April 15, 1976

- Municipal traffic control
- Military command and control
- Refinery/chemical process control
- Transportation control and dispatch

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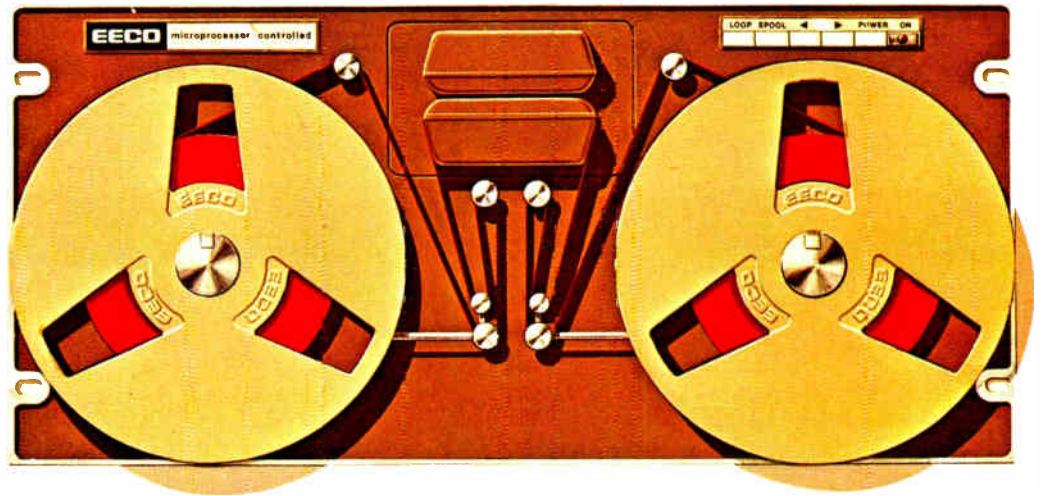
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In the arithmetic/logic-unit block, the computational logic sits side by side with data routing paths and the input/output ports that handle the control-register inputs and memory outputs. The timing function ties the other functions together by providing the various clock phases needed to drive all parts of the system.

But the systems generally differ in capability and speed (see table on p. 96). Almost in dead heat are the AMD 2900 and MMI 6700 designs. More points go to the AMD system, which can operate twice as fast off less power. Nevertheless, with 17 working ALU registers and two address operations, both systems offer the digital designer a large measure of high-quality design capability at very reasonable costs.

AMD's 4-bit slice is typical of processor-slice architecture, since it includes a high-speed ALU, a 16-word-by-4-bit two-port RAM (to handle the two-port address configuration), and all the associated circuit blocks for shifting, decoding and multiplexing. Crucial to the layout is the 9-bit microinstruction word-decode block that selects the ALU source operands, the required ALU function, and the ALU destination registers. Thus configured, the microcontroller can be cascaded either with full look-ahead logic capability or with ripple carry. Also, it has three-stage outputs, and it can provide various status flag outputs directly from the ALU.

Double address operation is made possible on the CPU chip by the two-port RAM and an ALU fast enough to handle concurrent input sequences in turn without slowing up the system. Essentially, any of the 16 words

of the RAM can be read from one of its ports under control of the address field input selector. Meanwhile, data from the other port is being read with the same code. Both data groups then appear simultaneously at the RAM port output for ALU processing.

Only 11 AMD chips are required to implement a typical central processing unit (Fig. 10). Four distinct data-processing functions are needed—the microprocessor slice, the I/O bus interface transceivers, the microprogram control, and the CPU control, including priority interrupt—plus whatever main memory is needed. These 11 chips replace about 200 TTL packages.

Motorola's ECL 4-bit-wide CPU chip design is sliced parallel to the data flow so that it, too, is fully expandable. The advantage of this approach is that the system can be extended both laterally to any bit length in increments of 4 bits and vertically. This kind of ECL pipe-line design achieves very high data throughput—rates of under 50 ns.

Configured somewhat differently from the Schottky TTL units, the slice contains a mask-programable latch network, the ALU, an accumulator, the shift network, input and output bus controls, and associated interconnections. This configuration copies most mainframe controller designs built with hardwired ECL packages.

To build or to buy?

Of course, engineers do have an alternative to putting together their own microcomputers from what might be a bewildering array of competing devices. For a reasonable cost (considering the design time, assembly, and testing), packaged microcomputer boards are available from essentially three types of sources:

- Semiconductor companies themselves are offering prototype boards and single-board microcomputers and microprocessors. Most notable examples are Intel's 8-bit SBC 80/10 [*Electronics*, Feb. 5, p. 77] and Texas Instruments' 16-bit 990/4 based on the 9900.
- Minicomputer manufacturers, growing concerned about the impact of the microprocessor on their low-end OEM business, have extended their lines downward. Their major weapons in this battle will be the quantities of development software that they have built up over many years and their ability to offer customers the option of moving upward to more complex systems while still maintaining software compatibility.
- Independent manufacturers of logic modules, such as PCS Inc., Flint, Mich., Pro Log Corp., Monterey, Calif. and Control Logic Inc., Natick, Mass., are offering microcomputers based on popular types of microprocessors (mostly the 6800, 4040, and 8080). There is also a host of smaller manufacturers who, having designed a microcomputer for internal use, have decided to try the microcomputer business. (With a microprocessor, almost anyone can call himself a computer manufacturer—and some of these companies will survive.)

There are many cost factors that may escape an engineer's notice in his flush of enthusiasm to get into microprocessor system designing. Besides extra hardware, he should also consider cost of software development, prototype test, incoming inspection, documentation,

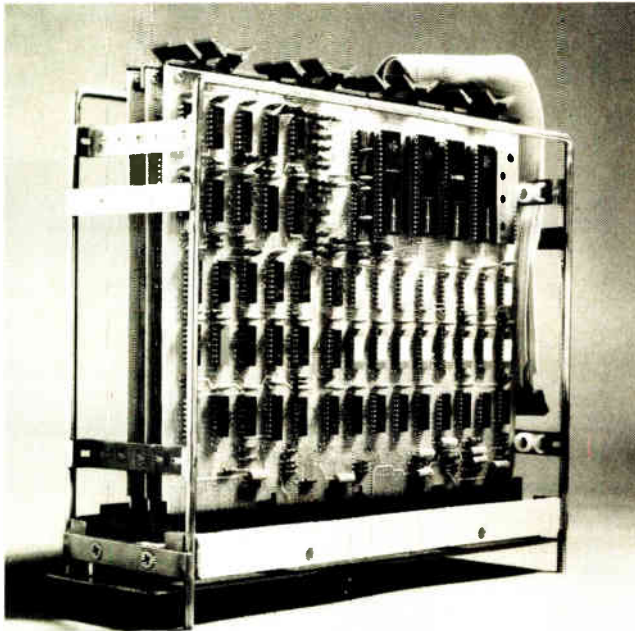
The let's-get-acquainted kits

An alternative to either buying microprocessors and designing your own system or buying fully packaged microcomputer boards is to buy an evaluation parts kit. They're available from all the semiconductor manufacturers as well as many independent sources. You can use them to familiarize yourself with a device before committing to it, and they can even be used for short production runs.

The kits typically include a CPU chip, a programable ROM chip, a RAM chip, I/O interface devices, additional circuits to complete the computer, and a printed-circuit board. Some semiconductor vendors also offer self-teaching aids, such as RCA's Micro-tutor, MOS Technology's KIM-1, and Texas Instruments' learning module. Such units will help an engineer learn machine language.

Another type of source is an electronics distributor. Cramer Electronics, for one, commissioned Microcomputer Technique Inc., Reston, Va., to design a set of parts kits called Cramerkits. Present versions use some of the most popular microprocessor types: several manufacturers' 8080s, Motorola's 6800, Texas Instruments' 9900, RCA's 1802, and Mostek's F-8.

Also, don't overlook the growing number of suppliers of hobby kits, such as MITS Inc., Albuquerque, N. Mex., with its Altair computers—the 8800, based on the 8080, and the 680, based on the 6800. MITS, in fact, is also active in software development, having recently introduced a version of the Basic language for interactive use on its computers.



11. Minicomputer maker's answer. Digital Equipment Corp.'s LSI-11 is a microcomputer built around custom MOS LSI chips. A member of the PDP-11 family, it runs the standard software.

production equipment, and special test equipment.

What an engineer must decide is whether he can do the same design job, and manufacture, test, and support his own microcomputers for less than he would have to pay for someone else's microcomputer. Intel, for example, sells its SBC 80/10 for \$295 in quantities of 100 (single units are \$495). Included, at that price, are the 8080A CPU, 1 kilobyte of RAM, sockets (only) for 4 kilobytes of ROM, two 8255 I/O devices allowing 48 programmable I/O lines, and interfaces (an 8251 serial interface device for a programmable communications line and interfaces for an RS-232 peripheral or a teletypewriter, plus clock circuitry and TTL circuits that are needed to complete the computer).

Texas Instruments, which has been in the minicomputer business for years, put it all together late last year when it sprung its 9900 16-bit microprocessor, and at the same time announced the 990/4 single-board microcomputer based on the 9900. For \$512 in quantities of 50, the 990/4 has the following major features: 8 kilobytes of memory, sockets for 2 kilobytes of programmable ROM or static RAM, and I/O interfacing through its communications register unit (CRU).

On the minicomputer front, Computer Automation Inc., Irvine, Calif. was an early entry with its Naked Milli, the LSI 3/05, built with TTL Schottky circuits. Although it does not use a microprocessor *per se*, its cost puts it in the same ballpark with many of the other one-board minicomputers. The CPU is built on a standard RETMA half-board and sells for \$295 in single units. With 1,024 bits of memory on another half board, the cost comes to about \$400. Computer Automation is proudest of its I/O interfacing scheme, which uses microprogrammable circuitry to tailor the I/O lines to any type serial or parallel peripheral device.

Digital Equipment Corp.'s LSI-11 is a 16-bit mini built around four MOS microprocessor chips custom-manufactured for DEC by Western Digital Corp. (But the Maynard, Mass., firm will probably soon begin its own production of the chips to serve as its own second source.) The LSI-11, at \$634 in 100 quantities, has a 4-kiloword RAM, a parallel I/O bus port, and other CPU circuitry on an 8.5-by-10-inch board. Aside from having the full weight of DEC's reputation behind it, the LSI-11 also has the full range of PDP-11 software going for it. More than about 20,000 PDP-11s of various sizes are in use, and it is a familiar computer in many OEM plants.

The latest minicomputer manufacture to slip in a one-board computer at its low end was Data General, Southboro, Mass. For its microNova, Data General is making its own 16-bit n-channel microprocessors in its Sunnyvale, Calif., semiconductor facility. As a member of the Nova family, the microNova runs all the already developed software. With 4 kilowords of memory, it sells for about \$570 in 100 quantities. Data General also says it will sell the microprocessor and memory chips separately, but this does not necessarily put the company in direct competition with semiconductor manufacturers. Users will likely first buy the complete boards. Later, when the volume justifies it, or when a different form factor is needed on the printed-circuit boards, the user will buy the chips, and assemble and test his own boards, still maintaining software compatibility.

At the other end of the microcomputer spectrum lie boards produced by the independents. Pro Log, for example, says it has the only logic processor system priced below \$100 (it's \$99 in quantities of 500). The system, PLS-401A, is a 4004-based system that includes a crystal clock, 80-character RAM, 16 lines of TTL input, 16 lines for output, and sockets for 1,024 words of memory. Pro Log essentially spans the Intel microprocessor line, offering computer boards with the 4040, 8008, and 8080, but it also has a 6800 board. □

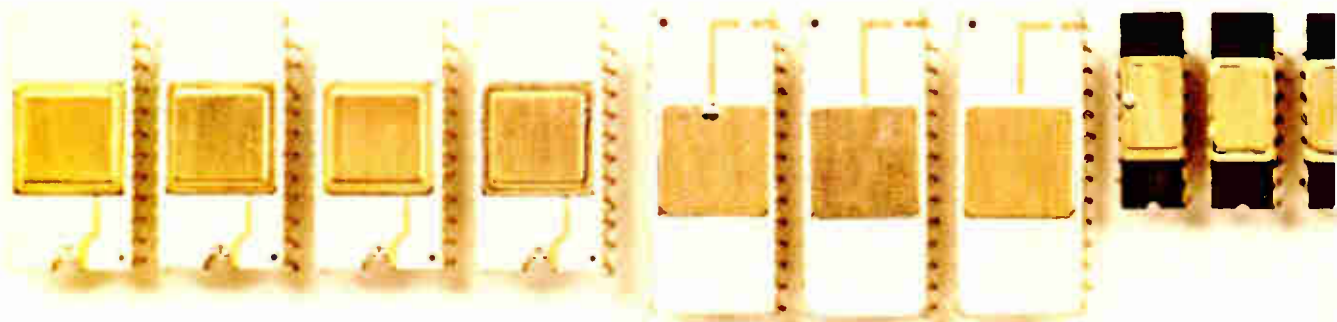
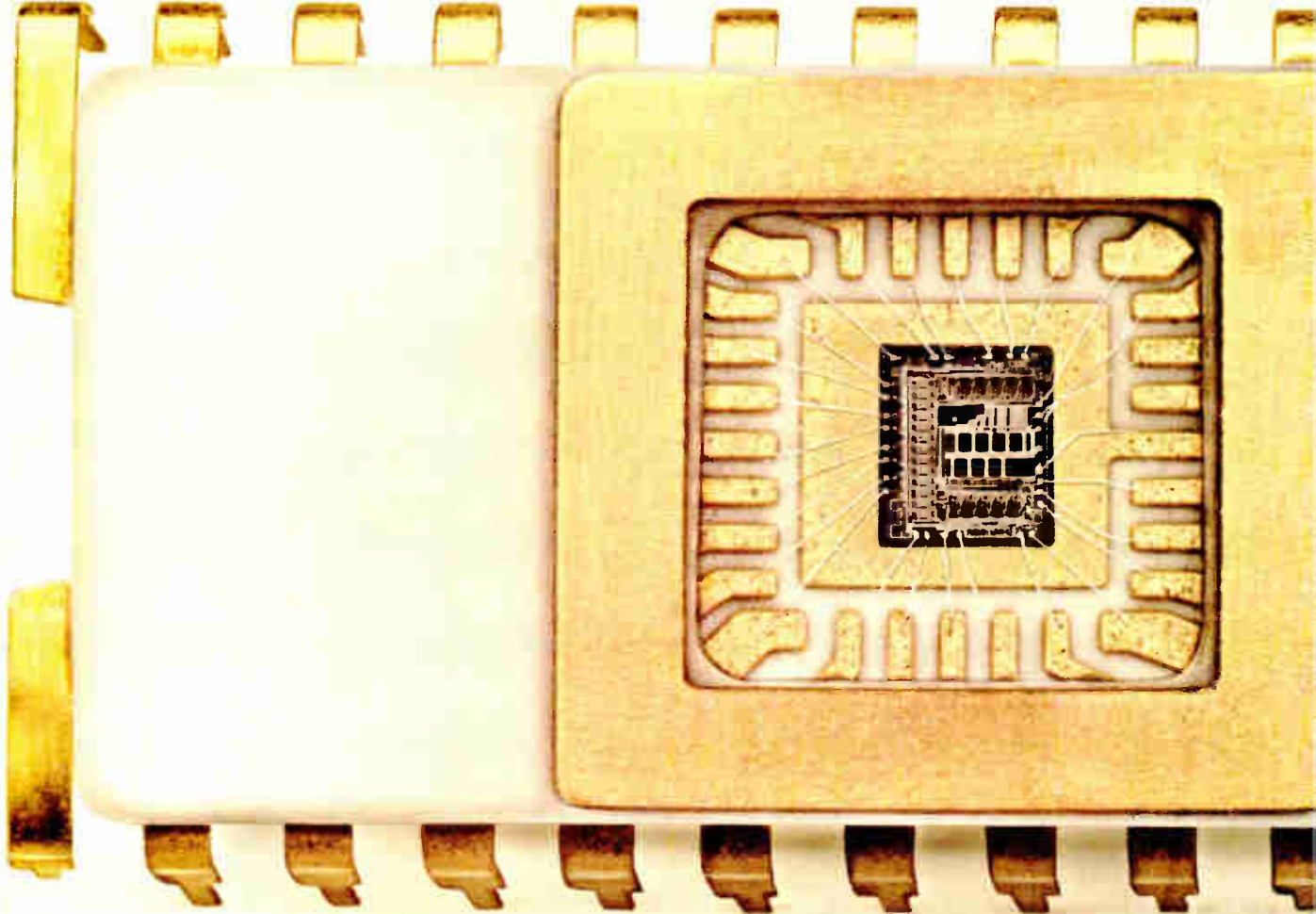
If you want to know more . . .

- Most of the major microprocessors have been covered in the pages of *Electronics*:
- Intel 4004 "Standard parts and custom design merge into four-chip processor kit," April 24, 1972, p. 112
 - Motorola 6800 "N-channel MOS technology yields new generation of microprocessors," April 18, 1974, p. 88
 - Intel 8080 "In switch to n-MOS, microprocessor gets 2- μ s cycle time," April 18, 1974, p. 95
 - Rockwell PPS-8 "Fast 8-bit microprocessor is versatile," June 27, 1974, p. 149
 - National PACE "Single-chip microprocessor employs minicomputer word length," Dec. 26, 1974, p. 87
 - Fairchild F-8 "Four-chip microprocessor family reduces system parts count," March 6, 1975, p. 87
 - Toshiba TLCS-12 "Twelve-bit microprocessor nears minicomputer performance level," March 21, 1974, p. 111
 - Intel 3000 "Bipolar LSI computing elements usher in new era of digital design," Sept. 5, 1974, p. 89
 - Texas Instruments SBP0400: "TIL takes bipolar integration a significant step forward," Feb. 6, 1975, p. 83
 - Monolithic Memories 6701 "Schottky-TTL controller put on a chip," March 7, 1974, p. 159
 - National SC/MP: "Scamp microprocessor aims to replace mechanical logic," Sept. 18, 1975, p. 81
- Information on software and design is provided in:
- "Designing with microprocessors instead of wired logic asks more of designers," Oct. 11, 1973, p. 91
 - "High-level language simplifies microcomputer programming," June 27, 1974, p. 103
 - "PLAs enhance digital processor speed and cut component count," Aug. 8, 1974, p. 109
 - "Preparation: the key to success with microprocessors," March 20, 1975, p. 101
 - "Microcomputer-development system achieves hardware-software harmony," May 29, 1975, p. 95
 - "The 'super component': the one-board computer with programmable I/O," Feb. 5, 1976, p. 77

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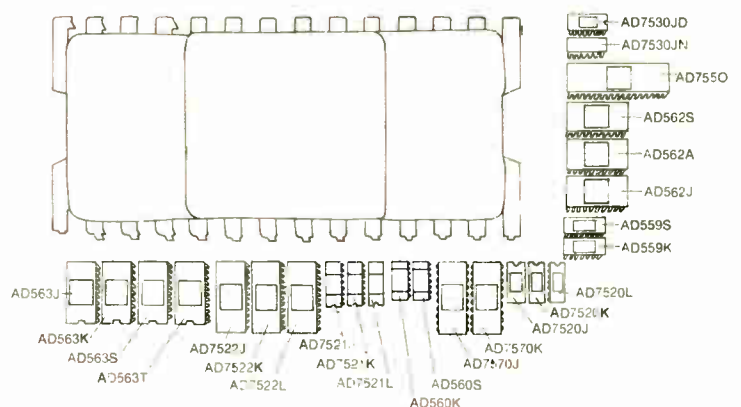
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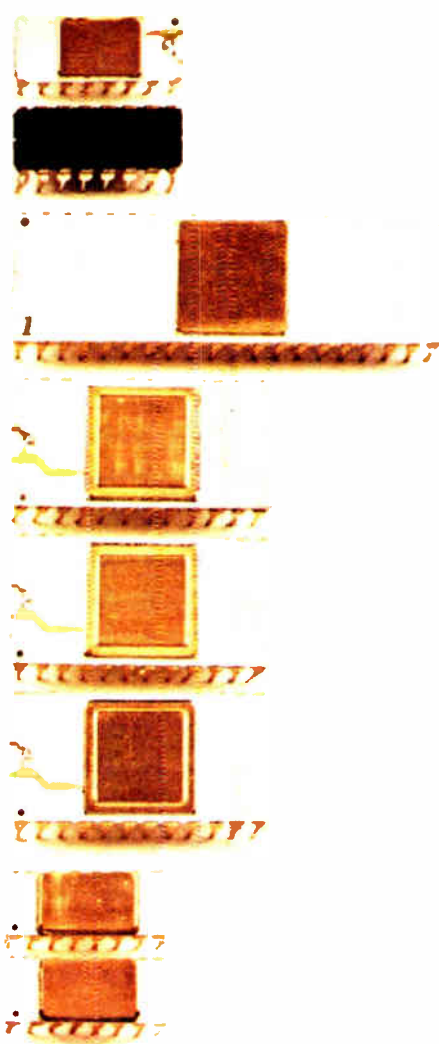
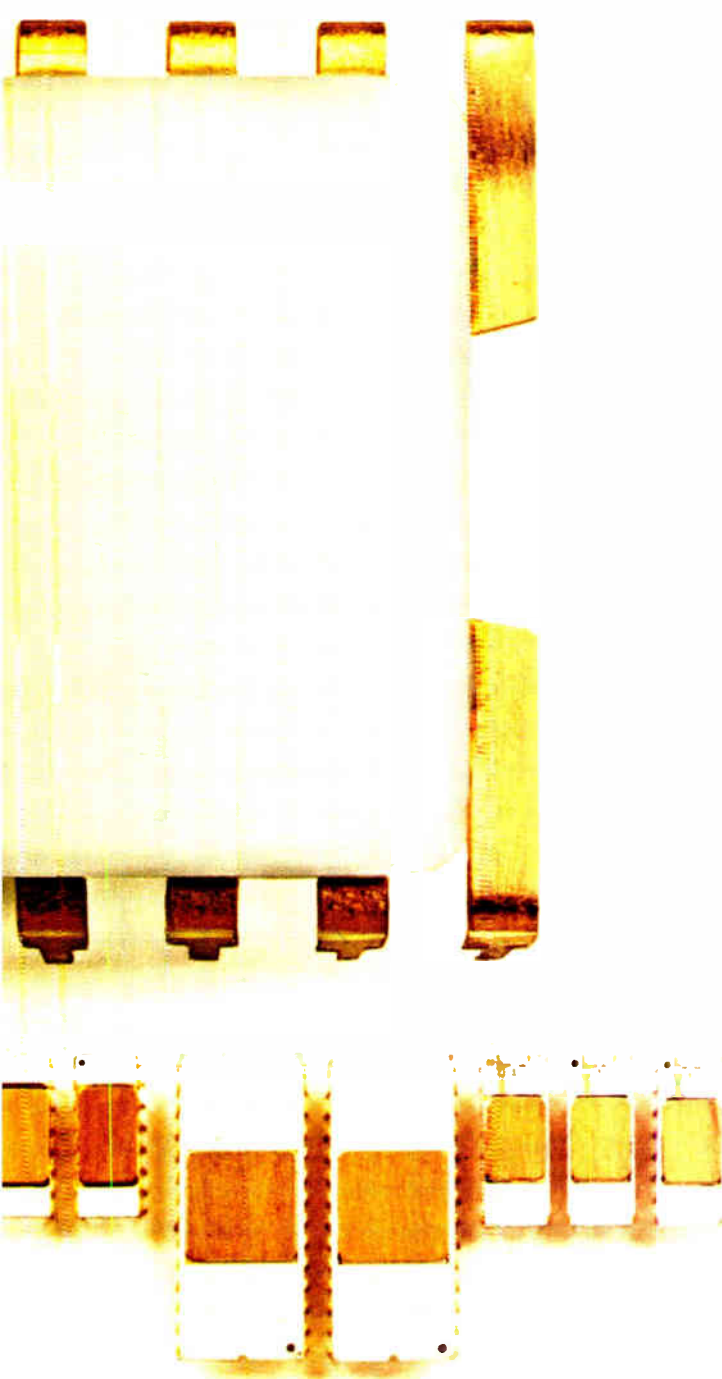
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MICROPROCESSORS

Software becomes the real challenge

It's true that microprocessors reduce hardware development time, but the tough task for the designer is now in programming and debugging. Even for the more experienced, software development is tricky. Learning to pick the right language level and how to work with it efficiently is essential.

Microprocessors simplify systems, but not the design process. "Hardware development time drops nearly to zero when you use a microprocessor. With the Intel 8008, we had a machine on the street in six months, and then with the 8080, we went from parts layout directly to final printed-circuit art work. But then the real design job started—writing and debugging the programs," says Frank Trantanella, president of Tranti Systems, a N. Billerica, Mass., maker of electronic cash registers.

Not all microprocessor system designs will involve so little hardware effort, but it is true that software is becoming of major importance in systems based on the device. The extent to which design engineers must immerse themselves in software-design methods depends on the intended uses of the systems they are developing.

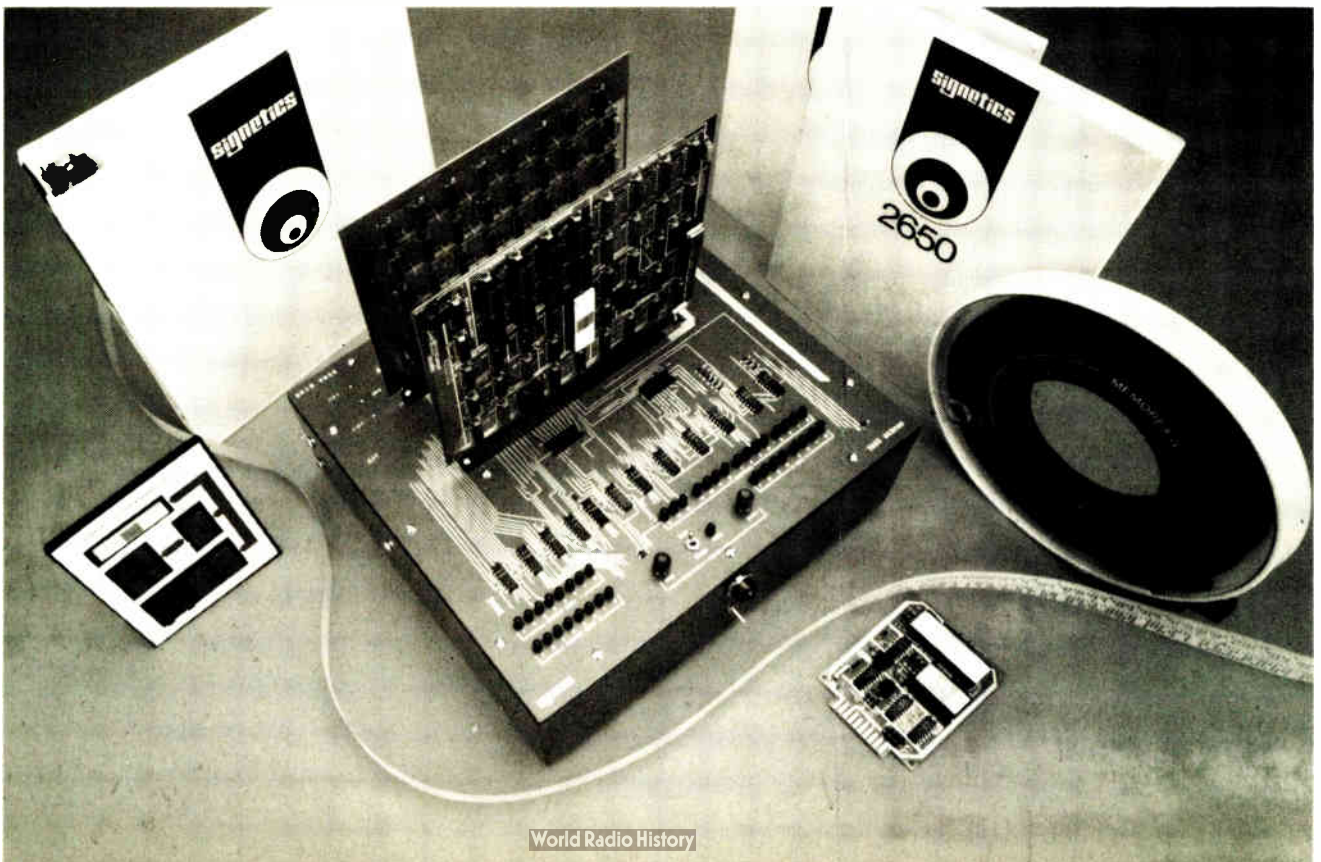
For example, programs in a traffic-light controller are a matter of simple logic replacement, and probably would not exceed 500–1,000 bytes, or about two 4,096-bit chips of random-access-memory or read-only-memory. In small business applications, however, data-handling microprocessors masquerade as mini-

computers. They require more extensive programs, possibly running close to the 64-kilobyte limit of the 16-bit address bus in most 8-bit microprocessors.

To varying degrees, engineers must become programmers when working with processors. For the more complex systems, chances are they will share the work with professional programmers—computer-science specialists drawn into the field by the rapid boom in programming. But even then, they will have to learn the basics to take care of the peripheral-control tasks off-loaded from the central processing unit.

Nearly every microprocessor manufacturer offers a complete package of development software programs: editors, simulators, monitors, assemblers, and, in a growing number of cases, compilers (see "Software tools aid program development," opposite). Generally they are available in three forms: in the manufacturer's development hardware; on magnetic tape for entry into a user-owned larger computer (so-called cross-computer programs), and from time-sharing services. Independent software houses offer programs that are installed

Software packages. Typical of the support available from semiconductor vendors is the Signetics offering—a basic design module to try out programs, manuals to help learn programming, and magnetic tapes with development software that can be run on larger in-house computers.



Software tools aid program development

There are five main categories of software programming tools for microcomputers; editors, translators (assemblers and compilers), loaders, simulators, and debuggers—each of which facilitates a stage of the development of the system operating program. The following capsule descriptions of each category are supplied by Irene M. Watson, a microcomputer consultant in Los Altos Hills, Calif.

Editors: programs that take the source program, written by the programmer in assembly or high-level language and entered through a keyboard or paper tape, and transfer it to a "file" in the computer's auxiliary memory, such as magnetic disk or tape. The editor also acts on special commands from the user to add, delete, or replace portions of the source program in the auxiliary memory. Editors can vary significantly in the ease with which they permit a user to make changes in the program. For example, some editors can operate only on entire lines in a program, whereas others can add, delete, or replace arbitrary character strings in the program. However, the less-sophisticated editors are usually easier to learn to use.

Assemblers and compilers: programs that translate source programs to object programs—the actual patterns of bits interpreted by the computer. They also print a program listing that displays, side-by-side, the source and object versions of the program while giving error messages and other kinds of diagnostic information useful to the programmer.

Loaders: programs that transfer the object program from an external medium, such as paper tape, to the microcomputer random-access memory. Some loaders also convert a relocatable version of the object program to a loadable version. A program might originally be assembled to reside in the microcomputer memory starting at address zero. If the compiler or assembler has allowed the object program to be relocatable, the programmer can specify to the loader the program's new base address and the loader will modify all addresses accordingly in the object program.

Another feature that is sometimes available is linkage

editing, which establishes the linkages between different object programs that make reference to one another. Linkage editing requires both a compiler or assembler and a loader program that can communicate the appropriate information.

Simulators: cross-computer programs that allow the user to test the object program by simulating the action of the microcomputer when the actual circuitry is unavailable. Simulators often provide certain kinds of diagnostic information unavailable with a debugger program (below) running on the actual microcomputer; warning of the overflow of a processor stack or of an attempt by the program to write into a location in the read-only-memory, for example.

They usually allow manipulation and display of the simulated microcomputer memory and central-processing-unit registers; setting of break points, where processing can be stopped at a certain program address or when the program reads or writes into a specified memory location, and tracing, in which each instruction in a certain address range is printed out as it is executed. Often they provide timing information, such as the number of instructions or machine cycles executed from program start to stop.

The power of a simulator varies from manufacturer to manufacturer, but it cannot completely replace program testing on the microcomputer itself, because the specific timing and external environmental conditions of the actual microcomputer hardware can never be completely simulated.

Debuggers: programs that facilitate the testing of the object program on the microcomputer and its input-output devices. They usually accept commands from the user to perform such functions as displaying or printing out the contents of the microcomputer memories, or the contents of the registers of the central processing unit; modifying the RAM; starting execution of the object program from a specific memory location, and setting a break point or stop execution of the program when the instruction at a specific memory location is reached in the program or when a given condition is met.

on time-sharing systems or sold for installation on an in-house computer.

Several semiconductor companies also have established libraries of programs contributed by users ("for those people opposed to reinventing the wheel," according to Motorola Semiconductor's software manager Wes Patterson). However, care is needed when using such programs, says Jerry L. Ogdin, president of Microcomputer Technique, Reston, Va., a consulting firm.

He recommends novice users of such programs assume the software to be a first draft that must be debugged and tested just as if it were generated in-house. Many of the programs, he says, are "redundant and error-laden, and many are naive solutions to well-understood problems." Nevertheless, the programs are available and could be useful with the proper precautions.

There may be a good argument for the available support software serving as the basis of choice between microprocessors, but the general industry practice is a decision based on how well the devices fit the intended

application. Then designers must decide how to program the selected processor so that it fits perfectly.

Their first, tentative efforts probably will involve programming directly in machine language—the actual pattern of bits interpreted by the device to perform its functions. Such programming is done in hexadecimal code, but the inherent tedium in translating instructions into the generally unfamiliar code soon surfaces.

Assembly language offers the engineer the ability to write instructions in mnemonic form, which he or she can associate with the actual function being performed. This is probably the most widely used method.

For such programming, many new hardware aids are coming onto the market—systems that include a keyboard and a cathode-ray-tube display, or a printer, or both, and magnetic tape or disk storage units. These help the programmer edit the programs and even to debug them on the particular microprocessor selected for the system (see the following article on design aids).

Not all assembler programs are the same, even if

designed for the same device. Careful study should be devoted to extra features such as the ability to use macroinstructions (a name associated with a sequence of instructions, with the assembler substituting the sequence of instructions every time the programmer writes a statement with this name), editing features, and the like.

Comparing assemblers

Irene M. Watson, a microcomputer consultant in Los Altos Hills, Calif., recently completed a study comparing the characteristics of various assemblers. She points out the following major features to look for:

- A format that is easy to use, read, and understand is essential. For example, the programmer should be able to set up his own format for the fields in each statement, and the assembler should not reject a statement because a particular field is started in the wrong column.
- The assembler should accept symbols for variable data quantities and addresses, rather than insisting on actual representation. Along with this goes the ability to translate data constants provided in the form most meaningful to the programmer—hexadecimal, ASCII code, or whatever.
- It should be able to handle arithmetic or logic expressions as operands, and then evaluate the expression and use the result as the operand value of the statement.
- Assemblers should be able to provide an alphabetical listing of symbols and their numerical values (usually a hexadecimal number). Similarly, they should be able to produce an alphabetically sorted cross-reference listing for each symbol in the program, along with the statement defining the symbol, and the statement referring to each symbol.
- The assembler should flag any source-program statements that violate assembly-language syntax rules. Error statements should, whenever possible, indicate the specific statement or field containing the error. They should not abort at the first error, but should flag it, place a skeleton instruction in the object code with the incorrect field set to zero, and continue as much of the program translation as possible.
- It should provide a macroinstruction facility in which variable parameters can be included in the macro statement and automatically inserted in the proper places in the instructions it defines. Assemblers can be compared on the basis of the number of macroinstructions that can be defined in a program, the total number of characters that can be included in all macroinstructions in the program, the level to which macro calls can be nested in macro bodies, and the number of parameters permitted for each macroinstruction.

The chief advantage of assembly-language programming is that it allows the designer to make maximum use of the microprocessor's capabilities. However, when programs get large—say beyond 2,000 bytes or between 500 or 1,000 program lines—it becomes difficult for any programmer to maintain the overall flow without errors inevitably creeping in.

Many subtle errors show up only under rare combinations of conditions, and thus nearly every program must be assumed to have undiscovered bugs that will have to be corrected later. Yet other engineers and

maintenance personnel may have difficulty understanding the intentions of the original programmer because of the shorthand nature of assembly language. Therefore it is important to keep good documentation of the program-writing process, showing the program in clear, understandable detail.

To forestall unintelligibility and to speed programming, languages appeared that are closer to standard English, the so-called high-level languages such as Fortran and Basic. Although they are widely known, problem-solving languages for use in computer applications involving computations, they have not been often used in designing microprocessor systems. Instead, manufacturers of microprocessors have emphasized systems-programming languages better suited to equipment design—handling inputs and outputs, managing internal resources, and so on.

Enter PL/M

The first such language developed especially for microprocessors was Intel's PL/M [*Electronics*, June 27, 1974, p. 103]. It is derived from PL/I, a problem-solving language developed by some IBM-computer users in the mid 1960s for business and scientific calculations.

Intel's PL/M compiler itself is a Fortran IV program, and will run on any 32-bit host processor. It also is available on time-sharing networks. Many new PL/M-type compilers are being designed to run on 16-bit minis, more widely available to engineers.

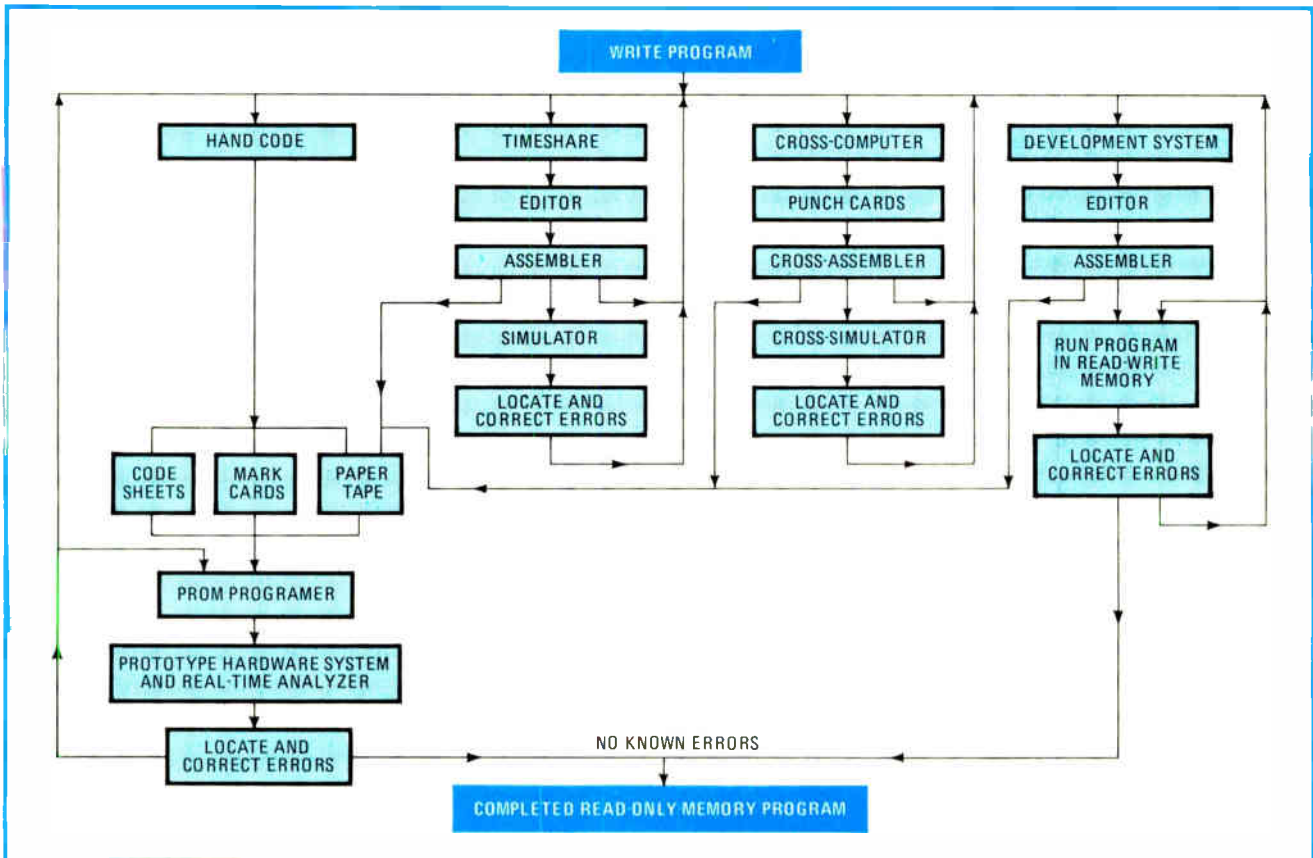
The language was formulated to help designers using Intel's 8008 chip. When the 8080 appeared, it was modified slightly to cover that device as well. Since its introduction, it has been improved many times—"There's been an average of one revision a month," says Intel's Paul Rosenfeld, software product manager for microcomputer systems.

The major problem with any high-level language is that the compiler takes over the job of optimizing the program by cutting out duplications and so on. Programmers, in a sense, get further away from the microprocessor and cannot perform the same tricks of processing that they can with assembly language. Nor can the program be as concise, so memory requirements are larger. It amounts to a tradeoff: less efficiency, but easy use of language and good documentation.

"Each user decides whether it's efficient enough," Rosenfeld says. "Some customers, when they start, generate twice as much code as they would with assembly language, but in six months, they usually are down to 1.5 to 1. Here at Intel, we get in the 10-to-25% range." But programming takes one-fourth to one-fifth the time of assembly-language, according to the firm.

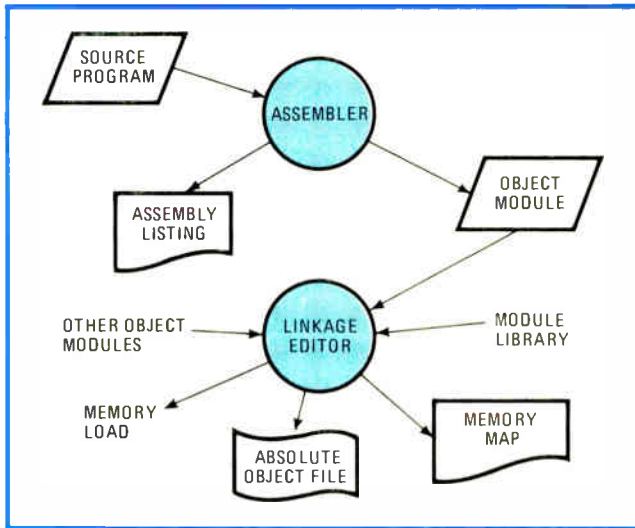
One important factor in the choice between assembly and high-level languages is the number of systems that will be produced. For high volumes, the addition of just one extra memory chip to each system could raise the overall cost to a noncompetitive level. (According to a corollary of Murphy's law, any program written for a high-volume system will turn out to be a few bytes beyond the capacity of a given number of memory chips, so an extra chip is always a possibility.)

With assembly language, it is much easier to redo



<p style="text-align: center;">HAND ASSEMBLY</p> <p>Advantages</p> <ul style="list-style-type: none"> • Relatively fast for small programs • No assembler processing time • No equipment costs • Results entered directly into programmer for read-only memories <p>Disadvantages</p> <ul style="list-style-type: none"> • Slow and tedious for larger programs • Very difficult to expand or contract program once written • Error-prone • Assembler-tested error conditions go unchecked <p>When to use</p> <ul style="list-style-type: none"> • OK for small jobs • As an alternative to assembler processing when the assembler is not readily accessible 	<p style="text-align: center;">MACROINSTRUCTIONS</p> <p>Advantages</p> <ul style="list-style-type: none"> • Repeated small groups of instructions replaced by one macro • Errors in macros need be corrected only once, in the definition • Duplication of effort reduced • In effect, new instructions can be created • Programming is made easier, less error-prone <p>Disadvantages</p> <ul style="list-style-type: none"> • Macros are not subroutines – every time a macro name is used, storage space is required for the defined instructions <p>When to use</p> <ul style="list-style-type: none"> • To replace small groups of instructions not worthy of subroutines • To create a higher instruction set for specific applications or for compatibility with other computers • Caution: whenever possible use sub-routines, not macros
<p style="text-align: center;">ASSEMBLY LANGUAGE PROGRAMING</p> <p>Advantages</p> <ul style="list-style-type: none"> • Symbolic references • Revisions easily incorporated with reassemblies • Symbolic code easier to read • Programming aids included • Values can be parameterized (table sizes, input/output port assignment) • Error checking included <p>Disadvantages</p> <ul style="list-style-type: none"> • Assembler system required (development hardware, terminal) • Some assembly processes are slow • Assembly language rules and formats must be learned <p>When to use</p> <ul style="list-style-type: none"> • Usually recommended for instruction-level coding 	<p style="text-align: center;">HIGH-LEVEL LANGUAGE</p> <p>Advantages</p> <ul style="list-style-type: none"> • Better control of software • Reduced programing cost • Faster programing • Well suited to program solving • Self-documenting • Easier maintenance • Transferability avoids reprogramming <p>Disadvantages</p> <ul style="list-style-type: none"> • Bigger programs – compilation efficiency • Cost of compilation • Programing experience required for good results <p>When to use</p> <ul style="list-style-type: none"> • For larger programs – 1,000 bytes or more • For low-volume products or prototype systems • For production systems when experience warrants

Design routes, pros, cons. There are many approaches to software design, shown by the chart tracing development steps. Similarly, there are advantages and disadvantages for each method of programming. (From course material prepared by Integrated Computer Systems, Inc.)



Linking up. Typical of charts describing software is the operation of the macroinstruction assembler and linkage editor from Motorola Semiconductor. Object code produced by the assembler enters linkage editor with other programs to produce the final code.

portions of the program to reduce the memory usage to fit into the desired number of memory chips. High-level language is best for lower-volume products where fast design turnaround is desirable and where the cost of an extra memory chip can be absorbed in favor of competitive advantages.

Making changes in PL/M

One of the largest users of PL/M outside of Intel is Sycor, Inc., Ann Arbor, Mich., a manufacturer of intelligent terminals. Sycor committed itself to the language about a year and half ago, according to software head Geoffrey Leach. But, he says, "in a sense that commitment was somewhat ill-advised, because the state of the Intel PL/M at that point was somewhat less than solid."

So the firm went its own way and made a number of improvements to the compiler. Now, compared with the early versions of the language, Leach says, "we feel we have achieved a 30% reduction in the amount of code the compiler produces."

Sycor uses its home-brewed version almost exclusively for all programming of 8080-based systems and does little in assembly language. "For the amount of software that we produce, the programmer productivity in assembly language was not sufficiently high to allow us to make our delivery schedules," Leach says.

These are large programs—typically for a fully configured system, the program runs to about 48 or 56 kilobytes of stored code. "I don't think our programs would be any smaller than if we had the same people do them in assembly language," he says. "I have to admit this is one of my favorite soap boxes.

"Programming in higher-level languages is often faulted on the grounds that much better code can be written in assembly language. But if you ask the person making that criticism to sit down and code a 48-kilobyte system in assembly language, you will find him making compromises, missing organizational structures, generally doing things which introduce extra code. That's

why I say that for an average programmer over a year I don't think we have necessarily lost anything in using PL/M."

The next system programming language to appear from a semiconductor manufacturer was the recently announced MPL, also a descendant of PL/I, from Motorola Semiconductor. The MPL compiler produces assembly language (the PL/M produces machine-level object language) and must be run through an assembler to generate the object language.

Motorola says this feature allows the user to study the assembly-language program for possible refinements before generating the final object code. This is "both a blessing and a curse" says Motorola's Wes Patterson, because the need to use an assembler results in a longer run on a computer.

MPL also allows the programmer to drop down from high-level language to assembly language in those areas where he feels it is important to conserve memory space. This may be useful, but the user must know how fully the compiler can take advantage of the microprocessor's ability to streamline instructions and save memory space.

However, the ability to drop into assembly language can be too much of a temptation for some programmers to resist, according to Gary Kildall, the consultant primarily responsible for the original PL/M. He likens it to "having a parachute while flying a plane—you may bail out too soon."

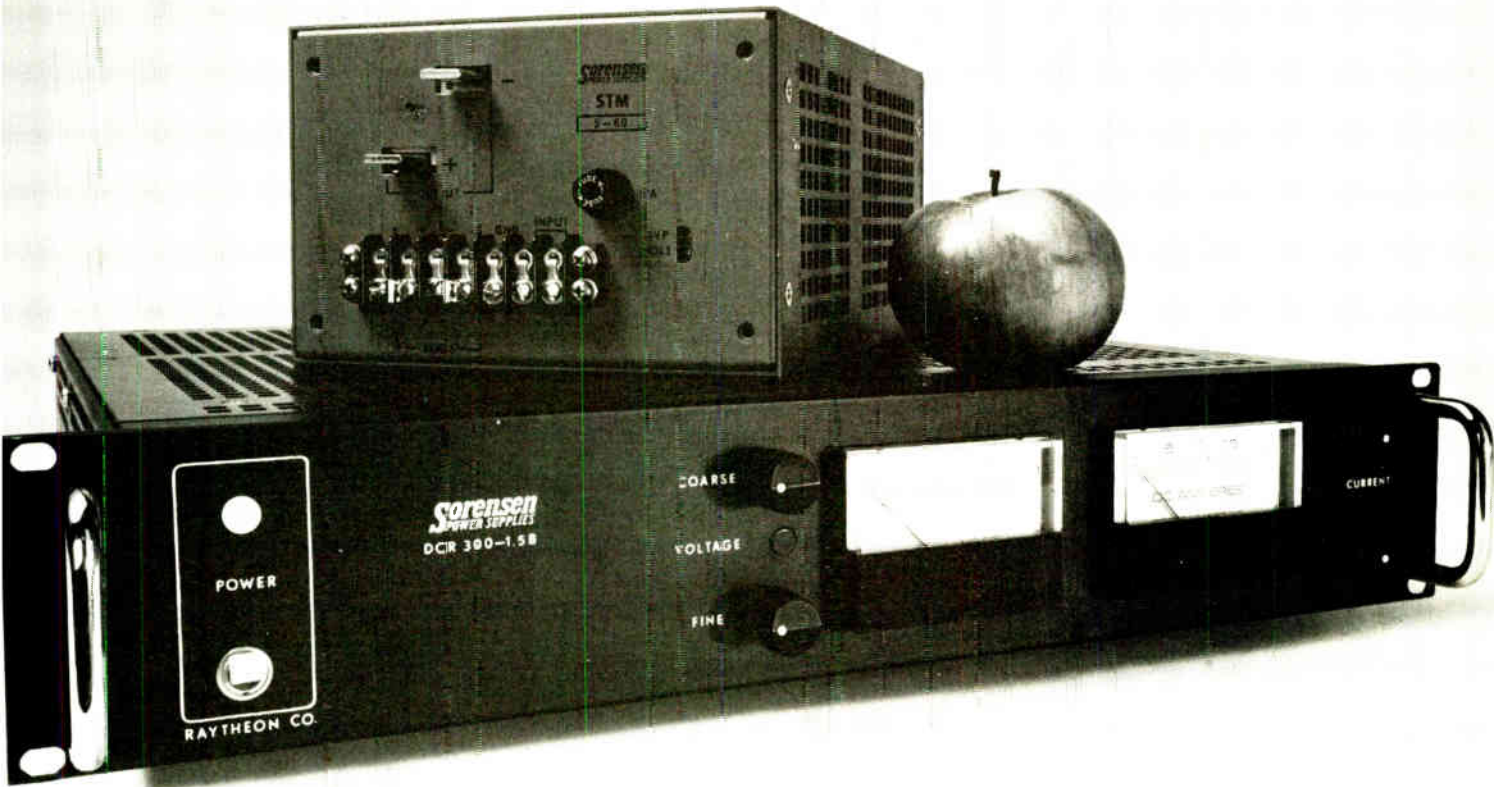
The assembly language pollutes the program, he says, because, when the programmer drops into assembly language, chances are others will have difficulty understanding what he was trying to do. With PL/M, Kildall points out, assembly language could be used to simplify particular parts of the program, but it is included as a subroutine, called by a high-level statement. This increases the overhead by the three bytes of the call, but it vastly increases the understandability, he says.

Other PL/M-type high-level-language compilers available, or just over the horizon are:

- SMPL, intended for use on National Semiconductor's IMP-16 devices, with another version due soon for PACE, another of the firm's microprocessors.
- PL/M 6800, written by Intermetrics, Cambridge, Mass., for the 6800.
- PL/W, written by Wintek Corp., Lafayette, Ind., for the 6800.
- PL μ S, for the Signetics 2650, developed primarily by Kildall.
- PL/Z, soon to come for the Z-80 of Zilog, Los Altos, Calif.

Various versions of Basic have also been written for the 8080 and other devices. Fortran compilers also are on the way from such sources as Zeno Systems, Santa Monica, Calif., and the Boston Systems Office, Boston, Mass. Many engineers point out that there is greater familiarity with these high-level languages because of their prevalence in minicomputers—so why switch to the PL/I derivatives? However, there is a noticeable bandwagon effect shaping up. Just as the 8080's head started led to its wide adoption, PL/M and its cousins threaten to become a *de facto* standard. □

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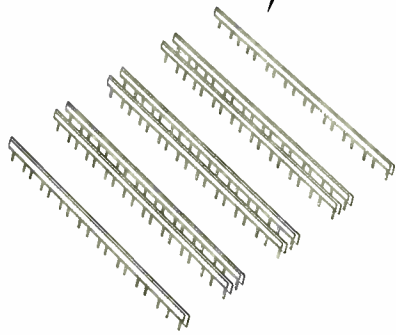
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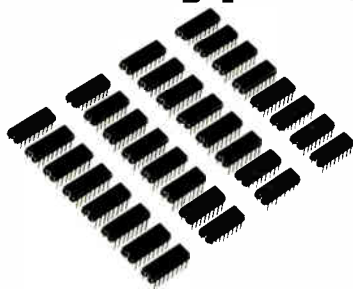
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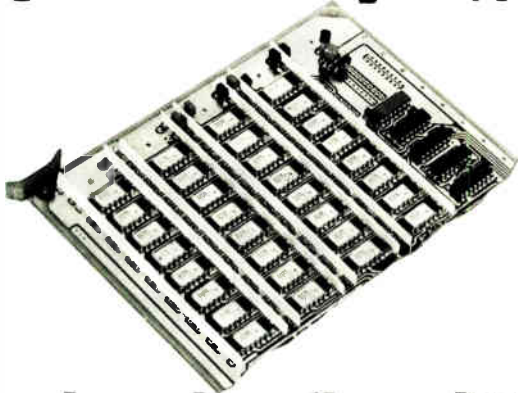
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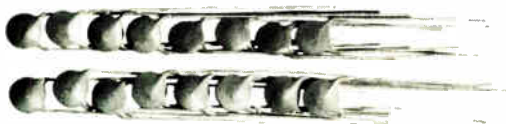


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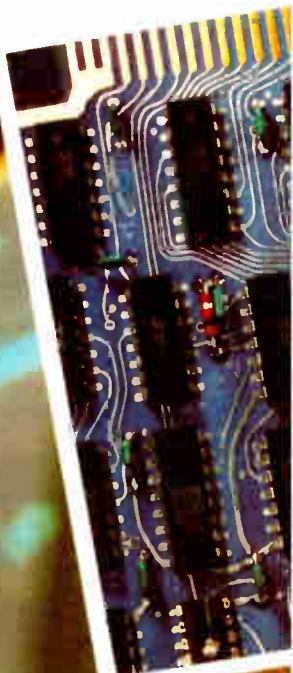
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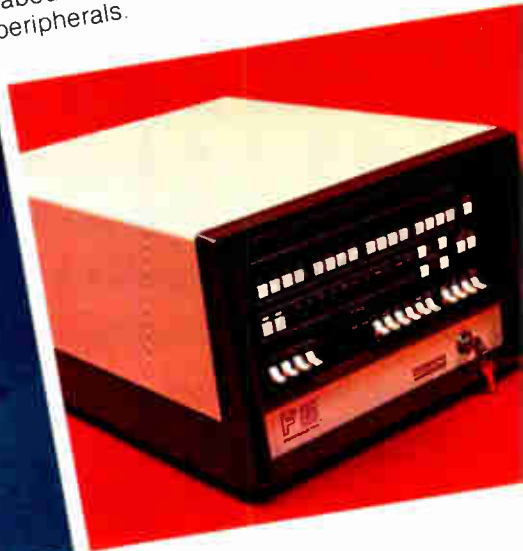
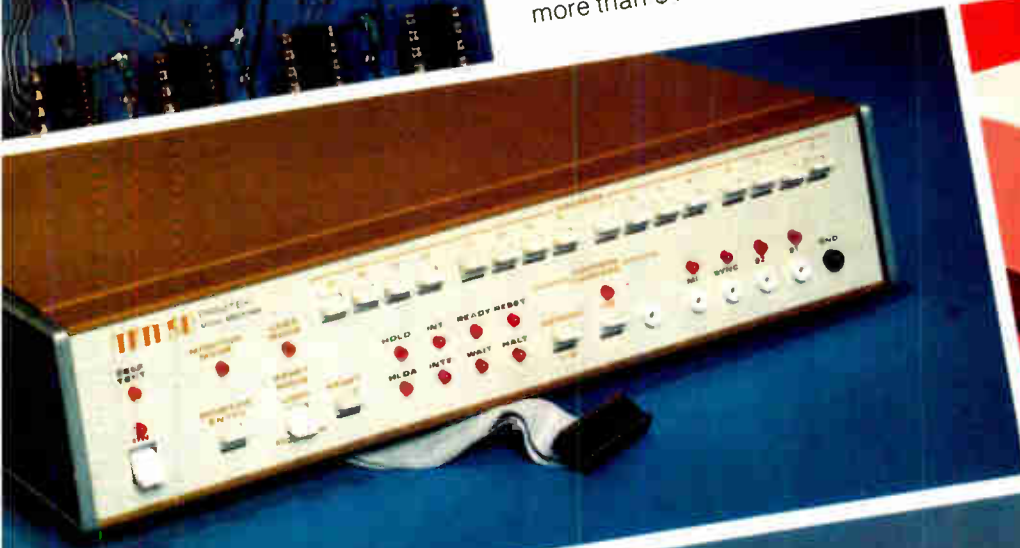
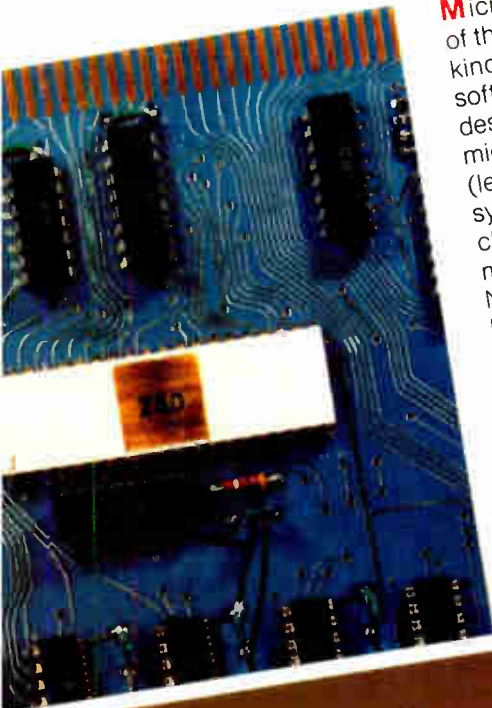
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Design aids



World Pacific History

Microprocessor-based systems are coming to the aid of the microprocessor-system designer. These new kinds of tools help the engineer develop and debug software as well as hardware. He can also simplify his design task by using pre-assembled prototype microcomputer boards, such as Zilog's Z80 board (left). Some of the rapidly emerging development systems available are (below right, and running clockwise) Fairchild's Formulator for the F-8 microprocessor, Signetics' TWIN for the 2650, National Semiconductor's system for the IMP-16, Rockwell's Assembler for the PPS-8, and (center) Ramtek Corp.'s MM80 for use on the Intel 8080 device. With a printer and keyboard connected to such systems, the engineer can enter programs in assembly language, edit them, perform the assembly, and then run the programs and debug them. Cathode-ray-tube displays are often available for easier interactive editing and debugging, as well as floppy-disk drives for rapid entry of programs. Prices range from about \$4,000 to more than \$10,000 for systems with peripherals.



MICROPROCESSORS

Designers need and are getting plenty of help

Chip makers and users alike are marketing the special tools and instruments that they've found useful in developing systems around specific chip families—and more universally applicable aids are starting to emerge, too.

New design tools and development systems are appearing as microprocessors force engineers to change their design methods from a hardware to a software base. Now, rather than perching on a workbench stool and facing an array of signal generators, volt-ohmmeters, and an oscilloscope, more engineers are finding themselves comfortably seated in armchairs in front of a keyboard, programing a microprocessor.

The development systems, in fact, bear about the same relationship to the software development process as the oscilloscope does to hardware development. Up to now, the major source of such development systems has been the semiconductor vendors themselves, who, as originators of the devices, have been the most familiar with them.

Every major semiconductor manufacturer offering a microprocessor also offers development system hard-

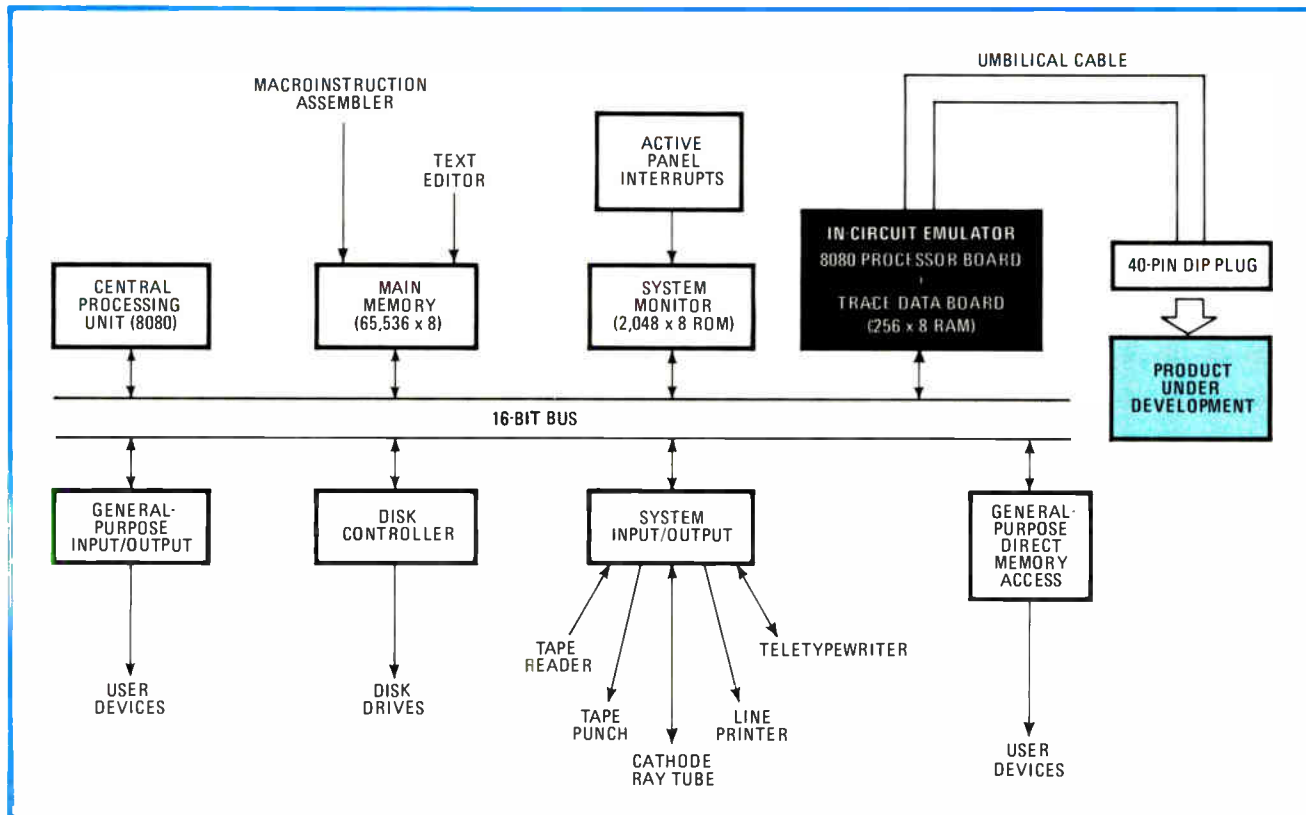
ware and software to support designers. (Some are simply called development systems, while others have names with a little more flair: Intel's Intellec, Motorola's Exorciser, Fairchild's Formulator, Rockwell's Assembler, Signetics' TWIN, and Scientific Micro Systems' MCSIM.) Even some of the companies second-sourcing microprocessor chips have come out with their own development systems that in some cases outdo those of the original developers.

Most of the systems from the semiconductor manufacturers are, despite individual claims of superiority for certain features, quite similar. All generally have resident software—monitor, assembler, editor, and debugger—and the latest models are appearing with an in-circuit emulation capability, so that users can debug programs using their actual prototype hardware.

Any differences lie in the quality of the resident soft-

Systematic analysis. One of the latest enhancements to Motorola Semiconductor's Exorciser is the system analyzer, shown plugged into the microprocessor board. With the switches the programmer can set a hardware breakpoint, and with the displays he can examine bus status.





ICE unfreezes developments. In Intel's microcomputer development system, the in-circuit emulation (ICE) module allows coordinated development of software and hardware. Designer can use internal MDS memory and I/O until they are available in the prototype.

ware—the features of each program and the amount of memory the software occupies within the system—and in the kinds of peripherals the systems can handle. The latest systems are being offered with floppy disks. These can store large blocks of software and also allow faster access, than, say, a magnetic-tape cassette.

Resident software

The software resident in the development systems—monitor, assembler, and editor—may not be an absolute necessity to the design of microprocessor-based systems, but the debugging features would be difficult to do without. A designer, for example, could use a time-sharing service or in-house computer for assembly of his programs and simulation of his system, but debugging his prototype requires many new techniques.

For debugging, an engineer needs the ability to set breakpoints, easily alter memory or register contents, execute the program in single-step fashion, and store the bus status for several cycles before hitting a breakpoint. It's also helpful to have a disassembler function, which reconverts his stored program from machine language to assembly language. And, since the debugger is itself a program, it would be convenient to be able to enter debugging commands in assembly language, rather than in machine language.

Until recently, the choice of microprocessor determined the development system, but that situation is now changing. Independent companies are working on "universal" systems, capable of handling any of several popular microprocessors. Moreover, there is a rapidly

growing body of knowledge among users, and many smaller companies, encouraged by their success in home-brewing their own development systems, are attempting to sell them to others. Most of these systems start out being limited to only one microprocessor family, but later versions are appearing that can handle two or more different devices. Other companies are offering add-on enhancements to existing systems supplied by the semiconductor companies.

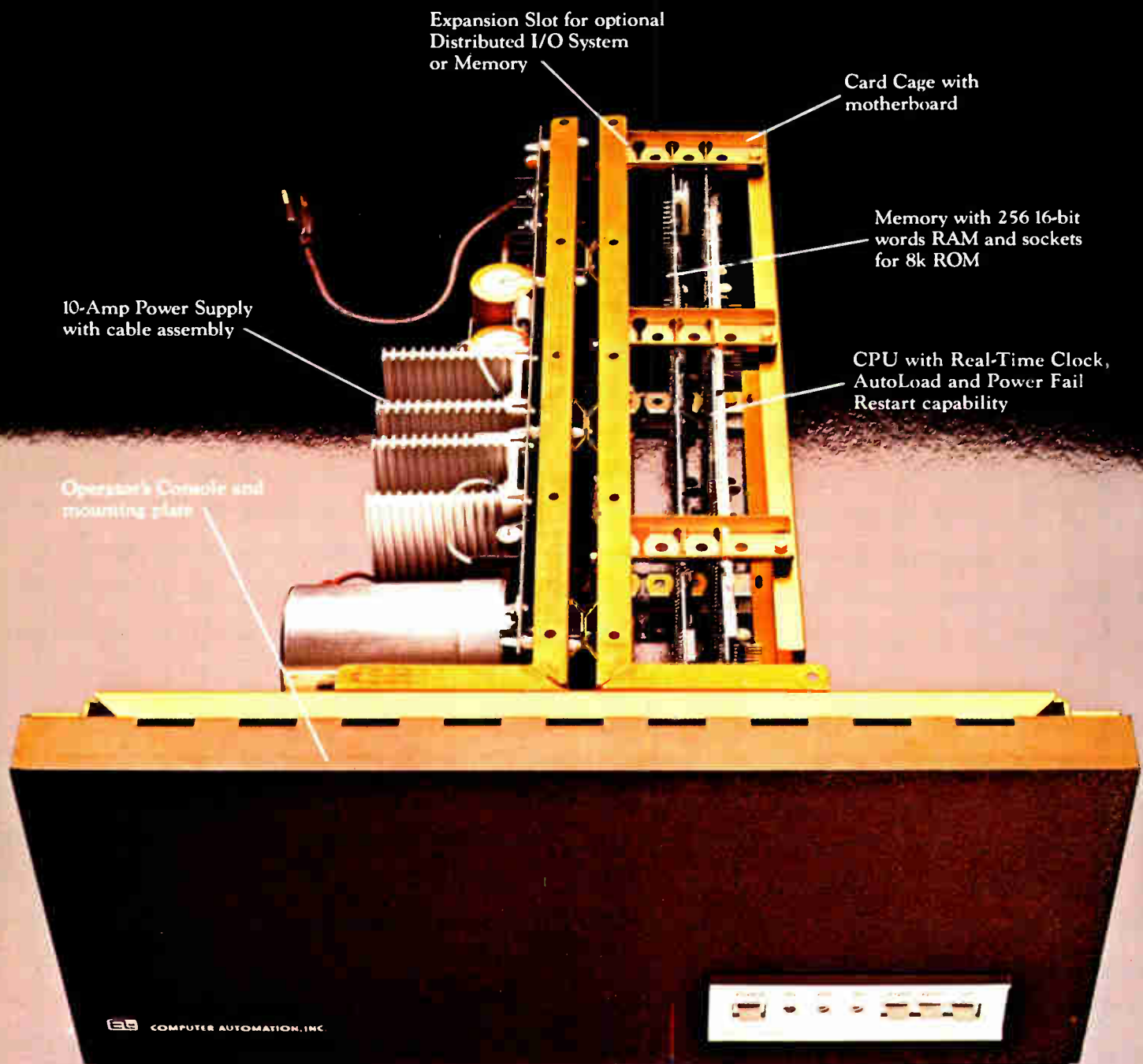
The idea of universality is an important one. New microprocessors are continually appearing, and most users would prefer systems that can be easily modified to work with the new devices. A fully equipped system—including display, printer, and floppy disks—can easily reach the \$10,000-plus range, and few design budgets could stand being swelled by such costs every time a new processor is used.

Some companies are building add-on units that augment the capabilities of the semiconductor manufacturers' basic development systems. There is also a series of simpler programming aids coming on the market, with resident assemblers and editors. Each of these systems is based on a particular microprocessor and can execute the programs on that device, but, for other devices, can only be used to assemble and edit programs.

In-circuit emulation

It was a semiconductor vendor—Intel Corp.—which touched off the new wave of development aids. That happened last year, when it introduced the in-circuit emulation function for its Intellec microcomputer devel-

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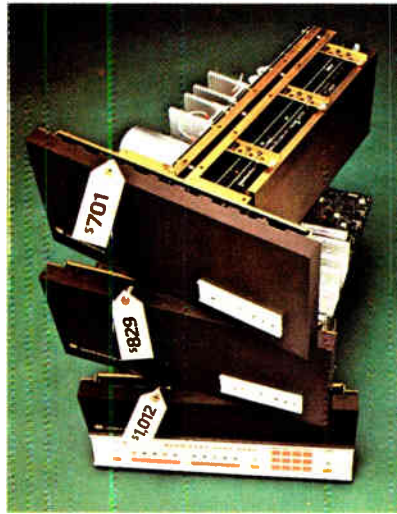
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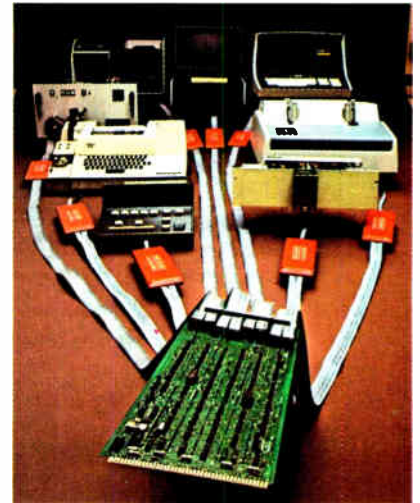
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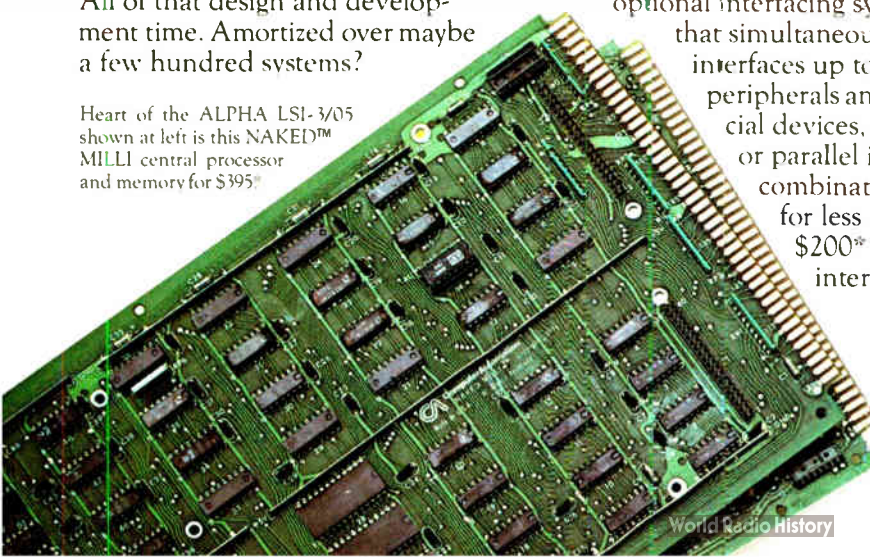
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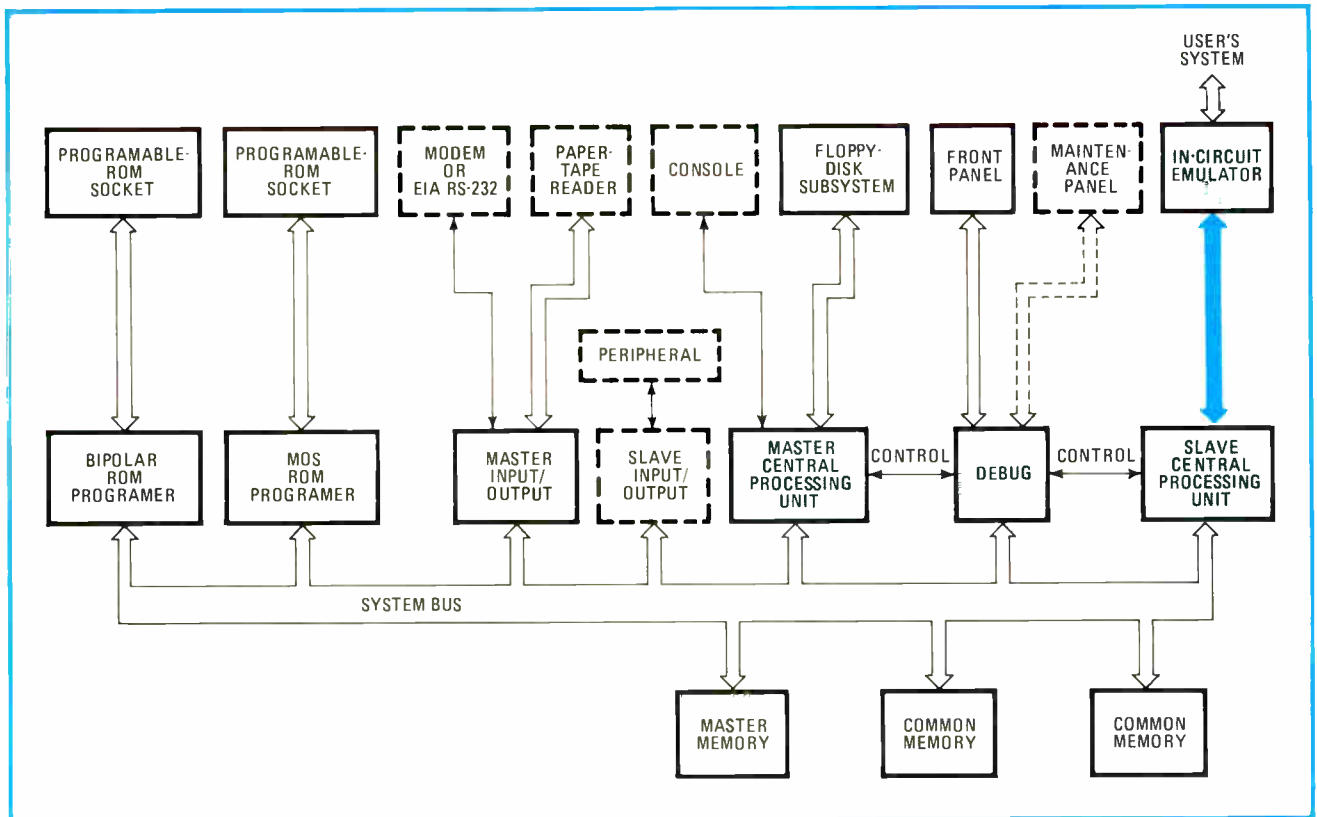
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Master and slave. In Signetics' TWIN—test ware instrument—one 2650 processor executes software unrelated to actual device, and another, the slave, executes software for prototype. Future versions could handle other processors by changing just the slave.

opment system for the 8080 microprocessor [*Electronics*, May 29, 1975, p. 91].

The aim of in-circuit emulation is to allow simultaneous development efforts by both the software and hardware design teams. Without in-circuit emulation, software could not be completely debugged until the prototype was completed—at best it could be run on a simulator, which usually copies a system only imperfectly. With in-circuit emulation, the hardware designer can build and check his prototype in stages and run software on whichever parts have been assembled, using the development system to substitute the facilities not yet included in the prototype. For example, the basic Intellec MDS at first provides memory and I/O lines. As these are built into the prototype, the designer can switch over and use the actual hardware.

The MDS with the emulation module is a two-processor system. One processor, a general-purpose unit based on the 8080, supervises the system running the assembler and editor programs and controlling the peripherals. The other processor is in the in-circuit emulation (ICE) module and emulates the action of the processor in the prototype. It gains access to the prototype hardware through a 40-pin DIP plug, inserted in the same socket that the prototype's processor will eventually use. Thus, as microprocessors appear, only the software and the ICE module need be changed to apply the system's full capabilities to that new device. Intel has announced two emulation modules so far—for the 8080 and for the 3000 series of bipolar bit-slice devices.

One system that its developers claim is universal is

Signetics' new TWIN, for test ware instrument [*Electronics*, March 18, p. 44]. The system, designed for Signetics by Millennium Information Systems Inc., Santa Clara, Calif., uses two processors—a master and a slave. The master processor is a Signetics 2650, but the slave can be any device, according to Millennium president Gerald Casilli. The master runs those programs, such as the disk operating system, that are independent of the type of processor in the prototype, while the slave runs the programs unique to the prototype's processor, such as the assembler, editor, and debugger. In its present version, the slave processor is a 2650, but in future versions, simply changing the slave board and entering new assemblers and debugging software could convert the system to any processor.

Similar simulation

Motorola Semiconductor has been supplying its Exorciser for use with its 6800 since mid-1975, but until recently it did not have an equivalent of the ICE function. Now, the company is making a double-barreled enhancement to the Exorciser—a system analyzer, plus a user system evaluator (USE) that is its answer to ICE. The system analyzer (see photo) is an extra board that plugs onto the top of the Exorciser's CPU board. It enables the programmer to set a breakpoint, display the status of the bus in hexadecimal code, and store the bus status for 64 bus cycles before and after a particular event. This data reveals how the program caused the processor to reach a particular step, when an error occurred, and where it went from there.

The USE board, which must be used with the system analyzer card, has a cable ending in a 40-pin DIP plug that plugs into the microprocessor socket, thus extending the Exorciser bus to the prototype. All internal debugging features then become available at the prototype, but the system can run off the prototype clock.

USE differs from ICE in that only one processor is used. As a single-processor system, the Exorciser offers much better emulation in real time, says Frank Tarico, Motorola product manager. Tarico concedes that dual-processor systems offer greater flexibility in adapting to new devices. However, when part of the system is controlled by the main processor and part by the emulation processor, waiting periods are inevitable while the control passes from one processor to another, thus upsetting the real-time emulation. To adapt the Exorciser to a new processor would require replacement of the master processor board and perhaps some of the other boards, according to Tarico, depending on the degree of difference between the new processor and the 6800.

One point that should be emphasized is that these systems are, in themselves, computers. Although their primary function is to help a programmer develop software for his microprocessor system, the development systems can run programs for other jobs. For example, Motorola Semiconductor plans to include an interpreter for a version of Basic language on its Exorciser. This would allow an engineer to use the Exorciser to solve general computation problems as well as to design new systems. And Texas Instruments' system for its 9900 is based on its 990 series minicomputer, which uses the 9900 as its CPU. This development TI system, being in fact a 16-bit minicomputer, can run high-level languages such as Fortran, Basic, and Cobol.

American Micro Systems Inc., Santa Clara, Calif., also is producing the 6800, using the same mask sets as

Motorola. However, AMI has designed its own set of development aids, both hardware and software. The system uses a keyboard and a CRT capable of displaying 25 80-character lines, and it runs with dual floppy disks.

Since only the processor modules need be changed to adapt some systems to a new microprocessor, other companies may choose to take advantage of a designer's existing investment and offer only a special module to handle a new device or add a feature to the system. For example, Digital Electronics Corp., Berkeley, Calif., has designed an enhancement, similar to USE, for the Motorola Exorciser. Called DICE/68, it extends the debug power of Motorola software to the user's 6800 system.

Enhanced exorcism

The DICE/68 plugs into the user's system through a 40-conductor flat cable and 40-pin plug, and it uses the Exorciser software to give the designer access to the prototype hardware. It extends the Exorciser 16-bit address bus, 8-bit data bus, and control lines out to the user. All facilities of the Exorciser, such as trace, breakpoint, and the ability to display and modify memory contents, may then be used for debugging.

The DICE front panel also helps in debugging system hardware. For example, panel-mounted light-emitting diodes indicate the status of prototype data and address buses, as well as control lines. Control switches on the console allow the DICE/68 user to halt the processor, single-step the processor, and initiate a nonmaskable interrupt, interrupt request, or reset.

Some development systems reserve certain portions of memory for internal use, and the designer must remember to avoid allocating these blocks of addresses to his prototype system. Others, such as Zilog's Z-80 development system, make all system memory available to the user's hardware when in the user mode. Zilog Inc.,

Let's pretend. Scientific Micro Systems' development tool, MCSIM, simulates the company's MicroController module, plugging directly into the prototype system. Although the panel displays just one line at a time, the lines can be 'rolled' to show complete program.





Interaction. Users of MOS Technology's microcomputer development terminal, MDT 650, can assemble programs and debug software with a keyboard or remote teletypewriter. Unit has 32-character display and can trace previous 128 machine cycles.

Los Altos, Calif., recently announced an enhanced version of the 8080 and is now readying a dual floppy-disk development system based on a single Z-80 processor. The processor performs both the internal system monitoring tasks when in the monitor mode and controls the user's hardware when in the user mode. In the user's mode, all system memory and peripheral devices are dedicated to the prototype hardware.

There are two different approaches adopted by development systems. Some have a minicomputer, or instrument, type of front panel, with many switches and lights, while others are almost completely bare, except for start and stop buttons and a couple of lights to show when the system is in operation. In either case, most of the commands and diagnostic information are obtained through a printer or a CRT screen anyway, but the instrument-type front panel can be helpful in debugging or repairing a system in the field.

With and without panels

Rockwell's PPS-8MP Assembler, for example, executes many debugging commands from a front-panel hexadecimal keyboard and instruction keys. Its LED display also shows hex addresses, instructions, and data.

Another example is Ramtek's MM80. Intended for systems based on the 8080, it is viewed by its designers as more of a hardware engineering tool, useful both for development and final test, than a software development system. Larry Krummel, product manager at Ramtek Corp., Santa Clara, Calif., says, "Everybody worries about software so much that they forget about the engineering aspects." The system does have a resident assembler, editor and debugger, all stored internally in read-only memory, and it can work with a keyboard terminal, such as TI's Silent 700 terminal. (Ramtek, in fact, uses Texas Instruments Supply Co. as its main distributor for the MM80).

National Semiconductor Corp. also has gone the switch-and-light-panel route for its development systems for the IMP-16 and PACE microprocessors. The

systems differ primarily in the basic central-processing-unit boards, and the earlier IMP-16 system can be converted to handle PACE simply by adding a new CPU board and making other minor conversions. The National development systems have the standard complement of assembler, editor and debugger software, plus a resident compiler for National's new SMPL high-level language. The compiler requires a memory of 12-kilobytes within the system.

Another system with a minicomputer front panel is Fairchild Semiconductor's Formulator, for the F-8. The front panel, under firmware control, provides an array of switches and LED indicators for direct access to F-8 registers and memory locations. From the operator's panel, the user can examine and alter the microprocessor storage, set hardware breakpoints, single-step the central processor, and even self-test the Formulator.

Instead of using an ICE module approach, the Formulator itself serves as the system breadboard, by providing extra card slots for breadboarding the user's system. In some cases a breadboard prototype may even be unnecessary, since the user can connect external I/O to the system. This would be useful in preliminary feasibility studies to determine if the processor can do a particular job. For example, the designer might connect directly to the control lines of the external system and use the Formulator as the F-8 controller.

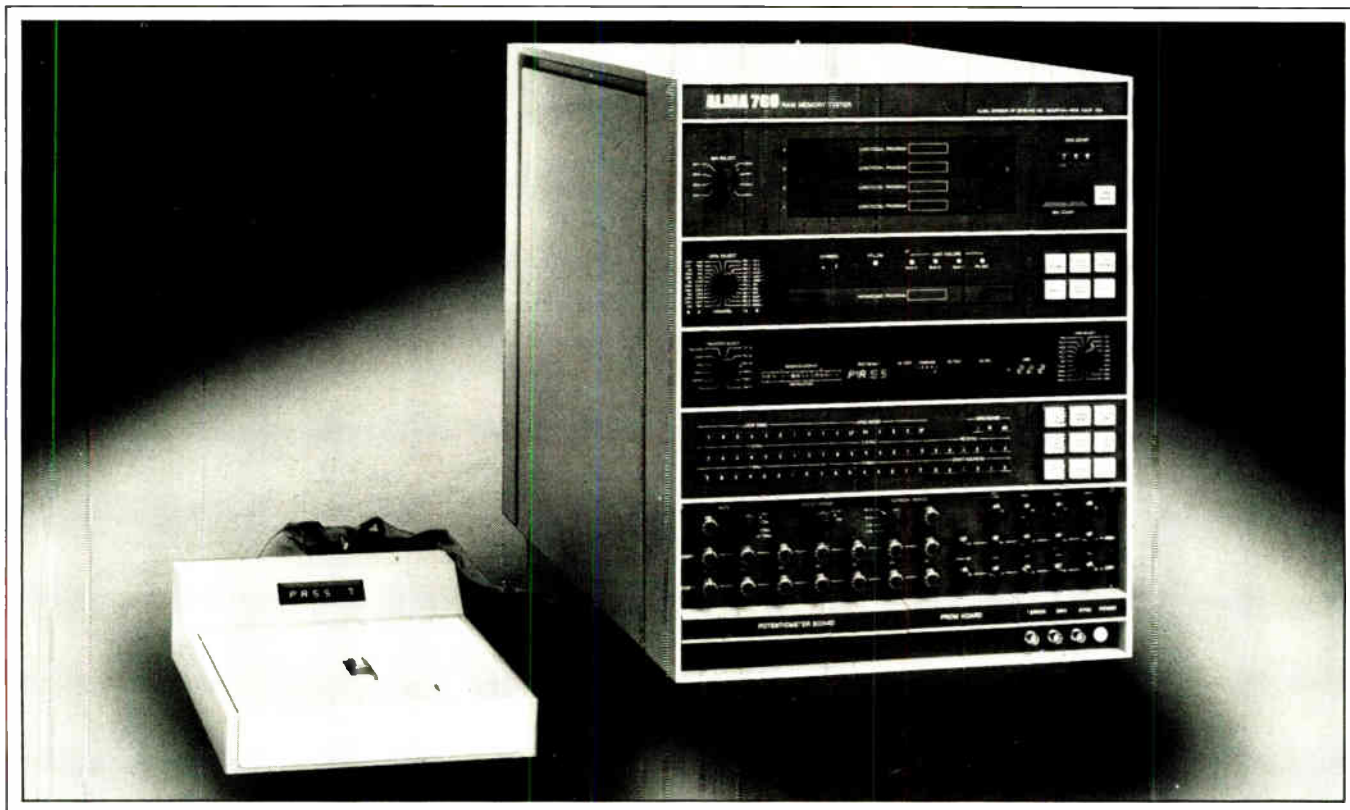
Two recent additions

Another new programming aid is the μ Scope, from Tranti Systems Inc., North Billerica, Mass. [*Electronics*, April 1, p. 120]. This system is an integral desk-top unit containing an alphabetic keyboard, a 10-key numeric pad and control keys, a CRT, a small alphabetic printer, a magnetic-tape cartridge for program storage, and an expandable memory. Its software (monitor, editor, and assembler) is resident in ROM. The software essentially assembles the program as it is entered, rather than in a later off-line pass-through. Since the program is assembled upon entry, the memory need not store line numbers, and only one byte of memory is needed for each byte of user program (although space is used to store labels, at 8 bytes per label).

The system itself is based on an 8080A. But the company says the software is universal and can be used for any 8-bit microprocessor.

The Microkit-8/16, from Microkit Inc., Santa Monica, Calif., also helps development of systems based on the 6800 and 8080 microprocessors. It includes in-circuit emulation capability [*Electronics*, March 18, p. 152]. The standard system has a CRT, a keyboard and two 2,000-bit-per-second cassette tape units. The editor can run at the 20,000-character-per-second I/O rate to the CRT display. (In fact, Microkit says it is selling the system as a word processor.) The in-circuit analyzer allows the system to monitor user-developed microcomputer hardware by plugging directly into the user's microprocessor socket. In fact, programs developed using the software development package can be loaded into the user equipment. The user can set software breakpoints and also interrogate the microcomputer for register, flag, and memory contents. □

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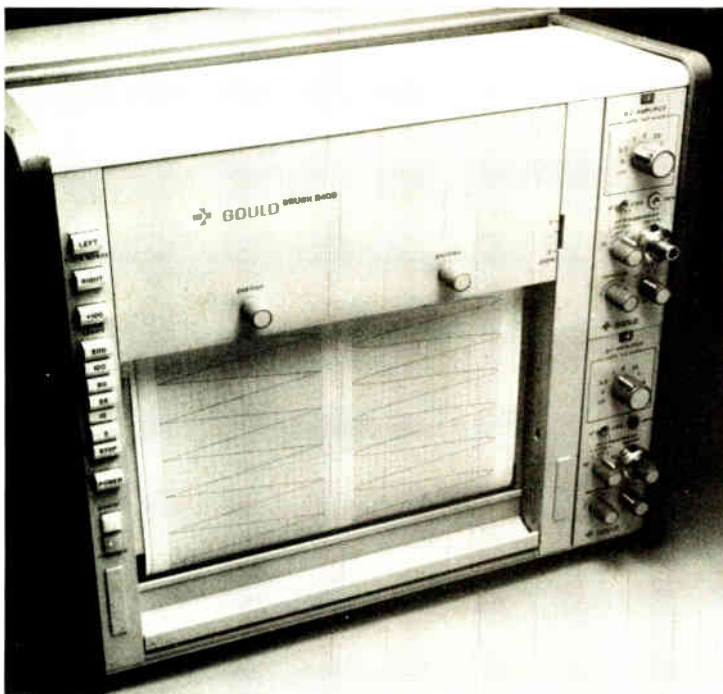
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Test methods change to meet complex demands

The variety of devices, unfamiliar failure modes, lack of access to internal logic, and higher test speed add to difficulty of checking devices. Moreover, extra testing at the board level is needed.

by Robert E. Anderson, *Omniconip Inc., Phoenix, Ariz*

Microprocessors are powerful little devices, but their complexity means testing is neither straightforward nor simple. Moreover, testing at the device level is not enough. Something can be wrong with the fabrication of the boards into which the processors are inserted, so a second level of testing also is necessary.

Essentially, there are two types of device testing for microprocessors: techniques similar to those used with the logic-circuit boards that the processors are replacing and system techniques similar to those used with computers. Once a microprocessor passes device testing and is on a board with other devices, there are several testing techniques to choose from. At both device and board levels, there are varying degrees of applicability of techniques, and this brief review will place them in perspective.

Microprocessor testing often is compared with logic-board testing and found to be more difficult. There are several reasons given.

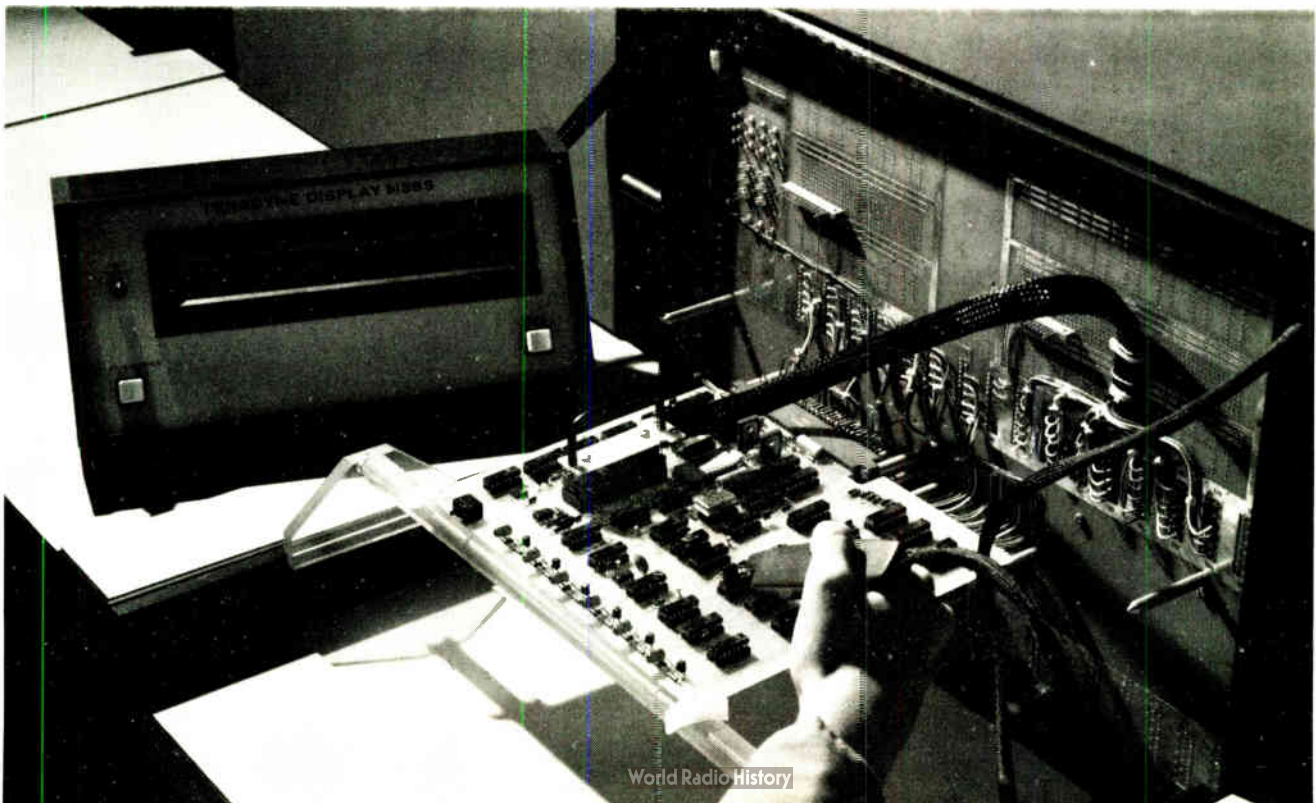
The first is the wide range of the characteristics of

currently available processors. The various architectures, chip layouts, fabrication processes, instruction languages, input/output pin assignments, and bus sizes preclude development of a standard test. However, this difficulty probably is overemphasized. Logic boards have equivalent variety, and good techniques have been developed to test them.

A more significant reason is that microprocessors have different failure modes from logic boards, and these are not well known to the users. By contrast, most failures of logic boards can be modeled by assuming that each integrated circuit or gate node can be "stuck-at-one" or "stuck-at-zero."

However, microprocessor vendors generally will not provide a user with the amount of detailed information required to create such a model, and processor failure modes are more complex than "stuck-at-one" and "stuck-at-zero." Also, detection of some microprocessor failures requires tests at operating speeds, and a wide variety of possible instruction sequences is needed be-

Microcomputer test. Microcomputer boards can be functionally tested without the microprocessor, ensuring that an expensive device will not be damaged by a faulty board. This Teradyne L125 circuit diagnostic system tests the board through the processor socket.



cause the uncertainty about failure modes means that worst-case test patterns have not been developed.

Another significant difference between microprocessor and logic-board testing is the relative amount of access from the tester to the internal logic circuit. Printed-circuit boards with a logic complexity equivalent to a microprocessor chip have three to four times as many I/O pins. The smaller number of pins on the microprocessor means that many more functions are controlled internally. The tester has less control and less access to intermediate results.

On the other hand, this increased logic capability makes the microprocessor a more intelligent device under test, which can be an aid. At the extreme, self-diagnostic programs can test microprocessors without an external tester.

A final factor making microprocessor testing more difficult is that more sophisticated test-system hardware is required because of the higher test speed required for microprocessors. Most logic boards can be tested at rates much slower than their operating rates. If the purpose of the test is to detect catastrophic failures, most of them are just as detectable at 1 kilohertz as they are at 2 megahertz.

Microprocessor testing must include a test of timing characteristics, because they are important in the device's operation and because the processor operates much closer to its maximum possible speed than do most logic boards. In addition, many of the processors are dynamic devices that have relatively high minimum operating frequencies.

Another aspect of the problem for the test hardware is matching the bus organization of most microprocessors. Information must be transferred between the processor and the tester across a 4-, 8-, or 16-pin bus within one clock cycle. What's more, because many buses are bidirectional, the tester must be able to switch between driving and sensing within a single clock cycle.

The special timing requirements, plus the need to synchronize the timing between the tester and the processor under test, necessitate a different test-system architecture from the kind used for logic-board testing. Larger processor test systems also include a parametric measurement capability that is rarely used for logic-board testing.

In one sense microprocessor testing can be easier than logic-board testing: as well as its already mentioned capability of assisting in the test process, its faults can't be corrected by replacing the errant components. It's all or nothing with a microprocessor chip, so there generally is no need to isolate the cause of a fault.

Applying board-testing techniques

Logic-board testing requires the production of input stimuli to the board under test and a comparison of the actual output responses to the expected correct responses. Microprocessor testing also can be implemented along these lines by applying test patterns and monitoring the output responses at each clock cycle (Table 1).

There are three fundamental techniques for producing input patterns suitable for processor testing:

pseudorandom pattern generation, manual programming, and algorithmic pattern generation.

Pseudorandom patterns are used as the input stimuli in at least one in-house microprocessor tester, and they probably will be used in others. This technique, widely used for logic-board testing, is based upon the principle that a large number of repeatable random patterns will exercise the microprocessor sufficiently and will propagate faults to output pins where they can be detected. As with logic-board testing, pseudorandom test patterns usually must be preceded by some specific test patterns to initialize and synchronize the microprocessor and to test highly sequential internal elements.

Advantages of this technique are the low cost of the tester and the small programming effort required to generate a large number of test patterns. The disadvantage is the danger of applying "illegal" input patterns that create indeterminate states or block subsequent input patterns. Also it may take considerable convincing before the microprocessor vendor will accept the failure of chips tested with pseudorandom patterns.

A second technique for producing input patterns is manual analysis, which is used with most of the available testers. Software digital simulators are a popular aid in this type of analysis because they provide the nodal logic-state information at every test, and because they can evaluate the comprehensiveness of the test program, letting the programmer concentrate on the undetected faults.

While digital simulators can be used by vendors who know the internal structure of the microprocessor, users do not have this information and must analyze the processor functions in order to generate input test patterns. This is generally implemented by writing assembly-language instructions and using a translator software package to convert the instructions to the input test patterns to be applied.

The advantage of this technique is that specific sequences of test patterns can be generated and easily modified, based upon failure experience during testing and in the field. A disadvantage, however, is the need for thorough knowledge of the microprocessor functions and assembly language to generate an adequate test program.

Algorithmic pattern generation, the third input technique, is available in testers from Macrodata Corp., Woodland Hills, Calif. and Fairchild Systems Technology, San Jose, Calif. It uses real-time generation of input patterns based upon a user's specified sequence of assembly-language instructions. The sequence is determined by a control program written by the test engineer in the test-system language.

This technique reduces the amount of test-system storage required, since repetitive instructions can be executed as loops or subroutines within the control program, while the tester hardware generates the actual patterns corresponding to each instruction.

It provides flexibility in generating various sequences of instructions and requires less program writing than an equivalent manual test program. Being more deterministic than tests with pseudorandom patterns, it facilitates testing the microprocessor's sensitivity to spe-

TABLE 1: LOGIC BOARD TECHNIQUES APPLIED TO MICROPROCESSORS

Techniques for producing expected output responses							
Techniques for producing input patterns	Real-time comparison testing		Stored responses recorded from known-good microprocessor		Stored logic-state responses generated		
	Known-good microprocessor	Emulated microprocessor	Signatures	Logic states	Manually	By simulator	
	Pseudorandom patterns	✓	*	*	○	○	○
	Manual programming	✓	*	*	✓	✓	✓
Algorithmic pattern generation	*	✓	*	✓	○	○	

Legend: ✓ = in use * = potential use ○ = impractical

ific instruction sequences. Disadvantages are the high cost of the present test systems and, as in the case of manual programming, the knowledge required of the microprocessor functions and its assembly language.

Producing expected output responses

There are three techniques for producing the expected output responses when testing microprocessors, just as there are with logic boards: real-time comparison testing, which includes comparison with a known-good processor and with an emulated one; stored responses from a known-good processor, which includes stored signatures and stored logic states, and manually generated logic-state responses, either with or without a simulator. In general, most of these output-generation techniques can be used with the three input techniques (Table 1).

One form of real-time comparison testing consists of applying input patterns to a known-good microprocessor as well as to the microprocessor under test. The output responses of the two devices are compared at each clock cycle and any discrepancy indicates a fault.

This technique is relatively easy to implement, but it requires evaluating and selecting the reference microprocessor and ensuring that it remains completely functional. It is used with the pseudorandom input technique and with the manual input technique as in the MPU-1 tester from Micro Control Co., Minneapolis, Minn. It could be used with algorithmic pattern generation, also.

Emulation is a real-time comparison test, in which the outputs of the microprocessor are compared with outputs of hardware circuits in the tester performing the same functions.

It is used only with algorithmic pattern generation, although it could be used with the other input techniques. Since the emulation must be at least as fast as the microprocessor under test, it was more useful with early processors than with the latest, higher-speed units.

The second output technique is to record the responses of a known-good microprocessor during program preparation. These responses are stored and used as the references to which the output response of the microprocessor under test are compared. They can be digital signatures, such as transition counts, representing the logic-state history at each output pin during the complete execution of the test program, or they can be the actual logic state at every output pin for every test.

No commercial tester uses the stored-signature technique, but it appears to have good potential. It can be used with all of the input techniques and provides a good compromise between the moderate data-storage requirements of the real-time comparison-testing technique and the repeatable results and independence from known-good microprocessors of the stored-logic-state techniques. A potential disadvantage is that the complete test program must be executed to obtain a pass/fail indication; thus the specific faulty instruction or test pattern would not be known.

Using the expected logic-state responses is the approach of the largest microprocessor test systems available, such as those manufactured by Fairchild, Macrodata, and Tektronix Inc. of Beaverton, Ore. These computer-based systems also are used to test ROMs, RAMs, etc. Logic-state responses also are used with several add-on buffer memories offered as microprocessor testing options for conventional board testing systems such as the 500-series board testers from Mirco Systems Inc., Phoenix, Ariz. The logic-state responses can be re-

TABLE 2: SYSTEM TESTING TECHNIQUES APPLIED TO MICROPROCESSORS

Microprocessor under test executes self-diagnostic program	Manually generated results of each routine	Real-time comparison testing with known-good microprocessor	Stored signatures recorded from known-good microprocessor
	In use	In use	Potential use

corded from a known-good microprocessor, or they can be generated by manual analysis or by software simulation.

All three of the stored-logic-state techniques are used primarily with test patterns created by translating manually programmed input patterns. They cannot be used with pseudorandom patterns because the large number of tests would require excessive storage. The stored-logic-state technique may be used with algorithmic pattern generation, so long as the outputs have been recorded from a known-good microprocessor.

Applying system-testing techniques

A major difference between a microprocessor and most logic-circuit boards is the intelligence of the microprocessor, which gives it a self-test capability. Therefore, one effective test technique is to operate the device in an environment similar to its actual application and to program it to do the same kind of operations. While this is not an exhaustive nor even a worst-case test, it is a cost-effective test for most users and it can be expanded as required by the failure experience in the product. There are three system-testing techniques suitable for microprocessor testing (Table 2).

In the simplest technique, a memory (instructions and data) and a means of monitoring the microprocessor outputs are required. The results of each diagnostic routine are compared to manually generated expected results. This is the test technique used by most users who build their own dedicated testers.

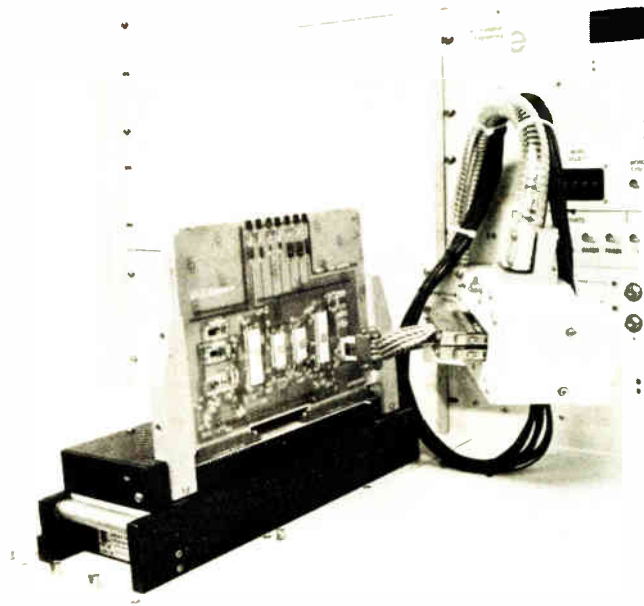
The diagnostic routines start with as few of the microprocessor functions as possible in order to verify the correct operation of the initial instructions. They build upon portions already tested, as new instructions or instruction sequences are tested.

This technique will identify only the failing instructions, rather than the specific problem within the microprocessor, since the output responses can only be checked after groups of many internal operations. However, this is adequate for most users, who are concerned only with isolating defective devices, rather than analyzing the causes of the failure.

The two other system-testing techniques compare the outputs of the microprocessor under test to a known-good processor or to stored signatures, such as transition counts or checksums, that have been recorded from a known-good device. Using checksums as the stored signatures is the approach of the MEX 68CT, the low-cost tester of large-scale integrated components developed by Motorola Semiconductor Products, Phoenix, Ariz., for its 6800 family.

Testing microcomputer boards

Once a microprocessor is assembled onto a printed-circuit board that includes random-access and read-only memories and other LSI logic circuits, that board is a microcomputer—which is more difficult to test than the average logic-circuit board. The microcomputer is a complex subsystem with few control or test points available at the board-edge connector. Also, its timing requirements usually are faster than test rates of most general-purpose board test-systems.



Guided probe. A high-speed functional board-test system like Instrumentation Engineering's System 390 can apply conventional guided-probe fault-isolation techniques to a fully loaded microcomputer board, despite the high data rates for the processor.

Several approaches can test microcomputer boards. The board can be tested with a self-diagnostic program in which the microcomputer is exercised like a system. Since this technique will not isolate faults on the board, most users will want to test the board's fault-isolation techniques first.

If a socket is used for the microprocessor, leads from the test system can be plugged in before the device is inserted. Then in-circuit ("bed-of-nails") testers or conventional logic-board testers like the L125 logic-board tester from Teradyne Inc., Boston, Mass., (shown on p. 125) can test for faults on the rest of the board. When a tested microprocessor is inserted, there is a high probability of the microcomputer functioning correctly.

In some cases, the conventional logic-board test system can provide input patterns to exercise the complete microcomputer board. However, the typical test rate of such systems is too slow to exercise the microprocessor directly. The two approaches used to accommodate this speed difference are a buffer memory to store a sequence of patterns that can be applied to the microprocessor in a burst and a procedure in which the tester forces the microprocessor into a wait mode until the tester is ready for the next pattern.

Another approach is the high-speed functional board test systems, such as the 390 from Instrumentation Engineering, Franklin Lakes, N.J. (shown above), which can apply large numbers of patterns on many board pins and use conventional guided-probe fault-isolation techniques despite the high test rate. These systems can provide confidence in the correct operation of the microcomputer board, including parametric and dynamic testing. However, their high cost limits their use to the very-large-volume users of microprocessors. □

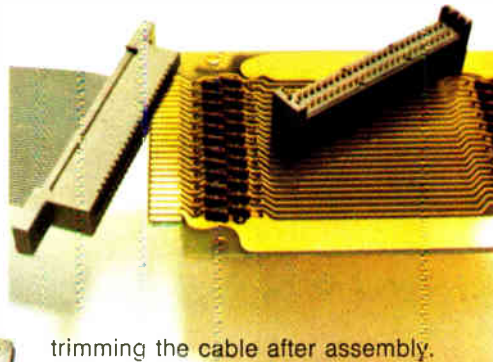
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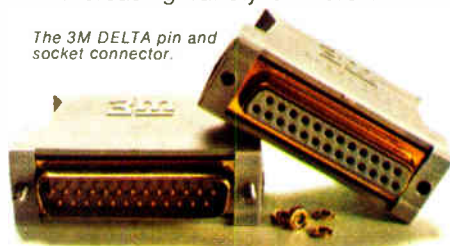
trimming the cable after assembly.

Connector units provide positive alignment with precisely spaced conductors in 3M's flat, flexible PVC cable. The connector contacts strip through the insulation, capture the conductor, and provide a gas-tight pressure connection.

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Assembly-cost savings are built in when you design a package with "Scotchflex" flat cable and connectors. But more important, 3M Company offers you the full reliability of a one-source system: cable *plus* connectors *plus* the inexpensive assembly aids that crimp the connections quickly and securely (with no special operator training required).

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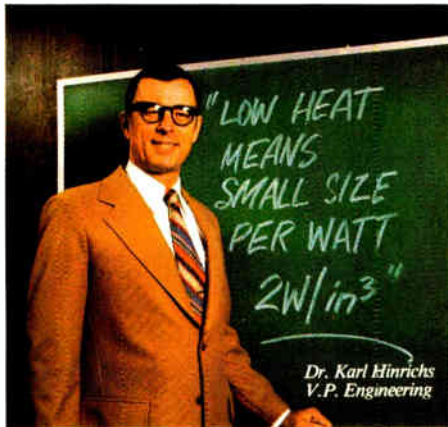
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THE BIG SWITCH

(and Powertec)

Why Switchers?



1. Twice the efficiency for a more economical, reliable system

Efficiency ratings of 80% are common in switching-regulated power supplies, compared to 40% or less for linear-regulated supplies. For the same output power level, then, the switched supply throws away only 1/9 the heat.

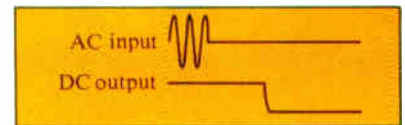
requires less space for sinks and fans. For the user, it means a smaller system . . . or more capability in the same package.

3. Fewer high-temperature, high-power components for improved reliability

Switching technology can replace the 22 hot (120°C Rise) power transistors of a 600-watt linear supply with 4 cool (20°C Rise) transistors. Also, the power-sharing resistors are eliminated, and both storage and filter capacitors are greatly reduced in size. The parts count of a switching regulator is higher, but the additional components operate at very low stress levels and do not add appreciably to the failure rate.



energy storage is performed "off-line" at high voltage (energy storage improves with the square of the voltage, while electrolytic capacitor volume is proportional to voltage). A switching-regulated supply can readily keep output voltages within regulation limits for 30 msec following loss of AC input power.



This represents a substantial improvement over the normal 2 msec achieved by linear power supplies where the cost and size of comparable storage are excessive.

6. Not completely a bed of roses

While advantages of switching regulators far exceed disadvantages, there are certain characteristics which require close consideration before final selection.



Switching generally produces an order-of-magnitude more EMI, both conducted and radiated, so that shielding and filtering must be integral to the design. Also, an order-of-magnitude difference in response time between switching and linear regulators dictates that a switcher be designed with adequate output capacity.

Below 300 watts, control circuitry cannot be appreciably reduced, so that low-power switchers are more expensive than the series equivalents. Above 300 watts, however, the inherent power-saving advantages of switching technology dominate, yielding lower costs at higher power.

SOME PRIME APPLICATIONS

- Add-on memory systems
- Computer main frames
- Telephone systems
- Display consoles
- Desktop instruments
- Data acquisition systems

Can you afford to waste 1750 watts?

AC INPUT POWER 2500 WATTS
(For 750 Watts DC output)

Conventional Series Regulated Design.
Efficiency = 30%



DC OUTPUT POWER 750 WATTS
DISSIPATED POWER 1750 WATTS (Wasted)

Powertec's New Super Switcher
Efficiency = 80%
(Model 9N15-50)

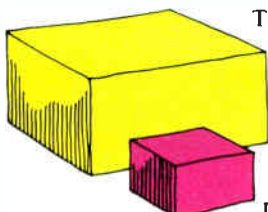
937 WATTS



750 WATTS
only 187 WATTS

This reduction in wasted power and heat-removal burden results in lower operating costs. Lower temperatures mean longer life for both supply and system.

2. One-fourth the size and weight reduces the size of your system



The same output power is available in less than 1/4 the size and weight of conventional supplies. High-frequency magnetics are small,

and less capacity is required to smooth high-frequency ripple. The low heat loss

4. Operation under brown-out conditions

Switcher operation over a +10/-20% line is available. A linear-regulated supply operating over a +10/-10% line would have to increase dissipation by 30% to meet a +10/-20% line requirement. A switching regulator's efficiency is nearly independent of input voltage range.

5. A 30-msec UPS for reduced down time

Energy storage time (carryover) is greatly improved over linear designs because

IS TO SWITCHERS

leads the way)

Why Powertec?



It isn't that we're not fighters. Over the years we fought our way to the top in open frame and sub-module power supplies. We fought hard for our position of leadership by developing new, innovative techniques . . . and by producing the highest quality power supplies at competitive prices.

This determination to "lead the way" is why we have placed such heavy emphasis on switching technology during the past five years. It's why Powertec's line of SS Series Super Switchers is already considered the industry standard . . . and why, today, there are over 4100 SS units in use throughout the world.

Good reasons for choosing Powertec switchers

Efficient, Small and Light

The SS Series case is a compact 10 x 7 1/4 x 5 inches. It weighs a remarkably light 12 pounds. Yet efficiencies of up to 80% are attained! This combination of efficiency and small size results in the highest warts/in³ available today.

Modularized by Function

Each Super Switcher uses functionalized modular P.C. boards to eliminate most wire harnessing, reduce potential high pot

failures, and increase reliability through design simplification.

Cyclic Testing and Burn-in

Each SS undergoes a 24-hour burn-in with cyclic testing where, at elevated temperature, AC input is turned on and off, the load step changed from N.L. to F.L. to N.L., and output terminals short circuited on and off during switching. Dependable long-life performance is assured, with minimum danger of "infant" failures.

Master/slave Capability

Up to four units can be paralleled on an *equal load sharing* basis . . . without power supply modification.

Advanced Features

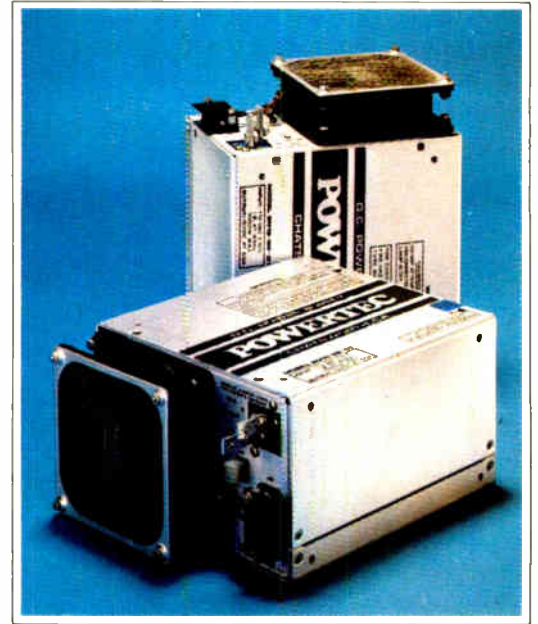
Slow turn-on circuitry protects against high line current surges. Energy storage time (carryover) assures output voltage within regulation limits for at least 30 msec. Overload and overvoltage protection, logic inhibit function, remote sensing, and remote voltage programming are standard features.

Broad Model Range

The SS line offers ten standard models, with outputs from 2V, 200A to 28V, 28A and an exceptionally wide range of inputs. Each model is programmable.

Highest Quality Components

Premium-grade low ESR capacitors are designed into output filter circuitry. A long-life fan and large internal heatsinks provide efficient cooling in any mounting plane.



Summing it up

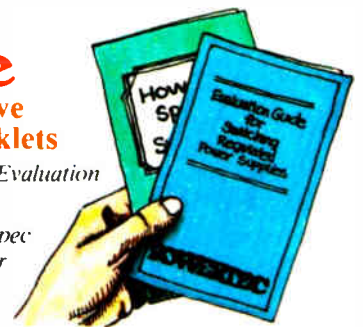
Any relatively new technology demands close evaluation of a company's reputation and past record. Powertec invites just such an evaluation . . . by you, personally. We're confident that our SS Series is unrivaled in quality, craftsmanship, and design. We're also confident that we can answer any questions or help solve any design problems you may have.

Just give us a call, or send us your specs and a statement of your requirements.

DC Output				
Model Number	Voltage Nominal	Current @ +40°C	Efficiency (Typical)	Price
9N2-200	2.0V	200A	55%	\$695
9N5-150	5.0V	150A	80%	\$695
9N5-120	5.0V	120A	65%	\$625
9N6-100	6.0V	100A	65%	\$625
9N12-50	12.0V	50A	75%	\$625
9N15-50	15.0V	50A	80%	\$625
9N17-42	17.0V	42A	80%	\$625
9N20-40	20.0V	40A	80%	\$625
9N24-33	24.0V	33A	80%	\$625
9N28-28	28.0V	28A	80%	\$625

Free Instructive Booklets

1. Switcher Evaluation Guide
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Ti's TMS 1000 series is unique among microprocessors. Versatile. Flexible. Cost-effective. For applications requiring economy, small size, low power, and high reliability. Printer controllers. Remote sensing systems. Cash registers. Appliance controls. Automobiles. Vending machines. Electronic games. Industrial automation. Communication systems. Smart terminals. Peripheral equipment. Test instruments. Gas pumps. Credit card verifiers. Telephone controls. Multiple timers. Data terminals. Traffic light systems. And many more.

Computer on a chip.

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Now, you can use microcomputers in a wide variety of applications where previously they were prohibited by economic and design considerations. The age of the pervasive microcomputer is here in the form of TI's TMS 1000 series: an ALU, memory, and I/O all on a single chip!

Cost-Effective

Already in volume production, this field-proven, p-channel MOS series of one-chip microcomputers is extremely low in cost compared to other design approaches.

For example, the best alternate approaches are 4-bit microprocessor devices generally requiring five to seven individual packages to do what one TMS 1000 does. Considering expenses such as stocking, pc board costs, component costs, testing, and inventory, the cost for production runs using such kits exceeds the single-chip TMS 1000 approach several times over.

Assembly costs are substantially lowered by the significant reduction in package count; and a TMS 1000 single-chip approach greatly enhances system reliability.

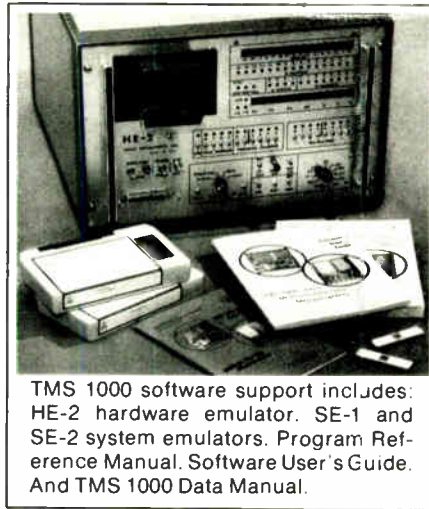
Design Flexibility

To help you match microcomputer to specific application needs, the TMS 1000 series is family-engineered to provide flexibility for a wide range of applications. The TMS 1000/1200 are basic 1024-instruction ROM microcomputers, ideal for low to medium complexity applications.

The TMS 1070/1270 members of the family are identical to TMS 1000/1200 but allow direct interfacing to high-voltage indi-

cators such as the popular neon type displays.

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Software and Prototyping Support

The fully supported TMS 1000 family offers a variety of design aids to assist you with your specific application. For example, the SE-1 or SE-2 system evaluators are chips functionally identical to the TMS 1000/1200 and TMS 1100/1300. They can be combined with external instruction memory so you can check your instruction programming before shifting into volume production.

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Worldwide timeshare software is available for simulator and

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Complementing the TMS 1000 series is TI's new TMS 1976 Capacitive-Touch Interface Circuit. It converts outputs of a capacitive-touch keyboard into signals compatible to the TMS 1000 series for applications using touch-to-operate controls.

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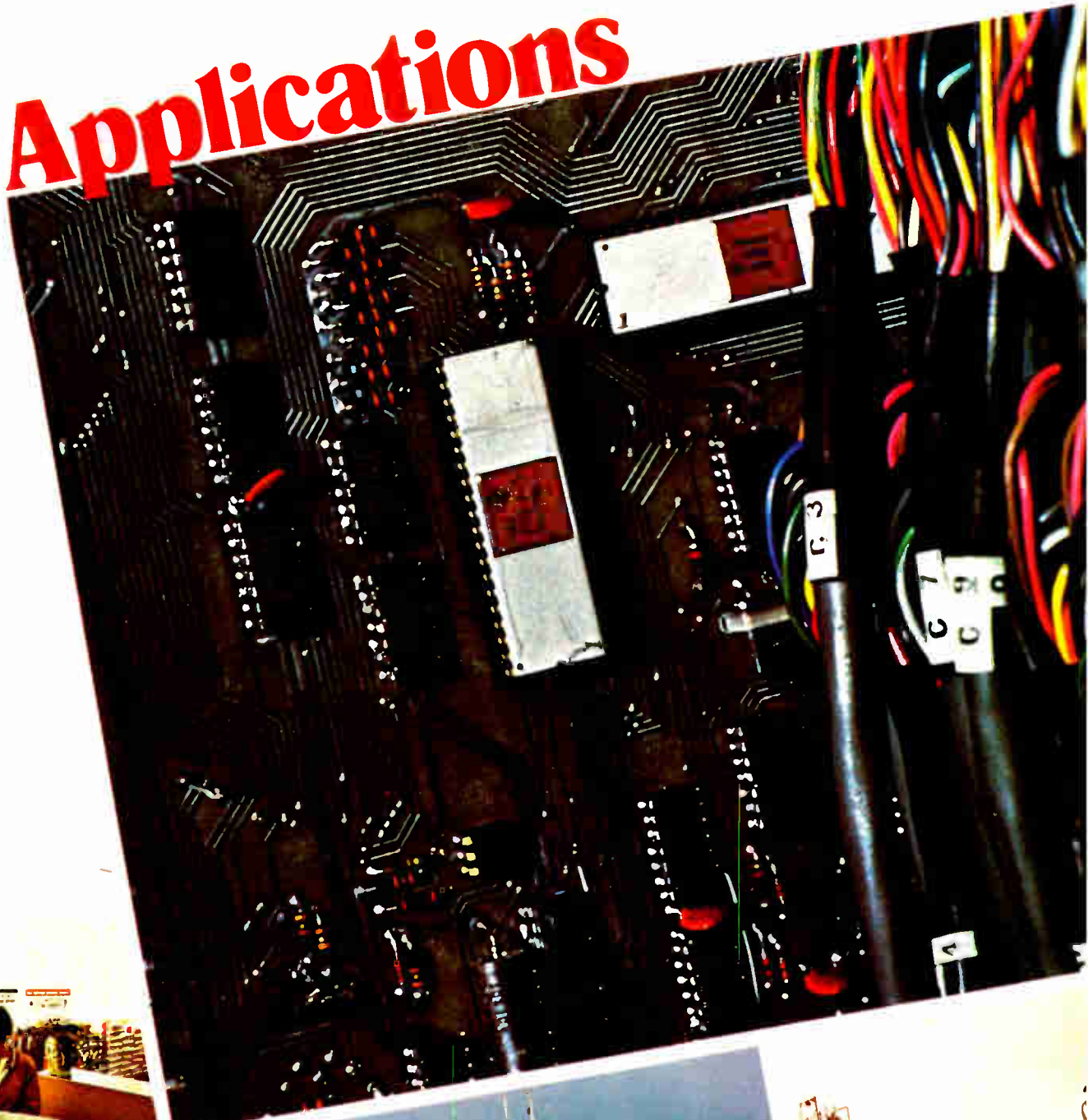
With such a vast range of applications, the TMS 1000 series will be used by some who are not totally familiar with electronic designs. TI's established network of field sales personnel backed by field-located microprocessor specialists will support your design efforts. TI also provides videotape instruction on a loan basis, as well as a full, inexpensive training course conducted in Houston. TI's applications staff is standing by to provide additional support. From the idea to the finished product TI will assist in design, training, and service.

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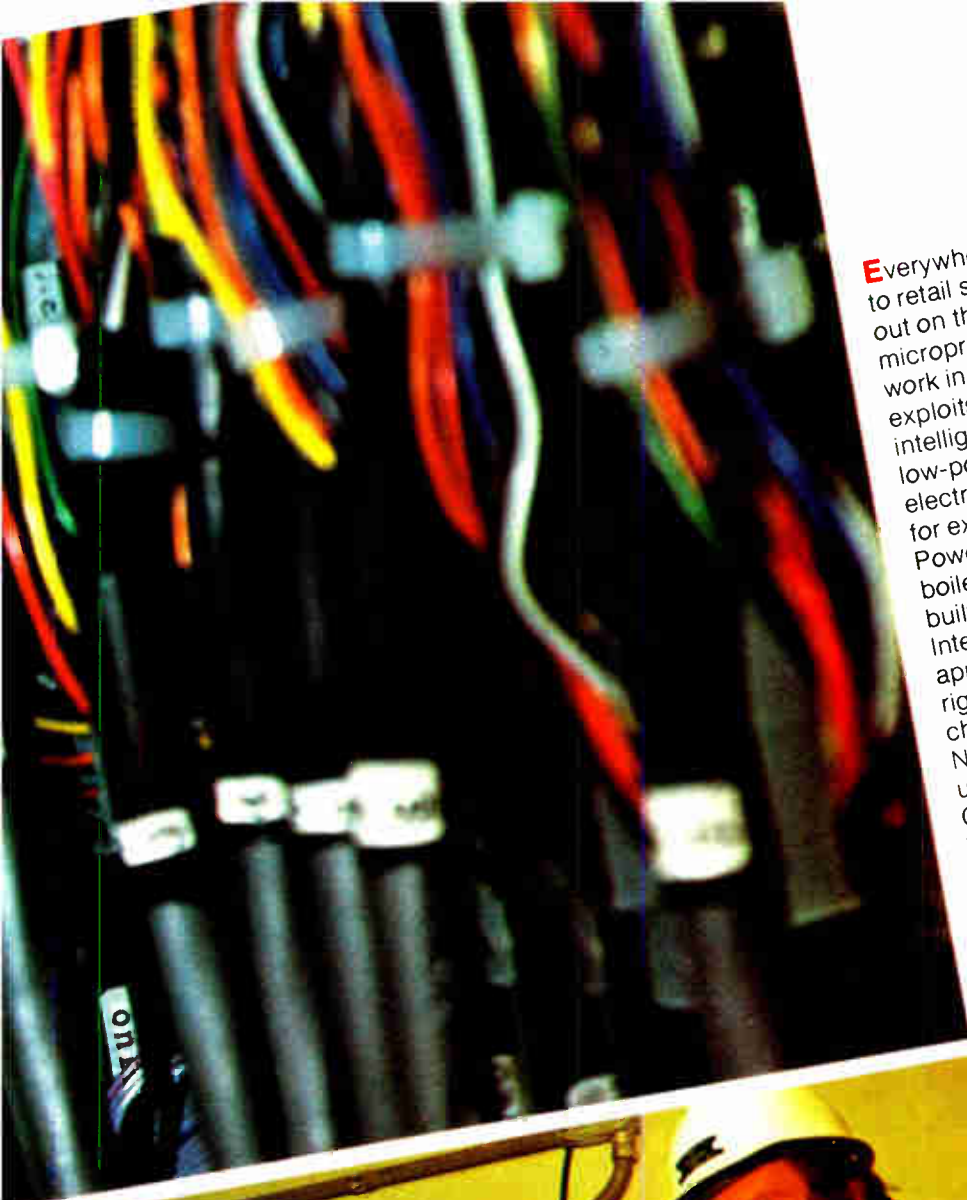
TEXAS INSTRUMENTS
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Applications



World Pacific History





Everywhere, from factories to retail stores to homes to out on the high seas, microprocessors are at work in equipment that exploits their programable intelligence, versatility, and low-power operation. In electric power production, for example, the Diamond Power Specialty Corp. uses boiler-cleaning equipment built by PCS Inc. around Intel 8080s (top). Other applications are (left to right) a supermarket checkout terminal made by National Semiconductor using the IMP 16C; a Canadian Fisheries and Marine Service boat carrying a herring shoal estimator, also fabricated with an IMP 16C; an oil refinery controlled by a Honeywell TDC2000 computer system based on a GI 1600; and a massive grain storage center that uses a Howe Richardson Scale Co. bulk-weighing system built around an Intel 4040. In the following pages, microprocessor users tell how microprocessors helped them solve design problems to provide improved equipment performance.



Users' ingenuity exploits device versatility

Wherever low-cost digital control is needed, microprocessors are taking over. In this section, system designers analyze their experience with 14 successful applications.

Bit-slice processor converts radar position coordinates

by Richard J. Smith
RCA Corp., Moorestown, N. J.

Ship-borne radars, like sailors, need to get their sea legs, and so they must convert the variable location-coordinates to a fixed-reference coordinate system. The radar's computer can do this, but only at the price of placing a heavy load on its central processing unit—the conversion must be updated every 5 milliseconds; the computations involve generating sines and cosines and must be performed with 24-bit precision. Introducing a microprocessor to do the task conserves CPU capacity.

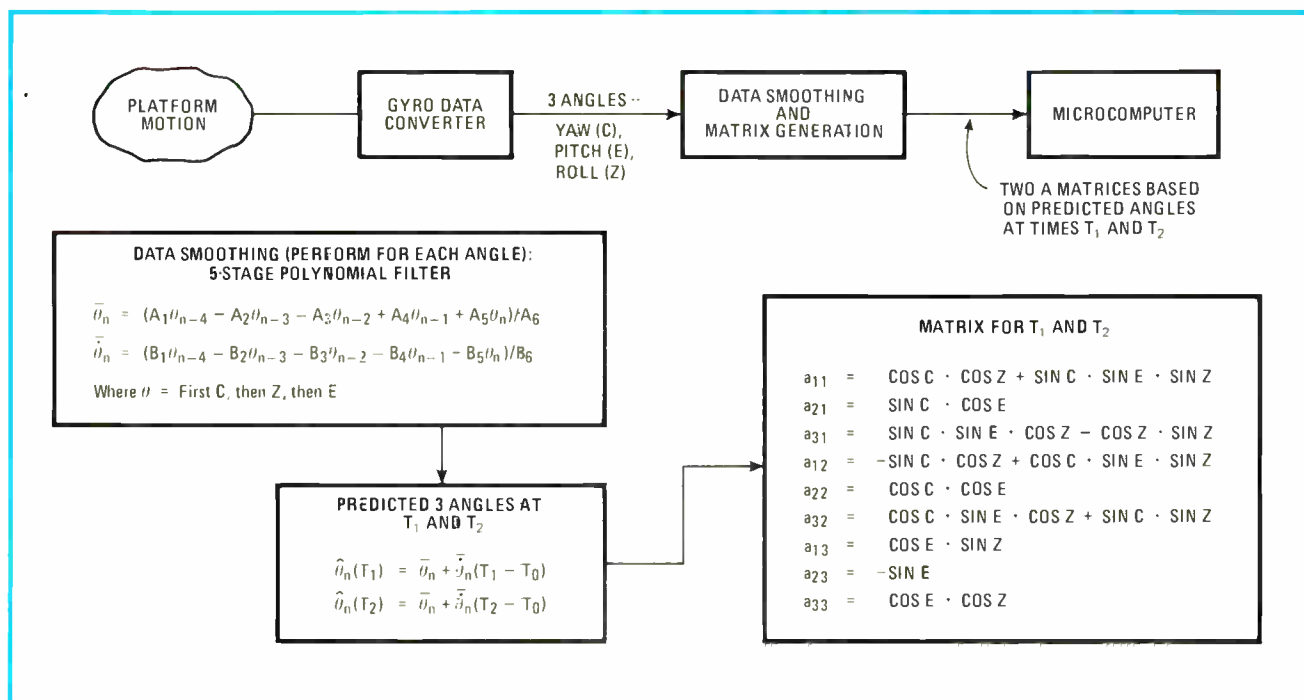
In the coordinate conversion (Fig. 1), three position angles (roll, pitch, and yaw) are sampled and digitized by a gyroscope data converter at time T_0 , then

smoothed using a polynomial filter. The A matrix, based on these variable coordinates, is multiplied by a reference matrix.

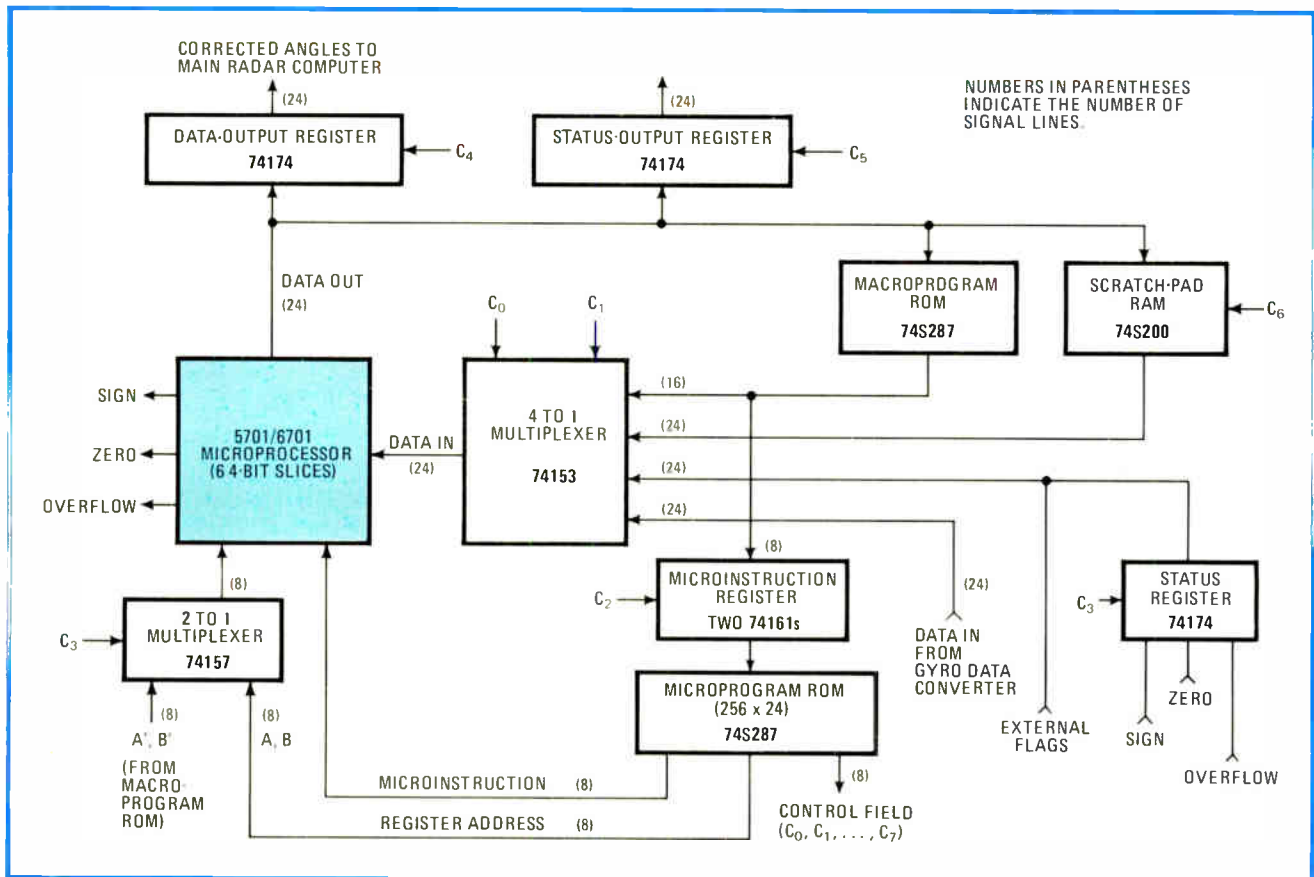
The rate of change for each angle is determined, so that the position at future times T_1 and T_2 can be predicted. The predicted angles are used to calculate their A matrices, which are multiplied by the reference matrix. The corrected coordinates are fed into the main computer of the radar system.

But removing the bulk of the conversion computations from the central computer requires considerable extra hardwired logic. Initial estimates for one system were 250 4-by-4.5-inch printed-circuit cards (using transistor-transistor logic medium-scale integration).

A microprocessor seemed to be the obvious means of simplifying the hardware; however, throughput and word-size requirements meant that a word-oriented processor such as the 8080 or IMP-16C could not be used. Furthermore, none of the word-oriented devices



1. **Coordinate conversion.** Variable coordinate angles of a shipboard radar platform are referenced to a fixed coordinate system 200 times per second by the data readings and processing indicated here. To avoid loading down main radar computer with these computations, they are performed in a bit-slice microprocessor. The entire computation is performed in less than 3 milliseconds.



2. 24-bit microcomputer. Six 4-bit microprocessor slices in parallel, plus other TTL chips, make up a general-purpose computer. The general-purpose instruction set is in the microprogram ROM; the specialized instructions that adapt the computer for coordinate conversions are stored in the macroprogram ROM. Input and output data are 24-bit digitized values of roll, pitch, and yaw angles.

could be guaranteed over the temperature range required in the military specifications for the radar system. The solution is to use a bit-slice processor, and the Monolithic Memories MMI 5701/6701 was selected.

This large-scale-integrated chip is essentially an arithmetic/logic unit and a 16-word register file (a multipoint random-access memory) in one 40-pin package.

Eight instruction lines decode to 17 internal control lines that determine the operation to be performed. The A-select and B-select lines address the register file to determine the source arguments to the ALU. The B-select lines always determine the destination register where the result is stored.

Operations such as add/subtract, shift, and store can be performed in a typical 4-bit device in one 200-nano-second cycle. Paralleling 4-bit slices permits applications such as this one. It does increase the cycle time because the carry bit must propagate through all slices. However, look-ahead generators can minimize the increase. Here, 256 operations can be performed via the 8-bit instruction fed into the read-only memory.

A bit-slice microprocessor requires more hardware than a word-oriented processor because the program of machine-level instructions is in external hardware. However, there are compensations: expandable word size, speed, and flexibility.

Although reflecting the application to the radar system, the block diagram in Fig. 2 essentially defines a

general-purpose 24-bit microcomputer. There are a macroprogram and a microprogram, each stored in its own read-only memory.

The macroprogram adapts the microprocessor to a particular purpose. For the coordinate-conversion application discussed here, the instruction set contains all of the steps needed for the computations that are listed in Fig. 1: input/output handshaking, a Taylor series for calculating sines and cosines, a reference-coordinate matrix, algorithms for matrix multiplication, and the like.

Tailored by the macroprogram

The microprogram is more or less a general-purpose instruction set, tailored to a specific application by the macroprogram. In fact, a combination of microinstructions defines a macroinstruction, while the number of instructions within that combination, or routine, depends upon the macrooperation being performed.

The macroinstructions specify start addresses for the microroutines used repeatedly by the macroprogram, which is 16 bits wide and expandable to 2^{24} words. The eight most significant bits of each macroprogram word define the start addresses, and the eight least significant bits specify the processor's register addresses or addresses for program branches.

One of the processor's two register addresses acts as a counter, keeping track of the sequencing through the

macroprogram, under the control of the microprogram.

The microprogram ROM controls the microoperations by an 8-bit instruction to the microcontroller, the microprogram control word, and two 74161 4-bit register addresses. The register does the sequencing through the microprogram. During the fetch cycle of a microroutine, control bit C_2 in the microprogram is set, enabling the register to be loaded from the start address register of the macroprogram.

The microinstruction at this address resets C_2 so that the 74161 also acts as counter. It is clocked at the end of each microcycle. The microregister sequences through the microprogram until another fetch cycle is encountered, at which time a new 8-bit address is loaded.

Besides C_2 , the microprogram has seven other control bits. This 8-bit control field (C_0 . . . C_7 in Fig. 2) acts as an event sequencer for all the hardware. During certain microinstructions, individual control bits are turned on and off, controlling the state of the hardware. For example, if C_4 is set, the data-out register is loaded from the microcontroller's output lines.

Bits C_0 and C_1 control the 4-to-1 multiplexer, which selects input data to the microcontroller. The data may come from the macroprogram, the scratch-pad random-access memory, the data-input register, or the status register. The RAM and the macroprogram ROM share an address, with the multiplexer distinguishing them.

Bits C_4 , C_5 , and C_6 control, respectively, the data-out

register, the status-out register, and the RAM write command. The 2-to-1 multiplexer selects addresses for the microprocessor's register file, with C_3 choosing the address from the microprogram or the macroprogram.

Bit C_7 may control external logic, whose status may be brought in and tested via the external flag lines. External logic systems can monitor through the status-output register.

Only 38 pc cards

The hardware in Fig. 2 requires 38 4-by-4.5-inch pc cards and is designed to operate conservatively at 2 megahertz (500-ns microcycles). This means that register-to-register operations are performed in 1 microsecond, and a 24-bit multiplication in 14 μ s.

The extent of the detail in this article is rather superficial, but the intent is to give an overview of a bit-slice microprocessor application operating under two levels of ROM control. The devices are very flexible to use, and logic designers should feel comfortable with them since they are specified at chip level, as are other medium-scale and large-scale integrated devices.

Too often, when trying to evaluate microprocessors, designers are intimidated by the software aspect of word-oriented microprocessors. If they approach the bit-slice microprocessor as they do the MSI functions that perform the same basic tasks, they can take advantage of some specialized designs in one LSI package.

Teleprinter redesign reduces IC count

by Frederick B. Scholnick
Compro Corp. Costa Mesa, Calif

Reducing the number of integrated circuits from 91 to 12 was reason enough to redesign a 30-character-per-second print mechanism. But simplifying the control logic with the Fairchild F-8 microprocessor chip set brought significant other benefits, such as power and cost savings. The print mechanism is included in a family of teletypewriter terminals intended for interactive communications and word-processing communication applications.

All of the logic required for dynamic control of the print mechanism and status and communications in the basic terminal are contained in the F-8 three-chip set and nine additional devices, two of which are standard large-scale-integrated chips. By way of contrast, the same functions required 90 transistor-transistor-logic units plus one LSI package in an earlier version of the terminals.

The redesign using a microprocessor took 40 days. It reduced the logic-board size from 10-by-10 inches to 4-by-4 in. Power dissipation dropped by 50%, and system cost was reduced by 20%. Other processors were considered, but the F-8 required 25% fewer peripheral integrated circuits than its closest competitors.

The F-8 configuration shown in the figure consists of three devices plus 1,024 bytes of external program and

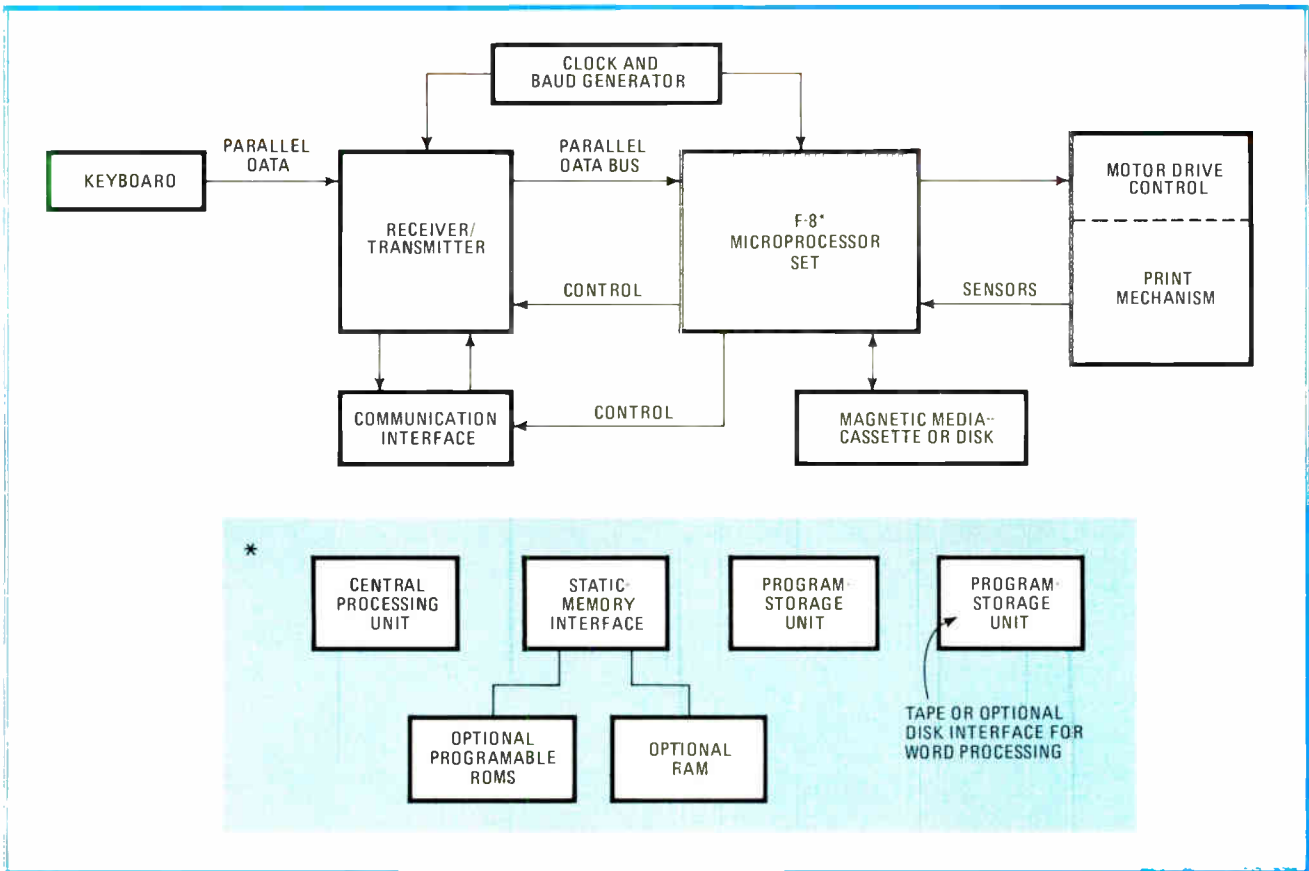
code-conversion read-only memory. The three chips are the 3850 central processing unit, the 3853 static-memory interface and the 3851 program-storage unit. The CPU and PSU each have two 8-bit input/output ports, which handle most of the data and control interfaces with the rest of the system. The SMI and PSU each contain a timer and an external interrupt, which are used in high-speed control of the stepper motor in the print mechanism.

The 64 bytes of scratch-pad memory in the CPU are adequate for the basic teletypewriter terminal. This configuration provides the seven-character buffer for data coming into the printer. Up to 32,000 bytes of external memory can be added if buffers are needed for such applications as a cathode-ray-tube interface or high-speed data transmission for storage in data blocks on cassette tape.

Adding program memory

The addition of one more program-storage unit provides the I/O ports and additional program memory needed for interface with external storage media such as cassette, magnetic tape, paper tape, or floppy disk for word-processing applications. Because the PSU is a compatible member of the bus-oriented F-8 family, it can be added to the system without needing any added IC interfacing.

The serial data interface and keyboard make use of a standard universal asynchronous receiver/transmitter and a standard baud generator. The receiver/transmitter performs bidirectional conversion between parallel and serial data under control of the F-8. It also has the capability of deciphering and adding start-stop and par-



MPU in a terminal. By using Fairchild's F-8 microprocessor set, Compro Corp. was able to reduce the IC count in its teletypewriter terminals from 91 to 12, to reduce system power by 50%, and to cut system cost by 20%. The three-chip set and nine other devices contain all the logic required for dynamic control of the print mechanisms and status and communications in the basic terminal.

ity bits in stream of the serial data.

The baud generator selected is the Fairchild 34702, which permits a simple switch selection of the most commonly used transmission rates—110, 115, 300, 1200, and 2400 baud. Other rates are also possible with multiple-bit selection. The 34702 also contains clock circuitry requiring an external crystal, which provides an output suitable for use as the F-8 clock.

The diagram for the overall system shows that the

F-8 handles control computations for the stepper motors. The only electronics in the system not described are the power amplifiers that drive the motors and the secondary power supply.

Compro's engineers used their own programmable ROM and ignored the built-in program in the F-8 power-storage unit. Production versions of the teletypewriter will have PSUs mask-programmed by Fairchild to the company's specifications.

Digital integrator enhances echo sounder's accuracy

by A. J. Wiebe and Dave Stevens

Environment Canada, Fisheries and Marine Service, Vancouver, Canada

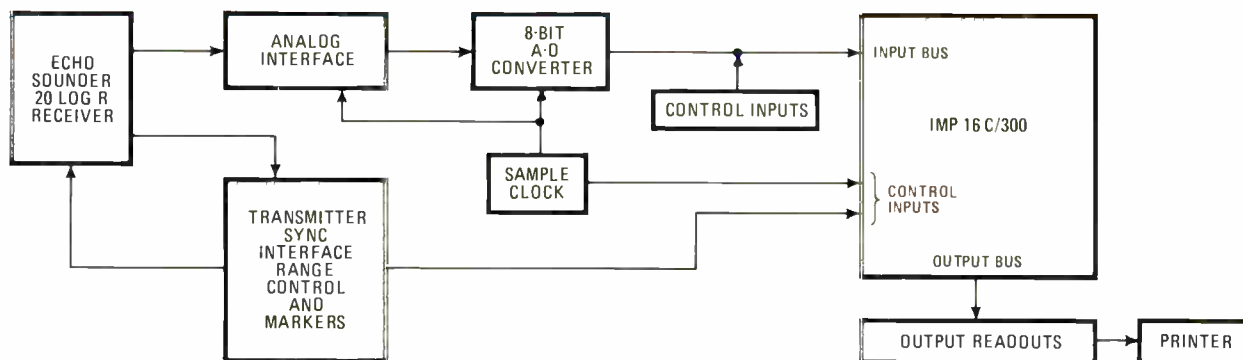
A good way to start an argument with a commercial fisherman for Pacific herring is to tell him how big his catch may be. But the Canadian government does it every year, during the two-month spawning season when the herring are readily available. Government patrol cruisers make echo-sounder estimates of the herring schools to help set harvest rates that will assure enough fish reach the spawning areas to maintain the species.

However, there can be quite legitimate disputes in reading the strength of the signal reflected from a

school of fish—and fishermen have echo sounders, too. To insure accuracy and consistency of sounding estimates, Environment Canada, Fisheries and Marine Service, has developed a microprocessor-controlled integrator that digitizes the data from the sounders.

Besides producing more accurate readings, the integrator increases the precision of the data, by refining the technique for discounting echo signals from the ocean floor. The system is undergoing ocean tests.

With only an echo sounder, the tonnage of herring in a school is estimated by integrating the signal strength over the area of the school. Area is readily determined from boat speed and the time required to cross the school; no subjective evaluation is required, and the determinations are consistent. However, the signal strength is displayed as a line of varying density. The standard method of subjective evaluation of line density



Fishing for signals

Data from the echo sounder is converted into digital words and read when it is above the noise threshold. The analog section of the system is linear for a 20-decibel range of input signals, and a comparator insures that no signals below the threshold enter the memory-data bus. The timing inputs are the echo-sounder pulse and the 2-kilohertz clock. The pulse sets the range of the timing and initiates the computer cycle, while the clock controls the analog-to-digital conversion at a rate of two samples per sound pulse and informs the processor that a sample is available.

The controls include:

- A bottom-level switch to start tracking of the ocean bottom.
- An intensity-variation thumbwheel to adjust for steady or unsteady bottom-return signals.
- A depth-variation thumbwheel for flat or varying bottom configurations.
- Bottom-threshold thumbwheels to set the intensity level above which signals are recognized as bottom signals.
- Range switches to set the time interval for the integration.

- A print switch to produce printing of short-total readouts.

- Another thumbwheel to drop numbers from the right, since only six digits can be shown.

The outputs include:

- The short-total readout, at 10 or 25 sound pulses.
- The long-total readout, at 500 sound pulses
- An intensity readout of the strongest signal in the bottom "box."
- A depth readout of the computer's decisions on distance to the bottom.
- A saturation shift-register with eight light-emitting diodes that flash when the saturation level is exceeded.
- A bottom-tracking LED that indicates the computer is tracking the bottom-return signals.
- A printer for hard copy of long-total readout and, if desired, of short-total readout.

The address bus is used to address all devices and registers. The write-peripheral flag strobes data into displays and into the printer register from the output bus for buffered data. The data-select flag uses a read-memory modified pulse to select on-chip random-access memory or external registers on the output bus for memory data.

often can lead to very variable estimates of school size.

Digitizing the signal strength and integrating this signal over specific time periods produces a number which, when corrected for system calibration, can be multiplied by the area to give a tonnage estimate for the school. The calibration constant is determined from the signal from a known fish density measured in a bait pond.

The cramped wheelhouse of the patrol boats and budget limitations immediately ruled out use of a mini-computer for digital integration. Selection of a micro-processor made the next question a matter of the choice between an 8-bit and a 16-bit device.

30-bit word size needed

In designing the integration program, it soon became apparent that word sizes up to 30 bits would be required for most efficient use of program memory. Double precision on a 16-bit processor obviously was the best way to go. Further, using single-instruction multiplication and division, rather than shift and add, would reduce programing steps. On the basis of these criteria, the National Semiconductor IMP-16C micro-processor was chosen.

This card has 256 16-bit words of random-access memory and 512 16-bit words of programable read-only memory. The program uses 500 of the PROM words, but only about 30 words of the RAM. One reason the program is able to make such minimal use of the read-only memory is that the IMP-16C permits using peripherals as memory instead of as input/output devices. This feature also saves two instruction steps in the program for each input signal.

Depths searched typically are less than 50 fathoms. Transmitted pulses are 1 millisecond in length, and the return is sampled twice each pulse.

Conventional circuits are used to filter a usable amplitude-modulated signal out of the noise coming from the echo sounder. The signal goes through a sample-and-hold circuit to an analog-to-digital converter running off a 2-kilohertz synchronous clock.

Depending on which timing range is used, the echo-sounder repetition rate is 112 or 225 pulses per minute. Short-term integration totals, displayed every 10 or 25 sound pulses but not usually printed out, are valuable chiefly when investigators want to look at smaller segments of a school. For estimating purposes to establish

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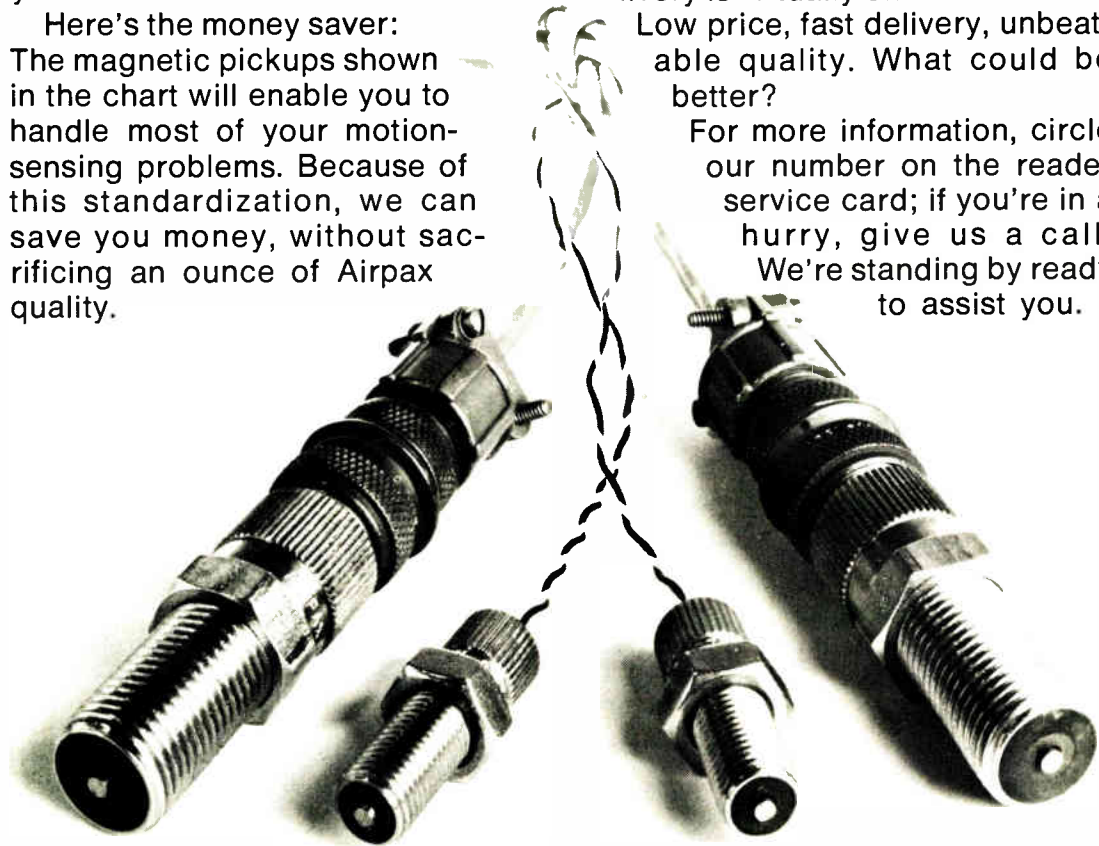
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Operating Temp:	-100 to 225° F	-100 to 225° F	-100 to 225° F	-100 to 225° F
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the harvest rates, long-term integration occurs every 500 pulses and the number is printed out. The microprocessor also marks lines on the echo-sounder's chart to indicate the depths where integration occurs.

The PROM program consists of a main control and five subroutines. The main control program monitors timing functions and accumulates totals. Three subroutines handle displays and printer output, and another one performs binary-to-decimal conversions.

The most complex of the subroutines is bottom tracking. The signal from the bottom must be eliminated from the integration, or else huge errors will occur in the estimate. The cross section of an ideal echo-sounder signal would show a sudden increase in signal strength as the top of the school is detected, along with a falling off of the signal through the school. A sharp drop in signal strength would occur at the end of the school, and

then the bottom signal would increase gradually.

The aim of the bottom-tracking subroutine is to approximate an ideal signal as closely as possible. In effect, the system makes a highly educated guess on the distance to the bottom. Human intervention is possible at any time—and is necessary at the beginning of the procedure because variations in signal strength mean the device can't decide which signals actually represent the bottom. So the operator sets the known depth through control-panel switches.

As the bottom signals rise and fall, the subroutine predicts a maximum and minimum of distance to the bottom for the next pulse. These two limits form a "box," within which the system will recognize the strongest signal as coming from the bottom. If the processor detects the bottom signal getting too close to one of the limits, the box is raised, lowered, or enlarged.

C-MOS processor automates motel phone system

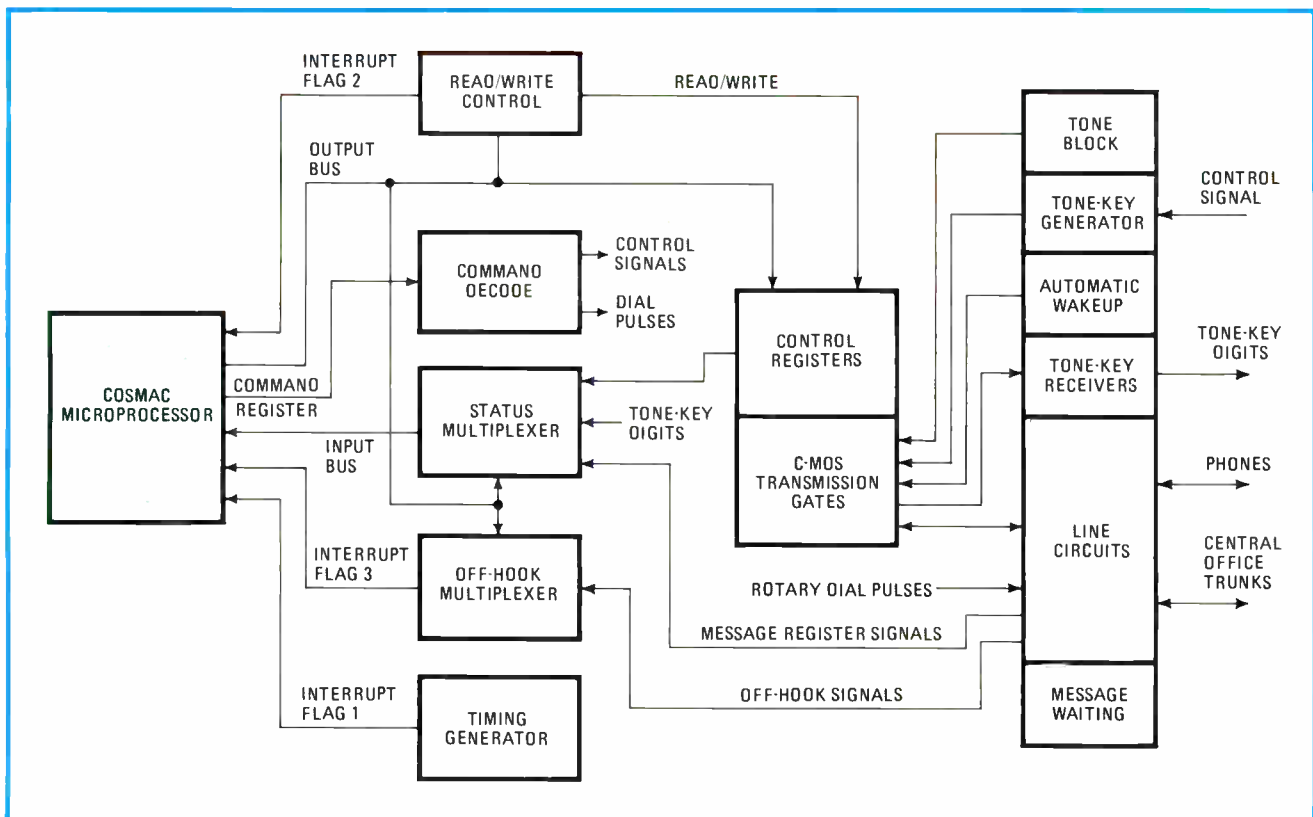
by Charlie L. Jones
Jupiter, Fla.

Most private-branch telephone exchanges aren't expected to produce automatic wake-up calls, but the modern ones in hotels and motels can do just that. The secret to this—and other features needed by the lodging

trade in its telephone systems—is microprocessor control, which permits adapting a PBX to a variety of business applications.

In designing a system that provided needed features for hotels or motels with no more than 112 extensions, an 8-bit complementary metal-oxide-semiconductor microprocessor was selected as the central control section. It provides low power dissipation, a suitable input-output structure and a C-MOS or transistor-transistor-logic interface.

Even without these features, a C-MOS processor would



1. Determining priorities. Key functions of the TDM switch are controlled by commands from the microprocessor via the command-decode module. Interrupt-priority levels are predetermined and assigned interrupt-flag lines. Here the timing generator has highest priority. Eventually there will be more integration on a single chip.

have been the choice. Other parts of the PBX used C-MOS circuits, and a long-term design goal was to put all switch-control circuitry on a C-MOS large-scale-integrated chip to interface directly with the microprocessor.

The device can handle both driven and polled interrupts. By pulling down an input line, extensions gain the immediate attention of the microprocessor, or the processor can periodically scan all lines to determine if service is needed. Cycle time was not critical, since the system need only scan 112 lines every 500 milliseconds.

RCA's Cosmac microprocessor, with up to 32 kilobits of solid-state memory, controls a time-division-multiplexed switch, and formats and transmits data to the peripheral devices. A cassette loads the program into memory, which gives flexibility to the lineup of features that may be offered.

The system interfaces with an integral display console that provides the video terminal, keyboard, and printer most lodging operators want for storing registration information and processing guests' telephone charges. The TDM switch interfaces with the room extensions, outside lines, central-office trunks, and a multibutton operator telephone that serves as inexpensive attendant console.

The microprocessor controls most of the specialized lodging functions through the TDM switch (Fig. 1). It writes data into the control shift registers to make phone connections and can read back data from the registers via the status multiplexer. The registers act as an extension of the microprocessor memory, because their memory is under processor read/write control.

Addressing the off-hook multiplexer permits the microprocessor to monitor all off-hook signals. By scanning these signals, the processor counts the dial pulses and determines which connections should be made.

The status multiplexer scans the message-register signals to keep a running total of all local phone calls from each room. It also reads the digits provided by tone-key receivers. While the system shown in Fig. 1 is equally adaptable to rotary-dial installations, the discussion that

follows assumes the installation is of the newer, tone-key type.

The microprocessor controls the main functions of the switch via the command-decode block. For example, it generates dial pulses and routes them to a central-office trunk line by sending the commands to the command-decode block. The dial pulses go through the line circuits providing the proper interface to the trunk lines. The ability of the microprocessor to provide dial signals for outside numbers is necessary for the abbreviated dialing feature, in which frequently called numbers may be reached by keying in a pair of digits.

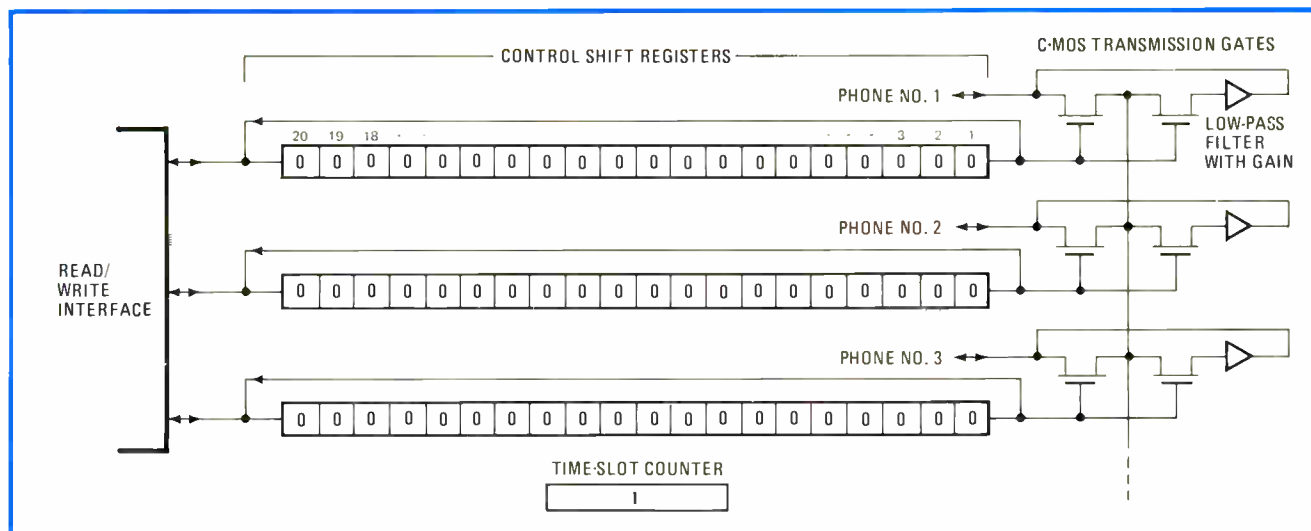
The control shift registers (Fig. 2) for each extension interface with MOS switches that actually are C-MOS transmission gates. The gates conduct whenever a logic 1 appears on the output of the controlling shift register, making the input to the transmission gate go positive.

The recirculating shift registers are being clocked at the same rate as the time-slot counter, which determines which one of the 20 time slots—that is, bit positions—for each shift register is controlling the conduction or non-conduction of the switch. At the point shown in the figure, no phone connections have been made.

The microprocessor can read or write to a specific time slot in a shift register by providing a read/write command and the number of the slot to the decode block. The command is executed when the counter turns up the same time-slot number as the one provided. The command affects all shift registers during the designated time slot.

When any phone is taken off-hook, the microprocessor writes a 1 in time slot 1 of the shift register controlling that phone and of the shift register controlling dial tone. It also sets a bit in time slot 1 of the register that control the gating of the signal to the receiver. As the bit circulates around each of these three registers, a sample of dial-tone signal is taken each time it reaches the last stage of the register. This sample passes through the low-pass filter, and the phone receives a dial tone.

As the caller begins to key in the numbers, the micro-



2. Making connections. Setting control bits in the shift registers initiates the proper connections to route telephone signals through transmission gates. The low-pass filter with gain recreates the analog audio signals.

processor removes the 1 stored in time slot 1 of the dial-tone register so that the phone no longer receives a dial tone. As numbers are keyed in, the signal generated from the phone is sampled and reconstructed in the low-pass filter. The microprocessor then reads the digits to determine the telephone number being called.

Making the call

If, in Fig. 2, phone 1 is calling phone 3, the microprocessor writes a 1 in time slot 1 of the register controlling phone 1 and writes a 1 in the register controlling ring-back tone. It sets a bit in time slot 2 of the control register for phone 3 and in the ring-tone control register, which causes phone 3 to ring.

When phone 3 is picked up, the processor writes a 1 in time slot 1 of the control registers for the two phones

and removes the bits in the ring-back-tone control register and the ring-tone control registers. This results in a connection between the phones, and the conversation can begin.

With an eye towards the long-term design goal of large-scale integration, it was essential to control as much of the switching as possible, thereby minimizing the number of small-scale-integration logic circuits needed. But excessive time spent servicing the switch would starve the peripheral devices.

Since it is hard to determine in the early design state how many peripheral operating features will be required, it's hard to decide how much margin for their operation must be left. But too much margin causes the costs to soar. Ultimately, the answer lies in design experience rather than in hard and fast rules.

On-line display terminal fits many different systems

by Toshiyuki Tani

Matsushita Communications Industrial Co., Yokohama, Japan

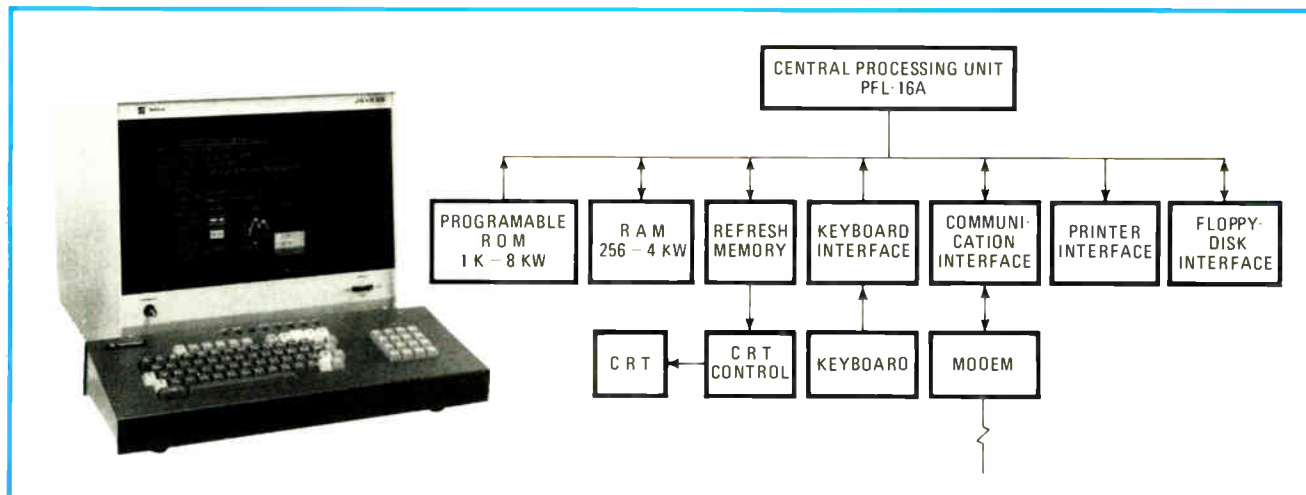
CRT display terminals are very convenient for a good many on-line uses and would attract many more customers if only they cost less. Standardization on a microprocessor-based model is the answer. Instead of building as many models as there are end uses, the designer can make one terminal satisfy a wide variety of business and environmental conditions simply by reprogramming its microprocessor.

The figure shows the microprocessor-based JK-435 cathode-ray-tube display terminal (a), as well as a block diagram of its elements (b). The central processing unit is a PFL-16A microprocessor made by Panafacom Ltd., a joint venture of Matsushita Electric Co. and Fujitsu Ltd. It accepts incoming data from the keyboard via its interface or from, say, a remote computer via the modem and the communications interface. It processes

the data into 11-bit elements for display and into field-control bit-sequences that are not for display. In so doing, the microprocessor acts under the direction of the program stored in the field-programable read-only memory. Any processed data for which it needs temporary storage—or for that matter, any momentary surplus of input/output data—is held in the random-access memory. Lastly, the microprocessor transfers the 11-bit display data to the refresh memory—also a RAM. There it stays while being read out repeatedly onto the cathode-ray tube by the CRT control.

To reverse the process, and read out the contents of the display, the microprocessor picks up the data from the refresh memory and again processes it under the ROM's direction for printout, storage, or transmission.

The PFL-16A microprocessor has a 16-bit word length, a 3-microsecond basic instruction cycle, 33 basic instructions, five arithmetic registers and two index registers, and three interrupt levels. In addition, it can control 256 inputs and outputs. Evidently, it performs almost as well as a minicomputer. But more specific reasons for preferring it to other microprocessors for this display application are:

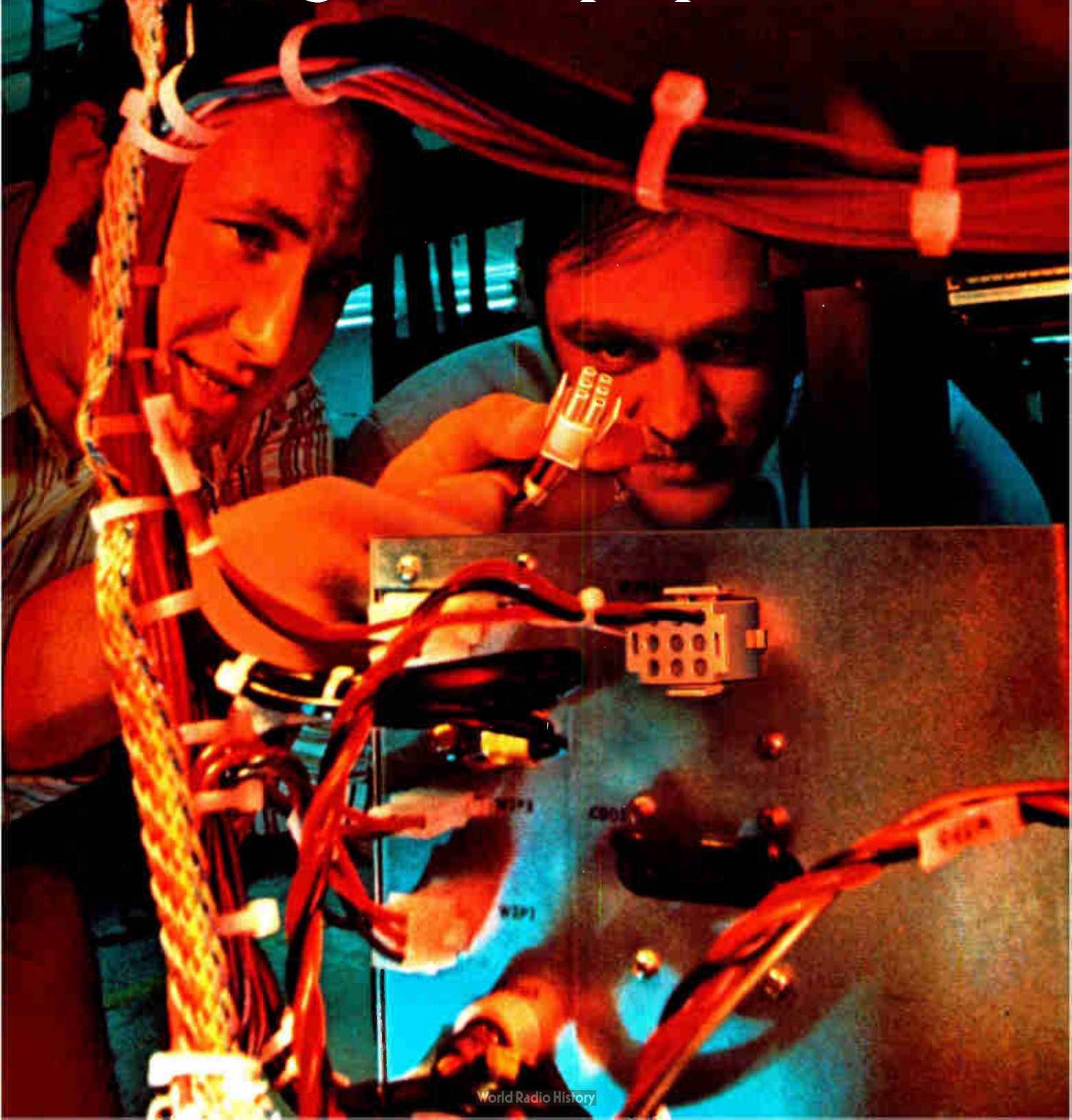


Processor-controlled CRT terminal. Varying the firmware that controls the microprocessor in terminal (a) enables one cathode-ray-tube display to satisfy many different end uses. The CRT can display graphs or characters, including alphanumeric and Japanese characters. Block diagram (b) shows use of PFL-16A microprocessor. Refresh memory stores data that the CRT control reads out for display.

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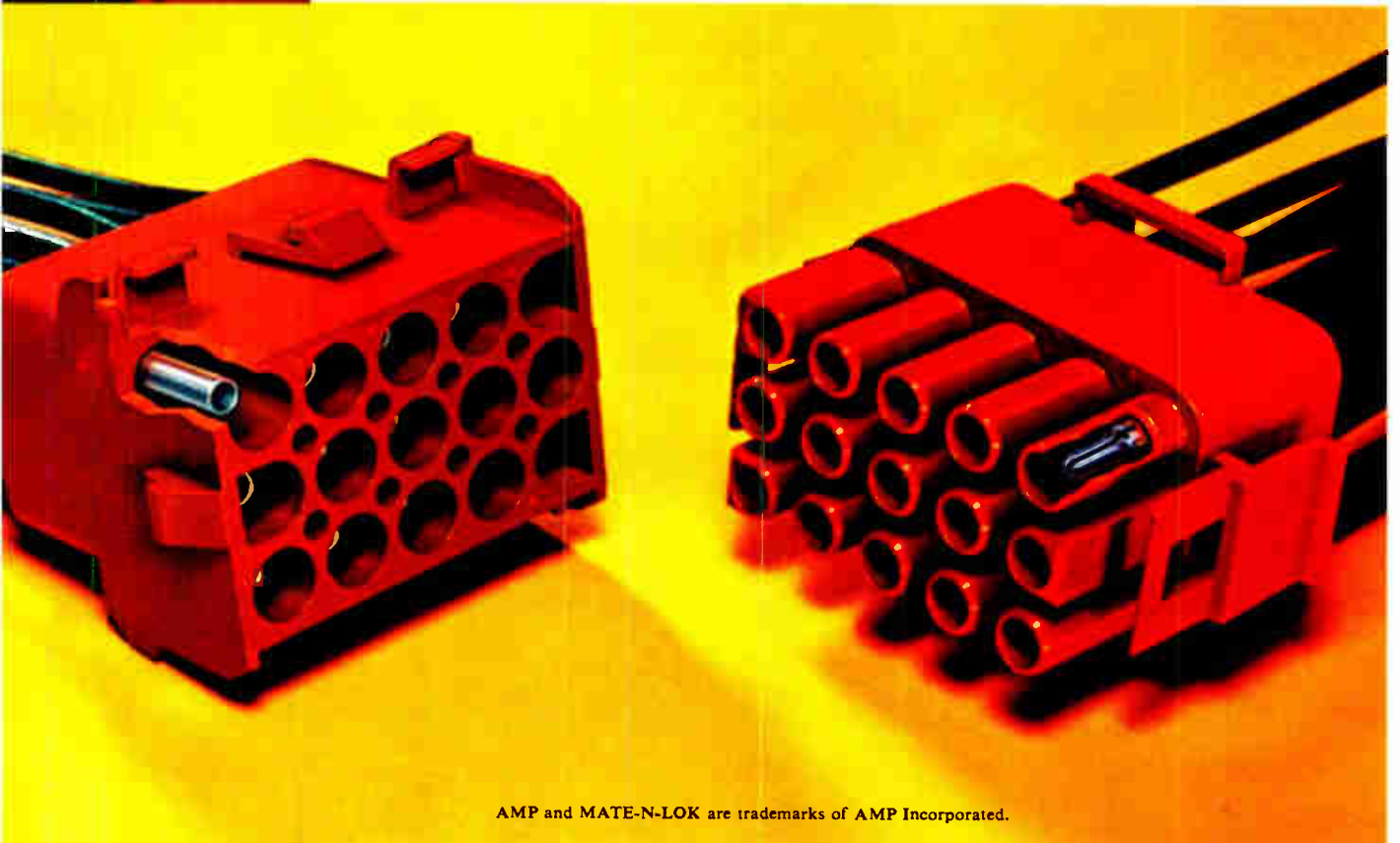
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- The versatility of its addressing system, which includes direct, indirect, and relative addressing as well as an index modifier. This versatility saves many program steps, and thus reduces ROM requirements.
- Instructions that can handle data by the bit, byte, or word, again conserving program space in ROM.
- The 16-bit words, which are better than 4- or 8-bit words for handling the 11-bit display data elements. (More generally, too, 4- or 8-bit microprocessors need more memory and process data more slowly since each instruction requires two or three words.)
- Programing and debugging are simple because one instruction corresponds to one word.

The ROM that stores the control program may contain anything from 1,024 to 8,192 words, depending on system requirements. The RAM can hold anything from 256 to 4,096 words.

Despite the PFL-16A's speed, the retrace rate of the CRT's picture area is on the slow side—approximately 44 hertz. Nevertheless, the images appear free of flicker because the CRT has a P39 phosphor, which can hold a trace for the fairly lengthy period of 200 milliseconds.

What's to be seen on the screen

The 14-inch high-resolution cathode-ray tube can display 24 or 25 80-character lines. Each 11-bit display data element consists of 8 bits for character data, 1 for memory protect, 1 for cursor display, and 1 for graph designation. A total of 128 different characters include alphanumeric, punctuation marks, and Japanese katakana characters. Simple graphics can also be displayed.

The field-control data, which is not displayed, controls the image or field that will follow the one currently on display. This data controls the subsequent field's brightness or darkness, use of ruled lines, character blinking, and even nondisplay.

Besides the alphanumeric and kana characters, the keyboard contains 16 program-function keys, including character insert, character delete, or data transmission. The modem, which links the CRT display to the central computer, comes in two versions: an asynchronous system with speeds of 110, 200, 300, 600, and 1,200 bits per second, and a synchronous system with speeds of 2,400, 4,800, and 9,600 b/s.

An optional printer and flat disk may also be interfaced to the PFL-16A. (The terminal, incidentally, is plug-compatible with the IBM 3270.)

Transfer of data to or from these peripheral units is entirely controlled by firmware—the program in the ROM. Only the interfaces are completely “hard-wired.” Firmware also controls most of the CRT displays such as field protection, field erase, control of numeric field, tab, backtab, character insert, character delete, scrolling, and erase. The terminal units can be connected so that they meet the transmission control procedures at the central computer. If the central computer is equipped with software for other CRT display or terminal units, this terminal can be linked to it with a slight modification of its own software.

In short, the design of this cathode-ray-tube display terminal minimizes the role of hardware while playing up its programability.

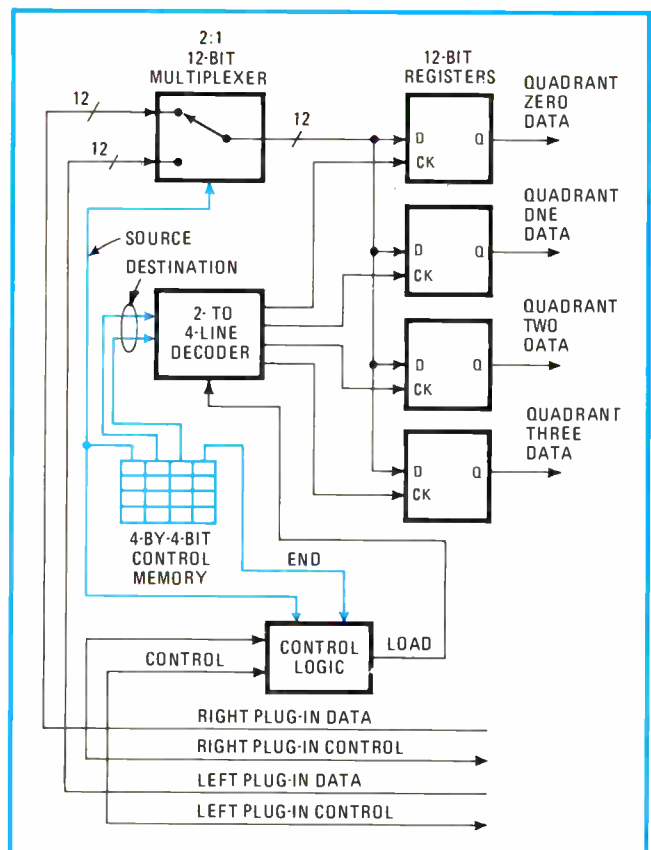
Microprocessor routes data inside programable scope

by Fred A. Rose and Steven R. Smith
Norland Instruments, Fort Atkinson, Wis.

Microprocessors have bred a new species of general-purpose laboratory instruments, with most of the convenience of computer-based systems at a much less inconvenient price. But in Norland Instruments' model NI 2001 programable calculating oscilloscope, an Intel 8080 microprocessor does more than process the input data—it also controls almost all phases of the instrument's operation, from monitoring the front-panel controls to routing the input signals to their correct destinations in memory.

The instrument acquires data rather like a digital transient recorder. It accepts up to four channels of digitized data simultaneously, each channel being up to 12 bits wide and operating at sampling rates up to 1 megahertz. The four channels enter through two plug-in slots, much like the arrangement of vertical deflection

1. Road map. Multi-line data from a number of sources can be directed to any one of several outputs under microprocessor control, even though the device is too slow to handle the data itself. Here, a microprocessor (not shown) programs a 4-by-4-bit memory array that sets up the high-speed logic that is actually the data path.



plug-ins in an oscilloscope. The data from each channel is stored in any one of four random-access-memory arrays, each 12 bits wide and 1,024 bits deep.

The user can manipulate and modify this data under program control for a number of purposes—maybe converting it into engineering units or deriving such quantities as power—and can display the results in a variety of oscilloscope-like presentations. For example, the instrument can simultaneously acquire and digitize a voltage and a current waveform, then multiply the two point by point to produce an instantaneous power waveform. This derived waveform exists in the memory of the NI 2001 as properly scaled values, which can be read out in watts on the screen of a cathode-ray tube along with the original waveforms.

Switching direction

But to revert to the 8080's role as traffic director, the NI 2001 can acquire data in any combination of channels and plug-in slots, and ideally it should also be able to direct data from any channel from either slot to any one of the four sections of memory. But the number of possible combinations is large, and some are prohibited. For example, one section of memory cannot be chosen for more than one channel of data.

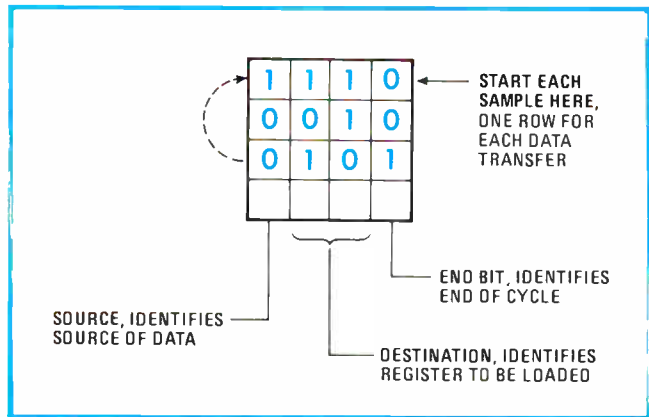
At the same time, the actual data transfer rate—up to 48 bits every microsecond when all four channels operate at 1 MHz with 12-bit resolution—is far beyond the ability of any microprocessor, or even a minicomputer, to process under program control.

The solution to this dilemma is to combine high-speed hard-wired logic for data handling with a microprocessor to control the logic through a control memory (Fig. 1). The microprocessor reads the front-panel switches on the plug-ins to determine how many plug-ins are in use and how many channels within each plug-in are activated. It then verifies that the switch positions are compatible. If the switch positions are not compatible, a red error light is illuminated, and the machine comes immediately to a halt.

Tabling the data

When a permissible combination of front-panel selections is present, the microprocessor writes a table into a 4-word-by-4-bit control memory (Fig. 2). This table forms a control program for a sequential control implemented in hardware, and it provides switching instructions for the various multiplexers involved in the data transfer. The hardware controller transfers the data at the required high rate.

In the control table, the first bit in each line identifies which plug-in is the source of the data, the next two bits identify which of the four quadrants of the memory are to be loaded from this input, and the last bit identifies the final instruction in the array. In Fig. 2, the first word is an instruction to take the data from the first (lowest-numbered) active channel of the right plug-in (1) and transfer it to the memory's third quadrant (11). The second word instructs the hardware to accept data from the first (lowest-numbered) active input of the left plug-in (0) and feed it to the first quadrant of the memory (01). The third instruction takes data from the second active



2. Routing traffic. The 4-by-4-bit control table contains information needed by input-switching hardware to direct digitized input data. The first bit identifies the input, the second two bits identify the output, and the fourth bit identifies the last step in the cycle.

channel of the left plug-in (0) and feeds it to the memory's second quadrant (10). Since the fourth bit of this command is a logic 1, it is the last command in the array, so the instrument will then return to the first word and repeat the cycle.

Evidently, another convention is also needed, and it is employed to keep the control array as small as possible. Whenever a plug-in is interrogated for its unput signal, the first request is for the lowest-numbered active channel, the second request for the next-lowest active channel, and so on. The circuitry to maintain this protocol is within the plug-in; the mainframe of the instrument simply assumes that the plug-in is adhering to the rule.

With the mainframe, the 12 lines from each of the two plug-ins feed into a 12-bit 2:1 multiplexer that selects the proper input based on the first bit of the control table. The output bus of the multiplexer is tied to four 12-bit registers. The clock signal for these registers is a load command generated by control logic. This "clock" strobes a 2-to-4-line decoder which sorts the two center bits of the control array's 4-bit command onto four separate clock lines. Consequently, only the 12-bit register that corresponds to the proper memory quadrant receives a clock signal when its data is present on the 12-bit data bus; the other 12-bit registers remain inactive.

Doing what each does best

Hard-wired logic capable of making the logical decisions required to write the control table would be discouragingly complex, but the programmable microprocessor produces the answers in a straightforward manner. Similarly, the data transfer rate is too high for the microprocessor to handle alone, but, with the help of the microprocessor-written control table, the hard-wired logic easily manages it.

At the time of this design, the only microprocessor with sufficient capability was the Intel 8080. Since then, several comparable units have become available. The 8080 remains an excellent choice for this application, but would undoubtedly have many competitors were the instrument being designed today.

Blood analyzer tests 30 samples simultaneously

by H. Miranda and M. Hatzimmanuel
Union Carbide Clinical Diagnostics, Rye, N. Y.

A microprocessor controls a centrifugal spectrophotometer that analyzes in real time the chemical reactions of 30 blood samples in parallel and prints out the results as well as displaying them on a cathode-ray tube. The instrument, the Centrifichem, performs end-point analysis, which indicates the difference between the initial and final absorbance values of the sample and a reagent, as well as kinetic or enzyme analysis, which requires calculation of the reaction rate.

The Centrifichem, shown in Fig. 1, whirls the samples, contained in 30 cuvettes arranged around the periphery of rotating disk. As the rotor picks up speed, the centrifugal force transfers the reagents from an inner disk to the cuvettes, which have transparent tops and bottoms. The chemical reactions are measured as the cuvettes containing the serum pass through the beam from a lamp mounted at the top of the apparatus. The light can be filtered as desired. The rotor is timed so that the exposure of each chemical reaction in the light beam is long enough that its absorbance peak can be measured, yet is short enough to track the 30 kinetic reactions in real time.

The system performs 18 standard analyses that have been programmed, but the memory has the capacity to define the parameters of 39 different tests. The light transmitted through each sample generates a phototube output that is digitized and processed in the microprocessor circuit, as shown in Fig. 2. The 8-bit system, built around the Intel 8008 microprocessor, has greater capacity and flexibility than a hard-wired system, yet it is less expensive. What's more, the use of fewer integrated circuits provides higher reliability. The Centrifichem is configured in modules—analogue basket, front-panel control, printer, cathode-ray tube, left-hand con-



1. **Test station.** Blood analyzer is arranged for fast, accurate measurements. Hard-copy printout provides permanent record.

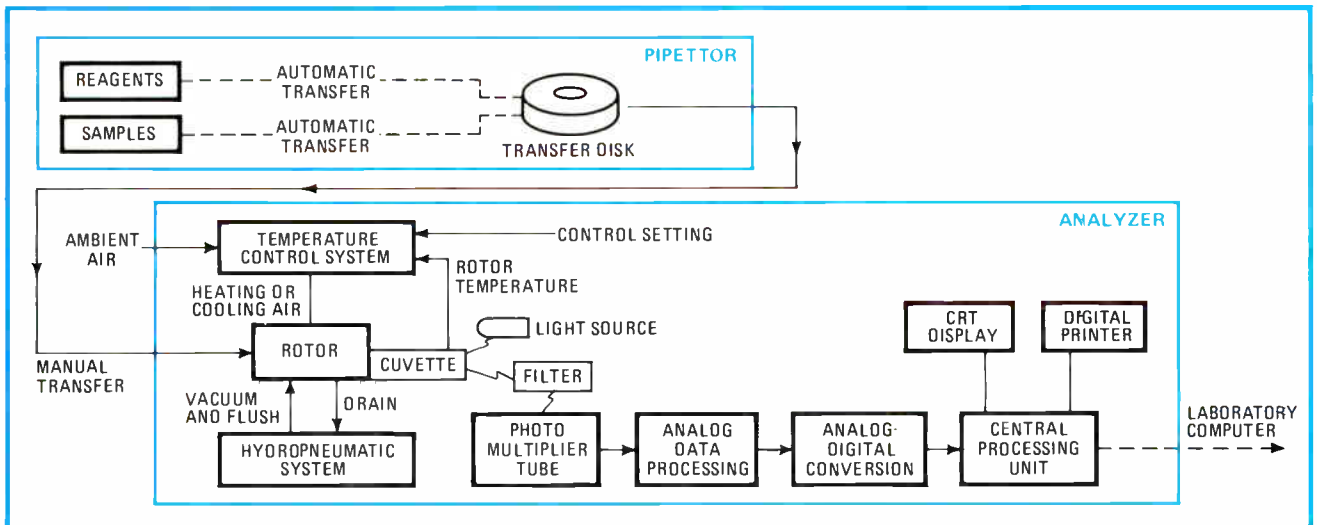
rol, motor-speed control, and the microcomputer.

The microcomputer must read test parameters entered through the front panel, process data, print the results, and recognize special instructions after printout. The special instructions may be to read the contents of the data that has been gathered and stored in memory, update data on command, recalculate and print, or restart the test without slowing the rotor.

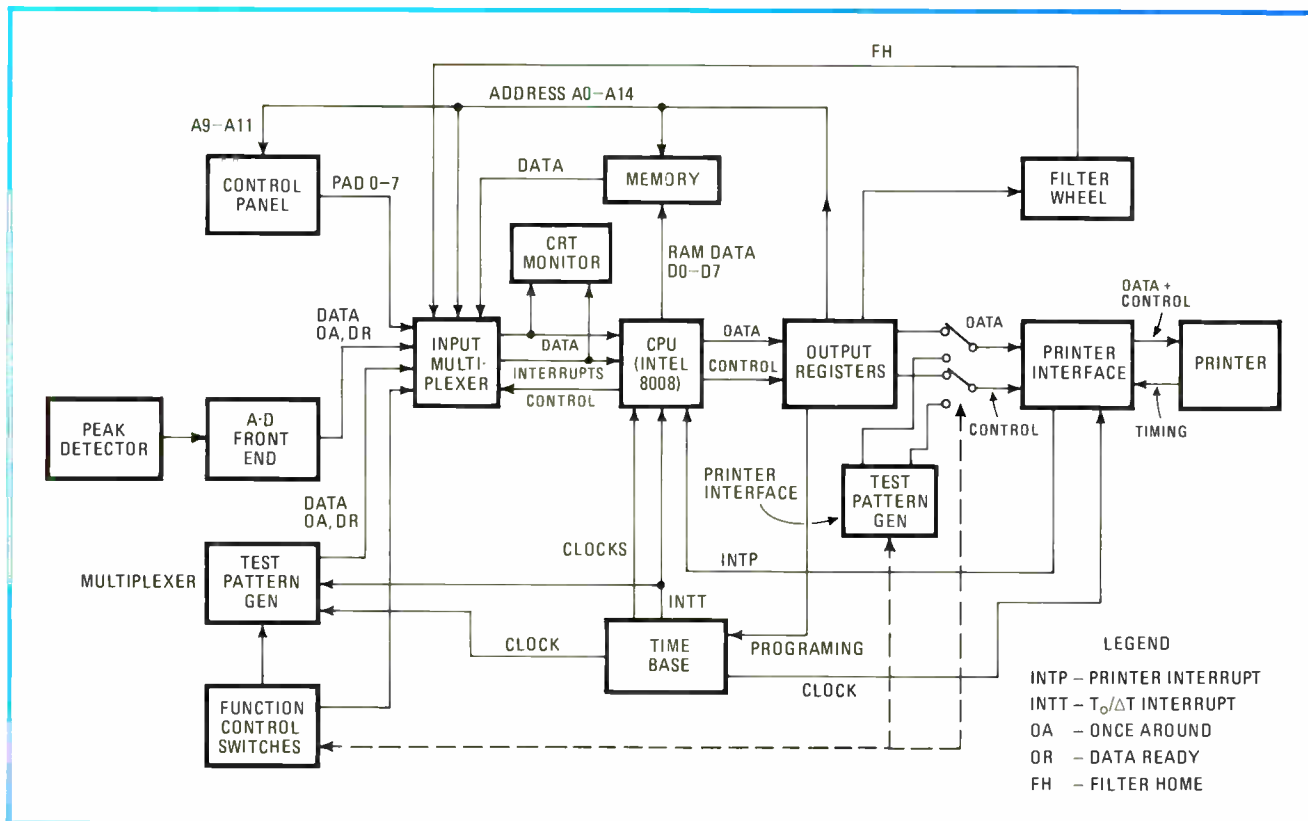
Optical clocking identifies samples

To associate each value of light transmission or absorption with the correct sample, an optical clocking signal is derived from the disk mounted on the rotor shaft. This light pulse and the photocell produce a peak detector-reset signal and a convert-command pulse that drive a 12-bit analog-to-digital converter.

The converter busy signal and a zero-reference (once-around pulse) from the rotor generate interrupts to the microprocessor to indicate when new data is available. By counting interrupts, the processor can synchronize



2. **Centrifugal spectrophotometer.** Centrifichem has 30 cuvettes around rotor so that 30 blood samples can be tested with reagents in parallel. The microprocessor that controls the operation is programmed with all the parameters to conduct any of 18 different tests.



3. Well designed. The 8008 CPU receives data via a multiplexer. Maskable interrupts facilitate gathering high-speed data from the rotor and detecting errors. The data is read for eight consecutive revolutions of the rotor and averaged to improve noise correlation.

the receive data with each test sample. To minimize errors resulting from noise, data is measured during each of eight consecutive revolutions of the rotor, and the values are averaged.

Two types of chemical tests are performed by the instrument. One type determines the difference in absorbance values at initial time T_0 and final time ($T_0 + N\delta T$), where N is the number of measurements and δT is the time interval between measurements. Other tests, which determine kinetic or enzyme reactions in the sample, require the calculation of the reaction rates. In addition, the results sometimes require normalization or conversion. The variables required for these functions are T_0 , δT , filter position (band-pass selected to match the absorbance wavelength of the reaction), selection of rate or terminal for the type of reaction being measured, and units of concentration or absorbance.

These parameters may be supplied to the machine through a series of thumb-wheel switches or automatically assigned by the memory upon entry of a standard test code. In Fig. 1 the rotor position is on the left and the control panel is on the right.

Figure 3 shows how maskable interrupts are organized to collect data from the rotor in real time and detect errors that may be encountered in gathering the data. For example, when it is time to gather the absorbance data, the central processor arms the once-around interrupt in order to find the first cuvette in the array of samples.

When the interrupt is received, the interrupt-service routine initializes a counter and arms both the data-

ready and once-around interrupts. Each time a data-ready interrupt is received, data is read and stored, the counter is incremented, and interrupts are re-enabled.

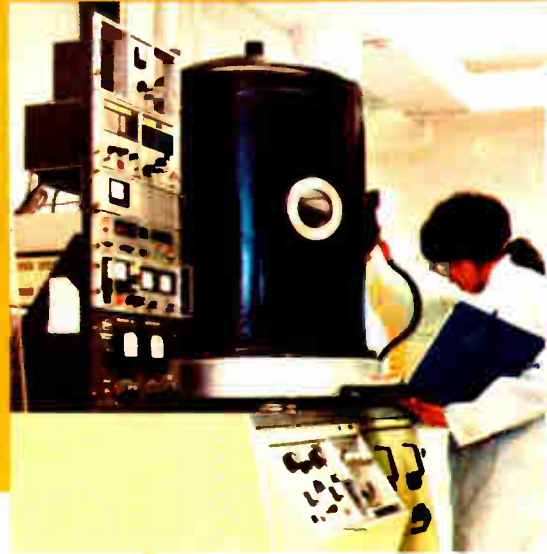
Upon receipt of the next once-around interrupt, the counter is checked to ensure that all 30 data readings were taken. If not, the set of readings is discarded and the sequence is repeated to avoid error. When data collection is finished, the once-around and data-ready interrupts are disabled until the time comes to once again read data.

External counters call time outs

Time outs for the T_0 and ΔT intervals are handled by external counters, programable by the central processor, that interrupt the CPU upon expiration of the preset time interval. This timer interrupt is also maskable so that time outs can be ignored when necessary upon completion of a run. Rearming the printer and the push-button signals to print out results are also handled as maskable interrupts.

Two interrupts in the system cannot be disabled. These are the logic-reset function, which allows a test to be started over without slowing down the rotor, and the spin-off interrupt, which tells the CPU that processing for a run has been stopped. Input data is multiplexed, and because more than eight input ports are needed, an output channel is used to enable one of two banks of input channels. Any subsequent input instructions receive data from the selected channel of the enabled bank.

For software, the high-level PL/M language, enhanced with certain subroutines in assembly language,



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is used instead of assembly language to shorten the programming time required and because it is easier for the average engineer to understand than assembly language. However, PL/M has its drawbacks. Its inefficient use of memory is probably the worst. By experimenting with syntax, the memory capacity needed for programming was reduced from about 7.5 kilobytes to less than 6 kilobytes. However, use of assembly language could easily have reduced it to 4 to 5 kilobytes.

In addition, it was impossible to write in PL/M the interrupt handlers that gather the real-time absorbance data because the code could not execute quickly enough

to handle the data rates involved. Therefore, assembly-language subroutines were interfaced to the main body of the PL/M code. And to increase efficiency, several specialized mathematics routines for multiprecision arithmetic were also written in assembly language, which is not difficult to interface with PL/M.

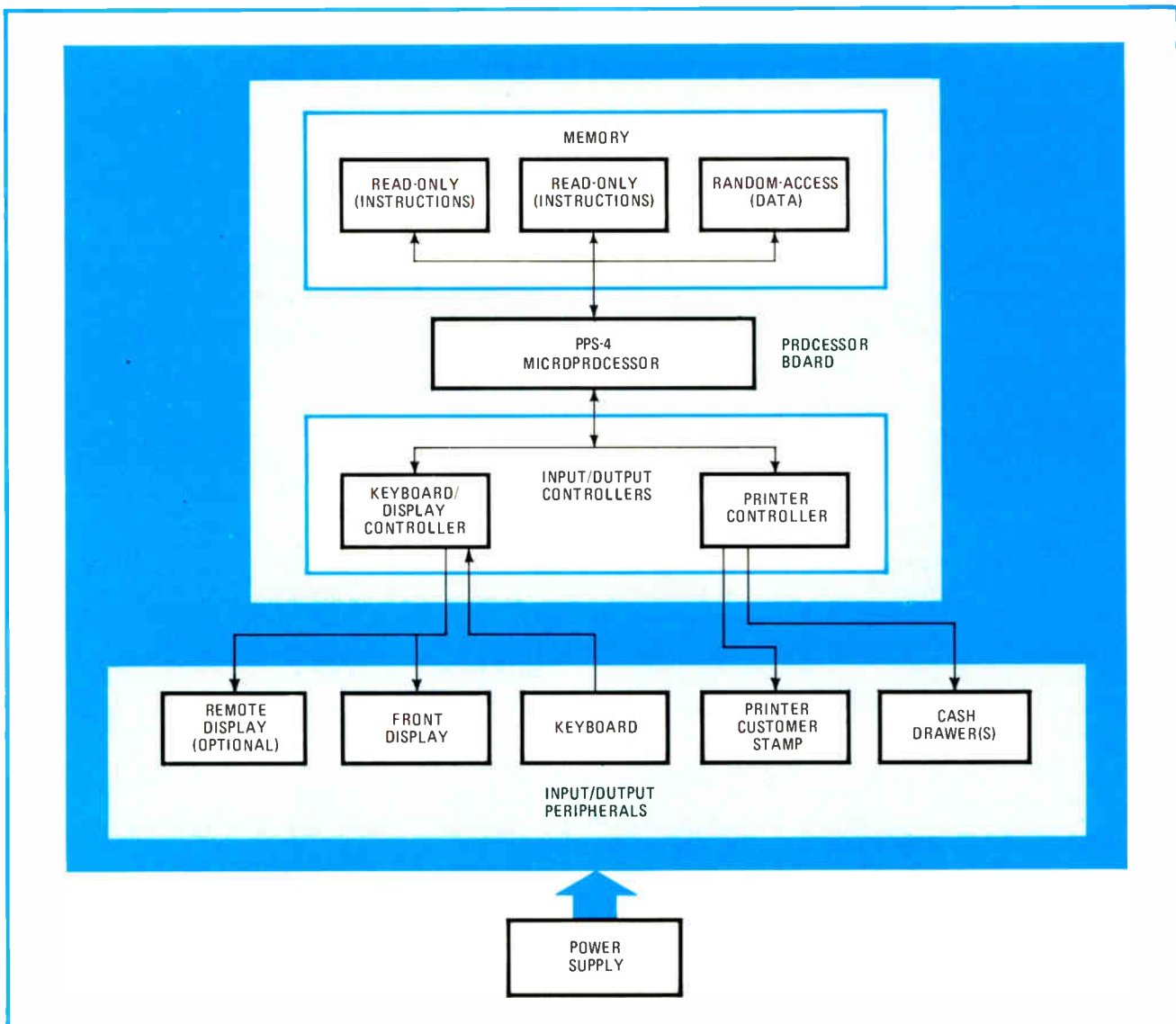
To facilitate fault isolation at the system level, a panel of light-emitting diodes was built into the microcomputer module to indicate the status of the bus and data inputs. Pattern programs compare actual operation with desired results, and other routines check the programmable read-only memory.

Four-bit chip set cuts cash register's cost and size

by Ed Sonn

Data Terminal Systems, Maynard, Mass.

Only by offering to do more for about the same price can an electronic cash register compete with the highly efficient electromechanical cash register found in small and medium-sized retail stores. To stake a claim in the market, Data Terminal Systems in 1971 brought out the successful DaCap 44, a stand-alone programmable elec-



Inside the register. The processor board in Data Terminal Systems' series 300 electronic cash register holds the six microprocessor chips. It handles information to and from the memories and the input (keyboard) and output (display and printer) portions of the machine.

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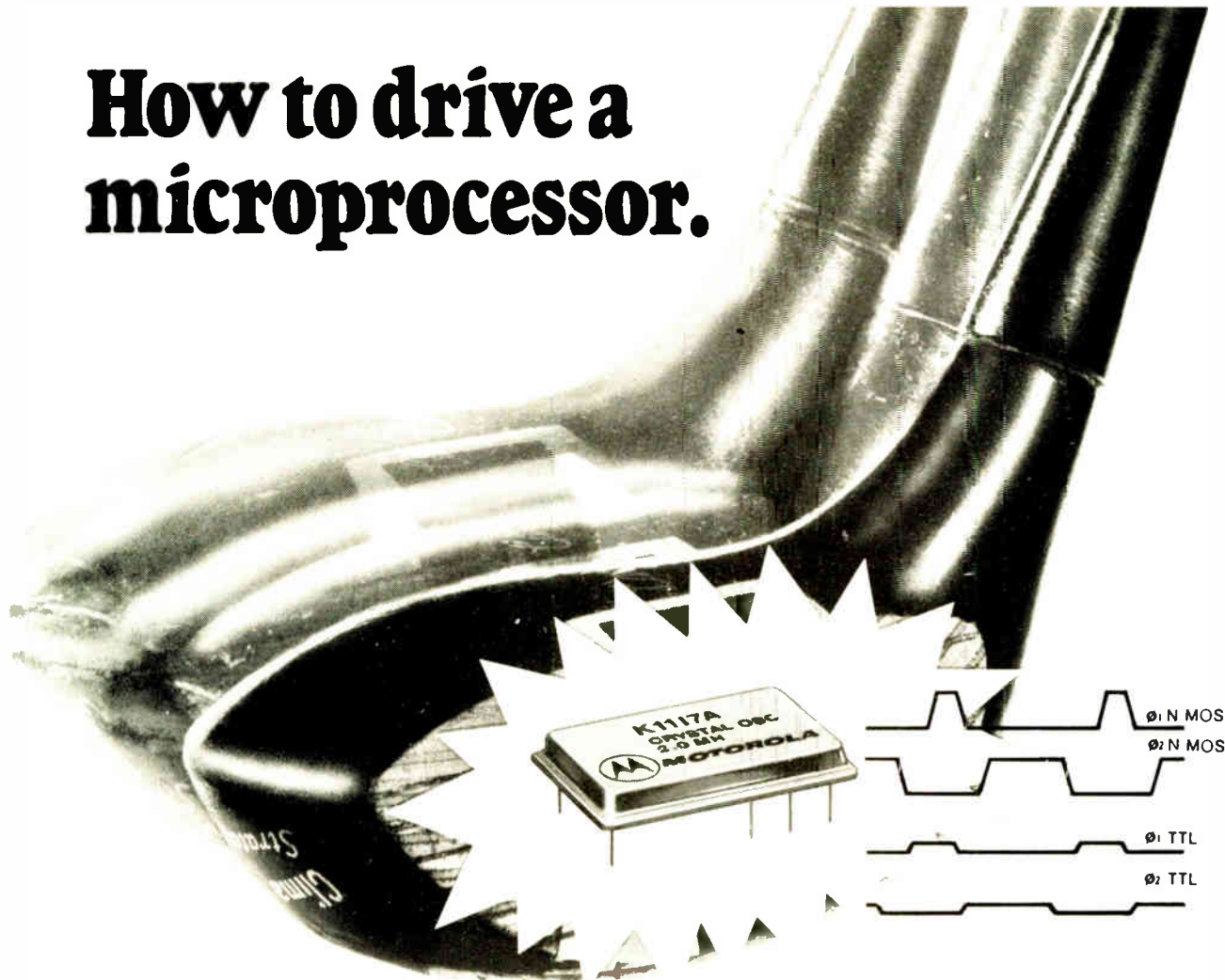
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tronic register costing \$3,000. To compete in the broader, lower-priced market the company began developing a new model in 1973, the series 300, to be priced around \$1,500.

The series 300 had to meet four important design considerations. It had to have fewer electronic components than the DaCap 44. It had to be simple to take apart and repair. It had to be smaller than its predecessor yet still be capable of housing a battery pack inside the cash-register cabinet, instead of outside, as on the DaCap 44. The battery, needed as backup in case of a power failure, had to be able to provide one hour of operation and protecting the memory for 24 hours.

The selection of a microprocessor for the 300 can best be understood in light of the design of the DaCap 44. At the heart of the earlier system was a processor and memory board composed of an arithmetic/logic unit, eight random-access memories, and six read-only memories, plus some small- and medium-scale transistor-transistor-logic chips. In addition, this processor board contained power regulators, a clock, drive logic for the printer, and drivers for the cash-drawer solenoids, numeric display, and keyboard. A second board—the keyboard card—consisted of reed-switch type keys and the keyboard matrix scanning logic. A third card, a numeric display consisting of light-emitting-diode read-outs and latch/driver circuits, was also required.

Deciding factors

The microprocessors available at the time included the Intel MCS-4004 and the Rockwell PPS 4. Neither was perfect for the application—the PPS 4, for instance, lacked an interrupt scheme. Compensating for this lack, however, the PPS 4 has two peripheral controllers, and these, plus its price, tipped the balance in its favor.

One of the two controller chips handles the keyboard and display, and the other handles the printer. The printer controller performs all real-time control functions required to operate a Seiko type 101 or 102 drum printer. The general-purpose keyboard/display controller, however, eliminates all real-time processing associated with keyboard and display. It scans a 64-key array with two-key rollover logic and places the detected keystrokes in a nine-position first-in/first-out memory for processing. It can also refresh either an 8- or a 16-digit display.

The PPS 4 microcomputer set economizes drastically on space. A single printed-circuit card, about 60% the

size of the DaCap 44 processor board, includes: the CPU, RAM, and ROM; the printer and display controller chips complete with drivers; the keyboard scanning logic; a dc-to-dc converter, and the display itself.

This new design has no need for a separate display board or for active components on the keyboard card. On the other hand, it does add a bus board, designed to link the microprocessor bus to the outside world. The bus board permits the user to enlarge the system by adding optional cards for functions such as automatic change dispensing, communications, and automatic weighing of purchases.

Aside from the packaging and circuit cost reproductions that it makes possible, the LSI microprocessor set also cuts packaging and power supply costs dramatically. Because it needs much less power, the number of batteries falls from three to one, which can easily be mounted within the cash-register chassis rather than in a separate power pack.

Although the final product has proved to be reliable, easy to manufacture and service, and less expensive than its predecessor, the use of an LSI MOS design instead of SSI or MSI TTL at that time suffered from some drawbacks. First of all, interfacing to the PPS-4 for purposes of expanding the system required special interface chips supplied by the manufacturer. In the case of the low-price electronic cash register, these chips were more expensive than the device to be interfaced.

Secondly, the microprocessor at that stage of its development reduced the design flexibility of attempts to modify the capabilities of the system. If a logic designer has access to data buses, registers, and strobes, he can usually satisfy custom requirements by adding a small amount of logic. Access to these elements in an LSI system is, of course, not possible.

Finally, the instruction sets of off-the-shelf microprocessors were general-purpose and inefficient for a particular application. While the designer of a SSI/MSI processor can tailor the instruction set and system architecture to an application, the design of a custom LSI microprocessor is prohibitively expensive for this relatively low-volume type of application. As memory and microprocessor costs decrease, however, inefficiency in the use of memory becomes less of a factor. In cash registers, speed is usually not a problem. Moreover, since the design of the series 300, advances in microprocessor technology and economics have made these devices increasingly flexible and easy to use.

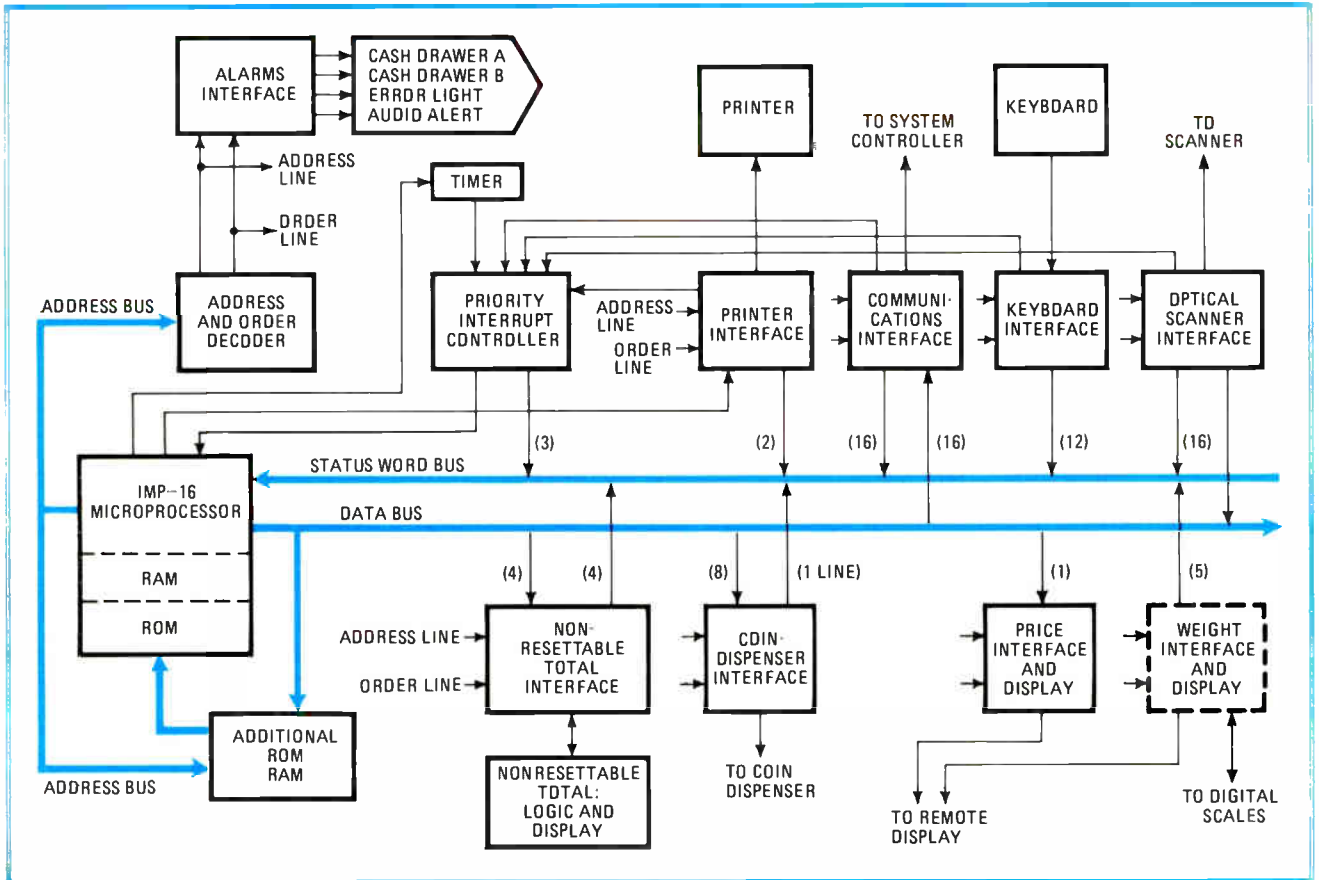
Checkout terminal takes on many supermarket tasks

by Milton Schwartz
National Semiconductor Corp., Santa Clara, Calif.

Supermarkets, more than most other stores, need highly adaptable point-of-sale terminals. Equipment requirements vary—a small store may require just the electronic equivalent of a cash register, and a chain may require multiple interlinked units, each with electronic

scales, highly annotated printouts, remote readouts, and laser-based universal-product-code scanners. Computational and reporting requirements vary—chains differ in the way they handle food stamps, checks, cash, discount coupons, and even bottle deposits. Taxes and taxable items vary from state to state and town to town. Finally, the terminals must supply management data that meets the needs of the individual chain.

To enable its Datachecker T2500/T3000 terminals to handle all these requirements, National Semiconductor uses an IMP-16 microcomputer in them. On the basic IMP-16 card is a 5-chip central processing unit (one



1. Does everything but bag. Block diagram of microprocessor-controlled supermarket checkout terminal shows how printer, keyboard, weighing scale, and various peripherals are tied to the IMP-16 central processor by buses. The address-and-order-decoder decodes 3-bit order codes and 5-bit address codes onto just one address line and one order line that go to all the peripherals.

NSC 3.000			
DATE	01 01	0.013	TIME
REGISTER NUMBER	REG 1	200	CLOCK NUMBER
STORE NUMBER	ST 021.7		
FOOD STAMP ELIGIBLE	S	1.89 GR	GROCERY
	S	2.45 MT	MEAT
	S	1.45 GR Tx	GROCERY, TAXABLE
	S	3.89 PR	PRODUCE
	S	1.47 G-M Tx	GENERAL MERCHANDISE, TAXABLE
	S	2.13 LB	WEIGHT
118 FOR 49 CENTS	S 1/ 0.49	1.04 PR	
	S	.89 PR Tx	PRODUCE, TAXABLE
31 OR 89 CENTS	S 3/ 0.89	.89 GR	
	S	.42 OR	DAIRY
	S	.42 OR V	DAIRY, VOID
	S	.42 DEL	DEL CATESSEN
PRICE LOOKUP NUMBER	1	1.00 GR	
PLU NUMBER/QUANTITY	1 5	5.00 GR	
	4	2.16 LB	
	S 1/ 0.49	1.06 PR	
PLU NUMBER	100	.26 GR	
QUANTITY	3	21.98 TTL	TOTAL
STORE COUPON	201	.30 CP CR	COUPON CREDIT
		.15 NCP CR	STORE COUPON CREDIT
		21.53 TTL	TOTAL
		12.59 TTF	TOTAL ELIGIBLE FOR FOOD STAMPS
		8.94 MTL	MONEY TOTAL
		10.00 T-F	TOTAL FOOD STAMPS TENDERED
		3.00 N-C	MISCELLANEOUS NON-CASH
		5.00 CKT	CHECK TENDERED
		10.00 C-T	CASH TENDERED
		21.26 ITL	INTERMEDIATE TOTAL
		.27 TTX	TAX
		21.53 TTL	TOTAL
		28.00 TND	TOTAL AMOUNT TENDERED
CUSTOMER COUNT	3 CST	6.47 CHG	CHANGE
		.06 CHF	CHANGE FROM FOOD STAMPS
ACKNOWLEDGEMENT		THANK YOU	

2. The summing up. Register slip from intelligent checkout terminal provides breakdown of both cash and non-cash transactions.

control read-only memory plus four register and arithmetic/logic chips), 256 16-bit words of random-access memory and 512 16-bit words of ROM, plus a clock generator, flag circuitry, interrupt timing, jump condition inputs, and data buses. Other cards add 1,000 16-bit words of RAM and 6,000 16-bit words of ROM and hold input/output buffer circuitry for driving the interfaces on the word and data buses.

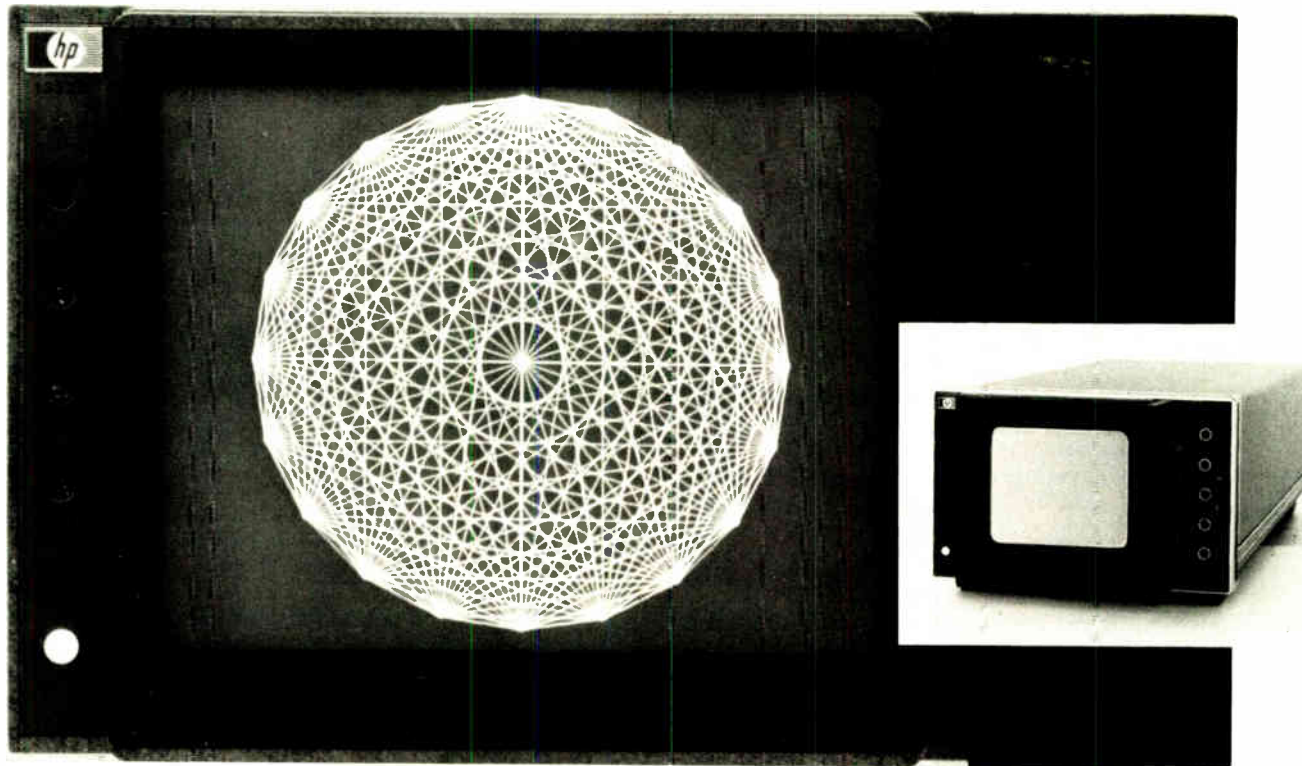
Linked to the IMP-16 by two buses are up to nine interface circuits. These connect the microcomputer to the keyboard, printer, an outside controller, as well as to various peripherals.

The keyboard has a 10-key numeric pad, up to 10 keys for store departments (such as dairy, produce, etc.), 10 function keys, and a scale-interface key. It is very like the keyboard on the cash register familiar to supermarket checkers.

The printer is an 18-column drum-type model that produces the sales slip.

The communications interface links the terminal either to other terminals or to a dual-processor controller. A supermarket may first install the terminals as stand-alone units, then may connect 16 of them through a polling interface for broader accounting and management-information record keeping. Later, up to 23 terminals may interact with a dual-processor controller for an in-store centralized system. Finally, binary-synchronous interface controllers, compatible with most protocols,

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addition to medical and instrumentation systems.

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SYSTEK MICROPROCESSOR & MICROPROCESSOR-BASED SYSTEM

FUNCTION MODULES (SAM²-SYSTEM)

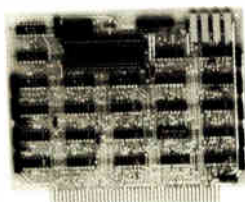
- PROCESSOR
 - Processor-8 (P)
 - Processor-8/1 (M/P)
 - Processor-8/1H (M/P)
- MEMORY
 - SAM²-ROM [1KB (M)
2KB (P)]
 - SAM²-ROM(1KB)/RAM(1KB) (P)
 - SAM²-ROM(1KB)/RAM(4KB) (P)
 - SAM²-RAM [1KB (P)
2KB (P)]
 - SAM²-RAM 8KB M²-RAM (P)
 - SAM²-RAM 256B (M)
- INTERFACE
 - SAM²-PIC/1
 - SAM²-TTY(for ASR-33)
 - SAM²-PTR
 - SAM²-SIF
 - SAM²-BA
 - SAM²-INP
 - SAMAC-8/1 CSL [(M)
(P)]
 - CMT/Control
 - DISPLAY/Control
 - KEYBOARD/Control
 - SAMAC-8 Standard I/O
(fr ASR, PTR, CSL)

MICROCOMPUTER SYSTEM

- SAMAC-8
- SAMAC-8/1
- SAMAC-8/1H

MICROPROCESSOR-BASED SYSTEM

- SAMAC-9000S For Scientific Areas Programmable Calculator System
- SAMAC-EC/X for Small Data Processing Electronic Management Machines
- SAMAC-SC/X for Industrial Automation Sequence Controller
- SAMAC-WP/F for Word Processing and electronic typewriters -WP/M
- SAMAC-POS/X for Point-of-sale and electronic cash registers
- M-200 for Billing Machine
- NCT-9000 for Photo Typesetting Machine



SAM²-MODULE



SAMAC-8/1H

NOTES: (M) ... Module
(P) ... PCB

SAMAC WP200 WORD PROCESSOR

The SYSTEK SAMAC WP200 is a computer based Text Editing System. It basically consists of those, LSI Micro-computer with semi-conductor memory, ROM and RAM, dual magnetic cassette tape transports, and the input/output typewriter. The SAMAC WP200 is designed to have many kinds of automatic features which are necessary for the text writing and editing work.

And also designed to have the expandable capability by easily equipping with the peripheral device, such as CRT display, high speed printer, paper tape unit and communication control device.

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Electronics/April 15, 1976

SAMAC 9000S PROGRAMMABLE CALCULATOR

SAMAC 9000S is a sophisticated programmable table-top calculator of revolutionary design suitable for a wide range of applications in science and technology.

In contrast to the ordinary computer, SAMAC 9000S requires no specific language, allowing any person to write programs and operate easily with a minimum of training. As an alternative, manual calculation is possible.

The calculator has outstanding memory capacity in its class: 2,000 program steps and 200 words of data storage in the basic configuration, and 10,000 steps and 1,000 words if additional memory is installed. Since a number of special function capabilities necessary for scientific and technical calculation are incorporated, SAMAC 9000S can fulfil the most sophisticated task. Not only are display tubes and a digital printer provided in the standard configuration but also a cassette magnetic tape unit is included.

160 Circle 160 on reader service card

may be added to link up with a remote computer.

The various peripherals attachable to the terminal include a display, electronic scales, an optical universal-product-code scanner, coin dispensers, and a nonresettable-total counter, which records the terminal's gross dollar activity. Figure 1 indicates the requirements for each peripheral.

In addition, to avoid distributing all address lines to each peripheral, the system uses a centralized address and order decoder. With its 1-of-32 and 1-of-8 decoding circuits, only two lines need go to each peripheral.

These two address and order lines also go to the alarms interface, to signal the opening of a cash drawer, and to alert the cashier to his errors. For example, if a cashier inadvertently rings a sum above a predetermined limit (say \$100 instead of \$1), the IMP-16 sends single-bit codes through the address lines to light lamps and ring bells.

Interrupts in abundance

The system is basically interrupt-driven. All interfaces capable of generating an interrupt—the printer, keyboard, scanner, and communications interfaces—are linked to a controller, which establishes the priority and passes the interrupt to the IMP-16. The processor polls peripherals to ascertain their status and initiates the proper interrupt routine once it recognizes a peripheral.

When an interrupt occurs, a last-in/first-out stack saves the subroutine and interrupt return address. Use of a pull command simplifies the extraction of priority subroutines from several levels of nested operation. A system timer produces interrupts at regular intervals. If these interrupts are not acknowledged, the timer automatically re-initiates the system, preventing looping.

The IMP-16 has a basic 43-command instruction set, augmented by a 17-command extended set in system programming. Its Fortran cross assembler runs on an IBM 360. The programmer, having written an assembly program that fits a specific retailer's requirements, can keypunch it or enter it through a terminal and then can call it up on the terminal for editing and debugging.

Supermarkets that use such custom-tailored point-of-sale terminals run more efficiently. For instance, they give the clerks better control over cash and noncash transactions—discount coupons, bottle deposits, cash refunds, credits, and checks are handled automatically and documented fully in the register slip shown in Fig. 2. Included among the subtotals is the amount computed and displayed by the IMP-16 microprocessor as payable by food stamps.

Automatic tax calculation, based on a tax table or on a fixed rate programmed into memory, insures more accurate tallies of total purchases. Depending on state and local tax requirements, some food items are not taxable. These exceptions are programmed by the store manager into the terminals.

Checkout is speeded up by having tables of commonly purchased items and their prices stored in memory. Then the clerk need enter only code numbers, instead of slowly punching in each item's department and price data. The manager can add and delete products, or he can code the price per pound of produce and meat so that an electronic scale displays total price.

In addition, the store manager gains better control of his operation because he has complete figures for gross sales, taxable sales collected, total refunds, amount and number of coupons, food stamp volume, department totals, and many other specific items.

More complex video games keep player interest high

by T. George Blahuta
Midway Manufacturing Co., Franklin Park, Ill.

The microprocessor, busy bee of the electronics world, is now engaging in fun and games as well as drudgery. Although the earliest video games in arcades were built with transistor-transistor logic, they were so simple they could soon become boring to many players. And the manufacturers, lacking the capability to design their own TTL logic, had to buy the designs and sometimes even the logic packages as well.

Designing games around the microprocessor has increased their complexity by two to five times, and allows the manufacturer to design his programs right in his own shop. What's more, changing to the microprocessor has cut development time by 75%.

Of course, the transition from TTL was not accomplished without difficulties. In the first place, the data rate required for the faster scan to keep the image on the video screen is far beyond the capabilities of microprocessors. And, although this problem was solved with a random-access memory, the technicians were at first

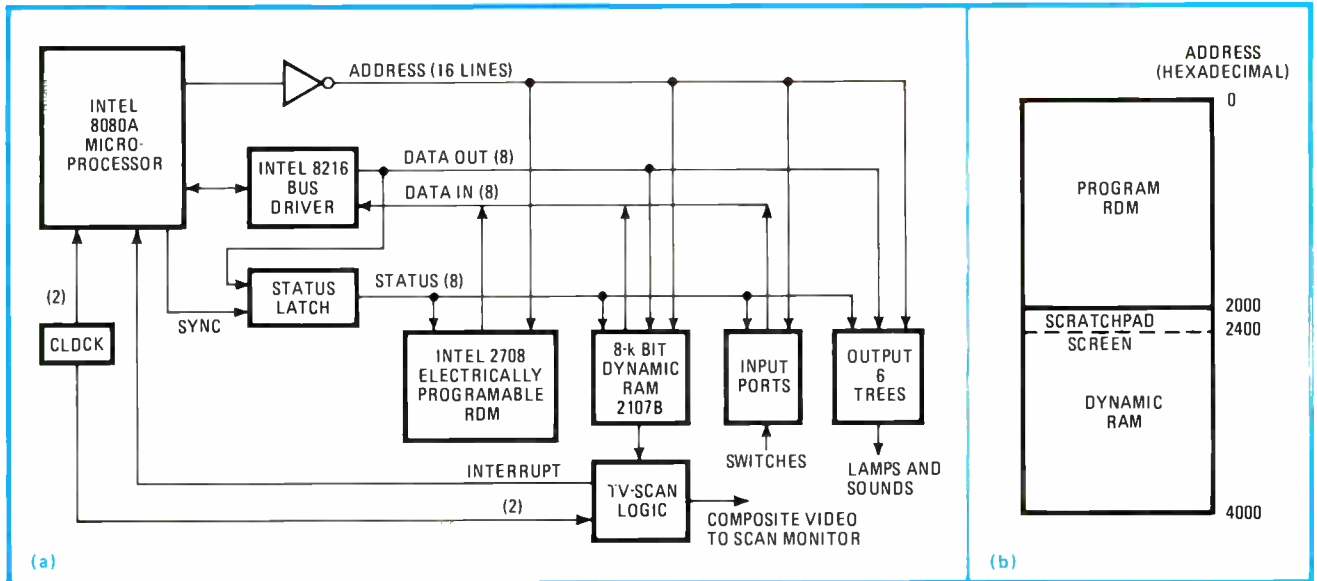
frightened by the microprocessor and did not fully understand the waveforms involved in its operation.

Training quickly increased the proficiency of the technicians, and a read-only memory was programmed to isolate problems they had with RAMs. With this help and their increasing expertise, the technicians could repair twice as many defective boards as before, and ironically, the high repair rate created a serious parts shortage as suppliers struggled to keep with demand.

The microprocessor was adapted for use with the video display by storing the picture information in a large RAM, and reading it out on to the screen one bit at a time, while conventional horizontal and vertical deflection circuits generate the raster just as in any home TV set. The pattern on the screen is 224 horizontal lines, each line consisting of 256 dots. The RAM therefore must hold the 224×256 bits of information that determine whether the individual dots are bright or dark.

In this arrangement, the microprocessor is not used for scanning the picture, but merely changes the contents of the RAM at a slow rate—once every frame or even every few frames. The only interaction between the microprocessor and the screen-scanning logic is an interrupt signal at the bottom of the screen that the microprocessor uses for synchronization and timing.

Midway chose the Intel 8080A microprocessor, 16 In-



1. Game circuit. Because microprocessor is too slow to generate raster scan for arcade video game, image is plucked from RAM and impressed on screen during conventional raster scan (a). Microprocessor responds to inputs from switches controlled by players, forms new images according to program stored in electrically alterable ROM. Memory map (b) shows ROM and RAM for typical game.

tel 2107 dynamic RAMs and an Intel 2708 electrically programmable read-only memory (Fig. 1). Intel's MDS 800 hardware/software development system [*Electronics*, May 29, 1975, p. 95] was modified to develop and debug programs. The Intel system was chosen for speed, register capacity, availability of parts, and support in developing games and programming.

RAM configured for screen pattern

The RAM contains 57 kilobits to correspond to the screen pattern of 224 by 256 dots. The raster reads out the memory in 1/30 second. The microprocessor uses 1 kilobyte by 8 bits of the RAM as a scratchpad without any significant loss of vertical resolution. Conventional input/output ports are handled by the microprocessor as on/off switches.

A series of games has been written in 3 to 5 kilobytes of instructions (Fig. 2). A good portion of each game consists of patterns. A typical game requires 8 kilobits of read-only memory for the program. An equivalent hard-wired circuit could require 150 TTL packages. The microprocessor writes the image on the screen by moving the two-dimensional pattern changes from the programmable ROM to the RAM a byte at a time.

Each byte move shifts the pattern incrementally to simulate motion. The interrupt limits the number of operations within the interrupt routine. Since the interrupt generates the synchronous signals, it provides timing information to the main program. Its accurate clock times an output switch that must be kept open for a certain length of time. Finally, the interrupt checks the state of input ports and flags changes to the memory.

A game program is designed in two parts: the main game-logic pattern and the interrupt. The main program sets an action in motion and checks for its completion. The interrupt moves the pattern and informs the main program an expected condition is met. For example, a pattern might be a car at point A with velocity

B traveling in one direction until condition C is met.

The interrupt veers the pattern from point A at velocity B and informs the program when condition C is met. The main program then initiates the next operation, part of which may be sound or light output. The interrupt operates from the blanking pulse when the scan reaches the bottom of the video screen.

The MDS 800 for developing and debugging programs has been expanded by replacing its teletypewriter with a floppy disk, a powerful operating system, a high-speed printer, and a cathode-ray-tube terminal. The floppy disk and printer handle the vital editing and assembly function at 10 times the speed of the unmodified system. The initial debugging is checked on the MDS monitor as the new program is run from the MDS memory, and final debugging is conducted with an in-circuit emulator on an erasable programmable read-only memory that is repeatedly blasted by pulses from a programmable-ROM programmer on the actual game board.

2. Quick on the draw. Basic microprocessor circuit is used for a variety of games by changing instructions stored in read-only memory.



Distributed control boosts process reliability

by Anthony M. Demark

Honeywell Process Control Division, Fort Washington, Pa.

When a control failure can produce catastrophic effects, as in the chemical or petroleum processing industries, the concern for reliability dominates design decisions. So, in recent years, the process industries have been moving toward distributed control because of its increased reliability. Failure in one part of a distributed system need not shut down the entire process, since each part operates independently.

Microprocessors are fairly new on the distributed-control scene, but they fit well on the bottom rung of a hierarchy of controls. One example is the TDC 2000 controller file that is built around General Instrument's CPI600 microprocessor.

The file has the conversion and computational circuitry for controlling eight process loops. It has 28 control algorithms stored in a read-only memory. And the operator can configure his control strategy with a remotely locatable pushbutton panel. He also can make his selections through cathode-ray-tube control stations, or directly through the minicomputer that is at the top of the control hierarchy.

The controller file in the figure is organized around a 16-bit bidirectional data bus that allows the CPI600 or the data-highway interface to gain access to information in any of the controller cards.

Generally the microprocessor controls the data bus and implements the control strategy stored in random-access memory by executing specific sections of the 120-kilobit ROM. These strategies always involve the encoding of the process inputs via the analog-to-digital converter, calculation of valve responses and conversion to analog form by eight independent digital-to-analog converters, and transmission of the responses to the process-control valves—basically eight loops of control.

The data entry panel is serviced via the interface card at the completion of the control calculations. Information too critical to remain in the volatile RAM, is periodically transferred into the core memory.

Using the coaxial data highway and highway interface card, a remote supervisory computer or central CRT display can gain access to information stored in the controller memory. The card requests control of the bus from the processor, addresses the location of interest, and conditions the data for transmission to the requesting device. It is this interface that truly implements the distributed-control architecture, since it permits communication among all elements of the control system.

The CPI600 and four companion circuits were developed for this application. All five custom circuits were designed using an n-channel ion-implant process.

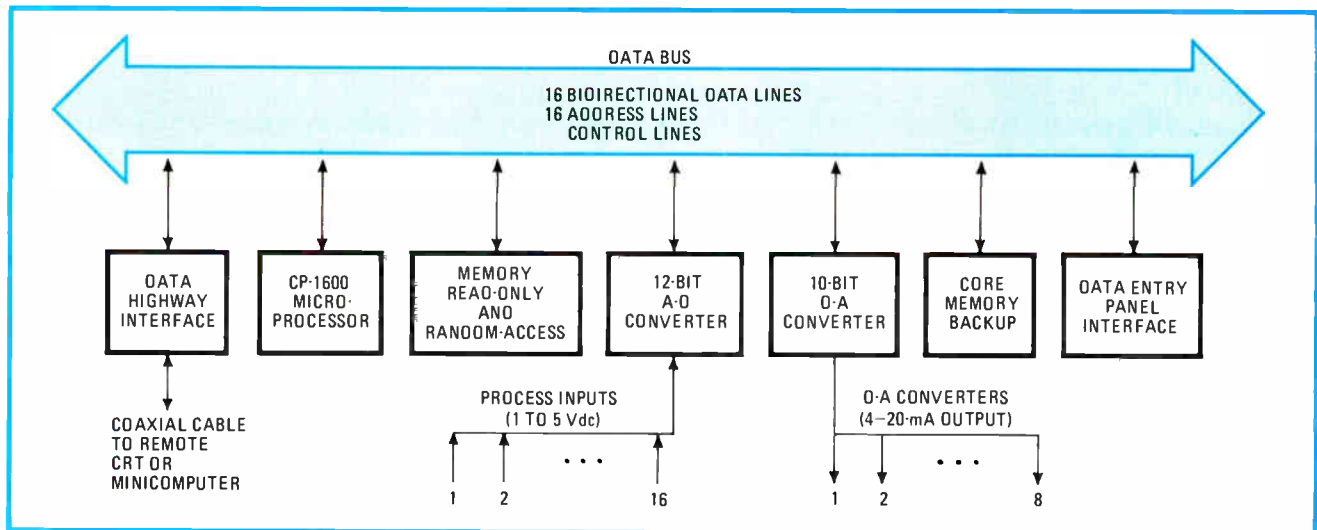
Large arithmetic content

The 16-bit architecture of the central processing unit resulted from the large arithmetic content of the control algorithms, often involving 48-bit products.

The other chips are a 256-word-by-4-bit RAM circuit built into a 512-by-16-bit memory array, 23 512-word-by-10-bit ROM circuits storing the controller's operating program, a 16-channel analog multiplexer that contains the address latches and switches needed to connect any of the 16-process inputs—1-5 volt dc signals representing temperature, pressure, and flow to the a-d converter, and a dual 10-bit pulse-width d-a converter that stores and converts calculated valve signals into analog form.

The design challenge was to get all the digital-control advantages of the microprocessor without violating the critical rules for safe, reliable process operation. The chief areas of concern were power supply, independent valve outputs, conventional displays, firmware operating aids, memory volatility and diagnostics.

The control system must operate from a single, loosely regulated dc source (22.5 to 30 volts), so it can use rugged, reliable ferro-resonant power supplies for the process transmitters, valves, and control equipment. Also, this type of supply can be paralleled for redun-



Tying into the system. The TDC 2000 components connect to the 16-bit bidirectional databus for communication among controller components and also to permit the controller to talk with other peripherals or with a hierarchical computer, if there is one.

dant operation, a highly important reliability feature in a plant that can't tolerate instrument power loss.

The various logic and control circuits require 14 amperes at 5 volts dc, and modest amounts of ± 12 -v dc power. The 12 v supplies were handled by two integrated-circuit regulators, and a simple inverter (+24 to -24 v). But the only technique that promised efficient 5 v dc from 24 v dc was a switching regulator, which was used in spite of its reputation for generating electrical interference. The end result was a 70%-efficient supply isolated from noise by four-terminal electrolytic capacitors and shielding.

Experience shows that users can tolerate loss of automatic control for eight loops, but assuming handwheel control for eight valves would place great strain on the plant operating staff. An independent storage register and a d-a converter for each valve output virtually eliminates the possibility of simultaneous failure of more than one output.

A custom circuit contains a 10-bit register that stores the digital equivalent of the valve signal. This register is available for parallel loading by the microprocessor and for increment/decrement manual intervention by a process operator. This chip also contains a pulse-width d-a converter that converts the digital value into a 4-to-20-milliampere dc signal. The circuits that provide manual control operate from a single 24 v dc supply and can

function without the remaining controller circuitry.

Process control operators sometimes prefer conventional analog displays. The significant amount of interfacing that this option entailed was feasible only when integrated into the valve-storage-and-conversion chip described above. The hardware features of the d/a converter chip and firmware initialization routines greatly simplify operating rules, thereby reducing the probability of the operator inadvertently disturbing the process.

The convenience, access time and costs of solid-state memory are hard to beat. However, it is volatile. Battery backup schemes are all limited by life, capacity, maintenance, or shipping considerations. The cost and power consumption of a parallel core was also excessive. So a hierarchical concept using the 4,096-by-1-bit core memory was used. Variable data is stored in the volatile RAM memory, with all critical values serially transferred to core three times per second.

If the microprocessor, analog input system or analog output system fails any of the extensive, hardware and firmware diagnostic tests, the system prevents the processor from transferring calculated outputs to the valve d/a converters. This keeps potentially erroneous information from reaching the process and maintains the valve signals at a previously valid level. In addition, a "watch-dog" timer monitors the program execution time to eliminate any infinite loops.

Standard process controller can be programmed in field

by Bruce Allen

Bristol Division, American Chain and Cable Co., Waterbury, Conn.

Programming a microprocessor for a complex and refined process-control application can be wildly expensive when done on a large computer and very time-consuming if done on a simple microcomputer development system. A quick low-cost alternative—if the right kind of minicomputer is at hand—is to trick the minicomputer's macroassembler into producing the microprocessor's machine language instead of its own. That was how the operating codes for the UCS-3000 process controller were written.

Industries as diverse as the chemical, petrochemical, oil, gas, water treatment, food, steel, and paper are equally well served by the microprocessor-based UCS-3000. This process controller, which can function either in a network of controllers or independently, is a standard unit that does not need custom programming. Instead, engineers in the field, with no specific training in computer techniques, decide on the machine's initial configuration and may change that configuration later without shutting down the process.

As elements in a network, the units are cost-effective, and run unattended, each of them controlling a very small segment of a batch or continuous process. As a stand-alone device, a unit handles either complex process control or data acquisition and reduction and formats the output for printers, cathode-ray-tube display

terminals, floppy disks, and other peripherals.

The design revolves around 24 pseudo-hardware building blocks—basically programable calculators, Boolean logic blocks, counters, data storage units, etc. Several hundred blocks may be interconnected in each process controller through 1,000 possible software connections. To handle all this, an Intel 8080 microprocessor is augmented by a sophisticated multi-programmed operating system and a device-independent multi-buffered input/output software system. The 8080 also employs a modular process I/O interface, plus memory, communication I/O, and operator interfaces.

Meeting expectations

Demands on the 8080 are high. It must execute hundreds of logic equations as effectively as a programable controller and must solve generalized arithmetic equations faster than a programable calculator. It must time external events to a resolution of 4 milliseconds and control the on/off outputs to within 0.1 second. It has to measure process variables with 12 bits of resolution, and then control proportional devices based on calculations accurate to one part in 16 million, with a dynamic range of 10^{77} and with time constants up to several days or integration times of a month. Lastly, it must efficiently handle two-way asynchronous ASCII data communications on several devices simultaneously up to 9,600 baud, and it must handle full-duplex synchronous multi-drop transfers up to 250,000 baud.

The 8080 is therefore used to its fullest extent. There is a three-layered interrupt structure that produces 486 interrupts, and a complete direct-memory-access structure that allows each of 30 I/O boards to handle DMA

7.0 dB

Specification

INSERTION LOSS

6.0 dB

Typical

5.0 dB

Subminiature Attenuators

1.30

1.20

Specification

Typical

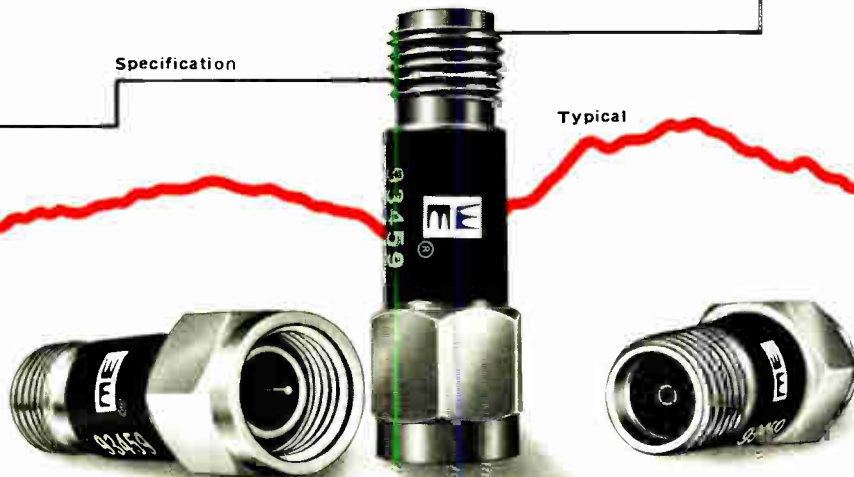
VSWR

1.10

1.00

1.0 GHz

18.0 GHz



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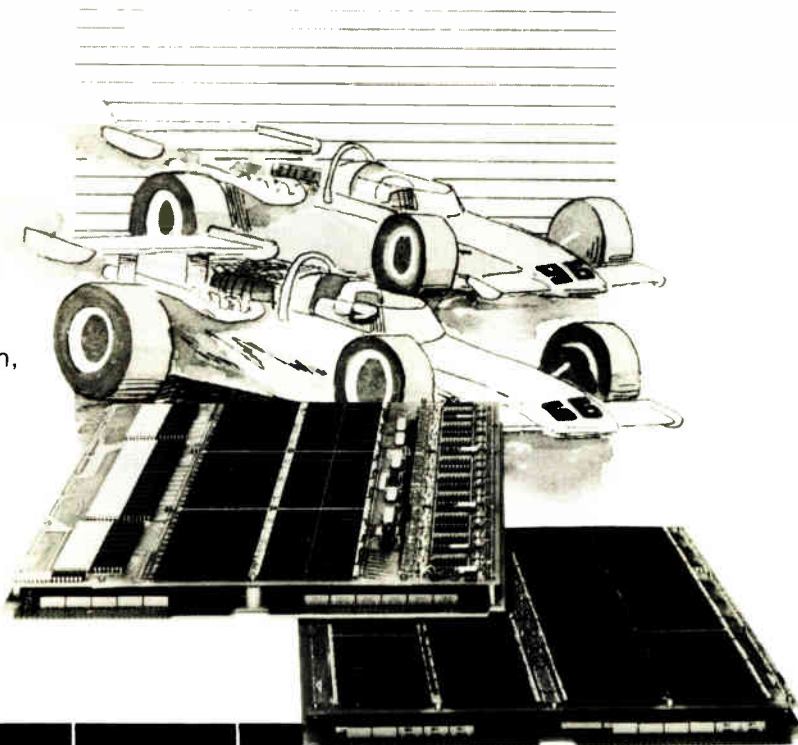


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MEMORY SIZE	16K	32K	16K	32K	16K	32K	16K	32K
CYCLE TIME	650	650	650	850	650		650	750
ACCESS TIME	250	250	270	300	280		265	300
PHYSICAL SIZE	11.75x15.4 x1.0	11.75x15.4 x1.0	11.75x15.4 x1.0	11.75x15.4 x1.0	11.75x15.4 x1.0		11.5x13.7 x1.0	11.5x13.7 x1.0
COMPATIBILITY 16K TO 32K	YES		NO		NO		NO	



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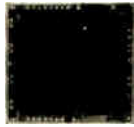
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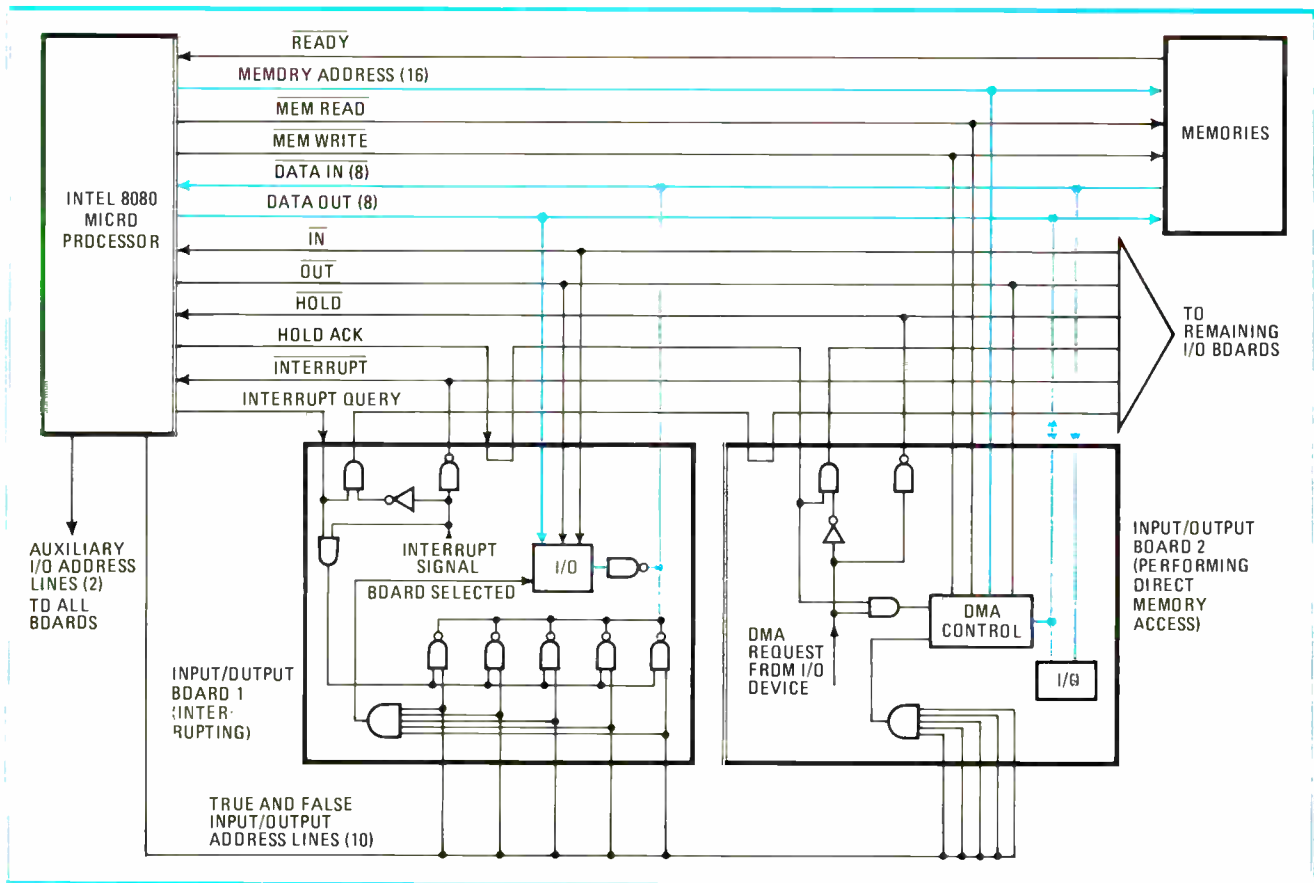
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Process control in action. Up to 30 identical I/O boards may be addressed through 10 lines, but each board is connected to only five. Board 1 is shown as performing interrupt, and board 2 is performing direct memory access. Only the active elements are depicted for each function. Interrupt and direct-memory-access queries are daisy-chained through each I/O board until intercepted by a requesting board.

transfers at full 8080 speed (see figure). Memory consists of 65,536 bytes implemented in core and in semiconductor, both random-access and programable read-only memory.

To simplify input and output, all devices communicate over an 8-bit output data bus and a separate negative-data input bus. In addition, the 8080 sends 12 address lines to the boards. Ten of them carry the 5-bit board addresses, a different assortment of five lines ending up on each board. When a board is selected, its five address lines are high. The other two address lines go to all the boards, for further device selection.

In the first level of the interrupt structure, there are six interrupts internal to the microprocessor and a single external one, which is shared by all 30 I/O boards.

To notify the 8080 that it has an interrupt to be serviced, a board simply pulls down the bus INTERRUPT line. The 8080 then sends out an INTERRUPT QUERY, which elicits its five-bit address from the nearest board with an interrupt pending. This address triggers a second-level interrupt that branches to one of 30 program starting points. Meanwhile the 8080's original query resets the interrupt on the now serviced board and allows other boards to generate additional first-level interrupts.

A third level of interrupts may be triggered by the 16 digital inputs on each I/O board. Each of these 16 points on a board may be selectively armed to generate an interrupt on change of state. When this happens, the

board pulls down the INTERRUPT line as before. However, the software must also determine which bit changed state and then transfer the information to the appropriate interrupt service program.

A direct-memory-access transfer may be initiated by any I/O board, by pulling down the common HOLD line and waiting for a HOLD ACK from the microprocessor. Then the board places its memory address on the 16-bit memory address and either puts data on the DATA OUT bus and issues a MEM WRITE, or issues a MEM READ and takes data from the DATA IN bus. Then the HOLD is released by the I/O board and the CPU resumes operation.

To program the 8080 for a complex continuous-process-control application, experience indicated that none of the Intel assemblers and simulators—let alone PL/M—would be particularly suitable. For one thing, they require a lot of expensive computer run time: the 8080 cross assembler, for instance, being written in the high-level language of Fortran, is a slow way to produce 8080 machine language. For another, they do not allow linking of subroutines, though that would be no problem in the case of a one-time processor development.

An alternative is to buy a microcomputer development system based on the microprocessor that will eventually be used. But again, for a job of any size, the process turns out to be slow, and the crude operating systems usually lack linking capability.

But a third, highly efficient, approach may be used by

anyone with a modern minicomputer disk operating system. This kind of minicomputer has a macro assembler for converting its own assembly language into its own machine language. But it can be tricked into using its assembler to convert 8080 assembly language into 8080 machine language by storing in it a library of macroinstructions that define the 8080 instruction set. This assembler can be run at least 10 times as fast as a Fortran-based cross assembler and will take only one fifth the mini's core space.

Also, the assembler's output is not absolute code, i.e. a specific address for each machine instruction. Instead it is link-ready code. In other words, the program can be divided into subroutines, and an entire subroutine or module can be addressed instead of just an absolute location in that subroutine. Eventually, the link editor (or cataloger) will link the modules together. In addition,

programs can use a reference name for a not-yet-written subroutine, for its insertion later during linking.

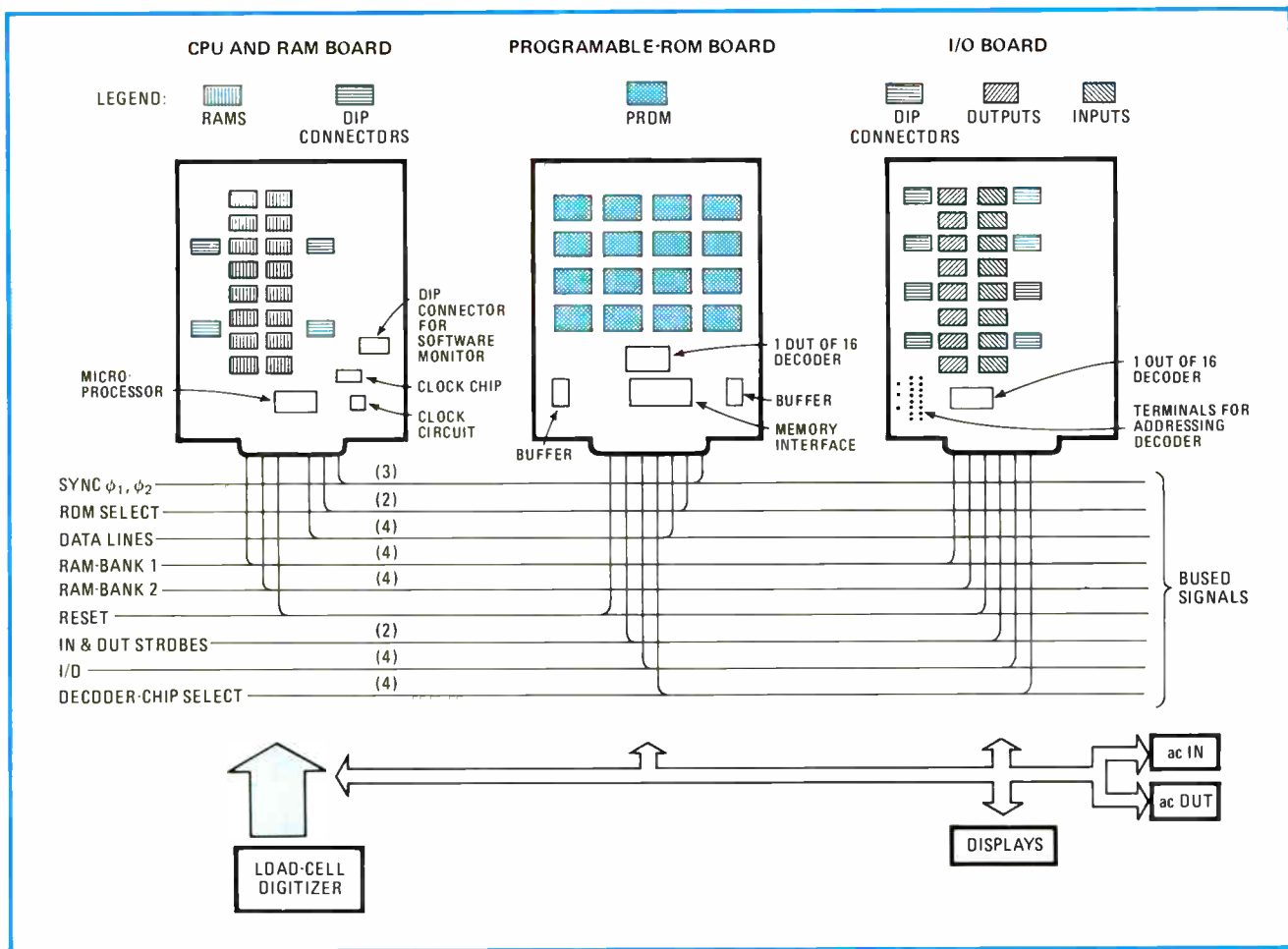
When the final program is ready to run in the 8080, an in-house-built microcomputer development system transfers it together with a debug program from the minicomputer disk to the 8080, where it is then debugged rapidly in its real environment rather than a simulated one. The process is so fast that a programmer working at a CRT terminal may edit source modules, assemble, link, and load a 20-k program in 5 minutes.

To customize the system for a particular application, an ACCOL compiler (run on the same minicomputer and itself written in Fortran) defines the control configuration of an UCS-3000 prior to shipment. ACCOL is the firm's own control-hardware-oriented language. In the field, a programmed panel enables the user to edit the USC-3000's software, again using ACCOL.

Bulk weighing system keeps operator honest

by Stanley E. Laberski
Howe Richardson Scale Co., Clifton, N. J.

A microprocessor controller enables a scale for such commodities as grain, chemicals, flour, and sugar not only to weigh them automatically, but also keep the operator honest. The Bulk-tronic can require the operator to identify himself by means of a number or badge reader before it will operate. What's more, until the



Bulk weighing. The CPU card, two PROM cards and 64 I/O cards plug into the system bus along with the a-d converter for the strain-gage load cells and the operator's display. All inputs and outputs, including power are transmitted through this bus. Two of the 16 RAMs are assigned to I/O-bank selection, and their output lines are hard-wired to the address terminals of the decoder.

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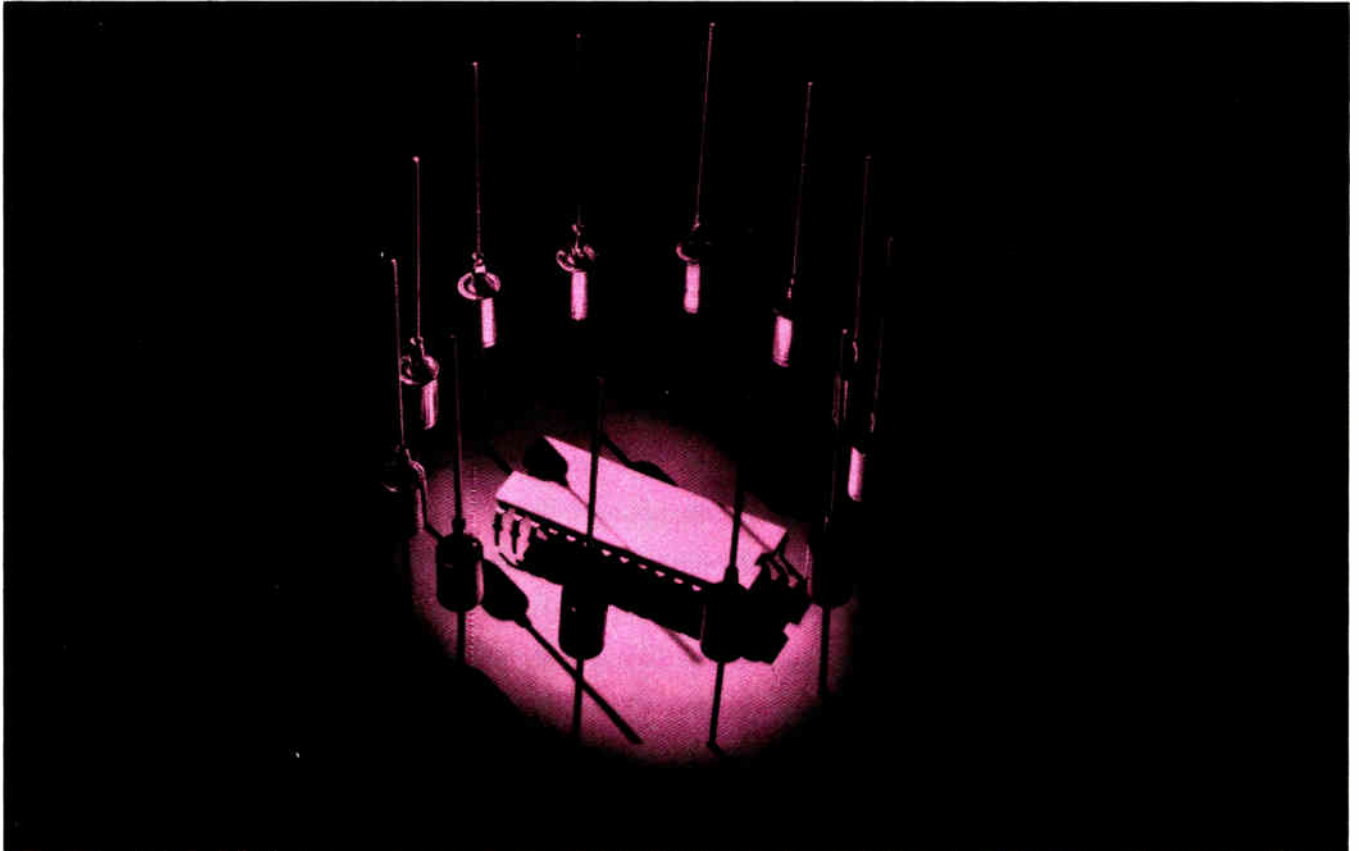
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weight has been logged by the scale's recorder, the controller won't open the hoppers to dispense the product.

To weigh a particular material, the operator selects by keyboard the product and the total weight desired. The controller then determines the optimum batch size for the available weigh hopper. If successive weighings are required, the controller totals the dispensed grain, adjusts the batch size to reach the desired weight, and cuts off the automatic cycling when all the commodity has been delivered and recorded.

The only way the system could be built economically and also provide system diagnostics and the capability to tie into a centralized computer system was to use programmable logic. After simpler devices had been tried and rejected, for reasons to be described later, the Intel 4040 microprocessor was chosen.

The maximum-capability system is built on three types of 6-by-8-inch cards that share a bus. The 4040 central processing unit is mounted on the first card, along with 16 random-access-memory chips; the second card contains the PROMs, and the third the I/O interface.

The cards plug directly into the bus, together with the analog-to-digital converter for the strain-gage load cells and the operator's numeric light-emitting-diode display. The bus is a 50-wire flat cable.

Each I/O card contains a 1-out-of-16 decoder plus terminals for hard-wired addressing of the device. By means of hard-wired addressing, the RAM output lines select the desired I/O bank with which the software is to exchange information. Any peripheral can have the addressing and decoder circuitry of an I/O card designed into it so that the software will treat it as an I/O card.

It was obvious from the beginning that the Bulk-tronic would need extensive I/O capability. Engineers started with the smallest and least expensive device—a single-card Intel 4004, together with support hardware for programming and debugging software. The 4004 uses the same programmable read-only memory chips as the PDP-16 minicomputer. A programmer controlled by a PDP 8 with editing, listing, and assembling capability was used to program the PDP-16 read only memory.

However, control simulations quickly showed that the

single-card 4004 had too small an I/O capability, so a larger, multi-card 4004 microcomputer was tried next. This device handled larger programs, which, however, were in assembly language and had no source-language listings with comments to aid in software debugging. Here is where the common PROMs proved valuable. The PDP-8 assembler was modified to accept 4004 source language, and the programmer to accept the PROM chips directly. These modifications made it possible to program and edit the 4004 in source language, add comments, and let the minicomputer assemble, load the programs into the PROM, and provide annotated listings of source and assembly language.

However, by now, it was apparent that the Bulk-tronic needed the more capable Intel 4040, with its ability to monitor individual instruction cycles, its larger number of subroutine nestings and index registers, and its larger instruction set.

Programmer can compensate for slow speed

Operating speed was found to be the only significant limitation of the 4-bit 4040 microprocessor. However, so long as the programmer keeps the instruction cycle time in mind, he can normally avoid problems because the system controls relatively slow real-time situations.

The maximum Bulk-tronic microcomputer system consists of one CPU card containing 1,280 hexadecimal character stored in 4-bit RAM. Also on the card is a dual-in-line package connector for attaching a software monitoring panel that contains single-step and stop-on-address controls and displays the instruction cycle. There may be two PROM cards, each with a memory interface chip and 16 PROMs for a card capacity of 4,096 8-bit instructions, and 64 I/O cards.

Each of the two PROM cards can service 32 I/O cards. And since each I/O card contains 32 inputs and 32 outputs, a maximum of 2,048 gated MOS inputs and 2,048 latched MOS outputs can be realized. There are also 64 p-channel MOS output lines from the 16 RAM chips, which are bought off the CPU through four 16-pin DIP connectors. The outputs of the first two RAMs also connect to the system bus, to implement I/O bank selection.

Measurement system logs analog data

by Richard E. Morley

Lion Precision Corp., Newton, Mass.

The acquisition and control of analog data on dimensions, pressure, flow, temperature, force, tension, and the like are widespread needs in industry. Meeting individual requirements with hard-wired logic imposes high engineering costs, and, in the end, the system becomes dedicated to a special purpose.

The Analog Data Acquisition Analysis and Control System (Adaacs) is a highly efficient, flexible microprocessor-based computer system designed for analog instrumentations systems (see figure, over). Its major functions are: to provide control of the instrumentation,

to provide digital encoding of analog data signals, to process the data, and to provide output data in analog and digital form to peripheral devices such as an alphanumeric display, meters, or a data-logging printer.

Contact and noncontact transducers provide the data in analog form to the Adaacs. If desired, closed-loop control of a process can be implemented.

Sixteen single-ended or eight differential analog input signals (expandable to 256) may be accommodated at the input interface. The Adaacs output interfaces include two EIA-standard output ports, which allow interface to a peripheral unit or a communication link. A third EIA interface is dedicated to a Termiflex Corp. HT/2 hand-held input terminal. Two output ports are provided for devices such as a meter and recorder.

The modular hardware and software of the system can meet the varying requirements of customers economically. A program function, the number of chan-

The Ten Most WANTED INSTRUMENTS



Brush Oscillograph 260



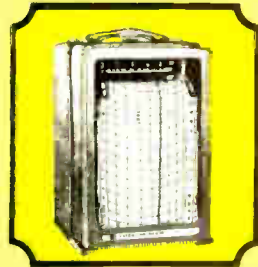
Nicolet
Digital Storage Oscilloscope



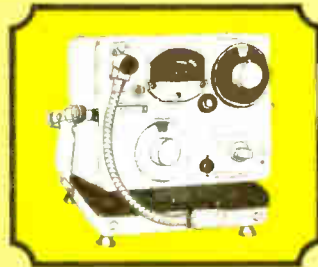
Hewlett-Packard 5302 A



Data Research
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Current tracer pinpoints failures

Instrument in family of troubleshooters for digital circuits uncovers faulty components; logic pulser is signal source

by Andy Santoni, Instrumentation Editor

Although the aim in troubleshooting digital circuits is to isolate the component that has caused a failure, no simple method has been devised until now to perform this function. At best, logic probes, oscilloscopes, and other digital troubleshooting gear have been able to determine no more than which node has failed—not which driver or receiver is responsible.

The model 547A current tracer from Hewlett-Packard Co. can determine precisely which component has failed because it can uncover the paths through which fault currents are flowing. For example, if a

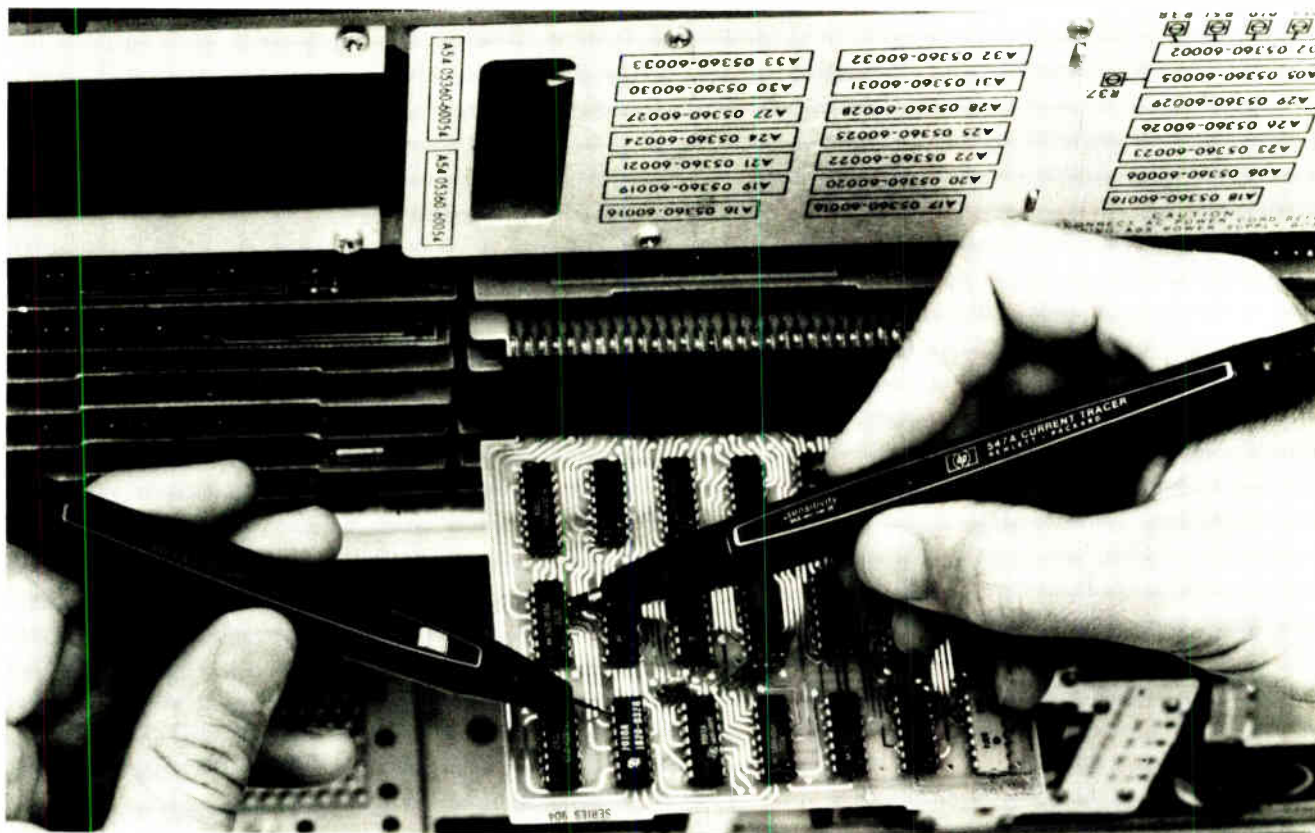
signal bus is stuck at ground, the 547A can determine whether the fault is in the receiver or driver, even in wired-OR circuits. The instrument can also uncover solder bridges or printed-wiring slivers on printed-circuit boards.

An adjunct to the current tracer is the model 546A logic pulser, which can also be used as a signal source for another member of this family of digital troubleshooting instruments, the model 545A logic probe [*Electronics*, March 4, p. 139], or other logic probes.

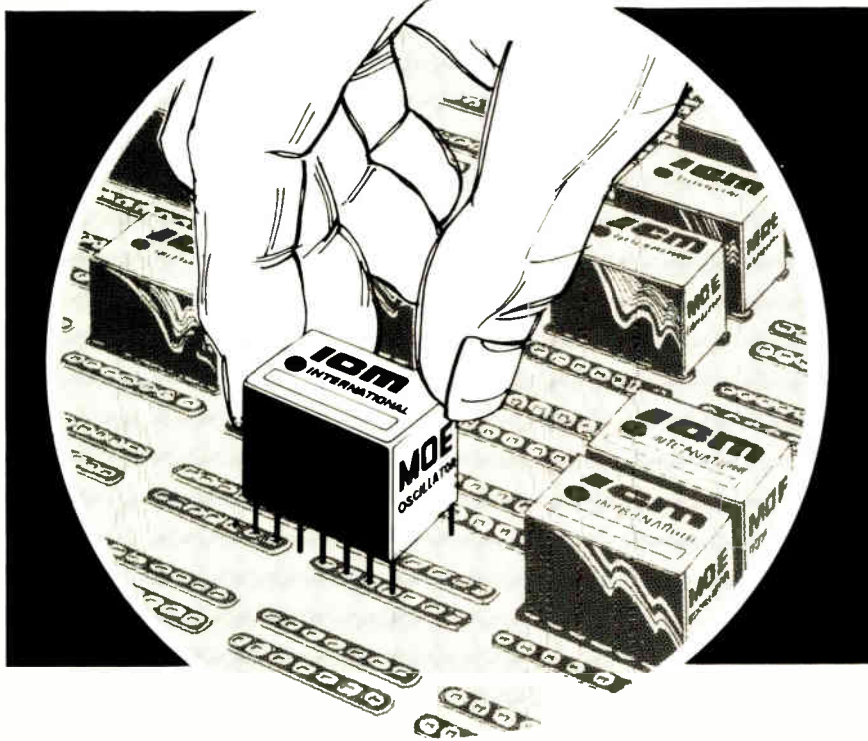
The current tracer, priced at \$350, locates low-impedance faults by fol-

lowing alternating-current pulses flowing to or from a fault. It senses the magnetic field generated by signals in the circuit or from the pulser, and a one-light indicator displays transitions, single pulses, and pulse trains. Because it is not voltage-sensitive, the tracer can be used with any logic family as long as current pulses over 1 milliamperere at repetition rates less than 10 megahertz are available.

The tracer uses a shielded inductive pickup and a wide-band, high-gain amplifier to provide the sensitivity needed to detect magnetic fields created by current changes



New products



INTERNATIONAL'S

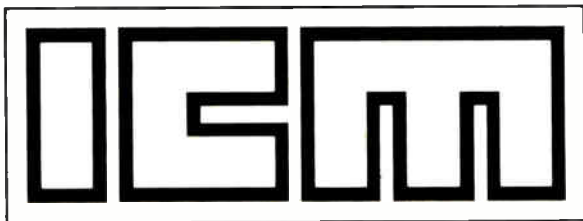
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MOE-5	6000KHz to 60MHz	+ .002% -10° to +60°C	Zero Trimmer	\$35.00
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International Crystal Manufacturing Company, Inc.

10 North Lee, Oklahoma City, Oklahoma 73102

along pc-board traces. The instrument's sensitivity is high enough to follow signals in multilayer boards, through the insulation in shorted cables, and on backplanes and motherboards.

In operation, the tracer is placed at a reference point, usually a node-driver output, and the sensitivity control is set so that the lamp just turns on. The probe can then be moved along the circuit path, and the lamp will go out when the shorted branch is passed.

Input sensitivity range is 1 milliampere to 1 ampere, and maximum current-transition rise time is 200 nanoseconds at 1 mA.

The current tracer requires a power supply of 4.5 to 18 volts dc with a maximum ripple of ± 500 mV above 5 v, and is protected against overloads up to ± 25 vdc for one minute. Maximum input current is 75 mA.

The tracer's power supply can be floating with respect to the supply of the circuit under test.

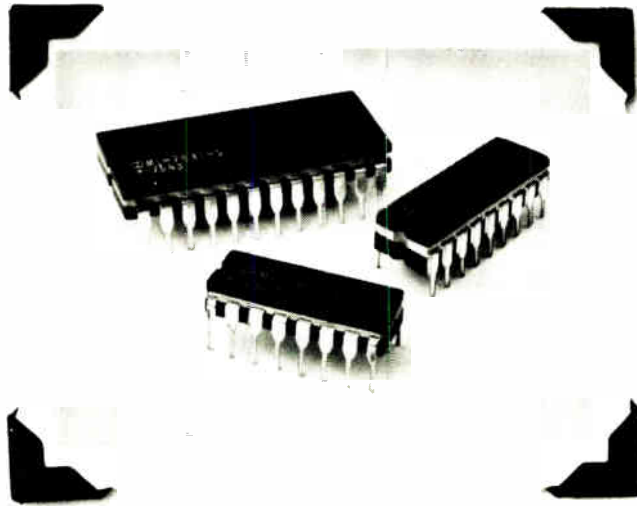
The model 546A logic pulser can drive high nodes low or low nodes high with short, high-energy pulses that cannot destroy the integrated circuits under test. It contains a read-only memory that allows push-button programmable operation with six output variations: single pulse, 100-hertz continuous-pulse stream, 100-pulse burst, 10-Hz continuous pulse stream, 10-pulse burst, or 1-Hz continuous pulse stream. The output waveform is chosen by pressing the push button or sliding it toward the probe tip; a table of codes is printed on the pulser's body.

A light-emitting-diode indicator monitors the pulser's output, eliminating the need to guess whether or not the output is active.

The pulser, priced at \$150, operates from supplies of 3 to 18 v dc and draws less than 35 mA. The top output is protected against continuous overloads of ± 50 v and short circuits, and the power-supply input is protected up to ± 25 v. Time-base accuracy is to within $\pm 10\%$.

Inquiries manager, Hewlett-Packard Co., 1501 Page Mill Rd., Palo Alto, Calif. 94304 [338]

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HM 7603 (three state)	256	32x8	16	40ns	50ns	\$2.95	\$5.95
HM 7610 (open coll)	1024	256x4	16	60ns	75ns	\$4.95	\$9.95
HM 7611 (three state)	1024	256x4	16	60ns	75ns	\$4.95	\$9.95
HM 7620 (open coll)	2048	512x4	16	70ns	85ns	\$9.95	\$19.95
HM 7621 (three state)	2048	512x4	16	70ns	85ns	\$9.95	\$19.95
HM 7640 (open coll)	4096	512x8	24	70ns	85ns	\$19.95	\$39.95
HM 7641 (three state)	4096	512x8	24	70ns	85ns	\$19.95	\$39.95
HM 7642 (open coll)	4096	1024x4	18	70ns	85ns	\$19.95	\$39.95
HM 7643 (three state)	4096	1024x4	18	70ns	85ns	\$19.95	\$39.95
HM 7644 (active pullup)	4096	1024x4	16	70ns	85ns	\$19.95	\$39.95

* Access time guaranteed over full temperature and voltage range Industrial ($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} \pm 5\%$)

Military ($T_A = 55^\circ\text{C}$ to 125°C , $V_{CC} \pm 10\%$)



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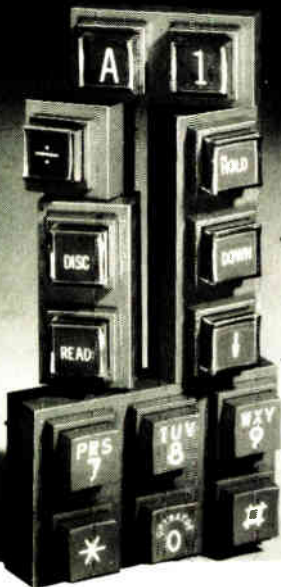
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New products

Meter samples fast

5½-digit dc unit takes 1,000 readings a second; options add resistance and ac-voltage scales

by Lawrence Curran, Boston bureau manager

Until now, users of dual-slope integrating digital voltmeters have had to settle for a maximum speed of 100 conversions per second in a 4½-digit instrument. But by using an extension of the dual-slope technique [*Electronics*, March 4, p. 26], Data Precision Corp. has come up with a 5½-digit entry capable of 1,000 conversions per second. The series 7500 is for use in automated test equipment and data-acquisition systems. It allows the user to choose from three conversion speeds, depending upon the amount of noise rejection required.

In addition, the new meter system allows the user to buy only the capability that he needs. The basic instrument, which can measure dc voltage and dc-voltage ratios, sells for \$2,995. It has a maximum error at 23°C of ±(0.007% of reading

+0.001% of full scale). It meets this specification for six months after calibration, the company says.

With the appropriate extra-cost options, the series 7500 is a universal ratiometer, according to company president Harold S. Goldberg. It will measure ac volts, ohms, and any ratio—including dc volts to ac volts and vice versa, ac volts to ohms and vice versa, dc volts to ohms and vice versa, ac volts to ac volts, and ohms to ohms.

Goldberg maintains that no other multimeter on the market offers this ratio-measurement versatility, and he points out that the 100-kilohertz frequency response of the ac voltmeter is no small achievement. The same is true of the 1,000-conversions-per-second capability, but it's a mixed blessing, Goldberg says. "One of the advantages of dual-

Choice of speed. Series 7500 meter can do up to 1,000 conversions a second. The basic instrument measures dc voltages and ratios, but options extend its capabilities.





Clean Sweep

F37 Log/Lin Sweep Function Generator


Precision Performance. F37's frequency setability is more accurate to begin with, because you can set your desired frequency with one fully calibrated coarse/fine control. The fine-tune vernier is centered on the dial so the output frequency meets accuracy specs wherever the vernier is set. And for easy and accurate sweep limit settings, you just swing the sweep limit cursor around.

Top Sweep Capability. Inside the F37's sturdy metal case is all the capability you need for sweep function generator applications — triggered sweep and burst modes, log/linear selection, and two separate plotter drive signals, for example. F37 sweep time is ten times faster, too, than competitive models — all the way from 10 picoseconds to 100 seconds.

You can count on F37's smooth performance and superior operating features because quality engineering and years of instrumentation experience are built into every Interstate Electronics unit.

F37 — the best sweep function generator you can buy for \$795.

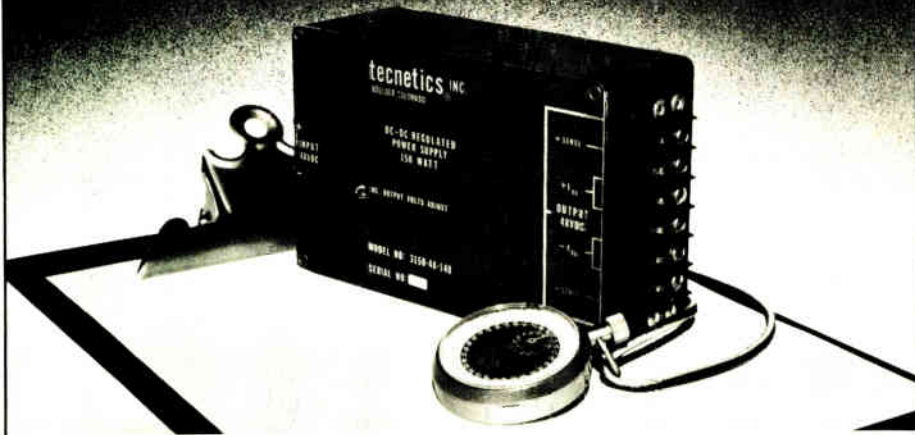
Interstate's SERIES 30 offers you a complete, economically priced line of quality-built function generators. Write for our SERIES 30 datapack.


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Circle 181 on reader service card

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EFFICIENCY EXPERT.



Up to 86% efficiency in Tecnetics DC to DC regulated converters.

When your design calls for a highly efficient regulated converter in a compact package, Tecnetics' 3000 series fits the bill. Efficiencies range from 66% to 86% with packing densities up to 2.78 watts per cubic inch. Our broad product line gives you a choice of models with 25, 50, 100 and 150 watts of power and outputs from 5 to 48 volts.

Standard features of the 3000 series include input-output isolation, overload and short circuit protection, input filters to reduce conducted EMI, and remote error

sensing to insure that the proper voltage is maintained at the point of load. All units are fully encapsulated and designed to meet the vibration, shock, humidity and altitude specs of MIL-E-5400.

So, when you are looking for state-of-the-art power converters, look to Tecnetics, the company with proven expertise. For more information and prices on the 3000 series, or three-hundred other power supplies, write for our 26 page catalog.

3000 SERIES HIGH EFFICIENCY REGULATED CONVERTERS

Output Power	150, 100, 50, & 25 watt models
Output Voltages	13 standard outputs from 5 to 48 V
Input Voltages	28VDC or 48VDC (48 VDC only on 150 w units)

Price range \$395-\$525.

Dimensions (excluding terminals):

25 & 50 watt:	4x4x2 inches 36 oz. Fully encapsulated
100 & 150 watt:	6x4x2 1/4 inches 60 oz. Fully encapsulated

Regulation:

Line (LL to HL)	0.3%
Load (1/2 to FL)	0.1%
Load (NL to FL)	0.4%
Temp	0.01% / °C

tecnetics® The Power Conversion Specialists P.O. Box 910,
1625 Range Street, Boulder, Colorado 80302 (303) 442-3837 TWX 910-940-3246

Circle 182 on reader service card

Roto-Kit, Inc. announces an ASCII Character Generator Kit for only \$79.95

FEATURES CRYSTAL OSCILLATOR FOR ACCURATE OUTPUT TONES OF 1070, 1270, 2025, AND 2225 PLUS BAUD RATES OF 110, 150, 300, 450, AND 600. IDEAL FOR TESTING MODEMS, ACOUSTIC COUPLERS, MINI COMPUTERS, ETC.

ORDER BY COUPON AND WE WILL PAY SHIPPING—USE YOUR MASTER CHARGE OR BANK AMERICARD.

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Model 88C

FOR MORE INFORMATION,
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ADDISON, ILL. 60101
(312) 543-2699.

182 Circle 242 on reader service card

New products

slope integration is its immunity to noise, but providing that immunity slows down the instrument. There's no way we can get rid of normal-mode noise with that 1-millisecond conversion. But if the user has a quiet signal or isn't greatly concerned about noise, he can get that speed."

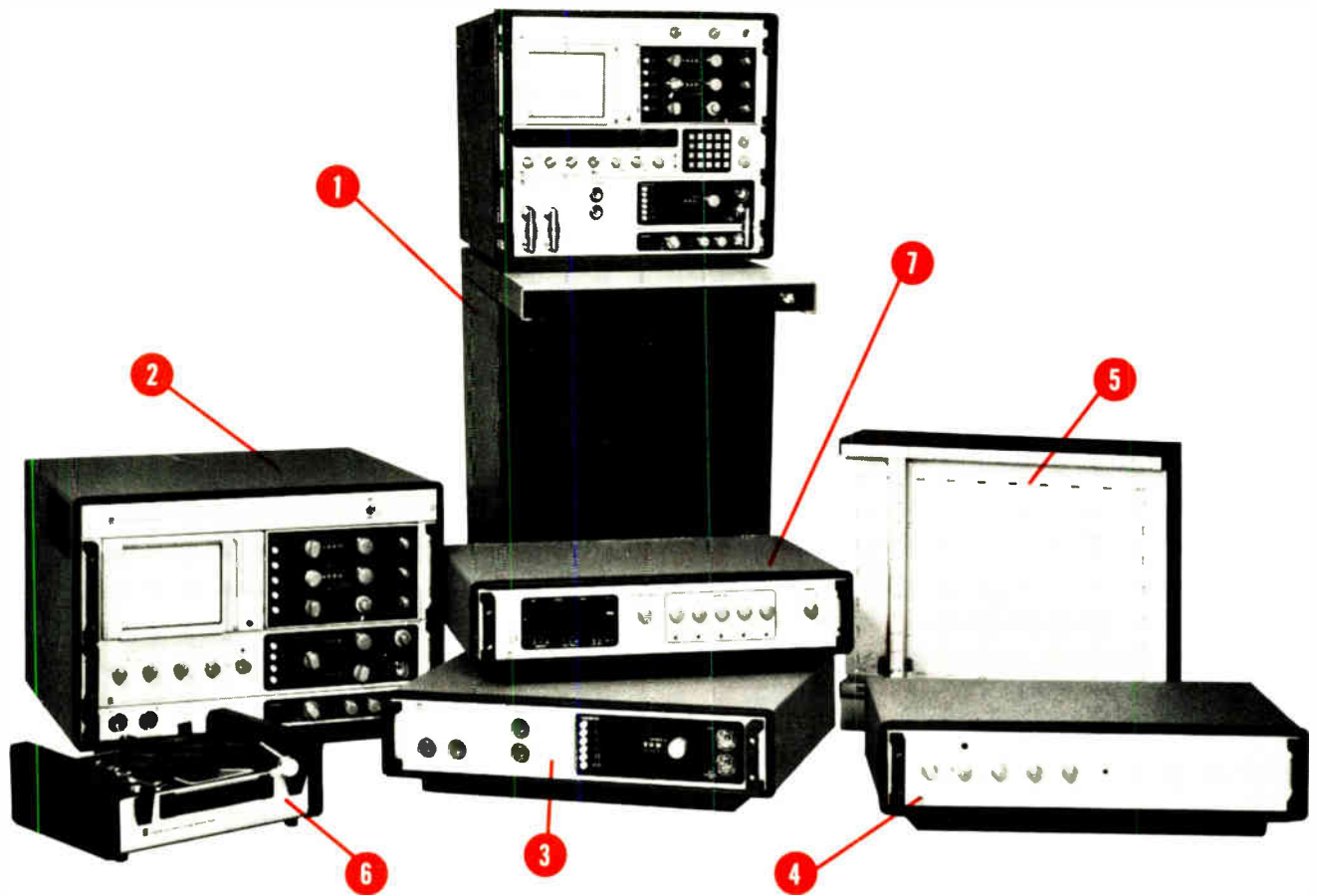
Data Precision also is offering front-panel or remote-control selection of slower conversion speeds for the user who needs better noise performance: 8 milliseconds (125 conversions/second) for the user who wants to filter out a lot of high-frequency noise, and 64 ms (15.6 conversions/second) to eliminate 60-hertz noise. When running at top speed, the instrument's noise rejection can be improved somewhat by switching its input active filter. But the filter does not have a very low-frequency cutoff because that kind of cutoff would slow down the instrument.

The quadruphase extension of the dual-slope integration technique is a big contributor to the instrument's speed. Developed by Paul Lucas, vice president for engineering, it integrates the unknown input for 200 microseconds to get the 1,000 conversions per second. The instrument integrates a large reference input for as long as is required to get within 1% of full scale. Then the comparator sends a signal that changes the reference current and the clock rate each by a factor of 100, reducing the load on the comparator for the final brief integration period, the company points out.

The series 7500 includes a binary-coded decimal output for easy interfacing to a computer. It also includes an optional (\$895) dedicated microprocessor to accommodate the IEEE 488 standard interface bus. The ac signal conditioner option adds \$545 to the price, while the ac reference is a \$495 option. The resistance signal conditioner goes for \$345, and a root-mean-square option is an additional \$100. Delivery time is 60 days.

Data Precision Corp., Audubon Rd., Wakefield, Mass. 01880. Phone (617) 246-1600 [339]

Electronics/April 15, 1976



Complete RF Network Analysis at prices you can afford

1 NARROW-BAND ANALYSIS

The new GR 2261 Synthesizer Network Analyzer was developed primarily for precision testing of narrow-band devices such as crystal or surface-wave filters, where amplitude, phase, and group-delay data is required. Besides preserving and enhancing the repeatability of measurements made with the 1710, the GR 1062 Synthesizer source adds the frequency resolution and stability needed to measure components with Q factors of up to several million, in the frequency range from 200 kHz to 500 MHz with 0.1-Hz increments.

2 BROAD-BAND ANALYSIS

The GR1710 RF Network Analyzer provides continuous swept-frequency transmission and reflection measurements of both magnitude and phase, from 400 kHz to 500 MHz with 0.005-dB resolution and over 100-dB dynamic range, dual measurement channels with 50- Ω and 75- Ω measuring circuits. Group-delay-measurement and Smith-Chart-display capabilities available as low-cost options.

3 PUSHBUTTON SIMPLICITY

The GR 1713 S-Parameter Sets add pushbutton selection for 50- Ω or 75- Ω measurements of the four S-parameters and includes a reference-plane extension and bias-insertion capability.

4 AUTOMATIC GREASE PENCIL

The GR 1716 Reference Storage Unit reduces magnitude, phase, or group-delay frequency-response errors by up to an

order of magnitude, permits automatic error correction, and provides a rapid means of rf comparison measurements.

5 X-Y PLOTS

The GR 1715 Sampling X-Y Recorder duplicates the 1710 and 2261 scope displays, even at the highest sweep rates, and features simple one-button operation and crisp 8-1/2 x 11 or 11 x 17-inch plots.

6 COMPONENT MEASUREMENTS

The GR 1710-P5 Immittance Probe provides swept measurements of impedance or admittance to characterize resistors, capacitors, cables, transistors, diodes, networks, etc.

7 PRECISION FREQUENCY MARKERS

The GR 1717 Frequency Marker/Counter provides five independently adjustable frequency markers with settable counter resolution and a 6-digit LED readout. This unit is operable only with the GR 1710.

For complete information, call or write:

 **GenRad**

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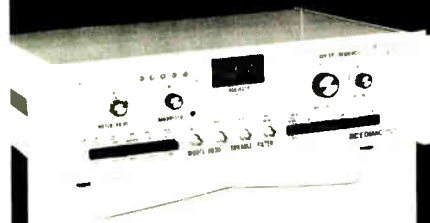
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The EDMAC Frequency Sleuth.

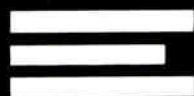


New Edmac Model 8030 Hi-Q Tunable Filter lets you search out those hard-to-identify frequencies. With it you can...

-  Eliminate unwanted background signals during signal analysis.
-  Analyze spectral components.
-  Measure harmonic distortions.
-  Secure adjustable, simultaneous band-pass and band-reject outputs.
-  Locate specific frequencies which indicate trouble areas during machine operation and testing.

Model 8030 tunes in selected frequency ranges from 1 to 30,000 Hz with corresponding independent bandwidth selections in a ratio of 100 to 1 for any given frequency, thus permitting maximum Q's of 100 to 1000. Sweeps through a preset frequency band in response to a remote voltage signal and can operate in a selectable mode to lock on and follow the strongest signal in a preset band. 130 microvolt RMS Filter background noise. Dynamic range to 95 db.

Find out more about the Model 8030 filter for your application. Write for descriptive literature.



**EDMAC
Associates, Inc.**

333 West Commercial Street
East Rochester, N. Y. 14445 (716) 385-1440

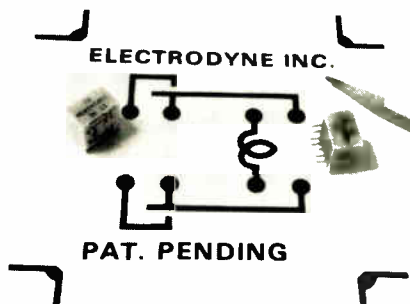
New products

Components

Relay is housed in tiny DIP

Electromechanical unit
can be driven by C-MOS;
switches 2 A at 28 V dc

Logic-compatible electromechanical relays in low-profile packages are continuing to proliferate. The latest is a double-pole, double-throw miniature unit from Electrodyne that can be driven directly by complementary-MOS-logic devices. This high-sensitivity electromechanical relay, the first in the company's



new series 10 family, is in a dual in-line package measuring merely 0.64 by 0.64 by 0.405 inch.

Electrodyne president A.E. Sprando says the new relay has a rotary balanced-armature design, rather than the glass-capsule reed switches commonly used in conventional miniature DIP relays. Since external interfacing devices, like amplifying transistors, are unnecessary, design costs are reduced, and less circuit-board space is needed, says Sprando. He adds that heat-sinking is not required.

Because of its proprietary ruggedized design, the series 10 unit may be placed directly on printed-circuit boards, flow-soldered, and then cleaned, without damage from heat or cleaning agents. The device is sealed against the environment in a molded plastic housing with a terminal-grid spacing of 0.1 by 0.3 in.

so that it can be plugged directly into DIP sockets for integrated circuits.

Although its coil power is only 30 milliwatts, the relay is capable of switching contact loads from dry circuits up to and including 2 amperes at 28 volts dc. Contact resistance is less than 50 milliohms, while contact-to-contact capacitance is only 0.3 picofarad. Furthermore, operating time for the units is 3 milliseconds, while electrical life expectancy at full-rated load is a minimum of 100,000 operations.

Unit price is \$12.60, dropping to \$6 each for lots of 1,000.

Besides the series 10 30-mw device, Electrodyne offers 1-, 2-, 3-, and 4-pole units in A, B, or C contact configurations.

Electrodyne Inc., 1404 21st St., Milwaukee, Ore. 97222 [341]

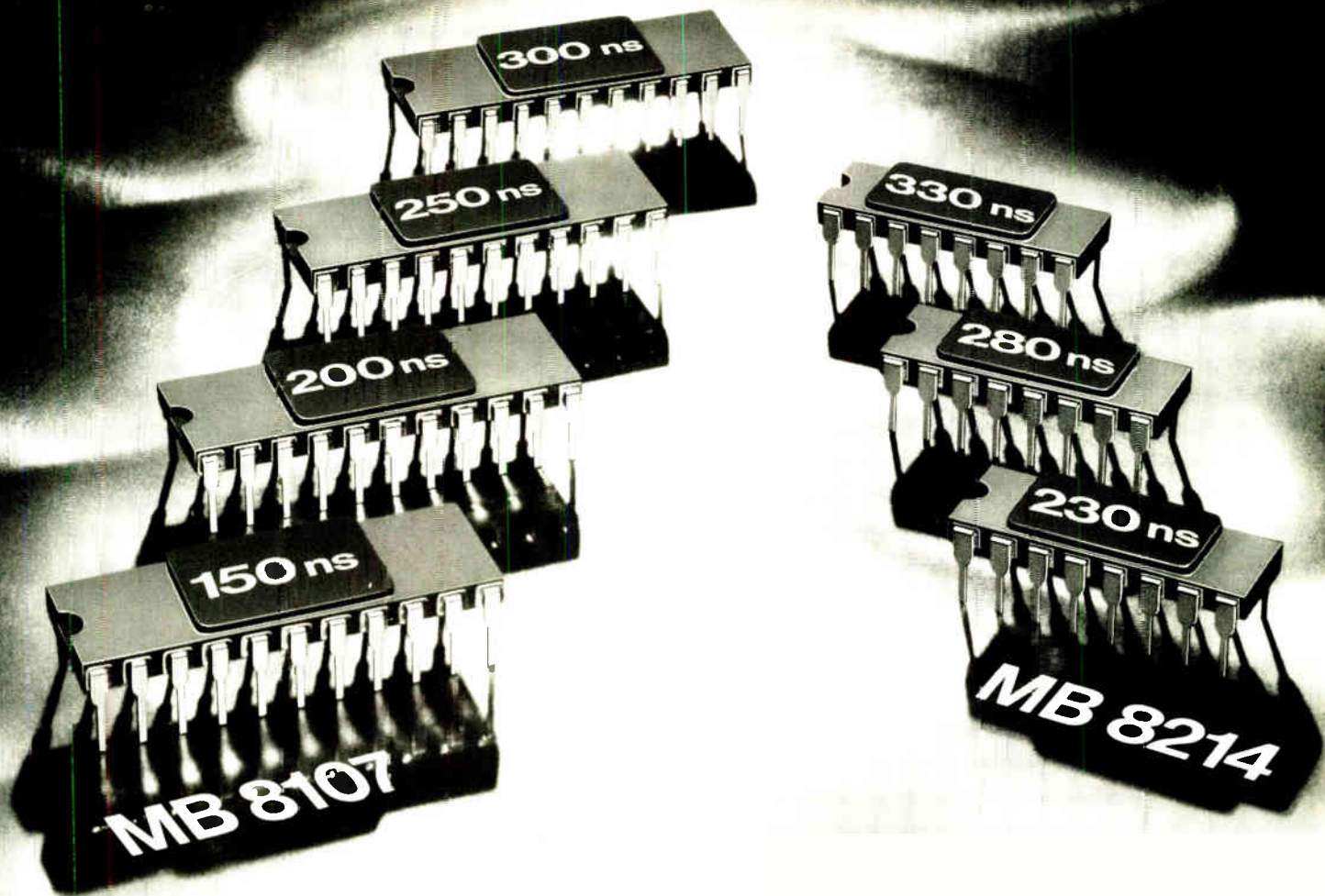
Ceramic capacitors
withstand up to 5 kV

A family of multilayer ceramic capacitors is available in a variety of sizes with voltage ratings from 1 to 5 kilovolts. Offered in 40 standard capacitances from 180 to 330,000 picofarads, the capacitors change value by less than 15% over the temperature range from -55°C to 125°C . The smallest units measure 0.25 by 0.20 by 0.15 inch, while the largest are 0.65 by 0.60 by 0.25 in.

Semtech Corp., 652 Mitchell Rd., Newbury Park, Calif. 91320. Phone William B. Krause at (805) 498-2111 or (213) 628-5392 [344]

Triac-output relays
switch up to 10 amperes

A series of solid-state relays rated for operation up to 10 amperes uses single triacs as the power-handling devices. Although the triacs do not work as well as dual SCRs in circuits with highly inductive loads, they provide cost savings of about 20%. The new relays, designated the TL 110 and TL 210, are for operation at



FUJITSU SEMICONDUCTORS

MOS MEMORY
4K Dynamic RAMs
MB 8214/8107

When it comes to semiconductor memories, faster speed can mean dollars of difference to you.

And when it comes to 16-pin and 22-pin industry-standard 4K RAMs, the best "money-savers" are the new MB 8214/8107 N-channel silicon gate MOS 4K RAM families from Fujitsu. Yes, with speeds that meet or exceed the best available anywhere, the MB 8214/8107 devices are sure to provide you with the type of performance you've been looking for. And both devices are fully interchangeable with your present source.

The 16-pin speed leaders

The new Fujitsu MB 8214 MOS 4K RAM family offers a 20ns speed advantage in the industry standard 16-pin 4K configuration with no increase in price! With Fujitsu 16-pin 4K RAMs, you get maximum access times of 330ns (type N), 280ns

(type E), or 230ns with the type H. And faster versions will be announced soon. Of course, all devices are fully TTL compatible, come in standard DIP packaging, and offer low power consumption for solid savings all around.

Four 22-pin chips to choose from

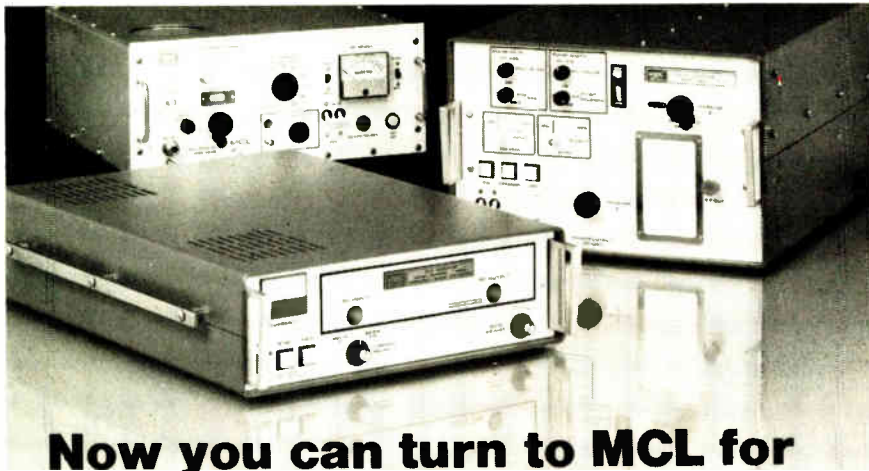
The Fujitsu MB 8107 22-pin family offers the industry-standard 2107/4060 pin-outs for full interchangeability. You have a choice of any of the three standard access times of 300ns (type N), 250ns (type E), and 200ns (type H)—all equal to, or better than, those of your present source. And, you have the additional availability of a very-fast model (type Y) with a fantastic guaranteed access time of only 150ns! In total, Fujitsu 4K RAMs are the way to go in semiconductor memories.

Proven reliability and available now
The MB 8214/8107 4K dynamic

RAM families are built by Fujitsu, a maker with proven reliability in the field of semiconductors and semiconductor memories. Stringent production standards, proven in-field performance, the most advanced processes, the capability to meet your requirements, and a price that's fully competitive—these and more add up to Fujitsu quality and Fujitsu service. So, contact Fujitsu now for the MB 8214, MB 8107, or any of your MOS memory requirements. Availability is NOW! Write or call for more information to Fujitsu California, Inc., Laboratory Division, 1280 East Arques Ave., Sunnyvale, California 94086, phone: 408-735-0735 telex: 346393.

FUJITSU LIMITED

Communications and Electronics
Marunouchi, Tokyo, Japan



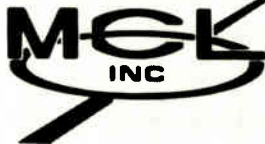
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MCL, Inc., 10 North Beach Avenue, La Grange, Illinois 60525. Or call (312) 354-4350.

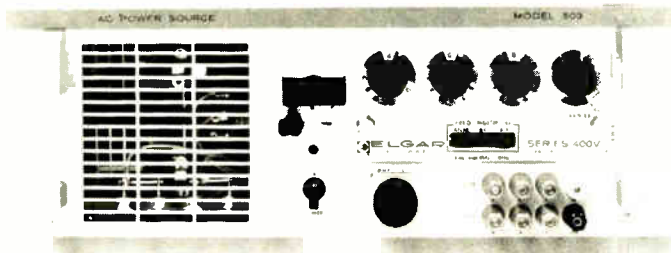
Circle 258 on reader service card

New products



140 and 280 volts rms, respectively. Triggering voltage is from 3 to 32 volts dc to accommodate all popular logic types. The relays have exceptionally high breakdown-voltage ratings—300 v for the 140-v units and 500 v for the 280-v devices. The optically isolated relays sell for about \$12.90 each in hundreds. Delivery is from stock.

Crydom Division, International Rectifier Corp., 1521 Grand Ave., El Segundo, Calif. 90245. Phone (213) 322-4987 [343]



Elgar Frequency Converters will never be out-phased.

Besides providing superbly regulated (.01%) undistorted AC power from 50 VA to 10 kVA, Elgar AC Power Sources (Frequency Converters) provide the potential to change. By simply adding plug-in modules and external interconnections, two or more units can be combined for 2-phase or 3-phase applications. And the frequency can be adjusted from 45 Hz to 10 kHz. Most important, all output functions are programmable. Why not phase out whatever you're using now, and give Elgar Frequency Converters a try? For more information,

contact Elgar Corporation, 8225 Mercury Court, San Diego, CA 92111. Phone (714) 565-1155.

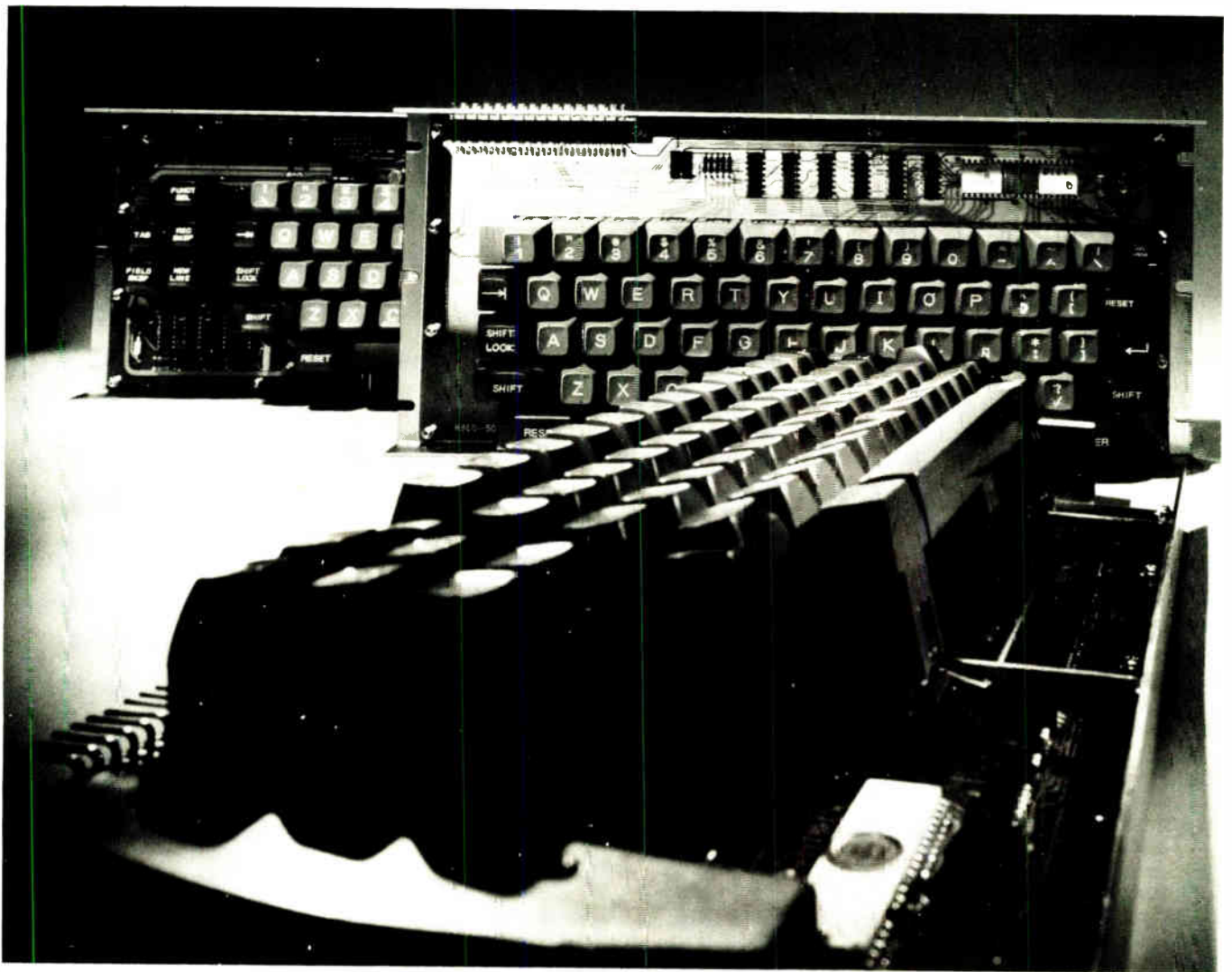


Elgar also is a leading producer of AC Line Conditioners and Uninterruptible Power Systems.

Foil heaters are compact and respond quickly

Supplied with a resistive temperature detector as an integral part of the heater element, a line of foil heaters has thicknesses of only 2 mils and a thermal time constant of less than 1 second. The flexible heaters can be cemented around crystal cans, thus eliminating the bulk of a component oven. Other applications include heating liquid-





Fujitsu brings you the light touch in keyboards

Are you a design engineer, production engineer, or other involved in the selection and purchase of components that go into the terminal equipment your company manufactures? Did you know that there is another type of keyboard on the market that offers a different type of key touch — a touch that can lead to productivity gains for your customers? Well, if you are, and if you didn't, then take a look at these new keyboards from Fujitsu and see what you (and your customers) have been missing. Fujitsu has a full line of keyboards available for terminal equipment, all

featuring the use of the Fujitsu FES-series snap-action key assembly. This highly reliable key assembly is a Fujitsu-engineered snap-action device that makes our keyboards easier to operate because it makes each key lighter to stroke, and with excellent tactile qualities. Thus, with smoother and lighter key touch, operators are less fatigued and, therefore, less prone to error. Fujitsu keyboards offer other advantages, too. Take the large capacity encoder fitted on each board — it's a MOS LSI ROM that helps to keep equipment size down and performance up. And there is a full selection of keyface styles (including

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Communications and Electronics
Marunouchi, Tokyo, Japan

For further information please contact

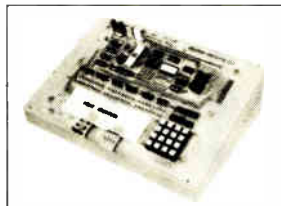
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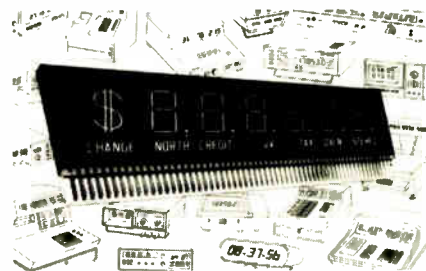
New products

crystal displays, stabilizing integrated circuits, and controlling the temperature of process baths. The unit shown in the photo is rated at 5 watts, has a 125-ohm detector and a 25-ohm heater, and allows control to within 1°F. In lots of 5,000, it sells for \$3.75 each. Delivery time is four weeks.

Photofabrication Technology Inc., Grenier Industrial Village, Londonderry, N. H. 03053. Phone (603) 668-4002 [345]

Screened-image displays include custom messages

The SP-400 series of planar gas-discharge displays includes both digits and customized fixed-format messages that are screened onto a glass substrate. Display areas up to 10 inches by 2 in. accommodate char-



acters and figures from 0.25 to 2 in. high. A typical unit, with seven character positions and seven message areas, sells for less than \$9 in lots of 5,000.

Screened Image Displays, Beckman Instruments Inc., Information Displays Operation, P.O. Box 3579, Scottsdale, Ariz. 85257. Phone (602) 947-8371 [346]

Thick-film, axial-lead resistors are very stable

A series of high-value resistors (resistance from 1 to 100 megohms) is made by a thick-film process that yields tolerances as tight as 0.05% and temperature coefficients as low as 25 ppm/°C. Unlike carbon-film resistors, the low-noise axial-lead devices can be produced in any quantity or tolerance at any time of

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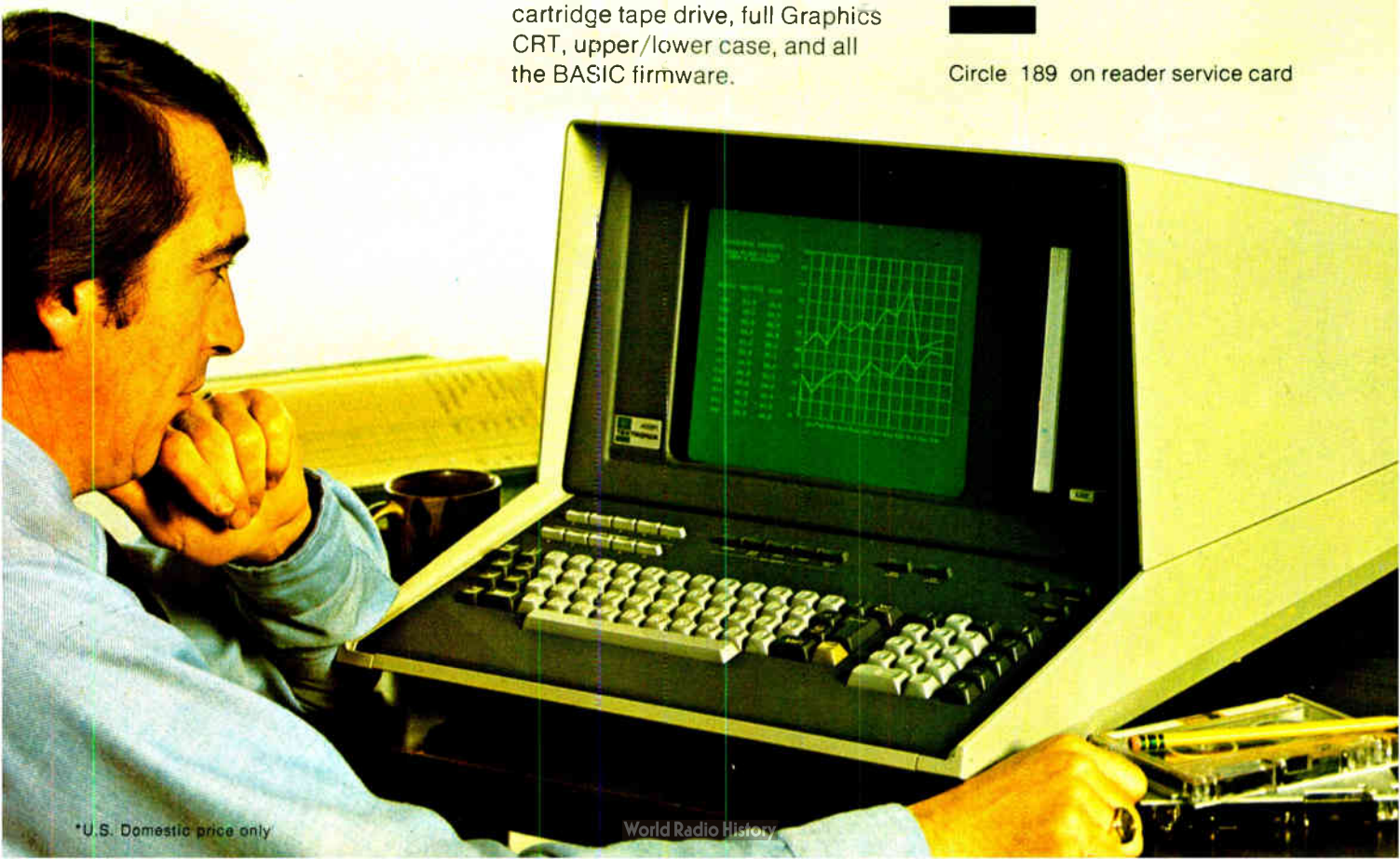
Talk to Tektronix today! Your local Sales Engineer will fill you in on our 4051 software. Our range of peripherals. Our flexible purchase and lease agreements. And he'll set up a demonstration right on your desk. Call him right now, or write:

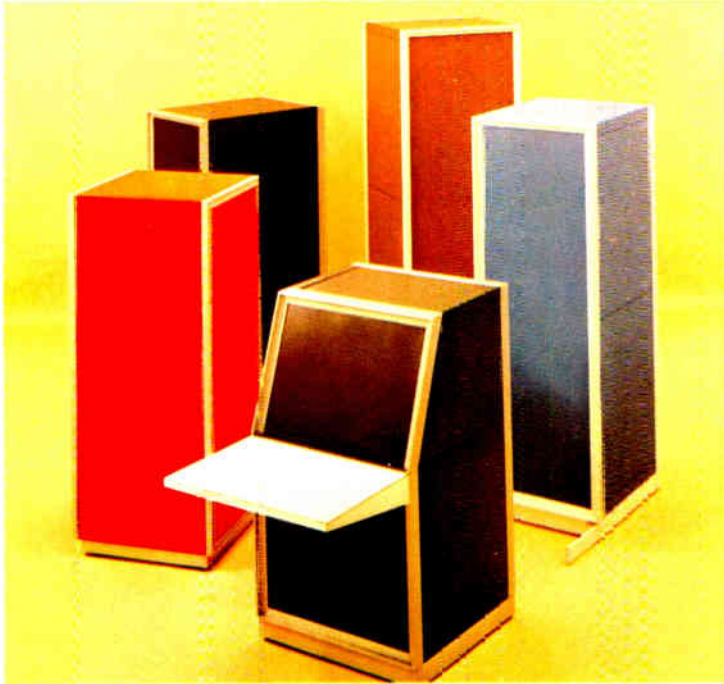
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Circle 189 on reader service card





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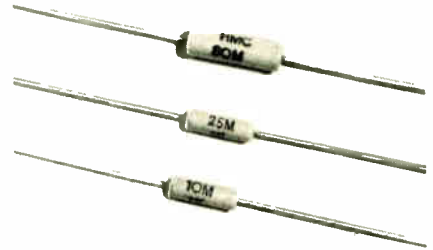
We think Optima racks are silent salesmen. Once you see how they get your product going, so will you. For size information, color selection, options and accessories, call 404-939-6340 or write...

OPTIMA

Optima® Enclosures a division of Scientific-Atlanta, Inc
2166 Mountain Industrial Blvd., Tucker, Georgia 30084

SA-87515

New products



the year that they are required.

Hy-Meg Corp., 245 W. Roosevelt Rd., West Chicago, Ill. 60185. Phone (312) 231-6688 [347]

Low-profile relays have 160-mW sensitivity

An extension of the widely accepted MPC series of relays, MPCS devices have low profiles and a pull-in sensitivity of 160 milliwatts. Capable of switching 2 amperes, the relays are offered in two versions: one has a single set of form C contacts, and the other has two. Measuring only 0.415 inch high by 0.600 in. wide by



1.1 in. long, the new MPCS series can operate directly from TTL driver circuits. The relays combine long life and high reliability with low cost. The version with a single form-C contact configuration sells for as little as \$1.88 in lots of 1,000.

Gould Inc., Allied Control Division, 100 Relay Rd., Plantsville, Conn. 06479. Phone (203) 628-9654 [349]

Polyester capacitors are rated up to 16 kV

Offered with voltage ratings from 2 kilovolts dc to 16 kv dc, a family of metalized polyester capacitors is



PROFIT

...a few ways Belden can help you protect your bottom line.

Wire and cable usually cost less to buy than install. And poor performance can cut into profitability deeper than potential penny-per-foot savings on an initial buy.

Here's how Belden can help protect your bottom line performance...

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UNIQUE PUT-UP CAPABILITY: Ask about Belden's UNREEL™ packaging concept. A dispensing system that eliminates the reel. And time robbing snails, backlash, and tangle problems. We have a number of ways to put-up wire that can save you production time and money.

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DESIGN KIT: If you're looking for design help, we have a kit that covers most of the nitty-gritty aspects of performance characteristics, costs, and material capabilities. Send for your kit, today.

GREAT DELIVERY: Belden has increased production capabilities and offers shorter lead times on most cable configurations. Check it out.

Profit protection is part of the Belden cable package. But, find out for yourself. Write: Belden Corporation, Electronic Division, P.O. Box 1327, Richmond, Indiana 47374.

8-55

...new ideas for moving electrical energy

BELDEN 

World Radio History Circle 191 on reader service card



Dialight sees a need:

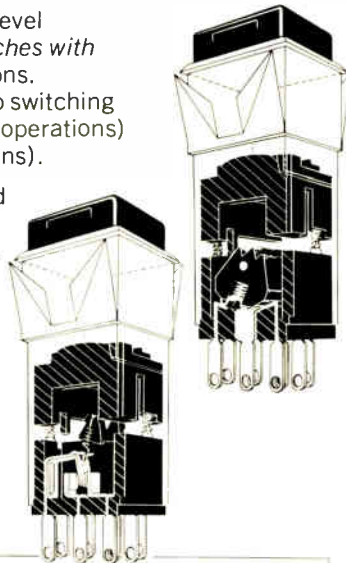
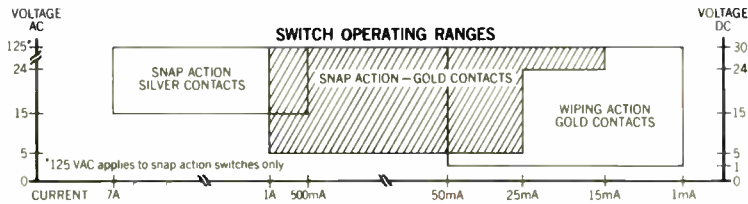
(Need: A switch for all reasons.)

Reason 1: Dialight offers three switch configurations to meet all your needs—*snap-action switches with silver contacts* for moderate-level applications,

snap-action switches with gold contacts for intermediate-level applications, and *wiping-action switches with gold contacts* for low-level applications. Each of these ranges is served by two switching actions—momentary (life: 600,000 operations) and alternate (life: 250,000 operations).

Reason 2: Dialight's snap-action and wiping-action switches come in a new modular design concept... a common switch body for either high or low current operation. All 554 series switches and matching indicators have the same rear-panel projection dimensions.

The snap-action switching mechanism guarantees a fast closing and opening rate. This insures that contact force and contact resistance



types. There are over 240 switch variations to choose from.

The 554 illuminated switch, designed for front of panel lamp replacement, gives you a choice of five different bezel sizes... 3/4" x 1", 5/8" x 3/4", 3/4" square, 5/8" square, and 1/2" square. The first four sizes are also available with barriers. You also get a choice of six cap colors... white, blue, amber, red, green, and light yellow... four different underlying filter colors... red, green, amber, and blue and a variety of engraved or hot-stamped legends... over 300 cap styles... over 100,000 combinations.

There is also a variety of terminal connections... solder blade, quick connect, and for PC board insertions.

Reason 4: Dialight's 554 series is designed as a low cost switch with computer-grade quality.

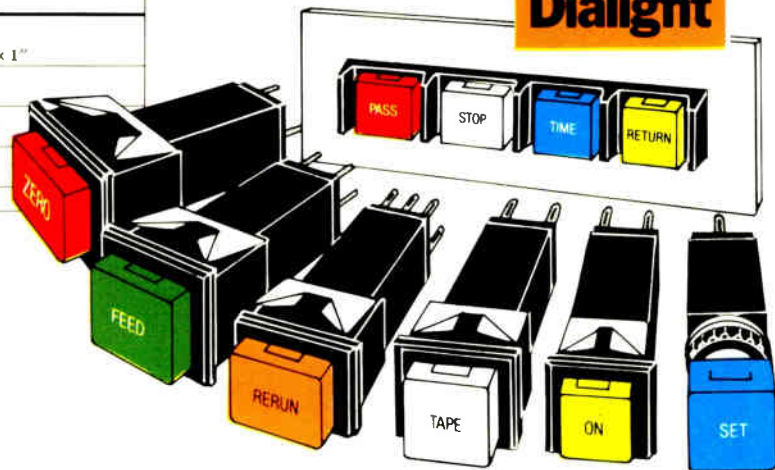


PRODUCT SELECTOR GUIDE						
SWITCHING ACTIONS	Snap-Silver contacts		Snap-Gold contacts		Wiping-Gold contacts	
	SPDT	DPDT	SPDT	DPDT	SPDT	DPDT
MOMENTARY	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
ALTERNATE	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
OPTIONS						
	PUSH BUTTON CAP SIZES					
	1/2" Sq.	5/8" Sq.	5/8" x 3/4"	3/4" Sq.	3/4" x 1"	
BEZEL MOUNTING TO ACCOMMODATE	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
BEZEL MOUNTING WITH BARRIERS TO ACCOMMODATE	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
PANEL MOUNTING TO ACCOMMODATE	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
MATCHING INDICATORS	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	

are independent of the switch's actuation speed.

In the wiping-action switch, the contacts are under constant pressure (A unique Dialight design). This insures long life with a minimum build-up of contact resistance.

Both switch types are tease-proof.



DIALIGHT

A North American Philips Company
203 Harrison Place, Brooklyn, N.Y. 11237
(212) 497-7600

New products



aimed at high-density packaging applications. Designated type X675HV, the capacitors are available with values up to 0.68 microfarad, insulation resistances of 30,000 megohms per microfarad, and a dissipation factor of less than 1% at 1 kilohertz. The capacitors have an operating temperature range of -55°C to 65°C . They can be operated up to 85°C with a 25% voltage derating. Delivery time for the devices is 30 days.

TRW Capacitors, 301 West O St., Ogallala, Neb. 69153 [348]

TOPICS

Components

Centralab Electronics division, Globe-Union Inc., Fort Dodge, Iowa, has introduced a line of slide potentiometers with an enclosed top slot that helps keep dirt from entering the unit. The series 700 devices are offered with both linear and audio tapers. . . . **Alco Electronic Products Inc., North Andover, Mass.**, is offering miniature rotary switches, the MRC series, with turret terminals suitable for hand-wired or printed-circuit applications. . . . **Allen-Bradley, Milwaukee, Wis.** has had its type CC quarter-watt cermet film fixed resistor, style RLR07, approved to Revision C of MIL-R-39017. This means that the resistors will now be available with a 1% tolerance as well as 2%.



Scanbe·gram



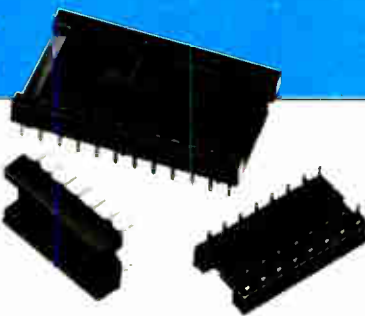
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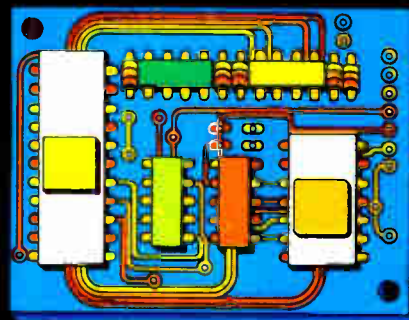
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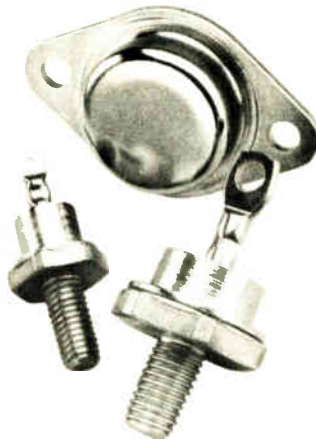
Semiconductors

Rectifiers rated at 500 V, 50 A

Close control of gold-doping limits leakage current; diodes recover in 50 ns

Gold-doping has been used for some time by rectifier manufacturers to control the recovery time of switching devices and make them faster. But too much gold in the process can lead to undesirably high leakage currents at elevated junction temperatures, limiting the maximum voltage possible. Unitrode Corp. has a proprietary gold-doping technique to closely control the amount of gold deposited—a method that has extended Unitrode's new family of switching rectifiers for power-supply applications to 500 volts at 50 amperes [*Electronics*, March 4, p. 26].

Peter Jenner, manager of product



marketing at the company, says only that Unitrode has developed a way to prevent over-doping with gold, and over-doping "shoots the leakage current way up." This control, combined with package materials that minimize thermal resistance, permits the extension beyond today's best devices, which are rated at 450 V at 12 A, says Fred Swymer,

Unitrode's manager of rectifier products.

The company hasn't sacrificed anything in recovery time, either, in its new line. All of the devices have a specified recovery time of 50 nanoseconds, which Swymer maintains is 25 ns faster than most devices now available.

At the low-current end of the scale, the Unitrode's family begins with 2-A and 4-A axial-lead devices. There are also a unit in a DO-4 package rated at 2 A, a DO-5-packaged rectifier at 50 A, a TO-3-housed device at 3 A, and a 30-A entry in a center-tap TO-3 package. Each of these devices has voltage ratings of 200, 300, 400 and 500 V, and each of them has a forward-voltage drop of 1.1 V at the output current. The highest leakage level for any of them is 1 milliamper.

Unitrode uses a hard-bonded assembly technique for these rectifiers in newly designed packages that minimize thermal resistance, at least in part, by using materials in the joining system that "handle the rated currents continuously with a good margin of safety," Swymer says. In effect, the company has doubled the current-carrying capability of the DO-4 and DO-5 packages, he says.

The 500-v, 50-A unit will cost \$17.20 in quantities of 100; the 200-v, 20-A rectifier is priced at \$10 in those quantities. Delivery time is two to four weeks.

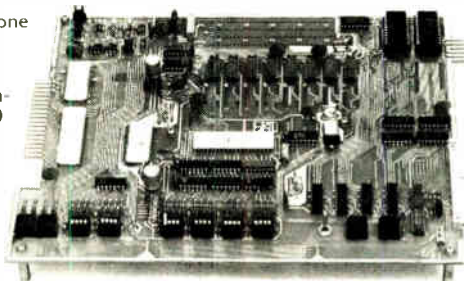
Unitrode Corp., 580 Pleasant St., Watertown, Mass. 02172. Phone Fred Swymer at (617) 926-0404 [411]

V-f converter also changes frequency to voltage

A monolithic voltage-to-frequency converter, the A-8400, has the added capability of performing frequency-to-voltage conversions. As a v-f converter, the unit converts voltages at 0 to +10 volts or currents at 0 to +1 milliamper to frequencies as high as 100 kilohertz. The full-scale frequency, set by an external resistor and capacitor, can be less

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than 100 kHz, if desired. Conversion linearity is within 0.05% at 100 kHz full scale, and within 0.01% at 10 kHz. The unit's temperature coefficient is typically ± 50 ppm/ $^{\circ}$ C. In the f-v mode, the time constant of the output integrator can be varied externally for flexibility in trading off response time and ripple.

Housed in a standard 14-pin ceramic dual in-line package, the A-8400 operates over the temperature range from 0 $^{\circ}$ C to 70 $^{\circ}$ C and has a unit price of \$15. The model A-8400-ETI, rated for operation from -25 $^{\circ}$ C to 85 $^{\circ}$ C, sells for \$20. Delivery of both units is from stock, the company says.

Intech/Function Modules, 1220 Coleman Ave., Santa Clara, Calif. 95050. Phone Bill Jumper at (408) 244-0500 [413]


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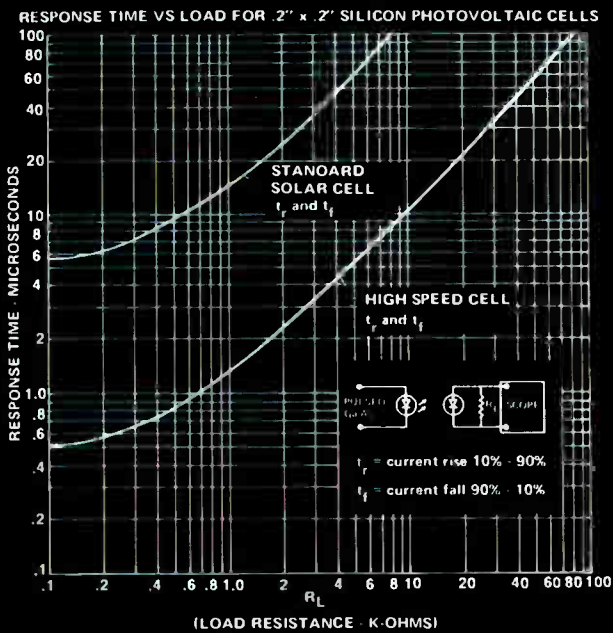
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ings as high as 45,000 A for the thyristors and 70,000 A for the diodes facilitate the design of fuseless control systems.

Power Semiconductors Inc., 90 Munson St., P.O. Box 296, Devon, Conn. 06460. Phone Janos de Warga or John Mungenast at (203) 874-6747 [414]

1-k random-access memory
has 25-ns access time

Emitter-coupled logic gives the 1,024-bit random-access memory, model HM 2110-1, a maximum access time of 25 nanoseconds and a power dissipation of 0.5 milliwatt per bit. A slightly slower memory, the HM2110, has an access time of 35 ns at the same power dissipation. Developed for scratch-pad, control, and buffer-storage applications in high-performance computers, the memories are the largest in Hitachi's line of extremely fast ECL RAMs. The family includes the 128-bit HD10147 which has an access time of 12 ns and a power dissipation of 3.3 mW/bit.

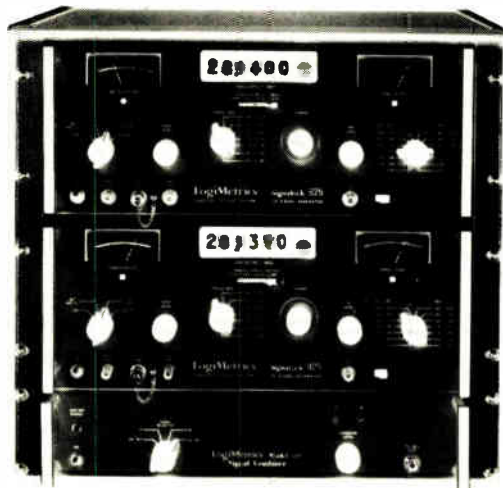
Hitachi Ltd., New Marunouchi Bldg., No. 5-1, 1-Chome, Marunouchi, Chiyoda-ku, Tokyo, Japan. In U.S., write to Bell & Stanton Inc., 909 Third Ave., New York, N.Y. 10022. Phone John P. Margaritas at (212) 759-4800 [415]

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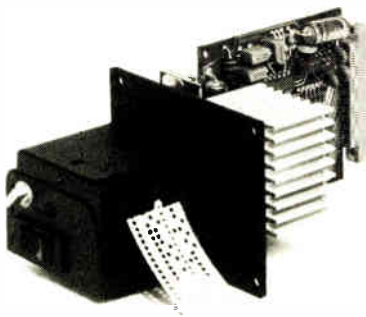
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may also strobe the output data. Power requirements are +5 V at 200 mA and 24 V at 600 mA. Stand alone versions with parallel or serial RS 232 outputs, fanfold box and spooler are also available. Price \$250 (1-99 units). Addmaster Corporation, 416 Junipero Serra Drive, San Gabriel, CA 91776. (213) 285-1121.

198 Circle 198 on reader service card

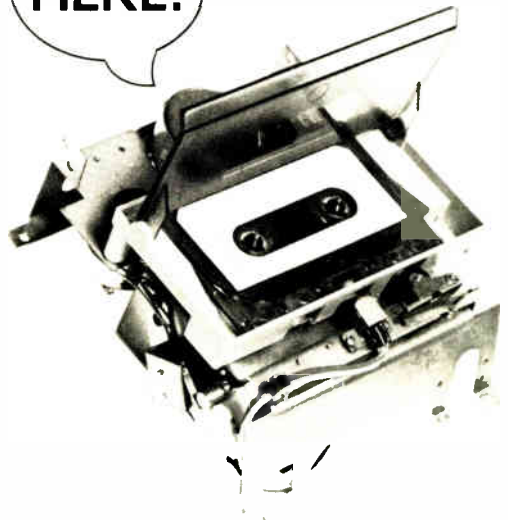
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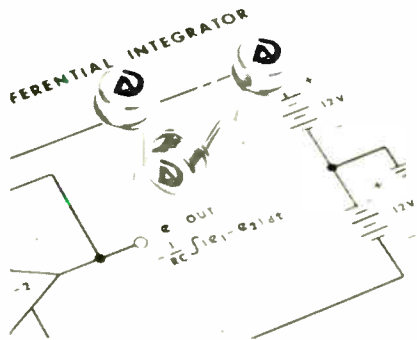
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New products



tion ratio of 160 dB. The unit pulls only 5 milliamperes from its ± 12 - to ± 20 -V dc supplies. This low power consumption, combined with a 200-millisecond warm-up time, makes the amplifier a good choice for battery-powered equipment. Housed in an eight-pin hermetic TO-99 can, the AM-490-2C sells for \$49 in small quantities. Two companion units are the AM-490-2B, which has a maximum drift of $0.3 \mu\text{V}/^\circ\text{C}$ and sells for \$44, and the -2A, which has a maximum drift of $1 \mu\text{V}/^\circ\text{C}$ and is priced at \$39. Delivery is from stock.

Datel Systems Inc., 1020 Turnpike St., Canton, Mass. 02021. Phone Eugene Zuch at (617) 828-8000 [416]

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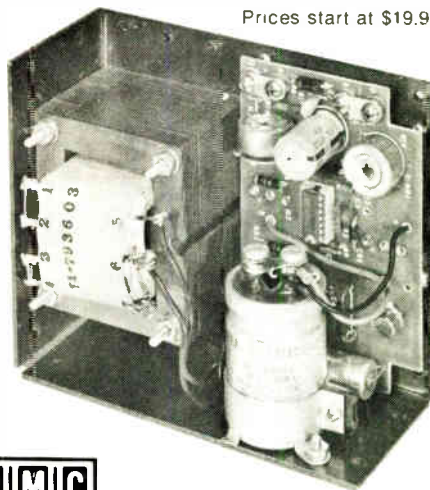
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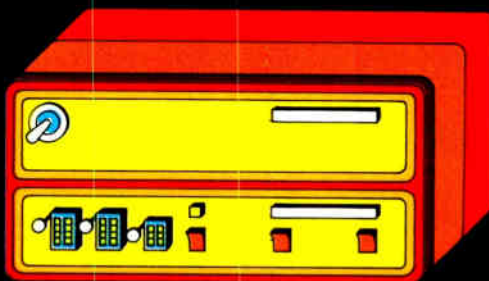
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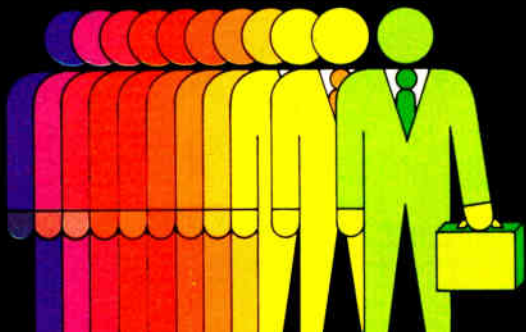
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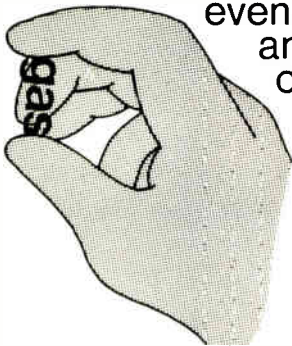
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Digital IC Tester Model 1248. Devices tested: 14 and 16 pins. TTL, DTL and CMOS @ 5V.

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Digital IC Tester Model 1249. Devices tested: TTL, DTL @ 5V, HTL @ 15V, CMOS @ 5V, 10V, 15V.



Tests performed: Same as 1248. Remarks: Interfaces with manual and automatic handlers. Multiple voltages for CMOS.

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Circle 251 on reader service card

New products

sions. These have access times and 100-piece prices of: 300 ns for \$15.30, 250 ns for \$19.80, and 200 ns for \$21.60.

Advanced Micro Devices Inc., 901 Thompson Pl., Sunnyvale, Calif. 94086. Phone (408) 732-2400 [417]

10-bit multiplying d-a converter sells for \$15

A monolithic C-MOS multiplying digital-to-analog converter with 10-bit resolution, accuracy, and linearity sells for only \$15 in hundreds. The AD7530 operates from a single 5-to-15-volt dc power supply and dissipates a total of only 20 milliwatts. The unit has a maximum temperature coefficient of gain of 10 ppm of full scale per degree Celsius and settles to within 0.05% of final value within 500 nanoseconds. Delivery is from stock.

Analog Devices Inc., P.O. Box 280, Norwood, Mass. 02062 Phone Lowell Wickersham at (617) 329-4700 [418]

TOPICS

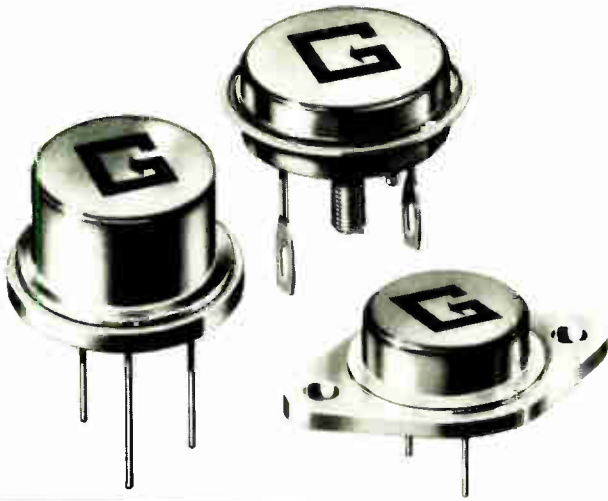
Semiconductors

Intersil Inc., Cupertino, Calif., has completed an agreement with **Signetics Corp., Sunnyvale, Calif.**, to become an alternate supplier of Signetics D-MOS devices, including ICs and a broad line of FETs.

Synertek, Santa Clara, Calif., is introducing a line of ion-implanted n-channel shift registers as direct replacements for the p-channel AMD 2833 and the Signetics 2533.

The Nitron division of McDonnell Douglas Corp., Cupertino, Calif., has introduced its NCM 7040—a 256-bit non-volatile p-MNOS memory. Priced at \$10 in hundreds, the unit is believed to be the first commercially available unit of its type.

Teledyne Crystalonics, Cambridge, Mass., is marketing FETs as diodes for the first time. The 1N5283 through 1N5314 devices are current-limiting units.



Q:

**WHERE CAN YOU GET
RELIABLE GERMANIUM
POWER TRANSISTORS?**

A:

GPD

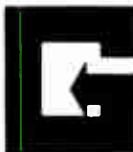
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TRANSISTOR FACTORY?**

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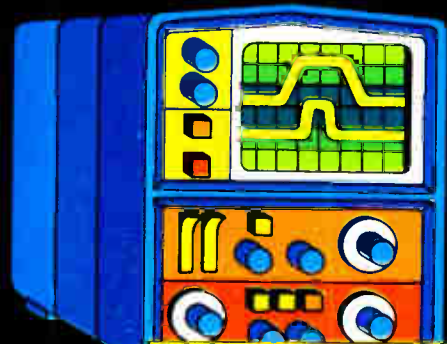
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THE 2650 IS OVER
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Your system's features can be extended with the speedier 2650. Current 2650 software will apply.

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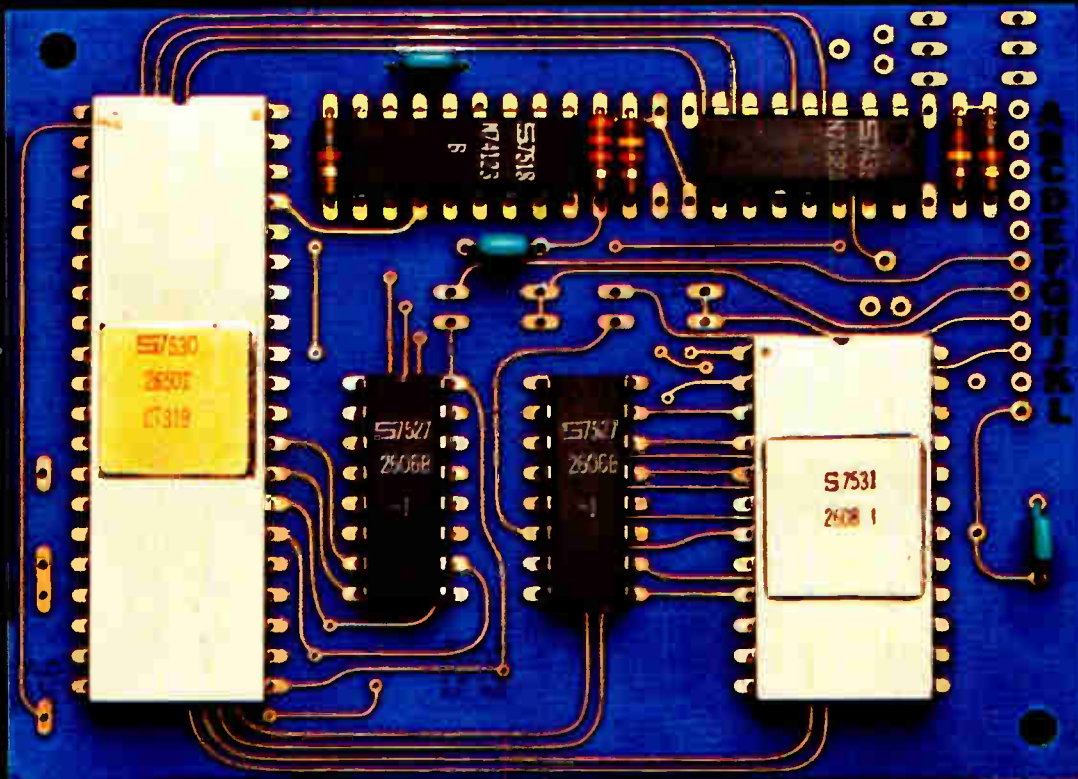
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THINK

Signotics μ P
a subsidiary of U.S. Philips Corporation

Circle 247 on reader service card 201

The easiest-to-use microprocessor



(Photograph approximately 2x actual size.)

The single-chip 2650 is easiest-to-buy, too. Now only \$21.50 (100-up).

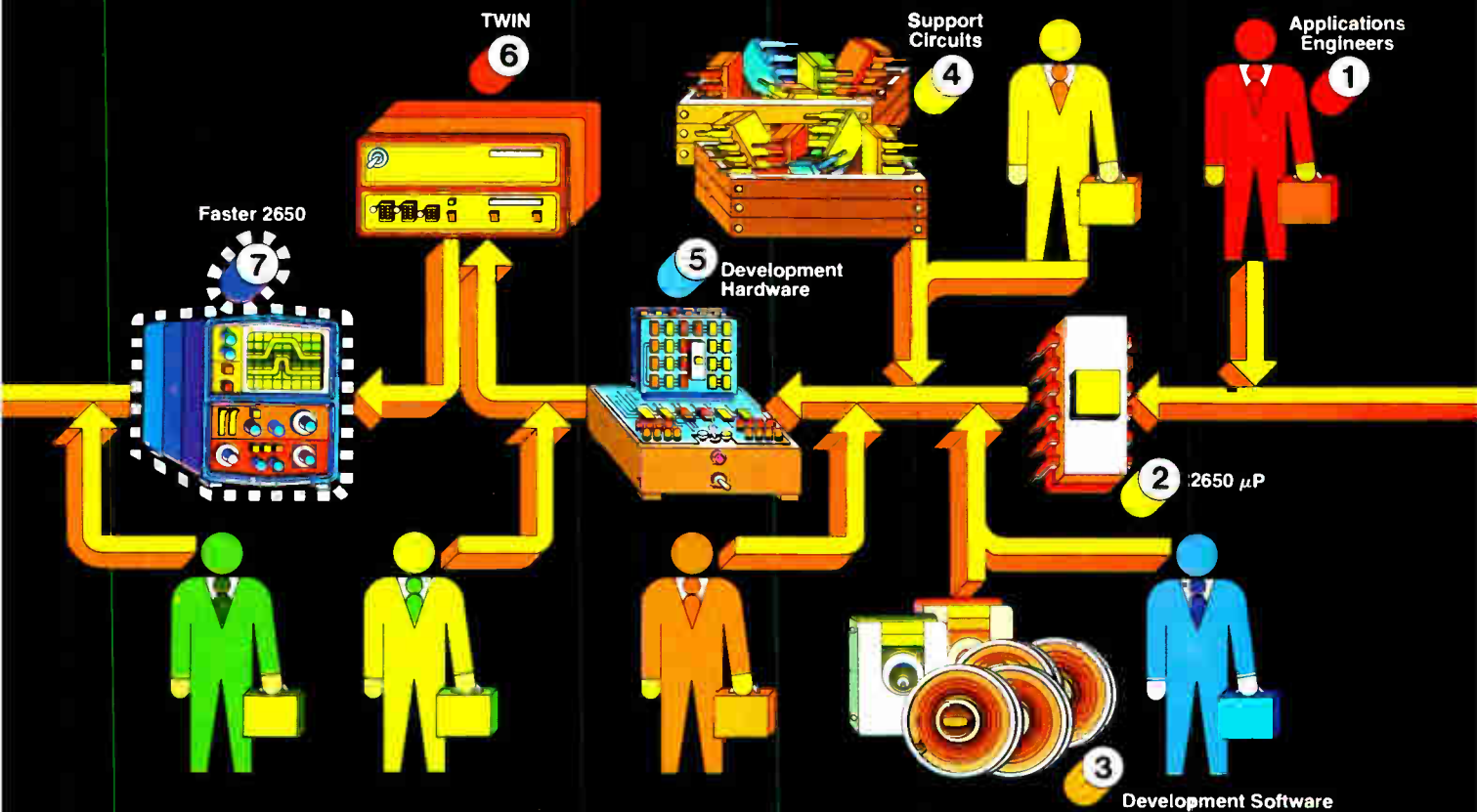
Full support of customer and product is the key to ease of development with the 2650. Applications engineers in the U.S. and abroad are at your beck and call at every stage. Software for almost anyone's requirements and machines. Development hardware is versatile and inexpensive. All circuits are multi-sourced.

Flow Chart: How to travel safely and quickly from spec sheet to your μ C.

- 1 Applications Engineers — in the field now, more coming. Specific assistance to you is available around the USA, and in Belgium, Holland, Germany, France, Sweden, Britain, Italy, etc.
- 2 Multi-sourced 2650 — available in any quantity from Signetics, at the unprecedented low price of \$21.50. Also available from AMS and Philips, and from Signetics' authorized distributors.

- 3 Development Software — includes the PL μ S, an extremely efficient High Level Language (compiler) that reduces programming effort and cuts development time. ANSI standard Fortran IV executes on most machines without alteration. 2650AS1000 1100 Assembler and 2650SM1000/1100 Simulator are available in both 32- and 16-bit, on GE and NCSS time-sharing.

- 4 Multi-sourced Support Circuits — You'll need MOS and/or Bipolar Memories, Interface and Logic. Signetics has *everything* for a complete system. Back up any item from other sources. Coming soon from Signetics are: Programmable Peripheral Interface and Communications Interface, A-D Converters, Synchronous Data Link Controller, 16k NMOS & Bipolar ROMs, 4k & 8k NMOS EROMs, and 8k Bipolar PROMs.



makes the easiest-to-develop microcomputer.

- 5** Development Hardware — Design/develop/prototype with a variety of cost/capability levels of hardware support. Including prototyping cards and kits, smart typewriter demo card, 4k-byte RAM card, and more. Applications help if you need it.
- 6** TWIN With Floppy Disks — “crashproofs” your system checkout. With DOS, Resident Assembler, and Text Editor. You develop programs and circuits together in an actual system environment with TWICE (TestWare In Circuit Emulator). PROM programming, too.
- 7** Over 30% Faster 2650 — By the time you’ve proven out your μC , you’ll have available a faster 2650 if you want it. Uses the same software. For still higher speeds, call Signetics Bipolar Microprocessor Marketing about our 2650 emulator using 3000 series μP .

You go from gleam-in-your-eye to proven prototype in less time for less cost, and the μC you develop is easier and cheaper to produce in quantity, when you start with the 2650. Start now by mailing the coupon.

Attach this to your letterhead for fast response.

Send me complete 2650 short form catalog.

Have a Field Applications Engineer call me for appointment.

My need is: immediate 6 months information only

My application is _____

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Title _____

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Subassemblies

Revamped hybrid line costs more

Citing price-yield ratios, Datel offers family of higher-performance devices

Within the last six months, the prices of commercial hybrid data converters have been dropping steadily. Bucking this trend, Datel Systems Inc. is replacing its low-cost devices with an expanded line of improved-performance units at much higher prices [*Electronics*, March 18, p. 44].

Only last September, the Boston-area firm started up its new hybrid facility with a trio of eye-opening products [*Electronics*, Sept. 18, 1975, p. 117]. This introductory HY series included a pair of self-contained 12-bit digital-to-analog converters sell-



ing for only \$29 each and a 12-bit analog-to-digital converter, also self-contained, for \$79.

These devices are no longer available. Instead, Datel is offering slightly superior pin-for-pin replacements, in addition to 15 brand-new models. In all cases, prices are at least 50% higher than those of the original products.

"Extremely low pricing placed a heavy burden on yield requirements, while customer requests for extended-temperature operation and metal-case packaging added further demands," a company

spokesman says. As a result, Datel's cost-to-yield ratios have been less than desirable, and the firm has decided to make a fresh start with a restructured product family.

There are 18 new devices in all—12 d-a converters and six a-d converters. Every model is a self-contained 12-bit unit, requiring no out-board components at all, not even a voltage reference. The converters, which are packaged in hermetically sealed glass or metal cases, are available in a choice of operating temperature ranges: 0°C to 70°C, -25°C to +85°C, or -55°C to +125°C.

All the new series HZ d-a converters settle to half a least significant bit within 3 microseconds. Linearity error is ± 0.5 LSB for binary versions, ± 0.25 LSB for binary-coded-decimal versions. Additionally, the units can be obtained with complementary-binary or complementary-BCD coding at no extra charge.

In quantities of 1-9, price ranges from \$49-\$175 each for converters

World's first 4-channel compact...



Dimensions (h x w x d) 154 x 316 x 410 mm. Weight just 3.5 kg.

having a gain temperature coefficient of 20 ppm/°C. Also being offered, for \$150 each, are binary and BCD units that provide a gain-temperature coefficient of 10 ppm/°C over the range of -25°C to +85°C.

All six a-d converters are successive-approximation binary units whose linearity error is ±0.5 LSB. Besides being pin-programable, they offer both parallel and serial output formats. Their gain temperature coefficient is 20 ppm/°C.

The three HZ versions, which have a conversion time of 8 μs, sell for \$149-\$215 each in lots of 1-9. The three HX models, with a conversion time of 20 μs, range in price from \$119 to \$185 for 1-9.

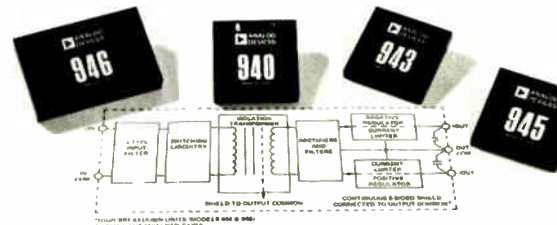
Except for military-temperature-range models, delivery is approximately 4-6 weeks for the d-a converters, 8-10 weeks for the a-d converters. For all military versions, delivery time is about 12 weeks.

Datel Systems Inc., 1020 Turnpike St., Canton, Mass. 02021. Phone (617) 828-8000 [381]

Analog Devices invades dc-dc converter arena

As a rule, manufacturers of encapsulated modules, like operational amplifiers and data-conversion devices, also sell the power supplies for these products, permitting customers to buy an entire complement of modules from one source. One of the leading module houses, Analog Devices, which claims to be the largest direct supplier of modular power supplies to end users, is now marketing a full line of dc-to-dc converters, too. The initial seven models are pin-compatible with competitive units.

"The dc-dc converter market is now approximately \$3 million and expanding at 20% a year," points out Fred Pouliot, marketing manager for analog modules. "Our improved performance, smaller size, and continuous (six-sided) shielding, coupled with an aggressive pricing strategy, will enable us to



achieve market leadership in the next 18 months," claims Pouliot.

Besides current-limiting, each of the seven models provides line and load regulation of ±0.05% maximum. All include a π-type input filter to reduce reflected input ripple current, and all can operate over the temperature range of -25°C to +71°C without power derating. At full load, minimum efficiency ranges from 48% to 62%, depending on the model.

Models 940, 941, 942, 943, and 945 are housed in a 2-by-2-by-0.375-inch package and have a continuous breakdown voltage rating of 500 v dc. Models 944 and 946 come in 3-by-2-by-0.6-in. packages with a

...with amazing triggering facilities

There's never been a spec. like this before.

- four 50 MHz channels plus
- two differentials (simultaneous display if needed) plus
- fully independent triggering of main and delayed time bases meaning
- main time base triggering on any of the four channels + composite + external + line and
- delayed triggering on any four channels plus composite.
- Moreover it all comes in a compact 9,6 kg construction.

So now you can display just about anything, for example a magnified view of any delayed section of a signal even when it is not directly related to the main time reference!

Easier to use too

One look at the PM 3244's front panel tells you everything. Controls are logically grouped and positioned to fall naturally to hand. So you study the screen and not the 'scope.

One look inside will tell you how it's done - with a Philips technique

called cold switching. This means that the actual switching is performed on the boards with simple DC signals from the controls. The removal of mechanical connections eliminates layout and electrical design restraints, which in turn allows the PC boards to be designed for optimum layouts at all frequencies and for all facilities. Reliability is therefore greater, both mechanically and electrically, and servicing is made easier.

Another Philips development gives you remarkable low 29 W consumption which eliminates the need for ventilation fans and holes. It also boosts reliability and allows the PM 3244 to work from a battery pack as well as just about any voltage/frequency combination. So the world's first 4-channel compact lives up to its name. Going anywhere that 4 channels are needed. Which in today's digital world means just about everywhere.

Find out more by contacting Philips or utilize our toll free HOT LINE number 800 645-3043. New York State residents call (516) 921-8880 collect.

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Circle 204 on reader service card 205

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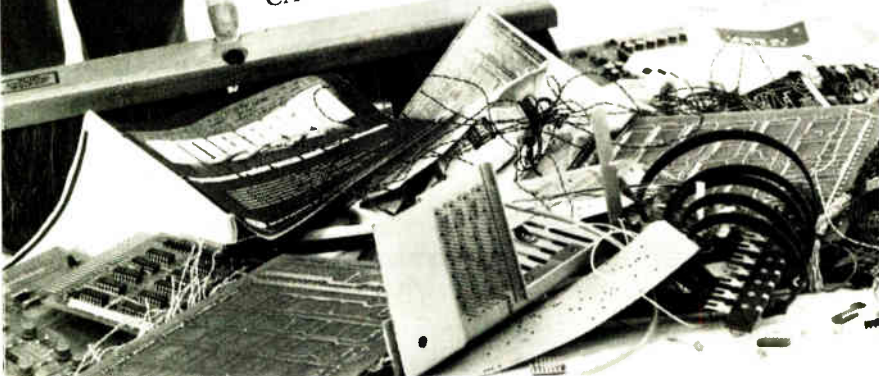
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New products

breakdown rating that is specified at 8,000 v dc.

Output voltage is 5, ±12, or ±15 v dc. For the 5-v units, output current is 600 or 1,000 milliamperes, and peak-to-peak output noise voltage is 50 millivolts at a 20-megahertz bandwidth. For the dual-output models, output current is ±60 or ±150 mA, and the 20-MHz output noise voltage is 35 mV pk-pk. Five of the units operate from a nominal input of 5 v dc, while the other two accept a nominal input of 28 v dc.

In quantities of one to nine, price ranges from \$62 to \$79. All models are available from stock.

Analog Devices Inc., P.O. Box 280, Route 1 Industrial Park, Norwood, Mass. 02062. Phone (617) 329-4700 [382]

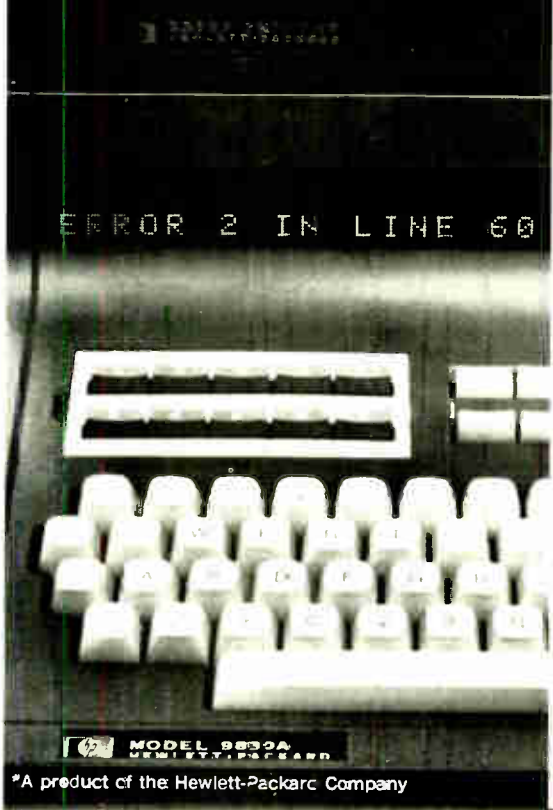
50-W switching supplies sell for less than \$200

Until recently, frame-type switching power supplies were economically feasible only for power ratings of at least several hundred watts. But new low-cost high-performance switching power transistors are steadily changing this situation. A young firm, Etatech Inc. of Placentia, Calif., is offering a family of seven switching supplies with ratings of 50 to 60 watts, priced at only \$175 each. In lots of 100, the price drops to \$138 each. Delivery time is two to four weeks for 5-v models, and six to eight weeks for all others. Adjustable output voltage and battery backup input are available as options.





These series B units, which measure 4 7/8 by 7 by 1 3/4 inches and weigh 2 pounds, can operate from line inputs of 95 to 130 volts root



HP9830A USERS: HAS THIS EVER HAPPENED TO YOU?



Memory overflow problems can now be a thing of the past. The EM-30 Extended Memory System eliminates the necessity of re-designing your programs as a result of ERROR 2.

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Infotek Systems

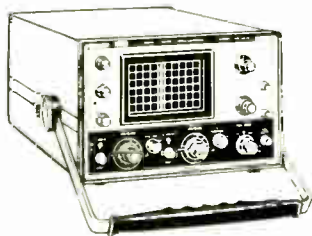
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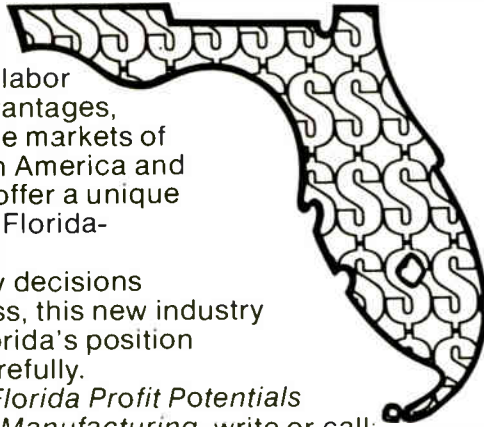
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World Radio History

New products

mean square at 47 to 440 hertz. Remote sensing, automatic recovery, and protection against overloads, short circuits, and overvoltages are standard.

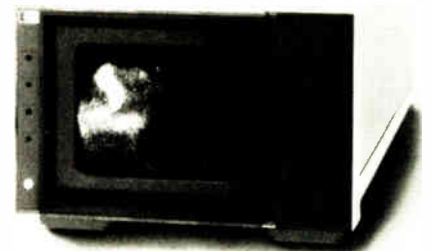
The seven models cover the output-voltage range of 2 to 60 v dc, with a minimum power-transfer efficiency of 75%. Typical output current is 10 amperes for the 2-v model, 10 A for the 5-v model, 5 A for the 12-v model, 4 A for the 15-v model, 2.25 A for the 28-v model, 1.5 A for the 48-v model, and 1.25 A for the 60-v model.

For all units, both line and load regulations are 10 millivolts maximum. Additionally, the series B models offer long life—their mean time before failure is specified as 70,000 hours, for a baseplate temperature of 80 C.

Estatech Inc., 187-M West Orangethorpe Ave., Placentia, Calif. 92670. Phone (714) 996-0981 [383]

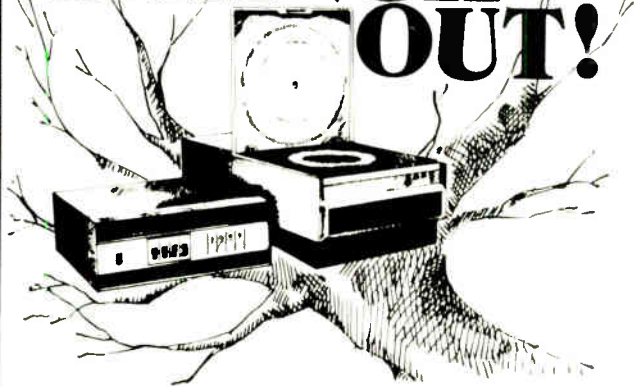
CRT display has maximum spot diameter of 0.2 mm

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Electronics/April 15, 1976

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Get "inside" your 8080 breadboards and know where you are every step of the way —

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The MM80 provides a complete control and test center for any system under test. Five scope probe points let you trigger on MI, sync, $\phi 1$, $\phi 2$ signals and specific address references. RAM diagnostic programs are provided. The LED display provides complete processor status information.

For the complete inside story on Ramtek's new MM80, call or write

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THE GRAPHIC DISPLAY COMPANY

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Send for bulletin TAF24

DATA DELAY DEVICES
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Circle 256 on reader service card

Circle 257 on reader service card 209

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Patent applied for

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OTHER OUTSTANDING FEATURES:

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New products

available in a version (Option 330) that is listed by Underwriters Laboratories in accordance with UL544. The display sells for \$1,500.

Hewlett-Packard Co., 1501 Page Mill Rd., Palo Alto, Calif. 94304 [384]

Low-noise chopper amplifier drifts less than 2 μV/year

The model MP221 low-level chopper amplifier is a low-noise differential device with an input impedance of 10⁹ ohms, an input bias current (in the noninverting mode) of only ±20 picoamperes, and an offset voltage drift of less than 1 microvolt per month or 2 μV per year. Intended for the amplification of the low-level signals that are generated by such transducers as load cells, thermocouples, and strain gages, the MP221 has a common-mode rejection ratio of 140 dB and an input common-mode voltage rating of 0.5 v. Housed in a compact, shielded metal case, the amplifier sells for \$64 in small quantities.

Analogic, Audubon Rd., Wakefield, Mass. 01880. Phone (617) 246-0300 [386]

TOPICS Subassemblies

Burr-Brown, Tucson, Ariz., has announced price cuts of up to 52% in its DAC80 and ADC80 line of 12-bit d-a and a-d converters. In hundreds, the ADC80 has been reduced to \$47.50 and the DAC80 to \$19.50. . . . **Analogic Corp., Wakefield, Mass.**, has cut the price of its MP2600 12-bit binary, 3½-digit BCD a-d converter from \$149 to \$89 for small quantities. . . . **Analog Devices Inc., Norwood, Mass.**, is offering the complete line of thin-film resistor networks made by its Resistor Products division in chip form. The networks are available in two accuracy grades, or they can be supplied untrimmed to allow active trimming after assembly. They are offered diced, scribed, in unbroken plate form, or as inked matrices.



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New products

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Tester handles 96-pin devices

Computer-controlled 20-MHz system does functional and ac and dc parametric tests

Even as the test-equipment industry is adjusting to the relatively new 48-to-50-pin standard on large-scale-integrated logic devices, designers of computer systems are pushing hard toward the next generation—very-large-scale-integrated (VLSI) circuits with 96 to 100 pins. Taking their cue from computers now under development in the U.S. and Japan, engineers at E-H Research Laboratories Inc., have completed development of a 96-pin, 20-megahertz Super LSI tester, the EH4700.

Earl M. Olsen, director of systems marketing, explains that the 4700 series is a family of modular test systems capable of performing dc and ac parametric, computer-rate functional, and real-time functional tests during a single device insertion. Like earlier systems, they can be used for either engineering or production tests of printed-circuit boards, logic arrays, and modules as well as VLSI circuits made with MOS, diode-transistor, transistor-transistor, and emitter-coupled logic, as well as Schottky TTL.

Ac parametric measurements are made on a single-shot basis. The dual dc measurement module will make current and voltage measure-

ments in a single parametric test. An IBM 1130 computer controls the system for both testing and data acquisition.

The dc package includes six voltage-forcing supplies and one current-forcing supply. These supplies are connected to a dc matrix that allows any supply to drive any of 96 fixture pins. The pins are driven by Kelvin twisted pairs and a driven guard. "The driven guard is important for the dc power and sense," Olsen says, "because it reduces the capacitance between power and sense lines and ground. This reduces the capacitance that must be charged and speeds dc tests, particularly for low-level measurements." The dc-measurement module can measure the current on any voltage-driven pin and the voltage on any pin.

The most important part of the 4700 is its test fixture, which includes 96 pulser/sensors—one for each pin. The pulsers require only 1.5 nanoseconds to swing the 800 millivolts of an ECL-level change and can swing 10 volts in 5 ns. The pulsers are back-matched 93-ohm drivers with a dynamic range that extends from -2 v to +8 v. Their programed levels are accurate to within 1%.

The system has two pairs of driving levels and two pairs of thresholds. The levels and thresholds at each pin are selectable under program control. Because of its sensor-per-pin configuration, along with its high-speed word generator and high-speed comparator, the 4700 can perform real-time functional testing at speeds up to 20 MHz.

Price of the tester ranges from \$700,000 to \$800,000.

E-H Research Laboratories Inc., 515 Eleventh St., Oakland, Calif. 94607. [391]

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New products

Design Engineers' Electronic Components Conference later this month in San Francisco. Called Q-Chek, the tester can check out cables for continuity, shorts, and crossed wiring between terminations. It can be used as a tool by mobile repairmen, or in original-equipment-manufacturer operations such as incoming inspection and quality assurance.

One model, the QC1001, can test more than 180 combinations of standard audio terminations, including commercial phone jacks, telephone- and military-type plugs, phonograph plugs, premium-quality connectors, and European DIN-type connectors. A second model has seven adapters, extending its testing range up to as many as 350 combinations.

Operating the cable tester is simple. The user just opens the cover, connects the cables to be checked to the proper connectors, and then depresses a set of programming pushbutton switches in sequence. An array of lighted indicators, then displays the condition of the cable.

Switchcraft Inc., 5555 North Elston Ave., Chicago, Ill. 60630 [393]

Reel-to-reel handler heats devices, not carrier tape

Large-volume users of semiconductor devices, such as the automotive industry, are finding as many as one out of four components fail incoming inspection when tested at 85°C. Most of these same parts pass the tests at room temperature. This situation has created a need for fast, high-temperature testing of reels of tape-fed transistors.

Unfortunately, if a portion of the paper or Mylar carrier tape (see

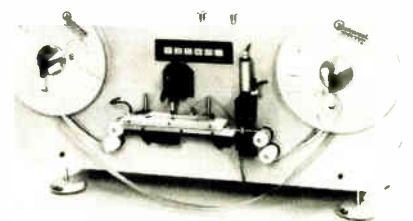


photo) is heated to the desired test temperature, the adhesive holding the semiconductor device to the tape can soften, causing the device to skew from its testing position. A reel-to-reel handler for the inspection and testing of transistors and silicon controlled rectifiers, the Lorlin 640T, has an optional mechanism that directs hot air at the devices so as to avoid heating the carrier tape. This eliminates the need for separate test ovens and prevents skewing. The new handler, which is among the first to handle three-leaded devices on tape, has a sense circuit that determines the existence and position of a transistor and high-speed operation.

The 640T can move 45,000 components an hour if they require no heating and zero test time. The actual throughput, of course, depends upon the test time required for the particular device, its thermal mass, and the temperature to which it is to be heated. Throughputs of 10,000 components per hour are realizable when testing transistors at 125°C.

A light-source/photodiode sensor is used to determine the position of each part, allowing greater accuracy and improving device-contacting. Parts missing from the tape or parts slightly out of position do not affect operation, because a test cycle will only begin when the sensor detects a component. The price of the machine varies from \$8,000 to \$14,000 depending upon options. Delivery time is 60 days.

Lorlin Industries Inc., Precision Rd., Danbury, Conn. 06810. Phone (203) 744-0096 [394]

Unit pinpoints shorts on printed-circuit boards

Many testers can determine that a short circuit exists between two or more points on a printed-circuit board. The problem is to determine the short's exact physical location. Short-Stop is an instrument designed to solve this problem. It drives a train of current pulses into the shorted node and allows the op-

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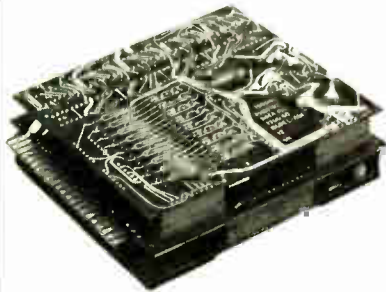
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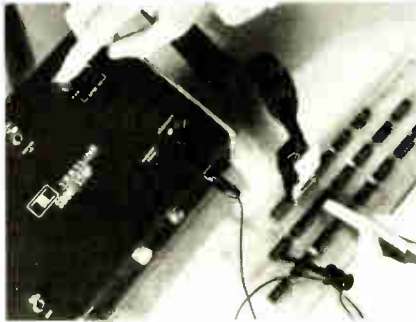
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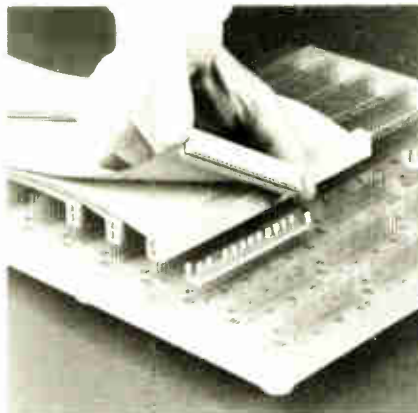


erator to trace the current with a probe that senses the magnetic field generated by the pulses. A slightly more complex tester called Short-Stop II is also able to determine which component is contributing a faulty input to a wired-OR data bus. The patented current-detecting probe used in both units responds to currents as low as 1 milliampere. Short-Stop sells for \$495, and Short-Stop II is priced at \$675.

Testline, 1625 White Drive, Titusville, Fla. 32780. Phone Roger Boatman at (305) 267-7212 [395]

Backplane I/O connector handles up to 50 pins

A backplane input/output connector is designed to allow connections directly over wrapped-wire pins on standard 0.1-by-0.2-inch grid spacings. The Scotchflex 50-position socket connector 3307 incorporates a polarizing key to ensure accurate positioning. The 3307 is actually a connector system which includes the socket, a strain-relief clip, a keying header, the polarizing key, and a



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New products

locator plate. The connector will mate with 26- and 28-gage solid or stranded wire and with 30-gage solid wire.

3M Co., Dept. EP5-31, P.O. Box 33600, St. Paul, Minn. 55133. Att: Dan Noonkesser [396]

System performs in-circuit and functional testing

The microprocessor-controlled Troubleshooter 400 is a printed-circuit-board test system that provides analog and digital fault analysis down to the component level. The in-circuit tester also provides extensive functional test capabilities. Its microprocessor allows the system's software to handle many functions that had been hard-wired. Thus the system is flexible enough to allow on-line generation and editing of



test programs, the compilation of such management data as statistics on component failures, and the automatic generation of test programs from a list of components.

The system includes a cathode-ray-tube terminal and keyboard for program preparation. During testing, the CRT provides operator instructions (such as to adjust a potentiometer) and data display. Mass program storage is by means of a floppy disk system, and a solid-state memory holds the test programs that are in use.

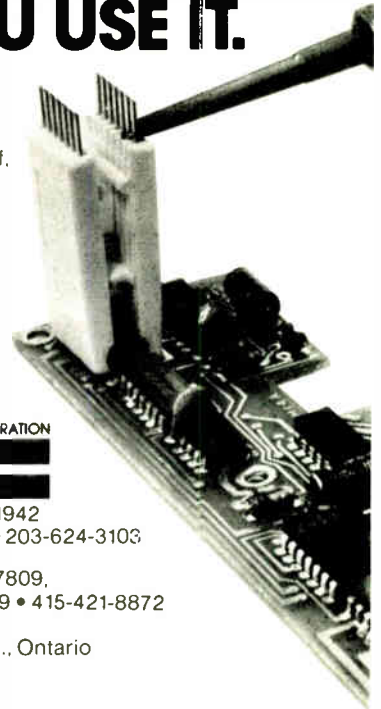
Because the Troubleshooter 400 has a bus structure, many optional accessories can be added easily. Pricing on the system starts at \$47,950; delivery time is 90 days.

Zehntel Inc., 2440 Stanwell Dr., Concord, Calif. 94520. Phone Craig Pynn at (415) 676-4200 [397]

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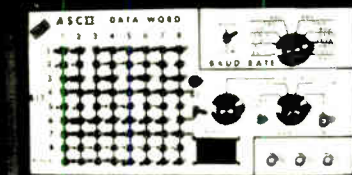
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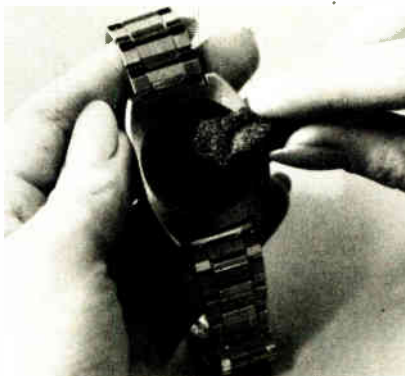
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steel wool and pencil erasers. They are available in sheets as large as 12 inches by 20 in. Delivery of the sheets is from stock.

3M Co., Visual Products Div., Dept VP5-97, P.O. Box 33686, St. Paul, Minn. 55133 [476]

A **silver-filled epoxy adhesive** and coating formulation is useful in microwave shielding, pc-board repair, and as a cold solder. The material has a volume resistivity of less than 10^{-4} ohm-centimeters. ECR-4100 is available in preweighed kits ranging from a 2-gram dual pack up to a 2-pound kit.

Formulated Resins Inc., P. O. Box 508, Greenville, R. I. 02828 [477]



Injection-moldable magnetic compounds made by combining a thermoplastic resin with predetermined loadings of ferrites has certain advantages over ceramic magnets. Chief among these are ease of fabrication of complex shapes, and the elimination of fragile preforms and secondary operations needed in the production of ceramic magnets. Magnecomp "A" is the first compound to become available. It has a maximum B-H product of 0.9×10^6 gauss-oersteds and is intended for such applications as indicators and small motors.

LNP Corp., 412 King St., Malvern, Pa. 19355 [478]

Bonding to Teflon and other fluorocarbon plastics is always a problem because of their reluctance to adhere to anything. So before cementing, encapsulating, or soldering Teflon-coated wire or wires coated with such other fluorocarbons as Fluon, Kel-F, Halon, and Kynar, their surfaces may be modified by being pretreated with Bondaid etchant. This stabilized dispersion of metallic sodium makes the plastics receptive to adhesives for bonding. Bondaid is offered in 1-ounce, 2-oz., half-pint, and pint bottles.

W. S. Shamban & Co., 11543 W. Olympic Blvd., Los Angeles, Calif. 90064 [479]

Insulating epoxy adhesives with volume resistivities of 10^{15} ohm-centimeters and 10^{16} ohm-cm resist moisture and bind strongly. The one-part thixotropic formulations cure in 1 hour at 100°C . Type 13 is a general-purpose adhesive, type 14 conducts heat rapidly, and type 15 has high peel strength. Type 14 has a volume resistivity of 10^{16} ohm-cm; the other two have 10^{15} ohm-cm. Available from stock, the adhesives sell for \$15 a pound.

Transene Co., Route One, Rowley, Mass. 01969 [480]

Rare-earth/cobalt permanent magnets with energy products in excess of 18 megagauss-oersteds have exceptional long-term stability.

Ceramic Magnetics Inc., 87 Fairfield Rd., Fairfield, N. J. 07006 [361]

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New literature

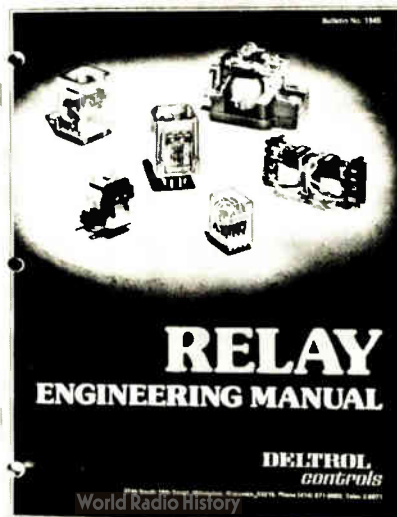
Chart recorders. Four basic strip-chart recorder measuring systems are explained in a 24-page catalog from Esterline Angus Instrument Corp., P. O. Box 24000, Indianapolis, Inc. 46224. Catalog number C200 covers permanent-magnet/moving-coil, electro-dynamometer, pressure-and-vacuum, and position-and-motion systems. Circle reader service number 421.

Snap-action switches. Technical bulletin No. 90 discusses important features of nine lines of snap-action switches made by Control Switch, a Cutler-Hammer Co., 1420 Delmar Dr., Folcroft, Pa. 19032 [422]

LED lamps. A reference set of nine data sheets describes the full line of light-emitting-diode lamps and panel-mounting hardware offered by Chicago Miniature Lamp, 4433 N. Ravenswood Ave., Chicago, Ill. 60640. The sheets show features, optical specifications, dimensional drawings, and electrical characteristics. Each data sheet includes five curves including one of relative intensity versus viewing angle. [423]

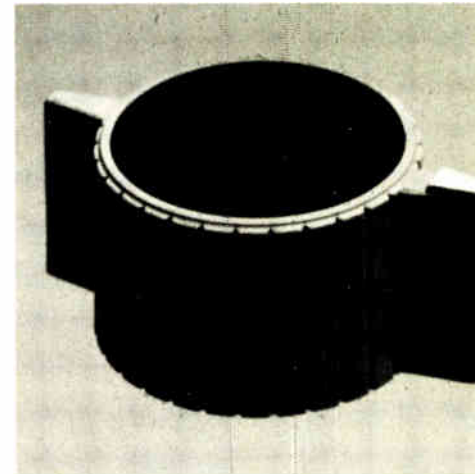
Coil winders. A 12-page catalog describes a line of numerically controlled coil winders. Included are photos and descriptions of seven machines made by Eubanks Engineering Co., 225 West Duarte Rd., Monrovia, Calif. 91016 [424]

Relays. General-purpose, power, and specialty relays are covered in a 32-page Relay Engineering Manual put out by Deltrol Controls, 2745 So. 19 St., Milwaukee, Wis. 53215.



Bulletin 1845 provides data on more than 40 relay types from latching units to antenna-switching devices. [425]

Control knobs. A 16-page catalog covers a wide variety of control knobs, molded of ABS plastic, and offered with aluminum shaft bushings in three sizes: 0.125, 0.1875, and 0.25 inch. Available in four



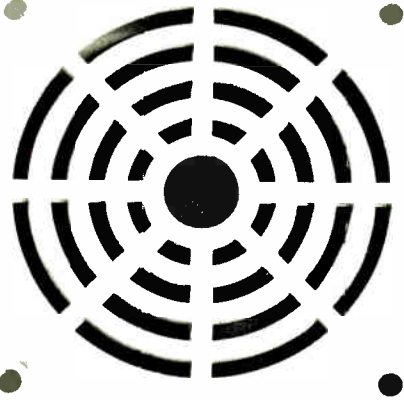
standard colors—black, gray, green, and blue—the knobs can be supplied with textured tops, metal inlays, skirts, pointers, and various indexing marks. The catalog can be obtained from Radial Controls, 2555 East 55 Pl., Indianapolis, Ind. 46220 [426]

True-rms ammeters. A pair of instrument bulletins provide technical data, prices, and features on a line of portable and edgewise panel true-rms ammeters. Information is provided on a number of analog meters with ranges from 25 microamperes to 1,000 amperes. Write to Gerry Frank, Greibach Instrument Service Inc., 25 Dock St., Mount Vernon, N. Y. 10550 [427]

Meters. A 30-page catalog of meters, indicators, and instruments is offered by Emico, 123 N. Main St., Dublin, Pa. 18917. Specifications, a mechanical drawing, a photograph, and a description of its outstanding characteristics are provided for each model in the catalog. [428]

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Circle 264 on reader service card

“Business is a *lot* better:

Seven things for management to worry about in the improving Electronics Technology Marketplace.

1. *Worry about the business cycle running your business*

In May, 1973, we published the first editorial in this series. The headline was “*Advertise? I can’t even deliver the orders I’ve booked*”, and the ad contained nine things to consider about advertising in a *boom*. In December, 1974, the sixth ad in this series was headed “*Business is lousy—let’s cut the advertising budget*”, and it offered seven things to consider about advertising in a *bust*. In May, 1975, the seventh ad stated that a boom was on the way, and suggested seven ways to prepare for it. Now it is March of 1976, and I have just been informed of two companies that are cutting their advertising because they have more orders than they can handle. I was tempted to headline this ad “*Here we go again!*” and offer “*one sure way to make this business cycle worse than the last*”. Because there *is* one sure way—and that’s to *let the business cycle run your business*.

2. *Worry about lousy forecasting*

One of the ways to let the cycle run your business is to let it influence your forecasting. We all have the same problem: In boom years, our forecasting gets increasingly bullish, and our visions of market share lose touch with reality. The result is that our forecasting, rather than helping smooth the business cycle, actually *aggravates* it. That’s because when the bust comes, it comes off of a peak that we have made artificially high, so we have farther to fall. Then all through the down time we continue to forecast gloom and doom so we are never ready for the recovery.

Let’s face it: *these cycles will continue*. They may even be shorter and sharper. The trick is to run the business steadily and *consistently* in spite of them. And good forecasting—forecasting that tries very hard to emphasize the constants and ignore the variables of the moment—is required. Good forecasting recognizes that we’re lousy at forecasting. Therefore we need to plan for various contingencies as well as expectations. Good planning isn’t predicting the future. It’s being ready for *any* future.

3. *Worry about technology change*

The next few years will bring dramatic changes in technology. The real impact of microprocessors, semiconductor memory, and other large-scale integrated circuitry is still in front of us. It will change the way we do business. It will change the fundamental economics of every electronic product, and every product that *could* be electronic. It will ruin companies that have not sharpened their *marketing* skills. It will change the competitive balance in many markets, and will force us to *change the way we sell*. Our changing technologies will bring us both opportunity and danger. Opportunity for those who develop a thorough understanding of technology trends, and apply that understanding in a *consistent* way to the fundamentals of their business. Danger for those who keep doing things the same old way, and let themselves be blown about by the winds of the marketplace.

4. *Worry about financial planning*

Electronics used to be a components-based, product-engineering, labor-intensive, assembly business. It is becoming a *materials-based, systems-engineering, capital-intensive, batch-processing* business. The increasing capital requirements of this new kind of electronics business are going to tax the ability to finance our growth. And outside money will be more difficult to get because the financial community is tired of our business cycles. (Bankers are shell-shocked from the recession and smarting under well-deserved criticism. The go-go banking fad is over.) *Consistency* of purpose in financial management—rather than overreaction to short-term conditions—is now essential.

Let's start worrying."

5. Worry about positioning

As technology changes and market forces become more complex, it becomes increasingly important to have a carefully considered "position" for your company and each of its product lines. Positioning errors will be increasingly expensive, and the fundamental questions like "What should our business be?" and "Can we really achieve that?" and "How will the competition react?" should be answered precisely. Once you've decided the positions, make sure you don't hide them from the marketplace. Use advertising—and use it steadily and consistently—to drive home your position and preempt your competitors.

6. Worry about market development

Let's not lose sight of the fact that one of the best ways to smooth out the business cycle is to broaden our markets. There are new markets waiting to be sold. There are still old ways of doing things that are waiting to be converted to electronics. Economics are on our side. Our new technologies are bringing new applications into our range. If we are going to achieve real growth instead of inventory bubbles", and mitigate the effects of the next downturn, our market development programs must be *consistent* in purpose, funding, and management priority.

7. Worry about how to sell up to management

The selling proposition is changing. In the old days, if you sold something like a connector or capacitor or relay, you could get the job done by calling on design engineers, buyers, and standards people. Unless it was a big deal—in which case it helped a lot to have *management* on your side. But now the market is being made—and the economic and technical decisions are being forced—by semiconductor technology. *And that technology is being sold at the highest levels of engineering management.* If you are not selling your product there, too, you will wind up being an afterthought—competing on price and specs in a game someone else controls. The message is clear: You *must* find more effective ways to sell up—to communicate with management. Your salesmen will have trouble doing it. Your top management can't do it and still run the business. Your advertising *can* do it. In fact, it is the one thing your advertising *must* do, even if it *doesn't do anything else.*

A few words in closing.

In looking back over what I've written, I find this is an advertisement about *consistency*. Consistency in planning, in forecasting, in selling, in management objectives. As a matter of fact, that's what this whole series has been about—consistency in the face of short-term business conditions.

To carry this theme into advertising, there *never* was a great advertising

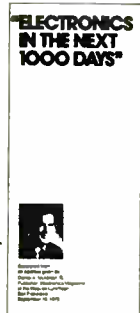
campaign that wasn't *consistent*—consistent in what it said, consistent in how often it appeared, and consistent as to *where* it appeared. And on that note:

- If you are going to use advertising to help you develop new markets, please remember that *Electronics* is the *premier* market development medium, and the only truly *international* medium.
- If you are going to use advertising for positioning, and to sell up, please remember that *Electronics* is *by far* the best-read and most-preferred publication among *engineering managers*.



Daniel A. McMillan III
Publisher

I'm consistent in at least one thing—I never get around to having speeches printed up until a while after I make them—if ever. This is one from last September's WESCON. It's about some of the same things as this ad. If you want a copy, send the coupon.



To: Dan McMillan, Publisher
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1221 Avenue of the Americas
New York, N.Y. 10020

Please send me a copy of "Electronics in the Next 1000 Days."

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A universal data collection system with these **standard** features;

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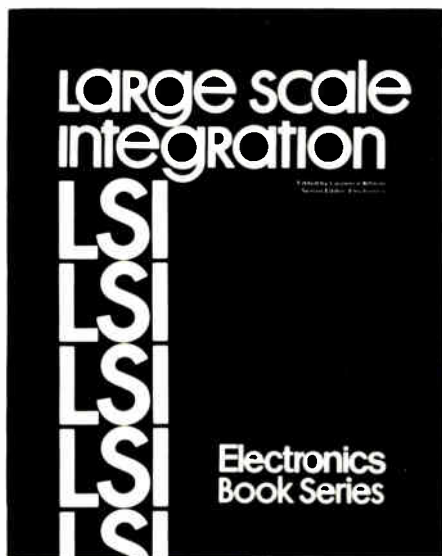
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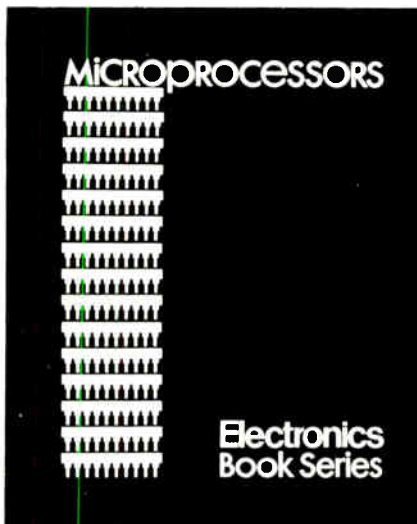
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Payment enclosed Bill firm
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Electronics Buyers' Guide

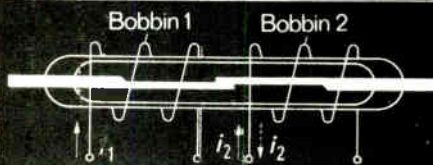
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a semi-hard magnetic alloy with rectangular hysteresis loop for impulse controlled self latching relays.



Properties:

- high remanence
- adjustable coercitive force

VACUZET 200 258 655 923

H _c	A/cm	15	30	50	75
B _r	T	1.5	1.45	1.45	1.25
B _r /B ₁₀₀	%	ca. 90			

For data sheet and further information apply to

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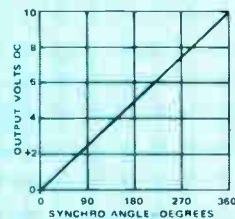
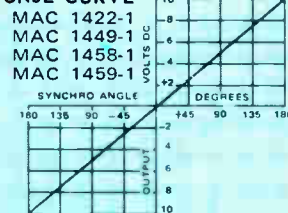
SOLID STATE 3 WIRE SYNCHRO TO LINEAR D.C. CONVERTER



FEATURES:

- Develops a DC output voltage linearly proportional to a synchro angle over a $\pm 180^\circ$ range.
- Completely solid state with all of the inherent advantages over a mechanical system such as:
 - High reliability (since there are no moving parts)
 - Light weight—6 ozs.
 - Small size
 - All units hermetically sealed

RESPONSE CURVE



MAC 1460-1
MAC 1461-1

- Wide temperature range operation
- Output short circuit protected
- Three wire inputs isolated from ground
- Package size may be altered at no extra cost
- Units can be altered to accept different line to line voltages or different operating frequencies at no extra cost
- Not affected by reference voltage or power supply variations.

UNIT	MAC 1422-1	MAC 1449-1	MAC 1458-1	MAC 1459-1	MAC 1460-1	MAC 1461-1
TRANSFER EQUATION	$\pm 1V/18^\circ$	$\pm 1V/18^\circ$	$\pm 1V/18^\circ$	$\pm 1V/18^\circ$	$+1V/36^\circ$	$+1V/36^\circ$
ACCURACY (+25°C)	½%	½%	½%	½%	½%	½%
ACCURACY (-25°C+85°C)	1%	1%	1%	1%	1%	1%
L - L SYNCHRO INPUT (VRMS)	11.8	90	11.8	90	11.8	90
FREQUENCY (Hz)	400	400	60	60	400	400
FULL SCALE OUTPUT	$\pm 10V$	$\pm 10V$	$\pm 10V$	$\pm 10V$	$+10V$	$+10V$
OUTPUT IMPEDANCE	$<1\Omega$	$<1\Omega$	$<1\Omega$	$<1\Omega$	$<1\Omega$	$<1\Omega$
L - L INPUT IMPEDANCE	$>10K$	$>30K$	$>2K$	$>10K$	$>10K$	$>30K$
REFERENCE VOLTAGE (VRMS)	26	115	26	115	26	115
OPERATING TEMP. °C	-25 - +85	-25 - +85	-25 - +85	-25 - +85	-25 - +85	-25 - +85
D.C. SUPPLY	$\pm 15V$	$\pm 15V$	$\pm 15V$	$\pm 15V$	$\pm 15V$	$\pm 15V$
D.C. SUPPLY CURRENT	$\pm 75MA$	$\pm 75MA$	$\pm 75MA$	$\pm 75MA$	$\pm 75MA$	$\pm 75MA$
BANDWIDTH	10Hz	10Hz	DPT.	DPT.	10Hz	10Hz
WEIGHT	6 oz.	6 oz.	6 oz.	8 oz.	6 oz.	6 oz.
SIZE	3.6x2.5x0.6	3.6x2.5x0.6	3.6x3.0x0.6	3.6x3.0x1.0	3.6x2.5x0.6	3.6x2.5x0.6

A.C. LINE REGULATION

A new method has been developed which allows us to provide a low distortion highly regulated AC waveform without using tuned circuits or solid state active filters of any kind.

The result is a frequency independent AC output regulated to 0.1% for line and load with greater than 20% line variations over a wide temperature range.

FEATURES:

- 0.1% total line and load regulation
- Independent of $\pm 20\%$ frequency fluctuation
- 1 watt output
- Extremely small size
- Isolation between input and output can be provided

Specifications: Model MLR 1476-1
AC Line Voltage: 26V $\pm 20\%$ @
400Hz $\pm 20\%$

Output: 26V $\pm 1\%$ for set point
Load: 0 to 40ma
Total Regulation: +0.1%
Distortion: 0.5% maximum rms
Temperature Range: $-55^\circ C$ to
 $+125^\circ C$

Size: 2.0" x 1.8" x 0.5"

Other units are available at different power and voltage levels as well as wider temperature ranges. Information will be furnished upon request.

SOLID-STATE SINE-COSINE SYNCHRO CONVERTER - NON VARIANT

This new encapsulated circuit converts a 3 wire synchro input to a pair of dc outputs proportional to the sine and cosine of the synchro angle independent of a-c line fluctuations.

- Complete solid state construction
- Operates over a wide temperature range
- Independent of reference line fluctuations
- Conversion accuracy—6 minutes
- Reference and synchro inputs isolated from ground

Specifications Model DMD 1508-2

Accuracy: Overall conversion accuracy 6 minutes. Absolute value of sine and cosine outputs accurate to $\pm 30MV$
Temperature Range: Operating $-40^\circ C$ to $+85^\circ C$, Storage $-55^\circ C$ to $+125^\circ C$

Synchro Input: 90V RMS $\pm 5\%$ LL 400Hz $\pm 5\%$

DC Power: $\pm 15V$ DC $\pm 10\%$ @ 50MA

Reference: 115VRMS $\pm 5\%$ 400Hz $\pm 5\%$

Output: 10V DC full scale output on either channel @ 5ma load
Temperature coefficient of accuracy: ± 15 seconds/ $^\circ C$ avg. on conversion accuracy ± 1 MV/ $^\circ C$ on absolute output voltages

Size: 2.0" x 1.5" x 2.5"

Units are available with wider temperature ranges and 11.8V LL, 26V reference synchro inputs. Information will be supplied upon request.

There is No Substitute for Reliability



GENERAL MAGNETICS • INC

135 Bloomfield Ave., Bloomfield, New Jersey 07003 - Tel. (201) 743-2700

Circle 228 on reader service card

Swage-Bond™ ... a revolution in trimmer reliability!

... here today at no extra cost in every Trimpot® Potentiometer

Historically, pin-to-element termination problems have been one of the primary causes of trimmer failure ... especially during handling and PC board process operations. Bourns exclusive Swage-Bond™ process virtually eliminates pin termination failure ... truly a revolution in trimmer reliability. Furthermore, Swage-Bonding results in a marked improvement in temperature coefficient consistency.

Other trimmer manufacturers utilize a simple clip-on termination. Some solder this connection, some rely on tension pressure alone. In the Swage-Bond process, the P.C. pins are secured **through** the substrate, with a high-pressure compression swage on both top and bottom sides. The pressure of the swage locks the pin solidly into the element, and thoroughly bonds it to the thick-film termination material.

Swage-Bond™ eliminates pin termination failure, provides more reliable tempco. Microphotograph shows trimmer element magnified 20X.



The seal that seals ... without springback

Bourns trimmers stay sealed when others fail. We know. We've tested them all. Bourns uses a chevron-type sealing technique, that seals without O-rings ... eliminating the windup and springback that frequently occurs with such seals. The result is faster and more precise adjustability ... with a seal that really works.



Wrap-around wiper for better setting stability

Bourns multi-fingered, wrap-around wiper delivers more consistent, more reliable performance. The unique design significantly reduces CRV fluctuations and open circuit problems due to thermal and mechanical shock ... by maintaining a constant wiper pressure on the element. Compare the ruggedness of Bourns design with the common "heat-staked" wiper designs. Compare performance. Specify Bourns.

HERE'S PROOF:

Send for a copy of our new engineering report on TRIMMER PERFORMANCE. Tell us about your application, and we'll provide qualification samples that best suit your needs.

Bourns reliability is available at ordinary prices ... off-the-shelf from nearly 100 local distributor inventories ... plus our largest-ever factory stock. TRIMMER PRODUCTS, TRIMPOT PRODUCTS DIVISION, BOURNS, INC., 1200 Columbia Avenue, Riverside, California 92507. Telephone 714 781-5320 — TWX 910 332-1252.



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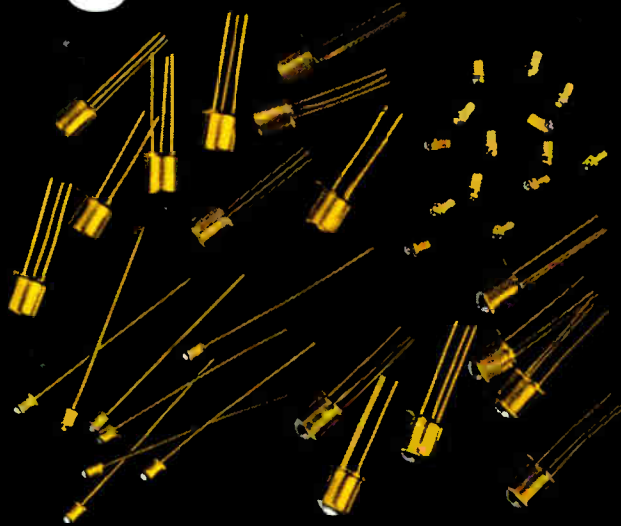
Circle 901 on reader service card

World Radio History

Get more current at lower light levels

Clairex photodarlingtons exhibit the highest sensitivity in the industry with specific types having a guaranteed light current (I_L) at 0.02 mw/cm^2 irradiance. A broad line of phototransistors and photodarlingtons is available in the TO-18, the "micro" (Pill) and an intermediate (Post) package.

The micro package is .060" in diameter and permits the assembly of arrays utilizing .100" centers. The intermediate package has a flange diameter of .098" which permits its use for small space applications and ease of product handling.



All units are hermetically sealed with either glass windows or glass lenses. The lenses provide a narrow angular response of $\pm 17^\circ$ while the win-

dows provide an angular response of $\pm 35^\circ$.

All Clairex phototransistors and photodarlingtons are 100% tested for light current (I_L) at a

stated irradiance... either per the standard Clairex specification, or per your special requirements. In addition, most Clairex units are tested to a minimum and maximum light current (I_L) limit... normally a 3:1 spread.

Because Clairex has specialized in opto-electronics since 1953, we probably stock the phototransistor or the photodarlington with the characteristics that you need.

Call (914) 664-6602 or write Clairex®, 560 South Third Avenue, Mount Vernon, New York 10550.

...with Clairex photodarlingtons and phototransistors.

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