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Synthesised signal generator for 10 to 1800MHz

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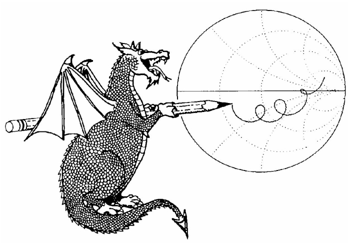

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Contents

There are two big articles in this issue. I decided to publish the complete articles rather than split them over two issues so that anyone who wants to build the equipment is not left waiting for the second part of the article.

I have also published an old article, from the German magazine UKW Berichte issue 2/1999. This contains more information on the design of inter-digital capacitors. It was requested by several subscribers following the article on a 100MHz bandpass filter published in issue 4/2003. There are some older articles that did not get translated and published, when there is a demand for any of these articles I am always happy to get them translated and published.

I am always looking for new authors or new articles. The article by Carl Lodström in issue 1/2004 has already been noticed by an Italian magazine - RadioKit Elettronica - and they will be translating it into Italian and publishing it later this year. So if you have an article to publish in VHF Communications it might find it's way into other foreign publications

I have published this issue a bit earlier than normal because I will be attending the Ham Radio exhibition at Friedrichshafen when I would normally be posting the magazines. Hopefully I will meet some of the subscribers at the exhibition

73s - Andy

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Synthesised signal generator for 10 to 1800MHz

The construction of a high quality signal generator presents a developer with one challenge after another. Several concepts and the most varied approaches to solutions are presented in this article To keep the amount of assembly and wiring as low as possible, and obtain the best possible signal quality, the author developed his own concept which is described below.

1. Introduction

A synthesised signal generator can be used as the signal source for a multitude of measurement and calibration operations. The essential factors in its usability are the range of performance and signal quality.

If we set ourselves the task of constructing a SUPER signal generator to laboratory standards of quality, it soon becomes clear that developing such a piece of apparatus would require a considerable amount of time, and furthermore the cost of realising it should not be underestimated.

So a concept was sought for the development of this signal generator that would keep the amount of assembly work as low as possible but would nevertheless supply a good signal quality, with harmonic signals as low as possible. This led to the "Syn-1800" synthesizer, a solution which has a few interesting details and the following performance:

- Frequency range: 10MHz - 1800MHz in one continuous band
- Smallest frequency division: 1Hz
- Precision of frequency dependent on TCXO/OCXO used
- Output: 0dBm to +10dBm (+13dBm to approximately 1500MHz)
- Power adjustment: in 0.1dB steps Analogue and digital power regulation (only approximately 0.2dB frequency dependence)
- Fully automatic power calibration (digital levelling)
- Digital frequency fine trimming

Technical data for prototype:

- Spectrum purity: (measured at +7dBm output)
- Harmonic attenuation 15 -1800MHz : >= 40dB

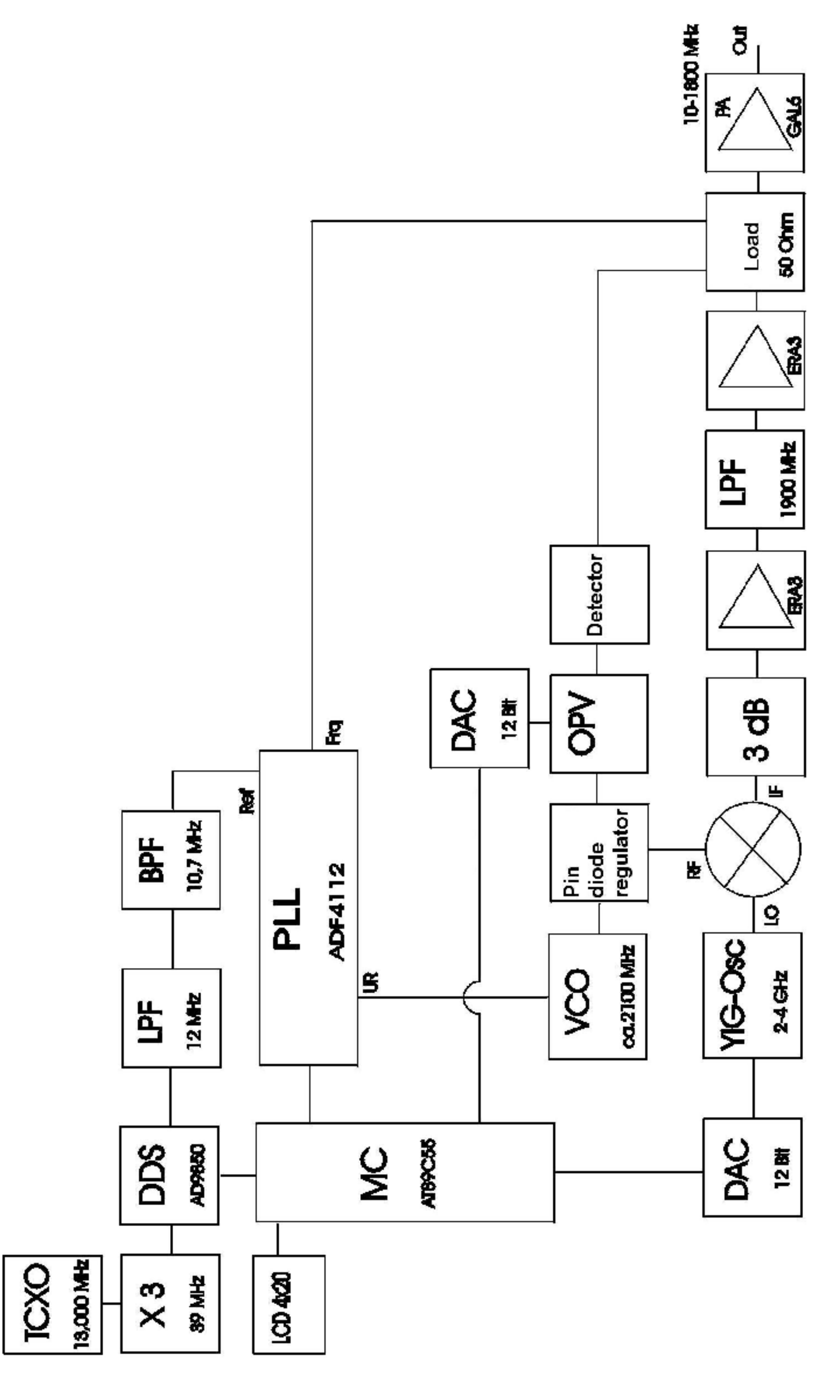


Fig 1: Block diagram of the 10 - 1800MHz synthesised signal generator.

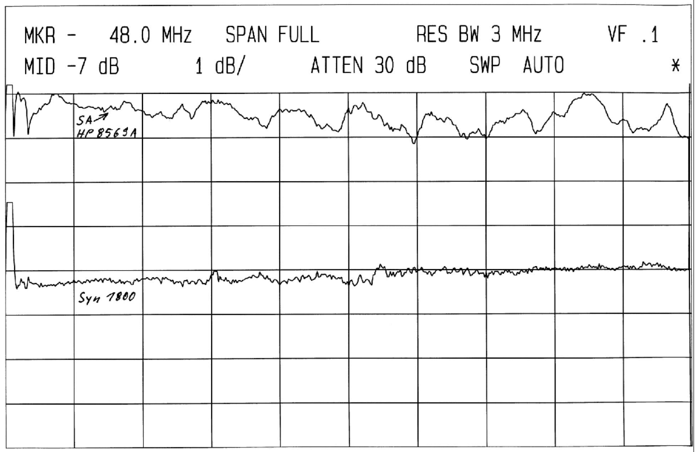


Fig 2: Graph of power regulation from 10 to 1800MHz.

- Harmonic attenuation at 10MHz : 34dB
- Spurious attenuation 10 -175 MHz: >= 40dB
- Spurious attenuation at 1800 MHz: 37dB
- LO suppression (2170MHz): 50dB Image frequency suppression (2180 - 3970MHz): 34dB - 53dB
- Precision of frequency (with 1ppm TCXO used) At 100MHz and 25°C Room temperature: after 10 min time running warm -10Hz: after 20 minutes -6Hz: after 30 minutes - 3Hz

2. Operating principle

The block diagram (Fig 1) provides a view of the individual functional units. The actual frequency synthesiser consists of a YIG oscillator (2 - 4GHz) and a VCO, which runs at approximately 2170MHz and has a tuning range of only approximately 30MHz. The YIG oscillator is tuned by a 12 bit digital to analogue converter.

Both signals are fed into a ring mixer, enhanced and filtered with a steep low pass filter. A small part of the signal generated is fed to the PLL. Only the VCO is re-adjusted with this control voltage. The necessary reference frequency of 10.7MHz is generated by a DDS and fed to the PLL. Using the DDS to generate the reference frequency, it becomes possible to set the output signal in 1Hz steps.

2.1. Advantages of this concept

- Expanded frequency range without band switching.
- Good harmonic attenuation without filter on top.
- The frequency precision is determined only by a reference oscillator (TCXO/OCXO).
- Low construction cost.
- Few manual calibration points.
- Small space requirement giving a small housing.

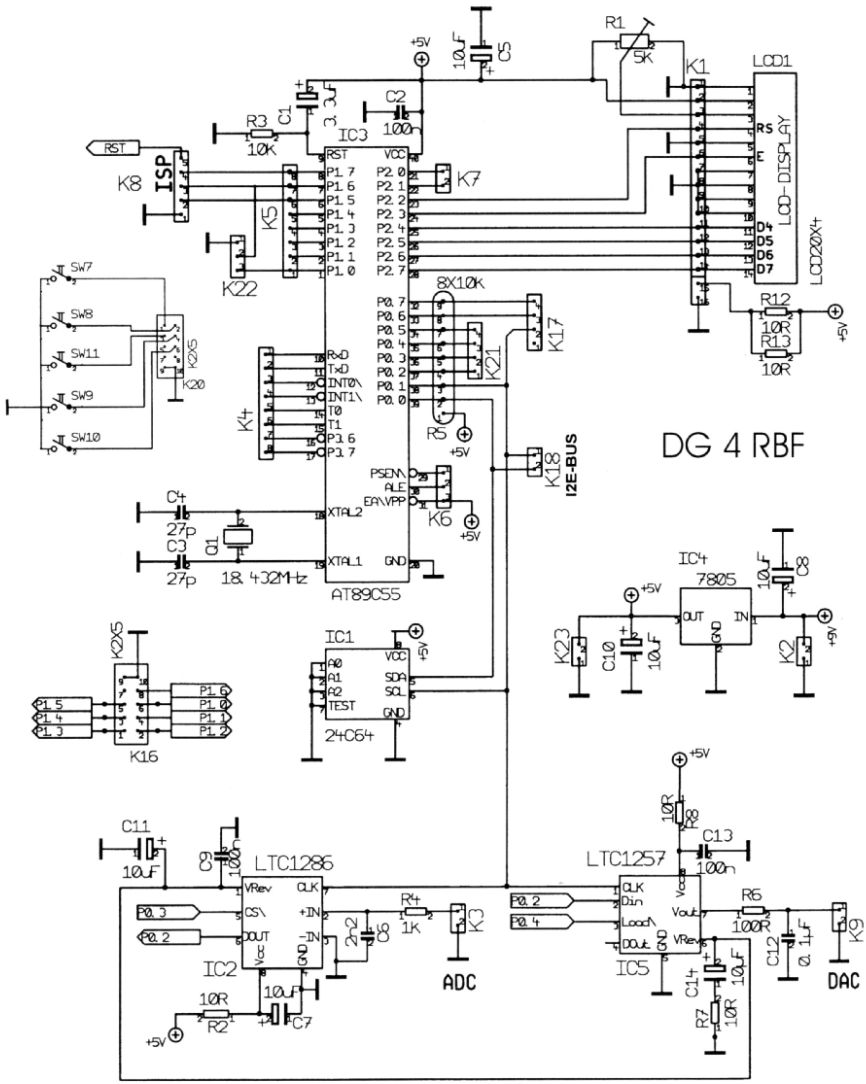


Fig 3 Circuit diagram of the new micro-controller for the 10 - 1800MHz synthesised signal generator.

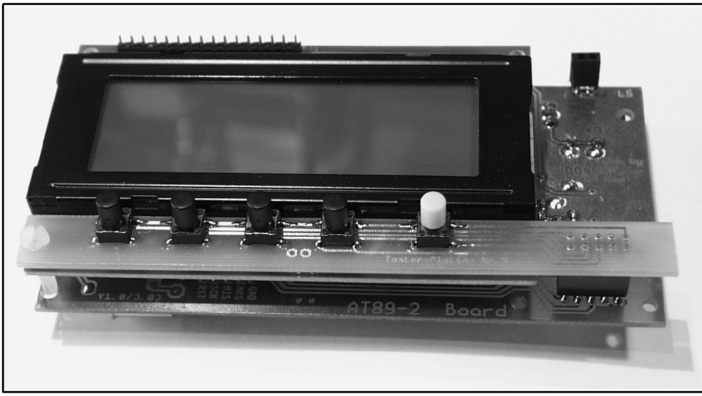


Fig 4: View of the LCD display mounted on top of the micro-controller board.

2.2. Precise power regulation through analogue and digital correction

The signal generator has analogue power regulation, which keeps the level constant, at approximately 1dB, over the entire range. When this is combined with a digital power corrector (corrector values every 10MHz), a very precise power setting is obtained. Thanks to a 50Ohm load at the output, with an additional amplifier for de-coupling, the output level is relatively independent of the load. Fig 2 shows the level regulation in the range from 10MHz to 1800MHz with 1dB/Div. These curves were recorded using an HP 8569A spectrum analyser in MAX HOLD mode, which itself only has a level precision of approximately +/- 1dB (top curve in Fig 2). A wobble generator type EIP 931 was used to give a more precise measurement result by means of the SA’s normalising function.

2.3. Cost of implementation

Using this concept and a modular construction procedure, in conjunction with a micro-controller (AT89-2 board), it was possible to keep the cost of implementation comparatively low.

3. The individual components

3.1. AT89-2 microcontroller board

A new circuit (Fig 3) and a new micro-controller board (AT89-2 board) were specially developed for this application, with a 4 line LC display. This equipment can be controlled using push buttons.

The LC display, with 4 x 20 characters, is assembled on one small printed circuit

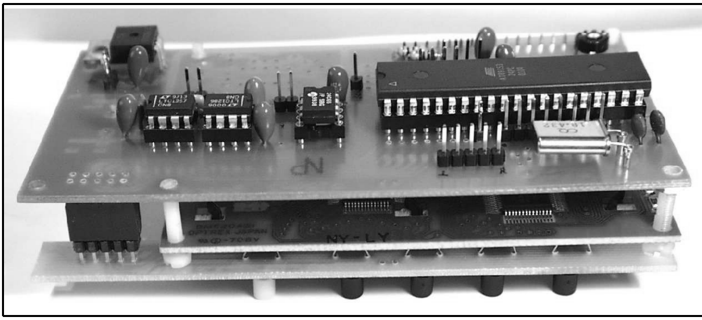


Fig 5: View of the micro-controller board with the LCD display underneath.

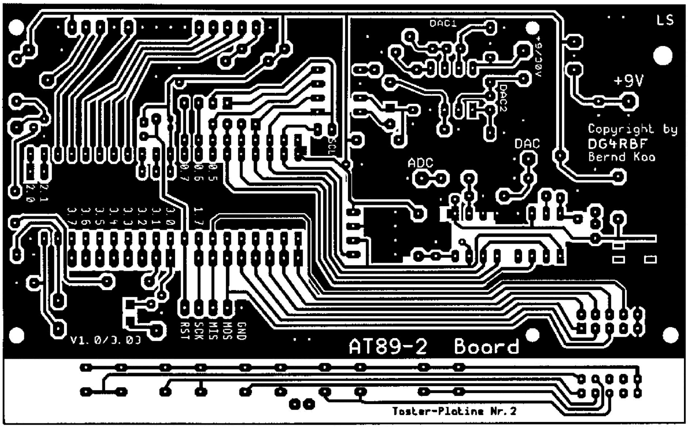


Fig 6: PCB layout for the AT89-2 micro-controller board.

board, and the push buttons are on another. These two boards can be positioned directly on top of the micro-controller board (Figs 4 and 5). This dispenses with the expensive wiring for an LCD and buttons and also gives the system more operational security. The micro-controller board can be mounted directly behind the front plate as a complete unit.

The micro-controller board was developed as a single sided board made from 1.5mm thick FR4 material for the AT89C52, AT89C55 and AT89S53 controllers from ATMEL (Fig. 6). These single chip micro-controllers need no EPROM and no external RAM. The program is saved directly in the micro-controller.

The board also has a socket for an EEPROM (24C64), together with the LTC 1286 12 bit AD converter and the LTC 1257 12 bit DA converter, with an internal voltage reference of 2.048V.

Additional components are also provided for on the board for future applications, but the relevant components should not be mounted here.

The single row connector strip attaches the standard 4 x 20 charatcter LCD display (pins 1-14). Pin 15 and pin16 are also accommodated. They can be used

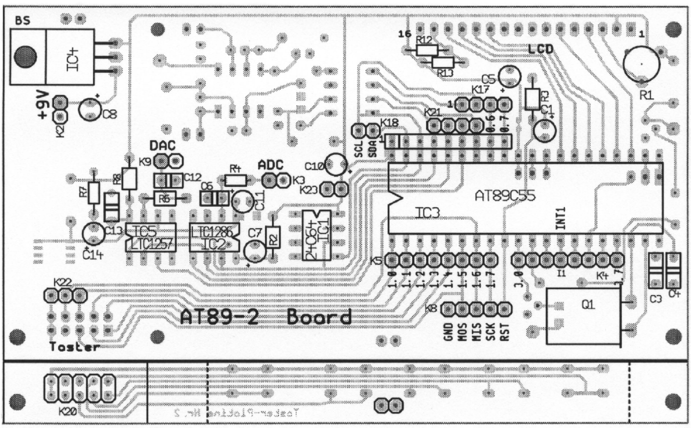


Fig 7: Component layout for the AT89-2 micro-controller board.

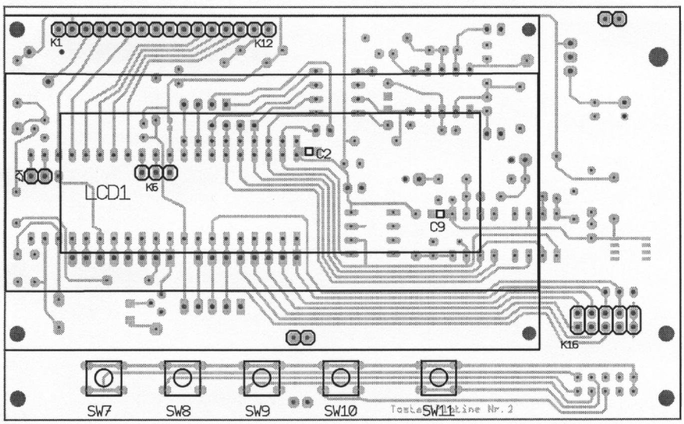


Fig 8: Component layout for the SMD parts on the micro-controller board plus the LCD display and switches

for back lighting. The R1 potentiometer adjust the contrast.

The program for the signal generator is stored directly in the AT89C55 processor. Setup information and calibration data are securely saved in a 24C64 EEPROM and are retained even when the system is switched off.

The narrow button board should be cut off before the components are fitted onto the main board. The components are fitted onto the top and bottom faces in accordance with the component drawings in Figs 7 and 8.

The display board has a 14 pin (16 pin) connector strip and the processor board has a 14 pin (16 pin) socket terminal strip; thus the display can simply be plugged on but remains detachable.

IC sockets should be used for the micro-

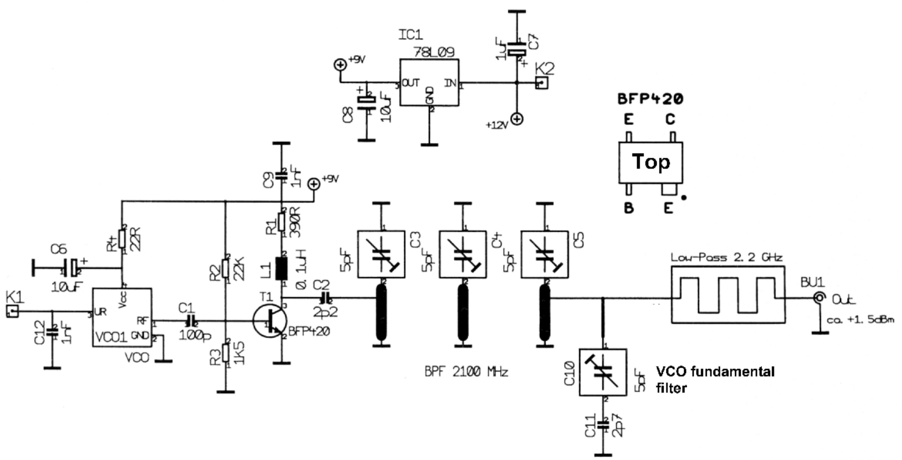


Fig 9: Circuit diagram of the VCO for the 10 - 1800MHz synthesised signal generator.

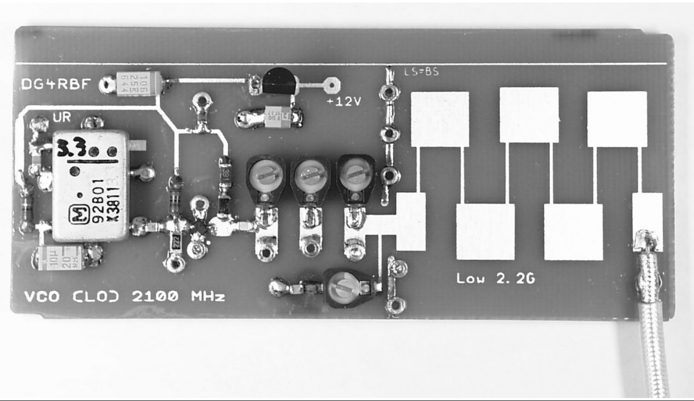


Fig 10: The completed VCO board.

controller and the EEPROM. If desired, the DA and AD converted can be inserted into IC sockets.

3.2. VCO assembly

A narrow band type of VCO is used, which should have a range of approximately 30MHz in the range between 2100MHz and 2200MHz. The search for a suitable VCO for this range turned out to be difficult, but it proved to be considerably easier to obtain VCO's with an output frequency of around 1000MHz. For this reason, a VCO producing approximately 1090MHz was chosen with a doubler stage.
A low pass filter, which would have been needed in any case, was integrated directly onto the 1.5mm thick epoxy printed circuit board (FR4).

3.2.1. VCO Operation

The VCO is followed by a doubler stage, using a BFP 420 from Siemens (Fig. 9).

This is followed by a three stage band pass filter using microstrip circuit technology. There is also a filter circuit for the fundamental frequency of the VCO (1090MHz) that suppresses it by up to 70dB.

It does not make sense to mount this filter circuit (C10 + C11) unless a spectrum analyser is available to calibrate it. Without a filter circuit, the fundamental frequency can still be attenuated up to approximately 45dB, which is still adequate.

At the output there is a 13 pole "printed" low pass filter, which is laid out for a cut-

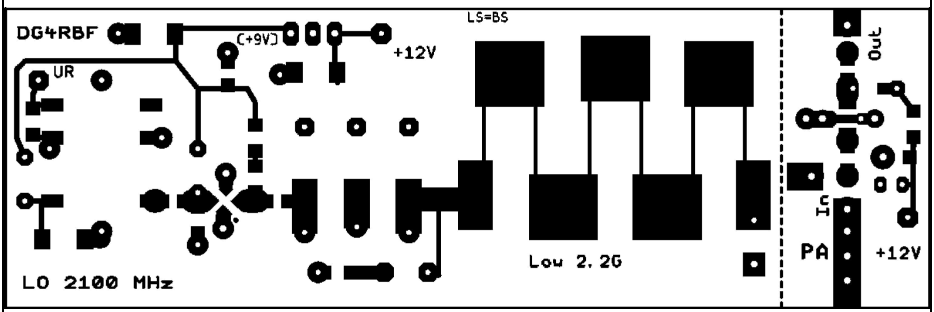


Fig 11: PCB layout of the VCO and PA boards.

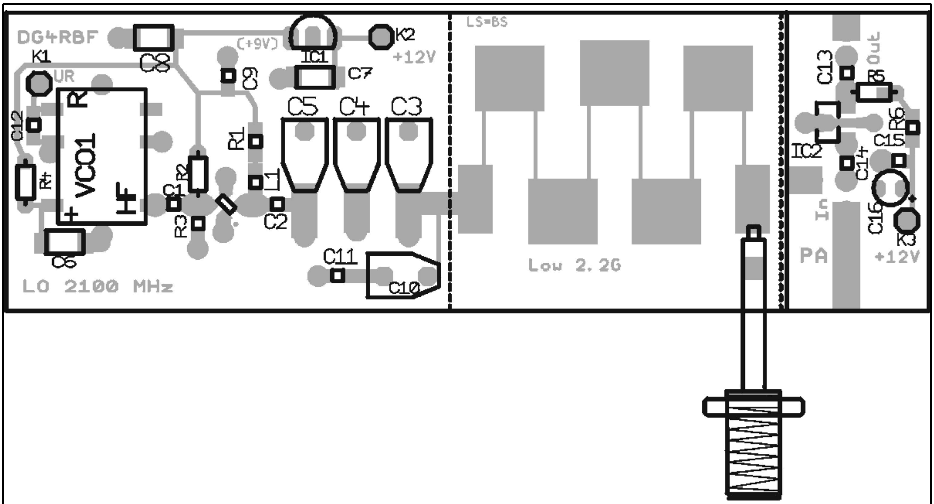


Fig 12: Component layout of the VCO and PA boards.

off frequency of approximately 2200MHz and needs no calibration (Fig. 10).

3.2.2. VCO Assembly instructions

The layout of the 107mm x 35mm VCO board (FR4), is shown in Fig. 11. The components are mounted on the component side in accordance with the component drawing in Fig. 12.

The completed board is fitted into a tinplate housing and well soldered to the earthing side. The board is slightly shorter than the standard housing, but this is not important. In order to avoid a waveguide effect when a lid is placed on top, and to ensure that the higher frequencies can overcome the low pass filter without interruption, either a partition must be soldered on at the marked point following the band pass filter or a piece of conductive foam material must pressed into the upper part of the housing. There are through connections on the board for soldering the partition.

3.2.3. VCO Calibration

If no spectrum analyser is present, then calibration is not possible, except using an mW meter. For this purpose, the trimmer of the band pass filter is turned to the minimum and then set to an overlap of approximately 1mm. The setting is then altered from this basic setting to the maximum value by gently rotating the trimmer with a (non-metallic) trimming tool. When the maximum value has been found by rotating the trimmer in each direction and the capacitor plates of the trimmer overlap only slightly, the calibration is correct. You should expect a signal level of approximately +1.5dBm. You cannot calibrate at the wrong frequency unless you rotate the trimmer too far (approximately halfway); then you'd be calibrating at 1080MHz!

If a spectrum analyser is present, the filter circuit trimmer can be set for minimum output of the fundamental frequency. This cannot be calibrated properly unless the board has been soldered into the tinplate housing. Since the filter circuit has a very narrow bandwidth, a control voltage of approximately 3.8V should be applied to the VCO and the lid's capacity should also be taken into

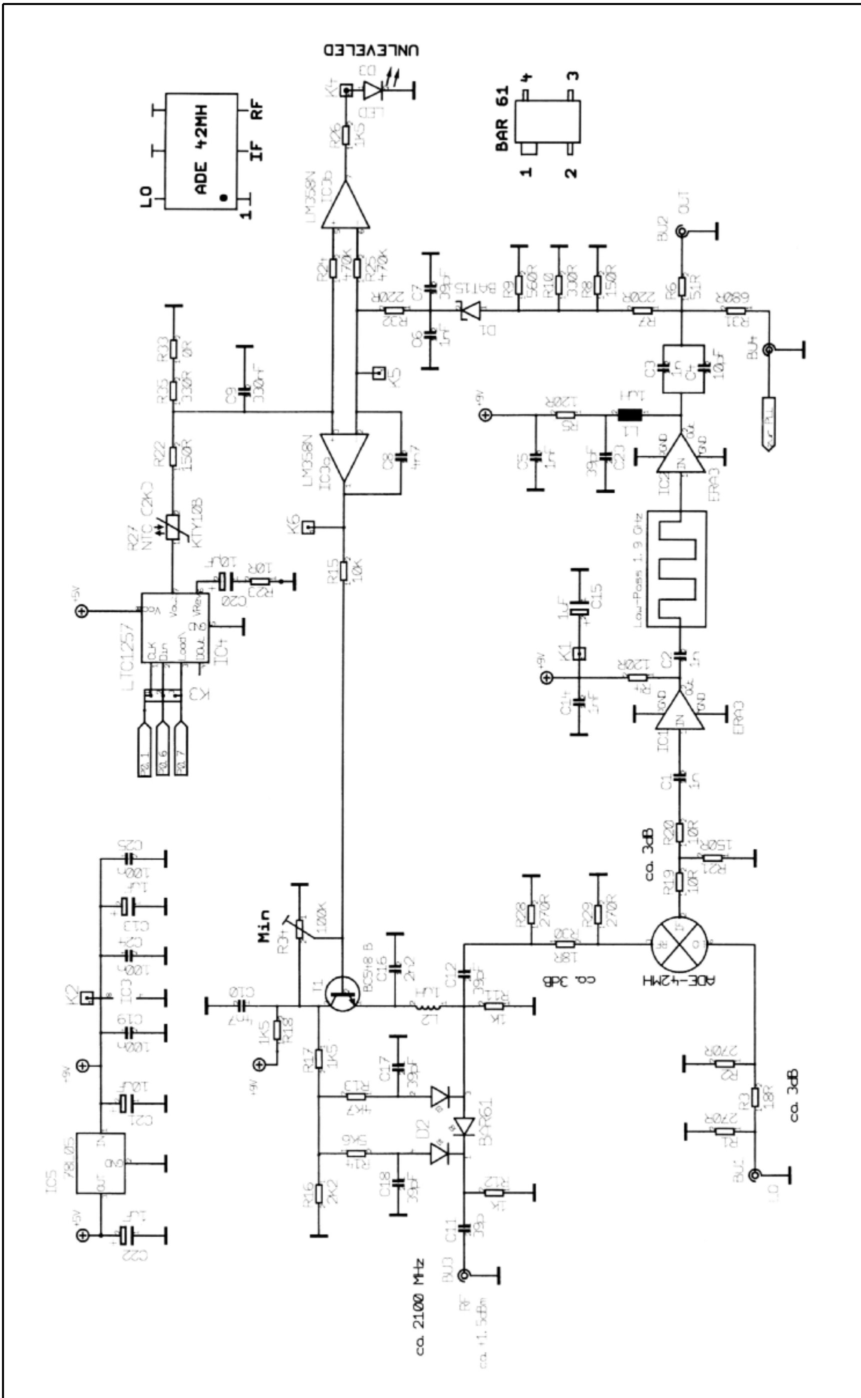


Fig 13: Circuit diagram of the mixer for the 10 - 1800MHz synthesised signal generator.

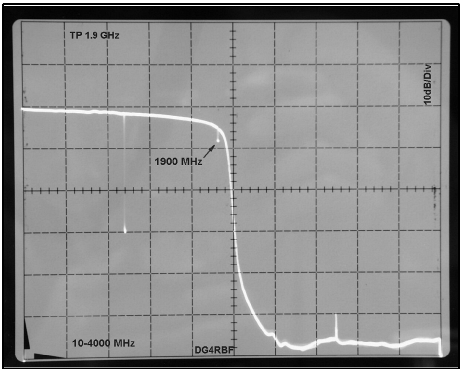


Fig 14: Frequency response of the 21 pole filter at the output of the mixer.

account.

3.3. Mixer assembly operation

The signal from the YIG oscillator is connected to socket BU1 (Fig. 13). Following an attenuator of approximately 3dB, the signal is fed to the ADE 42-MH mixer LO port. Approximately +13dBm should be detectable at the LO port, an acceptable signal is in the range between +10dBm and +15dBm.

The mixer can process frequencies between 5 and 4200MHz at the LO and RF ports, so that the intermediate range extends from 5 to 3500MHz. The signal from the VCO is connected to socket BU3. The level is set by means of the adjustable PIN diode attenuator (PIN diodes), using the BAR61 diode. This is fed to the RF input of the ring mixer via a 3dB attenuator.

A 3dB attenuator is also provided at the (intermediate frequency) mixer output to ensure that good phasing is obtained, and reflections are kept to a minimum. This is followed by two ERA3 MMIC amplifiers and a very steep 21 pole low pass filter with a cut-off frequency of approximately 1900MHz. This filter, which DG4RFB developed himself, takes the form of a microstrip and has already proved itself in various circuits. The steep flank of the filter is very important, since it has to suppress the LO signal at approximately 2190MHz, together with the image frequencies (Fig. 14).

The output is terminated with a 51Ohm resistor, which helps to make precise power regulation possible. For power regulation (levelling), some power is sampled before the 51Ohm resistor (R6), rectified using diode D1 (BAT15) and fed to an OP (IC3a), which re-adjusts the attenuator at the mixer input so that the output is kept constant.

Theoretically, such regulation circuits are extremely simple. In practice, however, it is often difficult, with broad band circuits of this kind, to obtain an “orderly” frequency response. Power levels within approximately 1 dB can be obtained in the frequency range between 10 and 1800MHz using the circuit presented here. Fig 2 shows the level regulation in the frequency range indicated at 1dB/Div. This curve was again plotted using an HP 8569A spectrum analyser, using the EIP 931. The lower curve in the diagram shows the test results.

At first glance, the parallel resistors R9 - R11, before the detector diode D1, seem to have no purpose, but these resistors can be used to influence the frequency response of the regulation circuit. If the resistance value is increased, then the power at the band end is increased, and vice versa. Thus varying these resistors can optimise the frequency response.

Digital power setting is achieved using the LTC 1257 12 bit DA converter (IC4). A defined voltage is applied to pin 3 of the regulation OP. The LTC1257 has an internal voltage reference of precisely 2.048V. At the output of the DA converter there is an NTC, together with a voltage divider. The resistance ratio of the voltage divider scales the output voltage for power regulation. The NTC compensates for the temperature coeffi-

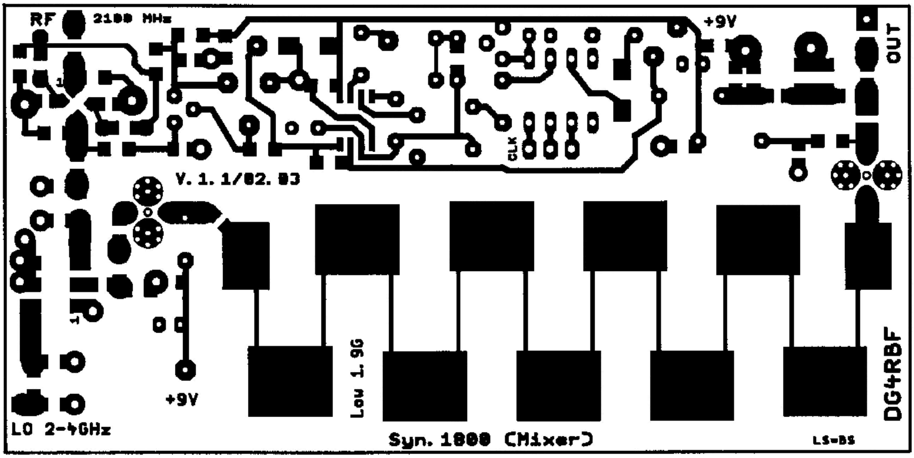


Fig 15: PCB layout for the mixer and filter.

cient of the detector diode (BAT15). It is possible to obtain quite good temperature compensation using the NTC. R33 is not normally required, and is provided only to give more options if another divider ratio is needed on the voltage divider. The second OP (IC3b) detects situations when the required power is not maintained and lights the UNLEVELED diode.

3.3.1. Mixer assembly instructions

The 109mm x 54mm printed circuit board layout for the mixer board is shown in Fig 15. All components are mounted on the foil side of the board (Fig 16). An IC socket is used for the LTC1257 DA converter. Make sure C12 is precisely positioned. When the components have been mounted, the board can be soldered into the tinplate housing. The

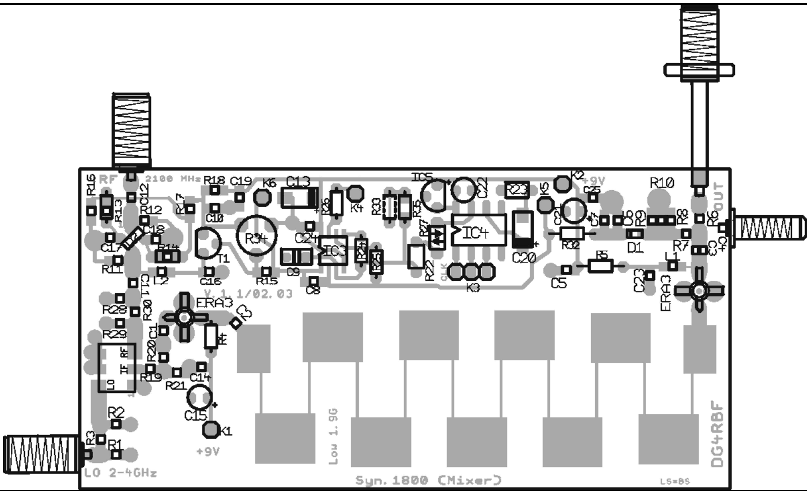


Fig 16: Component layout of the mixer.

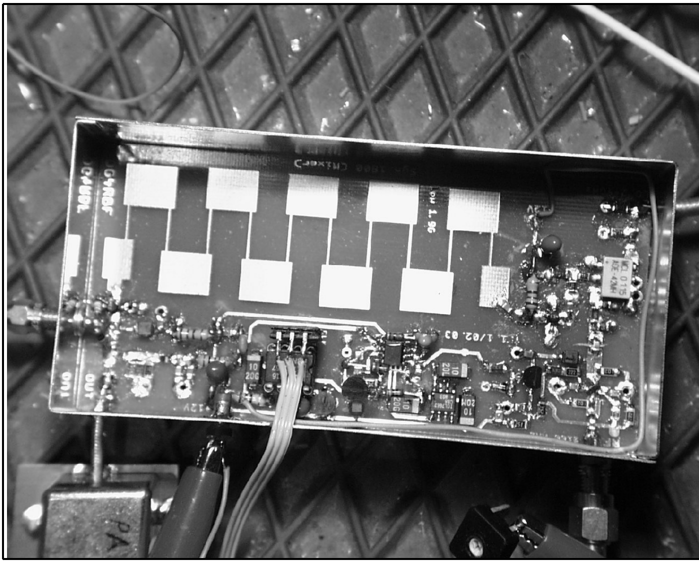


Fig 17: Picture of the completed mixer assembly.

power lead uses of a feedthrough capacitor. It is best to use SMA sockets for the RF inputs. The output is a flexible RF cable feeding the GAL6 PA.

The circuit diagram shows R31, which feeds some power to the PLL. This resistor is not positioned on the board, but is soldered on separately and leads to a nearby SMC socket. Fig 17 shows the completed mixer assembly.

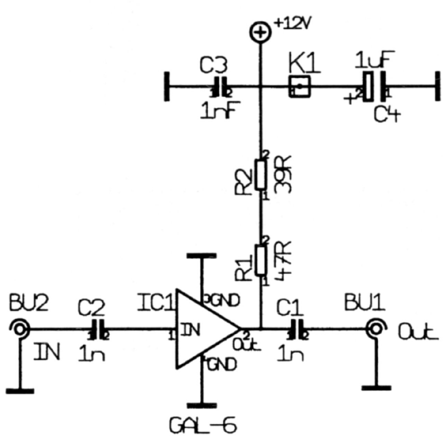


Fig 18: Circuit diagram of the GAL-6 output amplifier.

3.4. Output amplifier with GAL 6

The mixer board is followed by a separate output amplifier, which consists of a GAL 6 type MMIC from Mini Circuits. This component has similar performance to the ERA 6 and a very smooth frequency response, together with a high IP3 of 35.5dBm. It is thus extremely suitable for maintaining a signal with low harmonics.

By using this amplifier after the level regulation, an additional de-coupling from the output is obtained, so that the output regulation acts independently to the load at the output. This means that even if the connected load is mismatched the correct power is generated.

The circuit can be seen in Fig 18. The few components in the “PA” are assembled on a small board (see Fig 11, right) and then soldered into a small housing, or protected using a screening box.

The PA’s output should be fitted close to the output socket of the apparatus. To simplify the board manufacture, the small

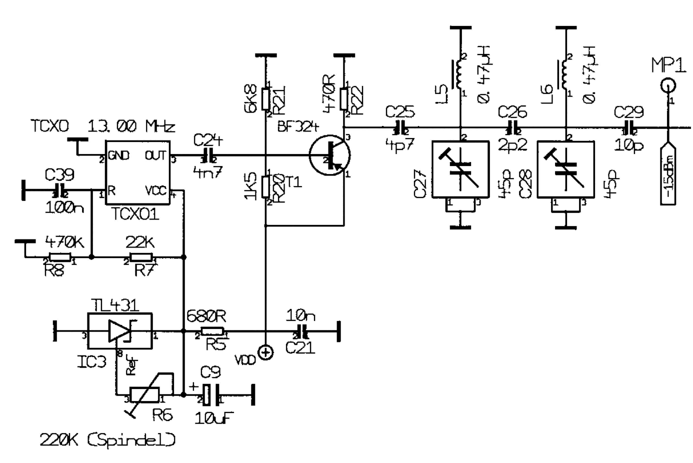


Fig 19: Circuit diagram of TCXO section of the PLL/DDS assembly.

board was added the VCO board, and should be cut off before assembly.

3.5. PLL/DDS assembly

In order to ensure that it can be copied easily, this assembly is divided into three construction sections and the assembly is described here step by step.

3.5.1. PLL/DDS operation

Construction section (1) includes the TCXO, with tuning and frequency tripling. A 13MHz (1ppm) temperature compensated quartz oscillator (TCXO) is used as a frequency reference. An adjustable voltage reference (TL431) of approximately 2.5 V is used for the power supply and tuning voltage. The fine setting can be adjusted to precisely 13MHz using the spindle trimmer. The TCXO is followed by a BF324 frequency multiplier and a 39MHz band pass filter (Fig 19).

Construction section (2) concerns the DDS, with filter and amplifier stage. The DDS generates the reference frequency of the PLL and generates a 10.7MHz signal, which can be tuned in very small steps, from the clock frequency of 39MHz. The familiar AD9850 from Analog Devices is used as the DDS.

At the output of the DDS is a low pass filter with a cut-off frequency of approximately 12MHz. This signal is then amplified by an MSA886 and filtered by a matched 10.7MHz ceramic filter (Fig 20).

The PLL is contained in construction section (3). The ADF4112 is used, a modern component from Analog Devices. This PLL operates at up to 3GHz, has very good noise values and is used here with a pre-divider factor of only 8/9. The PLL component is programmed through a 3 wire bus by the microcontroller. Anyone interested in finding out more about this PLL component should consult the 24 page data sheet from Analog Devices. One important element in the PLL is the loop filter, which can be found at pin 2. Low loss foil capacitors should be used for the loop filter capacitors if possible. Since the PLL has to operate over a very wide range, the loop filter is naturally never optimally designed. Fortunately, the current for the charge pump can be programmed in 8 stages (0.63mA - 5.0mA), so that a certain matching can thus be achieved to the wide frequency range. An additional problem that has to be overcome is that the PLL does not normally

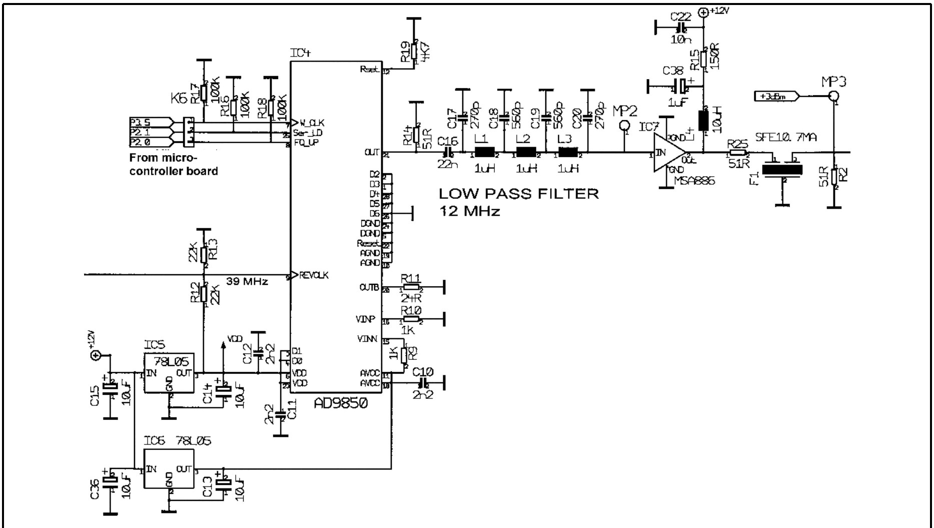


Fig 20: Circuit diagram of the DDS section of the PLL/DDS assembly.

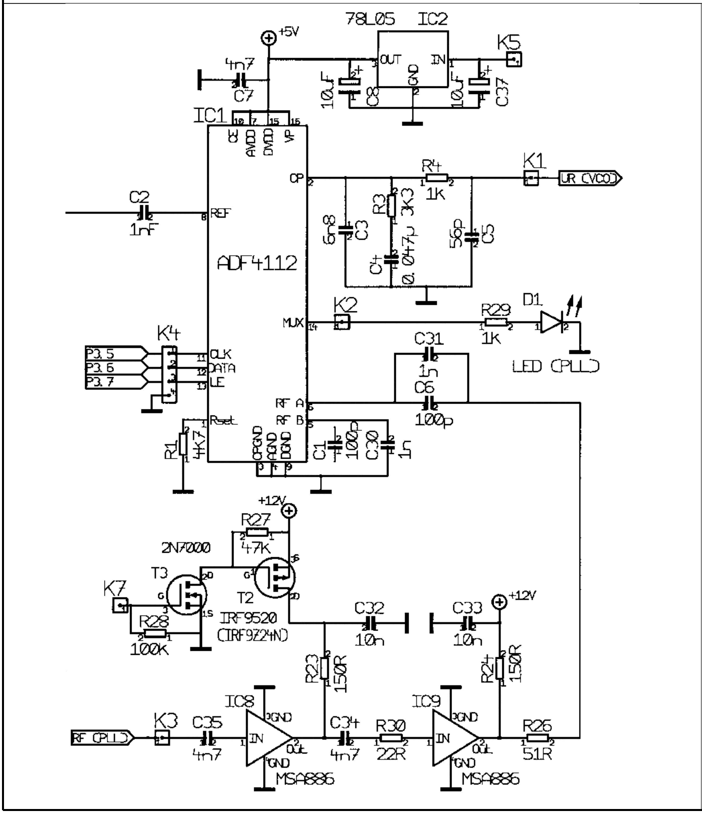


Fig 21: Circuit diagram of the PLL section of the PLL/DDS assembly.

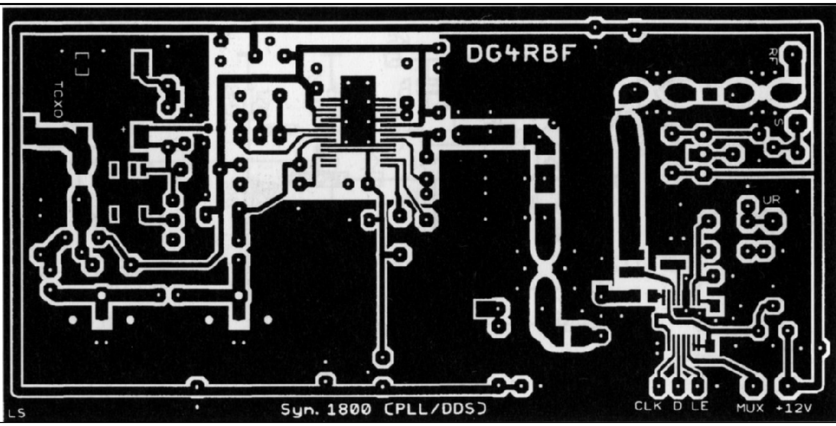


Fig 22: Track side PCB layout for the PLL/DDS board.

function below 100MHz. Below 100MHz a square wave signal can be used for the drive. Here we simply used an additional amplifier (MSA886), which is connected via the two transistors T2 and T3. If the power supply for this MMIC is switched off, then it works as attenuation. If it is connected up, then the subsequent amplifier IC9 is saturated and the PLL operates down to under 10MHz. The "MUX" output of the PLL is programmed as "Lock Detector" switching the LED on if the PLL is locked (Fig 21).

3.5.2. PLL/DDS assembly

Figs 22 and 23 show the PCB layout of the PLL/DDS board and Figs 24 and 25 show the component layout.

Construction section (1)

1 Through hole plate printed circuit board and fit into tinplate housing, but do not solder it in yet.

2 The pin holes, that are not used as earths. must be cleared on the "earthing side". (Sections 1 and 2

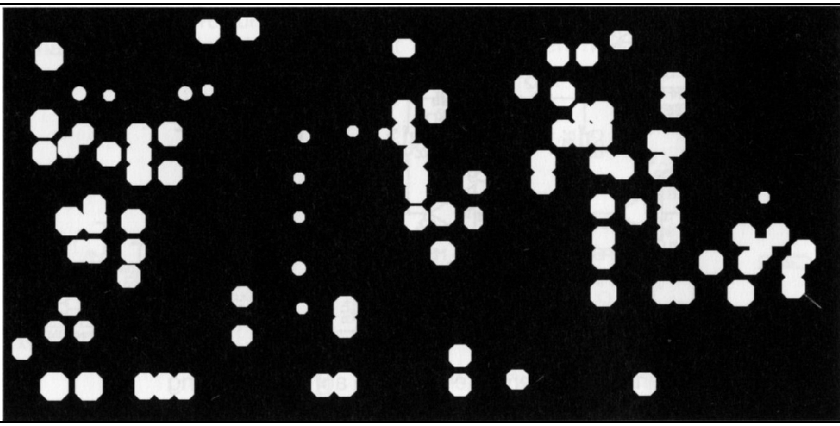


Fig 23: Component side PCB layout for the PLL/DDS board.

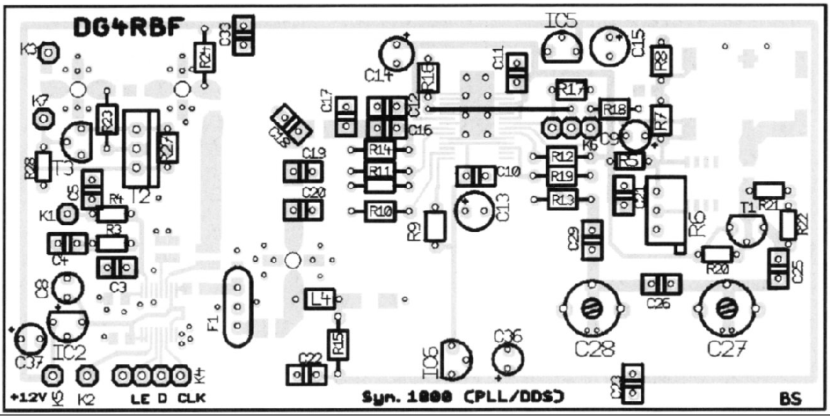


Fig 24: Component layout for the PLL/DDS board.

are not needed unless you are making the board yourself)

3 Fit the 3 regulators (78L05) with the associated filter electrolytic capacitors. Then connect up the 12V power supply and check that the voltage is 5V.

4 Fit all components for this section (1).

5 Turn trimmers C27 and C28 to maximum capacity.

6 Connect an mW meter to (MP1).

7 In turn, tune each trimmer slowly backwards, set them for the maximum level. Then set the trimmer to approximately half.

8 Use a frequency counter to check for 39MHz at (MP1).

Construction section (2)

1 Mount all the components for this section. Before the DDS IC is soldered in, the soldering pads are tin-plated on the board. The IC can then be soldered on, using a small

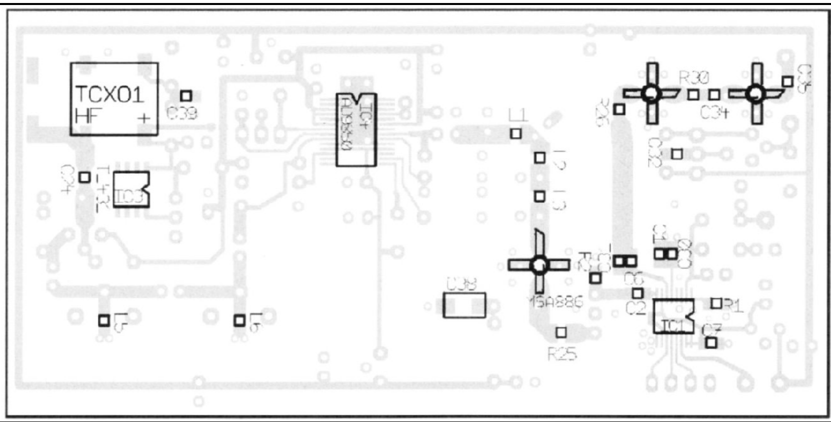


Fig 25: SMD component layout for the PLL/DDS board.

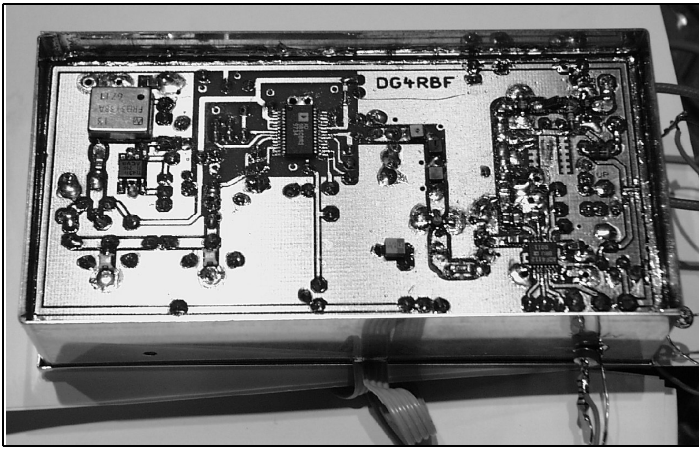


Fig 26: Completed PLL/DDS unit.

SMD soldering iron, without adding any more solder. The solder on the board should suffice. It is helpful to use a magnifying glass when soldering on this IC. But at any rate the soldering must be inspected using a magnifying glass. Don’t forget solder bridges at K6.

2 To check the functioning of this construction section, the micro-controller must be connected to K6. Once it has been switched on, the DDS IC is provided with the required data and a 10.7MHz signal should be available on (MP3) at approximately. +3dBm.

3 If a spectrum analyser is available, then this signal should be set with C27+C28 at the lowest noise level. (But this is not absolutely necessary.)

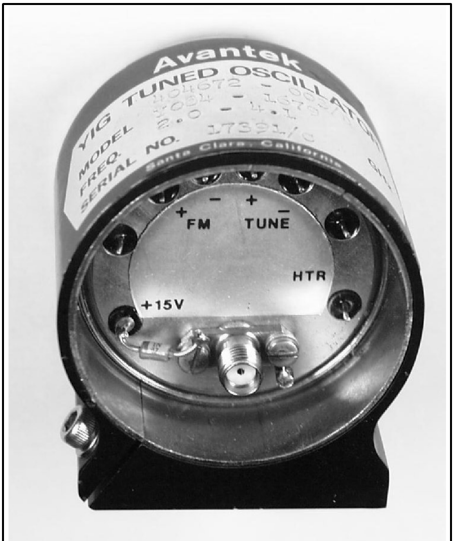


Fig 27: YIG oscillator used in the prototype.

Construction section (3)

1 Mount all the components for this section. The PLL IC can be soldered in using the same technique as in construction section 2. When connecting up the LED D1 at K2, don’t forget the resistor.

2 The PLL cannot be tested until all assemblies have been wired together.

Figs 26 show the PLL/DDS assembly

3.6. YIG oscillator

A YIG oscillator with a frequency of 2 - 4GHz is used as the main oscillator. These oscillators have recently become available on the surplus market at reasonable prices. Fig 27 shows the YIG used from Avantek.

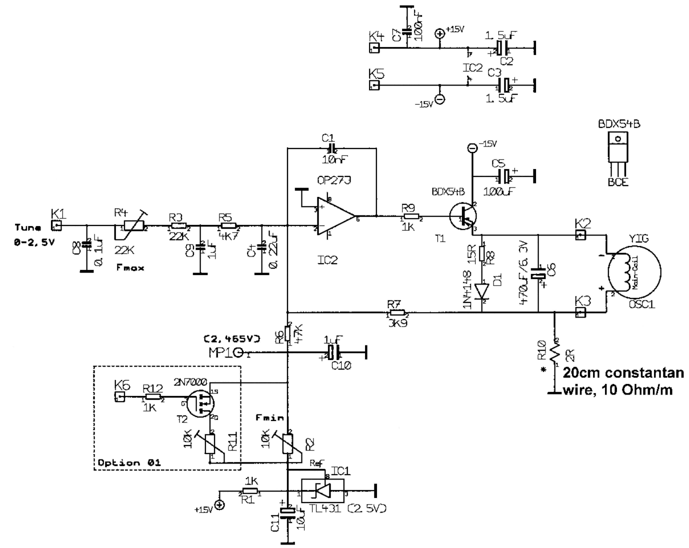


Fig 28: Circuit diagram of the YIG driver.

3.7. YIG driver

A YIG oscillator has at least two tuning coils, the main coil which is designated as “TUNE” and is used for tuning over the entire range and the FM coil for fine tuning or FM modulation. The frequency of the YIG oscillator is proportional to the current that flows through the tuning coil. Thus a YIG driver is also needed to drive the oscillator. The circuit variant used has a setting for the tuning gradient (Fmax), plus the addition of an offset value (Fmin), Fig 28. The oscillator can thus be best matched to the tuning conditions. A reverse coupling through R7 serves to make sure that the frequency remains stable when the oscillator warms up. An important factor here is the resistor R10, which consists of 20cm of constantan wire (10 Ohm/m) and which is made into a small air-core coil. This circuit has proved itself extremely well in practice. The BDX 54B power transistor must be mounted on a heat sink. Fig 31 shows this board. The micro-controller

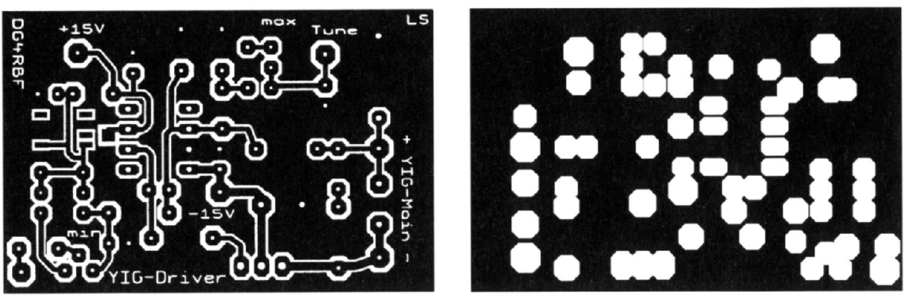


Fig 29: PCB layout for the YIG driver.

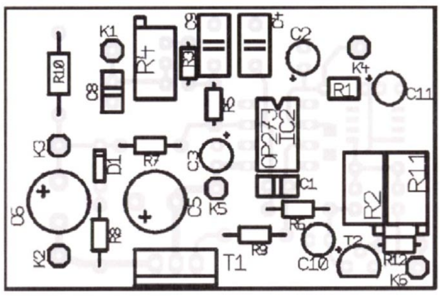


Fig 30: Component layout fro the YIG driver

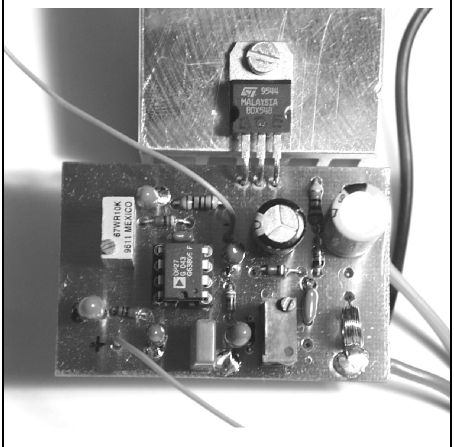


Fig 31: The completed YIG driver assembly.

must be connected to the YIG driver using a screened cable. The option 01 which is specified on the wiring diagram and the components drawing is not fitted. Figs 29 and 30 show the PCB layout for the YIG driver and Fig 31 shows the completed assembly.

3.8. RF ON/OFF

The 12V supply voltage of the VCO and the YIG oscillator is connected so that the RF output of the signal generator can be switched on and off. Two FET's are used for this purpose, see Fig 32 which shows the small circuit.

3.9. DC amplifier for automatic calibration

The signal generator has an automatic calibration function, which makes it possible for it to keep the output very constant over the entire frequency range. For this purpose, a diode detector with a frequency response as good as possible must be connected to the AD converter (LTC1286). This 12 bit AD converter is completely matched at an input voltage of +2.048V. But since a diode detector gives only approximately 1.2V at an input of +13dBm, we still need some further amplification for this DC voltage. Most detectors output a negative voltage. A simple OP connected as a DC voltage amplifier can solve both problems. The OP can be switched to accommodate a detector with negative or positive voltage. The amplification is matched to the detector by means of a potentiometer. Fig 33 shows the circuit. Since this amplifier consists of only a pair of components, the

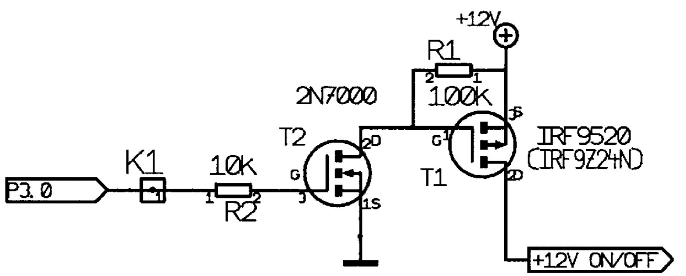


Fig 32: Circuit diagram for the RF On/Off control.

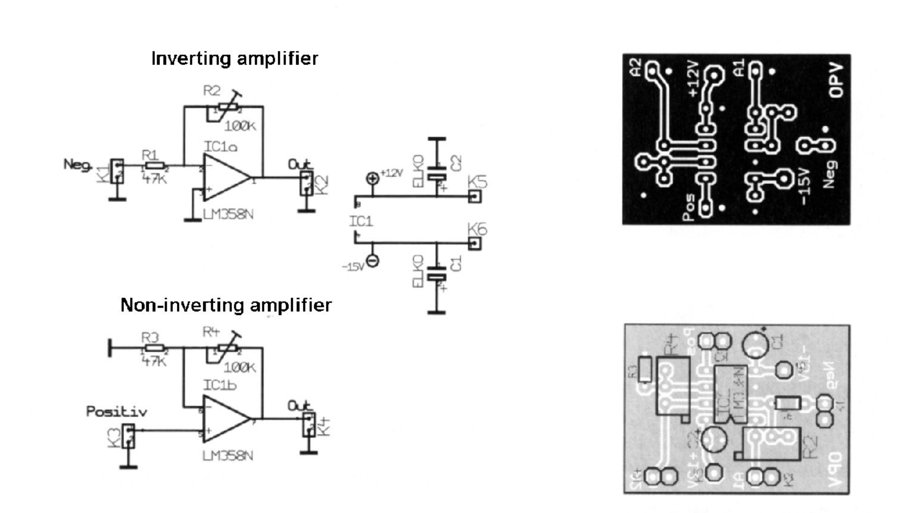


Fig 33: Circuit diagram for the calibration amplifier showing the two alternatives for positive or negative inputs plus a PCB layout.

simplest way to assemble it is on a small breadboard or using the "open air" technology. The input of this amplifier is best fitted on the rear face of the signal generator (BNC socket).

4. General assembly instructions

For a DIY board, the through platings are manufactured using 1.4mm compression

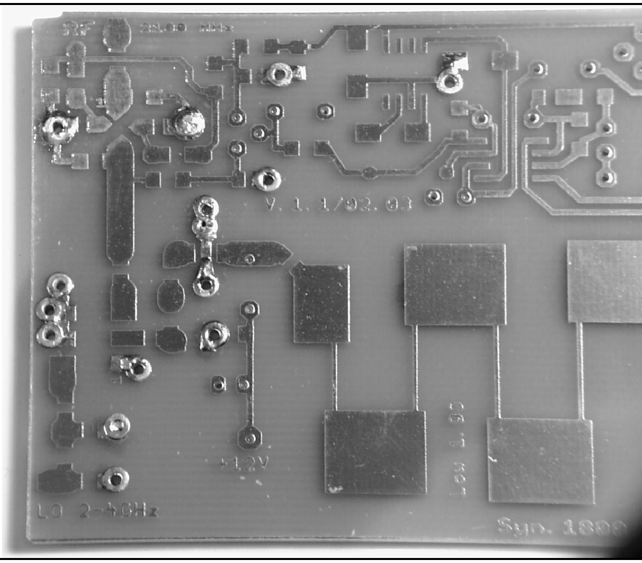


Fig 34: Example of through hole plating.

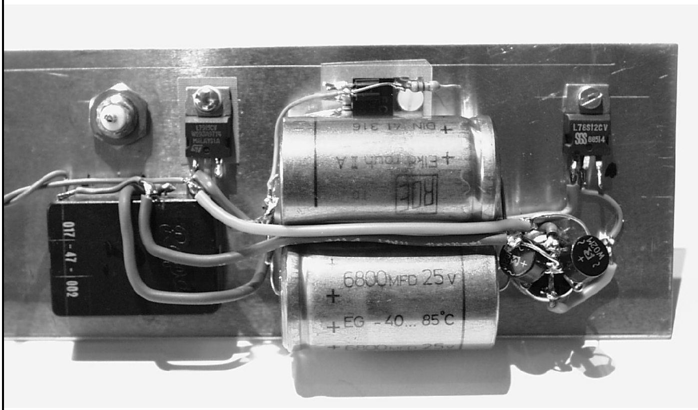


Fig 35: Power supply components mounted on the rear panel of the unit.

rivets (cable sheaths). This also applies to the MMIC's. A large through plating is positioned at each connection to earth of the ERA3. The through platings are already present on industrially manufactured boards.

4.1. Instructions on through plating

For high-frequency circuits it is very important to make sure the connections to earth are good. On a double sided board, the underside (earthing surface) is the only correct earth for high frequency use. If the earth needs to be on the topside of the board, make sure there is a good, low inductance through plating. It is important in this context that the shortest route earths as many "surfaces" as possible. This can be achieved by manufacturing several small through platings or one big through plating. The use of relatively large compression rivets has proved efficacious for DIY etched boards. I use cable sheaths made from copper for this purpose, which are available at reasonable prices for 0.5 / 0.75 square cable. The external diameter is then 1.4 / 1.8mm. The head of the cable sheaths is knocked flat before being soldered into the board. This can be done simply, by generating an appropriate hole in a piece of metal, inserting the cable sheaths into this hole and knocking the head flat with a light blow from a hammer. The cable sheaths prepared in this manner are then pressed into the board and soldered above and below. The ends left over on the bottom side are then ground off or filed off. Fig 34 shows the through platings.

4.2 Incorporation into a housing

If a small housing is used, as for the prototype, then a small fan (CPU fan, as used in computers) should be built into the rear panel. The fan can be set to run slowly and thus gently by means of a suitable series resistor. This ensures uniform temperature conditions and thus stable values for the frequency and the output.

4.3. Power supply

It is very advantageous if the transformer used is not placed in the signal generator housing, since even well screened transformers transfer a 50Hz hum to the circuit. The author uses a transformer with connecting cables which deliver 2 x 12V AC voltage at 1A. The rectification and stabilisation then takes place in the apparatus itself. Fig 35 shows the bridge rectifiers, voltage regulator and filter electrolytic capacitor, which are mounted directly on the rear panel of the housing. For this version of the power supply, a two pole switch must be used.

Table 1: Interconnections between assemblies.

Micro-controller	Mixer Board	Port	Plug	Pin	Function
K17	2	P0.1	K3	1	DAC clk
K17	3	P0.6	K3	2	DAC data
K17	4	P0.7	K3	3	DAC load
Micro-controller	**PLL/DDS board**	**Port**	**Plug**	**Pin**	**Function**
K4	8	P3.7	K4	3	PLL LE
K4	7	P3.6	K4	2	PLL data
K4	6	P3.5	K4	1	PLL clk
K7	1	P2.0	K6	3	DDS soldering pad
K7	2	P2.1	K6	2	DDS data
K4	6	P3.5	K6	1	DDS clk
K4	4	P3.3	K2		MUX/PLL error
K4	5	P3.4	K7		Hi/Lo for PLL
K4	1	P3.0			RF On/Off switch
K5	8	P1.7			RF On/Off button

4.4. Inter-connecting assemblies

Table 1 and Fig 36 show the interconnections and will be of assistance for wiring up the assemblies.

5.

Putting into operation and calibration

The YIG driver must be set first. At this point, the tune voltage, which comes from the DA converter, has not yet been connected to the YIG driver. Nor has the VCO regulator voltage, which comes from the PLL.

The calibration on the YIG driver then proceeds step by step.

1 Connect spectrum analyser or frequency counter to the output.

2 Turn “Fmin” potentiometer all the way to the right.

3 Turn “Fmin” potentiometer all the way to the left, until a reading of approximately 25MHz appears at the output.

4 Set the Syn 1800 signal generator to 10MHz and connect the tune voltage from the DA converter to the YIG driver. The frequency must now increase to approximately 35MHz.

5 Use “Fmin” to select 35MHz.

6 Set Syn 1800 signal generator to 1010MHz and use “Fmax” to calibrate at approximately1035MHz.

7 Now connect the regulator voltage from the PLL to the VCO. The PLL should now engage and the output frequency is then 1010MHz.

8 If everything has gone right so far, measure the regulator voltage on the VCO again and use “Fmin” to select approximately 3.8 to 4.0V.

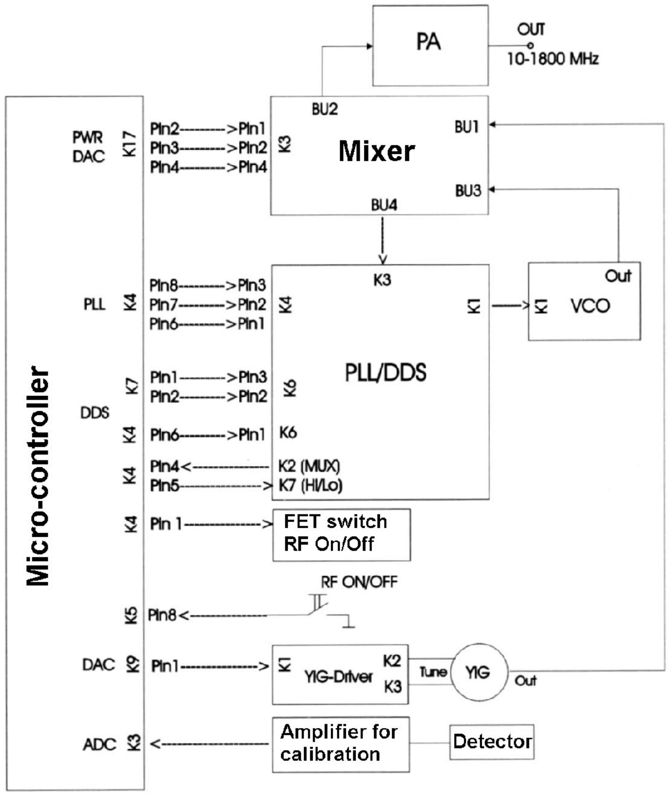


Fig 36: Diagram showing the interconnections between the various assemblies.

Finally, the calibration function (PWR) must be carried out for the power, and immediately afterwards the fully automated calibration function (FRQ) can be carried out for the digital frequency response correction. Both functions are described in greater detail below.

Help

- Should the PLL not engage in the range between 10 and approximately 100MHz, check whether the Hi/Lo switching for the PLL reference frequency is functioning correctly.
- Should the PLL not engage at the top end of the band, check the regulator voltage. Re-balance if necessary, using “Fmax”. (3.8 – 4.0V)
- Should the PLL not engage at 10MHz, check the regulator voltage on the VCO. Increase it to 4.0 to 4.2V if necessary.

Frequency calibration

After a warm up period of approximately 15 minutes, the output frequency can be set, using the R5 trimmer, at the TXCO, with the help of a precise frequency counter. A fine adjustment can also be carried out later using software.

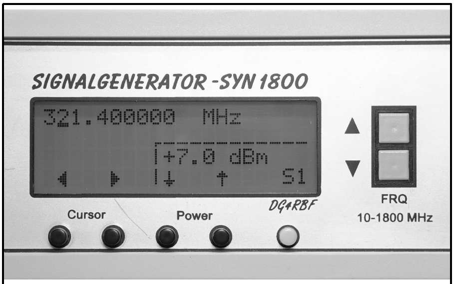


Fig 37: Display showing the five operating buttons.

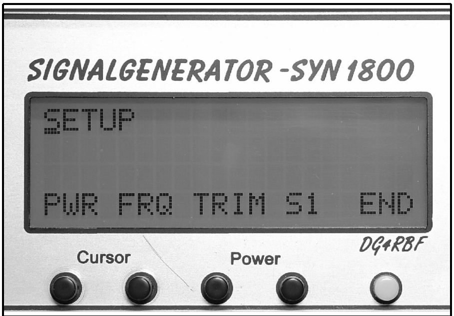


Fig 38: Display showing setup menu.

6.

Operation and functions of software

The display used has 4 lines, so that the lowest line can be used for annotating buttons positioned beneath it.

Fig 37 shows the display with the 5 operating buttons below the display and the two separate buttons near the display.

The first two buttons below the display can be used to move the cursor (in the diagram is under the 2) right or left. The frequency buttons (near the display) can then be used to change the corresponding position of the frequency. Since the frequency setting is programmed with an overrun, the frequency can be adjusted simply and quickly.

The next two buttons below the display are used to adjust the output in 0.1dB steps. Here a progressive adjustment speed has been used, which again makes it easier to operate. The fifth button (S1) has two functions: a short press means the high/low switching for the PLL is manually altered. If this button is pressed for approximately 3 seconds the display will change to the setup menu, which can be seen in Fig 38.

Setup functions

- PWR = power calibration (and balancing of R34)
- FRQ = fully automatic frequency calibration
- TRIM = fine trim for precision of frequency
- S1 = switchover parameters for S1 /High/Low switching of PLL
- END = end of setup menu

6.1 Power calibration

Before the calibration routines are carried out, the equipment should be allowed to warm up for about 15 minutes.

Set the frequency to 100MHz and activate the button [PWR] in the setup menu. The message: CAL Min (R34) appears. Now you must connect an mW meter to the output of the signal generator, using R34 on the mixer board set the minimum level (approximately -10dBm to -5dBm). Then activate the button [SET].

Now the power is calibrated in 1dB steps between +13dBm and 0dBm, with the mW meter remaining connected for this purpose.

Now the message: CAL +13dBm XXXX appears

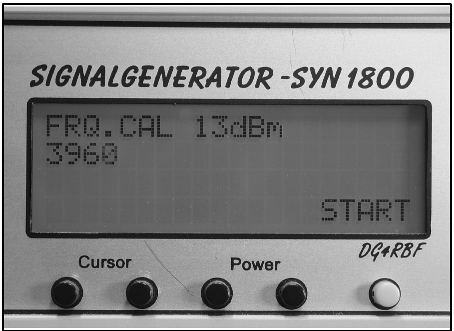


Fig 39: Display for automatic frequency calibration.

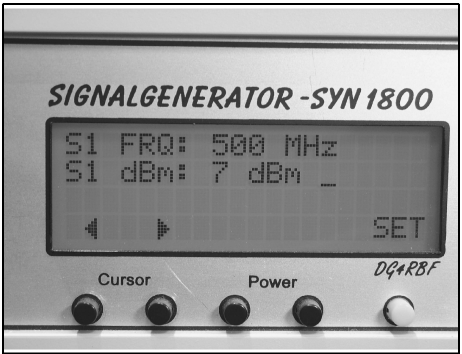


Fig 40: Display showing High/Low switching parameters.

Using the cursor button [< >], set the power to +13dBm. The 4 digit number, which is displayed behind +13dBm, should lie somewhere between 3000 and 3500. Should the value lie outside this range, the voltage divider after the DA converter (LTC1257) should be adjusted. If +13dBm is selected, this is confirmed with the button [SET]. Next,: CAL +12dBm XXXX appears. Set the power level to the pre-set power of +12dBm, once again using the cursor button [< >], and confirm using [SET]. Repeat this procedure down to 0dBm.

6.2 Fully automatic frequency calibration

Immediately after carrying out the power calibration for +13dBm to 0dBm, you should carry out the fully automatic frequency calibration. Connect up a good diode detector to the output of the signal generator and connect the DC voltage output of the detector to the input of the DC amplifier (OPV) on the rear panel of the equipment. When the button [FRQ] is activated in the setup menu, the display shown in Fig 39 appears. The four-digit number that is displayed in the second line is the value for the AD converter. Set the OPV amplification so that a value between 3900 and 4000 is displayed. If the [START] button is pressed, the fully automatic frequency response calibration is started. You can follow the process on the display. The complete procedure lasts approximately 25 minutes. Some more detailed information on the significance of the values displayed during the calibration procedure:

- 1st line: shows the theoretical value for the ADC at the corresponding power level
- 2nd line: shows the instantaneous frequency
- 3rd line: shows the actual value for the ADC
- 4th line: shows the difference detected, which is saved in the EEPROM as a correction value.

The process is terminated automatically and the system returns to normal mode. Every time this routine is carried out, the pre-setting for the high/low PLL switching is subsequently set to +8dBm.

6.3 Trim - fine trim for precision of frequency

This function can be used to fine trim the output frequency. The value is set using the cursor button and confirmed with [SET].

6.4 Switching parameter for high/low switching of PLL

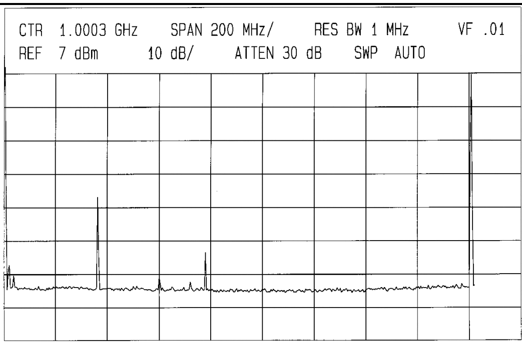


Fig 41: Output signal plot of the 10 - 1800MHz synthesised signal generator.

The parameters for the high/low switching of the PLL can be selected here if necessary The switching frequency can be selected first, using the cursor button, and confirmed using [SET]. Next the second line shows the power reading at which switching should take place. This can be selected in the same way. See Fig 40.

6.5 End of setup menu

Pressing the button [END] will end the setup menu.

6.6 Digital Level ON/OFF

If the fifth button (S1) is pressed and held down, the digital power correction can be switched on and off alternately.

6.7 Reset function

If the first cursor button is pressed and held down, the default parameters will return. But the calibration data in the EEPROM are not deleted.

6.8 Signal plots

Figs 41 an 42 show harmonics and signal quality at various frequencies from 100MHz to 1800MHz.. The plots were carried out using an HP8569A spectrum analyser.

6.9 Boards

If there is sufficient demand, the author will have some boards manufactured professionally. Individual YIG oscillators and VCO's are also still available. Enquiries by E-Mail please to: Info@DG4RBF.de

Any modifications or improvements can be found on the author's homepage. www.DG4RBF.de

The author has been using the signal generator for approximately 1 year and it works perfectly.

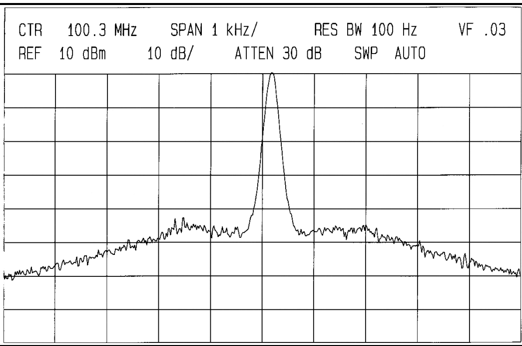


Fig 42: Output signal plot of the 10 - 1800MHz synthesised signal generator.

Table 2: Parts list for micro-controller.

IC1	24C64
IC2	LTC1286
IC3	AT89C55
IC4	7805
IC5	LTC1257
R1	5KΩ
R2,7,8	10Ω
R3	10KΩ
R4	1KΩ
R5	8 x 10KΩ
R6	100Ω
R12,13	10Ω
C1	3.3µF
C2,9,13	100nF
C3,4	27pF
C5,7,8	10µF
C6	2.2nF
C10,11	10µF
C12	0.1µF
C14	10µF
K1	K1 x 16
K2,3,7,9	K1 x 2
K4,5	K1 x 8
K6,22	K1 x 3
K8	K1 x 5
K12,18,23	K1 x 2
K16,20	K2 x 5
K17,21	K1 x 4
LCD1	LCD20 x 4
Q1	18.432MHz
SW-11	Conrad #705115
4 x black caps Conrad ~705115	
1 x Yellow cap Conrad # 705078	

Table 3: Parts list for VCO.

IC1	78L09
T1	BFP420
VC01	VCO
R1	390Ω
R2	22KΩ
R3	1.5KΩ
R4	22Ω
C1	100pF
C2	2.2pF
C3,5	5pF Sky
C6,8	10µF
C7	1µF
C9,12	1nF
C10	5pF
C11	2.7pF
L1	0.1µH
K1,2	K1 x 1
BU1	SMA with cable or semi ridgid

Table 4: PA parts list.

IC1	GAL-6
R1	47Ω
R2	39Ω
C1,2,3	1nF
C4	1µF
BU1,2	SMA
K1	K1 x 1

Table 5: PLL/DDS parts list.

IC1	ADF4112
IC2,5,6	78L05
IC3	TL431 (2.5v)
IC4	AD9850
IC7,8,9	MSA886
T1	BF324
T2	IRF9520
T3	2N7000
R1,19	4.7K
R2,14,25,26	51
R3	3.3K
R4,9,10,29	1K
R5	680
R6	220K trimer
R7,12,13	22K
R8	470K
R11	24

R15	150
R16,17,18	100K
R20	1.5K
R21	6.8K
R22	470
R23,24	150
R27	47K
R28	100K
R30	22
C1	100pF
C2,30,31	1nF
C3	6.8nF
C4	0.047F
C5	56pF
C6	100pF
C7,24,34,35	4.7nF
C8,9,36,37	10F
C10,11,12	2.2nF
C13,14,15	10F
C16	22nF
C17,20	270pF
C18,19	560pF
C21,22,23,32,33	10nF
C25	4.7pF
C26	2.2pF
C27,28	45pF trimer
C29	10pF
C38	1F
C39	100nF
L1,2,3	1H
L4	10H
L5,6	0.47H
TCX01	TCXO 13.00MHz
D1	LED
F1	SFE10.7MA
K1,2,3	K1 x 1
K4,5,7	K1 x 4
K6	K1 x 3

Table 6: YIG parts list.

IC1	TL431 (2.5v)
IC2	OP27J
Y1	BDX54B
T2	2N7000
D1	IN4148
R1,9,12	1K
R2,11	10K
R3,4	22K
R5	4.7K
R6	47K
R7	3.9K
R8	15
R10	2 (see text)
C1	10nF
C2,3	1.5F
C4	0.22F
C5	100F
C6	470F 6.3v
C7	100nF
C8	0.1F
C9,10	1F
C11	10F
K1-6	K1 x 1
OSC1	YIG 2-4GHz

7.0

Parts lists

Tables 2 - 6 show the parts lists for the main assemblies

8.0

Literature references

[1] Author’s homepage:
www.DG4RBF.de

[2] Author’s E-mail address:
Info@DG4RBF.de

[3] Analog Devices data sheet
www.analog.com

Henning-Christof Weddig, DK5LV

A modern 50/28MHz converter

The author presented some of his reflections on the design of very linear front ends for the VHF and UHF bands in two papers read at the Weinheim VHF Congresses, [1], [2]. The author came third in the radio equipment section of the DIY competition at the Weinheim VHF Congress in 2003 with a preliminary version of the circuit described here.

1. The Concept

The good inter-modulation test results for the HMJ-5 mixer by Watkin Johnson for another project played a decisive role when it came to a mixer for this project. The satisfactory use of the low noise RF 2360 broad band amplifier from RF Microdevices as an LNA [9] was likewise a crucial factor in the decision to try out this component in a 50MHz converter.

Many texts have already been published on the subject of 50MHz converters (e.g. VHF Communications [3], and *Funkamateur* [4]). But these units are only constructed with the standard Schottky diode mixers (class 7dBm or 17dBm) and with a Dual gate MOSFET [3] or a barrier layer FET in a gate circuit [4] at the front end.

When the converter is used in fixed operation, the front end (LNA) should be mounted directly at the base of the antenna, and only the actual converter should be in the shack, i.e. near the receiver. For this reason, the converter presented here is made up of two assemblies:

- The external unit, a pre-amplifier
- The internal unit, the converter.

Not having a special licence for 50MHz, I shall describe only the receive converter here. I am planning to expand the system to include a transmit converter.

2. Specimen equipment data

2.1. Pre-amplifier data

- Noise factor F: < 2dB (not measured due to lack of measuring equipment)
- Amplification G: 18.3dB, -0.2dB (transmission)

- Input intercept point: +18dBm (P_{in} = 2 * -12dBm, d_3 = 58.7dB)
- Output intercept point: +36dBm (calculated from input intercept point)
- 1dB compression point: +25dBm
- Power supply: 12-15V; 150mA

2.2. Converter data

- Noise factor F: approximately 8dB (simulation)
- Amplification G: -7.5dB (simulation), -8.4dB (measured)
- Input intercept point: +41dBm (simulation), +30.5dBm (measured) (P_{in} = 2 * 0dBm, d_3 = 61 dB)
- Power supply.: 12 -15V; approximately 140mA

2.3. Data for combination of LNA and converter

- Noise factor F: 4dB (noise factor of amplifier 10dB corresponding to – 110dBm for 20dB SINAD of amplifier for SSB bandwidth)
- Sensitivity -116dBm (noise factor of amplifier 10dB) (SSB bandwidth)
- Amplification G: 10.2dB, measured without attenuation of coax cable in between)
- Input intercept point: +14.4dBm (P_{in} = 2 * -21dBm, d_3 = 70dB)
- Output intercept point: +25dBm (calculated from input intercept point)

3. System simulation

In system simulation a system, e.g. a complete receiver, is divided up into assemblies, such as pre-amplifier, mixer, filter, etc.

The following data concerning the individual assemblies are from the data sheet specifications or from test data:

- Noise factor
- 1dB compression point
- Intercept point

The values for the entire system can be determined from this data. By varying the parameters of individual assemblies, the user can easily study the influence of specific parameters on the entire system without having to assemble the circuit and make all the measurements.

3.1. LNA system simulation

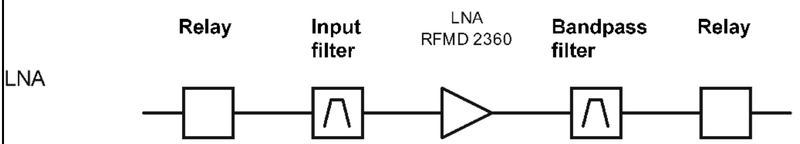
The IC RF 2360 (from RF Microdevices), which has proved its worth in another project, is used for the amplifier in the LNA [9]. Its upper limiting frequency is 1.5GHz, so strong out of band signals must be kept away from the amplifier IC by filters.

The filter in front of the amplifier should display the lowest possible insertion loss, since this has a direct influence on the noise factor of the entire system. An attenuation of 0.5dB appears achievable.

The LNA is connected to the signal path by two coax relays, and a value of 0.2dB has been assumed for the transmission loss of each relay for the simulation.

A low pass filter at the output of the LNA increases the attenuation as the frequencies become higher. For the RF 2360, the data sheet specifications [15] (F = 1.2dB, G = 20dB, $OPIP_3$ = +36dBm, P_{1dB} = 24dBm) were used.

The intercept point for each of the passive assemblies (coax relay, filter) was



	Relay	Input filter	LNA	Bandpass filter	Relay	Total
NF (dB)	0.20	0.50	1.20	0.50	0.20	1.91
Gain (dB)	-0.20	-0.50	20.00	-0.50	-0.20	18.60
OIP3 (dBm)	100.00	100.00	37.20	100.00	100.00	36.50
OP1dB (dBm)	100.00	100.00	24.00	100.00	100.00	23.30
IP3+ (dBm)	0.00	0.00	60.34	0.00	0.00	
NF+ (dB)	0.13		1.20		0.00	
Po (dBm)	-118.20	-118.70	-98.70	-99.20	-99.40	

Input Pwr (dBm) -118.00 System Temp (K) 290.00

Modulation: Custom

System BW (MHz)	0.00	MDS (dBm)	-138.27	Input IP3 (dBm)	17.90
S/N (dB, Actual)	20.27	S/N (dB, Req'd)	20.00	Output IP3 (dBm)	36.50
Srce Temp (K)	290.00	Sens. Loss (dB)	0.00	OIM3 (dBm)	-371.20
Te Eff. (K)	159.75	Sensitivity (dBm)	-118.27	ORR3 (dB)	271.80
SFDR3 (dB)	104.11	G/T (dB/K)	-16.53	IRR3 (dB)	90.60

Fig 1: System simulation for the LNA of the 28/50MHz converter.

given a value of +100dBm. This value is for real filters, which are assembled using ferrite materials. This is unrealistic, but can be used as an approximation for a starting point at low input levels.

The system simulation of the LNA can be seen in Fig. 1. The data obtained for SSB operation (bandwidth 2.4kHz) can be found in column 1 of Table1.

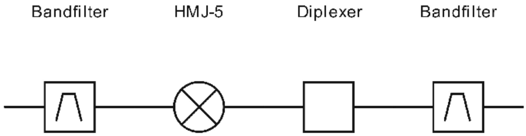
3.2. System simulation of converter

The converter consists of the following assemblies:

- Input filter (insertion loss = noise factor = 3dB)
- HMJ-5 mixer (data sheet specifications: mixer loss 6dB, noise factor 7dB, $IPIP_3$ = +38dBm; OPIP3 = IPIP3 + G =+38dBm – 6dB =

Table 1: Simulation data for the LNA, Converter and both.

Simulation data	LNA	Converter	Both
Noise figure F	1.91dB	12.98dB	3.41dB
Input for 20dB SINAD	-118.27dBm	-107.2dBm	-116.76dBm
Amplification G	18.6dB	-12.5dB	3.1dB
Input intercept ($IPIP_3$)	17.9dbM	41.0dBm	16.44dBm
Output intercept ($OPIP_3$)	36.5dBm	28.5dBm	19.45dBm
Intermod. ($SFRD_3$)	104.11dB	112.13dB	102.14dB



	Bandfilter	HMJ-5	Diplexer	Bandfilter	Total
NF (dB)	3.00	7.00	0.50	3.00	12.98
Gain (dB)	-3.00	-6.00	-0.50	-3.00	-12.50
OIP3 (dBm)	100.00	32.00	100.00	100.00	28.50
OP1dB (dBm)	100.00	16.50	100.00	100.00	13.00
IP3+ (dBm)	0.00	60.74	0.00	0.00	
NF+ (dB)		2.24	0.22		
Po (dBm)	-110.00	-116.00	-116.50	-119.50	

Input Pwr (dBm)	-107.00	System Temp (K)	290.00		
Modulation: Custom					
System BW (MHz)	0.00	MDS (dBm)	-127.20	Input IP3 (dBm)	41.00
S/N (dB, Actual)	20.20	S/N (dB, Req'd)	20.00	Output IP3 (dBm)	28.50
Srce Temp (K)	290.00	Sens. Loss (dB)	0.00	OIM3 (dBm)	-415.50
Te Eff. (K)	5463.46	Sensitivity (dBm)	-107.20	ORR3 (dB)	296.00
SFDR3 (dB)	112.13	G/T (dB/K)	-27.60	IRR3 (dB)	98.67

Fig 2: System simulation for the converter of the 28/50MHz converter.

+32dBm), P_{1dB} = 16 dBm (assumed value, not specified in data sheet)

- diplexer insertion attenuation = noise number = 0.5dB)
- output band filter (insertion attenuation = noise number = 3dB)

There are not many details in the literature concerning the noise factors of passive mixers. For Schottky diode mixers, the noise factor should be approximately 0.5dB higher than the mixed attenuation.

The HMJ- 5 is a passive FET mixer; on the basis of the data sheet specifications, a value was assumed for the noise factor which was 1dB higher than the mixed attenuation.

According to the manufacturer's specifications, the intercept point for Schottky diode ring mixers from Mini Circuits can be calculated as being 10 to 15dB higher than the 1dB compression point.

No 1dB compression point is specified for the HMJ-5 from Watkin Johnson, so it was assumed to be 10dB below the intercept point.

The system simulation for the converter can be seen in Fig. 2. The data obtained (sensitivity and inter-modulation free dynamic range [SFRD3] in SSB mode; bandwidth 2.4kHz) can be seen in column 2 of Table 1.

The results for the two intercept points are amazing: the output intercept point is lower than the input intercept point! But since the amplification of the converter is negative, and the output intercept point is formed by adding the input intercept point (in dB) to the amplification of the converter, this apparent contradiction can be explained.

If we compare the $OPIP_3$ of the LNA with the $IPIP_3$ of the converter, we see that the converter has a lower value. The

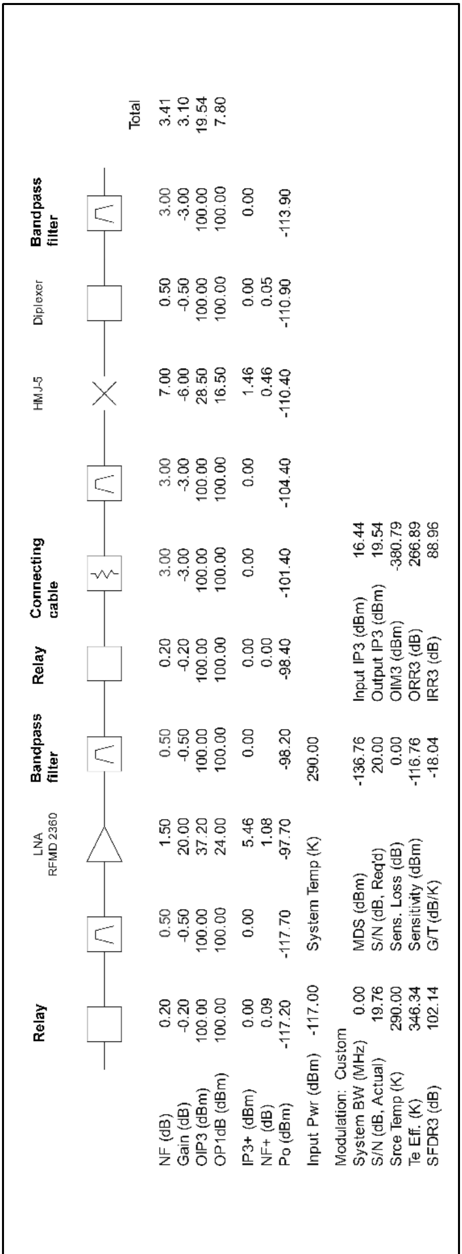


Fig 3: System simulation for the complete 28/50MHz converter.

converter thus determines the total IP.

3.3. System simulation for the combination of the LNA and the converter

The system simulation of the inter-connected assemblies, the LNA and the converter, can be seen in Fig. 3. An attenuation of 3dB was assumed for the coax cable between the two assemblies. The entire system thus obtains the values in column 3 of Table 1.

The intercept point of the amplifier in the LNA accounts for the biggest fraction (IP_3+ = 5.46dBm) of the total intercept point.

If this converter is inter-connected with an amplifier (the receiver of a transceiver) to make a total system, the receiver must have a higher input intercept point than the $OPIP_3$ of the converter, so that the total system is not degraded any further.

If the following data are assumed for the transceiver:

- noise factor F: 10dB
- $IPIP_3$: +30dBm
- amplification G: 0dB

we obtain values for the entire system corresponding to Fig. 4 and column 1 of Table 4.

Note: The amplification for a real receiver is normally greater than 0dB, but this value was specified as being this low so that the $OPIP_3$ of the total system could be seen more easily.

Although the total intercept point has only degraded by 3dB, the sensitivity and the inter-modulation free dynamic range drop by 5dB.

If the input intercept point of the trans-

Table 2: Data of input intercept values for the transceiver amplifier

$IPIP_3$ of transciver amplifier dBm	Total system $IPIP_3$ dBm
18	12.94
19	13.48
20	13.96
21	13.39
22	14.76
23	15.07
24	15.34
25	15.57
26	15.76
27	15.92
28	16.05
29	16.15
30	16.24

Table 3: Data of noise figure values for the transceiver amplifier

Noise figure of Transceiver amp. dB	Total system Noise figure dB
1	3.81
2	4.12
3	4.48
4	4.90
5	5.38
6	5.91
7	6.50
8	7.14
9	7.84
10	8.58
11	9.36
12	10.18
13	11.03

ceiver is further reduced, the total IP deteriorates in accordance with Table 2.

We see that no dramatic deterioration in the total IP occurs until the $IPIP_3$ of the transceiver is in the order of magnitude of the input $IPIP_3$ of the LNA and the converter combined.

The considerable increase in the total noise factor is also unsatisfactory. Table 3 shows the interconnection, with the total noise factor as a function of the noise factor of the transceiver.

Here too, we can see a dramatic deterioration in the total noise factor if the noise factor of the amplifier exceeds that of the system combining the LNA and the converter. This result is amazing at first glance, for it is generally assumed (see article by DJ7VY in [15]) that, due to the high amplification of the LNA (100 x power amplification), the following stages have only a slight effect (1/100) on the noise factor of the total system!

This statement is correct for the interconnection of the LNA and the converter. Why does what is still a high noise factor for the transceiver have such an effect on the total noise factor?

If we look at the input level associated with each individual noise factor (e.g. for 20dB SINAD, SSB-bandwidth = 2.4kHz), a noise factor of 3dB means an input signal of -117dBm, a noise factor of 13dB then corresponds to a signal of -107dBm = 1µV / 50Ω.

Table 4: Simulation data for the LNA and transceiver amplifier, "new" converter and both.

Simulation data	LNA, converter & transceiver amp.	"New" converter	Both
Noise figure F	10.59dB	8.31dB	4.34dB
Input for 20dB SINAD	-109.58dBm	-111.86dBm	-115.83dBm
Amplification G	3.1dB	-7.50dB	12.8dB
Input intercept ($IPIP_3$)	16.75dBm	35.0dBm	11.7dBm
Output intercept ($OPIP_3$)	19.85dBm	27.50dBm	24.50dBm
Intermod ($SFRD_3$)	97.55dB	111.24dB	98.35dB

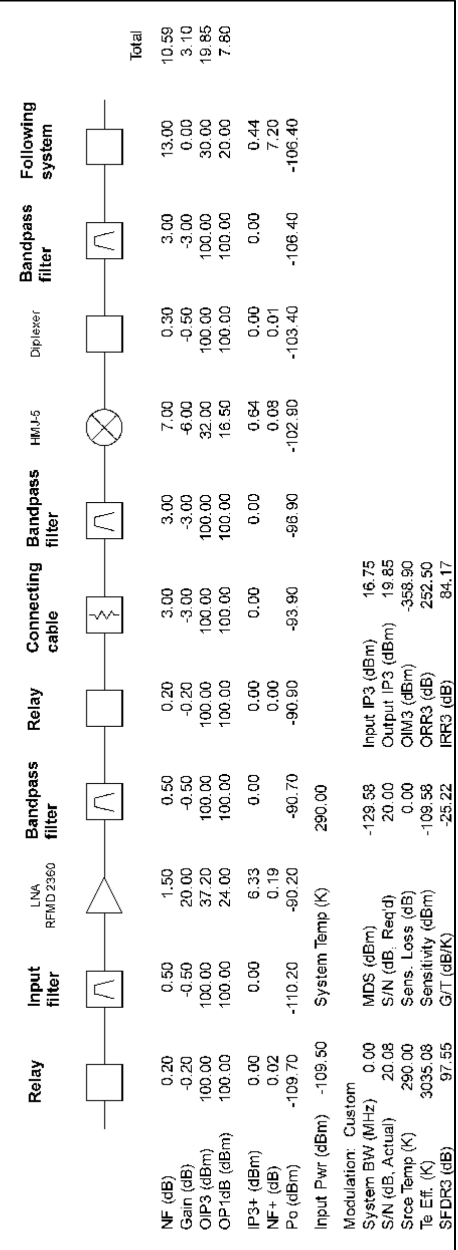


Fig 4: System simulation for the complete 28/50MHz converter.

So if the system consisting of the LNA, the converter and the transceiver should generate a total noise factor of 3dB, the amplification of the LNA and the converter should be at least 10dB!

The amplification of the system consisting of the LNA and converter, however, is only 3.1dB, since all the stages after the LNA weaken the signal.

So it seems natural to assume that an additional amplifier could be inserted between the converter and the transceiver to increase the amplification again. Even if this amplifier were completely free from inter-modulation, it would increase the requirements on the intercept point of the transceiver!

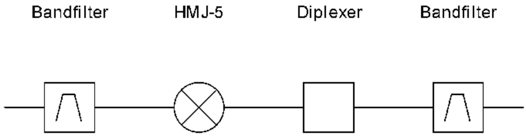
As an experiment, an amplifier (F = 3dB, G = 4dB, $OPIP_3$ = 29dBm) is connected into the converter combination between the diplexer and the output band filter. The noise factor of the total system, including the booster, is reduced from 8.58dB by approximately 2dB to 6.37dB, but the total $IPIP_3$ is reduced from 16.24dBm to 14.2dBm ($IPIP_3$ of amplifier +30dBm).

With an $IPIP_3$ for the amplifier of +20dBm, we have a deterioration of the total $IPIP_3$ to 11dBm.

We thus recognise that the improvement in sensitivity due to the loss of the intercept point has to be paid for.

If you wish to avoid this disadvantage and, if at all possible, to manage without an additional amplifier at the output of the mixer in the converter, the attenuation values of the band filter must be reduced. This cannot be paid for with these band filters, in view of the basic Q of the coils (80 - 100), except through a correspondingly high bandwidth.

The attenuation of the feed cable, at 3dB, appears to be set decidedly high. If this is



	Bandfilter	HMJ-5	Diplexer	Bandfilter	Total
NF (dB)	0.50	7.00	0.50	0.50	8.31
Gain (dB)	-0.50	-6.00	-0.50	-0.50	-7.50
OIP3 (dBm)	100.00	28.50	100.00	100.00	27.50
OP1dB (dBm)	100.00	16.50	100.00	100.00	15.50
IP3+ (dBm)	0.00	63.97	0.00	0.00	
NF+ (dB)		4.74	0.36		
Po (dBm)	-112.50	-118.50	-119.00	-119.50	

Input Pwr (dBm)	-112.00	System Temp (K)	290.00		
Modulation: Custom					
System BW (MHz)	0.00	MDS (dBm)	-131.86	Input IP3 (dBm)	35.00
S/N (dB, Actual)	19.86	S/N (dB, Req'd)	20.00	Output IP3 (dBm)	27.50
Srce Temp (K)	290.00	Sens. Loss (dB)	0.00	OIM3 (dBm)	-413.50
Te Eff. (K)	1676.20	Sensitivity (dBm)	-111.86	ORR3 (dB)	294.00
SFDR3 (dB)	111.24	G/T (dB/K)	-22.94	IRR3 (dB)	98.00

Fig 5: System simulation for the "new" 28/50MHz converter.

replaced by a cable attenuation of 2dB (e.g. approximately 30m RG 213) and an insertion attenuation of 0.5dB for each band filter and for the diplexer, we then obtain the following results for the system calculation for the new converter; see Fig. 5 and Table 4, column 2.

If the new converter is connected to the LNA and the transceiver, the system simulation (Fig. 6) gives us the data in Table 4, column 3. The band filter and connection cable attenuation values are set lower, and the input level is selected in such a way that, for SSB bandwidths (2.4kHz), 20dB SINAD is obtained.

In spite of the amplification for the LNA and the converter of 12.8dB, we only obtain a level of sensitivity which is lower than what we would expect to obtain from the receiver (-107dBm) and the increase in amplification (12.8dB). However, the reason lies in the fact that the LNA and converter assemblies are not noise-free, and their noise contributions reduce the sensitivity.

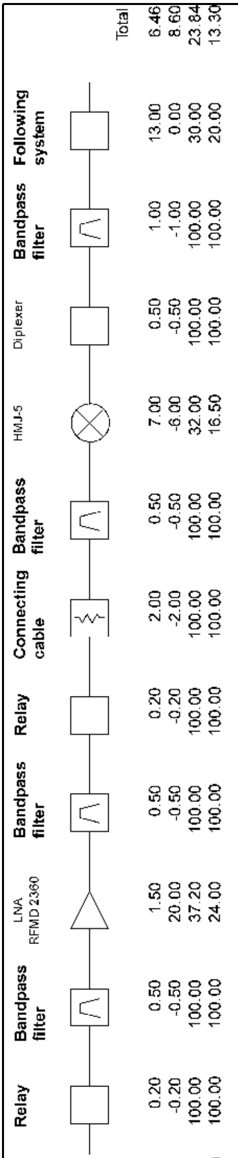
4. Description of circuit

4.1. LNA

Fig. 7 shows the circuit diagram for the amplifier assemblies (LNA).

To avoid any degradation of the high level signal strength performance of the converter, a low noise broadband amplifier - type RF 2360 – is used, as in [9].

Provision must be made for selection at the input and output, so that the system as a whole (LNA, converter and amplifier) is not unnecessarily burdened with out of band signals that are too strong (shortwave, VHF range, etc.).



	Relay	Bandpass filter	LNA RFMD 2360	Bandpass filter	Relay	Connecting cable	Bandpass filter	HMJ-5	Diplexer	Bandpass filter	Following system	Total
NF (dB)	0.20	0.50	1.50	0.50	0.20	2.00	0.50	7.00	0.50	1.00	13.00	6.46
Gain (dB)	-0.20	-0.50	20.00	-0.50	-0.20	-2.00	-0.50	-6.00	-0.50	-1.00	0.00	8.60
OIP3 (dBm)	100.00	100.00	37.20	100.00	100.00	100.00	100.00	32.00	100.00	100.00	30.00	23.84
OP1dB (dBm)	100.00	100.00	24.00	100.00	100.00	100.00	100.00	16.50	100.00	100.00	20.00	13.30
IP3+ (dBm)	0.00	0.00	3.39	0.00	0.00	0.00	0.00	1.06	0.00	0.00	1.20	
NF+ (dB)	0.05		0.50		0.00			0.10	0.01		3.88	
Po (dBm)	-114.20	-114.70	-94.70	-95.20	-95.40	-97.40	-97.90	-103.90	-104.40	-105.40	-105.40	

Input Pwr (dBm)	-114.00	System Temp (K)	290.00		
Modulation: Custom					
System BW (MHz)	0.00	MDS (dBm)	-133.71	Input IP3 (dBm)	15.24
S/N (dB, Actual)	19.71	S/N (dB, Req'd)	20.00	Output IP3 (dBm)	23.84
Srce Temp (K)	290.00	Sens. Loss (dB)	0.00	OIM3 (dBm)	-363.88
Te Eff. (K)	993.94	Sensitivity (dBm)	-113.71	ORR3 (dB)	258.48
SFDR3 (dB)	99.30	G/T (dB/K)	-21.09	IRR3 (dB)	86.16

Fig 6: System simulation for the complete 28/50MHz converter.

The input filter was calculated and simulated with the help of the “RFSim99” program as a 20MHz wide Butterworth filter.

Compared with Chebyshev filters, Butterworth filters are easier to calibrate, since they only have to be calibrated to the maximum of the transmission curve and not, in addition, to the specified return loss and/or ripple in the transmission range.

The filter circuit with the original component values can be seen in Fig. 8; the simulation result can be seen in Fig. 9. The insertion loss at the mean frequency is consequently only 0.2dB.

The calculated component values can very easily be achieved; individual helical filter coils (Neosid 511830) can be used for the inductances of the parallel resonant circuits.

If the bandwidth is reduced to 10MHz, the inductances of the parallel circuits are reduced by half, the capacitances are doubled; the inductance of the series circuit is doubled, and the capacitance of the series capacitor is halved. However, the realisation of this filter appears to be too difficult.

A test assembly of the 20MHz wide filter on tinplate produced a low insertion loss of 0.5dB; a printed circuit board assembly gave an insertion loss of 0.65dB (Figs. 10 and 11).

In order to obtain better attenuation on the lower filter flank, the mean frequency of the filter was pushed up compared to the simulation, and the return loss in the transmission range was expanded.

A Neosid 5036 coil was used as the series coil of the filter in the specimen equipment. But the coil’s core had to be screwed right in. It is better to use type 5048 (rated value < 1µH), as shown in

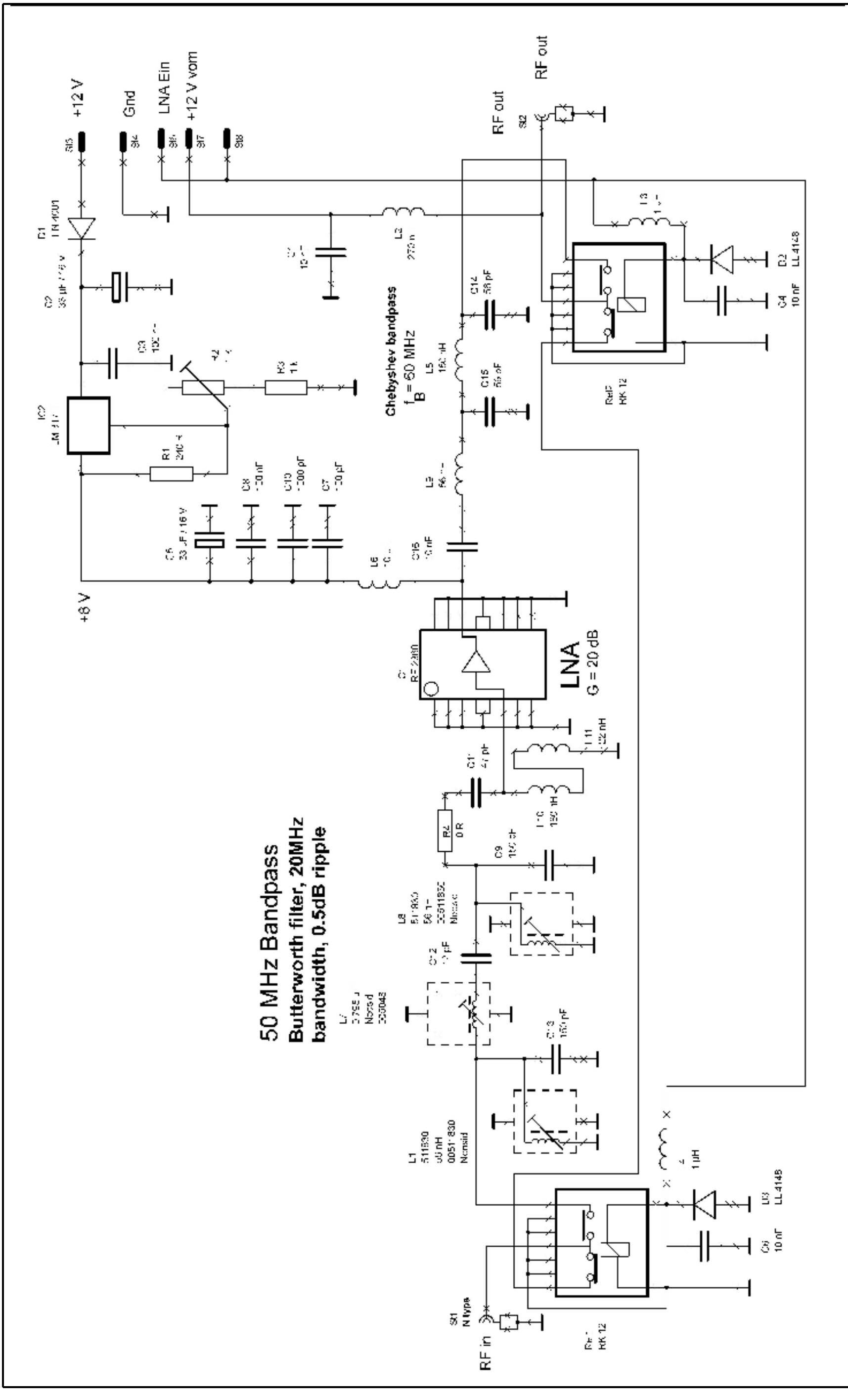


Fig 7: Circuit diagram of masthead amplifier for the 28/50MHz converter.

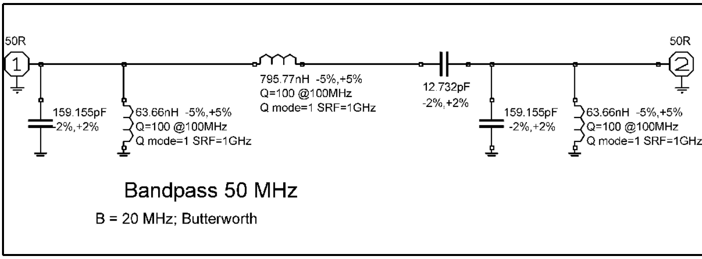


Fig 8: Circuit diagram of the 50MHz bandpass filter.

the circuit diagram (Fig. 7). A test on a specimen Neosid 5048 coil using an inductance meter (R&S LARU) revealed that the desired value of 795nH can be obtained easily.

The low pass filter at the output of the LNA was calculated for a reference frequency of 60MHz and for Chebyshev characteristics. An SMD coil (Q approximately 30) can be used for the inductance, without affecting the insertion loss too badly. The simulation of the low-pass filter can be seen in Figs. 12 and 13.

For transverter mode to be used, or in order not to overload the subsequent amplifier when the input signals are strong, the LNA can be switched into the signal route using coax relays. This is why connections S16 and S18 are provided on the printed circuit board.

If there is a remote power supply, the power supply and/or the supply voltage for the coax relays of the LNA come from the internal conductor of the converter coax relay via St2, the de-coupling choke, L2, and the blocking capacitor, C1, to St7.

If the power supply for the LNA has to come from an externally fed voltage and the relays Rel1 and Rel2 have to be

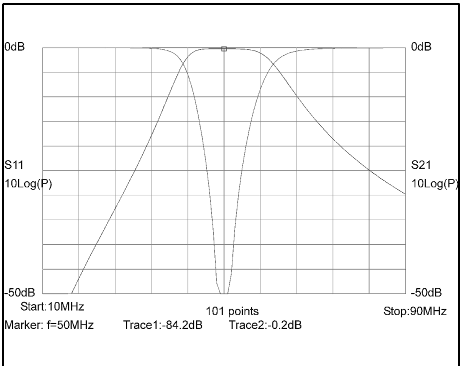


Fig 9: Simulated performance of the 50MHz bandpass filter.

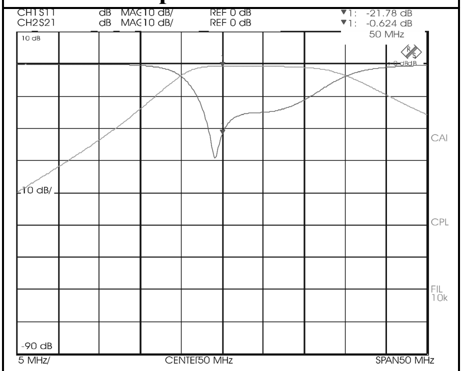


Fig 10: Measured performance of the 50MHz bandpass filter.

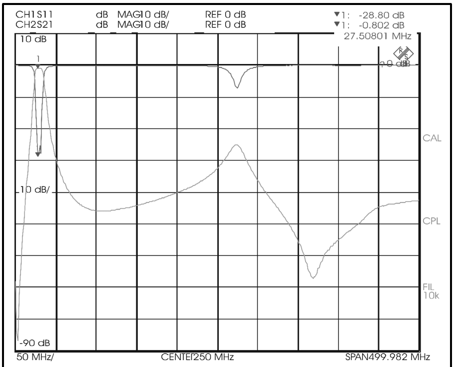


Fig 11: Measured wide band performance of the 50MHz filter.

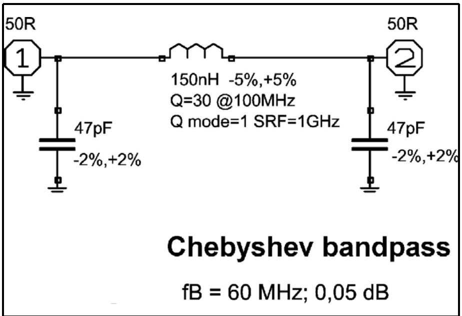


Fig 12: Circuit diagram of the 60MHz low pass filter.

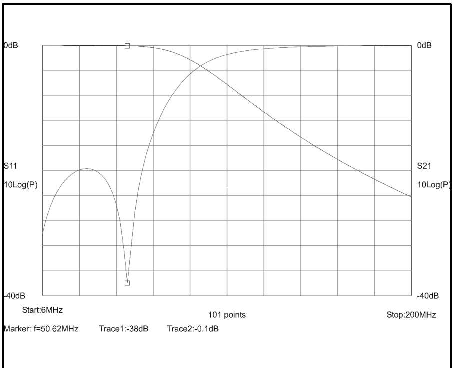


Fig 13: Simulated performance of the 60MHz low pass filter.

switched through, St7 has to be connected to St8 and St6 to St3.

The power supply voltage and switching voltage can be fed in separately through their own cable.

The RF 2360 amplifier is designed for cable television applications (CATV) and can be operated in accordance with the data sheet, or else in a system where there is a 50Ω or 75Ω system impedance [6]. The component is supplied in an SO-16 housing.

The data sheet contains several test circuits for a 50Ω or 75Ω system impedance, together with various frequency ranges. Some test circuits of the data sheet contain an input coupling capacitor and others do not.

According to the data sheet [6], the internal circuit of the IC consists of two FETs wired in cascade. Both active components are biased using internal voltage dividers. This would require a coupling capacitor in the input. On the other hand, in the description of the pin connections there is a reference to the fact that the input pin is de-coupled with regard to DC voltage, and thus no external DC voltage coupling is needed. Moreover, the specification of a lower limiting frequency points to an internal capacitor.

For 50Ω system impedances, according to the test circuit (broadband matching 5 to 1500MHz), a series inductance of 4.7nH is provided for in the input. The power supply voltage is fed to the output via a 1µH choke and the coupling capacitor reading is 10nF.

The circuit diagram also shows two striplines at the input and output. But their impedances and lengths are not specified.

In addition to the broad (50Ω) connections for the SMA sockets at the input and output, the test circuit layout also shows a narrower microstrip line section at each of these locations. Broadband matching can possibly be achieved with the help of the inductance in the input.

All pins not in use are earthed. In another test circuit (5 - 50MHz, 75Ω system impedance), the unused pins remain free.

For the specimen printed circuit board, the S11 parameter in the frequency range from 5 to 50MHz was determined by means of a network analyser. The measured values are listed in Table 5.

The matching elements required were determined with the help of the MIMP program (Motorola Impedance Matching

Table 5: Measured values of S11 for the printed circuit board.

Frequency MHz	Real S11 Ω	S11 Phase °	Equivalent series capacitor pF
5	98	-109	167
10	102	-96	164
15	103	-67	156
20	102	-53	147
22	102	-50	142
25	101	-46	135
28	100	-44	127
30	99	-42	124
35	97	-37	119
40	96	-34	116
45	95	-31	112
50	94	-28	109

Programme; description in [14]) for an inductance of 200nH parallel to the input of the RF 2360 and a series capacitance of 47pF. As an experiment, an SMD coil giving 220nH was inserted for the inductance, which gave optimal matching at 45MHz and was still adequate at 50MHz. In the circuit created, the inductance is provided by means of a series circuit of a 180nH and a 22nH SMD coil.

For the frequency response and the input matching of the LNA IC with the L transformation element (47pF, 220nH) without the output low pass filter, see Fig. 14.

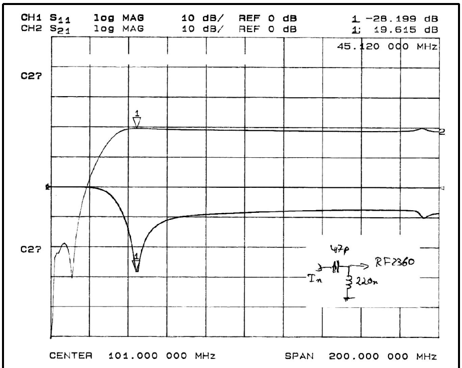


Fig 14: Frequency response at the input of the LNA.

Due to the wide frequency range of the amplifier, the cold end of the choke, L5, was blocked with capacitors to provide the power supply for the IC.

4.1.1. Power supply

The external power supply (11 to 15V) can be fed either through your own power supply cable or via the internal conductor of the coax cable from the converter through a choke (L2). The voltage for the LNA is stabilised using a type LM 317 T adjustable voltage regulator (in a TO 220 housing). The terminal pins on the printed circuit board are wired up in accordance with their applications.

The series diode in front of the voltage regulator prevents any damage arising from accidental battery reversal.

According to the data sheet, the LNA's power supply can be anywhere between 6 and 9V. The selected value was 8V. It can be adjusted using the potentiometer, R2, on the voltage regulator.

Figs 15 and 16 show the frequency response and the matching of the complete LNA printed circuit board. The input reflection (S11) in the operating

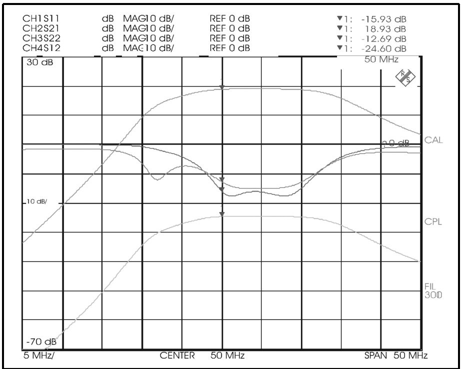


Fig 15: Frequency response of the completed LNA

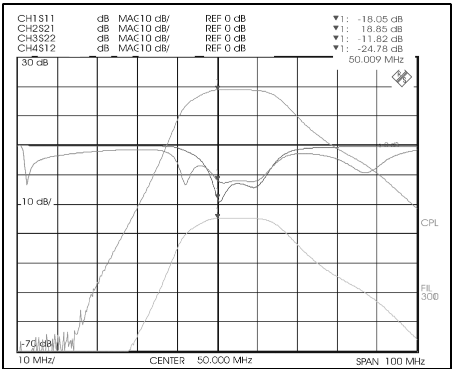


Fig 16: Frequency response of the completed LNA

range is adequate, at -18dB, and the total amplification amounts to 18dB, but the output reflection (S22) amounting to -11dB could do with some improvement.

It can be seen from the curve for S22 in the data sheet that the output reflection is not realistic either. A value of 50Ω - j17Ω was determined on the specimen printed circuit board using the network analyser. This imaginary component, -j17Ω, corresponds to a capacitor of 172pF at 50MHz, and was compensated for by a 56nH choke in series.

Alternatively, the output low pass filter can be modified by omitting the input capacitor and the output capacitor reduced to 18pF.

The transmission loss in the de-activated condition is 0.2dB.

4.2. Converter

Fig. 17 shows the converter's circuit diagram. The circuit is relatively simple:

A three stage band filter (mean frequency 50MHz) is followed by the mixer, the intermediate frequency connection goes to a diplexer and, once again, a three stage band filter with a mean frequency of 28MHz.

4.2.1. Band filter

The band filters were drafted and simulated on the LNA with the help of the "RFSim99" (Tools/Design/Filter) program as three pole Butterworth filters.

The 50MHz band filter was designed, as for the LNA, with a bandwidth of 20MHz, and the 28MHz filter for a bandwidth of B = 10MHz.

The 28MHz filter with the original component values can be seen in Fig. 18. The simulation result is shown in Fig. 19. The insertion loss at the mean frequency is only 0.2dB.

Figs. 20 and 21 show the measured frequency response and the matching of the calibrated band filter in the prototype. The spurious resonance at approximately 280MHz can be traced back to a winding capacitance of the series coil.

4.2.2. Mixer

The HMJ-5 mixer is a passive mixer with FETs, which are biased using a DC voltage of 3V, applied from outside (bias current). According to the data sheet, it can be used for frequencies from 40MHz upwards at the RF Port and from 30MHz at the LO Port. In this application, the frequency limit at the LO Port is slightly

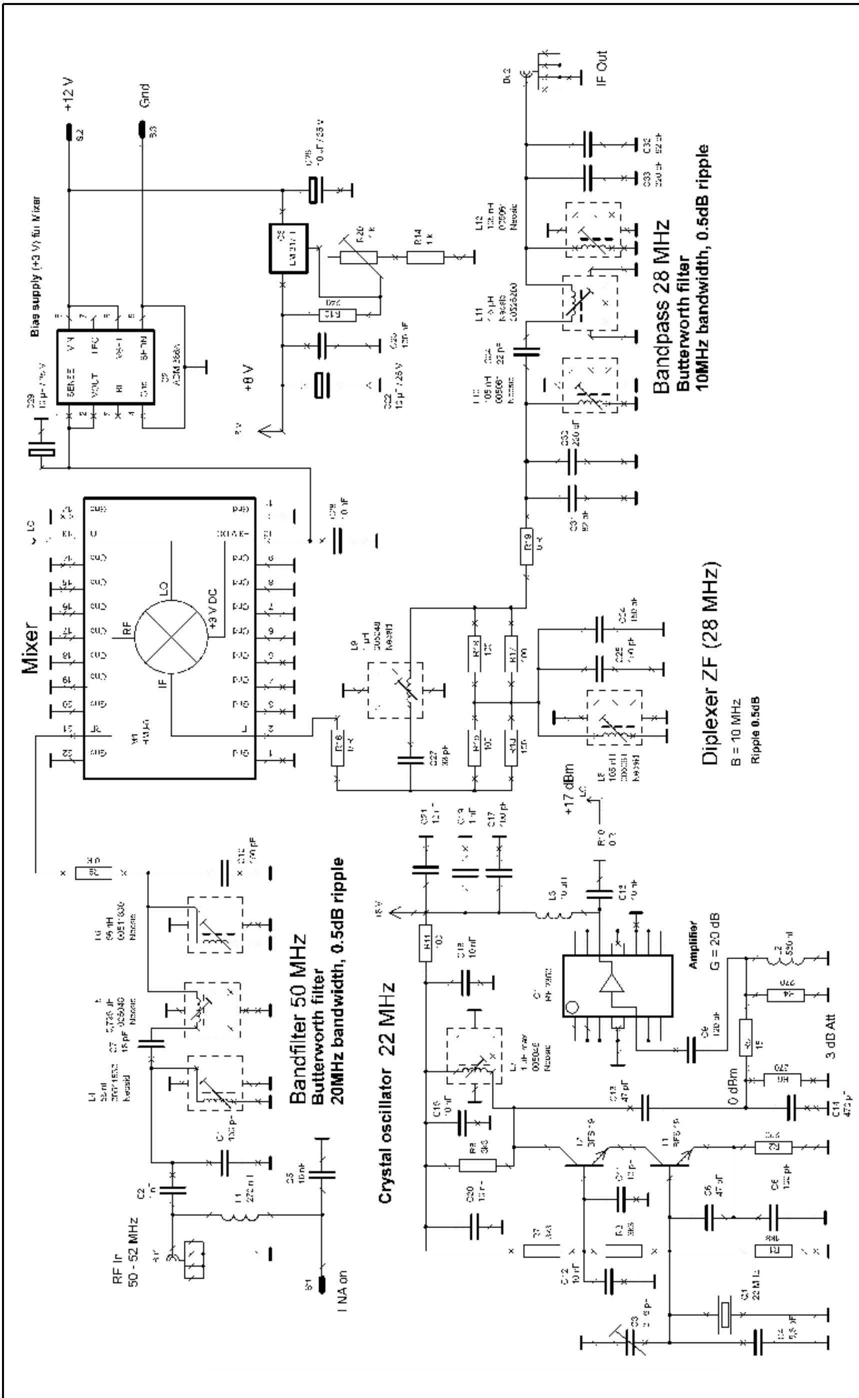


Fig 17: Circuit diagram of the 28/50MHz converter.

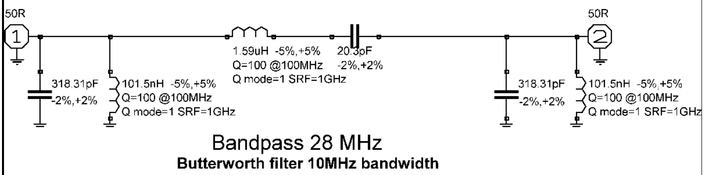


Fig 18: Circuit diagram of the 28MHz bandpass filter.

undershot, but operation should be possible.

In accordance with the data sheet, the following values should be obtained when the mixer is operated in the 6m band:

- $IPIP_3$ = 38dBm
- Mixer loss: 6dB
- LO to RF isolation: >50dB
- LO to IF isolation: > 50dB
- RF port return loss > 20dB
- intermediate frequency return loss > 20dB
- LO port return loss > 20dB

The HMJ-5 mixer is terminated at the intermediate frequency port only, with a diplexer (bridged T filter calculated using the formulae in [12, 13]). According to [9], a broadband connection is required for all ports with Schottky diode ring mixers.

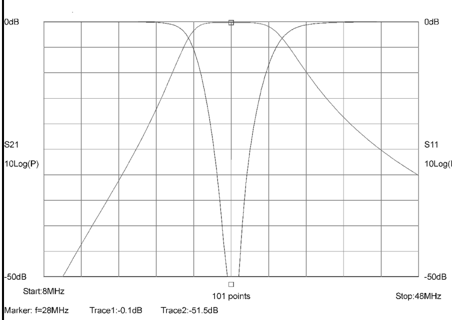


Fig 19: Simulated response of the 28MHz bandpass filter.

This view is not shared in [8], where it is considered that only a load with the correct impedance at the intermediate frequency port is necessary up to the fifth mixed product (LO and RF).

Since the matching of the LO port to the system impedance (here 50Ω) is frequently poor, a suitable matching must be provided, according to [8].

If the mixer is used in the 50MHz converter, then according to the data sheet the return loss at the LO port is so good that no additional measures are needed for impedance matching.

At the intermediate frequency output (after the diplexer), 0dBm of the following mixed products (Table 5) is generated in the frequency range between 0 and 100MHz for an input signal at the RF port F = 50MHz.

Note that the mixed products in the filter attenuation band of the diplexer are reduced by the filter activity

4.2.3. Diplexer

Two circuit variants can be used for the diplexer:

1 Band pass filter (series circuit, parallel circuit), bridged T-filter [11]

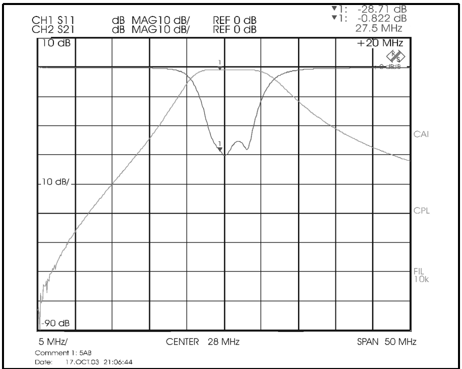


Fig 20: Measured response of the 28MHz bandpass filter.

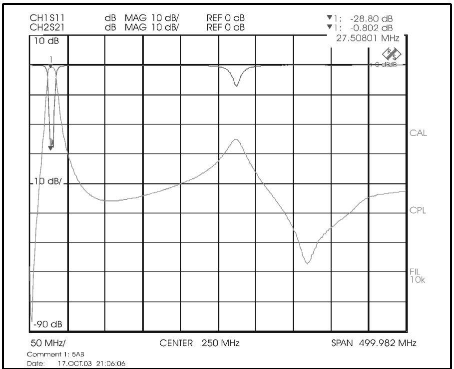


Fig 21: Measured wide band performance of the 28MHz filter.

2 Low pass/high pass combination [16]

The formulae for calculating the components are difficult to reproduce from [11], but the formulae in [10] will help you. [13] gives a detailed description of the drafting of diplexers

In order to obtain insertion loss as low as possible, with reasonable component values for the band pass diplexer, the operating bandwidth should not be selected too low. A low operating bandwidth has the consequence that the series resonant circuit has a high L/C and the parallel resonant circuit has a low L/C ratio.

For an operating quality of Q = 2.8, corresponding to a bandwidth of B = 10MHz with a mean frequency of 28MHz, easily obtainable values are achieved - see Fig. 23 and Fig. 24 shows the result of the simulation.

It can be seen in Table 6 that mix products below 16MHz arise from the desired intermediate frequency. Since the diplexer is followed by a band filter,

Table 6: Mix products produced at the diplexer.

Frequency MHz	Level dBm	Mix product
6	-50	RF - 2 x LO
16	-35	3 x LO - RF
22	-44	LO
28	-6.4	ZF = RF - LO
38	-55	RF - LO
44	-42	2 x LO
50	-40	RF (estimate > 55dB)
56	-68	2 x RF - 2 x LO
60	-50	5 x LO - RF
66	-59	3 x LO
72	-25	RF + LO
84	-57	3 x RF - 3 x LO
88	-60	4 x LO
94	-54	RF + 2 x LO

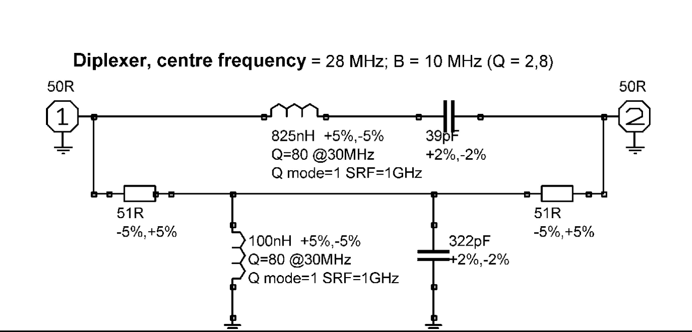


Fig 22: Circuit diagram of the diplexer.

these mix products are not attenuated by the second type of diplexer. So this type has been rejected, although it can be assembled using SMD chokes throughout, and would not need calibrating.

Figs. 24 and 25 show the measured frequency response and the matching of the calibrated diplexer in the prototype. We can see from Fig. 23 that the matching (S11 < -20dB) is maintained up to frequencies of 500MHz. The spurious resonance at approximately 380MHz can probably be traced back to a winding capacitance of the series coil.

In order to guarantee low insertion loss and broadband matching, the inductances of the series and parallel circuits have to be calibrated. The calculated capacitances also have to be maintained.

If we make our selection in accordance with the bandwidth (operating quality) of the diplexers and the inductances of the band filter, in this case B = 10MHz, a good broadband matching is guaranteed in the filter attenuation band of the 28MHz band filter – see simulation in Fig 27. This is how the intermediate frequency port of the mixer “sees” all undesirable mixed products. However, the rounding off of the transmission curve is striking.

Figs. 28 and 29 indicate the measured frequency response and the matching of the calibrated diplexer with the subsequent band filter in the prototype. Both in the mean frequency range (28MHz) of the combination and in the filter attenuation band, the intermediate frequency port “sees” a real load. This characteris-

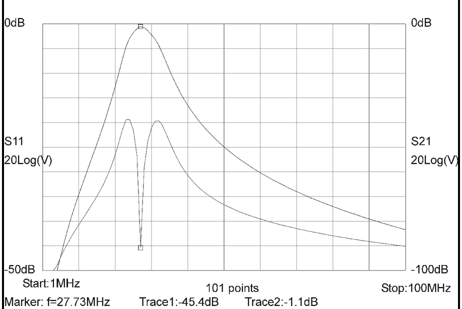


Fig 23: Simulated performance of the diplexer.

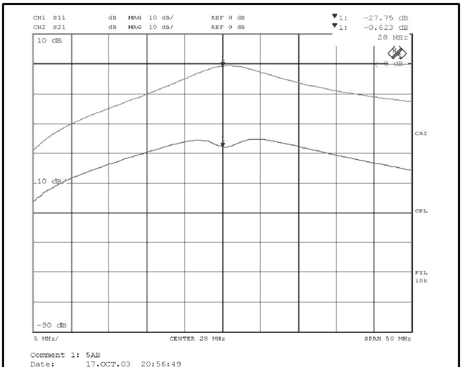


Fig 24: Measure performance of the diplexer.

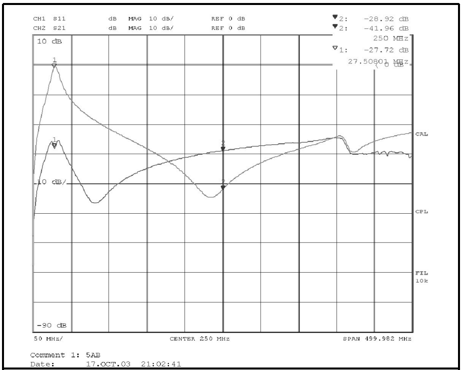


Fig 25: Measure performance of the diplexer.

tic, which is required for the low intermodulations operation of the mixer, is also achieved without an FET amplifier stage in the gate circuit.

4.2.4. Oscillator frequency generation

The 22MHz quartz oscillator is set out as a Colpitts circuit. One small peculiarity may be the configuration of the two transistors. Here we have a cascade circuit, in which the first transistor in the emitter circuit represents the active stage of the oscillator and the second transistor in the base circuit represents the necessary de-coupling and carries out the buffering of the oscillator signal. The oscillator circuit attenuates harmonics by the resistance in the collector circuit of the second stage. An output of 1mW = 0dBm can be detected at the capacitive tap of the circuit.

Since the mixer requires a power of +17dBm for the local oscillator signal ($1.58V_{eff} = 4.44V_{ss}$), the signal is amplified, using a low noise and easily driveable MMIC (RF 2360 from RF Microdevices).

Measurements using the network analyser indicated poor input matching. The input impedance at 22MHz was determined as 100Ω -j100Ω. The necessary matching elements were determined with the help of the MIMP program (Motorola Impedance Matching Programme; description in [14]) as an inductance of 560nH parallel to the input of the RF 2360 and a series capacitor of 120pF.

The 3dB attenuator in the amplifier input provides for level matching. This attenuator was not required in a prototype, since its use, measured with a 100MHz oscilloscope, reduced the oscillator level too much.

Measurements at the intermediate fre-

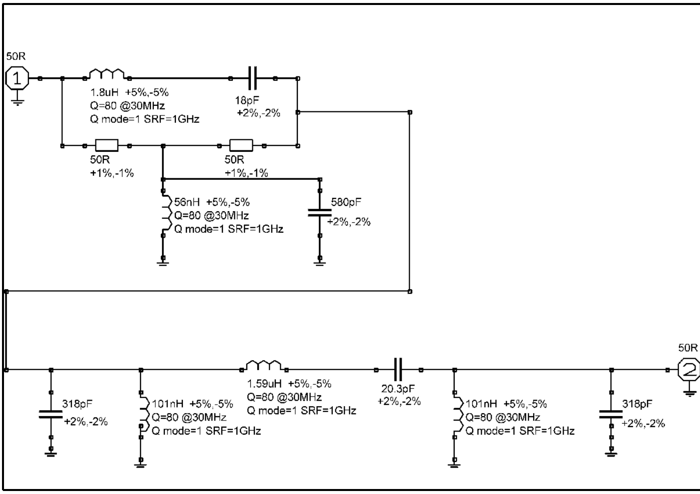


Fig 26: Circuit diagram of the diplexer for 10MHz bandwidth.

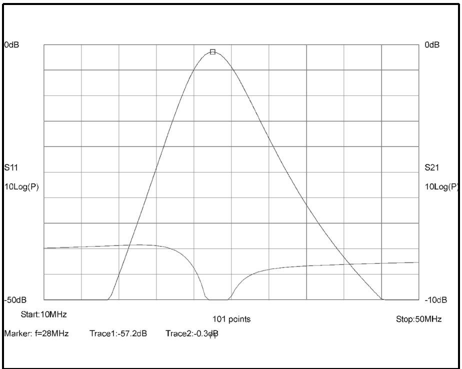


Fig 27: Simulated performance of the diplexer.

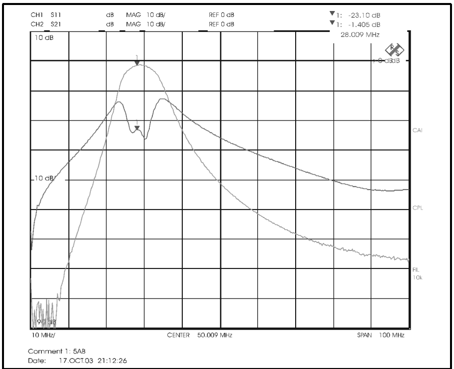


Fig 28: Measured performance of the diplexer.

quency output of the entire equipment using the spectrum analyser, however, revealed a tendency to oscillate in the 1GHz range. It could be suppressed by the additional de-coupling on the base of T2 with a 10pF capacitor. Only then could the level be adjusted using the attenuator.

4.2.5. Power supply

The oscillator and amplifier are supplied using an LM 317 T adjustable voltage regulator (in a TO 220 housing) from the external power supply. The 3.3V bias voltage for the mixer is obtained by means of the ADM 666 fixed voltage regulator (in the SO 8 housing).

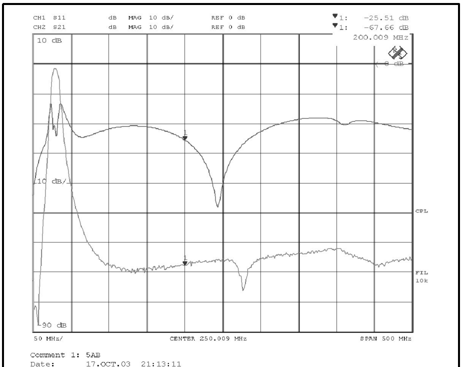


Fig 29: Measured performance of the diplexer.

5. Literature

[1] Reflections on the design of large-signal resistant receiver front ends for the 6m, 2m, 70cm and 23cm band with modern components; Dipl.-Ing. Henning Christof Weddig; Proceedings of the 46th. VHF Congress, Weinheim 2001

[2] Reflections on the design of large-signal resistant receiver front ends for the 2-m and 70-cm band with modern components; Dipl.-Ing. Henning Christof Weddig; Proceedings of the 47th. VHF Congress, Weinheim 2002

[3] 28/ 50 MHz transverter; Wolfgang Schneider, DJ8ES; VHF Communications 2/1994, Pages 107 - 111

[4] 50MHz transverter for short-wave transceiver; Martin Steyer, DK7ZB; *Funkamateur* 8, 9, 10 /1995

[5] HMJ-5 data sheet; Watkin Johnson; www.wj.com

[6] RFMD 2360 data sheet; RF Microdevices; www.rfmd.com

[7] Reducing IMD in high-level mixers;

John B. Stephenson KD8 OZH; QEX May/June 2001

[8] Personal communication with Roy Allan, Watkin Johnson electronica 2002

[9] Large-signal resistant LNA for the 2-m band; Henning Weddig; DUBUS 4/2002

[10] Diplexer for ring mixers; Eugen Berberich DL8ZX; VHF Communications 1/1998 pages 11 - 17

[11] Matching circuits for diode ring mixers; Joachim Kestler DK1OF; VHF Communications 2/1980 pages 94 - 95

[12] Modern input section for 2-m receiver with wide dynamic range and slight inter-modulation distortions; Michael Martin DJ 7VY; VHF Communications 4/1978 pages 218 - 229

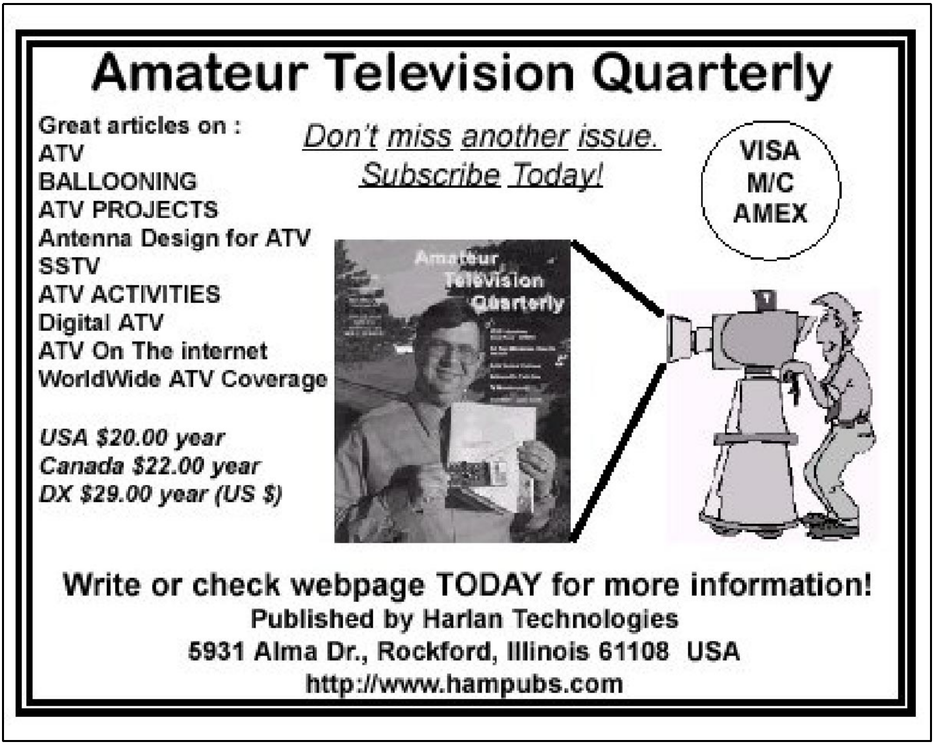
[13] www.qrp-props.net

[14] MIMP, Motorolas Impedance Matching Program; Dipl. Ing. Henning Christof Weddig; VHF Communications 3/2001, Pages 130 - 138

[15] RF 2360 data sheet; RF Microdevices; www.rfmd.com

[16] The Diplexer Filter; ARRL Handbook 2002; Pages 16-39 to 16-40, see also: W.E. Sabin, W0IYH; Diplexer Filters for the HF MOSFET Power Amplifier; QEX July/August 1999

.To be continued



Gunthard Kraus, DG8GB

Design and realisation of microwave circuits, part 10

Development of a 2GHz oscillator

This article was originally published in UKW Berichte issue 2/1999 but it was not translated and published in VHF Communications. It has been included here because it contains details of designing inter-digital capacitors and was referenced in the article by Gunthard Kraus about a 100MHz bandpass filter published in issue 4/2003 of VHF Communications. Several subscribers requested that it was published - Andy.

1.0
Design description

1.1 The BFR92 transistor

The modern transistor BFR92 is still being produced by Siemens They provide a large number of S parameter files for their semiconductors on the Internet. It was no problem to download the appropriate "S2P" file for the operating point "4 V / 10mA", since they were arranged by collector current (rising in steps of 1 mA) and collector voltage (rising in steps of 1 V). The file used for the article below are shown in Table 1. (Note: the values for "zero Hertz" were estimated and added by hand, since PUFF would otherwise report an error if the simulation began with zero.)

1.2 Consideration of footprint capacitances

In spite of the space-saving SMD housing form, each component has two small capacitances from both "connections" to earth. These capacitances have more effect on an oscillator than on an amplifier circuit. It is therefore initially necessary to get a general idea of the order of magnitude of these additional capacitances. This can be calculated with a pocket calculator using the familiar formulae for a plate capacitor.

1.3 Important circuit details

The zero signal current of the transistor should be 10mA. It is usually set or stabilised with a basic voltage divider and an emitter resistance. Here we must take into account that the voltage divider is selected to be as high impedance as possible, since it represents an additional attenuation.

For a selected zero signal current of 10mA, the two divider resistances have the values 3.3kΩ and 3.9kΩ. They are entered in the AC circuit diagram as a parallel circuit from the base to earth.

The C2 capacitor from the emitter to earth should have as little effect on the emitter resistance as possible, otherwise the desired effect of S11 exceeding 1 and

Table 1: S parameters for BFR92.

! F	S11		S21		S12		S22	
! GHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
0.00	0.716	0	23	180	0	90	1	0
0.010	0.7158	-5.0	22.883	175.8	0.0022	85.2	0.9840	-2.2
0.020	0.7068	-9.8	22.641	171.6	0.0048	84.0	0.9756	-4.6
0.050	0.6847	-24.1	21.791	160.6	0.0124	78.8	0.9433	-11.2
0.100	0.6008	-45.1	19.271	144.3	0.0221	71.0	0.8515	-19.5
0.150	0.5134	-62.3	16.401	131.0	0.0298	65.3	0.7581	-24.7
0.200	0.4474	-76.5	14.016	121.9	0.0356	62.9	0.6806	-27.2
0.250	0.3892	-88.9	12.039	114.4	0.0402	62.0	0.6199	-28.5
0.300	0.3444	-99.3	10.482	109.0	0.0450	62.3	0.5780	-28.8
0.400	0.2906	-115.9	8.269	101.1	0.0540	62.3	0.5229	-28.4
0.500	0.2581	-131.0	6.764	94.2	0.0630	63.7	0.4861	-28.1
0.600	0.2396	-142.6	5.739	89.2	0.0722	64.4	0.4639	-27.5
0.700	0.2239	-154.2	4.986	84.4	0.0815	65.0	0.4504	-27.5
0.800	0.2223	-163.3	4.384	80.4	0.0912	64.8	0.4405	-28.0
0.900	0.2152	-172.1	3.923	76.6	0.1011	64.8	0.4321	-28.7
1.000	0.2172	178.7	3.564	73.4	0.1102	64.6	0.4244	-29.5
1.100	0.2222	172.2	3.281	70.1	0.1204	64.4	0.4194	-30.8
1.200	0.2273	165.9	3.045	66.8	0.1301	64.1	0.4113	-31.5
1.300	0.2274	160.3	2.821	64.0	0.1404	63.3	0.4067	-32.8
1.400	0.2318	154.4	2.627	61.7	0.1494	62.8	0.4023	-34.1
1.500	0.2357	151.0	2.486	58.9	0.1594	62.0	0.3976	-35.7
1.600	0.2513	145.5	2.330	55.9	0.1695	61.2	0.3935	-37.1
1.700	0.2550	140.8	2.214	52.8	0.1792	60.5	0.3866	-38.6
1.800	0.2663	136.1	2.125	50.9	0.1890	59.5	0.3826	-40.4
1.900	0.2791	134.3	2.039	48.3	0.1987	58.6	0.3767	-42.4
2.000	0.2838	130.6	1.935	45.7	0.2089	57.6	0.3708	-44.1
2.200	0.3025	124.4	1.784	41.1	0.2289	55.7	0.3584	-48.4
2.400	0.3260	118.1	1.663	36.0	0.2487	53.6	0.3424	-52.8
2.600	0.3530	113.2	1.570	31.2	0.2686	51.4	0.3258	-57.6
2.800	0.3742	108.8	1.473	27.1	0.2883	49.1	0.3083	-62.7
3.000	0.4003	105.3	1.403	22.5	0.3079	46.7	0.2914	-68.9
3.500	0.4617	96.7	1.236	13.3	0.3539	40.4	0.2438	-88.5
4.000	0.5198	89.4	1.105	4.1	0.3994	34.2	0.2151	-115.5
4.500	0.5713	83.2	1.007	-3.8	0.4430	27.5	0.2102	-146.2
5.000	0.6123	77.4	0.916	-12.1	0.4799	20.4	0.2334	-174.0
5.500	0.6586	71.3	0.803	-19.3	0.4958	12.6	0.2400	159.3
6.000	0.6582	66.2	0.772	-22.2	0.5416	8.6	0.3341	154.1

! SIEMENS AG Semiconductor Group, Munich

thus negative input resistance is impaired. So a small SMD RF choke of 22nH is wired in series with the 82Ω resistor. A series loss resistance of 10Ω is added, in accordance with the manufacturer's specification (Q=50) Its self resonance is taken into account by a capacitance of 0.25pF.

The output from the oscillator is taken through a 3dB attenuator on the collector for broadband matching. The DC voltage drop caused by the collector resistance of 56Ω is compensated for by a parallel circuit with a 22nH choke.

1.4 AC circuit diagram for simulation with PUFF

Now let's gather together the elements still missing for the simulation.

For the ceramic resonator, the newest Internet documents from Siemens are consulted. For the selected type of resonator, with a cross section of 6 x 6 mm.[2] and ε = 38, the quality is Q = 600, and is predominantly limited by the ohmic losses of the silver coating and the skin effect. We thus consider the resonator as a lossy transmission line. The following data in PUFF component list F3:

ql 12.3Ω 90° 600Qc

The resonator is coupled to the transistor circuit through an inter-digital capacitor, which impairs the operating quality and thus the noise characteristics of the oscillator if it is selected to be too big. It's value lies somewhere in the vicinity of 0.2pF.

With this solution, we must not overlook the fact that, due to the inter-digital structure, additional inherent capacitances to earth arise. They are very dependent on the board thickness and the actual dielectric constants of the board material. For this design, we simply start from a capacitance value in the order of the coupling capacitance required (0.2pF) on each side.

As regards the two capacitors, C1 and C2, of the capacitive voltage divider, the value provided of 1pF each is used for the first draft. But in the next section we shall investigate its influence and optimise the circuit.

Thus, taking all the details mentioned into account, we arrive at a lavishly detailed configuration for the PUFF simulation, Fig 1. The dotted line shown here between points A and B is an imaginary separation between the resonator section with the coupling capacity and the active part of the circuit, which produces the negative input resistance required for the permanent oscillation. We can thus now vary different component values in the transistor circuit with PUFF's "component sweep" and deter-

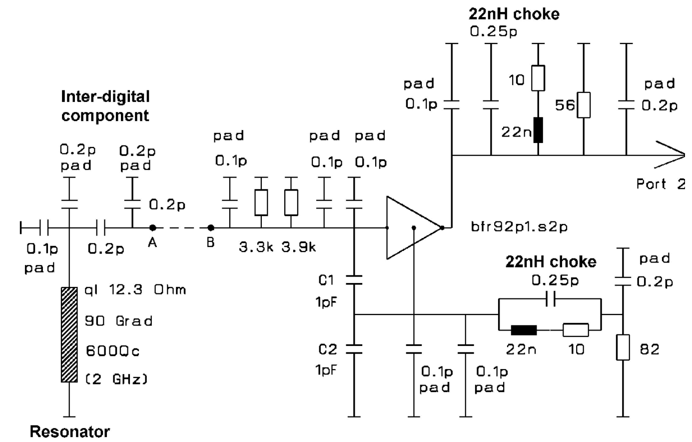


Fig 1: AC circuit diagram of oscillator for simulation with PUFF.

mine their influence on the S11 factor of the circuit (i.e. at point “B”).

1.5 Definition of C1 and C2

With the help of PUFF and its “component sweep”, the optimal values of the two capacitors are determined, one after another. “Optimal” means that we are trying to obtain the highest (positive) value for the input reflection, S11, at f = 2GHz. To do this, we proceed as follows:

Step 1:

First, the components required for the amplification circuit from point B alone are entered in list F3 (to the right of the separation line in Fig. 1) and the corresponding simulation circuit is created in field F1.

Step 2:

Likewise, a question mark is entered under capacitor C2 in F3 (component “e”) in front of the actual component value, with 1pF. The other settings such as “design frequency 2GHz, board thickness = 1.5mm, ε = 4.3, copper thickness = metal thickness mt = 0.035 mm, tangent of loss angle = loss tangent = 0.02” have hopefully already been entered in the file. If necessary, call up the file used with a text editor and check the entries!

Step 3:

After pressing on F2, we first alter the axial division for the “swept capacitor C2” from 0 to 2pF on the horizontal axis of the lower diagram (“rectangular plot”).

Step 4:

If we start the plotting process (Fig 2), then we very soon notice that we obtain a maximum value for C2 = 0.8pF at S11. We enter this value in list F3 against component “e”, once we have removed the question mark again.

Now the question mark is put against the value for capacitor C1 in F3 (component “m”) instead. Fig. 3 gives the result of the plotting process. One very satisfactory observation is that the value of C1 = 0.8pF (as in C2) precisely matches, and produces the maximum value of S11.

1.6 Determination of coupling capacitor required

First, we supplement the circuit in field F1 by adding the resonant section, including the inter-digital structure with the pad capacitances. But we still do not have the constant current source “cs.dev”

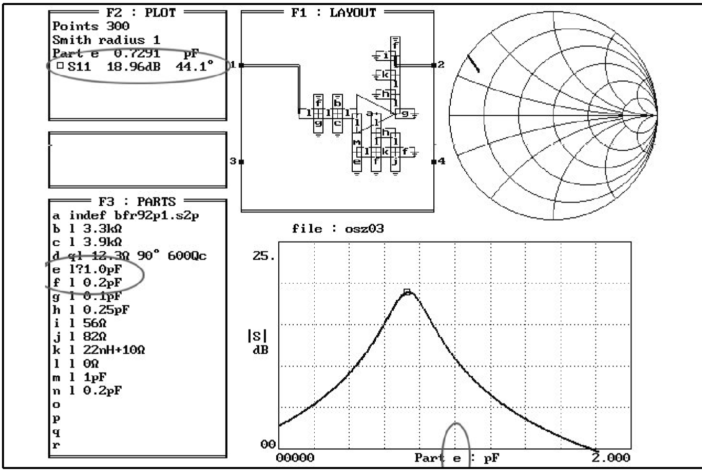


Fig 2: Determining the optimal value of C1.

already referred to. It is triggered by port 1, and feeds its output signal directly in at the resonator connection.

If we now set the radius of the Smith chart on 30 and plot the forward amplification S21 in the area between 1.8 and 2GHz (Fig. 4), we now need only look at the direction in which the S21 circuit on the Smith chart is curved.

A curve to the left means that the point of the oscillation application has already been reached, and even passed. The resonator has consequently already been attenuated again through the "excess negative resistance", and S21 has thus decreased. The only remedy against this is to make the coupling capacitor smaller.

A curve to the right means that the negative input resistance of the transistor circuit is not yet sufficient to cover the losses. The oscillator is therefore still oscillating, and the coupling capacitor must be enlarged.

At the precise application point of the oscillation, we obtain an infinite amplification, S21 – this point must be searched for with the aid of PUFF.

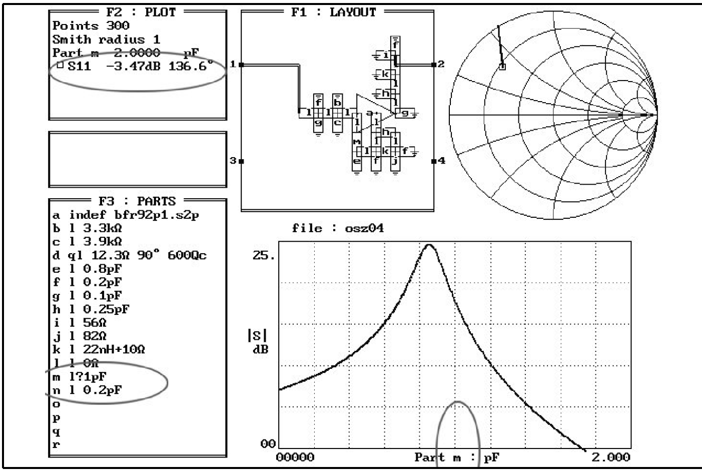


Fig 3: Determining the optimal value of C2.

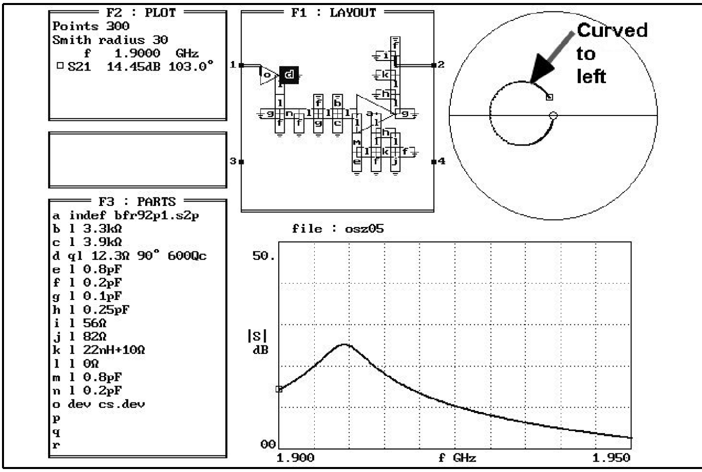


Fig 4: First simulation run for the project.

As can be seen from Fig. 4 and from the Smith chart curve to the left, the oscillator is oscillating for a long time and the coupling must be reduced. Fig. 5 shows the necessary changes to the coupling capacitor (component "n") to find precisely the application point we are searching for, with S21 > 100 dB.

Release the earth connection on the resonator, connect the resonator end which this makes accessible to port 1, and plot the input reflection S11 for the area around the resonance frequency, with a high resolution. The application point for the oscillation lies at the point where S11 is precisely zero and the phase changes from "-180 degrees" to "+180 degrees". If this "check simulation" is carried out very precisely, I'm pleased to say that we obtain precisely the same frequency value as with the new method.

As already stated, it does not make very much sense to select this operating condition. The smallest scatter or change leads to the breakdown of the oscillation or prevents oscillation from starting. So the positive feedback is set to be stronger than is necessary, and then initially, through a suitable amplitude stabilisation, we increase the oscillator voltage,

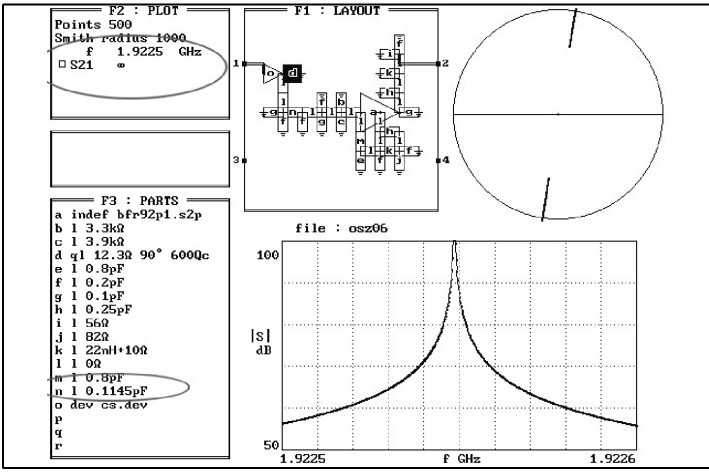


Fig 5:Determining the point of oscillation by changing the coupling capacitor at the resonator.

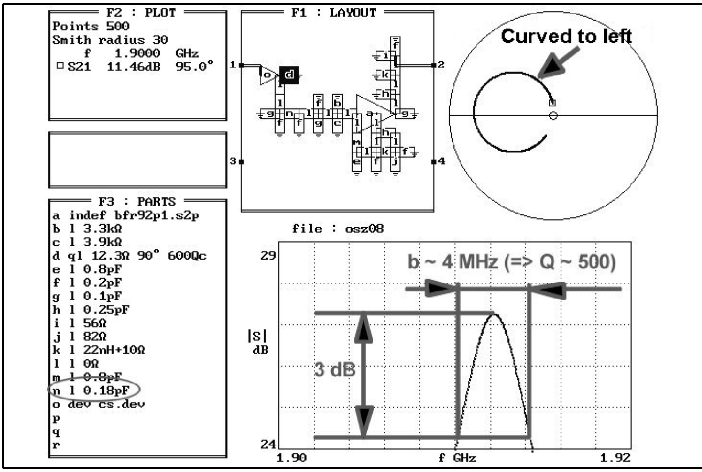


Fig 6: Definition of the coupling capacitor for a Q≥500.

and then reduce the amplification as the amplitude increases, until a stable, maximal output level is obtained under all possible operating conditions.

This can be obtained by making the coupling tighter until, through the "excess negative resistance", a circuit quality of app. Q = 500 to 1000 is set. It can then easily be recognised from the rectangular plot that the S21 curve displays a 3dB bandwidth from approximately 2 to 4MHz, in accordance with the well-known quality / bandwidth formula.

Fig. 6, finally, represents this operating case. From it, we can detect that the coupling capacitance needs to be max. 0.18pF, and should take the form of an inter-digital capacitor. As was mentioned earlier, the oscillation frequency, due to various additional capacitances in the circuit, has to be below the natural resonance of the resonator.

The simulation already leads us to suspect that we will probably essentially not exceed 1910MHz.

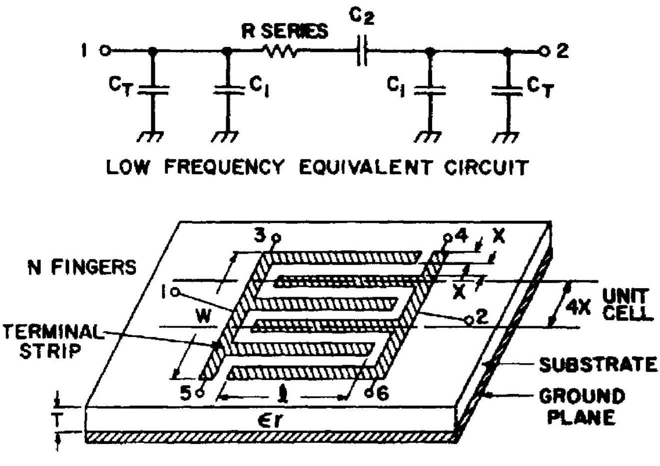
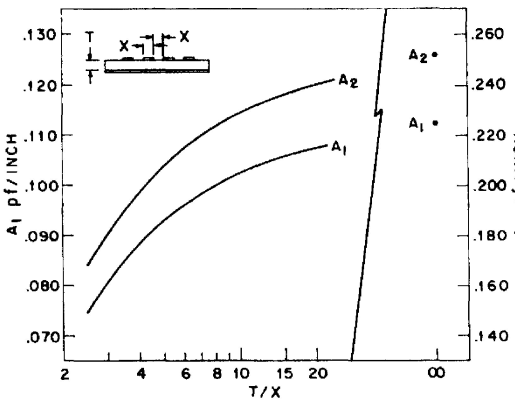


Fig 7:Geometry of the inter-digital capacitor.



Effect of substrate thickness on C_2.

Fig 8: Determining the sizes A_1 and A_2 for X=0.254mm and for a board thickness of T=1.5mm, i.e. T/X=5.9

1.7 Calculation of an inter-digital capacitor

The most important principles can be found in the article by Gary D. Alley [1]. He uses the finger structure represented in Fig. 7, in which both the finger width and the interval between fingers are described by "X" and are identical. The following relationship with the finger length then applies for the coupling capacitance (in pF):

$$C_{coupling} = \frac{L^2}{W} x(\varepsilon_r + 1)x[(N-3)xA_1 + A_2]$$

Where:
L = finger length in inches
W = width of formation in inches
N = number of fingers
ε_r = relative permittivity of board

A_1 and A_2 are two values which depend on the relationship of the board thickness (T) to the interval between the fingers referred to (X). Their values for the T/X relationship used can be taken from Fig. 8.

The inter-digital capacitor can thus be drafted for 0.18pF in the following manner.

Step 1:

As a preliminary, select, for example, a structure with 6 fingers and a finger width and/or interval between fingers, X = 0.01 inch = 0.25 mm This gives a width W for the formation of:

W=11 x 0.01 inch = 0.11 inch = 2.79mm

The relative permittivity of the FR4 material for f = 2GHz is still, according to experience, only ε = 4.3.

Step 2:

For a board thickness T = 1.5mm and an interval X = 0.254mm, there is a relationship of:

$$\frac{T}{X} = \frac{1.5mm}{0.254mm} = 5.9$$

In addition, from Fig. 8 we obtain the values: A_1 approximately 0.095 and A_2 approximately 0.22.

Step 3:

Thus the above formula can be used to calculate the values for a table for finger lengths of between 0.04 inch (approximately 1mm) and 0.12 inch

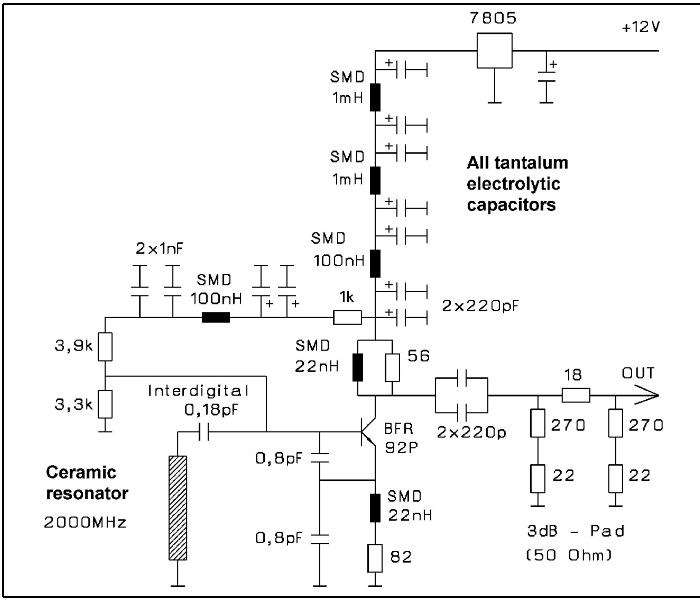


Fig 9: Circuit diagram of designed oscillator.

(approximately 3mm), with a step width of 0.002 inch (approximately 0.5mm) :

Finger length in inches	0.04	0.06	0.08	0.1	0.12
Finger length in mm.	1.016	1.524	2.032	2.54	3.048
Coupling capacitance in pF	0.0426	0.096	0.17	0.27	0.38

The rest is not a problem, for with a finger length of 0.08 inch (approximately 2mm) we have almost arrived at C = 0.18pF.

1.8 Circuit diagram and board layout

As stated in the previous section of the article, the power supply passes through a fixed voltage regulator and some expensive filters. The complete circuit is shown in Fig. 9. Fig. 10 shows the fully equipped board in the milled aluminium housing and the broadband filter for the operating voltage. The inter-digital capacitor, the ceramic resonator, the filter with the tantalum electrolytic capacitors and the attenuator at the output are easily recognisable.

1.9 Test results

The output frequency was specified at f = 1.896540GHz using a frequency counter (hp 5245). A 24 hour measurement yielded a frequency change of max. 200kHz. The frequency change is greatest in the first 5 to 10 minutes; a remedy can be provided by a temperature controlled oven.

The formation is mechanically very stable, due to the milled aluminium housing and the 3mm thick cover with “conductive silver sealing”, and so the sensitivity to feadback is very low. Mechanical shocks, e.g. from a screwdriver, can displace the frequency by a maximum of some kHz, and then it finally returns to the old value.

The use of a fixed voltage regulator for the stabilisation of the power supply

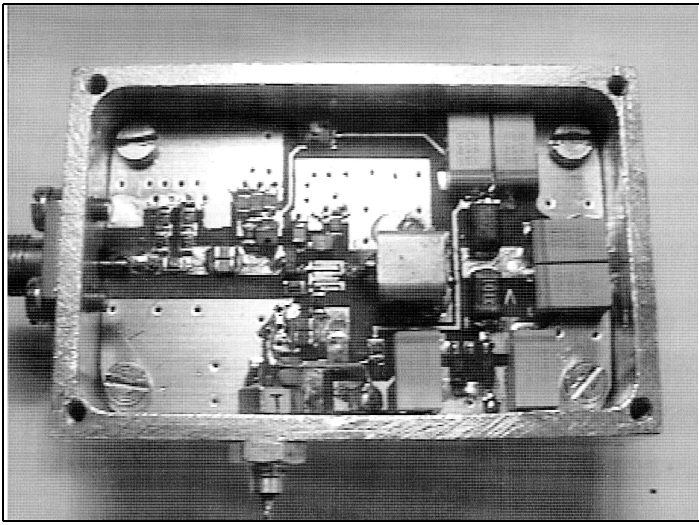


Fig 10: Completed prototype of the oscillator in a milled aluminium housing.

voltage also pays dividends If we increase the applied power supply voltage by 1V, the frequency changes only by approximately 5 kHz.

2.0 References

[1] Gary D. Alley: "Interdigital Capacitors and Their Application to Lumped-Element Microwave Circuits". IEEE Transactions on Microwave Theory and Techniques, Vol. MTT, NO. 12, December, 1970, Page 1028.

50MHz
UKSMG

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Gunthard Kraus, DG8GB

Internet Treasure Trove

ANSOFT

Once there was a feature film called "The Empire Strikes Back". That's what I was reminded of when I downloaded the all new free of charge student version of the RF CAD "Designer" software from Ansoft (N.B.: almost 80 megabytes!). Never have so many tools been made available for simulation and for development in general. Naturally, it takes a while to familiarise yourself with the package, but it's worth it. Virtually all areas are covered, virtually all the calculators for RF and microwave engineering are provided. However, there is unfortunately one way in which Ansoft has stayed true to its old habits. There is scarcely any documentation – in some cases, none at all – to explain what has been left out of the student version. And of course, you find this out as soon as you ask the software to solve any really complicated practical problems. But apart from this, it's first class!

Address: http://www.ansoft.com/

The N4UJW Antenna Design Lab

That's exactly what this site has to offer: any amount of software and information relating to antennas and antenna calculation. And a search through the list of links unearths some interesting things. There's something hidden behind every item on the screen.

Address: http://www.hamuniverse.com/

RF Avenue Resources Directory

Anyone opening up this page has a few problems, as you're initially confronted with an endless list of documents concerning RF and microwave engineering. Of course, it's all nicely and neatly sorted out. You could spend hours here...

Address:
http@//www.newwaveinstruments.com/resources/rf_microwave_resourcesdigital_wireless_communication_directory.htm#Directory

LC

This doesn't refer to a resonant circuit but to the firm of LaCray – who are well known for their extremely fast mainframe computer. It's no surprise that people use such expensive equipment mainly for complicated EM simulations of expensive antennas. But it's not exactly obvious why the company is now allowing people to download the "LC" EM simulator used for this purpose at no charge. Certainly the computer you use should be a Cray computer, but a Linux version is kindly provided for those possessing Intelx86. Do feel free to nose around on your own. It’s really very interesting.

Address: http://lc.cray.com/

Marska WLAN Pages

Even up in Finland there are some active people, which is why it’s worth rummaging around on this homepage. One very interesting subject is what you can find here under the heading “2.4 GHz WLAN antenna – Do it yourself”. You can choose between English or Finnish texts. But anyone who doesn’t speak any Finnish will have given up already during the search, and will not be looking for it any longer.

Address:
http://www.saunalahti.fi/%7Eelapal/antennit.html

USMICROWAVES

This manufacturer describes itself as a “manufacturer of MIC thin film technology” That means it’s a source of unending interest for those who want to be comprehensively informed concerning the state of the art in relation to all types of these active and passive microwave components. In addition to the data, layout design rules and/or application notes, etc. are also available in all sections.

Address:

http://www.usmicrowaves.com/

Semiconductor Datasheets on the WEB

This is a page full of pleasant surprises for original developers and anyone who likes messing around, as everything here is nicely and neatly alphabetically sorted and frequently provided with links.

Addresses: http://www.bgs.nu/sdws.html

Radio Netherland

Just for a change, not pure technology, but tips and technology concerning the subject of “Long-distance reception on the medium wave and short wave”. Plus a collection of facts relating to the relevant antennas.

Address:
http://www.mw.n/realradio/practical/index.html

Microwave Active Antenna Group

This site (which is run by the University of Colorado) is also guaranteed not to be boring, for the students are very active and post their well documented research results on the homepage.

Address:

http://nemes.colorado.edu/microwave/theses.html

Free Radio and Computer Programs

What makes this such a fascinating site is that you can just call up one program after another to see whether you might need them. The choice is wide, and there's certainly enough here to be going on with...

Address:
http://www.btinternet.com/g4fgq.regp/index.htmlS102

Vectron

All about crystals - that's the motto here. Follow the links listed to find the application notes which cover every conceivable aspect of this subject.

Address:
http://www.otek.com/products/appnotes/index.htm

Estland Amateur Group

How about a trip to see the real Northern Lights in Estonia? Here you will discover that progress and hi-tech have penetrated almost as far as the Arctic Circle. Some very interesting links and articles!

Address:

http://www.estpak.ee/andrew/ham/ha,htm

QRZ.COM

Fertile ground for all radio enthusiasts. Here too, you can rummage around endlessly among programs and technical documents...

Address:
http://www.qrz.com/download/main/index.html

Dxing.Info

Another site to rummage around and browse in – everything you could need in relation to physics, technology and equipment know-how for DX reception.

Address: http://www.dxing.info/

WAOTRALI

This is an animation program (Waves on Transmission Lines) from the Flensburg Technical College. It can help to clarify the propagation of signals on lines in the time domain. Various transmission signals can be selected from a catalogue, such as sinusoidal signals and pseudo-statistical digital signals of various lengths, among others. The WAOTRALI program is available for downloading from the website of the Institute for Communications Technology of the Flensburg Technical College.

Address:

under www.fh-flensburg.de/kt/

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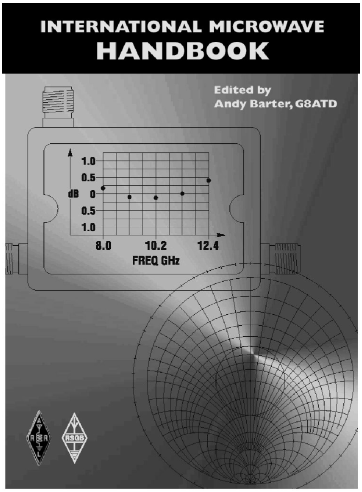

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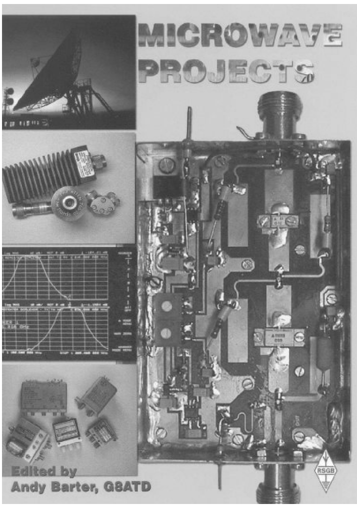

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