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Radio Amateur Worldwide

Especially Covering VHF,
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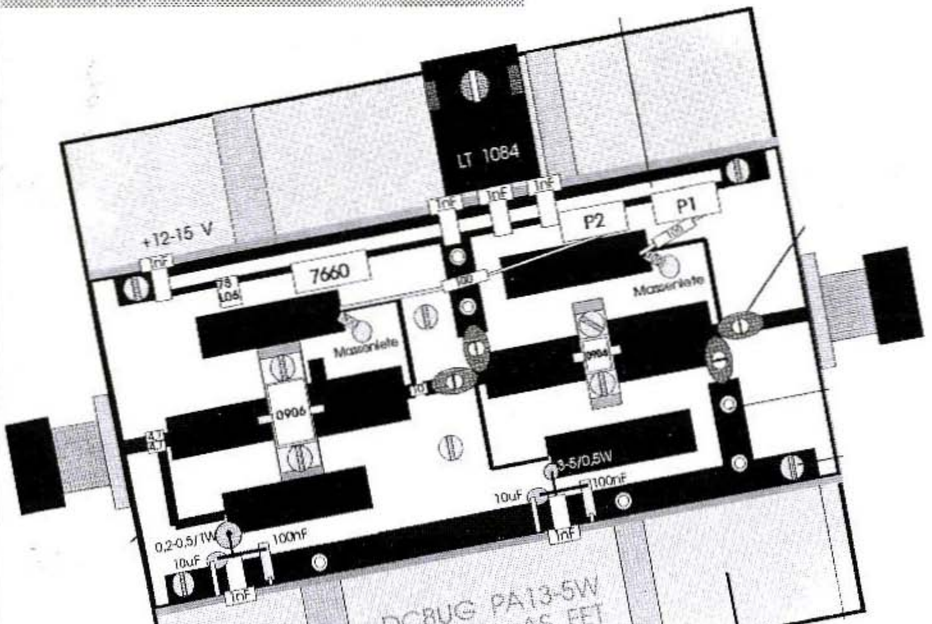
VHF COMMUNICATIONS

Volume No.26 . Autumn . 3/1994 . £4.00

13cm PA designed using 'PUFF'



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Harald Fleckner, DC8UG

A 13cm GaAsFET Power Amplifier Developed using the 'PUFF' CAD Software Package

Transistorised power amplifiers for the frequency range between 2,300 and 2,400 MHz have frequently been described in recent years. (1)(2)(3)(4)(5)(11)

The 2-stage power amplifier introduced here supplies an initial output of 5 Watts at 23 dB amplification in the 13cm band.

1. INTRODUCTION

The circuit was developed using the PUFF CAD software package, which makes it amazingly simple to calculate and simulate even relatively complicated microwave circuits. Several publications (7)(8), together with our own research, have already put the capability of the low-cost software used to the test, so that very positive results were to be expected.

The goal of the project was to develop several amplifiers using the software, build them, and compare the readings with the simulated values. Three different types of amplifier were involved in this project, with different performance figures varying from 4 to 12 Watts in the given frequency range.

The following article describes the selection of semi-conductors, the simulation/analysis of the amplifier circuit using the CAD software, the building of the 5 Watt amplifier and the readings obtained.

2. SELECTING SEMI-CONDUCTORS

The transistors used in the amplifier were Mitsubishi type, from the 0900 range for UHF power amplifiers. They were, in actual fact, N-channel Schottky

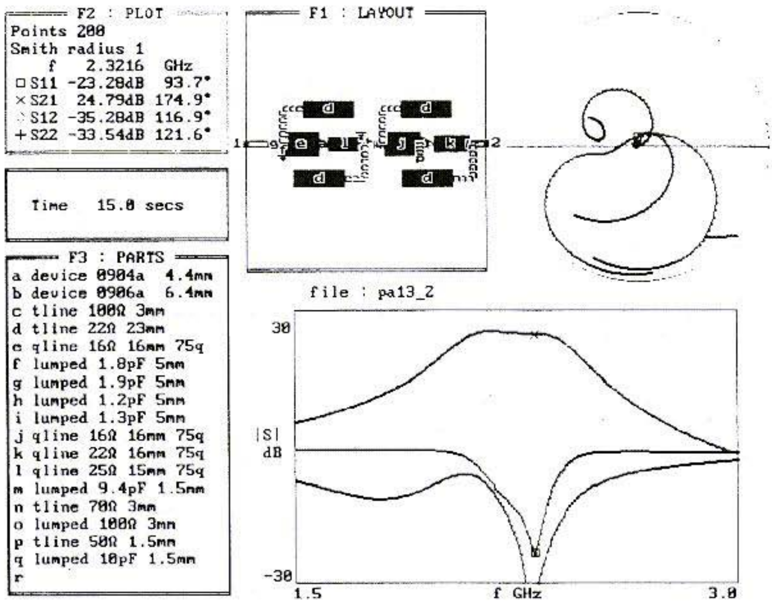


Fig.1: Screen Dump from the PUFF CAD Package

GaAs power FET's, which had already been successfully used in the construction of several circuits (6)(11), and which could be obtained at relatively low cost. Their power spectrum stretched from 0.6W (the 0904 type) right up to 10W (the 0907 type) for amplification levels of between 8 and 13dB, depending on type and frequency.

The performance figures targeted by the development:

Amplification:	> 20 dB at k > 1
Output:	min 5 W at
	max 1dB compression
Band width:	100 MHz

$Z_{in} = Z_{out} = 50\Omega$ at return loss $\geq$ 20dB

could therefore be attained only with a 2-stage amplifier.

The type 0906 seemed a suitable high-level stage transistor. It displayed particularly high operational thermal stability because of its large ceramal housing and, in contrast to the 0905, which was usually running under strain, easily supplied 37dBm = 5W at 1dB compression, thus guaranteeing stable operation with permanent output - e.g. for ATV transmitters. The type 0904 was a suitable driving transistor, because it displayed a high level of amplification (13dB) for a compression-free output amounting to almost 28dBm = 630mW. The S-parameters of the selected transistors required for the development of the circuit came from the Mitsubishi data bank, and applied under the following DC conditions:

MGF0904: UDS = 9 V at ID = 0.2 A

MGF0906: UDS = 10 V at ID = 1.1 A

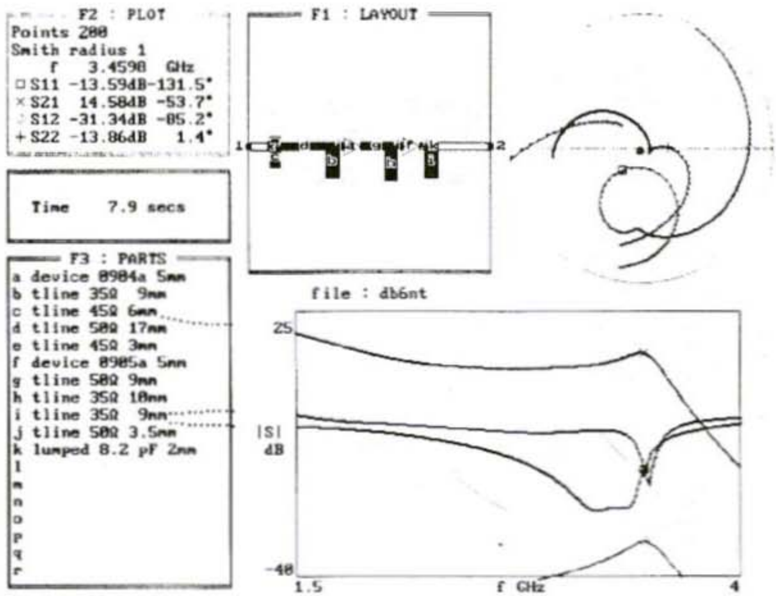


Fig.2: Frequency plots of a Circuit for the 9cm band

The efficiency of these transistors was normally about 40%, so that a DC input power of more than 12 Watts was required in operation, and the resulting power loss had to be dissipated through a heat sink of sufficiently large dimensions.

3. SIMULATION AND ANALYSIS OF AMPLIFIER CIRCUIT USING CAD SOFTWARE

The method of functioning and the operation of the PUFF CAD software are comprehensively described in (7)(8)(9), so here we shall merely list and analyse the results obtained.

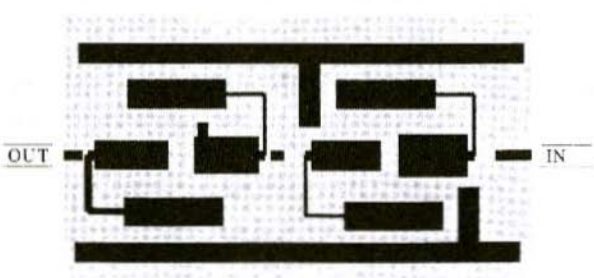


Fig.3: Board Layout generated using 'PUFF'

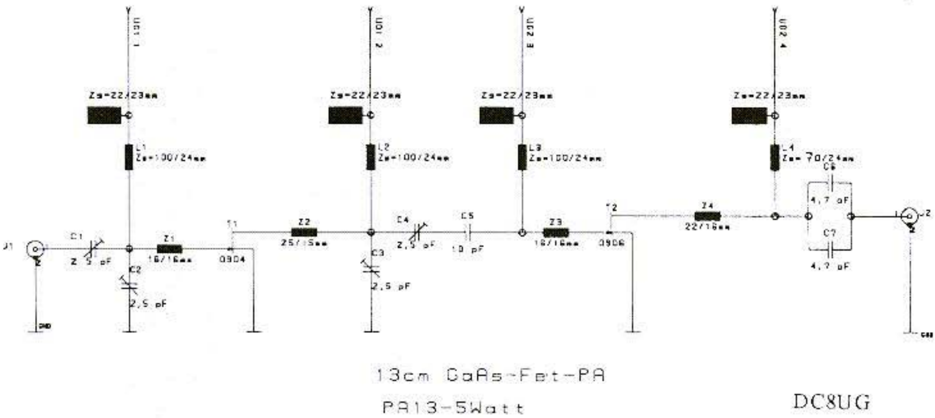


Fig.4: Circuit of the 13cm GaAsFET Power Amplifier

Fig.1 shows the screen dump from PUFF with the draft layout of the circuit, the associated Smith diagram, the parts and the paths of the scatter parameters over the frequency range selected (1.5 to 3.0 GHz). The plot window (top left) also shows the size and phase of the scatter parameters for the selected operating frequency (2.3216 GHz) in the order:

- input impedance (S11) with return loss value
- amplification (S21)
- feedback (S12)
- and output impedance (S22) with return loss value.

The stability factor of the amplification circuit at the operating frequency can be determined from the calculated scatter parameters. The theoretical relationships required for this can be found in (10). Determining the absolute stability (K > 1) using this factor has been tried and tested as best for normal HF amplifiers, so that from knowledge of the scatter parameters the frequency range over which the circuit will be stable can easily be indicated. A quadripole (amplifier) is absolutely stable if it always remains stable whatever the adapted load at the input and output and never self-excites.

The gain slope obtained (S21) as a function of the frequency showed a marked resemblance to that of a coupled band filter. This characteristic was obtained, firstly, through the lengthwise layout of the transmission lines (qlines/tlines) for each stage and, secondly, through the 50Ω coupling of the two stages.

With the lamina-disc method on the other hand, previously used frequently by the author for circuit matching, there is usually a gain slope like a deep pass - less reduction in amplification at low frequencies, maximum at the frequency to be transformed, and a more or less sharp reduction thereafter. This happens because the laminae, soldered on crosswise, act like stubs, which have either an inductive or a capacitive influence, depending on the frequency and length.

NAME	TYPE	VALUE	STYLE	COMMENTS
C1	TC	2.5pf	Teflon/Ceramic	Trimmer
C2	TC	2.5pf	Teflon/Ceramic	Trimmer
C3	TC	2.5pf	Teflon/Ceramic	Trimmer
C4	TC	2.5pf	Teflon/Ceramic	Trimmer
C5	C	10pf	Tekelec-Chip	Capacitor
C6	C	4.7pF	ATC-Chip	Capacitor
C7	C	4.7pF	ATC-Chip	Capacitor
J1	N			N-Connector
J2	N			N-Connector
L1	TL	Zs= 100/24mm	Stripline	Trans-Line
L2	TL	Zs= 100/24mm	Stripline	Trans-Line
L3	TL	Zs= 100/24mm	Stripline	Trans-Line
L4	TL	Zs= 70/24mm	Stripline	Trans-Line
T1	FET	0904	Mitsubishi	N-GaAsFET
T2	FET	0906	Mitsubishi	N-GaAsFET
ZS	TL	Zs= 22/23mm	Stripline	Trans-Line
Z1	TL	Z= 16/16mm	Stripline	Trans-Line
Z2	TL	Z= 25/15mm	Stripline	Trans-Line
Z3	TL	Z= 16/16mm	Stripline	Trans-Line
Z4	TL	Z= 22163mm	Stripline	Trans-Line

Fig.5: Component List for the Amplifier

To make this clearer, Fig.2 shows the simulated frequency response curve in accordance with a circuit published in (6) for the 9cm band, with 0904 and 0905 transistors, without DC choking. With slight modifications to the circuit, this amplifier can also be operated at 13cm without problems, as shown by an article in (11), though of course at considerably less than 20dB amplification.

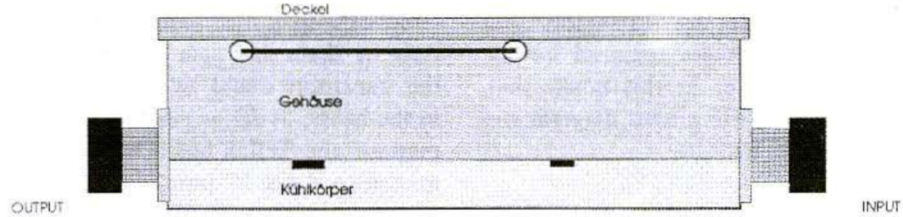
The readings shown in Fig.1 gave the following output values for the draft circuit:

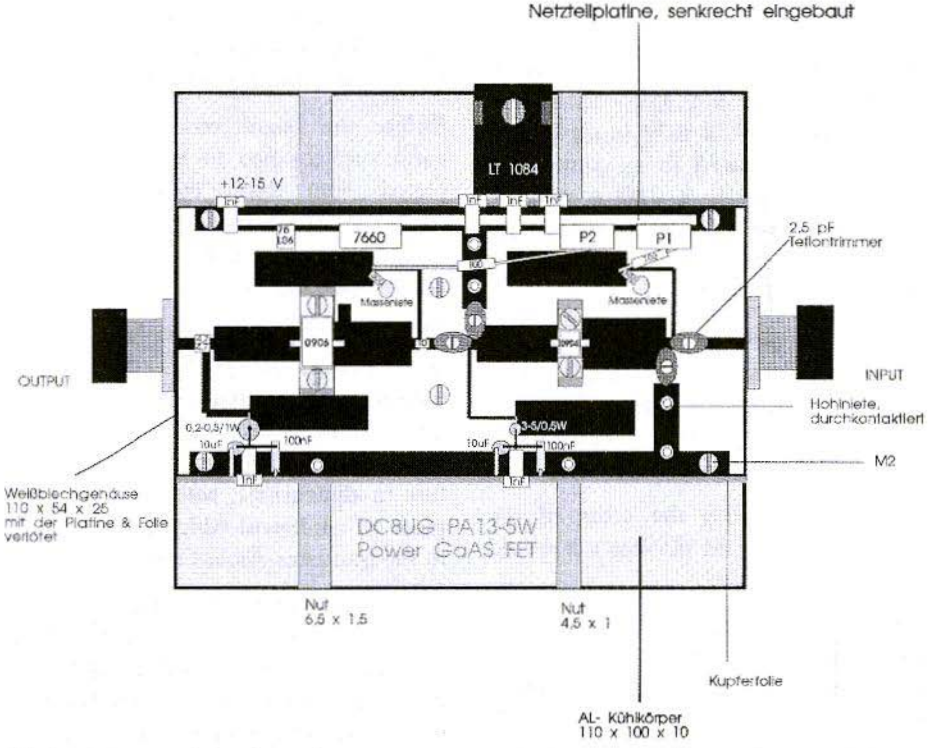
- Return loss input: -23dB
- Return loss output: -33dB
- Amplification at 2,320 MHz: 24.8dB
- Feedback: -35dB
- K-factor at 2,320 MHz: 5
- Band width (-3dB): -280/+120 MHz

Fig.3 shows the layout generated by the CAD software as a print-out from a laser printer for Teflon-based material with a substrate thickness of 0.79mm. The subsequent introduction of a correction factor to generate a precise photographic model is thus possible. The reversed image is pictured, as generated on the exposed board.

The tracks on the longitudinal board side are earth surfaces inserted subsequently, which are through-hole plated to the earth surface when the circuit is assembled.

In the parts list in Fig.1, we can also recognise the discrete modules required for the circuit under the description of





Fig's.6a& b: Side view of mechanical structure and the Component Placement and Assembly plan
(Deckel = cover; Genhäuse = housing; Kühlkörper = heatsink Netztellplatine, senkrecht wingebaut = PSU board, vertically mounted; Weißlechhgehäuse = tinplate housing; mit der platine & folie verlötet = soldered to board and foil; Nut = slot; Hohlniete durchkontakiert = hollow rivet, through-hole plated; AL - Kühlkörper = Al heatsink; Kupferfolie = copper foil

"lumped". These are capacitors and resistances which are required for the circuit to operate. In this connection, Fig.4 shows the HF circuit diagram and Fig.5 the parts list.

4. ASSEMBLING THE AMPLIFIER

The amplifier circuit was built on a Teflon board (er = 2.33) with dimensions of 109 x 54 x 0.79 (mm) For its part, it was screwed to an aluminium cooling body (110 x 100 x 10mm), which was used for fastening and as a heat sink for the power transistors and voltage controllers (Fig.6).

The use of epoxy resin based material was excluded, since power amplifiers in this range already produce dielectric losses of 20% (app. 1dB), i.e. a loss of 1W at 5 Watts output.

So, compared with the costs of the transistors (app. DM 60/Watt), it would be a false economy.

The DC power supply system was assembled on an epoxy board, coated on both sides (91 x 20 x 1.6mm), which was vertically soldered to the longitudinal side of the housing (Fig.6) within. Its circuit corresponded to the one published in (6).

Figs. 7, 8 and 9 show the screen, layout and parts list for this power supply. The components are mounted on the foil side, so that the earth surfaces have to be through-hole plated.

Grooves were milled in the heat sink so that the drain and gate connections of the transistors could be soldered flush to the board, as far as possible. For this purpose, the Teflon board had recesses measuring 4.4 x 17 (mm) and 6.4 x 22 (mm), into which the transistors were inserted and then screwed to the heat sink (see Fig.6). There was also a copper foil between the board and the heat sink (115 x 57 x 0.08mm), which was later soldered to the tinplate housing. It provided a very good earth connection between the transistors, the board, the housing and the heat sink.

Before the board was mounted, the earth surfaces had to be through-hole plated with 2mm copper (hollow) rivets. At least 4 rivets per longitudinal side and earth connector are required for this (see Fig.6).

The board was fastened to the heat sink at 6 points, using M2 screws. The transistors each required 2 threaded holes in the baseplate for the source connection, which were best provided, true to dimensions, with the help of a piece of cardboard which corresponded to the transistor dimensions.

The dimensions of the tinplate housing were 110 x 55 x 28 (mm) and before assembly it was provided with the necessary bores for the feedthrough capacitors and recesses for the N-sockets. The housing itself was then soldered together, and soldered to the longitudinal sides of the screwed-on board. The soldered-on sockets could then be screwed to the heat sinks on the front faces as well.

The best insertion and commissioning procedure is as follows:

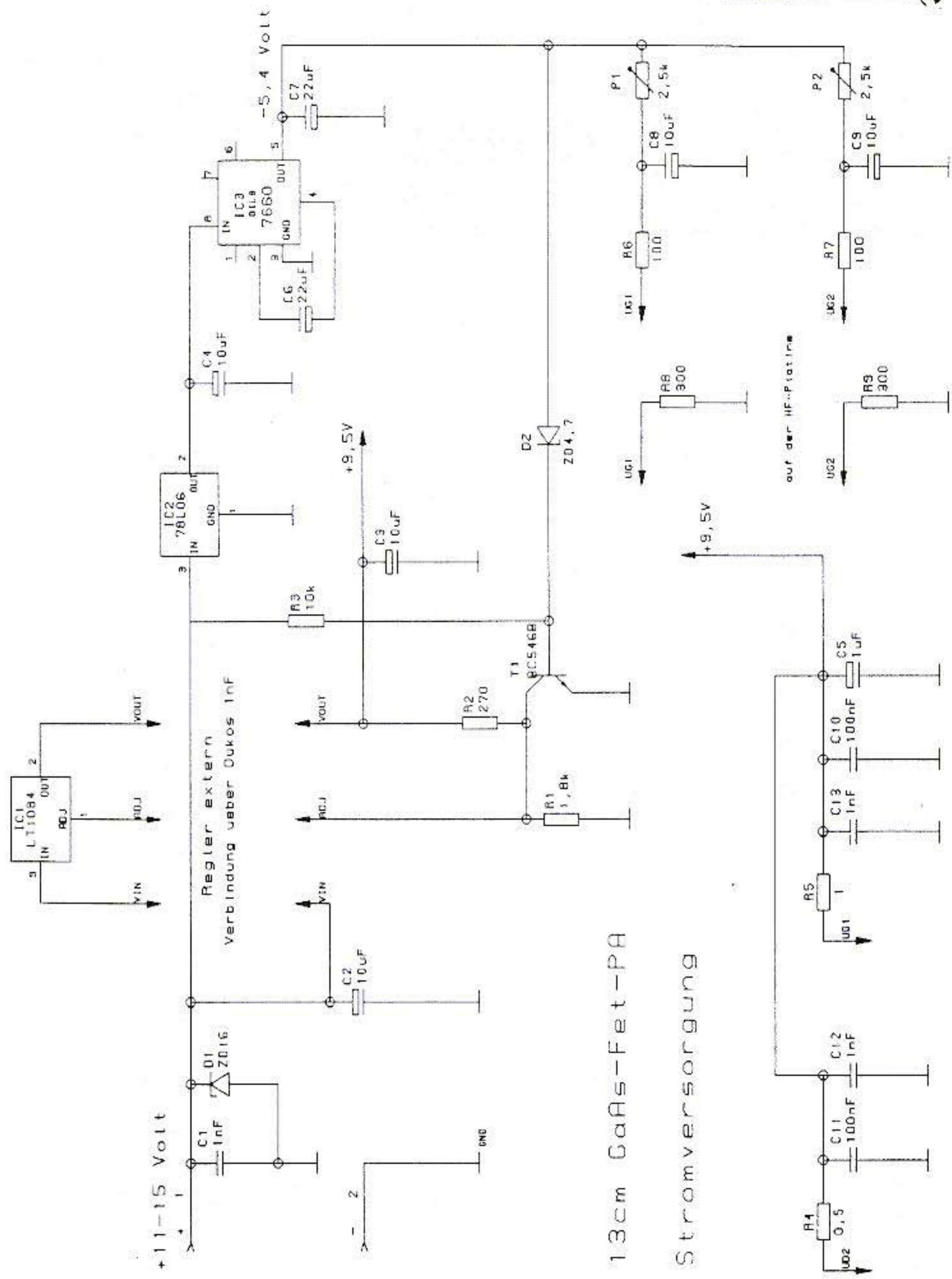


Fig.7: PSU Circuit
(Stromversorgung = power supply; Regler extern,Verbindung ueber Dukos 1nf = external regulator, connection through 1nF feedthrough capacitors; auf der HF-platine = on the HF board

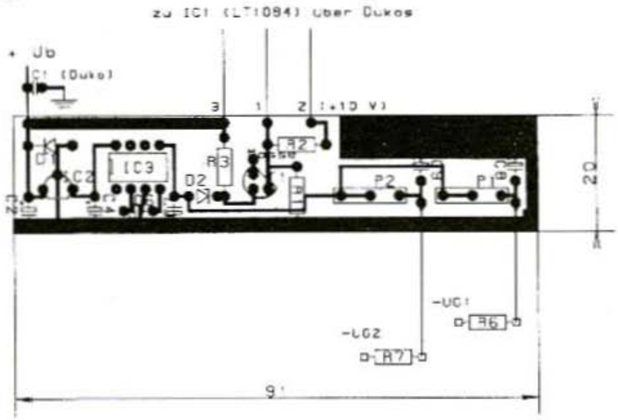


Fig.8: Layout and Component Overlay for the PSU (Dukos = feedthrough capacitor)

NAME	TYPE	VALUE	STYLE	COMMENTS
C1	C	1nF	Feedthrough	Capacitor
C2	EC	10uF	Tant/16V	Electrolytic
C3	EC	10uF	Tant/16V	Electrolytic
C4	EC	10uF	Tant/16V	Electrolytic
C5	EC	1uF	Tant/16V	Electrolytic
C6	EC	22uF	Tant/10V	Electrolytic
C7	EC	22uF	Tant/10V	Electrolytic
C8	EC	10uF	Tant/10V	Electrolytic
C9	EC	10uF	Tant/10V	Electrolytic
C10	C	100nF	Sibatit	Capacitor
C11	C	100nF	Sibatit	Capacitor
C12	C	1nF	Feedthrough	Capacitor
C13	C	1nF	Feedthrough	Capacitor
D1	Z	ZD16	Zener Diode	
D2	Z	ZD4.7	Zener Diode	
IC1	LT1084		TO247	Low drop reg
IC2	78L06		TO92	+ve Regulator
IC3	ICL7660		DIL8	-ve Regulator
P1	P	2.5k (2k)	Piher/Cermet	Potentiometer
P2	P	2.5k (2k)	Piher/Cermet	Potentiometer
R1	R	2k (22k ll 2.2k)	Metal film	Res, 2.2 x 6.3mm
R2	R	270	Metal film	Res, 2.2 x 6.3mm
R3	R	10k	Metal film	Res, 2.2 x 6.3mm
R4	R	0.2 - 0.5 /1W	Metal film	Res, 2.2 x 6.3mm
R5	R	3 - 5 /0.5W	Metal film	Res, 2.2 x 6.3mm
R6	R	100	Metal film	Res, 2.2 x 6.3mm
R7	R	100	Metal film	Res, 2.2 x 6.3mm
R8	R	300	Metal film	Res, 2.2 x 6.3mm
R9	R	300	Metal film	Res, 2.2 x 6.3mm
T1	NPN	BC546B	SOT54	NPN Transistor

Fig.9: PSU Component List

- Assemble and mount power supply board
- Gate resistances (R6, R7) should already be soldered onto power supply for better mounting (see Fig.8)!
- Assemble and wire up the 6 feedthrough capacitors (1nF) and the blocking capacitors C3, C5, C10, C11
- Fasten (insulation!) and connect up voltage controller by means of feedthrough capacitors
- Mount and connect up resistances (R4, R5, R8, R9) to and on HF board
- Mount trimmers (C1, C2, C3, C4)
- Mount chip capacitors (C5, C6, C7)
- The power supply (UG and D) can now be tested.
- Mount GaAsFET's

The static current levels can now be set:

0904 - ID = 0.2A; 0906 - ID = 1.1A

Note: for continuous operation in unfavourable conditions, it is advisable to mount the amplifier on an additional heat sink (e.g. the housing wall), to ensure stable operation.

5. READINGS

The prototype amplifier was constructed so that a 5 Watt output could be achieved with an input of 28mW at 2,320 MHz. The measurement was carried out using a type HP 432 Wattmeter and a 30dB attenuator from Narda.

Fig.10 shows the transfer characteristic of the amplifier.

At 5 Watts output, the compression range begins, i.e. a further increase in power leads to a considerable worsening of the inter-modulation interval; (1dB compression $\cong$ -33dB_{in}).

Fig.11 shows the power amplification at an input 10mW over the frequency range.

Curve A shows the measured gradient arising if the amplifier is tuned to 2,320 MHz.

Curve B shows the gradient obtained through simulation, in accordance with Fig.1.

Consequently, the amplifier has a band width of 300 MHz. Its amplification reduction at the band limits is of course somewhat less than in curve B. The reasons for this are the losses conditional on the circuit, which can not be covered completely by the simulation.

The linear amplification of 2dB obtained is only slightly different from the calculated value. If the amplifier is broad-band tuned, so that its course corresponds to curve B, the amplification falls by about 1dB (20%) as the band width increases.

To sum up, we can say that using PUFF low-cost software to develop simple integrated high-frequency circuits can be highly recommended. True, the efficiency is very much reduced by comparison with high-end products such as, for example, Super-Compact, but the results obtainable are more than adequate for the amateur sector.

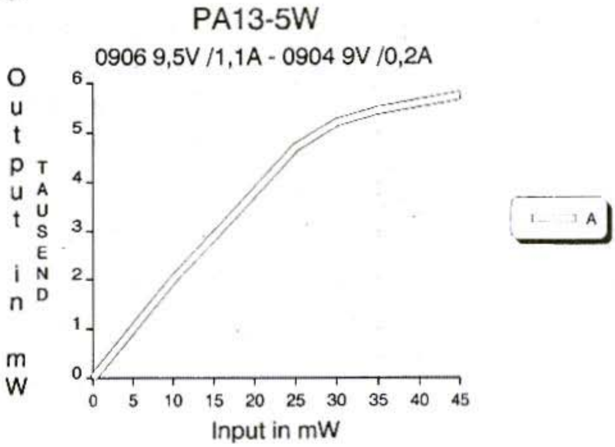


Fig.10: Transfer Characteristics of the Amplifier Tausend = thousand)

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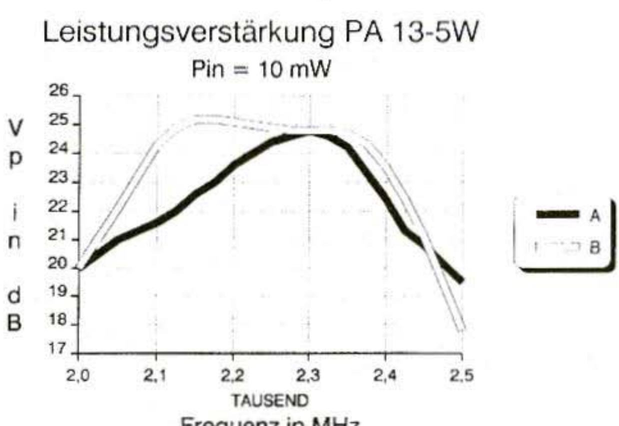

Fig.11: Comparison of Measured and Simulated Power Amplification (Leistungsverstärkung)

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***Note**: The PUFF software package is available from KM Publications. Please see our software catalogue on the rear cover of this issue.*

Richard A. Formato, Ph.D., K1POO

Improving Impedance Bandwidth of VHF/UHF Yagis by Decreasing the Driven Element L/D Ratio

The antenna literature hints that increasing the element diameter in a Yagi improves its impedance bandwidth (see, for example, [1] at page 11-15). But the author is not aware of data showing what degree of improvement can be obtained. This tech note describes the effect of increasing driven element diameter and presents results for a typical three-element array. While the technique is frequency independent, it is especially useful for antennas from mid-VHF through UHF.

Fig.1 shows typical Yagi geometry. The antenna consists of parallel elements spaced along the array axis. The RF source excites the driven element (DE), which is usually a centre-fed dipole as shown (length L, diameter D). Other DE configurations, such as folded dipoles, are sometimes used, but they are not considered here. On one side of the DE is a longer element (R) which acts as a reflector. On the other side are shorter elements (D1...DN) which act as directors. The reflector and directors are parasitic elements.

In most Yagi designs all elements are the same diameter, and they are electrically thin. *Thin* elements have L/D > 1. Elements that are not thin are *fat*. Thin and fat elements have different current distributions. The current along a very thin element is nearly sinusoidal, but this approximation becomes progressively worse as the element becomes fatter.

An element's self impedance is determined by its free-space current distribution, which varies considerably with the L/D ratio. A Yagi's input impedance is determined by the DE self

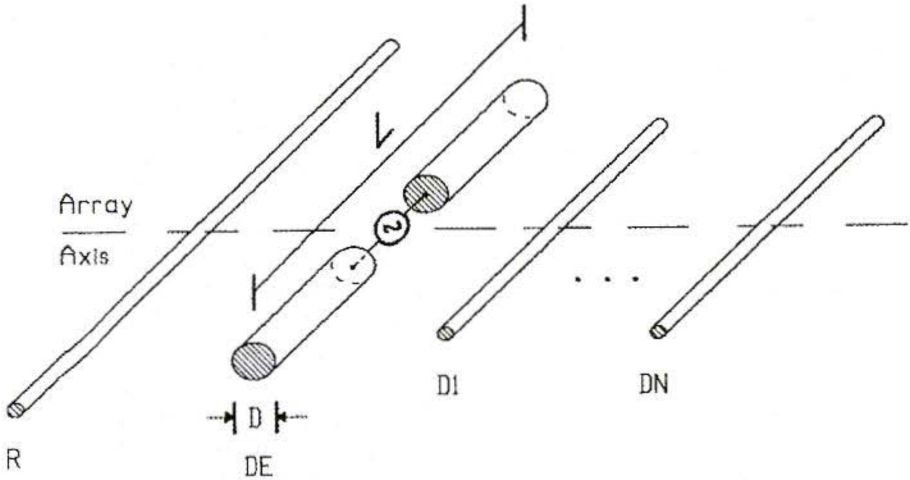

Fig.1: Yagi Array Geometry

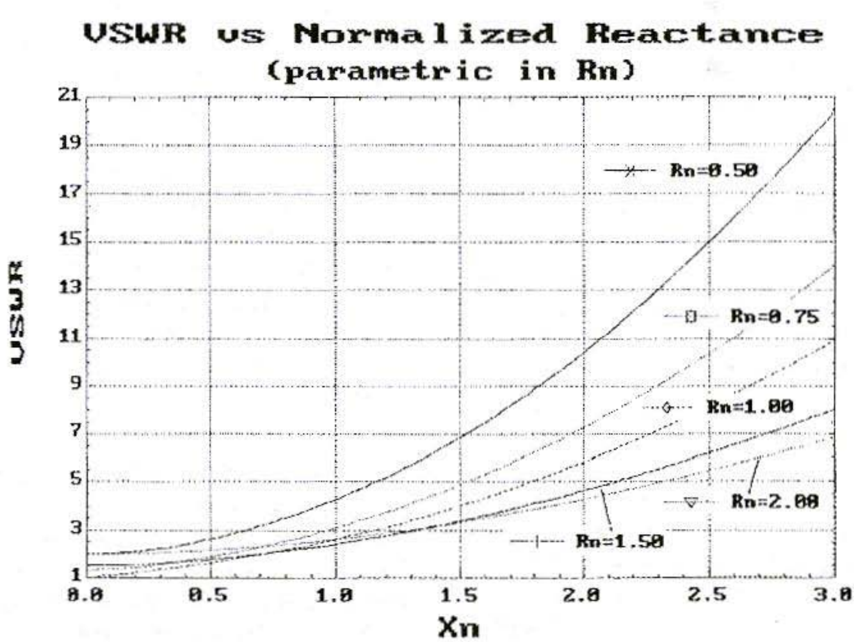

Fig.2: VSWR vs Normalised Reactance

impedance and its mutual impedance with every other element in the array, but the DE's influence is dominant. The design objective is to increase bandwidth by adjusting the DE self-impedance to improve the match to the feed system characteristic impedance.

The conjecture that changing the DE's L/D ratio can significantly alter a Yagi's input impedance rests on the following observations:

- the input resistance of well-designed Yagis is usually lower than 50Ω, often by quite a bit
- in general, VSWR increases more quickly with load reactance when the load resistance is less than the feed system characteristic impedance
- the radiation resistance of a centre-fed dipole passes through a maximum as its L/D ratio decreases

Low input resistance is apparent from published Yagi design data (see, for example, [1]-[5]). The other two observations are discussed below.

Fig.2 plots VSWR vs the magnitude of the normalised load reactance. Several curves are presented for different values of normalised load resistance. Xn and Rn are calculated by dividing the load reactance and resistance, respectively, by the feed system characteristic impedance, Z_o, which is assumed to be purely resistive. In most antenna systems Zo=50+j0Ω. In a 50Ω system, an actual load resistance of 25Ω is a normalised resistance Rn=0.50 (top curve in Fig.2). A load reactance of 125 ohms (Xn=2.5) produces a VSWR of 15. Note that only the magnitude of the reactance is important, not its sign (inductive or capacitive).

It is evident from Fig.2 that VSWR is more sensitive to increases in Xn when Rn is low. For example, increasing Xn from 2.5 to 3 causes the VSWR to go from 15 to 20.5 when Rn=0.5, but only from 5.6 to 6.9 when Rn=2. Because of their low input resistance, Yagis tend to exhibit this sort of VSWR sensitivity. It is reasonable to expect that a DE which increases the Yagi radiation resistance will improve performance by reducing VSWR sensitivity to input reactance. The initial design objective in selecting a better DE configuration is therefore to maximise its radiation resistance.

The self-impedance of a centre-fed, free space dipole is plotted as a function of diameter in Figs. 3(a) and 3(b). The input resistance appears in Fig.3(a). The different curves are for different element lengths as indicated. The dipole diameter varies from zero (infinite L/D) to 0.1 (4.5 <U> L/D <U> 5.0). Note that L and D are in wavelengths. For 0.45 <U> L <U> 0.50 wave, the resistance increases until the diameter is near 0.05 wave, then it decreases. The maximum resistance for a fat dipole is considerably higher than it is for a very thin one, which is important in trying to increase the Yagi's input resistance.

Fig.3(b) plots the dipole's input reactance. A half-wave dipole is inductive for very small diameters, passes through resonance near 0.05 wave, then becomes capacitive. The 0.475 wave dipole shows two resonances, one near a diameter of 0.003 wave, and the other near 0.043 wave. The shortest antenna

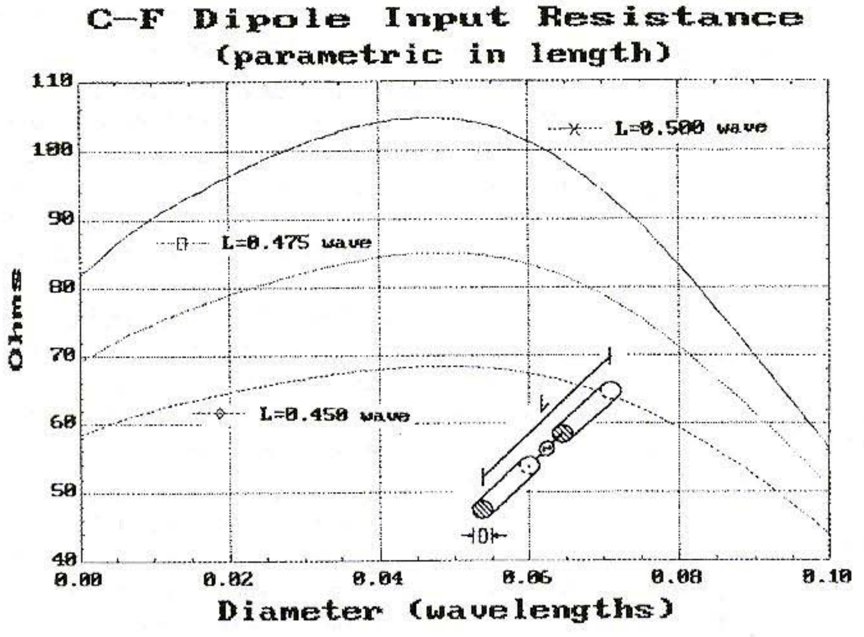
C-F Dipole Input Resistance
(parametric in length)
Ohms
110
100
90
80
70
60
50
40
0.00
0.02
0.04
0.06
0.08
0.10
Diameter (wavelengths)
L=0.500 wave
L=0.475 wave
L=0.450 wave
L
D

Fig.3a

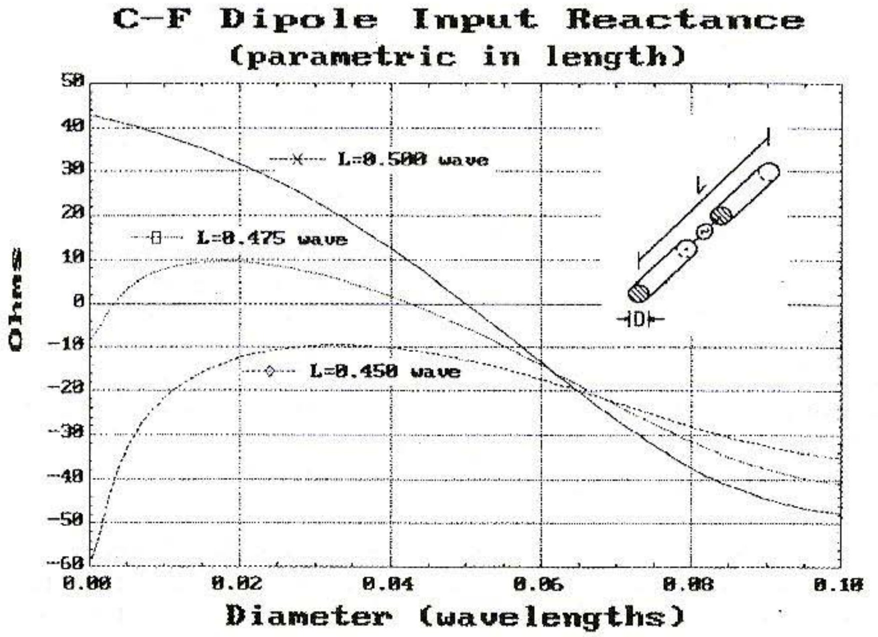
C-F Dipole Input Reactance
(parametric in length)
Ohms
50
40
30
20
10
0
-10
-20
-30
-40
-50
-60
0.00
0.02
0.04
0.06
0.08
0.10
Diameter (wavelengths)
L=0.500 wave
L=0.475 wave
L=0.450 wave
L
D

Fig.3b

(0.450 wave) is always capacitive. How the reactance changes with diameter is important determining the DE resonant frequency; but resonating the DE is not a primary objective at this point.

The effect of L/D on input impedance was investigated by modelling a well-designed, three-element Yagi with thin and fat DEs. The original antenna with the thin DE is referred to as the "prototype". It consisted of a 0.479 wave reflector, a 0.453 wave DE, and a 0.451 wave director. Each element was 0.005 wave diameter. The three elements were uniformly spaced 0.5 wave along the array axis. This antenna is described in [3], Table 5-4.

The modified prototype is referred to as the "improved" array. The only difference between the two antennas is the DE diameter, which was increased to 0.0486 wave (L/D=9.3/90.6, improved array/prototype). This diameter was chosen because it maximises the self resistance of a 0.453 wave dipole (70.23Ω). Other diameters could also be used, since the resistance is not particularly sensitive to changes in diameter between about 0.04 and 0.055 wave.

Prototype antenna performance is shown in Fig.4, and the improved array in Fig.5. The x-axis is the ratio of operating frequency to the design frequency, F_o.

The prototype forward gain and FB ratio are plotted in Fig.4(a). Maximum gain is 9.56dBi at $0.991F_o$, and maximum FB is 6.35dB at $0.979F_o$. The improved array's gain and FB curves are so close to those in Fig.4(a) that they are not reproduced.

Increasing the DE diameter does not affect maximum gain or FB.

Input resistance (R), reactance (X), and VSWR (relative to 50 ohms) appear in Figs. 4(b) and 5(a), which should be compared directly. The most important differences are the improved antenna's higher input resistance (55.9 vs 22.34Ω) and its substantially smaller VSWR variation (1.8-5.7 compared to 2.46-10.7). The improved array's VSWR is much easier to match than the prototype's, which should result in better impedance bandwidth.

Since both antennas are inductive at the design frequency (X=14.4/79.9Ω, prototype/improved array), the simplest matching scheme is to add capacitive reactance to resonate the antenna at F_o. For convenience, it is assumed F_o=299.8 MHz (1 meter wavelength). If series capacitors are used, then the total required capacitance is 36.87pF for the prototype and 6.34pF for the improved array. The effect of adding series capacitance is shown in Figs. 4(c) and 5(b), which should be compared directly.

Note: The details of how reactance is added at the feed point are not considered. A capacitor is the simplest way to add capacitive reactance, but not the only one. Whatever approach is taken, feed system symmetry must be preserved in order to avoid unbalancing the antenna.

The minimum resistance is similar in both designs, but R increases more quickly and reaches higher values in the improved array. This effect is actually beneficial because of the VSWR behaviour discussed in connec-

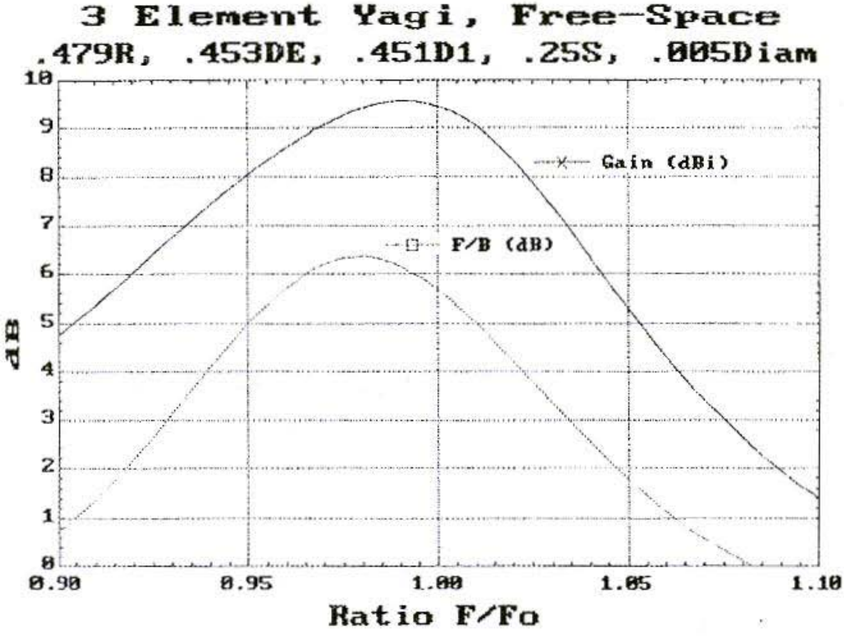
3 Element Yagi, Free-Space
.479R, .453DE, .451D1, .25S, .005Diam
dB
Gain (dBi)
F/B (dB)
Ratio F/Fo
0.90
0.95
1.00
1.05
1.10

Fig.4a

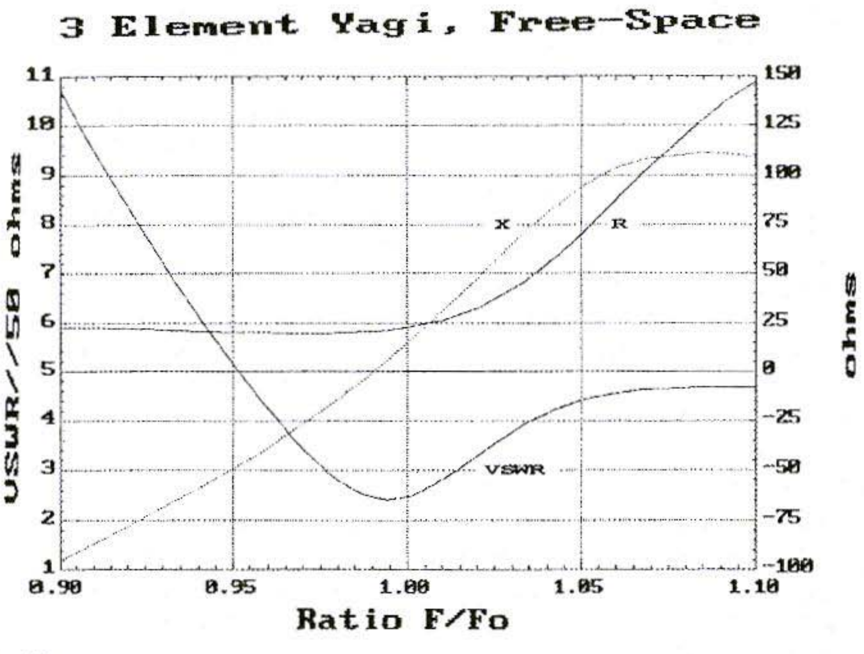
3 Element Yagi, Free-Space
VSWR//50 ohms
ohms
X
R
VSWR
Ratio F/Fo
0.90
0.95
1.00
1.05
1.10

Fig.4b

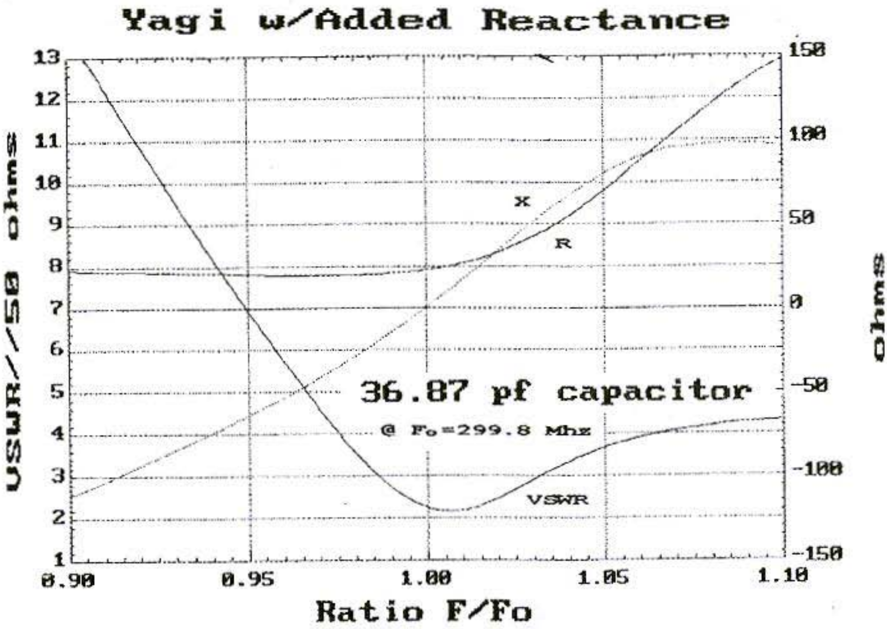

Fig.4c

tion with Fig.2. Maximum resistance in the improved Yagi is about 280Ω near $1.05F_o$.

The series capacitors bring both antennas into resonance (X=0) at F_o=299.8 MHz. The prototype's VSWR is 2.24 at the design frequency, and its minimum VSWR is 2.16 at $1.007F_o$. The reason the VSWR is not better than 2.24 at F_o is that the input resistance is still low compared to the feed system impedance of 50Ω. Comparing the prototype's VSWR with and without added reactance shows that the improvement is only marginal.

Fig.5(b) shows that the fat DE provides much better performance. The VSWR is only slightly above 1:1 at F_o, and it is below 2.5:1 from $0.981F_o$ to $1.014F_o$, an impedance bandwidth of 3.3% of F_o.

The improved antenna's VSWR is better at F_o because its resistance is close to the feed system characteristic impedance of 50Ω. Thus, the larger DE diameter increases the array's radiation resistance as expected. Matching the improved antenna is simply a matter of neutralising its input reactance.

There are several matching techniques not considered here which can improve the VSWR even more. The simplest is to adjust the DE L/D ratio so that both the radiation resistance is as close as possible to 50Ω and the array is resonant at F_o.

Matching networks, impedance matching feeds such as a T-match, or antenna tuners are some of the other possible techniques for improving impedance bandwidth.

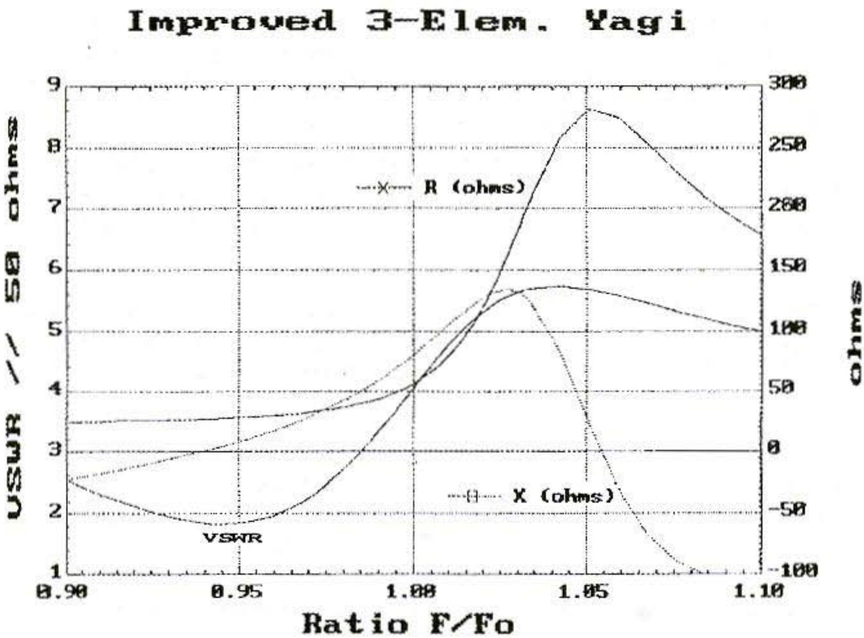
Improved 3-Elem. Yagi
R (ohms)
X (ohms)
VSWR
VSWR // 50 ohms
ohms
Ratio F/Fo
9
8
7
6
5
4
3
2
1
300
250
200
150
100
50
0
-50
-100
0.90
0.95
1.00
1.05
1.10

Fig.5a

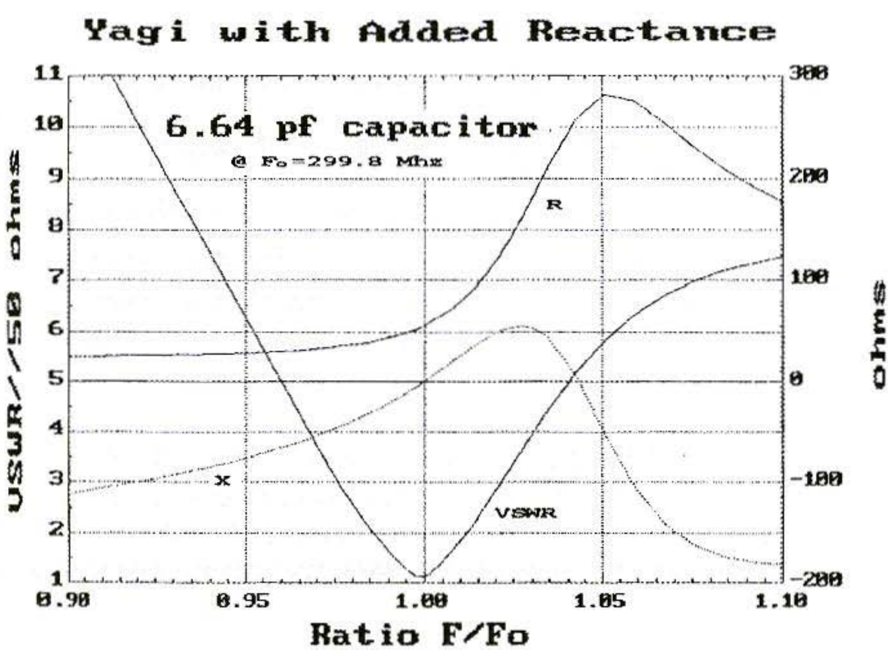
Yagi with Added Reactance
6.64 pf capacitor
@ Fo=299.8 Mhz
R
X
VSWR
VSWR//50 ohms
ohms
Ratio F/Fo
11
10
9
8
7
6
5
4
3
2
1
300
200
100
0
-100
-200
0.90
0.95
1.00
1.05
1.10

Fig.5b

These methods work best with a Yagi whose VSWR has already been lowered using the L/D technique. The data in this tech note provide a starting point for further experimentation and illustrate the degree of improvement attainable with a fat driven element.

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[1] The ARRL Antenna Book, 16th edition, Gerald Hall, K1TD, editor, American Radio Relay League, Newington, CT, 1991.

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[3] Antenna Theory and Design, Warren G. Stutzman, Gary A. Thiele, John Wiley and Sons, New York, 1981.

[4] Antenna Theory, Analysis and Design, Constantine A. Balanis, Harper & Row, New York, 1982, Sect. 9.3

[5] The ARRL Handbook 1993, Seventieth Edition, American Radio Relay League, Newington, CT, Chap. 33

Matjaz Vidmar S53MV (ex YU 3 UMV, YT 3 M)

A DIY Receiver for GPS and GLONASS Satellites Part-3

3. THEORY OF OPERATION OF GPS AND GLONASS RECEIVERS

3.1. GPS/GLONASS Receiver Principles of Operation

Since the signals transmitted by GPS and GLONASS satellites are similar, the receiver design for any of these systems follows the same guidelines. The principle block diagram of a GPS or GLONASS receiver is shown in Fig.11. Only a single channel receiver is shown for simplicity. The problem of simultaneously receiving more than one signal (like the C/A-signal and both P signals from four or more satellites) will be discussed later.

Since the user's position, velocity and attitude are unknown in a navigation problem, satellite navigation receivers generally use either one or more omnidirectional antennas. All satellite navigation signals are circularly polarised (usually RHCP) to allow the user's receiver to further attenuate any reflected waves, since circularly polarised waves change their sense of polarisation on each reflection. Reflected waves are a major nuisance in precision navigation systems: they represent an unpredictable propagation anomaly which is a major source of measurement errors.

The radio signals collected by an omnidirectional receiving antenna are weak. A low-noise amplifier will prevent any further degradation of the signal-to-noise ratio, but it can not reduce the thermal noise collected by the antenna nor unwanted navigation

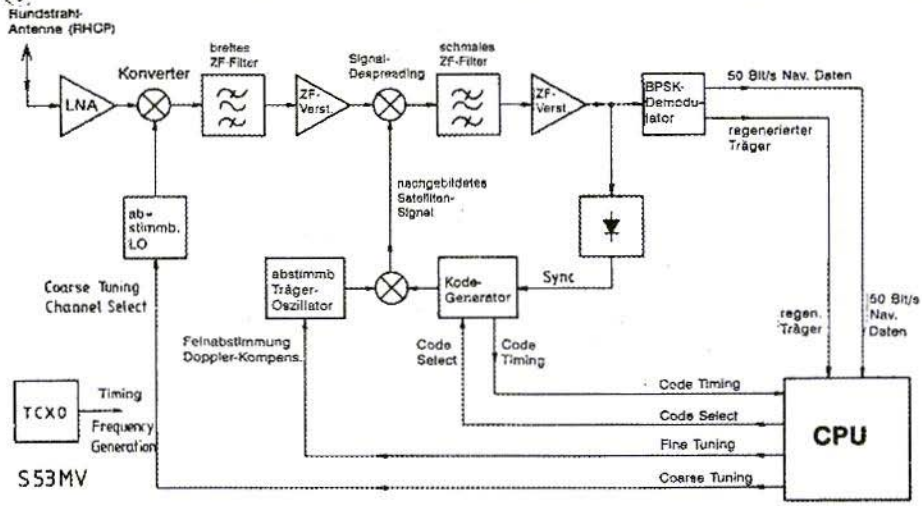

Fig.11: Principle Block Diagram of a GPS/GLONASS Receiver

satellite transmissions on the same frequency. GPS and GLONASS satellite signals are wideband, ranging from 1 MHz (GLONASS C/A-code) to 20 MHz (GPS P-code), and the satellite transmitter power is limited to around 25dBW EIRP (L1 C/A-code for both GPS and GLONASS) or even less than this (P-transmissions), making the signal usually weaker than the thermal noise collected by the antenna.

Although buried in thermal noise and interference, these signals can still be used, since the given bandwidth and megabits-per-second rates apply to a known code and not to the information bandwidth, which is smaller than 1 kHz for both timing and Doppler shift measurements and the navigation data transmitted at 50bps. In other words, GPS and GLONASS signals are direct-sequence spread-spectrum signals, using Code-Division Multiple Access (CDMA) techniques [7].

A GPS or GLONASS receiver will first downconvert the signals to a suitable IF and amplify them before further processing. At this stage a wide IF filter, corresponding to the complete original signal bandwidth, can be used to improve the dynamic range of the receiver. The downconverter may be made tuneable if widely separated channels are to be received, like the GLONASS C/A-transmissions.

The wideband IF signal is then multiplied by (mixed with) a locally-generated satellite signal replica, modulated by the same code. If the locally generated code is synchronised to the satellite transmission, the bandwidth of the desired mixing product will collapse down to almost zero, since two identical 0/180-degrees BPSK modulation processes exactly cancel each other. on the other hand,, the bandwidth of all unwanted signals, like noise or interference, will be further expanded by this operation to a double bandwidth.

Since the bandwidth of the desired signal collapses, this operation is usually called signal spectrum despreading. The desired signal can now be filtered-out with a narrow IF filter having a bandwidth ranging from 100 Hz to 10 kHz in a GPS or GLONASS receiver. After the narrow IF filter, the signal-to-noise ratio finally achieves usable values and typically reaches 20dB.

The filtered IF signal is then used for several purposes. First, it is used to acquire and maintain synchronisation of the locally generated code. Dithering the locally-generated code back and forth by a fraction of the bit period generates an amplitude modulation on the filtered signal. The phase of this modulation contains the information required to keep the synchronisation of the local code generator.

The filtered IF signal is also fed to a BPSK demodulator (usually a squaring PLL or a Costas PLL) to extract the 50bps navigation message data. The BPSK demodulator also provides a regenerated carrier that is used for Doppler-shift measurements. On the other hand, the code-timing information is obtained from the local code generator. All three signals, code timing, Doppler shift and 50bps navigation data are fed to the receiver CPU to compute the user position, velocity, accurate time etc.

For Earth-located,, slowly-moving users, the Doppler shift on the satellite signals is mainly due to the satellite motion and amounts up to +/- 5 kHz on the L1 frequency. In most cases some fine tuning will be required to compensate the Doppler shift in front of the narrow IF filter. Some fine-tuning capability is also required to compensate the local oscillator frequency drift. In GPS and GLONASS receivers all of the required frequencies are obtained from a single TCXO with a stability of a few parts per million. Since one part per million is 1.6 kHz at the L1 frequency, the frequency uncertainty of the receiver is comparable in magnitude to the expected Doppler shift.

Like in all spread-spectrum-systems, the initial code sync acquisition is a critical operation in a GPS or GLONASS receiver. Most receivers make an exhaustive search for C/A-code synchronisation. Testing a possible code phase typically takes around 10 milliseconds each, so an exhaustive search may take more than 10 seconds. This figure needs to be multiplied by the number of frequencies tested, due to an unknown Doppler shift or unpredictable TCXO drift.

A "cold start" of a GPS or GLONASS receiver may therefore take up to one hour, since the receiver does not know which satellite (PRN# or CHN#) to look for nor the Doppler shift nor the code phase. A "warm start" is much faster since the receiver should know the almanac satellite ephemeris, the approximate user location and the approximate time. From this information one can get all visible satellites and compute the corresponding Doppler shifts, so that the code phase and the TCXO drift are the only unknowns left.

The period of the P-code is far too long to make an exhaustive sync search practical. All P-code receivers need to acquire the C/A-code first, decode the navigation data and synchronise their local P-code generator to the C/A-code transmission first. Since the P-code rate is only 10 times the C/A-code rate, there are very few possible P-code phases left to be tested to lock on the P-transmission.

GPS and GLONASS have been designed to supply timing codes, the user position being computed from the measured propagation time differences. Additionally, the user velocity can be computed from the already known position and the measured Doppler-shift differences on the signal carriers.

Although the Doppler shift can also be measured on the code rates, this measurement is usually very noisy. On the other hand, no absolute delay difference can be measured on the carrier, since the carrier phase becomes ambiguous after 360 degrees.

Finally, relating the carrier phase to the code phase may produce excellent results, but requires an accurate compensation of ionospheric effects, which have opposite signs: the ionosphere delays the modulation and at the same time advances the carrier phase!

Besides the described principle of operation of a GPS or GLONASS receiver, there are some other possibilities. For example, the C/A-code sync could be obtained much faster using an analogue (SAW) or digital (FFT) correlator. To evaluate ionospheric errors, codeless reception techniques can be used to receive both P-transmissions on L1 and L2 frequencies without even knowing the codes used.

3.2. Digital Signal Processing (DSP) in GPS/GLONASS receivers

After the principles of operation and the required functions of an electronic circuit are known, one has to decide about the technology to practically implement the circuit. In most cases GPS or GLONASS receivers are mobile units installed on vehicles or even portable handheld units. The receiver weight, size and power-consumption are all important. While every GPS or GLONASS receiver must have an antenna, a RF front-end and a digital computer to solve the navigation equations, the IF signal processing may include just a single channel in a simple C/A-only receiver or more than 10 channels in a full-spec L1 & L2 P-code receiver.

When the same circuit function needs to be duplicated several times, like the IF processing channels in a radio-navigation receiver, it is usually convenient to use Digital Signal Processing (DSP) techniques. An important advantage of DSP over analogue circuits is that duplicated channels are completely identical and require no tuning or calibration to accurately measure the difference in the time of arrival or Doppler shift of radio-navigation signals. A single DSP circuit can also be easily multiplexed among several signals, since the internal variables of a DSP circuit like a PLL VCO frequency or phase can be stored in a computer memory and recalled and updated when needed again.

The bandwidth of the navigation satellite signals is several MHz and this is a rather large figure for DSP. Implement-

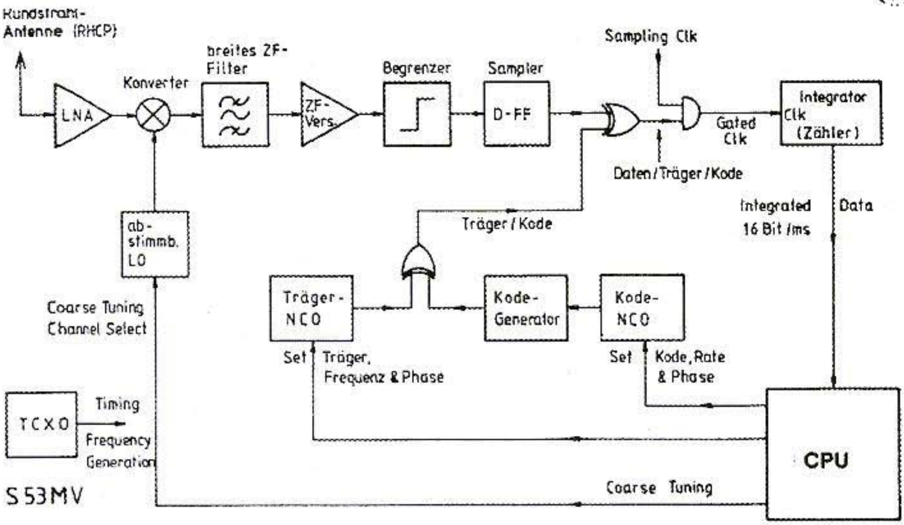

Fig.12: Principle Block Diagram of a 1-bit DSP GPS/GLONASS Receiver

ing the whole IF signal processing of a GPS/GLONASS receiver completely in software (like described in the introduction to DSP techniques in [8]) is difficult although it has been done [9] for the GPS C/A-code using powerful microcomputers. Most GPS/GLONASS receivers use a combination of dedicated DSP hardware and software for IF signal processing. Dedicated DSP hardware is only used where the bandwidth is large and the functions are relatively simple, like the local satellite signal replica generation and the signal despreading, while all other functions, including all feedback loops, are implemented in software.

When designing a DSP circuit and in particular when designing dedicated DSP hardware it is essential to know, besides the signal bandwidth or sampling frequency, also the resolution or number of bits per sample required to represent the signals involved [10]. A GPS or GLONASS signal is a constant amplitude signal and limiting is therefore not harmful. However, after the wide IF filter in the receiver there is a mix of many satellite signals of different strength and lots of thermal noise as well. If such a mix of signals is limited, the resulting intermodulation distortion degrades the signal-to-noise ratio by around 2dB.

Since navigation satellite signals are pseudo-random sequences, all undesired signals and all intermodulation products only affect the desired signal in the same way as thermal noise. Therefore, in a GPS/GLONASS receiver, very few bits are required to represent the wideband IF signal. Most GPS/GLONASS receivers simply limit the wideband IF signal, thus accepting the 2dB sensitivity degradation and representing each sample with just two quantisation levels or one single bit. Increasing the number of bits per sample only increases the

DSP hardware complexity while bringing marginal sensitivity improvements, so that no known receiver design uses more than 3 bits per sample (8-level quantisation).

On the other hand, an 1-bit/sample DSP GPS/GLONASS receiver may have a really simple IF signal processing as shown on the principle block diagram on Fig.12. The IF signal is limited, so no AGC is required. Signal sampling and A/D conversion is performed by a single D type flip-flop. Signal despreading or multiplication with the locally generated signal replica is accomplished with an exclusive-or gate. Since the narrow IF can be selected close to zero, the narrow IF bandpass filter may be replaced by a lowpass filter or an integrator. In the case of 1-bit samples, the latter is simply a counter with the clock set to the sample rate and gated by the input signal.

However, after the narrow IF filtering the resulting signal can no longer be represented with a single bit per sample, if the sample rate of the narrowband signal is significantly reduced. In a C/A-code receiver, the integrator is read and then reset each millisecond, to match the period of either GPS or GLONASS C/A-codes, since the auto- and cross-correlation properties of these codes are only maintained over an integer number of code periods. An integration period of 1 ms corresponds to a narrow IF bandwidth of +/- 500 Hz around the centre frequency. The latter is a very good choice for a GPS or GLONASS receiver.

Any further signal processing after the integration can be conveniently performed in software, since an interrupt rate of only 1 kHz can be accepted by any microprocessor. The accumulated data in the integrator has a resolution of 12 to 14 bits, so any further software processing can be done without any loss of quantisation accuracy nor processing speed of a general-purpose 16-bit microprocessor.

Dedicated hardware is also required for the generation of the local signal replica. Carriers or rates are conveniently generated in Numerically Controlled oscillators (NCOs). An NCO includes a digital adder and an accumulator. In every clock cycle, a constant representing the desired output or rate is added to the accumulator. If an analogue output were desired, the accumulator content could be fed to a ROM containing a sine table and then to a D/A converter, forming a direct digital frequency synthesiser.

In a 1-bit DSP navigation-receiver the sine table and D/A converter are not required. Since the DSP hardware operates with 1-bit data, it is sufficient to take the MSB of the NCO accumulator as the frequency output. Two NCOs are required: on for the carrier frequency and another for the code rate. The code-rate NCO supplies the clock to a code generator like the ones shown on Fig.8 or 10. The output of the code generator is exclusive-or gated with the output of the carrier NCO to produce a BPSK-modulated satellite signal replica.

Of course both NCOs have to be accurately steered to the required frequency and phase to maintain lock on the incoming signal. The feedback function can be performed by the microprocessor, since the feedback speed is very low: a 100 Hz update rate is usually fast enough. Finally, the NCO frequency can be easily steered modifying the addition constant and the NCO phase can be easily steered modifying the accumulator content. In a time-multiplexed IF channel, both can be easily stored by the microprocessor and recalled when the channel hardware is switched back to the same satellite signal.

From the technology point of view, a DSP IF channel can be built on an "Eurocard" size printed circuit board using just bare 74HCxxx logic. A single IF channel may also be programmed in a programmable-logic integrated circuit. Finally, the complete IF signal processing with 6 or 8 independent channels may be integrated in a single custom integrated circuit. Commercial satellite navigation receivers use custom integrated circuits essentially to prevent unauthorised duplication. On the other hand, bare 74HCxxx logic is preferred for an amateur, home-made receiver. Hopefully programmable-logic ICs will some day become standardised and the necessary programming tools cheap enough to allow amateur applications.

3.3. Multi-channel reception of navigation signals

A satellite navigation receiver should be able to receive the signals from four or more satellites at the same time, to be able to measure time and Doppler differences. When the GPS specifications were published back in 1975 [4], the digital computer was the largest and most complex part of a satellite navigation receiver. Both GPS and GLONASS receivers were initially intended to have several analogue IF processing channels, one per each signal type per satellite. Since these receivers were intended for military vehicles like fighter aircraft, tanks or battle ships, the price and complexity of several analogue IF processing channels was almost unimportant.

Early civilian GPS receivers also used analogue IF processing, although initially limited to the C/A-code and one or two time-multiplexed IF channels. Time-multiplexing is difficult with analogue IF channels, since the latter have to reacquire lock each time the satellites are changed. Lock Acquisition may take 15 to 20 seconds, so that the measurement loop through four or more satellites takes several minutes. These receivers were only suitable for stationary or slowly-moving users.

The introduction of DSP techniques and inexpensive computers allowed much faster multiplexing. Since the variables of a DSP circuit can be stored and recalled, a DSP IF channel does not need to reacquire lock each time it is switched to another satellite signal. A DSP IF channel is typically switched among satellite signals around a hundred times per second making the whole loop among all required signals a few ten times per second. However, because of the available signal-to-noise ratio, the navigation solution in a C/A-code receiver only needs to be computed about once per second.

All current commercial GPS and GLONASS receivers use DSP IF processing.

Small handheld C/A-code receivers have one, two or three time-multiplexed IF channels. Mobile C/A-code receivers have 5, 6 or even 8 independent channels so that no multiplexing is required. Time multiplexing makes the carrier lock and Doppler measurements difficult and unreliable, so it is undesired in mobile receivers.

Unfortunately, multi-channel GLONASS receivers require a wider raw signal IF and a much higher sampling rate due to the wide FDMA channel spacing. On the other hand, GPS receivers require the same raw IF bandwidth regardless of the number of channels thanks to CDMA. The higher sampling rates required for GLONASS are a little impractical with currently available integrated circuits. Maybe this is another reason why GPS receivers are more popular and GLONASS is almost unknown. Since faster ICs will certainly be available in the future, one can expect that combined GPS/GLONASS receivers will become standard.

In this article I am going to describe a single-channel C/A-only receiver using fast time multiplexing. This receiver can be built in two versions: GPS or GLONASS. Although both versions use the same modules as much as possible, this is not a combined GPS/GLONASS receiver yet. The main limitation of a single IF channel, time-multiplexed receiver is that the maximum number of simultaneously tracked satellites is limited to four or five, so that a combined GPS/GLONASS receiver does not make much sense.

3.4. Practical GPS receiver design

The block diagram of the described GPS receiver is shown on Fig.13. In the microwave frequency range, at L-band, the antenna needs a direct visibility of the satellites. Therefore it has to be

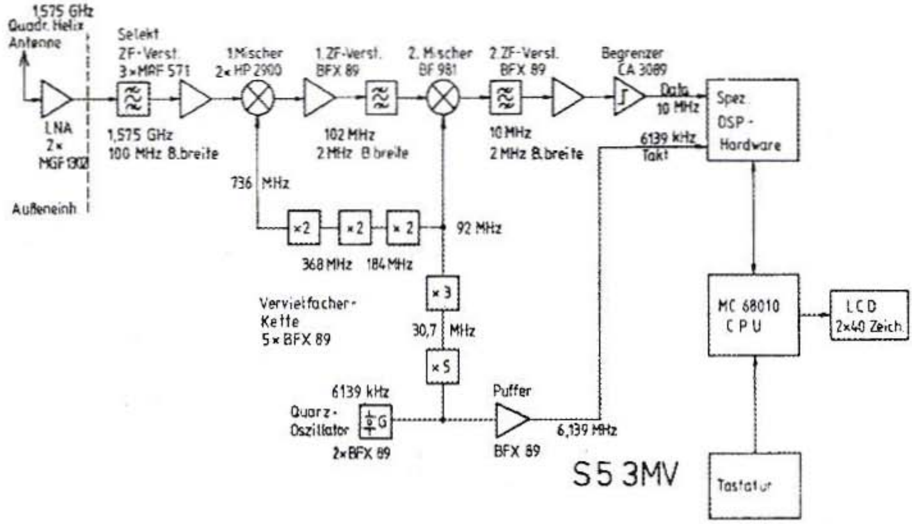

Fig.13: GPS Receiver Block Diagram

installed outdoor, on the vehicle roof or on top of a portable receiver. Due to its excellent performance, a half-turn quadrifilar helix is used as a circularly polarised, hemispherical-coverage antenna.

The LNA is installed directly under the antenna. Using two inexpensive GaAs-FETs it achieves 30dB of gain making any following (reasonable) cable loss almost unimportant.

The GPS receiver includes a fixed-tuned downconverter to a suitable IF, an IF amplifier and limiter, a dedicated DSP hardware, a MC68010 based microcomputer with a small keyboard and a LCD display and a single master crystal oscillator for all frequency conversions and sampling rates. The down-conversion from the GPS L1 frequency (1575.42 MHz) is made in two steps for convenient image filtering. The first wide IF is in the 102 MHz range and the second wide IF is in the 1O MHz range. The wide IF bandwidth is set to around 2 MHz. The actual value of the wide IF bandwidth is not critical, since filtering is only required to prevent spectrum aliasing in the signal sampling circuit.

A frequency of 6139 kHz was selected as master crystal oscillator frequency of the described GPS receiver, since the best TCXOs are usually available for the frequency range between 5 MHz and 10 MHz.

The output of the 6139 kHz master oscillator is used both as the sampling frequency for the IF A/D conversion and as an input to a chain of multiplier stages to supply all of the frequencies required in the downconverter. Limiting the temperature range from 0 to 30 degrees C, as encountered during normal receiver operation, the TCXO was replaced by a much less expensive conventional crystal oscillator in all of the prototypes built.

Sampling the 10 MHz wide IF signal with 6139 kHz produces a third down-conversion to a 2303 kHz nominal centre frequency. The latter is the final carrier frequency that needs to be regenerated in the dedicated DSP hardware. The dedicated DSP hardware is designed as a microprocessor peripheral with read and write registers and is interrupting the MC68010 CPU once every millisecond to match the GPS C/A-code period.

In the portable, stand-alone GPS receiver, the operating software is stored in a compressed form in a 32kbyte EPROM. After power-on reset, the software is decompressed in 128kbytes of battery-backed CMOS RAM, which is also used to store the system almanac and other data to speed-up the acquisition of four valid satellites. For the same reason the CPU also has access to a small battery-backed real-time clock chip.

A small 8-key keyboard is used to select the various menus of the operating software and manually set some receiver parameters if so desired. The portable version of the GPS receiver is using a LCD module with integrated driving electronics and two rows of 40 alphanumeric (ASCII) characters each, to display the receiver status, the almanac data or the results of the navigation computations.

3.5. Practical GLONASS receiver design

The block diagram of the described GLONASS receiver is shown in Fig.14. The GLONASS receiver uses the same type of antenna and LNA and the same dedicated DSP hardware and micro-computer as its GPS counterpart. The main difference between the two receivers is in the downconverter. The GLONASS receiver includes a tuneable downconverter, otherwise the wide FDMA channel spacing would require impractically high sampling rates in the dedicated DSP hardware.

The downconversion from the GLONASS L1 frequency range (1602 to 1615.5 MHz) is made in two steps for convenient image filtering. To reduce group-delay variations, the first conversion is made tuneable and the second is fixed. . n this case the only contribution to group-delay variations across the GLONASS L1 frequency range are the tuned circuits at 1.6 GHz. Group-delay variations introduce errors in the measured time differences, so they immediately affect the accuracy of a navigation receiver. This problem does not exist in a GPS receiver, since all GPS satellites transmit on the same carrier frequency and any signal filtering produces the same group delay on all satellite signals that exactly cancels-out when computing the differences.

Both wide . Fs are fixed tuned at 118.7 MHz and 10.7 MHz respectively. To avoid any group-delay variations in the wide . Fs, the frequency synthesiser steps must accurately match the channel spacing so that all signals are converted to the same . F values. Finally, the . F limiter should not introduce a variable

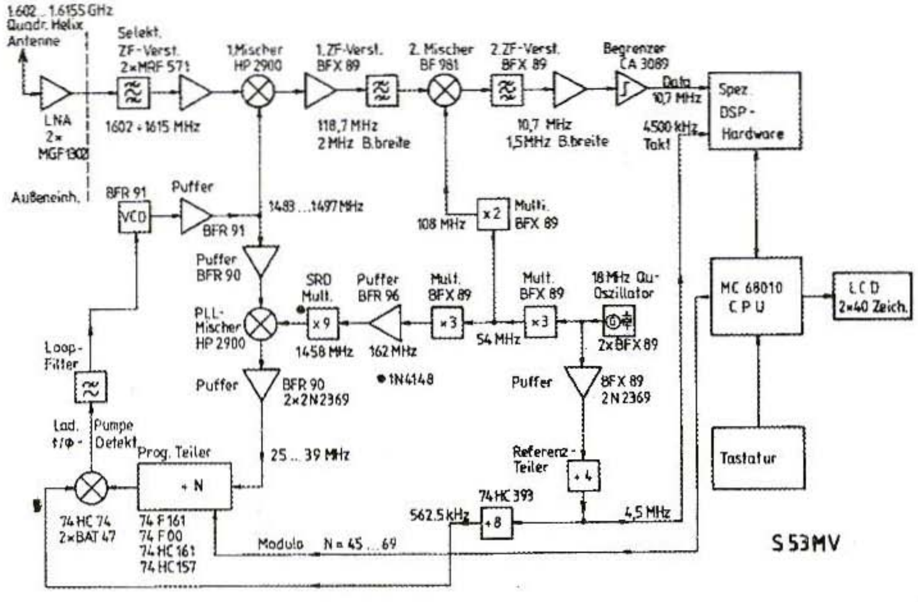

Fig.14: GLONASS Receiver Block Diagram

delay as the input signal strength is changed when switching among channels. The second wide IF signal at 10.7 MHz is sampled with 4500 kHz producing a third downconversion to a nominal centre frequency of 1687.5 kHz.

There are several difficult-to-meet requirements for the frequency synthesiser supplying the signal for the first conversion. This synthesiser has to provide a clean signal in the frequency range from 1483 to 1497 MHz in steps of 562.5 kHz. Its phase noise should be low enough to allow carrier lock and 50bps navigation data demodulation: its spectral linewidth should be about 10 times narrower than required in a voice SSB receiver. Finally, in a time-multiplexed, single-channel receiver the synthesiser should be able to switch and settle to another frequency in less than 1 ms the GLONASS C/A-code period, to avoid increasing the switching dead time.

The frequency synthesiser is a PLL with a frequency converter in the feedback loop, to decrement the divider modulo, increase the loop gain, speed-up the settling and improve the output phase noise performance. The feedback signal is downconverted to the frequency range 25 to 38 MHz, so that a very low programmable loop-divider modulo between 45 and 69 is required. The comparison frequency is set to 562.5 kHz.

A well-designed PLL will settle in 100 to 200 clock periods of the comparison frequency and the described PLL achieves this performance with a settling time between 200 and 300 microseconds.

The described GLONASS receiver is using a master crystal oscillator at 18.000 MHz. This frequency is multiplied by 6 to obtain the 108 MHz signal required for the second conversion and by 81 to obtain the 1458 MHz signal required for the PLL feedback-loop conversion. The master oscillator frequency is divided by 4 to obtain the 4500 KHz sampling frequency and by 32 to obtain the 562.5 kHz PLL reference frequency. Like in the GPS receiver, in place of an expensive TCXO conventional crystal oscillators were used in all of the prototypes built, limiting somewhat the operating temperature range.

In the described GLONASS receiver, the microcomputer has one function more. Besides controlling the dedicated DSP hardware, keyboard and LCD display, all identical to the GPS counterparts, the microcomputer has to set the frequency synthesiser when switching among channels. The operating software is very similar to that in the GPS receiver and has the same hardware requirements: 32kbytes of EPROM, 128kbytes of battery-backed CMOS RAM and a battery-backed real-time clock.

3.6. GPS/GLONASS dedicated DSP hardware design

Although the theory of operation of an 1-bit DSP GPS or GLONASS receiver has already been discussed, the practical implementation still offers many different choices and some additional problems to be solved. For example, from the theoretical point-of-view it is unimportant whether the code lock or the carrier lock is achieved first. In practice, the code lock should be achieved first and should be completely independent from the carrier lock, both to speed-up the initial signal acquisition and to avoid loosing lock at short signal dropouts (obstructions, fading) or receiver frequency reference instabilities.

The block diagram of the practically implemented GPS/GLONASS dedicated DSP hardware is shown on Fig.15. Although the implemented hardware is intended for a single channel, time multiplexed operation, it differs significantly from the theoretical block diagram shown on Fig.12. The main difference is that there are four signal-despreading mixers (multipliers, ex-or gates) and four integrators (counters) for one single channel.

In practice, two separate signal-despreading mixers are required when downconverting to a narrow IF of almost zero. The mixers are driven with the same satellite signal replica, modulated with the same code, but with the carriers in quadrature. In this way no information is lost after signal despreading, downconversion and integration. The code lock can be made completely independent from the carrier lock, since the narrow IF signal amplitude-can be computed out of the I and Q integration sums without knowing the carrier phase. The same I and Q integration sums are used in a different way to achieve carrier lock and extract the 50bps navigation data. Due to the low sample rate (1 kHz) the latter are conveniently performed in software.

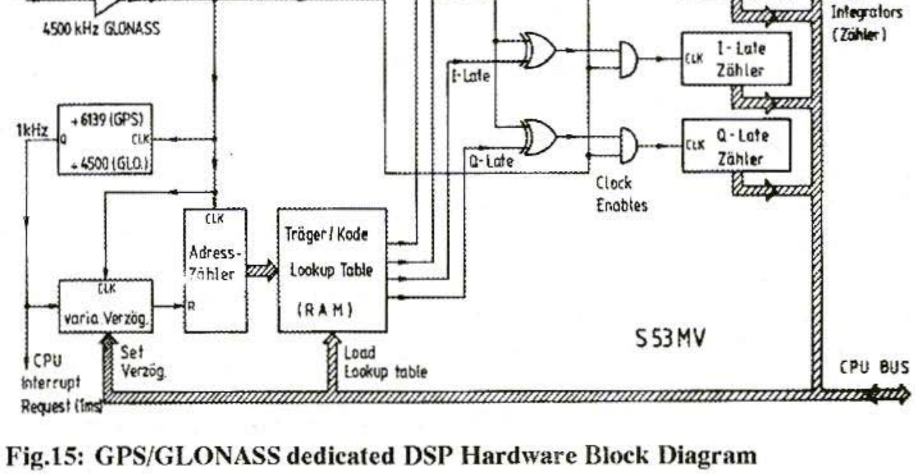

Fig.15: GPS/GLONASS dedicated DSP Hardware Block Diagram

Although code lock may be maintained by dithering the locally generated signal replica, two separate narrow IFs for an "early" and a "late" local signal replica provide a 3dB improvement in the signal-to-noise ratio on time-delay measurements. The former solution, code dithering, is usually used in receivers with an analogue narrow IF, since it is difficult to build two identical circuits in analogue technology. The latter solution is used in receivers with a DSP narrow IF, since DSP circuits perform the same numerical operations and are therefore mathematically identical.

To achieve the 3dB signal-to-noise improvement, two separate sets of I and Q signal-processing chains for the nearly" and "late" signal replicas need to be used. This brings the total number of signal-despreading mixers and integrators to four. Of course the local signal replica generation includes the generation of four different signals: I-EARLY, Q-EARLY, I-LATE and Q-LATE. All these signals can be obtained from a single carrier and code generator, since they are merely delayed versions of the same signal: either the carrier or the code or both are delayed. In DSP, delays can be easily obtained with shift registers.

On the other hand, the local satellite signal replica generation can be simplified with a look-up table. Since the integration period is 1 ms and the input sample rate is 6139 kHz (GPS) or 4500 kHz (GLONASS), there are only 6139 or 4500 different bits to be stored in the look-up table for each despreading mixer and integrator. The look-up table is written by the microcomputer since it does not need to be updated very frequently.

The carrier frequency only needs to be updated less than once per minute while the carrier phase can be adjusted in software since both I and Q integration sums are available. The code rate does not need to be adjustable if the code phase can be corrected every 10 milliseconds. For the latter reason the code phase is made adjustable in hardware by a variable-delay circuit.

The variable-delay circuit used to adjust the code phase also brings a disadvantage. The carrier frequency can only be adjusted in steps of 1 kHz, since the carrier phase should be continuous when the address counter reaches the end of the look-up table and is reset back to the beginning. The carrier frequency error can therefore reach +/- 500 Hz and although it is compensated in software, it degrades the sensitivity of the receiver by up to 4dB (at +/- 500 Hz error).

There are several ways to avoid this problem, like two separated code and carrier look-up tables or a double-length table with a presettable address counter. However, in practice the simplest circuit was preferred in spite of the 4dB sensitivity penalty. Both GPS and GLONASS receiver prototypes are therefore using the simple look-up table generator described above.

The local signal replica generation also explains the choice of the input sampling rates and wide IF nominal centre frequencies. Ideally, to avoid spectrum aliasing the wide IF nominal centre frequency should be equal to 1/4 of the sampling rate or any odd multiple of this value: 1536 kHz for GPS or 1125 kHz for GLONASS.

In practice 6139 kHz was selected as the sampling rate for the GPS receiver to avoid interference with the GPS C/A-code rate (1023 kHz), since the described look-up table generator maintains a fixed phase relationship between the code transitions and sampling rate. Considering the various conversion frequencies obtained from the same source, an IF of 2303 kHz resulted after signal sampling.

In the GLONASS receiver, any interference between the sampling rate and code rate are unimportant since all satellites use the same C/A-code. The sampling rate of 4500 kHz was chosen for convenience. Considering the operation of the frequency synthesiser, the final wide IF value could be chosen in 562.5 kHz steps. The value of 1687.5 kHz was selected to avoid some spurious frequencies generated in the synthesiser.

Finally, the described dedicated DSP hardware always requires the support of a microcomputer. The latter should compute and load the look-up tables first. After each interrupt request (every millisecond) the microcomputer reads all four integrated sums. From the I and Q components it computes the early and late magnitudes used to search and maintain code lock. The code phase required to maintain lock is at the same time the result of a time-delay measurement, referenced to the receiver clock. The difference of two such measurements is a parameter of a navigation equation.

On the other hand, the I average and Q average are supplied to a Costas-loop demodulator to recover the carrier and demodulate the 50bps navigation data bits. Then the subframe or line sync is detected to format the data stream and check the parity bits before the navigation data is used in the computations.

10. LITERATURE

All literature references in this article are to be found on page-77 of issue 2/94

(To be continued)

Dr. Ing. Jochen Jirmann, DB1NV

Radio-Astronomical Experiments in the 70cm Band

At the 1990 VHF-UHF Congress, Hermann Hagn - DK8CL - presented the first results obtained from his amateur radio telescope using a 3m mirror. The following article demonstrates how, by using a different signal processing technique, you yourself can detect cosmic radio emissions using a single 19-element Yagi.

1. SELECTING THE OBSERVATION FREQUENCY

The stimulus to getting involved in radio-astronomical experiments came from DK8CL's paper at VHF-UHF 90 (1), which investigated cosmic radio emissions in the frequency range around 1.72 GHz. Since not every amateur has a fully mobile 3m mirror, the obvious question was whether you couldn't also work with simpler Yagi aerials. With this in view, the first matter to be clarified is the optimal observation frequency.

In the present state of receiver technology, extremely low noise factors can be easily attained, even in the gigaHertz range, so that no clue can be derived from this. In the end, the thermal noise from the receiver installation is caused by the "black body radiation" which all warm bodies transmit, and the spectrum distribution of which is described by Planck's law of radiation.

In the high-frequency and microwave ranges, we describe the noise properties of an amplifier in terms of the noise temperature. The noise output of an ohmic resistance is described using the known equation:

$$Pr = kT_0B$$

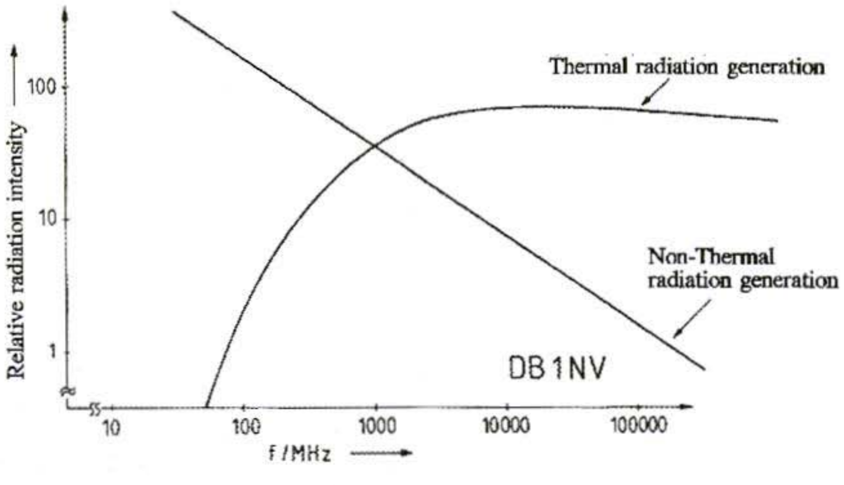

Fig.1: Radiation Properties of Astronomical Objects in the Microwave Range

where

k = $1.38*10^{-23}$Ws/K Boltzmann constant

T_0 = Absolute temperature in degrees Kelvin

B = Signal bandwidth in Hertz

This is also known as the Johnson approximation. Here the noise output is independent of the frequency and is conditioned only by the temperature and the band width. The noise temperature of an amplifier is the temperature of a moving load at the input, at which the amplifier noise is equal to the resistance noise. Even a few astronomical objects, such as the Sun and the Moon, emit predominantly thermal radiation, corresponding to their surface temperature. Depending on the optical density of the object, we receive noise output densities which are either constant or rising with the frequency.

Anyone wanting to know more about thermal radiation and how it can be described mathematically will find further information in (2) and (3). Most radio-astronomical sources also generate radiation through non-thermal processes, such as synchrotron radiation from electrons moved in the magnetic field. Non-thermal radiation is characterised by a power density which decreases as the frequency increases, in accordance with (4). Fig.1 from (4) gives a much simplified picture of the spectrum distribution of thermal and non-thermal radiation sources.

Apart from the Sun, the most powerful radio sources are mainly of non-thermal origin. So it seems sensible to choose a low observation frequency for our first experiments. The lower limit will be determined by the dimensions of the aerial and the level of interference from the atmosphere, domestic appliances and industry, which increases below 1 GHz. Even professionals sometimes accidentally include home-made interference signals in their measure-

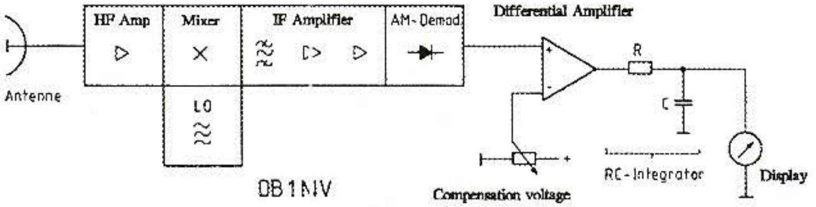

Fig.2: A Radio-Astronomical Direct Receiver

ments, and many "pulsars" have turned out to have their origins in an electric fence in a nearby pasture.

So the author decided to carry out his experiments in the 70cm band. This frequency is not far from a standard radio-astronomical observation band (406 - 410 MHz).

2. RECEIVER TECHNOLOGY

The simplest radio-astronomical receiver, which is also the type used in (1), is shown in outline in Fig.2. After multiple amplification and frequency conversion, the input signal reaches a rectifier which demodulates the noise signal. The output voltage contains a large fraction stemming from the residual noise of the receiver installation and a small, variable fraction from the radio source in space. So we subtract an adjustable DC voltage, which corresponds to the receiver noise

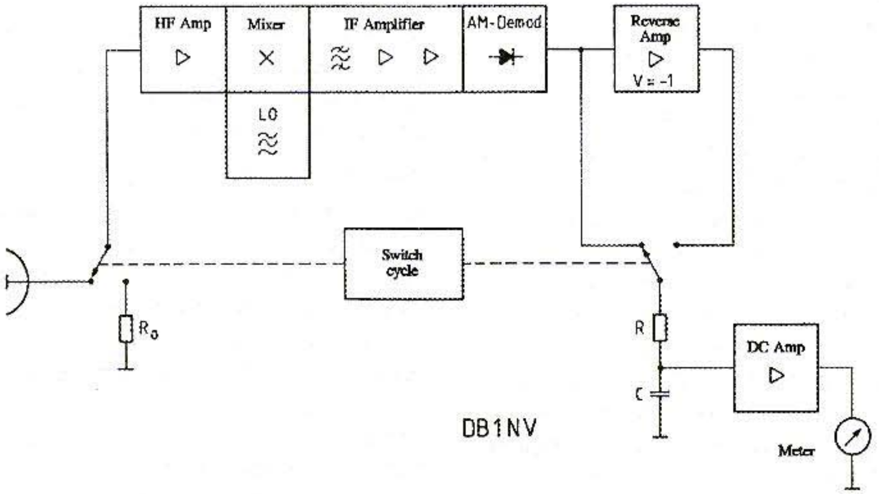

Fig.3: A Radio-Astronomical Receiver as per the Compensation Principle (Dickie Receiver)

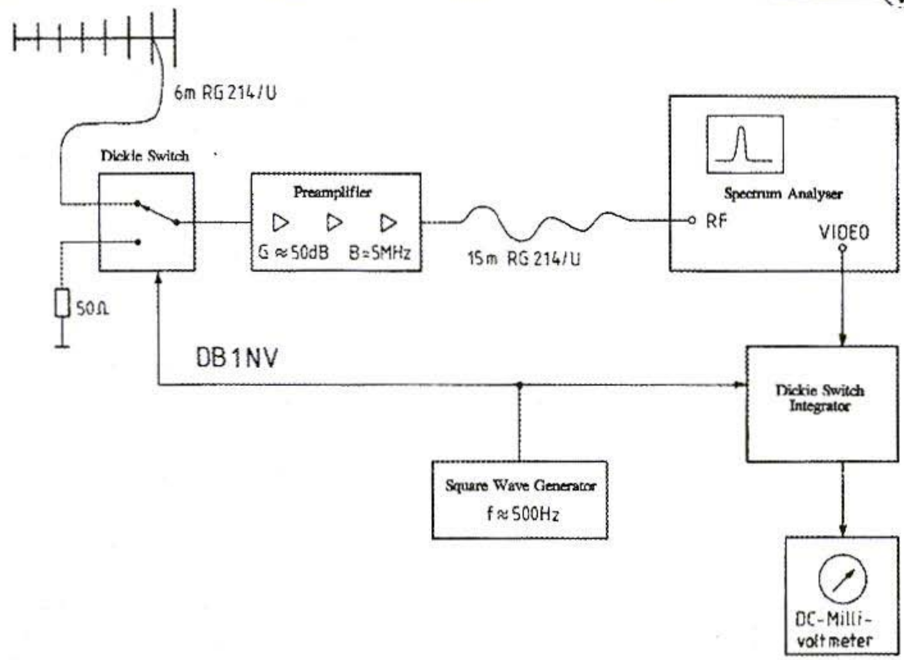

Fig.4: The Author's Dickie Receiver

and greatly increases the difference. An RC module with a long time constant in the seconds range provides information on the static oscillations of the noise level, and the smoothed voltage controls the display instrument or the recorder.

The disadvantages of this layout are obvious. If the noise reading of the receiver or its amplification oscillates to only a minimal extent, then this immediately shows through in the output as zero point drift.

Since these problems were actually much more serious in the valve era, the radio-astronomer Robert Dicke, of the Massachusetts Institute of Technology, developed a solution in 1946, which is still called a "Dicke receiver" today. Fig.3 shows the outline layout. At the input of the receiver is mounted a switch, which periodically connects the receiver with the aerial or with a terminating load. At the receiver output is a second, synchronously operating switch, which continuously switches the inverted output voltage to the output-side low pass filter when the receiver is connected to the terminating load.

Thus the receiver noise is periodically subtracted from the total signal. As can easily be comprehended, a (slow) change in the receiver noise factor has essentially no effect on the measurement, and an amplification drift influences only the size of the reading, not the zero point.

A professional Dicke receiver can still detect signals which are 30dB below the noise!

3. A SIMPLE DICKE RECEIVER

Fig.4 shows the author's 70cm band experimental rig: a single 19-element Yagi (!) with app. 15dB gain powers the Dicke switch through 6m of RG214/U. Naturally, it would have been more advantageous to mount the switch and the pre-amplifier directly on the aerial and not in the attic, and thus eliminate the 1.5dB cable damping, but in the development phase it's more important to have an accessible installation location.

The pre-amplifier is a five-stage former channel amplifier for television band IV, which was balanced at 435 MHz. Its first stage had been equipped with a CF300 to bring the noise factor down to values below 1dB. The Philips amplifier used, with high-quality, cleanly dimensioned, silver-plated shell circuits, was most suitable for this application.

It is important here that the pre-amplifier should not oscillate, even in the case of a false adapted load at the moment when the switch is switched, since the high-frequency pulses which otherwise arise are controlled by the receiver downstream. The CF300 drain circuit thus has 100Ω damping and is only loosely coupled to the next circuit. The pre-amplifier has a band width of 5 MHz and an amplification of about 50dB.

The receiver used was the author's spectrum analyser, which is operated in zero span mode. Switching to analyser mode enables interference signals to be located rapidly. The second part of the Dicke switch is connected to the video output of the analyser and powers the display instrument, an analogue millivoltmeter. The switch cycle originates from a square-wave generator, e.g. a function generator.

As can be seen, the receiver uses standard technology for the most part. So it's only the unusual Dicke switch assemblies which require closer examination.

Fig.5 shows the high-frequency switch, which consists of two PIN diodes (type BA379 or BA479), which are controlled alternately by a zero-symmetrical AC voltage of about 10 Vss. The diode which is blocked at any time certainly sees only 0.7 V "blocking voltage" - namely the flow voltage of the conducting diode. But no interference arises through capacitive inductive disturbance.

It is important that the downstream pre-amplifier has a high pass filter at the input, since otherwise harmonics from the switching frequency modulate the operating point in such a way as to cause interference.

The output side part of the Dicke switch is an operational amplifier, which can be wired up to the +1/-1 amplification using a FET (5). The low pass filter after the switch has a limiting frequency of 1 Hz, so that the display function is not too sluggish if the aerial is manually set. The output-side pre-voltage potentiometer can be used to balance the display at zero if there is no signal (Fig.6).

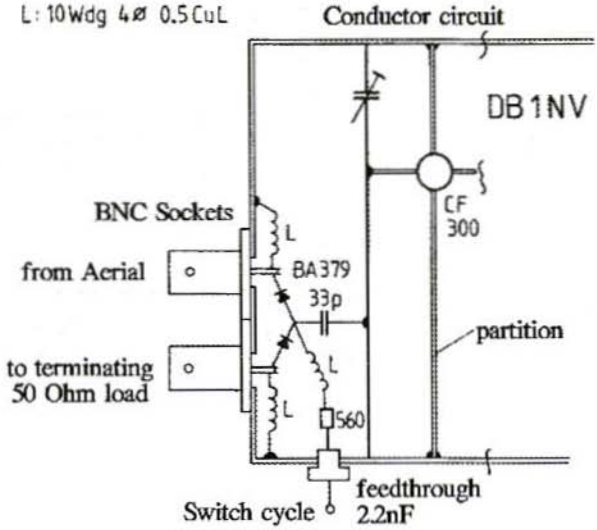

Fig.5: The High-Frequency Switch at the Preamplifier Input

4. RESULTS OF OBSERVATION

In the first experiment, the solar noise was investigated without a Dicke switch. On various days, an increase in noise of between 3 and 4dB was detected. The variations can clearly be traced to varying environmental interference levels. The solar noise was then used to optimise the Dicke switch. The steadiest display was obtained using the maximum intermediate-frequency band width of the analyser (200 kHz), a 500 Hz switch cycle, and a video band width of 1 kHz. The switch cycle turned out to be relatively uncritical. The thermal noise from the warm ground can be satisfactorily detected by the measuring rig if the aerial is swung up from 0°elevation.

Anyone reconstructing these results will straight away find a number of "suspect" signals, all of which are of earthly origin. It is only at night or at the weekend that the author can carry out reasonable observations in a residential area. The daytime interference level during the week is far too high. Many weak little carriers can be detected in the evening, and these are probably interference signals from television sets in the form of cycle harmonics. As these are narrow-band interference sources, you can usually find a free segment of the band where there is no interference.

Atmospheric inversion conditions with overshoots are unsuitable for observations, since at such times the entire 70cm band is occupied by weak signals. In case of doubt, the only thing that helps is to observe a signal for several hours, to see whether the source moves as the Earth rotates (15°an hour).

So far the following objects have been observed (in late Summer and Autumn):

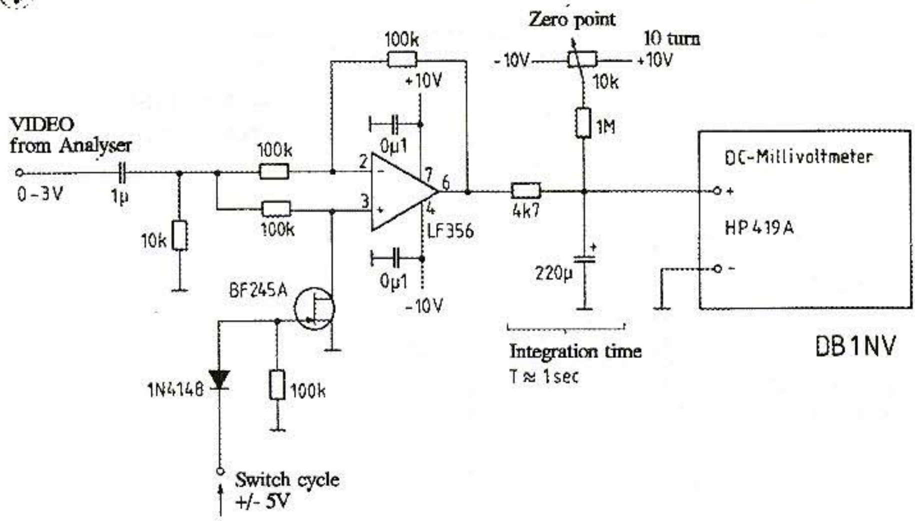

Fig.6: The Output-side Switch

The strongest source, apart from the Sun, is the galactic centre in the constellation of Sagittarius. The maximum reading was obtained in the South at 20° elevation, towards 9.00 p.m. Summer Time, at the end of August. Even at 0° elevation, the signal clearly rose above the thermal Earth noise.

A very weak signal could be found at the same observation time from an Easterly direction at 70° elevation. It was about 14dB below the Earth noise. It was possibly the Cygnus A source in the Cygnus constellation.

At about 10.30 p.m. one evening at the end of August, another very weak source was found below 20° elevation in the Northeast. It could be assigned to the Cassiopeia A source.

A search for the thermal signal from the Moon and for emissions from the Crab Nebula in Stier during January and February was unsuccessful. At the time of the search, the interference level in the 70cm band was definitely high. At 100 MHz, the Crab Nebula is weaker by a factor of 10 than the strongest sources Cassiopeia and Cygnus.

Following these encouraging results, obtained using the simplest of aerial installations, the author is planning to repeat the experiment with Yagis dimensioned for 408 MHz and with a Dicke switch/pre-amplifier mounted directly at the distributing point.

In the 406 - 410 MHz reserved for radio astronomy, a low interference level should be reckoned with. Moreover, a change in the QRL should offer the possibility of using a professional two-axis rotating stand for the experiments.

5. APPENDIX: ESTIMATING THE SENSITIVITY OF THE RECEIVER SYSTEM

According to the manufacturer, the 19-element aerial used has a gain of 15dB over a dipole, which corresponds to an aerial gain of 32. With a dipole absorption area of

$$A_D = 0.13\lambda^2 = 6.37 \cdot 10^{-2}\text{m}$$

we have a Yagi aerial absorption area of:

$$A_y = G \cdot A_D = 32A_D = 2\text{m}^2$$

According to (6), the radio source Cassiopeia A supplies a power flow of S = 18600.10-26 W/m²Hz at 100 MHz. It can be estimated from (4) that the non-thermal radiation output of a radio source falls by 6.7dB per decade when the frequency rises. Consequently, it is 4dB smaller at 430 MHz than at 100 MHz, and amounts to S430 = 7400.10-26 W/m²Hz. For a receiver band width of 200 kHz, the receiver aerial supplies a signal of:

$$P_S = S_{430} \cdot B \cdot A_y$$

$$= 7400 \cdot 10^{-26} \frac{\text{W}}{\text{m}^2 \cdot \text{Hz}} \cdot 2\text{m}^2 \cdot 2 \cdot 10^5 \text{ Hz}$$

$$= 3 \cdot 10^{-17}\text{W} = -135\text{dBm}$$

If the system noise temperature is assumed to be T = 500 K, which is credible on the basis of the cable losses between the pre-amplifier and the aerial, then the noise output of the receiver installation amounts to

$$P_R = kT_0B = 1.38 \cdot 10^{-23}(\text{Ws/K}) \cdot 500\text{K} \cdot 2 \cdot 10^5(1/\text{S})$$

$$= 1.4 \cdot 10^{-15}\text{ W} = -118\text{dBm}$$

Consequently, the radio-astronomical signal is about 17dB below the thermal noise.

The simple Dicke receiver is clearly able to detect signals which are 17dB below the inherent noise of the receiver. Professional receivers attain values above 30dB here.

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Logarithmic Converters and Measurement of their Characteristics

Values with a wide range can be converted onto a logarithmic scale by means of a logarithmic converter, to make them easier to grasp. The accuracy, operative range and actual frequency required determine the choice of the appropriate circuit principle.

1. INTRODUCTION

A significance increase in the use of logarithmic converters in the very recent past has probably been caused by the appearance of suitable integrated circuits. As examples, I could cite: Berberich (2), Jirmann (8), Schneider (9) and Zimmermann (12). The advantages of recording a reading on a logarithmic scale are known: constant relative precision and a wide range of measurement. A measurement range of from 80 to 120dB is desirable in electro-acoustics and high-frequency engineering, for the readings lie over a range with this kind of width. The requirements for accuracy of measurement are usually not very high: ± 1dB is often quite sufficient. But integrated converters can not attain this precision, modest as it is for measuring purposes.

Logarithmic converters can operate on various principles. This article ignores those which operate using control processes or oscillation feedback. The first type is too slow for use in spectrum analysers or wobblers, while (4) provides most information on the second type.

In order to be able to dimension and measure accurate logarithmic converters, a sufficiently precise and sensitive

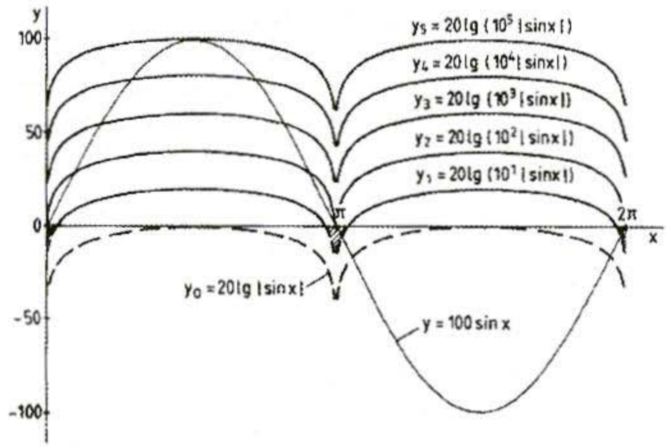


Fig.1: Basic functioning of a Logarithmic Rectifier, using the example of a Sine Curve

signal source is required. We shall explain in detail how such a source can be easily provided by means open to amateurs, and how it is used.

2. MODE OF OPERATION

An analogue or digital gauge, an oscilloscope or strip chart recorder, is connected to the output of a logarithmic converter. The output must therefore supply sufficiently smoothed out DC, and yet be able to follow changes in readings fast enough. So a rectifier and a low-pass filter are required. A single frequency is applied to the converter input if a narrow-band application (intermediate-frequency section) or a single-tone measurement is involved. In other applications, the converter has to handle more than one frequency. There can be noise, or an additional signal in the useful frequency range. A second signal, which people tend to ignore, often stems from an insufficiently shielded oscillator in a receiver, the signal from which can falsify the measurement during wobbling using broad-band technology.

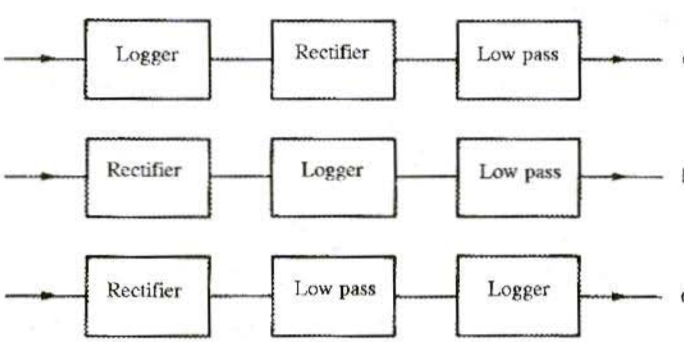


Fig.2: Three types of Series connection for Logger, Rectifier and Low Pass

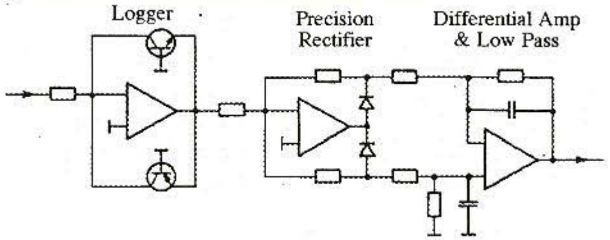


Fig.3: A solution for the Low Frequency range as per Fig.2a, using Analogue Computational Circuits

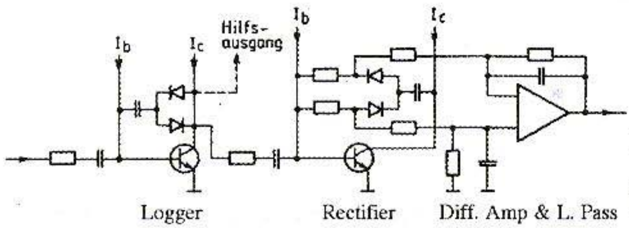


Fig.4: A solution for the High Frequency range

If we begin with the formal assumption that the input signal in the converter is distorted in a logarithmic function, then a mathematical difficulty immediately arises with the negative half-wave. The logarithm of negative values is imaginary and pluri-valent. It's not just a case of reversing the sign. The way out is to position the rectifier in front of the logger. Instead of a sine function, then, an |sin| function is fed into the logger. The output signal then looks like Fig.1. The multipliers used have been selected in such a way that the ordinates can also be interpreted as decibels (20.lg), whilst the input voltage is multiplied by ten, a hundred, etc.. The sine-form input voltage curve has been plotted only once. It goes with the input voltage curve, y2. So such a converter converts each momentary value for the input voltage into the correct momentary value for the output voltage. The output value changes by 20 units if the input value changes ,y the factor 10. It is immaterial in this context whether we are looking at the momentary or the average value after a low pass, because all output curves are congruent.

Complementary circuit engineering makes it possible to form logarithms from negative input values in all cases which are technically feasible. They then come out as negative values. The circuit element which correctly assembles the logarithms from the positive and negative half-waves is, once again, a rectifier.

At high frequencies it becomes more and more difficult to carry out logarithmic distortion and to rectify momentary values with sufficient accuracy.

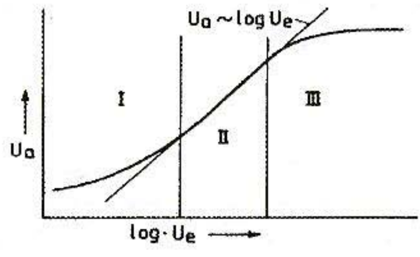
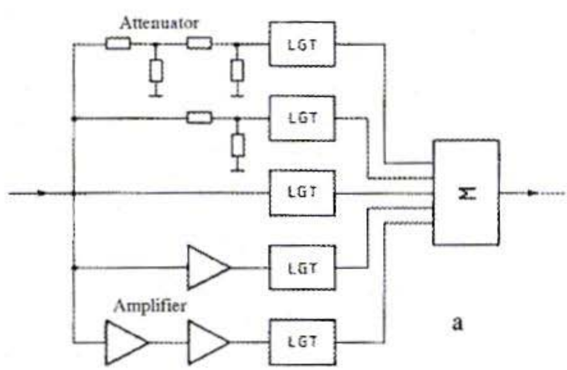


Fig.5: Properties of Circuit in Fig.4

But there are rectifiers with a high frequency range and accurate loggers for low frequencies. Thus we finally obtain the three meaningful combinations of logger, rectifier and low pass sketched in Fig.2. All three layouts are used and have their advantages and disadvantages. The layout in Fig.2a suppresses negative parts of the output function, which are shown as dotted lines in Fig.1. This combination thus has a function-determined threshold and additional errors with low input voltages, which correspond to the shaded area on the y1 curve. The additional error can be avoided, in principle, by point rectification. Circuit b suffers from the fact that precise rectification, even at low frequencies, is possible only for 4 decades, whereas logging can function with 9 decades. Its advantage is that it does not exhibit the errors referred to above. Combination c does not convert momentary values. But the rectifier can be created on an extremely broad-band basis, for example simply using high-frequency diodes. The logger, by contrast, needs to be designed only for the relatively low frequencies which the low pass lets through. The rectifier works in the quadratic or linear range and this means many characteristics which are expected from a logarithmic rectifier are missing, e.g. continuous rectifier selection.



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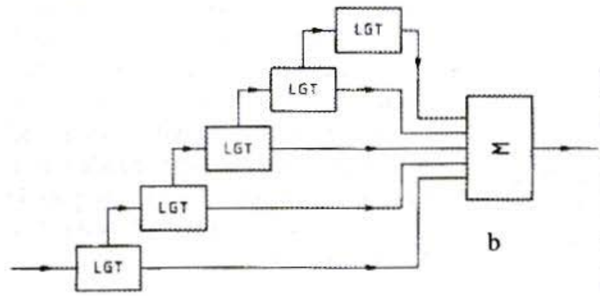

Fig.6:
Successive Conversion:
a) Parallel Circuit
b: Series Circuit

LGT - Logger - Rectifier - Low Pass, as Fig.4

3. SPECIMEN CIRCUITS

All the tricks of analogue computer technology can be successfully applied in the low-frequency range. The circuit laid out with operational amplifiers - Fig.3 - following the layout of Fig.2a will work in the voice frequency range if appropriate amplifiers are selected, together with rapid transistors and diodes, but will fail in the high-frequency range. We can now build a much faster, but also less complete, operational amplifier with a single transistor. A type of transistor for which fT = 5 GHz provides for an open-loop voltage gain of from 50 to 100 at approximately 50 MHz, falling on a linear basis at higher values. The circuit from Fig.4 will thus have the desired relationship between the input and output voltages only over a narrow range, perhaps 10 to 20dB. As long as the input voltage is too low to provide sufficient current for the logarithmic diodes mounted in the counter-coupling

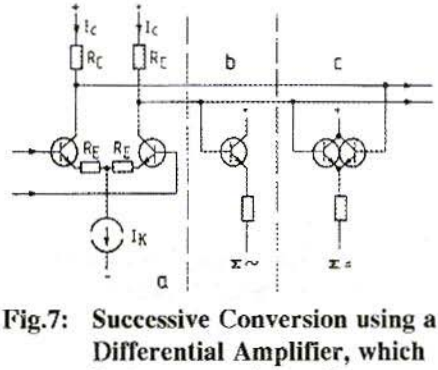

Fig.7: Successive Conversion using a Differential Amplifier, which is also very suitable for Integration

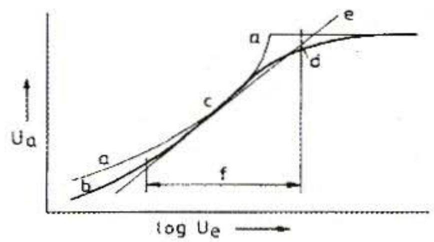

Fig.8: Properties of Circuit in Fig.7
a. Output AC with rigerous limit
b. Output DC in Quadratic Rectification Range
c. Best Approximation Range
d. Hyperbolic Tangent Transistion into Limit
e. Rated curve
f. Tolerable Error Range

to the first transistor, the output value will rise on a linear basis. This expresses itself in the floating point representation of Fig.5 as part of an exponential function (I). If logging is used, a curved section is generated (II) with the desired form. Finally the amplifier is saturated and the output value becomes constant (III).

In order to broaden the logarithmic range, several stages can be connected together to a successive converter, as in Fig.6. Parallel operation (Fig.6a) requires more components - additional dampeners and amplifiers. They can be operated over a wider frequency range than the Fig.4 circuit in every respect. The frequency range of the entire layout corresponds to that of the individual stage. The output values for all the grades are collected together in a summation circuit. A joint low pass in the adder can also be used, instead of the individual low-passes.

In series operation, the amplification available in each stage is used to provide amplified voltage for the next stage. The connection is at the "auxiliary output" point in Fig.4. No additional components are now necessary. But the frequency errors of all stages are added together, which leads, above all, to low input values. This can be clearly recognised in a converter by Braubach which works on this principle (3). But if it is a case of a narrow-band application, as with Berberich (1), then a frequency cycle error has no significance. The converter is optimised for the operating frequency. It is also important that conversion does not occur instantaneously in such a converter. So here too you can't expect all the advantages of logarithmic rectification.

There are more practical circuits for series operation, which work with differential amplifiers. The principle can be seen in Fig.7, and the calculations can be found in Tietze and Schenk's work (10). The circuit is suitable for integration and so it (or something similar) is used in all the more recent intermediate-frequency integrated circuits. The equipment-building industry has customised circuits based on this principle, to which radio amateurs have no access. They can only build rigs from discrete components, as per Jirmann (7), or use first-generation IC's, which contain precisely the transistors required; that gives better compatibility for the characteristics and causes fewer temperature problems. Such a solution is several degrees better than using an intermediate-frequency IC if improved accuracy is the goal.

An emitter follower (b) can simply be connected to the differential amplifier (a) in Fig.7, in order to de-couple the AC, or else a Townsend current rectifier (c), made of two emitter followers, can be connected up (c). The total outputs of all stages are fed into

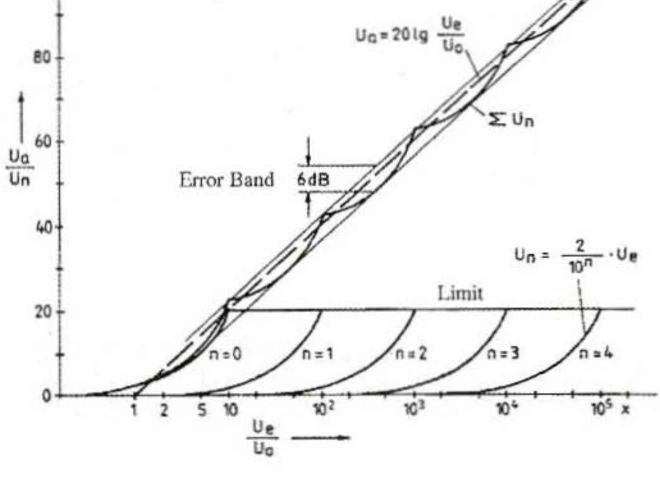

Fig.9: Construction of Conversion Characteristic for Series Connection of stages as Fig.7

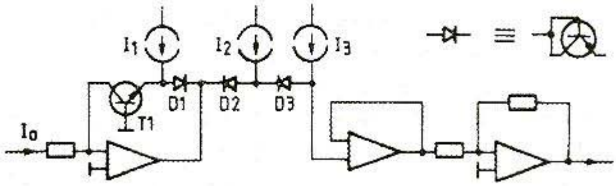

Fig.10: Logger after the Diode Rectifier for a layout as per Fig.2c

appropriate summation circuits. The total of all AC values is the momentary logging of the input voltage. The total of all DC increases (i.e. if the Townsend currents are subtracted) corresponds to the mean arithmetical value for the rectified AC currents.

Whilst for the first total it is a requirement that the phase displacement between the various stages is insignificantly small, this requirement does not apply to the DC total. The only requirement here is that the amplitude displacement in the useful frequency range is insignificant. The frequency range is thus not determined by a rigorous phase requirement but by a less rigorous amplitude requirement.

Several stages as per Fig.7 form a successive converter, with many properties of the circuit contributing to its conversion characteristics. Initially, the stage amplification can be selected which is given by the ratio $R_C : (R_E + 2 \cdot UT/I_k)$ (U_T, temperature voltage = 26 mV). The characteristic gradient thus obtained is shown as a in Fig.8 and corresponds to an e-function in the floating point representation. If the level control reaches a height at which the IC attains the combined constant emitter current, I_k, the output voltage can increase no further. This is shown by the fact that the characteristic bends into a horizontal line. The rectifier has a quadratic and a linear range, just like diode rectifiers. The quadratic range causes the a curve to drop in the left-hand area as soon as the b curve appears. This creates a better range of best approximation, which is shown as c.

Finally, the transition at the limit is right-angled only if R_E is quite large. If $R_E = 0$, the transition is a hyperbolic tangent (tan h) function. All practical cases lie between the extremes and contribute to a rounding up, d, so that finally a rather wide range is created with a sufficiently low error, f.

It is up to the skill of the circuit developer how he or she combines the various options into a conversion characteristic which is as straight as possible. A five-stage converter for 80dB can be obtained as per Jirmann (7) with an error of ± 2dB. Constructing the conversion characteristic as per

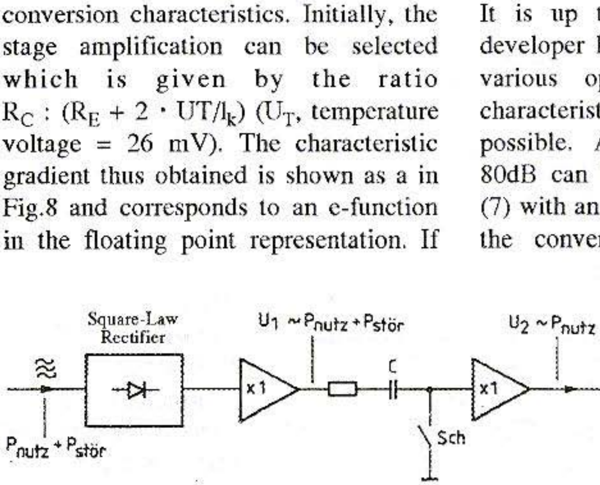

Fig.11: Elimination of the display of Interference after a Quadratic Rectifier

Fig.9, without taking in the rounding up effects, gives an error of ± 3dB at a stage gain of 20dB.

Halving the stage gain will reduce the error to ¼. It is thus not that much of a problem to develop successive converters with errors of considerably less than ± 1dB using this principle.

Converters of this type will have a frequency range of a few MHz in a discrete format. Nowadays integrated circuits are manufactured with faster and faster processes. Thus the relatively new IC NE604A, it is said, can be used with approximately constant properties from the low-frequency range up to 21.4 MHz (13). Similar values can be obtained using transistor arrays if the transistors they contain guarantee $f_T > 500$ MHz.

The layout in Fig.2c is particularly suitable for expanding the frequency range upwards, because it is still only the rectifier which needs to be dimensioned for the high frequencies. Even with reasonably priced diodes, 100 MHz can easily be obtained, whilst special diodes can even operate at up to 10 GHz. The characteristic of such diode rectifiers has a bend in it, with a quadratic range below $2.U_T$ and a linear range above it. It is not generally known that such a characteristic, the reasons for which are explained in (5), can be precisely logged. The circuit for this is shown in Fig.10 and should be briefly explained.

As long as the current supplied by the rectifier, I_0, is smaller than I_1, D1 acts as a Townsend current diode with a constant voltage drop. The logging can be carried out through a known process

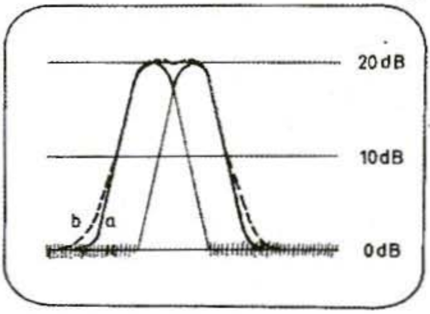

Fig.12: Spectrum Analyser display for various types of Rectifier:
a. Logarithmic
b. Linear or Square-Law Rectifiers

in T1. If I_0 is larger than I_1, then D1 acts as an additional logger. The conversion gradient becomes twice as steep. I1 should therefore be selected to be as large as the current value supplied by the rectifier during the transition from the quadratic to the linear range. Together with I_2 and I_3, diodes D2 and D3 provide for temperature compensation over the entire conversion range and allow the zero point of the output voltage to be established for any rectifier current, I_0, desired. For T1, and for D1 to D3, it is advantageous to select a transistor array in which three transistors are wired up as transdiodes (top right in Fig.3). The connection between basis and collector eliminates the influence of the extrinsic base resistance within the transistors, and we have more of an ideal diode. You can find another solution to the same problem in Vieland (11).

4. INFLUENCE OF TYPE OF RECTIFIER

A logarithmic rectifier has infinite rectifier selection, i.e. it ignores all smaller signals. So it is initially irrelevant whether it is first rectified and subsequently logged or vice versa. It is necessary only for the momentary value to be correctly converted at all times. Nor does it have any importance whether the rectifier evaluates the peak value or the area under the curve following a logger, as long as you just disregard the additional inaccuracies of junction rectification for low input signals. However, the point rectifier must be capable of following the differential frequency between the useful signal and an interference signal, which is certainly easier to achieve for narrow-band applications than for broad-band converters.

A quadratic rectifier supplies an output value which corresponds to the total of all input power values. There is no rectifier selection. But this behaviour can also be put to profitable use. The interference oscillator or the noise during the wobbling in receivers can create a raised (i.e. false) base line. This can be remedied by a circuit as per Fig.11. During the beam feedback, the wanted signal generator is switched off and the switch Sch is closed. The capacitor, C, is then charged with the voltage corresponding to the interference power level. If Sch is now opened and the wanted signal is switched on again, then the output voltage, U_2, no longer contains the interference signal fraction. The process functions with interference voltages of up to $2 \cdot U_T \sqrt{2} = 40$ mV. The second amplifier must have very low offset voltage and bias current values.

With regard to its properties, the linear rectifier lies between logarithmic and quadratic equipment. In a layout such as Fig.2c, you will scarcely notice any difference, because the logging in the linear range has a gradient twice as steep. An interference signal of the same value as the wanted signal doubles the output value in the quadratic range. In the linear range, it is initially multiplied only by $\sqrt{2}$ (3dB), and the doubling of the gradient makes the same change out of this as in the quadratic range.

It is much easier to look at the variations between rectifiers on the screen of a spectrum analyser (Fig.12) than to wade through a long description. It is known that the ideal analysis filter, based on the best resolution and the fastest frequency changes, has a round cone and a form factor of 60: 3dB of 4.4. Thus two spectrum lines are ideally represented when they are like the thin lines in Fig.12.

The total picture obtained from a logarithmic rectifier is shown by the thick lines. In the area of the cone, it follows the strongest signal at any time. A slight rounding up occurs in the vicinity of the picture noise, due to the stochastic nature of the noise voltage. Linear and quadratic rectifiers generate the dotted line curve. The analyser has clearly lost some resolution! In the vicinity of the noise, the level indicated is far too high, which may possibly not be recognised if the video filter for the cut-off frequency has been selected with too low a value.

5. MEASUREMENT OF CONVERTER PROPERTIES

The usual method of testing a logarithmic converter is to connect a signal generator in series and alter its output voltage in defined stages. It is worth having a look at the guaranteed data of the generator first. Using very precise equipment, you may be able to use precise stages of, for example, 0.1dB. The absolute tolerance can be set within ± 1dB. I've still never seen a specification providing for the monotony in stages we expect from every 10-Mark D/A converter! Sometimes, when precise stages are being used for through switching, another coarse attenuator is wired up, and the + 1dB tolerance initially present can then become - 1dB. M.a.W., the monotony is 20 LSB! Such a generator is not suitable for measuring a logarithmic converter within which there are rated errors of ± 1dB.

Here it is certainly more appropriate to modulate the signal generator using AM, which finally also co·rresponds to changing the amplitude by a small amount. If we now let the output voltage hunt through the area of interest (for which no more accurate calibration divider is required - a Preh 110 attenuator can do it too), then it is easy to find the point of deviation from the ideal gradient, in the shape of a change in the steepness of the conversion characteristic. On top of that, constructing the entire gradient as the integration of the steepness gradient is difficult.

So if the gauging industry can be of no further use to us, we have to fall back on physical principles. There is a law of nature which can provide us with all amplitudes in precise stages over a very wide dynamic range in fractions of seconds: decaying oscillation. Czech (6) used decaying oscillation to measure the quality of oscillation circuits. This led me to the idea of using the same process as a signal source for testing logarithmic converters.

An oscillation circuit made up of the components L, C and R will oscillate as long as all these components are constant, in such a way that successive amplitudes are always in the same ratio.

$$\theta = \ln \frac{A_n}{A_n + 1} = \frac{\pi}{Q} \qquad (1)$$

applies for the logarithmic decrement, θ.. For the natural logarithm, we can also write:

$$\ln \frac{A_n}{A_n + 1} = 10 \cdot \lg \frac{A_n}{A_n + 1} \qquad (2)$$

As 20 · lgAn/An + 1 can also be referred to as Δ A/dB, we get

$$\Delta\ A/dB = \frac{\pi \cdot 20}{\ln 10 \cdot Q} = \frac{27.3}{Q} \qquad (3)$$

For a circuit quality of 50/100/200/500, successive amplitudes have differences of 0.546/0.273/0.1365/0.0546dB. Rectification, which lets the peak negative value appear between two peak positive values, halves the stage height. With thoroughly achievable circuit Q values of between 100 and 200, we get a grading which leaves nothing to be desired.

Attenuation is complete when the amplitude has fallen below the noise voltage of the oscillation circuit. With a sufficiently high input voltage, U_{an}, a decay range of 100dB can easily be obtained. The noise voltage, U_r, is

$$U_r = \sqrt{(4 \cdot k \cdot T \cdot \Delta f_r \cdot R_{res})} \qquad (4)$$

where:

k = Boltzmann constant

$1 \cdot 38 \cdot 10^{23}$W/K

T = Absolute temperature.

With the noise band width Δf_r,

$$\Delta fr = \Delta f_{-3dB} \cdot \frac{\pi}{2 \cdot \sin p /2}$$

$$= 1.57 \cdot \Delta f_{-3dB} \qquad (5)$$

Three different oscillation circuits are used for the measurements described below. The first, with a relatively low frequency, came about because a suitable coil was in the DIY box. The other two correspond to common intermediate frequencies. Table 1 lists the relevant oscillation circuit data. Apart from the values for L and C, the values calculated using the above formulae for the logarithmic decrement, θ, the amplitude stage, ΔA, the 3dB and noise band widths, Δf_{-3dB} and Δf_r, the resonance resistance, R_{res}, the noise voltage, U_r, the initial voltage, U_{an}, for 100dB oscillations, the number of oscillations above 100dB, n, and the time for the attenuation process can be obtained.

The action of the oscillation circuit is triggered by a pulse. Fig.13 shows a suitable circuit. The capacitor, C_1, is loaded with an adjustable voltage. This is done slowly through a high-level resistance, so that no significant energy excitation is linked into the oscillation circuit. If the switching transistor is now energised, then the energy stored in C_1 is transferred to the oscillation circuit. Suitable values for C_1 can also be obtained by means of Table 1.

The switching transistor remains live during the decaying period. Its low "On" resistance prevents additional losses in the oscillation circuit. Since C_1 is now parallel to C, the oscillation frequency becomes somewhat lower. This process can be repeated periodically if the circuit has enough time to decay and if C_1 is again fully loaded.

To avoid any stress on the oscillation circuit, the voltage is derived through a complementary source follower, which of course contributes some noise of its own. Should the resonance resistance not be very high and the load not particularly small, you can even decouple directly from the coil, using 1 or 2 coupling windings; alternative output in Fig.13.

This simple de-coupling can be used without any additional equipment in the measurement of an NE604A at 450 kHz or 10 MHz.

Table 1	Resonant Frequency		
	5.4 kHz	450 kHz	10 MHz
Coil L	29mH RM 10 Shell Core 30nF Styroflex	28 Wdg 0.8 CuL Ring T94-Mix 1 Amidon	8 Wdg 1 Cu Silvered Ring T-94 Mix 1 Amidon
Capacitor C	300	10nF Styroflex	5 x 100pF Ceramic 1
Q	0.0105	175	150
log Decrement θ	0.091	0.018	0.021
Δ A/dB	18/28.3 Hz	0.156	0.182
$\Delta\ f_{-3dB}/\Delta\ f_r$	300kΩ	2.57/4.04 kHz	66.7/1.5 kHz
R_{res}	0.37μ V	6.2kΩ	4.8kΩ
U_r	37mV	0.63μV	2.85μV
U_{an} for 100dB	1100	63 mV	285 mV
n for 100dB	230ms	640	550
Time for 100 dB	1nF Styroflex	1.4ms	55μs
Coupling C_1		1 nf Styroflex	47 pF Ceramic 1

For an initial test of the process, I took a low-frequency voltmeter which has a successive converter for the linear dB scale, with stages similar to Fig.7. Since it has a high input resistance of 1 MΩ, I didn't even need a source follower. A brief square pulse from a function generator was used to trigger the action of the 5.4 kHz oscillation circuit. It can be seen in the top beam track in Fig.14.

The best energy excitation is provided by a pulse length equal to half the oscillation period (93 μs.). So in this special case no circuit as per Fig.13 is needed. But it is always to be recommended when the frequencies are high and when the load can not be estimated with sufficient precision. The lower beam track in Fig.14 shows the first ten oscillations. The grading and the circuit

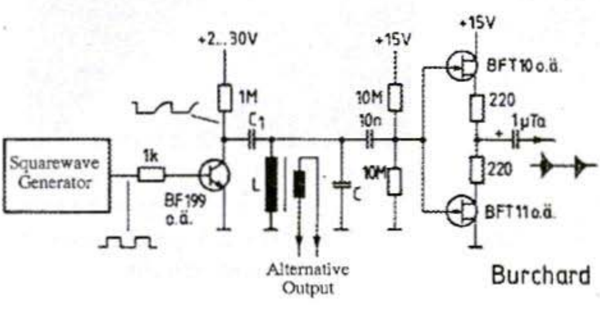

Fig.13: Circuit for Generating Decaying Oscillations

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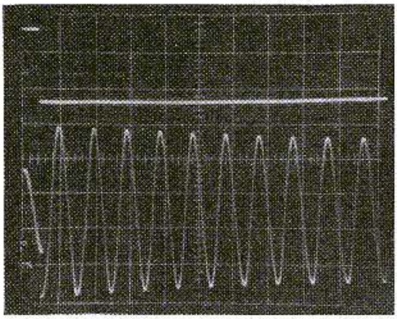

Fig.14: The First Ten Decaying Oscillations
Y1: 2V & Y2: 100mV/div
X: 20ms/div

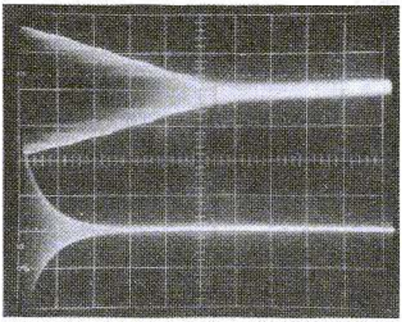

Fig.15: Testing a Five-Stage Converter similar to Fig.7
Y1: 200mV & Y2: 100mV/div
X: 20ms/div

Q values can be determined from the reduction in amplitude using equation (1). Fig.15 shows the entire decaying process, with the voltage at the AC total point of the converter above and the input voltage below. Considerable improvements can still be made to the resolution.

For Fig.16, the zero line has been displaced to the bottom edge of the picture and the Y amplification has been quadrupled. Now we can recognise a lot of details. The converter has 5 stages and works over a range of 50dB. There are thus 5 clear levels to distinguish, at each of which one stage reaches its limit.

The limiting level for the earliest stage in the converter lies somewhat above the initial voltage. The conversion characteristic forms a wave curve, which always indicates a wave peak at the

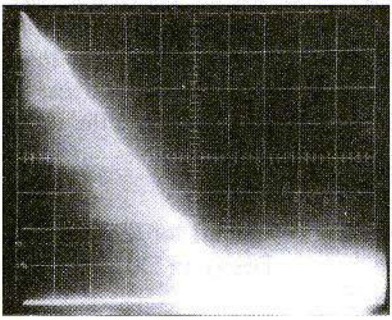

Fig.16: Better Resolution of Log Curve from Fig.15
Y: 50mV (0 at bottom edge)
X: 20ms/div

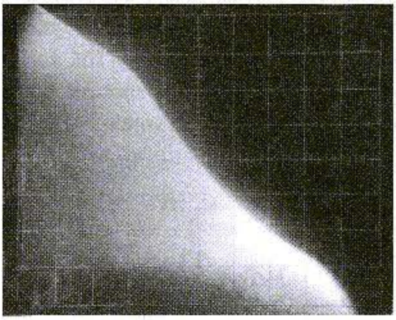

Fig.17: Still Higher resolution using Timebase Sweep and further increased Y amplifications; both axes 2dB/div

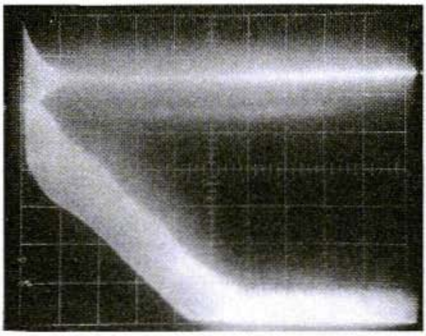

Fig.18: Measurement of an NE604A at 5.4 kHz Y1: 200mV & Y2: 100mV/div X: app. 35ms/div (20dB/div)

point where a stage comes to an end, with a wave trough in between peaks. This correlates with the curve plotted in Fig.9.

To measure the curve exactly, the time scale has to be correlated with the flat dB stages. To this end, we start from Fig.14 or 15 and alter the time base in such a way that the amplitude of the decaying oscillation falls by 10 or even 20dB over the full screen, corresponding to 31.6% or 10%. We have then set 1 or 2dB per division and can now select 5, 10 or 20dB/division by switching the coarse staging of the time base. Fig.17 shows a high resolution, in which the Y amplification has been altered in such a way that the curve drops below 45° in the centre. Thus the errors of this converter can be measured at ± 0.6dB. If you can use a delayed time base, you can examine the entire curve section by section.

The NE604A intermediate-frequency integrated circuit contains any logarithmic converter, and can stand as an example of many similar products here. The application note (13) gives a suitable application circuit. If we remove the capacitor earthed through pin 12, this IC operates from low frequencies to over 20 MHz. It has been observed that the IC has a tendency to oscillate if the impedance at the log output, pin-5, is greater than 100Ω. It should be assumed beforehand here that this output is in the same phase with the input voltage during one half-wave, but in the reciprocal phase in the other half-wave. A positive feedback can thus come into being very easily through small stray capacitances in an experimental rig. So a blocking capacitor providing at least 100pF is required at pin 5. The output is a current output, i.e. an open collector. The output voltage is proportional to the load resistance. If you wish to observe momentary voltages, then this is possible only at rather low frequencies or low load resistance, because of the capacitor.

A simple block wiring diagram can demonstrate the internal structure of the NE604A. It shows five amplifier stages with rectifiers connected up, which are all working on an addition circuit. We do not know in advance whether we are dealing with a momentary value converter, but we can determine this using the decaying oscillation. This converter should always give the same conversion curve in a specified frequency range, due to the formation of the DC sum.

If we operate the NE604A at 5.4 kHz, we get Fig.18. The load resistance selected was 1kΩ, so that the top limiting frequency is 1 MHz. That is fast enough for all details.

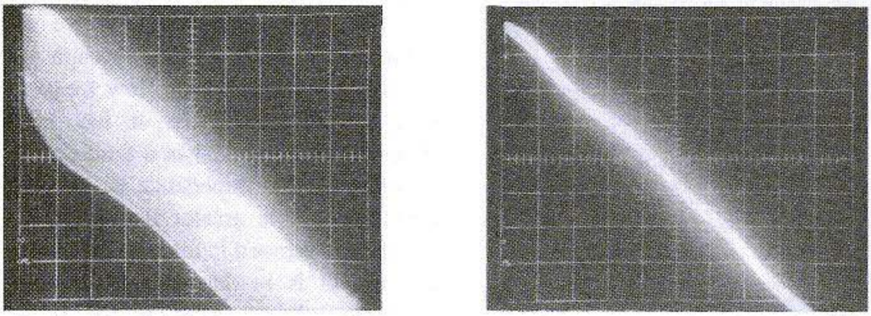

Fig.19: Determination of Conversion Error, both axes 10dB/div
a. with small Load Capacitance (100pF)
b. with large Load Capacitance (10nF)

Several details of this picture stand out immediately. Three wave crests are clearly visible, while a fourth can be conjectured to be at about the height of the noise. There is no fifth one forming. The conjecture is obvious that there are only four gain stages involved in the conversion. However, the dynamic range clearly exceeds 80dB. The stage amplification can be estimated at 25 to 30dB from the wave crest interval. The output voltage curve has a flat lower limit. In momentary conversion, the output voltage should always fall to the noise level at a zero crossing, as is indeed the case in Fig.16. Why things are different here I must leave open.

Finally, another band-form structure is recognisable in the logged curve. Fig.19a shows it even more clearly. I have no explanation for this either.

The top limit corresponds to the output voltage when the peak value is meas-

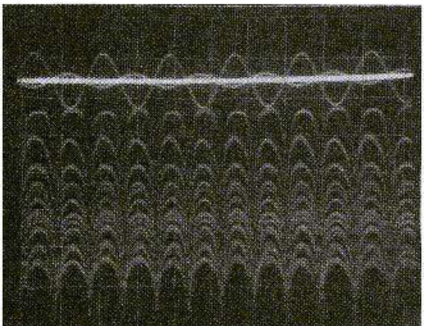

Fig.20: Representation of Logging Precision
Y1: 200mV & Y2: 100mV/div
X: 100ms/div (timebase sweep)

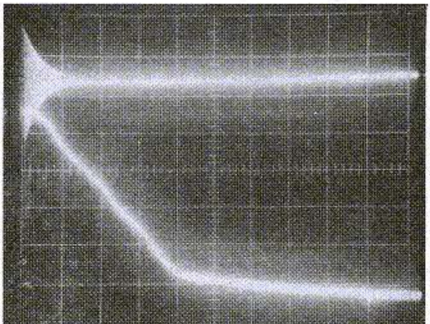

Fig.21: Measurement of an NE604A at 450 kHz
Y1: 200mV & Y2: 10mV/div
X: 20dB/div

ured. The average value is obtained if the load capacitance is made big enough. For Fig.19b it was selected at 10nF, which certainly gives rise to residual ripple, but allows the output to remain fast enough for the rapid rise in voltage when the action of the oscillation circuit is triggered. The peak value and the average value do not give congruent curves. Particularly in the region of high input voltage, the average value curve is flatter. The biggest deviation from a straight line is at -20dB, and a marked bend at about -40dB also stands out. The gradient is markedly steeper above than below. The total conversion error obtained from Fig.19b amounts to exactly ± 2dB. This is a very good reading for the small number of stages and the wide dynamic range.

And finally, Fig.20 was produced in order to examine the internal functioning of the NE604A. It was derived from Fig.18 through a delayed time-base sweep, which was triggered using the Y2 curve. When the trigger level is hunted through, a different curve is produced for the momentary voltage every time, which can now be compared with Fig.1. All these curves should actually be similar, which is in no way the case here. For it is not only the forms of the half-waves which are different. Thus the IC in no way forms the correct momentary value. Not all the advantages of logarithmic rectification can be expected in practical use.

Now the behaviour at higher operating frequencies is naturally also of interest. For Fig.21, the NE604A was connected up to the 450 kHz oscillation circuit. With a load of 1kΩ/100pF, we already obtain the average value, and we also see that 3 wave crests have been formed. The only other noteworthy feature is the "tail" of the curve, the slow decaying below -80dB. This can not be seen at 5.4 kHz or even at 10 MHz, and corresponds to a time constant of 1 to 2ms.. According to a personal report from N.Rohde (*), he has observed a similar effect on a TDA1576. I wouldn't like to say what the reason for the effect might be. It is possible that operating point displacement or local thermal effects on the crystal play a part. Because of the low time constant, it does not occur if the curve is passed through in a substantially shorter or longer time. Nor is it to be seen if no more than 80dB of the logarithmic range is used.

Finally, a curve which is very similar to Fig.21 is also obtained at 10 MHz, but without the "tail" - i.e. the curve falls steadily away to about 6mV (app. -90dB) and runs horizontally from then onwards. To produce this, the load resistance has to be reduced to 50Ω, with the output voltage still only 2.5mV.

6. CONCLUSION

The decaying oscillation process can always be made use of if the output of the logarithmic converter is sufficiently rapid to follow the sudden voltage rise when the action of the oscillation circuit is triggered. The requirements for decaying, on the other hand, are comparatively easy to meet. A point in the circuit can often be found where it is guaranteed - for example, in front of the low pass filter. Or the possibility exists of raising the speed by means of a few other components - as with the NE604A here. Converters following the principles of Fig.2c can not be measured using this procedure. Nor is this necessary if logging as per Fig.10 is applied. The characteristic is not waveform and the single area which calls for more detailed examination is the transitional range between quadratic and linear operation.

Two examples were used to demonstrate the type of curves and results which could be expected. Using any logarithmic converter IC, properties were demonstrated which were not to be found in the data sheet and the application note. Those who wish to develop such converters themselves have a precise and sensitive signal source available in decaying oscillation. Optimising measures can be seen on the screen immediately.

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