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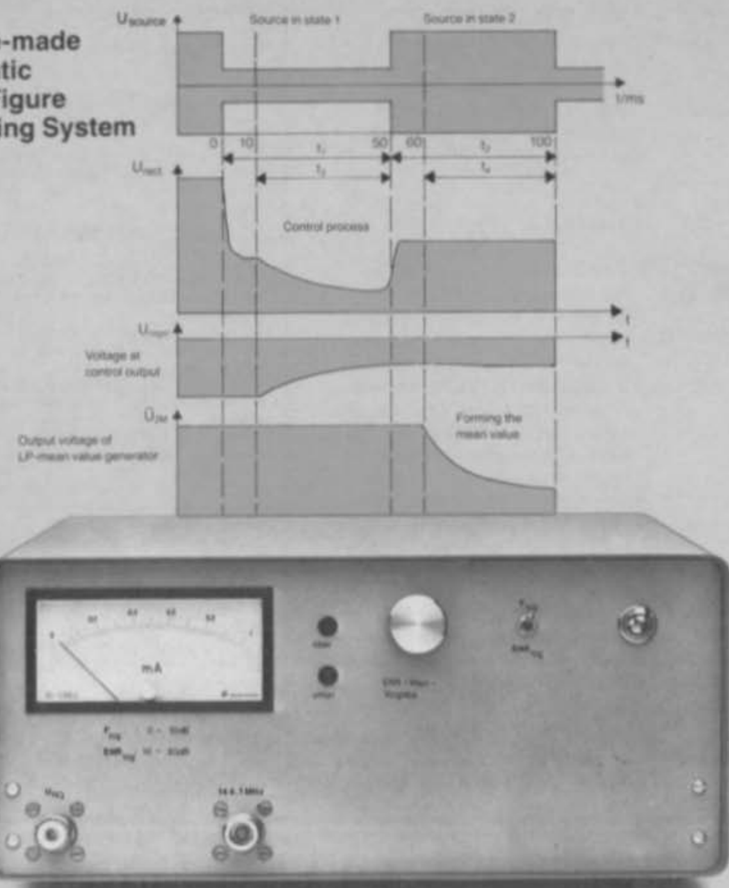
A Publication
for the Radio-Amateur
Especially Covering VHF,
UHF and Microwaves

VHF communications

Volume No. 15 · Spring · 1/1983 · DM 6,50

A Home-made Automatic Noise-Figure Measuring System



VHF communications

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Contents

In the Focus

It is with special pleasure and some pride that I publish a Home-Made Noise-Figure Measuring System. As a UHF-minded radio amateur I struggled to obtain "the very best" noise figure for my equipment and optimum measuring techniques for over two decades now, always wishing I had an instrument like this.

Martin Dohlus (26) is the son of the company founder Hans Dohlus, DJ3QC. Martin is an engineer, doing post-graduate studies at present. He worked in our laboratory in his vacations in the last years. I was able to pass on some of my experience to him and to also discuss measuring problems with him. This eventually led to the development and publication of this noise-figure system.

In our material price list at the end of this edition, you will find an offer of a kit for the Noise-Figure Measuring System (although the concluding part of the description is still to come). Of course, the price may not be in reach of a number of amateurs but, how about considering the construction of such an instrument as a club project?

When the system is completed, and you are about to start measuring noise figures, don't forget to refer to the article "Some Pitfalls in Noise Figure Measurement" (VHF COMMUNICATIONS 1/1982), and check-off the various points in a similar way to a pilot consulting his check-list before take-off.

With kind 73s

your's

Robert E. Lentz

DL3WR

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Martin Dohlus

A Home-Made Automatic Noise-Figure Measuring System

This two-part article describes an automatic noise-figure measuring system that allows rapid alignment for minimum noise figure. If the noise source is calibrated, it is also possible for absolute noise-figure measurements to be made. The frequency range of the measuring system is determined by the noise source. The described measuring system possesses a 144 MHz input, but it is easily possible for it to be changed to other frequency ranges such as 29 MHz, 10.7 MHz or even AF. The noise figure is read off directly in dB on the meter, as can be seen in the photograph of the author's prototype in Figure 1.

In contrast to most noise-figure measurements such as the 3 dB method of Y-factor method, that only allow a time-consuming alignment process, the measuring system described here allows automatic measurements to be made in a rapid sequence, which means that the results of the alignment can be seen immediately. In practice, such a measuring system is very useful, especially in conjunction with passive mixers; however, also in conjunction with converters and preamplifiers using expensive input transistors, one will soon see that the costs of such devices are only worthwhile if they can be aligned to optimum on a noise-figure measuring system. In order not to bore our practical readers, we are going to keep the theory of noise-figure measurements to a minimum.

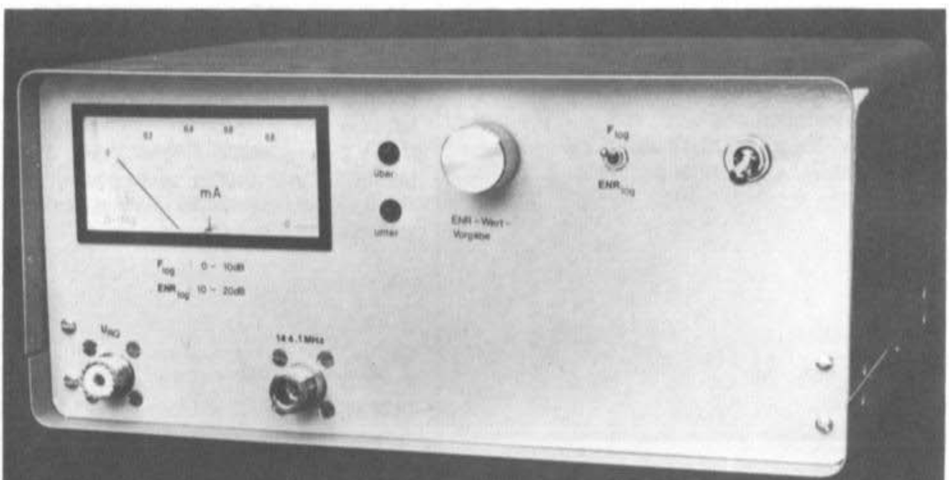

Fig. 1: Photograph of the author's prototype of the noise-figure measuring system

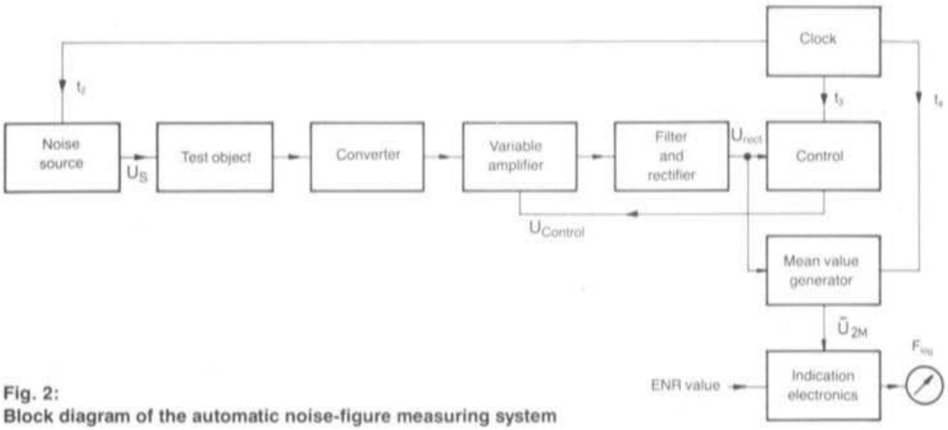

Fig. 2:
Block diagram of the automatic noise-figure measuring system

1. MEASURING TECHNOLOGY

The noise figure is a criterion for the sensitivity of a system. However, it does not exist in the same manner as voltage, current, or power. This means that it can only be measured indirectly. The measuring technology has not changed considerably subsequent to the IEEE-standardization in 1957.

During the measurement, the test object is excited by two known noise levels one after another, and the output power is determined. These two levels then allow the noise figure to be calculated (1).

The term „Excessive Noise Ratio" – ENR – specifies the noise source with which the system is to be driven.

$$ENR_{log} = 10 \lg \left(\frac{P_2}{P_1} - 1\right)$$

P_1: Available output power from the source in state 1 (passive)

P_2: Available output power from the source in state 2 (active)

Both power levels are mean noise powers and are referred to the bandwidth B.

If P_1 corresponds to the power that a resistor provides at ambient temperature (1 kT_0), the noise figure can be calculated according to the following equation:

$$NF_{log} = ENR_{log} - 10 \lg \left(\frac{P_{2M}}{P_{1M}} - 1\right)$$

P_{1M}: Output power of the test object when driven with P_1

P_{2M}: Output power of the test object when driven with P_2

The measuring technology that can be derived from this equation is used in virtually all automatic noise-figure measuring systems. The best systems achieve accuracies of ± 0.2 dB using this system.

1.1. SPECIAL FEATURES OF THE DESCRIBED METHOD

The block diagram of the system is shown in **Figure 2; Figure 3** shows the time-plan of the measurement. The „clock" switches the noise source at a speed of 50 ms. The source is passive during the period t_1, and is active during t_2. The output noise powers of the test object are amplified and converted to AF-level. It is now possible for the noise levels to be determined using the mean value of the noise voltages.

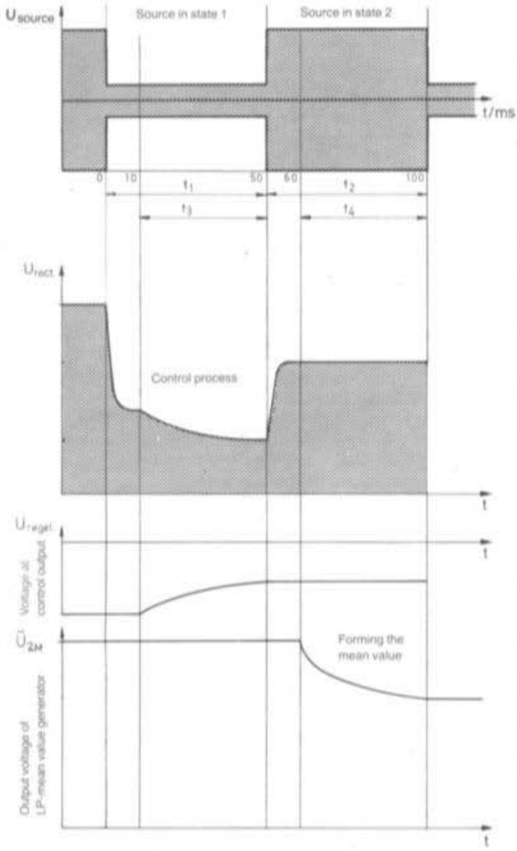

Fig. 3:
Time-plan of a measurement

$$\overline{U}_{1M} = \sqrt{const \times P_{1M}}$$

$$\overline{U}_{2M} = \sqrt{const \times P_{2M}}$$

$$NF_{log} = ENR_{log} - 10\ lg \left[\left(\frac{\overline{U}_{2M}}{\overline{U}_{1M}} \right)^2 - 1 \right]$$

$\overline{U}_{1M}$: Mean value of the AF-noise voltage when the source is in state 1; (passive)

$\overline{U}_{2M}$: Mean value of the AF-noise voltage when the source is in state 2 (active)

In order to ensure that the transcient behaviour on switching the noise source on and off does not have an adverse effect on the measuring results, the „mean values" are only formed during the periods t_3 and t_4. The formation of the mean value is achieved using a lowpass filter and an I-control.

The proportionality factor „const" is determined via the variable amplifier so that U_{1M} has a defined value. This means that a fixed relationship exists between U_{2M} and NF_{log} (equation 5) with the exception of the term ENR_{log}.

This relationship is taken into consideration in the evaluation electronics so that the noise-figure can be directly indicated.

It is difficult to give the accuracy of the described system as a single number. The accuracy of the noise source has a considerable influence. In the case of the following typical values, the maximum error caused by stages subsequent to the test object is less than 0.4 dB:

ENR_{log} = 17.0 dB
NF_{log} = 2.0 dB
V = 20.0 dB
V = Gain of the test object

A detailed discussion of possible errors, and measures which can be taken to increase the measuring accuracy are to be discussed in an appendix.

2. BRIEF DESCRIPTION OF THE CONSTRUCTION

As can be seen in **Figure 4**, the measuring system can be split into six modules:
Noise source
Receive converter
Demodulator and variable amplifier (RMG 03)
Oscillators
Control electronics (RMG 02)
Read-out electronic and reference-voltage generator (RMG 01)

Figures 5 and 6 show the prototype from above and below. The individual modules are to be described individually in the following sections.

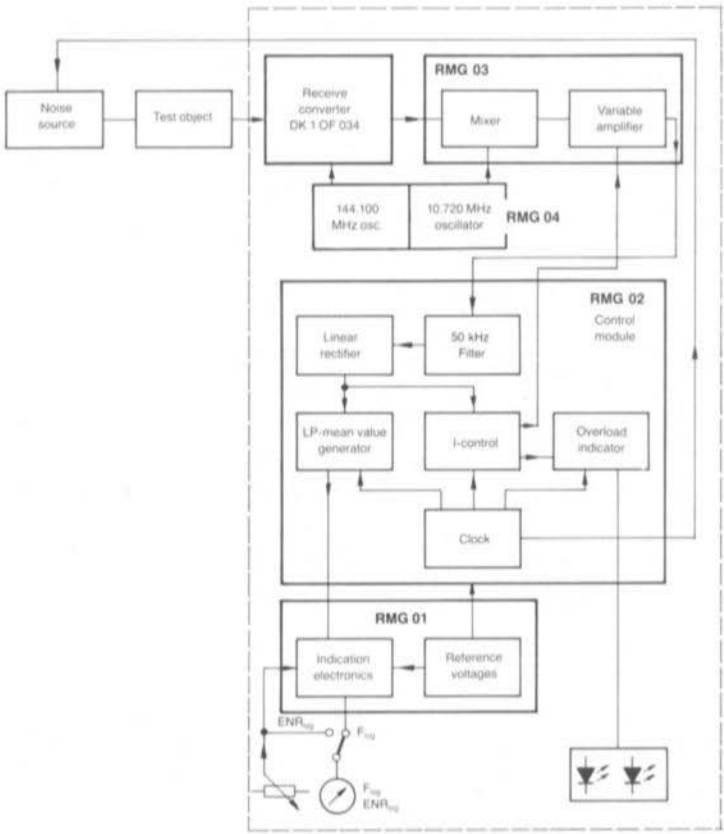

Fig. 4: Modules of the noise-figure measuring system

3. NOISE SOURCE

The noise source can be built up in a similar manner to that described in (2). It is only necessary for it to be extended so that the switching between P_1 and P_2 can be made electronically **(Figure 7).**

It is advisable for the noise source to be installed in a separate case so that it can be directly connected to the test object. This ensures that measuring errors due to attenuation, reflection, and transformation in the additional connectors and cables will not falsify the measuring results.

The knowledge of the ENR-value is very important for absolute noise-figure measurements. It can be determined by comparing it with calibrated noise sources; for instance at a university, technical college or even other amateurs with calibrated sources.

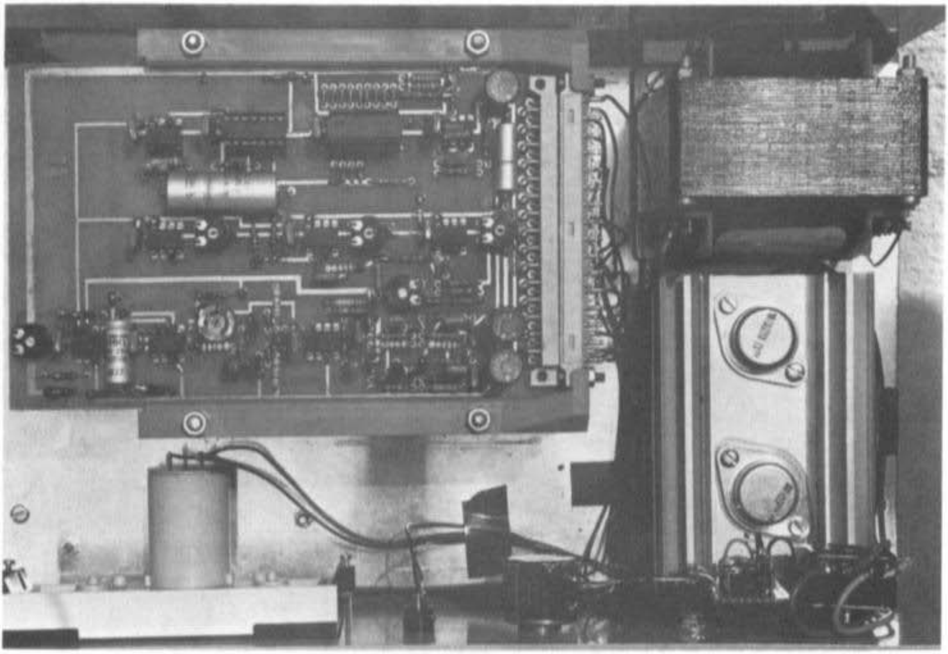

Fig. 5: Plug-in boards RMG 01 and 02 and power supply

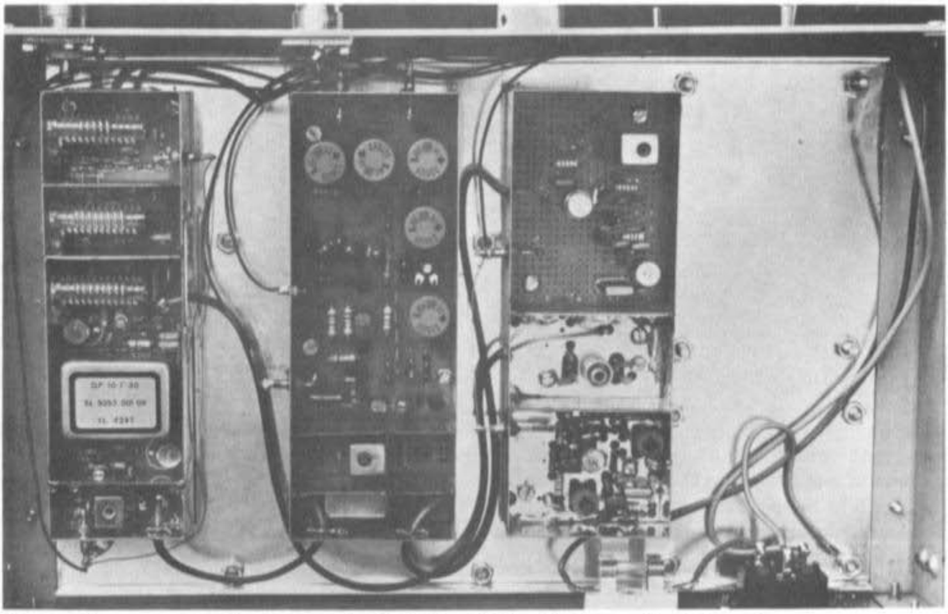

Fig. 6: The screened modules converter, RMG 03 and 04 on the lower side of the system

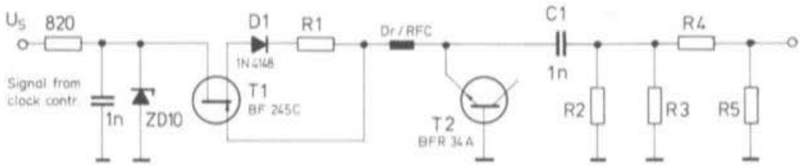

Fig. 7:
The noise-source is operated with a switched voltage of at least 12 V

4. RECEIVE CONVERTER

The input module DK 1 OF 034 described by J. Kestler in (3) is suitable for use in the noise-figure measuring system after carrying out a few modifications. **Figure 8** shows the modified circuit.

4.1. BANDWIDTH

The highest possible measuring bandwidth is required in order to measure the characteristic value of the noise in a fast, **and** accurate manner. For this reason, measuring bandwidths of several MHz are often used for professional applications. If radio communications are made in this frequency range, usually screened cages are used. Since considerable radio communication is made on the amateur bands, and the radio amateur will hardly have a screened Faraday cage available, the author has chosen an RF-bandwidth of only 30 kHz.

The crystal filter XF-107B of the original description has been replaced by a 30 kHz crystal filter. Due to the different impedance of the filter, it is necessary to increase the values of resistors R 1, R 2 to 2 kOhm, whereas C 1 and C 2 are replaced by 30 pF trimmers.

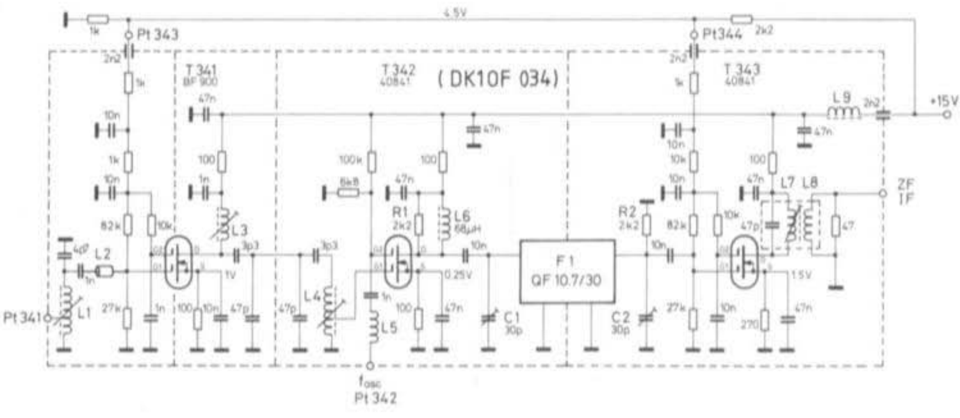

Fig. 8: A part of the circuit DK 1 OF 034 is used as receive converter

4.2. OUTPUT COUPLING

The FM-demodulator CA 3089 is not used during the noise measurements. The 10.7 MHz noise-signal is therefore coupled out after L 8 and the 47 Ohm resistor.

4.3. CONTROL

The gain of the input module DK 1 OF 034 can be influenced greatly with the aid of the control voltage U_C. However, module RMG 03 is responsible for the gain control in order to allow the use of other receive converters and to avoid the higher noise-figure that would be present when the gain was controlled down. For this reason, U_C is kept at a constant value via a voltage divider.

Although the noise figure of the input transistor was given to be 2 dB, we were only able to obtain a value of 4.5 dB after carefully aligning this converter.

5. THE DEMODULATOR AND AGC AMPLIFIER

The demodulator and control module is designated RMG 03. It is designed so that it can also be used with other receive modules. The noiseband (10.685 – 10.715 MHz) is converted to an AF-band of 5-35 kHz with the aid of the described receive converter and a 10.720 MHz oscillator.

5.1. CIRCUIT DESCRIPTION

Figure 9 shows the circuit diagram of the demodulator and AGC amplifier. The mixer IE 500 converts the noise band to AF-level. It is provided with two 50 Ohm matching filters connected in series at the IF-output which are provided to ensure that no RF-signals can be fed to the connected audio amplifier. The first stage of the AF-amplifier is also designed so that it represents a 50 Ohm termination. Since the noise voltage is in the order of several μV under unfavourable conditions, a considerable amount of filtering is required for the voltage supply and operating point adjustment. For this reason, an additional voltage of approximately 10 V is stabilized and passed through two RC-links which are connected in series.

The lower cut-off frequency of the amplifier is designed to be 1 kHz in order to ensure that no measuring errors are caused by the 1/f noise of the transistor. The FET T2 is used as a variable resistor and allows the overall gain to be varied by approximately 40 dB.

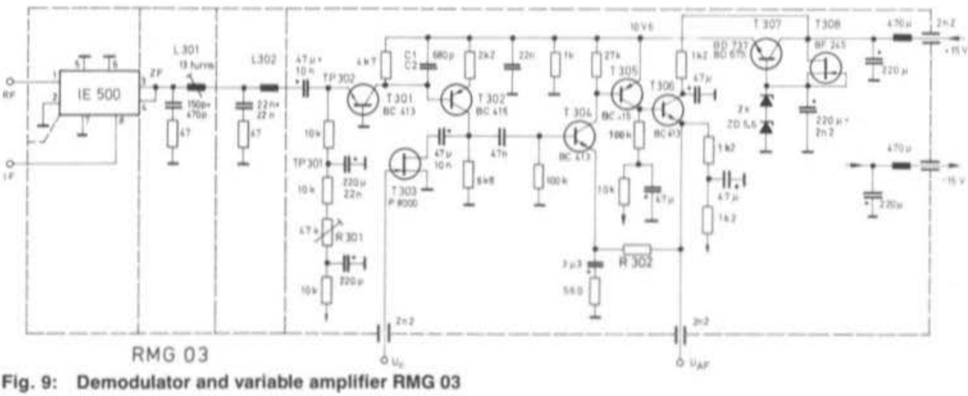

Fig. 9: Demodulator and variable amplifier RMG 03

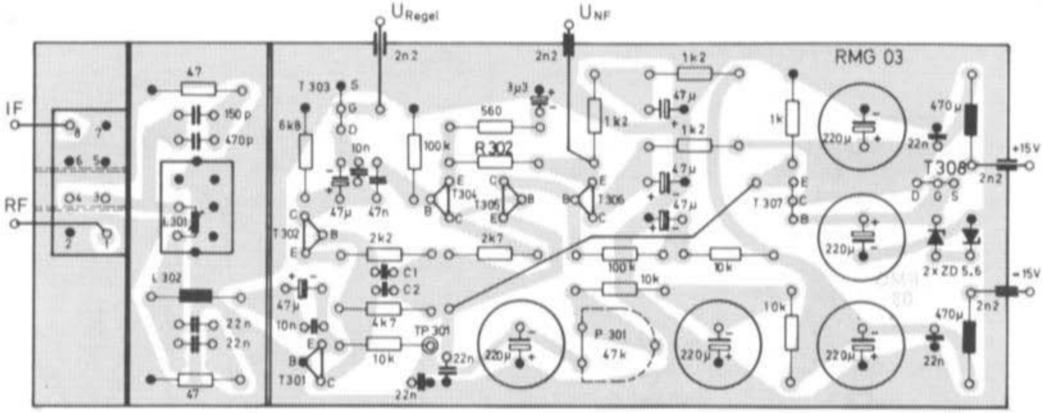

Fig. 10: Component locations on the single-coated PC-board RMG 03. Dimensions are 135 × 50 mm

5.2. CONSTRUCTION OF MODULE RMG 03

A PC-board of 135 mm × 50 mm was designed for accommodating this module. The component locations are given in **Figure 10**.

L 301: Special coil set D 41-2165; 13 turns of 0.3 mm enamelled copper wire

L 302: 120 μH choke

R 302: 220 kOhm

This resistor is reduced in value after the noise alignment of the receive converter.

The PC-board can be enclosed in a standard metal box and should be provided with the screening panels shown in the circuit diagram and in **Figure 11**.

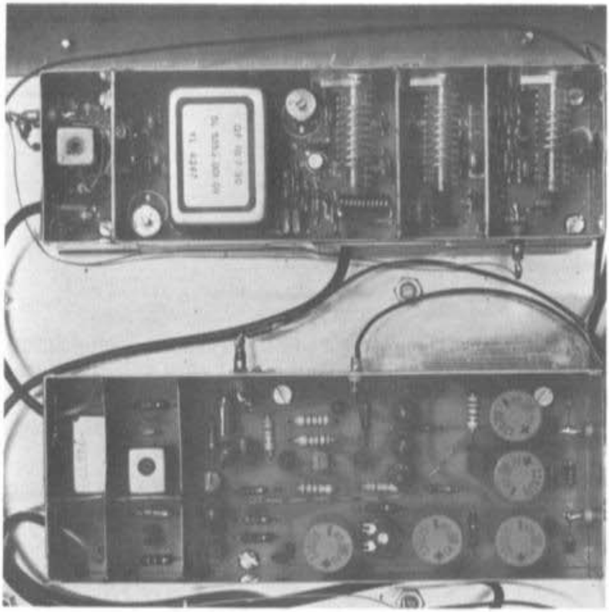

Fig. 11: The photograph shows the receive converter (above), and module RMG 03 (below)

5.3. SWITCHING ON AND ALIGNMENT

Before commencing alignment, one requires a voltmeter (approx. 10 kOhm/V), an oscilloscope, and an AF-generator (at least a 10 kHz square-wave generator with variable voltage divider).

The input U_C should be connected to a variable, negative voltage (e. g. via a 100 kOhm potentiometer between ground and − 15 V). The internally stabilized voltage of 10.6 V should be checked after connecting the operating voltage. Resistor R 1 should be adjusted so that a voltage of − 5.8 V is present at TP 1. Due to the large time constant of the filtering for the operating point voltage, the alignment can only be carried out slowly. For this reason, it takes several seconds after switching on for the stage to operate. The AF-generator is connected to TP 2 via a 1 MOhm resistor, and aligned to approximately 10 kHz. The voltmeter is now connected to U_C. A voltage of approx. − 10 V is fed to U_C. The output voltage of the AF-generator is now set so that U_{AF} is not distorted. The gain between TP 2 and U_{AF} should be approximately 10^5. On slowly reducing the value of U_C, the gain will at first remain fairly constant, after which it will drop suddenly **(Fig. 12).** This voltage threshold U_{CT} should be noted. It is required for the alignment of the control circuit. A gain range of approximately 40 dB should be possible by varying the bias voltage.

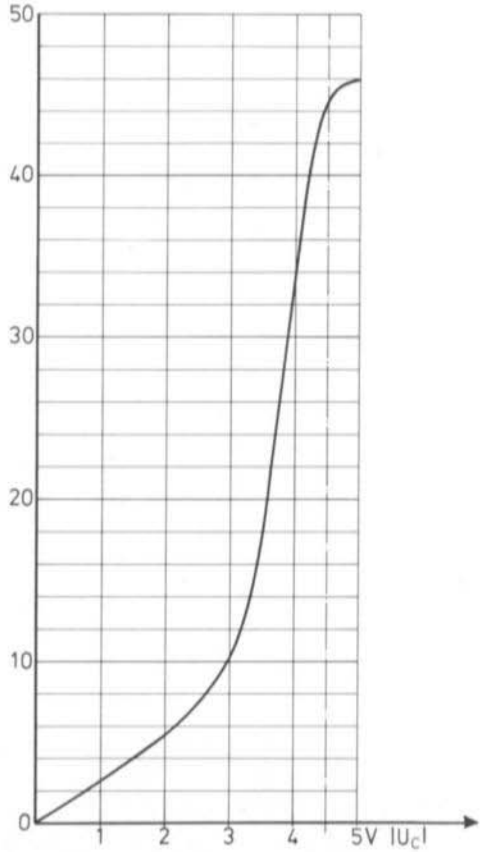

Fig. 12: Gain as a function of the control voltage

6. OSCILLATORS

A carrier of 133.400 MHz at 0 dBm is required for driving the receive converter. This can be achieved using a local oscillator circuit such as provided on module DJ 7 VY 002 by M. Martin in (4). Very few modifications are required:

Q : 66.700 MHz
L 7: 7 turns (otherwise as described)
L 9: 5 turns (otherwise as described)
The signal is coupled out after F 4.

The mixer of the RMG 03 is driven with a 10.720 MHz signal at a level of 7 dBm. The circuit described by F. Krug, DJ 3 RV in (5) can be used for this. Of course, one will not require the components for switching the oscillator.

Part 2 or this article is to describe the following modules:
Control module RMG 02
Indicator electronics, and reference voltage generator RMG 01

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VHF COMMUNICATIONS 14,
Edition 3/1982, pages 172 – 189

Matjaž Vidmar, YU 3 UMV

A digital storage and scan converter for weather satellite images

Part 2: Storage Module

Edition 4/1982 of VHF COMMUNICATIONS described the electronic module board YU3UMV 001. Part 2 is now to describe the storage board YU3UMV 002. As was mentioned in the appendix to part 1 on page 208, the original design has been equipped with the latest 64 kBit memories in order to obtain a 384 kBit storage that provides a spatial resolution of 256 lines of 256 pixels, and 64 grey levels.

Part 3 of this article will describe a colour modulator with VHF oscillator that allows the images to be displayed on a CCIR PAL colour TV-receiver.

If there is sufficient interest among our readers, the author would be willing to discuss how this video storage module can be used für SSTV.

2. STORAGE MEMORY BOARD YU3UMV 002

The frame storage module YU3UMV 002 comprises the main 64k x 6 Bit main storage, the write and read scan clock generators, and the D/A converter in order to regenerate the standard, analog video signal. A memory capacity of 64k x 6 Bit enables a spatial resolution of 256 lines of 256 pixels to be obtained with 64 grey levels. In the described circuit, one line of the frame memory is used as a buffer memory during the write process and the remaining 255 lines comprise the required picture on the TV-monitor. PC-board YU3UMV 002 generates a 320 line, non-interlaced TV-frame. The remaining 65 lines are required for the vertical fly-back and an upper and lower edge on the screen. Both negative and positive video signals are available at the output, which means that the storage is compatible with almost any CCIR TV-monitor available on the market.

The serial data generated by YU3UMV 001, or another source, are firstly converted to a parallel format. In order to avoid disturbing the read operations from the frame memory, data is written into the frame memory during the horizontal fly-back period. The frame memory is scanned in both write and read modes by generating the addresses using a series of binary counters. It should be mentioned immediately that it is only important to read the data out of the memory exactly in the same sequence that it has been written into it; the physical position of the data within the memory is not important from the user's point of view. It is thus important to immediately distinguish between external memory scanning (corresponding to the image scanning), and internal memory organization, which is also a bi-dimensional matrix. These two organizations have no relationship to another (at least not in theory), which means that all address lines are equivalent from the user's point of view, except for some technical constraints in the case of dynamic RAMs, which we shall discuss later.

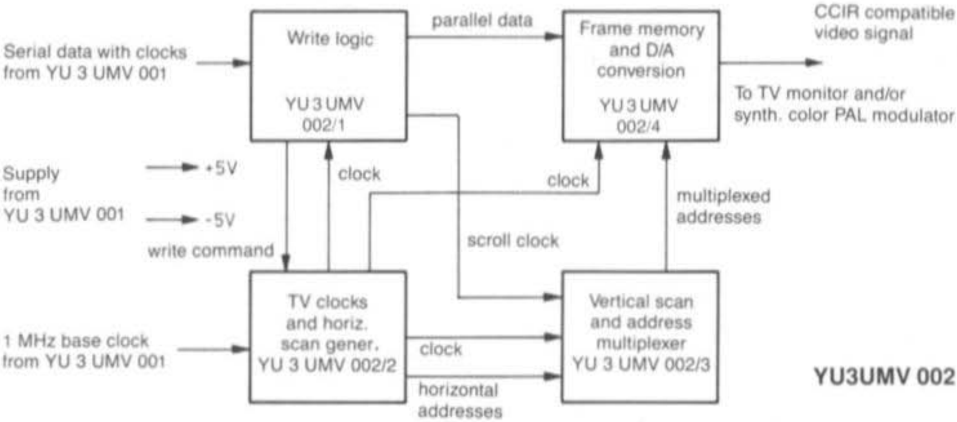


Fig. 12: Block diagram of module YU3UMV 002

The same circuits that generate the scanning addresses in the read mode, also generate the TV-blanking and synchronizing pulses. These are combined with the digital video information in the D/A-converter to obtain a standard, analog TV video signal.

2.1. CIRCUIT DESCRIBTION

In order to simplify the description of the circuit, the actual circuit diagram of the frame memory YU3UMV 002 was divided into four parts as shown in the block diagram given in **Figure 12.**

2.1.1. Write Logic

The write logic shown in **Figure 13** comprises the serial-to-parallel conversion, the write-cycle synchronizing circuit, and the write pixel counter.

The serial data originating from YU3UMV 001 (or other source) are clocked into the shift register I 201. I 202 counts the number of bits clocked into I 201. After all six data bits of a pixel (grey levels) have been accepted by I 201, I 202 will generate a strobe pulse to transfer the data into the latch of I 201. A delayed strobe pulse also resets the SR-flipflop comprising two NOR gates (1/2 I 203), which in turn resets the I 202 counter and generates a request for a write cycle to the write-cycle synchronizing flipflops (I 204).

The write command is synchronized with the rise slope of the $\overline{RAS}$ clock (Row Address Strobe) at the end of a TV-line in order to perform the write cycle during the horizontal fly-back. The write command also advances the write pixel counter to generate the write horizontal addresses WHA 0 to WHA 7.

The next pixel clock pulse sets the SR flipflop enabling I 202 to count the bits once more and to repeat the write cycle. After 256 pixels have been written into the memory, the pixel counter reaches its final state, after which pin 7 ($\overline{CO}$ = Carry Out) of I 206 will go low thus inhibiting further write cycles, and will generate a scroll clock pulse, which sets a new line in the image.

The following line can only be written when the write pixel counter has been reset by the line clock pulse (compare the time plan given in Figure 9 of part 1 of this article).

The pixel counter can count up or down, according to the scanning direction of the image to be displayed. A front panel switch is provided to select either right (West-to-East) or left (East-to-West) scanning, according to whether the polar-orbiting satellite is in its ascending or descending mode: (North of South going).

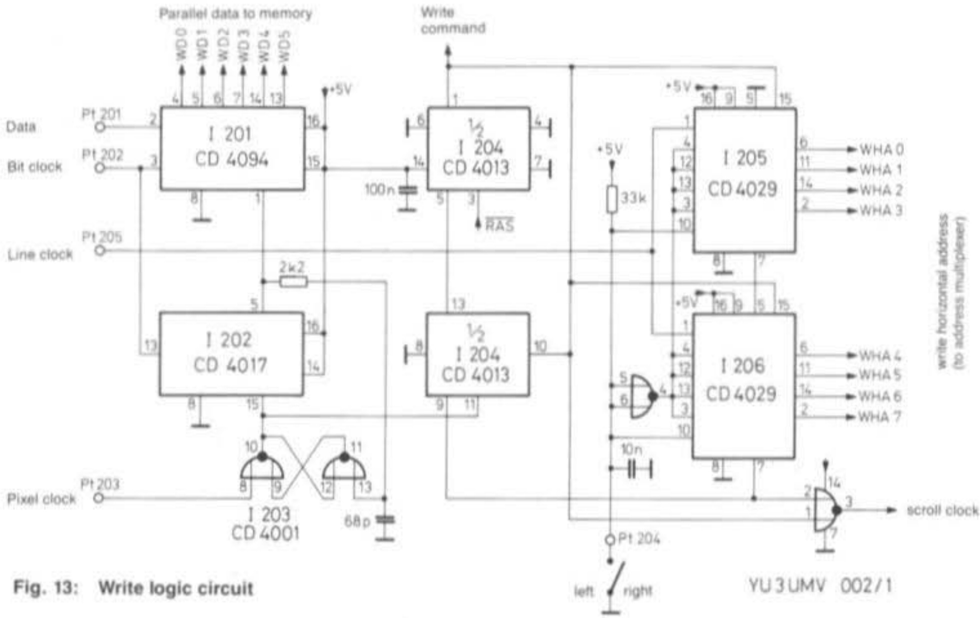


Fig. 13: Write logic circuit

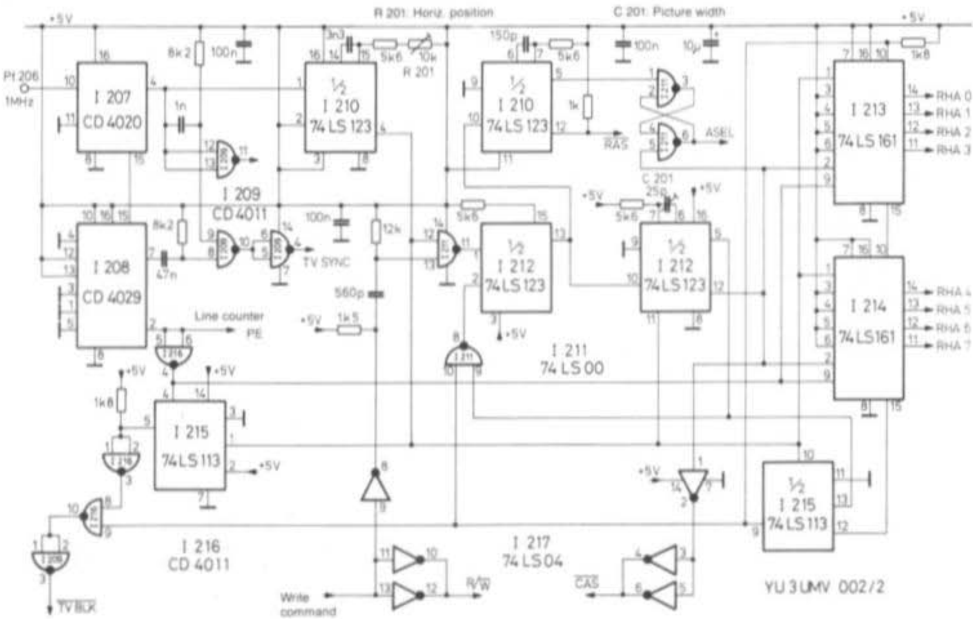


Fig. 14: TV-pulse and horizontal scanning generator

2.1.2. TV Clocks and Horizontal Scan Oscillator

This part of the circuit is given in **Figure 14** and includes a divider and a series of mono-stables to generate the various synchronizing pulses that are all derived from the 1 MHz clock on module YU3UMV 001. In addition to this, it also includes the horizontal pixel oscillator and the read pixel counter.

The 1 MHz clock pulse is fed to I 207 which divides it by 64 to obtain a frequency of 15.625 kHz corresponding to the TV line frequency. This frequency is divided further by 32 in I 207 and by 10 in I 208 to provide a total division factor of 320 to obtain the 48.8 Hz frame (vertical) frequency. Two simple monostable circuits obtained using C-MOS gates (1/2 I 209), provide the composite TV synchronizing pulses, designated $\overline{\text{TV SYNC}}$. The horizontal blanking pulses are obtained in one half of I 215 whereas vertical blanking pulses are obtained by delaying the pulses present at pin 2 (Q 4) of I 208 using a flipflop (1/2 I 215). The composite TV blanking pulses are then designated $\overline{\text{TV BLK}}$.

The clock and other signals required to drive the dynamic memories are best explained together with **Figure 17**.

At the commencement of a TV-line, a pulse generated in one half of I 210 (pin 4) commences the horizontal pixel oscillator built up using the two mono-stable circuits of I 212. The period of the horizontal pixel oscillator can be adjusted with the aid of C 201. This determines the width of the required image. Since there are 256 pixels per line, the useful line length is in the order of 51.2 μs out of the 64 μs of a complete TV-line, including fly-back.

The most difficult task during the design of this scan converter was to retrieve the data at a sufficiently high rate from the relatively slow 64 kBit dynamic memories available. The parameter of interest is the read cycle time, which is specified as 230 ns even for the fastest 150 ns access time devices. A "page mode" reading process is the only possible choice.

The $\overline{\text{RAS}}$ clock pulse is generated in the second, retriggerable mono-stable circuit of I 210 (pin 12). Since the associated RC-constant is quite high, the mono-stable circuit is continuously in the active state when triggered by the fast pixel oscillator. In this manner, a long $\overline{\text{RAS}}$ read pulse is generated. The $\overline{\text{CAS}}$ (Column Address Strobe) clock pulse is generated by delaying (and amplifying) the pixel oscillator pulses. An SR-flipflop (1/2 I 211) generates the ASEL (Address Select) signal that controls the address multiplexer.

Each pulse of the pixel oscillator advances the pixel counter by one, generating the read horizontal addresses RHA 0 to RHA 7. As soon as the 256 pixels have been counted, a flipflop is triggered (1/2 I 215) that disconnects the feedback path of the oscillator. Any write request is synchronized with the rise slope of the $\overline{\text{RAS}}$ clock pulse. Since the feedback of the pixel oscillator is interrupted, the write command produces a single $\overline{\text{CAS}}$ pulse. The counters, flipflop, and mono-stable circuits are then reset by the next line start pulse generated in the first half of I 210 (pin 4).

During the vertical fly-back period, the page mode cycles are shortened to a few $\overline{\text{CAS}}$ cycles in order to decrease the memory power dissipation, since their only function is to enable write cycles.

2.1.3. Vertical Scan and Address Multiplexer

The vertical scan generator comprises the scroll counter and the line counter. These circuits are shown together with the address multiplexer in **Figure 15.**

The most obvious solution is to scan the memory in exactly the same way during the write and read operations. Unfortunately, this is quite unsatisfactory when receiving radiometer, scanned images from polar orbiting satellites, since the displayed images are usually divided into two sectors, one containing old image data, and the other new information being written into the memory. A much more elegant method is to scroll the image: New data lines are introduced to the top or bottom of the image field and the previous information is shifted down or up respectively. In this way, the display acts in a similar manner to a window moving along a radiometer-scanned image. Fortunately, scrolling is quite easy to implement in practice.

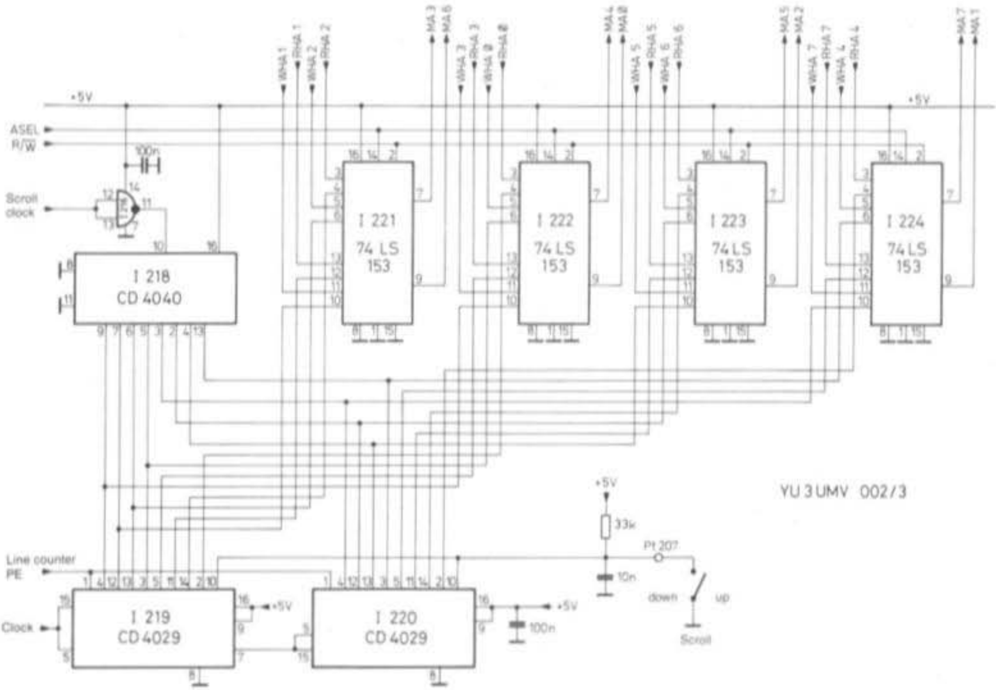


Fig. 15: Vertical scanning and address multiplexer

The scroll counter I 218 provides the vertical addresses during the write process. The scroll counter is incremented after writing a complete line into the frame memory. The scroll counter also supplies the start address for the line counter that generates the vertical addresses during the read process. In this way, data is always written into the first scanned line of the TV frame memory. This line acts like a buffer memory. Since the content of this line is continuously changing, it is blanked by the $\overline{\text{TV BLK}}$ signal.

Whether the previous image information is shifted up or down is dependent on whether the line counter is counting up or down respectively. A front-panel switch is provided to select the scroll up for North-to-South scanned images, and scroll down for South-to-North images.

The 64 kBit memories require 16 address Bits to select the desired location in the memory. Most 64 kBit dynamic RAMs have 8 address lines. The 16 Bit adress is then provided sequentially as two consecutive 8 Bit words. Since the delay between supplying the first part of the address, and the second part is quite short (down to 20 ns), a fast electronic switch (low-power Schottky TTL), designated as address multiplexer, has to be used. The address multiplexer shown in Figure 15 has the additional function of switching between read and write addresses during write cycles. The address multiplexer includes eight 4-to-1 switches controlled by the two select lines: ASEL for the selection between the first and second part of the address, and $R/\overline{W}$ for the selection between read and write addresses. The eight outputs MA 0 to MA 7 drive the memory address lines directly.

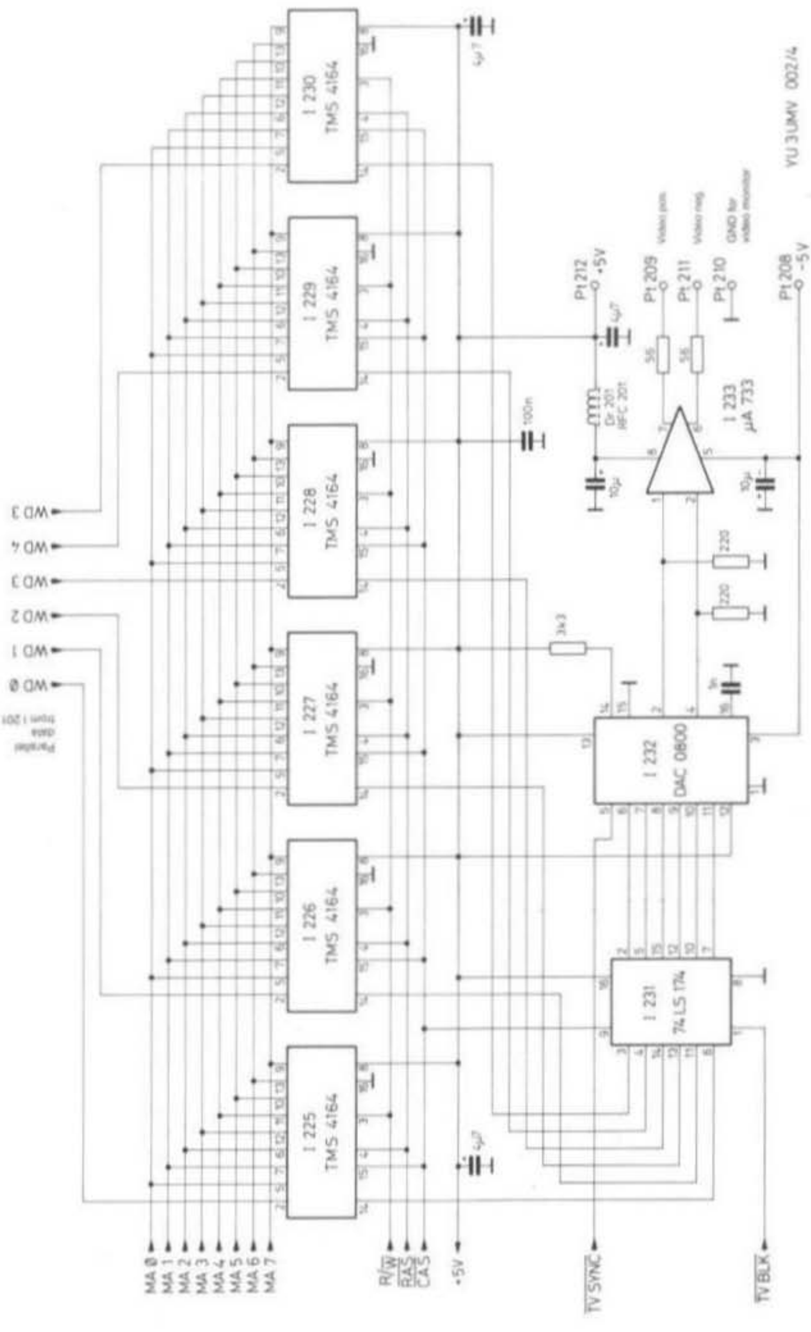


Fig. 16: Video storage and digital/analog converter with output video amplifier

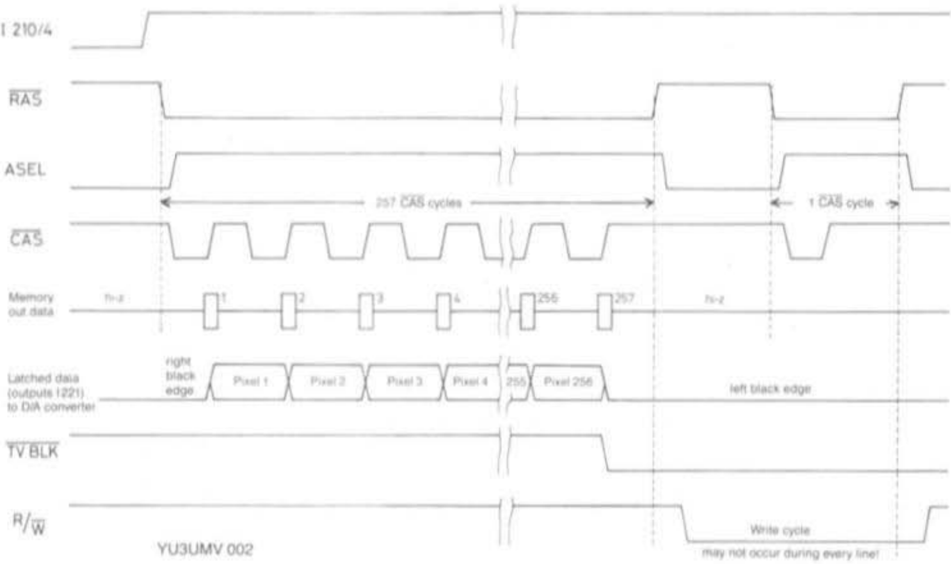


Fig. 17: **Read and write processes in the video storage module**

2.1.4. Frame Memory and D/A Converter

The frame memory and the D/A converter are shown in **Figure 16** together with the associated logic circuitry. The six 64 kBit dynamic memories are operated in parallel: Each memory stores one Bit of the 6 Bit data word which represents one individual pixel of the image. The data word at the output of the memory is valid only for a short period (see **Figure 17**). A data latch (I 231) is triggered by the rise slope of the CAS clock pulse in order to extend the data to the whole cycle. The TV BLK signal resets the latch and Thus forces the outputs to zero (black level).

Integrated circuit type DAC 0800 is a current-multiplying D/A converter. The output current is a fraction of the current flowing to the + REF pin 14, and the fraction is determined by the digital word present at the B 1 to B 8 inputs. B 1 is the most significant Bit and is driven by the TV SYNC signal. The synchronizing pulses are somewhat greater than prescribed by the TV-standard, however, no disadvantage has been noticed in practice. The data word containing the video information is applied to the six subsequent inputs. The last input, representing the least significant Bit, is not used.

The DAC 0800 is a very fast digital/analog converter, and the fall time of the output current is in the order of 100 ns. For this application, it is much more important that it does not generate large switching transcients as was the case with older integrated D/A converters, such as MC 1408. This means that a fast (and critical) sample-and-hold stage could be eliminated at the video output.

The output level of I 232 is, however, quite low. For this reason, a video amplifier µA 733 (I 233) is used to increase the signal level to approximately 1.5 V_{pp}/75 Ohm, which is suitable for most TV-monitors.

2.1.5. Interfacing to YU3UMV 001

The frame memory module YU3UMV 002 requires exaxtly the same control signals as the previously designed 16 k x 6 Bit storage module, which means that no modifications are required to any circuits on module YU3UMV 001. However, there are some slight differences in the connection of the resolution-zooming selector (Figure 4 of part 1). Now, only a three-position selector is used (instead of four) since the 2.4 kHz signal is no longer required and the corresponding connection to Pt 107 is deleted.

Table 1 of part 1 is thus no longer valid and is now replaced by **Table 2** below.

Figure 18 shows the interconnection of the two modules and the connection of the few controls. Although the storage capacity has been multiplied by four in comparison to the prototype, it will be noted that the interconnections to the image format selector given in Figure 5 of part 1 remain unchanged. A three-level switch is shown, but this is only a suggestion in order to clean up the front panel somewhat and to simplify the operation. Finally, it should be noted that the $\overline{\text{ENABLE}}$ input Pt 116 should be grounded if the scan converters YU3UMV 001/002 are only to be used for APT reception – in other words not for digital, HRPT images.

Zooming resolution switch Bit clock	Sampling frequency	METEOSAT WEFAX	NOAA APT 1)	METEOR 240 lines/min.	METEOR 120 lines/min. 2)
19.2 kHz	2400 Hz	x 2	x 2	x 2	– – –
9.6 kHz	1200 Hz	x 1	x 1	x 1	x 2
4.8 kHz	600 Hz	– – –	VIS + IR	– – –	x 1
2.4 kHz	300 Hz	– – –	– – –	– – –	– – –

1) Meteo/NOAA switch (Pt 11) in NOAA position
2) External 2400 Hz synchronisation required

Table 2: Possible image formats of the 64 kByte storage module

2.2. CONSTRUCTION

The frame memory module YU3UMV 002 is accommodated on a double-coated PC-board having the same dimensions as the control board YU3UMV 001 (190 x 85 mm). The conductor side of this PC-board is given in **Figure 19** together with the components location plan. The connection pin density of the integrated circuits demands a very close geometry on the board; for this reason, extreme concentration is required when soldering the components into place in order to ensure that no unwanted solder bridges are made. Special attention must be paid to the condition of the through-contacts, which are provided on the component side below the integrated circuits. Remember, that it is not possible to check or correct these after soldering the ICs into place!

The MOS-ICs of the B-series are protected, which means that there are no advantages of using sockets. However, if sockets are preferred, it is important to only use the very best quality available. Low-cost sockets easily cause poor contacts, which are very difficult to locate in such a complex circuit.

Similar to YU3UMV 001, all connections to switches, connectors, and the electronic module are made via connection pins. The only connection that requires a certain amount of care is the video output. Although the video signal level is high (1.5 V_{pp}), it is a wideband signal having a wide dynamic range, and is thus very sensitive to interference generated by the logic circuits. Experience has shown that such interference is usually obtained by ground loops, which underlines the importance of good grounding.

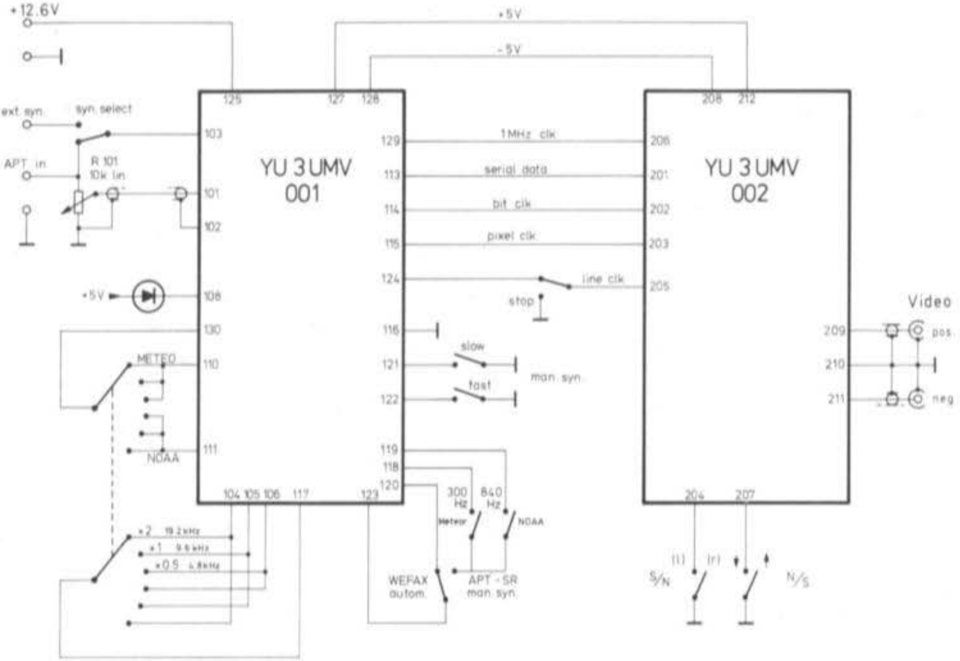


Fig. 18: Interconnection of the modules "Electronic Board" and "Video Storage Module"

2.3. SELECTION OF THE COMPONENTS

The most important components of module YU3UMV 002 are listed later. It is recommended that C-MOS ICs of the new B-series are used. All TTL circuits are low-power Schottky types, since only these are fast enough, and can be driven by C-MOS logic.

Time-determining components always cause problems due to their wide tolerances. A spread of 100% was noticed for the dual mono-stables type 74LS123 made by different manufacturers! This means that it is important for the two 74LS123 to be from the same manufacturer and, if possible, have the same date of manufacture printed on the case.

There are a number of different 64 kBit dynamic memories available on the market. The major differences between 16 pin-DIL RAMs are in the function of pin 1. This pin enables a self-refresh mechanism in some memories, whereas others do not have this pin connected. Both types can be marked 4164! The circuit of module YU3UMV 002 was designed for memories not having this self-refresh feature.

The 64 kBit memories can have different internal organizations, for example, the TMS 4164 (Texas Instruments) is organized as 256 rows x 256 columns, whereas the HM 4864 (Hitachi) has 128 rows x 512 columns. This is important in practice, since the HM 4864 requires only half as many cycles as the TMS 4164 for refresh. Finally, each manufacturer selects his memories into various speed groups after production. Memories having a row acces time of 150 ns or less are required for this circuit.

The maximum time between two refresh cycles is usually specified as 2 ms for 128 row memories, and 4 ms for 256 row memories. Experiments have shown, however, that dynamic memories are able to maintain the data without refresh for many seconds at normal ambient (room) temperatures! Probably, the above mentioned limits only apply for operation at the maximum permissible ambient temperature, and maximum device dissipation power. Furthermore, in contrast to computer application, 100 percent reliability is not required here, and it is possible for a complete refresh to be performed only once every TV-frame (20 ms) in the case of 256 row memories, or twice in the case of 128 row memories.

It is also possible for the "page-mode" read cycle to be increased longer than the maximum value specified in the data sheet (usually 10 μs). The power dissipation and thus the operating temperature of the memories are very low in this circuit, since they are dependent mainly on the number of $\overline{RAS}$ cycles per second, which is very low in our application due to the page-mode addressing.

Modern dynamic memories are usually specified in the data sheets as being fully TTL compatible. Unfortunately, this does not necessarily mean that low-power TTL circuits can directly drive highly capacitive memory clock and address lines. In particular, the active pull-up of the low-power Schottky ICs may not be sufficient, and an external pull-up resistor (680 Ohm – 1.5 kOhm) may be required. The author has had no such problems in conjunction with the TMS 4164, however, he had many such problems in conjunction with earlier circuits. Both low-power Schottky TTL circuits and dynamic memories exhibit the large variations of these parameters from manufacturer to manufacturer.

I 201:	CD 4094
I 202:	CD 4017
I 203:	CD 4001
I 204:	CD 4013
I 205, 206, 208, 219, 220:	CD 4029
I 207:	CD 4020
I 209, I 216:	CD 4011
I 210, I 212:	74LS123 (see text)
I 211:	74LS00
I 213, I 214:	74LS161
I 215:	74LS113
I 217:	74LS04
I 218:	CD 4040
I 221 – I 224:	74LS153
I 225 – I 230:	TMS 4164-15 or HM 4864-2 for other types see info. in text
I 231:	74LS174
I 232:	DAC 0800 (National Semiconductors
I 233:	μA 733 CK (Signetics)
R 201:	10 kOhm linear trimmer, spacing 10/5 mm
C 201:	22 pF plastic foil trimmer (Phillips: green)
RFC 201:	six-hole ferrite choke

All electrolytic capacitors are tantalum types.

The 100 nF bypass capacitors are ceramic disk types or multi-layer ceramic. All other capacitors are plastic-foil types, since cheap ceramic capacitors usually have too high a temperature coefficient.

List of 64 k memory ICs that can be used in the YU3UMV 002 module

Type:	Manufacturer:
TMS 4164	Texas Instruments
MCM 6665	Motorola
UPD 4164 D	NEC
HM 4864	Hitachi
MB 8264	Fujitsu
IMS 2600	INMOS
MK 4564	Mostek
I 2164	Intel
NMC 4164	National Semiconductor
TMM 4164 C	Toshiba
MSM 3764	Oki Semi
F 4164	Fairchild
HYB 4164	Siemens

All these 16-pin DIL ICs should be usable without modifications in module YU3UMV 002. However, the author has only been able to check types TMS 4164 and HM 4864 in the actual circuit.

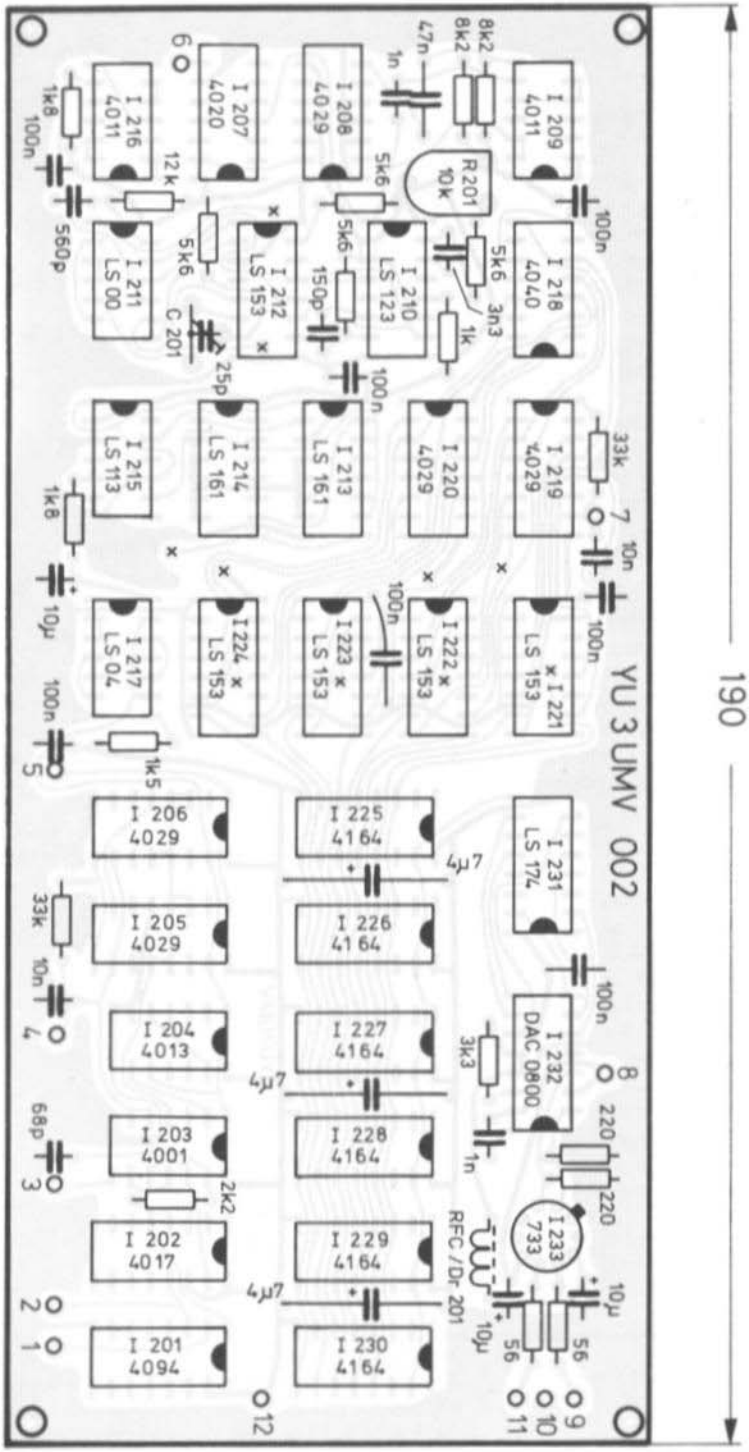


Fig. 19:
The video storage module is accommodated on a double-coated PC-board with through-contacts

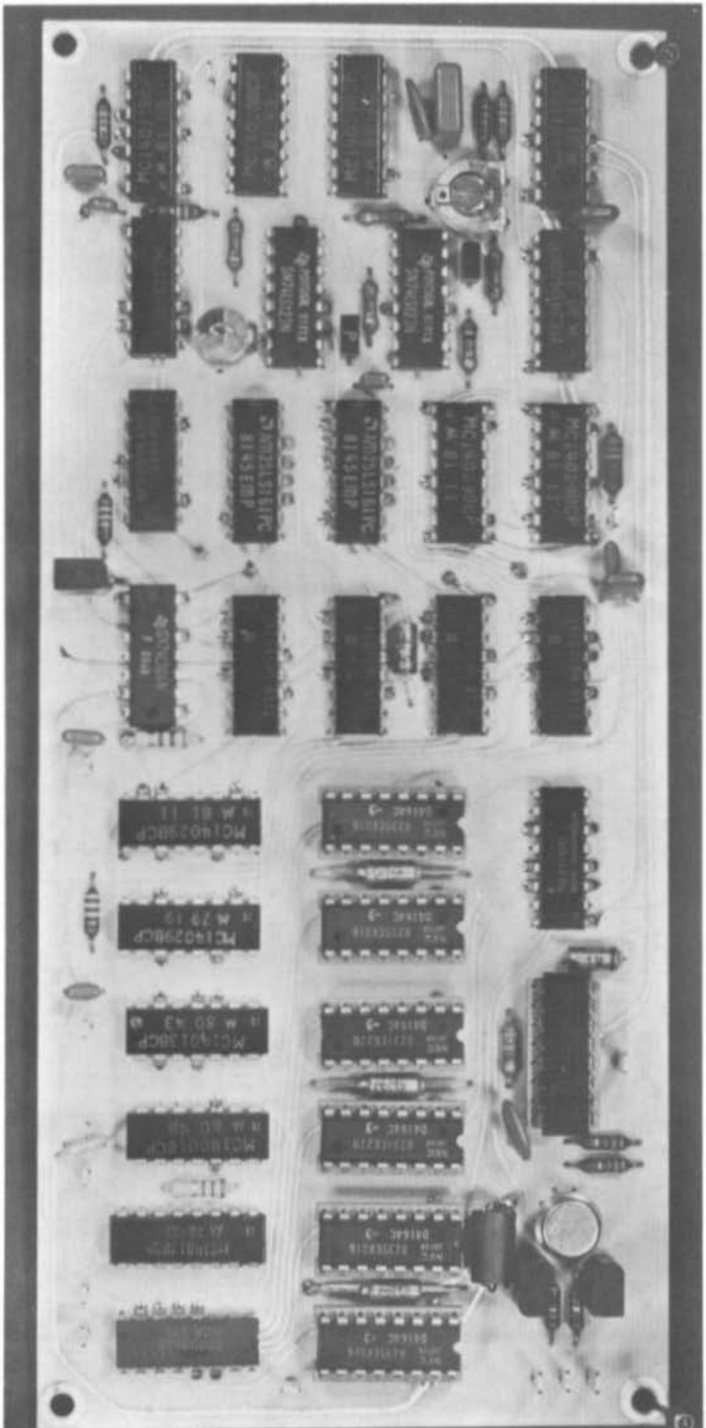
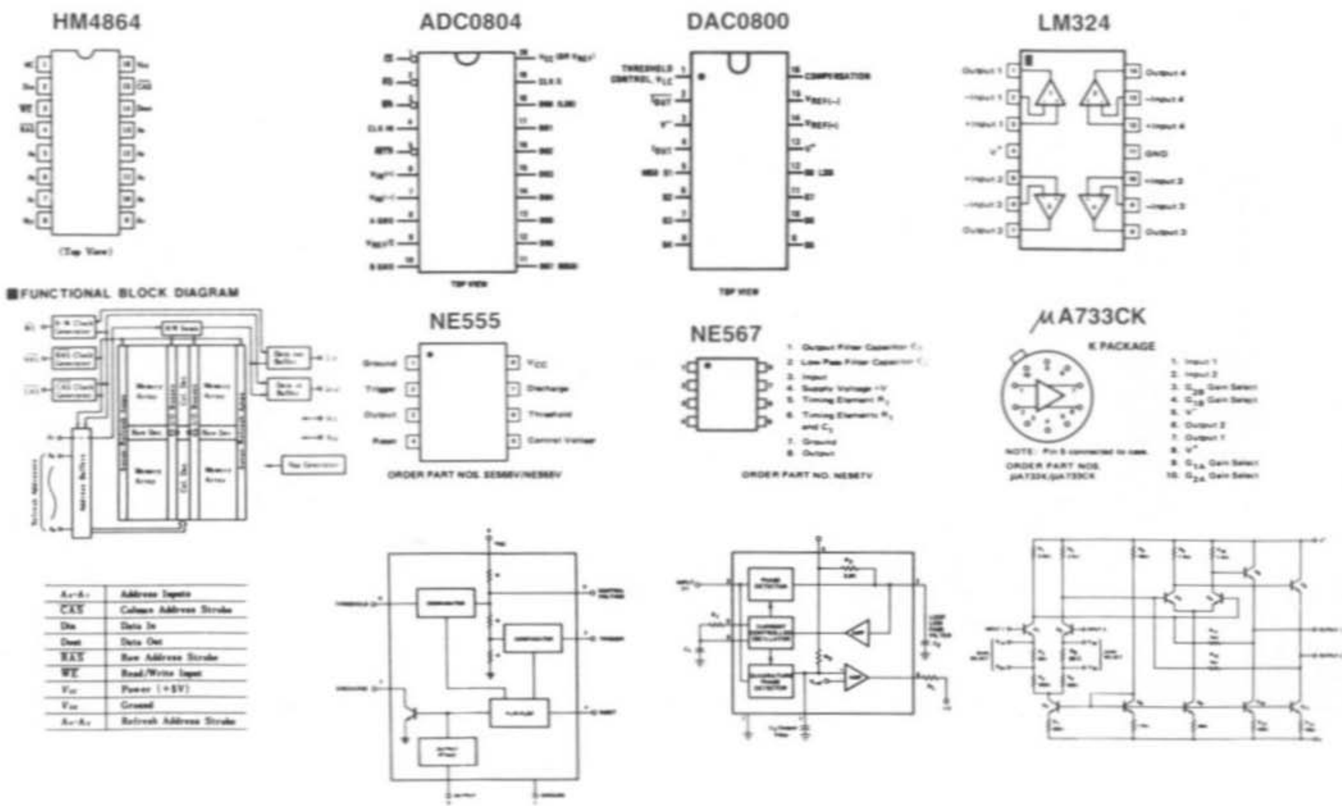


Fig. 20:
A photograph of the author's prototype YU3UMV 002



A_0–A_7	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{in}	Data In
D_{out}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{cc}	Power (+5V)
V_{ss}	Ground
A_0–A_6	Refresh Address Strobe

Connection diagrams of the less-known integrated circuits

2.4. ALIGNMENT

Since module YU3UMV 002 obtains the power supply, clock pulses, and control signals from module YU3UMV 001, it is obvious that the latter module must have been already tested before connection, at least the power supply and the 1 MHz oscillator. There are only two trimmers on the board of the second module. It is recommended that the alignment be commenced with R 201 (horizontal position) at minimum and with C 201 (horizontal width) at a center position.

After switching on the modules, a pattern showing the random initial memory content should appear on the TV-monitor, which will probably be shifted to the left on the TV-screen. It is now possible for the two trimmers to be aligned for correct position and width of the image.

It should be noted that the adjustment of the image width has precise limits. If C 201 is completely misaligned, one may not able to obtain any image at all! After adjusting R 201 and C 201, it may be necessary for L 101 on module YU3UMV 001 to be realigned to suppress any interference and/or difficulties in the synchronization of the TV-monitor.

3. APPENDIX
Operation of Dynamic RAM Memories

The actual storage elements in dynamic RAMs are capacitors (reverse polarized PN-junctions) that are internally organized as a two-dimensional array of rows and columns. Each storage capacitor has an associated MOS-transistor switch, which can connect it to the common column line.

Each memory access cycle (read, write, page-mode operation, or only refresh) starts with a negative transition of the $\overline{\text{RAS}}$ clock pulse; Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks are high during standby. This $\overline{\text{RAS}}$ clock pulse strolls the first part of the address, designated Row Address, into the corresponding latch of the memory. The content of the latch is immediately decoded, and all the capacitors of the selected row are connected to the corresponding common-column lines. Each common-column line is terminated in a sensitive amplifier to detect whether the small storage capacitor was charged or not.

Since each actual capacitor is leaky, it cannot store the information for an indefinitely long period of time. For this reason, the logic automatically restores the charges on the capacitors after the column-sense amplifiers have detected the states of the corresponding capacitors: The capacitors found charged are charged to the full supply voltage, whereas the capacitors found discharged are completely discharged. This process is called "Refresh", and it must be performed sufficiently frequently to maintain the information in the memory. Since each $\overline{\text{RAS}}$ clock cycle only refreshes a single row of the memory capacitor array, a certain number of $\overline{\text{RAS}}$ cycles is required for the full refresh of the complete array.

C ≙ Column	A ≙ Address
R ≙ Row	S ≙ Strobe

In order to communicate with the memory, the second part of the address has to be provided together with the negative transition of the $\overline{\text{CAS}}$ clock pulse, usually 20 to 100 ns after the $\overline{\text{RAS}}$ transition. The column address is stored in a latch, and decoded by selecting the desired column-sense amplifier/refresh logic. During a read operation, the column decoder simply connects the output of the selected column-sense amplifier to the output pin of the memory IC.

In order to write the data into the desired memory cell, the selected column-refresh logic is forced to copy the data present at the data input pin, instead of the data at the output of the column-sense amplifier. This is achieved by charging or discharging the selected cell capacitor correspondingly.

For some particular applications, like video displays, the exact order in which data will be read from, or written into the memory is known. If cells from a single row are to be accessed, it is not necessary to repeat the same row address each time. More than one $\overline{\text{CAS}}$ cycle may be performed during a single $\overline{\text{RAS}}$ cycle, accessing many different columns. This mode of operation is called "Page Mode". It provides a considerably higher data flow since a number of operations need not be repeated!

Gerd Otto, DC 6 HL

A Mini-SSB-Transceiver for 144 MHz

Part 1

A large number of descriptions have been published for transmit and receive converters for the higher frequency bands 70 cm, 23 cm, and higher. These are usually driven with available (commercial) 10 m or 2 m transceivers. If these transceivers are also to be used for operation on the 2 m or 10 m band, this means that they must be disconnected and reconnected, and how often it is that one wishes to have a separate transceiver for use as driver.

For this reason, the author has designed a small, inexpensive 144 MHz transceiver whose technical specifications are at least equal to, if not much better than the commercial equipment available on the market.

On the transmit side, the output power has been limited to values that are suitable for driving the transverter. This allows the power transistors to be deleted, and thus to construct a very compact unit having dimensions of only 148 mm x 74 mm x 30 mm. According to the application, it can be constructed for a frequency range of 144 to 146 MHz, or 135 to 137 MHz.

1. CONCEPTION AND CONSTRUCTION

Single-conversion with an intermediate frequency of 9 MHz is used for both transmit and receive.

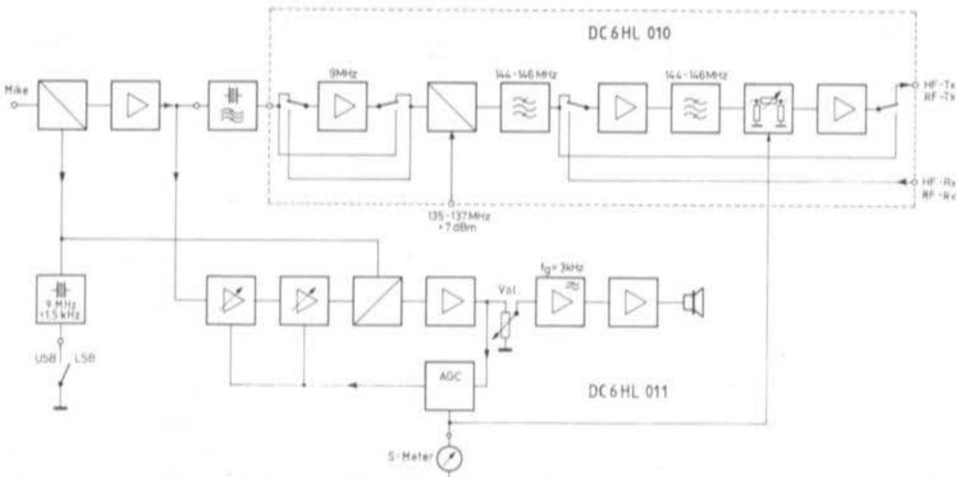


Fig. 1: All components shown outside of the dashed case belong to module DC6HL 011

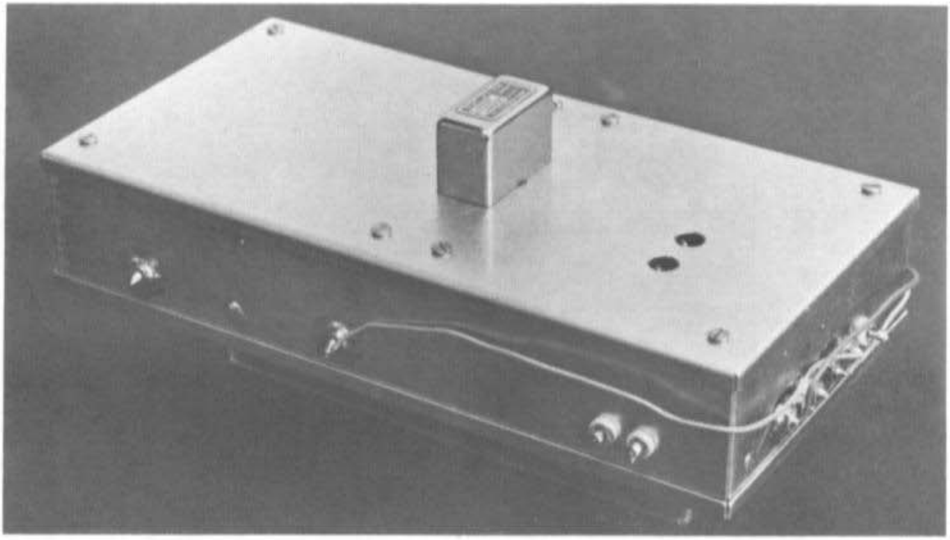


Fig. 2: A complete 2 m transceiver is available if a VXO and a linear amplifier from 5 mW to 0.5 W are added to this module. Suitable modules are to be described in later editions of this magazine.

Expensive and larger components such as crystal filters are used both in the transmit and receive path (see **Figure 1**).

All components are accommodated on a small, double-coated PC-board with through-contacts, and the 9 MHz crystal filter is used to interconnect the AF/IF-board to the RF-board.

In order to achieve ideal electrical conditions, the crystal filter is mounted outside of the metal case, and only its connections protrude into both chambers, in which the PC-boards are accommodated. This allows the high selectivity of the filter to be utilized to the full (see **Figure 2**).

The operating voltage of the miniature transceiver is between 12 V and 16 V. A voltage stabilizer circuit is provided on the RF-board to ensure that the internal operating voltage is maintained at 11.5 V, which can also be used for external accessories.

The transmit/receive switching is made via a PTT-contact which is grounded. The stabilized voltages + U_{TX} and + U_{RX} are also available for external applications.

2. CIRCUIT DESCRIPTION

2.1. AF/IF Board DC 6 HL 011

This part of the circuit is shown in **Figure 3.** All component numbers are higher than 50.

2.1.1. Transmit Path

The AF-signal is fed from the microphone via Pt51 to the input of the integrated mixer I 51, which is built up symmetrically. The drive is made, however, in an unbalanced manner, in order to save using an AF-transformer. For this reason, it is important that inputs 7 and 8 are connected symmetrically, in other words short-circuited for the 9 MHz local oscillator frequency. The RF-signal is injected in a balanced manner (non-grounded). A DSB-signal is available at the push-pull output circuit comprising L 52, whose carrier suppression is excellent, providing that R 51 has been aligned for correct balance. The signal is passed via a buffer (T 51) to the monolythic crystal filter 9M22DI. The termination of the filter is made using the 680 Ω load resistor of the buffer together with the parallel capacitor connected to Pt54.

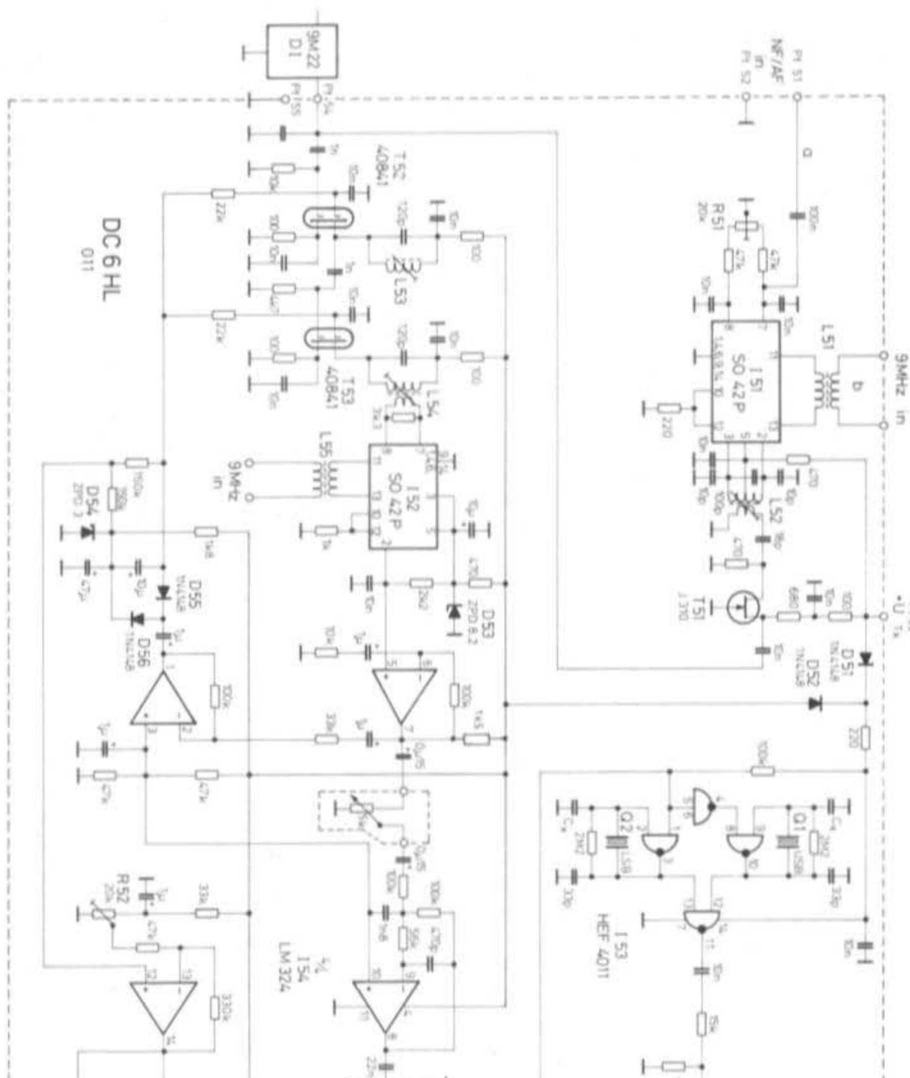


Fig. 3: Circuit diagram of the AF/IF board of the transceiver.

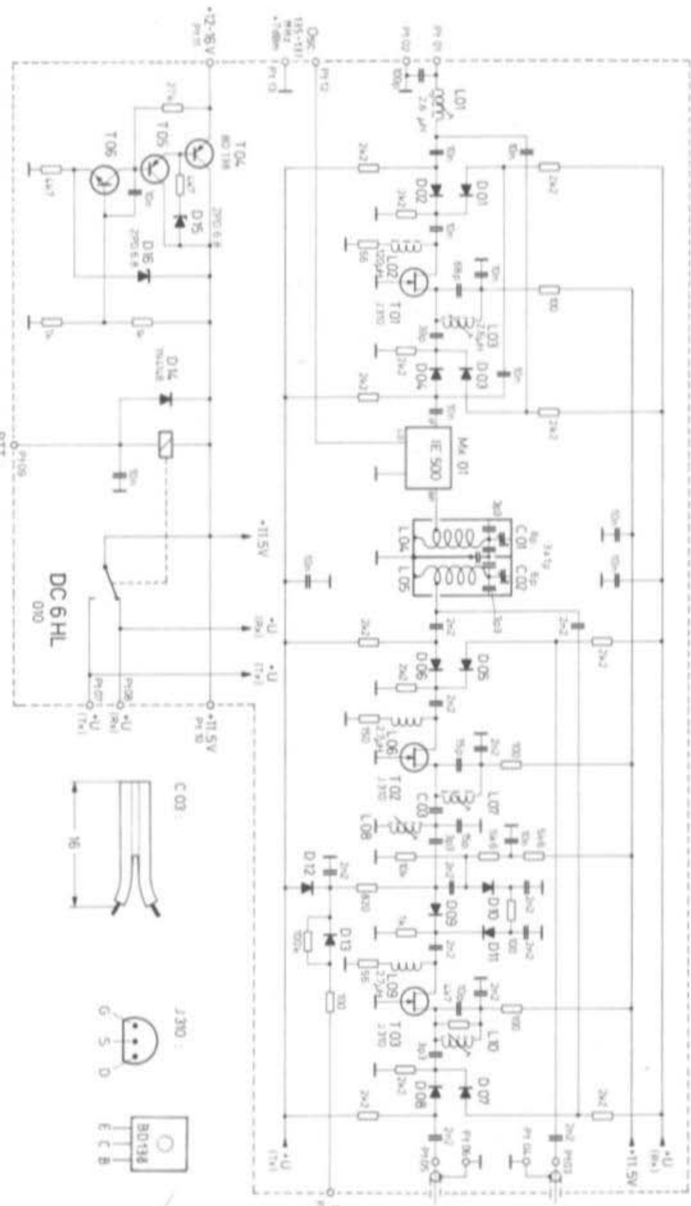


Fig. 4: Circuit diagram of the VHF-module DC6HL 010

2.1.2. Receive Path

After passing through the crystal filter, the IF-signal is passed through the two AGC amplifier stages comprising T 52 and T 53, and is fed via the resonant circuit comprising L 54 to the integrated mixer I 52. The mixer is also provided with the 9 MHz local oscillator frequency via L 55. The demodulated AF-signal is available at the load resistor of 2.2 kΩ, and is subsequently amplified by 11 times in a part of the quadruple operational amplifier I 54. The signal path is separated at the output of this amplifier.

The AF-signal drives an active lowpass filter via a coupling capacitor of 0.15 µF and the external AF-volume control. This lowpass filter is achieved using a further part of I 54. It is designed for a cutoff frequency of 3 kHz. I 55 supplies sufficient output power for driving a small loudspeaker. The operating voltage for this IC is fed in via Pt58 before stabilizing so that the varying load will not have an effect on the control circuit.

In order to generate the AGC-voltage for the receiver, an AF-voltage is tapped off from I 54/7 and fed to a further amplifier with a gain of three times. This, in turn, drives a voltage doubler rectifier comprising D 55 and D 56. The basic level of this rectifier circuit is maintained at + 3 V using the zener diode D 54. This means that a voltage of + 3 V is present at the anode of D 55 which will be driven towards negative voltages. The control voltage is available directly at the gate 2 connections of T 52 and T 53.

In addition, this voltage is divided by two and drives a further operational amplifier that generates the control voltage for the PIN diodes (Pt62). Its operating point and thus the threshold of the PIN-control can be varied with the aid of trimmer R 52. The amplifier output can also be used for driving an S-meter via connection point Pt 61. The 20 kΩ trimmer potentiometer is used for adjusting the zero point, and the 47 kΩ trimmer is used to set the full-scale value.

2.1.3. Carrier Oscillator

The subcarrier for the upper and lower sideband is generated in a quadruple NAND-gate (I 53). The required oscillators are actuated by shorting, or opening a ground contact, and their output signals are combined at a further gate.

The squarewave signal of 11 V (peak-to-peak) drives transformers L 51 and L 55 via a voltage divider. In order to generate the operating voltage for the carrier oscillator, diodes D 51 and D 52 combine the transmit and receive voltage so that an additional, continuously available voltage is not required.

2.2. VHF-BOARD DC 6 HL 010

The circuit diagram of this module is shown in **Figure 4**; all component numbers are less than 50.

2.2.1. Transmit Path

The operating voltage + U_{TX} switches diodes D 02, D 04, D 06, and D 08 to conduct. The transformation link comprising 100 pF and L 01 matches the crystal filter to the input of the 9 MHz amplifier equipped with T 01. At the output of the crystal filter, the impedance is transformed to 50 Ω with the aid of the 39 pF coupling capacitor.

The ring mixer Mx01 converts the signal to 144 MHz. The mixer is followed by a two-stage bandpass filter and two amplifier stages with intermediate bandpass filter and PIN-attenuator. The PIN-attenuator is opened in the transmit-mode with the aid of diode D 12.

The signal is passed via a resonant circuit comprising L 10 and connection point Pt 105 and leaves the transmit amplifier at output HF-TX.

2.2.2. Receive Path

The operating voltage + U_{RX} causes diodes D 01, D 03, D 05, and D 07 to conduct so that the VHF-signal from input HF-RX can pass through the two-stage 144 MHz amplifier with PIN-attenuator. This is followed by the bandpass filter comprising L 04 and L 05 and the mixer that converts the signal to 9 MHz. The output of the mixer is terminated by the input impedance of the 9 MHz amplifier.

After the signal has passed through the amplifier, it is fed via D 03 and the transformation link, comprising L 01 and the 100 pF capacitor, to the crystal filter.

2.2.3. Voltage Stabilization and PTT-Switching

Transistors T 04 to T 06 form a voltage stabilizer circuit that is driven with a voltage of + 12 V to + 16 V. The internal operating voltage of + 11.5 V is provided at the output. The circuit can be short-circuited but requires a diode (D 15) to actuate. The operating voltages for transmit and receive are selected by the relay, which is controlled from the PTT-connection.

3. COMPONENTS

T 01 – T 03:	J310 (Siliconix) possibly also BF246
T 04:	BD 138 (Siemens)
T 05:	BC 415 (PNP)
T 06:	BC 413 (NPN)
D 01 – D 08:	BA 282, BA 244 (switching diodes)
D 09 – D 11:	BA 379 (PIN, Philips)
D 12 – D 14:	1N 4148, 1N 4151
D 15, D 16:	C6V8 (zener diodes)
Mx01:	IE-500, SRA-1 or better: SRA-1H or even better: SRA-3H
L 01, L 03:	Special coil set, type 5138 (blue/red/white)
L 02:	120 μH miniature choke
L 04, L 05:	Air-spaced coils from 0.8 mm dia. silver-plated copper wire (see drawing), 7.5 turns on 6 mm former, coil tap: 1.25 turns from the cold end
L 06, L 09:	2.7 μH miniature choke
L 07, L 08, L 10:	Special coil set, type 5118 (silver-plated)
C 01, C 02:	Ceramic miniature spindle trimmer 6 pF (Philips)
C 03:	16 mm piece of 120 Ohm balanced cable (see Fig. 4)

All other capacitors: Ceramic disk types for 2.5 mm spacing.
All resistors for 10 mm spacing or smaller, (some resistors are mounted vertically).

Relay:	RS-12 V or RHD-12 V (National)
T 51:	J310 (Siliconix) or BF 246
T 52, T 53:	40841 or similar DG-MOS FET
I 51, I 52:	S042P (Siemens)
I 53:	HEF 4011 (due to speed, no alternative possible)
I 54:	LM324 (National Semiconductor)
I 55:	LM386 (National Semiconductor)
D 51, D 52:	1N4148, 1N4151
D 53:	C8V2 zener diode
D 54:	C3V3 zener diode
D 55, D 56:	1N4148, 1N4151
Crystal filter:	SSB, with carrier crystals type 9M22DI (Nikko Denshi) or XFM-9B (KVG)
L 51, L 55:	2 x 6 turns double-wound, approx. 0.3 mm dia. enamelled copper wire on toroid core R6, 3N30 (Siemens)
L 52 – L 54:	Special coil set type 5138 (blue/red/white)

Ceramic disk capacitors: 2.5 mm spacing
100 nF capacitors (2 pcs.): 5 mm or 7.5 mm spacing

Polarized capacitors: Tantalum electrolytics, drop type, 16 V

2 pcs. trimmer potentiometers 20 kOhm: round types, approx. 6 mm dia.

15 pcs. feedthrough capacitors for solder mounting, approx. 2.2 nF (value uncritical), short construction;

4 pcs. PTFE feedthroughs
1 metal case, 74 x 148 x 30 mm

Dr. Manfred Wieser, OE 7 WMI

A VFO with frequency-locked loop

The most critical part of a frequency-locked loop is the frequency-to-voltage converter. Conventional circuits such as (1), and (2) use RC or LC links for frequency discrimination and exhibit considerable disadvantages because of this with respect to temperature stability and/or characteristic slope. Based on an article in (3), experiments were made using a PAL-delay line as frequency discriminator. The result of these experiments is a continuously variable VFO of simple construction, whose stability is sufficient for applications in FM-systems up to and including the 70 cm band.

1. CIRCUIT

As can be seen in **Figure 1**, the output signal of the VCO (constructed according to details given in Figure [4]), is generated directly at the required frequency, after which it passes through a two-stage buffer amplifier. Approximately 20 mW (into 50 Ohm) are available at the output; a small part of the output power is tapped off and used to drive divider I 1. The division ratio of the subsequent dividers I 2 and I 4a can be programmed by disconnecting conductor lanes. The reset signals for the dividers, steep, negative pulses of the NAND-gate I 3 set the flipflop I 4b and also drive the delay line VZL. The signals at the output of the delay line are amplified in transistor T 4 and reset flipflop I 4b. The frequency information is now provided in the keying ratio of the output voltage of the flipflop; if this squarewave voltage is integrated, one will obtain a DC-voltage that is linear-proportional to the frequency. Since the saturation voltage of the TTL-output transistors is very temperature-dependent, a C-MOS analog switch I 5 is provided before integration.

The integrated squarewave voltage is compared to a (variable) DC-voltage. This is provided by operational amplifier I 6, which is used as comparator and integrator. The output voltage of this OP-amp. provides the control signal for the varactor diode D 1 of the VCO after further filtering. The antiparallel diodes D 2 and D 3 at the input of the OP-amp. reduce the transient time.

1.1. Operation of the Frequency/Voltage Converter

The frequency/voltage converter comprises the delay line (VZL), transistor T 4, and flipflop I 4b. Pulses at the input of the VZL appear at the output with a delay of 63.943 μs. Further pulses can be fed into the delay line before the first pulse has reached the output, and these are delayed by the same value. This principle can be used up to pulse frequencies of approximately 1 MHz.

Figure 2 shows the time plan at output Q of the flipflop for various input frequencies. In the case of frequencies whose even multiples are 1/63.943 μs = 15.64 kHz, the keying ratio will

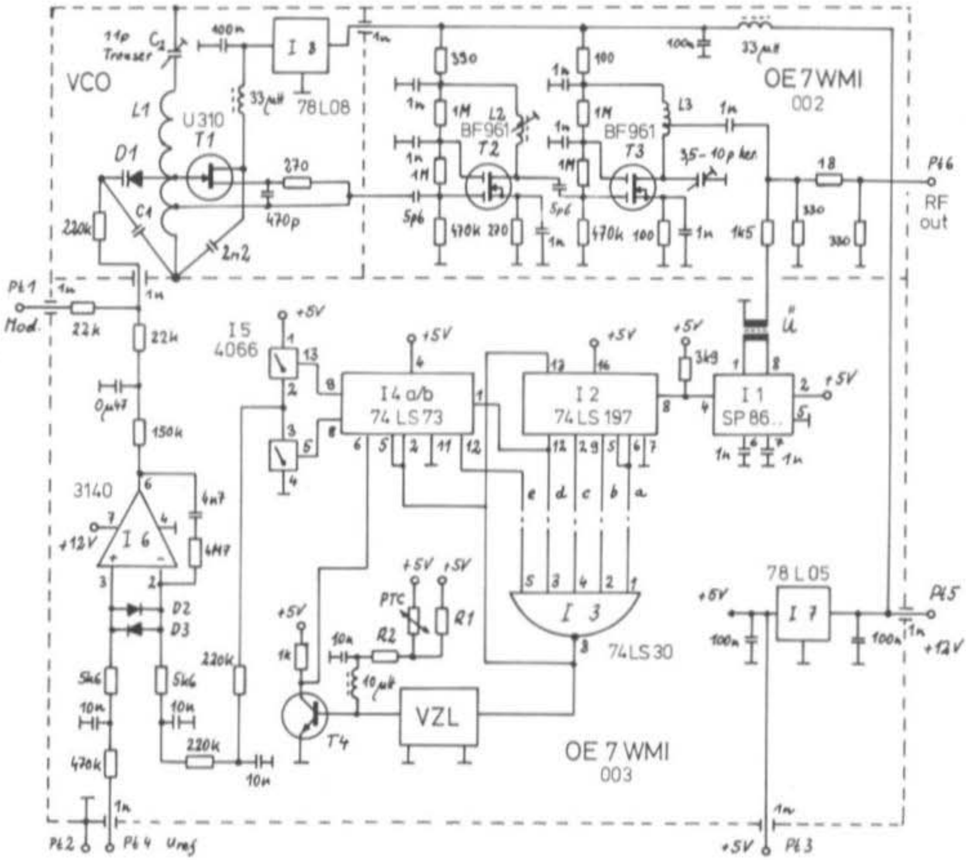


Fig. 1: VCO, Buffer amplifier and frequency/voltage converter

jump from 0 to 1 (or from 1 to 0). The variation range in which the keying ratio is clearly defined, thus amounts to 15.64 kHz; in practice, however, it is necessary for maximum and minimum keying ratios to be avoided for stability reasons (jumping into another frequency range). The theoretical variation range of the required frequency results from Δf = 15.64 x n (kHz) n . . . division ratio. If a certain output frequency is divided by Δf, i.e. $f/\Delta f$ = a, b, one will usually obtain a rational number. The figures behind the comma, when multiplied with the operating voltage b x U_{op} = U_{int}, will correspond to the DC-voltage from the frequency/voltage converter. The two subsequent final frequencies with which the division $f/\Delta f$ results in a whole number, are the theoretical corner frequencies:

$f_l/\Delta f$ = a, 0; $f_u/\Delta f$ = (a + 1), 0

An example for the 144 MHz band:

n = 170; U_{op} = 5 V, therefore
Δf = 170 x 15.64 kHz = 2658.62 kHz and
$f/\Delta f$ = 145000/2658.62 = 54.539
U_{int} = 0.539 x 5 V = 2.69 V

The corner frequencies can then be calculated as:

f_l = 54 x 2658.62 kHz = 143565 kHz and
f_u = 55 x 2658.62 kHz = 146224 kHz

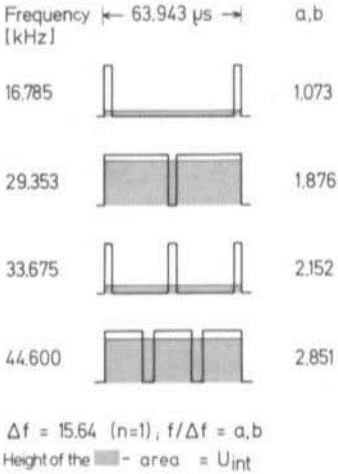


Fig. 2:
Various input frequencies generate different keying ratios, and finally integrated voltage values

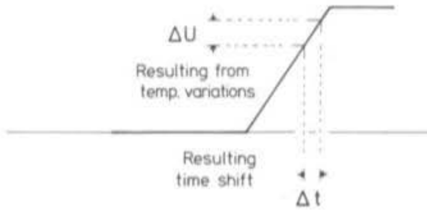


Fig. 3:
Flat slopes reduce stability

The frequency/voltage converter operates exclusively in the time domain, which means that it receives its information direct from the time plan of the input signal. For this reason, the steepness of the rise and fall slopes has a direct effect on the stability, as is shown in **Figure 3.** A good compromise between slope and current drain is provided by the use of low-power ECL, and low-power Schottky ICs. However, this limits the maximum VCO-frequency that can be processed to 180 MHz. Transistor T 4 is critical with respect to its temperature behaviour; since it is operated with a low collector quiescent current (90 µA), temperature variations effect a shift of the quiescent current by shifting the base-emitter voltage, which has drastic effects on the operating point: With increasing temperature, the pulse will become wider, the switching slope will be shifted in the time domain, and the frequency will drift upwards. This can be avoided by using a faster switching transistor, and using a PTC-resistor thermically coupled to the transistor in the base-current line.

This means that they have sufficient spacing to the limits of the 144 MHz amateur bands. The optimum division ratios for a number of common frequency ranges have been calculated with the aid of a computer (**Table 1**):

Band (MHz)	I 1	I 2 + 4a	Corner Frequencies (MHz)
144.0 – 146.0	:10	:17	143.565 – 146.224
133.3 – 135.3	:10	:17	132.930 – 135.589
135.0 – 137.0	:16	:11	134.870 – 137.622

2. CONSTRUCTION

The circuits of the VCO, buffer amplifier, and frequency/voltage converter shown in Figure 1 are accommodated in three chambers formed by the required screening panels; the VCO is built up without PC-board, and has therefore not been designated. The VCO and the two boards can be mounted in a metal case of 74 x 111 x 30 mm, see **Figure 4.**

The holes for the feedthroughs, or feedthrough capacitors are drilled on the side of the case, and in the two intermediate panels of 72 x 28 and 60 x 28 mm which are constructed from 0.5 mm tin plate. These holes have a diameter of 3.5 mm, and should be drilled with a spacing of 10 mm from the cover. A hole of 6 mm diameter should be drilled in the center of the other cover for alignment of trimmer C 2. The position of all holes can be seen in Figure 4 and in the photograph of the author's prototype given in **Figure 5.** After these preparations, the feedthrough capacitors are soldered into place and the case in fitted together.

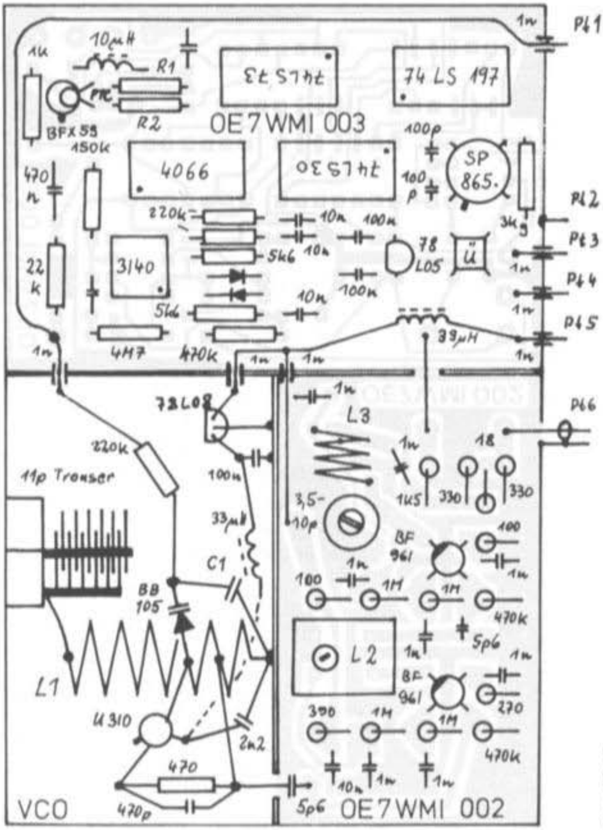


Fig. 4: Component locations for VCO, buffer (OE7WMI 002) and frequency/voltage converter (OE7WMI 003)

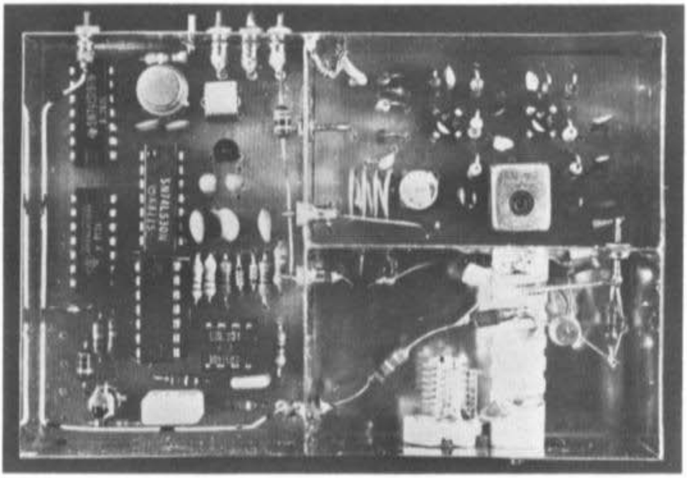


Fig. 5: Photograph of the author's prototype constructed according to Fig. 1 and Fig. 4. The delay line is to be found on the conductor side of the board.

The buffer amplifier is soldered into position with a spacing of 5 mm, and the digital part with a spacing of 12 mm from the base panel, and they are then soldered all around the board to the case. The constuction of the VCO can be made easily by comparing Fig. 4 and Fig. 5.

The previously calculated division ratio is programmed according to **Table 2** on PC-board OE7WMI 003.

	e	d	c	b	a
1	*	*	*	*	
2	*	*	*		*

etc. in dual code

	e	d	c	b	a
29				*	
30					*

The * means that the appropriate conductor lane must be disconnected.

Finally, the four adjacent connections of the delay line should be bent carefully close to the plastic case, (the two other connections are not required and can be disconnected), and the delay line can be soldered to the PC-board directly.

2.1. Special Components

T 1:	U310	
T 2,T 3:	BF961	
T 4:	BFX59 or BFY 90	
D 1:	BB 105	
D 2, D 3:	1 N 914 or 1 N 4148	
I 1:	According to frequency range or division ratio:	
SP 8655 B		1:32
SP 8657 B		1:20
SP 8659 B		1:16
SP 8660 B		1:10
I 2:	74LS197	
I 3:	74LS30	
I 4:	74LS73	
I 5:	4066 in a socket	
I 6:	3140 in a socket	
I 7:	78L05	
I 8:	78L08	
L 1:	Aged ceramic coil, 6 turns of 10 mm dia. or silverplated copper wire of 1 mm dia. wound on a glas rod of 8 mm dia.	
L 2:	3.5 turns of 0.4 mm dia. enamelled copper wire, using special coil set 5140500000, orange core	

L 3:	3.5 turns of 0.8 mm dia. silver-plated copper wire, wound on a 6.5 mm former
VZL	PAL delay line, e.g. Siemens AZ 1702, or AZ 1706
PTC:	Siemens P 270-C11, colour black
R 1, R 2:	see text, standard each 680 kOhm
C 1:	see text, for 144-146 MHz: standard 1 nF
Tr 1:	Double-hole core (Siemens B 62152-A7-X17) primary and secondary 3 turns, each of 0.2 mm dia. enamelled copper wire

3. ALIGNMENT

Firstly connect only the VCO and amplifier. The constant 6 V is now connected as bias voltage for the varactor diode. Adjust the frequency of the VCO with the aid of a frequency counter by aligning C 2 to the center of the band; the two circuits of the buffer amplifier are aligned for maximum output power (20 to 30 mW). The value of capacitor C 1 and the coupling point of the varactor diode determine the variation range of the VCO. It must be less than the theoretical variation range, since otherwise the frequency in the vicinity of the corner frequencies could jump into another frequency range. For this reason, C 1 should be varied while observing the frequency counter until one is within the variation range even at maximum variation of the diode voltage (O V to U_{op}).

After connecting the control loop (varactor diode is connected to the output Pt 1 of the digital portion), the VFO will be ready for operation if the previously mentioned adjustments had been carried out correctly. However, it is advisable to check with a frequency counter to see whether the VFO jumps to another frequency range on varying the reference voltage.

Now a word regarding the temperature compensation of transistor T 4: The PTC-resistor is bent over transistor T 4, and thermically coupled to it with the aid of heat-conductive paste. The increase of the parallel (R 1), and decrease of the

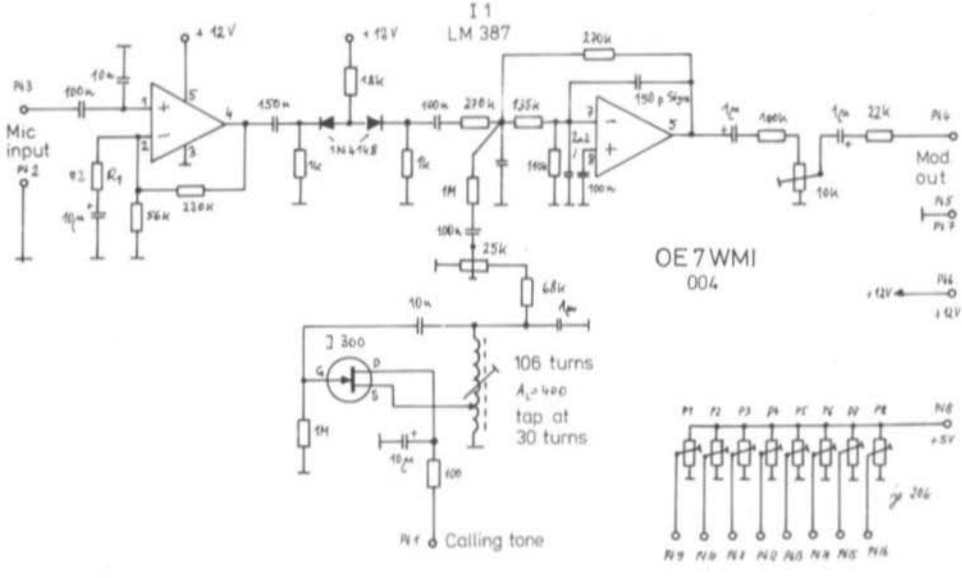


Fig. 6: The FLL-VFO can be used as FM-transmitter using this simple modulator and calling-tone generator

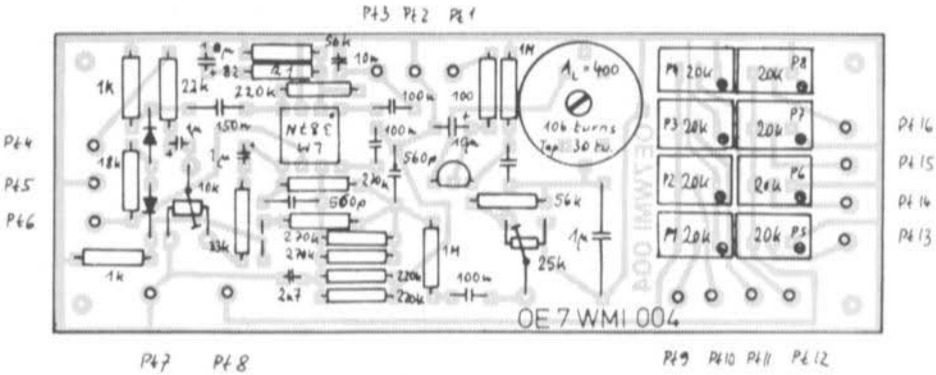


Fig. 7: The single-coated PC-board for modulator and calling-tone generator OE7WMI 004

series resistance (R 2) operate against the temperature drift of the transistor. A value of 680 kOhm has been found as optimum value for R 1 and R 2 in several prototypes.

The author would like to point out to a difficulty that was encountered with one prototype: This prototype exhibited a noise as interference on the modulation. The cause of this was a strong noise generated in the stabilizer 78L08.

4. ACCESSORY MODULES

4.1. Modulator

It is possible to use the VFO both as local oscillator in a receiver and as an oscillator in FM-transmitters. **Figure 6** shows a modulator and calling-tone generator for the latter application. Both circuits, as well as 8 trimmer potentiometers for programmable frequencies are accommodated on board OE7WMI 004 (**Figure 7**). The circuit does not offer any special features, both construction and alignment are easy; it is only necessary to align the frequency deviation limiter and calling-tone level. If the microphone gain is too low, this can be increased by reducing the value of R 1.

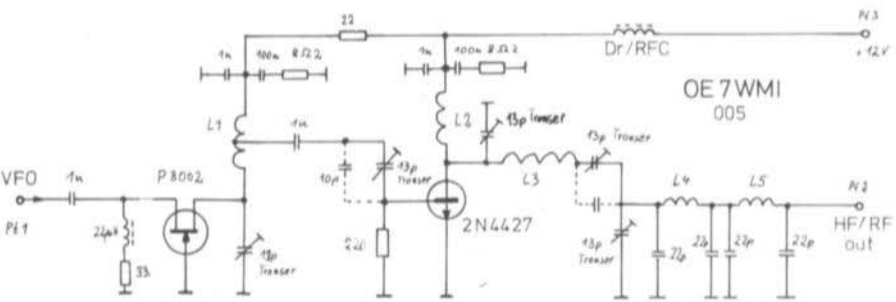


Fig. 8: This VHF-amplifier with lowpass filter amplifies the transmit power to 1 W

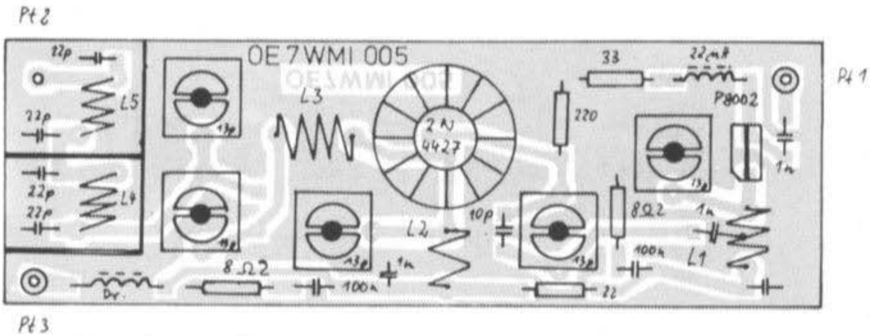


Fig. 9: The single-coated PC-board for the transmit amplifier OE7WMI 005

4.2. Transmit Amplifier

The circuit of a VHF-transmit amplifier (OE7WMI 005) with lowpass filter and an output power of 1 W is given in **Figure 8**. This PC-board can be accommodated in an additional metal case. The construction of this module can be seen in **Figure 9**. The alignment is simple: The five trimmer capacitors should be aligned for maximum power at the center of the band.

4.2.1. Special Components for OE7WMI 005

L 1: 3 turns of 1 mm dia. silver-plated copper wire, wound on a 6 mm former, coil tap at the center;
L 2: 3 turns of 1 mm dia. silver-plated copper wire, wound on a 6 mm former;
L 3: 4 turns, otherwise as L 2
L 4, L 5: 4 turns of 0.8 mm dia. enamelled copper wire, wound on a 5 mm former
Metal case: 3711130

5. OPERATING AT HIGHER FREQUENCIES

It is not possible to use the described design without change for higher frequencies, such as 430 to 440 MHz. The metal case is not stable enough, which means that frequency variations due to thermal or mechanical variations of the case cannot be completely compensated for due to the finite loop gain. Frequency errors will remain that are not permissible, even in FM-systems.

There are two ways of using the VFO for higher frequencies:

Either one can use a case with thicker side panels such as cast aluminium cases which allow the VFO to oscillate directly at the required frequency, or one can use a frequency multiplication. If the 2 m-band is to be avoided, one can use the frequency range 215 to 220 MHz as VFO-frequency.

Both types require a divider having a higher cutoff frequency (unfortunately also higher current drain) in the digital circuit. For this reason, the divider SP 8515 is used in the circuit of OE7WMI 006 (see **Figure 10**). The programming and construction are, otherwise, identical to that of OE7WMI 003, and it is only necessary to use a stabilizer 7805 with its higher rating. This can be directly connected to the case next to the delay line to provide better cooling, or it can be soldered into position there. **Figure 11** shows PC-board OE7WMI 006 that was developed for this application instead of board 003.

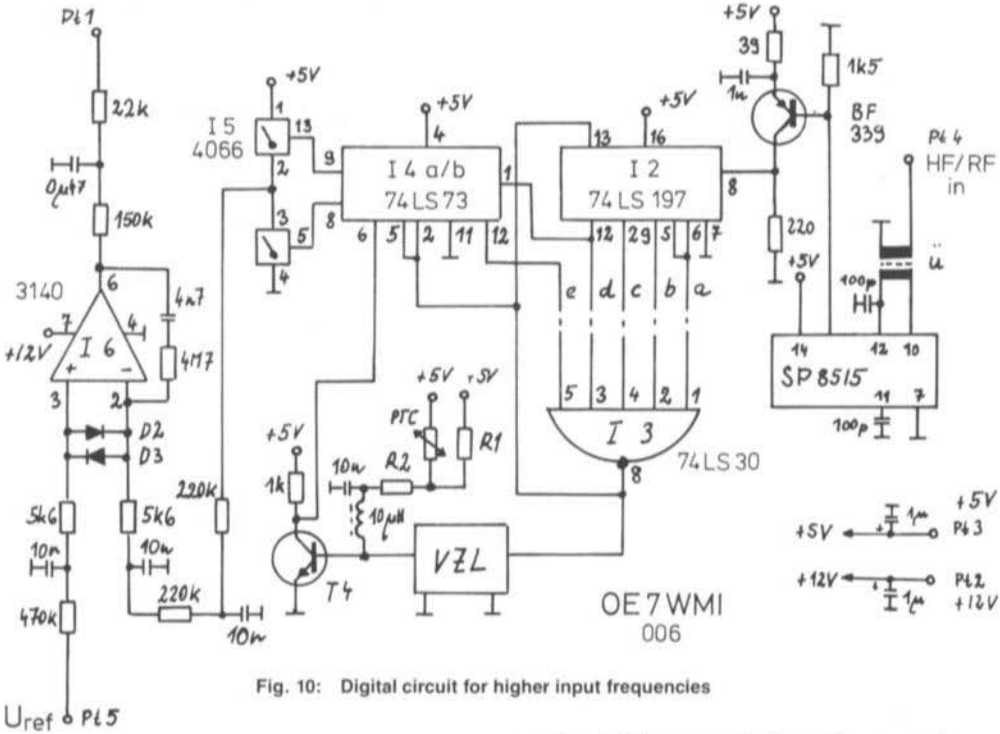


Fig. 10: Digital circuit for higher input frequencies

6. FURTHER APPLICATIONS

The FLL-VFO is also suitable as inexpensive solution for stabilizing frequencies in many applications. Several possibilities that have been examined with success by the author are to be mentioned briefly:

One can use the same VFO without large modifications for transmit and receive if the same division ratio results for both frequencies (e.g. 144 to 146 MHz and 133.3 to 135.3 MHz). The switching of the frequency ranges can be obtained using

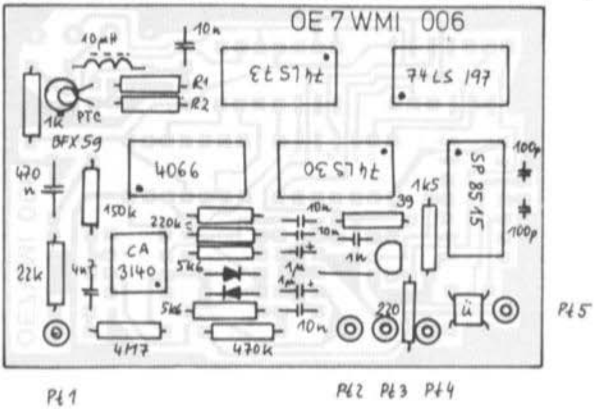


Fig. 11:
The single-coated PC-board OE7WMI 006 for a frequency/voltage converter with a higher input frequencys

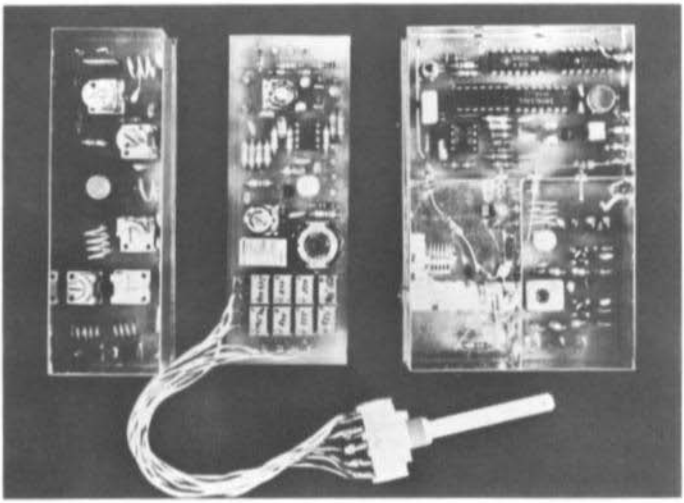


Fig. 12: FLL-VFO with modulator, calling-tone generator and 8 variable fixed frequencies, as well as a transmit-amplifier for the 144 MHz band

an additional capacitance and an RF-switching diode in the VCO. If the reference voltages are also switched at the same time (with the aid of a C-MOS analog multiplexer 4066), one will have obtained the whole frequency processing for both transmit and receive, which will form the basis of an inexpensive FM-transceiver (**Fig. 12**).

If different division ratios are required for transmit and receive, one can use an additional digital switching (AND/OR) at the inputs of I 3 as a simple solution.

Or course, one can also use reconversion methods even with a delay line-VFO. In this manner, one could save the ECL-divider and could use available crystals, since one is relatively versatile in the selection of the conversion frequency. Reconversion will also improve the overall stability, providing that one uses a stable crystal.

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Erwin Schaefer, DL 3 ER

A Stripline GaAs-FET Preamplifier and Mixer for the 10 GHz Band complete with IF-Preamplifier, Image Frequency Filter, and Power Supply.

Part I

GaAs-FET preamplifier and mixer for the 10 GHz band in stripline technology complete with IF-preamplifier, image frequency filter, and power supply.

The following article is to describe the result of a large number of experiments with components for the 3 cm band in order to provide suggestions for stripline preamplifiers and mixers, thus allowing an alternative to straight-through mixers. The article is not to describe the hardware down to the last detail, but is more a collection of experiment results and will include many tips and aids to design. In order to indicate the information that is to be given, the article is to be commenced with an index.

1. STRIPLINE HYBRID MIXER FOR 10 GHz

1.1. General Details

The idea for this article was based on publications describing such equipment for lower frequencies (1.2 and 2.3 GHz) in VHF COMMUNICATIONS, and whether these circuits could also be used on 10 GHz now that suitable mixer diodes having low noise figures are available for this application (4). The experiments were made exclusively using Schottky diodes type BAT 14-073, 14-083, and 14-093 (see **Figure 1**), which are manufactured by Siemens. According to the data sheets, single-sideband noise figures of between 5.5 and 6.5 dB are possible. These values require an IF-noise figure of approximately 1.5 dB.

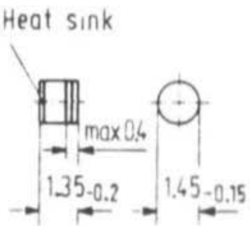


Fig. 1:
Construction of the 10 GHz mixer diode BAT 14-073

The results of the experiments confirmed the values given in the data sheets. With the exception of a calibrated, professional semiconductor noise source, no special measuring equipment was required. Only those aids were used that any serious microwave amateur will usually have available, or will have access to. With the exception of the noise generator, the author did not need to loan out any equipment (QRL).

1.2 Noise Figure Measurements

By the way, the author also uses a home-made noise source for the 10 GHz band, that was calibrated by comparing it to a professional noise source. Since this may be of interest to other amateurs, the main features are now to be given:

The main component is a conventional detector probe in a waveguide type R 100 (WR 90) where a diode 1 N 23C is driven into its blocked range via a resistor of approximately 10 kOhm and a stabilized voltage of approximately 10 V. The diode was selected for maximum noise power. A circuit as described in (9) and (11) (current injection via FET) would be more suitable. The calibrated noise power is 14 dB ENR.

All noise generators using this technology have one thing in common and that is that the generated noise power will vary when an RF-power of more than 0.5 mW is injected to the noise diode. This means that the calibration will no longer be correct. It is possible that an additional directional coupler or circulator may be able to suppress this effect. Absolute measurements on straight-through mixers, or mixers with a low suppression of the oscillator frequency can be problematic when not using the previously mentioned aids, and can only be used for orientation.

By the way, the noise source constructed by the author is also used in an automatic noise figure measuring system (9) with success. It allows the ratio (S+N)/N to be determined clearly.

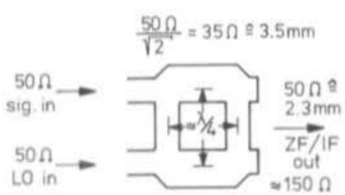


Fig. 2:
Hybrid ring for 10.25 GHz

1.3 Design of the Mixer

The design of the ring hybrid mixer was made in a similar manner to (4) and (10). The principle of construction is shown in **Fig. 2.** The following material was used for the PC-board:

RT/Duroid 5870 having:

E_r = 2.35 and
d = 0.79 mm

This results in a conductor lane width of approx. 2.3 mm for the two 50 Ohm branches and a conductor lane width of approx. 3.5 mm for the two 50 Ohm/$\sqrt{2}$ branches. According to the equation given in (7)

$$E_{eff} = 1 + (E_r - 1)\left[\frac{1}{2}\left(1 + \frac{1}{\sqrt{1 + \left(\frac{10}{w/h}\right)}}\right)\right]$$

the velocity factor is:

$$V_p = \frac{1}{\sqrt{E_{eff}}} \sim 0.7$$

The length of the square ring results as 5.1 mm with $\lambda/4_{10.25\,GHz}$ after taking E_{eff} and V_p into consideration. However, 4.5 mm was selected in order to extend the $\lambda/4$-length somewhat into the conductor lane (bandwidth).

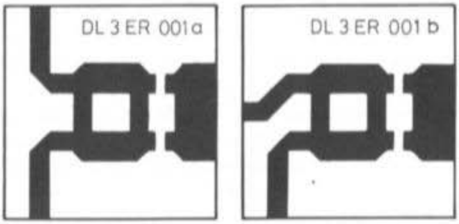


Fig. 4:
PC-board of the hybrid ring mixer;
Left: for connection to semirigid cable,
Right: for waveguide mounting

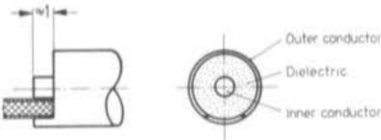


Fig. 5:
Mounting of semirigid cable (RG-141) to microstrip boards

Figure 3 shows all dimensions of the PC-board, and **Figure 4** shows two different versions according to whether the receive signal is to be extracted using a coupling pin directly from the waveguide, or via semirigid cable. The oscillator frequency is fed in using semirigid cable in both cases. This cable can be soldered to the board virtually without mismatch when soldered as shown in **Figure 5.**

The design of the pin probe and the mounting of the mixer board on the waveguide are indicated in **Figure 6.**

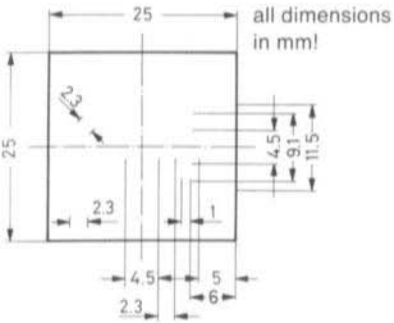


Fig. 3:
Dimensions of the 10.25 GHz hybrid ring mixer

The two mixer diodes are soldered into place quickly, without using too high a soldering-iron temperature. The lowpass filter for the IF is obtained as capacitance on the PC-board, and it also represents a $\lambda/4$-line of low impedance. The IF-preamplifier is directly, capacitively coupled to the output of the mixer.

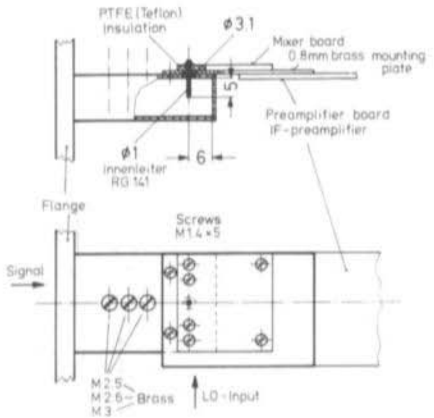


Fig. 6:
Mounting and coupling of a mixer board to R 100 (WR 90) waveguide

The crystal-controlled oscillator frequency of 10.368 GHz is obtained by multiplying the output frequency of a 1152 MHz oscillator by nine. A 3-stage filter is provided at the output. The signal purity is monitored during the experiments using a 20 dB coupler connected to a spectrum analyzer, since frequency multipliers having a high frequency modulation factor can be critical. The local oscillator power amounts to approximately 10 mW, and can be adjusted with the aid of an attenuator.

A home-made IF-amplifier is used for the input circuit of the intermediate frequency at 144 MHz. This amplifier must have a good linearity range of at least 20 dB with the AVC switched off. The AF-output power is measured with a thermometric power meter (HD 434 A). The noise generator has already been mentioned.

1.4. Measured Values

1.4.1. Receive Mixer

f_0 = 10.368 GHz
IF = 144 MHz
f_{in} = 10.224 GHz

Oscillator power saturation from approximately 3 mW; sensitivity loss below approx. 2.5 mW.

Noise figure:
3–3.5 dB (double-sideband)
6–6.5 dB (SSB with 10.224 GHz filter, see 3.)

Suppression of the oscillator frequency approx. 12 dB, whereby any unpaired diodes of the given type were used; (**Figure 7**).

The given measuring values were achieved with both types of construction (board 50/50 Ohm, and with probe coupling to the waveguide).

When using the waveguide construction, the minimum noise figure could only be obtained after alignment of the matching screws on the signal side.

1.4.2. Transmit Mixer

The local oscillator signal was fed in with the power of approximately 10 mW at 10.368 GHz. The IF-power at 144 MHz amounted to approximately 5 mW. Approximately 0.5 mW SSB-power was measured at 10.224 GHz.

The efficiency is most certainly not optimized. No further experiments were made to further optimize the circuit, however, later experiments have indicated that it is possible to reduce the size of the previously large, narrowband frequency oscillator chains.

2. IF-PREAMPLIFIER

In order to ensure that the noise figure of the mixer is not deteriorated after taking the conversion loss into consideration, it is necessary for the subsequent IF-preamplifier to possess a high gain and a low noise figure.

A wideband amplifier described in a Siemens application sheet (**Figure 8**) equipped with a low-cost BFT 66 is able to fulfill these demands. The

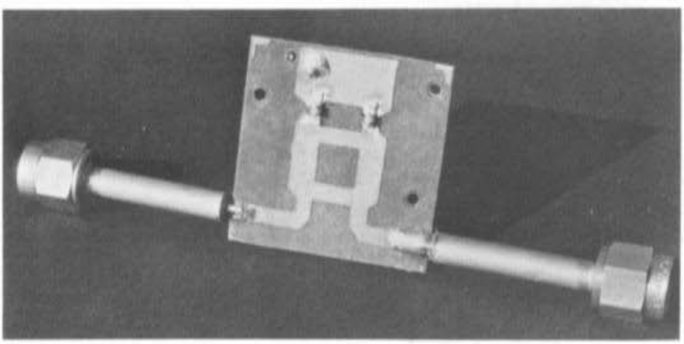


Fig. 7: A prototype 10 GHz hybrid ring mixer using two BAT 14-083 F

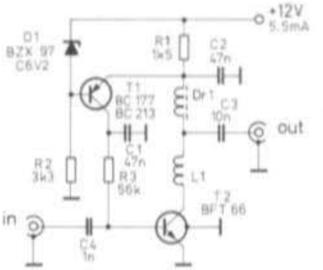


Fig. 8:
Low-noise preamplifier for 30–150 MHz
L 1: 4 turns of 0.3 mm enamelled copper wire wound on a 4 mm former, self-supporting
RFC 1: Ferrite choke 2–3 µH, e.g. 5 turns of enamelled copper wire on a ferrite bead

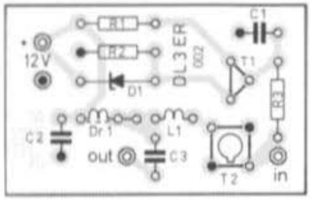


Fig. 9:
Double-coated PC-board for the wideband IF-preamplifier (approx. 30 to 150 MHz)

capacitance and inductance values have been changed somewhat in order to limit the frequency range. The electrical values obtained are:

Gain = 15–20 dB
Frequency range: = 30–150 MHz
Noise figure: approx. 1.5 dB

The given operating frequency range allows the common intermediate frequencies of 30 MHz and 100 MHz often used for the X-band to be covered.

The output impedance of the mixer is in the order of 150 to 300 Ohm. This is listed as a common value for Schottky diodes, which will also be affected by the oscillator power. It is necessary that the signal level is small with respect to the oscillator power.

The direct connection of the IF-preamplifier to the mixer provided good measuring results which means that an input matching was not required. An attempt to improve matching using a variable transformation link and taking the S-

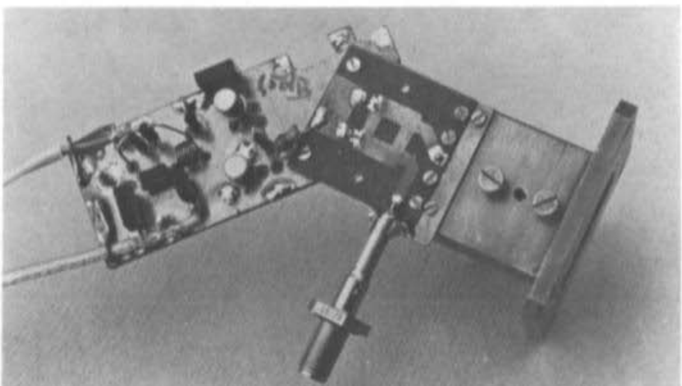


Fig. 10:
Microstrip mixer with waveguide injection and IF-preamplifier (author's prototype)

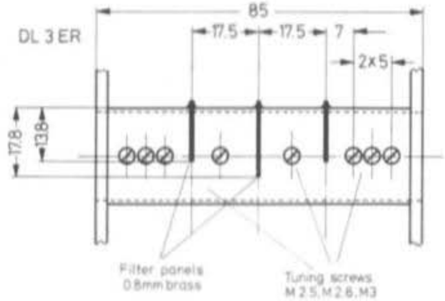


Fig. 11:
Dimensions of a two-stage waveguide filter for 10 GHz

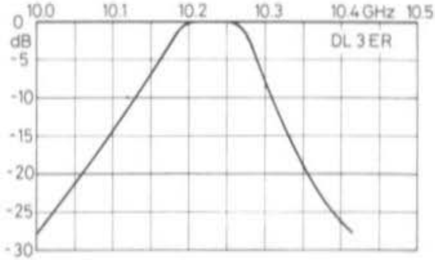


Fig. 12:
Passband range of the filter described in Fig. 11.

parameter of the BFT 66 into consideration, resulted in a hardly noticeable noise figure improvement. However, if a coaxial cable is to be connected between mixer and preamplifier, the noise figure will be deteriorated considerably even if this is only a few centimeters in length.

The amplifiers are built up on a 1.5 mm thick PC-board of 40 mm x 25 mm. This double-coated PC-board is designated DL 3 ER 002, and all components are mounted on the ground side of the board (**Figure 9**). Suitable counter-sinks should be made – using a drill – around the holes for insulation of non-grounded components. The transistor BFT 66 is soldered into position on the conductor side of the board. This facilitates removal later, if required; no tendency to oscillation was observed. The case and the emitter connection of the BFT 66 were through-contacted to the ground side.

3. TWO-STAGE WAVEGUIDE FILTER FOR 10 GHz

Several filters were required for the experimental construction and for carrying out the measurements. They should be easy to construct and are easily reproducible. The construction of this filter originates from Max Münich, DJ 1 CR, and is based on a professional prototype.

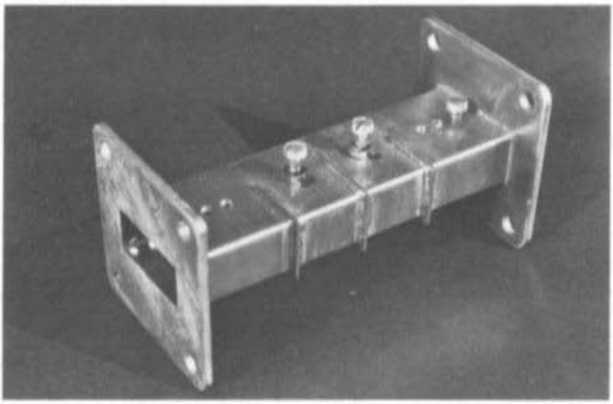


Fig. 13:
Photograph of a completed two-stage filter

Figure 11 shows virtually all important details. The waveguide (R 100, WR 90) is cut with a circular or hand-saw to the given dimensions. The width of the cut should correspond exactly to that of the panels to be inserted in order to ensure that these fit tightly. They are finally soft-soldered together with the two connection flanges (heat up on an electric cooker, or Butan-gas flame). The author used a conventional soldering fluid comprising hydrochloric acid/zink filing solution. This flux can be removed more easily by intensive washing with hot water than the flux of conventional solder.

The measured values are shown in **Figure 12**, which were obtained using a simple power measurement (Gunn oscillator, absorption wavemeter, directional coupler at the input, as well as microwattmeter at the output).

The insertion loss in the passband range is in the order of approximately 0.5 dB. The filter (**Figure 13**) has not been plated galvanically. The filter is easily tunable with the aid of the tuning screws and their counter-nuts. The input and output of the filter are provided with the usual three screws for tuning and have springs to maintain the adjustment; when higher demands are to be placed on the stability, counter-nuts can be used. The filter has satisfied all demands placed on it in practice.

Friedrich Krug, DJ 3 RV

Versatile IF-module suitable for 2 m Receivers, or as an IF-module for the SHF Bands

Part V: Description of the IF-amplifier module DJ3RV 002 and BFO-module DJ3RV 004

This part of the description describes the heart of the IF-module. This IF-amplifier is able to handle signals at low distortion over a dynamic range of more than 100 dB.

It is advisable to describe the BFO-module at this point since its signals can be used for alignment of the modules that have been described already.

The next edition will describe the demodulator module, and give details regarding the interconnection of all modules, as well as recommendations of a suitable power supply and AF-amplifier.

4.2.2. IF-Module DJ 3 RV 002

PC-board DJ 3 RV 002 is equipped with a double-notch filter and a controlled IF-amplifier with AGC voltage generator and connection for an S-meter.

The notch filter is mainly provided when using the IF-module in a shortwave receiver; interference carriers that must be suppressed with a notch filter are hardly present on the VHF, UHF, and microwave bands. The components on the PC-board are arranged so that the notch filter can be deleted. In this case, the IF-amplifier remains fully operational, and could be then installed in a metal case having dimensions of 74x111 mm.

Circuit Description

Figure 44 gives the circuit diagram of the module, whose operation was described in detail in part 3 (VHF-COMMUNICATIONS 3/1982). The input signal is fed in via a coaxial connector from the crystal filter module and is passed via a relay to the notch filter, or directly to point Pt 20 on the PIN diode attenuator of the IF-amplifier.

The notch filter possesses an amplifier at the input equipped with T 1 and T 2b, which compensates for the insertion loss of the filter, and the source follower T 2a and T 3. The filters can be aligned separately with the aid of varactor diodes D 4 and D 5. This has the advantage that two different interference signals can be filtered out. Furthermore, it is very difficult to achieve an exact tracking even when using selected components.

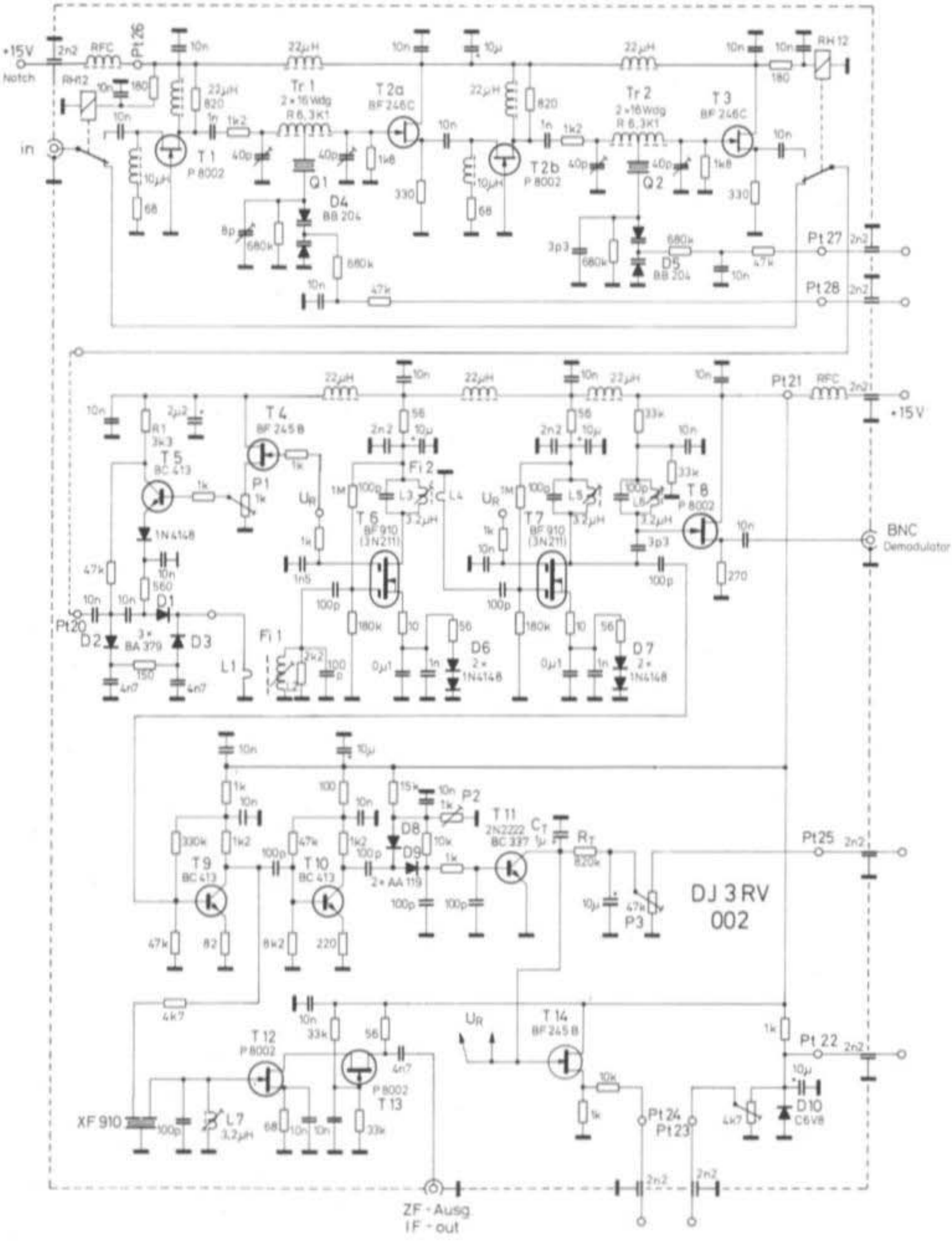


Fig. 44: Controlled IF-amplifier with double notch filter

The IF-amplifier corresponds to the circuit diagram given in Figure 13 with the exception of three modifications. In order to achieve a better decoupling, an additional 22 µH choke was placed in the power supply line between T 7 and T 8. The 22 kΩ resistor parallel to L 3 can be deleted. The critical stability in the control behaviour encountered with the first prototype when not using this resistor was not noticed when constructing later prototypes. The third modification is due to a drawing error in Figure 13: The 1 nF bypass capacitor between the emitter of T 5 and diode 1 N 4148 to ground is drawn at the wrong position. It should be between diode 1 N 4148 and the 560 Ω resistor, otherwise large intermodulation distortions will be caused. The value of the bypass capacitor was also increased to 10 nF. The author would like to thank DK 5 LV here for the extensive measurements.

Components

The details given in section 4.2.1. are also valid for the selection of components for this and for the subsequent modules.

The inductances are all built up using the special filter set D 41-2165, colour: orange, after removing the center pins that do not fit into the holes on the board. They can be removed easily with the aid of tweezers.

L 1 + L 2:	3.5 turns + 17.5 turns, approx. 0.2 mm dia. enamelled copper wire
L 3 + L 4:	17.5 turns + 4.5 turns, approx. 0.2 mm dia. enamelled copper wire
L 5:	17 turns, approx. 0.2 mm dia. enamelled copper wire
L 6:	17.5 turns, approx. 0.2 mm dia. enamelled copper wire
L 7:	17 turns, approx. 0.2 mm dia. enamelled copper wire
Tr 1, Tr 2:	2 x 16 turns of 0.2 mm dia. enamelled copper wire twisted together and wound on a toroid core Siemens R 6.3 K 1

Mounting the Components

Figures 45 and 46 give the components location plan, and a photograph of the author's prototype.

The prototype board is double-coated, but does not possess through-contacts, which means that the ground points of the components marked in the component location plan must be soldered at both sides of the board.

The mechanical work should be made firstly, and should be executed according to the details given already in Section 4.2.1. When installing the board into a 30 mm high case, the spacing between base and surface of the PC-board should amount to approx. 4.5 mm.

After this, it is possible for all components to be mounted on the PC-board with the exception of the connection of the input connector. The source resistors of the FETs T 1, T 8, and T 12 should be selected so that the transistors are operated at a slope of approx. 20 mS. The values given in the circuit diagram for the source-resistors only serve as orientation values. In order to measure the transistors, the details given in the previous section should be observed. The author used all those FETs for modules DJ 3 RV 002 to 004 that were not paired together for module DJ 3 RV 001.

If the transistors type BF 910 (T 6 and T 7) are sunk into the board, it is necessary for the drilled-out ground connection to be replaced by a wire bridge on the conductor side, and this is indicated as a dashed line in the component location plan. Otherwise, the IF-amplifier will oscillate!

Preparations and Alignment

The author has used the following "check list" for the preparations and alignment:

Firstly switch on the IF-amplifier without notch filter, and continue in the following sequence:

- Dampen the input of the PIN-attenuator (Pt 20) with a 56 Ω resistor to ground with no signal fed to the input
- Place the wipers of potentiometers P 1 and P 3 to ground Adjust P 2 to null Ω.
- Terminate the demodulator output with 50 Ω.
- It is now possible for the operating voltage of + 15 V to be connected to Pt 21. It is advisable to use a power supply with an adjustable current limiting and to increase this slowly towards higher current values. The current drain should amount to approximately 75 mA.

If it differs greatly from this, a fault will be present in the circuit, or an incorrect operating point will exist for T 8 or T 12. It is easy to establish whether the amplifier is oscillating with the aid of an oscilloscope or millivoltmeter connected at the output to the demodulator, and at the IF-output. If this is the case, a ground fault will exist such as a forgotten feedthrough connection.

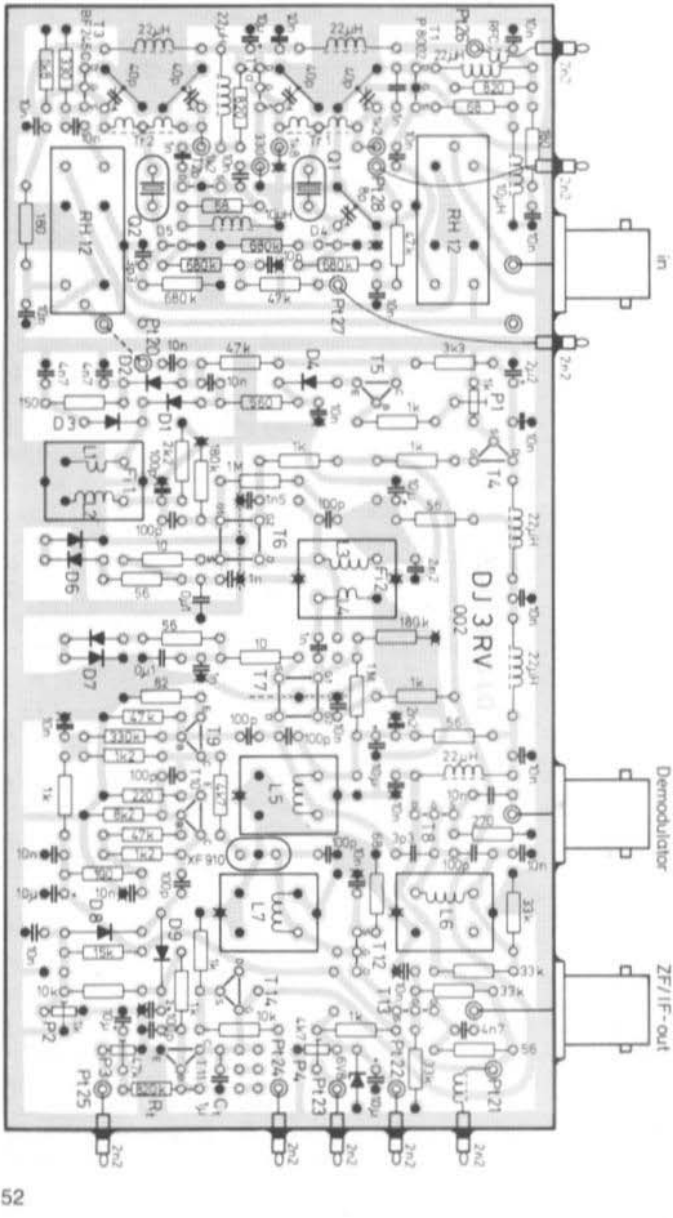


Fig. 45: Double-coated PC-board DJ 3 RV 002 with component locations. The positions marked with crosses show points where through-contacts must be made. The PC-board allows various circuits to be made, which will be discussed at the end of this article.

- Check that approx. 6.8 V are present at Pt 22 and that Pt 22 is connected to Pt 25 using a wire bridge outside of the case.
- Adjust P 3 so that a voltage + 5.6 V is present at the wiper (10 μF capacitor). All voltages should be measured at high impedance using a voltmeter with ≧ 1 MΩ!
- P 1 should be adjusted so that a voltage of + 4.8 V is present at the collector of T 5. Approximately + 3.1 V will then be present at the emitter of T 5. The operating current at Pt 21 will then amount to approx. 100 mA.

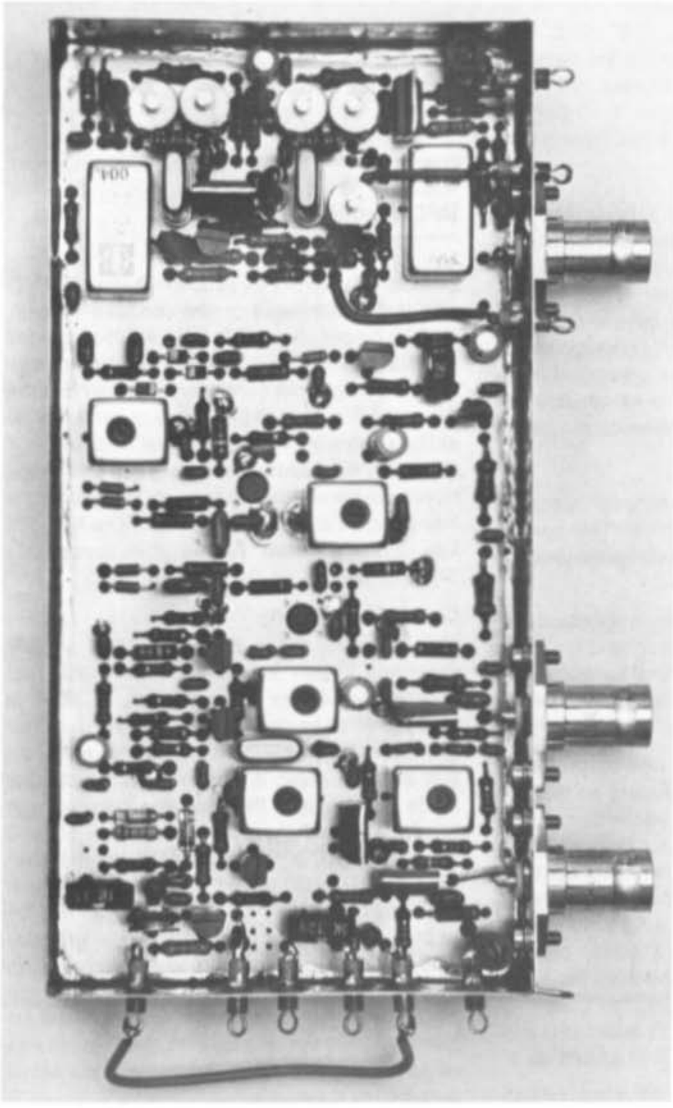


Fig. 46: Photograph of the author's prototype module DJ 3 RV 002 showing the component layout

- Remove the 56 Ω resistor connected to Pt 20 and directly connect this point via a wire bridge, or direct to the input socket. Feed a 9 MHz signal at a level of – 100 dBm, and align inductances L 1 to L 6 for maximum level at the demodulator output. The cover on the conductor side of the board should be in place during this alignment.
- The level at the input should now be increased to approximately – 60 dBm, after which the level at the output to the demodulator is aligned with P 2 to 10 mV_{rms} (28 mV_{pp}). The level behaviour shown in Figure 16 should be present when the input signal level is varied.
- The alignment of filter XF 910 is made with the aid of L 7 to obtain the best passband curve. This is made by sweeping the input signal (frequency deviation < 100 Hz). In order to ensure that the control operation does not falsify the shape of curve, the signal should be below the level of the control threshold, or the control should be slowed down by connecting a tantalum electrolytic of 10 μF in parallel to C_T.

After this, the IF-amplifier is ready for operation with the exception of the S-meter. This can be aligned only together with the complete receiver as was described in section 3.3.4.

In order to align the notch filter, it is necessary for the IF-amplifier to be switched off and the input connector connected according to the wiring plan. The output of the filter in front of point Pt 20 should be terminated with 50 Ω.

It is necessary for the notch filter to be slowly swept during the alignment process so that the transient time is known. An oscilloscope with storage tube is very suitable for displaying the output signal. Since most amateurs do not have such an instrument, it is only possible to carry out this measurement using a point-for-point measurement. The alignment signal can be taken from the crystal oscillators of the BFO-module DJ 3 RV 004, by pulling the frequency with the aid of the trimmers. This board also provides a reference voltage for Pt 27 and Pt 28.

It is necessary for each filter to be aligned individually. This is achieved by removing the coupling capacitors and bridging each stage. The alignment should be made at the center of the band with the aid of the 20 pF trimmer, and the 40 pF trimmers are used to align a symmetrical notch. A voltage variation range from + 1 V to + 20 V at Pt 27, or Pt 28 resulted in a pulling range of 2.2 kHz in conjunction with the crystal XF-901, however, the symmetric behaviour of the notch deteriorates at the band limits.

The current drain at Pt 26 should amount to approx. 100 mA.

4.2.3. BFO-Module DJ 3 RV 004

PC-board DJ 3 RV 004 accommodates the BFO with three switchable crystal oscillator circuits, and the output stage. This module also provides a swept oscillator for 9 MHz equipped with a low-frequency sawtooth generator designed for slow sweeping. This swept-frequency generator is an aid for alignment of the crystal filter circuits and is especially provided for those readers that do not have such measuring equipment. This part of the board can be cut off later and the BFO will then fit into a metal case having the dimensions 74 mm x 111 mm.

Circuit Description

The operation of the BFO-circuit was already described in part 3 (VHF COMMUNICATIONS 3/1982). An output level of max. 0 dBm is required when using it together with the demodulator board DJ 3 RV 003. As can be seen in the circuit diagram given in **Figure 47**, the Schottky diode at the gate of the oscillator transistor can be deleted, and the output amplitude aligned with the aid of C 3. The value of C 3 was in the order of 33 pF to 150 pF in the various prototypes. It is also possible for the voltage stabilizer REF 01 to be replaced by a pass transistor with zener diode. However, even these component-saving measures do not deteriorate the quality of the signal. However, if the circuit is to be used for intermodulation measurements, these measures should not be used since the carrier noise would then be too great.

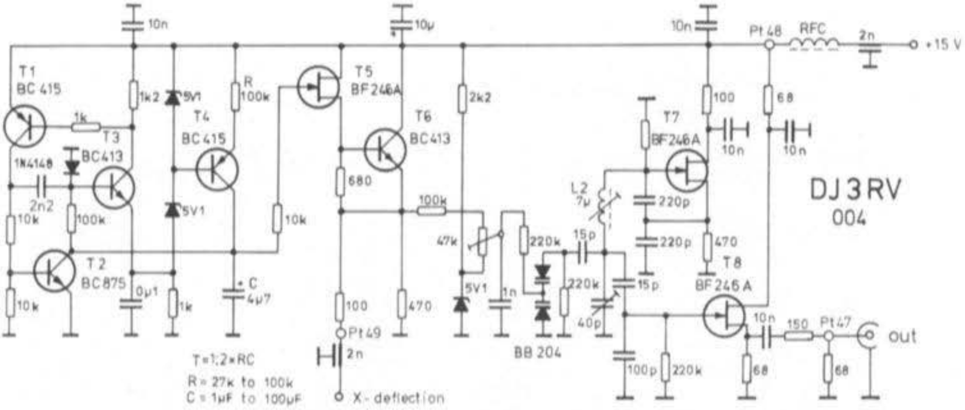


Fig. 47a: **A swept-frequency oscillator as alignment aid for module DJ 3 RV 004**

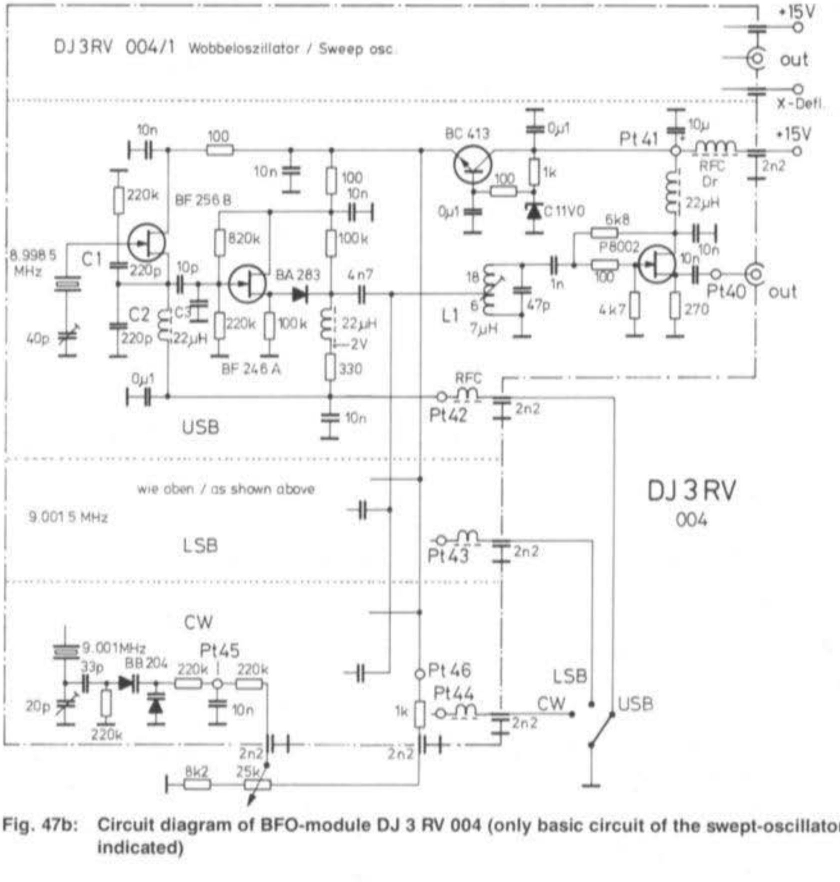


Fig. 47b: **Circuit diagram of BFO-module DJ 3 RV 004 (only basic circuit of the swept-oscillator is indicated)**

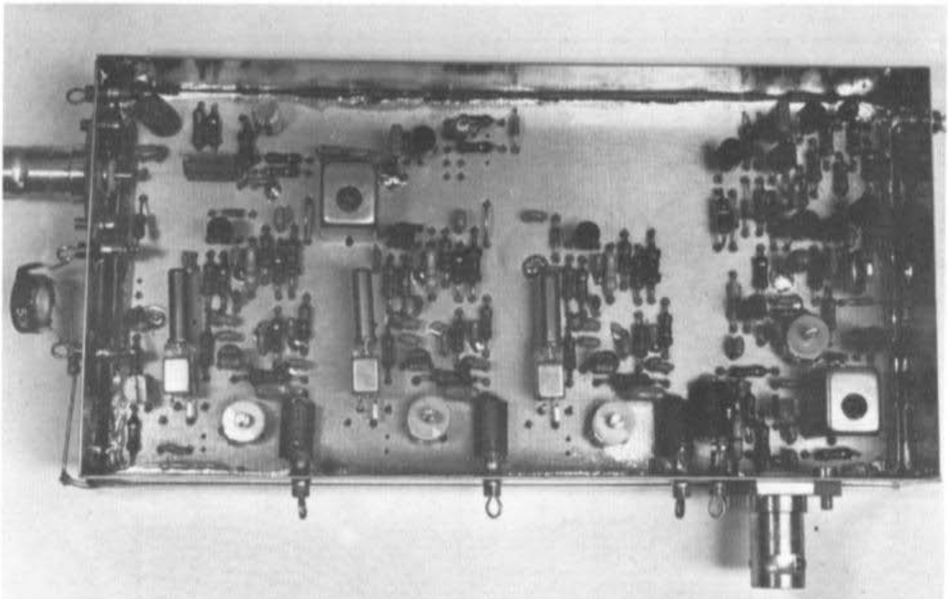


Fig. 48: Photograph of the author's prototype DJ 3 RV 004 showing the simplified voltage stabilization

The circuit of the swept-frequency oscillator does not possess any special features, and is very similar to that of the crystal oscillators.

The 9 MHz signal is fed via a source follower and an attenuator and is coupled out at a level of approx. − 20 dBm into 50 Ω. This level will not overdrive the crystal filter stages.

The sawtooth generator is built up with discrete components. Capacitor C is charged from a current source via R, zener diode C5V1, and transistor T 4 until transistor T 3 conducts, which then discharges capacitor C via T 1 and the Darlington transistor T 2. Transistors T 3, T 1, and T 2 are then blocked again, and capacitor C will be charged again. The sawtooth voltage is coupled out at low impedance with the aid of transistors T 5 and T 6. The sweep deviation can be varied using the 47 kΩ potentiometer.

Components

L 1: 7 μH, 18 + 6 turns of approx. 0.2 mm dia. enamelled copper wire in special coil set D 41-2165, colour/orange

L 2: 7 μH, 25 turns, otherwise as L 1.

Construction Details

As can be seen in **Figure 48,** the PC-board can be installed in a 30 mm high metal case. This means that the crystals must be directly soldered into the circuit, or be provided with a socket for horizontal mounting.

The heat sink of transistor P 8002 must be slightly shortened, or bent.

The rest of the components can be mounted after completing the mechanical work, with the exception of C 3. The component locations are shown in **Figure 49.**

Connection and Alignment

The BFO and the swept-frequency generator are completely separate circuits that must be aligned separately.

For those readers that intend to construct all boards of this series of articles and who do not possess a swept-frequency generator, it is advisable to firstly complete the BFO-board. This allows one to have suitable signals for alignment.

One will then only require a calibrated attenuator having a maximum attenuation of 100 dB.

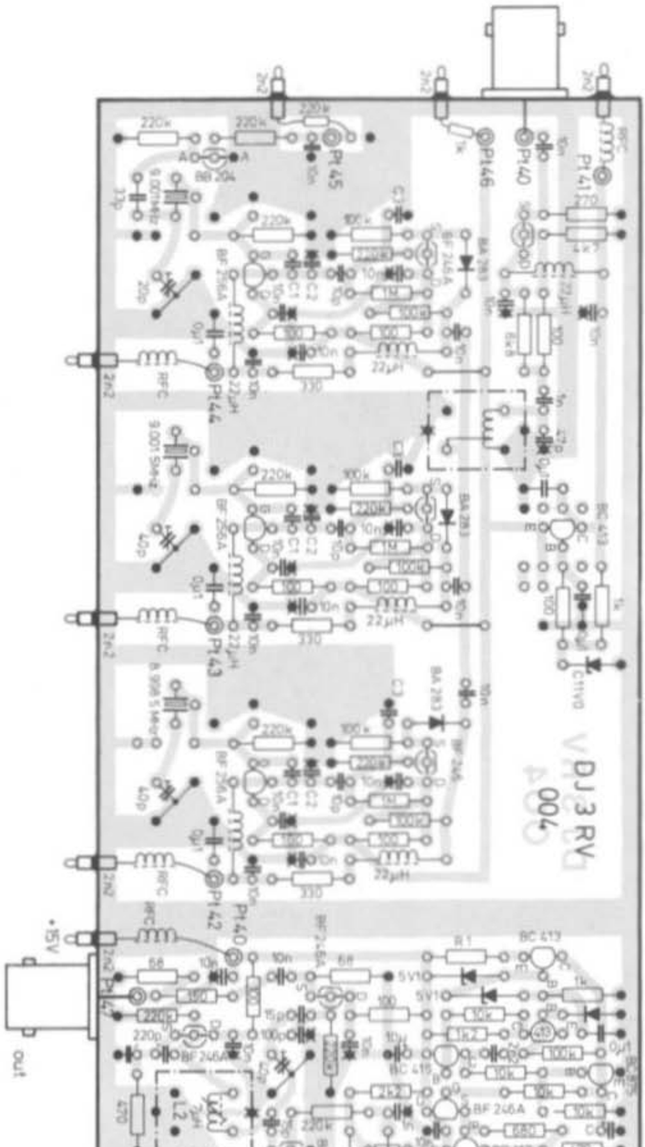


Fig. 49:
Component location plan of the double-coated PC-board DJ 3 RV 004; the positions marked with crosses on the PC-board should be provided with through-contacts.

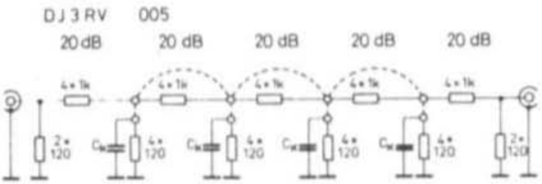


Fig. 50:
Four different attenuation values of 100 dB, 80 dB, 60 dB, and 40 dB can be realized using wire bridges.

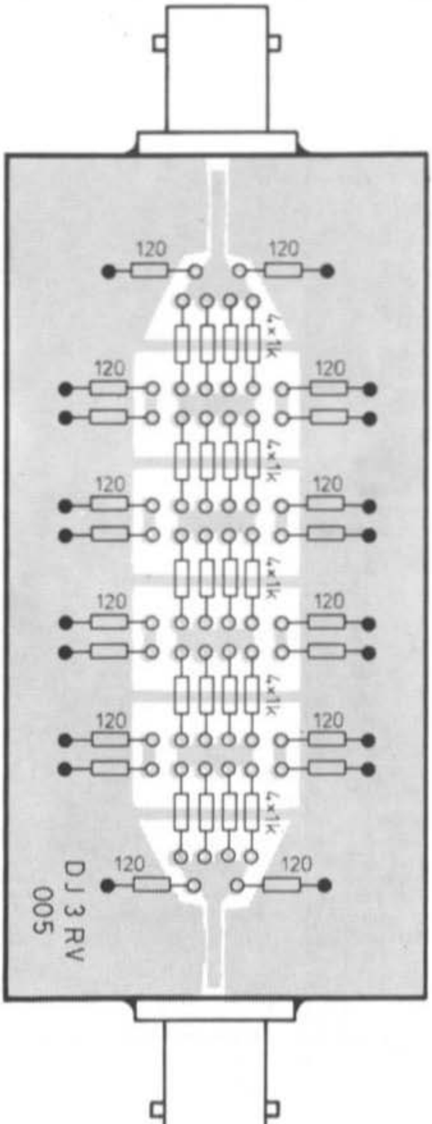


Fig. 51:
Single-coated PC-board DJ 3 RV 005 with component plan

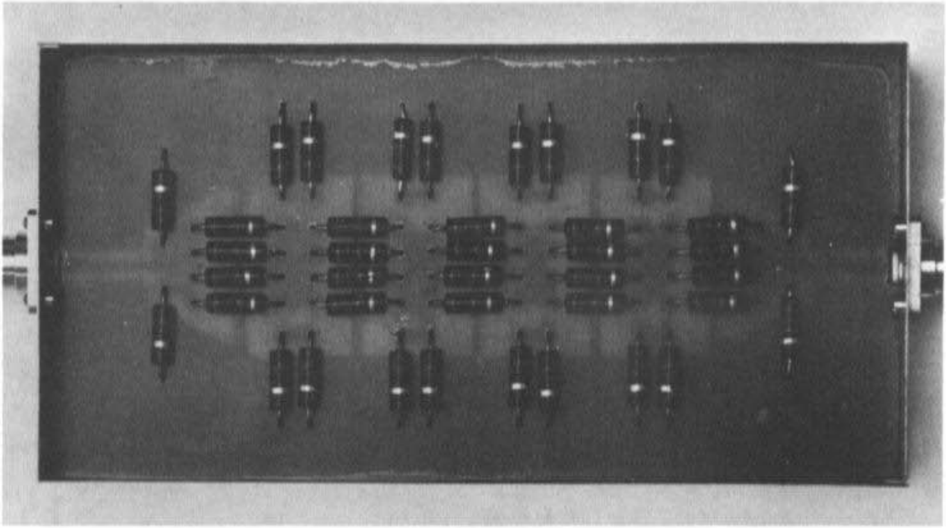


Fig. 52: Photograph of the author's prototype 100 dB-attenuator; impedance 50 Ω

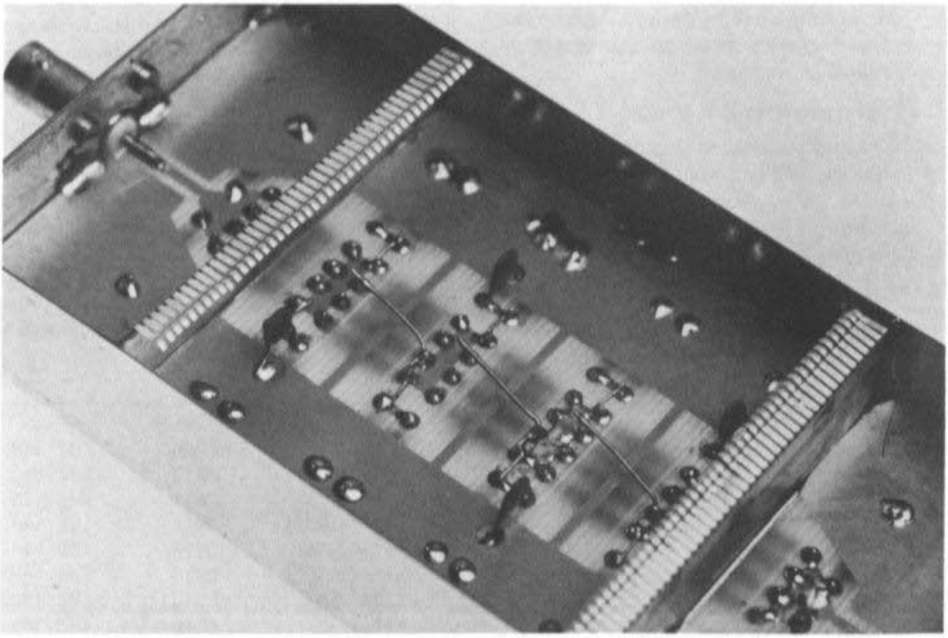


Fig. 53: The wire bridges and compensating capacitors can be seen on the conductor side of the board. This allows the attenuator to also be used in the 145 MHz range. The value of the four capacitors is in the order of 1.5 to 8.2 pF; this depends on the type

Section 4.2.4. is to describe a matching home-made attenuator for this.

The swept-frequency generator does not offer any problems and was equipped with C = 4.7 μF and R = 100 kΩ in the author's prototype. The alignment and measurements are made as follows:

- Connect the operating voltage of + 15 V to Pt 48. The current drain should amount to approx. 40 mA.
- A sawtooth voltage of 4 V_{pp} and approx. 1.8 Hz should be present at Pt 49 (x-deflection).
- Set deviation control (47 kΩ pot.) to zero and adjust the 40 pF trimmer to 2/3 of the maximum value.
- Adjust the frequency of the output signal to 9 MHz with the aid of L 2. The output level should then amount to approximately − 20 dBm into 50 Ω.

A maximum sweep deviation of ± 40 kHz can be adjusted with the aid of the deviation control, and the center frequency should be aligned with the aid of the 40 pF trimmer.

The BFO is just as simple to align:

- Connect the operating voltage of + 15 V to Pt 41. The current drain should amount to approx. 40 mA with the crystal oscillator switched on; (connect Pt 42, Pt 43, or Pt 44 to ground as required).
- 10 to 11 V should be present at Pt 46.
- Align the crystals to their nominal frequency with the aid of the series trimmer. In this case, approximately + 5 V must be connected to Pt 45.
- Align L 1 for maximum output level using the CW-crystal XF 903.
- Align the output level with the aid of C 3 to approximately − 5 dBm (75 mV_{rms}).

4.2.4. Home-Made Attenuator

Figure 50 shows the circuit diagram of a five-stage attenuator using a π-circuit of 20 dB per stage. The switching is made by providing bridges on the board. The insertion loss amounts to 40 dB, and 3 x 20 dB can be switched in additionally. The component locations are shown in **Figure 51.**

As can be seen in the photographs given in **Figures 52 and 53,** the 74 mm x 148 mm single-coated PC-board DJ 3 RV 005 is also enclosed in a metal case. Only two resistance values of 120 Ω and 1 kΩ are required. All resistors should be low-inductance and low-capacitance types. Capless, composite carbon resistors have been found to be very suitable.

When higher demands are placed on the accuracy, it will be necessary for the resistors to be selected. When using a 50 Ω attenuator in a π-circuit having 20 dB attenuation, the exact value of the series resistor amounts to 247.5 Ω, and that of the resistors to ground to 61.1 Ω. When using a capacitive compensation, the attenuator can be used up to approximately 150 MHz.

MATERIAL PRICE LIST OF EQUIPMENT

described in Edition 1/83 of VHF COMMUNICATIONS

A home-made automatic noise-figure measuring system

1. Noise source			Art. No.	**Ed. 1 + 2/83**
Parts	noise source	1 metal case, 1 N connector, 1 BNC socket, 2 transistors, 2 diodes, 1 chip capacitor, 1 disc cap., 2 carbon- and 4 metal film resistors, 1 RF choke	6750	DM 35.00
2. Receive converter				
PC-board	DK10F 034	single coated, with printed component location plan	6442	DM 12.00
Parts	RMG E.K.	3 transistors, 1 crystal filter 10.7/30, 3 coil formers with core, 1 Neosid coil, 2 RF chokes, 1 ferrite bead, 1 m each of 0.8 and 0.12 mm dia. as well as 1 mm dia. silver plated wire, 2 foil trimmers, 3 feed-through and 24 ceram. disc capacitors, 23 resistors, 1 N connector, 1 metal case	6751	DM 105.00
Kit	**Receive converter, complete with above parts**		**6752**	**DM 115.00**
3. Indication electronics/Reference voltage generator				
PC-board	RMG 01	single coated, drilled, with component location plan	6753	DM 31.50
Parts	RMG 01	9 OpAmps, 1 temp. compensated Z-diode, 12 switching diodes, 9 ceramic and 2 tantalum capacitors, 18 trimmer potentiometers, 44 carbon and 15 metal-film resistors	6754	DM 65.00
Kit	**Indication electronics/ Reference voltage generator, complete**		**6755**	**DM 95.00**
4. Control module				
PC-board	RMG 02	Double coated with through-contacts	6756	DM 46.00
Parts	RMG 02	4 transistors, 19 switching and 2 Z-diodes, 6 FET-OpAmps, 2 OpAmps, 2 C-MOS ICs, 19 ceram. disc. caps., 5 tantalum and 3 aluminium electrolytic caps., 3 foil caps., 6 trimmer potentiometers, 40 carbon resistors	6757	DM 120.00
Kit	**Control module, complete with above parts**		**6758**	**DM 165.00**
5. Mixer and variable amplifier				
PC-board	RMG 03	single coated, drilled, with component location plan	6759	DM 23.00
Parts	RMG 03	1 ring mixer, 8 transistors, 2 Z-diodes, 1 coil kit, 1 m wire 0.3 mm diam. 3 RF chokes, 12 ceram. disc caps., 6 tantalum and 5 aluminium electrolytic caps., 4 feed-through caps., 1 trimmer potentiometer, 19 resistors, 1 metal case	6760	DM 130.00
Kit	**Mixer and variable amplifier, complete**		**6761**	**DM 150.00**

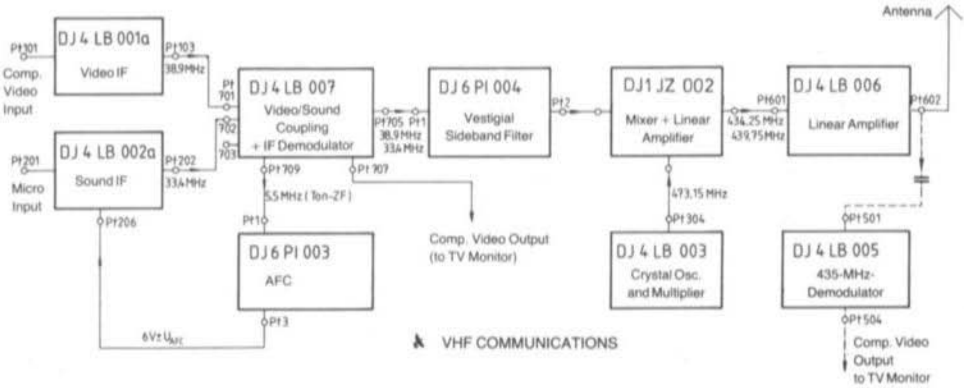
			Art. No.	Ed. 1 + 2/83
6. Dual crystal oscillator				
PC-board	RMG 04	single coated, drilled, with component location plan	6762	DM 23.00
Parts	RMG 04	5 transistors, 3 Schottky-diodes, 1 precision voltage regulator, 3 coil kits, 1 coil former with core, 1 two-hole core, 1 m wire each: 0.12 mm dia., 0.3 mm dia., 0.8 mm dia. silver plated, 7 RF chokes, 2 foil trimmers, 22 ceramic disc caps, 2 feed-through caps., 1 tantalum electrol. cap., 13 resistors, 1 crystal each: 66.7 MHz and 10.72 MHz, 1 metal case	6763	DM 206.00
Kit	**Dual crystal oscillator, complete**		**6764**	**DM 225.00**
7. Remaining parts for the noise-measuring system				
Parts	RMG E1	2 each: 31-pole connectors, male and female, 1 potentiometer 5 kΩ/10 turns, 2 switching- and 2 LEDs (red), 1 toggle switch	6765	DM 75.00
Parts	RMG E2	1 mains transformer 220 V/2 x 15 V/2 A, 2 bridge rectifiers, 1 PC-board DK10F 028, 2 electrolytic caps. 1000 µF/40 V	6766	DM 67.00
Kit	**Automatic Noise-figure measuring system, all parts from 1 to 7**		**6767**	**DM 899.00**

OE 7 WMI VFO with frequency-locked loop	**Ed. 1/1983**
PC-board OE7WMI 002, 003 and VCO: single coated, with component location plan	DM 24.00
PC-board OE7WMI 004: single coated, with component location plan	DM 19.50
PC-board OE7WMI 005: single coated, with component location plan	DM 19.00
PC-board OE7WMI 006: single coated, with component location plan	DM 19.00
Metal case 7411130	DM 5.50

Other parts on request!

DJ 3 RV	**Versatile IF-Module**		**Editions 4/81; 2/82; 3/82; 4/82; 1/83; 2/83**		
PC-board	DJ 3 RV 001a	double-coated, drilled		6729	DM 28.—
PC-board	DJ 3 RV 001b	double-coated, drilled		6730	DM 28.—
PC-board	DJ 3 RV 002	double-coated, drilled		6749	DM 28.—
PC-board	DJ 3 RV 003	double-coated, drilled		6746	DM 28.—
PC-board	DJ 3 RV 004	double-coated, drilled		6748	DM 28.—
PC-board	DJ 3 RV 005	single-coated, drilled		6747	DM 18.—
P 8002	Power-FETs		packets of 10	9069	DM 89.—
BFQ 69	UHF transistor			9577	DM 8.50
Tinned-metal case		74 × 148 × 30		9501	DM 6.50
Toroid core	R6,3K1			9159	DM 1.50
Coil set	D41 – 2165	orange		9166	DM 2.50

An Amateur-Television Transmitter for Home Construction



A television transmitter built from modules described in VHF COMMUNICATIONS is shown in the above **block diagram**. Each function is realised on an individual PC-board. Each PC-board is built into its own tinned-metal box, which leads to a very clean operation without unwanted stray coupling and without problems caused by radiation. Each module may be aligned and tested on its own. All this encourages the home constructor since it makes it easy to understand the different functions, and it finally leads to a high-value ATV transmitter to which all possible video sources (black/white or color) may be connected.

For an amplification of the transmit power, a variety of linear amplifiers for the 70 cm band may be used (not FM »linears« !), whereby care should be taken to adjust the drive so that the output power does not exceed half the PEP value of the SSB mode.

The ATV modules listed have been published by three authors. The descriptions are detailed and will enable successful duplication. They are to be found in the following **editions of VHF COMMUNICATIONS:**

VHF COMMUNICATIONS	1/1973	VHF COMMUNICATIONS	4/1977
VHF COMMUNICATIONS	2/1973	VHF COMMUNICATIONS	3/1981
VHF COMMUNICATIONS	2/1976	**This set of 6 editions is available**	
VHF COMMUNICATIONS	1/1977	**at DM 24.—**	

Individual kits:

DJ 4 LB 001a	kit, complete	DM	98.—	DJ 6 PI 004	ready-to-operate	DM	115.—
DJ 4 LB 002a	kit, complete	DM	99.—	DJ 4 LB 003	kit, complete	DM	92.—
DJ 4 LB 007	kit, complete	DM	90.—	DJ 1 JZ 002	kit, complete	DM	131.50
DJ 6 PI 003	kit, complete	DM	50.—				

Set of complete kits for the 70 cm ATV transmitter (without power amplifier)
comprising DJ 4 LB 001a, DJ 4 LB 002a, DJ 4 LB 007, DJ 6 PI 003, DJ 6 PI 004, DJ 4 LB 003, DJ 1 JZ 002 **DM 650.00**

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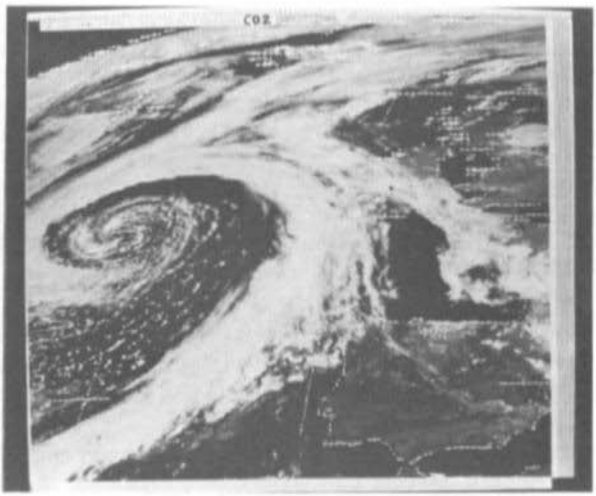
VHF communications

offers ...

A System for Reception and Display of Weather-Satellite Images using a digital scan converter/storage module with 256 lines, 256 pixels and 64 grey levels

As a modern replacement for the DC3NT video processor, VHF COMMUNICATIONS is now able to offer a digital scan converter with the above mentioned features. The 2400 Hz subcarrier is fed from the VHF receiver (DC3NT 003/004), processed and stored in the scan converter, and the CCIR video output can be displayed on any suitable monitor. The scan converter itself consists of two PC-board modules and will be published in editions 4/1982 and 1/1983. We can, however already offer these modules since they are available since February 1983.

All these modules are available as kits, ready-to-operate aligned modules, or as complete equipment in cabinets (see next page).



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A) A complete system as kits

Part in the system	Described in Edition	Kit designation	Art. No.	Price DM
1. **Parabolic antenna,** 1.1 m diam., 12 segm. to be screwed or riveted together, 3 plastic supports for radiator	3/1979	**Set of 12 segm. + supports**	0098	**180.00**
		Riveting machine + rivets	0105	**93.00**
		1.7 GHz Cavity radiator kit	0091	**90.00**
2. **Low-noise amplifier for 1.7 GHz** (Originally described for use at 2.4 GHz, this unit is tuned to 1.7 GHz)	1/1980	**DJ6PI 010**	6565	**225.00**
3. **METEOSAT Converter,** consisting of two modules – Output first IF = 137.5 MHz)	4/1981	**DJ1JZ 003**	6705	**189.00**
	1/1982	**DJ1JZ 004**	6714	**185.00**
4. **VHF Receiver,** frequency range: 136 – 138 MHz, Output: 2400 Hz sub-carrier	4/1979	**DC3NT 003**	6141	**225.00**
	1/1980	**DC3NT 004**	6145	**80.00**
5. **Digital scan converter** (256 × 256 × 6 Bit)	4/1982 1/1983	**YU3UMV 001** **YU3UMV 002**	6736	**675.00**
6. **PAL-Color module** with VHF mod.	2/1983	**YU3UMV 003**	6739	**150.00**

B) Aligned ready-to-operate PCB-modules and equipment

Cavity radiator for above parabolic antenna	0092	**150.00**
VHF receiver for 136 – 138 MHz, DC3NT 003	6731	**395.00**
Oscillator for VHF receiver, DC3NT 004	6732	**168.00**
Digital scan converter (256 × 256 × 6 Bit) YU3UMV 001 + 002	6734	**1150.00**
PAL-Color module with VHF oscillator YU3UMV 003	6738	**285.00**

C) A complete system, ready-to-operate in cabinets

Parabolic antenna, 12 segments, riveting machine and rivets, cavity radiator, supports		**423.00**
METEOSAT converter with GaAs-FET preamplifier and mixer, 2 channels, in casing	3026	**645.00**
Antenna for orbiting satellites, DJØBQ-137 (VHF COMMUNICATIONS 4/1981)	0101	**198.00**
Power combiner for above, AT-137	0306	**98.00**
6-channel VHF receiver in cabinet, programmed for: 137,130/137,300/137,400/137,500/137,620/137,850 MHz	3300	**1298.00**
Digital scan converter, 256 × 256 × 6 Bit, with control electronic, in cabinet	6735	**1980.00**
PAL-Color module with VHF oscillator and power supply, in cabinet	6737	**650.00**
Video monitor, black/white, with 31 cm C.R.T.	3301	**550.00**

A new service of UKW-BERICHTE/VHF COMMUNICATIONS:

All 10 editions of VHF COMMUNICATIONS containing information on weather satellite reception	6742	**49.00**
Dissemination Schedule of METEOSAT, incl. surface mail	005D	**3.00**
Audio Compact Cassette with 2 × 30 minutes of selected subcarrier recordings of METEOSAT and NOAA, resp.	6740	**25.80**

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