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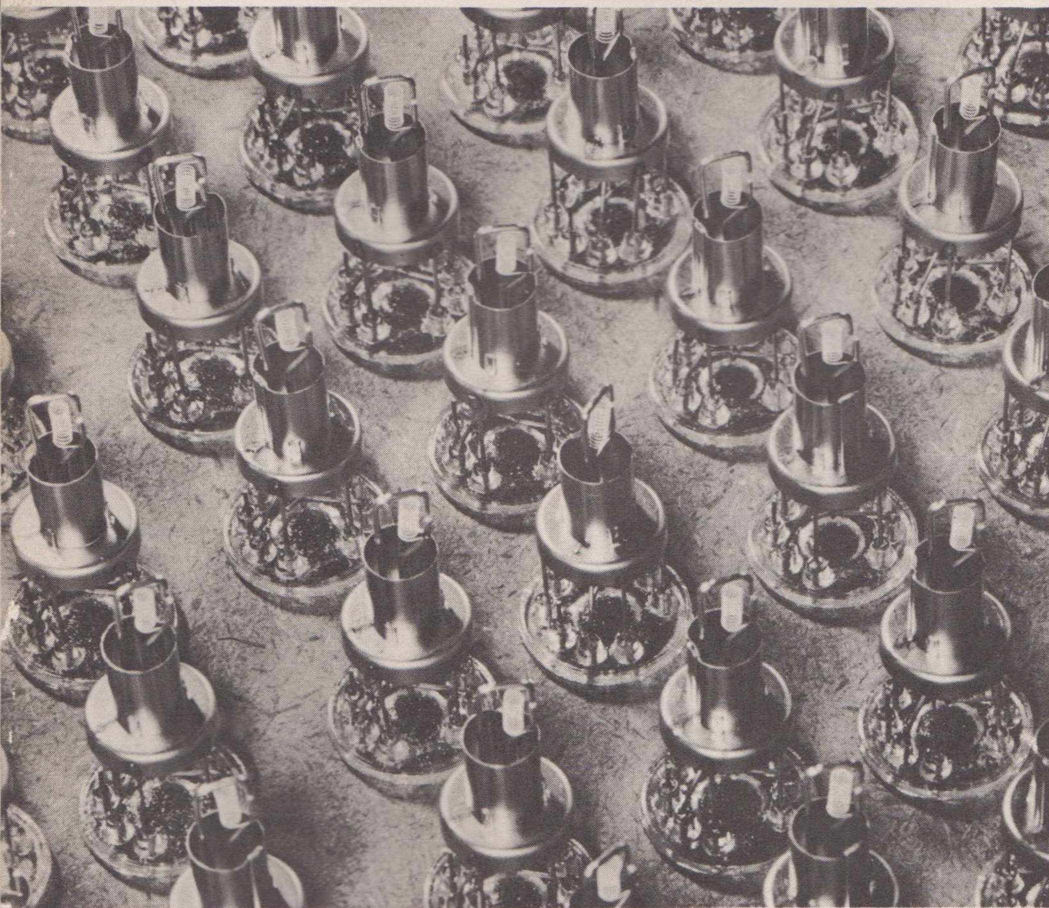

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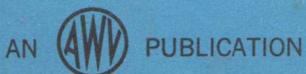

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SECOND BREAKDOWN EFFECTS ON TRANSISTOR APPLICATIONS

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Second breakdown (S/b) is a potentially destructive phenomenon which occurs in bipolar transistors (n-p-n and p-n-p) when the transistor absorbs a critical amount of energy. As shown in Fig. 1, the initiation of second breakdown is

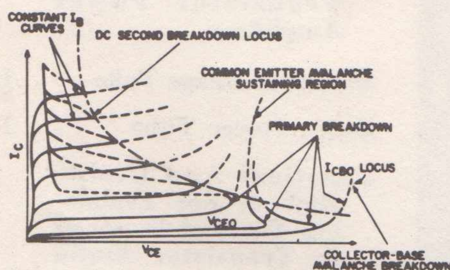


Fig. 1 - Transistor collector characteristics.

characterized by an abrupt decrease in collector-to-emitter voltage. The output impedance changes instantaneously from a large positive value to a negative value, and then finally to a small positive value. Fig. 2 shows that, in general, transistors having higher frequency response or faster switching-speed characteristics are more susceptible to failure from second breakdown. The critical energy required to produce second breakdown varies with operating conditions.

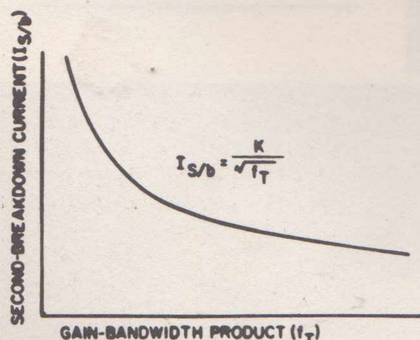


Fig. 2 - Variation of second breakdown with gain-bandwidth product.

Forward-Biased Second Breakdown

With the emitter-base junction forward-biased for normal transistor operation, the severity of second breakdown depends on the operating collector-to-emitter voltage, the duration of the applied voltage, and the temperature of the transistor. In this mode of operation, the positive field applied to the base produces a concentration of carriers at the emitter periphery which, in turn, creates localized hot spots. The intensity of these hot spots, and thus the severity of the S/b problem in any given device, depends on the transverse base field present and the base transit time.

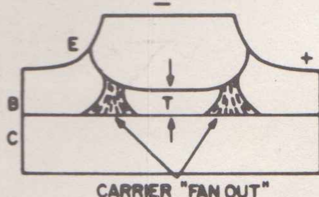


Fig. 3 - Current concentrations in forward-bias mode.

* *In actual transistor operation, the current is injected approximately as e^{-x}, where x is the distance from the emitter periphery, but the "cone" concept of current density is still valid.*

Fig. 3 shows a model of a transistor structure connected in the forward-bias mode. The current injected* into the base region from the emitter tends to fan out in a cone-shaped pattern as it approaches the collector junction. Anything that narrows the base of the cone increases the current density and therefore increases the likelihood that hot spots and consequent second breakdown will occur. The model suggests several conditions that can increase the susceptibility of a transistor to second breakdown:

1. A narrowing of the base thickness which shortens the cone:
   (a) a high-frequency design in which the thickness of the base is intentionally reduced and the carriers have little chance to fan-out;
   (b) a high-frequency design having a "drift" or diffused field which accelerates the carriers and thereby reduces the transit time through the base region;
   (c) an increase in the collector voltage which moves the depletion layer (actual base-collector junction) closer to the emitter-base junction;
2. A pinching of the cone by the transverse field produced by base-current flow.

The maximum power dissipation in a transistor that is limited only by thermal resistance is independent of the applied voltage. When collector current I_C as a function of voltage is plotted on a log-log scale, as shown in Fig. 4 (a), the portion of the curve having a slope of -1 represents the region in which the device is thermally limited. For devices

limited by second breakdown, this maximum operating area is bounded by a line having a slope of —1.5 to —2.5, depending on the device. Fig. 4 (b) indicates three possible situations:

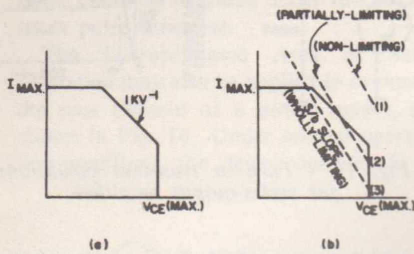


Fig. 4 - Typical area of safe operation.

1. The second breakdown slope can be non-limiting, i.e., fall completely outside the maximum operating area. Consequently, the device is fully usable within its voltage, current, and power maximum ratings.

2. The second breakdown slope can intersect the constant power curve and partially limit the device under higher-voltage and higher-power conditions.

3. The second breakdown slope can fall entirely within the constant-power curve and wholly limit the device, preventing it from delivering rated thermal power.

Reverse-Bias Second Breakdown

When the emitter-base junction is reverse-biased, as shown in Fig. 5, the field present in the base is reversed and

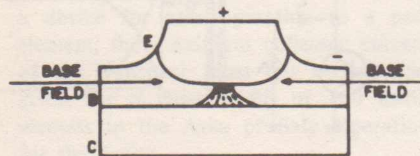


Fig. 5 - Current concentrations in reverse-bias mode.

all of the minority carriers as they are transmitted to the collector are pinched into a single point (in the case of a circular-emitter geometry) or into a line (in the case of an interdigitated geometry). Consequently, to encourage fanout, it is even more important to maximize base thickness and to avoid potential gradients in the base region which create an axial accelerating field. The amount of energy that the device will withstand in this mode of operation is substantially less than for forward-bias operation because a heavy carrier concentration is spread over even less area at the collector junction. This critical amount of energy is a function of the load inductance and the base-emitter termination, as shown in Fig. 6.

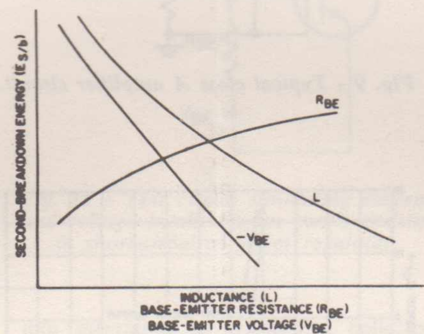


Fig. 6 - Critical second-breakdown energy as a function of load inductance and base-emitter terminations.

Device Ratings to Insure Safe Operation in a Forward-Biased Mode

Probably the one standard criterion that most completely defines the dc and pulse operation limits for a transistor in the forward-bias mode is the Area of Safe Operation. Fig. 7 (a) shows the Area of Safe Operation for the 2N3055, a device thermally limited within its ratings. Fig. 7 (b) shows the area for

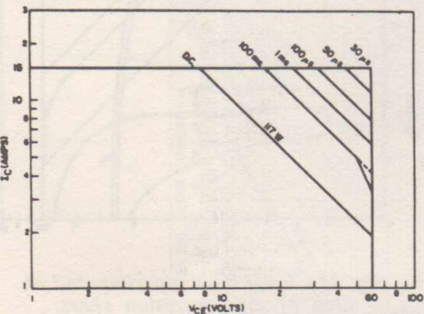


Fig. 7(a) - Area of safe operation for 2N3055

the 2N3879, a transistor designed to operate at high V_{CE} where the device is limited by second breakdown, not thermal conditions.

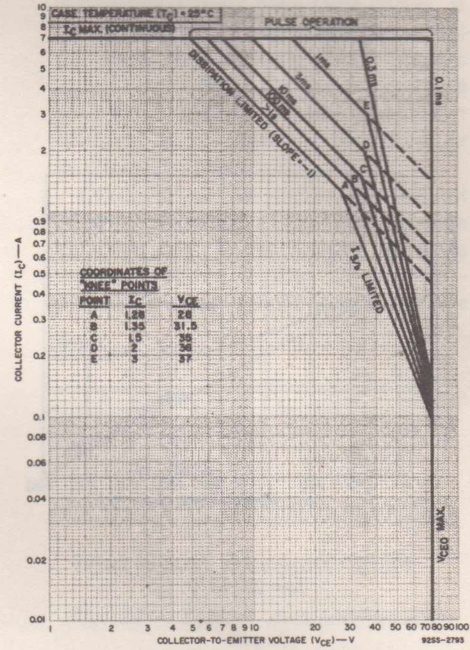


Fig. 7(b) - Area of safe operation for 2N3879.

Increasing case temperature affects the power-dissipation limits far more than the second-breakdown limits of a transistor. Therefore, as shown in Fig. 8, separate temperature-derating curves are required for these two limiting factors. For dc operation, Fig. 7 (b) may be used directly to determine the maximum allowable power. For pulse operation at temperatures greater than 25° C, however, Fig. 8 must be used in conjunction with Fig. 7 (b) as follows:

1. For a specified pulse width and collector-to-emitter voltage, V_{CE}, determine from Fig. 7 (b) the maximum collector current at 25° C, using the appropriate "Dissipation-Limited Curve" (or its dashed-line extension).
2. Refer to the dissipation-limited curve shown in Fig. 8 to determine the percentage current derating at the specified temperature. Apply this derating to the value of I_C obtained in step 1 to obtain the maximum current for dissipation-limited operation.
3. If the specified value of V_{CE} required the use of a dashed-line extension of a dissipation-limited curve in step 1, then repeat step 1, using the curve marked "$I_{S/b}$ limited."
4. Repeat step 2 using the $I_{S/b}$ limited curve in Fig. 8.

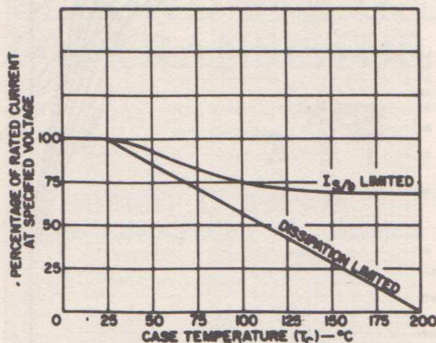


Fig. 8 - Dissipation derating curve for 2N3879.

5. The maximum allowable current is the smaller of the two values obtained in steps 2 and 4.

For repetitive-pulse operation, the actual case temperature to be used in Fig. 8 is the sum of the maximum ambient temperature and the rise in case temperature resulting from the average transistor power dissipation. The temperature rise is the product of average power dissipation and the thermal resistance from case to ambient, which depends on the heat-sink properties.

Many circuit applications can be directly evaluated by the Area of Safe Operation. The margin of safety in all class A operations can be determined by simply plotting the operating point on this graph and derating the curve to the actual operating temperature of the case.

As an example, the worst-case load line of the transformer-coupled class A amplifier shown in Fig. 9 may occur anywhere from open- to short-circuited output, and from low to high frequency, depending on such things as the quality of the output transformer and the frequency response of the output transistor. Thus, several load lines may be required before the true worst-case condition is found. Two load lines are shown in Fig. 10, one representing a low-frequency, low-impedance condition, and the other a high-frequency, open-circuit condition. These load lines are shown in Fig. 11 superimposed on the Area of Safe Operation for the 2N3055 transistor used. As a result, the actual circuit operating

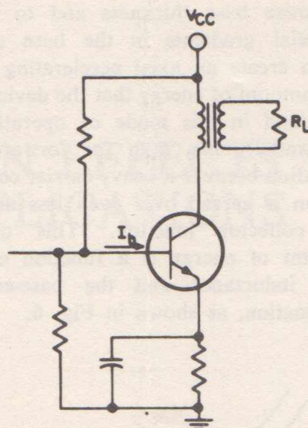


Fig. 9 - Typical class A amplifier circuit.

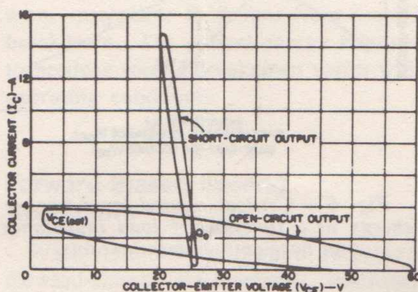


Fig. 10 - Load lines for class A amplifier.

conditions can be directly compared with the capability of the device.

There are many other applications for the safe-operation curves, however, which are not so obvious. When the series out-

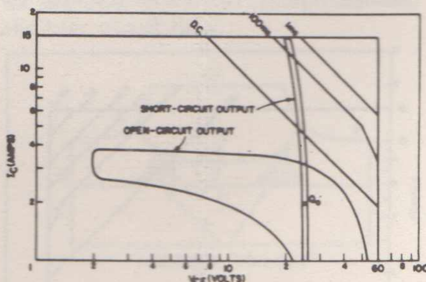


Fig. 11 - Load lines superimposed on area of safe operation chart.

put power amplifier shown in Fig. 12 is first turned on and a low-frequency drive signal is present, V_{CC} is the initial voltage across the collector-emitter circuit of the upper transistor, and h_{FE} I_B is the

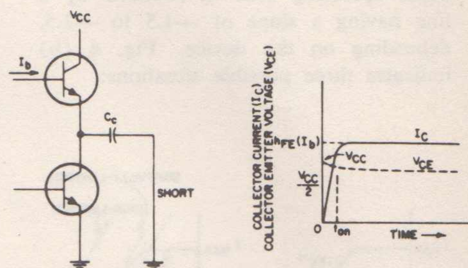


Fig. 12 - Turn-on transient conditions for series-output amplifier.

initial current which flows to charge the coupling capacitor. The time constant R_LC will typically be 10 milliseconds or more. The power dissipated during this time can be considerably above the rating of the device. By the use of the pulse ratings shown in Fig. 7, however, it can be determined whether this pulse condition is within the safe operating area of the device.

Another use of the safe area of operation for a power amplifier occurs under short-circuited output conditions, as shown in the circuit in Fig. 13. In this case, one-half the supply voltage (it is assumed that the coupling capacitor C is charged to $\frac{V_{CC}}{2}$ and that this component is relatively fixed even at low frequencies) will appear

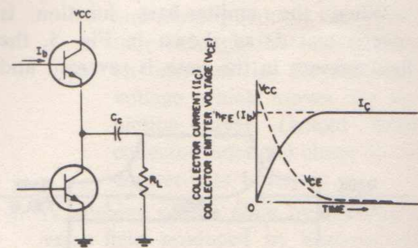


Fig. 13 - Short-circuit conditions for series-output amplifier.

across the collector-emitter terminals, and the collector current will be h_{FE} I_B for the duration of the input signal. For a wideband amplifier operating at 5 Hz, the duration of the signal will be 100 milliseconds. The input signal is usually a

sine wave, but under short-circuit conditions there is no feedback and the output current approximates a square wave. Thus, the worst-case conditions would be $\frac{V_{CC}}{2}$ and I_C (peak) for 100 milliseconds. Reference to the pulsed safe-area curves would quickly indicate whether the transistor could be operated under this maximum pulse condition.

The forward-biased Area of Safe Operation may also be applied to evaluate the pass element of a power supply, as shown in Fig. 14. Under normal operating conditions, the device operates in a class A mode. However, if a short circuit is applied to the output, a collector current of h_{FE} I_B will flow and the full input voltage will appear across the pass element until the input is disconnected by some overload-sensing device. If an input fuse is used as the protective device, the time t for disconnect may be typically 100 milliseconds. Therefore, to fully specify a device for safe operation as a pass element, the maximum collector current of the transistor must not exceed that given for a pulse width of 100 milliseconds in the Area of Safe Operation for the device.

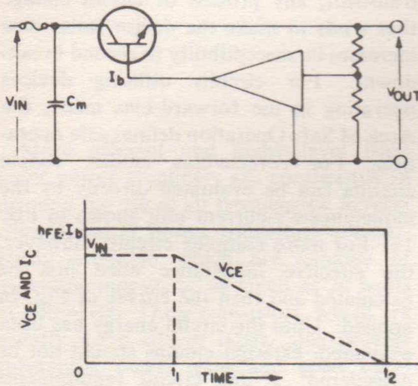


Fig. 14 (a) Simplified series-regulator circuit, and (b) Current and voltage waveshapes for pass transistor in short-circuited series regulator.

Device Rating to Insure Safe Operation in a Reverse-Biased Mode

Specifying devices for safe operation in the reverse-bias mode is not as simple as for the forward-bias mode. For power application, however, the worst-case load is inductive; thus, the capability of the device is usually specified for inductive loads. Fig 15 shows a test circuit that can be used to evaluate the Area of Safe Operation for a transistor under inductive loads. The transistor to be tested is driven into saturation to a specified collector current I_C. The input pulse is then removed and the transistor is back-biased by V_{BE} and R_{BE}. The data obtained can be plotted as shown in Fig. 16. Fig. 16 (a) shows the collector current as a function of inductance under fixed reverse-bias conditions. Fig 16 (b) and 16 (c) show the derating of collector current as V_{BE} and R_{BE} are changed from the test conditions.

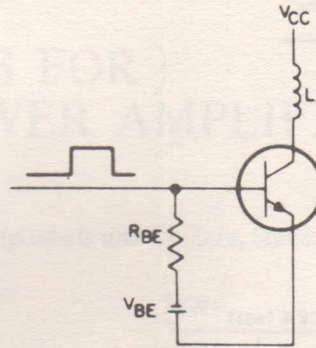


Fig. 15 - Test circuit simulating current and voltage conditions for pass transistor in short-circuited series regulator.

Because the test circuit uses an inductance, the maximum safe operating conditions for solenoid drivers, relay drivers, hammer drivers, and the like can be determined directly from these curves. If an investigation of the circuit shows that the operating condition is outside the safe operating conditions for the device being considered, then, and only then, is it necessary to use clamping techniques or to change to another transistor.

Other reverse-bias applications are not as easily evaluated as that of the simple inductive load. In the case of a switching regulator, shown in Fig. 17, the "free-wheeling" diode should commutate the energy in the inductor to the load during the "off" period of the transistor. The actual safe operating conditions can be obtained directly for all the reverse-bias conditions once the circuit is functioning. From the voltage and current waveforms shown in Fig. 18, the effective inductance presented to the transistor during turn-off can be calculated as follows:

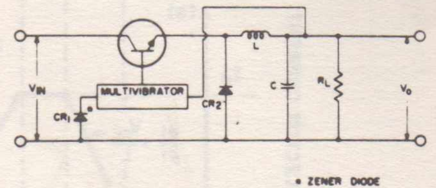


Fig. 17 - Typical switching-regulator circuit.

The voltage V induced by a current change in an inductor is given by

$$V = L \frac{di}{dt}$$

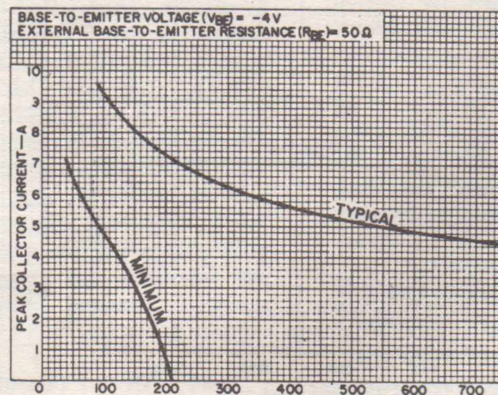


Fig. 16 - Reverse-bias, second breakdown characteristics for 2N3879 under various conditions.

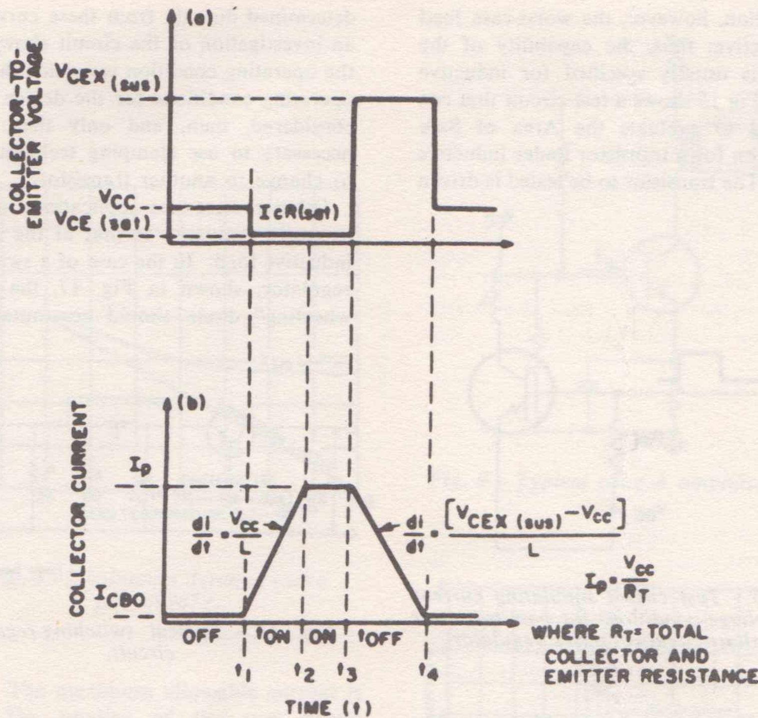


Fig. 18 - Voltage and current waveforms for switching-regulator circuit.

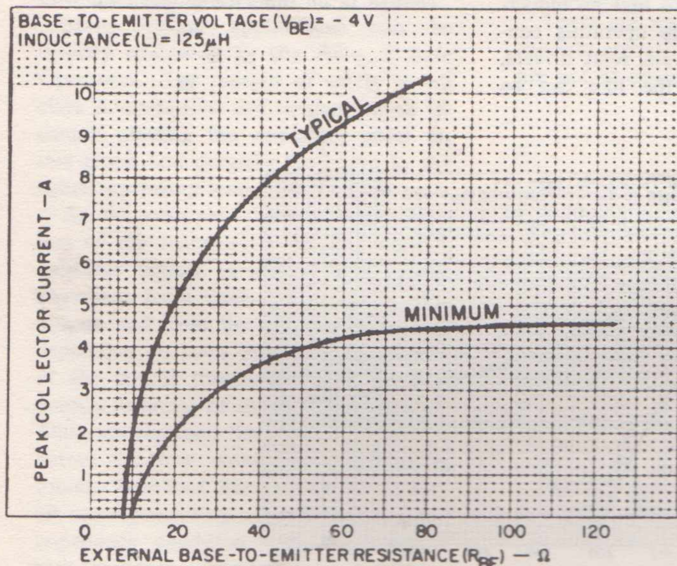
Thus, from Fig. 18, the inductance L is given by

$$L = (V_{CEX}\ (sus)\ - (V_{CE}) \left(\frac{dt}{di}\right)$$

From the waveforms shown in Fig. 18, the maximum voltage across the transistor V_{CEX} can be determined and the rate of change of current can be obtained (generally a linear ramp). When this information is known, the effective inductance can be calculated. The data presented in Fig. 16 will then show whether operation is safe. This waveform analysis can also be applied directly to the case of the open-circuited class A power amplifier and the open-circuited auto-ignition system.

Summary

As a general rule, fast devices are more prone to second breakdown failures than slow devices. Therefore, for a given transistor, any process of circuit change that tends to make the device faster also increases its susceptibility to second breakdowns. For circuits utilising devices operating in the forward-bias mode, the Area of Safe Operation defines safe operation. For reverse-bias modes, simple circuits can be evaluated directly by the inductance-v's-current plot shown in Fig. 16. For more complex circuits, however, the effective inductance must first be calculated and then the curves of Fig. 16 applied. Until the circuit energy has been evaluated, external clamps should not be considered. If the circuit requirements exceed the capabilities of the device, then, and only then, should external protective circuits be added.



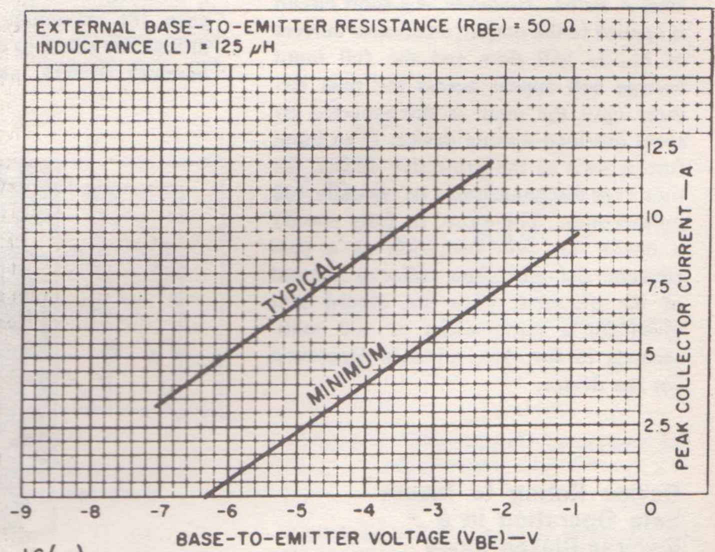


Fig. 16 - Reverse-bias, second breakdown characteristics for 2N3879 under various conditions.

DESIGN TRADE-OFFS FOR RF TRANSISTOR POWER AMPLIFIERS

By ROBERT MINTON
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More efficient and higher-level transistor power amplifiers are consistently in demand for use at all frequencies. Several commercial rf power transistors are currently available which are capable of providing outputs of as much as 20 watts at 400 MHz. These transistors, which are usually n-p-n silicon types, also provide substantial power gain and good operating-circuit efficiency. RF power transistors have been used successfully as class A, B, and C tuned power amplifiers with excellent frequency and temperature stability.

These power transistors are being designed into both airborne and ground transmitting equipments in increasing numbers. In such circuit applications, rf power transistors have established their ability to operate efficiently and reliably for long periods of time. The success of these transmitting equipments is largely the result of design trade-offs which provide a good balance between the optimum performance capabilities of the transistors and stable, reliable, and efficient circuit operation. This paper discusses some of the design trade-offs necessary for good rf power transistors and reliable circuit performance.

General Discussion

In the design of any power amplifier, certain design trade-offs are necessary to satisfy the given objectives. These trade-offs are largely influenced by the type of circuit application required for the power amplifier. If maximum operating reliability is of prime importance, the rf power transistor may have to be operated below its full capabilities. If the power amplifier is operated from a dc battery, or if the space requirements are such that the size of the dc power supply is limited, power gain may have to be sacrificed for optimum power efficiency. Other factors which influence the design trade-offs are frequency stability, type of modulation, and ambient temperature considerations.

Selection of Proper RF Power Transistor

When a circuit application requires the use of transistors as rf amplifying devices, the transistors selected must be capable of performing the intended function most economically and efficiently. They must be capable of operating reliably over the frequency range of interest and of providing a practical amount of power gain. As a result of the increasing number of rf power transistors available on the commercial market, circuit designers can now be selective in the choice of devices. The choice of a transistor depends on such factors as maximum power output, maximum operating frequency, power efficiency, power gain, and cost per watt of power generated. How well a particular transistor manufacturer can satisfy these requirements will determine the ultimate use of his product.

Design Trade-offs for RF Power Transistors

The design trade-offs practised in the development of power transistors are as follows:

- Frequency versus Voltage
- Frequency versus Current
- Frequency versus Power

E. O. Johnson[1] has considered the relationship of these transistor parameters in detail, and has shown by analysis that the ultimate performance limits of a transistor are set by the product $Ev_s/2\pi$, where E is the dieletric breakdown voltage of the semi-conductor material used and v_s is its minority. carrier saturated drift velocity. This product, which has a value of about 2×10^{11} volts per second for silicon, emphasizes the fact that a semiconductor material has a maximum capability for energizing the electrical charges that process a signal. If the operating frequency of a device is high, the frequency time period is short, and only a small amount of energy can be given to a charge carrier. Consequently, the power output and the power amplification must be relatively low. At low frequencies, the inverse is true. The physics of semi-conductor devices impose an inverse relation between frequency and power parameters which is independent of the thermal-dissipation arguments commonly used to justify the necessary trade-off between these paramaters.

Frequency-Voltage Design Trade-off

For a silicon power transistor, the best possible trade-off between frequency capability f_T and maximum allowable applied voltage V_m is given by[2]

$$V_m = \frac{Ev_s}{2\pi f_T} = \frac{2 \times 10^{11}}{f_T} \text{ volts} \quad (1)$$

This equation indicates the inverse relationship between maximum allowable applied voltage and frequency. If a transistor is designed to have the best possible frequency capability, the resultant maximum allowable peak operating voltage will be low.

Practical circuit applications generally require that the maximum peak-voltage rating be at least twice the dc supply voltage, or sufficiently higher to provide an adequate safety margin for voltage transients. The maximum collector-voltage rating of an rf power transistor must also be high enough to avoid breakdown under conditions of strong reactive loading. As a result, it may be necessary to achieve a design trade-off in the maximum frequency capability.

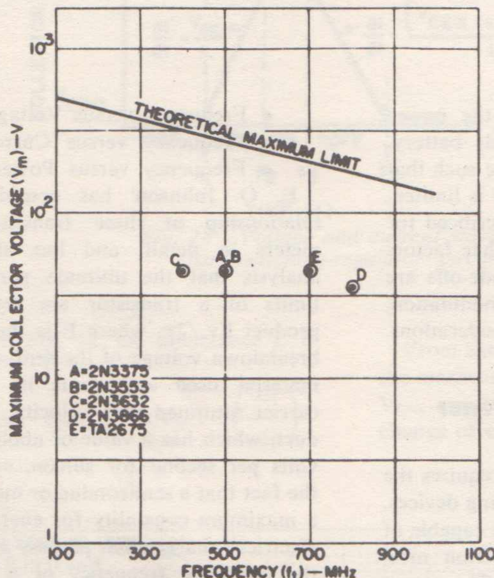

Fig. 1 - Voltage-frequency relationship for rf power transistors.

Fig. 1 shows the theoretical relationship between maximum collector voltage V_m and frequency f_T, together with the actual relationship between breakdown voltage V_{CEV} and f_T for five RCA overlay rf power transistors.

There are two main reasons why the device performance falls short of the theoretical limit. First, the breakdown voltage V_{CEV} is primarily determined by surface leakage and is generally somewhat lower than V_m, which is equal to the dielectric breakdown field E. Second, the overlay devices are designed primarily for 28-volt operation, and the necessary design trade-offs have been imposed. The most recently developed devices (the 2N3866 and the RCA Dev. No. TA2675) tend to lie closer to the maximum curve.

Frequency-Current Design Trade-off

The best possible trade-off between maximum collector current I_m and frequency f_T is given by[3]

$$I_m X_c = \frac{E v_s}{2\pi f_T} \qquad (2)$$

where X_c, the reactance of the collector-to-base capacitance is equal to $2\pi f_T C$. Eq.(2) indicates that there is an inverse relationship between maximum attainable peak collector current and frequency. The maximum peak collector current is usually limited primarily by the practical consideration that the current amplification factor varies approximately inversely with emitter current at high values of emitter-current density. The maximum peak-collector-current rating, therefore, may be established by the amount of reduction in current gain which can be tolerated at high frequencies. Eq.(2) also indicates that a device designed for high peak currents has a substantially reduced output impedance.

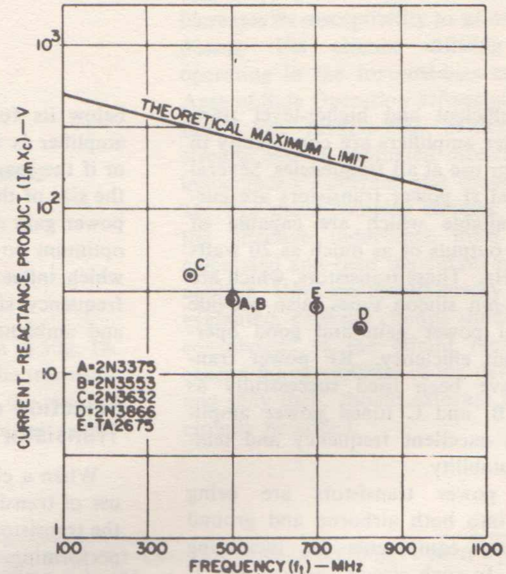

Fig. 2 - Current-frequency relationship for rf power transistors.

Fig. 2 shows the theoretical relationship between the current-reactance product $I_m X_c$ and frequency f_T, together with the actual relationship for the overlay transistors. Again, the discrepancy between device performance and the theoretical curve results from the fact that the necessary trade-offs have been applied to the transistors to assure practical values of high-frequency current gain.

Frequency-Power Design Trade-off

The relationship between peak power, impedance level, and frequency for a transistor can be obtained by multiplying Eq.(1) and Eq.(2), as follows:

$$V_m I_m X_c f_T^2 = \left(\frac{E v_s}{2\pi}\right)^2 \qquad (3)$$

Eq.(3) can then be rearranged to obtain the following relation for peak power P_m (where $P_m = V_m I_m$):[4]

$$(P_m X_c)^{1/2} = \frac{E v_s}{2\pi f_T} \qquad (4)$$

Eq.(4) shows that, for a given device impedance, the peak power or volt-ampere product must necessarily decrease as the frequency f_T is increased. Eq.(4) also indicates that transistors should be designed to operate at relatively high currents for the best trade-off between power and frequency capability. Although high-current, low-voltage operation requires a decrease in impedance level, it does not impose the decreased frequency capability that would result if the device were designed for low current and high voltage.

The maximum peak power determined from Eq.(4) for a transistor with a specified f_T and X_c is obviously much greater than can be obtained in a practical situation. Certain constraints of circuit design restrict the maximum peak power to a much lower value. In a practical circuit design, the applied dc supply voltage is not V_m, but is usually equal to or less than $V_{CEV}/2$. Because the maximum breakdown voltage V_{CEV} of a transistor is determined by surface leakage effects, the applied voltage is prohibited from approaching the maximum theoretical value V_m, and the peak-power is always lower than indicated by Eq.(4). In addition, the peak power is limited by the power-dissipation capability of the transistor. All power transistors have some finite thermal impedance between the collector junction and case which causes power losses within the devices. In practical circuit applications, the peak power capability of an rf power transistor is limited by the power-dissipation capability of both the particular device and the circuit. Fig. 3 shows the theoretical relationship between the power-reactance product $(P_m X_c)^{1/2}$ and frequency f_T, together with the actual relationship for RCA overlay transistors.

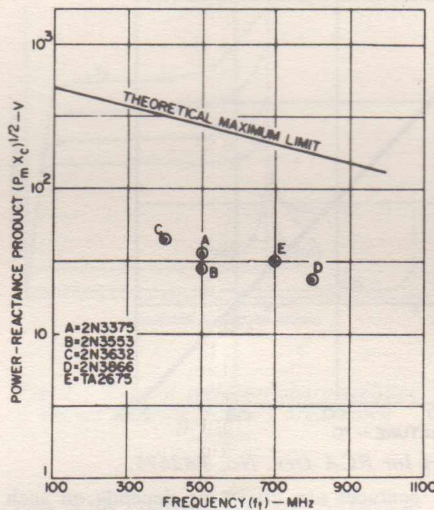

Fig. 3 - Power-frequency relationship for rf power transistors.

Design Trade-offs for RF Transistor Power Amplifiers

When a transistor is operated as a high-frequency power amplifier, the objective is usually to obtain as much power output as possible with good power gain and power efficiency and a minimum amount of harmonic distortion. How well these objectives can be realized depends on the design trade-offs which must be imposed to obtain reliable circuit operation.

Choice of Operating Mode

Transistor rf power amplifiers can be operated in class A, B, or C arrangements. The choice of mode of operation depends on several factors, including the amount of output power, power gain, and power efficiency required. When moderate amounts of output power and high power gain are the prime objectives, the class A arrangement is usually employed. However, the power efficiency is low in class A operation, and a high level of device power dissipation results. Class A operation of transistors is usually confined to low-signal-level stages in which the requirements for dc input powers can be kept low.

When circuit-design requirements demand several watts of rf power output, one of the cutoff modes of operation is used. Class B and class C operation are characterized by good collector-circuit efficiency and a relatively high power output in proportion to the average dissipation in the transistor. During periods of zero input signal, the power-supply drain and the collector dissipation are low. Class B operation usually results in higher power gain, but the collector efficiency is lower than in class C operation. The higher-power-level stages of an rf power amplifier are generally operated in either the class B or class C mode to obtain good power efficiency, usually with some sacrifice of power gain.

Choice of Circuit Configuration

To achieve a particular set of design objectives, a circuit designer must select a circuit configuration capable of providing the greatest latitude. The choice of circuit configuration is primarily influenced by operating frequency, power gain, bandwidth and rf stability requirements. The circuit configuration should also allow simplicity in the design of coupling networks used in both input and output circuits.

Both the common-base and common-emitter circuit configurations are frequently used in rf power amplifiers. At very high frequencies, the apparent power gain of the common-base circuit configuration is somewhat greater than that of the common-emitter circuit. However, the common-base circuit configuration is at best only conditionally stable. Frequency stability is usually established by imposing special conditions on the source and load impedances and on the circuit itself. The apparent increase in power gain of the common-base circuit, therefore, may be a result of regeneration.

The common-emitter circuit configuration is basically unconditionally stable. However, large-area high-gain devices of the interdigitated and overlay structures can produce unstable operation. In general, this instability can be avoided by careful circuit design and layout techniques. At extremely high frequencies, the emitter lead inductance restricts the power-gain capability of the common-emitter circuit.[5,6] A compromise in power gain is usually accepted and the common-emitter circuit is most frequently employed because of its better rf stability. Wide bandwidths are also obtained more easily by use of the common-emitter configuration.

Circuit-Design Considerations

When the mode of operation and the circuit configuration have been selected, the circuit designer must utilize the circuit techniques necessary to obtain the best performance from the rf transistor Optimum performance of the devices can be realized only if the circuit designer understands the importance of certain transistor characteristics. In the design of rf power amplifiers, the following transistor characteristics are important:

(a) maximum collector dissipation,
(b) maximum collector voltage,
(c) maximum peak collector current,
(d) high-frequency current-gain figure of merit (f_T),
(e) input and output impedance or admittance characteristics.

Power-Dissipation Considerations

The dc supply voltage, power output, power gain, operating frequency, and harmonic distortion are usually specified for a particular application. The most important consideration in the circuit design then becomes the power-dissipation capability of the transistor. The maximum power that can be dissipated before thermal runaway occurs depends to a great extent on how well the heat

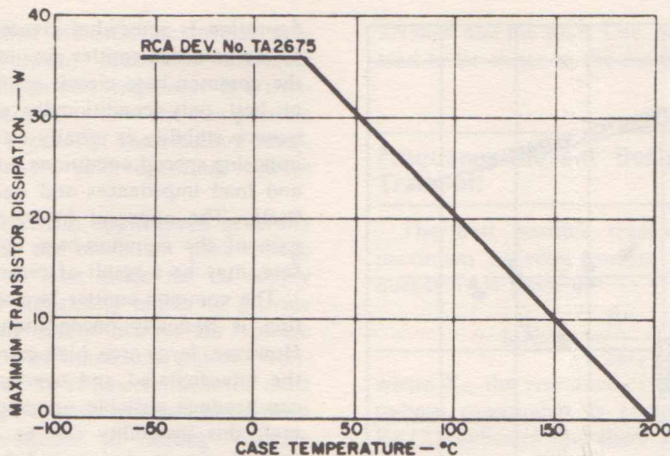

Fig. 4 - Dissipation derating chart for RCA Dev. No. TA2675.

generated within the transistor is removed. When heat is removed by conduction, the amount removed is an inverse function of the thermal resistance. Obviously, therefore, the rf power transistor selected should have the lowest possible value of thermal resistance to minimize the power-dissipation problem. The power-dissipation capability P_d of a transistor can be determined from the following expression:

$$P_d = \frac{T_j - T_a}{\Theta_R} \quad (5)$$

where T_j is the maximum collector-junction temperature, T_a is the maximum ambient temperature, and Θ_R is the total circuit thermal resistance.

Fig. 4 shows the power-dissipation capability of the RCA Dev. No. TA2675 power transistor as a function of temperature. This curve relates the power-dissipation capability of the device to the case temperature, and thus to the thermal-resistance value as measured from the collector junction to the case. If the thermal-resistance path from the transistor case to the ambient surrounding is appreciable in a particular installation, the power-dissipation capability of the transistor is greatly reduced. The circuit designer must minimize both circuit and external thermal-resistance paths if full power dissipation capability of the transistor is to be realized. When compactness is a prime requirement, it may be necessary to derate the transistor to avoid excess power dissipation.

Because the transistor and the associated circuit have losses, a concerted effort must be made to obtain the highest possible power efficiency. Typical power efficiences ranging from 50 to 85 per cent can be obtained in most practical circuits. The extent to which higher percentages are attainable depends on such factors as collector supply voltage, efficiency of coupling networks, and operating frequency.

The use of the lowest feasible power-supply voltage usually results in increased power efficiency. However, the increase in efficiency is generally accompanied by a decrease in power gain of the transistor. In addition, the use of low-voltage power supplies increases the peak-current demand on a given transistor if a high level of rf power output is required. Under such conditions, the resultant current gain may be low, so that the attainable power is again reduced. Fig. 5 shows curves of collector-circuit efficiency and power output as functions of dc supply voltage. As the supply voltage is decreased, the collector efficiency increases, but the rf power output or power gain decreases as shown.

In a practical case, the dc supply voltage is usually established, and the circuit designer must select a transistor capable of providing both the required power gain and power efficiency for the specified power output.

Power losses in tuned coupling networks can be minimized by maintaining a high ratio of unloaded Q to loaded circuit Q. At the lower frequencies, efficient lumped-constant-element circuits can be designed which have minimum power loss. At higher frequencies, however, the use of lumped-constant-element circuits can introduce appreciable circuit losses. Strip-line or cavity-resonator-type circuits are usually employed at the higher frequencies to minimize circuit losses.

The power-dissipation problem in an rf amplifier can be reduced by proper selection of the operating frequency. The reduction in power efficiency with frequency can be attributed to the fact that the saturation voltage of a transistor increases with increasing frequency.[7] As a result, power losses in the transistor increase and rf power output is reduced. Fig. 6 shows the variation of collector-circuit efficiency and power output with frequency. The lowest feasible operating frequency should be used if power efficiency is of primary concern. If the operating frequency is established by design requirements, reduced power efficiency may be a necessary trade-off to obtain the required power output.

Collector-Breakdown Voltage Considerations

Transistor voltage breakdown is a function of both the individual device characteristics and the associated circuit. The maximum collector-voltage ratings established by a transistor manufacturer usually indicate the safe limits to which

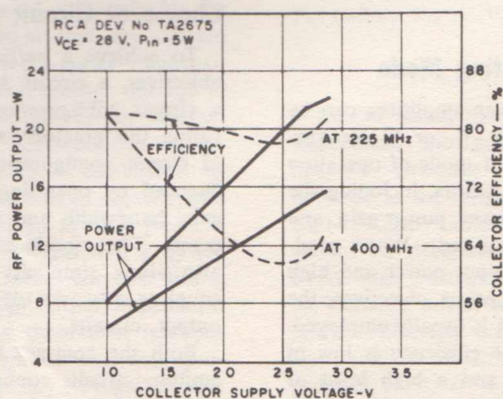

Fig. 5 - Power output and collector efficiency of the RCA Dev. No. TA2675 as functions of collector supply voltage.

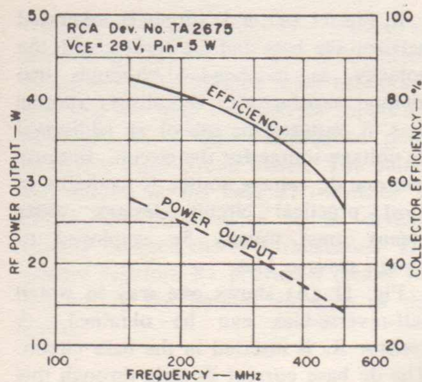

Fig. 6 - Power output and collector efficiency of the RCA Dev. No. TA2675 as functions of frequency.

the collector junction can be stressed without breakdown occurring. The circuit designer must be capable of interpreting these voltage ratings and adjusting circuit operating conditions so that the maximum ratings will not be exceeded.

There are several breakdown voltages with which a circuit designer must be familiar when he chooses a transistor for a given circuit or selects the operating dc supply voltage. Fig. 7 shows a typical family of collector characteristics, with base current as a parameter, together with the voltage-breakdown characteristics. The collector-to-base breakdown voltage with the emitter open, V_{CBO}, approaches the avalanche voltage V_A.[8,9,10] Collector-base breakdown of a transistor operating in a common-base connection is caused by avalanche multiplication. In common-emitter circuits, avalanche breakdown occurs at the collector-to-base voltage at which the common-emitter current transfer ratio, beta (β), becomes infinite.[11]

As shown in Fig. 7, the collector-to-emitter breakdown voltages are considerably lower than the collector-to-base breakdown voltages. The choice of the common-emitter circuit for stability reasons requires a design trade-off with respect to breakdown-voltage capability. The collector-to-emitter breakdown-voltage curve V_{CEO} indicates the maximum voltage which can be applied for a forward-biased base-emitter junction. If an rf power transistor is intended for class A operation, the dc supply voltage must be limited to one-half of V_{CEO}. In class B or class C operation, where the transistor is at cutoff or reverse-biased, the collector-to-emitter breakdown voltage

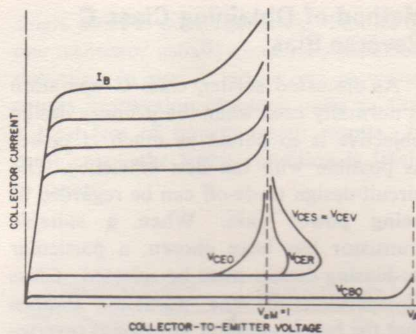

Fig. 7 - Typical collector-characteristics curves showing primary breakdown voltages.

V_{CES} is the limiting condition. Any resistance added in series with the base-emitter junction of the transistor causes the breakdown voltage to vary between V_{CES} and V_{CEO}; the limiting breakdown voltage is then indicated as V_{CER}. For class B or class C circuits, the dc supply voltage should not exceed one-half of the V_{CES} or V_{CER} rating. These voltage-breakdown ratings provide a good indication of the safety margin that exists for a given circuit application.

Frequently, a circuit designer exercises all the necessary precautions to avoid voltage breakdown, and failures still occur for no apparent reason. Analysis of damaged transistors rarely indicates the failure mode. Most of the unexplained failures are blamed on a second-breakdown mechanism.[12] In general, second breakdown (S/b) in a junction transistor is a condition in which the output impedance changes instantaneously from a large positive value to a negative value, and then finally to a small positive value, as shown in Fig. 8.

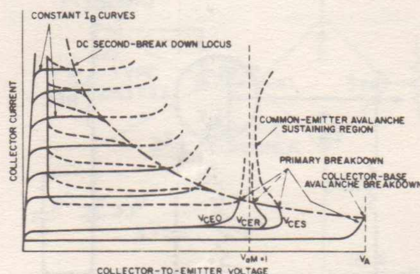

Fig. 8 - Typical collector-characteristics curves showing locus of second breakdown (S/b).

When the load applied to the collector circuit is purely resistive, the dc supply voltage and operating conditions can be adjusted to avoid S/b. As shown in Fig. 9, operation along a resistive load line AB assures that S/b does not occur. In high-frequency operation however, the load may not be purely resistive. Because of the reactance in the tuned output circuit, the load line becomes elliptical, as shown by curve CDE in Fig. 9. The operating point may then swing through the S/b region, and junction breakdown may occur. Most S/b failures occur during the tune-up process, when attempts are being made to obtain the required rf power output from the transistor. For reliable circuit operation, the maximum collector-voltage ratings (including S/b rating) should be sufficiently high to avoid breakdown under conditions of strong reactive loads. The rf power transistor must be capable of withstanding high VSWR under varying load conditions without collector-junction breakdown.

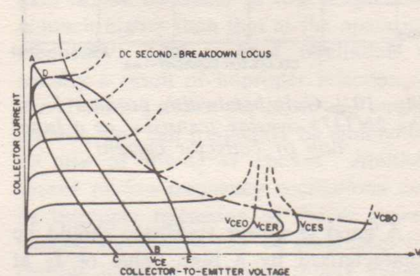

Fig. 9 - Typical collector-characteristics curves showing reactive-load operating point outside of S/b locus.

Peak-Collector-Current Considerations

To provide substantial power output, an rf transistor must be capable of handling high peak collector currents. As mentioned previously, the maximum peak-collector-current rating is usually limited primarily by the practical consideration that the current amplification factor varies approximately inversely with emitter current at high values of emitter-current density. The maximum peak-collector-current rating, therefore, may be established by the amount of reduction in current gain which can be tolerated at high frequencies.

In a practical circuit application, trade-offs in peak collector current are usually a result of other factors such as power

output, power gain, supply voltage and operating frequency.

High-Frequency Current-Gain Figure of Merit (f_T)

The high-frequency current-gain figure of merit f_T is essential in determining the power-gain capability of a practical rf power transistor. The circuit designer uses the f_T value mainly in comparing the power-gain capabilities of various transistors being considered for an application. The f_T of an rf transistor varies with dc emitter or collector current, as shown in Fig. 10.

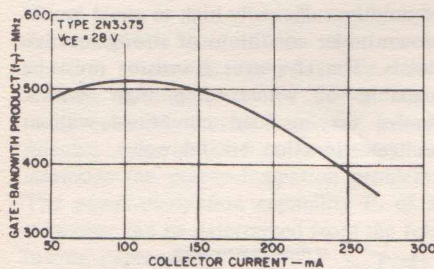

Fig. 10 - Gain-bandwidth product f_T of the 2N3375 overlay transistor as a function of collector current

A good rf power transistor should be characterised by a high value of f_T at high levels of dc emitter or collector current to provide substantial power gain at the operating frequency.

Input and Output Impedance or Admittance Characteristics

Under large-signal conditions, the instantaneous values of the input and output impedances or admittances vary considerably over the range of applied signal level and operating frequency. The circuit designer must know the character of the input and output impedances or admittances as a function of both current and frequency if proper coupling networks are to be designed. In circuits requiring wide bandwidths, the input and output parameters can serve as an indication of the suitability of a particular transistor for the application. Although these characteristics are determined by device design, they can be altered considerably by the source and load conditions imposed on the transistor.

Method of Obtaining Class C Reverse Bias

As discussed earlier, class C operation is normally used when the primary design objective is to obtain as much rf power as possible with the best efficiency. The circuit-design trade-off can be regarded as being power gain. When a suitable transistor has been chosen, a particular dc-biasing circuit must be selected. Class C operation of the transistor implies that the base-to-emitter junction is reverse-biased so that the device is at cutoff when the input signal is zero. There are several methods by which the base-to-emitter reverse bias can be achieved. Fig. 11 shows three methods.

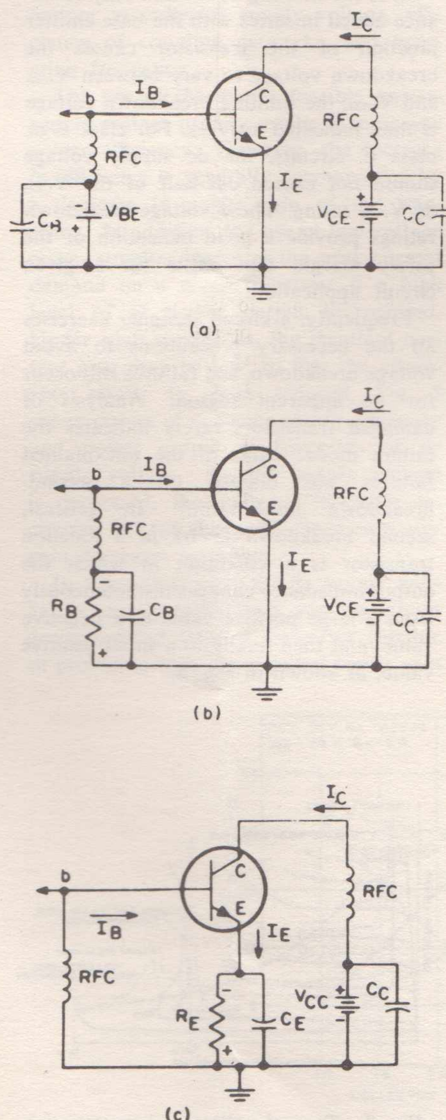

Fig. 11 - Three methods for obtaining class C reverse bias.

In Fig. 11 (a), a dc supply is connected between the base and the emitter with the polarity as indicated. Although this method satisfactorily establishes reverse bias, it requires the use of an additional dc voltage source for the circuit. Because just one dc voltage source is available in most practical circuit designs, other means must usually be employed to obtain reverse bias.

Fig. 11 (b) shows one way in which self-reverse-bias can be obtained. A resistor R_B is inserted in the base circuit. The dc base current flowing through this resistor establishes a reverse bias voltage between the base and emitter junctions. Although this method effectively produces the reverse bias, the value of R_B must be selected with great care; too large a value can reduce the collector-to-emitter breakdown voltage significantly.

Fig. 11 (c) shows the best method of obtaining reverse bias for a class C stage. In this circuit, a resistor R_E is inserted in the emitter lead. Although obtaining reverse bias in this manner does not effect the collector-to-emitter breakdown voltage, the resistor R_E must be properly bypassed by a capacitor C_E to eliminate any degenerative effects on transistor power gain. At higher frequencies, it is rather difficult to obtain total bypassing with a capacitor because of its lead inductance. However, the leads of the capacitor can be cut to such a length that they form a series resonant circuit with the capacitor at the desired operating frequency. This method of obtaining total rf bypassing is extremely effective, but may be restrictive to bandwidth requirements.

Parallel Operation of Power Transistors

In some applications, more power is required than can be provided by a single transistor. (The increase in required power output may be the result of design trade-offs imposed for maximum reliability and stability reasons.) One solution which is widely used is the parallel operation of transistors. RF power transistors can be directly paralleled at a single point, as shown in Fig. 12 (a). In this arrangement, however, the transistors must be matched for power gain at the desired frequency to obtain good load sharing. In addition, the reduction in both input and output impedances makes it more difficult to minimize circuit losses.

Fig. 12 (b) shows another method of paralleling transistors at high frequencies. In this circuit, a separate input network is provided for each base, and the inputs are combined at a higher-impedance point to reduce input-circuit losses. The balancing circuit in the base of transistor T_1 allows the input drive to be divided equally between the two transistors. The emitter resistors R_E provide a means for monitoring the emitter currents of the units.

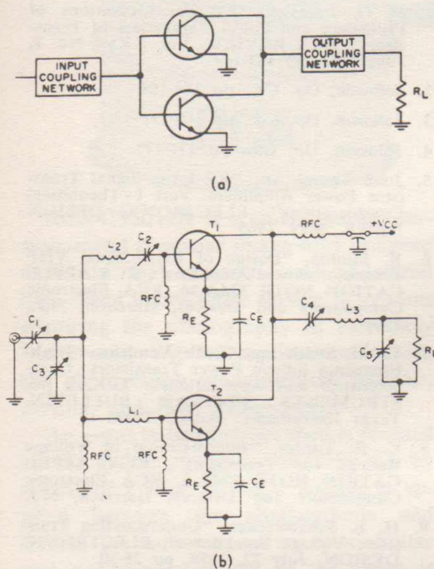

Fig. 12 - Two methods for parallel operation of power transistors.

It has been found experimentally that the paralleling of several transistors at a single point usually results in a reduction in the total power output. For example, paralleling two units results in an output slightly less than twice that expected from a single unit. Fig. 13 shows the paralleling efficiency of RCA Dev. No. TA2675 transistors operated at 300 MHz. The practical paralleling efficiency is always less than 100 per cent even with carefully matched transistors, primarily because it is difficult to maintain perfect symmetry in the circuit arrangement. Currents flowing into and out of the transistors may not be equal. Although special circuit-balancing techniques can be used, circuit design becomes complex and circuit tuning is difficult to achieve.

Another disadvantage of direct paralleling of a large number of transistors at a single point is poor reliability. Failure of one transistor usually causes a substantial reduction in power output or, at worst, causes destruction of other units so that a total loss of power output results. In most cases, the worst condition is likely to occur.

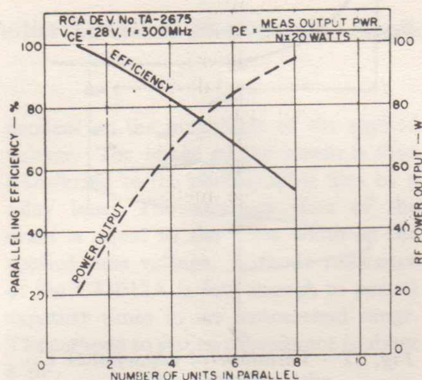

Fig. 13 - Paralleling efficiency and power output of the RCA Dev. No. TA2675 as a function of the number of units in parallel.

One approach to assuring good reliability in parallel operation is shown in Fig. 14. This system takes advantage of the isolating properties of hybrid networks.[13]

The 7-watt input signal is amplified to a level of 22 watts and fed into a hybrid power divider. The output power from the hybrid is split equally and fed into two separate amplifiers, each of which contains two transistors in parallel. The 38-watt output signals from the separate power amplifiers are led into a second hybrid and recombine to produce 70 watts of power to the load. Because of the isolating properties of the hybrid power combiner, a failure of one amplifier reduces the total power output, but does not cause failure of the other amplifier.

The system shown in Fig. 14 requires the use of additional components and a certain amount of redundancy. The increased number of components may be the necessary design trade-off to assure maximum circuit operating reliability.

Frequency Instability in RF Power Amplifiers

Frequency instability often occurs even though the common-emitter circuit is used. Perhaps the most troublesome type of frequency instability in an rf transistor power amplifier is low-frequency oscillations. Such oscillations occur because the gain of the transistor at low frequencies is much higher than that at the operating frequency. This type of oscillation is usually a result of improper selection of the rf chokes within the input and output circuits, and can frequently be eliminated by use of low-Q rf chokes. Another source of low-frequency oscillations can be improper bypassing of the dc power supply; this source can be eliminated by careful selection of power-supply bypass capacitors. It may be necessary to provide separate capacitors for high and low frequencies, as shown in Fig. 15.

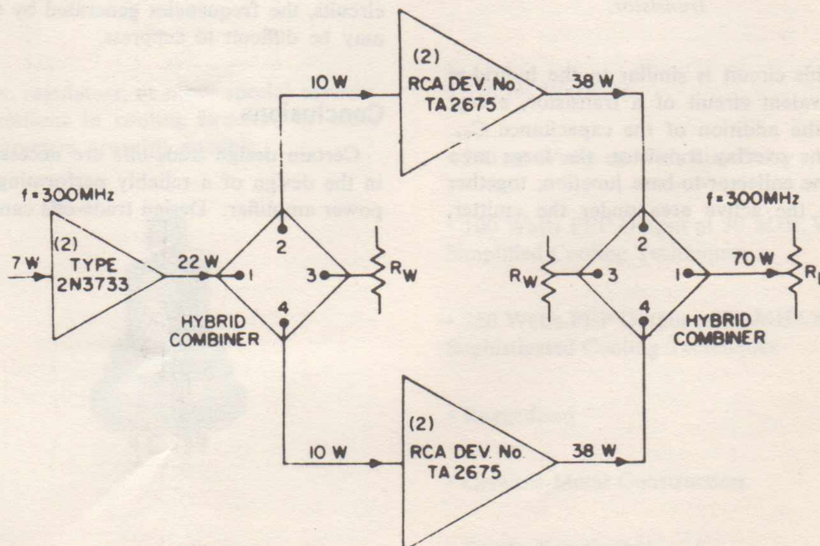

Fig. 14 - System of parallel operation using hybrid combiners.

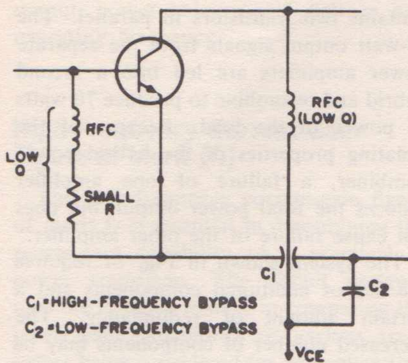

Fig. 15 - Circuit showing method for bypassing the power supply to eliminate instability.

Another type of frequency instability which can occur is parametric oscillations. These oscillations are usually produced by the nonlinear collector-to-base junction feedback capacitance C_{bc}. Fig. 16 shows the simplified equivalent circuit of an overlay transistor.[14]

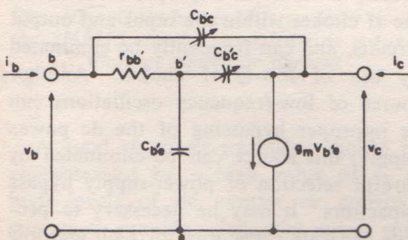

Fig. 16 - Equivalent circuit of an overlay transistor.

This circuit is similar to the hybrid-pi equivalent circuit of a transistor, except for the addition of the capacitance C_{bc}. In the overlay transistor, the large area of the collector-to-base junction, together with the active area under the emitter, results in a relatively high collector-to-base capacitance. Because this capacitance is usually much larger than the capacitance C_{bc}, it must be included in the equivalent circuit together with parameters defined by the hybrid-pi circuit.

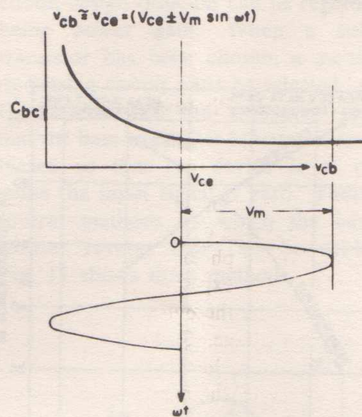

Fig. 17 - Variation of capacitance C_{bc} with collector voltage.

The capacitance C_{bc} varies non-linearly with the transistor collector voltage, as shown in Fig. 17. If a sinusoidal voltage such as that shown is developed in the collector output circuit, the capacitance C_{bc} contains components of both the fundamental frequency and harmonic frequencies because of the non-linear charge-voltage characteristics of the capacitance. The harmonic currents produced by C_{bc} can circulate in the output circuit and cause unwanted output signals. The harmonic currents can be reduced by designing the output circuit to have a high loaded Q. In broadband circuits, the frequencies generated by C_{bc} may be difficult to suppress.

Conclusions

Certain design trade-offs are necessary in the design of a reliably performing rf power amplifier. Design trade-offs can be applied to both the amplifying device and the circuit. The device-design trade-offs which can be made are related to frequency, voltage, current and power. The circuit-design trade-offs are associated with power output, power gain supply voltage, operating frequency and circuit stability. How well these trade-offs are applied both to the amplifying device and to the circuit determines the ultimate performance and reliability capabilities of a solid-state rf power amplifier.

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NEWS & New Releases

BI-PLANAR IMAGE TUBE

Monovoltage Type for Extremely Fast Shutter Service in Photographic Application

RCA-C33012A is a small, sturdy, ceramic-metal bi-planar image tube designed expressly for research and industrial high-speed light-shutter service in systems requiring the photography of extremely fast events. Typical applications include the photography of detonation, ballistic, plasma, and laser phonomena.

An event to be photographed is focused on the photocathode of the C33012A by means of a lens. When a voltage is applied between the photocathode and screen, the tube acts as an open shutter and a luminous image of the event is produced on the phosphor screen. The brightness of this screen image is dependent on the magnitude of the applied voltage. The image on the screen is then transferred to the photographic film by a relay lens. The exposure time of the event is equal to the pulse width of the applied tube voltage. Cathode resistance of the C33012A is low enough to permit exposure times in the nanosecond range. The cathode to screen capacitance is about 8 pF.

Precise alignment and close spacing between the photocathode and phosphor screen of the C33012A provides uniform resolution from centre to edge and eliminates distortion. Typical resolution is 25 line-pairs per mm at 12 kV with incandescent light on the photocathode. Resolution is a function of tube voltage and the wavelength of incident light.

The C33012A employs an S-11 photocathode having a resistivity of less than 250 ohms per square at 22° C and an aluminized P11 phosphor screen. The screen cutoff ratio for this tube is above 1 x 10^5.

Features

- Typical Centre and Edge Resolution of 25 line-pairs per mm at 12kV with incandescent light on photocathode.
- Designed for Shuttering with Pulse Voltages of 12 to 15kV and Pulse Widths as Low as 5 nanoseconds
- Screen to Cathode Capacitance of About 8 pF
- Photocathode Resistivity of Less than 250 ohms per square at 22° C
- No Distortion Within 1.4" Screen Diameter
- Screen Cutoff Ratio Above 1 x 10^5
- Flat Input and Output Windows
- Aluminized P11 Phosphor Screen
- S-11 Spectral Response
- Ceramic-Metal Construction

BEAM POWER TUBE

RCA-Dev. No. A2814 is a very small, low-cost conduction-cooled beam power tube designed specifically for applications where dependable performance under severe shock and vibration is essential. It is rated for use as an rf linear amplifier.

The A2814 features a unique filamentary cathode that enables the user to achieve useful power in less than 250 milliseconds. This extremely fast warm-up is achieved with simple fail-safe circuits.

The A2814 and variants of its basic design may also be useful in applications such as rf power amplifiers or modulators, rf power amplifiers or oscillators, hard-tube modulators, rf power amplifiers, regulators, or other special services. Variations in cooling structure or other parameters are also possible.

- 350 ms Warm-up
- 250 ms Warm-up With Bias Delay
- 100 Watts PEP Output at 30 MHz With Simplified Cooling Techniques
- 250 Watts PEP Output at 30 MHz With Sophisticated Cooling Techniques
- Ruggedized
- Ceramic-Metal Construction
- Conduction Cooled

PRACTICAL AND USABLE METHODS FOR EVALUATING THERMAL RUNAWAY IN TRANSISTOR AUDIO OUTPUT STAGES

By M. S. FISHER Radio Corporation of America

Mathematical derivations expressing thermal runaway in terms of basic device parameters are generally quite complex and inaccurate. For this reason, many designers of transistor circuits are not aware of the relative importance of the various factors which determine the junction temperature at which thermal runaway will occur. As a result, a designer may check out an amplifier experimentally to determine whether it operates under the specified set of conditions, but he will be totally unaware of the safety margin involved.

This Note describes a usable and practical method for evaluating and even calculating thermal runaway. The analysis is based on a set of experimental data for a given circuit. The results of the analysis show the effects of various parameters on thermal runaway, and thus permit the designer to evaluate the relative safety margin of a particular circuit design.

Causes of Thermal Runaway

The basic concept of thermal runaway can be described as follows. As ambient temperature increases, the junction temperature of a transistor increases as a direct result of the external temperature rise. However, the higher junction temperature also causes an increase in transistor dissipation which, in turn, results in a change in temperature rise between junction and ambient. The total effect can be compared to a closed-loop system in which an induced change in junction temperature causes a change in dissipation, which causes a change in the temperature rise between the junction and ambient, which then causes a further change in junction temperature.

If the increase in junction temperature causes sufficient increase in dissipation (i.e., if the rate of change of dissipation is high enough with respect to junction temperature) so that the resulting temperature rise is equal to or greater than the original change in junction temperature, then no further external temperature change is required for continued increases in junction temperature, and thermal runaway occurs. This condition is similar to an electrical positive-feedback system that has a loop gain of unity. If the loop gain is less than unity (i.e., if the increase in temperature rise is less than the induced change), the junction temperature increases more than the ambient temperature, but a stable equilibrium point occurs.

Experimental Analysis

To determine whether the loop gain is high enough to initiate runaway, it is necessary to know two factors: (1) the rate of change of dissipation with respect to junction temperature, and (2) the change in temperature rise which results from a given change in dissipation. The second factor can easily be determined as the product of the increase in power dissipation P_C and the thermal resistance Θ. Under dc conditions, the first factor can be determined from the collector-to-emitter voltage (assumed constant in an output stage where dc resistance is negligible) and the transfer characteristic between collector current and junction temperature. This transfer characteristic is a function of the circuit configuration, component values, and device parameters (such as common-emitter current transfer ratio β, collector-cutoff current I_{CO}, base-to-emitter voltage V_{BE}, and others).

The difficult and inaccurate part of the analysis occurs when an attempt is made to develop this transfer characterstic from the theory. However, the transfer characteristic can be determined experimentally if the circuit under consideration is operated at a low collector-to-emitter voltage V_{CE} to avoid dissipation and the case temperature T_C is varied (in an oven or heat controller) to provide the desired values of collector cur-

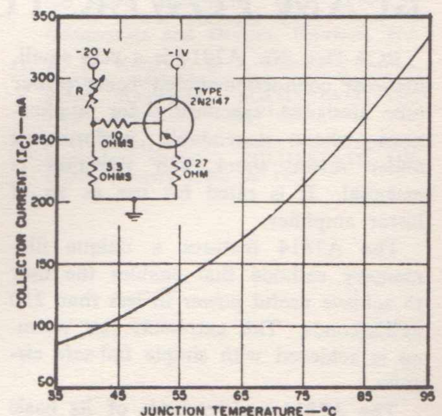


Fig. 1 - Transfer characteristic of typical output-stage dc bias arrangement plotted on linear co-ordinates to illustrate non-linearity.

rent I_C as a function of junction temperature T_J.

Fig. 1 shows a transfer characteristic determined experimentally for a typical output-stage dc bias arrangement using a 2N2147 transistor. The curve is plotted on linear coordinates to illustrate the non-linearity of the transfer characteristic. At low junction temperatures, the slope (or change in I_C for a given change in T_J) is small. As junction temperature increases, the slope increases, and thus the loop gain also increases.

When the curve of Fig. 1 is re-plotted on semi-log graph paper, as shown in Fig. 2, it can be seen that the transfer characteristic is a pure exponential over the range of interest. (This relationship exists because of the exponential nature of collector current I_C as a function of base-to-emitter voltage V_{BE} and the exponential nature of collector-cutoff current I_{CO}.) For the curve in Fig. 2, collector current doubles for every increase of 30°C in junction temperature.

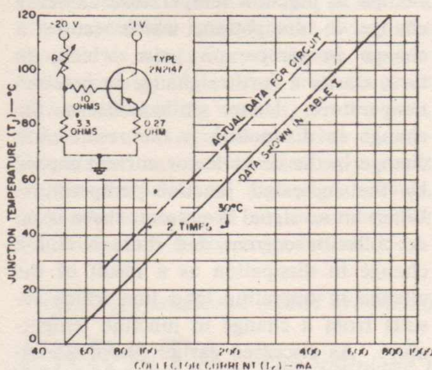


Fig. 2 - Transfer characteristic of Fig. 1 re-plotted on semi-log paper.

The junction temperature at which thermal runaway will occur can be determined for dc operating conditions by use of a chart such as that shown in Table I. For example shown, the collector current I_C is assumed to be 0.1 ampere at a junction temperature T_J of 30° C. The transfer characteristic is assumed to be parallel to that obtained in Fig. 2 (i.e., to have the same slope so that I_C doubles for every change of 30° C in T_J). Data for T_J and I_C are given in Columns 1 and 2, respectively. Column 3 shows the collector dissipation P_C, which is equal to the current I_C (from Column 2) times the collector-to-emitter voltage V_{CE} (assumed to be 20 volts in the example). Column 4

TABLE I — CHART FOR DETERMINING THERMAL-RUNAWAY POINT
($I_C = 0.1$ A at $T_J = 30°C$; $\Theta = 5°C/W$; $V_{CE} = 20$ V)

	Column 1 Junction Temperature T_J-°C	Column 2 DC Collector Current I_C-A	Column 3 DC Collector Dissipation P_C-W	Column 4 Temperature Rise $T_{J-\infty}$-°C	Column 5 Temperature at Infinity $T_{J-\infty}$-°C	Column 6 $\frac{\Delta T\infty}{\Delta T_J}$
Row 0	0	0.05	1	5	−5	—
Row 1	30	0.1	2	10	20	+25/30
Row 2	60	0.2	4	20	40	+20/30
Row 3	90	0.4	8	40	50	+10/30
Row 4	120	0.8	16	80	40	−10/30

shows the temperature rise between the junction and infinity, $T_{J-\infty}$ which is equal to the dissipation (from Column 3) times thermal resistance from junction to infinity, $\Theta_{J-\infty}$ (assumed to be 5°C/W). The infinity point is defined as the ambient point at which no temperature change results from a change in dissipation.★ Column 5 shows the temperature at the infinity point $T\infty$, which is equal to the junction temperature T_J (from Column 1) minus the temperature rise (from Column 4). Column 6 shows the change in $T\infty$ between a row and its preceding row divided by the corresponding change in T_J. For example, $T\infty$ increases by 20°C from Row 1 to Row 2, while T_J increases by 30°C; therefore, Column 6 for Row 2 is +20/30.

As junction temperature increases, the increase $T\infty$ required to produce a given increase in T_J becomes smaller because the slope of the transfer characteristic increases with junction temperature (i.e., loop gain increases). By the time Row 4 is reached ($T_J = 120°$ C.), $T\infty$ is decreasing for increases in T_J, Column 6 is negative, and runaway has occurred. The point at which thermal runaway occurs is the point at which $\Delta T\infty / \Delta T_J$ in Column 6 is zero. For the data shown in Table I, it can only be determined that this point occurs somewhere between temperatures of 60°C (where $\Delta T\infty / \Delta T_J$ is positive) and 120°C (where $\Delta T\infty / \Delta T_J$ is negative). A closer determination can be made by use of smaller increments between the rows or by mathematical analysis.

Mathematical Analysis

In order to derive an equation for the junction temperature at which thermal runaway occurs, it is necessary first to derive an expression for the transfer characteristic which was plotted from the experimental data. Such an expression is derived in Appendix I-A* for a pure exponential in terms of D, the number of degrees required to double the current. The current I_0 at zero junction temperature can be determined by extrapolation of the curve to zero or by solution for I_0 at known values of I_C and T_J. For the data plotted in Fig. 2, the value of D is 30°C and the value of I_0 is 0.05 ampere. The collector current I_C is then given by

$$I_C = 0.05\ e^{(0.69)(T_J)/30} \qquad (1)$$

It should be noted that D is the slope of the exponential curve plotted on semi-log paper, as shown in Fig. 2. If D is not a pure exponential (i.e., varies with junction temperature), the value of D is obtained from the slope of the curve at the junction temperature of interest.

As discussed in connection with Table I, the point at which runaway occurs can be determined by use of smaller and smaller increments of T_J until the following condition is reached:

$$\lim_{\Delta \to 0} \frac{\Delta T\infty}{\Delta T_J} = 0 \text{ or } \frac{d\,T\infty}{d\,T_J} = 0$$

When this definition is used for thermal runaway and zero collector resistance is assumed, an expression can be derived for the junction temperature at which thermal runaway occurs, T_{JR}. This expression, which is derived in Appendix I-B*, is as follows:

$$T_{JR} = \frac{D}{0.69} \ln \frac{D/0.69}{I_0 \Theta_{J-\infty} V_{CE}} \qquad (2)$$

For the data shown in Table I, the following solution is obtained by use of this equation:

$$T_{JR} = \frac{30}{0.69} \ln \frac{30/0.69}{(0.05)(5)(20)} = 94°C.$$

Effects of Changes in Various Parameters

Examination of Eq.(2) reveals that idling current I_0, collector-to-emitter

★ *It should be noted that the infinity point is not the ambient in the immediate vicinity of the device, especially if the device is enclosed and the air is still, because the immediate ambient temperature can change as a result of dissipation. A runaway problem can exist when an amplifier is placed in a closed environment because of the high thermal resistance to infinity.*

voltage V_{CE}, and thermal resistance $\Theta_{J-\infty}$ all have the same effect. Therefore, if the values of two or more of these parameters are changed but the product of the three remains the same, the value of T_{JR} does not change. For example, in a given circuit with fixed values of D and $\Theta_{J-\infty}$, the voltage could be doubled if the idling current were cut in half, and the runaway temperature would not change.

The factor D appears in two places in the numerator. A higher value of D (more junction-temperature change required to double the collector current) results in a higher value of T_{JR}, as would be expected for a circuit with a higher stability factor. However, if a circuit that has a higher value of D is operated near the limit of its thermal-runaway capability, greater variability results from changes in I_0, $\Theta_{J-\infty}$, or V_{CE}. This effect can lead to smaller safety margins for high line voltages, component tolerances, and the like for a circuit that has a better stability factor. Reasons for this effect are discussed below.

Appendix I-C* derives equations that show the effect on T_{JR} of changes in the various parameters in Eq.(2). These equations are used below to illustrate the effect of changes of a factor of two from the original condition:

If the value of D is doubled, the new value of T_{JR} is given by

$$T_{JR2} = 2(T_{JR1} + D_1) \quad (3)$$

That is, T_{JR} increases by more than two times.

If the product $I_0\Theta_{J-\infty}V_{CE}$ is doubled (by changes in any or all of the three parameters), the new value of T_{JR} is given by

$$T_{JR2} = T_{JR1} - D \quad (4)$$

That is, a change by a factor of two in $I_0\Theta_{J-\infty}V_{CE}$ (possibly as the result of a change of $\sqrt[3]{2} = 1.26$ in each parameter) decreases T_{JR} by D°C.

As an example, it is assumed that two circuits have similar T_{JR} values of 100°C, but different D values of 30°C and 60°C (the latter circuit must have a higher $I_0\Theta_{J-\infty}V_{CE}$ product to provide a T_{JR} of 100°C). In either circuit, the $I_0\Theta_{J-\infty}V_{CE}$ product could change by a factor of two as a result of supply-voltage variations or a change in thermal resistance resulting from (1) transistor tolerances, (2) improper connection to the heat sink, or (3) location of the circuit in a crowded environment.

Because the value of T_{JR} decreases by D degrees in either case, in the circuit where D was originally 30°C the value of T_{JR} becomes 70°C. In the "more stable" circuit where D is 60°C, however, T_{JR} is reduced to 40°C. This example illustrates the fact that a circuit cannot be judged for stability by the D factor alone. Only a complete analysis in terms of thermal runaway under "worst-case" conditions reveals the actual safety margin.

(It will be shown later that, of the two circuits in the example, the one that has the higher value of D will also "run away" at a lower ambient temperature. This result emphasizes that the analyses must be carried to a solution for ambient temperature before a true evaluation of the thermal capability is achieved.)

DC Conditions for Thermal Runaway

Appendix I-D* shows how T_{JR} can be eliminated from the equations to provide an expression for the operating conditions at the point where thermal runaway occurs. As shown, the point of thermal runaway is reached for the following conditions:

$$\Theta_{J-\infty}I_C V_{CE} = T_{RR} = D/0.69 \quad (5)$$

In other words, thermal runaway occurs if the temperature rise due to direct current and voltage equals the D/0.69 factor. It should be noted, however, that the collector current I_C in this equation is the value obtained when the junction temperature has increased to T_{JR}. It may take some time, even hours, for the temperature (and thus the collector current) to rise to this value and for runaway to occur. It is desirable, then, to determine what dc conditions must exist at the time of initial turn-on to cause eventual increase of the junction temperature to T_{JR} and thus to cause runaway. Appendix I-E* derives this condition for the assumption that there is no temperature rise at the first instant (because of the thermal capacitance) so that the junction temperature is equal to the ambient temperature. The result shows that the initial (t = 0) dc conditions required to cause eventual thermal runaway (when there is **no** change in ambient temperature) are given by

$$V_{CE}\, I_C\, (t=0) = \frac{D}{(0.69)\,(e)\,(\Theta_{J-\infty})} = \frac{D}{(0.69)\,(2.72)\,(\Theta_{J-\infty})}$$

It should be emphasized that this expression can not be used if the ambient temperature changes. It can be used only if the dc conditions at time zero are measured at the maximum expected ambient temperature. Even under these conditions, the expression does not give an indication of the safety margin in terms of changes in the ambient temperature.

The ambient temperature which produces thermal runaway under dc conditions, T_{AR}, can be determined by combination of Eqs.(2) and (5), as follows:

$$T_{AR} = T_{JR} - D/0.69 \quad (7)$$

This ambient temperature, T_{AR}, is of most concern to the circuit designer. Eq.(7) shows that T_{AR} is lower than T_{JR} by 0.69 degrees under dc conditions.

AC Conditions

Although only dc operating conditions have been considered thus far, the results of the dc analysis can also be used for analysis of an audio output stage that develops ac power. Two types of audio output stages are discussed below, a single-transistor class A output stage and a two-transistor push-pull class AB output stage.

As mentioned previously, thermal runaway, in its fundamental form, is a closed-loop phenomenon in which an induced change in junction temperature causes a change in dissipation, which causes a change in temperature rise which, in turn, causes a further change in junction temperature. Under dc conditions, the change in dissipation is the result of a change in the dc collector current caused by the increased junction temperature. When an ac signal is present, there is no dc collector current, but there is still a change in dissipation as a result of the change in operating load line which results from a change in junction temperature. As discussed earlier, thermal runaway occurs when the rate of change of dissipation with respect to junction temperature becomes great enough for the loop gain to become unity. Therefore, if the rate of change of collector dissipation with respect to junction temperature is different under ac conditions than under dc conditions, the temperature at which runaway occurs is also different. In both class A and class AB operation, however, the "worst-case" conditions occur during dc (idling) conditions. As a result, both Table I and Eqs.(1) through (7) can still be used.

In a class A output stage, dissipation is always highest when there is no ac power output. For this dc condition, therefore, the equations may be directly applied. For experimental verification, a class A output stage should be checked out by increasing the ambient temperature while the output stage is idling.

Eq. (4) shows that T_{JR} decreases by D°C. when the product $I_C\Theta_{J-\infty}V_{CE}$ is increased by a factor of two. Under dc conditions, this lower junction temperature reduces the idling current to half the original value (because current doubles every D degrees), with the net result that the temperature rise at the new value of T_{JR} remains the same [see Eq.(5)]. In a class A amplifier, therefore, a decrease of D degrees in T_{JR} causes a decrease of D degrees in T_{AR}, the ambient temperature required to cause thermal runaway.

In a two-transistor class AB push-pull output stage, two factors make the analysis more complex. First, maximum dissipation occurs at decreasing signal levels as idling current increases toward class A push-pull. Second, the rate of change of dissipation with junction temperature at high signal levels is very low. (These relationships can be demonstrated by drawing the different load lines that occur at different idling currents and performing the integrations necessary to find average power.)

Two cases must be considered for the two-transistor class AB stage. In the first case, operation is such that, when the junction is near T_{JR} maximum dissipation occurs at high signal level (because of low initial idling current). In this case, the value of T_{JR} calculated from dc considerations may be exceeded as a result of the dissipation at high signal levels, and yet runaway will not occur because the dissipation is less regenerative. However, if the signal is cut off and operation returns to dc while the junction temperature is higher than T_{JR}, thermal runaway will occur. In other words, thermal runaway can be made to occur if the ambient temperature is increased, some power is dissipated at high signal levels to heat the junction above T_{JR}, and the signal is then cut off to return the stage to dc conditions.

In the second case, operation is such that, when the junction is near T_{JR}, maximum dissipation occurs during idling (because of high idling current). In this case, maximum temperature rise occurs during idling and operation is as discussed for the class A stage. Therefore, runaway is made to occur simply by increasing the ambient temperature.

In either case, runaway occurs at the dc condition, and Table I or Eq.(2) may be used to determine T_{JR}. In the first case, however, the effective ambient temperature (which is the ambient temperature listed in Table I) is much greater than the actual external ambient temperature because of the temperature rise caused by the non-regenerative dissipation. The actual external ambient temperature T_{Aext} is determined as follows:

$$T_{Aext} = T_{JR} - P\,\Theta_{J-\infty} \qquad (8)$$

where P is the non-regenerative maximum dissipation at the high signal level.

Because operation of a class AB stage may be as described for either case, experimental verification involves the following tests. First, the ambient temperature is increased in steps. At each step, temperature is brought to equilibrium (provided runaway does not occur). Next the signal level is varied to determine the signal which causes the highest dissipation (the signal level required may change slightly as heat-sink temperature changes). If temperature equilibrium is obtained, the signal is then cut off and the idling current is observed for a decrease (stable) or an increase (unstable).

In either of the two cases described, when T_{JR} is decreased by D degrees as a result of increasing the product $I_O\Theta_{J-\infty}V_{CE}$ by a factor of two, as in Eq.(4), the external ambient temperature required to cause T_{JR} to be reached also decreases by D degrees. In the first case, Eq.(8) shows that T_A must change by the same number of degrees as T_{JR} because $P\Theta_{J-\infty}$ is a constant. In the second case, the analysis is the same as for the class A stage because dc conditions exist.

Appendix II* shows sample calculations for the various conditions described.

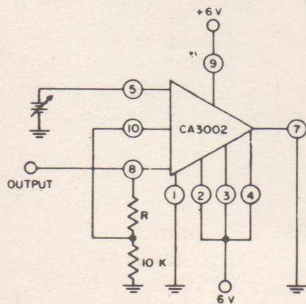
Conclusion

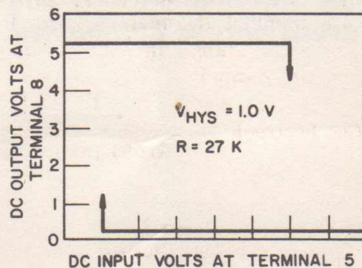
The table and equations in this note describe thermal runaway under dc conditions. Table I can be used even if collector resistance is present; however, the equations are valid only for zero collector resistance. In either case, the concept described can be applied to an entire system analysis because the results are based on an experimental D factor for the system rather than a set of equations describing the system. The use of this D factor makes the analysis accurate and practical.

**Note—Appendices I and II are included in RCA Application Note AN-3191 available free on request from Sales Dept., AWV.*

ERRATA: *The following is the conclusion to the article "Application of the RCA-CA3002 Integrated Circuit IF Amplifier" appearing in the November, 1966, issue of Radiotronics.*

Schmitt Trigger. Fig. 18 shows the use of the CA3002 as a Schmitt trigger. In this application, the input is applied to terminal 5 and both the output and the feedback are taken from the output emitter-follower at terminal 8. The emitter-follower output isolates the feedback loop from the differential pair and makes it possible for the circuit to drive low-impedance loads. An additional advantage is that neither half of the differential pair saturates as the resistance of the feedback loop is varied. Fig 18 also shows the output swing and associated hysteresis of the Schmitt trigger as a function of resistor R and the dc input voltage level at terminal 5.





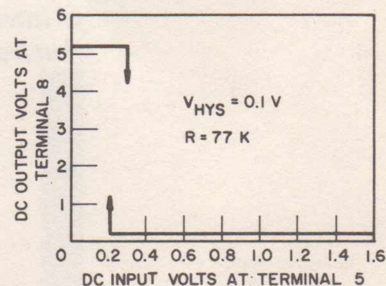
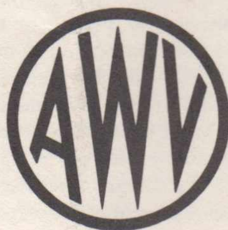


Fig. 18—Schmitt trigger circuit and output swing and associated hysteresis.



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