ELECTRONIC COMPONENTS & APPLICATIONS

Philips Components

PHILIPS

Electronic components & applications

Volume 10, No.1

During the 1980s, most electronic companies made technological innovation top priority for competitive success. And many supported this idea with massive investments in R&D in a desperate effort to grab and maintain the leading edge. Though the basis of their beliefs seemed sound, in many instances they ignored one vital fact. That technological advancement must be geared to meeting customer needs in the marketplace. As a result, many exciting and highly expensive projects ultimately foundered simply because at the end of the day there was no market for the final product. Current thinking, with the lessons of the 80s in mind, appears to have moved away from this idea and puts other factors high on the list of priorities. Factors like organizational excellence, product quality and customer knowledge and service. Technological innovation must, of course, still feature, but not as an end in itself. Otherwise it could end up like a Trojan Horse, insidiously draining our resources and undermining our strengths. And like the Trojans of old, we too could be driven to extinction.

(Photo: N. Koudis, Benelux Press B.V.)

Contents

Full-wave sensorless drive ICs for brushless DC motors

DOMINIQUE POUILLOUX

As their name suggests, permanent-magnet brushless DC motors have neither a mechanical commutator nor brushes; instead, they have a wound stator and a permanent-magnet rotor. So there's no brush wear or arcing, they're very efficient and capable of rapid acceleration and high-speed operation. These features make brushless DC motors a very attractive choice for a host of applications in the computer, home entertainment and automotive industries. However, the appeal of such features is somewhat diminished because these motors depend on complex electronic commutation and need expensive rotor position monitors using magnetoresistive or Hall-effect sensors.

Our TDA514x range of single-chip, highly-integrated drive circuits not only restores the appeal of 3-phase brushless DC motors but considerably enhances it. These ICs provide full-wave power drive to the motor stator windings. Full-wave drive results in higher power density and less torque ripple than can be achieved with half-wave drive.

The commutation timing is determined electronically by the ICs and remains optimum regardless of the type of motor or its load. The need for costly rotor position sensors is eliminated because the commutation timing is determined by internally sensing the zero crossings of the back-EMF generated by the three stator windings during their non-energized periods.

As an additional benefit, all the ICs have a very accurate digital tacho output, and some of them have facilities for generating phase (position) information from a simple, inexpensive external pick-up coil or AC-coupled Hall-effect sensor, as required for monitoring the position of the tape in VCR scanner head motor drives. Also, each IC contains an uncommitted operational transconductance amplifier which can be used for motor speed control by regulating the DC supply to the output driver stages.

All our TDA514x circuits are fabricated with a standard bipolar process, operate from an unstabilized supply of 4 V to 18 V and require very few peripheral components. Power consumption is minimized by using I²L circuitry for performing the logic functions and by adopting adaptive base drive for the transistors in the power output driver stages.

These outstanding features make the TDA514x family an ideal choice for increasing the cost effectiveness and reliability of a wide range of 3-phase brushless DC motors such as those used for driving VCR scanner heads, compact discs, camcorder tapes, computer hard/floppy disks, cooling fans, automotive fuel pumps and blower motors for climate control.

TDA514x RANGE OVERVIEW

Our TDA514x range of drive ICs for brushless DC motors comprises the TDA5140A/AT, TDA5141 and TDA5142T.

The TDA5140A/AT provide 3-phase full-wave drive current of up to 600 mA for brushless DC motors such as those used for driving VCR scanner heads, computer floppy disks, compact discs and camcorder capstans. These ICs also provide accurate speed information without the need for an external sensor and can generate position information from a simple inexpensive external pick-up coil or Hall-effect sensor as required for VCR scanner head drives.

The TDA5141 is an identical but higher power circuit which provides 3-phase full-wave drive current of up to 1.8 A for driving brushless DC motors such as those used in personal computer hard disk drives and cooling fans.

The TDA5142T provides 3-phase full-wave drive current of up to 150 mA for three pairs of external push-

pull bipolar transistors or power MOSFETs. This IC is intended for use with continuously running unidirectional high-current motors for applications such as large computer hard disk drives, automotive fuel pumps/blower motors and industrial applications. It also provides accurate speed information and, additionally, incorporates electronic braking.

THE TDA5140A/AT AND TDA5141 MOTOR DRIVE ICs

The TDA5140A and TDA5141 are pin-compatible and are shown in block form in Fig.1. They are identical except for the 3-phase full-wave drive current they can provide: up to 600 mA for the TDA5140A and up to 1.8 A for the TDA5141. Both are in 18-pin plastic DIL packages with internal heat spreaders. The TDA5140AT is identical to the TDA5140A but comes in a 20-pin plastic SO package for surface mounting.
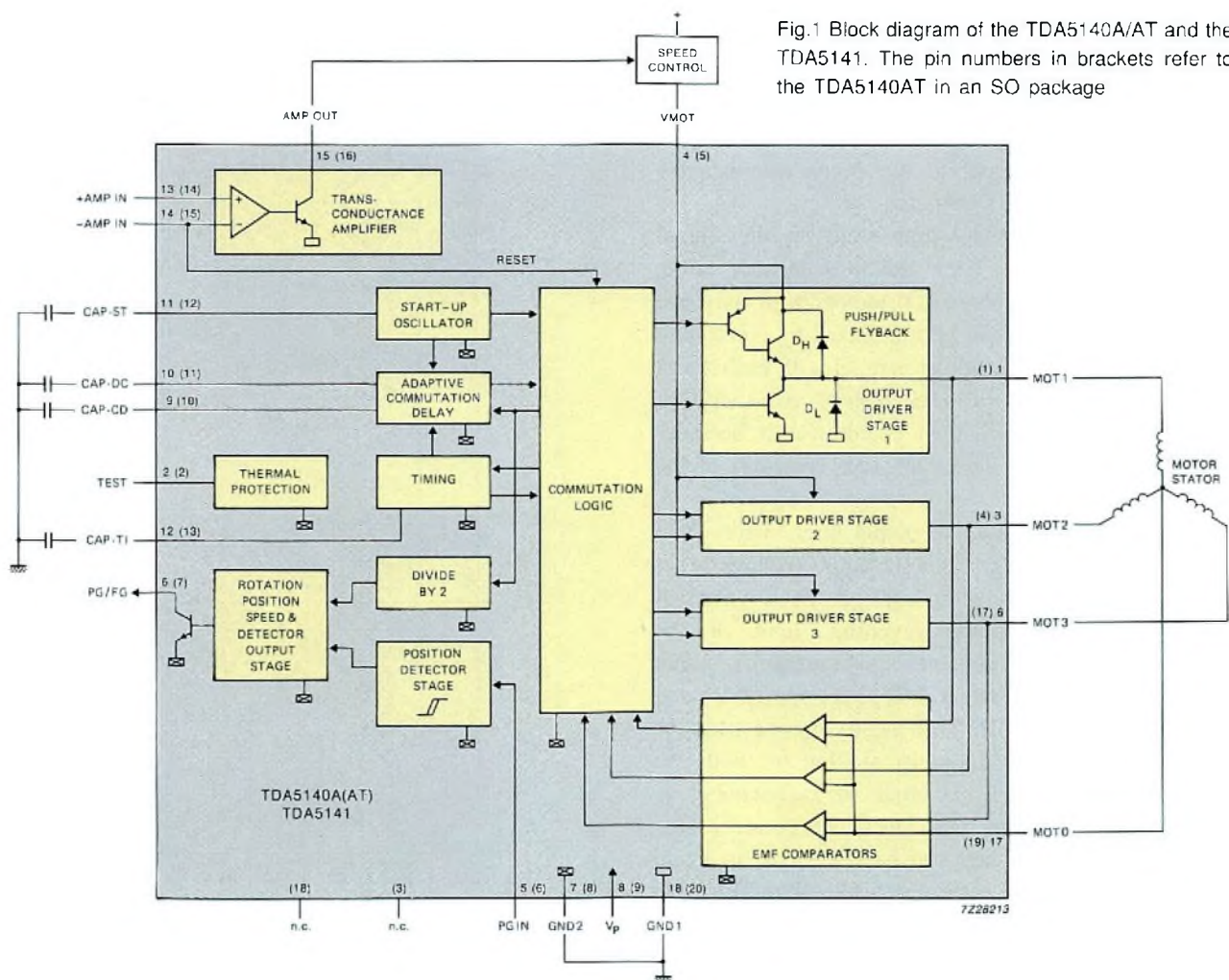

Fig.1 Block diagram of the TDA5140A/AT and the TDA5141. The pin numbers in brackets refer to the TDA5140AT in an SO package

Output driver stages

The three push-pull power output driver stages operate in switch-mode and each have three output states; HIGH for sourcing current, LOW for sinking current and floating (high impedance). They have low saturation voltage (2.1 V at an output current of 500 mA) and incorporate output current limiting and thermal protection of each output transistor. Motor drive outputs MOT0 to MOT3 can be connected to motor stator windings in star or delta configuration. If the stator windings are connected in delta configuration, an artificial symmetry point must be created for connection to the MOT0 pin of the IC by also connecting three 1 kΩ ± 1% resistors in star configuration to the outputs.

Because of the highly inductive load presented by the motor stator windings, the output driver stages of the ICs incorporate anti-parallel collector-emitter diodes for the push-pull output transistors to absorb the energy in the flyback pulses that occur each time the current through a stator winding is switched-off. These diodes can also be used to facilitate electronic braking by using an external switched transistor and resistor connected in parallel with them (between the output driver stage supply pin VMOT and ground pin GND1) to absorb the converted mechanical energy of the motor when it free-runs after switch off. Reversal of the supply to the stator windings for braking purposes is not permitted.

The rapid current/voltage transitions in the output driver stages can cause EMI and/or acoustical noise, especially with axial air-cored coil motors with only one permanent magnet. This can be minimized by connecting a series RC damping network in parallel with each stator winding. However, care must be taken to avoid slowing down the transients to such an extent that it becomes impossible to accurately detect the zero crossings of the back-EMF.

The ICs also incorporate an output reset facility. If a voltage level which exceeds the IC supply voltage by at least 0.7 V (current limited to 200 µA by an external resistor) is applied to the inverting input of the uncommitted operational transconductance amplifier, output MOT1 is set floating, output MOT2 is set LOW and output MOT3 is set HIGH. This facility can be used for pre-positioning the rotor to assist starting or, with the addition of some simple external logic circuitry, to implement a braking function. Once the power output stages have been reset, they can be turned off to avoid continuous dissipation by activating a "sleep" mode of the IC. This is achieved by injecting a current (>600 µA) into the TEST pin.

Thermal protection

Each of the six transistors in the three push-pull output driver stages is thermally protected by circuitry that switches off all six push-pull output transistors if the temperature of any of them exceeds a typical level of 140 °C. The outputs reset when the temperature reduces by 30 °C.

Since approximately pulse-shaped power is dissipated by the IC during motor start-up, this is the most critical period for possibly reaching or exceeding the thermal limits of the IC. The resultant temperature rise during this period is a function of the magnitude and duration of the power pulse, the ambient temperature and the thermal characteristics of the IC package. Figure 2 shows the thermal limits for motor control ICs in DIL18 or SO20 packages. If a particular motor causes the thermal limits of the IC to be exceeded during start-up, a possible cure may be to gradually apply the supply voltage as the motor is started.
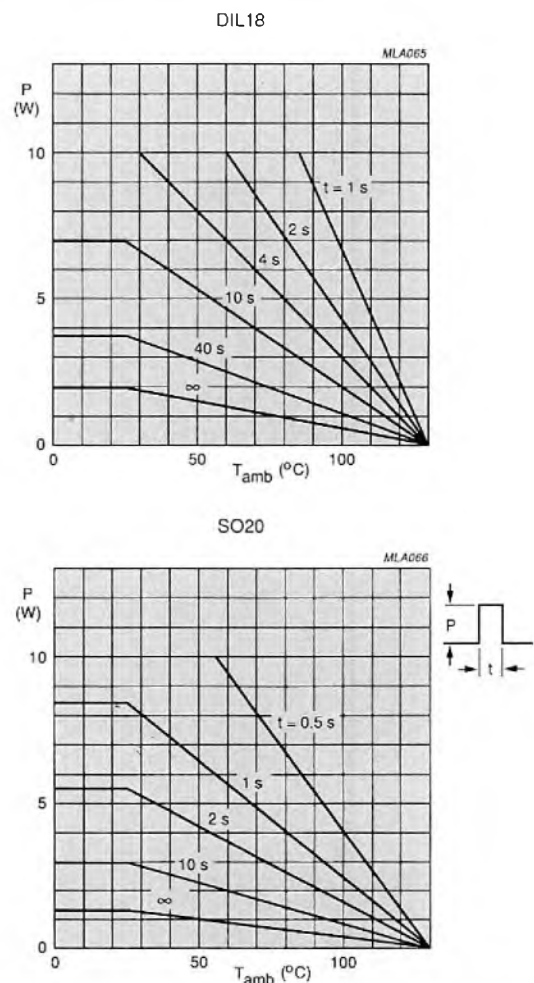

Fig.2 Thermal limits for motor control ICs in DIL18 or SO20 packages

The TEST pin of the IC is used to test the thermal protection function during production. However, it can also be used to activate the "sleep" mode as described under the previous heading.

Commutation

Figure 3 shows that, since the IC has three 3-state output driver stages, there are six possible combinations with each output in a different state: one HIGH for sourcing current, one LOW for sinking current and one in the high impedance (floating) state. The HIGH and LOW outputs conduct the energizing current for two of the (series-connected) stator windings. The floating output presents a high impedance between the commutation logic block and the remaining non-energized stator winding. This allows the zero crossings of the back-EMF it generates to be detected by the associated internal EMF comparator selected by the commutation logic block.

Figure 4 shows that, for each stator phase, commutation consists of a sequence of alternating energized periods separated by a non-energized period during which the zero crossings of the back-EMF occur.

The interval between a zero crossing of the back-EMF and the next energized period (commutation delay) must not exceed 30° of the energizing cycle. This period is defined, dependent on the motor load and speed, by the adaptive commutation delay block. Each interval between two successive energizing half cycles (twice the commutation delay) is measured, halved to obtain the commutation delay, and stored by constant-current charging/discharging of two external capacitors at pins CAP-CD and CAP-DC. The charges on these two capacitors are alternately sampled by the adaptive commutation block to determine the previous commutation delay.

The IC also defines a watchdog time during which back-EMF zero crossing detection is inhibited so that the flyback pulse which occurs after one of the IC outputs has been switched off isn't detected as a "false" zero crossing of the back-EMF. The watchdog time is defined by constant-current charging/discharging of an external timing capacitor connected to the CAP-TI pin of the IC. In fact, the watchdog time serves two purposes, the second of which is described under the next heading.
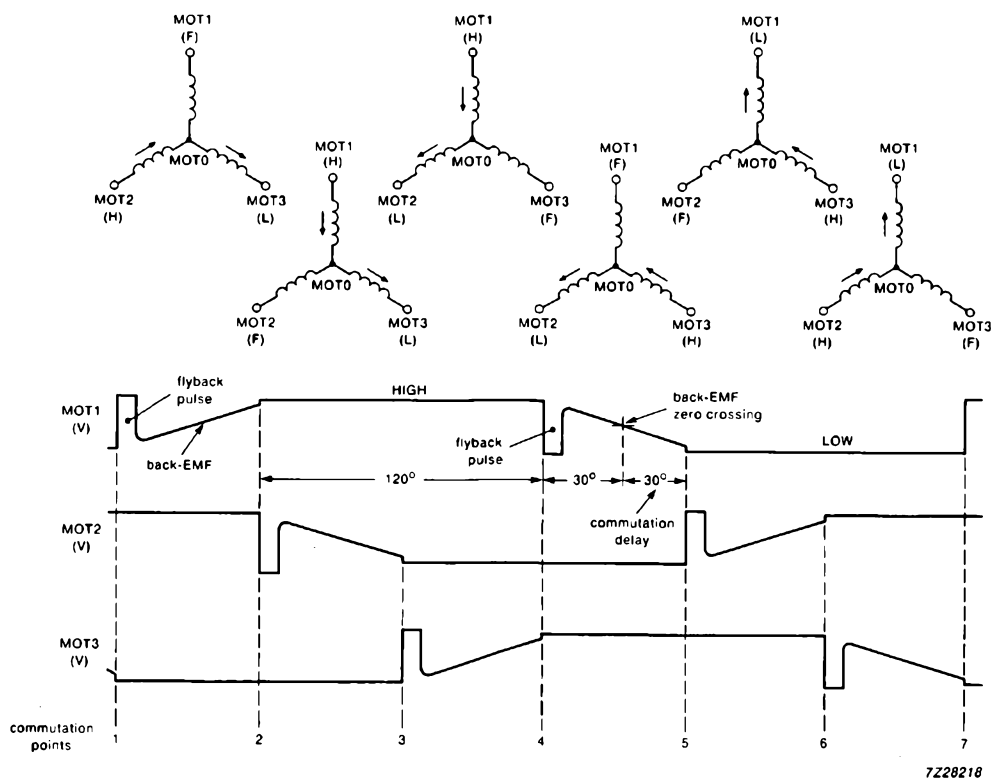

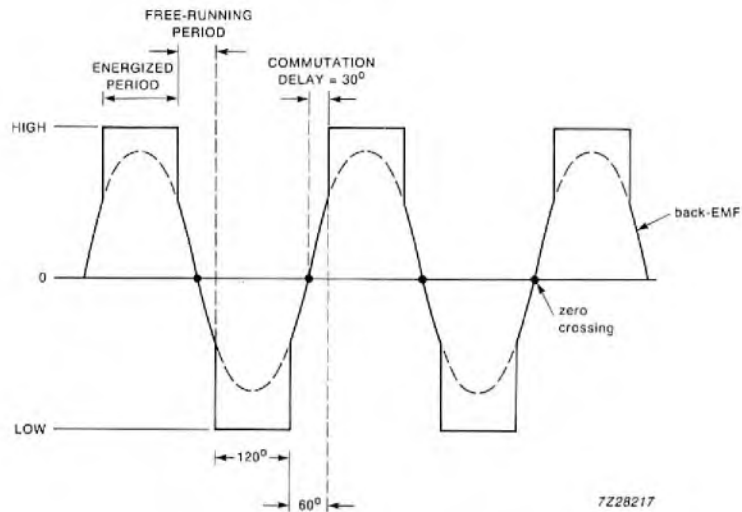Fig.3 The six combinations of IC output states

Fig.4 Commutation for a stator phase

Motor start-up

Because there is no back-EMF from the motor windings to detect at motor start-up, there is a special start-up circuit built into the ICs. A start-up oscillator generates a start-up pulse to set the motor drive outputs of the IC to the next state. The duration of the start-up pulse is determined by the value of a capacitor connected to the CAP-ST pin. The start-up oscillator is disabled as soon as sufficient back-EMF is generated for a zero crossing to be detected (normally running motor).

Dependent on the status of the IC outputs, and the initial position of the rotor relative to the stator, the IC/motor combination reacts to a start-up pulse by either running normally (successful start because sufficient back-EMF is generated) or behaving like a stepper motor (unsuccessful start because insufficient back-EMF is generated). In the latter case, a start-up pulse causes the rotor of the motor to either remain stationary or rotate a single step of 60 electrical degrees and oscillate around its new position.

The IC has the "intelligence" to distinguish whether or not the motor start-up procedure is successful. Part of this "intelligence" is provided by the previously mentioned watchdog time defined by an external capacitor connected to the CAP-TI pin of the IC. The watchdog time has two purposes, the first of which was described under the previous heading. Its second purpose is to define the period allowed following a start-up pulse for detection of a zero crossing of the back-EMF from the motor (normal running). Once this time has elapsed, the three outputs from the IC are set to the next state by another pulse.

Figure 5 shows the starting behaviour of a computer hard disk drive motor controlled by a TDA5141.

The starting procedure can be assisted by using one of the reset facilities of the IC. If the CAP-ST pin of the IC is connected directly to ground before the motor is stopped, and then re-connected to ground via the starting capacitor when rotation has ceased, the rotor will come to rest in a position from which the first start-up pulse will always cause a successful start.
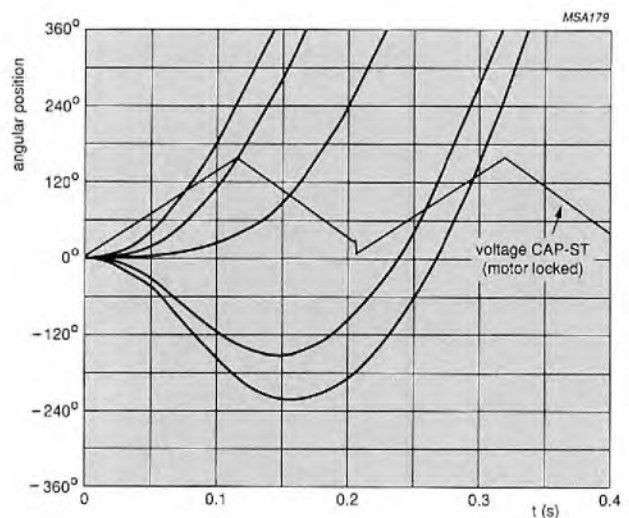

Fig.5 Starting behaviour of a computer hard disk drive motor controlled by a TDA5141

Motor speed and position information

The ICs also use each zero crossing of the back-EMF to generate very accurate digital tacho pulses (FG) without the need for a sensor in the motor. Since each zero crossing of the back-EMF causes an FG pulse transition, the FG tacho pulses have a duty factor of 50% and a frequency of half the commutation frequency. They can be used, for example, to generate interrupts for an external controlling microprocessor.

Some slight inaccuracy (jitter) of the FG tacho pulses can be caused by inaccurate back-EMF from the motor due to unequal angles between the three motor phases. Back-EMF distortion can also be caused by subharmonics (usually half the EMF frequency) due to asymmetry in the electromagnetic circuit of the motor. Errors due to either of these causes can be corrected by connecting a frequency divider to the PG/FG output of the IC. A ÷3 circuit will eliminate FG pulse jitter due to motor phase tolerance; a divider with a different ratio will eliminate FG pulse jitter due to back-EMF harmonics.

Tacho pulse jitter can also be caused by the small offset between the EMF comparators in the IC. This problem can be solved by using only one edge of the tacho pulses to derive speed information, i.e. the edge caused by a positive-going back-EMF zero crossing or the edge caused by a negative-going zero crossing.

Accurate phase (position) information, as required in VCR scanner motor drives, can also be derived from the tacho pulses by using information from an inexpensive wide-tolerance pick-up coil or AC-coupled Hall-effect sensor connected to the PG IN pin to merely identify particular PG tacho pulses as position (PG) pulses. T h e speed and position pulses are made available externally as a time-division multiplexed pulse train at the PG/FG open-collector output pin. The FG tacho pulses which have

been identified as position (PG) pulses are easily recognized because, unlike normal tacho FG pulses (duty factor of 50%), the duration of their LOW periods is reduced to about 15 μs.

Motor speed control

In brushless DC motor systems which don't use one of our ICs, it is common practice to control the speed of the motor by using pulse-width modulation (PWM) to control a DC to DC converter which provides a supply directly to the motor windings. The motor windings then act as the flywheel inductor for the converter. This system cannot be used with our control ICs because the switching spikes generated would prevent accurate detection of the zero crossings of the back-EMF for commutation purposes.

All our control ICs therefore include an uncommitted operational transconductance amplifier (OTA) that can be used to control the speed of the motor by determining the level of the DC supply to the output driver stages of the IC at the VMOT pin.

In all the speed control systems, a microprocessor senses the tacho (FG) pulses and provides the input to the control amplifier, either as PWM for digital control, or as a DC level via a DAC for analog control.

Digital control

Figure 6 is a circuit using the OTA for digital motor speed control. Here, PWM is supplied to the input of the OTA which supplies the base current to control the duty factor of the power switching transistor of an external DC to DC converter. The smooth DC output from the converter supplies the output driver stages of the IC at the VMOT pin.
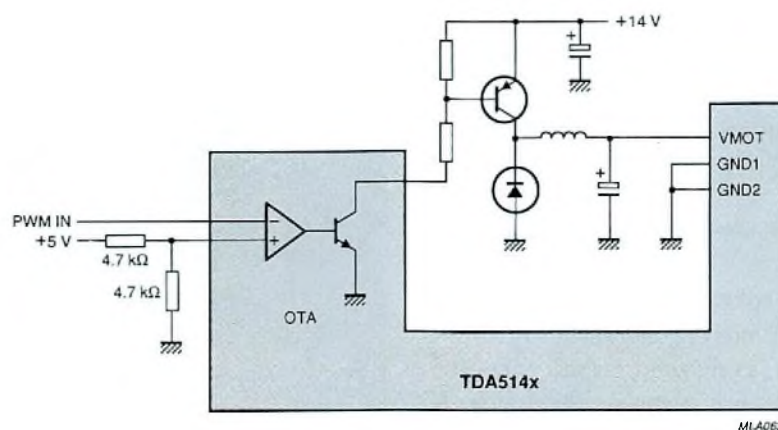

Fig.6 Digital PWM motor speed control circuit
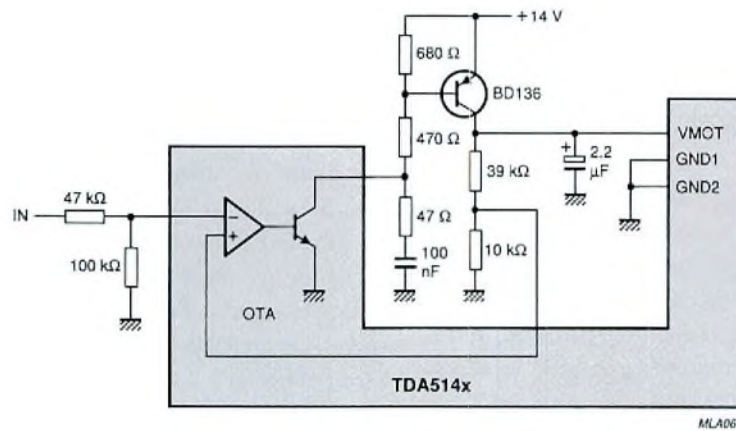
Fig.7 Voltage amplifier circuit for analog motor speed control

Analog control with a voltage amplifier

Figure 7 is a motor speed control circuit using the OTA and an external transistor as a voltage amplifier for providing a controllable supply voltage for the output driver stages of the IC at the VMOT pin. This circuit includes a frequency compensation network (R3C2) with a time-constant of 4.7 µs (34 kHz) which reduces the open-loop gain before the phase shift of the OTA poles becomes excessive.

Analog control with a current amplifier

A motor speed control circuit using the OTA and an external transistor as a current amplifier for providing a controllable supply voltage for the output driver stages at the VMOT pin of the IC s shown in the evaluation board circuit diagrams (Fig.10 and Fig.13). An important property of this amplifier is that its output impedance increases at higher frequencies, thereby reducing torque ripple at commutation frequencies.

TDA5140A and TDA5141 application evaluation boards

An application evaluation board using the TDA5140A to drive a VCR scanner head motor is shown in Fig.8.

The same application evaluation board using the TDA5141 to drive a 3½ inch computer hard disk is shown in Fig.9.

Figure 10 is the circuit diagram for these application evaluation boards.

Fig.8 An application evaluation board using the TDA5140A to drive a VCR scanner head motor

Fig.9 An application evaluation board using the TDA5141 to drive a computer hard disk motor

Fig.10 Circuit diagram of the evaluation boards shown in Fig.8 and Fig.9

THE TDA5142T MOTOR DRIVE IC
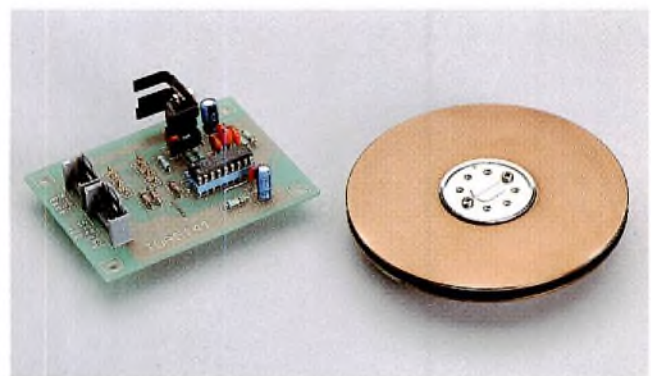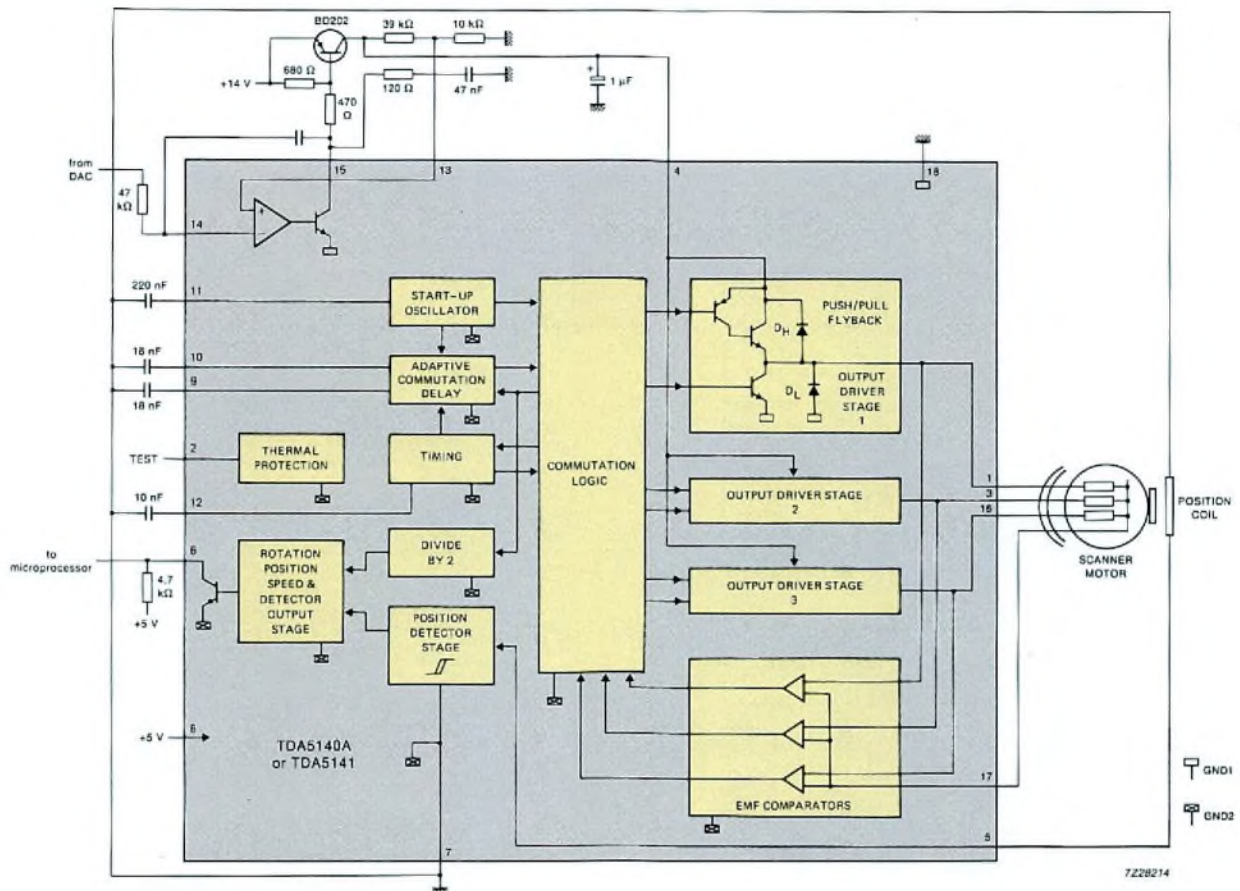
This IC, shown in block form in Fig.11 is in a 24-pin plastic SO package for surface mounting. It can provide up to 150 mA for full-wave drive of 3-phase high power brushless DC motors via three pairs of external push-pull bipolar transistors or power MOSFETs.

The TDA5142T doesn't have a facility for motor position sensing (PG pulse generation) because the type of application for which this IC is intended doesn't require it. Also, instead of the tacho (FG) pulses being generated solely from the zero crossings of the back-EMF as previously described, the HIGH to LOW transitions of the FG pulses are caused by each zero crossing of the back-EMF, and the LOW to HIGH transitions are caused by each commutation pulse. The frequency of the tacho pulses is therefore equal to the commutation frequency. For maximum accuracy, speed information should be derived from the negative-going edges of the FG pulses.

The TDA5142T also incorporates a braking function.

In all other respects, the operation of the TDA5142T is the same as that previously described for the TDA5140A/AT and the TDA5141.

Braking function

As shown in Fig.11, the TDA5142T has a built-in braking function. When the BRAKE input at pin 8 is left floating or connected to a voltage level of at least 2.7 V, the motor runs normally. Connecting the BRAKE input at pin 8 to ground, or to a level of less than 2.3 V, brakes the motor by setting outputs PA, PB and PC to their LOW state (lower transistors off), and setting outputs NA, NB and NC to their high impedance state (upper transistors on).

TDA5142T application evaluation board

Figure 12 is a circuit diagram of an application evaluation board using the TDA5142T to drive a very large computer hard disk via three pairs of external power transistors. A photograph of this evaluation board is shown in Fig.13.
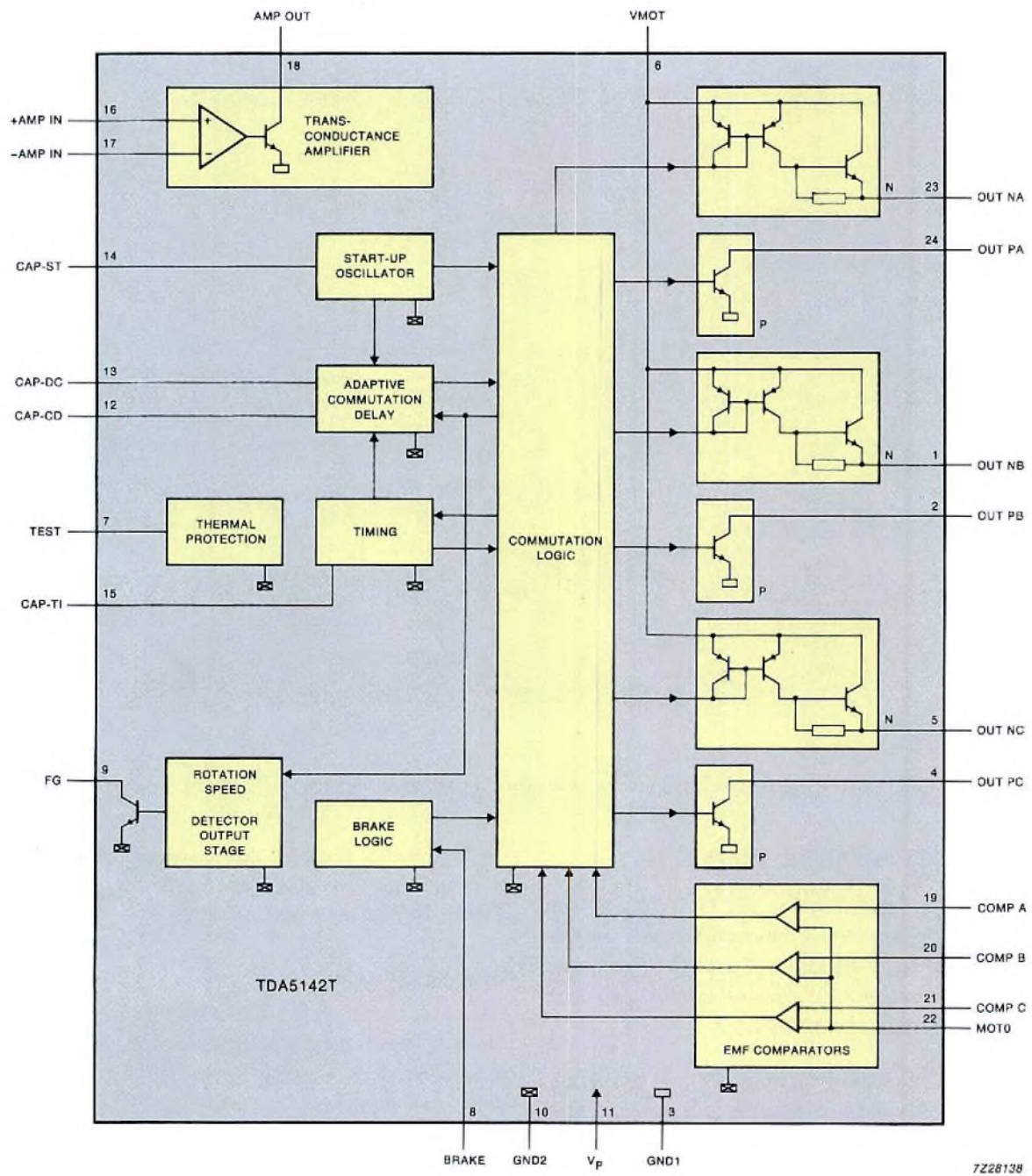
Fig.11 Block diagram of the TDA5142T

Fig.12 Circuit diagram of evaluation board shown in Fig.13
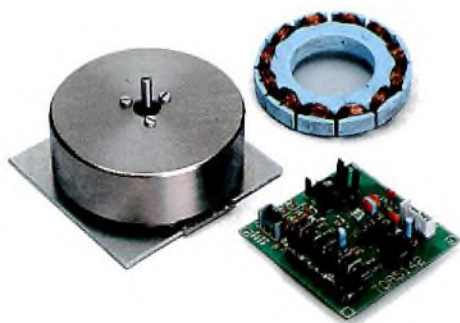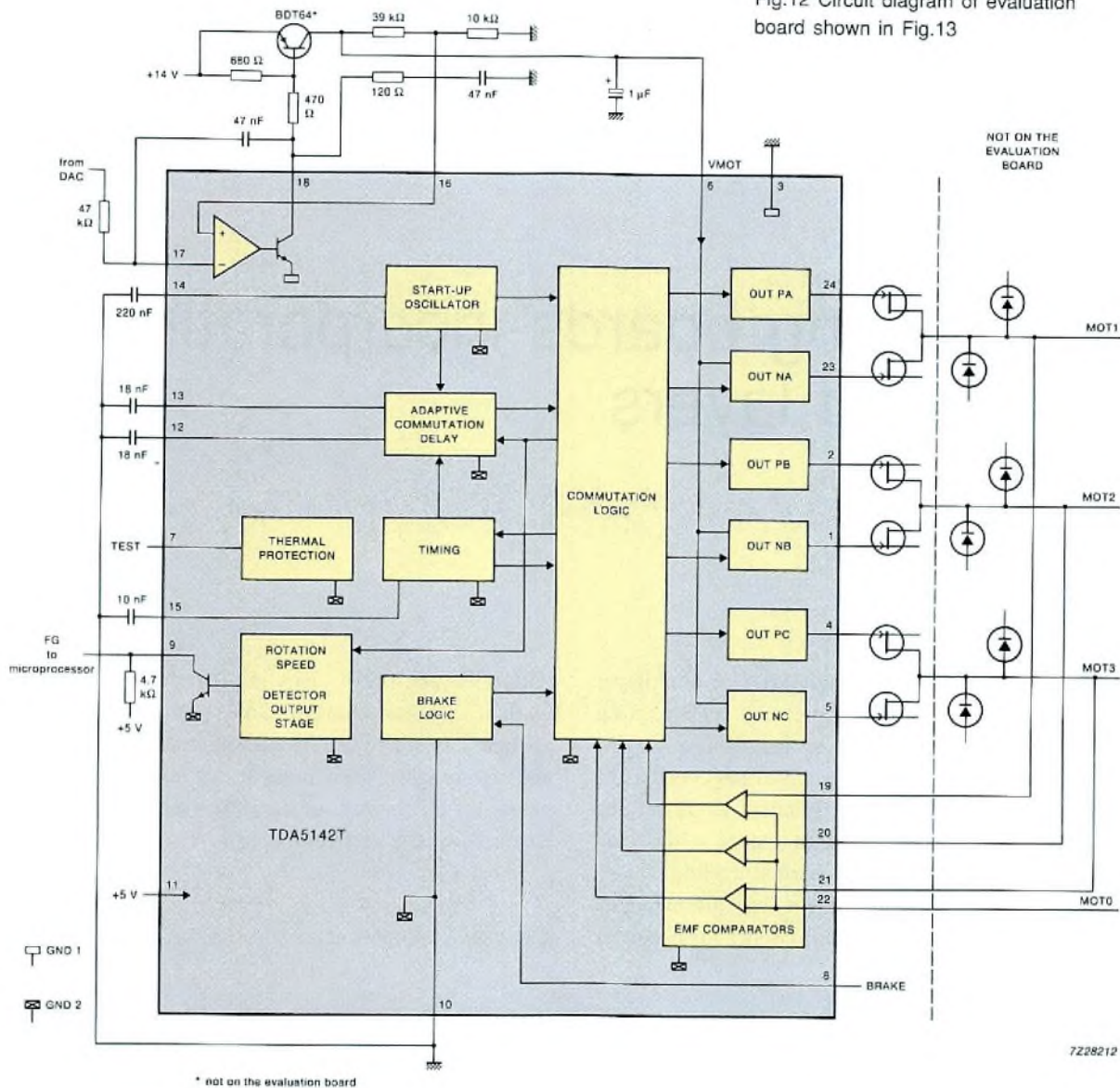
Fig.13 An application evaluation board using the TDA5142T to drive a large computer hard disk motor via three external power transistors

FURTHER INFORMATION ABOUT BRUSHLESS DC MOTOR DRIVE ICs

Further information about our drive ICs for brushless DC motors is given in the associated data sheets and in an application note "TDA514x brushless DC motor drive circuit family". These documents can be obtained from your local Philips sales organization listed on the back cover.

Printed wiring boards incorporating Cu-invar-Cu layers

ALFRED GOBERECHT

The biggest advantage of mounting SMDs on multilayer printing wiring boards (PWBs) is the very high packing density that can be achieved on the board. The biggest disadvantage, however, is the mismatch of the coefficients of thermal expansion (CTE) of the standard PWB and the component outlines. This mismatch can cause solder joint failure during PWB assembly and thermal cycling.

Philips has solved this problem by producing a multilayer board with metal planes of copper-invar-copper (CIC) between layers. This results in a low coefficient of thermal expansion, making the boards ideal for use in applications where leadless ceramic chip carriers are used and high reliability requirements are imperative. These CIC planes have distinct advantages over such materials as Kevlar®, quartz and compliant layers.

® Registered Trademark of E.I du Pont de Nemours.

An example of high-density packing of chip outlines on a multilayer board

20% copper/60% invar/20% copper properties

TCE, –55 °C to +155 °C	= 6.0 ppm/K
thermal conductivity	= 164 W/m/K (x,y axis)
average tensile stength (annealed)	= 16 W/m/K (z axis)
average yield strength (annealed)	= 60 000 psi
modulus of elasticity	= 19×10^6 psi
electrical resistivity	= 5.5 $\mu\Omega$/cm (DC)
density	= 8.4 g/cm^3

Fig.1 Thermal coefficient of expansion as a function of copper content in copper-clad invar

WHAT IS CIC?

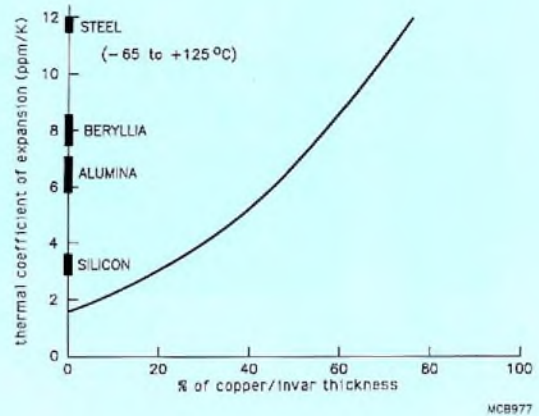CIC (or copper-clad invar) consists of outer layers of high thermal conductivity copper, metallurgically bonded to a core of invar, a nickel-iron alloy (36% Ni – 64% Fe) with an extremely low coefficient of thermal expansion (less than 7% that of pure iron). The bonding is done by a cold roll-cladding process, requiring no adhesives or brazing alloys.

By varying the relative thickness of the copper to invar, we can get a range of CTEs compatible with almost any component outline (see Fig.1 and Ref.1). Also, the excellent thermal properties of CIC make it an ideal heatsink and heat spreader. What's more, it adds rigidity to the multilayer board, and can be used as a power and ground plane.

TYPICAL MULTILAYER BOARD CONSTRUCTION

We have been developing multilayer boards incorporating CIC planes since the early 80s, and in 1987 we set up a pilot production scheme. With the cooperation of our customers, we have designed and tested a large range of boards, choosing polyimide glass as the base material.

Figure 2 illustrates the basic construction of our most common type of board. Two CIC planes are positioned next to the outer (cap) layers. The thicknesses of these layers can range from 0.15 mm to 0.5 mm, and the copper/invar/copper ratio can vary from 20/60/20 to 5/90/5. Voltage, ground and signal layers are positioned between the two CIC planes. Because the packing density of the board can be very high, the inner layers may need buried via interconnections. Thermal via holes connect the large thermal paths beneath the high-wattage components to the two CIC planes, which in turn dissipate the heat to a cold wall or to a cold wall edge.

The growth in SMD technology has had a big influence on PWB design. SMD boards must be flat to allow the screening of the solder paste on the lands; the maximum allowable bow of the board therefore should be no more than 0.5%. To meet this stringent requirement, a multilayer board incorporating CIC planes must have a balanced board construction along the Z axis.

Current board types

When constructing a multilayer board, one must consider the number of SMDs to be mounted, the amount of power to be dissipated, and the cooling system available. These factors determine the number and thickness of CIC planes to be used, as well as their position within the board.

Our board constructions can be divided into three types. The first type, which we have already described with reference to Fig.2, consists of two CIC planes positioned next to the outer layers. Several thousand boards of this type are manufactured in our factory every year.

The second type consists of three CIC planes – one plane centrally located and the other two positioned near the outer layers. This board is constructed in two halves. One half of the board has a single CIC plane and some signal layers and is processed as a blind via layer (Ref.2). The advantage of this type of construction is the ease with which the electrical interconnections and thermal vias between the outer layers and the adjacent CIC plane can be made. The other half of the board comprises two CIC planes, situated so that the board is symmetrical about the x,y plane. This half is processed in the same way as the first half. Both halves are then laminated together, interconnected and finished in the standard way. Special care is taken to ensure that the half products are a perfect match during manufacture, right up to the final stage, and that each half-board is flat during mechanical and chemical operations.

signal layer with blind via (cap layer)

CIC layer

signal layer with buried via

power, ground plane

signal layer with buried via

CIC layer

signal layer with blind via (cap layer)

thermal via hole   via hole   edge thermal via hole

MCB97B
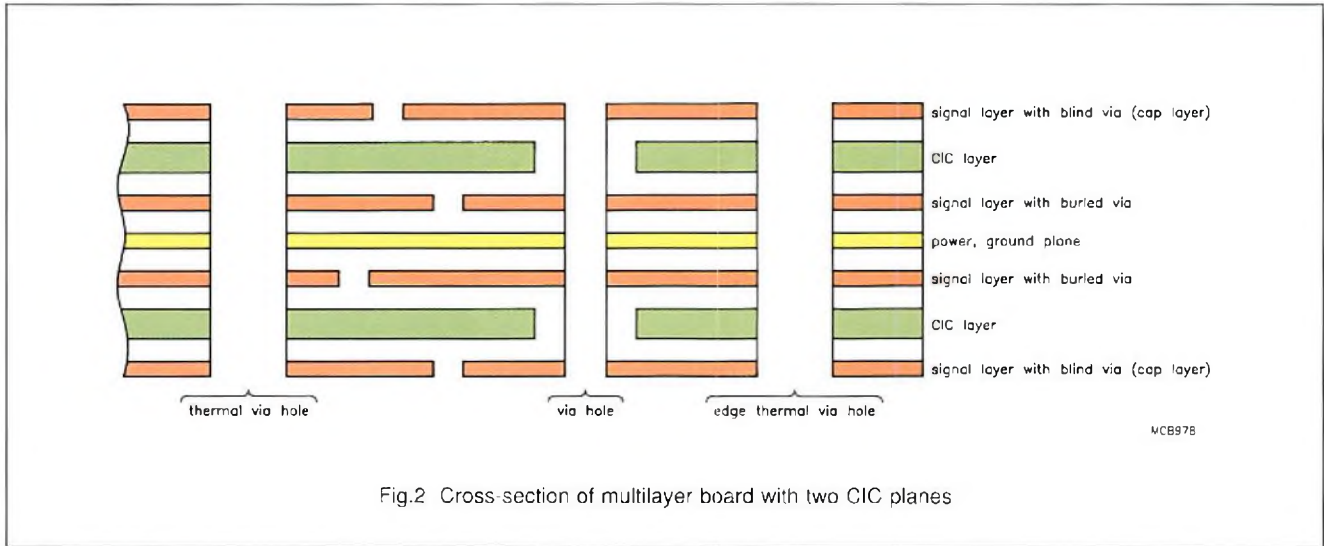
Fig.2 Cross-section of multilayer board with two CIC planes

A row of 5 via holes on a pitch of 1.27 mm, drilled 0.4 mm in a multilayer board 2.8 mm thick. Two CIC planes of 0.25 mm, and 10 coppers layers can also be seen
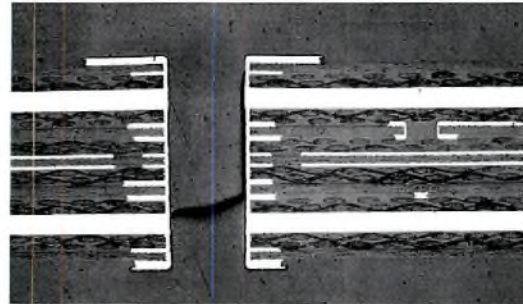
The same board showing a buried via hole and one thermal riser drilled 1.1 mm
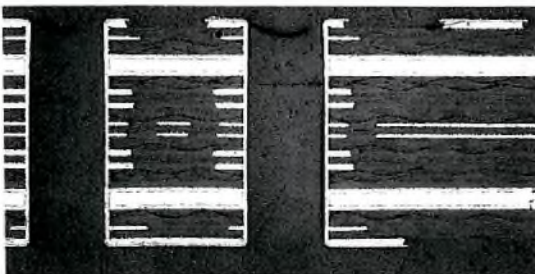
The same board, this time showing two thermal risers drilled 1.1 mm, on a pitch of 2.54 mm
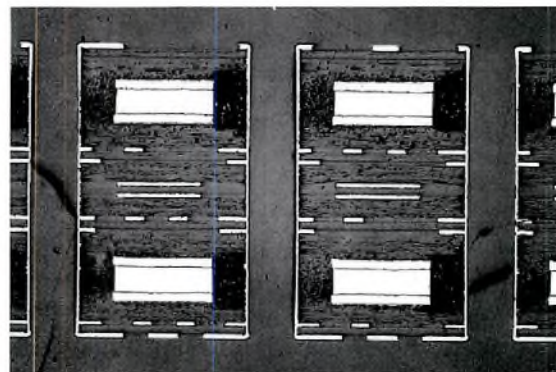
Multilayer board 3.5 mm thick, with via holes of 0.6 mm, on a pitch of 2.54 mm. Two CIC planes, each 0.5 mm thick, are also shown, with the copper and invar quite distinct

Figure 3 illustrates the make-up of the two halves, and shows a cross-section of the end result. The three CIC planes must be physically identical to each other. The layer 'a' represents a double-sided laminate and two or three plies of prepreg, 'b' is the thickness of the stack of several inner layers separated by prepreg, while 'c' is usually 2 or 3 plies of prepreg, but it could also be a logic layer with or without buried holes sandwiched between prepreg layers. This type of board is used when the thermal requirements of the design are high and when there is an overall constraint on board thickness.

The third board type incorporates four CIC planes; each plane being 150 μm thick to limit weight. The central planes are used as voltage and ground planes, but all four planes are used to maintain a low CTE.

Fig.3 Construction and cross-section of a multilayer board with three CIC planes

THE IMPACT OF CIC PLANES IN MULTILAYER BOARDS

The use of CIC planes in multilayer boards has had a significant impact on board design. Board thicknesses of 2.4 mm to 3.4 mm are now being used. Also, SMD technology has resulted in high-density boards utilizing fine line spaces and small through-holes. The use of small-diameter holes has increased board aspect ratio – aspect ratios of 6 or 7 are no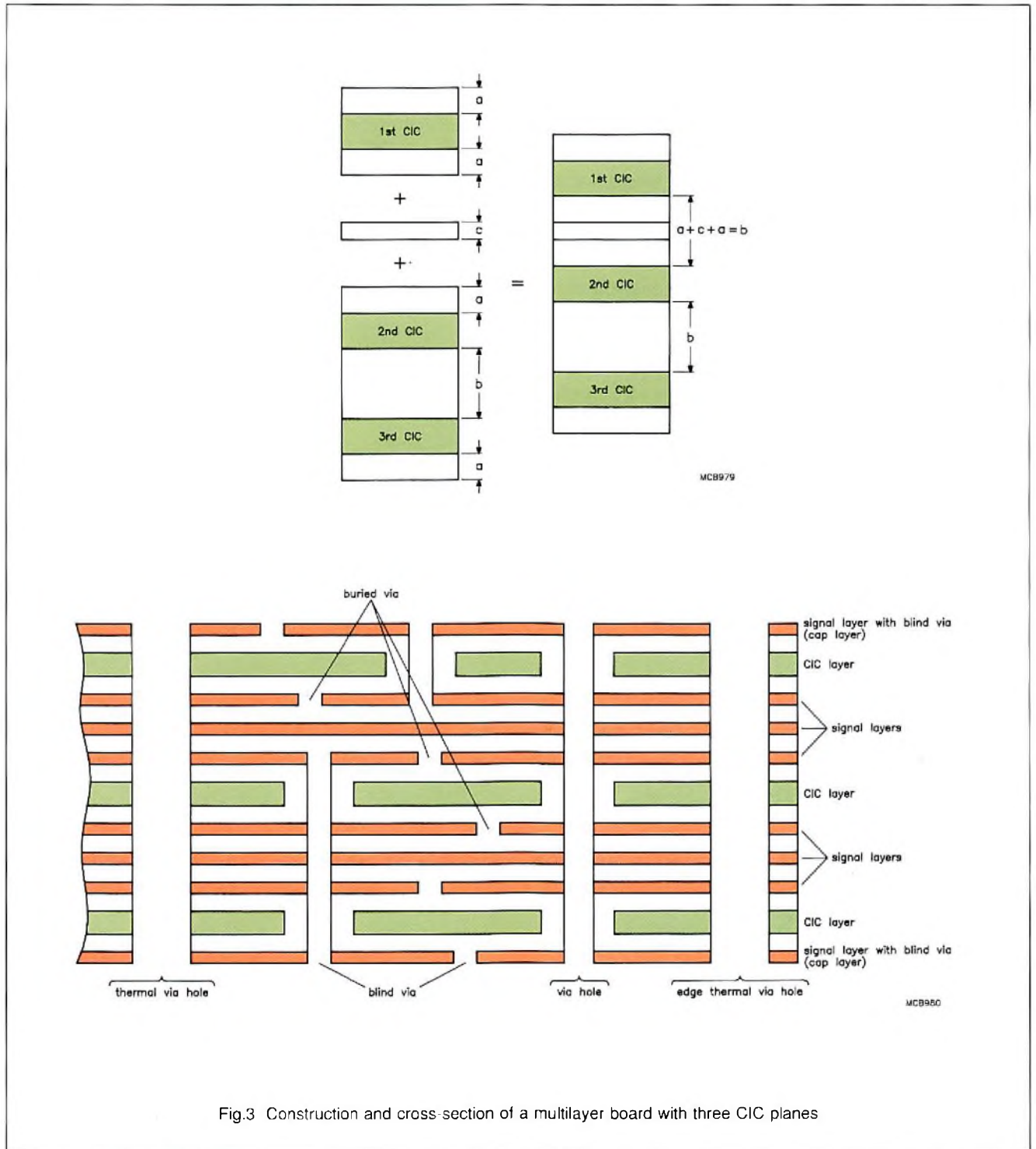 exception. This high aspect ratio makes plating of the holes more difficult, and so the plating process used for through-holes in thick multilayer boards must be adjusted accordingly.

New laminates

Because SMDs require only small via holes, we are producing electrical interconnections with vias only 0.4 mm in diameter. These via holes have the usual plating of copper 25 µm thick, but the resulting copper barrel inside the via must be able to withstand thermal expansion during soldering, service operations and environmental stress. It is important that both the customer and the board supplier are involved in selecting the base material specific to requirements. The most common materials are polyimide glass and epoxy glass with high glass transition temperature. The inherent safety features of these laminates ensure a reliable product. We are one of the few printed wiring board manufacturers who can process this large range of base material products. For years we have had the technology to manufacture polyimide multilayer boards,

even for military applications. We are constantly improving our equipment and machinery park in order to fulfil high-tech product specifications. Right now we are investigating new types of high-temperature epoxy/BT laminates in our development department.

Conclusion

We have considerable knowledge and experience in the manufacture of printed wiring boards incorporating CIC. The capabilities of our technical staff are second-to-none, and they are always there to help you, the customer, make your decisions; decisions such as the choice of CIC ratios, the board thicknesses, the number of plies of CIC and the type of substrate material. By involving us at the start of your project, you have access to our technology and expertise, and by combining our efforts, we can achieve the best possible solution, every time.

REFERENCES
1. Copper-clad invar for reliable packaging and interconnection of headless ceramic chip carriers by F.J Dance, Texas Instruments.
2. Blind and buried vias for multilayer PWBs by A. Goberecht – Electronic Components and Applications Vol.8 No.4.

I²C-bus control programs for consumer applications

TJEU HORSCH

During the more than twenty years that we've been supplying integrated circuits for radio/audio and TV, we've built an unrivalled reputation for keeping our customers at the forefront of circuit design and innovation. This reputation wasn't earned solely by providing ICs to meet the industry's needs, but also by offering extensive applications support.

In recent years however, we've taken advantage of the rapid advances in IC manufacturing technology to incorporate digital control and signal processing circuitry into our radio/audio and TV concepts, thereby improving their performance and adding a host of new facilities and features. The first digital IC addition to a TV set was a microcomputer to facilitate more accurate and stable tuning and digital/remote control of analog signal levels such as saturation, contrast, brightness, sound volume and tone.

Having introduced digital control into consumer equipment ICs, it soon became evident that there was a need for a simple, inexpensive and standardized method of interconnecting them. That's why we developed our two-wire Inter IC (I²C) bus which is now used extensively to facilitate the design of computer-controlled TV and radio/audio equipment.

Although the combination of analog and digital signal processing and control undoubtedly brings many benefits to both manufacturers and end-users, it also causes many new headaches for design and service engineers who must quickly familiarize themselves with digital techniques and software. To help solve this problem, our TV and radio/audio IC applications support embraces both hardware and software.

An important part of our customer support package is a set of I²C-bus control programs (on 5¼ inch or 3½ inch diskettes) that allow engineers to evaluate, analyze and test the functions of I²C-bus compatible ICs for radio/audio and TV, even if they don't understand the internal software structure of the circuits. All that's needed to run the control programs is an IBM compatible PC with MS-DOS/PC-DOS and at least 512 kbytes of RAM. An I²C-bus interface board must be connected between the I²C-bus of the board under test and the CENTRONICS parallel printer port of the PC.

The simple interface boards (for either single-master or multi-master systems) can be assembled by the user or can be ordered from Philips. The single-master interface is timed by the PC and operates at about 10 kHz. The multimaster interface can be set via software to operate at one of fifteen speeds between 1 kHz and 99 kHz.

The present set of I²C-bus control programs comprises:

- IICTV program for controlling digital and analog TV signal processing ICs which have an I²C-bus interface

- IICRADIO program for controlling radio/audio ICs which have an I²C-bus interface.

Both programs incorporate a database containing IC control data, and a set of easy to use dedicated or universal menus for controlling the ICs. All the menus are self-explanatory and the desired functions can be accessed with a single keystroke. The dedicated menus show all the control functions of the associated IC divided into logical groups. All data communication on the I²C-bus is subjected to error checking and, if errors occur, they're displayed on the screen of the PC as simple, easily understood messages.

IICTV AND IICRADIO PROGRAMS

These two programs each incorporate:

• dedicated menus for some I²C-bus compatible TV or radio/audio ICs

• a database containing the control data for the ICs

• a database transceiver menu from which all ICs in the database can be accessed. For each IC, this menu displays the registers together with their subaddress, symbolic name and register contents. The register contents for each IC can be easily changed by simply entering a hexadecimal number. This menu is useful for accessing ICs which are in the database but don't yet have a dedicated menu

• a universal I²C-bus transmitter/receiver menu for constructing up to seven user-defined I²C-bus messages. This menu can be used, for example, to control ICs which aren't included in the database structure e.g. microcontrollers

• a change mode settings menu to enable/disable automatic background functions such as error checking, audible warning to indicate control range limits, transmission rate and parallel port selection

• a tracer menu for limited display of all the data on the I²C-bus, or only the data transmitted to one slave address. This menu can only be used if a multimaster interface is installed

• a menu for reading/writing 128/256-byte I²C-bus compatible RAMs and (E)EPROMS type PCF85XX

• help functions at any level

• system initialization for initialization of all the ICs in a certain hardware configuration with the values currently present in the database

• an initialize database menu for changing the structure of the database to match the ICs in a certain hardware configuration; this menu allows one or more of all the ICs in the program to be activated, de-activated, set monitorable, set not monitorable, included or excluded.

The I²C-bus compatible ICs that can be controlled from the dedicated menus and/or the database transceiver menus in the IICTV and IICRADIO programs are listed in Table 1 and Table 2.

Some menu examples

The rear menu shown in the photograph is for the RGB processor TDA4680. The functions of the IC are divided into toggle bits and control parameters. To change one of the toggle functions, the cursor is positioned on the corresponding field and the space-bar pressed. The control parameters can be changed by entering a (decimal) number or using the <>, = or down/up keys. Status information is automatically read out and displayed in the bottom right-hand corner of the menu.
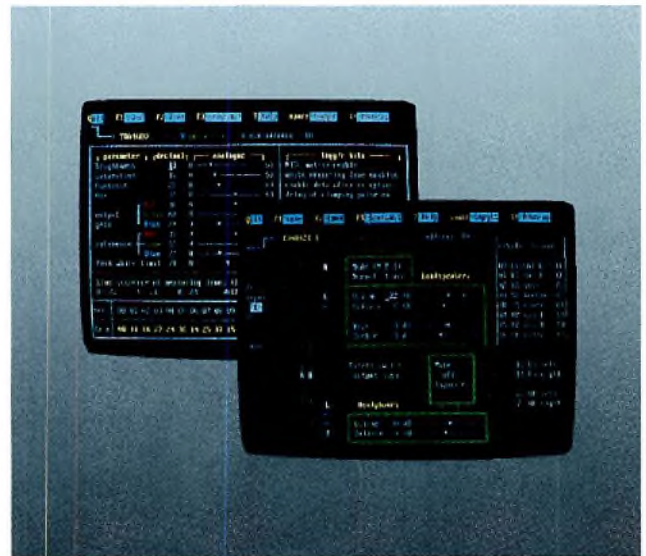
The front menu shown in the photograph is for the hi-fi Stereo Audio Processor TDA8421. Instead of being normal text, the display is now in the form of a block diagram of the IC. Hexadecimal codes indicate the settings of the various analog controls and the state of the internal switches. The settings of the normal analog controls are also given in dBs. The cursor can be moved to various positions to select the desired functions. If a hexadecimal number is altered, the corresponding dB value(s) is automatically modified accordingly. Pressing the "?" key obtains a help menu.

One of the dedicated menus in the IICTV program is for controlling the TSA551X family of digital PLL frequency synthesizers in TV sets. For this menu, the screen is divided into logical blocks such as tuner band definitions, selected transmission standard and preset programme specifications. If the data in any block is changed, the corresponding data in any of the other blocks is automatically adapted accordingly. The values sent to the

TSA551X registers are displayed and the status byte of the IC is automatically read out.

Features of this menu are:

- user-defined tuner presets (band limits, band switches and the tuner crystal oscillator frequency)

- six channel number/frequency conversion tables for various parts of the world

- user-specified channel number/frequency conversion table

- ten user-defined programme presets

- automatic read-out of the status byte of the TSA551X family IC

- tuner frequency band can be swept through

- storage of fourteen different (tuner) presets on disk under user-defined names.

TABLE 1
ICs that can be controlled by the IICTV program

Type number	Function	Menu	
		dedicated	database transceiver
PCF85XX	CMOS RAMs and (E)EPROMs	✓	
PCF8574(A)	8-bit I/O expander		✓
SAA1064	LED driver (2-digit static and 4-digit dynamic)		✓
SAA1300	quintuple high output current switching circuit		✓
SAA7280	terrestrial digital sound decoder	✓	✓
SAA9051	digital multistandard colour decoder	✓	✓
SAA9056	digital SECAM colour decoder		✓
TDA4670	picture signal improvement (PSI) circuit	✓	✓
TDA4680/5	RGB processor	✓	✓
TDA8415	TV and video recorder stereo/dual sound processor	✓	✓
TDA8421	hi-fi stereo audio processor	✓	✓
TDA8425	hi-fi stereo audio processor	✓	✓
TDA8433	deflection processor	✓	✓
TDA8440	video/audio switch for colour TV sets	✓	✓
TDA8442	I²C-bus interface for colour decoders	✓	✓
TDA8443A	YUV/RGB interface circuit		✓
TDA8444	octuple 6-bit DAC	✓	✓
TDA8466	PAL/NTSC colour decoder	✓	✓
TDA9140	PAL/NTSC/SECAM colour decoder/sync processor	✓	✓
TDA9150	deflection processor	✓	✓
TDA9160	PAL/NTSC/SECAM colour decoder/sync processor	✓	✓
Teletext	teletext control board	✓	✓
TSA551X family	PLL frequency synthesizers	✓	✓

NOTES:
1. Some of the menus are not yet finalized because some ICs are still being developed.
2. The diskettes are regularly updated by adding new menus.

There is also a similar dedicated menu in the IICTV program for controlling digital PLL frequency synthesizers of the TSA551X family in satellite TV receiver applications. Features of this menu are:

- user-defined tuner presets (band limits and band switches)
- a channel number/frequency conversion table (40 channels) for region 1 as defined by "WARC 1977"

- up to seven user-defined channel number/frequency conversion tables
- ten user-specified programme presets
- automatic read-out of the status byte of the TSA551X family IC
- tuner frequency band can be swept through
- storage of fourteen different (tuner) presets on disk under user-defined names.

TABLE 2
ICs that can be controlled by the IICRADIO program

Type number	Function	Menu	
		dedicated	database transceiver
CCR910S	RDS decoder microcontroller	✓	
PCF85XX	CMOS RAMs and (E)EPROMs	✓	
PCF8566	universal 96-segment LCD driver	✓	
PCF8574(A)	8-bit I/O expander		✓
PCF8576	universal 160-segment LCD driver	✓	
PCF8577(A)	universal 64-segment LCD driver	✓	
SAA1064	2-digit static and 4-digit dynamic LED driver	✓	✓
SAA1300	5-bit high current output circuit		✓
TDA1551	BTL power amplifier	✓	✓
TDA8421	hi-fi stereo audio processor		✓
TDA8425	hi-fi stereo audio processor		✓
TDA8442	quadruple 6-bit DAC with two switched outputs	✓	✓
TDA8444	octuple 6-bit DAC	✓	✓
TEA6100	FM IF system/tuning interface	✓	✓
TEA6300	sound fader control circuit with three inputs	✓	✓
TEA6310	sound fader control circuit with one input	✓	✓
TEA6330	sound fader control circuit with one input	✓	✓
TSA6057	PLL frequency synthesizer for radio	✓	✓

NOTES:
1. Some of the menus are not yet finalized because some ICs are still being developed.
2. The diskettes are regularly updated by adding new menus.

REFERENCE

"The I²C-bus specification", ordering code 9398 358 10011

Black matrix colour picture tubes

The colour-picture tube is a strange contrast to the normal world of electronic components. On the one hand it must meet exacting technical specifications and performance criteria, dictated these days by the stringent resolution requirements of current satellite systems (precursor to HDTV). And on the other hand it must satisfy demanding aesthetic standards dictated by the requirements of the day, and by the ever changing preferences of a viewing public.

For some time the viewing trend has been towards bright, high-contrast pictures to allow daytime TV viewing, coupled with dark, inconspicuous screens when the set is switched off. Recently this trend has become stronger leading to a demand for picture tubes with even darker screens.

Philips' latest 45AX colour-picture-tube range, embodying a new *black matrix* system, has been developed to satisfy the above market needs. In particular, the trends toward larger (jumbo) screens and toward higher screen resolution (in anticipation of future HDTV) can realistically be met only with a black matrix system. So our well-known HiBri system, till now the best tube technology available, will gradually be replaced completely by black matrix.

Top of the range is still the Black Line series with low-expansion invar shadow masks allowing them to be driven at higher beam power than iron-mask tubes. This means they can employ lower-transmission faceplate glass to give even darker screens than standard black matrix tubes, and improved picture contrast without any sacrifice of picture brightness.

Standard 45AX tubes too, will be moving over from HiBri to black matrix, starting with the most popular sizes (66 and 59 cm), so soon all 45AX tubes will be supplied in black matrix.

EVOLUTIONARY APPROACH

To take full advantage of the latest technological advances as they occur, we adopted an evolutionary approach to the development of the 45AX range. Initially, the range was based on our proven HiBri technology. The Black Line series, as well as employing invar shadow masks had 40% transmission faceplates (instead of the standard 52%) and gave a visual performance superior to the then current black matrix tubes, with hardly any of their drawbacks (mainly screen patchiness and poor white uniformity). But to be ready for HDTV when it comes, with its greater demands on resolution and hence mask pitch, we now consider the time is right to move over to a new black matrix system. Already used successfully in our professional colour-monitor tubes, this system employs a novel deposition process that overcomes the problems associated with earlier black matrix systems.

Our professional colour monitor tubes (shown here in production) are now widely specified by monitor and computer manufacturers. In this application, where the demands on resolution, colour purity and contrast have long been severe, we have been using the PVP black matrix system for several years

NEW DEPOSITION PROCESS FOR SUPERIOR BLACK-MATRIX PERFORMANCE

Philips' new black-matrix deposition process, currently in use for its colour monitor tubes and now to be introduced into its 45AX range, makes use of a cross-linkable polymer PVP (poly vinyl perolidium) to define the matrix lines during the photolithographic stage.

As with the phosphor-stripe pattern, the black matrix pattern is made using a photolithographic process with the shadow mask as template. A protective layer of PVP is deposited onto the faceplate and exposed to UV light through the mask, with the source located at one of the gun positions. This is repeated twice more for the other two gun positions. The PVP is then developed and the unexposed portion removed to leave a pattern of lines on the inside of the faceplate.

A layer of graphite is then deposited over the pattern and adheres to the faceplate glass between the lines, which are then removed to leave the finished black matrix pattern on the faceplate.

Finally, the three phosphors are deposited between the black matrix lines in the standard way.

The major difference between this and the conventional black matrix process is in the properties of the PVP layer.

The conventional process uses a protective layer (PVA) whose curing properties are relatively independent of UV intensity. The layer may then cure right up to the periphery of the UV spot (i.e. to the edge of the diffraction pattern produced by the mask slots), and incomplete curing at the periphery leaves rough edges in the protective layer on development.

The cross-linked PVP molecules, in contrast, cure only above a certain threshold of UV intensity, so the problematic region near the periphery of the UV spot remains completely uncured and is removed on development, leaving a clean straight edge.
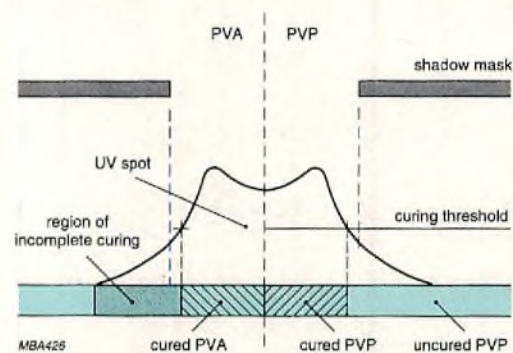
The conventional process uses a protective layer (PVA) whose curing properties are independent of UV intensity. The layer may then partially cure right up to the edge of the UV spot, and leave a rough edge on development. The cross-linked PVP molecules, in contrast, cure only above a certain threshold of UV intensity, so the region near the periphery of the UV spot remains completely uncured, and leaves a clean straight edge on development

The new PVP process, with its much finer edge definition and more regular phosphor stripe width gives the advantages of:

- **greatly improved white uniformity**
- **better colour saturation**
- **reduced screen patchiness** for a more pleasing appearance when the set is switched off
- **higher screen brightness** – since the finer definition of the new process allows for greater mask transparency and also for greater use to be made of the electron spots as the phosphor stripes can be wider and more closely spaced
- and most important for future HDTV, **greater resolution** – since the finer edge definition allows ultimately for finer pitch phosphor stripes.
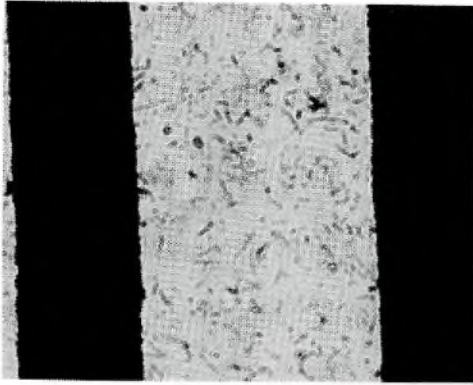
The new PVP deposition process *(top)* produces much sharper graphite lines than the PVA process *(bottom)*, and hence allows for much closer tolerances on the phosphor stripes

The advent of HDTV in the coming years will place stringent demands on picture tube performance. Demands on picture brightness and contrast, colour purity, resolution and stability. Demands that Philips' new 45AX black matrix range is ideally equipped to meet

DRYPACK protects ICs in large plastic packages against moisture

LEO VAN GEMERT

If infrared or vapour-phase soldering is used to surface-mount an IC in a large plastic package (QFP or PLCC), vapourization of the small amount of moisture absorbed by the package during storage can increase the internal pressure to such an extent that the plastic cracks. This phenomena is known as Moisture Induced Plastic Package Cracking (MIPPC).

To provide an immediate solution to the problem of ensuring trouble-free soldering of ICs in MIPPC-sensitive packages, we can now deliver them packed in a resealable moisture-resistant plastic packet called a DRYPACK.

INFLUENCING FACTORS FOR MIPPC

The sensitivity of a plastic IC package to MIPPC is a function of:

- the chip area (size of the die pad)
- the thickness of the plastic used for the package
- the temperature and duration of the soldering process
- the moisture content of the package.

Mechanical characteristics of the package

Since larger surface-mount IC packages such as PLCCs and QFPs usually have larger die pads and thinner packages than the smaller SO packages, they are more susceptible to MIPPC.

Soldering method

Because wave soldering causes only brief exposure of the package to heat, it doesn't cause MIPCC. Similarly, localized heating such as that applied during resistance or laser soldering is not a cause of MIPPC because it doesn't significantly increase the internal temperature of the package. However, if infrared or vapour-phase soldering is used, care must be taken to avoid MIPPC by pre-drying the ICs or obtaining them from a DRYPACK.

Moisture content of the package

Comprehensive investigations have revealed that the risk of MIPPC is completely eliminated if the moisture content of a large plastic IC package doesn't exceed 0.1% by weight.

PREVENTION OF MIPPC

Using a different type of plastic

MIPPC would of course be eliminated if the IC packages were manufactured from a less absorbent type of plastic. Investigations into a new moulding compound for this purpose are in progress but it will be some time before such a material is available.

Drying ICs before they are soldered

MIPPC can also be prevented by drying ICs to reduce the moisture content of their packages below 0.1% by weight prior to soldering, but this is time consuming and involves extra handling of the IC resulting in an increased risk of mechanical or ESD damage.

Preventing moisture absorbtion during storage

The most obvious method of eliminating MIPCC is to prevent IC packages absorbing moisture by storing them in a moisture-resistant enclosure. This is the function of the Philips DRYPACK.

PHILIPS DRYPACK

Philips DRYPACK is a laminated plastic packet that maintains the moisture content of the packages of the ICs it contains below 0.1% by weight for up to a year. It must be stored at a temperature below 30 °C in an atmosphere of less than 60% relative humidity (RH). The DRYPACK contains a desiccant and a humidity indicator which allows the moisture content to be checked when the bag is opened.

Using ICs from a DRYPACK

Before using ICs from a DRYPACK, it is essential to check the humidity indicator. If it shows RH of less than 30% (the colour of the 30% dot has not changed from blue to pink), the ICs it contains are ready for use. However, to prevent them absorbing moisture after the DRYPACK is opened, the ICs must be soldered onto a PCB within the period specified in Table 1. The times indicated in Table 1 apply to ICs awaiting soldering at a temperature of not more than 25 °C in an RH of less than 60%.

TABLE 1
Maximum time before soldering ICs from a DRYPACK if the RH indicator shows less than 30%

package	max. time before soldering (h)
QFP44	24
QFP48	24
QFP64, 80, 100	48
QFP120, 128, 160	96
PLCC44, 68, 84	96

TABLE 2
Drying times if a DRYPACK indicates more than 30% RH

package	temperature (°C)	drying time (h)
QFP44	125	8
QFP48	125	6
QFP64, 80, 100	125	10
QFP120, 128, 160	125	12
PLCC44, 68, 84	125	12

If the humidity indicator in a DRYPACK shows RH of more than 30% (the colour of the 30% dot has changed from blue to pink), the DRYPACK has been damaged, opened, or stored under too severe climatic conditions. In this case, to eliminate any possibility of MIPPC, the ICs contained in the DRYPACK must be dried before soldering. Figure 1 shows the reduction of moisture content as a function of time for some large plastic IC packages. Table 2 gives the recommended drying times for reducing the moisture content of large plastic IC packages from an initial level of 0.3% by weight. Although drying to a

moisture content of 0.1% by weight is sufficient, the figures quoted in Table 2 include a built-in safety margin by giving the times required to achieve a moisture content of 0.05% by weight.
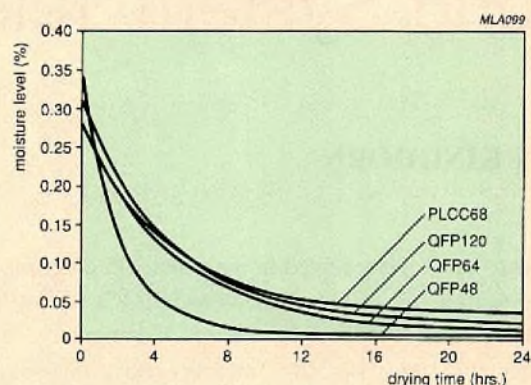

Fig.1 Moisture content as a function of drying time for ICs in a selection of large surface-mount packages

Resealing a DRYPACK

If some of the ICs from an opened DRYPACK are not used, the desiccant and humidity detector should be reinserted and the DRYPACK resealed within half an hour of opening by using commercially available heat-sealing equipment. The time for which a resealed DRYPACK can be stored depends on the time since it was originally packed, and the time it remained open before resealing.
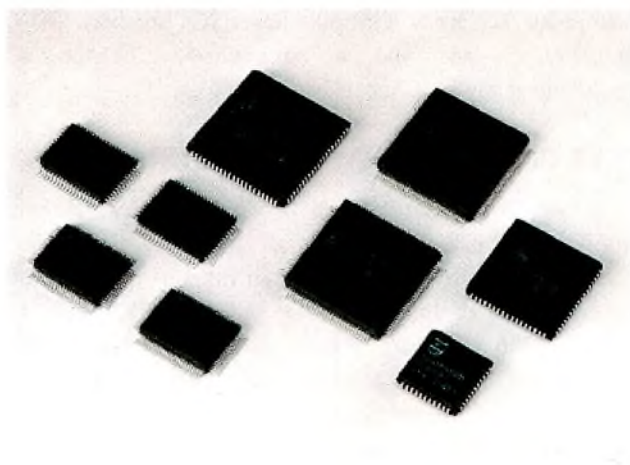
World System Teletext (WST) ICs

JOHN KINGHORN

Teletext can now be received in more than 35 countries by over 40 million TV sets, and the decoding ICs for most of them have been supplied by Philips Components. Ever since inauguration of the first teletext service in the early 1970s, Philips has been actively involved in developing the service and introducing it throughout the world. For example, Philips helped to draw up the World System Teletext standard which is now adopted by many countries. Recent developments such as FLOF/FASTEXT/TOP and enhanced language facilities have all been made possible by using the Philips-designed Computer-Controlled Teletext (CCT) approach to overcome the limitations of earlier teletext decoders.

Because Philips teletext ICs are computer-controlled via the I^2C-bus, they add flexibility to TV set design by allowing teletext decoders for different markets to be simply inserted into the same basic TV chassis or separate "plug-in" module.

To help TV set manufacturers meet the needs of specific market areas, Philips teletext ICs are backed by evaluation boards and a comprehensive range of production-ready software packages.

TELETEXT SYSTEM CONFIGURATIONS

As shown in Fig.1, there are two basic teletext system configurations using WST ICs.

The first configuration, shown in Fig.1(a), uses one of our new range of Integrated VIP and Text (IVT) ICs. If the SAA5246 (IVT1.0) is used, an external 8K × 8-bit SRAM must be added for storing four pages (extension packet mode) or eight pages (normal mode). With an SAA5244 (IVT1.1), a single-page RAM is built into the chip so that no external RAM is necessary. If the SAA5247 (IVT1.1BMC) with Background Memory Control (BMC) is used, there is an on-chip single-page RAM and facilities for storing up to 512 pages in external DRAM which is rapidly scanned on each page request, thereby giving near-instant page access.

The configuration shown in Fig.1(b) is intended for top-of-the-range analog, digital or features TV sets. It uses Digital Video Teletext (DVT) IC SAA9042 with either a Video Input Processor (VIP) SAA5191 or a dataline slicer SAA5235/6.

An overview of Enhanced Computer-Controlled Teletext (ECCT) ICs and teletext software (SAFARI) packages is given at the end of the article.
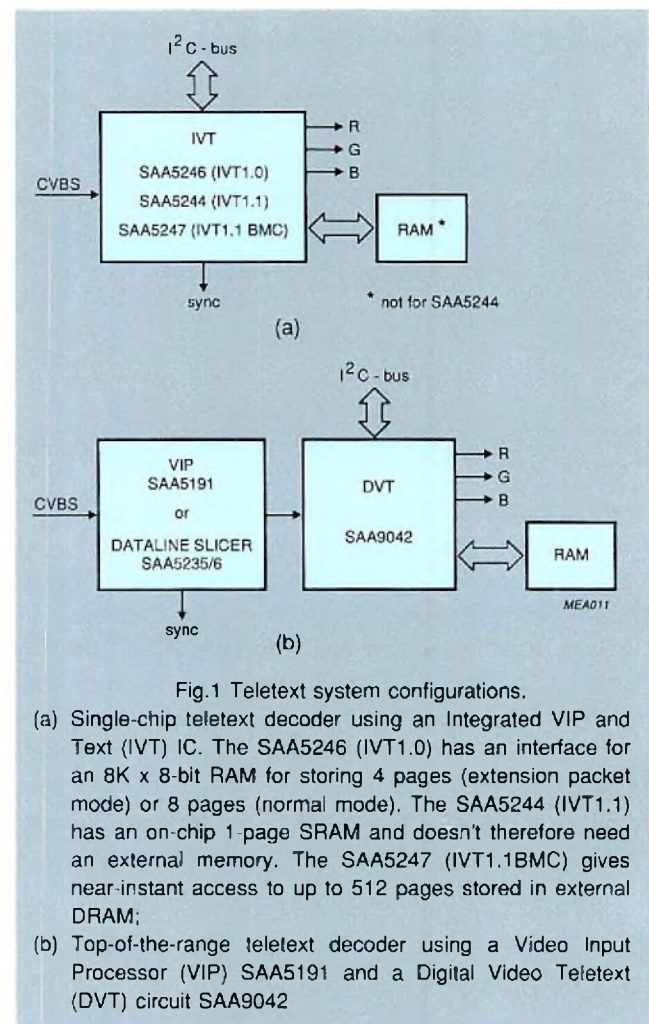

Fig.1 Teletext system configurations.
(a) Single-chip teletext decoder using an Integrated VIP and Text (IVT) IC. The SAA5246 (IVT1.0) has an interface for an 8K x 8-bit RAM for storing 4 pages (extension packet mode) or 8 pages (normal mode). The SAA5244 (IVT1.1) has an on-chip 1-page SRAM and doesn't therefore need an external memory. The SAA5247 (IVT1.1BMC) gives near-instant access to up to 512 pages stored in external DRAM;
(b) Top-of-the-range teletext decoder using a Video Input Processor (VIP) SAA5191 and a Digital Video Teletext (DVT) circuit SAA9042

SINGLE-CHIP INTEGRATED VIP AND TEXT (IVT) CIRCUITS

This new family of single-chip Integrated VIP and Text ICs (IVT) for decoding 625-line based World System Teletext (WST) transmissions are all based on a combination of our well-established Enhanced Computer Controlled Teletext (ECCT) circuit SAA5243, with some additional features, and our Video Input Processor (VIP2) SAA5231.

The VIP section of these new ICs uses new mixed analog and digital circuitry for data slicing and the display clock PLL functions. This has allowed us to considerably reduce the number of peripheral components required and to completely eliminate all close tolerance and adjustable components from the peripheral circuitry.

Features common to the entire family of IVT circuits are:

- complete single-chip teletext decoders
- single +5 V power supply
- simple control via a microcontroller and the I^2C-bus
- use of a digital data slicer and display clock PLL minimizes the number of peripheral components
- support both video and scan-related synchronization modes
- RGB interface to standard colour decoder ICs has a push-pull output and requires only two external resistors
- data capture performance is comparable to that of our VIP2 video input processor SAA5231
- optional storage of packet 24 in the display memory
- teletext signal quality, video signal quality, 625/525-line video input, and the language/ROM variant in use can all be read via the I^2C-bus
- automatic odd/even field output with software override for de-interlacing circuits
- the display PLL can be made to free-run, and the rolling header can be disabled via the I^2C-bus
- VCS to SCS mode for stable 525-line status display
- 25th display row for software-generated status messages or FLOF/FASTEXT/TOP prompts
- software selection of field flyback or full-channel data acquisition.

Single-chip integrated VIP and Text IC SAA5246 (IVT1.0)

The first member of our IVT family is the SAA5246 (IVT1.0) which is an ECCT look-alike which interfaces with an external 8K × 8-bit SRAM for storing eight pages (normal mode) or four pages (extension packet mode). Unique features of the SAA5246 are:

- available in a DIL-48, QFP-64 or SDIL-52 plastic package
- four independent acquisition circuits
- interfaces with 8K × 8-bit SRAM
- software compatible with ECCT systems
- packet 8/30/2 mapped to different extension chapter to facilitate VCR programming
- currently available language variants:
  - **SAA5246P/E**: West European
  - **SAA5246P/H**: East European
  - **SAA5246P/T**: Euro-Turkish
- improved display of accented characters
- suitable for FASTEXT and TOP
- automatic Hamming checking of FASTEXT extension packets
- extension packet capture for extended languages
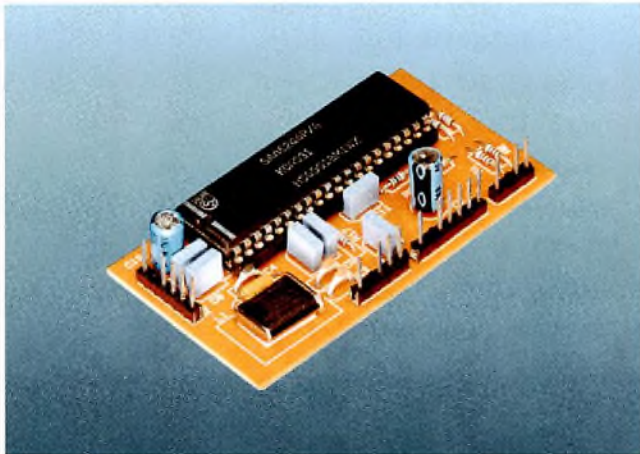- maximum supply current: 128 mA.
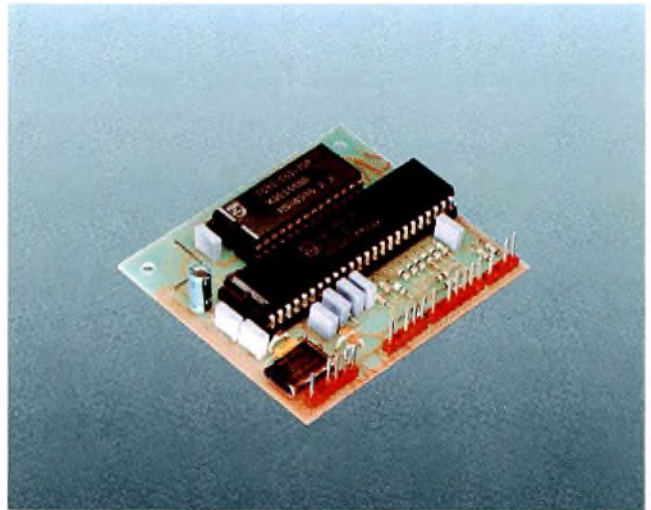
Evaluation board for a complete single-chip World System Teletext decoder (excluding microcontroller) using SAA5246 (IVT1.0) in a DIL encapsulation.

Single-chip integrated VIP and Text IC SAA5244 (IVT1.1)

The second member of our IVT family, the SAA5244 (IVT1.1) which has a built-in 1.3 K × 7-bit SRAM which can store one teletext page plus extension packets for FASTEXT and is therefore truly a 1-chip teletext system. Other unique features of this IC are:

- DIL-40, QFP-44 or SDIL-42 plastic package. The DIL package is "pin-aligned" with that of the IVT1.1BMC circuit (SAA5247)
- single-page acquisition system
- no external RAM needed
- some software compatibility with IVT1.0 (SAA5246)
- 32 supplementary characters for on-screen display
- suitable for user-friendly FLOF interface
- currently available language variant:
  - **SAA5244P/A**: West European (not Spain)
- maximum supply current: 148 mA.

Evaluation board for a complete single-chip World System Teletext decoder (excluding microcontroller) using SAA5244 (IVT1.1)

Single-chip integrated VIP and Text IC SAA5247 (IVT1.1BMC)

The third member of our IVT family, the SAA5247 (IVT1.1BMC) is very similar to the IVT1.1. It has the same features but also includes background memory control (BMC) to give "instant access" to up to 512 pages stored in external DRAM. It also has the following unique features:

- DIL-48 plastic package which is "pin-aligned" with that of the IVT1.1 circuit (SAA5244)
- directly interfaces to 256 K × 4 bit and 1 M × 4 bit DRAMs
- stores every page transmitted by the broadcaster
- access to any page in a maximum of half a second
- software compatible with the IVT1.1 circuit (SAA5244)
- on-chip display RAM of 1.3 K × 8 bits
- suitable for FLOF/FASTEXT and TOP
- currently available language variant:
  - **SAA5247P/A**: West European (not Spain)
- maximum supply current: 180 mA.

DIGITAL VIDEO TELETEXT (DVT) CIRCUIT SAA9042

This I^2C-bus controlled IC acquires, decodes and displays 625-line and 525-line World System Teletext in an analog, digital or features TV set. It is used with a teletext video input processor (VIP SAA5191) or a dataline slicer (SAA5235/6) for data regeneration, and a single-chip 64 K × 4-bit or 256 K × 4-bit DRAM page memory.
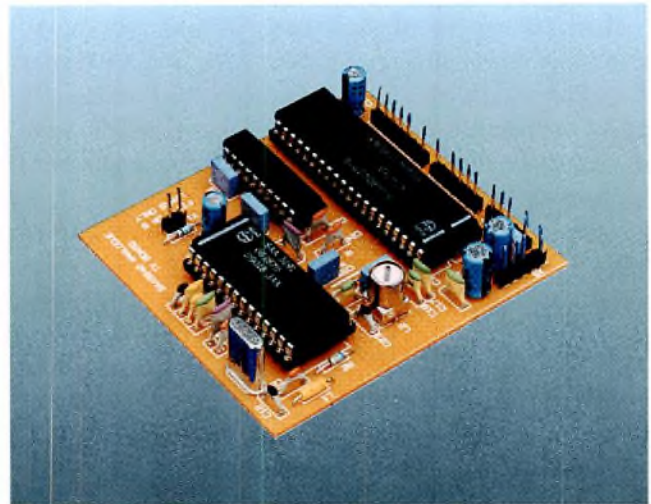
Evaluation board for a complete World System Teletext decoder (excluding microcontroller) using Video Input Processor (VIP) SAA5191 and Digital Video Teletext (DVT) circuit SAA9042

Features
General

- directly interfaces up to 1 Mbit of DRAM
- fully independent acquisition and display timing
- three display modes:
  - normal
  - 32 kHz (progressive scan)
  - 100 Hz/120 Hz (field doubling)
- single +5 V power supply.

Acquisition

- simultaneous update of up to 8 pages
- up to 100-page memory capability
- software selectable 625/525-line operation
- VBI and full-channel operation.

Display

- stable display by slaving from scan-related timing signals

- automatic selection of up to seven different languages

- software controlled RGB level eliminates the need for hardware adjustment

- up to 27 display rows; 0 to 24 plus 1 or 2 status rows.

TELETEXT VIDEO INPUT PROCESSORS

A teletext video input processor (VIP) IC extracts the teletext data from the composite video, regenerates the clock and provides teletext data output for applying to a digital video teletext (DVT) IC or an enhanced computer-controlled teletext (ECCT) IC.

Teletext video input processor (VIP) SAA5191

This IC is for use with our DVT circuit SAA9042. It has:

- high-performance adaptive data slicer

- data clock regenerator

- 13.5 MHz character display clock derived from a PLL including an adaptive sync separator; the design of the PLL allows the display to be locked the TV line scan for stable status messages.

Teletext video input processor (VIP2) SAA5231

This IC is for use with our ECCT circuits SAA5243P and SAA5245P. It has:

- high-performance adaptive data slicer

- data clock regenerator

- 6 MHz character display clock derived from a PLL comprising an adaptive sync separator, horizontal pulse detector, and VCO; the design of the PLL allows the display to be locked to a VCR for stable status messages.

ENHANCED COMPUTER-CONTROLLED TELETEXT (ECCT) CIRCUITS

The combination of our SAA5231 teletext video input processor (VIP2) and an enhanced computer-controlled teletext (ECCT) IC from our SAA5243/45 series forms the heart of most existing World System Teletext decoders.

These two ICs are recognized as industry standards and have outstanding performance, especially under adverse reception conditions. A decoder built with these two ICs:

- performs all the World System Teletext decoding functions

- is controlled via a microcontroller and the I^2C-bus for design flexibility

- has a 192-character set

- covers most major languages

- can automatically select national character sets

- incorporates software selection of field flyback or full-channel data acquisition

- handles up to four simultaneous page requests

- has a 25th display row for software-generated status messages or FLOF/FASTEXT/TOP prompts

- available language variants:
  - **SAA5243P/E**: Western Europe
  - **SAA5243P/H**: Eastern Europe
  - **SAA5243P/K**: Arabic and English
  - **SAA5243P/L**: Arabic and Hebrew
  - **SAA5243P/R**: Baltic States and Cyrillic
  - **SAA5243P/T**: Euro-Turkish
  - **SAA5245P/A**: languages of the Americas.
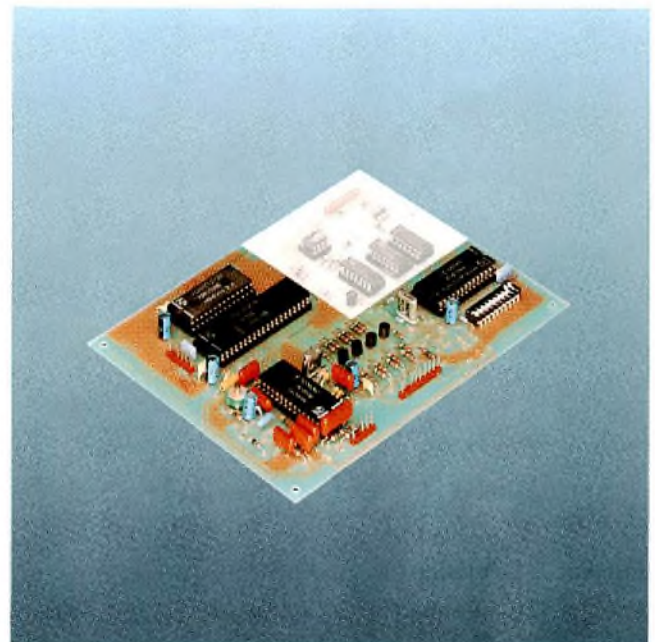
Evaluation board for a complete World System Teletext decoder (including microcontroller) using Video Input Processor SAA5231 (VIP2) and ECCT circuit SAA5243P/E. The screened area is not part of the teletext decoder

SOFTWARE SUPPORT

Philips have always supplied software to support design-in activities so that TV set manufacturers can quickly evaluate new teletext products and features at little expense. However, since the volume of software required for a modern TV set is constantly increasing, its cost, relative to the cost of the hardware, is also increasing. This is why we now offer TV set manufacturers a range of production-ready software packages called SAFARI (Stand-Alone FASTEXT And Remote Interface) as shown in the Table.

SAFARI software packages incorporates built-in options that can be 'link'-selected by the set manufacturer to allow design of a range of high-performance, state-of-the-art text decoders covering numerous market requirements.

SAFARI software packages

CTV971S	As CTV970S + additional OSD capabilities
CTV972S	As CTV971S + X/26 decoding (Europe)
CTV973S	As CTV971S + TWIST + X/26 decoding (Arabic)
CTV974S	CTV972S variant (W.Europe + Turkey)
CTV975S	CTV971S variant for 525-line ECCT IC SAA5245P
CTV976S	CTV973S variant (Baltic, Greece, Yugoslavia)
CTV990S	TOP (Table Of Pages) decoding
SAA9042 R1.1	Multi-page FASTEXT using DVT (Demo. only)

SAFARI features

- displays all the standard World System Teletext pages currently transmitted
- translates all the language extension packet information for displaying on the screen
- decodes Full Level One Features (FLOF/FASTEXT) teletext
- automatic page pre-capture
- index and page up/down function
- user-controlled LIST mode option can store four favourite page numbers per channel in a non-volatile memory
- pages N-1, N+1 and N+2 requested in non-FLOF transmission
- browse function
- on-screen status display
- automatic switching to full-field operation (via packet 8/30)
- incorporates factory test facilities
- interfaces to many TV tuning and control software packages.

Further information

For further information regarding the availability of software, please contact one of the addresses on the back cover. For information on related subjects, please refer to "Documentation on ICs for consumer applications" ordering code 9398 374 30011.

An integrated chipset for cellular mobile telephones

TREVOR HALL AND PETER HART

Cellular mobile telephones have been with us now for several years. The first equipments were complex, highly priced and affordable only by the business sector. However, a rapid increase in the number of users has steadily reduced the price to the consumer and opened up a wider market. In order to remain competitive, set makers must continue to strive towards reduced costs. and the path to achieving this aim is the adoption of an optimum architecture which minimizes the complexity through extensive use of VLSI.

Existing sets comprise a mix of analog functions performed by standard integrated circuits, and digital functions performed by custom/semi-custom circuits. But the development of a six chip-set approach using bipolar and CMOS technologies, where appropriate, achieves a more optimal solution.

OVERALL ARCHITECTURE

Figure 1 shows the architecture adopted and is suitable for both AMPS and TACS systems. Careful attention to low current consumption has resulted in a chipset targeted at portables, transportables and mobiles.
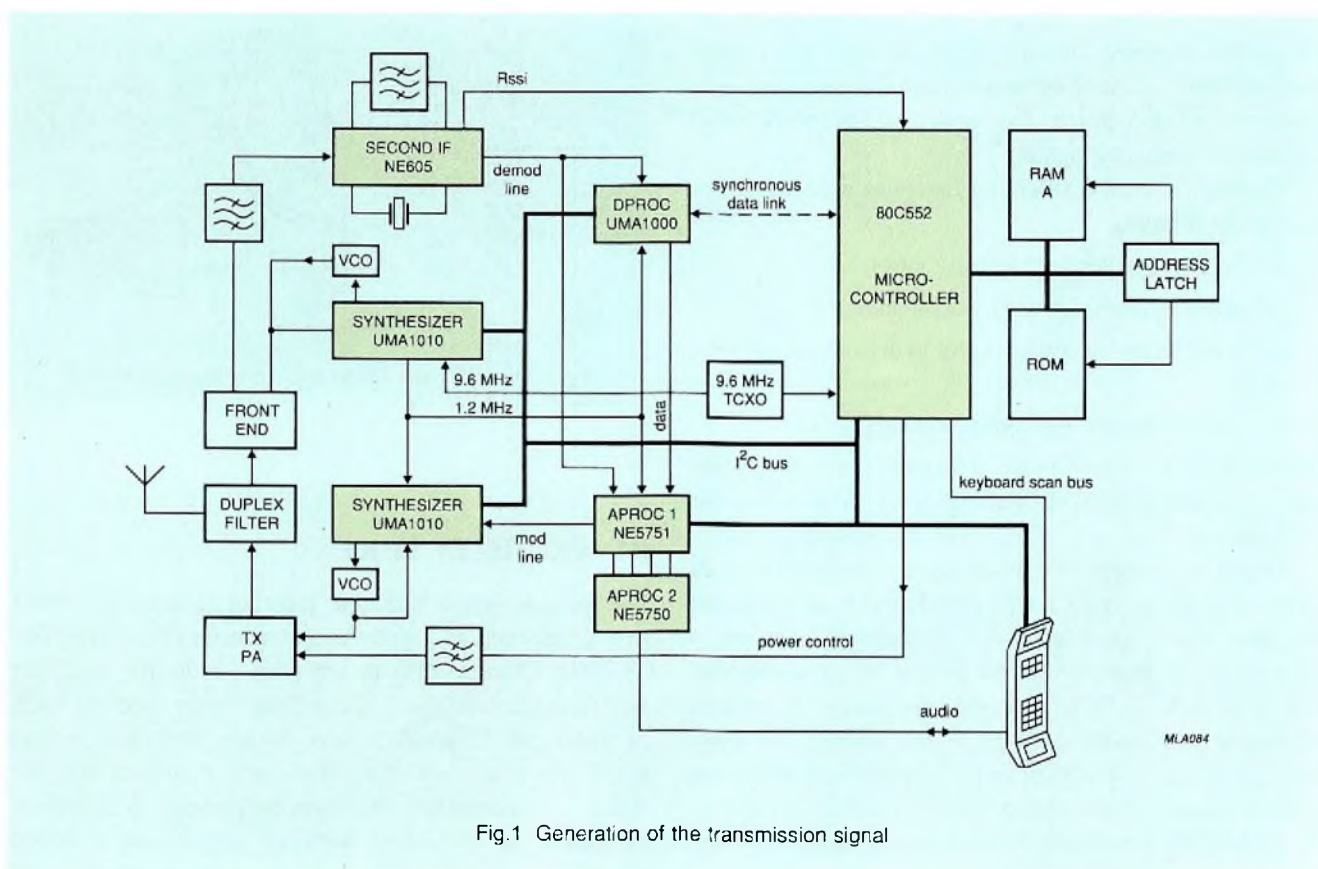

Fig.1 Generation of the transmission signal

The RF section comprises a single-chip frequency synthesizer, and a single-chip second mixer/oscillator/IF amplifier/demodulator.

VLSI has been used to greatest effect in the baseband processing area. A single CMOS data processor IC performs all functions associated with control data, supervisory and signalling tones.

All voice, alert and DTMF functions are contained on two audio processor devices, one CMOS and the other bipolar. Switched capacitor integrated filter technology, used in all baseband processing functions, achieves the minimum number of external passive components.

A single 9.6 MHz TCXO is used as the clock source for the whole chipset; the microcontroller and the receiver frequency synthesizer are clocked directly from this source.

The reference frequency chain of the frequency synthesizer includes a divide-by-eight sub-clock output of 1.2 MHz. This is used as the clock source for both data and audio processing. Using the 1.2 MHz clock for these functions reduces current consumption, and with all clocks derived from a single source there should be no problems with aliasing or beat frequencies.

A cellular mobile telephone spends the majority of its operational life in idle mode monitoring the data streams being sent on the control channels. Reduced current consumption in this mode is important to maximize up-time between battery charges. The microcontroller and associated memory is a major source of current consumption, so the data processing function has been fashioned to maximize the time the microcontroller operates in a standby mode.

There are a number of circuit functions which need the transmitter disabled:

- the microcontroller for system control

- frequency synthesizer when out of lock

- audio processor for VOX control in discontinuous voice mode

- and data processor for control channel access.

Disabling of the transmitter is performed by a single line with controlling devices 'pulling low' in a wired-OR configuration.

The two-wire serial I²C-bus is used to communicate all control data between the microcontroller and the peripheral circuitry. This offers a number of advantages including a reduced pinout requirement, the smaller IC encapsulation, and both reduced PCB area and complexity. In present equipment, the multi-layer PCB is possibly the most expensive single component so the chipset facilitates using a much cheaper board with a reduced number of layers.

Adding features to the basic chipset is simple because a wide range of I²C-bus compatible devices is available.

The microcontroller is used as the system master for normal operation of the six-chip set, but multi-master operation is a feature of the I²C-bus and this can be very useful for production testing.

I²C BUS

The I²C bus provides the main control highway of an equipment (Fig.2). Essentially it provides a local area network for integrated circuits. Each IC has its own 7-bit address and is connected to the two-wire serial bus. The interface protocol is self-checking and self-arbitrating, allowing more than one master controller in the system at the same time. Data is transferred at up to 100 kbps as a message block consisting of device address, a read/write control, and a data block.

The multi-master facilitates a simple test harness taking full control of the equipment for complex functional system tests and alignment during production. Test functions of the ICs not used in normal operation can be exercised in this way.
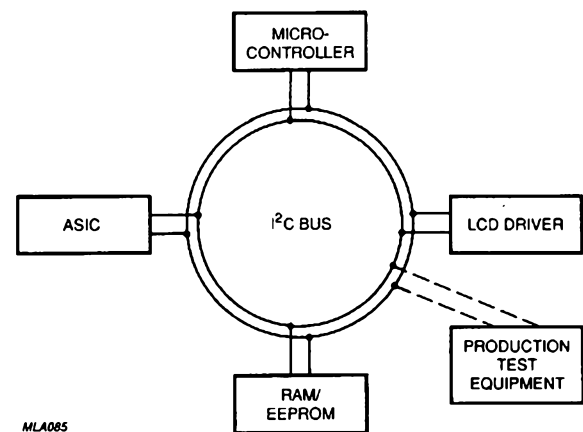

Fig.2 NE5750 and NE5751 audio processor schematic

RF ARCHITECTURE

The receiver adopts a double superhet architecture with a first IF between 45-100 MHz and a second IF of typically 455 kHz. Discrete devices are used for the RF amplifier and first mixer stages. The second mixer, second local oscillator, all IF amplification, limiter, demodulator and RSSI functions, are integrated into a single-chip; the NE605. It is operable with input frequencies to the mixer in excess of 500 MHz with IF amplification up to 25 MHz.

The receiver's first local oscillator is a single-loop frequency synthesizer normally operating at the first IF above the reception frequency. In order to reduce component count and complexity, the traditional 3-chip approach to frequency synthesizers (prescaler, divider/comparator and loop filter) has been combined into a single IC. Two variants are available; the UMA1012 for up to 550 MHz, and the UMA1010 for between 400 MHz and 1150 MHz. In other respects the devices are identical. Features include; a low RF drive requirement, digital and analog phase comparators for both fast locking and low spurious outputs, power-down, and low current consumption.
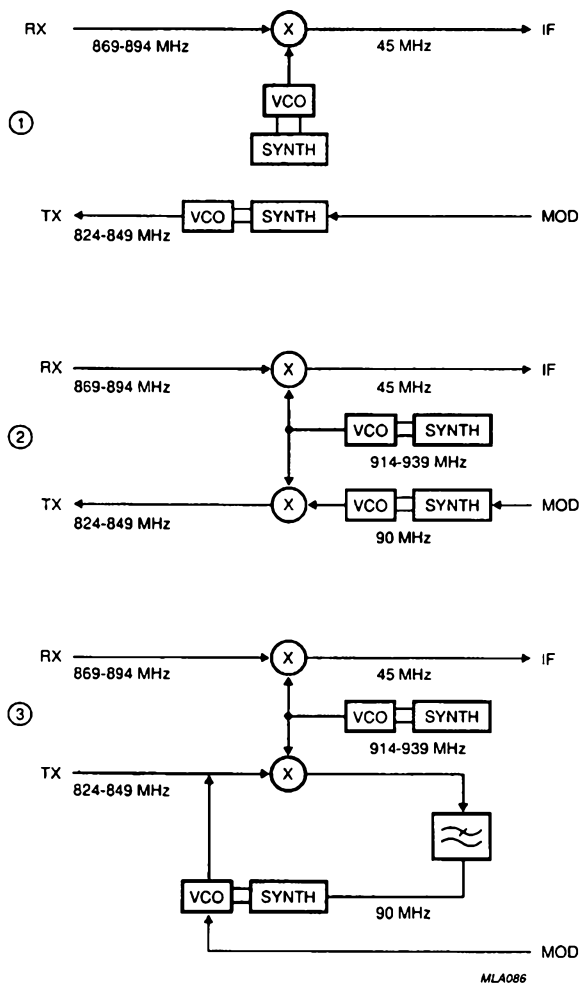
Fig.3 UMA1000T data processor block diagram

The RF transmission signal can be derived in a number of ways (Fig.3) with the UMA1010 or UMA1012 as appropriate. The first method uses a separate frequency

synthesizer, similar to the receiver local oscillator but operating at the transmission frequency (Fig.1). An alternative is to operate the synthesizer at half the transmission frequency and use a frequency doubler to alleviate potential transmission pulling problems when the TX PA is activated.

The second method uses a fixed VHF synthesizer frequency of 45 MHz (the duplex distance) + RX IF. This is mixed with the receiver local oscillator to give the transmission signal. A bandpass filter is used to suppress the mixer image and oscillator feed-through. The fixed-frequency VHF source is modulated, and for this reason, a synthesizer has been employed in preference to a crystal oscillator with which it would be difficult to produce sufficient frequency deviation.

The third method uses a mixer-loop synthesizer to derive the transmission signal. A VCO output operating at the transmission frequency is mixed with the receiver's local oscillator output and the difference frequency is extracted by a low-pass filter. This frequency (45 MHz + the receiver IF) is input to the VHF synthesizer.

In all three methods, modulation is applied to the transmit VCO. A loop bandwidth of around 200 Hz is used in the transmitter synthesizer path, achieving a flat modulation characteristic above 300 Hz and permitting sufficiently fast switching time.

Hybrid power modules are used to amplify the transmit signal to the level required according to the power class of the equipment. A range of modules has been developed for different power classes, supply voltages and drive requirements. Power modules offer the advantages of minimising development time, reducing manufacturing and assembly costs, small size and zero alignment.

The cellular system requires the transmit power to be reduced in 4 dB steps down to 6 mW. To achieve a flat characteristic, independent of gain spreads in the amplifier stages, a power levelling loop external to the PA module is used. The output of the power module is adjustable by varying the supply voltage to one or more of the amplifier stages. A power sensor in the output of the transmitter generates a DC voltage related to the transmitter output power. This can comprise a simple diode detector, or a more complex system using a coupler with multiple sensing to reduce sensitivity to load VSWR. The sensor output is compared with a reference DC level using a voltage comparator and the difference used to control the power output. The loop will settle, such that the sensor output will be equal to the reference level. The reference level is derived directly from the microcontroller and is set according to the required output power. Non-linearities in the sensor may be accommodated by suitable software calibration of the reference level.

AUDIO PROCESSING FUNCTIONS

All audio functions associated with the voice channel are processed in two integrated circuits (Fig.4). Microphone amplification, VOX provision, compression, expansion and audio power output are provided in a bipolar IC, the NE5750. All filters, pre-emphasis, deviation limiting, de-emphasis, signal path switching, volume control and tone generation are provided in a CMOS IC, the NE5751. Switched capacitor techniques have been used to integrate fully all filter functions. The tone generator is used for DTMF signalling, ringing tones and key confirmation. The pinouts of the two ICs have been arranged so that a straightforward interconnection is achieved on the PCB layout. Access to different parts of the audio signal path is inherent in this approach and eases the connection of ancillary units such as modem, hands-free adaptor etc.

DATA PROCESSING FUNCTIONS

All functions associated with control data, supervision and signalling are incorporated into a single-chip CMOS data processor, the UMA1000 (Fig.5). The architecture and the interfacing with the microcontroller have been designed to minimize overall current consumption and software requirements.

In the reception path, the UMA1000 provides slicing, clock recovery, word synchronization, majority voting and error correction. A dedicated two-wire asynchronous bus passes the fully decoded data word to the microcontroller. Clocking is under control of the microcontroller and is not time critical. With this arrangement, the microcontroller with associated memory can remain in a low current standby state for a significant fraction of time - typically 90% when monitoring control channels. When operating on
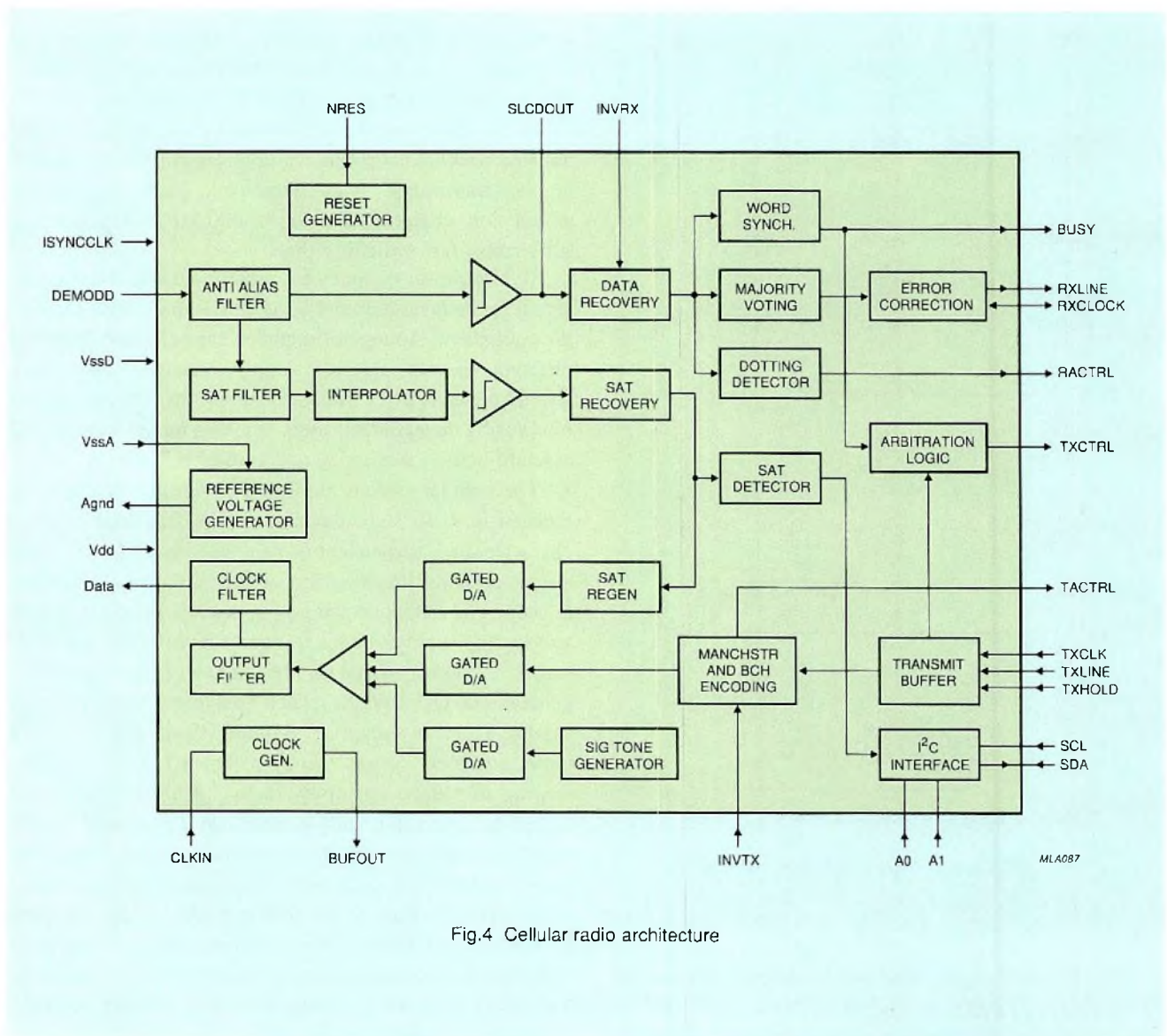

Fig.4 Cellular radio architecture

a voice channel, a dotting detector detects bit synchronization preceding a data burst. This is used to blank the audio path directly to prevent data bursts from being heard by the user. In the transmission path, the device incorporates error encoding, word formatting and filtering. The data message to be transmitted is passed from the microcontroller to the data processor via the serial link where it is held in a buffer. The microcontroller can trigger immediate transmission of the data at the appropriate time. The base station returns the status of the channel access within the busy/idle stream. If the busy/idle stream does not revert to 'busy' during the specified window,

transmission is aborted. This time-critical sequence is performed by the data processor IC independent of the microcontroller.

The data processor also provides the signalling tone and supervisory tone functions. SAT signals are isolated from the voice channel by a narrow bandwidth switched capacitor input filter. Two digital PLLs and counters achieve SAT determination and transponding, resulting in a very robust SAT processor.

The data processor achieves virtually zero external component count with a particularly low current consumption of 2.8 mA.
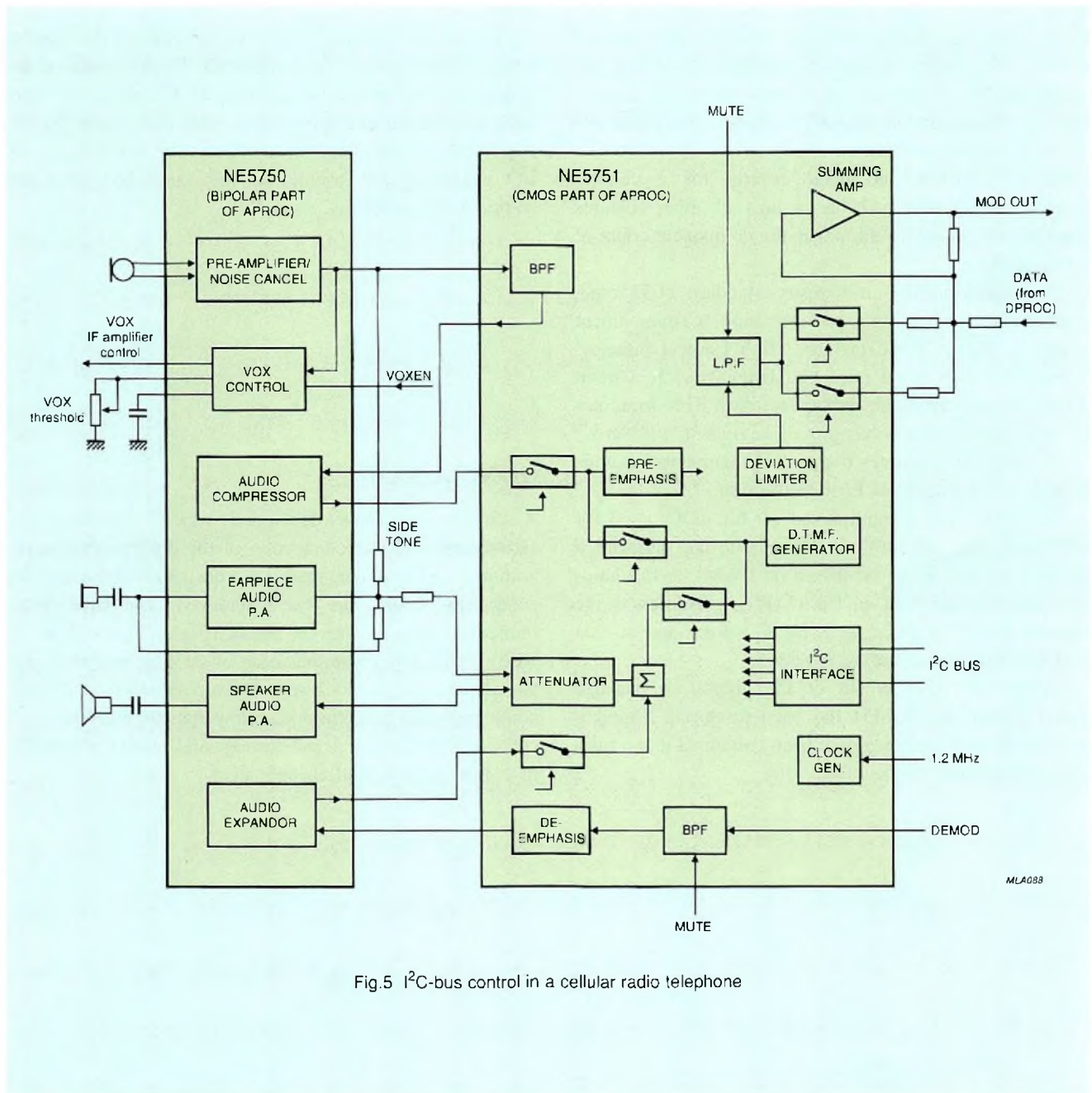

Fig.5 I²C-bus control in a cellular radio telephone

MICROCONTROLLER

The microcontroller handling the functions of a cellular portable must satisfy the two conflicting requirements of low power and high operating speed. These two main requirements can be met with the PCB80C552, a derivative of the 8051 microcontroller. This processor, constructed in CMOS technology will operate with an instruction cycle time of less than 1 μs, and about 50% of the operations execute in one cycle. However this device also supports extensive power saving modes, giving around 75% power saving in a standby mode, and a micro-power power-down mode for backup battery operation. The low power modes ideally complement the UMA1000T data processor. This device processes the continuous cellular data stream, decodes and buffers complete messages, enabling the microcontroller to operate in a burst processing mode. Thus the processor may spend in excess of 90% of the time in a standby mode.

Having satisfied the main criteria for a cellular portable, the PCB80C552 has a host of other features which help to simplify and reduce the component count of an equipment.

The processor has an industry standard 8052 core, which gives access to an extensive range of development support facilities. These include 'High Level Language' support (PL/M51 - a Pascal like language), 'In Circuit Emulation' and symbolic debug facilities. This promotes fast development and debugging of equipment software.

The processor operates over a wide temperature range and has a high degree of EMC protection.

The device has a multiplexed 10 bit ADC, used for RSSI processing, battery voltage monitoring etc, and a pseudo 8 bit analog output (based on PWM). A full hardware implementation of an I²C UART in addition to the standard RS232 UART, six 8 bit I/O ports and an 'on chip' watchdog timer are all included.

During the development of the chipset, a package written entirely in PL/M51 has been produced. Together the software and hardware have been combined into a fully functional cellular radio.

OTHER I²C PERIPHERALS

In addition to the major components of the Cellular Radio Chipset, there are a large number of general purpose peripheral ICs with I²C interfaces. For example; the PCF8576 is one of a range of LCD matrix and segment drivers. This device can address up to 160 segments, and is cascadeable for larger displays. It is available in TAB packaging, allowing the device to be directly mounted onto a flexible connector driving the LCD. With only a six wire connection to the main PCB (power, I²C and contrast control), this again shows cost advantages in the reduction in PCB area over that needed for normal direct LCD drivers.

This device exhibits most of the advantages that can be attained when using I²C peripherals for the addition of features to any particular equipment. The range of such devices cover most requirements, with the availability of EEPROMs, RAMs, clock/calendars, tone generators and I/O expanders, all usable on the same bus with no compatibility problems.

CONCLUSION

A chipset has been developed which simplifies the architecture and interconnection of the different functions within a cellular telephone. A substantial reduction in component count has been achieved, compared with implementations in current use, through the adoption of VLSI, serial intercommunication of control functions and the use of a single clock source. This reduction in overall complexity shortens equipment development time, reduces costs in manufacturing and testing, and results ultimately in a more reliable and cheaper item.

TDA4670 Picture Signal Improvement (PSI) circuit

PETER KELTING

The quality of a TV picture can be enhanced by correcting the degradation of definition caused by the bandwidth limitations imposed on the chrominance and luminance signals by their separation filters. Philips' unique Picture Signal Improvement (PSI) IC, the TDA4670, which is a successor to our well-known Colour Transient Improvement (CTI) circuit TDA4565, achieves this by considerably improving the quality at the vertical edges of the features in the picture, see Fig.1. The IC contains two main sections. The first section, colour-difference signal processing, consists of Colour Transient Improvement circuitry which improves the colour definition of the display by decreasing the rise and fall times of the colour-difference signal transients. The second section, luminance signal processing, comprises a variable luminance delay line with aperture correction (luminance signal peaking) and noise reduction by coring. This not only ensures coincidence of the luminance and colour-difference signals on the display, it also enhances the contrast. All these functions and parameters of the TDA4670 are selected and controlled via the I²C bus[*].

At the vertical edges of a feature in the picture the minimum transient times are 150 ns for the luminance signal and 800 ns for the colour-difference signals due to their restricted bandwidths (e.g. 5 and 1.3 MHz for the PAL B/G transmission standard). To improve the luminance signal transient response and thereby enhance the contrast, PSI superimposes symmetrical overshoots on the luminance signal transient. This aperture correction (peaking) amplifies the high-frequency content of the luminance signal, but it also increases the noise level. These increased noise levels in areas of the display with little structural change are attenuated by a coring stage.

To improve the colour-difference signal transient response, the output signal is retained at its pre-transient value during the transient and is switched to its new signal level at the end of the transient. Colour Transient Improvement establishes approximately the same rise and fall times for the colour-difference signal transients as those of the luminance signal at the vertical edges of the features in the picture. The additional luminance signal delay to compensate for the colour-difference signal delay introduced by CTI is provided by a delay line consisting of all-pass active filter stages.
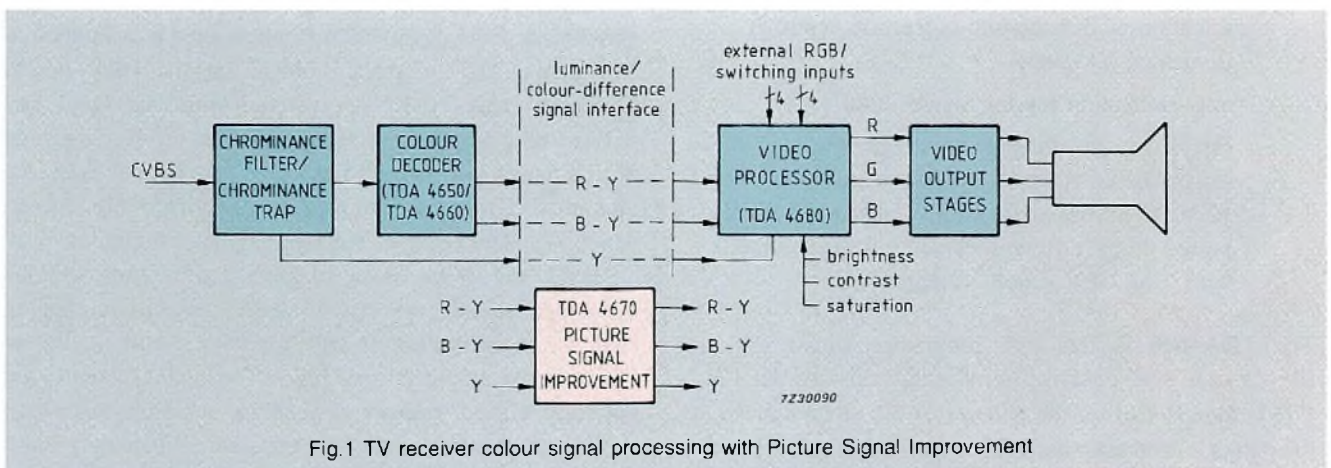

Fig.1 TV receiver colour signal processing with Picture Signal Improvement

The TDA4670 contains the following features:

- CTI circuits to decrease the rise and fall times of the colour-difference transients to those of the luminance signal

- adjustable luminance signal peaking, with symmetrical pre- and post- overshoots superimposed on the transient (aperture correction)

- noise reduction in areas of the picture with relatively small changes in the picture content due to amplitude suppression of low-level signals by coring

- selection of the luminance signal delay in steps of 45 ns to achieve a maximum delay difference between luminance and colour-difference signals of ±22.5 ns (a 22.5 ns delay difference is not noticeable to the viewer)

- automatic luminance signal delay adjustment using an internal control loop, with the horizontal line frequency as a reference, which corrects production tolerances in the delay line, temperature and supply voltage changes

- gated clamping to an internal reference voltage for both the luminance and colour-difference signals to establish signal-independent, reference black levels for all three signals

- minimum number of external components; the CTI capacitors are integrated on the chip, only the peaking, coring, black level clamp and the luminance delay control loop capacitors are external to the TDA4670

- external control via the I²C-bus enables the following parameters to be controlled:

  - Colour Transient Improvement on/off

  - selection of the luminance signal delay in steps of 45 ns between 20 and 1155 ns

  - selection of the value of aperture correction (4 values)

  - selection of the aperture correction centre frequency (2 values)

  - noise reduction (coring stage) on/off

  - establishes the threshold voltage levels in the sandcastle detector for sandcastle pulses of 5 or 12 V, to ensure compatibility of the sandcastle pulses from different synchronization circuits with 5 or 12 V supply voltages.

The TDA4670 is fed with luminance signal (Y) and (R − Y), (B − Y) colour-difference input signals, see Fig.2. CTI is independent of the polarity of the input signals, i.e. the colour-difference signal inputs can have either positive or negative polarity. Therefore, the TDA4670 can be conveniently inserted between a multi-standard colour decoder and a video processor with negative colour-

difference signals on both interfaces. Since the amplitudes of the input and output signals are consistent for each of the signal paths, the TDA4670 can be included in any design with a luminance/colour-difference signal interface. If the TDA4670 is used with a large-area flicker reduction TV receiver (field frequency = 100 Hz), then the TDA4670 must be positioned before the feature module.

The nominal input and output signals of the TDA4670 for a 75% colour-bar signal are:

- VBS/luminance signal (Y) input/output: 0.45 Vpp

- (R − Y) colour difference signal input/output: 1.05 Vpp

- (B − Y) colour difference signal input/output: 1.33 Vpp.

COLOUR-DIFFERENCE SIGNAL PROCESSING

Colour-difference transients at the vertical edges of the features in the picture (with minimum rise and fall times of 800 ns) are more than five times as long as those of the corresponding luminance signal (150 ns) due to their restricted bandwidths. The principle of CTI operation is to retain the colour-difference output signal at its pre-transient value during the transient, and to switch the colour-difference signal to the new signal level only when the transient is finished. The resultant colour-difference transients have approximately the same rise and fall times as the luminance signal, due to this switched equalizer technique. However, the luminance signal has to be additionally delayed to obtain coincidence of the luminance and colour-difference transients on the display.

The input colour-difference signals are fed through gated black level clamp circuits where they are clamped to an internal DC reference voltage on the back porch. Clamping pulses (BK) are derived from the burst key pulses, the clamping is active 1 μs after the leading edge of the burst key pulse. The input capacitors store the internal DC reference voltage to establish a black level which is independent of the input signal amplitudes.

From the black level clamp circuits, both colour-difference signals are fed to buffer amplifiers, analog switches incorporating storage capacitors, and finally, to output buffer amplifiers, see Fig.2. The analog switches are normally closed, but are opened for a colour-difference signal with a sufficiently fast transient. When they close again at the end of the colour-difference transient, the total impedance of the buffer amplifiers plus the analog switches is so low that the storage capacitors charge quickly.
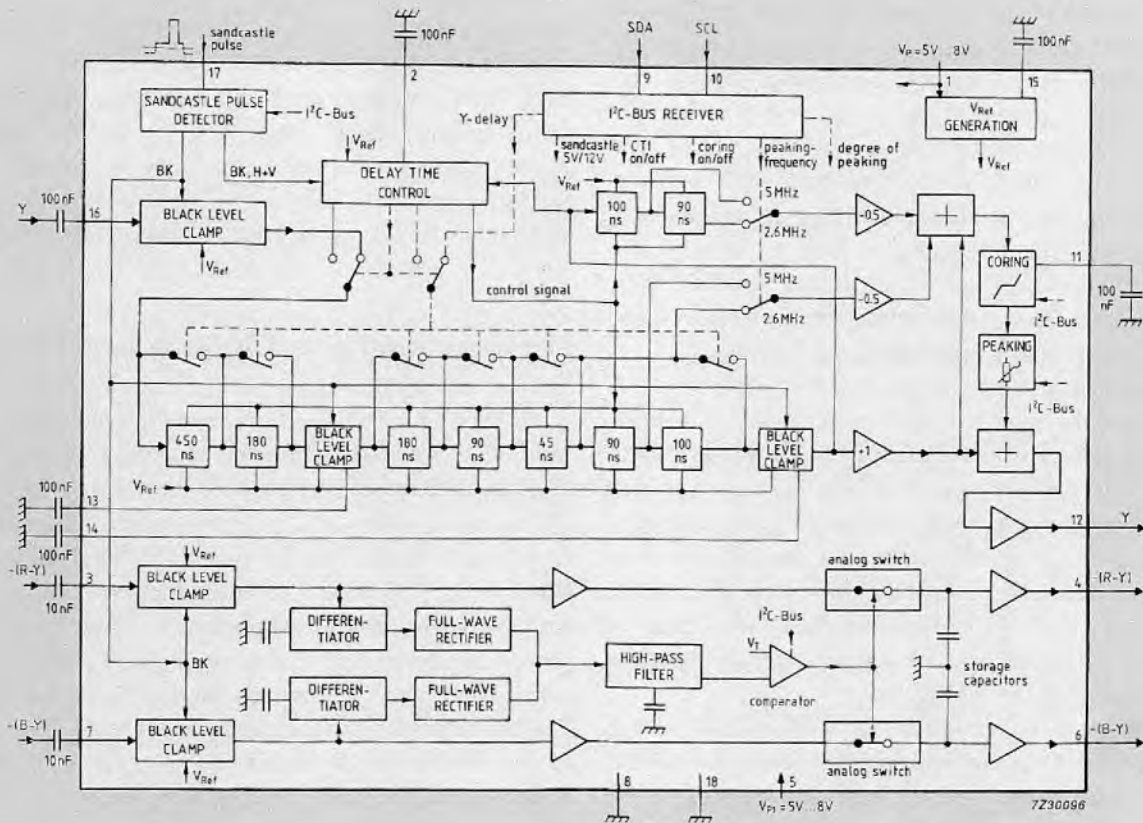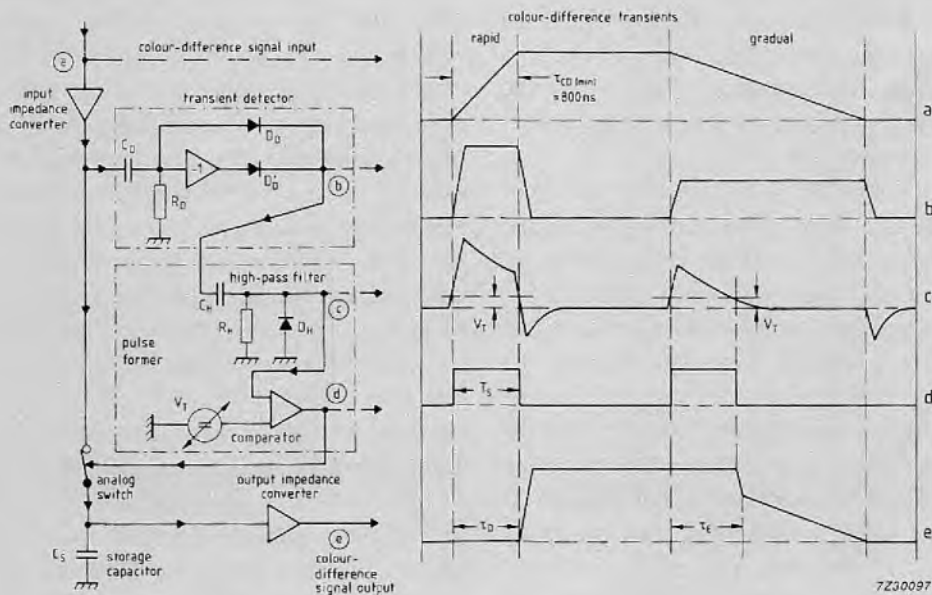
Fig.2 TDA4670 block diagram

Fig.3 CTI circuit and waveforms

Both analog switches are switched synchronously by a circuit consisting of differentiators, full-wave rectifiers, a high-pass filter and a comparator. Figure 3 shows the arrangement for one of the colour-difference signals. The positive voltages generated by rising or falling colour-difference transients at the full-wave rectifier outputs are added and fed through the high-pass filter to the comparator. On the second input of the comparator is a DC voltage V_T. When the high-pass filter output is greater than V_T the comparator opens both analog switches. Both analog switches are opened when one or both colour-difference signals has a sufficiently fast transient.

The transient detector, consisting of the differentiator (C_D, R_D) and the full-wave rectifier, generates a voltage which is proportional to the gradient of the colour-difference transient, Figs 3(a) and 3(b). The full-wave rectifier output is zero when the colour-difference signal is constant. The pulse former, consisting of the high-pass filter and the comparator, determines the time for which the analog switches are open, Figs 3(c) and 3(d). This time is approximately equal to the defined colour-difference transient time $R_H C_{11}$ (≈ 800 ns).

For the rapid colour-difference transient the analog switches are open for the total transient time. The colour-difference signals remain at the levels existing before the transient due to the voltages stored on the capacitors C_S. At the end of the colour-difference transient the analog switches close, and the colour-difference signals increase very rapidly to the new levels (with approximately the same transient times as the luminance signal). The gradual colour-difference transient is also recognized as a transient, but is too gradual to justify closing the analog switches for its total duration. When the voltage defined by time constant $R_H C_{11}$ equals the comparator voltage V_T the colour-difference signals revert to the levels of the colour-difference inputs, as shown in Fig.3(e).

For very gradual colour-difference transients the high-pass filter output voltage does not exceed V_T so that the analog switches remain closed, and the colour-difference signal outputs follow the colour-difference signal inputs. The CTI stage is independent of the order and polarity of the colour-difference transients. For this reason, the TDA4670 operates with both positive and negative colour-difference input signals. It is, of course, necessary, that the colour-difference input signals do not exceed the operating range of the TDA4670. CTI operation can be switched off via the I²C-bus. The analog switches are then constantly closed to inhibit CTI operation. The colour-difference signals with or without colour transient improvement are fed out of the TDA4670 on pins 4 and 6.

LUMINANCE SIGNAL PROCESSING

Luminance signal processing in the TDA4670 is divided into three sections: firstly, luminance signal delay with black level clamping: secondly, automatic adjustment of the luminance signal delay: and thirdly, the aperture correction filter with noise reduction by coring. Since aperture correction also uses delay stages, these are designed to be part of the total luminance signal delay.

Luminance Signal Delay With Black Level Clamping

The luminance/sync signal (VBS) consisting of the luminance signal (Y), blanking signal and the sync signal is fed from the chrominance trap via a coupling capacitor to pin 16. The VBS signal is clamped to an internally-generated DC reference voltage, V_{Ref}. To ensure that the luminance signal is compatible with the limited operating range of the delay stages, V_{Ref} is set to a voltage which is slightly less than the mid-voltage of the luminance signal. Black level clamping is performed on the back porch by the clamping pulses (BK) which are derived from the burst key pulses. The DC reference voltage corresponding to V_{Ref} is stored by the coupling capacitor and is updated every line. The design of the TDA4670 enables it to operate with VBS signal inputs 3 dB greater than the nominal 0.45 Vpp.

The series-connected delay stages are selected independently via the I²C-bus, as shown in Fig.2. The first five switches in parallel with the delay stages select the 450, 2×180, 90 and 45 ns delay stages, the sixth switch selects the two final delay stages of 90 and 100 ns simultaneously. (This final pair are also used for aperture correction in conjunction with a further pair of 90 and 100 ns delay stages). With this sequence of delay stages, and a nominal delay of 20 ns in the remaining circuits, it is possible to select a luminance signal delay between 20 and 1155 ns in steps of 45 ns. The maximum difference between the desired and selected luminance signal delay is therefore less than ±22.5 ns: an error of 22.5 ns between the luminance and colour-difference signals on the picture is so small that picture definition is not affected.

The delay stages consist of cascaded second-order all-pass filter sections. The filter coefficients are selected to maintain an optimally-flat frequency response over the bandwidth of the luminance signal. The frequency response changes very little until the limit frequency is reached (Bessel filter with absolutely no overshoot in the group delay). This provides a constant group delay for the luminance signal which is equal to the delay of the delay stage.

To change the group delay for a specified limit frequency, either the order of the all-pass section is changed, or all-pass sections are connected in series. In the TDA4670 both methods are applied. Each of the delay stages is an all-pass section (with an order between 2 and 12) with an optimally-flat frequency response. All-pass sections with an order greater than two consist of cascaded second-order all-pass sections. A second-order all-pass section can be constructed using two capacitors. However, in the TDA4670, second-order all-pass sections use three capacitors, since the capacitor values are smaller and require less chip area.

The all-pass sections are realized as active RC circuits with a group delay defined by the resistor and capacitor values. The capacitors are integrated on the chip. The resistors are realized by difference-amplifier stages so designed that the transistor conductance is determined by its DC current. By varying the transistor DC current, the transistor conductance, and therefore, the group delay, of the all-pass section is changed. This enables the group delay to be controlled independently of component tolerances and external factors. This dependence of the transistor conductances on their DC currents is the basis for automatic adjustment of the luminance signal delay.

Not only the second-order all-pass sections but also those with an order greater than two are DC-coupled in series, so that any DC offsets will result in a large shift in the DC operating point. To prevent these offsets restricting the operating range of the delay stages, and thereby distorting the luminance signal, two extra black level clamp circuits are introduced to clamp the luminance signal to the internal black level. The first black level clamp circuit is after the 450 and 180 ns delay stages, the second is after the 100 ns delay stage. This extra clamping ensures that the operating range in the TDA4670 is not exceeded as long as the luminance signal input remains within its specified range.

Automatic Luminance Signal Delay Adjustment

The luminance signal delay is determined by the RC time constants of the active all-pass sections. During the manufacture of ICs, absolute tolerances are large but relative tolerances are small by comparison. Therefore, the tolerances of the on-chip resistors and capacitors have relative values which vary little from each other, and have the same deviation from their theoretical values. When the delays of the delay stages are adjusted to their theoretical values by a simultaneous adjustment of all the resistors or capacitors, then all the delay stages have a very small absolute error, singly or when connected in series. In

practice, the DC currents of all the transistors are adjusted simultaneously to establish this very small error in the luminance signal delay.

The transistor DC currents are adjusted simultaneously by an automatic adjustment control loop which compares the actual luminance signal delay with its nominal value. From the difference between these two values a control signal is generated which adjusts the error between the two values to zero. During the automatic adjustment it is not possible to use the luminance signal delay for any other purpose. It is performed during specific lines of the vertical blanking interval when no picture component is transmitted, see Fig.4.

To monitor the actual luminance signal delay a feedback loop is connected around the variable Y-delay line to create an oscillator, the amplifier output is a rectangular oscillator signal, OS. The period of the oscillator signal, T_O, is exactly double the total delay of the Y-delay line, τ_D, plus a small additional delay in the amplifier, τ_A. Therefore:

$$T_O = 2(\tau_D + \tau_A).$$

The factor 2 in the equation is due to the inversion in the amplifier of the output pulse from the Y-delay line. A fixed selection of the available delay stages is used during automatic adjustment, this selects all the delay stages except for one 180 ns delay stage and the final pair of the 90 and 100 ns delay stages for aperture correction. The nominal delay is:

$$\tau_D = (450 + 180 + 90 + 45 + 90 + 100) \text{ ns} = 955 \text{ ns}.$$

The reference or measurement time for automatic adjustment, T_M, is the line period, T_L, less half the duration of the burst key pulse, T_{BK}. Therefore, the measurement time, T_M, is:

$$T_M = T_L - \frac{T_{BK}}{2}$$

With a burst key pulse duration of 4 μs and for the European horizontal scan time of $T_L = 64$ μs, then, $T_M = 62$ μs. T_M is very much longer than the fixed delay used for automatic adjustment, $T_M \gg \tau_D$. Therefore, the delay τ_D is multiplied by 32 during the automatic adjustment. The oscillator signal OS is fed through a 1:32 frequency divider which increases the oscillator signal period to $32T_O$.

Automatic adjustment is based on the assumption that the measurement time T_M, equals the increased oscillator signal period $32T_O$, for exact automatic adjustment. Therefore, by substitution in the equation $T_M = 32T_O$,

$$\tau_D = \frac{1}{64}\left(T_L - \frac{T_{BK}}{2}\right) - \tau_A$$

when T_L = 64 µs, T_{BK} = 4 µs and τ_A = 13.75 ns, then τ_D = 955 ns. τ_D is dependent not only on T_L but also on the duration of the burst key pulse, T_{BK}, and the amplifier delay, τ_A. However, these values are so small relative to T_L, that their effect on the total delay is minimal.

In Fig.4, switch S_2 selects the specific delay stages for automatic adjustment which overrules normal I²C-bus

selection. Switch S_2 is switched by the timing control output TDS (derived from the burst key pulse of line 8 or line 321). The black level clamp circuits have 8 lines (9 – 16 or 322 – 329) after the leading edge of the TDS signal to establish the new black level for the delay stages used for automatic adjustment.
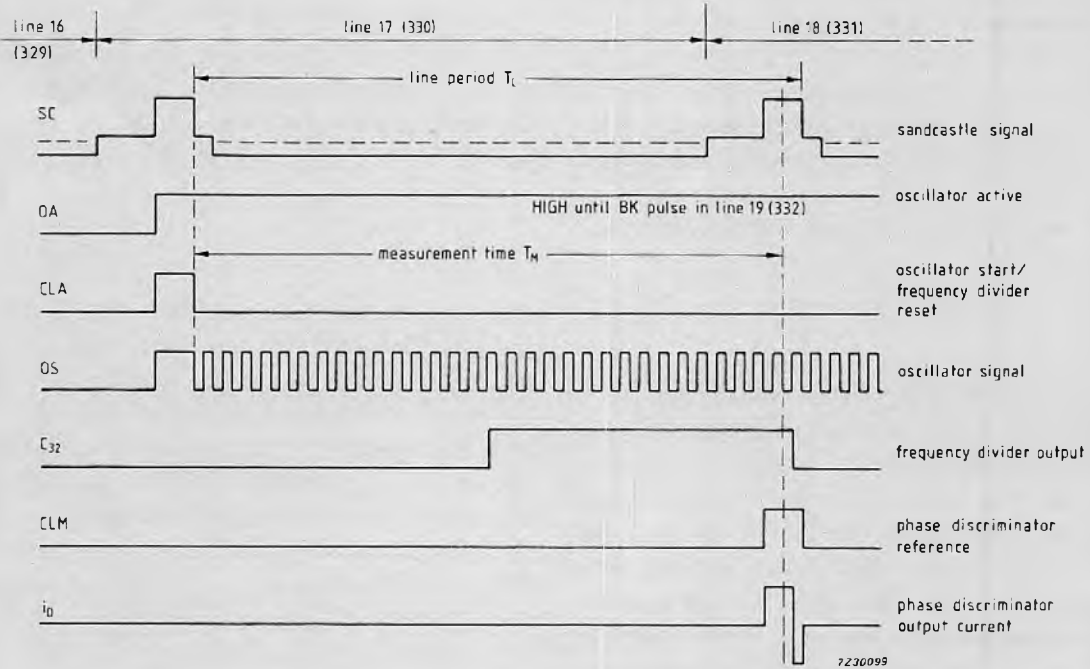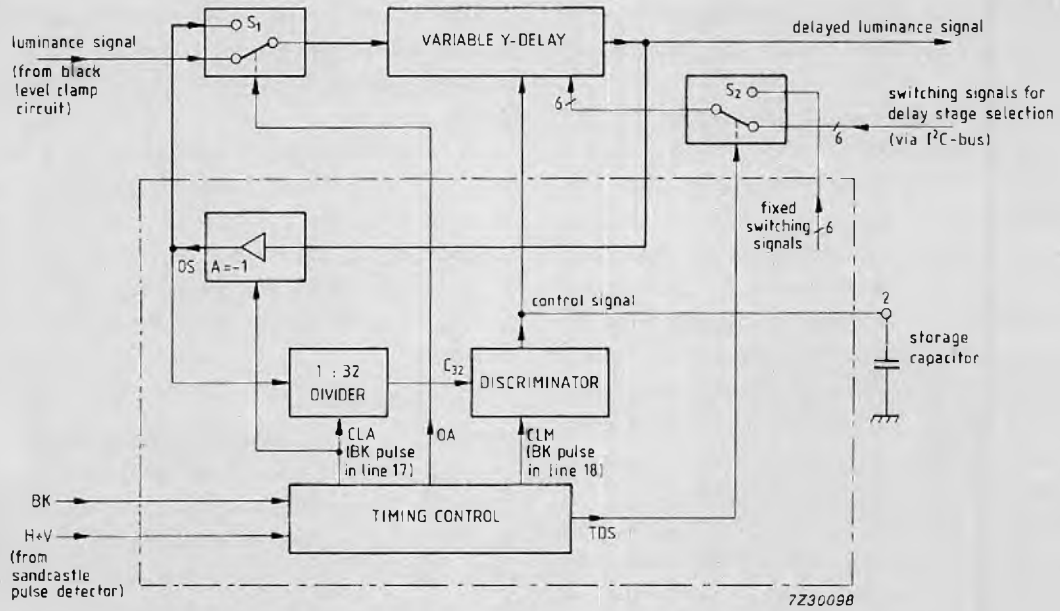
Fig.4 Automatic delay adjustment circuit and timing

Automatic adjustment begins in line 17 (330) when switch S_1 is switched by the leading edge of the burst key pulse (signal OA) to close the automatic adjustment control loop. Simultaneously, signal CLA (identical to the burst key pulses of lines 17 and 330) resets the frequency divider and sets the oscillator signal, OS, to a HIGH level. The latter is necessary to achieve the correct phase of the oscillator signal at the start of the measurement time. The oscillator signal starts to oscillate on the trailing edge of the CLA pulse and initiates the automatic adjustment.

The oscillator signal frequency is divided by 32 in the frequency divider. The phase of the frequency divider output C_{32} is compared in the phase discriminator with the reference signal CLM (CLM is identical to the burst key pulses of lines 18 and 331). The phase of the frequency divider output C_{32} relative to the middle of the reference signal CLM determines the polarity of the phase discriminator output current, i_D. When the trailing edge of C_{32} coincides with the middle of CLM ($T_M = 32T_O$) the mean value of the phase discriminator current is zero, otherwise i_D is positive or negative (a positive value is shown in Fig.4).

The phase discriminator current charges the external capacitor connected to pin 2. Its stored voltage is the control signal to adjust the DC currents of the transistors in the delay stages, which determine the resistor values for the correct RC time constants. Automatic adjustment adjusts the delay τ_D every consecutive field blanking interval, until the actual and nominal luminance signal delays are exactly equal. The trailing edge of the burst key pulse of line 19 (332) switches S_1 (via signal OA) to open-circuit the feedback loop, and switches S_2 (via signal TDS) to return delay stage selection to I²C-bus control.

Although during the automatic adjustment only six of the nine delay stages are set to their nominal RC time constants, the small relative tolerances of on-chip components ensures that the automatic adjustment is satisfactory for any other combination of delay stages selected via the I²C-bus. Only relatively small delay offset errors remain, but major externally-induced delay offsets caused by variations in temperature and supply voltage are compensated.

The NTSC-M transmission standard has a horizontal scan time of 63.5 μs which gives a nominal delay of ≈ 947 ns, for $\tau_{BK} = 4$ μs and $\tau_A = 13.75$ ns. In practice, this difference has little effect on the automatic adjustment procedure since it is relatively small. However, due to the different delay characteristics of the chrominance filter and chrominance trap for the NTSC-M transmission standard, different delay stages will be selected for the correct luminance signal delay during normal operation.

Aperture Correction Filter With Noise Correction

Aperture correction (peaking) in the TDA4670 increases the gradients of the luminance signal transients and increases the contrast by providing symmetrical overshoots at both extremes of the transients. The symmetrical overshoots are generated by a transversal filter using all-pass filter sections integrated on the chip, see Fig.5. Aperture correction, degree of peaking and the coring stage are all selected and controlled via the I²C-bus.

Symmetrical overshoots are obtained by the generation of a correction signal which is then added to the luminance signal transient. This correction signal (S_4) consists of three components: the inverted luminance signal halved in amplitude (S_1), the luminance signal delayed by τ (S_2), and the inverted, delayed (by 2τ) luminance signal halved in amplitude (S_3). The principle of aperture correction, using the correction signal to increase the gradient of the luminance signal and provide symmetrical overshoots is shown in Fig.6. The amplitude of the overshoots and the increase in the gradient are determined by the multiplication factor α applied to the correction signal S_4. The output luminance signal (S_5) is:

$$S_5 = S_2 + \alpha S_4 = S_2 + \alpha(S_1 + S_2 + S_3)$$

This equation is realized by a transversal filter using all-pass sections with delays of τ and 2τ to realize S_2 and S_3. If the luminance signal has a very gradual transient then S_1, S_2 and S_3 tend to coincide, so that S_4 is very small (and S_5 is practically S_0 delayed by τ). A delay of τ is equivalent to multiplication by $\exp(-j2\pi f\tau)$ in the time domain, so that by substitution in the equation $S_4 = S_1 + S_2 + S_3$, and applying the Euler transform:

$$|S_4/S_0| = 1 - \cos 2\pi f\tau$$

This is the transfer response of a bandpass filter with a maximum output at $f = 1/(2\tau)$. Low-frequency components are damped (until maximum damping at $f = 0$) and correction signal S_4 consists of the high-frequency components of the luminance signal.

The complete transfer function is:

$$A = \frac{S_5}{S_0} = \frac{(S_2 - \alpha S_4)}{S_0} = e^{-j2\pi f\tau} + \frac{\alpha S_4}{S_0}$$

which reduces to:

$$|A| = 1 + 2\alpha \sin^2(\pi f\tau).$$

This transfer function is shown in Fig.7 for values of α of −0.1, 0, +0.2 and +0.5. When α is positive, the maximum amplitude of the transfer function is $(1 + 2\alpha)$ at $f = 1/(2\tau)$. When α is negative, the minimum amplitude is <1 at $f = 1/(2\tau)$.
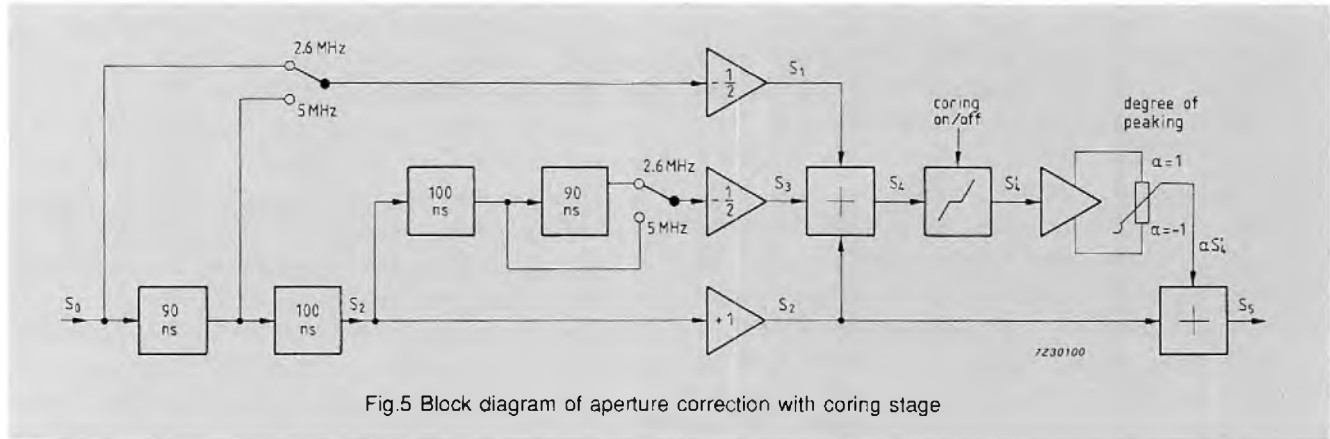
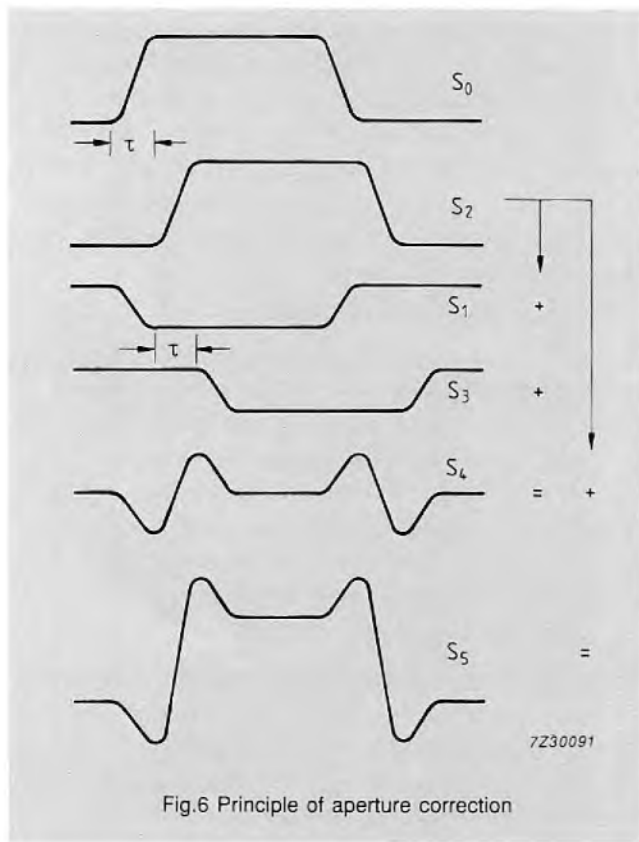Fig.5 Block diagram of aperture correction with coring stage

Fig.6 Principle of aperture correction

The latter results in a worsening of picture definition, but with a very noisy signal (snow on the picture) there is a noise reduction which actually improves picture quality. The filter dimensions are such that above the frequency $1/(2\tau)$ only luminance signal components exist which are small or insignificant, hence the dashed lines in Fig.7.

In Fig.5, S_1 and S_3 are halved in amplitude and inverted by operational amplifiers. Positive and negative values of the multiplying factor α are realized by the degree of peaking potentiometer. Two bits of I^2C-bus data select α to give degrees of peaking of -4, 0, $+3$ and $+6$ dB $(20\log(1 + 2\alpha))$.

To obtain symmetrical overshoots, a delay τ is required which approximately equals the minimum rise time of the luminance signal. Bandwidth and rise time are related by the equation, $\tau_r = 1/(2f_r)$. For a luminance signal bandwidth of 5 MHz, τ has to be 100 ns. Video recorders have a narrower bandwidth and therefore τ is 190 ns. In the first case, a positive value of α sets the maximum value of the transfer function to 5 MHz and in the second, to 2.63 MHz. τ is realized by double pairs of delay stages with delays of 90 and 100 ns. The I^2C-bus selects only two delay stages for a bandwidth of 5 MHz, $\tau = 100$ ns, or all the delay stages for a bandwidth of 2.63 MHz, $\tau = 190$ ns.
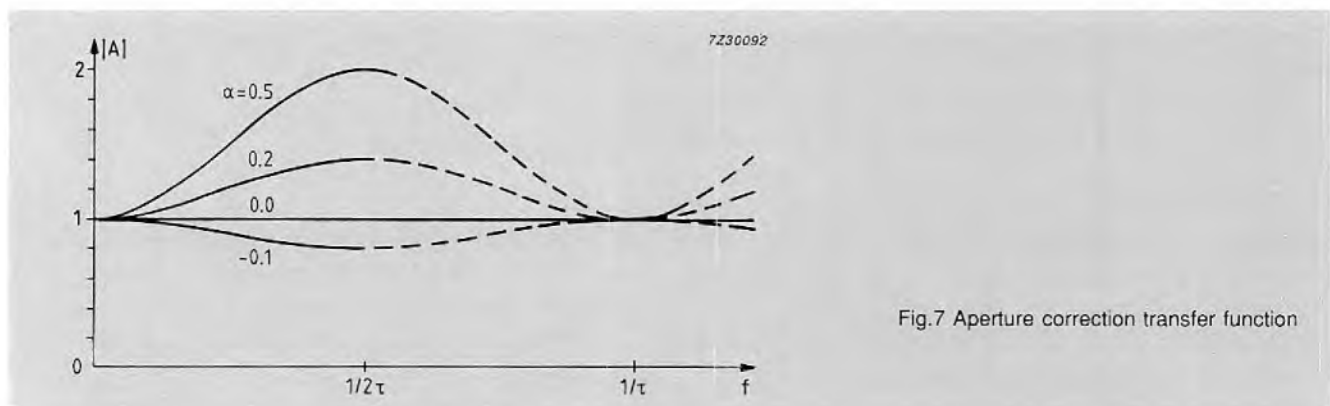
Fig.7 Aperture correction transfer function

Aperture correction increases the gradient of the luminance signal transients and provides symmetrical overshoots by increasing the high-frequency response up to $f = 1/(2\tau)$ using the correction signal. This increases the high-frequency noise levels, which are visible on the picture in large areas with little or no structure. These increased noise levels are caused by the correction signal S_4. To reduce these noise levels, a coring stage is positioned after the correction signal generation circuit, but before the degree of peaking potentiometer. When the coring stage is switched off $S_4' = S_4$. When it is switched on it has only a small effect on aperture correction at large signal levels.

The noise levels are considerably smaller than the correction signal as shown in Fig.8. The correction signal is shown without high-frequency noise in Fig.8(a) and with high-frequency noise in Fig.8(b). When the high-frequency noise content of signal S_4 is attenuated within the limits $\pm V_S$, the correction signal is as shown in Fig.8(c). The noise level of the output signal from the coring stage S_4' is completely attenuated, except during the rising and falling edges of the luminance signal transient, where its effect on the picture is reduced due the increased structure. The coring stage reduces only the high-frequency noise in the correction signal S_4 due to aperture correction, i.e. there is no noise reduction when $\alpha = 0$ (degree of peaking = 0 dB). When the degree of peaking is negative, noise reduction results from the addition of the inverted correction signal. Coring should not be applied in this case, as it removes the noise reduction effect of negative peaking.
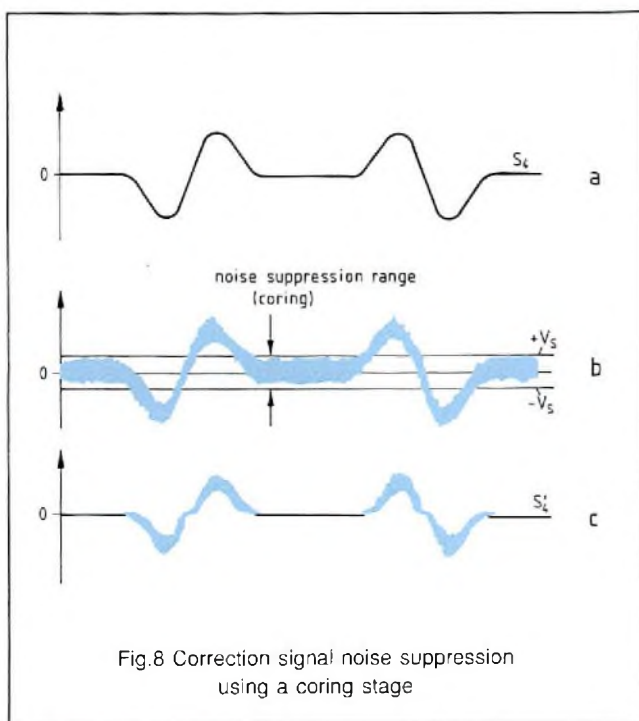
Fig.8 Correction signal noise suppression using a coring stage

The non-linear characteristic of the coring stage is shown in Fig.9. In the TDA4670 the noise suppression range is approximately 13% of the maximum luminance signal range, offset compensation ensures symmetry about the zero voltage level. The coring stage is selected via the I²C-bus.
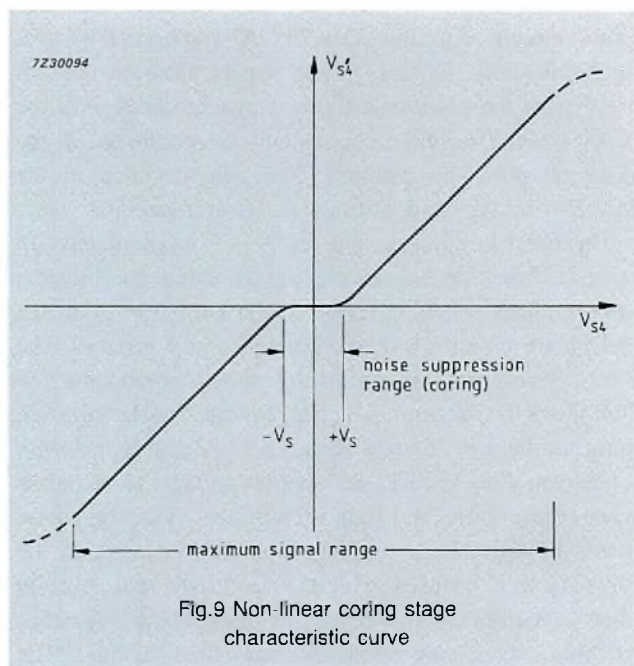
Fig.9 Non-linear coring stage characteristic curve

AUXILIARY CIRCUITS

The auxiliary circuits for Picture Signal Improvement in the TDA4670 are:

- reference supply voltage circuit
- sandcastle pulse detector circuits
- I²C-bus receiver

Reference Supply Voltage Circuit

Many circuits in the TDA4670 require reference voltages and currents which are independent of supply voltage fluctuations and temperature. A reference DC voltage, V_{Ref}, to supply these internal voltages and currents, is generated using electron band-gap energy levels. The external voltage on pin 1 supplies the V_{Ref} circuit, luminance processing circuits, sandcastle pulse detector and the I²C-bus receiver. V_{Ref} is de-coupled by the 100 nF capacitor on pin 15.

The colour-difference processing circuits are supplied by the external voltage on pin 5. Supply voltages on pins 1 and 5 must be between +5 and +8 V DC. In practice, both pins may be connected to the same supply voltage. Pins 8 and 18 must be connected to the same earth by minimum-length separate tracks.

Sandcastle Pulse Detector Circuits

Most of the circuits of the TDA4670 need to be synchronized to the input line and field frequencies. In particular, the black level clamp circuits require the burst key pulses, and the delay time control circuits require the H + V sync pulses. These pulses are derived from the external sandcastle pulses on pin 17 which are supplied by a synchronization circuit, e.g. the TDA2579A Horizontal/Vertical Synchronization Circuit. The synchronization circuit ensures that the sandcastle pulse is synchronized with the CVBS signal. The three components are combined in the sandcastle pulse by addition. They are decoded in the TDA4670 by the sandcastle pulse detector circuits.

The burst key pulses and the H + V components are extracted from the sandcastle pulses using comparators with reference switching levels. These are fed to the black level clamp circuits and delay time control circuits. The voltage levels of the sandcastle pulse components are determined by the supply voltage of the synchronization circuit. In the past this was always a 12 V supply, but with the tendency to reduce the supply voltage to decrease power consumption and reduce chip area, synchronization circuits now often use a 5 V supply. To ensure that the TDA4670 can be used with the sandcastle pulses from either synchronization circuit, the comparator reference switching levels are switched via the I²C-bus. The switching levels of the sandcastle pulse components are then defined for either a 5 or 12 V synchronization circuit supply voltage.

I²C-bus Receiver

Picture Signal Improvement operation in the TDA4670 is selected and controlled via its two-wire I²C-bus. This provides data (SDA) and clock (SCL) inputs to the integrated I²C-bus slave receiver where the serial data is converted into control signals for the different functions of the TDA4670. Each data transmission consists of three bytes. The module or slave address of the TDA4670 (bits A_6 to A_0) is 1000100_2. The first byte consists of the module address followed by the read/write bit (always = 0 for data receive), so that the first byte is 88_{Hex} = 10001000_2. The second byte is the sub-address of the function to be addressed, and the third byte is the data of the addressed data or parameter (see Ref.2). Sub-address 10_{Hex} = 00010000_2 selects the comparator switching levels in the sandcastle pulse detector, switches CTI on/off and selects the luminance signal delay. Sub-address 11_{Hex} = 00010001_2 selects aperture correction, degree of peaking and the coring stage.

APPLICATION

The external components for the TDA4670 are the storage and coupling capacitors, their values are not critical, see Fig.10. Supply voltages at pins 1 and 5 are normally connected together and de-coupled by a 15 Ω resistor and a 47 µF capacitor. The Y, −(R − Y) and −(B − Y) input signal currents are 0.1 µA, maximum, when black level clamping is not selected and 190 µA, maximum, during black level clamping. The sandcastle pulse on pin 17 can be either a 2 or 3-level pulse supplied from a synchronization circuit with a 5 or 12 V supply voltage.
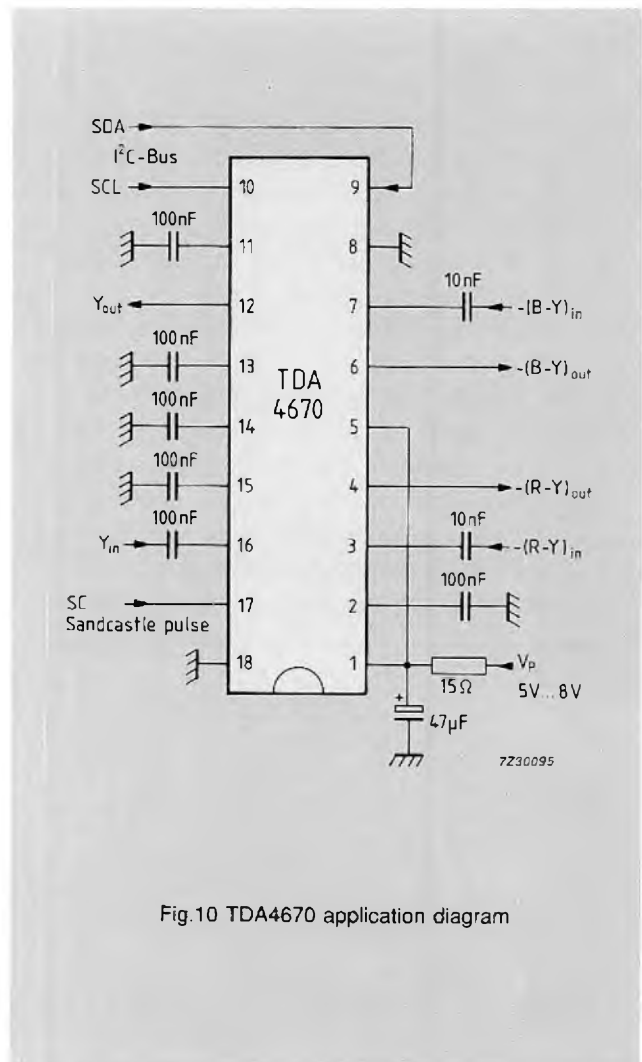

Fig.10 TDA4670 application diagram

The delayed, aperture-corrected, luminance signal and the transient-improved colour-difference signals are fed out of the TDA4670 with nominal gains of unity. The output resistance of the luminance signal output (pin 12) is 160 Ω, maximum, and the output resistances of the colour-difference signal outputs (pins 4 and 6) are 100 Ω, maximum. All three outputs supply a current of 1 mA, maximum, or can sink a current of at least 0.4 mA.

Two important functions of the TDA4670, colour transient improvement and aperture correction, are shown in Figs 11, 12 and 13. The oscilloscope traces in Fig.11 show the input and output $-(R - Y)$ colour-difference signals for input signal rise and fall times of 900 ns. With CTI switched on, the rise and fall times are reduced to less than 150 ns, roughly equivalent to the minimum luminance signal transient time.

Figures 12 and 13 show the effect of the aperture correction (peaking) on the luminance signal. Figure 12 shows aperture correction when the maximum value of the transfer function is at 5 MHz (τ = 100 ns), and Fig.13 shows aperture correction with a maximum value at 2.6 MHz (τ = 190 ns). In both cases the degree of peaking is +6 dB.

7Z30102
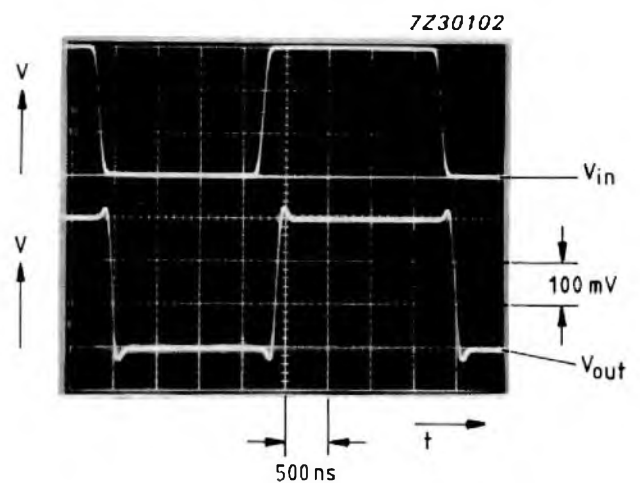
Fig.12 Aperture correction with τ = 100 ns (5 MHz). A degree of peaking of +6 dB is applied to the luminance signal; the luminance signal input on pin 16 is band-limited to about 5 MHz (upper trace), the maximum in the frequency response of the transversal filter at 5 MHz (τ = 100 ns) provides the peaked luminance signal output on pin 12 (lower trace). The luminance signal output is delayed by about 200 ns.

7Z30101
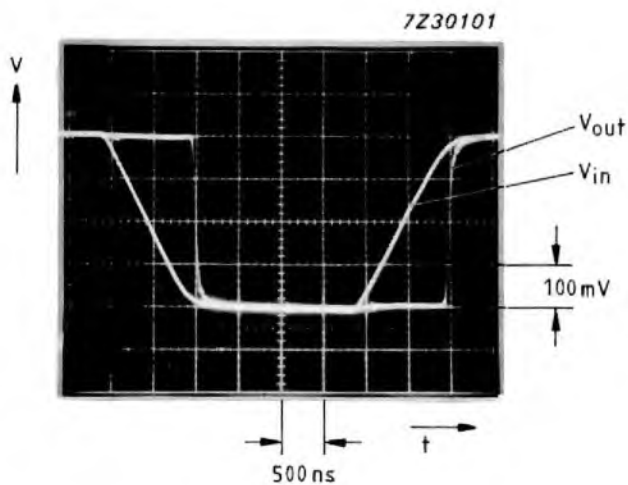
Fig.11 CTI operation. Trapezoidal-shaped (R − Y) colour-difference input signal on pin 3 with rise and fall times of about 900 ns, and the (R − Y) colour difference output signal on pin 4 with rise and fall times of <150 ns.

7Z30103
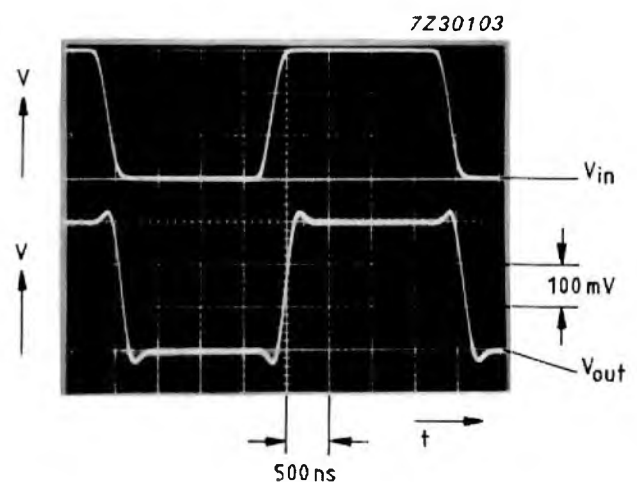
Fig.13 Aperture correction with τ = 190 ns (2.6 MHz). As in Fig.12, but with a luminance signal input band-limited to approx. 2.5 MHz, the maximum in the frequency response of the transversal filter is at 2.6 MHz (τ = 190 ns).

REFERENCES

1. H. Harlos: 'Picture Signal Improvement in Colour TV Receivers', IEEE Transactions on Consumer Electronics, Vol. CE-31, No.3, August 1985.

2. Philips' publication, 'The I²C-bus specification', Jan. 1989, ordering code 9398 358 10011.

3. 'Analog multi-standard colour decoder ICs TDA4650 and TDA4660', Feb. 1990, ordering code 9398 071 60011.

Colour monitor tubes with magnetic-field suppression and antistatic coating

AD VAN DEN EEDEN AND SEYNO SLUYTERMAN

Philips Components' range of colour monitor tubes are now available with several options – VLMF (Very-Low-frequency Magnetic Field) suppression to allow monitor manufacturers to meet the latest Nordic requirements, and anti-glare/antistatic coatings for greater operator comfort.

The proliferation in the use of computer terminals and stand-alone PCs has led to some major changes in working practices. This is especially true of office and industrial-control environments in which many individuals are now expected to spend hours of their working day in close proximity to computer monitors. Naturally the well-being of these individuals is important to computer manufacturers and though there has never been any evidence of adverse effects from computer monitors, several computer manufacturers are now actively engaged in setting up stringent specifications to guarantee the safety of their equipment.

Two areas of recent interest are in the suppression of very low-frequency magnetic fields emanating from the monitor-tube deflection coils and of electrostatic-potential build-up on the monitor screen. These areas were first studied by the Swedish Department of Labour in response to mild concern expressed by some employee organizations over the possible harmful effects of working for long periods close to computer monitors. Though their studies could find no foundation for this concern, on the sound principle of "better safe than sorry", they introduced

statutory requirements with regard to VLMF and electro-static build-up for all computer monitors manufactured in or imported into Sweden. These requirement have since been taken up by all Nordic countries, and are also likely to become mandatory in several other European countries.

The options now available to our colour monitor tubes easily ensure that computer and monitor manufacturers will be able to comply with these Nordic requirements.

VLMF SUPPRESSION

The deflection yoke of a monitor tube generates a *dipole* magnetic field that decreases very rapidly with distance in front of the screen (a dipole field, in fact, falls of as the cube of the distance from the radiating centre of the deflection coil). A standard deflection yoke generates a rather low magnetic field of around 5×10^{-7} mT (around 1% of the Earth's field) 50 cm in front of the screen. However, with the high line frequencies and short flyback times of modern monitors, not only the magnetic field but also the flux density $(\partial B / \partial t)$ has been a subject of interest, since apart from the safety aspect, variations in the field can cause interference with other electronic equipment. The Nordic authorities have therefore studied the flux density and set limits on its maximum values (see later for details of these).

Yoke modification for multipole suppression

Figure 1 shows the operating principle of our new yoke assembly and Fig.2 shows details of the compensating coils.
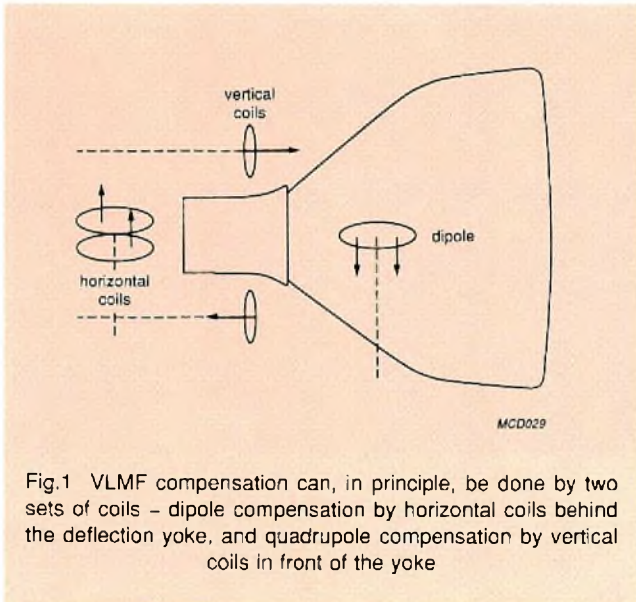

Fig.1 VLMF compensation can, in principle, be done by two sets of coils – dipole compensation by horizontal coils behind the deflection yoke, and quadrupole compensation by vertical coils in front of the yoke
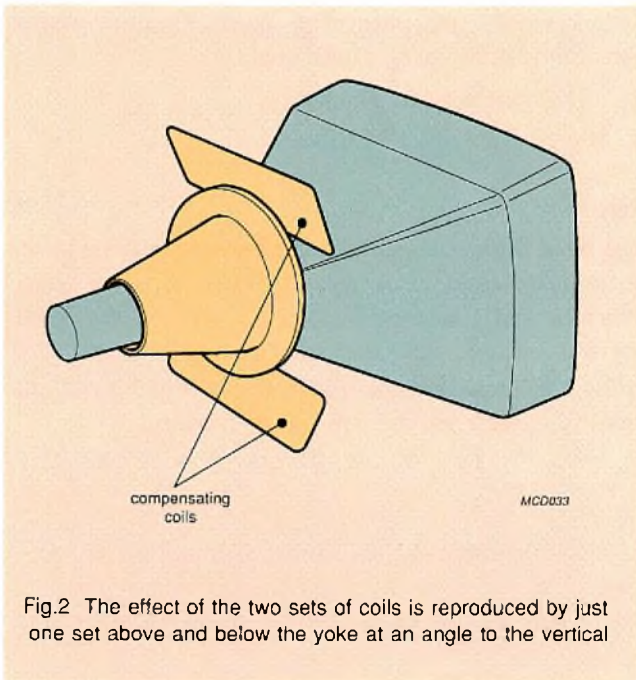

Fig.2 The effect of the two sets of coils is reproduced by just one set above and below the yoke at an angle to the vertical

In principle, the field can be compensated by two sets of coils (Fig.1): horizontal coils behind the deflection yoke, above and below its axis, and vertical coils at the front of the yoke (Ref.1). The horizontal coils would compensate the dipole magnetic field generated by the yoke but because they are displaced from this dipole, a residual

quadrupole field remains. Since this falls off as the fourth power of the distance, for larger distances it can be neglected. But for shorter distances (encountered with computer monitors), further compensation is needed and this can be provided by the vertical coils. The remaining field after compensation by the vertical coils consists of octupole (8-pole) and higher multipole components which fall of very rapidly with distance and hence are negligible at the distances encountered with computer monitors.

In practice, the effects of the two sets of coils can be reproduced almost exactly by just a single set mounted above and below the yoke at a slight angle to the vertical (Fig.2). The compensating field produced by this set coincides very closely with the resultant field produced by the vertical and horizontal coils. There is, however, a residual hexapole (6-pole) field with this arrangement, but since this decreases as the fifth power of the distance, its effect here is negligible.

Figure 3 is a photograph of the new yoke. The compensation coils can be seen supported on formers at the front of the yoke assembly.
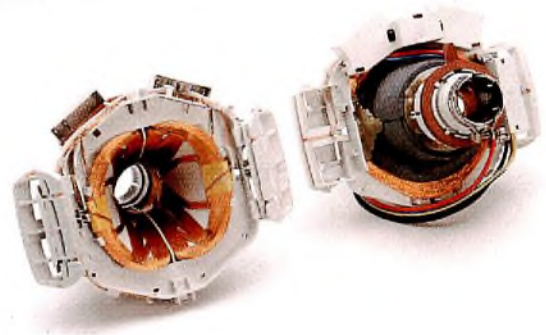
Fig.3 New deflection yoke with compensation coils

VLMF measurement and results

Measuring setup

The measuring setup we've adopted is based closely on that proposed by the Swedish authorities (Ref.2).

Measurements are made using a Combinova MFM 1000 magnetic-field meter (Ref.3) with an antenna comprising three mutually perpendicular coils. The antenna can be mounted on any one of seven fixtures (Figs 4 and 5), five of which (numbered 1 to 5 in Fig.4) are located on the surface of a sphere 0.65 m in radius centred 15 cm orthogonally behind the centre point of the display screen. The other two fixtures (numbered 6 and 7) are located on the screen axis at distances of 0.45 and 0.85 m from the centre of the sphere.
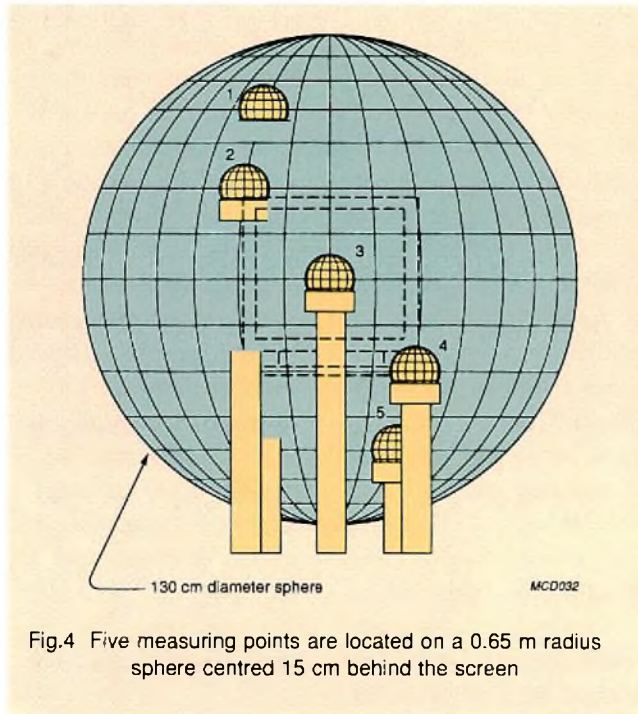
Fig.4 Five measuring points are located on a 0.65 m radius sphere centred 15 cm behind the screen
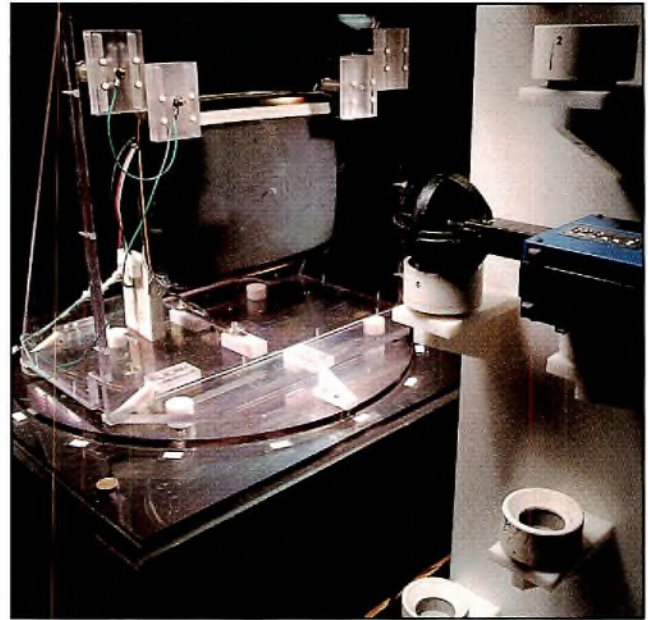

Fig.6 Measuring apparatus and fixtures for locating the antenna

measuring position	Y, Z coordinates (mm)	
1	460,	460
2	250,	600
3	0,	650
4	−250,	600
5	−460,	460
6	0,	450
7	0,	850
screen centre	0,	150

Fig.5 Positions (Y,Z coordinates) for VLMF measurements

In addition to the seven measurements mentioned above, measurements 1 to 5 are repeated as the display is rotated around its axis in increments of 22½° − making a total of 82 measurements in all.

A photograph of the measuring apparatus is shown in Fig.6.

Requirements

To meet the requirements set down by the Swedish authorities, at all indicated positions:

- $\partial B/\partial t$ must not exceed 15 mT/s
- B must not exceed 60 nT.

Results

The table below summarizes the results of measurements on 14-inch monitor tubes (type M34ECL15....). Experience indicates that positions 6 with the tube in the home position and 4 with the tube rotated through 225° (10 × 22½) encounter the highest magnetic fields and flux density, so these are the only values reported.

TABLE 1
Worst case measurements of B and $\partial B/\partial t$

	max	mean	lim	units
Peak magnetic field B				
Pos 4	12.0	7.8	60	nT
Pos 6	21.0	18.3		
Flux density $\partial B/\partial t$				
Pos 4	9.0	6.4	15	mT/s
Pos 6	12.0	10.0		

From these results it's clear that the performance of our colour monitor tubes with VLMF suppression falls well within Nordic requirements.

ANTI-GLARE ANTISTATIC (AGAS) SCREENS

The advantages of anti-glare monitor screens are rather obvious: easier working in bright surroundings, better visibility and hence less operator eye-strain. The advantages of antistatic coatings are somewhat less obvious but are primarily directed towards reduced deposits of dust (and other aerosol materials) on the screen and less chance of electrostatic discharge effects (such as the tingling sensation that comes when a hand approaches the screen).

Our current generation of monitor tubes can be provided with a single anti-glare coating whose performance compares favourably with direct-etch tubes, or with a combined antistatic/anti-glare coating.

Two-step process

Table 2 illustrates the current two-step antistatic (AS) anti-glare (AG) process used on our monitor tubes.

TABLE 2
Two-step AGAS process

	antistatic	anti-glare
technique	spinning	spraying
material	Sb_2O_3	TEOS*
process	in-line	in-line

* TEOS (tetra ethyl ortho silicate) is used for applying a hard strongly adhesive SiO_2 coating

The antistatic layer (deposited by spinning) is impregnated with minute conductive particles to allow continuous discharge of the monitor screen during operation. Note: if only anti-glare properties are required, this first process can be omitted.

Table 3 summarizes the antistatic properties of our AGAS monitor tubes.

TABLE 3
Antistatic properties of AGAS tube

	standard (no AS)	antistatic
surface resistance	10^{13} $\Omega/\square$	$= 10^9$ $\Omega/\square$
discharge time (voltage from 25 kV to 3 kV)	>10 min	<60 s

To comply with Nordic requirements, the surface resistance should lie between 10^3 and 10^{10} $\Omega/\square$, and from the table it can be seen that our AGAS tubes do indeed fall within these limits.

Finally, Fig.7 compares the reflectivity of our anti-glare coating with that of a direct-etch tube, a comparison that's clearly illustrated by the photographs in Fig.8.
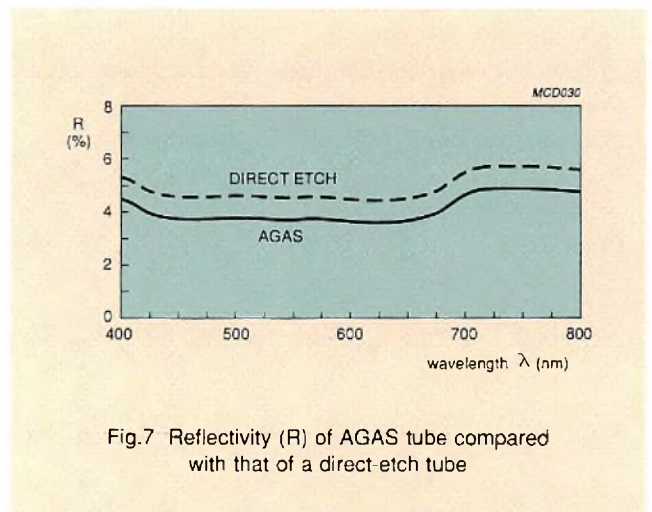
Fig.7 Reflectivity (R) of AGAS tube compared with that of a direct-etch tube
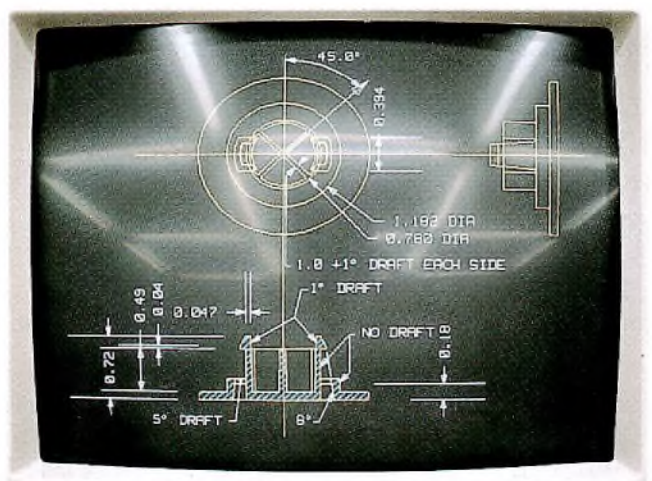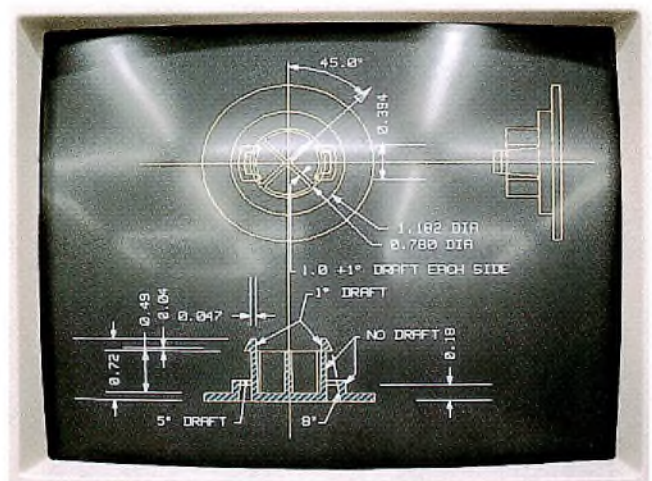
Fig.8 Subjective effect of the improvement in reflectivity of AGAS tube over a direct-etch tube (AGAS tube top)

REFERENCES

1. Sluyterman A.A.S.; "The radiating fields of magnetic deflection systems and their compensation"; Proceedings of the Society for Information Display, Vol. 29, No. 3; 1988.
2. "Testing Visual Display Units – Test Methods", National Council for Metrology and Testing, Sweden.
3. Combinova, Box 20050, 161 20 Bromma, Sweden.

Introducing the Philips SensorFET

JULIAN HUMPHREYS

The increasing popularity of current-mode control in switched-mode power supply and motor drive applications has led to widespread use of current sensing techniques in power-conditioning circuits. Such techniques have traditionally involved either a series resistor or current transformer to monitor the instantaneous current in the switching device. Both techniques present serious disadvantages to the designer. Insertion of a series resistor results in power loss to the circuit which must be dissipated by the resistor. A high-power, low-resistance, non-inductive component is thus generally required which can add appreciable cost to the system. The alternative method of using a current transformer can also be costly and is usually inconvenient.

The Philips SensorFET is a Power MOSFET which divides load current into power and sense components. The sense current can then be monitored with a cheap signal-level resistor, thus avoiding power loss and presenting circuit designers with a simple and efficient means of current sampling.

SENSORFET CONSTRUCTION

A PowerMOS transistor is essentially an IC comprising many thousands of small individual transistors connected in parallel. Each of the transistor elements within the device is identical and current distributes equally between their equal on-resistances. It's possible to isolate the source connections to several cells from those of all the other cells and bring them out to a separate bond pad. The PowerMOS is then effectively two transistors: a low $R_{DS(ON)}$ power transistor and a high $R_{DS(ON)}$ sense transistor. Current will share between the two parts according to the ratio of their on-resistances. This is the principle of operation of the Philips SensorFET.

The relative sizes of the two FETs are determined by the ratio of the number of sense cells to power cells which is about 1:1500. This ratio primarily determines current

distribution between the sense and power cell areas, and is given by the drain-to-measure current ratio (sense ratio), I_D/I_M. The sense ratio is defined for the condition where the measure and source terminals are held at the same potential ($V_{MK} = 0$ V). Since this ratio is about 1500:1, the drain current and the current in the source power lead may be considered the same.

The SensorFET is assembled in a standard 5-pin TO-220 plastic encapsulated package; the two extra pins being the measure terminal and kelvin-source connection. Figure 1 shows the symbol for a SensorFET. Its equivalent circuit is shown in Fig.2, illustrating two parallel FETs with separate source connections but common gate and drain connections. The separate source connection is termed the measure terminal.
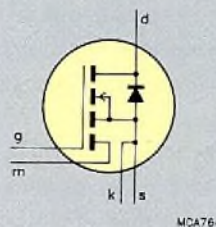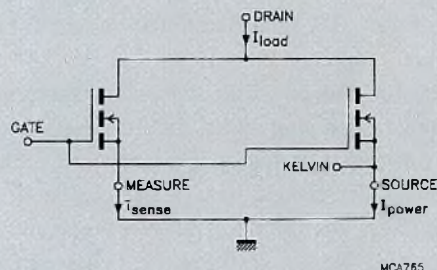

Fig.1 SensorFET symbol

Fig.2 SensorFET equivalent circuit

SENSORFET OPERATION

Current sensing is achieved with the insertion of a signal-level resistor between the measure and kelvin-source terminals, avoiding the necessity for a measure resistor in the power circuit. The calculation of load current is straightforward provided certain design rules are adhered to. The derivation of these rules is easily understood when considering the on-state model of the SensorFET.

Figure 3 shows the on-state model of the SensorFET separated into its resistive components: a bulk-drain resistance R_B (common to both parts), and two active resistances $R_{DM(ON)}$ (drain-to-measure on-state resistance) and $R_{A(ON)}$ (resistance of the power part). R_{sense} represents the external sense resistor. Using this model, sense voltage may be expressed as:

$$V_{sense} = R_{sense} \times \frac{I_D \times R_{A(ON)}}{(R_{DM(ON)} + R_{sense})} \qquad (1)$$

Equation 1 may be rearranged to give expressions for R_{sense} and I_D.

$$R_{sense} = \frac{V_{sense} \times R_{DM(ON)}}{\{(I_D \times R_{DM(ON)}) - V_{sense}\}} \qquad (2)$$

$$I_D = V_{sense} \times \frac{(R_{sense} + R_{DM(ON)})}{(R_{A(ON)} \times R_{sense})} \qquad (3)$$

In Eq.1, if R_{sense} is much larger than $R_{DM(ON)}$, then $V_{sense} \approx I_D \times R_{A(ON)}$. This value is clearly the maximum sense voltage that can be obtained and as such represents the compliance of the measure terminal. A value of $R_{A(ON)}$ may be determined from the potential between the measure and kelvin terminals with the measure terminal open-circuit, $R_{A(ON)} = V_{sense}/I_D$. A value of $R_{DM(ON)}$ can be gained from $R_{DM(ON)} = R_{A(ON)} \times n$, where n is the sense ratio. Since R_B will be very small compared to $R_{DM(ON)}$, the latter may also be measured directly from the drain-to-measure on-state resistance. Typical values for SensorFET BUK795-60A (60 V, 36 A) are: $R_{A(ON)} = 21$ mΩ, $R_B = 24$ mΩ and $R_{DM(ON)} = 35$ Ω with $n = 1645$.

To maintain accuracy it's important that the sense voltage be measured with respect to the kelvin terminal as depicted in Fig.3. To understand the necessity for the kelvin terminal, consider the situation if the low side of the sense resistor and power source were connected to a common ground. The equivalent circuit would then be as shown in Fig.4 with the additional resistance R_G representing wire resistance, ground-loop resistance, and contact resistance in the power circuit. This resistance adds to the active component $R_{A(ON)}$, making Eq.1 inaccurate. The kelvin-source terminal which connects directly to the source metallization, allows R_G to be by-passed, essential for the correct application of Eqs 1 to 3.
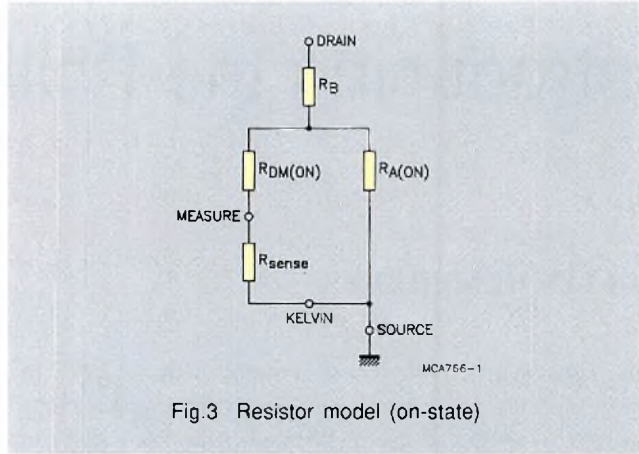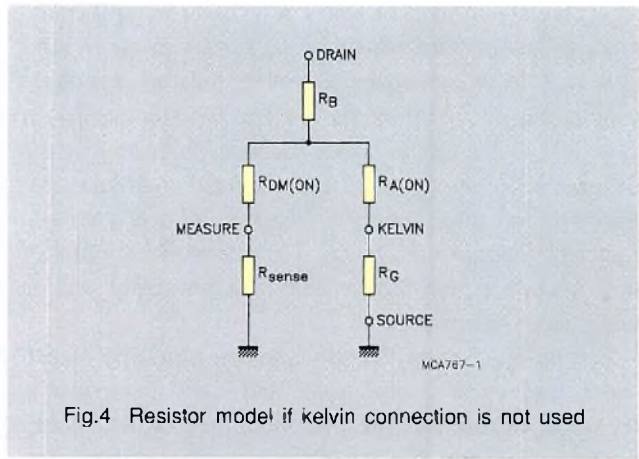

Fig.3 Resistor model (on-state)

Fig.4 Resistor model if kelvin connection is not used

PROPERTIES OF THE SENSE RATIO

Some of the properties of the ratio I_D/I_M when $V_{MK} = 0$ V are now considered.

Examples of sense ratio as a function of drain current, gate-source voltage, and junction temperature are given in Figs 5 to 7. You can see that sense ratio is essentially independent of current and junction temperature. In the latter case there is less than a 2% change in sense ratio between 25° C and 175 °C. Figure 6 shows logic level and standard SensorFET types; you can see that the sense ratio increases slightly as gate-source voltage is reduced.

Sense ratio as a function of temperature and gate voltage are device characteristics specified with the SensorFET data.
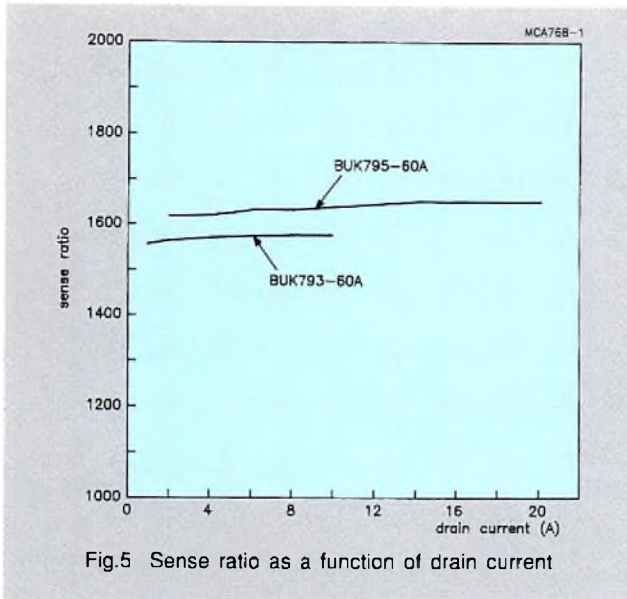
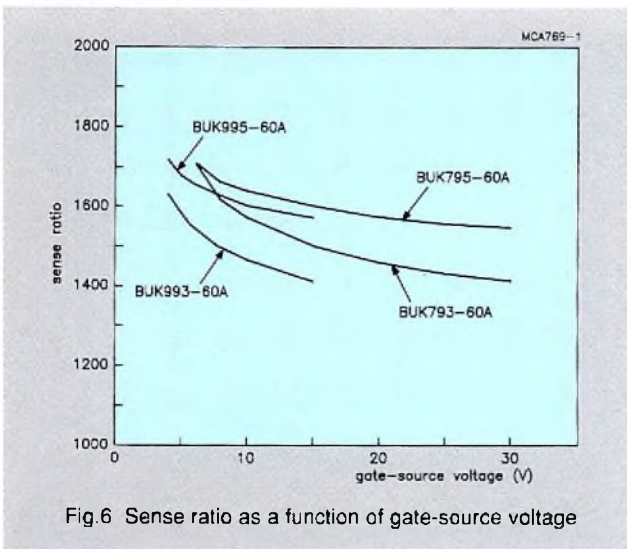Fig.5 Sense ratio as a function of drain current

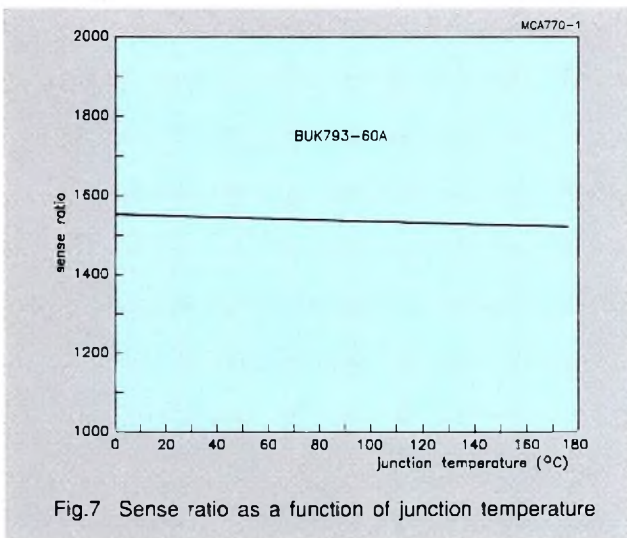Fig.6 Sense ratio as a function of gate-source voltage

Fig.7 Sense ratio as a function of junction temperature

CURRENT SENSING

Figure 8 shows a typical SensorFET application. A resistor connected between the measure and kelvin terminals converts sense current into a sense voltage which is then fed into a comparator for short-circuit detection. The effectiveness of this type of circuit, and others using resistive current sensing, clearly depends on the accuracy with which the load current may be predicted from the sense voltage.

Fig.8 A typical SensorFET application
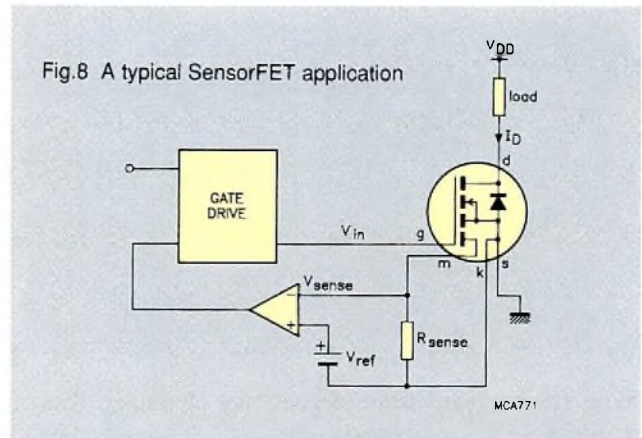
Equation 3 may be rearranged to express the effective sense ratio n'.

$$n' = n \times \left[1 + \frac{R_{sense}}{R_{DM(ON)}} \right] \tag{4}$$

Equation 4 demonstrates an important point: the effective sense ratio is a function of the ratio of sense resistor to drain-measure resistance.

The on-resistance of a Power MOSFET is a function of junction temperature and approximately doubles between 25 °C and 150 °C. The value of $R_{DM(ON)}$ is therefore temperature sensitive as described in Eq.5

$$R_{DM(ON)}[T] = R_{DM(ON)}[25 \, °C] \times \exp^{k(T-25)} \tag{5}$$

where $k = \left[\frac{1}{125} \right] \times \ln \left[\frac{R_{DM(ON)}[150 \, °C]}{R_{DM(ON)}[25 \, °C]} \right]$

Inclusion of the temperature sensitive expression for $R_{DM(ON)}$ in Eq.4 yields n' as a function of sense resistance and junction temperature.

Plotting this expression, Fig.9 demonstrates how the sense ratio becomes increasingly temperature dependent as the value of R_{sense} becomes comparable to, and greater than, $R_{DM(ON)}(25 \, °C)$. Modifying Eq.1 to include temperature variation results in:

$$V_{sense}[T] = \frac{I_D \times R_{sense}}{n \times \left[1 + \frac{R_{sense}}{R_{DM(ON)}[25 \, °C] \times \exp^{k(T-25)}} \right]} \tag{6}$$
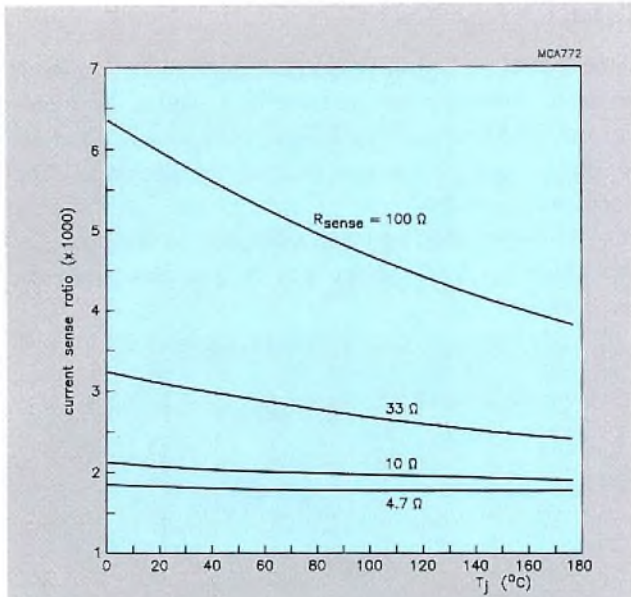
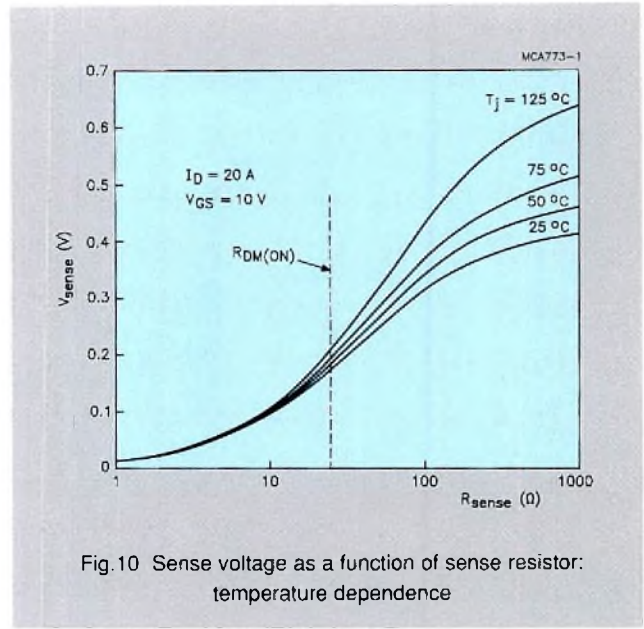Fig.9 Sense ratio as a function of temperature for the BUK795-60A at $R_{DM(ON)}$ = 35 Ω

The increasing temperature dependency of sense voltages for values of R_{sense} greater than $R_{DM(ON)}$ is shown clearly in Fig.10.

Figures 11(a) and (b) show a comparison between measured and calculated values of V_{sense} as a function of drain current. Results for the BUK795-60A and BUK793-60A are given for several values of R_{sense} at T_j = 25 °C and 125 °C. Equation 6 is seen to accurately predict sense voltages for values of R_{sense} less than or comparable to $R_{DM(ON)}$. Above this value some discrepancy is observed when sensing at high currents. This is explained by the effects of internal heating and difference in power dissipation for the sense cells compared with the power cells. Once R_{sense} starts to exceed $R_{DM(ON)}$, current flowing in the sense cells is significantly reduced compared with that in the power cells and hence the degree of internal heating in the power and sense parts differs. The ratio of power and sense resistances falls slightly and sense current rises.

As well as the variation with temperature, device-to-device spreads in $R_{DM(ON)}$ and I_D/I_M (V_{MK} = 0 V) must also be considered in relation to the effect on sensing accuracy. Table 1 shows the sensing parameters for the BUK795-60A.

TABLE 1
Sensing parameters for the BUK795-60A

	min.	typ.	max.
$R_{DM(ON)}$ Ω	–	35	50
I_D/I_M	1560	1645	1730

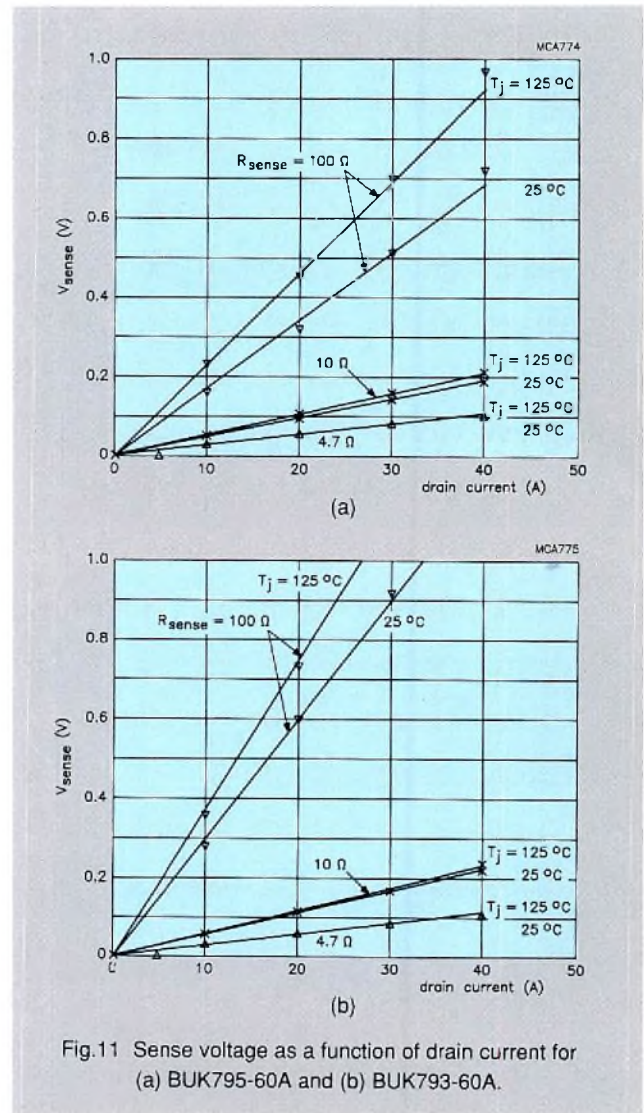Fig.10 Sense voltage as a function of sense resistor: temperature dependence

(a)

(b)

Fig.11 Sense voltage as a function of drain current for (a) BUK795-60A and (b) BUK793-60A.

Sense voltage as a function of R_{sense} for typical and limit devices is shown in Fig.12. Sense resistor values less than $R_{DM(ON)}$ generate sense voltages insensitive to any spread in parameters. For R_{sense} greater than $R_{DM(ON)}$, sense voltage becomes increasingly susceptible to device variation. The above results demonstrate how good accuracy is achieved for resistive current sensing when a sense resistor less than the drain-to-measure on-resistance is chosen. For the majority of applications such a constraint is not a problem. There may, however, be some circumstances when current sensing at low currents requires a larger sense voltage than can be generated by a resistor of the above magnitude. In such cases it may be necessary to use the virtual-earth current-sensing method.
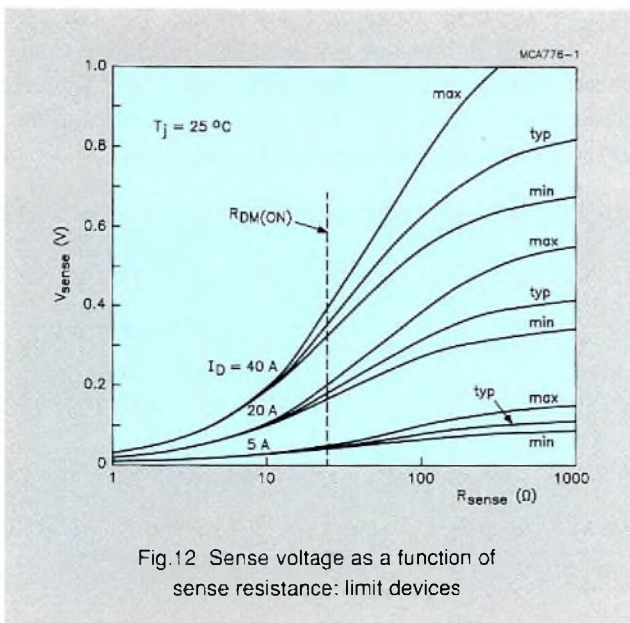
Fig.12 Sense voltage as a function of sense resistance: limit devices

Figure 13 shows the circuit for virtual-earth current sensing. The equation describing sense voltage is now:

$$V_{sense} = \frac{I_D \times R_{sense}}{n} \qquad (7)$$
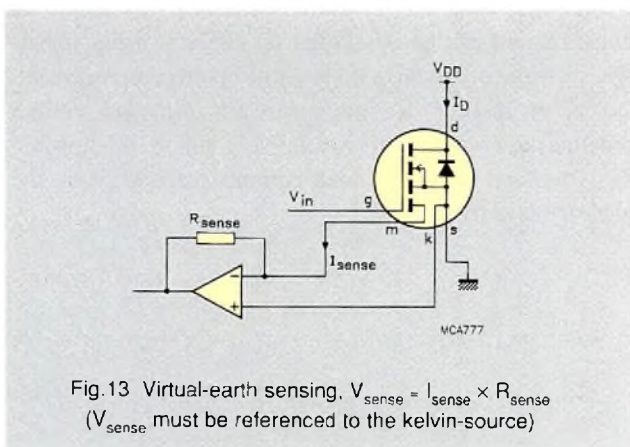
Fig.13 Virtual-earth sensing, $V_{sense} = I_{sense} \times R_{sense}$
(V_{sense} must be referenced to the kelvin-source)

A major advantage of the virtual-earth method is that the sense ratio becomes independent of the sense resistance and junction temperature. The ratio is equal to the data sheet value. The primary constraint of the virtual-earth circuit is the need for the op-amp to sink the sense current. Attention to this point is only required if you're using virtual-earth sensing at high currents.

NOISE SUPPRESSION

During switching intervals, the sense current is not well defined and can appear noisy. Current spikes are evident which originate from the charging of the gate-source capacitance and circuit stray capacitance and inductance. To avoid false information feeding through from the current sense, a simple RC filter can be used to remove turn-on transients.

SPECIAL OPERATION MODES

Diode conduction

The sense and power parts of the SensorFET are structurally identical: they both have a built-in anti-parallel diode. Certain applications, such as AC motor control, use this diode as an integral part of the circuit operation (see Fig.14). During the conduction cycle of the SensorFET's internal diode, reverse sense current will flow. If a virtual-earth sense circuit is being used, then the sense voltage is a true reflection of load current. Diode conduction is, however, bipolar and as such the on-resistance is modulated by the current flow. Consequently, the presence of a sense resistor between the measure and kelvin terminals has a direct influence on the value of $R_{DM(ON)}$ and hence the sense ratio. Current sensing during the diode's conducting cycle is thus inaccurate using the resistive method.

Recovery current overshoot

MOSFETs in bridge circuits can experience high current overshoot at turn-on owing to the recovery current of the flywheel diode in the opposing leg. Consider the circuit of Fig.14 as an example, starting with current flow in the flywheel diode of the upper leg. When the MOSFET in the lower leg is switched on, a large current overshoot gives rise to a high peak sense voltage. The size of this overshoot is a function of the original current in the diode and the turn-on speed of the SensorFET. The sense voltage will therefore pass through a peak at turn-on which may be more than double the on-state level. Again low-pass filtering should be used to avoid any false triggering of over-current protection circuitry.
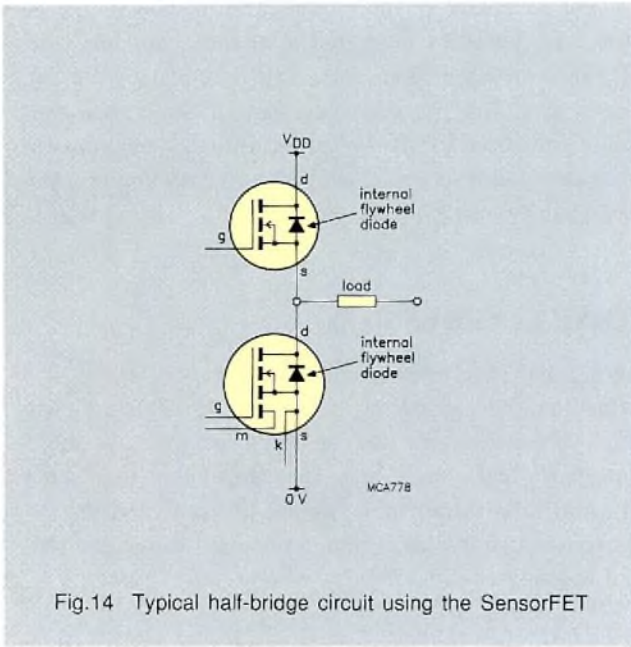
Fig.14 Typical half-bridge circuit using the SensorFET

Avalanche operation

The ability of a SensorFET to dissipate energy while operating in its avalanche mode, is independent of the sense circuitry between the measure and kelvin terminals. The SensorFET is, however, unable to provide accurate current sensing during a period of avalanche operation since it's operating outside its linear mode and hence the on-state model of Fig.3 is not applicable. Consequently the sense voltage during the inductive turn-off period is not representative of the avalanche current flowing in the device.

High-speed switching

The kelvin-source connection provides for very fast switching. Theoretically, the switching speed of a MOS-FET is limited only by the ability of the drive circuit to charge and discharge the gate capacitance. In practice for a standard 3-terminal MOSFET, the switching transitions represent a large di/dt which reacts with the finite inductance of the source bonding wire and source lead. This gives rise to a potential difference between the source metallization and external source terminal. This voltage adds to or, depending on the sign of di/dt, subtracts from the applied gate drive to oppose the switching transition.

The SensorFET enables gate drive to be referenced directly to the source metallization, by-passing the inductances of the power source connection. Very fast switching speeds are thus possible.

COMPATIBLE ICs

As a general rule, current-limiting comparators and operational amplifiers require a 100 to 200 mV sensitivity for SensorFET compatibility. We have recently developed two suitable ICs for use with the SensorFET: the AU2903 dual low-power voltage comparator, and the AU2904 dual low-power operational amplifier. Both these ICs can operate from a single power supply and have an input common-mode voltage range which includes ground. You can find more detailed information on these ICs in Philips Components 'Linear Products' Data Handbook IC11. Table 2 shows several suitable driver/control ICs available on the market that comply with SensorFET requirements.

TABLE 2
Compatible driver control ICs

device	description	application
MC33152	SensorFet driver	microprocessor interface
MC33034	motor controller	brushless DC motors
MC34129	current-mode controller	push-pull SMPS

All these devices function comfortably with output voltages that SensorFETs provide.

CONCLUSION

The SensorFET offers a simple and cost effective method for current sampling in power circuits. Instantaneous device current can be monitored by either a cheap signal-level resistor, or by the virtual-earth op-amp arrangement. Choice of resistor is straightforward provided certain guidelines are adhered to. A relatively simple relationship exists between sense and load currents. dependent on the value of sense resistor used.

Abstracts

Full-wave sensorless drive ICs for brushless DC motors

The TDA514x range of single-chip, highly-integrated drive ICs are ideal for increasing the cost effectiveness and reliability of 3-phase brushless DC motors such as those used for driving VCR scanner heads, CDs, camcorder tapes, computer hard/floppy disks and automotive fuel pumps. Commutation timing is determined by internally sensing zero crossings of the back-EMF generated by the three rotor windings, eliminating the need for costly rotor position sensors. The ICs have a very accurate digital tacho output, and some have facilities for generating phase (position) information from a simple external pick-up coil or AC-coupled Hall-effect sensor. They also contain an uncommitted operational transconductance amplifier that can be used for motor speed control by regulating the DC supply to the output driver stages.

Printed wiring boards incorporating Cu-invar-Cu layers

A new design of multilayer printed wiring board is now available with incorporated copper-invar-copper (CIC) planes for high-density packing of SMDs, in applications where high reliability requirements are imperative. Each CIC plane has an extremely low thermal coefficient of expansion, is an ideal heatsink and heat spreader, adds rigidity to the multilayer board, and can be used as a power and ground plane. Also, by varying the ratio of copper to invar (a nickel-iron alloy), a range of CICs compatible to almost any outline can be achieved.

I^2C-bus control programs for consumer applications

A set of I^2C-bus control programs is available on diskette that allow engineers to evaluate, analyse and test the functions of I^2C-bus compatible ICs for radio/audio and TV, even if they don't understand the internal software structure of the circuits. All that's needed to run the control programs is an IBM compatible PC and a simple I^2C-bus interface board connected between the I^2C-bus of the board under test and the CENTRONICS parallel printer port of the PC. The programs incorporate a database containing IC control data, and a set of easy to use dedicated or universal menus for controlling the ICs. All the menus are self explanatory and the desired functions can be accessed with a single keystroke. The dedicated menus show all the control functions of the associated IC divided into logical groups. All data communication on the I^2C-bus is subjected to error checking and, if errors occur, they're displayed as simple messages on the PC screen. All data written to the register(s) of the IC is checked for illegal range and forbidden combinations with other control settings.

Black matrix colour picture tubes

Philips' latest 45AX colour-picture-tube range embodies a *black matrix* system based on a novel deposition process. The range has been developed to satisfy the latest market needs of bright, high-contrast pictures to allow daytime TV viewing, coupled with dark, inconspicuous screens when the set is switched off. In addition, the trends toward larger (jumbo) screens and higher screen resolution (in anticipation of future HDTV) can realistically be met only with a black matrix system. Philips well-known HiBri system, till now the best tube technology available, will therefore gradually be replaced completely by black matrix.

DRYPACK protects ICs in large plastic packages against moisture

If infrared or vapour-phase soldering is used to surface mount an Ic in a large plastic package, vapourization of the small amount of moisture absorbed by the package during storage can increase the internal pressure to such an extent that the plastic cracks. This phenomenon is known as Moisture Induced Plastic Package Cracking (MIPPC). An immediate solution to the problem can be provided by delivering ICs in MIPPC-sensitive packages in a resealable moisture-resistant plastic packet called a DRYPACK.

World System Teletext (WST) ICs

This article gives an overview of the two basic teletext system configurations using WST ICs. The first configuration uses one of our new range of Integrated VIP and Text (IVT) ICs SAA55244/5246/5247. The SAA5246 (IVT1.0) needs an external 8K × 8-bit SRAM for storing four pages (extension packet mode) or eight pages (normal mode). With an SAA5244 (IVT1.1), a single-page RAM is built into the chip so that no external RAM is necessary. The SAA5247 (IVT1.1BMC) with Background Memory Control (BMC) has an on-chip single-page RAM and facilities for storing up to 512 pages in external DRAM which is rapidly scanned on each page request to give near instant page access. The second configuration is intended for top-of-the-range analog, digital or features TV sets. It uses an SAA9042 Digital Video Teletext (DVT) IC with either an SAA5191 Video Input Processor (VIP) or an SAA5235/6 dataline slicer.

An integrated chipset for cellular mobile telephones

The complex circuitry of existing mobile telephones is a compromise consisting of standard-function ICs for processing the analog signals, and ASICs for performing the digital functions. The six dedicated bipolar and CMOS ICs of the described chip-set reduce circuit complexity and power consumption and are suitable for both AMPS and TACS systems. The RF section of a mobile telephone using the chip-set comprises a single-chip frequency synthesizer, and a single-chip second mixer/oscillator/IF amplifier/demodulator. Switched-capacitor integrated filter technology and VLSI are fully exploited in the baseband processing area where a single-chip CMOS data processor performs all the functions associated with data control and generation of supervisory and signalling tones. All the voice, alert and DTMF functions are performed by two audio processor ICs, one CMOS, the other bipolar. The microcontroller at the heart of the system is the low-power high-speed PCB80C552 which is a derivative of the industry-standard 8051.

TDA4670 Picture Signal Improvement (PSI) circuit

The quality of a TV picture can be enhanced by correcting the degradation of definition caused by the bandwidth limitation imposed on the chrominance and luminance signals by their separation filters. This is done by the I^2C-bus controlled TDA4670 PSI IC, successor to the well-known TDA4565 Colour Transient Improvement (CTI) IC. The TDA4670 improves the colour definition by the display by decreasing the rise and fall times of the colour-difference signal transients. It also includes a variable luminance delay line with aperture correction (luminance signal peaking) for contrast enhancement, and performs noise reduction by coring to eliminate the consequent increase of noise level on the luminance signal.

Colour monitor tubes with magnetic-field suppression and antistatic coating

Philips Components' range of colour monitor tubes are now available with several options – VLMF (Very-Low-frequency Magnetic Field) suppression coils to allow monitor manufacturers to meet the latest Nordic requirements, and anti-glare/antistatic coatings for greater operator comfort. The magnetic field is compensated by two coils mounted above and below the yoke at a slight angle to the vertical, and measurements clearly indicate that the performance of the tubes with VLMF suppression falls well within Nordic requirements. Furthermore, our current generation of monitor tubes can be provided with a single anti-glare coating whose performance compares favourably with direct-etch tubes, or a combined antistatic/anti-glare coating.

Introducing the Philips SensorFET

The Philips SensorFET is essentially a Power MOSFET that divides load current into power and sense parts. Instantaneous sense current can then be monitored by either an inexpensive signal-level resistor, or by the virtual-earth opamp arrangement. This reduces power losses and offers an efficient method of current sampling in power circuits. A relatively simple relationship exists between sense and load currents, so circuit design is straightforward provided certain guidelines are adhered to.

ICs für die sensorlose Ansteuerung von bürstenlosen Gleichstrommotoren

Die Reihe TDA514x umfaßt hochintegrierte-Einchip-Ansteuerungs-ICs, mit denen die Zuverlässigkeit und Kosteneffektivität von bürstenlosen Dreiphasen-Gleichstrommotoren, die zum Beispiel für VCR-Abtastköpfe, CD-Spieler, Camcorder, Festplatten- und Diskettenlaufwerke sowie für Kraftstoffpumpen in Kraftfahrzeugen benutzt werden, erheblich gesteigert werden können. Die Kommutierungszeiten werden durch internes Abtasten der Nulldurchgänge der Gegen-EMK, die durch die drei Rotorwicklungen erzeugt wird, bestimmt, so daß keine aufwendigen Rotorpositions-Sensoren erforderlich sind. Die ICs verfügen über einen sehr genauen digitalen Tacho-Ausgang, und einige ICs sind dazu noch in der Lage, Phasen-(Positions-)Informationen von einer einfachen externen Sonden-spule oder einem AC-gekoppelten Halleffekt-Sensor abzuleiten. Die ICs enthalten einen universellen Transkonduktanz-Operationsverstärker, mit dem die Motordrehzahl durch Regelung der Gleichstromversorgung für die Ausgangstreiberstufen gesteuert wird.

Leiterplatten mit Cu-Invar-Cu-Schichten (CIC)

Es sind jetzt neuartige Multilayer-Leiterplatten mit Kupfer-Invar-Kupfer-Schichtaufbau (CIC) verfügbar. Sie erlauben eine hohe Packungsdichte von SMD-Bauelementen in Applikationen, bei denen eine hohe Zuverlässigkeit oberste Priorität besitzt. Die CIC-Schichten besitzen einen extrem kleinen Wärmeausdehnungskoeffizienten und sind ideale Wärmesenken und Wärmeverteiler. Außerdem tragen sie maßgeblich zur Erhöhung der Steifigkeit der Multilayer-Leiterplatte bei und können sowohl als Stromversorgungs- und als auch als Masseebene verwendet werden. Durch Variieren des Dickenverhältnisses zwischen Kupferschichten und Invarschicht (Nickel-Eisen-Legierung) entsteht eine Familie von CIC-Leiterplatten, die für praktisch jeden Applikationsfall eine geeignete Lösung bereitstellt.

I²C-Bus-Steuerprogramme für Anwendungen in der Unterhaltungselektronik

Eine Reihe von I²C-Bus-Steuerprogrammen ist jetzt auf Diskette erhältlich, mit denen Techniker auch dann die Funktionen von I²C-Bus-kompatiblen ICs für Radio-, Audio- und Fernsehgeräte auswerten, analysieren und testen können, wenn sie die interne Software-Struktur der Schaltungen nicht kennen. Um diese Steuerprogramme benutzen zu können, braucht man lediglich einen IBM-kompatiblen PC und eine einfache I²C-Bus-Schnittstellenkarte, die zwischen den I²C-Bus der getesteten Leiterplatte und den parallelen Schnittstellenanschluß des PCs geschaltet wird. Die Programme enthalten eine Datenbank mit IC-Steuerungsdaten sowie eine Reihe von bedienerfreundlichen speziellen oder universellen Menüs zur Steuerung der ICs. Alle Menüs sind leicht verständlich, und die gewünschten Funktionen können mit einem einzigen Tastendruck aufgerufen werden. Die speziellen Menüs enthalten alle Steuerfunktionen des entsprechenden ICs, die in logischen Gruppen zusammengefaßt sind. Die gesamte Datenkommunikation auf dem I²C-Bus wird einer Fehlerprüfung unterzogen. Wenn Fehler gefunden werden, erscheinen entsprechende Meldungen auf dem Monitor des PCs. Bei allen Daten, die in Register des ICs geschrieben werden, erfolgt eine Prüfung auf unzulässige Bereiche und unzulässige Kombinationen mit anderen Steuereinstellungen.

Black-Matrix-Farbbildröhren

Die neueste 45AX-Farbbildröhren-Reihe von Philips wird mit einem speziellen Bildschirm-Beschichtungsverfahren, dem sogenannten Black-Matrix-System, hergestellt. Diese Bildröhren-Reihe wurde entwickelt, um die Nachfrage nach einem brillanten, kontrastreichen Bild auch bei Tageslicht sowie nach einem dunklen, unauffälligen Bildschirm bei ausgeschaltetem Fernsehgerät zu erfüllen. Außerdem kann dem Trend nach größeren Bildschirmen mit höherer Auflösung (im Vorgriff auf HDTV) praktisch nur mit dem Black-Matrix-System entsprochen werden. Die bislang beste Bildröhrentechnologie, das bekannte HiBri-System von Philips, wird aus diesem Grunde nach und nach vollkommen durch das Black-Matrix-Sytem ersetzt.

DRYPACK schützt ICs in großen Kunststoffgehäusen vor Feuchtigkeit

Werden ICs in SMD-Technik mit Infrarot- oder Dampfphasenlöten montiert, kann bei großen Kunststoffgehäusen der Innendruck der verdampfenden Feuchtigkeit, die das Gehäuse während der Lagerung absorbiert, so ansteigen, daß der Kunststoff rissig wird. Dieses Phänomen ist unter der Bezeichnung "Moisture Induced Plastic Package Cracking" (MIPPC) bekannt. Das Problem der MIPPC-empfindlichen ICs läßt sich durch ein neues, gegen Feuchtigkeit versiegelbares Gehäuse namens DRYPACK umgehen.

ICs für World System Teletext (WST)

Dieser Beitrag liefert eine Übersicht über die beiden grundlegenden Videotext-Systemkonfigurationen auf der Basis unserer WST-ICs. In der ersten Konfiguration wird ein IC aus unserer neuen IVT-Reihe (IVT = Integrierte Video input processor- und Teletext-Schaltung) SAA55244 /5246/5247 verwendet. Die Schaltung SAA5246 (IVT1.0) kann mittels eines externen 8K × 8 bit-SRAMs im "erweiterten Paket-Betrieb" (extension packet mode) bis zu vier Videotext-Seiten, im Normalbetrieb sogar acht Videotext-Seiten speichern. (Videotext heißt nach deutscher Norm "Fernsehtext", internationaler Oberbegriff ist "Teletext".) Die Schaltung SAA5244 (IVT1.1) verfügt über ein eingebautes 1-Seiten-Speicher-RAM, benötigt also keinen externen Seitenspeicher. Die Schaltung SAA5247 (IVT1.1BMC) mit "Hintergrund-Speicher-Steuerung" (Background Memory Controller, BMC) besitzt ebenfalls ein On-chip-1-Seiten-RAM, erlaubt aber darüber hinaus das Abspeichern von bis zu 512 Seiten in einem externen DRAM, das bei jeder Seitenanforderung sehr schnell durchsucht wird, so daß sich ein quasi-wartezeitloser Zugriff auf die gewünschte Seite ergibt. Die zweite Systemkonfiguration ist für Fernsehgeräte der Komfort-Spitzenklasse mit analogen und digitalen Funktionen vorgesehen. Hier kommt ein Digital Video Teletext (DVT)-IC SAA9042 zum Einsatz, in Verbindung entweder mit einem Video Input Processor (VIP) SAA5191 oder mit einem Dataline Slicer SAA5235/5236.

Ein integrierter Chipsatz für zelluraren Mobilfunk

Die komplexen Schaltungen von Mobilfunk-Telefonen bestehen aus Standard-ICs für die analoge Signalverarbeitung und ASICS für digitale Funktionen. Mit den sechs anwendungsspezifischen bipolaren und CMOS-ICs des beschriebenen Chipsatzes ist es möglich, die Schaltung wesentlich einfacher aufzubauen und gleichzeitig die Leistungsaufnahme zu reduzieren; diese Bauelemente eignen sich sowohl für AMPS- als auch für TACS-Systeme. Der HF-Teil eines Mobilfunk-Telefons mit dem Chipsatz besteht aus einem Einchip-Frequenzsynthesizer und einem Einchip-Mischer/Oszillator/ZF-Verstärker/Demodulator als zweitem IC. Die integrierte Filtertechnologie mit geschaltetem Kondensator sowie die VLSI-Technologie werden im Basisbandbereich voll ausgenutzt, wo ein Einchip-CMOS-Datenprozessor für alle Funktionen im Zusammenhang mit der Datensteuerung und der Erzeugung von Kontroll- und Signaltönen zuständig ist. Alle Sprach-, Warn- und DTMF-Funktionen werden von zwei ICs zur Audiosignalverarbeitung, einem CMOS-IC und einem Bipolar-IC, gesteuert. Als Schlüsselbauelement des Systems dient ein sehr schneller Mikrocontroller PCB80C552 mit geringer Leistungsaufnahme, der vom Industriestandard 8051 abgeleitet ist.

Die PSI-Schaltung TDA4670 zur Verbesserung des Bildsignals (Picture Signal Improvement)

Die Qualität eines Fernsehbildes kann durch die Korrektur der Auflösungsverminderung verbessert werden, die infolge der Verkleinerung der Bandbreite des Chrominanz- und Luminanzsignals durch die Filter zur Trennung dieser beiden Signale entsteht. Diese Korrektur erfolgt durch die I²C-Bus-gesteuerte PSI-Schaltung TDA 4670, die der Nachfolger der bekannten CTI-Schaltung TDA 4565 (Colour Transient Improvement) ist. Die integrierte Schaltung TDA 4670 verbessert die Farbauflösung des wiedergegebenen Fernsehbildes durch eine Verkürzung der Anstiegs- und Abfallzeit schneller Farbdifferenzsignalübergänge. Sie enthält auch eine Luminanzverzögerungsleitung mit variabler Laufzeit und Aperturkorrektur (Erzeugung eines einstellbaren symmetrischen Überschwingens an steilen Signalflanken, Peaking) und sorgt für eine Unterdrückung der besonders störenden Rauschsignale bei kleinen Nutzsignalpegeln (Coring), um die Auswirkungen des Rauschpegelanstieges im Luminanzkanal durch die Aperturkorrektur zu verhindern.

Farbmonitorröhren mit Magnetfeldunterdrückung und antistatischer Beschichtung

Farbmonitorröhren von Philips Components sind jetzt in verschiedenen Ausführungen erhältlich. Mit VLMF-Unterdrückungsspulen (VLMF: Very Low-frequency Magnetic Field) ermöglichen sie den Monitorherstellern die Erfüllung der neuesten Nordic-Anforderungen. Die spiegelungsfreie antistatische Beschichtung bietet größeren Sehkomfort. Das Magnetfeld wird durch zwei Spulen kompensiert, die über und unter dem Joch mit geringer Abweichung von der Vertikalen montiert sind. Messungen haben deutlich gezeigt, daß unsere Monitorröhren mit VLMF-Unterdrückung die Nordic-Anforderungen voll und ganz erfüllen. Außerdem können bei unserer aktuellen Monitorröhren-Generation mit einer einzigen Entspiegelungsschicht eher günstigere Ergebnisse erzielt werden als mit einer kombinierten Antistatik-/Entspiegelungs-Beschichtung oder mit direkt geätzten Röhren.

Einführung des SensorFET von Philips

Der SensorFET von Philips ist im wesentlichen ein Leistungs-MOSFET, der den Laststrom in einen Leistungs- und einen Abtastanteil aufteilt. Der direkte Abtaststrom kann dann entweder durch einen kostengünstigen Signalpegel-Widerstand oder durch die Operationsverstärker-Anordnung mit virtueller Masse überwacht werden. Hiermit werden die Leistungsverluste reduziert und eine effiziente Stromabtastung in Leistungsschaltungen ermöglicht. Zwischen dem Abtast- und dem Laststrom besteht ein relativ einfacher Zusammenhang, so daß der Schaltungsentwurf nicht kompliziert ist, wenn bestimmte Richtlinien beachtet werden.

CI de commande biphase sans capteur pour moteurs sans balais à courant continu

La gamme TDA514x de CI de commande à puce unique et à haute intégration augmente parfaitement la rentabilité et la fiabilité des moteurs sans balais à courant continu triphasé tels ceux utilisés pour actionner les têtes de lecture des magnétoscopes, les disques compacts, les cassettes pour camescopes, les disques durs, les disquettes pour ordinateurs et les pompes d'injection pour automobiles. Le temps de commutation est déterminé en détectant intérieurement les croisements au point nul de la sonde FEM arrière, générés par les trois enroulements du rotor, ce qui évite de recourir à de coûteux capteurs de positionnement. Les CI ont une sortie tachymétrique numérique très précise et certains sont dotés de systèmes permettant de générer des informations de phase (position) à partir d'une simple bobine exploratrice externe ou à partir d'un capteur à effet Hall couplé au CA. Ils comportent également un amplificateur asservi de transconductance pouvant être utilisé pour le réglage de la vitesse du moteur en ajustant l'alimentation en CC aux amplificateurs d'attaque de sortie.

Cartes imprimées à couches Cu-invar-Cu

Une nouvelle conception de cartes imprimées multicouches, à couches internes cuivre-invar-cuivre (CIC), a été mise au point. Elle permet une implantation à haute densité de CMS, dans des applications pour lesquelles des exigences de haute fiabilité sont impératives. Chaque couche CIC – à coefficient de dilatation thermique faible – est un dissipateur et un conducteur thermique idéal. De plus, elle augmente la rigidité de la carte multicouches et peut être utilisée comme radiateur. En modifiant le taux de cuivre par rapport à l'invar (alliage nickel-fer), il est possible d'obtenir une gamme de circuits CIC compatibles avec la plupart des configurations.

Programmes de commande de bus I²C pour applications grand public

Un ensemble de programmes de commande de bus I²C est disponible sur disquette et permet aux ingénieurs d'évaluer, d'analyser et de tester les fonctions des CI destinés aux applications radio/audio et TV, compatibles bus I²C, même s'ils ne comprennent pas la structure interne des logiciels des circuits. Un PC compatible avec les ordinateurs IBM ainsi qu'une simple carte d'interface pour bus I²C, reliant le bus I²C de la carte testée à la sortie imprimante parallèle CENTRONICS de l'ordinateur, sont les seuls éléments nécessaires pour faire fonctionner les programmes de commande. Ces programmes comprennent une base de données regroupant des données relatives à la commande du CI ainsi qu'une série de menus spécialisés et polyvalents d'utilisation facile permettant de commander les CI. Tous les menus sont auto-explicatifs et les fonctions souhaitées sont accessibles à l'aide d'une seule touche. Les menus spécialisés indiquent toutes les fonctions de commande des CI associés divisés en groupes logiques. Toutes les transmissions de données du bus I²C sont soumises à la détection d'erreurs et si celles-ci se produisent, elles sont affichées comme simples messages sur l'écran de l'ordinateur. Toutes les données enregistrées dans le(s) registre(s) du CI sont vérifiées afin de détecter toute gamme erronée et les combinaisons interdites par d'autres contrôles de commande.

Tubes-image couleur black matrix

La nouvelle gamme de tubes-image couleur 45AX de Philips est caractérisée par nouveau procédé de dépôt. Cette gamme a été mise au point afin de répondre aux derniers besoins du marché en matière d'amélioration de la brillance et du contraste, permettant de regarder la télévision à la lumière du jour. De plus, l'écran foncé donne un aspect discret lorsque l'appareil est mis hors service. En outre, seul le système black matrix permet de réaliser des écrans de plus grande taille et à plus haute résolution (en prévision de la future TVHD). Le fameux système HiBri de Philips, qui constitue jusqu'à ce jour la technologie la plus avancée en matière de tubes, sera donc progressivement et entièrement remplacé par le black matrix.

DRYPACK protège les CI de l'humidité dans des conditionnements en plastique de grande taille

Lorsque l'on a recours au brasage à infrarouge ou en phase vapeur lors du montage en surface d'un circuit intégré dans un conditionnement en plastique de grande taille, il se peut que la faible quantité d'humidité absorbée par le conditionnement lors du stockage augmente la pression interne à un point tel que la matière plastique se fissure. Ce phénomène est connu sous le nom de fissurage du conditionnement en plastique provoqué par l'humidité (MIPPC = Moisture Induced Plastic Package Cracking). Une solution immédiate au problème consiste à placer les CI en boîtiers sensibles au MIPPC dans un conditionnement en plastique, appelé DRYPACK, résistant à l'humidité et pouvant être refermé hermétiquement.

Circuits intégrés pour WST (Système de télétexte mondial)

Cet article donne un aperçu des deux principales configurations de systèmes de télétexte utilisant des CI WST. La première configuration utilise l'un des CI de notre nouvelle gamme de circuits IVT (Integrated VIP and Text), à savoir le SAA5244/5246/5247. Le SAA5246 (IVT1.0) requiert une mémoire RAM statique externe de 8K × 8 bits permettant de mémoriser quatre pages (possibilité de mode paquet) ou huit pages (mode normal). Grâce au SAA5244 (IVT1.1) une mémoire vive d'une seule page est incorporée au circuit intégré, de sorte qu'aucune mémoire vive externe n'est nécessaire. Le SAA5247 (IVT1.1BMC) avec commande de mémoire en arrière-plan (BMC) comprend une mémoire RAM pour une page ainsi que des systèmes permettant de mémoriser jusqu'à 512 pages en mémoire RAM dynamique externe rapidement explorée à chaque demande de page et permettant un accès de page presque instantané. La deuxième configuration est destinée aux téléviseurs analogiques, numériques ou avec fonctions de haut de gamme. Elle utilise un CI SAA9042 Digital Video Teletext (DVT) doté soit du processeur pour entrée vidéo (Video Input Processor, VIP) SAA5191 soit d'un filtre limiteur de liaison SAA5235/6.

Un ensemble de puces intégré pour la radiotéléphonie mobile cellulaire.

Les montages compteurs des radiotéléphones mobiles numériques actuels sont constitués de circuits intégrés standard pour le traitement des signaux analogiques et de circuits intégrés spécifiques pour l'exécution des fonctions numériques. les six circuits bipolaires et CMOS spécifiques diminuent la complexité du montage et la consommation et conviennent aussi bien pour les systèmes AMPS que TACS. La section RF d'un radiotéléphone mobile équipé de cet ensemble de puces comprend un synthétiseur de fréquence et un mélangeur/oscillateur/amplificateur IF/démodulateur. La technologie des filtres intégrés à condensateur commuté et l'intégration de haut niveau sont largement exploitées dans la section de traitement de la bande de base où un processeur de données CMOS exécute toutes les fonctions relatives au contrôle des données et à la génération des tonalités de surveillance et de signalisation. Toutes les fonctions vocales, d'alerte et DIMF sont exécutées par deux circuits intégrés de traitement audio, l'un CMOS, l'autre bipolaire. Le coeur du système est le microcontrôleur rapide basse puissance PCB80C552, dérivé du 8051 employé dans l'industrie.

Circuit d'amélioration des signaux de l'image (PSI) TDA4670

La qualité d'une image de télévision peut être améliorée en corrigeant la perte de qualité de la définition due à la limitation de la bande passante imposée aux signaux de chrominance et de luminance par leurs filtres séparateurs. Cette opération est effectuée par le TDA4670, CI de PSI, commandé par le bus I²C, succédant au TDA4565, CI bien connu d'amélioration de transition des couleurs (CTI). Le TDA4670 améliore la définition des couleurs de l'écran en diminuant les temps de montée et de descente des signaux de transition de la différence de couleur. Il comporte également une ligne de retard de luminance variable avec correction de l'ouverture (alignement de crête du signal de luminance) pour amélioration du contraste et réduit le bruit afin d'éliminer l'augmentation du niveau de bruit qui en résulte sur le signal de luminance.

Tubes moniteur couleur avec suppression du champ magnétique et revêtement antistatique

La gamme de tubes moniteur couleur de Philips Composants est à présent disponible avec différentes options, telles les bobines de suppression VLMF (Very Low Frequency Magnetic Field), permettant aux fabricants de moniteurs de répondre aux dernières exigences en vigueur dans les pays scandinaves, et les revêtements antireflets/antistatiques pour un plus grand confort de l'utilisateur. Le champ magnétique est neutralisé par deux bobines montées au-dessus ou au-dessous du déviateur formant un angle par rapport à la verticale. Les mesures indiquent clairement que le fonctionnement des tubes dotés de suppression VLMF satisfait aux exigences des pays scandinaves. Il est en outre possible d'appliquer aux tubes moniteurs de la dernière génération soit une couche unique anti-reflets, dont l'efficacité soutient la comparaison avec les tubes à traitement chimique, soit une couche antistatique/antireflets.

Introduction du SensorFET Philips

Le SensorFET Philips est un transistor MOS de puissance possédant deux sorties de courant : une sortie de puissance et une sortie permettant la lecture du courant circulant dans le transistor MOS. Le courant instantané issu de cette deuxième sortie peut être traité soit par une résistance faible puissance (de faible coût), soit par un amplificateur opérationnel dont la masse sera reliée à la masse virtuelle du SensorFet. Ce composant permet la réduction des pertes de puissance, il permet aussi d'obtenir une représentation du courant efficace circulant dans le circuit de puissance. Une relation relativement simple unit le courant de lecture et le courant de sortie; de ce fait, sans modifier fondamentalement le circuit de puissance, la conception des circuits est aisée.

Circuitos integrados de control sin sensores en onda completa para motores de c.c. sin escobillas

La familia de circuitos integrados monochip de alta integración para el control de motores de c.c. TDA514X resulta ideal para mejorar la relación entre el coste y la fiabilidad en el control de motores de c.c. de 3 fases sin escobillas del tipo habitualmente utilizado en las cabezas de exploración de magnetoscopios, reproductores de compact disc, videocámaras, unidades de discos flexibles/duros de ordenadores y bombas de combustible en automóviles. La temporización de la conmutación se determina a partir de un sensor de cruce por cero interno de la fuerza contraelectromotriz que se genera en los tres bobinados del rotor, eliminándose de esta forma la necesidad de utilizar costosos sistemas de control de posición del rotor. Estos circuitos integrados incluyen una salida tacométrica digital de alta precisión, y algunos de ellos ofrecen la posibilidad de elaborar información de fase (posicionamiento) a partir de una sencilla bobina sensora o de un sensor de efecto Hall acoplado en c.a. Contienen también un amplificador operacional de transconductancia que puede utilizarse para el control de la velocidad del motor mediante la regulación de la tensión continua de alimentación de las etapas de excitación de salida.

Placas de circuito impreso con capas de Cu-invar-Cu

En la actualidad se dispone de una nueva tecnología para el diseño de placas de circuito impreso multicapa mediante la incorporación de capas de cobre-invar-cobre (CIC) para encapsulados SMD de alta densidad, en aplicaciones donde se exige una alta fiabilidad. Cada capa CIC tiene un coeficiente de expansión extremadamente bajo, actúa como radiador y dispersador de calor ideales, añade rigidez a la placa multicapa, y puede usarse como plano de masa y de alimentación. Además, variando la relación entre cobre e invar (una aleación de níquel-hierro), se puede conseguir una gama de capas CIC compatible con casi cualquier configuración.

Programas de control del bus I²C para aplicaciones de consumo

Se dispone de una serie de programas de control para el bus I·C que permiten a los ingenieros evaluar, analizar y comprobar el funcionamiento de los circuitos integrados compatibles con el bus I·C para radio/audio y TV, aunque desconozcan la estructura del software interna de los circuitos. Lo único que se necesita para utilizar dichos programas de control es un PC compatible y una sencilla tarjeta interface I·C conectada entre el bus I·C de la tarjeta bajo prueba y el puerto paralelo CENTRONICS del PC. Los programas incorporan una base de datos que contiene los datos de control de los circuitos integrados, así como un conjunto de menús universales o específicos de fácil utilización para el control de los circuitos integrados. Todos los menús son autoexplicativos, y las funciones deseadas son accesibles mediante una pulsación única en el teclado. Los diferentes menús específicos muestran todas las funciones de control del CI asociado divididas en grupos lógicos. Todas las transmisiones de datos a través del bus I·C están sujetas a la comprobación de errores y, en caso de que se detecte alguno, éste es visualizado como un sencillo mensaje en la pantalla del PC. Todo dato escrito en el(los) registro(s) de control de los circuitos integrados es verificado en lo que se refiere al margen permitido y a las combinaciones prohibidas con otros ajustes de control.

Tubos de imagen en color black matrix

La gama más reciente de tubos de imagen en color Philips 45AX incorpora un sistema *black matrix* basado en un nuevo proceso de deposición. Esta gama se ha desarrollado de forma que satisfaga las necesidades actuales del mercado en cuanto a brillo, imágenes de alto contraste que permitan una buena visión de TV a la luz del día, y pantallas oscuras e invisibles cuando el televisor esté desconectado. Además, la tendencia hacia las pantallas gigantes (jumbo) y hacia las de mayor resolución (anticipándose a la futura televisión HDTV) sólo podrá materializarse realmente mediante el uso del sistema *black matrix*. Por consiguiente, el conocido sistema HiBri de Philips, hasta ahora la mejor tecnología disponible en la producción de tubos de TV, será gradualmente reemplazado por el sistema *black matrix*.

El encapsulado DRYPACK protege los CIs en grandes encapsulados plásticos contra la humedad

Cuando se utiliza soldadura por infrarrojos o por fase de vapor en el montaje superficial de un circuito integrado con encapsulado plástico de gran tamaño, la vaporización de la pequeña cantidad de humedad absorbida por el encapsulado durante el almacenamiento puede incrementar la presión interna hasta tal extremo que el plástico se rompe. Este fenómeno es conocido como ruptura del encapsulado plástico inducida por la humedad (Moisture Induced Plastic Package Cracking, MIPPC). Una solución inmediata al problema consiste en suministrar los circuitos integrados con un encapsulado plástico resistente a la humedad, denominado DRYPACK.

Circuitos integrados para el World System Teletext (WST)

Este artículo ofrece una visión resumida de las dos configuraciones básicas de sistemas de teletexto que utilizan circuitos integrados WST. La primera de ellas emplea una de nuestras nuevas familias de circuitos integrados de proceso de señales de vídeo y texto, VIP & Text (IVT). SAA5244/5246/5247. El SAA5246 (IVT1.0) requiere una memoria SRAM externa de 8K × 8 bits para el almacenamiento de cuatro páginas (modo de extensión de paquetes) u ocho (modo normal). Con el SAA4244 (IVT1.1) se incluye una memoria RAM de una página en el propio circuito integrado, de forma que no resulta necesaria una memoria RAM externa. El SAA5247 (IVT1.1BMC) con Control de Memoria de Archivo (BMC, Background Memory Control) incluye en el propio chip una memoria RAM de una página, así como facilidades para almacenamiento de hasta 512 páginas en una memoria DRAM externa que se explora con gran rapidez cada vez que se solicita una página, proporcionando un acceso prácticamente instantáneo a ésta. La segunda de las configuraciones está destinada a los aparatos de TV analógicos o digitales de la más alta gama de prestaciones. Utiliza un circuito integrado de vídeo digital de teletexto SAA9042 (DVT, Digital Video Teletext), un procesador de entrada de vídeo SAA5191 (VIP, Video Input Processor) o un segmentador de datos en línea SAA5235/6.

Montajes integrados para teléfonos móviles celulares

La compleja circuitería de los teléfonos móviles existentes implica un compromiso entre los circuitos integrados estándar para el proceso de las señales analógicas y los ASICs para las funciones digitales. Los seis circuitos integrados dedicados bipolares y CMOS del montaje descrito reducen la complejidad del circuito y el consumo de potencia, y son válidos para sistemas AMPS y TACS. La sección de RF de un teléfono móvil que utilice estos circuitos integrados consta de un sintetizador de frecuencia monochip y de un segundo chip sencillo mezclador/oscilador/amplificador F.I/demodulador. La zona de proceso de banda base utiliza ampliamente tecnología de filtros integrados de condensador conmutado y VLSI (integración a muy gran escala), en la que un procesador de datos CMOS ejecuta todas las funciones asociadas con el control de datos y la generación de tonos de supervisión y señalización. Todas las funciones de voz, alerta y DTMF son ejecutadas por dos procesadores de audio integrados, uno de ellos CMOS y el otro bipolar. El microcontrolador en el corazón del sistema es el PCB80C552, que es un microcontrolador de baja potencia y alta velocidad, derivado del 8051 estándar.

Circuito de mejora de imagen (PSI) TDA4670

La calidad de imagen de TV puede mejorarse si se corrige la degradación en la definición debida a la limitación del ancho de banda impuesta por los filtros separadores de las señales de luminancia y crominancia. Esta mejora puede conseguirse mediante el uso del circuito integrado controlado por el bus I^2C TDA 4670, sucesor del popular circuito de mejora de los transitorios de color (CTI) TDA 4565. El TDA4670 mejora la definición del color en la pantalla mediante la reducción de los tiempos de subida y bajada de los transitorios de la señal de diferencia de color. Incluye también una línea de retardo variable para la señal de luminancia con corrección de apertura (seguimiento de picos de la señal de luminancia) para la mejora del contraste, reduciendo el ruido mediante bobinas para eliminar el incremento de los niveles de ruido de la señal de luminancia.

Tubos en color para monitores con supresión de campo magnético y revestimiento antiestático

La gama actual de Philips Components de tubos en color para monitores incluye diversas opciones: supresión del campo magnético de muy baja frecuencia (VLMF, Very-Low-Frequency Magnetic Field) para satisfacer las recientes especificaciones en los países nórdicos, así como recubrimientos antirreflectantes y antiestáticos para mayor comodidad del usuario. El campo magnético se compensa mediante dos bobinas situadas encima y debajo del yugo con un pequeño ángulo respecto de la vertical. Las mediciones indican claramente que el comportamiento de los tubos con supresión de VLMF satisfacen adecuadamente los requerimientos de los países nórdicos. Además, nuestra generación actual de tubos para monitores puede suministrarse con un recubrimiento antirreflectante cuyas prestaciones compiten favorablemente con los tubos o con un recubrimiento antiestático/antirreflectante.

Presentación de los transistores SensorFET de Philips

Los SensorFET de Philips son esencialmente transistores MOSFET que dividen la corriente que circula por la carga en una parte de potencia y otra de control. La corriente instantánea de control puede ser monitorizada tanto con una económica resistencia de muestreo de nivel como mediante un montaje de masa virtual con amplificador operacional. Este dispositivo reduce las pérdidas de potencia y ofrece un eficiente método de muestreo en corriente en circuitos de potencia. Existe una relación relativamente sencilla entre las corrientes de control y carga de manera que el diseño del circuito es inmediato siempre que cumpla determinadas normas.

Authors

Ad van den Eeden received a PhD in chemistry in 1984 and joined Philips in March the following year. In 1989 he moved to Philips' Technology Centre Display Components (TCDC) and is currently department manager for process development with special responsible for coatings.

Leo van Gemert was born in Arnhem, The Netherlands, in 1960 and graduated in chemical engineering from the University of Breda in 1984. The same year he joined Philips Components and since then he has been involved in IC package development and technology.

Alfred Goberecht was born in 1938 and in 1961 he received a chemical-industrial engineering degree from RHIK, Brussels, Belgium. The following year he joined MBLE, Brussels, working initially on non-linear resistors. In 1965 he became a process engineer for printed-circuit boards and for the last 15 years he has been involved in PCB technology development. More recently he has also been involved in international customer service.

Trevor Hall was born in Hampton, England in 1960. He graduated with a BSc (Eng) from London University in 1981 and then joined Mullard (subsequently Philips Components) as a development engineer, working on teletext and Viewdata products. In 1985 he moved to the Application Laboratory to work in the Mobile Communications Group on the use of micro-controllers within cellular radio equipment, and real-time software design. He is currently section leader within this group responsible for the application support of Philips' cellular radio chipset.

Peter Hart was born in London in 1947. He received a BSc in electronic engineering from Sussex University and in 1970 joined the Application Laboratory of Mullard (subsequently Philips Components). He has worked on the applications and development of RF power transistors and modules, receiver and frequency synthesizer ICs and components for cellular radio and cordless telephones. He is currently group leader in the Communications Section primarily responsible for cellular radio and RF applications.

Seyno Sluyterman was born in Eindhoven, The Netherlands, in 1952 and graduated in physics from the University of Eindhoven in 1979. The same year he joined Philips' Consumer Electronics Division where he was involved in the development of deflection units for monochrome and colour picture tubes. This activity was subsequently transferred to the Display Components BU of Philips Components Division and in 1986 Seyno became manager of a group responsible for basic development of deflection units. In 1989 he became group leader of the Advanced Technology Department of Philips' Technology Centre Display Components.

Julian Humphreys was born in Rotherham, England in 1962. After graduating from Liverpool University, he joined Philips Components in 1986, working as a measurement engineer. In 1988 he received a doctorate for his research into failure modes of high voltage bipolar transistors. He is currently responsible for the Power Semiconductor Application Laboratory at Hazel Grove, England

Peter Kelting was born in Uetersen, Germany in 1946 and after graduating from the Technical School of Hamburg in 1970, he joined Philips' Product Concept and Application Laboratory, Hamburg. As a member of the television group, he was involved in the development of horizontal deflection circuits and remote control circuits. Since 1981 ha has concentrated on applications of colour TV decoders and picture-signal improvement circuits.

John Kinghorn was born in Newcastle upon Tyne in 1950, and obtained his degree in electronics from the University of Sussex in 1971. He then joined the Mullard Application Laboratory, Mitcham, UK, working initially on switched-mode power supplies and digital systems. Since 1973 he has been involved in the development of teletext systems and ICs. He is currently text section manager in the applications laboratory of Philips Semiconductors' Integrated Circuit and Application Centre in Southampton.

Dominique Pouilloux was born in 1959 and graduated from the Electronics High School, Caen, France, in 1983. The same year he joined Philips Semiconductors, Caen, as an IC design engineer. After a period at the Philips Research Laboratories, Eindhoven, he joined the Caen Marketing Team in 1987 as international product marketing manager with responsibility for Caen audio and motor control products.

Philips Components

PHILIPS