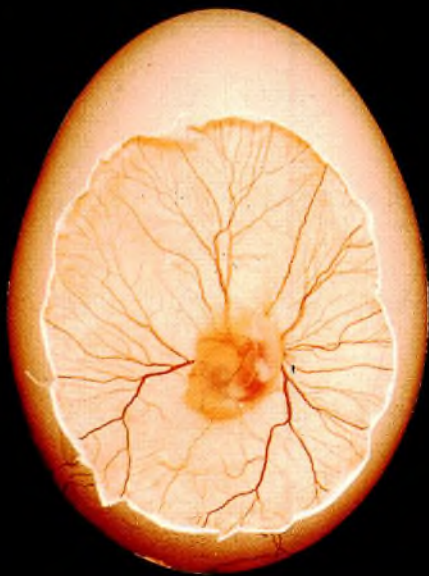


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Editors

Edmund G. Evans (Mitscham)
William E. Martin (Eindhoven)
Michael J. Prescott (Mitscham)

Design and Production

Cees J. M. Gladdines
Bernard W. van Reenen
Michael J. Rose

Design consultant

Theo Kentie

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It is in temperature control, particularly in time proportional control systems that thyristors and triacs have found their métier. In chicken hatcheries, for example, deviations of more than 0.1°C can represent a considerable loss in investment. In the article beginning on page 164 attention is paid to understanding these ubiquitous devices and of the ways in which various manufacturers rate them. Reading and interpreting the small print in data sheets requires a sound knowledge of the devices but yields its reward in fundamentally reliable systems.

Reliability proven: BDW55/56 gold-gold medium-power transistors

S. SLIEDREGT

Following the successful introduction of barrier-layer metallisation and eutectic chip bonding (Ref.1), it became possible to design a version of the well-tried SOT-32 series of medium-power plastic-encapsulated transistors that could replace TO-5 metal-can devices in professional applications. Obviously, such devices would have to be of established, exceptional reliability. Accordingly, a two-year programme of reliability investigation was initiated to establish the properties of the new design beyond all reasonable doubt.

Samples of the first of the series, the BDW55, were subjected to testing at, and above, design ratings for periods up to 10 000 h. The main reliability conclusions were:

- wire bonds, failure rate less than 15×10^{-9} /h per bond with 60% upper confidence level;
- electromigration, none observed after 10 000 h at twice rated current;
- thermal (power) cycling, useful life in excess of 500 000 cycles at a peak junction temperature of 175 °C.

From these results it is clear that these new transistors have a reliability well in excess of design expectations.

This article is based on results obtained by the staff of Philips' Central Quality Laboratory, Discrete Semiconductors, Nijmegen, The Netherlands.

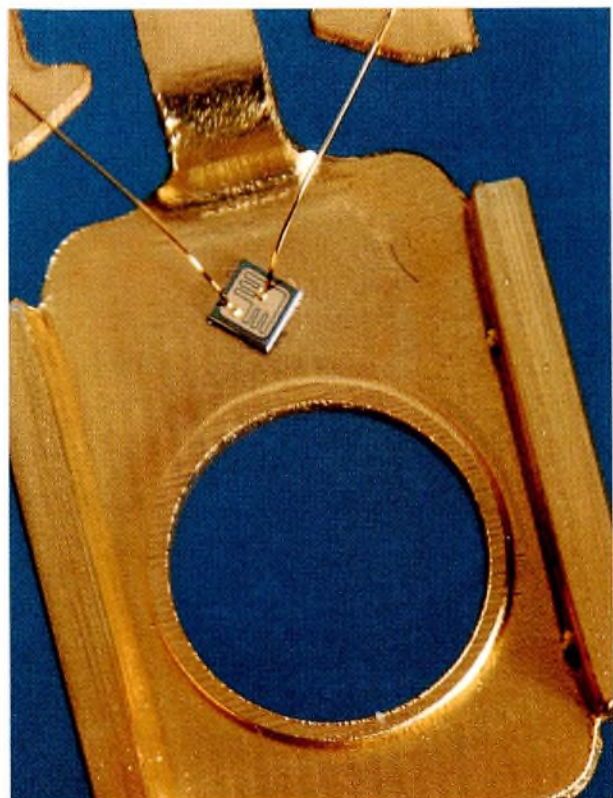


Fig.1 A BDW55 transistor before encapsulation, showing gold-metallised, passivated chip surface, gold internal connecting wires and gold-plated lead frame

DEVICE DESCRIPTION

The BDW55, BDW57 and BDW59 are general-purpose, n-p-n, 8 W power transistors in SOT-32 (TO-126) plastic packages intended for applications where high reliability is essential, especially telecommunications. A complementary, p-n-p series, BDW56, BDW57, BDW60, is also available. Figure 1 shows a BDW55 before encapsulation; Table 1 gives principal data. The main design features of the series are:

- passivated silicon-planar chip;
- titanium-platinum-gold barrier-layer metallisation;
- gold-silicon eutectic, hard-soldered chip bond;
- gold connecting wires;
- gold-plated lead frame;
- silicone-plastic case.

The materials and methods used in each aspect of the construction of the device must be reliable in service, reproducible in production, and compatible with all other materials and methods used. Provided it is not misused, a silicon chip alone has no failure mechanism and does not wear out. All the problems are introduced in the process of making electrical connections to the chip, providing heat flows paths and protective encapsulation.

Chip-to-lead-frame bond

The bond between chip and lead frame provides mechanical anchorage, makes the connection to the collector, and constitutes the main path for the transfer of heat from the device. Each of these functions is important for the performance and life of the device.

A soft-soldered bond has limitations, particularly for power semiconductors. Its thickness is difficult to

control accurately in production, so its thermal resistance may be high to begin with. Soft solder tends to deteriorate with time, increasing thermal resistance still further. Its strength also decreases as the metallurgical change progresses.

Gold forms a eutectic (minimum melting-point mixture) alloy with silicon which melts at 370 °C. Using it as a hard solder, a bond between the chip and the gold-plated lead frame is obtained that is alloyed with both surfaces. These bonds have proved to be mechanically strong, highly controllable in production, exceptionally proof against thermal-cycling stresses, and of low, predictable thermal resistance.

To ensure uniform production, a special bond-test procedure has been developed. This is based on a pulse measurement of junction-to-ambient thermal resistance R_{thj-a} . The value of V_{BE} is measured immediately before and after a power pulse is applied to each transistor. The change in V_{BE} indicates the rise in junction temperature, which, in turn, is related to the thermal resistance. Careful correlation between bond quality and V_{BE} change enables limits to be set against which all devices are checked.

Metallisation

The barrier-layer metallisation system was devised to overcome finally the major disadvantage of the plastic package: its lack of hermeticity. A silicon device chip is not affected by moisture, except for a temporary increase in leakage when impurities are also present. A passivated chip is not affected at all.

Aluminium is the easiest metal to use for the film that interconnects regions of the chip and provides metal pads to which the internal connecting wires can be bonded. Aluminium is easy to deposit, adheres well to silicon dioxide, and does not diffuse into silicon at the

TABLE 1
Quick reference data for BDW55 series, SOT-32 medium-power transistors

		BDW55	BDW57	BDW59	
Collector-base voltage (open emitter)	V_{CBO} max	45	60	100	V
Collector-emitter voltage ($R_{BF} = 1 \text{ k}\Omega$)	V_{CEr} max	45	60	100	V
Collector-emitter voltage (open base)	V_{CEO} max	45	60	80	V
Collector current (peak value)	I_{CM} max		1.5		A
Total power dissipation up to $T_{mb} = 95^\circ\text{C}$	P_{tot} max		8		W
Junction temperature	T_j max		175		°C
D.C. current gain $I_C = 150 \text{ mA}$, $V_{CE} = 2 \text{ V}$	h_{FE} typ		40 to 250		
Transition frequency $I_C = 50 \text{ mA}$, $V_{CE} = 5 \text{ V}$	f_T typ		250		MHz

eutectic hard-soldering temperature. Unfortunately, aluminium is susceptible to electromigration — transport of conductor material in the direction of electron flow — at the high current densities required (approaching 10^6 A/cm²).

When aluminium metallisation is used, the choice of a suitable metal for the connecting wires becomes difficult. Aluminium wires work-harden as the result of thermally-induced stresses between wire and plastic package, and may eventually fracture. Gold wire does not work harden, but gold combines with aluminium at elevated temperatures to form brittle intermetallic compounds that weaken the wire bond to the point where it is fractured by thermal stresses. The rate of formation of these compounds depends on temperature, according to Arrhenius' Law; the useful life of devices using gold wires with aluminium metallisation is about 7 000 h at a junction temperature of 150 °C.

These difficulties would be resolved by the use of gold metallisation. Gold is far less susceptible to electromigration, does not corrode, and makes excellent bonds to gold wires. However, gold does not adhere well to silicon dioxide and diffuses into the silicon chip at the eutectic bonding temperature, reducing h_{FE} and V_{EBO} .

It was to make gold usable as chip metallisation that the titanium-gold barrier-layer system described in Ref. 1 was developed. A layer of titanium is deposited onto the chip first to act as a barrier to attack by the gold. Titanium adheres well to silicon and silicon dioxide and does not diffuse into silicon at the eutectic soldering temperature. A layer of gold, which adheres well to titanium, is then deposited to act as the surface metallisation.

It was found that, with the single titanium barrier layer, failures occurred due to the diffusion of gold through the barrier layer: although useful lives of more

than 10^5 h at a junction temperature of 150 °C could be obtained. For applications requiring the highest reliability and useful life, an additional barrier layer of platinum is deposited between the titanium and gold layers. This is the system used for the BDW55 series of SOT-32 ultra-reliable medium power transistors.

Wires, bonds and encapsulation

For the reasons mentioned in the previous section, gold wires, 50 μ m in diameter, are used in the BDW55 series for chip to lead-frame connections of base and emitter. Attachment is by ultrasonic wedge bonds, a method capable of good control and, consequently, excellent quality.

The choice of encapsulant lies, in practice, between silicone plastic and epoxy. Since the encapsulant is in intimate contact with the electrical components of the device, it is important that it be free from impurities that might cause leakage and corrosion. Although the choice is not clear cut, an advanced silicone plastic is used for the package of the BDW55 series devices. With epoxies there is always the chance of some unreacted component remaining after curing.

The complete devices

Figure 2 shows the principal constructional features of the BDW55 series devices as discussed in the foregoing sections. All exposed surfaces within the package are either of gold or passivated silicon: both are extremely resistant to the effects of moisture and impurities. The function of the package is thus reduced largely to one of mechanical protection only, and hermeticity is reduced to very secondary importance.

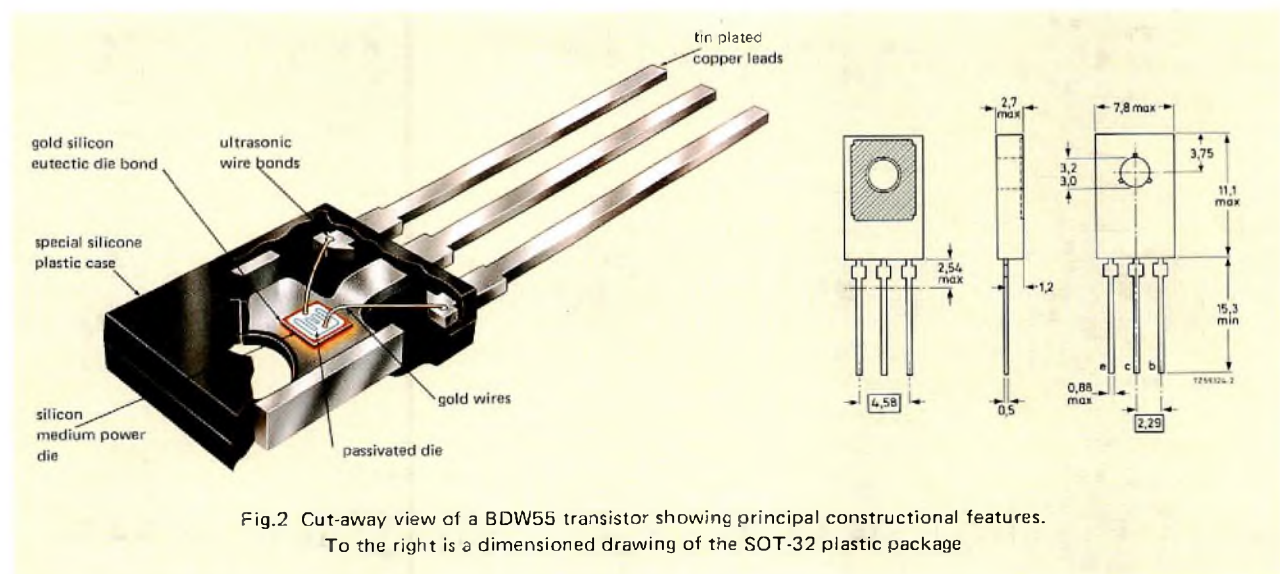


Fig.2 Cut-away view of a BDW55 transistor showing principal constructional features. To the right is a dimensioned drawing of the SOT-32 plastic package

RELIABILITY FUNDAMENTALS

Definitions

The systematic study and comparison of reliability performance requires the adoption of agreed definitions and quantitative descriptions (Ref.2). Those in general use are given in IEC Publication No. 271; they are used here. Those definitions that apply to the BDW55 programme are:

Reliability, general: The ability of an item to perform a required function under stated conditions for a stated period of time.

Failure rate, observed: The ratio of the total number of failures in a single population to the total cumulative observed time on that population.

Failure: The termination of the ability of an item to perform its required function.

A number of types and degrees of failure are defined:

Complete failure: Failures resulting from deviations in characteristic(s) beyond specified limits such as to cause a complete lack of the required function.

Partial failure: Failures resulting from deviations in characteristic(s) beyond specified limits but not such as to cause a complete lack of the required function.

Partial failures are often divided into Major and Minor Partial Failures to facilitate study of the deviation process.

For reliability measurement purposes, both 'required function' and 'stated conditions' are defined with respect to the published characteristics and ratings. However, for the BDW55 series, one purpose of the test programme was to verify and finalise the design ratings for the devices.

Reliability characteristics

Unfortunately, semiconductor devices do fail in service, a property they share with most other components. Observation of a batch of devices operating under the same conditions reveals that the incidence of failure varies with time. From the moment of switch-on the failure rate decreases, it remains constant for a time, and then rises again. This behaviour generates the familiar bathtub curve of Fig. 3.

Investigation of failures yields causes that divide naturally into two categories: failures due to faulty manufacture, and failures due to some wearout mechanism inherent in the design or construction of the device. The premature failures due to faulty manufacture are generally termed early or workmanship failures.

Thus, the curve of Fig. 3 can be considered to be the resultant of the falling early-failure-rate curve and the rising wearout-failure-rate curve, Fig. 4.

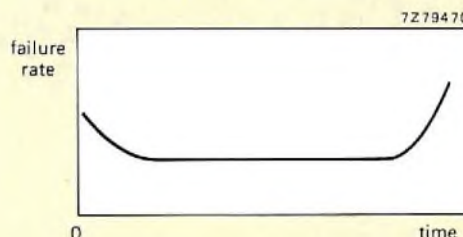


Fig.3 Variation of failure rate with time for a batch of devices operating from new: the familiar bathtub curve

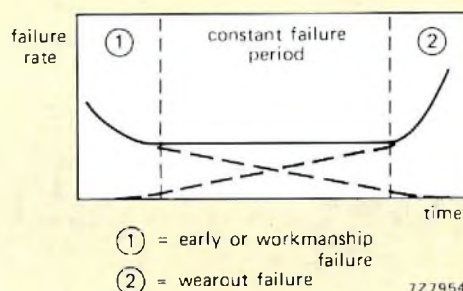


Fig.4 The bathtub curve reflects the falling incidence of early failures and the rising incidence of wearout failures

Measuring reliability

Reliability R is defined quantitatively as the probability that a device from a batch of devices having an observed failure rate λ will continue to function for a time t :

$$R = \exp(-\lambda t).$$

It is assumed that λ remains constant during period t and that the device operates under the same conditions as those under which the failure rate was observed.

Established, production devices are generally tested at one or more Absolute Maximum ratings. This ensures that the device reliability is fully explored and that the maximum of data is obtained in a test of practical duration. Testing at values greater than the ratings may yield results that cannot be directly related to Absolute Maximum conditions, by causing premature failure in sound devices.

A new device design, such as the BDW55, must be evaluated at a variety of stress levels. This is especially important where, as in this case, the device is required to be of exceptional reliability. Moreover, the results obtained from such testing can be used to make preliminary predictions of the effect of derating the device in service to obtain greater reliability.

TESTS: METHODS, CONDITIONS AND PURPOSES

The programme of tests carried out on the BDW55 transistor was designed to ensure that the device would perform its required function with exceptional reliability. The programme had four particular aims:

- to identify the wearout mechanism that determines end of useful life;
- to estimate the effect of derating on useful life;
- to measure device stability as a function of operating conditions;
- to establish a satisfactory burn-in or screening procedure to reduce the incidence of early failures in critical applications.

Storage

Samples of BDW55 transistors were stored at elevated temperatures to explore the time and temperature dependence of the following failure modes:

- open wire bonds to chip or lead frame;
- degradation of bond between chip and lead frame;
- reduction of h_{FE} due to diffusion of gold through the titanium and platinum barrier layers.

Encapsulated devices were tested as follows:

storage temperature (°C):	100	150	175	200	225
number tested:	110	110	110	60	35

Since the plastic encapsulant deteriorates at higher temperatures, further testing was carried out on unencapsulated devices:

storage temperature (°C):	250	300	350
number tested:	35	60	40

Current

Samples of BDW55 transistors were operated, bottomed, at high currents to explore the relationship between current density and time for failures due to electromigration. The following combinations of current, junction temperature and sample size were used:

I_E (A):	0.7	1	1.5	2
T_j (°C):	100	150	150	160
number tested:	110	110	60	35

Dissipation

To investigate the reliability behaviour of the BDW55 under moderate operating conditions, a batch of 110 devices was tested at $T_{amb} = 25^\circ\text{C}$; $P_{tot} = 1250\text{ mW}$; $I_E = 44\text{ mA}$ and $T_j = 110^\circ\text{C}$.

Cut-off

Prolonged operation under cut-off conditions yields information about the state and stability of the chip surface. All testing was carried out at $V_{CE} = 44\text{ V}$ and $V_{BE} = -1\text{ V}$:

T_{amb} (°C):	100	150
number tested:	110	110

Further testing was also carried out at ambient temperatures of 175°C and 200°C .

Thermal (power) cycling

Thermal cycling can induce thermal fatigue in wire bonds to chip and lead frame, and in the chip to lead-frame bond. To determine the relationship between the number of thermal cycles and junction temperature required to induce thermal fatigue, samples of the BDW55 were subjected to power cycling, 2½ minutes on, 2½ minutes off, at an ambient temperature of 25°C :

power (W):	3	2.75	2.5	2.25
T_j peak* (°C):	294	272	250	228
number tested:	20	30	40	50

power (W):	2	1.75	1.5	1.25
T_j peak* (°C):	206	183	161	139
number tested:	60	70	80	90

* average value.

Wet testing

The effect of moisture is an important consideration with plastic-encapsulated devices. Accordingly, samples of the BDW55 were exposed to a variety of combinations of temperature, pressure and relative humidity. In some cases, identical tests were carried out using both encapsulated and unencapsulated devices. In addition, similar tests were carried out with and without applied voltage in order to compare the effect on reliability.

Boiling water. A total of 44 devices were immersed continuously in boiling water at 100°C . Of these, 25 were encapsulated and 19 unencapsulated.

Tropical conditions. The following tropical conditions were applied continuously:

relative humidity (%):	70	95	85
temperature (°C):	55	55	85
number tested:	30	50	30

An additional 20 devices were exposed to cyclic tropical conditions: 16 h at 55 °C followed by 8 h at 25 °C with a peak relative humidity of 95 to 100% (IEC68-2-4 Test Da).

Wet cut-off. Samples of the BDW55 were operated at $V_{CE} = 44$ V and $V_{BE} = -1$ V, continuously applied:

temperature (°C):	55	55	85	123*
relative humidity (%):	70	95	85	100
number tested:	110	110	60	100**

* At a pressure of 122 kPa (1,2 atmospheres).

** Comprising 50 encapsulated and 50 unencapsulated.

Mechanical and climatic testing

The ruggedness of the BDW55 has been proved by the following mechanical and climatic tests.

Temperature cycling. To test the reaction of the device to rapid changes of temperature, 50 loose devices, and 50 devices mounted on a heatsink (using the recommended method of mounting) were cycled between +150 °C and -65 °C. The devices were exposed to both temperatures for 30 minute periods, with a transition time of 5 minutes between the extremes.

Mounting test. Using the mounting method recommended in the published data, 10 samples of the BDW55 were each mounted on and removed from a heatsink 10 times.

Applied force. The following tests were carried out in accordance with the requirement of IEC Publication No. 68:

- lead pull; (IEC68-2-21 Test Ua)
- lead bend; (IEC68-2-21 Test Ub)
- lead torque; (IEC68-2-21 Test Ud)
- drop; (IEC68-2-32 Test Ed)
- shock; (IEC68-2-27 Test Ea)
- vibration fatigue; (IEC68-2-6 Test F (B2))
- variable frequency vibration; (IEC68-2-6 Test F (B4)).

Solderability. Solderability tests according to IEC 68:

- solderability as new; (IEC68-2-20 Test T)
- solderability after 4 weeks tropical testing; (IEC68-2-4 Test Da).

Heat resistance. Samples of BDW55 transistors were given a simulated soldering treatment, 300 °C for 11 s, followed by 5 temperature cycles between -65 °C and +150 °C, as above.

Salt spray test. A total of 19 samples of BDW55 transistors, 10 encapsulated, 9 unencapsulated, were exposed to a spray of salt (NaCl) solution; (IEC68-2-11 Test Ka).

Failure criteria

To monitor the progress of the life tests, such device characteristics were regularly measured as would both determine whether the device was capable of fulfilling its design function and indicate the cause of any failure. These characteristics are listed in Table 2, together with the type of failure that they indicate.

The ΔV_{BE} measurement is that carried out on all production devices with eutectic chip bonding, as described earlier. For the BDW55, a 100 mA emitter-current pulse as shown in Fig. 5 is applied. During the $V_{CE} = 10$ V part of the pulse, the value of V_{BE} is measured as a reference. Immediately on cessation of the $V_{CE} = 40$ V part of the pulse, V_{BE} is again measured. The difference between the two values is ΔV_{BE} which is proportional to the increase in junction temperature and, consequently, to the junction-to-ambient thermal resistance. This thermal resistance is largely determined by the quality of the chip-to-lead-frame bond.

Limits were set on the measured characteristics to define Minor and Major Partial, and Complete Failures. These limits are given in Table 3.

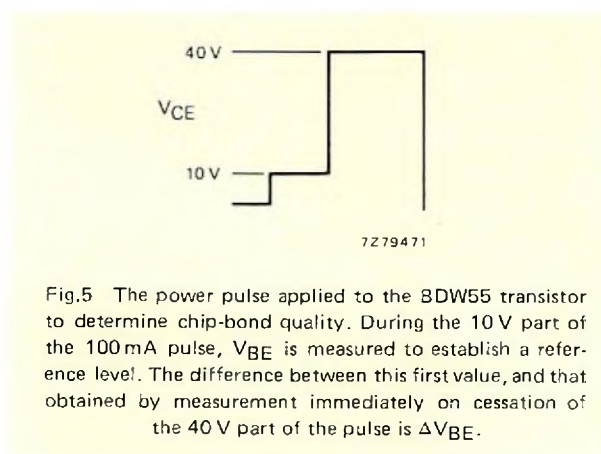


Fig.5 The power pulse applied to the BDW55 transistor to determine chip-bond quality. During the 10 V part of the 100 mA pulse, V_{BE} is measured to establish a reference level. The difference between this first value, and that obtained by measurement immediately on cessation of the 40 V part of the pulse is ΔV_{BE} .

TABLE 2
Measurements made to detect failures during life tests; measurement conditions and purpose

characteristic	description	measurement conditions	failure mode indicated
V_{BCO}	forward voltage of base-collector diode	$I_{BC} = 1 \text{ A}$, $I_E = 0$, $T_{amb} = 25^\circ\text{C}$.	high resistance of chip or wire bonds
V_{BEO}	forward voltage of base-emitter diode	$I_{BE} = 1 \text{ A}$, $I_C = 0$, $T_{amb} = 25^\circ\text{C}$.	high resistance of wire bonds
flutter	intermittent operation	$I_E = 1.5 \text{ A}$, $f = 100 \text{ Hz}$, $T_{amb} = 25^\circ\text{C}$.	intermittent wire bonds
$V_{CE \text{ sat}}$	collector-emitter saturation voltage	$I_C = 500 \text{ mA}$, $I_B = 120 \text{ mA}$, $T_{amb} = 25^\circ\text{C}$.	high resistance of chip or emitter-wire bonds
I_B (1)	base current required for a given collector current	$I_E = 5 \text{ mA}$, $V_{CB} = 2 \text{ V}$, $T_{amb} = 25^\circ\text{C}$.	reduction of h_{FE}
I_B (2)	(as above)	$I_E = 50 \text{ mA}$, $V_{CB} = 2 \text{ V}$, $T_{amb} = 25^\circ\text{C}$.	reduction of h_{FE}
I_B (3)	(as above)	$I_E = 150 \text{ mA}$, $V_{CB} = 2 \text{ V}$, $T_{amb} = 25^\circ\text{C}$.	reduction of h_{FE}
I_{CBO}	leakage current of collector-base diode	$V_{CB} = 30 \text{ V}$, $I_E = 0$, $T_{amb} = 25^\circ\text{C}$.	contamination of chip, unstable chip surface
I_{EBO}	leakage current of emitter-base diode	$V_{EB} = 5 \text{ V}$, $I_C = 0$, $T_{amb} = 25^\circ\text{C}$.	contamination of chip, unstable chip surface
ΔV_{BE}	fast thermal resistance measurement	see Fig. 5, $T_{amb} = 25^\circ\text{C}$	deterioration of chip bond

TABLE 3
Failure criteria for BDW55 transistors

characteristic	failure criteria		
	Minor Partial	Major Partial	Complete
V_{BCO}	250 mV increase	> 1250 mV	> 2000 mV
V_{BEO}	250 mV increase	> 1250 mV	> 2000 mV
flutter			open/short
$V_{CE \text{ sat}}$		50 mV change	
I_B (1)	192 μA		
I_B (3)	0.93 to 3.6 mA		
I_{CBO}	> 10 μA	> 20 μA	> 100 μA
I_{EBO}	> 10 μA	> 20 μA	> 100 μA
ΔV_{BE}			50% increase

TEST RESULTS

All failures recorded during the BDW55 test programme were Complete Failures as defined in Table 3. No Partial Failures were observed.

Storage

No Complete Failures occurred in the encapsulated devices after 60 weeks (10 080 h) at temperatures between 100 °C and 225 °C.

Of the unencapsulated devices tested, none failed in the 36 weeks (6048 h) of the 250 °C test. The 300 °C and 350 °C tests both resulted in failures after two weeks (336 h). These failures were due to the gold plating lifting off the lead frame. However, the wires remained attached to the plating.

Current

After four weeks (672 h) of the 0.7 A current test, two failures were recorded. No failures occurred in the remainder of the 60 weeks of the test. No failures occurred after 60 weeks testing at 1 A, 1.5 A, or 2 A.

The cause of the two failures recorded in the 0.7 A test was found to be overheating due to a short circuit caused by a particle of gold on the chip metallisation pattern.

Dissipation

After six weeks, one failure occurred in the dissipation test. No other failures were recorded during the rest of the 60 week duration of the test.

The failure observed was found to be due to a short circuit in the chip metallisation.

Cut-off

After four weeks at $T_{amb} = 100\text{ }^{\circ}\text{C}$, the cut-off test resulted in two failures. A further failure occurred after six weeks. No further failures occurred during the remainder of the 60 week test. No failures were recorded during the 60 weeks testing at $T_{amb} = 150\text{ }^{\circ}\text{C}$.

The first two failures recorded in the $T_{amb} = 100\text{ }^{\circ}\text{C}$ test were found to be due to short circuits in the chip metallisation. The failure that occurred after six weeks was due to a cracked chip; examination showed that there was probably a crack at the edge of the chip at the onset of the test.

Thermal (power) cycling

No failures occurred in the 1.25 W test after 10 000 h, in the 1.5 W test after 8000 h, or in the 1.75 W test after

10 000 h. No failures occurred due to open or short-circuit devices during the 2 W test, but there was a general increase in the value of ΔV_{BE} . The tests at powers greater than 2 W resulted in progressively early end-of-life failures due to deterioration of the chip bond.

Wet testing

Tropical conditons. No failures resulted from the 10 000 h of each of the tropical tests.

Boiling water. No failures occurred during 500 h immersion in boiling water of both encapsulated and unencapsulated devices.

Wet cut-off. After 60 weeks of the 55 °C, 70% relative humidity test, no failures were observed. During the 55 °C, 95% relative humidity test, one failure occurred after 24 weeks (4032 h), a further two failures occurred after 30 weeks (5040 h), and a further two after the full 60 weeks. One failure occurred in the 85 °C, 85% relative humidity test after two weeks. All these failures were found to be due to a short circuit in the gold metallisation of the chip.

After 40 h of the 123 °C, 100% relative humidity test, no failures were recorded. One failure occurred after 48 h; after 11 days (264 h), a total of 18 devices had failed. All failures were due to high leakage current. Analysis showed that the device surfaces were contaminated, mainly with copper.

No difference was apparent between the performance of encapsulated and unencapsulated devices.

Mechanical and climatic testing

Temperature cycling. During the 500 cycles of this test, one failure was recorded after 10 cycles in the loose devices, but no further failures occurred. No failures were recorded among the mounted devices in 500 test cycles. The one failure was due to shorting of the gold metallisation pattern of the chip.

Mounting test. No failures.

Applied force. No failures.

Solderability. All 60 new devices passed the solderability test. After four weeks in a tropical environment, 53 out of 60 devices passed.

Heat resistance. No failures.

Salt spray test. Encapsulated samples were sprayed with salt (NaCl) solution for 500 h. One failure was recorded due to high leakage current. The unencapsulated devices were sprayed for 200 h. No failures were recorded.

STABILITY

The absence of Minor or Major Partial Failures attests the extreme stability of the BDW55 during all life tests.

Storage

Bond resistance and leakage currents remained stable during all storage tests. Some variation in the base current required for a given collector current was observed: this is an indication of the stability of h_{FE} . Figure 6 shows how the average value of I_B for $I_C = 5\text{ mA}$ varied during the 10 000 h of the various tests. The maximum change of I_B for any given device observed during these tests was 20%. Figure 7 shows the average value of I_B for $I_C = 150\text{ mA}$ during the storage tests. The variations of I_B for $I_C = 50\text{ mA}$ were intermediate between those of Figs 6 and 7.

Current

Stability during the current tests was also good. Both bond resistance and leakage currents remained stable. The stability of h_{FE} was similar to that observed during

the storage tests; this is shown in Fig. 8, which shows the average values of I_B for $I_C = 50\text{ mA}$. The pattern of change of I_B for $I_C = 5\text{ mA}$ and 150 mA was similar to that for $I_C = 50\text{ mA}$.

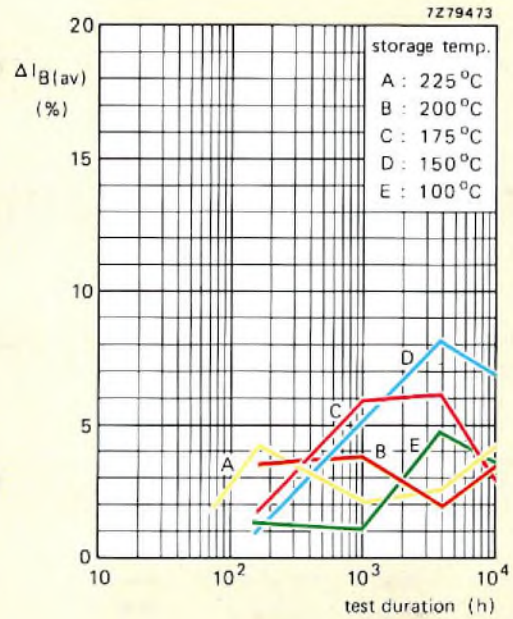


Fig.7 The change in the average values of I_B for $I_C = 150\text{ mA}$ during the various storage tests

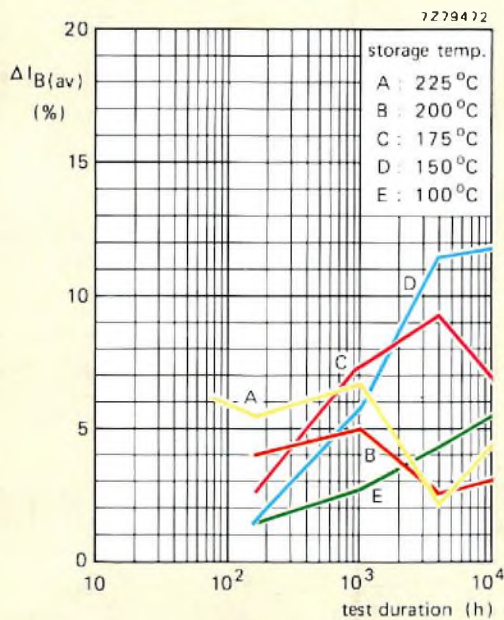


Fig.6 The change in the average values of I_B for $I_C = 5\text{ mA}$ during the various storage tests

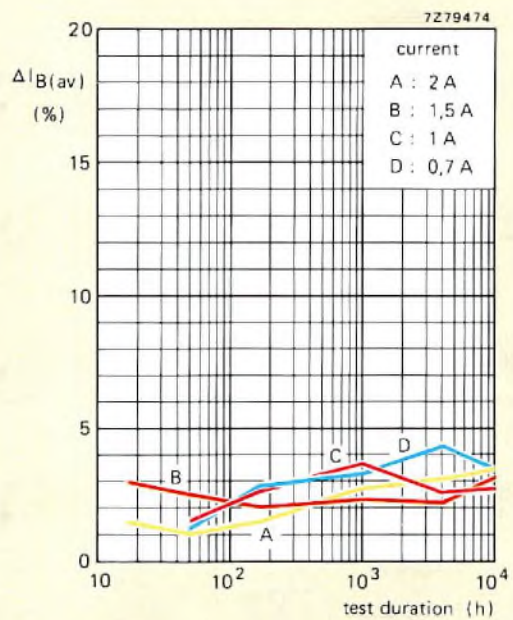


Fig.8 The change in the average values of I_B for $I_C = 50\text{ mA}$ during the current tests

The maximum variation observed in any one device was 25%; this occurred for $I_C = 50\text{ mA}$ during the 2 A test.

Figure 9 shows the distribution of I_B values for $I_C = 50\text{ mA}$ before and after 10 000 h operation at 1 A.

Dissipation

Bond resistance, leakage currents and h_{FE} all remained stable during the dissipation test.

Cut-off

Bond resistance remained stable; leakage current remained below $1\text{ }\mu\text{A}$ after 10 000 h testing at $100\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$. The distribution of h_{FE} varied little throughout all cut-off tests.

Thermal (power) cycling

Leakage current and bond resistance both remained stable. There was little variation in h_{FE} ; Fig. 10 shows the distribution of I_B for $I_C = 5\text{ mA}$ before and after 10 000 h (120 000 power cycles) at $P_{tot} = 1.75\text{ W}$. This was the largest change in the I_B distribution pattern that occurred during the thermal cycling tests.

Wet testing

Tropical conditions and boiling water. Figure 11 shows the variation of the average value of I_{CBO} during the tropical and boiling water tests. Both encapsulated and unencapsulated devices were immersed in boiling water for 500 h.

The value of h_{FE} was also comparatively unaffected by exposure to moisture. This can be seen in Fig. 12 where the average change in I_B for $I_C = 5\text{ mA}$ is plotted against test duration. The maximum average deviation does not exceed 13%.

Figure 13 shows the change in distribution of I_B for $I_C = 5\text{ mA}$ during the 500 h of the boiling water immersion test for encapsulated and unencapsulated devices. It is apparent that there is little difference in the effect of boiling water on devices with and without encapsulation.

Wet cut-off. The average value of I_{CBO} during the wet cut-off tests is given in Fig. 14. Generally, increase in leakage current was small, well below the Minor Partial Failure level of $10\text{ }\mu\text{A}$. The largest increase occurred in the $123\text{ }^\circ\text{C}$, 100% relative humidity test. This was found to be due to contamination of the chip surface.

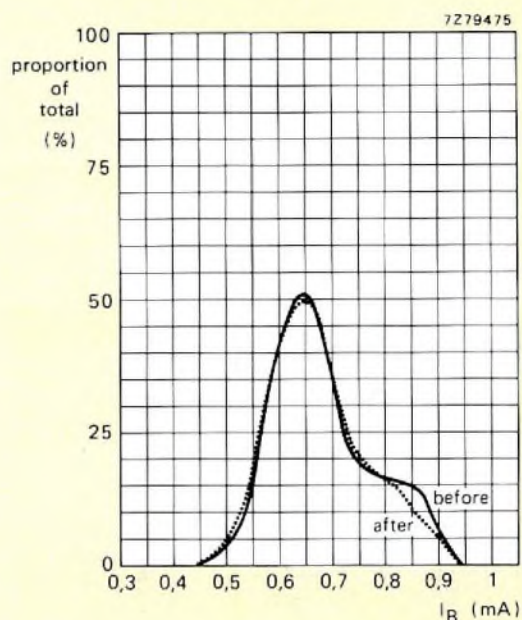


Fig.9 Distribution of values of I_B for $I_C = 50\text{ mA}$ before and after the 1 A current test

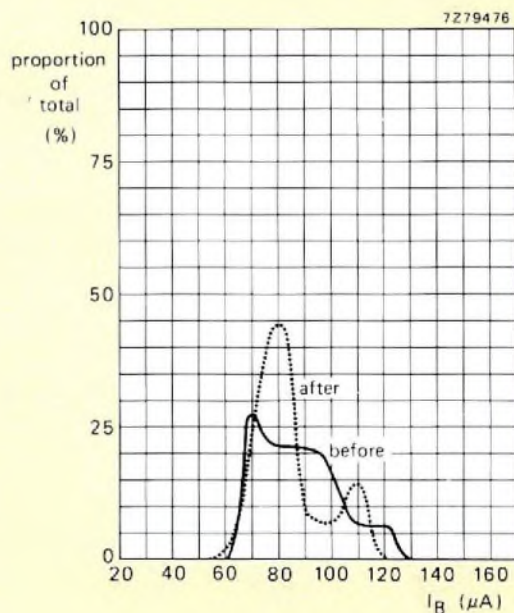


Fig.10 Distribution of values of I_B for $I_C = 5\text{ mA}$ before and after the $P_{tot} = 1.75\text{ W}$ thermal (power) cycling test

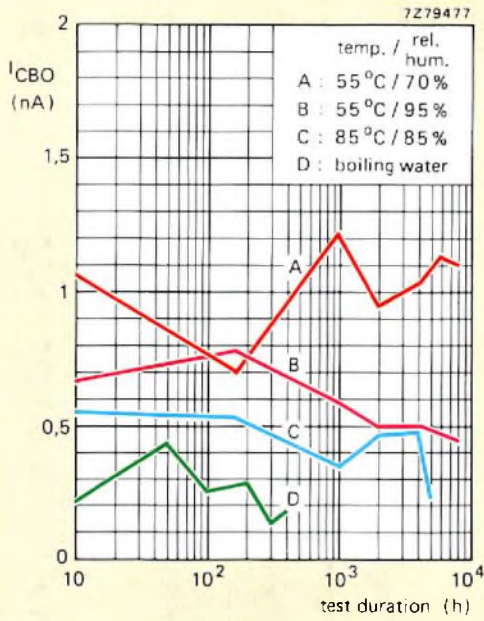


Fig.11 Average I_{CBO} measured at 30 V during the various wet tests

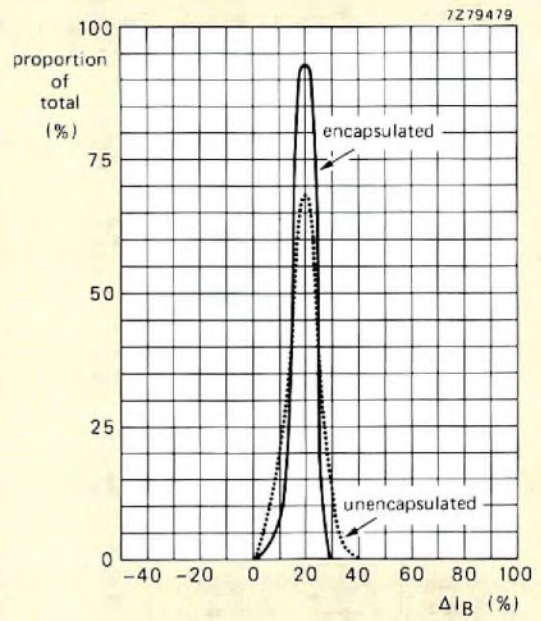


Fig.13 The change in distribution of the change in values of I_B for $I_C = 5 \text{ mA}$ after the 500 h immersion in boiling water of encapsulated and unencapsulated devices.

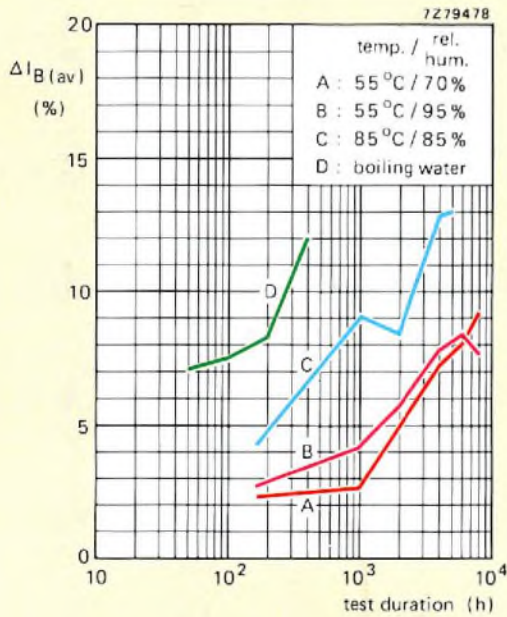


Fig.12 The change in the average values of I_B for $I_C = 5 \text{ mA}$ during the various wet tests.

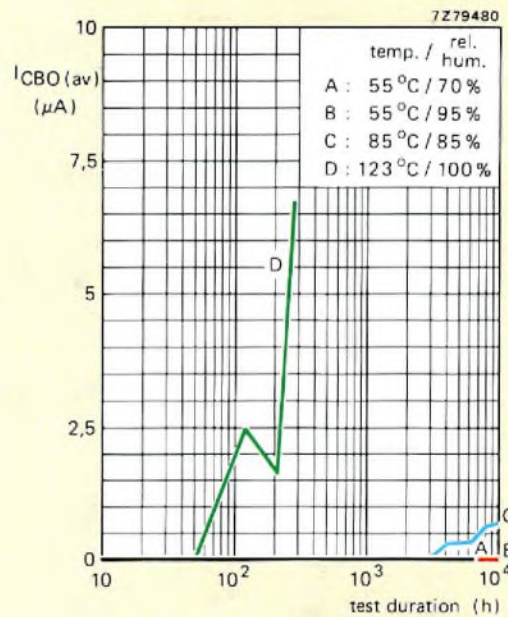


Fig.14 The variation in the average values of I_{CBO} measured at 30 V during the wet cut-off tests

A similar pattern was observed in the variation of h_{FE} during the wet-cut-off tests. Figure 15 shows the average change in I_B for $I_C = 5 \text{ mA}$. Again, the largest change occurred during the 123°C , 100% relative humidity test due to contamination.

Mechanical and climatic tests

The BDW55 proved stable during all mechanical and climatic tests.

RESULTS: SUMMARY AND ANALYSIS

The reliability of the BDW55 transistor design has been explored by means of about 16 million device-hours testing under conditions that include operation at well in excess of design ratings. The results have:

- finalised the design ratings;
- established the principal cause of early failures;
- determined the end-of-life failure mechanism;
- shown that the design is highly resistant to the effects of moisture;
- provided an indication of the in-service reliability of the device.

Design ratings

The ratings of the BDW55 series, summarised in Table 1, are as designed with the exception of the maximum junction temperature. This was designed to be 150°C . As a result of the test programme, the maximum junction temperature for production devices was fixed at 175°C . Although the test results indicate that the BDW55 will operate reliably at even higher temperatures, the practical value is limited by the dissociation temperature of the plastic encapsulation.

Early failures and burn in

All early failures were found to be due to particles of gold bridging the base and emitter metallisation tracks on the chip surface. The observed failure rate for this type of early-failure mechanism is shown as a function of time in Fig. 16.

Precutionary measures, including the insertion of an additional 100% visual inspection into the production process for the BDW55, are expected to virtually eliminate failures due to gold particles. This would greatly reduce the need for burn in.

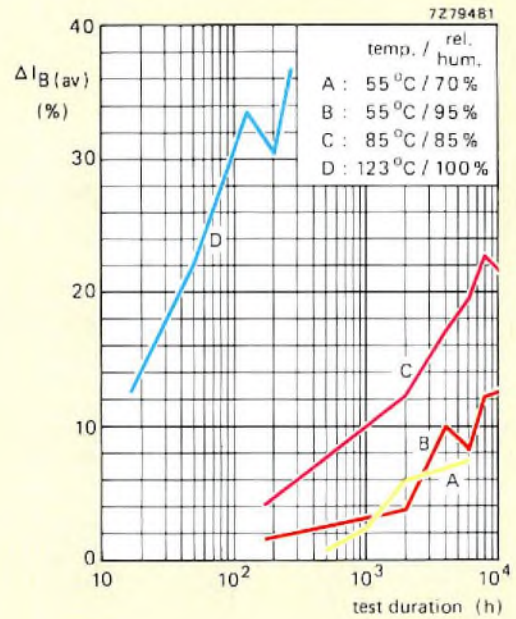


Fig.15 The change in the average values of I_B for $I_C = 5 \text{ mA}$ during the wet cut-off tests

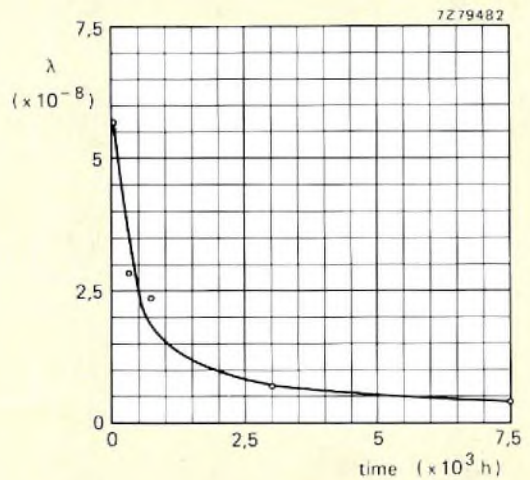


Fig.16 The incidence of early failures due to shorting of the chip metallisation by gold particles as a function of time

Wearout

Only one end-of-life failure mechanism has been isolated: deterioration of the chip-to-lead-frame bond. This bond is, nevertheless, extremely robust. At a peak junction temperature of 175°C (1.5 W dissipation in free air at an ambient temperature of 25°C), the useful life should be well in excess of 500 000 cycles, as shown by Fig. 17. Even at the extremely high confidence level of 97.5%, the life expectancy is over 150 000 cycles.

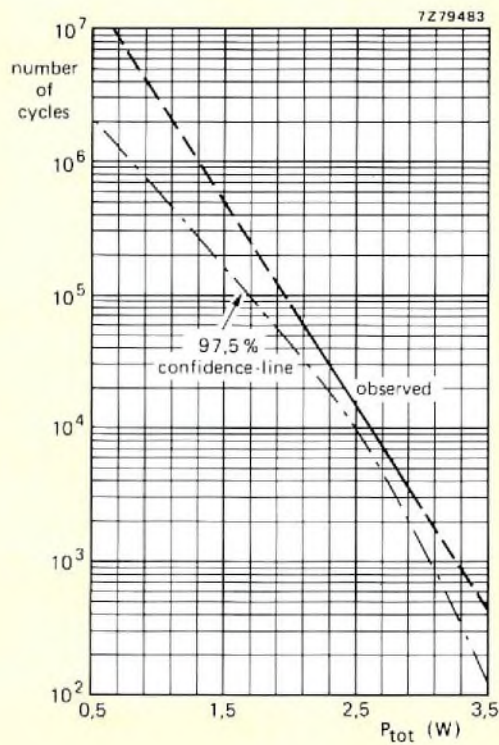


Fig.17 Useful life in number of power cycles as a function of power and junction temperature. Both observed and 97.5% confidence failure curves are given.

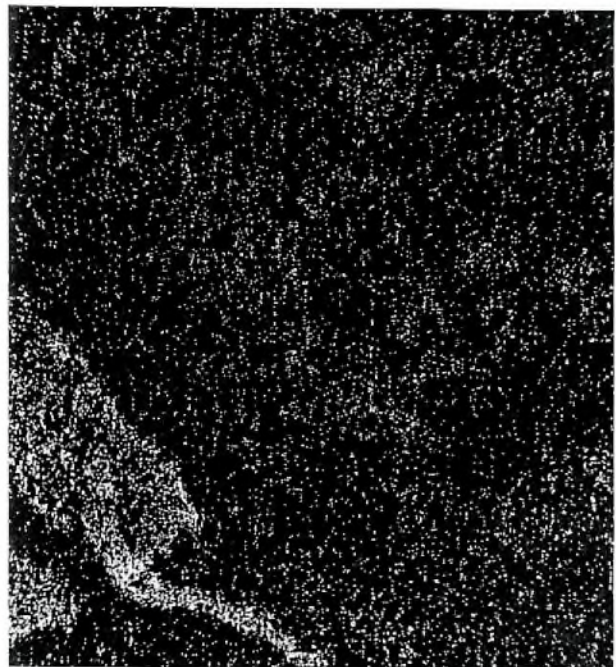
Moisture

It is clear from the results that *pure water* has no effect on the BDW55. Even salt spray does not result in significant increase in leakage after 200 h on an unencapsulated device. This vindicates the design philosophy which aimed at reducing the function of the plastic encapsulant to that of mechanical holding and protection only. During the long-period wet cut-off tests, the only failures induced were due to shorting of the chip metalisation, an early failure mechanism which will be virtually absent in production versions. No failures resulted from tropical storage, or storage in boiling water, even of unencapsulated devices.

Failures induced in the 123 °C, 100% relative humidity, cut-off tests were caused by contamination, not by corrosion. This is demonstrated in Fig.18 where a scanning electron photomicrograph of the corner of a BDW55 that failed after 16h of this test due to high leakage is compared with the same view of the device, but scanned for copper.



(a)



(b)

Fig.18 (a) Scanning electron microscope photograph showing part of a BDW55 transistor after 16 days at 123 °C and 100% relative humidity. The device failed due to high leakage. (b) The same view, but scanned for copper. It can be seen that chip and bond wires are contaminated.

Reliability in service

Observed failure rate. An indication of the failure rate to be expected in normal service can be obtained from the results of the test programme. A total of 13.7 million device-hours testing has been carried out at, or about, the Absolute Maximum Ratings established for production devices. In the course of these tests, only five failures were recorded: an observed failure rate of 0.036%/1000 h. However, of these five failures, four were early failures which will be largely eliminated by the additional stage of inspection. Thus, if only 75% of potential early failures are removed by this inspection, the observed failure rate would fall to about 0.0015%/1000 h.

Maintaining reliability. This degree of reliability will be maintained in production by regularly subjecting samples of BDW55 series transistors drawn from production to a similar programme of tests to that described here. Sampling will, as usual, be according to MIL-STD-105D. The results from these tests will provide further evidence of device reliability, but that is not their main purpose. These results will be fed back to correct deviations in production conditions and methods, and to make minor improvements in device design, so gradually improving on the already excellent reliability.

CONCLUSION

It is evident that the combination of titanium-platinum-gold metallisation and gold-silicon eutectic chip bonding has made possible a major advance in the design of power semiconductor devices. By providing a chip surface,

consisting either of gold or passivating glass, that is virtually immune to corrosion, the problem of the hermeticity of plastic packages has been solved. For damage to occur to devices using the BDW55 technology, contaminant as well as moisture must be present. However, these contaminants would be as damaging to other circuit components — printed circuit boards, wires, devices, leads — as to the transistors themselves.

The ultrasonic wedge bonds used with 50 μm diameter gold wire have proved exceptionally reliable. Of a total of 2600 devices with four bonds per device, tested for 15.5 million device hours, the observed failure rate per bond was, with 60% confidence, better than $15 \times 10^{-9}/\text{h}$.

The eutectic chip bonds proved almost immune to the effects of thermal (power) cycling. They form the final link in the chain of technology that makes the BDW55 and BDW56 series of power transistors the most advanced now available.

The test programme reported here was carried out on the BDW55. A similar programme carried out later on its p-n-p complement, the BDW56, confirmed that the results and conclusions apply equally to that transistor.

References

1. 1973. Improving the reliability of semiconductor devices — Titanium-gold metallization. Philips' Product Information No. 57.
2. DRYDEN, M. H. 1976. Design for reliability. MTC 13: 395-432 (No. 130).
3. LEENDERS, W., et al. 1974. Titanium-gold: high-reliability transistor metallization. Electronic Applications Bulletin 32, 70-80, (No. 2).

Application note

TDA1011: versatile 2 to 6 W audio amplifier

There is an extensive market for audio amplifiers with power outputs between 2 W and 6 W for use in battery and mains-powered domestic entertainment equipment. For this class of equipment, limited space and economic considerations dictate the use of integrated audio circuits which are easy to heatsink and require few peripheral components. Unfortunately, the conventional power DIL integrated circuit package is expensive and difficult to mount. It also occupies a relatively large area of the printed-wiring board, is difficult to attach to a heatsink and, in some cases, it conducts heat onto the printed-wiring board.

For the foregoing reasons we have encapsulated our new 2 W to 6 W audio amplifier type TDA1011 in a single-in-line (SIL) plastic package. The SIL package has a single row of nine pins along one edge and incorporates a cooling tab which extends from the other edge. The main advantages of this type of construction are:

- The single row of connecting pins simplifies insertion, allows the circuit to be positioned anywhere on the printed-wiring board, even near the edge, and facilitates direct routing of the copper tracks.
- It is very simple and inexpensive to fix to a heatsink.
- When the circuit is used without a heatsink, the thermal resistance between the crystal and ambient is $60^{\circ}\text{C}/\text{W}$. This value can be reduced for the higher power applications by extending the area of the

cooling tab with a heatsink (R_{th} between crystal and cooling tab = $12^{\circ}\text{C}/\text{W}$). The cooling tab is internally connected to the substrate of the circuit so that insulation is not usually needed between the cooling tab and the heatsink.

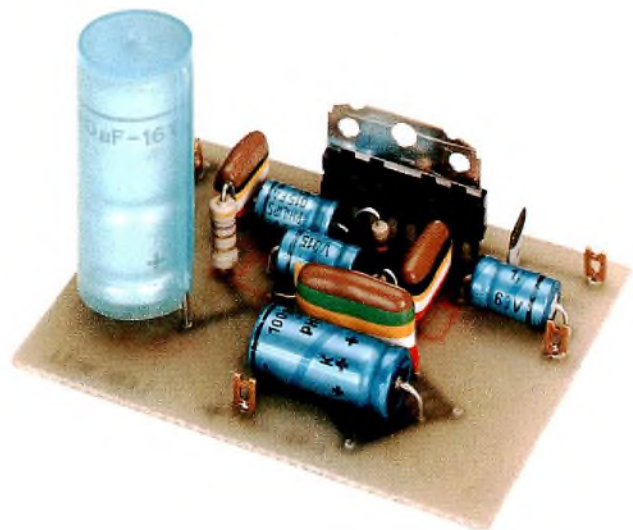


Fig.1 A 9 V battery-powered 2.2 W audio amplifier using the TDA1011

This note is based on a laboratory report. Requests for additional data should mention the title of the note, the issue of E.C.&A. in which it appeared, and the nature of the applicant's interest.

APPLICATIONS

The TDA1011 in battery-powered equipment

The basic circuit of the TDA1011 connected as an audio amplifier for 6 V or 9 V battery operation is given in

Fig.2. The performance figures for the circuit are given in Table 1. The figures apply for an input frequency of 1 kHz and are given for both the nominal battery voltages and the end of life voltages.* Heatsinks are not required for these circuits.

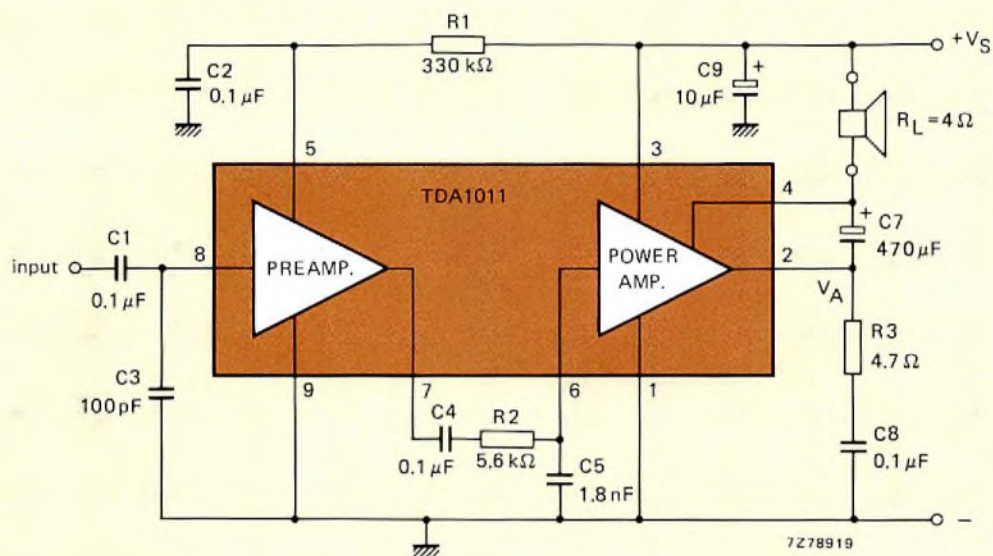


Fig.2 Basic circuit for battery-powered applications of the TDA1011

TABLE I
Performance of battery-powered circuits.

	6	3.6*	9	5.4*	Unit
Battery voltage:					V
Maximum power developed in $R_L = 4 \Omega$ ($d = 10\%$):	0.9	0.22	2.2	0.75	W
Distortion at $P_O = 0.5 P_{O \max}$:	0.32	0.45	0.35	0.5	%
Quiescent current:	10	7.5	12	9.5	mA
Input sensitivity for $P_O = 50 \text{ mW}$:			1.5		mV
Input sensitivity for $P_{O \max}$:	7.4	3.6	11.3	6.5	mV
Input impedance			200		k Ω
A-scale weighted S/N ratio ($P_O = 50 \text{ mW}$, $R_S = 0 \Omega$):			68		dB
-3 dB frequency response (ref. $0.5 P_{O \max}$ at 1 kHz):			100-16000		Hz

* A 1.5 V cell is considered to be exhausted when its terminal voltage drops to 0.75 V during operation. Under these conditions, the average voltage of the loaded and unloaded cell is 0.9 V.

The TDA1011 in mains-powered equipment

The basic circuit of the TDA1011 connected as an audio amplifier for mains-derived 12 V d.c. operation is given

in Fig.3. The performance figures for the circuit are given in Table 2. The figures apply for an input frequency of 1 kHz.

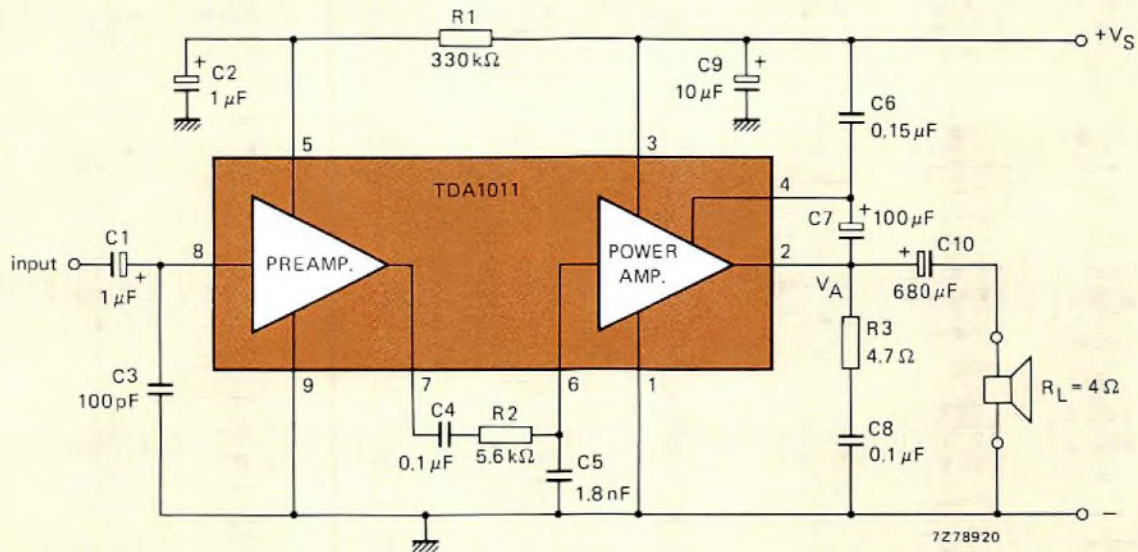
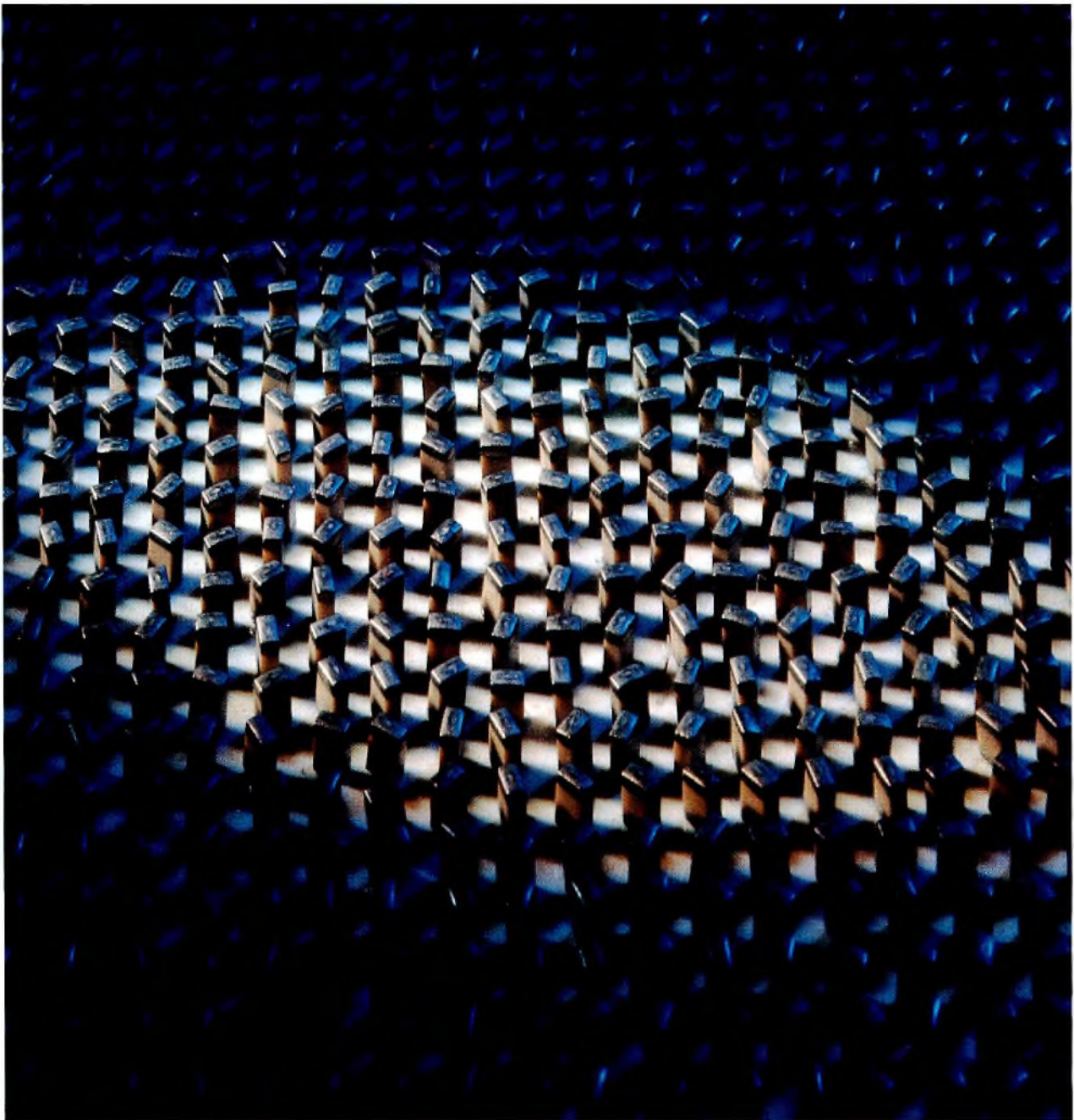


Fig.3 Basic circuit for mains-powered applications of the TDA1011

TABLE 2
Performance of mains-powered circuits.

	12	16	Unit
Supply voltage	12	16	V
Maximum power developed in R_L ($d = 10\%$):	3.8	6.2	W
Distortion at $P_O = 1$ W:	0.4	0.35	%
Quiescent current:	13.5	16	mA
Supply mid-point voltage at pin 2:	6	8.1	V
Maximum worst-case dissipation with sine-wave drive:	2.3	4	W
Overall voltage gain:		50	dB
Input sensitivity for $P_O = 1$ W:		6.5	mV
Input impedance:		200	k Ω
A-scale weighted S/N ratio at $P_O = 50$ mW;			
$R_S = 0 \Omega$:		68	dB
$R_S = 8.2$ k Ω :		60	dB
100 Hz supply voltage ripple rejection:		37	dB
-3 dB frequency response (ref. 1 W at 1 kHz):		90-16000	Hz
Minimum area of 1.5 mm flat bright aluminium heatsink ($T_{amb} = 45^\circ\text{C}$)	10	30	cm ²



Multilayer chip capacitors are extremely small — some are barely more than a cubic millimetre in volume — which makes them ideal for use in thick and thin film hybrid circuits for coupling, decoupling, and frequency discriminating applications such as in TV tuners, wrist watches, complex car radios, pacemakers and both professional and consumer products where space is at a premium.

These capacitors have palladium electrodes stacked alternately with layers of ceramic dielectric. With this form of construction, where alternate electrodes are connected together at each end, one multilayer chip capacitor is effectively many capacitors in parallel. Since parallel capacitances are additive, their use enables one to achieve the highest CV product per unit area available in the industry today.

Two types are offered: one using our dielectric material NPO for capacitances up to $0.01\ \mu\text{F}$ where high stability ($\pm 30\ \text{ppm}/^\circ\text{C}$) or a high Q factor is necessary; the other uses our K1800 dielectric material for capacitances up to $0.47\ \mu\text{F}$ for use where requirements are less severe. The temperature range for both types is -55 to $+125^\circ\text{C}$.

Multilayer chip capacitors are high technology products and their reliability is excellent.

Single-phase rectifier circuits with CR filters

Part 1 - Theory

A. LIEDERS

INTRODUCTION

The rectifier and CR filter combination seems, at first sight, to be a simple enough circuit. Mathematical analysis, however, quickly proves otherwise. The nature of the problem is summarised by Martin (Ref.1):

“The half-wave diode rectifier with RC filter is a common electronic circuit and one of the simplest in appearance. The appearance is misleading because it has proved to be an exceptionally difficult circuit to treat analytically. Indeed, as far as I know, there never has been a successful analysis of a practical circuit. Of course, certain hypothetical cases have been treated in nearly every text book, but the results obtained are of little practical use because the simplifying assumptions are not valid in practical circuits. The difficulty in treating the circuit is not one in technique, because it will be apparent later that the operation of the circuit can be outlined rather accurately. Instead, the problem is primarily one of the tedium in making graphical solutions of transcendental equations, performing numerous integrations, and so on.”

Later in his discussion, Martin writes:

“It is quite clear from the preceding analysis that it is possible to compute the various factors of interest in rectifiers with RC filters, but that it would be an extremely time-consuming proposition. Fortunately, a careful set of *experimental determinations* (author's italics) has been made by Schade and the results tabulated in a universal system of dimensionless parameters.”

Schade's original work may be found in Ref.2.

However, if one assumption is made, mathematical analysis becomes relatively simple. This assumption is that the filter capacitor charges and discharges linearly: an assumption that is fully justified, provided that the CR product of the filter network is much larger than the period of the mains-voltage waveform. Furthermore, even when the CR product of the filter network is not much larger than the period of the mains-voltage waveform, the use of this assumption yields results that correspond closely to the measured values.

An analysis on this basis was first made by Kammerloher (Ref.3), who investigated thermionic rectifier circuits. Unfortunately, not all the expressions needed were derived. In particular, the expression for repetitive peak forward current was omitted; this was apparently not so important with vacuum tube rectifiers. Also, it can be shown that Kammerloher's expression for the r.m.s. diode current is incorrect: it was derived from the active power consumed by the whole circuit, and not directly from the current flowing through the rectifier itself.

The nomograms given by Schade are valid for thermionic rectifiers, but attempts to adapt them to silicon rectifier circuits have not been completely successful (Refs. 4 and 5). This is especially true for low-voltage circuits where the diode forward voltage drop can no longer be ignored. Under these circumstances, the values obtained are in significant disagreement with measurement.

The analysis given in the first part of this article yields relatively simple equations for rectifier circuit design. In the second part (to be published later), it is shown that the values obtained from the equations agree well with

TABLE 1
List of symbols

Symbol	Definition
C	filter capacitor
D	rectifier diode
f	mains frequency
$I_{C(rms)}$	r.m.s. value of filter-capacitor ripple current
$I_{F(AV)}$	average forward current through diode
$I_{F(AV)max}$	maximum permitted diode average forward current
I_{FIM}	maximum inrush (surge) current
I_{FRM}	repetitive peak forward current through rectifier diode
I_L	load current
I_{rms}	r.m.s. value of diode current
i_{1-2}	instantaneous value of current through R_s during the period from 1 to 2
P_D	rectifier diode power dissipation
P_v	surge-limiting resistor power dissipation
Q	electric charge
R_F	diode forward resistance (as defined in Fig.1)
R_{FD}	diode forward resistance (as defined by traditional methods)
R_L	resistance of load
R_s	source resistance ($R_T + R_v + R_F$, or $R_T + R_v + 2R_F$)
R_T	resistance of power transformer seen looking into the secondary
R_v	surge-limiting resistance
r	ripple factor ($V_{C(rms)}/V_L$)
T	period of mains waveform
t	time
V_{CM}	peak value of ripple voltage in a doubler
$V_{C(rms)}$	r.m.s. value of filter-capacitor ripple voltage
V_F	diode forward voltage (as defined in Fig.1)
V_{FD}	diode forward voltage (as defined by traditional methods)
V_L	mean value of fluctuating rectified direct voltage
V_M	peak secondary voltage
V_{rms}	r.m.s. value of filter input voltage
V_{RWM}	crest working voltage of diode
v	open-circuit secondary voltage of transformer
v_L	instantaneous value of rectified voltage
v_n	rectified and inverted negative portion of input to filter for a doubler
v_p	rectified positive portion of input to filter for a doubler
v_1	minimum value of v_L
v_2	maximum value of v_L
x	= ωt
α	half conduction angle
δ	phase lag between peak of sinusoidal input voltage waveform and half-point of conduction angle
ϕ	= $\delta - x$
ω	angular frequency of mains

ERRATA

measured

empirical values. The second part also presents a set of nomograms, derived from the equations, enabling circuit designs to be achieved in a minimum of time and allowing the effects of changes in component values to be easily visualised.

THE RECTIFIER CIRCUIT

For the purposes of this analysis, the semiconductor rectifier is represented by the equivalent circuit of Fig.1a. A voltage source V_F is connected in series with an ideal diode, having zero forward resistance and infinite reverse resistance, and a resistance of fixed value R_F . The circuit values are obtained from the characteristics of a real rectifier as shown in Fig.1b. Note that the value of V_F must be determined by extrapolation as shown in Fig.1b and thus is not the V_F given in the published data.

A list of symbols used in this article is given in Table 1. The symbols for rectifier-diode parameters are generally in accordance with IEC Recommendation No.148. Unless otherwise stated, all quantities are expressed in SI units.

Equivalent circuit

The equivalent circuit for a half-wave rectifier with CR filter, shown in Fig.2, is used as the basis for the analysis, which is subsequently extended to cover other rectifier arrangements. Transformer leakage inductance is ignored. Source resistance R_s is the sum of R_T the resistance of the power transformer as seen from its secondary, R_F the diode forward resistance, and R_v the value of the surge-limiting resistor. Note that a separate surge-limiting resistor is not necessary if the other circuit resistances are sufficiently high.

Circuit operation

Fig.3 shows the waveforms of the voltages in the rectifier and filter circuit, where it is assumed that the filter capacitor charges and discharges linearly. The open-circuit voltage v of the transformer secondary is given by:

$$v = V_M \cos(\omega t - \delta),$$

where V_M is the peak secondary voltage, and the other symbols have their usual meaning. Diode D conducts only during intervals 1-2 and 1'-2', when $v > (v_L + V_F)$. Filter capacitor C is charged when the diode conducts, and discharges through load R_L during the interval 2-1'. Although the charge and discharge curves are exponential, they can be closely approximated by straight lines as in Fig.3. Since the interval during which the capacitor charges (1-2) is shorter than the interval

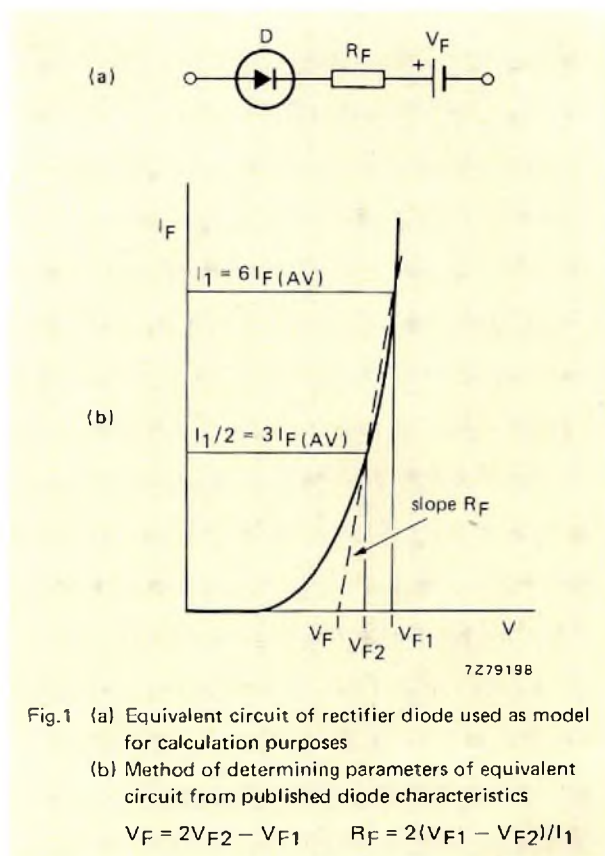


Fig.1 (a) Equivalent circuit of rectifier diode used as model for calculation purposes

(b) Method of determining parameters of equivalent circuit from published diode characteristics

$$V_F = 2V_{F2} - V_{F1} \quad R_F = 2(V_{F1} - V_{F2})/I_1$$

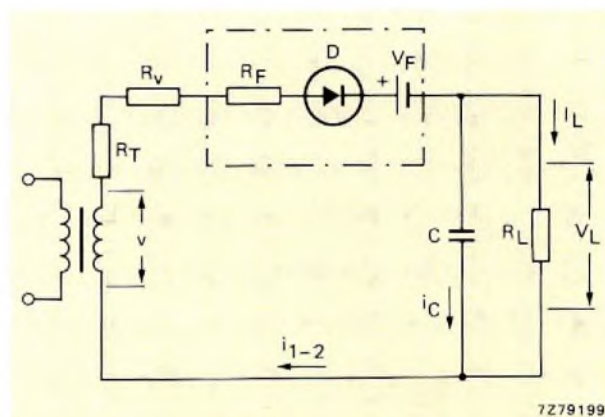


Fig.2 Equivalent circuit of half-wave rectifier with CR filter showing circuit elements and quantities considered in analysis

during which it discharges (2-1'), the peak value of the charging current must be considerably higher than the value of I_L , the average current through R_L .

Diode conducting angle 2α is bisected by the ordinate of Fig.3, which passes to the left of the maximum of the cosine curve by phase lag δ .

All equations required for the design of a rectifier and CR filter circuit will be derived using Fig.3. Two

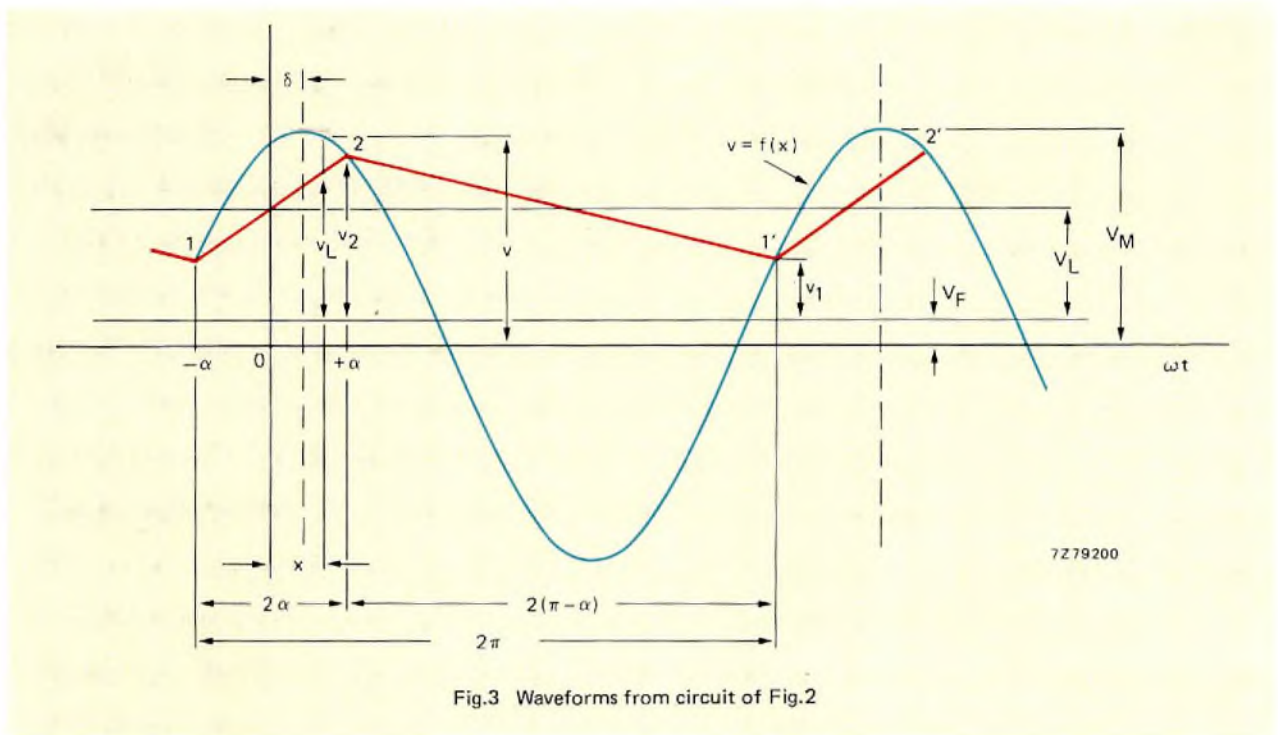


Fig.3 Waveforms from circuit of Fig.2

quantities are fundamental to the analysis: the half-conduction angle α , which is primarily a function of R_s/R_L , and phase lag δ , which depends on α , ω , C , and R_L .

Expression for α

Fig.3 shows that:

instantaneous
Minimum value of output voltage

$$v_1 = V_M \cos(-\alpha - \delta) - V_F$$

$$= V_M \cos(\alpha + \delta) - V_F, \quad (1)$$

and that:

Max

$$v_2 = V_M \cos(\alpha - \delta) - V_F, \quad (2)$$

Since we are assuming that the capacitor charges and discharges linearly, it follows that:

$$V_L = \frac{v_1 + v_2}{2}$$

$$= V_M \frac{\cos(\alpha + \delta) + \cos(\alpha - \delta)}{2} - V_F$$

$$= V_M \cos \alpha \cos \delta - V_F,$$

which can be rearranged to give:

$$V_M = \frac{V_L + V_F}{\cos \alpha \cos \delta}. \quad (3)$$

It further follows from Fig.3 that:

$$v = V_M \cos(x - \delta).$$

Substituting for V_M from Eq.3, we obtain:

$$v = \frac{V_L + V_F}{\cos \alpha \cos \delta} \cos(x - \delta). \quad (4)$$

Combining Eqs.1, 2, and 3 gives an expression for the peak-to-peak ripple voltage:

$$v_2 - v_1 = 2V_M \sin \alpha \sin \delta$$

$$= 2(V_L + V_F) \tan \alpha \tan \delta, \quad (5)$$

whence, as can be seen from Fig.3:

$$v_L = \left(\frac{(V_L + V_F) \tan \alpha \tan \delta}{\alpha} \right) x + V_L, \quad (6)$$

during the interval from 1 to 2.

The instantaneous value of the current flowing through R_s during the period corresponding to the conduction angle 2α is:

$$i_{1-2} = \frac{v - V_L - V_F}{R_s},$$

which, with Eqs. 4 and 6, gives:

$$i_{1-2} = \frac{V_L + V_F}{R_s} \left(\frac{\cos(x - \delta)}{\cos a \cos \delta} - \frac{\tan a \tan \delta}{a} x - 1 \right) \quad (7)$$

The charge that flows through R_s during the same interval is:

$$Q = \int_{-a/\omega}^{+a/\omega} i_{1-2} dt = \frac{1}{\omega} \int_{-a}^{+a} i_{1-2} dx \quad (8)$$

by the substitution $x = \omega t$. Under steady-state conditions, the same charge is drained by R_L during the period of the mains $T = 2\pi/\omega$. Thus:

$$Q = I_L T = I_L 2\pi/\omega \quad (9)$$

Equating Eqs. 8 and 9, and substituting from Eq. 7, gives:

$$I_L = \frac{1}{2\pi} \int_{-a}^{+a} i_{1-2} dx, \\ = \frac{V_L + V_F}{2\pi R_s} \int_{-a}^{+a} \left(\frac{\cos(x - \delta)}{\cos a \cos \delta} - \frac{\tan a \tan \delta}{a} x - 1 \right) dx.$$

After integration:

$$I_L = \frac{V_L + V_F}{\pi R_s} (\tan a - a), \quad (10)$$

which is independent of δ . Putting $I_L = V_L/R_L$ gives:

$$\frac{\pi}{\tan a - a} = \frac{V_L + V_F}{V_L} \cdot \frac{R_L}{R_s} \quad (11)$$

Expression for δ

The charge received by C during interval 1-2 may also be written as:

$$Q = (v_2 - v_1)C \quad (12)$$

Substitution by Eq. 5, gives:

$$Q = 2C(V_L + V_F)\tan a \tan \delta \quad (13)$$

Again, under steady-state conditions, this charge is drained by R_L during the interval 2-1', so that:

$$Q = I_L t_{2-1'} \\ = \frac{V_L}{R_L} \frac{2(\pi - a)}{\omega} \quad (14)$$

Eqs. 13 and 14 together yield an expression for $\tan \delta$:

$$\tan \delta = \frac{\pi - a}{\omega C R_L \tan a} \cdot \frac{V_L}{V_L + V_F} \quad (15)$$

Now that expressions are available for a and δ , we can derive the other equations needed for the design of a half-wave rectifier with a CR filter.

At this stage it is convenient to introduce a dimensionless quantity A, such that

$$A = \frac{V_L + V_F}{V_L} \cdot \frac{R_L}{R_s}$$

for a half-wave rectifier circuit. The value of a as a function of A is tabulated in Table 2.

CALCULATION OF CIRCUIT VOLTAGES

The input voltage and ripple voltage are calculated as outlined below.

Input voltage V_{rms}

It has already been shown (Eq. 3) that:

$$V_M = \frac{V_L + V_F}{\cos a \cos \delta}$$

Thus, since: $V_M = V_{rms} \sqrt{2}$,

it follows that the transformer open-circuit secondary voltage is given by:

$$V_{rms} = \frac{V_L + V_F}{\sqrt{2} \cos a \cos \delta} \quad (16)$$

Ripple voltage $V_{C(rms)}$

The r.m.s. value of the sawtooth ripple voltage is:

$$V_{C(rms)} = \frac{v_2 - v_1}{2\sqrt{3}}$$

Substitution by Eq. 5 gives:

$$V_{C(rms)} = \frac{(V_L + V_F)\tan a \tan \delta}{\sqrt{3}} \quad (17)$$

The ratio of $V_{C(rms)}$ to V_L is the ripple factor r :

$$r = \frac{V_{C(rms)}}{V_L} = \frac{V_L + V_F}{V_L \sqrt{3}} \tan a \tan \delta \quad (18)$$

TABLE 2 The value of α as a function of A

A	SECOND OR (IF FIRST DIGIT IS 1) THIRD SIGNIFICANT DIGIT OF A									
	0	1	2	3	4	5	6	7	8	9
0.6	1.4217	1.4197	1.4178	1.4159	1.4139	1.4120	1.4101	1.4082	1.4064	1.4045
0.7	1.4026	1.4008	1.3990	1.3971	1.3953	1.3935	1.3918	1.3900	1.3882	1.3865
0.8	1.3847	1.3830	1.3813	1.3795	1.3778	1.3761	1.3745	1.3728	1.3711	1.3695
0.9	1.3678	1.3662	1.3645	1.3629	1.3613	1.3597	1.3581	1.3565	1.3549	1.3534
1.0	1.3518	1.3503	1.3487	1.3472	1.3457	1.3441	1.3426	1.3411	1.3396	1.3381
1.1	1.3367	1.3352	1.3337	1.3323	1.3308	1.3294	1.3279	1.3265	1.3251	1.3237
1.2	1.3223	1.3209	1.3195	1.3181	1.3167	1.3153	1.3139	1.3126	1.3112	1.3099
1.3	1.3085	1.3072	1.3059	1.3045	1.3032	1.3019	1.3006	1.2993	1.2980	1.2967
1.4	1.2954	1.2942	1.2929	1.2916	1.2904	1.2891	1.2879	1.2866	1.2854	1.2842
1.5	1.2829	1.2817	1.2805	1.2793	1.2781	1.2769	1.2757	1.2745	1.2733	1.2721
1.6	1.2709	1.2698	1.2686	1.2674	1.2663	1.2651	1.2640	1.2629	1.2617	1.2606
1.7	1.2595	1.2583	1.2572	1.2561	1.2550	1.2539	1.2528	1.2517	1.2506	1.2495
1.8	1.2484	1.2473	1.2463	1.2452	1.2441	1.2431	1.2420	1.2409	1.2399	1.2389
1.9	1.2378	1.2368	1.2357	1.2347	1.2337	1.2327	1.2316	1.2306	1.2296	1.2286
2	1.2276	1.2177	1.2082	1.1991	1.1902	1.1816	1.1733	1.1652	1.1574	1.1498
3	1.1424	1.1352	1.1282	1.1214	1.1148	1.1083	1.1020	1.0959	1.0899	1.0840
4	1.0783	1.0727	1.0673	1.0619	1.0567	1.0516	1.0466	1.0417	1.0368	1.0321
5	1.0275	1.0229	1.0185	1.0141	1.0098	1.0056	1.0015	0.9974	0.9934	0.9895
6	0.9856	0.9818	0.9781	0.9744	0.9708	0.9672	0.9637	0.9603	0.9569	0.9535
7	0.9502	0.9470	0.9438	0.9406	0.9375	0.9344	0.9314	0.9284	0.9254	0.9225
8	0.9197	0.9168	0.9140	0.9113	0.9086	0.9059	0.9032	0.9006	0.8980	0.8954
9	0.8929	0.8904	0.8879	0.8855	0.8831	0.8807	0.8783	0.8760	0.8737	0.8714
10	0.8692	0.8669	0.8647	0.8625	0.8604	0.8582	0.8561	0.8540	0.8520	0.8499
11	0.8479	0.8459	0.8439	0.8419	0.8400	0.8380	0.8361	0.8342	0.8323	0.8305
12	0.8286	0.8268	0.8250	0.8232	0.8214	0.8197	0.8179	0.8162	0.8145	0.8128
13	0.8111	0.8094	0.8078	0.8061	0.8045	0.8029	0.8013	0.7997	0.7981	0.7966
14	0.7950	0.7935	0.7919	0.7904	0.7889	0.7874	0.7860	0.7845	0.7831	0.7816
15	0.7802	0.7788	0.7774	0.7760	0.7746	0.7732	0.7718	0.7705	0.7691	0.7678
16	0.7664	0.7651	0.7638	0.7625	0.7612	0.7599	0.7587	0.7574	0.7561	0.7549
17	0.7537	0.7524	0.7512	0.7500	0.7488	0.7476	0.7464	0.7452	0.7441	0.7429
18	0.7417	0.7406	0.7394	0.7383	0.7372	0.7360	0.7349	0.7338	0.7327	0.7316
19	0.7305	0.7295	0.7284	0.7273	0.7263	0.7252	0.7241	0.7231	0.7221	0.7210
20	0.7200	0.7101	0.7007	0.6918	0.6834	0.6754	0.6677	0.6604	0.6534	0.6467
30	0.6403	0.6342	0.6282	0.6225	0.6170	0.6117	0.6066	0.6016	0.5969	0.5922
40	0.5877	0.5834	0.5791	0.5750	0.5710	0.5672	0.5634	0.5597	0.5562	0.5527
50	0.5493	0.5460	0.5427	0.5396	0.5365	0.5335	0.5305	0.5277	0.5248	0.5221
60	0.5194	0.5167	0.5142	0.5116	0.5091	0.5067	0.5043	0.5020	0.4997	0.4974
70	0.4952	0.4930	0.4909	0.4888	0.4867	0.4847	0.4827	0.4807	0.4788	0.4769
80	0.4750	0.4732	0.4713	0.4696	0.4678	0.4661	0.4644	0.4627	0.4610	0.4594
90	0.4578	0.4562	0.4546	0.4531	0.4516	0.4501	0.4486	0.4471	0.4457	0.4443
100	0.4428	0.4415	0.4401	0.4387	0.4374	0.4361	0.4348	0.4335	0.4322	0.4310
110	0.4297	0.4285	0.4273	0.4261	0.4249	0.4237	0.4225	0.4214	0.4203	0.4191
120	0.4180	0.4169	0.4158	0.4148	0.4137	0.4126	0.4116	0.4106	0.4095	0.4085
130	0.4075	0.4065	0.4055	0.4046	0.4036	0.4027	0.4017	0.4008	0.3998	0.3989
140	0.3980	0.3971	0.3962	0.3953	0.3945	0.3936	0.3927	0.3919	0.3910	0.3902
150	0.3893	0.3885	0.3877	0.3869	0.3861	0.3853	0.3845	0.3837	0.3829	0.3822
160	0.3814	0.3806	0.3799	0.3791	0.3784	0.3776	0.3769	0.3762	0.3755	0.3748
170	0.3741	0.3733	0.3727	0.3720	0.3713	0.3706	0.3699	0.3692	0.3686	0.3679
180	0.3673	0.3666	0.3660	0.3653	0.3647	0.3640	0.3634	0.3628	0.3622	0.3615
190	0.3609	0.3603	0.3597	0.3591	0.3585	0.3579	0.3573	0.3568	0.3562	0.3556
200	0.3550	0.3495	0.3443	0.3394	0.3347	0.3304	0.3262	0.3222	0.3184	0.3148
300	0.3114	0.3081	0.3049	0.3019	0.2990	0.2962	0.2935	0.2909	0.2884	0.2859
400	0.2836	0.2813	0.2791	0.2770	0.2749	0.2729	0.2709	0.2690	0.2672	0.2654
500	0.2636	0.2619	0.2603	0.2587	0.2571	0.2555	0.2540	0.2526	0.2511	0.2497
600	0.2484	0.2470	0.2457	0.2444	0.2432	0.2419	0.2407	0.2395	0.2384	0.2372
700	0.2361	0.2350	0.2339	0.2329	0.2318	0.2308	0.2298	0.2288	0.2279	0.2269
800	0.2260	0.2251	0.2242	0.2233	0.2224	0.2215	0.2207	0.2198	0.2190	0.2182
900	0.2174	0.2166	0.2158	0.2151	0.2143	0.2136	0.2128	0.2121	0.2114	0.2107
1000	0.2100	0.2093	0.2086	0.2079	0.2073	0.2066	0.2060	0.2054	0.2047	0.2041
1100	0.2035	0.2029	0.2023	0.2017	0.2011	0.2005	0.2000	0.1994	0.1988	0.1983
1200	0.1977	0.1972	0.1967	0.1961	0.1956	0.1951	0.1946	0.1941	0.1936	0.1931
1300	0.1926	0.1921	0.1916	0.1911	0.1907	0.1902	0.1897	0.1893	0.1888	0.1884
1400	0.1879	0.1875	0.1870	0.1866	0.1862	0.1858	0.1853	0.1849	0.1845	0.1841
1500	0.1837	0.1833	0.1829	0.1825	0.1821	0.1817	0.1813	0.1809	0.1806	0.1802
1600	0.1798	0.1794	0.1791	0.1787	0.1784	0.1780	0.1776	0.1773	0.1769	0.1766
1700	0.1763	0.1759	0.1756	0.1752	0.1749	0.1746	0.1742	0.1739	0.1736	0.1733
1800	0.1730	0.1726	0.1723	0.1720	0.1717	0.1714	0.1711	0.1708	0.1705	0.1702
1900	0.1699	0.1696	0.1693	0.1690	0.1687	0.1684	0.1681	0.1679	0.1676	0.1673
2000	0.1670	0.1664	0.1661	0.1659	0.1657	0.1655	0.1653	0.1652	0.1649	0.1647

CALCULATION OF FILTER CAPACITANCE

It follows from Eqs. 15 and 18 that the filter capacitance C is given by:

$$C = \frac{\pi - \alpha}{r\omega R_L \sqrt{3}} \tag{19}$$

CALCULATION OF CIRCUIT CURRENTS

The r.m.s. and peak diode currents are calculated as outlined below.

R.M.S. diode current

Since current flows through the diode during the interval 1-2 only, the r.m.s. value of the diode current is given by:

$$I_{rms} = \left[\frac{1}{2\pi} \int_{-\alpha}^{+\alpha} i^2_{1-2} dx \right]^{1/2} \tag{20}$$

Squaring and integrating Eq. 7 gives:

$$\int_{-\alpha}^{+\alpha} i^2_{1-2} dx = \frac{(V_L + V_F)^2}{R_s^2} \int_{-\alpha}^{+\alpha} \left(\frac{\cos^2(x - \delta)}{\cos^2 \alpha \cos^2 \delta} + \frac{\tan^2 \alpha \tan^2 \delta}{a^2} x^2 + 1 - \frac{2\cos(x - \delta)\tan \alpha \tan \delta}{a \cos \alpha \cos \delta} x - \frac{2\cos(x - \delta)}{\cos \alpha \cos \delta} + \frac{2\tan \alpha \tan \delta}{a} x \right) dx.$$

This integration is performed in Appendix 1, where it is shown that:

$$\int_{-\alpha}^{+\alpha} i^2_{1-2} dx = \left(\frac{\pi I_L}{\cos \alpha \cos \delta (\tan \alpha - a)} \right)^2 (\ell + m + p) \tag{21}$$

where:

$$\ell = \alpha + \frac{\sin 2\alpha \cos 2\delta}{2}$$

$$m = 2\sin \alpha \sin^2 \delta \left(\frac{a \sin \alpha}{3} - \frac{2(\sin \alpha - a \cos \alpha)}{a} \right)$$

$$p = 2\cos \alpha \cos^2 \delta (a \cos \alpha - 2\sin \alpha)$$

Finally, combining Eqs. 20 and 21 gives:

$$I_{rms} = \frac{I_L}{\cos \alpha \cos \delta (\tan \alpha - a)} \left[\frac{(\ell + m + p)\pi}{2} \right]^{1/2} \tag{22}$$

Peak diode current

The peak value of i_{1-2} is found by differentiating Eq. 7 and equating the result to zero:

$$\frac{di_{1-2}}{dx} = \frac{V_L + V_F}{R_s} \left(-\frac{\sin(x - \delta)}{\cos \alpha \cos \delta} - \frac{\tan \alpha \tan \delta}{a} \right) = 0,$$

and thus:

$$\sin(\delta - x) = \frac{\sin \alpha \sin \delta}{a}$$

Now, putting $(\delta - x) = \phi$ gives:

$$\phi = \arcsin \left(\frac{\sin \alpha \sin \delta}{a} \right) \tag{23}$$

so that:

$$x = \delta - \arcsin \left(\frac{\sin \alpha \sin \delta}{a} \right)$$

Substituting for x in Eq. 7 and using Eq. 10 yields the peak repetitive forward diode current:

$$I_{FRM} = \frac{\pi I_L}{\cos \alpha \cos \delta (\tan \alpha - a)} \left(\cos \phi - \frac{\sin \alpha \sin \delta}{a} (\delta - \phi) - \cos \alpha \cos \delta \right) \tag{24}$$

This expression may be simplified by first considering the one term:

$$\frac{\cos \phi - \frac{\sin \alpha \sin \delta}{a} (\delta - \phi) - \cos \alpha \cos \delta}{\cos \delta}$$

which equals:

$$\frac{\cos \phi}{\cos \delta} - \frac{\sin \alpha \tan \delta}{a} (\delta - \phi) - \cos \alpha$$

It is found that, with practical circuit values:

$$\frac{\cos \phi}{\cos \delta} - \frac{\sin \alpha \tan \delta}{a} (\delta - \phi) \approx 1$$

to an accuracy of 0.1%. We can therefore simplify Eq. 24 to give:

$$I_{FRM} = \frac{\pi I_L}{\cos \alpha (\tan \alpha - a)} (1 - \cos \alpha) \tag{25}$$

Note that this expression for I_{FRM} is independent of δ .

OTHER RECTIFIER CIRCUITS

So far, only half-wave rectifiers have been considered. However, the expressions derived above can be readily adapted to other rectifier circuits. Design equations for the following rectifier circuits with CR filters are given below:

- bridge rectifier (Fig. 4);
- centre-tapped full-wave rectifier (Fig. 5);
- half-wave rectifier (Fig. 6);
- symmetrical voltage doubler (Fig. 7).

Bridge and full-wave rectifiers

In the expressions that follow, $n = 2$ for the bridge circuit of Fig. 4 and $n = 1$ for the full-wave circuit of Fig. 5.

$$A = \frac{2(V_L + nV_F)}{V_L} \cdot \frac{R_L}{R_s} \tag{26}$$

$$\tan a - a = \frac{\pi}{\Lambda} \tag{27}$$

$$\begin{aligned} \tan \delta &= \frac{\frac{\pi}{2} - a}{\omega CR_L \tan a} \cdot \frac{V_L}{V_L + nV_F} \\ &= \frac{2 \left(\frac{\pi}{2} - a \right)}{A \omega CR_s \tan a} \end{aligned} \tag{28}$$

$$V_{rms} = \frac{V_L + nV_F}{\sqrt{2} \cdot \cos a \cos \delta} \tag{29}$$

$$\begin{aligned} r &= \frac{V_L + nV_F}{V_L} \cdot \frac{\tan a \tan \delta}{\sqrt{3}} \\ &= \frac{\Lambda R_s \tan a \tan \delta}{2R_L \sqrt{3}} \end{aligned} \tag{30}$$

$$C = \frac{\frac{\pi}{2} - a}{r \omega R_L \sqrt{3}} \tag{31}$$

$$I_{rms} = \frac{A I_L}{2 \cos a \cos \delta} \left[\frac{\ell + m + p}{2\pi} \right]^{1/2} \tag{32}$$

where ℓ , m , and p are as given for Eq. 21.

$$I_{FRM} = \frac{A I_L (1 - \cos a)}{2 \cos a} \tag{33}$$

Half-wave rectifiers and symmetrical doublers

In the expressions that follow, $n = 1$ for the half-wave circuit of Fig. 6 and $n = 2$ for the symmetrical doubler of Fig. 7.

$$A = \frac{V_L + nV_F}{nV_L} \cdot \frac{R_L}{R_s} \tag{34}$$

$$\tan a - a = \frac{\pi}{\Lambda} \tag{35}$$

$$\begin{aligned} \tan \delta &= \frac{\pi - a}{\omega CR_L \tan a} \cdot \frac{nV_L}{V_L + nV_F} \\ &= \frac{\pi - a}{\Lambda \omega CR_s \tan a} \end{aligned} \tag{36}$$

$$V_{rms} = \frac{V_L + nV_F}{n\sqrt{2} \cdot \cos a \cos \delta} \tag{37}$$

$$\begin{aligned} r &= \frac{V_L + nV_F}{nV_L} \cdot \frac{\tan a \tan \delta}{\sqrt{3}} \cdot \frac{\pi - na}{\pi - a} \\ &= A \frac{R_s}{R_L} \cdot \frac{\tan a \tan \delta}{\sqrt{3}} \cdot \frac{\pi - na}{\pi - a} \end{aligned} \tag{38}$$

This expression for the ripple factor r in a symmetrical voltage doubler is derived in Appendix 2.

$$C = \frac{\pi - na}{r \omega R_L \sqrt{3}} \tag{39}$$

$$I_{rms} = \frac{A I_L}{\cos a \cos \delta} \left[\frac{\ell + m + p}{2\pi} \right]^{1/2} \tag{40}$$

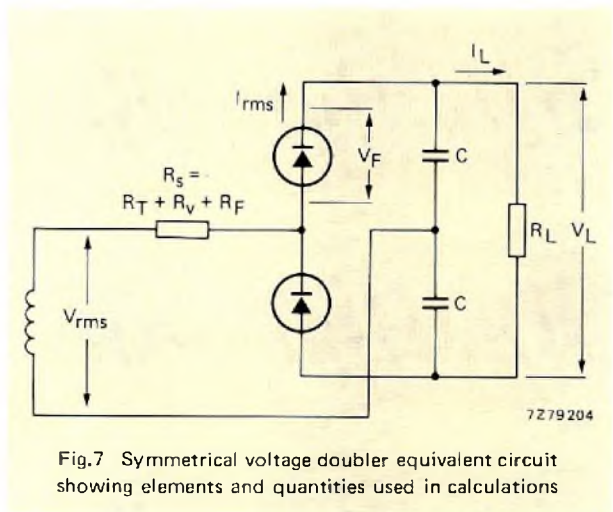
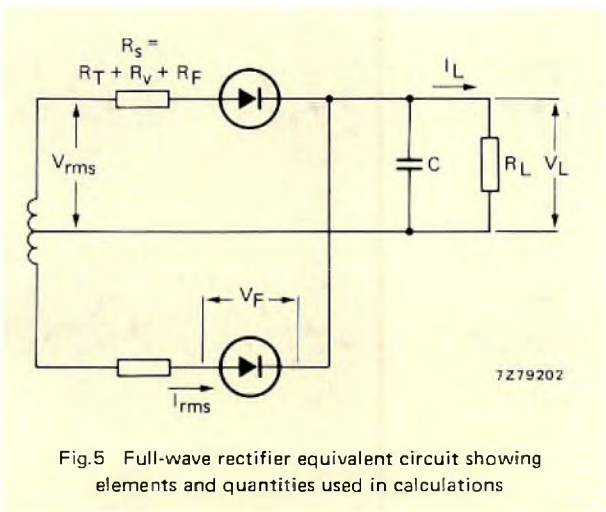
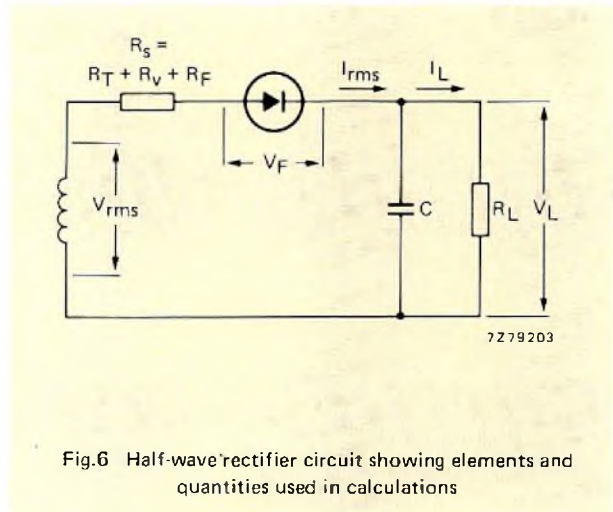
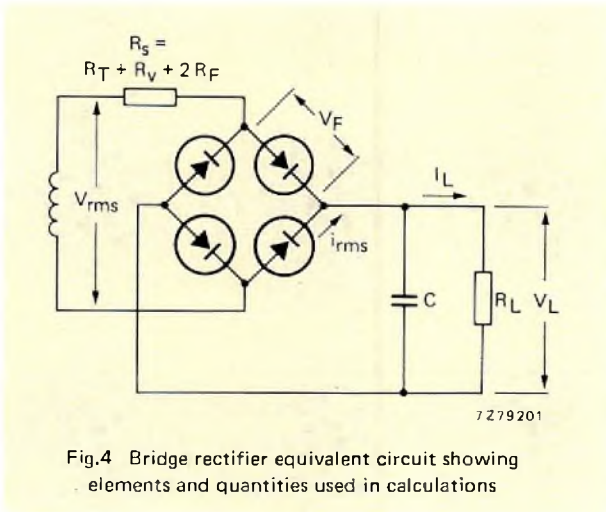
where ℓ , m , and p are as given for Eq. 21.

$$I_{FRM} = \frac{A I_L (1 - \cos a)}{\cos a} \tag{41}$$

Part 2 will compare values derived from these equations with those derived from previously used methods and from experiment.

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APPENDIX I

Solution of expression for diode r.m.s. current I_{rms}

$$\begin{aligned}
 \int_{-a}^{+a} i^2 I_{-2} dx &= \left(\frac{V_L + V_F}{R_s} \right)^2 \int_{-a}^{+a} \left(\frac{\cos^2(x - \delta)}{\cos^2 a \cos^2 \delta} + \right. \\
 &+ \frac{\tan^2 a \tan^2 \delta}{a^2} x^2 + 1 - \\
 &- \frac{2\cos(x - \delta) \tan a \tan \delta}{a \cos a \cos \delta} x - \\
 &\left. - \frac{2\cos(x - \delta)}{\cos a \cos \delta} + \frac{2\tan a \tan \delta}{a} x \right) dx, \\
 &= \left(\frac{V_L + V_F}{R_s} \right)^2 (a + b + d - g - h + k).
 \end{aligned}
 \tag{42}$$

Integrating:

$$\begin{aligned}
 a &= \frac{1}{\cos^2 a \cos^2 \delta} \int_{-a}^{+a} \cos^2(x - \delta) dx, \\
 &= \frac{1}{\cos^2 a \cos^2 \delta} \int_{-a}^{+a} \frac{1 + \cos 2(x - \delta)}{2} dx, \\
 &= \frac{1}{\cos^2 a \cos^2 \delta} \left[\frac{x}{2} + \frac{\sin 2(x - \delta)}{4} \right]_{-a}^{+a}, \\
 &= \frac{1}{\cos^2 a \cos^2 \delta} (a + \frac{1}{2} \sin 2a \cos 2\delta).
 \end{aligned}$$

$$b = \frac{\tan^2 a \tan^2 \delta}{a^2} \int_{-a}^{+a} x^2 dx,$$

$$= \frac{\tan^2 a \tan^2 \delta}{a^2} \left[\frac{x^3}{3} \right]_{-a}^{+a} = \frac{2a \tan^2 a \tan^2 \delta}{3}.$$

$$d = \int_{-a}^{+a} dx = 2a.$$

$$g = \frac{2 \tan a \tan \delta}{a \cos a \cos \delta} \int_{-a}^{+a} x \cos(x - \delta) dx,$$

$$= \frac{2 \tan a \tan \delta}{a \cos a \cos \delta} \left[x \sin(x - \delta) + \cos(x - \delta) \right]_{-a}^{+a},$$

$$= \frac{2 \tan a \tan \delta}{a \cos a \cos \delta} \left[a \sin(a - \delta) + \cos(a - \delta) - \right.$$

$$\left. - \left\{ -a \sin(-a - \delta) + \cos(-a - \delta) \right\} \right],$$

$$= \frac{2 \tan a \tan \delta}{a \cos a \cos \delta} \left\{ a \sin(a - \delta) + \cos(a - \delta) - \right.$$

$$\left. - a \sin(a + \delta) - \cos(a + \delta) \right\},$$

$$= \frac{2 \tan a \tan \delta}{a \cos a \cos \delta} (a \sin a \cos \delta - a \cos a \sin \delta +$$

$$+ \cos a \cos \delta + \sin a \sin \delta - a \sin a \cos \delta -$$

$$- a \cos a \sin \delta - \cos a \cos \delta + \sin a \sin \delta),$$

$$= \frac{2 \tan a \tan \delta}{a \cos a \cos \delta} (2 \sin a \sin \delta - 2 a \cos a \sin \delta),$$

$$= \frac{4 \tan a \tan^2 \delta}{a \cos a} (\sin a - a \cos a).$$

$$h = \frac{2}{\cos a \cos \delta} \int_{-a}^{+a} \cos(x - \delta) dx,$$

$$= \frac{2}{\cos a \cos \delta} \left[\sin(x - \delta) \right]_{-a}^{+a}$$

$$= \frac{2}{\cos a \cos \delta} \left[\sin x \cos \delta - \cos x \sin \delta \right]_{-a}^{+a}.$$

$$= \frac{4 \sin a \cos \delta}{\cos a \cos \delta}, = 4 \tan a.$$

$$k = \frac{2 \tan a \tan \delta}{a} \int_{-a}^{+a} x dx$$

$$= \frac{2 \tan a \tan \delta}{a} \left[\frac{x^2}{2} \right]_{-a}^{+a} = 0.$$

Inserting these expressions for a, b, d, g, h, and k into Eq. 42 gives:

$$\int_{-a}^{+a} i_{1-2}^2 dx = \left(\frac{V_L + V_F}{R_s} \right)^2 \left\{ \frac{a + \frac{1}{2} \sin 2a \cos 2\delta}{\cos^2 a \cos^2 \delta} + \right.$$

$$+ \frac{2a \tan^2 a \tan^2 \delta}{3} + 2a -$$

$$\left. - \frac{4 \tan a \tan^2 \delta}{a \cos a} (\sin a - a \cos a) - 4 \tan a \right\},$$

$$= \left(\frac{V_L + V_F}{R_s \cos a \cos \delta} \right)^2 \left\{ (a + \frac{1}{2} \sin 2a \cos 2\delta) + \right.$$

$$+ \frac{2a \sin^2 a \sin^2 \delta}{3} + 2a \cos^2 a \cos^2 \delta -$$

$$\left. - \frac{4 \sin a \sin^2 \delta}{a} (\sin a - a \cos a) - \right.$$

$$\left. - 4 \sin a \cos a \cos^2 \delta \right\},$$

$$= \left(\frac{V_L + V_F}{R_s \cos a \cos \delta} \right)^2 \left\{ (a + \frac{1}{2} \sin 2a \cos 2\delta) + \right.$$

$$+ 2 \sin a \sin^2 \delta \left(\frac{a \sin a}{3} - \frac{2(\sin a - a \cos a)}{a} \right) +$$

$$\left. + 2 \cos a \cos^2 \delta (a \cos a - 2 \sin a) \right\},$$

$$= \left(\frac{V_L + V_F}{R_s \cos a \cos \delta} \right)^2 (\ell + m + p). \quad (43)$$

where ℓ , m , and p are as defined for Eq. 21.

Finally, combining Eqs. 10 and 43 gives:

$$\int_{-a}^{+a} i_{1-2}^2 dx = \left(\frac{\pi I_L}{\cos a \cos \delta (\tan a - a)} \right)^2 (\ell + m + p). \quad (44)$$

APPENDIX 2

Derivation of expression for ripple factor in voltage doubling rectifier circuit

Rectification in a voltage doubler circuit is a similar process to half-wave rectification, the main difference being that both positive and negative portions of the applied alternating voltage are rectified, and are then added to obtain the doubled output voltage V_L . Fig. 8 shows the waveforms in a symmetrical voltage doubler. Here, v_p is the rectified positive portion of the input, and v_n the rectified (and inverted) negative portion. The sum of these two voltages is the fluctuating voltage v_L whose mean value is V_L (delivered to the load).

It can be seen from Fig. 8 that the peak value of the ripple voltage is:

$$V_{CM} = \frac{v_2 - v_1}{2}, \quad (45)$$

where: $v_2 = v_{p2} + v_{n2}, \quad (46)$

$$v_1 = v_{p1} + v_{n1}. \quad (47)$$

Considering triangles ABC and CDE in Fig. 8, it follows that $DE/a = AB/(\pi - a)$, or:

$$\frac{\{(V_L/2) + V_F\} - v_{n2}}{a} = \frac{v_{p2} - \{(V_L/2) + V_F\}}{\pi - a}. \quad (48)$$

Now considering triangles FGH and HIJ, it follows that $FG/a = IJ/(\pi - a)$, or:

$$\frac{v_{n1} - \{(V_L/2) + V_F\}}{a} = \frac{\{(V_L/2) + V_F\} - v_{p1}}{\pi - a}. \quad (49)$$

Eq. 48 gives:

$$v_{n2} = \left(\frac{V_L}{2} + V_F\right) + \frac{a}{\pi - a} \left\{ \left(\frac{V_L}{2} + V_F\right) - v_{p2} \right\}, \quad (50)$$

and Eq. 49 gives

$$v_{n1} = \left(\frac{V_L}{2} + V_F\right) + \frac{a}{\pi - a} \left\{ \left(\frac{V_L}{2} + V_F\right) - v_{p1} \right\}, \quad (51)$$

Substituting for v_{n2} and v_{n1} in Eqs. 46 and 47 (using Eqs. 50 and 51), introducing the results into Eq. 45, and rearranging gives:

$$V_{CM} = \frac{1}{2} (v_{p2} - v_{p1}) \frac{\pi - 2a}{\pi - a}. \quad (52)$$

Using Eq. 5 for $(v_{p2} - v_{p1})$ gives:

$$V_{CM} = \frac{(V_L + 2V_F)(\pi - 2a)}{2(\pi - a)} \tan \alpha \tan \delta. \quad (53)$$

Since the r.m.s. value of V_C (sawtooth waveform) is given by:

$$V_{C(rms)} = \frac{V_{CM}}{\sqrt{3}},$$

the ripple factor of the voltage doubler must be:

$$r = \frac{V_{C(rms)}}{V_L} = \frac{(V_L + 2V_F)(\pi - 2a)}{2\sqrt{3} \cdot V_L(\pi - a)} \tan \alpha \tan \delta. \quad (54)$$

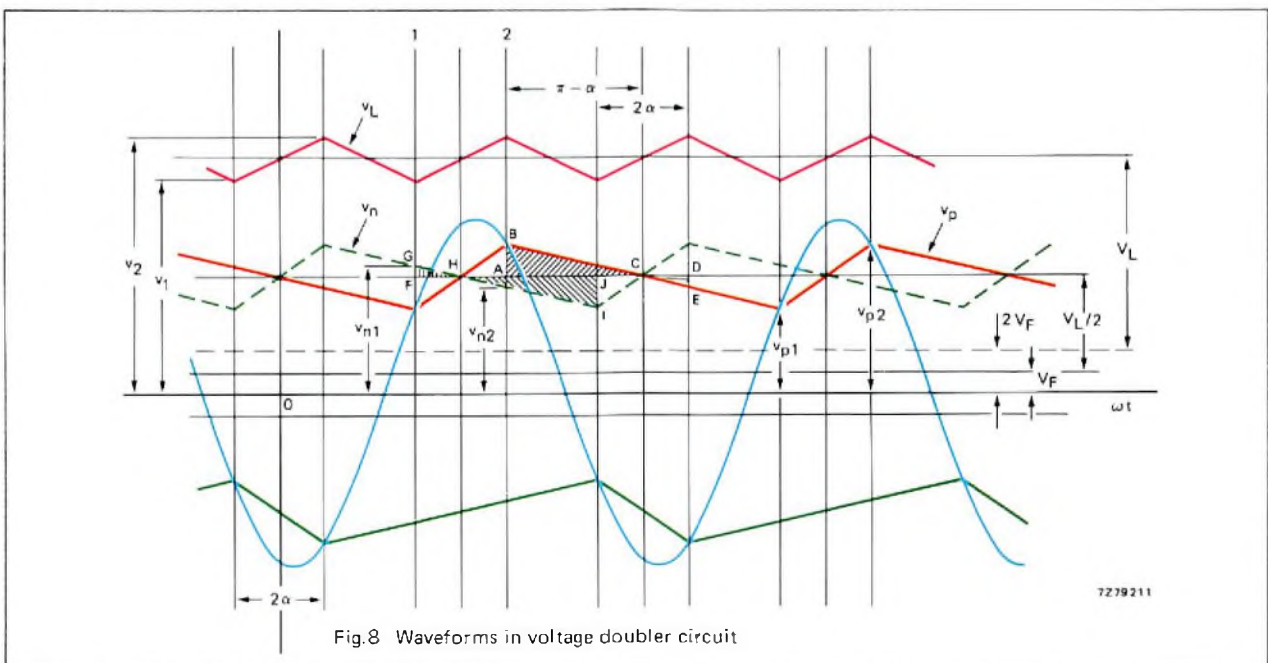


Fig.8 Waveforms in voltage doubler circuit

Understanding thyristor and triac data

P. G. NOBLE

INTRODUCTION

The importance of reliable and comprehensive data, together with the advantages of the absolute maximum rating system, was outlined in Ref. 1 which related to rectifier diodes. This present article extends the treatment to thyristors and triacs, and aims at enabling the circuit designer to use our published data to the full and to be confident that it truly describes the performance of the devices.

A brief survey of short-form catalogues is an insufficient method of comparing different devices. Published ratings and characteristics require supporting information to truly describe the capabilities of devices; thus comparisons between devices whose performance *appears* to be similar should not be made on economic grounds alone. Manufacturers have been known to quote ratings

in such a way as to give a false impression of the capabilities of their devices.

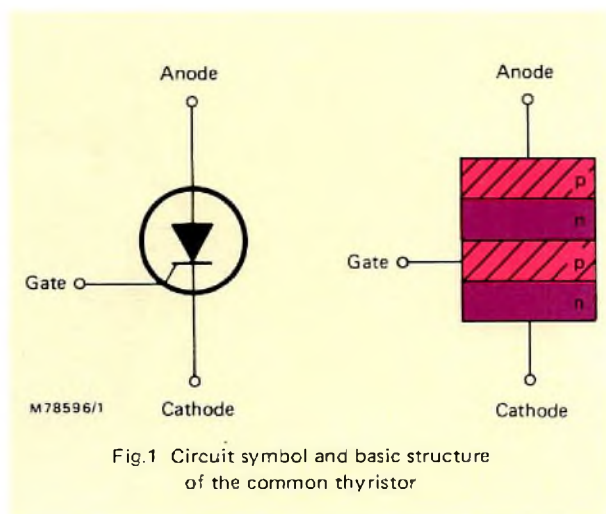
Ratings and characteristics given in published data should always be quoted with the conditions to which they apply, and these conditions should be those likely to occur in operation. Furthermore, it is important to define the rating or characteristic being quoted. Only if data is both complete and unambiguous can a true comparison be made between the capabilities of different types.

THYRISTORS

Thyristor is a generic term for a semiconductor device which has four semiconductor layers and operates as a switch, having stable on and off states. A thyristor can have two, three, or four terminals but common usage has confined the term thyristor to three-terminal devices. Two-terminal devices are known as switching diodes, and four-terminal devices are known as silicon controlled switches. The common, or three-terminal, thyristor is also known as the reverse blocking triode thyristor or the silicon controlled rectifier. Fig. 1 shows the circuit symbol and a schematic diagram of the thyristor. All our thyristors are p-gate types; that is, the anode is connected to the stud (or heatsink) of the encapsulation.

The thyristor will conduct a load current in one direction only, as will a rectifier diode. However, the thyristor will only conduct this load current when it has been 'triggered'; this is the essential property of the thyristor.

Fig. 2 shows the static characteristic of the thyristor. When a small negative voltage is applied to the device,



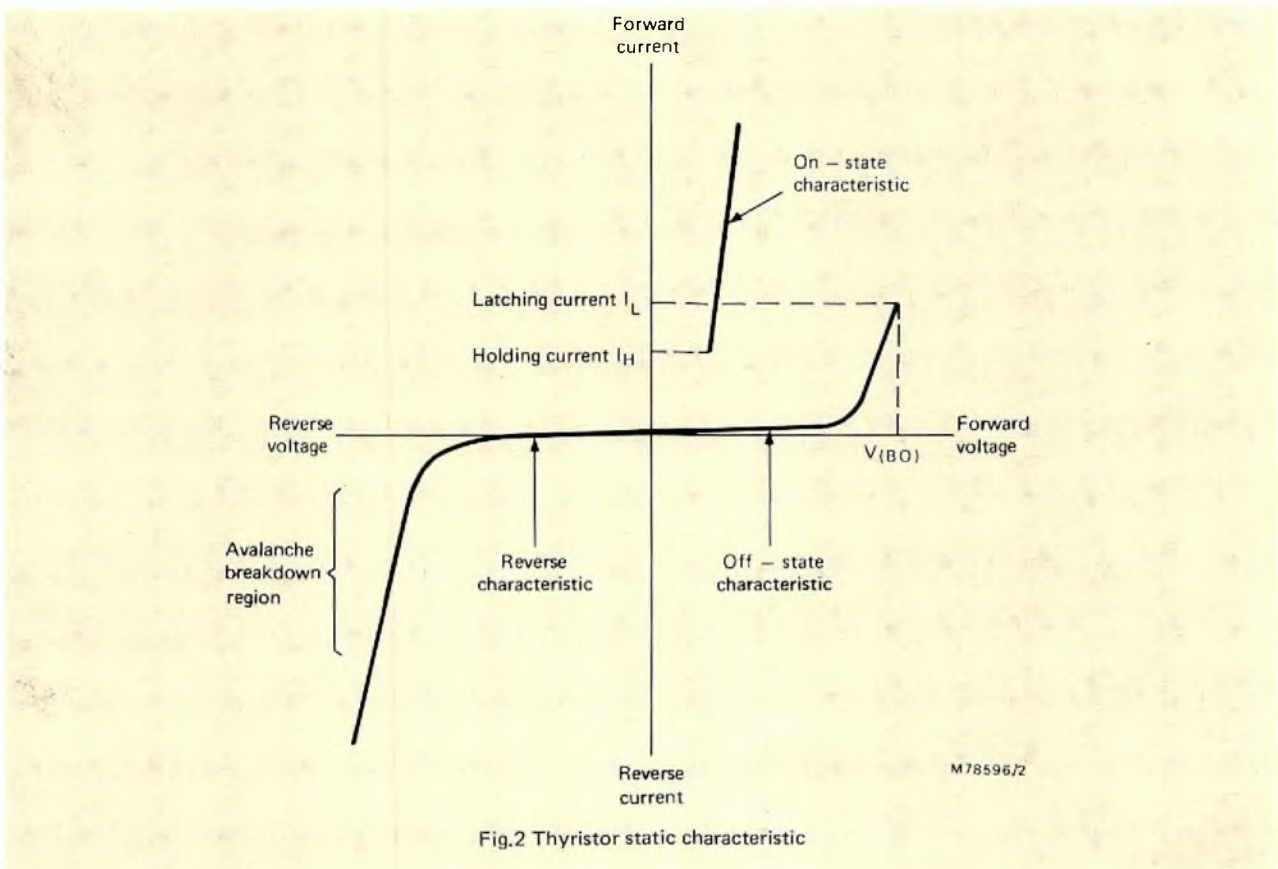


Fig.2 Thyristor static characteristic

only a small reverse leakage current flows. As the reverse voltage is increased, the leakage current increases until avalanche breakdown occurs. If a positive voltage is applied, then again a small forward leakage current flows which increases as the forward voltage increases. When the forward voltage reaches the breakover voltage $V_{(BO)}$, turn-on is initiated by avalanche breakdown and the voltage across the thyristor falls to the on state voltage V_T .

However, turn-on can occur when the forward (anode-to-cathode) voltage is less than $V_{(BO)}$ if the thyristor is triggered by injecting a pulse of current into the gate. If the device is to remain in the on state, this trigger pulse must remain until the current through the thyristor exceeds the latching current I_L . Once the on state is established, the holding current I_H is the minimum current that can flow through the thyristor and still maintain conduction. The load current must be reduced to below I_H to turn the thyristor off; for instance, by reducing the voltage across the thyristor and load to zero.

Thyristors are normally turned on by triggering with a gate signal but they can also be turned on by exceeding either the forward breakover voltage or the permitted rate of rise of anode voltage dV_D/dt . These alternative methods of switching to the conducting state, however, should be avoided by suitable circuit design.

THYRISTOR DATA

The published data for thyristors contains information on voltage, current, and temperature ratings, the thermal resistances associated with the devices, as well as electrical and switching characteristics.

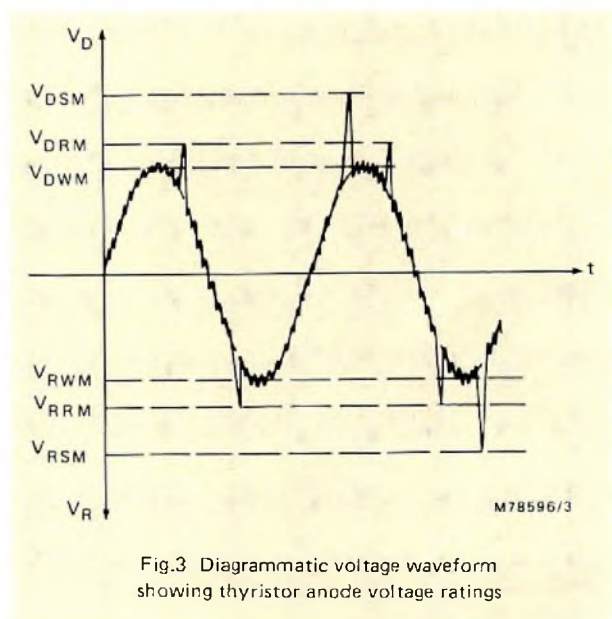


Fig.3 Diagrammatic voltage waveform showing thyristor anode voltage ratings

Anode-to-cathode voltage ratings

The voltage of the a.c. mains is usually regarded as a smooth sine wave. In practice, however, there are a variety of transients, some occurring regularly and others only occasionally. Although some of the higher-valued transients may be removed by filters, thyristors must still handle anode-to-cathode voltages in excess of the nominal mains value.

The following reverse off-state voltage ratings are given in our published data (see Fig. 3).

- V_{RSM} : the non-repetitive* peak reverse voltage, which is the peak value of non-repetitive voltage transients. This rating should be quoted with the maximum duration of transient that can be handled (usually $t \leq 10$ ms).
- V_{RRM} : the repetitive* peak reverse voltage, which is the peak value of transients occurring every cycle.
- V_{RWM} : the crest (peak) working reverse voltage, which is the maximum continuous peak voltage rating in the reverse direction, neglecting transients. It corresponds to the peak negative value (often with a safety factor) of the sinusoidal supply voltage.

The forward off-state voltages corresponding to V_{RSM} , V_{RRM} , and V_{RWM} are listed below.

- V_{DSM} : the non-repetitive peak off-state voltage applied in the forward direction.
- V_{DRM} : the repetitive peak off-state voltage applied in the forward direction.
- V_{DWM} : the crest (peak) working off-state voltage applied in the forward direction.

Both the repetitive and non-repetitive voltage ratings are determined partly by the voltage limit that prevents the thyristor being driven into forward or reverse breakdown, and partly by the instantaneous energy (resulting from an increase in leakage current) that can be dissipated in the device without exceeding the rated junction temperature.

When a thyristor is to operate directly from the mains supply, it is advisable to choose a device whose repetitive peak voltage ratings V_{RRM} and V_{DRM} are at least 1.5 times the peak value of the sinusoidal supply voltage:

* The repetitive voltage is usually a function of the circuit and increases the power dissipation of the device. A non-repetitive transient voltage is usually due to an external cause and it is assumed that its effect has completely disappeared before the next transient arrives (IEC Publication 147-0).

this peak value is typically 600 V for 240 V single-phase mains and 1200 V for 415 V three-phase mains. This figure forms part of the type number; for example BTW38 600R (the final R indicates that the anode of the device is connected to the stud/heatsink).

Anode-to-cathode current ratings

The following current ratings are given in our published data (see Fig. 4). Note that the suffix T implies that the thyristor is in the on state.

- $I_{T(AV)}$: the average value of the idealised mains current waveform taken over one cycle, assuming conduction over 180°. For devices mounted on heat-sinks, the $I_{T(AV)}$ rating should be quoted for a particular mounting-base temperature T_{mb} ; our devices are generally characterised at a mounting-base temperature of at least 85°C. A device can have an artificially high current rating if the mounting-base temperature is unrealistically low; ratings with no associated mounting-base temperature should be regarded with suspicion.
- $I_{T(RMS)}$: the r.m.s. on-state current. This rating gives the maximum r.m.s. current that the thyristor can handle. It is important for large values of the form factor when the r.m.s. current rather than the average current may be the limiting rating.
- I_{TRM} : the repetitive peak forward current. This rating is the peak current that can be drawn each cycle providing that the average and r.m.s. current ratings are not exceeded.
- I_{TSM} : the non-repetitive (surge) peak forward current. This rating is the peak permitted value of non-repetitive transients, and depends on the duration of

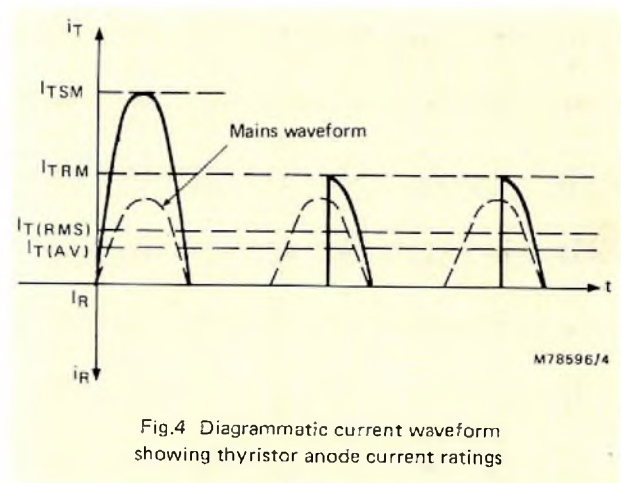


Fig.4 Diagrammatic current waveform showing thyristor anode current ratings

the surge. Our published data quotes the I_{TSM} rating for $t = 10\text{ms}$, the duration of a half-cycle of 50 Hz mains. However, American manufacturers quote I_{TSM} for $t = 8.3\text{ms}$ (half-cycle of 60 Hz mains), and thus American surge ratings should be appropriately derated (multiplied by 0.83) before comparing them with European surge ratings.

The surge rating also depends on the conditions under which it occurs. Our I_{TSM} rating is quoted under the *worst probable* conditions that is, $T_j = T_{j\text{max}}$ immediately prior to the surge, followed by reapplied $V_{RWM\text{max}}$ immediately after the surge. An unrealistically high I_{TSM} rating could be quoted if, for example, $T_j < T_{j\text{max}}$ prior to the surge and the voltage is not reapplied.

- dI_T/dt : the rate of rise of on-state current permissible after triggering. An excessive rate of rise of current causes local heating and thus damage to the device. The rate of rise of current is determined by both the supply and load impedances, and can be limited by additional series inductance in the circuit.
- I^2t : a dimensional convenience specifying the capability of a thyristor to absorb energy. This rating is required for the selection of fuses to protect the thyristor against excessive currents caused by fault conditions. It is normally only valid over the range

3 to 10ms; in our published data, a value is quoted for 10ms, in which case:

$$I^2t = \int i^2 dt, \\ = \left(\frac{I_{TSM}}{\sqrt{2}} \right)^2 \times 10^{-2} \text{ (A}^2\text{s)}. \quad (1)$$

The user matches the minimum I^2t capability of the thyristor to the worst-case I^2t let-through of a range of nominally-rated fuses to obtain a fuse that will protect the device under worst probable conditions.

Values of I^2t other than those quoted for 10ms can be estimated by referring to the appropriate published curves of non-repetitive surge current against time. For example, Fig. 5 is the non-repetitive surge current curve for a thyristor whose I^2t at 10 ms is $800\text{ A}^2\text{s}$. From Fig. 5, $I_{TS(RMS)}$ at 3 ms is 470 A and therefore I^2t at 3 ms is given by:

$$I^2t \text{ (3 ms)} = I_{TS(RMS)}^2 \times t, \\ = 470^2 \times 3 \times 10^{-3}, \\ = 662.7 \text{ A}^2\text{s}.$$

To summarise, when selecting an appropriate fuse the following conditions must be taken into account.

- 1) The fuse must have an r.m.s. current rating equal to, or less than, that of the thyristor it is to protect.

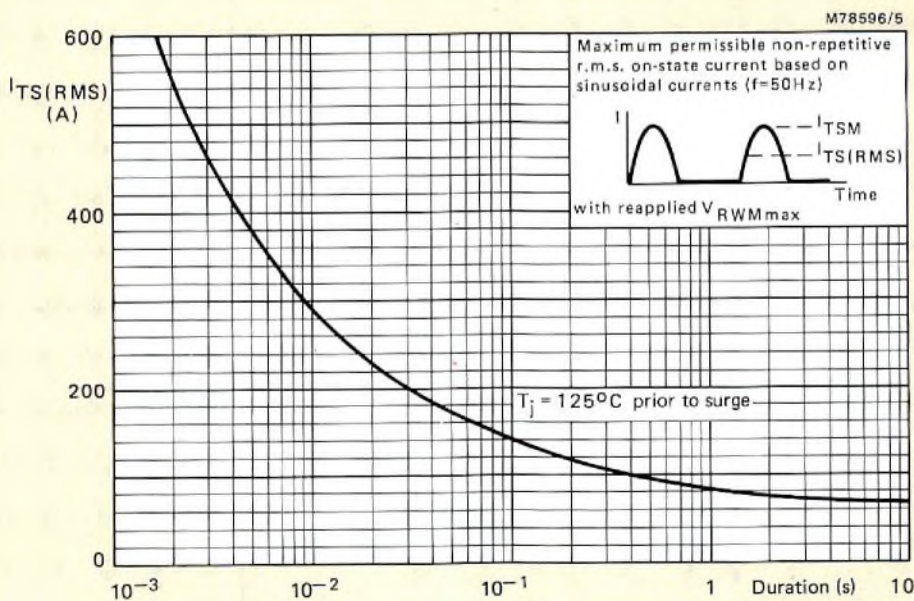


Fig.5 Non-repetitive surge current as a function of time

- 2) The I^2t at the r.m.s. working voltage must be less than that of the thyristor taken over the fuse operating time.
- 3) The arc voltage of the fuse must be less than the V_{RSM} rating of the thyristor used.

A comprehensive and detailed discussion of the fuse protection of thyristors and triacs is given in Ref. 2.

Gate-to-cathode ratings

The following gate-to-cathode ratings are given in the published data.

- V_{RGM} : the gate peak reverse voltage.
- $P_{G(AV)}$: the mean power dissipation, averaged over a 20 ms period.
- P_{GM} : the peak power dissipation.

The gate-to-cathode power ratings should not be exceeded if over-heating of the gate-cathode junction is to be avoided.

Temperature ratings

Two temperature ratings are given in the published data.

- T_{stg} : the storage temperature. Both maximum and minimum values of the temperature at which a device can be stored are given.
- T_j : the junction temperature. This is one of the principal semiconductor ratings since it limits the maximum power that a device can handle. The junction temperature rating quoted in our published data is the highest value of junction temperature at which the device may be continuously operated to ensure a long life.

As semiconductor manufacturing techniques improve, so the junction temperature ratings of some new devices can be increased. However, high junction temperature ratings should not be quoted simply on the assumption that the user will derate devices appropriately. Semiconductor failure mechanisms are temperature dependent and continuous operation at an artificially high $T_{j\max}$ is likely to result in reduced life.

This practice is distinct from the normal derating of a semiconductor device that a user may choose to perform in order to increase the reliability of a circuit.

Thermal characteristics

The following thermal resistances and impedances are given in our data.

- $R_{th\ j-a}$: the thermal resistance between the junction of the thyristor and the ambient (assumed to be the surrounding air).
- $R_{th\ j-mb}$: the thermal resistance between the junction and mounting-base of the device.
- $R_{th\ mb-h}$: the thermal resistance between the mounting-base of the device and the heatsink (contact thermal resistance).
- $Z_{th\ j-mb}$: the transient thermal impedance between the junction and mounting-base of the device. The value given in the published data is for non-repetitive conditions and a particular pulse duration. Under pulse conditions, thermal impedances rather than thermal resistances should be considered. Higher peak power dissipation is permitted under pulse conditions since the materials in a thyristor have a definite thermal capacity, and thus the critical junction temperature will not be reached instantaneously, even when excessive power is being dissipated in the device.

The published data also contains graphs of $Z_{th\ j-mb}$ against time (for non-repetitive conditions) such as Fig. 6.

The values of the various thermal resistances between the thyristor junction and the surroundings must be considered to ensure that the junction temperature rating is not exceeded.

The heat generated in a semiconductor chip flows by various paths to the surroundings. Fig. 7 shows the various thermal resistances to be taken into account in this process. With no heatsink, the thermal resistance from the mounting-base to the surroundings is given by $R'_{th\ mb-a}$. When a heatsink is used, the heat loss direct to the surroundings from the mounting-base is negligible owing to the relatively high value of $R_{th\ mb-a}$ and thus:

$$R_{th\ mb-a} = R_{th\ mb-h} + R_{th\ h-a} \quad (2)$$

Where appropriate, our published data contains power nomograms such as that in Fig. 8. These nomograms relate the total power dissipated in the thyristor P , the average forward current $I_{T(AV)}$, the ambient temperature T_{amb} , and the thermal resistance $R_{th\ mb-a}$, with the form factor a as a parameter. They enable the designer to work out the required mounting arrangement from the conditions under which the thyristor is to be operated.

Usually, the nomograms are designed for use in 50 Hz

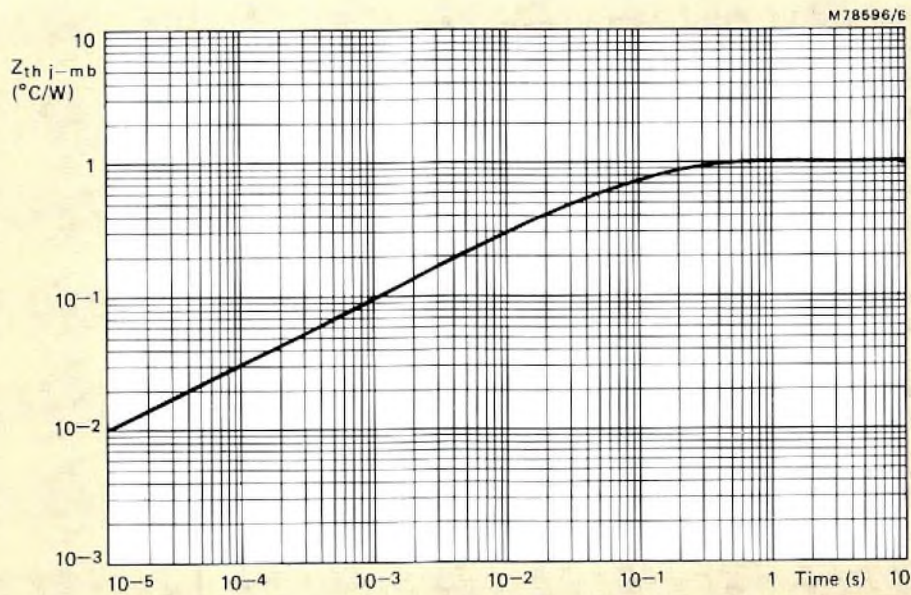


Fig.6 Thermal impedance between the junction and mounting-base as a function of time

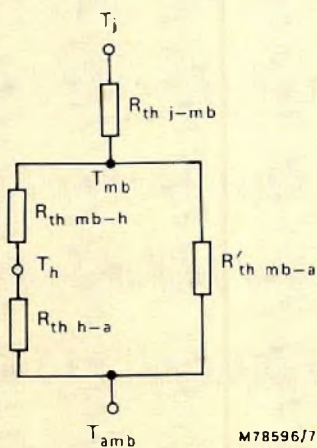


Fig.7 Heat flow paths

- 3) Starting from the appropriate value of $I_{T(AV)}$ on a nomogram such as Fig. 8, move vertically upwards to intersect the appropriate form factor curve (interpolating if necessary).
- 4) This intersection gives the power dissipated in the thyristor on the left-hand axis of the nomogram and the mounting-base temperature on the right-hand axis.
- 5) Moving horizontally across from this intersection to the appropriate value of ambient temperature gives the required mounting-base to ambient thermal resistance $R_{th\ mb-a}$.
- 6) The required heatsink thermal resistance $R_{th\ h-a}$ can now be calculated from Eq. 2 since the mounting-base to heatsink thermal resistance $R_{th\ mb-h}$ is given in the published data.

sinusoidal applications, when the procedure below should be followed.

- 1) Determine the values of $I_{T(AV)}$ and $I_{T(RMS)}$ for the relevant application.
- 2) Determine the form factor, which is given by:

$$a = \frac{I_{T(RMS)}}{I_{T(AV)}} \quad (3)$$

Example

A thyristor (to which Fig. 8 applies) is operated at an average forward current $I_{T(AV)}$ of 12 A and an r.m.s. forward current $I_{T(RMS)}$ of 19.2 A. The maximum anticipated ambient temperature is 25°C. Now, Eq. 3 gives:

$$a = \frac{19.2}{12} = 1.6.$$

Thus, Fig. 8 gives the power $P = 20\text{ W}$ and the mounting-base temperature $T_{mb} = 105^\circ\text{C}$. Also, at this power and

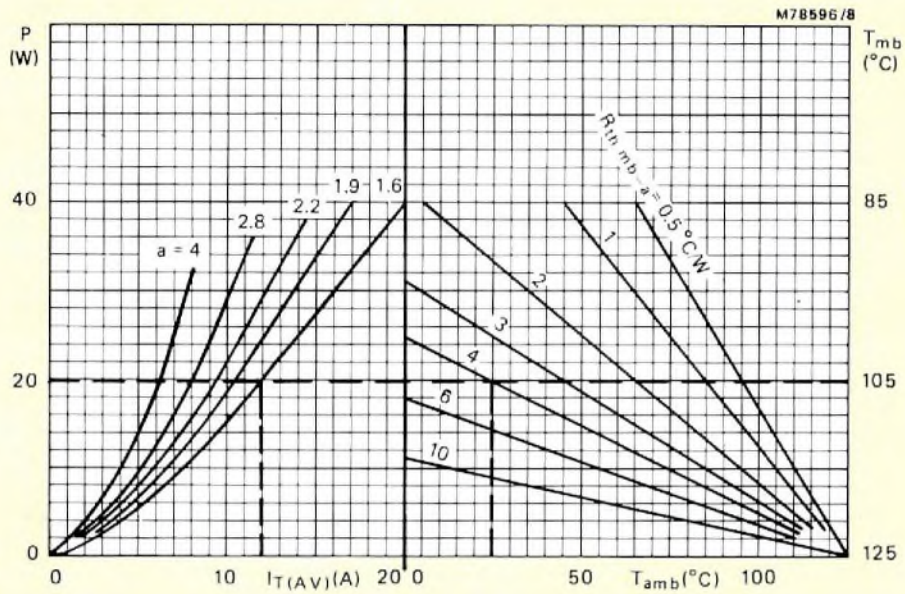


Fig.8 Nomogram for obtaining the appropriate value of thermal resistance between mounting-base and ambient for a given value of average forward current, form factor, and ambient temperature

an ambient temperature of 25°C, Fig. 8 gives the value of $R_{th\ mb-a}$ to be 4°C/W.

The published data gives the value of $R_{th\ mb-h}$ (using a heatsink compound) to be 0.2°C/W and then Eq. 2 gives:

$$R_{th\ h-a} = 4 - 0.2 = 3.8^{\circ}\text{C/W.}$$

Mounting torque

Two values of mounting torque (for stud-mounted devices) are given in the published data. A minimum value is quoted below which the contact thermal resistance rises owing to poor contact, and a maximum value is given above which the contact thermal resistance again rises owing to deformation of the stud or cracking of the crystal.

The surface of a device case and a heatsink cannot be perfectly flat, and thus contact will take place on several points only with a small air-gap over the rest of the contact area. The use of a soft substance to fill this gap will lower the contact thermal resistance. We recommend the use of proprietary heatsinking compounds which consist of a silicone grease loaded with an electrically insulating and good thermal conducting powder such as alumina. The use of insulating washers and heatsinking compounds (for TO-220 devices) is discussed in detail in Ref. 3.

Anode-to-cathode characteristics

The following anode-to-cathode characteristics are included in the published data.

- V_T : the forward voltage when the thyristor is conducting. This characteristic is measured at particular values of forward current and junction temperature. The junction temperature is usually low ($T_j = 25^{\circ}\text{C}$, for example) since this is the worst case, and the measurement must be performed under pulse conditions to maintain the low junction temperature. The published data also contains curves of forward current against forward voltage, usually for two values of the junction temperature: 25°C and $T_{j\ max}$ (see Fig. 9).
- dV_D/dt : the rate of rise of off-state voltage that will not trigger any device. This characteristic is given at a particular junction temperature $T_{j\ max}$ and forward voltage $V_D = \frac{2}{3} V_{DRM\ max}$.

The values of dV_D/dt quoted in our published data are normally specified assuming an exponential waveform. This facilitates the design of RC suppression or 'snubber' circuits for device protection, when required. Fig.10 illustrates the definition of dV_D/dt . The final voltage applied to the device V_{DM} is chosen as $\frac{2}{3} V_{DRM\ max}$ and the junction temperature is $T_{j\ max}$.

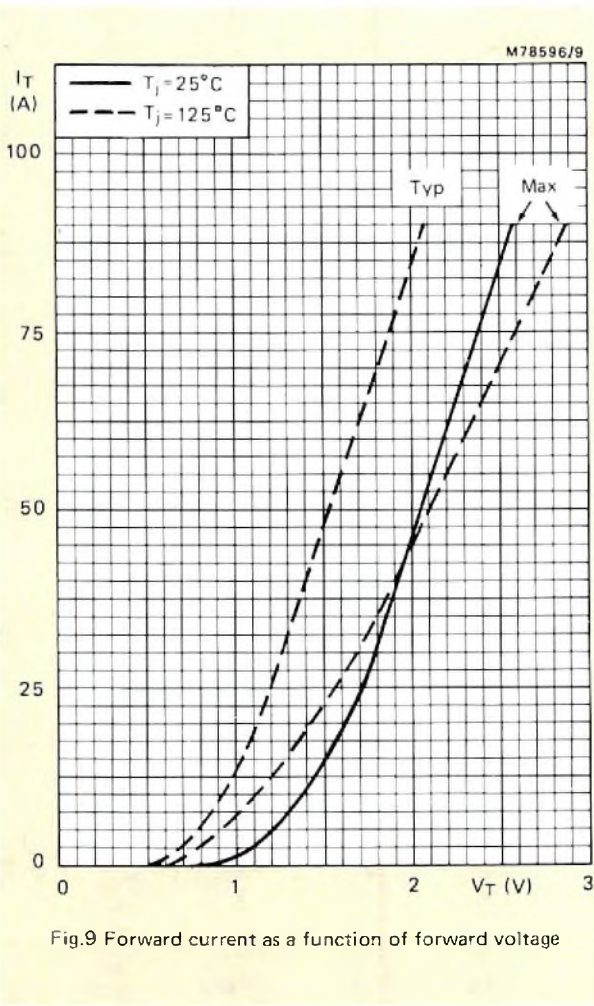


Fig.9 Forward current as a function of forward voltage

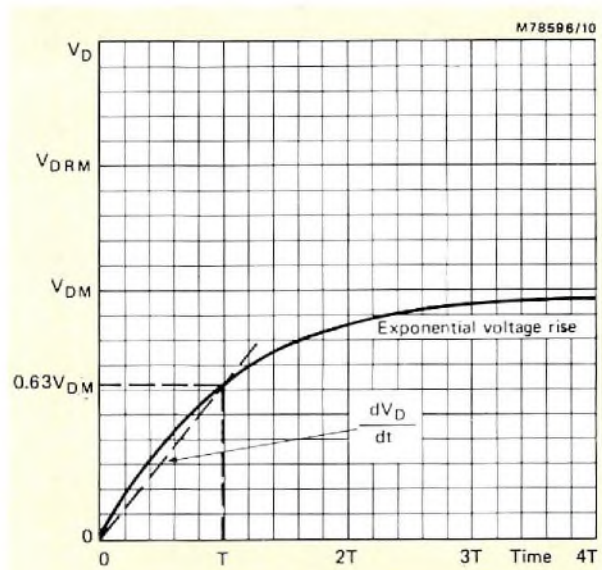


Fig.10 Definition of the rate of off-state voltage dV_D/dt

Fig. 10 shows that dV_D/dt is given by the expression:

$$dV_D/dt = \frac{0.63 V_{DM}}{T}$$

where T is the exponential time constant;

$$= \frac{0.63 \times \frac{2}{3} V_{DRM \max}}{T}$$

$$= \frac{0.42 V_{DRM \max}}{T} \text{ V}/\mu\text{s}. \tag{4}$$

Note that thyristors are available with $dV_D/dt = 1000 \text{ V}/\mu\text{s}$; they are distinguished from normal types (typically 200 to 300 $\text{V}/\mu\text{s}$) by the letter C added to the type number (for example, BTW92 800RC).

The dV_D/dt capability of a thyristor increases as the junction temperature decreases. Thus curves such as Fig. 11a are provided in the published data so that designers can uprate devices operated at lower junction temperatures.

The dV_D/dt characteristic can also be increased by operating the device at a low supply voltage. Thus the published data also contains curves such as Fig. 11b which shows how dV_D/dt increases as the ratio $V_{DM}/V_{DRM \max}$ decreases.

Note that V_{DM} is unlikely to be greater than $\frac{2}{3} V_{DRM \max}$ (often it cannot, owing to the restriction of $V_{DWM \max}$) and therefore the fact that dV_D/dt approaches zero as V_{DM} increases above the value of $\frac{2}{3} V_{DRM \max}$ does not cause problems.

Thus the information in our published data allows the designer to arrive at a value of dV_D/dt which is appropriate to actual circuit conditions.

- I_R : the reverse current. This characteristic is given for the worst probable conditions; that is, the reverse voltage $V_R = V_{RWM \max}$ and a high junction temperature.
- I_D : the off-state current. This characteristic is again given for the worst probable conditions; that is, the forward voltage $V_D = V_{DWM \max}$ and a high junction temperature.
- I_L : the latching current (see Fig. 2). This characteristic should be quoted for a particular value of the junction temperature.
- I_H : the holding current (see Fig. 2). This characteristic should again be quoted for a particular value of the junction temperature.

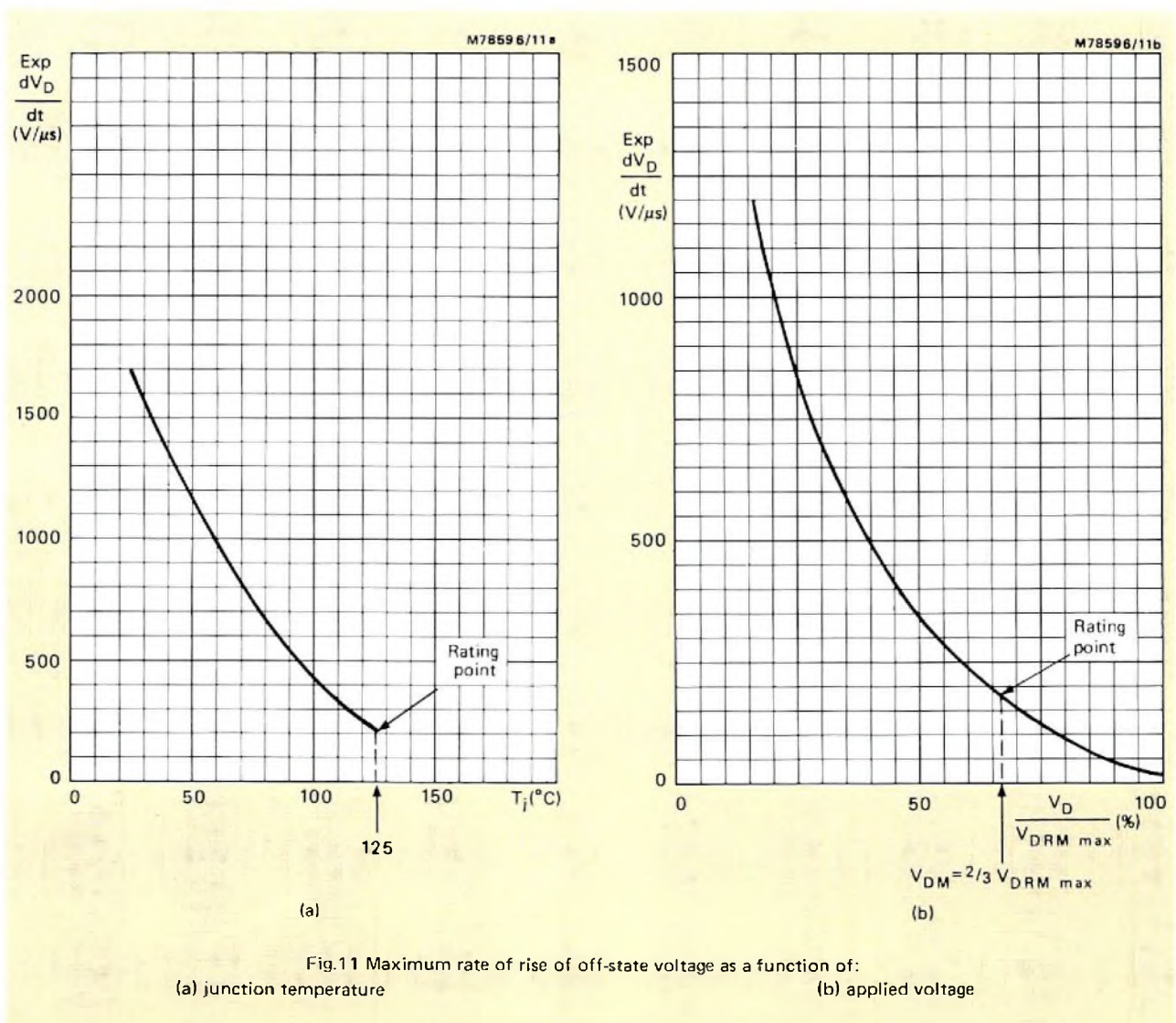


Fig.11 Maximum rate of rise of off-state voltage as a function of:
 (a) junction temperature
 (b) applied voltage

Gate-to-cathode characteristics

The following gate-to-cathode characteristics are given in the published data.

- V_{GT} : the gate-to-cathode voltage that will trigger all devices. This characteristic should be quoted for particular values of applied voltage V_D and junction temperature.
- I_{GT} : the gate-to-cathode current that will trigger all devices. This characteristic should again be quoted for particular values of applied voltage V_D and junction temperature.
- V_{GD} : the gate-to-cathode voltage that will not trigger any device. This characteristic should be quoted under the worst probable conditions; that is, forward voltage $V_D = V_{DRM \max}$ and junction temperature $T_j = T_{j \max}$.

A gate drive circuit must be designed which is capable of supplying at least the required minimum voltage and current without exceeding the maximum power rating of the gate junction.

In some instances, the published data contains curves such as Figs. 12 and 13. In practice, a load line is constructed on Fig. 12 from a value on the voltage axis given by the open-circuit voltage of the trigger pulse supply, through a point whose coordinates are as follows: typically five times the minimum gate trigger current I_{GT} at the lowest junction temperature $T_{stg \min}$ and the minimum gate trigger voltage V_{GT} . The current value can be estimated from the expanded graph of the possible triggering area (Fig. 13). The slope of this load line defines the required source impedance of the drive circuit and, by reference to the power curves, the maximum permitted pulse duty cycle can be determined. Note that the load line must *not* intersect the maximum power curve.

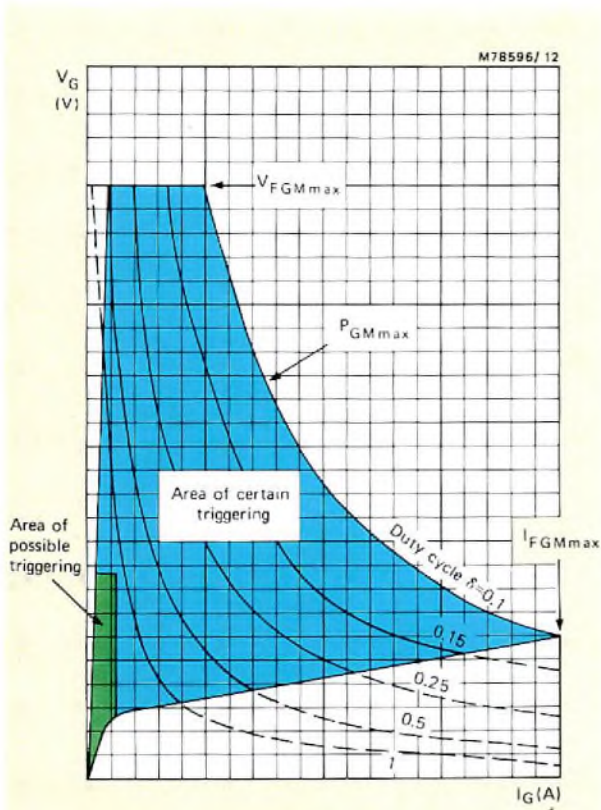


Fig.12 Gate characteristic (forward voltage against forward current) with curves applicable to the average power dissipation $P_{G(AV)} = P_{G(AV) max}$

When curves such as Figs. 12 and 13 are not included in the published data, graphs such as Figs. 14a and 14b (which relate the minimum values of V_{GT} and I_{GT} for safe triggering to the junction temperature) are provided. In this case, the following design procedure is recommended, using the power curves shown in Figs. 15a and 15b.

- 1) Determine the maximum average gate power dissipation $P_{G(AV)}$ from the published data (normally 0.5, 1.0, or 2.0 W) and then select the appropriate power curve; that is, Fig. 15a for 0.5 W, and Fig. 15b for 1.0 or 2.0 W.
- 2) Estimate the minimum ambient temperature at which the device will operate, and then determine the minimum values of V_{GT} and I_{GT} from curves such as Figs. 14a and 14b in the published data. Note that it is assumed that at switch-on $T_j = T_{amb}$.
- 3) Determine the minimum open-circuit voltage of the trigger pulse drive circuit and select the best scale on the chosen power curve (Fig. 15a or 15b) to accommodate this voltage.
- 4) Plot the point on the power curve whose coordinates are given by $V_{GT min}$ and $5 \times I_{GT min}$. Construct a load line from the value on the voltage axis given by the open-circuit voltage of the trigger pulse supply through the above point. The slope of this load line

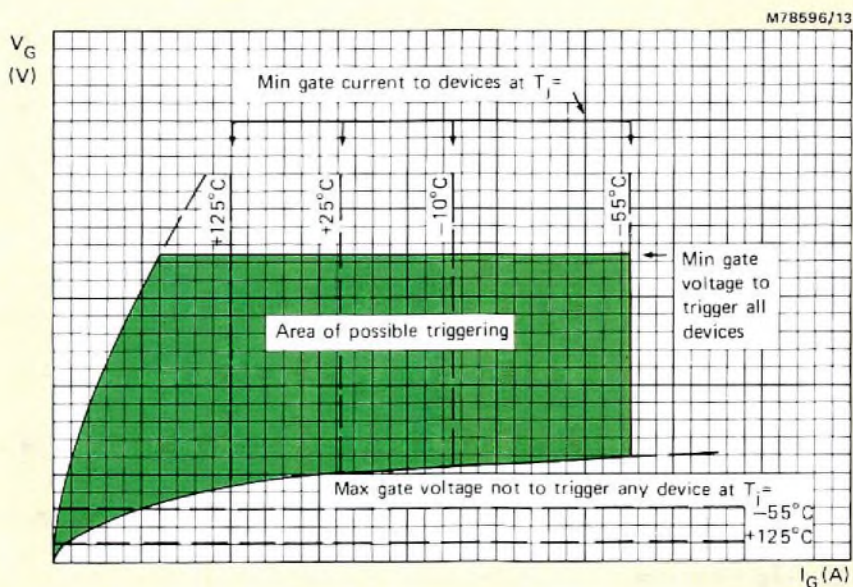


Fig.13 Expanded section (low voltages and currents) of Fig. 12

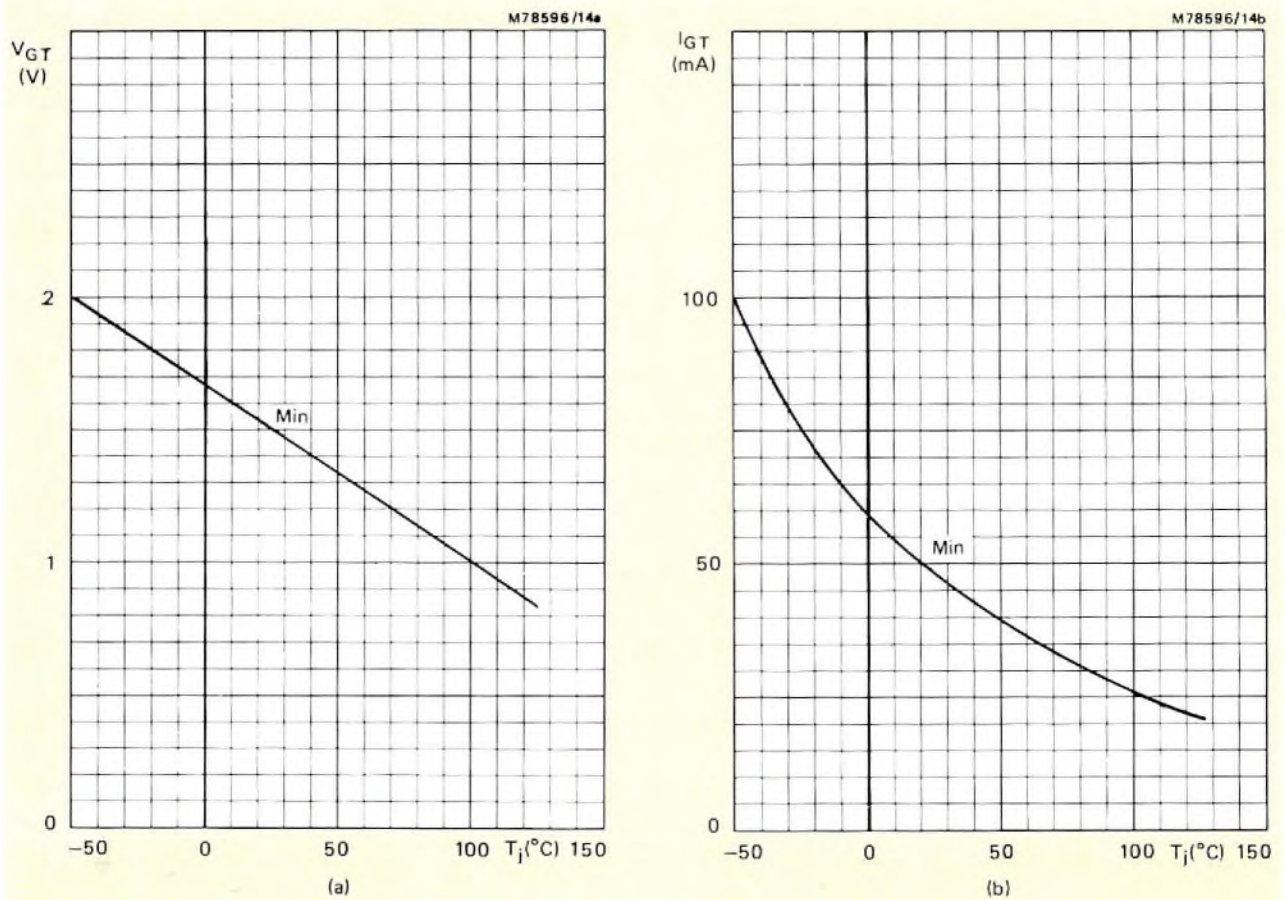


Fig. 14 Relationship between gate characteristics and junction temperature:

(a) minimum gate-to-cathode voltage that will trigger all devices V_{GT}

(b) minimum gate-to-cathode current that will trigger all devices I_{GT}

gives the maximum allowable source resistance for the drive circuit.

- 5) Check the power dissipation as follows.
 - (a) The load line must not intersect the curve for the maximum peak gate power $P_{GM \max}$.
 - (b) The load line must also not intersect the curve which represents the maximum average gate power $P_{G(AV)}$ modified by the pulse mark-space ratio. For instance, in Fig. 15b for a thyristor with $P_{G(AV)} = 1 \text{ W}$, the 4 W curve can be used for a 1:4 mark-space ratio ($\delta = 0.125$).

An illustration of how the above design procedure operates is given by the following example.

Example

A thyristor has the V_{GT}/T_j and I_{GT}/T_j characteristics shown in Figs. 14a and 14b, and $P_{G(AV)} = 0.5 \text{ W}$ and $P_{G \max} = 5 \text{ W}$. A suitable trigger circuit using a TT61 trigger transformer and operating at a $T_{\text{amb min}}$ of

-10°C is to be designed. The procedure is as follows.

- 1) Fig. 15a is selected, as $P_{G(AV)}$ is 0.5 W.
- 2) From Fig. 14a $V_{GT \min} = 1.75 \text{ V}$, and from Fig. 14b $I_{GT \min} = 66 \text{ mA}$.
- 3) The characteristics of the TT61 are shown in Fig. 16. At minimum supply (18 V), the open-circuit voltage is seen to be 4.5 V; the outer scales of Fig. 15a are therefore applicable.
- 4) Point A is plotted at 4.5 V. Point B is plotted at the coordinates $V_{GT \min}$ and $5 \times I_{GT \min}$, that is at 1.75 V and 330 mA, and load line ABC is constructed as shown. Note that point C is at 570 mA. The worst-case load line for the TT61 is AC', where C' is at 610 mA. The design therefore lies within the limits set by the TT61 ratings and the circuit will perform as required.

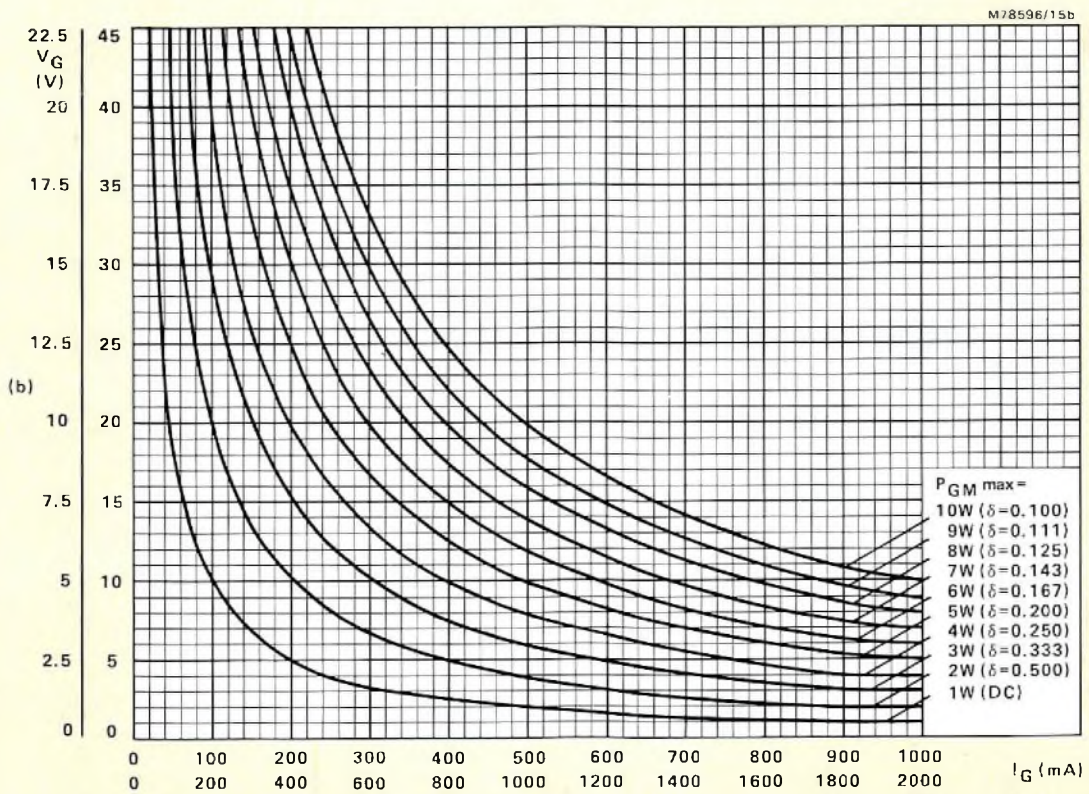
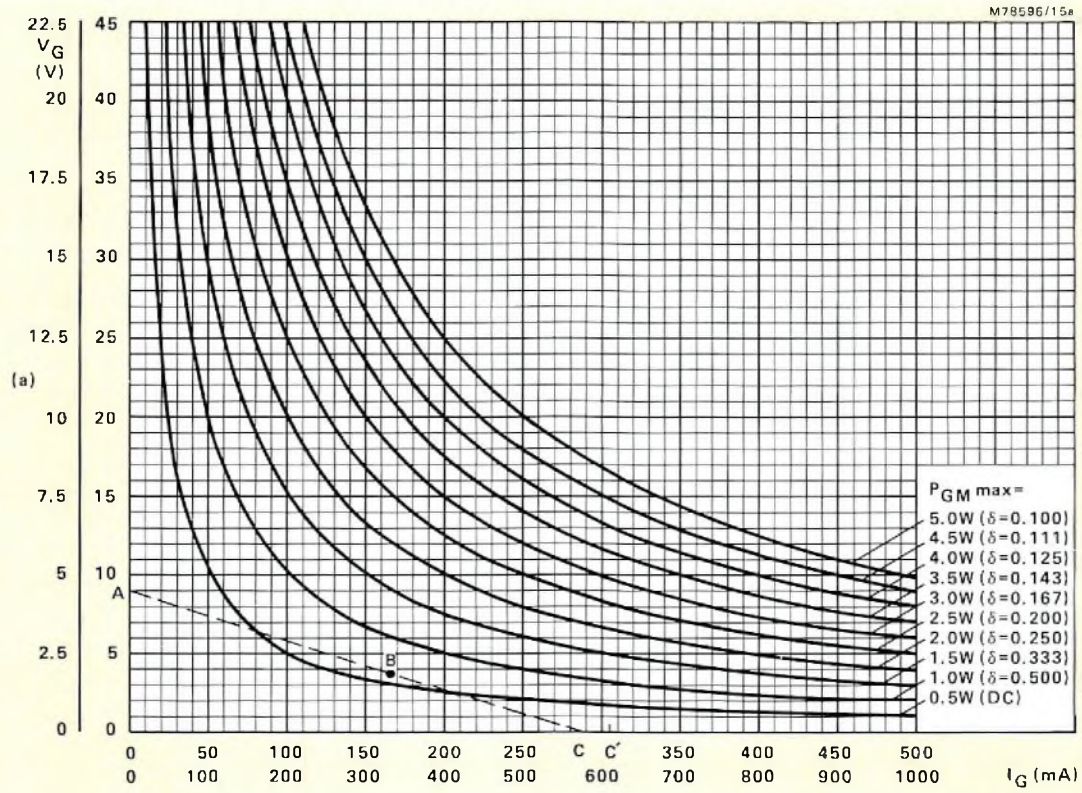


Fig.15 Design procedure power curves:

(a) $P_{G(AV)} = 0.5W$

(b) $P_{G(AV)} = 1.0$ or $2.0W$ (for $2.0W$, the current scales should be multiplied by 2 and the power curves then have twice their marked value)

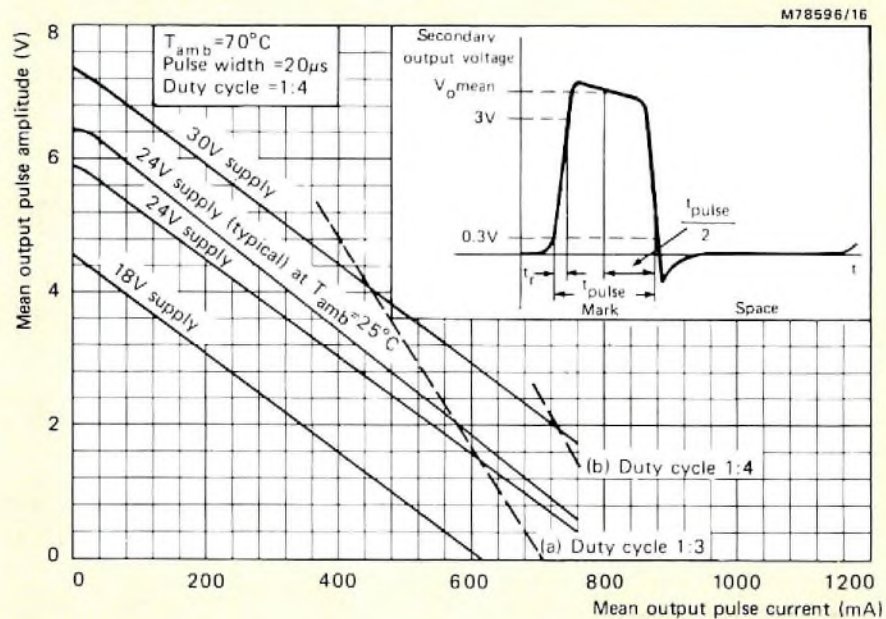


Fig.16 Worst-case regulation curves for TT61 trigger transformer. Curves (a) and (b) show dissipation limitation (80Ω series resistor)

5) (a) As required, the load line does *not* intersect the 5 W curve.

(b) From Fig. 16, the duty cycle is 1:4; that is, $\delta = 0.25$ which is represented by the 2 W curve in Fig. 15a. Again, as required, the load line ABC does *not* intersect this curve.

Thus the TT61 may be used to trigger the thyristor under the specified conditions.

Switching characteristics

Two important switching characteristics are usually included in our published data. They are the gate-controlled turn-on time t_{gt} (divided into a delay time t_d and a rise time t_r) and the circuit-commutated turn-off time t_q .

Gate-controlled turn-on time t_{gt}

Anode current does not commence flowing in the thyristor at the instant that the gate current is applied. There is a period which elapses between the application of the trigger pulse and the onset of the anode current which is known as the delay time t_d (see Fig. 17). The time taken for the anode voltage to fall from 90% to 10% of its initial value is known as the rise time t_r . The sum of the delay time and the rise time is known as the gate-controlled turn-on time t_{gt} .

The gate-controlled turn-on time depends on the conditions under which it is measured, and thus the

following conditions should be specified in the published data.

- Off-state voltage V_D ; usually $V_D = V_{DWM \max}$.
- On-state current I_T .
- Gate trigger current I_{GT} ; high gate currents reduce the turn-on time.
- Rate of rise of gate trigger current dI_G/dt ; high values reduce turn-on time.
- Junction temperature T_J ; high junction temperatures reduce turn-on time.

Circuit-commutated turn-off time

When a thyristor has been conducting and is reverse-biased, it does not immediately go into the forward blocking state; minority charge carriers have to be cleared away by recombination and diffusion processes before the device can block reapplied off-state voltage. The time from the instant that the anode current passes through zero to the instant that the thyristor is capable of blocking reapplied off-state voltage is defined as the circuit-commutated turn-off time t_q (see Fig. 18).

The following conditions should be given when this characteristic is quoted.

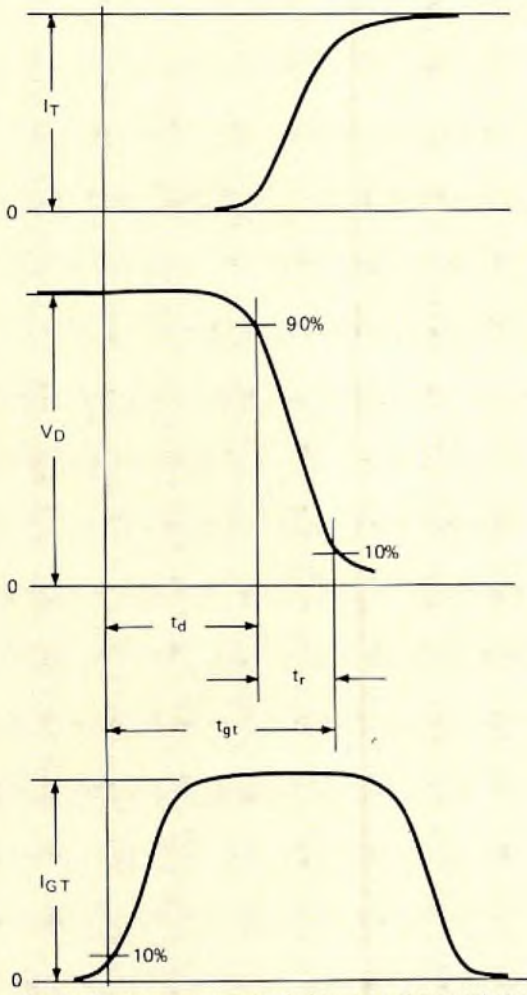


Fig.17 Thyristor gate-controlled turn-on characteristics

- On-state current I_T ; high on-state currents increase the turn-off time.
- Reverse voltage V_R ; low reverse voltages increase the turn-off time.
- Rate of fall of anode current $-dI_T/dt$; high rates increase the turn-off time.
- Rate of rise of reapplied off-state voltage dV_D/dt ; high rates increase the turn-off time.
- Junction temperature T_j ; high temperatures increase the turn-off time.
- Gate bias V_g , negative voltages decrease the turn-off time.

TRIACS

The triac, or bi-directional triode thyristor, is a device that can be used to pass or block current in either direction; it is therefore an a.c. power control device. It is equivalent to two thyristors in anti-parallel with a common gate electrode. However, it only requires one heatsink compared to the two heatsinks required for the anti-parallel thyristor configuration. Thus the triac saves both cost and space in a.c. applications.

Fig. 19 shows the triac circuit symbol and a simplified cross-section of the device. The triac has two 'main terminals' MT1 and MT2 (the load connections) and a single gate. The main terminals are connected to both p and n regions since current can be conducted in both directions. The gate is similarly connected, since a triac can be triggered by both negative and positive pulses.

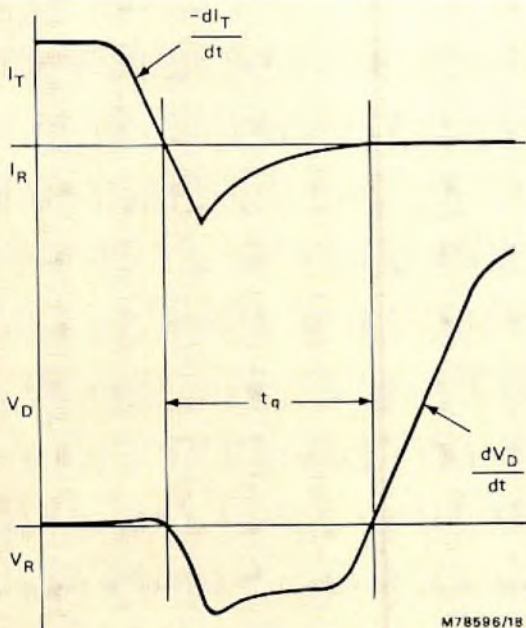


Fig.18 Thyristor turn-off characteristics

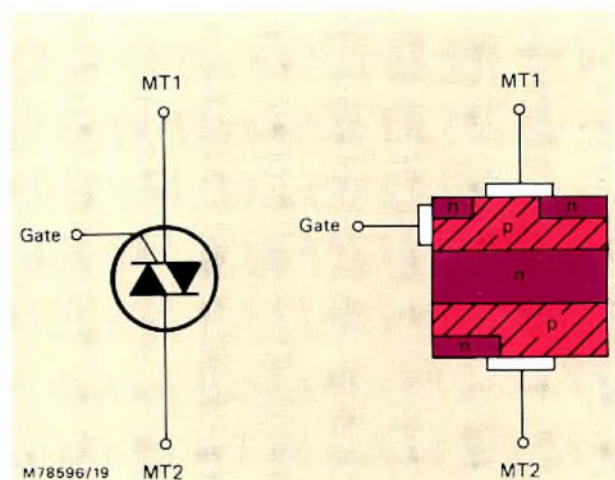


Fig.19 Triac circuit symbol and simplified cross-section

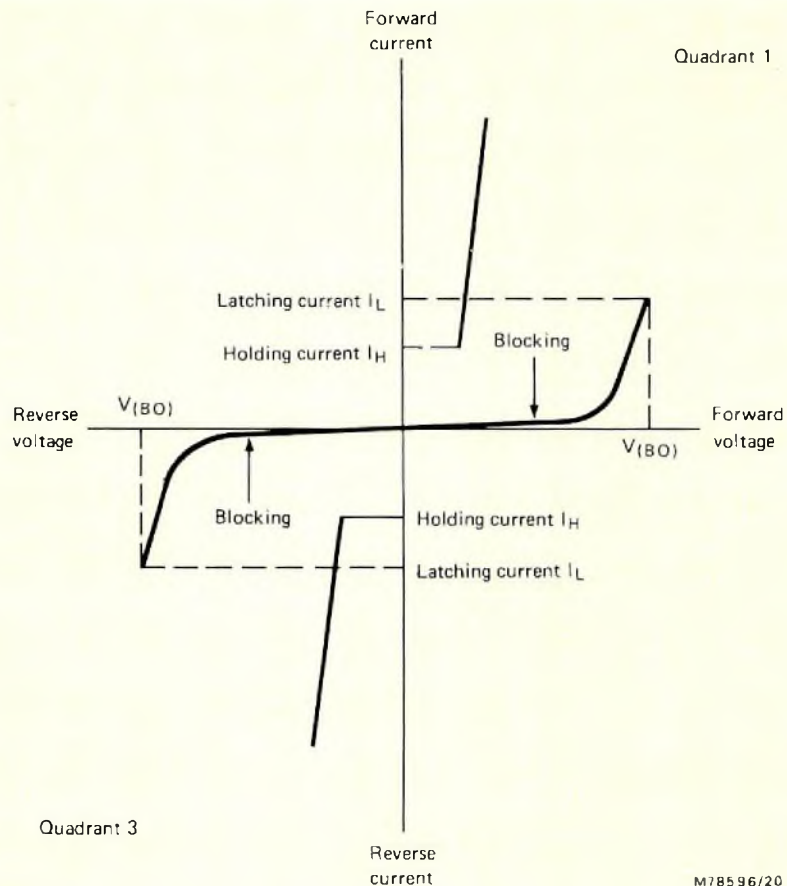


Fig.20 Triac static characteristic

The voltage/current characteristic resembles that of a thyristor: Fig. 20 shows the triac static characteristic which consists of two 'positive' parts of the thyristor characteristic. When terminal 2 of the triac is positive with respect to terminal 1, the triac operates in quadrant 1 of the coordinate axes. If the triac is not triggered, the small leakage current increases as the voltage increases until the breakover voltage $V_{(BO)}$ is reached and the triac then turns on. As with the thyristor, however, the triac can be triggered below $V_{(BO)}$ by a gate pulse, provided that the current through the device exceeds the latching current I_L before the trigger pulse is removed.

When terminal 1 is positive with respect to terminal 2, the triac operates in quadrant 3 of the coordinate axes. The blocking and conducting characteristics are similar to those in quadrant 1 but the polarities are reversed. The triac can be triggered in both quadrants 1 and 3 by either negative or positive pulses on the gate; the value of the latching current depends on the polarity of the gate pulse.

The triac, like the thyristor, has holding current values below which conduction cannot be maintained.

TRIAC RATINGS AND CHARACTERISTICS

The ratings and characteristics of the triac are similar to those of the thyristor discussed previously, except that the triac does not have any reverse voltage ratings (a reverse voltage in one quadrant is the forward voltage in the opposite quadrant). However, one characteristic requires special attention when choosing triacs: the rate of reapplied voltage that the triac will withstand without uncontrolled turn-on.

If a triac is turned off by simply rapidly reversing the supply voltage, the recovery current in the device would simply switch it on in the opposite direction. To guarantee reduction of the current below its holding value, the supply voltage must be reduced to zero and held there for a sufficient time to allow the recombination of any stored charge. To ensure turn-off, the rate of fall of current during the commutation interval (turn-off period) and the rate of rise of reapplied voltage after commutation must both be restricted. An excessive rate of fall of current creates a large number of residual charge carriers which are then available to initiate turn-on when the voltage across the triac rises.

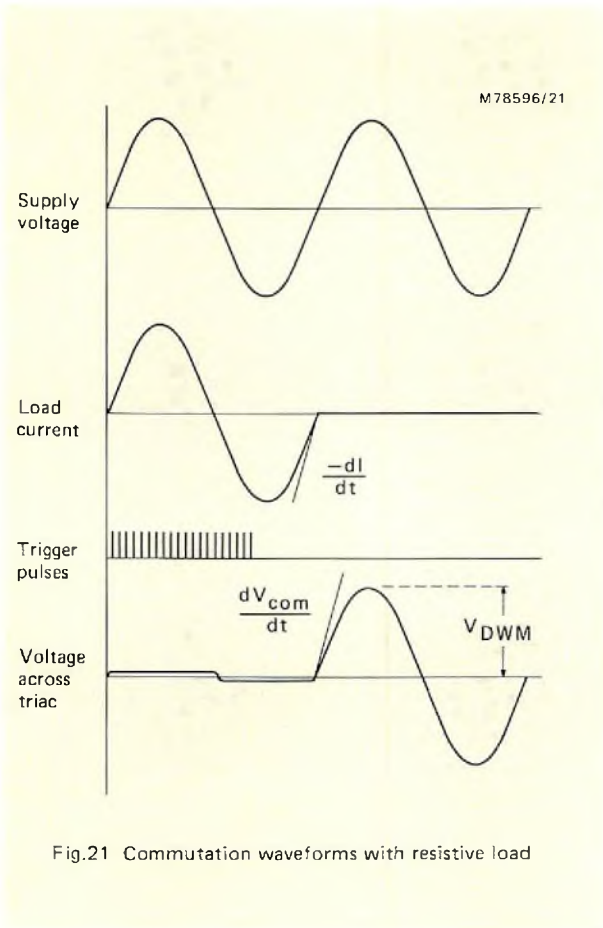


Fig.21 Commutation waveforms with resistive load

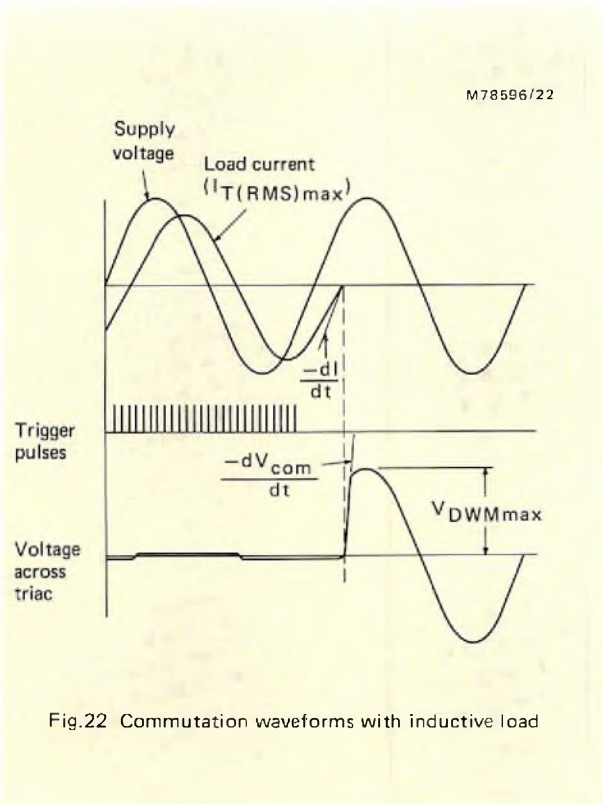


Fig.22 Commutation waveforms with inductive load

Thus, with supply frequencies up to 400 Hz and a sinusoidal waveform, commutation does not present any problems when the load is purely resistive, since the current and voltage are in phase (see Fig.21). However, with an inductive load (Fig.22) the current lags behind the voltage and consequently commutation can present special difficulties. When the current has fallen to zero after a triac has been conducting in one direction, the supply voltage in the opposite direction will have already reached a significant value. The triac will then switch on immediately unless dV/dt is held less than that quoted in the published data by suitable circuit design.

The rate of rise of commutating voltage which will not cause the device to trigger spuriously is known as the dV_{com}/dt and is an essential part of triac published data. However, dV_{com}/dt is meaningless unless the conditions to which it is applicable are also provided, particularly the rate of fall of on-state current $-dI_T/dt$. The other conditions which should be specified are:

- junction temperature T_j (or T_{mb} at $I_{T(RMS)max}$),
- reapplied off-state voltage V_D ,
- r.m.s. current $I_{T(RMS)}$.

Our published data also contains graphs such as Fig.23 which relate dV_{com}/dt to $-dI_T/dt$ with the junction temperature as a parameter. The characteristic dV_{com}/dt is specified in the published data under the worst probable conditions; that is:

- $T_{mb} = T_{mbmax}$,
- $V_D = V_{DWMmax}$,
- $I_{T(RMS)} = I_{T(RMS)max}$.

To enable designers to economise as far as possible, we offer different values of $-dI_T/dt$ (at the same dV_{com}/dt) for some of our triac families. These different values are differentiated by the suffixes G, H, or J to the type number; Table 1 shows the meaning of these suffixes.

TABLE 1
Triac type number suffixes

Suffix	$-dI_T/dt$ (approx)
G	$\frac{1}{2}I_{T(RMS)max}/ms$
H	$I_{T(RMS)max}/ms$
J	$2I_{T(RMS)max}/ms$

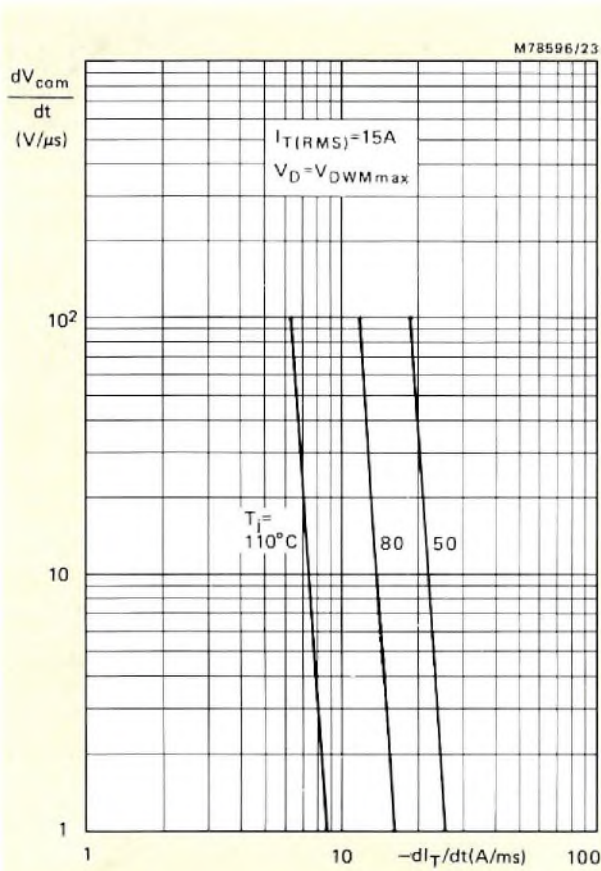


Fig.23 Rate of rise of commutating voltage as a function of the rate of fall of on-state current, with junction temperature as a parameter. Other conditions are: r.m.s. current $I_T(RMS) = I_T(RMS)_{max}$, and reapplied off-state voltage $V_D = V_{DWMmax}$

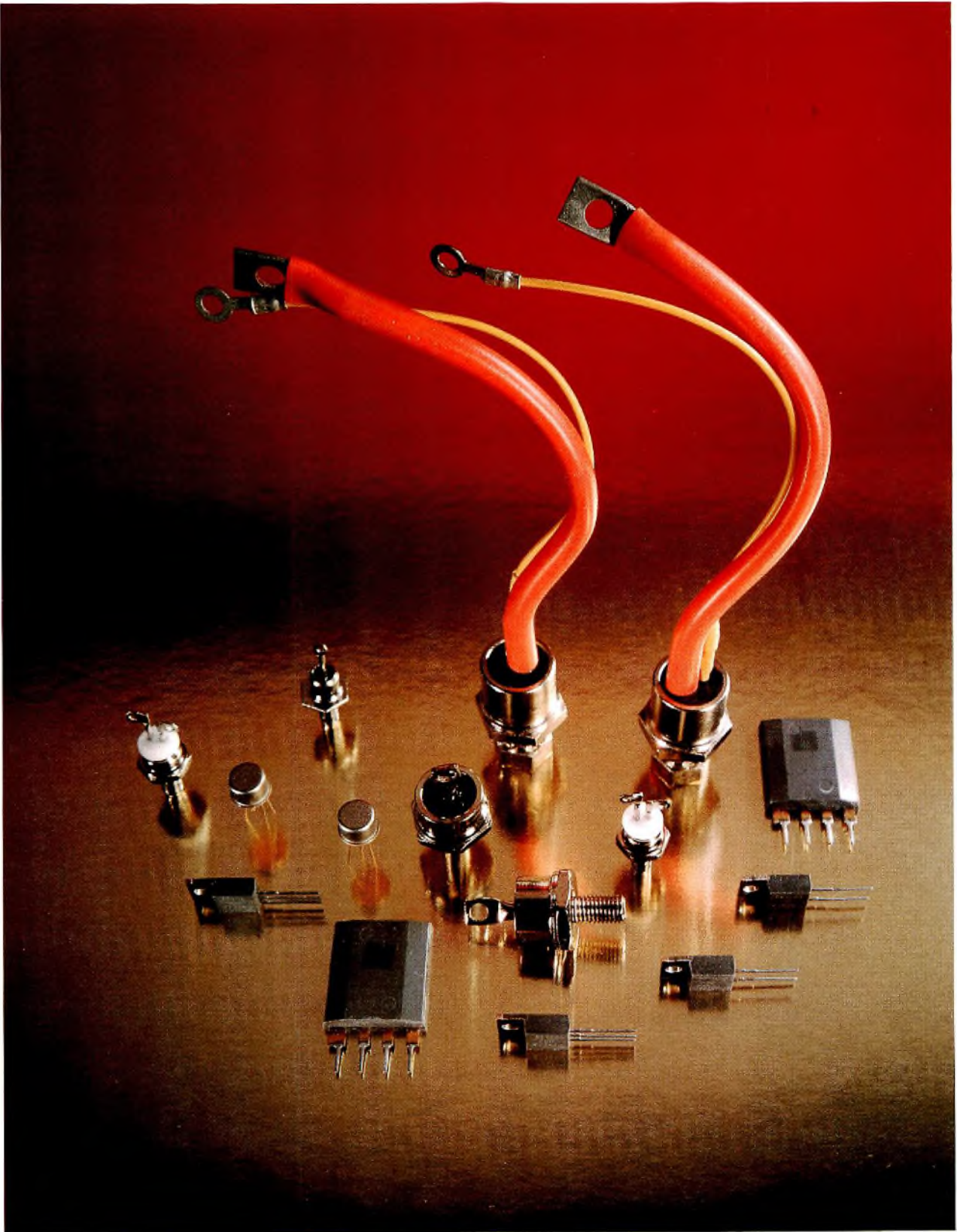
Triacs with H and J suffixes are suitable for inductive loads with a power factor of up to 0.7, while with resistive loads the flexibility of our range allows a more economical device, suffix G, to be used with complete confidence.

ACKNOWLEDGEMENT

We would like to thank B. G. Starr of the Mullard Application Laboratory, Mitcham, for technical assistance with this article.

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2. HAMPSON, L., 'Fuse protection of semiconductor diodes, thyristors, and triacs', *Mullard Technical Communications*, Vol. 13, No. 128, October 1975, pp. 302 to 319.
3. 'Thermal resistance of insulators for TO-220 devices', *Technical Note 107, TP1694, Mullard Limited, 1978; Philips Technical Note 101, ordering code 9398 010 10011.*



Some examples from our extensive range of power devices for control applications. The triacs and thyristors shown here have excellent performance characteristics and high reliability. Conservatively rated, they offer the highest guarantee of satisfactory operation even under conditions of heavy overloads. The foregoing article explains how you can get the best out of them.

Publications news

Multitext

Television-based text display systems are now receiving increasing attention throughout the world. This comprehensive full-colour publication describes a system, using our range of LSI circuits, for the reception, control, and display of both teletext and viewdata information. Full details are given of two alternative remote control systems, each based on only two ICs, a teletext decoder using four ICs and a memory block, and a combined teletext/viewdata receiver requiring a further two ICs. The way in which the teletext decoder is interfaced to the tv receiver is described, and the application of the teletext ICs in VDUs is briefly discussed.

TDA1008 frequency-dividing and gating IC for electronic organs

The popularity of electronic organs has been boosted in recent years by the rapid expansion of the home entertainment market. This 16-page publication describes the TDA1008, an advanced IC which enables the organ designer to provide effects such as sustain, percussion, fifth coupling, and many others without any significant increase in circuit complexity. Some popular organ systems are briefly described and compared with a simplified system using TDA1008 ICs.

A 16K PROM – its design and application

This 4-page Technical Note outlines some of the considerations behind the design of high-density high-speed programmable read-only memories, in particular the Signetics 82S190/191, a 16 384-bit PROM organised as $2K \times 8$ bits. Fusing reliability and the design of the diode array are discussed, and brief mention is made of the possible use of high-density PROMs in sequential controllers.

TDA1022 – an integrated bucket-brigade delay line for audio signal processing

Artificial delay has many potential applications in the electronic production and reproduction of music and speech, including the provision of equalisation, simulated reverberation, and special effects such as vibrato and chorus. The TDA1022 is an integrated 512-stage bucket-brigade delay line providing wideband artificial delay for a variety of audio applications. In this 24-page publication, the operation and characteristics of the TDA1022 are discussed and a number of practical delay circuits are given.

Single-chip multiprocessor arbiter using the Signetics 82S105 FPLS

The Signetics Field Programmable Logic Sequencer (FPLS) provides a convenient and cost-effective way of implementing a single-chip synchronous arbiter for multiprocessor systems. This 8-page publication describes the arbiter structure and operation, and shows how the FPLS approach offers significant savings in both parts and board space compared with arbiter designs using discrete MSI arrays.

Quality of SOT-32 plastic power transistors

This 4-page Technical Note describes the Quality Assurance procedures used in the manufacture of our SOT-32 medium-power plastic transistors. These devices are widely used in general industrial applications, as well as in consumer radio, audio, and tv equipment. The results of five years of accelerated life tests are presented, and it is shown that the useful life is in excess of 75 000 thermal cycles and the overall failure rate is about $6 \times 10^{-6}/h$, both measured under Absolute Maximum Rating operation.

Copies of the publications mentioned can be obtained upon written application either to the publications department of one of the companies listed on the back cover or to the Editor, stating the nature of the applicant's interest.

The P² CCD 500B linear imager

M. HERMANN and J. WÖLBER

The profiled peristaltic charge coupled device (P²CCD), a recently developed variant of the conventional CCD, evolved from the need to combine the high charge handling capacity of the surface channel device with the high clocking frequency and high transfer efficiency of the deep buried channel device.

In this article we shall describe the operation of the P²CCD with particular reference to video imaging. This will lead to a description of the new P²CCD 500B linear imager and its application as a line scanner suitable for scanning films or slides for reproduction by television.

TABLE

Comparative performance of the surface channel device, deep and shallow buried channel devices, and the P²CCD.

type	transfer efficiency	charge handling capacity (electrons/cm ²)	limiting frequency (MHz)
surface channel CCD	0.9999	10 ¹²	10
deep buried channel CCD	0.99999	10 ¹¹	100
shallow buried channel CCD	0.99999	10 ¹²	25
P ² CCD	0.99999*	8 x 10 ¹¹	180

* Recently a transfer efficiency of 0.999999 has been measured corresponding to an average loss of 6 electrons between each stage.



The P²CCD 500B linear imager

OPERATION

In the conventional CCD, charge transfer is effected either at the surface of the substrate (surface channel CCD) or in the bulk of the substrate (buried channel CCD). The surface channel device, whilst possessing a high charge handling capacity, has the drawbacks of limited transfer efficiency and relatively low clocking frequency (typically 10 MHz). These are due to the interference effects caused by charge interaction with surface states, and to the sharply defined potential barriers in the vicinity of the electrodes (Fig.1), which are not conducive to efficient charge transfer. In contrast, the potential barriers in deep buried channel devices are not so sharply defined owing to fringe field effects, and this coupled with the absence of surface states in the bulk of the substrate, leads to high transfer efficiency and high clocking frequency (up to 100 MHz). Charge handling capacity however, is severely limited in deep buried channel devices.

We may mention here the shallow buried channel CCD which to some extent represents a compromise between surface and deep buried channel devices. Whilst possessing high transfer efficiency and high charge handling capacity, the shallow buried channel device does unfortunately have a rather limited clocking frequency (up to 25 MHz).

Let us consider now how the advantages of both surface and deep buried channel devices are combined in the P²CCD.

A cross-section of the P²CCD is shown in Fig.2. An n-type silicon twin layer (n₁ and n₂) with a thickness of several microns, is deposited on a negatively biased (isolating) p-type substrate. At its top, the n-type layer is isolated from an array of electrodes by an oxide layer. Charge transfer takes place within this n-type layer, separation being achieved by a negative voltage applied to the appropriate electrode. Storage of charge packets, which occurs beneath each electrode, is effected by the application of a positive voltage to the electrode concerned.

The n-type layer consists of a very thin (0.2 μm) heavily doped region n₁ and a thicker lightly doped region n₂. This has the effect of producing a dual mode transfer system, the majority of the charge (90%) transferring in the n₁ region slightly below the surface (thereby avoiding surface states), and the remainder transferring in the n₂ region. Advantages of this system are:

- High charge handling capacity due to the major part of the charge transferring close to the silicon surface.
- High transfer efficiency since interaction with surface states is avoided (values as high as 0.999999 having been measured).
- High clocking frequency (about 180 MHz) since the remainder of the charge is transferred within the bulk of the substrate where the potential barriers are less sharply defined.

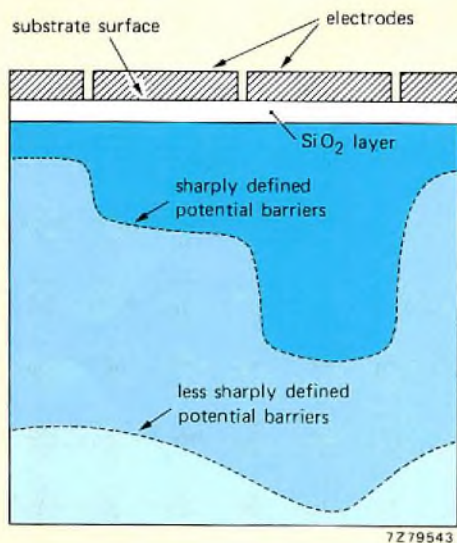


Fig.1 Potential function at the surface, and in the bulk of the substrate where fringe fields (i.e. fields from adjacent electrodes) become important

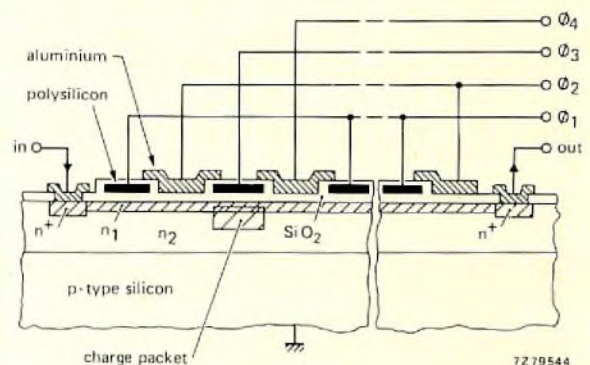


Fig.2 Cross-section of the P²CCD showing the two n-type layers (n₁ and n₂)

VIDEO IMAGING

The small size and low operating voltages of the CCD, coupled with very high signal-to-noise ratio and quantum efficiencies (up to 90%), have led to increasing interest in its use as a video imager.

The P²CCD 500 B (Fig.3), is a linear imager which can be used for scanning films or slides. It comprises two interlaced linear arrays each containing 250 photo-sensors. Each array connects with a four phase P²CCD charge shift register via 250 integration elements. The shift registers (A and B in Fig.3) can be isolated from the integration elements by potential barriers; this prevents charge flowing from the integration elements to the shift registers during the integration time, i.e. the time in which an image line is scanned.

The effective length of a row amounts to 7.5 mm, this being defined by a window in an aluminium coating which acts as a screen. A p-type diffusion zone separates the photo-sensors from each other, and reduces 'blooming' by preventing charges gathered in the individual elements from dispersing.

During the integration time, a positive voltage is applied to the photo-gate (PG). This brings the integration elements to the condition in which they can store photo-electrons generated by the incident light.

On completion of the image line scan, i.e. at the end of the integration time, a pulse applied to the photo-gate causes the accumulated charge packets to transfer to the shift registers, whereupon they are shifted step by step to the output by clock pulses.

CHARGE TRANSFER IN THE P²CCD

To illustrate the transfer process in the shift registers, Fig.4 shows the configuration of the photo/integration elements and the individual cells of the shift registers, with clock inputs ϕ_1 to ϕ_4 . The clock pulses are shown in Fig.5.

If the voltages at ϕ_1 and ϕ_2 are raised above that at PG, charge originating at element B, for example, transfers to cells 1 and 2 of the lower shift register, and charge originating at A transfers to cells 1' and 2' of the upper shift register. Charge from elements C, D and Eetc., transfers in like manner, separation being maintained by low voltages on ϕ_3 and ϕ_4 (as described earlier with reference to Fig.2).

At instant t_1 (Fig.5) the voltage at PG is raised, thereby halting charge transfer to the shift registers which can then receive the next supply of charge from the photo-elements. At instant t_2 , the charge in cell 1 is shifted to cell 2 and subsequently to cell 3 by lowering the voltage at ϕ_1 and raising that at ϕ_3 . A similar transfer occurs in the upper shift register, separation being maintained in both registers by the low voltages on ϕ_1 and ϕ_4 . The advancing process is repeated continually until all the charge packets have reached the output registers, readout being effected via outputs OS and OD. Since the output signals of the two registers are obtained in complementary pulse trains, a simple addition of the two partial signals yields the total signal. It is necessary however, to filter out a residual clock pulse arising from asymmetries in the individual pulse trains.

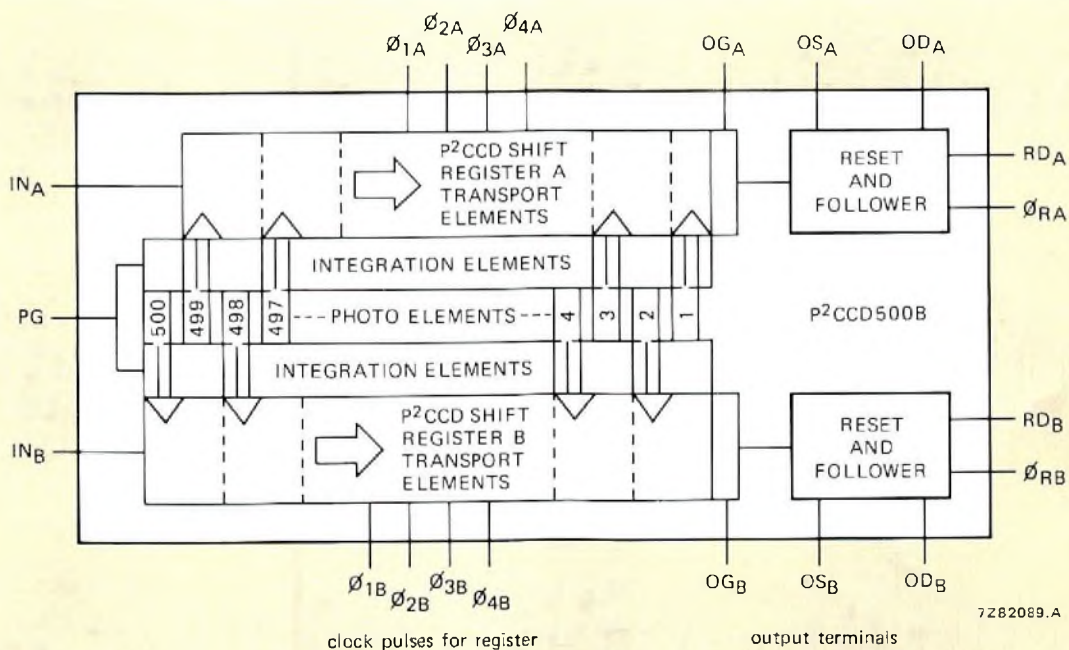


Fig.3 Block diagram of the P²CCD 500B linear imager

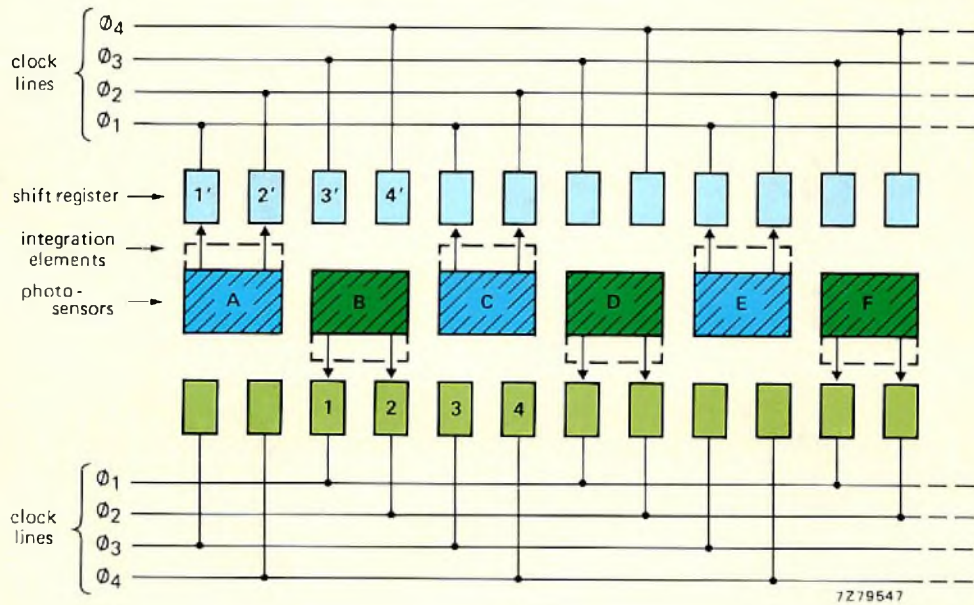


Fig.4 Representation of the photo-elements with their corresponding places in the shift register

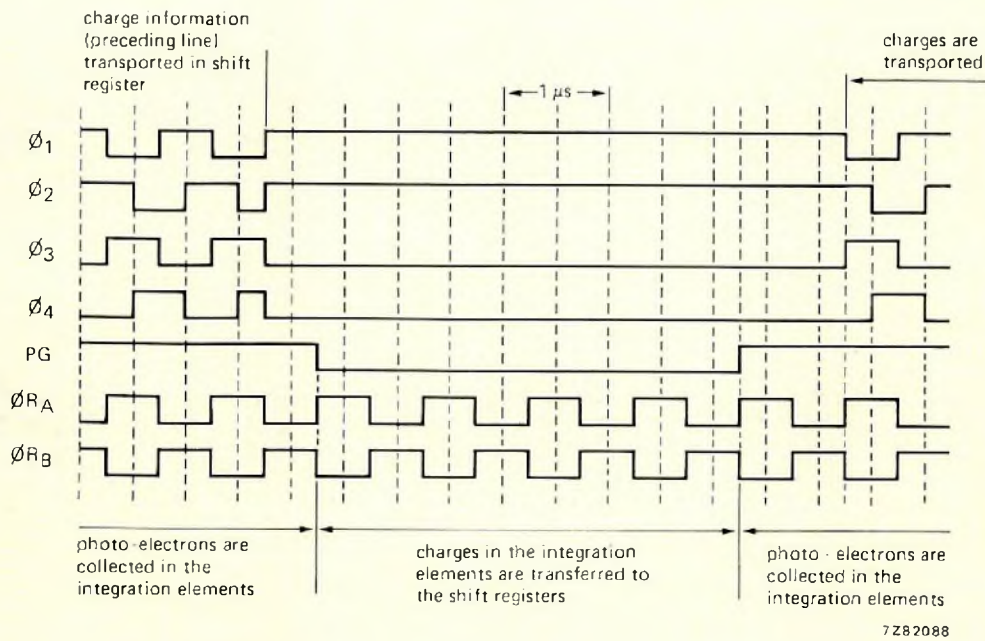


Fig.5 Representation of the clocking pulses which effect charge transfer

Complementary pulse trains at the reset clock lines ϕ_{RA} and ϕ_{RB} (Fig.3), reset the stages each time a charge packet has been read out.

In this manner, an image of the scene is built up line-by-line, each line being produced as a series of charge packets, the relative magnitudes of which provide a representation of the light intensity distribution over the scene.

DESIGN ADVANTAGES

Besides the intrinsic advantages of the P²CCD referred to earlier, the 500B imager offers numerous additional advantages over former devices.

Reduced transfer losses

Provision of a shift register on either side of the photo-sensors has the advantage that each register need contain only 250 storage places instead of 500, so that the total losses occurring within the shift registers are reduced significantly. As a bonus, the clocking frequency can be halved, leading in turn to a marked simplification in the design of driving circuitry.

Also, since charge transfer within the shift registers is separated physically from the photo/integration functions, the shift registers can be shielded from incident light which would otherwise cause blurring of the charge packets during transfer.

Enhanced blue sensitivity

Figure 6 compares the spectral sensitivity of the P²CCD 500B with an ideal curve for 100% quantum efficiency and a curve representative of former charge-coupled imagers. The significantly higher blue sensitivity of the 500B, which makes for more accurate colour rendition, was achieved by paying special attention to the electrode configuration in the photosensitive area.

FILM SCANNER FOR TELEVISION REPRODUCTION

Conventionally, films or slides are scanned for television either by means of a vidicon tube, or by use of a 'flying spot scanner'. Both methods have the drawbacks of excessive bulk and high voltage operation. In contrast, the P²CCD 500B is compact and able to operate at low voltages. In addition, its enhanced blue sensitivity means that the scanning of colour films for television is no longer beset by the problems associated with former CCD scanners.

The scanning of two-dimensional images by a linear pick-up device requires at least one relative movement between image and device. A practical set-up for scanning slides is shown in Fig.7. It comprises three sensors, each dealing with a different primary colour. The slide is illuminated by conventional means (i.e. mirror, 50W halogen lamp, condenser and heat protection filter), and a scaled-down image is projected onto the sensors via a splitter and appropriate colour filters.

At the end of each line scan, a rotating square prism advances the image one line width by means of parallax displacement, repeated scanning of the slide being effected by each new prism face deflecting the image in turn. The prism is rotated at 750 rev/min corresponding to a scan rate of 50 images per second.

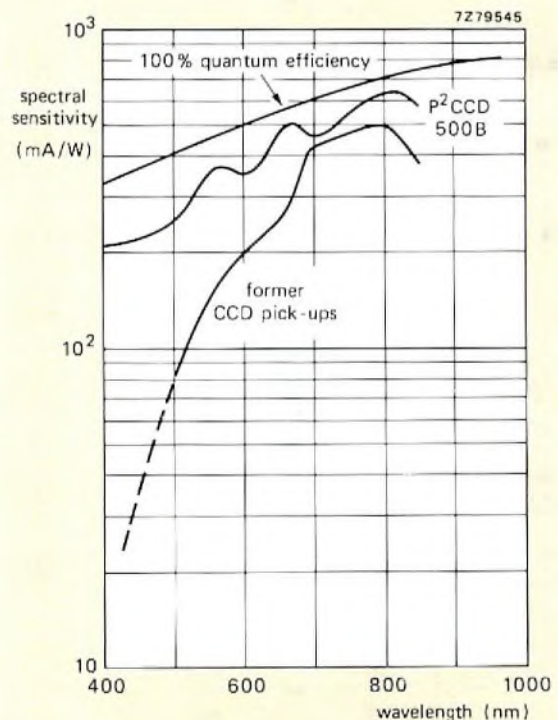


Fig.6 Spectral sensitivity as a function of wavelength

P²CCD LINEAR IMAGER

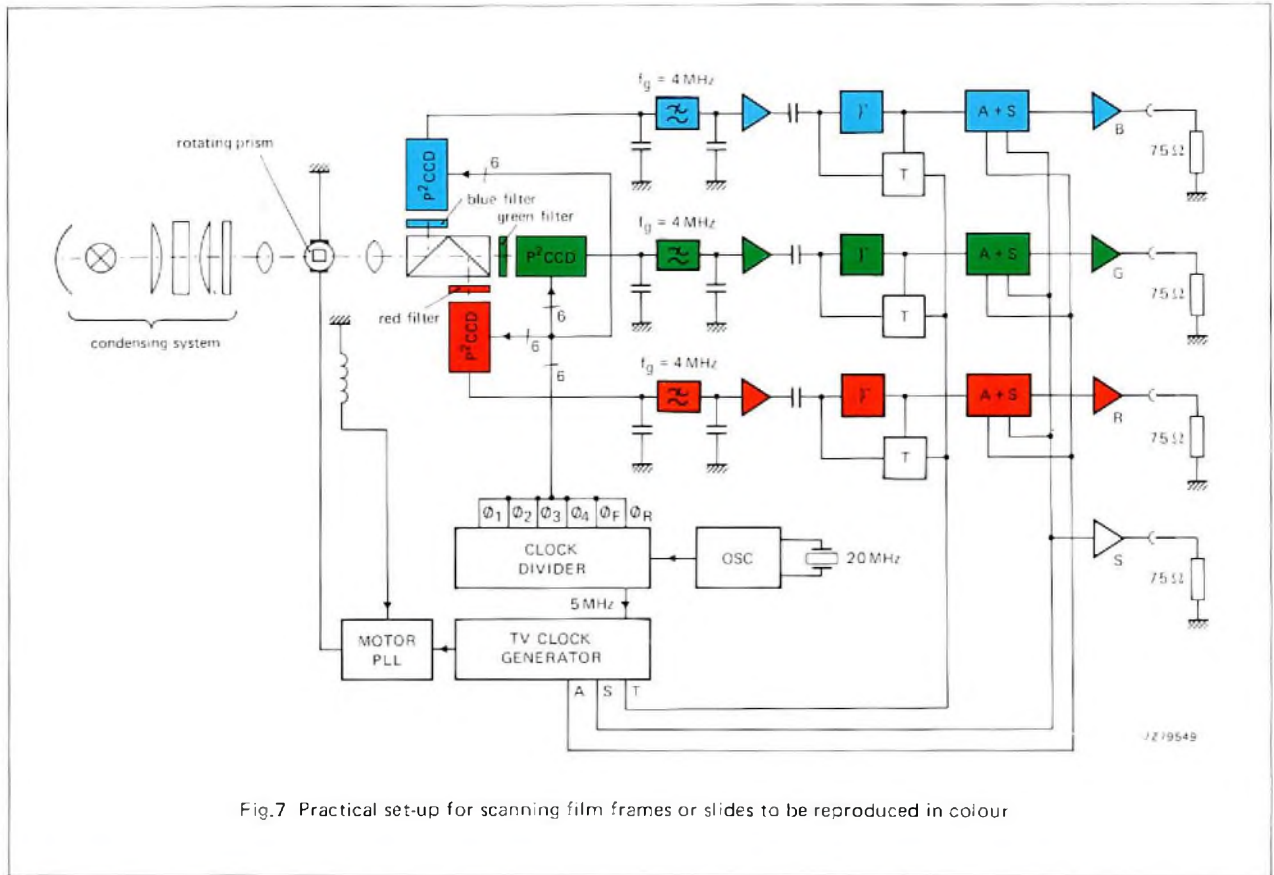


Fig.7 Practical set-up for scanning film frames or slides to be reproduced in colour

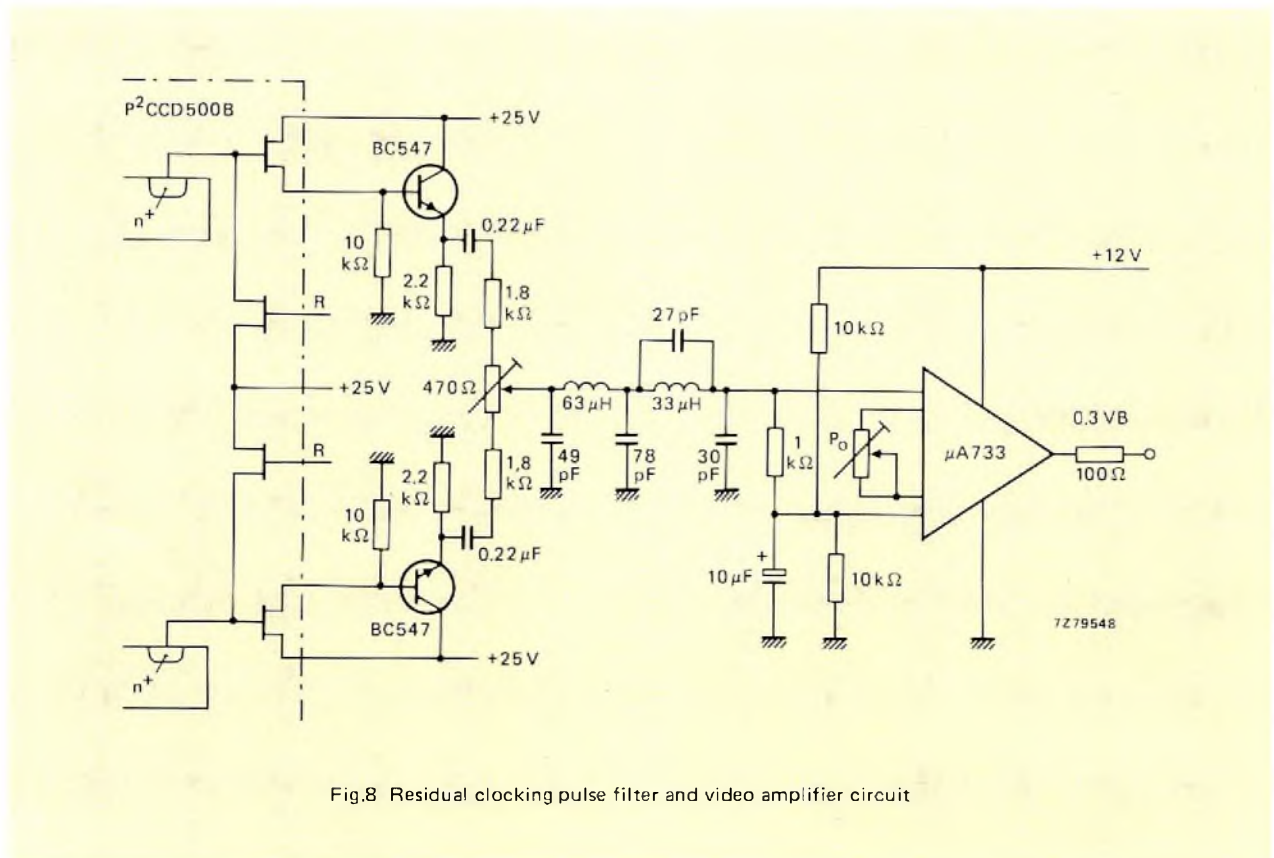


Fig.8 Residual clocking pulse filter and video amplifier circuit

In each scanner, the two partial signals generated by the shift registers are processed by reset and follower circuits (integrated in the chip) prior to being fed via emitter followers to a resistive matrix where they combine. Subsequently, the residual clock pulse interference is removed by a low-pass filter with a cut-off frequency f_g of 4 MHz (Fig.8), and the signal is raised to 0.3 VB by means of a video amplifier (VB being the video/blanking signal).

The set-up can be readily adapted for scanning films. To effect this, the film speed must be synchronised with the rotation of the prism, so that an advance of one frame coincides with a new prism face deflecting the image. Note, however, that provision must be made for interlacing, and for time conversion to adapt the speed of the scanner to that required for television reproduction (i.e. 25 full frame/second).

OPERATIONAL DETAILS

Scanning conditions

According to the CCIR standard, the duration of a visible line sweep must be $52 \mu\text{s}$. Hence, within this time the shift registers must access all the image elements (charge packets) constituting the line, so that:

$$N = (52 \mu\text{s}) \times f_c$$

where N denotes the number of storage cells required in each shift register and f_c its clocking frequency. Also, to maintain the spatial and chronological properties of the image, the clocking pulses should always be in the same phase at the start of each line. This is assured by choosing for f_c an integral multiple (M) of the line frequency f_L , so that:

$$f_c = M f_L = M / (64 \mu\text{s})$$

since the total time between the start of each line is $64 \mu\text{s}$ ($52 \mu\text{s}$ sweep plus $12 \mu\text{s}$ flyback time). In this way the need for a start-stop oscillator for generating f_c is obviated.

Combining the two equations above gives:

$$N = (52/64)M.$$

Hence, it is evident that the choice of N is limited, and we must choose from the possible values the one that is closest to the number of storage elements actually available, i.e. 250 in the 500B scanner. Putting $M=320$ which corresponds to a clocking frequency of 5 MHz, gives $N=260$. Therefore, to access a line in $52 \mu\text{s}$ whilst maintaining the phase relationship between clock pulses and line scans, we require a shift register of 260 cells. In

the 500B scanner, this means that 10 image elements are missing from each line. Nevertheless, the experimental model was designed with $f_c = 5 \text{ MHz}$ since, in normal reproduction by monitor, the image edges lie within the blanking period.

The theoretical resolution will therefore be 5 MHz. Allowing for the Kell factor, this figure should be reduced to 4 MHz.

Pulse sequences

The pulse sequence shown in Fig.5 has been shown to give good results. Individual clock pulses have an overlap of 50% at a scanning ratio of 1:2, the different pulse trains being derived from a master frequency of 20 MHz via a 1:4 divider. Figure 9 shows the timing diagram of the individual pulses.

The blanking pulse, the horizontal pulse and the photo-gate pulse are all derived, by way of an I²L circuit, from a fundamental frequency of 2.5 MHz which is itself derived from the clock line ϕ_1 .

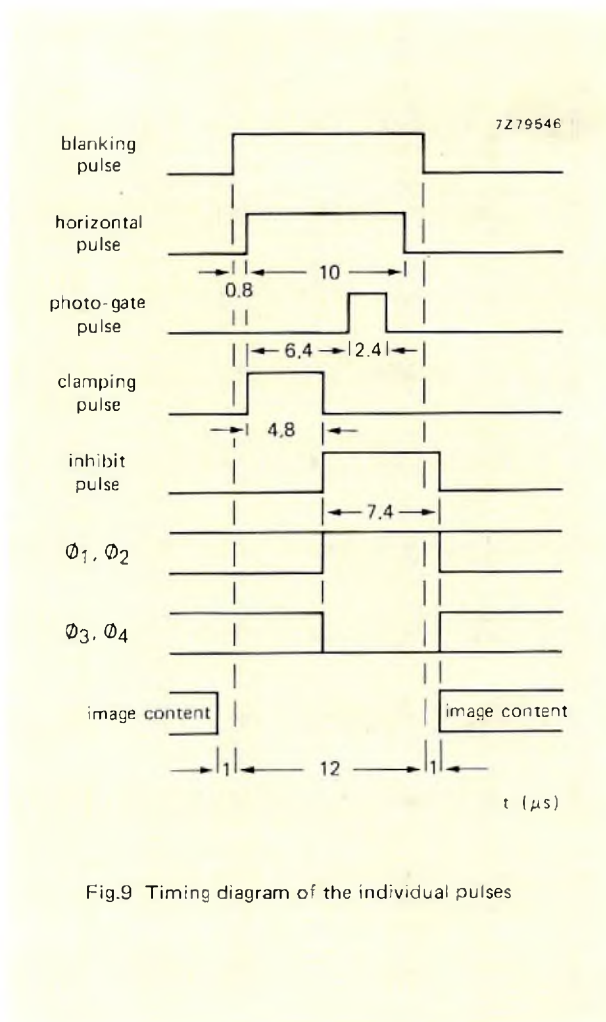


Fig.9 Timing diagram of the individual pulses

The duration of the clamping (4.8 μs) and inhibit (7.4 μs) pulses, which are derived from the horizontal pulse, are chosen so that the photo-gate pulse lies within the inhibit pulse, to allow transfer of charge from the photo-sensors to the integration elements. In addition, the inhibit pulse deblocks the clock pulse 1.0 μs after the blanking pulse ends, so that the first image element can be read out at that instant, thereby skipping the 10 missing elements.

After 250/(5 MHz) = 50 μs, the last image element will have been read out – just 1.0 μs before the next blanking pulse starts. Further readout of the registers will supply only the dark current.

Gamma correction with blanking and addition of synchronising pulses

To allow for the curvature of the picture tube drive characteristic, the signal is subjected to gamma correction. Following this it is provided with the required flyback and synchronising pulses referred to a level of 1 V p-p across 75 Ω.

Gamma correction is achieved by negative (current) feedback produced by transistors TR₁ to TR₃ and diodes D₁ to D₆ (Fig.10), the gamma value being adjusted to 1/3, i.e. $V_0 = V_i \exp(1/3)$.

For efficient operation of the gamma correction, it is necessary to fix the reference levels for image 'black' and image 'white'. A clamping circuit, consisting of the FET TR₄ and the operational amplifier TBA221B (which fixes the black level at 0 V), serves to maintain the reference level for black, monitoring of the level taking place during flyback. The reference voltage for white (2 Vp-p) is adjusted by a potentiometer P₀ in the video amplifier circuit (Fig.8).

Blanking pulses (B pulses) and synchronising pulses (S pulses) are provided by transistors TR₅ to TR₁₁ which also provide impedance transformation to ensure that the white level is maintained at 2 Vp-p.

Performance

A photograph of the picture produced by a television monitor (Fig.11) illustrates the quality obtained with the set-up described above.

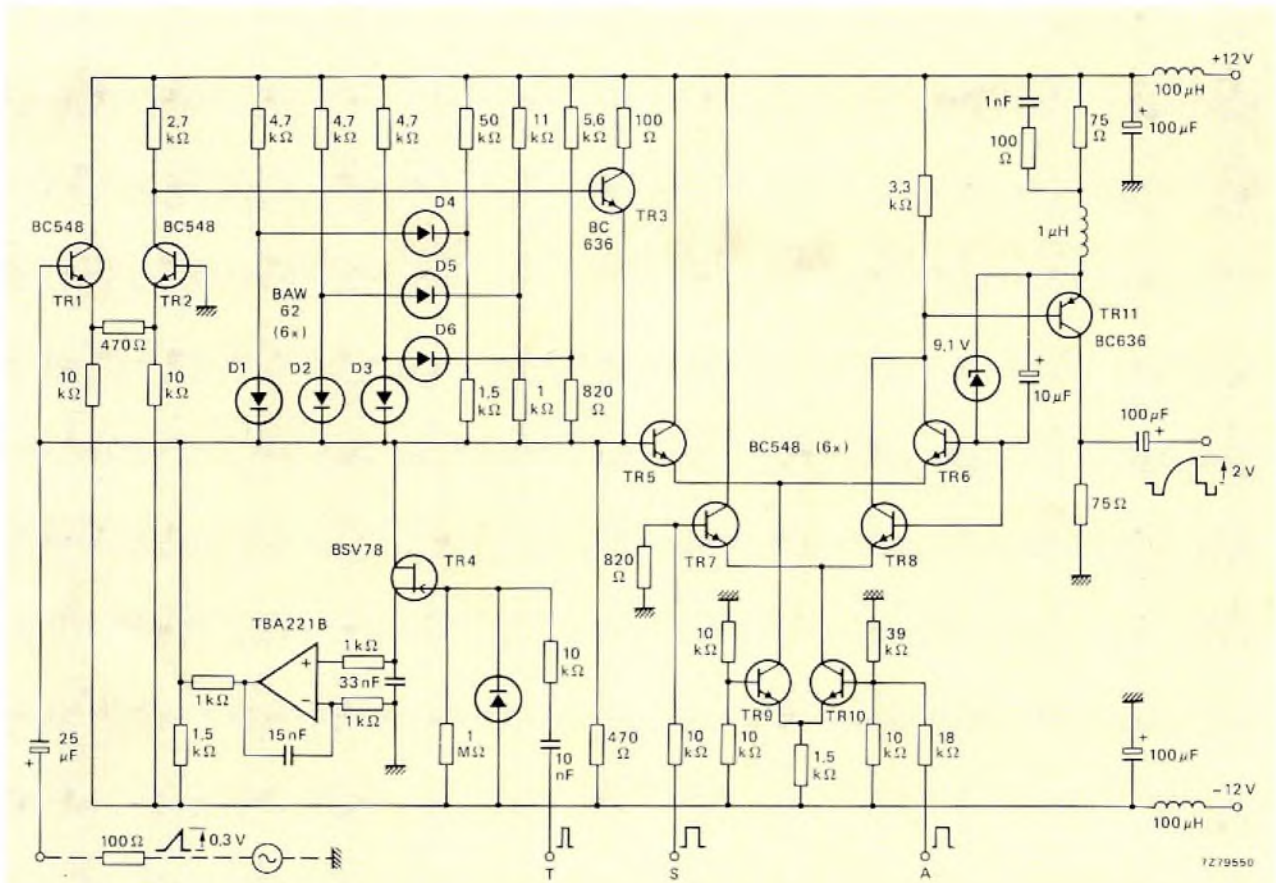


Fig.10 Circuit for gamma correction, blanking, and synchronisation

FUTURE DEVELOPMENT

In future arrangements, the brachial type of colour separator will be replaced by a dichroic system or one employing a phase grating. Advantage can then be taken of the resultant gain in luminance by the use of smaller lenses (with a consequent saving in cost).

Another likely development is the use of the film motion itself to effect the relative displacement between image and sensors, thereby eliminating the rotating prism.

Finally, the resolution of about 4 MHz already meets the requirements imposed by present-day television

broadcasting. We are nevertheless, producing a line scanner with three sensors — each of 652 elements — integrated in a single crystal. This will improve resolution and reduce the problem of maintaining line coincidence in colour television reproduction. In this way we shall avoid the remaining limitations and take full advantage of the system.

Acknowledgement

The authors wish to thank Mr. L. J. M. Esser of the Philips Research Laboratories, Eindhoven, for his advice in the preparation of this article.



Fig.11 The TV screen displays the slide projected onto the laboratory model P²CCD scanner in the foreground.

Research news

THE LSI REVOLUTION

At a time when the full impact of Large-Scale Integration (LSI) on electronics is becoming self-evident, a special issue of Philips Technical Review has been entirely devoted to describing some of the detailed and extensive research being carried out in the various Philips Research Laboratories on this topical and important subject. Obviously, a single issue cannot give anything like a full picture of Philips activities in the IC field, not even in research, but it is felt that the contents will be of great interest to all working in electronics, even though development is now so rapid that those in the front line of research may regard certain approaches as already somewhat dated.

Below we reprint *verbatim* complete abstracts for the contents of the Philips Technical Review (Vol 37, No 11/12, 1977) on LSI.

H. Bosma and W.G. Gelling: LSI – a revolution in electronics

Introductory article to a special issue on large-scale integration. A general picture is given of the progress – in silicon-crystal manufacture, lithographic techniques, physical and chemical treatments and the layout of the circuits – that now enables some 10 000 gates to be mounted on a single chip at a density of 300 per mm². The design and testing of such large circuits would be an impossible task without the aid of a computer. Physical and chemical processing is also controlled by a computer.

C. Niessen: Computer-aided design of LSI circuits

In the design of LSI circuits it is necessary to have CAD facilities available. Circuit-analysis techniques can be used to verify analog circuits that are not unduly large,

such as digital modules. Large LSI circuits cannot be handled in this way, and digital design aids are far more useful here. For this reason, and also because the digital technique is simpler for the designer, LSI circuits will increasingly be made with the aid of digital techniques, even for functions that are essentially of an analog nature. The repertoire of CAD software available includes logic-simulation programs for verifying the correct operation of the circuit, programs that provide help in layout design or that produce the layout completely automatically, and programs that make test procedures for LSI circuits and check their quality. Finally, for a number of widely used technologies there are also CAD systems in which the computer program includes the transition from one design phase to the next.

R.A. van Doorn and N.A.M. Verhoeckx: An I²L digital modulation stage for data transmission

In transmitting data signals via telephone lines use is made of 'modems', in which the signals are subjected to various operations such as filtering, modulation and demodulation before transmission and after reception. Depending on the transmission rate, different filter characteristics and different modulation methods may be used. A unit in fairly general use is the linear modulation stage, consisting of a filter and a product modulator. In digital form this modulation stage is particularly versatile, since it is only necessary to replace the contents of a digital memory to make the circuit comply with entirely different specifications. To produce a digital modulation stage in the form of an integrated circuit, it is not only necessary to make an accurate analysis of the logic design (word lengths, sampling rates), it is also necessary to make the best use of the special features of

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the semiconductor technology employed. This article describes the design and construction of a digital modulation stage for data-transmission applications in the form of an I^2L circuit, with particular attention to these two aspects.

H. Heyns, H.L. Peek and J.G. van Santen: Image sensor with resistive electrodes

Sensors based on charge-transfer devices (CTDs) are an important category of solid-state image sensors. They are small silicon chips in which once in every frame period an optical image, converted into a pattern of charge packets, is shifted via vertical CTDs to the bottom of the image matrix, where it is processed into a video signal by means of a horizontal CTD. Difficulties involved are the low blue sensitivity (dense electrode system) and 'blooming'. The article discusses an image sensor in which the vertical transfer takes place in 'potential channels' with a vertical gradient produced by resistive electrodes. The image matrix of 4.2×5.6 mm has 300 lines and 200 columns. Each line is transferred in a time much shorter than a line period; the rest of the time is available for the removal of charge due to overexposure. Since the electrode system is not very dense, the sensor is also sensitive in the blue.

L.D.J. Eggermont, M.H.H. Hofelt and R.H.W. Salters: A delta-modulation to PCM converter

The development of LSI circuits makes it possible to use digital techniques in a telephone network, both for transmission and for switching. This can have considerable economic advantages, provided the analog/digital and digital/analog converters are inexpensive. This implies that the use of expensive analog filters has to be avoided. The article describes an A/D converter in which the analog signals are indirectly converted into the standard PCM code via an HIDM code ('high-information delta modulation'). It is shown how the conversion of this intermediate code into the PCM code can be resolved into its elementary functions and subsequently combined so as to produce a design suitable for fabrication as an LSI circuit. A description is given of the design of the circuit in an LSI technology that combines a high packing density with low dissipation. The technology used is four-phase dynamic MOS logic.

A.G. Bouwer, G. Bouwhuis, H.F. van Heek and S. Wittekoek: The Silicon Repeater

The Silicon Repeater is a machine that makes repeated and reduced projections of a single photomask with accurate positioning on a silicon wafer coated with photoresist. The use of this machine greatly simplifies

the production of integrated circuits. In addition, the absence of mechanical contact between wafer and mask minimizes the risk of damage to mask and photoresist, thus improving the yield of the production process. The exposure of a three-inch wafer takes two minutes; the positioning of an exposure, and the realignment of the wafer after an intermediate operation, can be carried out to an accuracy of about $0.1 \mu\text{m}$. The smallest details in a circuit can have a dimension of $2 \mu\text{m}$.

J.P. Beasley and D.G. Squire: Electron-beam pattern generator

An electron-beam machine for making complex and precise patterns such as those required for integrated circuits is described. A $0.25\text{-}\mu\text{m}$ diameter beam of electrons controlled by a computer draws patterns on a metallized substrate covered in electron-sensitive resist. After development and etching a pattern is produced (maximum dimensions 42×42 mm) which can be used directly or as a mask to be copied by other means. A two-stage deflection system is used. The first stage (relatively slow) deflects the beam to within a 2×2 mm square, the second stage (relatively fast) draws the appropriate part of the pattern inside the square. The pattern is made up from trapezia of maximum size $32 \times 32 \mu\text{m}$. The patterns can be positioned to an accuracy of $\pm \frac{1}{8} \mu\text{m}$ with the aid of a set of markers pre-deposited on the substrate. A complete mask containing details as small as $0.5 \mu\text{m}$ takes 1 to 3 hours to draw.

J.P. Scott: Electron-image projector

An electron-image projector is a machine for reproducing very fine patterns rapidly and at high resolution. Electrons are emitted from a photocathode material coating the mask and are accelerated and focused on the substrate by highly uniform electric and magnetic fields. This exposes an electron-sensitive resist coating the substrate and so reproduces the pattern at unity magnification. The PRL projector includes a number of new features which have made the method more generally applicable for the production of integrated circuits than hitherto. These include the use of caesium iodide as the photoemitter material, a new design for the magnet and a method of automatic alignment using Bremsstrahlung X-rays, including improvements to the signal detection and processing. The machine has been in use for two years and achieves an alignment accuracy of $0.1 \mu\text{m}$ and a resolution (limited by back-scattering of electrons in the substrate) of $0.3 \mu\text{m}$. The complete cycle of loading, pumping down, alignment, exposure and removal of the processed slice takes about 3 minutes.

Abstracts

Reliability proven; BDW55/56 gold-gold medium-power transistors

Using titanium-platinum-gold barrier-layer chip metallisation in combination with gold-silicon eutectic bonding and glass passivation, a new family of plastic encapsulated medium-power transistors has been introduced which could replace TO-5 metal-can hermetic transistors. A test programme carried out on the BDW55, the first of the new transistors, conclusively demonstrated its immunity to moisture and its freedom from the effects of thermal fatigue and electromigration within its Absolute Maximum Ratings. As a result of the programme, the design maximum junction temperature of 150°C was increased to 175°C for production devices. Measures are taken to eliminate the principal cause of early failure and make burn-in virtually unnecessary.

Single-phase rectifier circuits with CR filters

Part 1 – Theory

The semiconductor rectifier and CR filter combination is considered in detail in this two-part article. In part 1, the transformer-fed half-wave rectifier and CR filter circuit is analysed and new, simple, and exact equations are derived. Similar equations for full-wave, bridge, and symmetrical voltage doubler circuits are also presented.

Understanding thyristor and triac data

The published data for our range of thyristors and triacs is described and explained; a brief description of the characteristics of thyristors and triacs is also provided. It is shown how data can be presented in a misleading way, while the content and presentation of our published data is justified.

The P²CCD 500B linear imager

The P²CCD 500B linear imager incorporates 500 photo-sensors and can be used to scan slides or films for reproduction by television. A set-up for scanning colour slides is described comprising three imagers each dealing with a different primary colour, and the way in which the set-up can be modified to scan films is indicated. A system resolution of about 4 MHz means that the requirements of present day broadcasting are met with ease.

Zuverlässigkeit geprüft; Gold-Gold-Transistor mittlerer Leistung

Eingeführt wurde eine neue Transistorenfamilie mittlerer Leistung in Kunststoffgehäusen, bei denen die selbstpassivierende Halbleitermetallisierung durch Titan-Platin-Gold in Verbindung mit der eutektischen Gold-Silizium-Bondung und Glas-Passivierung angewendet wird. Diese Familie ist geeignet, die hermetisch dichten Metall-TO5-Gehäuse-Transistoren zu ersetzen. Ein Prüfprogramm, das am BDW55, dem ersten dieser neuen Transistoren, durchgeführt wurde, demonstriert schlüssig seine Unempfindlichkeit gegen Feuchtigkeit und das Fehlen thermischer Ermüdung sowie Elektromigration im Bereich der absoluten Grenzwerte. Als Ergebnis dieses Programms wurde die zulässige maximale Sperrschichttemperatur von 150°C auf 175°C für Serienprodukte heraufgesetzt. Messungen wurden angestellt zur Behebung der Hauptursachen für Frühausfälle, so dass die künstliche Alterung (burn-in) praktisch entfallen kann.

Einphasen – Gleichrichterschaltungen mit RC-Filtern

Teil 1 – Theorie

In der aus zwei Teilen bestehenden Veröffentlichung, werden Halbleiter-Gleichrichterschaltungen in Verbindung mit RC-Filtern ausführlich behandelt. Im ersten Teil erfolgt die Analyse eines aus einem Transformator gespeisten Einweg-Gleichrichters einschließlich des dazugehörigen RC-Filterns. Es werden neue, einfache und dennoch exakte Gleichungen abgeleitet. Entsprechende Gleichungen für Zweiweg-Gleichrichter, Brücken- und symmetrisch Spannungsverdopplerschaltungen runden die Ausführungen ab.

Zum Verständnis von Thyristor- und Triac-Daten

Neben einer kurzen Beschreibung der charakteristischen Eigenschaften unserer im Programm enthaltenen Thyristoren und Triacs werden deren Daten angegeben und erläutert. Darüber hinaus wird gezeigt, wie leicht es zu Fehlinterpretationen von an sich richtigen, korrekt publizierten Daten kommen kann.

Zeilenförmiger Bildaufnehmer P²CCD 500B

Der zeilenförmige Bildaufnehmer P²CCD 500B enthält 500 Fotosensoren und kann zum Abtasten von Dias oder Filmen bei Wiedergabe über Fernsehleinrichtungen verwendet werden. Ein Aufbau zur Abtastung von Farbdias wird beschrieben, bei dem 3 Systeme jeweils für eine andere Ausgangsfarbe vorgesehen ist. Ferner wird der Weg aufgezeigt, auf dem der Aufbau zur Abtastung von Filmen modifiziert werden kann.

Une fiabilité éprouvée; transistors de puissance moyenne or-or BDW55/56

En utilisant la métallisation de la puce par une couche d'arrêt titane-platine-or en combinaison avec la liaison eutectique or-silicium et la passivation du verre, une nouvelle famille de transistors de moyenne puissance sous enveloppe plastique a été introduite, susceptible de remplacer les transistors sous boîtier métallique hermétique TO-5. Un programme d'essai effectué sur le BDW55, le premier de ces nouveaux transistors, a démontré qu'ils étaient insensibles à l'humidité et aux effets de la fatigue thermique et de l'électromigration dans les limites de fonctionnement maximum absolues. A la suite de ce programme, la température de jonction maximale de 150 °C a été élevée à 175 °C pour les besoins de la production. Des mesures ont été prises en vue d'éliminer la cause principale de défaillances prématurées et de rendre pratiquement inutile tout essai préliminaire à température maximum.

Circuits redresseurs monophasés avec filtres CR

1ère partie – Théorie

L'association de redresseurs à semi-conducteurs et de filtres CR est examinée de façon détaillée dans cet article composé de deux parties. Dans la première partie, le circuit formé par le transformateur alimentant le redresseur à une alternance et le filtre CR est analysé et de nouvelles équations, simples et exactes, en sont tirées. Des équations similaires pour des circuits doubleurs de tension symétriques, des redresseurs à double alternance et en pont sont également présentées.

Compréhension des données relatives aux thyristors et aux triacs

Les données publiées pour notre gamme de thyristors et de triacs sont décrites et expliquées; une brève description des caractéristiques des thyristors et des triacs est également présentée. L'article montre comment des données peuvent être présentées d'une façon trompeuse, et justifie le contenu et la présentation des données que nous publions.

Caméra linéaire P²CCD 500B

La caméra linéaire P²CCD 500B comporte 500 senseurs optiques et peut être utilisée pour analyser des diapositives ou des films afin de les reproduire sur écran de télévision. Un dispositif qui permet d'analyser les diapositives couleur est décrit; il comprend trois caméras dont chacune est réservée à une couleur primaire différente; la façon de modifier cette installation pour analyser les films est également indiquée.

Fiabilidad comprobada: transistores de potencia media oro-oro BDW55/56

Empleando metalización de chip titanio-platino-oro en combinación con unión eutéctica silicio-oro pasivación de vidrio, se ha introducido una nueva familia de transistores de potencia media encapsulados en plástico que pueden reemplazar transistores en cápsula metálica hermética TO-5. Un programa de pruebas llevado a cabo con el BDW55 el primero de los nuevos transistores, demostró de forma concluyente su inmunidad a la humedad y la ausencia de los efectos de la fatiga térmica y electromigración dentro de sus Valores Máximos Absolutos. Como resultado del programa, la temperatura de unión máxima de diseño de 150 °C se aumentó a 175 °C para los dispositivos de producción. Se han tomado medidas para eliminar la principal causa de fallos prematuros y hacer virtualmente innecesario las pruebas de choque térmico.

Circuitos rectificadores monofásicos con filtros CR

Parte I-Teoría

En este artículo en dos partes se considera en detalle la combinación rectificador semiconductor y filtro CR. En la primera parte se analiza el circuito rectificador de media onda alimentado por transformador y filtro CR, y se deducen nuevas, sencillas y exactas ecuaciones. También se presentan ecuaciones similares para los circuitos de onda completa, puente y doblador de tensión simétrico.

Interpretación de los datos de tiristores y triacs

Se describen y explican los datos publicados para nuestra gama de tiristores y triacs; se da también una breve descripción de las características de tiristores y triacs. Se muestra como los datos pueden ser presentados en forma equívoca, al propio tiempo que se justifica el contenido y la presentación de nuestros datos publicados.

El captador de imagen por líneas P²CCD 500B

El captador de imagen por líneas P²CCD 500B incorpora 500 fotosensores y puede ser empleado para explorar diapositivas o películas para reproducción por televisión. Se describe en equipo para exploración de diapositivas de color que consta de tres captadores de imagen por líneas cada uno de los cuales responde a un color primario distinto, y se indica como puede modificarse el equipo para explorar películas.

Authors



M. Herrmann was born in Herrstein, Germany in December 1936. From 1956 he attended the University of Mainz, where he obtained a Diploma in Physics and in 1964 a doctorate for his research into electronic emission processes. He subsequently joined Heimann G.m.b.H. Wiesbaden where he worked on the development of low light level television tubes. In 1970 he joined the VALVO Applications Laboratory, Hamburg, specializing in the development of charge-coupled devices and their application to video imaging.



A. Lieders graduated from the Technical University of Prague in 1942. From then until 1945 he worked on the production of mobile radio equipment at Ostmarkwerke G.m.b.H., Prague, and from 1945 to 1948 he was development engineer for radio receivers, first with Telefunken and later with Tesla-National Enterprises. Since 1950 he has occupied leading positions with several Brazilian electronics companies in Sao Paulo, and from 1957 to 1965 was co-owner and technical director of Inelbras-Electronic Industry, a company producing radio and TV kits for hobbyists. Since 1974 he has directed the TV department of the Philips Electronic Components and Materials Application Laboratory for Ibrape, Brazil.



Paul Noble studied Physics at Bristol University and graduated with an honours degree in June 1976. After a brief period in the Arabian Gulf working in the oil business and at sea, he returned to the United Kingdom and joined Mullard Ltd. as a technical writer in April 1977. Since December 1978 he has been working as a technical writer for a public relations company.



S. Sliedregt was born in Delft, The Netherlands, in 1934. He studied electrical engineering at the Hogere Technische School, 's Gravenhage, from where he graduated in 1957. He joined the Elcoma division of Philips in 1958 to work in the semiconductor quality laboratory in Nijmegen. Since 1974, he has been responsible for the release of components for military and aerospace applications. He also leads the Nijmegen group concerned with semiconductor reliability and failure analysis.



J. Wölber was born in Hamburg in December 1939. He studied telecommunications at the Fachhochschule, receiving the degree of Ing in 1963. In the same year he joined the VALVO Applications Laboratory, Hamburg as a member of the television group. In 1972 he became responsible for picture tube applications and since 1977 he has led the group concerned with digital applications in consumer appliances.

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- India:** PHILIPS INDIA LTD., Elcoma Div., Band Box House, 254-D, Dr. Annie Besant Rd., Prabhadevi, BOMBAY-25-DD, Tel. 457 311-5.
- Indonesia:** P.T. PHILIPS-RALIN ELECTRONICS, Elcoma Division, 'Timah' Building, Jl. Jen. Gatot Subroto, P.O. Box 220, JAKARTA, Tel. 44 163.
- Ireland:** PHILIPS ELECTRICAL (IRELAND) LTD., Newstead, Clonskeagh, DUBLIN 14, Tel. 69 33 55.
- Italy:** PHILIPS S.p.A., Sezione Elcoma, Piazza IV Novembre 3, I-20124 MILANO, Tel. 2-6994.
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- Mexico:** ELECTRONICA S.A. de C.V., Varsovia No. 36, MEXICO 6, D.F., Tel. 533-11-80.
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- New Zealand:** PHILIPS ELECTRICAL IND. LTD., Elcoma Division, 2 Wagener Place, St. Lukes, AUCKLAND, Tel. 867 119.
- Norway:** NORSK A/S PHILIPS, Electronica, Sørkedalsveien 6, OSLO 3, Tel. 46 38 90.
- Peru:** CADESA, Rocca de Vergallo 247, LIMA 17, Tel. 62 85 99.
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- Uruguay:** LUZILETRON S.A., Rondeau 1567, piso 5, MONTEVIDEO, Tel. 9 43 21.
- Venezuela:** IND. VENEZOLANAS PHILIPS S.A., Elcoma Dept., A. Ppal. de los Ruices, Edif. Centro Colgate, CARACAS, Tel. 36 05 11.