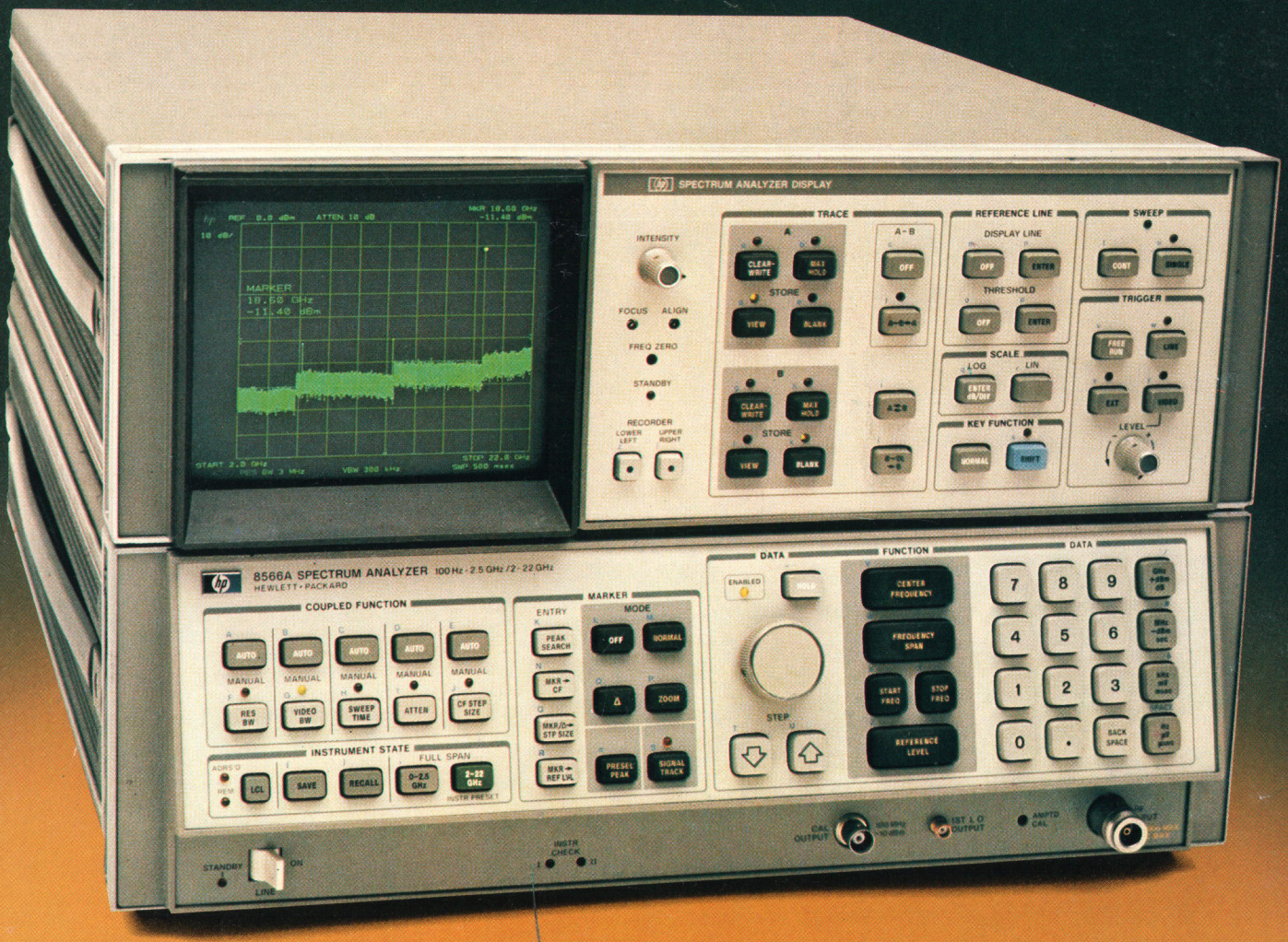
AUGUST 1979

HEWLETT-PACKARD JOURNAL



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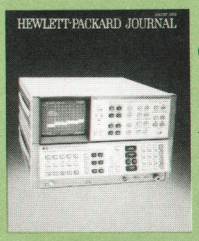


Microwave spectrum analyzers were first recognized as practical measurement tools during World War II when they were used to evaluate how effectively radar transmitters concentrated their radiated power into spectral bandwidths detectable by the receivers. The narrowest resolution bandwidth of these first analyzers was a wide 100 kHz, the maximum frequency sweep was merely 30 MHz, and results were only qualitative. Nevertheless, the kind of information they provided—separation and simultaneous display of the frequency components that make up a signal—proved to be invaluable in analyses of complex signals. Further developments came slowly, but by the 1960s, bandwidth had narrowed to 1 kHz, 2-GHz sweeps were possible and spectrum analyzers were beginning to find wide use on the lab bench for evaluating the performance of mixers, oscillators, amplifiers, and other high-frequency circuits as well as providing quantitative measurements of electromagnetic interference and radio spectrum activity. By the 1970s, resolution had sharpened to 100 Hz and it had become possible to measure amplitude and frequency directly from the display. Now for the 1980s, the new microprocessor-controlled Model 8566A is capable of 10-Hz resolution, 20-GHz sweeps, and precision digital readout of amplitude and frequency. (The 8566A on the front cover is displaying a 20-GHz sweep—the steps on the noise floor occur where the sweeping local oscillator automatically steps back in frequency and then continues the sweep upwards using the next higher harmonic.)

Usually the design of a digital system controller and external hardware is parcelled out to several engineers, each of whom faces a basic problem: how to test each module thoroughly before integrating the modules into the system. The 8170A Logic Pattern Generator, described on page 20, addresses this problem by being able to simulate real-time data-bus traffic, complete with handshake signals when needed. Thus, it can be used to test modules for bus compatibility so that hardware, firmware, and software development can proceed independently.

As the range of applications for HP-interface-bus-controlled instrument systems has expanded, there has been a growing demand for some means of allowing the bus to operate with units separated by more than the 20 metres that the standard bus circuitry allows. This limitation on distance is now removed by the development of the 37201A HP-IB Bus Extender, described on page 26. This device transfers the HP-IB data through a modem onto telephone lines and sends it reliably any distance the telephone system allows—half way around the world if need be—to another extender that converts it back to HP-IB format for the units at the distant location.

-H. L. Roberts

New Performance Standards in Microwave Spectrum Analysis

Low-level microwave signals not previously identifiable with spectrum analyzers can be measured up to 22 GHz with the aid of this new analyzer's low phase noise, 10-Hz bandwidth, and high sensitivity.

by Siegfried H. Linkwitz

ADVANCING TECHNOLOGY NOW makes it possible for a spectrum analyzer designed for the microwave frequency range (above 1 GHz) to achieve the same frequency and amplitude accuracies as the best of those designed for lower frequencies.

In the past, spectrum analyzers designed for the microwave range had limited accuracy for the measurement of an unknown signal's frequency, and were unable to resolve closely spaced spectral components. These limitations existed because of the difficulty of determining the exact frequency of the wideband voltage-tuned microwave local oscillator used for frequency conversion and because of the local oscillator's inherent instability.

A new microwave spectrum analyzer, Model 8566A (Fig. 1), incorporates new solutions to these problems, bringing to the microwave region the performance formerly associated only with high-grade spectrum analyzers designed for lower frequencies. The performance of the new Model 8566A is such that it is possible, for example, to measure the frequency of a 20-GHz signal with ±32-Hz accuracy. Furthermore, the new analyzer's stability and low phase noise allow the use of a 10-Hz resolution bandwidth throughout its extremely wide 100-Hz-to-22-GHz input range, enabling for the first time the resolution of close-in, power-line related sidebands on a microwave signal (Fig. 2).

To achieve frequency accuracy in this instrument, frequency synthesis techniques are used to establish the start frequency of a sweep very accurately, and a "lock-and-roll" technique then allows smooth continuous tuning across the sweep. A self-calibrating discriminator-stabilized swept oscillator technique, described in the article beginning on page 13, obtains the low phase noise and residual FM required to meet the stringent requirements of narrowband frequency sweeping (spans as narrow as 100 Hz) while also allowing the instrument to make very wide sweeps (up to 20

Fig. 1. *The Hewlett-Packard Model 8566A Spectrum Analyzer has a frequency range of 100 Hz to 22 GHz and an amplitude range of −134 dBm to +30 dBm. The 10-Hz minimum resolution bandwidth is useful to 22 GHz. For the majority of measurements, only the dark-colored keys need be used to select the frequency span and amplitude reference level and to set the tunable markers for frequency and amplitude readout. The other parameters are selected automatically and all control settings are displayed on the CRT.*

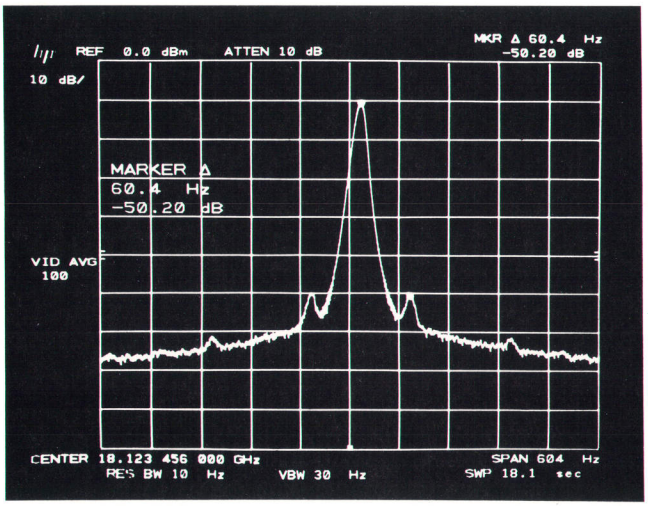


Fig. 2. *Spectrum display of an 18-GHz signal made by the Model 8566A Spectrum Analyzer with a 10-Hz resolution bandwidth across a frequency scan of 600 Hz. The Δ marker (rightmost brightened dot) is positioned on a 60-Hz line-related sideband that is 50 dB below the carrier. Until now, this high degree of resolution, made possible by the low phase noise and 10-Hz resolution bandwidth of the 8566A, had not been available in microwave spectrum analyzers.*

GHz wide).

Unprecedented flatness in the new analyzer's frequency response was made possible by extensive use of microcircuit technology. Ideally, front-end circuit elements should be small compared to the wavelength of the input signal so the elements will behave as lumped circuit constants even at the highest frequencies encountered. The front end of a microwave spectrum analyzer, however, has to process signals of extremely short wavelengths, e.g., 15 mm at 20 GHz. Consequently, the input preselector filter of the new analyzer was integrated with the input mixer to achieve the response flatness desired, as will be described in the article beginning on page 8.

Microprocessor Control

Similar in organization to the 100-Hz-to-1500-MHz Model 8568A Spectrum Analyzer,[1] the new Model 8566A uses microprocessors for instrument control, for display data processing, and for operation on the HP interface bus (HP-IB).* A block diagram is shown in Fig. 3. As is commonly done in spectrum analyzers, the input signal goes through a series of frequency conversions to a fixed IF frequency (21.4 MHz) where the resolution bandwidth filtering takes place. The first local oscillator is swept so the individual frequency components of the input signal are heterodyned one by one into the 21.4 MHz slot for subsequent detection and display on the frequency scale of the CRT display.

The detected video signal is sampled and stored digitally with 1000×1000-point resolution for repetitive read-out by the display circuits. The video detector includes a "rosenfell" detector[2] that enables the display circuits to present a more accurate reconstruction of the video signal than is usually achieved with digital storage of spectrum analyzer signal traces.

Microprocessor control led to the implementation of operating features that are especially useful for a microwave analyzer. For example, the instrument can sweep over its entire 100-Hz-to-22-GHz frequency range without requiring the operator to be concerned with the four bandswitching points. For all frequency spans, the manual tuning control requires the same number of turns (1½) to move a signal across the display, an especially convenient feature in view of the wide range of frequency spans offered, from 100 Hz to 20 GHz. A signal track mode maintains a drifting signal identified by a marker at center screen by automatically retuning the analyzer. The frequency of the drifting signal is also displayed continuously.

Digital storage of a spectrum enables flicker-free viewing even though the instrument may sweep slowly. Digital storage also allows comparisons of two spectra and other data manipulations, such as normalizing a trace (subtracting errors stored during a calibration sweep). With the analyzer's HP-IB port connected to a desktop computer, the stored data can be reformatted in the computer and then displayed in the new format on the analyzer's CRT.

Under computer control, the analyzer can be used for complicated or time-consuming measurement routines with minimum operator involvement. It can also interact through the HP-IB with other instrumentation such as plotters and signal generators. It is thus ideally suited for automatic component test of amplifiers, mixers, and oscillators, as well as for such tasks as spectrum searches for RFI or unknown, intermittent signals. Every front-panel function can be programmed through the HP-IB and additional functions are provided to simplify the data handling between a controller and the instrument.

Quiet, Accurate, Local Oscillator

The capability of resolving low-level signals that lie close to a large signal is a function of the phase noise characteristics of the local oscillator as well as of the analyzer's filter bandwidth and shape factor. The local oscillator's phase-noise characteristics will be impressed on any signal on the spectrum display and could mask the smaller of two signals. To minimize this effect, the synthesized local oscillator of the 8566A was designed for outstanding spectral purity. For example, noise sidebands for input signals up to 5.8 GHz are more than 80 dB below the signal carrier in a 10-Hz bandwidth at 320 Hz offset from the carrier.

Like other microwave oscillators, the new analyzer's local oscillator has a limited tuning range (2-6 GHz) whereas frequency spans of several gigahertz are desirable for microwave spectrum analysis. In addition, the YIG-tuned oscillator commonly used as a local oscillator in microwave spectrum analyzers can be set to a given frequency with an accuracy no better than a few megahertz because of nonlinearities in the magnetic tuning structure. However, for steady-state outputs, much better accuracy can be achieved by phase-locking the oscillator to a known harmonic of a stable lower-frequency reference. This principle is applied to the sweeping local oscillator of the 8566A by initially phase-locking the oscillator to a start frequency accurately synthesized from a stable reference,

*Hewlett-Packard's implementation of ANSI/IEEE 488-1978.

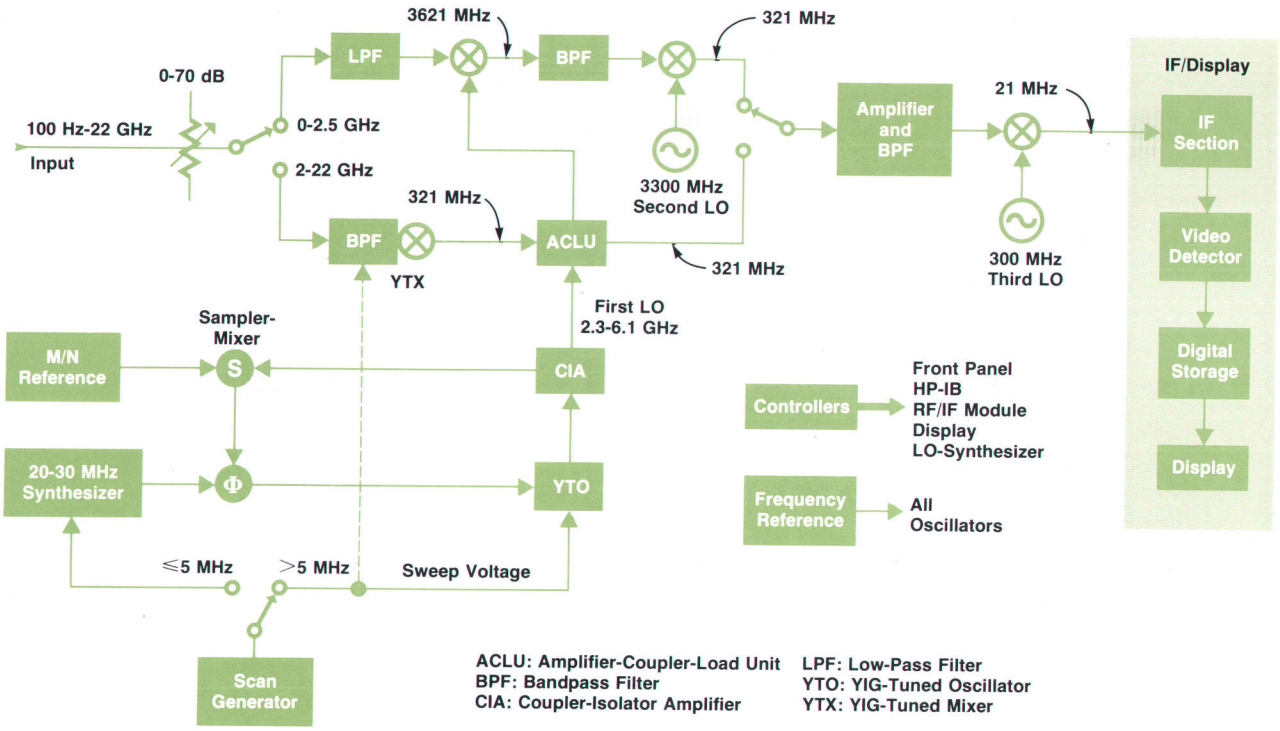


Fig. 3. *Simplified block diagram of the Model 8566A Spectrum Analyzer. Detailed descriptions of the front end and the synthesized first local oscillator will be found in the articles that follow.*

then opening the phase-lock loop while retaining the corrected tuning voltage on a storage capacitor, and adding a precision linear ramp to the tuning voltage to sweep the frequency.

If the selected frequency span exceeds the tuning range of the YIG oscillator, the sweep stops at the end of the tuning range, a new start frequency at the lower edge of the oscillator's range is synthesized, and the sweep continues using the oscillator's next higher harmonic. Known as the "lock-and-roll" technique, this occurs under microprocessor control without any intervention on the part of the operator.

The lock-and-roll approach is used in the 8566A for frequency spans as narrow as 100 Hz and as wide as 22 GHz—over eight decades of span width. An internal, oven-controlled, 10-MHz, crystal frequency standard with a stability of one part in 10^9 per day establishes the basic accuracy of the synthesizer. The start frequencies are synthesized with a resolution of one hertz, and the sweep contributes an error of less than 1% of span width to the resulting stop frequencies, e.g., ±1 Hz for the 100-Hz span. This level of accuracy has not been available for microwave spectrum analysis in the past.

The exceptional stability of the local oscillator allows the use of a 10-Hz resolution bandwidth. Microwave signals, however, often do not have the frequency stability to permit measurements in a 10-Hz bandwidth. Therefore, a wide range of bandwidths is provided in the 8566A so an optimum bandwidth is available for any measuring situation. These range up to 3 MHz in a 1 - 3 - 10 sequence. With this large number of bandwidths to choose from, sweep time can be minimized since sweep time is generally constrained by the selected bandwidth (the sweep time must be slow enough to allow the resolution bandwidth filters to respond to changes in signal level, the allowed time being inversely proportional to the square of the bandwidth).

Sensitivity, Flatness, Distortion

In a broadband receiver such as a spectrum analyzer, a compromise must inevitably be made between sensitivity, frequency-response flatness, and distortion caused by overloading the input mixer. For the 2-to-22-GHz input frequency range, a YIG-tuned preselecting filter in the 8566A improves distortion performance by attenuating large signals lying outside the frequency range of interest. However, the presence of such a filter can degrade flatness because of standing waves that develop as a result of impedance mismatches between the filter and the input mixer. In the past, the solution to this problem was to insert attenuation between the two components. This, however, caused a loss of sensitivity.

Another way to avoid this problem is to keep the length of transmission line between the filter and the mixer much shorter than one-quarter wavelength at the highest frequency of interest, i.e., much less than 3 mm at 22 GHz. This is done in the 8566A by integrating the filter and mixer in a single unit using microcircuit technology. As a result, flatness is better than ±2.2 dB up to 20 GHz and no lossy padding is required. Although the lower conversion efficiency of harmonic mixing degrades sensitivity, sensitivity at 22 GHz is still better than −114 dBm (the highest harmonic used is the fourth).

For the frequency range from 100 Hz to 2.5 GHz, the instrument uses a broadband single-balanced mixer preceded by a low-pass filter. This gives a sensitivity of −134

SUMMARY SPECIFICATIONS

HP Model 8566A Spectrum Analyzer

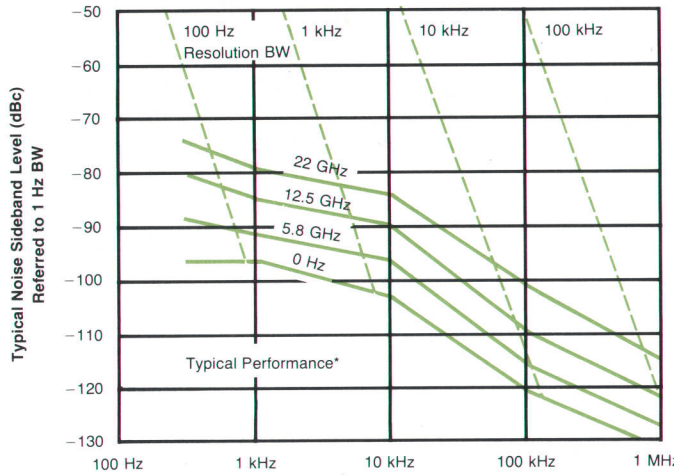
Frequency

RANGE:
100 Hz to 22 GHz.
2 GHz to 22 GHz preselected.
100 Hz to 22 GHz sweep in SINGLE SWEEP mode.

RESOLUTION: 3-dB bandwidths of 10 Hz to 3 MHz in a 1-3-10 sequence.

ACCURACY
FREQUENCY REFERENCE ERROR (AGING RATE):
$<1\times10^{-9}$ /day and $<2\times10^{-7}$ /year.
CENTER FREQUENCY:
Spans ≤5 MHz: ±(2% of frequency span + 10 Hz + frequency reference error × center frequency).
Zero Span: ± frequency reference error × center frequency.
FREQUENCY SPAN:
±1% of indicated separation for spans ≤5 MHz.
±3% of indicated separation for spans >5 MHz.
MARKERS: Same as Center Frequency.

SPECTRAL PURITY: Noise sidebands ≤80 dB below signal, 320 Hz offset, 100 Hz to 5.8 GHz tuned frequency (fundamental mixing) with 10-Hz resolution bandwidth.



Typical Single Sideband Noise Normalized to 1 Hz BW.*

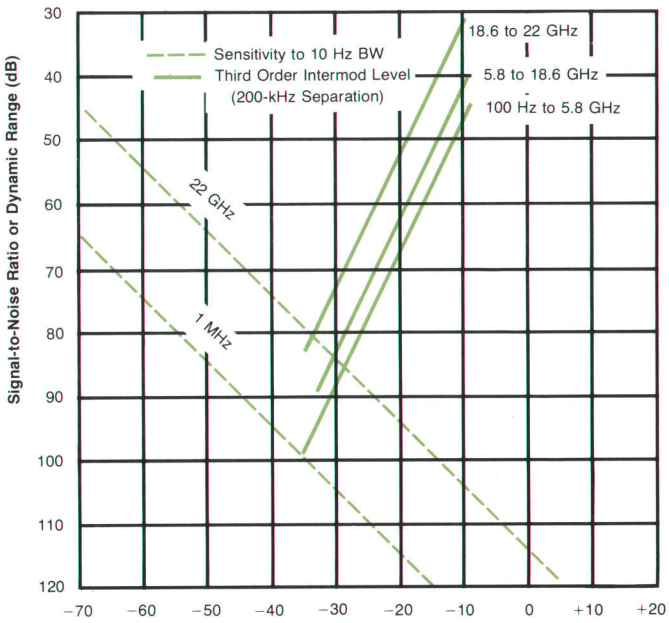
Amplitude

RANGE: −134 dBm to +30 dBm (32 nV to 7.07 volts, 50Ω). Displayed 10, 5, 2, or 1 dB/division or linear on a 10-division linear scale.

DYNAMIC RANGE
SECOND-HARMONIC DISTORTION:
<−80 dBc, 100 Hz to 700 MHz
<−70 dBc, 700 MHz to 2.5 GHz
} −40 dBm mixer level
<−100 dBc, 2.0 GHz to 22 GHz −10 dBm mixer level
THIRD-ORDER INTERMODULATION DISTORTION:
THIRD-ORDER IM INTERCEPT:
Specified { +7 dBm, 100 Hz to 5.8 GHz.
+5 dBm, 5.8 GHz to 18.6 GHz.
Typical* { +12 dBm, 100 Hz to 5.8 GHz.
+10 dBm, 5.8 GHz to 18.6 GHz.
+5 dBm, 18.6 to 22 GHz.
IMAGE AND MULTIPLE RESPONSES: <−70 dBc, 100 Hz to 18.6 GHz.
AVERAGE NOISE LEVEL (SENSITIVITY): For 10-Hz resolution BW:
−134 dBm, 1 MHz to 2.5 GHz.
−132 dBm, 2 GHz to 5.8 GHz.
−125 dBm, 5.8 GHz to 12.5 GHz.
−119 dBm, 12.5 GHz to 18.6 GHz.
−114 dBm, 18.6 GHz to 22 GHz.

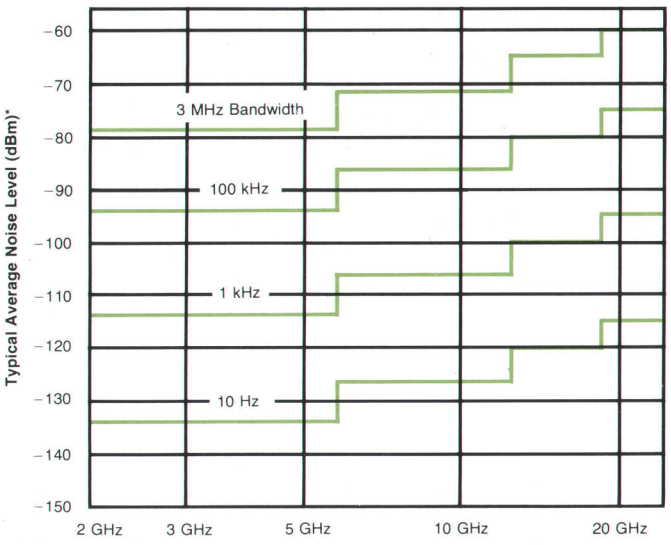
ACCURACY: Measurement accuracy is a function of technique. The following sources for uncertainty can be summed to determine achievable accuracy (at constant ambient temperature, assuming the error correction function and preselector peak have been used, and avoiding unnecessary control changes between calibration and measurement).
CALIBRATOR UNCERTAINTY: ±0.3 dB.

*Typical, non-warranted performance parameters useful in applying the instrument.



Typical Optimum Dynamic Range.*

FREQUENCY RESPONSE UNCERTAINTY (FLATNESS):
±0.6 dB, 100 Hz to 2.5 GHz.
±1.7 dB, 2.5 GHz to 12.5 GHz.
±2.2 dB, 12.5 GHz to 20 GHz.
±3 dB, 20 GHz to 22 GHz
COMPARISON UNCERTAINTY (resulting from one of the following techniques for comparing the unknown signal with the calibrator):
REPOSITIONING SIGNAL TO CALIBRATION LEVEL: ±1.2 dB*.
USING MARKER: ±3.2 dB*.



Average Displayed Noise Level

(continued)

Sweep

SWEEP TIME: 20 ms full span to 1500 s full span. Zero Frequency Span, 1 μs full sweep (of display) to 1500 s full sweep.

Input

RF INPUT: 100 Hz to 22 GHz, 50Ω dc coupled. Precision Type N female. Diode limiter 100 Hz to 2.5 GHz. Preselected 2.0 to 22 GHz.

MAXIMUM INPUT LEVEL

AC: +30 dBm (1 watt) continuous power.

DC: <100 mA current damage level.

ATTENUATOR: 70-dB range in 10-dB steps.

Outputs

FIRST LOCAL OSCILLATOR: 2.3 GHz to 6.1 GHz; > +5 dBm into 50Ω.

DISPLAY: X, Y, and Z outputs for auxiliary CRT display.

RECORDER: Horizontal sweep output (X), video output (Y), and penlift/blanking output (Z) to drive an X-Y recorder.

Instrument State Storage

Up to 6 sets of user defined control settings may be saved and recalled.

Remote Operation

All analyzer control settings (with the exception of video trigger level, focus, align, intensity, frequency zero, amplitude cal, and line power) may be programmed via the Hewlett-Packard Interface Bus (HP-IB).

General

ENVIRONMENTAL: Operation 0°C to 55°C. <95% relative humidity, 0°C to 40°C.

EMI: Conducted and radiated interference is within the requirements of CE 03 and RE 02 of MIL STD 461A, and within the requirements of VDE 0871 and CISPR publication 11.

WARM-UP TIME

OPERATION: Requires 30 minute warm-up from cold start, 0° to 55°C. Internal temperature equilibrium is reached after 2 hr. warm-up at stable outside temperature.

FREQUENCY REFERENCE: Aging rate attained after 24 hr. warm-up from cold start at 25°C. Frequency is within 1×10^{-8} of final stabilized frequency within 30 minutes.

POWER REQUIREMENTS: 50 to 60 Hz; 100, 120, 220 or 240 volts (+5%, −10%); approximately 650 VA (40 VA in standby). 400 Hz operation available.

WEIGHT: 50 kg (112 lb).

DIMENSIONS: 280 mm H × 426 mm W × 600 mm D (11 × 16¾ × 23½ in).

PRICE IN U.S.A.: $47,500. 400-Hz operation, add $400.

MANUFACTURING DIVISION: SANTA ROSA DIVISION
1400 Fountain Grove Parkway
Santa Rosa, California 95404 U.S.A.

dBm, a flatness of ±0.6 dB, and a third-order intermodulation intercept point of +7 dBm for closely-spaced signals. The input signal is automatically switched to the appropriate mixer by the microprocessor according to the frequency span selected.

The combination of high-performance analog circuit components and internal data handling by microprocessors has resulted in a spectrum analyzer that sets new standards for measurement capability and user convenience in the microwave frequency range.

Acknowledgments

The development of the Model 8566A Spectrum Analyzer extended over several years and involved a great number of people. Many different approaches to the microwave front end, the LO synthesizer, and the measurement display were investigated. Some proved to be impractical, others became key elements for other instruments, such as the 86290A Sweeper and its YIG-tuned multiplier, and the signal synthesis scheme used in the 8672A Synthesized Signal Generator.

Much help with the system definition, plus encouragement and support despite lengthening schedules, came from Rit Keiter, Santa Rosa engineering lab manager (now general manager for the Santa Rosa spectrum analyzer operations). His ideas, together with those of Dave Eng, industrial design manager, and of many others, formed the basis for an easy-to-interface front panel that combined the feel of a knob-controlled analog instrument with the precision of a keyboard-controlled digital machine.

In addition to those mentioned in the following articles, recognition should go to the following for their contributions to the 8566A: Irv Hawley, spectrum analyzer section manager (now R&D manager for the network measurement operation at Santa Rosa), who always maintained the flow of resources and, with critical questions, kept the project on track; Ron Trelle, for the overall product design with particular attention to cooling, shielding and vibration control; Art Upham, for the design of the third converter, YTX driver, and miscellaneous circuitry whenever the need arose; Rich Pope, for the second LO phaselock loop and electronic test tools for the YTX production; Rex Bullinger, for the HP-IB interface; Lynn Wheelwright, for his support in developing the digital control system, and Dee Humpherys and his design team for the development of the IF/display section.

Numerous other people in many areas of Hewlett-Packard contributed to the project. Many of their contributions, like GaAs FETs and YIG spheres, are buried deep inside the instrument and are barely visible even on a detailed block diagram. Yet it was this joint effort—true teamwork—that made the 8566A project succeed.

References

1. S.N. Holdaway and M.D. Humpherys, "The Next Generation RF Spectrum Analyzer," Hewlett-Packard Journal, June 1978.
2. S.N. Holdaway, D.H. Molinari, S.H. Linkwitz, and M.J. Neering, "Signal Processing in the Model 8568A Spectrum Analyzer," Hewlett-Packard Journal, June 1978.

Siegfried H. Linkwitz

Born in Bad Oeynhausen, Germany, Siegfried Linkwitz is a 1961 graduate (Diplom Ingenieur) of Darmstadt University, Germany. Siegfried joined HP shortly after graduation and has since worked on vector voltmeters, signal generators, sweepers, and spectrum analyzers (including the 8566A, for which he was program manager). A resident of Santa Rosa, California, Siegfried is married and has one son, 14, and one daughter, 16. In his spare time, he enjoys windsurfing, skiing, and designing hi-fi equipment. A member of the Creative Initiative Foundation, he also leads groups on fulfilled living.

Broadband Input Mixers for a Microwave Spectrum Analyzer

by John C. Lamy and Frank K. David

TO PROVIDE THE USER with state-of-the-art spectrum analyzer performance over a broad range of frequencies, a dual front-end approach was chosen for the Model 8566A Spectrum Analyzer. The input section has two independent heterodyne conversion channels: a 2-to-22 GHz YIG-preselected harmonic mixer chain, and a 100-Hz-to-2.5-GHz up-down converter chain. As indicated in Fig. 1, these alternative paths are selected automatically by a mechanical relay that is under control of a microprocessor.

The dual approach was chosen because present-day YIG technology, which provides the analyzer's spurious-free microwave performance, is not applicable at lower frequencies. The use of two techniques enables top performance over the full 100-Hz-to-22-GHz operating range of the instrument.

2-to-22-GHz Band

The 2-to-22-GHz band on the 8566A is a modern implementation of a classical concept: a multiconversion heterodyne receiver with a broadband input mixer. Much of the system's performance depends on the input mixer, which converts the input signal frequency to a fixed IF. When the frequency of the sweeping local oscillator (YTO) equals the input signal plus or minus the first IF, a response is generated in the IF detector. The response appears as a pulse on the display, which sweeps in synchronism with the LO as the LO sweeps the signal past the IF.

The broadband front-end mixer traditionally reduces to an extremely simple piece of hardware: a single diode in a

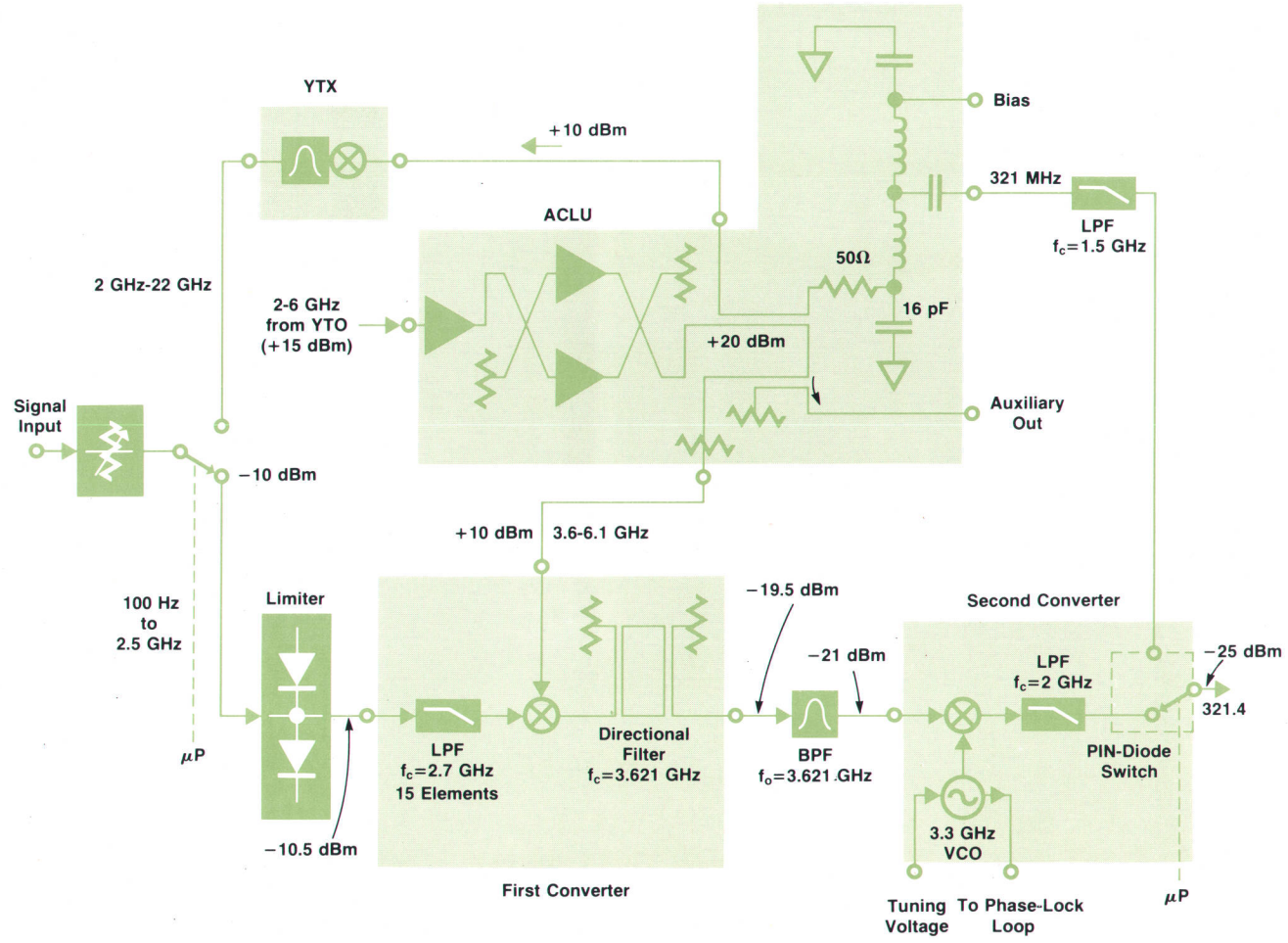


Fig. 1. *Block diagram of the input section of the Model 8566A Spectrum Analyzer. The control microprocessor selects the appropriate signal path according to the frequency span selected.*

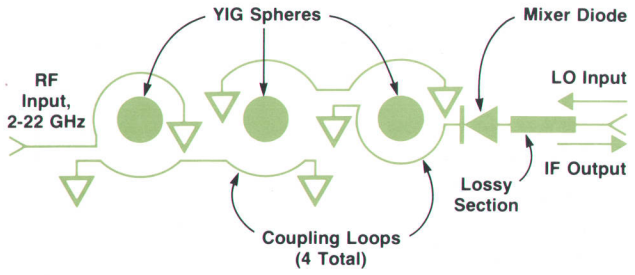


Fig. 2. *Schematic representation of the YIG-tuned filter and mixer (YTX) used in the 8566A. Although this shows all the coupling loops in the same plane, the two loops for each YIG sphere cross at an angle so coupling occurs only at the resonant frequency of the YIG sphere, which is a function of the dc magnetic field strength.*

structure made small compared to the wavelength of the signal, LO, and IF frequencies.

Simple? Yes, except that there is a great deal more involved than appears on the surface. Four kinds of unwanted responses are generated along with the wanted response: those resulting from image frequencies, multiples (frequencies that beat with harmonics of the LO), out-of-band signals, and signal harmonics. The traditional solution to the problem is to precede the input mixer with a tunable narrow-band filter that tracks the frequency tuning of the analyzer. This suppresses the unwanted responses but trades off performance because of the impedance mismatch between the preselector filter and the mixer. The mismatch causes standing waves to develop on the transmission line between them, introducing substantial variations in the analyzer's frequency response. The solution to that problem has been to insert attenuation between the preselector and the mixer, which results in some loss of sensitivity.

In short, the preselector eliminates unwanted responses but forces a trade-off between flatness and sensitivity, two key performance characteristics of the analyzer.

The YIG-Tuned Mixer

This trade-off was eliminated in the 8566A by integrating the mixer diode with the YIG-tuned preselector such that there is essentially zero line length between them. The complete structure is called the YIG-tuned mixer, or YTX.

Operation of the high-band front-end system can be explained with reference to Fig. 1. The 2-to-6-GHz swept LO signal is applied to the ACLU (amplifier-coupler-load unit) where it is amplified and leveled by a saturating FET amplifier. It is then coupled to the main line where it travels to the YTX diode, switching the diode on and off. The on-off ratio (conduction angle) is controlled by the dc bias applied through the bias port of the ACLU. Different conduction angles are chosen for the various harmonics of the LO, enabling operation to 22 GHz.

Three YIG spheres with their coupling loops form the YTX bandpass filter, as shown in Fig. 2. The filter is tuned to the analyzer's instantaneous frequency by varying the applied magnetic field. An input signal passing through the filter is alternately transmitted and reflected back by the mixer diode as the diode switches on and off. Frequencies above 2 GHz in the transmitted part terminate in the 50Ω resistor of the ACLU. The 321-MHz IF generated at the mixer diode passes through the ACLU tuned circuit and into the IF section. Because of the preselector, it is not necessary to use a relatively high first IF to space the image frequency far enough from the desired signal to make it easy to deal with, another advantage of the preselector approach.

The YTX is designed to mix on the first through fourth harmonics of the LO. The control microprocessor selects the appropriate harmonic so the harmonic bandwitching is transparent to the user.

Design Considerations

Although the use of microcircuitry solved the major problems, there were others that had to be dealt with. The first was how to guarantee 70-dB rejection of unwanted signals. A rule of thumb in YIG filter design is that each resonator sphere can contribute about 25 dB of stopband isolation, so three spheres seemed to be about right. But then, how do you guarantee that all three spheres are subject to the same magnetic field intensity as the intensity is varied over a 10-to-1 range? The error can be no more than 1 part in 2000, equivalent to a tuning error of 10 MHz, or one-half the preselector 3-dB bandwidth at a center frequency of 20 GHz. Since the H field is controlled by the 1.35-mm (0.054-inch) gap in the electromagnet, a 1/2000 error is less than 0.75 μm (30 millionths of an inch) of pole-face nonparallelism, virtually impossible to hold in production since it would be the sum of machining tolerances in three relatively large pieces of steel.

The usual way to maintain acceptable parallelism in a multi-sphere structure has been to shim the pieces with tape at strategic points. The way used for the YTX is to intentionally grind the pole faces with a slight tilt and then,

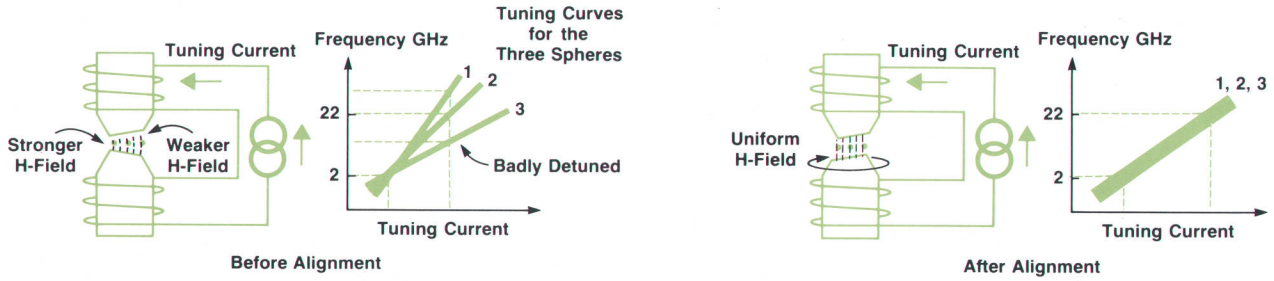


Fig. 3. *Misalignment of the tuning magnet pole faces, shown exaggerated here, causes the three YIG spheres to have different tuning characteristics. Rotating the pole pieces to bring the tilted faces into parallel alignment achieves identical tuning characteristics for the three spheres.*

Precision Assembly of a YIG-Tuned Mixer

Examination of the YIG-tuned mixer for the Model 8566A Spectrum Analyzer indicated that it could not be manufactured by traditional manufacturing methods. To maintain the designer's intent while achieving efficient fixturing it was concluded that the engineer who did the mechanical design of the YTX should also develop the tooling for manufacturing. In this way, it would be possible to avoid the problems that occur when a manufacturing engineer develops concepts that differ from the design engineer's. This placed a heavy burden on the design engineer as the assembly fixturing was constantly being evaluated and changed, but it paid off in that the final design was nicely manufacturable.

A photograph of the interior of the YTX is shown in Fig. 1. The main part is the circular piece with the three holes where the YIG spheres are located. This part is molded of Fiberite and then gold-plated. The D-shaped part surrounding it is made of copper for good heat conduction. The small microcircuit at the upper right corner is a heater and the device at the lower right corner where the flying lead connects is a thermistor. The heater maintains the YIG spheres at a slightly elevated temperature so their temperature can be held constant during fluctuations in the ambient.

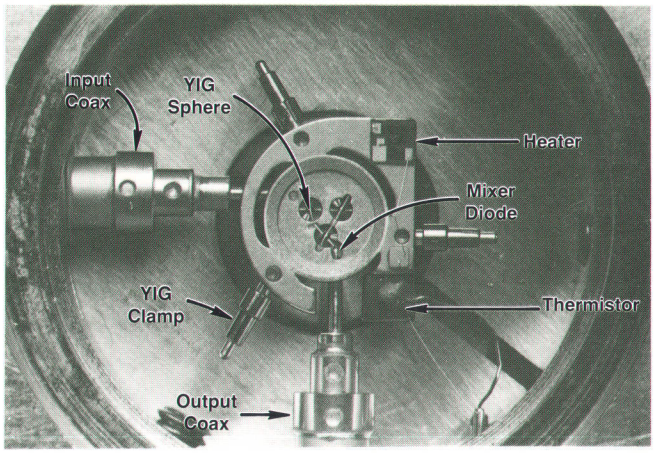


Fig. 1. *Internal view of the YIG-tuned mixer (YTX). The circular part that has the three holes for the YIG spheres is only 9 mm in diameter.*

The thermal circuit to the three YIG spheres is completed by metal rods that are held in cylindrical spring-loaded clamp circuits, shown protruding from the D ring. The rod ends are accessible through plug-holes in the external magnet structure so, with the magnets in place, the rods can be rotated and moved axially to find the position for best temperature compensation. This adjustability is obtained while maintaining good thermal contact. The clamps are firm enough to obviate the need for any additional clamping device or cement to prevent movement during shock and vibration.

The YIG sphere coupling loops are just visible in the photo. Only 50 μm (0.002 inch) thick, these have to be dimensioned and positioned very precisely. For example, the distance between a loop and a YIG sphere must not vary by more than 25 μm (0.001 inch). It would be very difficult for even a highly skilled person to form and position these loops with the precision required. This problem was solved by using state-of-the-art chemical milling techniques to mill the loops from beryllium copper, obtaining sturdy parts with a tolerance of ±5 μm (0.0002 inch) and excellent repeatability. These are checked in the assembly area with an optical comparator just before assembly.

Molding on the Production Line

Molding of the dielectric for the coaxial sections presented some special problems. Injection molding was considered but rejected because of the fragility of the coax parts (there is a 665-to-172-μm center conductor transition) and the fear that the air-filled microballoons required to obtain the correct dielectric constant could separate from the resin and fillers when exposed to restricted flow under high pressure. Tooling was developed that would allow the center conductor to be inserted and positioned accurately after the outer section is filled with the dielectric in a plastic state. The assembled unit is then cured in a pressure vessel to minimize any expansion of trapped air due to the elevated curing temperature. After the curing, the lead lengths and excess epoxy are trimmed, and then the coax assembly is tested with a time-domain reflectometer to assure its acceptability. All of these operations are performed in the final assembly area to assure maintenance of the tolerances desired.

Special Soldering Techniques

A key element in the mounting of the very small parts was the use of solder cream (solder granules suspended in flux). It is used as a liquid preform that enabled us to solder parts that could not be soldered by conventional means.

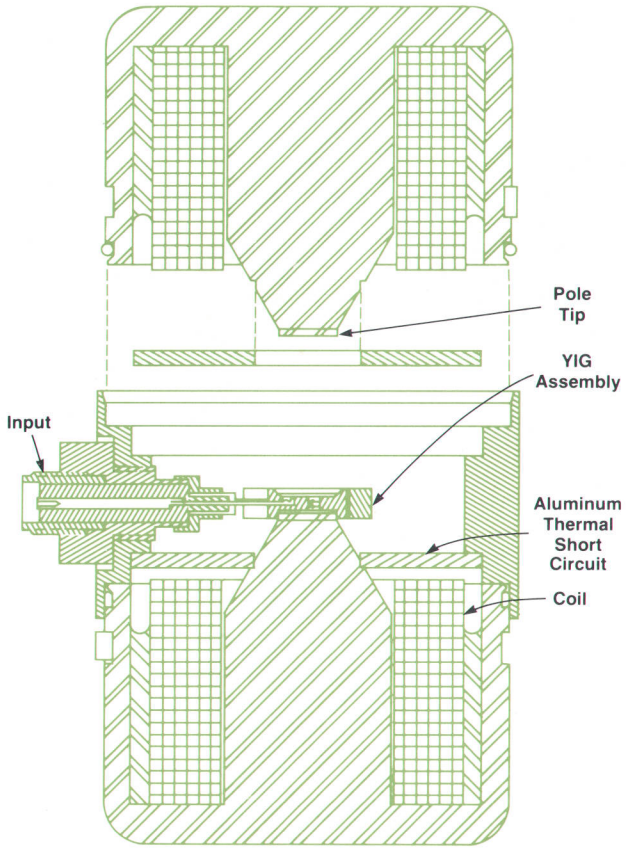


Fig. 2. *Cross-section of the YTX.*

It became apparent that soldering the entire structure at one time was impractical, so some means had to be found that would allow soldering without reflowing previously-made solder joints. The solution was to use solders with higher melting temperatures for the early operations. As a result, it is possible to solder the coax sections to the assembled central unit during final operations, obtaining a well-bonded grounding structure.

Thermal Design of the Magnet

A major objective was to provide a constant, uniform magnetic flux under all environmental conditions. A cross-section of the magnetic structure with the YIG-sphere assembly in place is shown in Fig. 2. The pole tips of the magnet are made of a material that has a different thermal expansion ratio from the main body so the magnet gap remains constant despite changes in the ambient temperature.

However, some short-term differential heating of the magnet occurs whenever the tuning coil current is changed with the greatest change occurring at the high end of the YIG tuning range where the current is proportionately high. Because of the relatively poor thermal conductivity of the nickel-iron alloys used, a temperature gradient would exist between the poles and the main body since the outside surface dissipates heat more readily than the pole faces. This results in changes in the gap spacing, hence in the YIG tuning. This problem was minimized by installing aluminum discs between the pole faces and the outer ring as shown in Fig. 2. These serve as thermal short circuits between the pole faces and the magnet body reducing the differential heating by a factor of 10 (a single slot cut radially in each disc prevents the formation of eddy currents). Residual short-term temperature differentials are compensated for by the microprocessor control system (see box, page 15).

Acknowledgments

Special thanks are due Earl Heldt of the Stanford Park Division for the original mechanical design. Dick Lyon made major contributions to the design. Pete Planting developed the microballoon material and provided technical support for the soldering processes.

-Lee Olmstead

with the structure assembled, use a desktop computer test program that indicates to the test technician how much the pole pieces should be rotated with respect to each other around their common axis so the tilt in one pole face will match the tilt in the other (Fig. 3). The computer controls test instruments that make frequency response curves as the filter is tuned throughout the 2-to-22-GHz range. Misalignment of the pole faces causes the frequency response curves to have three humps. The technician measures the frequency separation between adjacent humps and enters this value into the computer, which then calculates the amount of rotation required to bring the pole faces into alignment. Usually, one pass is sufficient to achieve virtually perfect parallelism. This procedure takes less than 15 minutes.

A second problem concerned the impedance match looking from the diode toward the ACLU load where the input signals would normally terminate. To meet our flatness goals, the return loss had to exceed 20 dB over the entire 2-to-22-GHz range. Although this can be done up to 6 GHz, it is unrealistic to expect this performance of the SMA connector pairs used for the connections, not to mention the transitions from coax to microstrip and so on. To surmount this problem, the YTX uses polyiron-loaded dielectric in a specially designed molded coax assembly (Fig. 2). The polyiron is lossless at the IF and LO frequencies, but above 6 GHz it becomes lossy and acts as a good termination to signals above 12 GHz, giving outstanding flatness.

Amplifier/Coupler/Load Unit

Of the several functions that the amplifier/coupler/load unit (ACLU) performs, its contribution to the high-band flatness is most noteworthy.

First, it provides a relatively constant LO power to the YTX's single-diode harmonic mixer. For some harmonics, the mixer's conversion efficiency is a function of the diode's conduction angle, and the conduction angle changes with changing LO power level. The FET amplifier in the ACLU operates in a saturated mode, and therefore provides gain compression that greatly reduces the YTO power variations that exist unit-to-unit and as a function of frequency and temperature. The amount of gain compression is shown in Fig. 4.

The second contribution to flatness is the isolation and match that the coupler load portion of the ACLU provides for the signal input to the YTX. Input signals in the 2-to-22-GHz range go into the YTX, mix in the diode, and then go into the ACLU. If any significant portion of this signal reflects off the ACLU's input and returns to the YTX, ripple will be produced in the YTX's conversion efficiency. This doesn't happen, due in part to the isolation from the amplifier's output provided by the coupler, and also to the termination provided by the 50Ω thin-film resistor. The 50Ω resistor is ac-coupled to ground through the 16-pF capacitor (see Fig. 1) such that it terminates frequencies of 2 GHz on up, but allows 321 MHz to exit the IF port with only small loss (about 3 dB). The 16-pF capacitor and some thin-film inductors provide a 321-MHz tuned matching network to match the nominal 50Ω IF impedance to the series combination of the 50Ω resistor and the mixing diode in the YTX (a combination of approximately 150Ω).

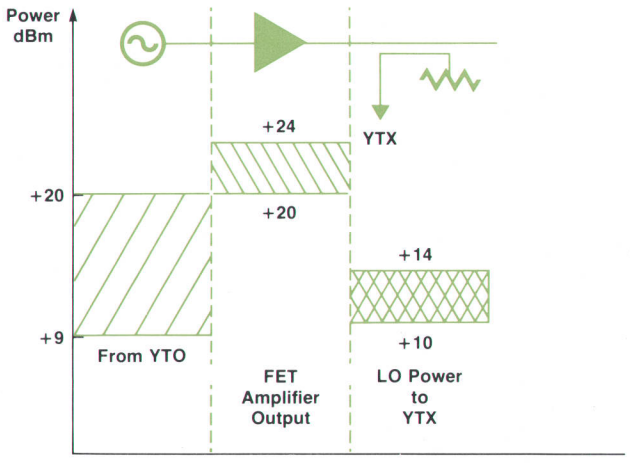


Fig. 4. *Variations in the local oscillator power supplied to the mixer diode are compressed by operating the FET amplifier in a saturated mode.*

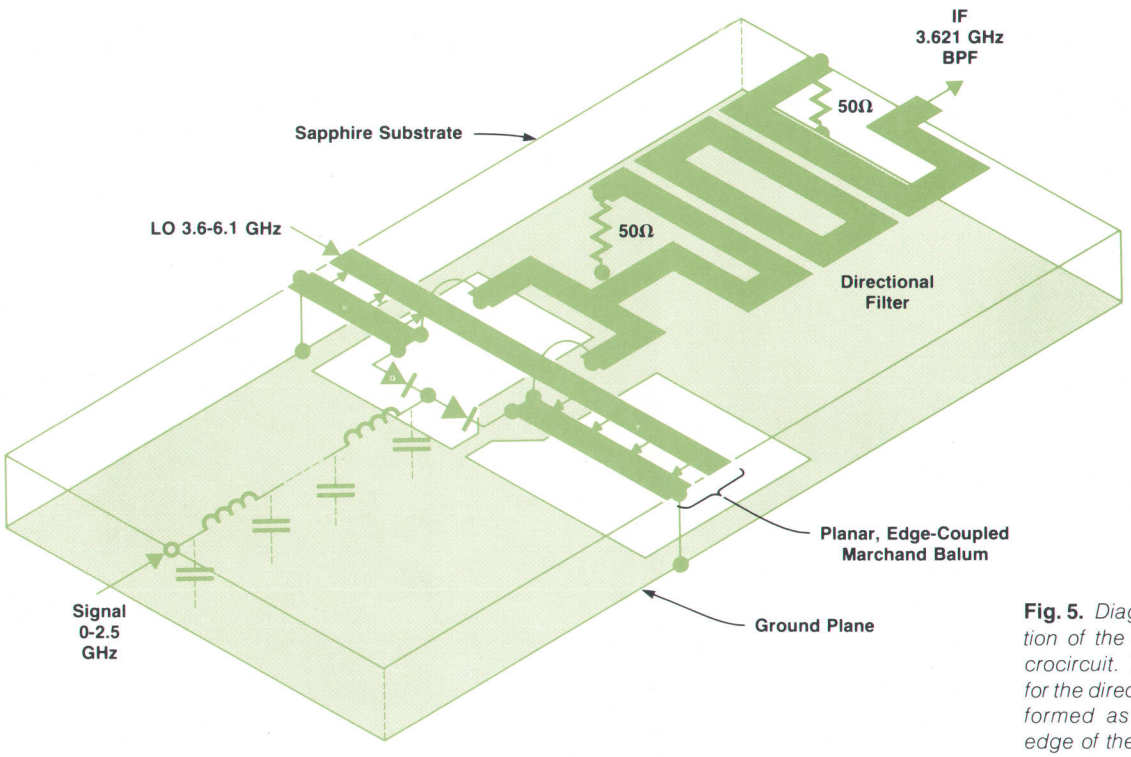


Fig. 5. *Diagrammatic representation of the second converter microcircuit. The 50Ω terminations for the directional filter are actually formed as thin films along the edge of the substrate.*

0-to-2.5-GHz Band

As shown in Fig. 1, the ACLU is the supplier of local oscillator power for both frequency bands. To remove the problem of image response in the 0-to-2.5-GHz band, a double frequency conversion is performed on the input signal. First there's an up-conversion to a fixed 3.6-GHz IF and then, after some filtering, a down-conversion to a 321-MHz IF.

Although the image response is effectively removed by this technique, the added components compound the problem of trying to fit maximum performance into minimum space. This problem was kept in check by using thin-film technology and a high degree of integration of components. Microcircuit technology is used in the assembly of the limiter, first converter, second converter, and ACLU.

Limiter

The limiter's function is to reduce the burn-out susceptibility of the first-converter mixing diodes from an overload at the input. It does this very well for CW input powers between 1 milliwatt (onset of limiting action) to 10 watts. When not limiting, the device is virtually transparent to the incoming signal (loss <1 dB, VSWR <1.25). A back-to-back diode arrangement eliminates the need for dc blocks or returns allowing the limiter to operate to very low frequencies, even dc.

First Converter

The first converter is designed to achieve a good balance of flatness, low distortion, and conversion efficiency. Because the frequency response and distortion characteristics in the 0-to-2.5-GHz range are determined primarily by the first converter's conversion flatness and distortion, these parameters were optimized in a trade-off with conversion efficiency, giving a flatness of ± 0.6 dB for the input signal range of 100 Hz to 2.5 GHz. For a -30-dBm input to the first converter, the harmonic distortion and third-order distortion products are 70 dBc and 90 dBc respectively over the range of 100 Hz to 700 MHz, which covers the important communication bands.

Several specific parts of the first converter, shown in Fig. 5, contribute significantly to its good performance. The planar, edge-coupled, realization of a Marchand balun,[1] which carries the LO signal to the diodes, contributes to good flatness by isolating the signal and IF paths from the LO port. Distortion is reduced by bringing the LO in on the broadband, balanced structure. Distortion is further reduced by use of an integrated dual beam-lead diode that has closely matched parameters for each of the diodes in the pair. Finally the directional filter is crucial in achieving good flatness without excessive reduction in conversion efficiency. This filter passes the 3.6-GHz IF with minimal insertion loss while providing a good resistive termination for all of the other frequencies produced in the mixer.

Second Converter

The second converter achieves its function in a small volume with good efficiency and low phase noise.

The 3.3-GHz VCO in the second converter is a push-pull two-transistor oscillator using a microstrip horseshoe resonator.[2] Typically, microstrip resonators have comparatively low unloaded Q (around 250), and hence are not noted for particularly low phase noise when used in oscillators. By optimizing the resonator's dimensions (for maximum unloaded Q) and by running low bias current in the transistors (7 mA per transistor) the loaded Q of the oscillator was improved to the point that at 1 MHz away from the carrier, phase noise in this oscillator is as low as

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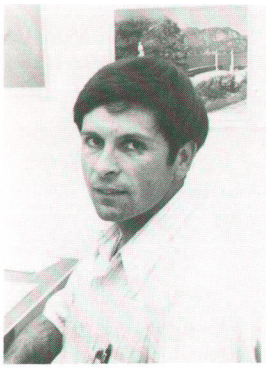
With HP since 1968, John Lamy was project leader for the 85660A RF Module, the 8557A Spectrum Analyzer, and the 435A/8481A Power Meter, and was design engineer for the 8555A spectrum analyzer tuning section. John was born in Kansas City, Missouri, and received his BSEE degree in 1968 from Massachusetts Institute of Technology. Now a resident of Santa Rosa, California, he is married and has a seven-year-old son. In his spare time, John enjoys backpacking and sailing and is actively involved in the Creative Initiative Foundation.



Frank K. David
An HP employee since 1969, Frank David was project engineer for the 8566A microcircuits, including the low-range front end mixer, filters, oscillator, and limiter. Frank received his BSEE degree in 1965 from the University of California at Berkeley and his MSEE degree in 1975 from Oregon State University. A native of Sacramento, California, he is married and has two "active" children (ages six and three). Frank spends much of his leisure time landscaping his yard, doing masonry work, and camping with his family.

that in a typical YIG-tuned oscillator (−135 dBc/Hz). The close-in phase noise performance is improved by phase-locking the oscillator to a harmonic of the instrument's 100-MHz reference frequency. A microcircuit sampler serves as the phase detector. It samples the 3.3-GHz signal at the 100-MHz rate and the resulting dc is used to control the VCO.

The conversion efficiency of this converter was enhanced by taking advantage of the fact that the frequencies at all three mixer ports are fixed. These ports are tuned so as to reflect the energy of higher mixing products back to the mixing diodes where they are reconverted to the IF frequency. This raises the conversion efficiency, which initially was 25%, up to 40%.

Acknowledgments

Far more people participated in the design and introduction of these microwave components than we can adequately acknowledge here—it has been truly a large scale team effort. Two contributors stand out on the YTX: Rit Keiter for initial concept and continuing guidance, and Robert Joly for establishing the basic realization.

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1. N. Marchand, "Transmission Line Conversion Transformers," Electronics, December 1944.
2. R.E. Pratt, R.W. Austin, and A Dethlefsen, "Microcircuits for the Microwave Sweeper." Hewlett-Packard Journal, November 1970.

A Synthesized Microwave Local Oscillator with Continuous-Sweep Capability

by Larry R. Martin, Kenneth L. Lange, and Stephen T. Sparks

THE FREQUENCY ACCURACY and stability of the Model 8566A Spectrum Analyzer allows the use of a resolution bandwidth of 10 Hz anywhere within the 100-Hz-to-22-GHz range of the instrument. The instrument's accuracy, stability, and sensitivity also give it the ability to measure microwave frequencies at very low signal levels with an accuracy approaching that of the best microwave frequency counters. The low phase noise enables the analyzer to make measurements in the audio frequency range as well as the RF and microwave ranges, and in many cases allows it to measure the phase noise of microwave oscillators directly.

Performance of this caliber requires synthesizer accuracy in the local oscillators. To achieve this accuracy along with a sweeping capability, the frequency-conversion chain in the Model 8566A uses seven phase-locked loops, two of which have direct sweeping capability. A block diagram is shown in Fig. 1.

When the analyzer's input frequency is in the 0-to-2.5 GHz range where the broadband front end is used, the instrument operates as a conventional high-IF machine with a first IF of 3.6214 GHz. A 3.3-GHz source reduces this IF to a second IF of 321.4 MHz, which is further down-converted by a 300-MHz signal to a final IF of 21.4 MHz. When the input frequency is in the 2-to-22-GHz range where the preselector is used, the 321.4-MHz IF becomes the first IF and the 3.3-GHz source is disabled.

The YTO (YIG-tuned oscillator) loop shown in Fig. 1 is the final summing loop of the synthesizer system that functions as the first local oscillator in both frequency ranges. The inputs to this loop are a fixed reference frequency from the M/N loop, a fixed or swept frequency from the low-

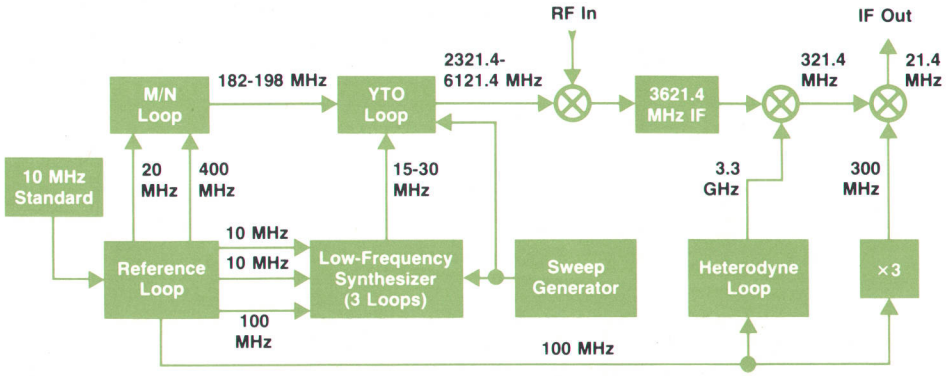

Fig. 1. *Frequency conversion chain uses seven phase-locked loops, two of which can be swept. All are referenced to a 10-MHz oven-controlled crystal frequency standard that has an aging rate of less than one part in 10^9 per day.*

frequency synthesizer, depending on the sweep range, and a sweep control from the sweep generator, also depending on the sweep range. The M/N loop provides YTO tuning steps in 10-MHz increments and the low-frequency synthesizer interpolates between the 10-MHz steps.

Before the start of a frequency scan, the YTO is tuned by a 12-bit digital-to-analog converter (DAC) such that its unlocked frequency lies 20 to 30 MHz below the Nth harmonic of the M/N loop output. The YTO output is mixed with the Nth harmonic and the resulting difference frequency is applied to a phase-frequency detector, as shown in Fig. 2. The other input to the phase-frequency detector comes from the low-frequency synthesizer. When the loop is closed the output of the phase detector is applied to the YTO tuning coils, forcing the YTO to track a combination of the M/N loop and low-frequency synthesizer frequencies.

The output frequency of the M/N loop, which ranges between 182 and 198 MHz, is defined by the equation:

$$f_{M/N} = 200 - 10M/N \text{ MHz}$$

so the Nth harmonic is 200N−10M. Thus, the frequency of the YTO loop in the locked condition is:

$$f_{YTO} = 200N - 10M - f_{lfs} \text{ MHz}$$

where f_{lfs}, the output of the low-frequency synthesizer, can be varied between 20 and 30 MHz in 1-Hz steps when setting a start frequency.

For frequency sweeps greater than 5 MHz, the M/N loop and the low-frequency synthesizer establish a precise start frequency, as determined by the main control microprocessor in response to the front-panel or HP-IB inputs. The YTO control voltage for this frequency is then retained on a capacitor, the YTO phase-lock loop is opened, and the sweep voltage is added to the YTO tuning voltage (see Fig. 2). When the frequency sweep is less than 5 MHz, the frequency sweep is generated within the low-frequency synthesizer and the YTO remains phase-locked to it and the M/N loop throughout the sweep.

10-MHz Increments

The high-purity M/N output originates in a voltage-controlled oscillator (VCO) that uses the same type of fore-

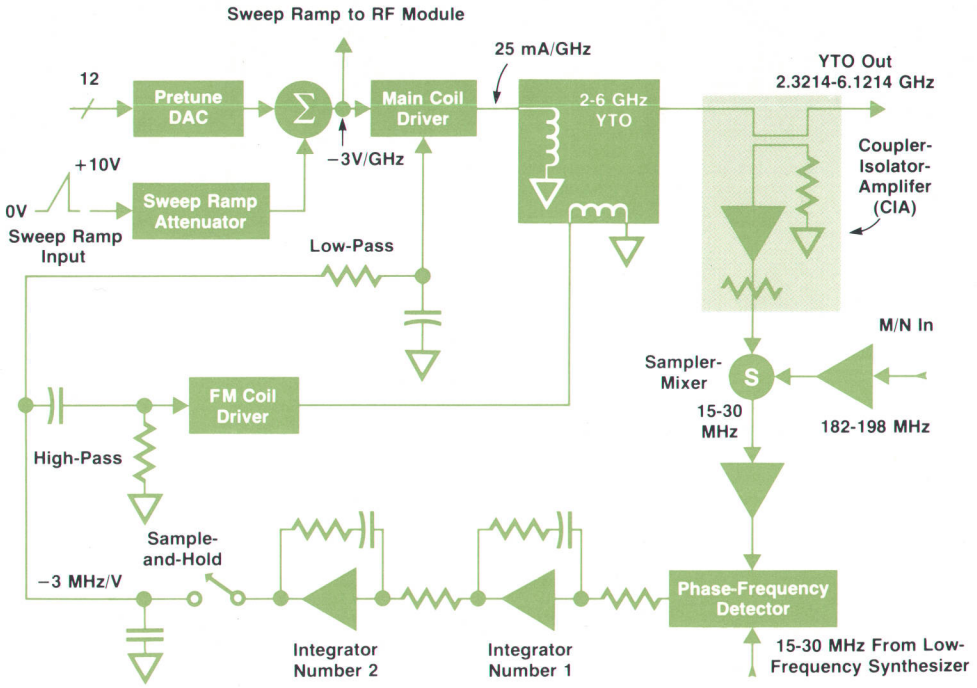

Fig. 2. *YTO (YIG-tuned oscillator) control loop locks the YTO to a combination of the M/N and low-frequency-synthesizer loop frequencies.*

Some Microprocessor Contributions to Spectrum Analyzer Performance

by Michael S. Marzalek

The new Model 8566A Spectrum Analyzer uses virtually the same digital hardware as the Model 8568A.[1] In fact, both instruments share the same IF/Display unit, which means they are identical from the 21-MHz third IF on through the video detector to the display processing circuits. The differences, from the digital point of view, are in the control of the front end and the first and second IF stages.

Because of the fundamental differences between the analog circuits in the new 8566A and those in the 8568A, there were new opportunities to use the power of microprocessor control to enhance performance. One area in which digital control contributes to the 8566A's performance is in helping the YTX (YIG-tuned mixer) track the YTO (YIG-tuned local oscillator). Through phase-locking techniques, the YTO is always tuned precisely at the start of a sweep but, by necessity, the YTX operates open loop. Delays between the actual frequency scan and the tuning ramp, hysteresis in the tuning magnets, and self-heating of the tuning coils all contribute to mistracking of the YTO and the YTX. Since it is necessary for the YTX to track the YTO within ±10 MHz (3-dB bandwidth) in spite of step changes as wide as 22 GHz, methods of compensating for mistuning of the YTX had to be developed.

Sweep delays are equalized by resistor-capacitor time constants inserted in the faster circuits. Hysteresis effects are compensated for by tuning the YTX well below the start frequency before the start of a sweep so it approaches the start frequency from below and continues upwards during the scan. The decision made by the microprocessor on how far to go below the start frequency and how long to hold it there before starting the sweep is based on the relationship between the previous frequency of the YTX and the new frequency.

Heating Effects

The effects of differential thermal expansion in the YTX tuning magnet, already reduced a factor of 10 by aluminum thermal short circuits (see page 10), are further reduced by firmware routines to a point where they are negligible for most applications. When a frequency change is called for, the microprocessor calculates the final temperature, T_x, that the YTX magnet would arrive at, proportional to the power dissipated in the YTX ($T_x = K_1 \times f_c^2$, where the center frequency f_c, is proportional to the coil current that causes the heating). The microprocessor also stores a variable that is indicative of the magnet's present temperature, T_i. At the end of each sweep, the microprocessor then calculates a new value of T_i such that:

$$T_i \leftarrow T_i + K_2 (T_x - T_i)(t_s + t_p)$$

where K_2 is the self-heating thermal conductivity of the magnet, t_s is the sweep time, and t_p is the nominal end-of-scan processing time.

The microprocessor then uses T_i to calculate a tuning coil current offset, applied through a DAC, to compensate for the short-term self-heating effect. The only restriction in the application of this technique is that the analyzer should be kept sweeping since it is the only way the processor has of keeping track of time.

Another new function performed by the microprocessor is determination of the time required for phase-error transients to die down before a sweep starts. An example will illustrate the need. If the YTO were sweeping a 5-MHz scan, the narrowest open-loop scan, a change in center frequency could cause the frequency to step over a band-switching point, causing the YTO to step from one end of its tuning range to the other. This frequency step could be as large as 3 GHz, yet the sweep start must be within 2% of 5 MHz or 100 kHz when the sweep starts. The microprocessor, by knowing the frequency the YTO is coming from, the frequency to which it is going, and the span width, calculates the time the YTO must be held in the phase-lock state to allow transients to die down to the point where the frequency specification can be met.

Preselector Peaking

In cases where a critical level measurement requires the YTX to be tuned exactly to a signal's frequency, the microprocessor can perform a preselector peaking routine. This routine is called when the display marker is positioned on the signal of interest and the PRESEL PEAK pushbutton is pressed. Using the offset DAC, the microprocessor tunes the YTX to maximize the amplitude response of the displayed signal and then retains the offset. The offset is also stored along with the control settings whenever the SAVE pushbutton is pressed.

Reference

1. M.S. Marzalek and L.W. Wheelwright, "Developing the Digital Control System for the Model 8568A Spectrum Analyzer," Hewlett-Packard Journal, June 1978.

shortened coaxial cavity resonator as the Model 8672A Synthesized Signal Generator.[1,2] To obtain the desired tuning range with a high-Q resonator, the VCO runs at twice the M/N output frequency, or 364 to 396 MHz. The oscillator output is mixed with a 400-MHz reference to derive a difference frequency in a range of 4 to 36 MHz (Fig. 3). The mixer output is amplified and then divided down in frequency by the factor M, which ranges from 8 to 27. This is applied to one input of a phase-frequency detector. The 20-MHz reference is divided by N and applied to the other input of the phase-frequency detector, the output of which controls the VCO. When locked, the VCO frequency must then satisfy the relationship:

$$20/N = (400 - f_{VCO})/M \text{ MHz}$$

or,

$$f_{VCO} = 400 - 20\ M/N \text{ MHz}$$

This is divided by 2 to derive the M/N output frequency:

$$f_{M/N} = 200 - 10\ M/N \text{ MHz}$$

Since the YTO is locked to the Nth harmonic of this frequency such that:

$$f_{YTO} = 200N - 10M - f_{lfs} \text{ MHz},$$

it can be seen that the Nth harmonic moves in 10-MHz steps when M is incremented, and 200-MHz steps when N is incremented. M and N were selected such that N changes after M steps through its range. Stepping M through its

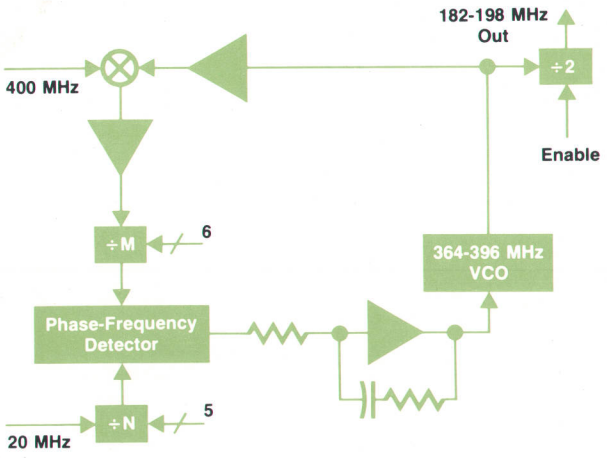

Fig. 3. *Block diagram of M/N loop.*

range causes the Nth harmonic to step across 200 MHz in 10-MHz increments.

Interpolation

The low-frequency synthesizer has three VCO loops that are interconnected in various ways to enable the analyzer to scan frequency spans as narrow as 100 Hz with the same relative accuracy and low phase noise as the broadband sweeps. This is done with a divide-and-upconvert scheme.

The basic source of the low-frequency synthesizer sweep frequencies is loop 1 in Fig. 4. It has a 75-150 MHz VCO whose output frequency is divided by 5 to generate an output in the 15-30 MHz range. This output is used directly by the YTO phase-lock loop for frequency sweeps ranging from 100 kHz to 5 MHz. In this range, the start frequency is settable with 1-kHz resolution.*

For narrower frequency spans, the other two loops come into play. The loop 1 output is then divided down by a factor of 5 or 100, depending on the sweep range. Loop 2 serves to up-convert the divided-down sweep frequency to a range between 160.15 and 166 MHz (see Fig. 4).

The final frequency translation takes place in loop 3. This loop has a VCO operating in a range of 199 to 300 MHz. This VCO output is applied to a mixer whose other input is the output of loop 2. The difference frequency output of the mixer is divided by 2 and the result is divided down to 5 MHz by a factor N_1, using fractional-N techniques,[2] and

*These numbers for span width and start frequency settability apply when the input frequency is below 5.8 GHz where LO fundamental mixing is employed. For higher input frequencies where harmonic mixing is used, the numbers are multiplied by the harmonic number. For example, at 20 GHz (4th harmonic mixing), the span width can be as wide as 20 MHz with the YTO locked to the low-frequency synthesizer, and the start frequency is settable with 4-kHz resolution.

Switch Position	Output Range	Synthesis Resolution	Scan Width
1	15-30 MHz	1 kHz	0.1-5 MHz
2	19.9-30	20 Hz	5-100 kHz
3	19.995-30	1 Hz	0.1-5 kHz

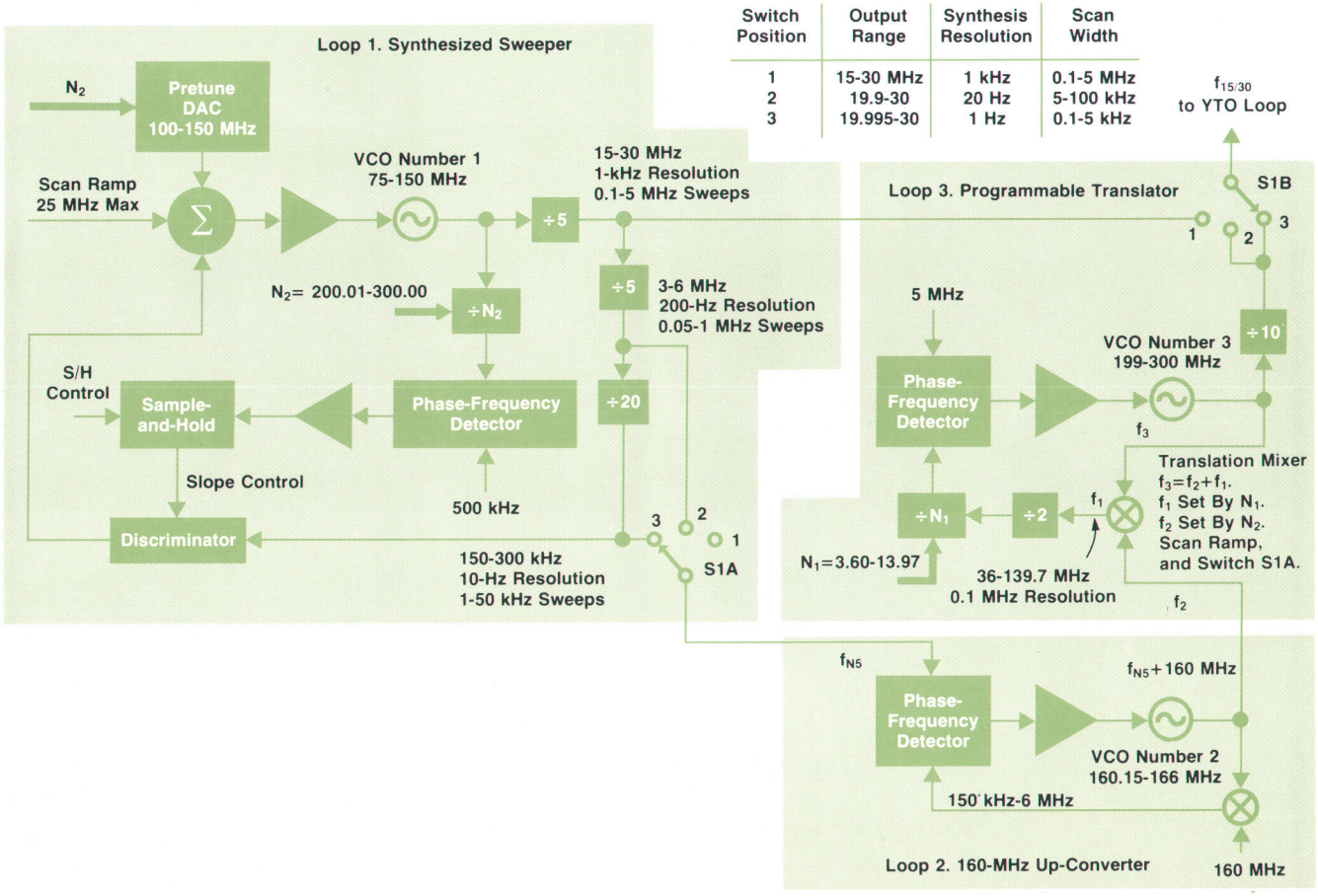

Fig. 4. *The low-frequency synthesizer has three loops. Loop 1 is the basic source of a frequency that is divided down then up-converted by loop 2 and translated by loop 3 to derive an appropriate frequency for control of the YTO.*

A Precision Discriminator with a Controllable Slope

by Stephen T. Sparks

The VCO that generates precision sweeps in the low-frequency synthesizer of the Model 8566A Spectrum Analyzer is controlled through a feedback loop that includes a discriminator (see Fig.4, page 16). A key characteristic of this discriminator is that the slope of its voltage/frequency response curve is adjusted by a phase-lock loop, thus enabling highly accurate narrowband sweeps.

A block diagram of the sweep-frequency control system is shown in Fig. 1. The discriminator is the pulse-count type in which the input signal triggers a pulse generator, which generates a single pulse of constant width and height for each cycle of the input. These pulses are integrated to obtain a dc current that is proportional to the input frequency.

The transfer characteristic of the discriminator is characterized by the equation:

$$I_2 = Kf + B$$

where K is the slope of the response curve, f is the input frequency, and B is an offset (see Fig. 1). A frequency change Δf results in an output change ΔI that is a function of K only. In the usual discriminator, the term K is subject to warm-up and long-term drift that exceeds the 0.1% accuracy desired for the 8566A. Therefore, some precise means of modifying K is needed to maintain accuracy.

Given that two points determine the slope of a line, fixing two points will fix K. In the discriminator described here, care was taken to reduce the offset B to negligible proportions. Thus, the origin is one of the fixed points on the response curve.

The second point is fixed during the pre-sweep interval while phase lock is being established. During this interval, the scan input where the sweep ramp is applied is zero (I_3 in Fig. 1). A precise pre-tune current (I_4) corresponding to the start frequency is fed into the VCO control loop. The N_2 phase-lock loop (Fig. 4, page 16), also programmed to the start frequency, then functions to adjust current source I_1 until lock is achieved. The discriminator response curve is thereby rotated to the point where the pre-tune current drives the loop to the desired start frequency. This, in effect, sets the second point, fixing K. The discriminator response is thus tied to the analyzer's frequency standard by way of the 500-kHz reference.

When the scan starts, the voltage that sets I_1 is stored in a sample-and-hold, opening this leg of the phase-lock loop. The discriminator is in the feedback loop that controls the VCO and it causes the VCO frequency to closely follow the tuning ramp, eliminating the effects of any tuning nonlinearities or temperature coefficient that may be in the VCO.

Precision Pulses

If the discriminator is to be truly linear, the width and height of the

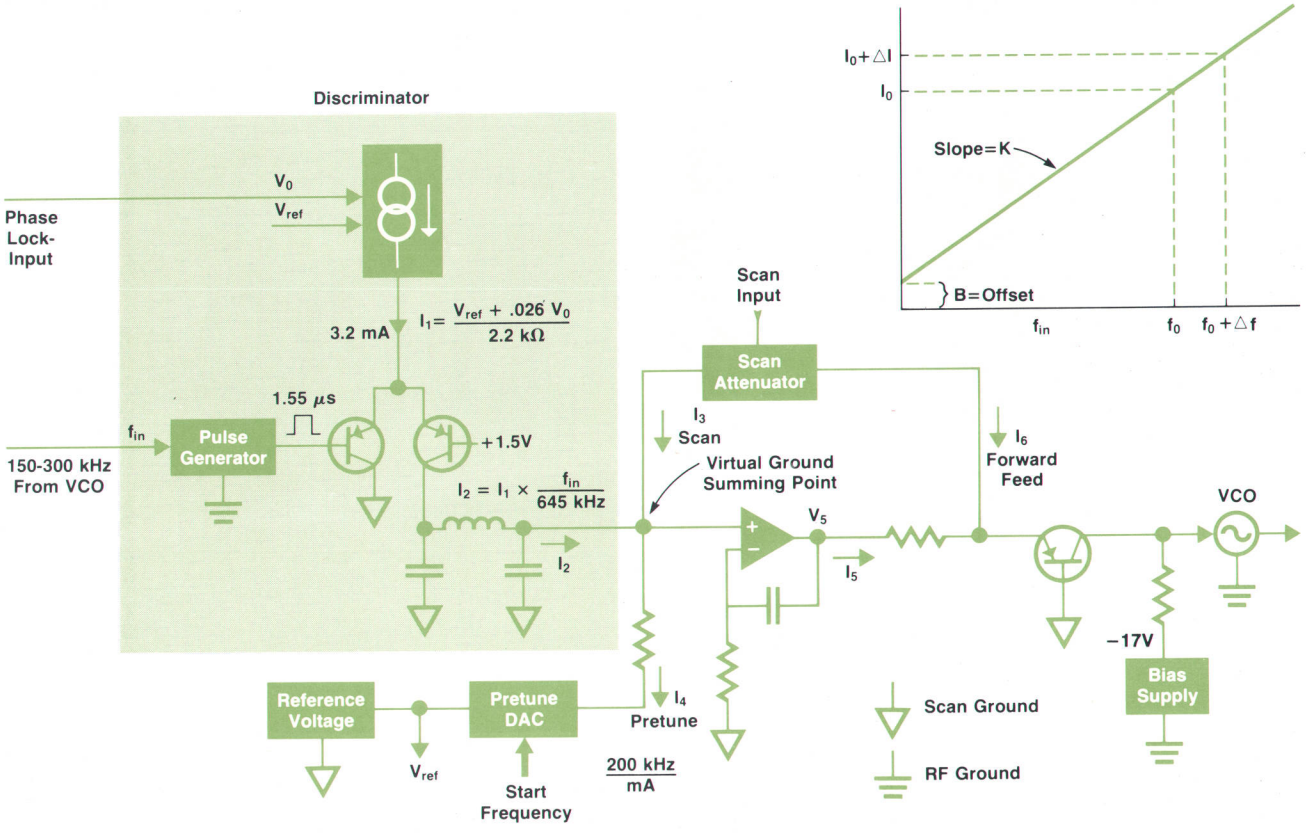

Fig. 1. *VCO control systems uses a pulse-count discriminator that has controllable response.*

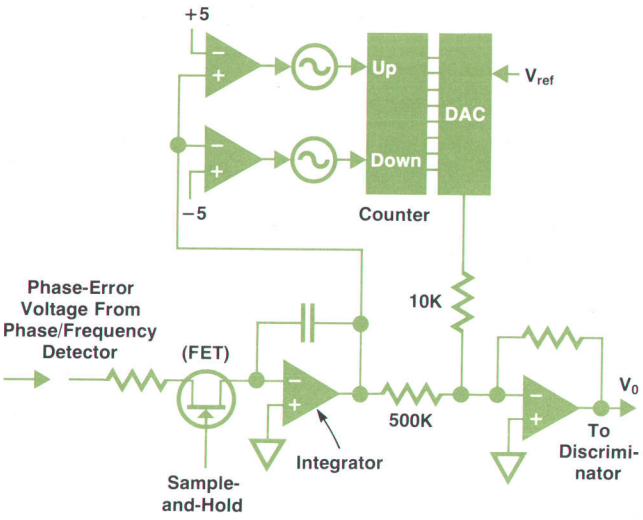

Fig. 2. *Digital sample-and-hold.*

discriminator output pulses must be uniform at all input frequencies. Uniform pulses are obtained in this discriminator by using the input pulses to drive a common-emitter transistor that has a resonant LC circuit in its collector circuit. Each pulse saturates the transistor, causing the LC circuit to ring at 5.2 MHz. The ringing waveform is applied to a ÷16 counter. Prior to each input pulse, the counter is preset to 6. Its MSB output then goes high on the second zero crossing of the ringing waveform (count = 8) and goes low again eight cycles later (count = 16). The width of the pulse generated by the MSB output is thus determined precisely by the frequency of the ringing circuit. These pulses are integrated to obtain I_2 (Fig. 1).

An important feature of this arrangement is that presetting the counter and using the MSB output causes it to ignore the first cycle of the ringing waveform. The first cycle is of low amplitude and of variable period because of the finite saturation time of the driving transistor. Also, at high input frequencies the LC circuit may not have settled down from the previous pulse, causing further variations in the first cycle. Skipping the first cycle results in a significant improvement in discriminator linearity.

The discriminator response deviates from a straight line less than ±0.002% for an integrated pulse current (I_2 in Fig. 1) ranging from 0 to 2/3 of I_2 max, and the incremental linearity, which determines the accuracy of narrow scans, is within ±0.03%. The discriminator actually operates between 1/3 and 1/2 of I_2 max, corresponding to an input range of 200 to 300 kHz.

Fast Lag and Slow Droop

Current I_6 in Fig. 1 is a portion of the sweep ramp that is applied directly to the VCO, reducing the excursions of voltage V_5. This reduces sweep lag, the amount by which the VCO frequency lags the scan ramp. The lag, which is proportional to scan rate, occurs because of the finite bandwidth of the discriminator, which was made low to reduce noise contributed by the discriminator. The I_6 feedforward current reduces sweep lag by a factor of 10, so the maximum sweep lag is only 0.15% of scan width.

Very slow sweeps, on the other hand, are a potential source of another problem: droop in the sample-and-hold circuit. Since scans can take as long as 1500 seconds each, leakage in the sample-and-hold capacitor would have to be less than 50 pA to maintain scan accuracy.

The sample-and-hold voltage is held in an integrator, shown in Fig. 2. To reduce the effects of sample-and-hold drift, the oscillator system was designed so the integrator has only a limited influence on the frequency; it can adjust the frequency by only ±0.04%. This range, however, is insufficient to correct for long-term drift in the discriminator. Thus, a digital-to-analog converter (DAC) and related circuitry was added to the integrator, as shown in Fig. 2. If the output of the integrator attempts to exceed ±5V during the phase-lock interval, one of the two oscillators shown in Fig. 2 is turned on, either clocking the counter up or down. The counter drives the DAC whose output is summed with the analog integrator output, thus contributing to the output V_0. Counting continues until the total output steps past the value required to achieve phase lock. The phase error voltage then causes the analog circuit to retreat, cancelling the overshoot. This shuts off the oscillator, and leaves the analog circuit in the middle of its range. The contribution of droop in the analog circuit after the sample-and-hold switch opens is thus reduced to negligible proportions because the major portion of V_0 is held in the DAC.

compared to a 5-MHz reference. The following equation thus applies:

$$(f_{VCO3} - f_{loop2})/2N_1 = 5 \text{ MHz}$$

or,

$$f_{VCO3} = 10N_1 + f_{loop2}.$$

The VCO3 frequency is thus offset from the loop 2 frequency by $N_1 \times 10$ MHz, where N_1 ranges from 3.60 to 13.97.

The VCO3 frequency is divided by 10 to place it in the 19.9-to-30-MHz range and then supplied to the YTO loop. The output of loop 1 is thus divided down by factors of 50 or 1000 and then offset in frequency to place it in the proper range for the YTO.

What this scheme accomplishes is the reduction of the phase noise, residual FM, and synthesis-related spurious outputs of loop 1 by as much as 60 dB (20 log 1000) for frequency spans of less than 5 kHz, thus enabling the analyzer to meet the more stringent requirements of narrow-band scans. In addition, for spans less than 25 kHz, the gain of the YTO loop is increased about 10 dB. Although this degrades the far-out phase noise somewhat, it improves the close-in phase noise and line-related spurious performance. Of course, loops 2 and 3 make their own phase-noise and spurious contributions but these have been held to a minimum through careful circuit design and shielding.

As a result of these measures, residual FM, start frequency offsets, and drift during a scan are always less than 0.1% of scan width (one "bucket" of the 1000-point digitally-stored display is 0.1% of the scan width). Note that there is no overlap of the tuning ranges of any of the VCOs in the instrument. Overlapping VCO frequencies are a prime source of troublesome "crossing spurs" in a synthesizer, so this system eases the difficulty of meeting the desired spurious specifications. Spurious outputs are at least 90 dB below the carrier while broadband phase noise is at least 10 dB below that of the YTO loop.

For frequency spans greater than 5 MHz, where the sweep ramp is applied directly to the YTO, the synthesizer sweeping function is disabled and it then provides start frequencies with 1-Hz resolution.

Discriminator-Stabilized VCO

Loop 1 uses a stabilization system that includes a fre-

quency discriminator in the phase-lock loop, as shown in Fig. 4. During a sweep, the loop 1 VCO is controlled by the discriminator output and is therefore sensitive to the discriminator's frequency-to-current response. During the pre-sweep interval, the phase-lock error voltage tunes the VCO by adjusting the slope of the discriminator's response while a known input current is applied to the discriminator, as explained on page 17. Then, when the VCO output divided down to 500 kHz becomes phase-locked to a 500-kHz reference, the discriminator slope is precisely known.

When a sweep is initiated, the error voltage from the phase detector is stored in a sample-and-hold circuit, effectively opening this feedback loop. A voltage ramp for sweeping the VCO is applied to a summing network along with the discriminator output (and the dc pretune voltage). The discriminator output thus functions as a negative feedback signal to cause the VCO frequency to closely track the ramp, thus correcting for any nonlinearities in the VCO tuning curve. Since the discriminator frequency-to-current response has been set accurately by the phase-lock loop, outstanding sweep accuracy results.

Controlling Residual Responses

Because the M/N output remains enabled during these sweeps (it is disabled during sweeps greater than 5 MHz), there is a possibility that residual responses could be generated by M/N harmonics that mix with the YTO in the input mixer to produce sum or difference frequencies near the first IF. An analysis of this situation determined that such mixing products could occur. Therefore, the YTO output is coupled to the phase-lock loop through a microcircuit directional coupler that has a 2-to-6-GHz GaAs FET amplifier in the coupled arm (see Fig. 2). Pads in the amplifier input and output attenuate the YTO signal such that the net gain through the pads and amplifier is 0 dB. The reverse isolation, however, is increased by the pads which, with the reverse isolation of the amplifier, gives a total reverse isolation more than 40 dB greater than the reverse isolation of the coupler itself. Residuals due to the M/N loop have thus been reduced to the point that most lie below the noise floor of the analyzer, even with the 10-Hz resolution bandwidth.

Acknowledgments

Rick Chan designed the scan generator and YIG driver circuits. We would also like to thank Jim Thomason, Ken Astrof, and the other members of the 8672A Synthesized Signal Generator design team on whose work much of the 8566A local oscillator design was based.

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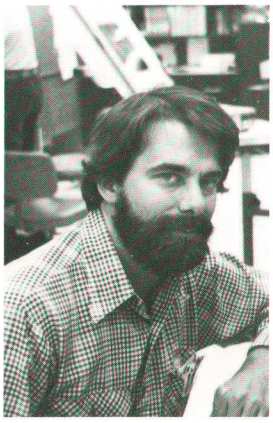

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Steve Sparks received his BSEE degree in 1968 and MSEE degree in 1969 from the University of California at Berkeley. AT HP, he contributed to the circuit design of the 8601A and 8605A Sweepers, the 8407A and 8754A Network Analyzers, and the 8672A Signal Generator (he joined HP shortly after graduation from high school). Steve keeps busy with a variety of activities: backpacking, jeep trips, photography, restoring antique radios, brewing beer at home, cooking, winetasting, and flying small planes. He also grazes cattle and plans to develop a vineyard on his 50-acre ranch.

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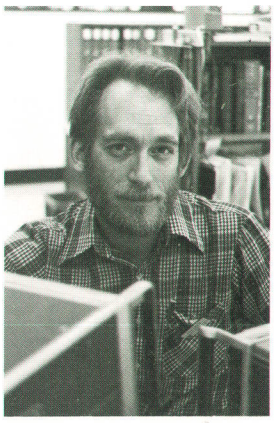
Larry Martin received his BSEE degree in 1967 from Kansas State University. An HP employee since that same year, Larry was a project manager for the 8672A Synthesized Signal Generator, contributed to the design of the 8555A spectrum analyzer tuning section, and earned an MSEE from Stanford University along the way. Larry lives in Santa Rosa, California, is single, and keeps busy with photography, wine tasting, softball, tennis, and basketball. He also enjoys flying a sailplane occasionally.



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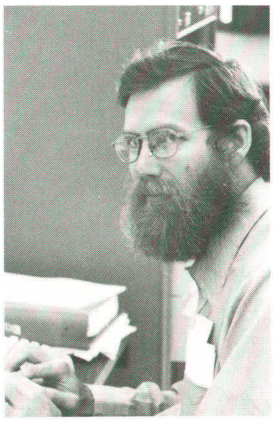

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Mike Marzalek received his BSEE degree in 1969 from the University of California at Berkeley and his MSEE degree in 1972 from Stanford University. With HP since 1969, Mike designed the microprocessor software for the 8566A, designed hardware for the 8568A Spectrum Analyzer, and contributed to several synthesized signal generators. Born in Springfield, Missouri, and raised in southern California, Mike is married and spends many of his leisure hours crosscountry skiing, down-hill skiing, playing folk guitar, and working in stained glass.

A Digital Pattern Generator for Functional Testing of Bus-Oriented Digital Systems

Simple interfacing enables this flexible pattern generator to drive digital buses or other multichannel logic systems for functional testing with long digital sequences

by Günter Riebesell, Ulrich Hübner, and Bernd Moravek

AS MICROPROCESSORS and other sequential state machines continue to penetrate more and more applications areas, component manufacturers add a greater variety of LSI devices to their range of products that support digital processor systems. Thus, data buses, for carrying data traffic between devices within a digital system as well as handling data traffic between the system and its peripherals, are being found in a growing number of system designs.

This is raising special problems in hardware testing during the design and development of a digital system. With data traffic in modern digital systems routed over a shared bus, the controller and all logic subassemblies must be tested for bus compatibility under real-time conditions at every stage of the design. Until recently, thorough checkout of the subassemblies was not possible until the controller software was developed. On the other hand, the controller software could not be finalized until the system subassemblies were completed. Thus, design verification during the early stages of system development has generally been a trial-and-error procedure that inevitably led to critical design changes when debugging the system during the later development phases. These design changes occurred at a time when wrong decisions would lead to severe cost penalties and loss of time.

Lab-built toggle switch boxes have been used for setting lines high or low for functional testing of subassemblies in which specific input patterns are supposed to result in specific output patterns according to the truth table of the device under test. Unfortunately, switch boxes are capable of static testing only, and investigations of complex devices over several clock cycles are awkward and time-consuming. As an alternative, many users build pattern generators. These, however, generally have limited sets of patterns, are usually restricted to a narrow range of bit rates and output levels, and are unable to interact with the devices under test.

Fig. 1. *Model 8170A Logic Pattern Generator produces long sequences of 8-or 16-bit parallel digital words as bus stimuli for functional tests of multichannel digital hardware. It operates at clock rates up to 2 MHz, internally or externally supplied.*

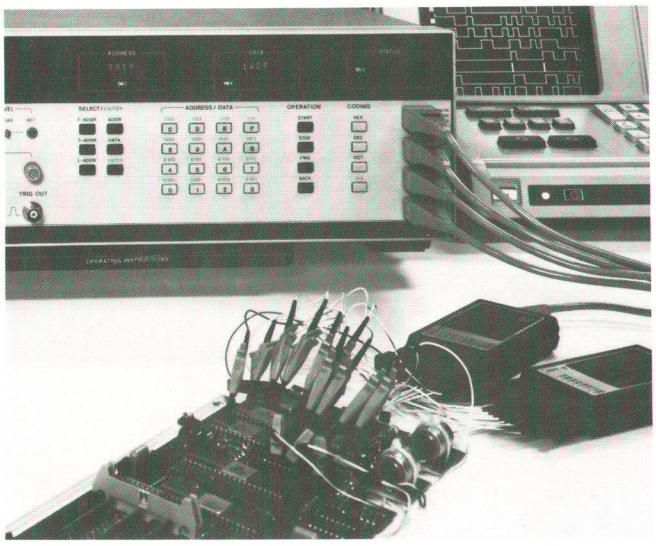


Fig. 2. *Miniature probes like those used with logic state analyzers facilitate hook-up to the system being tested.*

A Multichannel Source

To resolve the testing problem, a new programmable data generator has been designed for functional checkout of multichannel digital hardware. The new generator, Model 8170A (Fig 1), produces sequences of 8-bit parallel words up to 1024 words long for functional testing. Alternatively, it can produce 16-bit parallel words with a maximum sequence length of 512 words. An option expands these sequence lengths by a factor of four. Functional checkout with this generator simulating all operational conditions is a powerful fault-finding technique which, if applied early in the design stage, allows the hardware, firmware and software to be developed independently.

The new instrument can generate the sequence data in synchronism with an external clock or with its own clock at rates up to 2 MHz, enabling most systems to be tested functionally at full operating speed. The instrument also outputs a clock signal and a data-valid (DAV) signal equivalent to a clock signal, for the use of the device under test.

Output levels are pushbutton selectable to be compatible either with TTL circuits (0V low, 5V high) or CMOS circuits (0V low, 3-15V high, adjustable). Both output modes also have a 5-kΩ idle or off state. Miniature probes connected to pods, like the probing systems used with HP logic state analyzers,[1] facilitate hook-up to the device under test (Fig. 2).

Internal Organization

The heart of the Model 8170A Logic Pattern Generator is a battery-supported, nonvolatile, read-write random access memory (RAM). Data, memory addresses, and operating modes are entered into the memory through the front-panel keyboard, by way of the HP-IB,* or through an RS 232C/CCITT V.24 input. Depending on user practice, data can be entered in the binary, octal, or hexadecimal number systems and addresses can be entered in decimal, octal, or hexadecimal. The instrument converts the inputs to binary for entry into the memory, eliminating the need for the user to perform numerical base conversions. When address/data check or recall is wanted, alphanumeric LEDs display the selected memory address and its contents individually using the selected code (see Fig. 1).

Typical bus traffic is simulated by the 8170A as it reads out the data in its memory in an ascending address sequence at a rate determined by the selected clock. This mode of operation, shown in the simplified block diagram of Fig. 3, is known as the internal address mode. On receipt of a START command the 8170A outputs the stored data continously (AUTO cycle) or just once (SINGLE cycle) between the first and last addresses selected by the user.

The ascending address sequence is generated by a counter that accesses the data stored in the RAM. Because the RAM actually consists of several RAM ICs that may have slightly different access times, the data bits are held briefly in latches and then strobed to the outputs simultaneously to avoid skew problems.

An output stage is shown in Fig. 4. It is basically a TTL-to-MOS driver with a switch (Q1) that shuts off the CMOS supply voltage when the outputs are to be placed in the idle (high-impedance) state. The instrument's outputs automatically revert to the idle state after data at the last address has been produced in the SINGLE cycle mode. This state allows the probes to remain hooked to a data bus without loading the bus. It also allows the data in the instrument's memory to be changed without affecting the device under test while the change is being made. The outputs also revert to the idle state when the instrument is turned on, and whenever the STOP command is given.

When supplying data to an interface bus, the 8170A can operate asynchronously in a handshake mode, enabling real-time simulation of system/peripheral interaction. As shown in the timing diagram of Fig. 5, it can work with either a 2-wire or 3-wire protocol. The DAV (data valid) signal generated by the 8170A is output through one of the

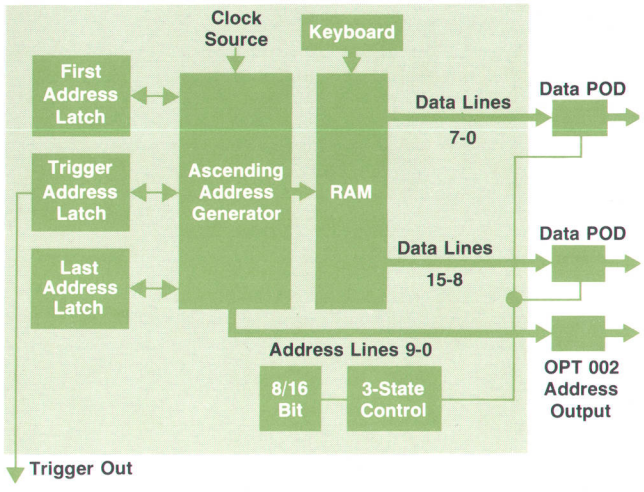


Fig. 3. *Block diagram of the 8170A operating in the internal address mode. In this mode, the memory contents are supplied to the outputs in ascending order beginning at the first address specified and ending at the last address. A trigger output pulse is generated whenever the address being accessed in memory matches the address in the trigger address latch.*

*HP-IB: the Hewlett-Packard interface bus, HP's implementation of ANSI/IEEE 488-1978.

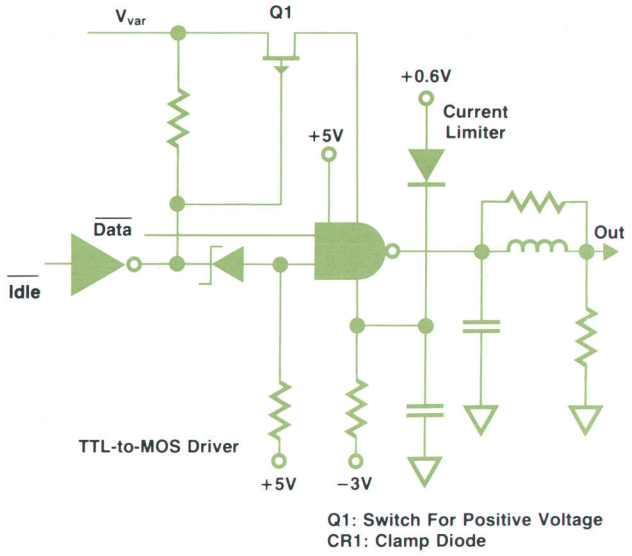


Fig. 4. *Output drive level is determined by the voltage V_{var} supplied to the MOS bias input of U1, a TTL-to-MOS driver. Q1 turns off V_{var} to place the output in the idle (high-impedance) mode.*

probe pods, and the RFD (ready for data) and DAC (data accepted) signals generated by the system under test are brought in through probes on the same pod.

Breakpoints

For detailed investigation of device operation with a logic analyzer or oscilloscope, the 8170A generates a trigger output pulse when a particular address in the memory is reached. Any address between the first and last addresses can be selected as the trigger address.

The trigger output is particularly helpful in determining when and why a system "crashes." Knowing approximately where in the program the fault occurs, the user can enter an address from this part of the program into the trigger register and then feed the TRIG OUT signal to the 8170A's BREAK IN input. During execution of the program, the trigger pulse will halt the program at the trigger address with the data outputs remaining in the active state. The precise address at which the fault occurs may then be found by single-stepping the stored program in ascending or descending order by using the FWD or BACK keys.

The BREAK IN capability may also be used to stop the program in response to a signal or qualifier from the device under test. This signal could be one that indicates a possible malfunction or forbidden condition. Any pulse greater than +2V in height and 40 ns in width will stop data generation at the current address. Data generation may be resumed from the most recent address by pressing the START button or by applying a pulse (>+2V, 40ns) to the START IN connector.

ROM Simulation

When operating in its external address mode, the 8170A Logic Pattern Generator can function as an erasable, programmable, read-only memory (EPROM), outputting data in response to externally supplied addresses and enable signals (Fig. 6). Unlike EPROMs, however, the logic pattern generator allows program steps to be changed quickly via the front-panel keyboard. This can be a great help during the finalization of software for a system under development. All ROM-related functions can be quickly checked out and the ROM design corrected and verified before the actual ROM goes to manufacture.

When the 8170A is being used as a ROM simulator, a separate probe pod with active address line receivers enables the system under test to select the addresses of data stored in the generator's memory. Access time is typically 520 ns.

Also provided are four ENABLE lines that function as qualifiers in the external address mode. For example, these may be used as four additional address lines when testing digital machines that have 16-bit addresses, thereby providing a means of selecting the portion of the total 64K address space in which the 8170A addresses will lie. If more memory space is required, two or more 8170As may be used in parallel with the ENABLE inputs functioning essentially as instrument-select lines.

Friendly Syntax

The syntax for operating the instrument from the keyboard makes operation straightforward. Some examples of user convenience are short-form entry of addresses and data (omitting leading zeros), multiple consecutive data entry (holding down the ENTER key causes the same data to be loaded into successive memory locations), automatic incrementing of the address register when a data entry is made, and the single-step FWD and BACK keys.

Syntax similar to the keyboard is used for programming

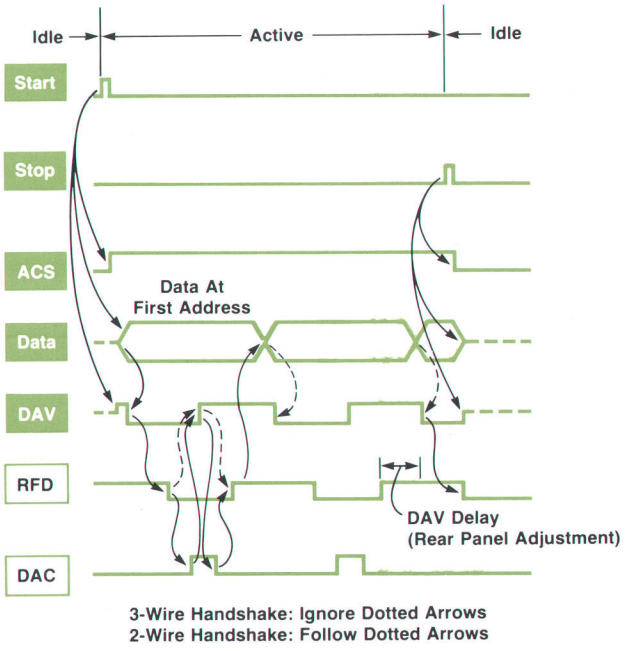


Fig. 5. *Handshake protocol for operating the 8170A in the asynchronous (non-clocked) mode. It works with either 2-wire or 3-wire protocols, as selected by front-panel pushbuttons. The delay (DAV) is adjustable over a range of 300 to 800 ns. (ACS high means the outputs are in the active rather than the idle state).*

the 8170A via the HP interface bus. Two HP-IB modes, accessed through separate HP-IB addresses, are provided. When the keyboard mode has been addressed, all functions controlled by the front-panel pushbuttons are programmable using mnemonics related to the pushbutton functions. When the data mode is addressed, data supplied over the HP-IB is loaded into successive memory locations between START and STOP addresses defined while the instrument was in the keyboard mode. The data mode also enables the 8170A to report its memory contents to the test system controller.

Simplified Data Entry

Until now, parallel data generators used individual LEDs to display the status of each channel at a particular address. This meant that the operator had to scrutinize the 16 LEDs of a 16-channel instrument to check the memory status at each memory address. The 8170A makes things much easier by allowing data to be entered and displayed in a variety of number bases (octal, decimal, or hexadecimal for addresses, and binary, octal, or hexadecimal for data). For example, to load the pattern 01101011 into address 10 using hexadecimal the user executes the following keystrokes:

ADDR 1 0 DATA 6 B ENTER

Since data is always stored in binary, changing the number base affects only the display (and numerical entry) and does not affect the stored data or the data output

When a key in the ADDRESS/DATA group is pressed, the binary equivalent of that key is stored in one of the 4-bit display registers and the content of the register is displayed in the selected format in the corresponding position on the display. When the ENTER key is pressed, all the information in the data display registers is converted to a single binary number and stored in memory at the indicated address.

Data transfer into and out of memory is always carried out in 8-bit bytes. To display the contents of a memory address in hexadecimal, each 8-bit byte is separated into two 4-bit segments and then each 4-bit segment is converted to the equivalent hexadecimal digit for display. To convert to octal, the two 8-bit bytes, taken together, are separated into groups of three bits, as shown in Fig. 7, and by addition of a leading zero, each group of three bits is expanded to a 4-bit segment for storage in a display register. The same hexadecimal conversion is then performed on each 4-bit segment but in this case the highest digit will be 7 because of the leading zero.

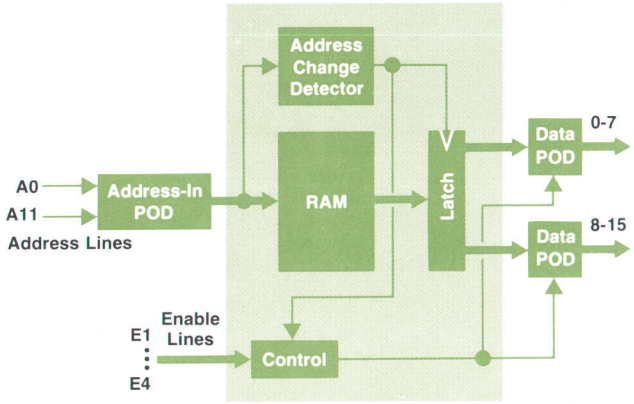


Fig. 6. *Block diagram of the Model 8170A Logic Pattern Generator operating in the external address mode. Data is output whenever the address-change detector, consisting of exclusive-NOR gates, detects that there has been a change of address. Alternatively, one of the enable inputs may be used as a clock input for timing the data output. A data-valid signal is also generated.*

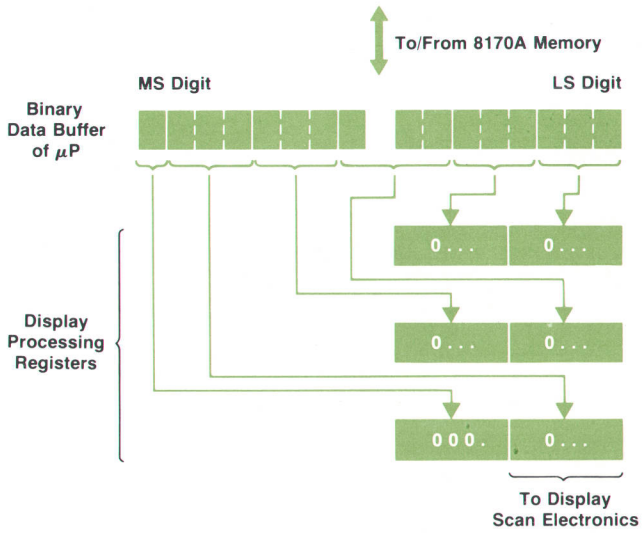


Fig. 7. *Conversion of a 16-bit binary number stored in memory to an octal number for display involves separation of the binary number into 3-bit groups and addition of a leading zero to each group. The resulting 4-bit number may then be stored in a display register.*

Binary-to-decimal conversion is more complex since, unlike octal and hexadecimal, decimal numbers are not related to integral powers of 2. In this case, to match the capabilities of the 6800 microprocessor, the "add-3" algorithm[2] is used to convert a binary number to decimal for display. For the decimal-to-binary conversion when data is entered, the Horner scheme is used.

Preselected Patterns

To facilitate the entry of certain often-used data patterns, entry of the following patterns has been reduced to a few keystrokes:

Pattern	Application	Key
All 0s	Clear memory	0
All 1s	Set memory	1
Ascending count	Simulate counter, check DAC linearity, etc.	C
Descending count		D
Pseudorandom data	Noise simulation	E

To select one of these, the operator holds down the DATA key while pressing the selected pattern key (0, 1, C, D, E) for two seconds. The display then reads "Mem chg?" (memory change?), which the user confirms by pressing key 1 (for "yes"). The selected pattern is then loaded into the memory. If key 0 were pressed, the memory would remain unchanged and the display would revert to display of address and data. This routine prevents accidental loss of memory contents by unintentional loading of the memory with one of these patterns.

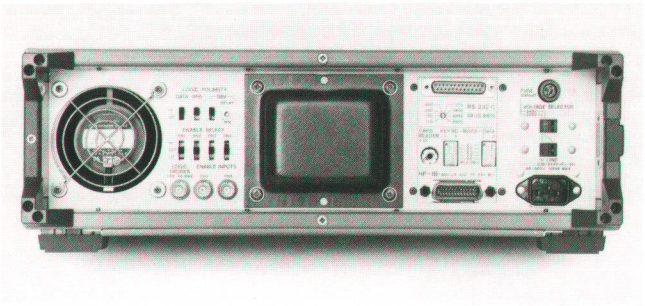


Fig. 8. *The ENABLE SELECT switches and two of the four ENABLE inputs are on the rear panel. Also on the rear panel are the LOGIC POLARITY switches, DAV DELAY adjustment, RS 232C BAUD RATE select, and HP-IB addresses (KEYBOARD and DATA MODES).*

The PRBS (pseudorandom binary sequence) pattern is generated by firmware. By means of the microprocessor's rotate instruction, one of the microprocessor's accumulators functions as the shift register of a hardware equivalent. A counter detects 16 shift operations and then initiates an operation that loads the current pattern into memory. Since the firmware program always begins by loading 0001_{16} into the accumulator, the PRBS pattern is always the same.

Designed-in Serviceability

As with other complex, microprocessor-based devices, traditional troubleshooting techniques would be inadequate for the 8170A so serviceability had to be designed in. Serviceability is optimized by inclusion of test routines in the firmware and by making the necessary provision for signature analysis,[3] such as including switches for opening feedback loops and disabling certain circuits, and including the necessary stimulus programs in the controller ROM.

When turned on, the 8170A automatically runs through a self-check routine that includes illumination of all LED indicators to give the operator confidence that the basic system is functioning.

Two methods of generating the stimulus for signature analysis are implemented. In one, free run, the data bus is opened at the microprocessor and the CLRB instruction is applied. This causes the microprocessor to step through its entire address field. The most significant address line is used as both a START and STOP signal for the signature analyzer, defining the entire address field as a measurement window. Thus, the functioning of the processor, address-bus and data-bus ROMs, and decoding circuitry are verified in one measurement.

In the second method, implemented when the free-run method has been completed, ROM-resident routines for signature analysis of various subunits are accessed through the keyboard. Several of these routines are associated directly with particular circuit boards, making it easier to locate the circuit at fault.

Acknowledgments

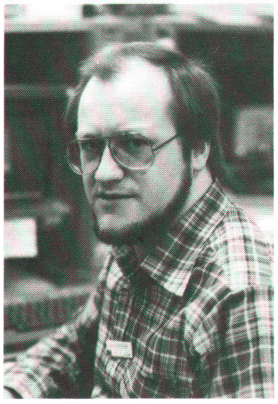
Arndt Pannach initiated the 8170A project while Jörn Kos was responsible for overall guidance. Dietmar Seiffert optimized the HP-IB programmability. Mechanical design was by Horst Link.

References

1. W.A. Farnbach, "The Logic State Analyzer—Displaying Complex Digital Processes in Understandable Form," Hewlett-Packard Journal, January 1974.
2. "Analog-to-Digital Conversion Techniques with the 6800 Microprocessor System," Motorola Application Note 757.
3. R.A. Frohwerk, "Signature Analysis: A New Digital Field Service Method," Hewlett-Packard Journal, May 1977.

Ulrich Hübner

Born and raised in Stuttgart, Germany, Ulrich Hübner studied at the technical universities in Aachen and Stuttgart. He joined HP GmbH's medical division in 1967, then moved to the instrument group, where he developed low-cost oscilloscopes. Since 1975 Ulrich has been involved in data generator design and was responsible for the 8170A hardware design. Ulrich is married, has one child, and enjoys swimming and skiing in his spare time.



Bernd Moravek

A native of the Rheinland area (Germany), Bernd Moravek earned his Diplom Ingenieur degree at the Technische Hochschule Aachen in 1977. He joined HP the same year, plunging directly into the 8170A project. The serial interface and the implementation of signature analysis are his contributions. Bernd is married and spends much of his spare time playing organ at home and in cathedrals.

Günter Riebesell

A native of Hamburg and a graduate (Diplom Ingenieur) of the Technische Universität Braunschweig, Günter Riebesell joined HP in 1973, working initially on the 8016A and 8084A Data Generators. He then became project leader for the 8170A and was responsible for development of the instrument's software. Günter is married, has a two-year-old son, and enjoys filming and skiing in his leisure time.

SPECIFICATIONS

HP Model 8170A Logic Pattern Generator

MEMORY

CAPACITY: 8192 bits.

DATA BUS FORMAT: 8 bits × 1024 words or 16 bits × 512 words.

POWER-OFF STORAGE: Internal battery provides memory retention for approximately 3 weeks at room temperature. Battery recharges when 8170A is switched on.

OPERATING STATES

IDLE: Permits entry of address, data and operating parameters. Data and DAV output in 3-state.

ACTIVE: Continuous data output.

BREAK: Static data output. FWD/BACK enables data change by stepping address.

ADDRESS MODES

INTERNAL: Data generation in ascending address sequence from first to last address. Rate governed by clock (see 'Clocking').

EXTERNAL: Data output follows external address and enable signals. DAV generated at each new address. Data and DAV in 3-state when instrument not enabled. Clock and cycle modes disabled.

MAXIMUM ADDRESS RATE: 2 MHz.

ADDRESS TO OUTPUT DELAY: 400 ns typical, 550 ns maximum.

ENABLE TO OUTPUT DELAY: 100 ns typical, 130 ns maximum. DAV at minimum delay.

CLOCKING

INTERNAL: 20 Hz to 2 MHz in 5 decade ranges, adjustable by vernier.

RATE JITTER: <0.2%.

EXTERNAL: dc to 2 MHz. For input specs, see 'Auxiliary inputs'.

MANUAL: Operated by FWD and BACK keys.

HANDSHAKE: 2-wire/3-wire handshake capability selectable. External handshake signals determine timing of data readout. If MAN and Handshake selected, FWD/BACK provides trigger for next handshake cycle.

CYCLE MODES

AUTO CYCLE: Data is continuously generated between first address (F-ADDR) and last address (L-ADDR).

SINGLE CYCLE: Data is generated once between F- and L-ADDR. After cycle completion, 8170A returns to IDLE state.

Output Signals

DATA: Pods provide 16 output lines D0 to D7 (Model 15455A), and D8 to D15 (Model 15456A), Pos/neg true selectable on rear panel.

CONTROL: Data valid (DAV) generated with each word. Pos/neg true selectable on rear panel. DAV line via Control Pod Model 15454A.

DAV DELAY (adjustable on rear panel):

NON-HANDSHAKE: 100 ns to 700 ns.

2- OR 3-WIRE HANDSHAKE: 300 ns to 800 ns.

DAV WIDTH (at +1.3 V): See following table:

Clock Mode	DAV Width
Internal Clock	Clock period/2 ±50 ns
Manual Clock	10 μs (typical)
External Clock	
Width 40 ns - 200 ns	250 ns (typical)
Width >200 ns	External width ±50 ns

STATUS: Idle, Active and Break states indicated on lines ACS (Active state) and BRS (Break state)—fed via Control Pod Model 15454A:

Status	ACS	BRS
Idle	LO	HI
Active	HI	HI
Break	LO	LO

POD OUTPUT CHARACTERISTICS

TTL SETTING

FAN OUT: 5 standard TTL maximum.

LEVELS: high +4.5 V to +5 V; low −0.5 V to +0.4 V. Idle (3-state) 5 kΩ typical.

SIGNAL CHARACTERISTICS (1 standard TTL load):

TRANSITION TIMES (+0.4 V TO +2.4 V): 25 ns typical, 50 ns maximum.

DISTORTED HIGH LEVEL: ≥+3.5 V (i.e. preshoot, overshoot, ringing lie above this level).

DISTORTED LOW LEVEL: ≥+0.8 V (i.e. preshoot, overshoot, ringing lie below this level).

VARIABLE SETTING (CMOS)

MAXIMUM LOAD: 50 pF (high impedance).

LEVELS: high +3 V to +15 V adjustable, low −0.5 V to +0.4 V. Idle (3-state) 5 kΩ typical.

HIGH LEVEL TO MEASUREMENT PIN VOLTAGE TRACKING: ±0.2 V typical, ±0.5 V maximum.

SIGNAL CHARACTERISTICS (50 pF, +15 V):

TRANSITION TIMES (20% to 80%): 35 ns typical, 60 ns maximum.

DISTORTED HIGH LEVEL: ≥+12.0 V.

DISTORTED LOW LEVEL: ≤+2.5 V.

OUTPUT PROTECTION: All outputs protected against short circuit and external voltages from −1.0 V to +18 V.

AUXILIARY OUTPUTS

TRIGGER: Generated at trigger address (T-ADDR).

FORMAT: NRZ.

LEVEL: standard TTL.

FAN OUT: 5 standard TTL maximum.

PROBE: +5 V dc, 400 mA maximum.

POD INPUT SIGNALS

ADDRESS: 12 lines (positive true), A0 to A9 via Address Pod Model 15453A; A10, A11 (for Option 001 Extended Memory) via Control Pod Model 15454A. Additional enable lines (EN1, EN2 via Control Pod; EN3, EN4 via rear panel) allow a number of 8170A's to be addressed from a 16-bit bus; selectable levels pos/neg/don't care.

CONTROL (Model 15454A): Ready for DATA (RFD) and Data Accepted (DAC). In 2-wire handshake, RFD level pos/neg selectable. In 3-wire handshake, RFD and DAC conform to ANSI/IEEE 488-1978.

POD INPUT CHARACTERISTICS

INPUT IMPEDANCE: >10 kΩ|| ≤25 pF.

LEVELS: high ≥+2.0 V; low ≤+0.8 V.

MAXIMUM EXTERNAL VOLTAGE: ±18 V.

AUXILIARY INPUTS

CLOCK IN: For external clock signal input.

START IN: External signal starts data generation. Prompts 8170A transition from Idle/Break to Active state.

STOP IN: External signal stops data generation. Prompts 8170A transition from Active/Break to Idle state.

BREAK IN: External signal halts 8170A at current address, outputs remain active. Prompts 8170A transition from Active to Break state.

INPUT CHARACTERISTICS (all positive edge triggered):

INPUT IMPEDANCE: >10 kΩ|| ≤25 pF.

LEVELS: high ≥+2.0 V, low ≤+0.8 V.

MINIMUM WIDTH (at +1.3 V): 40 ns.

MAXIMUM EXTERNAL VOLTAGE: ±18 V.

HP-IB CAPABILITY

INTERFACE FUNCTIONS IMPLEMENTED: SH1, AH1, L4, SR1, RL1, T5, PP0, DC0, DT0, C0.

KEYBOARD MODE: Remote programming of all front panel keys and functions. Coded loading and readout of data. Speed: 3 ms per character typical.

DATA MODE: Fast binary loading and readout of data only. Speed: 3 ms per byte typical.

RS 232C/CCITT V.24 CAPABILITY

Remote programming and listing of memory content, and display of current data bus format and address/data coding. ASCII 7, parity even.

BAUD RATE: 110, 150, 300, 600, 1200, 2400, 4800, 9600 selectable. Automatic generation of 2 stop bits for 110 baud, one stop bit for others.

General

POWER: 100, 120, 220 or 240 V, +5%−10%; 48-66 Hz, 110 VA maximum.

ENVIRONMENTAL: 0 to 55°C, with relative humidity to 95% at 40°C.

WEIGHT: 11 kg (24.3 lb).

DIMENSIONS: 133 mm H × 426 mm W × 422 mm D (5.2 × 16.8 × 16.6 in).

ACCESSORIES SUPPLIED

2 data output pods (Models 15455A, 15456A)

1 address input pod (Model 15453A)

1 control pod (Model 15454A)

Pods complete with Snap-on Assembly, wires, hook-on clips and carrying case.

OPTIONS

001: Additional 24K-bit memory for output format 8 bits × 4096 words or 16 bits × 2048 words.

002: Address driver (Model 15452A). Provides 10 address output lines A0 to A9, positive true. 3-state capability in idle state.

FAN OUT: 10 standard TTL maximum.

LEVELS: High ≥+2.4 V, low ≤+0.5 V.

SIGNAL CHARACTERISTICS (into 1 standard TTL):

TRANSITION TIMES (+0.5 V to +2.4 V): ≤50 ns.

DISTORTED HIGH LEVEL: ≥+2.4 V.

DISTORTED LOW LEVEL: ≤+0.8 V.

PRICES IN U.S.A.: 8170A, $5000; Opt. 001, $500; Opt. 002, $250.

MANUFACTURING DIVISION: BÖBLINGEN INSTRUMENT DIVISION
Herrenbergerstrasse 110
D-703 Böblingen
Federal Republic of Germany

An HP-IB Extender for Distributed Instrument Systems

This instrument eliminates the 20-metre distance restriction for HP-IB systems, enabling local and remote groups of instruments to operate together, usually with no extra programming. Modems or twin-pair cable provide the communications medium.

by David H. Guest

SINCE ITS INCEPTION in the early 70s, the HP Interface Bus (HP-IB) has greatly simplified the assembly of do-it-yourself instrument systems, lessening the need for custom engineering.[1] Its adoption as a standard* encouraged a proliferation of interest at a time when the industry realized the need for more organized methods of interconnecting instruments and other products with an intelligent controller. Such has been its success that now available are over six hundred different products worldwide, each of which is compatible with the standard and capable of being interfaced readily with any of the others.

When the HP-IB was originally devised, its designers initially tackled the immediate problems of local bench-top and rack-mount systems. As incorporated in products frequently described in these pages, the HP-IB provides a convenient means of interfacing local devices and a controller, but it makes no direct attempt to solve the problems of those wishing to access remote groups of instruments. Engineers are now finding an increasing need to monitor and control production processes from a central site, acquire data from diverse locations, and perform measurements that are inherently remote, as in testing communications plants. These applications still tend to require special engineering, or they might use a remote minicomputer to schedule detailed operations and communicate results via an RS232C modem data link to the central site—not an efficient or cost-effective approach for simple measurements.

The new HP Model 37201A HP-IB Extenders (Fig. 1) overcome the problem of distance. Used in pairs, they provide a direct extension of HP-IB facilities to a distant site, thereby putting all the convenience of the HP-IB technique directly at the disposal of those configuring distributed instrument systems.

The extenders do not provide a new interface scheme, but do provide a means of overcoming the 20-metre distance limitation of the existing standard bus, adding a whole new dimension to the HP-IB's possibilities. An assembled HP-IB system may be split into two isolated groups of instruments that communicate through a pair of extenders connected by a data link. The remote instruments appear functionally as if they were directly cabled to the local bus. The pair of HP-IB extenders and their associated data link are essentially transparent, that is, the interface behavior of programmed HP-IB systems is operationally identical with and without the extenders. For simple configurations, additional systems programming is usually unnecessary. Fig. 2

*HP-IB is Hewlett-Packard's implementation of ANSI/IEEE Standard 488-1978 and is in general compliance with the draft IEC Standard 625-1 expected to be published in 1979.

Fig. 1. *The Hewlett-Packard Model 37201A HP-IB Extender converts standard HP Interface Bus activity into a serial form for communication via normal full-duplex modems or twin-pair cable. Functioning in pairs, extenders enable two distant clusters of bus-interfaced instruments to operate as one.*

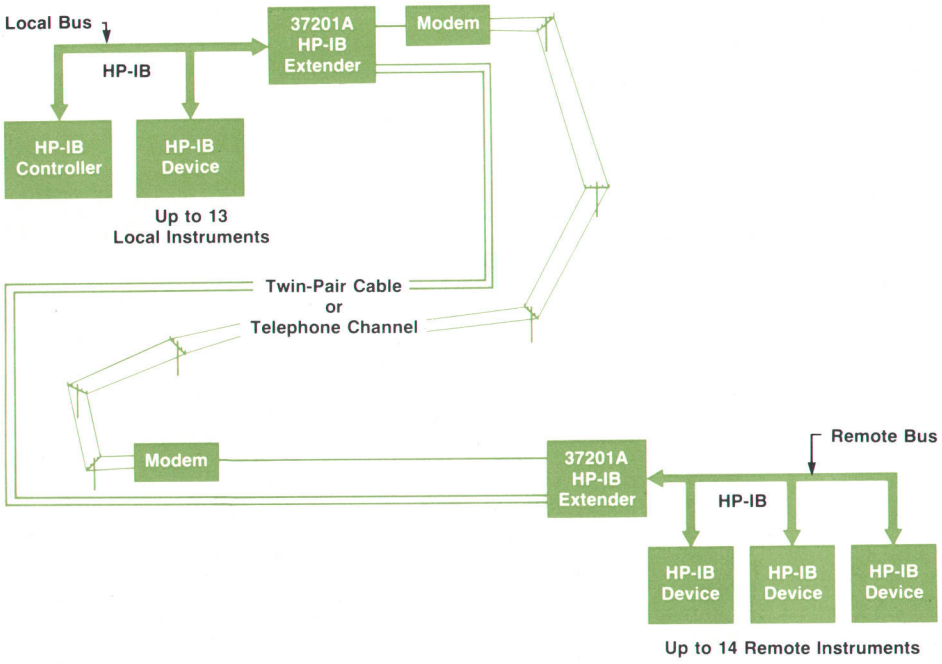


Fig. 2. *Two distant clusters of instruments are connected through a pair of 37201A HP-IB Extenders in this basic configuration. The controller can communicate with the remote instruments as though they were connected to the local bus.*

illustrates how devices are linked together using extenders.

Although fundamentally the extenders operate in pairs, various techniques (to be described later) may be used to provide access through one extender to more than one remote site.

Transparent HP-IB Extension

In general, HP-IB data travels in both directions between extenders so each extender is required to accept or source data, depending on the direction of transmission, in place of the distant responding device. Each 37201A Extender does this by hand-shaking HP-IB bytes from the device into its serial transmit buffer, or out of its serial receiver buffer to the device (see Fig. 3). This avoids end-to-end transmission of the three bus handshake lines (DAV, NRFD and NDAC), and the much slower system operation that this would entail. Along with each data byte, a copy of the five management lines (IFC, ATN, SRQ, EOI and REN) is also sent, giving a pair of bytes for transmission. Additionally, upon any change in one of the relevant management lines, a new copy of all five lines is sent; the associated data byte is marked as a dummy in this case.

Interpretation of data received by one extender from another is governed by a private protocol designed specifically for the purpose. This protocol is distinct from the HP-IB, although extension of HP-IB systems is, of course, its purpose. The user or programmer does not become involved with the protocol in any way, control still being through HP-IB operations. All translations are done automatically by the extenders.

Those closely familiar with details of the complete set of HP-IB functions will realize that strict implementation of the parallel-poll function subset is an insoluble task for any extension scheme. Devices are required to respond to a parallel poll in a much shorter time than interextender communications can achieve. Consequently, this HP-IB function is not supported by the 37201A HP-IB Extender. Serial poll, however, is fully accommodated. Also, the 37201A does not allow passing of bus control to a device at the remote site, a feature not usually required in the instrument systems for which it is mainly intended.

Serial Transmission between Extenders

For communication, the 37201A Extenders require a full-duplex data link, that is, one that allows transmission in both directions simultaneously. Standard data modems connected to the extender's RS232C (V.24) interface allow extension of HP-IB operation to any part of the world linked by telephone, either using switched-network (dialed) operation or dedicated leased lines. Both synchronous (up to 19.2 kbit/s) and asynchronous modems (150, 300, 600, and 1200 bit/s) are supported by the 37201A. Where continuous monitoring or control is not required, remote instrumentation can be called on a dialed connection, automatically if required, only when information is needed, thus avoiding the cost of leased lines. The higher transmission speeds, however, usually require leased-line operation.

Communication over short distances of up to 1000 metres can be provided without modems by using low-cost twin-pair cable (four wires) directly connected to the extenders. Balanced differential drive and transformer isolation give excellent immunity to interference pickup. The twin-pair bit rate is fixed at 20 kbits/s and during transfer of long strings of HP-IB data bytes, this gives a useful transmission rate up to at least 775 data bytes per second.

For transmission purposes, the 37201A's serial protocol takes byte pairs (data and bus-control bytes) from its transmit buffer and assembles them into variable-length transmission blocks or packets, each packet containing as much data as was available, up to a maximum of 30 byte pairs. Variable packet length improves efficiency. Each packet also has an identification header, a tail, and certain protocol information. In synchronous operation, the receiver searches for the header on a bit-by-bit basis as a means of

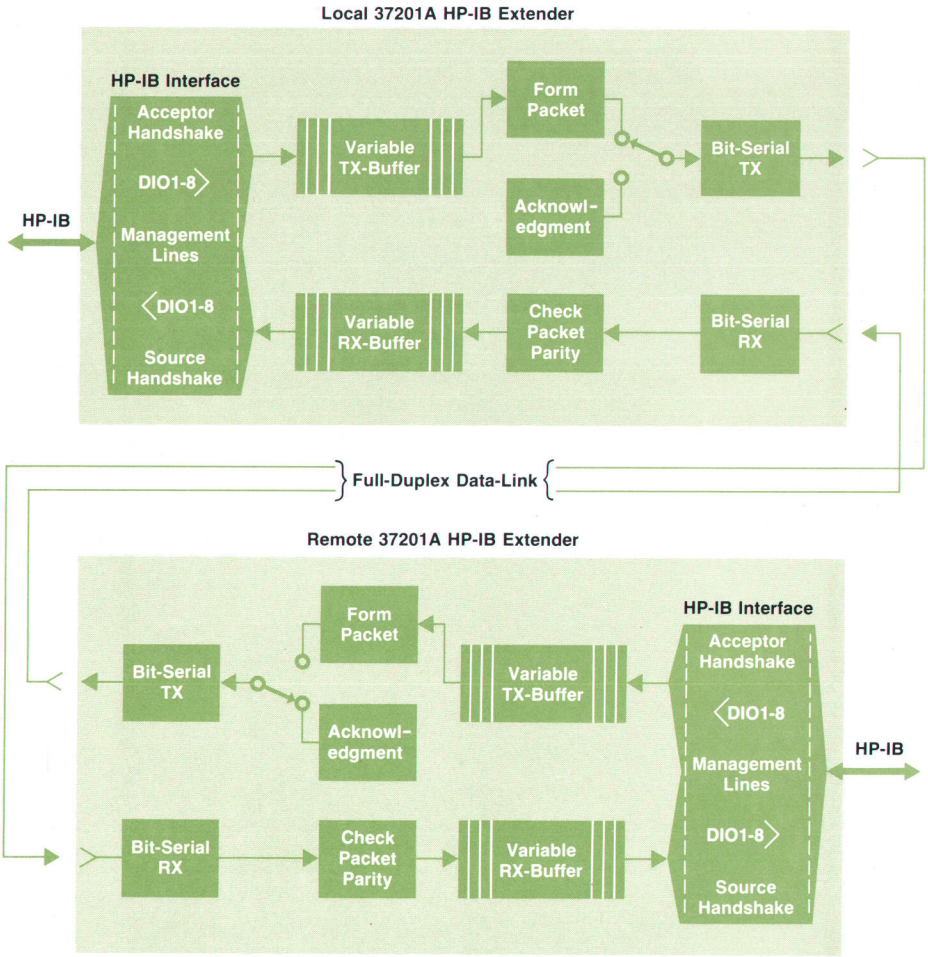


Fig. 3. *Simplified block diagram illustrates the functional operation of a pair of 37201A HP-IB Extenders.*

establishing byte-sync.

Error Detection and Correction

Corruption of data in transit between devices is a problem not usually encountered with normal HP-IB systems, but this becomes a matter of great importance in extended buses. Particularly with dialed-up modem connections, data transmission errors due to transient phenomena are highly probable. Since even a single-bit error on the bus is enough to cause complete operational breakdown, such errors obviously cannot be tolerated. Effective elimination of communication errors was therefore a prime objective in the design of the 37201A.

Forward error-correction techniques, such as those used in space applications for correction of relatively few isolated errors, are quite inappropriate in telephone data transmission where long strings of bits are commonly corrupted. For this reason, 37201A's use the only other possible approach, namely, correction by retransmission.

For error detection purposes, each transmitted packet has redundant longitudinal and vertical parity information added so that when received, packets can be checked for parity correctness in two dimensions. This technique is not quite as efficient in detecting certain errors patterns as a cyclic redundancy check, but it avoids special-purpose generating and checking hardware and may be performed very rapidly by microprocessor firmware. In fact, the vertical (byte) parity is automatically created and checked by the microprocessor system's serial-communication devices, leaving only a longitudinal byte summation for firmware. When a packet is received correctly, a short acknowledgment packet is returned to the originating extender, allowing it to proceed with new data. A corrupted packet is discarded and no acknowledgment returned. This causes the originator to retransmit the packet, which of course must be clearly marked as a repeat otherwise there is danger the receiver might implement the same data on the local bus twice—the acknowledgment itself may have been corrupted.

The user is unaware of these operations taking place, except in so far as HP-IB operation might slow down noticeably in the event of repeated errors. Even prolonged data-link breaks do not upset HP-IB functions—they merely stop, continuing faultlessly when the link is restored.

Coordinating Data Flow

In local HP-IB systems, any instrument temporarily unable to cope with further data bytes prevents overflow by

A Comprehensive Approach to Automatic Troubleshooting

Designers of microprocessor-based instruments usually incorporate routines to enable their products to self-test themselves. The overhead incurred is generally little more than the cost of some extra read-only memory, provided the technique is designed in from the outset. This is perhaps fortunate, because the complexity of features now available means that the user often has no other simple way of checking that the equipment is fully functional.

Very often these tests go no further than a pass/fail decision and make little attempt at aiding troubleshooting of a fault. One reason for this is that the lengthy program needed for fuller fault diagnosis cannot be accommodated economically, and even when it can, many instruments lack a suitable method of displaying results to the service technician.

While also incorporating a pass/fail test, the 37201A solves these two difficulties with a different approach to implementing a troubleshooting aid. Desktop computers such as the HP Model 9825A are commonly found in HP-IB environments, and for this reason, the 37201A's fault-diagnostic system is based partly on facilities available with this machine. At first sight, use of the 37201A's HP-IB port to give access for fault location using the computer would seem an obvious approach but in practice, so much of the 37201A is concerned with the HP-IB that an unacceptably large proportion of faults would prevent diagnosis from even beginning. Instead, an edge-connector is provided for coupling the 9825A Desktop Computer's standard 16-bit I/O interface card (98032A) directly into the 37201A's microprocessor.

Some 18 test files, each dedicated to testing individual parts of the 37201A, are available on a tape cartridge along with a master program. Under control of this master program running in the desktop computer, one file at a time is transferred to the 37201A with the aid of a short loader program resident in the 37201A firmware. For checking, a copy is also passed back to the master program. The first two bytes transferred indicate to the loader where in RAM the file is to be stored. The file is really a subroutine suitable for running on the 37201A's microprocessor and, having executed the transfer, the loader executes a subroutine call to the address given by the first two bytes. Each of the files (subroutines) has been carefully designed, along with facilities in the 37201A's hardware, to perform a simple diagnostic test as unambiguously as possible. Results of each test are passed back to the desktop computer, using the same routine used in checking the initial transfer, for interpretation by the master program. An appropriate printout or display then shows the operator which components are likely to be associated with any failure discovered.

Although individually they are fairly elementary, taken together the 18 sets of tests do a very comprehensive job of indicating the area of failure. Depending upon how closely the microprocessor is tied in to each functional circuit, a fault can often be pinpointed right to a particular IC pin, although in other cases only a small group of ICs can be identified. Appropriate routines have been designed for each of the areas tested. Stimulus-and-response tests with various bit patterns are used for random logic, the communications paths are exercised with data and looped-back progressively further from the processor, store and load of test patterns checks the RAM, parity tests are performed on each ROM device, and checks are carried out on operations of the microprocessor itself. Simple loop-back jigs are needed to test the drivers and receivers of the rear-panel interfaces because otherwise the processor cannot monitor or drive the outboard sides of these devices.

The technique does have its limitations, however. If the processor has a fundamental fault then even the loader will not run and no diagnosis can be reached, other than that the immediate area of the processor has failed. In this event, facilities for the use of signature analysis[1] are provided.

For convenience, tests are divided into three functional circuit areas (processor, HP-IB, and serial communications), with a complete test of the entire 37201A taking less than three minutes. Other advantages of cartridge storage for test routines are that extra ROM is avoided in the instrument (some 50% more would have been required) and that tests and operator readouts can easily be corrected and amended at late stages of development without affecting the product itself.

By its nature the 37201A HP-IB Extender presents very much a "black box" image to the user and service technician, and could easily have been a difficult device to troubleshoot. The diagnostic test system has already been invaluable in production testing and should prove a most useful aid in occasional field servicing.

-Peter Roubaud

Reference

1. R.A. Frohwerk, "Signature Analysis: A New Digital Field Service Method," Hewlett-Packard Journal, May 1977.

holding up the three-wire handshake sequence. With extended buses, however, no such direct mechanism exists. What, then, stops a sourcing device from pouring bytes down the serial data-link at a rate faster than a distant instrument can accept them? This is an additional function of the error-correction protocol. A slow acceptor device soon causes the associated extender's receive buffer to fill to capacity with bytes awaiting transfer. At this point, the extender prevents transmission of new data by failing to acknowledge any further packets until buffer space becomes available, thereby avoiding overflow. In turn, the transmitting extender holds up the source's handshake when its transmit buffer reaches capacity.

Automatic Dialing

Although the pair of 37201A's carry out their basic extension function without need for program control, the extender at the HP-IB controller end can be addressed as an HP-IB device in its own right for several purposes. One of these is the control of an automatic dialer that may be connected to the RS366 (V.25) interface provided on the extender. This enables a local controller and its associated extender to dial one of a number of extenders, each with its individual group of HP-IB instruments, automatically under program control. The dialer accepts the required telephone number from the controller via the extender's RS366 (V.25) interface and when the call is automatically (or manually) answered, transparent HP-IB control of that group of instruments can begin immediately. This provides an economical way of occasionally accessing remote data collection stations, avoiding the expense of dedicated leased circuits.

When HP-IB activity with a particular remote station is complete, the local station disconnects (goes "on-hook"), again on an addressed instruction from the controller.

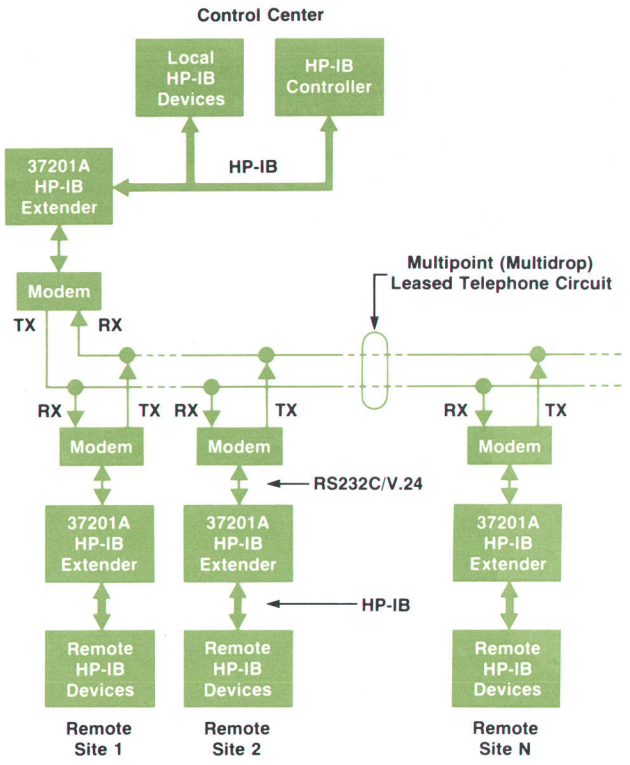


Fig. 4. *Multipoint connection using a 4-wire telephone circuit enables a controller to communicate with instruments at up to 31 remote sites, one site at a time.*

Within a minute of losing recognizable data packets, the remote extender also disconnects. This automatic disconnection was felt to be essential since otherwise any failure of the dialed connection could leave the remote station "off-hook" and therefore unable to respond to further call attempts, clearly an undesirable situation for an unmanned station.

Multipoint Operation

If several distant stations must be accessed frequently, a multipoint (often called multidrop) arrangement is called for (Fig. 4). Telephone companies arrange leased telephone circuits specifically for this type of configuration, enabling all the remote modems' receive ports to be functionally connected in parallel with the local controlling modem's transmit port, and all remote transmit ports in parallel with the local receive port. All remote modems receive continuously so that each extender is able to wait for its own address (preassigned by switch selection). A packet containing the required address is sent from the controller-end 37201A following an addressed instruction from the controller. This causes the 37201A that recognizes its own address to turn on its modem's carrier and begin corresponding with the controller 37201A. Any previously addressed station automatically turns off. For example, switching from any other multi-point station to station 7 in the middle of an HP-IB applications program is executed very quickly and conveniently by means of the addressed instruction M7.

Loss of Remote Data

Although the extension of an HP-IB system adds a degree of hardware complication, great stress has been laid on simplicity of use and verification of correct system operation. The latter is most important when remote stations are inconveniently located. In particular, facilities have been provided for determining that a pair of 37201A's and their associated data link, which usually will be under control of a telephone company, are properly cabled-up and functioning correctly.

Each 37201A has a LOSS OF REMOTE DATA LED indicator that gives immediate confidence of correct operation by extinguishing when the extender pair has been brought successfully into mutual communication. It stays off as long as packets are both received and acknowledged, but any prolonged data-link failure is reliably signalled within eight seconds. In the absence of HP-IB traffic, when packets would not otherwise be sent, the extenders exchange dummy packets to keep testing the link. This means that extinction of LOSS OF REMOTE DATA indicates correct operation of the link and extender pair regardless of whether other HP-IB devices are connected or operating.

System Considerations

Without actual physical disconnection, the pair of extenders can effectively be isolated from the local (controller) bus by addressing an IDLE instruction to the local 37201A. This prevents communication with the remote site until a future ACTIVATE instruction occurs, leaving the local instruments to run a program on their own. At first sight, this idling of the extension functions may seem a strange feature to want, but it provides solutions to several very practical operational problems.

Being transparent, the extenders do not know the physical location of the device for which any particular message is destined. Consequently, normal operation requires that all messages be transmitted to the opposite site. This means that all bus operations, even local ones, ordinarily can proceed only at a speed limited (usually) by the rate at which the serial link allows data to be transmitted. At 1200 bits/s asynchronous, for example, the effective HP-IB rate will be about 38 data bytes/second. For local transactions not involving distant instruments, such a relatively slow speed may be inconvenient. Using the IDLE function increases the bus speed, enabling the local 37201A to complete the handshake cycle at a rate of up to some 2400 data bytes/s (and of course watching for its own address) but otherwise taking no active part in bus operation. Judicious use of IDLE and ACTIVATE instructions can thereby reduce the effects of slow data rates.

Another use of the IDLE function is in avoiding system hang-up when data-link failure occurs—not an uncommon event in dialed-up connections. Data-link breakdown may result in the local 37201A's transmit buffer rapidly reaching capacity since the data has nowhere to go, and in this event, the 37201A automatically avoids data overflow by holding up the handshake. Such a suspended handshake, of course, usually means that further normal bus operation cannot proceed, not even local transactions.

To cope with such situations a feature may be preselected by the programmer to clear the transmit buffer automati-

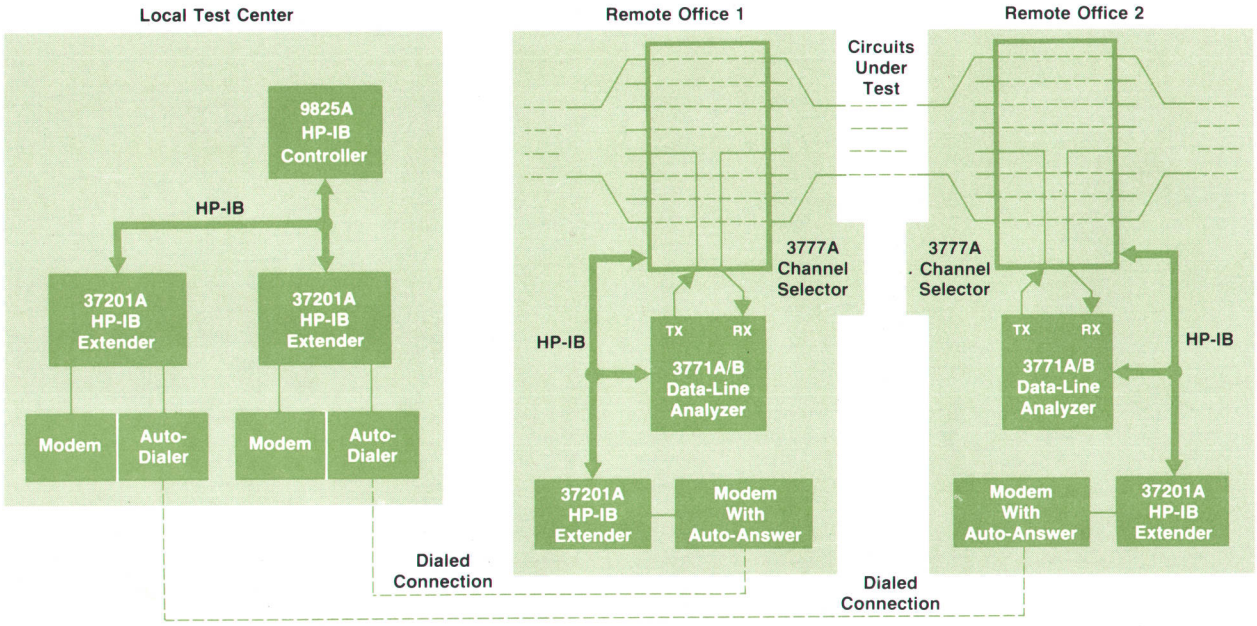
Applying the 37201A HP-IB Extender

Uses for extended HP-IB systems are virtually unlimited, but the system outlined here clearly demonstrates many of their possibilities. The diagram shows how a telecommunications test center can perform remote measurements on large numbers of leased telephone circuits as they pass through distant offices. High quality private-line telephone circuits, often used for data transmission and other demanding tasks, may be accessed for testing at the offices through which they are routed. Transmission measurements, for example of level, noise and transient phenomena, need to be carried out routinely to verify quality, and as required when faults are reported.

Using 37201A HP-IB Extenders, the necessary equipment at any two remote offices may be operated readily from a conveniently placed test center, eliminating the need for remote personnel. Control of the circuit access switching and of the measurement equipment is by standard HP-IB commands. The bus is extended to the remote sites by pairs of 37201As over modem connections, using auto-dialers and auto-answering modems. This enables the appropriate two offices in the network to be called simultaneously for end-to-end testing of the desired circuit.

Normally, circuits are routed straight through the channel selectors at each site but, under HP-IB control, each end of any particular circuit can be intercepted and switched to data-line analyzers for transmission measurements. Control of the measurements is also from the local center and results are passed back there, all via the HP-IB. With more complex switching arrangements, powerful network management systems can be built using readily available techniques.

-Simon Murray



cally upon prolonged loss of remote data, thereby enabling handshake operations to resume. Data is lost, but a data-link failure results in loss of remote control anyway, and the feature enables local operation to continue without manual intervention (given a suitable controller program). Upon such a data-link failure, the local 37201A can also request service (SRQ) from the controller to alert it of the event. Following the service request and a serial poll, the controller's next action should be to idle the extender so that local bus operations can proceed uninhibited by the failed data link.

Monitoring the Extenders

With many of its facilities in use, the 37201A interacts in a complex manner with a data link, modems, dialer, instruments and other 37201A's. Keeping track of system activity could be a significant problem, particularly when the unexpected occurs at an unattended station. Being designed for systems work, however, the 37201A goes a long way toward providing full information about its own operational state and that of its interfaces.

Basic information is provided by front-panel LEDs, and for unattended operation similar data may be obtained from the local 37201A's status byte by serial polling. The local 37201A can be enabled to request service (SRQ) for reporting the occurrence of several events including the success or failure of an automatic dialing operation and of data-link breakdown. Further useful operational data can be obtained by addressing the local 37201A to talk, whereupon it issues four data bytes of additional information to the controller.

Implementation and Self-Test

Needless to say, the data handling and control functions just described are undertaken by a microprocessor. In fact, along with its RAM and 7K bytes of program ROM, the microprocessor is the very heart of the 37201A and per-

OPERATING CHARACTERISTICS
HP Model 37201A HP-IB Extender

HP-IB DATA RATES*
TWIN-PAIR CABLE INTERFACE: 775 data bytes/s.
SYNCHRONOUS MODEM INTERFACE: 744 data bytes/s at 19.2k bits/s and pro-rata at lower serial data rates.
ASYNCHRONOUS MODEM INTERFACE: 38 data bytes/s at 1200 bits/s and pro-rata at lower serial data rates.
*Assumes continuous data byte transfer between two devices on short error-free link.
SERIAL DATA RATE
TWIN PAIR CABLE OPERATION: 20kbits/s fixed.
ASYNCHRONOUS MODEM OPERATION: 150, 300, 600, 1200 bits/s.
SYNCHRONOUS MODEM OPERATION: Up to 19.2kbits/s.
TWIN PAIR CABLE INTERFACE
RANGE: 1000 metres.
CABLE TYPE: Twin twisted pair with separate shields (recommended type HP8120-1187).
LONGITUDINAL ISOLATION: Provides rejection of common-mode interference.
MODEM INTERFACE: Compatible with EIA RS-232C and CCITT V.24.
AUTODIALER INTERFACE: Compatible with EIA RS-366 and CCITT V.25.
POWER REQUIREMENTS: 100/120/220/240Vac, +10–13%; 48 to 66 Hz; 30VA max.
OPERATING TEMPERATURE: 0 to +55°C.
DIMENSIONS: 89 mm H × 426 mm W × 356 mm D (3½×16¾×14 in.).
WEIGHT: 5.7 kg (12.5 lb).
PRICE IN U.S.A.: $1840.
MANUFACTURING DIVISION: HEWLETT-PACKARD LTD.
South Queensferry
West Lothian EH309TG
Scotland

forms nearly every activity. It is surrounded by specialized parallel I/O for controlling the HP-IB, modem, and dialer interfaces, and serial I/O devices for asynchronous and synchronous serial communication. Line coding and decoding circuits condition the serial data for transformer-coupled balanced transmission in the twin-pair cable mode, thereby providing excellent immunity to longitudinal (common-mode) noise interference.

Means of verifying correct operation of a data handling device such as the 37201A are most important, since there is ordinarily little the user can tell about its continuing ability to fully perform the task. This is particularly true in the event of system failure when quick identification of the failed device is needed. To this end, the 37201A has a self-test mode that causes repeated exercising and testing by the microprocessor of nearly all the instrument's hardware. In addition to tests on ROM, RAM and the processor itself, the HP-IB and serial interfaces are automatically looped-back for verification of correct operation. Failure is clearly indicated by the wrong pattern on the front panel LED indicators.

David H. Guest

David Guest's early interest in amateur radio led to a B.Sc. honors degree at Heriot-Watt University, Edinburgh, Scotland. After joining HP in 1970 he continued part-time study leading to an M.Sc. degree. At HP, he contributed to the 3761A Bit Error Detector and was project leader on the 3770A Amplitude and Delay Distortion Analyzer, earning two patents relating to techniques used in the 3770A. When family responsibilities permit (he has a son, 1) David relaxes by water-color painting and extending his musical appreciation with his wife's professional guidance. He recently built a traditional mercury barometer—not a measurement technique he expects HP to adopt.

Acknowledgments

Much of the hardware design and most of the microprocessor firmware programming was undertaken by principal contributors Peter Roubaud and Simon Murray. With much interaction, Peter specialized in the HP-IB functions and Simon in the communications. Tony Cowlin efficiently packaged the concept. Thanks are also due to David Warren, many of whose early ideas were incorporated and who groomed a high-level language compiler into a key development tool.

Reference

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