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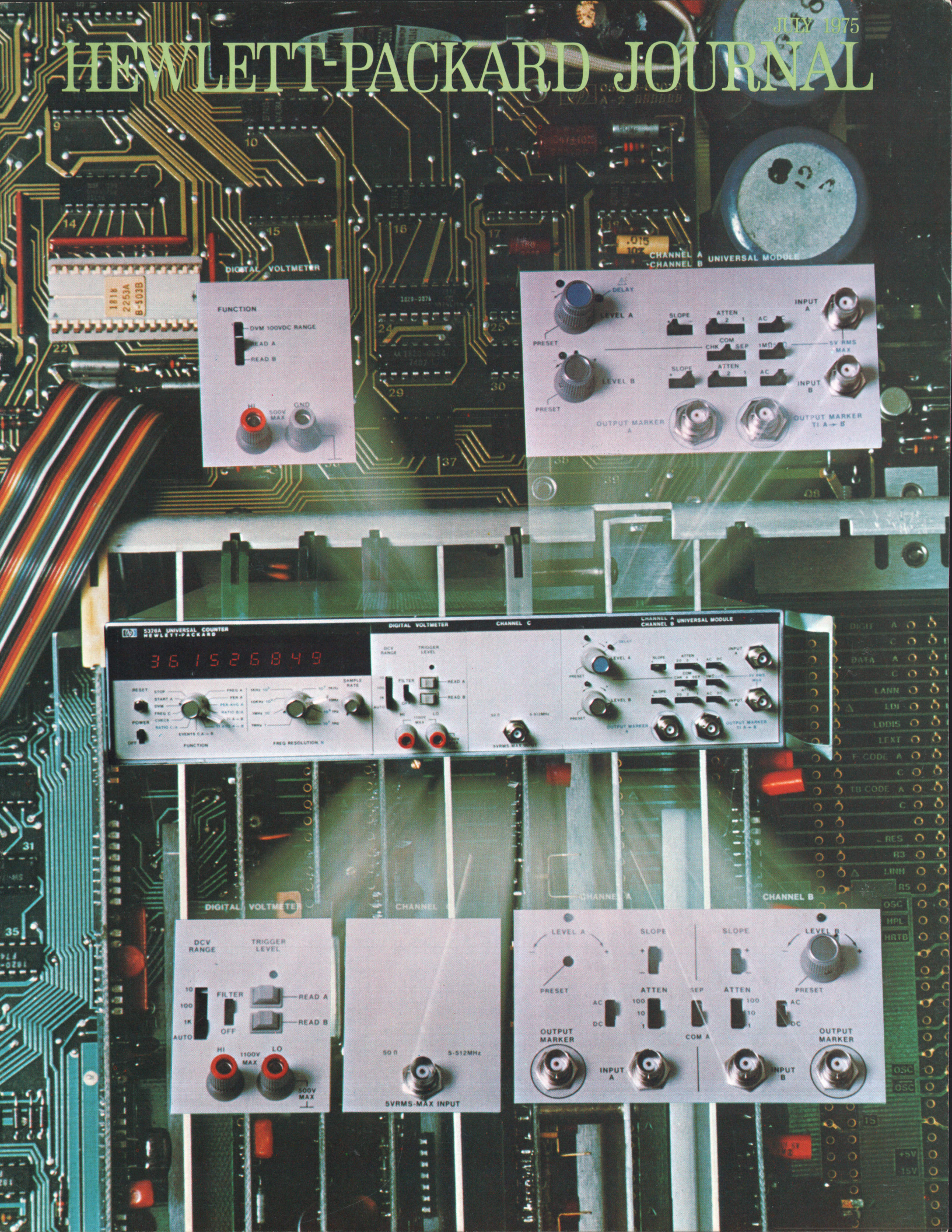


Modularity Means Maximum Effectiveness in Medium-Cost Universal Counter

A single mainframe and a wide choice of optional timer, counter, and DVM modules provide better performance at lower cost, meet each user's needs precisely, and leave room for future growth.

by James F. Horner and Bruce S. Corya

HOW DO YOU DESIGN AN INSTRUMENT for the broad middle range of electronic counter applications? How do you meet each user's needs precisely, yet offer room for future growth? How do you decrease cost yet increase performance?

The answers to these and many similar questions, we believe, are found in the new Model 5328A Universal Counter, Fig. 1. This single instrument is the successor to six counters, Models 5326A/B/C[1] and 5327A/B/C. It offers improved performance, lower cost, and several new features. Its modular design makes it possible for a user to choose only the features he needs, yet leaves the door open for expansion at a later date.

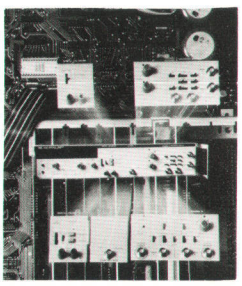
What It Is

The 5328A is basically a power supply and counter mainframe that supports user-selected options. In its standard configuration it offers a complete portfolio of universal-counter functions:

- Frequency—100-MHz direct count
- Period—100-ns resolution
- Period Average—10-MHz clock
- Time Interval—100-ns single-shot resolution
- Time Interval Average
- Totalize—100 MHz
- Ratio—100 MHz/10 MHz
- Check.

The inputs have matched (±4 ns) 100-MHz amplifiers with ac or dc coupling, ±2.5V trigger-level range, three-position attenuators (×1, ×10, ×100), 1-MΩ input impedance, slope controls, trigger lights that act like logic probes, and high-speed output markers.

Capabilities can be greatly expanded by selecting options. Two DVM options provide dc voltage measurements. One is an economy version that offers millivolt sensitivity, 10-MΩ single-ended inputs, 125V range, 0.5% accuracy, and the "read trigger level" function. The other is a high-performance unit that has 10-μV sensitivity, automatic or manual range control to 1000V, 10-MΩ floating inputs, switchable filter, 0.03% accuracy, read trigger level function, variable integration time, and high-speed acquisition (up to 300 readings per second with two-digit resolution). For applications requiring greater frequency range, a 5-to-512-MHz direct-count option is avail-



Cover: *Model 5328A Universal Counter and its optional input modules are superimposed on a background photograph showing the counter's interior and the bus-oriented architecture that makes its high degree of modularity possible. Input modules available include two DVMs, two universal timer/counter modules, and a 512-MHz frequency counter module.*

In this Issue:

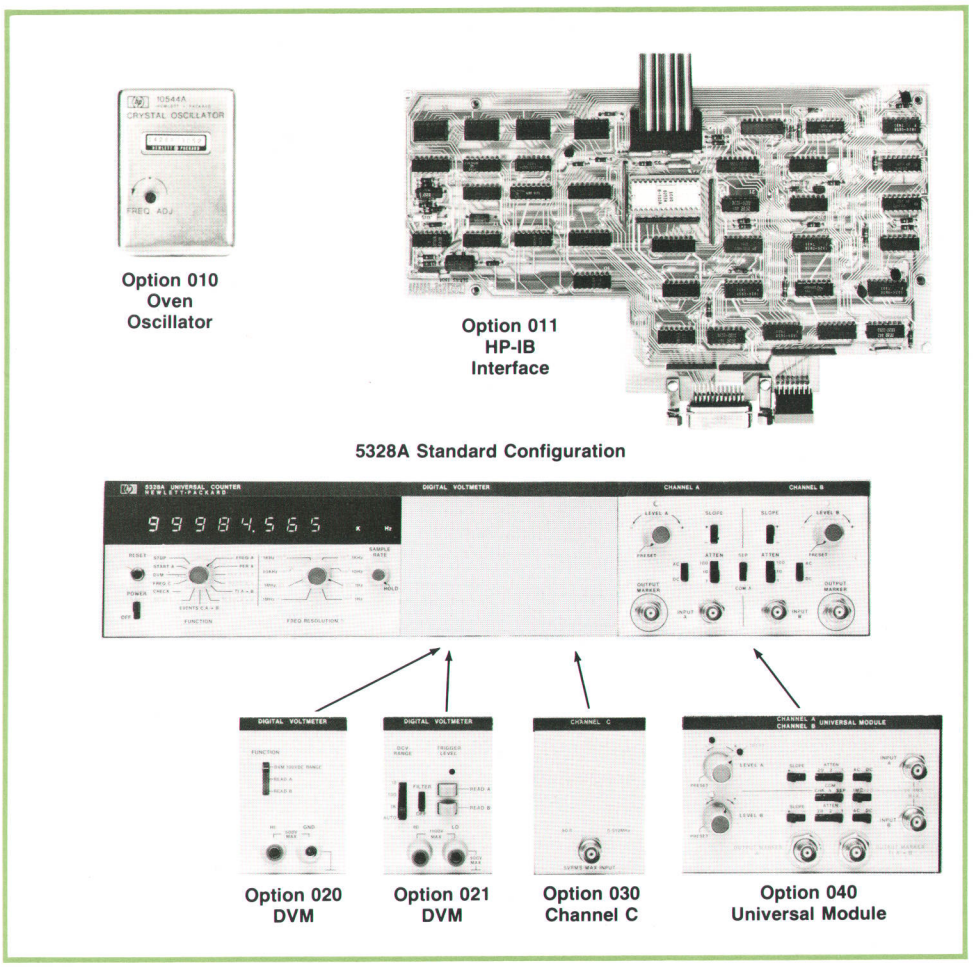


Fig. 1. *Model 5328A Universal Counter and options. Standard configuration, consisting of mainframe and universal module, provides all standard universal counter functions, has trigger lights and output markers. Direct counting range is 100 MHz. Optional universal module has one more digit of time interval resolution and a jittered clock for problem-free time interval averaging. Channel C option has a 512-MHz direct counting range. Digital voltmeter options—economy and high-performance—can read channel A and B trigger levels as well as external dc voltages. Other options are high-stability time base oscillator and HP interface bus module.*

able. This option offers 15-mV sensitivity across the band, 50Ω fuse-protected input, and a ninth digit added to the eight-digit mainframe. For applications requiring a precision time base, a high-performance oven-stabilized time base option is available.

For greater precision in the basic counter functions, there is a high-performance universal module. It has a 100-MHz clock for increased resolution in time interval and period measurements. Its functions are:

- Frequency—100-MHz direct count
- Period—10-ns resolution
- Period Average—100-MHz clock
- Time Interval—10-ns single-shot resolution
- Time Interval Average—100-MHz phase-jittered clock
- Totalize—100 MHz
- Ratio—100 MHz/10 MHz
- Check—100 MHz

The inputs have matched (±2 ns) amplifiers, ac/dc coupling, ±2.5V trigger level range, three-position attenuators (×1, ×2, ×20), 1-MΩ or 50Ω switchable input impedance, slope control, logic-probe trigger lights, channel-A high-speed marker, time-interval A-to-B high-speed marker, and a variable-delay feature.

For systems applications an HP interface bus (HP-IB) option is available.

Organization

The new counter is organized into four main operating regions (see Fig. 2):

- The main counter area
- The input options area
- The power supply area
- The HP-IB area.

Each region operates relatively independently and communicates to the others through an internal bus system (see article, page 9).

The power supply provides regulated dc voltage for the other operating areas of the instrument. Its capacity is sufficient to accommodate any combination of options. The main on-off switch of the instrument operates only the central power supply regulator; the main ac power line is never broken. Unregulated dc is constantly fed to the oven oscillator (if installed), eliminating the need for time-base warm-up. The fan gets its power from the ac power line by way of a triac, which is switched off by an optical isolator when the instrument is turned off.

Main Counter Area

The main counter area contains all of the functional subunits of a standard counter with the exception of input signal conditioning and special logic, which are contained in the input options section. The decade counting assembly contains eight decades of BCD counting logic, latches, and output multiplexing logic. The time base assembly contains eight counting decades, output multiplexing logic, and synchronizers to generate precise timing signals for the main gate. The oscillator section contains the standard room-temperature 10-MHz oscillator circuit and the input/output logic to accept an external signal from the rear panel or an internal signal from the optional crystal oven oscillator.

The sample rate section controls the instrument display cycle. Inhibit, reset, main gate, transfer and sample rate signals are generated in this section, as is the BCD digit address code for the strobed display. Generation of decimal point and annunciators and BCD data decoding are accomplished by the display control circuits. Data out of the decade counting assembly or the input option modules is decoded and displayed on the eight-digit LED display.

The function selector serves as the main signal switch of the instrument. It routes input signals through multiplexers to the decade counting assembly and/or the time base. At the same time, it interacts with the display control circuits to determine the beginning and end of the display cycle. The precision ECL main gate signal is created on the function selector through interaction with the time base assembly. The function selector also has extensive interaction with the input option modules. It is the main receiver of the high-speed data from the modules and the originator and receiver of module arming pulses.

The flexibility of the 5328A comes from the ability of all these operating subsections to accept diverse data from various combinations of input option modules. This is accomplished through the use of a 4K read-only memory (ROM) as the master control of the instrument. Located in the display control section of the instrument, the 4K ROM accepts the four-bit function code and the three-bit time base code from the front-panel switches or the HP-IB remote programming board, and generates 32 bits of output data which are transmitted throughout the instrument to set up each subsection for the particular measurement situation. Various combinations of input option modules are accommodated without circuit change as different ROMs are plugged into the instrument. This provides inherent obsolescence protection for the user. As each new input module is engineered, the mainframe needs only a new ROM (supplied in an update kit) to accept it.

Input Options Area

The input modules are the main interface between the instrument and the outside electronic environment. They accept input signals and convert them into the proper form to be handled by the main counter circuits.

In the universal module reside the main input amplifiers and Schmitt triggers. High-speed synchronizers for complex timing measurements also reside in the universal module. One of the key performance options of the 5328A is the selection of one of the two universal modules. The prime difference between the two is the basic clock rate. In the standard unit the basic 10-MHz clock provides 100 ns as the fundamental timing unit. In the high-performance unit, a phase-lock multiplier extends this rate to 100 MHz and a basic timing unit of 10 ns. In the time interval averaging function, the multiplier unit, upon command from the ROM, phase modulates the 100-MHz clock with band-limited noise to prevent the synchronous lockup problems associated with this measurement.[2] Replacement of the standard universal module with the high-performance module replaces TTL technology with ECL technology without burdening the instrument mainframe with unnecessary cost.

The middle section of the option module area provides the instrument with extended frequency capability. A 50Ω fuse-protected 512-MHz amplifier and Schmitt trigger feed the 512-MHz decade. Latches in this option strobe the ninth (least significant) digit from the module onto the data bus and into the display. In functions not requiring an input from this module, ROM lines deactivate the output strobing circuitry and the ninth digit on the display goes blank. The ninth LED digit is loaded into the mainframe display board only when the channel C module is installed.

The third region of the option section contains the inputs for the optional digital voltmeters. Using a voltage-to-frequency conversion technique,[1,3] these modules provide an output suited to the frequency measuring capabilities of the mainframe. The low-cost unit provides the 5328A with inexpensive access to the important capability of trigger level measurement as well as an excellent general-purpose single-ended voltmeter. In this unit and the high-performance unit, trigger level measurement is selected by means of switches located on the DVM panel. When the user selects either READ LEVEL A or READ LEVEL B, the DVM module disconnects itself from the external banana input jacks, attaches itself to the selected trigger level voltage, disengages the function and time base front-panel switches, places the code DVM on the function code bus and places 0.1-s gate time (1-mV sensitiv-

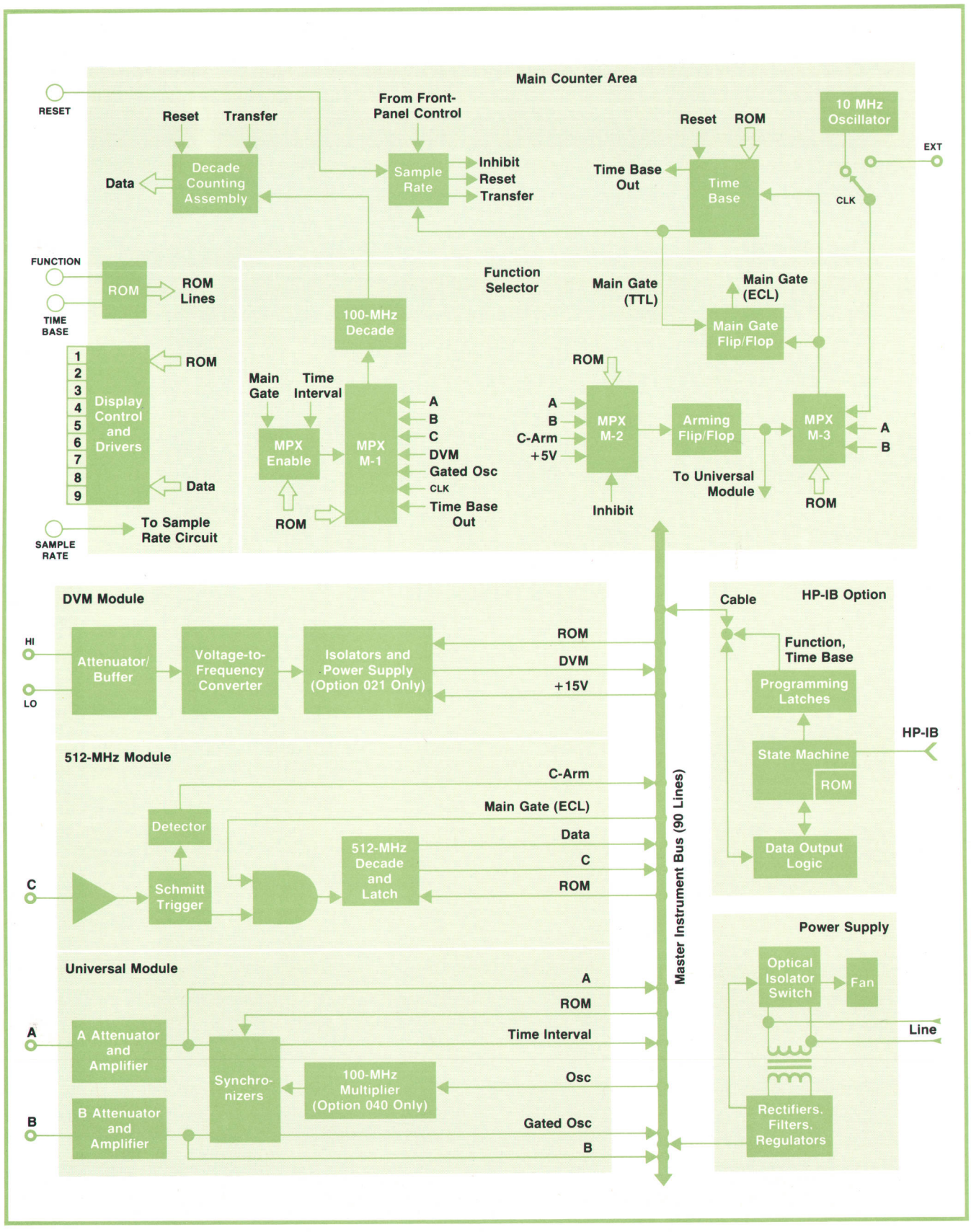


Fig. 2. *Four main operating areas are the main counter area, the input options area, the power supply area, and the HP-IB area. These communicate via the master instrument bus. Future options can be accommodated easily by a change of read-only memory (ROM).*

Mechanical Design of an Option-Configurable Counter

The mechanical design of the 5328A Universal Counter was a key factor in achieving the desired goals of modularity, serviceability, and low-cost producibility. The question that had to be answered was, "How do we structure a package to allow the customer to configure his own instrument efficiently from a wide range of options?"

Adoption of the new HP System II instrument enclosure, with its structural front casting to support front panels, was the first step down the road to a modular universal counter with multiple front-panel configurations. The next step was to design optional hardware printed circuit cards to plug directly into a common data bus on the motherboard, thus allowing any desired option mix. The space remaining on the motherboard was dedicated to the counter circuits common to any set of options. Placing these circuits on the motherboard made space available to plug the HP-IB option into the motherboard and out the rear panel. Placement of the power supply in the rear corner of the package allowed for both heat sinking and the mechanical integrity required for many of the heavier components. Thus, the 5328A was divided into four major sections—counter mainframe, power supply, input options, and HP-IB interface card.

By taking advantage of the mechanical strength inherent in the System II corporate package and the rigidity of the motherboard in the horizontal plane, the 5328A was designed with a single cross-member bracket instead of a large chassis. This feature allows access to the entire motherboard from both sides (Fig. 1). The HP-IB option can be removed from the instrument for test while still electrically attached by a cable. The modular power supply can be completely tested before it is installed. The common motherboard circuits can be electrically isolated into five separate circuits. Available in a kit are diagnostic test cards (Fig. 2) that replace the function selector circuits and use the instrument's display to output test information. This allows rapid failure detection, often at the component level. Thus the modularity of the 5328A has been used to achieve the desired level of serviceability.

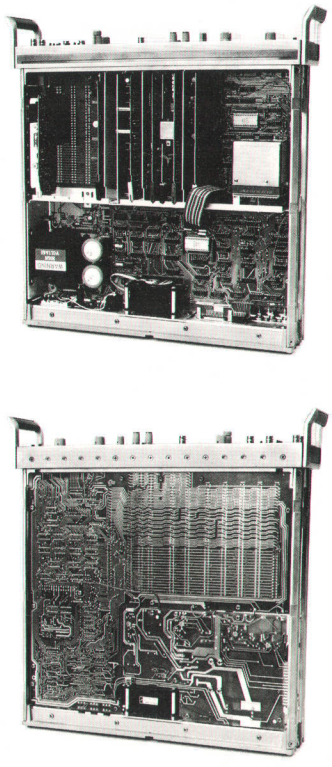


Fig. 1. *Single-cross-member design allows access to both sides of motherboard.*

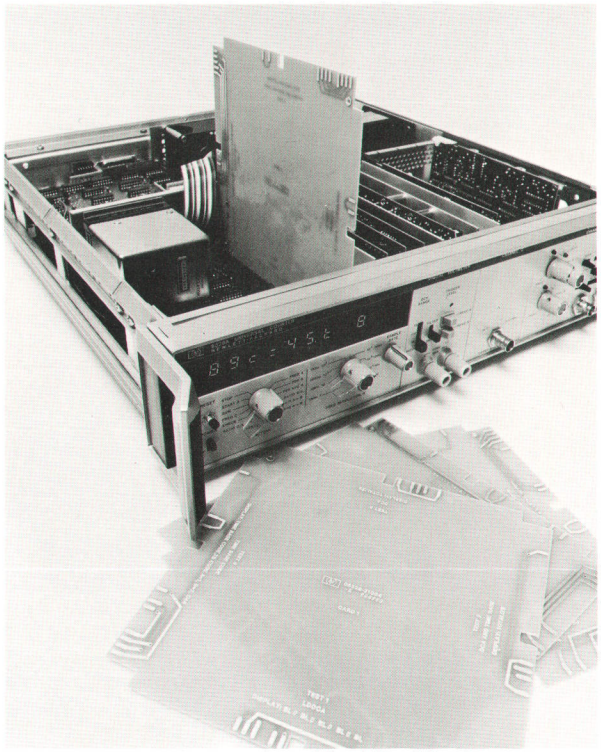


Fig. 2. *Diagnostic test cards use the display to output test information, often pinpointing failures to the component level.*

Efforts to minimize factory cost in the 5328A were made in fabricated parts manufacture and instrument assembly. The placement of the circuits on the motherboard eliminated the need for at least five printed circuit boards and their connectors. By fabricating the motherboard and the power supply printed circuit board on the same blank and separating them later, a savings of nearly 50% was made. The modular front-panel concept was aided by building two extrusions, one for the display and control section and one for the option modules. Dedicated tooling to blank these extrusions provided significantly superior and lower-cost front panels than had previously been available because a subpanel and a dress panel were replaced in each module by a single extrusion panel. By loading components on the motherboard and using printed-circuit-mounted switches extensively, the total wiring time for the 5328A was reduced to less than 20% of that required for any 5326 or 5327 unit. Assembly time was further reduced by decreasing the fabricated parts count by the design of multiple-function mechanical parts.

ity) on the time base bus. Upon release of the READ LEVEL switch, the instrument returns to its previous state. Thus the user can check his trigger levels without having to change and reset his function and time base settings.

The high-performance DVM option provides the user with the measurement capability of a manual or autoranging floating DVM that has a range of 10 μV to 1000V and a basic accuracy of 0.03%. For particularly noisy environments, a switchable filter may be engaged to increase normal mode rejection to 50 dB at 50 or 60 Hz. Isolation for this option is accomplished through special high-speed transformers, optical isolators, and an on-board switching dc-to-dc power supply. Although no remote programming of the front-panel controls is possible, remote controlled voltage measurement is quite easy. Through the use of special range controls in the V-to-F converter, a conversion factor of 10 kHz/volt is maintained regardless of the DVM's range. The voltmeter may be placed in autorange and the user simply programs the DVM function from the HP-IB and any voltage from 10 μV to 1000V is measurable.

This technique results in a small problem. If, for example, the user puts 900 volts on the input terminals, the output frequency is 900 × 10 kHz = 9 MHz. In a measurement time of one second, this would provide a resolution of 1 part in 9×10^6, far beyond the resolution limit of the V-to-F converter. To prevent the user from misinterpreting his results, the module blanks the meaningless data, thus providing the user with a display that contains only accurate data.

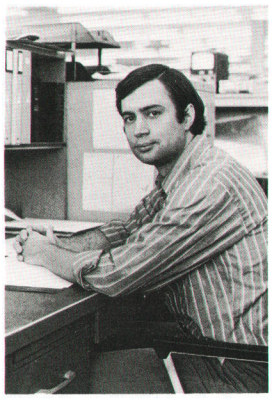
In the measurement of trigger levels, the high-performance DVM performs much like the low-cost version, with an important exception. Measurement of trigger levels normally requires the user to compensate mentally for the attenuation factor used in the universal module input attenuator. For example, if one volt is the trigger level voltage, ×1 attenuation yields an effective trigger level of one volt, ×10 attenuation yields ten volts, and ×100 attenuation yields 100 volts. The high-performance DVM, in combination with the high-performance universal module, eliminates the need for mental multiplication, automatically reading out the effective trigger level in the three possible ranges of ±2.5 volts, ±5 volts and ±50 volts.

HP-IB Area

The fourth area of the instrument, the HP-IB board, provides for control of the counter by the HP interface bus. Plugging into the main instrument bus through a ribbon cable, the internally mounted HP-IB board controls function, time base, cycle rate, arming, and virtually all other controls in the instrument with the exception of the DVM and universal module front-panel controls. A special module programming system in the HP-IB board allows any future module to be programmed through the present HP-IB system. For a more detailed description of the capability of the HP-IB option, see the article beginning on page 9.

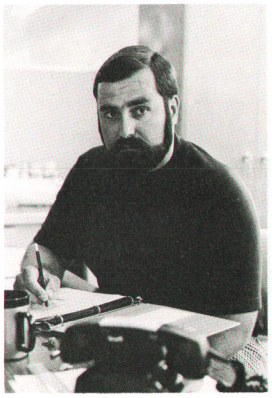
Acknowledgments

The 5328A project was a team effort from beginning to end. The key members of the team were Karl Blankenship, Ian Brown, Mike Wilson, Al Langguth, and Bill Jackson. In addition to the design team,



James F. Horner

Jim Horner, project manager for the 5328A Universal Counter, is a graduate of Stanford University—he received his BSEE degree in 1966 and his MSEE in 1968. With HP since 1970, he's contributed to the design of the 5327 Universal Counters and served as project leader for the 5306A Multimeter/Counter. Before joining HP he served for two years as an officer in the U.S. Army. Born in Paso Robles, California, Jim now lives in Santa Clara with his wife and two daughters. The Horners are proud of their mini-ecosystem that includes a garden and seven egg-laying chickens. Jim enjoys all sports and coaches a volleyball team made up of HP engineers. He's also a hang-glider pilot and a novice astronomer.



Bruce S. Corya

Bruce Corya was product designer for the 5328A Universal Counter, and before that was product designer for the 5381A/82A Counters, the 5300B Measuring System, and several 5300-Series snap-on modules. He joined HP in 1969, just after graduating from Purdue University with a BSME degree. In 1971 he received his MSME degree from Stanford University. Bruce was born in Greensburg, Indiana. He and his wife, who live in Santa Clara, California, both work at HP's Santa Clara Division and are travel enthusiasts. Bruce enjoys sports, particularly swimming and participating in the Santa Clara Division softball league.

SPECIFICATIONS
HP Model 5328A Universal Counter

Input Characteristics

CHANNEL A AND B (standard and option 040)
SENSITIVITY:
25 mV rms, 0—40 MHz (dc coupled)
20 Hz—40 MHz (ac coupled)
200 kHz—40 MHz (ac coupled and 50Ω with Opt. 040)
50 mV rms, 40 MHz—100 MHz
Min. pulse width: 5 ns, 140 mV p-p
COUPLING: ac or dc, switch selectable
IMPEDANCE: 1 MΩ || <40 pF (switch selectable 1 MΩ or 50Ω nominal with Opt. 040)
TRIGGER LEVEL: Variable over ±2.5 volts times attenuator setting with 0 volt preset position.
TRIGGER SLOPE: independent selection of + or − slope
ATTENUATORS: ×1, ×10, ×100 (×1, ×2, ×20 with Opt. 040)
DYNAMIC RANGE: 25 mV to 1 V rms × attenuator setting for 0—40 MHz; 50 mV to 500 mV rms × attenuator setting for 40—100 MHz
MAXIMUM INPUT (dc coupled):
X1: 250 V rms, dc—50 kHz
1.25×10^7 V rms/freq., 50 kHz—2.5 MHz
5 V rms, 2.5—100 MHz
X10, X100: 250 V rms, dc—5 MHz
1.25×10^8 V rms/freq., 5—100 MHz
X2, X20: 250 V rms, dc—500 kHz
(Opt. 040) 1.25×10^8 V rms/freq., 0.5—25 MHz
5 V rms, 25—100 MHz
Ac coupled: Vmax = 200 V (peak + dc) for dc—20 Hz; same as dc coupled for frequency greater than 20 Hz.
Opt. 040 50Ω position: 5 V rms, dc—100 MHz
CHANNEL INPUT: Common A or separate, switch selectable. In COM A position, sensitivity remains the same. Impedance becomes 1 MΩ || <65 pF for the standard and 500 kΩ || <65 pF for the Option 040 high impedance position. 50Ω position remains nominal 50Ω.
CHANNEL C (option 030)
SENSITIVITY: 15 mV rms, 5 MHz—512 MHz
TRIGGER LEVEL: 0 V, fixed
IMPEDANCE: 50Ω nominal
MAXIMUM INPUT: 5 V rms
INPUT PROTECTION: Fused
COUPLING: dc

Frequency Measurements

FREQUENCY A (standard and option 040)
RANGE: 0—100 MHz direct count
RESOLUTION: 1 MHz to 0.1 Hz in decade steps
ACCURACY: ±1 count ±timebase error
DISPLAY: kHz, MHz
FREQUENCY C (option 030)
RANGE: 5—512 MHz direct count
RESOLUTION: 1 MHz to 0.1 Hz in decade steps
ACCURACY: ±1 count ±timebase error
DISPLAY: kHz, MHz

Period Measurements

PERIOD A (standard and option 040)
RANGE: 0—10 MHz
RESOLUTION: 100 ns to 1 s in decade steps
(10 ns to 0.1 s with opt. 040)
ACCURACY: ±1 count ±timebase error ±trigger error*
DISPLAY: ns, μs, ms, s
PERIOD AVERAGE A (standard and option 040)—the period of the signal at the A input is averaged over the number of periods, N, indicated by the resolution switch (N=1 to 10^7).
RANGE: 0—10 MHz
RESOLUTION: 100 ns to .01 ps in decade steps
(10 ns to .001 ps with opt. 040)
ACCURACY: ±1 count displayed ±timebase error ±trigger error*/N

Time Interval Measurements

TIME INTERVAL A TO B (standard and option 040)
RANGE: 100 ns—10^8 s (10 ns—10^7 s with opt. 040)
RESOLUTION: 100 ns to 1 s in decade steps
(10 ns to 0.1 s with opt. 040)
ACCURACY: ±1 count ±timebase error ±trigger error*
TIME INTERVAL AVERAGE A TO B (standard and option 040)—The time interval between a start signal at A and a stop signal at B is averaged over the number of time intervals, N, indicated by the resolution switch (N=1 to 10^7).
RANGE: 0.1 ns—10 s (0.1 ns—1 s with opt. 040)
RESOLUTION: $\pm 100\ \text{ns}/\sqrt{N} \pm 10$ ps
$\pm 10\ \text{ns}/\sqrt{N} \pm 10$ ps with opt. 040
ACCURACY: (±100 ns ±trigger error*)/$\sqrt{N}$ ±4 ns ±timebase error
(±10 ns ±trigger error*)/$\sqrt{N}$ ±2 ns ±timebase error with opt. 040.
The opt. 040 has a "jittered" clock in time interval averaging for those cases when the input is coherent with the 5328A's clock frequency.
MINIMUM PULSE WIDTH: 25 ns (10 ns with opt. 040)
MINIMUM DEAD TIME: 150 ns (40 ns with opt. 040 and maximum repetition rate of 10 MHz). "Dead time" is the time between the preceding time interval's stop event and the current time interval's start event.

*Trigger error is <0.3% of one period for sinewaves of 40 dB S/N or better and amplitude equal to sensitivity of counter. For any waveshape, trigger error is less than

$$\frac{\pm 2 \times \text{peak noise voltage}}{\text{signal slope}}$$

(or $\frac{\pm .0025\ \mu s}{\text{signal slope in V/}\mu s}$ for 40 dB S/N)

Ratio Measurements

B/A AND C/A (standard and option 040)—The ratio of the frequency at B (or C for C/A function when option 030 is installed) to the frequency at A is measured for N counts of A where N is selected by the resolution switch (N=1 to 10^7).
RANGE: A: 0—10 MHz
B: 0—100 MHz
C: 5—512 MHz
RESOLUTION: 1 part in NB/A (or NC/A)
ACCURACY: ±1 count of B (or C) ±trigger error* of A × freq. of B (or C) (N > 1)
For N = 1, add ±120 ns × freq. of B (or C)
(±12 ns × freq. of B or C with Opt. 040)

Digital Voltmeter Measurements

DVM (option 020 and 021)—Trigger levels of input channels A and B and external voltages may be measured. (Performance: 60 days at 23°C ±5°C and RH >80%)

MAXIMUM SENSITIVITY:	OPT. 020	OPT. 021
Meas. Time (N=):		
10 s (N=10^7)	1 mV	10 μV
1s (N=10^6)	1 mV	100 μV
0.1 s (N=10^5)	2 mV	1 mV
10 ms (N=10^4)	20 mV	10 mV
1 ms (N=10^3)	200 mV	100 mV
RANGE:	0 to ±125 Vdc	±10, ±100, ±1000 Vdc, and AUTORANGE
FULL RANGE DISPLAY RESOLUTION: (1s meas. time)	±0.9999, ±9.999, ±99.99, ±125.0	±12.5000, ±125.000, ±1000.00
ACCURACY: (20 min. warm-up)	±.5% reading ±4 mV	±.03% reading ±.004% range; for 1000 V range: ±.087% reading ±.004% range
TEMP. COEFFICIENT (0 to 40°C)	±.05% reading/°C ±0.5 mV/°C	±.002% reading/°C ±.001% range/°C
INPUT TERMINALS	Single ended	Floating pair
INPUT IMPEDANCE:	10 MΩ	10 MΩ
NORMAL MODE REJECTION RATIO:	>60 dB at 60 Hz (50 Hz) ±0.1%	>80 dB at 50 Hz or greater with filter on
EFFECTIVE COMMON MODE REJECTION RATIO: (1-kΩ unbalance)		dc: >120 dB ac: >120 dB for multiples of 60 Hz (50 Hz) with filter on
RESPONSE TIME: (step input)	70 ms	10 ms (filter off)
MAXIMUM INPUT	±500 V	HI to LO: ±1100 V all ranges; LO to chassis ground: ±500 V
TRIGGER LEVEL MEASUREMENTS:	2 mV display resolution	1 mV display resolution; trigger level reading automatically multiplied by setting of attenuator switch if using option 040 universal module

Totalizing and Scaling Measurements

START A (standard and option 040)—The number of counts at the A input is totalized for N=1 on the resolution switch. For N>1, A/N is totalized and the scaled output (A/N) is available at the Timebase Out rear panel connector.
RANGE: 0—100 MHz for N=1
0—10 MHz for N>1
EVENTS C, A TO B (standard and option 040)—The number of events at the C input is totalized during the synchronized time interval (i.e., a multiple of 100 ns, or 10 ns for opt. 040) defined by inputs to channel A and B.
ACCURACY: ±1 count of C ±trigger error* of A and B ±freq. of C × 120 ns
(±1 count of C ±trigger error* of A and B ±freq. of C × 12 ns with opt. 040)

Measurements with Delay (Option 040)

Delay mode is activated by inner concentric knob on LEVEL A control of option 040 Universal Module (red LED indicates delay is activated). In delay mode, Channel A triggers and is then disabled from triggering again until the delay times out (disabled state occurs within 1 μs after triggering). Channel B is continuously disabled until the delay times out. After the delay, both A and B are enabled. The delay time may be measured by placing the counter in TI A—B and the Universal Module in check (CHK).
DELAY RANGE: 20 μs to 20 ms continuously adjustable
MINIMUM DEAD TIME: 1 μs between stop and next start (T.I. average measurements only)
MEANINGFUL FUNCTIONS: FREQ A, PER A, PER AVG A, TI A—B, TI AVG A—B, RATIO C/A, START A, EVENTS C, A—B

HP-IB Interface (Option 011)

Provides digital output of measurement data ("talker") as well as input for remote program control ("listener").
PROGRAMMABLE FUNCTIONS: Function, Resolution, Sample rate (max, or manual control), Arming, Display modes, Measurement modes, Output modes, and Reset commands.
HP-IB COMMANDS: responds to the following bus commands (see HP-IB Users Guides for definitions)—Unlisten, Untalk, Local Lockout, Device Clear, Serial Poll Enable, Serial Poll Disable, Go to Local, Selected Device Clear, and Group Executive Trigger.
SERVICE REQUEST (SRQ): if enabled, indicates end of measurement.
MAXIMUM DATA OUTPUT RATE: 500 readings/second.

General

DISPLAY: 8 digit (9 with Opt. 030) LED display
BLANKING: Suppresses display of unwanted zeros to left of most significant digit
STORAGE: Holds reading between samples; can be overridden by rear panel switch.
SAMPLE RATE: Variable from less than 2 ms between measurements to HOLD which holds display indefinitely.
GATE OUTPUT: Rear panel output; TTL levels; high when counter gate open
TIMEBASE OUTPUT: Rear panel output; TTL levels
CHECK SIGNAL: With function switch in CHECK, counter should display 10 MHz ±1 count. With opt. 040, place function switch in Freq A and universal module in CHECK (CHK)—counter should display 100 MHz ±1 count.
TIMEBASE:
STANDARD CRYSTAL
AGING RATE: $<3 \times 10^{-7}$/month
TEMPERATURE: $<2.5 \times 10^{-6}$ 0° to 50°C
LINE VOLTAGE: $<1 \times 10^{-7}$ for 10% change
OPT. 010 OVEN OSCILLATOR
AGING RATE: $<5 \times 10^{-10}$/day after 24-hour warm-up
SHORT TERM: $<1 \times 10^{-10}$ rms/sec
TEMPERATURE: $<7 \times 10^{-9}$ 0° to 50°C
LINE VOLTAGE: $<\pm 5 \times 10^{-9}$ for 10% variation
WARM-UP: $<\pm 5 \times 10^{-9}$ in 20 min.
EXT. FREQ. STD. INPUT: 30 kHz to 10 MHz signal of amplitude >1.0 V rms into 1 kΩ. Maximum input: 5 V p-p. Correct reading obtained only with 10 MHz input. Other inputs give scaled readings. For opt. 040 only, the following constraints apply: ext. freq. std. must be 10 MHz for Period Avg., TI Avg., Period (N=1), and TI (N=1).
TRIGGER LIGHTS: Light is ON when input is above trigger level; OFF when input is below trigger level; BLINKING when channel is triggering. Operative over frequency range 0—100 MHz.
MARKER OUTPUTS: Inverted channel A and channel B Schmitt trigger outputs available on front panel; 0 to −100 mV levels into 50Ω; <20 ns delay. With Opt. 040, channel A Schmidt trigger and TI A—B marker outputs (0 to −50 mV) available on front panel. TI A—B is high during the time interval measured by the counter. Outputs protected from inadvertently applied voltage to ±5 Vdc.
ARM: rear panel switch turns arming ON or OFF. With arming ON, the measurement is armed by an input other than the input involved in the measurement. The following are armed by an event at B: FREQ A, PERIOD A, PERIOD AVG A, FREQ C, DVM, RATIO C/A; the following are armed by an event at C: TI A—B, TI AVG A—B, EVENTS C, A—B, RATIO B/A.
OPERATING TEMPERATURE: 0° to 50°C
POWER REQUIREMENTS: 100/120/220/240 V rms, +5%, −10% (switch selectable), 48—66 Hz; 150 VA max.
WEIGHT: Net 8.5 kg (18 lb, 12 oz).
PRICES IN U.S.A.:
5328A Universal Counter, $1,300.
Opt. 010 High Stability Time Base, $525.
Opt. 011 HP-IB Interface, $350.
Opt. 020 DVM, $200.
Opt. 021 High Performance DVM, $500.
Opt. 030 Channel C, $400.
Opt. 040 High Performance Universal Module, $350.
Optional Accessories: handles, rack mount brackets.
MANUFACTURING DIVISION: SANTA CLARA DIVISION
5301 Stevens Creek Boulevard
Santa Clara, California 95050

many others made significant contributions to the project. Dexter Hartke should be credited with first proposing the 5328A modular concept and Ken Jochim should be credited with bringing the 5328A through the investigation stage. Ian Band provided management support at critical stages in the project and along with Ken MacLeod was instrumental in product definition. Bill Kampe and Martin Neal provided invaluable marketing support. Credit for successfully transferring the 5328A into production goes to Bob LaFollette, Rich Endo, Roy Criswell, Mike Freeman, Steve Balog, Jim Carlson, and Terry Bales. Credit for service support and manuals goes to Richard Buchanan and the fastest pen in the West, Irv Simmons.

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Using a Modular Universal Counter

Here's what the various features of the new Model 5328A Universal Counter can do for the user.

by Alfred Langguth and William D. Jackson

MODEL 5328A UNIVERSAL COUNTER provides a great deal of flexibililty and measurement power in one instrument. New functions, new outputs, better performance at lower cost, system compatibility, and modularity are among its contributions. It has been engineered to give the user a new confidence in his ability to make complex measurements of time, voltage, and frequency.

Instrument-User Feedback

Setting up the measurement has always been the most difficult aspect of using a universal counter, especially adjusting trigger levels and input signal conditioning so the input amplifiers trigger at the proper points on the input waveform. Even someone very familiar with the typical instrument had to check carefully to be sure that the interval measured by the instrument was the one he hoped to measure. The 5328A makes measurement setup much more straightforward and reliable by increasing the instrument-user feedback and making more information available. Three-state trigger lights, marker outputs, and digital readout of trigger levels all serve to increase awareness of what measurement is actually being made.

The trigger lights on the 5328A have three stable states. They blink when the input amplifiers are triggering, remain off when the input signal is below the adjusted trigger level setting, and remain on when the signal is above it. This is very similar to a logic probe function, with the important exception that the threshold voltage is adjustable over a range of ±2.5 volts times the attenuator setting.

This trigger light scheme allows the user to determine the status of the input amplifiers at a glance. If the LED is off, he must lower the trigger level to find the trigger point. If the LED is on, he must raise it. If changing the level causes the LED to change state without blinking, then not enough signal is present, and either reducing the attenuator setting or increasing the signal amplitude is required. If the LED will not change state, then the dc value of the signal is outside the trigger level range, and the user must either increase the attenuation or switch to ac coupling.

The polarity of low-repetition-rate pulses can be determined by observing the trigger lights. Negative pulses cause it to blink off, while positive pulses cause it to blink on.

Another useful technique is to attach a 1-MΩ 10:1 divider probe to the input. Setting the trigger level to +0.14 volts makes the trigger light and probe a TTL logic probe, and a setting of −0.13 volts makes them an ECL probe. But there is an instrument behind this kind of probe. Unlike logic probes, these can be used to measure in-circuit propagation delays and rise times.

The A and B markers are digital outputs generated by internal Schmitt triggers. Whenever the input signal crosses the preselected threshold voltage, these outputs change state. They operate over the full 100-MHz frequency range of the input amplifiers and change state within twenty nanoseconds of a triggerable event. By displaying these markers and the input signal on an oscilloscope, the trigger points typically can be monitored to within a few nanoseconds and a few millivolts of their actual values. Problems involving false triggering now become simple to solve, as shown in Fig. 1.

The high-performance universal module replaces the B marker with one labeled TI A—B OUTPUT. This is the measured time interval. It can also be superimposed upon the input signal on an oscilloscope.

Another advantage of these markers is their usefulness as a trigger source. Since the input amplifiers have better than 25-mV sensitivity and generate fast-rise-time outputs, the marker outputs can be used to

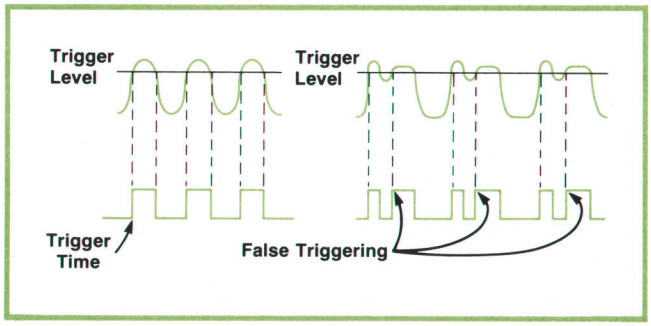


Fig. 1. *Marker outputs show when the input amplifiers are triggering. Trigger levels can be monitored with an oscilloscope by displaying the input signal and the marker. Markers can also show false triggering, and can be used to synchronize other instruments.*

synchronize oscilloscopes or other equipment when the input signal itself is not suitable.

Now suppose that an integrating DVM is installed in the 5328A. Besides measuring externally applied voltages, these modules can also read and display the internal trigger levels for the A and B input channels. This direct readout ability makes trigger level selection and adjustment very easy.

READ LEVEL in combination with the three-state trigger light can also be used to measure the peak-to-peak voltage of signals within the common mode range of the input. This is done by placing the counter in READ LEVEL, measuring both points where the trigger light stops blinking, and taking the difference between these two points.

Bus Structure Adds Power

The modular structure of the 5328A would not be so useful without a flexible and complete means for the individual modules to communicate with the instrument mainframe. For this purpose, a parallel two-way information bus was established between all modules and the mainframe (see Fig. 2, page 5). Capable of providing everything from power supplies to important gating, display, and status signals, this ninety-line bus allows complete two-way communication not only between module and mainframe, but among modules as well. Any module, or the HP-IB interface, can use the bus to take independent control of display, function, or time base.

This convenient means of information exchange and control, combined with a mainframe capable of accepting signals from several modules simultaneously, makes the 5328A capable of making new measurements that were omitted from previous instruments because the cost of the extra circuits to implement them would not have been justified. This extra performance includes new functions, complete arming capability, and a very powerful yet simple to use HP-IB interface.

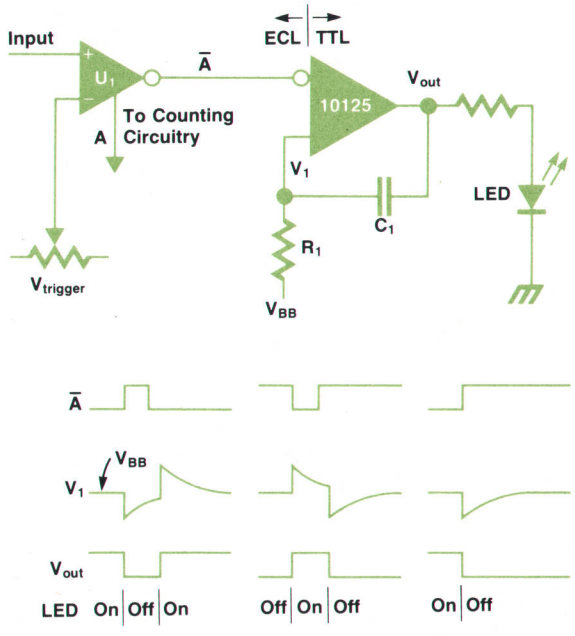
New Functions

Two new ratio measurements, C/A and B/A, are available. They offer the full bandwidth, sensitivity, and frequency capabilities of the A, B, and C input amplifiers.

It is also possible to totalize the channel C input during the synchronized time interval defined by TI A—B. This same time interval can be used as the integration time for the DVM, a feature that is useful for

Three-State Trigger Lights

The three-state trigger lights use an ECL-to-TTL translator in a simple but interesting feedback configuration. When the input signal is higher than the trigger voltage, $\bar{A}$ is an ECL low level; when the input is below the trigger voltage, $\bar{A}$ is an ECL high. For quiescent signals, V_1 is at V_{BB}, the ECL threshold voltage, and V_{out} is a TTL signal of polarity opposite that of $\bar{A}$. When $\bar{A}$ changes state, causing V_{out} to change, C_1 forces V_1 to follow it and then decay exponentially toward V_{BB} with time constant $\tau = 1/R_1C_1$. For example, let $\bar{A}$ go from high to low. V_{out} then goes to a TTL high, turning on the trigger light and forcing V_1 to some voltage between V_{BB} and V_{out}. Until V_1 decays to below the ECL high level, $\bar{A}$ will have no further effect and the trigger light will remain on. If $\bar{A}$ stays low, V_1 will reach V_{BB}, but will still be higher than $\bar{A}$ and the LED will stay on. If $\bar{A}$ has returned high, then when V_1 crosses the ECL high level, V_{out} will switch to a TTL low, turning off the LED and forcing V_1 downwards. Similar but opposite waveforms occur for $\bar{A}$ changing from low to high. Hence, a pulse of either polarity as short as two or three nanoseconds is inverted and stretched to greater than 20 milliseconds, long enough for the human eye to see. For signals whose frequency is higher than the blinking rate, the circuit reaches a steady-state condition where the pulse duty cycle is 50% and the LED blinks at a visible rate.



applying a scale factor to voltage measurements.

Of course, all of the standard universal counter functions are offered, including Frequency A, Period A, Period Average A, TI A—B, TI Average A—B, Totalize A, Totalize Clock, Check, Frequency C, and DVM.

Arming

In the armed mode, an input channel that is normally not used in a particular measurement can be used as a trigger source to give independent control of the time a measurement is to begin. This mode is activated by setting the rear-panel NORMAL/ARM switch to the ARM position.

As can be seen in Fig. 2, only two measurements are armed in the normal operating mode: Frequency A and Frequency C. All other measurements are free running ("armed by the sample rate"). In the armed mode, the measurement is generally armed by an amplifier not used in the measurement. Channel B was chosen whenever possible.

Another means of arming the counter is the LINH (Low Inhibit) input on the rear panel. Grounding this input will inhibit arming. For arming any measurement that is free running, the LINH input need be opened only momentarily (about 1 μs) for arming to occur. For measurements armed from amplifier channels A, B, or C, LINH must be high when that channel is triggered for arming to occur.

Function	Normally Armed By	In Armed Mode Armed by Event in Channel
Frequency A	A	B
Period A	Sample Rate	B
Period Average A	Sample Rate	B
Ratio B/A	Sample Rate	C
Time Interval A—B	Sample Rate	C
TI Average A—B	Sample Rate	C
C, TI A—B	Sample Rate	C
Ratio C/A	C	B
Frequency C	C	B
DVM	Sample Rate	B
Start A	Measurement Controlled by Function Switch	
Start Clock	Measurement Controlled by Function Switch	
DVM, TI A—B	Sample Rate	C
DVM/A	Sample Rate	B

Fig. 2. *Normally measurements are initiated when the first desired signal enters the counter, or by the sample rate circuits. In the armed mode, the measurement begins only after an event occurs in the arming channel.*

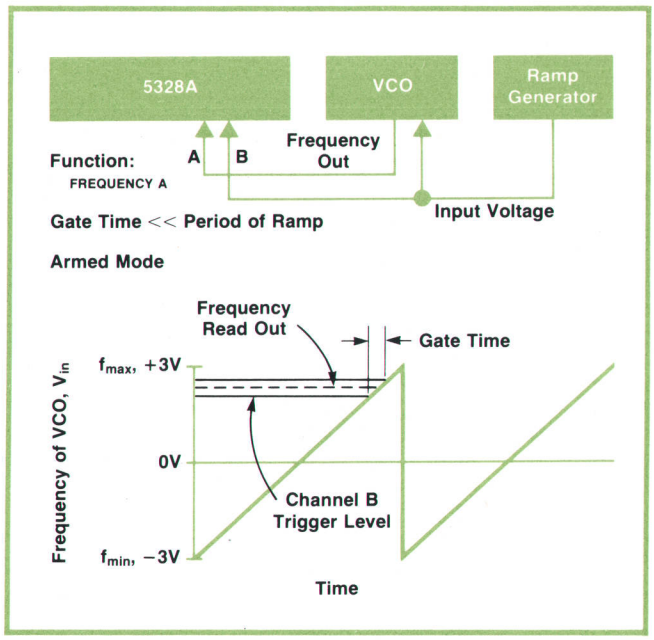


Fig. 3. *In the armed mode the counter can be used to check the output frequency of a voltage-controlled oscillator as a function of its input voltage.*

The counter can also be armed, and the NORMAL/ARM switch programmed, via the HP-IB interface.

Many interesting applications can be devised for the arming system. One is shown in Fig. 3. Here a ramp voltage is applied to a voltage-controlled oscillator and to channel B of the 5328A. The VCO frequency output is applied to channel A. The counter is then put into FREQ A, ARM, with a gate time that is a small fraction of the ramp period. The trigger level voltage of Channel B can then be varied, and the counter will display the VCO output frequency as a function of the input voltage given by trigger level B.

For doing armed TI measurements without a C channel, the LINH input is available. Placing the ARM/NORMAL switch in NORMAL, and pulsing the LINH input high will cause the counter to arm. With channel C, an arming signal may be applied to channel C with the switch in the ARM position.

An example of a more complex armed measurement is shown in Fig. 4. Here a signal composed of bursts of two different frequencies is connected to channel A. An arming signal is put into channel B to trigger the counter whenever a burst of the desired frequency comes along, thereby causing the counter to measure only that frequency. The LINH input is also used to control the triggering, so that only selected arming signals in channel B will be effective. This can be useful for measuring frequency-shift-keyed signals.

Universal Modules

The standard universal module is capable of

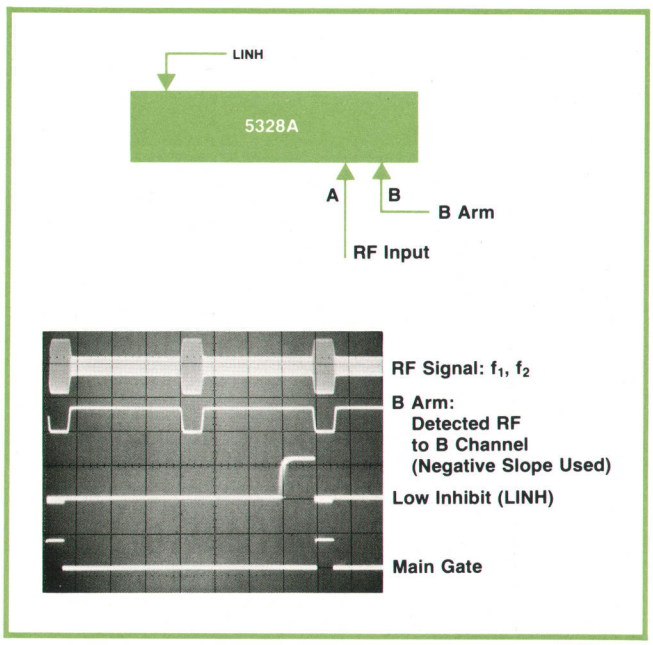


Fig. 4. *The counter can be armed by two inputs simultaneously to make more complex measurements. Here the arming channel is channel B, but the* LINH *input must be high when channel B is triggered for arming to occur.*

100-ns resolution for single-shot time intervals while the high-performance version multiplies the 10-MHz mainframe oscillator up to 100 MHz and can therefore resolve 10 ns in single time intervals. In TI average, the high-performance unit introduces a random phase jitter into its clock to prevent lockup on intervals occurring at rates synchronous with harmonics of the instrument clock.[1] Since resolution in this mode increases as $\sqrt{N}$, where N is the number of time intervals averaged,[1] the ten-nanosecond module will converge to a given resolution 100 times faster than the standard 100-ns module.

The input amplifiers of both universal modules have greater than 150-MHz bandwidth and 25-mV basic sensitivity over a ±2.5-volt common mode range. Because ECL logic levels are nominally from −800 mV to −1600 mV, the sensitivity and trigger level range in ×1 attenuation are adequate to measure propagation delays and rise times of these devices. Caution is advisable when making such measurements, however. Even though both modules are fully capable of making repeatable average measurements with resolution much less than a nanosecond, the basic absolute accuracy is only specified to be within ±4 ns for the standard module and ±2 ns for the high-performance version. This means that each instrument must be individually calibrated against some standard and its absolute measurement error subtracted from the displayed time interval if absolute accuracy better than the instrument specification is required. The specified accuracy is adequate for measuring such logic families as TTL and MOS directly. The ×2 attenuator setting of the high-performance module creates a ±5-volt trigger level range with 50-mV sensitivity and optimizes the amplifiers to measure 5-volt logic families.

In the READ LEVEL function, the high-performance module multiplies the actual trigger level by 1 or 2, depending on the attenuator setting, before it goes to the DVM. Thus the DVM reads the actual trigger point including the effects of input attenuation. A 50Ω/1-MΩ switch is provided in the high-performance module to optimize impedance matching at the amplifier inputs: 50Ω for fast signals in a 50Ω environment, 1 MΩ for reduced circuit loading or use with oscilloscope probes. Hysteresis compensation for time interval measurements allows more accurate determination of trigger points.[2] This causes the amplifier to trigger typically within 5 mV of the selected trigger level.

Delay

Measurements with delay are also possible with the high-performance universal module. This feature causes the counter to ignore unwanted signals that would normally trigger the input amplifiers and make a particular measurement impossible. When a non-zero delay is selected, once channel A triggers, it is prevented from triggering again until after the selected delay. Channel B is continuously disabled until after the delay. The delay is adjustable from 20 μs to 20 ms by means of a front-panel control. It can be measured by placing the counter in TI A—B and the universal module in check.

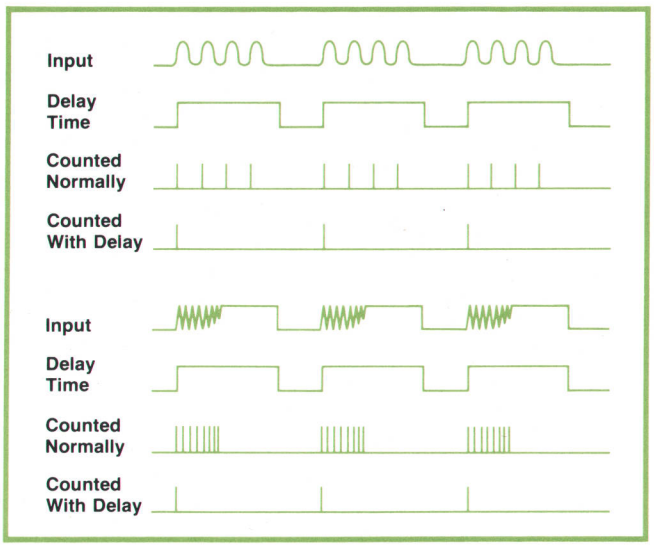


Fig. 5. *High-performance universal module has a variable delay feature. In time interval measurements, delay causes the counter to ignore stop events until the delay times out. Delay can also be used in frequency, period, ratio, and totalize measurements to inhibit triggering on unwanted triggerable events.*

HP-IB Option Fits Simple or Sophisticated Systems Applications

Mounted inside the 5328A mainframe, the optional HP-IB module makes the counter compatible with the HP Interface Bus.[1,2] The counter's display reading can be read out onto the HP-IB and most of the front-panel and rear-panel mainframe controls can be programmed by commands on the HP-IB.

Programmable controls include all positions of the FUNCTION and TIME BASE switches, the sample rate, and the NORMAL/ARM switch. The counter can be commanded to make a single measurement or self-trigger continuously.

Programs consist of strings of alphanumeric characters coded according to the American Standard Code for Information Interchange (ASCII). The counter's repertoire includes 43 commands, each consisting of one or two characters. The P command sets up standard initial conditions and must come first in the ASCII string. R, reset, or T, reset and trigger, should come last. Other commands can be in any order.

Data output is very flexible. The counter can be programmed to wait until its current measurement has been read out before self-triggering for another measurement, or to self-trigger without waiting. Normally, data output occurs at the end of a measurement, but the counter can be programmed to read out the contents of its display anytime it is addressed, regardless of whether a measurement is in progress (readout on the fly). Another command disables display storage; combined with readout on the fly, this makes it possible to read out the current information in the decade counting assembly at any time, regardless of the state of the measurement.

Still another command disables the reset signal to the decade counting assembly. This causes the results of a series of measurements to be added together, a useful feature for averaging.

```
10    CMD "?U9", "PF4G5T", "?Y5"
20    INPUT (13,*) D
30    END
```

Fig. 1. *A 9830A Calculator program to measure a frequency in channel A of the 5328A Counter. Counter and calculator are interconnected by the HP Interface Bus.*

Simple or Sophisticated

In most applications the counter will be told simply to take a reading and output the results. Very little knowledge of the counter's repertoire is required to write this kind of program. Fig. 1 shows an example of a 9830A Calculator program to measure a frequency in channel A. In the command sequence, P sets up standard initial conditions (maximum sample rate, arming off, storage on, and so on). F4 sets the function to Frequency A. G5 sets the gate time multiplier at 10^5 (10-Hz resolution), and T initiates a single reading. Notice that the user can simply ignore programming features such as storage off, disable decade reset, arming on, readout on the fly, and so on, because the P command turns them all off.

The 5328A lends itself to rather sophisticated applications

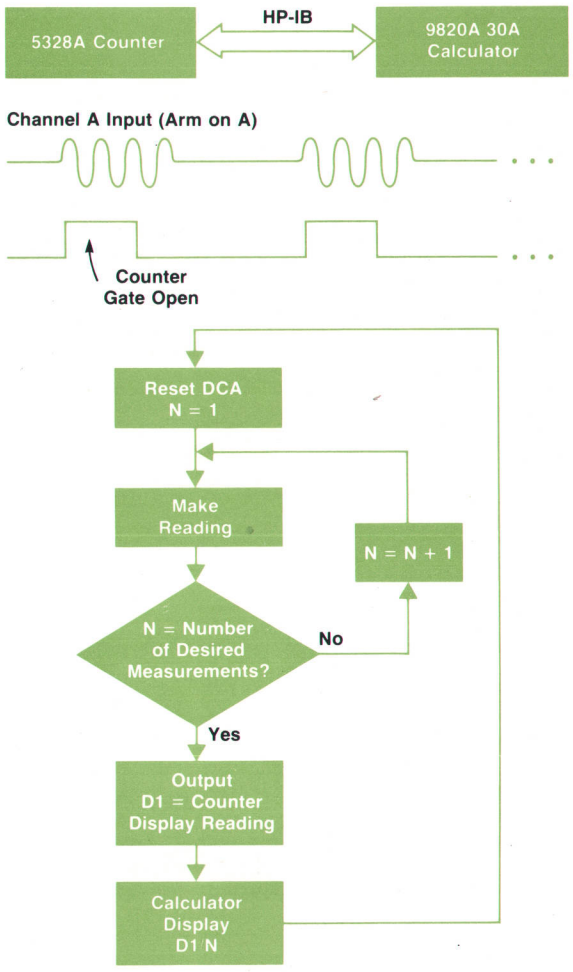


Fig. 2. *Measurement averaging using a 5328A Counter and a 9830A or 9820A Calculator.*

when necessary. As an example, consider the problem in measurement averaging shown in Fig. 2. A series of measurements may be taken with the decade counting assembly reset disabled, causing all of the measurement values to be accumulated in the decade counting assembly. When the desired number of readings have been taken, the result can be read out and divided by the number of readings to obtain the average. Although each individual measurement could be read out and accumulated externally, the method shown here, using internal accumulation, can be nearly an order of magnitude faster.

References

1. D.W. Ricci and G.E. Nelson, "Standard instrument interface simplifies system design," Electronics, November 14, 1974.
2. Hewlett-Packard Journal, January 1975.

Many measurements that would not otherwise be possible can be made using this feature. Time intervals from a start event to one of many stop events can be made by adjusting the delay to ignore intervening stop events until the correct one occurs (see Fig. 5). Frequency measurements of signals containing

noise that would normally cause extra trigger events can be made by setting the delay to disable the input during that part of the waveform where the noise normally occurs. Contact bounce in electromechanical relays and other unwanted inputs can thus be prevented from introducing error into a measurement.

Frequency C Module

512-MHz direct counting capability is provided by the channel C module even though the mainframe circuitry can only count 100 MHz. In the Frequency C function, the gate on the mainframe counting assembly is held open and a second gate in the C module is enabled by the main gate bus line. A high-speed decade in the module is inserted into the decade counting chain without prescaling. After a measurement is completed, circuits in the module use display information from the bus to strobe the least significant digit onto the display along with the mainframe display (see Fig. 2, page 5).

DVM

The integrating DVM options interface to the mainframe by converting the input voltage to a frequency at 10 kHz/volt. In the READ LEVEL function, these modules also use the bus lines to disable the mainframe function and time base and force the mainframe to make a DVM measurement.

In the armed mode, DVM measurements are initiated only when channel B triggers. This ability to control a measurement externally is especially useful for measuring dc levels that vary with time, such as in digital-to-analog converters.

The high-performance DVM combined with the HP-IB interface makes remote controlled voltage measurements extremely simple. It has a floating input with internal optical isolators to translate its output to chassis ground so it outputs directly onto the module bus like any other module. The front panel for the DVM is not programmable, but an autoranging scheme has been designed with systems applications in mind. It automatically selects the proper attenuator range for any input signal, yet always maintains the same output format. As higher attenuation levels are chosen, the least significant digits that become invalid are blanked from the display. Hence, any voltage from 10μV to 1000V is measurable. READ LEVEL is not programmable.

HP-IB Module

The HP-IB module makes the 5328A compatible with the Hewlett-Packard Interface Bus (see box, page 13). The counter can serve both as a talker and a listener. The simplest configuration consists of the 5328A connected to an HP-IB printer, such as the HP 5150A. Only one cable is required. All measurements made by the counter are printed for a permanent record.

The full power of the HP-IB interface is realized by including the counter in a system that has a controller, such as an HP 9830A Calculator. In such a system, the counter can operate in an interactive mode as an universal counter, timer, and DVM.

Acknowledgments

The 5328A would never have existed without the creative ideas and hard work of the rest of the design team: Mike Wilson, Ian Brown, and Karl Blankenship. Thanks to Dee Norman who put the 2000 holes in our motherboard, and to Ken MacLeod, Gary Sasaki, Ken Jochim, Bill Kampe, Ian Band and many others for their inputs. Finally, a special word of appreciation to Jim Horner. As project leader, he kept us working closely together toward precise goals, but in an atmosphere encouraging personal creativity.

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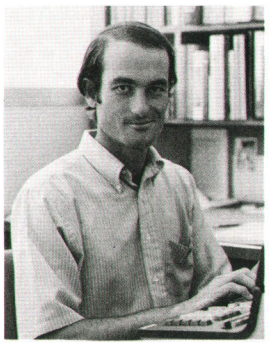
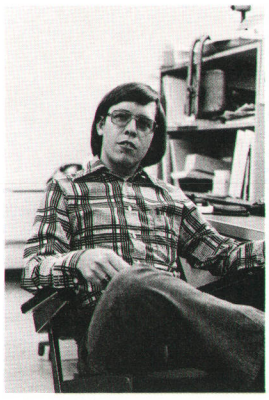
2. K.J. Jochim and R. Schmidhauser, "Timer/Counter/DVM: A Synergistic Prodigy?," Hewlett-Packard Journal, April 1970.



William D. Jackson

Bill Jackson designed the HP interface bus option for the 5328A Universal Counter. He's been with HP since 1970 and had previously designed a remote programming interface for the 5326/27 Counters. Bill was born in Tuscon, Arizona, graduating in 1970 with a BSEE degree. He's single, likes to play tennis and listen to music, and is an official of the HP Santa Clara Division basketball league. He lives in San Jose.



Alfred Langguth

Al Langguth designed the two universal modules and the channel C module and contributed to the overall system design of the 5328A Universal Counter. With HP since 1971, he's also done design work on the 5327 Counter series. Originally from Blythe, California, Al received his BSEE degree from Massachusetts Institute of Technology in 1970 and his MSEE from Stanford University in 1971. Last year, he and his wife moved to Los Altos, California, where Al now spends much of his time adding a new garage and woodworking shop to their home. He's also interested in photography and enjoys outdoor activities like biking, camping, and exercising his dog.

Synthesized Signal Generator Operation to 2.6 GHz with Wideband Phase Modulation

New plug-ins give the Model 8660-series Synthesized Signal Generators programmable operation to 2.6 GHz and a capability for phase modulation.

by James A. Hall and Young Dae Kim

INCREASING USE OF THE 2-GHz bands for long-haul communications and for satellite tracking and telemetry, coupled with the growth of navigational systems, radio astronomy and meteorology in the 1 to 2 GHz band, has intensified the need for precision test instrumentation for this range of frequencies. At the same time there is increasing use of phase modulation (ϕM) in communications, telemetry, and navigation systems, so phase-modulated signal generators are needed for testing these systems.

These needs have led to the development of new plug-in sections for the Hewlett-Packard 8660-series Synthesized Signal Generators: a 1-MHz-to-2.6-GHz RF section, and modulation sections with the capability for wideband phase modulation. (Fig. 1).

First introduced in mid-1971, the 8660-series Synthesized Signal Generators combine the frequency resolution, stability, and programmability of a synthesizer with the output level calibration and AM/FM capability of a signal generator.[1,2] The new Model 86603A RF Section plug-in increases the frequency range, providing synthesized frequencies from 1 MHz to 2.6 GHz in 1-Hz steps up to 1.3 GHz, and 2-Hz steps up to 2.6 GHz. The output level is calibrated and adjustable over a range of more than 140 dB, from at least +7 dBm down to −136 dBm (0.5 V to

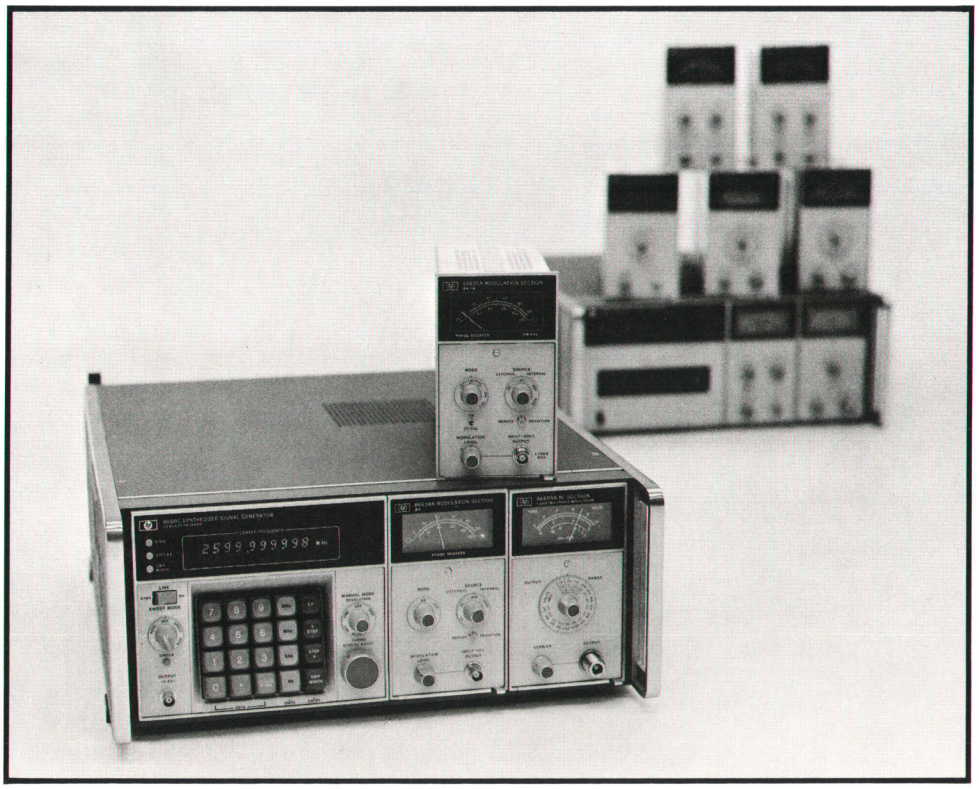


Fig. 1. *The 8660-series Synthesized Signal Generator family has three new plug-ins and a new mainframe. The new RF Section plug-in gives frequency coverage to 2.6 GHz and the other two plug-ins are modulation sections that add phase modulation capability. The new mainframe and plug-ins are compatible with previously announced plug-ins and mainframes (background).*

0.03 μV rms).

Phase modulation capability (ϕM) is provided by two new modulation section plug-ins, the Models 86634A and 86635A, operating in conjunction with the RF section. Model 86635A provides both FM and ϕM capability with maximum modulation rates of 1 MHz in either mode. Model 86634A is a phase-modulation-only plug-in that provides wideband modulation rates with good linearity from dc to 10 MHz. Peak ϕM deviation of either plug-in is metered and adjustable up to $\pm 100°$ for center frequencies up to 1.3 GHz, and $\pm 200°$ for center frequencies between 1.3 and 2.6 GHz. This capability, coupled with the >140 dB calibrated output range, makes the synthesized signal generators useful for testing a wide variety of phase-modulated systems, and for lab-bench applications such as examining the behavior of phase-lock loops.

The previously announced modulation sections in the 8660 series may also be used with the new 2.6-GHz RF section to give AM, FM, and pulse modulation, in addition to the new phase modulation capability. Programmability of frequency, output level and modulation via either BCD or the HP Interface Bus also makes the new 2.6-GHz capability available for computer or calculator controlled test systems.

Operation to 2.6 GHz

The 2.6-GHz frequency range is obtained in the new Model 86603A RF Section with the help of a frequency doubler. A block diagram is shown in Fig. 2. Basic operation for output frequencies below 1300 MHz is identical to the earlier Model 86602A 1 - 1300 MHz RF Section:[3] two microwave signals, one that is varied in 100-MHz steps and one that is varied in 1-Hz steps, are supplied by the synthesizer mainframe; these are heterodyned to derive a difference frequency that is routed through an ALC detector and an attenuator to become the output signal. The microwave signal that varies in 1-Hz steps has a range of 3.95 to 4.05 GHz, and the 100-MHz-step signal ranges from 2.75 to 3.95 GHz, giving a maximum difference frequency of 1.3 GHz.

To obtain frequencies above 1.3 GHz, the difference frequency is routed via a relay to the frequency doubler. The doubler consists of a transmission-line balun that produces two signals 180° out of phase, balanced with respect to ground. The signals drive a full-wave Schottky-diode rectifier resulting in a rectified sine wave that has a strong component at twice the input frequency. The input fundamental and odd harmonics are suppressed by the circuit's symmetry.

The double-frequency signal is processed through a bandpass filter that further suppresses the input fundamental and the third and higher harmonics. The filter, however, has a wide enough passband (500 MHz) to allow wideband modulation sidebands to pass with minimum distortion. The filter is tuned to track the output frequency by a varactor under control of digital signals originating in the mainframe digital control unit (DCU).

Following the filter, the signal is amplified by two identical amplifiers in cascade to bring it up to the desired level. It was possible to use inexpensive

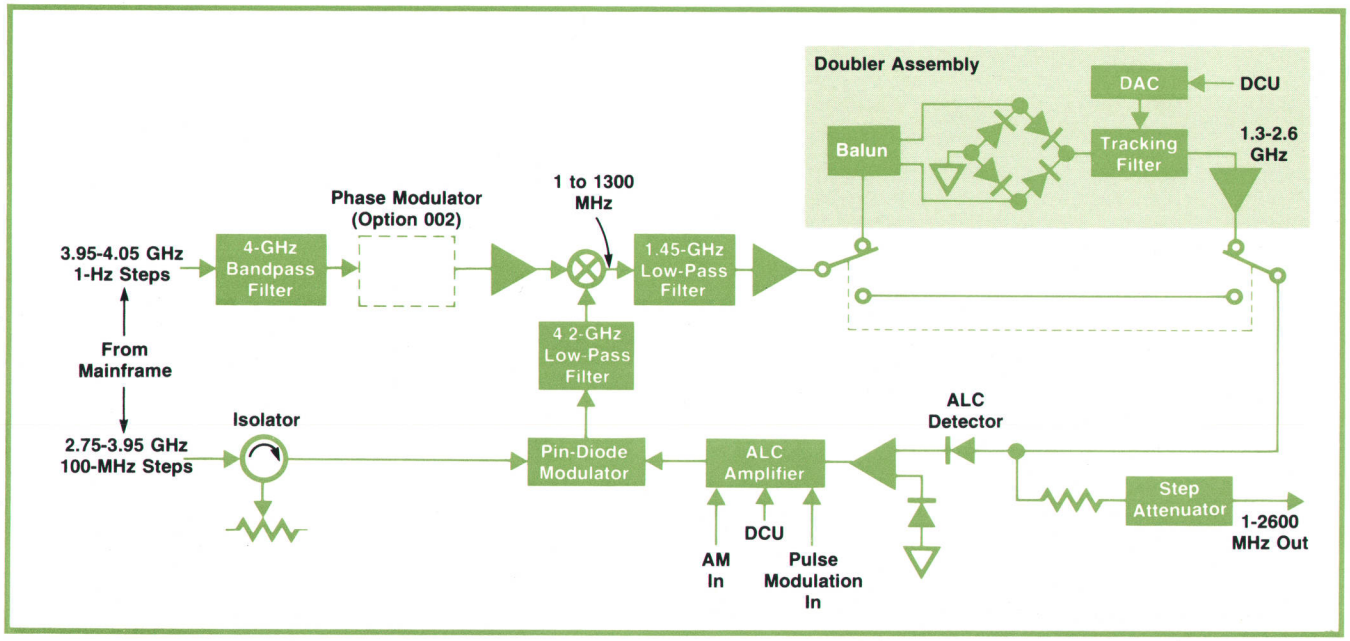


Fig. 2. *Block diagram of the Model 86603A 2.6-GHz RF Section. Microwave signals supplied by the mainframe give difference frequencies over a range of 1-1300 MHz in 1-Hz steps. The frequency doubler extends the output range to 2600 MHz.*

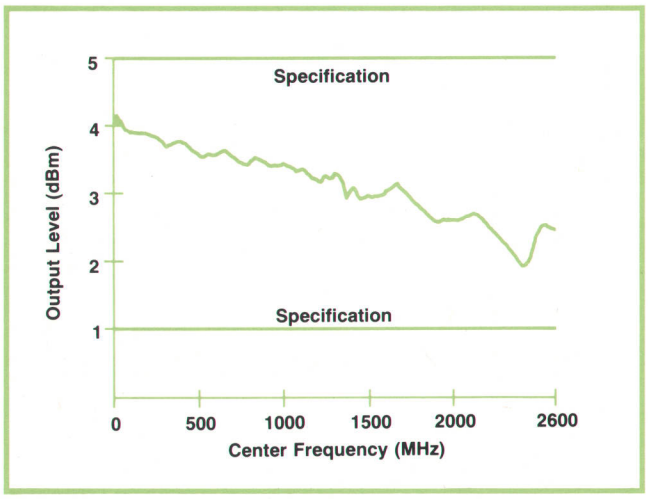


Fig. 3. *Output level as a function of frequency for a typical Model 86603A RF Section at an output level of +3 dBm.*

printed-circuit microstrip techniques for these amplifiers because they need to work only over an octave bandwidth and the discrete transistors used have more than enough gain in this frequency range. Each amplifier uses two HP type 35821E transistors in a common-emitter configuration and has approximately 12-dB gain over the 1.3-to-2.6-GHz range.

The amplified signal goes to the output attenuator. It is also detected, amplified, and routed back to a PIN-diode modulator in the signal path of one of the input microwave signals to give closed-loop control of the output amplitude, thus compensating for the frequency response of the system. The output flatness achieved is shown in Fig. 3.

Because the output frequency is double that derived from the microwave signals provided by the mainframe, a new mainframe (Model 8660C) has been designed using a modified digital control unit to give direct selection and display of the output frequency throughout the full 1-2600-MHz range. This mainframe operates identically to the Model 8660B at output frequencies below 1300 MHz, but when used with the Model 86603A 2.6-GHz RF Section, it automatically switches in the RF section's doubler when a frequency above 1300 MHz is selected and computes the two microwave frequencies needed to supply one-half the output frequency to the doubler. As far as the operator is concerned, the Model 8660C operates the same whether the output is below 1300 MHz, above 1300 MHz, or when stepping, sweeping, or tuning through 1300 MHz. Frequency resolution above 1300 MHz, however, is 2 Hz rather than 1 Hz because of the frequency doubling.

For use in the earlier 8660A and 8660B mainframes, an optional version of the 2.6-GHz RF section (opt 003) is available.* This version has a front-panel switch for inserting the doubler in the signal path (the switch may also be activated by remote control). With the doubler in, the output frequency is twice that indicated by the mainframe.

Phase Modulator Operation

Equipping an 8660-series generator for phase modulation requires one of the two ϕM modulation sections and an RF section equipped with the phase-modulator factory-installed option (opt 002). Either Model 86602B (1-1300 MHz) or Model 86603A (1-2600 MHz) may be supplied with this option. The actual phase modulation takes place in the RF section while the modulation section supplies the internally-generated modulating signals, establishes the modulation level for either internal or external signals, and meters the peak deviation.

As was indicated in Fig. 2, the phase modulator is in the signal path of the 3.95-4.05 GHz microwave input signal in the RF section. The modulator is a four-port circulator with varactor-diode phase shifters at two of the ports (Fig. 4). Each diode is biased at an operating point that causes the diode capacitance to

*Older mainframes with serial number prefix 1349A and lower need a field update kit that insures proper thermal conditions and power supply regulation to avoid possible damage to the new RF section. Details are available at HP field offices.

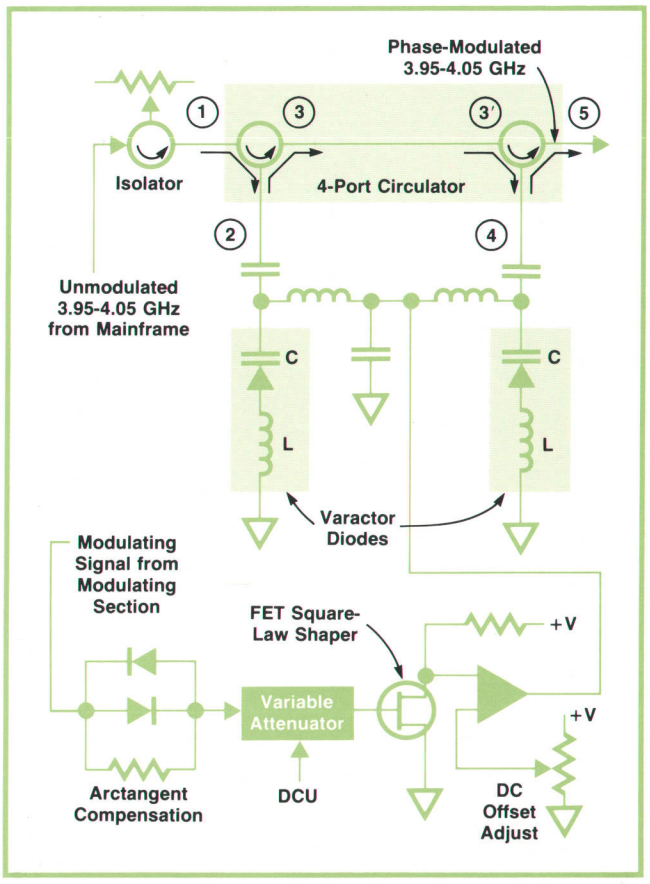


Fig. 4. *Phase modulator is inserted in the path of one of the microwave signals in either the 86602A 1.3-GHz or the 86603A 2.6-GHz RF Sections.*

Phase Modulation

What is Phase Modulation?

Phase modulation (ϕM) is a form of angular modulation in which the phase of a carrier wave is varied in proportion to the instantaneous amplitude of the modulating signal. To characterize the amount of ϕM on a carrier wave, a modulation index, m, is defined:

$$m = \Delta\phi_{peak}$$

where $\Delta\phi_{peak}$ = peak phase deviation of the carrier in radians. There is a direct relationship between modulation index and the resultant carrier and sideband levels, as shown for the carrier and first through third sidebands in Fig. A. Note that with no phase deviation (m = 0) the carrier level is unity and the sideband levels are zero. As the deviation is increased, the carrier level decreases and the sideband levels increase. The sidebands are spaced at a frequency interval equal to the modulation frequency.

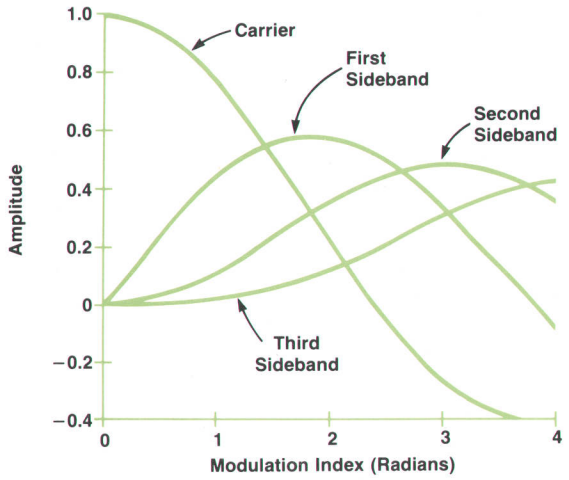


Fig. A

How is Phase Modulation Like Frequency Modulation?

In frequency modulation (FM), a more familiar type of angular modulation, the frequency of a carrier wave is varied in proportion to the instantaneous amplitude of the modulating signal. Because frequency is the time derivative of phase, ϕM and FM are directly related. The equivalent modulation index, m, for FM is:

$$m = \frac{\Delta f}{f_m}$$

where Δf = peak frequency deviation in Hz and f_m is the modulation frequency. With sinusoidal modulation, ϕM and FM with the same modulation index have exactly the same RF spectrum. This is illustrated by a comparison of Figs. B1 and B3.

How Does Phase Modulation Differ from Frequency Modulation?

In ϕM the modulation index depends only on the amplitude of the modulating signal and is independent of the modulation frequency. Therefore, as the modulation frequency is varied, the sideband levels in ϕM remain constant and only the frequency spacing varies. This is illustrated by Figs. B1 and B2. Contrasted with this, the modulation index in FM depends on both the frequency deviation, determined by modulating signal amplitude, and the modulating frequency. For constant frequency deviation, the modulation index varies inversely with modulation frequency. This is illustrated by comparing Figs. B3 and B4.

Looking at this another way, the amount of frequency deviation generated by phase modulating a carrier varies directly with the modulating frequency. For this reason large frequency deviations can be generated using high-rate ϕM.

The relationship between FM and ϕM is important in understanding the errors that can result in measurements involving a mixture of FM and ϕM equipment. For example, when using an FM signal generator to test a ϕM receiver, the receiver demodulated output drops 6 dB per octave as the modulating frequency increases. This must be accounted for when measur-

be series-resonant with its own lead inductance at 4 GHz.

The capacitance C of the abrupt-junction diodes varies approximately as $1/\sqrt{V}$, where V is the bias voltage:

$$C \approx K/\sqrt{V}$$

where K is a constant. Neglecting the loss in the varactor circuit, the reactance X of the series-tuned circuit as seen by the circulator is:

$$X = \omega_o L - \frac{1}{\omega_o C} \approx \omega_o L - \frac{\sqrt{V}}{K\omega_o}$$

Therefore, for a given RF frequency ω_o, the reactance X of the series-tuned circuit varies approximately as the square root of the voltage that biases the diode.

Again neglecting the loss in the varactor circuit, a voltage wave incident on the varactor circuit is reflected with a phase shift ϕ:

$$\phi = -2 \arctan (X/Z_o),$$

where X is the varactor circuit reactance and Z_o is the characteristic impedance of the transmission-line circuit. From this it can be seen that as X varies from $-\infty$ to $+\infty$, ϕ varies $\pm\pi$ radians ($\pm 180°$).

The non-reciprocal characteristic of the ferrite circulator separates the reflected wave from the wave incident on the varactor circuit. The signal applied to port 1 is coupled to port 2. The part reflected from port 2, which is phase-shifted according to the varactor reactance, is coupled to port 3. Using two circulators in series with their varactor circuits driven in parallel gives a theoretical phase-modulation range of $\pm 360°$. However, by restricting the range to $\pm 100°$, good modulation linearity is assured.

The phase-modulator driver circuit uses the square-law response of a FET to compensate for the square-root relationship between the reactance X and the varactor voltage V. A diode-resistor circuit gives a non-linear attenuation that compensates for the arctangent relationship between the reactance X

ing modulation frequency response or when considering the FM generator's contribution to overall harmonic distortion. Also, care must be exercised to ensure that the maximum allowable phase deviation of the ϕM receiver is not exceeded at low modulation frequencies.

When modulating with non-sinusoidal waveforms (square wave, triangular wave, etc.), the task of simulating ϕM with an FM generator is more difficult. This is because these more complex waveforms contain harmonic frequencies that must produce the proper amount of deviation with respect to the fundamental.

These difficulties can be overcome to some extent by passing the modulating signal through a differentiator to give a 6 dB per octave rise in amplitude as the modulation frequency increases (pre-emphasis), thus maintaining a constant modulation index. The limitations of this approach are discussed in the main text.

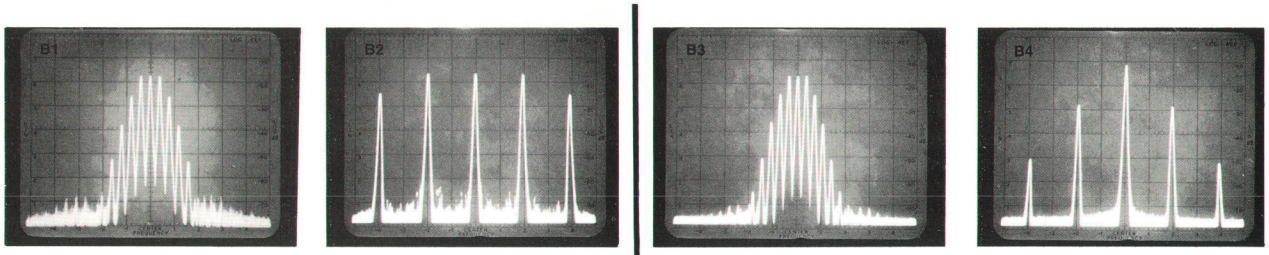
A Second Difference

With FM, the instantaneous carrier frequency varies directly with the modulating signal amplitude and the maximum and minimum carrier frequencies occur at the positive and negative peaks of a sinusoidal modulating waveform. In ϕM the instantaneous frequency varies as the time derivative of phase so the maximum and minimum carrier frequencies occur at the zero crossings of the sinusoid where the waveform rate of change is highest.

This 90° phase difference is only important when considering secondary effects such as how incidental AM generated in an FM or ϕM modulator affects the output RF spectrum. It has little practical significance when using ϕM to simulate FM or vice versa.

Why ϕM

With the many similarities that exist between ϕM and FM, why use phase modulation? One important reason is that phase modulation can be applied directly to a carrier signal and does not require modulation of the carrier oscillator as in FM. For this reason, ϕM is often used in systems where a highly stable carrier frequency is required, as in narrowband communications and telemetry systems. In digital communications systems, phase shift keying (phase modulation with discrete phase states) is often used because a stable carrier frequency at the source eases the problem of carrier recovery at the receiver, and in many applications it offers better spectral efficiency (more bits per Hz of RF bandwidth) than frequency-shift keying (FM with discrete frequency states).



Rate = 20 kHz
Index = 1.45

100 kHz
1.45

ϕM; Deviation = 83° (Peak)

Rate = 20 kHz
Index = 1.45

100 kHz
0.29

FM; Deviation = 29 kHz (Peak)

and phase shift ϕ.

Although the tuned varactor circuit would theoretically allow optimum modulation linearity to be achieved at only one microwave frequency, good phase linearity for all the RF section's output frequencies is obtained because the input microwave frequency varies only ±1.25% (3.95 - 4.05 GHz). Phase modulation distortion is typically less than 2% at modulation rates up to 1 MHz and typically is less than 5% at 10 MHz. The system can actually be driven through a range of ±115° with very little loss of linearity. This range is doubled to ±230° in the Model 86603A RF section at carrier frequencies above 1.3 GHz where the frequency doubler is used.

The sensitivity of the modulator varies by about 5% as the microwave frequency varies from 3.95 to 4.05 GHz. This is compensated for by a variable attenuator that is controlled digitally by the mainframe.

Modulator incidental AM is typically less than 10%. This relatively low AM and the low distortion are preserved by the use of wideband circuits following the modulator.

An alternative approach to phase modulation would have been to use an FM modulator with the frequency response of the modulator shaped so its output would simulate phase modulation (see box). A problem arises, however, because the frequency deviation then varies as a function of the modulation frequency. At high modulation frequencies, very wide deviations are required, placing a practical limit on the upper modulation frequency. At low modulation frequencies, very low deviations result and a lower limit is imposed by residual FM noise. At best, these two extremes encompass a frequency range of three or four octaves.

No such limits exist with the phase-modulation scheme used in the 8660 system. A modulating frequency range of dc to 10 MHz is thus possible.

Acknowledgments

Our acknowledgment and thanks to Hamilton

Chisholm for the design of the digital control unit in the 8660C mainframe, to Skip Crilly for the design of the 86634A Modulation Section, to Charlie Sallberg for the design of the 86635A Modulation Section and also for environmental testing of the new mainframe and modulation and RF section plug-ins, to Charles Cook for the plug-in product design, to John Hasen for his guidance of the modulation section design and his investigation of phase modulation characterization, and especially to Section Manager Brian Unter for his guidance and counsel throughout the project and for his many contributions to product definition.

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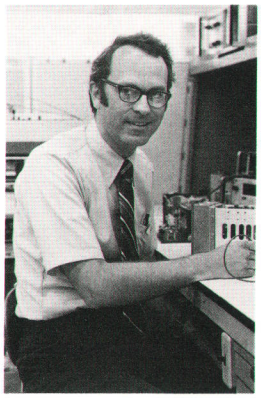
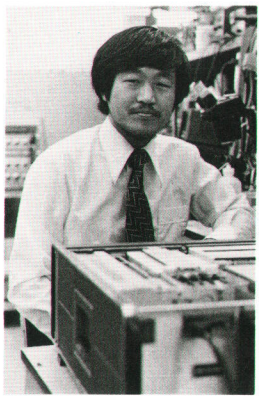
3. R. Hassun, M. Humphreys, D. Scherer, Y.D. Kim, B. Stribling, C. Cook, "Synthesized Signal Generation to 1.3 GHz," Hewlett-Packard Journal, March 1973.



James A. Hall

With 13 years experience in microwave communications, Jim Hall joined HP in 1972 to work on a prototype satellite TV receiver (HPJ Aug. 74). When that was completed, he was named project manager for the 8660 system. Born in Halifax, Virginia, Jim has a BSEE from North Carolina State University and an MS in Physics from Lynchburg College (Va.). With a daughter, 8, and a son, 5, Jim's major leisure-time activities have become family camping and fishing.



Young Dae Kim

A graduate of Seoul National University (BSEE), Young Dae Kim worked as a microwave engineer in Korea before obtaining a scholarship that led to an MSEE degree at South Dakota State University. He joined HP in 1969 and is doing further graduate work at Stanford in the HP Honors Co-op program. Kim worked on the 11661A Frequency Extension Module before becoming project engineer for the 86603A RF Section. Kim's married, and he enjoys table tennis and oriental checkers.

ABRIDGED SPECIFICATIONS

8660C Synthesized Signal Generator Mainframe

FREQUENCY SELECTION: keyboard control panel allows selection of CW (or center frequency) by entry keys or synthesized tuning dial. Least significant digit: 1 Hz.
REFERENCE OSCILLATOR:
INTERNAL: 10-MHz quartz oscillator. Aging rate less than ±3 parts in 10^8 per 24 hours.
EXTERNAL: Rear-panel switch allows operation from 5- or 10-MHz signal.
REFERENCE OUTPUT: Rear-panel BNC connector provides 0.5 to 1 Vrms (INT) into 170 ohms or voltage nominally equal to external input (EXT).
DISPLAY: Ten-digit numerical LED display of CW frequency is active in either local or remote mode. Spring-loaded pushbuttons switch to display of sweep width, selected step size, or characters being entered on keyboard.
SYNTHESIZED SEARCH: synthesized search dial changes synthesized output frequency 180 steps per revolution. Step sizes are 1 Hz, 1 kHz, 1 MHz, or any step size entered through keyboard (2 Hz minimum above 1300 MHz).
DIGITAL SWEEP:
TYPE: symmetrical about CW/center frequency. Sweep width is divided into 100 synthesized steps for fastest sweep speed or 1000 steps for slower speeds or Manual Sweep.
SWEEP WIDTH: continuously adjustable over range of RF section installed.
SWEEP END POINT ACCURACY: same as reference oscillator accuracy.
SWEEP SPEED: selectable 0.1 s, 1 s, or 50 s per sweep (Auto or Single).
SWEEP OUTPUT: 0 to +8 V stepped ramp.
MANUAL SWEEP: synthesized search dial allows manual sweep over width selected in 1000 steps (LED display follows output frequency during manual sweep).
SINGLE SWEEP: initiated by momentary contact pushbutton.
FREQUENCY STEPPING: after step size has been entered on keyboard, depressing STEP↑ or STEP↓ key increments frequency up or down by desired step size.

Remote Programming

FUNCTIONS: CW frequency, frequency stepping (STEP↑, STEP↓), and output level, and most modulation functions are programmable. Note: digital sweep is not programmable.
FREQUENCY: CW frequency is programmable over entire range with same resolution obtained in manual operation.
FREQUENCY STEP: STEP↑ or STEP↓ may also be programmed to change output frequency by previously selected step size.
OUTPUT LEVEL: programmable in 1-dB steps over output range of RF section installed.
PROGRAMMING INPUT:
CONNECTOR TYPE: 36-pin Cinch type 57 (optional HP-IB interface; 24-pin Cinch type 57).
LOGIC: TTL compatible (negative true).
INTERNAL FAN-IN FROM PROGRAMMING CONNECTOR: 10; (required current approximately 15 mA per line in the "1" state).

General

LEAKAGE: Meets radiated and conducted limits of MIL I-6181D.
POWER: 100, 120, 220, or 240 volts +5%, −10%, 48-66 Hz. Approximately 350 watts.
WEIGHT: (Mainframe only): net, 23.8 kg (53 lbs).
DIMENSIONS: 425 mm W × 176 mm H × 599 mm D (16.75 × 6.94 × 23.63 inches).

Model 86603A RF Section

(Requires 11661B Frequency Extension Module in mainframe)
FREQUENCY RANGE: 1-2600 MHz (2599.999 998 MHz).

	CF <1300 MHz	CF ≥1300 MHz
FREQUENCY RESOLUTION:	1 Hz	2 Hz
HARMONICS:	<−30 dB (Slightly higher above +3 dBm)	<−20 dB
SPURIOUS:	−70 dB	−64 dB
SIGNAL-TO-PHASE-NOISE RATIO (for CW, AM, and ϕM):	>45 dB	>39 dB
SIGNAL-TO-AM-NOISE RATIO	>65 dB	>65 dB

OUTPUT LEVEL (into 50Ω): 1-1300 MHz, +10 to −136 dBm; 1300-2600 MHz, +7 to −136 dBm.
OUTPUT ACCURACY: ±2.5 dB to −76 dBm, ±3.5 dBm to −136 dBm. Specifications slightly degraded above 1.3 GHz for output levels >+3 dBm.
FLATNESS: <±2.0 dB at output meter readings between −6 and +3 dB.
IMPEDANCE: 50Ω
VSWR: <2.0 on +10 and 0 dBm ranges; <1.3 on −10 dBm range and below.
OUTPUT LEVEL SWITCHING TIME: <50 ms (<5 ms for any change on same attenuator range).

	CF <1300 MHz	CF ≥1300 MHz
AMPLITUDE MODULATION:		
MODULATION DEPTH (at output levels ≥3 dBm):	0 to 90%	0 to 50%
3-dB BANDWIDTH (at 0-30% AM and CF ≥ 10 MHz):	100 kHz	5 kHz
DISTORTION (at 30% AM):	<1%	<5%
INCIDENTAL ϕM (at 30% AM):	<0.2 radians	<0.4
INCIDENTAL FM (at 30% AM):	$0.2 \times f_{mod}$	$0.4 \times f_{mod}$
FREQUENCY MODULATION:		
RATE	dc to 200 kHz	dc to 200 kHz
MAXIMUM PEAK DEVIATION	200 kHz	400 kHz
INCIDENTAL AM (75 kHz peak deviation at 1 kHz rate):	<−60 dB	<−60 dB
FM DISTORTION:	<1%	<1%
PULSE MODULATION:		
RISE-FALL TIME	50 ns	50 ns
ON/OFF RATIO	>40 dB	>60 dB
PHASE MODULATION:		
RATE	dc to 10 MHz	dc to 10 MHz
MAXIMUM PEAK DEVIATION	0 to 100°	0 to 200°
ϕM DISTORTION (at 1 MHz rate):	<5%	<5%

WEIGHT: 5 kg (11 lbs); 11661B Frequency Extension Module (required) adds 1.8 kg (4 lbs) to mainframe.

Model 86634A Modulation Section

(Requires RF Section with option 002)
ϕM RATE: dc −10 MHz
MODULATING SIGNAL: External or internal
INPUT LEVEL REQUIRED OF EXTERNAL SOURCE: 2 Vrms max
INPUT IMPEDANCE: 50Ω
INTERNAL SOURCE: 400 Hz and 1 kHz, ±5%
METER: 0-100° peak ϕM; 0-200° for CF ≥1.3 GHz.
REMOTE PROGRAMMING: External ϕM only.
WEIGHT: 1.8 kg (4 lbs)

Model 86635A Modulation Section

(Requires RF Section with option 002)
FM AND ϕM RATE: dc −1 MHz
MODULATING SIGNAL: (Same as for Model 86634A above except input impedance = 600Ω).
METER: 0-10, 100, 1000 kHz FM, 0-100° ϕM; for CF ≥1.3 GHz, 0-20, 200, 2000 kHz FM, 0-200° ϕM.
FM CENTER FREQUENCY LONG-TERM STABILITY: Typically less than 200 Hz/hr. Drift can be removed by pressing FM CF CAL button, which phase-locks FM oscillator momentarily to mainframe reference.
REMOTE PROGRAMMING:
FUNCTIONS: Int/Ext ϕM or FM. Also FM CF CAL.
MODULATION SETTING RESOLUTION: 1/50 of range selected.
WEIGHT: 2.6 kg (6 lbs)
PRICES IN U.S.A.:

Minimum keyboard-controlled 2.6-GHz System		Minimum CW ϕM System	
8660C Mainframe	$7,900	8660A Mainframe	$6,200
86631B Auxiliary Section	$300	86634A ϕM Modulation Section	$1,400
11661B Frequency Extension Module	$3,000	11661B Frequency Extension Module	$3,000
86603A 2.6-GHz RF Section	$6,000	86602B 1.3 GHz RF Section	$4,100
		Option 002 (ϕM capability)	$1,500
Total	$17,200		$16,200

Model 86635A ϕM/FM Modulation Section: $2,200
Model 86603A (opt 003) 2.6 GHz RF Section for use with 8660A/8660B mainframe: $6250
MANUFACTURING DIVISION: STANFORD PARK DIVISION
1501 Page Mill Road
Palo Alto, California, 94304

Applications of a Phase-Modulated Signal Generator

Once a capability is made available, applications emerge. Here are a few that have been found for the phase-modulated synthesized signal generator in HP's own laboratories.

by James A. Hall

AS THE NUMBER OF APPLICATIONS for phase-lock loops (PLLs) grows, more and more engineers are faced with the need to evaluate the performance of these devices. FM signal generators can be used for this purpose but there are several advantages to using a synthesized signal generator with phase modulation (ϕM) capability. For example, a synthesizer's output is locked to a crystal reference that is accessible to external circuits so all the oscillators in a complicated measurement set-up can be locked to a common reference.

A phase-modulated synthesizer permits a measurement of frequency response to be swept while maintaining constant phase deviation. This avoids the excessive phase deviation at low modulation frequencies and the loss of signal-to-noise ratio at high frequencies that would occur with FM. For measurements of PLL transient response, phase modulation is a necessity.

Fig. 1 shows a basic PLL measurement system. By measuring the PLL error voltage, the closed-loop error as a function of input phase deviation and as a function of slew rate can be determined. From these measurements, loop bandwidth and dynamic range can be inferred.

Closed-loop gain can be measured by using a spectrum analyzer to examine the output of the PLL's voltage-controlled oscillator. Closed-loop gain is easily determined by taking advantage of the fact that with ϕM the modulation index remains constant as the modulation frequency varies. At a modulation index of less than 0.5 (30° peak deviation), the first-order sidebands of a phase-modulated wave can be considered proportional to the modulation index* and the higher sidebands are of insignificant proportions. By noting the VCO sideband level as a function of modulation frequency, one has a measure of the PLL closed-loop response. Loop bandwidth and peaking can be measured readily with this technique.

*The ratio of the first sideband amplitude to carrier amplitude equals approximately one-half the modulation index.

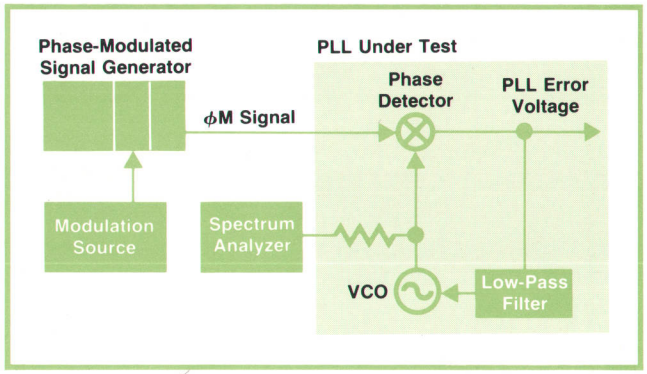


Fig. 1. *System for measuring a phase lock loop's closed-loop gain and error.*

These measurements give results in terms of magnitude only. By using a network analyzer to measure phase response as well as magnitude, one obtains the complete closed-loop transfer function. For this test, the output of the PLL VCO must be demodulated in a phase detector.

One set-up for doing this is diagrammed in Fig. 2. Synthesized signal generator #2 serves as a stable local oscillator for the phase detector. By using a variable dc source at the phase modulator input, the output phase of the signal generator can be offset to operate the phase detector in the center of its linear range. Gain-phase measurements are then made in the usual way.

At high modulation rates, the excess phase contribution of synthesized signal generator #1 must be considered. Typical excess phase shift of the 86602A/86603A RF Section operated with the 86634A or 86635A Modulation Section is shown as a function of frequency in Fig. 3. Note that the excess phase shift is a linear function of frequency and may therefore be considered as a constant time delay, equivalent to a length of lossless transmission line.

The method of generating a local-oscillator signal shown in Fig. 2 is only one of several possible. With it, however, measurements are possible at modula-

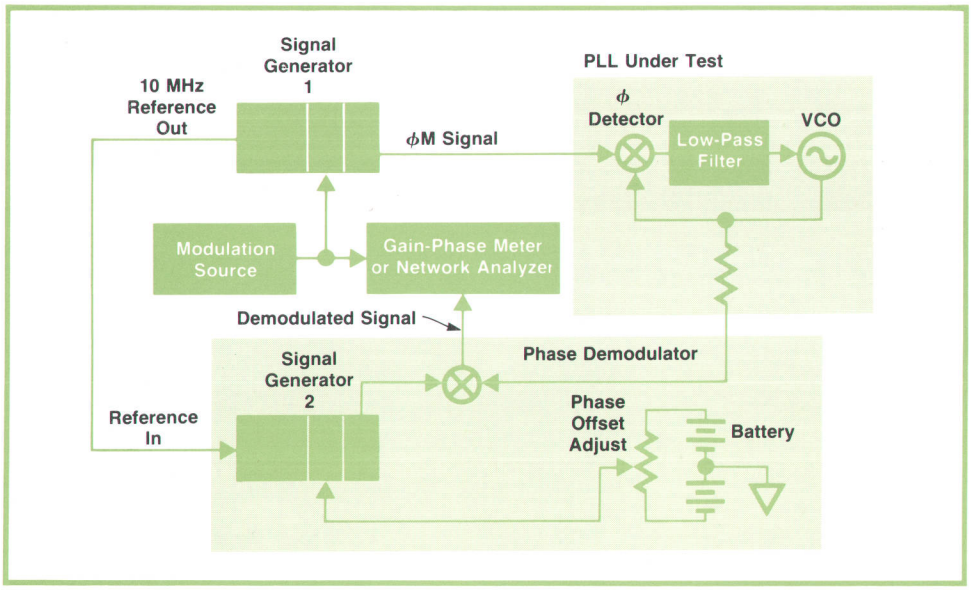


Fig. 2. *Measuring the closed-loop transfer function of a phase lock loop.*

tion rates down to dc, unlike systems that use a phase-lock loop to recover the carrier for use as an LO signal. The set-up of Fig. 2 also allows measurements in systems where the input RF frequency differs from the VCO frequency, for example where frequency dividers are included in the loop.

The transient response of the PLL can be measured by observing the phase demodulator output with an oscilloscope while driving the modulation input of signal generator #1 with a square wave or pulse train.

Phase Detector Characterization

Phase detector circuits can be difficult to evaluate for linearity and sensitivity and for changes in these characteristics with changes in frequency or input level. This is particularly true of some of the new all-digital phase-frequency detectors.

One quick method of evaluating a digital phase detector is shown in Fig. 4. The "÷N" block is one means of getting a reference frequency within the range of the phase detector under test. Another synthesized signal generator could be used in place of a frequency divider as was done in Fig. 2.

The response of a widely-used digital phase-frequency detector obtained by the set-up of Fig. 4 at two different frequencies is shown in Fig. 5.

Digital Phase Modulation

The fact that the phase-modulation technique used in the 8660 system is an analog method does not preclude its use as a digital phase modulator when evaluating various digital phase-modulation schemes or formats.

Biphase modulation is obtained by driving the synthesized signal generator's modulation section with a square wave. If the square wave is symmetrical with respect to ground (no dc offset) and the modulation meter reads 90° peak deviation, the modulation will be ±90°. This results in a 180° difference between the two phase states.

Adding the output of two digital generators to obtain a four-level modulation signal results in a quadriphase PCM signal. If phase states of 0°, 90°, 180°,

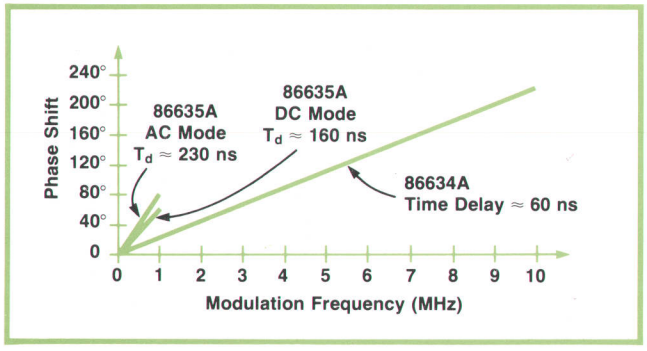


Fig. 3. *Excess phase shift of the 8660-series modulation system measured between the modulation section input and the RF section output.*

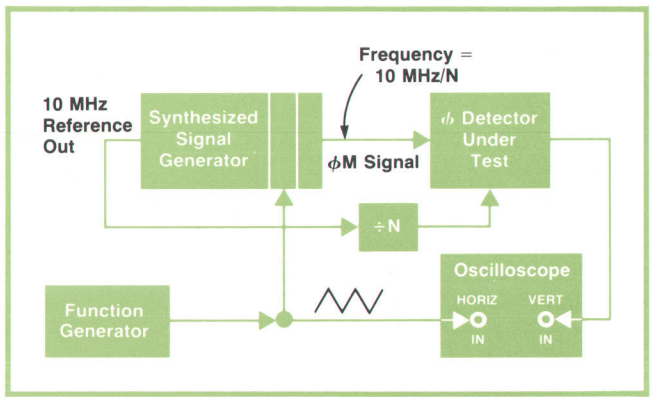


Fig. 4. *Set-up for measuring phase detector characteristics.*

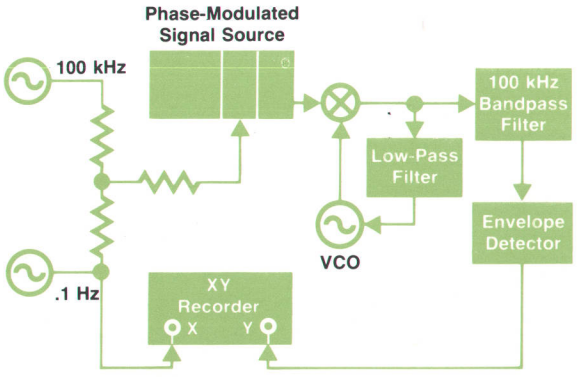
Measuring Modulation Linearity

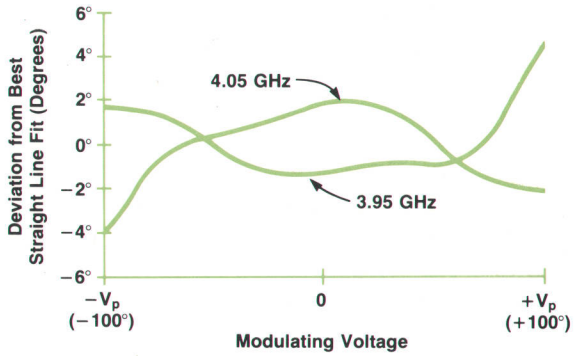
The distortion in the output of a phase modulator can be expressed in a number of ways. For the 8660 system, it is specified in terms of total harmonic distortion in the demodulated output signal. This is measured with a very linear wideband phase demodulator.

For some applications, linearity in terms of deviation from a best straight line is more meaningful. This can be determined by measuring the derivative (incremental slope) of the modulator's phase-vs-voltage characteristic, a technique that has been used for many years in testing FM communications systems.* The derivative of the linear part of the characteristic is a dc term, second-order curvature results in a slope, and so on. By numerically integrating the derivative, an accurate plot of phase change versus voltage is obtained. This method has an advantage in that a perfect demodulator is not required for the measurement.

A system for measuring the incremental slope is shown in the diagram. Two modulating signals are applied simultaneously to the phase modulator under test. One is a very low frequency signal (~0.1 Hz) with sufficient amplitude to give full-scale modulation, in this case ±100°. The other is a low-level, high-frequency tone (>50 kHz) that gives about 2° deviation. This signal varies the input voltage by a small amount ΔV while the low-frequency signal moves the ΔV variation over the complete input range of the modulator, and hence over the modulator's complete characteristic.

The modulated output of the unit under test is demodulated by a narrow-bandwidth phase-lock loop. The VCO of the phase-lock loop tracks the low-frequency phase variations quite closely, maintaining a very low error output. This means that the phase detector operates at essentially the same point on its characteristic at all times and thus does not contribute any nonlinearity to the measurement.





The high-frequency tone, being outside the bandwidth of the phase-lock loop, appears superimposed on the error voltage with an amplitude proportional to the slope of the modulator's phase-versus-voltage characteristic. It is amplitude detected and then applied to the Y axis of an X-Y recorder. The X axis is driven by the low-frequency modulating signal. The resulting plot is a graph of modulation sensitivity versus input voltage or, putting it another way, the derivative of phase change versus input voltage.

By integrating this curve numerically, an accurate plot of phase change versus voltage input is derived. If the dc component of the modulation sensitivity curve is ignored, then the constant-slope term in the modulation characteristic drops out. The resulting curve is a plot of deviation from best straight line. A plot typical of a Model 86603A RF section's modulator at minimum and maximum modulator carrier frequencies is shown above.

*R. Urquhart, "A New Microwave Link Analyzer with High-Frequency Test Tones," Hewlett-Packard Journal, September 1972.

and 270° are desired, the modulator is driven ±135°. This is well within the capabilities of the 8660 system at RF frequencies above 1.3 GHz and can typically be obtained at lower frequencies by overdriving the system to ±135°.

The capabilities of the 8660 system make it unnecessary to build VHF, UHF, or microwave digital phase modulators from scratch when evaluating digital phase modulation schemes. The problem is reduced to building the necessary baseband waveform generators.

Waveform Synthesis

In designing circuits and systems, it is often necessary to evaluate the effects of harmonic distortion on performance. For this, a test signal with known and controllable distortion is useful. This can be done with the set-up shown in Fig. 6.

The two synthesized signal generators are locked to a common reference frequency and their outputs are summed in a resistive adder. By using a controllable dc voltage to vary the phase of the $2f_o$ generator, and by varying its output with the level control, a signal is obtained that has a second harmonic variable in amplitude and phase. An analysis of the effect of second harmonic distortion on the circuit under test can then be made. For example, the effect of second

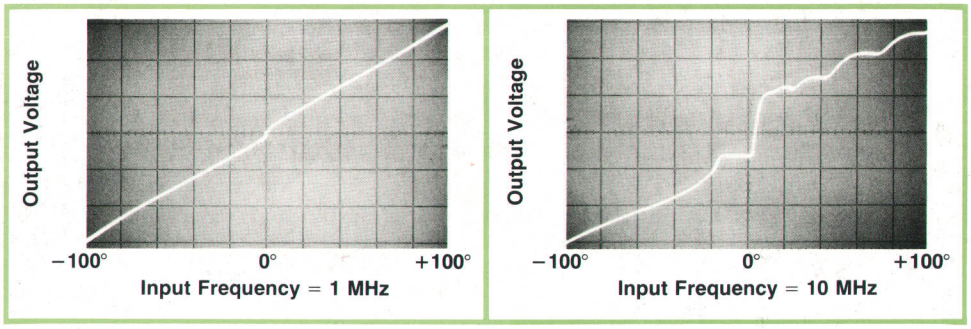


Fig. 5. *Effect of frequency on the performance of a digital phase-frequency detector, using the set-up of Fig. 4 for the measurement.*

harmonic distortion on the RF spectrum of an FM signal is readily made with this method.

Microwave Frequencies

There are many times when it would be desirable to use the frequency setability and modulation capabilities of the 8660 system for conducting tests at frequencies well above 2.6 GHz. These can be obtained by upconverting the 8660 output using a mixer with a microwave signal generator serving as the local oscillator.

Because the 8660 system makes available a wide range of high frequencies, it is possible to select mixer input frequencies that space undesired mixing products far away from the desired output frequency. The filtering problem is therefore greatly simplified and may even be non-existent because of the passband of the following circuits.

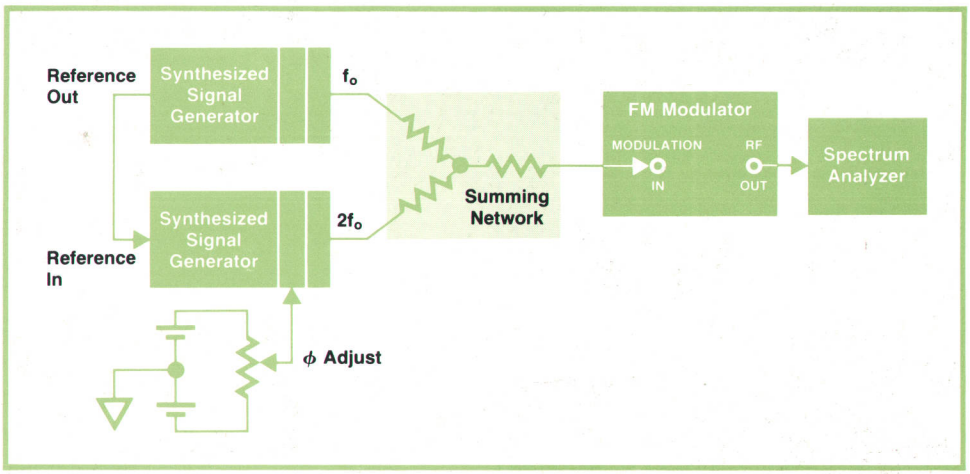


Fig. 6. *Using two phase-locked signal generators to synthesize a signal with controllable second-harmonic distortion.*

Hewlett-Packard Company, 1501 Page Mill Road, Palo Alto, California 94304

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Technical Information from the Laboratories of Hewlett-Packard Company

Hewlett-Packard S.A., CH-1217 Meyrin 2 Geneva, Switzerland
Yokogawa-Hewlett-Packard Ltd., Shibuya-Ku Tokyo 151 Japan

Editorial Director • Howard L. Roberts
Managing Editor • Richard P. Dolan
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