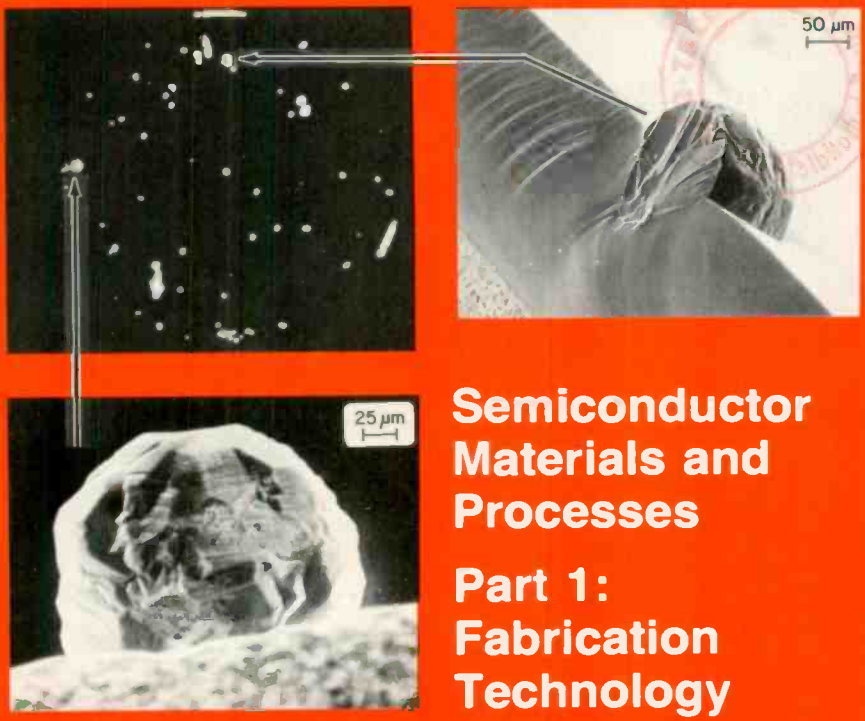
RCA Review

Optical Scan for Defects



Semiconductor Materials and Processes

Part 1: Fabrication Technology

March 1983 Volume 44 No. 1

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Our cover shows a laser scanner map of bumps and defects on an epitaxially grown film. The scanning electron micrographs shown to the right and below are of slices through two of the larger defects. The photo on the right shows a growth that started at the original substrate, but that continued at a faster speed than its environment; that below is a crystallite of silicon, probably due to nucleation initiated by a particulate (possibly silicon dust). The figure is taken from the paper, "Optical Scanner for Dust and Defect Detection," by Steigmeier and Auderset.

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Semiconductor Materials and Processes

Part 1—Fabrication Technology

Contents

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Introduction

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There is a very strong temptation in writing an introduction such as this to call to the reader's attention the remarkable revolution in solid state electronics that has occurred over the past decade. Such prose has often been written during the past two decades. Each time such words were written they were true, and they are still true; the worlds of optoelectronics and microelectronics continue to excite, stimulate, and amaze all of us who have had the good fortune to be associated with them.

Our introduction begins more soberly by noting that first and foremost the papers that comprise this two-part issue of the *RCA Review* (Part 2 will appear in the June 1983 issue) are technical research reports written by specialists in their fields and are intended to reach their prime audience—other specialists.

It has been our pleasure, as guest editors, to interpret the subject of Semiconductor Materials and Processes in its broadest sense. Epitaxial growth, etching, lithography, ion implantation, and measurement technologies are highlighted along with papers on materials and devices. It was difficult to find a logical, two-part division of the papers. Roughly, the papers in Part 1 (this issue) cover fabrication technology and devices. The papers in Part 2 (June 1983) concentrate on the preparation and properties of materials.

In choosing from the papers submitted, we have expressed our own fascination with the range of subjects and disciplines studied by RCA researchers. For example, you might expect that the science of optics needs to be mastered in the course of research in lithography. It is not surprising, also, to read of measurement methods for dust and defects that depend upon skilled application of optical techniques. An unexpected application of optical methods, however, appears in the paper describing techniques to characterize polycrystalline silicon. On the other hand, almost perversely, the two

papers that deal with diode lasers are less concerned with optics than with chemistry and electronics.

To further demonstrate the unexpected applications of these various disciplines, we have chosen as illustrations of products drawn from this research papers on power transistors and solar cells. In the world of remarkable revolutions in microelectronics and optoelectronics, these "less glamorous" devices are shown to require as great an understanding of the interactions among materials and processes as is required for integrated circuits.

Optical Scanner for Dust and Defect Detection

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Abstract—An automatic wafer and mask inspection system of high sensitivity and uniform sensitivity across the wafer is presented. The results of extended testing give a detailed account of the system's performance in different fields of application (IC technology, solar cells, thin films, and others).

1. Introduction

The semiconductor device technology imposes severe conditions on processing standards in terms of absence of defects in starting materials and cleanliness during processing. In many cases particle contamination and defects contribute considerably to the low yields experienced in large-scale integrated circuits. The situation becomes even more crucial as circuits are reduced to micron and submicron dimensions. Thus there is a need for establishing an objective quality level that goes beyond subjective judging under bright-light illumination.

Several different laser scanning instruments have been proposed for automatic inspection of wafers.[1–3] When this program started, we felt the need to build an improved instrument that (1) provides a visual defect and dust pattern display and (2) eliminates the flying spot mirror-deflection scanning with its drawback of varying scattered-light pickup geometry across the wafer and the resultant sensitivity limitations. These requirements were met with the instrument described in this paper. Since June 1977, several of these scanners have been operating successfully at different locations within RCA, and a U.S. patent[4] was issued on Feb. 9, 1982. The instrument, produced by Fluorocarbon,[5] is commercially available. Other instruments have also been developed, partly using similar principles, but predominantly with the flying spot scanning method.[6]

The present instrument is designed for sampling needs in a factory and is not intended for on-line use. For this reason there are no provisions for cassette-to-cassette wafer loading, although it appears possible to incorporate this feature if desired. It was felt that high-standard cleanliness conditions and freeness from defects can easily be maintained by sampling rather than by feeding the full production line through an additional processing step, which might provide additional risk and cost. And so, we aimed for extremely high sensitivity. Further, our scanner method permits the study of patterned wafers in the early processing stages, a function not provided for by other methods. In another mode of operation, the present scanner can be used for thin-film quality assessment and material acceptability check. Due to its simplicity the present instrument can be produced at low costs. In fact, its commercial version[5] is among the lowest priced of such instruments on the market today.

2. Description

The experimental arrangement of the laser scanning system is shown in Fig. 1. The wafer or thin-film device to be tested is illuminated

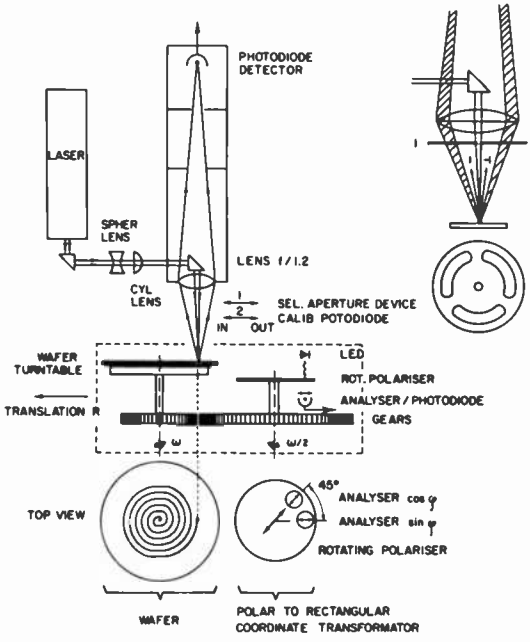

Fig. 1—Measuring arrangement.

with low-power laser light (red version: 4 mW HeNe 6328 Å; blue version: 15 mW HeCd 4416 Å; ultraviolet version: 4 mW HeCd 3250 Å). The laser beam is focused by three consecutive lenses (one of which is a cylindrical lens) into a spot of elliptical shape about 50 μm × 230 μm on the wafer. This minimum spot size is imposed by the diffraction limit in the tangential direction and the pitch of the spiral scan in the radial direction. The scattered light is collected in a coaxial arrangement by a large aperture camera lens f/1.2, passed through a spatial filter, and detected by a high-speed photodiode. Thus, the specularly reflected light is prevented from reaching the detector by a beam stop (represented by the prism mount). The wafer rests on a turntable, held down by vacuum. Scanning of the wafer is performed by translating the rotating turntable with respect to the beam. Thus, the light spot describes a spiral path on the wafer with a pitch of 200 μm. With the present system, round wafers of 1- to 5-inch diameter or square chrome masks of 2 to 4 inches can be scanned. Minor mechanical changes would permit an extension, e.g., to 6-inch round and 5-inch square.

For displaying the spatial pattern of scattered light on a storage scope, we make use of polar-to-rectangular coordinate transformation. The turntable of frequency ω is geared to a second one of frequency $\omega/2$ which consists of a polarizer rotating between a light-emitting diode and a fixed analyzer/photodiode arrangement. Two of these analyzer/photodiode arrangements, displaced by 45 degrees in polarization, provide a signal which (apart from a dc shift) is proportional to cos φ and sin φ, respectively, of the rotation angle φ on the wafer turntable. This follows from the function of multiple angles if the light intensity passing through a rotating polarizer and a fixed analyzer is given by $I_0 \times \cos^2(\varphi/2)$. Multiplication of cos φ and sin φ by the translation of the whole turntable system, given by the resistance R of a multiturn potentiometer proportional to the translation, provides the coordinate transformation $x = R \times \cos\varphi$, and $y = R \times \sin\varphi$.

Fig. 1 shows further that this instrument can be used on patterned wafers. The more or less regular (or periodic) structures of a pattern can give rise to undesired light diffraction, superseding in intensity the light originating from random scattering events. To avoid this, a selective aperture device (denoted by 1 in Fig. 1) can be inserted underneath or above the collecting lens. This spatial filter blocks the lowest order diffracted light from reaching the detector while the scattered light can pass. This feature is less easily incorporated in flying spot scanning methods.

The coaxial arrangement is of vital importance. By collecting the

light always under the same scattering geometry irrespective of the spatial location of an event on the wafer and by a constant detector spot, one can avoid the spatially varying detector sensitivity. Thus, very high sensitivity and sensitivity uniformity across the wafer can be achieved, as long as a sufficiently high electronic gain-bandwidth product is used. With this method the drawback of the flying spot scanning method can be circumvented, and more subtle details can be observed.

Fig. 2 is a block diagram of the instrument. The scattering events are counted in a digital counter and simultaneously displayed as a true map of the wafer on the CRT display. The display can be used in connection with a microscope attachment to directly inspect and identify a certain event in situ right after scanning. A dc bias potentiometer (called Threshold I) is used to set the intensity threshold for an event to be detected. There are provisions in the circuit for (a) a test pattern display to check the working state of detector and electronics and (b) a calibration procedure to sense the laser intensity reaching the wafer and, if it should vary due to laser power loss with time, to account for it by appropriate gain adjustment. The latter represents a convenient means for the operator to easily check for calibrated conditions.

The electronics has been designed for high stability (see Table 1); the limiting drift of the instrument is given by the laser intensity stability.

Fig. 3 shows the blue (4416 Å) version of the instrument, and Fig. 4 shows the mechanical unit for the red version (6328 Å). The uv version is identical to the blue version, but with different laser

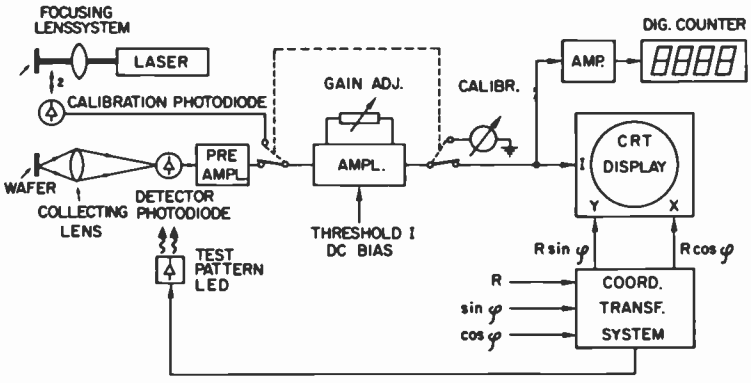

Fig. 2—Block diagram.

Table 1—Laser Scanner Specifications

Wafer size: 1 to 5 inches (expansion to 6 inches) round; 2 to 4 inches (expansion to 5 inches) square.	
Scan time for 4-inch wafer: 10 sec.	
Spot size: 50 μm × 230 μm	
Scanning spiral pitch: 200 μm	
Turntable rotation: 1800 rpm	
Depth of focus (max. wafer level variation): ±1.5 mm	
Limiting bandwidth of detector/electronics: >100 kHz	
Event pair resolution at 3 inches and threshold I 750 units: <10 μm	
Sensitivity (smallest particulate or hole observed in scanner *and* microscope): 0.75 μm. Probably much smaller (see text)	
Time stability of the instrument: ±1 unit of threshold I dc bias (resulting fully from the laser intensity stability).	
Microscope attachment:	enlargement: 200×
	resolution: about 1 μm
	working distance: 17 mm

mirrors and uv optics. The appropriate version is chosen according to the desired light penetration depth into the wafer or film. The blue version is most convenient for general use since it permits the study of present day thin films in addition to bulk material; in silicon the penetration depth is typically about 2000 A for blue light of 4416 A, about 200 A for uv and about 2.5 μm for red.

The microscope attachment can be used for direct inspection of a scattering event on the stage. First the wafer is scanned with the aligned microscope. Then, the turntable is kept stationary. Using the display pattern, one changes angle φ and translation R so that the moving scope spot coincides with the event on the storage scope. The defect or dust then is within the microscope viewing field.

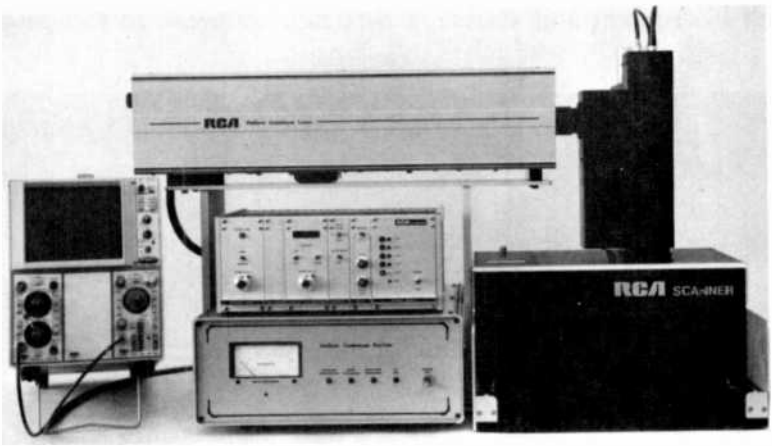

Fig. 3—Blue version of scanner with HeCd laser (4416 Å).

Fig. 4—Mechanical unit of scanner, red version with HeNe laser (6328 Å).

3. Performance

Typical dust and defect patterns, as observed on the storage scope display, are shown in Fig. 5 for three different sensitivities set by threshold *I*. Defects such as scratches, fingerprints, stain marks can of course be easily detected and do not require a high sensitivity; they will not be discussed further. Note in Fig. 5 the wide range of the instrument, which can be expanded by introducing attenuators between preamplifier and amplifier (see block diagram, Fig. 2).

The smallest particle or defect size that can be detected by any such instrument is of course of particular interest. In this respect

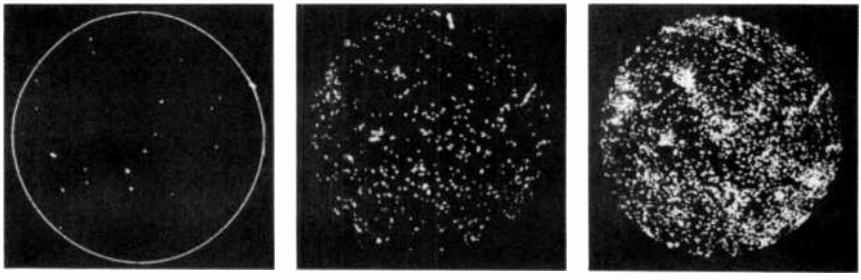

Fig. 5—Typical dust/defect pattern of a wafer taken at three different settings of the intensity threshold (threshold I).

it should first be pointed out that many commercial instruments provide grossly misleading specifications or labeling on the selecting dials by giving exact size (in μm) of dust particles or defects that supposedly are detected. It should be stressed that it is impossible to state exact size in absolute terms since holes, defects, and dust particles of identical size scatter light with greatly different efficiency. The scattering efficiency (or cross section), apart from the particle or defect *size*, very strongly depends on the refractive index (or index change), shape (form, facetting, etc.), surface quality (smooth, rough) of the particle or defect. Calibration in terms of size can only be stated for a well-defined environment, and only if calibration by some secondary means (like microscopy, transmission electron microscopy, etc.) has been performed. It is for this reason that the present instrument is provided with a microscope attachment for direct inspection and calibration purposes.

We have used several methods to establish the detectability limit of the present scanner in terms of size:

(1) On a wafer exhibiting very few events (to permit an unambiguous interpretation), we have, with the microscope attachment, positively observed particulates and defects as small as 1-μm diameter.
(2) We have designed an electron-beam-written chrome mask with four different arrays of holes of sizes 5, 2, 1, and 0.75 μm (see Fig. 6). Due to the regularity of the holes it is possible to judge at which sensitivity setting a particular size is still detected, despite some in-between events. We have established that 0.75-

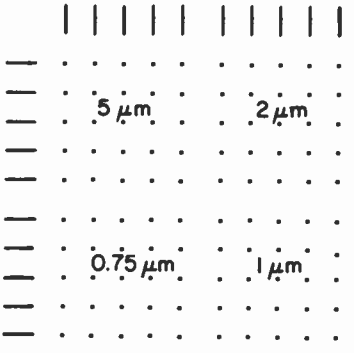

Fig. 6—Chrome mask for testing detectability limit of scanner. Dots represent regular arrays of holes of specified diameter etched into chrome film (kindly supplied by R. Geshner and J. Mitchell).

μm-diameter holes in a chrome film can be detected with the present scanner. One also knows that scattering from particulates or defects is considerably (maybe 10 to 100 times) more efficient than from straight holes.

From these experiments we conclude that the detectability limit for defects in terms of size of the present instrument is certainly 0.75 μm and most likely of the order of the wavelength of the light (i.e., about 0.4 μm).

A relative calibration in terms of size of one instrument against another, or of one instrument with time, has been provided by M. Leahy by designing silicon wafers with arrays of etched-in pits of different dimensions.[7]

Extended tests have been made on the usefulness of the scanner, and there is no doubt that it can detect events that are beyond the detection capability of inspection under bright-light illumination. The instrument has been applied in various areas within the RCA Solid State Division during the last few years to:

—maintain cleaning stations in perfect condition
—trace particulate contamination in reactors for epitaxial growth and in diffusion reactors
—detect particulates and defects on epi silicon and SOS wafers
—development of mass cleaning facilities for silicon wafers to be used as solar cells
—show evidence of tweezer marks
—show evidence without oxidation techniques of defects on epitaxial layers, such as slip lines, subtle surface scratches (due to scrubbing, swabbing, and/or removing of surface protrusions), etch pits, etc., all normally not visibile in wafer inspection
—incoming inspection of chrome photo- and electron beam masks

3.1. Some Particular Applications

3.1.1. Epitaxial Growth

Several epitaxial layers of the power transistor process have been scanned to study the question of surface protrusions or growth irregularities that frequently appear on them. In addition to a few large bumps there are quite a number of smaller defects not easily seen under bright-light illumination by eye. A typical resulting wafer map is shown in the middle part of Fig. 7. To determine the nature of these defects we cut through two of the larger ones, as shown in Fig. 7, and performed scanning electron microscopy (SEM) on the cross sections. It can be seen in the top part of Fig. 7 that

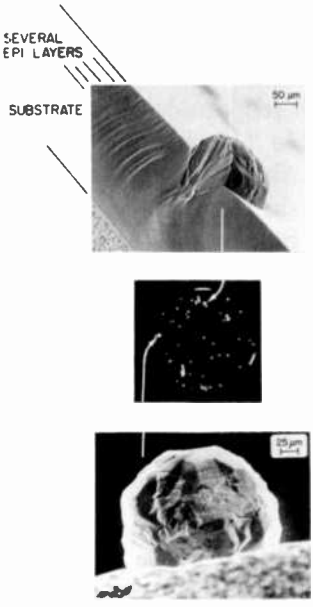

Fig. 7—Center: Scanner map of bumps and defects on epitaxially grown films. Top and bottom: SEM photomicrographs of two of the larger defects as marked in center photo (courtesy of L. Krausbauer).

this defect consists of material that started to grow at the original substrate surface, and it must have grown at a faster speed than the environment. From the bottom part of Fig. 7 it is seen that this material consists of large single crystals of silicon, since the silicon (111) and (100) faces can easily be identified. The conclusion is that nucleation must have taken place at the substrate surface in the epitaxial growth, and that this nucleation most likely was initiated by a particulate, possibly of silicon dust. These bumps or defects are of course disadvantageous for further processing of the wafers. The scanner thus can determine the acceptability limit and serve as an objective instrument with rapid feedback for improving epitaxial growth conditions.

In an effort to improve the substrate quality for epitaxial growth, a correlation extending over a considerable time was made in the factory of the substrate defect counts and the yield of power transistors produced from the wafers. As a result of a very good correlation, appropriate measures were taken that caused the yield of a particular type to increase from 50 to 80%.

3.1.2. MEBES Mask Incoming Inspection

Several MEBES (electron beam lithography) masks, from different manufacturers, were inspected with the scanner, and the results are presented in Table 2. It is quite obvious that there are appreciable differences in the fluctuations of the counts and in the average counts per mask. Despite the finding that not all (or maybe only a few) of these defects are causing defects in the present day processed masks, it is interesting to learn that manufacturer A is known to produce masks with best performance in terms of defects after processing (as detected, e.g., with the KLA photomask inspection system[8]). It is also seen that filtering the resist provides a lower count figure. We anticipate an increasing relevance of such testing as integrated circuit dimensions shrink.

Table 2—Incoming Inspection of MEBES Masks* (Counts on 10 masks from 4 different manufacturers, A to D)

(a) COP

A	B		C	D
0	3	41	40	38
0	19	7	7	33
0	10	70	22	68
3	2	4	55	27
0	13	69	5	25
0	168	25	70	20
0	2	33	10	57
10	24	13	28	5
4	10	116	8	41
5	0	30	87	20
Ave. 2.2	25.1	40.8	33.2	33.4

(b) PBS

A	B		D
	resist unfiltered	filtered	
7	190	37	73
0	11	31	61
1	60	36	33
5	24	31	187
5	25	11	263
0			62
0			31
6			40
4			39
0			27
Ave. 2.8	62.0	29.2	81.6

* Data supplied by J. Mitchell

3.1.3. Development for Mass Cleaning of Solar-Cell Wafers

In a study of the feasibility of megasonic cleaning[9] of a large number of silicon solar-cell wafers per unit time, the scanner served as a diagnostic and control tool to monitor the performance of the cleaning. Due to the rapid feedback of very detailed information (display of the pattern of contamination) it has played a vital role in the successful completion of this program.

3.1.4. Dust and Defects on Patterned Devices

A very attractive application of the scanner is to detect defects and dust on patterned wafers. As mentioned above in connection with Fig. 1, this application can be achieved with the scanner. For some very fine and particularly for very regular patterns, it is less successful, except possibly for the early processing stages; this needs further study. In many instances, however, it works well. The top of Fig. 8 is a photomicrograph of a patterned wafer exhibiting a defect. The two bottom displays of Fig. 8 show the application of the scanner. When the scanner is used without special precautions, the display (bottom left) only shows the diffraction pattern originating from the diffracting elements given in the wafer pattern. For this display a 30-dB attenuation was inserted to avoid full blooming. At this sensitivity and with the superimposed "Maltese cross" (diffraction pattern), it is hopeless to observe any defects. After inserting the selective aperture device to block off the lowest diffraction orders caused by the more or less regular patterns (see Fig. 1), we obtain a display of the defect (bottom right part of Fig. 8), and this at a very much higher sensitivity (0-dB attenuation). In fact, with the microscope attachment we have performed a direct inspection and established that the defect shown in the top photomicrograph is the very bright spot indicated by the arrow in the bottom right of Fig. 8.

3.1.5. Other Applications

The scanner can be used in a mode differing from the one for dust and defect detection. This application (described in detail in ref. 10) is based on using the threshold I setting for which a particular wafer or wafer section just turns to full (blooming) writing level. The corresponding threshold I value is a direct measure of the structural perfection of the bulk part of a wafer or film, i.e., the parts between the individual defects. This application is extremely useful in ma-

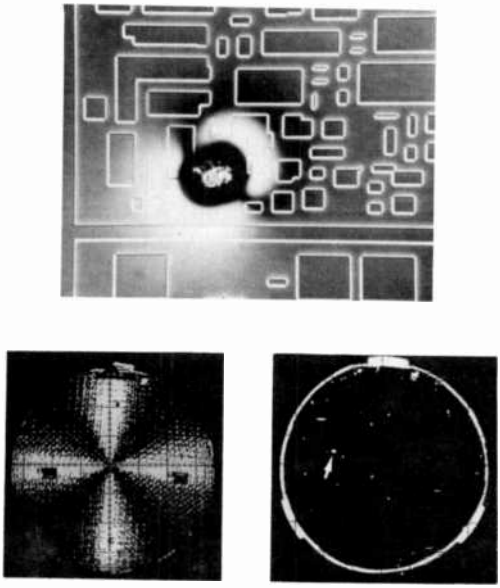

Fig. 8—Top: photomicrograph of patterned wafer (× 52) with defect (courtesy of A. Dreeben). Bottom left: Scanner display of same wafer *without* selective aperture device, taken with 30-dB attenuation. Observed are the diffraction patterns created by the fine array patterns on the wafer. Bottom right: Scanner display of same wafer *with selective aperture device*, taken with 0-dB attenuation. Defect of top micrograph is now observable (arrow).

terial perfection and/or acceptability characterization in many instances.[11] One of the predominant items is the characterization of structural perfection of LPCVD polysilicon layers grown at different deposition temperatures.

4. Conclusion

The main advantage of the present scaner as compared to other methods can be summarized as follows:

(1) The coaxial arrangement permits an extremely high sensitivity and sensitivity uniformity across the wafer. The sensitivity is of such a high level that defect and polishing nonuniformities can be observed in many of the very high quality wafers sold by the leading manufacturers and considered to be acceptable in the semiconductor industry. The current defect level of the scanner on freshly unpacked wafers from two leading manufacturers is of the order of 20 to 40 events.

(2) With the microscope attachment, the scattering events can be inspected after scanning on the stage. An unambiguous size calibration is possible for a given environment.
(3) The selective aperture device allows the inspection of dust and defects on patterned wafers, particularly at the early process stages.
(4) In another mode ot operation,[10] the scanner can be used successfully for wafer and thin-film quality assessment and for acceptability judgment in terms of structural perfection of bulk and thin-film material. This is of high interest for a wide range of materials: bulk silicon to amorphous silicon, polysilicon, epitaxial silicon, silicon on sapphire (SOS), many thin-film materials, photomasks, and videodisc material.
(5) The scanner offers an excellent performance-to-cost ratio.

Acknowledgment

Many contributions to this work are gratefully acknowledged: K. Knop for suggesting the coordinate transformation system; A. Mayer for advice on requirement conditions and useful feedback with respect to cleaning; M. Derendinger and E. Rohner for mechanical constructions; H. Lusch and M. Tgetgel for building and testing electronics; J. Lauffer and S. Vecrumba for helpful feedback from the application point of view; R. Geshner and J. Mitchell for the chrome masks for detectability testing and for testing the scanner on MEBES masks; M. Leahy for supplying test structures; L. Krausbauer for SEM studies; A. Dreeben for supplying patterned wafers; W. Bösenberg, L. Jamiolkowski, W. Burrell and others for supplying wafers; and many others for useful suggestions and help.

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Rapid Characterization of Polysilicon Films by Means of a UV Reflectometer

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Abstract—A UV reflectometer is described that was originally developed for the measurement of the near-surface crystallinity of silicon on sapphire. It is shown that this instrument can also be used to characterize the surface roughness of amorphous and polycrystalline silicon films.

Introduction

The maximum of the room-temperature reflectance spectrum of single-crystal silicon lies at a wavelength of about 280 nm, corresponding to a photon energy of 4.4 eV. It is caused by optical interband transitions at and in the neighbourhood of the X point of the Brillouin zone. An earlier work[1] had shown that this maximum reflectance value can be used to determine the surface quality of silicon. Based on that work, a fast, nondestructive and quantitative method to characterize the near-surface crystallinity of hetero-epitaxial silicon on sapphire (SOS) films was developed.[2] The method employs a measurement of the reflectance at $\lambda \approx 280$ nm (which is influenced by both degraded crystallinity and surface texture or "haze") and a second measurement at $\lambda \approx 400$ nm (which is mainly influenced by surface texture) for reference.

We show in this paper that the individual reflectance values at these two wavelengths can, each in a different way, be used to characterize the surface quality of amorphous and polycrystalline silicon

films. First, the UV reflectometer developed for SOS quality control on the product line is described. Then the application of the instrument for the measurement of silicon films grown by low-pressure chemical vapour deposition (LPCVD) is discussed.

Instrument Description

The UV reflectometer is designed to measure the reflectance of semiconductor wafers at various fixed wavelengths in the ultraviolet spectral region. In particular, it was developed to measure the reflectance of silicon-on-sapphire (SOS) wafers at a wavelength of $\lambda = 280$ nm and at other wavelengths in the ultraviolet.

The optical layout is shown schematically in Fig. 1. The instrument uses a deuterium lamp, which provides a continuum light source. The filter holder has two compartments for interference filters and can be fixed in two positions for a choice of wavelengths. The transmitted light is reflected by the mirror and focussed by lens I in a plane close to the chopper such that the light spot on the sample surface has a diameter of 4 to 5 mm. During about 45% of the chopper time cycle, the light beam is reflected by the chopper blades in the direction of lens II and the detector. There is zero reflection during about 5% of the chopper time cycle, because the corresponding parts of the chopper blades are blackened. During the remaining 50% of the time cycle, the light is transmitted by openings in the chopper wheel and reflected by the sample in the direction of lens III and the detector. The reflecting chopper blades are

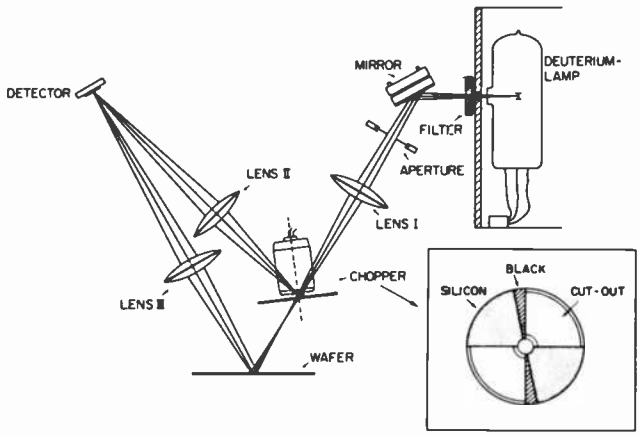


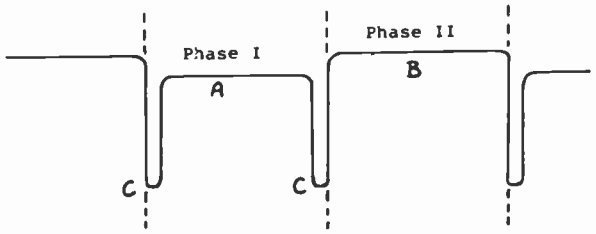
Fig. 1—Optical scheme of the UV reflectometer.

made of well-polished single-crystal silicon so that the reflectance at any wavelength is close to the ideal reflectance value of silicon.

The detector is a silicon photovoltaic device having an enhanced UV response. The electric signals from the detector (reference signal A and sample signal B) are used to form the difference signal $A-B$. The difference signal is normalized by dividing by the signal A in order to eliminate fluctuations and drift of the lamp intensity. With silicon chopper blades of the ideal reflectance values, the signal $(A-B)/A$ would be a direct measure of the deviation of the reflectance of the sample from the ideal value. Since the surface quality of the silicon blades may change with time, the signal $(A-B)/A$ after phase-sensitive detection and amplification is set electronically to zero for a reference wafer of high-quality single-crystal silicon. In a subsequent measurement of an SOS wafer, the signal $(A-B)/A$ is a direct measure of the reflectance deficiency of the SOS wafer at the measuring wavelength. It is displayed in the digital voltmeter (DVM) display unit.

Circuit Description

The light level reaching the detector has a time variation as shown below



Here the level A is the reflected intensity from the chopper and level B that from the sample. Level C is the zero level, which occurs when the light strikes the black painted bars on the chopper wheel. The function of the circuit is to obtain an output signal proportional to $A-B$, but normalized to the difference value $A-C$ which measures the lamp intensity.

A logic signal, positive during phase I and zero during phase II, is derived from a separate light source mounted in proximity to the chopper wheel. The output from the detector is amplified by a variable gain amplifier, D in Fig. 2. The capacitance coupled output of D is held via resistor 1M to ground potential during phase I by the

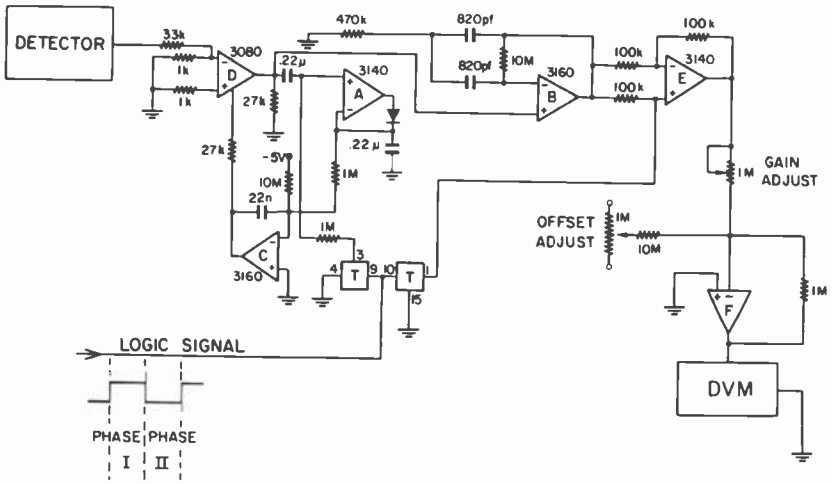
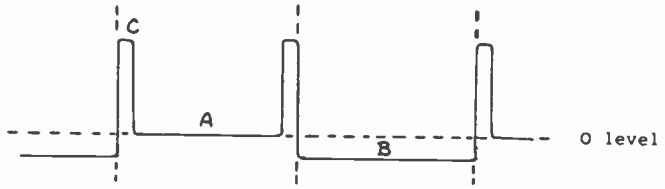


Fig. 2—Amplifier circuit diagram.

switch T. The signal presented to the positive input of amplifier A appears therefore as below



with the zero level close to level A. Amplifier A in Fig. 2 measures the most positive value of this waveform and so measures the level difference $C-A$. Amplifier C operates in a feedback loop to control the gain of amplifier D so that the level difference $C-A$ is always constant at about 500 mV regardless of the lamp intensity.

The output of amplifier D, which is the normalized signal described above, is amplified by the bandpass amplifier B and phase-sensitive detected by E. The output of E is smoothed and adjustably offset at amplifier F before being measured at the DVM. Thus the DVM measures a signal proportional to the difference $A-B$, normalized to eliminate the effect of variation in lamp intensity. The sensitivity of the DVM is adjusted so that one unit on the display corresponds to a reflectance deficiency of 0.05% at a wavelength of $\lambda = 280$ nm.

Characterization of Polysilicon Films

Recently, it was shown[3] that only films deposited as amorphous silicon and subsequently crystallized by annealing have the high quality, in terms of structural perfection and surface roughness, that is required for critical applications. Any method to characterize the surface quality must therefore be applicable to both amorphous and crystalline films. Fig. 3 shows the absorption coefficient K (and the light penetration depth $d = 1/K$) of single-crystal silicon[4] and LPCVD amorphous silicon.[5] It can be seen that at $\lambda = 280$ nm, the penetration depth in either phase is smaller than 100 Å. We can conclude, therefore, that the incident light probes very near the surface of amorphous and crystalline films. This is still reasonably accurate for light of wavelength 400 nm incident on an amorphous film ($d \simeq 150$ Å). A polycrystalline film however is probed to a depth of about 1000 Å at $\lambda = 400$ nm. Correspondingly larger probing depths hold when the scanner is used for dust and defect detection in the quality control mode at a wavelength of $\lambda = 4416$ Å.[6] The scanner method is therefore more useful for probing bulk structural perfection in polycrystalline films.

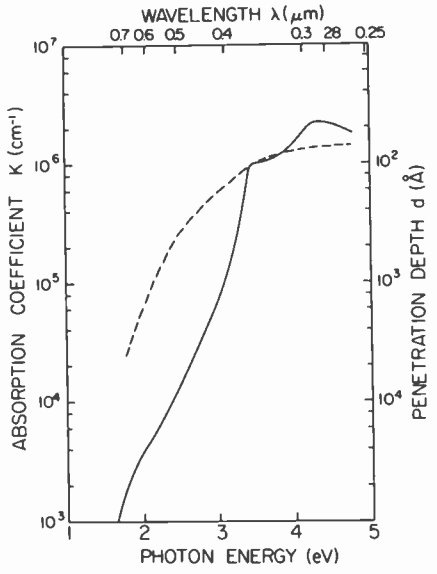


Fig. 3—Absorption coefficient determined by ellipsometry of single-crystal silicon (solid line, from Ref. [4]) and LPCVD amorphous silicon (dashed line, from Ref. [5]) versus photon energy.

The basis for the use of the UV reflectometer to characterize silicon films is illustrated in Fig. 4, where the reflectance of single-crystal silicon is compared to that of polycrystalline and amorphous films. Single-crystal material shows two maxima in this spectral range at $\lambda = 275$ nm and $\lambda = 365$ nm. These maxima can still be seen in the curve taken from a very rough polysilicon film, but the absolute reflectance is considerably reduced. The difference between the single-crystal and polysilicon reflectance curves increases with decreasing wavelength due to the increasing amount of light scattered from the rough surface at shorter wavelengths. The reflectance curve of a smooth amorphous film does not display any structure in this range and is lower than single crystal at the main maximum but higher in other spectral regions, e.g., at $\lambda = 400$ nm.

The vertical scales in Fig. 4 at 280 nm and 400 nm indicate the reflectance difference ΔR_{280} and ΔR_{400} relative to the single-crystal standard. One ΔR unit at 280 nm corresponds to about 0.05% loss of absolute reflectance and at 400 nm to 0.03% loss.

Fig. 5 shows the reflectance difference ΔR_{280} of undoped polysilicon films annealed for 30 min at 900 to 950°C versus root-mean-square surface roughness σ. The determination of σ as a measure of the vertical surface irregularities associated with lateral dimensions of the order of a hundred to a few thousand Å has been reported before.[7] It is done by measuring the loss of reflection in the surface plasmon region ($\lambda = 350$ nm) of a thin silver film evaporated onto the silicon surface. It was found that σ was smaller than 15 Å

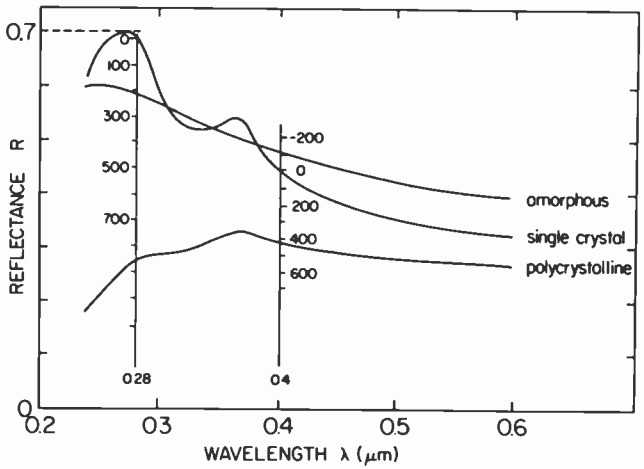


Fig. 4—Reflectance of single-crystal silicon, a rough polysilicon film, and a smooth amorphous silicon film versus wavelength.

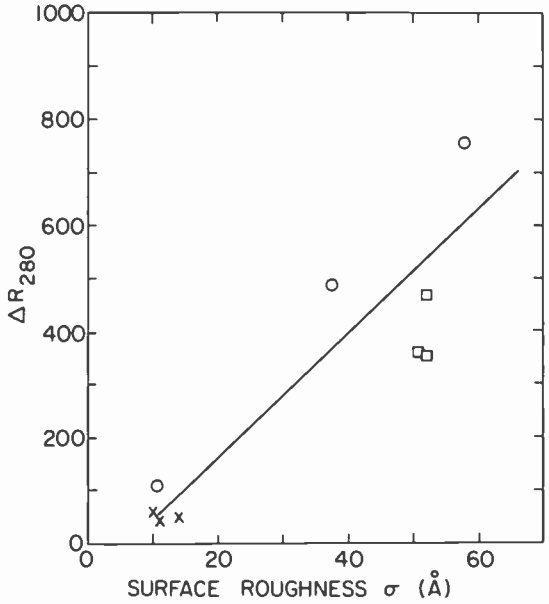


Fig. 5—Reflectance difference ΔR_{280} of undoped polysilicon films annealed at 900 to 950°C versus root-mean-square surface roughness. Xs are for deposition for temperature $T_d \leq 580$°C; Os for $T_d = 600$°C; and □s are for $T_d = 620$°C. The solid line is a guide to the eye.

for films originally deposited in the amorphous phase, i.e., at $T_d \leq 580$°C. Deposition at 620°C results directly in polycrystalline films with σ values between 50 and 60 Å, whereas $T_d = 600$°C occasionally gave a smooth surface but at other times produced rough films. The technique is sensitive but it does not lend itself to rapid quality control on the product line.

Fig. 5 shows that ΔR_{280} and σ correlate rather well for these annealed films. In particular, the high quality, low-T_d films all have small ΔR_{280} and σ, and even the $T_d = 600$°C films follow the correlation in spite of the run-to-run variation of their surface quality. (We do not want to speculate on the result that the extrapolation of the line would cut the abscissa at a value of about 5 Å, because surfaces with a roughness below 10 Å are difficult to prepare, even in a polished reference wafer.) The ΔR_{280} measurement can thus be used for a rapid roughness characterization of polycrystalline films irrespective of whether they have been initially grown as amorphous or polycrystalline films.

The second objective is to use the relectometer for a roughness characterization in the as-grown state. This is particularly relevant

for this application since it has been found that the surface roughness does not change upon annealing, even for very smooth amorphous films, which crystallize in the annealing process. It can be seen from the reflectance curve for amorphous silicon in Fig. 4 that 280-nm light is not suitable to check a smooth and amorphous film, since the amorphous state pulls the reflectance downwards, i.e., in the same direction as roughness does. Light of 400-nm wavelength is well suited, however, since the amorphous state pulls the reflectance upwards into the range of negative ΔR_{400} values of about -100 units for smooth amorphous films. Fig. 6 illustrates this effect; all low-T_d amorphous films cluster around -100 units whereas all rough films have values above $+150$ units. The ΔR_{400} measurement can thus be used for a combined smoothness/amorphousness characterization of the as-grown films and also as a meaningful predictor of surface quality after post-deposition annealing or corresponding processing steps.

It has also been shown that there is a strong dependence of the surface roughness of in-situ phosphorus-doped (gas flow ratio $PH_3/SiH_4 = 8.10^{-4}$) silicon films on the deposition temperature and that this dependence is similar to the case of undoped films.[8] The ΔR_{280} and ΔR_{400} values of these films are plotted in Figs. 7 and 8, respectively. It is worth noting that at the low-roughness end, the ΔR values are generally higher than those of undoped films (dashed lines) of the same roughness.

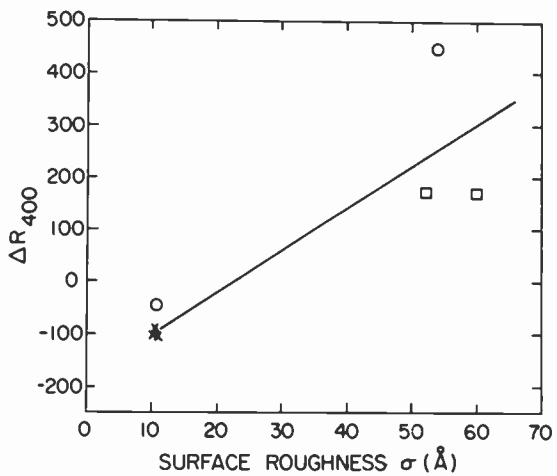


Fig. 6—Reflectance difference ΔR_{400} of undoped as-grown silicon films versus root-mean-square surface roughness. Xs are for $T_d \leq 580°C$, amorphous; Os for $T_d = 600°C$, mixed; and □s are for $T_d = 620°C$, crystalline. The solid line is a guide to the eye.

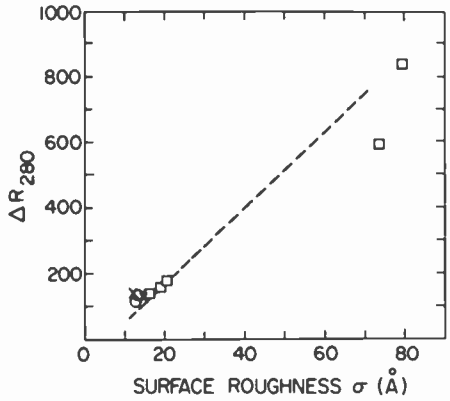


Fig. 7—Reflectance difference ΔR_{280} of in-situ phosphorus-doped ($PH_3/SiH_4 = 8.10^{-4}$) polysilicon films annealed at 900 to 950°C versus root-mean-square surface roughness. Xs are for $T_d \leq 570$°C; Os for $T_d = 580$°C; □s for $T_d \geq 600$°C. The dashed curve illustrates the data obtained on undoped films in Fig. 5.

Such effects of doping on the intrinsic reflectance spectra of semiconductors are well known. For example, by doping with 5×10^{19} cm^{-3} of arsenic the maximum in the spectrum of single-crystal germanium at 4.5 eV (which is also caused by interband transitions at the X point of the Brillouin zone) is slightly shifted and reduced by about 6% relative to its original value.[9] Similarly, the optical properties of amorphous silicon in the ultraviolet are strongly influenced by phosphorus doping.[10] Since our films contain more than 10^{20} cm^{-3} phosphorus atoms,[11] we can expect a decrease of the reflectance by

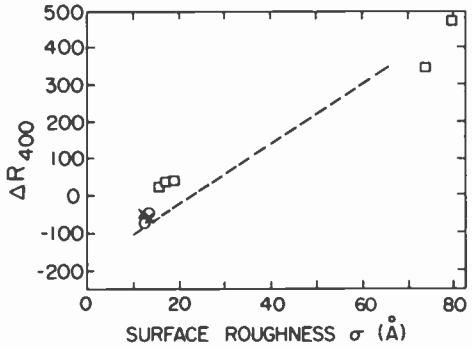


Fig. 8—Reflectance difference ΔR_{400} of in-situ phosphorus-doped ($PH_3/SiH_4 = 8.10^{-4}$) as-grown silicon films. Xs are for $T_d \leq 570$°C, amorphous; Os for $T_d = 580$°C, mixed; and □s for $T_d \geq 600$°C, crystalline. The dashed curve illustrates the data obtained on undoped films in Fig. 6.

a few percent, which will show up, for example, as additional tens of units compared to ΔR_{280} measurements for undoped films.

This effect should be taken into account when surface quality standards are set for doped polysilicon films. If this is done, there is again a fair agreement between roughness and ΔR_{280} measurements of the annealed and ΔR_{400} measurements of the as-grown films. Phosphorus-doped films grown at T_d = 600°C or 620°C are polycrystalline but still of medium surface quality with $\sigma < 25$ Å. Thus the ΔR_{280} values of these films also correlate well with the roughness, while the ΔR_{400} values are small but positive because of the crystalline nature of the films. Phosphorus-doped films grown at T_d = 640°C have rough surfaces with σ = 70 Å as shown in Figs. 7 and 8.

Summary

We have described a UV reflectometer developed for the near-surface quality control of silicon-on-sapphire films on the product line. In addition to the SOS application, the instrument can be used to characterize the near-surface quality of undoped and in-situ phosphorus-doped polysilicon films. It is recommended that the λ = 400 nm reading be used as a direct check of the as-grown state, i.e., as a combined measure of smoothness/amorphousness quality. Correspondingly, the λ = 280 nm reading should be used as a direct check of the smoothness after post-deposition annealing or equivalent process steps. Both these readings correlate with the root-mean-square surface roughness measured by an optical laboratory technique. This statement also holds for phosphorus-doped samples, provided the appropriate small doping-induced correction is taken into account.

After the initial laboratory work was done, we received and measured several batches of amorphous and polycrystalline films grown by LPCVD at various RCA locations. The data obtained on these samples agree very well with the correlation between roughness and ΔR values as illustrated by Figs. 5 through 8. More important, the roughness (and ΔR) versus growth-temperature behaviour is also nearly identical to the laboratory results. That means that the amorphous growth process and rapid characterization by UV reflectometer (and Laser Scanner) can be transferred to the product line in a straightforward manner.

Acknowledgments

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The Growth and Characterization of Epitaxial Solar Cells on Resolidified Metallurgical-Grade Silicon*

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Abstract—This paper describes the results obtained at RCA Laboratories in the development of a solar-cell process based on using epitaxial thin films grown on a substrate made from low-cost metallurgical-grade (MG) silicon. The properties of the starting MG feedstock are described and related to the observed problem of SiC particle formation during ingot solidification. Data obtained on the size, spacial distribution in ingots, and the subsequent effect of particles on epitaxial solar-cell performance are presented. Methods for significantly reducing the SiC particle density were developed and are discussed along with the characteristics of solar cells made in particle-free material. The rotary-disc reactor used for epitaxial growth of solar-cell structures and its scale-up to large area and high throughput is described.

1. Introduction

The possibility of the application of solar cells to generate substantial amounts of electrical energy for terrestrial applications relies heavily upon achieving significant cost reductions in the manufacture of future solar-cell modules. Such cost reductions must be achieved without a major sacrifice in solar-cell performance, because many of the costs associated with the auxillary electrical and structural support systems depend upon the power output per unit area of the solar-cell modules. The price of photovoltaic modules has been reduced during recent years, but the present price of $7–10/Wp is still too high, primarily because bulk silicon wafers are used for

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fabricating the solar cells. The wafer cost now constitutes about half that of the finished module. Wafer costs in turn can be subdivided into the cost of polysilicon material and fabrication of the wafer. Wafers can be fabricated via an ingot solidification process combined with a slicing technique[1] or may be formed by a ribbon process.[2] Some advances have been made in these technologies and several are being practiced on a commercial basis using expensive ($60–80/kg) semiconductor grade polysilicon as the starting material. Significant progress has also been achieved in developing processes to produce low-cost polysilicon; however, these processes have been demonstrated only on a laboratory scale.

In practice, therefore, present photovoltaic wafers are manufactured by conventional, energy-intensive processes. The problem is further aggravated because thick (250–500 μm) wafers are used for mechanical reasons, whereas a thickness of only about 25–50 μm is required for efficient energy conversion with silicon solar cells.

This paper describes work conducted at RCA Laboratories over a period of several years that was directed at providing a solution to the above problem by developing a solar-cell process based on using epitaxial thin-films grown on a substrate made from low-cost metallurgical-grade (MG) silicon. This approach to the manufacture of low-cost solar cells was arrived at in an evolutionary manner. First, demonstration of efficient (14%) solar cells was achieved with 15–50 μm epitaxial films grown on high-quality single-crystal silicon substrates.[3] Later, the epitaxial technique was combined by application on several different substrates[4] derived from MG silicon, thus demonstrating the feasibility of obtaining high-quality epitaxial layers on a low-cost substrate. Recently, this work was extended with development of a large-scale ingot solidification technology using MG silicon feedstock along with the advanced development of epitaxial technology and equipment. The epitaxial work included research and development required to bring a novel RCA developed rotary-disc[5] epitaxial reactor to a stage suitable for solar-cell growth on MG silicon substrates. An important part of this work involved further development and scale-up of this reactor.

This paper concentrates on three salient technical features of the work described above. First a brief discussion is given of the physical and chemical properties of MG silicon followed by a description of the solidification methods used to form ingots. Characteristics of the solidified ingots as they relate to usefulness for substrates in the subsequent epitaxial growth are then described. In section 3 the epitaxial process used to make solar-cell structures and the electrical properties of such solar cells made on MG-derived silicon sub-

strates are presented. Particular attention is focused on the results obtained, and their relationships to MG-derived substrates. Section 4 describes the development of the rotary-disc reactor for use in solar-cell growth. Emphasis is placed on the high-volume aspects and the growth characteristics on large-area (up to 4 inches square) substrates. Some results for solar cells grown in this reactor are also given.

2. Metallurgical-Grade Silicon and Ingot Formation

Metallurgical-grade silicon is produced primarily for use in the aluminum and steel industries and has a current worldwide production rate of about one-half million metric tons per year. It is extracted from quartzite by carbonaceous reduction at high temperature (1850°C) in very large arc furnaces. The MG silicon is taken from the furnace in liquid form about 2 tons at a time and quickly solidified in molds, after which it is broken up into small chunks for sale at about $1.50/kg.

These chunks are physically quite porous, having a silicon content of 97–99% with the remainder typically made up of the elements listed in Table 1. About 1% of the MG silicon so produced is extensively purified, generally by the Siemens process, and sold to the semiconductor industry at about $80/kg.

To reduce cost while still meeting the requirements for solar cells, an intermediate approach for upgrading MG silicon is directional solidification. In directional solidification, most of the metallic impurities which have low segregation coefficients move to the last

Table 1—Spark Source Emission Spectrographic Analysis of MG Silicon

Element	ppmw
B	<10
Al	1300
Ca	14
Cr	11
Cu	10
Fe	1500
Mg	<0.5
Mn	170
Mo	<10
Ni	38
Ti	190
V	<3
Ba	<1
P	<50
Sn	<10
Sr	<3

material to freeze, leaving the remainder of the ingot relatively pure (see Table 2). This upgraded material is not useful for fabricating semiconductor devices and solar cells without further purification, but can be used as a substrate for solar cells made in an epitaxially grown silicon layer.

In our work, this approach was explored by fabricating and studying epitaxial layers and solar cells made on ingot material prepared at several commercial laboratories by different directional solidification methods.[6] Ultimately, a suitable working relationship was established with Crystal Systems, Inc. (CSI) to study solidification of MG silicon by the Heat Exchanger Method[7] (HEM) from selected commercial grade MG feedstocks. Such ingots were examined physically and chemically to establish their crystallinity, defect density, and impurity content. After a baseline level of purity was established, the primary method of ingot evaluation was by fabricating and studying the electrical characteristics of epitaxial solar cells made in the material.

Early in the work, it was found that the amount and type of impurities present in the MG feedstock have a major effect on the quality and useful amount of silicon obtainable from an HEM ingot. Specifically, the high carbon content present in most MG feedstock is related to the formation of particulate inclusions (mostly SiC) during solidification. These particles were found to have a detrimental effect on solar-cell performance by causing shunting, thereby limiting the yield of useful substrate material. The particles are revealed when the substrate wafers are chemically etched. The material immediately surrounding the particle etches more rapidly than the bulk silicon, leaving a pit with the particle in the valley

Table 2—Typical Impurities in MG Silicon (C_L), Equilibrium Segregation Coefficients (k), and Amount Expected after Directional Solidification (C_s)

Element	C_L (ppmw)	k	$C_s = C_L \times k$ (ppmw)
Al	1300	3.0×10^{-2}	39
B	11	0.8	8.8
Ca	250		
Cr	390	1.1×10^{-5}	0.004
Cu	60	8.0×10^{-4}	0.048
Fe	4200	6.4×10^{-6}	0.027
Mg	<5	3.2×10^{-6}	<0.001
Mn	120	1.3×10^{-5}	<0.002
Ni	100	1.3×10^{-4}	0.013
P	10	0.35	3.5
Ti	500	2.0×10^{-6}	0.001
V	230	4.0×10^{-6}	<0.001
Zr	30	$<1.6 \times 10^{-5}$	<0.001

as seen in Fig. 1. The size of the visibly detectable particles varies from 10 μm to as large as 500 μm in diameter, and their density within a given HEM ingot tends to be greater near the top and much lower near the seed or bottom end. The density and spatial distribution were found to vary somewhat with the source of MG feedstock. However, when pure semiconductor-grade feedstock was used in the same HEM apparatus, no particles were found, showing that particles are not equipment-related. An etched section of an ingot showing a typical particle distribution is shown in Fig. 1.

Physical and chemical analysis, powder x-ray diffraction, emission spectroscopy, and Auger analysis were made and have shown that the particles are primarily β-SiC, although Fe and Ca were also found to be associated with or in close proximity to the particles examined.

MG feedstocks obtained from a variety of domestic and foreign manufacturers were evaluated; however, the MG silicon feedstock obtained from Silicon Smelters Limited of Pietersberg, South Africa was found to be a much purer source than any of the domestic feedstocks investigated during this work. This supplier has one of the world's purest quartz deposits and uses a proprietary mixture

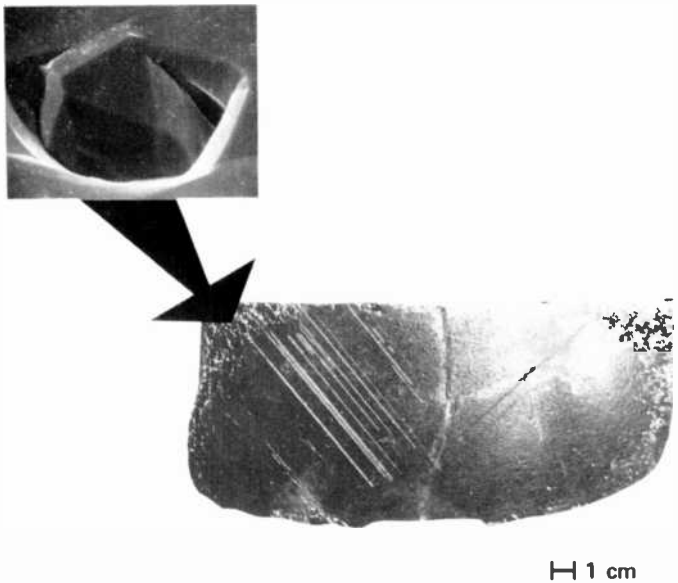


Fig. 1—SEM of typical particle as seen after etching; etched cross section of typical domestic MG singly solidified ingot showing particle distribution.

of carbonaceous reductants. The arc furnace operation of Silicon Smelters Ltd. is different from others because they make silicon primarily for the silicone industry, which requires a purer grade of metallurgical silicon. This MG silicon was both singly and doubly directionally solidified by HEM, and the density of SiC particles observed upon etching was found to be considerably less than domestic sources of MG silicon, as shown in Figs. 2 and 3.

Carbon analysis using the fusion technique was carried out on various MG feedstocks. The results on a number of samples from each source showed variation which was to be expected due to the inhomogeneous nature of MG silicon; however, the Smelters Ltd. material showed a lower range of values, 20-1500 ppmw, compared to 1000 to 3400 ppmw for the other sources.

The double solidification was performed by first removing about 5 mm of the outer surfaces of the singly solidified ingot and using the core of this ingot for the second solidification. Etching a cross section of this ingot revealed that the particles were confined to the top outer periphery of the ingot as shown in Fig. 3.

3. Ingot Characterization by Solar-Cell Fabrication

In addition to the etching and chemical analyses described above, the quality of the HEM solidified ingots as substrate material for epitaxial growth was assessed by fabricating and evaluating solar cells made on wafers sectioned from the bottom, middle, and top of the ingots. These evaluations included yield of particle-free cells and absolute and relative efficiency of the completed solar cells. A

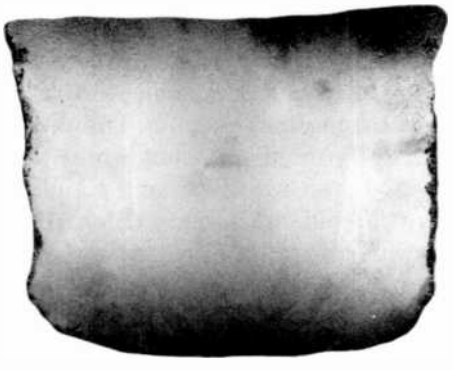
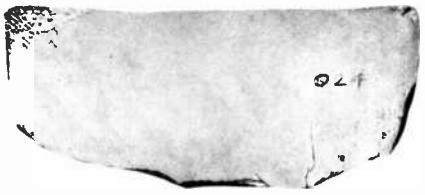


Fig. 2—Particle distribution, South African single solidification.



1 cm

Fig. 3—Particle distribution, South African double solidification.

sufficient number of cells were made from each section so that by simply counting the number of cells free from the shunting effect of particles, an assessment could be made of any reduction in particle density as well as the location of the highest density of particles within a given ingot.

For example, in single solidification of typical MG feedstocks other than the Smelters Ltd. source, the yield of nonshunted epitaxial cells ranged from 45 to 65%, with more than half of the shunted cells located near the top of the ingot. Single solidifications of the Smelters Ltd. feedstock resulted in about 80% yield, with most of the shunted cells still coming from near the top of the ingots. Double solidifications of the South African material generally resulted in about a 90% yield, with particle loss confined to very near the top of the ingot.

The absolute and relative performance levels of solar cells made in particle-free substrate material are described below.

3.1. Baseline Epitaxial Growth Process

The baseline epitaxial growth process utilized a laboratory-scale horizontal reactor to qualify HEM silicon substrates prior to use in the rotary disc high throughput reactor. The doping profile of the structure used extensively in our previous work[4] with epitaxial solar cells is shown in Fig. 4, and was used as a standard in this work.

The growths were carried out using dichlorosilane in a standard horizontal reactor. The quartz tube had a cross section of 5×10 cm and held a silicon carbide-coated graphite susceptor that was 30 cm long. Heating was accomplished by rf induction into the susceptor, which was inclined horizontally, and the walls of the reactor were air-cooled. Hydrogen was obtained from a Pd-Ag diffusion cell. The doping gas was diborane diluted with hydrogen at the 10- to 20-ppm level, and further diluted as needed before insertion into the

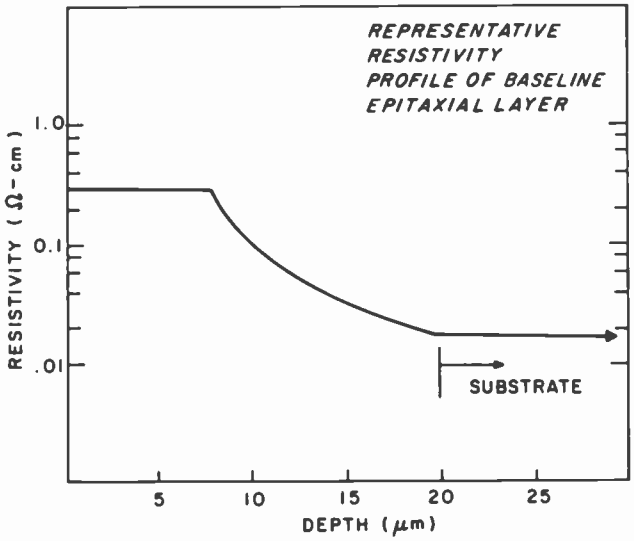


Fig. 4—Doping profile of epitaxial solar-cell structure.

reactant gas stream. Dichlorosilane was metered as a gas directly from the cylinder, and temperatures were measured with an optical pyrometer and corrected for emissivity and quartz adsorption effects. Typically, the temperature during growth is 1100°C and the growth rate is 5 μm/min.

3.2. Epitaxial Solar-Cell Performance

The data on epitaxial cells not showing the effects of particles were examined in terms of absolute and relative efficiencies and cell parameters to reveal performance levels within and between the HEM ingots. Examples of such data for epi-cells made on several typical solidifications are given in Table 3. In this table, the column marked $\eta_{epi}/\eta_{control}$ indicates the average efficiency achieved for the epi/HEM cells relative to that of epi cells made on control substrates of Czochralski (CZ) quality. Some important conclusions and indications deduced from these and similar data taken on other ingots are:

- Among the HEM ingots there is little difference in the best and average cell performances between the various ingots studied. It should be noted however that the cells made on double-solidified ingots (e.g., ingot 020) showed uniformly good performance, $0.92 \leq \eta_{epi}/\eta_{control} \leq 0.97$, from the top to the bottom portions of these ingots.
- Average efficiencies for all (except 001) 1- and 2-cm^2 cells are 10

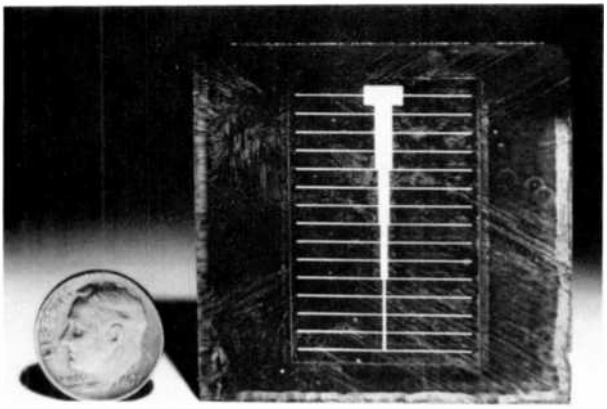
Table 3—Summary of Solar-Cell Characteristics for Epitaxial Cells Made on HEM Ingots[a]

Ingot	Cell Area (cm^2)	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF —	η_{bar} (%)	η_{corr}[b] (%)	$\eta_{epi}/\eta_{control}$ —
001 (Ave)	1.05	15.4	561	0.758	6.55	9.92	0.88
001 (Best)	1.05	15.6	560	0.763	6.66	10.07	0.84
001 (Ave)	2.07	14.6	568	0.762	6.28	9.50	0.84
001 (Best)	2.07	15.1	572	0.768	6.63	10.02	0.83
001 (Best)	10.2	14.9	558	0.693	5.76	8.30	—
003 (Ave)	1.05	16.7	569	0.757	6.74	10.90	0.96
003 (Best)	1.05	17.0	572	0.785	7.62	11.58	0.95
003 (Ave)	2.07	15.7	564	0.745	6.61	10.00	0.89
003 (Best)	2.07	17.0	561	0.751	7.16	10.81	0.89
003 (Best)	10.2	15.5	579	0.754	6.77	9.71	—
011 (Ave)	1.05	16.3	577	0.794	7.47	10.60	0.99
011 (Best)	1.05	16.7	584	0.806	7.86	11.16	1.01
011 (Ave)	2.07	16.5	581	0.786	7.55	10.72	0.99
011 (Best)	2.07	17.0	581	0.799	7.88	11.19	1.04
020 (Ave)	2.07	16.7	577	0.795	7.66	10.88	0.96
020 (Best)	2.07	16.8	580	0.808	7.88	11.20	0.92
020 (Best)	1.05	17.2	581	0.814	8.13	11.55	0.95
020 (Ave)	10.2	16.6	576	0.761	7.27	10.19	—
020 (Best)	10.2	16.9	580	0.777	7.63	10.68	—
018 (Ave)	1.05	16.4	576	0.776	7.34	10.41	0.87
018 (Best)	1.05	16.8	577	0.807	7.81	11.10	0.88
018 (Ave)	2.07	17.4	575	0.799	8.03	11.40	0.91
018 (Best)	2.07	17.4	575	0.799	8.03	11.40	0.91
026 (Ave)	1.05	16.5	567	0.790	7.39	10.49	0.88
026 (Best)	1.05	16.9	570	0.812	7.81	11.09	0.93
026 (Ave)	2.07	16.8	564	0.767	7.28	11.09	0.93
026 (Best)	2.07	16.7	570	0.771	7.35	10.44	0.88

[a] Total epitaxial layer thickness 20 μm for all cells.
[b] Corrected for AR coating.

to 11%. Values for 10-cm^2 cells are close to 10% with only the fill factor somewhat lower than for the small cells. The best cell of 10-cm^2 area was made on doubly solidified ingot 020 and is shown in Fig. 5.

- Average and peak efficiencies for cells made on substrates from ingot 011 are equal to the epi-controls, which are made on high-quality CZ substrates. Since this ingot was solidified from semiconductor-grade silicon, the data indicates that HEM substrates made from the same feedstock as CZ silicon are equally as good for epitaxial solar cells.
- The values of $\eta_{epi}/\eta_{control}$ between 0.83 and 0.97 indicate a loss of efficiency of 3 to 17% due to the use of HEM/MG substrates to make the epi cells. Some of the loss, especially in the lower effi-



AM-1 CELL PERFORMANCE

J_{sc}	V_{oc}	F.F.	η	Area
mA/cm^2	mV	–	%	cm^2
23.7	580	0.777	10.7	10.2

Fig. 5—10-cm^2 solar cell made on doubly solidified ingot 020.

ciency cases, is no doubt due to the presence of grain boundaries, point and line defects, and possibly very small inclusions. The remaining loss is due to a lower diffusion length (25–35 μm) measured in the epi-HEM cells compared to those on the CZ substrates (30–50 μm). Since the HEM/MG substrates, after solidification, still contain relatively high levels of known lifetime killers, these could easily account for this difference.

Additional estimates of the best performance obtainable from epi/HEM cells were obtained by using the services of Applied Solar Energy Corp. (ASEC). They used an established shallow-junction, fine-grid, double-layer AR coating cell process to make 24, 4-cm^2 cells on epi-layers grown on substrate wafers drawn from doubly solidified ingot 020. Control epi-layers grown on CZ substrates were also included in the experiment. The AM-1 characteristics of the completed cells were measured both at ASEC and at RCA. A summary of the results is given in Table 4. The data demonstrate:

- Solar-cell efficiency of ~12% is possible with epi-HEM/MG structures.
- Good average cell characteristics with $\bar{\eta} = 10.9\%$.
- The basic 20-μm epi structure is capable of high efficiency, i.e., $\eta \sim 13.5\%$, for control cells.

Table 4—Summary of Performance of 4-cm² Epitaxial Solar Cells Fabricated by ASEC

Cell Type	J_{sc}	V_{oc}	FF	η	No. Cells
Average Values					
Epi/SC[a]	26.0	0.597	0.774	12.0	12
Epi/HEM	24.6	0.576	0.742	10.5	23
Best Cells					
Epi/SC	26.3	0.604	0.847	13.4	
Epi/HEM	25.0	0.587	0.796	11.7	

[a] Epi/SC = Epitaxial cell on single-crystal Si control substrate.

4. Rotary-Disc Epitaxial Reactor Development

The method of producing solar cells described here relies on the growth of a thin (20 μm) layer of homoepitaxial silicon. For such a solar cell to be cost effective, certain requirements must be met by the reactor chosen. For example, large-area epitaxial solar cells require substrates with areas of about 100 cm², with square or rectangular shapes preferred for high packing density when assembled in the module.

The primary requisites are capability of reasonably high throughput of 100–300 wafers per hour with the ability to grow on square or rectangular wafers of up to 100-cm² area (≈10 cm on a side).

4.1. System Description

The HTR (High-Throughput Reactor) used in this work is best described as a rotary-disc type.[8–12] This equipment consists of a vertical stack of individual composite susceptors, each separated by spacers and each capable of holding two wafers, one on the top and one on the bottom. Gases are introduced by means of a distributor tube along the length of the stack. The stack rotates and is heated by a 50-kW, 450-kHz output, rf load coil placed around a quartz bell jar that surrounds the susceptor stack. The gas distributor tube can be rotated to direct the gas flow in a controlled sweep from side to side during growth. Details of this rotary-disc susceptor configuration are shown in Figs. 6 and 7. For comparisons, other conventional reactor designs are illustrated in Fig. 8. The rotary-disc reactor has several significant advantages over the barrel, horizontal, and pancake reactors:

(1) A higher wafer stacking density for a given reactor volume gives the rotary-disc reactors a higher wafer throughput per batch than other types of reactors. Comparative 100-mm-diameter

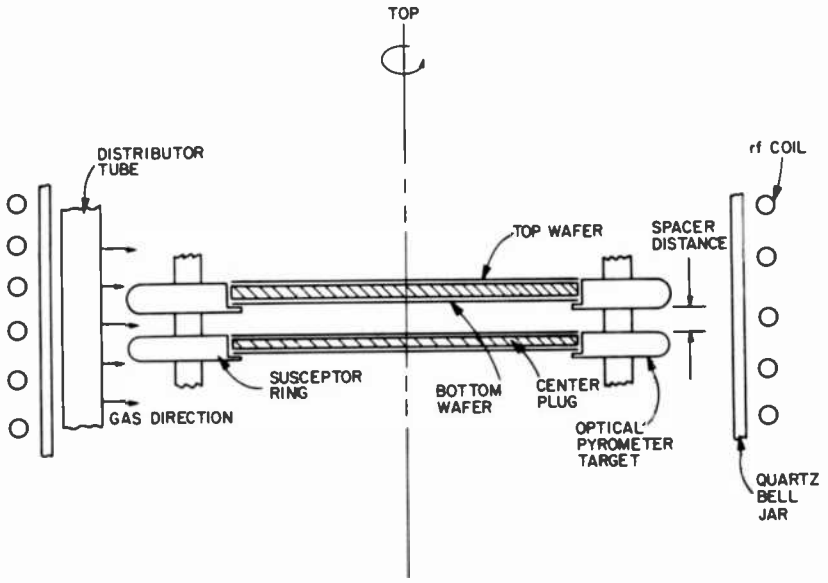


Fig. 6—Schematic of one section of a rotary-disc reactor.

wafer capacity for a given reactor volume allows 40 wafers for the rotary disc, 20 wafers for a barrel, and 10 wafers for a pancake reactor. In addition, the rotary-disc reactor capacity can be expanded by adding more length to the stack array. Expansion in wafer diameter is restricted only by the ability to uniformly heat the wafer.

(2) The higher wafer loading capacity in the rotary-disc reactor allows for higher chemical efficiency in use of gases and source chemicals and lower power consumption per wafer. Our work has shown that at 1-μm/min growth rate, the hydrogen consumption per wafer is one-half that of barrel reactors and power consumption is one-third.

(3) Thickness and resistivity uniformity can be controlled in the rotary-disc reactor by adjusting each region of the stack array. This feature, along with the ability to replace discrete parts of the susceptor array, gives this reactor a cost effective advantage over other types of reactors that use a single unified susceptor for a multitude of substrates.

4.2. Operational Growth Characteristics

The rotary-disc reactor has several variables some of which are not found in other reactor types. Apart from temperature, silicon-source

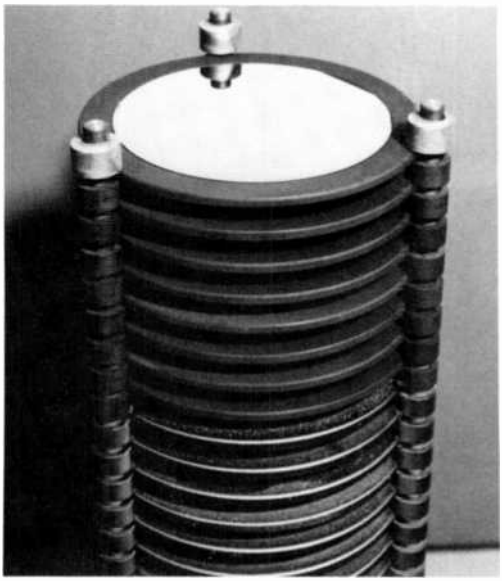


Fig. 7—Rotary-disc susceptor stack.

concentration, and substrate diameter, one must consider spacer distance between susceptor rings, ring diameter, distributor-tube slot width, gas velocity and positional direction of the gas stream at the time of growth. These variables were explored to optimize the uniform growth of 20-μm-thick layers over large area substrates.

4.2.1 Temperature

The temperature of each susceptor location is controlled by adjusting both the exterior rf load coil turns and the spacing between susceptor rings. Since the temperature of the substrate during growth is largely responsible for the growth rate, temperature uniformity is one of the parameters necessary for thickness uniformity wafer to wafer.

4.2.2 Spacer Distance

As in the case of temperature, the spacer distance between wafers is important for growth rate uniformity. This parameter is unique in the rotary-disc reactor and, therefore, gives an additional degree of freedom in establishing growth uniformity, along with adjustment of conditions for the temperature profile. For example, a wider

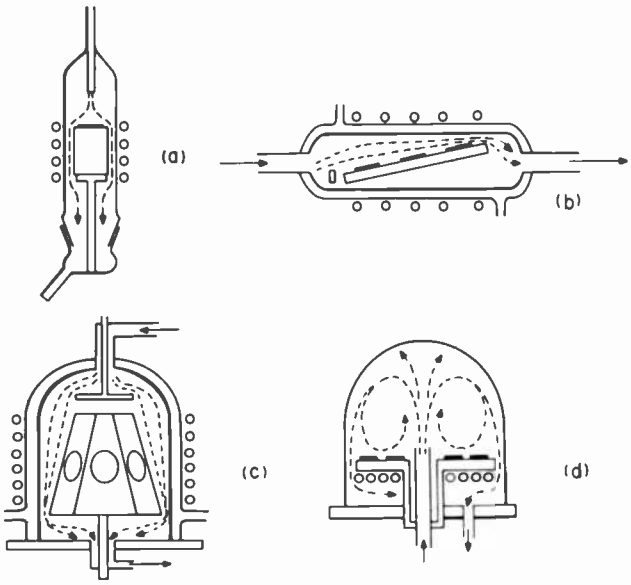


Fig. 8—Four conventional reactor designs.

spacing allows more source gas to enter between the susceptor rings and therefore increases growth rate. This spacing option allows the adjustment of growth rate locally for a small temperature variation in the stack to achieve overall growth rate uniformity on all wafers.

4.2.3. Susceptor Ring Width

The width of the susceptor ring is useful in controlling gas stream conditions as the gas enters the susceptor stack. A wider ring allows for more gas heating and the establishment of proper boundary conditions before the source gas encounters the substrate. Ability to control this unique rotary-disc parameter has significantly contributed to achieving thickness uniformity from center to edge on the wafer.

4.2.4. Distributor-Tube Slot Width and Gas Velocity

The width of the distibutor tube slot is used to choose the spread angle of the gas exiting the slot and the volume of gas delivered to the stack. These conditions are controlled to yield the desired gas velocity component for proper growth rate magnitude and uniformity.

4.2.5. Gas Directional Control

During epitaxial growth, the directional position of the gas stream is controlled by either sweeping the slot side to side or holding the stream direction pointed at a particular part of the rotating wafer for a period of time. This permits a control of the gas direction over the wafer which results in a more uniform growth rate. The work done here has been directed at optimizing these operational growth characteristics for maximum growth rate, growth rate uniformity from wafer to wafer and from center to edge of the wafer, and extension of batch size to yield greater throughput of wafers.

4.3. Results Using the Rotary-Disc Reactor

Runs made with a loaded stack of 40 three-inch-diameter single-crystal CZ wafers gave resistivity uniformity ±10%. Center-to-edge thickness uniformity for the wafers was ±6% and wafer-to-wafer thickness uniformity was ±10%. These specifications are well within the requirements for epitaxial solar cells. Selected solar cells were fabricated from the epitaxial wafers in one run by a diffusion step to form the junction and then evaluated for cell characteristics (Fig. 9). These data showed good uniformity of cell efficiency in the 9.5 to 10.7% range.[13]

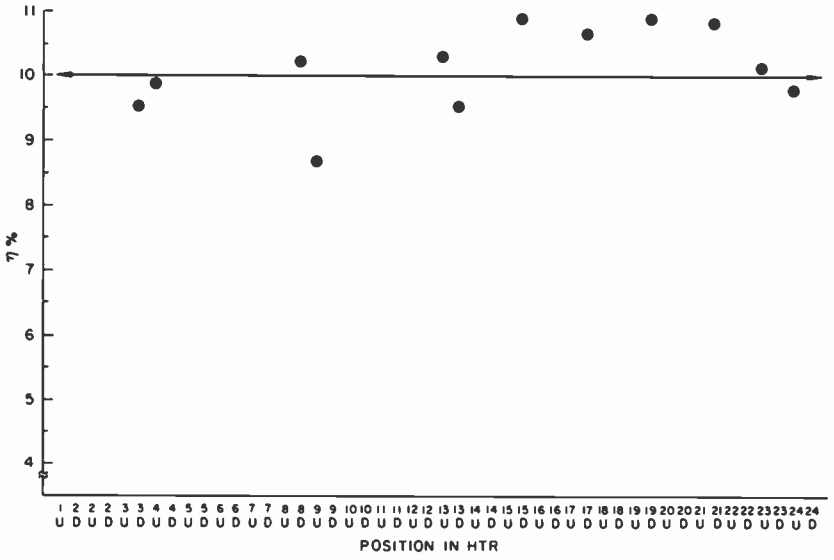


Fig. 9—Solar-cell efficiency for HTR.

In addition, the reactor was used to evaluate 10-cm × 10-cm square substrates. The equipment size restricted the stack capacity to ≈10 wafers, but enabled us to evaluate the conditions for uniform growth. A novel distributor tube was developed, and the susceptor design was modified to optimize the growth parameters. Results showed the growth on 100-cm² area wafers gave thickness variations of ±5% on all points of the wafer.

Experimental runs were also made in which 7.6-cm-diameter control CZ wafers were mixed with MG/HEM substrates. The averaged results for five such runs are given in Table 5. About 60% of the cells made on HEM substrates from ingot 010 showed shunting effects that were traced to the high particle content of this ingot. This accounts for the low values of open-circuit voltage (V_{oc}) and fill-factor (FF). In contrast, only 20% of the cells from ingot 018 exhibited obvious particle-related effects. Comparison of the three best 42-cm² area cells with the 2-cm² cells also from ingot 018 shows that only the fill-factor is lower for the large-area cells. The solar-cell values obtained for the control CZ wafers are similar to those obtained in runs in which no MG/HEM material was included, indicating that cross-contamination from the MG material during epitaxial growth is not a problem.

5. Discussion and Conclusions

This paper has described ingot solidification of MG silicon to form substrates for the fabrication of epitaxial solar cells. Epitaxial growth conditions, solar-cell results, and the development of an advanced epitaxial reactor configuration have been discussed.

In ingot solidification, it was found that the HEM process could be used to form large almost single-crystal ingots from commercial grade MG feedstock. The major problem experienced with most of the MG feedstocks was silicon carbide particle formation and retention in the ingots. The HEM process was found to be insensitive

Table 5—Average Cell Parameters for Five HTR Runs

Substrate	J_{sc} (mA/cm²)	V_{oc} (mV)	FF —	η_{ar} (%)	Cell Area (cm²)
Control (CZ)	24.01	579	0.75	10.5	42
Ingot 010 (Foreign Source MG)	22.15	538	0.52	6.2	42
Ingot 018 (So. African MG)	23.13	570	0.62	8.2	42
Ingot 018 (Best 3, no particles)	23.2	576	0.65	8.7	42
Ingot 018 (2-cm² cells)	23.4	581	0.79	10.7	2

to the presence of the particles in that breakdown of crystallinity during ingot growth did not occur at particle sites, but rather twins are sometimes formed that propagate from particle locations. Twins generally do not adversely affect solar-cell performance, but particles inside a cell area cause severe shunting of the solar-cell output, thus limiting the yield of useful substrate material. Particle density and location in HEM ingots solidified from several MG sources were characterized. The particles were identified as SiC with complexing of heavy metals in their vicinity, and their source was found to be in the MG feedstock and not from the crucible walls or HEM equipment. In general, the particles in a completed ingot were confined to the top one-fourth to one-third of the ingot volume and sometimes also near the bottom.

Three methods were found that significantly reduced the particle density. Of these, selection of a MG feedstock low in carbon and iron was the most effective. Double solidification was also important in reducing particle content and further confining them to very near the top of the ingot. The observation that the particle problem was reduced when larger (10-kg) ingots were solidified has positive implications for large-scale production by this method.

In the absence of particles, the HEM material was found to be a suitable substrate for the fabrication of epitaxial layers and solar cells. Reasonably high efficiency (10–12%) solar cells were made in layers grown on substrates made from several sources of MG silicon.

The rotary-disc reactor described here has demonstrated the capability of high throughput of wafers and expansion to large-diameter wafers. This work has demonstrated that the reactor can be used to grow on both round and square wafers, and is compatible with the use of MG derived substrates. In the particular equipment used, which has size limitations, a 40-wafer stack was demonstrated for 7.6-cm round wafers and a 30-wafer stack for 10.1-cm round and 7.1-cm square (10-cm diagonal) wafers. Limited results on 10-cm square (14.2-cm diagonal) wafers indicate no technical limitations to prevent future stack size extension to 40 or more such wafers. No significant differences in thickness, electrical, or solar-cell parameters were observed in comparing upfacing with downfacing wafers, and along the length of such stacks.

The work described here has resulted in considerable progress in the development of the several technologies needed for the production of efficient solar cells using a process starting with raw MG silicon. With additional development, this process holds great promise for commercial application.

Acknowledgment

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Electron-Flood Techniques to Neutralize Beam Charging During Ion Implantation

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Abstract—The problem of beam charging and charge damage on wafers during ion implantation is reviewed, and beam-charge neutralization by electron-flood techniques is examined. The operational characteristics of such a system installed in a Varian/Extrion CF4 ion implanter is reported for different ions, energies, and beam currents, and its effects on implant dose accuracy are discussed. Data for complete neutralization of beam charging are presented, and slight overflooding with electrons is recommended. Finally, some more subtle effects of ion-beam charging on the dielectric properties of thin oxide layers in test devices have been investigated, and the benefits of using electron flood are demonstrated.

1. Introduction

The implementation of ion implantation in silicon devices and circuits was delayed in the 1960s until high-temperature post-implant annealing was demonstrated to be effective in removing crystalline damage associated with implantation.[1] In the 1970s, ion implantation became a standard production technique, particularly for low-dose implant applications such as threshold adjust for MOSTs, substrate or well doping, resistors, and the base region of bipolar transistors. In recent years, with the availability of medium- (~1-mA) and high-current (~10-mA) ion implanters, ion implantation has become the only doping technique used in the fabrication of many devices and circuits. For example, advanced CMOS ICs rely on ion implantation for doping of both source/drain and polysilicon gates and interconnects.

In these applications, the very high rate of charge deposition and induced charges on the surfaces of 3- to 4-inch-diameter wafers can cause serious damage to the wafers and the devices or circuits on them,[2-3] ranging from degradation of dielectric properties (such as breakdown voltages and/or noisy higher leakage currents) to shattering of wafers due to electrical arc discharge. Beam charging can cause wafer stickiness in automated wafer transfer systems and electrostatic attraction of dust particles; charge damage on wafers during implantation obviously affects product yield, performance, and/or reliability. Both, therefore, deserve serious attention so that they will not remain as obstacles in many high-current implant applications. Electron flood has emerged as a practical solution to neutralize the positive charges deposited or generated by the ion beam on the surface of a wafer, which is either an insulator or is partially covered by an electrically insulating film such as SiO_2, Si_3N_4, or photoresist.

2. Beam Charging

When a positively charged ion beam hits the surface of a silicon wafer, secondary electrons as well as sputtered neutral, positively ionized, and negatively ionized atoms, photons, and absorbed gas molecules are emitted due to energy transfer from the incident ions to the target surface. At ion energies typical for ion implantation, the secondary electron emission coefficients are of the order of 2–20.[4] The secondary electrons are prevented from traveling up the beam line by a negative biased suppressor ring (~ -500V) at the entrance to the Faraday cup, and many of them are captured by the space-charge potential of the ion beam until the beam is again space-charge neutralized. For low-current ion beams ($\lesssim 50$ nA), which are electrostatically scanned over the target surface, the return of all secondary electrons to the target area is usually sufficient to prevent beam charge damage (even for dielectric wafers) as long as the ion beam is over-swept on the target and covers the perimeter of the target holder, which is electrically conductive and is connected to ground through a low-impedance charge integrator. However, as the current levels of ion beams increase, coupled with wafer sizes of 4 inches or more, a rapid buildup of positive charge on the target surface can result if the target is nonconducting, leading to electrical arc discharge and physical damage to the devices and circuits on the wafer (Fig. 1).

It should be pointed out that even for implanters designed with space-charge neutral ion beams, such as the NV 60-10 implanter

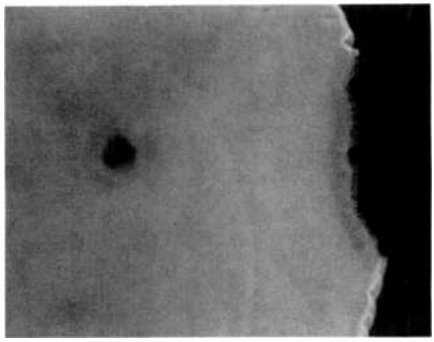

Fig. 1—Photomicrograph of damage to devices due to electrical arc discharge during ion implantation. Magnification 200×.

by Nova/Eaton, the loss of secondary electrons from the surface of an electrically insulating layer can result in a buildup of positive charges[13] on the order of a few tens of volts, sufficient to cause dielectric breakdown in 300-Å-thick gate oxides used in advanced circuits. Moreover, beam charging also causes perturbation of the beam profile and substantial inaccuracies in both the dose integration and implant uniformity. Under these conditions, the target surface must be neutralized.

3. Beam-Charge Neutralization

There are three main methods to space-charge-neutralize a steady-state ion beam for efficient beam transport. They are

(a) electron and secondary electron injection into the beam from an external source,
(b) electron flow into the beam via a plasma bridge, and
(c) electron production within the beam by ionization of a low-pressure gas.

These methods have been analyzed in detail by Holmes[5] who concluded that gaseous neutralization (c) is the most superior (99% efficient), followed by method (b) (97%) and method (a) (60–90%).

Gaseous neutralization of the beam charge is not a practical approach for ion implanters, however, since it requires an extremely long Faraday cup for adequate electron generation rate. A plasma bridge emitter[6] has been shown by Ward and King to reduce the space-charge potential in a 500-mA ion beam to less than 40 V. Its disadvantages are a high neutral gas flow and potential for target contamination. The method used for neutralizing ion beam charge

in commercial ion implanters is electron flooding of either the target surface or of the ion beam within the target Faraday system. We will limit our discussion in this paper to the effect of the Extrion/ Varian electron-flood system on medium current implanters (DF4/ DF5), its operation, characteristics, and effectiveness.

4. The Extrion Electron-Flood System

The Varian/Extrion electron-flood system is designed to neutralize the charge in the ion beam by passing it through a cloud of low-energy electrons after the Faraday system has measured the actual beam current for dose control purposes. Fig. 2 shows a diagram of the electron-flood system within the Faraday cage. The heart of the system is the electron-flood gun, which consists of a tungsten filament and reflector plate biased at $-350/-600$ V with respect to the Faraday cage. When the filament is heated, electrons are emitted from the surface and are accelerated up to 350/600 eV toward the walls of the Faraday assembly, producing more secondary electrons with a mean energy of just a few electron volts. The ion beam traps the electrons it needs to neutralize the effect of its own net charge, and the rest of the electrons strike the Faraday walls and return to the flood gun circuit. Most of the low-energy electrons trapped in the ion beam do not neutralize the ions to form neutral atoms, but follow spiral paths of their own and can travel in either direction in the ion beam. When the ion beam strikes a dielectric and pro-

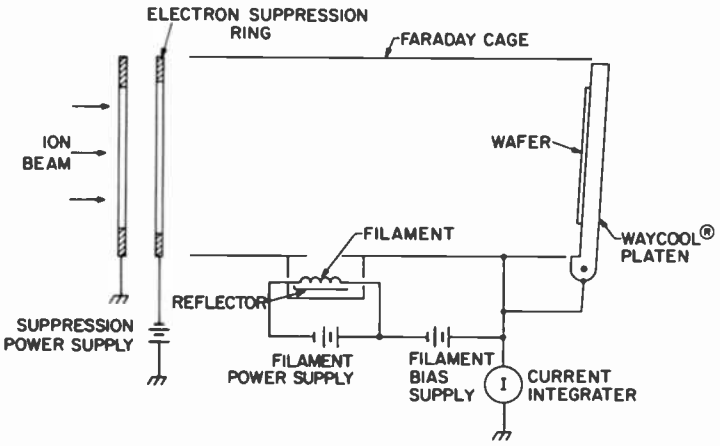

Fig. 2—Schematic diagram of the Varian/Extrion electron-flood system within the Faraday cage.

duces a static charge, these trapped electrons in the beam are immediately attracted to that charge to neutralize it.

The electron-flood gun is located near the ion beam entrance of the Faraday assembly; there is no direct line of sight between the tungsten filament and the target area. This ensures that damage to semiconductor by high-energy electrons is avoided, as is direct contamination from the electron-flood gun filament.

Electron-flood gun emission current is adjustable from 0–5 mA (DF4/DF5) and 0–15 mA (DF4-3000). Obviously a higher electron-flood emission current is required when a higher beam current is used for the implantation. Varian/Extrion[7] recommends that the electron-flood emission current be roughly 10 times the ion beam current for beam currents above 100 μA for DF4/DF5 implanters; at ion beam currents below 100 μA, they recommend that the electron flood not be used.

5. Experiments with Electron Flood on DF4 Implanters

The use of a thin conductive film such as 100-200 Å of aluminum[8] over dielectric materials has been reported to prevent dielectric breakdowns during ion implantation, leading to devices and resistors with lower popcorn noise. Apart from the extra processing steps that this generates, the thin aluminum film can create two problems, namely, thickness variation across the wafer and poor step and corner coverage. Thickness variation leads to poor control of the amount of ions implanted into the silicon, and poor step and corner coverage can lead to catastrophic damage due to electrical arc discharge. Fig. 3 shows a photomicrograph of a device with arcing damage in the SOS wafer after a source/drain $^{11}B^+$ implant at 40

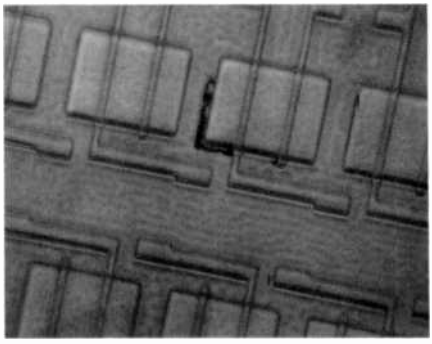

Fig. 3—Photomicrograph of a device covered by 200-Å aluminum showing arcing damage after a source and drain $^{11}B^+$ implant.

keV to a dose of $2 \times 10^{15}\,cm^{-2}$ in an Extrion 200-DF4 ion implanter, despite a 200-Å aluminum coating on the wafer during the implantation. No evidence of any arcing had been observed when a similar lot of wafers was implanted with a beam current of 100 μA and an electron-flood emission current of 1 mA. However, arcing damage returned even with electron flooding of the ion beam when the 200-Å aluminum conductive coating was eliminated, indicating that charge-induced damage was still taking place in spite of the electron flood.

Experiments designed to test the efficiency of the electron-flood system on DF4 implanters were carried out. We measured the voltage on a $1^1/_2$-inch-diameter aluminum electrode on top of an insulating 3-inch-diameter sapphire substrate while it was being implanted in the implanter with the electron-flood system turned on. This was accomplished with a vacuum electrical feedthrough installed in the target chamber of the ion implanter.

Fig. 4 shows a picture of the test target with a piece of thin wire attached to the backside of the metal foil. Vinyl insulation on the part of the wire near the target was stripped off so that it would not charge up or out-gas when hit by the ion beam. The side wall of the Faraday assembly was removed and the special test target was lowered into the Waycool® wafer holder which was then clamped securely at the 7° implant position. The other end of the metal wire from the test target was then soldered to the vacuum electrical feedthrough and the side wall plate of the Faraday cup was carefully closed up again. A Fluke differential voltmeter, model 825A, was

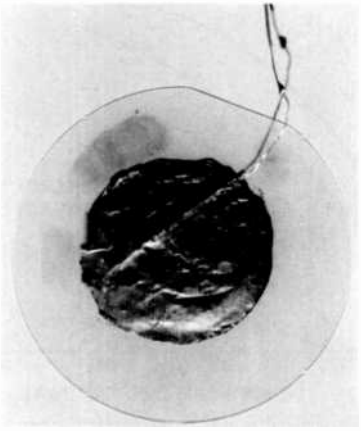

Fig. 4—A test target showing a piece of thin wire attached to the backside of the aluminum foil at the center of a 3-inch sapphire wafer.

used to measure the voltage developed on the metal electrode target with respect to machine ground when it was being implanted with or without the electron flood.

Using this experimental setup, it was observed, contrary to previous data from Varian/Extrion,[7] that the electron-flood system could in fact over-neutralize the positive charges from the ion beam, resulting in the target being charged negatively to about −10 V. Thus there exists an optimum electron-flood emission current for each combination of target, ion species, energy, and ion beam current at which the beam charging at the target is completely neutralized. Furthermore, it was observed that the optimum electron emission current was also a function of ion-beam tuning and the geometry of the Faraday assembly. A highly diffused ion beam (de-tuned) required less than a fifth of the electron-flood emission current for complete target neutralization as compared to a tight and well-tuned ion beam. Thus, data were recorded only after optimum ion-beam tuning was achieved under each of the conditions.

Fig. 5 shows the electron filament emission current (I_{EF}) for complete neutralization of target charging by $^{11}B^+$ ion beams at 50 keV and at 150 keV, as a function of scanned beam current (I_B). The data was obtained with the low bias mode (−350 V) on the electron gun. (The high bias mode, −600 V, was found to be disastrous unless the suppressor ring at the entrance to the Faraday cup is biased at more than −600 V instead of the usual −500 V to prevent the

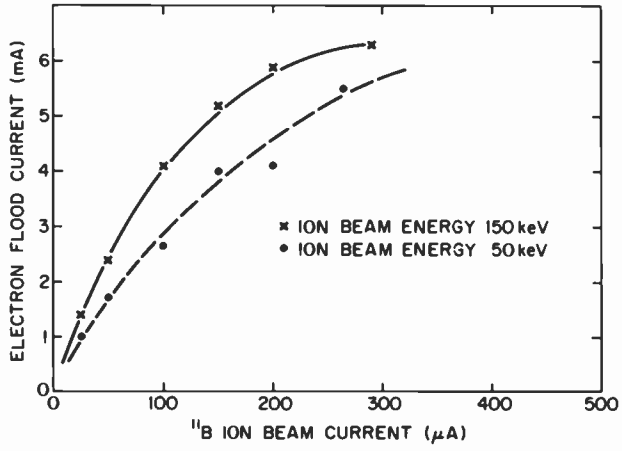

Fig. 5—Electron filament emission current for complete neutralization of target charging by $^{11}B^+$ beams at 50 keV and at 150 keV as a function of scanned beam current.

escape of electrons.) It can be seen that below I_B ~100 μA, I_{EF} is a linear function of the ion-beam currents, and above I_B ~200 μA, I_{EF} starts to show saturation effects. Attempts to obtain data for I_B above 300 μA for the $^{11}B^+$ ion beam failed for two reasons. First, in the presence of ~6 mA of electron-flood current, the ion beam would not stay tuned on a DF4-3000 implanter. Second, the entire Faraday assembly became so hot from the heat radiated from the electron gun tungsten filament that the target wafer clamped onto a Waycool® holder cracked due to the temperature difference between the two sides of the wafer. This indicates that the entire Faraday assembly needs to be Freon®-cooled for operation of the electron-flood option above 6-mA emission current. There is also a high potential for target contamination when the entire Faraday assembly becomes heated.

The dependence of I_{EF} on the ion energy is clearly obvious from the data shown in Fig. 5 and was investigated further at constant I_B = 100 μA and at I_B = 200 μA. The results are shown in Fig. 6. For $^{11}B^+$ ion energy below 50 keV, I_{EF} has a strong dependence on E_I, the kinetic energy of the impinging ion. At energies above 100 keV, I_{EF} has only a weak dependence on E_I. This is in qualitative agreement with the experimental ion-induced secondary electron yield coefficient γ from aluminum when bombarded by ions,[4] which value increases rather steeply with ion energies below 50 keV. Clearly, for a higher value of γ, more flooding electrons are needed for charge neutralization at the target surface. Similar curves of I_{EF}

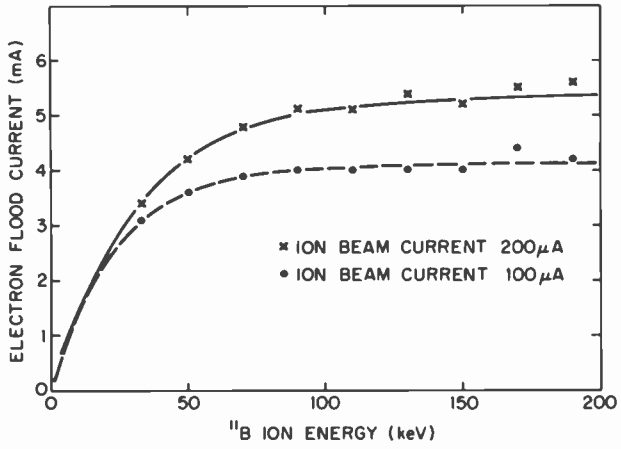

Fig. 6—Electron filament emission current for complete neutralization of target charging by $^{11}B^-$ beams as a function of ion energies.

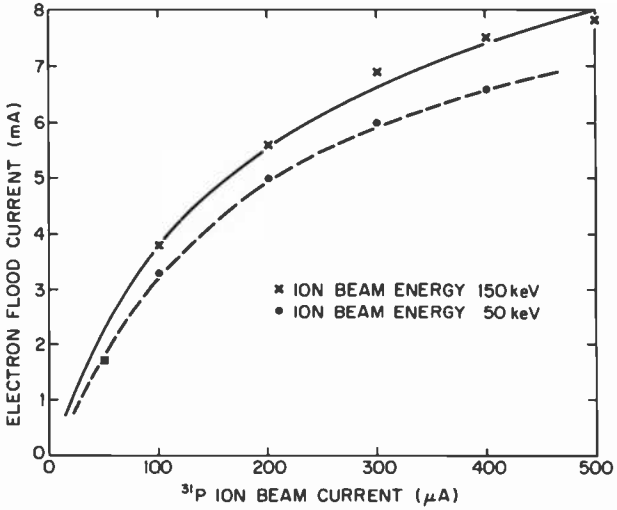

Fig. 7—Electron filament emission current for complete neutralization of target charging by $^{31}P^+$ beams at 50 keV and at 150 keV as a function of scanned beam current.

versus I_B and I_{EF} versus E_I have been obtained on a DF4-3000 implanter for $^{31}P^+$ and for $^{75}As^+$ ions. These are shown in Figs. 7, 8, 9 and 10.

An experiment was also performed to investigate the effects of the test target material on the optimum electron-flood emission current, I_{EF}. A similar test target with a silver electrode instead of aluminum was used for the experiment. The results of the experi-

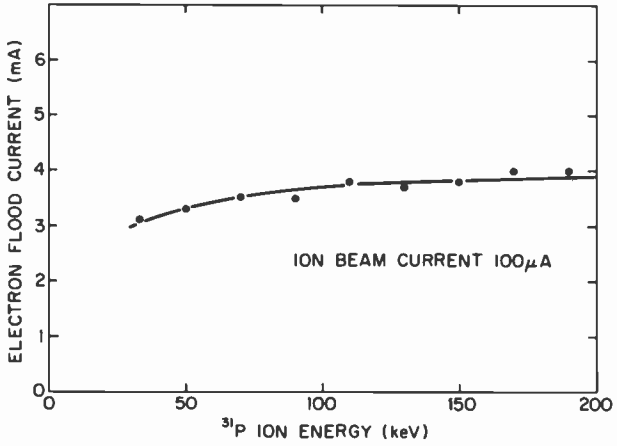

Fig. 8—Electron filament emission current for complete neutralization of target charging by $^{31}P^+$ beams as a function of ion energies.

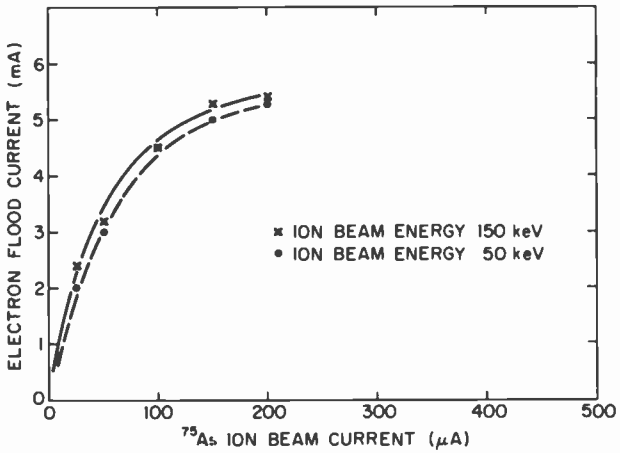

Fig. 9—Electron filament emission current for complete neutralization of target charging by $^{75}As^-$ beams at 50 keV and at 150 keV as a function of scanned beam current.

ment are depicted in Fig. 11, which shows I_{EF} versus I_B for $^{31}P^+$ at 150 keV for the two different target materials, aluminum and silver. Silver is known to have a higher ion-induced secondary electron emission coefficient, γ. However, the other factor that must be considered is the effective electron-induced secondary electron emission coefficient, δ_e, since the target is simultaneously bombarded with electrons trapped in the ion beam. These electrons moving with the ion beam could have effective energies of 100 eV or more due to the

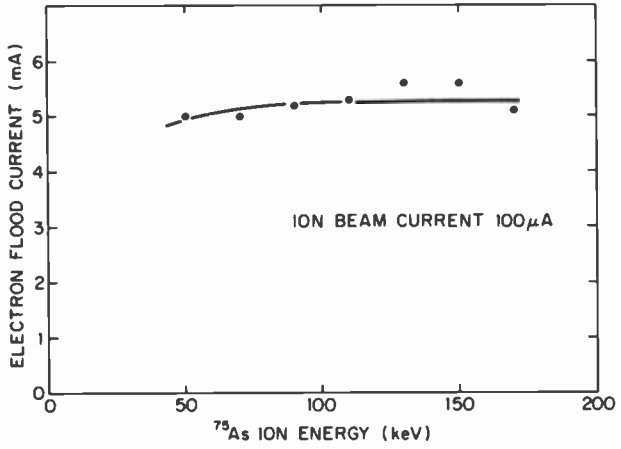

Fig. 10—Electron filament emission current for complete neutralization of target charging by $^{75}As^-$ beams as a function of ion energies.

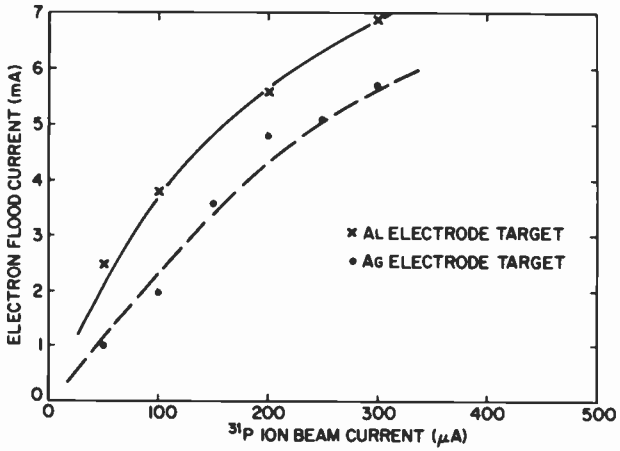

Fig. 11—Electron filament emission current for complete neutralization of target charging as a function scanned $^{31}P^+$ beam at 150 keV for two different target materials, aluminum and silver.

effects of the electron suppressor ring biased at −500 V and to the motion of the ions. For perfect charge compensation, we must have

$$J_i (1 + \gamma) = J_e (1 - \delta_e), \qquad [1]$$

where J_i is the current density of the incident ions and J_e the current density of electrons incident on the target. Thus,

$$J_e = J_i \frac{1 + \gamma}{1 - \delta_e} . \qquad [2]$$

We see that J_e is more critically dependent on δ_e than on the value of γ, and it is not trivial to determine a priori whether a different target material may require more or less electron gun emission current for complete charge compensation. Should δ_e be larger than unity, which is common for many insulators for $E_e > 200$ eV, perfect charge compensation can never be achieved for any value of J_e or, hence, I_{EF}.

During an actual implantation of silicon device wafers, it is very difficult, if not impossible, to achieve perfect charge neutralization on the surfaces of the wafers being implanted, since, apart from the values of γ and δ_e, the area ratios of surfaces covered by SiO_2, Si_3N_4, or Al_2O_3 to exposed silicon are not readily available. The data presented here are meant only as a guideline for setting the optimum electron-flood emission currents to neutralize beam charging during implantation. As long as adequate beam-shape can be maintained, overflooding by 10–20% is much safer than underflooding. Our ex-

periments showed that overflooding did not cause negative charging of our capacitor target by more than -5 to -10 V, which is roughly the mean energy of the secondary electrons from the walls of the Faraday assembly.

As a finalè to the series of experiments reported here, an attempt was made to determine the voltage on the test target without electron flooding when implanted with an $^{75}As^+$ ion beam at 100 keV. Theoretically the target should charge up to 100 kV. Experimentally, the target disintegrated in a couple of seconds before any steady state was reached!

6. Implant Dose Accuracy with Electron Flood

Dose accuracy tests were performed by implanting wafers with $^{31}P^+$ ions at 100 keV with a scanned beam current of 100 μA and with or without the electron-flood system turned on at 5-mA electron filament emission current. The doses implanted were 10^{15} cm^{-2} in both cases. The test wafers were capped with ~0.5 μm of deposited SiO_2 and then furnace-annealed at 1000°C for 30 minutes in dry nitrogen ambient. Resistivity measurement by four-point probes showed that samples implanted with and without the electron flood were 76.9 ± 2.0 Ω/sq. and 77.1 ± 2.0 Ω/sq., respectively. The theoretically predicted value[12] for these implants is 75.5 Ω/sq., which agrees well with the measured values.

7. Effects of Electron Flood on Test Devices

The potential benefits of using electron flood were investigated in advanced CMOS technologies in which polysilicon is used as a mask for ion implantation for self-aligned source and drain regions. Osburn et al.[9] reported recently on the phenomenon of edge breakdown of polysilicon gates over thin oxides during ion implantation, and attributed the effect to ion beam charging of the gates during ion implantation. Their results indicated a dramatic decrease in the average dielectric strength of the gate oxide as a function of $^{75}As^+$ implantation dose above 10^{15} cm^{-2}. Using thin oxide capacitors with $POCl_3$ diffusion-doped polysilicon electrodes, we were able to monitor the more subtle effects of the damage to the thin oxide by beam charging with and without the use of the electron-flood system.

A schematic diagram of the monitor capacitor is shown in Fig. 12. The starting wafers were 3-inch-diameter, n-type, 0.1 Ω-cm Czochralski silicon wafers, and were cleaned in SC1 and SC2 solutions[10] prior to the growth of 2000-Å field oxide. Another 700 Å of thermal

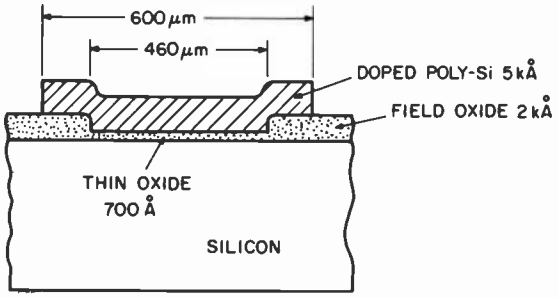

Fig. 12—Schematic diagram of a test capacitor used for monitoring the effectiveness of the electron flood.

oxide was grown after the field oxide was photolithographically defined and etched. A polysilicon electrode film was then deposited by LPCVD, later doped by $POCl_3$ to obtain a sheet resistivity of ~15 Ω/sq. in 0.5 μm of poly, and defined to provide overlapping of the field oxide region.

The dielectric properties of the SiO_2 underneath the polysilicon electrode right after fabrication were investigated by measuring the leakage current as a function of bias voltage of the polysilicon-SiO_2-Si capacitor shown in Fig. 12. The leakage currents were measured by a Keithley Model 26000 picoammeter and log(I) versus bias voltage were recorded on an x–y recorder. The ramp voltage rates were kept at 0.3 V/sec. The measurements were repeated on the same devices after implantation with 200 μA of $^{75}As^+$ ions at 100 keV to a dose of 4×10^{15} cm^{-2} with and then without the use of the electron flood. Care was taken not to bring the devices close to catastrophic breakdowns during each measurement. A total of 100 devices was monitored. About two-thirds of the devices survived both implantations with little or no degradation in leakage currents, as shown in Fig. 13. The slightly lower leakage currents at low voltages before the onset of leakage currents due to Fowler-Nordheim tunneling of electrons[11] is probably due to humidity or simply curing of the devices in a vacuum target chamber for the ion implantations. The catastrophic oxide breakdown voltages are in the neighborhood of 50–60 V and are not shown in Fig. 13. However, about one-third of the tested devices exhibited marked changes in the dielectric properties of the thin oxide, apart from lower field breakdown voltages that were already reported.[9]

Typical results in this group are shown in Fig. 14. The leakage currents after ion implantation are no longer a smooth function of bias voltage, and spikes in leakage current appear after ion implantation, even with the use of the electron flood, since perfect

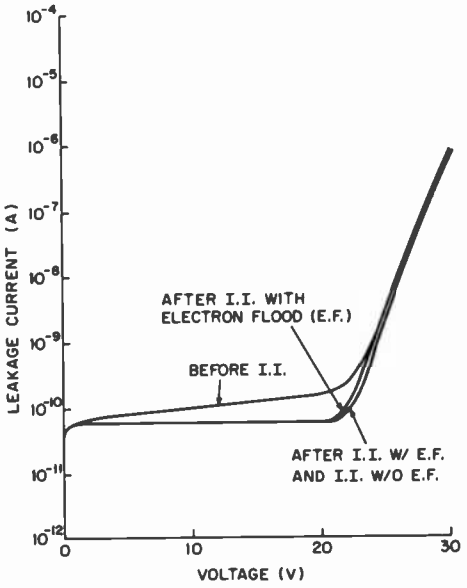

Fig. 13—Plot of log I vs voltage for the majority of monitor capacitors before ion implantation, after ion implantation with electron flood, and after ion implantation without electron flood.

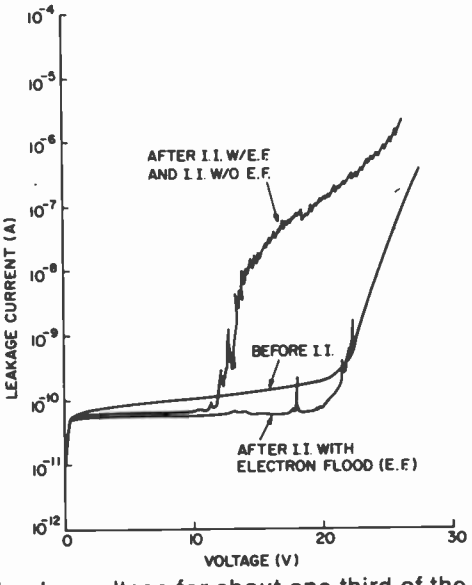

Fig. 14—Plot of log I vs voltage for about one-third of the monitor capacitors before ion implantation, after ion implantation with electron flood, and after ion implantation without electron flood, showing degradation due to beam charging.

beam charge compensation was most likely not achieved. It can be seen that the damage to the thin oxide film due to beam charging of the polysilicon electrode is much more severe after implantation without the electron flood. Subsequent annealing at 450°C for 30 minutes in dry nitrogen showed that this is not due to an unannealed radiation effect. The subtle changes in the dielectric properties of oxide films are responsible for poorer device performance, apart from lower breakdown voltages, such as higher popcorn noise. The test capacitors that show these subtle changes in dielectric properties after ion implantation cannot be distinguished by outward appearances from the rest of the devices on the wafer. There are no obvious damages due to arc discharge, and attempts to examine defects in these damaged devices under an infrared microscope were not yet successful. When the monitor capacitors were increased to 150-mil diameter, the capacitor electrode collected enough beam-induced charges during ion implantation to cause damages that were easily observable under ordinary microscopes, as shown in Fig. 1.

8. Conclusions

In summary, the problem of beam charging and charge damage on wafers during ion implantation has been reviewed, and beam-charge neutralization by electron-flood techniques was examined. The operation characteristics of an electron flood system in a Varian/Extrion CF4 ion implanter have been studied. Data for complete neutralization of beam charging for different combinations of ions, energies, and scanned beam currents have been obtained. Slight over-flooding is recommended, as well as cooling of the entire Faraday cage, when using electron flood during ion implantation. Finally, the effects of beam charging during ion implantation on the dielectric properties of thin oxide layers were investigated using monitor capacitors, and subtle increases in the leakage current as well as occurrence of numerous spikes were observed and reported. The elimination or reduction of these adverse effects by using electron flood during ion implantation should improve product yield, performance, and reliability in VLSI circuit fabrication.

Acknowledgment

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Crystal Growth of Mode-Stabilized Semiconductor Diode Lasers by Liquid-Phase Epitaxy

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Abstract—A brief description of the liquid-phase expitaxial (LPE) process and the LPE growth equipment required for diode-laser fabrication is presented. Planar-geometry laser structures are described as a preamble to the treatment of complex mode-stabilized devices. LPE growth over nonplanar substrates is discussed and presented as the *major* technique for the fabrication of low- and high-power, single-mode, reliable diode lasers. Major types of single-mode AlGaAs/GaAs and InGaAsP/InP laser structures are also presented.

1. Liquid-Phase Epitaxial Growth

Liquid-phase epitaxy (LPE) is a single-crystal growth process where precipitation of material from a supersaturated liquid solution occurs onto a substrate having a crystalline structure similar to that of the precipitate. The liquid solution must consist of at least two components, one of which is the solvent (usually a group III element) and the other the solute. As a saturated solution is cooled to a lower temperature, the solution becomes supersaturated, causing precipitation of the solute from the solution. Due to energy considerations, growth or precipitation is preferred on substrates having the same or similar lattice constants as the solute. Large differences in lattice parameters will result in polycrystalline growth where the substrate plays only a small role in the initial nucleation of the growth.

Over the last 20 years liquid-phase epitaxy has emerged as the major technology for the fabrication of optoelectronic devices. These devices include light-emitting diodes (LED), solar cells, and double-

heterojunction (DH) injection lasers. LPE is also used in the fabrication of microwave devices such as Gunn oscillators, IMPATT diodes and field-effect transistors (FET).

The liquid-phase epitaxial growth method was originally developed at RCA Laboratories by Nelson[1] in 1963. His technique employed a furnace that could be tipped in such a manner to allow a liquid solution to roll onto a substrate under preset growth conditions. This technique yielded grown epitaxial layers with large variations in thickness across the substrate and poor substrate surface morphology. A "dipping" technique[2] was soon developed to overcome these problems and improve the quality of the grown layers. In the "dipping" technique a substrate is immersed or floated on a melt usually heated in a vertical-furnace growth system. Substrates were then grown with uniform layer thickness and good surface morphology. However, only a single layer could be grown at any one time. Thus, the "multibin" technique[3–5] was developed for the growth of successive layers. The "multibin" technique consists of sequential positioning of a substrate under saturated melts contained in bins inside a high-purity graphite boat. The multibin technique is significant because it is well suited for the growth of very thin layers required in multiple-layer structures. It provided for the first time a way to initiate and terminate growth at precisely controlled times. Also, since the solutions are contained in individual bins separated by graphite walls, a clean wiping action is obtained as the melt is removed from the substrate, thus leaving behind mirror-like grown surfaces. These improvements also led to uniform composition and thickness control over relatively large areas. At the present time, the multibin technique is the most widely used liquid-phase epitaxial growth method.[6,7]

LPE growth is performed at temperatures well below the melting point of the solid and can thus avoid problems normally associated with very high growth temperatures. The composition of solvent and solute incorporated in the grown layer is determined by the phase diagram for that system. The phase diagram also provides the temperature range over which growth may occur. For example, the phase diagram for the GaAs system can be seen in Fig. 1. Binaries are not the only crystalline compounds that can be grown by LPE; ternary and quaternary compounds may also be grown. However, there are limitations since certain binaries used in the growth of ternary and quaternary layers are not always miscible. This leads to miscibility gaps[8] related to the lattice mismatch between the two systems. Therefore, for the case of two immiscible binary systems,

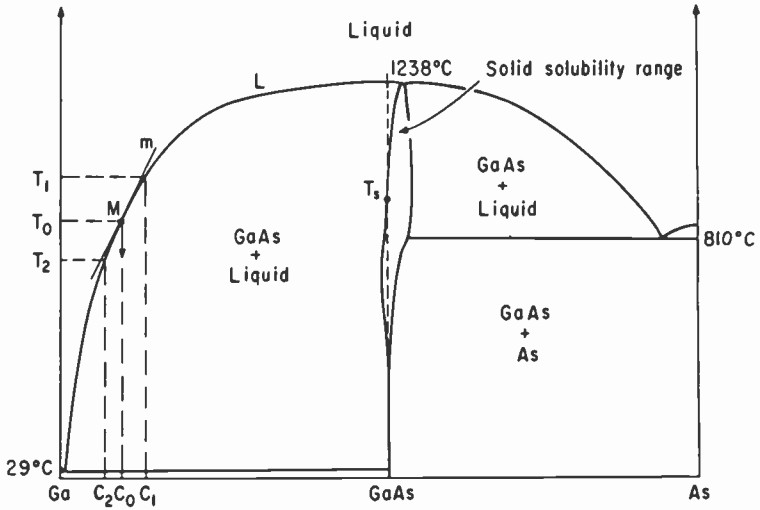

Fig. 1—The Ga-GaAs-As phase diagram for constant atmospheric pressure.

a solid precipitate of two binary phases results instead of one ternary phase.

The actual growth of the precipitate or layer is a nonequilibrium process. A driving force (Δenergy) for nucleation is necessary at the growing interface of the crystal to allow growth to take place. The driving force is usually due to a supersaturation condition resulting from the lowering of the temperature below the equilibrium condition given by the phase diagram or a concentration gradient across the melt because of localized depletion of the melt. Therefore, the actual transport of solute in the melt to the substrate is a diffusion process governed by the concentration gradient across the melt.[9] In addition, there may be convection effects present in the system. Thus, the rate limitations for LPE growth are a combination of both interface kinetics as well as liquid-phase transport mechanisms.

In the multibin technique two methods or types of crystal growth can be utilized[10] (see Fig. 2). The first method is called single-phase growth and, as the name implies, there is only a single phase present during the growth process. For LPE growth the single phase is the liquid. There are also different types of single-phase growth procedures called supercooling, step-cooling, and equilibrium cooling.[10] All three types require that all melt components be accurately weighed and heated to the exact temperature for saturation of the

melt. Any small differences will result in the melt being over- or under-saturated for growth. In the equilibrium cooling technique the substrate is brought in contact with the exactly saturated melt and then cooled at a fixed rate. The major problem with this method is that the substrate may be melt-etched or dissolved instead of grown upon. As mentioned previously, a driving force for nucleation is required for growth to occur. The step-cooling and supercooling techniques are used to create this driving force. The methods are similar in that the substrate and solution are at a temperature below the saturation temperature before the substrate is brought in contact with the melt. This temperature difference should be large enough to create a supersaturated condition, but not so large to cause spontaneous precipitation. At this point the substrate is brought in contact with the melt. The difference between the step-cooling and supercooling techniques is that the temperature differential is held constant for the step-cooling technique until growth is terminated, while for the supercooled growth the cooling of the melt continues at a fixed rate. The supercooling technique increases the driving force for nucleation causing it to occur more uniformly over the substrate surface, resulting in the growth of highly uniform layers.

Some of the problems associated with single-phase growth are demonstrated when LPE growth is perfomed on InP layers. The high vapor pressure of phosphorus over the solution results in a continual loss of material from the melt during the growth cycle. Thus, the composition of the solution will change with time and thereby change the saturation temperature of the melt. This problem makes it extremely difficult to obtain reproducible growth results using this method.

The-phase growth method (Fig. 2) is employed to compensate for this phosphorus loss during the growth. A solid phase of InP, usually in the form of a wafer, is floated on the melt surface resulting in a melt which will automatically be compensated for any phosphorus loss. The only disadvantage of this method is that the amount of supercooling which can be achieved is reduced because growth occurs on the InP material floating on the top surface of the melt as the melt temperature is decreased. Therefore, only a localized supersaturation condition is created for growth with this technique. However, this localized supersaturation is usually adequate for preventing the substrate from dissolving when it is first introduced into the melt, and thus uniform nucleation across the substrate surface takes place. This is the method most widely used today in the fabrication of material for multiple-layer structures. Fig. 2 il-

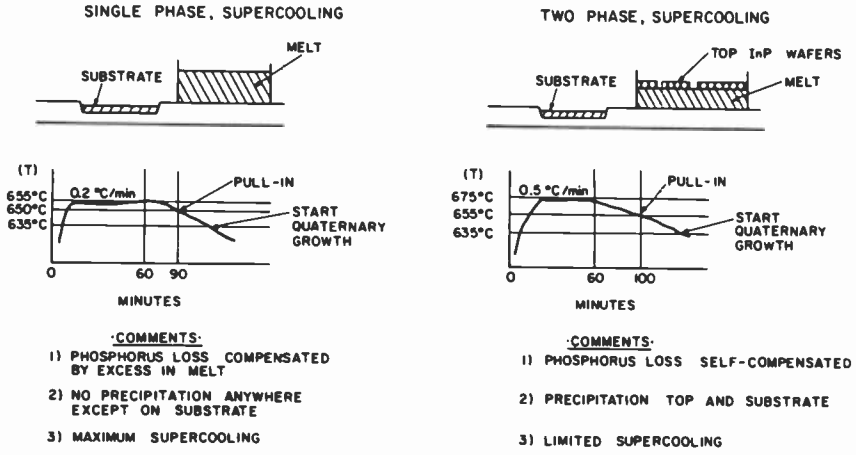

Fig. 2—Single-phase and two-phase LPE growth methods.

lustrates the difference in supercooling effects between single-phase and two-phase InGaAsP growths.

2. LPE Equipment

A block diagram of a liquid-phase epitaxy system is shown in Fig. 3. The high-purity quartz tube having one end closed contains the multibin graphite boat in which the actual growth takes place. The inert atmosphere of H_2 inside the quartz tube is provided by a hydrogen purifier. The vacuum connection is used to evacuate the H_2 gas lines during the start-up and shutdown of the hydrogen purifier. The high-purity nitrogen line allows the system to be flushed of the H_2 environment prior to opening the growth chamber to the atmosphere. All the gas lines and system parts except for the quartzware are made from #316 stainless steel. All valves and connections in the gas flow system are TIG welded wherever possible and metal-gasket sealed when not. The connection between the quartz tube and the stainless steel end plate is made with an O-ring seal. The top-slide, thermocouple and bottom-slide rods are made from high-purity semiconductor-grade quartz. They are used to position and move the graphite boat during the growth cycle. O-rings seal the quartz rods during positioning. The system is helium leak-tested to a leak rate of $\leq 1 \times 10^{-9}$ atm.cc/sec. The actual oxygen content in the gas stream is measured using a fuel cell and is routinely found to be ≤ 0.1 ppm.

The temperature control system controls temperature during the

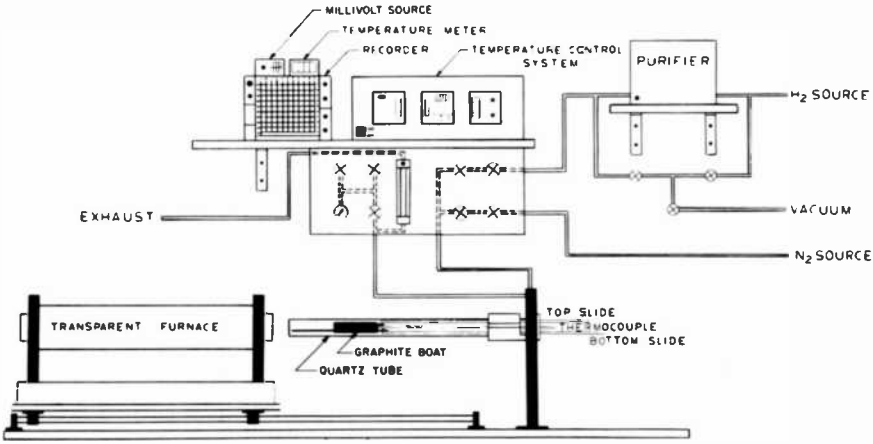

Fig. 3—Block diagram of an LPE system.

heat-up and cool-down of the semi-transparent gold furnace during epitaxial growth. The transparent furnace is mounted on a linear translation system to allow the furnace to be rolled on and off the quartz tube. This minimizes the amount of time the substrate is exposed to the H_2 ambient at the growth temperature. At this temperature the substrate surface is subject to thermal decomposition leading to the loss of the high-vapor-pressure element (usually group V) from the substrate. Excessive loss of the group V element will lead to a surface rich in the low-vapor-pressure element (usually group III) causing poor nucleation at the substrate-melt interface. The LPE-boat temperature is normally measured using a platinum thermocouple at the end of the boat, and is monitored in the system using a strip chart recorder and digital temperature meter. A photograph showing a crystal growth system used to grow long-wavelength InGaAsP lasers is shown in Fig. 4.

The LPE growth procedure is normally a two-step process consisting of a pre-bake step and the actual growth step. The pre-bake step involves loading the graphite boat with the melts, flushing the system with H_2 to remove any oxygen in the system, and baking them in the H_2 ambient at a temperature ~50°C higher than the actual growth temperature. This step is performed to remove any trace of oxide formation from the melts. If this oxide is not removed, it will react with the substrate during the growth step and impede nucleation at the substrate-melt interface. Prior to the growth step the graphite boat is loaded with the source and substrate wafers, then flushed with H_2 to remove any oxygen in the system. The quartz tube containing the boat is then inserted in the furnace and

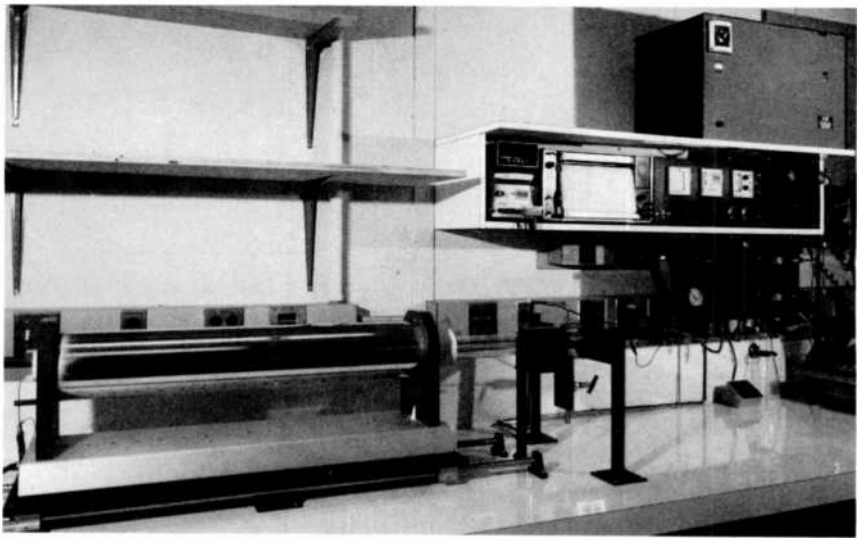

Fig. 4—Photograph of LPE system used for the growth of long-wavelength InGaAsP lasers.

heated to the growth temperature (~650–850°C). Fig. 5 shows a typical growth cycle for AlGaAs double heterojunction lasers. When the growth temperature is reached, the top sources are normally dropped from the top slider onto the melts by pulling the top slider from the graphite boat. The melts are then allowed to equilibrate with the sources for ~1 hour assuring that the melts are properly saturated for the growth temperature. The furnace is then programmed to cool down at a fixed cooling rate (~0.2–2°C/min). After a fixed amount of cooling the bottom slider of the graphite boat is moved using the quartz rod to position the substrate under the first melt. After a fixed growth time or temperature decrease, the bottom slider is moved once again to position the substrate under the second melt. This process is repeated during the cooling cycle until all the layers are grown on the substrate. After the growth is completed, the furnace is rolled off the quartz tube and the graphite boat is cooled with fans as quickly as possible to prevent decomposition of the grown substrate.

Fig. 6 is a photograph of a partially disassembled seven-melt boat showing the top and bottom sliders in their initial positions. This boat not only has a top source for each melt but also an additional source in the bottom slider that precedes the substrate into each melt and assures saturation of each melt just prior to growth being initiated onto the substrate.[3] The source wafers are dropped onto

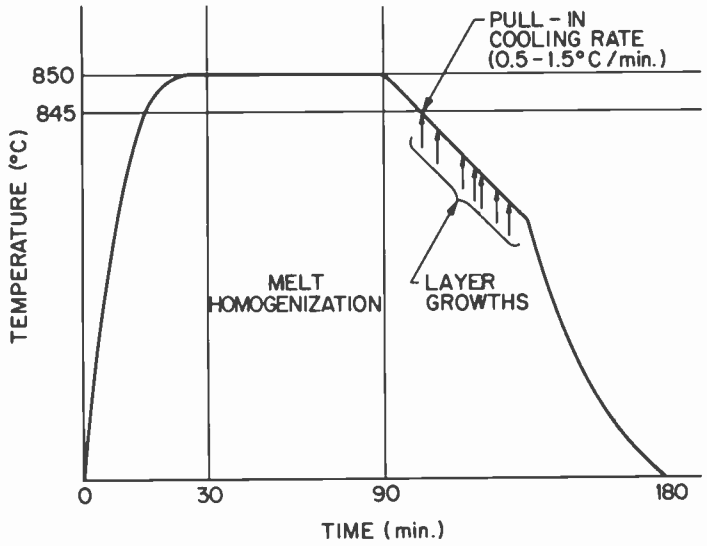

Fig. 5—Diagram of a typical LPE growth cycle for AlGaAs-laser fabrication.

the melts, which are spread uniformly (0.5 to 3 mm in thickness) over the substrate growth area by quartz block weights. The boat is made from high-purity graphite machined using standard machine shop techniques. The boat is vacuum fired (1×10^{-7} Torr at 1200°C) to remove any impurities which may have been absorbed in the graphite during machining.

Another important consideration in obtaining uniformly thick layers and well-defined interfaces between grown layers is the longitudinal temperature gradient along the boat.[3] If the growth sub-

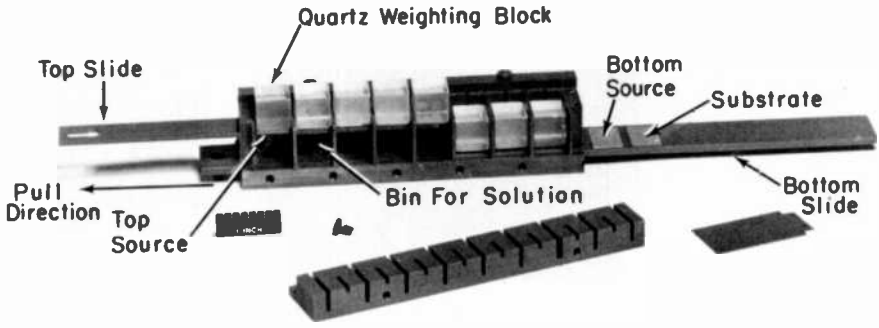

Fig. 6—Photograph of partially disassembled seven-melt graphite boat used for LPE growths of laser structures.

strate enters a melt bin at a temperature higher than the melt temperature, there may be partial dissolution of the substrate or the previously grown layer due to the localized undersaturation at the melt-substrate interface. Therefore, an increasing temperature gradient is required to create an oversaturated conditon such that deposition rather than dissolution occurs. However, too large temperature gradients whether increasing or decreasing can also cause problems in obtaining uniform thickness control. Generally, a temperature gradient of $\cong 0.1°C/cm$ positioned such that a "cold" substrate enters a "hot" melt is optimal. The "cold substrate into hot melt" method[3] has been the only LPE technique allowing the growth of uniform layers of thicknesses below 0.1 μm.

A Nomarski interference photograph of the top surface of a planar LPE-grown multilayer structure is shown in Fig. 7. The surface is relatively smooth. Terraces are present but their height is small (200–500 Å) and they do not impact device performance. Multilayer planar structures have constituted the basis for the simplest type of cw diode laser, the stripe-geometry double-heterojunction (DH) laser.

3. Planar-Geometry Diode Lasers

The simplest cw diode lasers are composed of a multilayered planar geometry with an oxide-defined stripe for current confinement (Fig. 8a). When the diode is forward biased, carriers are injected from p-

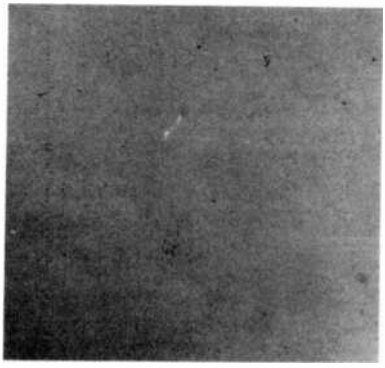

Fig. 7—Nowarski interference micrograph of top surface of planar DH-laser material.

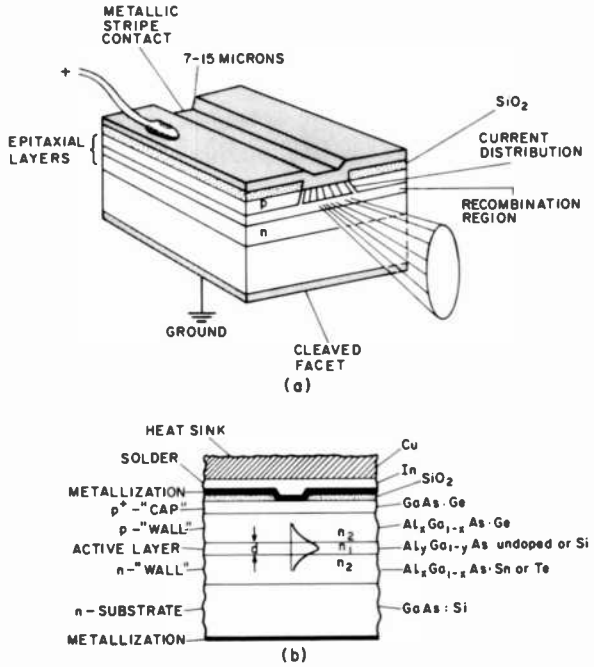

Fig. 8—Schematic representations of: (a) the stripe-geometry double-heterojunction laser structure; (b) the cross section of a heterojunction AlGaAs laser ($x-y > 0.25$; $n-n_2 > 0.2$) for cw room-temperature operation. The active layer of thickness d(0.05 to 0.2 μm) is placed 2 to 3 μm away from the contact stripe.

and n-type layers into a recombination region where they recombine to give light. Stimulated recombination and cleaved-end mirrors provide light amplification in a resonator. Lasing action occurs when enough carriers are injected to provide the optical gain needed to overcome the cavity's internal and external losses.

For cw operation at room temperature, low lasing-threshold currents are required, which implies a thin recombination region. In turn, the lasing transverse spot size—which is rather small (0.5 to 1 μm)—provides a divergent beam of 30° to 40° full-width half-power (FWHP) in the plane perpendicular to the junction. In the plane of the junction, light confinement is controlled by the current flow, and thus the lasing spot is comparable in size to the stripe-contact width. The laser emission is then elliptical (Fig. 8a) with typical transverse and lateral beamwidths, at half power, of 40° and 10°, respectively.

The emitting area on the cleaved facet is defined by the built-in

dielectric profile; the emitted light can therefore be thought of as an optical mode of a two-dimensional dielectric waveguide. For use in systems it is important that a single Gaussian-like beam be obtained at all drive levels of interest (that is, stable fundamental optical-mode operation). In reality, stripe-geometry devices, with a few exceptions, generally have an unstable optical mode.

The cross section of a stripe-geometry double-heterojunction (DH) laser is displayed in Fig. 8b. Four layers are deposited on a GaAs substrate: n-type $Al_xGa_{1-x}As$; an n, p, or undoped "active" layer, $Al_yGa_{1-y}As$; p-type $Al_xGa_{1-x}As$; and a p^+-GaAs layer for contact. The compositions are such that x is greater than y, which gives an active layer of lower energy bandgap ($\Delta E_g \geq 0.3$ eV) and higher refractive index ($\Delta n = n_1 - n_2 \geq 0.2$). Consequently, carriers injected from the n- and p-$Al_xGa_{1-x}As$ layers are confined to the active layer, where they recombine to produce light. The generated radiation is trapped in the one-dimensional dielectric guide formed by the active layer of thickness d and index n_1, and the confining layers of index n_2. This waveguide in the plane perpendicular to the junction (the transverse direction) supports only the fundamental mode as long as d is less than 0.4 μm and Δn is greater than 0.2.[11]

For practical diodes, d is typically 0.05 to 0.2 μm and Δn is greater than 0.2, and thus a stable fundamental transverse mode (that is, in the plane perpendicular to the junction) is always the case. By contrast, along the active layer (the lateral plane) the mode confinement is provided by the current flow alone, which, for standard stripe-contact (10- to 15-μm wide) devices, often results in a series of instabilities:[12,13] strong nonlinearities ("kinks") in the light-current (L-I) characteristics; pulsations; excess noise; and optical-mode beam shifts. Such behavior can seriously affect or even prevent the use of stripe-contact diode lasers for most systems-oriented applications. As a result, current state-of-the-art laser diodes represent tremendous efforts in recent years to achieve laser-mode stabilization by changing the basic planar-DH stripe-geometry structure (see Section 4).

The stained angle-lapped cross section of a planar geometry device is displayed in Fig. 9. The active layer is ≅500 Å thick and is quite uniform across the wafer(≅½ in.). With liquid-phase epitaxy, active layers as thin as 300 Å have been realized.[14] Thin active layers are important for achieving high-radiance edge-emitting LEDs, high-power diode lasers, and low-threshold-current-density diode lasers. For three-layer double heterojunction (DH) devices (Fig. 8), LPE growth has provided to date the lowest lasing threshold current densities[14,15] (see Table 1). The threshold current density

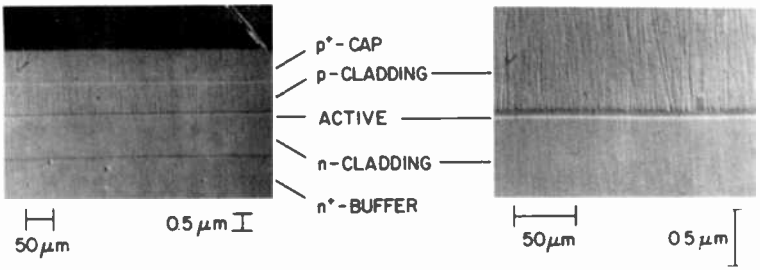

Fig. 9—Stained 1°-angle-lapped cross section of planar DH-laser material. The active layer is ≈500 Å thick.

characterizing a laser structure is obtained from planar devices without current confinement (so-called "broad-area" lasers). In Table 1 we show the minimum broad-area laser threshold current densities for AlGaAs/GaAs and InGaAsP/InP DH devices grown by liquid phase epitaxy (LPE), organo-metallic chemical vapor deposition (OM-CVD), vapor-phase epitaxy (VPE), and molecular-beam epitaxy (MBE). With the possible exception of MBE-grown InGaAsP/InP devices, the variation in minimum threshold for different growth techniques does not necessarily reflect the material quality. That is because the relationship of the optical gain vs. the injected current density[21] appears to be growth-dependent. In turn, for DH structures of similar geometry but grown by different techniques the value of the minimum threshold current density and its associated active-layer thickness will be different.[22] For example, in AlGaAs/GaAs DH lasers with an Al concentration differential of 30% between the active and the confinement layers LPE devices provide a minimum average threshold current density of 700 A/cm^2 at active-layer thicknesses around 800 Å,[16,23,24] while OM-CVD devices provide a minimum average threshold of 600 A/cm^2 at active-layer thicknesses around 1300 Å.[16] Differences in gain-current relationships between LPE and OM-CVD-grown lasers are also reflected in different threshold current vs. device length dependences.[25]

For diode lasers with active-layer thicknesses below 300 Å the injected carrier distribution is quantized in discrete levels, which

Table 1—Minimum "Broad-Area" Threshold Current Densities (A/cm^2) for DH Lasers Fabricated by Various Growth Methods

System	LPE	OM-CVD	VPE	MBE
AlGaAs/GaAs	475[14]	560[16]	—	800[19]
InGaAsP/InP	670[15]	≅1000[17]	≅1000[18]	1800[20]

in turn strongly affects laser operation.[26,27] Lasing in quantum-well structures has originally been demonstrated in devices grown by LPE, with active layers as thin as 150 Å.[27] The growth of such lasers by LPE was made possible by using a cylindrical multibin graphite boat of special design, in which the substrate is briefly exposed (~50 ms) to different melts by rotating it back and forth using a computer-controlled stepping motor. However, vapor-deposition techniques (OM-CVD, MBE), due to relatively slow growth rates and a high degree of layer uniformity across the wafer, have proven more suitable for the fabrication of optimum quantum-well lasers.[28]

4. Lateral-Mode Stabilization in Diode Lasers

As mentioned above, planar stripe-geometry devices generally have poor electro-optical characteristics due to the lack of tight mode confinement in the lateral direction (i.e., the plane of the junction).

The two general approaches to lateral-mode control have been tight current confinement by narrow contact stripes and the formation of real-index lateral waveconfining structures (waveguide or antiwaveguide, as shown in Fig. 10). Tight current confinement by narrow stripes[29,30] (3–7 μm) provides lasers of "kinkless" L/I characteristics to at least 10 mW cw, wide, non-Gaussian astigmatic beams, and multimode spectra. Only structures with built-in lateral

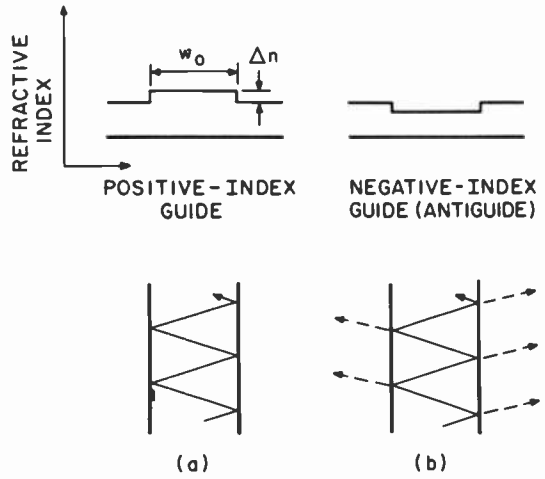

Fig. 10—Refractive-index variation in the lateral plane and ray-optic representation of light propagation. (a) Positive-index guide and (b) negative-index guide (antiguide).

wave confinement have resulted in single-mode lasers; i.e., devices which operate over wide ranges of drive current in a stable fundamental mode as well as in a single longitudinal mode. Figure 10 displays the basic wave-confining structures: the positive-index waveguide (i.e., a local increase in refractive index) and the negative-index waveguide (i.e., a local decrease in refractive index). In a positive-index guide, the guided mode is "proper" or "trapped" in the sense that it is totally internally reflected at the dielectric boundaries (bottom Fig. 10a). The amount of refractive index change Δn and the spatial extent of the index variation w_0 are chosen such that the structure supports only one mode: the fundamental one. The first-order mode cut-off condition is [11]

$$\sqrt{\Delta n}\, w_0 \leq \lambda/\sqrt{8n} \qquad [1]$$

where n is the averaged refractive index. Eq. [1] holds for passive waveguides. In active waveguides gain-loss considerations can allow stable fundamental-mode operation at w_0 values twice the one given by Eq.[1].[11,31,32]

The negative-index guide or antiguide differs from a positive-index guide in that the "guided" modes are "improper," i.e., upon reflections at the dielectric boundaries part of the light is refracted into the outer regions (bottom Fig. 10b), and thus the mode will vanish after propagating a finite distance in a passive guide. The refracted light can be thought of as radiation loss α_R:[33]

$$\alpha_R \cong \frac{(m+1)^2 \lambda^2}{2w_0^3 n^2 \sqrt{2|\Delta n|/n}} \qquad [2]$$

where m is the mode number. Although in a passive guide "leaky" modes cannot be supported for long distances, in active structures electronic gain can overcome the radiation losses and allow sustained propagation and oscillation of leaky modes. The strong dependence of the radiation loss on the mode number provides discrimination against high-order lateral-mode oscillation in some high-power single-mode devices. In order to fabricate positive or negative-index waveguides, three baseic techniques have been used: etch-and-regrowth (Fig. 11a); one-step LPE over nonplanar substrates (Figs. 11b and c); and preferential dopant diffusion (Fig. 11d). The etch-and-regrowth technique consists of embedding a mesa of planar DH material in high-resistivity material. The current is then mainly confined to the mesa. LPE over nonplanar substrates provides structures where lateral mode control is obtained due to lateral variations in active-layer thickness (Fig. 11b) or to lateral variations in the thickness of the cladding layers (Fig. 11c). In all cases a guide

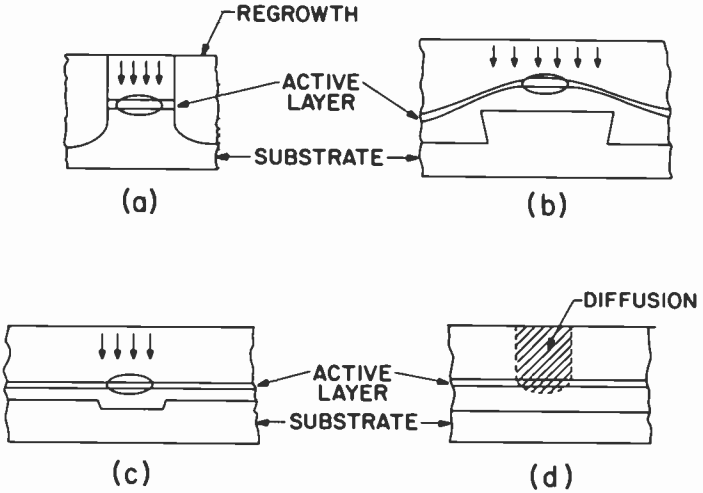

Fig. 11—Schematic representations of the basic methods used for lateral mode confinement: (a) etch-and-regrowth; (b) LPE over nonplanar substrates for which the active-layer thickness varies; (c) LPE over nonplanar substrates for which a cladding layer varies in thickness; (d) preferential dopant diffusion.

or antiguide is formed in the lateral direction. Below we describe LPE growth over nonplanar structures (Figs. 11a–c) with emphasis on LPE over nonplanar substrates.

5. LPE Growth Over Nonplanar Structures

a. Growth Over Nonplanar Substrates

In order to obtain structures of varying active and/or confinement-layer thickness (Figs. 11b and c) LPE has to be performed atop a patterned substrate. The discovery of the fact that LPE growth is strongly affected by topographical features etched into the substrate (channels, terraces, mesas) occurred independently in 1975 at three laboratories.[34–36] The first nonplanar-substrate laser was reported by Burnham and Scifres.[34] Studies of LPE growth characteristics over channels have been done by Botez et al.,[34,37] Kirkby et al.,[35] Funakoshi et al.,[38] and Andreev et al.[39] To illustrate these characteristics, we show schematically in Fig. 12 the growth stages above a channel (Fig. 12a), a terrace (Fig. 12b), and a mesa (Fig. 12c). Before going any further, it must be stressed that in all cases considered here the material used as a mask for substrate etching is removed prior to growth, and thus growth over substrate channels defined by oxide films[39,40] will not be treated.

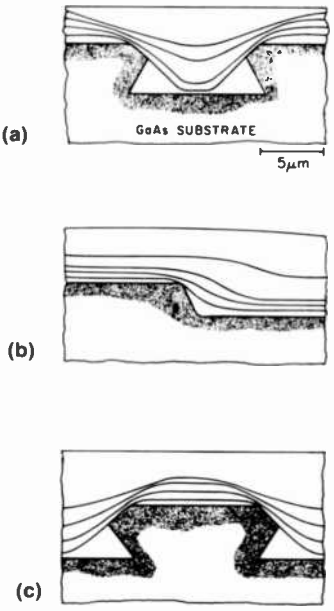

Fig. 12—Schematic representation liquid-phase-epitaxial growth stages over various topographical features etched into GaAs substrates: (a) a channel, (b) a terrace, and (c) a mesa.

The substrates are in all cases (100)-oriented. The various substrate-surface features are obtained by preferential chemical etching through windows in oxide masks. The main driving force for nucleation is the LPE growth dependence on local surface curvature. It can be shown from thermodynamical considerations[41] that for a given temperature, variations in surface curvature are associated with variations in chemical potential of the solid. In order to maintain equilibrium, variations in chemical potential of the solid have to be matched by variations in chemical potential of the liquid solution, which in turn are directly related to relative deviations in solute concentration C (i.e., $\Delta\mu = kT(\Delta C)/C$). Then one obtains, for equilibrium near a curved solid surface of radius R, the following relationship:[37,41]

$$\frac{\Delta C}{C} = \frac{2\gamma V_m}{kT}\frac{1}{R} \qquad [3]$$

where γ is the surface tension, V_m is the crystal molar volume, and R can be positive or negative depending on whether the surface is convex or concave, respectively. As shown in Fig. 13, the net effect is that at a fixed temperature T_e, for which equilibrium exists be-

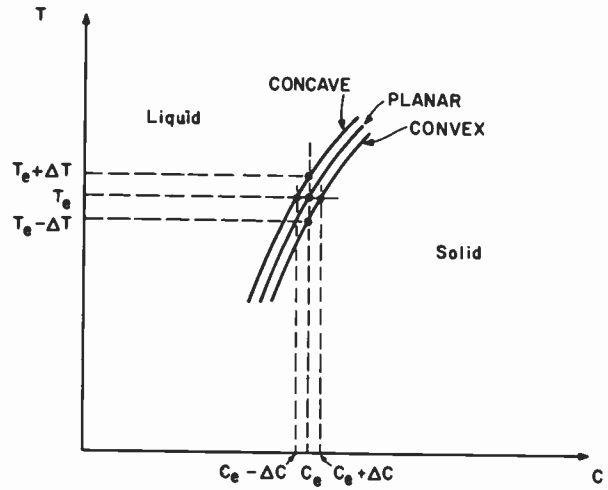

Fig. 13—Liquidus curves for planar, concave, and convex surfaces around the temperature T_e. At T_e a solid of planar surface is in equilibrium with a liquid of solute concentration C_e.

tween a solution of solute concentration C_e and a planar surface, the curved surfaces will be in equilibrium for different solute concentrations: $C_e \pm \Delta C$, depending on whether the surface is convex or concave. Conversely, at a given solute concentration C_e, equilibrium will be reached at the temperatures $T_e \pm \Delta T$ for concave and convex surfaces, respectively. Thus, a melt of concentration C_e at T_e is effectively undersaturated for the convex case, with subsequent melt-etch of the convex surface, and effectively supersaturated for the concave case, with subsequent rapid growth on the concave surface. As can be seen from Fig. 12, there is always a tendency to fill in concave parts of the surface (e.g., bottom corners of dovetail-shaped channels) and melt-etch convex parts of the surface (e.g., channel "shoulders"). The preference of LPE growth for concave over convex surfaces, while most evident in the incipient growth stages over channels, is still a major factor in the shaping of the various grown layers.[35–37] Another important factor is lateral mass transfer from melt-etched areas (e.g., channel shoulder) or planar areas (e.g., flat bottoms of channels) to concave areas. Then the driving forces are on one hand differences in surface tension along the liquid-solid interface[35,37] as the curvature varies, and, on the other hand, lateral diffusion induced by local solute concentration gradients between melt-etched areas and filled areas.[38] The overall tendencies are rapid growth in concave areas and slowed growth in

convex areas, such that the total free energy is minimized with the eventual result of obtaining a flat surface.

The various growth stages over a channel, a terrace, and a mesa are illustrated in Fig. 12. Just as discussed above, in all cases growth occurs preferentially in concave areas over convex areas with the tendency to eventually flatten the surface. Depending on the structure geometry that one seeks to obtain, one can control the growth features not only by such obvious parameters as etched-channel geometry, but also by growth conditions such as the amount of supercooling,[35,38] the growth temperature,[35,38] and the cooling rate. For instance, melt-etch of the channel shoulders can be prevented by using initial supercooling (2–10°C),[35,38] relatively low growth temperatures (700–800°C),[35,38] and fast growth rates (1–2°C/min).[35,38] Another growth characteristic, fast fill-in of channel to a flat surface [as needed in channeled-substrate-planar (CSP) structures], also requires low-growth temperatures,[35] but moderate supercooling and growth rates.[38] In all of the above cases, the substrate is considered to be oriented perfectly in the (100) direction. However, if the substrate is misoriented with respect to the (100) direction, growth over channels can be dramatically affected as discussed in Section 6.

The grown layers shown in Fig. 12 are contiguous across the wafer. However, for thin layers, such as the active layer of laser structures, growth can be discontinuous due to (a) melt-etch on convex parts of the n-confinement layer[34,42,43] (Fig. 14a) and (b) lack of growth on the (111)A planes in InP-based structures[44] (Fig. 14b). Such devices have resistive shunt currents on either side of the active region, which could prevent cw laser operation.

Typical fabrication steps in the fabrication of a nonplanar-substrate laser are displayed in Fig. 15. In this case the fabrication of constricted double-heterojunction (CDH) lasers[48] is illustrated. The

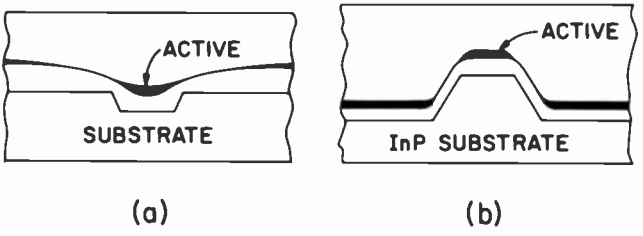

Fig. 14—Discontinuous-active-layer LPE growths: (a) over channels (AlGaAs/GaAs or InGaAsP/InP systems) and (b) over mesas (InGaAsP/InP system).

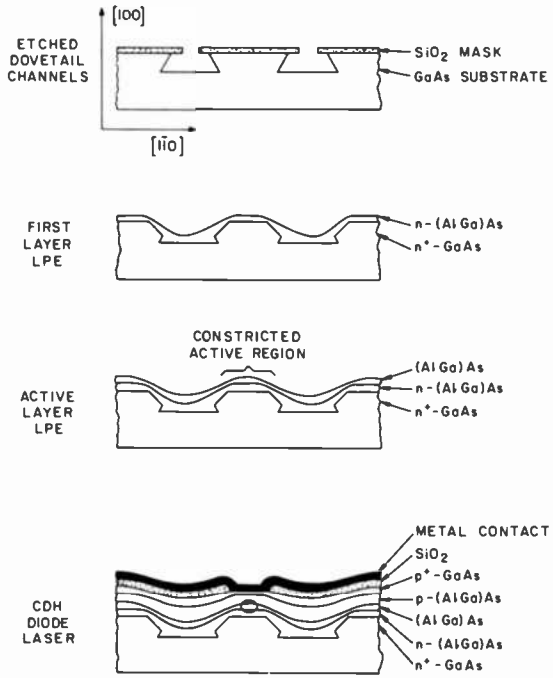

Fig. 15—Schematic representation of the fabrication steps of CDH devices. A ridge-guide device is considered.

first step is the etching of channels into a GaAs substrate. The channels are dovetail-shaped; that is, parallel to the [011] direction on a (100)-oriented GaAs substrate. V-shaped channels are not used because during LPE growth the mesa separating a pair of V-channels can be easily melt-etched, which in turn prevents the formation of a convex surface above the mesa, the very characteristic of the CDH geometry. By contrast, the mesa between two dovetail channels is melt-etched only at the sharp convex shoulders of those channels (see Fig. 15) and thus, grown layers of negative curvature can easily be attained above the mesa (bottom Fig. 15). The channels' etching is performed by using SiO_2 window masks and the solution 1:8:8 (H_2SO_4:H_2O_2:H_2O) at 20°C. Pairs of 5-μm-wide stripes are originally formed in SiO_2 with the help of standard photolithographic techniques. Then the etchant is used for ~1 min to form 4-μm-deep channels of 10-μm-wide top widths. The interchannel spacing is typically 32 μm. The SiO_2 film is subsequently removed with buffered HF and the whole surface is lightly etched with a NaOH:H_2O_2 aqueous solution [8 g NaOH in 200 ml water, and 20 ml H_2O_2 (30

percent) in 200 ml water] for 1 min. The channeled substrate is then cleaned and loaded into the LPE boat.

LPE is performed using the thin-solution technique,[3] which allows reproducibility and uniformity in the deposition of thin layers (<0.2 μm). Growth of at least four epitaxial layers occurs between 850°C and 820°C while the cooling rate is ~1°C/min. Thus, as opposed to CSP structures,[38] the growth temperatures for CDH devices are not limited to values below 780°C. During the first-layer growth (i.e., n-AlGaAs) the channel shoulders are partially and preferentially melt-etched (Fig. 15). In order to avoid heavy melt-etch, a controlled amount of cooling (3–5°) is provided before the introduction of the substrate under the first solution. The active layer is subsequently grown. Its lateral thickness variation is dictated both by local surface curvature as well as by the relative position of the channels' direction with respect to the substrate misorientation direction (see Sec. 6). After growth of a four-layer CDH structure, standard oxide-stripe technology is used for placing 10-μm-wide metallic stripe contacts above the mesa separating the channels.

Fig. 16 illustrates the top surface of a CDH wafer right after

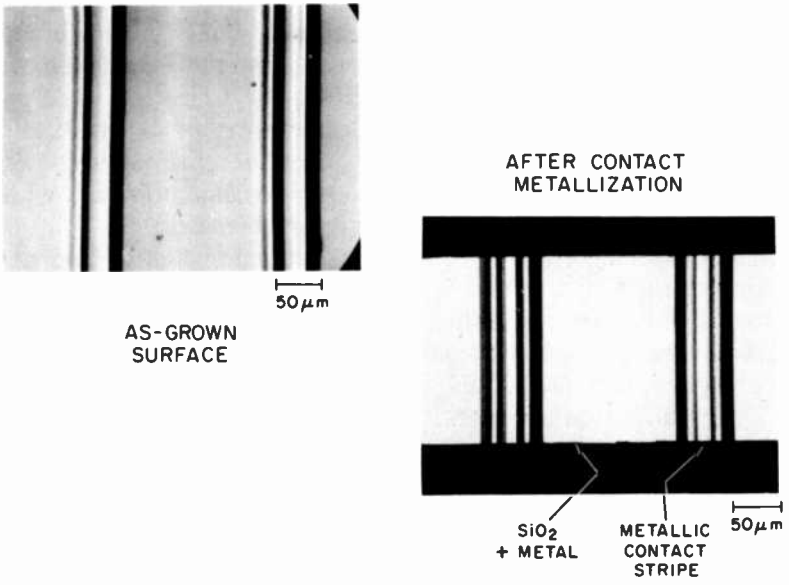

Fig. 16—Nomarski interference photographs of the top surface of an as-grown CDH wafer, and the top surface of a CDH-laser bar with SiO_2-defined contact stripes and metallization.

growth, and after metallization and contact-stripe definition with SiO_2. The as-grown surface is very smooth and shows no terracing features as opposed to the top surface of planar DH wafers (see Fig. 7). It must be stressed that lack of terracing is characteristic of nonplanar-substrate LPE growths in general. The only features that can be observed are fine meniscus lines running perpendicular to the channels' direction. The left side of Fig. 16 shows how 10-μm-wide SiO_2-defined contact stripes are placed atop the residual mesas of CDH wafers. The presence of residual channels and mesas at the top surface of the grown CDH wafer makes stripe-contact alignment with the intended lasing cavity a trivial job.

b. Growth Over Nonplanar DH Structures

In order to realize buried-heterostructure (BH) lasers (Fig. 11a) a mesa of planar DH material is first obtained by chemical etching. A second LPE growth is then performed which embeds the mesa in high-resistivity material. An optical waveguide is thus built in the lateral direction.

Two types of BH lasers can be realized using this technique: (a) standard BH devices (Fig. 17a), for which an oxide atop the mesa acts as mask against growth,[45] and (b) planar-top BH devices (Fig. 17b), for which the convexity of the mesa prevents growth of thin layers atop it.[46] In standard BH devices the regrowth is uneven (i.e., higher growth rate near the mesa than away from it).[45] That provides a nonplanar top surface, which is undesirable for cw bonding and mounting. By contrast, in planar buried-heterostructure (PBH) devices [46] the mesa is totally embedded in regrown material, which provides the flat top surface suitable for cw bonding.

A combination of growth over nonplanar substrates and nonplanar structures is the double channel (DC)-PBH laser (Fig. 17c).[47] In that case the mesa is delineated by channels etched into a planar DH structure. The regrowth is similar to the one for PBH devices. The presence of channels aids in nucleation and produces more uniform growth around the mesa.[47] For these reasons the regrowth in DC-PBH devices is quite similar to the growth of CDH lasers[48] over nonplanar substrates (see Fig. 15).

6. Effects of Substrate Misorientation on LPE Growth Over Nonplanar Substrates

For a substrate the degree of misorientation α is defined with respect to a specific crystallographic direction [hkl] (see Fig. 18). That

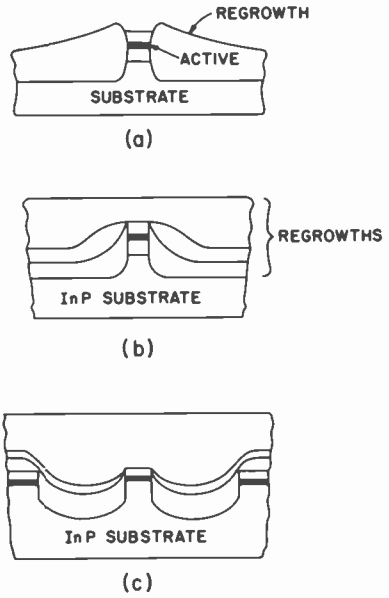

Fig. 17—Types of lasers obtained by LPE growth over nonplanar DH structures: (a) the buried-heterostructure (BH) laser (AlGaAs or InGaAsP); (b) the planar-BH (PBH) laser[46] (InGaAsP/InP); (c) the double-channel PBH (DC-PBH) laser[47] (InGaAsP/InP).

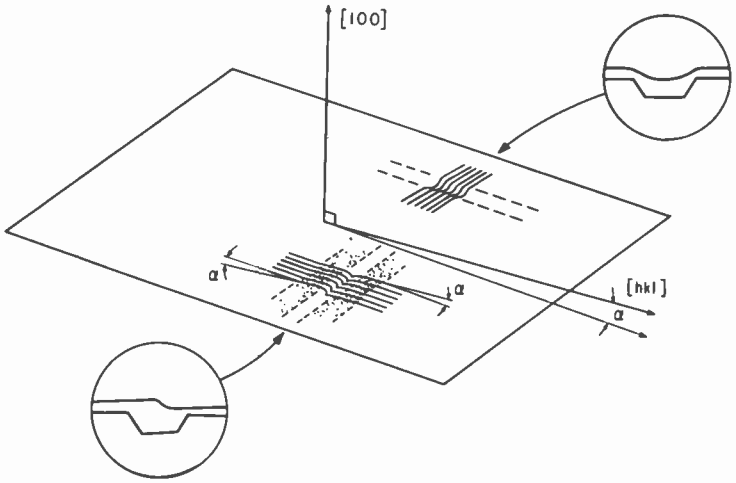

Fig. 18—Diagram showing the effects of substrate misorientation on liquid-phase epitaxy over channels. The substrate is misoriented α degrees off the (100) plane and toward the [hkl] direction.

is, the [hkl] direction is the tilting direction defined as the line in the (100) plane that is normal to the intersection between the substrate plane and the (100) plane. As far as LPE growth over channels is concerned, the other parameter of interest is β, the angle between the [hkl] direction and the channels' axis (see Fig. 19). For simplicity we call α, the tilt angle and β, the misorientation angle.

As shown in Fig. 18, when the substrate misorientation direction is parallel to the channel direction, the LPE growth is symmetrical. Otherwise, the presence of the channel(s) triggers the formation of terraces (Fig. 18) in what appears to be a tendency to reconstruct the low-surface-energy (100) plane.[36,37] For thick layers, such terraces are reflected in some degree of asymmetry in layer cross section.[37] For thin layers, however, the effects of misorientation can be quite dramatic. Thus, as shown in Fig. 20, when the substrate misorientation is 1–2° off (100) toward [010], (i.e., β = 45°) the active-layer thickness decreases to one side while increasing to the other side. This semileaky-guide shape is a direct result of the crystal tendency to reconstruct the (100) plane. When the misorientation direction is parallel to the channels' directin (bottom of Fig. 20) the active layer takes a symmetrical shape of the ridge-guide type, due to reduced growth over the shoulders of the residual n-AlGaAs mesa (see Fig. 12c). The two active-layer shapes, semileaky-guide and ridge-guide, are largely responsible for lateral mode control in most

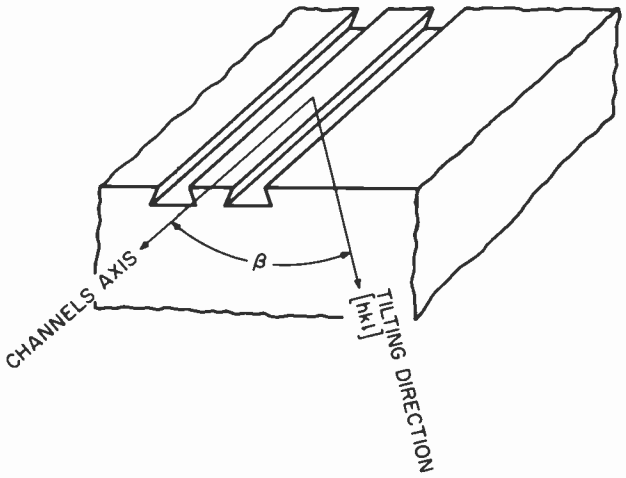

Fig. 19—Diagram showing the definition of β, the angle between the substrate-mis-orientation direction (the tilting direction) and the channels' axis.

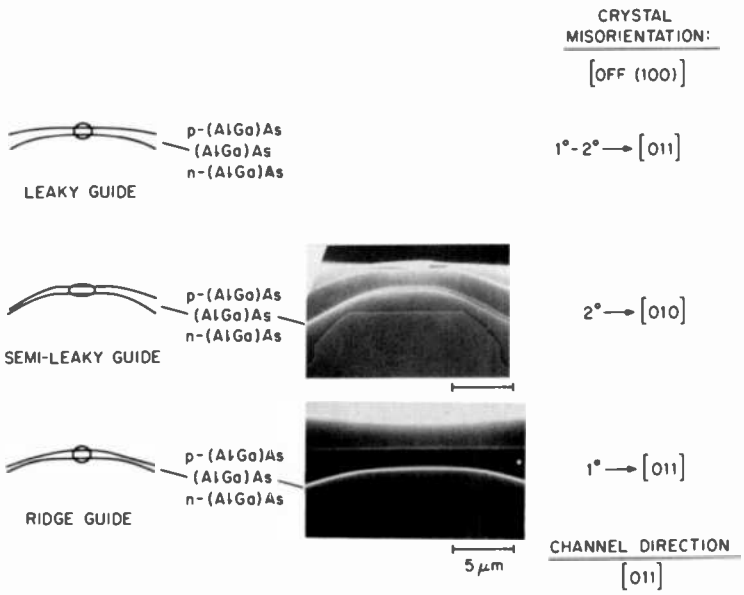

Fig. 20—Types of CDH structures according to their active-layer thickness variation. Leaky-guide devices could only be obtained above a channel shoulder.[49] The active layers above the mesa are shown in scanning-electron-microscope photographs for both semi-leaky- and ridge-guide devices.

CDH lasers. We have never encountered above the mesa a leaky-guide shape for the active layer. Leaky-guide active layers have only been obtained over channel shoulders.[49]

An extreme case is $\beta = 90°$; i.e., when the substrate misorientation direction is perpendicular to the channel axis. Then large terracing is formed when growing over a pair of channels.[50] We show in Fig. 21 a comparison between structures grown over pairs of channels in substrates of diametrically opposed misorientation angles. On one hand, the constricted double-heterojunction large-optical-cavity (CDH-LOC) structure[51] is grown on a substrate of misorientation direction parallel to the channels' axis (i.e., $\beta = 0$), and, on the other hand, the terraced-heterostructure (TH-LOC) structure[50] is grown on a substrate of misorientation direction perpendicular to the channels' axis (i.e., $\beta = 90°$). The structures were grown with the same etched-channel geometry, the same layer compositions, the same growth times, and, furthermore, the same amount of substrate misorientation (i.e., $\alpha = 1°$). Yet, just a 90° change in misorientation direction has a dramatic effect on the geometry of the

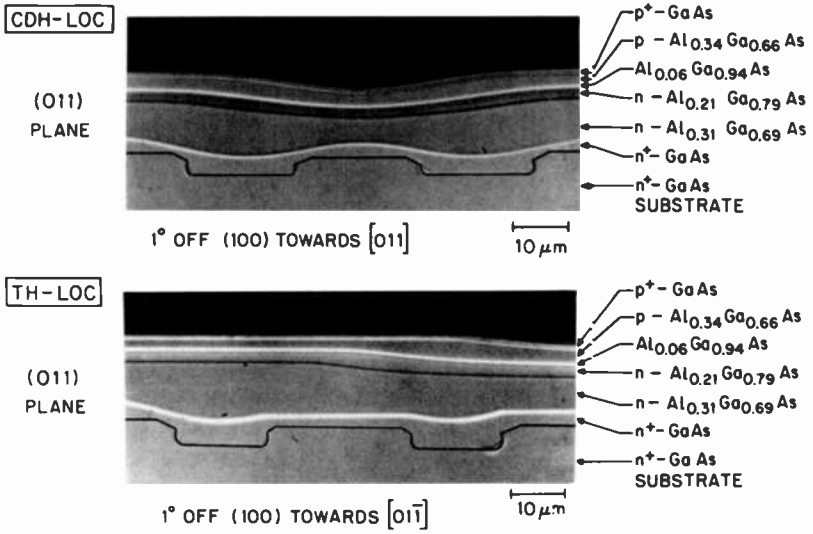

Fig. 21—Photomicrographs of lightly etched cross sections of CDH-LOC and TH-LOC laser structures. The structures were grown for the same etched-channels geometry, the same layers' compositions and growth times, and the same amount of substrate tilt angle (α = 1°). The only difference is in the substrate misorientation direction: β = 0° for CDH-LOC; β = 90° for TH-LOC.

grown structures. For obvious reasons the lasing cavity position and geometry are different for the two structures (see Fig. 22). For the CDH-LOC laser the lasing cavity is symmetrically placed above the mesa separating the channels and is composed of a convex-lens-shaped active layer atop a concave-lens-shaped guide layer. For the TH-LOC laser the lasing cavity is on the terrace slope, away from the mesa, and is composed of asymmetric convex-lens-shaped active and guide layers. It is generally found that while growing over nonplanar substrates one has to keep both the substrate tilt angle, α, and the substrate misorientation angle, β, under tight control.

7. Typical Mode-Stabilized Laser Structures and Results

In this section we present some of the more sophisticated mode-stabilized laser structures realized by liquid-phase epitaxy. The lasers are treated in two groups: low-power (1–7 mW/facet) single-mode devices and high-power (10–50 mW/facet) single-mode devices. Only a few representative structures and results are presented. An extensive review of both low- and high-power single-mode lasers can be found elsewhere.[52]

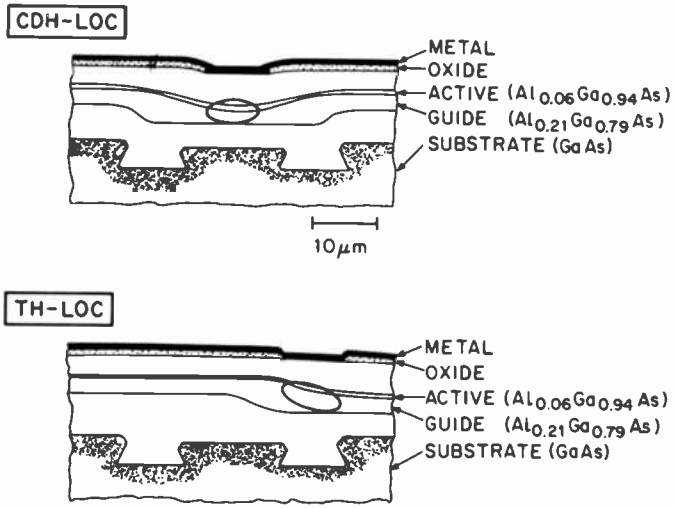

Fig. 22—Schematic representations of the CDH/LOC and TH-LOC laser structures and their respective lasing areas.

a. Low Power Single-Mode Lasers

The term "low power" refers to single-mode devices that can operate *reliably* at power levels, in the 1- to- 7-mW/facet range. For AlGaAs devices the upper limit for reliable operation is directly related to the lasing spot size; i.e., the maximum (linear) power density for reliable operation is ≅1.5 mW/(μm of lasing width) for coated double-heterojunction (DH) devices.[53,54] InGaAsP devices seem to have little or no facet-induced degradation, at least at power levels below 10 mW. In general, however, InGaAsP lasers have serious heating problems,[12] possibly accounting for the fact that to date acceptable reliability has been demonstrated only for power levels in the 3- to 5-mW/facet range. Thus, InGaAsP devices can be thought of as low-power lasers.

As mentioned in Section 4, a major category of mode-stabilized devices are buried-mesa structures (see Fig. 11a). Two such devices are schematically depicted in Fig. 23: the buried-heterostructure large-optical-cavity (BH-LOC) AlGaAs laser [55] and the BH InGaAsP laser. The AlGaAs device incorporates the LOC concept;[56] that is, the growth of a layer between the active layer and the n-confinement layer having an index of refraction between the indices of those layers. The additional layer, commonly called the guide layer,

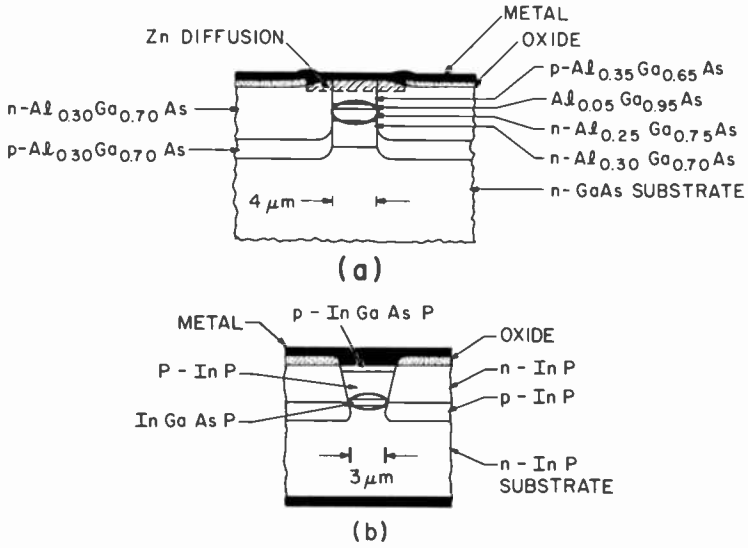

Fig. 23—Schematic representation of buried mesa structures: (a) AlGaAs BH-LOC laser and (b) InGaAsP BH laser.

allows the propagation of a large transverse optical mode: 3–4 times larger than for a standard DH device (Fig. 8b).

For both devices, lasing in only the fundamental mode to high drive current levels above threshold is obtained for mesa widths in the 2- to 3-μm range.[32,55] For InGaAsP devices the maximum mesa width for single spatial mode operation is the same over the 1.2- to 1.6-μm emission wavelength range, since the first-order mode cutoff condition (Eq. [1]) is virtually wavelength independent.[32]

Current confinement is easily achievable in AlGaAs structures by growing high-resistivity AlGaAs burying layers. For InGaAsP/InP BH lasers that option is not yet available (i.e., high-resistivity InP), and thus current blockage relies mostly on grown back-biased p-n InP junctions. The position of the back-biased junctions has to be very close to the active layer in order to prevent shunt currents around the junctions. When tight current confinement is achieved, both AlGaAs and InGaAsP BH lasers have the lowest thresholds (~10 mA) of any types of mode-stabilized devices. A good measure of lateral current confinement is the threshold current normalized per micron of mesa width. Minimum values of around 4 mA/μm have been achieved for both AlGaAs[55] and InGaAsP[46] devices.

In Fig. 24 we display typical good characteristics of InGaAsP BH lasers. While minimum threshold current values of 8.5 mA and

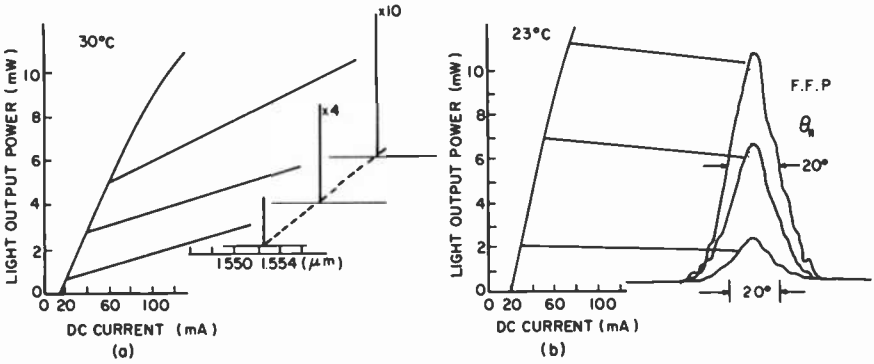

Fig. 24—Typically good characteristics of InGaAsP BH lasers: (a) Light/current characteristic and spectra of 1.55-μm deivce; (b) Light/current characteristic and lateral far-field patterns of 1.3-μm device. All illustrations are after Mito et al.[46]

13 mA have been achieved[46] at $\lambda = 1.3$ μm and 1.55 μm, respectively, the mean value of the thresholds is in the 20- to 25-mA range. This spread in threshold currents is due to geometry variations across the wafer, induced during device fabrication, and to different amounts of shunt current from device to device. Single-longitudinal-mode operation is achieved up to 5 mW (Fig. 24a), while single spatial-mode operation is obtained to power levels above 10 mW/facet (Fig. 24b). The lateral far-field patterns often show "ripples" due to scattering of light off the mesa walls. Such scattering, on one hand, provides dramatic increases in threshold for InGaAsP/InP mesa widths below 1.5 μm[57] and, on the other hand, discriminates against high-order-mode operation[58] so that mesas approximately twice as wide as predicted by theory (Eq. [1]) can be used for single fundamental-mode operation.[32]

The other major class of low-power devices is nonplanar-substrate devices. Figure 25 shows two typical nonplanar-substrate lasers: (a) the AlGaAs CDH laser[48] and (b) the InGaAsP close-confinement-mesa (CCM) laser.[59] In both cases the lasing cavity is formed above a substrate mesa. However, since there is no LPE growth on the (111)A planes of InP, the active layer is discontinuous for the InGaAsP device. Then, in order to prevent shunt currents, back-biased junctions are grown on either side of the mesa (Fig. 25b). The growth of discontinuous p- and n-type InP layers for current confinement is very similar to the growth used in PBH devices (see Fig. 17b).

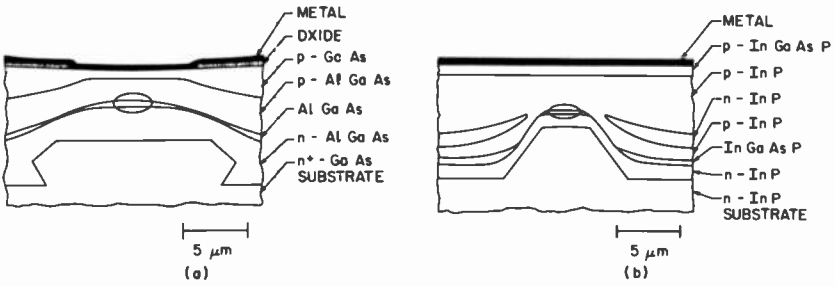

Fig. 25—Schematic representation of nonplanar-substrate devices: (a) Constricted double-heterojunction (CDH) AlGaAs laser;[48] and (b) Current-confinement-mesa (CCM) InGaAsP laser.[59]

In Fig. 26 we show light-current characteristics at various heat-sink temperatures for both CDH and CCM lasers. The maximum cw operating temperatures (i.e., 170°C for the CDH device and 125°C for CCM device) represent the highest operating ambient temperatures for AlGaAs and InGaAsP cw lasers, respectively. CDH lasers exhibit an unusually mild threshold-current temperature dependence over the 20–100°C temperature interval. That is, when the threshold current as a function of temperature is written in the empirical form:[11]

$$I_{th}(T) = I_{th}(0°C)\exp\left(\frac{T}{T_o}\right) \qquad [4]$$

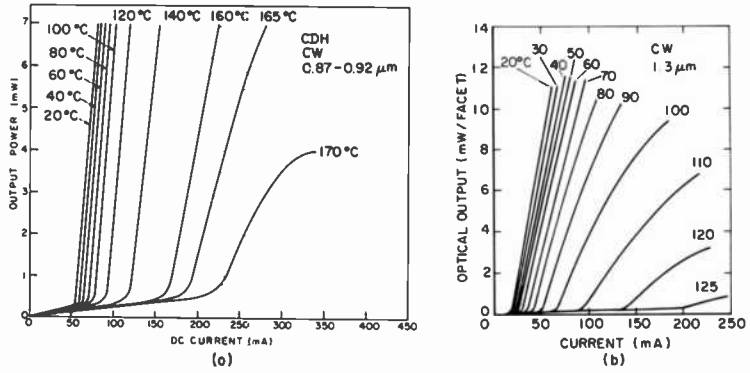

Fig. 26—Nonplanar-substrate devices: (a) Light/current characteristics at various heat-sink temperatures for AlGaAs CDH laser[48] and (b) light/current characteristics at various heat-sink temperatures for the InGaAsP CCM laser (after Nomura et al.[59]).

where T is the ambient temperature in °C; T_0 values in the 300–400°C range are obtained.[60] By contrast, standard DH AlGaAs devices have T_0 values in the 150–180°C interval [11,60] and thus, the threshold current varies with temperature two to three times faster than for CDH devices. The high T_0 values in CDH lasers are due to a temperature-dependent current focusing effect and represent a direct consequence of the fact that in the CDH structure a sizable portion of the current is not used in lasing.[48] The same concept has been recently applied to InGaAsP devices, by growing CDH-like 1.3-μm lasers.[43] Then T_0 values as high as 97°C were obtained, in contrast to the 50–70°C values characteristic of InGaAsP devices.[12] The CCM device has little or no leakage currents and thus exhibits normal T_0 values for InGaAsP lasers: 50–60°C.

Growths over single channels (Figs. 14a) also provide low-power mode-stabilized devices. By tight current confinement (back-biased junctions or narrow stripes) threshold currents around 10 mA can be achieved.[61,62] Fundamental-mode cw operation to 25 mW cw has been realized from InGaAsP devices[63,64] for which only the n-cladding layer varies laterally in thickness (see Fig. 11c).

b. High-Power Devices

The most powerful single-mode devices reported to date[50,51,65] are grown by LPE. As pointed out in the previous section, for low-power devices the single-mode power that can be obtained reliably is limited by the mode spot size. At the same time the mode lateral width is limited by the condition for fundamental mode operation in a positive-index guide (Eq. [1]). Thus, reliable single-mode operation could not be achieved at powers above 5 mW/facet. Two basic approaches have been taken to overcome these limitations:

(1) Increase the lasing spot size both perpendicular and parallel to the junction, *plus* introduce a mode-dependent loss mechanism (lateral antiguiding,[51] lateral absorption,[65] or scattering[55,58]) to discriminate against high-order-mode oscillation.

(2) Eliminate facet degradation by making nonabsorbing-mirror (NAM) laser structures.[66,67]

The most successful devices to date, the constricted-double-heterojunction large-optical-cavity (CDH-LOC)[51] (Fig. 27a) and the channel-substrate-planar (CSP)[65] (Fig. 27b), use the first approach. Large transverse spot size (1–2 μm at $1/e^2$ points in intensity) is assured by the LOC structure in the CDH-LOC laser and by very thin active layers (400–600 Å) in the CSP laser. High-order lateral

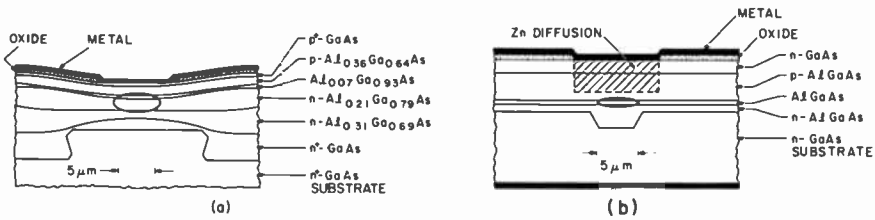

Fig. 27—Schematic representation of high-power single-mode laser types: (a) constricted double-heterojunction large-optical-activity (CDH-LOC)[51] and (b) channeled-substrate-planar (CSO).[65]

mode oscillation is suppressed by lateral antiguiding losses in the CDH-LOC (i.e., the negative-index contribution of the guide layer) and by lateral absorption losses in the CSP (i.e., GaAs-substrate proximity to either side of the channel). Both devices have threshold currents in the 60- to 80-mA range. However, the CDH-LOC device has a spot size roughly twice that of the CSP device. Consequently, CDH-LOC lasers have narrower beams and provide higher single-mode powers (40 mW vs 20 mW) than CSP lasers. Another LOC-type structure is the TH-LOC laser (see Figs. 21b and 22b). Its electro-optical characteristics (Figs. 28 and 29) are similar to those for CDH-LOC lasers. Single-mode cw operation is obtained to 50 mW in narrow beams and a single spectral mode. The 50-mW figure is relevant since it represents the highest cw power into a single mode ever reported for semiconductor lasers.

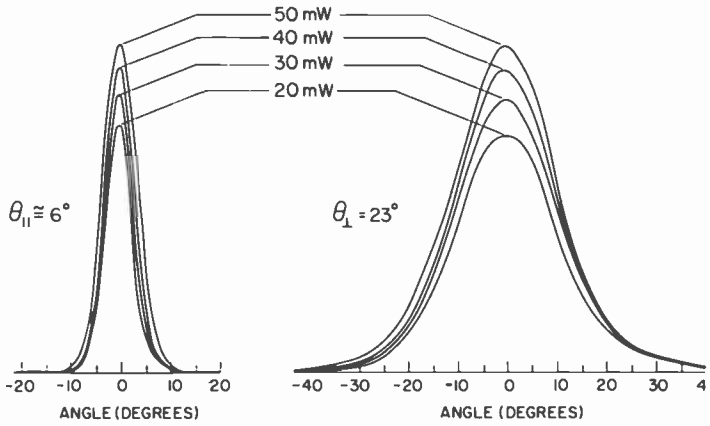

Fig. 28—Lateral and transverse cw far-field patterns for the TH-LOC laser.[50]

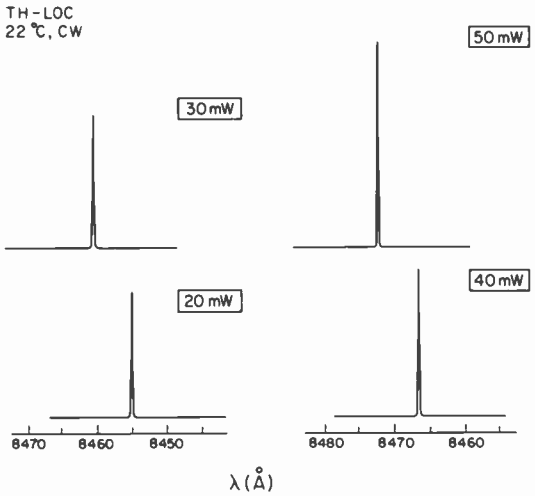

Fig. 29—CW spectra to 50-mW/facet output power for the TH-LOC laser.[50]

The other major approach to high-power reliable operation is the elimination of facet degradation by creating nonabsorbing-mirror (NAM) structures. In conventional AlGaAs diode lasers intense nonradiative recombination at the facet depletes the minority carriers and in turn the effective bandgap narrows.[66] Lasing light is thus heavily absorbed at the facet, a process that eventually results in catastophic mirror damage. To prevent such effects, one has to create at the mirror facets regions of higher bandgap than in the lasing region. NAM structures can be obtained by "burying" the facets in high-bandgap material[68] or by preferential Zn diffusion.[66,67] We show in Fig. 30 a NAM-BH-LOC structure fully realized by LPE. A BH-LOC-type device (Fig. 23a) is first fabricated. Then trenches are etched in a direction perpendicular to the buried mesa. LPE regrowth in the trenches provides a passive waveguide for light generated in the active laser region. Upon cleaving the device in the passive region, a NAM device is obtained since the mirror regions are optically passive. The NAM-BH-LOC laser has demonstrated three times[68] the output pulse power of the BH-LOC laser.

8. Device Reliability and Conclusion

Liquid-phase epitaxy is currently the crystal growth method used for the majority of optoelectronic devices. While the dominance of LPE in optoelectronics is, in part, historical (i.e., OM-CVD and other vapor deposition methods have been developed relatively recently),

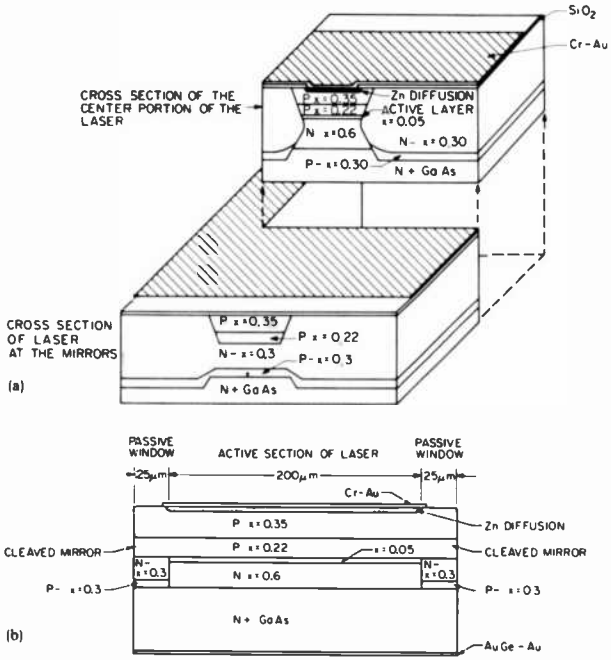

Fig. 30—Schematic representation of the nonabsorbing-mirror (NAM) BH-LOC laser.[68] (a) Diagram of the structure and (b) sideview of the structure (after Blauvelt et al.[68]).

certainly its intrinsic reliability has also been responsible for its preemptive position. On one hand, from a thermodynamic point of view LPE is the growth method closest to equilibrium and thus most likely to form stoichiometric solids, and, on the other hand, the metallic solvent in contact with the substrate is bound to act as a getterer of impurities.

The best diode-laser reliability data belong to LPE-grown devices.[53,69–71] By eliminating or avoiding diode failure mechanisms such as rapid bulk degradation, metallization failure, and facet degradation, drive-current degradation rates around 10^{-5} hr^{-1} have been achieved for AlGaAs devices aged at 100°C heatsink temperature.[69] Such results imply room-temperature extrapolated *median* lives approaching 10^6 years. For extrapolations, activation energies around 0.6 eV are used for AlGaAs devices. However, the vast majority of results are for low-power (3–5 mW/facet) lasers. Lifetests on high-power devices are relatively scarce. Cw operation for thousands of hours at 15 to 20mW/facet have been reported[52,67] for some of the devices discussed in the high-power laser section. Over 10,000

hours of operation at 40-mW peak power and 50% duty cycle have been achieved with CDH-LOC lasers.[72] More work is needed in high-power devices since one must first overcome problems associated with bonding and metallization before tackling problems related to the grown-material quality.

In conclusion, liquid-phase epitaxial growth is the major method for the fabrication of state-of-the-art cw diode lasers. LPE has produced the most powerful[50,51,65] and most reliable[69,71] diode lasers to date. By tight control of growth parameters such as substrate misorientation, highly uniform and reproducible laser structures can be achieved.[48,69,70] For the near future one can envision that crystal growth methods such as OM-CVD may replace LPE in the fabrication of very large quantities of low-performance diode lasers, while LPE remains the major avenue for obtaining high-performance lasers.

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Ohmic Contacts for Laser Diodes*

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Abstract—Requirements for ohmic contacts to laser diodes are discussed, and properties of Schottky barrier tunneling contacts are reviewed. A procedure is described for measuring contact resistance on fabricated laser material without the need for specially constructed samples and contact configurations. Measurements of contact resistance and estimates of specific contact resistance are given for Ti/Pt/Au contacts to surfaces with three different doping levels. It was found that below a p-type carrier concentration of 1×10^{19} cm^{-3} the contact resistance is likely to be too high for good device performance. At higher doping levels, a specific contact resistance as low as $\sim 2 \times 10^{-6}$ ohm cm^2 was obtained. Oxide stripe lasers provided with the type of contact discussed in this paper have been operated without failures for periods up to 7 years at a current density at the contact of 6–8 kA/cm^2. It appears therefore that these contacts satisfy the need for low resistance and durability and that, at the same time, they do not cause any obvious material degradation.

Introduction

Semiconductor lasers are especially sensitive to ohmic-contact properties, as laser failures can often be attributed to problems with the contact or to disturbances introduced into the structure during contact fabrication. One of the most successful contacts to GaAs lasers is the Schottky barrier tunneling structure, which is obtained when a metal film is applied to a highly doped semiconductor. Not only can such contacts have extremely low resistance values, but they also introduce very little damage into the crystal lattice compared to other processes requiring alloying or sintering for the achievement of low contact resistance.

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The most important contact is generally the one applied to the p-side of the device, since it is the one nearest the active region of the laser and thus must allow transfer of most of the heat generated in the device.

A typical oxide-stripe planar double-heterostructure laser structure is shown in Fig. 1. It can be seen that it has a narrow contact region on the p-side of the device, introduced for the purpose of restricting the flow of current. Such contact regions are used in many other structures, including such nonplanar types as the CDH or BH lasers.

In the following sections, a brief review will be given of the Schottky contact as it applies to GaAs, after which a method will be described for measuring the contact resistance on completed laser material. Results of a series of measurements in which p-type contacts were applied to different underlying material will be given. It will be shown that they are in agreement with expectations, and that there is a minimum carrier concentration in the semiconductor that is necessary to achieve low values of contact resistance.

Theory

Carrier transport across a metal-semiconductor boundary proceeds by thermionic emission for low semiconductor doping densities and by tunneling for high doping densities. A number of papers have been published analyzing contact properties where one or both of these mechanisms are expected to operate. For the case of ohmic contacts, however, the transport must be mostly by tunneling in

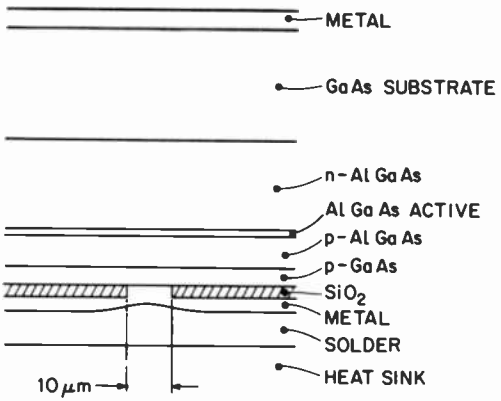

Fig. 1—Planar DH laser construction showing the current-constricting stripe contact.

order to obtain reasonably low values of contact resistance. In this case, the following approximate expression for the specific contact resistance has been obtained:[1,2]

$$R_c \sim \frac{C_1}{\sqrt{N}} e^{C_2 \sqrt{N}}, \qquad [1]$$

where C_1 includes Richardson's constant and the effective mass and the semiconductor permittivity, and C_2 includes the barrier height and the effective mass and permittivity. As the carrier concentration N increases, R_c becomes very small. Calculated values for p-type GaAs with 10^{19} cm^{-3} carrier concentration range from 2×10^{-4} (Ref. [1]) to 2×10^{-6} (Ref. [2]).

Measurement of Contact Resistance

A number of different methods have been described for the determination of contact resistance. Among them are the transmission line model,[3] the extended transmission line model,[4] and the "transfer length" method.[5] They generally rely on using an array of similar contacts from which, by making various measurements, the specific contact resistance can be extracted. Since, as mentioned earlier, an array of contacts already exists as part of the normal laser device processing, it was decided to also use this to evaluate the contact properties.

In contrast with the situation when measuring contact resistance on a homogeneous layer, the p layer in typical laser material involves two or more separate regions of different conductivity. In addition, (1) the thicknesses of these layers are not uniform due to various perturbations commonly occuring in liquid-phase epitaxy; (2) the composition of the layers, particularly the Al content of AlGaAs layers may vary across the wafer; and finally (3) the pn junction, which forms one boundary of the structure, may change in impedance at different regions of the wafer. All or some of these parameters combine to yield a considerable variation in material properties which makes it difficult to obtain reliable values for the "end correction" or the "transfer length" used in the usual techniques for contact resistance measurements. It can be said, in general, that those methods appear most promising that do not rely on comparing one region of material with another in order to obtain the contact resistance.

As is well known, the property of the contact observed in devices is the contact resistance, which is dependent on the contact geom-

etry and the direction of current flow. The contact property, dissociated from geometrical factors, is the specific contact resistance, which is taken as an intrinsic property of the metal-to-semiconductor interface. In the present case, because of the difficulties mentioned above, only the contact resistance is being measured, and the specific contact resistance is estimated by multiplying the contact resistance by the contact area. It will be shown later that the specific contact resistance obtained by this means nevertheless assumes reasonable values that are essentially in agreement with those obtained by other means.

The method used in this work is based on that described by Terry and Wilson.[6] Fig. 2 shows a typical bar of laser material provided with a series of stripe contacts (the stripes are embedded in a layer of dielectric, not shown in the figure). Passing a current between contacts 1 and 4, one measures the potential across 2 and 3, which is taken to represent the voltage drop across a length b of material of width t and thickness a due to a sheet resistance ρ/a. Switching the current contacts to 2 and 4 in Fig. 2 and repeating the measurement, one obtains an increase in the measured voltage because of the inclusion of contact resistance. The resistance R at a contact is taken to be

$$R = \frac{1}{2}\left[\frac{V_{2,3}}{I_{2,3}} - \frac{V_{2,3}}{I_{1,4}}\right]. \qquad [2]$$

The scheme described averages the resistance of two contacts. It is easy to see that a single contact can be measured by fixing one current lead on contact 3, and switching the other current lead between 1 and 2. Thus, by traversing three contacts across a laser

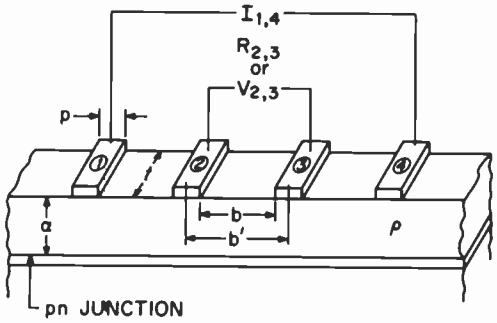

Fig. 2—Geometry of a laser "bar" used to determine contact resistance.

bar, one can measure a single contact at a time and obtain a detailed picture of the variations in contact resistance between a number of contacts.

To explore the meaning of the measurement obtained by this method, it is convenient to idealize the situation by assuming a contact with no resistance and determining what the above described process actually measures. The straightforward calculation of the resistance between two rectangular contacts placed on a homogeneous wafer of conducting material has been done by Hall[7] using the method of conformal transformations. The result is

$$R_{2,3} = \frac{2\rho}{at}\left(\frac{b}{2} + p - \frac{2a}{\pi} \ln \sinh \frac{p\pi}{2a}\right), \quad [3]$$

where ρ is the average resistivity of the layer, taken here to be bounded on one side by a pn junction, and the other constants are defined in Fig. 2.

If the contact width is large enough, $p/a >> 1$ and one obtains

$$R_{2,3} \approx \frac{\rho}{t}\left(\frac{b}{a} + \frac{4 \ln 2}{\pi}\right), \quad [4]$$

where $\rho b/ta$ is the resistance of a layer of resistivity ρ, cross sectional area ta, and length b. The term $(4\rho/\pi t)\ln 2$ is attributed to current crowding under the contacts.

The case of a potential measurement $V_{2,3}$ has also been worked out by Hall, who shows that the finite width of the contact leads to the potential

$$V_{2,3} = I_{1,4}\frac{\rho}{t}\left(\frac{b}{a} + \frac{p}{a} - \frac{4}{\pi} \ln \cosh \frac{p\pi}{4a}\right), \quad [5]$$

where the current is applied across contacts 1 and 4. For $p/a >> 1$,

$$\frac{V_{2,3}}{I_{1,4}} \approx \frac{\rho}{t}\left(\frac{b}{a} + \frac{4 \ln 2}{\pi}\right). \quad [6]$$

Comparing this expression with Eq. [4], we see that in the limit of large p/a the potential drop between two adjacent stripes is equal to the bulk term plus a term equal in magnitude to that produced by current crowding. Thus, the difference between these two mea-

sured values, which in the ideal case approaches zero, should be equal to any other resistances in the circuit, including the contact resistance.

It has been shown[8] that if the contact resistance is large enough, the value of the current crowding resistance contained in Eq. [4] no longer applies, since the current flow is then modified by the contact resistance. Another difficulty arises from the failure of this method to evaluate the specific contact resistance, independent of geometrical factors. The justification for the use of the method is based on the following considerations. For small values of contact resistance, the method becomes increasingly accurate since the perturbation of the current flow under the contact will be more nearly determined by the resistivity of the semiconductor. Thus, in the case of very low contact resistance, where for example one is often unable to measure a "transfer length", this method may be preferrable to others. On the other hand, for large contact resistance values, errors in the estimate of the current crowding contribution become less important compared to the contact resistance itself. In the actual measurements made using this method, which will be discussed next, it was found that reasonable values can in fact be obtained in most practical cases.

Experimental

Standard DH as well as CDH type material was used for these measurements. The p surface was provided with a 1000 Å SiO_2 deposit, and photolithographic techniques were used to open 10-μm stripes in the dielectric film. After performing the indicated Zn diffusions, the metallization (consisting of 600 Å Ti, 800 Å Pt, and 1000 Å Au) was applied by thermal evaporation. The substrate was maintained at 250°C during the depositions, and the wafers received a further modest heat treatment during the evaporation of Sn used as the n contact.

Typical laser bars were cleaved from the completed wafer, and an array of stripes along a bar was covered with wax, as shown in Fig. 3. The bar was next immersed for 15 seconds in HF under ultrasonic agitation, which was generally sufficient to lift the metallization between stripe areas. Mounting of the bar on a printed circuit board, shown in Fig. 4, allowed convenient attachment of voltage and current probes to each stripe region.

The measurement is carried out as shown in Fig. 5, where the switching device is a high speed relay (e.g., Bristol Synchroverter). The square wave signal is measured on an oscilloscope or any instrument capable of measuring ac signals, and the amplitude ΔV

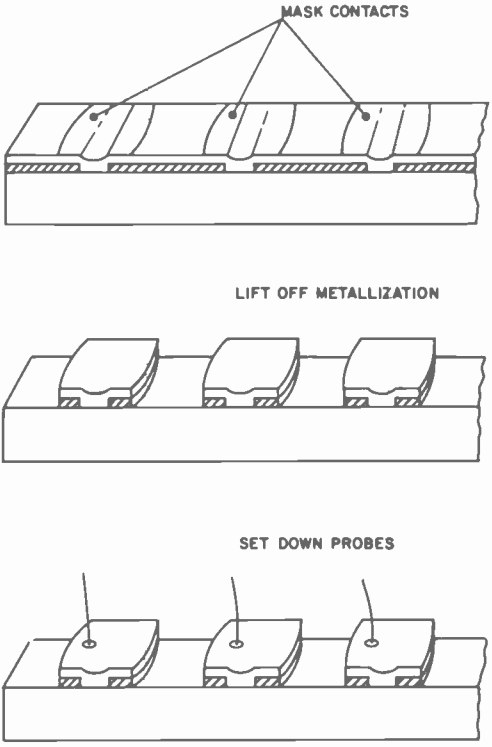

Fig. 3—Sample preparation for contact resistance measurements.

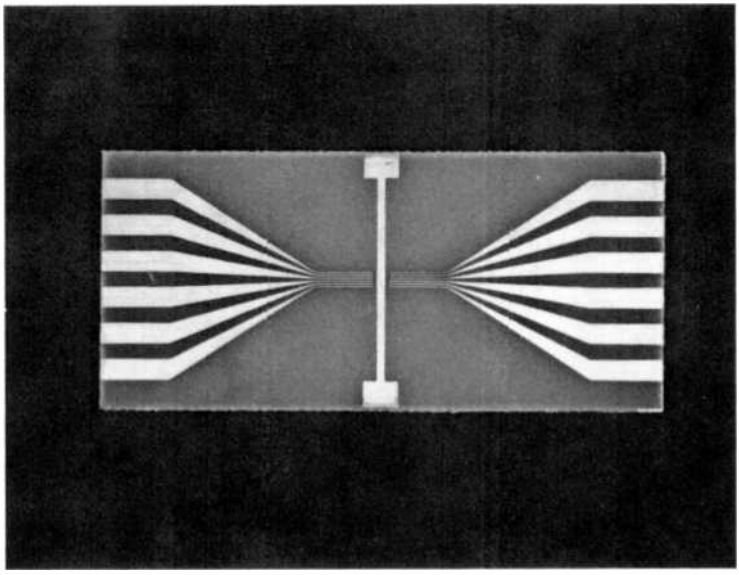

Fig. 4—Printed circuit board for voltage and current contacts.

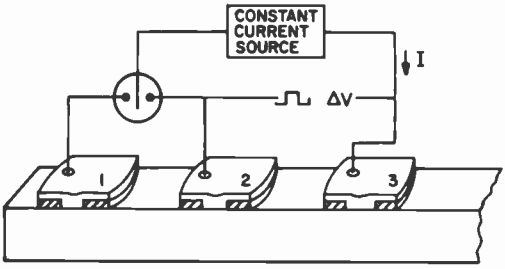

Fig. 5—Electrical connections for measurement of resistance of contact no. 2.

when divided by the current I yields the contact resistance R of the middle contact. As mentioned earlier, the specific contact resistance R_c is obtained by multiplying R by the contact area.

Three different surface doping levels were used to compare ohmic contacts as shown in Table 1. The first was obtained by diffusing zinc from a low (2%) concentration Zn/Ga source yielding a surface carrier concentration of approximately $1–2 \times 10^{19}$ cm^{-3}; the second was obtained by growing the LPE cap layer from a melt containing almost 50 at% Ge, which resulted in a doping level of $\sim 4 \times 10^{19}$ cm^{-3}; and the last utilized a diffusion of zinc from a $ZnAs_2$ source, yielding a surface carrier concentration of approximately 1×10^{20} cm^{-2}. These concentrations were not measured directly in the present work, but were obtained from published data for similar diffusions and LPE growths.

Conclusions

It can be seen from Table 1 that a surface carrier concentration of $1–2 \times 10^{19}$ cm^{-3} is just barely sufficient to produce good ohmic con-

Table 1—Comparison of Contact Resistances for Three Different Semiconductor Surface Concentrations

Type of Surface	Zn/Ga Diffused	Ge Doped LPE	$ZnAs_2$ Diffused
Surface Carrier Concentration (cm^{-3})	$1–2 \times 10^{19}$	$3–4 \times 10^{19}$	1×10^{20}
Contact Resistance (ohms)	3.3–3.7	0.2–0.35	0.1–0.5
Average Contact Resistance (ohms)	3.5	0.25	0.23
Specific Contact Resistance (ohm-cm^2)	$4.2–4.7 \times 10^{-5}$	$5.4–9.5 \times 10^{-6}$	$1.4–7 \times 10^{-6}$

tacts. On the other hand, both the Ge doped LPE layer (as originally pointed out by Ketchow[9]) and the highly zinc diffused surface produce adequate low-resistance contacts.

Results similar to these have been reported by Matino and Tokunaga[10] who obtained values of 2.7 to 4.3 $\times$ 10^{-5} ohm-cm^2 for a 1 $\times$ 10^{19} cm^{-3} surface concentration and 1 to 2.1 $\times$ 10^{-6} ohm-cm^2 for a 6 $\times$ 10^{19} cm^{-3} surface concentration. This, as well as the trend toward lower specific contact resistance with increasing surface carrier concentration, support the view that the present method is capable of yielding reasonable values in agreement with other measurement techniques. In contrast with other techniques, the present method has the advantage of allowing measurement and monitoring of contact properties on actual device material.

Ohmic contacts deposited according to the method described in this paper have been applied to planar DH lasers operated continuously at room temperature for periods up to 7 years. These devices had the rather high threshold current of 300 mA, typical of devices fabricated at that time, and the current density at the p-type contact was 6–8 kA/cm^2. It appears, therefore, that such contacts satisfy the need for low resistance and durability, while at the same time they are not the cause of any obvious material degradation.

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Positive-Resist Processing Considerations for VLSI Lithography

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Abstract—The resolution and packing density requirements for VLSI manufacture present new processing considerations for positive-resist optical lithography. More attention to the processing details are required as well as better control of processing conditions. The more violent dry etching techniques and high energy implants place new demands on the positive-resist masking properties. Topographical features make dimensional control more difficult and severely narrow the latitude of the positive resist process. Resist thickness variations, reflections off sidewalls, and standing-wave phenomena are responsible for the diminished process latitude. High quality aerial images enhance process latitude. Preserving the quality of the resist image reduces dimensional deviations on topographical features. Computer modeling of positive resist exposure and development provides useful information for accessing the effects of several processing parameters.

1. Introduction

Although positive resists have been commercially available for many years, only recently have they come into their own as the dominant lithographic imaging material for IC manufacture. In spite of their more stringent and less forgiving processing conditions as compared to negative resists, the move to positive resist materials has been spurred by the increased resolution demands of higher density VLSI designs. Even on flat surfaces the issues of dimensional control, edge acuity, process latitude, and process uniformity are difficult to reproducibly control. With the feature-size dimensional requirements now approaching the step height of the device topography, effective positive resist processing is made even more difficult. Other

aspects of VLSI processing are also placing more severe demands on the positive resist masking properties.

In this work, we discuss positive resist processing considerations for VLSI fabrication. Factors affecting linewidth control and process latitude on topographical features are then reviewed. Linewidth variations as a function of resist-thickness changes for various process conditions are presented. The experimental data is compared to computer simulations of the positive-resist development process.

2. Positive Resist Processing Sequence

Most conventional positive-resist materials used for optical lithography employ a novolac resin with a diazoquinone sensitizer. The following processing steps are usually employed to pattern these materials: dehydration bake of substrate, adhesion promoter application, resist coating, softbake, exposure, development, and hardbake. A resist strip step is eventually done after an etch or implant step. Although coating conditions, baking cycles, exposure and development parameters differ for various resist materials, the general trends we discuss here are valid for most positive resist materials. These trends are based on our experiences in processing HPR-204 resist material.[1] A brief discussion of each aspect of the positive-resist processing sequence follows.

2.1 Dehydration Bake

As the name implies, the purpose of this bake is to remove water from the substrate surface. Temperatures as high as 300°C with bake times of 30 to 60 minutes are recommended for dehydration bakes. Hydrated surfaces produce different hydroxide species that are often difficult to completely remove. At temperatures less than 650°C, silicon dioxide surfaces form silanol groups in the presence of water. Although the bulk of the absorbed water species is removed during a dehydration bake procedure,[2] complete removal of these polar functional groups is difficult with most dehydration bake treatments. Some surfaces absorb water more readily than others. Phosphorous-doped silicon dioxide and polysilicon pick up moisture quite readily. Longer and more severe baking sequences are sometimes required to remove moisture adequately. It is often advantageous to get these surfaces coated immediately after deposition or annealing.

2.2 Adhesion Promoter Application

The use of an adhesion promoter is essential during positive resist processing. These chemicals react with silanol groups (SiOH) on the substrate and attach an organic functional group. Although several chemicals can be used as an adhesion promoter, hexamethyldisilizane (HMDS) is by far the most common choice.[3–5] There are several methods for applying the HMDS adhesion promoter, including immersion,[3] flooding the wafer on a spinner, and vapor deposition. After allowing an adequate time for the HMDS to react with the wafer surface, the excess must be removed from the wafer surface. The presence of excess HMDS (more than a monolayer) can prevent the resist from wetting the wafer surface, and sometimes residual HMDS can react with the resist or film moisture to hinder development. Spin drying can be used to remove excess HMDS, although adequate ventilation and exhaust at the wafer chuck is required. A short ovenbake (5 min) is generally more effective than spinning, but temperatures in excess of 90°C can decompose the organic monolayer structure.

Vacuum vapor deposition can also be used for the HMDS treatment. HMDS has a sufficient room-temperature vapor pressure to react effectively with the wafer surface. If this treatment is performed directly after pulling the wafers from a furnace, the surface has effectively been fixed and subsequent exposure to moisture does not appear to deteriorate the adhesion properties. HMDS can be diluted with solvents and retain its effectiveness. It is important that the dilution solvent be compatible with the resist solvent system. Fluorocarbons and cellosolve acetate are generally used with the positive resist system. Ten and 20% HMDS solutions are commercially available. The use of HMDS solutions on aluminum metallization is of questionable value, but it is still widely used to help insure good photoresist adhesion to these surfaces.

2.3 Coating

Positive resist films for VLSI patterning applications are almost universally spin coated. Thickness control, uniformity, and low defect density are the primary requisites of a good coating process. Striation-free resist formulations are essential to insure uniform coating thickness across a wafer. Detailed studies[6] have shown that the most uniform coatings are obtained at spin speeds greater than 4000 rpm. Spin times of 30 seconds or more are required to obtain

uniform coatings at the 4000 rpm spin speed. More rapid spin speeds may permit shorter spin times, but speeds greater than 7000 rpm tend to produce spattering, do not reduce the spin-coating thickness appreciably, and generally produce greater spinner wear. Coating thickness uniformity on a good spinner can be made to be less than ±50 Å across 3-inch-diameter wafers. Viscosity and the evaporation rate of the resist solvent influence the coating thickness.[7,8]

Maintenance aspects are of crucial importance in the coating operations. Chuck wobble should be small. Chuck leveling and spin-speeds should be checked regularly. Adequate exhaust at the spinner cup, and well-cleaned waste trap and spinner chucks are essential for a clean, low-defect coating operation. Resist should not be allowed to flow over the wafer edge prior to spinning. This procedure helps to insure no backside coating of the wafer. Spattering of resist off the sidewalls of the spinner cup can be troublesome, but good spinner cup designs should minimize this effect. Ease of maintenance, the exhaust, and the waste disposal system are important features to examine when selecting coating equipment.

2.4 Softbake

The softbake procedure is one of the most crucial steps for positive-resist linewidth control. The purpose of this step is to remove resist solvent (usually, cellosolve acetate) from the film. Although this process in itself is not difficult, other competing processes make the softbake step difficult to control. Heating the resist film also tends to decompose the sensitizer and to remove moisture from the film. Both of these tend to make the resist less sensitive to the actinic wavelength. The moisture content of the positive resist film is extremely important. Good humidity control within the room and oven is important to obtain reproducibility. Humidities below 30% at 72°F present difficulties. Resist films exposed in the absence of moisture produce a base insoluble reaction product.[9,10]

The nature of the softbake oven is also important.[11,12] Topside and bottomside bakes produce different development characteristics for the resist film. The resist thickness change due to film shrinkage can also be different for various baking techniques. Microwave baking can also be used, but the bake cycle is dependent on substrate composition, doping, and the exact configuration of the microwave cavity.[13,14]

A controlled softbake cycle requires extraordinary attention to detail on a day-to-day basis if linewidth control for VLSI is to be

achieved. Slight differences in air flow, temperature and bake times can produce large changes in the resist development rates. Poorly controlled softbake cycles can produce slow development both at the resist surface and at the substrate interface.

2.5 Exposure

Positive resist exposure equipment for VLSI patterning applications is most certainly done with projection lithography. Light-source uniformity and intensity need to be carefully controlled as a matter of routine. Most projection printers are quite sensitive to temperature variations. Any breakdown in their air conditioning and environmental system can produce catastrophic results, and the machine should be checked out thoroughly before reuse after a breakdown. The exact exposure dose depends on several considerations, including resist type, resist thickness, the substrate, desired resolution, and feature size.

Wafer and mask flatness is important for the projection machines. Generally, flatness deviations within the exposure field should be kept below the Rayleigh limit, $\lambda/2(NA)^2$, where λ is the actinic wavelength and NA the numerical aperture. Flatness gauges are commercially available. It is important to note that the flatness of the substrate can change during wafer processing. Subtle changes in processing conditions, the substrate composition, and state of the impurities can dramatically change the susceptibility of the wafer to warpage.[15,16] High-temperature processing steps can be particularly troublesome. Single-side coatings with high stress films is another way to introduce flatness deviations. Flatness deviations can also produce registration errors.

The resolution capability of projection aligners is usually proportional to the actinic wavelength divided by the numerical aperture. Table 1 shows a comparison of the imaging characteristics of a

Table 1—Comparison of Imaging Characteristics of Perkins-Elmer 220 Projection Printer and a Typical 10× Direct Wafer Stepper

	Numerical Aperture	Wavelength (nm)	Depth of Focus $\lambda/2(NA)^2$ (μm)	Coherence (% Pupil Fill)
PE 220	0.167	365,405,436	±7.3	0.8–0.5
Stepper	0.32	436	±2.1	0.5
		405 and 436		

$\lambda/NA_{220} \approx 2.61$; $\lambda/NA_{Stepper} \approx 1.36$.

Perkin-Elmer 220 projection printer and a typical 10× direct wafer stepper. Nominally, the resolution capability of a wafer stepper is twice that of the Perkin-Elmer 220 exposure system. Fig. 1 shows the calculated aerial images[17,18] for a 10× stepper at various degrees of defocus with a one micron line-spacing grating pattern. Although these changes in the exposure pattern may appear to be slight, they produce dramatic changes in the quality of the resist image. At this resolution level on a stepper, the change in focus due to step heights becomes significant enough to change the aerial image the resist sees. Fig. 2 displays SEM micrographs of isolated-line resist images exposed on an Optimetrix 8010 10× reduction direct wafer stepper. Various features sizes are displayed along with two focus settings. The exposure and development parameters are adjusted so that the bottom of the resist image gives the 10× reduced features size on the mask for feature sizes well within the optical imaging resolution limits. The exposing wavelengths are 405 nm and 436 nm, the substrate is bare silicon, and the softbaked resist thickness is 1.3 μm. During the development cycle, less than 100 A of resist was lost from the unexposed portions of the resist film.

The resist images on the left in Fig. 2 were obtained at a focus setting within the Rayleigh defocus limit. The resist images on the right are outside the Rayleigh defocus limits listed in Table 1 (~ 3 μm defocus). Resist wall profiles for the 2.0 and 1.5 μm feature size are nearly identical for both the in-focus and defocus conditions. At the 1.0 μm feature size, the wall profile has degraded and the printed feature size is reduced for the nominal mask feature size. Degraded resist wall profiles are observed for the defocused resist images.

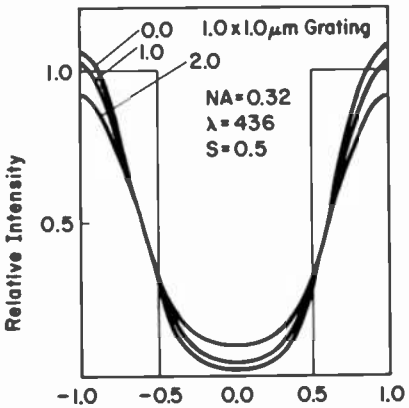

Fig. 1—Calculated aerial images for 10× reduction stepper.

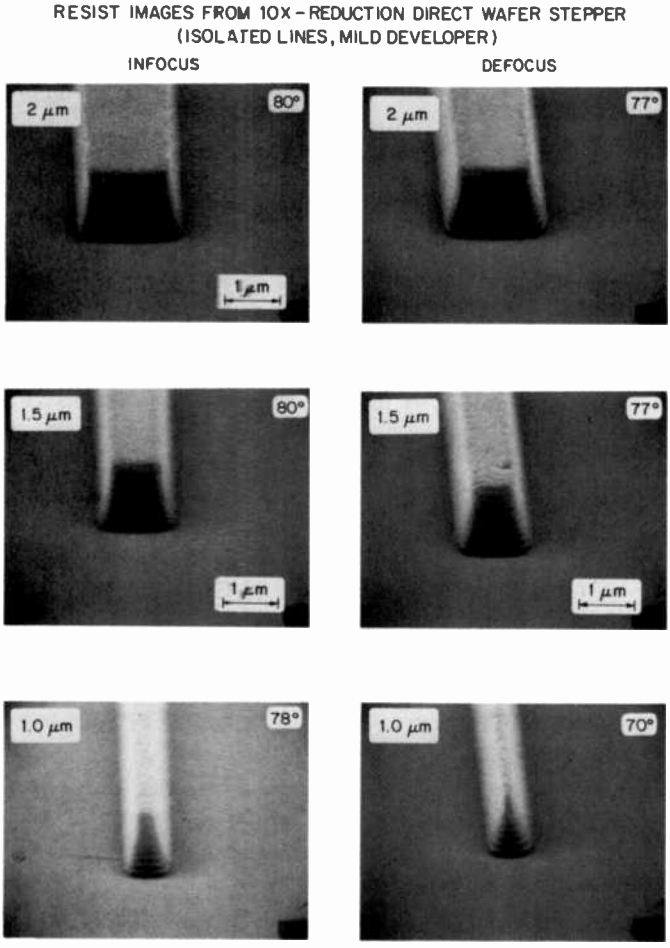

Fig. 2—SEM Micrographs of isolated line 10× reduction resist images, all at 20K, 85° magnification (constant exposure and mild development cycle).

More substantial changes in the linewidth and wall profile are obtained at the 1.0 μm feature size. All of these changes in linewidth control and the resist wall profile can be attributed to changes in the quality of the aerial image. Aerial image degradation for our 10× stepper begins at feature sizes below 1.4 μm. At this point, process latitude decreases and mask biasing considerations become much more important.

2.6 Development

Development of positive resist materials is usually done in an aqueous base. Several types of solutions are used and different results are obtained for each. These aspects will be addressed in more detail in the experimental portion of this work. Adequate temperature control for the development system is essential for reproducible linewidths. The contrast[19,20] of the resist system is related to developer concentration and the percent sensitizer in the resist formulation.[22] In addition, the basic species of the developer can also produce significant contrast and selectivity variations. Both exposed and unexposed resist are etched to some degree during the development process. It is usually advantageous to minimize the erosion of unexposed resist during the development process. Generally, slow development rates minimize resist thickness loss for unexposed regions, enhance selectivity between unexposed and exposed regions, and improve contrast. Development processes with these properties improve the quality of the final resist image.

The effect that the development cycle has on the quality of the resist image is illustrated in Figs. 2 and 3. Mild and harsh developer solutions are compared at similar levels of exposure to obtain the same feature size. The harsh developer has a faster development rate and attacks unexposed resist material to a greater degree. Fig. 2 displays resist images for the mild developer and Fig. 3 the resist images for the harsh developer. The unexposed resist film thickness losses are 100 Å and 400 Å, respectively. In every case, the wall profile has deteriorated for the harsh developer solution indicating a degraded resist image. The ramifications of degraded resist images on process latitude are discussed in more detail in Sec. 4.

Immersion, puddle, and dynamic spinning development processes are now being used. Immersion bathes are sometimes difficult to maintain, but satisfying results can be obtained. Proper agitation of the bath (usually nitrogen burst) and temperature controls are necessary. Used developer has to be discarded frequently because dissolved resist organics have a tendency to redeposit themselves on the substrate. Puddle and dynamic spin development use fresh developer for every wafer. These systems require a well maintained spinner and an adequate cup and exhaust design to contain the corrosive bases. These development systems also require suitable temperature controls. Small changes in developer concentration can dramatically influence the development rate and the etching of unexposed resist material.

Recently, there has been a trend to use metal-ion-free (organic)

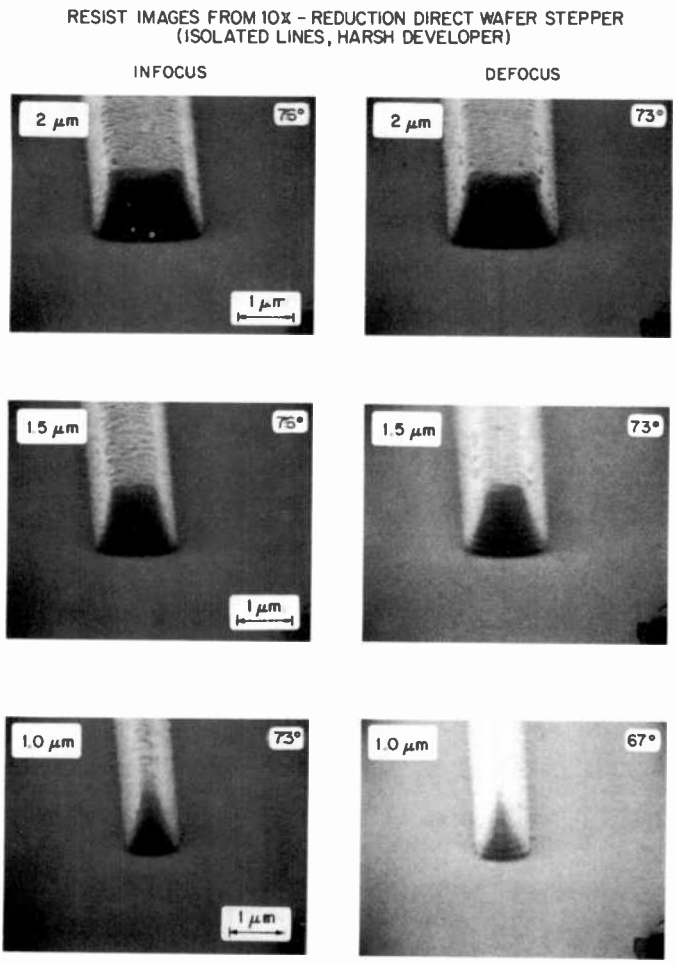

Fig. 3—SEM micrographs of isolated line 10× reduction resist images, all at 20K, 85° magnification (constant exposure and harsh development cycle).

developers rather than inorganic developers. The motivation behind this trend is to reduce the alkali metal contamination (mainly sodium) of MOS devices. At room temperatures, most commercial organic developers are characterized by more rapid development rates, less sensitivity between exposed and unexposed portions of the resist, and reduced contrast. These factors obviously contribute to degraded resist image quality. It is not clear at this point, whether milder development conditions for this type of developer will pro-

vide improved resist image quality. The development mechanism or competing side reactions for organic developers may be significantly different from those for inorganic developers. Radically different temperature dependencies (actually of opposite signs) of the development rates are observed for inorganic and organic developers,[22] as well as different development behavior for the same concentration or pH solution.

The main problems in the development process are resist lifting due to poor adhesion, difficulty in dimensional control due to process variations, and resist residues. The last can usually be corrected by using an over-exposure or over-development strategy, provided critical dimensional control does not then present difficulties. Usually, a proper mask bias strategy is needed to employ this residue minimization strategy.

2.7 Hardbake

The hardbake process traditionally follows the development of the resist. It is done primarily to harden the resist film and to improve resist adhesion to the substrate. The sensitizer in the resist is decomposed during the process, but generally through a different mechanism than UV exposed sensitizer. The resist also tends to flow during the hardbake cycle, which can result in increased dimensional control deviations. It is usually desirable to hardbake under conditions where thermal flow is minimized or to use a well-characterized, well-controlled resist flow process.

Post-development processing considerations of the resist have changed with VLSI processing conditions. Plasma etching and high-energy, high-dose implants present new processing considerations. High-energy, high-dose implants can heat the resist to temperatures greater than the normal postbake temperature. Resist flow can occur and cracking of the resist film is possible. In most cases, the cracking and excessive heating can be avoided with a cooled wafer platen with good wafer-to-platen contact. In some cases, it is desirable to increase the hardbake temperature to reduce the cracking phenomena. However, the higher bake temperature leads to resist flow and reduced dimensional control. Similar phenomenon can also occur under violent plasma etch conditions.

Plasma pre-treatments[24,25] and deep-UV exposure (<300 nm)[26,29] of resist films have been used to reduce resist flow phenomena at high temperatures. Several new resist formulations[30–32] have claimed

higher hardbake temperatures and greater resistance to resist flow. The reduction of thermal flow is not the only consideration for post-development bakes and treatments. During plasma etching, the resist material can react with or absorb chemical species from the plasma. Unwanted side-reaction products and contaminates are possible with plasma etching techniques. For example, positive resist film tends to absorb moisture. The presence of water contaminants in a plasma etch system can lead to plasma polymerization phenomenon. Thus, in many cases it is desirable to postbake the resist film immediately before plasma etching.

Another post development treatment that has been proposed involves the destruction of the resist sensitizer by UV exposure prior to the postbake treatment.[33] The motivation behind this strategy is to allow the nitrogen gas (the diazo decomposition product) to evolve from the film. Presumably, the normal postbake cycle can form a crust on the outside of the resist that prevents the escape of the nitrogen from the thermal decomposition of the diazo group. This trapped nitrogen tends to accumulate at the resist-substrate interface thereby reducing adhesion during wet chemical etches. A reduction in undercutting has been reported using the post development UV flood exposure technique prior to hardbaking.[27,33] However, UV-exposed (>300 nm) resist material usually flows to a greater degree during the postbake cycle, introducing more significant dimensional changes.[34]

2.8 Stripping Of Resist Films

Many of the implants and plasma etching techniques that a positive resist will see during VLSI processing require improved stripping procedures. Conventional sulfuric acid, peroxide stripping solutions can have difficulties removing resist that has been baked at high temperatures or seen some unusual plasma chemistries. Oxygen plasma stripping can remove the bulk of the resist, but a thin film of residual polymer materials frequently remains. Chemical cleaning is usually required to remove these residues.[35]

Plasma polymerization reactions[36–37] can occur during the plasma etching of the substrates which produce residues that cannot be removed effectively. Another factor during plasma resist strips is the tendency for sodium and other metals to be left behind on the substrate surface.[38–39] These residues are another justification for following the plasma strip operation with chemical cleaning.

3. Factors Affecting Dimensional Control on Topographical Features

The resolution requirements for new VLSI designs are rapidly approaching the dimensions of the step heights. Resist thickness variations will significantly affect the desired critical dimension. Fig. 4 is a schematic of a spun-on resist film on an isolated line feature. The thinner portions on the top of the step tend to be overexposed while the thicker portions on the bottom of the step tend to be underexposed. The maximum and minimum resist thicknesses tend to be associated with the bottom and top of the step, respectively. Although the maximum and minimum linewidths tend to be located at these positions, the exact position also depends on other factors. The reflectivity of the substrate is one of these factors. Fig. 5 is a ray diagram of probable reflections off the side-wall of a step. Since the resist films is also exposed by reflections off the substrate, regions near the top of the step tend to be underexposed and regions near the bottom of the step tend to be overexposed. This effect runs counter to the resist thickness change and can produce a linewidth deviation similar in magnitude to that incurred by the resist thickness change. This effect is also sensitive to the nature of the side wall and substrate reflectivity. Fig. 6 shows the relative sensitivity of spacewidth dimension for various exposures and resist thicknesses as determined for the Perkin-Elmer 220 projection aligner.

Superimposed on these two effects is the standing wave phenomenon.[40–42] A schematic of this phenomena is shown in Figure 7a. As a photoresist film becomes bleached, light is reflected off the substrate. This reflected light interferes with the incident light to produce a resultant intensity amplitude. Actually, this diagram is simplified, since the reflected beam is reflected downward again due to the refractive index change at the air-resist interface; hence, multiple reflections occur and the term standing wave arises. This interference phenomena modulates the exposure of the resist film as a function of resist thickness. The periodicity of the distances be-

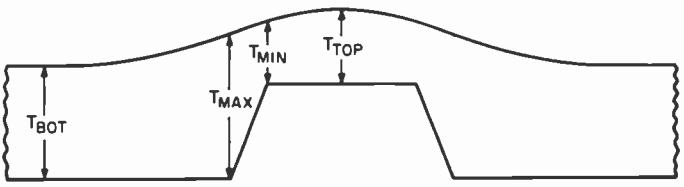

Fig. 4—Schematic of a spun-on resist film on an isolated line feature.

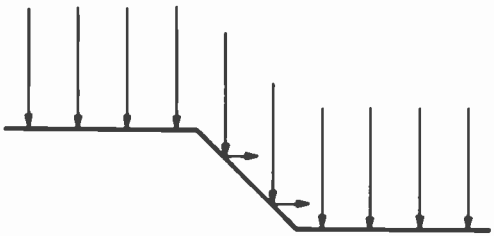

Fig. 5—A ray diagram of probable reflections around the sidewall of a step.

tween intensity node maximums or intensity node minimums is given by $\lambda/2n$; where, λ is the actinic wavelength and n is the refractive index of the resist film. For a 436-nm mercury-line exposure, this distance is nominally 1280 angstroms. There is an intensity minimum near the resist-substrate interface for any reflective substrate. The standing-wave phenonomen produces sinusoidal linewidth deviations that are a function of the resist thickness, i.e., the standing-wave phenomenon effectively modulates the energy coupled into the resist film as a function of resist thickness.[43] For thicker spun-on resist films, these deviations are less substantial

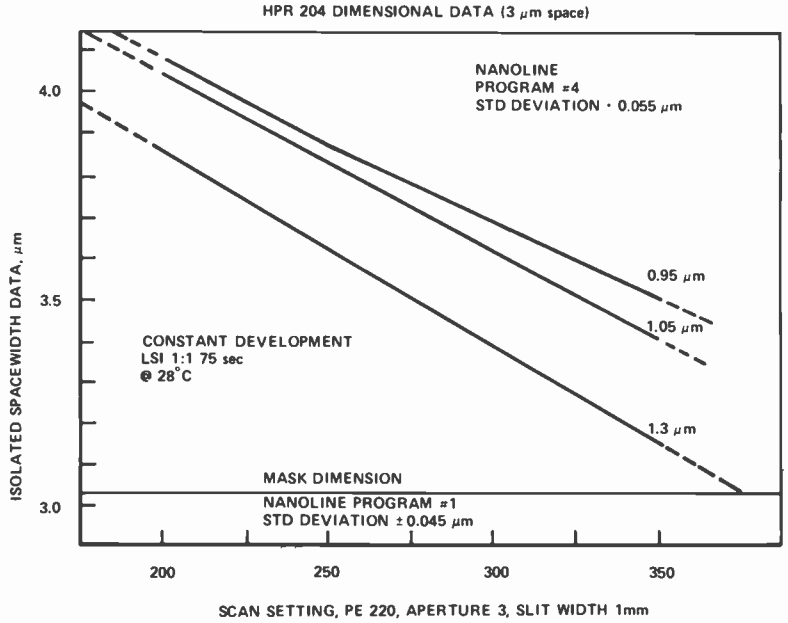

Fig. 6—Relative sensitivity of spacewidth dimensions to exposure and resist thicknesses variations.

because the total exposure energy becomes larger relative to the energy coupling differences. More pronounced standing-wave effects are observed for the more reflective substrates and the more monochromatic light sources. The magnitude of the standing-wave-induced linewidth variation has been reported to be as large as 0.4 μm on highly reflective substrates.[44]

There are additional difficulties in linewidth control for oxidized substrates. Here the oxide film is transparent (Fig. 7b) and has a refractive index similar to that resist material (i.e., 1.46 for oxide and 1.60 for positive-resist material). A maximum or minimum exposure node can exist at the SiO_2-resist interface depending on the resist thickness and the oxide thickness (See Fig. 7b).

To control linewidths on topographical features, a resist process must address each of these issues. Both resist thickness variations and substrate reflections should be minimized. Multi-level resist processing schemes[45–49] have been proposed that employ a spun-on sublayer to planarize topographical features, so that the top layer of resist exhibits less substantial thickness variations. Dye addition or prolonged baking of the sublayer have been used to minimize substrate reflections.[50] These techniques improve the situation, but,

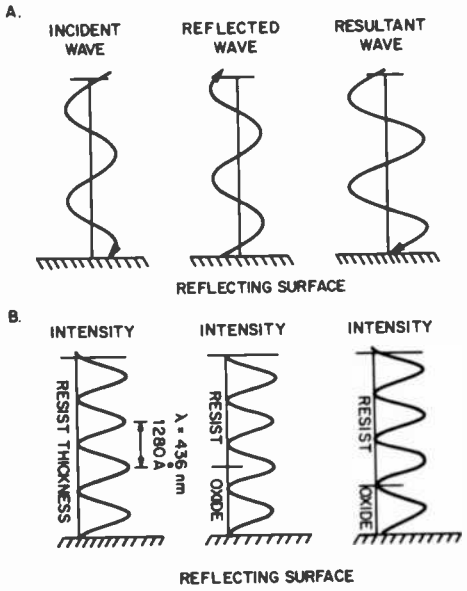

Fig. 7—Schematics of standing wave phenomena: (a) wave amplitudes on reflective substrates and (b) intensity variations on reflective and transparent substrates.

in practice, resist thickness variations can still exist for the top resist layer and the absorbance properties may not be sufficient to totally eliminate the effects of substrate reflections. Even under the best of circumstances, good control of positive-resist linewidth dimensions and adequate process latitude are crucial for realistic VLSI manufacture.

4. Process Latitude Considerations

The control of linewidth on nonplanar surfaces presents one of the most challenging problems for VLSI fabrication. Even careful control and constant adjustment of the lithographic process cannot prevent linewidth deviations on and at the edges of three-dimensional features. The resist thickness change at a step on the substrate produces a monotonic change in linewidth that, in many cases, is the dominant contributor to dimensional deviations. Other contributions are due to reflections off sidewalls and standing-wave phenomenon.

In this section we investigate the change in dimension dA, linewidth or spacewith, with a change in the resist thickness, dT. The ratio dA/dT we will term as the dimensional acuity. It is defined for a given film thickness and for specific exposure and development conditions. The most desirable dimensional acuity parameters show small changes in dimension for a given resist thickness change. This parameter depends on a number of factors, but in general, it appears that any factor that degrades the quality of the positive resist image also degrades the dimensional acuity.

In practice, the measurement of the dimensional acuity parameter is difficult for the cases of interest for VLSI manufacture. Standing wave phenomena that modulate the monotonic linewidth deviations as a function of resist thickness are relatively strong effects for the 10× reduction direct wafer stepper exposure tools due to the monochromatic nature of the actinic light source. However, careful experimental design can minimize these difficulties. Ideally, absorbing substrates or highly polychromatic light sources can be used to effectively eliminate the standing-wave effect.

A Rudolph film thickness monitor set at a film refractive index of 1.6 was used to monitor the resist thickness with sufficient accuracy. The resist thickness of a softbaked film is used for all our data. The dimensional measurements were made with a Nanoline III Critical Dimensional Computer. A nominal 3 μm space was measured with Program #4 with calibration of the spacewidth of the bottom of the resist image verified by SEM micrographs. A resist

thickness in the vicinity of 1.3 μm was exposed and developed to give the nominal dimension of the mask feature. The Nanoline gives precise and reproducible dimensional data, but this data is also sensitive to sidewall profile changes. However, while the absolute magnitude of the dimensional acuity parameters may not be entirely accurate, the measurements suffice for relative comparisons between different processing and imaging conditions. All other dimensional measurements at the reduced spun-on thicknesses were taken at the same exposure setting and for the same development cycle. Fig. 8 shows spacewidth data at various resist thicknesses using the Optimetrix 8010 wafer stepper. The substrate is bare silicon and the exposing wavelengths are 405 nm and 436 nm. The periodicity of the linewidth deviation closely matches that predicted by the standing-wave equation, ~1300Å.

The estimated magnitude of the standing-wave dimensional modulation between the maximum and minimum intensity nodes is 0.15 μm. The dimensional acuity monotonic linewidth deviation estimated from data at the intensity nodes maximums is nominally 0.4 and 0.8 for the mild and harsh developer solutions, respectively. The mild and harsh development cycles correspond closely to those used to obtain the resist images displayed in Figs. 2 and 3. Obviously, the development cycle, in this case the developer type, plays an important role in determining the dimensional acuity parameter. Process latitude in terms of controlling linewidths on topography is significantly reduced with harsher types of developers and developing cycles.

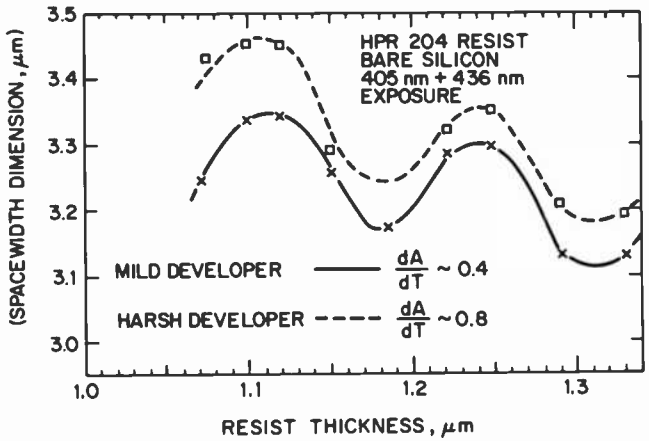

Fig. 8—Dimensional data for 10× reduction direct wafer stepper images for various resist-film thicknesses.

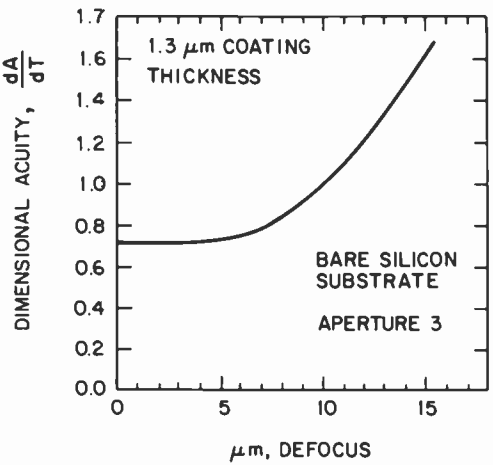

Fig. 9—Dimensional acuity parameter versus defocus for PE220 imaging system.

The quality of the aerial image also affects the dimensional acuity parameter. Fig. 9 plots dimensional acuity parameter data versus the defocus for the PE 220 imaging system. Greater linewidth deviations on topography (i.e., increased dimensional acuity parameters) are obtained for degraded aerial images.

This data shows that dimensional deviations on topography can significantly change with exposure and processing conditions. As the topography becomes more severe and at feature sizes approaching the resolution limits of the imaging tools, it appears that higher exposure doses and milder development cycles will be required to obtain acceptable process latitude. Preserving the quality of the positive image should be a primary consideration for a VLSI lithographic process.

5. Modelling of Linewidth Dependence on Film Thickness

The number of different experiments that can be performed has practical limitations. If we want to explore the full range of possible parameter values in a given experiment, therefore, it is desirable to be able to model the experimental conditions analytically. We have calculated the dependence of resist linewidth on film thickness using a modification of the program SAMPLE.[51] The program determines the optical image of a simple one-dimensional feature and then simulates the development process. To model the experimental situation we use as a fixed mask object, a long 3-μm-wide space.

All the resist parameters[21] used in the calculation are values that were previously measured on HPR 204 films. The parameter values used are listed in Table 2. The imaging system is a simulated 10× wafer stepper with numerical aperture of 0.28 and partial coherence factor of 0.7. The exposure dose is somehwat arbitrary and we use values typical of those used in practice. The development parameters are those measured for Hunt LSI developer diluted 1:1 with water. The development time is set so that a perfect image is produced in a film of nominal thickness. This means that when a film of that thickness is exposed with the 3-μm space, the width of the opening in the developed resist film at the substrate is also 3 μm.

The first set of calculations were performed for a resist layer on a silicon substrate. The illumination is assumed to be monochromatic and well collimated. The results also apply to substrates coated with SiO_2 or other transparent layers, since the interference effects are not significantly changed by a transparent layer. The second set of calculations used aluminum as the substrate. This surface is even more highly reflecting and can be expected to provide the most pronounced effect of linewidth variation. Two ranges of film thickness were explored: 0.5 to 0.7 μm and 1.0 to 1.5 μm. For the former we use an exposure dose of 50 mJ/cm², for the latter 70 mJ/cm².

Fig. 10 shows a typical profile of a developed resist pattern. The pattern is symmetric about $x = 0$, the midpoint of the object. The profile of the wall structure due to the standing-wave pattern is

Table 2—Parameter Values Used in the Model Calculations

Image Calculations

Equal amounts of 406 and 435 nm illumination
Projection system with numerical aperture 0.28
Partially coherent illumination (0.7)

Exposure Calculation

Resist (Dill parameters):

Wavelength	A(μm^{-1})	B(μm^{-1})	C(cm^2/mJ)
435	0.64	0.017	0.015
406	0.95	0.050	0.015

Resist Refractive Index:
1.65 at 435 nm
1.67 at 406 nm
Substrate Index: 5.61 + 0.19

Development Calculations for Positive Resist

Development rate: $g = 0.5\ (E/2.5\ mJ/cm^2)^{11/32} nm/s$ with saturation at 340 nm/s
Development time: 103 s

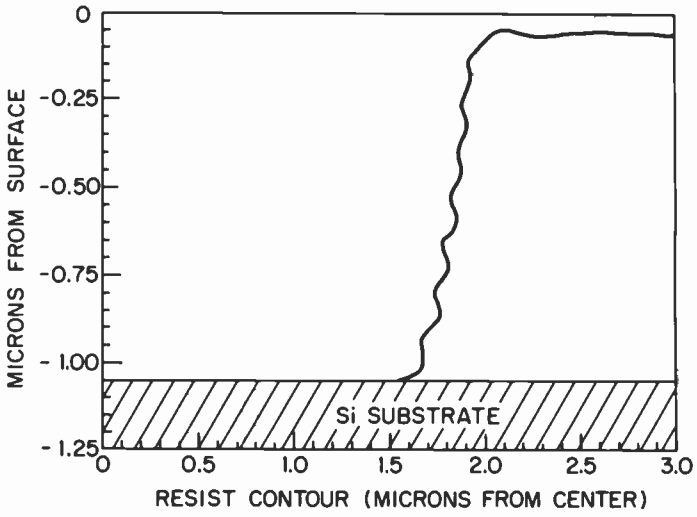

Fig. 10—Typical calculated resist profile after development.

clearly visible. The width of the developed opening (3.06 μm in this case) is defined by the coordinate at which the profile touches the substrate. This width, A, is plotted as function of film thickness, T, in Figs. 11 and 12 for the two thickness ranges.

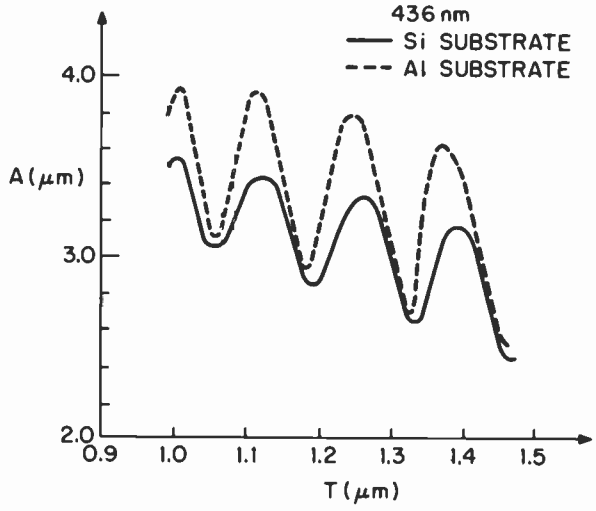

Fig. 11—Calculated variation of feature size with resist thickness for thick films. The object is a 3-μm-wide space; monochromatic light is used for exposure; and the calculation is performed for two different substrates.

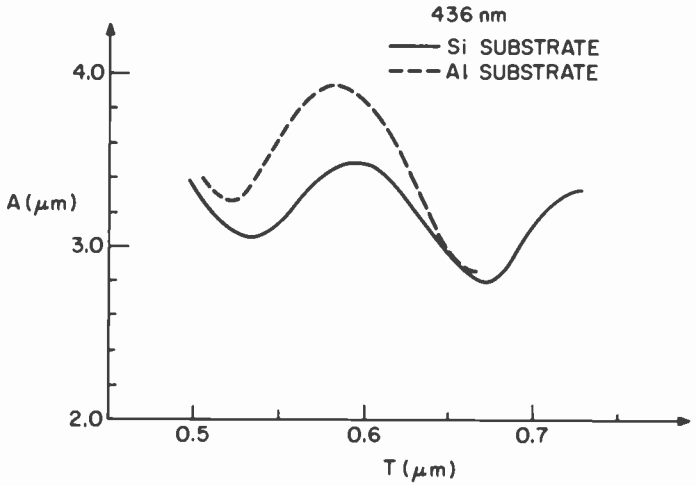

Fig. 12—The same plot as Fig. 11, but for thinner films.

We can compare the data of Fig. 11 for the thick film on the silicon substrate with the experimental results (Fig. 8). The general shape of the curves agree very well. The average slope $dA/dT = 1.0$, is somewhat larger than either of the experimental slopes. The interference oscillations are about twice as large as those of the experimental data. The latter were obtained by exposing with the Optimetix 8010 wafer stepper under illumination conditions in which both the 436 nm and 405 nm, as well as the continuous radiation in between, are used for exposure of the resist. To see whether this difference is significant to cause the reduced oscillation amplitude, we simulated it in the model by using an illumination with equal amounts of 405 and 436 nm radiation. The results are shown in Fig. 13 where the linewidths under the two radiation conditions are compared directly. It can be seen that the two-wavelength model fits the experimental results more closely, but that the experimental oscillations remain smaller. This may be due to less coherence than we have assumed or, perhaps, to diffusion of the sensitizer after exposure.

Fig. 11 shows that in the case of an aluminum substrate, we can expect considerably larger interference effects (the amplitude of the oscillations is about double that of the silicon substrate). This is due to the higher reflectivity of the aluminum compared to silicon (92% versus 49%) which causes the regions where the standing waves have minimum intensity to receive almost no exposure. Therefore, it will be much more difficult to control the linewidth on an aluminum substrate than on all the other kinds.

Fig. 12 shows the variation with film thickness in the case of thinner films. The general trend is the same as in the case of the thick films. In particular, the amplitudes of the oscillations are about the same in both cases.

The calculated linewidths are all derived for the case of planar structures. They thus describe only one part of the problem that arises due to steps on the substrate, that caused by changes in resist thickness. The reflections at the discontinuities in the topography and related features are not taken into account. In addition, the topographic steps and the finite film thickness mean that the image cannot be in focus everywhere. To see how large this effect can be, we calculated resist profiles for planar structures with varying degree of focus. In Fig. 14 we compare the resulting profiles for perfect focus with those in which the image is defocussed by 2 μm, which is approximately the theoretical depth of focus of this lens. The results show that we can expect a substantial increase in the variation of linewidth with film thickness for this much defocus.

So far the calculations have assumed a perfect resist, i.e., we predict that the linewidth in the substrate will be equal to the width of the opening in the resist at the interface. This may or may not be true, since the resist may not adhere perfectly to the substrate or the resist may be erroded during the etching step. In either case, the effect will usually depend on the exact profile of the resist edge. To demonstrate the magnitude of this effect we compare calculated resist profiles in Fig. 15 for films of 1.25 and 1.32 μm thickness.

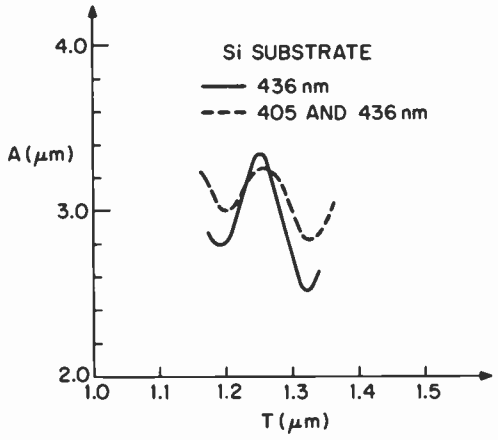

Fig. 13—Comparison of two different exposure conditions: monochromatic light and light containing two wavelengths.

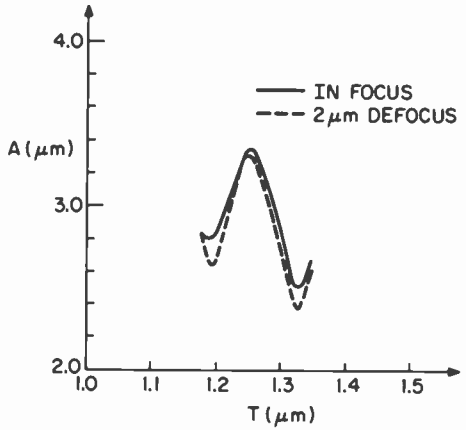

Fig. 14—Effect of defocus on film thickness variation.

These two values correspond to maximum and minimum values in Fig. 10. It can be seen that for the narrow space the line edge is much shallower than for the wide space, since the top of the profiles are much less affected than the bottom by the thickness variation. This implies that if the resist is erroded during etching of the substrate, the width of the etched space will grow faster for the shallower structure than for the steeper structure, and the resulting openings in the substrate will be more equal than would be predicted from Fig. 10 alone.

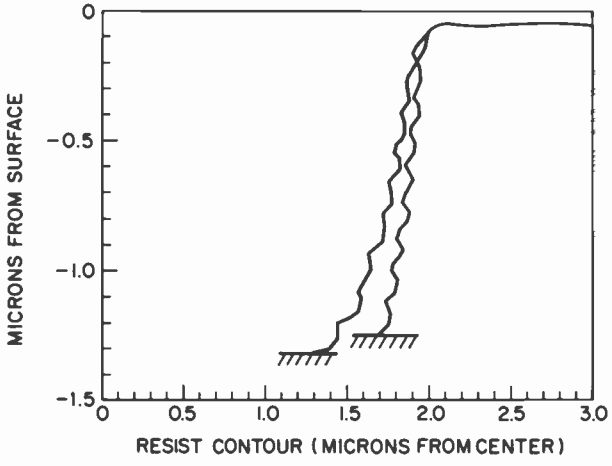

Fig. 15—Comparison of the calculated edge profiles for two films of 1.25 and 1.32 μm thickness. Exposure and development parameters are the same in the two cases.

6. Summary

The resolution and packing density requirements for VLSI manufacture present new processing considerations for positive resist optical lithography. More attention to the processing details are required as well as better controlled processing conditions. The more violent dry-etching techniques and high-energy implants place new demands on the positive-resist masking properties. Topographical features make dimensional control more difficult and severely narrows the latitude of the positive-resist process. Resist thickness variations, reflections off sidewalls, and standing-wave phenomena are responsible for the diminished process latitude. High quality aerial images enhance process latitude. Preserving the quality of the resist image reduces dimensional deviations on topographical features. Computer modeling of positive resist exposure and development provides useful information for accessing the effects of several processing parameters.

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Multilayer Resist Systems for VLSI Lithography

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Abstract—The increasing complexity of the integrated circuits creates a continuing demand for improved lithographic processes with higher resolution. One response to this demand is the increasing interest in multilayer resist systems. This paper reviews three kinds of such systems: two-layer systems, which generally use a wet development of the bottom layer; three-layer systems where the transfer and bottom layers are usually dry developed; and inorganic resist systems based on chalcogenide glass resists. The characteristics of these systems, along with their advantages, disadvantages, and uses, are discussed.

1. Introduction

The critical dimensions in VLSI circuits continue to become smaller and smaller as more and more devices are crowded into the same area. This puts increasing demands on the lithography, requiring the state-of-the-art imaging systems to be more refined. Even the best of these systems do not reproduce an object with perfect fidelity. The aerial image at the resist plane always has soft edges, which become more severe the smaller the dimensions are. To produce useable resist profiles from such images requires improved resists and better control of the resist processing.

Regardless of the lithographic system used, the exposure *inside the resist film* varies with depth in the film, due to absorption, diffraction effects, or reflection from the substrate. For exposure with an electron beam, there are additional effects due to backscattering in the film and from the substrate. These effects become important when the critical dimensions reach a magnitude comparable to the film thickness. On the other hand, the thickness of the resist film

cannot readily be reduced below the currently used 1.0 to 1.5 μm, because the film must protect the substrate during subsequent processing steps.

Most resist processing steps are not performed on flat surfaces, but on ones that have substantial steps on them due to previous procedures. The thickness of the resist film varies as it crosses these steps, and thickness changes translate into changes in feature sizes and profiles.

Despite all these difficulties, increasingly small patterns are being produced successfully with improved processes. One of the newest techniques is to separate the imaging and the protection requirements and assign them to two or more separate film layers.[1] The two processes most commonly used are shown schematically in Fig. 1. In both cases an organic film is first spun onto the substrate to form the *bottom layer*. It is thick enough to provide the protection for the subsequent processing steps. Because the film is applied from solution, the surface tension causes its top surface to be smoother than the underlying substrate surface.

The *top layer* consists of a film of energy-sensitive material, which can be exposed in one of the conventional lithographic imaging systems. This film can be made thin, so that the exposure is relatively uniform throughout its thickness. Because of this uniformity and because the film is more planar than it would be without the bottom

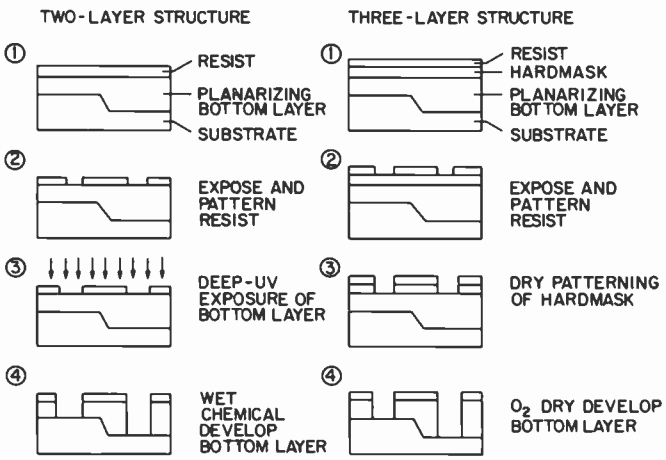

Fig. 1—Schematic of two- and three-layer resist structures.

layer, the imaging will exhibit higher fidelity with increased resolution and linewidth control. Thus we can expect a more accurate reproduction of the object. There are also some energy sensitive materials that have unusually useful properties and that can only be prepared and exposed in very thin layers, such as some of the inorganic materials. These must be applied over a thick bottom layer.

Once the top layer is exposed and developed, the pattern must be transfered into the bottom layer. This may be done with another photographic step, as shown by the two-layer structure in Fig. 1, or with one or more plasma etching steps. For some applications, a very thin intermediate *transfer layer*, or *hard mask*, is used to improve the fidelity of the pattern reproduction in the bottom layer, creating the three-layer structure shown in Fig. 1.

In this paper we will discuss two-layer systems, three-layer systems, and the special case of inorganic resist systems.

2. Two-Layer Resist System

2.1 The Portable Conformable Mask

The simplest multilayer resist system uses PMMA (polymethyl methacrylate) as the bottom layer and some other radiation sensitive material as the top layer. It evolved out of the conformable masking technique[2] which was used to improve the contact between the resist and the mask during high-contrast contact printing. Lin[3] generated the "portable conformable mask" in situ by depositing a film of positive photoresist (AZ 1350) on the PMMA bottom layer. This top layer is exposed by one of the conventional lithographic techniques. In the case of conventional optical imaging with near-UV light, the PMMA is unaffected by this step. The top layer can then be developed into a simple and effective mask for flood exposure of the PMMA film with deep-UV light. PMMA is only sensitive in the deep-UV region (210–260 nm), where the positive photoresist absorbs heavily.[4] The flood exposure of the bottom layer is a simple step, which does not require sophisticated lithographic equipment.

With this system, the contact between the two layers is as close as is physically possible. The exposure of the bottom layer can then best be described as a proximity or diffraction printing process.[5] When the sandwich is illuminated with deep-UV light a very precise contact print is produced in the upper region of the bottom layer. However, further down in the PMMA film the image is degraded due to diffraction effects. Depending on the dimensions of the structures involved, various groupings of diffraction peaks can

appear. Fig. 2 shows an example of a calculated intensity pattern 1 μm below the surface of the PMMA. The conformable mask has opening that extends from $x = -1$ to $x = 1$ μm. Despite these complicated exposure patterns, it has been possible to produce PMMA structures with small dimensions and very high aspect ratios.

In addition to providing improved resolution through the intimate contact, the portable conformable mask system has other advantages compared to a single-layer resist structure. Since the bottom layer is the one used to protect the substrate during the subsequent processing step, the top layer need not be very thick. This means that the resist film will be more uniformly exposed, and distortion of the image due to diffraction of the light in the film will be minimized. This results in sharper images with higher resolution.

The bottom layer may also serve to provide a smoother substrate for the resist film. The substrate wafer usually has significant topographical structure on its surface due to previous processing steps. Resist films applied to such surfaces will show considerable variations in thickness, leading to fluctuations in line width of the developed image.[6] An organic film of the type used for the bottom layer generally forms a smoother surface than the underlying substrate exhibits. More uniform resist films can be deposited on such a surface. The amount of smoothing obtained depends strongly on the nature of the film that forms the bottom layer.[7] If the softening temperature of the film is sufficiently low, then additional planarization can be produced by flow during the bake cycle.

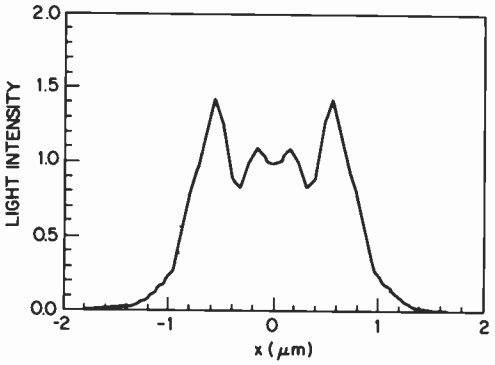

Fig. 2—Diffraction effects in the conformable mask system. The top layer (mask) has a 2-μm-wide slit in it and is uniformly illuminated by light of intensity 1. The light distribution in the bottom layer at right angles to the slit is shown in a plane 1 μm below the interface of the two layers.

The two-layer optical scheme has been commonly used to provide good patterns for metal lift-off.[1] This is possible because the exposure-development of the bottom layer is performed separately from that of the top layer. An example of this possibility is shown in Fig. 3, where fine line patterns are produced on a substrate with very pronounced topography. A conventional single-layer structure is shown for comparison.

2.2 Reduction of Interference Effects by Absorption

One of the limitations of optical lithography is that light is partially reflected at every interface. This causes interference effects to occur in the exposure pattern. The problem is particularly severe for resists coated on highly reflecting substrates, such as Si and Al. The optical interference of the incident and reflected beams changes the amount of energy coupled into the resist film for different thicknesses, leading to changes in feature sizes.[8] At the same time the

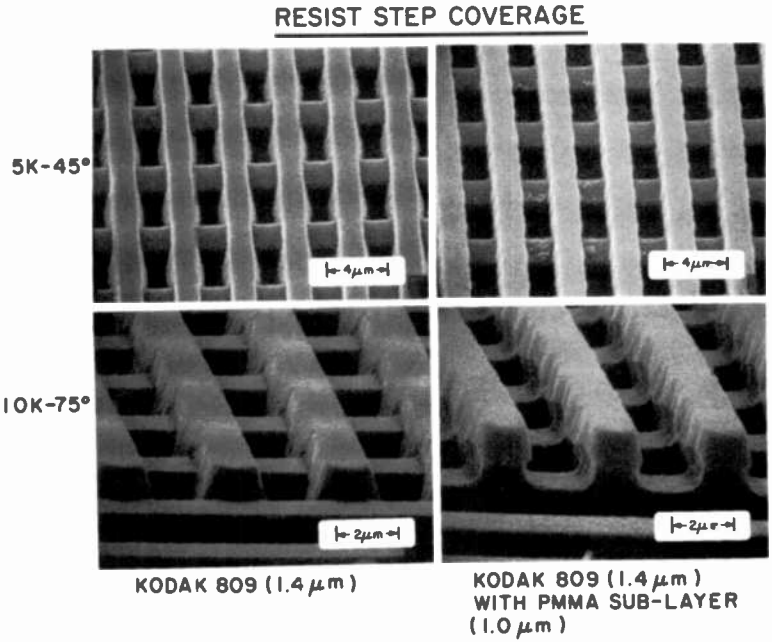

Fig. 3—Comparison of profiles generated with a two-layer process (right side) and with a conventional resist process (left side). The substrate is a grating of 3 × 3 μm dimension in 1-um-thick polysilicon. The resist (1.4 μm of Kodak 809) is patterned with a 2 × 2 μm grating at right angles to the substrate pattern.

exposure produces alternate layers of high and low solubility in the resist. During development, this may cause additional changes in the line width as the resist thickness changes.[6]

In a double-layer system, the interference effects during the optical exposure can be reduced by making the bottom layer absorbing at the wavelength of optical exposure of the top layer. It is necessary, however, that this absorption not produce any photochemical changes. If the bottom layer is not absorbing at this wavelength (as is the case for PMMA), then dyes must be incorporated into the film.[8] There is, however, a limit to the amount of absorption that can be tolerated due to the necessity of aligning the exposure to alignment marks that are located on the substrate. For direct-step-on-wafer tools, the alignment is usually performed with light of a wavelength identical, or close to, the exposing wavelength. In that case any increase in absorption reduces the signal-to-noise ratio of the alignment process.

To obtain a more quantitative feeling for these effects, we have performed some model calculations. In addition to the absorption of the bottom layer, we have also considered the reduction of coherence that may come about as the light travels twice through the relatively thick film. The calculations were performed with the program SAMPLE[9] which models exposure and development of resist layers. It calculates optical images of one-dimensional lines and spaces, the corresponding exposure of the resist, and the developed profiles. The substrate may consist of a bulk material with up to two films on it. This allows us to model, for example, tri-layer resist structures on a bulk substrate or bi-layer resist structures on a Si-SiO_2 substrate.

For these calculations we have used the situation of an aluminum film substrate, such as would be used for the metallization layer. This will produce a maximum amount of interference and will demonstrate the magnitude of the problem. The resist system consists of a thick PMMA bottom layer and a thin top layer of conventional positive resist, such as HPR 204. The values of the various parameters are shown in Table 1.

An example of the calculated results is shown in Fig. 4. Illumination is by a monochromatic lightsource of 435-nm wavelength, such as is used in most of the step-and-repeat machines, and the object is a 3-μm wide slit. The edge of the resist profile is shown after development for five different development times. The bumps in the edge, separated by one-half wavelength in height, are due to the interference effects. For this particular resist thickness, there is a very shallow "foot" at the bottom of the edge, which may cause difficulty with the subsequent processing step. An even more severe

Table 1—Parameter Values Used in the Calculations

Pattern image is a space of width 3 μm.
Projection system with numerical aperture 0.28.
Incoherent illumination at 435 nm.
Image in focus.
Exposure dose: 75 mJ/cm^2

Resist Parameters:
- Absorption coefficient: 1.055 μm^{-1}
- Absorption coefficient after bleaching: 0.094 μm^{-1}
- Bleaching parameter: 0.02 cm^2/J
- Film thickness: 0.5 μm
- Index of refraction: 1.65

PMMA layer index of refraction: 1.50

Aluminum substrate optical constants: 0.40–i4.84

Development parameters:
- Differential development rate: Exponential dependence on dose with slope 1.38

problem occurs when the thickness of the bottom layer changes, as it does when there are steps in the substrate. Fig. 5 shows three resist profiles after 57 second development for three different values of bottom-layer thickness. There are large variations in linewidth. In fact, for the bottom layer thickness of 2.05 μm, the resist is not cleared out at all. This is an extreme case, but it demonstrates the possible problems.

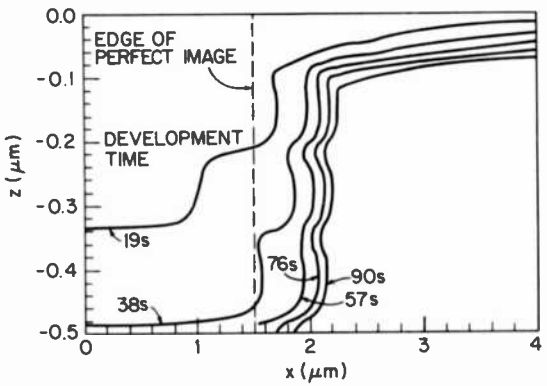

Fig. 4—Calculated resist contours after development for the times indicated. The substrate is Al coated with 2.00-μm PMMA and 0.5-μm HPR 204 resist. Exposure is by a direct-step-on-wafer machine with a 3-μm-wide slit as the object. The system is symmetric about $x = 0$. Z is the distance from the original resist surface. The parameters used in the calculation are listed in Table 1.

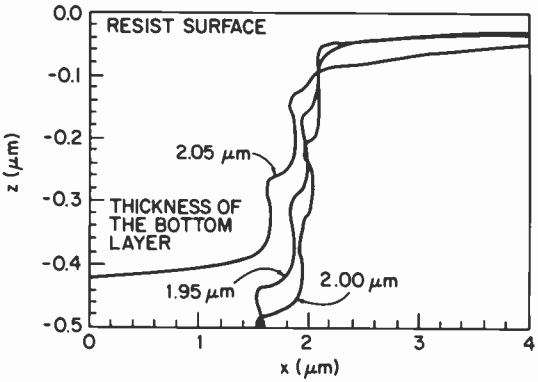

Fig. 5—Developed resist contours for three different thickness values of the bottom layer. The parameters are the same as in Fig. 4. The bottom layer is assumed to have no absorption and the development time is 57 s.

Next we include various degrees of absorption in the bottom layer. From the optical constants, we calculate the fraction of the incident light reflected back at the viewer off the substrate, R. Typical values are shown in Table 2, which also shows the development time required to produce a resist opening of the nominal 3 μm for a bottom layer thickness of 2.00 μm. As mentioned above, this time decreases with increasing absorption due to the increased coupling of light energy into the film. The Table also shows the width of the space produced with a bottom layer of 2.05 μm. We expect that an R of 0.05 is sufficient to perform a successful alignment. It corresponds to an absorption coefficient of 0.48 μm^{-1} for the 2-μm thick PMMA layer. The calculated profiles for this absorption coefficient in the two extreme cases of bottom-layer thickness (2.00 and 2.05 μm thickness) are shown in Fig. 6. The situation is considerably improved compared to zero absorption, with an edge shift of 0.1 μm

Table 2—Absorption and Development Times

Absorption coefficient (μm^{-1})	R	Development Time (sec)	Width of Space for Bottom Layer 2.05 μm (μm)
0.0	0.34	57	not cleared
0.14	0.19	46	2.48
0.29	0.11	40	2.72
0.48	0.05	38	2.84
0.86	0.01	38	3.00

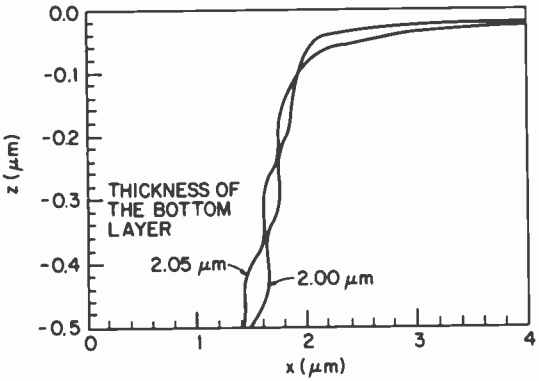

Fig. 6—The same curves as in Fig. 5 when the bottom layer has an absorption coefficient of 0.48 μm^{-1} at the exposing wavelength. Development time is 38 s.

remaining. At an absorption coefficient of 0.86 μm^{-1} the two edge profiles coincide, but $R = 0.01$ is probably too low for practical use.

2.3 Electron-Beam Imaging

The PMMA-resist double-layer technique has also been applied to the case where the original image is generated with e-beam lithography.[10,11] This realizes some of the same advantages as optical imaging. In addition, it can help overcome some of the limitations of e-beam lithography. Hatzakis[10] was able to improve the low sensitivity of PMMA and related resists by using a very thin top layer. Lin and Chang [11] addressed the major limitation of fidelity and resolution, the backscattering of electrons from the substrate. This causes a spreading of the exposed area, leading to poorer resolution and edge profiles. It also increases proximity effects, since adjacent exposed areas will absorb some of the electron energy. By using PMMA, which has a lower density and atomic weight than Si or SiO_2, as the effective substrate, the back scattering of electrons is diminished and the proximity effect is reduced.[12]

With electron beam exposure, it is not possible to expose the two layers independently, as in the optical case, because the electrons penetrating into the PMMA partially expose this material. The UV flood exposure can still be performed, but the extra exposure must be taken into consideration. Hatzakis et al have taken advantage of this phenomenon to form a structure with a single lithographic exposure.[10] The top layer still forms an etch mask when it is devel-

oped, but the bottom layer develops faster than the top layer, leading to undercut walls suitable for lift-off. The effect can be made more dramatic by using two different developers each of which selectively dissolves one layer with little effect on the other. This work was extended by Todokoro to combinations of PMMA and MPR resists.[13]

3. Three-Layer Resist Systems

The three-layer resist process was first reported by Moran and Maydan at Bell Laboratories.[14,15] These initial experiments used x-ray lithographic exposure tools. Since that time, similar experiments have been reported using other lithographic techniques that include optical,[8,16–20] electron-beam,[21–23] and ion-beam [24] exposures. The difference between these techniques and the two-layer system is the addition of a thin inorganic hardmask, usually less than 0.3 μm thick. Both the hardmask and the bottom planarizing layer are usually patterned by dry etching techniques. However, one worker[25] has proposed etching a thin hardmask material using a wet chemical process.

Resist features as small as 20 nm and gold lines as narrow as 40 nm separated by 80 nm center-to-center have been fabricated with a three-layer process using e-beam lithography.[21,22] Lines as narrow as 200 nm in 2-μm Hunt positive resist have also been fabricated using laser holography.[23]

Both sublayers (hardmask and planarizing layer) have different material requirements depending on the lithographic exposure tool, dry processing techniques, substrate composition, and their intended use. For example, SiO,[11] sputtered SiO_2,[16] spun-on SiO_2,[17,18,20] Si,[19,23] Si_3N_4,[23] and metals[21–23,25] have been used as hardmask materials.

In this discussion we will review the various material requirements for the hardmask and the planarizing sublayers. Since reactive ion etching (RIE) (also called reactive sputter etching) is of crucial importance for this technology, a brief discussion of this dry etching technique is included.

3.1 Planarizing Sublayer

The organic bottom layer used for planarizing device topology for most three-layer systems has been positive resist material (HPR 206 or AZ 1450J). Polyimides and PMMA have also been employed. The thickness of the sublayer is usually 1.5 to 3.0 times that of the

step height on the substrate. The positive resist material appears to be the most popular choice because of its superior planarization properties and its widespread use as a high purity lithographic material. Polyimide materials offer greater temperature stability (up to 350° C), so that a wider range of hardmask deposition techniques and conditions can be employed. However, this material has relatively poor planarization properties,[7] its purity is unconfirmed in IC processing, and it appears to be not as sharply defined during RIE development. PMMA sublayers also have poor planarization properties[7] and tend to undercut during RIE development.

The importance of obtaining highly planar surfaces to minimize resist thickness variations on all types of topographical features has been discussed previously.[7] Comparing Figs. 7 and 8 shows the ben-

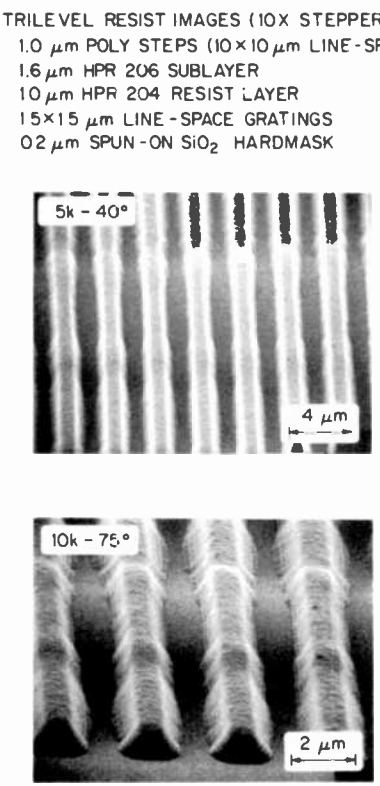

Fig. 7—SEM photographs of resist profiles formed in the top layer of a trilayer system. The exposures were produced by a 10× stepper and consisted of a pattern of 1.0-μm lines and 1.5-μm spaces. The parameters are listed on the figure.

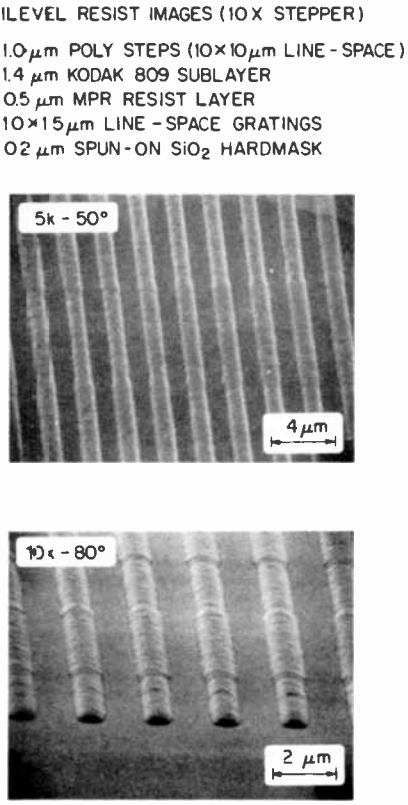

Fig. 8—Similar to Fig. 7 but with a top layer of MPR and a bottom layer of Kodak 809. The exposure gratings have 1.0-μm lines and 1.5-μm spaces.

efits of obtaining highly planar sublayer structures. Fig. 7 shows positive resist images on 10 × 10 μm topography with a conventional planarization sublayer. The linewidth deviation on the topography is ~0.4 μm. Fig. 8 shows positive resist images using a superior planarization sublayer. The linewidth deviation has been reduced to 0.1 μm. This linewidth deviation has been attributed to standing-wave phenomena and differences in resist exposure due to sidewall reflections.

All sublayers usually must be cured at temperatures in excess of the hardmask deposition temperature and of future processing temperatures. Thermal decomposition products (outgassing) can destroy the integrity of the hardmask material; cracking of the hardmask is also possible.

For e-beam, x-ray, and ion-beam lithography, the sublayer material requirements are not as demanding as they are for optical lithography. Planarization, beam stability, and removal of the resist layer from the substrate are the only requirements. For optical lithography, it is desirable that the sublayer be absorbing at the actinic wavelengths so that standing-wave phenomena and sidewall reflections be minimized. Positive resist material can be made absorbing after the sensitizer is thermally or optically destroyed by continued heating at high temperatures, usually in excess of 160° C. Dye additions to the sublayer have also been used to make the sublayer absorbing.[8] These additions do not appear to modify the RIE development characteristics of the sublayer.

Fig. 9 shows a comparison of a conventional resist system and a trilayer system with a highly baked sublayer of 1-μm Al topography. The trilayer structure shows dramatically improved dimensional control.

The preferred dry processing technique for the sublayer has been

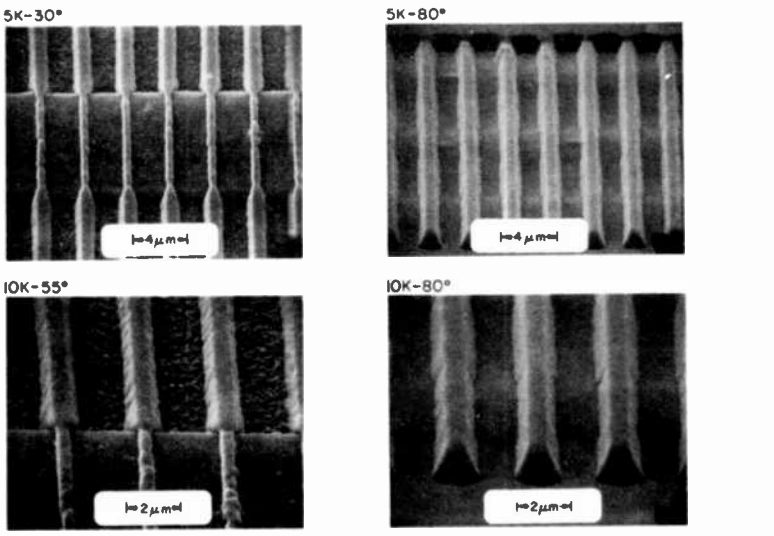

Fig. 9—Comparison of profiles generated with a three-layer process (right side) and those generated by a conventional resist system. The substrate is a grating of 10 × 10 μm dimension in 1-μm thick Al. The resist is pattern with a 1.5 × 1.5 μm grating.

RIE in O_2 plasma. Nearly vertical side walls are obtained and overetching of the sublayer does not appear to produce significant undercut with positive resist sublayers. Etch rates as high as 100 nm/min have been reported with minimal undercutting and dimensional losses (<0.2 μm).[8,17,18] Different planarizing sublayers may have different etch rates under the same dry etch conditions. For example, in oxygen etch-gas environments, PMMA generally etches at twice the rate of conventional positive resist material.[27]

The planarizing sublayer must usually be stripped in O_2 plasmas after hardmask removal. The issues of metal residue contamination[28,29] and radiation damage[30,31] to IC device structures must be addressed here as well as during RIE development of the sublayers.

3.2 Hardmask Selection

The primary function of the hardmask is to provide a plasma etch mask (RIE) for development of the planarizing sublayer. In addition, mixing and interface phenomena between the organic sublayer and resist layer are eliminated. Resists that have poor plasma-etch resistance characteristics can, under some circumstances, be used for pattern definition.

Other criteria must also be met besides O_2 RIE development resistance. Deposition temperatures must be kept below the thermal decomposition temperature of the sublayer (for resist material, <200° C). These techniques involve sputtering, evaporation, or plasma deposition. Maintaining clean operating conditions for the machines is not trivial. The relatively thin films must be uniform and defect-free. Spun-on SiO_2 glasses have also been used.[17,18,20] This material is attractive because of its ease of application and integration into the usual photolithographic processing schemes. These films, too, must be of sufficient quality and defect-free to produce uniform etching properties. Exposure of the glass solution to air causes decomposition of the film-forming ingredients, and rapid evaporation of the solvent prior to spinning can cause deposition of unwanted precipitates.

Thicknesses of the hardmask usually vary between 0.1 and 0.2 μm. This thickness provides reasonable plasma-etch resistance and minimal dimensional losses of the pattern during hardmask definition. One worker has proposed using thicker layers to prevent dimensional losses during development of the sublayer.[16] It should be pointed out that although the relative etch rates of the organic resists and the hardmask provide an indication of the relative dimensional losses, the sputtering action at the edge of the mask or

resist material may produce more substantial dimensional losses than indicated. Table 3 lists various hardmask materials and associated plasma definition data used in tri-layer processing techniques. All of the reported hardmask materials have been defined in the reactive ion etch mode. SiO_2 layers are currently the most popular choice for optical lithography. Metals (Ge and Al) and Si have been used in e-beam lithography to prevent charge build up. The metal layers are generally less than 0.1 μm thick for the e-beam application. Transparent hardmasks on an absorbing sublayer are desirable for optical lithographic applications, because reflections off a lower lying layer generally degrade the quality of the resist image.

3.3 Dry Etching Considerations

Dry etching techniques play a crucial role in the three-layer process. RIE has been the method of choice in this technology due to the need for highly directional etching with minimal dimensional losses. Actually, the synonymous term, reactive sputter etching, is more descriptive, since sputtering action accounts for the anisotropic etch characteristics. The term RIE will be used here, however, to be consistent with the literature.

RIE reactors usually have a parallel-plate configuration. The operating pressures range from 10^{-3} to 10^{-1} Torr. The electrode on which the substrates are mounted is powered. The low pressures and high potentials between the electrodes (i.e., increased mean free path) enables the reactive ions to be delivered in a directional fashion. The physical etching components can produce anisotropic etching with reasonably good selectivity.

Selecting the optimum RIE processing conditions involves several issues and in many cases compromises must be made. Low pressures

Table 3—Hardmasks for Trilayer Resist Processing

Material	Thickness (nm)	Etch Gas	Reference
SiO_2 plasma deposited	100	CHF_3	14,15
SiO_2 sputtered	200–1000	$CF_4 + H_2$	16
SiO_2 spun-on	100	$CHF_3 + CO_2$	17,18
SiO_2 spun-on	200	CF_4	20
SiO evaporated	100	CF_4	26
Si evaporated or sputtered	80	CF_4	19,23
Ge	25	CF_4	21,22

typically produce low etch rates, and high potentials appear to reduce selectivity. The move to higher pressures and low potential, however, makes anisotropic etching more difficult. In addition, plasma polymerization phenomena are more prevalent under these conditions.[32–34] Fluorocarbon gas mixtures have a tendency to form polymeric material on both the wafer surface and the reaction chamber. The addition of oxygen-containing gases to the fluorocarbon gas mixture has been used to minimize the effect of plasma polymerization.[34] The sputtering nature of the RIE processing also can produce residues from sputtered electrode and reaction chamber materials. Sputtered aluminum from substrate electrodes has produced residues on wafers during oxygen RIE definition of the planarizing layer. The difficulty has been overcome by coating the Al electrode with an organic material.[16]

Substrate heating during the etching process can introduce a variety of problems. Even though many electrodes are water-cooled, poor contact between wafer and electrode can cause excessive heating to occur at the wafer surface. Thermal decomposition of the organic planarizing sublayers is possible under some conditions. Patterned resist material can flow to a degree during the process and presents serious dimensional control problems. In addition, plasma chemistries can significantly change as a function of temperature. At higher temperatures, undercutting, resist erosion, and plasma polymerization can be more prevalent. Etch rates and undercutting phenomena appear to have a greater temperature dependence at higher operating pressures.[16] Proper temperature control at the substrate, therefore, plays an important role in RIE processes.

Radiation damage is an important issue in any dry etching process.[30,31] Although high energy electrons and ions impinging on the wafer certainly introduce damage, the deep-UV radiation from the plasma itself also plays a prominent role. A subsequent high-temperature processing step usually anneals out radiation damage in thin oxide films.[31]

Endpoint detection schemes have been developed for RIE processing modes. Laser interferometers have been used to monitor film thickness changes, and emission spectroscopy has been used to monitor concentrations of critical reactant or product species.

Maintaining high vaccuum systems and keeping them clean is an important aspect of dry etching technologies. A successful trilayer process will require low defect densities during definition of the sublayers.

4. Inorganic Resist Systems

Inorganic resists, typified by Ge_xSe_{1-x} (x = 0.10 to 0.33) and As_2S_3, have also been proposed for use in multilayer lithography schemes. Because inorganic resist technology is relatively new, a brief description is included here; for more detailed information the reader is referred to the papers of Yoshikawa,[36–41] Shimizu,[42–47] Tai,[48–55] and Chang,[55–62] as well as the compendium of papers presented at the Electrochemical Society *Symposium on Inorganic Resists*.[63]

These systems employ a thin film, typically 0.2 μm thick, of a chalcogenide glass. The films are formed either by thermal evaporation,[36,48,68] rf sputtering,[36,38] or electron beam evaporation from an appropriate source.[70] These films are strongly absorbing at wavelengths less than the band gap; in the case of $Ge_{0.1}Se_{0.9}$ the band gap is about 1.9 eV (615 nm) and the absorption constant at 500 nm is about[64] 7.50 μm^{-1}. When exposed to band-gap illumination, the films undergo certain physical and optical[43] changes. Of particular interest is the decrease in solubility in alkaline media.[36,65] While these changes have been utilized to record holograms[58,65,71] and relief patterns,[36] the sensitivity is poor, and considerable energy is required to cause an effect.

A dramatic increase in the sensitivity occurs when a source of silver is available on the surface of the glass. This can be supplied as either evaporated, elemental silver,[43,45,47,57,66] or as AgCl[60–62] or Ag_2Se,[37,50,67] the latter two forms being applied by immersion of the glass in an appropriate solution. Subsequent band-gap illumination "photodopes" the silver into the glass. After processing the wafer to remove any silver remaining on the surface (typically by dissolution in either an iodine[50] or an acid[37,38] "fixing" solution), it was found that the unexposed areas can be preferentially etched, compared to the exposed areas, either with aqueous alkali,[37] an organic base,[38,48] or a plasma.[40,57] By this means, modest sensitivity (about 100 mJ/cm^2)[37,40] and high contrast (about 5)[37,40] have been achieved. Lines and spaces of 170 nm were resolved using a holographic printing technique,[48] and shadowing experiments[41] indicate a resolution capability of at least 10 nm. Besides the use of band-gap illumination, these silver sensitized films have also been exposed using x-rays,[62] electrons,[38,67] and ions,[54,68,69]

Patterns developed in GeSe exhibit certain anomalies, all of which are beneficial. Firstly, there is a considerable defocus tolerance of ±2.5 μm for gratings of 0.6 μm lines and spaces,[72] a much larger value than is normally found for polymeric resists. Secondly, the variation of linewidth with exposure is small; a 14% exposure variation reportedly resulted in only a 20 nm variation in the width of

0.75 μm lines and spaces.[52] Thirdly, the times required for fixing and for wet development can vary by ± 10%.[72] Finally, there is an anomalous edge sharpening effect[52] as well as a photobleaching effect.[73] These last effects allow for the simultaneous printing, without bias, of features ranging in size from 0.5 to 5 μm, including both 0.5 μm isolated lines and spaces. A lens system would not ordinarily be capable of such performance.

In 1979 Tai et al,[49] realizing that Ag_2Se/GeSe resists are capable of high resolution, that GeSe is oxygen plasma resistant, and that the GeSe is highly absorbing of light with wavelengths below its band gap, proposed the use of this resist in a two-layer scheme in order to overcome the difficulties associated with standing-wave effects and step coverage. To demonstrate their scheme, these workers used a partially processed 16K MOS RAM wafer; steps on this wafer were as high as 1 μm. The wafer was first coated with 2.5 μm of hard baked HPR 206 resist as a planarizing layer, on top of which was deposited a 200-nm-thick film of GeSe. Because the image-forming top layer is thin, it can record a high resolution pattern; because it is highly absorbing, little light reaches the substrate and is reflected from it. This means that exposure variations due to standing waves are very much reduced without the need to incorporate a dye in the planarizing layer. In Tai's experiment the resist was exposed using either contact or projection printing. After removing the unexposed GeSe with aqueous alkali (the development step), the GeSe remaining served as a conformable mask for oxygen reactive ion etching of the underlying organic layer. Steep-walled profiles, with uniform line widths over steps, were obtained for spaces as narrow as 0.8 μm. Similarly, contact printing was used to demonstrate the absence of standing-wave effects on a highly reflecting aluminum substrate. The GeSe was found to be pin-hole free, as evidenced by the complete lack of any pin holes in the HPR layer. This system employs both a wet chemical step for the development of the GeSe and a dry step for etching the bottom layer. An all-dry process, in which, for example, CF_4 is used to develop the GeSe, is also possible.

Tai also demonstrated a bilayer scheme wherein the bottom layer, instead of being passive is photosensitive.[55] After a pattern has been delineated in the top layer (Ag_2Se/GeSe), that layer serves as a "portable conformable mask" through which the photosensitive resist is exposed. This is possible because the GeSe is opaque to the actinic radiation used to expose the photoactive layer. Using AZ 2400 as the bottom layer, 1 μm lines and spaces were produced with good fidelity. The system demonstrated was "all wet", in that both the development of the top layer and the pattern transfer to the

bottom layer were done with wet chemistry. These multilevel inorganic resist schemes are also discussed in Refs. [74] and [75].

5. Concluding Remarks

We have reviewed various multi-layer resist processes that are currently being applied to VLSI lithography. The two-layer process has the advantage of simplicity and ease of application and will be widely used as lithography with single resist layers becomes unreliable. Only currently used imaging and processing techniques are required, except for the simple far-UV flood exposure step. Good edge profiles can be obtained. On the other hand, the range of possible materials is limited by interaction of top and bottom layers. The most commonly used bottom layer material, PMMA, has poor dry-etch resistance. There are also complications due to the reflections off the substrate, which will increase in significance as the critical dimensions become smaller.

The trilayer processing scheme provides increased flexibility in selecting the sublayer and the patterned resist layer. It is compatible with most of the major potential lithographic imaging tools. The trilayer approach is not without its uncertainties. Three layers have to be defined and dimensional losses will be associated with each layer. For fine-line lithography, these losses must be minimized. Hardmask deposition conditions cannot use temperatures exceeding the thermal stability of the sublayer. Relatively thin (<0.5-μm thick) pinhole-free hardmask films must be obtained at low deposition temperature (usually less than 200° C). Dry development procedures for the hardmask and sublayer need to be well characterized and controlled. Low defect densities are required for the dry etching procedures.

The trilayer approach requires relatively new and more sophisticated processing procedures. These issues are especially significant for high volume fabrication. However, at the resolution levels and packing densities proposed for VLSI designs, the quality and versatility of the multilayer resist technology will play a crucial, if not decisive role.

The inorganic resist offers a different approach to improved lithographic quality. The Ge-Se/Ag system is capable of higher resolution because of the edge sharpening effect. It has good plasma etch resistance. In addition, the high optical absorption eliminates any reflection problems.

The formation and sensitization of the inorganic resist layers is not compatible with currently used processes, however, so that new techniques will have to be introduced. The opaque nature of the layer makes the alignment procedures more difficult. Thus, we can

expect that this technique will mainly be applied when the need for very high resolution or very steep edge profiles arises.

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Reactive Sputter Etching of Dielectrics

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Abstract—A highly selective and anisotropic dry-etch process has been developed for generating contact openings in various dielectrics. Etching is performed in a $CHF_3 + H_2$ gas mixture in a parallel-plate reactor using aluminum electrodes and operated in the RSE (reactive sputter etch) mode. The selectivity of the etch process is determined by the concentration of H_2 used in the plasma. The process is applicable to batch processing requiring high selectivity and can be used in cases requiring overetching without attacking the silicon substrate in the contact openings or the photoresist used for pattern definition.

1. Introduction

Anisotropic etching in rf-generated plasmas is widely used for selectively defining contact openings with vertical walls in dielectrics during the fabrication of VLSI devices. Vertical-wall profiles are usually produced by reactive sputter etching (RSE) in order to maintain pattern dimensions in high-density circuits. There are numerous publications on the etch characteristics of silicon dioxide and other dielectrics in fluorocarbons and other gases.[1–7] In some cases, hydrogen is added to the fluorocarbon gas to increase the selectivity of dielectric etching relative to silicon or photoresist;[1,2] in other cases, hydrogen may be present as an element in the fluorocarbon.[1,3] In this paper we describe a highly selective etch process using a CHF_3/H_2 gas mixture for the anisotropic etching of contact openings and vias in various dielectrics.

2. Experimental

The etching apparatus used is a dual-system parallel-plate reactor.[8] Both electrodes can be powered independently or simultaneously

through matching networks by separate power supplies. Power regulation is accomplished by control of incident power or by control of the potential (-dc bias) developed on the powered electrode during etching. Regulation by the latter method is employed in our experiments and etching is performed in the RSE mode. The rf frequency is 13.56 MHz. The aluminum electrodes are approximately 22 inches in diameter and are separated by about 2 inches. The lower electrode is temperature-controlled by a heat exchanger, and the upper electrode is water cooled. The gas flow is radial toward a central part in the lower electrode, and flow rates are regulated and monitored by mass flow controllers and mass flowmeters. The system can be evacuated (through a servo-controlled throttle valve) by a Roots blower and mechanical pump for pump-down or for operating in the plasma etch mode. The system is pumped through a gate valve and an adjustable iris by a diffusion pump and fore pump for operation in the RSE mode. In the experiments described here, the upper electrode and chamber walls were grounded during etching.

Two gas mixtures, CF_4/H_2 and CHF_3/H_2 were evaluated with respect to their etch characteristics. Among the materials studied were positive and negative photoresists, SiO_2, BPSG,[9] PSG, Si_3N_4, polysilicon, and single-crystal silicon. Etch rates were obtained for each species to determine process selectivity. Special emphasis was placed on obtaining high selectivities when using positive photoresist (HPR 204).

3. Results and Discussion

3.1 Etch Rates and Selectivity

Etch rates for positive photoresist (HPR 204), BPSG, thermal SiO_2 polycrystalline silicon, and single crystal silicon are shown in Fig. 1 for the case of etching in the CF_4/H_2 mixture. Etch rates are given as a function of the $H_2/(CF_4 + H_2)$ flow-rate ratio expressed as a percentage. The CF_4 flow rate was held constant at 20 cc/min and the H_2 flow rate was varied. The pressure in the system was 20 mTorr and the voltage on the electrode supporting the samples was -700 V. Corresponding etch rates in a CHF_3/H_2 mixture are shown in Fig. 2 which also includes etch rates for Si_3N_4. In this case the CHF_3 flow rate was held constant at 19 cc/min and the H_2 flow rate was varied. The pressure in the system was 15 mTorr and the electrode voltage was -700 V.

The data presented in Fig. 1 reveal relatively high etch rates for positive photoresist (HPR 204) and little or no selectivity for the etching of oxides relative to silicon under the conditions of the ex-

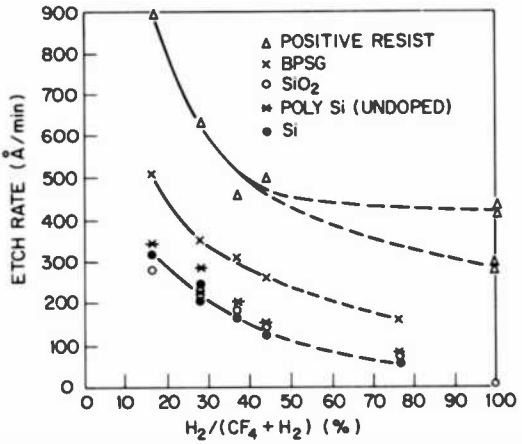


Fig. 1—Etch rate in CF_4 + H_2 as a function of H_2 flow rate ratio, P = 20 mTorr, CF_4 flow rate = 20 cc/min, bias voltage = −700 V.

periments. While improved performance could be expected under optimized conditions, it was decided at an early stage in these experiments that the CHF_3/H_2 system, based on the data in Fig. 2, offered a greater possibility of obtaining high selectivities in the etching of dielectrics relative to silicon and positive photoresist. A summary of etch rates in both gas mixtures is given in Table 1. Both positive and negative photoresists (HPR 204 and HNR 120)

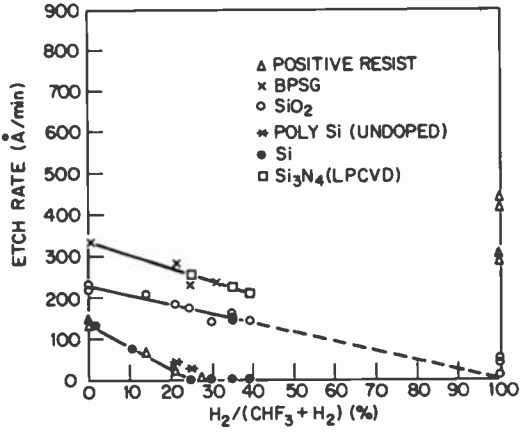


Fig. 2—Etch rate in CHF_3 + H_2 as a function of H_2 flow rate ratio, P = 15 mTorr, CHF_3 flow rate = 19 cc/min, bias voltage = −700 V.

Table 1—Etch Rates for Various Materials in CF_4/H_2 and CHF_3/H_2 Gas Mixtures

Etch Parameters	Etch Rates (Å/min)					
	HPR 204	HNR 120	BPSG	SiO_2	Polysilicon	Silicon
CF_4/H_2 7/23 (cc/min) −700 V, 24 mTorr	700	~0	165	80	80	60
CF_4/H_2 7/23 (cc/min) −960 V, 24 mTorr	1360	~10	240	135	135	85
CF_4/H_2 7/23 (cc/min) −960 V, 12 mTorr	1260	~5	205	120	70	60
CHF_3/H_2 19/6 (cc/min) −700 V, 15 mTorr	~5	~0	260	175	25	~0
CHF_3/H_2 19/6 (cc/min) −910 V, 15 mTorr	~20	10	360	250	60	~5

are etched slowly in the CHF_3/H_2 mixture, while positive photoresist is etched quite rapidly in the CF_4/H_2 mixture under conditions which give low etch rates for the case of the negative photoresist. The negative resist, HNR 120, was etched at comparably low rates in both mixtures. Large differences in the etch rates of photoresists in neat CF_4 and neat CHF_3 have been reported previously and better selectivities were obtained in general in CHF_3.[3]

Selectivity associated with the CHF_3/H_2 system is much improved over that of the CF_4/H_2 system. At a hydrogen concentration corresponding to about 25% of total flow rate, the etch rates for positive resist (HPR 204) and single-crystal silicon become zero while thermal SiO_2, BPSG, and Si_3N_4 are still being etched. Thus, very high selectivities can be obtained at this H_2 concentration. Polycrystalline silicon etches at a somewhat faster rate than single-crystal silicon and the etch rate goes to zero at slightly higher hydrogen concentrations. At a hydrogen flow-rate ratio of 25% and higher (see Fig. 2), polymer forms on the biased electrode surface and on the surfaces of any materials not being etched (such as silicon and photoresist). However, the oxide and nitride dielectrics continue to be etched. Below a hydrogen flow-rate ratio of 25% no detectable polymer is formed on the biased surfaces. This does not preclude, however, the formation of very thin carbonaceous deposits on exposed silicon and other surfaces.[5,6,10,11] The greatest selectivity is obtained at the polymer formation point. Similar results have been reported for the CF_4/H_2 system.[4] For practical purposes it is preferable to work at lower H_2 concentrations than the polymer formation point. The operating point has been selected between 19% and 24% H_2 depending upon the selectivity required. Many device test lots have been successfully etched in this regime. In applications where selectivity is not so important, H_2 may be eliminated or used at some intermediate flow-rate ratio. It should be noted that the H_2/CHF_3 ratio in the plasma is lower than that introduced into the reaction chamber because of the differential pumping rates for H_2 and CHF_3.[12] The flow rates used in these experiments gave uniformity of dielectric etching of about 5% across the substrate electrode.

One limitation of the CHF_3/H_2 system is the relatively low etch rates of dielectric layers. The following results summarize the influence of various parameters on etch rates. Figs. 3 and 4 show the influence of electrode voltage on the various etch rates for two H_2 flow rates, 5 cc/min and 6 cc/min, respectively. The etch rates for SiO_2 and BPSG increase quite quickly with voltage, while the etch rates for single-crystal silicon, positive photoresist, and polycrystalline silicon increase more slowly. The increase of 1 cc/min in H_2

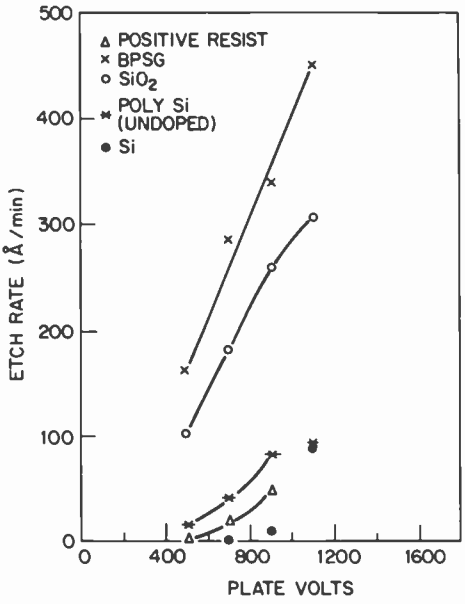


Fig. 3—Etch rate as a function of plate voltage in CHF_3 + H_2 (19 cc/min + 5 cc/min), P = 15 mTorr.

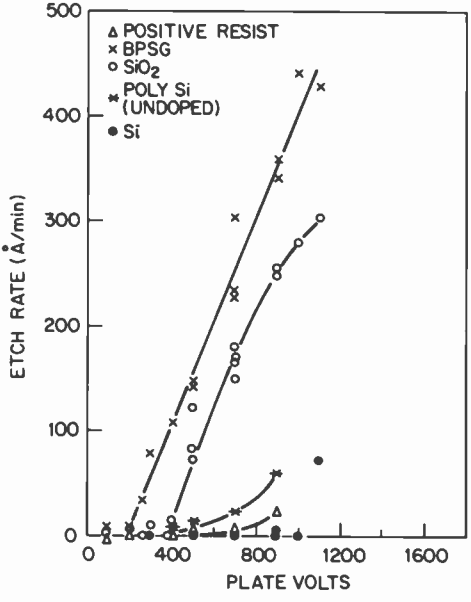


Fig. 4—Etch rate as a function of plate voltage in CHF_3 + H_2 (19 cc/min + 6 cc/min), P = 15 mTorr.

flow rate has little effect on the etch rates of the dielectrics but lowers the etch rates of the other materials, thus improving selectivity. Increasing the magnitude of the electrode voltage decreases the selectivity for a given hydrogen concentration. It should be noted that the electrode voltage is negative. For convenience only the magnitude of the voltage is plotted in Figs. 3 and 4.

In the next set of experiments, the H_2 concentration was varied, at a constant voltage of 1000 V, to improve selectivity. The results are presented in Fig. 5. The etch rates for the dielectrics and polycrystalline silicon decrease linearly with increasing H_2 flow rate until the polymer formation point is reached at about 10 cc/min of H_2. Under these conditions the etch rate for photoresist and single-crystal silicon is zero, and the etch rates for polycrystalline silicon, SiO_2, and BPSG are about 20 Å/min, 225 Å/min, and 330 Å/min, respectively.

The data presented in Fig. 5 indicate that increased etch rates can be obtained, while still retaining high selectivities, by increasing the magnitude of the electrode voltage. However, other problems arise at high voltages. Physical sputtering effects become more pronounced and trenching occurs in the bottoms of contact

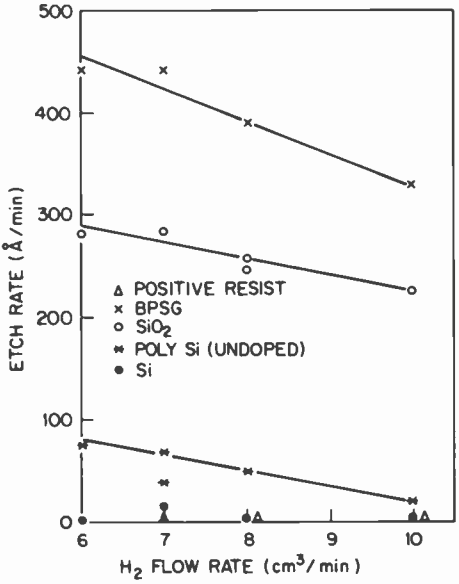


Fig. 5—Etch rate as a function of H_2 flow rate, P = 15 mTorr, CHF_3 flow rate = 19 cc/min, bias voltage = −1000 V.

openings adjacent to the walls of the openings. This effect occurs even under conditions of highly selective etching and is due to the reflection of incoming ions from the walls of the contact openings. Trenching effects are particularly undesirable in the case of shallow diffusions in bulk silicon. There is also a risk of sputtering material at high voltages into the contact openings, and vias formed in this way are usually not as clean as those formed at lower voltages. In this work, an electrode potential of -700 V was chosen by compromise for the etching of device test structures using BPSG as the reflow glass and HPR 204 as the photoresist.

3.2. Polymer Formation

As previously indicated, polymer formation occurs on biased surfaces that are not being etched when the hydrogen concentration is increased above the polymer formation point. These surfaces include the biased electrode, exposed silicon, and photoresist. No accumulation of polymer occurs on the dielectrics, which continue to be etched, and no accumulation of polymer occurs on biased surfaces at hydrogen concentrations below the polymer formation point.

Polymer formation can occur on all grounded surfaces at hydrogen concentration below the polymer formation point when either the CF_4/H_2 or CHF_3/H_2 mixtures are used.[12,13] The H_2 flow rate at which this happens depends on several factors including reactor geometry, power density, and pressure. The rate of polymer formation increases with H_2 concentration. In the experiments described here, polymer was formed on all grounded surfaces during etching but not on biased surfaces because etching was performed at hydrogen concentrations below the polymer formation point. The apparatus had to be cleaned periodically in O_2 plasma to remove deposits from grounded surfaces.

Polymer can also be removed in H_2 plasma. Evidence for this can be seen in Figs. 1 and 2. When photoresist was etched in 100% H_2, two different etch rates were obtained depending on the presence or absence of polymer in the system at the time of etching. The etch rate was observed to be slower when polymer was present due to the reaction of H_2 with polymer. Simultaneously, there was a noticeable etch rate for SiO_2 due to the presence of fluorocarbons formed in the etching of polymer by H_2. When the polymer was removed in O_2 plasma, the etch rate of photoresist was increased and the etch rate of SiO_2 decreased to a few angstroms per minute.

The frequency of polymer removal was varied from a clean-up after each run to once per week after running the system on a daily

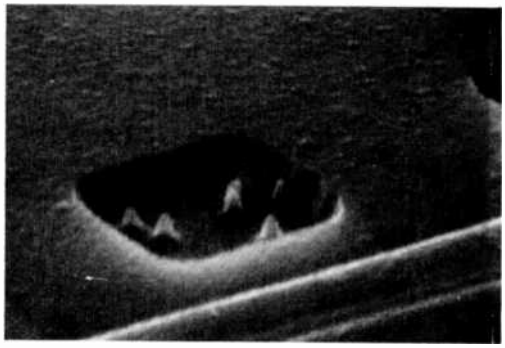
basis under laboratory conditions. Polymer coatings formed slowly and many runs were possible before cleaning was necessary. It was also found that the presence of polymer in the system, especially on the substrate electrode, improves the reproducibility of the process with respect to selectivity, etch rates and cleanliness of contact openings. Consequently, after each cleaning operation, all inner surfaces of the system were coated with a thin layer of polymer prior to further wafer etching. This was done by increasing the hydrogen concentration in the CHF_3/H_2 system above the polymer formation point and depositing about 500 nm of polymer on the substrate electrode. The polymer layer is slowly etched away during subsequent wafer etching and is replenished periodically. Our results indicate that frequent cleaning of the system is not necessary. Various materials such as quartz and teflon have been reported in the literature for covering substrate electrodes in order to avoid contamination due to back scattering of nonvolatile material physically sputtered from metal parts.[3,5,6] Of concern is the ease of removal of polymer once formed. It has been our experience that polymer directly formed by increasing the hydrogen concentration above the polymer formation point is easily removed in oxygen or hydrogen plasma or in procedures used to remove photoresist. Polymers or deposits formed due to back scattering and sputtering effects may end up on the walls of vertical contact openings[14] and are difficult to remove by means compatible with device processing.

3.3 Etching Device Contact Openings

Among the problems encountered in etching contact openings in device structures has been the occurrence of small "pyramids" on the bottoms of the openings, especially on polycrystalline silicon. An example is shown in Fig. 6a for the case of a 4 × 4 μm contact opening. This problem was alleviated by a photoresist "de-scum" process and by coating the aluminum electrode on which the wafers rested with a thin layer of polymer as described previously. In the de-scum process, the device wafers were etched in hydrogen for 2 or 3 min (in situ) prior to dielectric etching. The hydrogen etching was performed in the RSE mode at a pressure of about 15 mTorr and a plate voltage of −700 V. An example of 2 × 3 μm contact openings obtained in this manner for the case of BPSG (~600 nm) over thermal oxide (~100 nm) is shown in Fig. 6b. Many device wafer lots with VLSI pattern dimensions were successfully etched by the above procedure.

The presence of any surface residue from photolithographic pro-

(a)



(b)

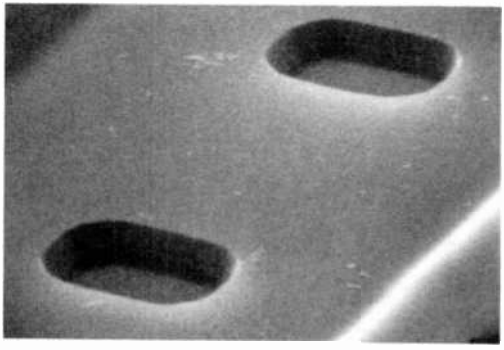


Fig. 6—Etched contact openings showing (a) "pyramids" resulting from residual stains after photolithography and (b) clean contact openings obtained after a preliminary photoresist "de-scum" in hydrogen plasma.

cessing or other sources, such as back scattering or sputtering, can have a pronounced masking effect when etching is performed under conditions of high selectivity. At higher pressures (50–100 mTorr), microvilli were occasionally observed in SEM micrographs of etched contact openings. This probably arose from sputtered material, which acted to mask the dielectric from being etched uniformly. At the lower pressures (~15 mTorr) normally used for dielectric RSE etching, this phenomenon was not observed.

4. Conclusions

Major differences were observed between the CF_4/H_2 and CHF_3/H_2 systems with respect to the selective etchings of dielectrics relative

to positive photoresist (HPR 204) and silicon. Much higher selectivities were obtained with the latter system, which was subsequently used for pattern transfer in the fabrication of devices with VLSI dimensions. This etching process is applicable to batch processing requiring high selectivity and can be used in cases requiring overetching without appreciable attack of silicon or photoresist. This is important in the case of shallow diffusions whenever it is necessary to over-etch because of such factors as nonuniformity in the thickness of the reflow dielectric, thicker thermal oxide on N^+ polysilicon than on bulk silicon, and nonuniformity in etch rate across a given wafer or from wafer to wafer.

The selectivity of the CHF_3/H_2 etch process is determined by the concentration of H_2 used in the plasma. The highest selectivity occurs at a hydrogen concentration corresponding to the polymer formation point. Below this concentration, no accumulation of polymer is formed on biased surfaces during reactive sputter etching. Polymer is formed, however, on grounded surfaces. Etching is performed at preselected hydrogen concentrations below the polymer formation point depending on the selectivity required.

Acknowledgments

We greatly appreciate technical discussions with H. Lehman and R. Widmer of Laboratories RCA, Ltd., Zurich. Their previous experience in the dry etching of fine grid patterns in SiO_2 using CHF_3 was very helpful at the outset of this program. R. Widmer also provided technical assistance at Princeton in our early experiments. We also wish to thank J. Vossen for providing the plasma etch equipment and for collaboration in carrying out various equipment modifications necessary for reactive sputter etching. We are indebted to O. Mesker for his skills in helping to keep the equipment operational.

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Patents Issued to RCA Inventors—Fourth Quarter 1982

October

S. P. Barlett, D. J. Dougherty and F. P. Lokuta Method of Forming a Mesa in a Semiconductor Device With Subsequent Separation into Individual Devices (4,355,457)
S. Berkman, M. T. Duffy and H. E. Temple Silicon Melting Crucible (4,356,152)
D. F. Bowman Circuit for Frequency Scan Antenna Element (4,356,462)
G. N. Butterwick Photomultiplier Tube Having a Stress Isolation Cage Assembly (4,355,258)
A. R. Dholakia and C. J. Bulocchi Apparatus for Sharpening a Cutting Stylus (4,355,382)
A. G. Dingwall Voltage Divider Circuits (4,354,151)
J. Durbin, Jr. and D. H. Pritchard Impulse Noise Reduction System for TV Receivers (4,353,093)
M. T. Gale and J. Kane Recording Blank and Method for Fabricating Therefrom Diffractive Subtractive Filter Metal Embossing Master (4,353,622)
E. R. Ganssle Spacecraft Separation Apparatus (4,355,775)
J. B. George and W. J. Testin Tuning Mode Arrangement Useful for Restricting Channel Selection to Certain Channels (4,355,415)
K. W. Hang and W. M. Anderson Partially Devitrified Porcelain Containing BAO.2MGO.2SIO2 and 2MGO.B203 Crystalline Phases Obtained From Alkali Metal Free Divalent Metal Oxide Borosilicate Glass (4,355,114)
K. W. Hang and W. M. Anderson Borosilicate Glass Frit With MGO and BAO (4,355,115)
W. E. Harlan Television Receiver On-Screen Alphanumeric Display (4,354,202)
F. Z. Hawrylo and G. H. Olsen Semiconductor Laser Diode and Method of Making the Same (4,355,396)
M. V. Hoover Field Effect Transistor Amplifier With Variable Gain Control (4,353,036)
M. V. Hoover Bridge Amplifiers Employing Complementary Field-Effect Transistors (4,355,287)
S. T. Hsu Method of Forming Self-Aligned Contact in Semiconductor Devices (4,353,159)
G. Kaganowicz and J. W. Robinson Method of Preparing an Abrasive Coated Substrate (4,355,052)
L. A. Kaplan Power Protection Circuit for Transistors (4,355,341)
L. B. Kimbrough and L. P. Wilbur, Jr. System for Applying and Tensioning an Implosion Protecting Band to a CRT With a Tension Between Selected Limits (4,352,226)
G. W. Looney Apparatus for Oscillating a Gas Manifold in a Rotary Disc Reactor (4,354,455)
N. O. Ny Musical Keyboard for Home Computer (4,352,313)
R. Ott Circuit and Method for Duty Cycle Control (4,355,283)
T. R. Pampalone and K. B. Killchowski Positive Radiation Sensitive Resist Terpolymers (4,355,094)
G. A. Reitmeier Sampled or Digitized Color in a High Speed Search Record and Replay System (4,355,324)
W. R. Roach Missing Order Defect Detection Apparatus (4,352,564)
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H. E. Schade CRT With Means for Suppressing Arcing Therein (4,353,006)
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R. G. Stewart Random Access Memory With Volatile and Non-Volatile Storage (4,354,255)
C. C. Wang and R. F. Bates Bis(Hydroxyalkyl) Disiloxanes and Lubricant Compositions Thereof (4,355,062)
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November

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T. V. Bolger Video Disc Vari-Speed Playback System (4,361,849)
W. C. Brooks Method for Electroforming a Replica on a Record Matrix (4,357,216)
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S. D. Burrowes Legibility for Alpha-Mosaic Characters (4,358,788)
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D. D. Mawhinney Wideband Microwave Frequency Divider (4,357,580)
P. E. O'Connell Video Disc Player Having Click Mechanism (4,361,884)
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G. H. Riddle Active Distortion Elimination Circuitry for a Video Disc Player (4,360,829)
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O. H. Schade, Jr. Transistor Amplifiers Exhibiting Low Input Offset Potentials (4,360,785)
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December

H. W. Becke and C. F. Wheatley, Jr. Power Mosfet With an Anode Region (4,364,073)
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W. A. Lagoni Horizontal and Vertical Image Detail Processing of a Color Television Signal (4,365,266)
N. R. Landry High Power Coaxial Power Divider (4,365,215)
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L. F. Wallace Method of Making Buried Channel Charge Coupled Device with Means for Controlling Excess Charge (4,362,575)
C. M. Wine Video Disc With Dynamic Stylus Cleaning (4,363,117)

AUTHORS

Heinrich Auderset graduated in mechanics in 1964. From 1964 to 1967 he worked at the Physical Meteorological Observatory in Davos, Switzerland on problems of global solar radiation standards. In 1967 he joined Laboratories RCA Ltd., Zurich. He was involved in work on Raman scattering of magnetic semiconductors, ferroelectrics and low dimensional materials like inorganic and organic conductors, and in the development of an optical scanner for dust and defect detection on semiconductor materials. At present he works on materials characterization of Polysilicon, VideoDisc and Optical Storage Materials by means of elastic, Raman scattering and optical scanner. In 1979 Mr. Auderset received an RCA Outstanding Achievement Award for his contribution to the development of the laser scanner.

Dan Botez received the BS degree (with highest honors) and the MS and PhD degrees in Electrical Engineering from the University of California, Berkeley, in 1971, 1972, and 1976, respectively. His doctoral studies were concerned with the characteristics of layers deposited over preferentially etched channels in GaAs, as well as with novel optical devices made possible by this method. For one year following graduation, he was a Postdoctoral Fellow at the IBM Watson Research Center. In 1977 Dr. Botez joined the Technical Staff at RCA Laboratories, Princeton, NJ, where his work resulted in "thick-window" high-radiance surface-emitting LEDs and in the development of a novel type of single-mode-stabilized cw diode laser: the constricted double-heterostructure (CDH) laser. The CDH laser has demonstrated cw and pulsed operation up to the highest ambient temperatures ever reported and represents the least temperature sensitive diode laser commercially available. His recent work has resulted in the constricted double-heterojunction large-optical-cavity (CDH-LOC) laser, which to date is the most powerful single-mode semiconductor cw laser and has made possible the optical recording of information at the highest data rates ever achieved.

In 1979 he received an RCA Laboratories Outstanding Achievement Award for contributions to the development of a high-density optical recording system employing an injection laser. In 1982 he was appointed a Research Leader in the Opto-Electronics group. Dr. Botez holds four patents and is a member of Phi Beta Kappa and the IEEE.

John C. Connolly received an AS degree in Mechanical Engineering Technology from Middlesex County College in 1973, a BS degree in Mechanical Engineering from Rutgers University in 1977, and is working toward an MS degree in Materials Science at Polytechnic Institute of New York. Mr. Connolly joined RCA Laboratories, Princeton, NJ, in 1979 as a Senior Technical Associate and was involved in the growth of multiple-layer heterojunction structures for the development of the constricted double-heterojunction (CDH) laser, a novel low-power single-mode-stabilized cw diode laser. More recently, he contributed to the development of a new type of high-power single-mode-stabilized cw diode laser: the terraced-heterojunction large-optical-cavity (TH-LOC) laser. In 1982, he was promoted to Associate Member of the Technical Staff. He is involved in the development of high-power constricted double-heterojunction large-optical-cavity (CDH-LOC) lasers for optical-disc recording and long-distance high-data-rate fiber optical communication.

Mr. Connolly is a member of IEEE, the American Vacuum Society, and the American Society of Mechanical Engineers.

John F. Corboy is an Associate Member of Technical Staff at RCA's David Sarnoff Research Center, Princeton, NJ and is a member of the Materials Synthesis Group within the Materials and Processing Research Laboratory. He joined RCA in 1959 working on the epitaxial growth of III-V compounds and the synthesis and crystal growth of organic compounds. From 1965 to 1980, he studied the properties of silicon on insulating substrates and was involved in the transfer of silicon-on-sapphire technology between RCA Laboratories and other divisions of RCA. Currently, he is involved in silicon homoepitaxy and in plasma etching of oxide films.

Mr. Corboy has been issued two U.S. patents and was the recipient of an individual RCA Laboratories Achievement Award in 1974.

Michael T. Duffy received the B.Sc. degree in chemistry from University College, Dublin, in 1958 and completed his Ph.D. studies in solid state chemistry in 1963. He was a teaching assistant at this University from 1961 to 1963. In 1964 he joined the University of Toronto as Research Associate and worked in molecular beam research until July 1966 when he joined the staff of RCA Laboratories. Since then he has been engaged in materials research in the field of integrated electronics. He has worked on the synthesis and characterization of various dielectrics in MIS structures and on the vapor phase growth of heteroepitaxial materials on insulating substrates, particularly sapphire. His work also included evaluation of CVD materials for contact

with molten silicon. More recent work involved analysis of the surface perfection of polished sapphire substrates and heteroepitaxial silicon films by IR and UV reflectance methods. He is currently involved in the development of processes for the reactive ion etching of dielectric films for VLSI processing and the characterization of amorphous and polycrystalline silicon films for VLSI application.

Dr. Duffy has been the recipient of three RCA Laboratories Achievement Awards for research contributions. He is a member of the Electrochemical Society.

Robert V. D'Aiello received a BS degree in Electrical Engineering, cum laude, and an MSEE degree from the Polytechnic Institute of Brooklyn in 1960 and 1961, respectively. He then served two years in the U.S. Army Corps of Engineers. In 1962 he joined RCA Laboratories, where he has done research on bulk Hall-effect devices at microwave frequencies, dielectric cavities, superconducting thin-film microwave devices, and silicon high-power avalanche-diode oscillators and amplifiers. In 1969 he received his PhD degree in Electrophysics from the Polytechnic Institute of Brooklyn. For the past several years, Dr. D'Aiello has done research and development in the area of silicon device processing and diagnostic measurement, with emphasis on high-power silicon devices including high-current Schottky-barrier rectifiers, high-voltage epitaxial switching transistors, and solar cells. He received an RCA Outstanding Achievement Award in 1973 for improvements in the processing of silicon power devices. His most recent work includes experimental studies of solar-cell fabrication techniques, including the fabrication of epitaxial structures on single-crystal and low-cost silicon substrates, as well as the optimization of standard technologies.

Dr. D'Aiello is on the adjunct staff at Middlesex County College and is a member of Eta Kappa Nu, Tau Beta Pi, Sigma Xi, and IEEE.

Norman Goldsmith received his BA degree, with honors, in Chemistry from Hunter College in 1959, and his MS degree in Physical Chemistry from Stevens Institute of Technology in 1964. He joined RCA in 1959, working at the Solid State Division, Somerville, NJ, on materials and process technology for silicon and gallium arsenide. His work in this capacity included the epitaxial growth of both gallium arsenide and silicon, materials purification, diffusion, vapor deposition, surface stabilization of semiconductor surfaces, clean oxide growth, and the development of nondestructive measurement techniques. In the course of this work he developed several important process techniques for silicon semiconductor devices. Among the more important

of these were the development of the BN diffusion system, which made possible the fabrication of CMOS circuits on bulk material, and the original work on depositing silica films from mixtures of silane and oxygen at temperatures below 400°C. In 1967 he joined Laser Diode Laboratories in Metuchen, New Jersey, and was appointed Executive Vice President of the firm in 1970. He returned to RCA Laboratories, Princeton, New Jersey, in 1971 to work on epitaxial-growth methods for silicon power devices. As part of this work he made important contributions to methods of data collection and the analysis of spreading resistance measurements. He also helped develop a novel infrared microscope for use in examining the inner structure of silicon and gallium arsenide.

In 1974 he assumed the position of Head, Lithography and Integrated Circuit Processing. His responsibility is the development of new processes for silicon and silicon-on-sapphire circuitry, nonvolatile memory devices, advanced techniques for process analysis and process control, and advanced projects in patterning and photolithography. His group has developed fabrication techniques for 0.3-μm gate-length CMOS/SOS transistors. Yield-predictive test activities of this group now include dry-etch process development, advanced lithography for both CMOS/SOS and CCD imagers, and manufacturing-yield improvement studies. His own work has been concerned with the application of computers to process control and the mathematical modeling of manufacturing yield. He has also managed a number of government contracts relating to all aspects of semiconductor manufacturing technology.

Mr. Goldsmith is a member of the American Chemical Society, the American Association for the Advancement of Science, and the Electrochemical Society and has three issued patents. He has given courses both at RCA Laboratories and at independent academic institutions on the application of non-destructive optical techniques to semiconductor process control. He was the recipient of an RCA Laboratories Achievement Award for his contributions to a group effort for improving the processing of power devices.

Günther Harbeke received the Physics Diploma in 1955 and the Ph.D. in Physics in 1958 from the Technical University in Brunswick, Germany. In 1961 he joined the staff of Laboratories RCA Ltd., Zurich. Prior to that he was with the Physikalisch-Technische Bundesanstalt in Brunswick. In 1963, he worked 9 months at the RCA Laboratories in Princeton. Dr. Harbeke has been working in research on the basic optical properties of semiconducting and insulating materials and on light scattering and phase transitions in solids. He received two RCA Laboratories Achievement Awards for team performance in 1962 and in 1969. Dr. Harbeke has a lecturing assignment at the University of Cologne and is a member of the Zurich, Swiss, German, and European Physical Societies.

Robert C. Hesser received his Associate degree in electrical engineering from Trenton Technical Institute in 1965. From 1965 to 1972 he worked at the Princeton University Accelerator Lab specializing in the 3 MEV Van De Graaff injection system. He joined RCA Laboratories in 1972, working on processing and testing of samples for the ion implantation system. Currently he works on ion implantation and laser annealing projects at the labs.

Michael Kaplan received a BS degree (Chemistry) from Rensselaer Polytechnic Institute in 1959. He earned MA and PhD degrees at Columbia University in 1961 and 1965, respectively. His field of study was electron-spin resonance of free radicals in solution. Since joining RCA Laboratories, Princeton, NJ, as a Member of the Technical Staff in 1965, Dr. Kaplan has been involved in studying materials for micro-recording/fabrication, working initially with lasers and later with electron beams. In the area of high-density, electron-beam recording, Dr. Kaplan modeled exposure profiles incident on resist surfaces as functions of the beam shape and spatial frequency being recorded. Later, this work was extended to square-wave-modulated optical exposures. Dr. Kaplan was also instrumental in developing a number of unique polymeric resists and holds several key patents in this area, including the very important basic patent on poly(olefin sulfones). Dr. Kaplan has extensively studied the developability of diazoquinone-sensitized resists as a function of exposure, and has related this to the amount of sensitizer destruction accompanying the exposure. More recently, he has designed and built two low-power x-ray lithographic systems to demonstrate the problems inherent in x-ray lithography and to investigate various experimental resists. He also studied the optimization of x-ray lithographic exposure tools, with special emphasis on the throughput of such systems using either whole-wafer or step-and-repeat exposure schemes.

Dr. Kaplan is a member of the American Chemical Society and Sigma Xi and a Fellow of the American Institute of Chemists. He holds seven U.S. patents.

Frank Kolondra graduated in 1963 from New Jersey Institute of Technology with a BS degree in Electrical Engineering. He started to work for RCA, Harrison, NJ, where he was responsible for all testing in the Transistor Development Shop. He spent several years maintaining testing equipment in the Quality Control Department and the Chemistry and Physics Laboratory working on Nuvistor electron tubes and thermoelectric materials. After joining RCA Laboratories, Princeton, NJ, he built a 100-kilogauss Nb_3Sn super-

conducting magnet. Later he was active in the development of radiation-hard devices and was operating the 1-million-volt Van de Graaff accelerator. He is now responsible for the ion-implantation facility.

Henry Kressel received a BA degree from Yeshiva College in 1955 (magna cum laude), an MS degree in Applied Physics from Harvard University in 1956, and an MBA in 1959 from the Wharton School of the University of Pennsylvania. He was awarded his PhD degree in Metallurgy and Materials Science in 1965 by the University of Pennsylvania and has attended the Technical Management Course at the Harvard Business School. He joined the RCA Semiconductor Division in 1959. He was initially engaged in the development of high-frequency silicon transistors and was instrumental in the development of many processes used in the manufacture of planar transistors. In 1961 he became head of a group responsible for research and development of silicon and GaAs microwave diodes, which contributed important advances in the field of high-power, high-frequency varactor diodes. In 1963, Dr. Kressel was corecipient of an RCA Semiconductor Division Achievement Award for contributions to this field. He was awarded an RCA David Sarnoff Fellowship for 1963-65 to pursue his doctoral studies. On his return to RCA in 1965, he became Head of the Device Physics Group in the Technical Program Laboratory and engaged in the investigation of avalanche and stress effects and optical properties of p-n Si and GaAs junctions.

In 1966, Dr. Kressel joined the Technical Staff of RCA Laboratories. He was corecipient of an RCA Laboratories Achievement Award (1967) for contributions leading to the first high-power, high-efficiency "anomalous mode" Si avalanche microwave oscillator. In 1968, he shared another Achievement Award with H. Nelson for the development of the first practical heterojunction injection laser. Dr. Kressel became Head, Optical Devices Research, in 1969 and Head, Semiconductor Device Research, in 1971. His activities included research and development of optoelectronic (semiconductor lasers, LEDs, and solar cells) and power silicon devices. In 1977, he was appointed Director of the Materials and Processing Research Laboratory at the David Sarnoff Research Center. The research in this laboratory includes work in the areas of III-V materials and optoelectronics devices, advanced power transistors and thyristors, polymers and photoresists, and growth of various magnetic, semiconductor, and insulator materials. In March 1979, Dr. Kressel assumed the duties of Staff Vice President responsible for Solid State Research. He is responsible for research and development of integrated circuits, discrete power transistors and optoelectronic devices.

Dr. Kressel has 32 issued U.S. patents and is a Fellow of the IEEE and the American Physical Society. He is Associate Editor of the *IEEE Journal of Quantum Electronics* and Chairman of the IEEE/OSA Steering Committee for the *Journal of Lightwave Technology*. He is a past President of the IEEE Quantum Electronics and Applications Society and was elected to the National Academy of Engineering in 1980.

Ivan Ladany received the BS and MS degrees from Northwestern University. In 1953, he joined the Naval Research Laboratory in Washington, DC, where he worked primarily in semiconductor device research. Among his accomplishments were several studies of dc and ac properties of semiconductor diodes and an analysis of inductive effects in pn-junction devices. He joined RCA Laboratories, Princeton, NJ, in 1966 as a Member of the Technical Staff and has worked since then on GaP, GaAP, InGaAsP, and GaAs electroluminescence. For his work on GaP electroluminescence, which resulted in significant improvements in these devices, Mr. Ladany received an RCA Laboratories Outstanding Achievement Award in 1969. His studies of GaAs:Si electroluminescent diodes demonstrated the achievement of very high efficiencies and a large tuning range for these devices. Mr. Ladany then concentrated his efforts in the area of injection lasers and was instrumental in developing RCA's first commercial GaAs lasers capable of cw operation. His current interests include the development of buried-heterostructure lasers in the InGaAsP system at 1.3-1.6 μm, as well as studies of ohmic contacts and methods for improving laser-to-fiber coupling. In 1980, Mr. Ladany shared in an RCA Laboratories Outstanding Achievement Award for his work on InGaAsP lasers.

Mr. Ladany holds more than 15 patents and is a member of the American Physical Society, the IEEE, and Sigma Xi.

Donald P. Marinelli is a graduate of RCA Institutes and has completed several courses in mathematics and chemistry at Mercer Country College. He joined RCA Laboratories in March 1960 and transferred to the Research Services Group in 1962. There he worked in various stages of tube technology and metallurgy. In 1964, he transferred to the Semiconductor Device Research Group, where he has worked on the development of a large number of different III-V compound electroluminescent devices. Mr. Marinelli is experienced in all practical aspects of III-V device technology, including crystal growth, photolithography, and metallization, including electron beam evaporation. He played a major role in developing the sophisticated processing sequence for the fabrication of RCA's long-lived cw AlGaAs laser diodes. He has also made many contributions to the design and assembly of various apparatus for liquid-phase-epitaxy growth systems.

Mr. Marinelli holds eight U.S. patents.

Ernst Meier graduated in fine mechanics in 1949. From 1949 to 1962 he worked with the Trueb and Taeuber Company on the development of electromechanical instrumentation. In 1962 he joined Laboratories RCA Ltd., Zurich. He was involved in optical measurements on semiconductors and insulators in the vacuum ultraviolet, ultraviolet, visible, and infrared region of the spectrum and in the development of optical instrumentation for in-process control in the IC technology. In 1968 he was promoted to TSA. At present he is working on the characterization of various materials for IC technology and of conducting polymers and VideoDisc material.

Dietrich Meyerhofer studied Engineering Physics at Cornell University and received the PhD degree in Physics from MIT in 1957. His thesis was a study of the ferroelectric transition in barium titanate. Since 1958 he has been a staff member at the RCA Laboratories in Princeton, NJ. His research has been concerned with galvano-magnetic and transport properties in semiconductors and insulators, with nonlinear optical effects and the properties of infrared lasers, and with holographic processes and materials. He has carried out studies of electro-optic effects in liquid crystals and of the mechanisms underlying the functioning of dynamic scattering and field-effect display devices. For two years, he was a member of an applied research group that was concerned with electronic and optic applications to the printing industry. This involved electronic photocomposition and holographic character generation, laser exposure of various kinds of printing plates, and electronic screening of black-and-white and color images for printing. The possibility of direct etching of gravure cylinders by Q-switched laser was demonstrated. The holographic investigations led to the demonstration that focussed image holograms can be used to produce high resolution microfiche.

More recently, Dr. Meyerhofer has been concerned with testing and characterizing resists for microlithography. In the case of the positive resist systems based on diazoquinone sensitizers in novolak resins, he studied the effect of exposure on the destruction of the sensitizer and the relationship between sensitizer and development rate (contrast and sensitivity). Exposures by uv light and electron beams were compared. To interpret the results obtained, he also developed appropriate analytical models of the microlithographic processes. These models are used for optimizing the process parameters.

Dr. Meyerhofer has also provided consultation to the MEBES and mask-making facility and to the optical lithography operations at the RCA Solid-State Division. He is a member of the American Physical Society, of the IEEE, and of Sigma Xi.

Edward A. Miller received the B.A. degree in Chemistry from LaSalle College in 1960 and the M.S. degree in Chemistry from Drexel University in 1966. In 1978 Mr. Miller was promoted to Associate Member of the Technical Staff. Since joining RCA Laboratories in 1960, Mr. Miller has been engaged in research on Czochralski growth of gallium phosphide, vacuum deposition of silicon, and vapor phase growth of III-V compounds and silicon. His recent interest has been with silicon epitaxial reactor development for silicon epitaxial power devices and solar cells.

Paul H. Robinson graduated from New York University with a BA degree in Chemistry in 1951 and received an MS degree in Physical Chemistry from Polytechnic Institute of Brooklyn and Massachusetts Institute of Technology in 1955. He was employed by MIT as a staff member at Lincoln Laboratory from 1952 to 1959. There he was part of a group which was the first to determine the oxidation kinetics, thickness, and isosteric heat of adsorption of oxygen on atomically clean germanium surfaces after oxidation. From 1959 to 1962, at Raytheon's Semiconductor Division Advanced Development Laboratories, Mr. Robinson was mainly involved with surface studies on silicon and silicon devices. He joined the research staff at RCA Laboratories in 1962 and developed the close-spaced technique for the vapor transport of germanium and III-V semiconductors. He has worked on the epitaxial growth of silicon, silicon device structures, and the characterization of silicon on insulators, and was the first person to use the silane system for this purpose. In 1964, along with C. W. Mueller of RCA Laboratories, he reported the first MOS devices made with these films. He also reported the first useful bipolar transistors made by means of an all-epitaxial approach and helped develop a technology for improving minority-carrier lifetime in silicon on insulator films. For the past several years Mr. Robinson has done extensive research and development work on epitaxial high-voltage device structures as well as on the growth and evaluation of epitaxial silicon solar-cell structures on both single-crystal and polycrystalline silicon substrates.

Mr. Robinson has received three RCA Achievement Awards and holds nine U.S. patents. He is a member of the Electrochemical Society.

John R. Sandercock graduated in physics from Oxford University with a B.A. in 1964 and D.Phil in 1968 on hot electron effects in semiconductors. Since then he has been working at Laboratories RCA Ltd., Zurich, in the field of light scattering in solids and has brought about significant improvements in the instrumentation for high resolution interference spectroscopy. He holds four patents.

Richard A. Soltis is a Technical Assocate at RCA's David Sarnoff Research Center, Princeton, NJ, and is a member of the Materials Synthesis Research Group within the Materials and Processing Research Laboratory. He joined RCA in 1960 working on the electrical characterization of III-V compounds, the characterization of photochromics, the chemical vapor deposition of thin film dielectrics and heteroepitaxial growth of III-V and II-VI compounds. He is presently involved in the characterization of polysilicon films and plasma etching of dielectrics.

Edgar F. Steigmeier received the Physics Diploma in 1955 and the PhD in Physics in 1960 from the Swiss Federal Institute of Technology (ETH) in Zurich. From 1960 to 1962, he worked for Brown Boveri Corporation, Baden, Switzerland, on heat conductivity and thermoelectricity. In 1962 he joined the Materials Research Laboratory of RCA Laboratories, Princeton, where he worked on basic properties and applications of thermoelectric materials such as Ge-Si alloys and III-V alloys, which has lead to high efficiency materials for power generation. In 1964 he transferred to Laboratories RCA Ltd., Zurich. There he worked on problems of heat transport, on optical properties of magnetic semiconductors, and materials involving soft lattice vibrations and phase transitions. Later work was concerned with light scattering of layer structures and of inorganic and organic conductors. At present he is involved in materials characterization (by means of elastic, Raman scattering and optical scanner) of VideoDisc, Polysilicon and Storage Disc materials. In 1969 Dr. Steigmeier received an RCA Laboratories Achievement Award for his contributions to the study of materials by means of Raman effect, and in 1979 a second one for the invention of a laser scanner for dust and defect detection. During the Academic year 1973/74 Dr. Steigmeier was teaching as a guest lecturer on Solid State Physics at the University of Fribourg, Switzerland. He holds one U.S. patent and is a member of the Zurich, Swiss, European, and American Physical Societies.

Martin Tgetgel graduated in fine mechanics in 1970. From 1970 to 1971 he attended the Swissair aircraft mechanics school. For the following two years he was employed with Standard ITT, Zurich.In 1973 he joined Laboratories RCA Ltd., Zurich. He was involved in investigations of charge storage on insulating materials and the development of electronic circuits for an optical scanner for dust and defect detection on semiconducting materials. From 1972 to 1976 he attended the Zurich City Evening College in Electronics. In 1978 he was promoted to TSA. At present he is working on circuit aspects of optical instrumentation for IC technology and of a tunneling spectrometer.

Lawrence Keith White majored in Chemistry and, in 1970, received his AB degree from Earlham College, Richmond, IN. In 1975 he received his PhD degree in Physical Chemistry from the School of Chemical Sciences at the Univesity of Illinois (Urbana). His doctoral thesis was entitled "Electron Paramagnetic Resonance Studies of Cu(11) Complexes." Dr. White was a postdoctoral Research Associate at the University of New Hampshire, Durham, where he worked on problems concerning the characterization of metal-ion sites in metalloproteins and biological crystals. In 1978 Dr. White joined RCA as a member of the Solid State Process group at the David Sarnoff Research Center, Princeton, NJ. There his work dealt with IC reliability and processing, including studies of metallization corrosion, chemical etching, and device topology. In 1979 he became a member of the Lithography and IC Process Group and is presently engaged in Lithography research for VLSI processing.

Dr. White is a member of the American Chemical Society, Sigma Xi, Phi Lambda Upsilon, Alpha Chi Sigma, and the Electrochemical Society.