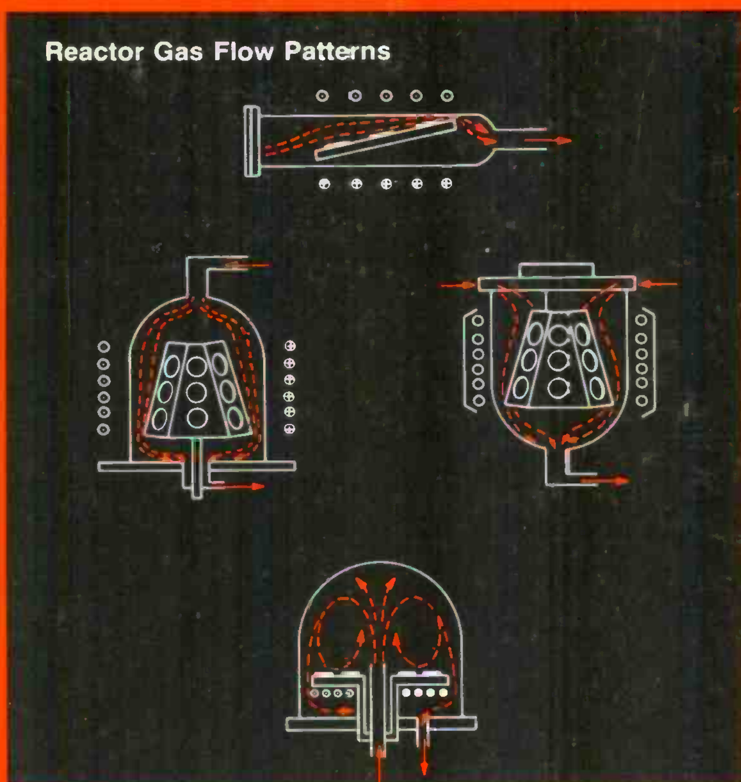
RCA Review



Semiconductor Materials and Processes
Part 2: Preparation and Properties

June 1983 Volume 44 No. 2

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Our cover shows schematic presentations of currently used reactor configurations for deposition of homoepitaxial silicon on IC wafers: horizontal, rf-heated barrel, radiant-heated barrel, and vertical. The gas flow pattern in each reactor is highlighted. The illustration is taken from the paper "Epitaxial Reactor Systems: Characteristics, Operation, and Epitaxy Costs" by Cullen, Corboy, and Metzl.

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Editor's Note

This *RCA Review* constitutes the second of a two-issue accumulation of RCA technical research reports on Semiconductor Materials and Processes. The papers are written by specialists in their fields and are intended primarily for other optoelectronic and microelectronic experts.

While Part 1 (March 1983) is mainly concerned with fabrication technology and devices, this issue concentrates on the preparation and properties of materials. Together, the two publications provide some indication of the depth and breadth of the subjects and disciplines studied by RCA scientists.

For the convenience of the reader, the table of contents from Part 1, the March 1983 *RCA Review*, is reprinted below:

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Epitaxial Reactor Systems: Characteristics, Operation, and Epitaxy Costs

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Abstract—In this paper we discuss the design and operating characteristics of various homoepitaxial reactor systems now being employed in the semiconductor industry. The parameters available for control of the deposit characteristics, specifically as related to the reactor configurations, are outlined. The current technology of slip control through rf-heated susceptor design is reviewed. The very significant advantages associated with reduced-pressure epitaxial growth are presented.* The throughputs and costs involved in each reactor are analyzed. Finally, we make some predictions concerning the future trends of development in epitaxial reactor technology.

1. Introduction

There has been a recent focus on improving the capabilities of epitaxial reactor systems to meet the needs of the various IC device structures fabricated in homoepitaxial silicon. As the spacings of the circuit elements are decreased, crystallographic defects have more impact on device performance and processing yields. Thinner deposits and relatively abrupt dopant profiles are required to accommodate the decrease in the device element spacings. At the same time, cost and throughput have become more important issues in response to the more competitive semiconductor market place. These factors have led to a re-evaluation of epitaxial reactor performance, redesign of systems, and optimization of reactor operation.

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* In this paper we deal only with silicon deposition from $SiCl_4$ and the halosilanes. We do not include references to the growing body of literature on reduced-pressure epitaxial growth from silane.

A number of reviews have been written in which discussions on reactor systems and operating characteristics are included. The most recent and complete is by Pogge.[1] Much of the discussion of reactor operation for heteroepitaxial silicon[2] is also applicable to homoepitaxial silicon reactor systems. The purpose of this review is to update the characteristics of the various reactor systems available today and to discuss in some detail the interaction between reactor characteristics and the manipulation of deposition variables that influence the capabiltiy to achieve the desired properties in homoepitaxial silicon. The cost of homoepitaxial deposition in the various reactors has also been analyzed since this is such an important factor in today's commercial environment. Recent developments are overviewed, and current and future trends are discussed.

2. Reactor Configurations

The currently employed reactor configurations are summarized in Table 1. The essential features of these various reactor designs are the geometry of the susceptor, the nature of the gas flow, and the method of heating the substrate. The gas flow patterns are shown schematically in Fig. 1.

2.1 Horizontal Reactor

The horizontal reactor is the most simple of the reactor types. For many years this was the most commonly employed configuration. In the United States it has generally been replaced because of the relatively low wafer capacity and the problem of downstream contamination of deposits when more than three or four wafers are aligned in the direction of the gas stream. Because of its simplicity, this reactor is used for basic studies in the U.S., and is still employed in commercial operations in Europe. The barrel geometry (described in the next section) has found favor over the horizontal configuration because it can accommodate more substrates per run without the need to align more than four wafers in a single row in the direction of the gas stream.

In the horizontal reactor, the gas flow is straightforward, entering the tube in one end and flowing symmetrically across the susceptor face. The nature of the flow in these two reactor types can be analyzed by established fluid flow relationships. This has been discussed in detail by Eversteijn,[3] Berkman,[4] and Ban.[5] Eversteijn applied the concept of a boundary layer to develop relationships that describe quantitatively the depletion of the nutrient gas. While

Table 1—Reactor Configurations

Common Reactor Nomenclature	Susceptor Geometry	Gas Flow	Method of Heat Input	Manufacturer
Horizontal	Parallelepiped slab	One pass displacement	rf coil outside chamber	ASM (U.S. and Netherlands)
Vertical	Disc, often called pancake	Recirculating	rf coil inside chamber	Epitaxy Equipment, Inc. (U.S.), Kokusai (Japan)
rf Barrel	Barrel	One pass displacement	rf coil outside chamber	Timesa (Switzerland), RCA In-House Produced Units
Radiant Heated Barrel	Barrel	One pass displacement	Heat lamps	Applied Materials, Inc. (U.S.)

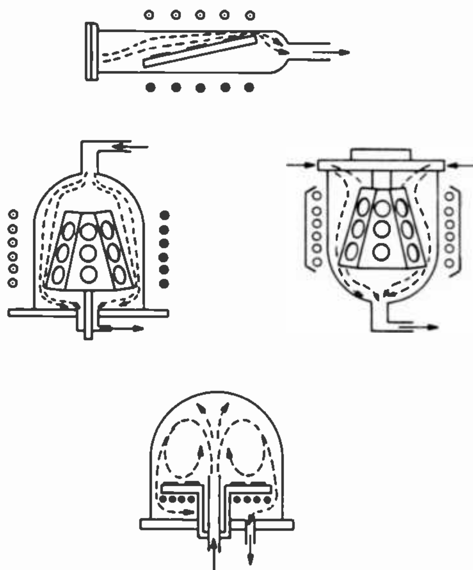


Fig. 1—A schematic presentation of the rf heated horizontal, barrel, and vertical reactor systems. Gas flow patterns are indicated.

there has been recent disagreement on the physical reality of the boundary layer, these relationships are nonetheless still useful in calculating the angle of tilt of the susceptor needed to provide uniform deposition of silicon in the direction of the gas stream. Refinements of fluid-flow calculations have been offered by the more recent investigators to more accurately explain experimental data.

2.2 The RF-Heated Barrel Reactor

In the original configuration of the rf-heated barrel reactor, the substrates were positioned in recesses on the outer surface of a cylinder with vertical walls and the reactant ambient was contained within an opaque quartz cylinder.[6,7] With this geometry, the deposit uniformity within a vertical row of wafers was controlled by "adjusting total gas flow and gas part location."[7] Within RCA, this type of reactor was optimized for the preparation of relatively thick deposits for power device applications.[8] For this application, a certain degree of slip in the homoepitaxial silicon is acceptable. In the RCA configuration, the deposit uniformity in the vertical direction is controlled by angling the susceptor face to decrease the annular area with distance down the susceptor. Also, a thin transparent quartz reactant gas envelope is employed. This reactor has been in contin-

uous operation for a number of years within RCA. Reactors designed using these basic concepts are now commercially available (Preti Engineering, San Giuliano, Italy and Timesa Microelectronics s.a., Biasca, Switzerland).

In the barrel reactor with the angled faces on the susceptor, the nutrient gases are introduced axially and flow symmetrically across the faces of the susceptor. The flow across any one face of the barrel susceptor is essentially the same as in the horizontal reactor, and therefore the nature of the gas flow can be analyzed according to the fluid-flow relationship mentioned earlier.

2.3 The Radiant-Heated Barrel Reactor

The radiant-heated barrel reactor has been employed in applications where the device performance is strongly influenced by crystalline perfection. With the use of heat input through radiation, slip in the substrate/deposit composite has been minimized (this is discussed later). The Applied Materials, Inc. radiant-heated reactors differ from rf-heated reactors not only in the method of heat transfer, but also with respect to the method of introducing the gases and the flow pattern in the annulus between the susceptor and the bell jar. The gases are introduced through two opposing jets located at the circumference of the upper section of the reactor. This is shown schematically in Fig. 2. As the gases meet, a complex unsymmetrical flow results in which much of the nutrient is channeled from top to bottom on one side of the reactor. As a result, the silicon deposition rate continually changes as the substrates are rotated through this channel of nutrient gases. The impact of this flow pattern is discussed in another paper in this issue.[9]

2.4 The Vertical Reactor

The vertical reactor geometry has received wide acceptance because it is relatively simple to operate and maintain. Until recently it has been difficult to control slip in this reactor, and a good deal of effort has been directed toward correcting this situation. This is discussed later. This configuration has been called the vertical reactor because the gas is introduced normal to the horizontal susceptor surface. It is also commonly referred to as the "pancake" reactor because of the geometry of the susceptor.

The flow pattern in the vertical reactor is complex. The gases are introduced from an inlet that protrudes through the center of the susceptor, impinge on the hemispherical upper portion of the bell

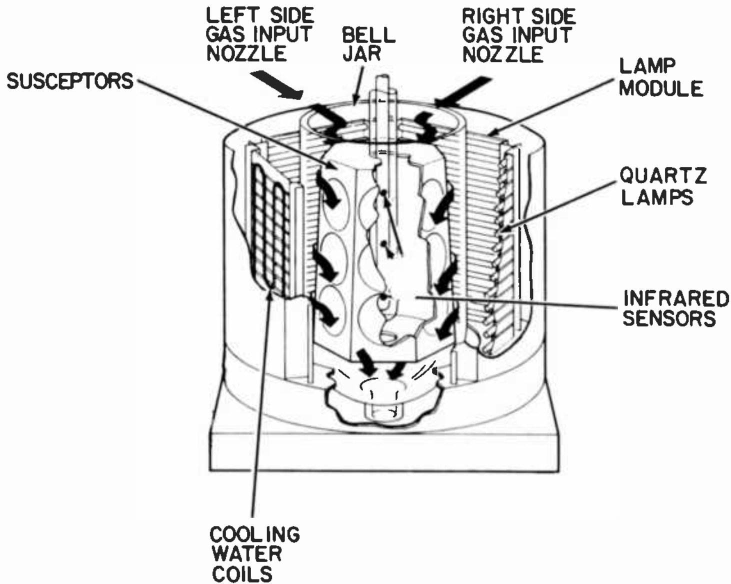


Fig. 2—A schematic cutaway of the AMC-7900 reactor. The gas flow pattern is indicated.

jar, and swirl down the sides of the bell jar and across the substrates. The gases may recirculate over the substrates many times before they exit through the annulus between the susceptor and the bell jar.

2.5 Susceptor Rotation

In the barrel and the vertical reactor types, the susceptor is rotated to compensate for asymmetries in the shape of the gas passage that result from nonsymmetrical quartz parts and lack of coincidence between the axis of rotation of the susceptor and the axis of the bell jar. In the case of the radiant-heated reactor, the susceptor is rotated both to compensate for the unintentional asymmetries of the apparatus and to achieve the desired deposit uniformities in the environment of the gas flow asymmetries imposed by opposing jet inlets.

3. Elements of Control in Epitaxial Reactors

The key deposit characteristics to be controlled in the epitaxial growth of silicon for device applications are:

- thickness uniformity
- resistivity uniformity

- dopant profile
- crystalline quality
- pattern integrity (shift and distortion).

Reactor variables available for control of the deposit characteristics are:

- method of the delivery of the nutrient gases to the substrate surface, i.e., the gas flow pattern
- control of the input of heat into the substrates; rf coil, heat lamp, and susceptor design
- deposition pressure.

An additional control parameter is the chemical nature of the nutrient gas. In general, however, the considerations involving the chemical nature of the nutrient gas are not specific to the reactor design. Since the emphasis in this discussion is on reactor design and optimization, we do not include a discussion of the choice of nutrient gases.

In efforts to achieve the desired deposit characteristics, the major control elements are set by the selection of reactor geometry, source gas, temperature, and rate. The deposition process is then "fine-tuned" within the limits possible with the particular reactor design. Many approaches are possible, but in general the control elements manipulated to achieve the desired deposit characteristics are as described in the following sections.

3.1 Thickness Uniformity

A source gas/deposition-temperature regime is chosen in which the deposition rate is not a strong function of the deposition temperature. Under these circumstances, small temperature variations on the susceptor surface are tolerable, and trimming of the temperature can be used to control other characteristics (see below). The thickness is then dominated by the manner in which the nutrient is delivered to the substrate surface. In the most simple horizontal reactor, the primary control elements are the angle of the susceptor in the quartz envelope and the flow rates of the various gases. The susceptor angle can be calculated according to known fluid-flow relationships discussed earlier. Using the concept of the boundary layer, the angle of the susceptor is adjusted in such a way that the cross-sectional area of the gas passage decreases in the direction of the gas flow. The depletion of the nutrient is balanced by a decrease in the boundary layer across which the nutrient species must flow to reach the substrate.

The equivalent control element in the barrel type reactors is the

angle between the susceptor face and the vertical bell-jar wall. As already mentioned, the nature of the gas flow in the horizontal reactor and a single face of the barrel reactor is essentially equivalent with respect to the fluid-flow dynamics. In the Applied Materials, Inc. radiant-heated reactors, an additional control parameter is added since the gas flow from the two opposing injection jets is not symmetrical. In this case the thickness uniformity is also a strong function of the orientation of the gas jets.

In the vertical reactors the deposit uniformity is a function of the distance between the hemispherical surface of the bell jar, the susceptor surface, and the gas inlet opening. Various gas inlet mechanisms have been used in the past. For instance, in one configuration the gas inlet was made up of two bell-shaped openings connected to the ends of a rotating T-shaped gas inlet. Such schemes have not proven, however, to be necessary. Sufficient control is achieved by a simple adjustment of the height of the inlet opening above the susceptor surface, and the initial choice of the bell-jar height and the back pressure of the gas exhaust. Thickness control is very good in this reactor. This may be in part due to the recirculating nature of the gas flow pattern.

3.2 Resistivity Uniformity

Even under the conditions that the overall deposition rate is not a strong function of the deposition temperature, the ratio of the rate of reduction (or pyrolysis) of the silicon bearing species to the dopant bearing species is sufficiently dependent on the deposition temperature to serve as a viable control element. Therefore the fine-tuning of the resistivity uniformity is carried out by adjusting the temperature profile across the susceptor in the direction of the gas flow. In the rf-heated reactors this control is achieved mainly by the overall position of the coil in relation to the susceptor and the coil design. In the rf-heated barrel geometries, the dominant control feature is the distance between the coil windings, while in the vertical reactor the dominant control is the distance between the susceptor and the various sections of the spiral coil attached to an insulating plate positioned below the susceptor.

In the radiant-heated reactor, the heat lamps are divided into three separate sections. The temperature of the two end sections may be independently offset in relation to the central controlled zone. By adjustment of the offsets, the top-to-bottom temperature profile can be adjusted.

3.3 Dopant Profile

Some of the approaches employed to achieve abrupt dopant profiles over heavily doped substrate areas are not specific to the reactor design. These include, for instance, sealing the backside of the substrate and the use of capping layers. Other approaches are influenced by the reactor design. A key reason for the shift in emphasis from the simple horizontal configuration to the barrel design was to accommodate as many substrates as possible without positioning many substrates in a single row along the direction of the gas flow. The problem of the transfer of material from an upstream to a downstream wafer clearly increases with the number of wafers in a single row. The barrel reactor essentially is made up of a series of short horizontal reactors wrapped around the circumference of the barrel. In this configuration each vertical row can be short as compared to the horizontal reactor. In the horizontal reactor special effort, such as very high total gas flows, must be employed to avoid the transfer of chemical species from the upstream to the downstream deposits.

Under normal operating conditions, it is reasonable to assume that the cross-contamination between substrates on the susceptor surface would be more of a problem in the gas recirculating (vertical) type of reactor than in the gas displacement (horizontal and barrel) reactor systems. In the gas displacement type reactors, chemical species unintentionally introduced into the deposition environment are more readily expelled from the system than in the recirculating reactor. Related to this is the ease of flushing of the reactor space. Where abrupt dopant profiles are required, it is accepted practice to incorporate a flushing step in the deposition sequence to purge the reactor of unintentionally added gas constituents.

Such flushing is more difficult in the vertical reactor, both because of the recirculating feature and the relatively large gas space within the reactor. It appears, however, that compensation can be made for these effects by the appropriate design of deposition sequence. This is not, however, documented in the literature. It is unlikely that the necessity to employ such procedures, such as more extensive flushing, will significantly impact on epi costs.

The use of reduced pressure is proving to be an important parameter in dopant profile control in silicon deposited from halide-bearing gases.[10–17] Significantly more abrupt dopant profiles can be achieved at reduced deposition pressures. The ease of use of reduced pressures is a function of the reactor configuration. Reduced pressures are readily achieved in the barrel geometry: the cylindrical geometry

can readily withstand the pressure difference, and the gas volume is relatively small. It is unfortunate that in the radiant-heated reactor, wall deposits on the inner surface of the bell jar increase with decreasing pressure. This constitutes a real disadvantage since reduced pressure operation requires additional reactor maintenance. The magnitude of this effect has not been documented in the literature. Success has been achieved in suppressing bell-jar deposits in the newest reactor systems.

In the rf-heated barrel reactor, the reduction of the deposition pressure is limited by the formation of a gas plasma. In the vertical reactor, the deposition gas is not surrounded by the rf coil and is separated from the coil by the susceptor. With the appropriate precautions in the design of the coil standoff insulators, reduced pressure operation is feasible in the vertical reactor.[18] Development activities are now in progress on reduced-pressure deposition in the vertical reactors, but results have not been reported in the literature to date.

An additional issue which is not as yet defined in the literature is the impact of reduced pressure on the vertical temperature gradient as a function of the method of heating the substrate. In the radiant-heated barrel configuration, reduced pressure does not significantly impact the radiation transfer of energy into the substrate. In the other reactors the gas environment is a factor in the transfer of the thermal energy from the susceptor surface to the substrate, and very significant increases in the thermal gradient normal to the substrate surface have been observed as the deposition pressure is reduced.[19] This may have a significant impact on slip control. It is possible that the recessed susceptor designs now being developed for the control of slip in the rf-heated reactor systems may also minimize the impact of reduced-pressure operation on the vertical thermal gradient. It may also prove to be necessary to employ susceptor recesses specifically designed for reduced pressure operation.

Reduced-pressure deposition is not possible in the conventional horizontal reactors. The quartz envelope, with a rectanglular cross section, would collapse under the pressure differential. The slab geometry susceptor can be enclosed within a cylindrical envelope, but this has the disadvantages that the rf coil is further removed from the load and the gas flow pattern over the substrate is considerably perturbed.

3.4 Crystalline Quality

A number of the important variables that impact the crystalline quality of the homoepitaxial deposits are not specific to the reactor

configuration. The most important of these is the condition of the substrate surface, both with respect to crystalline perfection as it enters the reactor and the in-situ removal of the natural oxide from the surface. The key reactor-related parameter is control of thermal gradients across the substrate, both in the direction normal to the surface and in the plane of the surface. The main motivation for the use of the relatively complex radiant-heated configuration has been that, since the silicon is heated by radiation, the thermal gradient normal to the substrate surface is essentially zero. The epitaxial silicon deposited in a radiant-heated reactor is therefore very nearly slip free. When slip is present, it is observed primarily at the top edges of the wafers on the top row and bottom edges of the wafers on the bottom row where the wafers are placed over a 12-inch vertical distance. This slip is clearly associated with thermal gradients in the plane of the susceptor face at the ends of the susceptor.

In the rf-heated reactors the substrate receives the thermal energy through radiation from the susceptor, through contact with the susceptor, and through convection in the gas layer between the substrate and the susceptor. As the result of the latter forms of heat transfer, a thermal gradient is imposed across the thickness of the silicon. This results in the generation of slip in the substrate, which is propagated into the deposit. Recent advances in susceptor design, which to a large extent compensate for this effect, are discussed in a separate section.

In all reactor types care must be taken to locate the substrates far enough away from the edges of the susceptors to avoid thermal gradients in the plane of the substrates that result from heat loss from the edges of the susceptor. In an effort to achieve as large a wafer load as possible, the wafer recesses are often located too close to the substrate edge.

3.5 Pattern Integrity

The control of pattern integrity relates to reactor design to the extent that reduced pressures can be employed and to the extent that the reactor can be operated at relatively high deposition temperatures without significantly increasing the time consumed in maintenance. Pattern distortion in (100) silicon decreases with increasing deposition temperature and decreasing growth rate.[13–15,20] It is not unusual to operate reactors in excess of 1200°C to control pattern distortion. In the radiant-heated reactor, this may result in increased maintenance due to bell-jar wall deposits. Operation of the reactor at these elevated temperatures is, however, common

practice when both pattern integrity and crystallinity are characteristics of concern.

Pattern distortion decreases with decreasing deposition pressure.[11–16] At reduced pressures, the deposition temperature can be decreased to advantage. Unfortunately, the bell-jar wall deposits also increase with decreasing deposition pressure. Therefore an optimum balance must be made between achieving acceptable pattern distortion and minimizing the wall deposits. There are other very real advantages, however, in the use of relatively low deposition temperatures. The key factor is the suppression of the solid-state diffusion of dopants, which becomes more important as device spacings are decreased. Also, as thermal gradients are decreased with decreasing deposition temperatures, slip and warpage are decreased. The deterioration of reactor components also decreases with decreasing deposition temperatures. We anticipate that, for these reasons, reduced pressure will be employed more commonly in the future.

4. Susceptor Design

We discussed susceptor design as it relates to the manipulation of gas flow across the susceptor surface in an effort to maximize deposit thickness uniformity. A good deal of discussion may be found in the literature on this topic. Susceptor design has also been employed over the years in an effort to suppress the introduction of stress into the substrate wafer. Unfortunately most of this effort has been proprietary and has not found its way into the literature. Recently McD. Robinson and co-workers[21,22] reported on the effectiveness of a specific susceptor design in the suppression of slip. This work has resulted in more open discussion among investigators in the field on the topic of susceptor design. This area of development is particularly relevant at this time because of the emphasis on the control of crystalline perfection to meet the increasingly demanding requirements for IC device applications.

It has been recognized in the past[23–26] that crystallographic defects are generated in a silicon wafer heated by a flat rf-heated susceptor at temperatures used in epitaxial growth. The sequence of events that leads to slip formation is as follows:

- The wafer lies on a flat surface. Ideally a perfectly flat wafer on a flat susceptor would be in direct contact over the entire area of the wafer; in reality this is not the case, and one can assume only local direct contact, with a gas gap between the wafer and susceptor over much of the area. Unless the wafer is badly distorted,

however, this is not the primary factor that leads to slip generation.

- The wafer is heated by conduction through direct contact with the susceptor, contact with the gas layer, and radiation.
- The front surface of the wafer is cooled through radiation into the relatively cool gas; this causes an axial (normal to the surface) thermal gradient in the wafer. The axial gradient is not the direct source of slip generation.[26]
- The axial gradient causes the wafer to curve, with the outer edges lifting from the hot susceptor surface and protruding into the cooler gas. This results in the introduction of radial (in the plane of the substrate) thermal gradients; as the edge lifts further from the susceptor surface, the effect is enhanced. Estimates have been made of the temperature of the edge based on the fluid flow in the gas[26] and radiation into the edge.[24]
- As a result of the thermal gradients, compressive stress is set up as the outer cooler rim of the wafer shrinks in relation to the hotter center. As the critical stress value is exceeded, the stress is relieved by slip both at the outer edges and at the center[25] of the wafer.

The generation of slip by the sequence described above is not a function of the thickness of the wafer[24,25] and is essentially independent of the formation of the epitaxial deposit.[26] It is also not a strong function of the rate of heating or cooling of the wafer.[26]

The generation of thermally induced slip is a function of the initial crystallographic quality of the wafer. Damage at the wafer edges is an important source of the introduction of slip. It is also known that oxygen intentionally introduced into the substrate for the purpose of internal gettering may significantly reduce the strength of the wafer. This will be an important consideration with the more common use of internal gettering in the future. To date, there has been no report in the literature of the relationship between oxygen content and slip generation during the epitaxial process.

In this discussion we have dealt only with defects introduced into the silicon through thermal effects. Crystalline defects can also result from lattice spacing differences when the dopant concentration and/or type in the substrate and the epitaxial layer is different. The relative contribution of these two factors has been discussed by Blanc.[27]

Various means have been proposed to minimize the formation of the radial thermal gradients as the wafer sits on the hot susceptor at epitaxial deposition temperatures. The simplest approach is to elevate the wafer by small protrusions from the susceptor surface.

It is reported that this is effective for 2-inch-diameter wafers but not for larger substrates.[28] Another approach has been to selectively thin the susceptor (by forming a recess in the back) to produce thermal gradients on the surface of the susceptor that leads to heating of the outer edge of the wafer to a temperature higher than the central portion.[29] It is reported that this is effective for 3-inch wafers in a horizontal epitaxial reactor. Such an approach would be specific to a particular susceptor/coil configuration. Other simple approaches have been to place the wafer in a flat-bottom recess in the susceptor so that the walls of the recess serve as a heat source radiating into the edge of the wafer.

McD. Robinson and associates have demonstrated[21,22] that if the wafer is placed in a recess which is a section of a sphere, there exists an optimum recess depth for which slip is reduced to zero (under the conditions employed by these investigators). The depth of the recess has been correlated with the thermal gradients across the surface of the wafer. While it has been found that the thermal gradients can effectively be reduced to zero, it has also been observed (as previously reported[29]) that minimum slip is achieved when the wafer edges are intentionally held at a temperature higher than the center of the wafer. This work was carried out in a horizontal reactor. We, and other investigators, have attempted to apply this technology to the vertical reactor. While success has been achieved in suppressing the slip, we have not been able to achieve slip-free substrates at the higher ($\gtrsim$1200°C) deposition temperatures.

Variations of the spherical recess have been investigated. These include a ledge with a spherical recess (as shown in Fig. 3), a ledge with a flat bottom recess,and a ledge with a recess curved at the outer edges but flat at the bottom.[18]

There is disagreement among investigators working with recessed susceptors on how the recesses lead to the suppression of slip. One view is that heat conduction is shifted mainly from contact (on a flat surface) to radiation and gas conduction (over recesses).[30] The other view is that the wafer conforms to the recess, thus increasing thermal input, particularly at the edges. Considering the conduction model, it is difficult to explain why the slip suppression is such a strong function of the depth of the recess. With the contact model, it is difficult to explain how each silicon wafer will be stressed to exactly the shape of the recess (at least at the edges). A general problem in dealing both conceptually and quantitatively with either of these models is that the curvature of the wafer at the deposition temperature will be a function of silicon materials variables as well as susceptor dimensions. It seems likely that the lack of reproduc-

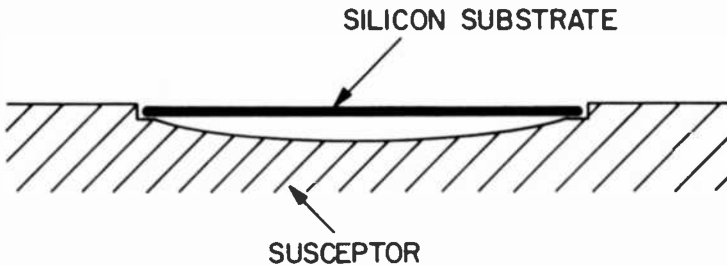


Fig. 3—A schematic cross section of a double-recess rf heated susceptor (not to scale).

ibility evident in this technology can be attributed to the fact that the differences in distortion of the various types of silicon are greater than the critical control dimensions of the susceptor shape. Thus, to make slip control through susceptor shaping a viable technology, it is necessary to develop methods wherein the effect is less a function of small dimensional changes.

To date, recessed susceptor technology has mainly been focused on the vertical reactor configuration. Efforts are now being made to apply this to the rf-heated barrel susceptor geometry. One can anticipate that if the recesses are operative through the radiation model, the technology already developed for the rf-heated pancake susceptors of the vertical reactors will be directly applicable to the barrel susceptors. If, however, the recesses are operative through conformance between the wafer and the recess, the current recess technology may not be directly applicable to the barrel configuration. No reports have been made to date of the suppression of slip through the use of recesses on the rf-heated barrel susceptors. This will certainly be a key issue in the future use of rf-heated barrel reactors.

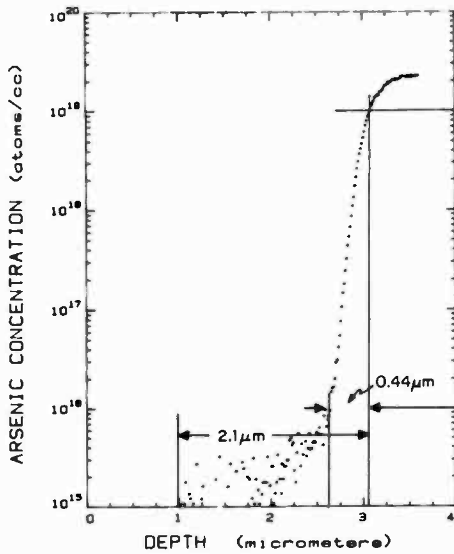
Another factor of concern in the recessed susceptor technology is the impact of reduced pressure on slip control. As the pressure of the deposition environment is reduced, the thermal conductivity of the gas is lowered, and gas convection in the recess between the substrate and the susceptor will be altered. We have previously pointed out that relatively large differences between the temperature of the substrate and the susceptor have been observed at reduced pressures.[19] The configuration of the susceptors shaped for slip suppression may prove to be a function of deposition pressure. The ease of slip control at reduced pressure with the shaped rf-heated susceptors will be an important consideration in the choice of the radiation or rf-heated reactor configurations.

5. Reduced-Pressure Epitaxial Growth

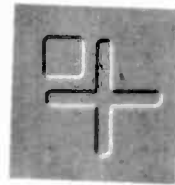
We have referred earlier (Sec. 3.3) to the use of reduced pressure as an additional epitaxial growth control element. At reduced pressures, gas diffusion rates are increased and convection currents are suppressed. Enhanced control of autodoping, pattern shift, and thickness and resistivity uniformity have been reported in reduced-pressure epitaxial growth from $SiCl_4$ or the chlorosilanes.[11-16] In thin epitaxial deposits (1–3 μm) for a number of applications the key issue is dopant profile control. In the thicker epitaxial deposits (~15 μm) for bipolar applications, a key issue is control of pattern integrity. In both cases the deposit characteristics are considerably enhanced by deposition at reduced pressure and relatively low deposition temperatures.

To put the proper focus on this important control element, examples of the impact of reduced pressure growth are shown in Figs. 4 and 5. Secondary ion mass spectrometry (SIMS) dopant profiles and micrographs of the alignment patterns are shown for deposits prepared at 760 and 100 Torr. Depositions represented in Fig. 4 were carried out from $SiCl_4$ and in Fig. 5 from SiH_2Cl_2. The improvement in deposit characteristics is evident.

$SiCl_4$ is typically used as the source gas at deposition temperatures ≥1150°C. At deposition temperatures above ~1190°C, the pattern integrity of (100) epitaxial silicon is acceptable, but for other reasons (for instance, lateral autodoping, slip, and reactor maintenance) the higher temperatures are undesirable. The use of reduced pressures in the temperature range between 1150 and 1190°C provides the needed control of the pattern integrity and at the same time inhibits the increase in the dopant transition width, which otherwise occurs with decreasing deposition temperatures. At lower extremes of the temperatures (1080-1100°C, with SiH_2Cl_2), the pattern distortion is acceptable for deposits less than 10 μm thick. Since the distortion shifts from negative to positive with decreasing pressure, if desired, the change in the outside edge dimensions of the patterns in the epi can be held to zero with the appropriate choice of pressure. At these lower temperatures, however, the more advantageous use of reduced pressure is in the control of the vertical dopant transition width. At 100 Torr, the transition width is not a strong function of temperature between 1080 and 1190°C. At atmospheric pressure, the transition width increases with decreasing deposition temperature.[31] An additional advantage in the use of reduced pressure is that, even when the deposition is to be carried

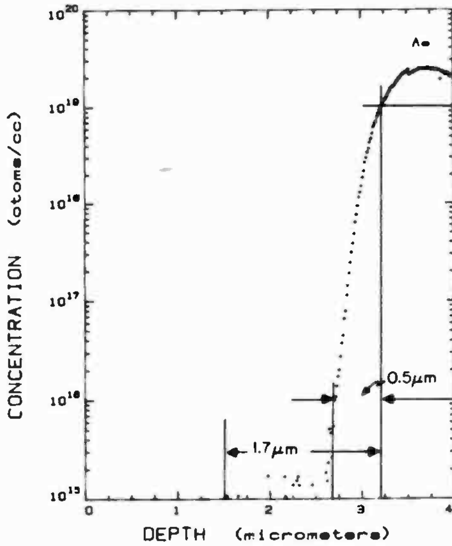


Atmospheric Pressure

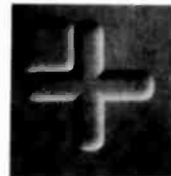


Before Epi

Atmospheric Pressure
t = 11.2 μm

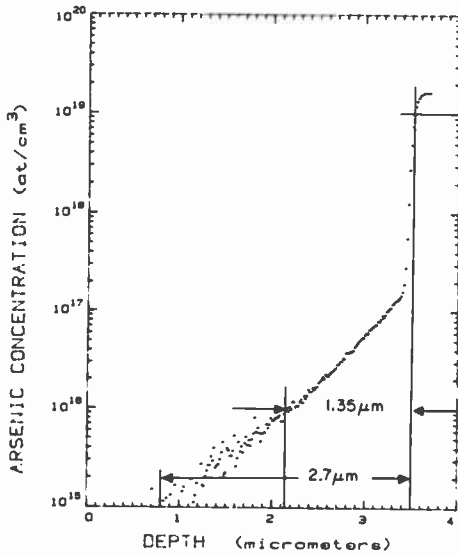


100 Torr

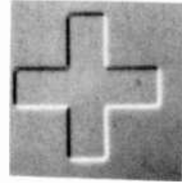


100 Torr
t = 13.8 μm

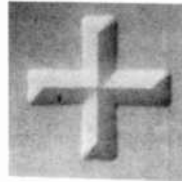
Fig. 4—Vertical dopant profiles and alignment pattern shapes for (100) silicon deposited at atmospheric pressure and 100 Torr from $SiCl_4$ at 1150°C. From Corboy and Cullen.[9]



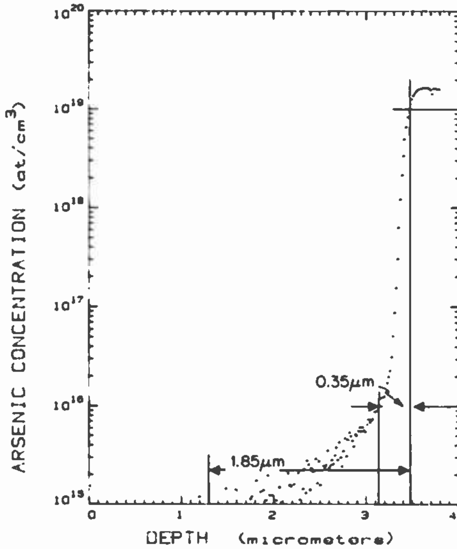
Atmospheric Pressure



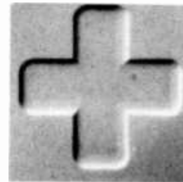
Before Epi



Atmospheric Pressure
t = 12.5 μm



100 Torr



100 Torr
t = 17.5 μm

Fig. 5—Vertical dopant profiles and alignment pattern shapes for (100) silicon deposited at atmospheric pressure and 100 Torr for SiH_2Cl_2. The samples for the profile was deposited at 1080°C; the sample for the pattern was deposited at 1100°C. From Corboy and Cullen.[9]

out at atmospheric pressure, the deposit characteristics can be made less sensitive to a number of operating variables by outgassing the components at reduced pressure prior to deposition.

In the past the reduced-pressure epitaxial growth technology has been impeded by an unwillingness on the part of the users to face increased maintenance related to pumps, back-streaming, etc. These problems can be minimized with relatively straightforward procedures using available technology. The reduced-pressure capability has been commercially available in radiant-heated reactors for a number of years, and operation well below 100 Torr is possible. Reduced-pressure facilities have now been made available in the vertical geometry for operation at pressures $\gtrsim$150 Torr.[18] In the vertical geometry the coil is in the reduced pressure environment, and gas plasma formation may be a limitation. It is anticipated that further development in the coil design will result in the capability to operate this reactor at lower pressures. In the rf-heated barrel configuration, the coil surrounds, but is not within, the deposition ambient. In this case the limitation is the formation of a gas plasma. It is reported that plasma development does not appear to be a problem to pressures less than 10 Torr at 220 kHz.[33] The availability of low-pressure facilitation in this geometry has been announced. The limiting factors in reduced-pressure operation may prove to be increased bell-jar coating in the radiant-heated reactors and increased thermal gradients in the substrate in the vertical reactor geometry.

6. Throughput and Costs

The separate but related issues of throughput and epitaxial deposit costs are discussed in this section. These are important considerations in today's competitive environment. Throughput is an important component of costs but is treated separately here because throughput indicates the number of reactors needed, with associated space, manpower, etc. The throughput and cost analysis of the AMC-7900 and the Gemini I reactors are based on experience. The corresponding inputs for analysis of the Gemini II are based on information from Epitaxial Equipment, Inc. personnel. In this section we do not include the horizontal reactor in the analysis since we have no experience in the operation of this reactor on a routine basis and because we do not consider it to be a viable apparatus for our needs. The wafer loading of the Timesa rf-heated barrel is the same as the radiant-heated barrel. Some difference in the throughput

would be anticipated because of the differences in time dedicated to maintenance of the two reactors.

6.1 Throughput

An example of the accounting of time consumed by an epi run is shown in Table 2. Throughputs of the various reactors are given in Table 3. Included in this table are values for epitaxial deposits on 4-inch substrates with deposit thicknesses of 3 and 15 μm and growth rates of 0.5 and 1.0 μm/min. An uptime value of 90% was used for the more simple vertical reactors, and both 75 and 90% uptimes were used for the radiant-heated reactor. In making a decision on which reactor to introduce into a new production facility, the 75% uptime represents a "worst-case" situation for maintaining one or two reactors in a production environment. Experience in other organizations has shown that unscheduled downtime can be considerably reduced when sufficient reactors are in place in a facility to

Table 2—Typical Run Sequence for the Deposition of a 7-μm-Thick Film (Atmospheric Pressure/$SiCl_4$/1190°C/0.5 μm/min)

Process Step	Time (min)	Auto Program Step
Unload and Load*	3.0	
High N_2 Purge	3.0	1
High H_2 Purge	2.0	2
Normal H_2 Purge	1.0	3
Heat to 850°C and Stabilize (Power clamped for soft start)	7.0	4
Heat to 1190°C and Stabilize (Ramp = 70°C/min)	7.0	5
Purge HCl to Vent	1.0	6
Etch	2.0	7
Post Etch Purge	2.0	8
$SiCl_4$ to Vent	1.0	9
Deposition #1	0.2	10
Postdeposition #1 Purge	5.0	11
$SiCl_4$ and Dopant to Vent	1.0	12
Deposition #2 (Based on 7.0 μm and 0.5 μm/min)	14.0	13
Postdeposition #2 Purge	2.0	14
Reduce Temperature to 850°C and Stabilize (Ramp = 70°C/min)	7.0	15
Heaters Off and Cool in H_2	3.0	16
Cool in N_2	3.0	17
Unload and Load*	3.0	
Total Run Time = 67.2 min.		

* In new 7810 reactors, the system is evacuated and backfilled once at start of run and twice at end of run. This takes approximately 4 min total. Therefore, total run time is reduced by approximately 2 min

Table 3—Comparative Throughput of the AMC-7800 and Gemini Reactors ($SiCl_4$ Atmospheric Pressure, 4-inch-Diameter Wafers)

Parameter \ Reactor	AMC-7900		*AMC-7800 AX		AMC-7900		*AMC-7800 AX	
Reactor Uptime (%)	75		75		90		90	
Deposit Thickness (μm)	3	15	3	15	3	15	3	15
Wafers/Run/Chamber	14		24		14		24	
For 1.0-μm/min Growth Rate								
Runs/Day/System	17	13	17	13	21	16	21	16
Wafers/Day/System	238	182	408	312	294	224	504	384
For 0.5-μm/min Growth Rate								
Runs/Day/System	16	11	16	11	20	13	20	13
Wafers/Day/System	224	154	384	264	280	182	480	312

Parameter \ Reactor	Gemini I				Gemini II			
	Single Chamber		Double Chamber		Single Chamber		Double Chamber	
Reactor Uptime (%)	90		90		90		90	
Deposit Thickness (μm)	3	15	3	15	3	15	3	15
Wafers/Run/Chamber	10		10		22		22	
For 1.0-μm/min Growth Rate								
Runs/Day/System	20	16	26	20	20	16	26	20
Wafers/Day/System	200	160	260	200	440	352	572	440
For 0.5-μm/min Growth Rate								
Runs/Day/System	19	14	24	16	19	14	24	16
Wafers/Day/System	190	140	240	160	418	308	528	352

Assumptions: 90% Operator Efficiency.
100% Yield.
Reduced fixed time cycle in the dual-chamber Gemini I and II due to overlapping runs.
Runs/day values are rounded to the nearest whole number.
Values above do not include scheduled maintenance.
AMC susceptor etched every 120 μm and the Gemini susceptor etched every 360 μm.

* No change in reactor geometry required—only the number of wafers on each susceptor face is increased.

warrant dedicated maintenance personnel. Under these circumstances uptime in excess of 90% can be realized. We operate a radiant-heated reactor in a laboratory environment with well over 90% uptime.

As one might anticipate, throughputs are dominated by the wafers/run values. There is a large effect in operating the AMC-7900 in the "extended" configuration. For 4-inch wafers, the capacity (wafers/run) of the Gemini I is less than half of the AMC-7900, but the loads of the Gemini II and AMC-7800 AX are similar (22 and 24 wafers, respectively).

6.2 Cost

The cost of producing an epitaxial silicon film varies with the thickness of the film, the number and size of substrate wafers, and the capital, operating, and maintenance costs of the reactor used. A cost analysis program, the Interactive Financial Planning System (IFPS), a product of Execucom Systems Corporation, is available through the RCA Computer Services Network. Through the use of a command language, this software allows the generation of a model of a process and the entry of data files representing various implementations of the model. Reports may be generated to show selected outputs of the model, and properties may be changed interactively (by using WHAT IF, IMPACT, SENSITIVITY, etc. statements) to show the effects of process variations on costs and throughput.

The cost model "REACTOR" was constructed to allow the evaluation of epitaxial deposition systems. The systems were evaluated both for IC (<15 μm) and power device (to 100 μm) wafers. Of the 150 variables in the model, 100 are input parameters. These include the times, utilities, and consumable items per run; capital, floor space, and inventory requirements; maintenance and etching times and costs; operator, shift, and efficiency parameters; and wafers per run for each size. The program then calculates the desired results, including throughput, total variable and capital costs per wafer, per run, and per year and also provides depreciated or after-tax costs if desired.

Reports may be generated to display any desired subset of the output (and input) variables, with labeling and in any format. Bar charts or probability distribution histograms are also available. In addition, the model may be modified or the input data altered by use of WHAT IF and other command statements. These interactive changes are reflected in subsequent output during the run, but need not be made permanent unless desired.

The data items included in this computer model are listed in Table 4. The percent of the total run cost for each variable cost item is shown in Table 5. The cost analysis is for the deposition of a 7-μm-thick film on a 100-mm substrate in the AMC-7800 AX reactor. It is interesting to note that the two largest cost items are power and labor. In this analysis it is assumed that one operator is responsible for one machine, which is clearly not the usual case in a production environment. This is, however, the simplest assumption for comparative cost estimates. With this format, the reader can readily adjust the costs for a specific case.

The variable costs involved in depositing 7-, 40-, and 100-μm-thick epi in the AMC-7900, Gemini I, and Gemini II systems are summarized in Table 6. To facilitate comparison of the costs, the values have been normalized, taking as unity the cost of deposition of a 7-μm deposit in the AMC-7900 AX, assuming 90% uptime. It can be seen that the variable costs are the lowest in the Gemini II reactor. For the deposition of 7-μm-thick deposits (on 100-mm sub-

Table 4—Data Items for Cost Analysis

Process Parameters
- Run Times
- Deposition Thickness
- Etch Frequency

Power and Chemical Input
- Nitrogen
- Hydrogen
- Deposition Gases
- HCl
- Dopant Gases
- Power

Power and Chemical Costs
- Nitrogen
- Hydrogen
- Deposition Gases
- HCl
- Dopant Gases
- Power

Equipment Cost
- Reactor
- Options
- Pump
- Generator
- Heat Exchanger
- Transformer
- Installation
- On Shelf Inventory

Floor Space and Cost
- Reactor
- Pump
- Generator
- Heat Exchanger
- Transformer

Replaceable Components Life and Cost
- IR Lamps
- RF Coil
- Bell Jar
- Susceptor
- Other Quartzware

Inventory and Maintenance
- Pump Oil Cost
- Filter Cost
- O-Ring Cost
- Quartzware Cleaning Interval
- Pump Maintenance Interval
- Maintenance Time Cost
- Scheduled Maintenance Time

Uptime and Work Hours
- Operator Efficiency
- Machine Uptime
- Hours/Shift
- Shifts/Day
- Days/Week
- Operator Cost Per Hour

Throughput vs Wafer Size
- 3-Inch Wafers Per Run
- 100-mm Wafers Per Run
- 125-mm Wafers Per Run

Table 5—The Percent of the Total Run Cost of Each Variable Cost Item Associated With a Typical AMC-7900 Deposition Run

Item	Cost (%)
Labor	23.44
Replaceable Components	
Bell Jar	1.69
Radiometer Sheath	2.51
Purge Baffle	1.56
Quartz Hanger	0.78
Cover Ring	0.44
Susceptor	11.15
IR Lamps	6.28
Utilities and Gases	
Power	24.46
H_2	7
N_2	0.09
$SiCl_4$	5.65
HCl	0.02
Dopant	1.04
Etching	4.31
Maintenance	
Labor	3.58
O Rings	2.34
Pump Oil	0.66
Total Per Run	100
Wafer 100 Per Run	24
Total Per Wafer	4.17

Conditions

- 7-μm-thick deposit
- 100-mm substrate
- 0.5-μm/min deposition rate
- Atmospheric pressure deposition
- $SiCl_4$ source gas
- 90% machine uptime
- One operator per machine

strates), the variable costs in the AMC-7900 AX are ~5% more than in the Gemini II. Deposition in the Gemini I reactor system is considerably more expensive than in either the Gemini II or the AMC-7900 AX reactors. The price differentials increase with increasing deposit thickness.

7. Experimental Reactor Systems

In the early part of this paper we described the configurations and operating characteristics of commercially available reactor systems. In this section we briefly discuss configurations that have been considered for further development and experimental systems not commercially available.

Table 6—A Summary of Relative Epitaxial Deposition Costs in the Gemini and AMC-7800 Reactor Systems

Reactor	Deposit Thickness (μm)	Normalized Variable Cost on 100-mm Substrate*	
		75% Uptime	90% Uptime
Gemini I	7		1.60
(Double	40		3.68
Chamber)	100		7.54
Gemini II	7		0.85
(Double	40		1.98
Chamber)	100		4.09
AMC-7800 AX	7	1.07	1
	40	2.49	2.36
	100	5.12	4.93

* With reference to 7-μm-thick epi in the AMC-9800 reactor, 90% uptime. Deposition conditions: $SiCl_4$, 760 Torr, 1 μm/min.

From the standpoint of both throughput and thermal conditions, it would be clearly desirable to develop the capability to deposit epitaxial silicon in the hot-walled reactor configuration now commonly being employed for the low-pressure chemical vapor deposition (LPCVD) of non-single-crystal silicon, oxides, and nitrides. The fundamental problem here has been, and continues to be, the suppression of homogeneous gas phase reactions at temperatures now required for epitaxial growth. To achieve deposits of the required homogeneity in this configuration, it will be necessary to carry out the depositions at well under 900°C where reactions at the substrate surface, rather than homogeneous gas-phase reactions, dominate. Another key issue here is the removal of the oxide from the wafer surface at the low deposition temperatures. To date, it has been necessary to sacrifice crystalline quality in silicon deposited from any source at temperatures less than 900°C in other than ultra-high vacuum systems. Deposition rates at the lower temperatures are also a problem, and therefore the development of this technology is directed toward device configurations that can be built in very thin silicon deposits.

Large loads are accommodated in modest reactor volumes in the rotary-disc cold-walled epitaxial reactor.[34] In this configuration, the silicon wafers are positioned on both sides of individual susceptors. The disc susceptors are then stacked axially and heated by rf. The gas is introduced through a distributor tube that directs the nutrient gases into the openings between the wafer surfaces. The rotary disc configuration is attractive from the standpoint of throughput. It could be a very economical approach and, therefore,

has been analyzed in detail for solar-cell applications. A key concern has been the ability to control the uniformity of the deposit with the substrates relatively closely spaced. Good control has been achieved, however, through manipulation of the gas inlets. The current problem with this reactor is the suppression of the thermal gradients in the plane of the substrates. As we have discussed previously, the radial thermal gradients are the origin of slip in the substrates.

An approach that avoids challenge of fundamentals is the continuous reactor in which wafers flow in and out of gas locks. This is feasible in the situation where thin films are desired, as is the case for MOS transistor applications. This approach can be used with either rf or radiant heating, with a good deal of flexibility in susceptor design and wafer positioning. It also offers a key advantage in that cassette-to-cassette loading and unloading can be readily facilitated. While there are no fundamental limitations here, we feel that a good deal of innovative engineering will be required to make this a commonly employed reactor configuration.

8. Summary

The focus in current reactor technology is on the choice between the radiant-heated barrel and the rf-heated vertical configurations. Of the capabilities available, for any one specific device application, one may face a limiting factor that dominates this choice. Until recently it has been necessary to select the radiant-heated configuration if slip in the epitaxial deposit significantly impacts device performance and processing yield in the application of concern. The outstanding feature of the radiant-heated reactor has been the very good control of slip. Now good progress is being made in slip control in the rf-heated vertical reactors through susceptor design. The amount of slip has been dramatically decreased, but it has proven to be difficult to achieve, at least at the higher deposition temperatures ($\geqslant$1200°C), the complete reduction of slip in the vertical reactors that have been reported in the rf heated horizontal reactor configuration.[22]

The difficulty of achieving reproducibility with the current approach to the susceptor recess design can be attributed to the combination of two factors: small changes in the recess dimensions have significant impact on slip control, and the shape of a curved (dished) substrate, at the deposition temperature, is a function of both the susceptor design and substrate variables. Clearly the critical dimension in the use of recesses in the susceptor is the distance from

the bottom of the wafer to the bottom of the recess. As the shape of the stressed substrate changes with material properties, this dimension will change. This must be considered in the susceptor design. An important materials variable is the oxygen content as related to internal gettering. As the spacings of IC components are decreased, the use of internally gettered substrates is becoming more common in the industry. Internal gettering provides an additional degree of control over the impact of impurities (unintentionally introduced during processing) on the crystalline structure of the silicon (see, for instance, a recent review[32]). The degree to which stresses are developed and tolerated in the crystal during the thermal cycling through thermal gradients involved in epitaxial growth is a strong function of the internally gettered process. Development of slip control in the vertical reactor is being carried out both by the manufacturers of the equipment and by the users. More specifically, development is being carried out by users who are intimately familiar with the internal gettering technology.

Now efforts are in progress to apply the recessed susceptor technology to slip control in the rf-heated barrel reactors. It is possible that the designs already developed are directly applicable to the barrel geometry, but this is still to be established.

Development of the reduced-pressure epitaxial growth technology is also being carried out by both the manufacturers of the equipment and the users. To date there has been less emphasis on reduced-pressure operation than on slip control. The impact of reduced-pressure operation has been more clearly demonstrated in the radiant-heated reactor than in the rf-heated vertical reactor, again based on nonproprietary information available as of the writing of this paper.

The deposition pressure may prove to be a variable in the suppression of slip through susceptor design in the rf-heated reactors. As the processes of the transfer of thermal energy from the susceptor to substrate change with decreasing pressure, it may be necessary to alter the susceptor design. On the other hand, at reduced deposition pressures it is not necessary to employ high deposition temperatures to control the pattern distortion. Slip control is considerably easier at the reduced deposition temperatures.

Aside from the factors discussed above, which directly impact the quality of the epitaxial deposits, the key issues are ease of maintenance, throughput, and cost. From an operator's point of view, the radiant-heated barrel and vertical reactors are very similar. From a maintenance point of view, the radiant-heated reactor is considerably more complex than the vertical geometry. Many of the hard-

ware-related maintenance problems that originally plagued the radiant-heated reactor have been solved. The remaining feature to be improved is suppression of the coating on the inner surfaces of the bell jar. The buildup of this coating during deposition is the dominant factor in determining the number of epitaxial runs that can be made prior to removal of the bell jar for cleaning. Due to the more efficient loading on a barrel as compared to a pancake-shaped susceptor, deposits produced in the AMC-7900 have been significantly less expensive than in the Gemini I. Now that the load of the Gemini II has been made similar to the barrel, the cost differences have decreased to less than 10%, with the Gemini II being the less expensive reactor to operate. Under these circumstances cost will be a secondary factor as compared to the other issues discussed above.

9. A Look at the Future

We anticipate that the emphasis will continue on crystalline perfection for applications in closely spaced integrated circuits. With the exception of specialized non-IC applications, it will not be feasible to make compromises in crystalline perfection for ease of reactor operation, to maximize throughput, or to operate at low temperatures.

The next "generation" of epitaxial reactors will be improved versions of the radiant- and rf-heated barrel and the rf-heated vertical reactor systems. There is real room for improvement in all of these systems. In the near future more will be gained from making these systems simpler and more reliable than from focusing on reactors that can be facilitated with automatic wafer handling.

Related to the above issue, it is essential that the trend toward increasing system complexity cease. Significant effort is now, and will continue to be, put on simplifying both gas manipulation and automated control systems.

The advantages associated with reduced-pressure epitaxial growth will be more appreciated, and reduced-pressure epitaxy will be more commonly employed. Lower deposition temperatures will be used in conjunction with reduced pressures. Through optimization of the pumping systems, maintenance related to reduced pressure epitaxy will not be a major consideration in the future. To be commonly accepted in the industry, the equipment must have a well-working reduced-pressure capability.

With the "customizing" of silicon for specific device applications and the more common use of internally gettered silicon, it will be

more necessary to take into consideration materials variables in the development of epitaxial growth processes. Particularly with regard to the control of crystallinity, the processes employed may prove to be strongly dependent on the silicon properties.

Emphasis will be put on epitaxial systems that can be automated as applications involving epitaxial deposits continue to expand, as, for instance, into MOS technology. Other priorities (as mentioned above) will, however, come before automated handling.

There will be a continuing trend toward the use of lower deposition temperatures to control slip and dopant diffusion in the solid. In applications where it is necessary, pattern distortion and gas phase autodoping (more of a problem at the lower temperatures) will be controlled by other means. In the next generation of reactor systems we anticipate that the emphasis will be placed on deposition temperatures above ~1000°C. Deposition temperatures significantly below ~1000°C will require further development in epitaxy technology, and will have greater impact only after procedures have been put in place to reduce the device processing temperature to well under 1000°C.

Acknowledgment

The authors wish to recognize the many informative discussions with S. Berkman on the fundamentals of the various reactor technologies. We also wish to recognize the participation of U. Roundtree, both in the general development of perspectives in the reactor technologies and more specifically for assistance in the development of meaningful throughput values. S. Hong and J. Maleyeff were very involved in the cost analysis, and their participation is appreciated.

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On a Relationship Between Substrate Perfection and Stacking Faults in Homoepitaxial Silicon

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Abstract—Imperfections and defects in silicon substrates used for homoepitaxial devices can be sources for the nucleation of stacking faults at the epi layer-substrate interface. These faults can be electrically active and degrade device performance. In addition to dislocations and impurity atoms, damaged layers on the substrate are also possible sources. Such damage can arise from the mechanical polishing processes for preparing the substrate and from ion implantation. Ion implantation is now used routinely for the formation of buried layers in several types of silicon bipolar device wafers. An evaluation of residual substrate damage resulting from ion implantation and its effect on epitaxial layers has been made.

Chemical etching has been used to reveal the damage in patterned device wafers prior to epitaxy. Using Nomarski microscopy, we have compared these samples with similarly etched epitaxial layers on companion wafers. Stacking faults in the epi layers have been correlated with etch pit formation in the buried layer pockets. The results show that residual damage and stacking fault formation are related.

1. Introduction

Imperfections, defects, and impurity atoms in silicon substrates used for devices fabricated in homoepitaxial silicon can be sources for the nucleation of stacking faults (SF) in epitaxial layers. These faults are believed to be widespread in silicon crystals and devices[1,2] and consist of two types—epitaxial and oxygen induced. More will be said about these later. As with other defects, these faults can be electrically active and degrade device performance.[2,3] In addition to grown-

in crystallographic defects, damaged layers on the substrate are also possible sources for stacking faults. Such damage can arise from the mechanical polishing processes used to prepare the substrate for device fabrication[1,4] and from ion implantation methods.[5,6] The latter method is now used routinely at the RCA facility at Findlay, Ohio, for the formation of Sb and As doped buried layers in several types of bipolar device wafers.

Ion implantation produces uniform, selectively doped regions in the silicon substrate. The implantation, however, is but one step in the formation of the patterned substrate. Other processes involve thermal oxidation to provide a masking layer and photolithography to define the regions to be etched and implanted. The buried layer is subjected to a high-temperature drive-in, and the wafer is annealed to eliminate damage from the implantation process, thereby reducing defect density and promoting the incorporation of the implanted dopant atoms at electrically active lattice sites.[2]

The importance of the annealing procedures and the variables involved have been pointed out by several authors. For example, S. Prussin[5] describes the effectiveness of a two-step annealing process in reducing ion-implant damage, and V. C. Kannan and D. D. Casey[7] also report that for implanted As, a two-step annealing procedure is more effective than a single-step process in reducing defect densities.

It was mentioned earlier that two classes of stacking faults are found—epitaxial and oxygen induced. Epitaxial SF nucleate at the epilayer-substrate interface and propagate into the epitaxial layers. Their formation depends on substrate surface and crystallographic quality, the presence of impurities, and the epitaxial deposition conditions.[2] The formation of oxygen-induced SF, as the name implies, occurs during oxidation steps. Prussin[5] reports that defects from surface damage interact with oxygen to generate SF. The influence of other process variables, including oxidation temperatures and cooling rates, has been discussed by Rohatgi and Rai-Choudhury.[8] McD. Robinson et al.[9] have reported the effects of buried-layer drive-in temperatures and crystal misorientation on oxygen SF formation. (For other details, see Refs. 2 and 10.)

The experimental results reported here provide a qualitative description of etch pit patterns in pre-epitaxial, ion-implanted Sb and As buried-layer device wafers and corresponding stacking faults in epitaxial layers deposited under several different conditions on such wafers.

This study was carried out at a time when we were observing problems in the control of defects in the epitaxial silicon prepared

at the RCA Laboratories for exploratory applications in the bipolar technology. The objective was to identify the source of the defects, particularly with respect to substrate conditions or epitaxial growth conditions. While the problem was specific rather than general in nature, we feel that the results are of interest and generally applicable in epitaxial silicon technology. The study is useful in that a source of epitaxial defects is identified that can be alleviated with the appropriate control.

2. Experimental

The three-inch substrates used for the devices were (100) oriented, 4–11 Ω cm, boron-doped to 10^{15}–10^{14} atoms/cm^3 from several suppliers. Randomly selected samples from several lots of the starting substrates were Wright-etched[11] and examined for defects. Most surfaces had no etch features, but occasionally a few stacking faults and dislocations were observed.

Wafer processing, up to the deposition of epitaxial layers, was performed by personnel at the RCA facility at Findlay. These steps included oxidation, device patterning, Sb or As ion implantation, and subsequent drive-in and annealing. The annealing procedure required 22 hours in several different atmospheres using carefully ramped temperature schedules.

3. Epitaxial Deposition

Epitaxial layers were deposited in an Applied Materials, Radiant Heated Barrel (RHB) reactor, Model AMC 7900.* Deposition conditions, epilayer thicknesses and ion-implant data are given in Table 1. Representative wafers were selected for examination from the several epitaxial runs, each of which included about twenty wafers.

Several pre-epitaxial device wafers from each lot of about twenty were retained for comparison with the epi runs. All or most of the epitaxial wafers were examined for as-grown characteristics, defects, blemishes, etc., using a Nikon Optiphot microscope with Nomarski interference contrast optics. One or two representative epitaxial samples were retained while the rest were processed for devices. One half of each selected wafer was then Wright-etched[11] and examined for defects by Nomarski microscopy.

* The epitaxial growth was carried out by J. F. Corboy and R. Pagliaro, Jr. at RCA Laboratories.

Table 1—Wafer and Epitaxial Processing Data

Type	Implant Dose/cm² at 80 keV	Epi Process	Epi Layer Thickness (μm)
As	As − 4 × 10^{15}	X ; Y	3.5
A	Sb − 1.5 × 10^{15}	X ; Y	7
B	Sb − 2.3 × 10^{15}	X ; Y	14
C	Sb − 4.8 × 10^{15}	X ; Y	14

X = $SiCl_4$/760 Torr/1190°C
Y = $SiCl_4$/100 Torr/1150°C

4. Experimental Results

Table 1 shows the different substrates that were examined, one with As implanted and three with different dose levels of Sb-implanted buried layers (BL). Each of them received epitaxial layers of appropriate thickness using a high-temperature (HT) and a low-temperature (LT) deposition process. The various substrates and processes have similarities and differences that are described below.

5. As-Implanted Buried Layers

The As-implanted buried layers illustrate a recurring similarity shared by all of the implanted samples. Figs. 1(a) and (b) show the center and edge, respectively, of a Wright-etched, pre-epitaxial wafer. Etch pits can be seen in the BL of Fig. 1(b), edge, but not in Fig. 1(a), center. Figs. 1(c), (d), and (e) show Wright-etched corresponding sections of a high-temperature epitaxial layer on a companion wafer. It is clearly evident that the chemical etch did not reveal any stacking faults in the center region [Fig. 1(c)] consistent with the absence of etch pits in the pre-epitaxial sample [Fig. 1(b)].

On the other hand, Figs. 1(d) and (e) show stacking faults in the epi over the buried layer of the edge region, corresponding to the etch pits in the pre-epitaxial wafer [Fig. 1(b)].

Low-temperature epitaxial layers were also deposited on the same type of wafers, and again, etch pits are found in edge regions of the pre-epitaxial BL [Fig. 2(b)] and corresponding SF are seen in the companion epi layer, Fig. 2(d). The lower density of etch pits in this pre-epitaxial sample is a variation that occurs among different wafers.

The absence of pre-epi pits and epi SF over the BL in the center

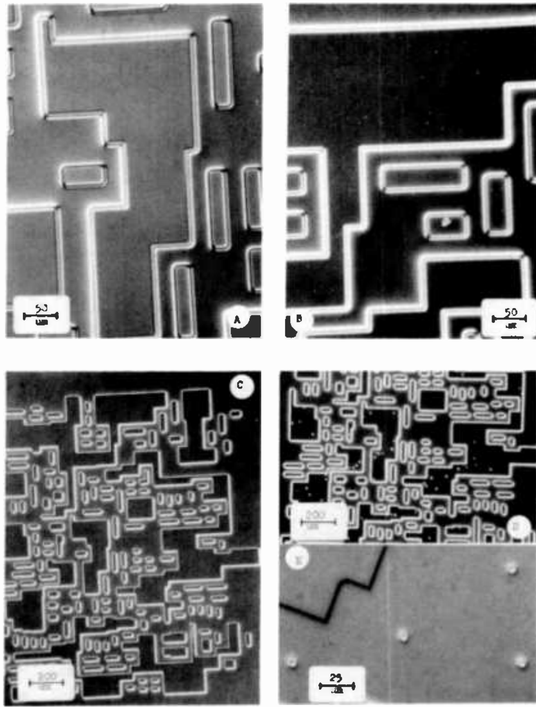

Fig. 1—Wright-etched, As-implanted wafer. Pre-epi—Center (a), edge (b). Epi X—Center (c), edge (d) and (e).

regions is consistent with reports by Katz and Hill[12] and Marcus et al.[13] that nucleation sites for SF are suppressed in BL regions including As implants.[3] Rozgonyi et al.[13] also report that a BL fabricated by ion-implantation did not nucleate epi SF.

The difference between edge regions, where epi SF are found, and center regions, where they are absent, is the recurring similarity between these and Sb-implanted wafers described below.

6. Sb-Implanted Buried Layers

Wafers implanted with Sb were investigated for three implant doses, for high-temperature deposition at atmospheric pressure, and for low-temperature deposition at reduced pressure, as shown in Table 1. They each have similarities and differences, some of which are summarized in Table 2. These and other noteworthy observations are discussed below.

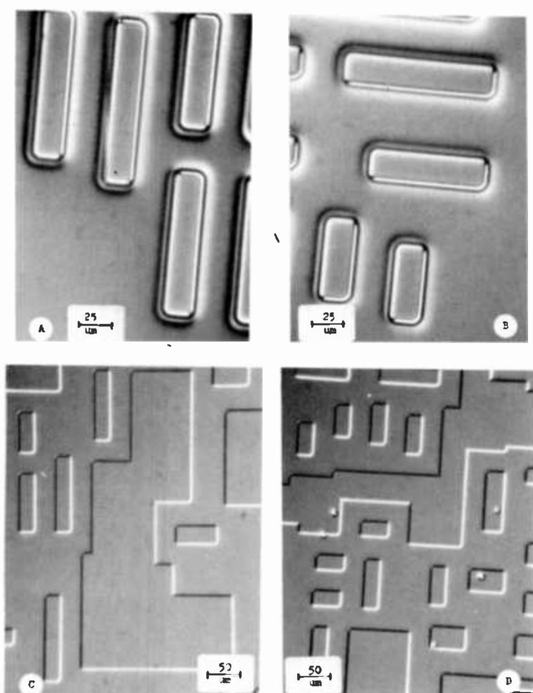

Fig. 2—Wright-etched, As-implanted wafer. Pre-epi—Center (a), edge (b). Epi Y—Edge (c).

7. Type A

The type A wafers received an Sb-implant dose of 1.5×10^{15} atoms/cm^2 in the BL regions. Note that the center regions of the pre-epi wafers [Figs. 3(a) and 4(a)] have very few etch pits, while the edges [Figs. 3(b) and 4(b)] have a high density of pits confined to the BL region. Further, the pre-epi wafer from the lot receiving the LT epi has an appreciably higher etch pit density [Fig. 4(b)].

The center regions [Figs. 3(c) and 4(c)] of wafers from both epi processes have lower SF densities than the edges [Figs. 3(d) and 4(d)]. In Fig. 3(d) it is seen that the SF predominate in the BL regions, but that there are some in non-implanted regions where it is possible that contaminating atoms also nucleated SF. It has been reported by Rozgonyi et al.,[13] for example, that stacking faults, related to the presence of S-pits, can occur in non-BL regions and at the same time be almost absent in BL. Contrary to this, it is noteworthy that in the present case, the higher SF density corresponds

Table 2—Defect Characteristics of Sb-Implanted Wafers

Type	Sample	Sb-Implant Dose (atoms/cm^2)	Center	Fig.	Edge	Fig.
A	Pre-epi	1.5×10^{15}	A few etch pits only in some BL.	3a	Moderate number of etch pits in almost all BL.	3b
	Epi-X		Low SF density mostly in BL.	3c	High SF density in BL, some in non-implanted regions.	3d
A	Pre-epi	1.5×10^{15}	A few etch pits only in some BL.	4a	High etch pit density in *all* BL.	4b
	Epi-Y		Very low SF density mostly in BL.	4c	Low SF density in BL.	4d
B	Pre-epi	2.3×10^{15}	Low etch pit density in BL.	5a	Moderate number of etch pits in *large* BL. High density in *some small* BL.	5b
	Epi-X		Occasional SF in BL.	5c	Low SF density in BL.	5d
B	Pre-epi	2.3×10^{15}	Very low etch pit density in *larger* BL. Moderate etch pit density only in some smaller BL.	6a	Low to moderate etch pit density in *larger* BL. High etch pit density in most smaller BL.	6b
	Epi-Y		Occasional SF in BL.	6c	Low SF density in BL.	6d
C	Pre-epi	4.8×10^{15}	Very low etch pit density in *most* BL.	7a	Moderate etch pit density in *most* BL.	7b
	Epi-X		Almost no defects.	7c	Low SF density in many BL.	7d
C	Pre-epi	4.8×10^{15}	Very low etch pit density in *most* BL.	8a	Moderate etch pit density in *most* BL.	8b
	Epi-Y		Low SF density in BL.	8c	High SF density in BL.	8d

X = $SiCl_4$/760 Torr/1190°C
Y = $SiCl_4$/100 Torr/1150°C

to the formation of etch pits in the BL of companion, pre-epi wafers. Reasons for this will be discussed later.

Another interesting observation is that the SF in the low-temperature epi [Fig. 4(d)] are confined to the BL and have a lower density than in the HT [Figure 3(d)]. On the other hand, the etch pit densities of the pre-epi BL [Figs. 4(b) and 3(b)] are just the reverse. The normal variation among wafers may account for this,

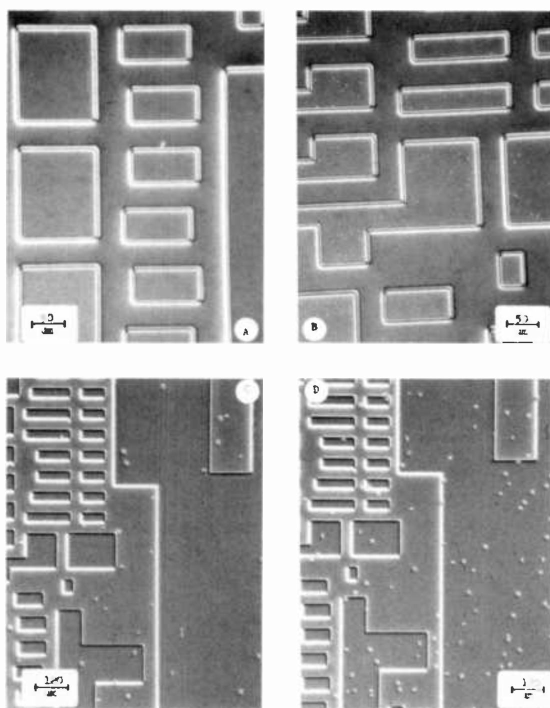

Fig. 3—Wright-etched, Sb-implanted, type A wafer. Pre-epi—Center (a), edge (b). Epi X—Center (c), edge (d).

but if Fig. 4(b) is representative of the wafers in the lot, then this result is preliminary evidence that the LT epi conditions suppressed the epi SF formation in this sample with the lowest Sb-implant dose.

8. Type B

With this intermediate Sb-implant dose (2.5×10^{15} atoms/cm^2), both of the pre-epi and both of the epi wafers are similar. Pre-epi center regions, as shown in Figs. 5(a) and 6(a), have very low etch pit densities in the BL, and there are only a negligible number of SF in the corresponding epi regions [Figs. 5(c) and 6(c)]. The larger BL in the edge regions of the pre-epi wafer, seen in Figs. 5(b) and 6(b), have a moderate etch pit density, and the corresponding epi edge regions [Figs. 5(d) and 6(d)] both have a low SF density confined to the BL.

The intermediate Sb-implant dose did not produce more SF than

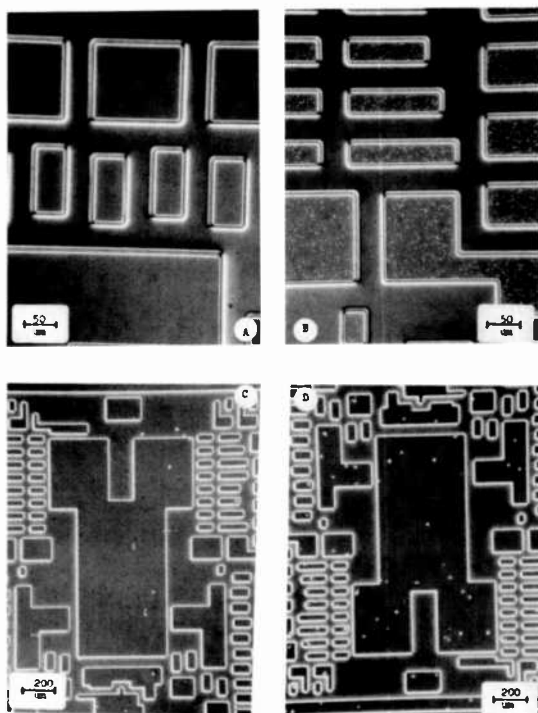

Fig. 4—Wright-etched, Sb-implanted, type A wafer. Pre-epi—Center (a), edge (b). Epi Y—Center (c), edge (d).

the lower dose, but the pre-epi etch pit pattern is different in that smaller BL regions were especially affected. Note, for example, the higher pit densities in Fig. 5(b). They did not, however, nucleate a correspondingly high epi SF density. This will be referred to again later.

There is no apparent effect of epi deposition conditions (HT vs. LT) on the SF formation, and again, SF are found in the BL contrary to the previous report.[13]

9. Type C

In the type C substrates, the BL regions were implanted to a level of 4.8×10^5 atoms/cm^2. Both pre-epi wafers are similar with very low etch pit densities in most BL of the center regions [Figs. 7(a) and 8(a)], and moderate densities at the edges [Figs. 7(b) and 8(b)]. The HT epi wafer has a somewhat lower SF density than the LT

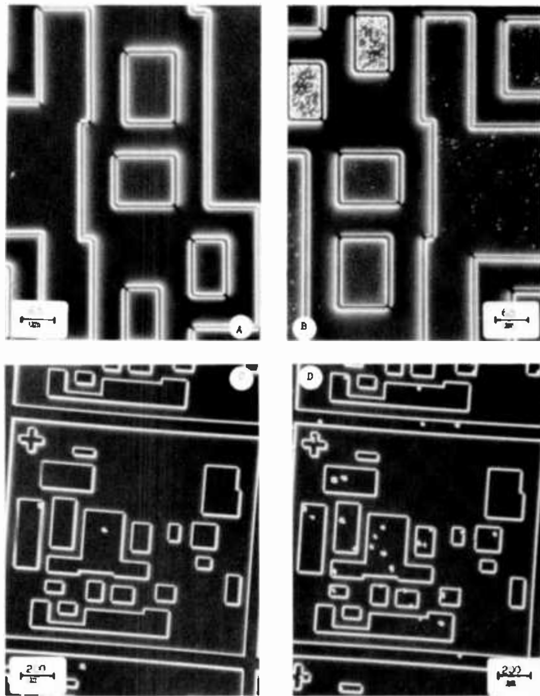

Fig. 5—Wright-etched, Sb-implanted, type B wafer. Pre-epi—Center (a), edge (b). Epi X—Center (c), edge (d).

[Figs. 7(c) and 8(d)], but this set of wafers does not establish either the epi process or the density of BL nucleation sites as the cause.

The higher SF densities at the edges are confined to the BL, suggesting that they result from the nucleation sites and not from spurious contamination. Recall that contamination accounted for some of the epi SF in the sample shown in Fig. 3. Excluding that sample, then, the present Type C, with the highest Sb-implant dose, has a higher SF density than Type B with the intermediate dose. This suggests a dependence of defect density on implant dose.

10. Discussion

Differences between edge and center regions of wafers can occur for several reasons. Others have reported, for example, that edge rounding causes anomalies and that the handling of wafers at the edge can introduce contaminants that nucleate stacking faults.[14] This can affect a region extending inward about 3 mm from the edge. In the present case, however, the affected regions may extend

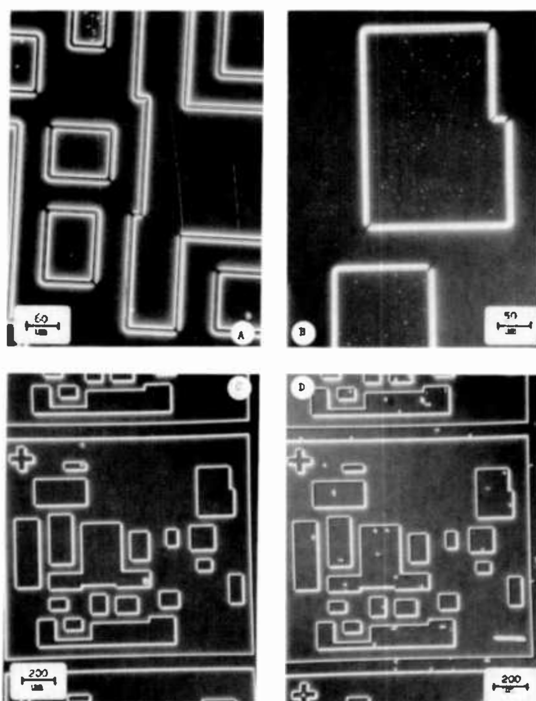

Fig. 6—Wright-etched, Sb-implanted, type B wafer. Pre-epi—Center (a), edge (b). Epi Y—Center (c), edge (d).

for about 12 mm, and we believe, therefore, that the primary cause is related to the ion implants.

Most of the epi SF nucleate in the BL at sites that can be revealed by etch pits. These sites are more numerous at the edges and account for the higher SF density there. The nucleating sites result from residual ion-implant damage in the BL.[5,6] The excessive edge damage that survives the annealing process can occur from a temperature difference between the centers and edges during the implant process.[15] It has been pointed out, for example, that the substrate temperature during implantation affects lattice disorder and diffusion of defects.[16] Further, the quality of epi layers over As implants was found to be sensitive to implant temperatures as well as to the dose.[17]

As mentioned earlier, Rozgonyi et al.[13] reported that their ion-implanted buried layers did not nucleate stacking faults. With diffused BL, SF only appeared in non-diffused regions and were attributed to S-pits. These authors also observed that only a small percentage of defects acted as nuclei for epi SF, and they speculated

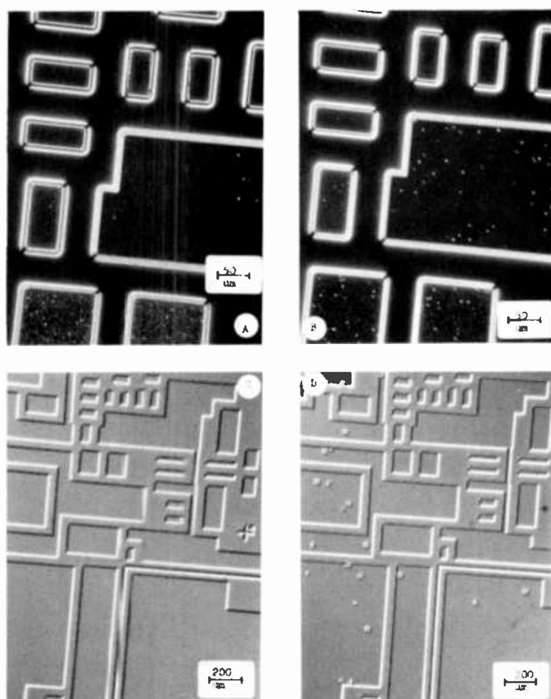

Fig. 7—Wright-etched, Sb-implanted, type C wafer. Pre-epi—Center (a), edge (b). Epi X—Center (c), edge (d).

that a colony of defects might be required to nucleate a stacking fault.

In our case, etch pits were identified in the BL of four different types of wafers. The pits varied in size and density, and in some cases, their formation also depended upon the dimensions of the BL regions. These observations show that the defects revealed by the etch patterns are related to the implantation and annealing process. The possibility of such a relationship, even after annealing, was pointed out by Tokuyama et al.[16] In the present wafers the residual defects from the implantation provide the necessary number of nucleation sites for the formation of the observed epi SF over the BL cells, thereby accounting for the difference from the previous report.

11. Conclusions

The experimental results of this investigation have shown that:

- There can be residual damage in the buried layers of As or Sb implanted and annealed Si wafers.

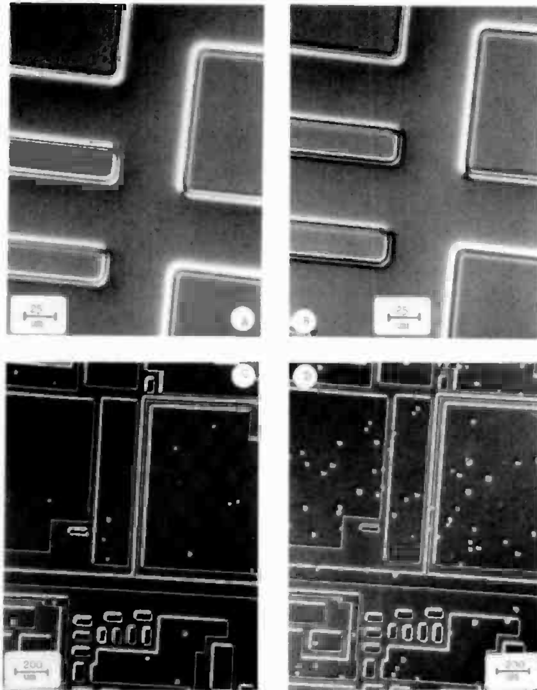

Fig. 8—Wright-etched, Sb-implanted, type C wafer. Pre-epi—Center (a), edge (b). Epi Y—Center (c), edge (d).

- The damage is greater near the edges of the wafers, probably resulting from an edge-to-center temperature difference during implantation.
- The results from wafers with different levels of implant doses suggest that the amount of residual damage is related to the dose level.
- The damage provides sufficient nucleation sites for the formation of epi stacking faults in epitaxial deposits over the buried layers. The density of stacking faults is higher at the edges corresponding to the region with greater damage.
- There is preliminary evidence that the formation of SF is partially suppressed by epi deposition with $SiCl_4$ at 100 Torr and 1150°C.

The conclusions are strongly supported by the repetitive observations relating chemical etch pit patterns in pre-epi buried layers to epi SF among four different types of wafers.

Acknowledgments

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An Investigation of the Factors that Influence the Deposit/Etch Balance in a Radiant-Heated Silicon Epitaxial Reactor

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Abstract—As the physical dimensions of integrated circuits become smaller and the thickness of the active device regions decreases, epitaxial films of a more perfect crystalline quality are required. High-quality epitaxial deposits can be prepared in the commercially available radiant-heated reactor (Applied Materials AMC-7900). Using the radiant-heated configuration, the thermal gradients normal to the substrate can be minimized. Maintenance in this reactor must be carefully programmed to avoid accumulation of deposits on the reactor bell jar which would attenuate the radiant energy. Despite the drawbacks associated with this approach, this reactor is widely used in the semiconductor industry where deposits with good crystalline perfection are required. Little is to be found in the literature, however, on the impact of the variables of total gas flow, location of the substrate on the susceptor, and susceptor rotation on the local deposition/etch rates and uniformity of the deposit resistivity. To develop an understanding of these factors, the reactor was operated in an experimental mode with no susceptor rotation. The results of this study and the implications with respect to operation of the reactor in the normal rotating-susceptor mode are discussed.

1. Introduction

As the physical dimensions of integrated circuits become smaller and the thickness of the active device regions becomes thinner, epitaxial films of a more perfect crystalline quality are required. The radiantly heated epitaxial reactor is capable of supplying high-

quality epitaxial deposits with some sacrifice due to time expended on maintenance. In support of our product divisions, this reactor has been installed and is being characterized in a laboratory environment.

The main thrust of the study reported here is to define the nature of the epitaxial deposits under the condition of no susceptor rotation. One may legitimately ask why this is of interest, under the circumstances that susceptor rotation is required to achieve the desired deposit uniformities. There are, however, a number of reasons why the zero rotation behavior is of interest. The introduction of the nutrient gases in this reactor is very unsymmetrical. The inlet jet geometry results in the formation of a vertical channel of nutrient gas through which the substrates are rotated. As a result, steady-state deposition is never achieved; the deposition rate is continually changing in an oscillatory fashion as the substrates move in and out of the gas channel. We wish to know the limits of the conditions under which the deposit is formed, and assess the impact on deposit properties. Another consequence of the channeling is non-uniform wall deposits. The formation of wall deposits is the central issue in the relatively heavy maintenance that this reactor requires. Thus, a knowledge of the zero-susceptor-rotation conditions is required as a base for optimization of the thermal configuration, rotation rate, gas inlet geometry, and suppression of wall deposits.

The reactor used for this work is the Applied Materials model AMC-7900. The physical configuration of the susceptor, bell jar, lamp modules, etc. is shown in Fig. 1.[1] A schematic cross-sectional view of the same configuration, but with more detail, is shown in Fig. 2.[1] In Fig. 3 a block diagram of the gas flow scheme and electrical interconnections is shown.

2. Assembly Description (Refer to Figs. 1, 2, and 3)

A quartz bell jar is rigidly mounted and is surrounded by five air/water cooled modules of fourteen lamps per module. A silicon carbide coated graphite susceptor, suspended by a quartz hanger that is attached to a steel liftable seal plate, is positioned in the center of the bell jar. Substrate wafers are placed in circular recesses in each face of the susceptor and the susceptor is rotated. A water and nitrogen cooled temperature sensor is inserted through an opening in the steel seal plate down through the quartz hanger and positioned in the center of the susceptor. The temperature sensor has three photodiodes, one for each temperature zone. A seal plate purge gas of approximately 90 liters/min (when H_2 is flowing) flows con-

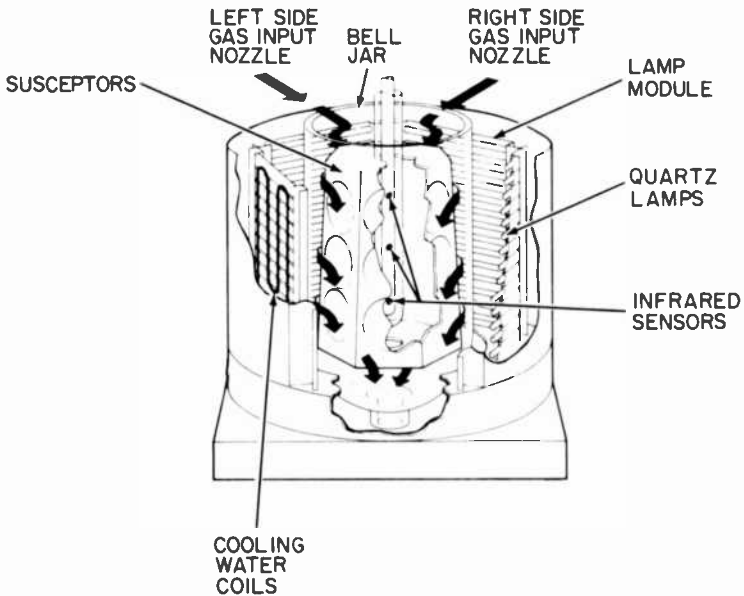


Fig. 1—AMC-7900 cut-away view of epi reaction chamber.

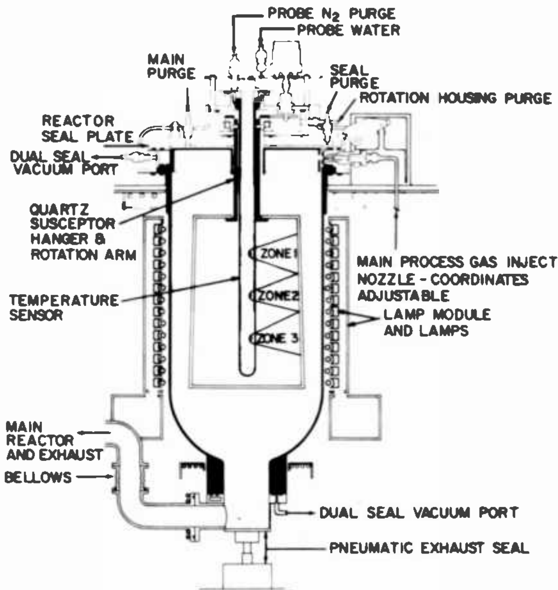


Fig. 2—AMC-7900 schematic view of cross section of the epi reaction chamber.

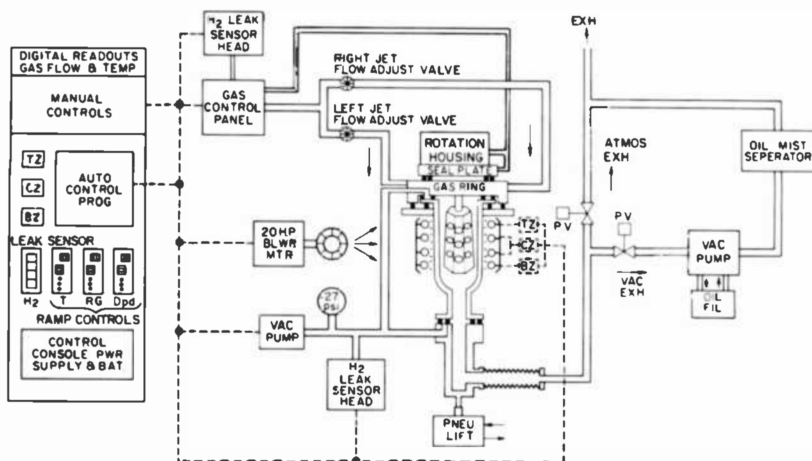


Fig. 3.—Flow diagram of the plumbing and electrical configuration of the AMC-7900 epitaxial reactor.

tinuously inside the seal plate. Approximately one quarter of the flow goes down through the quartz hanger, inside the susceptor, and out through a small hole centered in the bottom plate of the susceptor. The rest flows between the susceptor and the bell jar walls. This flow is not the H_2 main flow. The H_2 main flow is introduced into the reactor via the inject nozzles and flows between the bell jar walls and the susceptor. The vacuum pump, pump oil filter, and pump oil mist separator are mounted in separate cabinetry and remotely located. A separate control console that can be operated in a manual or automatic mode controls all system functions and is also remote from the reactor cabinet. The main gas inject nozzles are located approximately 60° to each side of the back center of the reactor (~120° apart). They face toward each other, and their flows are opposing. The flow down the length of the susceptor is not symmetrical, and in fact, significant channeling occurs. This method of introducing reaction gases into an epi reactor is not traditional and required investigation.

To more easily evaluate the variables that affect the epi parameters of growth rate, etch rate, thickness, and resistivity uniformity, we established a master identification code that described substrate positions on the susceptor and data location points on the substrate; this code is used in describing the results of these experiments (Fig. 4). A computer program[2] was written so that the data could easily be reduced to a manageable format.

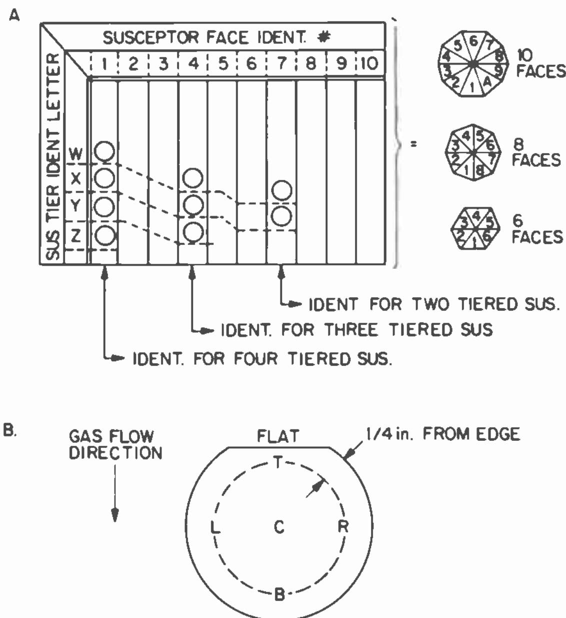


Fig. 4—Master identification code that describes the position of a substrate on the susceptor and the position that the data point was taken on the wafer.

3. Thickness and Resistivity Variations as a Function of Substrate Position with No Susceptor Rotation at Reduced Pressure (100 Torr)

To establish the flow conditions that exist in the reactor it was necessary to conduct experiments where the susceptor was completely loaded with substrates and *not rotated* during etching or deposition.

3.1 Experimental Conditions

A 15¹/4-inch-long 10-faced solid susceptor that holds three 3-inch-diameter wafers per face was used. It was fully loaded for each experiment with thirty (111) antimony doped (3×10^{18} atoms/cm^3) substrates. The main H_2 flow was set to 160 liters/min, the temperature to 1100°C, and the reactor pressure to 100 Torr. SiH_2Cl_2 and diborane were introduced at a controlled rate. The location of the susceptor faces was accurately determined with respect to the nozzle positions. The gas inject nozzles were set to a horizontal po-

sition of 8.5 (+) and a vertical position of 5 (+) (Figs. 2 and 3). Each wafer was then measured at five points for thickness using an infrared spectrometer (Nicolet) and for resistivity using a four-point probe.

3.2 Experimental Results

3.2.1 Thickness

The variation in epi thickness as a function of the wafer position in the reactor is shown in Fig. 5. These values represent a thickness measurement in the center of each wafer. The maximum in the thickness variation is a factor of 2.5. The thickness is from 6.5 to 9.2 μm on the wafers positioned on susceptor faces farthest removed from the inlet nozzles (to the front of the reactor). The thickness is from 14.0 to 16.0 μm on the susceptor faces that are nearest the gas inlet nozzles (at the back of the reactor). The thickness band drawn between 10.4 and 11.6 μm represents the thickness uniformity that is obtained over all data point positions using these growth conditions with susceptor rotation. There are three distinct top to bottom thickness regions as a function of the position in the bell jar (Fig.

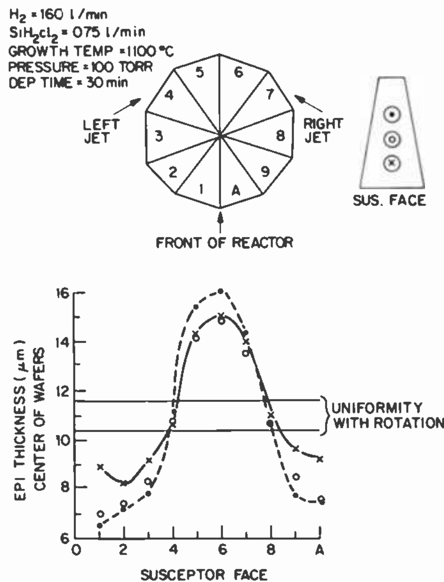


Fig. 5—Epi thickness variation (center of wafers) from the top to the bottom of each susceptor face as a function of the position of the wafer in the reactor (susceptor not rotated during epi deposition).

6). For susceptor faces that were to the front of the reactor (1,2,3,9, and A) the top wafer is the thinnest and the bottom wafer is the thickest. For faces 4 and 8 the top-to-bottom variation is small, and for faces 5, 6, and 7 the thickness variation is reversed: the top wafer is the thickest and the bottom wafer the thinnest. It should be pointed out that the top-to-bottom thickness variation on faces 4 and 8 (±5%) is much less than the thickness variation on the other faces (±11%). The horizontal center-to-edge percent thickness change is similar for all wafer positions (Fig. 7). The above experiment was repeated with H_2 flows of 82 and 190 liters/min. Similar results were observed (Table 1).

3.2.2 Effect of Total Flow on Growth Rate With Susceptor Rotation

The effects of total H_2 flow on growth rate using the experimental conditions described above but with the susceptor rotated at 3 rpm cw are shown in Fig. 8. Also included in this figure is the effect of H_2 main flow when the reactor was operated at 1190°C using $SiCl_4$ at atmospheric pressure. It is evident from this data that the total flow does not significantly affect the growth rate. The impact of the

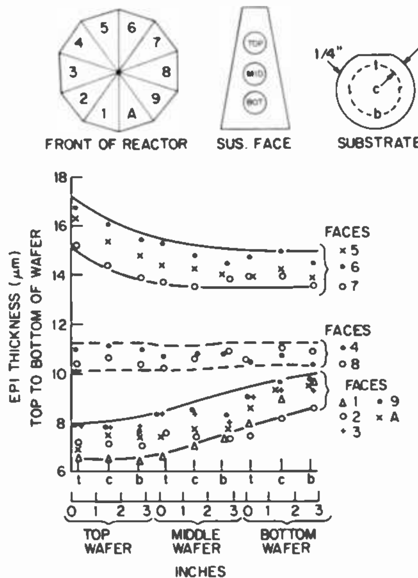
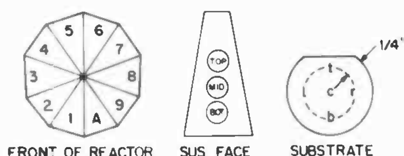


Fig. 6—Epi thickness variation from the top to the bottom of each wafer on each susceptor face as a function of the position of the wafer in the reactor (susceptor not rotated during epi deposition).



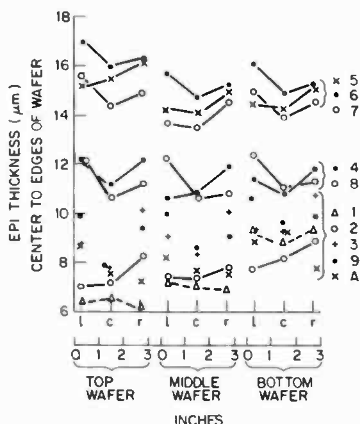


Fig. 7—Epi thickness variation from the center to the left and right edges of each wafer on each susceptor face as a function of the position of the wafer in the reactor (susceptor not rotated during epi deposition).

total flow on bell jar wall deposits and thickness uniformity is another issue that must be considered and will be the subject of another paper.

3.2.3 Resistivity

Resistivity uniformity in this reactor from top to bottom of each susceptor face is very susceptible to the temperature gradient. Trimming of the temperature gradient is the manufacturer's recommended method to optimize resistivity uniformity. The horizontal uniformity from the center to the edges of each wafer is not subject to control and is essentially predetermined by the reactor and susceptor design. In order to investigate resistivity uniformity as a function of the substrate position in the reactor and total flow, the control temperature zone was set to 1100°C, and the top and bottom slave temperature zones were adjusted to the same temperature. A temperature profile as determined with a thermocouple inserted into a face of a slab type test susceptor was used to verify that the temperature sensor circuitry was accurately registering the temperature (Fig. 9).

Table 1—Thickness Variation from the Top to the Bottom of Each Susceptor Face as a Function of H_2 Main Flow (No Susceptor Rotation)

		Minimum Thickness		Maximum Thickness			Thickness Variation Top to Bottom			Growth Rate (μm/min)		
										No Rotation		
H_2 Main (liters/min)	Dep. Time (Min)	Face	μm	Face	μm	Max. T/ Min. T	T < B Face	T = B Face	T > B Face	Min.	Max.	With Rotation
82	26	10	5.7	6	15.8	2.60	1,2,3,9,A	4,7,8	5,6	0.22	0.61	0.37
160	30	1	6.5	6	16.0	2.66	1,2,3,9,A	4,8	5,6,7	0.22	0.53	0.36
160	30	2&9	7.0	5	15.8	2.25	1,2,3,9,A	4,7,8	5,6	0.23	0.53	0.36
190	30	2&9	7.2	5&6	15.8	2.25	1,2,3,4,8,9,A	7	5,6	0.24	0.53	0.36

Susceptor = 10 faced × 15¼ inches high (three 3-inch-diameter wafers/face)
Growth temperature = 1100°C
Pressure = 100 Torr
SiH_2Cl_2 = 0.75 liters/min

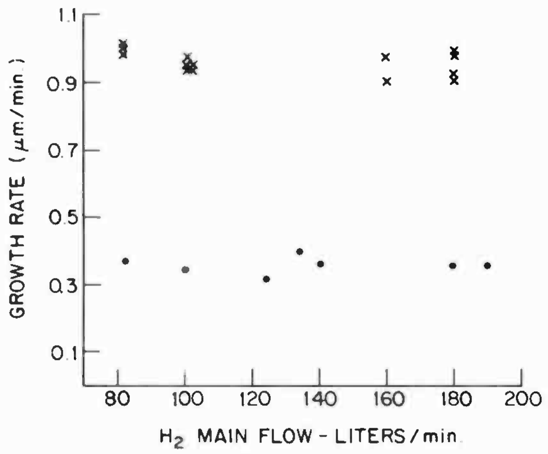


Fig. 8—Growth rate vs. H_2 main flow with susceptor rotated at 3 rpm cw.

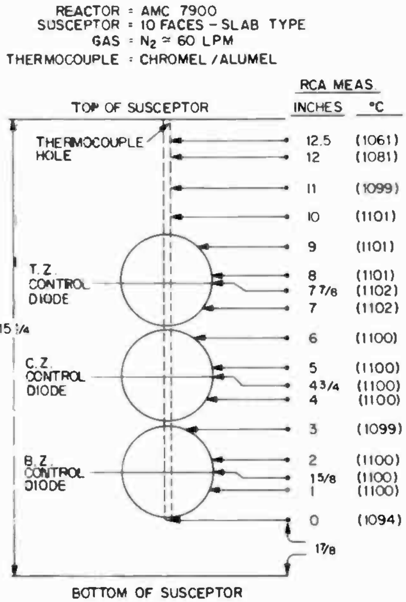


Fig. 9—Temperature profile using a slab type susceptor in the AMC-7900.

The same wafers were used for the resistivity and thickness uniformity studies.

The resistivity values measured at the center of the wafers did not vary by more than ±13% (2.95 to 3.8 Ω cm). The six faces (1, 2, 3, 8, 9, and A) to the front and sides of the reactor showed the largest variation (±13%) while the four faces (4, 5, 6, and 7) to the back of the reactor had the smallest variation (±6%). The magnitude of the resistivity, for all faces, ordered as follows: middle > top > bottom tier (Fig. 10). This is in contrast to the thickness variation profile which was reversed from the front to the back of the reactor (Fig. 5). The susceptor faces that had the least amount of silicon deposition also had the highest resistivities. It is interesting to note that the maximum resistivity variations occur at the same locations in the reactor as the minimum thickness range (front of reactor) and that the maximum resistivity points on the susceptor correspond to the minimum thickness points on the susceptor. The resistivity variation from top to bottom of each susceptor face, as a function of position in the reactor, varies by ±15%. Wafers on the center tier exhibit the highest resistivity, and wafers on the top and

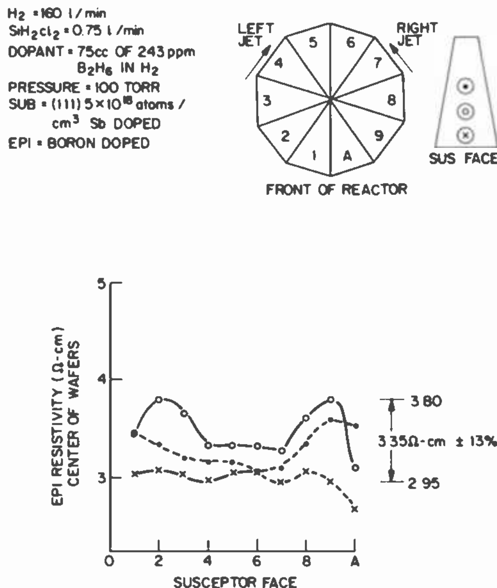
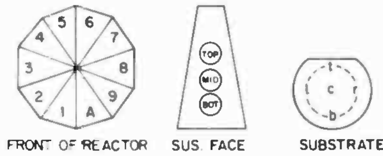


Fig. 10—Epi resistivity variation (center of wafers) from the top to the bottom of each susceptor face as a function of the position of the wafer in the reactor (susceptor not rotated during epi deposition).



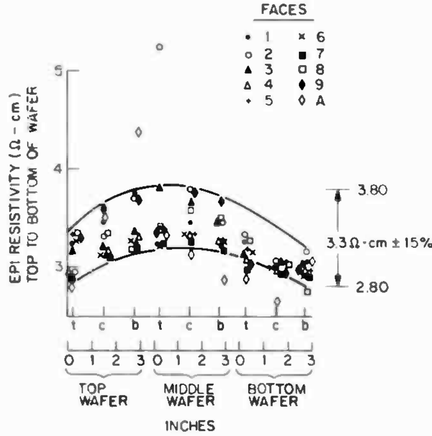


Fig. 11—Epi resistivity variation from the top to the bottom of each wafer on each susceptor face as a function of the position of the wafer in the reactor (susceptor not rotated during deposition).

bottom tiers exhibit lower and approximately equal resistivities (Fig. 11). The center-to-edge variation across each wafer as a function of the position in the reactor is shown in Fig. 12. The total spread is ±15% and has a distribution similar to the top to bottom profile. The resistivity uniformity experiment was repeated with a H_2 flow of 190 liters/min. The results were similar (Table 2).

4. HCl In-Situ Etch Rate Variations as a Function of Substrate Position With No Susceptor Rotation at Atmospheric Pressure

In this investigation we wished to use wafers on which the thickness could be readily determined at the five points of interest. This was accomplished using (111) antimony doped (3×10^{18} atoms/cm^3) silicon substrates with ~20 μm of 1×10^{16} atoms/cm^3 arsenic doped epi. Each wafer was identified and the thickness of the epi was measured and mapped using an IR spectrometer (Nicolet). As was the case for the thickness and resistivity experiments, a 15¼-inch-long ten-faced solid susceptor was loaded with thirty 3-inch-diam-

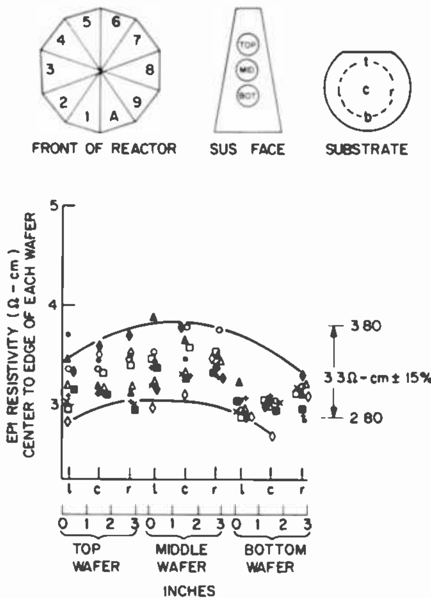


Fig. 12—Epi resistivity variation from the center to the left and right edges of each wafer on each susceptor face as a function of the position of the wafer in the reactor (susceptor not rotated during epi deposition).

eter substrates. The temperature was 1150°C (all zones) and the pressure was atmospheric. The H_2 main flow was 160 liters/min to which 3.2 liters/min of HCl was added (~2%) for a 60-min etch time. The HCl concentration of 2% by volume is a compromise concentration based in part on work done by Lang and Stavish[3] and our own etching experiments. Lang and Stavish demonstrated that the substrate can be selectively etched or polished depending on the etch temperature and HCl concentration. We have studied the etch rate as a function of the HCl concentration in the AMC-7900 reactor (Fig. 13). An HCl concentration of 2% gives the desired uniform etch rate with acceptable surface cosmetics. The 1150°C etch temperature was chosen because it represents a temperature that is compatible with the reactor with regard to the lifetime of lamps, O-rings, etc. and with bipolar (buried layer) device structures. The locations of the susceptor faces were accurately determined with respect to the nozzle positions, and susceptor rotation was not used during this study.

The silicon etch rate in the center of each wafer as a function of the wafer location in the reactor is shown in Fig. 14. The amount

Table 2—Resistivity Variation From Top to Bottom of Each Susceptor Face as a Function of H_2 Main Flow (No Susceptor Rotation)

H_2 Main (liters/min)	Center of Wafers	Top to Bottom of Susceptor Top, Center & Bottom of Wafers	Center to Edges
160	±13% Rows 4,5,6&7 = ±5.5%	±15% Middle wafer = highest Drops off equally for top and bottom wafers.	±15% Middle wafer = highest Drops off equally for top and bottom wafers.
190	±16.7% Rows 4,5,6&7 > ±13%	±17.6% Middle wafer = highest Drops off equally for top and bottom wafers.	±16.6% Middle wafer = highest Drops off equally for top and bottom wafers.
190	±12% Rows 4,5,6&7 = same	±16.7% Middle wafer = highest Drops off equally for top and bottom wafers.	±13.8% Middle wafer = highest Drops off equally for top and bottom wafers.

Susceptor = 10 faces × 15 1/4 inches high (three 3-inch-diameter wafers/face)
Growth temperature = 1100°C
Pressure = 100 Torr
SiH_2Cl_2 = 0.75 liters/min

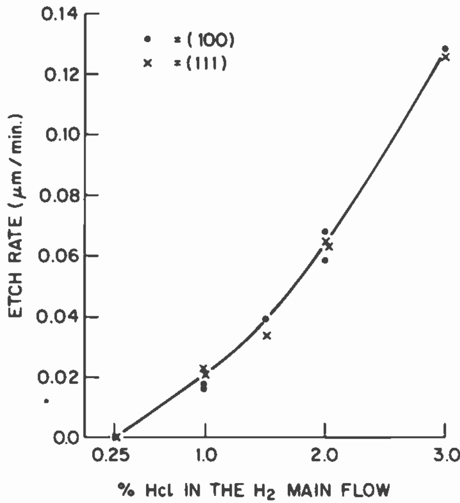
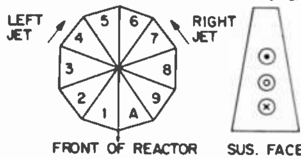


Fig. 13—Etch rate as a function of HCl concentration at atmospheric pressure on (111) and (100) oriented silicon substrates.



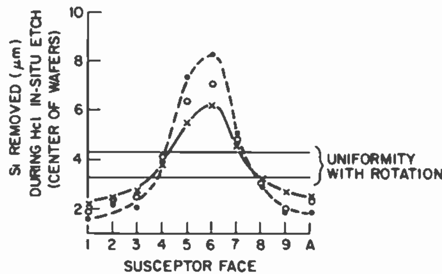


Fig. 14—HCl in-situ etch rate variation (center of wafers) from the top to the bottom of each susceptor face as a function of the position of the wafer in the reactor (susceptor not rotated during epi deposition).

removed varied between 1.6 μm (0.027 μm/min) and 8.3 μm (0.138 μm/min). The removal rate was highest on wafers on the susceptor faces to the rear of the reactor (5 and 6) and lowest on the wafers positioned to the front of the reactor (faces 1, 2, 3, 8, 9, and A). As was the case for thickness, the wafers on susceptor faces to the front of the reactor (1, 2, 3, 8, 9, and A) have the highest etch rate on the bottom tier wafers, and the lowest on the top tier wafers. Faces 4 and 7 have similar values for all three wafer positions, and on faces 5 and 6, the etch rate variation is reversed with the top tier wafer having the highest etch rate and the bottom tier the lowest. The etch rate down the length of each susceptor face at the top, middle, and bottom positions on the wafer on each susceptor tier is relatively uniform. The two exceptions are the top tier wafers on susceptor faces 5 and 6 (Fig. 15). The center to left and right edges have an etch rate pattern that is similar to the top-to-bottom pattern (Fig. 16).

5. Discussion

It is clear from the growth-rate vs. position data that the reaction gases are strongly channeled in the Applied Materials radiantly

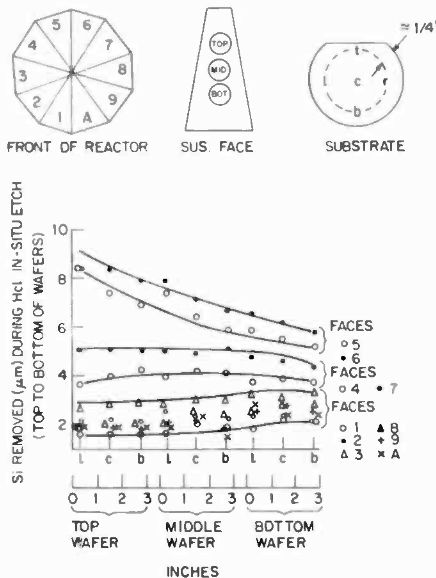


Fig. 15—HCl in-situ etch rate variation from the top to the bottom of each wafer on each susceptor face as a function of the position of the wafer in the reactor (susceptor not rotated).

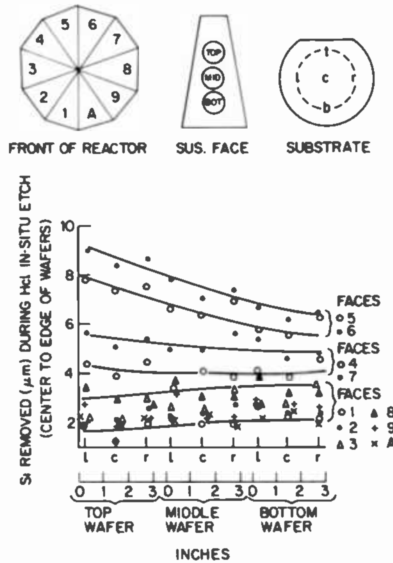


Fig. 16—HCl in-situ etch rate variation from the center to the left and right edges of each wafer on each susceptor face as a function of the position of the wafer in the reactor (susceptor not rotated during epi deposition).

heated barrel reactor. The ratio of the growth-rate change between the thickest epi (susceptor faces 5 and 6) and thinnest epi (susceptor faces 1 and A) is 1.65:1 (minimum) to 2.4:1 (maximum) and occurred on faces 180° apart. The top-to-bottom thickness variation on faces 1, 2, 3, 9, and A is reversed on faces 5, 6, and 7. This leads to the conclusion that as the reaction gases flow toward the front of the reactor, they simultaneously flow downwards, leaving a nutrient-starved region at the top front of the reactor. Experiments conducted with 82, 160, and 190 liters/min of H_2 main flow gave very similar results. Rotating the susceptor averages the growth rate variations such that uniformities of $\pm 8\%$ are easily obtained over all positions on all wafers in a run. Uniformities of $\pm 5\%$ can be obtained when all variables are carefully optimized. The effect of growth rate on epi defects and lateral autodoping has been discussed by Srinivason.[4,5] He has demonstrated that both the defect density and autodoping are affected by growth rate. Since we have demonstrated that the growth rate varies significantly with location in the reactor, it forces one to be alert to the possibility that as the growth rate changes over a wafer with susceptor rotation, the generation of defects and autodoping are constantly changing. The im-

pact of these changes on the deposit characteristics is the topic of current studies.

The resistivity uniformity did not vary by more than ±15% for all data points on all wafers under the condition of zero-susceptor rotation. Within this variation some interesting trends were observed. The maximum resistivity value occurred at the same locations in the reactor as the minimum thickness. This would be expected if the reaction gas concentration is the controlling variable. Typically the middle tier wafer exhibits the highest resistivity and the top and bottom tier wafers the lowest and have similar values. This is not readily explained but must be due to a combination of temperature and gas flow pattern. Fortunately this profile is easily altered by changing the temperature profile. With susceptor rotation and temperature profiling, resistivity uniformities of ±10% over all data points on all wafers are easily obtained, and values of ±6% are obtained when all deposition variables are carefully optimized. In our reactor the maximum resistivity uniformity (arsenic doping) is obtained when the top zone is 10°C lower and the bottom zone is 5°C lower than the center (control) zone temperature.

In-situ HCl etch rates varied by a factor of 5 (between 0.027 μm/min and 0.138 μm/min) depending upon the wafer location in the reactor. As was the case with growth rate, the etch rate variation from top-to-bottom of each face is reversed from front to back of the reactor. The top-to-bottom etch rate on any given susceptor face is reasonably uniform (±13.5%). The exceptions to this occur on the top and middle wafer on faces 5 and 6. When susceptor rotation is used, the etch rate variation is within ±13.5% over all data points on all wafers. The effect that the 5× change in etch rate during each rotation of the susceptor has on the generation of epi defects is not predictable and is currently being investigated.

It must be pointed out that bipolar device structures fabricated on wafers that were prepared in this reactor with HCl in-situ etching have had equal to or higher yields than those obtained from other type reactors. While this study is directed toward a more complete understanding of the processes involved in radiant-heated deposition, we do not want to give the impression that the gas channeling is a major problem in preparing material for current device structures. Good yields have been achieved in bipolar devices fabricated in silicon deposited in the barrel reactor under the normal susceptor rotation conditions. Further control of deposit properties, particularly over heavily doped pockets, is an appropriate goal. However, having achieved epi of adequate quality for current bipolar device structures, the reduction of reactor maintenance is now of equal importance.

Acknowledgment

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Comparison of Different SOI Technologies: Assets and Liabilities

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Abstract—Different methods used to obtain silicon-over-insulator (SOI) films are compared, based on the information available in the literature. All techniques are briefly outlined and their assets and liabilities are compared with special emphasis on application in different present and future processing technologies. It seems that at the present stage of development the "leader" cannot be clearly identified, and different technologies could favor different SOI approaches.

1. Introduction

During the last several years a great amount of interest has been generated in the growth of electronic-quality silicon over insulators (SOI).[1] Attempts have been made over the years to synthesize dielectrically isolated (D.I.) silicon islands to provide flexibility in the fabrication of a variety of integrated circuits. Currently the silicon-on-sapphire technology is being employed to provide dielectrically isolated silicon thin films for CMOS applications in which minority carrier lifetime is not a primary consideration. For bipolar applications, in which lifetime is a primary consideration, the currently employed D.I. process uses a thick polysilicon "handle" to support oxidized and patterned bulk silicon wafers during thinning to the desired configuration.[2] The complexity of the D.I. process and the high cost of sapphire wafers used for the D.I. CMOS technology has hampered the widespread application of the presently available D.I. technology.

A recent increase in interest in D.I. circuits, especially for applications in telecommunications, has led to renewed efforts in developing alternative schemes for the preparation of dielectrically iso-

lated silicon. The short-term objective of these efforts is to provide thin films of dielectrically isolated silicon with acceptable semiconductor properties by methods that are more readily executed and thus less expensive than current processes. An additional short-term objective is to provide an increase of packing density in both MOS and bipolar circuits. The more long-range promise of several of the new SOI approaches is the production of vertically integrated circuits, in which the single-crystal silicon over amorphous insulator (oxide) structure can be repeated more than once in the vertical direction. It has to be emphasized that for application in current state-of-the-art LSI and VLSI circuits, the defect density in silicon synthesized over SiO_2 must be low.[3]

In this paper the various approaches used to obtain SOI films are compared. Special emphasis is placed on selective chemical vapor deposition (CVD), also called ELO (Epitaxial Lateral Overgrowth) or LESS (Local Epitaxial Seeding of Silicon); these CVD approaches have been the focal point of work on SOI carried out at RCA Laboratories.

Each technique is briefly described, and its assets and liabilities are discussed with special emphasis on the near-future applications for production of improved conventional ICs and the potential for making vertically integrated circuits in the distant future.

2. Description of Different Techniques

So far the following techniques have been used to obtain SOI films: deep-oxygen implantation (SIMOX), oxidation of porous silicon (FIPOS), channeled ion implantation followed by solid state regrowth, graphoepitaxy utilizing CVD or melting, seeded or unseeded recrystallization of melted silicon, and ELO/LESS.

The SIMOX technique is schematically presented in Fig. 1. The oxide is formed under the surface of silicon by a high-dose ($\approx 10^{18}$ atoms cm^{-2}) deep-oxygen implantation followed by annealing.[4] Usually 120-keV energy of ion implantation is used. Higher energies spread the implant into a large volume of silicon (larger standard deviation); therefore, an increase of the implantation dose is required to form the oxide layer. Lower energy implant allows one to decrease the implant dose, but unfortunately this puts the oxide layer too close to the surface. Therefore, 120 keV seems to be a reasonable compromise. After annealing, crystallographic quality of the surface layer of silicon (about 0.1 to 0.2 μm thick) is good and very often is used as a seed for growth of an additional few-micron-thick homoepitaxial films. The SIMOX process can be repeated, and

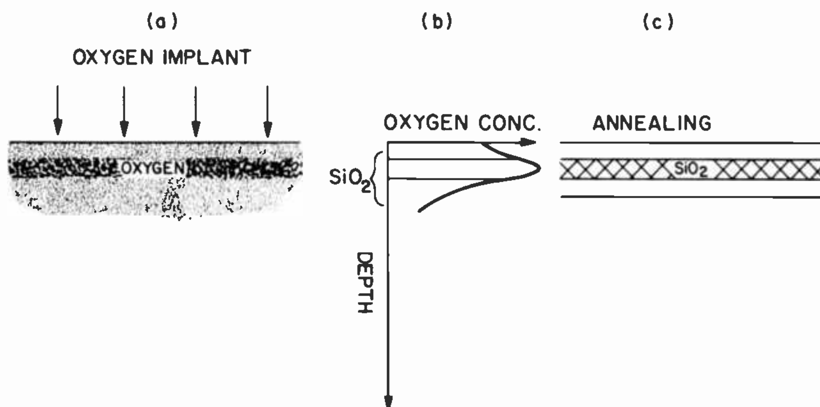

Fig. 1—Schematic representation of SIMOX, (a) oxygen implantation, (b) distribution of oxygen in silicon, and (c) formation of SiO_2 layer after annealing.

the second oxide film can be formed in the homoepitaxial film. A sandwich of a few SOI films made by SIMOX process has been demonstrated.[5] To obtain good crystallographic quality SOI films, the wafer temperature during ion implantation should be kept above 200°C.[5] This technique gives excellent quality silicon films over SiO_2 and has been successfully used for the fabrication of latch-up free 1K CMOS memory circuits[6] and other simpler circuits. The practical drawback of this technique is the high dose of oxygen implant required, which for present implanters takes about 10^4 to 10^3 seconds per wafer.[7] Future optimization of the oxygen-implantation process and application of high-current implanters could possibly reduce this time, although it is not clear if power dissipation during the ion-implantation process will become an insurmountable obstacle in reducing the time of implantation.

SIMOX is a method by which an oxide is formed under a silicon surface. Because an SOI film is synthesized by forming an oxide under silicon, it is difficult to imagine a processing scheme in which one transistor can be made on the top of the other by this method. Therefore, it is the author's belief that this technique cannot be used for fabrication of vertically integrated circuits.

The process used to form SOI films by oxidation of a porous silicon is shown schematically in Fig. 2. First, layers of various resistivities are formed by conventional processing (diffusions, ion implantations, or epitaxial growth). Subsequently, the silicon is electrochemically etched[8] to form porous silicon. Only the p^+ layer is etched when n is not attacked by solution. The oxidation rates of porous

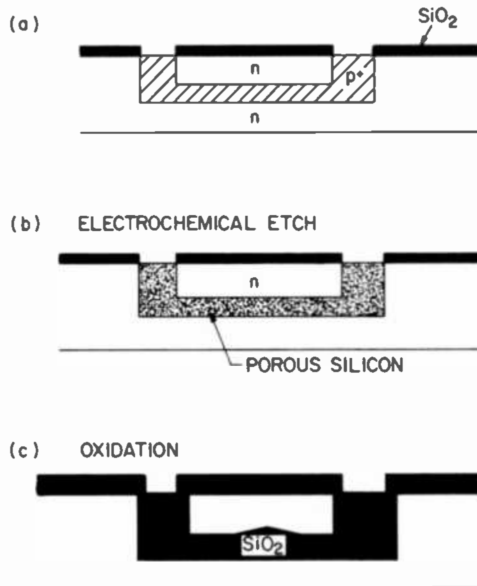

Fig. 2—Schematic representation of FIPOS process, (a) structure used for electrochemical etching (etch rate of n and p regions is different), (b) formation of porous silicon, and (c) oxidation of porous silicon forms SiO_2.

silicon and monocrystalline silicon differ by an order of magnitude;[8] therefore, during oxidation, oxide is formed underneath silicon islands. The structures have to be carefully designed to prevent dislocation generation in the silicon islands by stress from the oxide layers. After the process optimization, defect-free silicon islands 50 μm wide, a few millimeters long, and about 4 μm thick were obtained.[8] This material has been used for fabrication of LSI circuits: 16-bit microprocessor.[9] The practical drawback of this approach is the electrochemical etching necessary for porous silicon formation, a procedure not compatible with other IC fabrication steps. Because oxide is formed under silicon, it is difficult to imagine a processing scheme in which one transistor can be made on the top of the other by this technique. Therefore, as in the case of SIMOX, this technique cannot be used for fabrication of vertically integrated circuits.

During partial amorphization by ion implantation and solid-state regrowth, the process starts with deposition of polycrystalline silicon over SiO_2 (Fig. 3). Then the film is implanted with silicon. A channeled silicon ion beam amorphousizes most of the polysilicon layer leaving intact grains with major crystallographic axes that

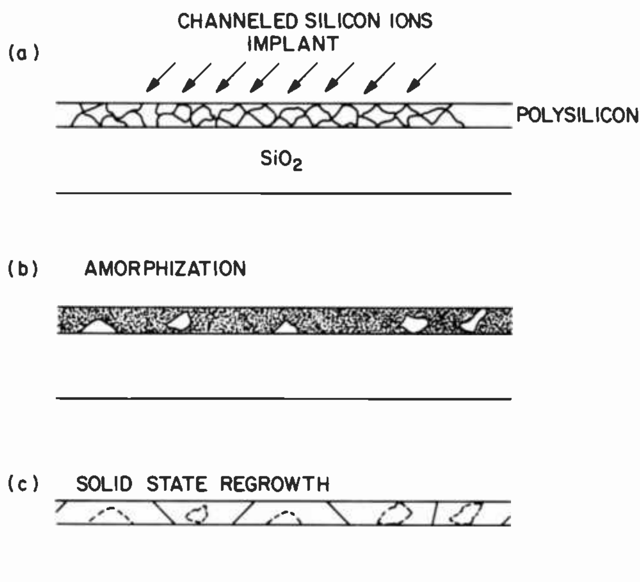

Fig. 3—Schematic representation of partial amorphization by silicon implantation and solid-state regrowth, (a) implantation with a channeled silicon beam, (b) grains with crystallographic orientation aligned along the beam direction do not become amorphousized by implantation, and (c) crystalline grains are used as seeds during subsequent solid-state regrowth.

are aligned along the channeling direction. These grains are used as seeds for solid-state regrowth, which takes place during a subsequent heat treatment. So far, it has been demonstrated that the size of polysilicon grains can be increased by this technique[10] although monocrystalline films or polycrystalline films with a grain size large enough for device application have not been obtained yet by this method. It is not clear if a channeled ion implantation will leave intact grains of only one orientation, a necessary condition for obtaining a monocrystalline film during solid-state regrowth.

Graphoepitaxy relies on inducing a crystallographic structure in a silicon film deposited on an amorphous substrate by providing a pattern relief structure in the substrate. The film can be formed by CVD deposition or by recrystallization from the melt. The pattern relief structure reduces the activation potential for nucleation and forces orientation of the silicon islands (formed in the initial stage of growth) in a desired direction.[11] Theoretically, graphoepitaxy has the greatest potential for SOI film fabrication. Unfortunately, prac-

tical problems with grid preparation and preservation of a grid during the solidification process have so far hampered development of this method. Also, there are still some problems with a detailed understanding of mechanisms involved in orientation of the islands (for an excellent review, see ref. 11). To the best of the author's knowledge, to date SOI films of sufficient quality for device fabrication have not been achieved by CVD graphoepitaxy. It should be pointed out that graphoepitaxy in combination with strip heater recrystallization has been successful in improving SOI film quality. A pattern of parallel strips put on the top of a recrystallizing SOI film has been used to pin the location of the grain boundaries present in the SOI films (for a detailed review and discussion, see ref. 11). Good devices have been made in these films. Unfortunately, in this case, graphoepitaxy also has all liabilities of strip heater recrystallization (discussed below).

Seeded or unseeded recrystallization of melted silicon can be divided into: (1) formation of SOI films during recrystallization from a melted zone which is scanned across a wafer, an equivalent of a traveling zone method, and (2) pulse melting of the polysilicon films on the wafer surface and recrystallization of the melted region after termination of a heat pulse. Different heat sources, a laser and an electron beam, high-intensity lamps, or a graphite strip heater, can be used for the formation of the melted zone. Each of these techniques is briefly described and its assets and liabilities compared.

The approach of recrystallization from the scanned melted zone is shown schematically in Fig. 4. The recrystallizing SOI film is sandwiched between dielectric layers and heated uniformly to temperature T_0, which can be between room temperature and 1200°C. Subsequently the melted zone is formed, in part or across the whole wafer, and moved across the wafer. Directional solidification can be spontaneous or can be induced by monocrystalline seeds which are initially in contact with the melted silicon. The major disadvantage of this technique is the high temperature (~1400°C) to which the substrate surface region (beneath the recrystallizing SOI film) is heated during recrystallization. Unless special precautions are taken to reduce this temperature and minimize the length of time during which material is exposed to this temperature, circuits already present in the substrate can be destroyed. Therefore, this technique would not be suitable for making three-dimensional circuits. In addition, large horizontal temperature gradients exist in the wafer heated locally to the melting point of silicon. The mechanical strength of silicon (upper yield point) decreases drastically with increasing temperature.[12] Hence, in the part of the silicon heated

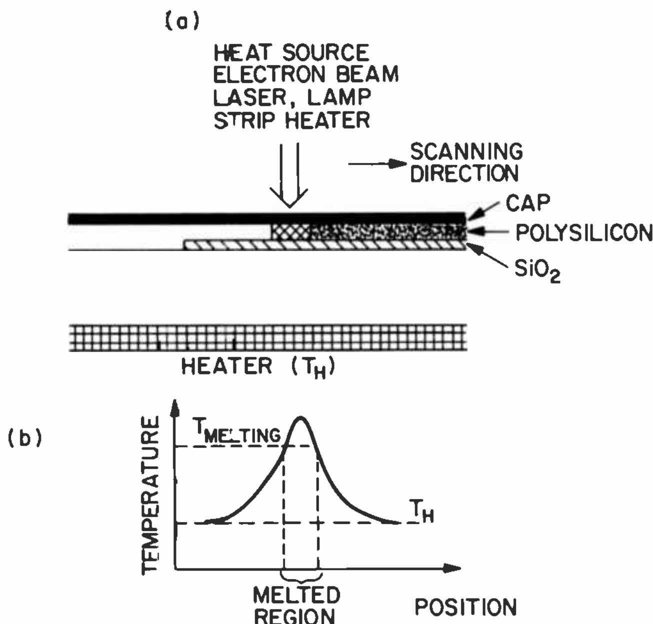

Fig. 4—Schematic representation of recrystallization from the scanned melted zone, temperature distribution in the SOI layers in the horizontal direction.

close to the melting point, stress introduced by these gradients will exceed the critical stress required for dislocation generation, and the wafer will become deformed plastically. Problems with slip and warpage of these wafers[7,13] during subsequent processing could adversely affect yield of IC circuits manufactured on these wafers. This problem is especially apparent for graphite strip heater recrystallization, after which warpage of 3-inch-diameter silicon wafers exceeds 25 μm[13] (measured with vacuum on).

During strip heater recrystallization a wafer is heated to 1000 to 1200°C, and the melted zone is formed across the entire wafer by a graphite strip heater placed a few millimeters above the wafer. A major advantage of this approach is the high speed of recrystallization; a 3-inch-diameter wafer can be recrystallized in a few seconds. Because the distance between the SOI film and the strip heater can change during the recrystallization process, e.g., due to a flatness deviation, there is a serious problem with a precise control of the amount of power dissipated to the SOI film. To have a comfortable margin for error, higher than minimum power required to melt SOI film is usually used, which leads to a higher temperature in

the melted zone and aggrevation of the previously discussed problems. Also, problems with carbon contamination can arise during strip heater recrystallization, although this can be overcome by sealing the graphite with protective layers.[13] Due to direct absorption of the light or electron beam by the recrystallizing layer, control of the power dissipated into the recrystallizing SOI film is more precise during laser, lamp, or electron-beam annealing than during strip heater recrystallization. Therefore, for these techniques the substrate surface under the oxide can be heated to lower temperatures and for shorter periods of time than during strip heater recrystallization. It is possible to optimize conditions to the point that the temperature/time of the substrate surface will be low/short enough to preserve devices present under the SOI film. Therefore laser, lamp, or electron-beam annealing could possibly be used for fabrication of vertically integrated circuits. As in the case of strip heater, the recrystallized films contain a high density of crystallographic defects introduced by the large temperature gradients.[13] At the present time it is impossible to predict the extent to which these defects would affect the performance of high-density circuits made on SOI films. Strip heater, laser, or electron-beam recrystallized SOI films have been produced of sufficient quality to make n- and p-channel MOS transistors.[14]

Because the laser spot size is small (10 to 100 μm in diameter) the time required to recrystallize a 3-inch-diameter wafer with a laser is prohibitively long ($\sim 10^3$ sec). An increase of the laser power and spot size is not a good solution. Power distribution in the laser beam is Gaussian; therefore, an increase of the beam size for the same average power density will result in a hotter center of the spot and higher temperature of the center of the melted area. This temperature can be high enough to cause significant melting of the wafer underneath the SOI film.[13] The recrystallization speed can be significantly increased if large area beams of incoherent light or electron beam would be used. The average power distribution in these beams is more uniform.

In the case of large area beams, the shape of the recrystallizing interface is extremely important. If crystallization starts at the center of the interface and proceeds to the edges, the density of the crystallographic defects is substantially reduced. So far, on a small scale, the recrystallizing interface has been successfully shaped by optically shaping the spot geometry or by providing a pattern on the surface that, by local variations in optical or thermal properties, gives the required heat flow pattern from the recrystallizing region.[15] To the author's knowledge none of these techniques has pro-

vided device-quality SOI films recrystallized with high throughput, but they have good potential for future applications.

During pulse-lamp recrystallization the entire surface of the wafer is melted by a light pulse (Fig. 5). After the termination of the pulse, slight horizontal temperature gradients develop due to more rapid heat flow through the silicon (seed regions where melt is in contact with silicon wafers) than through the SiO_2 mask. Then the silicon film starts to recrystallize around the seed regions, subsequently overgrowing the oxide. Due to surface tension and the volume dif-

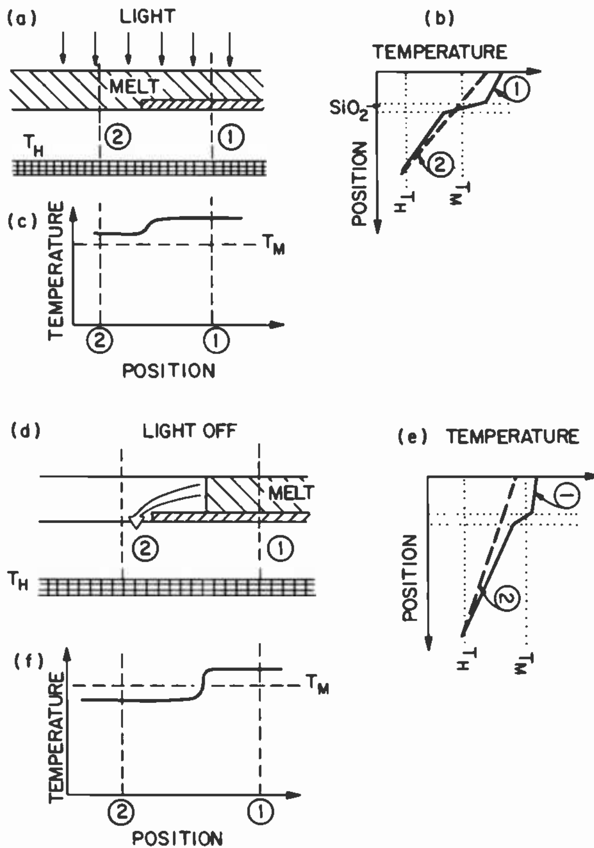

Fig. 5—Schematic representation of the pulse lamp recrystallization, (a) SOI film is melted by light pulse, (b) vertical temperature gradients in SOI film during light pulse (steady-state conditions), (c) horizontal temperature distribution during light pulse (steady state), (d) SOI film recrystallizes after pulse termination, and (e) and (f) horizontal and vertical temperature gradients.

ferences between melted and solid silicon, the surface of the recrystallized films is disturbed where the two solidification fronts, seeded on opposite sides of an oxide island, meet.[16] Because of the small temperature gradients present during the solidification, potential SOI films with low defect density and without warpage or slip of the substrates could be grown.[16] Unfortunately, as in the case of the strip heater recrystallization, the surface temperature of the substrate will be close to the melting point for ~1 sec; hence, this method will not be suitable for fabrication of vertically integrated circuits.

Another approach to obtain SOI films is the CVD Epitaxial Lateral Overgrowth (ELO) method, shown schematically in Fig. 6.[17,18] The silicon layer grown by CVD is seeded in the openings in a SiO_2 mask. If no nucleation of silicon on the SiO_2 surface takes place, the silicon grows vertically to the mask level and then laterally over the SiO_2 mask as it continues vertical growth. Growth can be stopped at any time, giving silicon islands defined in the oxide windows or partially formed over SiO_2, or it can be continued until the growth fronts seeded from different windows meet, forming a continuous film of silicon. This approach uses the mature and well-developed silicon CVD technology (equipment and procedures). The growth process can be completed in a few minutes with growth rates on the order of 1 μm/min at 1000°C.[19] The possibility exists to re-

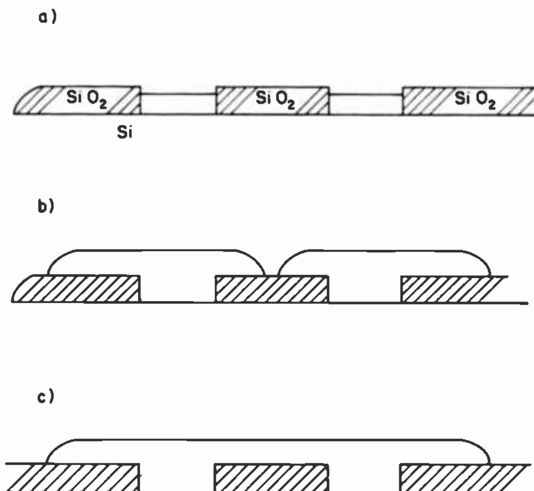

Fig. 6—Schematic representation of CVD Epitaxial Lateral Overgrowth (ELO). (a), (b), and (c) represent different stages of overgrowth.

duce the deposition temperature to significantly less than 1000°C. Relatively low temperatures and short deposition times should prevent any significant movement of junctions already present in the substrate. Then this technique can be classified as low-temperature processing and could be used for making three-dimensional integrated circuits.

Mask coverage is controlled by the ratio between a horizontal and a vertical growth rate. This ratio has been reported as high as 40:1.[20] To date good quality ELO films have been grown with the ratio of 1 to 2:1.[17,18] The growth and surface morphology of ELO films is a strong function of the growth conditions. Under the optimized conditions (100) oriented ELO films covering 20-μm-wide SiO_2 islands with smooth, mirror-like surfaces have been grown.[19]

To carry out growth of good-quality ELO films, it is essential to suppress silicon nucleation over the SiO_2 while homoepitaxial growth takes place (selective deposition). Historically it has been shown that by introducing HCl to the gas stream, the homogeneous nucleation over the oxide can be suppressed and selective growth can be carried out. Unfortunately, even if HCl concentration is large enough to suppress the homogeneous nucleation, a low density (10–10^3 cm^{-2}) of nuclei still can be found on the oxide suface. It is believed that they are formed around such defects on the oxide surface as pin-holes, contamination, and topological defects. For application of ELO films in VLSI or LSI circuits, this defect density is unacceptably high.

The growth/etch procedure has been proposed[19] to eliminate the nuclei. This procedure is based on the observation that formation of polysilicon nuclei on an oxide surface requires a certain amount of time: time for deposition of silicon atoms over SiO_2 and time for condensation of the deposited silicon atoms into the polysilicon nuclei.[20] If growth could be carried out for a period shorter than this critical time, stopped, and followed by an HCl etch, the silicon atoms deposited on SiO_2 would be removed prior to formation of polysilicon nuclei with a minimal etch of homoepitaxial silicon. After completion of the etch cycle the SiO_2 surface is free of the silicon atoms and the next growth cycle starts on the clean SiO_2 surface. The length of the growth/etch cycle is a complex function of: (1) gas composition, type of gases and their concentration, (2) pressure, (3) growth temperature, and (4) the type of reactor, and usually has to be established on an experimental basis.[17]

Under the conditions of suppressed nucleation, the ELO films with low densities (10^3 to 10^4 cm^{-2}) of dislocations and stacking faults have been routinely obtained.[21] It seems that under the op-

timized growth conditions ELO films are grown defect-free and that dislocations and stacking faults are introduced into the films during cooling, following the growth process, due to stress caused by a difference in the thermal expansion coefficients between oxide and silicon. The defect structure is sensitive to the orientation of the stress risers, e.g., edges of the oxide islands in relationship to the slip planes in silicon. For (100) substrates the [010] orientation (or equivalent) of oxide islands was found to give the lowest defect density.[21] The good electronic characteristics of the ELO films are the result of this low defect density. The minority carrier lifetime and the majority carrier mobility in ELO films are practically the same as the values obtained in homoepitaxial layers grown under the similar conditions.[22] The characteristics of devices such as p-n junctions, MOS, and bipolar transistors made in ELO layers were comparable to characteristics of devices made in homoepitaxial layers.[22]

The major disadvantage of the ELO technique is the low ratio of horizontal to vertical growth rates, which imposes serious limitations on the width of the oxide islands that can be covered by an ELO film of a given thickness. It is the author's belief that a better understanding of the growth mechanisms should allow us to significantly increase this ratio without compromising the ELO film quality.

3. Application of SOI

In most instances SOI films are being considered as a straightforward replacement of SOS (silicon-on-sapphire), and a significant reduction of material cost should result. This application requires a thin (0.5 μm) SOI film over the large area of oxide grown without additional geometrical constraints such as openings in the SiO_2 mask for seeding. The most suitable techniques are strip-heater recrystallization or deep-oxygen implantation. SOI films grown by ELO at the present stage of development are not suitable for use as a simple replacement for SOS. For ELO films with low defect density, the ratio between horizontal and vertical growth rate is low (close to 1.5), and, therefore, ELO cannot currently be used to form a thin 0.5-μm film covering large areas ($\approx$50 μm) of insulators. If the horizontal-to-vertical growth rate ratio could be increased to 50:1, ELO films could be considered as a replacement of SOS. However, it is not clear if this is achievable in the future although in the initial stage of growth, a ratio as high as 40:1 has been obtained.[20]

It must be demonstrated that this ratio could be maintained during the growth of low-defect-density films covering large areas of SiO_2.

So far the main development effort in SOI has been the use of SOI films to improve conventional circuit performance in improving the circuit structure. A major concern has been the elimination of latch-up in CMOS circuits. This has been achieved by forming SOI films on parts of a wafer in regions where one type of transistor (n or p MOS) was fabricated. In this case 1- to 3-μm-thick SOI films were used. Because a SOI film is required only on parts of a wafer, the best fabrication method is FIPOS.

Another approach to improve conventional CMOS circuit performance by modifying its structure is shown in Fig. 7. This structure can be obtained by growing a thick oxide, cutting holes in the oxide with plasma etching, and refilling the holes with selective epitaxy performed using the ELO procedure.[23,24] Although this approach does not give a total isolation between n and p type devices, a "bird beak" does not exist in the fabricated structures, and a thicker field oxide can be used. Since this type of transistor can be made smaller than conventional transistors, higher packing density and speed and lower power dissipation can be achieved than in the conventional configuration. The same approach and the similar benefits could be achieved using the ELO technique to make bipolar tran-

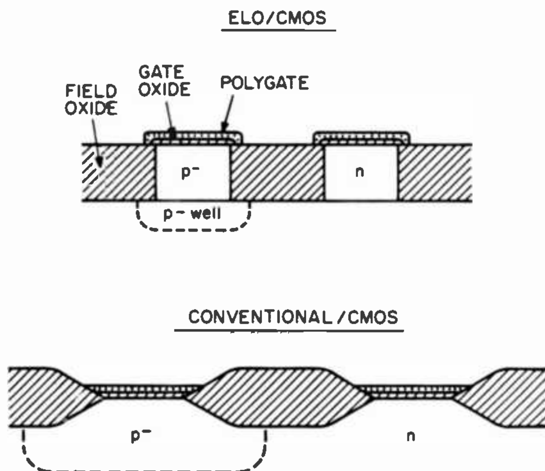

Fig. 7—Schematic comparison of field oxide isolation used by conventional MOS process and process based on ELO. Notice absence of "bird beak" in ELO process and better packing density.

sistors.[25] In the ELO bipolar circuits p-n-p and n-p-n transistors can be made symmetrically (same area of emitter and collector junctions) and, therefore, circuit performance could be improved by the ability to operate these transistors with upward as well as downward current flows.

Another area of SOI application will be the simplification of present processes which should result in yield improvement and cost reduction, e.g., dielectrically isolated bipolar processes. For dielectrically isolated bipolar circuits about 5- to 10-μm-thick SOI films should be used. ELO and FIPOS can easily provide desired geometries, while all other SOI methods have to be followed by an additional homoepitaxial growth of silicon to obtain the required thickness of epitaxial layers. Obviously new planarization techniques of the etched surfaces have to be developed before SOI films will be able to significantly simplify the D.I. process for bipolar transistors. An example of simplification of the presently used D.I. bipolar process by using SOI films is shown schematically in Fig. 8. In the conventional process silicon islands are formed by etching a silicon wafer. The wafer is oxidized and subsequently a thick (≈250 μm) polysilicon layer is grown on the front surface of the wafer to be used later as a handle. The wafer is then lapped from the back until the Si islands are insulated from each other. The lapping operation is a low yield step, and the lapped wafers are severely warped

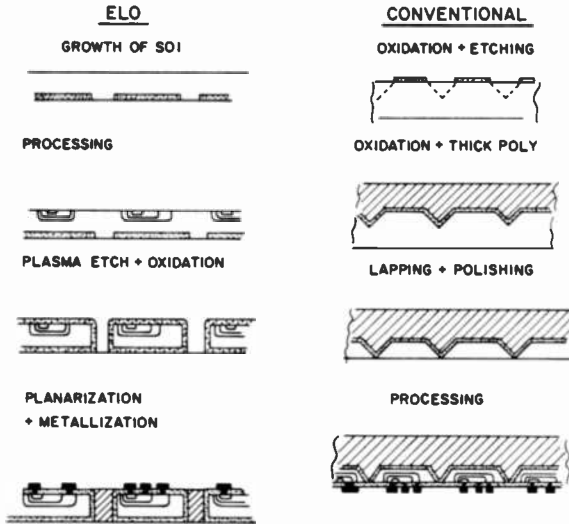

Fig. 8—Schematic comparison of processing steps in D.I. bipolar process: conventional and based on ELO.

by stress from the polysilicon film. This warpage significantly reduces the yield of the circuits made subsequently in the D.I. islands. In the ELO process for bipolar dielectric isolation an ELO film is grown over an oxide and transistors are fabricated in the ELO film. Then the ELO film is plasma etched and oxidized to define D.I. islands. Subsequently, the etched grooves are filled with polysilicon or glass to planarize the surface for metallization. Then the metal is evaporated, patterned, and sintered. Lapping operations or thick polysilicon layers are not necessary in this process, which should reduce the cost of the process and processing time and also improve the yield of D.I. bipolar circuits made on these wafers.

Another potential area of application for SOI films is three-dimensional circuits (vertically integrated). Since at the present stage it is impossible to predict which approach to three-dimensional integration will be used in the future, it is difficult to predict which SOI technology will be used. The layout of three-dimensional circuits will be a major factor affecting the choice of SOI technology used for their fabrication.

It is the author's belief that to achieve a major benefit from three-dimensional SOI circuits, the circuit components, e.g., decoders, invertors, and memory cells, should be built vertically with the current flowing in the MOS transistors in the vertical direction. An example of a vertical MOS transistor, which could be a building block of such circuits, is shown schematically in Fig. 9. The vertical transistor channel length is controlled by the thickness of the polysilicon gate, which could be easily controlled in the submicron range; therefore, devices with submicron channel length could be made using the conventional, e.g., 2 or 3 μm, design rules for circuit layout and photolithography. This approach to three-dimensional

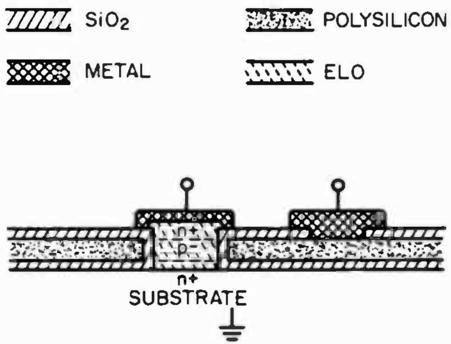

Fig. 9—Schematic diagram of vertical MOS transistors that could be made by the ELO process.

integration should lead to an increase in packing density and a decrease in the length of connections. Therefore, it should reduce power dissipation and increase circuit speed. The ELO process seems to be only one SOI method that could be used conveniently for fabrication of the vertical transistors in three-dimensional circuits. However, it has to be emphasized that different approaches to vertically integrated circuits, e.g., conventional MOS transistors (with gate current flowing in the plane that is parallel to the substrate) made in SOI layers formed one on top of the other, could favor other SOI technologies for three-dimensional circuits, e.g., laser recrystallization.

4. Discussion and Summary

The discussion of the SOI technologies presented above clearly shows that none of them has a clear advantage over the others and that their assets and liabilities should always be evaluated in a context of specific applications. In the author's opinion four criteria are important for any application and should be used as a base for general comparison; although emphasis on each of them can change significantly with the specific requirement of a given application.

(1) *Conventional processing*—Are the equipment and procedures presently used by the IC industry sufficient for a given SOI technology or should new equipment and processing procedures be developed? Capital investment and time required for development of new equipment or processing for production of SOI wafers by a given method can make implementation of this approach noneconomical.

(2) *Time*—The amount of time required to prepare SOI films on 50 four-inch-diameter wafers is an important consideration. Is this time similar to that required by other processing steps, or is it prohibitively long? This could significantly affect the cost of processed wafers.

(3) *Defect density*—Do SOI films contain high defect densities? This could provide a significant limitation in achieving high yield in high-density ICs.

(4) *Stage of development*—This is divided into four phases:
   - (a) Maturity—real circuits made, e.g., 1K CMOS 16-bit microprocessor, using a given method.
   - (b) Childhood—arrays of individual transistors made with good characteristics.
   - (c) Infancy—method developed to the stage that it provides monocrystalline SOI films. No data on electric properties of SOI films available.

(d) Early infancy—concept of obtaining a monocrystalline SOI film by a given method has not been demonstrated yet.

The stage of development could be one of the most important factors influencing future allocation of resources to be invested in the development of SOI technologies.

Because of the importance of using SOI films in the future for vertical integration, an additional criteria should also be included:

(5) *Three-dimensional circuits*—The possibility of using a given approach for vertical ICs must be considered. Is the temperature/time during formation of the SOI film low/short enough to prevent any significant movement of junctions already present in the wafer? Circuit layout is not taken into consideration.

All these criteria for the different SOI technologies are compared in Table 1.

As has been emphasized before, the answer to the question: Which technology is the most promising? is not clear and has to be asked

Table 1—Comparison of Different SOI Technologies*

Method	Assets	Liabilities
SIMPOX	A) Conventional processing B) Low defect density C) Development stage—maturity	A) No 3d B) Time of implantation
Porous Silicon	A) Low defect density B) Development stage—maturity	A) No 3d B) Nonconventional processing
Ion Implantation and Solid State Regrowth**	A) Conventional processing B) 3d possible	A) Stage of development—early infancy (can be achieved?)
Graphoepitaxy (CVD)***	A) 3d possible	A) Stage of development—early infancy (can be achieved?)
ELO	A) Conventional processing B) Low defect density C) 3d possible D) Time short E) State of development—childhood	A) Ratio between horizontal and vertical growth rates (overgrowth)
Recrystallization from Melt		
Pulse (Lamp) Melting	A) Time short B) Low defect density	A) No 3d B) Surface morphology C) Stage of development—infancy
Strip Heater (Traveling Zone Method)	A) Time short B) Stage of development—childhood	A) No 3d B) Defect density high
Laser (Traveling Zone Method)	A) 3d possible B) Stage of development	A) Defect density high B) Time long
Electron Beam (Traveling Zone Method)	A) 3d possible B) Time short	A) Defect density high
Lamp (Traveling Zone Method)	A) 3d possible B) Time short	A) Defect density high

Table 1—Continued

Method	Technology: Most Suitable For	Technology: Cannot Be Used For
SIMPOX	CMOS	Vertical integration
Porous Silicon	A) CMOS B) Bipolar	A) Vertical integration B) Replacement of SOS
Ion Implantation and Solid State Regrowth**		
Graphoepitaxy (CVD)***		
ELO	A) CMOS B) Vertical Integration C) Bipolar	A) Replacement of SOS
Recrystallization from Melt		
Pulse (Lamp) Melting	A) Bipolar	A) Vertical integration (?) B) Replacement of SOS
Traveling Zone Method:		
Strip Heater	A) CMOS B) Replacement for SOS	A) Vertical integration
Laser	A) CMOS B) Replacement for SOS	
Electron Beam	A) CMOS B) Replacement for SOS	
Lamp	A) CMOS B) Replacement for SOS	

* Criteria considered to be neither assets nor liabilities for a given technology are not included.
** In the case of technologies that are not sufficiently developed, comments on possible circuit applications are not made.
*** Only CVD graphoepitaxy is discussed here. Liquid graphoepitaxy has all problems of recrystallization from melt.

in the context of future applications. For vertically integrated circuits of the future, the most promising approach seems to be lamp/ laser scanned recrystallization or ELO.

For application in already present circuits, e.g., for latch-up elimination, the most promising seems to be oxidation of porous silicon although, for custom circuits, when performance considerations outweigh cost considerations, SIMOX looks very attractive.

The ELO technique seems to have the advantages of conventional processing, time (high throughput), low defect density, the possibility of three-dimensional structures, and a reasonable stage of development. The only one significant limitation is the overgrowth ratio, which imposes serious geometrical restraints and excludes, at present, the ELO technique from being used to fabricate films which can replace SOS. If this application is excluded from consideration, the ELO technique seems to be a good choice from the various SOI

technologies for the D.I. bipolar process, the formation of three-dimensional structures, or applications to improve conventional CMOS circuit performance.

Acknowledgment

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Double-Barrel III-V Compound Vapor-Phase Epitaxy Systems

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Abstract—A unique system for the growth of III-V compound multilayer structures—without interruption of crystal growth—is described. This system has generated large improvements in the synthesis of long-wavelength optoelectronic devices. A complete 1.3-μm laser structure can be grown in 30 minutes and more than 15 such structures can be grown in a single day. Single layers as thin as 60 Å have been measured. 1.3-μm InGaAsP cw lasers with lasing threshold currents as low as 45 mA and 1.0–1.7-μm InGaAs photodetectors with leakage currents below 10 nA and quantum efficiencies near 80% have been synthesized with the system.

1. Introduction

Vapor-phase epitaxy (VPE) is a crystal growth process whereby gases are used to deposit a solid semiconductor compound or alloy onto a crystalline substrate. Epitaxy is the phenomenon whereby the deposited solid adopts the crystalline structure of the substrate upon which it is deposited (as opposed to being amorphous or polycrystalline). In the VPE process, the solid alloy composition is determined by the gas composition which can be *linearly* controlled by electronic mass-flow controllers. Thus, indium, gallium and arsenic vapors can be used to form $In_xGa_{1-x}As$ alloys, while the addition of phosphorus-bearing vapors would produce $In_xGa_{1-x}As_yP_{1-y}$ alloys. The substrate ideally has a similar crystal structure and atomic spacing in order to minimize the formation of growth defects such as misfit dislocations and stacking faults.

Many of the key developments in the vapor-phase epitaxy (VPE) of III-V compounds have occurred at RCA Laboratories. Tietjen and

Amick[1] in 1966 demonstrated the hydride VPE process for GaAsP alloy deposition. Since then, much development has occurred, resulting in the successful fabrication of room-temperature cw lasers at 0.7, 0.85, 1.06, 1.25, 1.30, 1.55, and 1.65 μm, together with LEDs at 1.06, 0.13 and 1.55 μm and photodetectors for the 1.0-1.7 μm spectral region. Commercial products made with the VPE process include GaAs photocathodes, 1.06- and 1.3-μm lasers and LEDs, and 1.0-1.7 μm photodetectors. Red, yellow, and green LEDs made from VPE GaAsP and GaP have been available commercially for over a decade. The purpose of the present paper is to describe one of the latest advances in the VPE technique, the double-barrel reactor.

The advantages of VPE growth over other crystal growth techniques[2] for III-V compounds (e.g., liquid phase epitaxy (LPE), molecular beam epitaxy (MBE), and metalorganic chemical vapor deposition (MOCVD)) include:

1. Easy control of alloy composition.
2. Ability to "compositionally-grade" alloy composition.
3. Growth of smooth crystal surfaces.
4. Scale-up potential for mass-production.

2. Vapor-Phase Epitaxy: Hydride versus Chloride

The two most popular methods for the VPE growth of III-V compounds have been the so-called "chloride" method, whereby a group V chloride (e.g., $AsCl_3$) is passed over the metal to form a metal chloride (e.g., GaCl), and the so-called "hydride" technique, in which the group V element is introduced as a hydride (e.g., AsH_3) and the metal chloride is formed by passing HCl over the metal. Strictly speaking, the term "halide" should be used rather than "chloride", since I and Br have also been used as transport agents. The main advantage of the chloride system is that it has produced very low ($<1 \times 10^{13}$ cm^{-2}) undoped background impurity concentrations[3] in GaAs. Its main disadvantage is that gaseous $AsCl_3$ is introduced by heating a liquid and, therefore, its concentration will vary exponentially with temperature. The hydride system, on the other hand, has the advantage that all input reactants to the system are gaseous and can be carefully controlled in a linear manner. Thus, crystal compositions can be more carefully controlled with the hydride system, and this is the major reason for its use, especially with optoelectronic devices.

Although there are numerous previous reports of the growth of GaAs with arsenic vapor and gallium chloride, the first report on the growth of a high-quality III-V compound via the hydride tech-

nique must be traced to Tietjen and Amick[1] at RCA Laboratories, who synthesized GaAsP using HCl, Ga, AsH_3, and PH_3. Although an earlier patent exists on the growth of III-V compounds, whereby the use of hydrides of arsenic and phosphorous are *suggested,* no actual claims or examples of the use of arsine and phosphine are mentioned. After the growth of GaAsP had been accomplished, the technique was quickly adapted to the growth of other III-V compounds and device structures as well. The techniques described here are an outgrowth of the original studies of hydride vapor phase epitaxy of III-V compounds by many RCA workers, including Richman[4] and Enstrom et al.[5]

3. Single-Barrel VPE Reactor Design

The RCA single-barrel VPE growth system[6,7] is shown schematically in Fig. 1. The reactor tube (~25-mm internal diameter) is made of quartz except for areas that are not heated to high temperatures, which are made of Pyrex. Heat is provided by the use of "clamshell" resistance furnaces which surround the tube. Photographs of the quartz growth tube and of the complete system are shown in Figs. 2 and 3. The furnaces are left on at all times (except for disassembly or cleaning) and hydrogen flows through the tube constantly. Deposition is initiated by passing HCl gas over the indium and/or gallium metal (which is held at 850–900°C) in order to form metal chlorides. The area of indium metal held in quartz boats is considerably larger (~100 cm^2) than that of gallium metal (~25 cm^2). Arsine and/or phosphine (10% in H_2) are brought in through a separate tube and then mixed with the metal chlorides in a mixing zone. P-type doping is accomplished by heating a zinc bucket in a hydrogen atmosphere in order to obtain elemental zinc vapor which is then transported by H_2. N-type doping is accomplished by adding about 100 ppm H_2S gas to the group V line. All input reactant flows

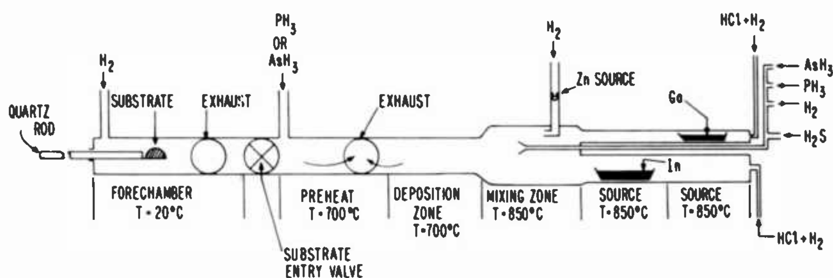


Fig. 1—Sketch of single-barrel VPE growth system.

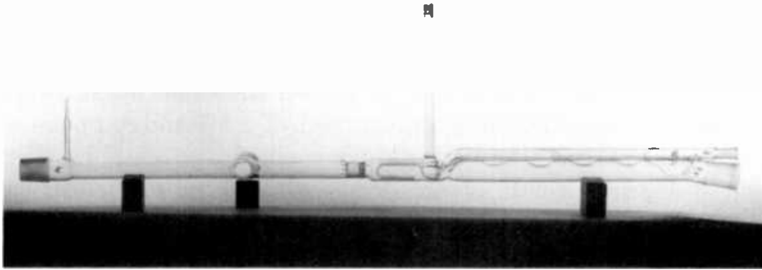


Fig. 2—Quartz tube used in single-barrel VPE system.

are controlled by electronic mass-flow controllers. Growth is initiated by inserting a polished substrate on a rotatable sample holder with a quartz spring that is attached to the end of the quartz rod and inserted into the forechamber, which is then flushed out with hydrogen while the input gas flows are being equilibrated. The substrate is sealed off from the growth chamber by a large Pyrex stopcock (substrate entry valve). After the forechamber is flushed out (~15 min at 2000 cm^3/min of H_2), the stopcock is opened and the quartz rod (which is supported by a close-tolerance 'truebore' gas bearing) is pushed in so that the substrate is moved to the preheat zone. This zone has an atmosphere of arsine and/or phosphine, corresponding to the substrate group V constituent, in order to mini-

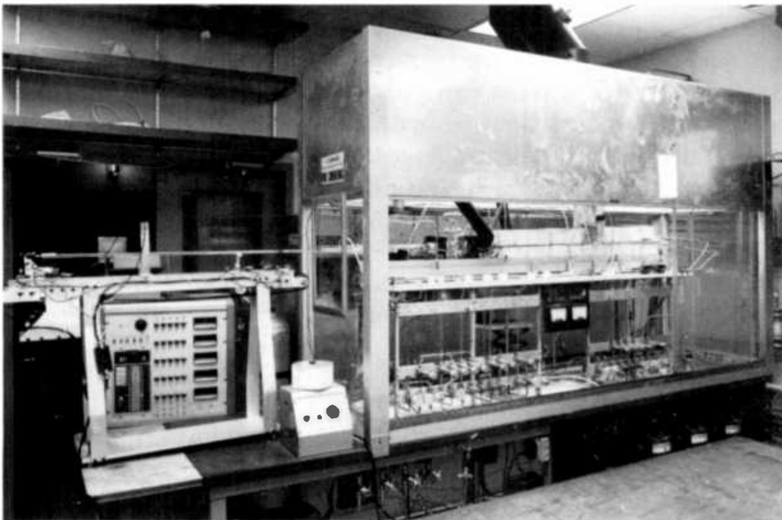


Fig. 3—Automated RCA single-barrel VPE system.

mize decomposition effects. The substrate is heated to a temperature near the growth temperature and then inserted into the growth zone where deposition takes place. The substrate is rotated (~10 rpm) during growth in order to smooth out any nonuniformities in temperature or gas flow. The temperature over the substrate is constant to within ±0.1°C. Thickness uniformities of ±5% and compositional uniformities of ±0.1 mol% have been measured with $In_{0.5}Ga_{0.5}P$ grown on GaAs. Growth is ended by withdrawing the substrate to the forechamber (before altering any of the flows) where it cools to room temperature in a hydrogen ambient. If the substrate is to be removed, the stopcock must first be closed. However, if subsequent layers are to be grown, the substrate is held in the forechamber while the reactant flows are changed and equilibrated (typically 15-30 min). The above process is then repeated. If compositional grading is desired, the control voltage to the appropriate mass-flow controller can be varied either abruptly (in discrete steps) or smoothly in a continuous fashion.

4. Limitations Imposed by the Preheat Process

One drawback of the single-barrel VPE process described in the previous section is in the preheat cycle. Here, substrate wafers are heated up to 650–700°C prior to growth without deposition or etching taking place. This temperature range equals or exceeds the congruent evaporation temperature[8] for most III-V compounds, and some preferential evaporation of the group V element is bound to take place. InP is particularly susceptible to this phenomenon, since its decomposition temperature is only around 400°C. Fig. 4 shows an extreme example of what can happen to an InP surface when it is heated to 670°C for 1 hour in hydrogen. Many pits and free indium globules are evident on the surface. This damage can be reduced by preheating the substrate in the appropriate group V hydride (i.e., AsH_3 or PH_3). Fig. 5 shows how the surface morphology of InP can be improved by using a PH_3 atmosphere during the preheat.

In addition to the surface morphology of a preheated layer, which is obviously degraded by the preheat decomposition, the microstructure of the material also suffers. A high density of defect loops has been observed[9] via transmission electron microscopy near the active regions of InGaP/GaAsP lasers, as shown in Fig. 6. This sample was lattice-matched throughout, as is evidenced by the lack of misfit dislocations at any interface. However, no group V gas was flowing during the preheat of any of the layers. This figure (together with other related ones not shown) leads to the conclusion that the de-

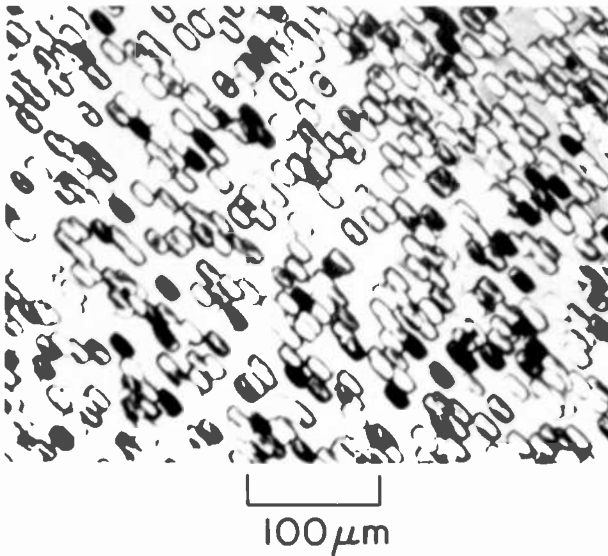


Fig. 4—Optical photograph of a (100) InP surface heated in H_2 at 670°C for 1 hour.

fects are dislocation loops on (111) planes with a vacancy character. The loops were formed by the coalescence of vacancies produced by interfacial decomposition due to preferential evaporation of phosphorus during the preheat of the n-(In,Ga)P layer prior to growth of the n-Ga(As,P) active region. Note that the substrate (In,Ga)P interface in Fig. 6 exhibits no decomposition, because Ga(As,P) has a higher dissociation temperature than (In,Ga)P. However, this interface probably also contains a significant excess point-defect density, as would any III-V compound surface that is heated above 600°C for any length of time. A rough estimate shows that the ratio of loop volume (assuming them to be one atom thick) to active region volume in Fig. 6 is $\sim 10^{-4}$. Thus, a very high point-defect concentration could easily develop in the active region, and subsequently serve as a source for degradation processes. The dislocation loops can be eliminated by using high flows of the group V carrier-gas and lower temperatures during preheat. However, an excess point-defect concentration may always be present to some extent, and should be viewed as a potential failure mechanism in any III-V compound light-emitting device prepared at elevated temperatures.

Fig. 6 also shows a cross-sectional TEM micrograph from an

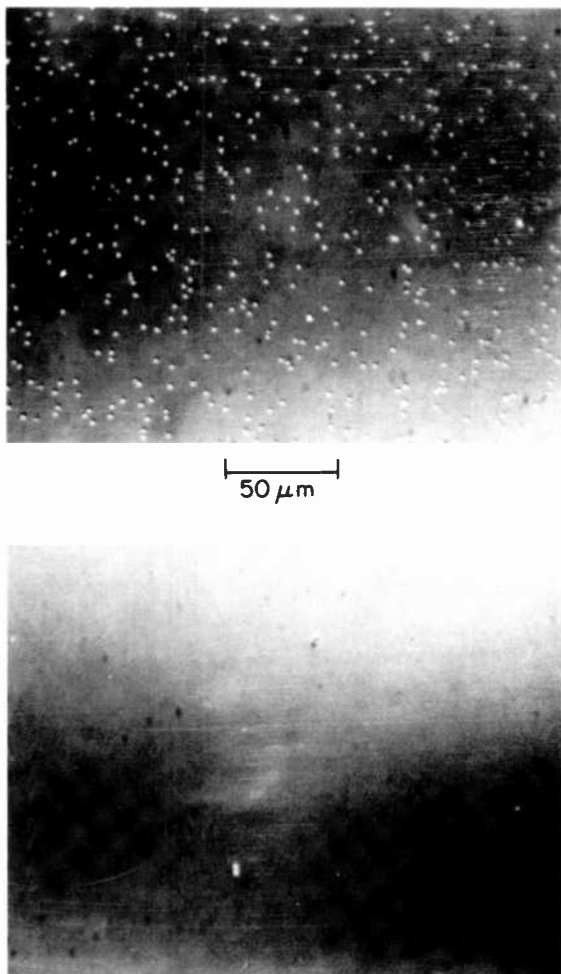


Fig. 5—Optical photographs of InP surfaces which show the effect of increased PH_3 flow upon surface morphology after heating to 650°C for 3 min (bottom photograph has highest PH_3 flow).

InGaAs/InGaP 1.06 μm laser that was preheated with high flows of the appropriate group V gas during preheat. The lack of interfacial defects is to be noted and testifies to the beneficial effect of using group V gases during preheat. Fig. 6 also demonstrates that planar and continuous laser cavities as thin as 900 Å can be prepared by the hydride technique. Cavities as thin as 400 Å have in fact been grown.

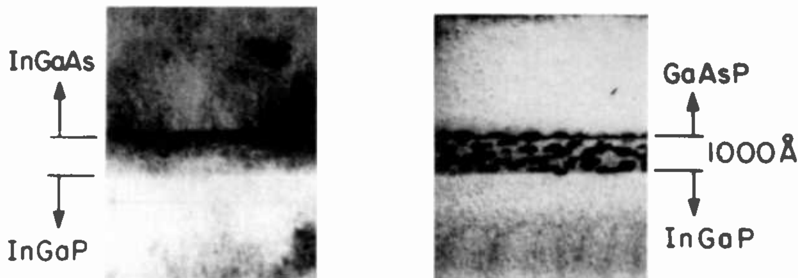


Fig. 6—Cross-sectional (011) transmission electron microscope (TEM) micrographs of InGaAs and GaAsP grown on InGaP. The sample on the right was *not* preheated in PH_3 and contains dislocation loops that have vacancy character (courtesy of M. S. Abrahams and C. J. Buiocchi).

5. The "Double-Barrel" VPE Reactor

The "double-barrel" VPE reactor[6] has been designed at RCA and is shown in Figs. 7–9. A similar system has been described by Watanabe.[10] The concept involves the use of two conventional VPE systems placed in parallel and feeding into a single-growth chamber. With this construction, different gases can be run through each tube, so that double-heterostructure lasers (e.g., InP/InGaAsP/InP/InGaAsP) can be prepared by simply switching the substrate from one tube to the other. This removes the need for preheat cycles, which may limit device performance since they can introduce interfacial defects. It is important to note here that *crystal growth is not interrupted during the switchover from one layer to another.*

A photograph of the quartz tube is shown in Fig. 7. A heat pipe surrounds the deposition zone (in order to maintain a uniform growth temperature) and obscures its view. A frontal photograph of this zone may be seen in Fig. 9. Here, the two separate circular-flow

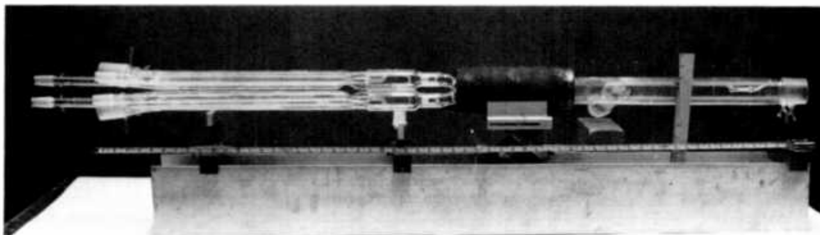


Fig. 7—Photograph of quartz tube used in the RCA "double-barrel" VPE reactor.

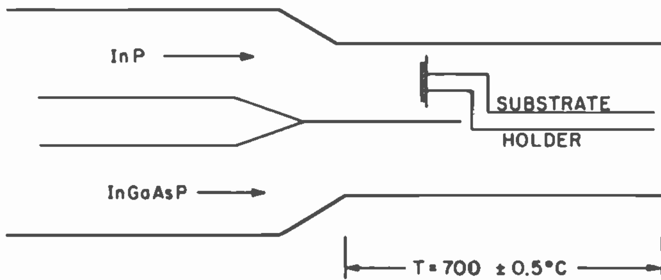


Fig. 8—Sketch of the "double-barrel" VPE growth tube.

tubes can be seen, along with the flat quartz plate that separates them and leads into the single-barrel growth zone. A sketch of the growth zone is shown in Fig. 8. The substrate can either be held just in front of each tube, or inserted into the tube if any mixing problems occur. Conversely, by holding the substrate at the end of the quartz plate and rotating it, extremely thin multilayers can be grown. It is estimated that by rotating the substrate at 200–300 rpm under normal VPE growth conditions, single atomic layers of each material could be deposited. This offers the unique possibility of preparing structures that exhibit quantum size effects.[11] For example, the solution of Schroedinger's equation for an electron in an

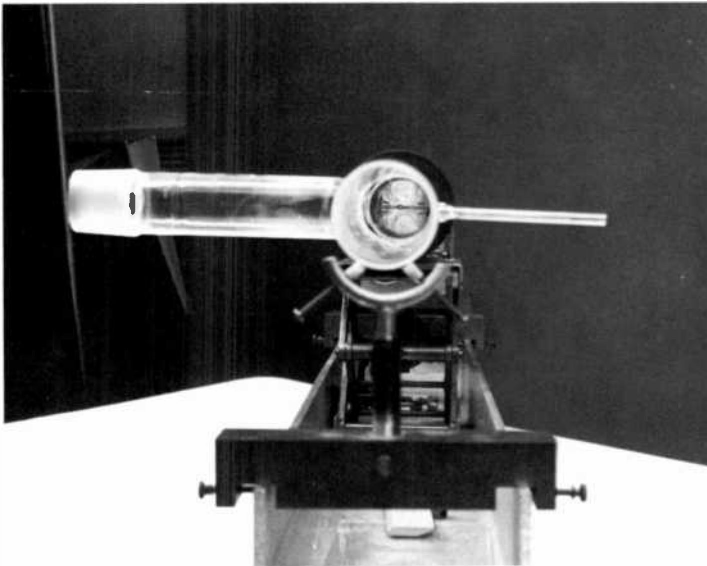


Fig. 9—Frontal photograph of the quartz tube shown in Fig. 8.

ideal one-dimensional infinite potential well predicts that the allowed energies vary as

$$E = \hbar^2/2m\ (n\pi/L)^2$$

where L is the width of the well in the electron mass and $\hbar$ is Planck's constant. For conventional layer thicknesses (>1000 Å), L is very large, and a continuum of energy states results. However, for very thin layers, discrete energy levels can be observed whose energies vary with thickness. Thus, the band structure (and the emission properties) of very thin layers may be tuned merely by adjusting the layer thickness. Details of the band structure (such as effective mass and dispersion relations), as well as the tuning of the laser emission wavelength with thickness, can be explored with such structures.[11] For example, a 1500 Å layer would have energy level separations of only ~0.02 meV, whereas a 200 Å layer would have levels separated by ~1 meV. Behavior of this type has been reported with AlGaAs structures grown by organometallic VPE.[12] Many "superlattice-type" structures have been grown via molecular beam epitaxy.[13] Blakeslee[14] has grown GaAsP superlattice structures via the hydride VPE method by pulsing the PH_3 gas. Fig. 10 shows a stained, angle-lapped (1°) section of a multiple InGaAs/InP

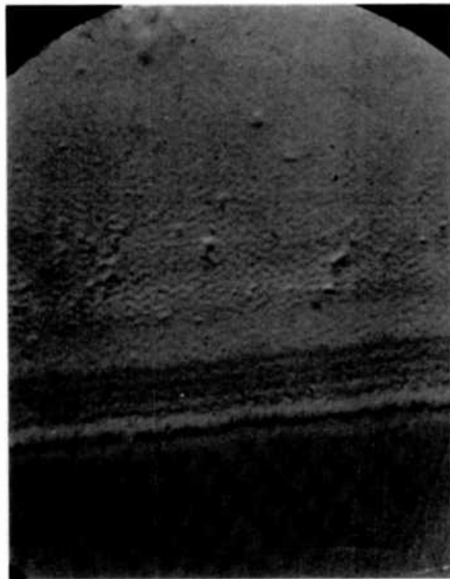


Fig. 10—SEM micrograph of a stained 1° angle-lapped section of a multilayer $In_{.5}Ga_{.5}As/InP$ heterostructure grown in the double-barrel reactor. Smallest layer thickness is ≅60 Å (courtesy of B. J. Seabury).

Table 1—Six Consecutive Double-Barrel CW Laser Growths*

Wafer	Substrate	$\lambda(\mu m)$	I_{th} (mA)
5788	(100)	1.277	110
5789	(100)	1.304	130
5790	(100)	1.266	150
5792	(100)	1.314	125
5795	(311)	1.252	120
5805	(311)	1.230	140

* 12-μm oxide-defined stripe contact.

multilayered structure. A minimum thickness of ~60 Å is to be noted.

Although exciting fundamental studies of this nature may be performed with structures prepared in the new reactor, its main practical advantage is a saving in growth time and materials, as well as the possible attainment of highly superior interfacial properties. Growth of a typical laser structure presently takes about 2 hours and involves four preheat cycles, including one at each of the two cavity interfaces. InP is particularly susceptible to decomposition effects at elevated temperatures. With the new system, the total growth time is reduced to 30 min, and all preheat cycles are eliminated (except for the original one, which is positioned 5–10 mm below the laser cavity). The reduced growth time would enable 15 or more laser wafers to be grown in a single day. The information given in Table 1 demonstrates the viability of the double barrel reactor. Six consecutive 1.3 μm InGaAsP/InP cw laser wafers were grown, yielding thousands of usable chips. The elimination of the preheat cycles is expected to yield cleaner interfaces, which should provide lasers with lower threshold current densities, higher efficiencies, and better reliability. Advantages of the double-barrel reactor are highlighted in Table 2.

Table 2—Advantages of Double-Barrel VPE Reactor

Cleaner Interfaces: Crystal growth is *not* interrupted when growing multiple (heteroepitaxial) layers.

Rapid Device Growth: A complete four-layer InGaAsP/InP/InGaAsP/InP 1.3 μm cw laser structure can be grown in about 30 minutes. Fifteen or more wafers of this type could be grown in one day.

Very-thin Layer Growth: Multiple layers, each as thin as 60 Å have already been grown, thus allowing "quantum-well" type structures to be fabricated. By rotating a substrate at ~250 rpm in front of the two barrels, layers on the order of 10 Å *might* be grown.

Cheaper: A factor six savings in material (gases, metals, etc.) costs results from the reduced growth time for devices.

6. Other Multibarrel VPE Reactors

A dual-growth-chamber GaAs VPE reactor was proposed by Watanabe et al.[10] in 1977 to produce abrupt changes in doping profile. This system was upgraded into a GaInAsP dual-growth-chamber reactor by Mizutani et al.[15] Other types of multibarrel reactors were independently conceived to grow (Ga,In)(As,P) by Olsen and Zamerowski[6] (the "double-barrel" reactor) and by Beuchet et al.[16] (the four-barrel "multichamber" reactor). The three types of reactors are shown in Figs. 8, 11 and 12.

The dual-growth-chamber reactor of Mizutani[15] (Fig. 11) consists of one horizontal chamber to grow InP and another parallel chamber to grow alloys of (Ga,In)(As,P). The substrate is supported by a rod mounted on a flexible rubber bellows so that transfer between chambers is accomplished by withdrawing and shifting the rod. Transfer can be effected within 2 s and heterointerface transition widths less than 50–60 Å are claimed. Although (in its present form) gallium-bearing alloys can only be grown in one of the chambers, and no provisions have been made for p-type doping, high-quality 1.3-μm cw lasers have been synthesized in the system (Cd was diffused-in after growth for p-contact).

The "multichamber" reactor of Beuchet et al.[16] (Fig. 12) consists of four parallel tubes, each with a specific function. The system has been automated so that interchamber transfer can be effected within 1 s. The purpose of each chamber is as follows:

First: preheat and substrate etch
Second: growth of n-InP
Third: growth of n-GaInAs
Fourth: growth of p-InP

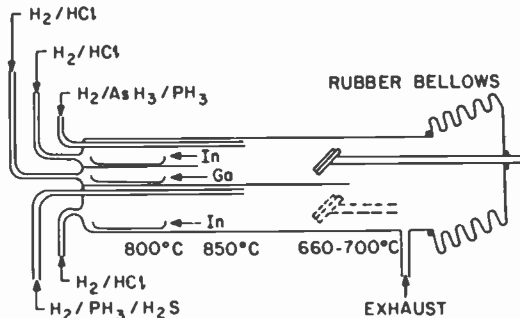


Fig. 11—Sketch of "dual-growth chamber" VPE reactor of Mizutani et al.[15] (courtesy of T. Mizutani).

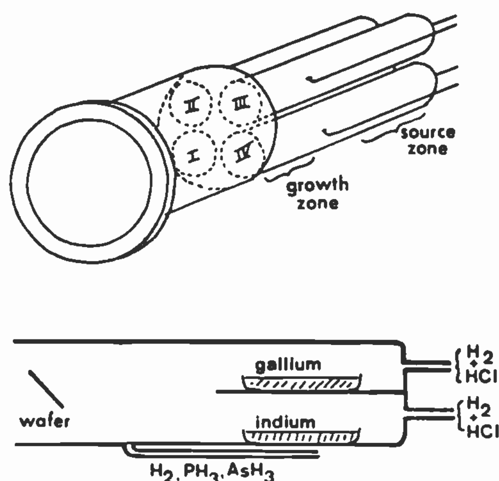


Fig. 12—Sketch of "multichamber" VPE reactor of Beuchet et al.[16] (courtesy of G. Beuchet).

Metallic zinc is used for p-type doping while H_2S is the n-type dopant. Other variants of the above procedures are possible.

7. Device Results

The viability of the double-barrel VPE reactor has been proven by the impressive list of device results achieved to date. These include routine synthesis of 1.3-μm InGaAsP LEDs, cw lasers and 1.0–1.7-μm InGaAs photodetectors. Table 1 contains device results from six consecutively grown double-barrel VPE lasers. The wavelength was intentionally varied by changing the input vapor flows. All devices lased in the cw mode at room-temperature and the yield of good chips from each wafer was on the order of 50%. Thus, thousands of 1.3-μm cw laser chips were synthesized in the time span of less than one day. (Note that good results were also obtained using InP substrates whose surface orientation was (311), rather than the conventional (100). Superior growth properties,[17] as well as device properties,[18] have been observed with (311) and (511) InP substrates. Reasons for these improvements are discussed in Refs. [17] and [18]).

Nonplanar 1.3-μm laser structures[19] have also been grown in the double-barrel reactor. These structures tend to have lower lasing threshold currents and offer better control of the optical beam due to lateral confinement by variation of the refractive index caused by thickness variations. Fig. 13 shows a power-current curve and an SEM photo from a stained cleavage edge of a VPE 1.3-μm non-

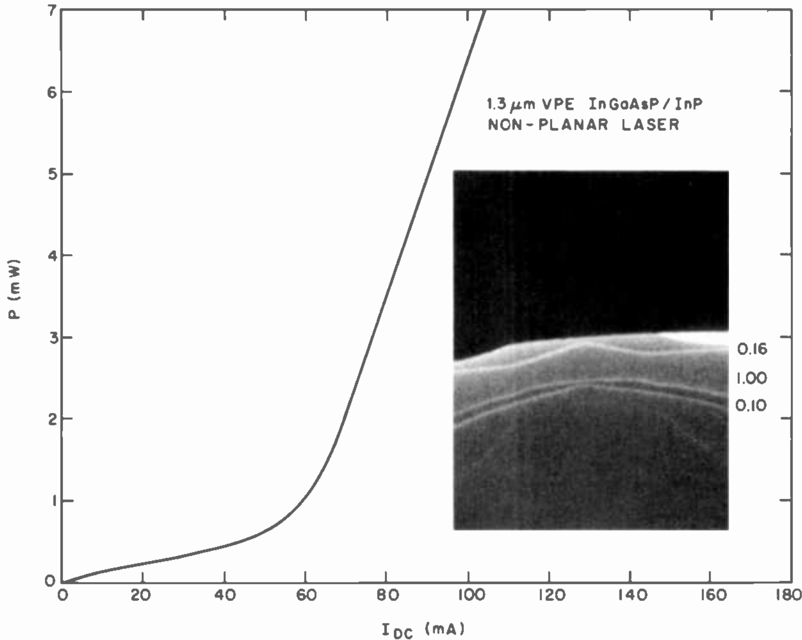


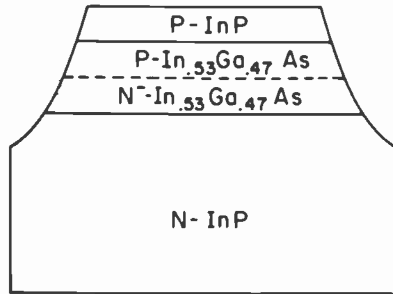
Fig. 13—Power-current curve and SEM stained cleavage photograph of a "non-planar" 1.3-mm cw laser grown in the double-barrel reactor.

planar device grown in the double-barrel VPE reactor over etched mesas in InP substrates. CW lasing thresholds as low as 45 mA have been observed with some structures, while cw power outputs in excess of 120 mW have been observed with others. Over 8 wafers (12 × 18 mm) of this type have been grown that gave cw lasing performance. Some single-mode behavior has also been noted.

High quality 1.0–1.7 μm InGaAs photodetectors[20] have also been synthesized in the double-barrel reactor. Fig. 14 shows a sketch and photo of the structure. Typical values are shown in Table 3.

8. Conclusions

The success of the double-barrel VPE reactor has demonstrated once again that basic materials research can lead directly to improvements in technology and in commercial devices. Basic materials characterization on inferior device structures uncovered crystal defects that were caused by the crystal growth process. Attempts to



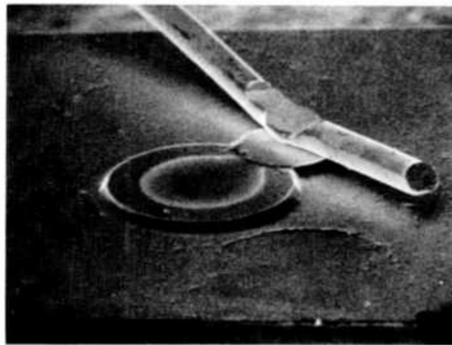


Fig. 14—Sketch and photograph of an RCA VPE 1.0–1.7 μm PIN detector.

eliminate these defects led to the design, construction, and successful demonstration of the double-barrel VPE reactor.

This system can grow III-V compound layers as thin as 60 Å. A complete 1.3-μm cw laser structure can be grown in 30 minutes and more than 15 such structures could be grown in a single day. High

Table 3—Typical Detector Characteristics (−10 V, 22°C)

Leakage Current	10−30 nA
Breakdown Voltage	65−75 V
Quantum Efficiency	60−80%
Capacitance	1 pF
Pulse Rise Time	<0.3 ns
Max. Operating Temperature	>180°C
Noise Equivalent Power (NEP)	<1 pW/Hz$^{1/2}$
Reliability	stable leakage at 60°C for 15,000 hours

performance 1.3-μm lasers and 1.0–1.7-μm photodetectors have been synthesized with the double barrel system.

Acknowledgments

The authors wish to thank their many colleagues at RCA Laboratories for assistance and advice. These include N. J. DiGiuseppe for device fabrication and testing; M. S. Abrahams and C. J. Buiocchi for TEM work; V. S. Ban for collaboration on the initial idea for this system; J. C. Connolly for design and construction of a modular gas flow panel for the double-barrel reactor; and M. G. Harvey for device bonding.

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LPCVD Polycrystalline Silicon: Growth and Physical Properties of In-Situ Phosphorus Doped and Undoped Films

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Abstract—In this application-oriented study we have investigated in-situ phosphorus doped LPCVD polysilicon films deposited in the temperature range from 560°C to 640°C and compared the results with those previously obtained on undoped films. X-ray diffraction, TEM, SEM, Raman and elastic light scattering, optical absorption and reflection, and other techniques were used to obtain information on the grain size, structure, structural perfection, strain, refractive index, surface roughness, and electrical conductivity. We found that to obtain phosphorus doped films of highest quality, deposition in the amorphous form, i.e., at temperatures not exceeding 570°C, is necessary. Of slightly lower quality, but acceptable for less critical applications are films deposited at 580°C $\leqslant T_d \lesssim$ 620°C. Layers deposited at $T_d \gtrsim$ 620°C are considered to be of poor quality.

1. Introduction

The use of high quality polycrystalline silicon layers as gate material, load resistors in memory cells, interconnects and other applications in IC device technology is of rapidly growing importance.

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Low pressure chemical vapor deposition (LPCVD) is the standard preparation method for polysilicon films in IC manufacturing. It has been reported in the literature that amorphous films are undesirable because of uncontrolled crystallization in post-deposition annealing. We have recently shown, however, that undoped polysilicon films deposited in the amorphous phase and subsequently crystallized have the high quality in terms of structural perfection and surface roughness that is required for critical applications.[1,2] In this paper we present results of similar studies on in-situ phosphorus-doped polysilicon films with the aim of providing application oriented recommendations. Using the same characterization methods as were employed for undoped films, we again conclude that deposition in the amorphous phase and subsequent crystallization provide stable films of superior quality.

2. Deposition Conditions

The film depositions were done in a conventional hot wall LPCVD reactor equipped with a 1-m^3 min^{-1} Alcatel double-stage rotary pump. The deposition pressure was kept constant by regulating the pump cross-section with a butterfly valve controlled from a pressure feedback circuit. The deposition temperature was measured inside the deposition tube during the film growth. All depositions were done on two-inch-diameter substrates placed perpendicular to the tube axis and spaced 1/4 inch apart. A deposition tube with an inner diameter of 124 mm was used. Sapphire substrates were chosen for measuring the film thickness, and ⟨100⟩ oriented silicon substrates covered with 300-nm thermally grown SiO_2 were chosen for measuring the physical properties. Phosphorus doped films with a thickness of 0.5 μm were deposited from concentrated monosilane with the addition of 1 vol % PH_3 diluted in N_2. The addition of PH_3 results in a reduction of the growth rate and in film thickness increasing from the wafer center towards the periphery. The growth experiments were done at deposition temperatures T_d = 560, 570, 580, 600, 620, and 640°C. Other deposition parameters were a pressure of 500 mT, SiH_4 = 300 cm^3 min^{-1}, and a dopant gas flow ratio of $PH_3/SiH_4 = 8 \times 10^{-4}$.

These process conditions are a compromise between the growth rate, the radial thickness uniformity, and the electrical conductivity of the films. The film thickness was measured with a Dektak surface profile monitor, as described previously[1] for undoped material. The growth rate as a function of the deposition temperature is shown in Fig. 1. The derived apparent activation energy of 44.6 kcal/Mol is

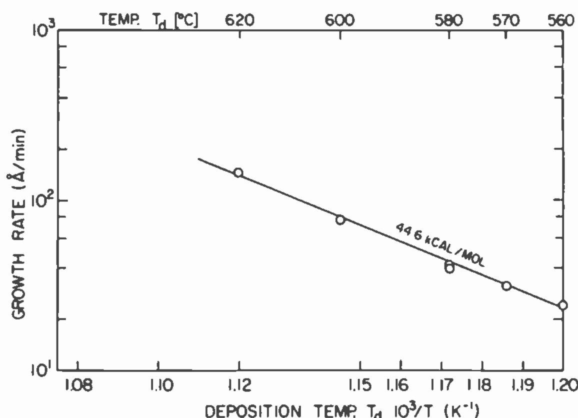


Fig. 1—Growth rate as a function of deposition temperature T_d for in-situ phosphorus-doped films. Deposition conditions: PH_3/SiH_4 = 8 × 10^{-4}, SiH_4 = 300 cm³ min⁻¹, deposition pressure 500 mT, substrate spacing 1/4 inch.

slightly larger than the 32–40 kcal/Mol which we reported for undoped material.[1]

The radial film-thickness variation was measured with the optical thickness monitor described by Sandercock.[3] The refractive index required for this method was obtained from correlation with the Dektak surface profile monitor thickness readings. The radial film-thickness variation of doped films as a function of deposition temperature is shown in Fig. 2. For comparison we have included the

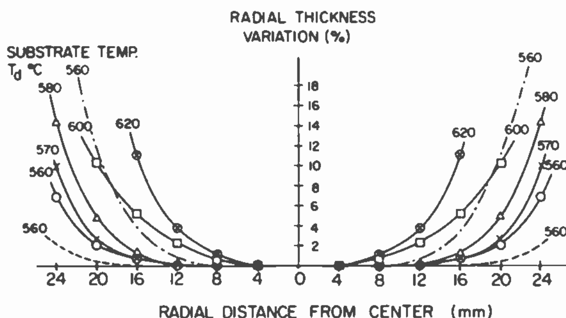


Fig. 2—Radial film thickness variation for in-situ phosphorus-doped films as a function of deposition temperature T_d. Deposition conditions: PH_3/SiH_4 = 8 × 10^{-4}, SiH_4 = 300 cm³ min⁻¹, system pressure 500 mT, substrate spacing 1/4 inch. The — - — - — curve shows the variation with a SiH_4 flow rate of 100 cm³ min⁻¹. The --- curve is for undoped, T_d = 560°C.

curve for undoped films deposited at 560°C which shows that the nonuniformity with the addition of phosphorus is considerably larger. The improvement of the thickness uniformity with increasing SiH_4 flow rate can be seen by comparing the curve for 100 $cm^3 min^{-1}$ SiH_4 deposited at 560°C with the curve for the normally used 300 $cm^3 min^{-1}$ SiH_4. Higher flow rates up to 500 $cm^3 min^{-1}$ might improve the thickness uniformity even further but would require a larger pump (e.g., a Roots blower) to handle the gas load.

3. Thermal Annealing

The Si/SiO_2 substrate wafers were cleaved after film deposition into four equal parts prior to thermal recrystallization and characterization. One part was kept in the as-grown state, while the others were annealed at T_a = 900, 950, and 1000°C for 30 min, respectively. It is important that such annealing treatments be done in a slightly oxidizing atmosphere with N_2 + 0.5 vol % O_2 in order to prevent the outdiffusion of the phosphorus. The thin SiO_2 films formed during these annealing treatments (<400 Å) were not removed prior to the characterization except for resistivity measurements.

4. X-Ray Diffraction and Transmission Electron Microscopy (TEM)

X-ray diffraction was used to examine the degree of crystallinity, crystallite size and texture (preferred orientation) of the as-grown and annealed layers (T_a = 900, 950, and 1000°C). The three most intense reflections from the {111}, {220} and {311} planes were recorded for each layer. The crystallite sizes D_{hkl} were determined from the width of the *hkl* lines by using the Scherrer formula; texture and degree of crystallinity were determined from the relative line intensities.[1]

TEM techniques (bright field, dark field, and selected area diffraction) were used to determine at various depths of the polysilicon layers the average crystallite size $\bar{S}$, the crystallite size distribution, and the degree of crystallinity. These investigations were performed[1] for as-grown layers and for those annealed at 1000°C.

The results of the X-ray diffraction and TEM measurements for phosphorus doped layers, shown in Figs. 3 through 8, are summarized in Table 1. Some of the results are very similar to those observed for undoped layers.[1,2] For example, as-grown layers deposited at 560° or 570°C are X-ray amorphous (no X-ray line intensity),

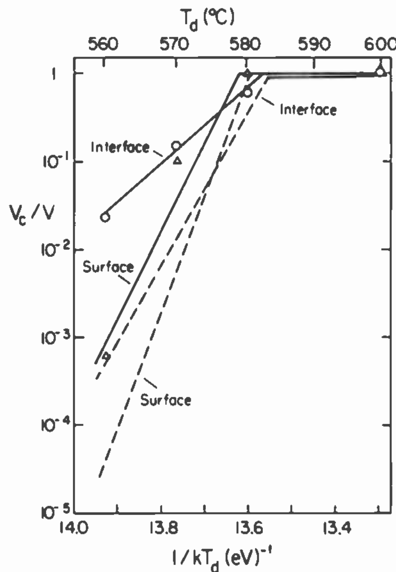


Fig. 3—Solid curve shows crystalline volume fraction V_c/V of phosphorus doped LPCVD silicon layers versus reciprocal deposition temperature, given by $1/kT_d$. Undoped layers (dashed curve) are shown for comparison.

although some crystallites are observed by TEM. Layers deposited at 580°C are mixed amorphous/crystalline, and layers deposited at 600°C or higher appear to be fully crystalline. Note, however, that the crystalline volume fraction V_c/V is somewhat higher for phosphorus-doped layers deposited at low temperatures ($T_d \leq 580°C$) than for the corresponding undoped layers (Fig. 3), i.e., in-situ phosphorus doping seems to slightly enhance crystallization (compare also results from Raman scattering). In terms of grain orientation only a weak texture is observed for deposition temperatures up to T_d = 620°C (⟨311⟩ for T_d = 580°C, ⟨111⟩ for T_d = 600°C, and ⟨111⟩ or ⟨311⟩ for T_d = 620°C), while a pronounced ⟨311⟩ texture is observed for layers deposited at 640°C (Table 1). This is in contrast to undoped layers deposited at 620°C for which a pronounced ⟨110⟩ texture was observed. The grain sizes D_{hkl} for phosphorus doped layers range between 200 and 1000 Å as compared to 100 and 770 Å for undoped layers. The grain size distribution for a layer deposited at 600°C is shown in Fig. 4.

Again, as in the case of undoped layers, all *annealed* layers are polycrystalline and their texture depends only slightly on the annealing temperatures. Furthermore, annealing favours the ⟨111⟩ texture for low temperature layers ($T_d \leq 600°C$). Layers deposited

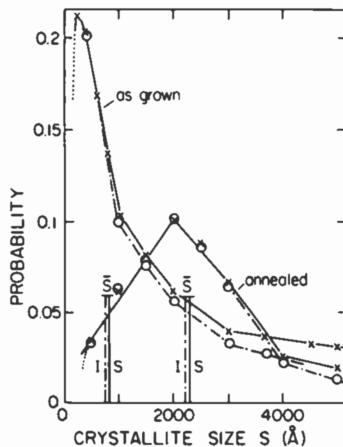


Fig. 4—Grain size distribution for a phosphorus-doped LPCVD silicon layer deposited at T_o = 600°C, as-grown and annealed at T_a = 1000°C (X = surface S, O = interface I).

in the polycrystalline form mainly preserve their preferred orientation, as expected, since the original deposition imposes some constraints on further grain growth: 600°C layers have a ⟨111⟩ texture, 620°C layers an equal number of ⟨111⟩ and ⟨311⟩ oriented grains, and 640°C layers exhibit a pronounced ⟨311⟩ texture.

In contrast to undoped layers, however, annealing increases the average grain size and changes the grain size distribution of all layers considerably (see Figs. 4 and 5). No correlation between the texture and the largest grain dimension could be found from the measurements. Average grain sizes as large as 3000Å are measured, with X-ray techniques, as well as by TEM (Figs. 4, 5, 6, and 7). Although grain sizes determined by X-ray line broadening can easily be off by a factor of two for values larger than about 1000 Å, we found a surprisingly good agreement between $\overline{D}$ (X-ray) and $\overline{S}$ (TEM)[2] measurements for large grain sizes (Table 1 and Fig. 8). Only phosphorus doped layers deposited at 620°C exhibit average TEM grain sizes $\overline{S}$ twice as large as the corresponding average X-ray grain sizes $\overline{D}$. This observed difference probably occurs because relatively many more grains smaller than $\overline{S}$ are found for the doped 620°C layers than for all other doped layers.

As in the case of undoped layers, we conclude from X-ray and TEM investigations that crystallization of amorphous or mixed amorphous/crystalline films does not lead to unreproducible structures; on the contrary, such films can be thermally converted into reproducible, stable polycrystalline films. For VLSI the large grain

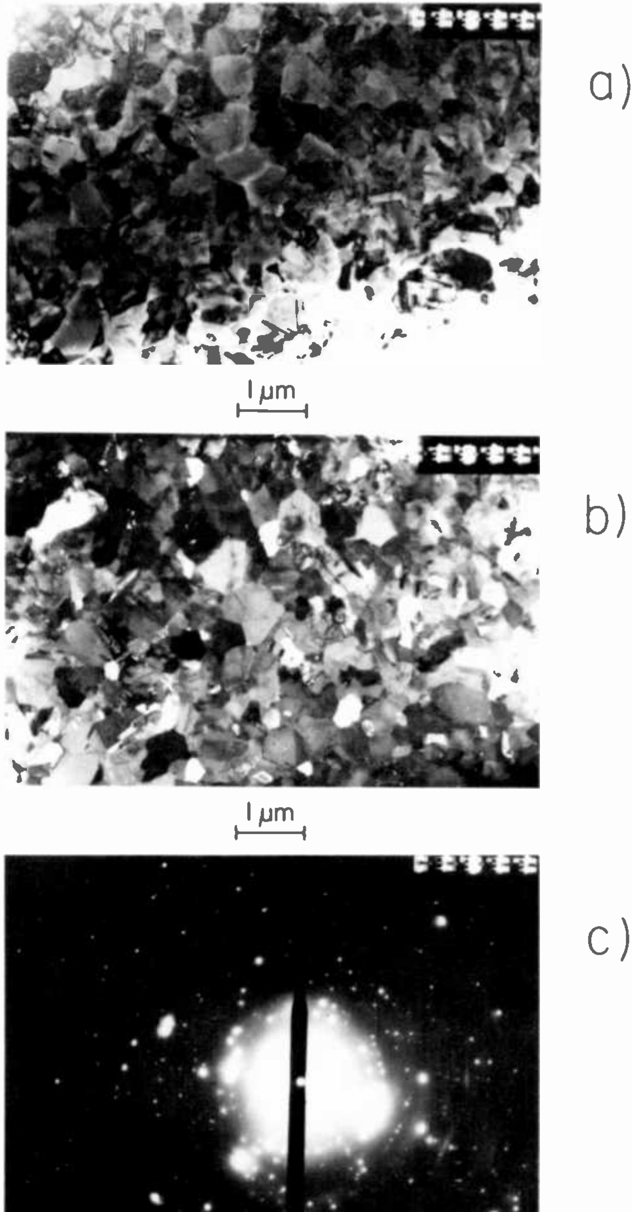


Fig. 5—(a) Bright field, (b) dark field, and (c) selected-area diffraction micrographs taken at the surface for a phosphorus-doped LPCVD silicon layer deposited at 560°C and annealed at T_a = 1000°C.

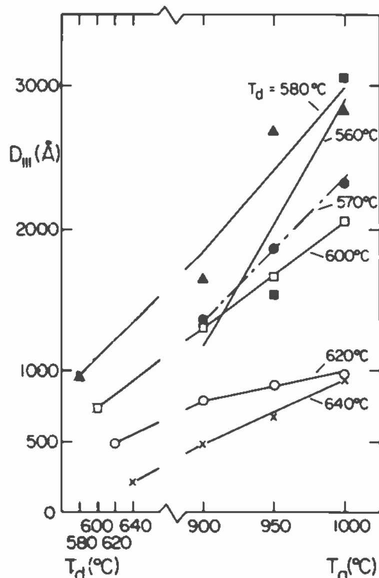


Fig. 6—X-ray grain size D_{111} as a function of deposition and annealing temperature for phosphorus-doped LPCVD silicon layers.

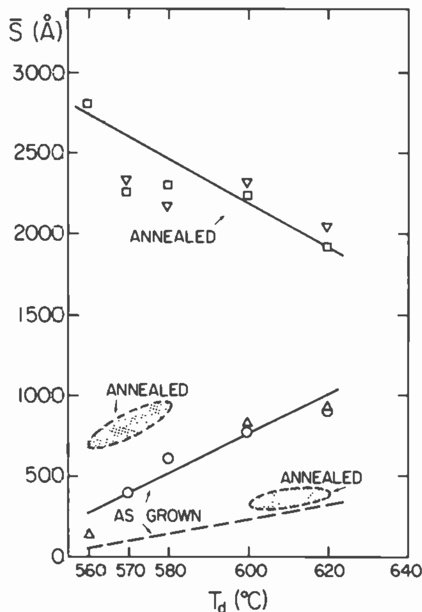


Fig. 7—Average crystallite size $\bar{S}$ for phosphorus-doped LPCVD silicon layers as-grown (O = interface, Δ = surface) and annealed at 1000°C (□ = interface, ∇ = surface) as a function of deposition temperature T_d. Undoped layers (dashed lines) are shown for comparison.

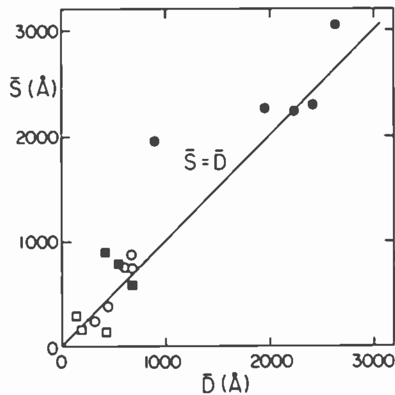


Fig. 8—Average grain size $\bar{S}$ evaluated from TEM versus average grain size $\bar{D}$ evaluated from X-ray diffraction. The data include the following samples: □ undoped as-grown, ○ undoped annealed, ■ phosphorus-doped as-grown, and ● phosphorus-doped annealed.

size of the annealed doped layers might seem to be problematic. However, since the surface roughness of these films ($T_d \leq 600°C$) is small (see Sec. 7), this fact will probably not be a serious problem.

Baudrant and Sacilotti[4] have also reported on in-situ phosphorus-doped LPCVD films deposited at ≅623°C. These authors used gas flow rates and, hence, deposition rates different from ours, however, and one cannot compare the respective film properties.

5. Light Scattering

5.1 Raman Scattering

The benefits of Raman scattering for the characterization of LPCVD polycrystalline silicon films, as grown or annealed, are based on the following points:[1,2]

- The degree of crystallization (amorphous, crystalline or mixed) can be judged in a few minutes by inspecting the Raman spectrum. A sharp peak at 522 cm^{-1} indicates a fully crystalline, a broad line at 483 cm^{-1} a fully amorphous layer, and a superposition of the two indicates mixed crystallization.
- The crystalline perfection of the films after annealing, apart from elastic scattering (see Sec. 5.2), can be read from the value of the peak intensity of the Raman line above background.
- The amount of lattice distortion and internal strain remaining in the films after annealing is apparent from a Raman line shape analysis. Material of low distortion and strain will exhibit a line

Table 1—Grain Size and Texture of Phosphorus Doped Layers by X-Ray Diffraction and TEM Measurements

	X-ray						TEM
T_d (°C)	$\bar{D}$ (Å)	D_{111} (Å)	D_{220} (Å)	D_{311} (Å)	Texture		$\bar{S}$ (Å)
As grown							
560	—	X-ray amorphous			—		140
570	—	X-ray amorphous			—	i s	2000 × 400 1600 × 400
580	670	960	610	430	⟨311⟩	i s	600 4900
600	580	835	460	450	⟨111⟩	i s	770 820
620	420	480	470	310	⟨311⟩ ⟨111⟩	i s	890 910
640	280	220	400	220	⟨311⟩		—
Annealed at 1000°C							
560	2650	3060	3050	1850	⟨111⟩	i s	2800 3300
570	2430	2330	2450	2530	⟨111⟩	i s	2260 2330
580	2250	2840	2060	1850	⟨111⟩	i s	2300 2170
600	1960	2440	1690	1760	⟨111⟩	i s	2240 2300
620	910	980	760	1000	⟨111⟩ ⟨311⟩	i s	1900 2040
640	940	950	1300	580	strong ⟨311⟩		—

D_{hkl} = grain size evaluated from the X-ray diffraction line (hkl) according to the Scherrer formula (see text)
$\bar{D}$ = average grain size evaluated from X-ray diffraction
$\bar{S}$ = average grain size evaluated from TEM measurements
i = measured at the interface
s = measured at the surface

shape resembling bulk single-crystal material. Strong and extended tails of the Raman line in annealed films, on the other hand, indicate that the material is highly distorted or strained and is undesirable for critical applications.

The standard Raman scattering technique[5] has been employed with 100 mW of 5145 Å laser light focused onto a spot 50 μm × 2 mm on the film. This power density is below the threshold for thermal crystallization, as we have verified. The light penetration depth into the films amounts to the reciprocal absorption coefficient to be discussed below.

The results for *undoped* polysilicon films, which are presented elsewhere,[1,2] can be summarized as follows. The *as-grown* low-tem-

perature-group films ($T_d \leq 580°C$) are found to be fully Raman amorphous, while some films in the high-temperature group ($T_d \geq 600°C$) are observed to be fully crystalline. *After annealing* (T_a = 900 to 1000°C), the low-temperature group exhibits a line shape close to single-crystal material. The high-temperature group, however, shows strong line shape tails which, when integrated, exceed bulk silicon by as much as 26%. This material, $T_d \geq 600°C$, was considered to be internally distorted and highly strained and unsuitable for device applications.

The corresponding results for in-situ phosphorus-doped polysilicon are shown in Figs. 9, 10 and 11. Fig. 9 shows the peak Raman line intensity. Any intensity above the amorphous value of 25 counts/sec is due to crystalline contributions. Compared to undoped material, the transition region from amorphous to crystalline is found to occur at 20 degrees lower temperature. A deposition at 580°C of phosphorus-doped films results in mixed amorphous/crystalline layers (as observed by Raman scattering); for $T_d \geq 600°C$, layers are fully crystalline. After annealing at 900 to 1000°C, all layers are crystalline with a deposition-temperature dependence of intensity (see upper part of Fig. 9) that differs somewhat from undoped. This may be related to the fact that the texture variation with T_d for doped layers (see Table 1) has also changed from that for undoped polysilicon.

To learn about the amount of strain and lattice distortion left in the layers after annealing at 900 to 1000°C (a factor that is very

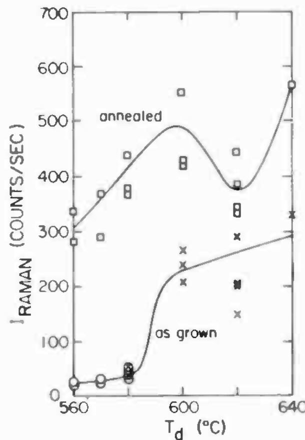


Fig. 9—Raman peak intensity for as-grown and 900 to 1000°C annealed phosphorus-doped polysilicon layers versus deposition temperature: ○ = amorphous, X, □ = crystalline, ⊗ = mixed.

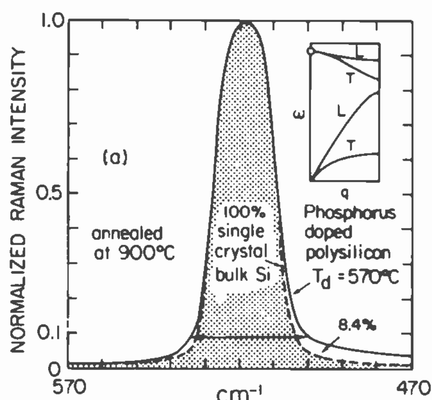


Fig. 10—Raman line intensity versus wavenumber of annealed (900–1000°C) low-temperature deposited (T_d = 570°C) phosphorus-doped polysilicon layer compared to single-crystal bulk silicon (dotted area). Note that the linewidth shown is to be taken as a relative measure due to the averaging process. The inset shows silicon phonon dispersion curves.

important for device applications), we again analysed the Raman lineshapes. Fig. 10 shows the results for layers deposited at T_d = 570°C in comparison to bulk single-crystal silicon, the phonon dispersion curves of which are given in the inset. The effect of strain and distortions is given by the tails on both sides of the line, mostly on the low-frequency (low-wavenumber) side. It represents an increase in area of 8.4%, which is very close to what had been found for the undoped low-temperature group. The high-temperature phosphorus-doped group shows a value of 12.5%, which is con-

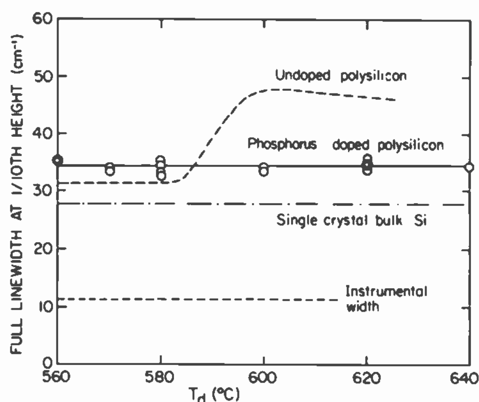


Fig. 11—Raman linewidth of annealed layers (900–1000°C) of phosphorus-doped polysilicon versus deposition temperature, and comparison with undoped polysilicon layers.

siderably smaller than found for undoped films (25.7%). This is seen more easily in Fig. 11, which presents the full linewidth at 1/10th maximum height (given by the arrow in Fig. 10) versus deposition temperature. Interpreted in the same manner as before,[1] we find that after annealing the phosphorus-doped polysilicon exhibits slightly more strain than undoped polysilicon; however, strain does not show much dependence on deposition temperature. The phosphorus doping seems to have partly prevented the poor crystallization previously observed for the layers deposited at $T_d \geqslant 600°C$.

5.2 Elastic Scattering

The technique of elastic light scattering can be used to determine the structural perfection of polysilicon layers.[1,2] In addition to intrinsic elastic scattering due to temperature or entropy fluctuations, extrinsic elastic scattering is produced by all kinds of structural imperfections of the bulk, e.g., mosaic misorientation, twinning, strain, grain boundaries, stacking faults, and dislocations (in general, all effects resulting in changes in refractive index), as well as by local defects. For the present case of rather smooth surfaces, we have found that the above volume effects dominate over scattering from surface roughness. As an example of the power of this technique for structural perfection analysis, we refer to work on SOS wafers where we have shown[6,7] that elastic light scattering is strongly correlated with UV reflectivity, which had previously been shown to be correlated[8] with the twinning density and the device yield.

Elastic light scattering measurements on polysilicon layers were performed by two methods. In the first, the spectrometer method, the same arrangement, power, and spot size were used as given above for Raman scattering except for an additional 10^6 to 10^8 attenuation filter inserted in front of the photomultiplier. The scattered elastic intensity is then recorded for the various wafers. In the second method, which uses the laser scanner in the quality control mode,[6,7] laser light falls onto the spinning wafer while being translated. The scattered elastic light originating from the bulk (i.e., not from dust or individual defects) is used as a measure of the crystalline perfection. Both methods were found to correlate extremely well.[7]

The results for *undoped* polysilicon films, which are presented elsewhere,[1,2] show that the best structural perfection (i.e., lowest elastic light scattering) is observed for Raman amorphous films ($T_d \leqslant 580°C$) and the worst (i.e., very much higher elastic intensity) for fully crystalline films grown at $T_d \geqslant 620°C$. The annealing procedure leaves the structural perfection unchanged.

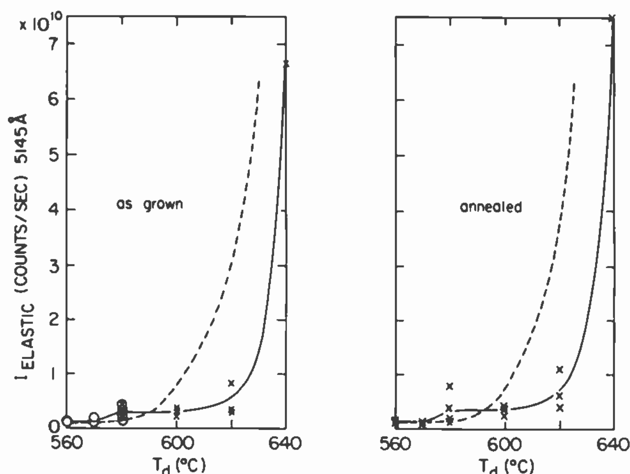


Fig. 12—Elastic light scattering peak intensity for as-grown (left) and annealed (right) phosphorus-doped polysilicon layers versus deposition temperature: O = amorphous, X = crystalline, ⊗ = mixed. The dashed curve is for undoped films.

The results for the *phosphorus doped* films discussed here are shown in Fig. 12 for as-grown and annealed material. These results were obtained with the spectrometer method and are compared with undoped layers. The gross features are quite similar. Again the low-temperature group $T_d \leq 570°C$ is of much better perfection than the high-temperature group ($T_d \geq 620°C$). The sharp increase in scattering intensity (i.e., decrease in perfection) occurs for doped material at a 20°C higher deposition temperature. Second, there is a slight increase in scattering (decrease in perfection) observed at 580°C, showing that $580 \leq T_d \leq 620°C$ provides material of intermediate structural quality. The structural perfection is unchanged with annealing, as for undoped material.

Fig. 13 shows the correlation of these elastic scattering results with those for Raman scattering for as-grown phosphorus doped films. It is seen that the data correlate quite well in the sense that low-temperature *amorphous* grown films are of high structural perfection, while high-temperature crystalline films are of rather poor structural perfection. Even the small step from 570 to 580°C can be recognized.

The results of the scanner method in the quality control mode are in full agreement with these findings; they will be published elsewhere in detail.[7] Since it allows rapid characterization of the films in terms of quality, this method is in fact most useful for production environments. Undoped polysilicon, as-grown or annealed, would

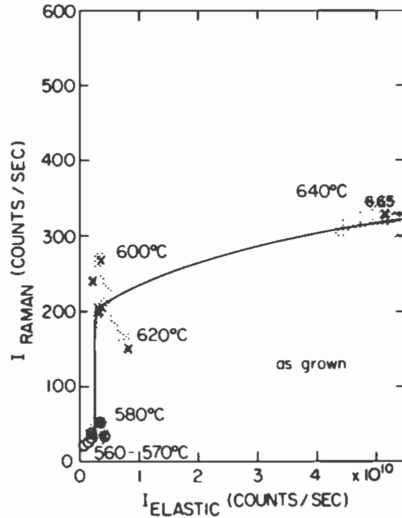


Fig. 13—Correlation between Raman and elastic intensity for as-grown phosphorus-doped polysilicon layers: ○ = amorphous, ⊗ = mixed, X = crystalline.

be acceptable for blossom "Threshold I" values of ≥570 units; they are unacceptable for <300 units. The corresponding figures for phosphorus doped polysilicon are highly acceptable for ≥450 units, of medium quality for >300 units, and unacceptable below 300 units.

The elastic light scattering data thus lead to the result that the structurally most perfect phosphorus-doped polysilicon should be deposited at T_d not exceeding 570°C. This should be considered for applications where extreme perfection is required. The next deposition temperature range, $580 \leq T_d < 620$°C, provides material of reasonable structural perfection that may be sufficient for many applications. The structural perfection of films deposited at T_d = 640°C is considered to be poor (see also the next section on optical absorption).

6. Optical Absorption and Refractive Index

6.1 Optical Absorption

To judge the light penetration depth for film characterization with Raman and elastic light scattering, we have measured the optical absorption at the two wavelengths involved in these measurements (5145 Å and 4416 Å). For this, we have grown polysilicon layers on quartz glass substrates concurrently with the layers grown on silicon/silicon oxide substrates. The absorption coefficient was then

determined from combined transmission and reflection measurements.

The results for *undoped* polysilicon are presented elsewhere.[1] It was found, in good agreement with light scattering, that the absorption coefficient of annealed films is close to bulk silicon for the low-temperature group ($T_d \leq 580°C$), while it is considerably higher for the high-temperature group ($T_d \geq 600°C$). The latter is believed to predominately originate from the large distorted volume portions, discussed in the previous section. These distorted regions of structural imperfection in the high-temperature group films give rise to a sizeable amount of internal scattering which results in a reduced transmission and an increased effective absorption coefficient.

For *phosphorus doped* polysilicon, the corresponding data of the

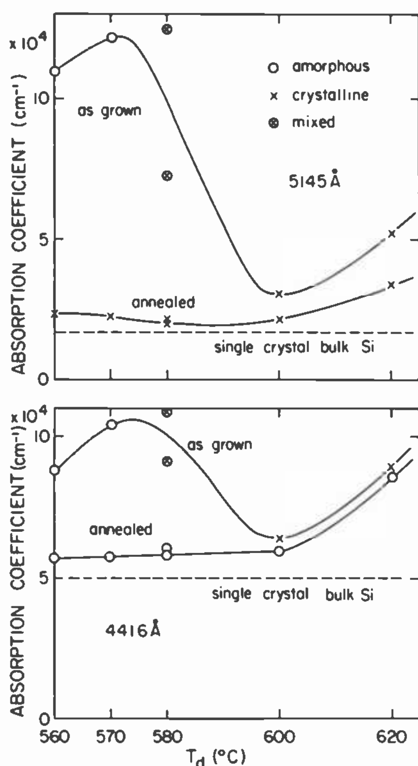


Fig. 14—Absorption coefficient of in-situ phosphorus-doped polysilicon versus deposition temperature, as-grown and annealed (900–1000°C), at 5145 Å (i.e., for Raman scattering) and at 4416 Å (i.e., for the scanner method).

present work are shown in Fig. 14 for wavelengths of 5145 Å (corresponding to Raman scattering and the spectrometer method of elastic scattering) and of 4416 Å (corresponding to the laser scanner). The light penetration depth can easily be read from this figure as the inverse absorption coefficient. It is seen in Fig. 14 that the annealed films at both wavelengths behave differently from undoped layers in the sense that the absorption coefficient is bulk-silicon-like over the whole range from T_d = 560°C to 600°C, confirming that over this whole range the films are at least of medium acceptability. The very good quality of the films for $T_d \leqslant 570°C$ as compared to $580 \leqslant T_d \leqslant 600°C$ does not show up, in contrast to what had been seen in elastic scattering (Fig. 12). For $T_d \geqslant 620°C$, however, a sharp increase in absorption occurs indicating inferior film quality, which is in accordance with the findings of the structural perfection studies.

6.2 Refractive Index

The refractive index is of importance for routine thickness measurements using the optical thickness monitor described by Sandercock.[3] The effective refractive index was measured on as-grown films as a function of the film deposition temperature by relating the optical thickness t_{opt} for $n = 1$ (as measured with the optical monitor) to the thickness reading with the Dektak surface profilometer t_{eff}, according to $n_{eff} = t_{opt}/t_{eff}$. The results, given in Fig. 15, show three distinct regions: $n_{eff} \cong 3.9$ for amorphous material deposited at $T_d \leqslant 580°C$; a transition region for T_d = 580 to 600°C, where the material is deposited with a mixed amorphous/crystalline

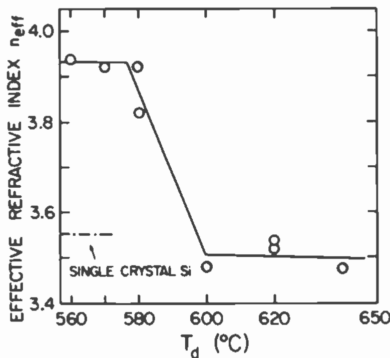


Fig. 15—Effective refractive index n_{eff} as a function of deposition temperature T_d for as-grown films.

structure; and $n_{eff} \cong 3.5$ for $T_d \geqslant 600°C$ for crystalline material. It is obvious that the large change in refractive index can also be used to get rapid information on whether the deposited material is amorphous or polycrystalline.

7. Surface Roughness

It has been shown by various authors that "bumps" and asperities on the initial polysilicon surface texture are determining factors for the poly-oxide interface and dielectric strength of the oxide. The surface roughness of polysilicon films and their characterization are therefore of particular importance for subsequent processing. There is a vast amount of literature on the measurement of surface roughness by mechanical, optical, and other techniques.

For very smooth surfaces, which are desired for the application to high-density ICs, optical techniques are preferable because of higher sensitivity and accuracy combined with their nondestructive and contactless nature. The total intensity and angular dependence of light scattered from surfaces with microirregularities whose heights are much smaller than the wavelength of the incident light and whose lateral dimensions are comparable to or greater than a wavelength can be explained by diffraction theory.[11]

Another optical technique makes use of the coupling of light to surface plasmons at a metal or metal-covered surface. A surface plasmon is a quantized collective oscillation of the electrons. It can also be viewed as a polarization wave propagating along the surface and carrying an electric field that is part longitudinal and part transverse. Surface plasmons cannot be excited by light on ideally smooth surfaces, but surface roughness provides the mechanism to conserve momentum tangential to the surface. This coupling causes dissipation of electromagnetic energy resulting in a loss of reflected light in the spectral region of the surface plasmon frequency. Many authors[12] have used silver films as metal layer covering the surface under study, since the surface plasmon frequency corresponds to a very convenient wavelength region of $\lambda = 3500$ Å. Equally important is the evidence that the evaporated silver film conforms to the contours of the original surface with an accuracy of a few Å, and further, adds no structure of its own.[13] The photon—surface-plasmon coupling is, in contrast to light scattering, strongest for lateral dimensions smaller than the wavelength of incident light.[11] The low spatial wavelength cut-off is of the order of the Fermi wave vector, i.e., a few Å, but in practice it is also influenced by the continuity, height distribution, and slope distribution of the surface.

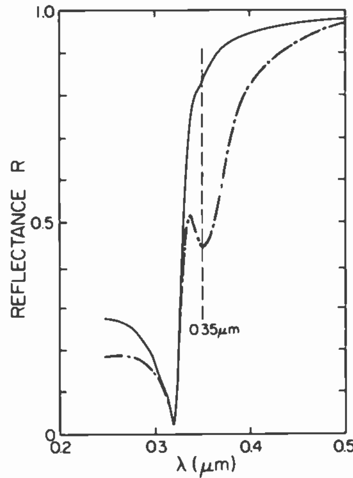


Fig. 16—Reflection of undoped silvered polysilicon films versus wavelength. The solid line is for T_d = 560°C; the dashed line is for T_d = 620°C, T_a = 950°C.

We have evaporated a silver layer of 700 to 1000 A thickness onto the surface of as-grown and annealed silicon films and then measured the reflectance. To illustrate the results, we show in Fig. 16 the reflectance spectra of two undoped silvered films in the wavelength range from 0.2 to 0.5 μm. Common to both curves is the long-wavelength part and the lower part of the steep volume plasma edge of λ = 0.32 μm. The solid line represents an as-grown film deposited at T_d = 560°C. It shows only a small indention at the surface plasmon wavelength λ = 0.35 μm. The dashed line is from an undoped film grown at T_d = 620°C and annealed at T_a = 950°C. We observe a dramatic loss of reflection, ΔR, due to stronger surface plasmon excitation which, in turn, is caused by much higher surface roughness in comparison to the low-T_d film. On the basis of this spectral dependence, it sufficed to determine the surface roughness on all films by a reflection measurement only at λ = 0.35 μm after silver evaporation. The reflection loss was normalized to the reflection value of a reference sample that is freshly silvered in each evaporation run together with the batch of unknown samples. As roughness standards we used a "superpolished" SiC mirror[14] (courtesy of W. J. Choyke, Westinghouse Research Laboratories, Pittsburgh, Penna.) with a root-mean-square surface roughness σ_{rms} = 5 to 8 Å, determined from total laser scattering intensity, and polished quartz plates with σ_{rms} = 8 to 10 Å. The root-mean-square surface roughness σ_{rms}, in the following denoted as σ, is defined by $\sigma^2 = \langle z^2 \rangle$ where z is the surface height relative to the mean surface level at

$z = 0$. The σ values of our films were obtained by using the calibration curve between ΔR and σ established by Cunningham and Braundmeier[15] who used the interferometric method of observation of fringes of equal chromatic order (FECO) to determine σ.

Fig. 17 shows the σ values of in-situ phosphorus-doped films (points and solid line) compared to undoped films[2] (dashed line) versus deposition temperature T_d. There is no difference between as-grown and annealed films outside of a small local variation of 1 to 2 Å. We see that σ values less than 15 Å can be reliably achieved only at deposition temperatures $T_d \leq 580°C$, as was the case for undoped films. These films are amorphous or mixed as-deposited, but the important point for critical device applications is that the smooth surface is preserved in the annealing process. In contrast to the undoped films, however, σ values smaller than 25 Å are still obtained up to $T_d = 620°C$, and the sharp transition to very rough films with σ values in excess of 70 Å occurs at $T_d = 625°C$. There seems to exist a correlation between excessive surface roughness and the occurrence of a strong texture. Undoped films had a very rough surface for $T_d = 620°C$ where a strong ⟨110⟩ texture and columnar growth[16] were observed. In-situ phosphorus doped films grown at $T_d = 640°C$ again have a high roughness and a strong

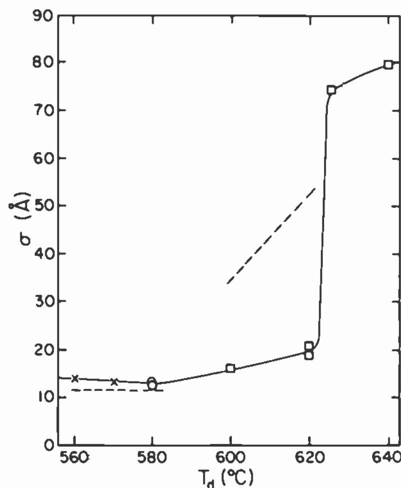


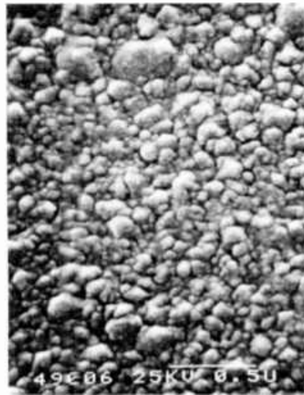
Fig. 17—Root-mean-square surface roughness σ of in-situ phosphorus-doped polysilicon films (as grown and annealed at 900–1000°C) versus deposition temperature; X = amorphous, ○ = mixed, □ = crystalline. The dashed curve illustrates data obtained on undoped films.

texture, this time of the ⟨311⟩ type. At this moment we do not want to overemphasize this correlation for the simple reason that we have not grown films at higher temperatures in either case.

As in the undoped films the surface roughness is not changed by the annealing process. This is surprising, particularly for the supersmooth, initially amorphous films that crystallize during annealing. It is even more surprising for the phosphorus-doped films, since the grain growth is strongly enhanced by the presence of phosphorus. The average grain size for $T_d \leq 570°C$ after annealing is 2000 to 3000 Å (see Table 1), which is a factor of 3 to 4 higher than for undoped films.[2] There is even an appreciable number of grains of a size around 5000 Å, i.e., of the order of the film thickness; and the surface roughness is still no more than $\sigma = 15$ Å. Since the peak-to-valley roughness is only a few times the value of σ, it amounts to just about 1% of the largest grain sizes. This surprising result can only be understood by crystallization phenomena near the surface such that the nucleation and growth of the crystallites are accommodated within the initially smooth contour.

The photon–surface-plasmon technique yields one number characterizing the vertical roughness; it does not give numerical information on the lateral structure. For this reason it is necessary to complement it by another technique, such as electron microscopy, to characterize the lateral structure. As for undoped films,[1] surface replica of the polysilicon films have been shadowed by oblique evaporation of platinum of 10 to 20 Å thickness. TEM micrographs of the shadowed replica show typical lateral dimensions of 100 to 300 Å for $T_d \leq 580°C$, 300 to 1000 Å for $600°C \leq T_d \leq 620°C$, and peak-to-valley roughnesses that are in good agreement with the optically determined values. (The technique has not been applied to films for $T_d > 620°C$.) A direct visual impression can also be gained from high-resolution SEM micrographs. Fig. 18 shows micrographs of the sample surface after the 1000°C anneal. It can be seen that the lateral dimension of the $T_d = 560°C$ film is typically about 200 Å. The $T_d = 625°C$ film has a far rougher appearance with lateral dimensions of 1000 to 2000 Å size. It seems fair to expect a smoother poly-oxide interface if an oxide is grown from the initially amorphous low-T_d material.

Rapid characterization of the surface roughness is possible by means of the UV Reflectometer, which had originally been developed to measure the near-surface crystallinity of silicon on sapphire.[8] The UV characterization of polysilicon is described in a separate article in a previous issue.[17]



a)

b)

Fig. 18—SEMs of the surface of in-situ phosphorus-doped polysilicon films annealed at T_d = 1000 after deposition at (a) T_d = 625°C, crystalline and (b) T_d = 560°C, amorphous.

8. Electrical Conductivity

The electrical conductivity at room temperature for the as-grown phosphorus doped films was measured with an evaporated-aluminum gap structure, as shown in the insert of Fig. 19. The thermally crystallized material, because of the high conductivity, could be measured directly with a 4-point probe. The films were given a buffered HF treatment prior to these measurements in order to remove existing surface oxides. The conductivity as a function of growth and annealing temperatures is shown in Fig. 19. With respect to the growth temperature, there are three distinct regions: a

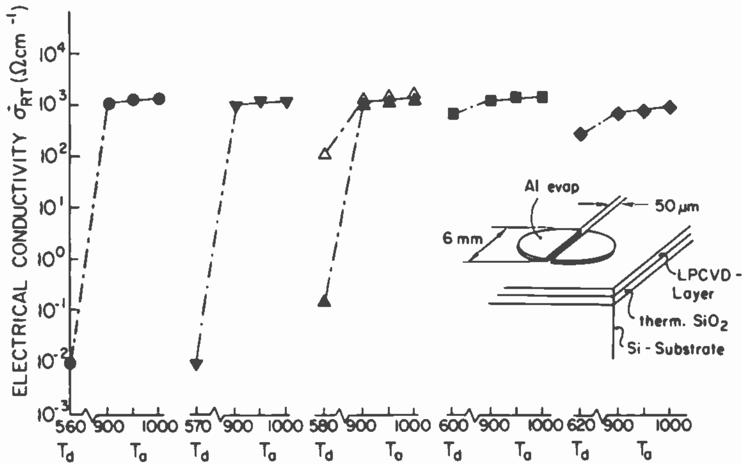


Fig. 19—Room-temperature electrical conductivity for in-situ phosphorus-doped films. T_d is the deposition temperature (°C), T_a is the annealing temperature (°C), and the deposition conditions are as follows: PH_3/SiH_4 = 8 × 10^{-4}, SiH_4 = 300 cm^3 min^{-1}, system pressure 500 mT, substrate spacing 1/4 inch.

low-temperature region with $T_d \leq 570°C$, where the material is fully amorphous (X-ray & Raman) with a low conductivity around 10^{-2} $(\Omega\ cm)^{-1}$; a transition region for T_d = 580°C, where the material has a mixed amorphous/crystalline structure with a conductivity between 10^{-1} and 10^2 $(\Omega\ cm)^{-1}$; and a region for $T_d \geq 600°C$, where the material is fully crystalline with a corresponding high conductivity between 10^2 and 10^3 $(\Omega\ cm)^{-1}$. Of interest for practical applications is the highest achievable conductivity for annealed material. Annealing treatments in N_2 + 0.5 vol % O_2 in the range of 900–1000°C results in a conductivity δ = 1–1.25 × 10^3 $(\Omega\ cm)^{-1}$. The corresponding sheet resistivity for a 0.5-μm thick film is 16–20 Ω/□. The conductivity decreases slightly as the growth temperature is increased above 600°C.

9. Conclusions

The growth conditions and physical properties of both as-grown and annealed in-situ phosphorus doped films are summarized in Tables 2 and 3 and can be compared with the corresponding conditions and properties for undoped films in Tables 4 and 5. The conclusions drawn from this detailed investigation are roughly similar to what has been given for updoped polysilicon[1,2] in the sense that the deposition in the amorphous phase provides the best properties of the

Table 2—Properties of Phosphorus-Doped As-Grown Films: SiH_4 = 300 cm^3/min, $PH_3/SiH_4 = 8 \times 10^{-4}$, p = 500 mT, substrate spacing = 1/4 inch

Properties	$T \leq 570°C$	$580 \leq T_d \lesssim 620°C$	$T_d \gtrsim 620°C$
Growth rate	25–32 Å/min	40–75 Å/min	143 Å/min
Effective refractive index	3.93	3.85–3.5	3.5
Typical radial thickness uniformity	7–10%	14–18%	>20%
Structure	amorphous	mixed amorphous/ crystalline	polycrystalline
Average grain size	—	700–5000 Å	300–900 Å
Preferred grain orientation	—	⟨311⟩, ⟨111⟩	⟨311⟩
Surface roughness (rms)	<15 Å	<20 Å	>70 Å
Electrical conductivity	10^{-2} (Ω cm)$^{-1}$	$10^{-1} - 7 \times 10^{-2}$ (Ω cm)$^{-1}$	3×10^2 (Ω cm)$^{-1}$
Laser scanner Threshold I (0 dB, 4416 Å)	≥450 units	300 to 450 units	≤300 units

material, and these properties (low strain, low surface roughness, good structural perfection, etc.) are unchanged upon annealing (under conditions comparable to actual processing). There are more subtle effects, however, for in-situ phosphorus doped polysilicon. (1) The transition temperature from amorphous to crystalline deposition temperature is reduced to about 580°C. (2) For very stringent requirements a deposition at 560 to 570°C in the amorphous form is recommended. (3) For many applications, however, the temperature range of $580 \leq T_d \lesssim 620°C$ might yield material properties

Table 3—Properties of Phosphorus-Doped Annealed Films (900–1000°C)

Properties	$T_d \leq 570°C$	$580 \leq T_d \lesssim 620°C$	$T_d \gtrsim 620°C$
Structure	Polycrystalline	Polycrystalline	Polycrystalline
Average grain size	2700 Å	2250 Å	1000–2000 Å
Preferred grain orientation	⟨111⟩	⟨111⟩	⟨111⟩ ⟨311⟩ for 620° strong ⟨311⟩ for 640°
Structural perfection	high	medium	low
Strain	medium	medium	medium
Surface roughness (rms)	<15 Å	<25 Å	>70 Å
Electrical conductivity (average value)	1.2×10^3 (Ω cm)$^{-1}$	1.4×10^3 (Ω cm)$^{-1}$	9.5×10^2 (Ω cm)$^{-1}$
Thermal activation energy		not measured	
Laser scanner Threshold I (0 dB, 4416 Å)	≥450 units	300 to 450 units	≤300 units

Table 4—Growth Conditions and Properties of Undoped As-Grown Films

Properties	$T \leq 580°C$ (low-T deposition)	$T \geq 600°C$ (high-T deposition)
Growth conditions	200 cm³/min 350 mT Substrate spacing ¼ inch	50 cm³/min 120 mT Substrate spacing ¼ inch
Growth rate	30 to 60 Å/min	50 to 150 Å/min
Effective refractive index	3.95	3.5–3.6
Typical radial thickness uniformity	<6%	<6%
Structure	amorphous	polycrystalline
Average grain size	—	160 to 320 Å
Preferred grain orientation	none for 560, 570°C weak ⟨311⟩ for 580°C	⟨311⟩ for 600°C ⟨110⟩ for 620°C
Surface roughness (rms)	<15 Å	52 to 60 Å (620°C)
Electrical conductivity	1×10^{-6} $(\Omega\ cm)^{-1}$	$3.5 \times 10^{-7} - 1 \times 10^{-6}$ $(\Omega\ cm)^{-1}$
Laser scanner Threshold I (0 dB, 4416 Å)	≥570 units	<350 units (620°C)

of lesser but sufficient quality. (4) Finally, deposition temperatures $T_d > 620°C$ result in poor material (high strain and low perfection) and should be avoided.

The growth rate increases with increasing temperature and is higher than 30 Å/min at $T_d = 570°C$, where films of the highest quality are still formed. The rate can be doubled in the upper part of the temperature range, which yields medium quality films. Far higher rates can be achieved at $T_d > 620°C$, but only at the cost of lower structural and surface perfection. It has further been shown that sheet resistivities of 16 to 20 Ω/□ can be achieved by in-situ phosphorus doping and in the high-quality low-T_d films.

Table 5—Properties of Undoped Annealed Films (900–1000°C)

Properties	$T_d \leq 580°C$ (low-T deposition)	$T_d \geq 600°C$ (high-T deposition)
Structure	Polycrystalline	Polycrystalline
Average grain size	700 to 920 Å	240 to 400 Å
Preferred grain orientation	⟨111⟩	⟨311⟩ for 600°C ⟨110⟩ for 620°C
Structural perfection	high	low
Strain	low	high
Surface roughness (rms)	≤15 Å	52 to 60 Å (620°C)
Electrical conductivity (average value)	1×10^{-6} $(\Omega\ cm)^{-1}$	1.3×10^{-6} $(\Omega\ cm)^{-1}$
Thermal activation energy	0.5 to 0.58 eV	ill-defined
Laser scanner Threshold I (0 dB, 4416 Å)	≥570 units	<350 units (620°C)

Acknowledgment

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LPCVD Polycrystalline Silicon: Growth and Physical Properties of Diffusion-Doped, Ion-Implanted, and Undoped Films

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Abstract—The texture and surface smoothness of polycrystalline silicon layers are important characteristics in the application of these layers as gates, interconnects, and load resistors in high-density circuits. In this work, amorphous and polycrystalline silicon layers were evaluated with respect to structural, topographical, and electrical properties before and after diffusion doping and ion implantation. Films prepared in the polycrystalline state by LPCVD frequently have a columnar growth structure which is associated with a rough surface. Diffusion-doping with phosphorus promotes grain growth and increases surface roughness. By contrast, films prepared in the amorphous state retain their initial smooth surfaces even after diffusion-doping with phosphorus and subsequent annealing. Amorphous films that are ion-implanted with phosphorus and annealed retain their initial smoothness but reveal inhomogeneity in grain structure from the tops of the films to the bottoms of the films depending upon the depth of the implant.

1. Introduction

Polycrystalline silicon layers fulfill many important applications in microelectronics, such as gates, interconnects, and load resistors. The morphology and surface topography of these layers can strongly

influence device performance especially in thin-film layered structures with fine device geometries. Surface asperities on layers prepared by conventional means may lead to a lowering of the dielectric field strength and enhanced tunneling currents in interfacing dielectrics.[1] Structural properties, as influenced by deposition and processing parameters, can have an appreciable effect on the electrical properties of the layers for a given level of dopant.[2] In this paper we discuss some of the structural, topographical, and electrical properties of polycrystalline and amorphous silicon layers both before and after ion implantation or diffusion-doping with phosphorus.

2. Experimental

The silicon films evaluated in this work were prepared by LPCVD and were selected from several different reactors. The deposition temperature ranged from about 560°C to about 620°C, and the substrates employed were thermally oxidized silicon (3-inch-diameter) wafers. Film thickness was usually 5000 Å. Some films were diffusion-doped with phosphorus by standard means using $POCl_3$, and some samples, which had been prepared in the amorphous state at 560°C, were ion-implanted with phosphorus, $^{31}P^+$, at 80 keV with an implant dose ranging from 5×10^{11} to $5 \times 10^{15}/cm^2$. Implanted films were provided with a thin SiO_2 cap (~350 Å of SiO_2 grown in steam + HCl at 800°C) and subsequently annealed at 950°C in N_2 for about 50 min.

The texture of the films was examined by x-ray analysis and by cross-sectional TEM. Surface roughness evaluations were made by UV reflectometry.[3] Resistivity measurements were made on the various films using a conventional four-point probe in the case of low-resistivity films and by a six-point probe[4] in the case of high-resistivity films. Sheet resistance measurements were made by providing strip contacts on the surfaces of the films and estimating the sheet resistance from the current-voltage curves.

3. Results and Discussion

3.1 UV Reflectance Measurements

An important consideration in these experiments was the surface smoothness of the silicon films both before and after processing. Fig. 1 shows reflectance values obtained on a set of samples deposited in the 560 to 622°C temperature range. As described in Ref. 3, the reflectance terms, ΔR_{280} and ΔR_{400}, represent the difference in re-

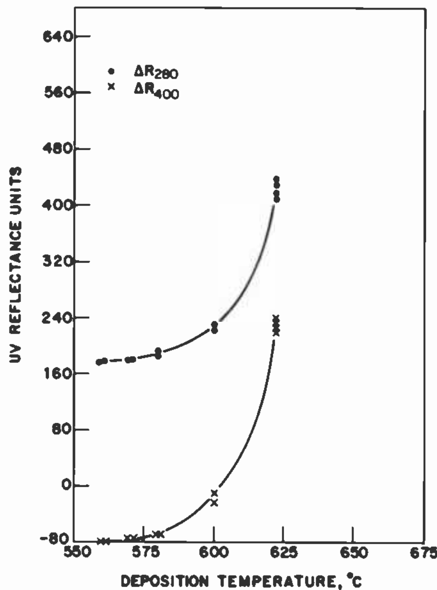

Fig. 1—UV reflectance values, ΔR_{280} and ΔR_{400}, obtained on a set of silicon films deposited in the 560 to 622°C temperature range.

flectance between a single-crystal silicon reference reflector and the silicon film being evaluated at the wavelengths indicated, namely, 280 and 400 nm. The term ΔR_{280} is used for assessing surface roughness on polysilicon films, while the term ΔR_{400} is preferred for evaluating films with amorphous character. A negative value is obtained for ΔR_{400} in the case of amorphous films, since their reflectance is higher than that of single-crystal silicon at this wavelength.

It can be seen from Fig. 1 that the values of ΔR_{280} and ΔR_{400} remain almost constant for films deposited in the temperature range from 560°C to about 580°C (corresponding to amorphous silicon films). At deposition temperatures above 580°C, the reflectance terms increase quite rapidly, indicating increasing surface roughness as the deposited films become polycrystalline in character. These results demonstrate the difficulty in controlling film surface roughness at conventional growth temperatures of about 620°C, especially since a gradient in the furnace-temperature profile is sometimes introduced to facilitate film-thickness uniformity throughout the furnace. Thus, not all films may be deposited at the same temperature in a given deposition run. In addition, diffusion doping of polycrystalline silicon films may increase surface roughness still further. Values of ΔR_{280} obtained on undoped and diffusion-doped films from each of two different LPCVD reactors are presented in

Table 1—Reflectance Values, ΔR_{280}, for Undoped and Diffusion-Doped Polysilicon Films.

Wafer No.	Reactor 1		Reactor 2	
	As-Deposited	$POCl_3$ (950°C)	As-Deposited	$POCl_3$ (950°C)
1	393	966	230	738
2	392	970	230	741
3	390	966	231	738
4	391	961	229	737
5	391	961	227	739
6	390	963	226	746
7	389	963	227	739
8	389	963	225	740
9	388	960	226	743
10	388	961	224	741
11	389	963	225	737
12	389	960	224	737
13	390	962	224	741
14	388	961	224	742
15	389	963	224	744
16	388	966	225	741
17	388	963	225	742
18	387	963	225	744
19	388	962	225	741
20	387	960	224	745
21	387	960	222	748
22	388	958	223	750
23	387	850	223	730
24	388	960	222	744
25	—	960	224	748

Table 1. It can be seen that a pronounced increase in the value of ΔR_{280} occurs after phosphorus doping. While part of this increase may be due to a change in the optical constants of polysilicon with doping,[3] it is likely that most of the change results from increased surface roughness due to grain growth.

It has been demonstrated that, when undoped and in-situ doped amorphous silicon films are crystallized, relatively smooth surfaces are obtained.[5,6] Similar results were obtained in this work when silicon films, initially prepared in the amorphous state at 560°C, were diffusion-doped with phosphorus and annealed at 950°C for 1 hour. Representative reflectance values are given in Fig. 2 for these films together with reflectance values determined for some of the undoped samples from Fig. 1 after annealing at 950°C for 1 hour in N_2. Comparably smooth films are obtained for diffusion-doped and undoped amorphous silicon films after crystallization.

Table 2 is a list of reflectance values obtained on a set of samples that were initially prepared in the amorphous state at 560°C and subsequently implanted with phosphorous and annealed at 950°C. Again it is apparent that smooth films are obtained at all implant doses.

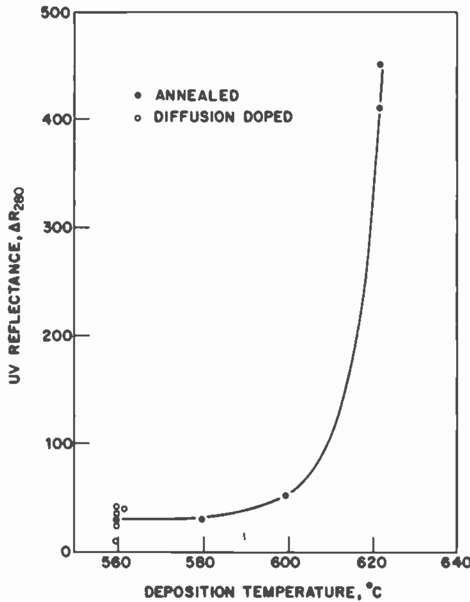

Fig. 2—UV reflectance values, ΔR_{280}, obtained on silicon films: ● after annealing at 950°C in N_2 for 1 hour, ○ after diffusion-doping and annealing.

3.2 X-Ray and TEM Analysis

The texture of some films was examined by x-ray and TEM analysis to determine grain size and structure and any relationship to surface roughness as determined by UV reflectance. A set of four sample pairs consisting of as-deposited and annealed films were examined by x-ray analysis for differences in crystallite structure. The sample pairs were selected from films initially deposited in the 560 to 622°C temperature range. The results are given in Table 3.

Crystalline sizes were calculated directly from the Scherrer equa-

Table 2—Reflectance Values Obtained on Silicon Films (T_d = 560°C) Before and After Implantation and Annealing.

	Reflectance Values				
	As-Deposited		After Implantation and Annealing		Implant Dose/cm²
Sample No.	ΔR_{280}	ΔR_{400}	ΔR_{280}	ΔR_{400}	($^{31}P^+$, 80 keV)
1	214	−70	46	19	5×10^{11}
2	217	−67	77	59	5×10^{12}
3	212	−64	56	26	5×10^{13}
4	215	−64	36	23	5×10^{14}
5	212	−64	57	52	5×10^{15}

Table 3—X-Ray Data Obtained on As-Deposited and Annealed Silicon Films.

Sample No.	Deposition Temperature (°C)	Annealed	D_{111} (Å)	D_{220} (Å)	I_{220}/I_{111}
2A	622	No	90	>705	9.57
2B	622	Yes	140	>1030	9.71
3B	600	No	80	230	0.22
3A	600	Yes	315	370	0.17
4A	580	No	Amorphous →		
4B	580	Yes	325	315	0.13
5A	570	No	Amorphous →		
5B	570	Yes	315	315	0.18

tion assuming that the line broadening observed was due to small-crystallite-size effects only. Calculated crystallite sizes thus represent minimum possible values. Of the samples evaluated, the sample pair deposited at 622°C was the most unique. Both the annealed and unannealed specimens exhibited a large degree of (220) texture and a unique crystallite structure. These samples seemed to have two types of crystalline domains—a randomly oriented polycrystalline matrix with a crystallite size of ~100 Å containing highly oriented (220) domains with a much larger crystallite size. In this case, only the crystallite size of the poly-matrix (~100 Å) is reasonably certain. The size of the larger (220) domains may be much larger than the calculated value of 705 or 1030 Å. If necessary, a more accurate value for the larger (220) domains can be obtained by the more laborious procedure of peak deconvolution followed by the application of integral breadths to differentiate between the broadening influence of crystal size and of microstrain. Annealing at 950°C for 1 hour in N_2 seems to have little or no effect on films deposited at 622°C. At this deposition temperature, annealed samples retain their original large degree of (220) texture with perhaps a slight increase of crystallite size of both domain types. The remaining sample pairs initially deposited in the 570 to 600°C temperature range appear to be random in orientation after annealing. As-deposited films at 570 and 580°C appear amorphous whereas their annealed counterparts are crystalline having a random texture with a calculated crystallite size of ~300 Å.

Because of the pronounced (220) texture of the films deposited at 622°C, the ratio of diffracted intensities, I_{220}/I_{111}, was used as an index for characterizing film texture. Values of this ratio are given in Table 3 for as-deposited and annealed films. It can be seen that the value of this ratio is small for films deposited at low temperatures and subsequently crystallized by annealing. Fig. 3 is a plot of the UV reflectance term ΔR_{280} versus the I_{220}/I_{111} ratio for samples

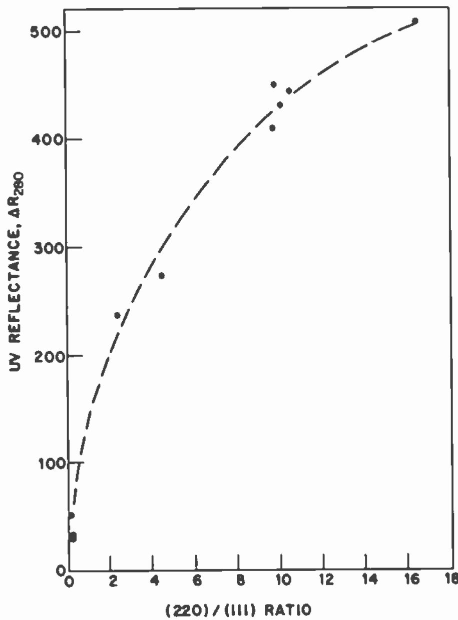

Fig. 3—UV reflectance values, ΔR_{280}, versus the x-ray intensity ratio I_{220}/I_{111}. The films were annealed at 950°C in N_2 for 1 hour.

obtained from several different sources. It is clear that surface roughness is strongly related to the (110) content of the films. The lowest values of ΔR_{280} are obtained at the lowest I_{220}/I_{111} ratios, which correspond to films deposited in the amorphous or mixed amorphous-polycrystalline state and subsequently crystallized by annealing. This is clearly observed in the cross-sectional TEM micrographs of Fig. 4 which show annealed films, initially deposited at 600°C and 622°C. The columnar (110) structure of the film deposited at 622°C is evident. Annealing had no apparent effect on this film, whereas the film deposited at 600°C was initially of mixed amorphous-polycrystalline structure and was completely crystallized upon annealing.

The texture of silicon films as related to deposition temperature and annealing has been described in detail in the literature.[7,8] The purpose of this discussion is to indicate the quantitative correlation between UV reflectance and film texture, and to emphasize the critical dependence of surface roughness on deposition temperature in the region conventionally used for the preparation of polycrystalline silicon films. A further complication is that furnace-temperature profiles may be skewed to obtain film thickness uniformity throughout the system. In addition, actual deposition temperatures

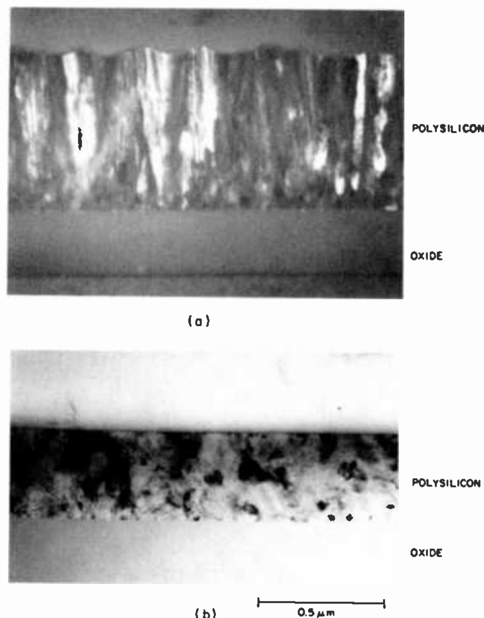

Fig. 4—Cross-sectional TEM micrographs of (a) a silicon film deposited at 622°C and (b) a silicon film deposited at 600°C. Both films were annealed at 950°C in N_2 for 1 hour.

may not be known accurately because of the difficulty in making such measurements at reduced pressures. By contrast, low-temperature deposition results in relatively smooth films even after diffusion-doping or ion-implantation and annealing. It has also been reported that improved grain structure results from the crystallization of amorphous films.[5]

3.3 Electrical Properties

The sheet resistance of diffusion-doped silicon films prepared by conventional means ranged from about 15 to 30 Ω/□. The sheet resistance of films prepared in the amorphous state and subsequently diffusion-doped ranged from about 12 to 20 Ω/□. The doping schedules were similar in all cases. It may be concluded that the sheet resistance of diffusion-doped films, which were initially amorphous, is as low or lower than that of films prepared at conventional growth temperatures.

The sheet resistance of silicon films deposited in the amorphous state at 560°C and subsequently implanted and annealed (as described previously) is plotted versus implant dose in Fig. 5. The

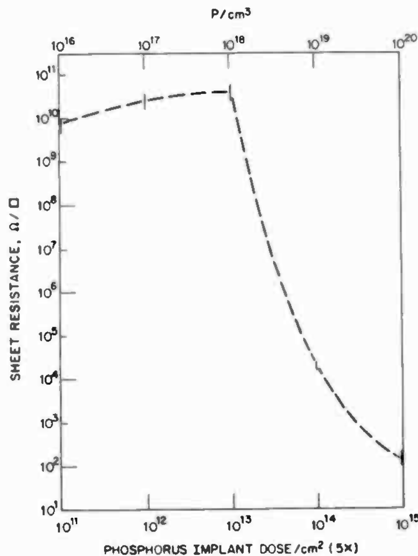

Fig. 5—Sheet resistance versus $^{31}P^{+}$ implant dose for silicon films initially deposited at 560°C. The films were provided with a SiO_2 cap and annealed at 950°C in N_2 for 1 hour. The implant energy was 80 keV.

initial increase in resistance with increasing implant dosage may be explained on the basis of carrier trapping in states at the grain boundaries, thus depleting a portion of each grain and generating potential barriers that impede carrier transport.[9] The steep part of the curve in Fig. 5 is similar to that obtained for films prepared in the polycrystalline state, except that a relatively high concentration of dopant is required before the sheet resistance begins to abruptly change from high values to lower values. This is indicative of small grain size.[10]

The ion-implanted samples were subsequently examined by cross-sectional TEM. The results indicate that at ($^{31}P^{+}$) implant doses of 5×10^{14} or greater, relatively large-grain polysilicon (~1500–2000 Å) is produced in the implanted surface region to a depth of about 1500 Å after annealing. The texture of the silicon below this region is apparently unaffected by the implant process and develops a fine-grained (~150–200 Å) structure. TEM micrographs (both bright-field and darkfield) corresponding to an implant dose of $5 \times 10^{15}/cm^2$ are shown in Fig. 6.

The reason for the growth of relatively large crystallites in the implanted region is not clear, especially if the films were truly amorphous at the time of implantation. Implantation with suitably channeled silicon ions and subsequent annealing have been used

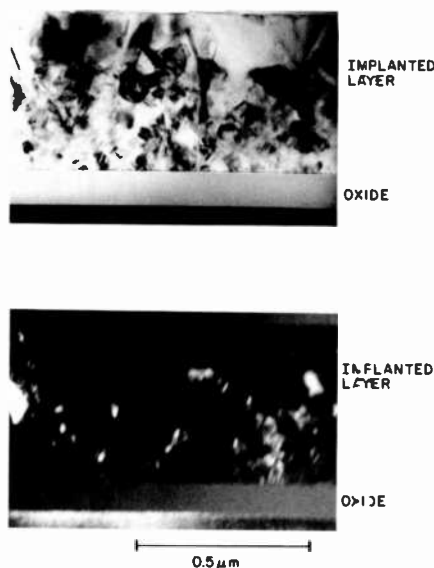

Fig. 6—TEM cross-sectional micrographs (top is brightfield and bottom, darkfield) of an ion-implanted and annealed film. Implant dose: $^{31}P^{+}$, 80 keV, $5 \times 10^{15}/cm^2$.

for increasing grain size in polycrystalline silicon films.[11] Silicon ion implantation followed by solid-state regrowth has also been used for improving the crystallinity of heteroepitaxial silicon on sapphire.[12] These effects may have some influence in the case of amorphous silicon films implanted with phosphorus if fine polysilicon grains were distributed throughout the material. However, the dosage at which we have observed the onset of enhanced grain growth is lower by about a factor of four than that employed in the referenced work above. The influence of phosphorus in promoting grain growth[13] may be the dominant factor favoring increased grain size in the implanted region. Little or no effect of implant dose was detected in the upper surface region in the case of implant doses ranging from 5×10^{11} to $5 \times 10^{13}/cm^2$. A fine-grain structure characteristic of undoped films resulted when these films were annealed. TEM micrographs corresponding to an implant dose of 5×10^{13} are shown in Fig. 7.

The fine-grain structure of the implanted films may account for the relatively high sheet resistance observed for implant doses of 5×10^{13} and higher. The resistivity of the films that received doses of 5×10^{14} and $5 \times 10^{15}/cm^2$ would probably be lower if the entire film thickness had the larger grain structure characteristic of the top 1500-Å surface region. It is likely that these films had a gradient

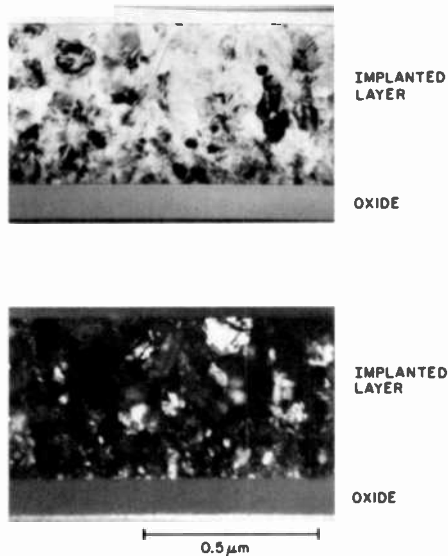

Fig. 7—TEM cross-sectional micrographs (top is brightfield and bottom, darkfield) of an ion-implanted and annealed film. Implant dose: $^{31}P^{+}$, 80 keV, $5 \times 10^{13}/cm^2$.

in conductivity from the surface regions to the bottoms of the films. The rapid decrease in sheet resistance at doses above $5 \times 10^{13}/cm^2$ may also be related to development of large surface grains in the implanted region. Higher energy implants would help in providing more homogeneous grain structure throughout the depth of the films.

Electrical conductivity measurements were made on ohmic contacts to films implanted with $^{31}P^{+}$ at 80 keV and a dose of $5 \times 10^{12}/cm^2$. A room-temperature sheet resistance of about $2 \times 10\ \Omega/\square$ was obtained, and the temperature dependence of electrical conductivity indicated an activation energy of between 0.57 and 0.62 eV. This is in good agreement with a value of 0.63 eV obtained on device resistors at an implant dose of $10^{13}/cm^2$ under the same implant conditions.[14]

4. Summary and Conclusions

The dependence of surface roughness of polysilicon films on growth and processing parameters can be conveniently monitored by UV reflectance measurements. Surface roughness increases rapidly with deposition temperature above 600°C. At conventional growth temperatures of about 620°C, a columnar growth structure characteristic of preferentially oriented (110) material may cause enhanced

surface roughness. This structure is much reduced in films initially prepared in the amorphous or mixed amorphous/polycrystalline state at lower temperatures and subsequently crystallized by annealing. Consequently, these latter films have much smoother surfaces.

Diffusion-doping with phosphorus increases the surface roughness of polysilicon films deposited at 620°C but causes little change in the surface roughness of films initially deposited in the amorphous state at 560°C. Amorphous films that are ion-implanted with phosphorus and annealed retain their initial smoothness but exhibit relatively large grain size in the implanted regions of the films for implant doses of $5 \times 10^{14}/cm^2$ or greater. Beneath the implanted regions, a smaller grain size, similar to that observed for annealed but undoped films, is obtained. Small grain size is also obtained throughout the film thickness for implant doses below $5 \times 10^{14}/cm^2$.

The sheet resistance of diffusion-doped silicon films, initially prepared in the amorphous state, is as low or lower than that of films initially prepared in the polycrystalline state at 620°C. The sheet resistance of phosphorus-implanted and annealed amorphous silicon films is less well defined because of the dependence of the grain structure on the implant dose and depth of the implant. Further work is needed to obtain lower sheet resistance values at the higher implant doses. It is expected, however, that this can be accomplished by increasing the depth of the implant.

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Silicon-Wafer Process Evaluation Using Minority-Carrier Diffusion-Length Measurement by the SPV Method

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Abstract—Measurement of the minority-carrier diffusion length L by the constant-magnitude steady-state surface photovoltage (SPV) method has become an important tool within RCA for evaluating the effect (on L) of silicon device fabrication steps. We present first a simplified description of the method and the practical information required for implementing this measurement technique. Substrate selection, sample preparation, data evaluation, and the limitations of the method are discussed in detail. Next, we describe the use of the SPV technique to monitor the unintentional introduction of heavy metal impurities at five different steps during wafer processing. The causes of wafer contamination are: (1) inadequate wafer cleaning, (2) handling wafers with stainless-steel tweezers, (3) frictional contact between wafers and metallic components in the end stations of ion implanters, (4) a malfunctioning boron-doping source, and (5) impurities introduced during epitaxial layer growth. The beneficial effect of adding 1-1-1 trichloroethane (TCA) to a furnace ambient is assessed by using the SPV technique and also by counting the number of crystalline defects delineated with Wright etch.

1. Introduction

In the fabrication of bipolar semiconductor devices, one of the most important material parameters is the minority-carrier lifetime τ (or an equivalent parameter, the minority-carrier diffusion length $L = \sqrt{D\tau}$, where D is the diffusion coefficient of the minority carriers). The constant-magnitude steady-state surface photovoltage (SPV) method[1] is in principle an excellent technique for determining L

because: (1) the method is nondestructive, (2) sample preparation is minimal, i.e., no contacts or junctions or high-temperature processing steps are required, and (3) the method is based on steady-state transport and is relatively immune to the slow trapping and de-trapping difficulties that affect lifetime measurements made by the photoconductive decay and other transient methods. It has been established as a standard test method of the ASTM.[2] Nevertheless, it does not seem to have received extensive use throughout the silicon device industry. For example, at the Symposium on *Lifetime Factors in Silicon* (February 1979, San Diego, CA), the SPV method was the method of choice in only one of nineteen papers presented.[3] It appeared that this lack of use of the method, despite its advantages, was due to technical difficulties in implementation rather than to a fundamental problem with the method itself. In subsequent work, these difficulties were addressed and virtually eliminated by the development of an improved measurement system.[4,5] This system is now used on a routine basis within RCA for measurements of L by the SPV method.

In this paper, the SPV method is used as a tool for evaluating the effect of device fabrication steps on the minority-carrier diffusion length of silicon wafers. To facilitate discussion of some of the measurement details, we present in Sec. 2 a simplified description of the SPV method. In Sec. 3, we describe the details of the sample preparation and data evaluation, and discuss the limitations of the method. In Sec. 4, we present specific examples in which the SPV method is used to monitor the creation of contamination-related recombination centers in silicon wafers.

2. Simplified Description of Method

The wafer under test (sample) is assumed to be in the form of a homogeneous semiconductor slab of thickness W, as shown in Fig. 1(a). One surface of the sample is uniformly illuminated by chopped monochromatic light of photon energy $h\nu$ slightly larger than the bandgap E_G of the semiconductor, while the opposite surface is kept in the dark. Electron-hole pairs are produced by the absorbed photons; some of these pairs diffuse to the illuminated surface where they are separated by the electric field of the surface space-charge region whose thickness is w, thereby producing a surface photovoltage ΔV. A portion of ΔV is capacitively coupled to a transparent conducting electrode adjacent to the illuminated face; this signal is then amplified and rectified to provide a quasi-dc analog output that is proportional to ΔV. The value of ΔV is a function of the excess

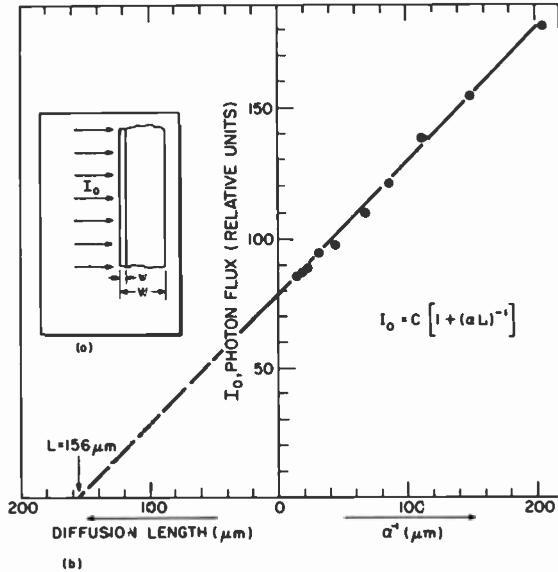


Fig. 1—(a) Sample geometry (inset). (b) Plot of relative photon flux vs reciprocal optical absorption coefficient.

minority-carrier density Δp at the edge of the surface space-charge region. This density, $\Delta p(0)$, is in turn dependent upon the incident light flux I_o, the optical absorption coefficient α, the optical reflectance at the illuminated surface ρ, the recombination velocity at the illuminated surface s, and the diffusion length L. For the sample geometry shown in Fig. 1(a), a steady-state solution of the one-dimensional diffusion equation is[6]

$$\Delta p(0) = \frac{I_o(1-\rho)}{D/L + s} \cdot \frac{\alpha L}{1 + \alpha L}, \qquad [1]$$

under the following simplifying assumptions:

$$\alpha W >> 1, \qquad [2a]$$
$$\alpha w << 1, \qquad [2b]$$
$$W >> L, \qquad [2c]$$
$$w << L, \qquad [2d]$$
$$\Delta p << n_o. \qquad [2e]$$

n_o is the majority carrier density. We return later to a discussion of these assumptions and their importance.

A series of different optical wavelength (λ) values is selected to provide different values of α. At each wavelength, I_o is adjusted to

produce the same value (a *constant magnitude*) of ΔV. It follows then, that $\Delta p(0)$ in Eq. [1] is a constant. If ρ is essentially constant over the wavelength region of interest, Eq. [1] may be written

$$I_o = C\,[1 + (\alpha L)^{-1}], \qquad [3]$$

where C is a constant. If I_o is plotted against α^{-1} for each constant-magnitude ΔV point, the result is a linear graph whose extrapolated intercept on the negative α^{-1} axis is L. This is illustrated in Fig. 1(b).

3. Implementation of the Measurement

3.1 Substrate Selection

Since diffusion length values as large as 250 μm were expected for properly processed wafers, 750-μm-thick, float-zone (FZ), (100)-oriented n-type wafers with a resistivity of 5-15 Ωcm were used in most of the experiments. The wafer thickness was chosen to satisfy the assumption (Eq. [2c]) that the sample thickness be much greater than the diffusion length. This point is discussed further in Sec. 3.4.2.

In the as-received condition, the measured values of L were at least 250 μm. The wafers were polished on one side and chemically etched on the other side. Wafers with both sides chemically etched could be used with the qualification that the etching be deep enough to remove any surface work damage produced by the wafer-slicing process. Since the SPV technique is sensitive to surface damage,[7] residual work damage can produce erroneous values of the measured diffusion length. Float-zone wafers were used instead of Czochralski (CZ) wafers to eliminate the complications that might be caused by oxygen (in different states of precipitation) that is normally present in CZ silicon at a concentration in the mid 10^{17} to low 10^{18} atom/cm^3. In as-grown float-zone material the oxygen concentration is typically less than 10^{16} atoms/cm^3. The minority-carrier diffusion length is not affected significantly by the presence of oxygen at such a low concentration.

3.2 Sample Preparation for SPV Measurements

N-type samples in this study were prepared by cleaning the wafers in standard Si-cleaning etches (SC-1 and SC-2),[8] removing any residual SiO_2 layers in buffered HF, and treating the wafer surface in an aqueous solution of $KMnO_4$. For p-type samples, the $KMnO_4$ treatment step would be omitted.

The purpose of the sample-surface preparation was to provide a large, stable surface barrier; this would, in turn, allow the development of a large, stable surface photovoltage during the measurement. Most of our samples are characterized at an SPV level (at the Si surface) of about 5 to 10 mV. In some cases when the diffusion length is very short (≤ 5 μm), it is necessary to work at lower SPV levels (~ 1 mV). Noise level and observed drift during the measurement procedure are typically $\leq 1\%$. A more complete account of the surface treatment details and the studies that led to the procedure described above will be published at a later date.

3.3 Data Evaluation

It is evident that the data points in Fig. 1(b) do indeed lie on a straight line, and this type of measurement result is normally observed. Occasionally, however, curvature is observed, and some of the possible reasons for this are discussed below.

Some quantification of the curvature of an I_o vs α^{-1} plot may be obtained by the following procedure: (1) Fit the data with a "best" straight-line plot which minimizes the sum of the squares of the differences between the I_o data points and the "best" straight line, and (2) determine the correlation coefficient r for that fit.[9] Under certain conditions, r will be a measure of the curvature of the I_o vs α^{-1} data plot.

For a perfect fit, r will have the value 1; this will be true if and only if every data point lies directly on the "best" straight line. Values of r less than 1 may occur for either (or both) of two reasons: (1) random fluctuations (noise) in the data, and (2) nonlinearity in the functional relationship between I_o and α^{-1}. The first reason will be present to some degree in any real measurement system, preferably at some small, relatively constant, level. The second reason may be present if one or more of the assumptions employed in the derivation of Eq. [1] are invalid.* A crude measure of (2) may be obtained by considering the extent to which the actual r falls below the minimum value of r expected as a result of (1).

Most calculator and computer programs for linear curve fitting (linear regression analysis) give r^2 (rather than r) as an output. For convenience, then, r^2 will be used as the parameter of correlation in further discussion.

* The second reason may also be present if a nonrandom error is built into the measurement system. This possibility was effectively eliminated by showing that the presence of the nonlinearity was both rare and sample-dependent.

It has been found experimentally that r^2 values between 0.99 and 1.00 are generally obtained from I_o vs α^{-1} plots, and 0.99 has been set as a minimum value of r^2 for which our data are considered reliable. This cutoff value is somewhat arbitrary. Some data plots with $r^2 = 0.98$ appear to have only random scatter of the data points about the "best" straight line; others show small but clearly perceptible curvature. Most data plots with $r^2 < 0.98$, however, show obvious curvature. It should be noted in passing that the cutoff value for r^2 is (and should be) system dependent. A noisy system would, for example, require a lower cutoff value of r^2 because of the larger random fluctuations in the I_o vs α^{-1} data.

3.4 Limitations of the Method

The limitations of the method fall naturally into two categories: (1) sensitivity (noise) limitation, and (2) fundamental limitations due to the assumptions stated in Eqs. [2a] through [2e].

3.4.1. Sensitivity Limitation

A sample with a given value of L will have, for a specific measurement system, a maximum limit on the value of SPV that it can produce over the wavelength range required for the measurement procedure described in Sec. 2. When L becomes so small that the system noise becomes comparable with the SPV, the value of r^2 for the I_o vs α^{-1} plot will decrease to some unacceptable level.

We have not yet reached the minimum value of L that it is possible to measure, based on the sensitivity limitation. Gold-doped silicon samples typically have measured diffusion-length values in the 1- to 2-μm range; however, values below 1 μm have been found, the lowest being 0.2 μm. It is important to note that despite a diminished SPV signal, the noise level was still sufficiently low that r^2 for this data plot was 0.999+, as indicated in Fig. 2(a). Also shown here, for contrast, (curve b of Fig. 2) is the SPV data for a sample with a large diffusion length (≈200 μm).

An additional indication of how small a diffusion-length value may be measured is found in the work of Moore.[10] Using an SPV measurement system that was specifically designed for his application, he is able to reliably determine L values in hydrogenated amorphous silicon (a-Si:H) as small as 0.02 μm.

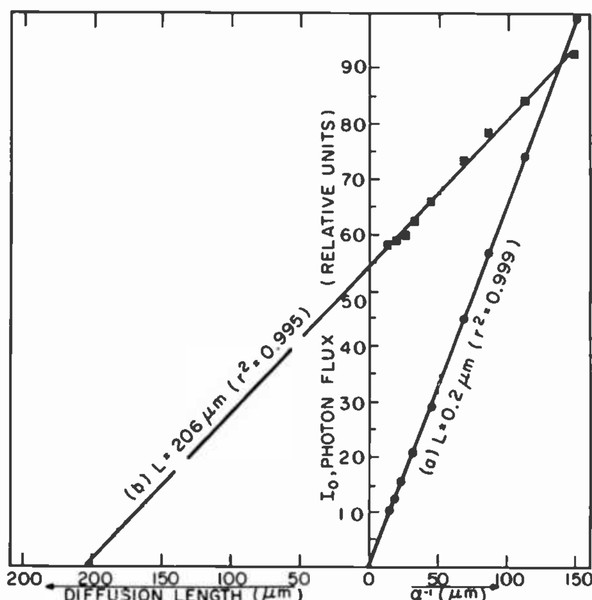


Fig. 2—Plots of relative photon flux vs reciprocal optical absorption coefficient illustrating two results of high-temperature furnace treatment: (a) wafer processed in a gold-contaminated furnace tube and (b) wafer processed in a clean furnace tube.

3.4.2 Fundamental Limitations Based on Eqs. [2a] Through [2e]

It is useful to examine the assumptions [2a] through [2e] that were used to derive Eq. [1]. Although a rigorous mathematical treatment is beyond the intended scope of this paper, some useful insights can be developed from a semi-quantitative consideration of the assumptions and the extent to which they are valid.

$$\alpha W >> 1 \qquad [2a]$$

This condition assures that all of the light entering the sample is absorbed before it reaches the rear (unilluminated) surface; the average penetration depth of the light in this case is α^{-1}. If this condition is not maintained, the I_o vs α^{-1} plot may become nonlinear. As a practical matter, detectable nonlinearity may occur for $3 < \alpha W < 4$; $\alpha W \geqslant 4$ is sufficient to assure a linear plot.

$\alpha w << 1$ [2b]

This condition assures that a negligible amount of light is absorbed in the space-charge region. It is not usually a difficult condition to meet. For example, the doping in our test-sample wafers is typically $\gtrsim 10^{14}/cm^3$ and $w \lesssim 2.5$ μm. The lowest value of α^{-1} used in the measurement is usually 14.3 μm; thus, $\alpha w \lesssim 0.18$. If it were desirable to use less penetrating light for the measurement, more heavily doped test-sample wafers could be used.

$W >> L$ [2c]

This is the most troublesome condition to meet because it requires very thick test-sample wafers to measure large diffusion lengths. Examination of an exact solution of the diffusion equation (not requiring $W >> L$)[11] shows that (1) $W > 4L$ is sufficient to give very accurate results, and (2) $2L < W < 4L$ gives results whose accuracy is dependent upon the surface recombination velocity at the unilluminated surface. For $W = 2L$, the inaccuracy of the apparent (measured) diffusion length L_A is ~10%. As a practical matter we assume that if $L_A < W/3$ the value is accurate, but if $L_A > W/3$ the numerical value is suspect and we can say only that $L \geqslant W/3$.

$w << L$ [2d]

The value of L_A determined by the SPV method is actually a collection length; i.e., it is the distance into the sample from the illuminated surface that defines a region from which optically generated carriers are collected. This collection length is equal to L if w is small enough to be neglected; i.e., if the carriers generated in the space-charge region (whose thickness is w) can be neglected. If w is not small relative to L, then $L_A > L$.

In crystalline silicon, non-negligible w is not usually a problem for the following reasons: (1) for processing studies, L values in the range of greatest interest ($L > 30$ μm) are much larger than w in the test sample wafers ($w < 2.5$ μm), and (2) if it were desired to study L values in degraded silicon (e.g., $L = 1$–2 μm in Au-doped material), one could use test-sample wafers with greater donor or acceptor doping to obtain much lower values of w.

It is interesting to note that in a-Si:H, the situation is very different; w is often much larger than L. A theoretical treatment of the relationship between L_A, L, and w has been given for this case by Moore.[12] One approach that can be used to reduce w is to flood the sample with unchopped light, thereby collapsing the space-charge layer.

$$\Delta p << n_o \qquad [2e]$$

Although it would be possible, in principle, to violate this condition if one were to use very lightly doped, very-long-lifetime silicon and intense light, the experimental arrangement of our measurements assured that the condition was always valid.

In summary, of the restrictive conditions imposed by Eqs. [2a] through [2e], only that due to Eq. [2c] is significant; the limitation imposed by it can be stated as follows: To accurately determine a diffusion length L, one requires a sample whose thickness W is at least $3L$.

4. Sources of Wafer and Furnace Contamination

Diffusion length values between 0.5 and 300 μm were measured on wafers that had been processed at high temperature (≥1000°C). In numerous cases, the source(s) of contamination were identified either by using the SPV method alone or, more commonly, by utilizing the SPV data along with other evidence. In the rest of this paper, several of these experiments utilizing the SPV method are discussed.

4.1 Inadequate Wafer Cleaning

As indicated in Sec. 1, the sample preparation required for a SPV diffusion-length measurement is minimal; no metal contact, p-n junction, or thermal oxide with a specified thickness is necessary. Consequently, it is relatively easy to process the same wafer through several high-temperature operations while measuring the diffusion length after each high-temperature step. In this manner, the same wafer can be used to evaluate the effect of sequential processing steps on the diffusion length.

However, a word of warning is appropriate. After a SPV measurement on a wafer but prior to inserting it back into the process sequence, the wafer should be properly cleaned in order to remove any metallic contamination from the wafer's surfaces; in particular, the manganese-containing layer formed during the surface-treatment procedure must be removed. A few times prior to an additional high-temperature operation, we unintentionally omitted thorough cleaning of surface-treated wafers. The diffusion-length values obtained from SPV measurements on these wafers after the additional high-temperature step were very small, varying between 1 and 10 μm. With suitable wafer cleaning, such as the standard SC-1 and SC-2 procedure, residual metallic impurities were always adequately removed from the wafers' surfaces; so consequently, the

diffusion-length values measured after subsequent high-temperature steps were not affected by the prior $KMnO_4$ surface treatment.

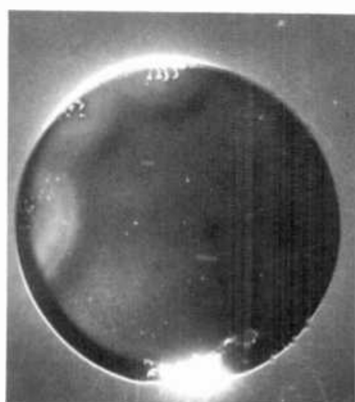
In normal processing, wafers do not come into contact with a source of heavy metal contamination as great as the $KMnO_4$ surface treatment. However, wafers can be contaminated by weaker sources of heavy metal impurities when the wafers are either improperly handled or inadequately cleaned before high-temperature processing. Two of these possible sources of heavy metal contamination are discussed next.

4.2 Stainless Steel Tweezers

There are several reports in the literature[13,14] that metallic contamination can be introduced into silicon wafers by gripping or slightly scratching wafers with stainless-steel tweezers. We performed a series of experiments in which the SPV technique was used to measure the lateral extent and the electrical effect of contamination produced in wafers by handling them in specific places on the wafers with stainless-steel tweezers just prior to putting the wafers into a high-temperature furnace. During the standard furnace cycle the wafers were annealed at 1200°C for 2 hours in a gas mixture containing N_2 and a few percent of O_2.

After the SPV measurements, the wafers were immersed in Wright etch[15] to delineate the presence of crystalline defects. The wafer photograph in Fig. 3(a) presents typical results for the wafers contacted by metal tweezers. In the photograph, the density of crystalline defects, in the form of light-scattering haze, is highest close to the three positions where the wafer was held with the stainless-steel tweezer. The defect density drops noticeably with increasing distance from the regions directly contacted by the tweezer. The lateral extent of the contamination-induced defects from the tweezer marks is not surprising, since the primary constituents of stainless steel are Fe, Cr, and Ni, which are all fast diffusers in Si.[13,14]

Included with the photograph in Fig. 3 is a crude wafer map of SPV values for the diffusion length at specific positions on the wafer. The diffusion length is clearly smaller at the three positions close to where the wafer was handled with the tweezer and becomes larger with increasing distance from the contacted spots. Furthermore, the negative effect of tweezers is even more noticeable when the data shown in Fig. 3(b) is compared with diffusion-length values measured on uncontaminated wafers that were annealed at 1200°C simultaneously with the contaminated wafers. The clean wafers usually had diffusion-length values exceeding 200 μm. The approxi-



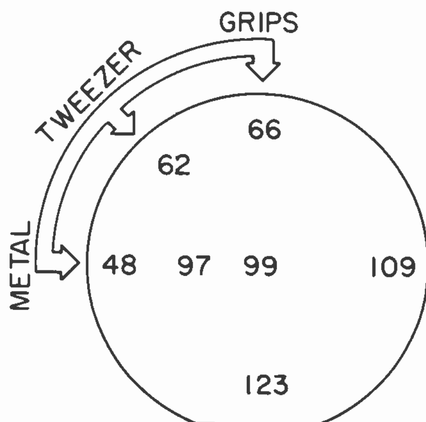


Fig. 3—(a) Photograph of Wright-etched wafer that was held in three positions by a stainless-steel tweezer prior to being inserted into a furnace set at 1200°C. The light-scattering haze produced by small etch pits is most intense next to the positions where the wafer was contaminated by the tweezer. (b) Crude map of the SPV values for the wafer shown in (a).

mate 2.5:1 variation in minority-carrier diffusion length across the wafer corresponds to a 6:1 ratio in recombination lifetime and a 1:6 ratio in the number of recombination centers, since $L \propto \sqrt{\tau}$ and $\tau \propto 1/N$.

The light-scattering haze in Fig. 3 is composed of defects of two sizes that are visible at high magnification: small, roundish defects having a diameter of 1 μm or less, and somewhat larger defects that are about 3 μm long by 2 μm wide. The small, round defects appear to be classic S-pits, which are small stacking faults or precipitates containing heavy-metal impurities.[14] The S-pit density is about 1–2 $\times$ 10^5/cm^2 in the heavy haze region, and is about 10^4/cm^2 in the center of the wafer. The microscopic structure of the 3-μm $\times$ 2-μm defects is not known at the present time.

4.3 Loading Stations in Ion Implanters

In the previous section, data was presented showing the detrimental effect on the minority-carrier diffusion length that results from han-

dling silicon wafers wtih stainless-steel tweezers prior to a high-temperature anneal. A similar effect has also been observed with wafers that were contaminated when they slid across metallic parts during the loading and unloading operations in certain commercial ion implanters. Figure 4 contains typical SPV and Wright-etch data for wafers that were annealed at 1200°C for 2 hours either in dry O_2 or with a small amount of 1-1-1 trichloroethane (TCA) added to the dry O_2 ambient. The wafers that went through the implanter were not implanted with any ions but were only transported in the loading apparatus; hence, the contamination was not introduced into the wafers by the ion beam. Furthermore, the contaminated wafers were not cleaned prior to being transferred into the furnace boat with clean teflon tweezers.

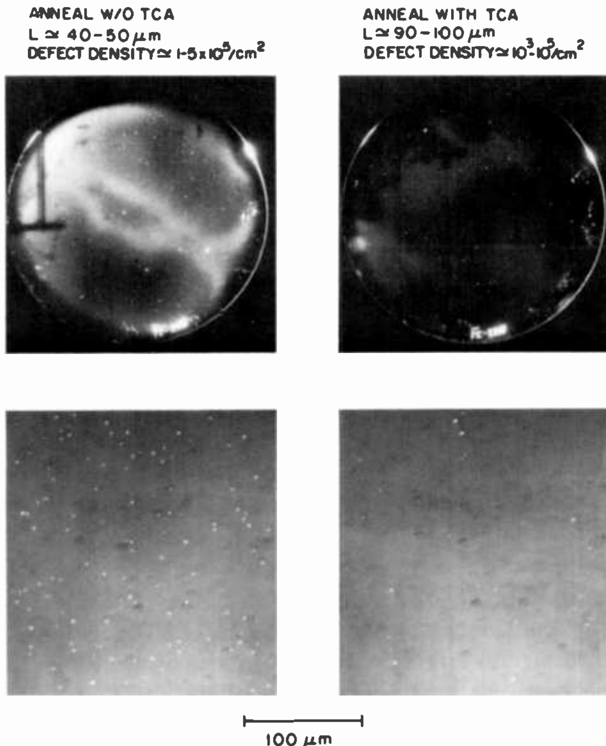


Fig. 4—Photographs and data showing that the addition of TCA to a furnace anneal reduces the defect density and increases the diffusion length. Bright spots in lower set of photographs are etch pits associated with crystalline defects that are caused by heavy metal contamination.

The contaminated wafers that were annealed in the dry O_2 ambient have average L values of 40 to 50 μm. As shown in the low- and high-magnification photographs of the wafer after Wright etching, a fairly high density of small crystalline defects (probably S-pits) is associated with the low L values. The presence of a small amount of HCl (formed by the oxidation of TCA in the furnace tube) in the dry O_2 ambient decreased the average number of crystalline defects by one to two orders of magnitude and raised the average diffusion-length values by a factor of about two.

4.4 Contaminated Boron-Doping Source

One of the doping sources that is commonly used for emitters in pnp structures and bases in npn structures is borosilicate glass (BSG) that is deposited on the silicon surface by chemical vapor deposition at atmospheric pressure and at a temperature of 350 to 400°C.[16] Subsequent to the deposition of the BSG on the surface of the wafers, boron diffusion into the wafers is carried out in a high-temperature furnace. In one device-fabrication facility where this doping technique was used for many years, sporadic problems with poor minority-carrier lifetime were encountered.

In an attempt to identify the cause(s) of the lifetime variations, wafers (some coated with BSG and some uncoated) were cycled through a standard emitter diffusion cycle. The average diffusion-length value for the six BSG-coated wafers was approximately 32 μm, while the average value for the six uncoated wafers was 36 μm. Both of these values were much lower than diffusion-length values of 150 to 250 μm that are normally obtained from clean wafers processed in clean furnaces. These results demonstrated that the short minority-carrier lifetimes and high leakage currents that were being observed on transistors were being caused either by contaminated BSG or by dirty boron-diffusion furnaces contaminated by some means other than the BSG. Since the BSG-coated wafers had slightly lower L values than the uncoated wafers, we theorized that contaminated BSG was the most likely cause of the poor minority-carrier lifetime. This hypothesis was verified when: (1) a leaking gas line was discovered on the CVD equipment used to deposit the BSG[17] and (2) device performance returned to its expected level after the CVD apparatus was fixed.

The atmospheric systems used to deposit BSG need not be significant sources of heavy metal contamination. Diffusion-length values in the range of 60 to 100 μm have been measured for wafers coated with BSG from atmospheric reactors other than the malfunctioning

one cited above. These larger values of L are sufficient for most silicon devices today, even for power devices with diffusion depths up to 30 μm.

One comment on the procedure for measuring the diffusion lengths of boron-diffused wafers is appropriate here. To eliminate the experimental inaccuracies in the SPV measurement produced by the boron-doped surface region, the measurements were performed either by illuminating each wafer's front surface after the boron-doped layer had been etched away or by illuminating the wafer's back surface. The same diffusion-length values were measured with either approach.

4.5 Epitaxial Layer Growth

So far, we have presented several examples demonstrating that the SPV technique can be successfully used to evaluate the electrical effect of heavy metal impurities introduced into wafers by four different operations associated with wafer processing. In this section, we demonstrate how SPV measurements can be used to assess the amount of heavy metal contamination that enters wafers during the growth of epitaxial layers.

In many cases, the epitaxial layer thickness can be less than 15 μm. Unless the expitaxial layer is strongly contaminated by heavy metal impurities, the actual diffusion length of the epitaxial layer will be significantly larger than the thickness of the epitaxial layer. Phillips[18] presented a detailed analysis in which he was able to extract the diffusion length in the epitaxial layer from the measured diffusion length. However, in the most common range of interest where the epitaxial layer thickness is much less than or about the same as the measured diffusion length, the extracted value of the diffusion length in the epitaxial layer is a very sensitive function of the recombination parameters in the region close to the epitaxial layer-substrate interface. The recombination parameters are often not known to the accuracy needed to obtain accurate values of the diffusion length in the epitaxial layer.

In our method, there is no need to directly measure the diffusion length in the epitaxial layer. The silicon layer is deposited on the same type of float-zone substrate previously described. *The important assumption is made that the contaminating species are distributed throughout the thickness of the epitaxial layer and the float-zone substrate in a relatively uniform fashion.* This assumption should be a fairly good one since: (1) float-zone substrates have no inherent gettering mechanism built into them as do Czochralski substrates

and (2) at the temperatures (1100–1200°C) normally used for epitaxial deposition, the heavy metal impurities have sufficiently high diffusion coefficients that the atoms can readily distribute themselves throughout the thickness of an entire float-zone substrate. Presuming the validity of the assumption, the diffusion-length value obtained using our approach is a fairly accurate measure of the contamination level introduced into the epitaxial layer during the growth process.

The presence of either a p-n or n^+-n junction of sufficient barrier height at the epitaxial layer-substrate interface could lead to erroneous diffusion-length values. This source of error can be removed by etching off the epitaxial layer before making the diffusion-length measurements.

SPV measurements were performed on numerous float-zone substrates with deposited epitaxial layers. The validity of the assumption about the uniformity of impurity distribution was repeatedly proven by the measurement of equal diffusion-length values on the front and back surfaces of a wafer. The diffusion length values varied from as low as 2 μm up to 150 μm, depending upon the reactor in which each layer was grown. The lowest values were measured on wafers whose epitaxial layers had been deposited on float-zone substrates that had not been properly cleaned (see Sec. 4.1). The SPV data has allowed us to determine which reactors are producing epitaxial layers with the largest amount of heavy metal contamination in the layers. However, with the exception of the poorly cleaned substrates, insufficient work has been done to pinpoint the exact cause(s) of the contamination-level variations between reactors.

5. Concluding Remarks

In the first portion of this paper, a simplified description of the constant-magnitude SPV method is presented along with short discussions on the limitations of the technique and the sample preparation needed to obtain reproducible results. The analysis demonstrates that the minority-carrier diffusion-length measurements are valid from values on the order of 1 μm to an upper limit that is approximately equal to one-third the thickness of the test wafer.

Five case studies that demonstrate the versatility of the method were presented. Four of these examples describe wafer contamination caused by inadequate cleaning, improper wafer handling, or an impure doping source. In the last example, a new method is outlined for assessing the level of contamination introduced during epitaxial layer growth.

Acknowledgments

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Design Guidelines for Power Switching Transistors

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Abstract—A set of silicon npn power transistors has been studied to determine the dependence of current-handling capability and switching speed upon the open-base, collector-emitter breakdown voltage, BV_{CEO}. Current-handling capability is characterized by the gain-current product, I_m. Switching speed is characterized by the critical current for base widening, I_{cr}. Each of these parameters scales with emitter area. Each parameter also decreases with increasing BV_{CEO} as a power law: $I_m \propto (BV_{CEO})^{-1.6}$ and $I_{cr} \propto (BV_{CEO})^{-2.7}$. These relationships aid in choosing the appropriate chip size for a specified gain-current product, switching speed and breakdown voltage.

1. Introduction

Designing a power transistor generally involves the development of a family of similar devices, each member possessing a different range of operating characteristics. To cover a wide spectrum of current-handling and voltage-blocking capabilities, changes are made in emitter area and in collector thickness and resistivity, respectively. We have systematically studied the effects of such changes upon the devices' operating characteristics, and we have determined some guidelines to aid the designer in choosing the proper chip size for a specified maximum current and breakdown voltage. We also

show how the switching speeds are related to this choice. Our work depends heavily upon previous contributions in this field.[1-6]

First, we discuss the physical structure of the transistors. Next, three parameters that characterize the devices' performance are defined and related to commonly acquired electrical data. From these data, we show how the three parameters are related to a set of performance specifications.

2. Physical Structure

All the transistors used in this study were double-diffused, epitaxial-collector, npn power transistors mounted in TO-3 packages. The p-type boron bases and n-type phosphorus emitters were diffused into the n-type collector region through standard processing similar to that used for RCA's 2N6678 Switchmax transistor. The resulting peak dc current gains, h_{FE}, ranged from 25 to 60, with most units having a gain of about 40.

Figs. 1 and 2 show typical impurity concentration profiles for a device. These profiles are derived from two-point spreading resistance data. Fig. 1 shows the emitter-base region. The emitter-base junction is 6 μm deep; the base-collector junction is 10.3 μm deep;

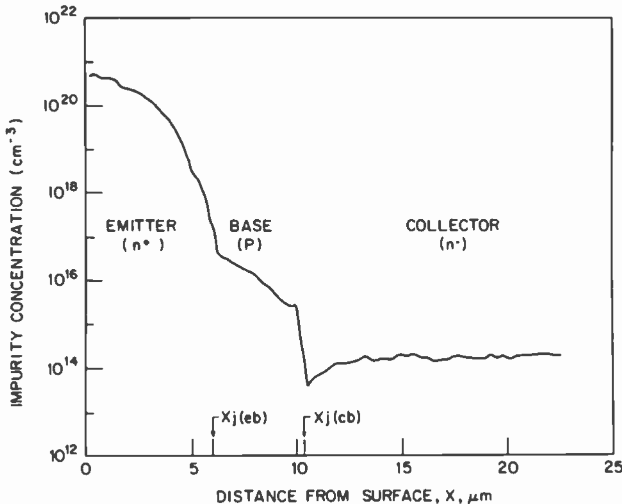

Fig. 1—Emitter-base impurity concentration profile derived from two-point spreading resistance.

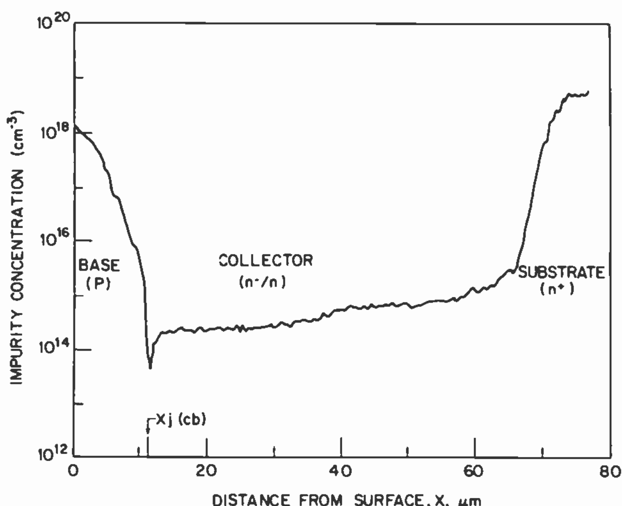

Fig. 2—Base-collector impurity concentration profile showing the epitaxial collector, buffer layer, and substrate region.

and the base width is obviously 4.3 μm. All devices had emitter-base profiles similar to that shown in Fig. 1. Variations in processing resulted in small variations in base widths and peak gain values.

A typical base-collector profile is shown in Fig. 2. The collector has three distinct parts. The region adjacent to the base-collector junction is the most lightly doped and supports the largest percentage of the reverse-biased collector-base voltage. Hence, this region essentially determines the breakdown voltage. To alter the breakdown voltage, the thickness and resistivity of the lightly doped collector region were changed. The resistivity and thickness of the collector regions in the devices with the highest breakdown voltages were 100 Ω-cm and 40 μm, respectively. Those of devices with the lowest breakdown voltages were 10 Ω-cm and 8 μm, respectively. The region adjacent to the n^+ substrate is a more heavily doped buffer layer. The buffer layer significantly extends the devices immunity to second breakdown, but does not support much reverse-bias voltage.

Three different interdigitated emitter patterns were used, each having a different emitter area, periphery, and chip size. Table 1 gives the pertinent data for each pattern. These data are also shown normalized to that of the smallest pattern, E_0. Note that emitter area, A, scales with chip size, but emitter periphery, P, does not.

Table 1—Dimensions of Three Interdigitated Emitter Patterns and Values of these Dimensions Normalized to Pattern E_0

Emitter Pattern	Emitter Area $A(cm^2)$	A/A_o	Emitter Periphery $P(cm)$	P/P_o	Chip Size $C(cm^2)$	C/C_o
E_0	0.065	1.0	8.13	1.0	0.21	1.0
E_1	0.100	1.56	11.4	1.4	0.32	1.56
E_2	0.134	2.1	14.7	1.8	0.42	2.1

3. Characteristic Parameters

A switching transistor must block a given voltage; it must carry a given current while in hard saturation [V_{CE}(Sat)]; and it must switch between these states as quickly as possible in a nondestructive way. As a measure of blocking voltage capability, we choose BV_{CEO}, the open-base, collector-to-emitter breakdown voltage. BV_{CEO} involves the transistor gain, but most of the transistors tested had peak dc gains (h_{FE}) near 40. In cases where a device's peak gain was other than 40, we found that BV_{CEO} scaled as $(h_{FE})^{1/4}$. All BV_{CEO} data were then scaled to a peak gain of 40.

To characterize the transistors' ability to carry current, we use the gain-current product, I_m. To characterize their switching speed, we use the critical current for the onset of base widening, I_{cr}. The determination of these parameter values and their relation to more commonly used characteristics are illustrated in Fig. 3.

3.1 Gain-Current Product, I_m

From a plot of h_{FE} versus I_c for constant and relatively low values of V_{CE}, one extrapolates the 6 db/octave roll-off of h_{FE} with increasing I_c to the point where $h_{FE} = 1.0$. The collector current associated with this point is defined as I_m. This gain-current product describes the gain properties of the unit as it approaches hard saturation. It is a reliable measure of the current-handling capability of the device. The larger I_m, the more current a device can handle. Note, however, that I_m is meaningless for relatively low collector currents where the dc gain is constant, or where the high-current gain approaches unity and rolls off faster than 6 db/octave with increasing I_c.[7]

$I_m = 600$ A in Fig. 3 and at $V_{CE} = 3$ V, for example, the device has a gain of 12 at $I_c = 50$ A. BV_{CEO} is 160 V. With a forced gain of 5 or less at $I_c = 50$ A, the unit is driven into hard saturation. If the power dissipation [V_{CE}(Sat) $\times$ I_c watts] is not destructively high, this unit can handle $I_c = 50$ A in the on-state. Should a forced

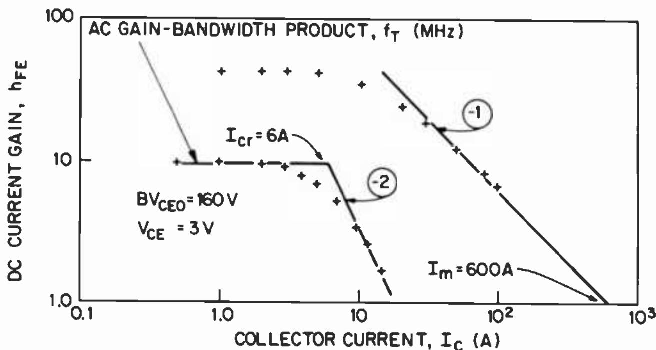

Fig. 3—Gain and gain-bandwidth dependence on collector current. The circled numbers indicate the log-log slopes for each set of data.

gain higher than 5 in the on-state be required, the device may be constrained to carry a lower current; for it will not be driven into hard saturation.

3.2 Critical Current for Onset of Base Widening, I_{cr}

The critical current for base widening is reached in the following way. Current flowing through the lightly doped collector causes an ohmic voltage drop. At the operating point where this ohmic voltage drop in the collector equals the applied collector-base voltage, $V_{CB} = V_{CE} - V_{BE}$, the collector-base junction is no longer reverse biased. The collector current at this point is the critical current for base widening, I_{cr}. At collector currents slightly larger than I_{cr}, the collector-base junction is forward-biased and holes flow into the lightly doped collector region from the base, increasing their spatial extent. This extention is electrically equivalent to widening the base region. A widened base implies a lower limiting frequency response, as measured, for example, by the gain-bandwidth product, f_T. f_T is proportional to the inverse square of the effective base width.

I_{cr} can be determined from a plot of f_T versus I_c with V_{CE} held constant (see Fig. 3). At low collector current, f_T is constant. When $I_c > I_{cr}$, f_T decreases as I_c^{-2}, as seen in Fig. 3. It has been shown that f_T should decrease as I_c^{-2} for collector currents greater than I_{cr}.[8,9] Essentially, the effective electrical base width increases as I_c, and since f_T is inversely proportional to the *square* of the base width, $f_T \propto I_c^{-2}$ for $I_c > I_{cr}$.

The data of the type shown in Fig. 3 were taken with the devices turned on; that is, a positive base-current pulse entered the base input terminal. This situation contrasts to the case where the device

is being turned off, and base current is *extracted* from the base input terminal. In the case of turn-off, the internal charge and current distributions are different from those distributions during turn-on. The frequency response may have a different distribution as a function of I_c and V_{CE}. Nonetheless, a device that is slow to turn on is likely to be slow turning off; so that the general switching-speed characteristics of a transistor can be inferred from its speed during turn-on.

4. Scaling Laws

4.1 I_m

Fig. 4 shows the dependence of I_m on BV_{CEO} for devices with the three emitter areas given in Table 1. Each data point represents the average value of measurements from ten or more devices. The three emitter areas used are in the ratios 1.0:1.56:2.1. The numbers in parentheses next to each curve in Fig. 4 are the measured ratios of I_m at a given value of BV_{CEO}: 1.0:1.6:2.5. This result suggests that for a given BV_{CEO}, I_m scales with emitter area, and not as emitter periphery, since the emitter peripheries scale as 1.0:1.4:1.8 (see Table 1). A straight-line fit to the data indicates that I_m decreases as $(BV_{CEO})^{-1.5}$. Fig. 5 shows the data of Fig. 4 normalized to the

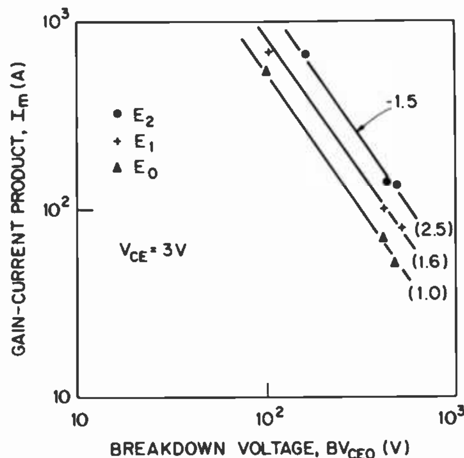

Fig. 4—The empirical relationship between gain-current product and breakdown voltage for devices with three different emitter areas. The slope of the lines is −1.5. Shown in parentheses next to each curve is the empirical scaling factor for each different emitter area. area.

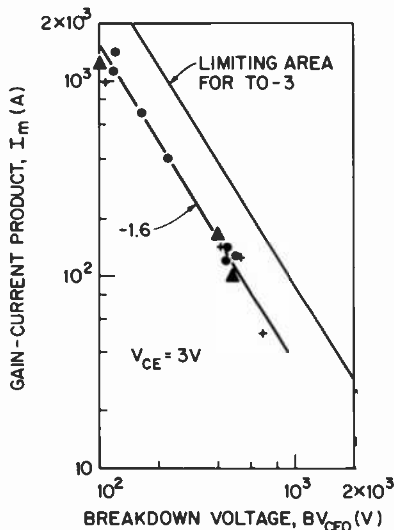

Fig. 5—The same as Fig. 4, but with additional data and with all data normalized to the largest emitter area, A_2. The slope of the straight-line fit is -1.6.

largest emitter area A_2. (Additional data have been added to Fig. 5). The straight-line fit gives a log-log slope of -1.6, which is in reasonable agreement with the curves in Fig. 4. Assuming that a 1 cm^2 (394 × 394 mil^2) chip is the largest chip to be put into a TO-3 transistor header, we have indicated the expected I_m-BV_{CEO} line for this maximum chip size in Fig. 5. These results show that a transistor's current handling power decreases rapidly with blocking voltage.

The data of Figs. 4 and 5 permit the selection of an emitter area and, hence, chip size for a particular device. Assume one wishes to have a BV_{CEO} = 450 V and a dc gain of 10 at I_c = 3 A and V_{CE} = 3 V (i.e., I_m = 30 A). From either Fig. 4 or Fig. 5, one finds that the emitter area should be 0.56 A_o, and since chip size scales as emitter area (see Table 1), the new device can be made on a roughly 0.19 × 0.19 cm (75 × 75 mil) chip.

Figs. 4 and 5 show the behavior of I_m with V_{CE} held constant at 3 V. Often, high-current gain is specified at other values of V_{CE}. Fig. 6 shows the dependence of I_m upon V_{CE}. These data are taken with devices having BV_{CEO} = 510 V and they are normalized to the largest emitter area, A_2. Over the V_{CE} values of 1 to 5 V, I_m varies by about a factor of two. The data of Fig. 6 give the adjustment required in the curves of Figs. 4 and 5 when V_{CE} changes from 3 V to a value between 1 and 5 V.

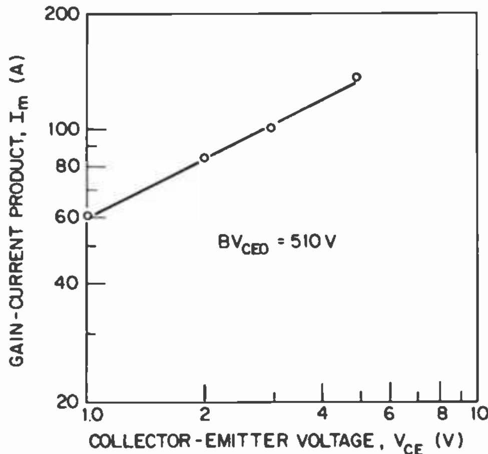

Fig. 6—The variation of the gain-current product, I_m, with collector-emitter voltage, V_{CE}. BV_{CEO} is fixed at 510 V.

4.2 I_{cr}

Fig. 7 shows the dependence of I_{cr} on BV_{CEO}. $I_{cr} \propto (BV_{CEO})^{-2.7}$. I_{cr} also scales with emitter area, but it decreases more rapidly with BV_{CEO} than does I_m.

If, for a given breakdown voltage, the collector region impurity profile is altered to minimize the collector region resistance, one finds that the collector resistance is proportional to the breakdown

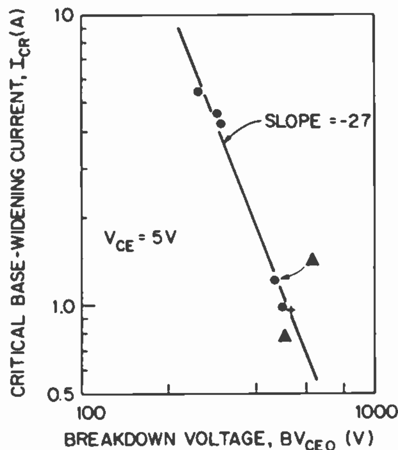

Fig. 7—The empirical relationship between the critical current for base-widening and breakdown voltage. The log-log slope (−2.7) is shown.

voltage raised to the 2.6 power.[10] In the present model, I_{cr} is inversely proportional to the collector resistance. Therefore, we expect I_{cr} to be proportional to $(BV_{CEO})^{-2.6}$ *if* the collector resistance has been appropriately minimized. Our experimentally derived exponent of -2.7 shows that we have achieved this nearly optimal condition. More importantly, our results agree well with the calculation relating, albeit indirectly, I_{cr} with BV_{CEO}.

Fig. 7 illustrates that the limiting frequency response or speed of a transistor switch decreases very quickly with increasing BV_{CEO}. One may compensate for this loss in speed at higher breakdown voltages by increasing the emitter area. Increasing the emitter area, however, overcompensates for the loss in current-handling capability with increasing BV_{CEO}, since I_m decreases only as $(BV_{CEO})^{-1.6}$ (see Figs. 4 and 5).

The onset of base-widening results from the forward biasing of the collector-base junction. As stated above, when the resistive voltage drop of the collector current passing through the lightly doped collector region equals the applied collector-base voltage, no applied reverse voltage exists across the collector-base junction. This condition defines the critical current, I_{cr}. One expects, therefore, that I_{cr} will be linearly related to the applied collector-base voltage through the collector conductance.

Fig. 8 shows the variation of I_{cr} with V_{CB} for a device with BV_{CEO} = 330 V. Also shown is the collector conductance as computed from

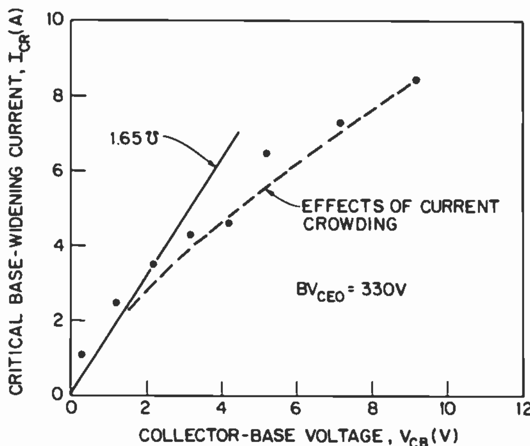

Fig. 8—The variation of the critical current for the onset of base-widening, I_{cr}, with collector-base voltage, V_{CB}. The collector conductance of 1.65℧ is shown as the solid line. The effects of base current crowding are shown by the dashed line.

the two-point spreading resistance data for the collector resistivity profile; the collector conductance is 1.65℧. The emitter area is A_2. At values of I_{cr} less than about 3 A, there is a nearly linear relationship between I_{cr} and V_{CB}. Beyond I_{cr} = 5 A, I_{cr} values fall below the line given by the collector conductance, and they become increasingly sublinear with increasing V_{CB}. This tendency is in part the consequence of current crowding in the base beneath the emitter,[11] which geometrically decreases the collector conductance. The dashed line shows the calculated effect of current crowding beneath an emitter finger (see Appendix).

Fig. 9 shows the data of Fig. 8 plotted as a function of the collector-emitter voltage V_{CE}. The empirical, straight-line fit indicates an effective collector conductance of 1.15℧. The data of Fig. 9 allow the designer to adjust the I_{cr} versus BV_{CEO} data of Fig. 7 should a specification on I_{cr} be given for values of V_{CE} other than 5 V.

In terms of switching parameters, the importance of I_{cr} is readily visualized. When switching along a resistive load line, R_L, the rise time, storage time, and fall time characterize the speed with which a transistor moves between the off-state ($I_c \cong 0$, $V_{CE} = V_{cc}$) and the on-state [$I_c \cong V_{cc}/R_L$; $V_{CE} = V_{CE}$(Sat)]. The rise time, t_r, is the time it takes for I_c to rise from ten percent to ninety percent of its maximum value. After a reverse base-current pulse has been applied to turn the unit off, the storage time, t_s, is the time required for the current to drop to ninety percent of its maximum value. The fall

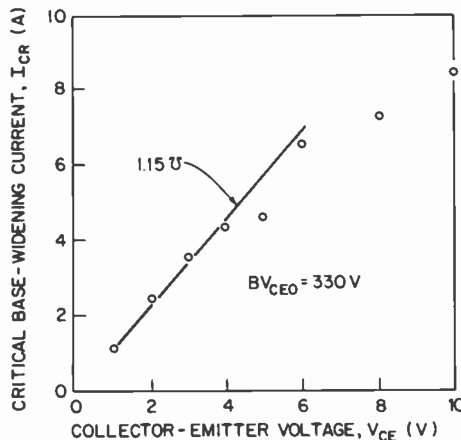

Fig. 9—The variation of the critical current for base-widening with collector-emitter voltage, V_{CE}. These data are those of Fig. 8. The solid line gives the effective collector conductance of 1.15℧.

time, t_f, is the time it takes the current to drop from ninety percent to ten percent of its maximum value.

For a fixed value of V_{CE} these times increase rapidly with increasing current, once the collector current exceeds I_{cr}. This is shown in Fig. 10, where t_r, t_s, and t_f are plotted versus I_c at $V_{CE} = 3$ V, and $V_{cc} = 200$ V. The device used in these measurements had an emitter area A_2 and $BV_{CEO} = 340$ V. R_L was adjusted to obtain I_c at $V_{CE} = 3$ V. Also shown are h_{FE} and f_T as a function of I_c ($V_{CE} = 3$ V). Once I_{cr} is reached at $I_c \cong 3$ A, all switching times increase very rapidly. Notice that h_{FE} does not drop off rapidly at $I_c = I_{cr}$.

5. Discussion and Conclusion

The results stated above are for a particular class of transistors, and the ranges of BV_{CEO}, I_{cr} and I_m over which data were taken are limited. Extrapolation far beyond the limits of the variables discussed for devices in this class should be undertaken cautiously. Close to these limits, the guidelines provided above are accurate and helpful.

All curves of I_m versus BV_{CEO} are presented at a constant value

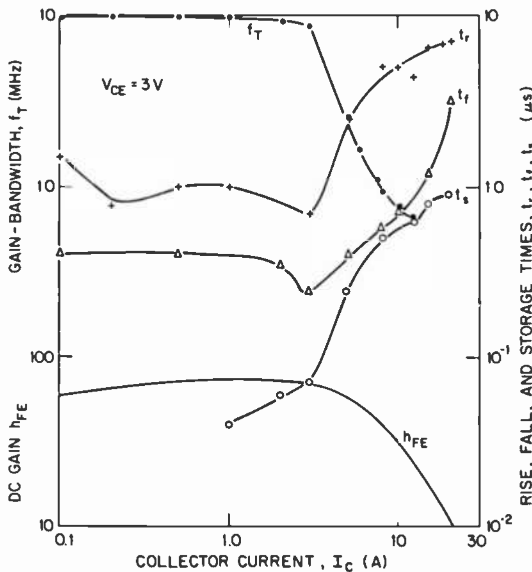

Fig. 10—Switching times for a device switching a resistive load as a function of collector current at constant collector-emitter voltage. Gain and gain-bandwidth characteristics are also shown.

of V_{CE}, irrespective of the devices' BV_{CEO} value. Since one expects a higher saturation voltage in a device with a higher BV_{CEO}, one might wish to use a higher constant value of V_{CE} for devices with higher values of BV_{CEO}. The rationale to do so is that if a device handles a larger amount of power, it can dissipate a larger amount of power in saturation. This notion has merit. The effect of such a procedure is to have I_m fall off less rapidly with BV_{CEO}.

For a given device structure, improvements in I_m result from increased emitter efficiency[12] and collector-base reverse-recovery time.[13] The results stated above would be similar for an improved device; but for a given set of current and voltage specifications, a smaller chip size could be used.

There are other important design parameters for power transistors. The list includes energy-handling capability, in both the forward and the reverse switching modes, and input and output reactances. Although attention was paid to these parameters in the fabrication of the sets of transistors used in this study, they were not studied as a part of the work reported.

In summary, we have found that both I_m and I_{cr} scale with emitter area and, hence, chip size. I_m scales as $(BV_{CEO})^{-1.6}$ and I_{cr} scales as $(BV_{CEO})^{-2.7}$. These relationships are reliable guides in the design of power transistor switches.

Acknowledgments

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Appendix

The geometrical increase in collector resistance arising from current crowding can be approximated in the following way. Fig. 11 shows schematically the vertical cross section of half an emitter finger of width $W_E/2$. The collector resistivity is assumed to be uniform; the collector width is designated W_c. The lower ohmic contact spans the entire half finger. The breadth of the upper ohmic contact depends on the degree of current crowding in the base beneath the emitter.[11] When the base current beneath the emitter causes significant voltage drops, current injection from the emitter into the collector occurs over a distance X_o. X_o is given by the approximate formula[12]

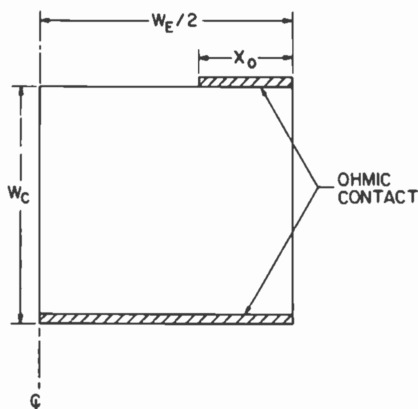

Fig. 11—Schematic cross section of half an emitter finger. Current crowding limits injection to an area X_o wide.

$$X_o = \frac{2kTPh_{FE}}{qR_{SB}I_c}, \quad X_o \leqslant W_E/2. \qquad [1]$$

k is the Boltzmann constant, T is the absolute temperature, P is the emitter periphery, q is the electronic charge, and R_{SB} is the sheet resistance of the base beneath the emitter. When $X_o \geqslant W_E/2$, the collector resistance is minimal and injection occurs over the entire emitter finger. When $X_o < W_E/2$, collector current is restricted, and the resistance increases.

An approximate formula for the increased collector resistance in ohms is[14]

$$R_c = R_{co}\left\{1 - \frac{W_E}{\pi W_c}\ln\cos\left[\frac{(W_E - 2X_o)\pi}{2W_E}\right]\right\}. \qquad [2]$$

R_{co} is the uncrowded, minimal collector resistance. Eqs. [1] and [2] were used to generate the dashed-line curve in Fig. 8, giving a good description of the effects of current crowding on I_{cr} and, hence, on the switching speed of a transistor.

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Patents Issued to RCA Inventors—First Quarter 1983

January

J. R. Archer Deflection Yoke Incorporating a Permeable Corrector (4,369,418)
G. R. Briggs Vehicle Multiplex System (4,370,561)
G. N. Butterwick Evaporator Support Assembly for a Photomultiplier Tube (4,370,585)
M. G. Caracappa Signal Correlation Means Employing Charged-Coupled Device Type Shift Registers (4,370,726)
D. J. Carlson and W. L. Lehmann Phase Locked Loop Tuning System Including a Prescaler Conditioned to Oscillate at an Out-of-Band Frequency (4,368,540)
J. W. Chamberlain and A. M. Goldschmidt Vertical Sync Independent Digital Skew Servo (4,368,492)
C. F. Coleman VideoDisc Player Having Record Retaining Mechanism (4,370,738)
A. T. Crowley Phase Comparator System (4,370,653)
N. V. Desai, R. F. Poll, and B. L. Goydish Method for Removing Carbon Particles From a Molded Article (4,369,307)
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G. A. Reitmeier Two Dimensional Adaptive Dropout Compensator and Chroma Inverter (4,376,955)
G. A. Reitmeier Adaptive Error Concealment (4,377,820)
M. D. Ross Slow Down Processor for VideoDisc Mastering Having Color Phase Error Detector/Corrector (4,376,954)
J. P. Russell System for Compensating for Intensity Variations and Beam Landing Errors in Flat Panel Display Devices (4,376,260)
A. Schwarzmann High Power, Low Frequency, Electronically Adjustable Attenuator (4,378,536)
F. N. Sechi Microwave Power Circuit With an Active Device Mounted on a Heat Dissipating Substrate (4,376,287)
R. L. Shanley, 2nd and R. P. Parker Signal Gain Control With DC Compensation (4,376,288)
R. W. Shisler and W. H. Barkow Television Deflection Yoke Having a Toroidally-Wound Deflection Coil (4,376,273)
J. O. Sinniger and A. D. Robbi Digital Timing System for Spark Advance (4,375,209)
B. N. Steven and L. R. Aldridge Apparatus and Method for Cleaning Recorded Discs (4,375,992)
A. Troiano Noise Responsive Automatic Peaking Control Apparatus (4,376,952)
G. J. Whitley System for Securing Component Leads to Printed Circuit Boards (4,377,026)
R. Williams Metal Electrode for Amorphous Silicon Solar Cells (4,378,460)
D. H. Willis Television Receiver Ferroresonant Power Supply Disabling Circuit (4,377,775)

AUTHORS

John F. Corboy is an Associate Member of Technical Staff at RCA's David Sarnoff Research Center, Princeton, NJ and is a member of the Materials Synthesis Group within the Materials and Processing Research Laboratory. He joined RCA in 1959 working on the epitaxial growth of III-V compounds and the synthesis and crystal growth of organic compounds. From 1965 to 1980, he studied the properties of silicon on insulating substrates and was involved in the transfer of silicon-on-sapphire technology between RCA Laboratories and other divisions of RCA. Currently, he is involved in silicon homoepitaxy and in plasma etching of oxide films.

Mr. Corboy was the recipient of an individual RCA Laboratories Achievement Award in 1974.

Glenn W. Cullen is Head of the Materials Synthesis Research group within the Materials and Processing Research Laboratory. He received the BS degree in Chemistry from the University of Cincinnati in 1953 and the PhD degree in Inorganic Chemistry from the University of Illinois in 1956. During the following two years, he served on the teaching staff and as a Group Supervisor in the Electronics Department of the U.S. Army Air Defense School (Surface to Air Missiles) at Ft. Bliss, TX, and was released from the Army Reserve Corps with the rank of Captain.

In 1958 Dr. Cullen joined RCA Laboratories, Princeton, NJ, as a Member of Technical Staff. Initially, he worked on the chemical stabilization of semiconductor surfaces. Later he was involved in the chemical-vapor deposition of Nb_3Sn, Nb, Ta, and Nb-Ta superconducting thin films. This activity included characterizing the electrical properties of the deposits at low temperatures in high magnetic fields. He then became involved in preparing and characterizing silicon thin films epitaxially deposited on insulating substrate materials.

Dr. Cullen received an RCA Laboratories Outstanding Achievement Award in 1963 and 1969. He was also a member of research teams that received David Sarnoff Corporate Research Team Awards in 1965 and 1973.

Dr. Cullen is a member of the American Chemical Society, the Electrochemical Society, the Society of Sigma Xi, and Alpha Chi Sigma. He has served as the chairman of the Electronics Division of the Electrochemical Society and as Chairman of a Gordon Research Conference on Crystal Growth. He has also served as a Trustee of the Federation of Materials Societies, as a member of a National Material Advisory Board Committee on high-purity silicon, and as a member of an Air Force Science and Technology Advisory group. He is a member of the Executive Committee of the American Association for Crystal Growth, and an Associate Editor of the *Journal of Crystal Growth*.

Arthur Dreeben completed his graduate work in Inorganic and Solid State Chemistry and Physics at the Polytechnic Institute of Brooklyn in 1950, after serving with the U.S. Army during World War II. He held a Teaching Fellowship at the Polytechnic and did research on infrared stimulable phosphors.

From 1950 to 1953 he was employed as a Research Chemist at the General Electric Research, and the Knolls Atomic Power Laboratories, on the development of analytical and radiochemical procedures. In 1953 he joined the Research Department of the Westinghouse Lamp Division as a Research Engineer. Here he did research in the field of luminescence including high-temperature phosphors, lamp phosphors, and transparent luminescent films.

He joined RCA Laboratories in 1958 as a Member of Technical Staff. He has worked on photoconductors, electroluminescence, and problems in crystal growth, dislocations and impurity precipitation in semiconductors. The latter work led to a better understanding of impurity behavior by identifying classical precipitate behavior, morphologies, and species in cadmium sulfide single crystals. He has also been concerned with the growth and properties of epitaxial layers of III-V compounds for various transferred-electron microwave devices including GaAs traveling wave transistors, and a novel type of solid state traveling wave amplifier. He developed a process for growing single-crystal sapphire using a CO_2 laser, and filaments from the process were made into the first video disc styli. He was also concerned with research and development of the EFG shaping technique for growing single-crystal sapphire ribbons for SOS devices. More recently he has been studying the relationships between the crystalline perfection of silicon substrates and the quality of homoepitaxial silicon.

Listed in "American Men and Women of Science", he is a member of the American Chemical Society, the Electrochemical Society, the American Association for Crystal Growth, Phi Lambda Upsilon and Sigma XI.

Michael T. Duffy received the BSc degree in chemistry from University College, Dublin, in 1958 and completed his PhD studies in solid state chemistry in 1963. He was a teaching assistant at this University from 1961 to 1963. In 1964 he joined the University of Toronto as Research Associate and worked in molecular beam research until July 1966 when he joined the staff of RCA Laboratories. Since then he has been engaged in materials research in the field of integrated electronics. He has worked on the synthesis and characterization of various dielectrics in MIS structures and on the vapor phase growth of heteroepitaxial materials on insulating substrates, particularly sapphire. His work also included evaluation of CVD materials for contact with molten silicon. More recent work involved analysis of the surface perfection of polished sapphire substrates and heteroepitaxial silicon films by IR and UV reflectance methods. He is currently involved in the development of processes for the reactive ion etching of dielectric films for VLSI processing and the characterization of amorphous and polycrystalline silicon films for VLSI application.

Dr. Duffy has been the recipient of three RCA Laboratories Achievement Awards for research contributions. He is a member of the Electrochemical Society.

Ray Ford received a BSEE degree from Wilkes College in 1974. He joined the RCA Power Design Activity in Somerville, NJ, as a Design Engineer. In this capacity he participated in the device design/development of the Switchmax line of RCA Power Devices for use in off-line switching power supplies. He also worked on a radiation-tolerant device TA9107 currently targeted for use in the MX AIRS Missile Program. In 1976 Mr. Ford transferred to the Power Device Development Group in Mountaintop, PA, where his responsibilities included the transfer of Power Device Designs into manufacturing. In 1978 Mr. Ford was named Engineering Leader of the newly formed Power MOS Design Activity in Mountaintop. His current position is Manager, Power MOS Design and Product Engineering.

Alvin Malcolm Goodman received a BS degree in Electrical Engineering from Drexel University, Philadelphia, PA, in 1952. He received an MA in 1955, and a PhD in 1958, both from Princeton University. From June 1956 to January 1957 he served as Research Assistant at Princeton University and then, up to June 1959, as Assistant Professor of Electrical Engineering at Case Western Reserve University, Cleveland, OH. He performed research at RCA Laboratories as a summer employee in 1954, 1955, and 1958, and became a Member of Technical Staff in June 1959. In 1982, Dr. Goodman was promoted to Senior Member of Technical Staff. During the year 1970–71, Dr. Goodman engaged in postdoctoral studies at the Swiss Federal Institute of Technology (Zurich).

Dr. Goodman has specialized in solid-state physics and semiconductor measurements and processing. He has received three RCA Laboratories Achievement Awards for work on metal-semiconductor contacts (1963), MNOS (*m*etal-*n*itride-*o*xide-*s*ilicon) memory devices (1969), and the passivation of semiconductor devices (1978). From 1973 to 1976, Dr. Goodman served as a Member of the Editorial Board of *Review of Scientific Instruments.* He is a member of the American Physical Society and Sigma Xi, a Senior Member of IEEE, and is listed in *American Men and Women of Science* and *Who's Who in Technology Today.*

Lawrence A. Goodman received the BS, MS, and PhD degrees in Electrical Engineering from Massachusetts Institute of Technology in Cambridge, MA. In 1970, after completing his doctoral dissertation on the optical properties of cadmium sulfide, he joined RCA Laboratories, Princeton, NJ.

At RCA, Dr. Goodman was initially concerned with various aspects of liquid-crystal displays. These investigations included studies of electrode preparation, surface-alignment phenomena, bulk electrooptical effects, and various electrical-addressing techniques. Recently, his research effort has concentrated on the design and fabrication of power MOS field-effect transistors and the effect of process-induced defects on the performance of bipolar and MOSFET transistors.

Dr. Goodman has received two RCA Laboratories Achievement Awards. He has also lectured on liquid-crystal displays and served as coeditor of an issue of *IEEE Transactions on Electron Devices* on displays. He is a member of IEEE, Tau Beta Pi, and Eta Kappa Nu.

Herman F. Gossenberger received BCemE and MChemE degrees from the Polytechnic Institute of Brooklyn in 1957 and 1959, respectively. He held a Sandia Corporation Research Fellowship from 1957 to 1959, and participated in a study directed toward optimizing the performance of nickel-cadmium batteries. In 1959 he joined Philco Corp. working on indium antimonide infrared detectors.

In 1961, Mr. Gossenberger joined the Materials Research Laboratory of RCA Laboratories, Princeton, NJ, and performed research on the formation of ohmic contacts to silicon and germanium, the stabilization of germanium surfaces, and the vapor-phase growth of germanium and niobium stannide. He has worked on numerous projects involving the vapor-phase growth of III-V semiconductor compounds for materials characterization and for device applications such as electroluminescent diodes, laser diodes, bipolar transistors, photoemitters, and secondary emitters. He has also worked on various projects requiring the application of low-pressure CVD for depositing thin films of such materials as amorphous and polycrystalline silicon, SIPOS, silicon nitride, and silicon dioxide. He is currently involved in an evaluation study of various gettering techniques used to minimize the introduction of impurities and defects into silicon during high-temperature processing steps.

Mr. Gossenberger received an RCA Laboratories Outstanding Achievement Award in 1979 for contributions to a team effort in the preparation and characterization of SIPOS layers utilized for the passivation of semiconductor devices. He is a member of the Electrochemical Society and IEEE.

Günther Harbeke received the Physics Diploma in 1955 and the PhD in Physics in 1958 from the Technical University in Brunswick, Germany. In 1961 he joined the staff of Laboratories RCA Ltd., Zurich. Prior to that he was with the Physikalisch-Technische Bundesanstalt in Brunswick. In 1963, he worked for 9 months at the RCA Laboratories in Princeton. Dr. Harbeke has been working in research on the basic optical properties of semiconducting and insulating materials and on light scattering and phase transitions in solids. He received RCA Laboratories Achievement Awards for team performance in 1962 and in 1969. Dr. Harbeke has a lecturing assignment at the University of Cologne and is a member of the Zurich, Swiss, German, and European Physical Societies.

Lubomir Jastrzebski received an MS degree in Physics from the University of Warsaw in 1971 and a PhD degree from the Polish Academy of Science in 1974.

From September through December 1974 he taught a graduate course on the optical and magneto-optical properties of solids at the Institute of Physics, Polish Academy of Science. At MIT, where in 1975 he began work as a visiting scientist with the Electronic Materials Group in the Materials Science and Engineering Department, he was appointed a Research Associate in 1976. In 1979 Dr. Jastrzebski joined RCA Laboratories as a Member of Technical Staff.

His scientific activity has been concentrated in the areas of crystal growth

of semiconductor and magnetic materials and device structures, the processing of semiconductor devices, the characterization of electronic properties of materials, interface phenomena related to device performance, and energy conversion.

He is now involved in the analysis of the microstructure of silicon for application in charge-coupled devices. He is studying the relationship between defects in starting material and those developed by processing, and the influence of both the original and process-induced defects on device performance.

He is a member of the American Physical Society and the American Association for Crystal Growth.

Liselotte Krausbauer received the diploma in physics from the University of Marburg, West Germany, in 1957. For 2 years she worked in the research institute of the West-German coal mining industry in Essen/FRG on the characterization of dust by optical methods and spent another 2 years in the development group for semiconducting devices and ICs of Grundig, Fürth/FRG. In 1962 she joined RCA Laboratories, Zürich, as a member of technical staff. She worked on the photoconductivity and photoluminescence of insulating and semiconducting materials for which she received an RCA Outstanding Achievement Award for her team contribution. She is now concerned with materials characterization by electronmicroscopy (transmission and scanning), X-ray, and optical methods. She is a member of the Swiss and West German Physical Society.

Ramon U. Martinelli received his AB and MS degrees from Dartmouth College in 1960 and 1962, respectively. In 1965, he received a PhD in Electrical Engineering from Princeton University.

Dr. Martinelli joined RCA Laboratories in 1965 and worked on various problems related to secondary and photoemission. He was the first to achieve bandgap-limited electron emission from silicon; for this he received an RCA Laboratories Achievement Award in 1970.

Since 1973, Dr. Martinelli has been working on numerous problems associated with power transistor design and development. An important product he was instrumental in developing was a 15-A, 450-V switching power transistor. In 1977 he received an RCA Laboratories Achievement Award for this work. Dr. Martinelli continues to work in such power-transistor areas as minority-carrier lifetime measurement and control, deep-level trap spectroscopy, and second breakdown in power transistors.

Dr. Martinelli is a member of the American Physical Society.

Joseph T. McGinn received his BS in Physics (with honors) in 1969 from Lowell Technological Institute, Lowell, MA, his MS in 1978 from the Mechanics and Materials Science Department of Rutgers University, and his PhD in 1981 from the same department.

Dr. McGinn joined RCA Laboratories as a Member of Technical Staff in 1969 and has been part of the Materials Characterization Research Group. His work has been principally in the area of characterization of electronic materials through the use of transmission electron microscopy and x-ray studies. He is currently actively engaged

in the study of deposition kinetics of LPCVD silicon at low temperatures and the growth of single crystalline films over amorphous insulators.

The areas in which Dr. McGinn has done extensive work leading to publication include: the initial growth of silicon in Al_2O_3; laser annealing of hydrogenated amorphous silicon; the role of buffered layers in the degradation of LEDs and solid-state lasers; the effect of oxygen doping on the structure of polysilicon films; the morphology of slope evaporated SiO_x films for liquid-crystal displays; the fault structure of fine gold particles in a silica matrix; the theory of annealing twin formation; and the defect structure and theory of fault formation of single-crystal silicon films grown over amorphous films.

Robert Metzl attended the University of Virginia as a National Merit Scholar and graduated from Johns Hopkins University, Baltimore, MD, with a degree in Electrical Engineering. He also received credits in graduate Ceramics courses at Rutgers University. He completed courses in computer programing, interfacing, and design while at RCA Laboratories, as well as courses in technical writing and quality assurance analysis taught by previous employers.

Mr. Metzl joined RCA in 1972 as a Crystal Growth Specialist. In 1979, he was appointed an Associate Member of Technical Staff. He is currently associated with the Process and Applied Materials Research Laboratory and is engaged in fabricating integrated circuits for research in dielectric isolated circuit structures and in designing and implementing data acquisition and analysis systems and control systems for epitaxial growth of silicon films. Other projects include the use of microcomputers for data analysis of optical measurements and for local training in digital-data acquisition and analysis.

Mr. Metzl spent eight years designing and implementing research and production systems for sapphire-ribbon growth and fabrication for SOS, including crystal-growth furnace and associated controls, and the growth and fabrication process. He has also designed and implemented computer systems for the crystal-growth cycle.

Mr. Metzl's previous experience includes the development of crystal pullers and growth of refractory oxide crystals for laser and other optical uses at Allied Chemical Corp., quality planning, control, and analysis at Westinghouse, design testing and optimization of automotive electronics at Bendix, and technical direction of the University of Virginia Radio Television Center.

Mr. Metzl is a member of the American Association for Crystal Growth and the Metal Science Club of New York.

Gregory H. Olsen received the BS Physics in 1966 and BSEE and MS Physics (magna cum laude) in 1968 from Fairleigh Dickinson University, where he was a Teaching Fellow in the physics department. He attended the University of Virginia from 1968 to 1971 and received a PhD in Materials Science.

Upon graduation, Dr. Olsen spent 18 months at the University of Port Elizabeth, South Africa, as a visiting scientist. While there, he continued his research on interfacial effects in metals. He developed a technique for growing dislocation-free iron whiskers and completed an extensive electron-microscope investigation of the epitaxial growth of iron on silver platelets.

In September 1972, Dr. Olsen joined RCA Laboratories as a Member of Technical Staff, where he has been involved with the vapor-phase crystal growth and characterization of III-V compounds for electro-optical applications. His fundamental studies on crystal defects have brought about marked improvements in photoemissive devices, lasers, LEDs, and avalanche photodiodes. This work has led to the commercial introduction of 1.3-μm InGaAsP LEDs, lasers, and photodetectors for optical communications. He has delivered numerous invited lectures on his research at international conferences, and has negotiated and directed many military and government research contracts.

Dr. Olsen has also studied growth defects in epitaxial silicon and has developed growth techniques for various hexaboride materials for application as thermionic emitters. He received RCA Outstanding Achievement Awards for his research in 1978 and 1980, and in 1980 was appointed a Research Leader in the Optoelectronics Group.

Dr. Olsen is active in many technical societies including the Electronic Materials Committee, the American Physical Society, and the Electrochemical Society. He is vice-president of the NJ Crystal Growth Association, Publicity Chairman for the 1982 IEEE IEDM Meeting and Program Co-Chairman for the 1984 American Association for Crystal Growth Conference. He was also the first recipient of the Young Author Award of the American Association for Crystal Growth in 1981.

Robert H. Pagliaro, Jr. joined RCA Laboratories, Princeton, NJ, in 1979 as a Research Technician in the Materials Synthesis Research Group, after completing three years at Indiana University of Pennsylvania as a Natural Science major prior to his employment. He was promoted to Technical Associate and Senior Technical Associate in 1981 and 1983, respectively. In 1983, he received a BA in Natural Sciences/ Physics Concentration from Thomas Edison State College.

His work has involved the CVD technique for developing processes, processing and characterizing silicon homoepitaxial films for devices such as impatt and varactor diodes and other multilayered silicon structures. He also has been involved in qualitative and quantitative performance analysis of: rf-heated barrel, IR-heated barrel, and rf-heated horizontal epitaxial reactors. The characterization of silicon heteroepitaxial films (silicon on sapphire) was part of his task in 1979 and 1980.

Anton Schujko joined RCA Laboratories in 1962 as a Research Technician after three years of laboratory experience, including epoxy laminate development at FMC Corporation. At RCA Laboratories he participated in the synthesis of fluorescent organic compounds, the formulation of magnetic coatings for computer discs and tapes, and in cadmium selenide vidicon research. More recently, he contributed toward improvements in the growth of shaped single-crystal sapphire, filaments by a laser technique, and ribbons by edge-defined, film-fed growth. Currently, he is a Senior Technical Associate involved in the characterization of silicon substrates and epitaxial layers.

Joseph M. Shaw received the BS degree in Physics from Seton Hall University in 1963. He has done graduate work in Metallurgy at the University of Pennsylvania.

After his discharge from the U.S. Navy in 1955, he was employed by E. I. du Pont de Nemours & Co., Inc., in Newark, New Jersey, as a member of the Physical Chemistry Laboratory of the Pigments Department. There he was concerned with the physical characterization of organic pigments and later with the development of flake pigments produced by the chemical vapor deposition of metals and oxide films.

In 1964 he joined the Process Research and Development Laboratory of RCA Laboratories, working on the application of vapor deposition techniques in the metallization of semiconductor materials. In 1970 he joined the Process and Applied Materials Research Laboratory and engaged in research and techniques relating to the vapor growth of insulators and oxides on MOS devices. He is presently a member of the Integrated Circuit Process Research Group. Mr. Shaw has received two RCA Laboratories Team Achievement Awards.

Ronald T. Smith joined RCA Laboratories as a Research Technician in 1963 after receiving a BS in Physics from Moravian College of Bethlehem, PA. He has studied as a part-time graduate student in the Department of Materials Science of the University of Pennsylvania completing three courses and the basis for a Masters Thesis. The Masters Thesis work has involved the solving of the crystal structure of YWO_2Cl.

He is presently a member of the Materials Characterization Group specializing in single-crystal x-ray diffraction studies. This area includes Laue, Weissenberg, pole-figure, and diffractometry techniques as well as computer-related data reduction programming. He has recently concentrated on the means for the characterization and qualitative comparison of thin films.

Richard A. Soltis is a Technical Associate at RCA's David Sarnoff Research Center, Princeton, NJ, and is a member of the Materials Synthesis Research Group within the Materials and Processing Research Laboratory. He joined RCA in 1960 working on the electrical characterization of III-V compounds, the characterization of photochromics, the chemical vapor deposition of thin film dielectrics and heteroepitaxial growth of III-V and II-VI compounds. He is currently involved in the characterization of polysilicon films and plasma etching of dielectrics.

Edgar F. Steigmeier received the Physics Diploma in 1955 and the PhD in Physics in 1960 from the Swiss Federal Institute of Technology (ETH) in Zurich. From 1960 to 1962, he worked for Brown Boveri Corporation, Baden, Switzerland, on heat conductivity and thermoelectricity. In 1962 he joined the Materials Research Laboratory of RCA Laboratories, Princeton, where he worked on basic properties and applications of thermoelectric materials such as Ge-Si alloys and III-V alloys, which has led to high efficiency materials for power generation. In 1964 he transferred to Laboratories RCA Ltd.,

Zurich. There he worked on problems of heat transport, on optical properties of magnetic semiconductors, and materials involving soft lattice vibrations and phase transitions. Later work was concerned with light scattering of layer structures and of inorganic and organic conductors. At present he is involved in materials characterization (by means of elastic, Raman scattering and optical scanner) of VideoDisc, Polysilicon and Storage Disc materials. In 1969 Dr. Steigmeier received an RCA Laboratories Achievement Award for his contributions to the study of materials by means of Raman effect, and in 1979 a second one for the invention of a laser scanner for dust and defect detection. During the academic year 1973/74, Dr. Steigmeier was a guest lecturer on Solid State Physics at the University of Fribourg, Switzerland. He is a member of the Zurich, Swiss, European, and American Physical Societies.

Alois E. Widmer received a BS degree in Electrical Engineering from the HTL Engineering School in Zurich, Switzerland in 1957. Until 1960 he was employed with Brown Boveri in Baden, Switzerland, where he was in charge of the manufacturing of high-power germanium and silicon diodes. In 1960 he joined the development laboratory of the RCA Semiconductor Division in Somerville, NJ, where he was involved in the field of various GaAs devices such as high temperature and varactor diodes. In 1962 he took up a position at the North American/Rockwell Science Center in Thousand Oaks, CA, where he worked on ion implantation methods for silicon device applications. He returned to Switzerland in 1965 and has been with Laboratories RCA Ltd., Zurich, since then. He has worked on various semiconductor material and device aspects, such as double heterojunction (GaAl) P structures for electro-optic modulation of light, and more recently on the growth aspects and characterization of polysilicon and silicide films for device applications.

Thomas J. Zamerowski received the BS and MS degrees in Chemistry from St. Joseph's College in Philadelphia, PA, in 1962 and 1964, respectively. His Master's thesis involved the synthesis of purine derivatives as potential antimetabolites under N.I.H. assistance. Until 1969, he attended Temple University under a teaching fellowship and worked on bandgaps and crystal field splittings of mixed transition metal oxides.

In 1970, he joined RCA Laboratories and has since been engaged in the vapor-phase growth of III-V compounds and their ternary and quaternary alloys for optoelectronic devices such as photocathodes, lasers, and LEDs. His most recent work has been connected with the growth of InGaAsP alloys for use as lasers, LEDs and photodetectors at 1.3 μm.