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Measurements of Noise in Charge-Coupled Devices*†

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Abstract—Experimental data are presented that verify the present theory of noise fluctuations in the operation of charge-coupled devices. This includes the correlated transfer noise due to trapping of charge signal by fast-interface states and white noise associated with optical and electrical introduction of input into a CCD register. Experimental results are also given on operation of an input circuit to a CCD register for introduction of signal with noise fluctuations that are less than shot noise.

1. Introduction

The charge-coupled device (CCD)[1] is an analog shift register with potential application in several important areas including image sensing, analog signal processing, and digital serial memory. The degree to which CCD's are incorporated into actual systems depends in large

* The material presented in this article, with the exception of Section 3.5, was presented originally at the 1972 International Electron Devices Meeting, Washington, D.C. on Dec. 4-6, 1972, in a paper, "Experimental Measurement of Noise in Charge-Coupled Devices," by J. E. Carnes, W. F. Kosonocky and P. A. Levine.

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measure upon their noise characteristics. Several workers[2-6] have more or less concurrently predicted, based upon analysis, that the CCD is inherently a low-noise device capable or S/N ratios on the order of 60 dB for reasonably sized structures. Most significantly, the noise level of the device is predicted to be low enough to permit image sensing operation at low light levels.[7] The work reported here was initiated to experimentally measure the noise levels of CCD's. It was found that the low noise predictions for these devices are essentially correct.

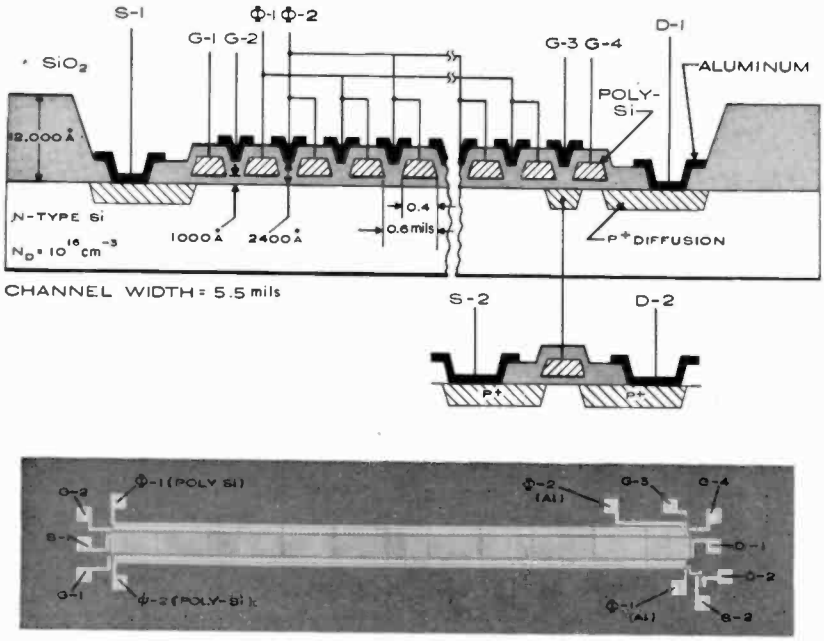

Fig. 1—Cross-sectional view and photomicrograph of 128-bit two-phase CCD shift register used in experimental measurements.

2. Experimental Procedure

The CCD's used in these noise measurements were 64- and 128-stage two-phase, polysilicon overlapped with aluminum gate devices.[8] A cross-sectional view of this device is shown in Fig. 1. The noise was measured using analog techniques with the CCD operating continuously at a clock frequency of 1 MHz. The experimental arrangement is shown in Fig. 2. The signal was introduced either electrically under control of the source diffusion voltage V_S and the input gate voltage

V_{IN} (actually two control gates were present as seen in Fig. 1) or by means of a movable light spot. This movable light spot allows the number of transfers to be varied using a single device and, thereby, provides a simple means for measuring noise associated with charge transfer within the CCD. The signal was voltage-sensed using the floating diffusion-source-follower output transistor (on-chip) combination. The dc signal level was also measured via an electrometer in the

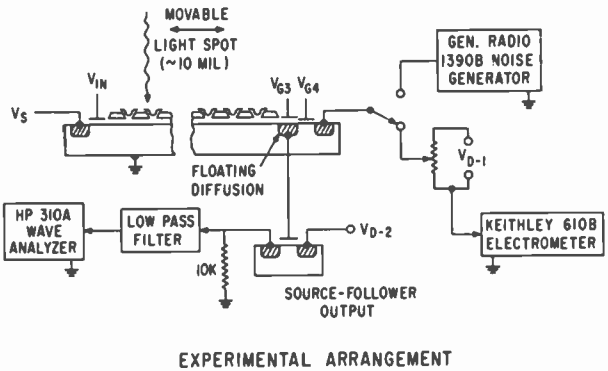

Fig. 2—Experimental arrangement of CCD noise measurements.

drain circuit. The noise level was measured using a wave analyzer.* A low-pass filter with cutoff at 500 kHz was used to exclude clock feedthrough voltages from the wave analyzer. Calibration was achieved by connecting a noise generator to the drain diffusion, biasing V_{G4} ON so the noise voltage also appeared at the floating diffusion and output transistor gate, and reading the noise level at the wave analyzer. This procedure essentially measured the transfer function of the output transistor and filter combination at the frequency of meansurement. Measurements were made using a wave-analyzer bandwidh ΔB of 3000 Hz with center frequencies ranging from 10 to 500 kHz. In this way the noise power spectrum could be measured.

3. Experimental Results

3.1 Clock Noise

The initial experimental observation was the presence of clock noise. This noise was not clock feed-through at the fundamental 1-MHz clock

* Hewlett Packard 310A.

frequency, but essentially white noise in the frequency spectrum of interest (< 500 kHz) due to the feed-through capacitance of phase-1 clock voltage to the floating diffusion. This background noise was unambiguously determined to be that associated with the clock pulsers. The magnitude of this background clock noise was about the same as the CCD noise sources introduced. Measurement of the CCD noise sources was therefore possible, but inconvenient and time consuming, since the background noise level had to be subtracted out in quadrature, point by point. In principle, a high-pass filter could be used to exclude this type of clock noise. In this experiment, the background noise was subtracted out in quadrature by hand, and all subsequent results reported have been processed in this manner.

3.2 Amplifier Noise

The noise associated with the output on-chip transistor was measured with the CCD clocks off, but with the dc voltages applied so that the output transistor was biased to its dc operating point. The thermal noise of the 10-kilohm load resistor and the transistor channel was below the sentivity of the measurement aparatus ($\sim 1\ \mu V$) and could not be observed. The $1/f$ noise of the transistor, however, was observable at frequencies below 10 kHz. No detailed quantitative measurements of this $1/f$ noise were taken.

3.3 Optical Signal Shot Noise

It was fully anticipated that any optically introduced signals would be accompanied by shot noise due to the quantum nature of photons. The mean-square, full-band (0–500 kHz) noise voltage at the floating diffusion ($F-1$) should be proportional to the average number of carriers in each charge packet N_{AVE} according to the equation

$$\overline{V^2}_{n,F-1} = \frac{q^2}{C_{F-1}{}^2} N_{AVE}, \qquad [1]$$

where C_{F-1} is the capacitance of the floating diffusion.

Since the drain current I_D is proportional to N_{AVE} according to

$$I_D = qN_{\mathrm{AVE}} f_c, \qquad [2]$$

where f_c is the clock frequency, we have for the full-band noise voltage

$$\overline{V^2}_{n,F-1} = \frac{qI_D}{C^2_{F-1} f_c}. \qquad [3]$$

Since full band is $f_c/2$, the mean-square noise voltage per Hz is then

$$\overline{v^2}_{n,F-1} = \frac{2qI_D}{C^2_{F-1} f_c^2}. \qquad [4]$$

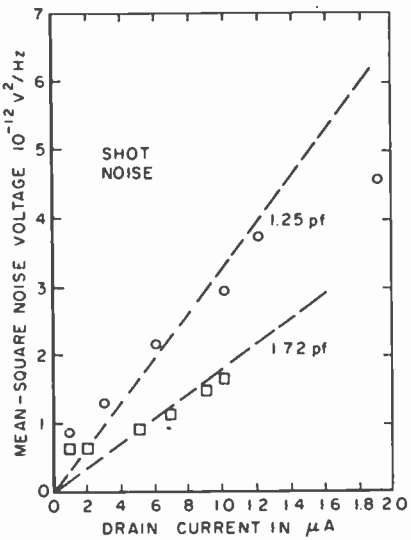

Fig. 3—Mean-square noise voltage per Hz referred to the floating diffusion vs. drain current. The data points represent two different devices. The dotted lines indicate shot noise theory with C_{F-1} as a fitting parameter.

Fig. 3 shows the mean-square noise voltage per Hz at the floating diffusion versus drain current for two different devices obtained by placing the light spot near the output, so that a negligible number of CCD transfers were required. Above I_D values of 0.4 μA the curve is reasonably linear with the dotted lines indicating a fit of Eq. [4], with C_{F-1} as a parameter. Measured values of C_{F-1} for these devices ranged btween 1.2 and 1.4 pF, reasonably close to the values determined by the shot-noise data. While these results are not surprising, they do serve to indicate that some degree of confidence in the experimental procedure and the quantitative results achieved therefrom is warranted.

3.4 Transfer Noise

The noise introduced by transfer of charge through the CCD was measured by moving the light spot away from the output. When this was done on devices with (111) substrate orientation with interface-state densities on the order of 10^{11} $(cm^2\text{-}eV)^{-1}$, an increase in the noise level was observed as shown in Fig. 4. The curves in Fig. 4 are

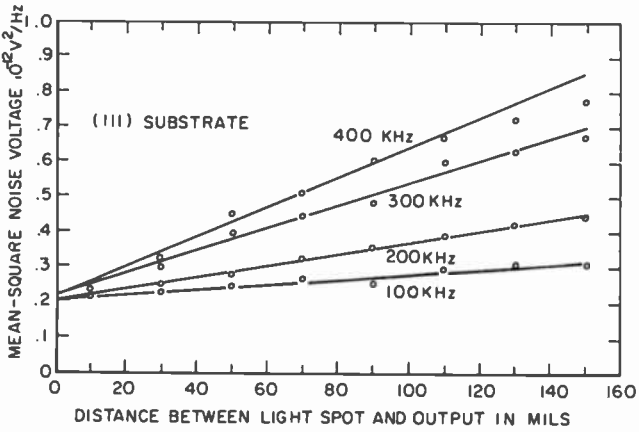

Fig. 4—Mean-square noise voltage per Hz vs. distance between light spot and output in mils. (One transfer occurs for every 0.6 mil). The parameter is the frequency of measurement. In all cases the measurement band-width was 3000 Hz.

for different measurement frequencies. The slope of the curves is proportional to the noise introduced at each transfer, and it is clear that this noise source is not "white". Thornber and Tompsett[6] have predicted that the spectral density of transfer noise in which the fluctuations of charge are correlated with adjacent packets should have the form

$$S_{TP}(f) \propto \left(1 - \cos \frac{2\pi f}{f_c}, \right) \qquad [5]$$

where $S_{TP}(f)$ is the spectral density of transfer process noise, and f is the measurement frequency.

Fig. 5 shows the slopes of the transfer noise of Fig. 4, on a per-transfer basis, plotted versus measurement frequency. Results for two different devices are shown. The bar on one data point indicates the typical range of the result when the measurement is repeated sev-

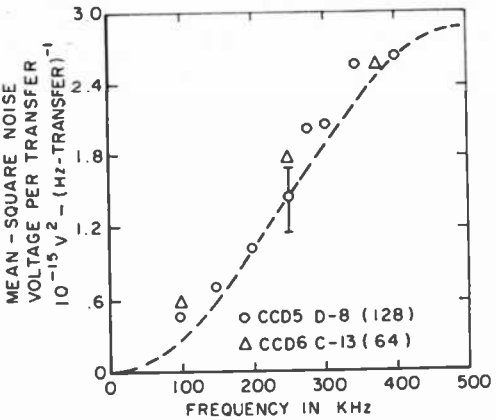

Fig. 5—Mean-square noise voltage per Hz per transfer vs. measurement frequency for a CCD on (111) oriented substrate. Results for two different samples are shown. The dotted line is the theoretically predicted spectral shape.

eral times. The dotted line indicates the shape predicted by Thornber and Tompsett with a magnitude appropriate for an interface-state density of 10^{11} (cm^2-eV)$^{-1}$, typical of (111) oriented substrates.

Further evidence that the transfer noise observed was due to interface state trapping fluctuations is shown in Fig. 6. Here the transfer noise is plotted versus drain current for both (111) and (100) substrates. The drain current in this test represents the charge signal,

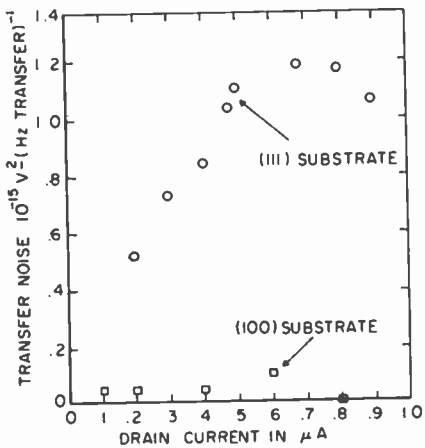

Fig. 6—Transfer noise per Hz per transfer versus drain current for (111) and (100) oriented substrates.

where about 0.9 μA corresponds to a full well. The (100) substrates typically have an order of magnitude fewer interface states than the (111) devices,[8] but they are in other respects identical. The transfer noise in the (100) device is at least ten times smaller than the (111) devices and is essentially unmeasurable for the 256 transfers and the background noise level involved here. Fig. 6 indicates one of the few departures from theory observed in these experiments. This departure involves the dependence of the trapping noise upon signal level. Our model (see Appendix 3 of Ref. [3]) indicates that the interface-state noise should be independent of signal level provided the signal is large enough to fill all states once each cycle. Disregarding the "edge effect" due to the fringing field under the storage and transfer gates,[9,10] this condition should occur for signal level densities given by

$$n_{SIG} > \frac{6f_o}{k_1}, \qquad [6]$$

where k_1 is a constant depending upon trapping center capture cross section and estimated to be $\sim 10^{-2}$ for the Si-SiO_2 interface.[11] Thus, under these assumptions, the interface state noise at 1 MHz might be expected to depend upon signal level only below signal densities of $6 \times 10^8\,cm^{-2}$, which for the devices used corresponds to drain currents of 1.3 nA. This discrepancy remains unresolved, although a more exact model based upon actual surface potential profiles may modify the expected results. However, it is our opinion that this particular departure from the theory is not sufficient to nullify the conclusion, based upon the results shown in Fig. 6, that the transfer noise observed in the (111) devices was due to interface-state trapping effects.

3.5 Noise Associated with Electrical Introduction of Signal

Our original analysis of noise suggests that it should be possible to introduce electrical signals into a CCD with less than shot noise, that is, with charge fluctuations associated with an RC circuit. The rms charge carrier fluctuations of an RC circuit is equal to $(1/q)\sqrt{kTC}$, which is 400 $\sqrt{C_{pf}}$ at room temperature[3] (C_{pf} is the value of the capacitance involved expressed in picofarads). Since the capacitance involved in a CCD is the capacitance of a potential well, C_{pf} can be on the order of 0.1 with rms fluctuations of only 126 at room temperature. In particular, such noise fluctuations should be independent of the size of the input-signal charge packet. In contrast, if charge representing 10% of a full well, which for the devices used in these measurements is

approximately 5×10^5 carriers, were introduced in such a manner that it was accompanied by shot noise, i.e., by optical means or by an electrical process involving a thermal excitation over a barrier (as would be the case where charge is "leaked" into the first potential well via a below-threshold channel), the rms shot-noise fluctuations would be ~ 700.

The measurements of the input noise, for operation of registers where the input signal is introduced into the first potential well by pulsing the input gates (G-1 and G-2 in Fig. 1), gave noise fluctuations several times larger than shot noise. Shot noise, however, was observed for optically introduced inputs and electrically introduced input when the charge is "leaked" into the first potential well via a below-threshold channel. The large noise fluctuations associated with the electrical introduction of input by pulsing the input gates with short-duration voltage pulses is probably connected with the collapse of the input channel and noise associated with the input pulse generator. When the input channel collapses, additional noise fluctuations arise, due to the partitioning of the channel charge between the source and the first potential well.

To minimize the noise associated with the collapse of the input channel, we have devised a low-noise input circuit. In the operation of this input circuit, the first potential well is initially overfilled and the excess charge is allowed to return to the source. The final amount of input charge is established by the height of the potential barrier under the first input gate. The same principle of operation was also described by Tompsett.[12] Another scheme for introduction of a low-noise fat zero that should have comparable performance was also recently reported by Emmons.[13,14]

The principle of operation of our low-noise input circuit is illustrated in Fig. 7. In this mode of operation the first potential well under G-2 gate is initially overfilled by applying a short pulse to turn on the source diffusion. Then, during the time when the source diffusion is turned off and while the excess charge signal flows back to the source, the input charge packet settles to its final magnitude. This is reached at the time just before transfer to the second potential well. For a fixed voltage applied to the G-1 gate, the size of the input charge packet depends on the voltage applied to the G-2 gate.

Another version of such low-noise input circuits that has been experimentally demonstrated (see Fig. 8) operates with the source diffusion maintained at a fixed potential. A dc offset voltage, corresponding to the input signal, is applied between the G-1 and G-2 gates and a common short-duration voltage pulse is applied. This operation

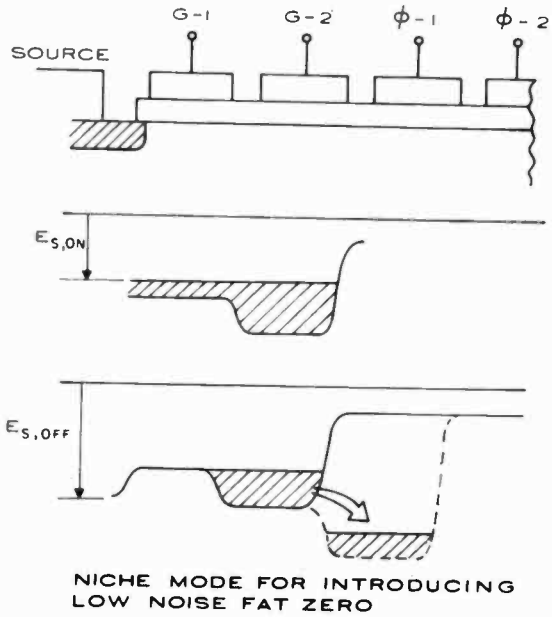

Fig. 7—Schematic diagram showing one mode of operation of the low-noise input circuit.

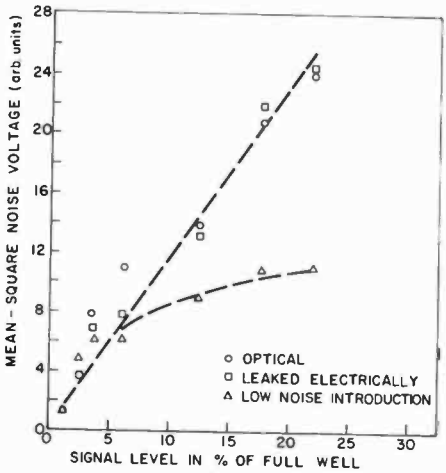

Fig. 8—Mean-sqaure noise voltage vs. signal level for optically introduced, electrically leaked, and low-noise electrically introduced signals.

results in "scooping" a low-noise charge-signal packet from the source and, during the following half-cycle, transferring it into the first stage of the shift register.

The experimental results[15] obtained on the operation of the low-noise input circuit are shown in Fig. 8. The measurements were performed at 100 kHz, and no quantitative calibration of the noise voltages observed was attempted. Transfer noise was negligible. The shot noise associated with optical inputs and electrical sub-threshold leakage inputs is also shown in Fig. 8 for comparison purposes.

As predicted, the fluctuations associated with the low-noise input show a clear saturation characteristic. The improvement in the measured noise level, however, was not as great as anticipated. The saturation level of the noise fluctuations from the data in Fig. 8 is about 3 times larger than the expected value of 400 $\sqrt{C_{pf}}$. Also, because the input gate structure of the register used for this test (See Fig. 1) was not designed for the low-noise operation, the maximum signal that could be introduced for the test in Fig. 8 was only 22% of the full well. It might be added at this point, that in order to have full flexibility for exercising the above low-noise input scheme using polysilicon–aluminum two-phase devices, a separate electrical access is needed to the first three to five gates.

Finally, it should be pointed out that the value for the rms noise fluctuations of 400 $\sqrt{C_{pf}}$ for introduction of electrical input and resetting of the floating diffusion was originally proposed[3] as a rough approximation for the noise associated with charging of a capacitor by a resistive channel. A more exact description of the noise associated with charging a capacitor by an IGFET channel was shown by Thornber[4] to be 400 $\sqrt{(2/3)C_{pf}}$. The same value was proposed by Boonstra and Sangster[16] for the noise-fluctuations associated with charge transfer between the stages of a bucket-brigade register.

To determine an exact expression for the noise fluctuations in the input charge packet for our low-noise input circuit, one must consider the details of the motion of charge returning to the source after the scooping process. This would enable one to determine the variance of the remaining charge packet just prior to transfer to the next stage. In the absence of such a detailed calculation, however, a reasonable estimate for this variance is kTC/q, since only the charge in potential band of kT/q should contribute significantly to the noise. This, indeed, turns out to be the same rms value of 400 $\sqrt{C_{pf}}$ as obtained for the RC circuit model.[3]

The low-noise input circuit is important for the introduction of low-noise fat zero necessary to achieve high transfer efficiency and

high dynamic range operation of surface channel CCD's. In addition, this circuit is useful for introduction of low-noise electrical signals into various analog and digital processing devices, including both surface and buried-channel CCD's.

4. Conclusions

The experiments described indicate that the low-noise predictions made for CCD's[2,3,4] are essentially correct. Noise associated with the transfer of free charge, expected to be small for efficient ($\eta \simeq 99.99\%$) CCD's was not observed. Transfer noise associated with interface state trapping was observed for devices on (111) substrates, but was too small to be observed on (100) substrates. The predicted spectral density of the transfer noise[6] was experimentally verified. Shot noise was observed when signals were introduced optically or were introduced electrically via sub-threshold channel leakage currents. The possibility of introduction of electrical input with fluctuations less than shot noise was experimentally demonstrated; however, the full low-noise potential of such an input circuit was not realized.

These low noise characteristics of CCD's, especially when low-noise input circuits are utilized, imply large dynamic range for analog devices, such as imagers and delay lines, and high light sensitivity for imagers.[7] These experimental results further confirm that the error-rate for charge-coupled memories will not be determined by CCD noise, since signal-to-noise ratios are very high (40-60 dB) for present state-of-the-art cell areas ($\sim 10^{-6}$ cm^2). Not until capacitor areas approach 10^{-8} cm^2 will CCD noise-induced error rates impose a fundamental limitation upon memory operation.

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A Microwave Automatic Vehicle Identification System

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Abstract—A microwave system using the second-harmonic reflection principle is used as a basis for an automobile labeling system. This system is capable of accommodating over 100 million different codes and can identify a vehicle passing at full speed from distances up to ten feet. Tolerances required for the interrogator–responder distance and orientation are quite loose. Optical systems and low-frequency induction systems (loop embedded in roadway) were also considered. Optical systems do not appear to have the capability of identifying one in over 100 million vehicles moving at highway speeds (the only such system known to have this capability is one designed to read railroad cars and employs a label 7 × 18 inches (18 × 46 cm), which is probably too large for use on private cars). Low-frequency induction systems require fairly large transponders on the vehicle, are somewhat critical in their mounting, and are not easily adaptable to other applications. The experimental microwave system described here uses a label 6 × 3 × ⅞ inches (15.2×7.6×2.2 cm), and it is expected this size could be reduced further. Systems operation and circuit design are described, and other possible applications for such a system are discussed.

1. Introduction

A practical system for automatic vehicle identification (AVI) would have many applications; one of the more immediate applications would be to enable the introduction of a billing system that could relieve the congestions that occurs at toll-collection points on highways and at bridges. At the present time, limited use is being made

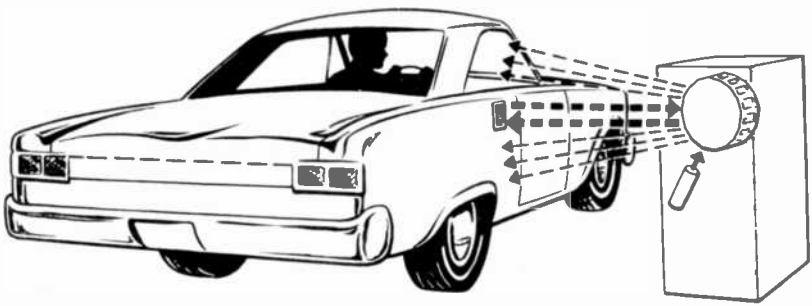


Fig. 1—Optical system.

of optical AVI systems, and various radio systems—both low-frequency induction loop and microwave—have been proposed. This paper describes a microwave AVI system that appears to offer considerable advantages over other systems.

Optical systems have the advantage that the identifying tag is simple and inexpensive—a series of strips printed on paper and glued to the window of the car, for example. There are several different techniques for scanning the tag. The simplest uses a multisurfaced rotating mirror and a light source such as a xenon lamp with suitable lenses. The most series defect of this technique for outdoor use is signal degradation due to weather effects and dirt. Also, for long codes and high vehicle speeds (see Fig. 1), the size of the tag may be too large for a passenger car.

The low-frequency induction loop systems are not as portable as

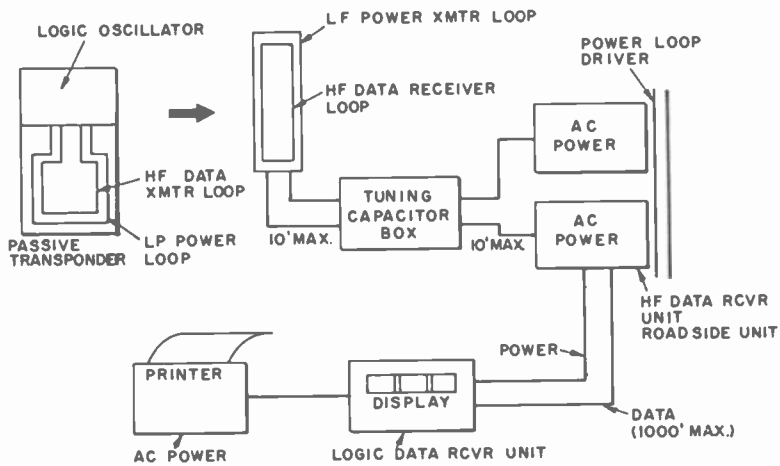


Fig. 2—Low-frequency induction system.

desired and the tag placement is generally more critical. Fig. 2 shows a typical implementation with the usual constraint that the tag not be closer than 3 to 4 inches (7.5 to 10 cm) from metal. Installation is customized for each type of vehicle and, therefore, the installed cost of the tag is likely to be high. Furthermore, the loop system is probably restricted to vehicle use on a highway and is not appropriate for applications such as airline luggage and personnel badges.

Other microwave systems require either substantial bandwidth[1] (as in the frequency scan system) or substantial interrogator power (as in the dual frequency transponder[2]).

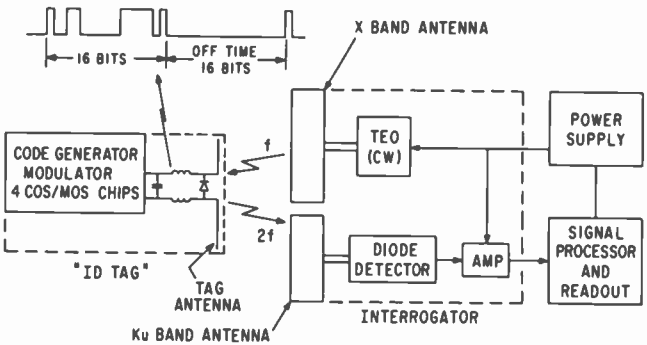


Fig. 3—Experimental automatic vehicle identification system.

2. Experimental Microwave AVI System

The experimental microwave AVI system described here offers all-weather operation and dirt immunity, is small and portable, requires small bandwidth, functions on low transmitter power (well within U.S. standards for radiation hazard), and is not critical as to its mounting position. The basic system, shown in Fig. 3, includes an interrogator operating at X-band to illuminate a passing tag which radiates back a coded signal at the second harmonic of the X-band input. The tag performs the frequency-doubling action by virtue of a nonlinear device (a Schottky-barrier silicon diode) connected across the terminals of the tag antenna via a matching section. The antenna is in the form of a flat, printed-circuit array of dipoles and is tuned to the geometric mean of the X-band received signal and the Ku-band (the second harmonic of X-band) re-radiated signal. This design provides good performance at both frequencies. To make the tag uniquely identifiable, the re-radiated signal is "on-off" keyed in coded

binary fashion. Keying, or modulation, is accomplished by the application and removal of the reverse bias on the doubler diode. Figs. 3 and 4 show the dc connection that is made to the diode to allow the bias modulation. The modulating waveform is derived from the COSMOS circuit code generator shown in Fig. 4. This circuit con-

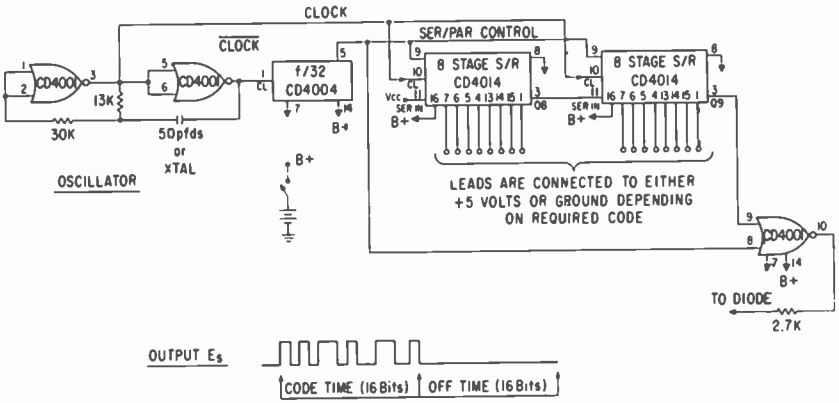


Fig. 4—Code generator/modulator for tag.

sists of four COSMOS chips: two eight-stage shift registers, four dual-input NOR gates on a single chip, and one counter. Two of the gates connected to two resistors and a crystal (or capacitor) form an oscillator which acts as the clock. The clock pulses shift the code, which is wired into the 16-stage shift register, to the output port. It will be noted that the counter output is used to reset the code word into the register after 16 clock pulses (the length of the word). This reset time lingers for 16 more clock pulses, which causes the register to output 16 consequtive "zeroes". The only other constraint on the code is that the first bit of the code word is always a "one". This configuration allows the decoder to easily recognize the beginning of each code word, as is discussed in more detail later. An example of a code word is shown below the circuit diagram of Fig. 4. The magnitude of the code waveform is roughly equal to the B+ voltage (4.5 to 6 volts). This voltage level provides sufficient back bias to prevent Ku-band re-radiation from the incident X-band signal that reaches the diode.

The coded amplitude-modulated signal is then re-radiated back toward the interrogator. A Ku-band receiving antenna accepts this signal and delivers it to an envelope detector whose output is amplified and clipped to 5 volts peak-to-peak. At this point, the signal is

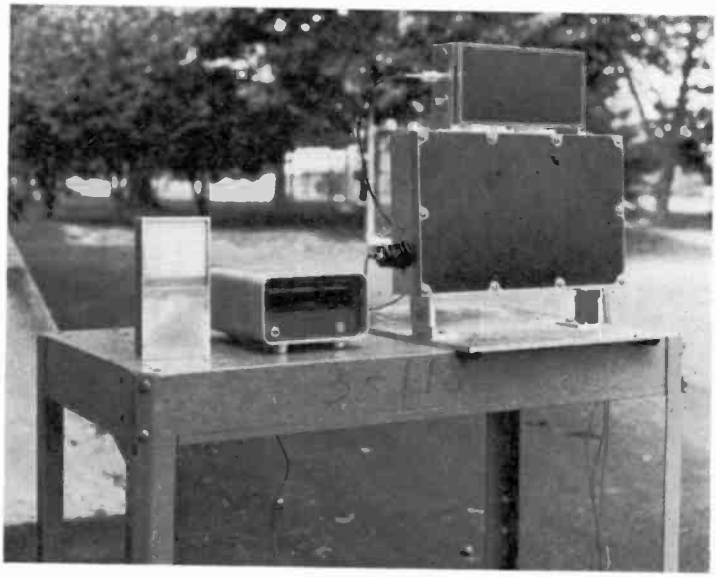


Fig. 5—System components.

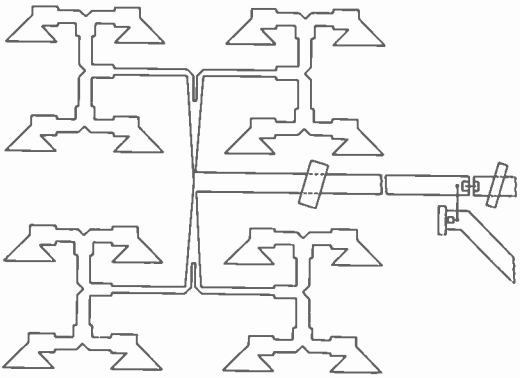
Fig. 6—Roadtest setup.

fed to the digital decoder, where the received code word is decoded and displayed on a numeric readout. In an operating system, the code word would be recorded together with the time, date, and any other pertinent data. Fig. 5 is a photograph of the entire experimental system showing the tag on the left, the digital processor with readout in the center, and the transmitter/receiver to the right. The system was tested (see Fig. 6) at drive-by speeds of up to 40 mph and functioned perfectly. Higher speeds were not possible in the limited test area available, but operation up to 100 mph should be possible.

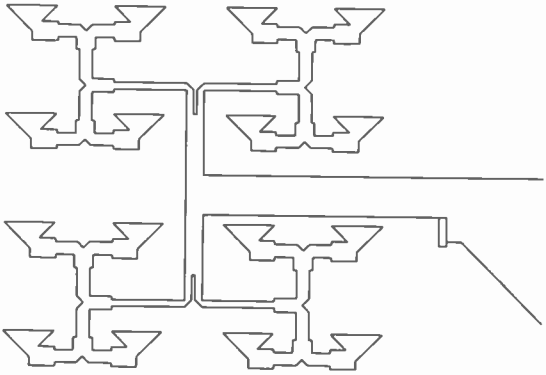
3. Identification Tag Configuration and Antenna Considerations

In the present, experimental version, the tag is fabricated on a 0.020 inch (0.05 cm) duroid double clad circuit board measuring 3×3.5 inches (7.6×8.9 cm). The antenna consists of 16 dipoles and corporate feed.[3] The dipoles are ½-wavelength at 12.4 GHz, which is the geometric mean frequency between the received microwave signal $f_1 = 8.75$ GHz and the transmitted microwave signal $2f_1 = 17.5$ GHz. The corporate feed is in the same plane as the dipole elements to eliminate the need for solder joints between the dipoles and the feed structure. The circuit patterns of the label showing the dipole elements and feed structure appear in Fig. 7. Half the pattern is etched on the top side of the circuit board and the other half is etched on the bottom side of the board (a positioned overlay of the two halves of the pattern is shown in the bottom of Fig. 7). The corporate feed structure is coupled to the doubler circuit by means of a capacitive gap etched on one half of the circuit pattern (see upper circuit pattern in Fig. 7). Impedance transformers included in the feed structure match the antenna impedance to the doubler at 8.75 GHz and 17.5 GHz. To achieve a unidirectional radiation pattern from the antenna, a back cavity is placed behind the antenna. The back cavity also serves as a housing for the label. A polystyrene sheet 0.240 inch (0.6 cm) thick by 3 inches (7.6 cm) square maintains the spacing of the antenna in the back cavity. A spacing of 0.240 inch (0.6 cm) corresponds to a quarter wavelength at the geometric mean frequency 12.4 GHz.

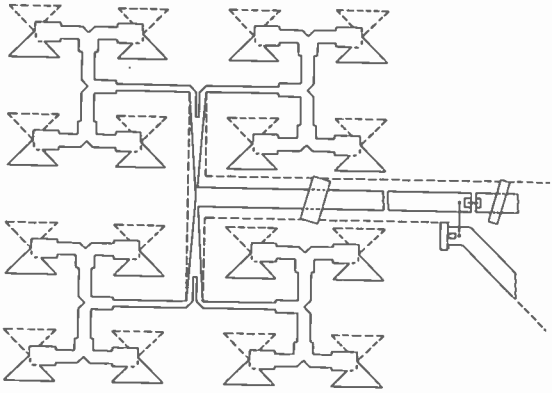
The doubler circuit consists of a nonlinear element (Schottky-barrier diode chip A25100) asymmetrically disposed between an open-circuit 50-ohm transmission line and a short-circuit 50-ohm transmission line. The lengths of the open-circuit and short-circuit lines were chosen so that the equivalent circuit of transmission line and diode is resonant at 8.75 and 17.5 GHz. The equivalent circuit is



(a) Upper circuit pattern of tag antenna



(b) Bottom circuit pattern of tag antenna



(c) Composite antenna pattern

Fig. 7—Tag antenna pattern (a) on top face of circuit board, (b) on bottom face of board, and (c) composite pattern (dotted lines are nonoverlapping portions of bottom pattern).

shown in Fig. 8, and the physical structure is shown in Fig. 7. The resonant condition was imposed to enhance the doubling efficiency at low microwave power levels.[4] To recover the 17.5 GHz signal at the antenna, a reactive termination is placed on the short circuit line where the 17.5 GHz signal is near maximum, i.e., a quarter wavelength at 17.5 GHz from the short-circuit end. The reactive termination used was an open-circuit 44-ohm stub 0.375 wavelengths from the short. Similarly, to enhance the power coupled from the antenna to the doubler at 8.75 GHz, a matching stub was used 0.220 wavelengths at 8.75 GHz from the open circuit end toward the

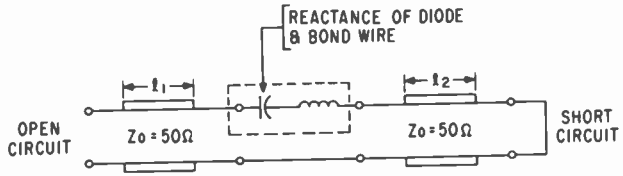


Fig. 8—Equivalent circuit of doubler.

antenna. Modulation of the 17.5 GHz signal is supplied through a low-pass filter consisting of a 1-mil (.0254 mm) diameter wire, 0.140 inch (0.35 cm) long, that acts as an rf choke and a 60 pF chip capacitor for an rf bypass. The printed-circuit pattern is designed to make access to the modulator leads convenient as shown in Fig. 7, for a discrete modulator. Access to circuit lead would be unnecessary, of course, if the modulator were integrated with the low-pass filter, as would be the case in a final design. The modulator in this initial implementation operates at clock rate of 50 kHz and is crystal controlled for ease in decoding. A final design probably would eliminate crystal control of the oscillator (because a capacitor is cheaper than a crystal) and require greater complexity at the decoder, whose cost is not as critical as that of the tag. This modulator configuration draws about 1 milliwatt of power from a six-volt mercury battery. It is expected that a final design of the modulator, using new low-threshold (1.1 volts) COS/MOS circuits, could operate at a power level below 10 μw. At such low power levels, a battery would last for years. It then also becomes feasible not to use a battery, but to extract the operating power for the modulator from the incident X-band interrogation signal. Fig. 9 is a photograph of the inside of the tag showing the printed-circuit antenna and the four-chip COS/MOS circuit, with the crystal and battery on the top right. Note that only the top pattern of the antenna is visible, because the dielectric substrate is not transparent.

4. Interrogator

4.1 Transmitter

The interrogator contains the X-band transmitter, the Ku-band receiver, the processor, and any other peripheral equipment required for a specific application. The transmitter is strictly cw; for the experiments, a 150 milliwatt TEO (transferred-electron oscillator) was used. The TEO output is coupled to the transmitting antenna through a 10-GHz coaxial low-pass filter, which essentially eliminates radiation of any harmonics.

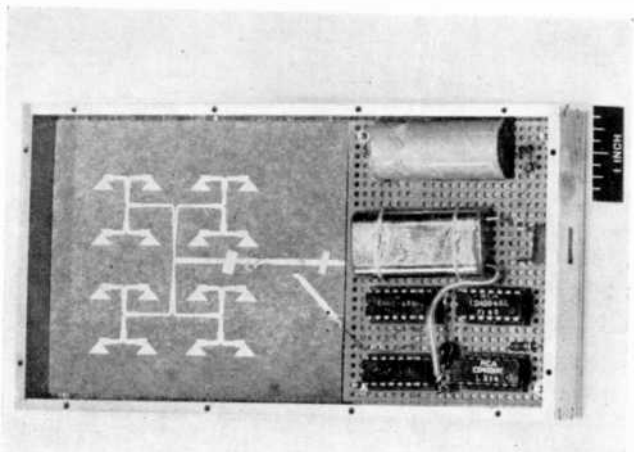


Fig. 9—Tag with cover removed.

The transmitting X-band antenna consists of 128 dipoles fed in phase. It is a printed-circuit antenna (similar to the one used in the tag) with a thickness of roughly ½ inch (1.3 cm) and requires much less space than would either a horn or a dish. Other particulars of the antenna are,

gain	— 25 dB
size	— 13 × 8 inches (33 × 20 cm)
beamwidth	— 10° × 5°
sidelobes	— 12 dB down or better

4.2 Receiver

The receiver uses the same type of antenna as the transmitter, but scaled down in size by 2 to 1, since the receiver operates at twice the

transmitter frequency. Its electrical specifications are therefore the same as those mentioned above. The output of the antenna is fed directly to a diode detector (a commercially available coaxial detector covering the range of 12-18 GHz was used). The modulation waveform from the detector, which is generated in the tag, is amplified and clipped via a chain consisting of a 40-dB pre-amplifier, a 50-dB clipper, and a 20-dB interface amplifier (all solid state). The bandwidth is 150 kHz and allows for essentially distortion-free signal transmission. As mentioned earlier, the receiver output signal level at this point is a maximum of 5 volts peak-to-peak. The signal is clamped to ground and +5 volts, thus making it ideal for driving digital logic circuits.

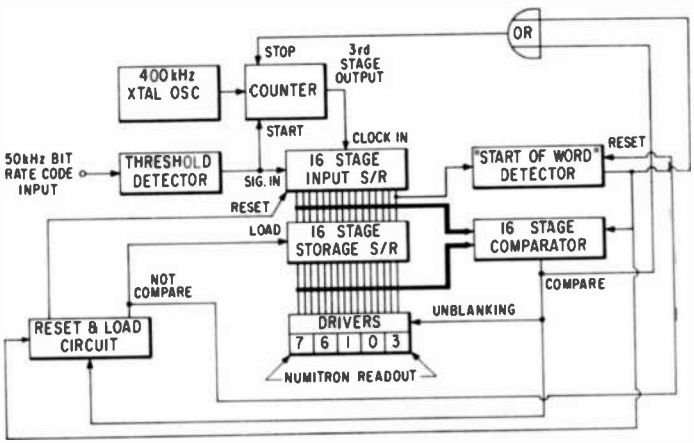


Fig. 10—Block diagram of processor.

4.3 Processor

With the exception of the input threshold circuit, the processor is entirely digital, using TTL logic chips. Fig. 10 is a block diagram of the processor. The adjustable input threshold is set so that a high signal-to-noise ratio must be reached before the signal is allowed to enter the decoded portion of the processor. In practice a 3- to 6-dB threshold signal-to-noise ratio is sufficient as measured by the absence of errors in decoding. The bandwidth of the threshold circuit is narrower than the receiver bandwidth by a factor of roughly 3 to 1 to further reduce the probability of a noise pulse "opening" the gate to the decoder. When a signal exceeds the threshold, a high gain opera-

tional amplifier changes state and causes a flip-flop to be set such that a gate is open to the incoming signal. The flip-flop will hold that condition until externally reset (by manual push button for the breadboard model, but automatically in a final system). At the first positive transition of the gate output, the counter is enabled and starts to count down from the 400-kHz crystal oscillator output. 400 kHz is 8 times the frequency of the oscillator in the tag that generates the code. After four cycles of the 400-kHz signal, the counter output goes to the low state and at that transition the output of the gate is sampled and stored in stage one of the input shift register. Eight cycles later and for every eight cycles of the 400-kHz oscillator thereafter the output of the gate is sampled and the "one" or "zero" is stored in stage one of the input register. Of course, the previously stored data is shifted down until the original "one" (that started the process) reaches the end of the input register.

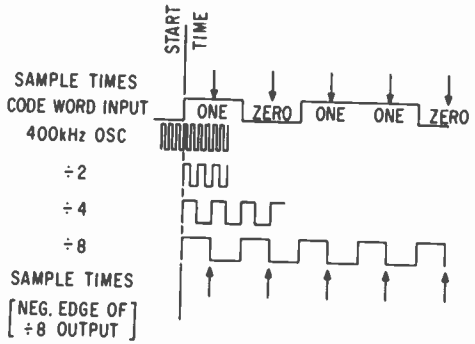


Fig. 11—Timing diagram of processor.

It should be pointed out that use of a 400-kHz oscillator and a divider allows sampling of the incoming bits essentially in the middle of their allocated time period. The timing diagram of Fig. 11 shows this more clearly. By sampling in this way, absolute frequency lock between tag and processor is not required, i.e., the relative drift can be as much as $\pm\frac{1}{2}$ bit per word. For a 16-bit word this amount of drift imposes about a 3% accuracy requirement (somewhat too stringent for simple RC oscillators, but easy to obtain with crystal controlled oscillators).

When the original "one" reaches the last stage of the input register, its presence there is detected, causing a number of events to occur: (1) the clock pulses for the register are stopped and (2)

the contents of the input register are compared, bit-for-bit, to the word stored in the lower storage register. If the word in the input register matches that in the second storage register, then that word is converted to decimal and displayed on the read-out. The system will stay in this "hold" condition until reset (the same manual reset as mentioned earlier). In an operating system the reset would come from the tape that records the code acknowledging that the code is properly recorded and the tape is ready for the next customer.

If, however, the code word in the input register does not match the word stored in the second register the following actions take place: (1) the word in the second storage register is replaced by the word in the input register (2) the input register is cleared, (3) the divider following the 400-kHz clock is reset and un-inhibited and awaits an input signal to enable it, (4) the read-out remains blanked, and (5) the comparator is disabled. It is clear, therefore, that in order to get a readout, the input signal must be above a threshold and that two consecutive identical code words must be received. The system is essentially error free, in the sense of corrupting a code when the threshold is set for a 3-6 dB signal-to-noise ratio. Under this condition the maximum range between interrogator and tag is about 10 feet (3 meters) for 150 milliwatts of radiated power, 25-dB-gain transmitting and receiving antennas, and direct detection. If the receiver used a superheterodyne configuration, i.e., a homodyne, a 30- to 40-dB improvement in sensitivity would occur over direct detection. This would allow the use of smaller, lower-gain, wider-beamwidth transmitting and receiving antennas for the same maximum range. Ten feet is probably a good maximum range for most applications.

5. Possible Improvements and Applications

The tag could be made entirely on one subtrate, including the antenna, doubler, and modulator. Its size would reduce to about $3 \times 3 \times \frac{1}{4}$ inches ($7.6 \times 7.6 \times 0.63$ cm) and it could possible be made to operate totally passively, utilizing the interrogator signal for the few microwatts required for the modulator circuits. The code length could be increased to 30 or 40 bits to allow increased user capacity and a more sophisticated code preamble to be built into the code word. This approach would permit non-crystal-controlled operation and allow the receiver–decoder to decode the bit rate as well as the identity of the tag.

Improvements in the interrogator could include the already mentioned homodyne detection coupled with antenna-size reduction. The

processor would be made somewhat more complex, so that it could run in the loosely synchronized fashion described above. Output signals from the processor would have to be made compatible with various peripheral equipments, such as tape stations, minicomputers, readouts, or printers.

Such an identification system could, of course, be used for purposes other than automatic toll collections. Restricted parking yards that require a validated code from a vehicle before the entrance gate opens is one such application. Since the final design could yield very small and lightweight tags, they could be worn as name tags that would allow the wearer entrance to restricted areas or they could be affixed to crates or luggage to create an inventory control system. Such a system could also be used to open car doors or to activate car ignition systems. A peripheral benefit of this application is that car theft would be made more difficult, since no keyway would exist on the door or the ignition. Other applications would probably come in time.

6. Conclusions

An experimental microwave identification system has been developed that is immune to dirt, weather, and clutter. Clutter-free operation results from the fact that unwanted returns at the transmitted frequency are not "seen" by the receiver, which is tuned to twice the transmitted frequency. The receiver is, therefore, also immune to interference from other transmitters within the operating system. A range of ten feet (3 meters) was attained using 150-mW radiated power, 25-dB receiving and transmitting antennas, and direct detection. Bench tests revealed that the same range was obtainable using two 15-dB antennas and homodyne detection. The sizes of the 15 dB antennas were $4\frac{1}{2} \times 4\frac{1}{2} \times \frac{1}{2}$ inches ($11.1 \times 11.4 \times 1.3$ cm) for X band and $2\frac{1}{4} \times 2\frac{1}{4} \times \frac{1}{2}$ inches ($5.7 \times 5.7 \times 1.3$ cm) for Ku band. Such small size would permit a portable interrogator suitable for use, for example, by police in tracking down lost or stolen vehicles. Complete integration of the tag would produce a package roughly $3 \times 3 \times \frac{1}{2}$ inches ($7.6 \times 7.6 \times 1.3$ cm) and it is estimated, would cost less than $10 when mass produced.

Acknowledgments

J. Avins gave generously in the area of digital design philosophy for the processor, T. Nolan built the entire system, H. Johnson provided

the TEO (150 mW output at X band), the X-band antenna was provided by the antenna skill center of RCA's Missile and Surface Radar Division, and L. Zappulla helped test and tune the antenna doubler used in the tag.

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Lumped-Element High-Power Trapatt Circuits*

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Abstract—A UHF lumped-element circuit was designed, built, and successfully operated. Circuit volume is only 1.7 in^3 and performance, in general, is equal to or superior to that of distributed circuits. Peak power levels of 300-400 watts with efficiencies of near 40% were consistently generated. The circuit is tunable over a frequency range of at least 20%. Virtues of the lumped-element oscillator, in addition to small size and high performance, include fairly rapid optimization and wide adaptability to diodes of differing characteristics. Preliminary experiments indicate that, with the use of flat coils, a circuit size reduction of yet another order of magnitude can be achieved, and that lumped-element Trapatt circuit techniques can be extended into at least the L-band range.

1. Introduction

High-performance Trapatt circuits have heretofore been of the distributed type, with a major dimension being a large fraction of a wavelength. Most distributed circuits are similar to one discussed by

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Evans,[1] who described its operation in terms of a wave repeatedly reflected between the diode and a filter element nearly one-half wavelength away. This type of Trapatt circuit is popular because the diode–circuit interaction is relatively easy to describe and also because it has in many cases yielded good performance. However, it suffers from a number of disadvantages including circuit size—which may be unacceptably large at UHF and lower L-band frequencies—and inherently narrow bandwidth characteristics. Finally, while it is true that distributed circuits lend themselves nicely to a time-domain description of the basic interactions, it does not follow that such circuits should be required for proper Trapatt performance. Thus it seemed appropriate to consider the possibility of a circuit in which no significant electrical length separates one circuit element from another and from the diode, i.e., a lumped-element circuit.

A program was undertaken to develop lumped-element pulsed oscillators at UHF and L-band frequencies. The effort was successful in that (a) the principle of lumped-element high-efficiency Trapatt operation was demonstrated, (b) significant size reductions were achieved, (c) performance in general was equal or superior to that of distributed circuits, and (d) a number of practical tuning features resulted. Though lumped-element amplification was also demonstrated, bandwidth investigations were not carried out in the present study.

We will first discuss the general design considerations involved in Trapatt oscillator circuits and diodes. Specific designs for a UHF lumped-element circuit and the associated silicon diodes are given in Section 3. "Box" and planar versions of the lumped circuit are described. Practical means for fabricating the required diodes are also discussed. Finally, in Section 4, we present experimental results for the box and planar UHF oscillators and an L-band planar circuit that has been used both as an oscillator and an amplifier.

2. General Design Considerations

It was discovered[2] that under certain very restrictive circuit and diode conditions, large amounts of UHF or microwave power could be generated at unusually high efficiencies. The mode in question was first labeled "anomalous" and later "Trapatt".[3] Experimental research helped shed light on various diode and circuit designs that were consistent with the attainment of high efficiencies. An analytic theory[4] for this mode and guidelines[5] that developed from the theory helped further define conditions for development of such oscillations at a specified frequency. Below we review these guidelines and relate them specifically to the design of the UHF oscillator in question.

2.1 Diode Considerations

Our first guideline relates the width of the n-region (assuming a conventional silicon pnn+ structure) to the center frequency of the band over which operation is desired.

$$W(\mu\text{m}) \approx \frac{7}{f\,(\text{GHz})}. \qquad [1]$$

In our UHF program the design frequency was $f = 0.5$ for which $W \approx 14$ μm. Such a depletion width for a heavily punched-through diode would lead to a breakdown voltage far exceeding 200 V. Not only are such diodes (which must also draw large currents) difficult to fabricate, but they would require power-supply voltages that for many applications are considered undesirably high. Hence, a compromise was called for. Fortunately, the relationship given in Eq. [1] is not highly critical, since Trapatt diodes should be capable of operation over a reasonably broad frequency band. Most of our diodes (described in more detail later) exhibit breakdown voltages in the range 185 to 200 V and work very well at 500 MHz. The corresponding depletion width is in the order of 8 μm.

The next choice that concerns the Trapatt designer is the doping density of the n-region. The appropriate information is contained in the design triangle that is discussed in Ref. [5]. The design triangle defines a (doping density) $\times$ (depletion width) product, which should be in the range 4×10^{11} to 10^{12} cm^{-2}. Intratriangle operation is desired since such has been shown both theoretically and experimentally to be consistent with near-optimum-efficiency operation. For our diodes, 6 ohm-cm ($n = 8 \times 10^{14}$ cm^{-3}) epilayers were grown for which $n_d w = 6.4 \times 10^{11}$ cm^{-2}, consistent with the above-stated restriction.

The design triangle also gives a preferred range for dc current density normalized to the critical value,

$$J_c = q v_s n_d. \qquad [2]$$

In Eq. [2] $q = 1.6 \times 10^{-19}$ coulomb and $v_s = 10^7$ cm/sec, the electron saturation velocity in silicon. For intratriangle operation (and for the $n_d w$ product of our diodes) we require $0.75 < j_{dc} < 1.5$, which corresponds to 10^3 A/cm^2 $< J_{dc} < 2 \times 10^3$ A/cm^2. Best operation was indeed found to lie in this range.

Our next choice concerns the diode area (diameter). The trade-

offs involved in choosing sample diameters are clear. The larger the diameter, the greater the potential power; however, uniform, relatively defect-free large-area diodes are difficult to fabricate and lead to required circuit impedances that are quite low.

The choice of sample diameter stemmed from the following reasoning. A diode with a breakdown voltage of 190 V would be expected[4] to operate at a dc voltage of roughly $0.64 \times 190 = 122$ V. Our goal was an output power of at least 200 W. It was considered prudent to design for 300 W, thereby leaving margin for error.

For our efficiency goal of 30%, the required dc input power would be $300/0.3 = 1000$ W. Thus, the required current would be

$$I_{dc} = P_{dc}/V_{dc} = 1000/122 = 8.2 \text{ A}. \qquad [3]$$

For a current density of 1.5×10^3 A/cm^2, which is in the middle of the range specified by the design triangle, an area of $A = I_{dc}/J_{dc} = 8.2/1.5 \times 10^3 = 5.5 \times 10^{-3}$ cm^2 is required. This corresponds to a diameter of 33 mils, which was the diameter chosen for our diodes (35-mil masks were employed, which, after etching, resulted in junction diameters of 33 mils).

2.2 Circuit Considerations

The guidelines also estimate the required fundamental-frequency-circuit impedance to be[5]

$$R_1 \sim \frac{0.8\,\eta V_b}{q v_s j_{dc} n_d A} = \frac{0.8\,\eta V_b}{I_{dc}}, \qquad [4]$$

where η is the per-unit efficiency. For $\eta = 0.3$, $Z_1 = 5.6$ ohms. Thus, the circuit must be capable of transforming the load impedance of 50 ohms to a value about an order of magnitude smaller. The circuit must also permit an adjustment of the imaginary part of the fundamental impedance seen by the diode. Thirdly, most harmonic energy must be trapped, i.e., only fundamental power is to be significantly coupled to a load. To ensure low harmonic power loss it will be sufficient (though perhaps not necessary) that the real parts of the lower harmonic impedances be small. This still leaves us with the choice of the harmonic reactances, which must not be left arbitrary.

The Trapatt diode, certainly more than most devices, depends on the values of the harmonic impedances for proper performance. Of course one can only provide for adjustment of a limited number of

harmonics. A larger number would require more controls, and each additional control greatly increases the time required for adjusting the circuit optimally to a given diode. However, in principle, the optimum performance improves with each additional control. Thus a compromse is required. It has generally been found by experience that for excellent performance at a specified frequency for a given diode, four adjustments can be sufficient (three if the frequency is not specified), and optimization time need not be excessive. The above is true, of course, only if the circuit is properly designed.

Conceptionally, at least, it is desirable to have independent adjustment of each impedance parameter (though practical considerations generally make total separation of functions impossible). Thus, independent adjustment was a consideration in our design.

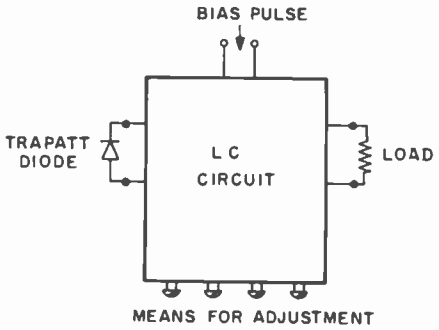


Fig. 1—Block diagram for design of lumped-element Trapatt circuit.

3. Reduction to Practice of Circuits and Diodes

3.1 Lumped-Element Circuit Design

Our objective was to provide an appropriate lumped-element circuit between the Trapatt diode and the 50-ohm load, with no more than four adjustments, and with means for biasing the diode. The situation is summarized schematically in Fig. 1. The circuit consists of capacitances and inductances, since resistive elements would absorb power, while their usefulness in wave-shaping for Trapatt diodes has not been demonstrated. The circuit must serve the following functions:

(a) Transform the real part of the load impedance (generally 50 ohms) to a level of about 5 to 6 ohms.

(b) Provide the proper reactance at the fundamental frequency. (According to the guidelines,[5] this reactance is small, though not quite

zero, and must make allowance for the package reactance).

(c) Trap all relevant harmonics (at least through the fifth, and preferably beyond).

(d) Provide a set of reactances at the lower harmonic frequencies consistent with stable high-efficiency Trapatt generation. In principle, there are many such sets, and finding one is usually an empirical process.

Since we are to permit four controls in the circuit, these may be loosely considered to optimize the real and imaginary parts of the fundamental impedance, R_1 and X_1, and the imaginary parts of the second- and third-harmonic impedances, X_2 and X_3, hopefully with a significant degree of independence among these four variables.

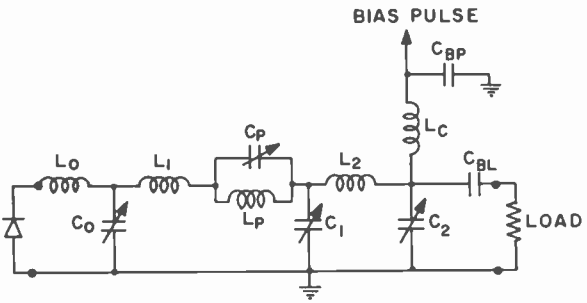


Fig. 2—Schematic of lumped-element Trapatt circuit.

A schematic of the circuit we designed to achieve the above objectives is shown in Fig. 2. Let us now turn our attention to the functions of the various elements. Typical approximate values for each element are indicated in parentheses. C_{BL} (100 pF) is a blocking capacitor required to keep bias-pulse power from being wasted in the load. L_c (100 nH) and C_{BP} (100 pF) form a low-pass filter that prevents rf power from leaking into the pulse circuit.

While the other elements are seen to comprise sections of shunt *m*-derived and constant-*k* low-pass filters, the values of the individual elements were not derived from standard filter theory. Rather, some of them are seen to be consistent with certain specific objectives relevant to Trapatt oscillator design. L_o (3 nH), which includes package reactance, is sufficiently large to ensure that the diode sees essentially an open circuit at harmonics higher than the third. Thus, 3 nH at 2000 MHz (the fourth harmonic) represents a reactance of 38 ohms,

considerably higher than the basic 5-ohm diode impedance level. Hence, any adjustment in the capacitances (unless they happen to result in accidental series resonance with L_o at a specific harmonic frequency) will not alter the near open-circuit impedance condition for the higher harmonics. L_1 is not essential to the design but is a necessary geometric inductance in connecting the elements. Other non-negligible inductances (not shown) are the series inductances associated with the variable capacitors.

The variable microwave capacitors have maximum values of 10 pF for C_1 and C_2 and 6 pF for C_o and C_p. C_2 (5 pF) has the sole function of adjusting the real part, R_1 of the fundamental impedance seen by the diode. It has little effect on the imaginary part, X_1, primarily because L_2 (30 nH) is sufficiently large to mask small changes in reactance. Changing C_2 has virtually no effect on the harmonics, since these are stopped before they reach this element. C_1 (8 pF) has a major effect on X_1 and also some effect on R_1. It too has little influence (at least for small changes) on the harmonic impedances. The major role played by C_p (6 pF) is to determine the all-important second-harmonic reactance, X_2. It order to be very effective in controlling X_2, it resonates with L_p (5 nH) in the vicinity of the second harmonic. Changing C_p also has some effect at the third harmonic but has little effect on the fundamental since its impedance is largely short-circuited by L_p at that frequency. C_o (3 pF) has no effect on the fundamental, since its impedance there ($-j$ 100 ohms) is largely short-circuited by the transformed circuit impedance at that point (5 ohms). This capacitor has a small effect on the second harmonic and a large effect on the third harmonic.

Thus, the circuit of Fig. 2 is seen to have the potential of trapping all the harmonics, while optimally adjusting the four most important parameters, R_1, X_1, X_2, and X_3 with a significant degree of independence of the various functions. The circuit also offers tunability over a reasonably broad frequency range. For a fixed value of C_p, which results in a simpler circuit, this degree of flexibility is lost.

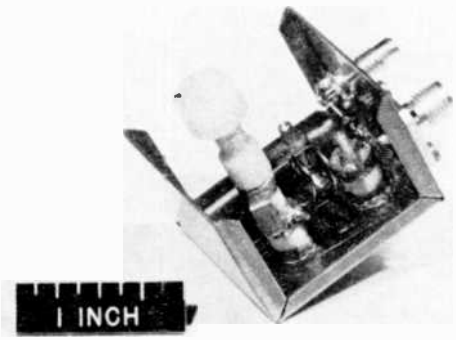
3.2 Box Circuit

Photographs of the developed lumped-element circuit appear in Figs. 3a and 3b, the former showing the circuit with the cover removed. All straps and coils are of copper, as is the box. Fig. 3b shows the external adjustments for C_o, C_1, and C_2. Since C_p is not grounded, special provision is made for its control. A nylon knob (seen in Fig. 3a) inserted through a hole in the cover is used to adjust C_p. The

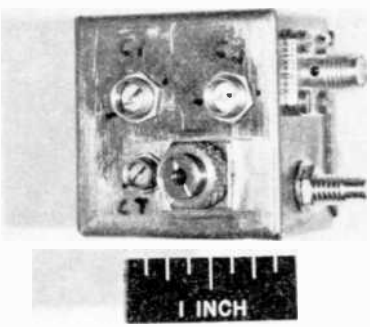
circuit volume is 1.7 in^3 and its weight is 2 oz. A full discussion of results obtained with this circuit is given in Section 4.

3.3 Planar Circuits

After completon of work on the "box" circuit, attention was turned to the task of further reducing the circuit volume with integrated-circuit techniques. Thus, a new circuit was developed in which coils were obtained by etched patterns on a Duroid board. The resultant size (0.2 in^3 exclusive of connectors) was an order of magnitude smaller than that of the box circuit. (No cover was used for the planar circuit; if radiation considerations mandate the use of a cover, circuit volume would probably increase to ≈0.4 in^3. Advantages of the planar circuit, in addition to much smaller size, include superior ruggedness, lower batch-fabrication costs, and a higher degree of reproducibility.



(a)



(b)

Fig. 3—Lumped-element circuit with and without cover removed.

A photograph of the UHF planar circuit is shown in Fig. 4. Though the presence of the ground plane only 0.125 inch from the upper plane requires some modification of the equivalent circuit of Fig. 2, operation of the planar circuit appears qualitatively similar to that of the box circuit.

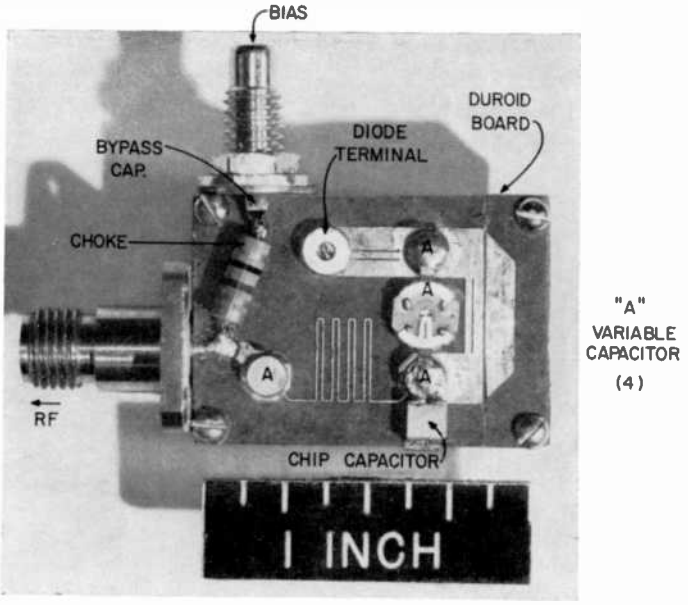


Fig. 4—UHF planar circuit. The letter A designates variable capacitors (four).

An L-band circuit with smaller coils and capacitors and a miniature etched choke was also fabricated and operated in the lower L-band range. In both planar circuits, all adjustments are made from the ground-plane side; thus, no problems involving detuning effects from the proximity of the adjustment tool are encountered.

3.4 Fabrication of UHF Diodes

Our approach to diode fabrication was based on theoretical guidelines (discussed in Section 2) and practical experience, which had been successfully combined in the past to develop Trapatt diodes, most recently at S-band.[6] Although this combination gave us a good start, it was not until we were able to overcome significant material and processing problems especially related to our high-current high-voltage requirements that we were able to reach our goals.

While p+nn+ diodes with reasonably abrupt junctions occasionally have worked quite well in the Trapatt mode, it has been our experience that consistently good current-carrying capabilities and rf performance are more readily obtainable with long diffusions, which, of course, result in highly graded junctions. Also, not surprisingly,

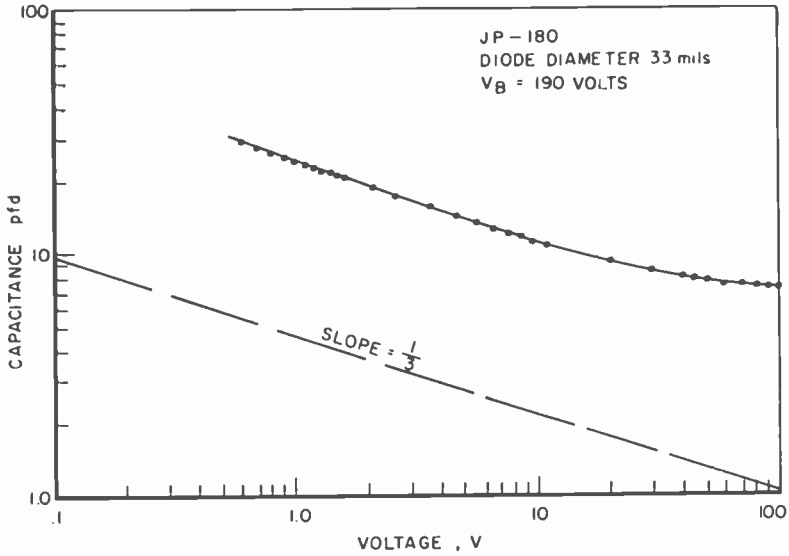


Fig. 5—*C-V* characteristics of 33-mil diode from 180 family.

there was evidence that maintaining low dislocation densities is particularly important for diodes that were to be of large area and high voltage. Thus, after encountering a number of problems, our objectives for the epitaxial silicon wafers were modified to include (a) especially high-quality substrates and epilayers and (b) large epilayer thickness (viz., 30 to 35 μm), which could accommodate long single diffusions and still result in diode breakdown voltages near 200 V. Such wafers were produced with standard equipment and modified processing utilizing dichlorosilane gas epitaxy.

The increased thickness of these layers allowed us to employ diffusion times of approximately 40 to 50 hours at 1150°C. In this manner graded junctions were produced of sufficient depletion-region widths and breakdown voltages. *C-V* characteristics typical of 33-mil diodes made from one such wafer are shown in Fig. 5. Note the ⅓ slope of the *C-V* plot that gradually changes into the punch-through range between 10 and 30 V.

The diodes were fabricated with a truncated mesa structure 33 mils in diameter, metallized on top and bottom with about 500 Å of chrome and 10,000 Å of gold, and thermal-compression bonded in a gold-plated threaded "pillbox" package consisting of a gold-plated copper pedestal and alumina insulation. The junction side of the silicon chip was mounted on the pedestal for superior heat-sinking. One-mil-wire leads were ultrasonically bonded to the top contact of the mesa such that a total of six leads connected the diode chip to the flange of the package. In this manner, a low-package inductance was assured. Care was taken to have at least two bonding points per wire on the top surface of the wafer. A gold-plated Kovar lid was welded to the flange of the package, thus completing the diode assembly. A number of chips were also mounted in larger varactor packages. There was no obvious difference in the performance of diodes that could be related to package type.

The above diodes easily met our original repetition rate objective of 10,000 Hz at a pulse width of 0.2 μsec. Modifications were required in order to operate at a repetition rate of 50,000 Hz. These included the bonding of a 0.020-inch copper sheet to the wafer. Thus, each 0.033-inch-diameter chip contained a 0.060-inch square of copper to help remove the heat. These diodes were subsequently hard-soldered into varactor packages or onto copper screws for use in the box circuit and the planar circuit, respectively, where they consistently operated well at the elevated repetition rate of 50,000 Hz.

4. Experimental Results

4.1 Box Circuit

The oscillator design frequency was 500 MHz. Performance of the oscillator was, in fact, optimum at about that frequency; however, the circuit was tunable so that near optimum results were obtained over the range 450-550 MHz. The highest power achieved was 470 watts at an efficiency of 44%. This result was obtained at a duty cycle of 1%, yielding an average rf power of 4.7 watts. No higher duty cycles were attempted. The above peak power, however, was accompanied by excessive AM noise. "High quality" outputs (i.e., those without such noise) were generally limited to about 200 to 300 watts at efficiencies of 20-30%.

The crystal detector output and spectrum typical of a high-quality output are shown in Figs. 6 and 7. The deep well-defined nulls that characterize the spectral display and are correlated with a noise-free crystal display are obtained only with careful adjustment. The asymmetry observable in the spectral display results from the long rise-time

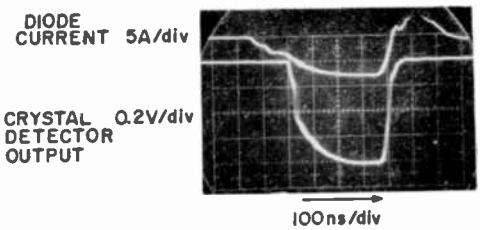


Fig. 6—Operational waveforms showing little jitter and no mode breakup.

of the pulsing circuit employed. The changing diode current causes a slight frequency change as well as an amplitude change across the length of the pulse.

The circuit was quite adaptable, accommodating diodes from the five different wafers tested. Tuning was generally convenient and relatively rapid. Interchanging similar diodes from a given wafer could usually be accomplished with either no tuning or adjustment of only one capacitor.

An oscillator was tested at a power level of 200 watts at an ambient temperature of from −12° to +200°F. The power change was small, the frequency shift was only 1 MHz, and spectral quality was maintained except for some impairment near the high-temperature extreme.

Using a network analyzer and a probe designed to measure the impedance seen by the chip within the package, data was obtained on the circuit for settings that gave good performance. A sample set of measurements for a 492-MHz oscillator is recorded in Table 1. The

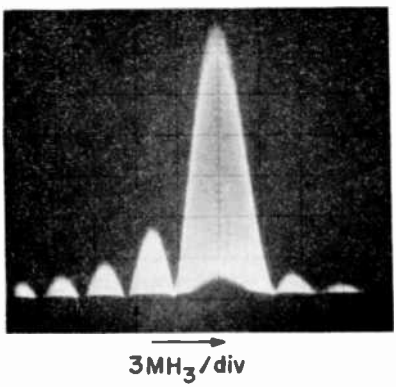


Fig. 7—Frequency spectrum for diode 181-27 in lumped-element circuit.

Table 1—Sample Circuit-Impedance Measurements

Harmonic Number	1	2	3	4	5	6	7
Impedance (ohms)	$6 + j1.5$	$1 - j1$	$2.5 - j5.5$	$0 + j70$	$0 + j275$	$50 + j160$	$5 - j160$

real part of the fundamental impedance, in all cases measured, was in the range 4-6 ohms, in accordance with the guidelines estimate. The imaginary part was inductive and, as expected, of small magnitude. The second harmonic was, in all cases, found to be nearly short circuited. This result contrasts sharply from these reported in the lierature[7] where the second-harmonic reactance is reported to be of significant magnitude, often comparable to or larger than the fundamental impedance level. There is no contradiction, however, since a variety of impedance sets, each associated with different diode waveforms, are consistent with high-efficiency generation. The third-harmonic impedance contains a non-negligible real part, indicating the possibility of a small loss at that frequency. In accordance with our design, the fourth- through the seventh-harmonic impedances are found to be essentially infinite, when compared to the fundamental impedance.

One of the four capacitances was changed by one turn and the impedances remeasured. The procedure was repeated for each capacitor. Table 2 summarizes the approximate results. The principle impedance change induced by a given adjustment (e.g., the change in X_3 induced by C_o in Fig. 2) is denoted as unity, and the change in other impedance parameters for the same adjustment is given as a fraction of the principle change. We note that, in accordance with our design aims, C_2 and C_1 control the real and imaginary parts, respectively, of the fundamental impedance with little effect on other parameters. C_p controls principally the second harmonic with a lesser effect on the third harmonic, while the effect of C_o is virtually restricted to the third harmonic. Thus, a significant degree of independent impedance-parameter adjustment was achieved.

Table 2—Relative Effect of Small Capacitor Adjustments on Impedance. (Figures Given Represent a Fraction of the Principal Change for a Given Adjustment in Circuit.)

Harmonic No.	Capacitor (see Fig. 2) C_2	C_1	C_p	C_o
1 (Real Part)	1.0	0.2	0	0
1 (Imag. Part)	0.2	1.0	0	0
2 (Imag. Part)	0	0.1	1.0	0.1
3 (Imag. Part)	0	0	0.6	1.0

4.2 Planar Circuit

The UHF circuit shown in Fig. 4 was built and tested as was a similar circuit designed for lower L-band. High-quality power outputs up to 300 watts were obtained in both cases. The UHF circuit oscillated over the range 520-600 MHz—somewhat higher than the design goal of 500 MHz—while the L-band circuit was operated at various frequencies from 1030 MHz to over 1250 MHz, including the design frequency of 1090 MHz.

The L-band oscillator was tested for single-knob tunability, a feature that is generally difficult to attain because of the critical importance of a number of harmonics. Changing only C_1 (Fig. 2), which we had previously noted to control the fundamental frequency reactance, moved the output frequency 46 MHz (4%), while the power dropped only 1.1 dB from its peak level of 215 watts, and high quality was maintained.

Finally, the L-band circuit was operated as an amplifier with a pulsed output power of 250 watts at 7 dB gain. The circuit was operated both in the dc-bias mode[8,9] and with conventional pulse biasing. In the former case, the amplifier is activated by the rf input pulse, with no accompanying bias pulse required.

5. Summary

Distributed-circuit interactions generally used to obtain and describe Trapatt oscillations are not necessary for high performance. Lumped-element circuits have been designed, built, and demonstrated at UHF (450-600 MHz) and L-band (1030-1250 MHz) frequencies. A small (1.7 in^3) UHF box circuit weighing 2 oz has yielded up to 470 watts of peak power at an efficiency of 44%. If high spectral purity is desired, power and efficiency must be compromised. Notable characteristics of the lumped-element circuit, in addition to high performance and small size, include tunability, adaptability to diodes of differing characteristics, and a high degree of independence in the adjustment of significant impedance parameters.

Planar versions of the lumped-element circuit were also developed and operated. Both UHF and L-band planar circuits, which use microwave-integrated-circuit techniques to obtain flat coils on a Duroid board, yielded 300 watts of power with relatively high spectral purity. An L-band amplifier with 7 dB gain produced 250 watts of output power, believed to be the highest ever reported for a single-device microwave solid-state amplifier of any kind. Advantages of the planar circuit over the box circuit include even smaller size (0.2 in^3), superior

ruggedness, lower batch-fabrication costs, and a higher degree of reproducibility.

A number of diode- and circuit-design parameters were calculated from theoretical guidelines previously developed. Diodes which gave the best results used very high-quality silicon substrates and deep diffusions into 6-ohm-cm epilayers. These large-area (5.5×10^{-3} cm^2) devices exhibit high breakdown voltages and high-current capacity, both necessary for high powers at the desired frequencies.

Acknowledgments

Many colleagues whose assistance in this program was indispensable are gratefully acknowledged—N. Goldsmith and P. Robinson for growing the epitaxial wafers, J. Reynolds and V. Lawson for heat sinking the diodes, J. Risko for several diffusions, S. Weisbrod who pretested diodes in distributed circuits, and K. K. N. Chang, T. Christy (Naval ordinance Laboratory), A. Rosen, and H. Sobol for their interest and encouragement. Also, some early unreported results (30 watts at 15% efficiency) by R. Chaffin of Sandia Laboratories using lumped capacitors helped motivate the approach described here.

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Microwave Frequency Dividers

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Abstract—This paper describes dynamic frequency-division circuits at microwave frequencies employing transferred-electron devices (TED's). Dynamic division by integers up to 6 and at frequencies as high as 16 GHz has been demonstrated. The linearity of the TED dividers is shown to be excellent. Input bandwidths as high as 10% were obtained in X-band. The phase stability of the dividers was found to be very good. With two-terminal TED's, it was demonstrated that a typical conversion loss of 3 dB could be obtained. With high-efficiency integral-heat-sink TED's, conversion loss as low as 0 dB was demonstrated. It has been established that these dividers operate with both pulsed and cw inputs and also with fm inputs within the dynamic bandwidth.

Preliminary results on dividers using planar Schottky-barrier-gate TED's are also reported. The use of planar 3-terminal devices provides input–output isolation and has potential for division with gain.

Introduction

In 1963 Gunn discovered that when a dc voltage is applied to a bar of *n*-type GaAs or InP, the current ocsillates when the average applied electric field increases beyond a threshold value of several kilovolts/cm.[1] With further experiments, Gunn showed that these current oscillations were associated with the transit of a high-field

space-charge domain from cathode to anode.[2] Further research revealed that these oscillations were a manifestation of the transferred-electron effect predicted independently by Ridley and Watkins[3] and by Hilsum[4] in the early 1960's. Since 1963, an intensive research effort has been carried out, and the physics of the transferred-electron effect is well understood. Transferred-electron devices (TED's) have been established as useful microwave oscillators and amplifiers and have found application in several military and commercial systems.

The potential of the transferred-electron effect for ultra-high-speed logic applications was recognized as early as 1967.[5-7] Threshold-logic circuits using TED's have been developed to demonstrate basic logic functions such as AND, OR, DELAY, and MEMORY. We reported earlier[8] another important application of TED logic, viz, dynamic frequency dividers at microwave frequencies. This paper describes further findings on the linearity and phase stability of a TED dividing circuit. The linearity and phase stability of TED dividing circuits have been measured and found to be excellent. Bandwidths of up to 10% have been achieved at X-band. Several possible applications of the TED divider are described.

Physical Principles of TED Logic

We will first briefly review the basic principles of TED logic. More complete descriptions are available in the literature.[9,10] When a TED is biased above the threshold field (E_{TH}), a negative differential mobility occurs due to the field-dependent transfer of conduction-band electrons from a low-energy–high-mobility valley to high-energy–low-mobility satellite valleys. Under this condition, an excess space charge introduced at the cathode travels towards the anode and grows exponentially as a result of the negative differential mobility. The growth rate is given by

$$\exp\left[\frac{t}{|\tau_r|}\right] = \exp\left[\frac{nel|\mu|}{\bar{v}\epsilon}\right]$$

where l is the length of the negative differential mobility region, $\bar{v}$ the average electron velocity, n the carrier concentration, ϵ the dielectric constant, and $|\bar{\mu}|$ the differential mobility. When this growth rate is sufficiently large, ($nl > 10^{12}$ cm^{-2} for GaAs), a mature high-field domain forms and the field outside the domain falls below the threshold field. The time constant involved in the transfer of electrons between conduction subbands is of the order of 3-5 psec and, conse-

quently, differential negative mobility is available well into the millimeter-wave range. It has been established that there exists a domain-sustaining field $E_s \leqslant E_{TH}$, such that once a mature domain is launched at the cathode, the applied field E_a can be reduced to $E_s < E_a < E_{TH}$ without causing domain collapse. $E_s < E_{TH}$ if the device length is greater than a critical length $l_a = 3.2 \times 10^4\, n^{-1/2}$ cm. For $n = 2 \times 10^{15}$ cm^{-3}, this critical length is of the order of 7 μm.

Consider a TED with $nl > 10^{12}$ cm^{-2} and $l > l_a$ biased to field E_a such that $E_s < E_a < E_{TH}$. Assume that a trigger pulse is superimposed such that the field at the cathode exceeds E_{TH}. This trigger pulse may be applied to the anode of a two-terminal TED or at the gate electrode of a three-terminal TED. If the trigger pulse width is greater than the domain formation time, a domain will be nucleated at the cathode and the device current will drop below the threshold value. The current stays at this level until the domain is collected at the anode at which time the current rises to the original value. After domain transit, the current remains constant until a new trigger pulse appears. The device thus acts as a monostable multivibrator.

The property of the TED that allows its use in dynamic division circuits is the existence of a refractory period after domain nucleation. As discussed earlier, when a mature domain forms, the field outside the domain falls to a very low value. Another trigger pulse appearing while a domain is in transit cannot raise the cathode field to the threshold value and, thus, has no effect on the device. If the second trigger pulse arrives after the first domain is collected at anode, a second domain is generated. If an input trigger signal is applied at twice the signal frequency, every other peak will nucleate a domain, and dynamic division by 2 is achieved. Division by 3, 4, . . . K, where K is an integer, can thus be similarly explained. In a TED frequency divider, the output frequency is the transit-time frequency and the input an integral multiple thereof.

It has been established that a three-terminal TED with a control-electrode or 'gate' close to the cathode is very useful for logic applications.[7] The most suitable gate contact is a Schottky barrier.[7] Domains can be triggered by applying a reverse bias to the gate. The advantages of a three-terminal TED are, (1) built in input/output isolation, (2) Schottky barrier gate has high input impedance, and (3) gain for fan-out is available.

A summary of the advantages of TEDs for ultra-high speed logic applications is[10]

(1) The TED is a threshold device and all threshold logic circuits can be implemented. Switching times of several picoseconds and delay-

dissipation products of a fraction of a picojoule are feasible.

(2) The shape and amplitude of the output are independent of the input. The TED regenerates amplitude and timing.

(3) The TED has a refractory period; when a domain is in transit from cathode (or gate) to anode, another domain cannot be triggered.

(4) The three-terminal, Schottky-gate TED has gain, and fan-outs of 10:1 appear feasible. This TED is also a unidirectional device.

(5) A mature domain moving through a uniformly doped TED with a nonuniform cross section will produce a current waveform proportional to the cross-sectional area. This property can be utilized in analog–digital converters, delay lines, etc.

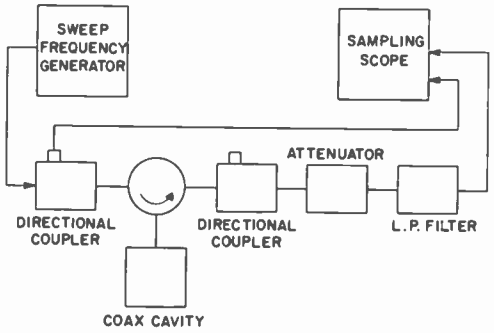


Fig. 1—Experimental arrangement for studying dynamic frequency division.

Dynamic Divide-by-K Circuits

The basic principle of operation of the TED frequency divider is described above. These dividers make use of the refractory-period property of the TED. This section describes an experimental study carried out on TED dividers. Most of these experiments were carried out using two-terminal sandwich-geometry devices. Early results obtained with three-terminal devices in dividing circuits are also described.

Fig. 1 is a schematic of the experimental arrangement used. A two-terminal TED with $nl \geq 2 \times 10^{12}\ \mathrm{cm}^{-2}$ is mounted in a coaxial cavity with a circulator to separate the input and output signals. A sampling oscilloscope is used to display the input and output signals. The TED is dc biased beyond the threshold voltage, so that it oscillates in the transit-time or circuit-controlled mode. The frequency of oscillation

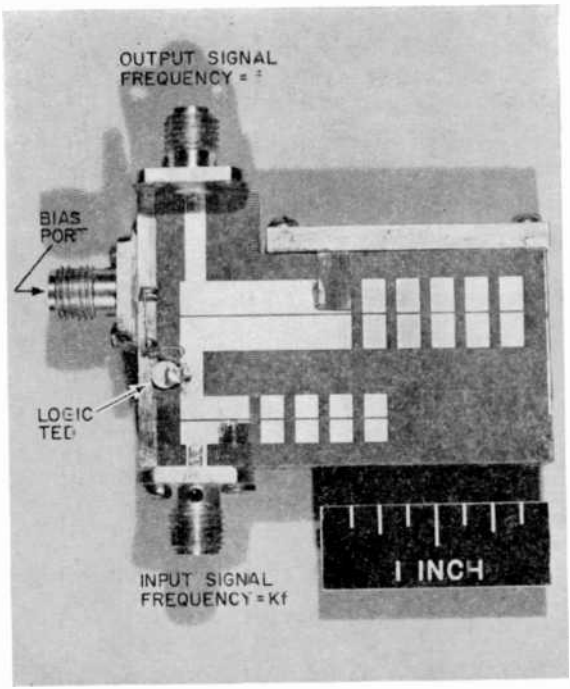


Fig. 2—Dynamic divide-by-2 circuit. Coupled-bar filter structures were used to isolate input and output signals.

and output power are measured. The dc bias is then reduced to the order of 0.9 V_{TH} so that the device ceases to oscillate. The frequency of the sweep generator at the input is adjusted to be 2, 3, or K (where K is an integer) times the frequency at which the TED was oscillating. The input signal amplitude is increased and, beyond a threshold level, an output is obtained. The input and output signals are displayed on a sampling oscilloscope. The output frequency and power are characteristic of the particular TED–cavity combination. We have demonstrated dynamic frequency division by integers up to 6. Fig. 2 is a photograph of a microstrip coupled-bar frequency-divider circuit. Input and output signals are separated here by using coupled-bar filter structures instead of a circulator.

Fig. 3 shows photographs of the input and output waveforms as seen on a sampling oscilloscope for division by 2, 3, and 4. The input frequencies are in X-band. The output waveform is closer to a sinusoidal shape when the frequency is close to 4 GHZ, since the frequency–length (fl) product is then close to 10^7 cm/sec, which is the saturated

electron velocity.[11] The active length l for the device used was 25 μm. This dividing circuit required an input power of 5.0 mW and had an output power of 2.5 mW, corresponding to a conversion loss of 3 dB. These figures include losses in the circulator and filter and are fairly typical for dividers using two-terminal TEDs. We have obtained conversion loss as slow as 0 dB using a high-efficiency (~7%) integral-heat-sink TED. Dynamic division has been demonstrated for frequencies as high as 16 GHz.

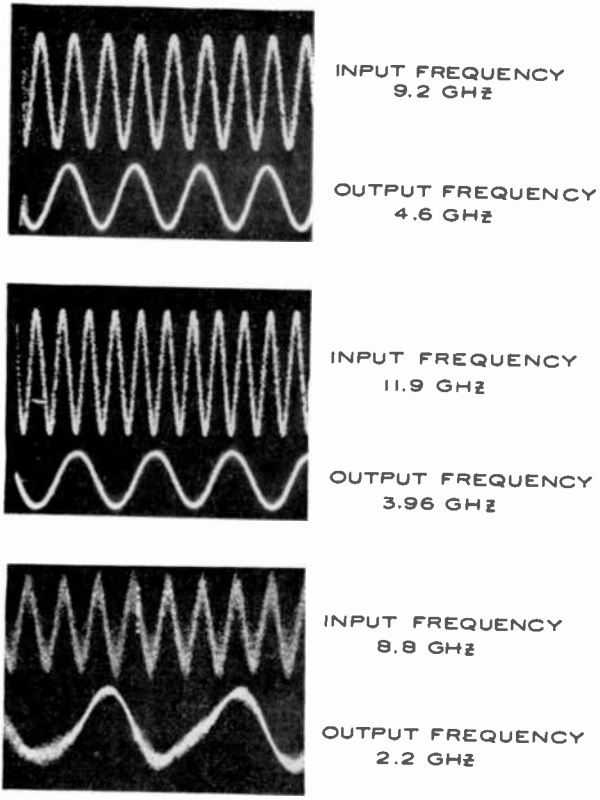


Fig. 3—Sampling oscilloscope waveforms showing microwave frequency division at X-band.

The linearity and bandwidth characteristics of divide-by-2 and divide-by-3 circuits were studied. The experimental arrangement shown in Fig. 1 with an automatic frequency counter substituted for the sampling oscilloscope was used. This allows frequency measurement to an accuracy of ±0.1 MHz. The linearity characteristics of typical divide-by-2 and divide-by-3 circuits are shown in Figs. 4 and 5,

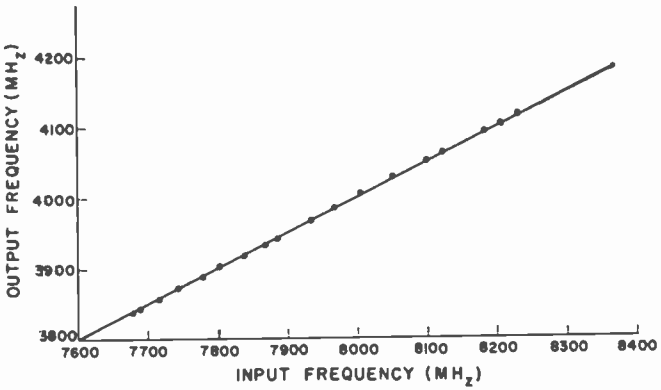


Fig. 4—Linearity characteristic of the divide-by-2 circuit.

respectively. In both cases the linearity is excellent. The bandwidth (for X-band input signals) is 8% for division by 2 and 3.1% for division by 3. Input bandwidth of 10% for X-band, divide-by-2 operation has been obtained using a device with $nl \approx 10^{12}$ cm^{-2}. The conversion loss for this device was 10 dB. The bandwidth of TED divide-by-K circuits is a function of the integer K, TED nl product, and impedance matching at the input and output frequencies.

The phase stability of the frequency-dividing circuit must be very good if it is to find use in any system application. The short-term

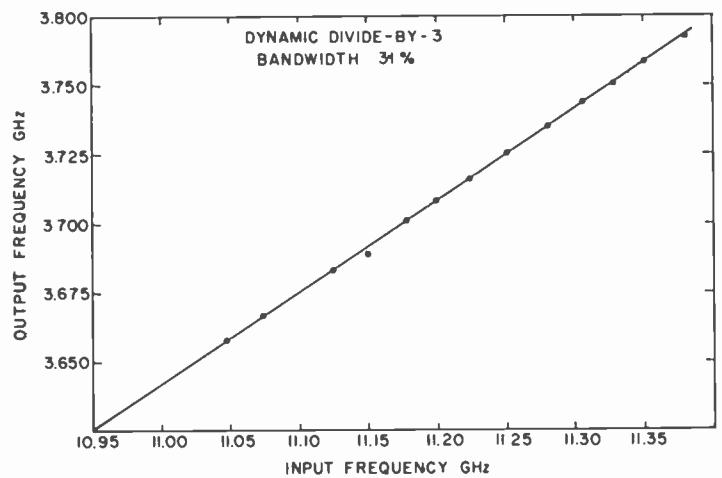


Fig. 5—Linearity characteristic of the divide-by-3 circuit.

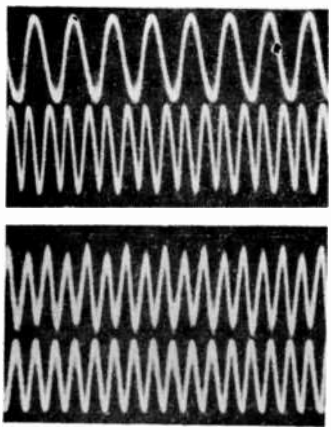


Fig. 6—Input and output waveforms of a divide-by-2/multiply-by-2 circuit. The output is almost an exact reproduction of the input indicating good phase stability of the divide-multiply circuit. The divide-by-2 output is also compared with the input.

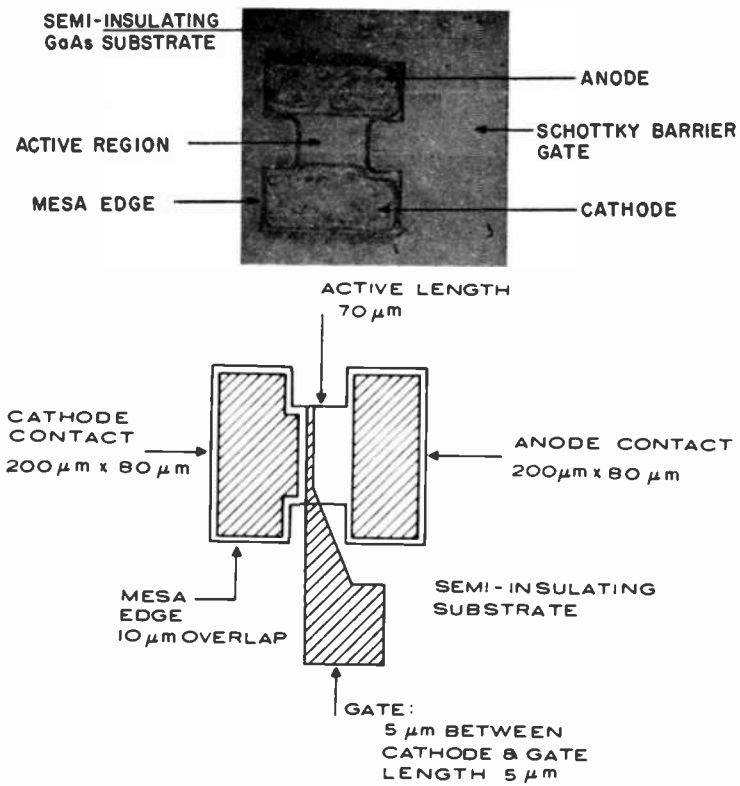
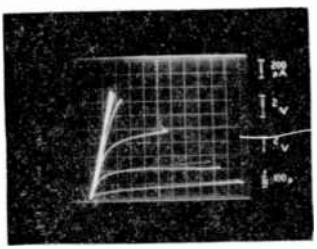
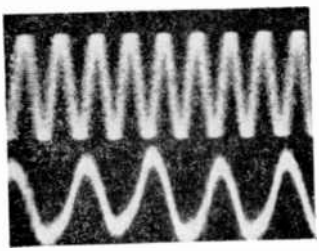


Fig. 7—Schematic diagram and photomicrograph of a planar, Schottky-barrier-gate TED.

stability of the circuit has been studied by multiplying it back to the input frequency level and comparing its waveshape, cycle for cycle, with the input over a large number of cycles. Frequency multiplication is done in a conventional varactor multiplier. The input to the divide-by-two circuit and the output of the divide-by-two and multiply-by-two are fed to the two-channel sampling scope. Fig. 6 shows sampling oscilloscope waveforms of a 9.0 GHz signal. The output follows the input exactly, and there is no observable phase slippage introduced by the dividing circuit after fifteen to sixteen cycles. The output of the divide-by-two circuit is also included in Fig. 6.



(a)



(b)

Fig. 8—Performance of a three-terminal, planar TED (a) *I-V* characteristic with gate bias as a parameter and (b) sampling oscilloscope traces of input and output of a divide-by-2 circuit using planar TED's.

Very preliminary results have been obtained with frequency dividers using planar three-terminal Schottky gate TED's. Fig. 7 shows a schematic diagram and a photomicrograph of a Schottky-barrier-gate TED. Fig. 8 shows the *I-V* characteristic of a three-terminal device and the input–output waveforms obtained when this device was used in a divide-by-2 circuit. This device had a very low ($<10^{12}$ cm^{-2}) doping times thickness product and no input and output matching circuits, and thus division with gain was not obtained.

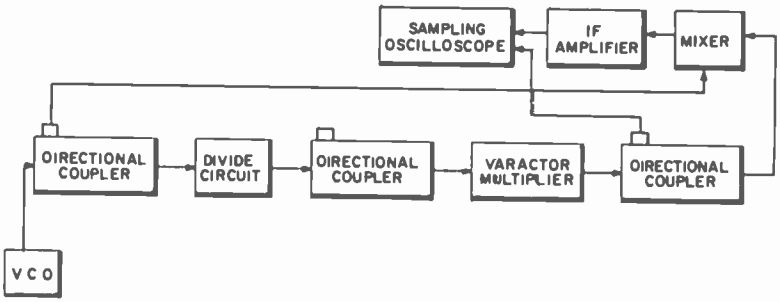


Fig. 9—An experimental arrangement for processing fm signals in a dynamic frequency divider.

Applications of TED Frequency Dividers

The high operating frequency bandwidth, linearity, and phase stability of the TED frequency divider makes it attractive for many systems applications, including microwave frequency synthesizers, frequency translation of high-frequency signals to low frequency for signal manipulation, and processing of FM signals. Processing of frequency-modulated and pulsed signals using the TED frequency divider will now be discussed in detail.

The experimental arrangement used in our study of frequency-modulated signal processing is shown in Fig. 9. A varactor-tuned cw transferred-electron oscillator is used (VCO) to provide the frequency-modulated rf signal at X-band. A triangular pulse modulation on the varactor bias resulted in the required 100-MHz frequency modulation of the TEO. The VCO output was fed through the frequency-dividing circuit. In order to compare the output of the divide-by-two circuit, the signal is multiplied by two in a varactor multiplier and mixed with the VCO output in a mixer. The mixer output is amplified and displayed on the oscilloscope. The multiplier output is detected and also displayed. Fig. 10 shows the results obtained. The top and bottom traces show the i-f output and the multiplier output, respectively.

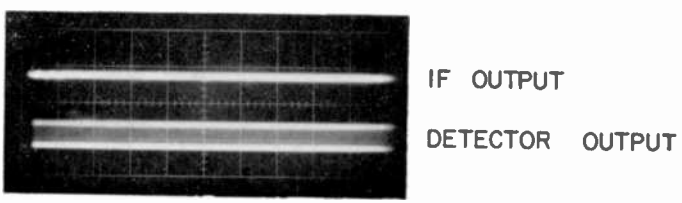


Fig. 10—The i-f and rf outputs of the processed fm signals.

The figure shows that i-f output is zero while the multiplier output is present. The absence of i-f output indicates that the two signals fed to the mixer (i.e., signal and VCO) are identical. This implies that the divide and multiply circuits faithfully follow the input fm signal. The VCO output and the divided–multiplied signal were displayed on a spectrum analyzer as shown in Fig. 11. The two traces were taken separately, and hence a point-by-point comparison is not possible.

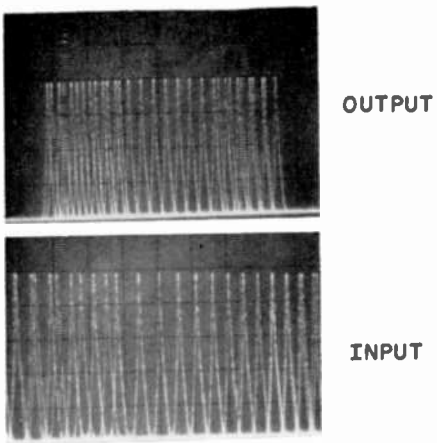


Fig. 11—Spectrum of frequency-modulated input-output signals processed by divide–multiply circuit.

Figs. 12 and 13 show the ability of the TED divider to process pulsed signals. Fig. 12 shows the input and output spectra for a pulse width of 2 μsec and a repetition rate of 10 kHz. The output and input pulse shapes are very similar. Fig. 13 shows the input and output spectra for a pulse width of 100 μsec and a repetition rate of 1 kHz. The input frequency was 8.9 GHz.

These experiments clearly indicate that it is possible to process fm signals through TED frequency-dividing circuits.

Conclusions

Dynamic frequency dividing circuits utilizing the transferred–electron effect in GaAs have been developed at microwave frequencies. Preliminary experimental results indicate that division by integers up to 6 is feasible. Both cw and pulsed signals at frequencies as high as 16.0 GHz have been processed through TED frequency dividers. Large bandwidths and low conversion loss combined with excellent linearity and phase stability make TED frequency dividers suitable for micro-

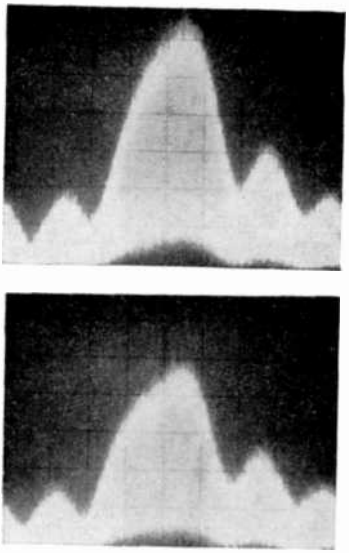


Fig. 12—Pulsed rf spectrum processed through divide-multiply circuits. The pulse width is 2 μsec and pulse repetition rate is 10 kHz.

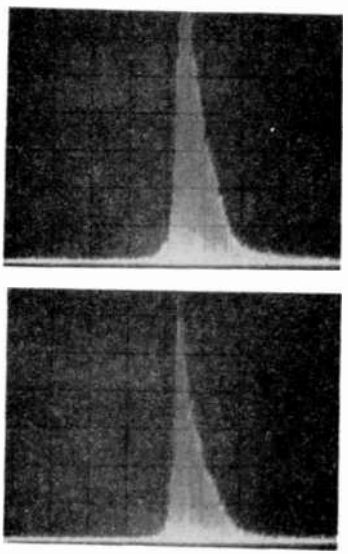


Fig. 13—Pulsed rf spectrum processed through divide-multiply circuits.

wave frequency synthesizers and signal processing systems. Frequency dividers using three-terminal planar Schottky-barrier-gate input TED's have the potential for division with gain, which is even more important for system applications.

Acknowledgments

The authors wish to thank S. T. Jolly for providing epitaxial GaAs wafers and R. Smith for fabricating the devices. The authors also thank F. Sterzer and M. Nowogrodzki for many helpful discussions. This work was supported by USAF Avionics Laboratory, Wright-Patterson Air Force Base, Dayton, Ohio, under Contract No. F33615-72-C-1874.

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GaAs FET for High Power Amplifiers at Microwave Frequencies*

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Abstract—The GaAs FET has been shown to have excellent potential as a microwave power amplifier. There are two major reasons for this. First is the inherently high figure of merit of GaAs as defined by the product of maximum electric field times maximum carrier velocity, and second is the very high electron mobility. These two effects combine to yield devices that have delivered 0.63 watt at 6 GHz with 1 dB gain compression. This paper discusses the suitability of GaAs FET's as microwave power amplifiers, device geometry and material parameters for optimum output power as a function of frequency, and finally device fabrication.

GaAs Versus Silicon for High Power at Microwave Frequencies

The most important part of a Schottky-barrier field-effect transistor is the region under the control, or gate, electrode. This is the part of the device where carriers are traveling at or near their peak velocity and the transit time of these carriers determines the upper frequency limit of operation. In addition, the electric field reaches its maximum

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value near the gate electrode so that breakdown voltage and therefore output power is limited by the nature of the semiconductor material in the vicinity of the gate.

E. O. Johnson[1] has defined a figure of merit for semiconductor power devices that improves with increased breakdown electric field and improves with increased carrier velocity. The reason for this is as follows. If a device has its length specified, the maximum frequency of operation will be limited by the amount of time it takes an electron traveling at its maximum velocity to transit through it. The maximum rf voltage swing will be fixed by the breakdown electric field multiplied by the device length. The output admittance per unit area is determined by the capacitive susceptance of the device, which is proportional to frequency and inversely proportional to device length. To increase frequency at constant admittance level requires a reduction in output power, resulting in the well known $Pf^2 = \text{constant}$ relationship.

Electrons in GaAs can travel a factor of two faster than they can in silicon, while the maximum electric field that can be maintained in GaAs is essentially the same as that in silicon. Based on the Pf^2 relationship, then, GaAs devices should have a factor of four improvement in output power over silicon devices at the same frequency. In addition, the electron mobility in GaAs is a factor of 3 higher than in silicon; thus, the input power for field-effect transistors should be a factor of three lower for GaAs. Thus, the intrinsic gain for a GaAs power transistor should be a factor of 12 higher than for a similar silicon device. This feature, together with the promise of greater output power make the GaAs FET very attractive as a device for microwave power amplification.

Maximum-Output-Power Design

A high-power device is generally operated at about f_T, which in the case of an FET is the transit time frequency, so that the selection of frequency fairly well fixes the length of the gate electrode. Under conditions of maximum output power, the control electrode voltage makes large enough excursions to completely deplete the carriers from under the gate. The output power is proportional to the maximum current times the maximum voltage swing. The current swing is proportional to the total number of carriers under the gate, or the product NT. The voltage swing is equal to the maximum voltage one can apply to the drain when the gate is fully reverse biased (no drain current), which is equal to the difference between the Schottky-

barrier breakdown voltage and the Schottky-barrier pinchoff voltage. Since the breakdown voltage decreases less than linearly with density and the pinch-off voltage increases linearly with density, the difference between the two decreases, goes to zero, and can be negative. Since the current increases with density, the product of current and voltage,

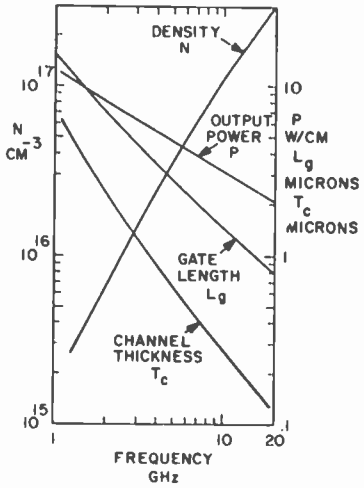

Fig. 1—Optimum channel-layer density and thickness, gate length, and output power versus frequency.

or the output power, has a maximum at a particular density. The optimum carrier concentration determined from this criteria and the gate length, epitaxial layer thickness, and power are plotted versus frequency in Fig. 1.

Extrinsic Losses

An operating FET requires ohmic contacts to the source and drain electrodes and thin-film metalization for the Schottky-barrier gate electrode. Both the contact resistance for ohmic contact, and the thin-film metalization resistance for the Schottky-barrier gate electrode introduce loss, and thus degrade power gain. For example, referring to Fig. 2, if one were to fabricate a 1.5 GHz power FET with the boundary condition of 1-dB gain degradation due to contact resistance, the maximum contact resistance that one can tolerate is 4×10^{-4} ohm-cm^2. The optimum carrier concentration for this frequency is 4×10^{15} cm^{-3}, and alloy contacts with low enough contact resistance can and have been made on material of this carrier concentration. On the other hand, for the same loss on a 10-GHz device, the contact

resistance must be less than 4×10^{-6} ohm-cm^2, while the optimum carrier concentration is 1×10^{17} cm^{-3}. Alloy contacts on 10^{17} cm^{-3} GaAs typically have too high a contact resistance (10^{-5} ohm-cm^2). As described in the next section we used double epitaxy to reduce the contact resistance to an acceptable value.

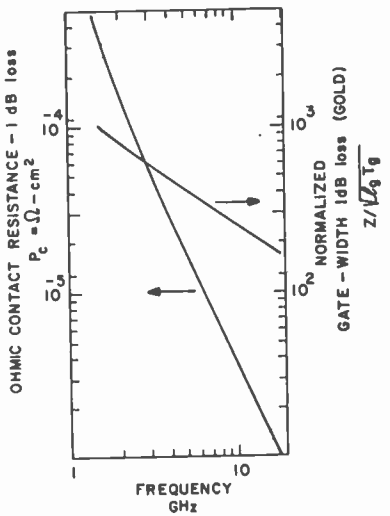

Fig. 2—Ohmic contact resistance and normalized gate width for 1-dB maximum extrinsic losses.

To maximize the output power of a device, the source periphery, or source width, must be as large as possible. This increase in width is accompanied by a reduction in input resistance of the semiconductor portion of the device and a corresponding increase in gate metalization resistance. When the latter becomes a significant fraction of the former, extrinsic gate metalization losses ensue. Fig. 2 shows the maximum normalized gate length as a function of frequency for a degradation of 1 dB due to gate metalization. As an example, at 10 GHz a gate 1.5 μm long by 400 μm wide must be 1.5 μm thick to limit the gate losses to 1 dB. Further increases in source width must be accomplished by the multiple-gate technique described in the following section.

Device Fabrication

Double epitaxy technology is employed in our device fabrication in order to obtain optimum carrier concentration in the channel layer,

while at the same time maintaining low contact resistance. The device fabrication steps starting with the double epitaxial layer are shown in Fig. 3. An initial evaporation on the heavily doped n+ layer forms of ohmic contact. A narrow gap is etched in the ohmic contact to define a source and drain and expose the n+ gallium arsenide over the channel region. A semiconductor etch is then used to remove the n+ layer in the gap, and expose the relatively high resistivity layer. Finally, the gate electrode is formed by a second metal evaporation that condenses precisely between the source and drain, without short circuiting, because of the cantilever effect of the overhanging source and drain electrodes. The entire device is in the form of a mesa so that the gate bonding pad lies on the semi-insulating surface of the gallium arsenide, and therefore avoids that form of parasitic capacitance.

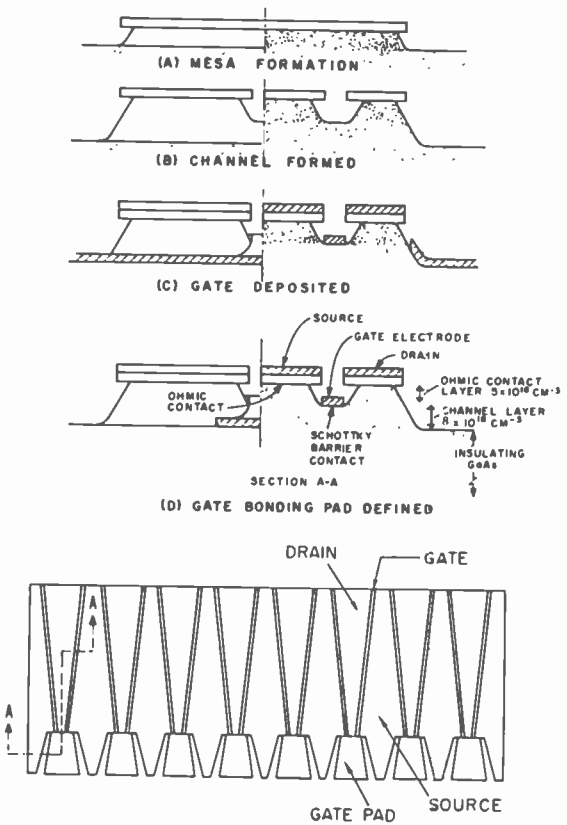

Fig. 3—Multigate FET fabrication steps.

The layout of the device shown in Fig. 4 is that of a multi-parallel-gate-structure with minimum cross-over capacitance. There are 16 gates that are 2 to 2½ μm long, and 0.016 inch wide. The gates are subdivided into pairs in the form of a "V", with the drain in the center of the "V" and the sources on the sides. The gate bonding pad joins the gates at the bottom of the "V". The sub-units are isolated, since each drain electrode is common only to one gate electrode,

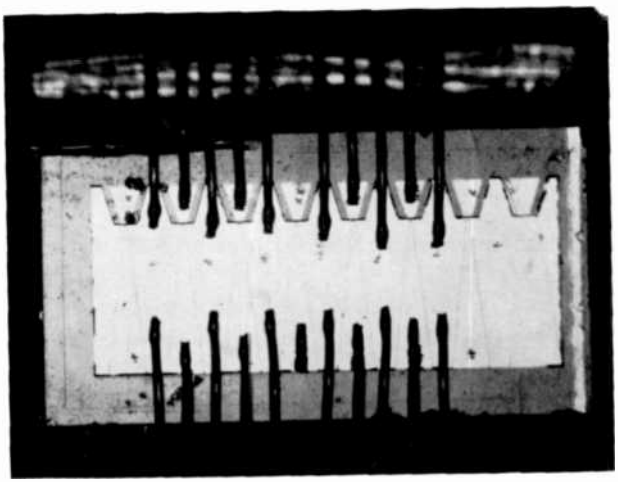

Fig. 4—Multigate FET with four units bonded into the circuitry.

but adjacent sub-units have a common source electrode. Since the sub-units could be interconnected by bond wires, there is no degradation due to overlay capacity. The active device size, 0.050 inch in the long dimension, is about as small as one can make it and still wire bond to each individual sub-unit. A smaller device size would have to be accompanied by an overlay interconnect technique, but this overlay would have to be done without significantly increasing feedback or output capacity.

Device Characteristic and Microwave Measurements

Fig. 5 is a series of current-voltage characteristics of the multigate FET as each unit was bonded into place. One unit corresponds to 0.032-inch-wide source (or gate). The maximum number of units tested on one pellet was 6 out of a possible eight. In a microstrip test fixture, the linear gain was typically 6 dB at 6 GHz and the output power was approximately 0.15 watt per unit at zero dB gain. That is,

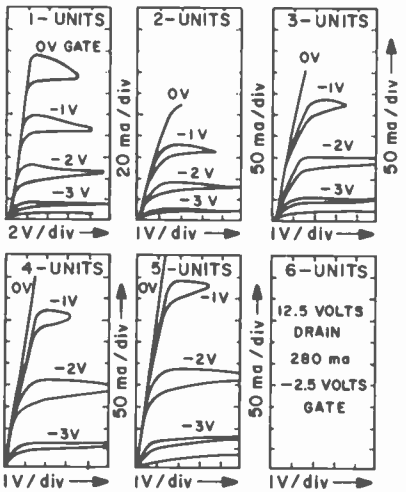

Fig. 5—Current–voltage characteristics of 6-unit FET as each unit is bonded into place.

for one unit bonded into place, 150 mW was obtained at unity gain, while for 6 units bonded into place, 1 watt was obtained at unity gain. When the FET was operated in the pulsed mode, the gain increased by about 3 dB. The compiled data for several devices, both cw and pulsed, is shown in Fig. 6.

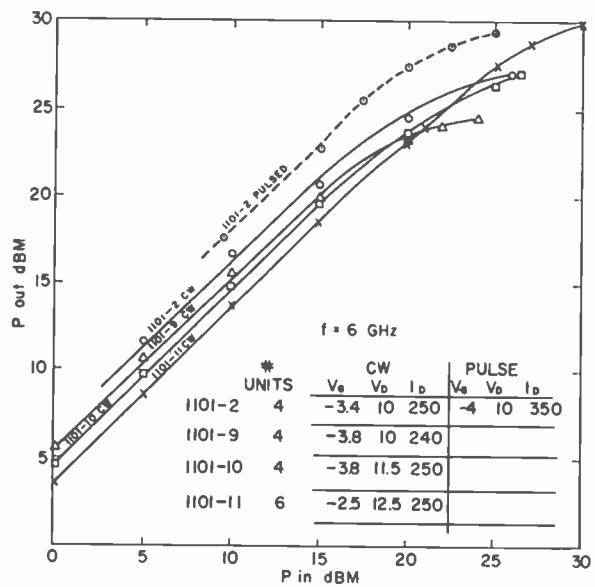

Fig. 6—CW and pulsed output power versus input power for 4- and 6-unit FET's.

Conclusion

The power amplifier capabilities of GaAs Schottky-barrier-gate FET's have just begun to emerge. The combined characteristics of high breakdown voltage associated with the Schottky-barrier electrode on GaAs together with the high saturation velocity and drift mobility of electrons in GaAs make this device well suited as a power amplifier at microwave frequencies.

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The Chemical Polishing of Sapphire and Spinel

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Abstract—The chemical polishing of sapphire and spinel in molten borax was investigated, and a technique has been developed for polishing both sapphire and spinel substrate orientations that lead to [100]-oriented epitaxial silicon and that produces very smooth scratch-free surfaces free of etch pits and work damage. The effect of temperature, melt composition, and spacer thickness upon the etch rate was determined. Silicon with high mobility has been grown on these chemically polished surfaces, and x-ray topographic micrographs have confirmed that they are free of work damage and scratches .

Introduction

This paper describes a chemical polishing technique that has been developed for preparing sapphire and spinel surfaces that are smooth, free of work damage and scatches, and are suitable for use as substrates upon which to deposit silicon films for MOS integrated circuits.

Single-crystal sapphire and spinel boules grown by the Czochralski technique using iridium crucibles are commercially available with diameters ranging from ¼ to 3 inches. For use as substrates for silicon growth, a boule is oriented by x-ray Laué techniques to a specific sapphire plane, the most common one for MOS applications being $[1\bar{1}02]$, which is about 57° to the C axis and leads to [100]-oriented silicon layers.

Once oriented, the boule is sliced into wafers by using a diamond saw (cutting rate about 10 mils/min). These wafers are then waxed onto a polishing block and polished using high pressure and diamond grit of successively smaller grit size to give a smooth, scratch-free, substrate surface. This polishing step is relatively expensive and is quite difficult because sapphire is such a hard material.

The substrates are cleaned in organic solvents to degrease them (usually chloroform and methyl alcohol) and then further cleaned in Caro's acid, rinsed twice in distilled water, and blown dry prior to being placed in the growth apparatus.

Robinson and Mueller[1] reported in 1964 that heat treatment of this mechanically polished sapphire substrate in hydrogen at temperatures ranging from 1250°C to 1500°C for various times prior to silicon growth produced significant changes in the surface structure of the sapphire substrate. This is an important step, since it is the surface atomic layers of the substrate that determine the nucleation and perfection of the silicon layers. The mechanically polished sapphire surface before heat treatment produced a ring-type electron diffraction pattern, as shown in Fig. 1. After heating in hydrogen at 1205°C for 30 minutes, the electron diffraction pattern shown in Fig. 2 was obtained; as can be seen there is a significant improvement in the crystallinity of the sapphire surface. This change in surface structure occurs probably by a combination of annealing and surface rearrangement, or both, as well as by a thermal etching process.[2]

This prefiring technique has received wide acceptance by most investigators concerned with the growth of silicon on sapphire, since it is simple and compatible with the epitaxial growth technique, and there is little chance of contaminating the sapphire surface with a species that may be electrically active in the silicon.

By far the most reproducible as well as the best crystallographic and electrical characteristics of silicon layers grown on sapphire substrates have been obtained on those substrates that have been prefired in hydrogen prior to silicon growth. This has not been the case for spinel, as discussed later.

The importance of having a scratch-free substrate surface for the growth of silicon can be seen from Fig. 3, which shows a poorly polished sapphire surface with a 0.2-μm-thick silicon film grown upon it. The growth is seen to take place preferentially upon the scatches, and the surface coverage was found to be incomplete at this silicon thickness. If a 1-μm-thick silicon film is grown on this poorly polished substrate, the scratch lines are found to be replicated on

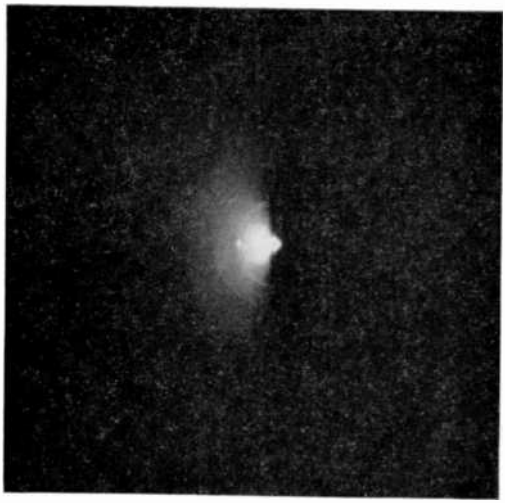

Fig. 1—Electron diffraction pattern of mechanically polished sapphire surface.

the surface of the silicon film. This can lead to diffusion spikes when junctions are prepared in the epitaxial layers.

The main objectives of chemical polishing of sapphire and spinel with molten borax ($Na_2B_4O_7$) are (1) to remove the work damage and underlying scratches produced by the sawing and polishing steps. (2) to possibly replace the relatively expensive mechanical polishing

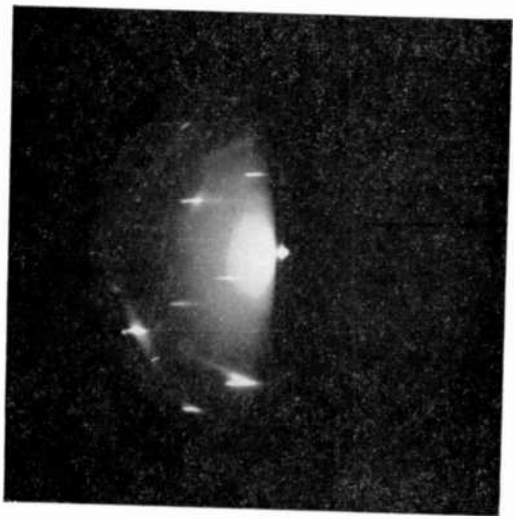

Fig. 2—Electron diffraction pattern of mechanically polished sapphire surface fired at 1250°C for 30 minutes.

step with an all chemical etching and polishing process, (3) to reduce the reactivity of the spinel substrate surface to hydrogen at the high growth temperature.

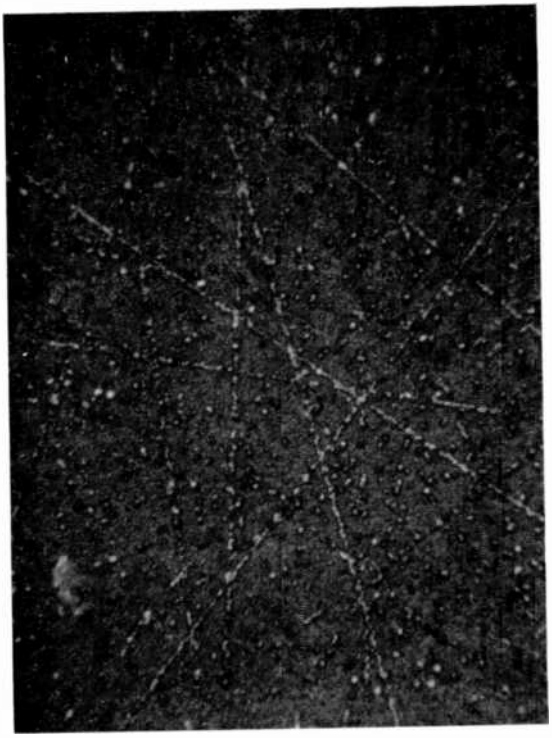

Fig. 3—0.2 μm silicon film grown on a poorly polished sapphire surface (original photographed at 200× magnification).

Experimental

The apparatus used for chemical polishing is shown in Fig. 4. The platinum crucible containing the molten borax was heated by a resistance furnace. Two different platinum-wire substrate holders were used. The first was for a single substrate and held the sample either directly above or immersed in the molten borax. The second holder, shown in Fig. 4, was developed for a batch, multiwafer, closed-spaced technique capable of polishing many wafers at one time.

Results

1. Chemical Stability of Spinel in Hydrogen at High Temperature

The chemical stability of stoichiometric spinel was compared with that of alumina-rich spinel in hydrogen over the temperature range

1005 to 1200°C, because poor quality silicon films have been consistently obtained in hydrogen at 1100°C on melt-grown stoichiometric spinel substrates, while silicon with good crystallographic and electrical properties have been obtained on alumina-rich substrates. It was found that

(1) alumina-rich spinel is more stable in hydrogen in the 1100 to 1200°C temperature range than is stoichiometric spinel;

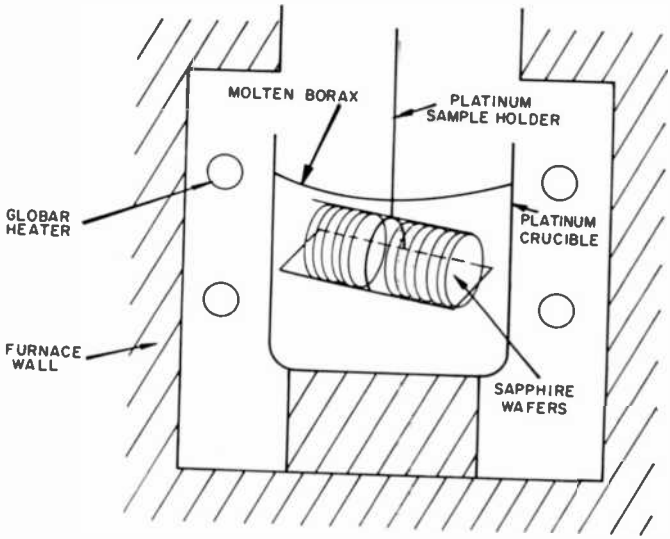

Fig. 4—Multiwafer etching apparatus.

(2) At 1200°C, the stoichiometric spinel surface reacts with hydrogen to liberate magnesium, which results in a film coating on the wall of the reaction chamber;

(3) The resulting spinel surface becomes alumina-rich, and a very large number of microcracks along crystallographic directions about 1-mil deep become visible at 200 × (Figs. 5 and 6)

Green[3] has recently attributed this cracking to the fact that a composition gradient is created by the Mg depletion of the spinel surface. Since the lattice parameter of spinel is a function of composition, a strain large enough to produce brittle fracture of the crystal surface results.

2. Etching Sapphire and Spinel in Borax

It was found that suspension of a [1$\bar{1}$02]-oriented sapphire substrate above molten borax at 1100-1150°C consistently produced a very

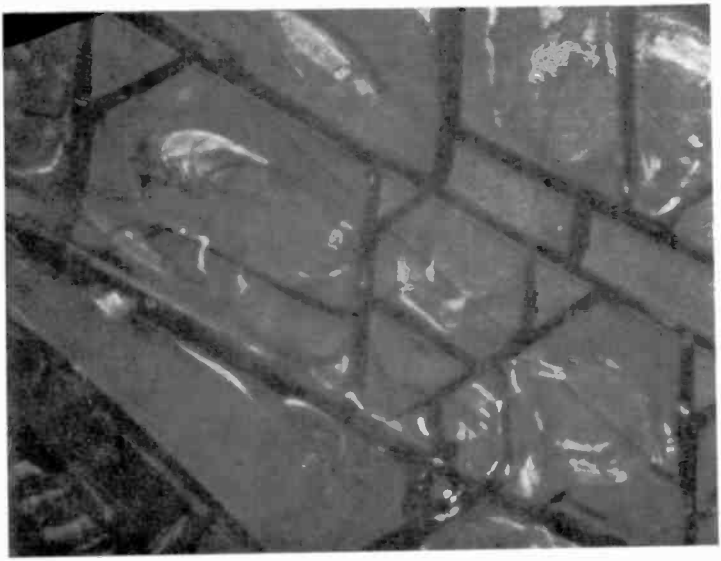

Fig. 5—[111] stoichiometric spinel heated in hydrogen 1 hour at 1100°C (original photographed at 200× magnification).

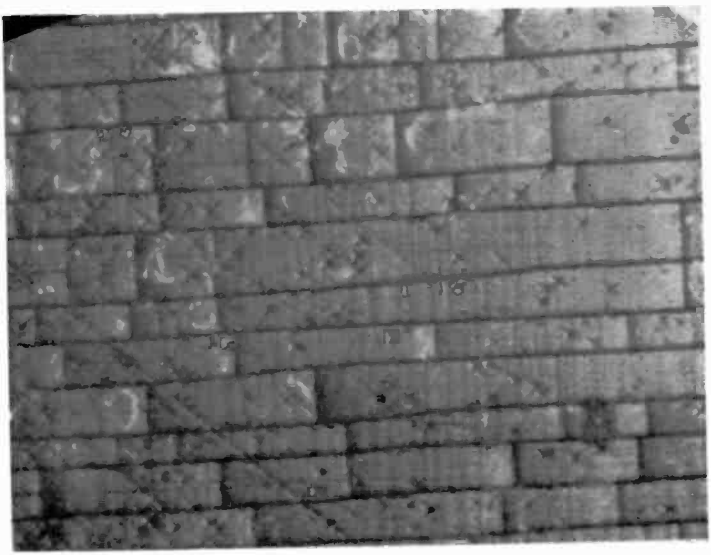

Fig. 6—[100] stoichiometric spinel heated in hydrogen 1 hour at 1100°C (original photographed at 200× magnification).

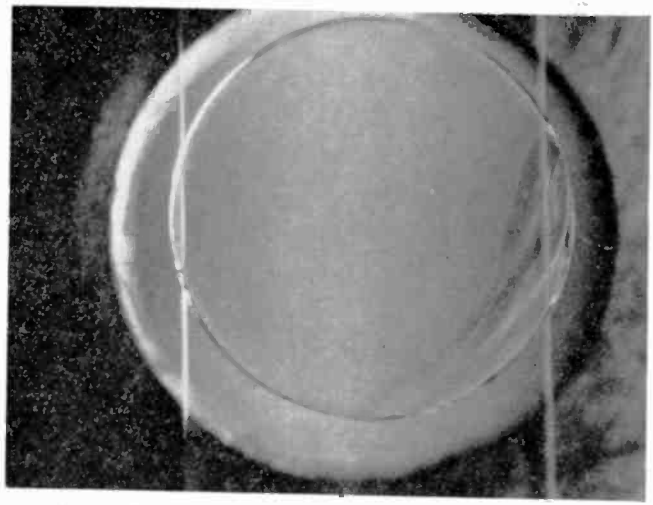

Fig. 7—[1102] sapphire substrate etched at 1100°C above molten borax (original photographed at 2× magnification).

smooth, flat sapphire surface containing no scratches (Fig. 7). Using these same conditions with [100]-oriented spinel produced preferential etching with a large number of etch pits. as shown in Fig. 8. If either the [1$\bar{1}$02]- or [0001]-oriented sapphire substrates or the [111]-

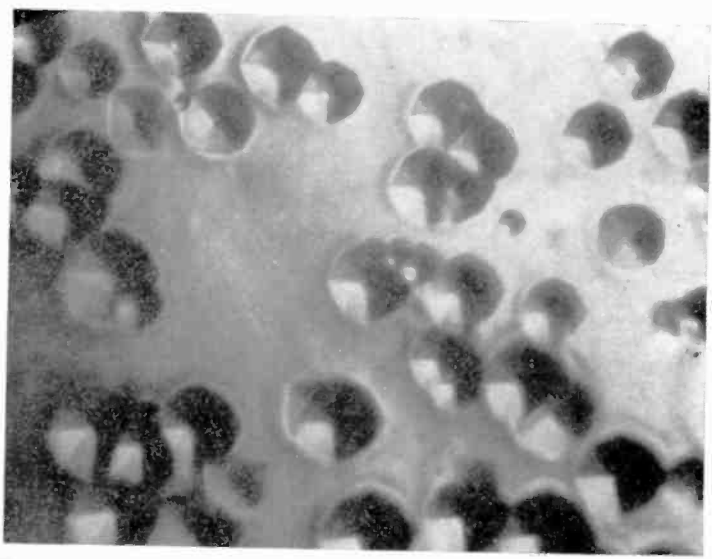

Fig. 8—Etch pits produced by borax etching [100] spinel at 1100°C (original photographed at 660× magnification).

or [100]-oriented spinel substrates were immersed into molten borax at 1100°C, a very badly pitted substrate surface resulted.

By decreasing the temperature of the molten borax to 800°C to 900°C range and immersing [100]-oriented spinel substrates, very smooth polished surfaces were obtained on both stoichiometric and alumina-rich material. A typical chemically polished spinel surface is shown in Fig. 9. Using these etching conditions the [111] spinel

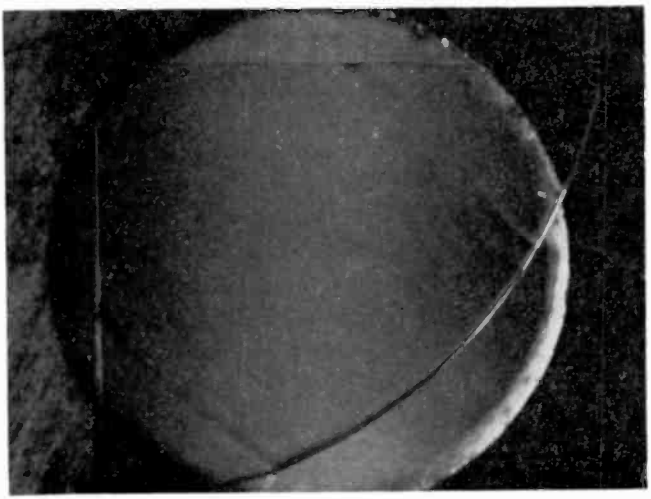

Fig. 9—Borax etched [100] spinel at 800° C (original photographed at 2× magnification).

orientation resulted in many etch pits, as shown in Fig. 10. Fig. 11 depicts the underlying scratches and damage that can be uncovered on both hydrogen prefired and mechanically polished substrates by chemically removing only 1 μm of material from the surface. It is quite evident that scratches are filled in and covered up by the mechanical polishing step.

The following chemical etchants have been reported for both sapphire and spinel:

H_2SO_4	PbF_2
H_3PO_4	SiH_4 (small amounts)
KOH	HCl
B_2O_3	$K_2S_2O_8$ potassium persulfate
V_2O_5	F_2

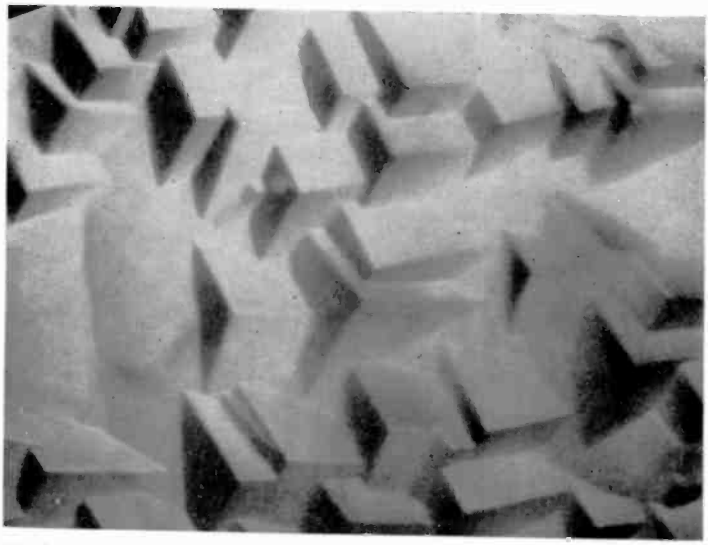

Fig. 10—Etch pits using [111] spinel at 800°C in molten borax (original photographed at 660× magnification).

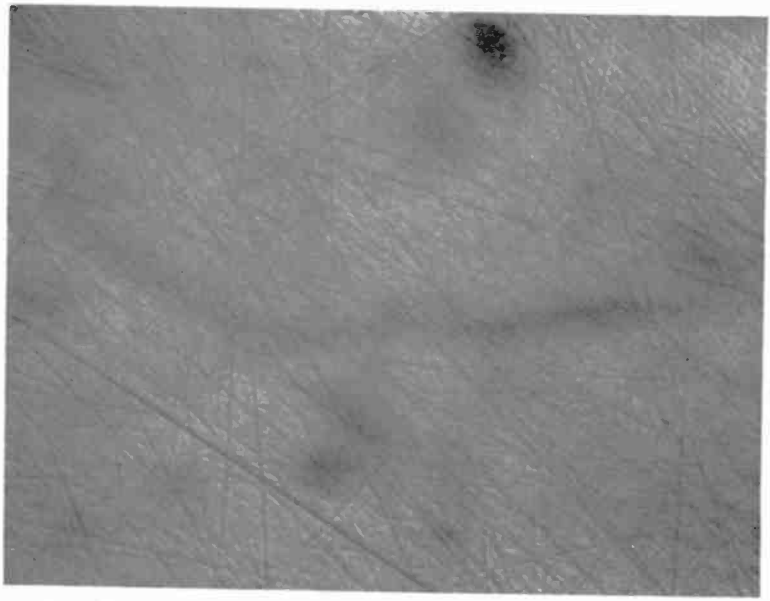

Fig. 11—Underlying scratches revealed by removing 1μ of sapphire surface using borax (original photographed at 200× magnification).

Most of these were found difficult to control and gave irreproducible results. All yielded poor-quality substrate surfaces and, as a result, poor-quality silicon films.

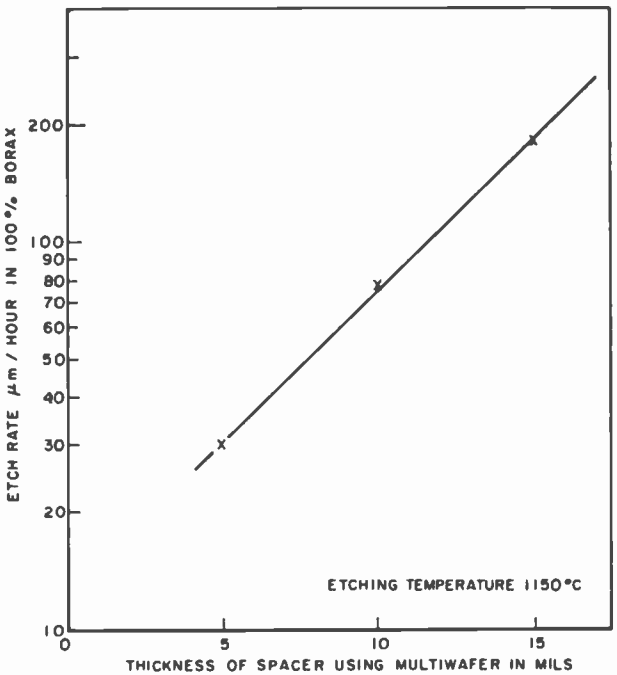

Fig. 12—Etch rate versus spacer thickness.

For use with the borax etching technique, a batch, multiwafer, closed-spaced etching technique has been developed whereby several as-sawed sapphire substrate wafers that have been rough lapped (25 μm Boron carbide) can be chemically polished satisfactorily by the removal of about 2 mils of material. The dependence of etch rate versus spacing between sapphire substrates for a temperature of 1150°C is shown in Fig. 12.

The quality of the sapphire and spinel borax polish as well as its etch rate were found to be very dependent upon the Al_2O_3 concentration of the borax melt. The etch rate of a single sapphire substrate immersed in molten borax at 1100°C as a function of the Al_2O_3 concentration of the melt over the concentration range 0-20 weight percent is shown in Fig. 13. The etch rate decreases with increasing concentrations of Al_2O_3; the better quality surfaces were obtained at the higher

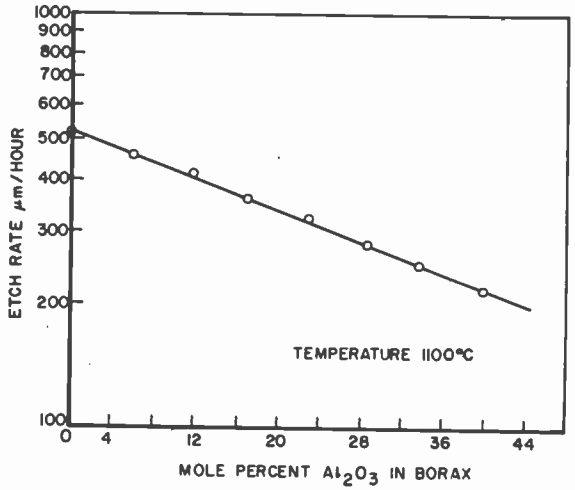

Fig. 13—Etch rate versus Al_2O_3 concentration in borax melt (etching time typically 3 minutes).

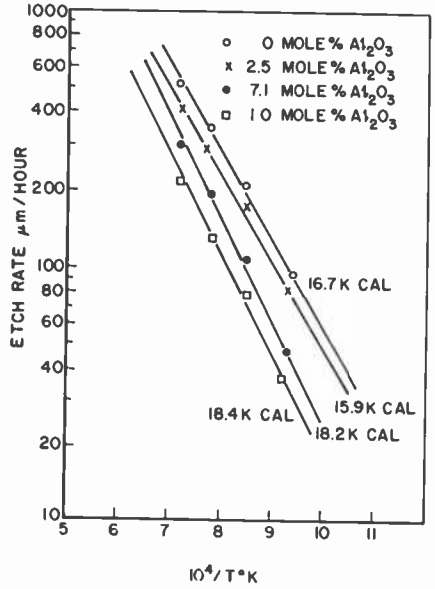

Fig. 14—Etch rate versus temperature.

Table 1—Mobility of 1-μm P- and N-Type Silicon Films On [1$\bar{1}$02] Borax-Etched Sapphire*

	Mobility cm^2/volt sec	Carrier Concentration
n-type	350-450	1×10^{16}
p-type	150-200	1×10^{17}

* Results are about equal to what is obtained on the best mechanically polished sapphire substrates.

Al_2O_3 concentrations, while the lower Al_2O_3 concentrations with their faster etch rates resulted in badly pitted sapphire surfaces.

The dependence of the sapphire etch rate upon temperature for four different Al_2O_3 concentrations in the melt are shown in Fig. 14. The activation energy for the process is between 16-18 kcal.

3. Mobility on Borax Polished Sapphire and Spinel

p- and n-type mobilities of 1-μm-thick silicon films have been measured on [1$\bar{1}$02] chemically polished sapphire substrates. These are shown in Table 1 and are approximately equal to those that have been obtained on the best mechanically polished hydrogen-prefired sapphire substrates.

The mobility results obtained on stoichiometric spinel are shown in Table 2. These samples had a minimum exposure to hydrogen at high temperature prior to growth and indicate that eliminating the work damage on stoichiometric spinel substrates significantly reduces the chemical reactivity of the spinel substrate surface to hydrogen at high temperature.

4. X-Ray Topography

X-ray transmission–reflection topographs on borax-polished and hydrogen prefired spinel and sapphire substrates are shown in Figs. 15 and 16. The topographs confirm that all the work damage and underlying scratches are removed by the borax polishing technique. In

Table 2—Mobility of 1-μm P- and N-Type Silicon Films On [100] Borax Etched Stoichiometric Spinel

	Mobility cm^2/volt sec	Carrier Concentration
n-type	500-600	$N_D \simeq 10^{16}$
p-type	200	$N_A \simeq 10^{16}$

Note: If SiH_4-H_2 system is used to grow silicon films at 1100°C on [100] stoichiometric spinel substrates having a mechanical polished surface, cloudy films having a low mobility and higher than normal resistivity result.

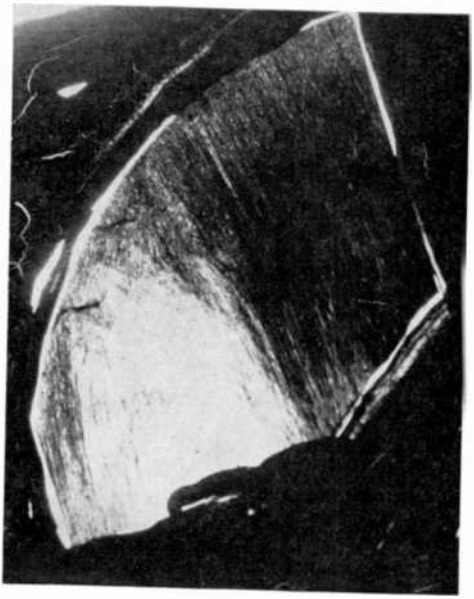

Fig. 15—X-ray topograph of [100] borax etched spinel surface reflection-transmission.

Fig. 16—X-ray topograph of a borax etched [1102] sapphire surface reflection-transmission.

the case of spinel, individual dislocations are resolved, which has not been reported for spinel surfaces prepared by other techniques.

5. Borax Polishing of Sapphire Spheres

Several sapphire spheres (½-inch diameter) were borax polished to remove about 5 mils of material. These were then examined by both x-ray Laué and optical techniques and showed that the dislocations originate on the C axis and then propagate along the three mirror planes of sapphire.

Summary

A technique has been developed for chemically polishing both sapphire and spinel substrate orientations that lead to [100]-oriented epitaxial silicon and that produces very smooth surfaces free of scratches, etch pits, and work damage.

The quality of the chemically polished surface was found to be dependent upon the etching temperature as well as the concentration of Al_2O_3 contained in the borax melt. Silicon with very high mobility has been deposited upon these chemically polished surfaces, and x-ray topographic micrographs has confirmed that they are free of work damage and underlying scratches. This technique looks very encouraging and could reduce the cost of both sapphire and spinel substrates.

Acknowledgments

The authors would like to thank S. H. McFarland for the x-ray topograph results reported as well as Ronald Smith for the x-ray Laué analysis. Thanks are also due to C. W. Mueller and H. Kressel for the encouragement that they have shown concerning this work. The authors would also like to express their appreciation to N. Goldsmith for critically reading this manuscript.

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The Electrostatic Field Near Weakly Deformed Conducting Surfaces

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Abstract—The calculation of the electrostatic field near a deformed capacitor surface has been reduced to a calculation scheme for surface charges. For weak deformations expansions in terms of the deformations are indicated. Numerical computations have been carried out for a sinusoidal shape of the electrode.

1. Introduction

In this paper the analysis of electrostatic fields near periodically deformed conducting surfaces is discussed. The methods and results can be applied to various systems and devices. The specific assumptions under which the present calculations have been carried out are suited for investigating effects of surface roughness on the performance of photocathodes as studied by Martinelli.[1] Another system of current interest, which we consider here to some extent, consists of light valves with a deformable mirror layer as developed by Roach et al.[2]

In the latter case the knowledge of the electrostatic field is of vital importance for an understanding of the electromechanical instability of the mirror surface (frost phenomenon).

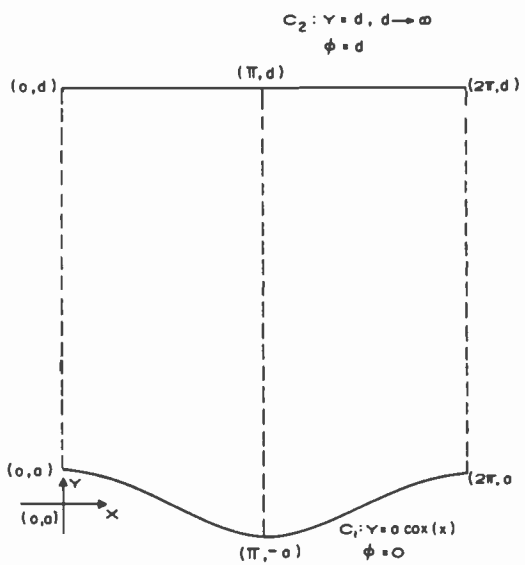

Fig. 1—Geometry of sinusoidal problem.

2. Sinusoidal Surface

The simplest configuration containing some of the essential aspects of the problems mentioned in the introduction is that exhibited in Fig. 1. In this planar capacitor (electrode shapes invariant in the z direction), one electrode (C_2) is flat and allowed to recede to infinity in the y direction while the other has a periodic sinusoidal shape of variable amplitude. A study of the trajectories of electrons emanating from such a surface will give an indication of effects arising from cathode roughness.

2.1 Formulation

The solution to this problem must satisfy Laplace's equation and must be asymptotically ($d \rightarrow \infty$) proportional to y. Therefore, an appropriate representation for the solution function is

$$\varphi = Ay + \sum_{n=0}^{\infty} C_n e^{-ny} \cos(nx), \qquad [2.1]$$

where the parameters (A, C_n) are to be chosen to satisfy the boundary conditions

$$\left.\begin{array}{ll} \varphi = 0, & y = a\cos(x), \\ \varphi = d, & y = d. \end{array}\right\} \quad 0 \leqslant x \leqslant \pi \qquad [2.2]$$

The form of the individual terms guarantee that the solution so represented will satisfy the appropriate periodicity and symmetry relations implicit in the problem.

Applying the second boundary condition one obtains

$$\begin{aligned} A &= 1 - \frac{1}{d} \sum_{n=0}^{\infty} C_n e^{-nd} \cos(nx), \\ &= 1 + 0\left(\frac{1}{d}\right), \end{aligned} \qquad [2.3]$$

exhibiting the fact that the terms under the summation represent effects local to the deformed surface (C_1). Thus, the form

$$\varphi = y + \sum_{n=0}^{\infty} C_n e^{-ny} \cos(nx), \qquad [2.4]$$

satisfies all conditions of the problem and the C_n are to be determined from the first of Eq. [2.2], to wit,

$$\left. y + \sum_{n=0}^{\infty} C_n e^{-ny} \cos(nx) \right|_{y = a\cos(x)} = 0. \qquad [2.5]$$

For a given number of terms (N), approximations to the C_n $(C_n{}^N)$ will be determined by requiring that Eq. [2.5] be satisfied in the sense of least squares, i.e., that

$$M = \int_0^{\pi} \{a\cos(x) + \sum_{n=0}^{N} C_n{}^N e^{-na\cos(x)} \cos(nx)\}^2 \, dx, \qquad [2.6]$$

be minimized with respect to the C_n^N. It is to be expected that the C_n^N will converge to the C_n as $N \to \infty$. Henceforth, the superscript (N) will be omitted, but is implicitly present.

When Eq. [2.6] is partially differentiated with respect to each of the C_m $(m = 0, 1, \ldots, N)$ in turn and the derivatives set equal to zero, the system of linear equations

$$\sum_{n=0}^{N} S_{mn} C_n = b_m, \; m = 0, 1, \ldots, N \qquad [2.7]$$

is obtained, with

$$S_{mn} = \frac{2}{\pi} \int_0^{\pi} e^{-(m+n)\,a \cos(x)} \cos(mx) \cos(nx)\, dx,$$

$$b_m = -\frac{2a}{\pi} \int_0^{\pi} e^{-ma \cos(x)} \cos(mx) \cos(x)\, dx. \qquad [2.8]$$

Making use of the identity (Fourier expansion)[3]

$$e^{z \cos(x)} = I_0(z) + 2 \sum_{k=1}^{\infty} I_k(z) \cos(kx), \qquad [2.9]$$

along with addition formulas for trigonometric functions, one obtains

$$S_{mn} = (-1)^{m+n} \{ I_{m+n}[(m+n)a] + I_{|m-n|}[(m+n)a] \},$$

$$b_m = (-1)^m a \{ I_{m+1}(ma) + I_{m-1}(ma) \}, \qquad [2.10]$$

and it is noted that $b_0 = 0$. The linear Eqs. [2.7] may be written in matrix form

$$\vec{Sc} = \vec{b}, \qquad [2.11]$$

with the elements of the matrix, S, and the column vector, $\vec{b}$, given by Eq. [2.10].

With these definitions the quantity M of Eq. [2.6] may be expressed as

$$M = \frac{\pi}{2}\{a^2 - \vec{c}'\vec{b}\} > 0, \qquad [2.12]$$

and the root-mean-square deviation of the potential on the boundary from zero for a given partial sum of Eq. [2.4] is

$$\text{RMS} = \sqrt{\frac{M}{\pi}}. \qquad [2.13]$$

This gives a measure of the degree of convergence at any stage as N is increased. Also any irregularities in the trend of M or RMS (both should be monotone decreasing) would be an indication of difficulties in the numerical solution. The matrix S is positive definite so that no pivoting is required in the solution of Eq. [2.11].[4]

The matrix coefficients of S as given by Eq. [2.10] cover a very large range for even modest values of the deformation parameter (a) and degree of approximation (N). Values of the product ($2Na$) as large as one hundred are certainly to be expected. Therefore, it may be useful to introduce a scaling into the system of linear Eqs. [2.11] so that the range of coefficients is reduced, and further to make their computation more consistent with computer programs for the modified Bessel functions [$I_n(z)$]. This is accomplished by introducing the diagonal matrix

$$D = \text{Diag}\,[(-1)^n e^{-na}], \qquad [2.14]$$

whose off-diagonal elements are zero. Premultiplying Eq. [2.11] by D and introducing the transformation

$$\vec{c_1} = D^{-1}\vec{c}, \qquad [2.15]$$

the transformed system

$$T\vec{c_1} = \vec{b_1}, \qquad [2.16]$$

is obtained wherein

$$T_{mn} = e^{-(m+n)a}\{I_{m+n}[(m+n)a] + I_{|m-n|}[(m+n)a]\},$$

$$b_{1m} = a\, e^{-ma}\{I_{m+1}(ma) + I_{m-1}(ma)\}. \qquad [2.17]$$

It may be verified that T is also positive definite and that the expression for the squared error Eq. [2.12] remains valid in the transformed variables, i.e., that

$$M = \frac{\pi}{2}\{a^2 - \vec{c}_1' \vec{b}_1\}. \qquad [2.18]$$

The expression for the potential function Eq. [2.4] in terms of the new variables is given by

$$\varphi = y + \sum_{n=0}^{N} (-1)^n C_{1n} e^{-n(y+a)} \cos(nx), \qquad [2.19]$$

where the coefficients C_{1n} are defined through

$$\vec{c}_1 = (C_{10}, C_{11}, \ldots, C_{1N})'. \qquad [2.20]$$

These new coefficients offer a certain convenience in judging computational results since the absolute value of their multipliers in the region of interest never exceeds unity (as exhibited in Eq. [2.19]).

For the boundary conditions shown in Fig. 1, the asymptotic value of electric field is unity. The results of this section may be scaled up by a multiplicative factor when a different value of asymptotic field is appropriate.

2.2 Surface-Charge Density

In relating the results obtained here to those to be obtained in a more general context in Section 3, it is useful to obtain expressions for the projected charge density function. That is, the charge density along the conducting surface C_1 (Fig. 1) with respect to a distance variable projected onto the x axis.

The charge density along the conducting surface C_1 is obtained through

$$\sigma' = \nabla\varphi \cdot \hat{n} \,|_{y=a\cos(x)}, \qquad [2.21]$$

where $\hat{n}$ is a unit vector normal to the surface (outward directed) and $\nabla\varphi$ is the gradient of the potential function. The unit normal vector is given by

$$\hat{n} = -\frac{\hat{i}\, a \sin(x) + \hat{j}}{\sqrt{1 + a^2 \sin^2(x)}}, \qquad [2.22]$$

wherein $\hat{i}$ and $\hat{j}$ are unit vectors in the coordinate directions. Choosing the potential on the flat electrode C_2 as $E_o d$, it follows that the asymptotic field is equal to $-E_o\hat{j}$ and we obtain from Eq. [2.19]

$$\frac{\nabla\varphi}{E_o} = \hat{j} - \sum_{n=0}^{N}(-1)^n n C_{1n} e^{-n(y+a)} \left[\hat{i}\sin(nx) + \hat{j}\cos(nx)\right]. \qquad [2.23]$$

When the scalar product of these two vector quantities is taken and the result evaluated on the boundary C_1, one obtains the desired projected charge density function

$$\sigma = \sqrt{1 + a^2 \sin^2(x)}\,\sigma',$$

or

$$\frac{\sigma}{\sigma_0} = 1 - \sum_{n=0}^{N}(-1)^n n\, C_{1n}\, e^{-na(1+\cos(x))}\left\{\cos(nx) + \frac{a}{2}\left[\cos(n-1)x - \cos(n+1)x\right]\right\}. \qquad [2.24]$$

Here, $\sigma_0 = -E_o$. Again use must be made of the Fourier expansion of the exponential function given by Eq. [2.9], and after a certain amount of manipulation one obtains,

$$\frac{\sigma}{\sigma_0} = 1 - \sum_{n=1}^{N}\sum_{l=0}^{\infty} E_{nl}\left\{\cos(l+n)x + \cos(l-n)x + \frac{a}{2}\left[\cos(l+n-1)x + \cos(l-n+1)x - \cos(l+n+1)x - \cos(l-n-1)x\right]\right\}, \qquad [2.25]$$

where

$$E_{nl} = \frac{\epsilon_l}{2} (-1)^{l+n} n C_{1n} e^{-na} I_l(na),$$

$$\epsilon_o = 1, \qquad [2.26]$$

$$\epsilon_l = 2, \; l \neq 0.$$

This expansion can be related to a final Fourier series expansion of the form

$$\sigma = \sigma_0 \sum_{m=0}^{N} D_m \cos(mx). \qquad [2.27]$$

While further analytic reductions are possible to put Eq. [2.25] directly in the form of Eq. [2.27], there is actually little motivation to do this since the D_m can be formed quite directly from the E_{nl} in a simple computer program segment for this purpose. The computer program designed to carry out the computations of this section is described in the Appendix.

2.3 Numerical Results

The major issues connected with the computations carried out from the results of this section are accuracy and convergence. The matrix T of Eq. [2.16], while positive definite for all N, will become very poorly conditioned for large values of N. The only remedy when such large values of N are required is to carry out the computations in extended precision. Otherwise, one must be content with parameter values for which the loss of precision is not a limiting consideration.

For a given amplitude of deformation of the surface C_1, i.e., given value of a, the value of N must be increased until convergence has been obtained. This will be indicated by convergence of the coefficients, C_{1n}, as well as a suitable decrease of the RMS error given by Eqs. [2.13] and [2.18]. The onset of numerical accuracy problems may be indicated by irregular behavior of the RMS error.

The indications are that the procedures described in this section provide an accurate computation procedure for deformation amplitudes in the range from zero to about 0.5, while useful results can be obtained up to an amplitude of about unity. At an amplitude of unity numerical inaccuracies become sufficiently limiting that useful results can no longer be obtained without extending the precision beyond the double precision used in the program (14 hexadecimal digits).

Fig. 2 exhibits some results obtained through the use of the computer program of the Appendix. In each case we exhibit the deformation amplitude a and the number of terms N used in the expansion for each case treated. This is followed by the coefficients of the Fourier expansion of potential (C_{1n}) from Eq. [2.19]. These are the coefficients that minimize the RMS error for the number of terms used and the resulting RMS error is also shown. Finally, the corresponding coefficients for the Fourier expansion D_m of the projected charge density function of Eqs. [2.25] through [2.27] are exhibited. Results are shown for $a = 0.001$, 0.01, 0.1 for $N = 1,2,3,4$; and for $a = 0.5$ for $N = 1,2,3,4,8,16,32$.

It is observed from the computations that the RMS error is given approximately by

$$\text{RMS} = \frac{1}{3} a^{-(N+1)}, \qquad [2.28]$$

and this may be used as a guide for the appropriate value of N for a given amplitude in the range from zero to 0.5. Values of the RMS error less than about 10^{-8} will not be observed due to the finite length of the number used in the computations. When an RMS error of zero is indicated, it means only that the error is less than this threshold.

From the results of Section 3, an expansion of Fourier coefficients of the projected charge density function may be obtained in powers of a. These are as follows:

$$\begin{aligned} D_0 &= 1.0 \text{ (exactly)}, \\ D_1 &= a - \frac{1}{4} a^3 + \frac{11}{96} a^5 + \cdots, \\ D_2 &= \frac{1}{12} a^4 + \cdots, \\ D_3 &= \frac{1}{64} a^5 + \cdots. \end{aligned} \qquad [2.29]$$

The validity of these expansions is confirmed by the results shown in Fig. 2 as well as additional computations carried out but not shown here.

In summary, the computer program of the Appendix, based on

```
A= .100000E-02   N=    1
THE      2 POTENTIAL COEFFICIENTS ARE
-.500000E-06 .100100E-02
RMS= .353553E-06
THE      2 PROJECTED CHARGE DENSITY COEFFICIENTS ARE
 .100000E+01 .100000E-02

A= .100000E-02   N=    2
THE      3 POTENTIAL COEFFICIENTS ARE
-.500000E-06 .100100E-02-.501000E-06
RMS= .265149E-09
THE      3 PROJECTED CHARGE DENSITY COEFFICIENTS ARE
 .100000E+01 .100000E-02-.666666E-12

A= .100000E-02   N=    3
THE      4 POTENTIAL COEFFICIENTS ARE
-.500000E-06 .100100E-02-.501001E-06 .376126E-09
RMS= .000000E+00
THE      4 PROJECTED CHARGE DENSITY COEFFICIENTS ARE
 .100000E+01 .100000E-02 .833326E-13-.151562E-14

A= .100000E-02   N=    4
THE      5 POTENTIAL COEFFICIENTS ARE
-.500000E-06 .100100E-02-.501001E-06 .376127E-09-.334668E-12
RMS= .000000E+00
THE      5 PROJECTED CHARGE DENSITY COEFFICIENTS ARE
 .100000E+01 .100000E-02 .833333E-13-.156263E-16-.266207E-17

A= .100000E-01   N=    1
THE      2 POTENTIAL COEFFICIENTS ARE
-.499975E-04 .100999E-01
RMS= .353543E-04
THE      2 PROJECTED CHARGE DENSITY COEFFICIENTS ARE
 .100000E+01 .999950E-02

A= .100000E-01   N=    2
THE      3 POTENTIAL COEFFICIENTS ARE
-.499967E-04 .101006E-01-.510026E-04
RMS= .263147E-06
THE      3 PROJECTED CHARGE DENSITY COEFFICIENTS ARE
 .100000E+01 .999975E-02-.666585E-08

A= .100000E-01   N=    3
THE      4 POTENTIAL COEFFICIENTS ARE
-.499988E-04 .101006E-01-.510122E-04 .386326E-06
RMS= .235903E-08
THE      4 PROJECTED CHARGE DENSITY COEFFICIENTS ARE
 .100000E+01 .999975E-02 .832599E-09-.151530E-09

A= .100000E-01   N=    4
THE      5 POTENTIAL COEFFICIENTS ARE
-.499988E-04 .101006E-01-.510122E-04 .386446E-06-.346617E-08
RMS= .000000E+00
THE      5 PROJECTED CHARGE DENSITY COEFFICIENTS ARE
 .100000E+01 .999975E-02 .833256E-09-.156053E-11-.260121E-11

A= .100000E+00   N=    1
THE      2 POTENTIAL COEFFICIENTS ARE
-.497514E-02 .109830E+00
RMS= .352490E-02
THE      2 PROJECTED CHARGE DENSITY COEFFICIENTS ARE
 .100000E+01 .995028E-01

A= .100000E+00   N=    2
THE      3 POTENTIAL COEFFICIENTS ARE
-.498749E-02 .110649E+00-.601884E-02
RMS= .263407E-03
THE      3 PROJECTED CHARGE DENSITY COEFFICIENTS ARE
 .100000E+01 .997498E-01-.658618E-04

A= .100000E+00   N=    3
THE      4 POTENTIAL COEFFICIENTS ARE
-.498756E-02 .110656E+00-.613079E-02 .494045E-03
RMS= .233096E-04
THE      4 PROJECTED CHARGE DENSITY COEFFICIENTS ARE
 .100000E+01 .997511E-01 .761294E-05-.148402E-04
```

Fig. 2—Example of computed results. (Contd. next page)

```
A= .100000E+00   N=    4
THE      5 POTENTIAL COEFFICIENTS ARE
-.498756E-02 .110656E+00-.613247E-02 .509283E-03-.480379E-04
RMS= .226513E-05
THE      5 PROJECTED CHARGE DENSITY COEFFICIENTS ARE
 .100000E+01 .997511E-01 .825952E-05-.331677E-06-.251677E-05

A= .500000E+00   N=    1
THE      2 POTENTIAL COEFFICIENTS ARE
-.111324E+00 .711696E+00
RMS= .623988E-01
THE      2 PROJECTED CHARGE DENSITY COEFFICIENTS ARE
 .100000E+01 .445296E+00

A= .500000E+00   N=    2
THE      3 POTENTIAL COEFFICIENTS ARE
-.117182E+00 .826215E+00-.241389E+00
RMS= .284140E-01
THE      3 PROJECTED CHARGE DENSITY COEFFICIENTS ARE
 .100000E+01 .468730E+00-.314508E-01

A= .500000E+00   N=    3
THE      4 POTENTIAL COEFFICIENTS ARE
-.117649E+00 .846874E+00-.335751E+00 .119113E+00
RMS= .114127E-01
THE      4 PROJECTED CHARGE DENSITY COEFFICIENTS ARE
 .100000E+01 .471394E+00-.220364E-02-.291284E-01

A= .500000E+00   N=    4
THE      5 POTENTIAL COEFFICIENTS ARE
-.117952E+00 .851044E+00-.364753E+00 .195283E+00-.688653E-01
RMS= .498466E-02
THE      5 PROJECTED CHARGE DENSITY COEFFICIENTS ARE
 .100000E+01 .471810E+00 .298085E-02-.748745E-02-.187079E-01

A= .500000E+00   N=    8
THE      9 POTENTIAL COEFFICIENTS ARE
-.117977E+00 .852239E+00-.376359E+00 .246986E+00-.168846E+00
 .146737E+00-.104857E+00 .542418E-01-.144315E-01
RMS= .270840E-03
THE      9 PROJECTED CHARGE DENSITY COEFFICIENTS ARE
 .100000E+01 .471908E+00 .430615E-02-.380587E-03-.129242E-03
-.485347E-03-.109635E-02-.147679E-02-.544044E-03

A= .500000E+00   N=   16
THE     17 POTENTIAL COEFFICIENTS ARE
-.117977E+00 .852243E+00-.376437E+00 .247698E+00-.192990E+00
 .165142E+00-.149972E+00 .141777E+00-.137484E+00 .134369E+00
-.128755E+00 .115989E+00-.928553E-01 .616129E-01-.309942E-01
 .103137E-01-.168086E-02
RMS= .165273E-05
THE     17 PROJECTED CHARGE DENSITY COEFFICIENTS ARE
 .100000E+01 .471908E+00 .431055E-02-.349284E-03 .176515E-04
-.529326E-06-.169137E-06-.559047E-06-.161127E-05-.387588E-05
-.759479E-05-.114950E-04-.118492E-04-.475792E-05 .688155E-05
 .102800E-04-.176684E-05

A= .500000E+00   N=   32
THE     33 POTENTIAL COEFFICIENTS ARE
-.117977E+00 .852243E+00-.376437E+00 .247698E+00-.192991E+00
 .165149E+00-.150020E+00 .142036E+00-.138628E+00 .138485E+00
-.140910E+00 .145530E+00-.152167E+00 .160773E+00-.171370E+00
 .184015E+00-.196592E+00 .214389E+00-.229244E+00 .238431E+00
-.234086E+00 .206800E+00-.150585E+00 .697988E-01 .173342E-01
-.845495E-01 .112095E+00-.995688E-01 .652532E-01-.315631E-01
 .107690E-01-.232758E-02 .240514E-03
RMS= .790253E-08
THE     33 PROJECTED CHARGE DENSITY COEFFICIENTS ARE
 .100000E+01 .471908E+00 .431055E-02-.349283E-03 .176601E-04
-.488208E-06-.420608E-08 .121422E-06-.528143E-10 .318332E-10
 .824756E-10 .199763E-09 .433257E-09 .831052E-09 .137825E-08
 .188613E-08 .188231E-08 .659875E-09-.229393E-06-.645851E-08
-.959388E-08-.842504E-08-.150331E-08 .742789E-08 .102305E-07
 .230311E-08-.888810E-08-.864104E-08 .411490E-08 .110349E-07
-.746866E-09-.114900E-07 .123560E-09
```

Fig. 2 (Contd.)—Example of computed results.

the results of this section, furnishes a useful tool for the determination of potentials present in the configuration of Fig. 1 for deformation amplitudes up to about 0.5. Eq. [2.23] furnishes a basis for determination of electric fields which may be useful to obtain electron trajectories in such an environment.

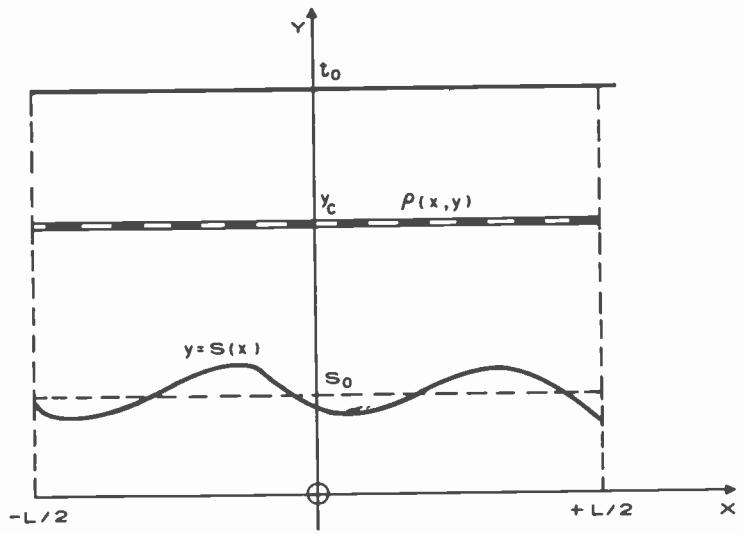

Fig. 3—Planar capacitor with lower surface deformed (bar with dashes indicates flat layer containing free charges).

3. Capacitor with Periodically Deformed Surface Including Free Charges

3.1 Formal Solution by Green's Function

The electrostatic field in a deformable mirror light valve is generally that of a planar capacitor containing a spatially varying charge distribution and having at least one surface periodically deformed (Fig. 3). The surface profiles are assumed to be z-independent and are described, respectively, by the functions

$$y = s(x) = s_o + \delta s(x) = \sum_q e^{iqx} s_q, \qquad [3.1]$$

and

$$y = t_o.$$

For simplicity, the electrical charges are confined to an internal flat plane;

$$\rho(x,y) = \sum_p e^{ipx}\rho_p \delta(y - y_c), \qquad [3.2]$$

$$\rho_p = \frac{1}{L}\int_{-L/2}^{L/2} dx e^{-ipx} \int dy\, \rho(x,y). \qquad [3.3]$$

The basic interval L is always considered as very large compared to the capacitor thickness ($t_o - s_o \equiv d \ll L$). In general, one wants to know the potential within the capacitor under the condition that the upper and lower surface have given constant potentials, φ_t and φ_s, respectively.

Since the system is assumed to extend uniformly in the z-direction it is sufficient to solve Poisson's equation in two dimensions. Under the simplifying assumption that the presence of polarizable matter in the interior of the capacitor can be disregarded, we have

$$\Delta\varphi(r) = -\rho(r), \quad r = (x,y). \qquad [3.4]$$

The most general solution of this equation is given by

$$\varphi(r_o) = \varphi^{fc}(r_o) + \varphi^{sc}(r_o) + \varphi^{sd}(r_o), \; r_o = (x_o,y_o), \qquad [3.5]$$

with[5]

$$\varphi^{fc}(r_o) = \int dx \int dy\, \rho(x,y)\, g(r,r_o), \qquad [3.6]$$

$$\varphi^{sc}(r_o) = \int_{\mathcal{L}} dl \frac{\partial\varphi}{\partial n} g(r,r_o), \qquad [3.7]$$

and

$$\varphi^{sd}(r_o) = -\int_{\mathcal{L}} dl\, \varphi(r) \frac{\partial}{\partial n} g(r,r_o). \qquad [3.8]$$

Here,

$$g(r,r_o) = \frac{-1}{4\pi} \ln [(x - x_o)^2 + (y - y_o)^2], \qquad [3.9]$$

is the appropriate Green's function (r_o being an observer's point in the interior, r being any different point in the interior or on the surface). In Eqs. [3.7] and [3.8], dl denotes a line element of the surface contour $\mathcal{L}$ and $\partial/\partial n$ denotes differentiation along the outward surface normal.

In Eq. [3.5] the potential is represented by superposition of three terms that are simple to interpret. The first term φ^{fc}, Eq. [3.6], is due to the presence of free charges in the interior. The conducting boundaries with externally applied potentials involve boundary conditions that can be uniquely satisfied by the second and third term in Eq. [3.5] (Dirichlet problem). The second term φ^{sc} is the potential due to a surface charge density $\sigma' = \partial\varphi/\partial n$, whereas the contribution of the third term has the form of the potential due to a surface dipole layer with dipole moment density $\vec{D} = -\varphi\hat{n}$.[5]

Carrying out the integrations in Eq. [3.6] we write

$$\varphi^{fc}(r_o) = \frac{1}{2} \sum_k \rho_k G_k(x_o, y_c - y_o), \qquad [3.10]$$

where the integral over x

$$G_k(x_o,a) \equiv -\frac{1}{2\pi} \int dx\, e^{ikx} \ln [(x - x_o)^2 + a^2], \qquad [3.11a]$$

exists only if restricted to a finite interval, which later can be extended to infinity. Choosing this interval as ranging from $-L/2$ to $+L/2$ we obtain

$$G_k(x_o,a) = \frac{1}{|k|} \left[e^{-|k||a|} e^{ikx_o} - \frac{2}{\pi} \sin\left(|k|\frac{L}{2}\right) \ln \frac{L}{2} + \frac{2}{\pi} \mathrm{si}\left(|k|\frac{L}{2}\right) e^{ikx_o} \right] + 0\left(\frac{1}{L}\right). \qquad [3.11b]$$

Here, the second term behaves like Dirac's delta function and can be

dropped for non-zero values of k. For large values of L, Eq. [3.11b] reduces to

$$G_k(x_o,a) = \begin{cases} \dfrac{L}{\pi}\left(1 - \ln\dfrac{L}{2}\right) - |a|, & k = 0, \\ \dfrac{1}{|k|}\, e^{-|k||a|} e^{ikx_o}, & k \neq 0\,. \end{cases} \qquad [3.11c]$$

Using these expressions we put the free charge potential into the form

$$\varphi^{fc}(r_o) = \frac{1}{2\pi}\rho_o L\left(1 - \ln\frac{L}{2}\right) - \frac{1}{2}\rho_o\,|y_o - y_c| + \frac{1}{2}\sum_{k\neq 0}\rho_k \frac{1}{|k|}\, e^{-|k||y_o - y_c|} e^{ikx_o}\,. \qquad [3.12]$$

The singular behavior of the $k = 0$ term is compensated for by other terms to be considered later. The electric field related to the potential of Eq. [3.12] is independent of L.

The second term in Eq. [3.5] is a contour integral containing the derivative of the potential, which is not known yet. This quantity is conveniently expressed in terms of unknown surface charges, which afterwards have to be determined from the boundary conditions. To convert the contour integral into an integral over the variable x, which in the following is always taken from $-L/2$ to $L/2$, we define

$$\sqrt{1 + s'(x)^2}\,\frac{\partial\varphi}{\partial n}\bigg|_{y=s(x)} \equiv \sigma(x) = \sum_k e^{ikx}\sigma_k\,, \qquad [3.13]$$

and

$$\frac{\partial\varphi}{\partial n}\bigg|_{y=t_o} \equiv \tau(x) = \sum_k e^{ikx}\tau_k\,, \qquad [3.14]$$

where $\sigma(x)$ is a "projected" surface charge density. Using these Fourier series, we write Eq. [3.7] in the form

$$\varphi^{sc}(r_o) = \frac{1}{2}\sum_k \sigma_k \left(-\frac{1}{2\pi}\right)\int dx\, e^{ikx}\ln[(x-x_o)^2 + (s(x)-y_o)^2]$$

$$+\frac{1}{2}\sum_k \tau_k\, G_k(x_o, t_o - y_o). \qquad [3.15]$$

The term arising from the deformed surface is in general difficult to evaluate. Since, however, it has the same periodicity with respect to x_o as the deformation $\delta s(x)$, it can be further transformed by using the Fourier series expansion

$$-\frac{1}{2\pi}\int dx\, e^{ikx} \ln\,[(x-x_o)^2 + (s(x)-y_o)^2] = \left\{\frac{L}{\pi}\left(1 - \ln\frac{L}{2}\right)\right.$$

$$\left. - (y_o - s_o)\right\}\delta_{k,o} + e^{ikx_o}\frac{1}{|k|}\, e^{-|k|(y_o - s_o)}(1-\delta_{k,o})$$

$$+\sum_p e^{ipx_o}\, e^{-|p|(y_o - s_o)}\, S^{+}_{p-k,|p|}\,. \qquad [3.16]$$

Here, we have defined

$$S^{\pm}_{p-k,|p|} \equiv \frac{1}{L}\int_{-L/2}^{L/2} dx\, e^{-i(p-k)x}\int_0^{\pm\delta s(x)} d\xi\, e^{|p|\xi}\,. \qquad [3.17]$$

In the flat case, this integral vanishes and Eq. [3.16] reduces to Eq. [3.11c]. Eq. [3.16] is straightforward to derive under the condition that $y_o > \text{Max}\ \{s(x)\}$. In this regime it defines an analytic function, which by continuation also represents the potential at all other points above the electrode.

Under the assumption that the values of the potential on the upper and lower surface are constant, the third term in Eq. [3.5] is independent of deformations and is generally given by

$$\varphi^{sd}(r_o) = \frac{1}{2}\,(\varphi_s + \varphi_t). \qquad [3.18]$$

Added to the Eqs. [3.12] and [3.15] this quantity completes the expression for the potential.

The L-dependent divergent terms cancel from the total potential if the system is electrically neutral, i.e.,

$$\sigma_o + \tau_o + \rho_o = 0. \qquad [3.19]$$

With this requirement the potential is given by the relation

$$\begin{aligned} 2q(r_o) = {} & \varphi_s + \varphi_t + \sigma_o\{(t_o - y_o) - (y_o - s_o)\} \\ & + \rho_o\{(t_o - y_o) - |y_c - y_o|\} \\ & + \sum_{k\neq 0} \frac{1}{|k|} e^{ikx_o}\{\sigma_k e^{-|k|(y_o - s_o)} + \tau_k e^{-|k|(t_o - y_o)} \\ & + \rho_k e^{-|k||y_c - y_o|}\} + \sum_{k,q} \sigma_k e^{iqx_o} e^{-|q|(y_o - s_o)} S^{+}_{q-k,|q|}\,. \end{aligned} \qquad [3.20]$$

Here, only the last term depends explicitly on the deformations. If the free charges are dropped from this expression it has the general form of the potential function in Eq. [2.1].

3.2 Boundary Conditions

The requirements that the potential should have constant values on the upper and lower surfaces is equivalent to the following equations for the Fourier transforms of the potential along the surfaces

$$\frac{1}{L}\int dx_o\, e^{-ipx_o}\varphi(x_o, y_o = s(x_o)) = \varphi_s\,\delta_{p,o}\,, \qquad [3.21]$$

and

$$\frac{1}{L}\int dx_o\, e^{-ipx_o}\varphi(x_o, y_o = t_o) = \varphi_t\,\delta_{p,o}\,. \qquad [3.22]$$

Explicitly written, these two conditions represent a system of linear inhomogeneous equations for the surface charge components σ_k and τ_k, respectively.

Because of the flatness of the upper electrode, Eq. [3.22] is the easier one to evaluate. For $p = 0$ it leads to

$$\sigma_o - \frac{1}{d}\sum_{k\neq 0} \sigma_k s_{-k} = -E_o - \rho_o \frac{t_o - y_c}{d}, \qquad [3.23]$$

wherein $E_o \equiv (\varphi_t - \varphi_s)/d$ is the constant field present in the case of no free charges and of no deformations. For non-zero wavenumber, $p \neq 0$, Eq. [3.22] reduces to

$$e^{-|p|d}\sum_k (\delta_{p,k} + |p|\, S^+_{p-k,|p|})\sigma_k + \tau_p = -\rho_p\, e^{-|p|(t_o - y_c)}. \qquad [3.24]$$

The boundary condition for the deformed electrode, Eq. [3.21], gives rise to the equations

$$(p = 0)$$

$$\sigma_o + \frac{1}{d}\sum_k L_{o,k}\sigma_k + \frac{1}{d}\sum_k e^{-|k|d}\, S^+_{-k,|k|}\tau_k = \qquad [3.25]$$

$$-E_o - \rho_o \frac{t_o - y_c}{d} - \frac{1}{d}\sum_k e^{-|k|(y_c - s_o)}\, S^+_{-k,|k|}\rho_k,$$

and

$$(p \neq 0)$$

$$\sum_k (\delta_{p,k} + |p| L_{p,k})\sigma_k \qquad [3.26]$$

$$+ \sum_k (\delta_{p,k} + |p| S^+_{p-k,|k|})(e^{-|k|d}\tau_k + e^{-|k|(y_c - s_o)}\rho_k) = 0.$$

In these equations, the coefficients $L_{p,k}$ are defined as

$$L_{p,k} \equiv \frac{-1}{2\pi L}\int dx_o \int dx\, e^{-ipx_o} \ln\left[1 + \left(\frac{s(x) - s(x_o)}{x - x_o}\right)^2\right],$$

$$= S^+_{p-k,|p|} + S^-_{p-k,|k|} + \sum_q |q| S^-_{p-q,|q|}\, S^+_{q-k,|q|}. \qquad [3.27]$$

On the basis of the Eqs. [3.23] to [3.27], the calculation of the potential may be performed using standard numerical methods. In the following a few simple and approximate results are discussed.

3.3 Perturbation Expansion for Weak Deformations

The equations for the surface charge components σ_k and τ_k contain coefficients that require the quantitative evaluation of (surface) integrals. In cases where the deformations represent weak perturbations, these integrals may be expanded in terms of the surface Fourier components s_q. Effects of low order in s_q can be studied by using in the Eqs. [3.23] to [3.26] the following series expansions:

$$S^{\pm}{}_{p,|k|} = \pm s_p(1-\delta_{p,o}) + \frac{|k|}{2}\sum_{q_1,q_2\neq o}\delta_{p,q_1+q_2}\, s_{q_1}s_{q_2}$$

$$\pm\frac{|k|^2}{6}\sum_{q_1q_2q_3\neq o}\delta_{p,q_1+q_2+q_3}\, s_{q_1}s_{q_2}s_{q_3}+\cdots, \qquad [3.28]$$

and

$$L_{p,k} = \frac{1}{2}\sum_{q,q'\neq 0} s_q s_{q'}\delta_{p,k+q+q'}\{|k+q+q'| - 2|k+q| + |k|\}$$

$$+\frac{1}{24}\sum_{\substack{q_1q_2q_3q_4\\ \neq 0}} s_{q_1}s_{q_2}s_{q_3}s_{q_4}\delta_{p,k+q_1+q_2+q_3+q_4}\{|k+q_1+q_2+q_3+q_4|$$

$$-4|k+q_1+q_2+q_3| + 6|k+q_1+q_2|$$

$$-4|k+q_1| + |k|\} + \cdots . \qquad [3.29]$$

The assumption of weak deformations, i.e., $|qs_q| \ll 1$, seems to be justified in the case of the elastomer type light valves of Ref. (2).

3.4 The Single Surface Without Free Charges

The set of Eqs. [3.23] to [3.26] and its solution are in general fairly involved. In order to obtain some insight and partial results we consider the simple situation of no free charges, $\rho_k = 0$. Furthermore, we move the flat electrode to infinity, $t_o \to \infty$, $d \to \infty$. This case represents a single deformed surface subject to an external homogeneous field E_o, directed towards the electrode. Under these circumstances one is left with the simplified set of equations

$$\sigma_o = -E_o, \quad \tau_o = -\sigma_o, \qquad [3.30]$$

and, for $p \neq 0$,

$$\tau_p = 0, \qquad [3.31]$$

$$\sigma_p = |p| s_p \sigma_o - |p| \sum_k L_{p,k} \sigma_k. \qquad [3.32]$$

For vanishing deformations, $L_{p,k} = 0$, it follows that $\sigma_p = 0$ $(p \neq 0)$.

Eq. [3.32] is written in a form so that for weak deformations the surface charge components can be obtained by iteration. Choosing the sinusoidal surface of Eq. [2.2] $\delta s(x) = a \cos(q_o x)$, $(q_o = 1)$, and identifying

$$D_n = \sigma_{nq_o} + \sigma_{-nq_o}, \qquad n \geq 1, \qquad [3.33]$$

one derives, with Eq. [3.29], the power expansions of Eq. [2.29].

Up to second order in the deformations, the potential is given by

$$\begin{aligned} \varphi(r_o) = {} & \varphi_s - \sigma_o (y_o - s_o) \\ & + \sigma_o \sum_{k \neq 0} e^{ikx_o} e^{-|k|(y_o - s_o)} s_k \\ & + \sigma_o \sum_k e^{ikx_o} e^{-|k|(y_o - s_o)} \sum_{q,q' \neq 0} \delta_{k,q+q'} |q| s_q s_{q'}. \end{aligned} \qquad [3.34]$$

From this expression the electrostatic energy of the field in the capacitor follows as

$$U = \frac{1}{2} \int_{-L/2}^{L/2} dx \int_{s(x)}^{\infty} dy \left[\left(\frac{\partial \varphi}{\partial x} \right)^2 + \left(\frac{\partial \varphi}{\partial y} \right)^2 \right]. \qquad [3.35]$$

Up to second order in s_q we find, apart from an additive constant, that

$$\delta U = -L E_o^2 \sum_q |q| s_q s_{-q}. \qquad [3.36]$$

The negative sign of this potential energy expression indicates that the surface of a condenser is in general unstable if no other forces, e.g., mechanical forces, are involved. The potential energy represented by Eq. [3.36] is the basic quanity for an analysis of the dynamics of mirror surfaces in light values as described in Ref. (2).

4. Summary

The present analysis of the electrostatic field near deformed surfaces is based on Fourier series expansions of the potential and of the surface charge densities. Using such expansions one can reduce the calculations of the potential to the solution of linear equations. The procedure described here is useful if the number of equations may be kept low and if the coefficients don't form an ill-conditioned matrix. The numerical results, which have been obtained for a sinusoidal shape, demonstrate that these requirements are met for small deformations.

Appendix—A Computer Program for Carrying Out Computations Developed in Section 2

Fig. 4 shows a printout of a program designed to carry out the computations indicated in Section 2. The language used is a dialogue of FORTRAN (FORTRAN PI) designed for use with the NTSS time sharing system in use at RCA Laboratories. Double precision (14 hexadecimal digits) has been used throughout.

The program has been modularized with a number of often used functions performed in subroutines. The first such subroutine, MBESN, computes a sequence of scaled modified Bessel functions of orders zero through N for a given real argument. In the program, this subroutine is fully documented with comment cards. The second subroutine, LUD, performs the factorization of a given matrix A into the product of two matrices which are respectively lower triangular and upper triangular. Pivoting is not used since it is presumed that A is positive definite. Finally, a third subroutine, BAKSUB, makes use of this factored form to solve a given system of linear equations.

These are followed by a main program which calls these subroutines to set up the matrix T in accordance with Eq. [2.17] and solve the resulting system for the coefficients (C_{1n}) of Eq. [2.19]. This is followed by a calculation of the RMS deviation, and then by a program segment which calculates the coefficients D_m of the Fourier expansion of the projected charge density function.

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[3] M. Abramowitz and I. A. Stegun, **Handbook of Mathematical Functions**, Eq. (9.6.34), p. 376, U.S. Department of Commerce, National Bureau of Standards, Applied Mathematics Series 55, 1964.

[4] George Forsythe and Cleve B. Moler, **Computer Solution of Linear Algebraic Systems**, Prentice-Hall, Englewood Cliffs, N. J. 1967, p. 119 (Exercise 23.15).

[5] J. D. Jackson, **Classical Electrodynamics**, John Wiley and Sons, Inc., New York, 1962, Chap. 1.

Fig. 4—Program listing.

```
ALLOCATE 4,6,1,1,12
      SUBROUTINE MBESN(X,B,NN)
C ***************************************************************
C
C     SUBROUTINE MBESN
C
C     PURPOSE
C         COMPUTES SCALED MODIFIED BESSEL FUNCTIONS OF THE FIRST
C         KIND OF ORDERS ZERO THROUGH N FOR A GIVEN ARGUMENT X,
C         I.E., EXP(-ABS(X))IN(X).
C
C     USAGE
C         CALL MBESN(X,B,NN)
C
C     DESCRIPTION
C           X - THE GIVEN ARGUMENT OF EXP(-ABS(X))IN(X).
C           B - AN ARRAY CONTAINING IN B(1) THROUGH B(N+1) THE
C               RESULTANT SCALED MODIFIED BESSEL FUNCTIONS
C               EXP(-ABS(X))IO(X) THROUGH EXP(-ABS(X))IN(X).
C          NN - AN INTEGER SPECIFYING THE HIGHEST ORDER SCALED
C               MODIFIED BESSEL FUNCTION DESIRED.
C
C     REMARKS
C         1.  THE ARGUMENT VALUE X MAY BE ANY REAL NUMBER AND
C             REMAINS UNCHANGED BY THE SUBROUTINE.
C         2.  THE ARGUMENT AND RESULTANT FUNCTION VALUES ARE
C             DOUBLE PRECISION.
C         3.  A VALID SINGLE PRECISION SUBROUTINE RESULTS IF
C             THE REAL*8 DESIGNATIONS AT THE BEGINNING OF THE
C             PROGRAM ARE CHANGED TO REAL, I.E., THE *8 IS
C             DELETED, AND THE COMMENT DESIGNATOR ('C') IS
C             REMOVED FROM THE SIXTH EXECUTABLE STATEMENT OF
C             THE PROGRAM.
C         4.  THE ARRAY B SHOULD BE DIMENSIONED TO ACCOMMODATE
C             THE MAXIMUM NUMBER OF FUNCTION VALUES WHICH WILL
C             BE REQUESTED, I.E., NMAX+1.
C         5.  IT MAY HAPPEN THAT A USER REQUESTS A FUNCTION
C             WHICH BE OUT OF RANGE BEING TOO SMALL TO HAVE
C             A VALID FLOATING HEXADECIMAL REPRESENTATION. IN
C             THAT CASE, A PROGRAM STOP WITH AN EXPLANATORY
C             MESSAGE WILL OCCUR.  FOR EXAMPLE EXP(-1.)I50(1.)
C             OR EXP(-400.)I400(400.).
C         6.  THE FUNCTION VALUES ARE MONOTONE DECREASING AND
C             HAVE 'FULL' RELATIVE ACCURACY, I.E., WITHIN
C             ABOUT 100 UNITS IN THE LAST AVAILABLE
C             SIGNIFICANT FIGURE.  THUS, THE VALUES ARE ACCURATE
C             TO ABOUT FIFTEEN SIGNIFICANT FIGURES IN DOUBLE
C             PRECISION AND FIVE SIGNIFICANT FIGURES IN SINGLE
C             PRECISION.
C         7.  THE ACCURACY HAS BEEN VERIFIED BY COMPARISON
C             WITH VARIOUS TABLES AS WELL AS COMPARISON WITH
C             EXISTING SUBROUTINES FOR THE ZERO AND FIRST
C             ORDER FUNCTIONS (SEE SUBROUTINE MOBES).
C         8.  THE COMPUTATION OF LOW ORDER FUNCTIONS FOR
C             EXTREMELY LARGE ARGUMENTS BY THE USE OF THIS
C             SUBROUTINE MAY BE TIME CONSUMING SINCE THE
C             RECURSION MUST START AT A VALUE OF ORDER
C             GIVEN APPROXIMATELY BY 3.0*SQRT(ABS(X)).
C
C     METHOD
C         DEFINITION - IN(X) ARE THE SOLUTION FUNCTIONS OF THE
C         DIFFERNTIAL EQUATION Y'' +(1/X)Y'-(1+(N/X)**2)Y = 0
C         WHICH ARE REGULAR AT X=0 AND NORMALIZED SO THAT THEIR
C         NTH DERIVATIVE EVALUATED AT X=0 IS EQUAL TO 2**(-N).
C         THEY ARE COMPUTED THROUGH BACKWARD APPLICATION OF THE
C         RECURRENCE RELATION WHICH THEY SATISFY FOLLOWED BY AN
C         APPROPRIATE RENORMALIZATION THROUGH AN IDENTITY.
C         REFERENCE - J.C.P. MILLER, INTRODUCTION TO VOL. X, BRIT.
C         ASSOC. FOR THE ADV. OF SCI., MATH. TABLES, CAMBRIDGE
C         UNIVERSITY PRESS, 1952, P. XVI.
C
C
C
C   JAN. 18, 1973
C ***************************************************************
```

(continued)

Fig. 4—Program Listing (continued)

```
      REAL*8 B(9999),X,Z,S,S1,ZERO,ONE,TWO,EPS,BET,TEMP
      REAL*8 FAC,CEE,DEE,EI,EN,T1,T2,T3
      ZERO=0.
      ONE=1.
      TWO=2.
      EPS=1.E-38
      CEE=14.*LOG(16.)
C     CEE=6.*LOG(16.)
      DEE=-65.*LOG(16.)
      Z=ABS(X)
      N=ABS(NN)
      IF(Z.NE.ZERO) GO TO 20
      B(1)=ONE
      IF(N.EQ.0) RETURN
      DO 10 I=1,N
   10 B(I+1)=ZERO
      RETURN
   20 EN=N
      IF(Z*Z.GT.EN*EN) GO TO 55
      IF(N.GE.10) GO TO 40
      FAC=ZERO
      IF(N.LT.2) GO TO 50
      DO 30 I=2,N
      EI=I
   30 FAC=FAC+LOG(EI)
      GO TO 50
   40 FAC=(N+.5)*LOG(EN)-N+.91894+ONE/(12.*N-1.)
   50 FAC=N*(LOG(Z/TWO))-Z-FAC
      IF(FAC.LT.DEE) GO TO 170
   55 IF(TWO*LOG(TWO/Z).LT.CEE) GO TO 90
      B(1)=EXP(-Z)
      IF(N.EQ.0) RETURN
      DO 60 I=1,N
   60 B(I+1)=X*B(I)/(I+I)
      RETURN
   90 L=N
      BET=(L+1)/Z
      TEMP=EXP(CEE)
      T1=ONE
      T2=-BET-SQRT(BET*BET+ONE)
  100 T3=T1-TWO*(L+1)*T2/Z
      IF(ABS(T3).GT.TEMP) GO TO 110
      L=L+1
      T1=T2
      T2=T3
      GO TO 100
  110 T3=ZERO
      T2=EPS
      S=EPS
      S1=ZERO
  120 T1=TWO*(L+1)*T2/Z+T3
      S1=S1+T1
      IF(S1.LT.S) GO TO 130
      S=S+S1
      S1=ZERO
  130 L=L-1
      T3=T2
      T2=T1
      IF(L.GT.N-1) GO TO 120
      S=EPS*(S+S1)/T2
      NU=N+1
      B(NU)=EPS
      IF(N.EQ.0) GO TO 145
      B(N)=EPS*(TWO*(L+1)/Z+T3/T2)
      S=S+B(N)
      IF(N.EQ.1) GO TO 145
      S1=ZERO
      DO 140 I=3,NU
      II=N-I+2
      B(II)=TWO*II*B(II+1)/Z+B(II+2)
      IF(B(II).GT.ONE/EPS) GO TO 170
      S1=S1+B(II)
      IF(S1.LT.S) GO TO 140
      S=S+S1
      S1=ZERO
  140 CONTINUE
```

Fig. 4—Program Listing (continued)

```
      S=S+SI
  145 S=S+S-B(I)
      DO 150 I=1,NU
  150 B(I)=B(I)/S
      IF(X.GE.ZERO) RETURN
      DO 160 I=2,NU,2
  160 B(I)=-B(I)
      RETURN
  170 PRINT "REQUESTED FUNCTION VALUE WOULD BE OUT OF RANGE LOW"
      STOP
      END
C
      SUBROUTINE LUD(N,A)
      REAL*8 A(50,50)
C     LU DECOMPOSITION WITHOUT PIVOTING
      IF(N.EQ.1) RETURN
      NM1=N-1
      DO 10 K=1,NM1
      KP1=K+1
      DO 10 I=KP1,N
      A(I,K)=A(I,K)/A(K,K)
      DO 10 J=KP1,N
   10 A(I,J)=A(I,J)-A(I,K)*A(K,J)
      RETURN
      END
C
      SUBROUTINE BAKSUB(N,A,B)
      REAL*8 A(50,50),B(50)
      IF(N.EQ.1) GO TO 40
      DO 10 I=2,N
      IM1=I-1
      DO 10 J=1,IM1
   10 B(I)=B(I)-B(J)*A(I,J)
      B(N)=B(N)/A(N,N)
      DO 30 K=2,N
      I=N-K+1
      IP1=I+1
      DO 20 J=IP1,N
   20 B(I)=B(I)-B(J)*A(I,J)
   30 B(I)=B(I)/A(I,I)
      RETURN
   40 B(1)=B(1)/A(1,1)
      RETURN
      END
C
C     PROGRAM FOR SOLUTION OF LAPLACE'S EQUATION
      REAL*8 A,ARG,SUM,RMS,BI(50),C1(50),FC(100),T(50,50)
      REAL*8 D(50),SWN,SWL,EN,ENL
  999 READ A,NN
      PRINT
      PRINT "A=",A,"   N=",NN
      IF(NN.GT.49) STOP
      MPN=0
   10 ARG=MPN*A
      MMAX=MPN+1
      CALL MBESN(ARG,FC,MMAX)
      M=0
   20 N=MPN-M
      IF(N.GT.NN) GO TO 30
      IF(N.LT.0) GO TO 40
      MMN=ABS(M-N)
      T(M+1,N+1)=FC(MPN+1)*FC(MMN+1)
   30 M=M+1
      IF(M.LE.NN) GO TO 20
   40 IF(MPN.EQ.0) BI(1)=0.
      IF(MPN.GT.NN) GO TO 50
      IF(MPN.NE.0) BI(MPN+1)=A*(FC(MPN+2)+FC(MPN))
   50 MPN=MPN+1
      IF(MPN.LE.2*NN) GO TO 10
      NNN=NN+1
      DO 60 I=1,NNN
```

(continued)

Fig. 4—Program Listing (continued)

```
 60 C1(I)=B1(I)
    CALL LUD(NNN,T)
    CALL BAKSUB(NNN,T,C1)
    SUM=0.
    DO 70 I=1,NNN
    II=NNN-I+1
 70 SUM=SUM+C1(II)*B1(I)
    SUM=A*A-SUM
    IF(SUM.GE.0.) RMS=SQRT(SUM/2.)
    IF(SUM.LT.0.) RMS=0.
    PRINT "THE ",NNN," COEFFICIENTS ARE"
    PRINT (C1(I),I=1,NNN)
    PRINT "RMS=",RMS
    DO 200 I=1,NNN
200 D(I)=0.
    D(1)=1.
    SWN=-1.
    DO 210 N=1,NN
    ARG=N*A
    NMAX=N+NN+1
    CALL MBESN(ARG,FC,NMAX)
    EN=SWN*N*C1(N+1)
    SWN=-SWN
    SWL=1.
    DO 210 LL=1,NMAX+1
    L=LL-1
    ENL=SWL*FC(LL)*EN
    SWL=-SWL
    IF(L.EQ.0) ENL=ENL/2.
    ID=L+N+1
    IF(ID.LE.NNN) D(ID)=D(ID)-ENL
    ID=ABS(L-N)+1
    IF(ID.LE.NNN) D(ID)=D(ID)-ENL
    ID=L+N
    IF(ID.LE.NNN) D(ID)=D(ID)-A*ENL/2.
    ID=ABS(L-N+1)+1
    IF(ID.LE.NNN) D(ID)=D(ID)-A*ENL/2.
    ID=L+N+2
    IF(ID.LE.NNN) D(ID)=D(ID)+A*ENL/2.
    ID=ABS(L-N-1)+1
    IF(ID.LE.NNN) D(ID)=D(ID)+A*ENL/2.
210 CONTINUE
    PRINT "THE ",NNN," PROJECTED CHARGE DENSITY COEFFICIENTS ARE"
    PRINT (D(I),I=1,NNN)
    GO TO 999
    START 999
```

Detection and Characterization of Localized Defects in Dielectric Films*

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Abstract—Capabilities and limitations of various types of analytical methods for detecting and characterizing localized imperfections in typical dielectric films used in present-day silicon semiconductor device technology are surveyed and compared. Dielectrics and insulators of particular interest include thermally grown silicon dioxide and layers of vapor-deposited silicon dioxide, silicate glasses, silicon nitride, aluminum oxide, and complex silicates in thicknesses ranging from several hundred angstroms to several micrometers. The preparation and application of these materials are briefly surveyed, and frequently encountered defects and some of their causes are reviewed. The analytical methods discussed in some detail include optical contrast microscopy, scanning electron microscopy, self-healing dielectric breakdown, selective chemical etching, electrolytic decoration, liquid-crystal techniques, electron-probe microanalysis, and ion microprobe mass analysis. Several additional methods are briefly noted. Particular emphasis is placed on recent improvements achieved in these analytical methods. Applications are discussed and illustrated with typical examples, and trends in future developments are indicated.

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1. Introduction

Dielectric films serve many essential functions in modern solid-state-device technology, and their structural, chemical, and electrical properties are key factors for improving device reliability, performance, and product yield. It is therefore important not only to control precisely the properties of dielectric films but also to measure their quality and to determine the presence and nature of any imperfections that may give rise to device failure so that appropriate corrections can be made in the processing.

Imperfections can be classified as nonlocalized defects resulting from general film properties and as localized defects. Imperfections may take the form of structural defects in the films (such as microcracks and stress), chemical contaminants that give rise to ionic motion (such as sodium ions), changes in chemical composition from that intended (such as non-stoichiometry), or electrical problems (such as insufficient dielectric strength).

It is the purpose of this paper to compare capabilities and limitations of analytical methods suitable for examining *localized* defects in dielectric films used in silicon microelectronic technology, with particular emphasis on recently established or improved methods. The types of films, their applications in device structures and processing, and the nature and causes of imperfections are briefly surveyed before the various analytical methods are discussed.

2. Dielectric Films for Microelectronic Applications

Three main classes of dielectric films for semiconductor device applications can be distinguished: (1) single oxides, (2) silicate glasses, and (3) nitrides. Several detailed reviews are available that describe their preparation, properties, and application in microelectronics.[1-8]

The most widely used of these materials is silicon dioxide, which can be thermally grown by reacting silicon with oxygen or water vapor at typically 1000-1200°C. This stoichiometric oxide has excellent dielectric properties and can be grown at high purity.[9,10] However, sodium and other ions can diffuse through the open network structure of SiO_2, with consequent degradation of semiconductor device parameters. The quality of SiO_2 layers deposited at low temperature (300-500°C) by chemical vapor reaction of silane with oxygen[11,12] or by rf-sputtering techniques[13] is similar but not quite as good as films thermally grown on silicon subtrates;[14] nevertheless, these deposited layers are technologically of great importance.[15,16]

Another important dielectric is silicon nitride[17] prepared by chem-

ical vapor deposition from silane (or silicon tetrachloride) and ammonia at a temperature of typically 850°C. The advantage of Si_3N_4 is its masking efficiency against ionic contaminants, due to its dense structure, but the stoichiometry must be carefully controlled to assure reproducible characteristics.[14,17]

Table 1—Applications of Inorganic Dielectric Films in Semiconductor Device Technology

Permanent Device Component	Temporary Processing Component
Dielectric insulation	Solid-to-solid diffusion source
Semiconductor surface passivation and stabilization	Doping diffusion mask
High-voltage junction passivation	Chemical etch mask
Hermetic chip sealing	Etch stop layer
Device surface protection	Etch control layer for step tapering
Metal interconnection protection (mechanical and chemical)	Ionic contaminant getter
Protection against plastic encapsulant components	Metal precipitate getter
Interlevel insulation for multilayer metallization	Selective oxidation mask
Ion-diffusion barrier	Surface purification (oxidation and stripping)
Radiation protection	
Gate dielectric in MOS structures	
Capacitor element	

Doped oxides and binary silicate glasses, such as phosphosilicates and borosilicates, are very important as semiconductor diffusion sources, as protective layers, and for junction passivation and sealing in conjunction with thermal SiO_2 primary passivating layers.[1-8, 15, 16, 18-21] These glasses can be readily deposited at low temperature (300-500°C) by gas-phase reaction of the hydrides (silane, phophine, diborane, arsine, germane) with oxygen,[15,21] or by hydrolysis of the chlorides at higher temperatures.[22]

Dielectrics for more specialized semiconductor device applications include powder deposited and fused multicomponent glasses[23] (such as lead aluminoborosilicates), aluminum oxide,[5,24] and tantalum pentoxide.[6,13] Only limited use has been made to date of titanium dioxide, niobium pentoxide, hafnium dioxide, zirconium dioxide, germanium silicate, boron nitride, and germanium nitride.[5,6]

Important applications are listed briefly in Table 1. The dielectric

film may be used as a permanent structural component of a device, or it may be used temporarily as an aid during device processing. The thicknesses of these layers may range from a few hundred angstroms to several or many micrometers. The required properties of the film are dictated by the particular application for which it is intended.

3. Types of Localized Defects in Dielectric Films

Many of the defects arise from improper processing or from inherent mutual incompatibility of the films with the substrate material.

Particulate contaminants (dust or reaction products) in the gas or vapor streams or on the substrate surface during chemical vapor deposition interfere with film nucleation and proper growth, resulting in voids, thin spots, partial or complete pinholes, or hillocks. Even if particulate impurities become embedded in the film during processing, such as thermal oxidation of silicon, they may constitute a potential source of device failure due to local weakening of the dielectric breakdown strength.

Pinholes in the films can also be caused by problems in photolithographic processing if the photoresist protects the film incompletely, or if the etchants used in the chemical patterning process penetrate through pinholes or thin spots in the resist coating.

Gas bubbles that weaken the dielectric strength of an insulator often arise during fusion of deposited glass powders if the melt temperature is too low or if the particle distribution is incorrect. Unacceptable surface morphology may result in this case. Topographical defects such as excessive surface roughness may also arise during chemical vapor deposition under incorrect process conditions.

Microfractures may be caused by excessive stress between the dielectric film and the substrate or between different types of films. Stress in films may develop during growth, deposition, pattern etching or heat treatments, especially if the linear thermal expansions of the components are mismatched. Cracks may form particularly during thermal shock on the initiation of or following high-temperature processing, excessive thermal contraction or cooling, or during temperature stress cycling and life testing of devices.

Localized defects also include embedded foreign particles, microcrystallites, or precipitates caused by reaction in the solid state. Oxides and glasses may devitrify in local regions under certain conditions. Depending on the specific function for which the dielectric film was intended, such defects may deleteriously affect doping and masking during diffusion, lead to films with lowered dielectric strength, or give rise to mask failures during chemical etching.

The topography of the substrate being coated with a dielectric film may cause defects in the film deposit, such as thin spots over snarp edges or film discontinuities in corners at the base of steep steps, that may lead to electrical shorts. A survey of failure modes[25] and discussion of methods specifically designed to improve the reliability of electron devices by optimized coverage of surface topography[26] were presented recently.

4. Methods for Analyzing Localized Film Defects

Techniques for detecting and characterizing localized defects in dielectric films can be defined as optical, electrical, electronic, mechanical, and chemical, as outlined in Table 2.[27] Many of these

Table 2—Survey of Useful Methods for Detecting and Characterizing Localized Defects in Dielectric Films

Optical Methods	Brightfield, darkfield, phase-contrast microscopy Nomarski differential interference-contrast microscopy Multiple-beam interferometry Light scattering
Electrical Methods	Standard dielectric breakdown Self-healing dielectric breakdown Electrochemical autography Electrolytic copper decoration Electrolytic gas bubble formation Electrophoretic decoration Corona-charging decoration Nematic liquid-crystal light scattering in electric field Current noise of metal stripes over dielectric
Electronic Methods	Scanning electron microscopy Transmission electron microscopy Replica electron microscopy Electron diffraction
Mechanical Methods	Surface profilometry by stylus instruments Sectioning techniques
Chemical Methods	Selective solution etching of films or substrates Preferential high-temperature gas-phase etching
Localized Composition-Analytical Microvolume Methods	Electron probe microanalysis Ion microprobe mass analysis Electron scanning chemical analysis Scanning Auger microprobe analysis Laser scanning photoemission Neutron activation combined with autoradiography X-ray and electron diffraction

methods are described in articles and handbooks dealing with thin-film analysis[3, 7, 28, 29] and are well known to workers in the field of microelectronics; they will therefore be noted only briefly at the end of this section.

Important improvements have been made in recent years in a number of methods. Several of these are discussed in some detail and illustrated with typical examples. These include optical contrast microscopy, scanning electron microscopy, self-healing dielectric breakdown, selective chemical etching, electrolytic decoration, liquid-crystal techniques, electron-probe microanalysis, and ion microprobe mass analysis. The last two methods are extremely important for identifying the chemical composition of detected localized defects such as inclusions, whereas the other methods are important for locating the exact site, shape, and structure of imperfections. A combination of several methods is generally necessary to detect, characterize, and correlate defects on the plane of the dielectric film surface or within the film structure.

Analytical methods for characterizing important nonlocalized defects in dielectric films include electrical, optical, chemical, and mechanical techniques. A discussion of these is outside the scope of the present paper and the reader is referred to the extensive literature available on this subject.[7, 28, 29]

4.1 Optical Contrast Microscopy

The simplest technique for examining a structure for defects nondestructively is by standard optical microscopy using various types of illumination such as brightfield, darkfield, and oblique or grazing lighting to emphasize projections and depressions in the sample surface. The application of optical contrast methods such as polarized light, phase contrast, and interference contrast can often enhance or intensify an image greatly or reveal structural details that are not visible otherwise. Microbubbles of gases in fused glass layers, for example, may not be seen under normal brightfield illumination, but are made visible with cross polarized light.

The most modern and popular method of optical contrast intensification is differential interference-contrast after Nomarski. The instrumentation is based on a two-beam shearing interference device in which the light beams are split and recombined in polarized light by means of birefringent optical components. The contrast and clarity of the microscopic image is thereby maximized with a three-dimensional effect where the details appear either in a bright and dark

image or in brilliant interference colors. Differences in elevation of defect structures of less than 100 angstroms can be made readily visible. Other morphological details that may prove of crucial importance in defect analysis and that may not be observable by other techniques of light microscopy can often be discovered by Nomarski differential interference-contrast. The method and its applications have been described in detail by Lang in a series of papers.[30,31]

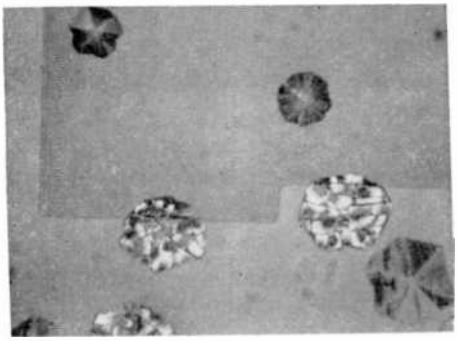

Fig. 1—Example of Nomarski differential interference-contrast microscopy. The photomicrograph shows detailed structures of localized defect regions in an arsenosilicate glass film deposited over silicon (35-μm-diameter crystallites) and over SiO_2 (locally cracked areas).

Fig. 1 shows a Nomarski differential interference-contrast photomicrograph of a vapor-deposited arsenosilicate glass layer after diffusion. The locally devitrified rosette-like regions in the glass can be seen much more clearly than under normal brightfield illumination. Several additional examples of interference-contrast applications are presented in subsequent sections of this paper.

4.2 Scanning Electron Microscopy

Detailed examination of local defects and surface morphology is best carried out with the scanning electron microscope (SEM). In this instrument a focused beam of high-energy electrons scans the sample surface in a rectangular raster. Effects of interactions of the primary incident electron beam with the specimen material are picked up by suitable detectors, amplified, and displayed as an intensity variation on a synchronously scanned cathode-ray tube. Of the various interaction effects used to produce an image in the display cathode-ray tube, the most common technique utilizes secondary electrons emitted from the specimen surface. The secondary-electron emission mode of operation is suitable for the majority of samples, including dielectrics.

Comprehensive discussions of principles and techniques of scanning electron microscopy are available for greater detail.[32-34]

There are many unique advantages to SEM for defect detection. Because the depth of focus in SEM is up to 1000 times greater than that in optical microscopy, it is possible to obtain a two-dimensional display of topographic detail with high contrast and good resolution, regardless of geometry or surface structure. Magnifications ranging from 10 to 100,000 times can be chosen electronically without change of focus.

The size of the sample area under examination can be extremely small since the localization ability or spatial resolution in present-day instruments is typically below 100 Å, as compared to about 3000 Å for light microscopy. Further improvements in resolution will soon be possible as the diameter of the electron beam probe is decreased by use of intense field-emission sources.

Another advantage of SEM is the simplicity of sample preparation. Insulating specimens can be made readily conductive (to keep the surface from charging in the beam) by coating with a very thin film of metal without impairing resolution. The mounted samples can be easily rotated inside the instrument in x, y, and z directions to obtain desirable angles for viewing and photographic recording.

Rapid advancements in instrumentation have made it possible to modify SEM or combine it with other techniques, thereby enhancing the capability of this already versatile and powerful analytical method even more. Electron diffraction analysis of areas down to micrometer range, which is now possible, will aid in the identification of particulate defects. The chemical composition of submicron-size particles can be determined by use of an energy-dispersive x-ray analyzer in the SEM.[28, 29, 34] More is said in the section on compositional characterization. A review of these and several other new SEM techniques was summarized by Johari.[35]

Microdefects in SiO_2 layers and local p-n junctions formed on transforming the defects during heat treatments were recently investigated by Galstyan et al.[36] They used the induced current mode of SEM for examining these junctions, and secondary electron emission for topographic studies of the oxide.

A selection of typical examples of scanning electron micrographs is presented to illustrate the application of SEM for dielectric detection by the secondary-electron emissive mode. Fig. 2 shows typical pinholes in a thermally grown SiO_2 film on a chemically etched silicon surface at magnifications of ×2,000 and ×10,000. The bottom diameter of the large holes measures 0.8 to 1 μm.

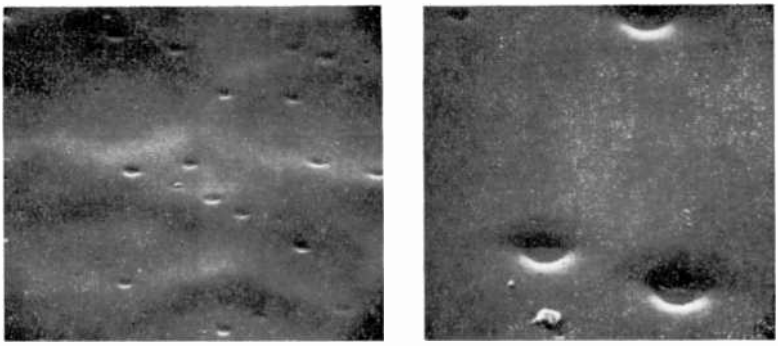

Fig. 2—SEM photomicrographs of pinholes in an SiO_2 film grown on chemically etched (111)-silicon.
left—×2000, 60°
right—×10,000, 60°. Bottom diameter of large holes measures 0.8-1 μm.

The value of the three-dimensional view obtainable with SEM obtainable under favorable viewing angles is especially apparent in the photomicrographs in Fig. 3. The deep microcracks formed in a thick layer of fused lead borosilicate during anneal treatments. The width of the microcracks is approximately 0.4 μm.

Fig. 4 shows the structure of a 1-μm-thick CVD (Chemical Vapor Deposited) SiO_2 film on a steep 70-μm-high wall of two circular silicon mesas. The sharp edge causes a rounded build-up of oxide. Some nodular welts and blisters in the dielectric coating are evident.

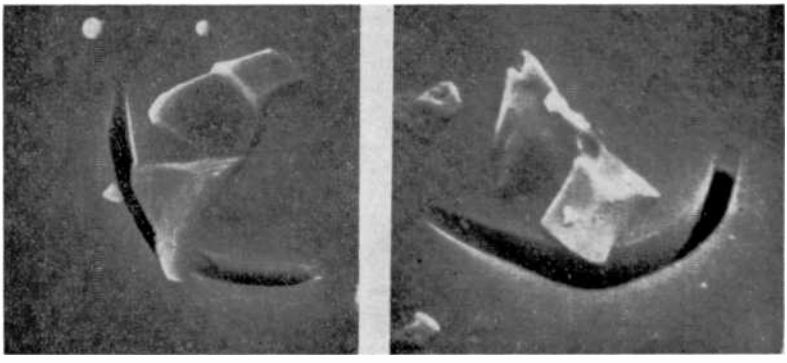

Fig. 3—SEM photomicrographs of 0.4 μm-wide microcracks in a fused glass layer, with debris of glass chips.
left—×10,000 at a viewing angle of 10° from the perpendicular.
right—×20,000 at 40° viewing angle.

Crystalline particles embedded in a doped oxide layer after high-temperature diffusion are shown in Fig. 5 before and after partial removal of the oxide films in HF-containing etchant. Thermal mismatch of the particles with the surrounding oxide has given rise to circular microcracks that enlarged on etching, exposing the crystalline imperfections. Electron microprobe analysis of the exposed crystals showed the absence of boron, phosphorus, or other elements with atomic numbers above 14; only silicon and oxygen were detected. Electron diffraction analysis identified the crystallites as β-crystabolite. This

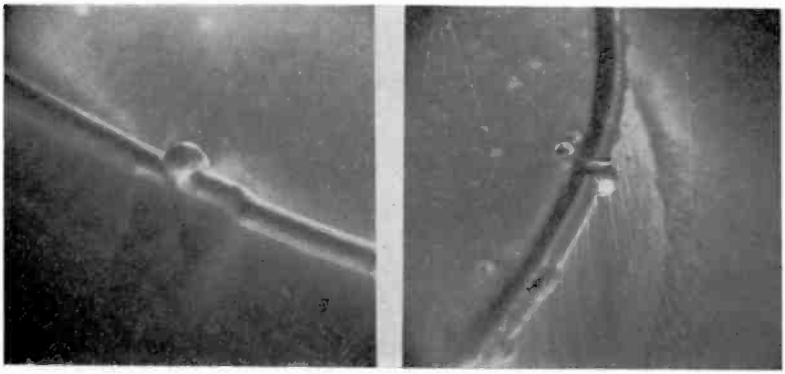

Fig. 4—SEM photomicrographs of a CVD SiO_2 film on steep silicon mesa walls showing various types of defects. Width of rounded buildup at edge measures 3-4 μm.

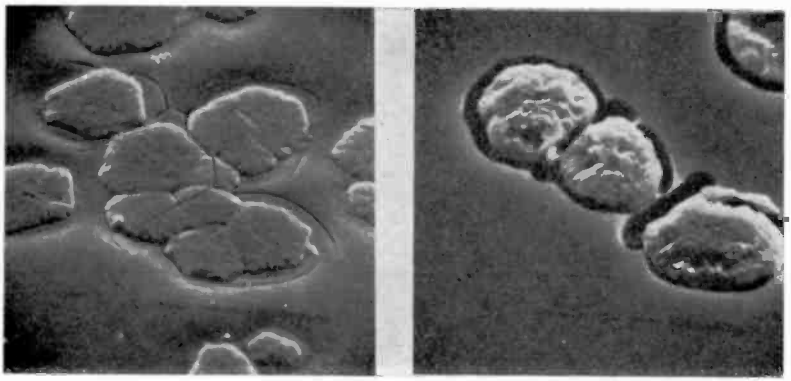

Fig. 5—SEM photomicrograph of crystalline particles (approximately 3 μm in diameter) embedded in doped SiO_2 and surrounded by microcracks.

left—Before etching (×10,000, 45°).
right—After partial etching (×10,000, 45°)

result is not too surprising since it is known that many contaminants can induce vitreous SiO_2 to locally devitrify into crystalline forms of silica.[37,38]

Examples of the use of SEM for examining the morphology and possible presence of local defects of CVD glass layers over steps in the substrate are presented in Fig. 6. The substrates in these examples are polycrystalline silicon-gate P-MOS integrated circuits. Phosphosilicate films with four different phosphorus concentrations were vapor-deposited at 450° C[18] and heated at 1000°C (60 minutes in nitrogen) to examine the effects on step tapering and surface smoothness of the glass.[26] Several additional examples of SEM are included in the subsequent sections.

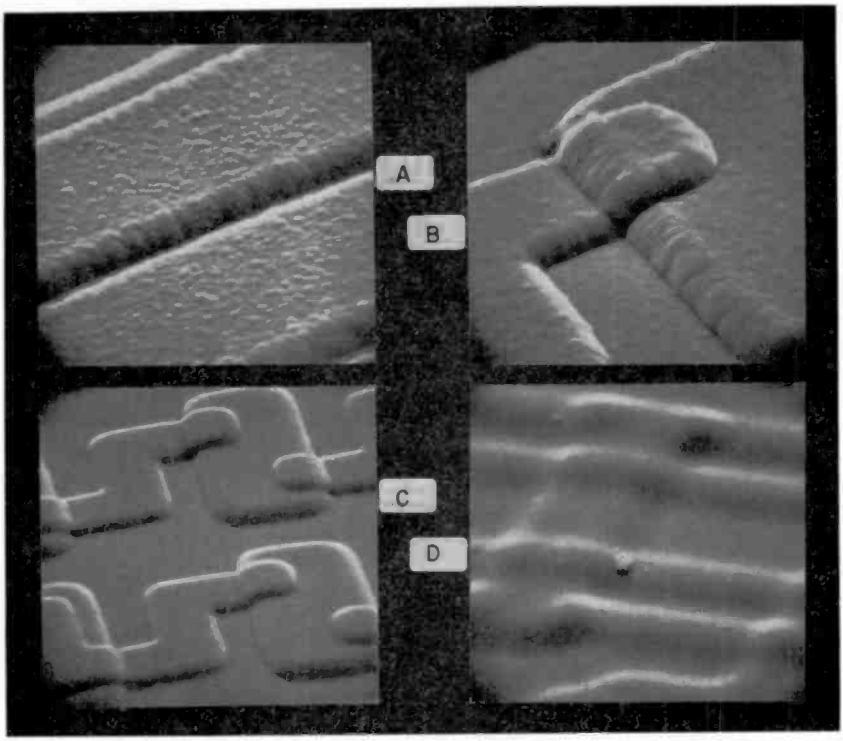

Fig. 6—SEM photomicrograph of 2-μm-thick CVD phosphosilicate glass layers of different compositions over steps in silicon gate P-MOS IC, showing various degrees of surface smoothness and tapering due to softening at 1000°C. Extent of melting increases as phosphorus content (wt. % P) in glass is increased from A to D. Minimum line within patterns measures about 4 μm.

A — 5.0 wt. % P: no melting
B — 6.4 wt. % P: slight melting
C — 7.9 wt. % P: strong melting
D — 10.3 wt. % P: excessive melting

4.3 Self-Healing Dielectric Breakdown

The electrical breakdown properties of a dielectric film are an important measure of the film integrity and quality. The dielectric strength of a film is critically affected by the presence of localized defects that may weaken the film structure, causing breakdown well below the intrinsic strength of the dielectric. A considerable amount of research has been conducted in recent years by Klein,[39,40] Worthing,[41] Osburn et al.,[42,43] and others to better understand the fundamental and practical aspects of dielectric breakdown.

In the usual procedure for measuring dielectric breakdown (by forming a capacitor structure in which the silicon serves as one electrode, the dielectric film is the insulator, and a deposited metal forms the counter electrode), only one minimum breakdown voltage value is obtained, because breakdown occurs at the weakest point. This value determines the merit of the dielectric for device applications, but does not reflect the intrinsic breakdown, or maximum dielectric strength, of the bulk material itself.

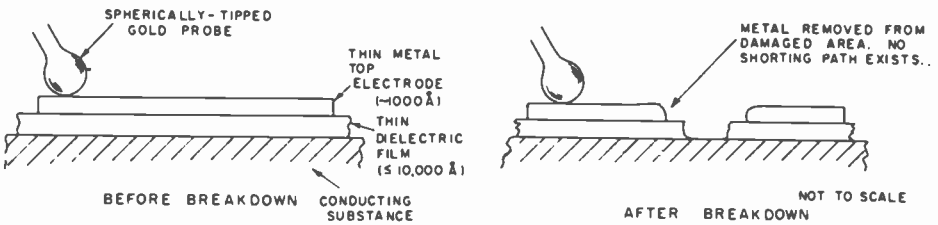

Fig. 7—Cross-sectional view before and after a self-healing breakdown event on an MIS capacitor. Top metal electrode is removed from damaged area so that no shorting path exists. Size of damaged area is out of proportion—typical damage is 5 μm across.

The self-healing breakdown technique[39,40] permits many measurements of a single sample. A thin metal upper electrode (≤1000 Å) is used on dielectric films of up to 10,000 Å thickness. When a voltage is applied across the dielectric film and breakdown occurs, the thin metal electrode is removed from the region of destruction by localized explosive heating. This process eliminates the weak point in the dielectric from the circuit since a conduction path in this region of the upper electrode is no longer present (Fig. 7). The test capacitor is still a good capacitor with a slightly smaller area. The damaged area is typically only several micrometers in diameter so that thousands of self-healing breakdowns may occur on one capacitor during testing.

The initial breakdown events occur at the weak spots in the film, but as the process continues these weak spots are destroyed and eventually the intrinsic breakdown strength is reached.

These experiments are most conveniently carried out using the ramp voltage technique described by Carnes and Duffy[44] in which a ramp voltage with a variable rise time (1-100 V/sec) is applied across the sample. Fig. 8 shows a circuit diagram of the apparatus; the

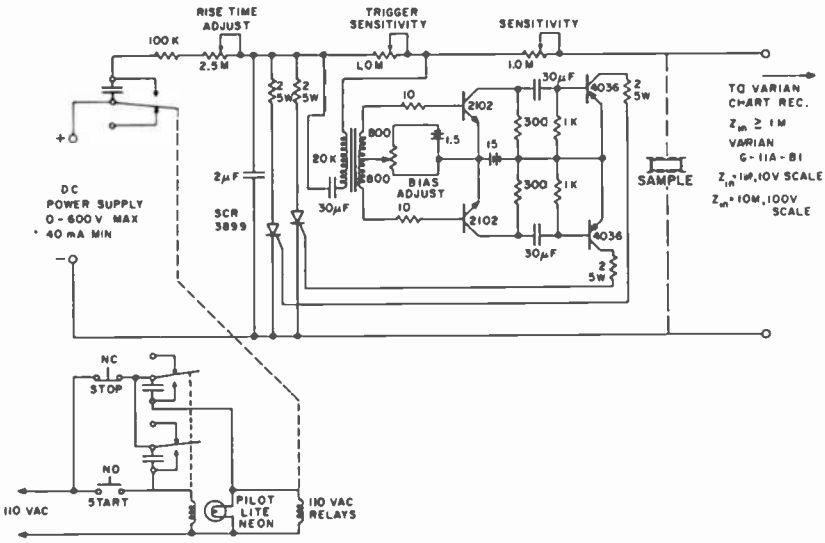

Fig. 8—Circuit diagram for ramp-mode self-healing-breakdown apparatus.

voltage across the sample is graphically indicated as a function of time on an automatic chart recorder. The voltage increases until breakdown begins; at this moment the increasing sample current fires an SCR, returning the sample voltage to zero, and another ramp sequence begins for a new breakdown at the next weakest site.

Typical self-healing breakdown recorder traces for three different dielectric defect densities are presented in Fig. 9. For each sample the breakdown voltage of each successive breakdown event from right to left, represented by the peak of each vertical trace, increases as weak spots are sequentially removed by the self-healing process. Eventually constant peak height is attained, indicating that all weak spots have been broken down. The constant peak height now indicates the intrinsic breakdown voltage of the dielectric. In Fig. 10 the breakdown voltage is plotted as a function of the $\log_{10}$ of the breakdown event

number for the three different dots shown in Fig. 9. The low-density sample attains the ultimate breakdown value after about 10 breakdown events, the median density after ~60, and the high-density after ~600.

Fig. 11 shows an enlarged high-density breakdown area of a silicon nitride film on silicon. The light area is the gold electrode; the circular spots are exposed silicon nitride from which the gold film melted away during the breakdown event. Darkfield photomicrography mapping before and after breakdown testing revealed that the cause of the weak spot breakdown can be correlated directly with surface imperfections on the silicon substrate before film deposition.

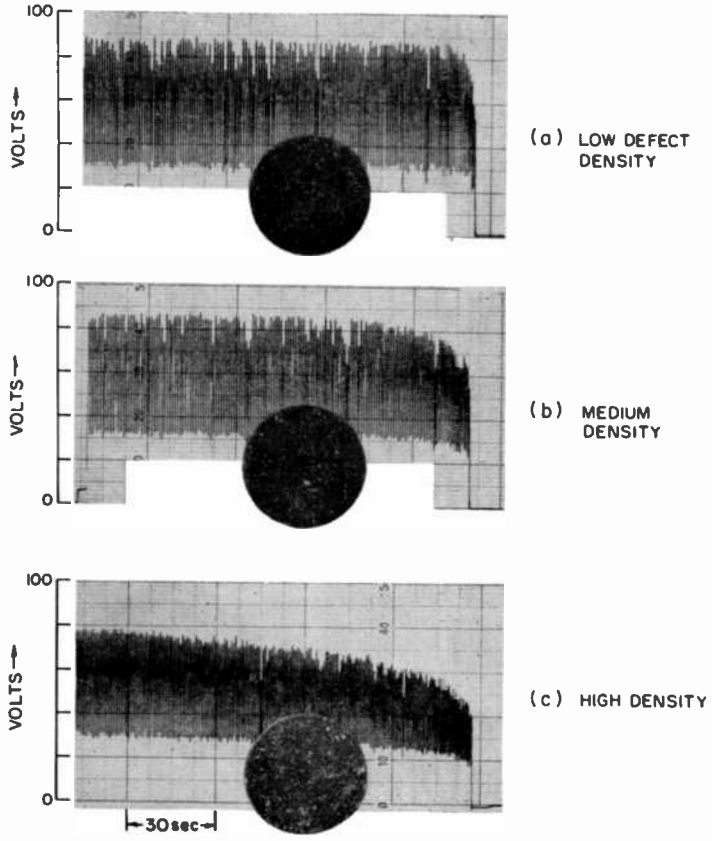

Fig. 9—Self-healing-breakdown recorder traces showing the weak spot profile for three different gold electrodes with different defect densities. The gold electrode areas before breakdown as seen by dark-field microscopy at ×50 magnification are shown in the inset on each trace. (Note that the traces proceed from right to left.)

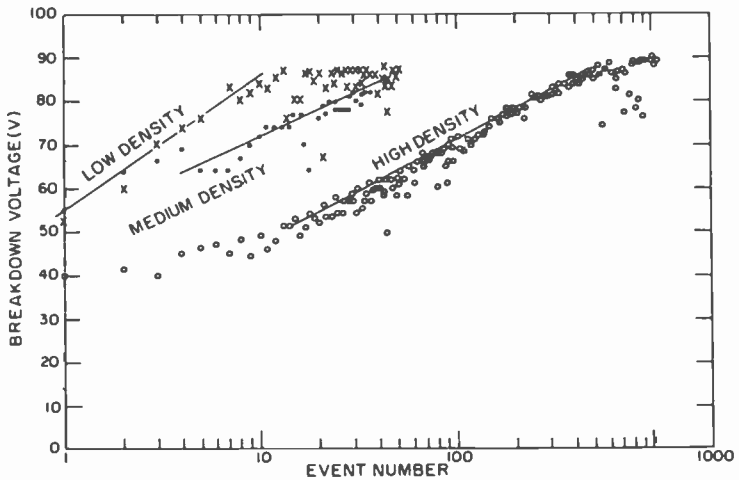

Fig. 10—Self-healing-breakdown voltage as a function of $\log_{10}$ of the breakdown event number for the same electrodes shown in Fig. 9.

Scanning electron micrographs of typical breakdown damage of Al_2O_3 on p-type silicon with gold electrodes are presented in Fig. 12. For the Si+ polarity, single spot breakdown occurs, whereas for the Si− polarity, clustering of many breakdown events occur.

The advantages of the voltage ramp self-healing breakdown technique are that it is fast and provides a distribution of defects according to their voltage breakdown characteristics, and also gives the intrinsic breakdown strength (ultimate voltage capability) of a dielectric film, all in one test sequence.

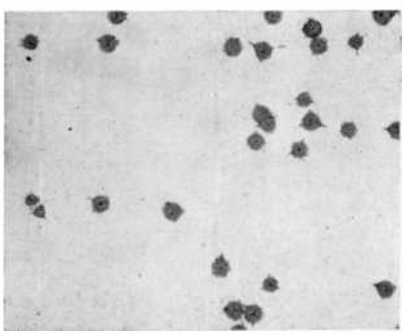

Fig. 11—Photomicrograph of high-density self-healing-breakdown area of a Si_3N_4 film on silicon. Light area is intact gold film. Grey areas (mostly 2.5 μm in diameter) show exposed Si_3N_4 after dielectric breakdown. Dark spot in center of each exposed Si_3N_4 area is damage to silicon caused by breakdown event.

4.4 Selective Chemical Etching

Localized defects in the categories of complete or partial film discontinuities such as pinholes, hairline cracks, and partial microholes can often be revealed by selective chemical etching. The etchant must penetrate through the defect opening and selectively attack the substrate material on which the dielectric film was grown or deposited. A sufficient period of time must be allowed for the etchant to react so that the attacked substrate becomes readily visible as an enlarged area underneath the defect.

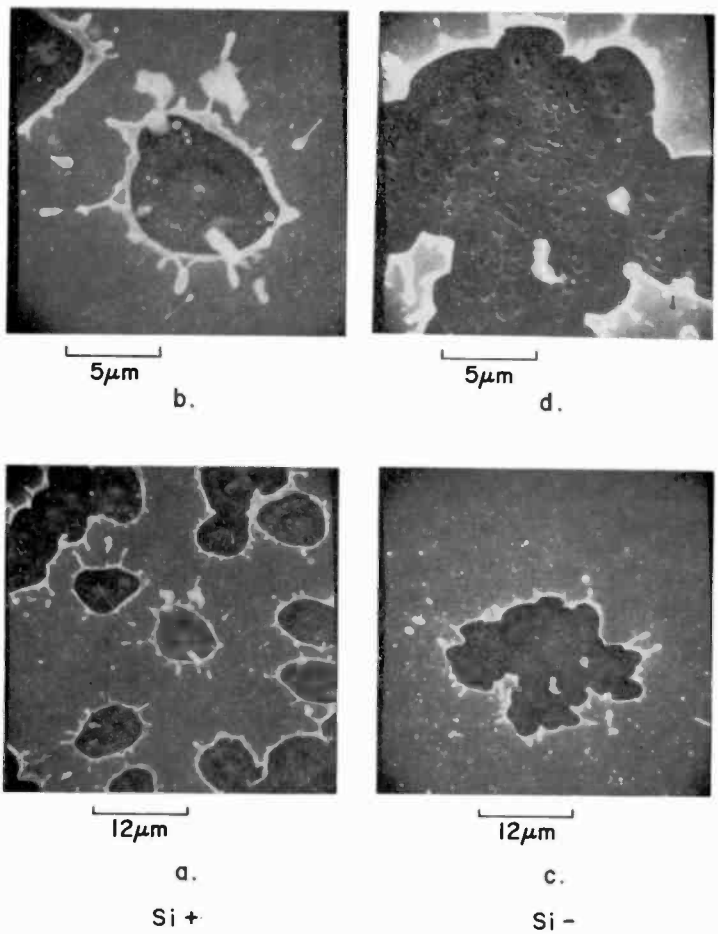

Fig. 12—Scanning electron micrographs of typical self-healing-breakdown damage of Al_2O_3 films chemically vapor deposited on p-type silicon subtrate wafers; (a) and (b) are both for Si+ (accumulation); (c) and (d) for Si− (depletion).

Partial discontinuities can often be detected by briefly etching the dielectric film prior to selective substrate etching. Fast etching imperfections latent in silicon dioxide films as reported by Lopez[45] are an example where this technique is applicable. Successive oxide and substrate etching could in fact be used to reveal partial pinholes of decreasing depth.

Several techniques have been developed for detecting pinholes in silicon dioxide layers on silicon substrates. One of the oldest is etching in dry chlorine gas at about 900°C, which attacks the silicon but not the oxide.[46] We have used a higher temperature (typically 1050°C) with improved results, especially for thick SiO_2. Etching is conducted in a quartz tube furnace that is purged with nitrogen before and after etching. The method is fast and allows ready identification and counting of pinholes under the microscope. The potential safety hazard is an obvious disadvantage and dielectric films other than SiO_2 are usually attacked in this procedure.

Selective silicon liquid etchants at elevated temperature have been used successfully for detecting discontinuities in SiO_2 films on silicon. Pyrocatechol-ethylenediamine-alcohol mixtures[47] are restricted to elemental silicon substrates and are extremely slow. Catechol-hydrazine[48] in aqueous or anhydrous media is applicable to both elemental and lightly doped silicon.

The simplest and most widely applicable method for most dielectric films on silicon is based on single-component alkali solutions, recently described in detail by Pugacz-Muraszkiewicz.[49] Typically, a 10 wt. % aqueous solution of sodium hydroxide is employed at 70° C to etch the silicon anisotropically, producing etch pits whose shape depends on the crystallographic orientation of the silicon. The time required to etch the geometrically characteristic pit for a given substrate orientation is related to the size of the opening in the dielectric and allows measurement of size and shape of a discontinuity. Both intrinsic and doped silicon up to dopant concentrations of about 10^{20} cm^{-3} can be used.

Dielectric layers deposited over metallized structures require different types of selective etchants for detecting discontinuities. Keenan and Runyan have described an electrochemical anodization test in a weak electrolyte solution for locating defects in SiO_2 protective coating over nickel-chromium resistors with aluminum leads.[50] They also noted the use of a ceric sulfate solution for selectively etching nickel-chromium under defective SiO_2 layers.

Detection of discontinuities in dielectric layers over aluminum metallization can be accomplished readily by immersion of the sample in aluminum etchants of alkaline[50,51] or acid[52,53] compositions. This

type of testing is of considerable technological importance in optimization of dielectric film deposition processes and for quality testing and failure analysis of integrated circuits and multilayer metallization structures. The examples presented in Figs. 13 to 16 were prepared in our laboratories and serve to illustrate the effectiveness of this method.

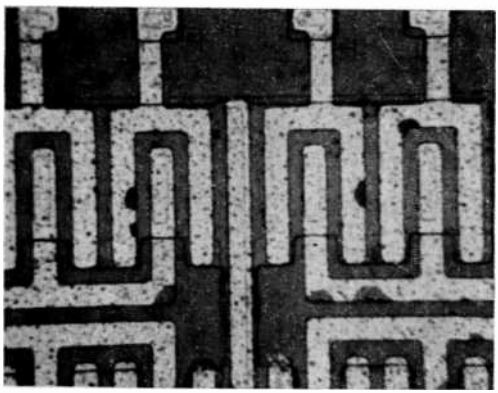

Fig. 13—SiO_2-overcoated aluminum metallized IC after exposure to aluminum etch. Each circular area in the 14-μm-wide metal stripes shows where the etch penetrated through a micropore in the protective oxide.

Fig. 13 shows part of an aluminum-metallized integrated circuit with a CVD protective overcoat of SiO_2. No defects could be found on microscopic inspection. The sample was then immersed in aluminum etch* for double the time required to dissolve exposed aluminum. The dark conspicuous spots in the aluminum pattern are areas where the etchant penetrated through pinholes in the oxide, dissolving the underlying metal. Most of the pinholes are submicron-size pores located along the edges of the metallization, hence the semicircular area surrounding each pore.

The presence of a microcrack through a protective glass layer over a large 410-μm-long aluminum capacitor has become evident in the photomicrograph, Fig. 14, after the sample had been immersed in aluminum etch. The actual crack and other defects were barely detectable by optical microscopy. The width of the aluminum removed under the microcrack measures about 10 μm, affording a convenient marking

* Aluminum etch: 100 ml H_3PO_4 (85%), 10 ml HNO_3 (75%), 25 ml deionized H_2O; used at 50-55°C, typically for 5-15 minutes, depending on aluminum thickness.

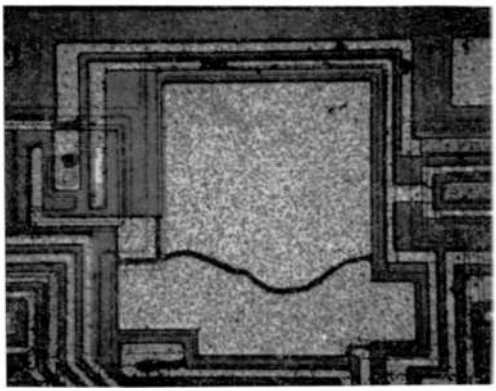

Fig. 14—Selectively etch-marked microcrack through protective glass layer over an aluminum metallized capacitor area. Width of aluminum removed under crack measures 10 μm. Width of glass crack is about 0.2 μm. Several other defects in the glass layer are evident that were not detectable before selective etching.

of the dielectric defect. Extending the length of etching enlarges the area beneath a discontinuity. Despite the extremely small width of these openings, the etchant penetrates readily. For defects that are less accessible to the etchant, the incorporation of an acid-stable surfactant should prove beneficial. Vacuum impregnation techniques can also be applied in such cases.[53]

Scanning electron micrographs of microcracks from the same device wafer shown in Fig. 14 are presented in Figs. 15 and 16 at low and high magnifications. These pictures were taken before alumi-

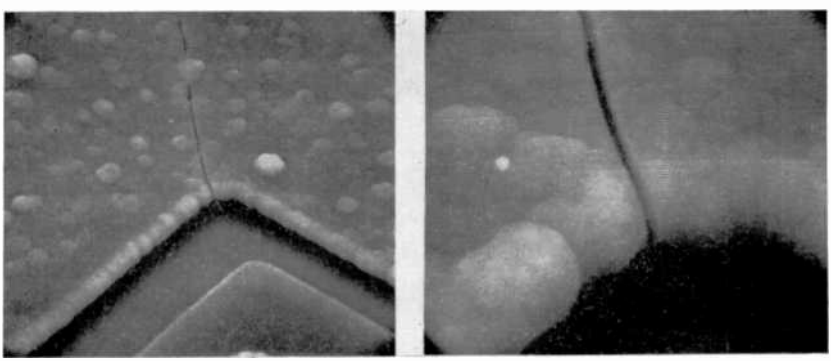

Fig. 15—Scanning electron micrographs of stress microcracks in CVD glass over aluminum (sample from same wafer shown in Fig. 14). Width of cracks is about 0.2 μm.

left—×2,000, 45° view from perpendicular
right—×10,000, 45° view from perpendicular

num etching. No change is visible by SEM after aluminum demarkation etching, as would be expected, since only the surfaces are seen by secondary electron emission SEM. The width of these microcracks is in the order of 0.2 μm. The thickness of the glass overcoat layer is 1.5 μm. The roughness in the glass over the metal area is due to the usual graininess of the aluminum.

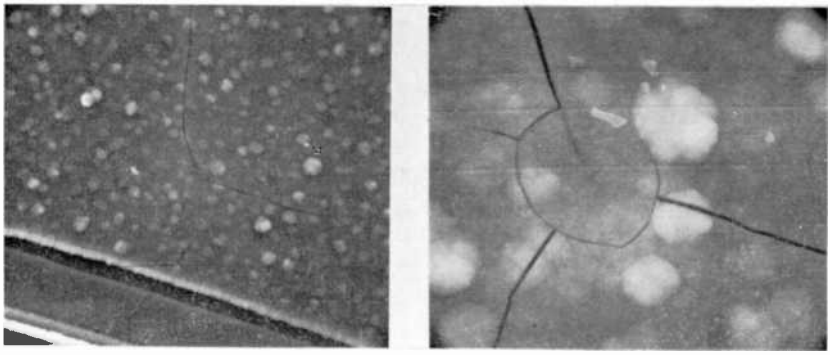

Fig. 16—Scanning electron micrographs of impact microcracks in CVD glass over aluminum. Width of cracks is about 0.2 μm.
left—×1,000, 2° view from perpendicular
right—×5,000, 2° view from perpendicular

4.5 Electrolytic and Electrophoretic Methods

Electrochemical techniques are particularly well-suited for detecting pores and microcracks in dielectric films on semiconductor substrates in wafer form. Some of these techniques are nondestructive and are therefore especially useful in process control.

Besser and Meinhard[54] described an electrolytic method in which pinholes in a dielectric film on a semiconductor substrate give rise to microscopically observable trains of fine hydrogen gas bubbles. The silicon wafer with the dielectric coating to be tested is immersed in a dissociable dielectric liquid (such as acetone or methanol[55]) so that anodic dc contact is made with the etched backside of the wafer and the bottom of the metal container. A copper anode is immersed in the liquid above the wafer and a potential of 10 to 100 volts is applied. Electrolysis takes place at defect sites in the dielectric film resulting in hydrogen microbubbles that can be observed under a low-power microscope. A diagram of the test assembly is reproduced in Fig. 17. The gas formation arises from electrochemical decomposition of the

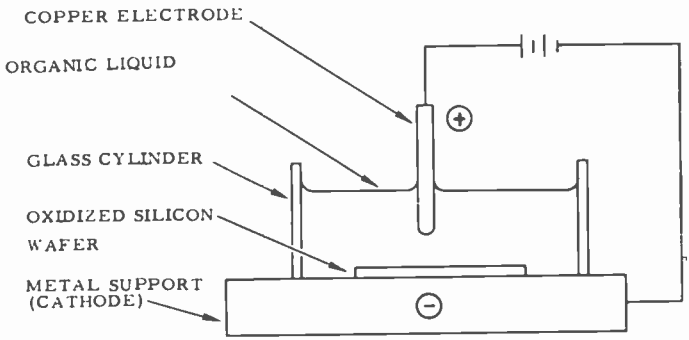

Fig. 17—Schematic of apparatus for electrophoretic decoration of dielectric defects. (After Ref. [54]).

dielectric liquid or of traces of dissolved water. The surface surrounding the defects in the dielectric film is being decorated by positively charged colloidal particles of copper oxysalts that migrate from the copper anode due to the electropotential. A refined instrument designed on this principle is available commercially.[55] It can be used both in the electrolysis mode for inspecting sites that give bubble formation, and in the electrophoresis mode for permanently decorating the defect sites.

Shannon[56] noted that the above methods did not consider the important factors of electric field distribution and surface voltage dependence of the dielectric and its relationship to film integrity. In his apparatus, shown schematically in Fig. 18, the uniformity of the electric field across the wafer was improved by use of a copper mesh as anode of a size larger than the diameter of the wafer. The potential gradient between the anode and the sample serves only to force the

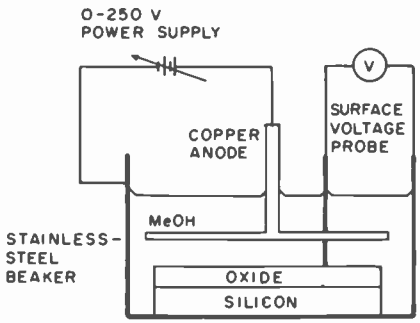

Fig. 18—Schematic of apparatus with improved field uniformity for electrolytic copper decoration of dielectric defect.

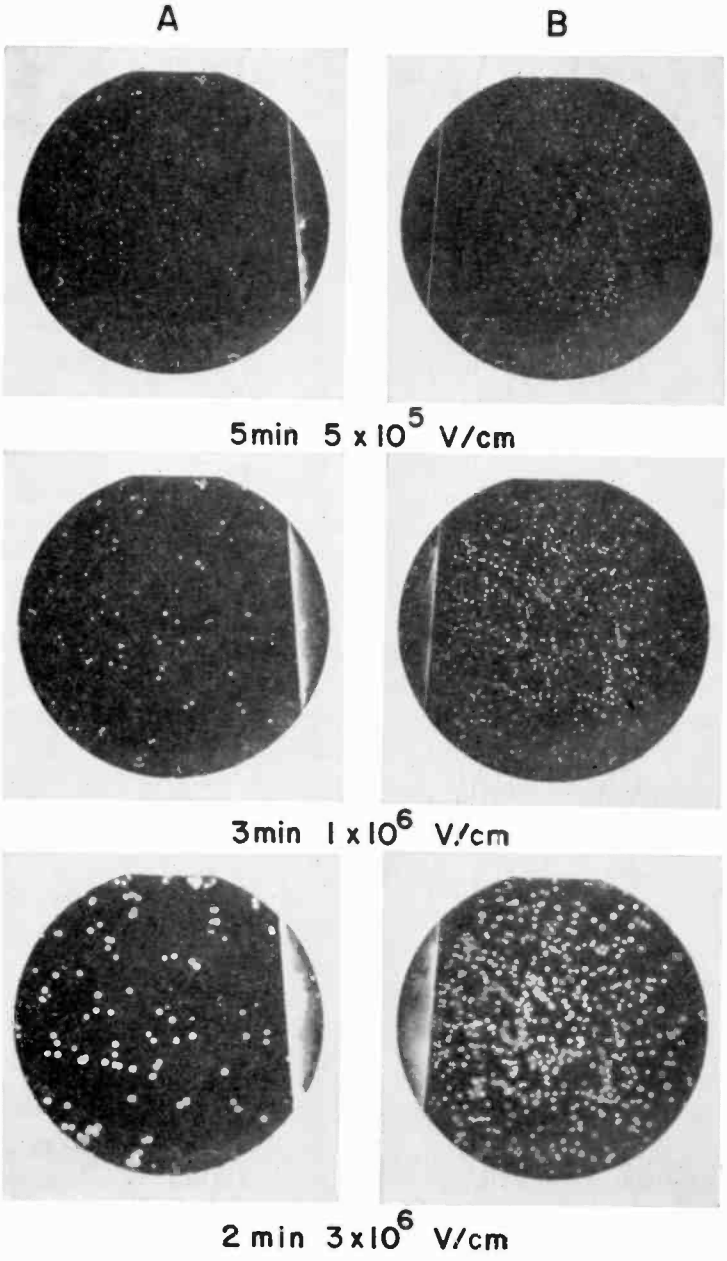

Fig. 19—Copper-decorated SiO_2 defects in two silicon wafers (1¼-inch diameter) as seen after application of successively increasing oxide fields. The defects were caused by failure of two types of photoresist (A and B) on prolonged exposure to buffered HF.

copper ions, which are released from the anode, to the vicinity of the dielectric film surface where they interact with the high field centers caused by the defects. A large fraction of this applied potential is dropped by the dielectric fluid (absolute methanol), and therefore only the voltage measured at the surface of the dielectric film controls the field within it. The voltage is measured at the dielectric film surface with a surface voltage probe and a digital voltmeter. Shannon found that the dielectric film integrity is relative, and is exponentially dependent upon the field and therefore on the dielectric surface voltage. The weakest parts of the dielectric film decorate first and additional, less weak sites, become decorated with copper as the electric field is increased. For a meaningful application of this technique, the conditions should therefore be fixed or varied in a standardized manner. The decorations grow in size but not in number as a function of time.

A practical illustration of the method is presented in Fig. 19. Two silicon wafers with 7000 Å of thermally grown SiO_2 were used to study the masking effectiveness of two different photoresists when immersed in buffered HF solution for a prolonged time period. After stripping the photoresist coatings, the oxide defects caused by resist failure were made visible for manual or automatic counting by copper decoration at three different oxide field densities as indicated in the figure.

The appearance of the copper decoration surrounding a defect varies with the size and geometry of the defect in the dielectric film. Fig. 20 shows enlarged views of decorated defects on wafers A and B from Fig. 19. Nomarski differential interference-contrast was used to make the detailed structure visible.

Besser and Meinhard[54] described a simple screening test based on electrochemical autography which is nondestructive and introduces no metallic contaminants. The unmetallized device wafer having a dielectric coating is placed face down on a white membrane filter impregnated with an electrolyte solution. The aqueous solution contains a redox reagent, such as a benzidine salt, a suitable surfactant, and a protective colloid. Electrical contacts are made as indicated in the schematic diagram (Fig. 21). The detailed procedure was described by McCloskey.[57] On applying a potential of only a few volts, local anodic oxidation of the colorless benzidine on the film to a dark blue reaction product takes place. The spots correspond to defect sites in the dielectric film where conductive silicon substrate is exposed. A concise autographic replica of the defects is thus created for microscopic inspection. The disadvantages of this technique are that no significant enlargement of the defect sites results, so that high-power microscopy is required to observe submicron-size decoration sites.

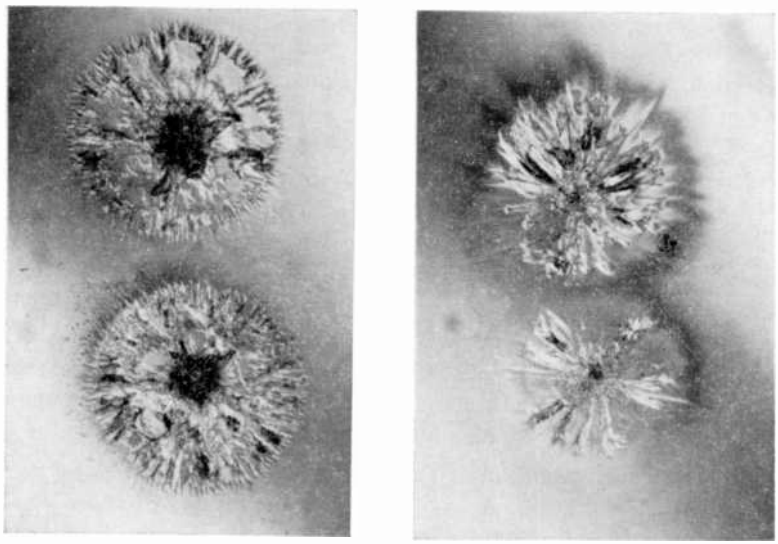

Fig. 20—Enlarged decorations on wafers A and B (Fig. 19). The geometric appearance of the decoration is influenced by the geometry of the defect site. Photomicrographs were taken with Nomarski differential interference-contrast to bring out detailed structure.

left—Diameter of decoration 290 μm.

right—Diameter of decoration 230 μm.

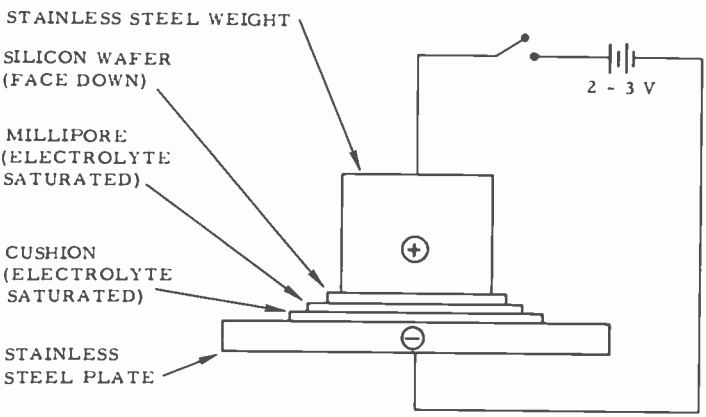

Fig. 21—Schematic of apparatus for electrochemical autography of dielectric defects. (After Ref. [54]).

Furthermore, extreme caution must be exercised because of the carcinogenic nature of benzidine and its salts.

Exploratory experimentation by Comizzoli and Kern[58] has indicated that selective electrophoretic deposition of intensely fluorescing dielectric particles offers a very sensitive means for detecting pinholes, microcracks, thin spots, and other defects in an insulator layer covering a conductive or semiconductive surface. Green fluorescing willemite and silver-activated zinc-cadmium sulfide, with its bright yellow-green ultraviolent fluorescence, are particularly excellent decorating agents for this purpose. Europium-activated yttrium oxide powder, with its intense red ultraviolet fluorescence, is another suitable decorating agent. A thermoelectric cold plate is used as sample stage to intensify the fluorescence of the phosphors excited by two filtered ultraviolet radiation sources positioned directly at the sample site. Decoration can also be carried out by corona charging of the oxide and immersion in a particle suspension. This technique allows both direct decoration of the defect and reverse decoration in which the defect is left bare and thus accessible to microscopic analysis.

4.6 Liquid-Crystal Techniques

Dynamic light scattering of nematic liquid crystals in an electric field is a very interesting novel method for observing defects in dielectric films and p-n junctions. The method is particularly well suited for screening and testing of metallized integrated circuits and other planar devices in wafer form, after pelletizing, and even after wire bonding to the contact pads. The active device area need not be contacted and the devices can be recovered by solvent rinsing after testing.

The application of liquid crystals for visualizing dielectric defects and testing of breakdown strength was reported by Keen.[59,60] Use of the method was subsequently described in some detail by several workers.[61-64]

Fig. 22 shows a schematic diagram of a typical experimental arrangement. A drop of a liquid crystal is placed on the surface of the device wafer to be tested and a thin cover glass, coated with a transparent, electrically conductive layer of tin oxide, is placed on top forming a cell of about 10 μm thickness. Any negative nematic liquid crystal can be used, but most of the exploratory studies were conducted with p-methoxy-benzylidene p-n-butyl aniline. The back of the wafer must be free from dielectric to electrically contact the metal vacuum chuck. The test voltage is applied between the back of the wafer and the tin oxide layer as indicated in the drawing, and the sample is observed under an incident light microscope. A typical pin-

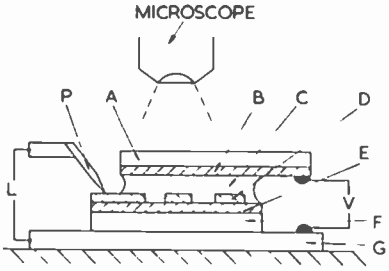

Fig. 22—Schematic of typical test assembly used in liquid-crystal techniques for visualizing dielectric defects. The probe (P) and electrometer (L) are auxiliary equipment to measure voltage across the dielectric; they are not needed for routine testing. (After Ref. [60]).

A — cover slide
B — tin oxide coating
C — liquid crystal
D — metallization
E — dielectric layer
F — silicon substrate
G — stainless steel vacuum chuck
V — voltage source

hole display of a 1500 Å thick SiO_2 film on silicon just above the threshold voltage is shown in Fig. 23.

If pinholes exist in the dielectric film, flow patterns in the otherwise clear liquid-crystal layer can be observed above the pinholes when a potential above a threshold of about 3.5 volts is applied. Initially the flow is laminar and visible local cells or vortices are formed. Electro-

Fig. 23—Photomicrograph illustrating electrohydrodynamic mode (laminar flow) at pinholes in a 1500Å-thick SiO_2 film just above the threshold voltage (4 volts applied). The focusing effect of the vortices is clearly seen. (Acknowledgment is made to the Controller of Her Majesty's Stationery Office for permission to reproduce this photograph).

hydrodynamic laminar flow patterns and the focusing effect of the vortices are visible due to the anisotropic refractive index of the liquid crystal. The voltage appears only at a defect site across the liquid crystal, hence the displays are localized around each defect.

The vortex flow accelerates with increasing voltage until at 7 volts turbulence sets in, causing vivid displays of strong dynamic light scattering around partial defects such as thin spots in the dielectric layer. Photomicrographs of this type of display are presented in Fig. 24. An identical area of a 1200 Å thick thermal oxide film at two bias voltages shows dynamic scattering at pinholes in the oxide above scratches. The scratches are in the silicon substrate and were introduced before oxidation. This electrohydrodynamic flow effect occurs wherever there is a current leakage path to the substrate and a field greater than the threshold of approximately 5×10^5 volts/cm across the liquid crystal. The thickness of the liquid-crystal cell does not effect the turn-on voltage of the display. The vortex diameter is directly proportional to the cell thickness. Since the liquid crystal is highly resistive and the currents required for a display are extremely small ($\sim 3 \times 10^{-6}$ A/cm^2), dielectric layers up to and past breakdown voltage can be tested non-destructively.

4.7 Chemical Composition Analysis of Localized Impurities

After detecting and accurately locating defect areas in dielectric films it is frequently necessary to ascertain their chemical composition, especially if the defects consist of particulate inclusions or contaminants. The volume of matter available for analysis is frequently in the range of cubic micrometers, requiring highly sophisticated instrumentation for successful characterization. Several micro- and ultramicroanalytical methods are available (see Table 2) to fulfill this usually difficult task.

Electron-probe microanalysis is useful for identification *in situ* of average elemental composition in localized impurity particles of typically 1 to 2 cubic micrometers in areas up to 1 μm in thickness. It is therefore particularly well-suited for problems involving characterization of crystallites, grains, precipitates, inclusions, individual layer sections, concentration gradients, etc. Basically, the electron-probe microanalyzer is an electron-probe x-ray primary emission spectrometer. It is often used in combination with the scanning electron microscope. The material is analyzed to a depth ranging from 200-20,000 Å, depending on sample and analysis conditions. Absolute detection sensitivity is about 10^{-15} g, and relative sensitivity typically 0.01 to 0.1 wt.% with a precision within ±5%. A thin conductive film must be deposited over dielectric material, which renders the method

destructive for such samples; other disadvantages are that the atomic number of the element to be detected must be at least 4, that the analyte must be absent in the substrate, and that the sample surface must be reproducibly smooth. Quantization is difficult and often requires composition standards. The method is time consuming and hence expensive. Nevertheless, the electron-probe microanalyzer has

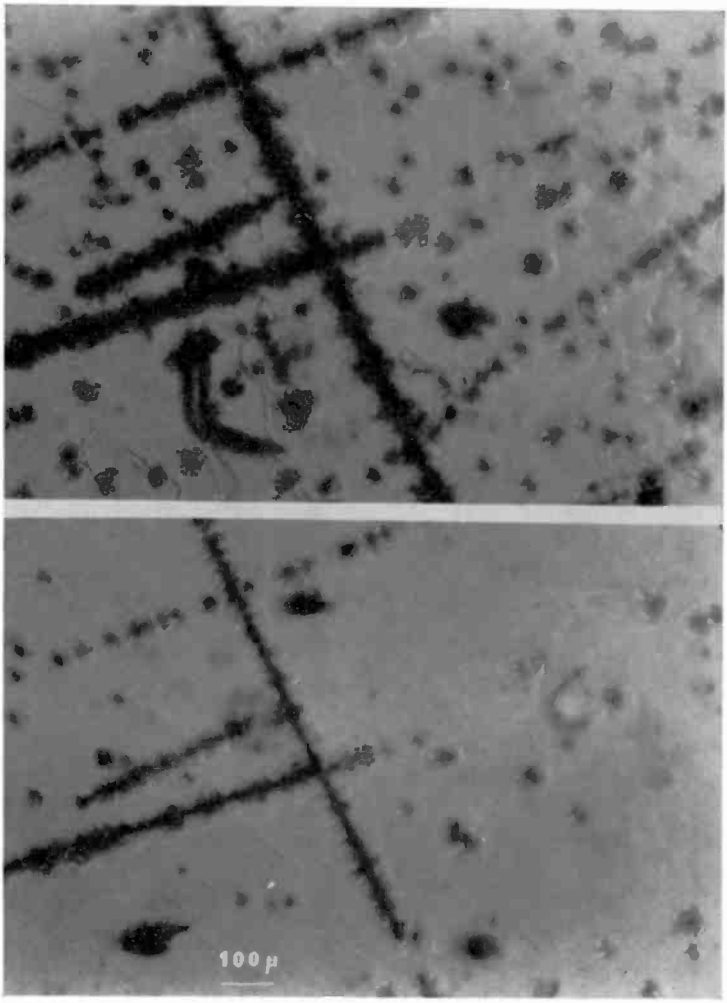

Fig. 24—Photomicrographs illustrating dynamic scattering mode (turbulent flow) at pinholes in a 1200Å-thick SiO_2 film: top—40 V bias, bottom—20 V bias. The scratches are in the silicon substrate and were made before thermal oxidation. (Acknowledgment is made to the Controller of Her Majesty's Stationery Office for permission to reproduce these photographs).

been an indispensible diagnostic tool for local composition analysis and has led to many important conclusions. A comprehensive treatment of this method was published by Birks.[65] For short reviews see, for example, Kane and Larrabee[28,29] and Johari.[35]. Swaroop[66] reported on its application to SiO_2 films, and Colby[67] recently reviewed its use in microelectronics failure analysis. An actual example of an application of electron-probe microanalysis for characterization of localized impurity crystallites in a dielectric layer was illustrated in the related SEM section.

Ion-probe microanalysis, also called ion microprobe mass analysis or secondary ion mass analysis, is at present one of the best semiquantitative survey methods with a very high detection sensitivity for ultramicro-analysis of impurity particles or other materials. A beam of a single species of ions is used to bombard the sample. The secondary ions generated by the primary ion impact are analyzed by a mass spectrometer. As in electron-probe microanalysis, a conductive surface coating is usually necessary for insulator materials, although negative primary ions can be used to reduce charging, and this method is 1000 to 10,000 times as sensitive. Layers near the surface as well as in the bulk of the film can be analyzed, since monolayers are successively stripped (sputtered) by the primary ion beam. A three-dimensional compositional characterization of the spatial elemental distribution can therefore be achieved. A sample area with a diameter of 1 to 20 μm is needed. All isotopes of each element are detectable without mutual interference with various degrees of sensitivity, typically in the parts-per-billion range, and with a routine accuracy of $\pm 5\%$. If suitable standards are available, absolute detection limits in the range of 10^{-15} to 10^{-19}g can be realized under favorable conditions. One of the disadvantages is the price of the instrumentation (around $250,000); nevertheless, it can be expected that its use will become much more widespread in the future. A brief review of the method for failure analysis has been presented recently by Colby.[68] Brief methodological reviews were given by Kane and Larrabee[28,29] and Bayard,[69] and more recently by Andersen and Hinthorne[70] and by Lewis.[71] Several examples that illustrate the application of the method to impurity analysis in dielectric films have been reported.[69,72,73] However, these applications were concerned primarily with impurity distributions over relatively large areas. The characterization of particulate contaminants requires a high degree of lateral resolution, depending upon particle size. Representative examples of lateral elemental distribution analysis, with lateral resolution in the range of 1 to 2 μm, have recently been published also.[70,74]

Electron spectroscopy for chemical analysis (ESCA) in its various forms is continuously being refined as more sophisticated instrumentation is rapidly becoming available. Its fundamental forms comprise electron impact spectroscopy, x-ray-induced photoelectron spectroscopy, vacuum UV-induced photoelectron spectroscopy, and Auger spectroscopy.[75] The majority of ESCA applications has been directed with great success toward characterizing monolayers, thin films, and solid surfaces, especially with respect to surface contaminants in trace quantities (see, for example, the survey articles noted in Refs. 76, 77). Another important variation is Auger spectroscopy in conjunction with simultaneous sputter-etching to obtain compositional depth profiles.[76,78] Of particular interest to the compositional characterization of localized impurities are combinations of these ESCA methods with the scanning electron microscope.[35] The combination of an energy-dispersive x-ray analyzer with the SEM has been noted in the section on SEM. The combination of SEM with Auger electron spectroscopy allows sensitive identification of micrometer-size surface structures with direct comparison of SEM and elemental images. In the form of the scanning Auger microprobe[79] the instrumentation is capable of producing both Auger and reflected electron micrographs with a spatial resolution of 3 to 5 μm, allowing the determination of composition together with topography of surface regions in the range of a few micrometers. Powerful characterization methods such as these will undoubtedly gain great importance for diagnostic and analytical work in future microelectronics research and materials control.

4.8 Miscellaneous Methods

Most of the useful methods listed in Table 2 for detecting and characterizing local defects in dielectric films have been discussed in more or less detail in the preceding sections. Some of the remaining methods are either well known or more restricted to special applications and will be mentioned only briefly.

Optical scattering techniques are useful for rapid inspection of the surface for irregularities such as pits, mounds, and particulate contaminants. A strong beam of light is focused on a polished surface and the surface is viewed from the side so that the reflected light is not observed. Any surface defects caused by changes in height or index of refraction will scatter (or reflect) light out of the normal reflection angle. Defects are visible especially well if the surface is illuminated at grazing incidence with a laser beam as light source. A 5-milliwatt helium–neon laser with a photomultiplier tube as detector can be used for scanning the entire wafer surface for observation in an output display.[80]

Surface profilometry with commercial stylus-type instruments, such as the Talysurf or Dektak, are very useful for measuring etch step heights, surface profiles and surface roughness of the dielectric layers. The measurements are carried out with a diamond stylus that senses changes in the mechanical height. This information is automatically recorded as a surface profile. Film thicknesses from about 20 Å (more typically 50 Å) up to 10 μm can be measured with an accuracy of a few percent.[81,82]

Optical multiple-beam interferometry based on a monochromatic light source, an interferometer attachment, and a metallurgical microscope can also be used for measuring step heights and surface irregularities with good sensitivity, precision, and accuracy (10-30 Å; more typically $\pm$ 35 Å).[28,81]

Current-noise measurements at high current densities can be applied to the detection of constrictions in thin metal films that are deposited over steps in dielectric layers. Localized defects in or caused by the underlying dielectric layer steps, such as sharp edges, microcracks, and surface irregularities are reflected in the current-noise level.[26,83]

Electron diffraction is a useful tool for identifying crystallites or crystalline imperfections of compounds on the dielectric film surface if they are present in sufficient quantity. The resulting diffraction ring diameters correspond to interplanar spacings in the crystal structure and serve as basis for identification of the compound. An example of the technique has been given in the section on SEM.

Electron microscopy is a well-established analytical technique for examining physical defects and microstructure in dielectric films with a resolution unsurpassed by any other method. Both surface-replica and transmission techniques have been used successfully for many years. Since sample preparation is rather tedious, the SEM is generally preferred for more routine inspection whenever possible. Recent advances in high-resolution transmission electron microscopy have made it possible to achieve magnifications up to 6×10^5 at the viewing screen, with resolution of fractional nanometers. Selected area diffraction and x-ray analysis can also be performed with modern electron microscopes.[84-86]

Radioactive tracers adsorbed from solutions on defect sites of dielectric surfaces can be used for decoration. In conjunction with autoradiography this relatively simple and specific technique offers an interesting possibility for marking the exact distribution of certain types of defects.[87]

Neutron-activation analysis[28,29] is another sensitive method available for identifying localized impurities in dielectric films, if combined with autoradiographic techniques to ascertain the spatial distribution of the resulting radioactive impurity elements. Energy spectrometry and half-life measurements of the radionuclides can be used for positive nuclear identification. Selective chemical etching of dielectric layers to expose activated particulate contaminants for autoradiographic analysis should make it possible to determine the depth distribution of localized impurities. The restrictions imposed by the radioactivation of unwanted film and substrate components, and the elaborate instrumental facilities required, are severe disadvantages of this potentially powerful technique.

Laser scanning internal photoemission is a very effective technique for studying the area distribution of sodium ions in thin silicon dioxide layers on silicon using a very small, high-intensity beam of ultraviolet light (He-Cd laser, 3250 Å). Area resolution is in the range of a few square micrometers. Determination of the area distribution of photoemission of electrons from silicon into SiO_2 permits detection of regions of alkali ion contamination as a lowering of the photoemission threshold energy. The laser scanning technique is also considered applicable to determination of localized regions in which immobile charge density (Q_{ss}) is lower than average, or in which the surface recombination velocity of minority carriers is higher than average.[88,89]

5. Conclusions

It is clear from the review presented above that a remarkable variety of useful analytical methods and techniques exists for detecting and characterizing localized imperfections in dielectric films. No single method satisfies all demands, and many of the techniques complement each other. A judicious application of a few of these methods for a given problem usually suffices to achieve the objectives.

The proper choice must be based on a number of considerations: Must the method be nondestructive? Is only detection of the defects required, or detection as well as compositional identification, and to what accuracy level? What range of area and depth resolution is needed? Can the substrate below the dielectric film be used for chemical attack or decoration? What is the expected defect density and how much of a defect enlargement factor is desired if one of the decoration methods is used?

Generally, the microscopic techniques including SEM are a good starting point. Decoration methods are especially useful if an enlarge-

ment of the defects is desired for visualization, photographic recording, or automated counting for statistical evaluation. Preferential chemical liquid etching is fast, simple, and definite for reliability testing of devices such as aluminum-metallized IC's The liquid-crystal technique is very attractive for nondestructive testing of device wafers. Electron-probe, Auger-probe, and especially ion-probe microanalysis methods are the methods of choice for compositional identification of particulate contaminants on a micrometer scale, offering truly amazing sensitivity.

The trend in the future in this field is undoubtedly in the direction of increasing sophistication of instrumental and automated techniques, with emphasis on nondestructive in-process control for microelectronic device production.

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Errata Notice

In the Sept. 1973 issue of *RCA Review*, the illustrations in Figs. 5 (p. 466) and 7 (p. 468) in the paper, "Space-Charge Instabilities in Transferred-Electron Devices," by B.S. Perlman are interchanged. The correct figures are given below.

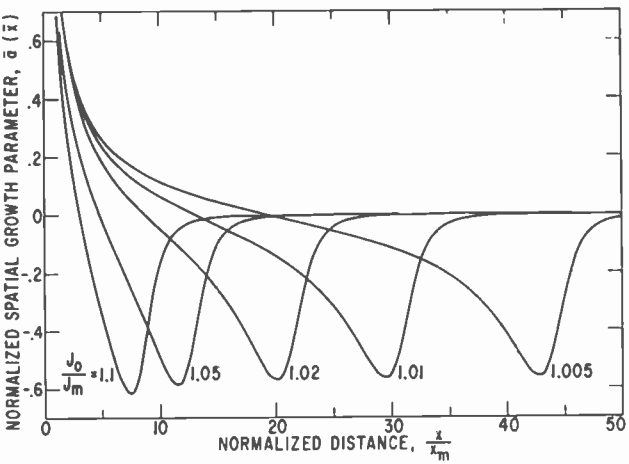

Fig. 5—Normalized growth parameter $\bar{\alpha}(\bar{x})$ as a function of the normalized distance from the (virtual) cathode for a uniformly doped device ($n_d(x) = n_d(0)$).

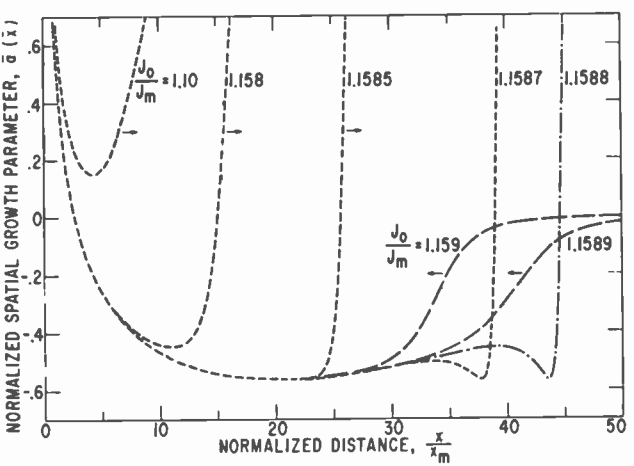

Fig. 7—Normalized growth parameter $\bar{\alpha}(\bar{x})$ as a function of the normalized distance from the (virtual) cathode for a device with a normalized length of 40 and 2:1 graded doping profile. Arrows indicate the progressive variation in $\bar{\alpha}(\bar{x})$ as the bias voltage is increased.

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A. S. Clorfeine graduated magna cum laude with a Bachelor's degree in electrical engineering from the College of the City of New York in 1959. Upon graduation he received the "Engineering Alumni of the City College Award in Electrical Engineering". He obtained his M.S. and Ph.D in electrical engineering from the Carnegie Institute of Technology (now Carnegie-Mellon University). Specific technical projects and accomplishments in which he has been involved include the first demonstrations of parametric amplification and millimeter-wave frequency conversion in superconductors, the concept of self-pumped parametric amplification in semiconductor diodes, the development of a theory for the Trapatt mode of oscillation, the establishment of a set of oscillator design rules, the attainment of record single-diode Trapatt L-band and S-band pulsed powers, and the development of cost-saving pulsing methods and lumped-element Trapatt oscillator and amplifier circuits at UHF and S-band frequencies. His work with superconductors resulted in an "Industrial Research-100" award. He has won or shared in three RCA Laboratories Achievement Awards.

Dr. Clorfeine is a member of Eta Kappa Nu, Tau Beta Pi, Sigma Xi, and the IEEE.

John J. Hughes joined ITT Federal Laboratories in 1950, where he worked in the Chemical Department, the Countermeasures Department, and the Microwave Tube Department. From 1958 to 1961 he was assigned to Associated Testing Laboratories as a representative of ITT, where he monitored and evaluated the environmental testing of microwave tubes. In 1962 he joined the RCA Manufacturing Division, Harrison, N. J., where he was a production foreman in the Microwave Tube Division. In 1963 he joined the Microwave Research Laboratory at RCA Laboratories, Princeton, N. J., where he has worked on plasma-tube studies, klystron design and integrated solid-state microwave techniques. He worked on the Blue Chip program at its inception and participated in the work on microstrip properties and the development of the integrated receiver.

Mr. Hughes is a member of the IEEE and is presently attending Middlesex County College.

R. D. Hughes joined RCA in 1933, working until 1938 in the Special Apparatus Department at Camden. At that time he was transferred to the Engineering and Research Department where he did television, sound, and radar development work. He moved to Princeton, upon the opening of the RCA Laboratories in 1942. He assisted in the development of the FM radio altimeter and other FM radar systems. Subsequent assignments in color-television transistor and electron-tube research followed. Since 1951, he has worked in the area of microwave research, including such areas as traveling-wave tubes, parametric devices, tunnel diodes, Hall-effect devices, superconducting devices, and most recently avalanche diodes. Mr. Hughes retired from RCA in June 1973.

S. T. Jolly received his B.Sc. degree in Metallurgy from the University of Wales in 1939. From 1940 to 1946, he served in the British Army. From 1946 to 1952, he was employed by EMI Ltd. supervising the Materials and Components Test and Evaluation Laboratory. Since 1953, he has been employed by RCA, initially as engineering leader responsible for the development of packaging hardware, power supplies, and magnetic head design used in the production of the Bizmac 301 and 501 computers. As manager of the Magnetic Head Design department from 1959 to 1963, he supervised the design and development of magnetic recording heads for professional audio, video, and digital recording, and assisted in the set up of associated production facilities. From 1963 to 1968, Mr. Jolly was an engineering group leader with RCA Defense Electronic Products, responsible for development work in computer memories, automated test equipment studies, and setting up a facility for the production of high resolution photomasks to be used in the manufacture of integrated-circuits. Mr. Jolly was the senior engineer responsible for initial design and process development for liquid-crystal displays. His present assignment is the development of epitaxial-growth processes and production of material for solid-state-microwave devices with the Microwave Technology Center, RCA Laboratories, Princeton, N. J.

Werner Kern received a certificate in Chemistry in 1944 from the University of Basle, Switzerland, and a diploma in chemical technology in 1946. He published a thesis on the chromatographic isolation and characterization of fluorescing polynuclear hydrocarbons which he discovered in soil. He was analytical research chemist with Hoffmann-LaRoche in Switzerland, and in 1948 transferred to their research division in New Jersey to develop new radiochemical methods. In 1955 he received an AB degree in Chemistry from Rutgers University and in 1958 joined Nuclear Corporation of America, where he became chief chemist directing research in nuclear and radiation chemistry.

He joined RCA Electronic Components in 1959 primarily to investigate semiconductor contamination and surface passivation by radiochemical methods. Since 1964 he has been at RCA Laboratories, where his activity has centered in semiconductor process research in silicon device passivation technology, new methods of chemical vapor deposition of dielectric films, and the development of associated analytical materials control methods.

Mr. Kern is a member of the American Chemical Society, the Electrochemical Society, the Research Honorary Society of Sigma Xi, and Geological Society of New Jersey, and is listed in American Men in Science. For his work in integrated-circuit process research, he received an RCA Achievement Award in 1966. Mr. Kern is the recipient of the T. D. Callinen Award for 1971 of the Dielectrics and Insulation Division of the Electrochemical Society in recognition of his pioneering work in chemical vapor deposition of glass films.

Richard J. Klensch received the BSEE degree from the University of Illinois in 1951. He did graduate work in the Electrical Engineering Department of Princeton University from 1952 to 1958. Mr. Klensch joined RCA Laboratories in 1952 to work with high-resolution radar and infrared detection devices. From 1954 to 1956, he served in the army as a radar instructor, returning to RCA Laboratories in 1956. Subsequently, he did research in the areas of microwave scanning antennas, time division multiplex systems, digital and analogue communications, and color television. In 1961, he participated in research leading to an advanced Naval Communications system, continuing this effort until 1966. From 1966 to 1967, he worked on new electronic half-tone generation techniques and CRT display systems. Since late 1971, Mr. Klensch has been investigating traffic safety control and microwave detection systems. He is a member of Sigma Xi and a senior member of the IEEE.

Ralph W. Klopfenstein received his B.S. in Electrical Engineering from the University of Washington (Seattle) in 1944. He subsequently studied Applied Mathematics at Iowa State University where he received the M.S. and Ph.D. degrees in 1951 and 1954, respectively. From 1943-46 he served in the United States Navy, completed the United States Navy Radio Material Program, and served as Radio Materiel Officer in the Pacific Fleet. He was employed by the RCA Victor Division, Camden, New Jersey, as an Electrical Engineer in 1948 where he worked on the development of high power filters and transmitting antennas for UHF and VHF television applications. Since 1953, Dr. Klopfenstein has been engaged in research at RCA Laboratories, Princeton, N.J., where he is a Fellow of the Technical Staff. From 1953-57 he was active in research in microwave and UHF filters and antennas. In 1957 he was named Head, Mathematical Services, with principal responsibilities in numerical analysis research and the deveopment of computer programs for applications in scientific problems. From 1962-63 he was on leave of absence and served as Director of the Computation Center and Professor of Mathematics at Iowa State University. Since 1963 he has been engaged in research related to the application of mathematics with a principal interest in the development of algorithms for the numerical solution of differential equations.

Dr. Klopfenstein is a member of the American Mathematical Society, Association or Computing Machinery, Institute of Electrical and Electronic Engineers, Mathematical Association of America, Society for Industrial and Applied Mathematics, and the Society of Sigma Xi.

Walter F. Kosonocky received the B.S. and M.S. degrees in electrical engineering from Newark College of Engineering, Newark, N. J., in 1955 and 1957, respectively, and the Sc.D. degree in engineering from Columbia University, New York, N. Y. in 1965. Since June 1955 he has been employed at RCA Laboratories, Princeton, N. J., where he has conducted research on application of new phenomena and new devices for information processing systems. This work has included ferrite memory systems, parametric digital devices, tunnel-diode circuits, tunnel-diode and transistor circuits, pattern-recognition systems, applications of lasers for digital systems (including a study of saturable absorbers for Q-switched lasers and semiconductor laser digital devices), optical hologram memory systems and page composition, optically controlled p-MOS circuits, and a liquid-crystal image converter. Presently he is working on the development and applications of charge-coupled devices.

Dr. Kosonocky is a member of Sigma Xi, Tau Beta Pi, Eta Kappa Nu, and a senior member of IEEE.

Peter A. Levine received the B.S. and M.A. degrees from Cornell University, Ithaca, N. Y., in 1967 and 1968, respectively. He joined RCA Laboratories, Princeton, N. J., in 1968, working in the area of Impatt and Trapatt diode microwave devices, with particular emphasis on noise properties. Most recently, he has been engaged in the development of charge-coupled devices.

Louis S. Napoli received his B.S. in 1959 and the M.S. in 1961 in Electrical Engineering, both from Rutgers University. He has pursued further studies in plasma physics at Princeton University and in electro-physics at the Polytechnic Institute of Brooklyn. Since joining the technical staff of RCA Laboratories in 1959, he has specialized in research relating to microwave phenomena in gaseous plasmas, solid-state microwave devices, and microwave integrated circuits. He is presently Head of the Microwave Components Technology Group in the Microwave Technology Center at RCA Laboratories. His work in collaboration with Dr. George Swartz on amplification at 24 GHz by the interaction of an electron beam with a cesium plasma was cited by Industrial Research Magazine as one of the 100 most important achievements in 1963. He is the recipient of RCA Laboratories Achievement Awards in 1963, 1965, and 1968.

Mr. Napoli is a member of Sigmi Xi, Tau Beta Pi, and Eta Kappa Nu, and IEEE.

S. Yegna Narayan received his B.Sc. (Honors) from the University of Delhi, India in 1959, his B.E. (Distinction) from the Indian Institute of Science, Bangalore, India, in 1962, and his M.S. and Ph.D. from Cornell University in 1964 and 1966, respectively. His graduate research dealt with the coupling of microwave energy to plasma systems. Since joining the staff of RCA Laboratories in 1966, Dr. Narayan has been working in the area of high-power epitaxial GaAs microwave devices. Most of his effort has been on the development of high-power cw X-band TEOs. He was the recipient of the RCA Laboratories Outstanding Achievement Award for the team effort in the development of GaAs transferred electron device technology. Dr. Narayan is now responsible for epitaxial GaAs growth in the Microwave Technology Center. He is an associate member of Sigma Xi, and a member of the American Physical Society.

H. John Prager is a graduate of the University of Vienna, Austria, and of the University of Michigan where he received an MSEE degree in 1940. He has been with RCA since 1943. His first assignment was with the RCA Electron Tube Division, Harrison, N. J., where he worked on the design and development of small power and receiving tubes. In 1959, he joined RCA Laboratories, Princeton, N. J., to perform research on solid-state microwave devices, such as varactors, tunnel diodes, optical devices, and avalanche diodes. In 1960, 1967, and 1972, he was co-recipient of RCA Achievement Awards for teamwork leading to the first tunnel-diode amplifier and down-converter, the first Trapatt diode oscillator, and greatly improved S-band diode amplifiers

Mr. Prager is a member of the IEEE.

Walter F. Reichert attended RCA Institutes in New York, where he received his certificate in the General Electronics Technology Course. He has attended Rutgers University, and has received his Associate degree in EE from Middlesex County College. Mr. Reichert has been employed at RCA Laboratories, Princeton, N. J., since 1961 as a Research Technician. During this time he has participated in experiments dealing with cesium recombination, double-stream amplifiers, crystal acoustics, surface-wave propagation in CdS, and GaAs Schottky-barrier diodes. At present he is working on development of GaAs field-effect transistors.

Paul H. Robinson graduated with a Bachelor of Arts in Chemistry, June 1951 from New York University College of Pure Arts and Science and received a Master Degree in Physical Chemistry for Polytechnic Institute of Brooklyn and the Massachusetts Institute of Technology in 1955. He was employed by M.I.T. as a staff member at Lincoln Laboratory from 1952-1959. While at Lincoln Laboratory he was part of a group which was first to determine the oxidation kinetics, thickness, and isosteric heat of adsorption of oxygen on atomically clean germanium surfaces after oxidation. This work was published and presented at the First Conference on Semiconductor Surfaces held in Philadelphia in 1956. He also worked on the electrochemical preparation of manogermane. From 1959 to 1962 he worked at Raytheon's Semiconductor Division Advanced Development Laboratories and was mainly involved with surface studies on silicon and silicon devices. He joined the research staff at RCA Laboratories in February 1962 and developed the closed-spaced technique for the vapor transport of germanium and III-V semiconductors. For the past 7 years he has worked on the epitaxial growth of silicon, silicon device structures, and the characterization of silicon on insulators. He was first to use the silane system for this purpose. He reported along with C. W. Mueller in 1964 the first MOS devices using these films. He also reported the first useful bipolar transistors on insulators using an all epitaxial approach and helped develop a technology for improving minority carrier lifetime in silicon on insulator films. He is a member of the American Chemical Society and the Electrochemical Society.

Jerome Rosen received his BSEE in 1969 and his MSEE in 1972, both from the Newark College of Engineering. From 1957 to the present, he has been engaged in research and development of microwave devices and subsystems in the frequency range 30 MHz to 40 GHz, including filters, couplers, discriminators, ferrite phase shifters, diode phase shifters, YIG filters, "lumped element" equivalents of microwave hybrids for VHF, and an Instantaneous Frequency Measurement Receiver (IFM). Currently, he is engaged in the development of a medium-gain, omnidirectional, coaxial, linear array antenna at X-band; a self-mixing X-band doppler radar for automobiles; a microstrip transmitter for the electronic signpost Automatic Vehicle Monitoring (AVM) system; and an integrated dual frequency antenna and low-power doubler for the electronic tag of the microwave Automatic Vehicle Identification (AVI) system. Mr. Rosen is a member of the IEEE Professional Group on Microwave Theory and Techniques.

Harold Staras received his B.S. from C.C.N.Y. in 1944, his M.S. from N.Y.U. in 1948, and his Ph.D. from the University of Maryland in 1955. Dr. Staras has had over 25 years of experience in research and development, primarily in areas relating to radio propagation, communications, and radar. He played an instrumental role in the development of tropospscatter in the 1950's. In his early days at RCA, which he joined in 1954, he worked on many government programs and examined among other things, an island as a natural VLF slot antenna, dipole characteristics in a magnetoplasma, the effect of high altitude nuclear explosions on communication systems, and the effect of rough surfaces and dense planetary atmospheres on data communication systems having moving terminals. As Head of Radio Systems Research at RCA Laboratories, analytic and experimental, he directed studies in specialized microwave communication and radar systems. These included an automatic vehicle location system, a radar immune to blinding and clutter for use in automatic braking, a microwave automatic vehicle identification system, and a microwave system for airport ground traffic control. He is currently engaged in system studies involving communication satellites.

During 1961-62, Dr. Staras was a Guggenheim Fellow and visiting professor at the Technion-Israel Institute of Technology. He is a senior member of IEEE and is also a member of several study groups of the CCIR and Commission II of URSI.

Chainulu L. Upadhyayula received the B.Sc. degree in Physics and the M.Sc. in Applied Physics from Andhra University, India, in 1955 and 1958, respectively, and the Ph.D. in Engineering from Brown University in 1968. During 1958-59, he was a trainee in the Atomic Energy Establishment, Bombay, India. From 1959 to 1964, he worked in the Electronics Division of the Atomic Energy Establishment. His work was in the area of nuclear electronic instrumentation. From 1964 to 1967, Dr. Upadhyayula was a research assistant and teaching assistant in engineering at Brown University where he was engaged in the study of electrical transport properties of semiconductors. During 1968-69, he was a Post Doctoral Fellow in Engineering at Brown University studying tunneling through superconducting metal-insulator-metal structures at cryogenic temperatures. Dr. Upadhyayula joined the RCA Microwave Technology Center at the David Sarnoff Research Center in Princeton, N. J., in 1969 and is presently concerned with semiconductor devices and device physics.

In 1970, Dr. Upadhyayula was a co-recipient of an RCA Laboratories Outstanding Achievement Award for a team effort in the development of GaAs transferred electron amplifiers. He is a member of Sigma Xi and the IEEE.

Richard D. Wance attended Pennsylvania State University for two years prior to joining RCA Laboratories in 1956. Since then, he has worked on projects involving impact ionization, plasma oscillations in semiconductors, close-spaced transport of semiconductor materials, epitaxial growth of silicon on insulators, and epitaxial growth of silicon for power devices. Mr. Wance is presently working in the Materials Research Laboratory doing spreading resistance analysis of epitaxial layers and related power device structures.

Roland K. Wehner received the Physics Diploma in 1961 and the PhD degree in 1964 from the University of Freiburg, Germany. After two and a half years of postdoctoral research at the University of Frankfurt/M., he joined in 1967 the technical staff of Laboratories RCA, Zürich. Dr. Wehner has been working on topics of solid-state theory, such as infrared absorption and light scattering by phonons in dielectric crystals. He has carried out studies of phonon–phonon interaction in sound absorption and heat transport theory. In 1973, he spent 9 months at the RCA Laboratories in Princeton, where he was engaged in work on the dynamics of surfaces of elastic media and electrostatic surface forces. Dr. Wehner is currently concerned with studies of structural phase transitions. He is a member of the Zürich, Swiss, German, European, and American Physical Societies.

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