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automated testing

RCA Engineer

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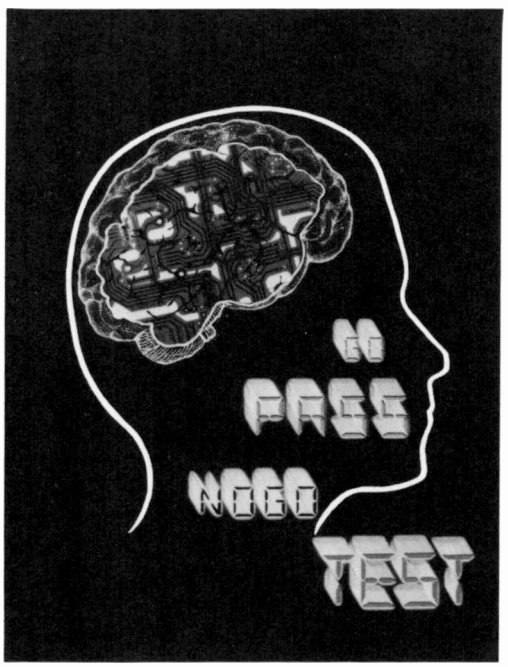

Cover design by Robert Fredrickson
Automated Systems Division,
Burlington, Mass.

□ To disseminate to RCA engineers technical information of professional value □ To publish in an appropriate manner important technical developments at RCA, and the role of the engineer □ To serve as a medium of interchange of technical information among various groups at RCA □ To create a community of engineering interest within the company by stressing the interrelated nature of all contributions □ To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field □ To provide a convenient means by which the RCA engineer may review professional work before associates and engineering management □ To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

Automated testing: An essential part of RCA's future

When one considers that 30 years ago the primary use of automated testing was for continuity tests of cable and wiring harnesses, the scope of contemporary automated testing applications is most impressive. Automated testing has spawned its own version of such disciplines as application software development, system architecture, and test instrumentation. Automated testing is now integral to the manufacturing process—a check on the integrated circuit, the board, the subassembly, and the final product before it reaches the customer. Product acceptance, and therefore product sales, are a function of testing integrity as well as fundamental design. In the factory, automated test provides quality feedback in the near real-time. In the field, automated testing cuts the downtime for fault detection, diagnosis and repair of complex systems—systems that would be impossible to maintain without automated testing.

Automated test engineers have known something about their field that has been only recently discovered by their fellow engineers: Automated testing is pervasive. There is no product, no discipline, no technology that is not a tool or a challenge for automated test engineers. They apply operations analysis to model and optimize the potential application. They call upon advanced system development tools to build test language compilers and operating systems for distributed-architecture automated test equipment. Test applications range from consumer electronics to turbine engines to laser designators. The most promising near-term payoff in the field of artificial intelligence is expert systems applied to diagnostics. As part of automated testing expert systems are on-line now, providing diagnostic support to computer field engineers and monitoring power generating stations.

Automated testing is forever in transition, and the watchword for 1985 appears to be "integration." Testing functions are being integrated with the prime system design so that monitoring and diagnostics are built in. Testing functions are also being integrated with the manufacturing and maintenance processes. The dividing line between operation and test, between prime and test equipment becomes blurred and disappears. It's an exciting time to be working in automated testing.

David M. Priestly

David M. Priestly
Director, Automatic Test Systems
Automated Systems

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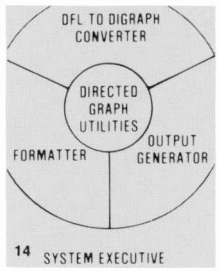
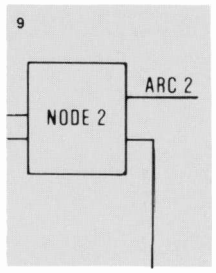
■ **Carver:** *"Built-in test and testability at the chip, board, subassembly, and system level will finally become a reality because they are needed in the manufacturing process."*

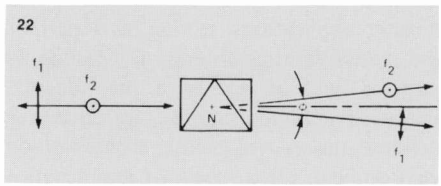
■ **Krieger:** *". . . using AI concepts for guidance rather than as a framework, we proposed and developed a data flow network approach to Level I (fault detection) vehicle diagnostics."*

■ **Glenny/Wong:** *"Automated flowchart generation is a computerized process for creating a flowchart representation from the source code of a program."*





■ **Fuhr:** *"The automation of the laser measurement system makes it possible to calibrate the scanner immediately prior to any antenna scan . . ."*

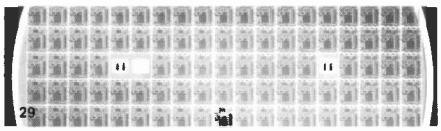


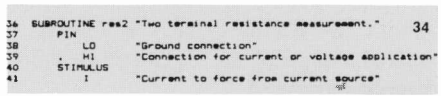
■ **Bösenberg/Goldsmith:** *"The prime function of parametric testing in an integrated circuit manufacturing environment is to ensure that the complicated fabrication process used to produce the integrated circuit has been completed satisfactorily."*

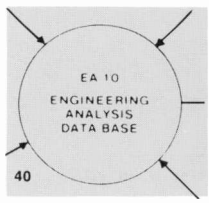
■ **Brehm:** *"The goals of the system design are met by hiding the tricky, tedious, difficult, and error prone aspects from the experimenter."*

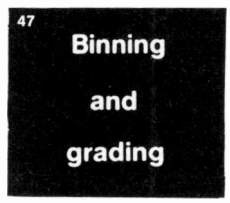
■ **McCarty:** *"Many factors were considered in making the decision to purchase an engineering analysis software package from a vendor."*

■ **Price:** *"There are many wafer parameters measured during processing, but WET measurements represent the result of all processing steps and their complex interactions."*









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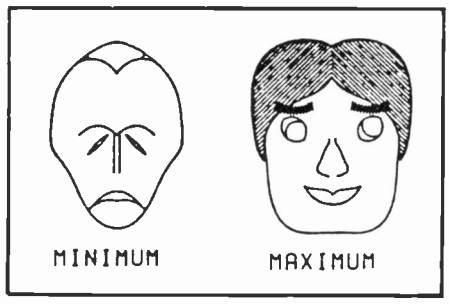

O.T. Carver

ATE trends into the 90s

The two primary areas of change in the next generation of ATE will be the user/maintainer's interaction with the system and the ATE's integration within the parent application.

Abstract: *There are two broad automatic testing applications: (1) testing within the manufacturing process where the objective is product quality assurance, and (2) testing within the maintenance process where the objective is to return failed items to operation. As ATE market drivers, these two applications have stimulated divergence in system design. But the divergence will become convergence as a result of what's happening in prime equipment design rather than by deliberate planning on the part of ATE developers. Built-in test and testability at the chip, board, subassembly, and system level will finally become a reality because they are needed in the manufacturing process.*

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Automatic test systems now serve in two distinct applications: testing as a part of the manufacturing process, and testing as part of field service or a maintenance process. Manufacturing test objectives are product quality and yield in a batch mode environment. Field service or maintenance testing objectives are fault isolation as the first step in repair and return to operation. The service test environment is random arrival of tested items by type. Manufacturing test anticipates assembly faults such as missing parts and solder splash shorts. Service test assumes that the item once worked and problems are caused by failed components.

The different test objectives and test environments have shaped two diverging automatic test systems approaches. Manufacturing tests incorporate in-circuit techniques, where a fixture provides test access to nodes and circuit paths on the board. In-circuit tests are primarily static, and test procedures are automatically derived from circuit topography. Field service tests are aimed at operational faults and depend on functional tests that exercise the unit under test (UUT) in almost the same way the item is stressed in normal operation. Maintenance diagnostics require months to develop and validate. Manufacturing testers incorporate test item handlers and simple robotics to take advantage of throughput gains in the batch mode. Maintenance testers are likely to involve instructed probing by the ATE operator. Manufacturing test programs are more likely to be coupled to CAD data; maintenance testing is likely to be coupled to the logistic system.

Both test approaches are being challenged by higher operating speeds and the longer test requirements of LSI/VLSI populated boards and modules as more and more functions are packaged in the same volume. This means test functions become more removed from direct, or even implied, access through external ports.

Changes underway

There is a pervasive change underway in prime equipment design that will put manufacturing and maintenance on a converging, rather than diverging, path. Design for testability has long been a designated solution for problems of mismatch between the test system and the tested item. If the prime designer would develop a test approach and let that test approach shape the design, the end product would reduce the need for complicated interface devices and cumbersome test techniques that are now developed after the fact by the ATE applications test program designer. The designated solution has failed because there is a lack of real incentive for the prime equipment designer to help solve the maintainer's problems.

Herein lies a basis for change. With large scale integration and embedded microprocessing at lower and lower functional levels, conventional test techniques are inadequate for development and manufacturing needs. In order to test the chip, test capability is designed into the chip. Ten to fifteen percent of the total chip area is typically assigned to test functions. This percentage of a chip with several hundred thousand transistors represents significant test capability. More test functions on the chip means less test system complexity off the chip—a good trade-off. Test capability at the lowest level, the chip, makes it easier to provide built-in-test (BIT) at the printed circuit board (PCB) and module levels. This is exactly the approach espoused for years by test system developers and test software designers. Testability will become a reality because the incentive is payoff in design and manufacture. The benefit to service and maintenance testing will be equally dramatic, although it comes as a gratuitous secondary effect.

Impact of BIT on ATE

As an indication of the BIT impact on ATE, consider the experience with avionics on the Boeing 757/767 aircraft.[1] Extensive BIT was introduced in the slat electronics unit. Table I is a comparison of application test program characteristics for the electronics unit with and without

Table I. *757 slat electronics unit test program characteristics*

	Without BIT	With BIT
Number of tests	750	182
Lines of ATLAS	9000	4500
Run time (min.)	90	20
Hours to produce	9400	2300

BIT. Test programs were written for the same ATE. Note that the time to run the tests, a recurring maintenance cost, was reduced by a factor of about 4 to 1, so the payoff was not limited to the development cost.

There is another significant trend with potential important ATE impact as a result of the confluence of several other ideas. The trend is the winnowing of maintenance levels to service/repair operations in the user location and maintenance operations at a depot or factory. "Repair" in this context can be as simple as pull and replacement of plug-in modules or boards. In the military, each service has an intermediate level of maintenance, populated by test and repair shops, supporting supply, inventory control and administration resources. There is growing incentive to eliminate or reduce the large investment and on-going logistics cost of supporting the intermediate maintenance function.

These evolutionary trends are illustrated in Fig. 1. Tester technology spans the ATE architecture, subsystem implementation, and test techniques. These will fuse into a generic test configuration with in-circuit, functional, analog, digital, and hybrid capabilities. It will be linked to functional levels above testing—assembly, test and rework, and field maintenance.

Off-line maintenance today is multilayered. The user recognizes a system problem, perhaps aided by system self monitoring, and performs first-level maintenance. This action may introduce a repairable, replaced item into a logistic channel on its way to another maintenance level. The user's action could also be a call to another maintenance level for help. The repairable item may itself be repaired by introducing another repairable item into the queue awaiting maintenance at another, higher maintenance level.

Maintenance levels are populated with testers, spare parts, repair benches, people, and procedures. They are very expensive. They are interconnected by logistic pipelines that are also very expensive—and they leak. Hence the incentive to merge maintenance levels and the appeal of an effective built-in test that diagnoses to a third or fourth level.

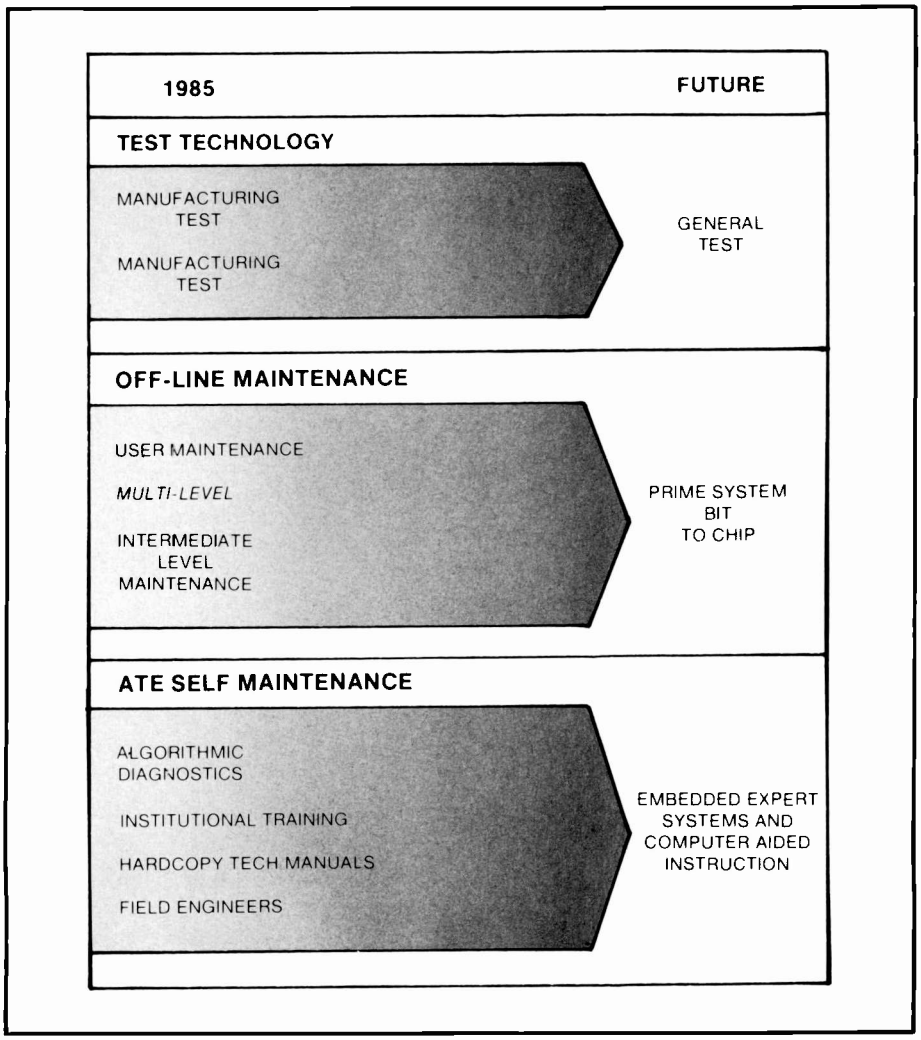

Fig. 1. *Evolutionary trends in ATE.*

ATE self maintenance, now an amalgam of diagnostic software, technicians, technical manuals, and access to a field engineer, will evolve toward not only BIT but embedded expert systems and intelligent computer-aided training.

The DoD has a farsighted view of the interrelation between test equipment, technicians, repairables handling, expendables transportation, etc., and the need for new technology in these areas. Under the name of Logistics R&D, there are specific technology needs that are targeted and given priority in the allocation of resources.

A priority Air Force objective is the reduction or elimination of intermediate-level maintenance. A demonstration project, know as Pave Splinter, has been initiated. The approach is to incorporate adequate testability, BIT, and reliability improvements in an avionics subsystem to eliminate the need for an intermediate shop's resources.

The mechanism for integrating the maintenance levels is elimination of the intermediate workload by reducing failure rates and by embedding test functions in the prime system. Historically, failure rate improvement has come from most of the new technology thrusts, especially large-scale integration.

Integration also will occur in another dimension. As previously discussed, manufacturing test software will become more closely coupled with CAD data. Test programs will make use of circuit design tools and computer-generated data developed during the design process. An analogous trend can be expected in service/maintenance testing. Automatic test will be linked with such functions as:

- **Workload scheduling.** Incoming test items will be bar-code scanned and entered into workload pool. The ATE will maintain, through its internal survey and monitor functions, a status of its test capability in terms of specific

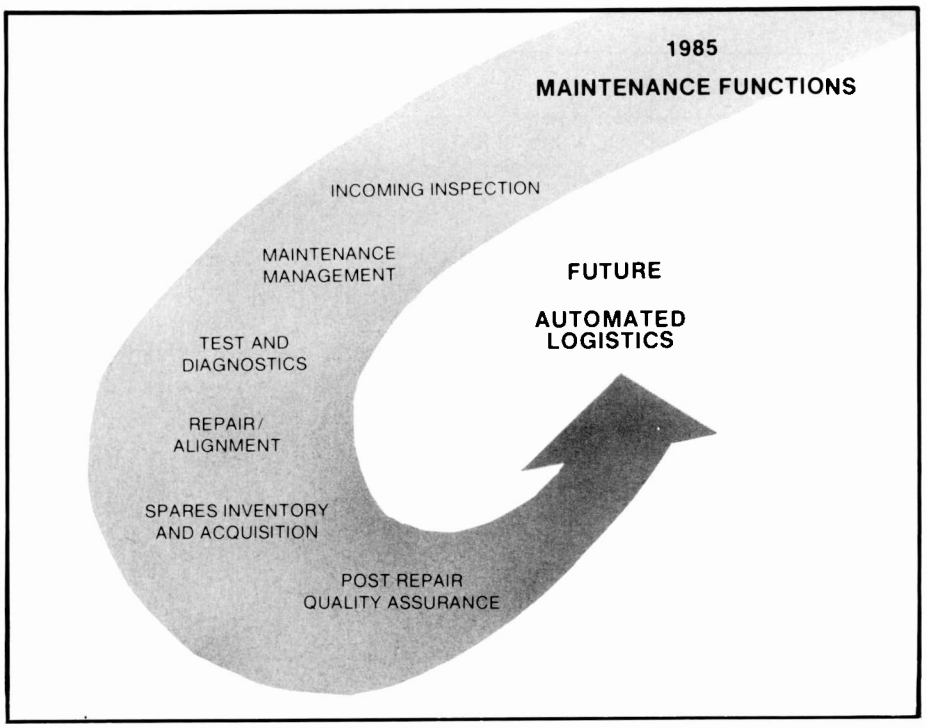

Fig. 2. *The future of ATE.*

units under test (UUT) that it is prepared to test. For example, if one channel of its dual pulse generator is not functional, the system monitor will scan the UUT list and delete those units requiring the dual channel pulse stimulus. The system monitor also tracks status of interface connection devices, cables, and test application software. Individual UUT test time and status of current testing are also known. Triggered by the UUT identification read by the bar code scanner, an increment of test workload will enter the system and all the above information can be provided to the maintenance manager. This information would be a basis for workload assignment to test stations and to test operators. Decisions to batch, assign priorities, or tailor a test station workload to digital PCBs or rf units can be made and updated for greatest productivity or for best response time to the customer.

- **Real-time inventory control**. Automated diagnosis provides the first indication of a failed item. This information, networked electronically with the processor that tracks items in stock, can determine whether a spare is available and, if so, designate a spare to a specific repair task and then update the spares available inventory. As part of inventory control, replacement spares requisitions can be initiated, accumulated, and parts can be ordered according to logistic stock rules.
- **Maintenance management**. Automated diagnosis can also provide repair manhour estimates, examine a priority queue, and schedule repairs according to need, spare parts availability, and repair resource availability. Maintenance history for each type of unit under test can be tracked, along with ATE test station status, and workload trends over time versus prime system type. Projections of workload and test station availability can be provided for a new mix of prime systems to be supported, answering such questions as "what happens to turnaround time if the number of systems that my test station supports is doubled?" ATE system software will be enhanced by expert systems that assist the operator in system self-test and restore-to-service. These systems will be highly interactive, and will adapt to the increasing skills the user gains through experience. The resident expert system will "learn" from ATE failure history, with the knowledge base and inference system updated and even tailored to the parent ATE.

The integration of maintenance functions is illustrated in Fig. 2. As the tester is seen today, it interacts with the operator/maintainer, with the item under test, the test software, the interface device, and the instruction manuals. Its function is constrained to test and diagnosis. But the end objective is maintenance, and this involves all the functions just described. Today, these functions interact through manually generated data transfers, largely on paper. In automated logistics, the ATE will look more like a maintenance subsystem, less like stand alone test equipment.

Prime system technology that might stress ATE capability will appear in four areas:

(1) High-speed, high-density large-scale integration as typified by the DoD VHSIC program.

(2) Millimeter wave radar and communications systems. The frequency increases are likely to come in three categories: 1) up to about 45 GHz, 2) from 45 to 100

Tom Carver holds a BSEE and an MEd, and has been involved in automatic test programs at RCA since 1956. His program experience includes the Multi-Purpose Test Equipment (MPTE), an early modular, general-purpose ATE built for the Army, fundamental studies to develop algorithms for automatic test point location, and support for modeling tools used to evaluate alternative maintenance concepts. Current programs include Post Deployment Software Support for the AN/USM-410, long range AN/USM-410 product improvements, and AI/ATE applications.

Mr. Carver has served on the AUTOTESTCON Board of Directors, is a member of the IEEE Instrumentation and Measurement Society Administrative Committee, and a member of the NSIA-ATE Committee.

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GHz, and 3) beyond 100 GHz. There are a number of systems in use or in development in the first category and prototyping is underway in the other two.

(3) Complex modulation schemes dictated by secure communications and frequency spectrum crowding. These systems are operational.

(4) Enhanced ATE capability into such hybrid areas as electro-optics; ATE applications will expand from current, rather modest use in electro-optics test.

Conclusion

The differences between factory ATE and off-line maintenance ATE will disappear. Maintenance testers will support in-circuit test fixtures. Both types of ATE will depend on prime equipment BIT to simplify test requirements.

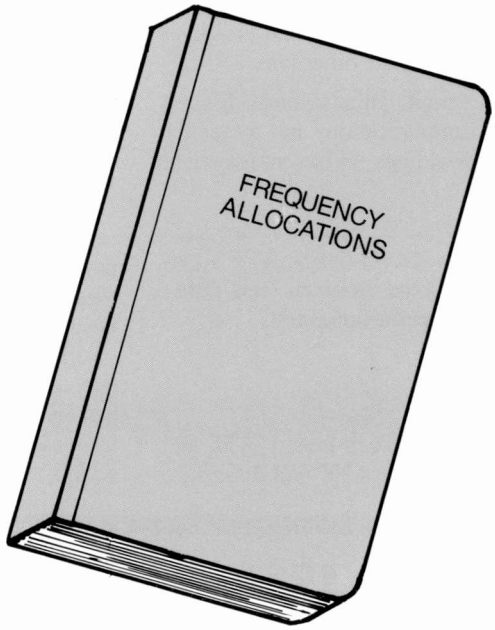
Effective built-in test will be commonplace, being "designed in" because of incentives for effective testing during development and manufacture. In the field, ATE will merge and be used with the prime equipment as built-in maintenance processors operating over a dedicated maintenance bus that tracks status and diagnostics down to the individual chip.

ATE will ride the fast-paced computer technology horse, providing ATE controllers with more processing power at less cost in reduced space. This processing power will be distributed into each functional block. Architecture will continue the trend toward distributed processing and the use of standard buses. The systems will incorporate expert systems to supplement conventional algorithmic diagnostics. Embedded intelligent computer aided instruction will adapt to the needs and skill level of the individual operator. Technical manuals will disappear.

References

1. J.J. Seli, "Automatic Test System Response C I Future Needs," *Proceedings*, 1984 Conference on Supporting Weapon System Technology Through the 1990's (August 14-16, 1984)

New book available: Frequency Allocations



The newest edition of *Frequency Allocations* has just been published by the RCA Frequency Bureau. This attractive pocket-sized book contains all international and U.S. allocations and regulations up to November 1984, including the results of the 1979 and 1983 World and Regional Administrative Radio Conferences.

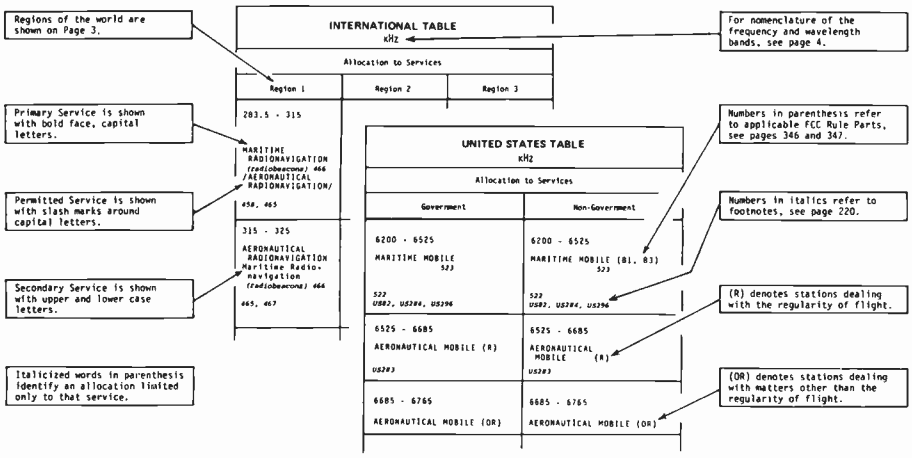
This new edition features:

- Worldwide allocations for all frequencies between 9 kHz and 300 GHz. A world map shows each of the ITU Regions.
- U.S. Government and non-Government allocations printed on studies of potential radio interference.
- Radio service assignments listed by Primary, Secondary and Permitted uses in each frequency band.
- A complete set of international, U.S. domestic, U.S. Government and U.S. non-Government footnotes that help explain or define the limon certain allocations.
- Other sections identify each frequency and wavelength band, provide the title for each FCC Rule Part, explain the new emission designations, and list all U.S. TV broadcast channel frequencies, standard frequencies, and special industrial, scientific and medical frequency bands.

For the system design engineer and engineering manager, this reference may be invaluable. It is the only publication we have seen that contains such often needed information. Its small size and new flexible binding are perfect for carrying in a jacket pocket or tucking away in a briefcase.

RCA employees may purchase a copy of *Frequency Allocations* for $4.00 (regular price is $5.00) through **Mrs. Dora Mineo, RCA Frequency Bureau, One Independence Way, Princeton, N.J.** Make checks payable to RCA Corporation. Non-RCA purchasers should address Mrs. Mineo at P.O. Box 2023, Princeton, N.J. 08540. For further information about placing company orders or quantity orders (10 or more), please call Mrs. Mineo at **Tacnet 254-9566 or (609) 734-9566.**

Guide to the 215-page frequency allocation table.



D.A. Krieger

Artificial intelligence concepts applied to ATE software

New user demands on ATE impel the diagnostic engineer to explore new ways to overcome the limitations on conventional diagnostic software.

Abstract: *There is growing interest in designing ATE systems that are easier to use, more economical to program, and capable of handling multiple faults in the unit under test (UUT). This has led us to examine and combine a number of advanced software concepts that enhance the diagnostic performance of our small portable test set (STE-M1/FVS). The techniques and theories of artificial intelligence (AI) suggested much of our approach, and the format of a data flow network was used to implement the top level test strategy. The data flow representation satisfies the criteria for a good AI representation, yet provides for efficient computation with a minimum of resources. This paper reports on an enhanced software development project completed at RCA Automated Systems.*

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The STE-M1/FVS is a microprocessor-based, software-driven portable test set. It is designed to thoroughly test the functional and operational integrity of the Abrams M1 Tank and the Bradley Fighting Vehicle (BFV). When a problem in the vehicle is detected it will be fault-isolated to the level of a cable or line replaceable unit (LRU).

The present software provides what is, in effect, an automated diagnostic flow chart. A subsystem test initially instructs the maintenance mechanic to configure the vehicle into a known state. Then it takes a measurement and compares its value to a predefined set of limits. On the basis of this comparison, the test either continues its Level I fault detection task or branches into Level II fault isolation routines. Level I refers to measurements made at the test connectors of the vehicle, which serve no function other than test point connection. Level II refers to measurements made with "T" shaped adapter hook-ups, which permit the test set to trace signals that are passed from an electronic box, through a cable, to another electronic box or device. The unidirectional, tree traversing nature of the approach means that diagnosis stops at the first isolated fault. Thus minor faults can mask the detection of major problems.

A corrective solution allows the Level I process to continue as far as possible, collecting and storing pass/fail information but delaying Level II fault isolation procedures until all the contextually related information has been collected.

Additionally, the present diagnostic software obscures diagnostic knowledge that is dispersed throughout a flow chart. This makes maintenance and modifications of existing software very difficult because the meaning of a particular piece of code lies deeply buried in the entire structure of the test. In general, flow charts do a good job describing a program, but they are a poor representation for diagnostic knowledge. The overall test strategy remains hidden by the representation.

A clear representation is important for practical, not simply for aesthetic reasons, because it enables the diagnostician to configure and debug diagnostic knowledge rather than diagnostic programs. It facilitates creative problem solving by human beings. One branch of AI deals with the development of knowledge-based expert systems. These systems employ symbolic manipulation (as opposed to standard numerical algorithms) to solve problems that require uniquely human reasoning abilities. Since these systems manipulate symbols instead of numbers, the development of powerful new forms of knowledge representation is critical to success. Patrick Winston,[1] a pioneer in this area, gives the following list of desiderata for good representations:

- They make important things explicit.
- They expose natural constraints.
- They are complete.
- They are concise.
- They are understandable.
- They facilitate computation.
- They suppress detail. Rarely-used information is kept out of sight but is still accessible.
- They are computable by existing procedures.

With these things in mind, and using AI concepts for guidance rather than as a framework, we proposed and developed a Data Flow Network approach to Level I (fault detection) vehicle diagnostics. This approach allows maximum vehicle information to be quickly collected and efficiently stored, deferring the Level II fault isolation process until all possible relevant vehicle information is collected. It also ful-

A role for artificial intelligence in ATE

Research work in the artificial intelligence (AI) field has been widely reported on within the past two years, but the practical applications remain few and highly specialized. Do you really need exotic programing languages encoded on machines with super speed and untold memory banks for practical uses of AI? Can you really expand AI past the game playing stages, beyond the "if-then-else" rules implementation of an expert system? These are the practical questions that need to be addressed when AI is being discussed.

At RCA's vehicle test systems engineering group, these are far more than academic questions. Since the mid 1970s we have built microprocessor test sets that fault-diagnose Army vehicles, with portable "suitcase" hardware (simplified test equipment) that the Army mechanic carries up to or into the truck, jeep, or armored vehicle. Our test systems face many of the problems that are now the focus of AI development. These test systems lack stimulus or means to manipulate vehicle and weapon system controls, and therefore a constant dialogue with the operator/mechanic is necessary. This is accomplished by using a terse, 40-character display on a hand-held set communicator. Expert troubleshooting diagnostics are encoded in the test set, and only "yes/no" responses are expected from the mechanic observing vehicle conditions. The problems we experience with field use and field acceptance of the test set appear to be suitable candidates for AI solutions. What are these problems, and what have we learned about the potential for AI?

We know that our operators (mechanics) get bored following long sequences of terse messages ("turn on turret power", "press and hold palm switch"). We realize that the test set tells them nothing at all about the progress of the test until the very end. Successful AI expert systems all use (or have added) features to explain to the user what the system has concluded, what it has done, and why. Those AI systems interface with reasonably skilled technical personnel, however; we find it difficult to relate the internal conditions of electronic systems to mechanics who are not proficient in reading schematics (or are not given schematics).

We know that our diagnostic test logic was both designed and tested on the basis of single faults. Army vehicles are not always repaired on the immediate detection of failure conditions, because the vehicle may still serve useful and needed functions. Testing in the presence of multiple faults creates several problems:

- Diagnostics valid with single faults may fail with multiple faults.
- The mechanic may be confused or frustrated by "finding" a different fault than the one he wanted to fix.
- Discovery and then fixing faults one at a time prolongs the overall repair time. Most users would like to find all faults with one pass.
- Conventional diagnostics can rarely continue to test after finding the first fault condition in the test sequence, because subsequent test logic relies on the condition of the preceding results.

The article by Dave Krieger describes what we are doing to improve the format and content of our programmed test logic, to improve the diagnostic accuracy of the test set, and enhance its acceptance to the user. What he describes may not look like AI. But there is an AI influence, and it was AI concepts that led us to our present position. We also realize the potential and need for further enhancements, and we expect that AI will again provide invaluable guidance.

When I look at his "dependency diagram" and "local expert" modules, I realize that nothing really new is embodied, only the means of representation. But what a difference that representation makes. Previous diagnostic logic spread evaluation of transfer functions throughout the test. Krieger has brought them into his local expert cluster. He can now represent the flowchart logic at a higher level. This is an excellent improvement for the designers and maintainers of the software, and it may be especially beneficial for the test set operator/ mechanic. For the first time, we may be able to tell the user what is happening in terms of "hand stations have malfunction", or "power distribution is OK", because of having clustered the evaluation of functions recognizable to the user.

More important, the test strategy is changed. Faults are detected and noted (pass/fail flags), but fault isolation is postponed. The new style test is designed to continue testing after the detection of faults, and it continues to evaluate the performance of "local expert" functions

fills most of the aforementioned criteria for a clear representation.

Data flow

Figure 1 presents, in the most general terms, the conventions we adopted for our data flow model. Basically, it is a directed graph. Each node in the graph is an independent module of diagnostic logic that corresponds to the constellation of hardware that makes up a functional subsystem. This we call a local expert. Whenever possible, it can test its designated subsystem independently from other local experts. The nodes are connected to one another via arcs. After a local expert executes, it sets its output arc either logic true or false depending, in part, on how far a set of subsystem measurements differ from the mode. The state of these arcs can enable or inhibit the execution of other nodes (local experts). Referring to Fig. 1, when node 1 executes, it sets arc 1 either logic true or false. If arc 1 is

until all permissable tests have been performed. At that time, the operator/mechanic can be notified of all malfunction conditions, although specific faulty replaceable components or cables may not yet be isolated. Fault isolation can continue at the operator's discretion until all faulty components are pinpointed. This should please users, because they can exercise decisions. In the future, I expect we will add intelligent guidance, advise users of the time and resources they may need to make the repairs, and even how to circumvent some of the problems.

Krieger's implementation runs on the same microprocessor test set that is currently fielded, using the same operating system, source code, and software development resources. Other than a few new measurement and storage constructs, the only thing new is the organization and strategy. However, we realize that the next steps may require significant augmentations. A larger, graphic set communicator will be needed to convey more meaningful information to the user. More memory and faster execution may be needed to search, hypothesize, and even learn and adapt. New utilities will be needed to support the development, documentation, and validation of the future enhancements.

I suspect that when we bring such new concepts into practical implementation, we will once more look at the results and say, "but it's not really AI."

R. E. Hartwell
RCA Automated Systems
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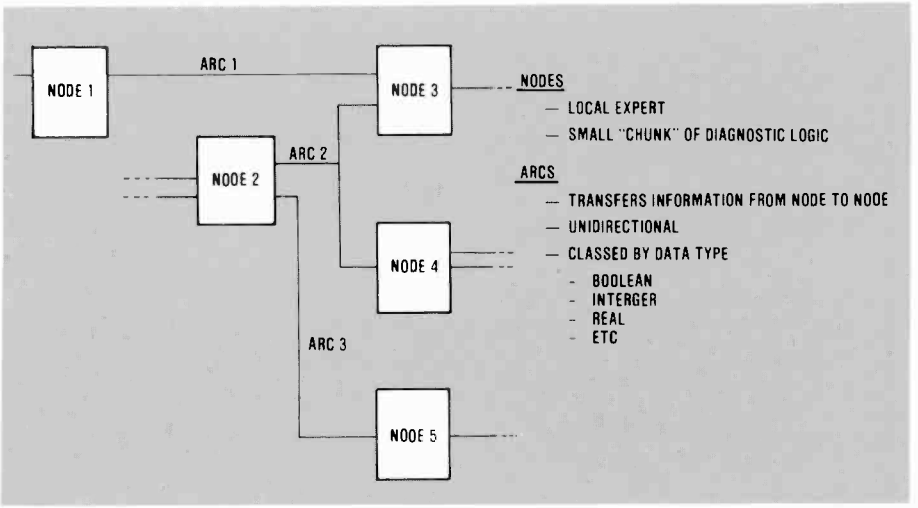

Fig. 1. *A generic data flow graph.*

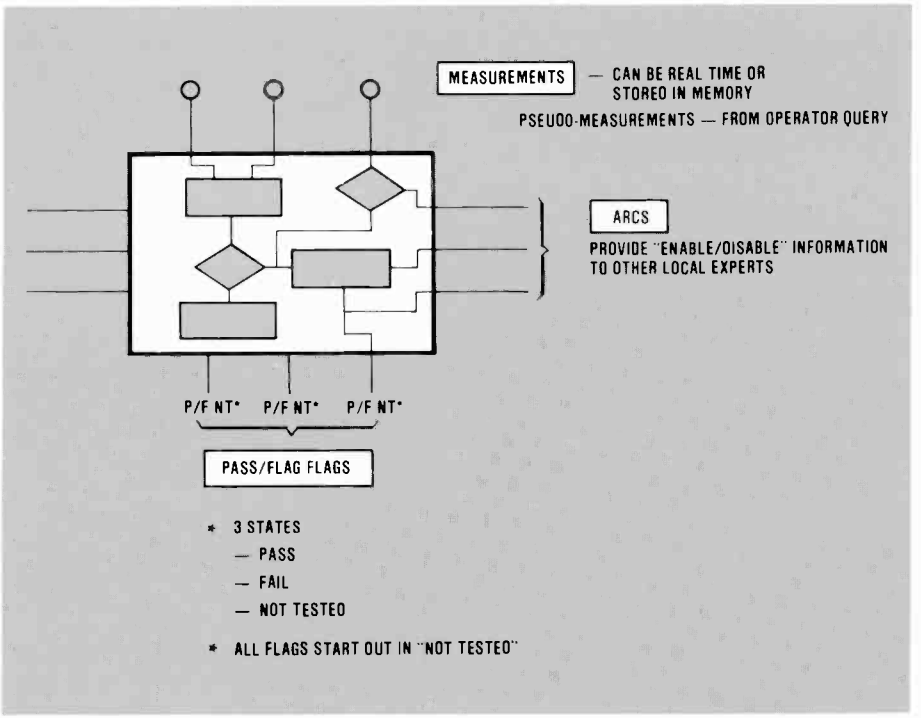

Fig. 2. *The layout of a typical node.*

logic true and arc 2 from node 2 is logic true, node 3 can execute. If arc 1 is logic false but arc 2 is logic true, node 3 is inhibited but node 4 is still enabled. Thus, regardless of the operational condition of the vehicle, all the logic that can execute does. This yields maximum vehicle information during Level I testing. Figures 1 and 2 show the conventions and terminology adopted for our data flow representation.

After a node's logic executes, one or more pass/fail flags is set (not to be confused with an output arc). This reflects whether a hardware entity meets its performance requirements or, in another sense, if its transfer function (input to output) is satisfactory. These results are stored for later use by the fault isolation routines. The logic that sets the output arcs determines if continued testing along a network path is possible in spite of a detected discrepancy between the pass/fail limits and the measurement.

For example, if the potentiometer that provides the speed reference signal to the traverse servo is out of tolerance, its corresponding fail flag is set. However, another set of logic within the local expert determines the state of its output arc. Basically, the local expert answers the question, "Is the potentiometer so far out of adjustment that nothing can be learned about the rest of the servo?"

As the test proceeds, local experts execute their diagnostic logic and put their results in logically encoded results registers (Fig. 4). At the end of the test, these registers are examined by the test manager, the top level of software, and a fault isolation strategy is initiated. From symptoms and

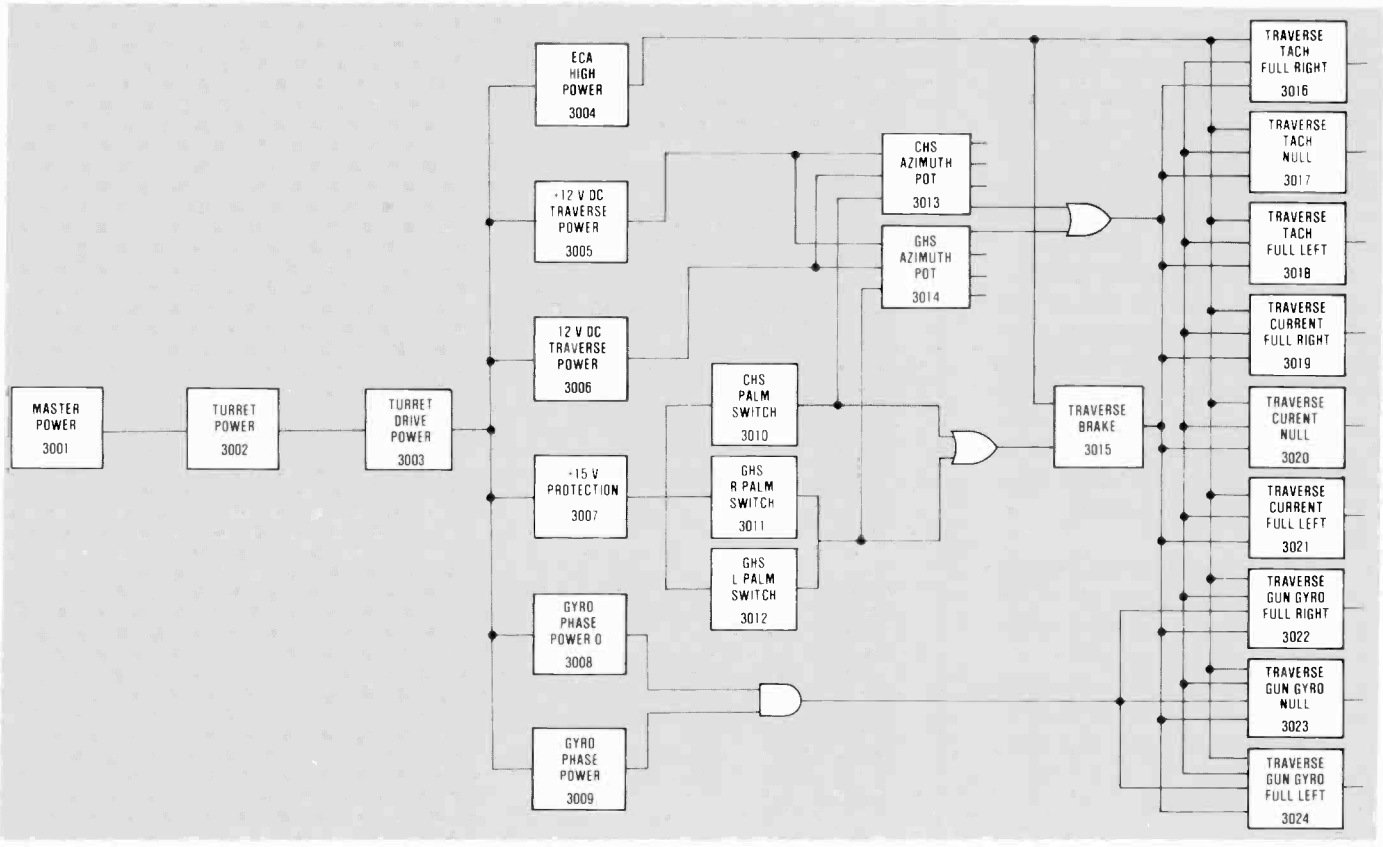

Fig. 3. *The data flow net for the Bradley Fighting Vehicle turret traverse subsystem.*

measurements identified as present in the diagnostic situation, and those known to be absent, the test manager derives a set of constraints. A constraint can be thought of as a subset of the total vehicle situation that must or must not occur in the final diagnostic model of the failure.

When Level I data acquisition ends, the test manager first looks at the arc information. An arc failure corresponds to some catastrophic subsystem failure in the vehicle that prevents further testing along a network path. Typically, the mechanic would want to fault isolate this problem first. Furthermore, the arc information is used to limit the search space to include only those subsystems whose corresponding local experts have fired.

Fault isolation

At this point all the pass/fail information has been logically encoded as a pattern of logic ones and zeros in the pass/fail flag register. A search for the physical cause(s) that led to this pattern involves generating a bit pattern that has a known correspondence to a constellation of system faults (in other words, a hypothesis) and comparing it to the fault signature residing in the flag register until a match is found.

As AI helped guide the choice of representation, the "generate and test" paradigm used by many AI programs provides the conceptual framework for fault isolation.[2] In our system a "hypothesis" is generated in the form of a bit mask. It is tested by comparing it to the bit configuration in the flag registers. The crude representation at the pseudo assembler level is necessitated by the physical and temporal constraints of a small portable test set and its real-time mission.

Issues involved in the creation of a good hypothesis generator include completeness, non-redundancy, and ordering. In our representation a complete hypothesis generator would simply be a binary counter that would generate every possible bit configuration and its known correlative of hardware failures. Obviously, for all but the most trivial systems, this is not practical or desirable. In lieu of completeness, at this early point in the implementation, we settled for a default mode that selectively vectors to presently fielded and validated fault isolation routines if no pattern match is found. This assures that for the worst case, our system will perform as well as the system presently fielded. It also allows us to incrementally add and reorder smarter and faster hypotheses while still producing improved and fieldable software.

The order in which hypotheses are called and tested can present a complex problem. Our implementation employs a technique, well known in the AI field, called context limiting. This technique is used to limit the combinatorial explosion inherent in rule based expert systems. We use it in its most basic form, to partition knowledge into context related subsets. Ordering of hypotheses within each of these subsets is driven by our customers' priorities. Their need for speed and ease of operator interaction directs us to test for and eliminate those candidate faults involving the least operator interactions. Thus, our first group of hypotheses would immediately lead to a diagnostic conclusion, faulting an LRU or a cable. Our second group would involve one cable disconnect, our third group might involve two cable disconnects, a special cable hook-up, and so on.

It is also conceivable to include those hypotheses that correspond to known recurring faults, or faults that resist conventional diagnostic solutions. The power and flexibility of this approach are built into the data flow representation. Optimum implementations are system dependent and remain to be studied.

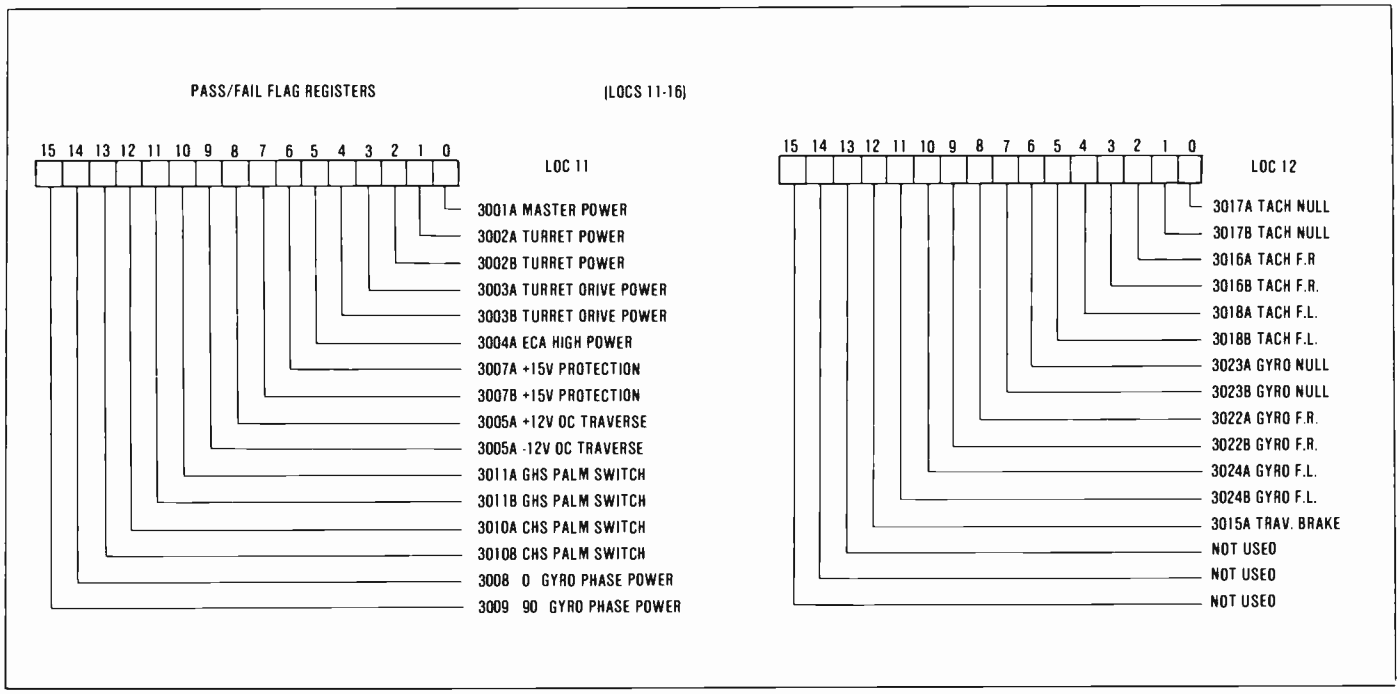

Fig. 4. *Results registers. The local experts execute their diagnostic logic and store the results here.*

Representation of the turret traverse test

The data flow representation makes the top level test strategy explicit. Figure 3 shows the data flow net for the BFV Turret Traverse subsystem. The necessary power supplies are first tested, in parallel where possible. Next the handstation signals that provide enable and velocity reference signals to the servo are examined. The servo states are designated full right (FR), null and full left (FL). These reflect the handstation positions that result in clockwise, no rotation, and counterclockwise rotation, respectively. In each of these states, the servo torque and speed outputs (armature current, tachometer, and gyro) are examined for their steady-state and transient response. The net provides a simple and concise statement of the test strategy that is easily modified when new discoveries are made.

Figure 4 shows a portion of a logically encoded result register. The entire diagnostic situation is efficiently stored in a few contiguous sixteen-bit memory locations. The system allows for very fast, very efficient retrieval and computation at assembly language speeds. Furthermore, this representation is language-independent. The entire network was implemented using the conventional diagnostic flow charts language used by the STE product line since its inception. Extensions to the language were added to enable the convenient storage and recall of measurements and flags. There is no reason that all the modules need be written in the same language. Any combination supported by the system software is possible.

Conclusion

The study of AI reveals new tools, new concepts and new ways of dealing with old problems. We have chosen from this field selectively and pragmatically, adapting ideas and concepts that enhance the diagnostic mission of our test set. We have chosen a data flow network for representing diagnostic knowledge because it fulfills the criteria for a clear representation. The test strategy is explicit and concise. Constraints are made explicit by clearly showing the dependence and independence between local experts. Data is collected and stored so as to facilitate fast, efficient computation. Some powerful new extensions were added to the diagnostic flow chart language that made possible the efficient collection and storage of vehicle data. With these extensions, the existing test procedures were easily adapted to the new representation.

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Automated flowchart generation

The Flowchart Generator for DFL (FCG) automatically generates flowcharts by transforming DFL source code into its graphical representation.

Abstract: *Automated flowchart generation is a computerized process for creating a flowchart representation from the source code of a program. The system automatically converts each logical construct of a particular language into its equivalent flowchart representation. Once the source code is converted into a flowchart format, the flowchart can be displayed or plotted on a suitable graphics display device.*

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Flowcharts have long been associated with computer programming and are considered an integral part of the programming process. They are the graphical representation of a programming language, facilitating comprehension of the control flow of a program.

One language that relies heavily on this concept is RCA's Diagnostic Flowchart Language (DFL). DFL, initially developed as an internal research project at RCA, was designed specifically for testing vehicle systems with the Simplified Test Equipment for the Army's Abrams M1 tank and Bradley Fighting Vehicle System (STE-M1/FVS: see Fig. 1 and the DFL sidebar). Application engineers use flowcharts to develop diagnostic tests for isolating problems in these vehicles. The flowcharts are then converted to DFL source code that is eventually compiled into object code for the target test set. Figure 2 exemplifies the correlation between the flowcharts and DFL source code. Note that since the flowchart contains both procedural and programming information, its purpose is twofold; it serves as a development tool for application engineers, and as the final documentation of the code.

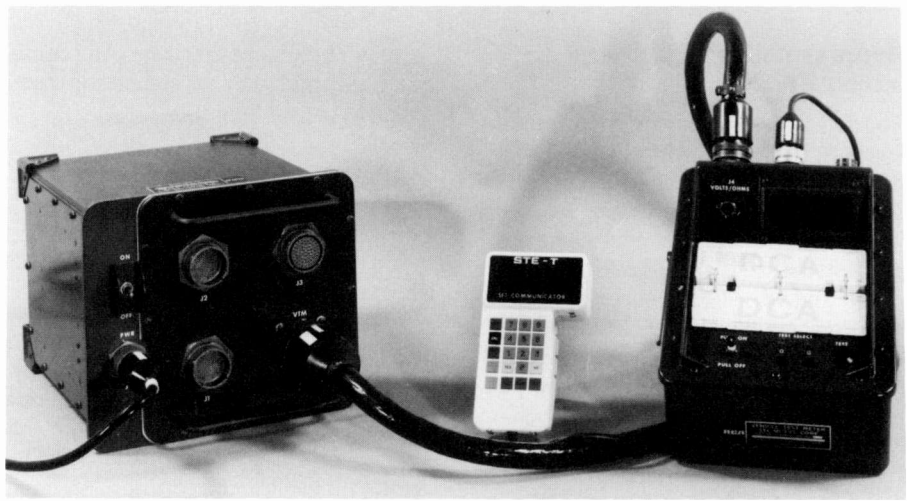


Fig. 1. *Simplified test equipment for the Abrams M1 tank and the Bradley Fighting Vehicle System.*

As with any software based product, the diagnostic tests for isolating faults in a vehicle are continually evolving. Improvements to current tests and additional diagnostic logic reflecting the manufacturer's modifications to the vehicles are constantly being developed. This results in frequent modifications to the DFL source code and to the corresponding flowcharts. While the code is directly edited by the application engineers, the flowcharts are controlled documents and must be changed by the drafting department. Therefore, engineers must not only edit the code, but must prepare engineering change notices for drafting and verify each updated flowchart page for every change made to the code. This constraint on modifying flowcharts produces time delays that prevent the flowcharts from reflecting the most recent code updates. In addition, as expected with two representations of each diagnostic test, configuration management is difficult.

Many of these problems can be alleviated through automated flowchart generation. Automated flowchart generation is a computerized process for creating a flow-

chart representation from the source code of a program. The system automatically converts each logical construct of a particular language into its equivalent flowchart representation. Once the source code is converted into a flowchart format, the flowchart can be displayed or plotted on a suitable graphics display device.

The Flowchart Generator for DFL (FCG) automatically generates flowcharts by transforming DFL source code into its graphical representation. Once plotted, the flowchart pages are complete and available for distribution. Since these pages are produced directly from the DFL source code, the flowchart matches the code exactly, an obvious advantage. Another benefit of the flowchart generator is the reduction of configuration management problems. Since only the DFL source code must be controlled, tracking code modifications is facilitated. Lastly, the flowchart generator increases the productivity of the application engineer. By reducing time spent on preparing change notifications and verifying drafting changes, engineers may concentrate more on the diagnostic logic of tests.

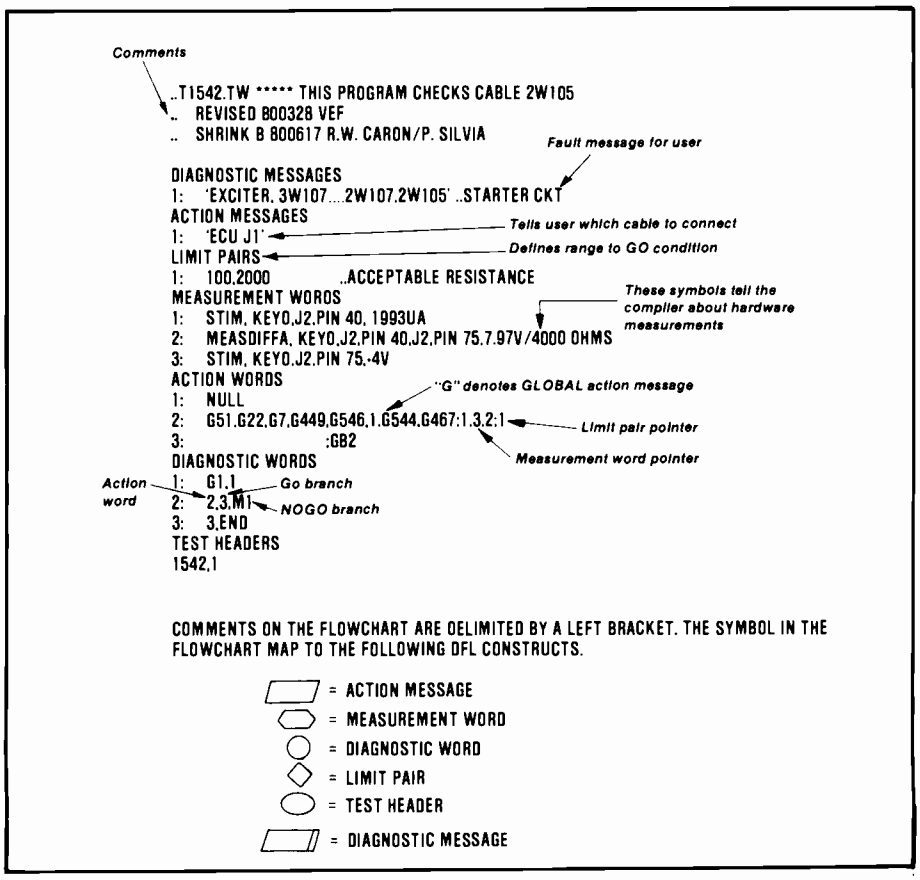


Fig. 2a. *Correlation between DFL source code and flowchart symbols.*

System overview

The DFL flowchart generator system logically consists of three concentric levels, as depicted in Fig. 3a. The innermost level portrays the kernel of functions for manipulating elements of the flowchart representation that are stored in the form of a directed graph (digraph). A digraph is the natural choice for the system's internal representation of a DFL test. Not only is graph theory well understood and the functions easily created, but every DFL test may readily form a directed graph. The concept of a directed graph is discussed below in further detail. The middle level contains three major subsystems that convert the input DFL source code into a directed graph, format the directed graph contents into flowchart pages, and produce graphical display data from the formatted directed graph. The outer level contains the system executive, which controls the operation of the entire flowchart generator.

The flow of data between the three subsystems (the DFL-to-digraph converter, the formatter, and the output generator) is illustrated in Figure 3b. The DFL-to-digraph converter accepts DFL source code as input and creates a directed graph with a node for each shape. The nodes are annotated with information such as shape, type and text. The formatter assigns page and location positions to the various flowchart shapes contained in this directed graph. It determines what information fits on a flowchart page and where this information is located on the page. The output generator constructs flowchart shapes from the information found in each node of the directed graph. A separate graphics library is used in this latter step.

Resources

The DFL flowchart generator system is implemented on a Digital Equipment Corporation (DEC) VAX 11/780. Display devices include a Nicolet Zeta 822 plotter and a DEC VT125 graphics terminal.

The majority of the system is written in VAX-11 Pascal. The graphics functions are provided by Precision Visuals Extended DI-3000 graphics package. Miscellaneous routines are provided by DEC VMS Run Time Library and System Services.

Data structure

All the major subsystems of the Flowchart Generator operate on the system's internal data structure (the directed graph). A directed graph consists of a set of nodes and a set of directed arcs that connect the nodes. The nodes contain application-specific information and the directed arcs specify relations (or adjacencies) between nodes. For example, consider the simple directed graph in Fig. 4. Pictured are a set of nodes A, B, C, D, and a set of arcs (A,B) (A,C) (B,D) (C,B) (D,A). Each ordered pair denotes a directed arc from the first element to the second. The directed arcs limit the movement between the nodes; starting at node A and traversing to node D, the directed arcs force node B to be visited. A path is a sequence of arcs from one node to another. A cycle is a path from a node to itself. In Fig. 4, a cyclic path consists of the arcs (A,B) (B,D) (D,A).

Directed graphs have many applications. For example, procedural information is easily represented by a directed graph. Consider the simple process of frosting a cake. If Fig. 4 depicts this process, then each node describes a state in the frosting process (or step in the procedure), and each arc signifies a transition between states. We can define the nodes in Fig. 4 as follows:

- Node A—the initial state of having an unfrosted cake and the basic ingredients to make the frosting.

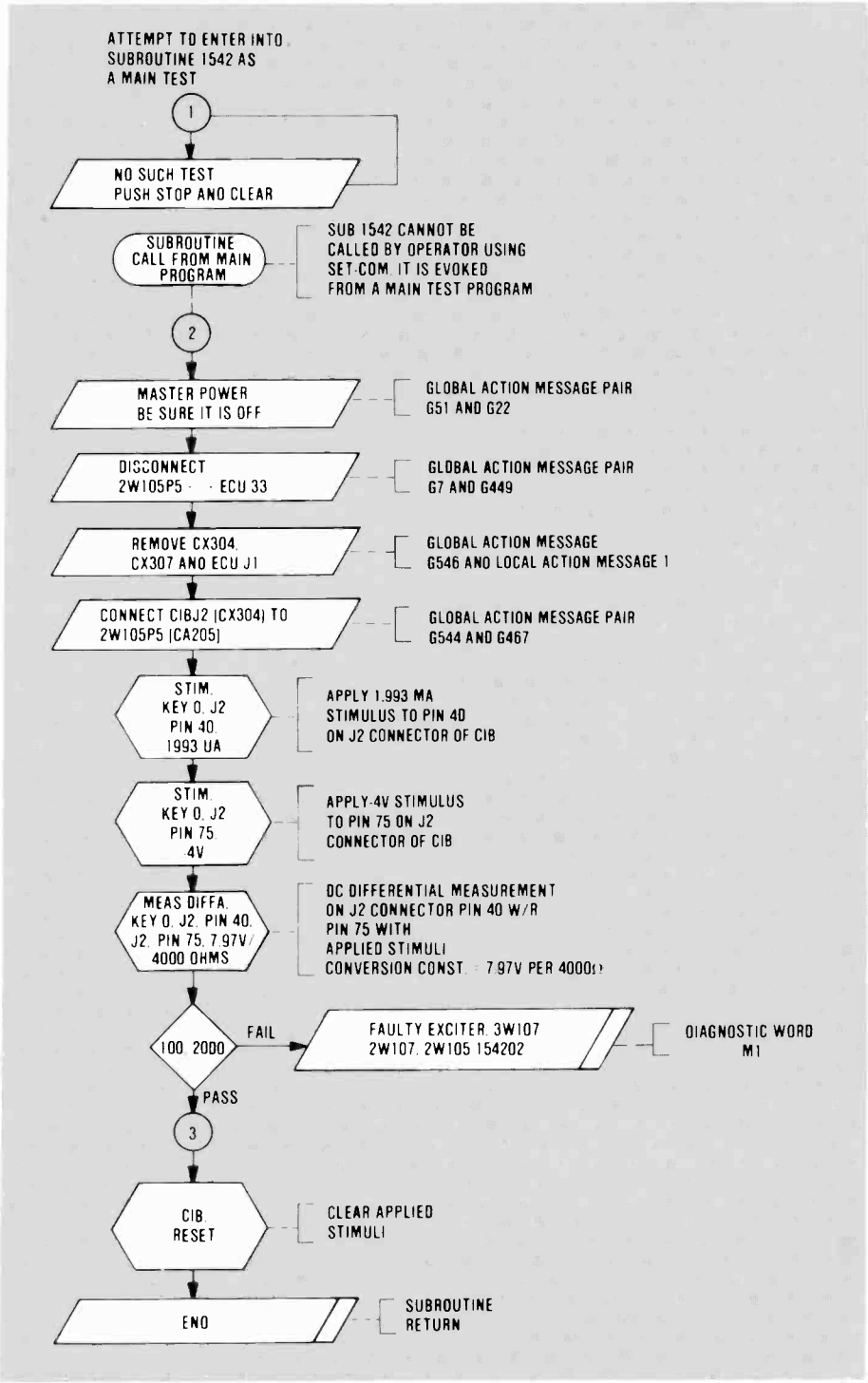


Fig. 2b *Manually drawn flowchart. Comments are shown within brackets to the right of the flowchart map.*

- Node B—combining the ingredients, such as butter, sugar, and vanilla, to make the frosting.
- Node C—obtaining chocolate to add to the frosting mix.
- Node D—placing the frosting on the cake.

Then, if we want to make a chocolate frosted cake, the nodes would be visited in the order: A, C, B, D. If a plain frosted cake is desired, the visitation order would be: A, B, D. The arc from Node D to Node A may represent that, once eaten, we must frost another cake.

A DFL diagnostic test can be considered as a procedure, and thus be represented as a directed graph. Each node can be a state, such as displaying a message (action message), making a measurement (measurement word), or making a decision (limits pair). This is the precise reason for choosing the directed graph as the system's internal data structure. Each node in the graph contains information such as the type of shape, the text within the shape and the position of the shape on the page. Arcs are delineated by associating pointers with each node. These pointers denote the parents and the possible children of a particular node. The node having no parent nodes is defined as the root of the digraph, and is equivalent to the beginning of a DFL test. A node having no descendants is defined as a leaf node, and usually represents the diagnostic termination (message) of a DFL test.

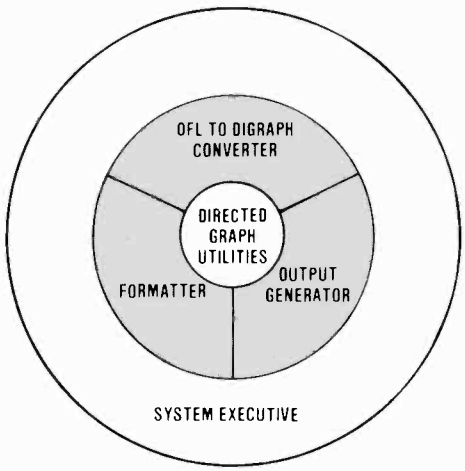


Fig. 3a. *DFL flowchart generator system configuration.*

Directed graph utilities

The graph utilities perform all operations on the directed graph data structure. Included are functions to create nodes, create arcs between nodes, modify the contents of a node, retrieve nodes, delete nodes, and delete arcs. Another utility provides the means of traversing a directed graph via a depth-first search. A depth-first search visits all the nodes by starting at the root of the graph and searching "downwards" from the current node until a leaf node or previously visited node is reached. The search then backtracks to a node having a branch not previously taken and continues searching "downwards" until another leaf node or previously visited node is reached. This process continues until all nodes in the graph are visited or until the desired node is found. An example of a depth-first search on a directed graph is given in Fig. 5.

The digraph utilities are easily adapted to other applications requiring a similar inter-

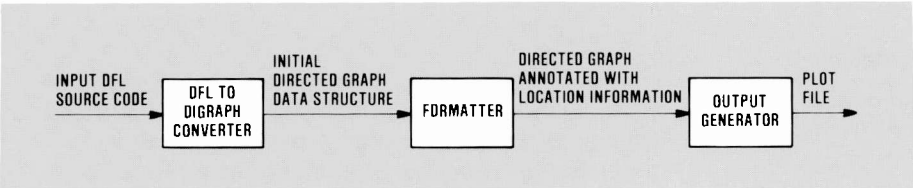


Fig. 3b. *Data flow diagram of the flowchart generator.*

nal data structure. This capability results from the technique, known as data hiding, used in developing the utilities. Data hiding is the method of creating a set of functions that allows manipulation of the system's data structure without specific knowledge of the implementation of that data structure. One advantage of this method is the simplicity in using these functions to access the data structure. For example, suppose a new digraph node is needed. A new node is created by invoking a single function that creates the node and annotates it with the specified information. Since all functions are perceived at this higher level, the work of creating new dynamic records, adding to array elements, and updating pointers is hidden from the program invoking the function. Another advantage is the ease of maintenance of the internal data structure. To modify the data structure, only the pertinent directed graph utilities need be changed; the subsystems using the graph utilities are unaffected. Therefore, data hiding is a powerful yet simple technique of layering the complexities of the system. Since each layer uses only the one beneath it to carry out some desired function, the entire system is logically designed, easily maintained, and portable.

DFL-to-digraph converter

The DFL-to-digraph converter (DDC) transforms the DFL source code of a diagnostic test to a directed graph representation. All the various sections of the DFL source code (action messages, measurement words, limits pairs, etc.) are converted into a sequence of directed graph nodes linked by appropriately ordered arcs. The DDC translates some of the source code into a more informative representation. For example, with the aid of external data tables, the source code of a measurement word is translated to contain information concerning the actual vehicle subsystem being tested.

Besides source code translation, the DDC permits implementation of flowchart shape comments. A new section added to the DFL source code allows the programmer to specify a comment for any flowchart shape. The DDC processes the new section by matching the input comment with the directed graph node representing the appropriate flowchart shape.

The processing performed by the DDC uses LR(1) parsers and the associated semantic action routines (see sidebar on parsers). These parsers generate flowchart shapes in the appropriate sequence while translating portions of the DFL source code into text for the flowchart shapes. A parser generator program automatically creates the parse tables from DFL code syntax tables specified in Backus-Naur Form (BNF). These parse tables are then used by the LR parsers to process the DFL source code. This method of processing greatly reduces program maintenance, since any change in the DFL syntax simply requires the parser generator program to automatically produce new parse tables.

Formatter

The formatter constructs a flowchart by efficiently allocating positions on pages for shapes, represented by the digraph nodes, according to established DFL flowcharting standards. The formatter traverses the directed graph using a modified depth-first search. It first processes the True Go Path (TGP) of the DFL test, formatting these

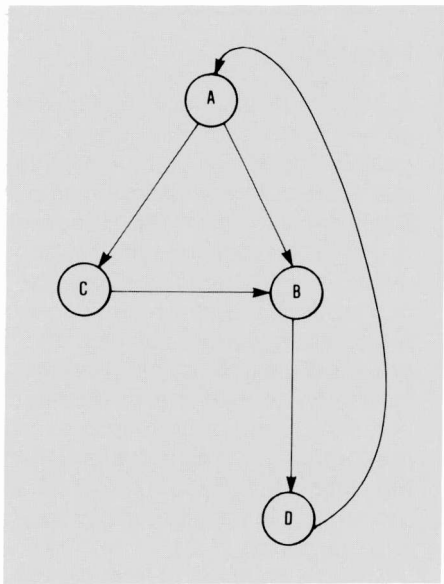


Fig. 4. *Example of a directed graph.*

shapes, lines and text onto the first pages. The formatter then deals with each fault path branching from the True Go Path. As it traverses the digraph, the formatter determines which shapes fit onto the current page by consulting a bit map image of the occupied areas. If the shape fits in the current position, the coordinates and page number are assigned to the node, the position on the page is updated, and processing of the graph continues. If the shape collides with another, the formatter decides whether to move down the current column, try another column, or start another page. The formatter not only traverses the digraph, but adds to it under certain circumstances. For example, if a branch to another page occurs, an off-page connector and associated lines must be added to the flowchart and

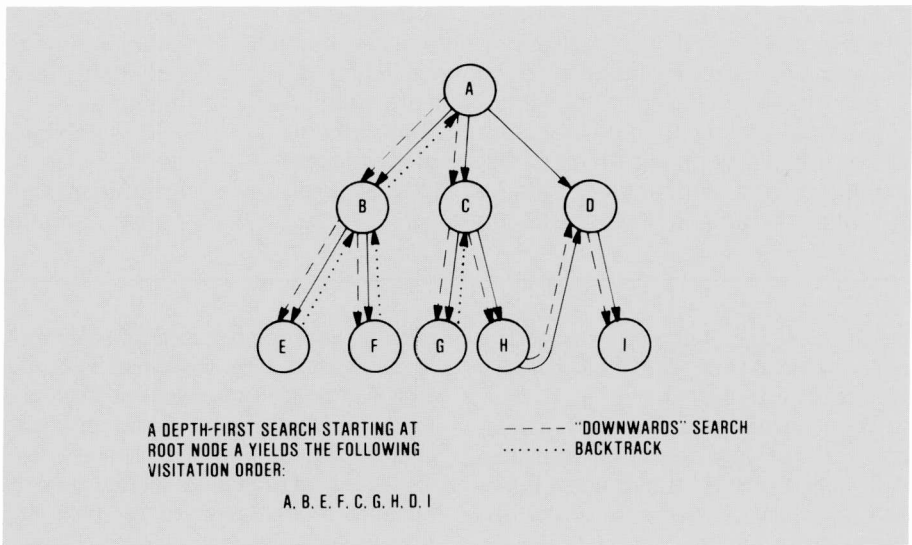


Fig. 5. *Depth-first search example.*

Parsers

Associated with every language is a set of grammar or syntax rules for all possible sentences in that language. A standard method for specifying the grammar rules of formal programming languages is in Backus-Naur Form (BNF). Each rule is composed of two symbol types; terminals and nonterminals. Terminals are the basic symbols that form "sentences" of a language, and are analogous to dictionary words such as dog, cat, boy, and run. Nonterminals are special symbols that represent sets of terminal symbols. For example, nonterminals might be a sentence, verb, or arithmetic expression. In BNF, nonterminals are denoted by enclosing them within the symbols "<" and ">". All other symbols in a grammar rule (or grammar production) are assumed to be terminals.

Using a finite set of terminals and nonterminals, the syntax of most programming languages can be specified by a context-free grammar. A grammar is called context-free if every construct of the language's grammar can be expressed in Backus-Naur Form. A context-free grammar for a langauge is valuable because it provides a precise, easy to understand syntax specification for the language. An example of a grammar in BNF is the following. Consider the sentence "The big dog ran after the ball." The following are grammar productions to specify this sentence.

1. <sentence> ::= <subject> <predicate>
2. <subject> ::= <article> <adjective> <noun>
3. <article> ::= the
4. <adjective> ::= big
5. <noun> ::= dog
6. <predicate> ::= <verb> <object>
7. <verb> ::= ran
8. <object> ::= <preposition> <article> <noun>
9. <preposition> ::= after
10. <noun> ::= ball

Note that the nonterminal "<noun>" is defined as either "ball" or "dog". Another possible sentence that can be formed with these productions is "The big ball ran after the dog." Both sentences are valid in terms of syntax, but vary in meaning. Thus, we can see that although a grammar can ensure syntactically correct sentences, it does nothing to ensure that each sentence has a valid meaning.

Once a context-free grammar for a language has been defined, an efficient parser can be constructed for that particular grammar. A parser is a software tool used to recognize grammar rules (or productions) within the input to the parser. This allows the parser to ensure that the input follows the grammar rules of the parser's target language. For example, if we have the sentence "The big dog ran after the ball," a parser could be used to check the syntax of this sentence; it would ensure that the adjective "big" modifies some noun, in this case "dog." One of the most common uses for a parser is in a compiler for programming languages such as FORTRAN or Pascal. The parser ensures that the user's program follows the syntax rules of the language and at the same time generates the machine code for the program. When a portion of the input being checked matches a grammar rule, the parser evokes the function associated with that rule to generate machine code representing the input. These functions are called semantic action routines because they give meaning to a particular grammar rule. For example, once the Pascal statement "A : = 5" matches one of the grammar rules for the Pascal language, the parser would use a function to generate the machine code equivalent of this statement.

Many types of parsers can be constructed. The type of parser is based upon the grammar specification of the language for which the parser is targeted. One of the more common parsers is a LR(1) (Left-to-right scan of the input, rightmost derivation) type. It operates upon a class of grammars known as LR type grammars. It is beyond the scope of this paper to go into the details of LR grammars and LR(k) type parsers. For more information on LR grammars, consult *The Theory of Parsing, Translation, and Compiling* by Aho and Ullman. Since most languages can be easily specified by an LR grammar, it makes the choice of a LR parser the most logical to implement a syntax checking program for a particular language. All parsers achieve the same goal of checking the input for syntactical correctness; they vary only in the means and efficiency of checking the input.

Principles of Compiler Design by Aho and Ullman and *Compiler Design Theory* by Lewis, Rosenkrantz, and Stearns are excellent texts on the theory behind parsers and compilers.

hence the digraph. Note that this shape does not correspond to any DFL code but is an artifact of the formatting step.

The structure of a flowchart page is crucial to the operation of the formatter. A flowchart page is mapped into a Cartesian coordinate system, the lower left corner defined as the origin (see Fig. 6). This allows for precise specification of the current position and the location of shapes, lines, and text. This coordinate system is then partitioned into columns. There are four main flowchart columns that may contain shapes, lines and comment text. To the side of each main column is a continuation column, reserved for connecting lines between shapes in different columns. This representation allows for production of a flowchart page that conforms to established DFL flowcharting practices.

The formatter constructs a data structure known as the page-object list. This list is a collection of pointers ordered by page number. Each pointer begins another list containing graph node pointers. The digraph nodes pointed to on a list are those nodes formatted on that particular

page. The purpose of the list is to increase the efficiency of the output device. Since the formatter uses a modified depth-first search algorithm to traverse the graph, all digraph nodes formatted onto a certain page are impossible to locate without duplicating the decisions made by the formatter. The page-object list alleviates this problem by allowing the output generator to easily access the digraph nodes formatted in a column, from the top to the bottom of each column, for each flowchart page.

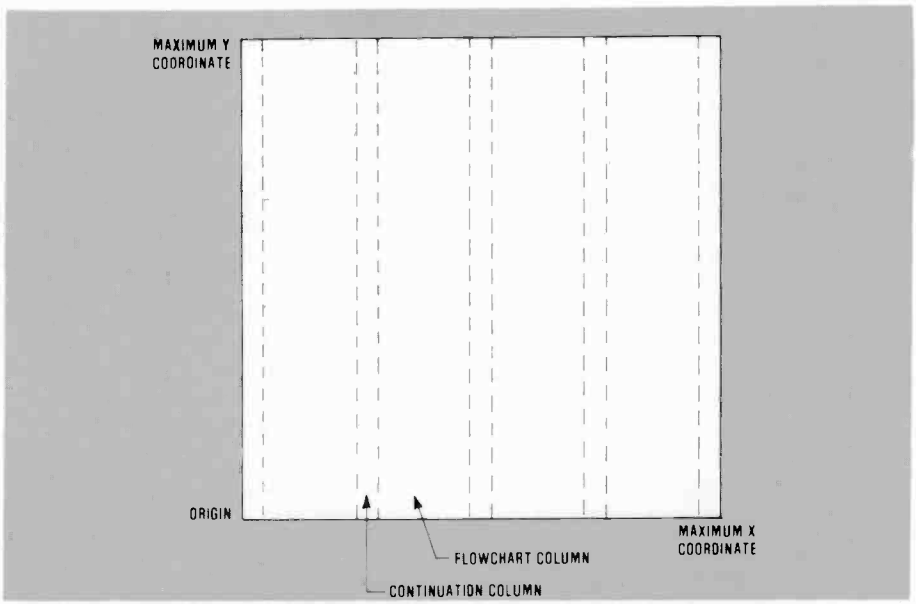


Fig. 6. *Flowchart page structure. The coordinate system is partitioned into four main columns and five continuation columns.*

Output generator

The output generator produces the graphics display data for the lines and text that compose the information contained on a flowchart page. It scans the page-object list to access the digraph nodes representing the flowchart shapes. For each shape encountered, the output generator evokes functions in the graphics library to create graphics display data for the lines and text. The graphics display data may be generated in two formats: a device-specific file, and a device-independent metafile. The device-specific file stores a flowchart page in a standard C-size (17 by 22 inch) format. The metafile allows the stored graphical image to be viewed on display devices through a metafile translator for a specific device, such as a DEC VT125 graphics terminal. At the user's option, either file format can be specified. A simple example of a computer generated flowchart plot is shown in Fig. 7.

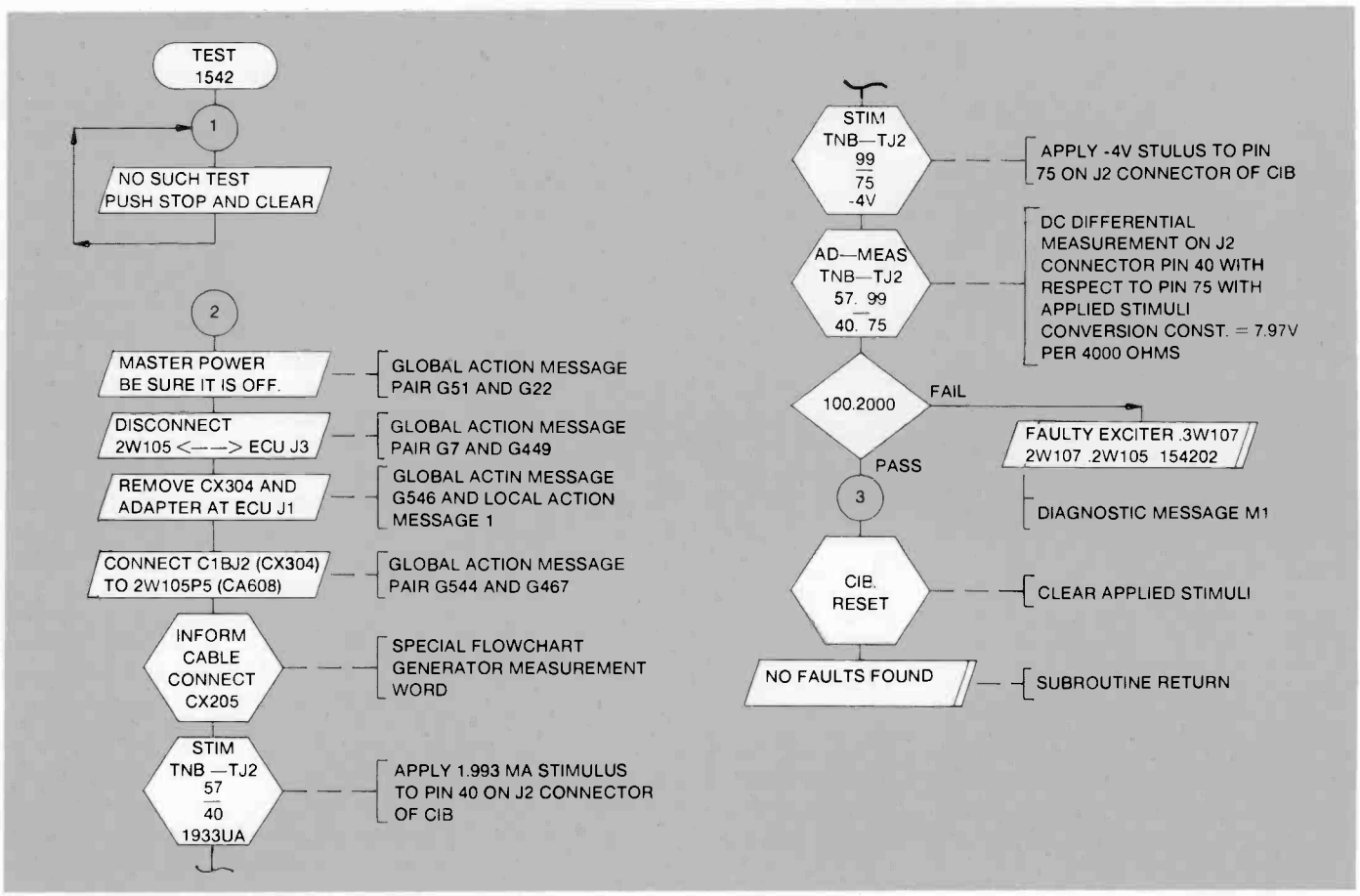
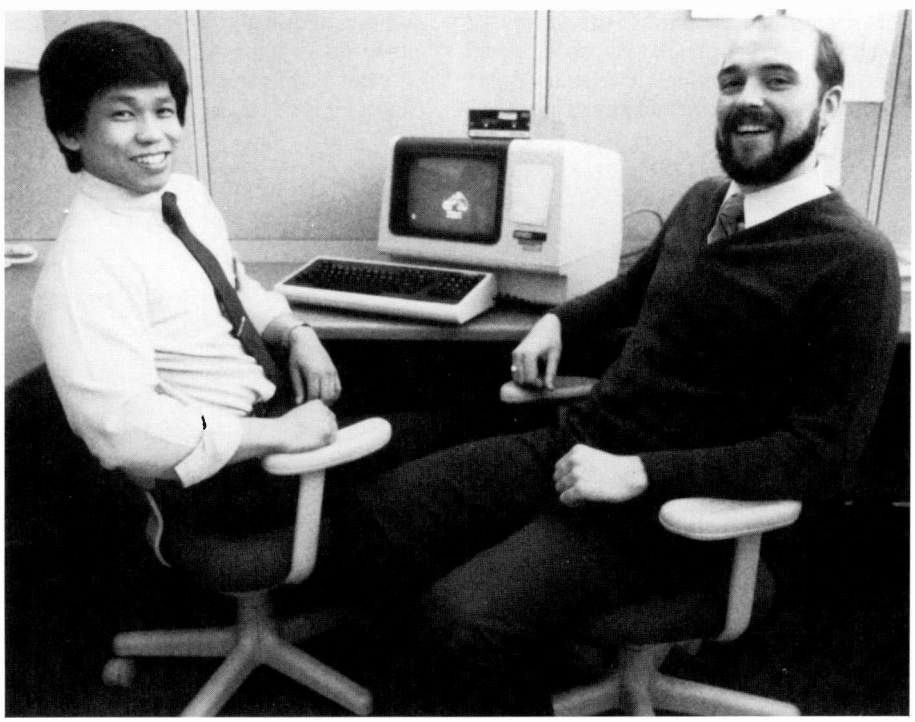


Fig. 7. *An example of a computer-generated flowchart.*

DFL

The Army's M1 tank contains numerous electrical, mechanical and hydraulic subsystems that are tested with the STE-M1/FVS test set. If assembly language code was used to program the test set for this vehicle, nearly one megabyte of memory would be required. The high cost of building a test set containing this much EPROM (erasable programmable read only memory), and the problems with managing the assembly code for all tests, spurred an internal research effort at RCA to develop a called Diagnostic Flowchart Language (DFL). DFL's object code is interpreted in the target test-set system. Its use in application tests has reduced the memory requirements of application code by a factor of five over the equivalent assembly language implementation of the tests. Moreover, with DFL, application engineers no longer need detailed knowledge of the measurement system hardware or the operating system of the test set. This decreases the time an applications engineer spends programming a test, thereby increasing the time available for developing the diagnostics of the test.

Since each DFL test represents a logical flow of control for testing a subsystem of the vehicle, application tests are defined using a standard flowcharting method. Most diagnostic tests contain a True Go Path. Completing the True Go Path signifies that the subsystem under test is operational. If a problem is detected while traversing the True Go Path, a branch into a fault path occurs. In the fault path, the problem is isolated to a line replaceable unit of the vehicle or a connecting cable within the subsystem. Once the flowchart for a diagnostic test is developed, it is implemented in DFL. Since the constructs of DFL closely follow the structure of the flowchart, the task of coding the test is simple. Figure 2 highlights the correlation of a diagnostic flowchart and the DFL code.



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Plotmaker

The plotmaker is a separate utility that allows the user to generate A-size (8 ½ by 11 inch) plots on the Nicolet Zeta plotter. The flexibility of the metafile translator system simplifies this process. Once the flowchart generator creates a metafile for a DFL test, the plotmaker uses the metafile translator to produce a graphics image that is scaled and translated to the desired size.

Future trends

An upcoming extension to the flowchart generator is the STE Graphic Compiler System (SGC). This system will allow the user to graphically edit a diagnostic test. The flowchart of the test will be displayed on a graphics terminal and may be edited by manipulating flowchart shapes, lines and text. Once the flowchart has been edited, DFL source code will be generated directly from the new flowchart. The graph utilities created for the DFL flowchart generator form the foundation of the STE Graphic Compiler. The output generator portion of the flowchart generator will be used by the SGC to produce flowchart plots. Both the FCG and SGC systems are illustrated in Fig. 8.

Summary

Automated flowchart generation of DFL provides many advantages, including enhanced configuration management, increased productivity, and improved code

documentation. The flowchart generator for DFL signifies the beginning of the automation of the rote tasks of application engineers, freeing more time for diagnostic development of tests. Eventually, a computer aided software engineering system will provide the complete environment for application programming.

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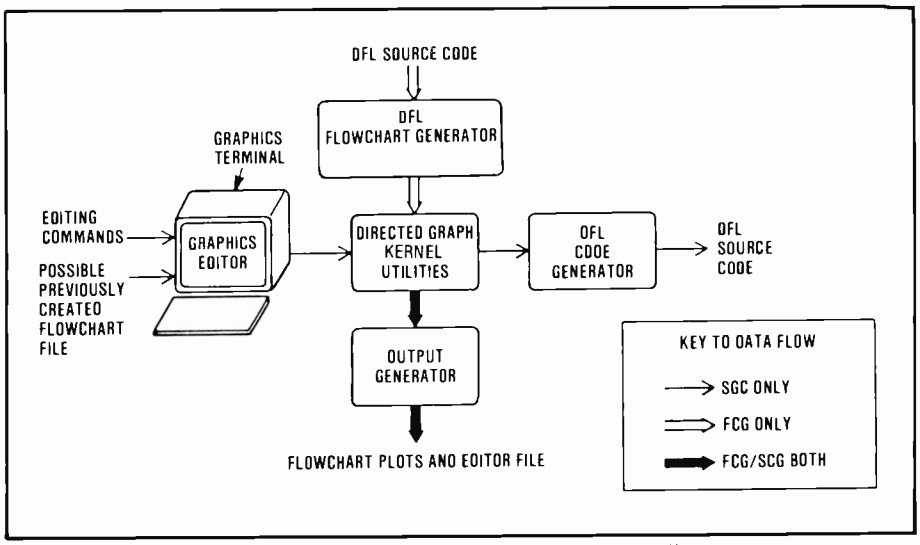

Fig. 8. *STE graphic compiler/flowchart generator system diagram.*

T.D. Fuhr

A laser measurement system for high-accuracy, automated near-field probe tracking

Unprecedented levels of accuracy and calibration speed for a near-field antenna scanner are achieved by a unique, automated, laser-based interferometric measurement system.

Missile and Surface Radar's new, second-generation near-field antenna test facility employs a 12-degree-of-freedom laser measurement system to produce the state of the art in accuracy and automation in the testing and alignment of phased array radar antennas. The results obtained with this measurement system, which contains more than 70 optical and electro-optical elements, represent an unprecedented level of accuracy for a near-field test facility. The lasers measure all scanner motions and provide information to calculate the position of an rf probe over a scan plane of 20 × 26 feet to a measured accuracy of 0.0034 inch RMS radial error over the entire scanning area. The mechanical calibration provided by the scanner laser measurement system is a highly automated, computer-controlled process requiring one operator and 15 to 45 minutes, depending on the selected scan scenario. In contrast, a manual scanner calibration would require approximately one week of effort for three trained personnel. The automation of the laser measurement system makes it possible to calibrate the scanner immediately prior to any antenna scan, thereby greatly reducing the risk of physical change to the scanner between the time of calibration and the time of the scan.

Abstract: *A 12-axis laser measurement system, the first of its kind, provides RCA Moorestown's new near-field antenna test facility with the state of the art in mechanical measurement accuracy needed for testing the next generation of lower sidelobe phased-array radars.*

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Reprint RE-30-2-4

This paper describes the rationale for and the implementation of this laser calibration system, the operational proof of the system, and its measured accuracy performance. The positional accuracy of the scanner obtained through the laser interferometers and the rapid, automated scanner calibration is making possible near-field testing of the new generation of low sidelobe antennas.

To achieve the lower sidelobes from these new antennas, the several thousand active phase shifters in the array must be resolved and adjusted to an rf phase error of less than one degree RMS. The positional accuracy requirements of the scanner are dictated by the needs of these new arrays.

In near-field testing, the phased-array antenna is placed in an environmentally controlled indoor facility. The antenna receives rf signals from a probe located approximately 10 inches from the array face. Ideally, the probe moves parallel to the array face, both vertically and horizontally, along an imaginary two-dimensional planar grid, and rf data is obtained at uniformly spaced intersection points. The phase and amplitude of the signal received by the antenna from the rf probe are digitized and transmitted to computers that collect and reduce the data.

Ideally, the rf probe must be precisely positioned at each intersection point along the grid. If the signal transmitted from the rf probe to the array is not measured at the exact intersection points, errors result in the near-field measurements that could possibly be a source of false sidelobe indications.

Scanner and laser architecture

Since the rf probe must scan horizontally along the X axis and vertically along the Y axis (Figs. 1 and 2), the scanner is configured to provide these motions. The scanner consists of a triangular cross-section steel tower, 24 feet tall, riding horizontally on Thompson recirculating linear ball bearings and Thompson hardened and ground 2-inch diameter steel shafts. The primary horizontal (X) rail is 35 feet long.

A small carriage containing the rf probe travels vertically on ¾-inch diameter Thompson shafts over the full height of the tower, passing in front of the antenna face. The primary horizontal (X) rail is aligned straight to within 0.003 inch in the vertical

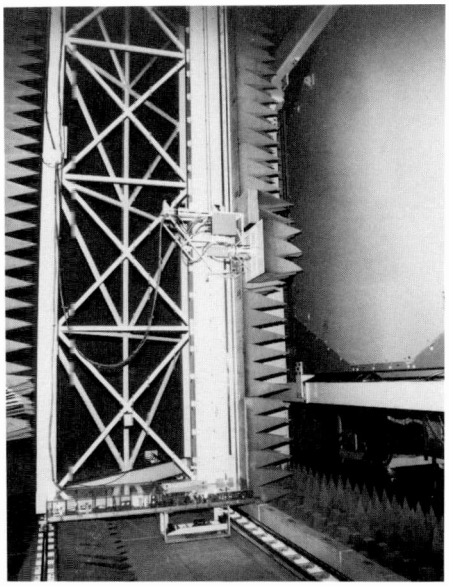


Fig. 1. The scanner positions the rf probe, which extends from the probe carriage, in front of the face of the phased-array antenna during a near-field test scan.

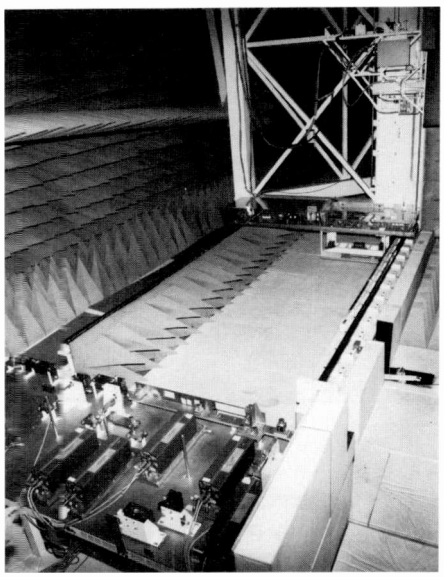


Fig. 3. The 12-degree-of-freedom laser measurement system, run from the five laser transducers on the fixed optical bench, measures all motions of the scanner. Scanner optics can also be seen on the tower shelf and at the top of the probe carriage. The carriage straightness reflectors, including the two fixed reflectors used for roll angle sensing, are located in the tower shelf subplate housing.

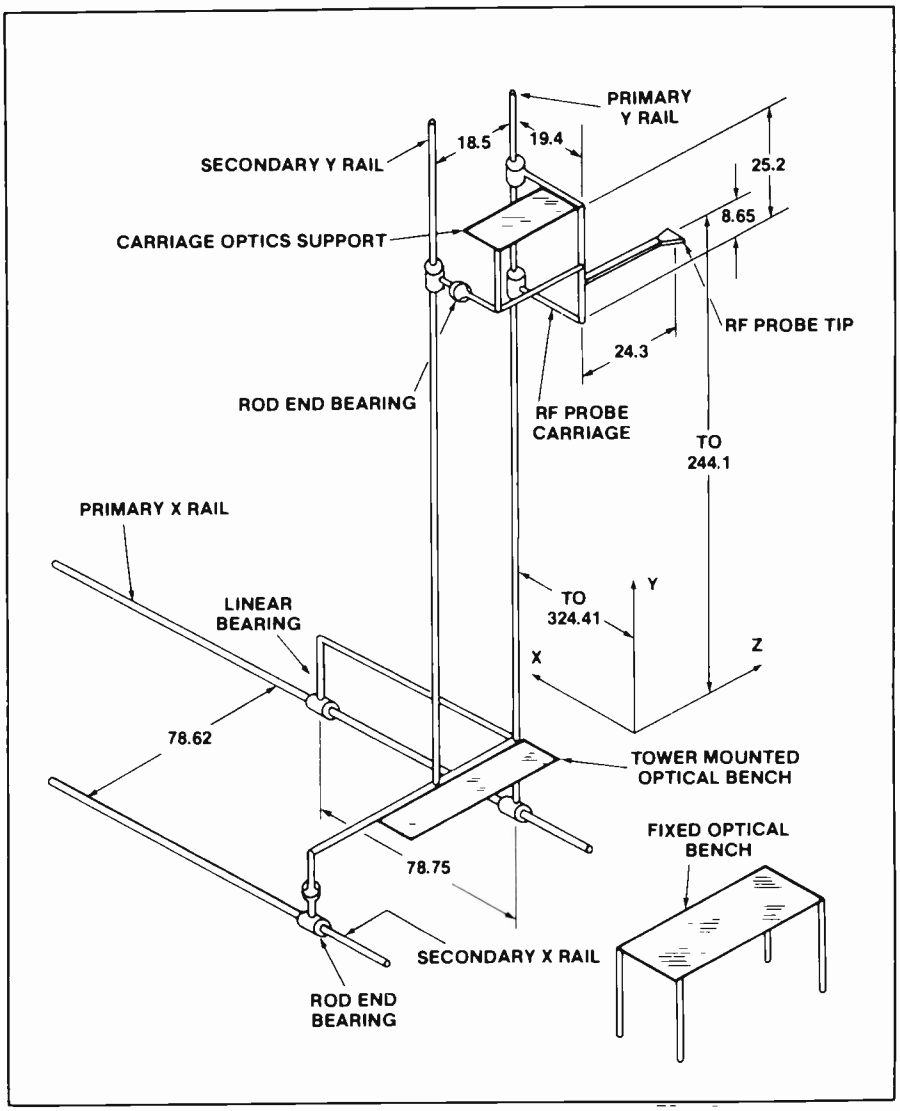


Fig. 2. *Scanner arrangements of near-field test facility (dimensions are given in inches).*

plane and 0.004 inch in the transverse plane. The primary vertical (Y) rail is straightened to 0.004 inch in both orthogonal planes. The secondary rails, which are essentially followers, are made parallel to their associated primary rails to within 0.004 inch in the vertical plane and 0.032 inch in the transverse plane. All straightness measurements are made with Hewlett-Packard long-range straightness interferometers and an HP 5526A laser transducer and display.

The mechanical accuracy of the scanner in positioning the probe tip over the scan plane is derived from the straightness and parallelism of the rails. However, the accuracy obtained from this stringent mechanical alignment is not sufficient to meet the formidable 0.004-inch RMS error probe positioning specification in each of the three axes (0.007-inch RMS radial error). To obtain this required accuracy, the rf phase data is corrected post-scan, based on the distance between the actual location of the probe as measured by the lasers (Fig. 3) and the ideal probe position on the imaginary uniform planar grid.

Because the probe is the rf radiation source of the near-field test system, a unique measurement scheme was needed to track its position. Optical elements could not be placed at the probe tip since they would disturb the rf field. This constraint eliminated any approach of directly tracking the probe tip position. In the final system, the probe tip position is calculated from data obtained by measuring all motions of the tower and carriage: 12 degrees of freedom plus an initial orthogonality error.

It is known from Newtonian mechanics that a rigid body contains 6 degrees of freedom in three-dimsenional space, and that all motions are a combination of translation along and rotation about each axis. The scanner can be considered a system of two independent rigid bodies, there-

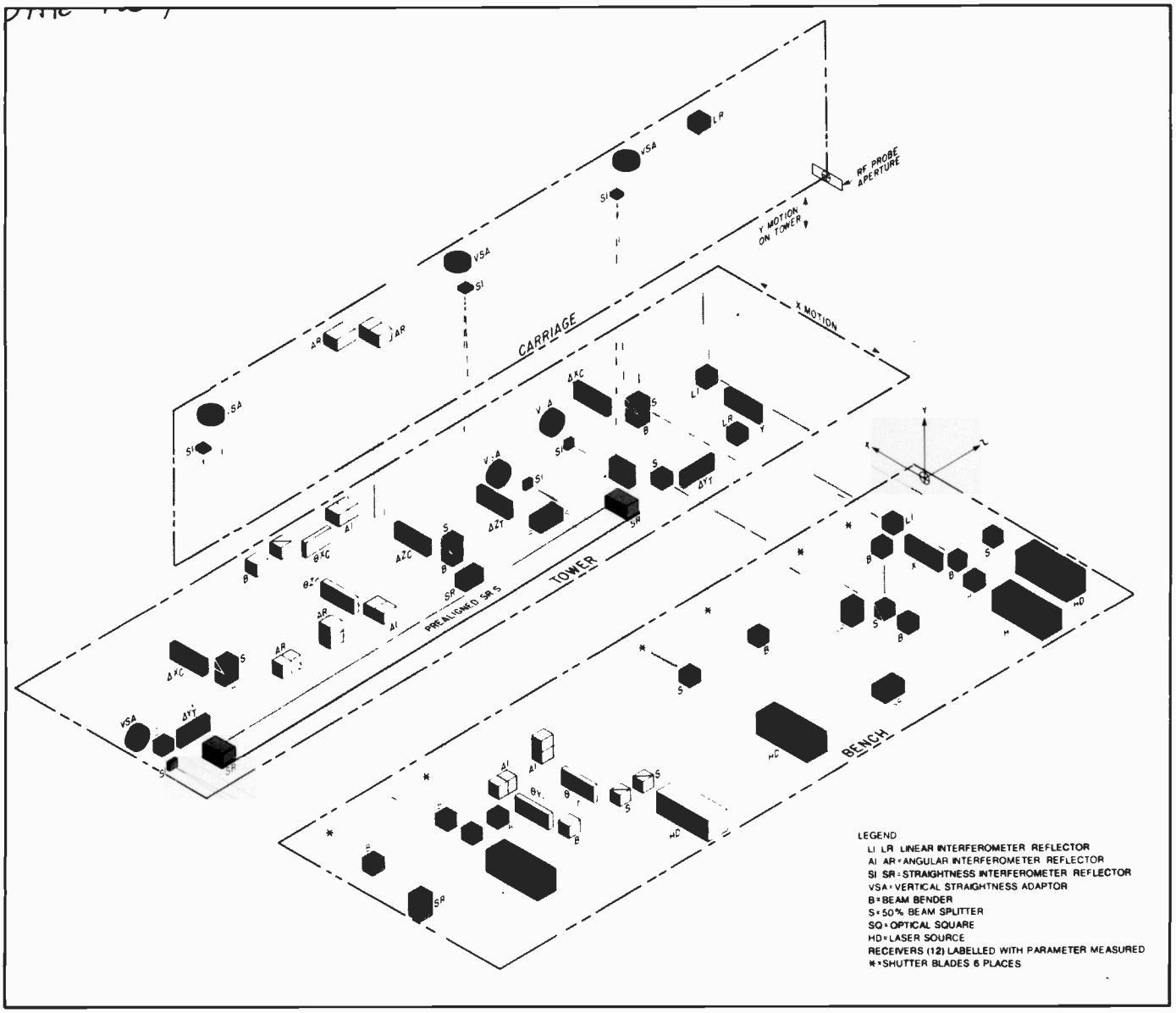


Fig. 4. *Arrangement of the laser optics for the near-field scanner.*

fore possessing 12 degrees of freedom. The laser system is configured to measure the 12 degrees of freedom present in the system. Using this information, it is possible to define the position of the probe tip in three-dimensional space.

Both tower and carriage motions are fully measured by the same basic laser interferometer architecture (see Fig. 4). One linear interferometer measures the motion of the body along its direction of travel. Two long-range straightness interferometers measure small displacements orthogonal to the direction of travel. A third straightness interferometer is present to allow the derivation of the roll angle, which is the rotation about the axis of travel or, in the case of laser interferometry, about the beam axis. Two angle interferometers measure the remaining two angular displacements of the body. All laser optical components in the system are manufactured by Hewlett-Packard and are a custom combination of elements from their 5501 and 5526 series of optics. A more detailed explanation of the laser optics and theory can be found in reference 1.

In the automated calibration of the scanner, the tower and carriage displacements are measured in separate runs. From this information, the probe displacement errors from the ideal rf measurement grid are determined. The calibration scenario uses the same dynamic conditions of scanner motion as are encountered in actual antenna scanning. The tower is stepped along the horizontal X rails at equal intervals under computer-commanded servo control, holding a steady position while data from the six tower measurement interferometers is sampled and averaged to smooth any random noise caused by local thermal effects in the anechoic chamber. The carriage displacement data is taken "on the fly" as the carriage moves vertically at its scan speed. The data sampling process is timed by the computer to occur at the proper Y location. A Perkin-Elmer 3250 mainframe computer is used as the system controller. In all scanner motions, the X and Y linear interferometers provide the data for positional feedback in the servo control. The horizontal hold/vertical scan data collection scheme of the laser calibration process is consistent with the actual antenna scan patterns.

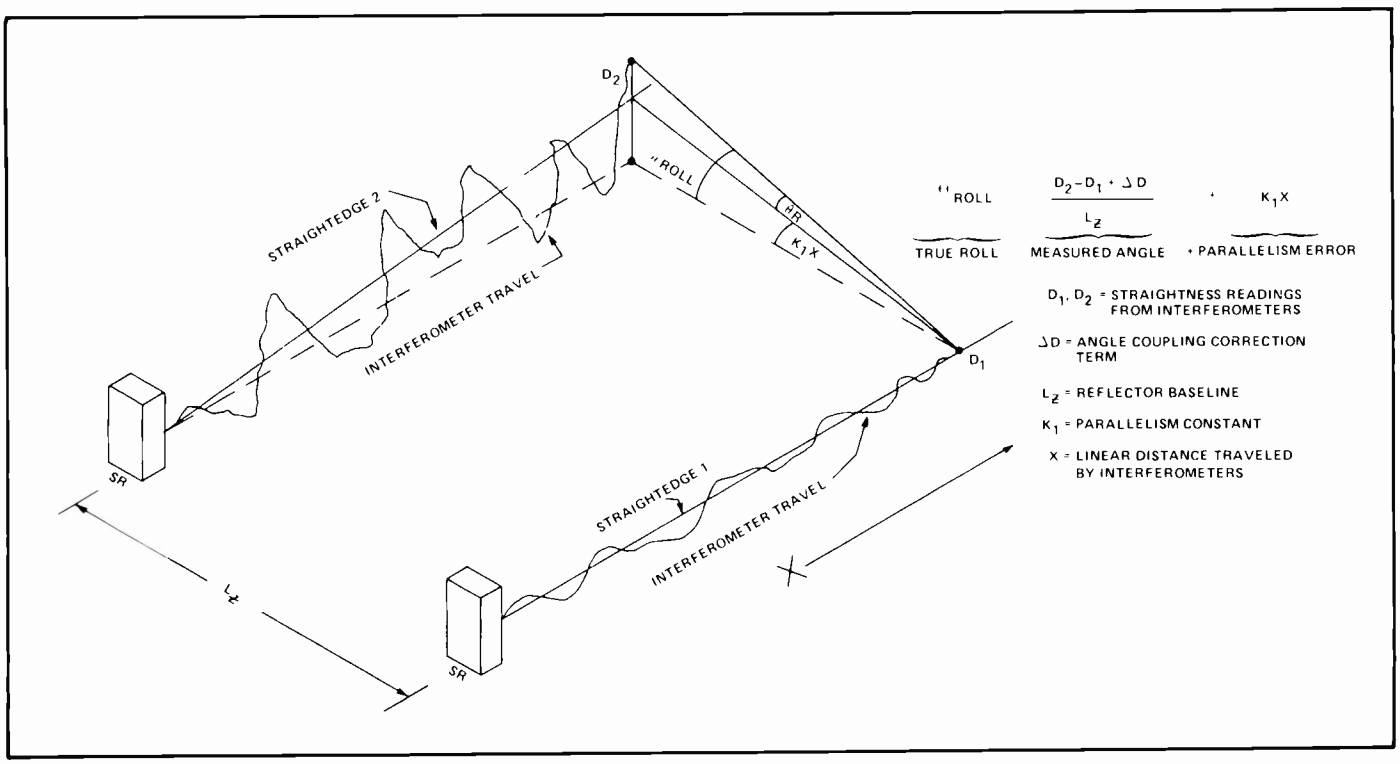


Fig. 5. *Laser roll angle sensing with straightedge misalignment.*

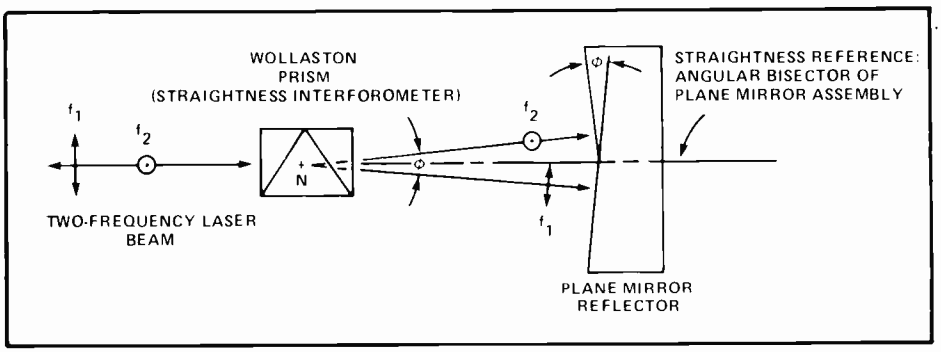


Fig. 6. *Straightness interferometer.[2] A Wollaston prism splits a laser beam into its two frequencies, f1 and f2 . An assembly containing two slightly angled plane mirrors then reflects the beams back through the prism. The phases of the two beams interfere with each other, thus providing data on optical path changes.*

Roll angle sensing

All scanner parameters are measured directly by the interferometers except for the two roll angles. At present, no interferometer exists that is capable of directly sensing a roll angle. To resolve this problem, the system uses data from two identical, displaced straightness systems (see Fig. 4) to mathematically derive the tower and carriage roll angles. The basic roll angle measurement configuration utilizing the two straightness interferometers is shown in Fig. 5. The reference straightedge, which defines the line of zero displacement, is optically determined by the perpendicular bisector of the two slightly angled mirrors constituting the HP straightness reflector. The angle of these mirrors is matched to the divergence angle of the Wollaston prism that constitutes the HP straightness interferometer (Fig. 6).

It is possible, and highly probable, that in the alignment of a straightness measurement system there will be a small degree of angular misalignment (on the order of microradians) between the optical straightedge and the interferometer line of travel. This phenomenon causes a slope in the straightness data directly proportional to the degree of angular misalignment. Since two straightness systems are used to indirectly measure the roll angle, there will be two different slopes corrupting the roll angle data. This non-parallelism of the two reference straightedges causes an artificial roll angle to be included in the data, proportional to the angular misalignment of the straightedges and the linear displacement of the interferometers along the line of travel. It is necessary to assess the parallelism in the measurement plane of these two straightedges in order to obtain a usable, common reference for the roll angle measurements.

A precision gravity level is used in conjunction with the two roll-angle straightness systems in order to determine the parallelism of the straightedges. This level is used to sense the true tower roll angle. The misalignment of the straightedges is determined mathematically by using the data from the level measurement, from the two straightness interferometers, and from a linear interferometer.

The misalignment is expressed in the form of a constant K in units of inverse distance. This constant is then multiplied by the linear distance traveled to obtain the artificial roll angle in radians. This quantity is then subtracted from the roll angle calculated from the straightness interferometer data to yield a value for the actual roll angle. A Federal Products electronic differential level on the one arcsecond resolution scale was used in this application in the system, and an HP85 minicomputer was employed for acquisition of laser data.

The tower roll angle is derived from data

obtained by the ΔYt and $\Delta Yt'$ straightness interferometers. The parallelism of the associated reflector straightedges is determined with the reflectors in their final positions on the fixed bench. The parallelism of the carriage roll angle reflectors, however, must be determined in a special setup before they can be placed into the system.

These two straightness reflectors are attached to a rigid housing that allows for independent reflector motion to facilitate the initial alignment. In this initial alignment, the reflector straightedges are oriented horizontally in a temporary setup on the optical bench. This allows the use of the gravity level on the tower to measure a true roll angle, and the measurement of carriage reflector parallelism is then made in the same manner as the tower reflectors.

After this parallelism has been determined, no further independent adjustments to the reflectors are allowed, ensuring that the relative orientation of the reflectors is not disturbed. When the carriage reflector housing is placed in its final position on a subplate under the optical shelf, the only adjustments to the pre-aligned reflector orientation are made by common motion of the entire housing. This restriction presents a uniquely difficult alignment task: the alignment of a vertical straightness system without adjustment to the straightness reflector; this alignment was achieved in the assembly of the scanner.

Remote probe tracking

Three benchmarks are established on the scanner to provide physical and mathematical reference points. The center of the X axis linear retroreflector is designated as the tower benchmark. Similarly, the center of the Y axis linear retroreflector becomes the carriage benchmark. The third benchmark is established at the center of the probe tip aperture, whose position in three-dimensional space is to be defined using displacements of the other two benchmarks as measured by the lasers.

Since lasers are an incremental measurement tool, a reference zero must be established. All lasers are set to zero with the tower and carriage in their mechanical stow position, and all laser measurements are made with respect to this stow position.

Gross displacements of the tower and carriage measured by the linear optics now become, by definition, linear displacements of the tower and carriage benchmarks. With the scanner in stow, precision length vectors between the three benchmarks are determined to assess the effects on probe tip motion of tower and carriage rotations obtained from the angle interferometers and the calculated roll angle. Small orthogonal displacements, measured by straightness interferometers, are treated as measurements made remote from a benchmark and are compensated for angle coupling effects, necessitating measurement of another series of vector lengths from the straightness interferometers to the appropriate benchmark. Any orthogonality error between the X and Y primary rails is measured using an optical square and is treated as an X axis displacement of the probe dependent upon the Y position of the carriage.

The position of the probe tip in three-dimensional space can be defined by a matrix equation (Fig. 7) that combines the probe displacement effects. Because of the post-scan data correction scheme, the accuracy of this probe position equation becomes the accuracy of the scanner.

Scanner verification

The proof of the probe position equation and scanner accuracy derives from the treatment of the tower and carriage as rigid bodies undergoing independent motions that contribute to the probe tip displacement. Probe motion is induced by these independent tower and carriage motions, all of which are measured by the internal scanner lasers. Since tower and carriage motions are independent, their effects on probe motion can be measured independently.

Both tower and carriage can cause the probe tip to move in three-dimensional space, resulting in six possible contributions to probe tip displacement. These contributions are designated X_x, Y_x, Z_x, X_y, Y_y, and Z_y, where the variable gives the direction of probe motion and the subscript denotes tower (x) or carriage (y) contribution. Once the differences between measured and calculated values of these displacements are determined, a Δ prefix is added to each of these terms to denote error in probe tip position calculated from that measured: ΔX_x, ΔY_x, ΔZ_x, ΔX_y, ΔY_y, and ΔZ_y. These are the final six scanner verification paths listed in Table I.

All measurements of probe tip displacement due to tower motions are performed with the carriage in stow position ($Y=0$) and all carriage dependent probe motions are measured with the tower in stow position ($X = 0$). Two further verification paths, $\Delta X_x'$ and $\Delta Z_x'$ have been included as additional checks on the algorithm with the carriage displace from the zero position ($Y > 0$) to assess the effects of this parameter on the probe position equation. In all cases, all lasers are reset to zero with the tower and carriage stowed.

During the verification a dummy probe was installed on the carriage and laser optical elements were mounted at positions approximating the final rf probe tip location. These elements were used in conjunction with an external Hewlett-Packard 5526A laser and appropriate straightness and linear components to determine displacements at the dummy probe tip. Displacement information from the scanner lasers was acquired, and the scanner was positioned under computer control.

The position of the dummy probe tip along the appropriate axis was calculated from this internal scanner laser data at specified grid points over the scan plane. This position was compared with measured values of probe tip displacement obtained from the external 5526A system and entered manually through a terminal keyboard. A granularity of 0.9 inch was used over the 26 feet of X travel, yielding 350 data points; the Y axis grid, established at 0.99 inch over the full 20 feet, yielded 241 data points. The deviations between measured and calcu-

$$\begin{bmatrix}\text{Probe}\\ \text{Position}\end{bmatrix} = \begin{bmatrix}\text{Linear}\\ \text{Displacements}\end{bmatrix} + \begin{bmatrix}\text{Orthogonality}\\ \text{Error}\end{bmatrix} + \begin{bmatrix}\text{Small Orthogonal Displacements}\\ \text{from Straightness Interferometers}\end{bmatrix}$$
$$+ \begin{bmatrix}\text{Tower Vector}\\ \text{Lengths}\end{bmatrix}\begin{bmatrix}\text{Tower}\\ \text{Rotations}\end{bmatrix} + \begin{bmatrix}\text{Carriage Vector}\\ \text{Lengths}\end{bmatrix}\begin{bmatrix}\text{Carriage}\\ \text{Rotations}\end{bmatrix}$$

Fig. 7. *Matrix equation defining probe tip displacement in three-dimensional space*

Table I. *Results of laser algorithm verification*

	Probe Tip Displacement Verification Errors (Inches RMS)		
Error Source	X Axis	Y Axis	Z Axis
Tower Motion			
Carriage Stowed (A)	0.0003	0.0010	0.0006
Carriage Displaced	0.0005	N/A	0.0016
Carriage Motion			
Tower Stowed (B)	0.0029	0.0001	0.0005
Orthogonality (C)	0.0011 (Max.)	N/A	N/A
Total $(A^2 + B^2 + C^2)^{1/2}$	0.0031	0.0010	0.0007
Specified	0.0040	0.0040	0.0040

Total Probe Position, Radial Error

System Requirement/Allocation: $0.0040\sqrt{3} = 0.0070''$

Current Performance: $[0.0031^2 + 0.0010^2 + 0.0007^2]^{1/2} = 0.0034''$

lated displacement were computed at each of these locations and analyzed for RMS error content. A Perkin-Elmer 3250 computer was used as the system controller for the verification.

Conclusions

The measured accuracies of the probe tip tracking algorithm show five of six verification paths to have errors in calculating the probe tip displacement in the range of 0.0001 inch to 0.001 inch RMS. Two of three axes, Y and Z, show a total position error also in that range (Y axis error = 0.0010 inch RMS; Z axis error = 0.0007 inch RMS). The X axis positional measurement accuracy, which includes an estimate of orthogonality measurement error, shows a 0.0031-inch RMS error.

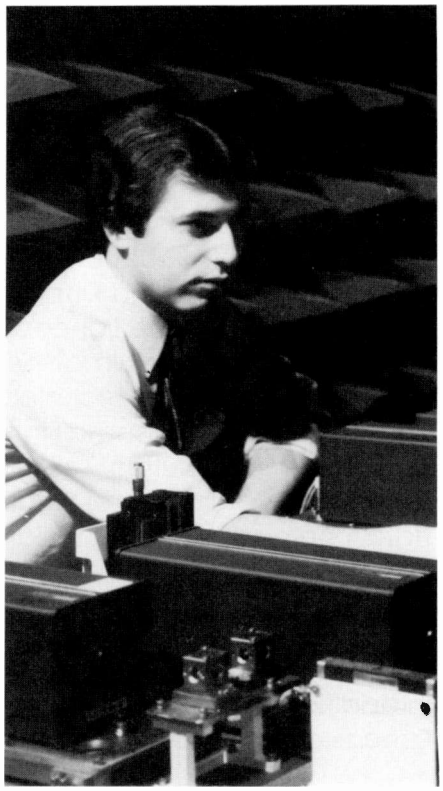
The measured 0.0034-inch RMS radial error is considered to be a conservative indication of the scanner performance for several reasons. This data includes residual errors from the external laser system, and the contribution of each scanner rotation is included twice in the verification. Also, an estimate of the maximum error due to uncertainty in the orthogonality measurement is included in the error summary rather than an RMS value.

The major contributor to the total scanner error resides in the ΔX_y path. While the other five verification paths show RMS errors ranging from 0.0001 inch to 0.001 inch, the residual error of the ΔX_y path alone was measured to be 0.0029 inch RMS, approximately three times greater than the next largest single error. The principal cause of this error is in the probe displacement induced by the carriage roll angle.

The inaccuracies in the measurement of this parameter are responsible for the relatively large ΔX_y error. With no vertical roll angle sensing, the ΔX_y path showed a 0.0038 inch RMS probe-position error. Therefore, while inclusion of the carriage roll angle correction into the probe position equation has provided an improvement over the uncorrected ΔX_y error, the correction effect is not as accurate as that provided by the tower roll angle measurements.

The difference in the accuracies between the calculation of the tower and carriage roll angles (the tower roll angle calculation is the main contributor to ΔY_x residual error of 0.0010 inch RMS) lies in the length of the baseline between the two reflectors. The baseline of the tower reflector measures approximately 66 inches, about 3:1 greater than the carriage reflector baseline. This baseline is the only significant difference in the layout and measurement method of these two systems.

The measured 0.0034 inch RMS radial error in probe position calculation provided by the laser calibration system was 2:1 under the specified error allocation of 0.007 inch RMS, and represents an unprecedented level of accuracy for a near-field scanner. In addition to its speed and accuracy, this automated laser measurement system has also shown a high degree of reliability in its first year of usage.



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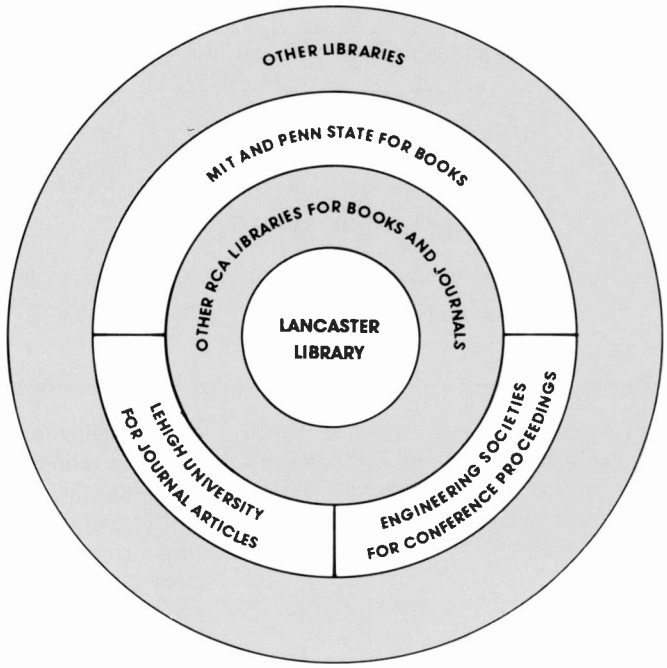

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- Service data on RCA videocassette recorders and VideoDisc players.
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W. A. Bösenberg | N. Goldsmith

Parametric testing of integrated circuits—an overview

Parametric testing is an essential element in adjusting the entire manufacturing process for maximum yield.

Parametric testing, as it applies to integrated circuits, requires sophisticated measurement equipment controlled by elaborate computer systems executing complex test programs. Most testing produces copious quantities of data that are reduced by other computers to make it comprehensible. In this introductory article we attempt to provide a general picture of how, and why, parametric testing is used in the design and manufacture of integrated circuits.

Test system description

Before describing how and why parametric testing is done, it is useful to understand the equipment used to make the tests. A number of different brands of equipment are used within RCA to make parametric tests. Despite the inevitable differences in details, all of the testers operate in fundamentally the same way. Figure 1 shows the block diagram of a typical test system operated by a dedicated minicomputer. One of the functions of the minicomputer is to control a set of test hardware in response to the commands of a test program. The same computer can also be used to generate the test program. The test hardware consists of programmable power supplies, meters, and an elaborate switching network. The computer can connect the test instruments using the switching network to, typically, any of 64 different output pins. These pins make contact, via probe cards, to pads on the circuits to be tested.

In addition to controlling the power supplies and the measurement equipment, the minicomputer stores the measured values onto disk files, and for archiving data, supports magnetic tape. In some systems the same computer that gathers the data is also used to analyze it. All of the test systems also incorporate an elaborate self-test routine to verify the accuracy and precision of the power supplies as well as testing to see that the switching matrix operates as expected.

Data analysis can be as complex a problem as testing. Every parametric test system we are familiar with comes with some provision for analyzing the data. Analysis reports are usually generated for each lot. However, when experiments are run, the reports have to be generated in accordance

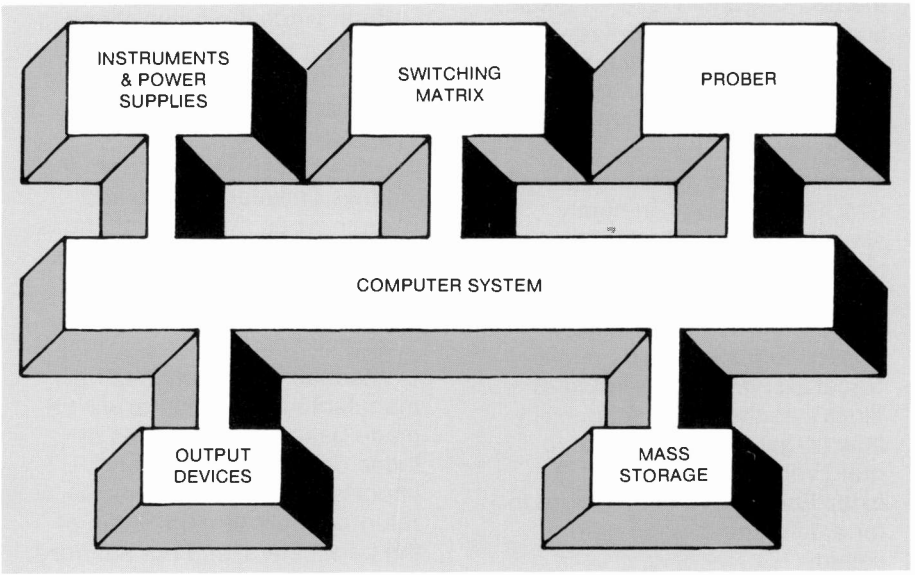

Fig. 1. *Typical test system operated by dedicated minicomputer.*

Abstract: *Parametric testing is widely used in the development and manufacture of integrated circuits. This paper introduces the reader to the basic concepts and provides an outline of how the elements of parametric testing work together.*

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Writing Test Programs—avoiding the gathering of garbage

Writing a WAT program that will measure the parameters sought is far from being an easy task. The article by Brehm illustrates an approach to building complex test programs from prewritten modules. The creation of the original modules and the specification of the order of application of the tests from these modules constitutes the true art of parametric test program generation.

Consider what happens in trying to establish the properties of the transistor shown in cross-section in Fig. A. The structure of the transistor is really quite simple. It has three electrodes called source (1), gate (2), and drain (3). The source and drain are of opposite conductivity type to the body (4). The gate is isolated from the body by a thin layer of insulation. In some technologies—notably CMOS—the body may be a region of opposite conductivity type diffused into the substrate. The transistor shown is an n-channel device, typical of p-well CMOS technology. In highly simplified terms, almost no current should flow from source to drain unless some minimum voltage (the threshold voltage) is applied to the gate. The curve-tracer display shown in Fig. B illustrates the expected current flow (Y-axis) as the source to drain voltage is increased (X-axis). Each curve in the figure is for a different value of gate voltage.

Integrated circuit designers and builders almost always describe a transistor in terms of its size (length and width) along with an extensive set of parameters that describe how well it operates. In fact, the design of circuits is based upon mathematical models of how a transistor operates, and the value of the parameters that are used in the model are derived from parametric testing. Three of the most common parameters are:

1. **Threshold voltage**—the minimum voltage that has to be applied to the gate to cause a specified current to flow between source and drain when a bias voltage is applied between the latter two electrodes.
2. **Leakage current**—the current that flows between source and drain when the gate voltage is zero (or at some voltage less than the threshold voltage) for a given bias between source and drain.
3. **Drive current**—the current that flows between source and drain when the gate voltage is at some predetermined value above threshold and a bias voltage is applied between source and drain.

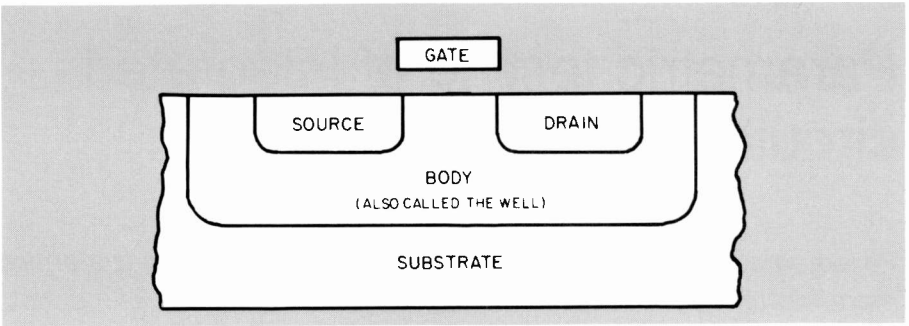

Fig. A. *Cross-section of a typical n-channel CMOS transistor.*

The main text describes how manufacturing decisions will be made based on the values of these parameters. It is very important that the data that is returned represent the value of the parameters, and not arbitrary currents and voltages. The temptation of the first-time user of a parametric test system is to simply apply the voltage or current called for in the test specification and obtain the relevant parameter. A much safer procedure is to first verify that the transistor being measured meets certain criteria. These criteria attempt to answer the question "is this structure a valid transistor?" The test sequence given below is used to answer that question. Failure to pass any of the tests will cause the test program to skip over that transistor. None of the data derived from it will appear in the database.

1. **Diode tests**—a set of tests are made on all of the diodes of the MOS transistor structure. These tests also confirm continuity between the tester pin and some part of the MOS transistor.

a. Apply a foward current and measure the voltage. Voltages below a lower limit are shorted diodes. Voltages above a high limit are open diodes or connections. Failure of either test aborts further tests.

b. Apply the voltage found in step a and measure the current. If the ratio of the foward current to this current is less than a limit, then the diode is a failure (does not rectify).

2. **Gate isolation test**—check to see if the gate is shorted to any of the other electrodes of the device. There is no way to test for open gates unless two probe pads are dedicated to one gate. Passing the transistor action test (below) guarantees that the gate is not open.

a. Ground all of the device terminals except the gate. Apply a test voltage to the gate and measure the current. If the current is greater than some limit, the device fails.

3. **Transistor action test**—check to see that the gate controls the current flowing from source to drain.

a. A small bias voltage is placed on the drain, typically 0.1V. A

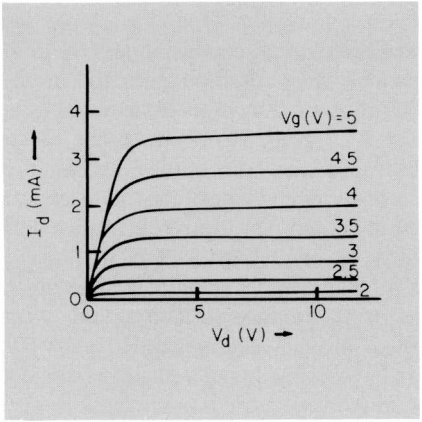

Fig. B. *Current flow as a function of drain current.*

small voltage (safely below the anticipated threshold voltage of the transistor) is applied to the gate. The source-drain current is measured. Devices are rejected as shorts if too high a current flows.

b. The same test as in a, but the voltage on the gate is chosen well above the anticipated threshold voltage. If the source-drain current is too high, the device is rejected as a short. If the source-drain current is too low, the device is rejected as being open. If the ratio of the second test to the first test is less than some chosen limit, the device is rejected for failing to show transistor action.

Transistors that pass all of these initial suitability tests are acceptable for parametric testing. Failure to test for suitability will "contaminate" the data base with values for improperly functioning devices.

The combination of these tests ensure that the source-to-drain current is controlled by the application of voltage to the gate and between the source-drain electrodes, not by unanticipated shorts in one or more of the electrodes. The tests also ensure that contact is continuous from the tester's computer-controlled power supplies and meters down to the electrodes of the transistor.

with the way the lot was subdivided. Most analysis systems provide for the generation of histograms, calculation of common statistical measures, historical or trend analysis, and the calculation of parameters derived from a set or sets of measurements. Graphical output is sometimes supported in the form of scatter plots of one or more variables against each other or the mapping of parameters using two- or three-dimensional plots. In general, the analysis of data is a separable function from that of testing. Sometimes the analyses are complex enough to require the use of a separate computer. F. Brehm's article in this issue discusses one approach to data analysis that has been followed by RCA Laboratories.

Parametric testing and circuit manufacturing

Although parametric testing is heavily used during the manufacture of integrated circuits, it is only indirectly connected with the functioning of specific products (see the article by F. McCarty in this issue). The prime function of parametric testing in an integrated circuit manufacturing environment is to ensure that the complicated fabrication process used to produce the integrated circuit has been completed satisfactorily. Unlike functional testing, which verifies that the circuits operate as required, parametric testing returns numeric values. Most integrated circuit fabrication lines require that the results of parametric testing must be within defined limits before the wafers will be released for functional testing. When used for this purpose parametric testing is often called WAT—wafer acceptance testing. For brevity, we will adopt the acronym to describe all uses of parametric testing. WAT serves a number of purposes for a manufacturing operation. The primary function is to avoid costly functional testing of parts that are unlikely to operate. The values of the parameters that are measured can be used to provide feedback to correct processing errors or drifts in the manufacturing process. Parametric testing, in fact, is an essential element in adjusting the entire manufacturing process so as to maximize the yield.

WAT is performed on special test structures that appear on each wafer processed through a manufacturing line. These structures are most often elements that are used in the circuits being manufactured; diodes, transistors, resistors and capacitors, for example. The same set of test structures appears on every wafer, independent of the changing nature of the product on the

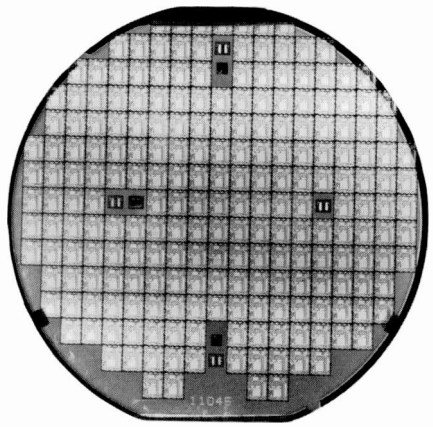

Fig. 2. *Typical wafer, showing knock-out positions.*

wafer. The test structures are usually grouped together to form a "chip." This pseudo-chip replaces one or more product chips on the mask, and is called a "knock-out" (for obvious reasons) or a "WAT key." The photograph in Fig. 2 shows a typical wafer as it appears at the end of the manufacturing cycle. The arrow points to one of the knock-out locations. The other knock-out positions are readily apparent in the photograph. Figure 3 is an enlarged view of a typical WAT key used in RCA factories.

Early in the development of a new technology it is not at all unusual to manufacture only test chips. The test structures used for technology development almost always address one type or another of a geometric question. A typical question would be "How close can one structure be placed to another without electrical interaction?" The test structures frequently address new ways of making circuit elements. To that end the mask set will probably include many more levels than will be found in the production set.

Once the basic fabrication technology has been defined, the manufacturing of the initial product (circuit) is begun. At this early stage of manufacturing as many as a third of the product sites on a wafer may be replaced by test chips. The test chip will replicate many of the important test structures used to develop the technology. A necessary condition of technology transfer from a laboratory or development activity to a manufacturing environment is the ability of the learning location to replicate the electrical properties of specific test structures. Once the process is stable, and large scale manufacturing of a product family has begun, the number of test chips is reduced to only four or five on a wafer. Sometimes the test structures are placed in the "streets", i.e. in the spaces between the chips that are

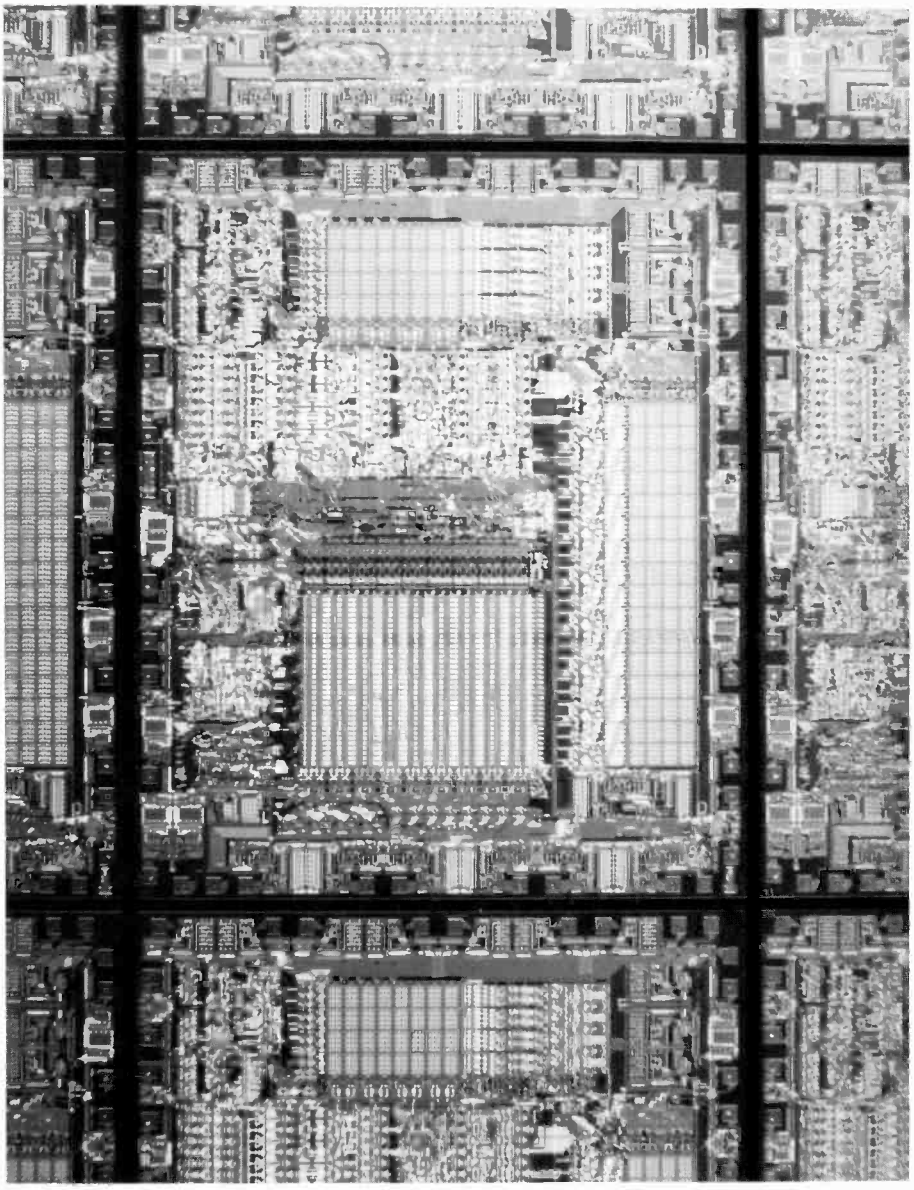

Fig. 3. *Typical WAT key.*

left to allow them to be cut apart from one another at the end of the manufacturing cycle. This latter approach is required when using wafer steppers that lack rapid, automatic reticle changers.

As you might imagine, there are many communities involved in the design, manufacturing, and testing of integrated circuits that require information about the status of the manufacturing line. Designers want information on the possibility of fabricating structures that are smaller than those on the present circuits so that they can shrink old parts in a cost-effective manner. Process engineers want information that they can use to bring the manufacturing procedures under tighter control by identifying those operations that detract from yield. Product engineering uses information derived from WAT to shift the fabrication process so as to yield greater proportions of premium priced products. The net result of these differing needs is that competition for space on a WAT key is intense. Furthermore, the WAT key itself must be kept small to minimize the loss of productive space on the wafer. This loss can be significant if the product dice are large. All of these compstitive pressures combine to make the design of an effective WAT key as difficult a job as the design of a new product.

The use of automatic testing equipment results in the need for large pads (typically 80 x 80 micrometers) within the WAT key to ensure proper contact of the probes. Most WAT key designs turn out to be limited by the number of pads that can be placed in the area allocated to the die. A single transistor, for example, may be hardly 1/100th of the area of a pad, yet a minimum of three pads are needed in order to test a transistor. One can arrange test transistors so that common types (n- or p-channel) have common gates and drains. This allows k transistors to be tested using only $k+2$ pads. However, if one of the electrodes in any one of the k transistors is shorted or open, none of the transistors can be fully tested. The awareness of such difficulties is one of the factors that makes WAT key designs so difficult. The objective is to produce structures that, when tested, provide unambiguous results that can be associated with a single process step or, at the very most, a single mask level.

A typical WAT program will contain as many as 100 tests and even more test statements. The most important parameters derived from WAT testing, for the control of a manufacturing line, are those that describe how well controlled the transistors are and those that describe how well the resistances of the various layers have been controlled. The parameters that describe transistor operation are threshold voltage, drive current, leakage current and breakdown voltage. The resistances are used to verify the proper operation of processes such as implantation, diffusion, oxidation, contact, formation, and occasionally, dimensional control.

Applications of parametric testing

Parametric testing is not limited to the gathering of electrical characteristics of circuit elements. It is possible to design structures whose electrical properties vary with size and placement. The sizes associated with the transistor also can be derived from a set of electrical measurements followed by proper data reduction.

RCA researchers were early pioneers in the use of parametric testing for yield prediction and yield analysis. Ipri and Sarace[1] showed that special patterns, which covered the entire wafer, could be designed to test the ability of the process to isolate and connect circuit elements. For example, metal continuity yield can be predicted from a measurement of meandering lines of varying length. The probability of a metal line being continuous decreases if the line is made narrower at the same length or is made longer at the same width. Knowledge of how the yield decreases with length and width allows the designer to optimize the number of good die per wafer.

In the case of yield analysis, W. Ham and A. Crossley[2] showed that it was particularly

useful to "map" the various parameters that were measured. Two-and three-dimensional displays of the transistor parameters discussed in the sidebar are often used to track down problems that arise in the manufacturing process. Patterns that repeat from lot to lot, for example, will point to process steps where the geometric orientation of the wafer and the manufacturing tool are fixed.

Another example of the advanced use of parametric testing is in the derivation of the complex factors that go into a modern transistor model. The input data is derived from parametric tests.

Conclusion

Parametric tests continue to grow both in number and in degree of complexity. We expect that this trend will continue or even accelerate to keep pace the growing complexity and shrinking feature size of integrated circuits. The advantages of increased complexity and speed of modern integrated circuits are obtained at the expense of longer and more intricate manufacturing methods. Parametric testing has become the indispensable tool in developing and maintaining new and efficient manufacturing methods.

References

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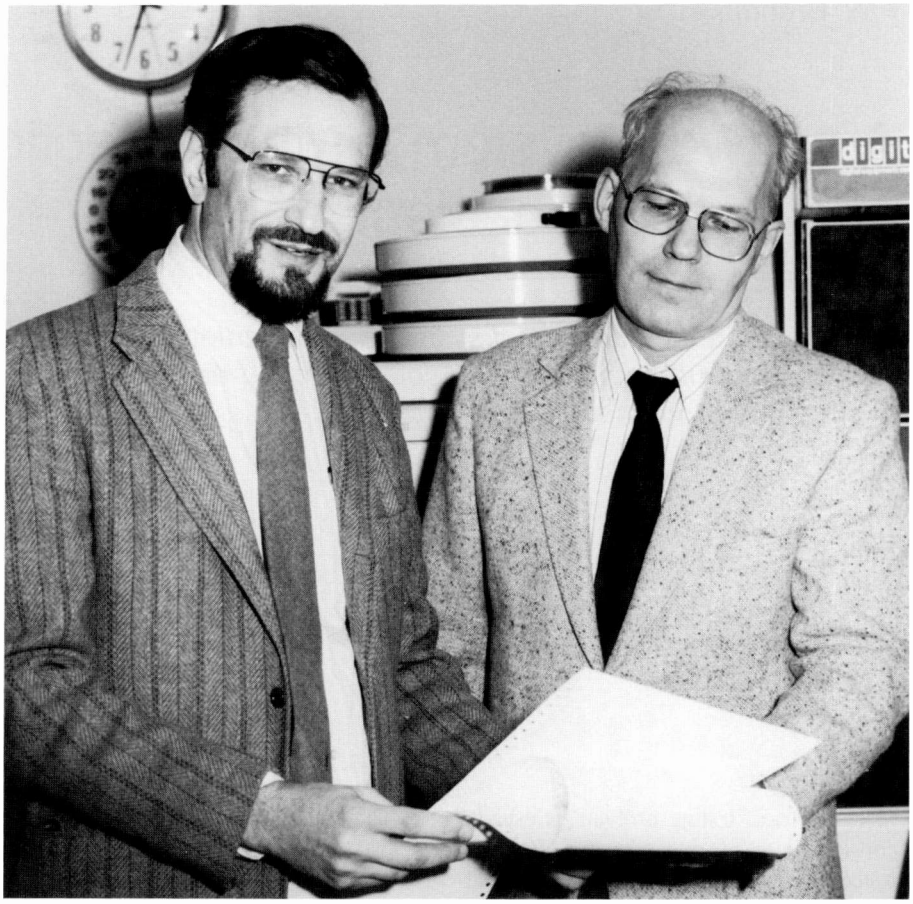

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F.W. Brehm

A software system for the collection and analysis of electrical data

Programming a complex test system can be tedious and time consuming, but the right kind of software can free the programmer from much of the drudgery.

The electrical testing problem is usually considered to be one where a circuit is tested for proper function: making sure that a memory remembers, or that a gate is logical, for example. The "functional" characteristics produced by this kind of test are useful for checking the design of a circuit. However, these tests yield little information about the design of the process or devices used to build the circuit. This kind of information is provided by another type of electrical testing: parametric testing.

Parametric testing is used to characterize the devices that make up a circuit and to provide information to the manufacturer about the quality of the process. For circuits made of discrete components—resistors, capacitors, individual transistors, etc.—parametric testing is performed by the manufacturer of the parts. The information needed by a circuit designer is collected into "spec sheets," while other control information is kept by the manufacturer.

Abstract: *Enough electrical data must be collected to make statistically significant statements about the performance of an experimental design for manufacturing large scale integrated circuits. The system described in this article aids in the collection and analysis of this data.*

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The Integrated Circuit Laboratory at the David Sarnoff Research Center, like a component manufacturer, is engaged in the design of the processes and devices used to manufacture integrated circuits. The data used in this design process are collected by several means. Optical methods may be used to measure parameters such as film thickness. The electron microscope may be used to study physical structures. The eventual goal, however, is to produce electrically active components on a silicon wafer. Enough electrical data must be collected to make statistically significant statements about the performance of an experimental design for manufacturing large scale integrated circuits. The system described in this article aids in the collection and analysis of this data.

System overview

The requirements of the system design are dictated largely by the interests of the researchers at RCA Laboratories. People who become expert in the use of a large and expensive tester are more interested in doing their own research than in writing test programs to gather data for another person's experiment. Conversely, there are many people who wish to use the tester but do not have the interest or time to learn how to program it. Therefore, the system must be able to collect the knowledge of the expert in an unobtrusive manner and allow another person to use the knowledge easily.

A study of the typical experimental method produces additional requirements. The experimental vehicle is usually a silicon wafer with many copies of a test pattern on its surface. This test pattern may contain one or more devices to be tested. The test procedure requires that measurements on each device of interest be saved with the location of the device and other identifying information. The information collected during testing should be presented by graphical and statistical methods.

The nature of process and device research results in a short lifetime for most test programs. This means that writing and running the test program and analyzing the data should be easy and reliable. The testing and analysis programs do not have to be as efficient as those used in a factory, because the goal is to optimize the efficiency of people, not of equipment.

A data flow diagram [1,2] of the overall system is shown in Fig. 1. An expert in testing or a device physicist designs an algorithm to be used for testing some structure. A computer code called the test function is developed to perform the algorithm while taking into account all of the peculiarities of the hardware on which it runs. This function is inserted into a library that is available to all who use the tester.

An experimenter who has the matching structure on a test wafer may use this function in a test program by supplying device

names, the test to be performed, and the other values required by the function. The program generator produces a test program and an analysis program. The test program is used to gather data from the wafer, and the analysis program produces wafer maps, histograms, and statistics.

The library

A library is divided into three parts: STRUCTURE definitions, FUNCTION definitions, and SUBROUTINE definitions. A STRUCTURE definition contains the menu of functions that may be used and the list of common values that every function uses. These values are usually the pad connections. A FUNCTION definition has the name of the subroutine that contains the code to perform the function and a list of values to be supplied. These values are usually the stimulus and limit values for power supplies. A SUBROUTINE definition contains a list of declarations of inputs and outputs that must be supplied, and the actual code to perform the measurement.

Figure 2 is a listing of a small library. This library is incomplete for several reasons. First, the FUNCTION and SUBROUTINE definitions are missing for the Res2V and Res4 functions named on lines 6 and 7 of the listing. Second, the functions in the menu are not enough to test the wide variety of resistor structures that exist. Finally, resistors are not the only structures that can be tested. These omissions will have no effect on the test program shown later, but a useful library will be more complete.

Notice the amount of internal documentation in the STRUCTURE and FUNCTION blocks. These are the two parts of the library that will be read by the person who writes a test program. This documentation, when written properly, allows a test programmer to use the library independently of the person who developed the test function.

This decoupling satisfies a major goal of the design. An expert can devote more time to developing new tests for old structures, or new structures that are sensitive to different conditions. Time is not wasted on written before. In most cases, a researcher may write a test program that will work the first time without having to consult with the person who is the expert on the testing system.

The SUBROUTINE block begins with declarations of all inputs (lines 37 through 44) and outputs (lines 45 through 49). The set of inputs should equal the set of values named in the ASK lines of the STRUCTURE and FUNCTION blocks. The SUBROUTINE will return values for one or more RESPONSE, and for one of the ERROR values.

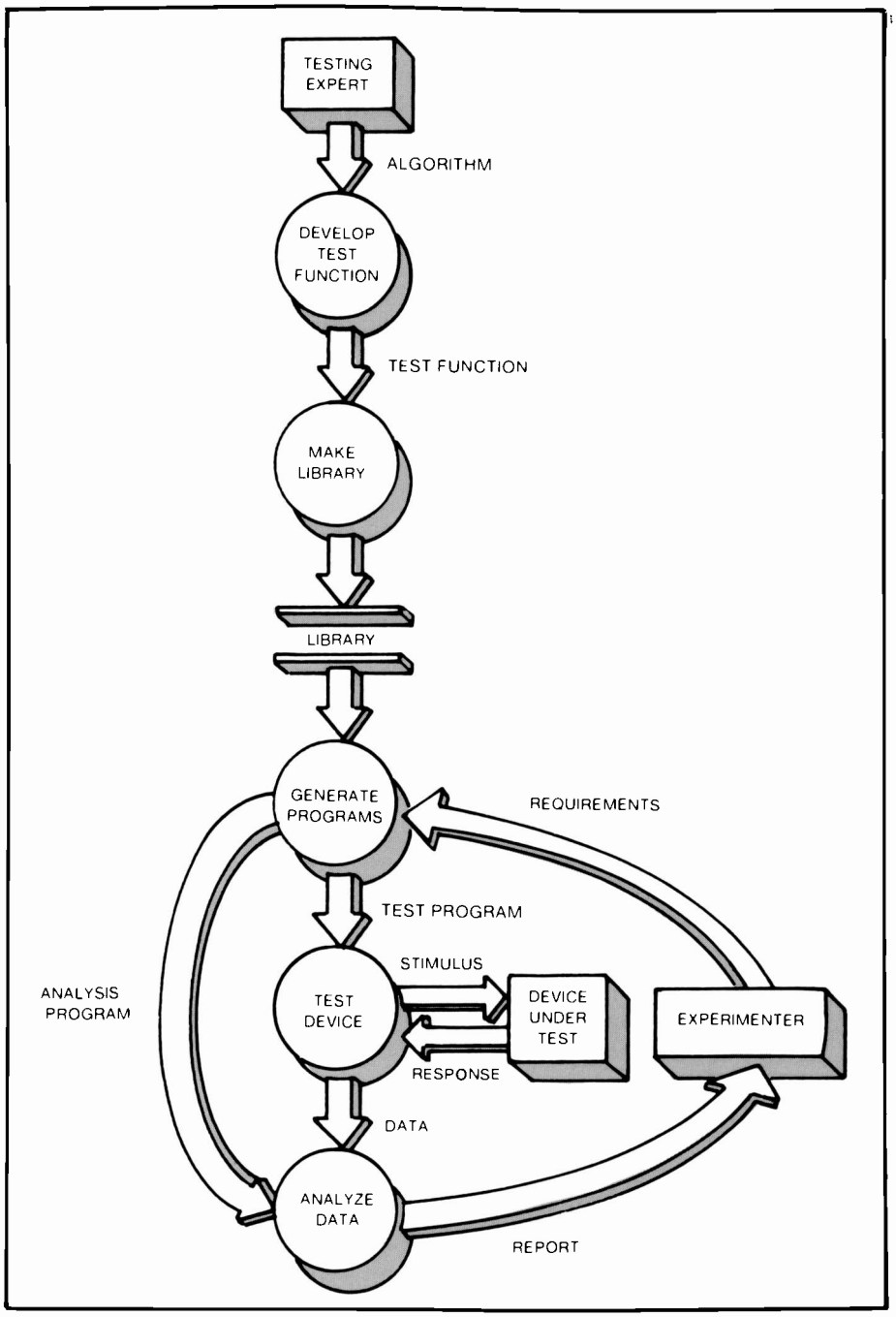

Fig. 1. *Parametric test system structure.*

There are several things to notice in the code of the SUBROUTINE in the illustration. All these were put in by the author of the routine, but probably would have been missed by an inexperienced or sloppy programmer. Line 61 contains a check for a power supply compliance limit. Failure to comply will cause erroneous values to be returned for the resistance of an open circuit. The resistance is assigned a value defined to be "OverRange", and the error code "Open" is returned. Line 68 checks that the absolute value of the measured voltage is not less than a value called "VM1Accuracy." This check was inserted after noticing that the routine sometimes gave negative values of resistance for a short circuit. The resistance is assigned a value of zero, and the error code "Short" is returned. Line 74 contains an explicit check for divide-by-zero. This protects against a nasty run-time error that is the result of a coding error in the test program. In this case

```
The numbers on the left are not part of the library.  They are for
reference only.  The sharp character ("#") introduces a comment.

 1  LIBRARY Sample "A consistent (if incomplete) library."
 2
 3  STRUCTURE Resistor "Resistor Structures"
 4      MENU
 5          Res2    "Two terminal resistance measurement"
 6      ,   Res2V   "Two terminal resistance measurement (force voltage)"
 7      ,   Res4    "Four terminal resistance measurement"
 8      ASK
 9          LO      "Ground connection"
10      ,   HI      "Connection for current or voltage application"
11      ,   C est   "Approximate capacitance of structure in farads"
12                  DEFAULT = 0.0
13      HELP
14          Resistances may be measured on two terminal or four terminal
15          devices.  The C est value should be supplied if the structure
16          has an area large enough that the charging time is
17          appreciable.
18      END
19
20  FUNCTION Res2 "Two terminal resistance measurement"
21      ASK
22          I       "Current to force"
23      ,   V max   "Compliance voltage for current source"
24                  DEFAULT = 100.0
25      CALL res2
26      HELP
27          The current I is forced from the HI to LO connections with a
28          voltage limit of V max.  The resulting voltage is measured
29          and the resistance R is calculated.  If the voltage is less
30          then the voltmeter accuracy then the resistance will be zero.
31          and the error "Short" will be returned.  If the compliance
32          limit V max is reached then the resistance will be OverRange
33          and the error "Open" will be returned.
34      END
35
36  SUBROUTINE res2 "Two terminal resistance measurement."
37      PIN
38          LO      "Ground connection"
39      ,   HI      "Connection for current or voltage application"
40      STIMULUS
41          I       "Current to force from current source"
42      LIMIT
43          V max   "Compliance voltage for current source"
44      ,   C est   "Approximate capacitance of structure"
45      RESPONSE
46          R       "Measured resistance"
47      ERROR
48          Open  = 1       "Resistance too high to measure"
49      ,   Short = 2       "Resistance too low to measure"
50      CODE
51          real      v
52          external file, mv1
53          integer   file
54          real      mv1
55
56          # CONNECT
57          call pin3 (LO, GND, VM1L)
58          call pin3 (HI, IS1, VM1H)
59
60          # FORCE
61          if (file(I, V max, C est) ~= InRange) { # compliance limit
62              R = OverRange
63              return (Open)
64              }
65
66          # MEASURE
67          v = mv1()
68          if (abs(v) <= VM1Accuracy) { # accuracy limit
69              R = 0.0
70              return (Short)
71              }
72
73          # CALCULATE
74          if (I ~= 0.0) # don't divide by 0
75              R = v/I
76      END
```

Fig. 2. *A sample library.*

the resistance is left undefined and would be considered "Empty" by the analysis routines.

The numbers on the left are not part of the library. They are for reference only. The sharp character (#) introduces a comment.

The program

To illustrate the programming process, let us suppose that we must investigate the uniformity of a polysilicon patterning process over the whole area of a wafer. We have a test pattern that contains a resistor whose value is proportional to the line width produced by the process. (A real test pattern would contain more devices because other factors may cause the resistance to change.) We know to expect resistances of about 10k ohms. This test pattern will be repeated many times on the wafer. The program to test the resistor is shown in Fig. 3.

The items named in the ASK list of the resistor library are defined on lines 8 and 9. The "C est" item will have a value of 0.0 as specified by the DEFAULT value in the library. The stimulus current and limit voltage are specified in lines 13 and 14. This program is quite small compared to one written from scratch. It does not have any explicit output statements, nor does it tell anything about the repetition of the test pattern. Instead it concentrates on the measurement of a single resistor.

The output statements are generated by the program generator from information in the library. The measurement program will be invoked each time the probes are resting on the test pattern. The measurements made by the test program will be stored along with the location of the pattern, the experiment identification, and the wafer identification.

This is another instance of decoupling in the system. The test programmer does not have to learn the exact format of the data files that the analysis program reads, and more importantly, cannot make mistakes in writing the code. The instructions to make the wafer prober work may also remain (blissfully) unknown.

This simple program cannot illustrate all of the facilities of the program generator. A stimulus value may be a function of a previously measured result. For example, the drive current of an MOS transistor may be measured at a gate bias several volts higher than the measured threshold voltage. The IF-THEN-ELSE control structure may be used to modify the flow of testing to avoid contaminating the data with measurements on devices that are not functioning properly. For example, it makes little sense to perform measurements that characterize the behavior of a MOS transistor if the threshold voltage changes after a stress is applied.

Running the program

A set of wafers (usually called a lot) is tested by giving the wafers and pertinent information to the system operator. The required information includes the probe card, the experiment or lot identification, and the

size of the pattern to probe. When the operator mounts each wafer on the prober the identity of the wafer and the name of the program must be supplied. The operator initiates the analysis by answering a few more questions, and the analysis printouts are delivered to the researcher.

The interaction between the operator and the test program is always the same, so operators do not have to go through a training period for each new program. This is a big advantage because a test program may be used to test only a few wafers.

The program generator provides more facilities that may not be appreciated by someone who has never tried to write and debug a test program. Debugging statements that may be enabled at run time are inserted by the program generator. This is invaluable when trying a new test program, or when the system hardware or a library function is suspected of misbehaving.

The numbers on the left are not part of the program. They are for reference only. The sharp character (#) introduces a comment.

The data analysis

The sample printout shown in Fig. 4 is, except for one detail, the default printout of the analysis system. The one detail is the format of the histogram. The portion of the sample program that produced this printout is shown in Fig. 5. Line 19 has been replaced by line 20, which sets the endpoints of the histogram display to 0 and 30,000. The number of categories, or bars, in the histogram was changed from 50 in line 21 to 60 in line 22. This produces a rational scale on the horizontal axis.

We can now see the result of our experiment. The patterning process has produced almost a two-to-one variation in line width over the wafer (see lines 21 and 22). The wafer map (lines 26 to 37) shows that the variation is strongly related to the position on the wafer. It looks like this test program will be used again!

Line 1 contains the lot, wafer, and program identification as entered by the operator. Notice that this is the second page of the analysis printout. The first page contains items such as the date and time the wafer was tested, the version number of the test program, and some information used by the system. Lines 3 through 5 contain the device, test, and response names from the test program. This is followed by a histogram (HIST), some statistics (STAT), a wafer map (MAP), and a population table (TABLE) for the wafer map. The first line of each of these contains the type of display, the internal test number, and the test title.

The graphics are low resolution because a line printer is used as the output device. This is sufficient for a quick look at the data. If high resolution graphics or multivariate

```
The numbers on the left are not part of the program.  They are for
reference only.  The sharp character ("#") introduces a comment.

 1 PROGRAM Poly "A program to measure one resistor."
 2  FROM LIBRARY Sample
 3
 4  VERSION 1.0   "F. Brehm for RCA Engineer"
 5
 6  DEVICE Poly "Poly resistor."
 7  IS STRUCTURE Resistor
 8      LO = 10 # Resistor common pad
 9      HI = 15 # Poly pad
10
11      TEST Res "Resistance of Poly resistor."
12      USE FUNCTION Res2
13          I      = 1E-4        # amps
14          V max  = 10.0        # volts
15          END TEST
16
17      END DEVICE
18  END
```

Fig. 3. *A sample program.*

```
The line numbers do not appear in the actual printout.  They are for
reference only.

 1  Lot EXP1 Wafer 2 Program POLY                                  Page 2
 2
 3  Device    POLY     Poly resistor.
 4  Test      RES      Resistance of Poly resistor.
 5  Response  R        Measured resistance
 6
 7  HIST   test      1 POLY:RES:R
 8     5|+    +    +    +    ++   +    +    +    +    +    +    +    +    |
 9     4|                     *    *                                       |
10     3|                     **** *                                       |
11     2|                    ***** *  **   *                               |
12     1|                    ******** ******  *                            |
13     0|+----+----+----+----+----+----+----+----+----+----+----+----+----|
14   0.00       5.00E+03  1.00E+04  1.50E+04  2.00E+04  2.50E+04
15        2.50E+03  7.50E+03  1.25E+04  1.75E+04  2.25E+04  2.75E+04
16         60  LIN categories from  0.00000      to   30000.
17
18  STAT   test      1 POLY:RES:R
19   Of   32 Observations   Of   32 Passing          32 Analyzed  LIN
20      0 <= UnderRange          0 <    6638.        Mean    =  1.3186E+04
21   Min   =  1.0113E+04    Min  =  1.0113E+04    Median  =  1.2738E+04
22   Max   =  1.8750E+04    Max  =  1.8750E+04    Std Dev =   2355.
23      0 >= OverRange           0 >  2.0888E+04    C of V  =  17.86%
24      0 Illegal Values      Pass = 100.00%       Analyze = 100.00%
25
26  MAP    test      1 POLY:RES:R
27      X =    499 to    504;  Y =    500 to    505
28           500
29          |-+----|
30      500+ 1111 +
31      501|111222|
32      502|322333|
33      503|444445|
34      504|666678|
35      505+ 989A +
36          |-+----|
37           500
38
39  TABLE  test      1 POLY:RES:R
40    Category Pop.  Low Limit      Minimum      Maximum      High Limit
41        1 (1)     7  1.0113E+04   1.0113E+04   1.0962E+04   1.0976E+04
42        2 (2)     5  1.0976E+04   1.1175E+04   1.1825E+04   1.1840E+04
43        3 (3)     4  1.1840E+04   1.1988E+04   1.2488E+04   1.2704E+04
44        4 (4)     5  1.2704E+04   1.2988E+04   1.3463E+04   1.3567E+04
45        5 (5)     1  1.3567E+04   1.3863E+04   1.3863E+04   1.4431E+04
46        6 (6)     4  1.4431E+04   1.4525E+04   1.5213E+04   1.5295E+04
47        7 (7)     1  1.5295E+04   1.5863E+04   1.5863E+04   1.6159E+04
48        8 (8)     2  1.6159E+04   1.6250E+04   1.6738E+04   1.7022E+04
49        9 (9)     2  1.7022E+04   1.7175E+04   1.7350E+04   1.7886E+04
50       10 (A)     1  1.7886E+04   1.8750E+04   1.8750E+04   1.8750E+04
51            10  LIN categories from   10113.      to   18750.
```

Fig. 4. *A sample analysis printout.*

```
The numbers on the left are not part of the analysis program.  They
are for reference only.  The sharp character ("#") introduces a
comment.

  1  # 0001 POLY:RES:R Measured resistance
  2       TOP
  3       C Device     POLY     Poly resistor.
  4       C Test       RES      Resistance of Poly resistor.
  5       C Response   R        Measured resistance
  6       #
  7       # Get the data
  8       TEST 0001
  9       TITLE POLY:RES:R
 10       DISTRIBUTION normal
 11       POLARITY     default
 12       PASS         underrange overrange
 13       #
 14       # Scale data as necessary
 15      #NEG ABS MULT RECIPROCAL etc.
 16      #TITLE POLY:RES:R
 17       #
 18       # Histogram
 19       #DISPLAY      default
 20       DISPLAY      0 30000
 21       #BARS         50
 22       BARS         60
 23       HIST
 24       #
 25       # Statistical summary
 26       LIMIT        default
 27       STAT
 28       #
 29       # Wafer map and population table
 30       BARS         10
 31      #LIMIT        default
 32      #DISPLAY      default
 33       AVERAGE
 34       MAP
 35       TABLE
```

Fig. 5. *The analysis program.*

analysis is required, then the data of interest may be written to a file in tabular form for processing by another program.

The histogram is constructed by dividing the display range into a number of categories and counting the number of data values that fall into each category. A vertical bar with height proportional to the count is drawn for each category. The wafer map is constructed the same way except for the final display. Each location on the wafer map represents a test site. The code letter shows the category for the measurement on that site. The table shown below the wafer map represents the population of each category in the map. Note that a plot of population ("Pop.") versus "Low Limit" would be a histogram.

The data axis is linear in this example. The data axis should be logarithmic for measurements such as transistor leakage current. When the data axis is logarithmic the size of each category is some multiple of the previous category. For example, dividing the range 1 to 1000 into three logarithmic categories would give the following table:

Category	Low Limit	High Limit
1	1.0	10.0
2	10.0	100.0
3	00.0	1000.0

The statistics table is divided into three columns. The first column represents all of the data. A PASS range (line 12 in Fig. 5) is defined to exclude any data that are measurement failures. In this example the PASS range could have been defined as 0.0 to OverRange, but it would not have made any difference. Additional data may be excluded for logarithmic statistics if they are not positive.

The second column represents all of the good measurements, but not necessarily all of the good data. If *a priori* knowledge exists about a "good" data range, then the LIMIT statement may be used to define it in the analysis program (line 26 in Fig. 5). The default limits are computed by a statistical procedure that attempts to remove any outliers or data points that are probably erroneous. The procedure is a modification of the method used to calculate fences in a boxplot.[3] It was developed by Achilles Kokkas with help from Russ Barton and Don Barton. No assumptions are made about the distribution of the data. The first, second, and third quartiles of the passing data are calculated. Call these q_1, q_2, and q_3. The limits are calculated by the following formulas:

$$\text{Low Limit} = q_1 - 3.0 * (q_1 - q_1)$$

$$\text{High Limit} = q_3 + 3.0 * (q_3 - q_2)$$

The third column gives some statistics for data that fall within both sets of limits. "Mean" and "Std Dev" are the sample mean and sample standard deviation, respectively. They are computed in the usual way when the data distribution is defined to be "NORMAL." For "LOGNORMAL" data the sample mean (μ) and sample standard deviation (σ) of the logarithm of the data values are computed. The printed statistics are calculated as follows:

$$\text{Let } w = e^{\sigma^2}$$

$$\text{and } m = e^{\mu}$$

$$\text{Then Mean} = m \cdot e^{\sigma^2/2}$$

$$\text{Std Dev} = m\sqrt{w^2 - w}$$

The coefficient of variation ("C of V") is the "Std Dev" divided by the "Mean" in percent.

The mean and standard deviation are quantitatively meaningless when the distribution is unknown. These statistics appear for historical reasons. Many people are familiar with these numbers and are uncomfortable with anything different. It would make more sense to print statistics that do not make any assumptions about the distribution of the data. These are called "non-parametric statistics."

The only non-parametric statistic in the printout is the "Median," or second quartile of the data. We (Achilles Kokkas and I) are experimenting with some non-parametric statistics. The midrange is, like the standard deviation, a measure of the spread of the data. It is equal to the third quartile minus the first quartile. A statistic similar to "C of V" above may be calculated by dividing the midrange by the median and expressing the result in percent. A statistic we call the "Symmetry Ratio" is a measure of the direction of greatest spread. When q_1, q_2, and q_3 are the first, second, and third quartiles of the data to be analyzed, the symmetry ratio is:

$$SR = (q_2 - q_1) / (q_3 - q_2)$$

The line numbers do not appear in the actual printout. They are for reference only.

The numbers on the left are not part of the analysis program. They are for reference only. The sharp character (#) introduces a comment.

Conclusion

The goals of the system design are met by hiding the tricky, tedious, difficult, and

error prone aspects from the experimenter. The test functions that require an intimate knowledge of the test hardware are the domain of the testing expert. These test functions are reusable, thereby eliminating redundant effort and allowing others to share the results of good programming practice. The price for this is paid by the expert, not the user. It is a small price because good documentation, which should be produced anyway, will reduce the number of telephone calls and visits from confused users.

The system software aids the user in many ways. Explicit read and write statements are not required in either the library or the program language, and are kept to a minimum in the analysis language. The operator follows the same procedure when running each program. The wafer prober, a fussy device, does not need to be programmed. Information used to identify the data is always collected and stored the same way. Identifying information is automatically carried from one step to the next.

The system does not guide the experimenter in the design of test chips, nor does it suggest an overall strategy. These functions would require the application of artificial intelligence research (that is, an expert system). In any case, the experimenter should have some idea of the measurements required for the experiment. This system does make it possible to use a complex tester without learning the details of its operation.

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Fred Brehm joined the Integrated Circuit Testing and Process Control group at RCA Laboratories in 1975. He worked in the areas of process control, semiconductor device simulation, international data communications, and VideoDisc and semiconductor device testing. He received the RCA Laboratories Outstanding Technical Achievement Award in 1977. Mr. Brehm is no longer with RCA.

F. McCarty

Integrated circuit engineering analysis system

We must establish a thoroughly complete method of evaluating our manufacturing processes and products, one that will enable us to make cost effective real-time corrections.

Over the last 20 years, integrated circuit technology has made enormous leaps in know-how, equipment, techniques, and results. Through advances in nearly every phase of semiconductor design and manufacture, we have come from one junction to hundreds of thousands of junctions per die; from one gate component per chip to thousands of gates contained in the same active area; from handling one device at a time to handling batches of wafers, each of which contains hundreds of large scale integrated circuits. Yet in one area, although difficult to believe, our industry is still using the technology of the fifties. That neglected area is engineering analysis. The industry started using lot card travelers to record in-process readings, operator, equipment IDs, and values of curve tracer readings for wafer accept and final test. The curve tracers have been replaced, but all else remains the same. To evaluate a low-yield wafer lot or a process change against normal production, it is first necessary to define normal production. Typically, this involves gathering all available information on lots fabricated during a time interval deemed to be normal, and then manually tabulating this generally incomplete information. From such a skimpy database, process, assembly, and test decisions are made that will financially affect that product line for years.

Abstract: *Today's semiconductor industry is experiencing a major evolution in the area of automation. Sophisticated computer aided manufacturing (CAM) systems are being introduced that are capable of handling the complex environment associated with semiconductor manufacturing. However, many systems rely on manual data entry, and depend on humans to establish a physical link between computers and very high technology processing equipment. As a result, the industry is still plagued with improper processing and invalid data related to human error, with substantial penalties in costs and time.*

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The competitive nature of the IC business demands devices that do more, are faster, and operate over wider environmental conditions—all at an increasingly lower cost. In order to satisfy this need the industry focus is now on CMOS technology. The momentum toward CMOS by the Japanese and some classical CMOS domestic vendors has increased dramatically during the past year. Over the next five years CMOS is expected to make enormous penetration in both memories and microprocessors.

In order to meet the market demands, accomplish the present long term plans, and achieve the yields required to remain cost competitive, we must establish a thoroughly complete method of evaluating our processes and products, one that will enable us to make cost effective real time corrections.

Today's semiconductor industry is experiencing a major evolution in the area of automation. Sophisticated computer aided manufacturing (CAM) systems are being introduced that are capable of handling the complex environment associated with semiconductor manufacturing. However, many systems rely on manual data entry, and depend on humans to establish a physical link between computers and very high technology processing equipment. As a result, the industry is still plagued with improper processing and invalid data related to human error, with substantial penalties in costs and time.

The RCA Solid State Division's Memory/Microprocessing facility in Palm Beach Gardens, Florida undertook the major task of defining and implementing an integrated circuit engineering analysis system. Once the system was defined, a specification was written and presented to management for review. Using the specification as a guide, a study was made to determine if the present RCA analysis software could be upgraded to support such a project, or if RCA should purchase the system from an outside vendor.

Comparison of results between RCA's Test Data Analysis System (TDAS) and outside vendor capabilities showed that Palm Beach Gardens definitely should purchase a vendor product. Many factors were considered in making the decision to purchase an engineering analysis software package from a vendor:

1. Is the software available today?
2. Is the software "user friendly?"
3. Does the software provide a common database?
4. Is the product supported by vendor representatives?
5. Will the software make use of existing software files?
6. Do training courses exist?

Various vendor software products were

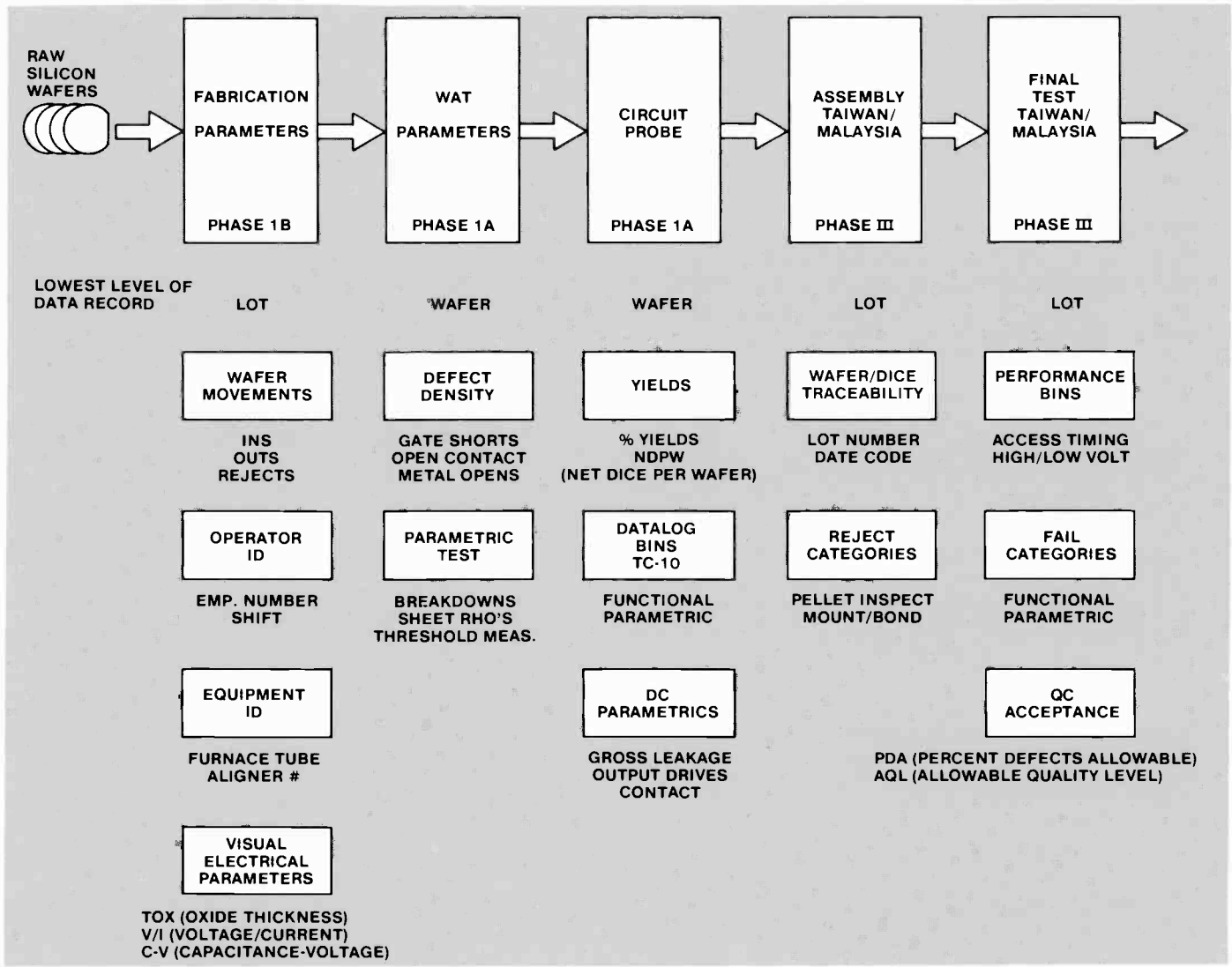


Fig. 1. *Data generation and flow through an engineering analysis system.*

evaluated before deciding on one vendor. No one vendor could meet all of the expectations defined in the specification. The decision was made to purchase Hewlett Packard's EA-10 software package due to the compatibility between EA-10 and the existing HP IC-10, which is a software package structured to store work-in-process (WIP) data for the manufacture of integrated circuits.

Figure 1 shows the flow for total wafer manufacturing data generation for an engineering analysis system. Although the flow shows five separate data generation areas, the initial implementation of the analysis system is only going to generate data from the wafer fabrication, wafer acceptance test, and wafer circuit probe areas. The assembly and final test areas will be added in the future.

Each area will generate unique data that relates to the particular function of the area.

Area	Data
Fabrication	Wafer movement
	Operator identification
	Equipment identification
	Visual/electrical
	Parametrics
Wafer acceptance test	Defect density
	Parametric test
Circuit probe	Yields
	Data log bins
	DC parametrics
Assembly	Wafer/die traceability
	Reject categories
Final test	Performance bins
	Fail categories
	Quality control acceptance

The lowest level of data recorded also will vary from one area to another. Fabrication, assembly and final test gather data at the lot level, and wafer acceptance test and circuit probe gather data from each individual wafer within a lot. The type of data collected at each area is also shown in Fig. 1, and represents only a small sample of the enormous amount of data that will be collected throughout the wafer fabrication and test procedures/steps.

In order to collect each individual type of data, different software packages were developed and tailored to pass data to a common database. Figure 2 shows the engineering analysis data collection flow in our present environment. Future plans for collecting data in the assembly and final test are not shown in the flow.

The EA-10 software package

The EA-10 (engineering analysis) system is an interactive, online system that allows all engineering groups to extract production

The engineering analysis system specification

Integrated Circuit Engineering
Analysis System Palm Beach Garden
Specification—1984

I. Purpose

To provide a user-friendly interactive computer system that is capable of monitoring, storing historical data, and evaluating and controlling key parameters that impact integrated circuit manufacturing.

II. Benefits

- Improved process control
- Reduced defect densities
- Increased product yield and quality
- Cost reduction
- Provision for long term historical data trends, graphics and plots for engineering analysis
- Accelerates the manufacturing learning curve by reducing the effective cycle time for product analysis.

III. Functions

A. Real-time data collection and historical data archive.

1. Real-time is defined as within a 24- hour period.
2. Data collection points (DCP) can be categorized into five general areas:
   - Fabrication parameters
   - WAT parameters (electrical parametric test)
   - Circuit probe (circuit functionality testing)
   - Offshore assembly
   - Final test

The quantity of data is specified in Fig. 3 at each data collection point. Phase I of the system will include circuit probe yield, bins, parameters by wafer, and fabrication parameters by WAT lot. The system must have the capability to collect assembly and test data in the future.

3. Data entries must be validated at each entry point.
4. Fabrication lot information within the past four months must be in the "ON LINE" database. The maximum number of lots in a four-month period is 1600 lots in 1984 up to 3500 lots in 1986. The maximum number of wafers in a lot is 45 at WAT and circuit probe.
5. Historical data archive must include fabrication lot information for one year.

B. Notification of equipment and process monitor alarm set points.

1. The system will notify the user on an exception basis of any process or equipment out-of-control condition through automatic report generation.
2. This feature is termed an alarm function for excepreporting.

C. Statistical correlation, graphical display, and report generation among process, equipment, and facility variables.

1. The system must make all of the data captured throughout the manufacturing process readily available to a wide user community in real-time.
2. Users must be able to proceed from question, to answer, to further questions without losing their analysis objective.
3. The system must be designed to maintain quick response time, even with many simultaneous users.
4. The system must be an interactive, on-line system that allows the process/product engineering groups in an integrated circuit environment to extract and analyze production data.
5. The system must have one integrated database that allows users to perform logical retrievals of data of any system parameter through a simple English-like query.
6. The analysis programs must include trends, scatter plots, histograms, statistical analysis and reports.
7. Reports, plots, etc. must have user-defined, alphanumeric label without the need for cross reference tables.

D. Real-time closed-loop equipment and process control.

1. The system will permit interfacing each measurement process monitor and "intelligent fabrication equipment directly to a central computer, for automatic data collection and recipe "download" at specific process steps.
2. Each link to computer will require individual customized software per semi standards (1982 secs 2) for each piece of equipment.

IV. Product Milestone

A. Phase I
   1. Circuit probe, yield, bins and WAT parameters by wafer.
   2. Fab parameters

B. Phase II
   1. Process control

C. Phase III
   1. Assembly and test

data for statistical analysis, graphic analysis, and reporting purposes. There are three basic steps to its operation :

Step 1: Transfer. Weekly/daily transfer of IC-10 WIP data and EN-10 engineering data into the EA-10 database.

Step 2: Data selection. User selection of data to be analyzed into user report file.

Step 3: Data analysis. Analysis of selected data in the user report file using EA-10 statistical analysis, graphics output, or report software. EA-10's data selection software converts a user request for data into an extract program.

Access command. This specifies the path to be used when data is collected. There are five path names in EA-10:

- Equipment
- Part
- All
- Date
- Process

Select command. This narrows the selection requests by eliminating lots that qualify according to the access statement.

Extract command. This tells the EA-10 software to file certain items and their related values if they have met the Access and Select command criteria.

Go-Now command. This compiles your selection request and extracts the requested data. Once your selection request is compiled and extracted, you can do any of three types of analysis on the extracted data:

1. Graphical
2. Statistical
3. Report writing

Graphics

When it comes to solving problems, one chart or graph can be worth a dozen reports. The following types of graphic representations are especially important to semiconductor engineers because they illustrate complex correlations and relationships in easy-to-read formats:

- Pie charts
- Line charts
- Scattergrams
- Horizontal or vertical bar charts
- Control charts

Statistical analysis

The statistical software consists of procedures for the statistical analysis of a file composed of parameters and variable names that have been selected by prior EA-10 extractions. The statistics software allows procedures in different category levels.

Elementary statistics

- Chisquare
- Frequency
- Scatter
- Correlation
- Groupsort
- Tabulate
- Elemstat
- Percentile

Advanced statistics

- Analysis of variance
- Canonical correlation
- Discriminant analysis
- Factor analysis
- Linear regression
- Polynomial
- Data smoothing

Data transformations

- Sum
- Gaussian
- Difference
- Random number
- Product
- Sine
- Divide
- Cosine
- Exponential
- Square root
- Inverse
- Power
- Log

Report writing

The report writer is called QUIZ, which is a product of COGNOS Corporation and is not sold by Hewlett Packard, but can be purchased separately. These are some of its advantages:

- It uses an easy-to-learn set of statements to produce reports in a formatted or unformatted style.
- Data can be accessed in a predetermined order.
- Data can be extracted by key value.
- Data can be sorted in ascending or descending order.
- A final summary of the report can be printed or displayed.

The EN-10 software

The EN-10 (engineering data collection) system is stored in the IC-10 database, and manually collects wafer fabrication engineering data for each wafer lot at selected operations. An example of EN-10 data collected on each lot in one of the fabrication areas is shown in Table I.

The TC-10 software

The TC-10 (tester data collection) system is structured to collect keithley wafer acceptance test (WAT) and circuit probe test results and enter the data into the EA-10 database. Future plans are to take Fairchild Sentry/Series 10 circuit probe test data and insert the data into the EA-10 database. Initially, data will be collected on magnetic tape and transferred to the database, but eventually communication links between tester host computers and the HP3000 will automatically transfer the data.

The IC-10 software

The IC-10 system monitors each lot in the fabrication area, providing management with up-to-the-minute status reports, and passes move/yield and equipment identification information to EA-10. All engineering-related data from IC-10 is automatically transferred to the EA-10 database. Operation lot tracking (OLT) is an extension of IC-10 and allows a lower level breakdown of a lot's status, providing a more detailed report for management. It also provides:

- Detailed "two-level" lot tracking.
- Increased process flexibility.
- Tracks between stations.
- Automatic on-line instructions.
- Improved operator productivity.

As can be seen in Fig. 2, the EA-10 software package is the hub of the analysis system. It contains software to generate various engineering reports, and also contains the common database to which all other software packages pass data. Each engineer uses a video display terminal to access the database. Real-time and historical data extractions can be performed with a minimum of computer knowledge. The "user friendliness" of the software system enables the engineer to concentrate on analyzing problems without spending time learning the intricate details of the software architecture. Once the requested data has been extracted from the database, the engineer has the option of using any of the three

Table I. *EN-10 data collection points.*

CMOS 2

1. P drive thickness (tox)
2. P drive resistance (Rs)
3. Active area inspect (CD)
4. P. Implant resistance (RS)
5. Depletion implant (Rs)
6. Gate oxide 2/anneal (tox)
7. Poly deposition (TSI)
8. N+ resistance on poly (Rs)
9. N+ resistance on single crystal (RS)
10. Gate critical dimension (CD)
11. Re-oxide thickness (tox)
12. P+ S/D resistance (Rs)
13. N+ S/D resistance (Rs)
14. Boron phosphorus silicon glass deposition/ density (SOITH)

CMOS 2 DLM (double-level metal)

1. P drive oxide thickness (tox)
2. P drive junction depth (tox)
3. Active area after etch insp. (CD)
4. P implant resistance (Rs)
5. Gate oxide 1 thickness (tox)
6. Gate oxide 2 thickness (tox)
7. Field oxide thickness (tox)
8. Poly silicon dep thickness (TSI)
9. Gate photo critical dimension (CD)
10. Re-oxide 1 oxide thickness (tox)
11. P+ diffusion resistance (Rs)
12. N+ diffusion resistance (Rs)
13. BPSG silicon thickness (SOITH)
14. Contact post etch insp. (CD)
15. Metal 1 deposition thickness (TM)
16. Metal 1 post etch insp. (CD)
17. CVD oxide thickness (tox)
18. VIA contact post etch insp. (CD)
19. Metal 2 deposition thickness (TM)
20. Metal 2 post etch insp. (CD)

CMOS I

1. P drive thickness (tox)
2. P drive resistance (Rs)
3. Active area insp. (CD)
4. Poly I deposition (TSI)
5. N+ poly resistance (Rs)
6. Gate critical dimension (CD)
7. P+ resistance (Rs)
8. N+ resistance (Rs)
9. Boron phosphorus silicon glass deposition/density (SOITH)

Note: CD = Critical dimension
Rs = Sheet RHO
SOITH = BPSG thickness
Tox = Oxide thickness
TSI = Silicon thickness
TM = Double-level metal

types of analysis (graphical, statistical, or report writing) or any combination of the three.

The EA-10 database receives data from a multitude of specialized software packages that collect data from different areas

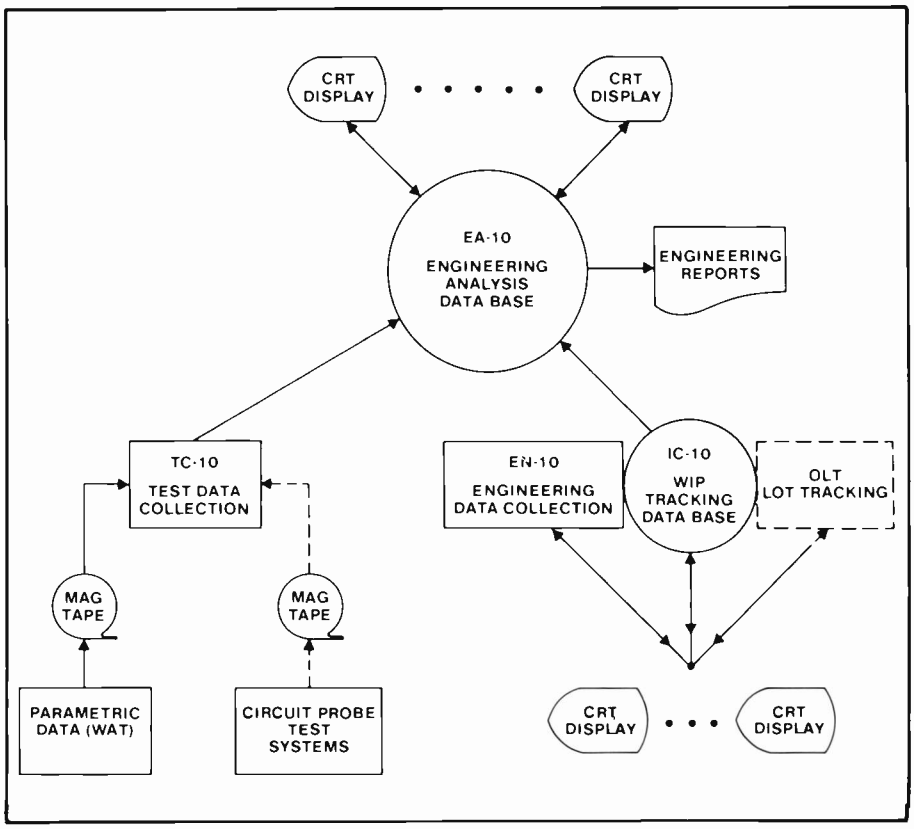


Fig. 2. *The EA-10 software is the center of the engineering analysis system.*

within the fabrication/test cycle. The IC-10 software package contains the WIP database, and all data is entered in a manual mode via video terminals throughout fabrication and test. This system also has the capability of capturing data that is not considered work-in-process, but is of an engineering nature, as shown in Table I.

At certain steps in the fabrication of a wafer, electrical tests are performed and the test results are passed on to the EA-10 database. This collection of test results is defined and supervised by EN-10. Once the data has been determined to be legitimate engineering data, it is entered into the IC-10 database. The OLT package adds more capability to IC-10. Information at lower levels can be collected to obtain a more detailed report on work-in-process, and instructions for each step within the fabrication process can be viewed on the video terminal by the operator, eliminating any confusion or questions on each task to be performed. The OLT box in Fig. 2 is shown in dotted lines because this software package has not yet been purchased and installed.

The TC-10 software package operates separately from the IC-10 database and transfers data directly to the EA-10 database. When each wafer/lot has completed the fabrication process, electrical tests must be performed on each test die, and on the circuitry of each die for which the wafer has been fabricated (circuit probe). The test dice are used to obtain parametric data that relate directly to the fabrication process. This test procedure is called WAT (wafer acceptance testing) and depending on the test results, the decision is made whether to continue testing on every die on each wafer in the circuit probe area.

The WAT parametric data is stored on the test system disc and transferred to magnetic tape on a daily basis. The magnetic tape contents are then loaded into the EA-10 database via TC-10 software, which converts the test data to the proper EA-10 format. Future plans are to connect the WAT test system directly to the EA-10 system with a communication link. The same philosophy of transferring circuit probe tests results will be used.

The method used to properly analyze data and derive concrete conclusions is to correlate the present data with valid data that has been collected over a period of time (historical data), and that resides in the same database. The engineering analysis specification for Palm Beach Gardens requires a minimum of four months of data to be present in the EA-10 database. Figure 3 shows the amount of data that will be collected in each area; you can readily see the large amount of data that may possibly be

	FABRICATION	WAT PARAMETERS		PBG TEST
	1600 LOTS / MO. PERIOD	45 WAFERS		45 WAFERS
WAFER MOVE INFO	150 DATE ENTRIES	80 DATA ENTRIES	YIELD	1 DATA ENTRY
OPERATOR ID	60 DATA ENTRIES		BINS	8 DATA ENTRIES
EQUIPMENT ID	609 DATA ENTRIES		PARAMETRICS	16 DATA ENTRIES/DICE
				X 25 DICE/WAFER
				400 DATA ENTRIES/WAFER
FABRICATION ELEC/ VISUAL	90 DATA ENTRIES	80 ENTRIES/WAF.		409 ENTRIES/WAFER
TOTAL 4 MONTH	360 ENTRIES/LOT	X 45 WAFERS/LOT		X 45 WAFERS/LOT
PERIOD	X 1600 LOTS	3600 DATA ENTRIES/LOT		18405 DATA ENTRIES
		X 1600 LOTS		X 1600 LOTS
	576,000 DATA ENTRIES	5,760,000 DATA ENTRIES		29,448,000 DATA ENTRIES

GRAND TOTAL OF DATA ENTRIES WITHIN A 4 MONTH PERIOD 35,784,000

ASSUME 10 CHARACTER/ENTRY = 357,840,000

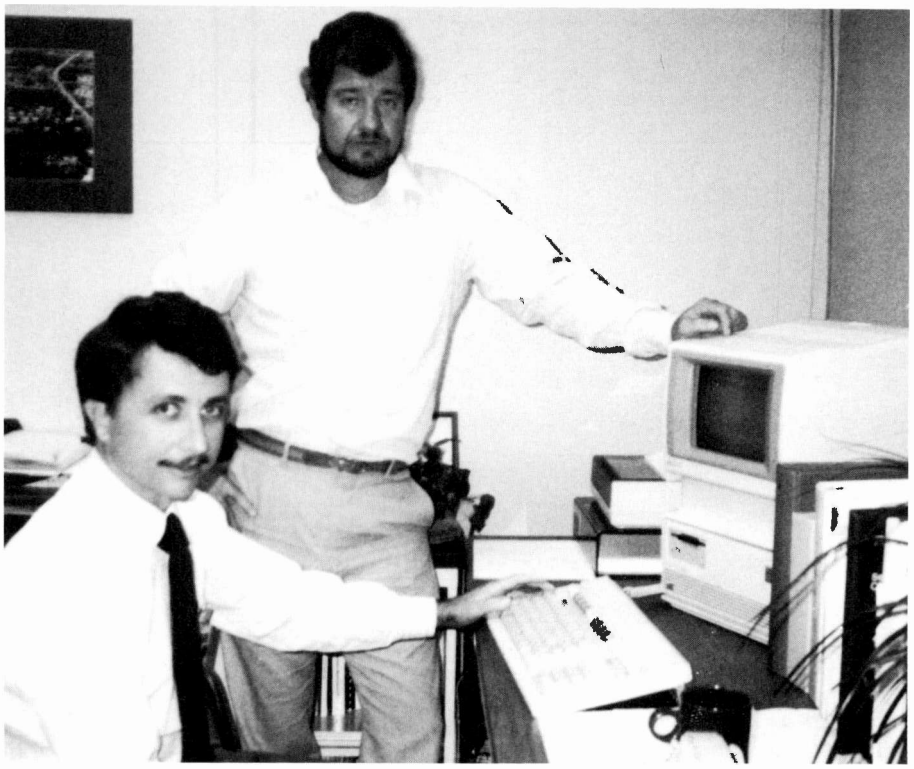
Fig. 3. *An example of the analysis data collected in each area.*

collected within a four month period. As the lot/wafers progress from fabrication to WAT to test, more and more data is collected and stored in the database. Over a period of four months, close to 36 million entries to the database may be made.

The Palm Beach Gardens EA-10 engineering analysis system is still in the early stages of collecting all the data that will directly correlate to product yield. The dynamic environment of an integrated circuit manufacturing facility requires that many independent parameters be constantly monitored and the results entered into the database. Procedures for collecting data manually by fabrication operators are very critical and must be clearly defined and error-proof before implementation, and they must be enforced by setting software flags that make entries mandatory. Normally a new procedure is implemented for approximately one month before making it mandatory; this way, everyone involved becomes accustomed to entering the new data.

George Gillespie (left) & Frank Mc Carty discussing engineering parameters that will be collected in wafer fabrication.

Although the ultimate goal is to collect engineering data from each collection point described in Fig. 3, Palm Beach Gardens has already benefited from reports derived from data extracted from the present EA-10 database, which does not receive data from all of the desired collection points. (Plans are to have all data collection points activated in 1985.) For example, a particular device type was experiencing zero-percent yield, caused by a defective ion-implant set up. The EA-10 analysis report located and isolated defective lots by date and the shift during which the implant was made, allowing for fast corrective action. In other instances EA-10 has been used to analyze "what if" situations for determining specification changes that could improve product yield. For example, data was extracted from the EA-10 database and sorted according to known process variation dates. Thirty-two combinations were reported from the extracted data, each showing a correlation of yield versus the



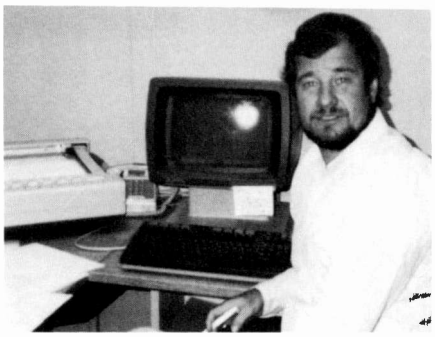
Chuck Palmer (sitting) and Frank McCarty using HP-150 PC to analyze data from the EA-10 database.

particular process variation. A simple task of selecting the best correlation report helped determine the process to follow in order to optimize yield.

This engineering analysis system is not, in the literal sense, a piece of manufacturing equipment. However, because of its potential to provide RCA with a competitive edge, it should be regarded as one. This system is as much a breakthrough in the state-of-the-art as are the new diffusion furnaces or mask aligners.

Acknowledgments

The author gratefully acknowledges the efforts of all who assisted in the preparation of this article. Special thanks must go to George Gillespie and Chuck Palmer for their advice and guidance.



Frank McCarty is a Member of the Technical staff in the Product Engineering Group. He received a BS degree in Computer Science in 1977 from Florida Atlantic University. Mr. McCarty joined the Palm Beach Gardens Computer Division in 1961 as a technician in the computer test group, advancing to Systems Analyst developing diagnostic software for the RCA Spectra computers, and as section leader of the Customer Systems Acceptance department before transferring into a special projects software group in 1971. In 1976, he joined the Solid State Division as a test engineer implementing and designing ROM and custom automotive device test programs, advancing to Section Manager of the Test Engineering Group. His present assignment is organizing a new diagnostic software group that is responsible for collecting all data within the IC manufacturing cycle that is pertinent to engineering yield analysis and storing the data in a common data base.

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W. Price

Wafer electrical testing in the factory environment

A factory environment requires high productivity at its automated test facilities. Locally customized software as well as carefully selected commercial software can provide flexibility and speed.

Wafer electrical testing (WET), often called wafer acceptance testing (WAT), is the measurement of certain wafer electrical characteristics to determine whether the completed wafer was processed correctly. These characteristics can include sheet resistances, betas, junction breakdowns, and other (usually dc) electrical parameters. Typically, these parameters are measured on five special diagnostic keys on each wafer.

In a factory environment, WET performs three important functions:

1. Quality inspection. Wafers that fail to meet acceptance limits need not be sent on to circuit probe.
2. Fast feedback to process engineers. WET quickly measures many basic process steps such as sheet resistances.
3. History of process performance. Process engineers can analyze parametric trends and relate them to process changes.
4. Checks factors that could indicate potential reliability problems.

There are many wafer parameters measured during processing, but WET measurements represent the result of all processing steps and their complex interactions.

Test system hardware

The Findlay Bipolar fab area uses a Keithley System 300 Parametric Tester to perform WET. This test system includes:

Abstract: *First, the author briefly states the purpose of wafer electrical testing, and lists the test hardware. Then, in more detail, he describes the software that increases productivity for both programmers and test equipment operators. Finally, future software enhancements are discussed that would improve engineering use of test data.*

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Reprint RE-30-2-8

- Voltage supplies: Two Kepko BOP 100-100V, 1A Two Keithley QDAC — 10V, 12mA
- Current supplies: Two Keithley 7916—100mA, 100V
- Voltage measurement: One Keithley 37615 voltmeter—50uV to 100V
- Current measurement: One Keithley 35810—2pA to 200mA
- Capacitance measurement: One Boonton Model 72B—0.1pF to 3000pF
- Frequency measurement: One HP 5345A counter (IEEE bus)—500MHz National Instruments GP1B11V-1 IEEE bus interface
- Test stations: Three Signitone Model S1007 manual probers
- Computer hardware: DEC PDP 11/23 cpu Main memory: 265 kb RAM Disk drives: Four RL02 drives—10Mb each Tape drive: One Kennedy Model 9800—800 & 1600 bpi Terminals: Two DEC VT100, Three Lear-Seigler ADM3A Line printer: One Data Products Model 600—600 lpm

Test system software

Much of the software for the System 300 has been written in Findlay to satisfy local needs. In a high volume production environment, high productivity for the WET operator is important, so the operator/computer interface has been optimized. The operator must enter data such as lot name, wafer number, key number, and start test. The computer must indicate wafer quality to the operator. To increase operator speed, the Findlay interface software minimizes the number of operator keystrokes without reducing flexibility. This is accomplished by listing the typical answer to each question asked of the operator. To accept the typical answer, the operater presses the return key. To enter something different, the operator types a different answer before pressing return. To increase system programmer productivity, a public domain software package called FLECS was acquired. FLECS has the effect of adding several structured statements to normal FORTRAN, creating a new, easy to learn structured language. FLECS programs are easier to read and debug, and take less time to write than standard FORTRAN programs.

With well over two hundred test programs written it is also important to be able to create and change test programs quickly and easily. To increase test programmer productivity, a test program generator was written in FLECS. Called "PREPRO," this generator allows programmers to reduce the number of repetitive tasks necessary to create or modify test programs. PREPRO was designed to do the following:

- Provide a flexible binning and grading system.
- Reduce programmer typographical errors by automatically generating many parameters that would otherwise have to be entered manually.
- Make test programs self-documenting so almost anyone can read them.
- Provide for fast test program generation and changes.

Here is an excerpt from a typical test program using PREPRO:

```
C TA9999 PROGRAM
& USE PROBE CARD BIMOS PROCESS 21
C-----------------------------------------------------------------
C REV 001 INITIATES PROGRAM                          12/06/82
C-----------------------------------------------------------------
C
       TO EXECUTE-CELL 1
& TEST 1
& NPN 1 5X1 5
& BETA
&      CRIT LOLIMIT HILIMIT IC(mA) VCE(V) IC-CLAMP(V) VCE-CLAMP(mA) DELAY(mS)
         T     50    1000   1       2        10          2             10
C
& TEST 2
& NPN 1 5X1 5
& BETA LOW
&      CRIT LOLIMIT HILIMIT IC(mA) VCE(V) IC-CLAMP(V) VCE-CLAMP(mA) DELAY(mS)
         F     20    1000   1       2        10          2             10
       FIN
       TO EXECUTE-CONTACTS-CELL 1
C
& TEST 900
& NPN 1 5X1 5
& CONTACT B E
&      CRIT LOLIMIT HILIMIT CURRENT(mA) VOLT-CLAMP(V) DELAY(mS)
         T     -1     14       1           20           4
C
& TEST 901
& NPN 1 5X1 5
& CONTACT B C
&      CRIT LOLIMIT HILIMIT CURRENT(mA) VOLT-CLAMP(V) DELAY(mS)
         T     -1     14       1           20           4
C
    FIN
```

Notice that the sample test program does not include probe numbers. On a previous test system (C-CAT), many of the typographical errors involved probe numbers. To reduce probe number typos, a "probe card definition file" is used. A probe card definition file consists of a list of device names for each fixed point probe card. The advantage is that probe numbers are typed only once for each probe card. Many test programs can use one probe card definition. The sample test program invokes the "BIMOS" probe card definition file with the statement "& USE PROBE CARD BIMOS." Here is a sample probe card definition file:

```
! BIMOS PROBE CARD
!
NPN 1.5X1.5:        E=12 B=11 C=4
VRT :               E=22 B=3  C=17
RES B&R 1.0 MIL:    R+=32 R-=7
RES B&R 0.4 MIL:    R+=31 R-=7
CAP EPI:            C+=14 C-=5


PMOS :              D=1 G=10 S=8
```

Another common typographical error in test programs was incorrect polarities. PREPRO8 automatically supplies the proper polarity by recognizing that the first part of the device name (NPN, LAT, VRT, PMOS, NMOS, etc.) indicates the polarity to be used.

Binning and grading

"Bins" and "grades" appear on the operator's screen to indicate the general result of the parametric tests being performed. A "bin" is a number that characterizes the quality of a specific diagnostic key on a wafer. For example, a "BIN 1" may mean that the key passed certain tests. Normally, default binning is used, where a "BIN 1" means the key passed all critical tests. The critical tests are indicated in the body of the program by the letter "T" under the word "CRIT," (meaning "True," this test is CRITical). The non-critical tests are indicated by an "F" (for False). A "grade" is a number, word, or phrase that characterizes the quality of the wafer as a whole. For example, a wafer that has a certain minimum number of BIN 1s can be defined as a grade of "GOOD," an "F1," or even a special instruction to the operator like "GIVE TO BILL PRICE." Default grading requires two BIN 1s for a wafer to have the grade F1 (meaning "Findlay #1," or good). This default can be overridden and special binning and grading can be explicitly stated by appending binning and grading statements to a test program. For example:

```
& BIN 1  ( 1 D 1 1 )
& BIN 2  ( 2 D 1 1 )
& GRADE F1 ( 1 1 D D D )
& GRADE F2 ( 1 T T T T )
& GRADE HOLD FOR B. PRICE ( 2 T T T T )
& GRADE FS ( T T T T T )
```

Based on C-CAT bin tables, binning is accomplished as follows:

1. The test results of one diagnostic key are compared to their respective limits. Each character inside the parenthesis of a bin statement corresponds to a parametric test.
2. For one key to match a particular bin, individual test results (such as BETA) must be equal to or less than the limit number indicated in the bin table.
3. "D" indicates "don't care"; it matches anything and indicates that the test is not "critical"—it is for information only, and not to be used as pass/fail criteria.
4. "F" indicates "fail."
5. "R" is an "OR fail" indicator. For example, BIN 2 (R R R) would indicate that to match a bin 2, test number 1, 2, or 3 must fail.

Example

```
C-----------------------------------------------------------------



& TEST 1
& NPN 1 5X1.5
& BETA
&      CRIT LOLIMIT HILIMIT IC(mA) VCE(V) IC-CLAMP(V) VCE-CLAMP(mA) DELAY(mS)
         T     50    1000   1       2        10          2             10
& LIMIT 2   LOLIMIT HILIMIT
              120     1080
C-----------------------------------------------------------------



& BIN 1  ( 1 D F F )
& BIN 2  ( 2 D F F )
```

To match "BIN 1" above, test 1 (NPN BETA) must pass the first set of limits (50, 1000), any result of test 2 (not shown)

will match the "D" (don't care) bin condition, and the third and fourth tests (not shown) must fall outside their respective limits to match the "Fs". To match "BIN 2," test 2 must match the first or second set of limits (50, 1000 or 120, 1080).

Grading enables the test program to tell the operator whether the wafer is scrap, good, or any other message desired. There are as many characters in the parenthesis as there are diagnostic keys on a wafer (usually five). The characters are checked to see if they match the bin results for the wafer being tested.

Grading example:
& GRADE GOOD (1 1 D D D)
& GRADE HOLD FOR B PRICE (1 T T T T)
& GRADE SCRAP (T T T T T)

As soon as any two keys on a wafer are "BIN 1," the message "WAFER #n = GOOD" is displayed, and that wafer need not be tested further ("D" is "don't care"). This tells the operator to go to the next wafer.

If a key has been tested, it matches one "T". If all keys have been tested and one key was a "BIN 1," the message "WAFER #n=HOLD FOR B PRICE" is displayed. If all five keys have been tested and the first two grades have not been matched, the message "WAFER #n = SCRAP" is displayed.

Data archive

The computer also must generate printed reports for test, process, and type engineers. Since many different engineers use them, the reports are largely self-documenting. All reports include device names, conditions, and limits, so one does not need to see the test program to interpret a report.

A tape archive system is used to keep wafer data for up to nine months (or longer with the purchase of more tapes). This tape archive system is useful for type engineers because they may be asked to investigate a wafer's parametric data after the wafers are shipped to Taiwan, packaged, and have been through final testing. Also, all test program revisions are archived.

Future enhancements

Currently, there are two types of real-time parametric test reports used: datalogs and histograms (histograms and 100-day trend plots are also available in a batch mode from the Somerville IBM 370). There have been requests for many other types of report printouts.

We are currently investigating ways that commercially available software can improve the presentation of WET data. Ideally, all reports should be displayed on a CRT screen and optionally printed. Also, reports should be in a form that can be edited to add additional notes or to do text searches. There should be a capability for *ad hoc* reports whose format is created by non-programmer engineers using a simple menu-driven system. An *ad hoc* report format could be saved for future use if desired. Typical reports would include tables, graphs, statistical functions, X-BAR-R charts, histograms, and trend plots. Besides different formats, a query language or menu is needed. A process engineer should be able to sit at a terminal and get answers for questions like, "What is the trend of B&R resistance for all BIMOS types over the past month?", "What types had any scrap today and what were the major failing parameters?", "What is the correlation between lateral VCEO and circuit probe yield for type X?", or "What is the variation of npn beta across the wafer for lot number 98099?". The computer might not be expected to interpret the questions as stated above, but an English-like query language or menu system would be useful. And perhaps the system could even anticipate problems and automatically generate an "alarm report" if an X-BAR-R analysis indicated that a parameter was drifting for a specific type.

For wafer electrical testing in a factory environment, increased productivity through additional "computer aided yield enhancement analysis" is an important next step.

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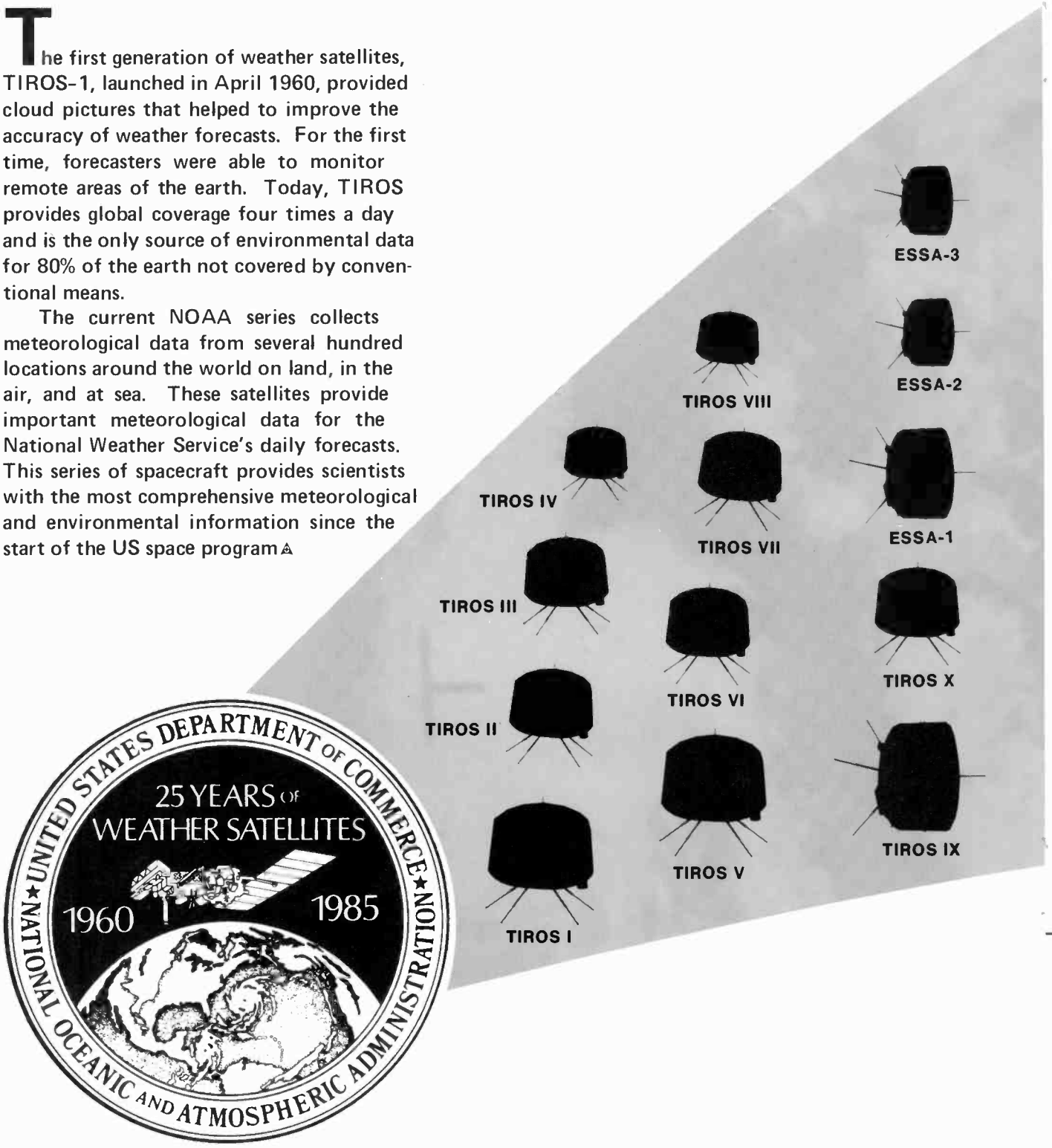
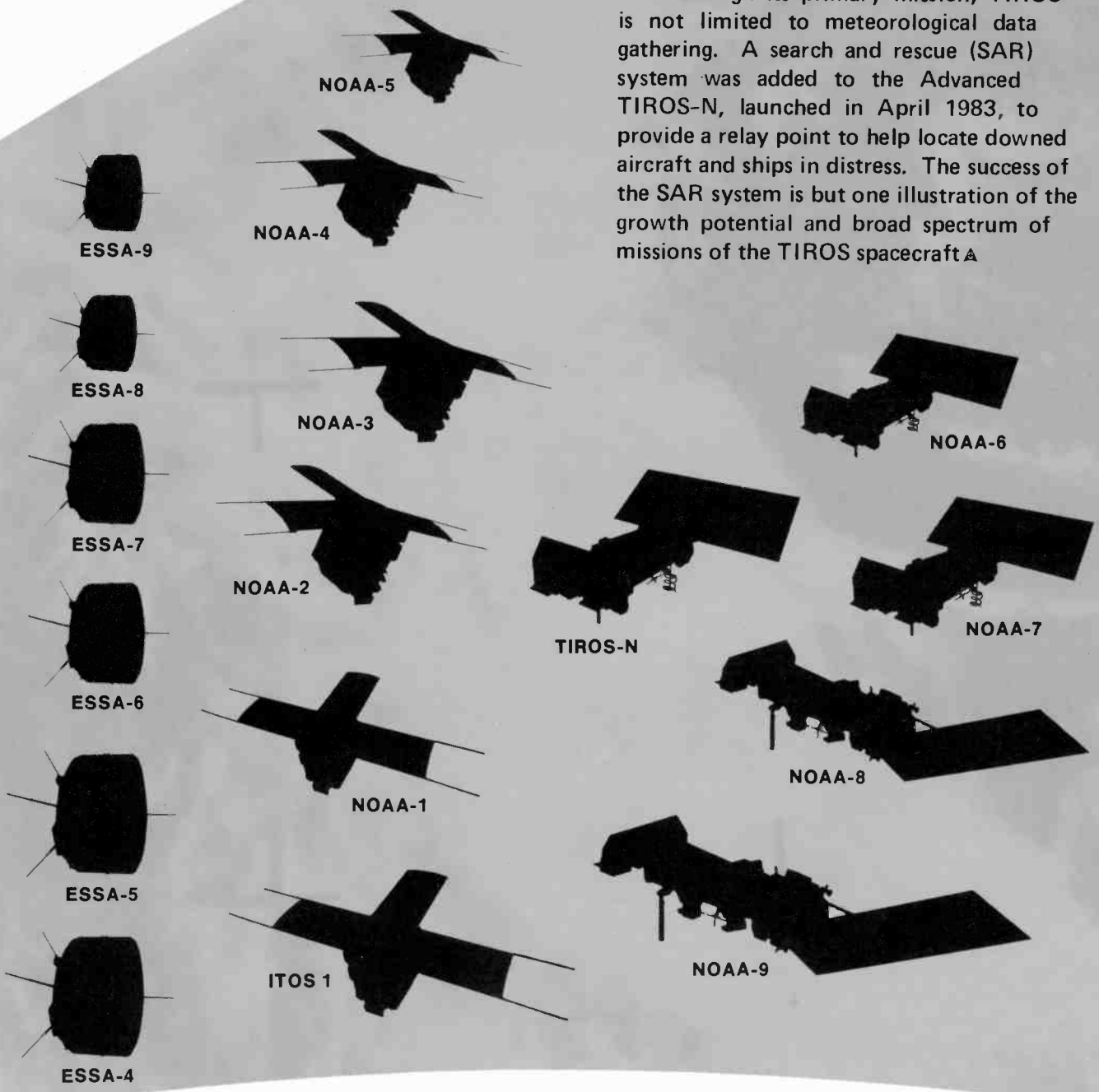
RCA Astro-Electronics Celebrates 25 Years of Weather Satellites

The first generation of weather satellites, TIROS-1, launched in April 1960, provided cloud pictures that helped to improve the accuracy of weather forecasts. For the first time, forecasters were able to monitor remote areas of the earth. Today, TIROS provides global coverage four times a day and is the only source of environmental data for 80% of the earth not covered by conventional means.

The current NOAA series collects meteorological data from several hundred locations around the world on land, in the air, and at sea. These satellites provide important meteorological data for the National Weather Service's daily forecasts. This series of spacecraft provides scientists with the most comprehensive meteorological and environmental information since the start of the US space program.





Although its primary mission, TIROS is not limited to meteorological data gathering. A search and rescue (SAR) system was added to the Advanced TIROS-N, launched in April 1983, to provide a relay point to help locate downed aircraft and ships in distress. The success of the SAR system is but one illustration of the growth potential and broad spectrum of missions of the TIROS spacecraft.

RCA

Astro-Electronics

Patents

Astro-Electronics

Callen, P. J.
Satellite dual bus power system—4494063

Broadcast Systems Division

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Television signal standards conversion using a helical scan VTR—4500930

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Duvall, W. E./Hwang, M. P.
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Signal sampling network with reduced offset error—4502079

Hermeling, Jr., G. C./Muterspaugh, M. W.
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Single controllable switch, push-pull inverter for a television receiver ferroresonant power supply—4492900

Maimpally, S. V./Tallant, 2nd, J. C.
Wideband kinescope driver amplifier—4494146

Government Communications Systems

Coyle, P. J.
Protective cartridge for disc record—4499996

Government Systems Division

Siryj, B. W./Lazzery, A.G.
Automatic handling mechanism for an optical disc enclosed in a protective cartridge—4502133

Missile and Surface Radar

Forquer, T. J./Li, H.
Multiprocessor-memory data transfer network—4491915

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Schwarzmann, A.
Folded dipole radiating element—4498085

RCA Laboratories

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Aschwanden, F.
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Bolger, T. V.
FIR chrominance bandpass sampled data filter with internal decimation—4500912

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Apparatus for frame-to-frame comb filtering composite TV signal—4498100

Cartwright, Jr., J. M.
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Dischert, W. A.
Video disc player having carriage drive mechanism—4493070

Faraone, L.
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Hammer, J. M./Neil, C. C.
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Noise suppressing Interface circuit in a kinescope bias control system—4502073

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Solid State Division

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Coincident pulse cancelling circuit—4502014

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Gentile, C. J./Hagge, M. L./Croes, R. C.
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Pen and Podium

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V. J. Benokraitis
A one-on-one hit avoidance model—*Modeling and Simulation*, Vol. 15, Part 2, pp. 727-733 (1/85)

G. Claffie
High performance optical disk jukebox-Presented at the SPIE Third International Conference on Optical Mass Data Storage, Los Angeles, Ca. (11/85)

G. Claffie
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H. W. Kaiser
RCA CMOS/SOS rad hard technology status—Presented at SDI Space Radar Discrimination Conference, Boston, Mass. (12/84)

R. Putatunda
Autodelay: A second generation automatic delay calculation program for LSI/VLSI chips-Presented at the International Conference on CAD, Santa Clara, Ca., and published in the *Proceedings* (11/84)

R. H. Schellack
The GaAs quick chip: A high-speed cell array for both analog and digital applications—*EDN*, Issue 23 (11/11/84)

D. C. Smith/R. Noto/J. C. Werbickas/G. Powell/S. Sharma
GVAUA and ATLAUA: A total gate array design capability—Presented at GOMAC 84, Las Vegas, Nevada, and also at the ICCAD Conference, Santa Clara, Ca., and published in the *Proceedings* (11/84)

L. E. Toombs/W. B. Schaming
Multifeature methods for target detection—*RCA Engineer*, Vol. 29, No. 6, pp. 56-60 (Nov/Dec 1984)

J. R. Tower/B. M. McCarthy/R. T. Strong/L. F. Pellon
Development of multispectral detector technology—*RCA Engineer*, Vol. 29, No. 6, pp. 48-55 (Nov/Dec 1984)

J. S. Zapriala/J. A. Gaev/N. Straguzzi
AI applications in future military systems—Presented at GOMAC 84, Las Vegas, Nev., and published in the *Proceedings* (11/84)

Astro-Electronics

D. Chu/G. Clark
Structural dynamic modification using modal analysis data—Presented at the 3rd International Modal Analysis Conference, Orlando, Fl. (1/85)

D. Chu/C. Trundle
Reanalysis techniques used to improve local uncertainties in modal analysis—Presented

at the 3rd International Modal Analysis Conference, Orlando, Fl. (1/85)

C. Hubert
Computer-aided stability analysis of spinning spacecraft with moving parts—Presented at the Rutgers Mechanical & Aerospace Engineering Colloquium, New Brunswick, N.J. (2/85)

J. C. Logrando
Evaluation of high voltage multilayer ceramic capacitors for spacecraft power supplies—Presented at the 1985 High Voltage Workshop, Monterey, Ca.(2/85)

L. O'Hara/A. Rosenberg/J. Sroga
Ground based 0.53 μm wind sensor—Presented at the Topical Meeting on Optical Remote Sensing of the Atmosphere, Incline Village, Nev. (1/85)

K. W. Schmidt
Bridging the generation gap: The sigma-3 computer upgrade program—Presented at the TeleXchange 6th International Meeting, Newport Beach, Ca. (1/85)

D. Solomon
Covariance matrix for a-b-y filtering—*IEE Transactions on Aerospace and Electronic Systems* (1/85)

Automated Systems

L. Arlan/E. H. Miller
Interactive color graphics support to intelligence analysis—Presented at the Verdugo Chapter, Association of Old Crows, Canoga Park, Ca. (2/85)

L. R. Armstrong/P. Berrett/E. G. Zablocki
Diesel engine power prognostics—Presented at the SAE International Congress and Exposition, Detroit, Mich. (2/85)

R. E. Hartwell
Artificial intelligence applied to diagnostics—Presented at the SAE International Congress and Exposition, Detroit, Mich. (2/85)

Government Communications Systems

H. R. Barton, Jr.
Predicting guaranty support using learning curves—Presented at the Reliability and Maintainability Symposium, Philadelphia, Pa. and published in the *Proceedings* (1/85)

RCA Laboratories

W. A. Bösenberg/C. W. Magee/E. M. Botnick
Chlorine content in dry and wet MOS gate oxides—*J. of the Electrochem. Soc.* 131, 2397 (1984)

J. B. Clegg/A. E. Morgan/H. A. M. DeGrafte F. Simondet/A. Huber/G. Blackmore/M. G. Dowsett/D. E. Sykes/C. W. Magee/V. R. Deline
A comparative study of SIMS depth profiling of boron in silicon—*Surface Interface Analysis*, 6, 162 (1984)

F. J. Feigl/R. Gale/H. Chew/C. W. Magee/D. R. Young
Current-induced hydrogen migration and interface trap generation in aluminum-silicon dioxide-silicon capacitors—*Nucl. Instum. Meth. Phys. Res.* B1, 348 (1984)

C. W. Magee
On the use of secondary ion mass spectrometry in semiconductor device materials and process development—*Ultramicroscopy* 14, 55 (1984)

C. W. Magee/E. M. Botnick
The use of secondary ion mass spectrometry in semiconductor device materials and process development—*RCA Engineer*, Vol. 29, No. 5 (Sept/Oct 1984)

C. W. Magee
Secondary ion mass spectrometer design considerations for inorganic and organic analyses—3M/NSF Sponsored Symposium in SIMS and FAB, St. Paul, Minn. (10/84)

C. W. Magee
Analysis of amorphous silicon photovoltaic material by secondary ion mass spectrometry—Invited presentation in a Symposium on Analysis of Ultrapure Materials, Eastern Analytical Symposium, New York City, N.Y. (11/84)

C. W. Magee
Materials characterization using ion beams-Invited seminar at Kodak Research Laboratory Rochester, N.Y. (11/84)

L. K. White
Approximating spun-on, thin film planarization properties on complex topography-*Journal of Electrochemical Society*, 132 (1), 168 (1985)

Missile and Surface Radar

W. A. Mulle
A distributed microcomputer architecture of tactical systems—Presented at the Electronics for National Security Asia Conference, Singapore (1/85)

Service Company

R. C. Bryant
Closed circuit television in security—Presented at the Philadelphia Chapter of the American Society for Industrial Security Seminar (3/85)

R. L. Layton
Office communications; requirements and solutions—Presented at the UNIX Users Conference, Dallas, Tex. (2/85)

Engineering News and Highlights

Hearn named CEE Administrator

Tony Hearn joined the RCA Corporate Engineering Education group (CEE) in January 1985 as Administrator, Engineering Education programs. For the past three years he has taught full time in the areas of digital electronics, microprocessors, industrial process technology, and finance at Lyons Technical Institute, Philadelphia Community College, and La Salle University. He has 15 years of circuit and system design experience in color television, government satellite systems, and commercial computer systems. Mr. Hearn received BSEE and MSEE degrees from Drexel University, and holds an MBA with a major in Finance from La Salle University.

Engineering Corporate Computer Center opens

The Engineering Corporate Computer Center (ECCC) became operational on January 31, 1985. The facility is owned and operated by Corporate Information Systems and Services (CISS), but is managed in conjunction with the participating business units.

The primary purpose of this new center is to provide support in shortening the overall design cycle for engineering. With user-supported software, designers will be able to take advantage of the 10-to-1 reduction in throughput time over their local minicomputers. The ECCC will be the repository for code used in electrical, thermal, and mechanical designs. Other applications will be added as necessary.

The ECCC is designed to be an additional computing resource for the participating RCA business units. Specifically, it comprises an IBM 3083J unit, which runs the IBM VM operating system in a batch mode. To gain access to the system, users will submit jobs either through their local VAX terminals or through the VM system at Cherry Hill. Using an Interlink 3711, the VAX-submitted jobs will be first translated to an acceptable IBM format and then processed on the IBM mainframe.

Initially, the business units participating in the ECCC are Astro-Electronics, Missile and Surface Radar, Advanced Technology Laboratories, Automated Systems Division, Government Communications Systems, Solid State Technology Center, Government Systems Division staff, and RCA Laboratories. Engineers and programmers at any of these units are urged to contact their business unit ECCC representative if they require additional information, or call **Tacnet 253-6638** for the name of their local representative.

The ECCC is currently supported by two groups: the Management Committee, and the Major Operating Unit User Committee. The first group comprises one member selected from each participating ECCC unit. Committee members have a direct vote in resolving major issues and deciding the future directions of the ECCC facility. Overall, however, the Management Committee is responsible for establishing policies regarding software acquisitions, hardware changes, and operating strategies.

The second group—the Major Operating Unit User Committee—has during the past year evolved into a gathering of individuals representing ECCC participants at the user level. Most of these committee members are MOU ECCC contacts, and they meet at least once every three weeks to discuss additions or changes to the communications configuration, new software installations, standards, and usage problems.

As the need for additional computing resources is discovered, the ECCC system will be re-evaluated.

Ed. Note: There will be an article in the July/August issue of *RCA Engineer* describing the evolution of the ECCC and how the facility functions.

Professional activities

Schmidt named Associate Fellow of AIAA

Charles A. Schmidt, Division Vice President and General Manager of Astro-Electronics, has been elected an Associate Fellow of the American Institute of Aeronautics and Astronautics (AIAA). Mr. Schmidt has been with RCA for 34 years.

Two at VCDD receive degrees

Raymond E. Keller, a senior technician in the Product Development group at VCDD, Scranton, recently received a Bachelor of Professional Studies degree with a major in Mechanical Engineering from Elizabethtown College, Elizabethtown, Pa.

Nicholas J. Spryn, a drafter/designer in Equipment Engineering at the Scranton plant, received a Bachelor of Professional Studies degree with a major in Electrical Engineering from Elizabethtown College.

(*More* →)

Obituary

Meade Brunet

Meade Brunet, former Vice President and Managing Director of the RCA International Division, died on February 10 at the age of 90. Mr. Brunet retired from RCA in 1966 after 44 years of service. He joined RCA in 1922, and was assigned to the sales department. From 1923 to 1925 he was RCA District Manager in Chicago, Ill. Subsequent promotions led to his appointment as Manager of the Engineering Products Department, and he later became Vice President of the RCA Manufacturing Company.

From 1939 to 1946, in addition to his other duties, Mr. Brunet was in charge of the Washington Sales Office, and was subsequently elected a Vice President of RCA. In 1946 he became Vice President and Managing Director, RCA International Division, and in 1957 he was made Staff Vice President in the Sales and Services organization of RCA. During 1960, he was assigned abroad for the electronic development program in southern Italy.

Yost is IEEE Centennial Young Engineer

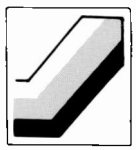
Left to right: Dr, Richard J. Gowen, 1984 IEEE President; Thomas D. Yost; Dr. Stephen Kahne, IEEE 1985 Vice President, Technical Activities.

Thomas D. Yost, Manager, Audio Circuit Design, Consumer Electronics (Indianapolis) has been named a Centennial Young Engineer by the Institute of Electrical and Electronics Engineers (IEEE). Cited by the IEEE Consumer Electronics Society, Mr. Yost received a "Centennial Key to the Future" from IEEE President Richard J. Gowen.

The "Keys to the Future" were presented to 34 individuals representing the Institute's 33 technical societies. Each recipient was identified as an individual in the early stages of his or her career "who best demonstrates sound understanding of the evolving technologies" in the individual's chosen field, and whose "progress shows the greatest promise for applying these technologies toward the development of new industrial products and systems for the improvement of society."

The keys were laser-cut from a three-inch silicon disk composed of metal oxide semiconductor material.

Technical excellence



Two new TECs formed

The Video Component and Display Division at Circleville, Ohio and RCA Service Company at Springfield, Virginia recently formed their own Technical Excellence Committees.

Springfield is a Government Services location of RCA Service Company. Organizational planning for its new TEC was conducted for about six months prior to installation. The charter was developed and approved, and the first set of committee members was selected. The first meeting was held on October 10, 1984.

The VCDD TEC at Circleville was formed on November 7, 1984. It has seven voting members and two advisory members representing management and Employee Relations.

Kearney wins Astro EEC Award

Chris Kearney has been presented with the Engineering Excellence Award for his innovative and expeditious design of the Attitude Logic Processor (ALP) firmware for the RCA Satcom H satellite. Analysis of on-orbit telemetry from Satcom G in late May 1983 indicated the possibility of realizing a significant improvement in the performance of the attitude control system. As a result, new attitude requirements were imposed on the Satcom H Attitude Logic Processor firmware.

Mr. Kearney assisted in the analysis of the Satcom G telemetry and provided important help in the selection of the improved design for Satcom H, and was the lead engineer in the production of the revised ALP package. Within rigid and demanding scheduling constraints, he designed and delivered the code. His insight and diligent effort were instrumental in the testing, modification, and final certification of the ALP firmware. As a result of this extraordinary effort, Satcom H was launched on schedule and has been meeting or exceeding all mission attitude requirements since launch.

Astro Engineering Excellence Team Award

Lawrence Slivinski, James Sturges, and **Jialing Yang** have won the Astro-Electronics Engineering Excellence Team Award for their analytical contributions in support of the DMSP S-9 spacecraft modal test and loads verification program. They were responsible for developing and adjusting the finite element model of the spacecraft, for pre-test analytical support for the structure test group, and for real-time analysis of the modal test data during the course of the test. To accomplish these tasks, new software programs were developed that were essential to the successful completion of the test and the final verification launch loads analysis. New software, implementing advanced structural dynamics mode synthesis techniques, was developed in order to analytically remove the effects of a solar array mass simulator, while adding the effects of the analytical solar array finite element model to the experimental spacecraft modal model.

Division-wide SSD award to Parker

Ken Parker, a member of Findlay's Equipment Technology Group, has been named as the recipient of this year's Solid State Division Technical Excellence Award. He was selected from a field of all Technical Excellence Award winners in SSD. The Division Award consists of an engraved bowl and a cash award.

Marion Technical Excellence Award

Jerry Hotmire, Quality Control Engineer at VCDD Marion, has been awarded the fourth quarter Technical Excellence Award. He was

selected for developing, establishing, making operational, and updating the HP-1000 Process Quality Computer System. This system has enabled engineering to maintain tight control of matrix opening sizes.

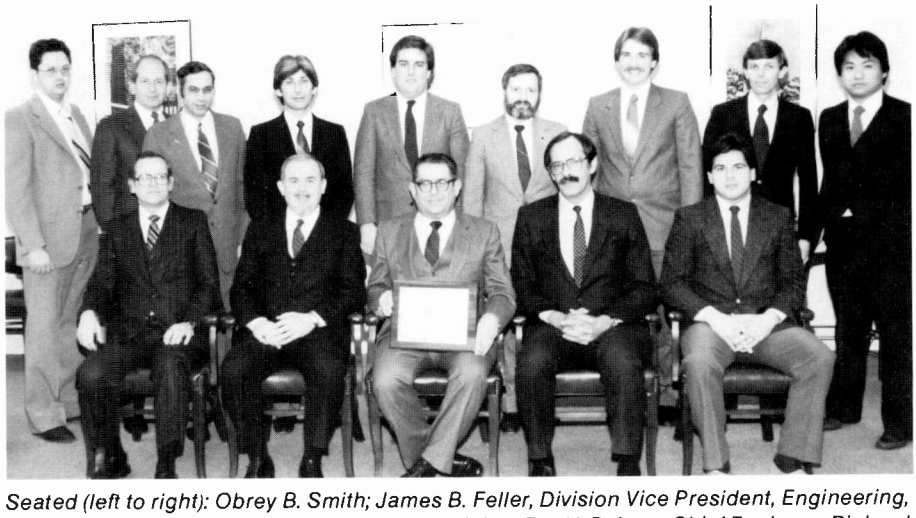
Mehling wins MSR annual award

Thomas H. Mehling has won the MSR Annual Technical Excellence Award for 1984. He was honored for outstanding contributions to AEGIS Combat System readiness and operational excellence. His services were specifically requested during March and April 1984 to assist in preparations for a special post-deployment operational test designed to challenge *USS Ticonderoga's* air defense capabilities. His ability to diagnose subtle and unusual problems and provide instantaneous solutions was a major factor in the extraordinary performance levels achieved.

During this period he operated virtually alone, relying on his ability and background to correct deficiencies. On a number of occasions he made computer program changes in a matter of hours that others estimated in terms of man-months. His habit of verifying his work by exhaustive testing contributes significantly to the immediate customer acceptance of his solutions to problems.

As the winner of the annual award, Tom will receive a special plaque honoring his accomplishments, a text or reference of his choice, and an extended weekend vacation.

Left to right: Fred I. Palmer, Chief Engineer; Thomas H. Mehling; James B. Feller, Division Vice President, Engineering, Government Systems Division.



Seated (left to right): Obrey B. Smith; James B. Feller, Division Vice President, Engineering, Government Systems Division; Thomas H. Mehling; Fred I. Palmer, Chief Engineer; Richard Rabbitz. Standing (left to right): Seth R. Putney, Ralph L. Stegall, Frank J. Reifler, Daniel L. Friedman, Michael S. Perry, Leonard H. Yorinks, Joseph P. Pryzbylkowski, William J. Graham, Stanley M. Yuen. Absent: Pradeep K. Agrawal, Daniel J. Wawrzyniak.

MSR third quarter awards

There were five winners of the 1984 third quarter Technical Excellence Awards in MSR, Moorestown, N.J.:

Pradeep K. Agrawal, for conceiving a special technique to overcome the need for extreme position precision in near-field antenna testing. The approach uses a laser system to determine probe displacement from a perfect measurement grid to provide the basis for phase adjustments. Dr. Agrawal's "k-vector" method simplifies computation of scanner positioning error compensation, thereby relaxing mechanical requirements for the extremely accurate ANFAST II measurement system.

Daniel L. Friedman, for his innovative solution to a potentially serious problem in a class of vertically launched SM-2/Block II missiles. The obvious solution, requiring missile design changes and significant computer program changes, would have involved extensive, costly delays. Mr. Friedman's alternative solution involved a simple parameter change in the computer program to avoid the conditions under which the problem could occur, providing efficient and timely resolution of the problem.

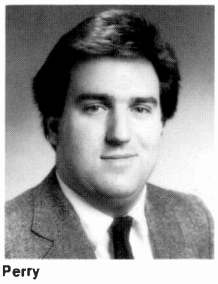
Seth R. Putney, for his systems engineering role in the design and development of the FAA's Request for Proposal for the Air Traffic Control Host Computer System. Mr. Putney's technical guidance provided a systematic and consistent approach to technical input and documentation. His efforts have contributed significantly to the FAA's Advanced Automation Project and to RCA's technical reputation.

Ralph L. Stegall, for exceptional technical accomplishment in successfully interpreting customer requirements and defining a system for the Multiple Object Tracking Radar. As lead systems engineer for the program, he defined the radar architecture, including the array and software subsystems. As the principal technical interface with the customer, he was responsible for selling the MSR concepts. The result is a new MSR product line with significant long-term business potential.

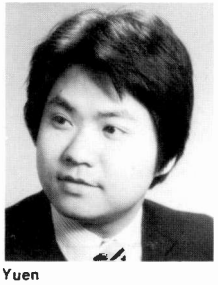
Leonard H. Yorinks, for special contributions to the achievement of ANFAST II operational capability. Dr. Yorinks developed calibration and alignment techniques for the rf receiver as well as test procedures to validate the calibration. He devised a series of experiments that resolved discrepancies between reported and anticipated data, and specified corrective action. His contributions to the identification and resolution of beam-pointing computer program deficiencies were especially valuable.

Fourth quarter MSR awards


Graham


Perry


Smith


Yuen

There were four winners of the fourth quarter MSR Technical Excellence Awards:

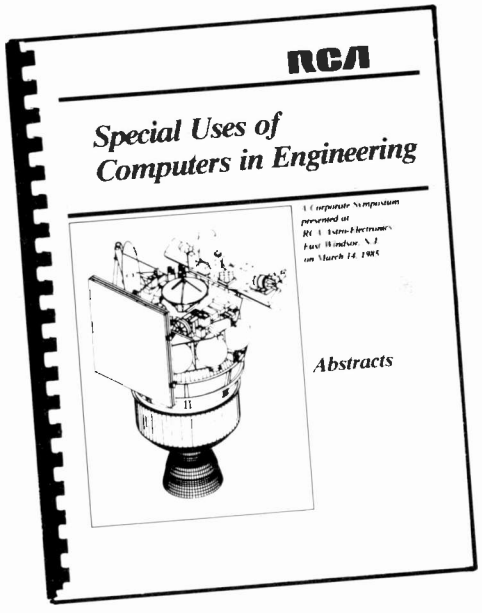
William J. Graham, for outstanding contributions to the Multiple Object Tracking Radar (MOTR) antenna design. When it became apparent that his original reflectarray design would not support all the MOTR marketing targets, Dr. Graham quickly shifted to a transmission lens array design. The computer-aided design tools he developed allowed him to rapidly perform the required tradeoffs and achieve an optimized design that meets all MOTR requirements.

Michael S. Perry, for successfully developing a new design for a 7-bit precision ferrite phase shifter for the Modular Advanced Tactical Radar. In addition to his development effort, he coordinated a pilot production run, set up a production test program, and conducted high-power tests at a vendor plant. The result is a production-ready design for a precision C-band phase shifter suitable for low-sidelobe phased arrays.

Obrey B. Smith, for his leadership and personal performance in the design, development, and test and evaluation of the New Zealand R76C5 fire control system. In addition to leading the hardware development team, he also contributed significantly to the successful factory acceptance tests of the first system. His technical direction and personal design contributions were a key element in the successful completion of the R76C5 development program.

Stanley M. Yuen, for developing a new technique of highly accurate, unambiguous, doppler discrimination of low cross-section targets using minimal radar dwell time. His spectral estimation algorithm—compatible with AEGIS system requirements—affords the rapid threat detection necessary for protection against close-in missile threats. Mr. Yuen's solution to this previously unresolved problem was successfully demonstrated by computer simulation using realistic air defense system parameters.

Astro-Electronics hosts computer symposium



On March 14, 1985 an RCA corporate symposium on "Special Uses of Computers in Engineering" was held at Astro-Electronics, Hightstown, N.J. The co-chairmen were **James P. Layton** and **Lawrence C. Scholz.** There were 90 attendees representing 14 RCA business units: Astro-Electronics, Corporate Staff, Automated Systems, Government Systems Division, RCA Service Company, RCA Records, Government Communications Division, Americom, RCA Laboratories, the Frequency Bureau, Missile and Surface Radar, Solid State Division, Consumer Electronics Division, and Corporate Engineering Education.

Robert Miller, Chief Engineer, Astro-Electronics was the first of ten speakers, and at the end of the day he felt that the symposium "provided a very worthwhile interchange between our groups at RCA who are using computers to improve engineering productivity. I think we should encourage frequent interchanges among our working level people on this subject. I heard one of the participants say that 'fifteen minutes of this meeting has saved me three weeks of work in developing a software package.' "

The day's activities included a tour of Astro-Electronics and a microcomputer demonstration.

Papers presented:

Use of computers in space engineering

R. Miller

In order to maintain its competitive position, Astro has been a leader in using computers in space and on the ground to achieve engineering productivity improvement. This spans the areas of design, test, in-orbit control, and operations.

Benefits of computer aided spacecraft design

Nelson F. Samhammer

Computer aided design and drafting (CADD), which has been available at a lower level of capability for years, has become available at a level of sophistication and cost effectiveness useful in the area of mechanical design. Early in 1984, we began our search for such a system to satisfy our needs. Ultimately, our selection process led us to the system that has been in operation at Astro since January 1983: PRIME MEDUSA.

Times, Terminal Interactive Menu Executive System

Jerry Golub

Menu input, which is popular for many transaction systems, is an attractive alternative to the current methods of input preparation for scientific and engineering programs. TIMES, a program to develop a menu input capability, has been written and successfully applied to two graphics programs and a Naval Battle Group simulation.

On-board spacecraft computers

Steven Teitelbaum

The space environment places constraints on computer design such as low power consumption, low weight, high reliability, and small production quantities. These constraints have a dramatic effect on the physical and

performance characteristics of present day spacecraft machines.

Computer aided microwave engineering

Dr. Barry S. Perlman

Computer-aided engineering (CAE) has permitted the microwave engineer to gain more functionality and benefit with increased productivity. For the microwave engineer, CAE includes computer-aided design (CAD) of circuits and devices, performance simulation, analysis and optimization, CAD for physical layout, prototype evaluation, and automated testing.

Intelligent man-machine interface for satellite control

R. H. Harten

The volume and complexity of telemetry information make it increasingly difficult for operators to notice and respond to abnormal spacecraft conditions. Current systems typically use a series of telemetry limit checks and alarms to monitor and signal abnormal conditions. Astro's Intelligent Man-Machine Interface project was initiated to explore ways of solving this growing problem.

VLSI semi-custom chip design by computer

Gary Gendel

A system for the automated design of an integrated circuit in use by RCA Solid State Division is based on a collection of various software tools that perform various tasks of IC design, driven by a single program called FASTRACK. This synergy produces rapid turnaround in design cycles and dramatically reduces development costs while insuring a very high probability of first-time success.

Computer-aided experimental structural analysis

C. Voorhees

Experimental structural analysis is another highly specialized area in the field of engineering that is a product of the computer revolution. With the discovery of the Fast Fourier Transform in 1965, FFT analyzers and computer-based structural analysis systems soon followed.

Computer-aided manufacturing at RCA Labs

Keith S. Reid-Green

In a corporate model shop, accuracy may be as important as repeatability. Computerized numerical control (CNC) may represent a way to make those parts that are unusually difficult to make manually. Fast turnaround is as much an issue here as anywhere else—an engineer waiting for a part is a source of wasted money.

The Engineering Corporate Computer Center

Dr. Ronald A. Andrews

The Engineering Corporate Computer Center (ECCC) is currently in operation. First production was in January. The management and operation staff are in place. Experience to date suggests the ECCC will meet the expectations of the user organizations.

Want to write for the *RCA Engineer*?

Need some tips?

Our author's guide gets right to the point . . .

If you are writing an article for the *RCA Engineer's* multidisciplinary engineering audience, the 48-page "Guide for *RCA Engineer* Authors" can show you practical ways to attract and maintain reader interest. The material specifically applies to RCA users. Experienced and novice authors can use many of the universally applicable principles, methods, and examples given here. Each chapter presents a series of Premises, Goals, and Methods that lead you through the writing effort.

The first chapter, "Article Mechanics & Specifications," defines the parts of a complete article package. The second chapter, "Article Content," contains idea starters that will help you to gather the right information and artwork, organize the material, establish and keep audience interest, and write for the reader. The third chapter, "Writing Style," illustrates by example the five major ways to improve written expressions by making them active, lean, clearly qualified, symmetric, and specific.

Send your request for a free copy of the "Guide for *RCA Engineer* Authors" to the *RCA Engineer* Magazine, Technical Excellence Center, 13 Roszel Road, P.O. Box 432, Princeton, NJ 08540-0432. Call Tacnet: 226-3090.

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