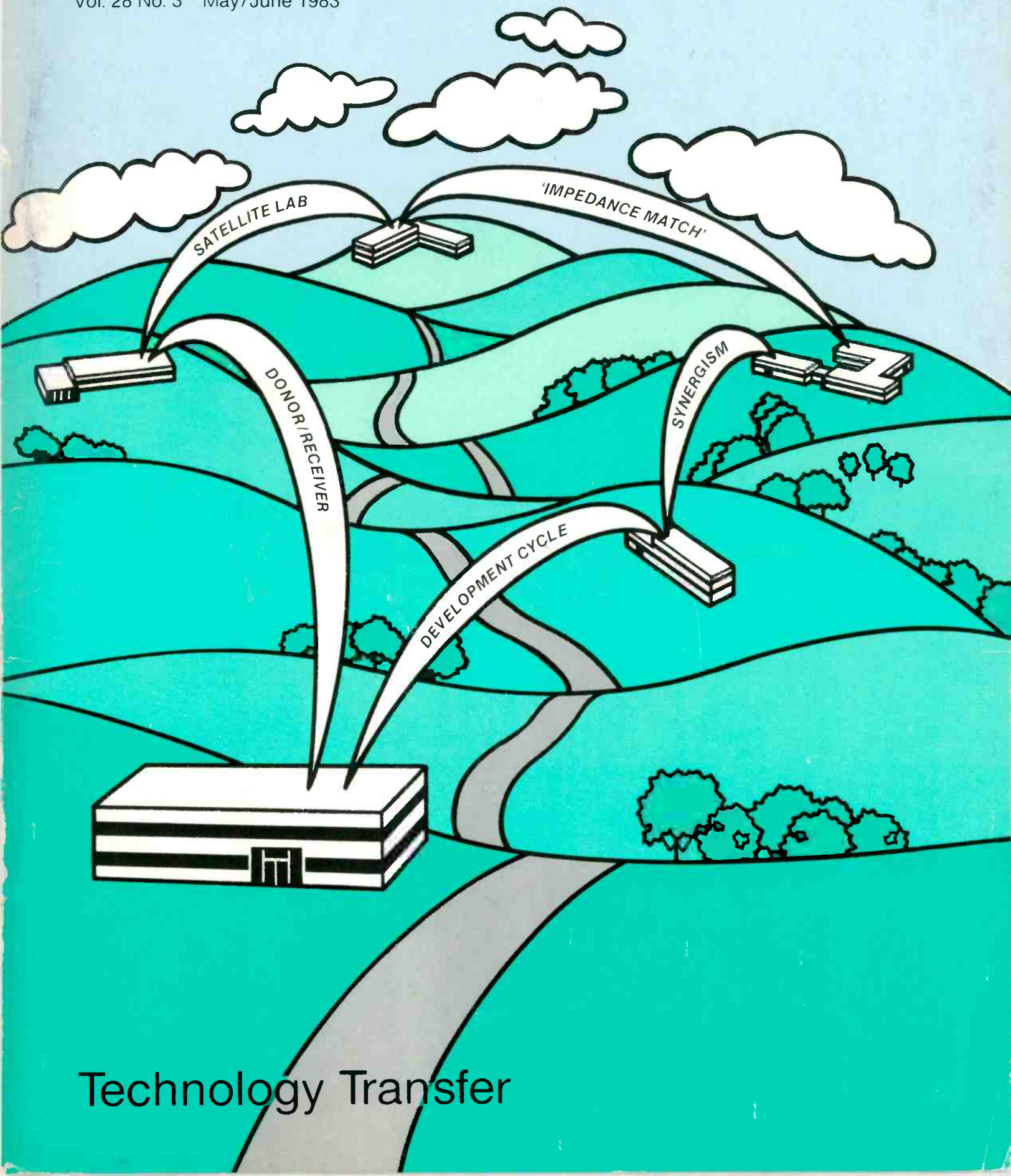
RCA Engineer

Vol. 28 No. 3 May/June 1983



Technology Transfer

Cover design by Louise M. Carr
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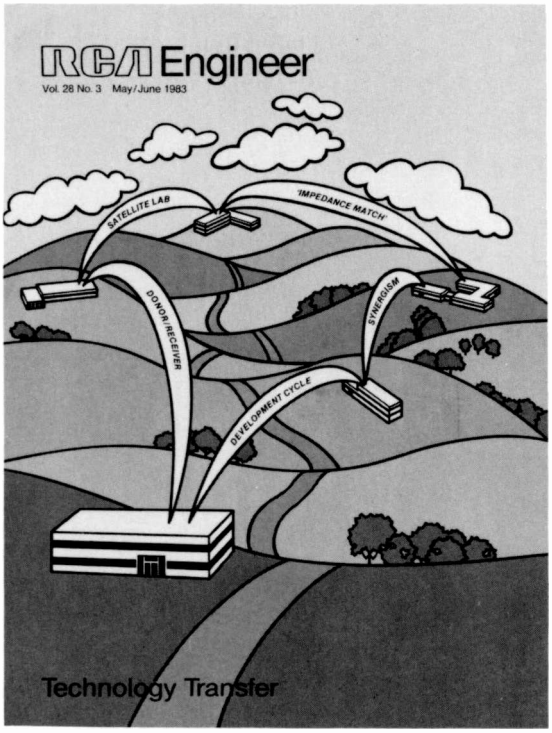

Our cover depicts the information bridges built between engineering groups during a successful technology transfer.

RCA Engineer

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• To disseminate to RCA engineers technical information of professional value • To publish in an appropriate manner important technical developments at RCA, and the role of the engineer • To serve as a medium of interchange of technical information between various groups at RCA • To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions • To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field • To provide a convenient means by which the RCA engineer may review his professional work before associates and engineering management • To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

H. Rosenthal

Technology transfer for industrial survival

It hardly seems possible to add anything useful to what has already been said about the impact of improved industrial productivity on the maintenance of our way of life in the United States. And yet, beneath the level of generalities, the success of our industry and our company comes down to the specific contributions each of us can make. Success results from the integration of all our contributions. Together, they shape the environment, the culture, the progress that makes up our way of life. We can no longer afford, as a company and as a nation, to fail to build on each other's work and on each other's ideas, or to fail to efficiently use all the tools possible.

And that puts some special obligations and duties on all of us, both the donors and the acceptors of transferred technology. The donors must take special pains to put their work in easily understood focus. They should document it clearly, and then stand behind the work to interpret it and to provide full assistance in the transfer as required. The acceptors on their part must be open to the work of others—willing to build on it and to resist the temptations of the "not-invented-here" syndrome.

The Engineering Information unit of Corporate Technology participates by providing channels for information exchange to aid in transfer of technology through the *RCA Engineer, RCA TREND, RCA Technical Abstracts* bulletin, Technical Symposia, Technical Excellence Committees and through a program of rigorous personal communications.

The issue is no longer one simply of desirability. Rather, because of the breadth and sophistication of our competitors worldwide, it has become one of survival for our company, our industry and our nation. With the full recognition of this significance, with the commitment and determination of our management, and with your help, I'm sure we will succeed.

Howard Rosenthal

Howard Rosenthal
Staff Vice-President, Engineering
Corporate Technology

RCA Engineer
Vol. 28 | No. 3 May | June 1983

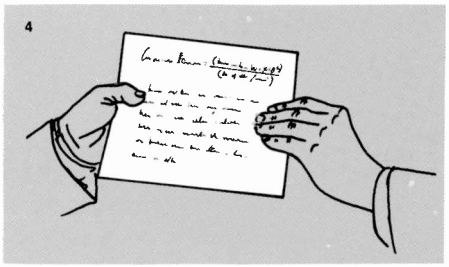
in this issue ...
technology transfer/energy

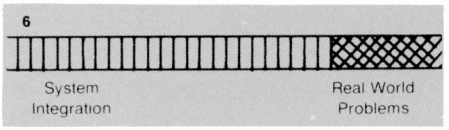
■ **Webster:** *"In RCA we are using the satellite laboratory concept to encourage technology transfer. . . . Although day-to-day management of these groups is the responsibility of the divisions, project planning and monitoring is a partnership responsibility between the Labs and the divisions."*

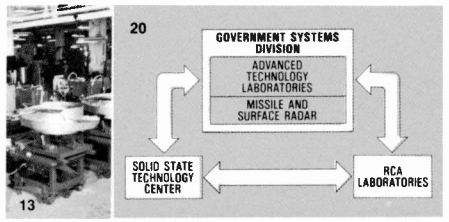
■ **Duschl:** *"It is in this role, as an organizational interface, that the technology transfer laboratories promise to become an essential part of the corporate structure."*

■ **Limberg/Stephens/McCorkle:** *"The MTC is an advanced manufacturing effort that bridges the gap between RCA Laboratories development and the daily needs of the factory."*

■ **Matulis:** *"The [technology transfer] model was developed from our experience and observations in mechanical device development, data and signal processing, system and operational analysis and computer programming, but is not limited to these disciplines.*

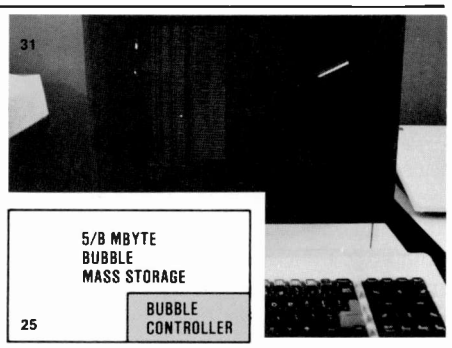






■ **Courcy/DelPriore:** *"By employing state-of-the-art microprocessor and memory technology, an extremely powerful automatic test capability has been packaged into a small, portable, rugged automatic test instrument meeting the military's requirements."*

■ **Hively:** *"The author expects gate arrays to yield to automated standard cells, which will become the dominant approach later in the decade."*



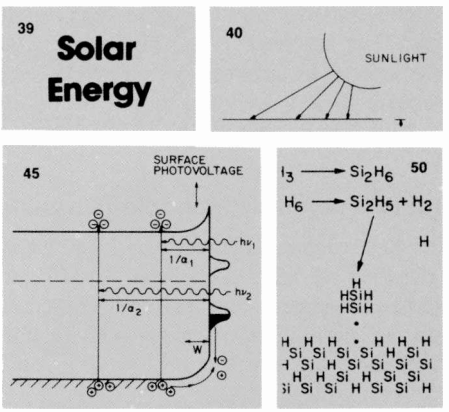
■ **Williams:** *" . . . as of this writing, RCA is seeking to sell its photovoltaic technology, as well as the specialized equipment associated with the solar-energy program."*

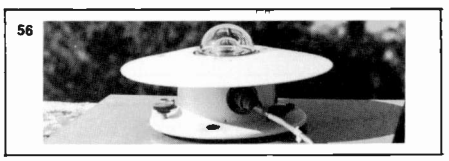
■ **Firester/Carlson:** *"Our research in amorphous-silicon photovoltaic modules will be both the price and performance leader in the next decade."*

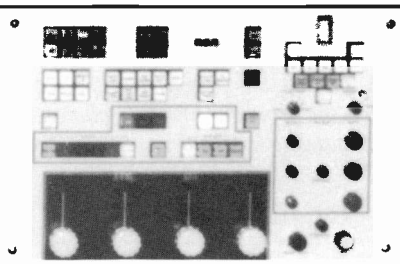
■ **Goldstein/Dresner/Moore/Szostak:** *"[This] method has helped in the optimization of several components of the deposition process and has furnished a convenient and ongoing monitor for evaluating the solar-cell material."*

■ **Catalano/Longeway/Weakliem:** *" . . . the decomposition of silane in a glow discharge, although a good method for the preparation of large-area thin-film a-SiH_x solar cells, is a most complex chemical system."*

■ **Stranix/Firester:** *" . . . RCA in a joint project with the Public Service Electric and Gas (PSE&G) Company of Newark, New Jersey performed an economic evaluation of photovoltaic plants in the PSE&G system."*







in future issues...
anniversary issue,
digital broadcast,
software

W.M. Webster

Technology transfer

Successful technology transfer in a large company reflects the cooperative and communicative spirit of the young entrepreneurial organization, mutual respect, and minimal ego competition.

In young entrepreneurial organizations where the inventor is the president, you never hear the words "technology transfer." If one of these companies survives and then succeeds in becoming a technology-based company with sales exceeding a few hundred million dollars, the odds are that the process, starting with invention and proceeding with development to product design, will involve separate groups at different times and often in different places. Now a new idea has to move through these different groups and finally into manufacturing. Perhaps more often than not something falls between the cracks; hence the interest in technology transfer. Interestingly, there wouldn't be many problems if all the groups (and their management) acted in concert to do the same things that the individual entrepreneur did.

I'm going to make some personal observations based on my experience with respect to technology transfer. Most of my experience has involved transferring projects within RCA from the Laboratories to development groups in the divisions. Sometimes we have done it well and sometimes poorly. Each time I think we have learned something.

Requirements for technology transfer

The first essential is a receiver. I know this may seem obvious but, when we have failed, often it has been because we thought we had an organization that could pick up the project when, in fact, we didn't. The receiving activity must have most of the following characteristics:

- It must be technically capable of pursuing the project through the next phase.
- It must have the stability in terms of funding and direction to finish the next phase.
- There must also be an "impedance match" for transfer at the other end.
- Most important, the project being transferred must have high priority in the eyes of the receiving activity's management.

The next requirement is a project that is *ready* to be transferred. A problem in moving projects from the Laboratories to the divisions arises if we think that we're ready to make the transfer when, in fact, we haven't done enough work at the Labs. An appropriate criterion is to say that a project is ready to transfer from the Labs to a division when technical feasibility has been reasonably well established, and when there are no known technical or economic "show-stoppers."

I use the words "reasonably well established" because sometimes there are problems that can't be anticipated or even found until the project moves to the next phase. On the other hand, there is no excuse for failing to run the kinds of tests, at every step, that represent the environment we would expect the product to encounter. The originating organization must feel responsible for understanding what the product is supposed to do and what the receiving organization is expected to do to meet the market need. There is no substitute for an intimate familiarity with these two factors.

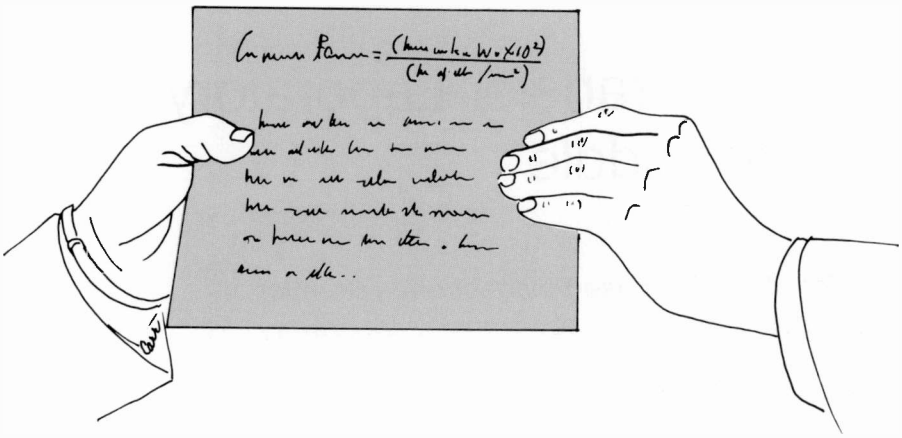
Another criterion that must be established is how to know when the technology has been effectively transferred. This criterion will vary from project to project. The basic condition that must be met is that the receiving organization must be truly and unconditionally comfortable taking on the responsibility for the project.

These three conditions seem pretty obvious and straightforward. How is it that we go wrong? Here is a list.

- The project wasn't right in the first place. No matter how well intended, the originating organization (for example, RCA Laboratories) didn't really understand what the division or market needed.
- The project wasn't ready for transference. The originating organization couldn't answer questions with respect to reliability, tolerances, costs, and so on. Perhaps no one asked these questions and the project was transferred anyway, only to bounce back and forth between the two operations.

Abstract: *"Technology transfer," a term heard often in large organizations, denotes a process by which a new idea moves through different groups and finally into manufacturing. Based on the author's experience in transferring projects within RCA from the Laboratories to development groups in the divisions, the observations in this paper cover the requirements for technology transfer, the problems and the solutions of technology transfer, and the satellite laboratory concept used by RCA Laboratories.*

Final manuscript received March 4, 1983.
Reprint RE-28-3-1



- There really wasn't a receiver. Usually this happened because the receiving organization was, in fact, largely committed to other more urgent projects.
- We thought the project was transferred and it wasn't. The originating organization started playing the role of "consultant," the receiving organization didn't want to admit it still had problems, and management eventually lost patience.

If we analyze the above, we come to the conclusion that if the two activities really understand each other and deal with each other with mutual respect and with minimal ego competition, then the transfer has a high probability of success. The minute we start playing games or fail to work as partners—as a team—we run into trouble.

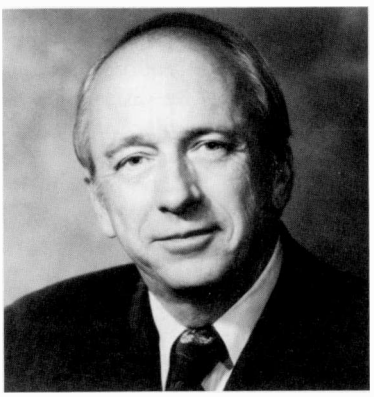
There is a role for documentation, for regular reports, for technical meetings, and for management reviews. All of these tools should be used in managing the project and its transfer from one activity to another. None of them will ensure successful transfer if understanding, mutual respect and cooperation are lacking.

The satellite laboratory concept

In RCA we are using the satellite laboratory concept to encourage technology transfer. The receiving organizations—essentially advanced development groups—are supported in large part or totally by the RCA Laboratories budget but are located in product divisions. Although day-to-day management of these groups is the responsibility of the divisions, project planning and monitoring is a partnership responsibility between the Labs and the divisions. The funding mechanism helps provide continuity. The requirement for a partnership in planning and monitoring develops good mutual understanding and trust, and the arrangement is significantly more conducive to the interchange of people, which is always the best way to transfer technology. These laboratories include the Solid State Technology Center in Somerville, the Manufacturing Technology Center in Indianapolis, the New Products Laboratory in Indianapolis, the Advanced Yoke Development Laboratory in Indianapolis, the Technology Transfer Laboratory in Lancaster, and an embryonic activity in VideoDisc in Indianapolis.

Although these laboratories substantially aid the transfer of technology from the Laboratories to the divisions, we still have a lot of room for improvement—as does everyone. Technical management tends to make the mistake of feeling that once a problem has been solved, it is solved forever. This is probably true of technical problems, but it's certainly not true of management problems that involve human nature. Managers involved in technology transfer must realize that egos exist and that the *natural* tendency for organizations is to drift apart—toward provincialism, the "not-invented-here" syndrome, secrecy, and mistrust. The only preventive medicine I know of is for the management of each activity to bend over backward to maintain a constructive relationship. Instead of each group being willing to meet the other halfway, each must be willing to go a good deal farther.

If the project works, there is always enough glory to go around. And if it doesn't, everyone has failed.



William Webster, Vice President, RCA Laboratories, is responsible for RCA's central research organization located at the David Sarnoff Research Center, Princeton, New Jersey; in Zurich, Switzerland; and, to the extent described in this article, the satellite laboratories in product divisions. A leader in the field of solid state physics, Dr. Webster joined RCA Laboratories in 1946 and made numerous contributions to tube and transistor developments. He rose through a series of management positions to become Staff Vice President, Materials and Device Research, in 1966, and has been in charge of RCA Laboratories since 1968. He was elected to his present position of Corporate Vice President in 1969.

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R.A. Duschl

The Technology Transfer Laboratory—A view from the middle

The successful transfer of a CCD-based inspection system for picture tubes vividly shows the technology-transfer-laboratory concept in action.

As part of the forward march of science and technology, the United States research community is undoubtedly the most prolific group in the history of civilization. From computers to rockets to microbes, our laboratories lead the world in most high-technology areas. Unfortunately, as our Japanese friends have shown us, our perennial leadership in the laboratory is no longer enough to guarantee our leadership in world markets. It seems we are often too busy pursuing tomorrow's breakthrough to fully capitalize on yesterday's success. As the *1982 RCA Annual Report* put it, "Even without new scientific breakthroughs, the technology is in hand to stimulate sweeping changes in our economy and our everyday lives."[1]

Abstract: *In today's competitive world, more than ever, it is imperative that our laboratory successes find their way quickly into the profit-generating portions of the business. This path, however, can be fraught with difficulty due to the common ideological polarization between production and research facilities. The Technology Transfer Laboratory at Lancaster was created as a kind of organizational interface with an aim toward reconciling these differing perspectives. This position in the middle can provide many unique advantages. The intra-organizational journey of one "high tech" project, the CCD-Based Inspection System for television picture tubes, brings some of the more important aspects to light.*

Final manuscript received March 29, 1983.
Reprint RE-28-3-2

There should be no doubt that being on the "cutting edge" of technology is an enviable position. However, more companies are recognizing the importance of getting this new technology into their manufacturing and design centers early and in a cost-effective way. RCA's answer to this problem was the formation of several technology transfer laboratories. The charter of these groups is to make sure RCA's successes in the laboratory (specifically, RCA Laboratories at the David Sarnoff Research Center or DSRC) are identified and appropriately applied to the operating divisions.

For many engineers and scientists, this problem of getting two necessarily different organizations—RCA Laboratories and a division—to communicate effectively is especially familiar. In engineering work it seems we are constantly vexed at the interface problem between the separate functional units of a system. It matters little that each unit can perform well locally when the success of the overall system depends on their mutual cooperation. Likewise, the continuing viability of a technical corporation like RCA increasingly depends on the synergy of its parts. It is in this role, as an organizational interface, that the technology transfer laboratories promise to become an essential part of the corporate structure.

Our specific activity, called the Technology Transfer Laboratory (TTL), specializes in transferring technology particularly applicable to manufacturing systems. We are located at the Video Component and Display Division (the VCDD was formerly Picture Tube Division in Lancaster) along with two other TTL groups to comprise a group of approximately 40 members. There is, however, a very close technical coupling between our on-site groups and the RCA Laboratories in Princeton, New Jersey. Through this unique set-up, TTL can monitor the heartbeat of the division while still having the necessary autonomy and technical resources to work on a problem's long-term cure rather than just the daily symptoms.

Since most *RCA Engineer* readers have spent their careers on one side or the other—in a division or at the Labs—it may be difficult for many to appreciate the view from the middle. On one hand, I see generally the unhampered, unhurried creativity at the Labs and on the other, the fast-paced race at the division to make the product better, faster, and more cost effectively. Having one foot in each location gives us access to the latest ideas, while also seeing firsthand what it takes to make them work in the real world.

CCD-Based Inspection System

An excellent example of how TTL uses its unique position to move high technology into the factory is a project known as the CCD-Based Inspection System. This is, by any standard, a most sophisticated project that uses a large-area charge-coupled device, fiber-optic links, a digital image processor, and the latest Hewlett-Packard minicomputer. And after two years of development, factory installation is slated for June, 1983. Its successful design is the result of TTL's cooperative effort with both the RCA Laboratories and VCDD as illustrated in Fig. 1. I believe that the story of this system's development vividly shows the TTL concept in action.

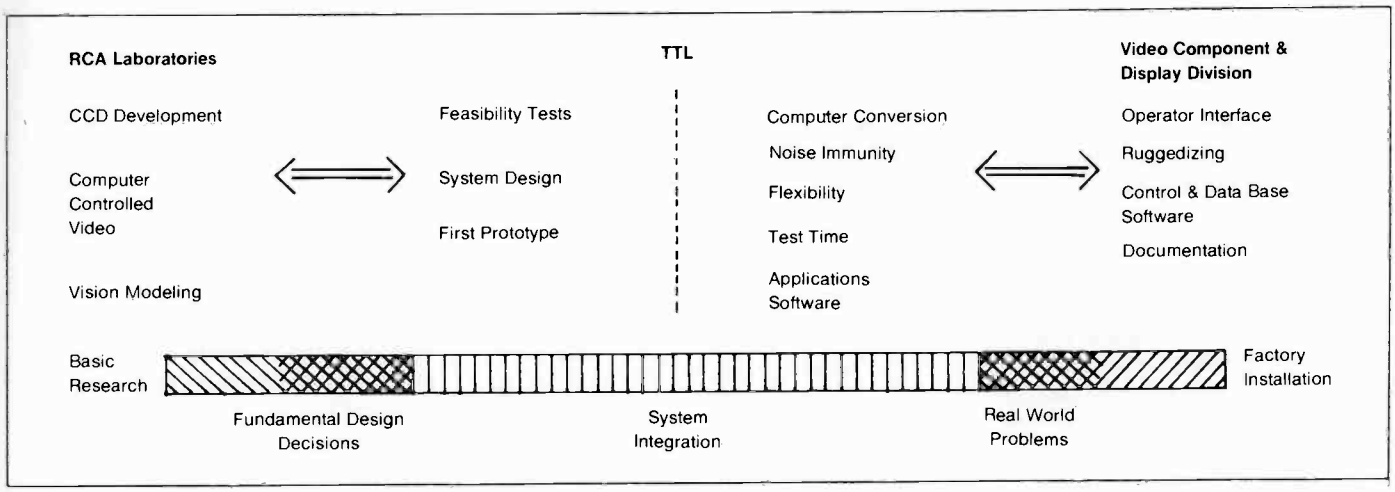


Fig. 1. The flow of technology from basic research to factory installation is represented for the CCD-Based Inspection System. The Technology Transfer Laboratory acts as an organizational interface to assure a smooth flow of appropriate technology.

Fundamental design decisions

We were faced with the need for an automatic picture-tube-inspection station. Such a system required the speed and flexibility of a human operator, but also demanded the calibrated vision and unbroken concentration needed to inspect tubes to meet VCDD's tight standards. Because of the long-term nature of such a project, TTL was asked to see if the technology was available to attempt a solution. Fortunately, TTL, though located at Lancaster, has close ties to one of the largest research organizations in the country—the RCA Laboratories. And, not surprisingly, there were three different basic research areas being worked on at the Labs that helped provide insight and answers to our fundamental design problems. The three areas and their contributions to the system are given in the following paragraphs.

Vision modeling

The basic problem was to try to simulate certain aspects of the human eye-brain combination and, in a limited sense, even improve on them. It was, therefore, very helpful to understand the "specifications" and processes behind the human visual system. For instance, the eye is sensitive to contrast deviations of less than 1 percent in certain spatial frequency ranges.[2] Matching this performance would place stringent demands on both the dynamic range of a sensor and the system's allowable noise figure.

Further discussion on visual research pointed to the importance of measuring both local and global features (at high and low spatial frequencies, respectively) when trying to judge image quality. Relating this to our inspection system, it meant that all picture information must be available simultaneously for us to do meaningful global analysis. This fact, along with the computational complexity of some analysis algorithms, strongly suggested the use of a digital frame store or image processor coupled to a relatively fast minicomputer.

Computer-controlled video

Investigation in this second area essentially supported the decision to use a frame-store and added more insight into sensor requirements. The work being done at Princeton was an attempt to interface a standard vidicon television camera to a digital computer. Video frame memories were not yet available when this work was started and the shortcomings of taking measurements "on the fly" became painfully obvious as the analysis algorithms expanded.

There was also difficulty in getting this raster-based camera to take repeatable measurements from another scanned device—the television picture tube. The vidicon camera itself presented further problems. Its analog nature, including drift, nonlinearities, and invariable data rates, were contrary to the precision and flexibility we were seeking.

Charge-coupled devices

The requirements for the inspection system's image sensor were becoming apparent. The sensor needed measurement accuracy, long-term repeatability, resolution and dynamic range comparable to the human eye, and an exposure method that was insensitive to TV raster. Fortunately, the large-area charge-coupled device (CCD) developed originally at the Labs and later at RCA Electro-Optics & Devices has these capabilities in addition to several others.

The CCD offers an elegant solution to the problem of obtaining accurate exposures from a TV raster. As mentioned earlier, regular TV cameras are not suitable for this task, and similar synchronization and positioning problems are also encountered with a solid-state linear array. A CCD area array, however, can be operated in a "staring" mode whereby it becomes the electronic equivalent to photographic film. In this mode, a shutter exposes the CCD for any integral number of TV frames to achieve an accurate snapshot, even with raster, and over a wide range of tube-brightness conditions.

Other important advantages of the CCD in this application are the two-dimensional spatial accuracy, its good blue response, absence of image lag, and its phenomenal dynamic range.[3] In fact, you will find a CCD in almost every astronomical observatory because of its ability to integrate light and then read it out with up to 4000 different shades of gray.[4]

System integration

After seeing CCDs used to probe the depths of the universe, it seemed that picking up a missing phosphor a few feet away would be relatively simple. The one important difference, however, was the field of view of the optics. We were constrained to image the entire tube face when inspecting for global defects (smears, sags, nonuniformi-

Charge-coupled devices

The solid-state image sensor that is used in this system is called a charge-coupled device (CCD). The basis for this device is the metal-oxide-semiconductor (MOS) capacitor, which is shown in Fig. A with a positive voltage applied across its electrodes. Under these conditions, the majority carriers in the silicon are repelled and a potential well is formed in the silicon substrate. Any electrons optically or thermally generated near this well will accumulate at the point of greatest potential, which is at the interface between the silicon and the silicon dioxide. It is often helpful to picture the mechanism just described as a bucket (potential well) partially filled by a fluid (electrons), as shown in Fig. B.

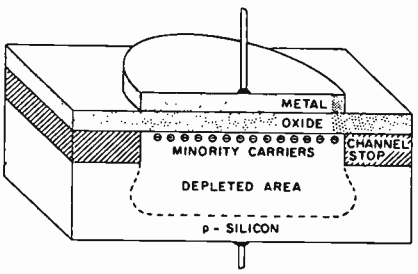


Fig. A. *MOS capacitor. Minority carriers (electrons) are attracted to the positive potential of the electrode.*

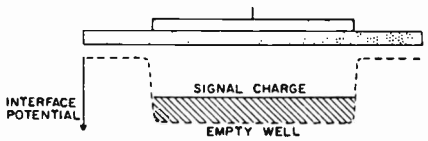


Fig. B. *Charge-coupled device model.*

If two of these MOS capacitors are placed relatively close together, their potential wells will overlap or couple, and any mobile electrons will then be attracted to the location with the higher interface potential. In terms of the fluid model, the charge flows to the deepest part of the combined well as in Fig. C. This gives the capability of transferring a charge packet throughout the silicon substrate by properly biasing external electrodes.

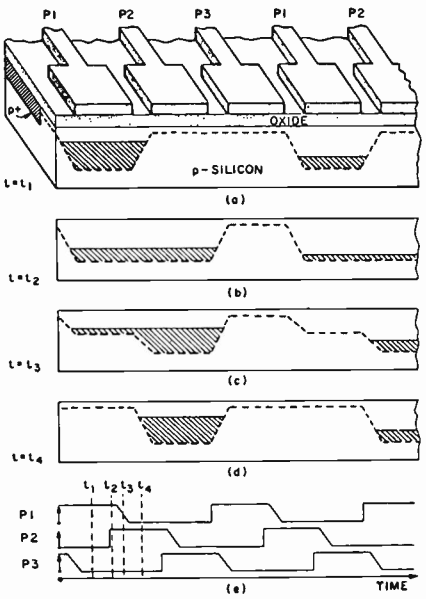


Fig. C. *Method of charge transport.* **(a)** *Cross section of silicon substrate.* **(b, c, d)** *Moving potential well at subsequent time intervals.* **(e)** *Drive waveforms for electrodes.*

Optically generated minority carriers allow the CCD to be used as an image-sensing device. One major difference in the RCA CCD is that it collects photons from its back side, as shown in Figs. D and E. This means that there are no dead spots in the imaging area that could partially obscure small points of light. The silicon bulk, however, must be thin enough so that the optically generated carriers can make it to a potential well before recombination.

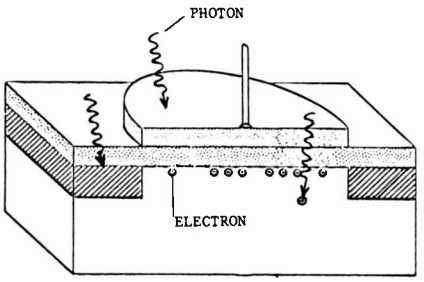


Fig. D. *Typical image sensor. Electrodes and channel stops block or attenuate many incident photons of light.*

A useful solid-state imaging array can be formed from the three basic MOS capacitor cells (Fig. C) by arranging them in a periodic sequence. Several types of readout organization are possible, but the RCA device uses the frame-transfer pattern that is schematically shown in Fig. F. After exposure, the resulting charge pattern in this device is completely shifted up one row, with the top row going into the horizontal register. This top row is then shifted serially until the entire row has been clocked one at a time into the output cell. From this point, the horizontal register is ready for the parallel load of the second row, with this sequence repeating until all the "buckets" have been emptied into the output register. This type of readout organization allows control of many pixels with only six external transfer electrodes, while also enabling all charge packets to be sensed at a single detection node.

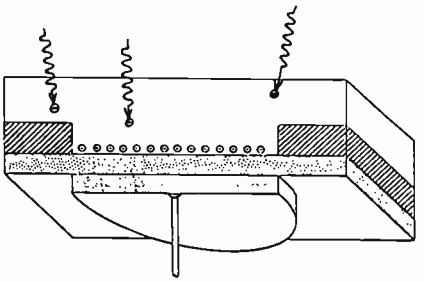


Fig. E. *RCA thinned CCD sensor. There are no opaque spots in the imaging area because light can be collected from the backside.*

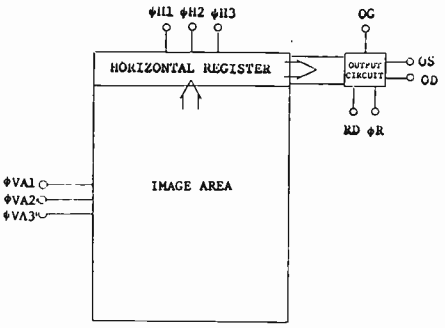


Fig. F. *Schematic diagram of the frame-transfer readout organization.*

Figures A through D are reprinted from C.H. Sequin and M.F. Tompsett, *Charge Transfer Devices.* Copyright © 1975 by Academic Press, Inc., New York.

ties); we also needed good resolution to pick out local defects (missing phosphors, blocked apertures, film splashes). The contradiction soon became apparent. We wanted many picture elements (pixels) so we could detect very small defects, but too many pixels would be difficult to digitize, store, and process in a reasonable amount of time.

The answer became apparent by again examining how the eye solves the problem. You can illustrate the process to yourself by examining Fig. 2. The eye doesn't see the several well-defined, high-contrast point defects from a viewing distance but rather it perceives one larger, lower-contrast blemish. The unique structure of the RCA CCD allows us to use a similar technique to solve our resolution dilemma. Figure 3 shows how a blemish that is smaller than a pixel can be detected. A judgment on this defect's severity is made by comparing the defect's total amount of light to the average of several neighboring pixels. This technique allows a good compromise for detection of both point defects and uniformity defects with a reasonable number of resolution elements. In effect, we are trading the CCDs fantastic dynamic range for more resolution. This is a favorable trade because today's word-oriented computers can process a picture with 12 bits of gray just as quickly as they can process a 1-bit binary image.

With this important problem solved, the system configuration shown in Fig. 4 was proposed. Again, the important design decisions called for the use of an RCA 320 × 512 CCD operated in the slow-scan staring mode and the use of an image processor to store the entire image in digital memory. As an added bonus, the image processor (IP) could be used to generate the test patterns needed on the picture tube under test. A typical test cycle would proceed as follows: (a) the computer determines test patterns needed and loads them into the IP; (b) the patterns are converted to analog and displayed on tube; (c) the shutter exposes the CCD for n TV frames; (d) the CCD information is digitized and loaded into the IP over test pattern data; and (e) the computer analyzes the picture off-line while the next tube moves into position.

Work on the basic configuration was begun to prove the fundamental design concepts. Most of the difficulty at this early stage was with the CCD camera development and the writing of control and analysis software for the image processor. The CCD head unit was completely custom designed to allow operation in the variable-scan, staring mode while also providing special electronics to preserve the CCD's 75-dB signal-to-noise ratio. The image-processing software was also of original design to allow the utmost of flexibility for early developmental stages.

After almost a year of preliminary work, it appeared feasible to use the proposed configuration to inspect picture tubes. We at TTL had drawn from the three basic research areas at the RCA Laboratories to prove that today's most advanced technology could finally begin to address this most difficult inspection problem. At this time, our emphasis would shift from working with the Labs to working with VCDD engineers.

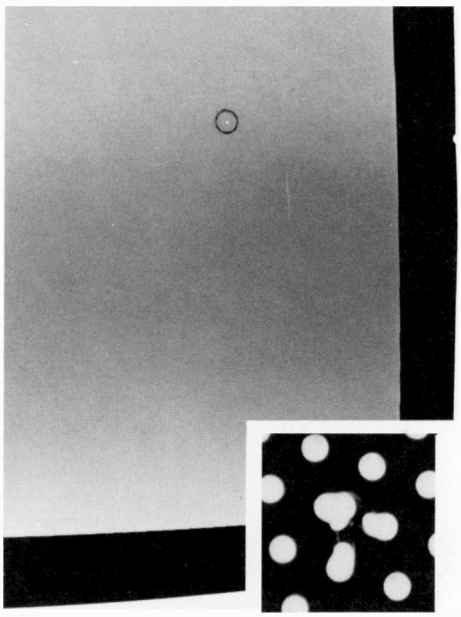


Fig. 2. The CCD mimics the human eye in its gray-scale and local averaging characteristics. Even though neither can "resolve" the defect (see inset) on the shadow mask, both can detect its presence by looking for local gray-scale variations.

Real-world problems

Often in the past, a project such as this one would be completely handed over to the division personnel at this stage of development. Here it would usually be repackaged and sent off to the factory where, after a few days of scrutiny, it would somehow end up little-used and little-appreciated. Both sides would have good intentions, but neither could communicate or see the other's point of view.

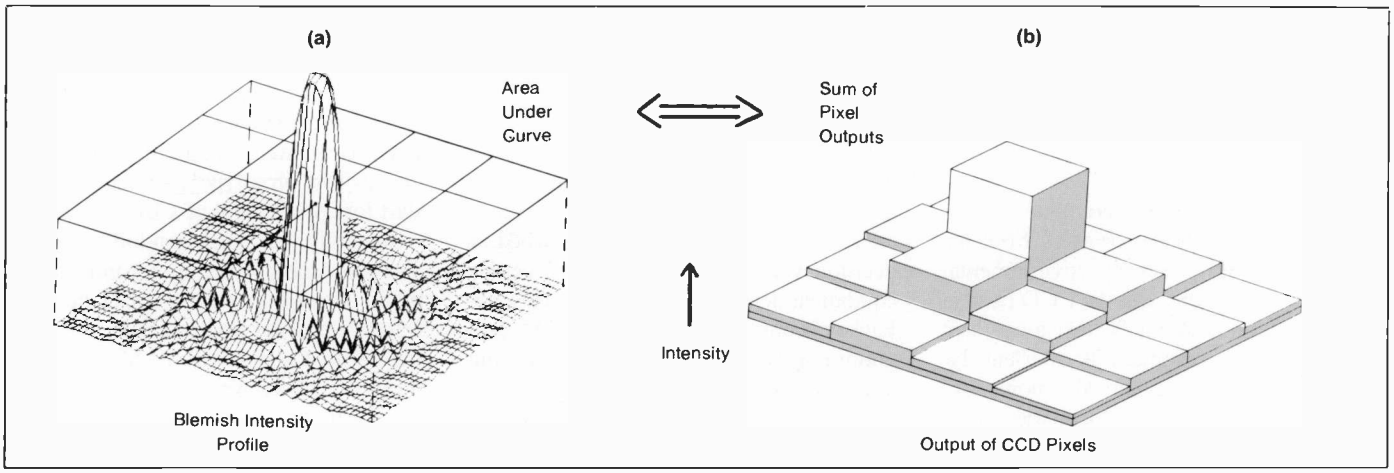


Fig. 3. **(a)** A defect's two-dimensional intensity profile is represented. The overlayed 4 × 4 grid shows the areas of the surface that would be locally averaged to form the CCD output as represented in **(b)**. Note that the areas under the curves of **(a)** and **(b)** are equal regardless of the pixel-to-defect alignment. Therefore, the extra light in the defect area can be accurately summed to determine the defect's severity. This "backhanded" measurement technique greatly reduces the number of resolution elements needed in order to look for very small defects.

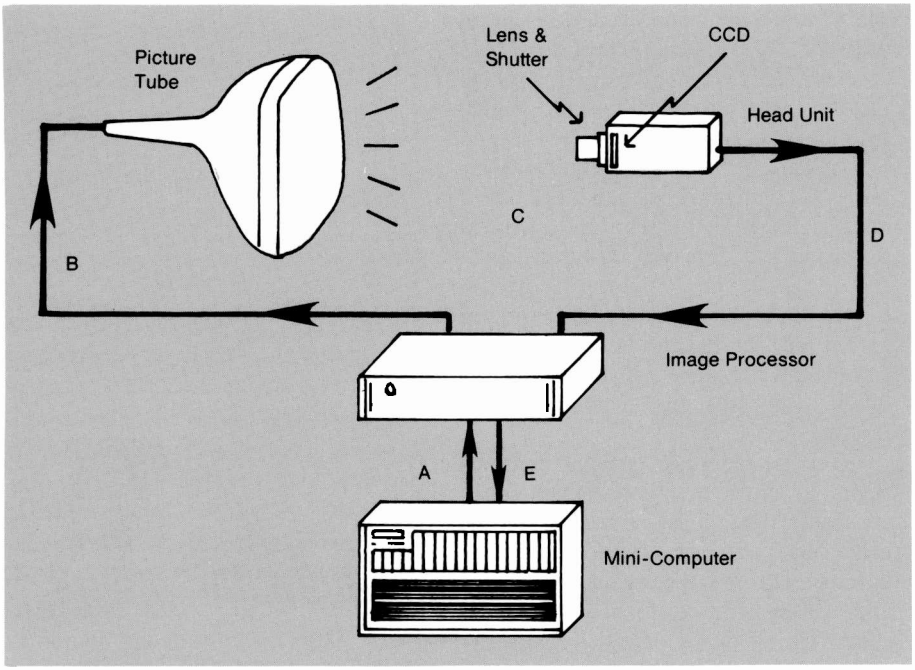


Fig. 4. Basic configuration of automated picture-tube inspection system. Operation would proceed as follows: (a) a computer determines test patterns needed and loads them into the Image Processor, (b) patterns are converted to analog and displayed on tube, (c) shutter exposes the CCD for *n* TV frames, (d) CCD information is digitized and loaded into the Image Processor over test pattern data, (e) computer analyzes picture off-line while the next tube moves into position.

Since avoiding this problem was essentially TTL's charter, we were determined to carefully examine both perspectives before transferring the project. And sure enough, from the manufacturing point of view, the system had some basic design problems. These were not quick-fix problems, but ones that took some time to solve and demanded a thorough knowledge of the system. And, more critically, these were problems that could kill the project if not worked out at this point. The following is a discussion of four "real-world" problems that TTL had to solve before the system was transferred to VCDD.

Noise

We wanted to keep the computer equipment and image processor away from the production line for several environmental and logistical reasons. But the CCD camera head, positioned about 30 feet away, still was expected to maintain its excellent dynamic range in an electrically noisy factory environment. The problem was solved by using fiber-optic links to couple all signals between the two separate locations. These links provide electrical isolation to prevent troublesome ground loops and also prohibit noise coupling from surrounding heavy equipment.

Upgradability

The newness of the CCD, which was barely out of the laboratory, was another factory concern. At this early stage in CCD development, the devices were rapidly getting larger and constantly being improved. We wanted future sensor upgrades to be as quick and painless as possible. To solve this problem, a custom-programmable scanner was designed into the system. This allows the CCD pixel count and even the drive waveform to be reprogrammed in a matter of minutes. This permits much flexibility in choosing only the sensor capacity that is needed for a particular application.

Computer choice

This problem was especially surprising and ultimately very time-consuming. Sometime after the first prototype was finished, a decision was made to standardize certain equipment developments by using Hewlett-Packard computers and the PASCAL programming language. Needless to say, our initial system used neither.

Since this system was expected to find long-term use in VCDD, conformance with these standards was deemed essential. The conversion would have been next to impossible for someone not intimately familiar with the system. Over 10,000 lines of test and system software were rewritten and modularized in PASCAL. A custom Direct-Memory-Access (DMA) interface and software drivers were also designed between the image processor and a Hewlett-Packard 1000A minicomputer.

Test time

During this project's development, the specification of total allowable test time had been further reduced. To meet this more stringent time constraint, some sophisticated parallel-processing techniques had to be devised. It was necessary to have four real-time programs running at once to meet our speed requirements. This setup used mailbox input/output for program synchronization and shareable extended memory (EMA) for program-to-program communications.

Figure 5 shows a flow diagram of the critical parts of the software system. We used machine code to program a bit slice in the image processor for preprocessing of calculation-intensive algorithms. A second program, which is 99-percent I/O suspended, is used to perform a DMA read to collect immediate results from the image processor. Yet another program looks at these results and starts processing as soon as enough data points are available. Finally, the last program is used for synchronization and error handling of the three other programs.

Technology transfer

Even while the previously described modifications were taking place, the technology transfer had already begun. Numerous meetings and several formal presentations were given to keep VCDD managers and engineers informed of our progress. As the time for transfer neared, VCDD engineers studied our schematics and logged some hands-on experience with our equipment. Even as we were putting the final touches on this first prototype, they had a running start for construction of a factory model.

Recently, the final handoff took place and was accompanied by a complete schematic package (in their format), numerous software analysis and exerciser routines (in the division's standard PASCAL), and a promise that we were just down the hall if there were any questions or problems. The last feature has to be one of the most important aspects of TTL—we are available on-site to give continued support until the unit is operational in the factory.

Of course, the VCDD engineers still have much work to do on the transferred

Image processor bridges image-understanding gap

The digital image processor, more than any other instrument, has been the driving force behind the current computer-graphics explosion. Once confined to the back rooms of NASA, recent advances in very large scale integration have allowed the image processor to be used in areas ranging from robotics to video games. A schematic diagram of a typical configuration is shown in Fig. A.

The major hardware and cost block is usually the large (in our system 3.9 Mbits) solid-state image memory, sometimes called a frame store. Each word of this memory contains the intensity data for one pixel of the image. This storage organization gives the computer high-speed, random access to precisely located pieces of the stored picture. Various analysis algorithms can then be programmed to enhance, measure, or even recognize specific features within a scene.

To sift through the huge amount of data contained in an image, many systems include an on-board microprocessor. This feature enables the host computer to use high-level graphics commands (such as READ BLOCK or DRAW CIRCLE); the actual pixel data manipulations are done by the microprocessor at high speed. A Writable Control Store in this block can also allow the user to implement time-critical operations (in our application, an edge-finding algorithm) by defining a new graphics command in microcode.

Another critical fuction of the image processor is to convert the mass of digitized picture data, stored in memory, back into a standard TV format for viewing on a monitor. This is accomplished by using digital-to-analog converters—look-up tables are used to assign colors to selected intensity bands, a technique known as false coloring.

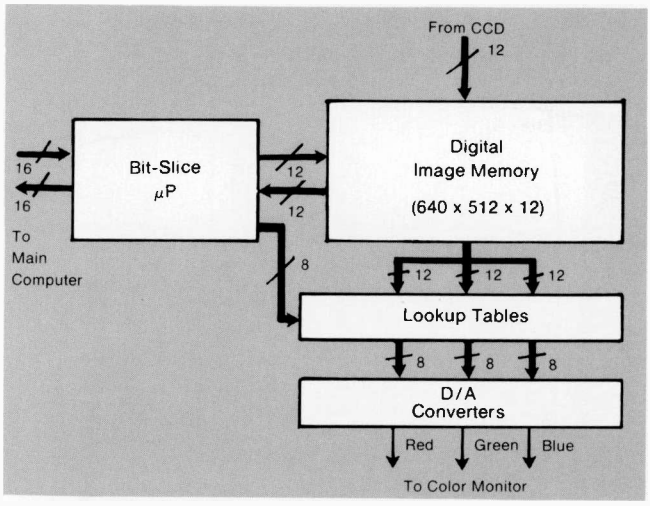


Fig. A. *Typical image processor configuration.*

Figures 6 and 7 in the main text dramatize the image processor's role in computer graphics. The two photographs are of the same image data but Fig. 6 is in computer readable format and Fig. 7 is in "human readable" format. Until recently, these vastly different data structures have kept the two worlds apart. But, with the advent of the image processor, the computer can finally bridge the gap and lend its power to problems in image analysis, generation, and ultimately to image understanding.

prototype unit. Basically, their role is to customize and repackage it. Some examples are the software for the operator interface, database management and reporting, and numerous control functions. This work will vary somewhat, depending on the system's location within a specific plant. But basically, after the first system is successfully placed, VCDD will assume all responsibility for this and for duplicate factory units.

Enhancements

As our role diminishes in the first factory model of the CCD-Based Inspection System, we are already working on the next generation. Much work can be done on developing faster and more accurate analysis algorithms. We are also in the process of incorporating an infrared CCD into this same inspection system using almost identical hardware and software. Again, we are working closely with the RCA Laboratories in both of these state-of-the-art applications.

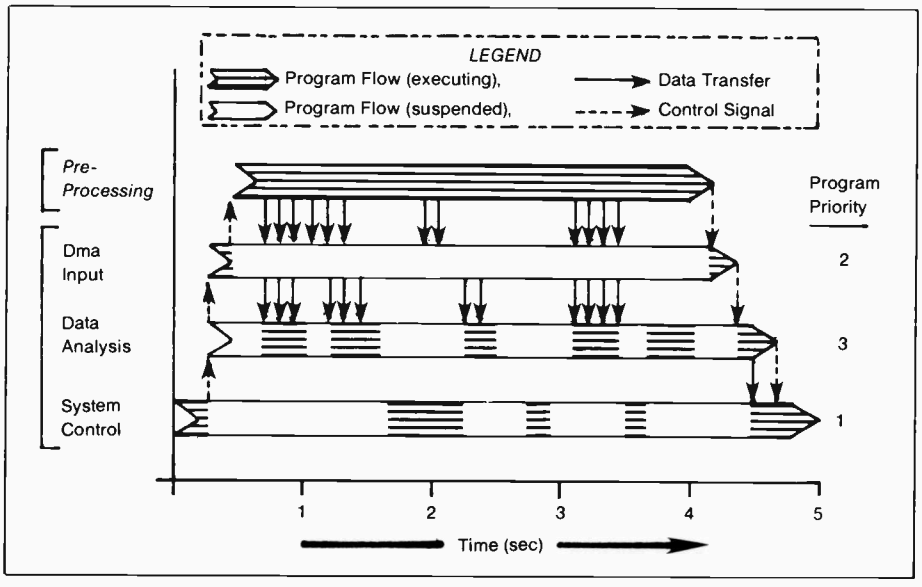
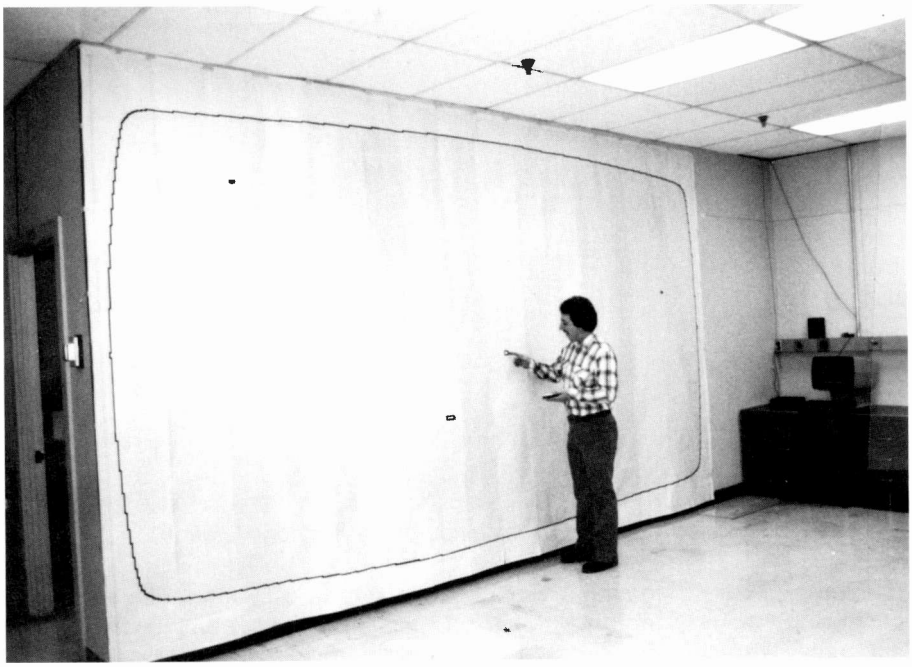


Fig. 5. Flow diagram of the software system. The preprocessing algorithm, which is programmed into the image processor, runs concurrently with the three programs in the minicomputer. This parallel software structure allows program activation only when defect data is available—which is random in nature. In practice, approximately 90 percent of this system's total run time can be used to execute other background (that is, data logging and user I/O) programs.



(a)

352	362	373	372	366	354	371	371	362	357	362	349	361	359
356	355	367	361	357	350	361	357	370	353	345	360	383	369
364	355	362	370	359	365	362	378	370	341	358	384	356	370
341	355	374	361	349	336	367	369	368	385	352	359	387	363
348	357	360	373	364	358	361	373	380	347	353	355	375	376
358	372	361	373	353	353	384	386	371	350	345	366	376	371
355	358	371	372	360	349	432	425	385	340	363	350	380	370
361	373	367	366	376	388	1005	990	402	379	352	363	360	362
35	359	364	379	364	386	1007	1001	398	342	354	370	370	365
351	360	368	380	367	361	529	426	376	365	348	351	372	373
358	364	376	366	366	342	374	379	361	356	348	371	366	371
347	360	363	381	359	363	359	364	374	349	354	348	364	368
356	361	384	368	358	343	360	372	355	356	347	371	378	363
359	373	376	377	363	347	361	364	386	361	352	346	359	384
350	371	379	379	362	361	362	369	358	347	361	351	364	371

(b)

Fig. 6. (a) This printout mural is used to dramatize just how much data is contained in one image of a picture tube. An actual segment of the 10′ × 20′ array is shown in **(b)**. Notice that this is also a close-up of the defect being pointed to in **(a)**. In a typical test, each data point is examined by the computer at least nine times.

Conclusions

The flow of high technology from the research lab to the factory floor has often been unnecessarily difficult in the past. The TTL concept was created with the goal of improving this problem. I believe that the successful transfer of the CCD-Based Inspection System validates this initial concept. Our main advantage is that we extend the vast resources of the corporate research center into the facilities of a particular division. Here we can listen, learn, and apply these resources in familiar surroundings, on familiar equipment and processes, and most important, with familiar faces.

In a recent article, George T. Rehfeldt, a vice-president at Cincinnati Milacron, commented, "We are moving from the bump, funk, and clunk era to a world in which everything whirs very gently."[5] For a high-technology company like RCA, this second industrial revolution means difficult competition but also fantastic growth opportunities.[6] It is in this future that the Technology Transfer Laboratory figures to be a vital link in the effective and timely transfer of RCA's wealth of technology to the blossoming high-tech marketplace.

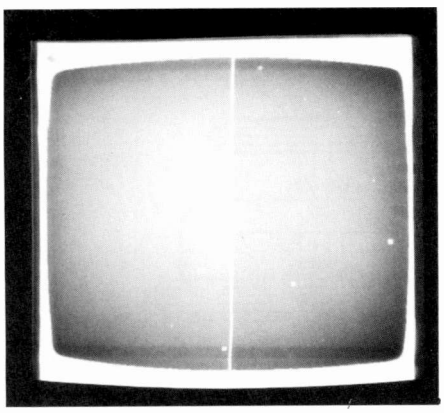


Fig. 7. This is the same image as in Fig. 6, but in a form more convenient for us—nondigital entities. It represents a typical output on the system monitor when inspecting a picture-tube faceplate with back-lighting. An overlay mask is used to electrically ignore data beyond the tube perimeter and also any bad CCD pixels. The out-of-spec defects are boxed in to provide visual feedback if necessary.

Acknowledgments

I wish to express my warmest appreciations to (counterclockwise from the top left on the monitor in the author photo) N.D. Welch, S.A. Werner, and C.M. Weaver, Jr. for their valuable contributions to this project. I also would like to thank the many people at the RCA Laboratories, EO&D, and VCDD who offered their insights and experience for the benefit of this program.

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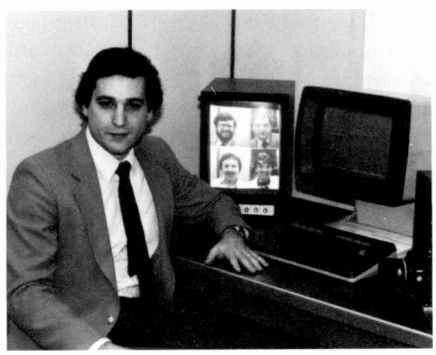

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The Manufacturing Technology Center: Key to advanced consumer-electronics manufacturing methods

This satellite laboratory, serving RCA's consumer electronics manufacturing centers, builds technological bridges based on the FACTS, and on other advanced methods for streamlining and improving manufacturing.

Abstract: *The Manufacturing Technology Center (MTC) builds a technological bridge between long-term RCA Laboratories development and the immediate needs of Consumer Electronics's manufacturing facilities. After summarizing MTC's role, the authors describe the FACTS (Factory Analysis Control and Tracking System) project, which successfully integrates computers and people into a system giving real-time control for total factory management. Full descriptions of this system and other projects are included. An automatic paint-finishing system, a system for use of leadless chip components, a high-speed manufacturing system for multiple switches, statistical methods applications, and other projects are described.*

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A market as competitive as consumer electronics demands efficient manufacturing methods. The latest manufacturing technologies must be translated into practical manufacturing processes that have high yields and low cost. The Manufacturing Technology Center (MTC) is part of RCA's efforts to compete successfully. The MTC, responsible for developing advanced manufacturing techniques and equipment for the Consumer Electronics Division, is a satellite of RCA Laboratories and is located at the Consumer Electronics Division headquarters in Indianapolis.

The MTC is an advanced manufacturing effort that bridges the gap between RCA Laboratories development and the daily needs of the factory. It also monitors worldwide manufacturing developments and translates up-to-date technology into practical manufacturing methods and systems. To accomplish these challenging tasks, the MTC is organized into skill centers (Fig. 1). Through these skill centers, the MTC can assign the appropriate talent to work on any project.

The skill-center approach is applied on a project basis. Thus, projects involving factory information systems are assigned to the Software Engineering group, robotic systems to the Assembly Equipment Design group, advanced test systems to the Advanced Electronic Systems group, and material handling projects to the Material Handling Systems group. Major projects that involve MTC and several other departments or plants are assigned to a Project Engineer for total project coordination.

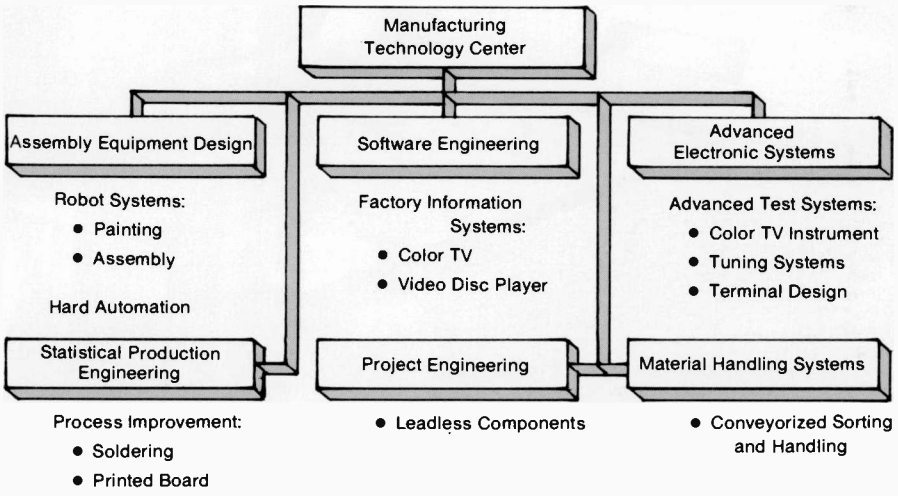

Fig. 1. *Organization of the Manufacturing Technology Center.*

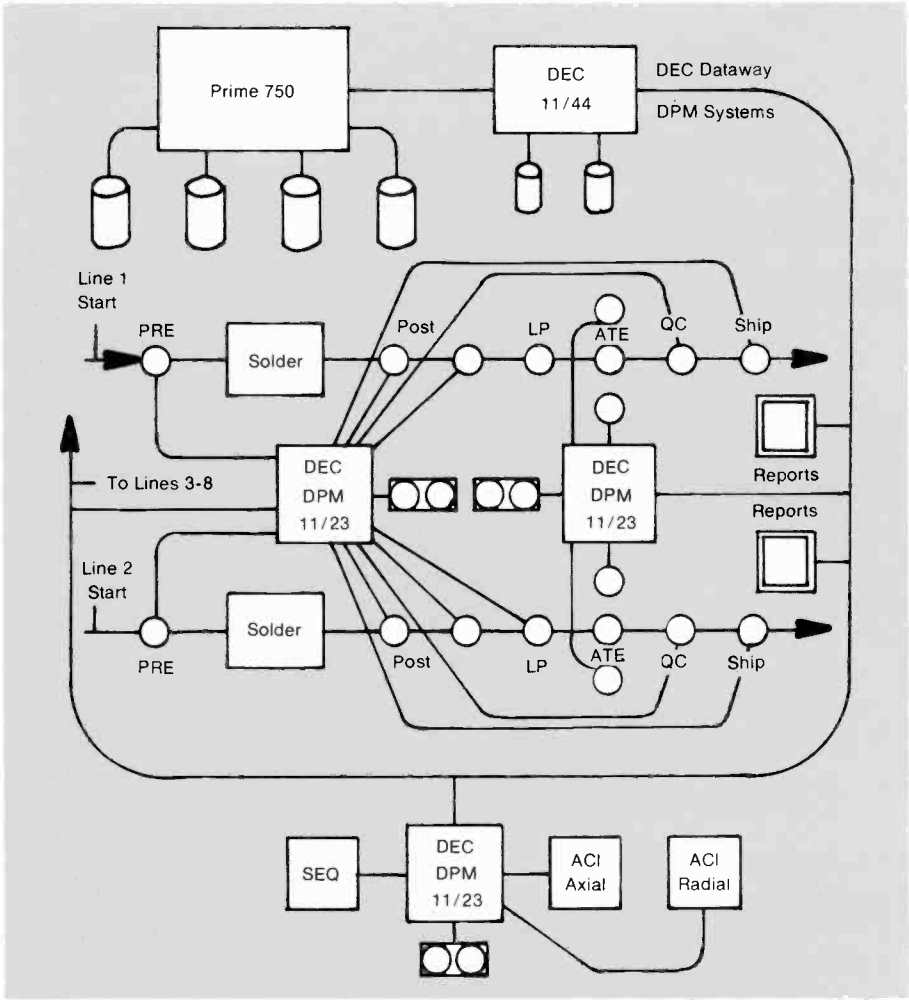

Fig. 2. *The FACTS system. The heart of the FACTS system is a PRIME 750 minicomputer with 1200 megabytes of disc storage and a DEC 11/44 minicomputer with 84 megabytes of disc storage. Each of the automatic test equipment (ATE) units transmits test data automatically to the computers. Operators, using FRED terminals, enter other test and repair data. The reports are presented on video display and printing terminals located throughout the plant.*

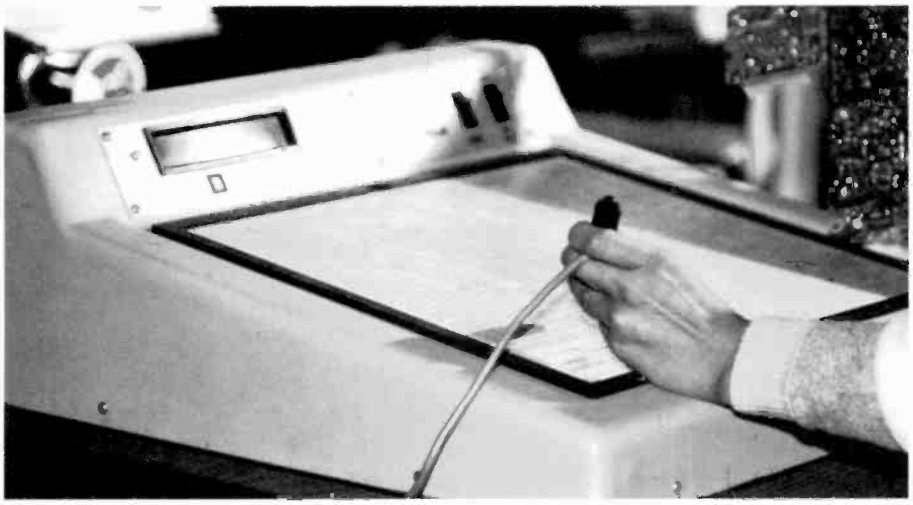

Fig. 3. *The FRED terminal. This custom-designed terminal is one of several located on each manufacturing line. It is used to transmit chassis serial numbers, repair codes, and part legends to the data-collection computer. Its digitizing tablet is used to translate line data into defect and repair codes.*

CAM for assembly processes

Up-to-the-minute information about the operation of an assembly line is necessary for the improvement of factory yields and product quality. With the increased complexity of consumer products and the automation of the assembly and testing process, the volume of available data has increased significantly. The traditional methods of manual data collection and analysis are slow and often subject to error. The FACTS project (**F**actory **A**nalysis **C**ontrol and **T**racking **S**ystem) is the next step toward the use of the speed and power of computers as a primary tool in real-time control for total factory management at Consumer Electronics.

The FACTS system will provide the following information at our Juarez chassis plant: Production counts, yield tracking, unit history on each chassis, process trend analysis, test equipment control, automatic component insertion equipment control, down-time recording, indirect labor control, and the potential elimination of manual records. The system has been installed on two chassis lines and will be expanded to operate on eight chassis lines.

The major components of the system are a PRIME 750, a DEC 11/44, six DEC DPM23s, and eight microprocessors. Data is collected directly from automatic test equipment, axial component inserters, radial component inserters, axial component sequencers, photodiode sensors, and manual-entry touchpad work stations. Figure 2 is a schematic layout of the FACTS system showing two assembly lines.

The data-storage, analysis and report-generation functions are performed by the PRIME 750. Data is accepted from the communications network, then stored on the four 300-megabyte disc drives. The communication network is controlled by the DEC 11/44 acting as a communication front-end processor. A single cable called a Dataway connects the DEC 11/44 with the six DPM23s. Each data station is connected to a DPM23. Data flow, then, is from the input station to its DPM23 concentrator, then on to the Dataway and the DEC 11/44 communication controller, and finally to the PRIME 750. Report distribution goes directly from the PRIME 750 to the many user terminals located throughout the Juarez plant via a local modem network.

Data input devices

Currently, every chassis is partially assembled by axial and radial component inser-

tion equipment. Each computer-controlled machine can collect data concerning its own efficiency and speed. This data is automatically transmitted directly to FACTS. Each chassis is also automatically tested and aligned. The results of each test cycle are also transmitted automatically to the FACTS system.

All of the data gathered from the chassis lines is collected via an MTC-developed terminal called FRED (**F**actory **R**eporting **E**ntry **D**evice). The information concerning solder defects, assembly errors, and the required repairs are entered using FREDs (Fig. 3). Each FRED has a flat, smooth digitizer touchpad on which a template of desired information has been placed. Data is entered simply by touching areas on the template corresponding to the observed defects or repairs. The chassis identity is entered via a built-in bar-code "light pen." The FRED translates each touched point into a part name or defect type, correlates it with the chassis serial number, and passes it automatically into the communications network. Each chassis line is configured with FREDs at all the desired manual data-entry points.

Accurate production counts are necessary for the efficient operation of a chassis plant. The production counts will be maintained by a series of eight microprocessors and photodiodes placed in the conveyors. These microprocessors tabulate the counts and pass them to the communications network on command from the FACTS system.

Automation—Hard and soft

As one of the next steps in Consumer Electronics's movement toward improved manufacturing, the MTC was commissioned to co-develop with the Indianapolis Components Plant an automatic paint-finishing system for TV plastic cabinet production (Fig. 4). The automatic spray-painting system consists of five major components: an automatic conveyor system, a paint-mask wash/dry system, a parts-handling robot, a five-axis Mitsubishi spray-paint robot, and a programmable controller to coordinate the entire process.

The TV cabinets are presented to the parts-handling robot by an indexing belt conveyor. Before the cabinets are removed from the conveyor, they are cleaned with electrostatic air jets to remove any loose dirt particles. The cabinets are removed from the conveyor and placed in the paint fixture by a custom-designed three-axis robot. A unique fixture grasps and centers

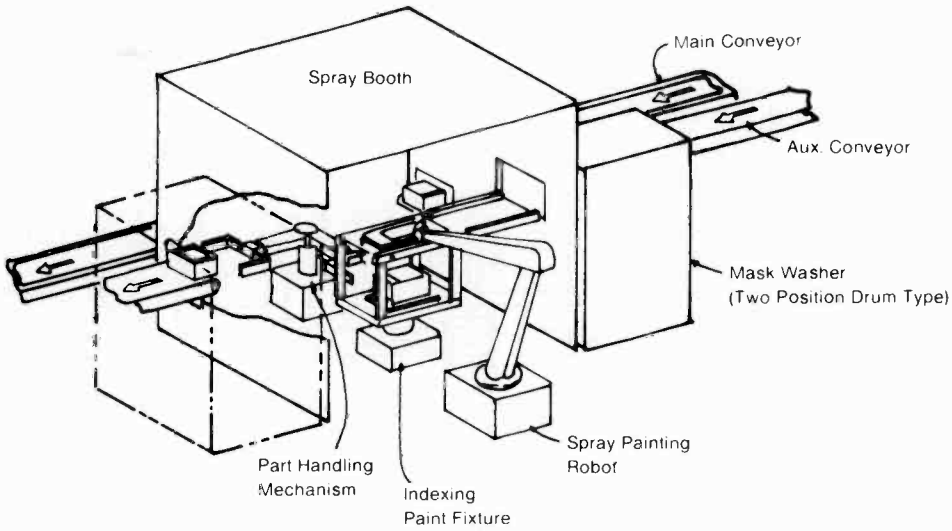

Fig. 4a. *Robotic spray-paint system. This is a schematic layout of the spray-paint system installed at the Indianapolis plant. Plastic cabinets enter on the auxiliary conveyor, are painted by the robot, and placed back on the main line.*

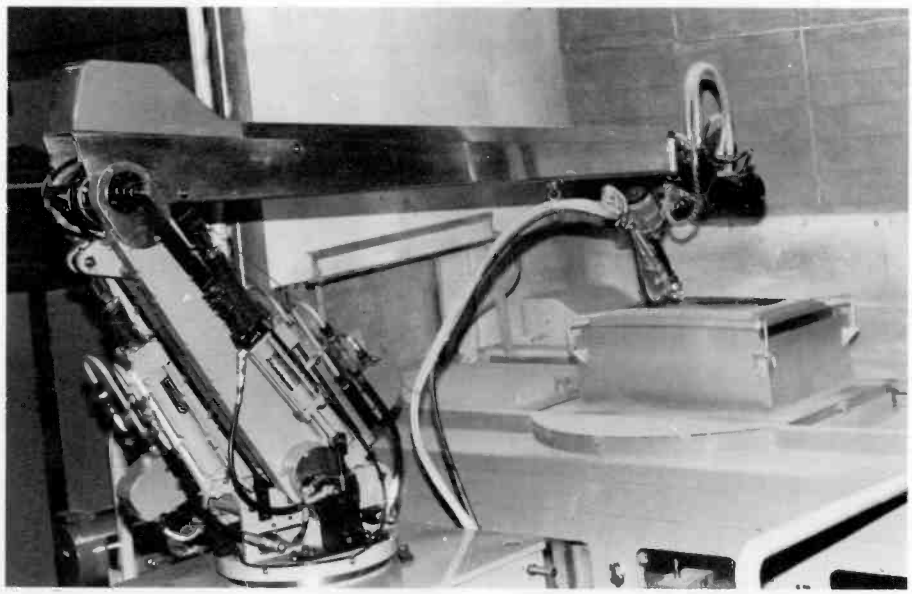

Fig. 4b. *The robotic spray-paint system.*

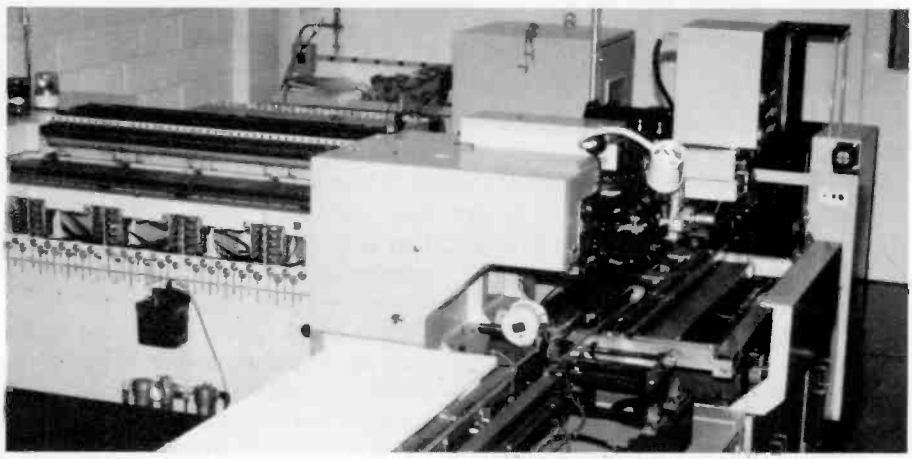

Fig. 5. *Chip-placement machine. This machine sequences chips, places the epoxy, and positions the chips on the board.*

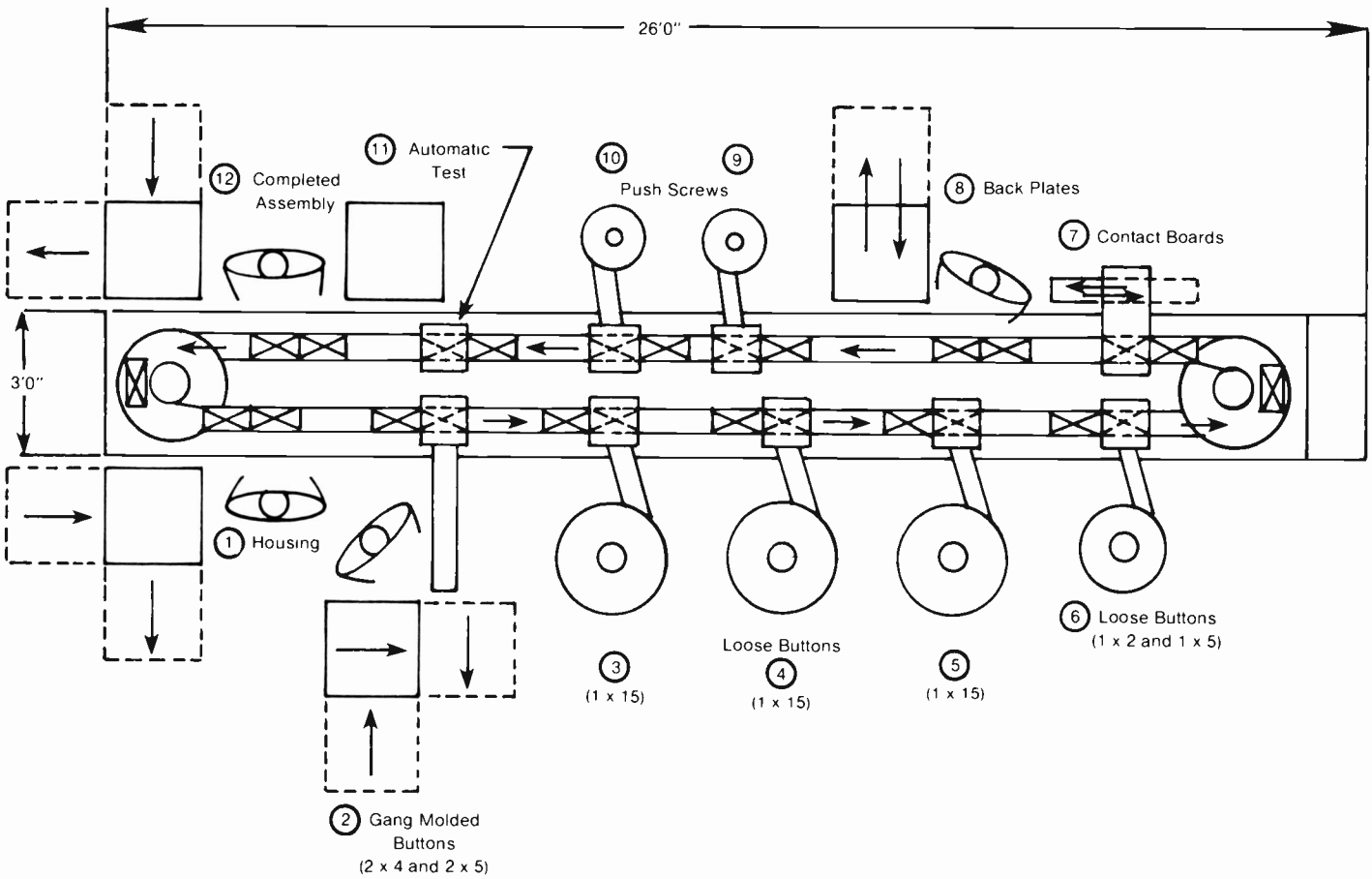

Fig. 6a. *Switch-assembly machine. The floor-plan layout shows the automatic assembly stations intermixed with manual assembly stations.*

Fig. 6b. *This view of the switch-assembly machine shows the actual system under construction. In the foreground are the vibratory feeders for switch components.*

the cabinet before inserting the part directly into the paint mask for spraying. The Mitsubishi robot uses a five-axis capability to eliminate the need for cabinet rotation during spraying.

After spraying, the cabinets are placed onto the main line by a simple indexing-and-cueing conveyor and a pick-and-place device. Thus, the cabinet flow is from the main line to the indexing belt conveyor, then to the parts-handling robot, to spray painting and back onto the main line via the pick-and-place device.

Paint masks must be washed at regular intervals to provide the high quality required in finished trim painting. This is accomplished through the use of a custom-designed automatic mask change and wash/dry system. The mask handler exchanges a clean dry mask for a used mask during the cabinet change cycle. Less than one second per part is lost because of mask changing; this is much faster than the older manual system.

Surface-mounted components

Leadless "chip" components are being introduced to Consumer Electronics by a multi-departmental task force that is led by the MTC Project Engineering group. The introduction of leadless "chip" resistors and capacitors to Consumer Electronics's product line requires close coordination of product design and manufacturing process. The introduction of a new component type also requires the coordination of reliability, safety, and quality testing.

A pilot product was selected to be redesigned and manufactured with leadless "chips." The components were subjected to environmental, safety, and stress testing to qualify their use in Consumer Electronics's products. Simultaneously, an assembly process and requisite equipment were co-developed with outside vendors.

The chip components were bulk shipped from the vendors and assembled to the

copper-track side of the printed circuit boards by use of a fast-drying epoxy cement. The equipment selected to do the assembly is shown in Fig. 5. The epoxy is cured in a low-temperature oven in 3 minutes. Soldering takes place on a wave-soldering machine that has been modified for chip soldering. This soldering process and that of the standard leaded components take place at the same time.

Electronic tuning—Latest challenge for automation

The recent trends in color TV toward electronic tuning have created a need for cost-effective assembly of switches to control these new tuning devices. Each color TV instrument with electronic tuning requires at least 12 switches for customer controls.

Product variety and multiple-switch configurations dictate the need for a flexible, high-speed manufacturing process. The MTC and the Bloomington Instrument Plant proposed and developed an assembly system to meet the need. This machine will be placed into production in 1983. The switch-assembly machine is composed of five major parts (Fig. 6): an asynchronous conveyor with buffer stations between assembly stations, switch-assembly stations (each dedicated to a type of switch assembly), manual assembly stations, an automatic test station, and a programmable controller.

The palletized conveyor features easily replaceable tooling on each pallet. The pallet tooling is dedicated to a specific switch configuration. The assembly stations are dedicated to a specific task needed to assemble each switch type. Some stations are used only when a specific switch configuration is manufactured. Manual stations are provided to handle older products with limited remaining product life. The test station can test all switch types for electrical and mechanical parameters.

The basic design allows for the introduction of future products with a minimum of tooling change and changeover time. This unique combination of manual and automatic stations provides the flexibility of our varied product mix and our low cost of manufacture.

Instrument-line automation

In the manufacturing process for color TV receivers, many final adjustments and tests are performed on the nearly completed instrument. The precision of these final alignment processes is very important to the performance and salability of the end product. Historically, these alignment steps have been performed by production-line operators who have subjectively evaluated picture and audio performance on the various test signals. Because this process is costly and results are variable, it is a natural fit to the MTC charter of exploring new manufacturing methods and automation.

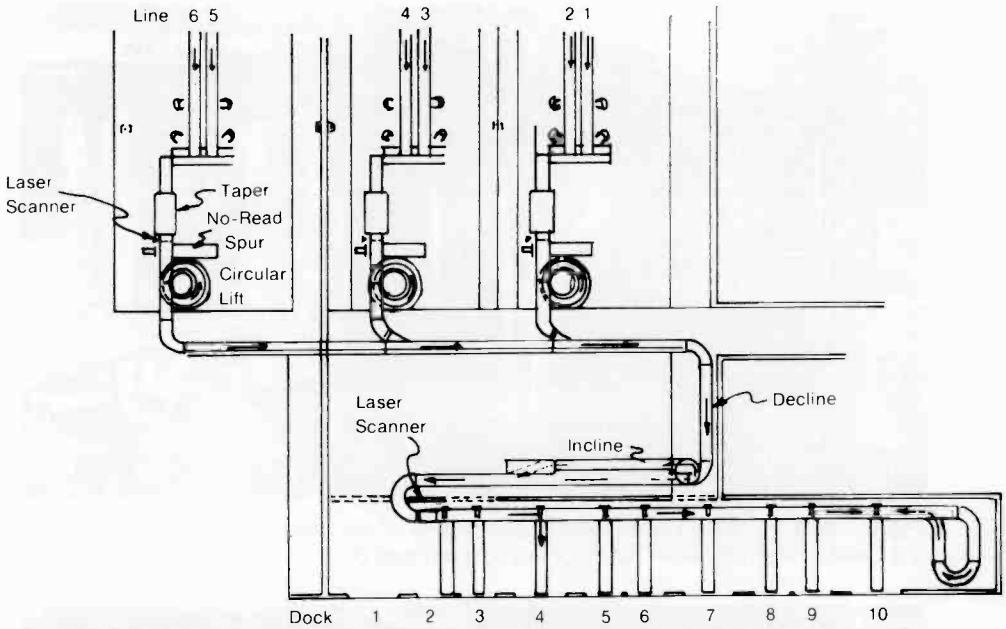

Fig. 7. *This floor-plan layout of the plastics-material-handling system shows the six finishing lines and conveyor in reference to the shipping dock.*

The first phase of the MTC automated instrument line is complete in the form of CAPAS (**C**onvergence **A**nd **P**urity **A**lignment **S**ystem). This system combines the functions of four production operations into one microprocessor-driven machine. In its center convergence mode, CAPAS generates a white crosshatched pattern on the receiver screen, optically examines the coincidence of the red, green, and blue components of the pattern, and computes the magnitude and type of current pulses necessary to custom magnetize a ferrite strip on the picture-tube neck to correct any errors. In its purity mode, CAPAS generates a flat green pattern, optically examines this pattern for maximum tolerance from any red and blue content in the picture, and makes corrections by physically moving the picture tube's deflection yoke and by making further magnetic adjustments to the ferrite strip.

The present CAPAS machine uses one operator to install the servo drive/magnetizer fixture on the picture tube. Efforts are underway to robotize that operation and to add two more axes of yoke manipulation that will affect edge-convergence adjustment. The CAPAS system provides a substantial labor and cost saving with a new measure of instrument-alignment consistency. CAPAS is currently in use on 110-degree instrument production.

Material handling—Total planning

The plastics material-handling system is a project that promotes the synchronization and smooth operation of the equipment, labor, and information components of a manufacturing and shipping system. It is an integrated material-handling system rather than just islands of automation gathered together. Portable plastic TV cabinets are packed into individual cartons. These are sealed and conveyed to the shipping dock and into waiting trailers (Fig. 7).

The flexibility, integration, and control are maintained by laser scanners that mechanically identify the cartons and by microprocessors that track and direct the contents to their destination. The system provides packing stations on six finishing lines. Operators place the cabinets into individual cartons and release them to the conveyor. Three random case sealers close, seal, and date code the cartons. Laser scanners identify the product through a bar-code label located on the side of the carton. Photoelectric "eyes" confirm flap sealing. If the carton identification or sealing is irregular, the carton is diverted to the no-read spur for repair. Otherwise, the carton travels up the circular lift to the transport conveyor (Fig. 8). Traffic "cops" direct the

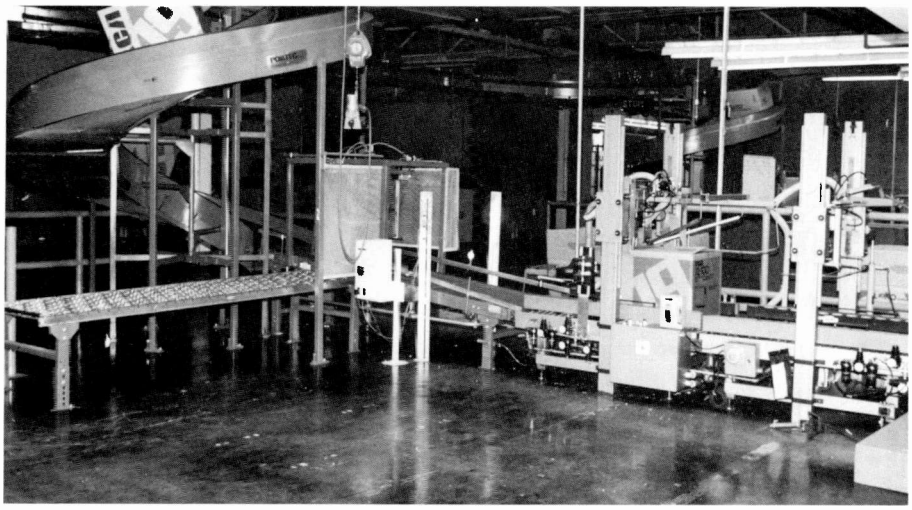

Fig. 8. *Packing area. The individual packaging of the plastic cabinet is released to the case sealer, identified, and conveyed overhead on its way to the dock.*

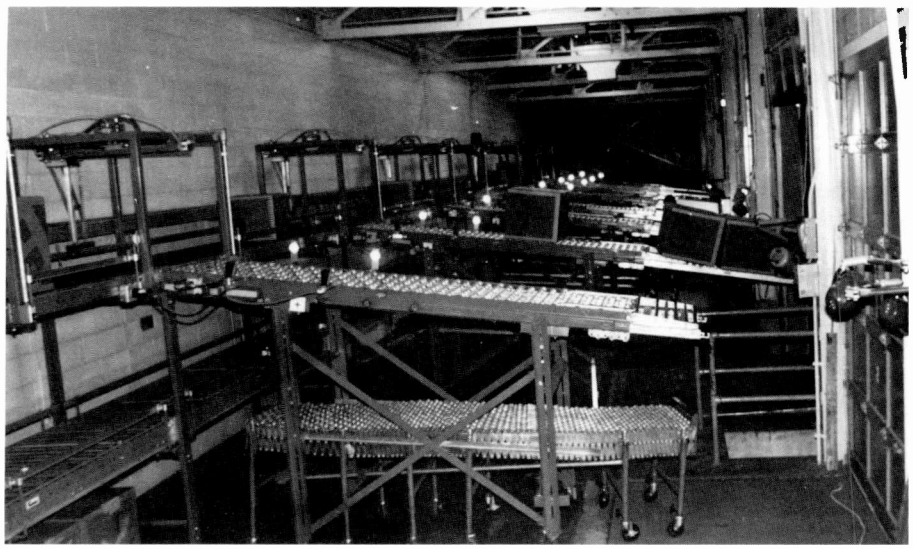

Fig. 9. *Dock area. The cartons are identified and tracked to the proper diverter. Each carton is automatically diverted into the proper trailer for loading.*

product from the three circular lifts as they travel along the single conveyor for transport to the dock.

As the cartons enter the dock area, they are identified again by laser scanner and tracked by photoelectric eyes as they travel along a 100-foot-long belt conveyor. When the cartons reach their preselected dock, they are diverted into the trailer (Fig. 9). When a carton cannot be diverted, it travels back into the production area and automatically re-enters the system. Operators load the trailers manually to make maximum use of the trailer capacity.

The current production count is displayed over each finishing line on an automatic display board. The production count, conveyor inventory, and individual trailer inventory are also displayed on any of three CRT terminals. These are located on the production floor, on the shipping dock, and in the shipping office. Printers are activated to produce copies of any information generated. This installation has totally eliminated lift-truck handling of finished cabinets.

Statistical production engineering

RCA Laboratories and MTC introduced statistical production engineering to printed-board manufacturing at the Indianapolis Components Plant. The printed-board manufacturing process is a mature technology that produces satisfactory yields at acceptable costs. This project started in October 1982. It encompasses only the solder-resist silk-screening process and will be expanded later to involve other areas of printed-board manufacture.

The major element of statistical production engineering is a knowledge of the process capability. This was learned by instituting a regular process-control audit (actual measurement of units from the screening machines). These data were charted and process control limits were established. The knowledge of actual process variations allows the application of scientific methods to process maintenance. Process-correction procedures were developed and instituted. Controlled experiments could then be conducted with repeatable results. This program has reduced scrap loss by 2 percent to date. It also has been possible to reduce in-process inspection for screening operations by 50 percent without a loss in product quality.

Scientific method for manufacture

Today's complex electronic products require equally complex manufacturing processes. This complexity requires the application of organized methods for controlling the manufacturing plant. Analysis and control of the manufacturing process requires the application of scientific methods to provide the answers that lead to higher yields and greater efficiency.

The use of the scientific method in the manufacturing process is exemplified by the soldering-improvement program at Consumer Electronics. The MTC was given the responsibility for improving soldering throughout the Consumer Electronics Division. MTC members traveled to Juarez to observe the production process and to analyze the soldering defects. The critical set-up parameters of the soldering equipment were also recorded (flux density, solder-wave temperature, conveyor speed, preheat temperature, and wave height).

This strong base of acquired production data supported the next step during which MTC members varied the soldering parameters in a controlled manner. Experiments were conducted on the assembly line; only one set-up parameter at a time was changed. Each experiment included a control sample to guarantee the validity of the test results. This control sample was a critical step in the experimental design since the true cause of soldering defects was not known. This method of analysis led to the identification of three areas for process improvement: product design, printed-board manufacturing process, and soldering equipment. The recorded improvements in soldering during this program have shown more than a tenfold reduction in soldering defects.

The future

To meet competition and to supply consumers with the latest products at the lowest cost, producers must use the latest in manufacturing technology. The MTC has proved to be a valuable asset in improving our manufacturing competitiveness. The effective use of this resource in conjunction with the expertise in our plants will help us maintain our leadership in the consumer-electronics market.

Authors McCorkle (left) and Stephens. Limberg was unavailable for photo.

Chuck Limberg joined RCA Consumer Electronics Division in 1979. Before joining RCA, he spent 10 years in various manufacturing management assignments. He was Manager of the Manufacturing Technology Center until he left RCA in April 1983. For further article information, contact one of the other authors.

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B.J. Matulis

Intracorporate technology transfer—Theories and practice

Research and Development managers have a fundamental responsibility to ensure that new ideas developed in the laboratory are transferred to products in the field.

Technology in one form or another has been with us for thousands of years. "Technology transfer," on the other hand, is a recently minted expression that acknowledges the explosion of technological change that has become an accepted fact of life during the past 20 years.

The popularity of technology transfer as a subject for scrutiny and dissection in the technical literature is eminently understandable—it is important. Indeed, it is the enabling force behind much of the world's commerce. And nowhere is it more prominent than in the area of national defense, where a single technological innovation can literally alter the real or perceived strength of a nation and have an equally significant impact on the economy. Understandably, then, the defense industry is weighted heavily toward technology, and, indeed, is supported in this approach by a number of government technology laboratories. It is the depth and the quality of Research and Development (R&D) that frequently determine the success, and even the survival, of defense contractors.

Government Systems Division, a typical defense/aerospace contractor, depends for its long-term research needs on the RCA Laboratories. For shorter development cycles (three to five years) the Division maintains a small R&D arm, the Advanced Technology Laboratories, which works closely with the business units on new technology applications. The Missile and Surface Radar (MSR) Engineering Department at Moorestown includes several advanced technology groups that concentrate on developments with cycles of two to three years.

This hierarchical approach to technology development is designed to maintain a high level of technology awareness in all the organizations and to assure meaningful support of the technological needs of the operating units.

Figure 1 depicts the interrelationships of these technology-oriented functions, and also includes another group of special interest to MSR: the Solid State Technology Center, the Solid State Division's R&D branch.

This paper addresses some of the problems of technology transfer in the context of the organizational structure outlined above. A generalized definition of technology transfer is given, with a model that indicates how critical elements interact to affect the outcome of the process. A summary of management approaches follows. This is a practical methodology for technology transfer as practiced in MSR.

Technology transfer defined

The popularity of technology transfer as an engineering management topic in recent years is reflected in the number of definitions advanced for the process. Indeed, one recent paper cited four distinctly different definitions in use at the same time within the federal government.[1] Golden[2]

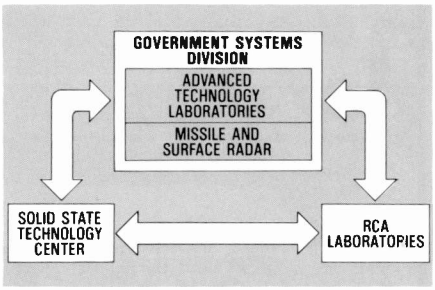

Fig. 1. *RCA Government Systems Division technology organization, with interfaces to corporate laboratories.*

This article is adapted from the author's paper "From the Laboratory to Product Design," published in the 1981 IEEE Engineering Management Conference *Record*, November 1981; copyright 1981 by the Institute of Electrical and Electronics Engineers, Inc.

Abstract: *Typical problems of product development are complicated by the growing need for implanting new and complex technologies during the development cycle. In practice, this becomes a matter of inserting new technology into a design—technology developed in independent laboratories that are often geographically (and almost always philosophically) separated from the design and development team. This paper provides a generalized definition for technology transfer, and a model to indicate how critical elements of the process interact. A summary of management approaches forms a body of practical methodology for the transfer process.*

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may come closest to the mark in his characterization of the transfer process as one that is so complex it almost defies description. In the context of this paper, technology transfer is defined simply as "the act of conveying a new method, process, or technique for solving a specific technical problem from one person or organization to another."

Modeling the process

A time-level mathematical model proposed by Nawaz Sharif and Haq[3] is structured with a level of complexity sufficient for detailed analysis. White's transfer schematic[4] features practical aspects of the process, given in considerable detail to permit inspection of the complex interactions. The model presented here, on the other hand, is a relatively simple one designed to show graphically the broad interaction of donor and receiver interest, the technology gap, and the period of donor-receiver overlap. The model was developed from our experience and observations in mechanical device development, data and signal processing, system and operational analysis, and computer programming, but is not limited to these disciplines. The model is shown in Fig. 2.

As with any analog signal, the concern with both amplitude and phase is critical. Some of the significant terms used in the model are:

- Interest—the product of effort expended in the area involved and an ingredient called "sponsorship." Sponsorship is the measure of organizational enthusiasm for the technology.
- Interest peak—the point where a shift to a "better way" occurs.
- Technology gap—the measure of time it will take for the interest of the receiver to reach the level necessary for effective transfer.
- Overlap period—the measure of the length of time after transfer that donor interest level must be maintained.
- Transfer point—the point in time when primary responsibility for the technology ownership is perceived by donor, receiver, and management to shift from donor to receiver.

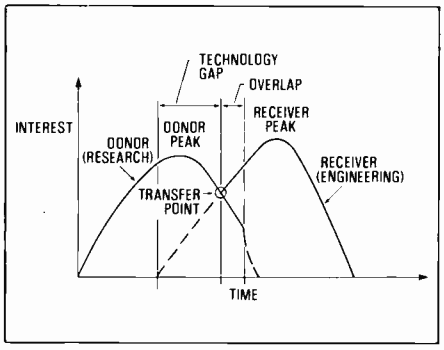

Fig. 2. *Basic technology transfer model, showing roles of donor and receiver. Note that receiver peak is often, but not necessarily, greater than donor peak.*

In general, the terms and the model show the following characteristics:

1. An obvious condition is that both a donor and a receiver exist.
2. Interest by the donor will always peak, because something more interesting will always develop.
3. A technology gap will exist between donor and receiver.
4. An overlap must exist between donor and receiver for optimum transfer.

Let us examine these characteristics as they affect management. First the obvious condition—both a donor and a receiver must exist. Although this may seem trivial, many research programs are undertaken with little or no visibility of where, or to whom, the transfer will take place. This is acceptable in pure research, where the fundamental requirement is a search for knowledge. There have even been examples of efforts begun as research and carried through to product by the original researchers, but these are exceptions.

Clearly, however, when the effort is directed to a particular problem by using a new method, technique, or process, then a receivership must be determined. In government programs, technology transfer is usually a requirement that is induced by the structure of the procurement process, where sponsorship of technology development lies in government laboratories.

Donor visibility of the actual transfer point is not necessary at the beginning of a project, and in fact would probably impede donor creativity and innovation. Figure 3 illustrates the impact on the basic model when the transfer is forced before the donor's peak interest point is reached. The technology will be perceived as not being ready and the receiver will not be encouraged to proceed. Thus, both donor and receiver interest in the technology will drop and delays will be encountered in product development. If the technology is good enough the delay may not be fatal to the project, but the competitive advantages may be lost.

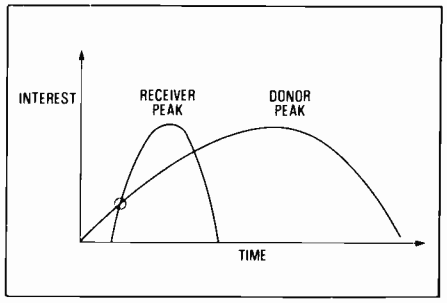

Fig. 3. *Early transfer, before donor peak interest is reached. Reaction to "premature" transfer will cause a drop in both donor and receiver interest.*

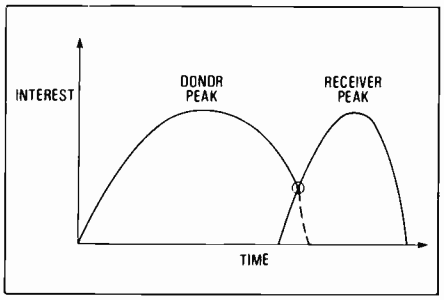

Fig. 4. *Late transfer, well beyond donor interest peak. Effect is often diversion of donor's effort to a "better way."*

Figure 4 shows a case in which the transfer occurs well beyond the donor's interest peak. If the donor's efforts are diverted to a "better-way" solution, serious delays may again be expected in getting the technology into the product. In this case the delay will almost always be fatal to the technology since the "better way" will gain more and more interest and will be very diffcult to overcome.

It should be noted that the interest level of the receiver is not limited to the peak magnitude of the donor. In fact, the receiver will often have more interest (effort and sponsorship) in a technology than will the original developer. If the receiver does not show at least a sustaining interest level at the transfer point, understanding will be impaired and the required enthusiasm to keep the effort going may well vanish.

What is necessary in this process is management realization that research cannot stay in the lab forever, that there are overall economic timetables to be met, and that a transfer plan is necessary. Without a plan, technology development tends to stretch out and will usually be overtaken by "better" technology. This is not to say that one can predict the time it takes to develop technology and make a timetable for transfer. It does imply periodic evaluation of the worth of a technology to the problem at hand.

The second characteristic deals with matching the interest levels of the donor and receiver. To make the transfer effective, management should ideally arrange the transfer at a time when the donor's interest is peaking and the receiver's interest level is at or above that of the donor. This means that a certain compatibility must exist between donor and receiver.

From experience we have found that transfer requires things, people, and attitude. The transfer can take place effectively only when the receiver has a positive attitude about the technology. The receiver must have a certain level of understanding and believe that the technology will provide a superior solution to this problem. Usually receivers exhibit a high level of enthusiasm when they are ready to accept ownership.

This brings us to the third characteristic that must be considered and managed—the technology gap. This is a measure of the ability of the receiver to accept the responsibility of proceeding with the technology development. In the model presented here, the technology gap is the measure of time between interest levels. What this means is that for effective planning one must know how long it will take for the receiver to reach the level of interest necessary for effective transfer. There are several implications here: Where will the technology be at the transfer point? What effort and sponsorship must be provided to ensure the receiver is ready? (Will the right people be available? Will the physical facilities be emplaced? What controls will be necessary?) How much time is needed to get there?

In government work the existence of a contract with firm delivery dates often provides the stimulus necessary for considering these issues. But consideration alone does not ensure project success, and often the delays on high technology contracts can be traced to underestimation of the technology gap. The program manager must look for the gap and manage its size. The fact that a new device or procedure has been available in the lab for a period of time and may be near its peak interest point does not necessarily mean that the engineering development team is ready to pick it up and run with it. We must measure the technology gap and then allow sufficient time to permit the growth of adequate interest levels.

The fourth characteristic for management consideration is the overlap period. This is the period during which the donor must maintain an interest in the technology after transfer of ownership has taken place. Overlap is required to either support the receiver, to continue to defend the technology, or to expand it. This is often a trying period for management, since the interest of the donor is usually dropping off sharply. Once the ownership transfer is perceived to have occurred, the donor is redirecting his interests in "better" directions. Unfortunately the "better way" is frequently not a new version of the recent effort, but a completely new approach. It is incumbent upon the management to plan for overlap programs to ensure program success.

Practical transfer methodology

The brief discussion of a transfer model illuminates some of the problems inherent in the transfer process. Our experience with technology transfer in the Engineering Department at MSR has been based largely on necessity, with new technology providing the leverage and our military customers providing the driving force by constantly increasing equipment performance requirements. Our early approaches to the process were based largely on classical management techniques, with relatively little conscious recognition of the special demands of technology transfer. With each project, however, we gained valuable experience, and it is noteworthy that our basic approaches today track closely with the general implementation theories from the literature. This section addresses a number of practices we have applied in MSR to make technology transfer work on a practical basis.

Organization structure

First, and probably most important, we attempt to use the organization structure to control and sustain the interest levels, technology gaps, and overlaps. As shown in Fig. 1, the hierarchy devoted to technology development is well suited to the mechanics of technology transfer. By carefully assigning complementary efforts in the various related groups, we have been able to draw effectively on the skills in each center to achieve technological innovation in our products.

Within each functional section of the Engineering Department we have established an advanced technology group whose function is to develop new and replacement products. (These were recently formed from a single Systems and Advanced Technology organization that provided this function in all technologies of interest.) These groups are the receiving organizations for technology from outside our business unit; they also serve as donor groups for the internal transfer of technology.

By establishing these groups as separate entities we have a mechanism to increase interest levels within the organization, a resource to develop talent without the pressure of demanding product schedules, and a place to collect the highest level of expertise possible and make this expertise available when it is needed. We have found this organizational scheme makes the transfer easier, keeps our technology gap manageable, provides a place for overlap operations after transfers take place, and promotes creativity and innovation.

The role of this organizational structure can be best understood by an example. In the late 1970s, the MSR Systems and Advanced Technology group began a project on the use and impact of Very Large Scale Integrated (VLSI) circuits within the AN/SPY-1 Radar. This radar, which is a fundamental part of the Navy's AEGIS Weapon System, was already designed and being successfully tested by the Navy when the study of VLSI impact was started. We realized that the insertion of VLSI into the sophisticated real-time signal processor held the potential for significant (more than 2 to 1) weight and volume savings, for improved performance, and for reduced costs. Incorporation of VLSI into the design was a joint venture involving the Advanced Technology Laboratories (which was leading the way in VLSI circuit designs), the Solid State Technology Center (which was developing VLSI devices), and the MSR Systems and Advanced Technology group.

At the beginning of the project the MSR technology team filled the role of technology receiver. They developed interest within MSR while closing the technology gap. This transfer took two years, and the role of receiver changed to the role of donor when the internal handover was made to equipment designers. The new system is currently in the final product-design stage and initial testing of the advanced system components indicates that performance, size, and cost achievements meet our predictions.

This type of organizational structure is not without pitfalls. Since the advanced technology organizations are not self-sufficient in regard to support services (drafting, mechanical engineering, prototype shop facilities, and so on), they must compete for these services with the product groups. This competition, if improperly managed, can impede the technology transfer.

Another problem is that of maintaining

motivation in the product group. The perception that all the "good work" goes to the advanced technology groups and that they appear to have different management standards makes the product manager's job difficult. To overcome these shortcomings we have recently divided our single Systems and Advanced Technology group into several sections. The functional technology expertise has been distributed with the applications managers to facilitate more effective technology transfers. Early indications show that this approach is working to sensitize our management to the process.

A second practice we have adopted deals with the mechanics of transfer—how the people are assigned. The importance of this subject is obvious from the attention it typically receives in the literature.[5,6]

As have others, we have found that the most effective method of technology transfer is through the mechanism of transferring people with the technology. In fact, a fundamental policy of the Advanced Technology Laboratories is to move at least 5 percent of the staff each year into the business units. This provides for dissemination of technical information and gives the individuals an opportunity to get first-hand experience with the problems faced by the product developers. A recent example of this process is the transfer of a number of ATL engineers to MSR, where their knowledge and expertise in computer technology are key elements in our successful Advanced Development models for the Army's Military Computer Family program.

Another method used to aid in the transfer process is to assign a small cadre of engineers (often only two or three) from one of our advanced technology groups to live with and work with their counterparts in the Advanced Technology Laboratories on the preliminary design effort. When the project is transferred back to MSR, our engineers come with it and stay with the project through the middle stages of final product design. The individuals themselves then experience the change of role from receiver to donor.

The advantages of this approach from the standpoint of continuity of effort are obvious. The transfer process is accomplished without major snags or dislocations, and the management of transfer points and overlaps is simplified. One drawback, of course, is the talent drain in the sponsoring organization. We have found that a great deal of extra care in personnel planning is necessary to maintain the integrity of a technology group when two or three of its members are absent for extended periods. The need for backfilling can become acute at times.

Still another result of this approach can be viewed as a mixed blessing. The long-term exposure to a project is certain to create a sense of identity in the engineers involved. As White[7] has pointed out, a few individuals will choose to remain with the project, more or less permanently. In our experience the loss of one promising engineer from an advanced technology group has been more than offset by his metamorphosis as one of our best young first-level engineering managers in the product design organization.

Parallelism

Parallelism is an approach we are using to minimize the technology gap between the laboratories, our advanced technology groups, and our product design organizations. In essence all groups are heavily engaged in a single effort, interest levels are high, and clearly there is no single ownership of the technology. Data developed in the lab is quickly transferred to the advanced technology group designing a test model. Information gained in the design of the test model is used by the design engineering group responsible for the final design.

The approach was developed more by necessity and coincidence than through formal design. Although the work in each of the three groups appears to be strikingly similar, the goal of each activity is unique. The labs group is providing a generalized methodology, the advanced technology group is defining the limits of feasibility, and the product design group is concentrating on producibility. With three groups working so closely together there is a positive, continuous information flow among them, and the time required for each group to obtain its goals appears to have been reduced.

One specific area where this concentrated effort is being applied is in the design of a superior phased array radar antenna system. The antenna technology involved is not only new but requires a degree of precision in component tolerances that would have been impracticable only a few years ago. This precision is attainable today through the use of computer-aided design and computer-aided manufacturing techniques. The Advanced Antennas and Microwave Technology group in MSR developed the new designs by using techniques developed at the Microwave Technology Center of RCA Laboratories, and then directed the flow to the product group. The transfers were accomplished smoothly, with strong indications that the product will be effectively producible and have superior performance characteristics.

The implementation of this approach is also not without penalty. A degree of duplication of effort and facilities cannot be avoided. For example, the computer facilities at RCA Laboratories have been duplicated at MSR to perform tests. Personnel resources tend to be spread over several tasks, and individual productivity is less than optimum. Overall, however, the product will reach completion much sooner than if the more traditional approach were used, and the sacrifices remain within manageable bounds.

Conclusion

From a management standpoint, a "successful" product is really successful only if it was developed at reasonable cost, without dislocating the structure and effectiveness of the implementing organization. This is especially important—and difficult—in an undertaking as complex as technology transfer, and calls for an extra dimension of management attention in several areas.

One of these is the planning area, which requires special emphasis and structure. In particular, the planning must be specifically oriented to the end product. This must be accomplished in spite of the need to keep the early developers unshackled by design details. The early and thorough definition of interfaces is also vital. The receiver at each stage of the process must be known, and even more important we must clearly identify what he needs. A total, in-depth orientation of all the participants at the beginning of the project is not just good management in technology transfer—it is an absolute must.

A second area of special concern is timing. When to move a project from one stage to the next is, of course, a matter of judgment. Frequently the judgment is exercised by the participants themselves or their managers. These people probably have built up a strong interest in the project, and want to do it right. If they take just a little more time, it will be better in the end. The danger in overriding their decisions lies in moving an early design prematurely, before it is solid. There are no concrete ground rules and very few overt signals that indicate precisely when the time is right to move to the next step. The only surety is that the people who have the project in hand will want to keep it longer than they should.

People transfer is a third area demanding special attention. It is clear that this technique of technology transfer is effective in terms of project success, but carries the seeds of long-term disruption of the organization. Our experience tends to bear out the effectiveness of transferring people with the design. We have no hard evidence to indicate any strong trends in terms of the impact on the donor organization.

The approach of sending people with the technology as it progresses through various design stages forces a consideration of how long they should remain in the new environment. The easy answer is that they stay until the job is done, and then go home. Our experience indicates the importance of establishing some sort of time limit for the transfers, to give the individuals involved a sense of security while retaining the thrust of the project. This area remains one that has more questions than answers.

An attendant problem involves motivation of individuals and groups, especially those who know their work will be taken away and that all further processing will take place at a remote place, by unknown people. Laboratory and advanced technology people have different interests and drives than do product designers. The problem is one of building—and sustaining—a common interest in, and drive for, the end product. This problem, of course, is not so much a mystery as simply an immense, time-consuming task that requires extraordinary skills in the project director.

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S.E. Courcy | G.A. Del Priore

Microprocessor architecture and mass-storage techniques for field-portable automatic test equipment

The newest Simplified Test Equipment for Army vehicles places great demands on memory capacity. Bubble memories will satisfy the unique requirements for this RCA product.

Abstract: *RCA Automated Systems manufactures Simplified Test Equipment (STE) for Army vehicles. Currently, the upgraded STE version, STE-X, features an enhanced microprocessor structure and mass memory-storage system. This system will successfully support current and future vehicles. The processor structure, processor selection, slave processors, mass program storage via bubble memory, bubble heaters, and future possible enhancements are covered.*

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Rugged and sophisticated test sets are required to keep today's Army vehicles, with their complex electronics and propulsion systems, at full combat readiness at all times. In the field or at the organizational support level, RCA's Simplified Test Equipment (STE) family allows quick and accurate isolation of faulty Line Replaceable Units (LRUs) or cables, while minimizing operator-training requirements or manuals.

By employing state-of-the-art microprocessor and memory technology, an extremely powerful automatic test capability has been packaged into a small, portable, rugged automatic test instrument meeting the military's requirements. The basic unit measures 12″x12″x13″, and is shown in Fig. 1. Exclusive of cover and test cables, the unit weighs about 40 lbs. The STE sets

Fig. 1. *Currently, STE-X is undergoing software validation, development, and operational testing at RCA Automated Systems, Burlington, Mass.*

are often used in the harsh "edge-of-battle" environment. The STE design addresses four basic requirements.

1. *Temperature extremes.* The STE must operate over ambient temperatures of −25° to 125°F. Components reach temperatures in excess of 170°F with solar loading of 370 btu/ft^2 at 115°F.
2. *Rain resistance.* The STE must withstand rain up to a rate of 2-in/hr. This rules out vents or fans, which in turn limits power consumption due to limited heat-dissipation capability.
3. *Portable.* Maximum weight for a "one-man-portable" equipment case is 45 pounds. Also, the test set must be small enough to fit through hatches and into tight vehicle compartments.
4. *Rugged.* The STE can withstand a 4-foot drop onto a hard surface, the kind

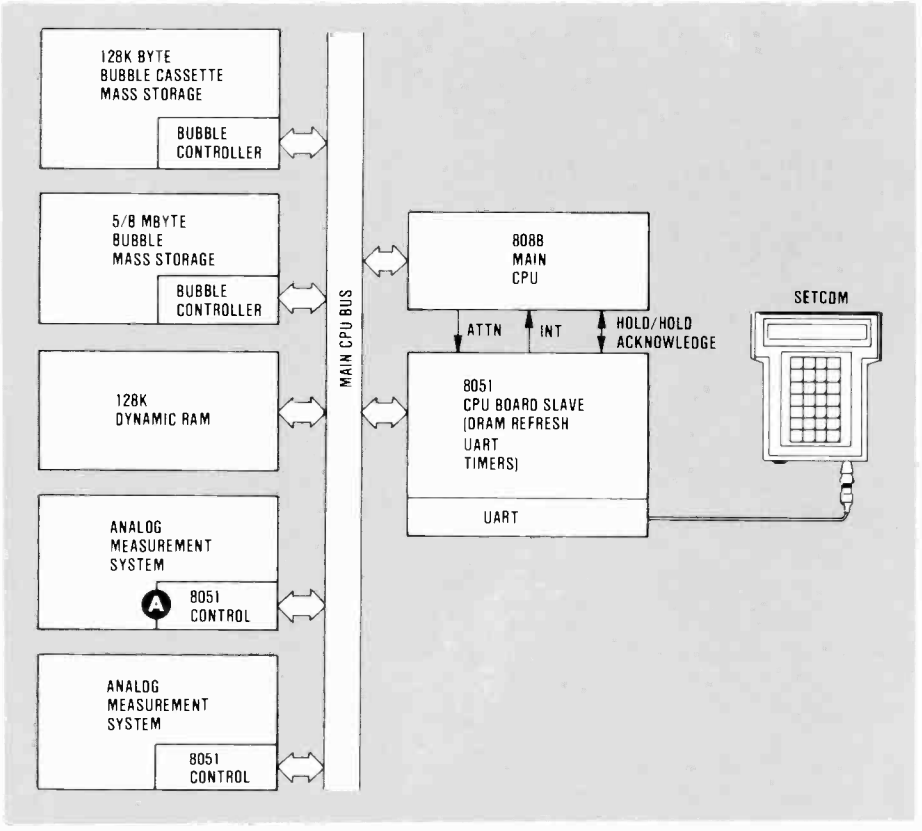


Fig. 2a. *STE-X block diagram. This diagram shows the bus architecture and the interrelationship of the 8088 master CPU and its slaves.*

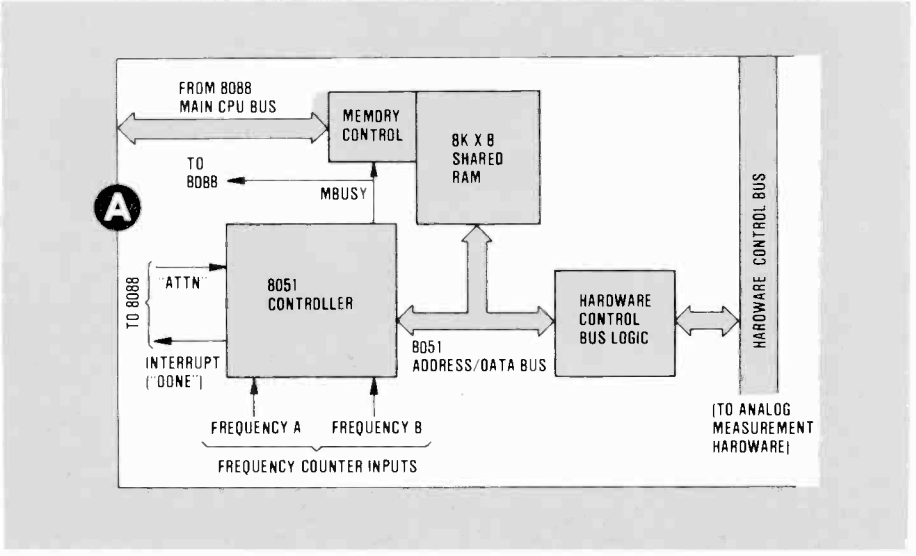


Fig. 2b. *Analog measurement system. This diagram depicts the slave processor, and its communication with the main processor, and communication with analog hardware.*

of rough handling Army mechanics can give their equipment.

This paper describes the microprocessor structure and the mass memory-storage system developed for the latest STE product—the STE-X. Besides the physical constraints, an overriding requirement of the STE-X system was to provide the flexibility and versatility necessary to successfully support current and future vehicles. Therefore, the STE-X must be easily reprogrammable (even in the field), and the system must be reconfigurable to adapt to changing Unit Under Test (UUT) requirements.

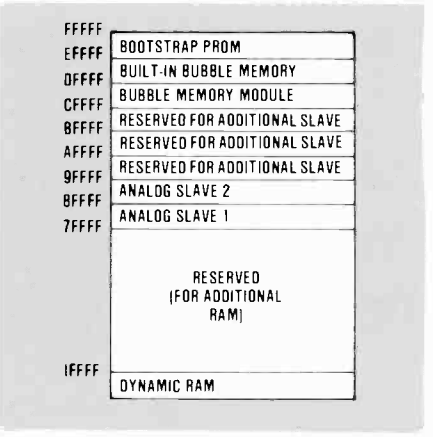


Fig. 3. *Memory-mapped functions for the main CPU. This diagram shows how the main CPU's memory space is used for communication with peripheral functions, as well as the basic program execution.*

STE-X processor structure

Before the STE-X was developed, STE systems were structured around a single 8-bit microprocessor. That central processing unit (CPU) executed all executive software application software routines. Typical tasks included: power-on setup, support of user input/output (I/O), test selection, measurement, and diagnostic decision-making. These activities stretched the performance limits of a single 8-bit CPU and limited the flexibility of the test system. For example, one central CPU was inadequate to generate (with software) a specialized stimulus waveform and to simultaneously analyze a UUT's response.

As the Army expanded the types of vehicles that needed to be tested, the STE system requirements also changed. A large memory capacity, able to support multiple-application software packages that use up to a megabyte of code, was anticipated. Also, the processor architecture had to be able to support a sophisticated file-handling system that facilitated software revisions. A 16-bit master CPU was deemed desirable to meet these memory requirements.

To provide flexibility and expandability, a multiprocessor architecture, as shown in Fig. 2, was employed. This architecture provides more analog measurement capability than a single processor, and provides an interface to a large, highly flexible memory system. In Fig. 2, the 8088 is the main CPU, the 8051s are the support processors, the dynamic random-access memory (DRAM) is the main system memory, and bubble memory provides nonvolatile mass storage of the test programs and operating system.

Bubble memory

Bubble memory is a nonvolatile, solid-state memory device that stores information on a garnet substrate by the presence or absence of a magnetic domain, or bubble.

Positions for these domains are created by permalloy tracks, laid out in the form of loops on the substrate (see Fig. A). The bubbles can be created (generated) or duplicated (replicated) for nondestructive readout by copper gates on the substrate through which a current pulse of appropriate amplitude and shape is passed. The bubbles are moved along the tracks by a rotating magnetic field created by two coils within the device and are maintained by two permanent magnets also within the device.

Detection is accomplished with a magneto-resistive detector, through which the bubbles are passed. To improve device yield, extra storage loops are designed into the device. A map of good loops is stored in the bootstrap loop, and is used by the support circuitry to mask out defective loops.

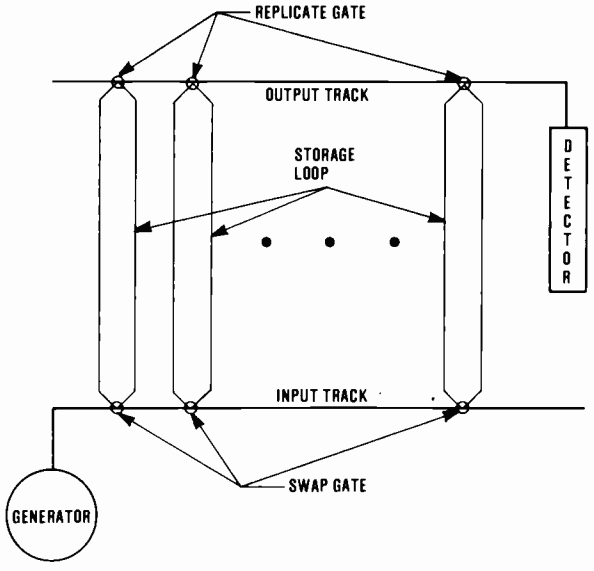


Fig. A. *This is a general description of bubble memory and not necessarily indicative of a particular manufacturer's architecture. Currently, Intel, Motorola, and several Japanese manufacturers produce bubble memory. The Intel product is used in our STE-X.*

Main processor selection

Many parameters were considered in choosing the most powerful and flexible processors consistent with the system power, size, and weight requirements. The main CPU had to have development system support (in-circuit emulators, compilers, linkers, and so on) to provide for hardware and software support and debugging, and high-level language support, to facilitate software development and maintenance. To maximize processing capability and future memory expansion, the use of a 16-bit processor was a design goal. However, initial investigations showed that the power and board space required to support a 16-bit data bus were inconsistent with the size and weight goals of the STE-X system.

As a result, intrasystem communications take place over an 8-bit-wide data bus to minimize board real estate and power consumption. Many 8- and 16-bit processors were considered, but attention was soon focused on the Intel 8088. It has the processing power of an internal 16-bit architecture, including hardware multiply/divide, 1 Mbyte of memory address space, development system support, and a Pascal compiler, yet it functions externally as an 8-bit machine.

The main memory selected for use with the 8088 consists of sixteen 64K $\times$ 1 dynamic RAMs (DRAMs) organized as 128K $\times$ 8. The DRAM was chosen over static devices because it provided the greatest amount of storage per square inch of board space. The 8088's large address space allows access of its peripherals as memory. By decoding the upper four address lines, the 8088's memory is partitioned into sixteen 64-kbyte blocks, which are assigned as in Fig. 3.

The 8088 can operate in two basic modes: maximum mode and minimum mode. Maximum mode is designed for very large, powerful systems with multiple masters and slaves. Although this is the most flexible and powerful configuration of the processor, it is also the most costly in terms of parts and space. Minimum mode, designed for simpler systems, is used in the STE-X; the mode provides sufficient versatility for the system while minimizing the parts requirements.

The executive system software for this test set is written in a high-level language, Pascal. High-level language programming provides the advantages of easier design, coding, debugging and maintenance of software than assembly language. However, high-level language programs tend to be larger and slower than well-coded assembly language programs, and prevent the programmer from directly using many processor resources. For example, initializing a block of memory (for "canned messages") is very simple and direct in assembly language (using a "Define Byte" directive), but would require a series of assignment statements (which generate "move-immediate" instructions) requiring several times the memory of the assembly language.

The Intel Pascal compiler has provisions for combining Pascal and assembly programs together. For example, certain hardware drivers that were space limited because they were to be located in an 8K bootstrap programmable read-only memory (PROM), also required direct use of many processor resources. These drivers were coded in assembly language, yet they are called by the Pascal executive software, thus combining the best features of both languages.

Slave processors

The 8088 in this system needed several support functions. Among these functions were the following: (1) Dynamic RAM refresh; (2) Three interval timers; (3) Free-running "time-of-day" timing; (4) Programmable Universal Asynchronous Receiver Transmitter (UART); and (5) Interface to analog measurement systems. Instead of implementing these functions with standard LSI (for example, a UART, timer, DRAM conroller, and so on), three single-chip microcomputers (Intel's 8051) were used to pro-

vide greater flexibility. The 8051 microcomputer chip contains a CPU (with hardware multiply/divide), 128 bytes of RAM (16 bytes of which are individually bit addressable), 4 kbytes of ROM (for program storage), two timer/counters, interrupt system, latched I/O pins (capable of both driving and sensing), and variable-baud UART.

In the STE-X architecture, the 8088 is directly supported by a slave processor. This 8051 accesses the same memory space as the 8088. It has provisions for accessing external memory (up to 64K). In addition, four I/O pins on the 8051 are used to provide the upper-order-address lines of the 20-bit address space of the 8088.

The "on-board slave," as it is referred to, accesses this memory via the multiprocessor channel on the 8088. This is accomplished by connecting two of the 8051 I/O pins to the hold/hold acknowledge pins through suitable synchronizing logic. The 8051 can access the shared RAM by asserting the 8088's hold pin, forcing the 8088 to release the bus at the beginning of its next cycle. The 8088 acknowledges this through its hold-acknowledge pin that, when asserted, informs the 8051 it can use the memory. Upon completion of its memory use, the 8051 returns control to the 8088 by de-asserting the hold line. This communication method is quite efficient in terms of both software and hardware resources. The synchronizing logic is little more than a flip-flop and the software bus access and release sequences are only a few bytes long.

All communications between the 8088 and 8051 are accomplished via an area of the main (8088) RAM reserved for this purpose. The communications commence when the 8088 places a command code and parameters into the reserved area, sets a handshake flag, also in this area, and activates an I/O port, setting a "command-pending" flip-flop sensed by the 8051. The 8051 then takes control of the memory, performs its function, updates its status words in the main RAM, clears the flip-flop, and releases the memory. Because the 8088 is locked during this operation, this action is totally transparent to the 8088, with the exception that 8088 software will take longer to execute in real-time compared to normally predicted instruction-execution times.

The 8051, in addition to providing slave functions as previously described, is in charge of the DRAM refresh operation. The 8051 has no provisions for operation with a conventional DRAM controller; it assumes its memory is always available. The basic refresh timer is one of the internal timer/counters in the 8051, set to give an interrupt every 250 μs. This interrupt forces the 8051 into its refresh routine, where it takes control of memory, places an address on the bus, and enables the external refresh circuitry, which refreshes

Table I. *Frequency counter specifications.*

Functions	Period A, Period B, Frequency A, Frequency B, Time Interval B is high, Time Interval, A to B (or B to A) Period A, Period B must measure period continuously, and must be capable of measuring at the same time.
Accuracy	Period AB; Accuracy $\approx\pm5$ μs, 1 channel, $\approx\pm20$ μs, 2 channel, resolution (1 or 2 channels) = 1 μs
Range	<20 μs to >16 s
Frequency	(Using 1-second gate) Gate accuracy ±5 μs Signal minimum high time, minimum low time = 1 μs
Maximum input frequency	Channel A = 500 kHz, square wave Channel B > 20 kHz, software determined
Time interval B high	
	Accuracy/resolution: 1 μs
	Range: 1 μs to 16 s
Time interval, A to B	
	Minimum pulse width, A, or B: 1 μs
	Accuracy: $\approx\pm5$ μs
	Range: <20 μs to >16 s

Table II. *Timer/counter setup for frequency counter.*

Function	*Timer 0 mode*	*Timer 1 mode*	*Timer 0 interrupt function*	*Timer 1 interrupt function*	*Interrupt 0 interrupt function*	
Frequency	16-bit, external clock	16-bit, internal clock	Software extended timer 0 to 24 bits	Count off gate	Count pulse on channel channel B	
Period	8-bit auto-reload, reload value = FF,external clock (used as interrupt generator	16-bit, internal clock, free-running	Read time on timer, 1 at 1st & pulse subtract for period on channel A	Software extended timer 1 to 24 bits	Same as timer 0 interrupt except for channel B	*Comments:* Enables continuous period measurement
Time interval B is high	16-bit internal clock, gated by INT0	Not used	Software extended timer 0 to 24 bits	Not used	Stop measurement	
Time interval A to B	8-bit auto-reload reload value = FF, external clock (used as interrupt generator)	16-bit internal clock	Start timer 1	Software extended timer 1 to 24 bits	Stop timer 1, end measurement	*Comments:* Reverse functions of timer 0 and interrupt 0 interrupts to get time interval, B to A

one-sixteenth of the DRAM. The net result is that the entire RAM is refreshed every four ms, meeting the RAM specifications. In addition, this method of RAM refresh provides very high performance, actually providing a higher percentage of memory-available time to the 8088 than some of the commercially available DRAM controllers, due to the elimination of DRAM-controller-generated wait states. This internal interrupt serves a second function. The interrupt routine divides it down to a 1-ms "tick" that is used as the time base for the 8051 timing. Consolidation of the DRAM-controller, UART, and timer functions saves power and increases performance and flexibility without sacrificing valuable board space.

The Intel 8051 contains a built-in UART function. It is a true hardware full-duplex UART with programmable baud rate, programmable number of stop bits, and numerous other functions. The baud rate is generated by dividing down either the 8051 processor clock or an external clock. The 8051 accomplishes this by use of the overflow from its second timer/counter, which can be set up as a programmable divide-by-N (N up to 256) counter. By suitable choice of clock rate, any desired baud rate may be generated. For example, a processor clock of 6.144 MHz will yield 4800, 2400, 1200, 600, 300, and 150 baud exactly, and will yield 110 baud within one percent. This inherent 8051 feature was used to eliminate the need for a separate UART chip and baud rate generator, saving board space.

To meet the fifth support function required by the 8088, control of the analog measurement systems, two additional 8051 slave processors are used. Unlike the slave described previously, which has access to the entire 8088 memory space, these slaves access only 8 kbytes of local RAM. This local RAM is accessible by the 8088 as well. One of the 8051 I/O pins is used to control which processor has access to this local memory. The 8088 uses an I/O port to generate an interrupt to the slave, thereby indicating it wants memory access. The slave grants this access and waits for the interrupt to occur again, indicating the master is done. At this point, the slave reads a control byte indicating what it should do (run program, do nothing, abort program), and performs the operation. Upon completion, the slave activates an interrupt to the 8088, informing it that the task is done. This structure is flexible enough to allow the master to download complex programs to the slave (for example, a "small" Fast Fourier Transform (FFT)) and the slave will perform it with little or no intervention on the part of the master.

One advantage of the 8051 as a slave in this application is its flexibility. For example, the 8051's crystal-controlled clock, the timer counters, and an interrupt line can be used to implement a two-channel, multifunction frequency counter. The result is a flexible, powerful frequency counter (see specifications, Table I) that, although lacking the range and accuracy of a dedicated hardware counter, provides far more than enough range and accuracy for automotive troubleshooting. All of this is done with little more hardware than the microprocessor itself, saving valuable board space and power.

Table II lists the counter functions and timer/counter setups for each. It should be apparent from this table that some software (around 500 to 1000 bytes) is still required, but the demands are less than those for implementing the entire counter in software. The analog hardware is controlled by a low-speed bus derived off the 8051 external data bus. This allows the analog hardware to be controlled by low-speed 4000-series CMOS logic.

In any microprocessor system, a certain amount of small-scale integrated and medium-scale integrated logic is needed to fit the various parts of the system together. This would include such functions as address, decoding, bus buffering, and I/O generation. Instead of the low-power Schottky transistor-transistor logic (LSTTL) devices traditionally used in this application, a new breed of CMOS (RCA's 74HC and 74HCT series high-speed CMOS) was used extensively. This logic has a switching speed that compares with LSTTL and has the low-power consumption of CMOS, a combination that is very useful in a high-speed system where power is critical.

Mass program storage

The mission of STE-X is to provide multi-vehicle, multi-system support. This places substantial demands on memory capacity. For example, present estimates of the memory required for the operating system and the M1 and BFVS application software exceed 500 kbytes. Plus, the memory media chosen ideally would meet all environmental requirements and would be reprogrammable without disassembly of the test system.

Most commercial mass storage, such as Winchester disks, floppy disks, cassette tapes, or strip cards, were considered to be too fragile to withstand the STE-X environment. Attention was, therefore, focused on solid-state memories, in particular the magnetic bubble. ROMs and electrically programmable ROMs (EPROMs) could not be used (because of lack of reprogrammability without system disassembly), and bubbles had a decisive advantage over electrically alterable memories such as EAROMs and EEROMs because bubbles have higher density. With current state-of-the-art EEROM chips (16K bit), about three times more board area would be required to replace an equivalent amount of bubble memory and its support circuitry. The bubble memory is supported as a system by its manufacturer (Intel) with a complete set of LSI support circuits (controller, coil drivers, function current generator, sense amp, and so on) that free the user from the details of driving the bubble memory.

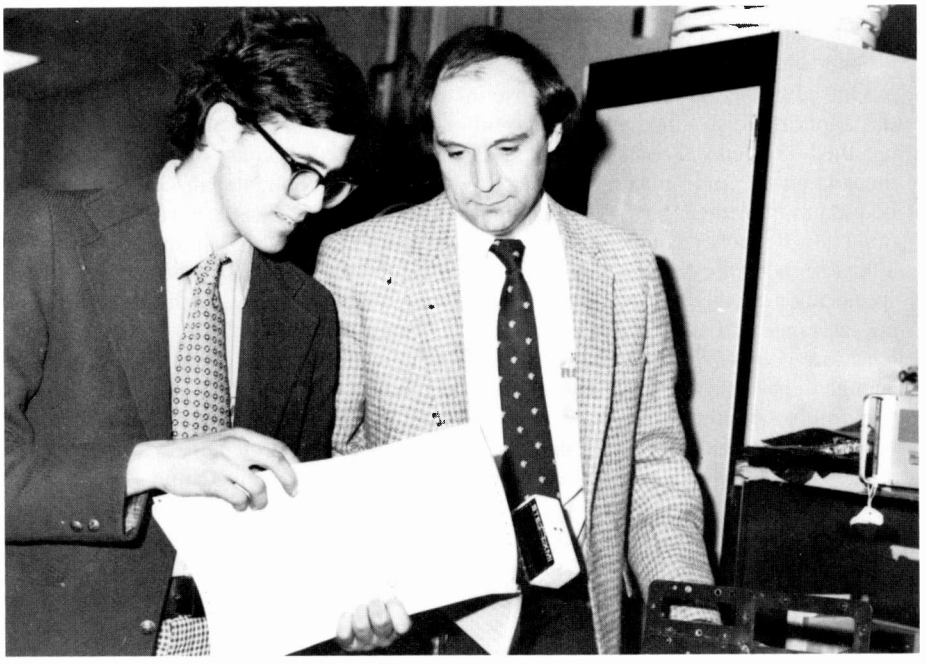
Unlike the electrically reprogrammable ROMs, however, software cannot be directly executed from bubble memory, because bubble memory is a sequential access memory, with data stored in a series of loops, somewhat analogous to the tracks on disk. The relatively long access time (about 40 ms on the average) is not a serious disadvantage, because all 500 kbytes of software need not be available simultaneously. To hold the software that is to be executed, 128 kbytes of DRAM are provided. If different software needs to be run, it is loaded into the RAM from the bubble.

Bubble heaters

Bubble memory currently has a low-end temperature range insufficient to meet STE-X environmental requirements. The main problem appears to be within the bubble-memory unit itself. A bubble-memory unit is not a "chip" in the sense of a conventional IC, but an assembly consisting of the bubble substrate and die surrounded by drive coils and bias magnets. Each one of these component parts of the bubble memory has its own characteristic, and a different variation of these characteristics with temperature.

Because of this, bubble memory has two temperature specifications—a nonvolatile storage temperature and an operating temperature. The nonvolatile storage specification is determined by the tracking between the bubble die and bias magnets. This temperature (available to −55°C) meets the STE-X requirements.

The bubble memory operating temperature specification (−20°C) currently is in-



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adequate for the STE-X. There exist two possible methods to extend this range. The first method is to temperature compensate the various drive signals to the memory to account for the changes in bubble characteristics over temperature. This approach, however, requires considerable circuitry and extensive knowledge of bubble characteristics. It would also require extensive (and expensive) qualification to produce a manufacturable design.

The second approach, and the one currently under investigation, is to use a heater to warm the bubble memory to its operating temperature range. This method is far simpler to design, build, and verify than temperature-compensation methods, and can be implemented at low costs. This approach has a drawback because of the temperature tracking requirements of the internal components of the bubble memory. The thermal gradients from the outside to the inside and across the memory must be limited. This puts a limit on the rate of heating of the memory, and hence, sets a lower boundary on the warm-up time.

The benefits, however, are that a commercial grade bubble (at about a fifth the cost of a military bubble) can be used to get the wide temperature operation at minimal cost. As with most heater applications, this heater requires some form of control to turn the heater off when the bubble has warmed up, and to notify the system the bubble is operational. The solution to this problem lies in a material with a positive temperature coefficient of resistance (switching PTC).

These PTC materials exhibit a slight negative temperature coefficient of resistance until they reach their switching (also known as anomaly) temperature, at which point they exhibit a large (often +50%/°C or more) positive temperature coefficient of resistance. By energizing the heater component containing this material with a constant voltage, the device will heat itself to a constant temperature and then keep itself there, regardless of the ambient temperature in the STE-X, all without external control circuitry. As the STE-X itself becomes even warmer, the resistance of the heater will continue to rise, and the power dissipated by the heater will drop to a negligible value. As a further bonus, the current through the heater can be sensed by use of a resistor and a comparator, and can be used to inform the main CPU that the bubble has warmed up. The PTC is rugged and inexpensive. In addition, it is inherently fail-safe, because there is no controller to fail and cause a heater to stay on and overheat.

In the future

The test set described in this paper is tentatively scheduled for production in mid- to late-1984. By then, advances in technology will be able to increase performance and decrease costs. Although the basic architecture will remain the same, changes will be made. By using the next generation of 256K DRAMs, memory capability can be doubled with half the memory chips now used. Finally, the next generation of bubble memory (4 Mbit) will eliminate a memory board and simultaneously provide 60 percent more storage than that now in the system.

J.W. Hively

Gate arrays or standard cells?

Gate arrays provide IC design solutions now, but standard cells may become the design solutions for designers in the 1980s, as circuit complexity increases, assessments of costs/benefits become more complete, and the market grows. RCA has the systems to compete in both technologies, and a special directorate to meet market needs.

Abstract: *Gate arrays and automated standard cells design systems provide complementary yet competing solutions for semicustom IC designs in the 1980s. To make an intelligent choice between the two approaches, an engineer should make a comparison of the economics of both approaches by assessing characteristics such as: complexity, die size, ease of design, turnaround time, packaging, flexibility, routability and cost. RCA's Solid State Division offers a highly automated design system that supports both gate arrays and standard cells. This design system is designed to be user-friendly and to maximize first-time design success.*

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It has been suggested that gate array technology represents a major revolution in the integrated circuit industry. A review of current and recent historical trends in integrated circuits indicates that major forces, revolutionary in nature, are driving an explosive growth in the number of gate array applications and gate array suppliers. But, the question is: Are we watching a gate array revolution, or a revolution being driven by our enhanced ability to design and manufacture cost-effective custom large scale integrated circuits?

Often-overlooked alternatives to gate arrays are standard cell semicustom circuits. This article will compare standard cells with gate arrays and will indicate the approach that is likely to be the most cost-effective for semicustom applications.

What is a semicustom integrated circuit?

Semicustom integrated circuits have been defined in various ways: As custom gate array "personalizations"; as uniquely programmed ROMs, PROMs, FPLAs (Field Programmable Logic Arrays), or PALs (Programmable Array Logic); as ICs "personalized" with from one to three unique mask levels on any base IC chip. All of these definitions are correct, but none is completely accurate. To clarify the definition, we can isolate some common denominators.

All definitions have in common a technique to implement a unique logic function inexpensively and quickly on a single integrated circuit chip. All approaches are restrictive inasmuch as the unique logic function must be defined within a specific structure, or architecture, and with the use of standard cells or logic building blocks. There is limited ability to design functions having unique electrical properties within any of the definitions. All definitions indicate a design methodology intended to minimize design cost and eliminate the need for a qualified integrated circuit design engineer, thereby allowing the design to be created by a logic design engineer.

A semicustom integrated circuit is "any custom integrated circuit that can be defined, designed, and implemented by the use of a set of standard structures—logic cells, circuit building blocks, or other predefined structures—with limited, or no, ability to structure unique electrical properties, but with provision for custom functional characteristics."

Many custom VLSI circuits, especially digital circuits, have no unique interface or electrical requirements, but require unique logic functionality. These circuits lend themselves to implementation through one of the various semicustom integrated circuit techniques available. All of these techniques lend themselves to design via various software design automation technologies, thereby:

- reducing design costs;
- reducing development time; and
- increasing the probability of first-time success.

Table I. *RCA gate arrays offered for CMOS LSI circuit development through the Solid State Division (automatically placed and routed).*

Family	Technology/attributes	Total gates	Pads I/O	Availability for design
PA20,000 Series	5 μm Bulk SiGate CMOS	250	46	Now
	Typical gate delay is 4 ns[1]	450	62	
	Operating voltage is 3-12 V	650	74	
		850	86	
		1000	94	
PA40,000 Series	3μm Bulk SiGate CMOS	650	74	Now
	Typical gate delay is 2.5 ns[2]	850	86	
	Operating voltage is 3-7 V	1000	94	
		1200	102	
PA50,000 Series	3μm Bulk SiGate CMOS	900	66	3Q83
	Double metal	1400	84	3Q83
	Typical gate delay is 2.5 ns[2]	2200	106	3Q83
	Operating voltage is 3-7 V	3200	130	4Q83
		4200	148	4Q83
		6000	172	4Q83
PA60,000 Series	SiGate CMOS/SOS (4μm, 2 μm)	650	74	Now
	Typical gate delay is 1-2 ns[3]	1200	102	Now
	Operating voltage is 3-12 V	2700	TBD	1Q84

NOTES: (1, 2, 3) 2 input NAND, FO = 2, local interconnect, (1) @ 10 V (2) @ 5 V (3) 4 μm @ 2 ns, 2μm @ 1 ns, both @ 10 V.

The primary force driving the semicustom revolution appears to be the basic economic need to develop custom integrated functions in a cost-efficient manner.

Semicustom techniques

The techniques available to implement a specific semicustom function on a single integrated circuit are as varied as the previous definitions. Standard programmable logic structures, such as PROMs and FPLAs, are very cost-effective when the logic to be implemented can use such a fixed structure and the required circuit performance requirements can be satisfied. These programmable circuits are mass produced as standard configurations to be programmed later, and they benefit from most of the same manufacturing efficiencies as other standard circuits. However, the flexibility and performance of these circuits are limited by their fixed architecture; therefore, FPLAs are frequently not suitable for many applications.

Gate arrays are arrays of logic gate components (transistors and resistors) in an uncommitted configuration that can be personalized by designing unique metal interconnection patterns. Depending upon the technology, gate arrays available in the industry are used to create semicustom circuits by personalization of from one to four unique levels (Table I). Gate arrays are more flexible than standard programmable structures, and can be used to implement high performance random logic functions.

Gate arrays are usually designed by placing predefined metal patterns describing various logic functions on the active component area of the array and then defining the interconnect pattern, to create a complete integrated circuit having unique functional characteristics.

Automated standard cells provide an alternate approach to designing a semicustom integrated circuit. A variety of these cells are usually available from a cell "library," much like a catalog of small scale integrated components. These standard cells represent basic logic components, each designed as an individual customized cell with all processing levels being unique. Most of these libraries contain cells that have at least one common denominator so they can be placed together in rows or columns—much like variable height or width building blocks—and then interconnected to create a semicustom function with no technical limit to the overall complexity (Table II).

Like gate arrays, the cells are predefined, and there is limited ability to design unique electrical functions. The design process is—like the design of a gate array—similar to the design of a printed circuit

Table II. *RCA PaCMOS standard cell libraries offered for CMOS LSI circuit development through the Solid State Division. The PaCMOS cells are all of fixed height and variable width with I/O parts at top and bottom of the cell.*

CMOS Technology	CMOS II[1]	CCL	CMOS/SOS	CMOS I	CMOS/SOS
Cell height	5.6	12.6	4.2	6.7	3.0
Pin spacing	0.45 (Mils)	0.8	0.9	0.56	0.4
Gate length (μm)	3	6.2	5	5	3
Delay (ns)[2]	3	10[3]	4[3]	5	2
Internal density (Mils/T)	1-1.9	5-8	2-3	1.5-3	0.9-1.4
Overall density (Mils/T)	4-6	12-20	7-9	6-10	4-6

(1) Available for design 3Q 1983

(2) Two input NAND, F.O. = 2, 5 V unless specified, local interconnect

(3) 10-V stage delay

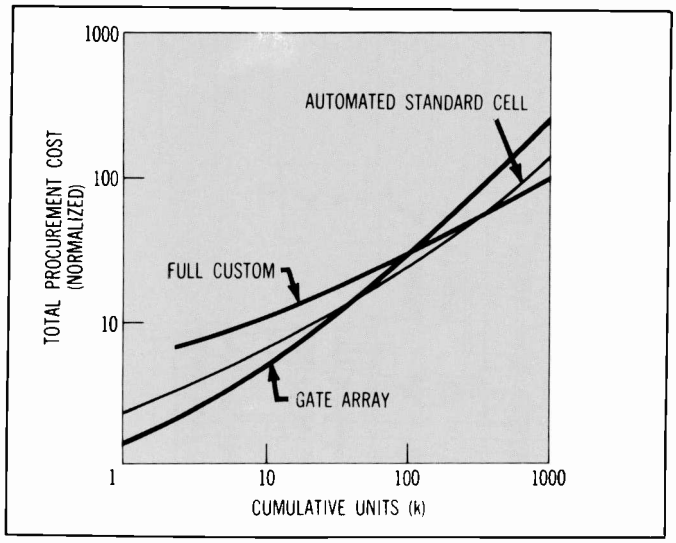

Fig. 1. *These curves indicate the relative procurement costs of gate arrays, fully automated standard cells, and full custom over a program's lifetime.*

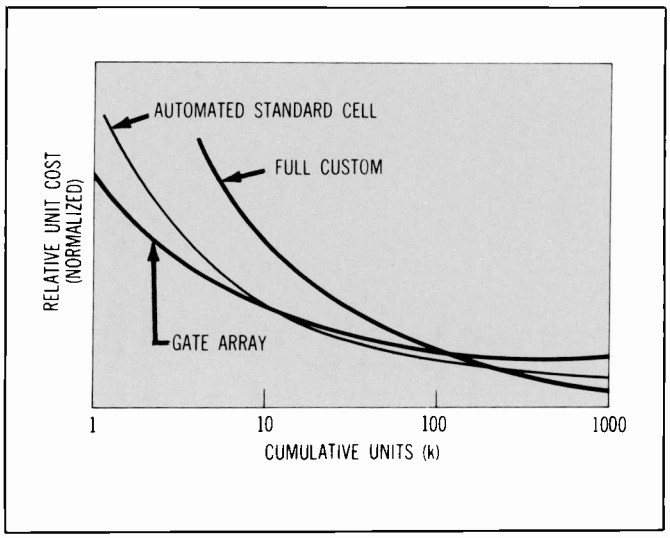

Fig. 2. *Amortized unit costs for two popular approaches to semiconductor logic. Full custom is included for comparative purposes.*

board in miniature, except that all masking levels must be created in order to produce a semicustom logic function. Unlike gate arrays, the transistor sizes in standard cells may vary from logic cell to logic cell, thereby providing improved circuit performance for the semicustom circuit.

Gate arrays or standard cells?

The various techniques described all satisfy the basic economic need for semicustom integrated logic circuits. The *best* technique for creating a semicustom integrated circuit, however, is the technique that provides the necessary circuit function and performance at the lowest overall cost. The total cost should be assessed from the beginning of the system's development to the end of the system's lifetime—this is the total procurement cost (Figs. 1 and 2). All of the techniques are available as tools for the design engineer to provide the most cost-effective system solution. There is no best choice for all applications. However, programmable standard structures, such as FPLAs, are frequently not suited for random logic circuits with VLSI complexities.

If a programmable standard structure, such as an FPLA, can provide the necessary performance and complexity it usually will provide the most economical solution. In this case, the design process is well defined. If a gate array or automated standard cell technique is selected, the choice has not been well defined and there are several issues to be considered by the design engineer in order to provide the most cost-efficient semicustom VLSI circuit.

Both gate array and automated standard cells, because of the regularity of their structures and the previous verification of their designs, lend themselves to automated design by computer. Design automation technology makes possible the implementation of a semicustom VLSI circuit layout from a logic diagram, under complete automatic computer control. This approach improves overall accuracy and reduces errors, makes it possible to design successfully the first time, and reduces the turnaround time and development cost. Design automation technology is considered essential for cost-effective semicustom LSI implementation. Some semicustom IC manufacturers, such as RCA's Solid State Division, have integrated both gate arrays and standard cells into a comprehensive automated design system, leaving the choice of approach to the design engineer.

To make an intelligent choice between gate arrays or standard cells, the engineer must make comparisons on the following points: complexity, die size, ease of design, turnaround time, packaging, flexibility, routability, and cost (Table III).

Complexity

Gate arrays are available in a wide assortment of complexity options. However, the complexity available from a gate array is fixed. If an application is smaller than the gate array, the design is inefficient; if the application is larger than the gate array, the design just will not fit.

Automated standard cells provide a complexity option that is technically unlimited and proportional to the application. Therefore, the design is always efficient.

Table III. *Comparisons of semicustom and full hand-packed custom design approaches to LSI logic circuits.*

	Semicustom		*Full custom*
Attribute	*Gate array*	*Automated standard cell*	
* Development cost	0.2	0.3	1
* Development time	0.2	0.25	1
* Final die size	1.5–2.0	1.1–1.4	1
* Production die size	1.7–2.2	1.2–1.5	1
Chip utilization	80%	100%	100%
Expected number of iterations to good samples	1	1	2
Flexibility	Low	Medium	High
Designer	Logic designer	Logic designer	IC designer

* Attributes are normalized to a full custom approach, assuming a 1000-gate complexity function.

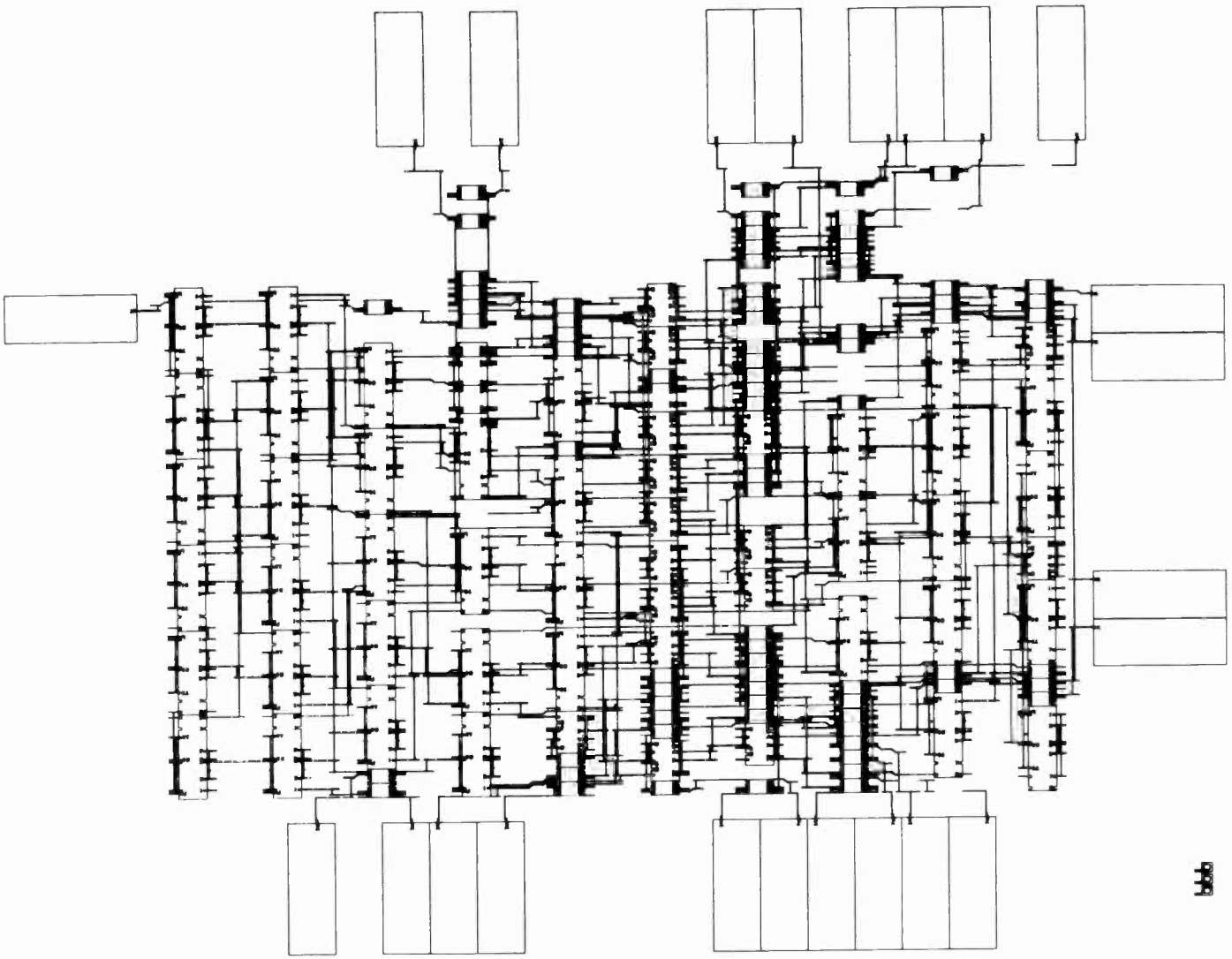

Fig. 3. *Check plot of a liquid-crystal display (LCD) Driver, implemented on RCA's PA20450 gate array as generated by the AUA (Automatic Universal Array) automatic placement and routing program. Check plots of this form are given to the customer to complete documentation.*

Die size

The final integrated circuit die size is important in determining the final component cost. Gate array die sizes are fixed and, for relatively efficient applications, frequently yield die sizes 1.5 to 2.0 times the size of a hand-packed custom circuit. Since automated standard cell designs are 100-percent efficient, the resultant die size is proportional to the complexity. However, some inefficiencies result (in the interest of achieving reduced design cost), so the die size is usually 1.1 to 1.4 times the size of a hand-packed custom circuit.

Ease of design

The design of a gate array and an automated standard cell semicustom circuit are essentially the same if supported by design automation. The logic is annotated with a set of standard logic building blocks from which design automation software automatically creates an integrated circuit design. The design procedure, in either case, is much like that for designing a logic board from a catalog of standard SSI/MSI circuit functions. In RCA's design system, many of the gate array logic cells and standard cells are functionally common, making it possible to map one design onto the other if circuit performance permits.

Packaging

Packaging technology must fit the application. However, packaging cost is often more important than IC die cost in determining the final component cost. With higher complexities and performance requirements, high pin-count packages are becoming important. High pin-count packages (greater than 48 pins) are expensive.

With gate arrays the chip size is fixed as are the total number of available bonding pads. This limits the choice of available packages for a specific complexity. In standard cell designs, on the other hand, only the specified number of bonding pads are used; circuits having higher complexity can be put into into a given package, or a circuit with the same complexity can be fit into a cheaper package with a smaller die cavity.

Flexibility

Gate arrays are designed to be somewhat universal for a class of applications. However, to be efficient, design compromises

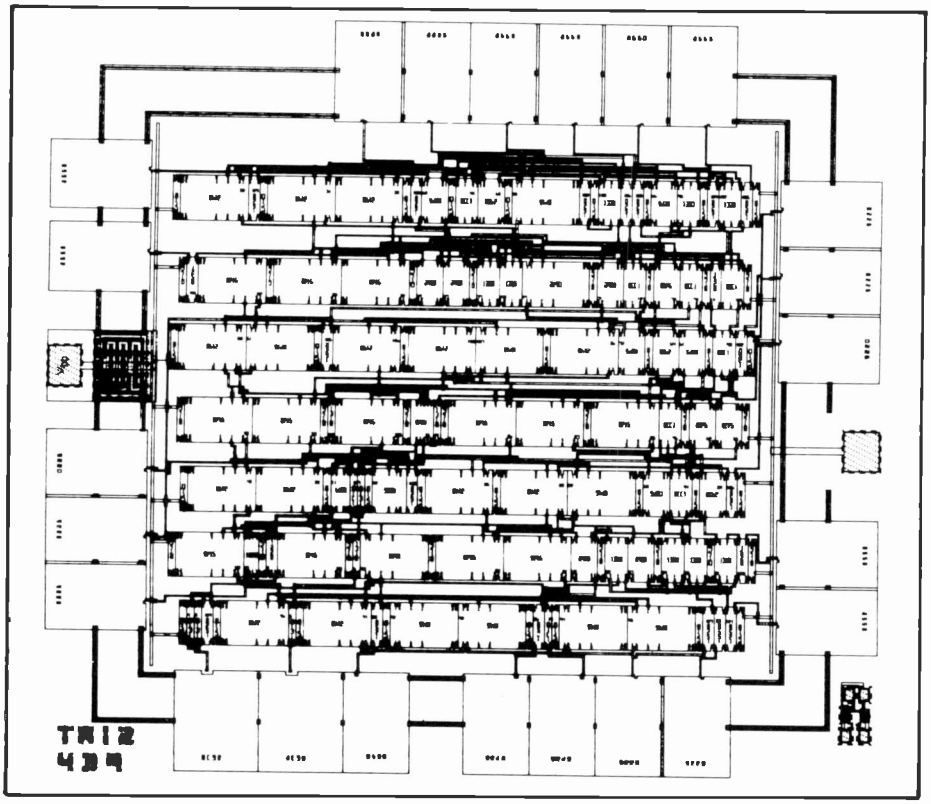

Fig. 4. *Check plot of an LCD Drive implemented on RCA's PaCMOS CMOS 1 standard cell system. This is the same circuit at scale as the LCD Driver implemented on the gate array in Fig. 3.*

must be made. The standard prediffused cells must have the components required to implement various logic functions and yet still allow the space necessary to interconnect these components. For applications that use many registers, or that use memory or PLA-like structures that could be densely packed, the silicon efficiency of a gate array design is reduced. If structures need to be added, require one additional transistor per function, or need one extra wire, they may not fit.

Standard cell design systems are very flexible when compared to gate arrays. New cells can be added to a family at any time as long as they fit the system requirements, such as having one fixed dimension. The cells are usually hand-packed and individually designed, and they are usually treated as "black boxes" by automated systems. The content of each cell is unrestricted.

Routability/design completion

Many gate array suppliers advertise a utilization factor such as 80 percent. Gate arrays by definition have a fixed number of interconnect wiring channels. The actual number of interconnections required is highly variable and is a function of the application.

It is very possible to design a function (probably highly parallel logic) that uses the number of gates allowed by the vendor for the gate array, only to learn later that the function cannot be interconnected. The only resolution to this problem is to redesign the function, sacrificing some feature, or to use a bigger gate array, sacrificing silicon and cost.

Standard cell design systems expand and contract the integrated circuit die size, adding interconnect paths as needed and, therefore, these circuits can always be interconnected.

Design cost

Differences in design cost may be a factor in the comparison of gate array and automated standard cell techniques. If logic simulation, automatic layout generation, and automatic design verification are used in the design process, then design costs are probably the same for either technique. In some cases, the cost for automatic layout generation is less for automated standard cells than for gate arrays because fewer constraints are placed on the interconnect software.

The major difference in cost between the techniques is that standard cells require additional masks and the processing of more wafers. This cost is often insignificant when reviewed as part of the overall procurement cost.

Turnaround time

One of the most significant advantages of the semicustom design technique is quick turnaround—from design input to samples. Gate arrays have an advantage: Prediffused wafers can be stockpiled and samples can be provided after simply completing the wafer processing. In contrast, standard cell design requires that wafers be sent through the entire wafer processing cycle because each mask layer is unique. This process typically takes three to five weeks longer, depending upon the manufacturer. In both cases the turnaround time is significantly less than with conventional custom designed circuits.

RCA's semicustom capability

RCA Solid State Division (SSD) has developed a comprehensive semicustom capability supported by design automation technology. It is intended to provide the systems manufacturer with a choice of techniques for an economic implementation of a semicustom integrated circuit while providing an efficient design process.

The RCA system supoports both gate arrays and PaCMOS automated standard cells with a variety of base gate arrays and automated standard cell libraries, in both CMOS/Bulk and CMOS/SOS technologies (Tables I and II; Figs. 3 and 4). The design automation tools that maximize first-time success are, with the exception of the layout programs, common to both techniques. Even older and smaller arrays designed for manual layout are supported by logic simulation and verification software. The design process for each technique is essentially the same, and may be transparent to the designer.

The design system

RCA's semicustom design system is highly automated and integrated. It is designed to provide a user-friendly design capability for the customer, and to be highly automated for first-time success through layout and design verification.

Within the RCA design flow (Fig. 5), the preferred method of operation is for

PaCMOS is an RCA trademark identifying the CMOS standard cell design system. It includes all CMOS technologies for which standard cell libraries are available.

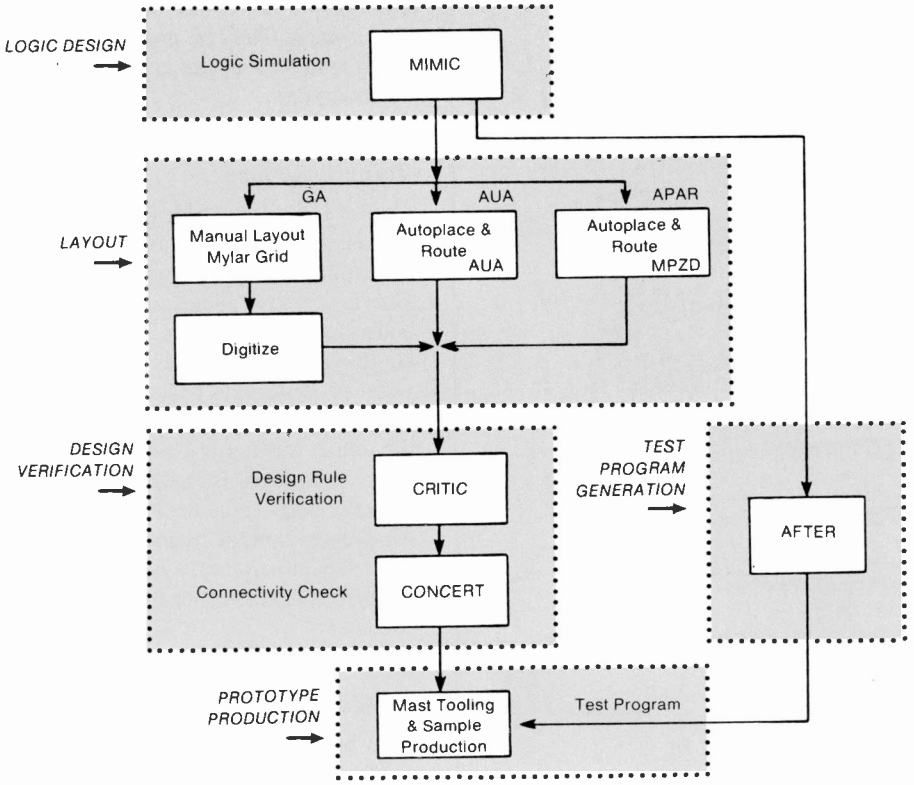

Fig. 5. *Semicustom design flow.*

the customer engineer to do the logic design and simulation with MIMIC and for RCA-SSD to control all other operations, beginning with the automated layout systems. To allow the customer engineer to control his design, RCA-SSD provides documentation and training on the use of the various gate arrays, PaCMOS libraries, and MIMIC.

The design engineer (customer engineer) gains access to the design systems (MIMIC and associated technology libraries) in one of three basic ways. The easiest interface to the system is via a Daisy Logician™ work station by the use of schematic capture software (Fig 6). The Daisy Logician provides easy documentation and automatically creates a MIMIC net list from the logic schematic entered. MIMIC is resident on SSD Semicustom's VAX 11/782™ host computer and can be accessed and interacted with via the Daisy (Fig. 7). If a Daisy Logician work station is not available, the design system can be accessed through either a dumb or intelligent terminal via the commercial Tymnet network, or through the RCA corporate computer network.

The major software components of the RCA semicustom design system are:

MIMIC — A powerful logic simulator

AUA — Automatic placement and routing for gate arrays

MP_2D — Automatic placement and routing of automated standard cells

AFTER — Automatic functional test encoding routine

CRITIC — Design rule verification

CONCERT — Connectivity certification

FASTRACK — An overall flow management system that integrates the design system

MIMIC

A powerful software simulation program, called MIMIC, allows designers of RCA semicustom LSI devices to model the logi-

Daisy Logician is a trademark of Daisy Corporation.

VAX is a trademark of DEC.

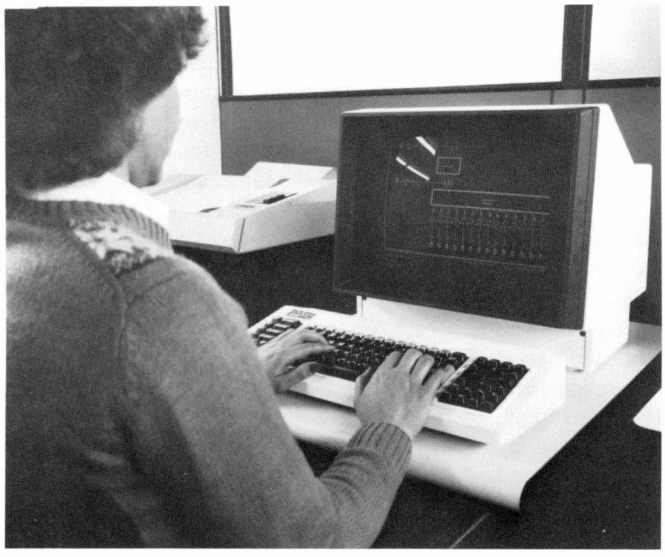

Fig. 6. *Entering the logic diagram of the LCD Driver into RCA's design system on the Daisy Logician engineering work station.*

Fig. 7. *MIMIC logic results of the LCD Driver as displayed back on the Daisy Logician. The MIMIC program is resident on the RCA/SSD Semicustom VAX 11/782 host computer and the Daisy is being used as an interactive terminal.*

RCA Solid State Division semicustom device operations

During 1982 RCA's Solid State Division established a separate product-line directorate, reporting to the Vice-President of Integrated Circuits, to specifically address the semicustom integrated circuit business (Fig. A). The charter of this directorate was to consolidate a variety of semicustom activities into a unified business unit and to participate in the rapidly growing but highly competitive semicustom business, now serviced by more than 60 companies worldwide.

The semicustom organization is using automated design software tools developed by the Advanced Technology Laboratories in Camden and the Solid State Technology Center in Somerville, as well as gate arrays and cell libraries developed in both of those organizations. These development tools have been integrated into one design system, and new design tools and products are being added by the semicustom activity.

The Semicustom directorate has installed a VAX 11/782 host computer in Somerville and has started to establish a worldwide computer network specializing in cost-effective semicustom LSI circuit development. Design and training centers are operational in Brussels, Belgium, and Somerville, N.J., with Daisy Logician engineering work stations tied to the host computer via data links.

A network of design representatives franchised to support RCA's semicustom business is starting to develop worldwide. Each of these design reps will own and operate a design center and will support customers with

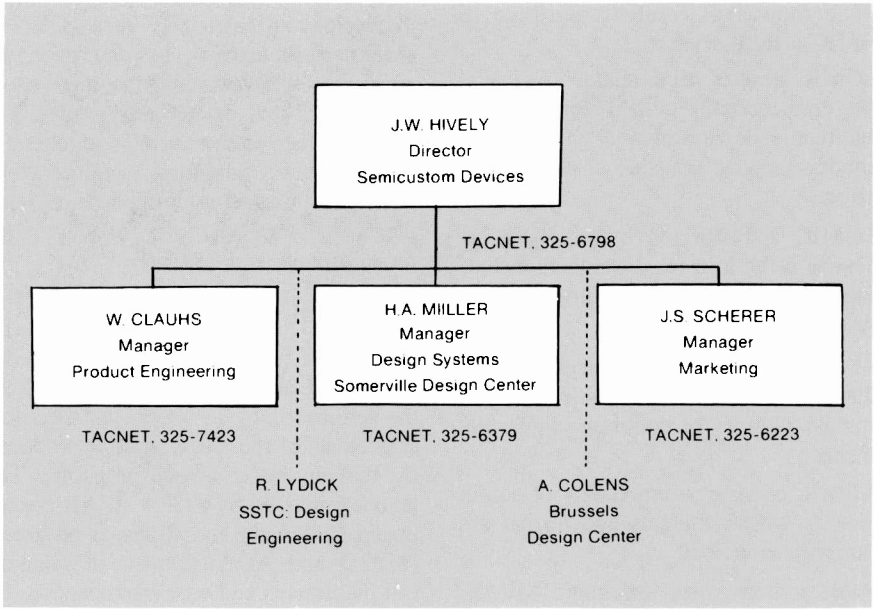

Fig. A. *Design support for all SSD Semicustom business is supported by this activity along with Marketing and Sales responsibility for all commercial product. Hi Rel sales are handled through the Hi Rel directorate at SSD.*

their designs through logic simulation. The first of these technical design representatives are Iselqui in Italy and Circuit 21 in Pennsylvania.

The semicustom business is often referred to as the gate array business and is driven by the market need for cost-effective custom digital LSI circuits. The merchant semicustom market is projected to be $6.6 billion by 1990. Of this, $4.4 billion will be in CMOS technology and the remaining $2.2 billion will be divided between bipolar and NMOS technologies. Gate-array-based circuits currently dominate the market with standard-cell-based circuits expected to gain dominance later in the decade. Semicustom circuits are replacing standard logic in most new systems designs and many old systems designs.

The Semicustom Device Operations directorate is dedicated to providing a system for cost-effective custom LSI solutions, the training and education required to promote this capability, and the high level of quality customer service required to make RCA a leader in the semicustom CMOS LSI business. The business emphasis is on first-time circuit success. Major investments being made in hardware and in the system will minimize human involvement and improve overall quality and productivity.

The semicustom organization is responsible for design and training support for all SSD semicustom business as well as marketing and sales for all commercial products. All high-reliability semicustom products are marketed and sold through SSD's Hi Rel product line. For more information contact: Jack Scherer (commercial products), TACNET 325-6632; or Jack Handen (Hi Rel products), TACNET 325-6643.

cal operation of digital circuits before device fabrication. Through the program, designers can discover logical flaws; race, hazard, or spike conditions; and timing and critical-path uncertainties.

The following features contribute to MIMIC's effectiveness:

- MIMIC models circuit elements such as bus connections, wire-tied elements, and bidirectional transmission gates. These models are not available in other simulators.
- MIMIC is supported by an extensive library of built-in logic elements including gates, latches, clocked flip-flops, and multiplexers.
- Through MIMIC's hierarchical network-description, designers can define their own standard library of common circuit elements.
- MIMIC can generate a variety of output reports whose contents and format are largely user-defined.
- And, perhaps most important, MIMIC has the ability to generate a test-pattern file acceptable as an input to automatic test equipment. Because the number of test patterns increases exponentially with the complexity of a design, the ATE interface can materially reduce test times and costs.

AFTER

The AFTER (Automatic Functional Test Encoding Routine) program aids in the generation of functional test patterns required for the testing of digital ICs on Automatic Test Equipment (ATE). Input/output truth tables, representing these tests, are created by the designer who uses the MIMIC logic simulation program by specifying the IC's inputs to MIMIC; its outputs are calculated by MIMIC. AFTER automatically translates these input and output conditions into test patterns suitable for execution on a variety of ATEs. ATEs currently supported are the Fairchild Sentry/Sentinel/Series 20, the Teradyne J283, and the Datatron test systems.

CRITIC

Another software tool available for the design of RCA semicustom LSI devices is the CRITIC program. CRITIC is an acronym for Computer Recognition of Illegal Technology in Integrated Circuits. CRITIC checks mask artwork by describing the mask as a series of polygons, in terms of the vertices that define these shapes. The program then automatically searches for and reports on minimum tolerance violations (width, spacing, and enclosure) and illegal topology relations (overlap, abut, cross, contain, and disjoint).

CONCERT

CONCERT (CONnectivity CERTification) is a layout analysis program that aids in the verification of the logical and electrical correctness of the mask artwork produced by the automatic layout programs. The layout generated by RCA's APAR (Automated Placement and Routing) programs (MP2D and AUA) consists of standard cell placements and wire interconnects. By examining this information, CONCERT can extract a net list from the artwork and automatically produce the logic description in the exact language required by the MIMIC logic simulator. This description is compared to the original MIMIC input to verify correctness of the wiring.

Ordinarily, since the IC layout is computer generated, no errors will be found. However, in those cases where the designer chooses to perform some manual modifications. CRITIC and CONCERT are important tools for validating the changes. In addition, parasitic capacitances of the interconnections, as laid out, are added to the MIMIC network-description file. This provides the designer with the ability to effectively simulate the physical layout itself, including layout parasitics. This re-simulation increases confidence that the layout is free from timing problems caused by the possibly excessive capacitance of signal lines. These capabilities make CONCERT a key ingredient in producing quick-turnaround, working custom chips that meet specifications the first time.

James Hively is Director, Semicustom Device Operations, at RCA Solid State Division. Mr. Hively has a BSEE from San Diego State University in 1963 and a MSEE from Arizona State University in 1969. Prior to joining RCA, he held various Circuit Design, Engineering Management and Business Management positions with Motorola, Fairchild and Texas Instruments since 1963. Mr. Hively joined RCA/SSD in February 1982, in his present postion, with the charter of establishing a new product-line directorate to address the semicustom integrated circuit business.

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Somerville, N.J.
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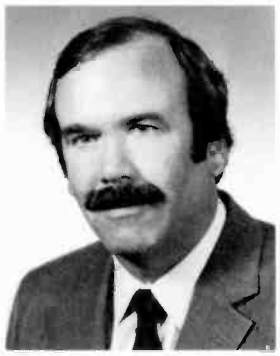
Making the comparison

The choice of approaches—gate array or automated standard cell—is left to the design engineer. This choice must be based upon the technology's ability to satisfy the system requirements and cost objectives. It is an economic choice.

The information provided in the comparison charts is often useful in selecting the best semicustom technique in RCA's comprehensive system.

Future

Forecasters have projected the development of a large market for semicustom integrated circuits during the 1980s. That market today is dominated by gate array technologies. The author expects gate arrays to yield to automated standard cells, which will become the dominant approach later in the decade. The shift from gate arrays will come about as circuit complexities increase to, and exceed, the 10,000-gate level; the shift will result from the improved flexibility and packing density inherent in standard cells, and the continuing pressure to maintain a simple design process.



B.F Williams

Sun sets on RCA energy research

RCA Laboratories has had a long history of research on electronic means for generating electricity and, in fact, our earliest experiments in solar cells go back more than 30 years. More recently, we have had a large program on amorphous-silicon solar cells, and this approach to generating electricity from sunlight appears to be among the most promising future alternatives to nuclear or oil-driven power plants. RCA's program began and prospered in a period of national concern and substantial government support. The technology achievements at RCA Laboratories have been outstanding and were capped last year by the first amorphous-silicon solar cell with efficiency in excess of 10 percent.

However, energy generation is not one of RCA's mainstream businesses, and the cost of proceeding with any realistic program to commercialize the technology could approach 100 million dollars. Over a year ago, RCA determined that it could not underwrite this business opportunity alone and has been seeking partners to continue the technology programs as a joint venture. Although the response to this effort has affirmed the strength of RCA's technology position, we have been unable to conclude an agreement that would provide the level of resources needed to continue the photovoltaic program.

Therefore, as of this writing, RCA is seeking to sell its photovoltaic technology, as well as the specialized equipment associated with the solar-energy program. We are redirecting most of the people involved to other research programs that are more directly supportive of RCA's present business plans and that represent other growth opportunities.

—Brown F Williams
Staff Vice-President
Display and Energy Systems Research

A.H. Firester | D.E. Carlson

Harnessing the sun with amorphous-silicon photovoltaics

An energy-efficient, large-area, panel process developed at RCA Laboratories features a fast, glow-discharge deposition to create amorphous-silicon active-device layers. The result: A leading photovoltaic solar-energy source.

Abstract: *The conversion efficiency of amorphous-silicon solar cells has improved steadily since 1974, and an efficiency of 10.1 percent was recently achieved at RCA Laboratories. The theoretical limit for the conversion efficiency is projected to be about 20 percent, and practical panel efficiencies should reach 12 to 14 percent within the next few years. Even higher efficiencies might be achieved in the next several years with stacked junction structures. For a pilot plant producing 30 megawatts of monolithic amorphous-silicon photovoltaic modules per year, we predict a manufacturing cost of less than $0.50 per peak watt ($W_p$).*

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Reprint RE-28-3-8

It has been less than a decade since the amorphous-silicon solar cell was conceived at RCA Laboratories.[1] Yet, within that short time, this device has been the research subject of hundreds of scientists throughout the world, and it now promises to become a significant generator of electric power within this century. Although the device and its constituent materials are scientifically fascinating, what has driven this explosive research growth is the economic potential of amorphous-silicon solar cells.[2]

Sunlight is free, nonpolluting and ubiquitous, yet solar cells are not used to generate very much of the electricity that we use. This is because conventional fossil-fuel power plants cost less to own and operate than today's solar modules and the required add-on components for complete power-generating plants.[3] Amorphous silicon provides a solution to this problem. Photovoltaic module cost is determined by the material and fabrication costs, and the performance (the amount of electricity each square inch of the module can generate). Performance also leverages the total plant costs, because fewer mounting structures, less land area, and so on, are required by higher-performance modules. Our research in amorphous silicon indicates that amorphous-silicon photovoltaic modules will be both the price and performance leader in the next decade.

This issue contains three companion papers. One, by Goldstein, *et al.,* discusses the electronic properties of amorphous silicon; a second, by Catalano, *et al.,* treats the chemistry of the deposition process; and the third, by Stranix and Firester considers the application of amorphous silicon for grid-connected electricity generation. In this paper, we will review why these devices are so attractive, how they are made, and what their performance and costs are expected to be.

The amorphous-silicon material

Pure amorphous silicon cannot be used for electronic devices due to a large concentration of defect states associated with dangling bonds. However, when amorphous-silicon films are grown in the presence of atomic hydrogen, a glassy silicon-hydrogen alloy (*a*-Si:H) is formed, and the material can exhibit the properties of a good quality semiconductor.

The best quality amorphous-silicon films have been deposited from either rf or dc glow discharges in silane (SiH_4). The substrate temperature is typically in the range of 200 to 300°C, while the silane pressure is usually in the range of 0.1 to 1.0 torr.

The composition and optical properties of hydrogenated amorphous silicon depend on the deposition conditions. For example, the hydrogen content decreases and the optical absorption increases as the substrate temperature increases. The films used in solar cells typically contain approximately 10 atomic percent of hydrogen and possess an optical gap of approximately 1.70 eV. Because this material is amorphous, it absorbs visible light much more strongly than crystalline silicon. Thus, an *a*-Si:H film about 1-μm thick can absorb a significant fraction of the energy in sunlight.

The electronic properties of *a*-Si:H are also well suited for photovoltaic devices because, as discussed by Goldstein, *et al.,* in another article in this issue, the diffusion length can exceed 1 μm in undoped films. This ensures efficient collection of photogenerated carriers in solar cells where the thickness of the active layer is approximately 0.5 to 1.0 μm.

The amorphous-silicon solar cell

The photovoltaic characteristics of an efficient *a*-Si:H solar cell are shown in Fig. 1.

The conversion efficiency is determined from the expression

$$\eta = J_m \cdot V_m / P_i$$
$$= FF \cdot J_{sc} \cdot V_{oc} / P_i$$

where J_m and V_m are the current density and voltage for the cell operating under maximum output-power conditions, and P_i is the incident sunlight power (about 100 mW/cm^2 for the sun directly overhead). J_{sc} is the short-circuit current density, V_{oc} is the open-circuit voltage, and the fill factor (*FF*) is a measure of the sharpness of the "knee" in the *I-V* curve.

Although a variety of *a*-Si:H solar-cell structures have been investigated, the best devices have been fabricated in a *p-i-n* configuration. Figure 1 depicts schematically the cross section of a typical amorphous-silicon solar cell. It consists of three thin layers deposited on a supporting sheet of glass. The first layer is a transparent conductor, such as doped tin oxide, approximately 70-nm thick. The second consists of the amorphous-silicon photovoltaically active layers, which typically consist of three sublayers: (1) a 10-nm *p*-type contact layer consisting of a boron-doped alloy of amorphous silicon and carbon (*a*-Si:C:H); (2) a 500-nm intrinsic layer; and (3) a 20- to 50-nm *n*-type contact layer. The addition of carbon to *a*-Si:H increases the optical gap so that the *p* layer acts as a window layer.[4] The last layer is a 100- to 500-nm-thick back-metallization layer of aluminum, or another reflective metal or metal combination. Thus, the total thickness of the amorphous silicon thin-film device is on the order of 1 μm.

The doped layers in the *p-i-n* structure establish an internal electric field that assists in the collection of photogenerated carriers. In high-performance cells, the electric field is relatively uniform across the undoped or intrinsic layer when the cell is short-circuited, and thus, almost all photogenerated carriers are collected. Figure 2 shows the spectral response or quantum efficiency of a high-performance *a*-Si:H *p-i-n* device. When such cells operate near the open-circuit condition, the internal field becomes very small, and then diffusion effects may dominate. If the diffusion length is larger than the thickness of the *i* layer, then a significant photocurrent can be collected even when the cell operates close to the open-circuit condition. However, if the diffusion length is small, then the collection region and hence the photocurrent will decrease as the cell is forward biased, resulting in reduced efficiency.[5]

Solar cell efficiency

The theoretical limit for the conversion efficiency of an *a*-Si:H solar cell can be estimated by making several assumptions. First, if there are no reflection or recombination losses then, from optical absorption data, $J_{sc} \cong 22$ mA/cm^2 for a 1-μm-thick film. The maximum value of V_{oc} is estimated to be approximately 1.0 V, assuming that the built-in potential is limited by recombination in band-tail states[6] (these tail states are a consequence of bonding distortions in an amorphous semiconductor). The fill factor for an ideal diode (with $V_{oc} \cong 1.0$ V) is about 0.87. Therefore, the theoretical efficiency limit is approximately 19 percent.

Even higher conversion efficiencies are possible if the solar cells are configured in a stacked or multijunction structure.[7] In stacked junction cells, two or more *p-i-n* structures are layered one upon the other with the optical bandgaps and thicknesses adjusted so that each *p-i-n* junction produces the same current. For example, the first junction might consist of an *a*-Si:H alloy with a wide bandgap, the second junction, *a*-Si:H, and the back junction, *a*-Si:Ge:H with a narrow bandgap. The theoretical limit of such structures should exceed 30 percent.

The conversion efficiency of *a*-Si:H solar cells has improved dramatically in recent years, as shown in Fig. 3. The best performance to date is 10.1 percent for a 1.09-cm^2 cell fabricated at RCA Laboratories.[8] The conversion efficiency should continue to improve as better doped layers and alloys are developed, and practical module efficiencies (depicted by the shaded bands in Fig. 3) approaching 20 percent are projected by the end of the decade.

Module manufacture

A key advantage of amorphous silicon over other photovoltaic materials is that a truly *integrated panel process* can be developed. Large-area, panel-sized substrates can be easily coated, thus panels do not have to be assembled from a mosaic of wafers. The panel structure, which RCA has developed to exploit this advantage, we term a series-intraconnected monolithic panel.[9] When finished, these monolithic panels consist of a series of individual, narrow strip cells spanning the width of the panel. These strip cells are interconnected in series along their long dimension. Figure 4 depicts such a panel, and the inset schematically shows how the transparent contact of each strip cell is connected to the back-metal contact of the adjoining strip cell. This structure

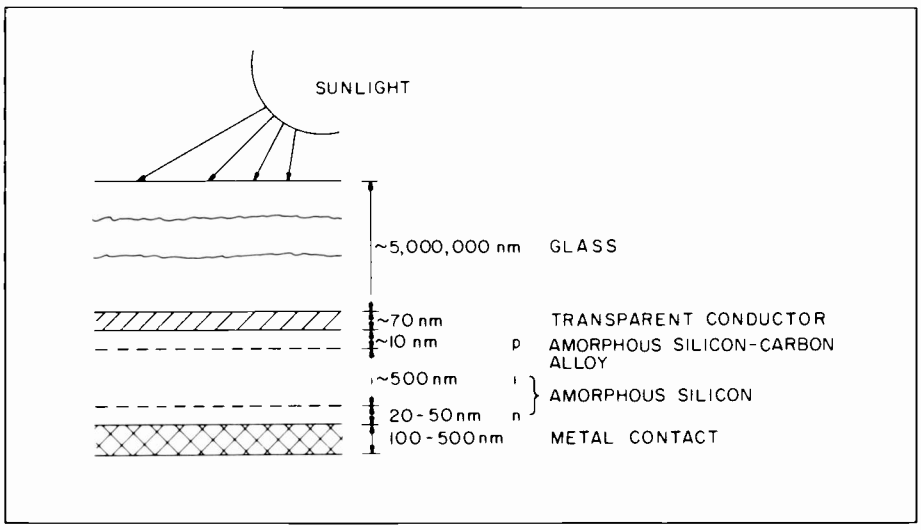

Fig. 1. *Cross-sectional structure of a single* p-i-n *amorphous-silicon solar cell.*

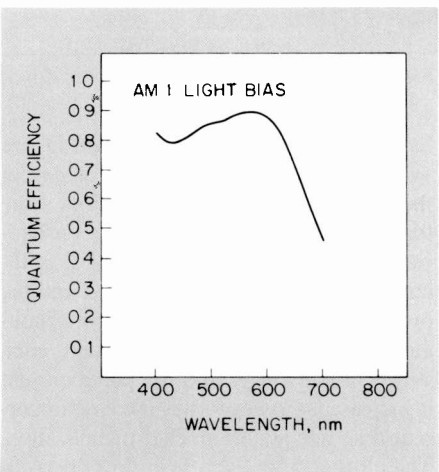

Fig. 2. *Spectral response of a high-performance* p-i-n *amorphous-silicon solar cell.*

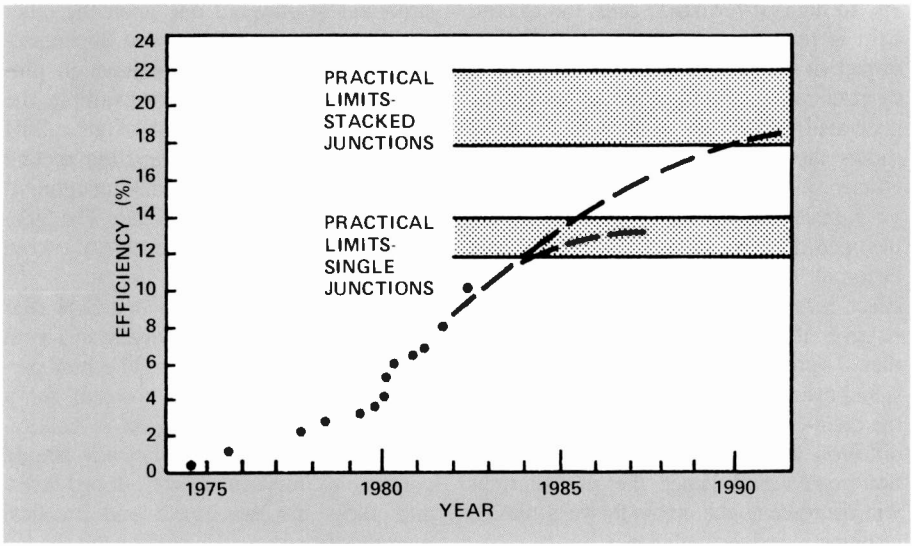

Fig. 3. *Amorphous-silicon photovoltaic device projections.*

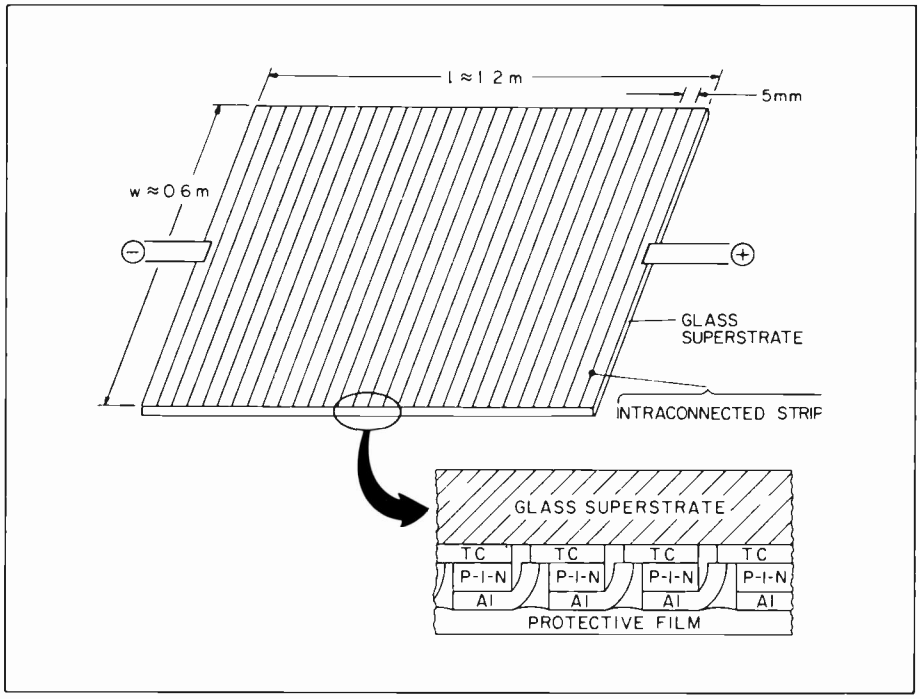

Fig. 4. *The amorphous-silicon monolithic-series intraconnected panel.*

has the virtue that it can be scaled in size *without* increasing the thickness of *any* of the deposited layers and, in addition, more than 97 percent of the module is unshadowed, active area. If the length, l, is increased, more strip cells are added and the overall panel voltage increases proportionately. If the width, w, is increased, each strip is made longer and the panel current is increased. However, this increase in current does not require thicker metallization. The current from each strip flows perpendicularly to the strip along the panel length, maintaining constant surface-current density.

Most important is that this monolithic panel can be fabricated by a process sequence in which the entire panel, or even a larger unit which can be cut into panels later, is processed at once. The panel fabrication process that we are developing at RCA is shown schematically in Fig. 5. It begins with a sheet of glass, perhaps 4′ × 4′. The glass is washed and dried **(a)** and then introduced into a belt furnace system for the chemical vapor deposition of the transparent contact **(b)**. Next, the transparent contact layer is divided into the narrow electrically-isolated strips that define the individual strip cells. Schematically, we show this division to be performed by laser scribing **(c)**, a rapid and low-cost technique.[10] Following this patterning operation, the three amorphous-silicon sublayers are deposited in three separated consecutive reaction chambers by glow-discharge deposition **(d)** in silane mixtures. The amorphous-silicon device deposition covers the entire panel. Now the panel is ready for its next laser scribing operation **(e)** to divide the amorphous-silicon active-device layer. This step provides a silicon-bare line on the transparent conductor where the back metallization can make contact. The back-metal contact is deposited by vacuum evaporation **(f)**. This is followed by a final laser-patterning operation **(g)** to electrically separate the back metallization into the final series-connected strip cells. Now, the *panel* is ready for testing **(h)**, protective lamination **(i)**, and finally, power-connector application **(j)**. At this point, the panel is complete. It is ready for packaging or for installation and sale.

Module costs

Amorphous-silicon photovoltaic modules are expected to be *very* inexpensive. They require very little silicon. In addition, glow-discharge deposition is a fast, low-temperature, large-area, continuous-deposition process that is, therefore, inexpensive. Finally, the modules lend themselves to continuous production—an assembly process is not needed to form large units from many smaller separate devices.

Because this is an energy-efficient, large-area, *panel* process—fabricating a structure which is intrinsically frugal in its use of expensive materials—the overall production costs will be low. We estimate that the production costs of these panels will be less than $0.50 per peak watt ($W_p$) in 1982 dollars at annual production volumes of 50 MW/yr. Figure 6 shows how these costs are distributed, based upon a panel conversion efficiency of 10 percent. As might be expected for a low-cost high-volume product, half of the total cost is in the direct materials. Of this cost component, slightly more than half is accounted for by the superstrate material—the tempered glass. Another important point, indicated by this analysis, is that the cost of the capital equipment can be less than 10 percent of the total product cost. This has significant implications for the capital required for building amorphous-silicon module factories. An examination of the cost components by process reveals that, excluding the cost of the glass superstrate, the cost of amorphous-silicon deposition, laser pat-

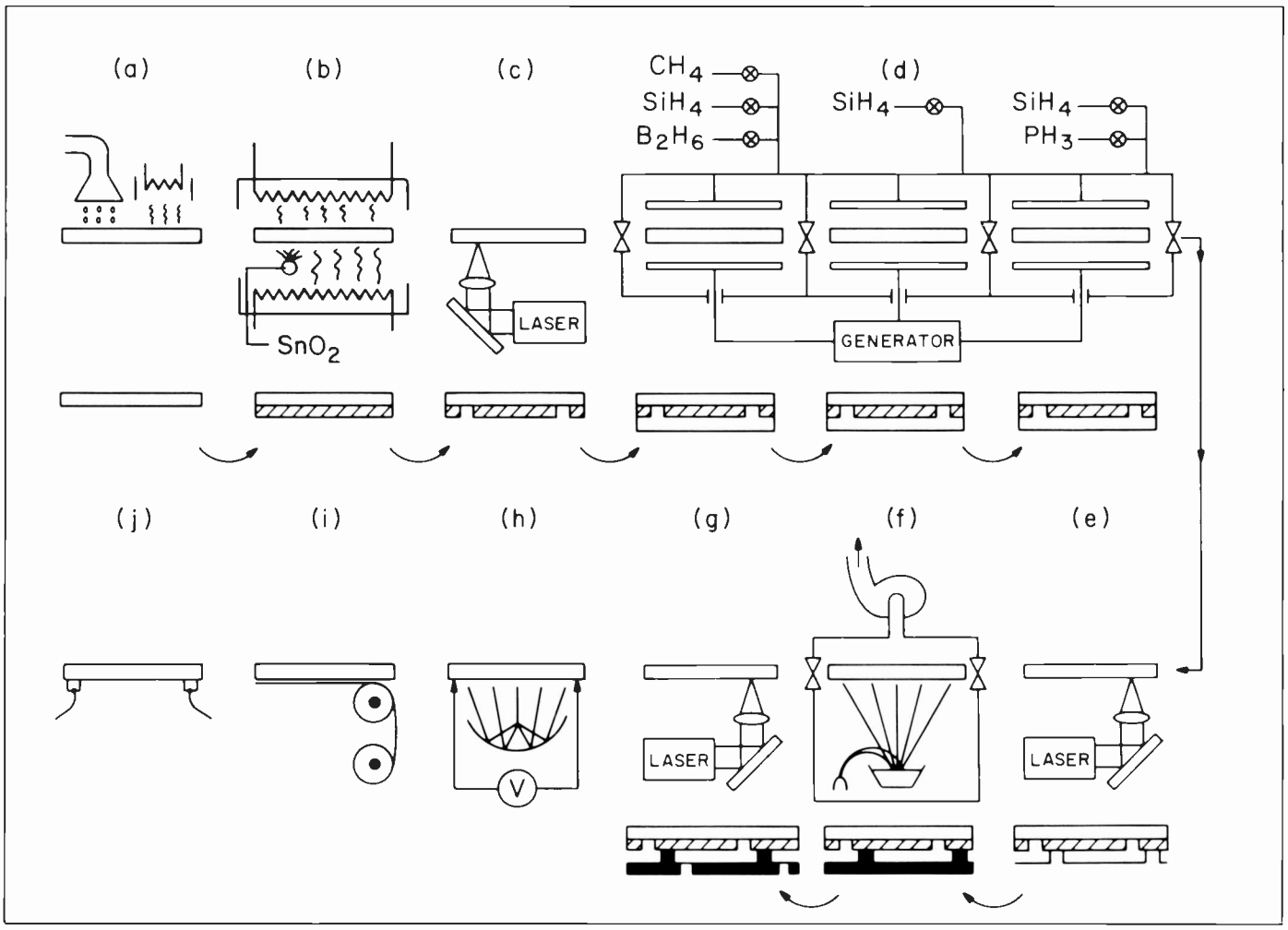

Fig. 5. *The production-process sequence for fabricating amorphous-silicon monolithic-series panels.*

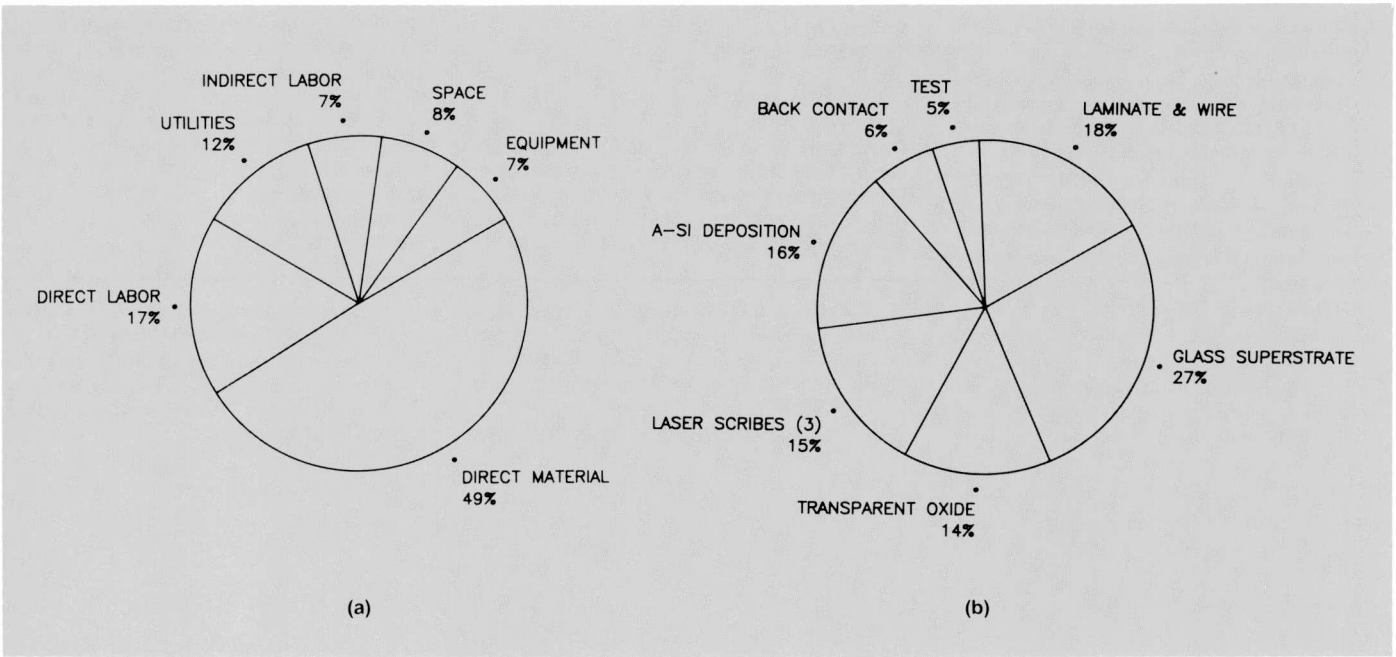

Fig. 6. *Amorphous-silicon monolithic-panel cost allocations;* **(a)** *production-cost allocations,* **(b)** *process-cost allocations.*

terning, transparent-conductive-oxide deposition, and module fabrication are of approximately equal importance. Although we believe these cost estimates to be realistic, the realization of these costs will depend on continued development in both the fabrication processes as well as the performance of the basic devices.

Outlook

More than 50 companies and universities are now involved in the research and development of amorphous silicon. Several companies sell products for portable calculators, watches, and other limited power applications. Progress, both research and commercial, should continue to accelerate in the next decade. Today's device efficiencies are expected to rise into the 15- to 20-percent range, while improvements in process technology should continue to increase the rate at which high-quality amorphous silicon can be produced. Amorphous-silicon modules will be inexpensive, costing less than $\$.50/W_p$ of solar-panel power-generating capacity. Thus, the amorphous-silicon monolithic module, as the performance and cost leader in photovoltaics, will lead the solar-energy competition to traditional petroleum-based electricity generation. The amorphous-silicon solar cell, an RCA invention, should have a very bright future.

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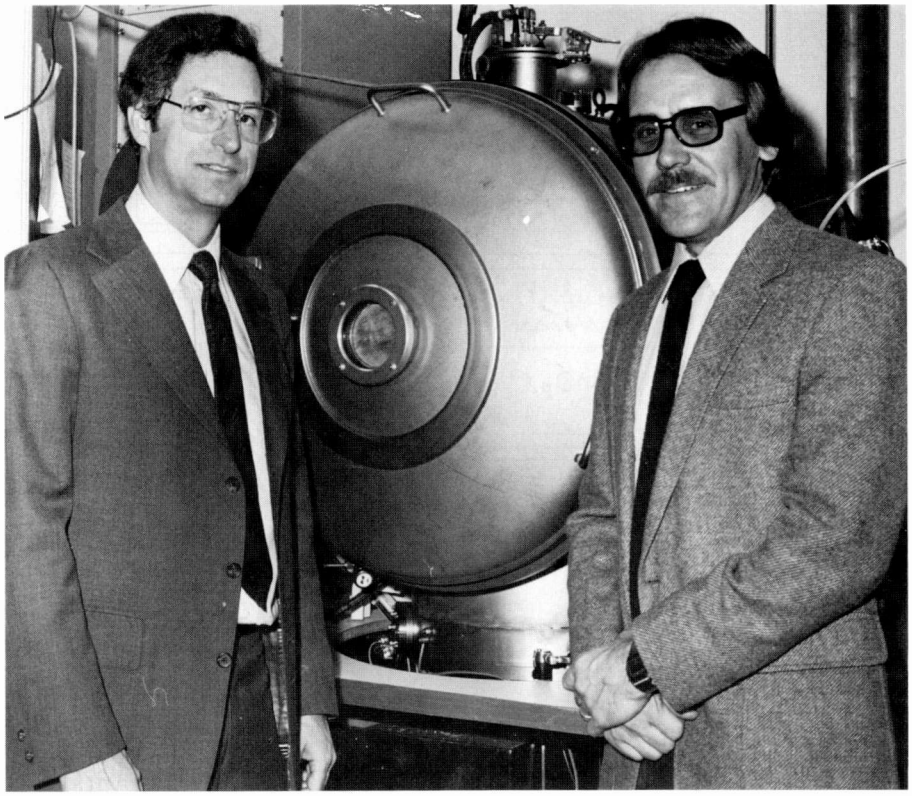

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Diffusion length and surface photovoltage*

The simplest and most reliable way to measure hole drift in thin films of amorphous Si:H turns out to be through the use of the silicon's own intrinsic surface barrier.

One of the most important properties of the semiconductor materials from which solar cells are made is the minority-carrier diffusion length, L_p. Until about 1980, the only direct measurement of this quantity for the case of hydrogenated amorphous silicon (amorphous Si:H or *a*-Si:H) had been through the use of the photo-electromagnetic effect.[1] This was an extremely difficult measurement, however, and could not be considered as a practical, continuing monitor of the quality of the *a*-Si:H material used in the solar-cell program. The only other possibility during this time was to estimate L_p (and other important material properties) from the characteristics of a completed solar cell. Such estimations, however, were often uncertain (if not actually misleading) due to complications introduced by the unknown properties of contacts, interfaces, and doped layers.

We describe in this paper a method for the fast, simple, and direct measurement of the diffusion length of undoped *a*-Si:H using surface photovoltage. Although this method has enabled us to study some of the properties of L_p (to be discussed later), perhaps its most consistently valuable contribution has been the input it has supplied to the film deposition effort. There, the method has helped in the optimization of several components of the deposition process and has furnished a convenient and ongoing monitor for evaluating the solar-cell material.

Abstract: *We describe a fast and direct method for the measurement of the minority-carrier diffusion length, L_p, in* a-*Si:H. The method centers on the creation by light of electron-hole pairs at different distances from the surface, and the use of changes in the surface barrier height to measure the drift of holes. We have used this technique for measuring diffusion lengths of up to 2.0 μm, for estimating the hole lifetime and space-charge density, and for studying optical instabilities. Currently, this measurement method acts as the primary ongoing monitor of material quality in the* a-*Si:H solar-cell program.*

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Basic principles of the method

The basic idea centers on the use of light to create carriers at varying distances from a fixed collection plane; the collected minority-carriers (in this case, holes) are then sensed. The fixed plane is the surface, which conveniently furnishes a surface Schottky barrier for minority-carrier collection; and the use of monochromatic light of different wavelengths (and hence different absorption coefficients) generates carriers at different depths below the surface. The method is illustrated schematically in Fig. 1.

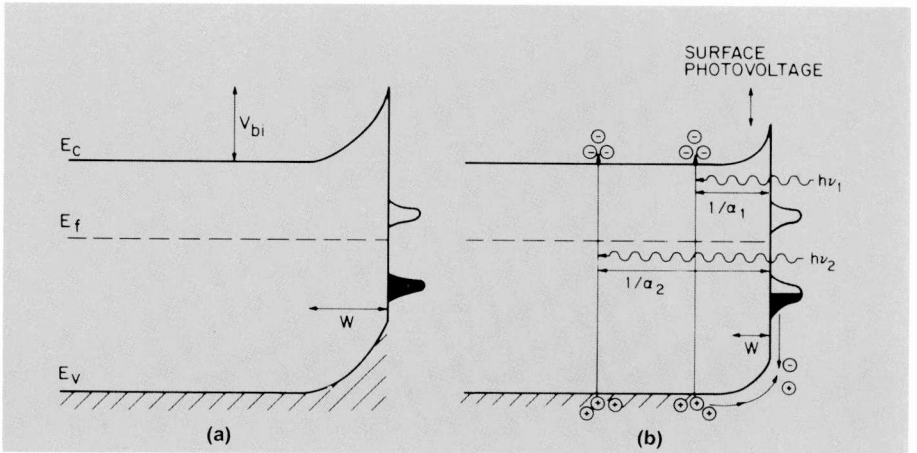

Fig. 1. *Schematic illustration of the basic principle for measuring* L_p. **(a)** *Typical* n*-type semiconductor;* **(b)** *Generation by light of electron-hole pairs and the subsequent drift of holes to the surface.*

Figure 1a describes a typical situation at the free surface of an n-type semiconductor with filled and empty surface states. The negative charge on the surface, together with its counterpart positive charge in the space-charge region, produces band-bending as shown and a Schottky barrier with built-in voltage V_{bi} and depletion width W. If the surface is illuminated now with light of photon energy $E > E_g$, and absorption coefficient $\alpha > W$, the process schematically illustrated in Fig. 1b will occur. Electron-hole pairs will be generated. Some holes will drift to the depletion region W, where they will be swept to the surface and will depopulate filled surface states, thereby decreasing V_{bi}. (Electrons will not contribute to changing the population of the surface states because of the barrier). The change in V_{bi} is called the Surface Photovoltage (SPV) and, in regions of light intensity below saturation (the saturated SPV is V_{bi}), the SPV varies with the hole concentration at the surface.

As mentioned earlier, the use of monochromatic light of different absorption coefficients α results in minority-carrier generation at different distances from the surface. If the light intensity at each wavelength is adjusted to give the same SPV, then it can be shown[2] that under certain conditions

$$I = \text{constant}\,(L_p + 1/\alpha) \qquad (1)$$

where I is the photon flux penetrating the surface. The particular advantage of always working with the same SPV in a given experiment is that we know we are dealing with the same hole concentration reaching the surface; hence we do not need to know either the absolute hole density or the actual relationship between hole density and SPV. This accounts for the relative simplicity of Equation (1). The intercept of Eq. (1) on the abscissa yields L_p. For a more detailed discussion of the method, the reader is referred to original publications.[2, 3, 4]

Several conditions must hold for the method to be successful. These are:

$$W < 1/\alpha < d \qquad (2)$$

$$L < d \qquad (3)$$

$$n > p \qquad (4)$$

$$L > W \qquad (5)$$

where W is the depletion width at the surface, d is the thickness of the semiconductor layer and n and p are the densities of the majority and minority carriers. Conditions (2) and (3) are easily met in principle by making the sample sufficiently thick (for a-Si:H we have found a sample thickness between 2.0 and 4.0 μm to be adequate). For semiconductors, condition (4) is usually introduced to ensure that the lifetime of the minority carriers is a well-defined property of the sample. In undoped a-Si:H, which is a slightly n-type photoconductive insulator, the hole lifetime will depend on the light level used in the experiment and the value of L_p obtained will be strictly valid only for that light level. Note that if, under illumination, the values of n and p (and also their mobilities) are of comparable magnitude, the measured value of L_p will describe an ambipolar diffusion length.

In our experiments, holes can be created in either a field-free region or a field region, depending on the width of the depletion layer shown in Fig. 1. Strictly speaking, we measure a collection length that then must be determined to be either field independent or field assisted. Condition (5) must be met if our measurement is to reflect a truly thermal, field-independent diffusion length. We will discuss this point as it relates to specific experiments.

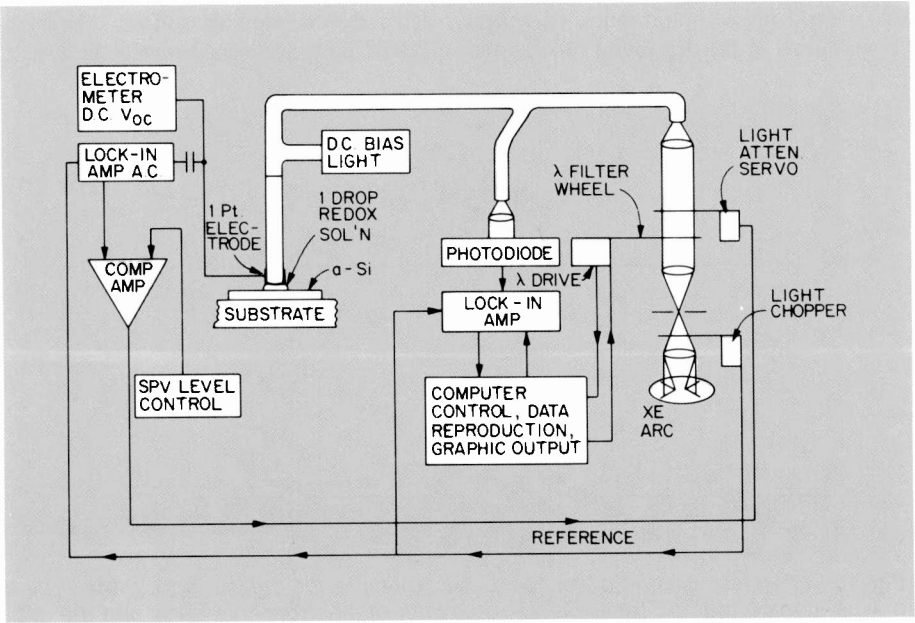

Fig. 2. *Diagram of the surface photovoltage apparatus and a liquid Schottky barrier.*

Sample preparation and apparatus

The samples were prepared by decomposition of SiH_4 in a dc glow discharge at substrate temperatures (T_s) of 330 and 240°C. A 200-angstrom-thick n^+ layer was first deposited on a polished stainless-steel substrate (to form an ohmic contact), followed by a layer of undoped material of thickness 2.0 to 4.0 μm. The first measurements of SPV due to the drift of holes to the surface were done with a Kelvin probe operating in vacuum.[5,6] The Kelvin probe[7] is an instrument that measures the change in surface potential without actually touching the surface. However, it is very susceptible to mechanical noise, and it is slow. Furthermore, the requirement of a vacuum environment to reproduce surface conditions slows the measurement even more. However, as the validity of the method became established and it became more and more a part of the solar-cell program, improvements in technique followed rapidly. Specifically, the development of a liquid contact[8] that produced a Schottky barrier eliminated at one stroke the need for both the unwieldy Kelvin probe and the bothersome vacuum environment. In addition, data acquisition and graphics display were computerized and made programmable, and fiber-optics were incorporated for the purpose of controlling and measuring the light intensity. The system currently in use is illustrated schematically in Fig. 2 and incorporates a number of noteworthy details.

Light sources

Two independent light sources are used. One is an appropriately filtered tungsten lamp that provides a "dc bias" illumination up to a level of about one sun (10^{17} photons/cm^2/s) and sets both the SPV magnitude and the light-intensity level of a particular experiment. The other is a chopped monochromatic light of variable wavelength (from a xenon lamp and interference filters) that provides much smaller

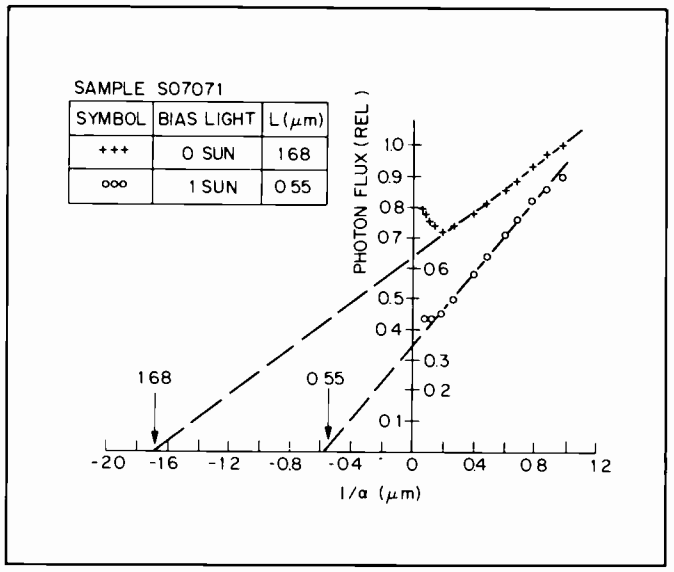

Fig. 3. *Typical plots, at 0.0 and 1.0 sun, or relative photon flux versus reciprocal optical-absorption coefficient in undoped a-Si:H. Values of L_p are as indicated at the abscissa intercepts.*

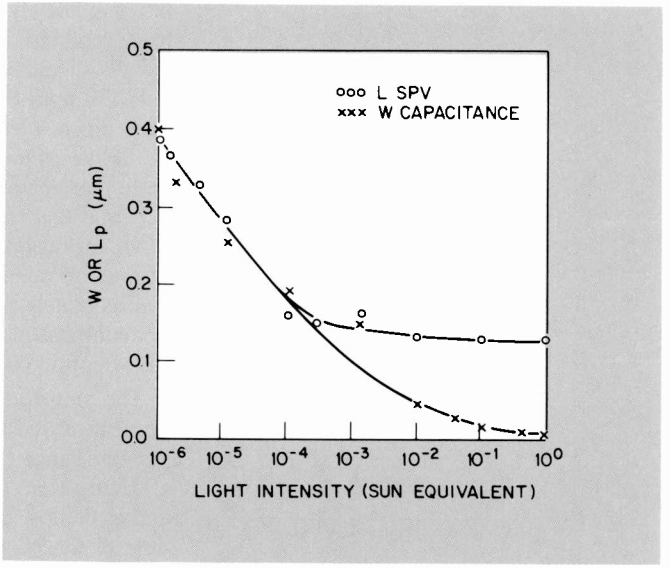

Fig. 4. *Diffusion length L_p as measured by SPV, and surface-barrier depletion width W as measured by junction capacitance—both terms are given as functions of light intensity.*

intensities and furnishes the "small signal" actually used in the measurement. Both light sources are separate, independently measured and controlled, and the light is brought to the sample by fiber optics.

Photovoltage pickup

The surface band-bending is due to, and the photovoltage is picked up by, a liquid oxidation-reduction (redox) solution[9] in contact with the semiconductor surface and platinum film counter-electrode all contained within the narrow gap between the end of the light guide and the illuminated surface. Only one drop of liquid is required, held in place by surface tension.[10]

Lock-in amplifier

The ac (small-signal) component of the surface photovoltage is amplified by a lock-in amplifier whose output is compared to an SPV level-control voltage. The difference or error signal is used to operate a servo-controlled light attenuator in the optical path of the monochromatic light. In this way, the SPV is automatically kept constant as the wavelength is changed (this is the condition of Eq. 1).

Microcomputer

The entire experiment, including the setting of the various light levels, the wavelength indexing, the data acquisition, the conversion to the photon density, the plotting of the results, and data reduction and storage is controlled by a microcomputer.

The complete procedure for the measurement of L_p is currently carried out in about 15 minutes with negligible noise levels.

Experimental results and discussion

Typical plots of I versus $1/\alpha$ for bias light intensities of 0.0 and 1.0 sun respectively are shown in Fig. 3 for a sample that is 2.5-μm thick and is prepared at 290°C. The constant photovoltages used for these (and subsequent) curves were about 500 mV or less. The *total* surface band-bending could be obtained by illumination with a high-intensity xenon arc that produced saturated, (complete) band flattening. A straight line is obtained for $1/\alpha < 3$ μm with intercepts at $L_p = 1.68$ μm and 0.55 μm for light intensities of 0.0 and 1.0 sun, respectively.

As mentioned earlier, the surface photovoltage method measures the total collection length for minority carriers, that is, the length due to drift in a field-free region, plus field-enhanced collection in the depletion region of the surface barrier. However, these can be readily separated either by measurements at high light levels, which strongly compress the depletion width, or by independent capacitance-voltage (C-V) measurements of the depletion width. For example, the difference between the two curves in Fig. 3 is due to the fact that at 0.0 sun the surface-barrier depletion width is large and L_p represents, at least in part, a field-assisted drift length, while at 1.0 sun the depletion layer width has collapsed to about 0.02 μm, so that the L_p of 0.55 μm is due almost totally to the thermal drift of holes.

Figure 4 perhaps illustrates this point more strikingly. Here we have plotted, on the same scales, L_p as measured by SPV and the surface-barrier depletion width as measured by junction capacitance—both as a function of light intensity. Note that although the depletion width continues to diminish with increasing light intensity, L_p reaches a value where it flattens and thereafter remains constant with light intensity. The "knee" in this curve clearly distinguishes the region of partially field-assisted L_p and essentially field-free L_p.

Note in Fig. 3 that there is an upturn in the data for very low values of $1/\alpha$, that is, more intensity is needed to produce the same SPV. This is believed to arise from electrons generated in the depletion region and flowing *toward* the surface, reducing the hole current to the surface.[11] This electron current arises because of strong electron-concentration gradients due to a combination of high surface-recombination velocity and high α (low $1/\alpha$).

Some important properties of L_p in *a*-Si:H

By use of the techniques and basic procedures described, we have measured room-temperature diffusion lengths in *a*-Si:H as high as about 2μm. Material of such good quality (recall that the total thickness of

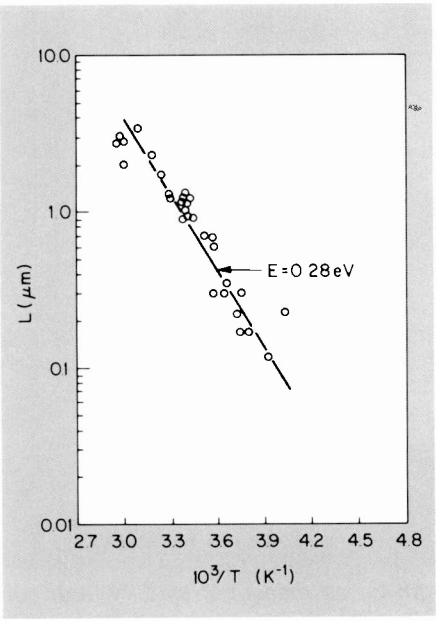

Fig. 5. *Temperature dependence of diffusion length* L_p.

the intrinsic layer in a typical solar cell is about 0.5 μm) is difficult to make consistently at this time and is known to depend on specific conditions of the silane discharge (pressure, geometry, and so on) and a lack of contamination. As research along these lines has continued, some important features of L_p, and properties related to L_p, have come to light. These include estimations of the hole recombination time τ, the degradation of L_p with prolonged illumination, an estimate of typical space-charge densities and the observation of Mott barriers (the Mott barrier, or punch-through barrier, a theoretical model for swept-out metal-semiconductor contacts, is defined as the limiting case in which the epitaxial layer is much narrower than the required depletion layer width; the Mott barrier is more sensitive to voltage variation than the Schottky barrier).

We can estimate the hole recombination time τ as follows: The independence of L_p with light intensity at high illumination levels (Fig. 4) indicates that we are dealing with a field-independent diffusion length given by

$$L = (\mu_c \tau kT/e)^{1/2} \qquad (6)$$

where μ_c is the conductivity mobility for holes. Hence, for L of approximately 0.5 μm, $\mu_c\tau$ is approximately 10^{-7}cm^2/V. For conduction in localized states not far from the mobility edge, values of μ_H/μ_c, where μ_H is the Hall mobility, have been estimated to be 0.1[12]; for conduction in the extended states this ratio might be expected to be somewhat higher. Measured values[17] of μ_H in heavily boron-doped a-Si:H have been reported to be approximately 10^{-2} cm^2/V s, and in lightly boron-doped a-Si:H (70 ppm B_2H_6) recent measurements have given a value of about 10^{-1}cm^2/V s.[14] If we assume that the latter value is more representative of that in undoped a-Si:H and that hole conduction takes place either in localized states not far from, or within, the valence band, then a value of τ approximately equal to 0.1 μs is obtained. For comparison, good-quality crystalline Si has a τ approximately equal to 10 μs.

The temperature dependence of L_p has been measured over a rather limited temperature range (limited at the high end by a decrease in the surface-barrier height, and at the low end by increasing response time of the photovoltage[15]) and is shown in Fig. 5. L_p is seen to increase as temperature increases and can be characterized by an activation energy of 0.28 eV. However, an almost total lack of independent experimental data concerning μ_c and τ prevents us from any further meaningful analysis of these data. In any event, the effect is not crucial to solar-cell operation since the temperature does not change much during cell operation.

On the other hand, maintaining solar-cell efficiency under prolonged illumination at intensities near 1 sun clearly *is* important. Under such illumination the efficiency of some cells is known to degrade. Although many factors go into determination of efficiency, and the change of any one of these factors may result in cell degradation, the diffusion length is certainly an important matter. Independent measurement has shown that in some of these samples the diffusion length may indeed degrade under illumination. This is often accompanied by an increase in the space-charge density resulting from light-induced centers near the midgap energy whose normal action is to trap holes, reducing the diffusion length. These centers are thought to be due to structural defects, which may involve trace contaminants. The effect is generally reversible by annealing at elevated temperature.

The space-charge density can be inferred from the light-intensity dependence of L_p by calculating the influence of the space-charge field on the diffusion of holes at low intensity (as in Fig. 4). When such calculations are made (within the commonly assumed framework of the thermionic emission-diffusion theory of the Schottky barrier) the experimentally determined values of L_p at low light levels (field-enhanced plus thermal diffusion) and high light levels (thermal diffusion alone) enable us to determine the space-charge density, ρ, uniquely. In the past such determinations of ρ were customarily made by capacitance measurements, often complicated by, for example, a frequency dependence. Here, it is all done optically. Typically, space-charge densities for L_p of about 0.5 μm are approximately 5×10^{15}/cm^3. For cases of very high L_p (1.5 to 2.0 μm), space-charge densities of less than 10^{14}/cm^3 have been observed. Secondary ion-mass-spectroscopy analysis shows that such low values of ρ cannot be due to low contamination alone, since oxygen and carbon levels are approximately 10^{19}atoms/cm^3, and many other impurities are present in the 1- to 10-ppm range. It must involve compensation either by p-type dopants or structural defects.

Part of the analysis described in the above paragraph leads to the necessity for invoking hole-trapping as the holes traverse the space-charge region, thus increasing the positive space charge. Such space-charge effects were already known from other experiments on a-Si:H solar cells. In some samples in which ρ is very small we have found that the process of carrier trapping is reversed, that is, instead of holes becoming trapped in the space-charge region, electrons are trapped, thus leading to a decrease in positive space charge as the light level increases. This process results in widening of the space-charge region to, in a few cases, the entire width of the sample. This behavior in a-Si is similar to that seen in crystalline materials and insulators and is characteristic of Mott barriers. In ordinary silicon devices this can be accompanied by punch-through. Thus, although Mott barriers are generally undesirable in ordinary silicon diodes, in a-Si:H solar cells they can be very useful; if the field extends completely through the body of the cell it means that the current flow will always be field-assisted, and thus will strongly enhance the collection of the photogenerated carriers.

Conclusion

We have presented here a description of a fast and direct method for measurement of the minority-carrier diffusion length, L_p, in a-Si:H. Currently, the method acts as the primary ongoing monitor of material quality in the a-Si:H solar cell program, and supplies the initial material evaluation to the people growing the a-Si:H films. In addition, we have used measurements of L_p to estimate space-charge densities, minority-carrier lifetimes, and to study optical instabilities in a-Si:H.

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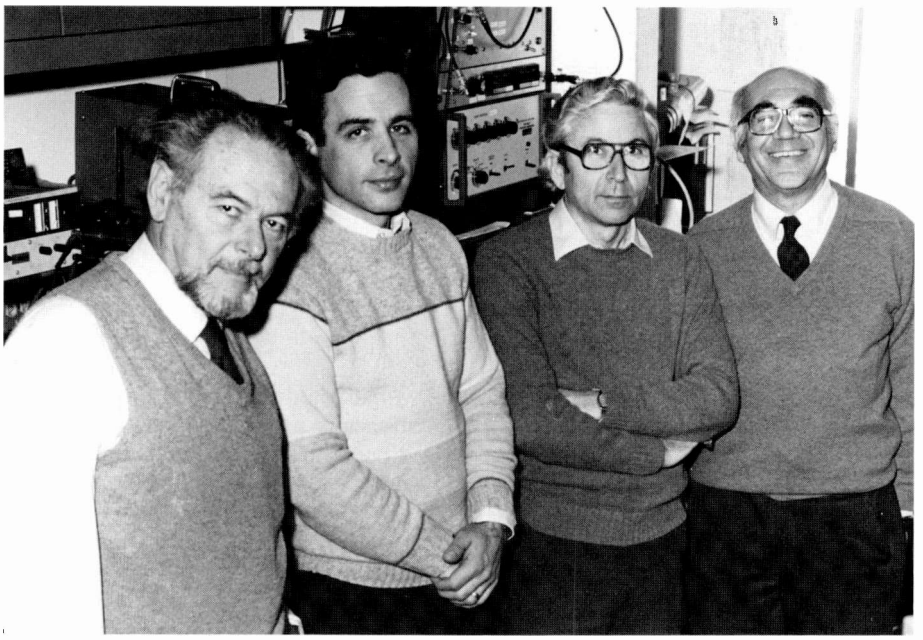

Authors (left to right) Moore, Szostak, Goldstein, and Dresner.

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Chemistry of silane discharges

By analyzing reaction pathways and the kinetics of the decomposition of gaseous silane in a glow-discharge reaction, RCA researchers are understanding how thin films of amorphous hydrogenated silicon—a critical material in solar cells—are formed.

Hydrogenated amorphous silicon has attracted commercial and research interest in recent years for its use in a wide range of electronic applications, especially photovoltaic solar cells. RCA Laboratories pioneered the use of amorphous-silicon solar cells,[1] and has recently announced a record conversion efficiency of over 10 percent for these devices,[2] reinforcing commercial interest in this material.

Amorphous silicon is a desirable material for photovoltaic cells for several reasons: First, the abundance of the raw material makes large-scale deployment for terrestrial use feasible; second, optical absorption in the material occurs near the value (1.5 eV) at which the maximum theoretical conversion efficiency is expected; and lastly, the carrier mobility and lifetime are sufficiently large to permit efficient collection of the light-generated carriers.

The desirable electrical and optical properties of amorphous silicon are due to the incorporation of hydrogen in the solid. Ordinarily, amorphous silicon prepared without hydrogen, for example by sputtering with argon or electron-beam evaporation in a vacuum, has unsatisfactory electrical transport properties because many unsatisfied bonds arise from the random network of silicon atoms, thus creating a high density of localized electron-energy levels.

The most satisfactory method for depositing amorphous-silicon films with hydrogen incorporated in the solid is the plasma decomposition of silane (SiH_4), a gas whose boiling point is −111.9°C. Silane reacts explosively with oxygen and is readily decomposed by heat, light, hydrogen-atom attack, and by gas discharges. The thermal decomposition of silane at temperatures of 1000°C and higher is used in the semiconductor industry to deposit thin layers of silicon on insulators for integrated circuit devices.[3] In this case, of course, no hydrogen is incorporated and the silicon grows as a crystalline film. However, when silane is decomposed in a low pressure (0.1 to 1.0 torr) glow discharge excited by either dc or rf electric fields, amorphous hydrogenated silicon films can be deposited on heated substrates placed in contact with the glow. The plasma decomposition method of film formation is desirable for several reasons. It is relatively easy to coat large areas uniformly, even if the films are only 100 angstroms thick. The process is easily controlled by adjusting the power dissipated in the plasma, and it is not sensitive to temperature since the energy initiating the reaction is much greater than the substrate temperature.

Although the role of hydrogen in determining the electro-optic properties of the solid is reasonably clear, the details of the mechanism by which film formation occurs during plasma decomposition is only now emerging. In this article we wish to review for the interested reader the various mechanisms by which silane decomposition occurs and give some insight on the manner in which plasma decomposition gives rise to the amorphous-silicon film. We will refer to the solid amorphous-silicon film as $a\text{-SiH}_x$ to denote the variable quantity of hydrogen that may be contained in the solid. The reader who is interested in the electro-optic properties of amorphous silicon is referred to the review articles in the literature.[4–6]

Abstract: *Thin films of hydrogenated amorphous silicon have desirable characteristics for use in large-area, low-cost solar cells. The films are readily deposited from the decomposition of gaseous silane in a glow discharge. A variety of silicon-containing molecules and ions are produced in the energetic glow discharge, and the process by which the film is formed is not well understood. We shall describe how we have used results from earlier studies on the decomposition of silane by several different monoenergetic radiation sources, together with studies we have done on the reaction kinetics of silane glow discharges, to deduce the principal reaction pathways. Many questions remain unanswered, but a clear picture is emerging of how the film is formed. This should aid in the preparation of good quality films for device applications.*

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Glow discharge processes

Glow discharges are used in a variety of applications.[7,8] Probably the most familiar example of a glow discharge is the neon tube, whose characteristic red glow is used for illuminated signs. When a gas at low pressure is ionized by a sufficiently large electric field, the gas becomes conducting and contains numerous ions and neutrals in excited states that emit radiation upon spontaneously relaxing to the ground state. The color of a glow discharge is determined primarily by the type of gas; a silane glow discharge is deep blue. Of course, the walls of a glass tube containing a silane glow discharge would become coated with a solid film resulting from the decomposition of silane. Since the composition and the electrical properties of films deposited from silane glow discharges depends not only on the temperature of the substrate on which the film is formed, but also on the properties of the gaseous plasma, we shall describe the glow-discharge process in sufficient detail to discuss the formation of reactive chemical species.

We will describe the characteristics of a dc discharge in a rather oversimplified way in order to illustrate the essential features. We assume that the discharge is excited between two plane, parallel electrodes a distance d apart and it is confined by suitable walls, as shown in Fig. 1. The discharge consists of alternating dark and light regions. Strong electric fields exist in the dark regions and charged-particle acceleration takes place in these regions. The discharge is excited and maintained by the emission of secondary electrons from the cathode, produced by the bombardment of positive ions accelerated across the cathode dark space. The positive ions are created in turn by electron-impact ionization of the gas molecules in an intensely luminous region, called the negative glow, which is adjacent to the cathode dark space. On the anode side of the negative glow, there is another dark space, called the Faraday dark space, whose width is comparable to the cathode dark space. The charge density in this region is low, but there is a relatively strong electric field present. The Faraday dark space is followed by another luminous region, the positive column, whose intensity is weaker than that of the negative glow. Finally, there is a thin dark space adjacent to the anode.

A striking characteristic of the dc glow discharge is that the cathode dark space, the negative glow, and the Faraday dark space remain unchanged as the distance between the electrodes, d, is changed. As d is made larger, the positive column expands and as d is made smaller it contracts. Returning to our example of the neon illuminating sign, which is made up of long glass tubing formed into letters and graphic shapes, what one sees is a long positive column. The luminous regions contain a high density of charged particles, typically 10^7 to 10^{10} cm^{-3}, but have approximate charge neutrality overall. These regions are called plasmas. An ideal gas at 1 torr and 25°C has a density of 3.5×10^{16} molecules cm^{-3}; therefore, the degree of ionization is quite small—something like one atom in 10^8 is ionized. The relatively low-energy discharges we are concerned with are sometimes called cold plasmas; the massive positive ions have an energy distribution characterized by a temperature that is typically 500 K, whereas the electrons have a distribution typified by a temperature ranging from approximately 10,000 to 100,000K (1 to 10 eV). Clearly, the two charge distributions are not in thermal equilibrium with each other; the electrons have a much higher thermal velocity, but the drift motion in an electric field is governed by ambipolar diffusion, that is, the charged-particle motion is coupled. It is this coupled motion that gives plasmas special characteristics, such as plasma waves and oscillations, which we need not specifically consider here.

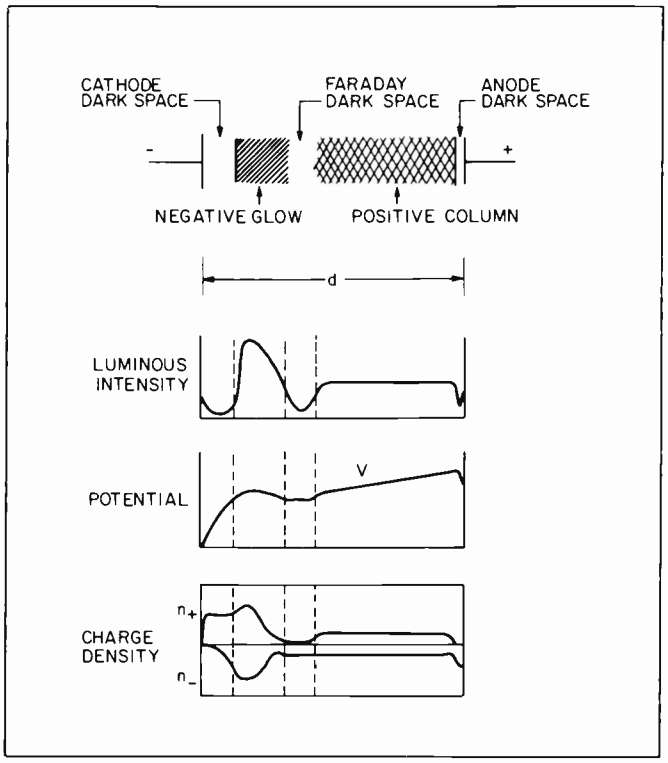

Fig. 1. The dc glow discharge excited between two parallel electrodes, which are a distance d apart. The various luminous and dark regions are indicated and the luminous intensity, the potential (V), and the positive (n_+) and negative (n_-) charge densities as a function of position between the electrodes are schematically illustrated.

Energetic electrons are required to ionize the gas, but in silane the ionization process may be accompanied by dissociation, as illustrated by the principal, low-energy ionization processes of silane shown below.

$$\begin{aligned}
SiH_4 + e^- &\longrightarrow SiH_4^+ + 2e^- && E_i = 11.7 \text{ eV} \\
&\longrightarrow SiH_3^+ + H + 2e^- && E_i = 12.3 \text{ eV} \\
&\longrightarrow SiH_2^+ + H_2 + 2e^- && E_i = 11.9 \text{ eV} \\
&\longrightarrow SiH^+ + H_2 + H + 2e^- && E_i = 15.3 \text{ eV} \\
&\longrightarrow Si^+ + 2H_2 + 2e^- && E_i = 13.6 \text{ eV}
\end{aligned}$$

In addition to these reactions, required to generate the ion-electron pairs needed to sustain the discharge by providing the needed conduction of current through the gas, there are additional neutral fragments produced by electron impact, at even lower energies.

$$\begin{aligned}
SiH_4 + e^- &\longrightarrow SiH_3 + H + e^- && E_d = 4.04 \text{ eV} \\
&\longrightarrow SiH_2 + H_2 + e^- && E_d = 2.16 \text{ eV} \\
&\longrightarrow SiH + H_2 + H + e^- && E_d = 5.7 \text{ eV} \\
&\longrightarrow Si + 2H_2 + e^- && E_d = 4.2 \text{ eV}
\end{aligned}$$

These neutral fragments contain unpaired electrons (a free radical in chemical terminology) and/or lone-pair occupied orbitals and are thus quite reactive. These fragments may react with the large background of unreacted silane to produce the higher silanes Si_nH_{2n+2} where n is an integer greater than 1, which are known stable compounds, or they may survive until a surface is encountered at which they surely recombine to become incorporated into a film.

Finally, there are the processes of ion-molecule reactions that result in larger ion clusters or which may produce other reactive species. For example, the reaction

$$SiH_2^+ + SiH_4 \longrightarrow SiH_3^+ + SiH_3 \qquad (1)$$

produces both an ion (SiH_3^+) and a free radical (SiH_3).

Clearly, the plasma regions—with all the excitation, dissociation and ion-molecule reactions that occur—are rich sources of reactive hydrogen-containing silicon fragments. To some extent, the experimentalist can control the mix of fragments and their energies by varying the gas discharge operating conditions—pressure, gas flow, and discharge current. It is, however, a tenuous control. At this stage, our knowledge of the effects of different discharge-operating conditions on the chemical content and energies of the gaseous plasma is quite incomplete.

Nevertheless, great progress has been made and our studies of the kinetics of silane decomposition and gaseous-product formation, by use of barometric and mass spectroscopic measurements, have enabled us to form a general outline of the important processes. We have made extensive use of earlier kinetic studies of the decomposition of silane, which employed various monoenergetic sources that are thus easier to model. The kinetics and mechanism of the decomposition are discussed in the next section.

Kinetics and mechanism of SiH_4 decomposition

The unimolecular decomposition of silane can be accomplished through a variety of radiation mediums. Excitation by monoenergetic sources has yielded the greatest amount of information on the decomposition process simply because the mechanisms and kinetics proceed from a fairly well-defined and narrow band of excited states. To gain an understanding of the mechanisms for the decomposition of silane, let us consider the results of irradiating silane with three different monoenergetic sources—ultraviolet radiation, infrared photons, and gamma-rays.

Let us first consider the decomposition of silane where small amounts of mercury (Hg) vapor are mixed in a reaction chamber with silane, and the mixture is exposed to 253.7-nm radiation.[9] The decomposition occurs via the excitation of mercury to a long-lived excited state, and subsequent collisonal energy transfer to silane, as given by reaction (2).

$$Hg\ (\text{excited state}) + SiH_4 \longrightarrow SiH_3 + H + Hg \qquad (2)$$

Radiation of this wavelength carries 4.9 eV of energy and leads exclusively to the production of SiH_3, the silyl radical; primarily because of the known reaction of H, the other decomposition product is[10]

$$H + SiH_4 \longrightarrow SiH_3 + H_2 \qquad (3)$$

Thus, for every silane molecule decomposed by the primary process given by (2), a second molecule is decomposed by the H atom, and two SiH_3 units are produced. These silyl monoradicals react with each other via reactions (4) and (5)

$$2\,SiH_3 \longrightarrow Si_2H_6 \qquad (4)$$

$$2\,SiH_3 \longrightarrow SiH_2 + SiH_4 \qquad (5)$$

to yield the stable gaseous product disilane, Si_2H_6, via (4), or a second intermediate SiH_2, the silylene diradical. The known reaction of SiH_2 with silane

$$SiH_2 + SiH_4 \longrightarrow Si_2H_6 \qquad (6)$$

is known as an insertion reaction;[11] that is, the SiH_2 unit inserts itself into an $\equiv$ Si–H bond, yielding $\equiv$ Si–SiH_2–H. Thus, we see that the decomposition of silane via 4.9-eV radiation leads to the primary intermediate SiH_3 via reaction (2), a reaction whose energy barrier is 3.9 eV.[12]

But what if one increases the radiation energy? Do new decomposition pathways become available? To answer this question, the direct decomposition of silane by vacuum-uv radiation at 147 nm was investigated.[13] Radiation of 147 nm carries 8.5 eV of energy, and thus can excite silane to a much higher state than that attained during the Hg-photosensitized decomposition. The results of this investigation were that silane decomposes via two primary processes, as given by reactions (7) and (8).

$$h\nu + SiH_4 \longrightarrow SiH_2 + 2H \qquad (7)$$

$$h\nu + SiH_4 \longrightarrow SiH_3 + H \qquad (8)$$

The energy barrier for reaction (7) is 6.74 eV and that for (8) is 3.9 eV, as mentioned earlier. But how were these two mechanisms sorted out, given that both the SiH_3 and the SiH_2 give rise to disilane, via reactions (4) and (6), respectively? The chemical technique used to differentiate between the two processes is the introduction of a free-radical scavenger into the silane. Nitric oxide, NO, is a known free-radical scavenger that is strongly reactive towards SiH_3 yet virtually inert to the singlet-state SiH_2 chemical species.[14] Thus, when NO is introduced into the reaction chamber during photolysis, the yield of the disilane product is seen to decrease to some finite lower limit,[13] demonstrating that some of the disilane is made via the NO-scavengeable SiH_3 intermediate, and some via the nonscavengeable SiH_2 intermediate. Appropriate treatment of the results of the radical-scavenging experiments permitted assignment of the fractional extents of primary processes (7) and (8) for the vacuum-uv photolysis as 0.83 and 0.17, respectively.[13] Similar scavenging experiments for the Hg-photosensitized decomposition showed complete suppression of the disilane product[14] consistent with reaction (2) as the mechanism.

Lowering the radiation energy below the threshold for the SiH_3-producing reaction discloses a further possible decomposition mechanism. Recently, silane was decomposed by IR multiphoton absorption[15] from a CO_2 laser, the radiation energy being 0.12 eV. The primary decomposition was shown to proceed almost exclusively via reaction (9),

$$nh\nu + SiH_4 \longrightarrow SiH_2 + H_2 \qquad (9)$$

which has an energy barrier of 2.4 eV. This reaction was distinguished from that given by (7), in which the SiH_2 is also made, in that none of the disilane product was scavengeable. If, in fact, reaction (7) were the decomposition process, one would expect a further generation of SiH_3 via reaction (3) of H with SiH_4 and subsequent formation of disilane via (4). Reaction (9) is also the known decomposition pathway for the pyrolysis of silane,[16] as one might well expect.

At this point, we have identified two major silicon-hydride

intermediates, both radicals, which are formed by the decomposition of silane—SiH_3 and SiH_2. However, we have not yet considered ion generation and reaction. For this, we turn to γ-ray radiolysis. Experiments[17] using 100-eV γ-rays from Co^{60} showed that, in addition to the higher energy dissociation pathways given by reactions (6) and (7), two other ion-generating mechanisms were occurring, as given by reactions (10) and (11),

$$\gamma\text{-ray} + SiH_4 \longrightarrow SiH_3^+ + H + e^- \qquad (10)$$

$$\gamma\text{-ray} + SiH_4 \longrightarrow SiH_2^+ + H_2 + e^- \qquad (11)$$

The ion SiH_2^+ was shown to be the most abundant, and its known reaction with silane[18] is given by reaction (1), mentioned earlier.

The SiH_3^+ ion reactions in the gas phase simply yield larger ions, $Si_xH_y^+$; and SiH_3^+-wall reactions are classic recombination reactions. Thus, for the γ-ray radiolysis, the primary ion-molecule reactions act to increase the concentration of the SiH_3 radical, via reaction (1). Of the three monoenergetic sources of silane decomposition discussed, the γ-ray radiolysis is the closest to the plasma decomposition of silane by electron impact, wherein both radicals and ions are known to be generated.

A summary of these various processes is contained in Fig. 2. Two points stand out as significant. First, the decomposition pathway available to the excited-state silane molecule is very much dependent on the energetics of the exciting medium. Second, regardless of the dissociation pathway, the principal intermediates that form the stable products are the monoradical SiH_3 and the diradical SiH_2. Thus, an integral part of understanding the silane-glow-discharge decomposition lies in understanding the energetics of the electron impact, as well as what reactions can occur.

Film formation

The process by which the a-Si:H_x film forms does not appear to directly involve the presence of ionized gas species; the measured ion flux at the substrate is simply too low to account for the observed growth rate. Instead, the predominant film-forming species appears to involve free radicals such as the monovalent SiH_3 radical. Other methods of a-SiH_x film formation, such as homogeneous chemical vapor deposition, are initiated by relatively low-energy exchanges and appear to proceed via the SiH_2 radical.[19] In contrast, the relatively energetic plasma ($>$ 5-eV) electrons and H atoms create primarily SiH_3 radicals, which we suggest dominate a-SiH_x film formation.

Evidence of the involvement of SiH_3 in the film-forming process again comes from experiments at RCA Laboratories in which nitric oxide is added to the plasma. Mass spectroscopic measurements show that the formation of the higher silanes, such as Si_2H_6, is lowered dramatically by its addition. Instead polysiloxanes are formed in a chain reaction that consumes SiH_3. In fact, the presence of as little as 2.5-percent nitric oxide completely halts the formation of the a-SiH_x film.

It is appropriate to view the process of film formation as one which involves more than a single gaseous species and which includes both homogeneous and heterogeneous reactions. The homogeneous gas-phase reactions are continually driving the composition of the gas to higher and higher molecular-weight silane polymers. At the same time, these polymers are reacting at the surface. The SiH_3 radical reacting at the surface eliminates one atom of hydrogen for each silicon-silicon bond formed. In

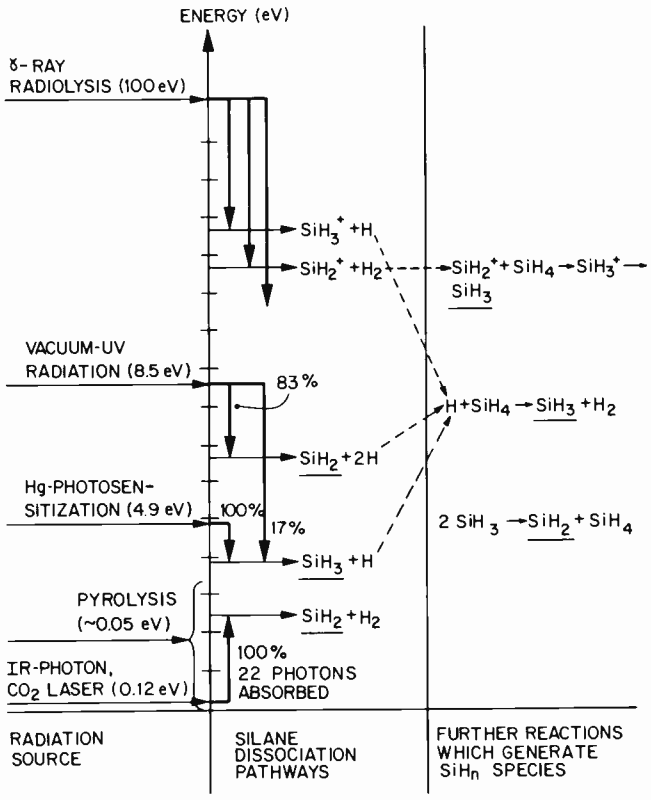

Fig. 2. Dissociation pathways observed for the decomposition of silane via various radiation media. The energy scale relates the input energy of the radiation source (shown on the left side of diagram) with the observed dissociation pathways (the center of the diagram). The percentages refer to the fractional extent of a specific process as compared with the other observed processes for that radiation-decomposition scheme. The further reactions listed on the right side of the diagram are not scaled to energy. Note that most of the processes lead to either SiH_2 or SiH_3, the prime candidates as film-forming intermediates.

contrast, the higher-molecular-weight polymers, which usually only have a single reactive site, eliminate a single hydrogen but bring a large number of SiH_2 units into the solid. Since subsequent surface-elimination reactions are limited by steric factors, the result is the incorporation of larger amounts of hydrogen in the solid. Polymer attachment results in the formation of "internal surfaces" lined with hydrogen. These surfaces are reactive and can be pathways for the diffusion of gases and so on, into the material. This results in a semiconductor with undesirable electrical and optical properties. Thus the composition and structure of the solid depends on the reaction rates and details such as gas flow rate, residence time, and so on. Figure 3 presents a schematic representation of these processes.

Summary

We have shown that the decomposition of silane in a glow discharge, although a good method for the preparation of large-area thin-film a-SiH_x solar cells, is a most complex chemical system. The energetic plasma environment allows the production of many possible film-forming intermediates. Our kinetic studies and our analyses of reaction mechanisms have enabled us to deduce the most important intermediates. Future studies will

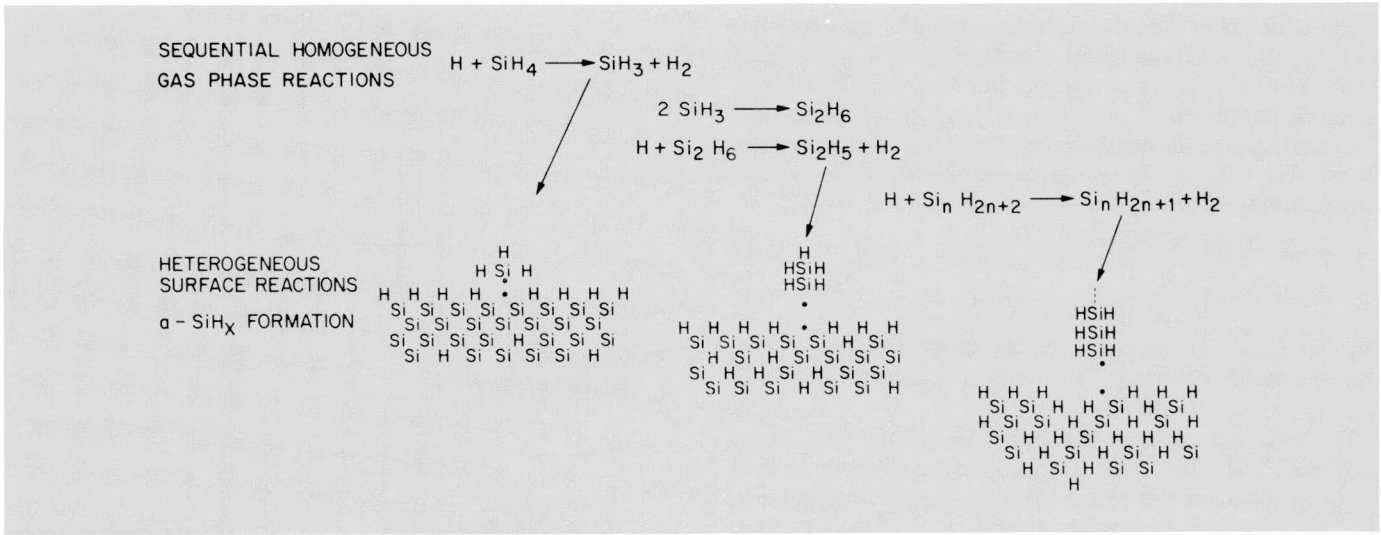

Fig. 3. A schematic illustration of the chemical reactions that take place during the plasma decomposition of silane and that lead to the formation of an *a*-SiH_x film. The energy dissipated in the plasma initiates a series of homogeneous gas-phase reactions resulting in the formation of higher-molecular-weight silane polymers. Simultaneously, heterogeneous surface reactions occur when the free radicals produced in the latter reactions encounter surfaces. The relative rates of these homogeneous and heterogeneous reactions govern the composition, structure, and properties of the resulting film.

further clarify the relative importance of the various possible film-forming intermediates as well as investigate the heterogeneous surface reactions. A clear understanding of the discharge chemistry will enable a more intelligent approach to the process design.

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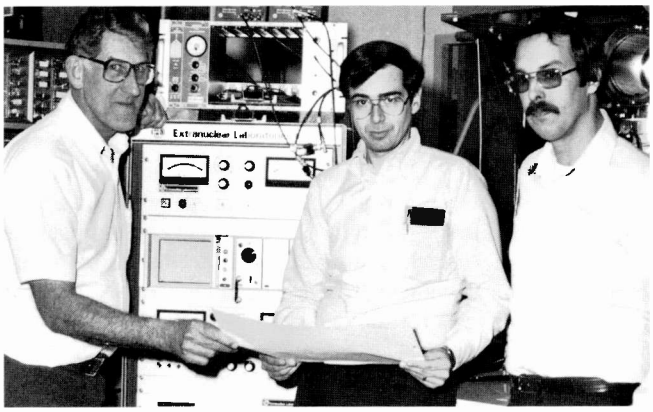

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A.J. Stranix | A.H. Firester

Sunshine in the Garden State—Solar-energy applications

RCA and the Public Service Electric and Gas Company collaborated on a study to determine the feasibility of solar-energy power generation in New Jersey.

The State of New Jersey uses 59 billion kilowatt-hours of electrical energy each year. However, in each year it also receives 60 times that much solar energy. Were we able to convert and store this energy with no losses, the solar energy falling on only 1.5 percent of the area of the Garden State could supply the electrical needs of the entire state. Lossless conversion and storage devices are not known, but for almost ten years RCA Laboratories scientists have researched materials and devices for the efficient and cost-effective conversion of light to electricity. The fruits of that labor are nearly complete in the form of the monolithic series-connected thin-film amorphous-silicon photovoltaic (*a*-Si PV) panel.

The RCA monolithic series-connected *a*-Si PV panel is anticipated to be both the cost and performance leader in the field of flat-plate photovoltaic modules in the coming decade. What makes this particularly exciting is that these modules will be able to play a role in the generation of grid-connected electricity in the United States. Earlier studies had indicated that, to do this, the cost of the photovoltaic modules would have to be less than $0.50 per peak watt, the cost of the total system would have to be approximately $1.00 to $1.50 per peak watt, and the device efficiency would have to equal or exceed 10 percent. None of these earlier studies, however, were actually performed by an electric utility nor were these studies done for future utility scenarios in which the utilities had already converted their generating capacities from intensive use of the petroleum fuels to the non-petroleum, more economical energy sources. Furthermore, none of these earlier studies were based on system designs that exploited the unique advantages of the RCA monolithic series-interconnected *a*-Si PV panels.

Abstract: *During the last decade, considerable attention has been given to terrestrial applications of photovoltaics (PVs) as a source of electricity. Most solar installations have been small, at remote locations, or in the sunbelt area. During this period, RCA Laboratories has conducted Research and Development work on amorphous-silicon (a-Si) thin-film PV cells. To better understand the technical and economic aspects of the application of a-Si PVs in New Jersey, a joint study was performed by RCA and the Public Service Electric and Gas (PSE&G) Company of a long-range PV application in the PSE&G electric system.*

Traditional system-planning models for capacity-reliability evaluation and production-cost simulation, with appropriate modifications to account for the unique energy-producing features of PV generation, are derived from calculations of the amount of conventional capacity that can be replaced by PV installations. The energy value of PV generation is based on the system-production cost savings resulting from the load-reduction effect of PV output. Based on capacity and energy values, the break-even capital costs of PV generation are calculated to be in the range of $1000 to $1350 (1982 dollars) per peak kilowatt, depending on the degree of PV capacity penetration. The higher the penetration, the lower the required break-even cost.

Based on a conceptual design of a 50-megawatt central-station-type PV power plant, RCA estimated that, for long-range applications in the period from 1990 to 2000, its installed cost can be lowered to $1000 per peak kilowatt (1982 dollars). If such a cost goal is attainable, then PV would provide an economically competitive, fuel-free intermediate/peaking generation alternative and, therefore, should be seriously considered in future utility capacity-expansion plans.

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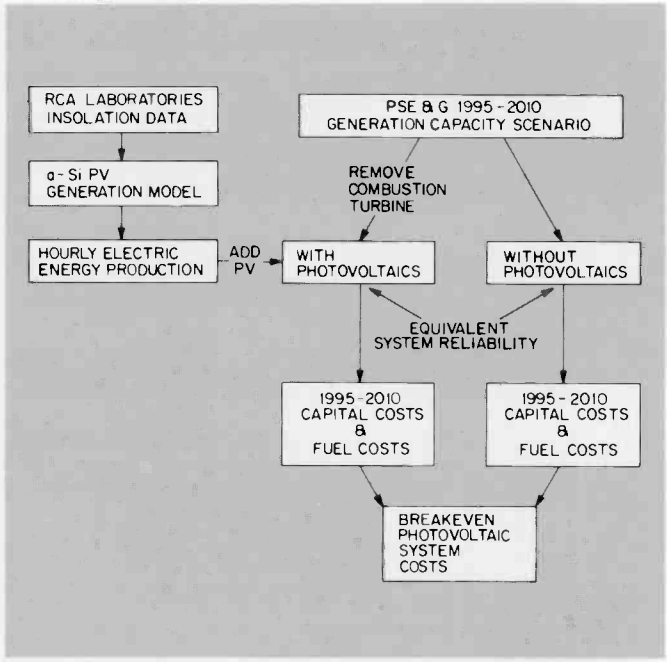

Fig. 1. Study methodology. This simulation study is based on the actual insolation data taken at RCA Laboratories, and the generation-capacity scenario planned by PSE&G. These two inputs are combined to yield a break-even value for a photovoltaic power plant based on traditional utility evaluation methods.

As part of our forward planning, and to address deficiencies in earlier studies, RCA in a joint project with the Public Service Electric and Gas (PSE&G) Company of Newark, New Jersey performed an economic evaluation of PV plants in the PSE&G system. The purpose of the study was to assess the long-range economic potential of applying PV generation in a large electric-power system. The project called for the use of actual New Jersey insolation (sun-ray exposure) data, conversion to electricity based on the RCA monolithic *a*-Si panel characteristics, and analysis by PSE&G using their own utility system planning and evaluation techniques.

This study and its results form the basis of this paper. Figure 1 is an overview of the methodology used in the study. The first step was to analyze the insolation data collected by RCA during one year. These data, along with the characteristics of a conceptual *a*-Si PV generation plant, were reduced to expected hourly electric-energy production. These expected energy-production values were used in a modified loss-of-load expectation analysis to evaluate the impact on utility-system reliability and to determine the capacity credit of PV generation. The expected operation of the PV plant was also used in production-costing analysis to determine the credit in system-production costs attributable to the PV-plant operation. For these analyses, PSE&G developed a long-range generation-expansion reference scenario that included the use of advanced combustion-turbine generation units as one type of future intermediate- or peaking-duty capacity addition that was replaced partially by a PV generation plant. A break-even capital-cost analysis was performed for various PV-generation penetration levels. The analysis took into account both the capacity and energy credits of PV generation. The break-even capital costs were then compared with the projected capital costs of a PV-generating station to determine the potential market penetration of a PV system.

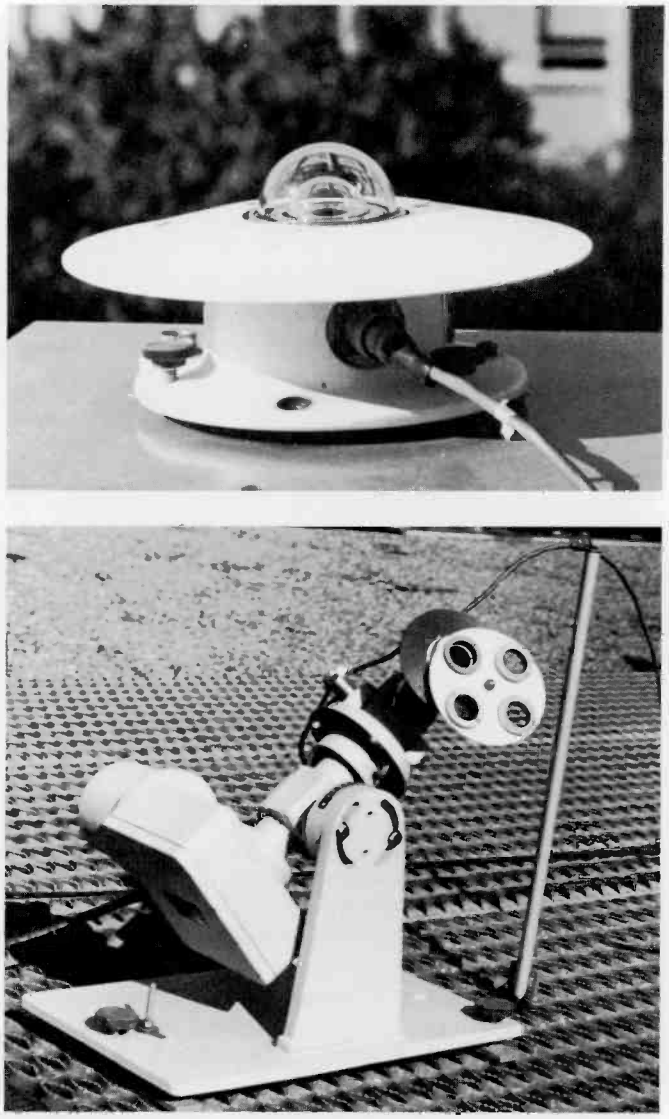

Fig. 2. Insolation measuring instruments. The upper photograph depicts a global pyranometer, which measures the intensity of *all* of the light incident upon it. The lower photograph shows a tracking pyrheliometer. This instrument tracks the sun in its path across the sky and measures only the unscattered light emanating directly from the sun itself.

Insolation analysis

As part of our *a*-Si solar-cell research program, we have monitored the insolation and weather conditions at RCA Laboratories for the past several years. We monitor the direct insolation as well as the global insolation. Direct insolation is monitored with a pyrheliometer mounted on a clock-driven tracking mount, and global insertion is measured by a horizontally mounted pyranometer. These two instruments are shown in Fig. 2. The meteorological conditions that are monitored include temperature, humidity, wind speed, and wind direction. All of these parameters are automatically recorded twice an hour by a test system controlled by a desktop computer. The recorded data is subsequently down loaded into a large computer system for future analysis documentation.

In this study, the insolation and temperature data for the year 1981 were used. Figure 3 shows the raw data for a typical summer day. During the determination of the projected electric-

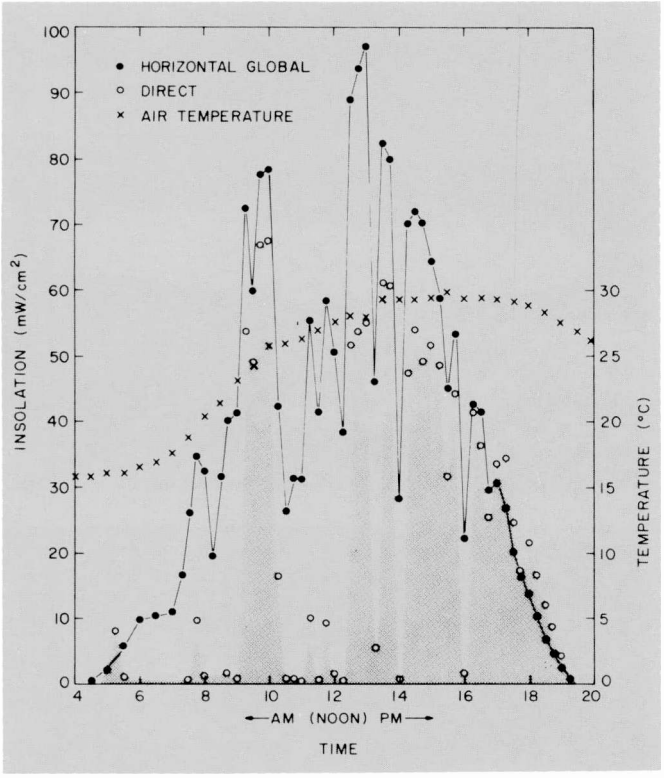

Fig. 3. Insolation and temperature of a typical summer day. Both the total insolation, as measured by a global pyranometer (●●●) and the direct insolation measured by a tracking direct pyrheliometer (ooo) as well as the outside air temperature (xxx) are graphed The random effect of clouds can be seen in fluctuations in the insolation.

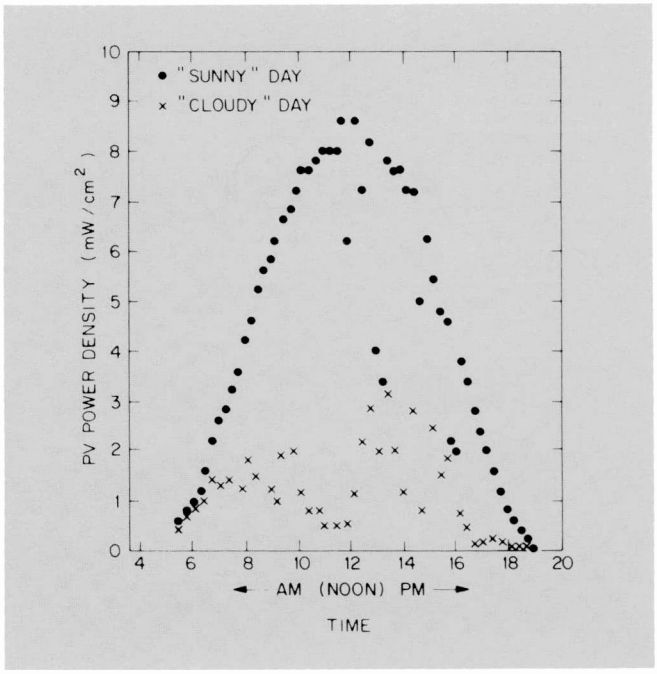

Fig. 4. Insolation bimodal characteristics. These were evidenced by a statistical analysis of the actual insolation data. Whole days and even more frequently, fractions of days could be characterized as "sunny" or "cloudy," depending upon the insolation level observed. The hourly insolation for two days typifying a "sunny" (●●●) and "cloudy" (xxx) condition are shown.

power output, this raw data, consisting of direct and global insolation (intensities I_D and I_G respectively), must first be converted into the total insolation (intensity I_T) that would be incident on a panel facing south and tilted at 40 degrees off the horizontal (latitude at Princeton is approximately 40 degrees). The mathematical formula that performs this conversion is:

$$I_T = I_D \cos \theta_T + (I_G - I_D \cos \theta_H)\,(0.75 + 0.25 \cos \theta_p)$$

where θ_p is the panel tilt angle off the horizontal, θ_H is the angle formed by a direct ray of sun with the vertical, and θ_T is the angle a direct ray of the sun makes with the panel normal. This simplicity becomes obscured when the daily and seasonal motion of the sun, the panel tilt, and the latitude of the panel location are included in the expressions defining θ_T and θ_H.

Sunshine-to-electricity conversion

On a panel, the conversion of insolation intensity to electricity is a function of the temperature and the operating efficiency of the PV panel. We assumed that, at the normal operating-cell temperature of 50° Celsius, the panel converted 10 percent of the incident sunshine into electricity. We modeled the effects of ambient temperature, T_A by the expression for efficiency:

$$\eta(T_A) = 10\% \times [1 - 0.0062\,(T_A - 50°\text{C} + 0.3I_T)].$$

Utility-system input data

Load prediction, system performance, and cost evaluations in PSE&G are approximated by normal distribution curves for the average day for each season. It was, therefore, necessary to present the PV-generation data for each season as a single normal distribution to facilitate evaluation by PSE&G. But, insolation data analysis indicates a bimodal normal distribution, one for "sunny periods" and one for "cloudy periods." Figure 4 illustrates this data pattern for both a sunny and a cloudy day. In combining this bimodal data, the standard deviation of the total PV generation for an average day is adjusted so that its 90th-percentile power value is the same as the 90th-percentile power on a "sunny" day. This adjusted standard deviation tends to reduce the probability of high PV generation and to increase the probability of lower PV-generation values during the summer and, therefore, provides a more conservative approach for assessing the capacity contribution of PV generation. Figure 5 graphically represents the data supplied to PSE&G.

PV capacity-value determination

Capacity value is the capacity contribution the PV-generation equipment makes to the system, expressed as a percentage of the contribution that a conventional generator would make under the same system and load conditions. Prime among these conditions is that the installed capacity and reserve be of sufficient magnitude that the system will have a maximum loss-of-load expectation (LOLE) of one day in ten years. A loss of load occurs when the demand exceeds the system's output.

In determining the PV capacity value, the reference system (with no PV) was expanded so that the LOLE of 0.1 day per year was maintained. To determine this system reliability, the system's predicted loads and their probability of occurrence are approximated by normal distribution curves for each day of peak load season (summer for PSE&G). Then, based on the

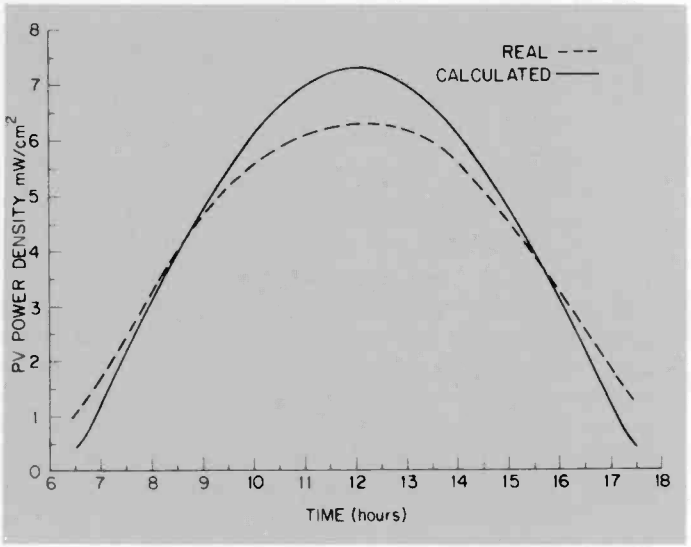

Fig. 5. Average daily insolation. The actual hourly insolation intensity was averaged over all the days in the summer season (---). The calculated curve (——) represents the insolation predicted by our insolation algorithm as fitted to the real data; this calculated data is used to predict the losses in the designed photovoltaic power plant.

generators that are available for service and their respective forced outage rates (historically based random-failure probabilities), the LOLE is calculated.

Next, some of the ACTs (advanced combustion turbine) were removed and PV generation was inserted until the LOLE of 0.1 day per year was again reached and the peak-power rating of the PV was noted. Since the electric load variability used in capacity reliability evaluations is approximated by a normal distribution, the PV-generation data was also represented as a single normal distribution to facilitate the combination of PV generation with the electric load for the capacity reliability analysis. In the analysis of the insolation data, it became clear that the hourly data has a bimodal statistical distribution with data points for "sunny" periods approximating one normal distribution and data points for "cloudy" periods approximating a second normal distribution. To conservatively take into account this bimodality, the standard deviation of the total PV generation for an average day was "adjusted" to make the 90th-percentile power value the same as the 90th-percentile power during a "sunny" period.

This adjusted standard deviation tends to reduce the probability of the high PV-generation values and increase the probability of lower PV-generation values during the summer. However, the overall differences between this adjustment and the direct use of the average day standard deviation is only a few percent. The hourly system load and its distribution is then modified by subtracting the hourly PV average contribution and its distribution. The hourly system load is then further reduced by an assumed effective forced outage rate of 4 percent due to equipment malfunctions in the PV installation. The ratio of the ACT power rating to the PV peak-power rating is the PV capacity value. The result is applicable only to the systems under study and the specific long-range generation expansion postulated. Furthermore, it is inversely proportional to the PV penetration level in the system. Table I shows the resulting capacity values of PV generation in terms of megawatts and dollars per kilowatt at different levels of PV penetration. The capital cost used for combustion turbines is $330 per kW (1982 dollars).

Table I. *Capacity value of photovoltaic (PV) power generation.*

Penetration	PV added (MW)	Capacity[1] value of PV (MW)	Capacity[2] value of PV ($)
2	170	120	232
5	480	300	225
10	910	540	198
15	1350	720	186

(1) In terms of MW capacity of displaced combustion turbine units.
(2) Per kW of PV capacity installed in 1982 dollars.

Table II. *Load model adjustment for incorporating PV output.*

Bi-hour	System[1] load (MW)	PV[2] (MW) generation	Net system load (MW)
08:00–10:00	8130	164	7972
10:00–12:00	8701	219	8482
12:00–14:00	8885	221	8664
14:00–15:00	8721	159	8562
18:00–20:00	8361	67	8294
20:00–22:00	7349	0	7349
22:00–24:00	6772	0	6772
24:00–02:00	5437	0	5437
02:00–04:00	5295	0	5295
04:00–06:00	5558	0	5558
06:00–08:00	6085	64	6021

(1) 1994 peak summer day.
(2) Corresponding to about five percent (5%) penetration.

PV energy-value determination

The PV energy value is the difference in production costs between two systems—one with PV and one without PV—operating under the same conditions and load. The difference comes primarily from the cost of fuel for the conventional generators. The production-cost program is used to simulate the system-generation operations for the two generation-expansion scenarios described above. The load model of the program consists of the annual megawatt peak load and the weekly, daily and bi-hourly per-unit-load shapes. The program automatically develops the system load in megawatts for any bi-hourly period using these per-unit factors. The PV output is incorporated in the corresponding bi-hourly load. Table II shows an example of the production-cost-program load-data modification.

The difference in cumulative present worths of total system-production costs for the two generation-expansion scenarios represents the energy value for the PV installations. The cumulative present worth of production-cost savings and the levelized annual-production-cost savings for PV generation are shown in Table III.

Break-even capital costs and economic feasible penetration

The break-even economic condition occurs when the present worth of all future revenue requirements for the base scenario (without PV) equals that for the alternative scenario with PV. Put in another way, the break-even capital cost for PV with

Table III. *Production cost savings of PV generation—1982 dollars.*

% PV penetration	Amount of PV added (MW)	Cumulative PW[1] of production cost savings (1994-2010) ($ x 10^6)	Levelized annual production cost savings ($/kW-Yr.)
2	170	223	146
5	480	593	145
10	910	942	132
15	1350	1027	121

(1) PW stands for present worth.

respect to an alternative type of conventional generation is determined by the capacity and energy values derived from the simulation results described above. The number of PV installations is varied in simulating the expansion scenario with PV, to evaluate the relationship between the level of PV capacity penetration and its break-even capital cost. The break-even costs and their relationship with the levels of penetrations are shown in Table IV.

This study consolidates the most significant power-plant design parameters to minimize the installed cost per annual kilowatt-hour output for a specific conceptual 50-MW PV power plant, based on the projected performance of thin-film *a*-Si PV panels.

The design is for a PV power plant located in central New Jersey at a latitude of 40 degrees. The design, performance evaluation, and cost analysis was an iterative process in which each design parameter was permitted to vary and its effect on the cost of annual output energy was determined. The performance evaluation predicts the annual output energy from the plant based on actual regional insolation and weather data, projected PV-conversion efficiency, and calculated shadowing and wiring losses. This projected evaluation is based on an algorithm that calculates the level of "ideal" insolation on a surface at any selected time, geographical location, and orientation to the earth's surface. This algorithm is modified to calculate the insolation level for an average seasonal day for the chosen time, geography and orientation as well as other physical design parameters of the plant.

The PV power plant consists of panels arranged into arrays (Fig.6). The arrays are then positioned into rows and columns in a field, and interconnected to the power-conditioning unit (PCU). The manner in which the panels are arranged into arrays, the field position of the arrays, and the field wiring design provide the means by which the criterion of the lowest energy cost is met.

Physical design

The basic building block is a 4-foot × 4-foot RCA monolithic series-connected *a*-Si panel. The cells, which are 4-foot long and approximately 0.4-inch wide, are connected in series with each other at the time of fabrication. This panel, at an efficiency of 10 percent and insolation of 1.0 sun (1.0 sun = 1000 watts/m^2 when the sun's rays are perpendicular to the surface of the earth on a clear day), has an output of 120 volts (dc), 1.25 amperes (max.) and 149 watts (max.).

The panels are arranged into a 36-foot × 8-foot array. This accommodates two rows of nine panels each for a total of 18 panels. The arrays are arranged in rows and columns to minimize land use, wire costs, wire losses, shadow losses and installation costs, and to maximize the energy delivered to the PCU. The field consists of four quadrants with the PCU located in the center (refer to Fig. 6). Each quadrant consists of 117 rows of 40 arrays per row. The rows face south, with a space of 8 feet between rows. Panels are tilted 30 degrees off the horizontal. The selected row spacing and panel tilt resulted in lowest energy costs per the performance evaluation algorithm.

Table IV. *Break-even capital cost of PV generation in 1982 dollars.*

% PV penetration	Amount of PV added	Break-even capital cost
2	170	1350
5	480	1350
10	910	1200
15	1350	1100

Electrical design

The electrical design consists of the array intraconnection, field wiring, and electrical protection. The nine panels in the array are connected in series and the two rows in parallel. This results, for the array, in a nominal dc voltage of 1000 at 2.5 amperes (max.) and 2700 watts (max.)

The forty arrays are connected as a bipolar 2000-VDC field voltage. The result is a three-wire system: +1000 VDC, −1000 VDC, and neutral. Number-4 AWG conductors are used for this connection. Maximum current per row is 50 amperes.

The row outputs are connected in parallel through bus lines to the PCU. Four rows in each of two quadrants are connected to a bus line. The line uses 250 MCM conductors and carries 400 amperes (max.).

Electrical protection is provided for both personnel and equipment. Each row can be isolated from the remainder of the plant and shorted out to permit maintenance. A surge suppressor is connected from the voltage connection of each array to ground. This provides protection from surges caused by lightening or the PCU.

Performance

A measure of performance of a power plant commonly used by utilities is capacity factor. A comparable term in the PV community is "annual kilowatt-hour per installed peak watt." These terms relate to each other as follows:

$$\text{Capacity factor} = \frac{(\text{Annual kWh/W}_p \times 10^3)}{(\text{No. of Hours/Year})}$$

The power-plant design under study has a capacity factor of 19.4 percent, and an annual kWh/W_p factor of 1.7. This compares to capacity factors of 30 to 90 percent for conventional power plants.

The capacity factor of a PV facility is a function of annual insolation and losses. In areas of higher annual insolation, the capacity factor for a PV plant could approach 30 percent. The capacity factor for conventional systems is determined by utility-system economic dispatch and unit availability.

Plant performance

Calculations for predicting plant performance are based on the following equation:

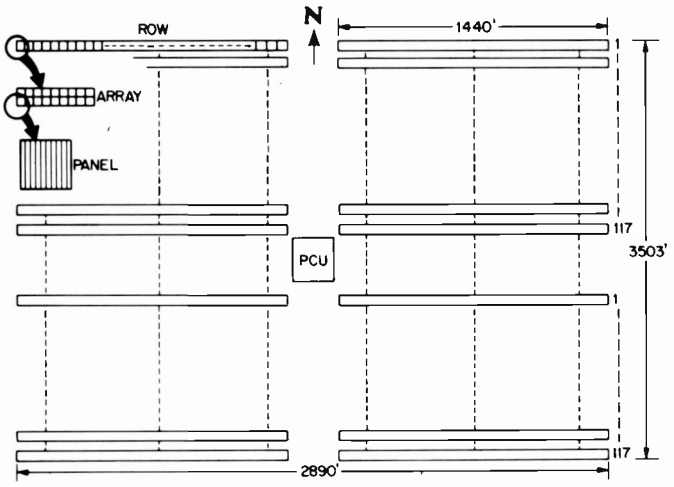

Fig. 6. Field layout. This figure shows the overall configuration of the PV power plant; how panels are assembled into arrays, and arrays into rows; and the layout of those rows with respect to the power-conditioning unit.

$$\text{Energy} = (\text{Insolation}) \times (\text{Geometric fraction of insolation}) \times (\text{Conversion efficiency}) \times (\text{Time interval}) - (\text{Losses}).$$

Insolation

The algorithm, as written, calculates the instantaneous level of insolation of an ideal day for the geographical area under consideration. This calculation was modified so that the resulting data, when reduced to an average seasonal day, is equal to the average seasonal day of actual weather described earlier. The calculations are made at 30-minute intervals every 30 days. The seasonal average day output energies are:

$$\begin{aligned}
\text{Spring} &= 0.051\ \text{KWh/ft}^2\ (0.556\ \text{KWh/m}^2) \\
\text{Summer} &= 0.048\ \text{KWh/ft}^2\ (0.524\ \text{KWh/m}^2) \\
\text{Fall} &= 0.039\ \text{KWh/ft}^2\ (0.424\ \text{KWh/m}^2) \\
\text{Winter} &= 0.039\ \text{KWh/ft}^2\ (0.422\ \text{KWh/m}^2)
\end{aligned}$$

Shadowing losses

Shadowing of the panels in one row by those of the row in front of them occurs primarily in the early morning and late afternoon during winter months. Its occurrence and extent are functions of the latitude, time of year, time of day, panel tilt, panel slant height, row-to-row spacing and east/west orientation. Shadowing could be completely avoided by increasing the row-to-row spacing. However, this would increase wire costs, wire losses, and land use. The plant, as designed, has a shadow loss of less than one percent. A subroutine in the algorithm calculates the instantaneous power loss and cumulative energy loss caused by shadowing. The calculated plant output is modified accordingly.

Wire losses

In calculating wire losses, the algorithm considers the current in each wire resulting from the insolation, as reduced by the shadowing losses. Both power and energy losses are calculated.

The wire losses (energy) for the specific design are 1.4 percent. They could be further reduced by increasing wire size or reducing wire length. The first option increases costs, the latter decreases costs, but increases shadowing losses. Trade-offs of this type were evaluated in terms of the prime criterion minimizing output energy cost to determine wiring configuration and wire size.

Table V. *50-MW PV plant cost estimate summary.*

Category	*Near term ($K)*	*Intermediate term ($K)*
Wire	1,948	1,387
Site preparation	1,616	808
Electrical protection	472	236
Array structure	30,046	18,814
SUBTOTAL	34,382	21,245
	(68.65 $/m²)	(42.42 $/m²)
	(6.37 $/ft²)	(3.94 $/ft²)
Power conditioning	7,500	5,000
10$ a-Si monolithic panels	31,048	15,524
SUBTOTAL	34,548	20,524
Land	4,650	4,650
TOTAL	77,580	46,419
	(1.61 $/$W_p$)	(.936 $/$W_p$)

Power conditioning losses

The design is based on PCUs of 5 MW capacity. Thus, 10 units are required. Although still in the design stage, it is expected that these PCUs will have an average annual efficiency of 96 percent.

Cost estimates

Having designed the PV plant, we estimated its cost of construction to identify the major cost components and to see how therse construction cost estimates compared with our utility break-even costs. The estimates presented are based in part on direct quotations, studies sponsored by the U. S. Department of Energy, and RCA's own research and development.

Table V gives a cost estimate summary for intermediate-term and near-term values. All costs are in 1982 dollars.

The operation and maintenance (O&M) costs are based on estimates of the required manpower and materials. Annual O&M cost is $241K or $0.044/ft² ($0.48/m²).

A typical conventional power plant has annual O&M costs of $15 /kW plus $0.003/kWh. Therefore, a 50-MW conventional power plant with a 60-percent capacity factor would have O&M costs of $1500 K.

The design and performance evaluation is based on an actual insolation year in central New Jersey. The design criterion is to comprehensively satisfy the essential technical requirements with a minimum cost of energy output. A summary of the characteristics of the design is given in Table VI.

Conclusions

Because of the time-constrained and intermittent nature of energy output, PV generation should be considered as an alternative form of intermediate- or peaking-duty capacity. Based on simulation studies performed with PSE&G system long-range expan-

Table VI. *Summary of plant characteristics.*

Power	50 MW (nominal)
Voltage	2000 VDC bipolar
Annual energy production	85.5 GWh
Area	232 Acres
Performance	
Capacity factor	19.4%
KWh/W_p	1.7
Costs	0.96 - 1.61 \$/W_p

sion scenarios by comparing PV generation with high-temperature combustion turbine units and using New Jersey insolation data, the break-even capital costs for a PV power plant, including the balance of plant, range from about \$1100 to \$1350 per peak kW (1982 dollars) depending on the degree of PV-capacity penetration, which varies from 15 to 20 percent of the system peak load. The higher the penetration, the lower the required break-even cost. Accordingly, as installed PV-generation costs approach these levels, PV generation should be considered in future utility capacity-expansion plans. Furthermore, based on the present rate of progress in amorphous-silicon photovoltaics, the cost objectives described above are achievable.

Acknowledgments

The authors would like to acknowledge the contributions of D. Kramer, K. Pitts, J.J. Skokowski, and M. Zonis of RCA; and N. Nour, T. Piascik, and W.S. Ku of the Advanced Systems Planning Group of the Public Service Electric and Gas Company of Newark, N.J.

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Authors (standing) Stranix and Firester.

Jack Stranix joined RCA Service Company in 1955. He held various technical support and supervisory positions on such programs as the TALOS Weapons Systems, the automated checkout equipment for the ATLAS missile, and the BMEWS system. He transferred to the International Licensing Corporate Staff in 1964. He administered RCA's licensing agreements on broadcast, avionics, communication and military products. In 1978, Stranix became Manager, Market Development for the Energy Laboratories at RCA Laboratories. He received a B.S. and M.S.E.E. from Drexel University, Philadelphia, Pennsylvania.
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Art Firester's bio appears on page 44.

Patents

Cablevision Systems

Korda, P.B.
Recovery of normally illegible, magnetically recorded information—31166

Commercial Communications Systems Division

Bendell, S.L.
Image tube suppression circuit—4375310

Brokl, S.S.
Receiver for jam-resistant TV signal—4378570

Consumer Electronics

Lehmann, W.L.
Input selection arrangement for applying different local oscillator signals to a prescaler of a phase-lock loop tuning system—4379271

Luz, D.W.
Duty-cycle controlled inverter power supply for a television receiver—4377776

Naimpally, S.V.
Signal separation networks—4376953

Shanley, 2nd, R.L. | Parker, R.P.
Signal gain control with DC compensation—4376288

Willis, D.H.
Television receiver ferroresonant power supply disabling circuit—4377775

Laboratories

Andrus, J.E. | Hang, K.W.
Apparatus for electrophoretic deposition—4376031

Avins, J.Y. | Phillion, O.W.
Circuit for detecting phase relationship between two signals—4379221

Bleazey, J.C.
Track skipper for video disc player—31223

Chambers, R.W. | McNeely, M.L.
Torrington, L.A.
Apparatus for molding a recorded disc—4379686

Datta, P. | Arroyd, N.A. | Friel, R.N.
Conductive molding composition—4378310

Dischert, R.A. | Williams, Jr., J.J.
Reitmeier, G.A.
TDM scheme for digital video processing—4376948

Dischert, R.A. | Flory, R.E.
Transmission system with sequential time-compressed baseband color—4376957

Glock, T.L.
Shielded beam guide structure for a flat panel display device and method of making same—4376258

Goodman, A.M.
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Gross, J. | Barkow, W.H. | Mirsch, J.W.
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Halon, E.
Plasma etching of aluminum—4375385

Hedel, R.H.
Stone sorting apparatus and method—4375854

Jebens, R.W.
Optical focus sensor—4381557

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Processing of video discs—4376087

Prabhu, A.N. | Hang, K.W.
Conductor inks—4376725

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Overglaze inks—4377642

Prabhu, A.M. | Hang, K.W.
Low value resistor inks—4379195

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Indium oxide resistor inks—4380750

Reitmeier, G.A. | Marlowe, F.J.
Self-enabling dropout corrector—4376289

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Two-dimensional adaptive dropout compensator and chroma inverter—4376955

Reitmeier, G.A.
Adaptive error concealment—4377820

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Digital error detection using bracketing—4380069

Ross, M.D.
Slow-down processor for video disc mastering having color phase error detector/correction—4376954

Russell, J.P.
System for compensating for intensity variations and beam landing errors in flat panel display devices—4376260

Sechi, F.N.
Microwave power circuit with an active device mounted on a heat-dissipating substrate—4376287

Sinniger, J.O. | Robbi, A.D.
Digital timing system for spark advance—4375209

Torres, R. | Woodward, O.M.
Loop antenna arrangement for inclusion in a television receiver—4380011

Troiano, A.
Noise responsive automatic peaking control apparatus—4376952

Whitley, G.J.
System for securing component leads to printed circuit boards—4377026

Williams, R.
Metal electrode for amorphous silicon solar cells—4378460

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Schwarzmann, A.
High power, low frequency, electronically adjustable attenuator—4378536

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Christopher, T.J. | Mehrotra, G.N.
Signal expander—4377788

Kelleher, K.C.
Video disc player having time-base correction and constant angular velocity turntable—4376956

Stevens, B.N. | Aldridge, L.R.
Apparatus and method for cleaning recorded discs—4375992

Ziegel, D.H.
Method and apparatus for sorting stones—4379510

Solid State Division

Butterwick, G.N.
Shielded focusing electrode assembly for a photomultiplier tube—4376246

Caprari, F.
Xenon flash lamp shield—4378583

Harford, J.R.
Gain-controlled amplifier system—4378528

Hoover, M.V.
Operational amplifier employing complementary field-effect transistors—4377789

Kaplan, L.A.
Current amplifier—4380740

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Photocurrent compensation for electronic circuitry exposed to ionizing radiation—4380741

Nyul, P.
Method for supplying a low-resistivity electrical contact to a semiconductor laser device—4380862

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Keller, S.C. | Ruth, L.C.
Non-loading digital voltmeter—4375616

Kunz, P.J.
Limp-stream method for selectively etching integral cathode substrate and support—4376009

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Shisler, R.W. | Barkow, W.H.
Television deflection yoke having a toroidally-wound deflection coil—4376273

Pen and Podium

Recent RCA technical papers and presentations

To obtain copies of papers, check your library or contact the author or his divisional Technical Publications Administrator (listed on back cover) for a reprint.

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J.A. Bauer
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J.A. Bauer
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K.D. Bedsworth | J.M. Bokoles
Computer Controlled Microwave Measurements for Near-Field Testing of Antenna Systems—Symposium of Computer-Aided Microwave Engineering, RCA Labs, Princeton, N.J. (4/15/83)

C.A. Blum
Computer-Aided Design & Development of Rectangular Coax—Symposium of Computer-Aided Microwave Engineering, RCA Labs, Princeton, N.J. (4/1583)

F.J. Buckley
Software Quality Assurance—IEEE Seminar, New Orleans, La. (3/83)

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The Application of Distributed Computers to Real-Time System—California State University, Sacramento, Calif. (3/83)

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M. Davis
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D.C. Drumheller
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J. Golub | W.A. Soper
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W.C. Grubb, Jr.
Minicomputers and Microcomputers for Non-Electrical Engineers—George Washington University, Washington, D.C. (10/29/82); Drexel University, Phila., Pa. (11/18/82); George Washington University, Washington, D.C. (2/11/83).

W.C. Grubb, Jr.
Solid State Electronics for Non-Electrical Engineers—George Washington University, Washington, DC (1/7/83); George Washington University, San Diego, Calif. (1/26/83); Drexel University, Phila., Pa. (4/21-22/83).

W.C. Grubb, Jr.
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E.T. Hatcher
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Stripline Component Design for Phased Array Column Combiner Networks—Symposium on Computer-Aided Microwave Engineering, RCA Labs, Princeton, N.J. (4/15/83)

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R.F. Kolc
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N.R. Landry
Precision Testing of Complex Stripline Networks—Symposium on Computer-Aided Microwave Engineering, RCA Labs, Princeton, N.J. (4/15/83)

H.D. Lewis | V.D. Stubbs, Jr.
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F.E. Oliveto
System Reliability—14th Annual Reliability Symposium, Bala Cynwyd, Pa. (4/20/83)

W.T. Patton
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G. Privette
Special Application Programming in the Applicon System to Facilitate Microwave Network Design—ASQC Meeting, Washington, D.C. (4/14/83)

R. Rabbitz
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M.D. Rauchwerk | A.B. Kabadi
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R.H. Edmondson
Skypath Control—NAB 61st Annual Convention & International Exposition, Television Engineering Session, Las Vegas, Nev.

Engineering News and Highlights

Altgilbers named GCS Ed Rep

Thomas E. Altgilbers was appointed Editorial Representative to the *RCA Engineer* for Government Communications Systems. He is Manager, Proposal Quality, responsible for developing techniques and guidelines to improve the general level of proposal effectiveness. He also has broad responsibilities in market planning, target evaluation and tracking, and investment planning and allocation. Mr. Altgilbers joined RCA as an Engineering Writer following his graduation from Indiana Institute of Technology in 1958 with a B.S. in electronic engineering. Since 1963 he has handled various assignments in proposal administration. From 1943 to 1951, he served as Naval Aviator after attending various U.S. Navy military schools.

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Haas is Patents Ed Rep

George E. Haas was recently named Editorial Representative to the *RCA Engineer* for Patent Operations, Princeton, New Jersey. Mr. Haas joined RCA in 1974 and for several years his responsibilities were related to the preparation and prosecution of patent applications. He is presently Staff Patent Counsel, in which capacity he handles patent interference and infringement matters. In addition, he reviews contracts with respect to technical data and patent-rights provisions, and he has responsibility for publishing RCA Technical Notes. Mr. Haas received a M.S.E.E. in 1971 from Marquette University and was graduated from the Georgetown Law Center in 1974.

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Kaminsky is RCA Service Company TPA

Murray F. Kaminsky is the new *RCA Engineer* Technical Publications Administrator for RCA Service Company, Cherry Hill. He will take over for Joe Steoger, who served as Service Company's TPA for years. Mr. Kaminsky, who is currently Manager, Engineering Integration, RCA Service Company, joined RCA as an Engineer at the Camden, N. J. plant in 1958. He has held a series of engineering and management positions at RCA and elsewhere, most recently specializing in voice/data communications and telephone network operations. He received both a B.S.E.E. and an M.S.E.E. from the University of Pennsylvania. Murray was Technical Publications Administrator for the Computer Division between 1968 and 1969.

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GSD's Hahn joins TPA network

Dr. Peter M. Hahn, who is a Staff Technical Advisor on the Government Systems Division (GSD) Engineering Staff, has been named Technical Publications Administrator (TPA). Since his graduation from CCNY in 1958, he has worked in three major areas: military communications switching, optical character recognition, and target detection and classification. Dr. Hahn originally came to RCA in 1966 after finishing his studies for the Ph.D. at the University of Pennsylvania. At that time he worked at MSR as a systems analyst. After a few years, he went to work for Philco Ford. He returned to RCA in 1976 as a Unit Supervisor in Government Communications Systems (GCS), working on ECOM. He left again in 1977 to become Chief Engineer of Sonic Sciences Inc., and returned two years later to join GCS's Advanced Mission Group. In his current role, Dr. Hahn is involved in the planning and analysis of the data and signal-processing elements of GSD's IR&D program. He also supports the business units in areas of his expertise. In addition to his work at RCA, Dr. Hahn is on the adjunct faculty at Drexel University where he teaches courses in estimation theory, identification of systems, and pattern recognition.

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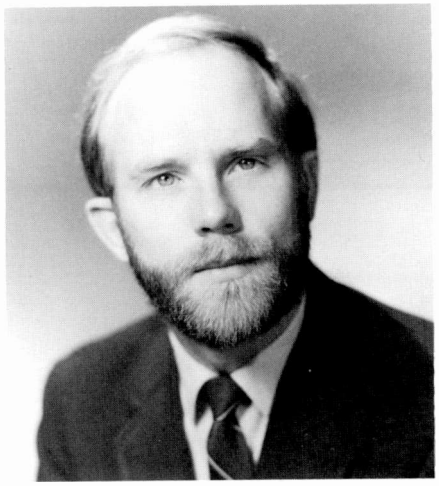


van Raalte is Director of VideoDisc Systems Research Laboratory

Appointment of **Dr. John A. van Raalte** as Director of the VideoDisc Systems Research Laboratory has been announced by **Dr. Jon K. Clemens,** Staff Vice-President for Consumer Electronics Research, at RCA Laboratories in Princeton, N. J.

Dr. van Raalte joined RCA Laboratories as a Member of the Technical Staff in 1964. In 1970, he was named Head of Display and Device Concepts Research, and in 1979 he was appointed Head of VideoDisc Recording and Playback Research. In this position, he directed efforts to support the development and market introduction of the RCA VideoDisc system in 1981.

Dr. van Raalte was awarded an RCA Laboratories Outstanding Achievement Award in 1969 for the development of a novel television projection system. A native of Copenhagen, Denmark he received B.S. and M.S. degrees from the Massachusetts Institute of Technology in 1960, an Engineer's degree in 1962, and a Ph.D. degree in 1964.

Consumer Electronics

Leonard J. Schneider, Division Vice-President, Manufacturing, announces the organization of Manufacturing as follows: **Robert C. Arnett,** Plant Manager, Bloomington Plant; **Bennie L. Borman,** Director, Manufacturing Engineering and Technology; **David R. Crawford,** General Manager, RCA Componentes-S.A. de C.V.; **David D. Eden,** Director, Crown Wood Products Operations; **Kenneth D. Lawson,** Director, Facilities Management; **James D. MacKay,** Plant Manager, RCA, Inc. (Canada); **James J. McDowell,** Manager, VideoDisc Player Manufacturing Operations-Bloomington Plant; **Leonard J. Schneider,** Acting Director, Components Operations; and **Kenneth S. Williams,** President and General Manager, RCA Taiwan Limited.

James R. Smith, Division Vice-President, Product Assurance, announces the appointment of **James J. Legault** as Manager, Consumer Acceptance Laboratory. Mr. Legault will report to the Division Vice-President, Product Assurance.

Leonard J. Schneider, Acting Director, Components Operations, announces the organization of Components Operations as follows: **Eric R. Bennett,** Manager, Cartridge Manufacturing Operations; **G. Bruce Dilling,** General Manager, Productos Electronicos de La Laguna-S.A. de C.V.; **Gary A. Gerhold,** Plant Manager, Indianapolis Components Plant; **Horst E. Haslau,** Manager, Equipment Development; and **Peter C. Hill,** Manager, Ferrite Operations.

Bennie L. Borman, Director, Manufacturing Engineering and Technology, announces the appointment of **Larry J. Byers** as Manager, Test Technology, and **Larry A. Olson** as Manager, Manufacturing Technology Center. Messrs. Byers and Olson will report to the Director, Manufacturing Engineering and Technology.

Larry J. Byers, Manager, Test Technology, announces the appointment of **Brian L. Whitcomb** as Manager, Chassis Test Systems, and **David B. Graves** as Manager, Integrated Circuits Test Systems. Messrs. Graves and Whitcomb will report to the Manager, Test Technology.

David R. Crawford, General Manager, RCA Componentes-S.A. de C.V. announces the appointment of **Alfred Crager** as Manager, Test Engineering. Mr. Crager will report to the General Manager, RCA Componentes-S.A. de C.V.

Edmund W. Riedweg, Plant Manager, Bloomington Plant, announces the appointment of **Brian E. Pollack** as Manager, Quality Control. Mr. Pollack will report to the Plant Manager, Bloomington Plant.

Alfred Crager, Manager, Test Technology, announces the appointment of **Darrel L. Billings** as Administrator, Mechanical Engineering. Mr. Billings will report to the Manager, Test Technology.

Globcom

Joe Terry Swain, Vice-President, Switched Services Engineering and Operations, announces the organization of Switched Services Engineering and Operations as follows: **William D. Barnum,** Director, Field Support Services; **Russell E. Blackwell,** Director, Computer Operations; **William A. Klatt,** Director, Network Operations; **M. Glen Looney,** Director, Computer Programs; **John P. Shields,** Director, Network Engineering; **Richard L. Chory,** Manager, Software Engineering; **Frank A. Middleton,** Program Manager, Systems Implementation; and **Jerome S. Bonow,** Administrator, Project Control.

Laboratories

James L. Miller, Staff Vice-President, Manufacturing and Materials Research, announces the organization of Manufacturing and Materials Research as follows: **Istvan Gorog,** Director, Manufacturing Technology Research Laboratory; **Marvin A. Leedom,** Director, Manufacturing Systems Research Laboratory; and **David Richman,** Director, Materials and Processing Research Laboratory.

Istvan Gorog, Director, Manufacturing Technology Research Laboratory, announces the organization of Manufacturing Technology Research Laboratory as follows: **David P. Bortfeld,** Head, Systems Research; **Istvan Gorog,** Acting, Advanced Technology Research; **James P. Wittke,** Fellow, Technical Staff; and **Martin Rayl,** Head, Productivity and Quality Assurance Research.

Marvin A. Leedom, Director, Manufacturing Systems Research Laboratory, announces the organization of Manufacturing Systems Research Laboratory as follows: **Charles B. Carroll,** Head, Electromechanical Systems Research; **Robert R. Demers,** Head, Design for Automation Research; **William G. McGuffin,** Head Instrumentation Systems Research; and **Keith S. Reid-Green,** Head, Mechanical Design Techniques Research.

David Richman, Director, Materials and Processing Research Laboratory, announces the organization of Materials and Processing Research Laboratory as follows: **Vladimir S. Ban,** Head, Organic Electronic Materials Research; **Glenn W. Cullen,** Head, Materials Synthesis Research; **Leonard P. Fox,** Head, VideoDisc Applied Process Research; **William L. Harrington,** Head, Materials Characterization Research; **Richard E. Honig,** Staff Scientist; and **Robert J. Ryan,** Head, Polymer Processing Research.

John A. van Raalte, Director, VideoDisc Systems Research Laboratory, announces the organization of VideoDisc Systems Research Laboratory as follows: **Marvin Blecker,** Head, Systems Evaluation Research; **John G. N. Henderson,** Head, VideoDisc Signal Systems Research; **James J. Gibson,** Fellow, Technical Staff; **Eugene O. Keizer,** Staff Scientist; **James J. Power,** Head, VideoDisc Player Control Research; **W. Ronald Roach,** Head, VideoDisc Playback Research; and **Michael D. Ross,** Head, VideoDisc Mastering Research.

Patent Operations

Paul J. Rasmussen, Director, Patents—Television Receivers, announces the appointment of **Joseph J. Laks** as Managing Patent Attorney. Mr. Laks will report to the Director, Patents—Television Receivers.

Solid State Division

Larry J. French, Division Vice-President, Solid State Technology Center, announces the organization of Solid State Technology Center as follows: **Philip K. Baltzer,** Head, LSI Systems; **Ronald C. Bracken,** Director, Computer-Aided Design and Photomask Operations; **Larry J. French,** Acting Manager, VLSI Design; **John M. Herman III,** Director, VLSI Manufacturing Technology; and **David S. Jacobson,** Director, VLSI Product Operations.

David S. Jacobson, Director, VLSI Product Operations, announces the organization of VLSI Product Operations as follows: **Richard H. Bergman,** Manager, Design, Test and Computer-Aided Manufacturing; **Robert A. Donnelly,** Manager, Program Management and Business Planning; **Davis S. Jacobson,** Acting Manager, Quality and Reliability Assurance; and **Richard H. Zeien,** Manager, Package and Assembly.

John M. Herman III, Director, VLSI Manufacturing Technology, announces the organization of VLSI Manufacturing Technology as follows: **Edward C. Douglas,** Manager, SOS Development; **Peter Ferlita,** Manager,. Manufacturing, Planning and Technical Training; **John M. Herman III,** Acting Manager, Process Engineering; **John M. Herman III,** Acting Manager, Equipment Repair and Maintenance; and **Roger E. Stricker,** Manager, Device Engineering.

Video Component and Display Division

Charles A. Quinn, Division Vice-President and General Manager, Video Component and Display Division, announces the appointment of **Robert K. Lorch** as Division Vice-President, Video Display Monitor Products. Mr. Lorch will report to the Division Vice-President and General Manager, Video Component and Display Division.

Mahlon B. Fisher, Division Vice-President, Engineering, announces the organization of Engineering as follows: **Robert W. Hagmann,** Manager, Applications Engineering; **Leonard F. Hopen,** Manager, Manufacturing Processes and Pilot Development; **Harlan R. May,** Manager, Yoke Planning and Coordination; **James C. Miller,** Manager, Technical Projects and Engineering Administration; **Albert M. Morrell,** Manager, Product Development; and **John M. Ratay,** Manager, Equipment Development.

Leonard F. Hopen, Manager, Manufacturing Processes and Pilot Development, announces the appointment of **Yoneichi Uyeda** as Manager, Materials and Processes and Manager, Panel Process Development and Laboratories. Mr. Uyeda will report to the Manager, Manufacturing Processes and Pilot Development.

Albert M. Morrell, Manager, Product Development, announces the organization of Product Development as follows: **Richard H. Godfrey,** Manager, Tube Design; **Robert L. Barbin,** Manager, Mount Development; and **Anthony S. Poulos, Jr.,** Manager, Type Engineering.

Bernard D. Brumley, Plant Manager, Marion Plant, announces the organization of Plant Manager as follows: **Harry G. Cox,** Manager, Plant Engineering; **Donald G. Crouch, Sr.,** Manager, Tube Manufacturing; **Richard A. Dessing,** Manager, Financial Operations; **Larry E. Leach,** Manager, Industrial Relations; **John E. Neal,** Manager, Materials; **Donald J. Ransom,** Manager, Product Safety, Quality and Reliability; **Walter R. Rysz,** Manager, Process and Production Engineering; **Richard W. Osborne,** Manager, Resident Engineering; **James S. Shepherd,** Manager, Tube Manufacturing; and **Donald M. Wallace,** Manager, Industrial Engineering and Standards.

John S. Ignar, Plant Manager, Scranton Plant, announces the organization of Plant Manager as follows: **John J. Bross,** Manager, Materials; **Donald R. Cadman,** Manager, Product Safety, Quality and Reliability; **Thomas R. Conway,** Manager, Plant Engineering; **Louis J. DiMattio,** Manager, Resident Engineering; **Richard F. Falusy,** Manager, Financial Operations; **Vincent C. Kneizys,** Manager, Manufacturing; **Jack I. Nubani,** Manager, Process and Production Engineering; **Daniel H. Ranlet,** Manager, Industrial Engineering and Standards; **Joseph C. Scagliotti,** Manager, Industrial Relations; and **Thomas J. Witowski,** Administrator, Manufacturing Support and Planning.

Professional activities

Forty-four RCA scientists honored for research advances in 1982

Dr. William M. Webster, Vice-President, RCA Laboratories, Princeton, N. J., announced that forty-four scientists have been given RCA Laboratories Outstanding Achievement Awards for contributions to electronics research and engineering during 1982. Recipients of individual awards are:

John G. Aceti, for development of automated inspection systems for VideoDisc caddies.

Leslie R. Avery, for the invention of novel devices for protecting bipolar integrated circuits against electrical overstress.

Dr. Charles W. Magee, for contributions to the field of secondary ion mass spectrometry.

Arye Rosen, for the development of high-performance silicon *pin* diodes for application to communication systems.

Elvin D. Simshauser, for the development of a stereo VideoDisc cartridge.

Recipients of team awards are:

Dr. Roger C. Alig, Dr. Dennis J. Bechis, Hsing Y. Chen, and **Richard H. Hughes,** for the development of advanced electron guns for color picture tubes.

Brian Astle, Michael Keith, Lawrence D. Ryan, Robert J. Siracusa, and **David L. Sprague,** for contributions leading to the development of a recommended industry standard for broadcast teletext in North America.

John P. Beltz, Kenneth W. Hang, Charles J. Nuese, and **Gerard Samuels,** for implementing cost-effective techniques for the production of silicon epitaxial wafers and fully passivated power transistors and thyristors.

John B. Berkshire, Bobby J. Rooks, and **Howard G. Scheible,** for contributions to conception, development, and implementation of a novel soldering technique leading to significant reduction in manufacturing defects.

Dr. Scott C. Blackstone, Werner Kern, and **Joseph M. Shaw,** for developing a technology for deposition and control of borophosphosilicate glass films on semiconductor devices.

Anthony W. Catalano, Dr. Joseph Dresner,

Dr. James Kane and **Dr. George A. Swartz,** for optimization of material properties leading to high-performance amorphous-silicon solar cells.

Michael T. Cummings, Raymond J. Menna, Robert W. Paglione, Dr. Barry S. Perlman, Stewart M. Perlow, and **Herbert J. Wolkstein,** for the transfer of essential technologies and skills for the fabrication of solid-state power amplifiers for RCA's all-solid-state communications satellite.

Dr. Ronald E. Enstrom, Maxwell M. Hopkins, Dr. Arthur Miller and **Dr. Rabah Shahbender,** for the elucidation of measuring techniques useful in strengthening glass-vacuum structures such as color television picture tubes.

Peter D. Gardner, Stuart T. Jolly, Dr. S. Yegna Narayan, and **John F. Paczkowski,** for contributions to the development of gallium indium arsenide field-effect transistors for microwave and logic applications.

Dr. Srinvas T. Rao and **Louis Trager,** for contributions to the technology of copper electro-deposition leading to improvements in VideoDisc mastering.

Enstrom elected Vice-President of Electrochemical Society

Ronald E. Enstrom, Display Processing and Manufacturing Research Laboratory, has been elected a Vice-President of the Electrochemical Society. The Society, with an international membership of about 6,000 scientists, has its headquarters in Pennington, N.J. Dr. Enstrom was previously Chairman of the Society's Electronics Division.

Symposium on computer-aided microwave and rf engineering

A Symposium on Computer-Aided Engineering (CAE) for microwave and rf applications was held at RCA Laboratories, Princeton, on April 14 and 15, 1983. The technical program consisted of a total of 24 pages, grouped into four contiguous sessions: computer-aided modeling, analysis and design; computer-aided design and measurement automation; computer-aided testing of antennas, networks, and systems; and computer-aided design and artwork information (APPLICON). In addition, time was allocated for an informal workshop on the central theme of Computer-Aided Design and Measurement Automation. This workshop was intended primarily to allow the attendees to discuss common areas of interest and to develop plans and strategies for future CAE development.

Barry Perlman, Manager, Computer-Aided Design and Testing, RCA Laboratories, organized and chaired the Symposium. Introductory speakers were **Fred Sterzer,** Director, Microwave Technology Center, RCA Laboratories, and **Bernie Matulis,** Chief Engineer, Missile and Surface Radar.

For a list of authors and their papers, refer to the March 1983 *TREND.*

J.J. Brandinger (speaking), and Dr. and Mrs. C. Richard Johnson, Jr.

Brandinger is keynote speaker at Eta Kappa Nu award banquet

Dr. Jay J. Brandinger, Division Vice-President and General Manager of RCA "SelectaVision" VideoDisc Operations, Indianapolis, was the keynote speaker at the annual award banquet of Eta Kappa Nu, the National Honorary Electrical Engineering Society. The purpose of the banquet, held on April 18, 1983, in New York City, was to honor the 1982 winner of the Eta Kappa Nu Recognition of Outstanding Young Electrical Engineers.

The winner, Dr. C. Richard Johnson, Jr., Associate Professor of Electrical Engineering at Cornell University, was honored for his outstanding contributions to the field of control technology, his cultural achievements, and his involvement in professional activities. This award program was established in 1936 to emphasize among electrical engineers that their service to mankind is manifested not only by achievements in purely technical affairs, but in a variety of other ways. The Chairman of the Eta Kappa Nu Award Organization Committee is **James A. D'Arcy,** RCA "SelectaVision" VideoDisc Operations.

During his address, "Creativity in the Industrial Environments," Dr. Brandinger discussed technological innovation, both radical and incremental, as it has progressed during the past 30 years, and examined the ways it has impacted our economic and social life styles. He used the RCA "CED" VideoDisc System as an example of radical innovation. Dr. Brandinger emphasized the growing importance of group innovation, and he concluded by challenging Eta Kappa Nu to create an additional class of awards that recognize innovative contributions by technical teams and companies.

MSR technical authorship excellence recognized

Abe Hopper and **De Lewis** of Missile and Surface Radar in Moorestown were recognized during the quarter for outstanding contributions. *Coordinate,* the New Jersey Society of Professional Land Surveyors' quarterly publication for which Abe was responsible last year, has received the "Excellence in Professional Journalism Award" for 1982 from the National Society of Land Surveyors and the American Congress on Surveying and Mapping. De's presentation of a paper on S-band data communications that he co-authored with **Vic Stubbs** was voted the best presentation in the cooperative target recognition category at the Tri-Service Combat Identification Systems Conference in February.

Stewart named fellow of the technical staff

Wilber C. Stewart, Display Processing and Manufacturing Research Laboratory, has been appointed a Fellow of the Technical Staff of RCA Laboratories. The designation of Fellow is comparable to the same title

used by universities and virtually all technical societies, and is given in recognition of "a record of sustained technical contribution in the past and of anticipated continued technical contribution in the future."

Two RCA Laboratories researchers elected to National Academy of Engineering

Two RCA Laboratories researchers, **Dalton H. Pritchard** and **Dr. Fred Sterzer**, have been elected to membership in the U.S. National Academy of Engineering (NAE), the highest professional distinction that can be conferred on an engineer.

The NAE cited Mr. Pritchard, a Fellow of the Technical Staff, for "significant contributions to the development of the NTSC color system with subsequent continued improvements and innovations in video technologies." Dr. Sterzer, Director of the Microwave Technology Center, was cited for "continuing significant contributions in development of advanced microwave devices and for motivating researchers in the forefront of microwave technology."

Election to the Academy honors those who have made important contributions to engineering theory and practice or who have demonstrated unusual accomplishments in the pioneering of new and developing fields of technology.

RCA Engineer article wins publication competition

"The RCA SelectaVision VideoDisc System" an *RCA Engineer* article by **H. N. Crooks,** who is Technical Liaison for "SelectaVision" VideoDisc Operations, was selected for a Technical Publications Competition Award by the New York Chapter of the Society for Technical Communications. Staffers at the *RCA Engineer* submitted the article, published in the March/April 1981 *Engineer*, in the "periodical article" category. The award was presented on June 8, 1983 at a banquet in New York.

RCA Engineer Ed Rep moderates symposium

Eva Dukes, who is the *RCA Engineer* Editorial Representative from RCA Laboratories, presented a paper and moderated a panel discussion at the 30th International Technical Communication Conference in St. Louis on May 1 to 4, 1983. Ms. Dukes spoke on "Authors' Strategies for Marketing Their Books." The session that she moderated, titled "Strategies for Professionals Who Must Write," also featured speakers Herbert B. Michaelson, IBM Corp., and H. Lee Shimberg, a consultant from Silver Spring, Md.

Astro awards for patent filing

Robert Miller (far right), Chief Engineer at RCA Astro-Electronics, presented awards for patent filing to the following engineers: Raj Gounder (far left), for "Antenna Construction"; and John E. Keigler (beside Miller) and Frank A. Hartshorne for a "Satellite Dual Antenna Pointing System."

Cherry Hill Government Systems Division employees are professionally active

Members of the Government Systems Division in Cherry Hill have undertaken a multitude of recent professional activities.

James B. Feller is Program Chairman for the upcoming EASCON '83 16th Annual IEEE Electronics and Aerospace Conference and Exposition, in Washington, D.C., between September 19 and 21, 1983.

Dr. Thomas A. Martin is Chairman of the Embedded Computer Software Committee of the AIAA Aerospace Technical Council, and he is also an RCA representative to the Technical Advisory Board of the Microelectronics and Computer Technology Corporation (MCC).

Dr. Jack Hilibrand is Secretary of the IEEE Philadelphia Section Awards Committee, and he is a Member of the IEEE National Fellow Committee and of the IEEE Solid State Circuits and Technology Committee.

Dr. Sidney Ross was Co-chairman of the ADPA Annual DoD Science and Engineering Technology Symposium, Naval Surface Weapons Center, White Oak, Md., held between May 3 and 5, 1983. Ross is also Co-chairman of the ADPA Executive Board Planning Committee: Workshop on University/Industry/DoD relationships. In addition, he is Deputy Program Chairman, EASCON '83 16th Annual IEEE Electronics and Aerospace Conference and Exposition, Washington, D. C., September 19 to 21, 1983.

Dr. Peter M. Hahn is Adjunct Professor at Drexel University, Philadelphia, Pa., where he teaches graduate courses in Estimation Theory, System Identification, and Pattern Recognition.

Allgyer was seminar chairman

Warren Allgyer, Director of Special Projects, NBC Engineering and Technical Services, was Chairman for a seminar on High Tech Programming called "How to Use the Tools," at Las Vegas, on March 22, 1983. The seminar was held by the National Association of Television and Programming Executives (NATPE).

Technical Excellence

RCA Astro engineering excellence awards made

Niederoest

McGiffney

The following Engineering Excellence Awards, together with citations, have been announced at RCA Astro-Electronics, Princeton, N.J.

Guido Niederoest received his Engineering Recognition Award for his outstanding contribution to the analysis of loads and development of design criteria for the GSTAR/SPCC spacecraft structures.

Guido Niederoest was the lead mechanical analysis engineer during the preliminary and final design phases of the GSTAR/

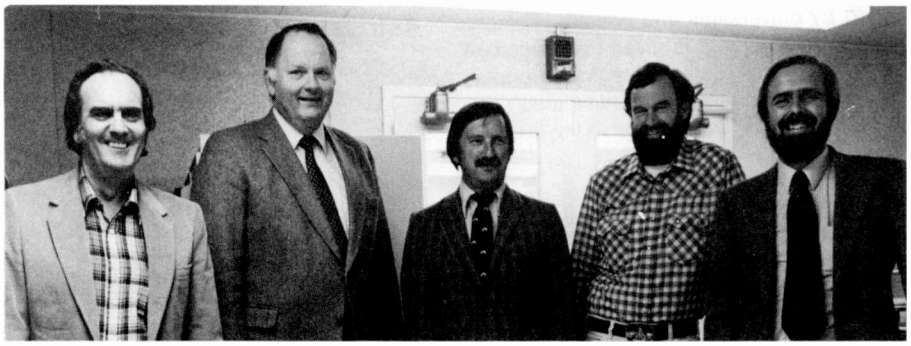
SPCC projects. He supervised the building of structural finite-element models of the primary and secondary structures and developed subassembly loads and frequency data for vendor usage. He provided timely support to ensure meeting of very stringent production schedules while maintaining controlled cost factors related to computer usage. Guido has received commendation for his work from both the customer and program offices.

Donald Z. McGiffney, received his Engineering Excellence Award for his outstanding contribution to the Preliminary Design of Telemetry, Tracking and Command Systems.

Don, a senior member of the technical staff at Astro, generated TT&C subsystem configurations for numerous proposals and preliminary designs. He developed outstanding Telemetry, Tracking and Command Subsystem configurations for Satellite Television Corporation's Direct Broadcast Satellite proposal; performed analyses for several contractual studies including the Mars/Lunar Geoscience Orbiter, the 30/20 GHz Demonstration System and the National Oceanic Satellite System. He provided systems engineering support for the RCA Satcom, Spacenet and GSTAR communications satellite programs currently being built at Astro.

William C. Schultz, Jr., David J. Iverson, James L. Martin, Ronald E. Lange and **John M. Meehan** are the 1982 winners of the Engineering Excellence Team Award for their outstanding effort in establishing the Defense Meteorological Satellite Program (DMSP) TRADS/TP2 ground system at the Payload Test Facility at Vandenberg Air Force Base, California. The teams outstanding performance included:

- Verification of systems engineering, implementation of required modifications, procurement of hardware and software as modified during system design verification.
- Subcontract technical management of four major procurements and resolving significant hardware/software interface problems.
- Exceptional competence in system test and demonstration.
- Schedule performance within stated program requirements.
- Cost performance well within initial estimates.
- Outstanding systems engineering contributions to the DMSP ground systems.
- Excellence in communications with management and customer.



Schultz Iverson Martin Lange Meehan

- Timely and effective support to the DMSP 5D-2, Flight 6 field operations at Vandenberg Air Force Base.

Cornett wins GCS Technical Excellence Award

The Government Communications Systems Technical Excellence Award has been made to **John S. Cornett** of Software Engineering for his outstanding and singular accomplishment in the software development for the front-end processor subsystem of the Functional Signal Simulator System. John coded, debugged, tested, documented and integrated his software in a little over six calendar months. Eleven to thirteen months are considered normal for an assignment of this scope. He succeeded in delivering a quality software product despite the time constraints, and his off-site fixes of on-site problems have worked the first time in all cases. The successful completion of this project and the one that preceded it have demonstrated to the customer RCA's capability to produce complex systems with extremely tight schedules and limited manpower. This effort has enhanced our reputation and led to a sole-source follow-on procurement for a new type of system.

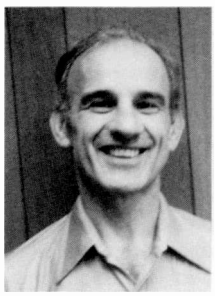
Government Communications Systems' Technical Excellence Award

Herbert Rubenstein of Systems Engineering received the Technical Excellence Award for his outstanding work in his support of Project E to Aerospace Systems in Burlington, Mass.

Specifically, Herb was required to evaluate the nuclear survivability/vulnerability requirements of a classified airborne system, confirm their justification, and establish realistic requirements. Herb executed a very detailed and complex field-theory analysis of the electromagnetic pulse (EMP) environment. He demonstrated that the specified requirements were excessive and unrealistic.

Evaluation of Herb's recommendations by Air Force EMP specialists resulted in a more appropriate specification level, and led to a formal citation by the Air Force acknowledging Mr. Rubenstein's personal professionalism and contribution to the program. Particular emphasis was placed on the fact that this work exemplified the type of DoD/industry technical dialog beneficial to both parties.

Mountaintop Technical Excellence winners announced



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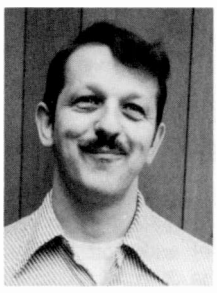

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Editorial Representatives

Contact your Editorial Representative at the TACNET numbers listed here to schedule technical papers and announce your professional activities.

Cablevision Systems

		TACNET
*John Ovnick	Van Nuys, California	534-3011

Commercial Communications Systems Division (CCSD)

*Bill Sepich	Camden, New Jersey	222-2156
Clinton Glenn	Meadowlands, Pennsylvania	228-6231

Consumer Electronics (CE)

*Eugene Janson	Indianapolis, Indiana	422-5208
Francis Holt	Indianapolis, Indiana	422-5217
Byron Taylor	Indianapolis, Indiana	426-3247
Don Willis	Indianapolis, Indiana	422-5883

Government Systems Division (GSD)

Advanced Technology Laboratories

*Merle Pietz	Camden, New Jersey	222-2161
Ed Master	Camden, New Jersey	222-2731

Astro-Electronics

*Frank Yannotti	Princeton, New Jersey	229-2544
Carol Klarmann	Princeton, New Jersey	229-2919

Automated Systems

*Paul Seeley	Burlington, Massachusetts	326-3095
Dale Sherman	Burlington, Massachusetts	326-3403

Government Communications Systems

*Dan Tannenbaum	Camden, New Jersey	222-3081
Thomas Altgilbers	Camden, New Jersey	222-3351

GSD Staff

*Peter Hahn	Cherry Hill, New Jersey	222-5319

Missile and Surface Radar

*Don Higgs	Moorestown, New Jersey	224-2836
Graham Boose	Moorestown, New Jersey	224-3680
Jack Friedman	Moorestown, New Jersey	224-2112

National Broadcasting Company (NBC)

*Bob Mausler	New York, New York	324-4869

Patent Operations

George Haas	Princeton, New Jersey	226-2491

RCA Communications

American Communications

*Murray Rosenthal	Princeton, New Jersey	258-4192
Carolyn Powell	Princeton, New Jersey	258-4194

Global Communications

*Dorothy Unger	New York, New York	323-7348

RCA Inc. (Canada)

		TACNET
Bob McIntyre	Ste Anne de Bellevue	514-457-9000

RCA Records

*Greg Bogantz	Indianapolis, Indiana	424-6141

RCA Service Company

*Murray Kaminsky	Cherry Hill, New Jersey	222-6247
Dick Dombrosky	Cherry Hill, New Jersey	222-4414
Ray MacWilliams	Cherry Hill, New Jersey	222-5986

Corporate Technology

*Hans Jenny	Cherry Hill, New Jersey	222-4251

RCA Laboratories

Eva Dukes	Princeton, New Jersey	226-2882

"SelectaVision" VideoDisc Operations

*Nelson Crooks	Indianapolis, Indiana	426-3164

Solid State Division (SSD)

*John Schoen	Somerville, New Jersey	325-6467

Power Devices

Harold Ronan	Mountaintop, Pennsylvania	327-1633 or 327-1827

Integrated Circuits

Dick Morey	Palm Beach Gardens, Florida	722-1262
Sy Silverstein	Somerville, New Jersey	325-6168
John Young	Findlay, Ohio	425-1307

Electro-Optics and Power Devices

John Grosh	Lancaster, Pennsylvania	227-2077

Video Component and Display Division

*Ed Madenford	Lancaster, Pennsylvania	227-3657
Nick Meena	Circleville, Ohio	432-1228
Jack Nubani	Scranton, Pennsylvania	329-1499
J.R. Reece	Marion, Indiana	427-5566

***Technical Publications Administrators, responsible for review and approval of papers and presentations, are indicated here with asterisks before their names.**

RCA Engineer

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