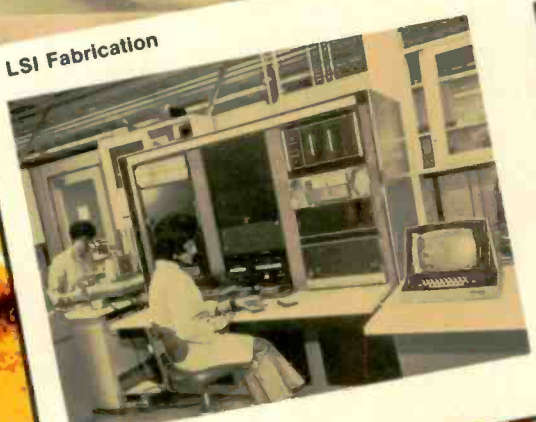
RCA Engineer

Vol. 26 No.2 Sept./Oct. 1980

LSI Design

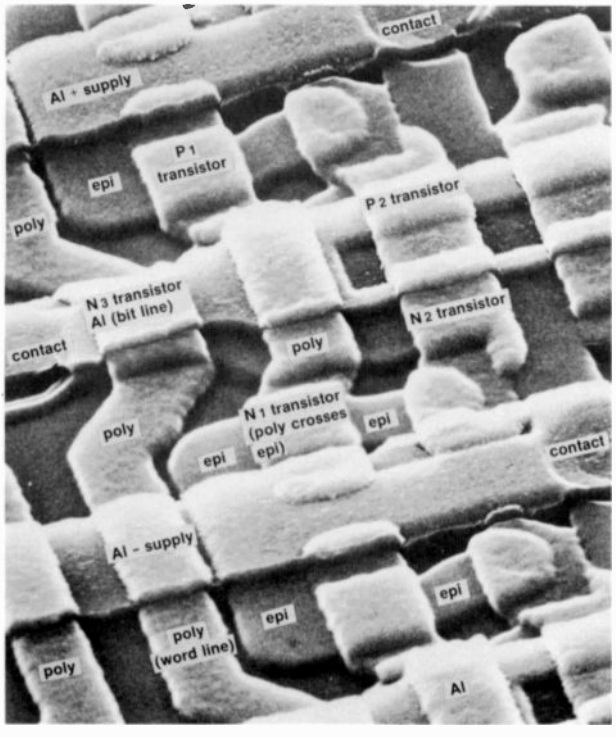
LSI Fabrication

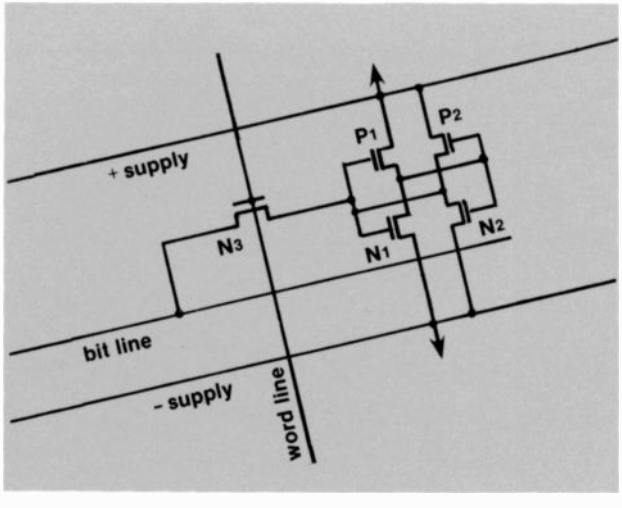


LSI Testing

LSI Application

LSI





Roger Stewart at the Solid State Technology Center (SSTC) gave us a black-and-white scanning electron photomicrograph of a CMOS/SOS buried-contact memory cell. Our printer added color via a special posterization process. Then we superimposed photographs showing the design, fabrication, testing and application aspects of large scale integration (LSI) for this special issue.

We've printed the original photograph, labeled it, and put Roger's schematic diagram below it so that you can see the five cross-coupled transistors forming the memory cell. There are three layers of material. The epitaxial silicon (epi) layer is the base layer, the polysilicon (poly) forms "word lines" that run top to bottom in the photo in the middle layer and the aluminum metal lines, "the bit lines," run diagonally on the top layer. Poly crosses epi where the transistors are located.

Good CMOS technology efficiently interconnects the three layers of material. Before, CMOS makers painstakingly interconnected all layers to metal. Today at RCA, with the help of Andy Dingwall (see article with Roger Stricker, p. 71) and other SSTC and division researchers, poly and epi in buried contact with each other form an efficient subterranean connection.

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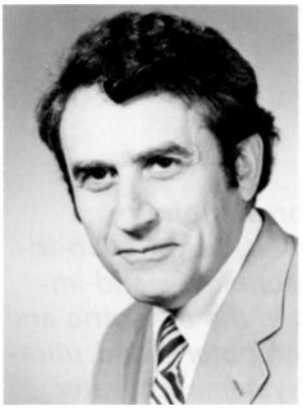


Henry Kressel

Human resources interconnect for VLSI

The economic power of nations used to be measured by steel production or shipbuilding. Now we are entering an age when microelectronics — wafer fabrication and chipbuilding — will become an important gauge of national technological competence. Microelectronics has reached center stage in corporate and national economic planning because complex integrated circuits form the heart of electronic systems.

Microelectronics success requires silicon — the most common raw material, and the dedicated efforts of very skillful teams of specialists in materials, computer science and electronic design — the scarcest resource. RCA has its share of the scarce human resources vital to success in microelectronics, and a distinguished record of innovation. RCA's management is dedicated to increasing our microelectronic ability both for the marketplace and for our internal needs.

The eighties will be the decade of circuitry featuring very large scale integration (VLSI) with more than 100,000 metal-oxide semiconductor (MOS) transistors per chip. The timely realization of such complex devices requires a highly-disciplined team effort that addresses, starting in the early developmental stages, issues of design, manufacture, reliability and testing. The production of these VLSI devices with micron-sized features will require increasingly complex equipment, computer-aided design and our understanding of physical and chemical phenomena that, before now, were inconsequential in integrated circuit fabrication. This issue of the *RCA Engineer* presents subjects ranging from the advanced process technology plans for the SSTC to the applications of custom integrated circuits to communications systems, broadcast equipment and consumer electronic products.

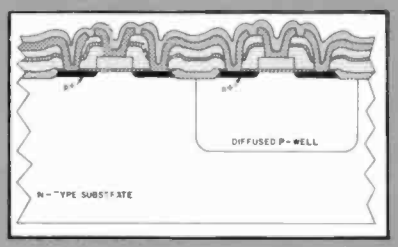
The successful manufacturers of VLSI devices will have masterfully managed the efforts of many specialists to achieve closely defined goals. The chain of interlocking skills will begin in the research laboratory, extend into the factory and end with the successful VLSI system performance. Working closely with the Solid State Division and other users, the David Sarnoff Research Center in Princeton, and the Solid State Technology Center (SSTC) in Somerville will continue to play vital roles in expanding RCA's solid state abilities.

Hey Kressel

Henry Kressel
Staff Vice-President
Solid State Technology
RCA Laboratories

Highlights

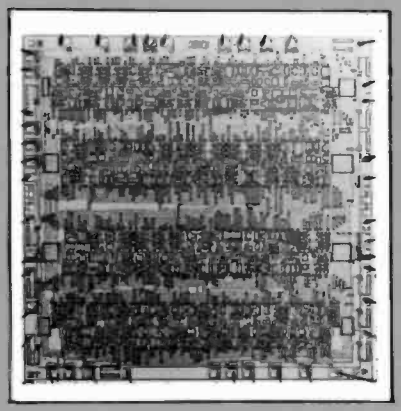
in this issue...



Fabrication technologies *include improved photolithographic and etching techniques for ICs with two-to-three micron gate-lengths; process techniques and improved cleanliness to reduce defects in the dielectric and interconnect layers on IC chips; and computer-aided, ultra-precise, closed-loop manufacturing systems for wafer processing.* *See articles on pages 4, 8, 18, 24, 29.*

Computer-aided design and testing *tools must keep up with the growth in IC complexity and the demands for: system, logic, circuit and process design; physical implementation (layout); test generation (fault coverage) and test data analysis; and verification/simulation at all levels. More importantly, the new tools and approaches must be practical enough to be accepted and used routinely.* *See articles on pages 33, 42, 46, 53.*

TEST	VECTOR
SA0	14
SA1	10
SA1	3



Applications *for the new LSI and VLSI technologies in this issue include 72 CMOS gate-universal-array applications implemented by nine different RCA division-locations; the Government Communications Systems' TENLEY/SEELEY program applications; CMOS random-access memories (RAMs); and more.* *See articles on pages 58, 64, 71.*

In future issues...

communications trends, mechanical engineering, human aspects of engineering, computer-aided design and manufacturing.

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I. Kalish

VLSI dimensions, designs and decisions

VLSI circuits designed without error and fabricated without flaw pose tough technical problems, but the decisions and cost-considerations that go into VLSI implementation in real electronic systems may be the hardest ones of all.

Abstract: *VLSI memory development has meant new fabrication and design problems but, for the most part, VLSI fabrication is upon us. The extreme complexity of VLSI circuitry poses design, simulation and testing problems but computer-aided design has attacked these problems. The hard decisions are between catalog parts and custom designs, between NMOS and CMOS technology.*

Twenty years of vigorous innovation, creative exploitation of the laws of nature and man's tools have carried semiconductor technology from the excitement of a single resistor-transistor logic (RTL) gate in a package to the routine expectation of 100,000-gate complexes. This transition signals the advent of VLSI, Very Large Scale Integration.

VLSI dimensions

The development of fabrication methods to make hundreds of thousands of components per package has meant more than just supplying systems designers with more functions at lower cost. It has drastically altered the strategy and the timing of the semiconductor product generation cycle. Figure 1 summarizes the traditional steps leading to a semiconductor product.

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Engineers use the electrical needs of a system to define the product. In the design phase, they generate a schematic and make a layout to establish the masks needed for fabrication. If evaluation confirms that the design meets system goals, the device can proceed into production. If the evaluation reveals design shortcomings, then that phase of the cycle is repeated.

To develop simple semiconductor functional electronic blocks, most engineers worked to define and refine the fabrication phase. They optimized technology to achieve the highest device performance consistent with practical manufacturing yields. Usually the definition, design and evaluation phases would take less than one year of engineering effort. VLSI has altered the effort allocation drastically. With the exception of memory development — and that exception is a major one — the developers of a VLSI circuit must assume that no new technology needs to be developed for its fabrication. It presupposes that a technology exists, usually as a result of a memory development effort, capable of fabricating and interconnecting thousands of components simultaneously. That technology is defined in terms of processing schedules for the factory and in terms of design rules for the designer. Table I lists some important design rules associated with MOS technologies. Their significance in determining the minimum device structure is illustrated in Fig. 2.

The design rules, together with modeling

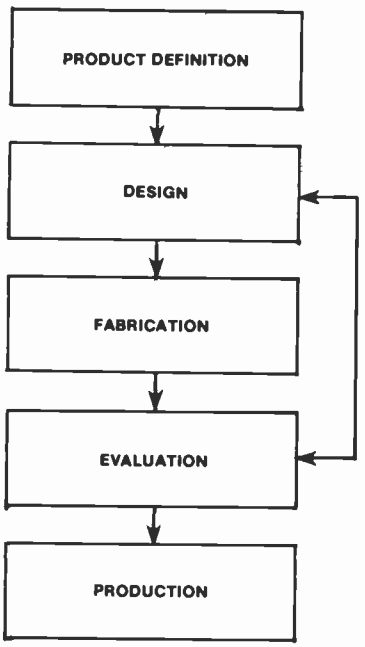


Fig. 1. Steps leading to a semiconductor product.

equations, provide the circuit designer with the transconductances, resistances and capacitances associated with the chosen

Table I. VLSI design rules.

	1980	1985
Channel length	2-5μm	1-2μm
Minimum contact	4μm x 4μm	2μm x 2μm
Metal width and spacing	10μm	6μm
Minimum feature spacing	1μm	.5μm

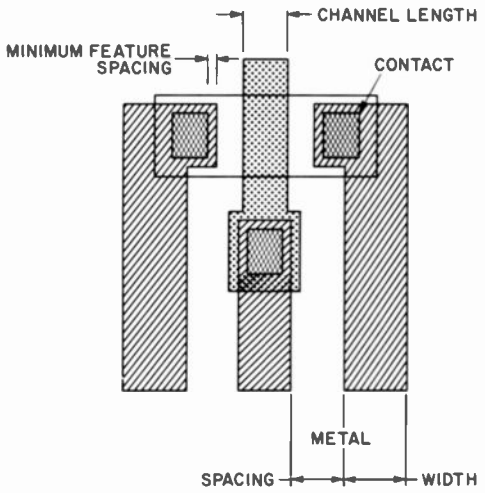


Fig. 2. Significance of VLSI design rules in determining minimum device structure.

technology and, therefore, permit the valid prediction of both circuit performance and chip size. Thus, the following problems remain: given 100,000 transistors of known electrical ability, how can we apply and interconnect all transistors to achieve a desired system function, and how can we verify, through appropriate testing, that the complex arrays will function satisfactorily even under worst-case conditions of both system-environment and process-related parametric variations? The successful solutions to these problems can require ten-to-twenty engineering years and a real-time expenditure of one-to-three years. The availability of human technical resources is the major problem limiting the growth of VLSI technology.

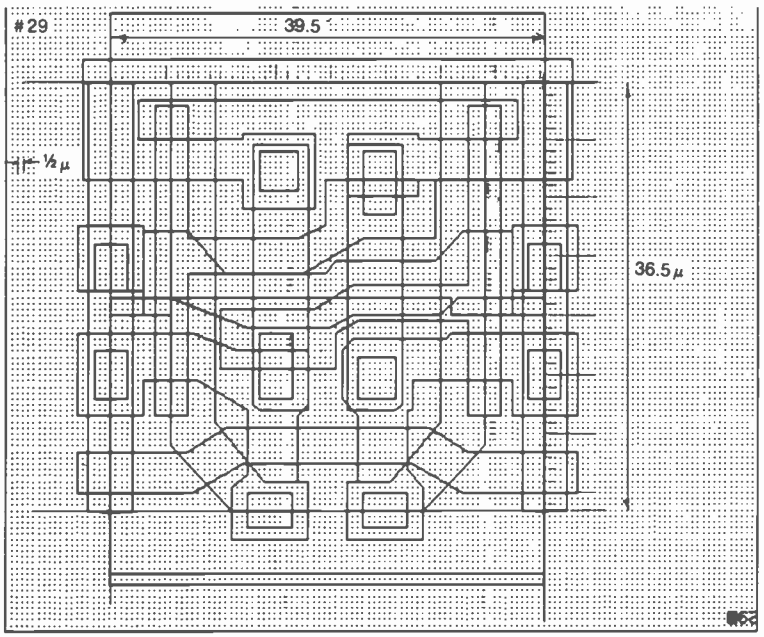
VLSI designs

Unlike other forms of VLSI, the development of semiconductor memories has meant the development of new technology. System requirements for semiconductor memories have been clearly defined — more, More, MORE! The acronyms have evolved from PMOS to NMOS to high-density NMOS to SOS and the features have diminished from mils to microns in response to a still insatiable demand for more bits-per-package. A specific memory design's universal applications and high-volume use have justified mammoth investments for engineering and for capital to establish the needed fabrication technology.

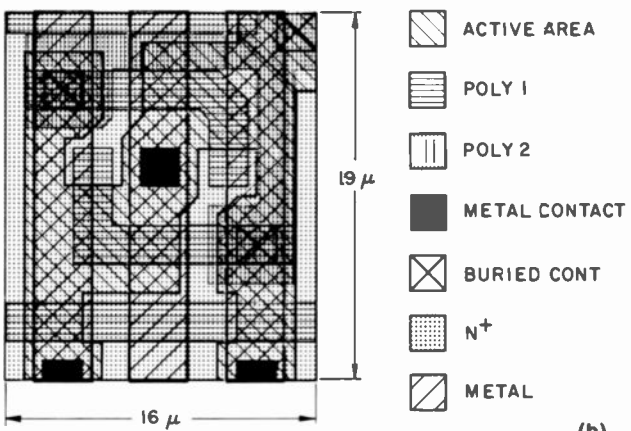
In the last five years, memory-cell sizes have shrunk from five square-mils-per-bit to less than one square-mil-per-bit, making 64K memories commercially feasible. A combination of circuit design, advanced technology and innovative device structures has increased this functional density. For example, dynamic memories offer the greatest functional density because capacitors store the information, thus making one-transistor memory cells possible. But customers need memories that can retain information indefinitely, so circuitry was developed to refresh (replace) the charge that tends to leak away. In addition, circuit advances in the sense amplifiers of memory circuits permitted the detection of extremely small packets of charge, making it possible to use minimum-sized storage capacitors. Clearly, advanced technology — mask-making, photolithographic resolution improvements and anisotropic plasma-etching techniques — has reduced minimum feature sizes.

Figure 3 shows how innovative device structures improve density. Both structures exemplify arrays of static memory cells designed using the limits of RCA's developmental three-micron CMOS II technology. The cells in Fig. 3a use a straightforward isoplanar silicon-gate CMOS technology and, because of the advanced design rules of the CMOS II technology, can be as dense as two square-mils-per-bit. The cells in Fig. 3b, in addition to exploiting advanced design rules, assume the increased process complexity of a two-level polysilicon process that can be used to achieve more efficient circuit crossovers and smaller load elements. This design approach results in a density of 0.6 square-mil-per-bit, a density compatible with the practical production of a 64K static memory. Figure 4, a scanning electron photomicrograph of a multiple polysilicon structure, illustrates vertical as well as horizontal structures in device design.

VLSI exploits technologies developed



TC1259 ALL METAL INTERCONNECTIONS — CELL AREA 2.24 MIL² **(a)**



DOUBLE POLY CELL **(b)**

Fig. 3. Arrays of static memory cells designed using RCA's developmental three-micron CMOS II technology.

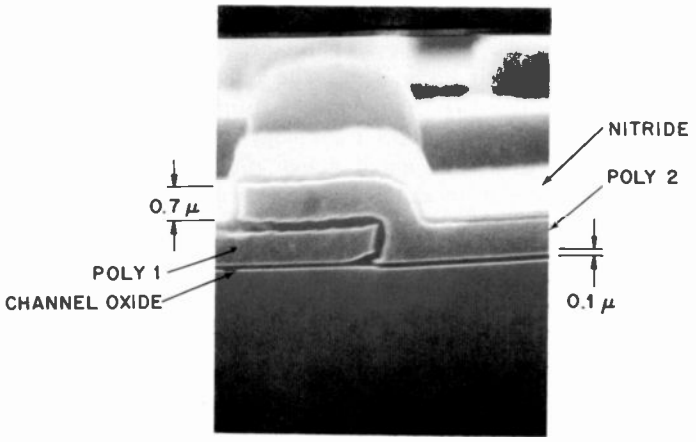


Fig. 4. SEM of multiple polysilicon structure.

Table II. CAD programs for LSI and VLSI.

Program name	*Function*
R-CAP	Circuit simulation program
LOGSIM	Logic simulation Time-based (gate delays)
TESTGEN	Logic simulation Worst cast hazard analysis
ART	Mask artwork manipulation
CRITIC	Design-rule checking
APAR	Automatic placement and routing programs MP2D, PP2D
AUTOROM	Automatic generation of pattern-generator and test programs from bit-pattern file

for high density memories to achieve complex logic functions. Also, as mentioned earlier, the design and evaluation phases demand a major engineering effort. Human talent for creative genius often is accompanied by human frailty and the potential for error. So, even a massive investment of talent in a complex microprocessor program would not guarantee success in a reasonable amount of time. This problem has been attacked through the innovative development of a number of programs for computer-aided design (CAD). These programs permit the designer to calculate the performance of a given schematic in terms of a potential technology, to validate an approach to implementing a given logic function, to define the topological interconnections needed to achieve a function using standard logic blocks, to generate the photomask patterns needed for device fabrication, and to define, automatically, test routines that will evaluate the finished devices. Table II describes some of the CAD programs now actively used by RCA LSI and VLSI designers.

VLSI decisions

Assuming that VLSI circuits can be designed without error, then fabricated without flaw, we will consider other aspects of VLSI implementation in a real electronic system. For example, should we use a standard catalog part or a custom design? The advantages of a custom part include the potential for a minimum parts count, a possible proprietary advantage in the use of an exceptionally high-performance design approach, and unique system-interface requirements. The advantages of catalog parts include lower cost, more predictable delivery, an established reliability history and more fully characterized designs. The disadvantages of custom designs include higher cost because the parts are usually made in lower volume, unreliable delivery because the design and evaluation cycles are unpredictable, and an increased probability that unanticipated bugs will be discovered during system prove-out. VLSI catalog functions include random access memories (RAMs), read only memories (ROMs) and microprocessors. Except in high volume applications such as automotive electronics, custom designs of such parts are rarely justified. Where LSI or VLSI custom parts are justified, different approaches can be taken to minimize risks. One of these approaches is the use of universal arrays.

A universal array is a circuit consisting of a matrix of identical logic elements, such

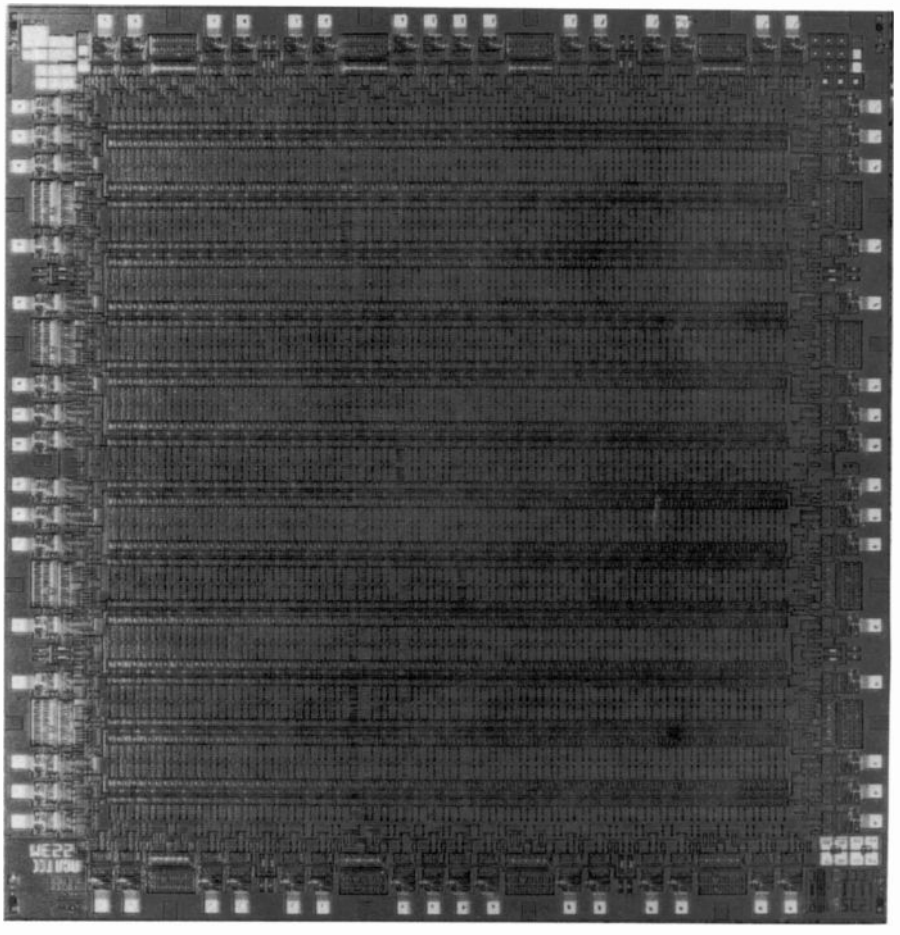


Fig. 5. Closed-cell logic (C^2L) circuit used to implement the PRIMUS color weather radar display program.

as gates. We can use the same array to implement many logic functions simply by modifying one mask level — the metallization used to interconnect the elements. This significantly reduces the engineering design time and, because the basic circuit elements have been proved out in other configurations, assures that the design will perform as predicted. The disadvantages of the universal-array approach are poor packing density and, because device geometries cannot be customized, less than the maximum speed inherent in a given technology. Where reduced package count is a primary system goal, however, the universal-array approach has been used very effectively. Figure 5 is a photograph of one of the closed-cell logic (C^2L) circuits used by RCA's Van Nuys Avionics Division to implement its successful PRIMUS color weather radar display program.

Figure 6 illustrates an automatic standard cell layout program that minimizes the need for design engineering. This approach, APAR (automatic placement and routing), also uses standardized building blocks to accomplish complex logic. Instead of the handful of different elements available in the universal-array approach, hundreds of different building blocks are available. These blocks are not located in prediffused positions on a silicon wafer. They are software definitions in a computer memory. A computer program is used to transform the logical requirements of a function into an array of optimally chosen and optimally interconnected elements.

A disadvantage of the APAR approach is that new masks have to be generated for all processing levels. This increases initial engineering costs and processing time, but these increases represent only a small part of the total design cycle and are usually justified by the increased density and performance of APAR designs. Figure 6 illustrates the application of APAR to implement a general processing unit function using SOS technology. Clearly, the APAR packing density is an improvement over the universal-array packing density. The large percentage of chip area devoted to metal interconnections is particularly significant. The number of components on a memory-structure chip is primarily limited by the size of the elements. In contrast, VLSI areas are limited by inefficient interconnections between random logic elements.

System requirements and cost-considerations primarily determine the technology chosen for VLSI. Most industry LSI approaches exploit the high density and performance of the dynamic NMOS approach for most applications, and use bipolar technologies where maximum speed is crucial. CMOS approaches excel where power, noise margin and ambient operating ranges are more important. The high component count of VLSI makes power a primary consideration because capacitively dissipated power will significantly limit the density advantage of dynamic NMOS approaches. The bipolar speed advantage is being eroded increasingly by the performance of short-channel (one-to-three microns) MOS structures. For these reasons, a high-density version of the CMOS technology that exploits short-channel, isoplanar and multiple-level interconnection options will emerge as the mainstream VLSI technology.

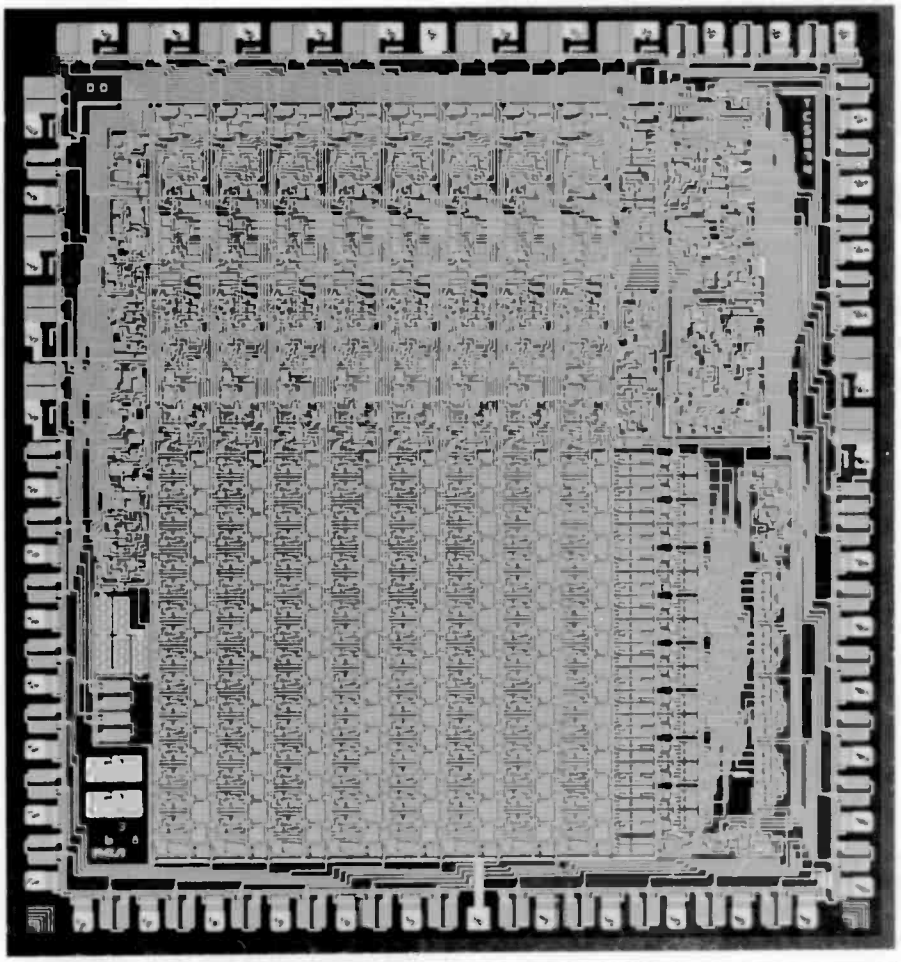


Fig. 6. The APAR circuit-design approach uses standardized building blocks to accomplish complex logic.

Iz Kalish has been involved in the design and development of semiconductor devices since joining RCA in 1953. He is presently Manager of the IC Design and Process Development group of the Solid State Technology Center where he is responsible for the development of the next generation of VLSI technology needed to implement high performance memories and microprocessors in both bipolar and field effect devices. Iz has authored several papers on semiconductor devices and a book, *Microminiature Electronics*.

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E.C. Douglas

Advanced process technology at the Solid State Technology Center

Teams at the Solid State Technology Center are exploring formable tools and process innovations to fabricate the next generation of high-density complementary metal-oxide semiconductor circuits.

Abstract: *The component density of metal-oxide-semiconductor integrated circuits (MOS IC) has been increasing rapidly in recent years and these trends toward larger circuit complexity and smaller individual component size have required a continuous refinement and advancement of process technology. This paper describes how RCA's Solid State Technology Center (SSTC) is meeting the challenge of very large scale integrated (VLSI) circuits with development programs in key technology areas.*

The challenge of high-density technology

The metal-oxide-semiconductor integrated circuit (MOS IC) industry has been characterized by an extremely rapid growth from medium scale integration (MSI) in 1965, (10^1 to 10^2 gates per chip) to very large scale integration (VLSI) manufacturable today, (10^4 to 10^5 gates per chip). Figure 1 shows the trend of this growth in gate complexity for both RCA's CMOS technology[1] and the NMOS technology[2] that is popularly used by other MOS IC manufacturers. Figure 1 also shows the actual and the projected growths of MOS IC die size[2]. These trends toward larger circuit complexity and smaller individual component size have required a continuous refinement and advancement of process technology in order to maintain high yields and to achieve manufacturing cost effectiveness. If these trends are to continue at the pace projected in Fig. 1, then the challenge to be met is the development of advanced process technology which can produce larger sizes of defectless chips and, at the same time, can achieve smaller feature sizes within the chip.

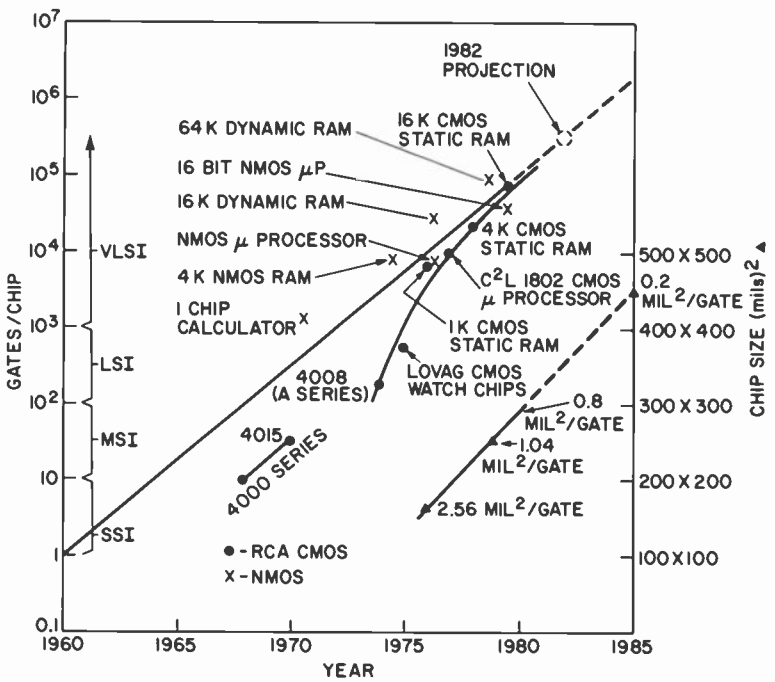

Fig. 1. Both the size and the density of integrated circuit chips has been increasing rapidly with time.

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A graphic illustration of the nature of this challenge is shown in Fig. 2 where the geometric structure of bulk transistors of gate lengths running from 7.5 to 2μm are shown. In order to keep up with the projected growth, photolithographic techniques and etching techniques which can controllably pattern 3μm and 2μm gate length structures must now be in the development stage. Since chip area is expected to increase by a factor of ~4 by 1985, process techniques must now be in the development stage which reduce the number of defects in the various dielectric and interconnect layers on the chips. In addition, increased cleanliness is required, both in layer-formation techniques and in the overall operation of the fabrication facility.

RCA's Solid State Technology Center is meeting the VLSI challenge on a broad front. Working on some projects in close cooperation with the Research Laboratories in both Princeton and Zurich, major process development programs are presently being pursued in the following areas:

- Fine-line photolithography
- Low-pressure chemical-vapor deposition (LPCVD)
- Direct digital control of thermal oxidation and diffusion
- Plasma etching
- Silicide metallization
- Upgrading of white room fabrication facility

In the following sections, the activities in each of these areas will be described and will be related to the overall SSTC goal of developing advanced processing for larger area, higher density integrated circuits.

Table I. Characteristics of contact and projection systems.

Technique	*Minimum feature size (μm)*	*Source wavelength (Å)*	*Overlay tolerance (μm)*	*Major limitations*
Contact	Submicron	Hg	0.5-0.75	defects, runout, mask cost, linewidth variation
Proximity	3-4	Hg Xe	0.5-0.75	minimum geometry, defects, linewidth control
Projection				
1:1	2-3	Hg	0.5-0.75	minimum geometry
1:1 (deep UV)	~0.5	2400	?	source, optics, resist availability
Direct step on wafer (DSW)	1.25-1.8	4040	0.125-0.35	accommodation of wafer distortion
X-ray	~0.3	4-8	?	source complexity, mask structure, registration
Electron beam direct write on wafer	0.1-0.2	—	0.1-0.3	cost, throughput

Fine-line photolithography

As the density of integrated circuits increases, limits are placed on both the minimum feature size that can be photoprinted and the control which can be achieved in the photoprinting process. Table I[3] summarizes the characteristics and major limitations of the photoprinting techniques which are presently being investigated by the IC industry. Proximity printing, 1:1 projecting printing, and direct-step-on wafer techniques are actively being studied at SSTC. In addition to using various types of photoprinters, automatic equipment is being used to coat wafers with photoresist and to develop the exposed wafer, thereby achieving a high degree of control and reproducibility in the chemical processing of photoresist.

Table I shows that although contact

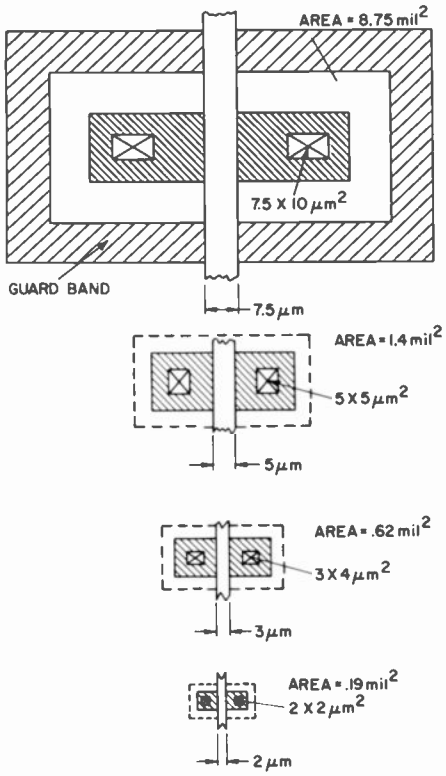


Fig. 2. A graphic illustration of the decrease in the area required for a bulk transistor as the gate length is decreased.

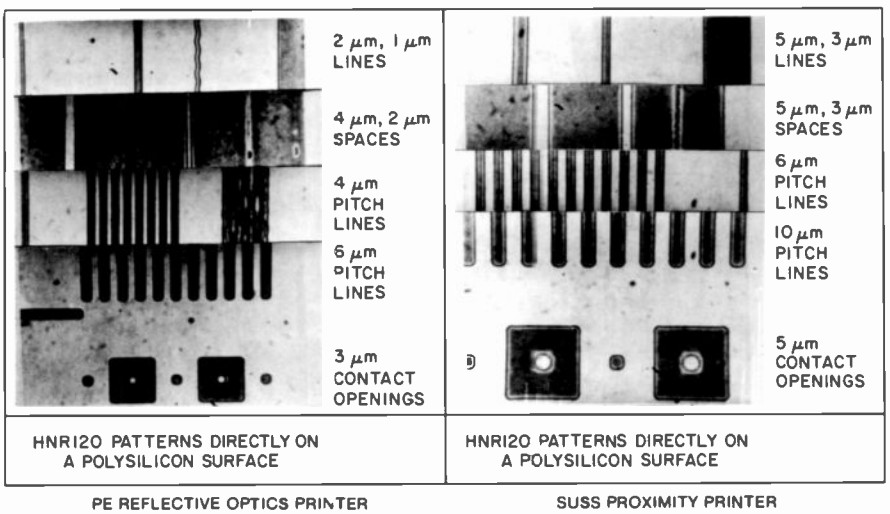


Fig. 3. Performance of various photo-printers. The dimensions given are those on the mask which was used to print the pattern. Each set of patterns was made with the same exposure, i.e., each set comes from the same wafer.

printing is capable of replicating submicron feature sizes, contact printing is unsuitable for VLSI applications because of the defects which are caused on both the photomask and the wafer by the contact process, and because of the runout which is caused by wafer/mask distortion when they are clamped together. For these reasons, even older, less demanding integrated circuit production is being shifted to the contactless proximity and image-projection techniques.

Proximity printing

A simple method of achieving contactless photoprinting is to space the mask a small distance from the wafer (2.5 to 25μm) and project a "shadow" of the mask onto the photoresist-coated wafer. This proximity-printing technique costs much less than image-projection systems since no lens is involved. The technique also has the flexibility of allowing the use of a wider range of illumination wavelengths which, like contact printing, is limited essentially only by mask transmissivity.

SSTC is experimenting with a Suss Model 55 Proximity Printer[4] and has found that feature sizes in the 3 to 5μm range can be printed under optimum conditions (Fig. 3). Since a proximity printer uses the diffraction-dominated shadow of a mask, the resulting exposed image (for the case of negative resist) is a trade-off between complete exposure, minimum resist-loss during development, and minimum "orange peel" on the one hand, and line-width deterioration and resist bridging on the other hand. Proximity printing also leaves noticeably rounded corners, and the nature of the surface underlying the photoresist can affect the exposed image. Polysilicon is the most difficult surface on which to pattern. The use of a broad-band, high-pressure, flashed-Xenon light source can minimize some of these problems by allowing a polychromatic printing-characteristic.

Reflective image projection

Image-projection techniques can improve the quality and control of contactless wafer-exposure. Early attempts in this direction used large-field, refractive lenses but were generally unsuccessful because of problems with lens aberrations, light scattering, temperature stability, telecentricity, focal depth and field coverage. Simply stated, it is hard to grind glass lens elements that can produce 3- to 4-inch diameter images with 1-to-2μm resolution. An alternate approach is to use reflective optics[5], and in addition to combine reflective optics with the scanning concept which reduces the complexity of the reflecting surface needed to cover a large field. The Perkin-Elmer 120 and 220 projection aligners used in SSTC are based on the scanning, reflective-optical principle which is diagrammed in Fig. 4.

Even though the accurately formed optical surfaces in a scanning reflective system are fewer in number and smaller in size when compared with the refractive system counterpart, the physical fabrication of a focusing mirror and its optical coating is still the limiting factor in 1:1 reflective-projection system. Improved measurement techniques, using a laser, allow the presently obtainable rms tolerances of finished optical surfaces to approach $\lambda/100$. This is sufficient to allow the printing of feature sizes in the 2-to-3μm range (Fig. 3).

Direct-step-on-wafer techniques

Direct-step-on-wafer (DSW) machines provide the printing technique with the optimum combination of minimum feature size and overlay tolerance[3,6]. This is achieved by using a 10:1 refractive projection system which employs a 10X reticle, projects and exposes an individual chip-size image on the wafer, and step-and-repeat-prints the number of chips needed to cover the wafer surface. Since the field size of a 10:1 reduction lens is relatively small, ~10mm (~400 mils) in diameter, stepper lenses can be fabricated to give ~1μm resolution capability. Figure 5 illustrates the operation of the Electromask 700SLR wafer stepper presently being used at SSTC.

The difficulties associated with a DSW machine are not in the lens. Positioning the

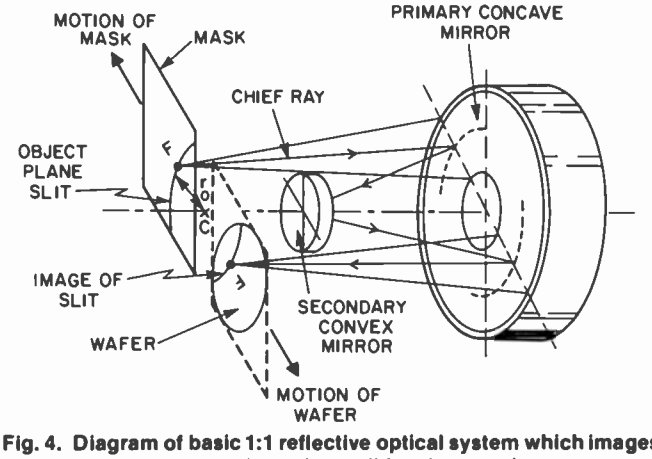


Fig. 4. Diagram of basic 1:1 reflective optical system which images a ring field (circular object plane slit) using a primary concave mirror and a secondary convex mirror. As shown, the mask and wafer must be translated in opposite directions at the same rate. In a real system, such as the Perkin Elmer (PE) 120 or 220, the optical path is bent with additional prisms so that both the mask and the wafer can be mounted on the same translating carriage.

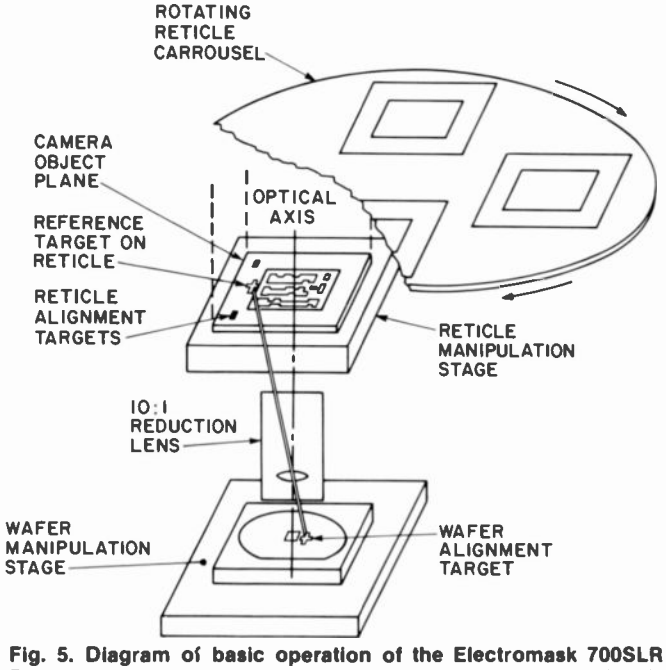


Fig. 5. Diagram of basic operation of the Electromask 700SLR Direct Step-on-Water 10:1 projection aligner. The machine is capable of automatic reticle changing, through the lens alignment, and $\pm$0.25 μm alignment tolerance.

wafer accurately during the stepping procedure, aligning the printing of each stepped exposure, and obtaining fast enough stepping operation in order to achieve a reasonable throughput are the difficulties. Positioning accuracy is achieved with a laser-interferometrically controlled air-bearing x-y table which is computer controlled and is capable of positioning accuracies within $\pm 0.25\mu m$. Alignment accuracy is achieved using a TV-based through-the-lens microscope system which aligns the 10X reticle directly to the wafer (Fig. 5). With only two alignments — one on each side of the wafer — the Electromask system is capable of overlay printing individual chips across the surface of a 3-inch wafer with $\pm 0.25\mu m$ overlay tolerance. Although the SSTC Electromask machine is not yet equipped with automatic alignment at each chip position, Electromask has developed such a system that can be retrofitted to the SSTC machine. All this automatic performance, however, makes it difficult to achieve high wafer throughput. With optimized printing of the largest available field and two automatic reticle changes per level of printing, the throughput of the Electromask machine will be between 30 and 50 wafers per hour.

Low-pressure chemical-vapor deposition — the quest for fewer defects

MOS ICs are fabricated by the systematic formation and patterning of layer upon layer of dielectric or interconnect materials. Figure 6 shows a diagram of such a layered structure which forms a complementary pair of bulk CMOS transistors (actual ICs may not use all of the layers shown). Of the eight layers used to fabricate the structure, six of them are deposited layers. For reliability and high yield, all eight layers should be perfectly uniform, with no included defects, and should contain no unwanted contaminants. In addition, as is evident from Fig. 6, the layers should conformally cover the various topological steps which result in the structure because of the patterning.

Until recently, the techniques used to deposit these layers have involved chemical-vapor deposition at atmospheric pressure which is in general plagued with problems of uniformity control and particulate formation[7]. The development of commercially available reactors for chemically depositing the required layers at much-reduced pressures (~0.5 torr) has helped to overcome these problems, and LPCVD reactors have already supplanted other techniques for forming silicon nitride (Si_3N_4) and undoped polysilicon layers. Work is presently underway at SSTC to establish LPCVD techniques for depositing both doped and undoped silicon dioxide (SiO_2) layers and for depositing doped polysilicon.

Two variants of the basic tubular LPCVD reactor are available, as shown in

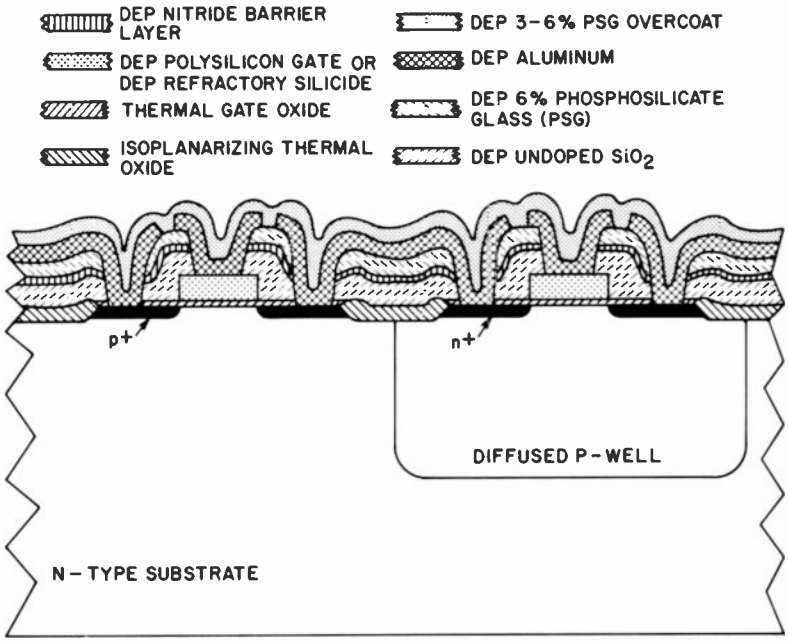


Fig. 6. Diagram of a layered structure forming a bulk CMOS complementary pair of transistors.

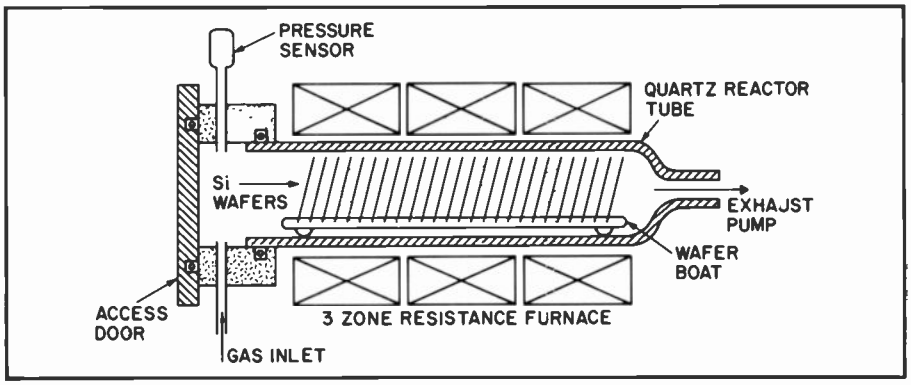


Fig. 7a. End-feed LPCVD reactor.

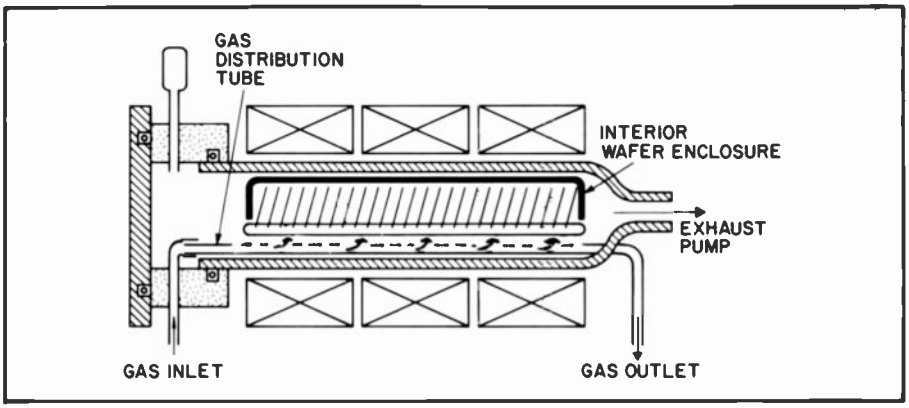


Fig. 7b. Distributed-feed LPCVD reactor.

Table II. Deposition processes available in commercial LPCVD reactors.

Layer	*Input gases*	*Deposition Temperature (°C)*	*Deposition rate** (Å/Min)*	*Reactor type*
Undoped SiO_2	SiH_4, O_2, N_2	400-430	100	Distributed
Doped SiO_2 (PSG)	SiH_4, PH_3, O_2, N_2	400-430	90-110	Distributed
Undoped Polysilicon	SiH_4, N_2	610-640	100-125	End feed
Doped* Polysilicon	SiH_4, N_2, PH_3	730	200	Distributed
Silicon Nitride (Si_3N_4)	SiH_2Cl_2 NH_3, N_2	740-800	40-65	End feed
High temperature Undoped SiO_2	SiH_2Cl_2, N_2, N_2O	960	120	End feed

*24 ohm/square layers, 3200Å thick, post-annealed for 30 min at 1000°C.

**The exhaust pump rate in all cases is 35-40 cfm.

Fig. 7. Either type of reactor can handle typically ~100 wafers per pump-down. The "end-feed" reactor shown in Fig. 7a was developed first and is used predominantly at higher deposition temperatures. Chemical vapor deposition processes are surface-catalyzed reactions, and if the reaction rate at the optimum deposition temperature is small compared to the mass transfer rate (the rate at which gas can be pumped through the tube), then the deposition process will be uniform because the density of active gaseous species is uniform, that is, the active species is not significantly depleted along the length of the tube. The optimum reaction conditions depend on temperature; Table II shows the conditions presently considered optimum for forming uniform layers of polysilicon, SiO_2, and Si_3N_4 using the end-feed reactor.

At temperatures lower than 950°C for the case of SiO_2 depositions (and at temperatures higher than 700°C in the case of undoped polysilicon), the pump rate cannot conveniently be made high enough to raise the mass-transfer rate above the reaction rate. Thus, in an end-feed reactor, non-uniform depositions occur both over the surface of a given wafer and as a function of the position of the wafer in the tube. This problem can be solved using the distributed-gas system shown in Fig. 7b and by using an enclosure inside the reactor which surrounds the wafers. Two parallel tubes run the length of the reactor, one carrying silane (SiH_4) and the other carrying oxygen (O_2) when SiO_2 is being deposited. These gases are injected into the interior wafer-enclosure uniformly along the length of the tube. Using this technique, the reacting species have a smaller distance to diffuse in order to reach all areas of all the wafers in the tube, hence significant active-species depletion is

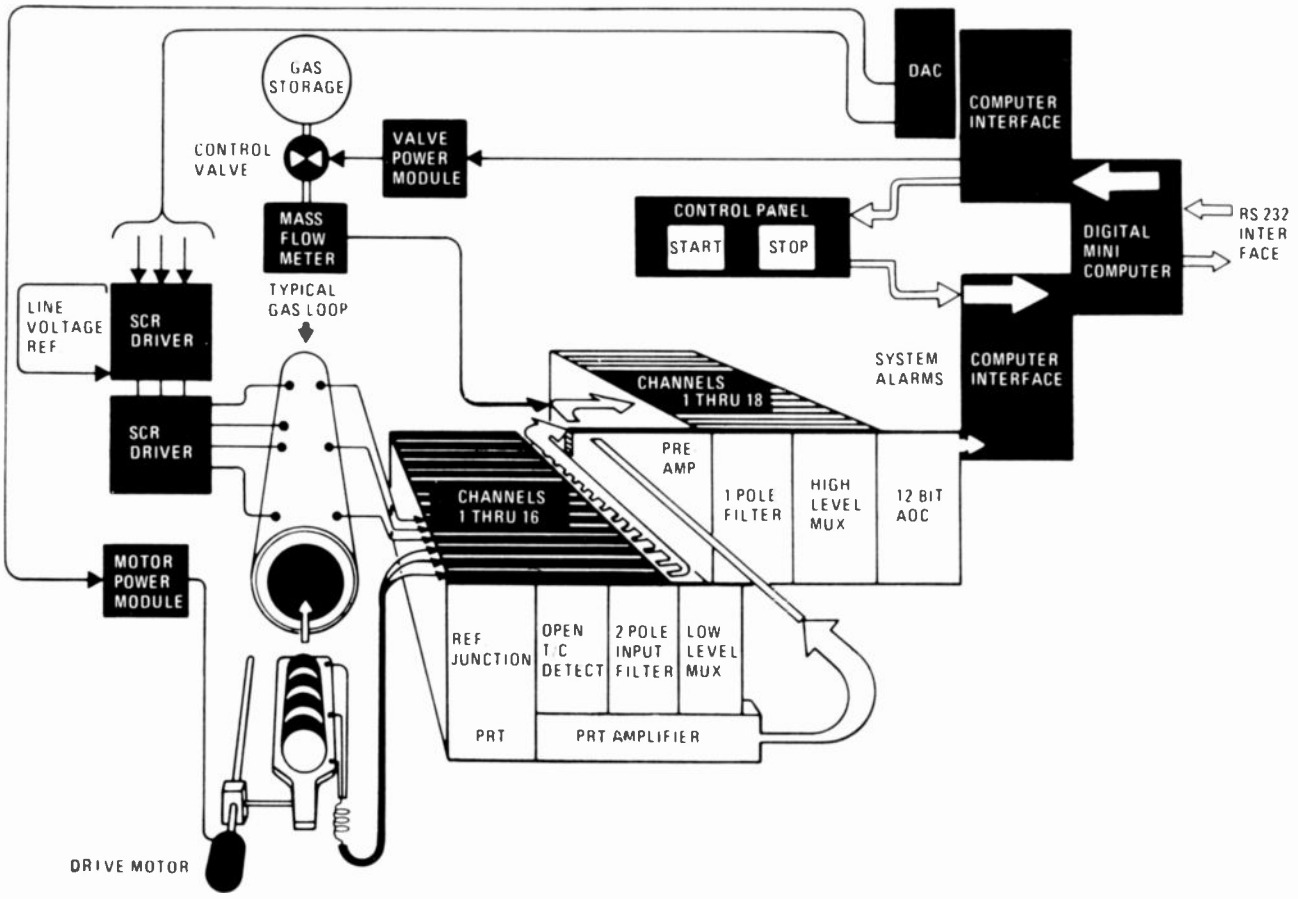


Fig. 8. Diagram of the electronic feedback systems used in a direct digital control (DDC) oxidation/diffusion furnace (Courtesy Thermco).

reduced over the region of a given wafer and hence deposition uniformity is increased. Layers of doped and undoped oxide having a ±5 percent variation can be achieved in the 400-500°C temperature range using the distributed-feed technique.

In those cases where depositions must be made in the 300-400°C temperature range, plasma-enhanced LPCVD can be used[8]. The use of a plasma to achieve chemical activation of layer deposition has the advantage of producing low-temperature films having good conformal coverage. A disadvantage of the technique is the odd stoichiometry that can result. Instead of the desired Si_3N_4, for example, one usually obtains $Si_xN_yH_z$ or $Si_xN_yH_zO_w$.

Because of the large number of wafers — typically ~100 — which can be uniformly deposited on in a single run, and because of the low-pressure operation, which uses much smaller amounts of reaction gas than reactors which operate at atmospheric pressure, LPCVD-deposition techniques are inherently more economical. Also, at the low pressures used, gas-phase nucleation is far less and hence particulate formation from this source is negligible. Deposition does occur on the reactor walls and on the wafer boat, but if the tube and boat are cleaned every 20th run in the case of undoped polysilicon when using a ~0.6μm deposition thickness per run, flaking is not a problem. The deposits on the hot tube walls are glassy and adherent, and any particles that may form have only a small chance of falling on the vertically-oriented wafers. With good uniformity and low layer defect potential, as well as the good conformal-coating properties, LPCVD is a natural for LSI applications[9].

Direct digital control of oxidation and diffusion

Although only two of the eight layers diagrammed in Fig. 6 are formed by thermal oxidation, significant oxidation, diffusion and annealing steps are required in the LSI fabrication sequence. The latter processing steps require that the wafers be inserted into and removed from high-temperature furnaces generally ranging in temperature from 800 to 1200°C. Besides the desired effects of oxide growth or dopant diffusion, this large thermal cycling of the wafers causes many undesirable side effects. These undesirable effects include the introduction of wafer-slip[10] due to insertion and/or removal from the furnaces at too rapid a rate, the introduction of oxidation-induced stacking faults[11] if improper pre-oxidation or post-oxidation ambients are used, or the precipitation of bulk-oxygen cluster-defects if incorrect post-processing anneals [12, 13] are used. These undesirable effects lead to MOS yield loss due to high leakages and individual transistor failure.

Greater control over the thermal processing of wafers can be obtained by using direct digitally controlled furnaces. A diagram of such a furnace system is shown in Fig. 8. The heart of the system is a microprocessor which organizes the overall furnace processing using feedback control loops. These control loops are used to insert and withdraw the wafer paddles at a specified rate, to raise or lower the furnace temperature at specified rates, to adjust the various gas flows as a function of time, and to monitor the actual temperature profile inside the furnace as a function of time. The microprocessor can, in addition, automatically clean the furnaces (using hydrochloric acid (HCl) or trichloroethane (TCA), perform an automatic calibration cycle and tailor the dynamic performance of the furnace to a given process step by appropriately adjusting the proportional band-control constants. Since these various furnace operations are specified in terms of a software instruction sequence, DDC furnaces provide a high degree of process reproducibility. All of these features can, of course, be achieved without digital control. But with digital control they can all be easily achieved at the same time. A disadvantage of digital control is that all control is lost if the computer system fails.

SSTC presently has 16 DDC 4-inch diameter tube furnaces and is actively developing LSI processing using their capabilities.

Plasma etching — transferring dimension accurately from mask to wafer

After fine-line photolithographic techniques have been used to define an etch mask (Fig. 9a), the next step is to etch the underlying dielectric or interconnect material with dimensional control. Plasma etching, or alternatively dry plasma-processing or dry etching, is a developing technology which promises to be critically important to the fabrication of high-density integrated circuits. Successful fabrication of high-density LSI requires etch control of fine lines. This etch control becomes difficult or impossible for wet chemical etching if the width of the line to

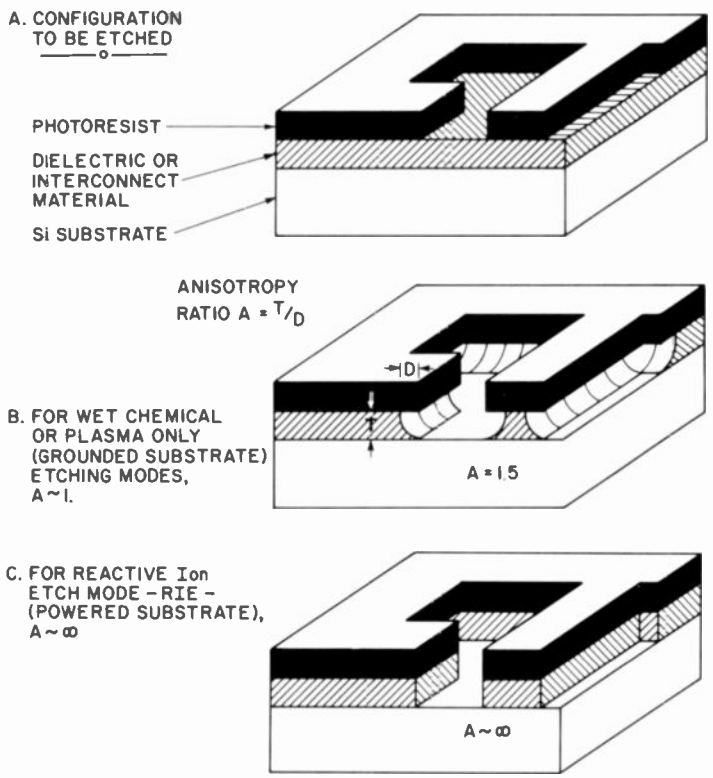
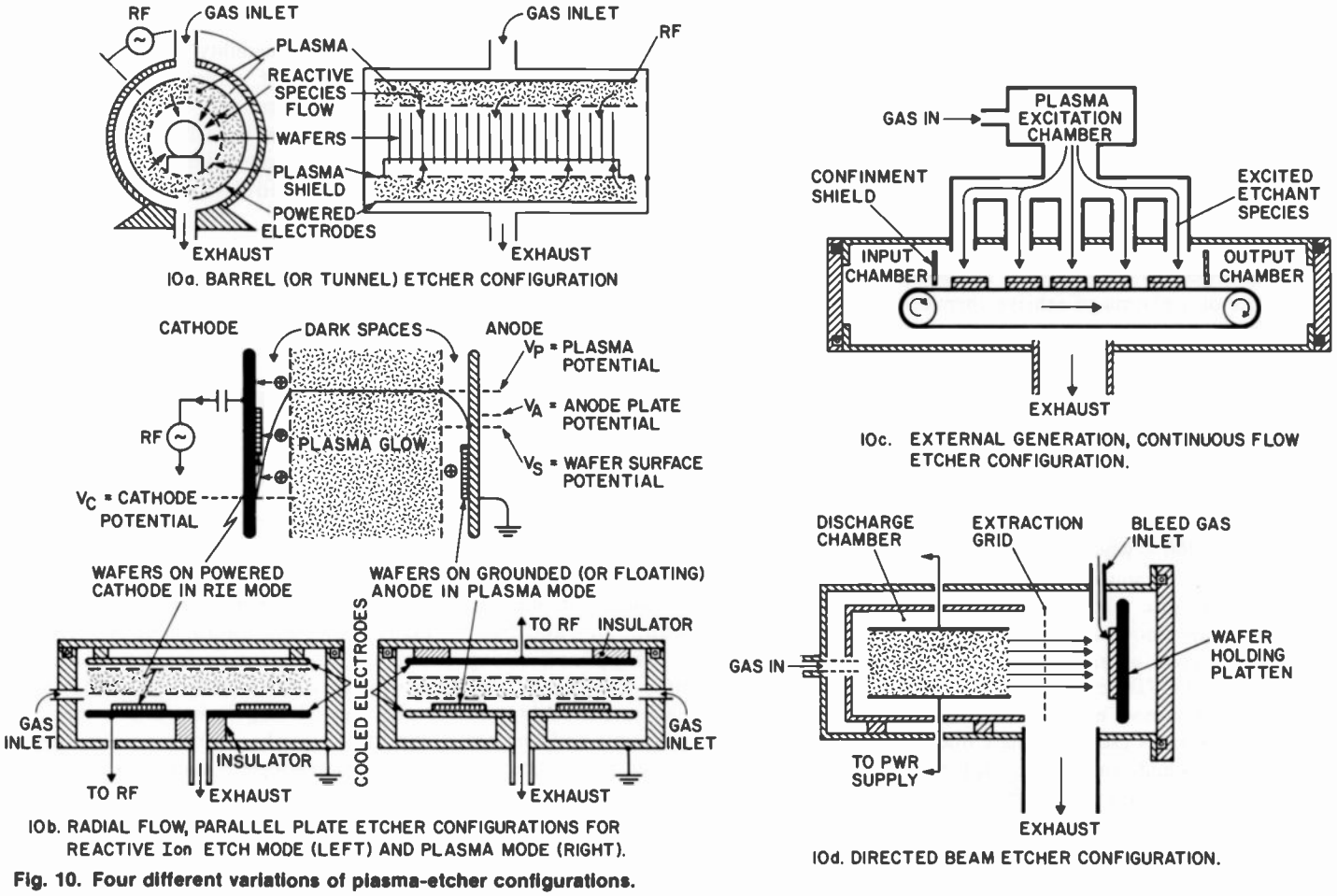


Fig. 9. Diagram of the etching process showing the starting configuration (A), and results when isotropic etching (A = T/D≃1) is used (B) or when anisotropic (C) etching (A~∞) is used.



IOa. BARREL (OR TUNNEL) ETCHER CONFIGURATION

IOb. RADIAL FLOW, PARALLEL PLATE ETCHER CONFIGURATIONS FOR REACTIVE Ion ETCH MODE (LEFT) AND PLASMA MODE (RIGHT).

IOc. EXTERNAL GENERATION, CONTINUOUS FLOW ETCHER CONFIGURATION.

IOd. DIRECTED BEAM ETCHER CONFIGURATION.

Fig. 10. Four different variations of plasma-etcher configurations.

be controlled approaches the thickness of the layer being etched. This difficulty is caused by the isotropic nature (Fig. 9b) of most wet chemical reactions and by the surface-tension effects associated with fluid flow which prevents the etchant and the reaction products from freely exchanging in confined surface topologies.

Plasma etching at low pressures overcomes these problems. Plasma processes are used to excite a normally inert gas to a chemically active species, and low-pressure surface-adsorption-desorption reactions — coupled at times with sputtering processes — allow good control of fine-line etching. By properly selecting reactor geometry and source-gas mixtures, a spectrum of controllable etching characteristics can be achieved which ranges from isotropic to highly anisotropic (Fig. 9c). This combination of features has caused the present intense interest in the development of dry-processing techniques for high-density LSI-circuit fabrication.

Four different varieties of plasma-etcher configurations (shown schematically in Fig. 10) are presently available for processing IC wafers. The barrel or tunnel reactor is shown in Fig. 10a. For this configuration, the wafers are held in a quartz boat inserted in the central "tunnel" portion of the cylindrical reactor. The plasma is excited, using an r.f. discharge, in a sheath region which surrounds the tunnel. The chemically active free radicals (i.e., excited neutrals) in the plasma diffuse to the wafers through holes in the central cylindrical plasma shield and react with the wafer surface causing etching through a reduced-pressure adsorption-reaction-desorption process. The etch products are pumped away by the exhaust system. Since no electric field exists in the central tunnel region, no ion bombardment takes place and the surface etching reaction is an isotropic, chemically driven process.

A second configuration, the radial-flow, parallel-plate reactor, is shown in Fig. 10b.

Table IIIa. Plasma generated species interaction with a solid surface.

Process	*A*	*B*
Etching species	Ions	Chemically active neutrals (radicals)
Driving force	Electric field	Diffusion
Arrival on surface	Highly directional	Random direction
Interaction with surface	Momentum transfer	Adsorption-reaction-desorption
Species leaving surface	Atom clusters	Gas molecules

Table IIIb. Processes occurring in various plasma-etch reactors.

Reactor	*Process combination*
Barrel	B
Parallel-plate RSE or RIE mode	A+B, A>B
Parallel-plate plasma	A+B, B>A
Continuous plasma flow	B
Directed beam	A+B+species activation on surface after adsorption

For this reactor configuration, the wafers to be etched are placed directly on the system circular-plate electrodes. Since an electric field exists in the vicinity of either electrode (see potential diagram in Fig. 10b), the wafers are not only exposed to the plasma-generated active chemical species, but also are exposed to bombardment sputtering by ions from the plasma. The magnitude of the electric field in front of each plate depends on: the applied voltages; the gas pressure; the plate separation; the secondary emission ratios of the wafers and the electrodes; and the geometric configuration of the reactor, for example the ratio of anode to cathode area[14]. The magnitude of the electric field in the vicinity of the cathode is generally the largest, and when the wafers are placed on the powered electrode (cathode) and the reactor is operated at low pressures (0.01 - 0.05 torr), the bombardment assisted plasma etching is called Reactive Sputter (Ion) Etching (RSE or RIE mode) which yields highly anisotropic etch results[15, 16, 17]. Verticle-walled structures (A~∞) have been obtained in SiO_2 which have an aspect ratio (height/width) of ~8[16].

When the wafers are placed on the anode, where the electric field is smaller, and the reactor is operated at somewhat higher pressure (0.1 - 0.5 torr), chemical processes dominate the etching and the etch results are closer to isotropic etching. By varying the wafer placement, the reactor pressure, or even powering both electrodes, a spectrum of etch characteristic from nearly isotropic (A~1) to nearly anisotropic (A ~∞) can be obtained. Tables IIIa and IIIb summarize the various etch processes. Although exposing the wafer directly to the plasma adds the extra dimension of physical sputtering and enhances the flexibility of parallel-plate etchers, it also introduces the disadvantage of increased radiation damage from the vacuum UV generated in the plasma. This can preclude the use of parallel-plate etchers for the fabrication of rad-hard products.

Two variations of the etcher configurations already discussed are shown in Figs. 10c and 10d. In the external generation, continuous-flow configuration, the chemically active species are generated in an external excitation chamber excited by a microwave discharge and then are sprayed onto the wafer surface using a manifold distribution arrangement. The etching properties here are the same as for the barrel reactor (Table IIIb). The directed beam etcher configuration shown in Fig. 10d forms a large-diameter ion

Table IV. Resistivity of various interconnect materials.

Material	*Resistivity η* ($\mu\Omega$-*cm*)	*Sheet resistance** (0.5μ*m layer*) (*ohms/square*)
Pure Al (alloy heated)	3.1-3.3	.062-.066
Al-1% Si (alloy heated)	3.5-3.6	.070-.072
Al-2% Si (alloy heated)	3.6-3.9	.072-.078
$TiSi_2$	15-20	0.3-0.4
$TaSi_2$, WSi_2	50-100	1-2
$MoSi_2$	100-150	2-3
n+ poly ($POCl_3$) (after laser annealing)	800-1000 (500-800)	15-20 (10-15)
p+ poly (boron doped oxide)	1750-2250	35-45
n+ poly (150eV p^{31}, $1.6\times10^{16}/cm^1$, 15 min. 1050°C)	800-1000	16-20
p+ poly (60KeV B^{11}, $1.6\times10^{16}/cm^2$, 15 min. 1050°C)	1250-1500	25-30
n+ poly (*in situ* doping, AMT/1200 reactor, 90 min. 850°C)	1000-1500	20-30

* Sheet resistance $\rho_s = \frac{\eta}{t}$ where t = layer thickness.

Resistance $R = \frac{L}{W}\rho_s$ where L and W are the length and width of the resistor structure.

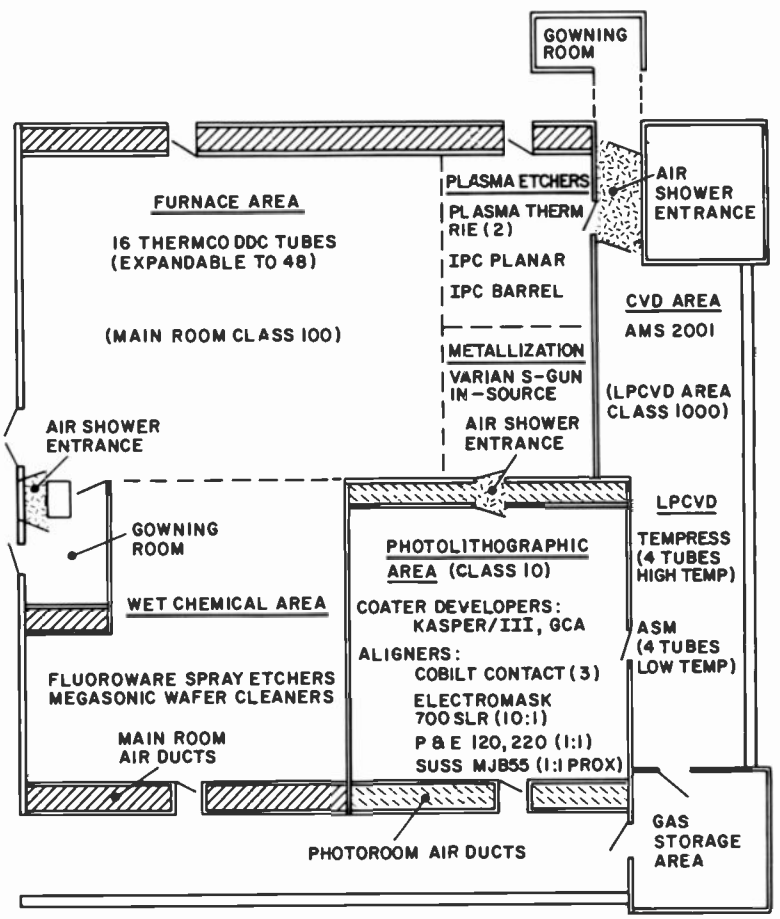


Fig. 11. Diagram of the white room fabrication facility in SSTC, Somerville, N.J.

beam using a discharge chamber and an extraction grid. This technique is similar to the RIE etch mode with the advantage that the ion bombardment energy is easier to control and can be adjusted to any desired value. This extra dimension of control combined with the single-wafer-at-a-time reactor design, can be used, for example, to activate (by bombardment) a species that has been introduced to the wafer surface through a bleed gas inlet and adsorbed onto the surface.

Routine plasma etching of polysilicon in barrel-type etchers using the CF_4-based chemistry is presently being used at SSTC to fabricate 5μm circuits. Active programs, both within SSTC and in cooperation with the Princeton Labs and the Zurich Labs, are underway to develop production-oriented, parallel-plate etchers for anisotropic etching of polysilicon, aluminum, and SiO_2 films.

Silicide metallization

As the density of integrated circuits increases, the device lateral dimensions and the layer thickness used must be scaled to smaller values. This includes the conductive interconnect layers of doped polysilicon and aluminum. If the layer conductivities (σ) or resistivities ($\eta = 1/\sigma$) are not also appropriately scaled, increased interconnect resistance will result which will lead to poor circuit performance. In some chips where circuit speed — low RC values — is critical, such as microprocessor or short-access-time memory chips, overall interconnect resistivity must be reduced even after scaling. As an example, in present memory chips using polysilicon access lines, RC delay accounts for ~5ns of the access time.

Table IV shows the resistivity of various interconnect materials. Polysilicon layers are presently widely used for both self-aligned structures and for structures requiring multilevel interconnects. The resistivities, however, are higher than desired. The low resistivity of aluminum cannot easily be exploited because process temperatures cannot exceed ~450°C after its use. A third class of materials, the refractory metal silicides, have resistivities between aluminum and doped polysilicon. These layers can be formed by alloying sputtered layers of polysilicon and refractory metal, titanium (Ti), tantalum (Ta), tungsten (W) or molybdenum (Mo); by co-sputtering the layers, for example, sputtering from a target made of tantalum silicide ($TaSi_2$); or by using chemical vapor deposition. RCA is exploring all three techniques at SSTC or at the Princeton Laboratories. Refractory-metal-silicide interconnect layers are targeted for use in the next generation of high-density LSI circuits.

The upgraded SSTC White Room facility

The successful fabrication of high-density integrated circuits requires, in addition to new processing techniques, a more carefully controlled fabrication environment. The SSTC White Room in Somerville has been renovated extensively to satisfy this environmental requirement. Figure 11 shows a layout of the SSTC White Room along with a listing of the major new pieces of equipment purchased to support the advanced process technology presently being developed.

The room is divided into three areas which are distinguished by the flow rate of the recirculated, filtered air. In all cases, the air is passed through high-efficiency particulate-air (HEPA) filters which remove all particulates over 0.2μm in size. Most of the particles larger than this are carried in by personnel, hence the need for dust-confining jumpsuits and air showers at the room entrances. The air-flow rate in the main room is adjusted to 65 linear-feet/min. The main room is Class 100, that is, an environment with a maximum of 100 particles per cubic foot with a size larger than 0.5μm and a maximum of 10 particles per cubic foot with a size larger than 5.0μm[19]. In a Class-100 room ~1 particle/cm^2-hour strikes a given wafer surface[20]. The LPCVD area has a lower flow-rate — 25 linear feet/min — and is rated Class 1000. The photolithographic area, which is rated as Class 10, has its own temperature (70°±2°F) and humidity 37.5±2.5%RH) control and has an air-flow rate of 100 linear feet/min. This flow rate exceeds the ~85 linear-feet/min flow rate threshold for laminar flow, i.e., air flow moving with uniform velocity following essentially parallel flow lines with an absence of eddies. With this type of processing environment, wafer defects caused by dust should be negligible even for large area circuits with feature sizes as small as 1μm.

Conclusions

A number of the new technology areas that are presently being explored at SSTC for use in fabricating the next generation of high density CMOS integrated circuits have been described. The challenge of VLSI CMOS ICs is a formidable one, but formable tools and a continuous series of process innovations are available to meet this challenge.

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R.A. Geshner

As chip size gets larger and more complex and line-size gets smaller and more sensitive to lithographic defects, the design engineers and manufacturing process engineers need to know.....

What electron-beams can do for LSI

Abstract: *The manufacturing electron-beam exposure system is a microlithography photomask-making system that can delineate, for today's LSI masks, extremely fine lines in complex geometrical configurations on electron-sensitive resist polymer. The author also reviews a constellation of related technologies.*

LSI designer problems

In 1950, a digital gate cost $10, was made with vacuum tubes and covered 2500mm^2. Today, a digital gate costs 1 cent and is contained within only .001mm^2. Today's design engineer must cope with ever-increasing design complexity on semiconductor chips that are becoming larger.

Devices (basic functional cells) and their line sizes are becoming smaller. Design density will continue increasing at the rate of 60 percent each year. With just this increase in complexity, the design engineer would be "pulling out his hair" if he didn't have a complete computer-aided design (CAD) system that allows computerized preparation of his design information with almost immediate translation to hard mask tools.

As an example, with smaller line sizes, the tolerance on transistor source-to-drain spacing gets smaller. This means line-size tolerances must get smaller to allow these devices to realize required performance gain and to stay within operating parameter specifications. Additionally, as the chip size gets larger there are fewer chips on the wafer, which means registration of each process mask step is more critical. These factors and defect density factors introduced during wafer processing take their toll in yield, raising the price of the semiconductor device. We need a lithography system that will keep the yield high, and also economically will make larger, more densely packaged circuits.

Typically, the design engineers must also prove out their design through an actual sample design-verification production run. They must produce a complete mask set and make wafers. In today's dynamic semiconductor industry, these design-verification runs have to be completed in record time. The design must be proven quickly to get the product into large-scale production and on the market if we are to realize an effective return on investment. It must be possible to modify the design and get masks quickly. The refined design must be documented and cast in concrete for production runs. Correct designs must be immediately reproducible from day to day to maintain production. The computer-aided-design, 1X mask production system developed around the manufacturing electron-beam exposure system (MEBES) helps the designer to accomplish these functions. Conventional masks are thin pieces of clear glass with an even thinner coating of opaque chromium in which the desired circuit configuration is delineated for a particular step in the semiconductor manufacturing process. The resolution of the delineated device structures can be no better than the quality of the mask used. In the past, masks were made only by optical microphotographic techniques. Some fundamental limitations in optics can limit our optically making masks for the larger, more complex IC designs. That is why we are in the electron-beam (E-beam) process business today.

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New tools in microlithography

Electron-beam technology for photomask generation has become a viable state-of-the-art in the last ten years. Several other technologies made this possible including CAD and other electro-mechanical-optical-chemical techniques such as laser interferometry, cryogenic-ion-pump vacuum systems, scanning electron-beam microscopes (SEMs), air bearings, servo-pneumatic vibration-isolation mounting, servo-motor control, microprocessors and computers, new polymer resist systems and a lot of ingenuity. We can use this equipment now to shoot a finely focused beam of energized electrons onto an electron-sensitive resist polymer. This beam will delineate extremely fine lines in complex geometrical configurations for making high-density, high-complexity large scale integration (LSI) semiconductor devices. RCA has been using a system approach to LSI mask fabrication for about two years.

Electron-beam technology is a complete system approach because it involves: the design engineer who specifies the design data; the CAD procedures and the design captured as a computer-readable representation; the actual lithographic techniques using the E-beam; and the process engineer who uses these new techniques to increase yield.

The main advantages of RCA's E-beam technology are that it can make: masks up to 5-inch x 5-inch over a 4.1-inch drawn field; line sizes down to 0.5 μm ± 0.1 μm; masks with defect densities of <1 defect/inch^2; complete mask sets from CAD tape to first contact prints in less than three days in more than 50 percent of the cases; and the most complex masks on any chip size up to 4-inch x 4-inch. An outline of some of the pertinent E-beam machine specifications is shown in Table I. A picture of SSTC's MEBES equipment is shown in Fig. 1. The specific advantages and disadvantages of E-beam lithography have been reviewed previously in an *RCA Engineer* article (Vol. 24, No. 3, Oct./Nov. 1978).

Table I. Typical E-beam machine specifications.

Drawing area	4.1 in. x 4.1 in. (5-in. x 5-in. plates)
Table speed	4 cm/s (≈94 in./min)
Interferometer correction resolution	1/32 μm (≈1.2 μin.)
Raster scan	256 μm (≈10 mils)
Maximum chip size	16 mm (≈0.63 in.) x 32mm (≈1.3 in.) without special partitioning
Pattern input type	Trapezoids
Raster butting error	±1/8 μm (≈5 μin.)
Writing address modes	2 (0.5-μm and 0.25-μm address)
Pattern resolution in 6000-Å positive resist	1 μm consistently, 0.25 μm with thinner resist using smallest address
Line-size control	±0.10 μm
Line definition	±1/8 μm (0.5-μm address)

Manufacturing problems

As designs become more complex and more dense, design rules (the size of the lines and spaces allowed in the design) will become smaller. RCA is actively working with 5 μm design rules now and is actively moving toward 3 μm rules. A 1 μm factory design is technically possible in the future. The use of 1 μm design rules in the 1980s will have a greater impact on semiconductor technology than any other single factor in the last 20 years. Although MEBES can effectively draw 1 μm lines from a system standpoint, other problems should be considered.

Let's look at some of the problems that 1 μm lines and spaces in LSIs could cause in the immediate future.

- *Defects* occur in 1X masks and on the wafer. Masks are manufactured and qualified by automatic 100-percent inspection with a 2 μm lower-limit defect-detection system (Fig. 2). If we get to 1 μm lines, on 1X masks, then in all probability at least 0.5 μm defects must be detected. This may be possible but is probably impractical because 0.5 μm detection would be very time-consuming.
- *Accuracy* in masks, registration, and printing on the wafer must be held to $<\pm 0.25$ μm. Today the tolerances on "runout" or variation across the mask are $>\pm 0.5$ μm. The wafers vary more than ±0.25 μm during fabrication due to stresses in the wafer caused by uneven topography and high-temperature process steps.
- *Metrology problems*. If dimensional tolerances must be held to ±0.25 μm, then the measurement techniques must be repeatable to at least ±0.025 μm (±1 μ inch).
- *Mask defect repair* could be a problem.

Fig. 1. MEBES mask and reticle drawing facility in a specially controlled clean room environment. The actual drawing equipment is shown on right and the computer console control is shown on left.

Fig. 2. KLA-100 automatic 100 percent mask inspection machine. This machine has a defect detection capability down to 2 μm and produces a hard copy map of all defects detected. It is tied directly to a laser chrome defect removal machine (see Fig. 3) and common software and data is shared between equipment.

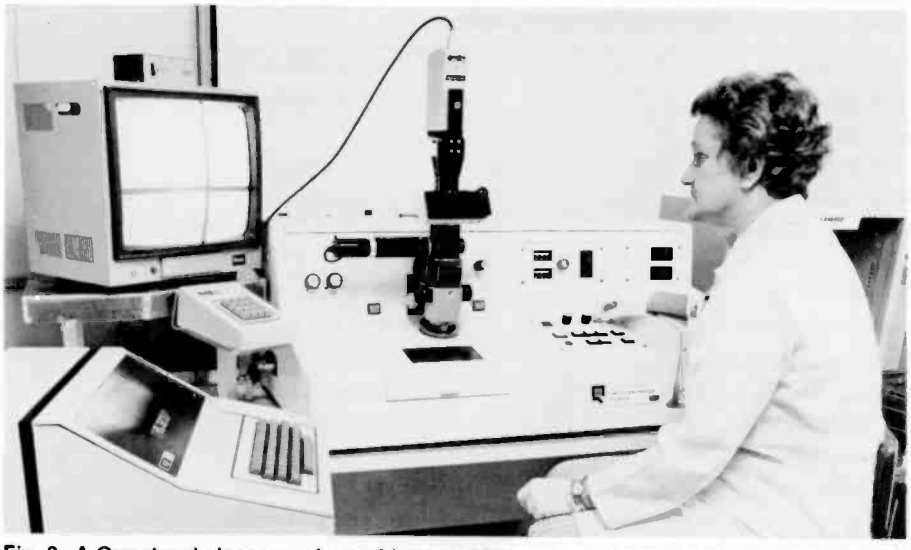

Fig. 3. A Quantronix laser repair machine used to remove extraneous chrome spot defects on a completed mask. This allows preparation of masks with, in some cases, zero defects/inch².

Today's practice is to use a laser to remove excessive chrome spots and thereby salvage masks with too high a defect density (Fig. 3). The 1 μm lines will require removal of 0.25 μm defects. These defects will be difficult to detect and may be even more difficult to remove when in close proximity to a critical device in a 1 μm space.

- *The problem of testing* a chip as complex as a complete computer seems overwhelming.

Yield (the number of good die per wafer) is the bottom line. We have listed a very few obvious manufacturing problems that could affect yield. We need the best systems approach possible to obtain the best yield possible.

Electron beam systems approach

RCA has a complete systems approach for solving the mask lithography dilemma. The systems approach can handle the design complexity problem for today's 3-to-5 μm design rules and can be used for the 1 μm design rules in the future. We solve today's problems with this systems approach by using 1X contact and 1X projection masks. The MEBES 10X reticle generation and direct-step-on-wafer (DSW) projection equipment can handle future requirements. The keystone of the system is the electron-beam equipment. This system encompasses computer design, magnetic tape transfer, archival storage, electron-beam mask writing, 100 percent automatic mask inspection and verification. We can adapt the system to all wafer lithography including contact printing, soft or proximity printing, projection printing and direct-step-on-wafer printing. The designer can use CAD to relieve his design complexity problem. The electron-beam gives him the line resolution and the quick turnaround (QTA) he requires, and gives the process engineer the tool-dimensional and defect-density tolerances he requires. This should allow RCA to get the best yield possible.

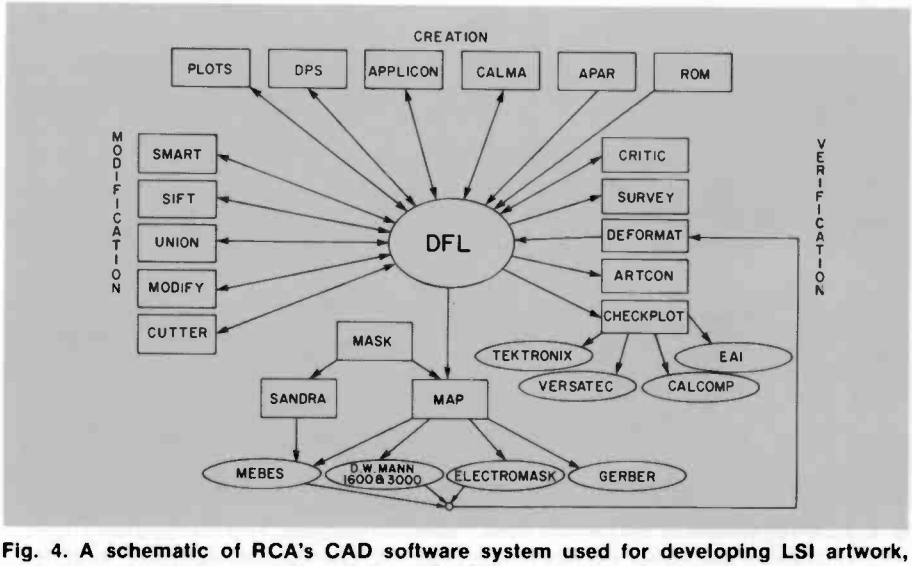

Fig. 4. A schematic of RCA's CAD software system used for developing LSI artwork, analyzing artwork design rule variation, checking artwork and preparing magnetic tape inputs to various pattern drawing equipment including MEBES.

Computer-aided design (CAD)

Figure 4 shows RCA's mask artwork system developed and assembled by a dedicated design automation (DA) group in Somerville, New Jersey. The heart of the system is a common artwork-specification design-file language (DFL). Designs can be created, modified and verified through a number of software programs. The initial design can be created by manual, interactive graphics, or by automated layout techniques as outlined on the top line of the schematic (Fig. 4). Similarly, modifications and verification of graphic designs can be accomplished by programs shown on either side of the diagram. For example, a design may be verified by CRITIC, the design-rule checking program. It is "batched" by the mask artwork program (MAP) for preparation of a magnetic tape that can drive various types of mask-generation equipment. One of these pieces of equipment is MEBES.

In the past, the designer would come to the "little-old-mask-maker" with a drawing of his design. The mask-maker would prepare artwork, make first-stage camera reductions for 10X reticles and make multiple-image masks on a step-and-repeat reduction camera. In "designing" the mask, the mask-maker had to determine things such as tone, orientation, geometry, grid or scribe-line size, test inserts, alignment marks, step-and-repeat size, and so on. All of these problems are now handled automatically by the MASK and SANDRA programs shown in Fig. 4.

All the mask criteria in these programs are called out or specified by the design engineer. The design engineer not only designs his circuit but he also completely designs the 1X mask. Technology files for standard technologies, such as LOVAG, closed-circuit logic (C^2L), linear and

bipolar, aid the design engineer. The technology file permanently delineates the array format for the particular technology and standardizes the mask design to reduce the large number of parameters the design engineer must specify. This file reduces the possibilities for error. A CAD-developed tape given to MEBES has all the array information and pattern information necessary to directly produce, through MEBES, a complete 1X master mask.

Magnetic tape proofing

The tape used to delineate patterns on MEBES can be inserted into "Deformat" (Fig. 4). "Deformat" allows us to checkplot circuit information on a 72-inch Versatec™ plotter (Fig. 5) at almost any scale factor in 8 minutes. We can check the design visually with this drawing (almost equivalent to a "blow-up" of an optical 10X reticle) or compare the checkplot on the drawing with the 1X mask using a microscope. This system will effectively troubleshoot designs, but will it make useful parts? Only a design verification part-fabrication run will assure this and prove the design.

MEBES

We have already reviewed MEBES machine specifications (Table I). These specifications are realistic, and reproducible from mask to mask with reasonable mask yield. In addition, we run a vigorous quality control verification procedure on every MEBES master and carefully maintain precise control over all mask processes.

Quick turnaround (QTA)

One MEBES 1X master can be written every hour. Actual run time on equipment for a fairly complete 1X design is only about 30 minutes. A special "Hi-Speed Corfil" programming method has improved MEBES writing time for more complex designs. Tests show that, with this technique for very dense complicated designs, the relative write time can be improved five times. Here is another example. Engineers made a mask set for an experimental RCA-designed 16K static RAM. This circuit had ~100K transistors. Using conventional, optical, pattern-generator 10X-reticle generation techniques for a 10X reticle for older, optical 1X mask-generation it was estimated that reticles could take up to 76 hours per layer. Optically generating these reticles was impractical since production time just to get to the 10X reticles was exorbitant. MEBES drew the 1X masters much more quickly, averaging 38 minutes a level.

Direct step-on-wafer (DSW)

RCA recently invested heavily in 10X projection aligners where 10X reticles are used directly in a wafer aligner rather than 1X masks. These new projection systems can resolve 1 μm lines and spaces. Therefore, 1 μm design rules are still possible.

MEBES can write 2X-to-10X reticles since it will write at any scale. Design automation has provided special reticle software. The reticles can be written in the same short intervals it takes to write a 1X multiple pattern. This makes it an extremely efficient reticle pattern-generator. On the new direct-step-on-wafer (DSW) projection systems just becoming available, we can "step" a full field of chips or as many as can be drawn in the 4-inch x 4-inch drawing field of MEBES — a 2-inch x 2-inch array of .200-inch chips (Fig. 9). For this application, MEBES is the only practical way to make reticles.

The "10X reticle system" approach alleviates some problems brought up in our discussion of 1 μm design rules. That is, the reticle defect size can now be 5 μm and current 2 μm detection limits are effective. The DSW machine is now responsible for and holds tight tolerances between mask sets. In addition, defects on 10X reticles are repaired more easily because a 1 μm line on a 10X reticle is now 10 μm.

Fig. 5. A 72-inch Versatec Plotter that allows preparation of paper drawings of information on magnetic tape at almost any scale factor in about 8 minutes. This machine is used to checkplot a MEBES tape input before a MEBES is drawn.

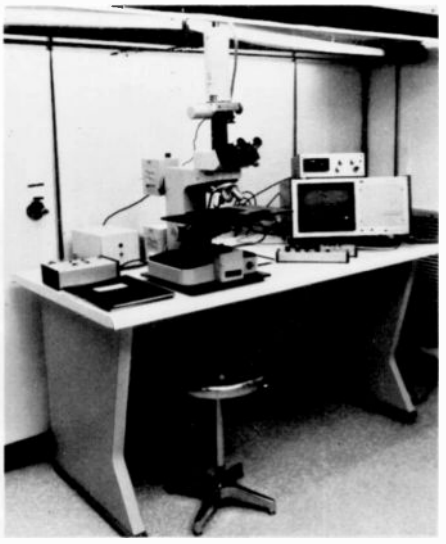

Fig. 6. An ultra precision ITP, digital, microdensitometer line edge sensing machine used to measure critical dimensions down to 1½ μm to an accuracy of ± 2 μinches.

Other innovations

Metrology

As line sizes get smaller, measurement accuracy and resolution become more critical. We have already explained why critical dimensions less than 1 μm on a mask or wafer are difficult to measure. The new lithography system approach also accounts for this problem. RCA has several of the most up-to-date cross-correlated scanning electronic-microscope systems available (ITP™—Fig. 6). Each machine in this system costs upwards of $75K. The system is heat-sensitive and must constantly undergo a rigorous calibration procedure.

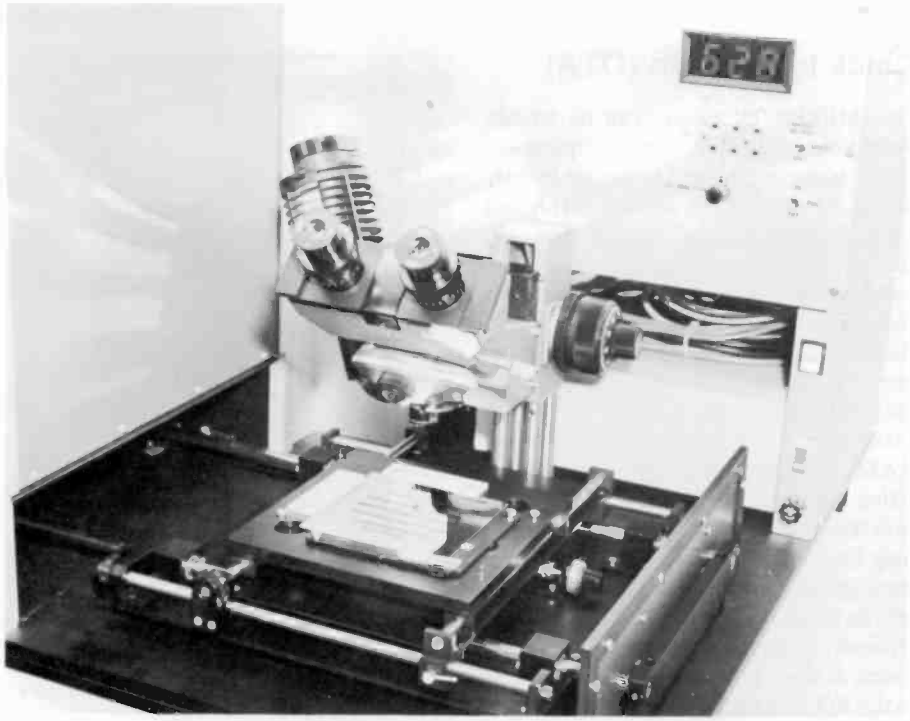

Fig. 7. RCA's diffraction grating laser line measurement equipment developed by RCA's Zurich Research Facility capable of measuring line width down to .6 μm to an accuracy of $<\pm$5 percent.

We have succeeded with new measurement techniques using diffraction gratings. The new diffraction-grating line-width tester (Fig. 7) is a highly precise and stable electro-optical apparatus developed by RCA's Laboratories in Zurich, Switzerland. This system will measure a target grating in an LSI design (line sizes as small as 0.6 μm) to an accuracy of $<\pm$five percent in only 17 seconds. This technique can be used on the mask and on the wafer for process optimization. The new technique depends on a He-Ne laser and automatic microprocessors to measure line-width accurately.

Glass inspection

We use various glass substrates for various mask applications, depending on the process to be used in wafer fabrication. The proper glass must be used for each process — the glasses have different coefficients of thermal expansion and pass different wavelengths of light. In the past, quality control people used an oil immersion objective lens to measure the refractive index of the glass before shipping it to the factory, to be sure it was right. Oil made this time-consuming and dirty. The RCA Zurich Laboratories came up with another way to sort the glass. A 254-nm light source will make various glass materials fluoresce with colors that depend on the type of glass. We can, therefore, sort the glass before we use it in MEBES and save time and defective runs because of "wrong glass." RCA has shared this technique with the glass industry.

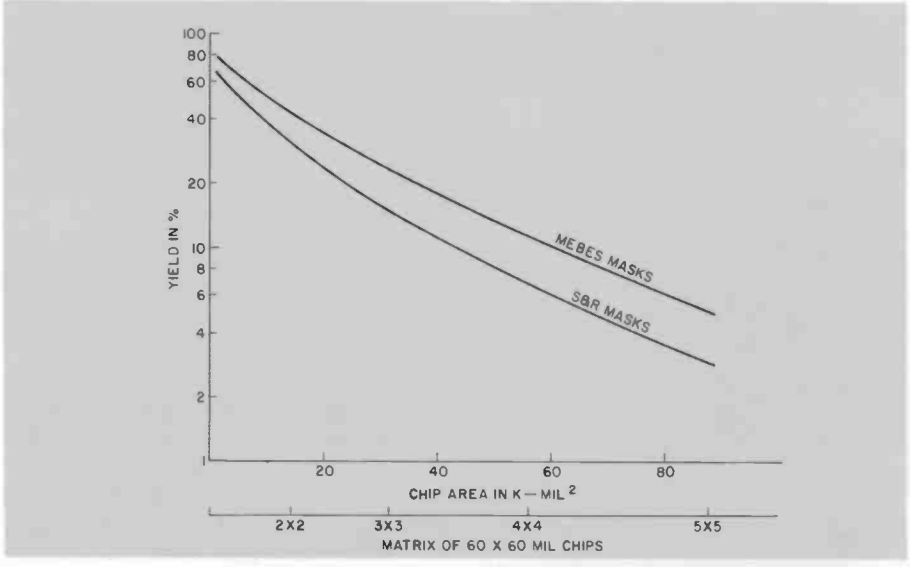

Fig. 8. This is a chart showing the relative yield of MEBES masks vs. conventional optical masks. A statistical matrix approach was used to establish this data. The chart shows yield differential vs. chip size. Chip size was varied by determining yield based on varying matrix sizes of .060-inch chips. The entire position of the pair of curves (i.e., relative yield of good chips) could change dependent on the quality of the process used to make the chips, however, the relationship of MEBES masks vs. optical masks would stay the same.

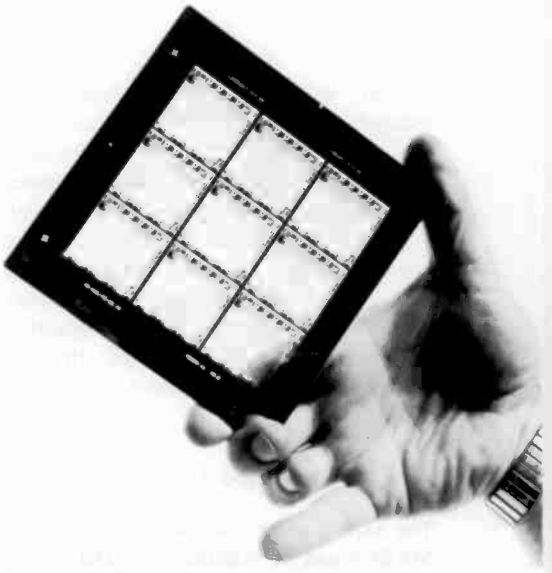

Fig. 9. A 5-inch by 5-inch-10X reticle made on MEBES in $\approx$40 minutes. Preparation of a similar multi-image 10X reticle for new direct step-on-wafer machines is not practical to fabricate by any other available technique other than MEBES.

Yield improvement studies

J.J. Fabula's group compared statistical yield on wafers using the same mask patterns made by both optical methods and E-beam methods. All masks were 100-percent inspected to assure they had equivalent defect densities. In fact, the optical masks really tested a little better than the MEBES masks. The group followed rigorous control procedures in processing wafers. They used a mix of optical and E-beam mask sets within each batch of wafers run so that processing could be eliminated from mask-yield data. In addition, they explored the effects of complexity and size of the chip design by breaking the experiment into various chip sizes.

The chip design had fairly loose design rules (1976 RCA design rules). The results of this extensive test show:

1. The MEBES mask sets gave a higher yield on wafers.
2. High yield with MEBES was even more evident on the larger chip sizes, with a 50-percent to 80-percent increase in chip yield on MEBES masks (Fig. 8).

Since KLA™ automatic inspection showed the defect density on optical masks to be marginally better than MEBES masks, this increase in yield on wafers can only be attributable to the improved chip-location and line-size accuracies in the MEBES mask set.

Other potentials

1. MEBES also can draw a number of different chip designs on the same master, thus allowing a design engineer to check out a number of designs on the same experimental design run.
2. MEBES has universal scaling and line biasing so that the engineer automatically designs at different scale factors on a separate mask set. He can test how his design could work with tighter design rules, without regenerating new DFL computer runs.

Bob Geshner is Manager of the Advanced Mask Technology activity in the Photomask Technology and Operations department at SSTC. He has been working in microlithography for most of the 20 years he has been with RCA. During his first years in Camden, he worked on microelectric packaging and printed-wiring standardization. Later, he developed the first automated large-scale artwork system using a Gerber numerically controlled printed-wiring artwork plotter. When his Microimage Technology group was moved to Somerville in 1973, he became the Engineering Leader of the Solid State Technology Center's quick-turnaround photomask facility. He was responsible for the development of the new MEBES facility. In 1978 he was appointed to his present position.

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Ultimately, the designer can put more chips on the wafer to increase yield provided his design can be adapted to the tighter design rules.

Conclusions

The design engineer and the process engineer now have a useful system, MEBES, for coping with the complexities of current and future LSI designs. We can hope for even more advantages. We must be alert to new technology in lithography to stay cost-competitive. In the future, new wafer technology in 1X projection printing and 10X direct step-on-wafer printing will require us to use a completely integrated lithographic system with higher resolution, quicker turnaround, lower defect densities and greater precision. Electron-beam lithography fits into this future, and gives RCA the necessary competitive tools.

W.A. Bosenberg

The Road to LSI: A Photographic Journey

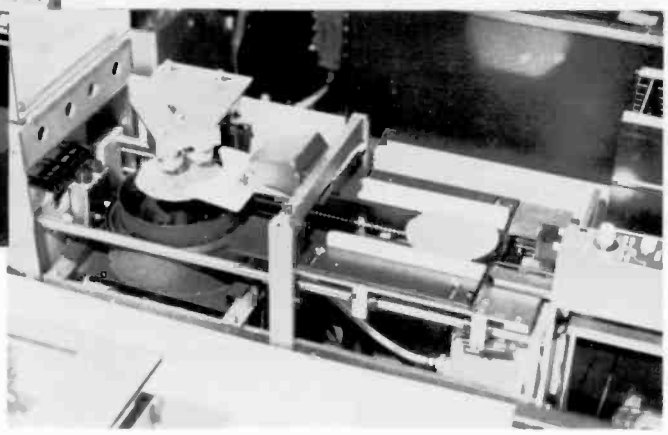
The long road from discrete components to LSI functions started with the invention of the transistor in 1948, passed through the development of the silicon planar technology in the late 1950s and broke into the open with the integrated circuit technology of the late 1970s. Since then, it has been an open road to the present sophisticated LSI technology.

Technological innovations achieved along the path to LSI have cleared a firm roadway now used to arrive at today's complex LSI product. The photographs and captions on these pages trace the essential steps in the current process as it is carried out at RCA's Solid State Technology Center.

1. *As integrated circuits become denser and more complex, so do the blown-up checkplots run on the computers. The various mask levels are superimposed and have various cross-hatchings. Layout errors are marked on the plot and corrected in the artwork file.*

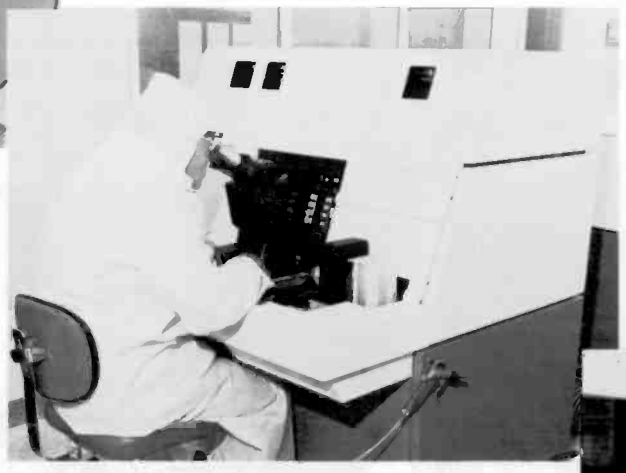
2. *Mask generation depends on electron-beam precision exposure. The location of the beam is monitored by an interferometer to 1/32 of a micrometer. For better accuracy, chromium on glass masks is preferred to emulsion on glass masks.*

3. *Patterning precision is achieved by photoengraving. The silicon wafer is coated with an ultraviolet-sensitive photoresist. This process is highly automated.*



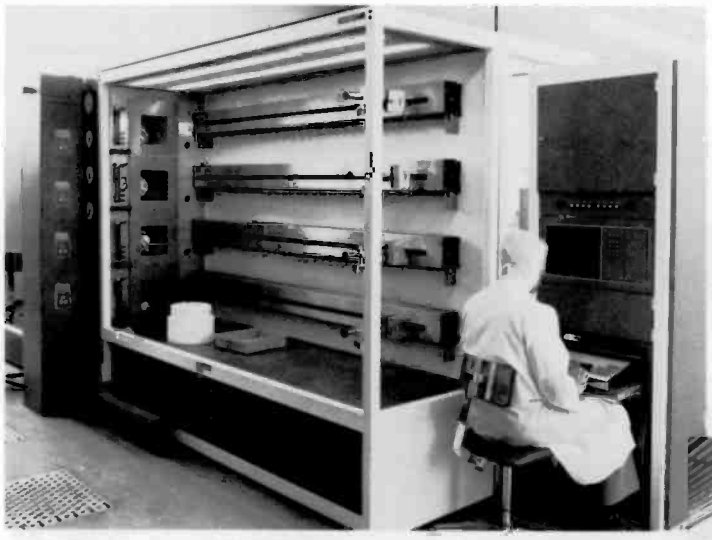
4. *The wafers are moved one at a time through ovens, then spin-coated. Next, the wafer is exposed under a precision aligner and developed, all in the same piece of equipment.*

5. *Alignment must be done under a microscope. The Suss aligner from West Germany allows wafers to be fed from one cartridge into another. The alignment and exposure can be done either in contact with the wafer or at a distance of about 20 μm.*

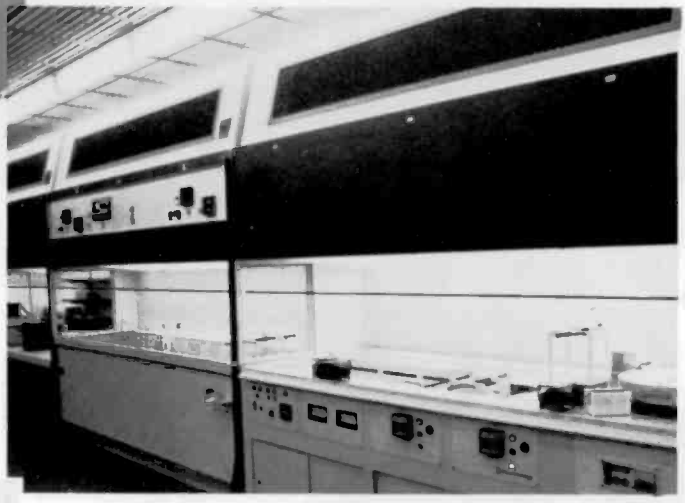


6. *Mask defects will print on wafers. If a perfect mask never touches the wafers, better yields can be expected. This Perkin-Elmer aligner uses scanning-projection mirror optics that allow deep-ultraviolet exposures for better resolution.*

7. *Even finer lines can be printed on this Electromask step-and-repeat aligner. A field of 3/8 inches by 3/8 inches contains four-to-nine LSI chips. Forty to a hundred fields are used per wafer. The positional accuracy is achieved by an air-bearing table and an interferometer. Linewidths down to 1.25 μm can be printed.*

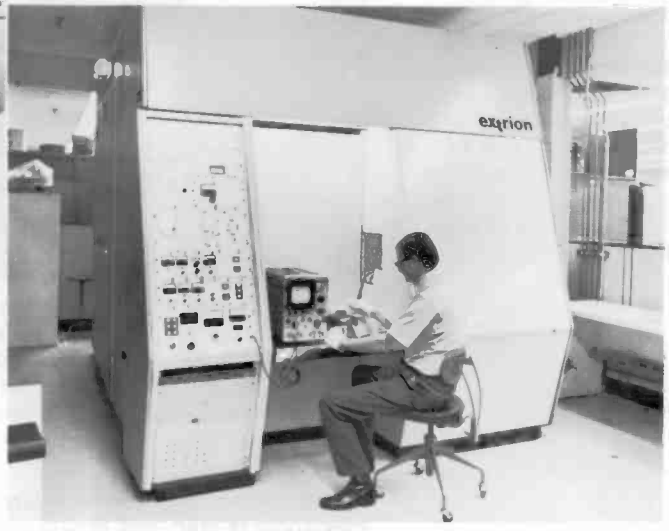


8. *Diffusion is a 1100° C heat treatment that distributes semiconductor donors and acceptors for making p-n junctions. Since it is more economical to use large-diameter silicon wafers, diffusion furnaces have become very large. This computer-controlled four-stack furnace not only allows exact gas-flow control and precise insertion and withdrawal of wafers, it also uses a computer to control temperature.*

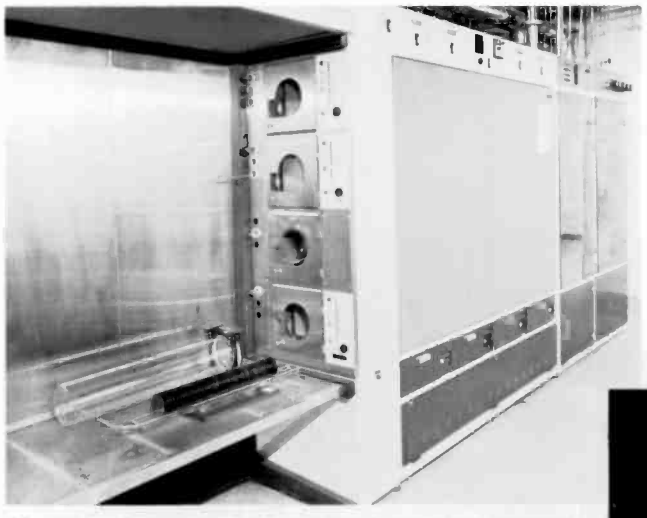


9. *Chemical hoods are made of corrosion-resistant plastics. They have laminar flow bonnets over the perforated work surface. Wet chemicals require close temperature control for consistent etch rates.*

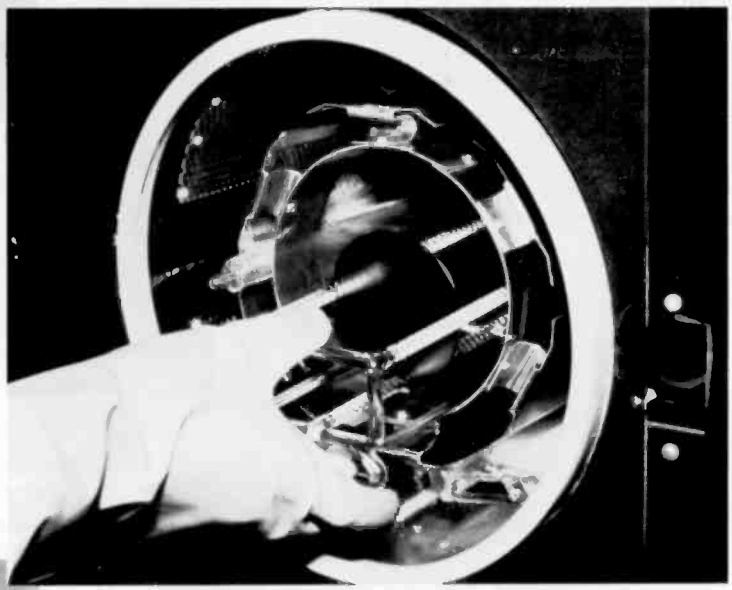
10. *This FSI spray-etch station looks like a washing machine. It allows 150 four-inch wafers to be cleaned, etched, rinsed and dried in one operation. Again, a computer terminal controls the operation and prevents incompatible chemicals from being sprayed together.*



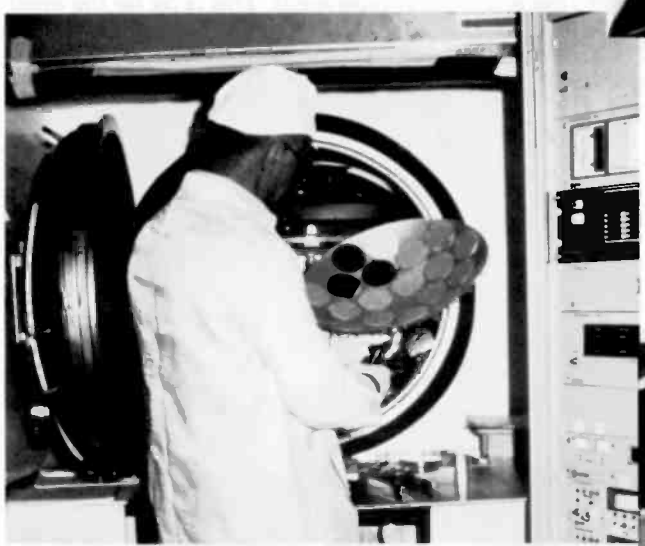
11. *Ion implantation precisely controls doping levels. Arsenic, boron and phosphorus are the most commonly implanted species. The depth of the implant depends on the acceleration voltage. The concentration can be measured as accurately as an electrical current.*



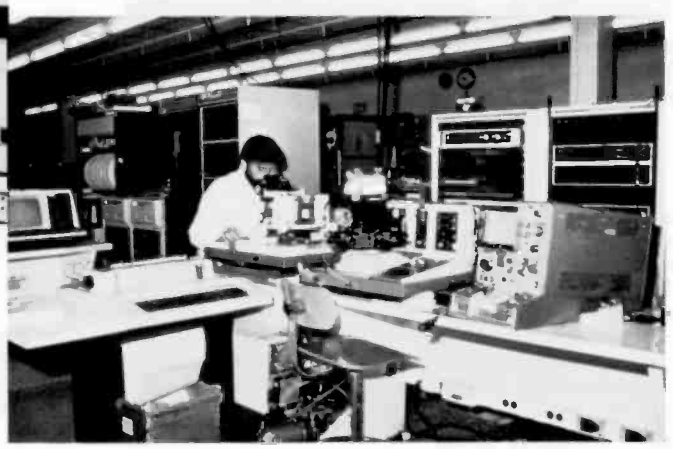
12. *Chemical-vapor deposition is used to deposit polysilicon, silicon dioxide, silicon nitride and phosphorsilicate glasses. By reducing the pressure, 100 or more wafers can be treated in one cycle. The uniformity of such low-pressure chemical-vapor deposition (LPCVD) systems is much better than that of atmospheric systems. Again, micro-processors control the process.*



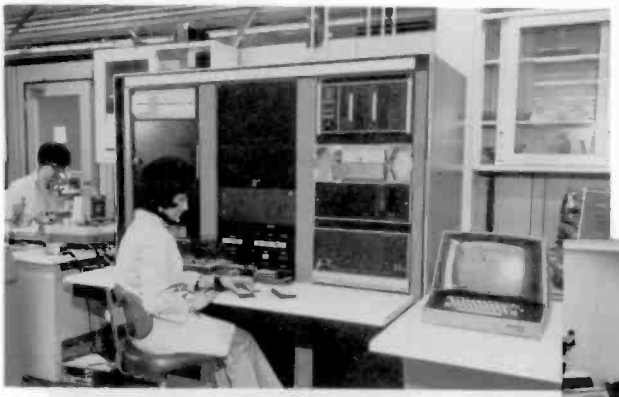
13. *Dry (plasma) etching has become more and more popular. It eliminates some of the wet chemical disposal problems. Fine geometries require the vertical walls achievable in reactive-ion etching (RIE) systems.*



14. *Most integrated circuits are limited in their density by how fine a metal line can be defined. This line must be continuous even over steps. No two lines can be shorted by a defect. This Varian S-Gun® system allows the precise deposition of silicon-aluminum alloys for integrated-circuit fabrication.*



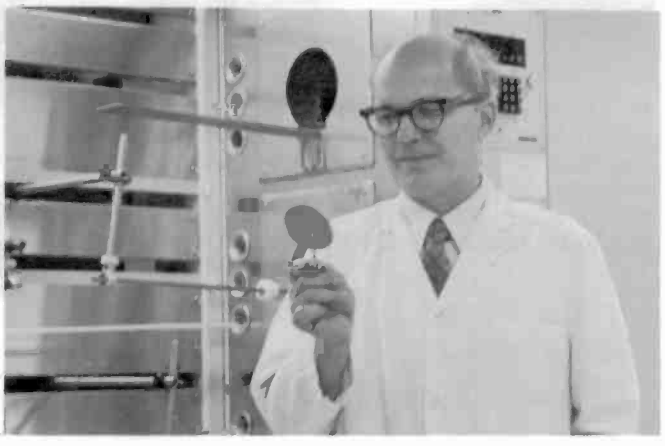
15. *DC-parameter testing is the first important test after the fabrication procedure is finished. NMOS and PMOS transistor parameters are measured. They must be closely controlled if an integrated circuit is to function.*



16. *The wafers are tested functionally on this Datatron tester. The test sequence must include all possible combinations. For VLSI circuits, such as memories, the total testing time would be prohibitive. To solve this problem, intelligent test sequences have been developed in computer software.*

17. *Dicing the wafer and mounting the pellets onto headers is done next. Then wires are bonded between the integrated circuit chip and the package leads. This is by far the most labor-sensitive area of integrated circuit fabrication. For SSTC integrated circuits, visual inspection procedures are rigorous.*

18. *Then the integrated circuits are encapsulated — usually in plastic. Random samples are pulled for life testing.*



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Computer-aided wafer processing

Complex solid-state products will require ultra-precise, closed-loop manufacturing facilities guided by computers reacting to direct-measuring product sensors.

Abstract: *The process-hardware portion of an SSD program focusing computer technology on wafer manufacturing is discussed relative to its development and current status.*

During the early seventies the Solid State Division (SSD) initiated an energetic program to apply computer technology to wafer manufacturing. This consistently followed SSD objectives to competitively manufacture devices by current wafer technologies and to reduce costs and improve profitability. The ongoing program encompasses product management, mask making, the broad spectrum of wafer processing and in-process as well as final testing. Command, supervisory and, eventually, closed-loop computer-aided hardware are being developed and applied. At the time, the program called for recognizable short-term improvements, minimized manufacturing disruption and maximized long-term benefits. As anticipated by the more computer-oriented supporters of the program, initial benefits far surpassed expectations (Table I). Quantification of the results, although extremely difficult because of the dynamics of wafer manufacturing, is currently progressing.

Our comments concentrate on the process-hardware portion of the computerization program. The highly critical computer hardware and software portions

Table I. Computer benefits summary.

	Cost reduction	*Improved yield*	*Quality & reliability*	*Consistent product*	*Improved customer response*	*Increased thruput*	*Flexibility*
Labor (Eng.-DL-IDL)*	X						
Operator skill (reduced)	X	X		X		X	
Operator error (lockout)	X	X	X	X		X	
Direct material efficiency	X						
Diagnostic capability	X	X	X				
Decision making	X	X	X	X			X
Process change capability	X	X	X	X			X
Tighter parameter control	X	X	X	X			
Reduced quality checks	X				X	X	X
Accurate process history		X		X	X	X	
Lot control	X				X	X	X
Instant inventory					X	X	X
Best route scheduling	X				X	X	X
Equipment utilization	X				X	X	X
Floor space	X						
Energy conservation	X						
Preventive maintenance	X	X		X		X	

* DL = Direct Labor
IDL = Indirect Labor (Technician, Maintenance)

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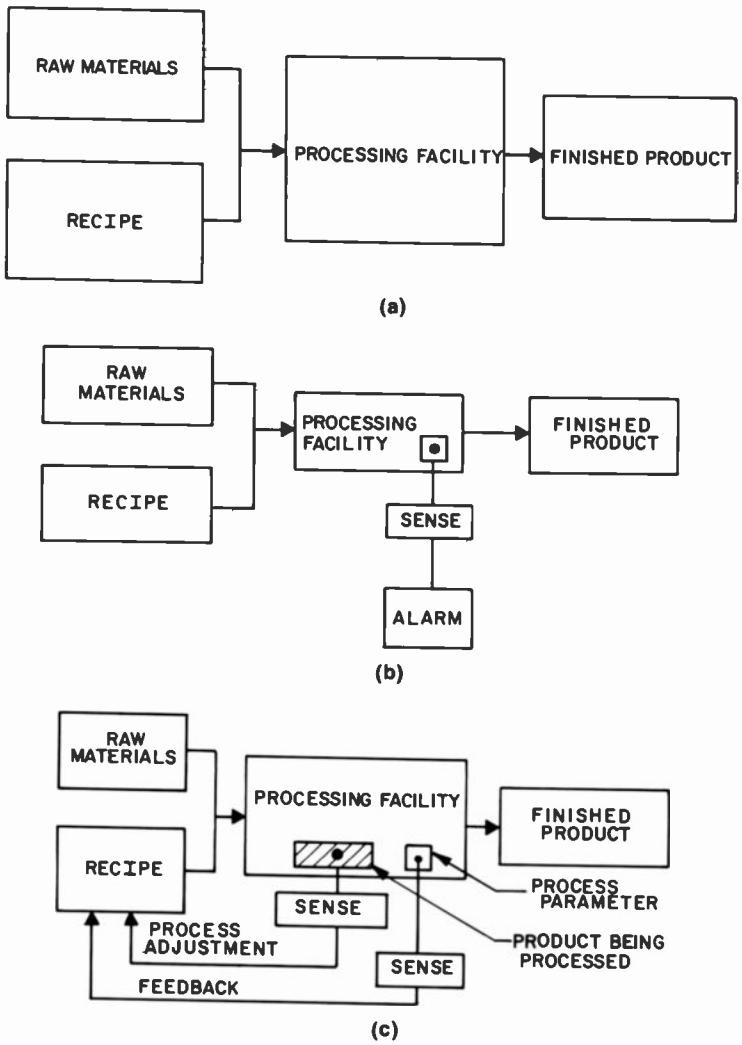

Fig. 1. Functional flow of the elements of the various hardware systems: (a) command, (b) supervisory, (c) closed loop.

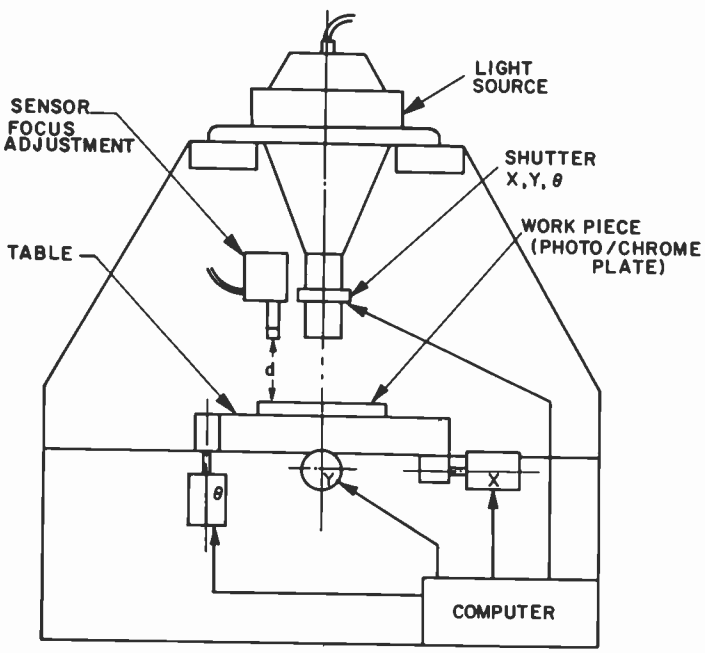

Fig. 2. Mask-pattern generator — command system.

Table II. Control concepts.

	Functions		
Concept	*Instruct*	*Alarm*	*Adjust*
Command	X		
Supervisory	X	X	
Closed loop	X	X	X

continue to be studied by the Solid State Technology Center (SSTC) computer groups.[1]

Table II summarizes the elements of command, supervisory and closed-loop hardware systems, and the block diagrams of Fig. 1 illustrate the functional flow in each of these systems. A close examination of manufacturing conditions, the state-of-the-art and practical constraints led to the conclusion that a combination of the three systems would be essential. Looking to the future, however, SSD concluded that closed-loop systems deserved emphasis.

An initial survey of existing technologies revealed two excellent examples of command and closed-loop systems (Figs. 2 and 3). Each had worked in a manufacturing environment for several years and each was self-contained. The mask pattern generator in Fig. 2, a command system, is turned on and commanded by a computer tape that uses an X, Y and θ system for table motions and an X, Y and θ system for shutter geometry adjustments. The system produces a reticle that, upon inspection, is accepted or rejected. If the reticle is rejected, operators appropriately alter the tape and run it again to produce a reticle for re-inspection. They repeat the process until the system produces an acceptable reticle. Then they file the final tape for future use. Recently, the tape generation system has improved to the point where rerun is rarely necessary.

The crystal puller (Fig. 3), a closed-loop system, is also started by signals from a computer tape, but sensors closely supervise it and continuously feed information back to a computer that consistently alters process parameters to satisfy identified needs. If we have reliable historical data in the computer memory we can accurately compare product performance to the product specifications.

SSD found several quasi-supervisory system examples but none that had the alarm mechanism built into the computer circuitry. Therefore, we could not tell the effects that real-time logging of process interruptions and computer-guided parameter adjustment prior to restart had on wafer yield. We soon had an opportunity to make such a study — the high-speed

bipolar (HSBP) diffusion system (Fig. 4) installed at Somerville during 1975 as the first step in the overall computer-aided manufacturing (CAM) program.

The HSBP diffusion complex, a supervisory system, follows a programmed, machine-readable process card containing basic step-by-step instructions. Audio and visual alarm systems alert the operator to malfunctions and, based on conditions at the time, the equipment continues processing, holds or shuts down. The system logs real-time. This helps the operator diagnose the malfunction and prepare corrective-action instructions needed to save the product.

After months of investigatory effort, detailed planning (including software, hardware, and process-parameter specification), design and layout, our CAM education really began the day we started-up the initial hardware complement. Grounding difficulties and noise problems occurred. Software, hardware and interface malfunctions hampered performance and had to be systematically identified and corrected. Experience with the HSBP diffusion system prompted improvements in the Palm Beach Gardens diffusion system, and both experiences influenced the architecture of the highly effective, low-defect direct digitally controlled (DDC) line at Findlay, Ohio. The Findlay system currently incorporates product management, data logging, process monitoring and control, lockout, equipment loading, equipment diagnostics and total supervision features. Engineers brought-up the unit there over a two-year period and added the supervisory elements when needed.

Results have far exceeded initial expectations. But we've drawn two basic conclusions concerning the hardware: (1) additional progress toward closed-loop operation depends on breakthroughs in the sensors, and (2) some operations may never be totally closed-loop systems because there may never be a practical way to measure certain product characteristics. Table III lists process parameters and product characteristics that require continual control. Some characteristics, such as degree of photoresist polymerization, elude measurement and, consequently, machine-guided process parameter adjustments must be based on resident history. In most cases, we cannot even directly measure temperatures. We must approximate temperatures based on the reaction of pre-calibrated instruments, such as the thermocouple shown in Fig. 5. Film-thickness control is even more

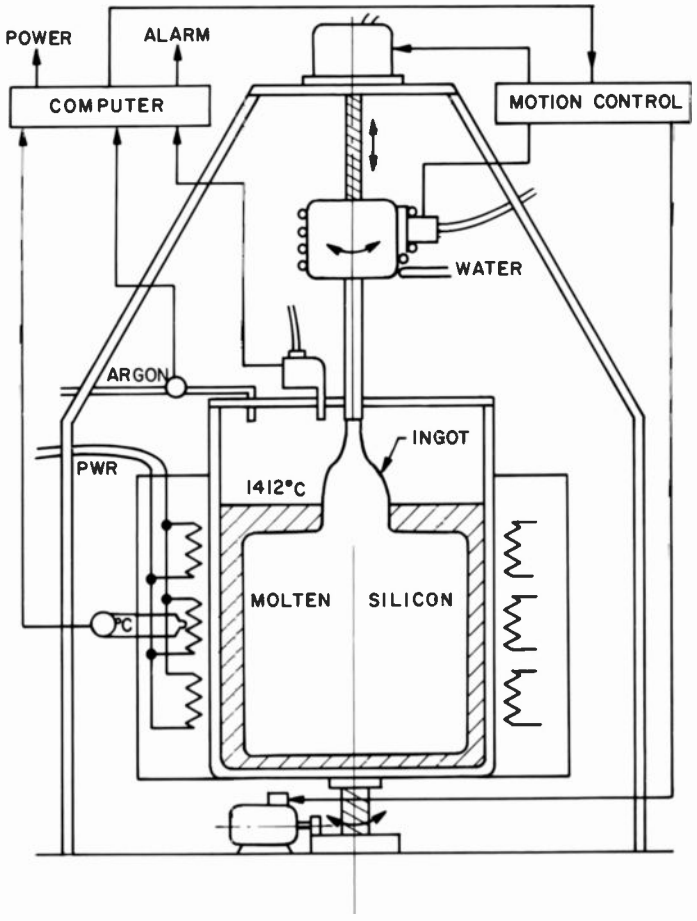

Fig. 3. Crystal puller — closed-loop system.

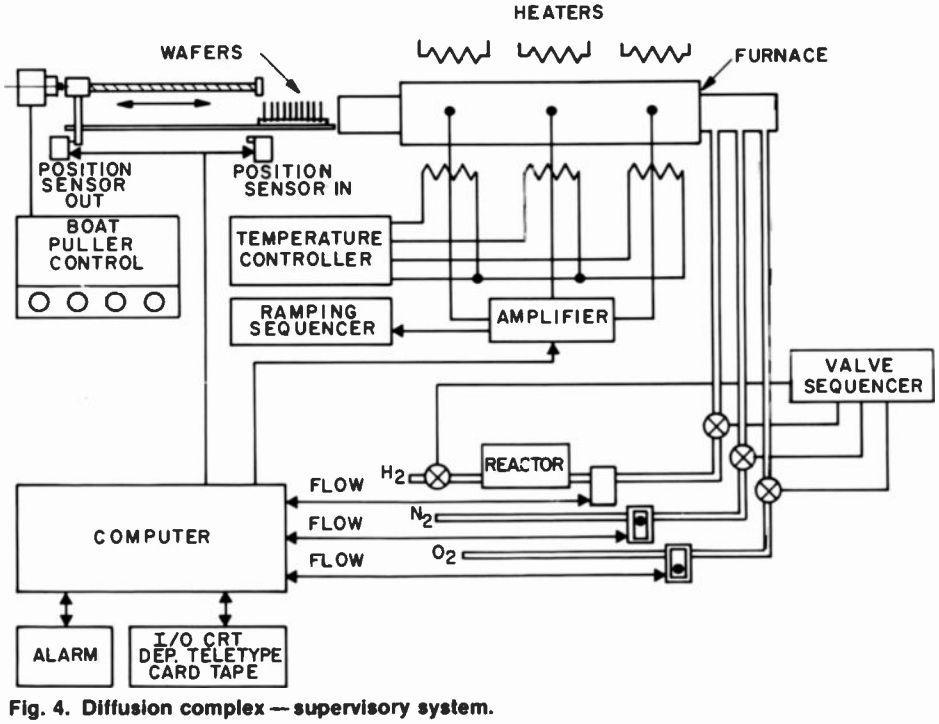

Fig. 4. Diffusion complex — supervisory system.

Table III. Major process parameters and characteristics.

- Temperature
- Pressure
- Time
- Flow rate
- Viscosity
- Composition
- Particle content
- Transparency
- Velocity
- Acceleration
- Distance
- Liquid level
- Resistivity
- Thickness
- Contamination
- Change in any of the above

precarious since it depends upon instruments that measure indirectly and provide, at best, only rough approximations of what is taking place on the surface of the product.

Clearly, the manufacture of more complex solid-state products will require ultra-precise, closed-loop facilities guided by computers reacting to direct-measuring product sensors. Current plans to address the process-control challenge of the 1980s and 1990s include in-house concentration on the sensor, software[1] and computer-hardware areas, as well as careful selection of computer-compatible process hardware for product manufacture.

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SSD Materials and Procurement
J. Watkins, S. Townsend, C. Edwards

Ray McFarlane was Manager, Equipment Technology, for solid-state signal ICs and special products before leaving RCA in August, 1980. During his 24 years with RCA, he was intimately involved in product and process design, as well as manufacturing facility development as related to waveguides, computer components, electron tubes, solid-state energy converters, integrated circuits and power transistors. His solid state experience includes all phases of product and facility development, including photomask generation and silicon growing through assembly, packaging and testing.

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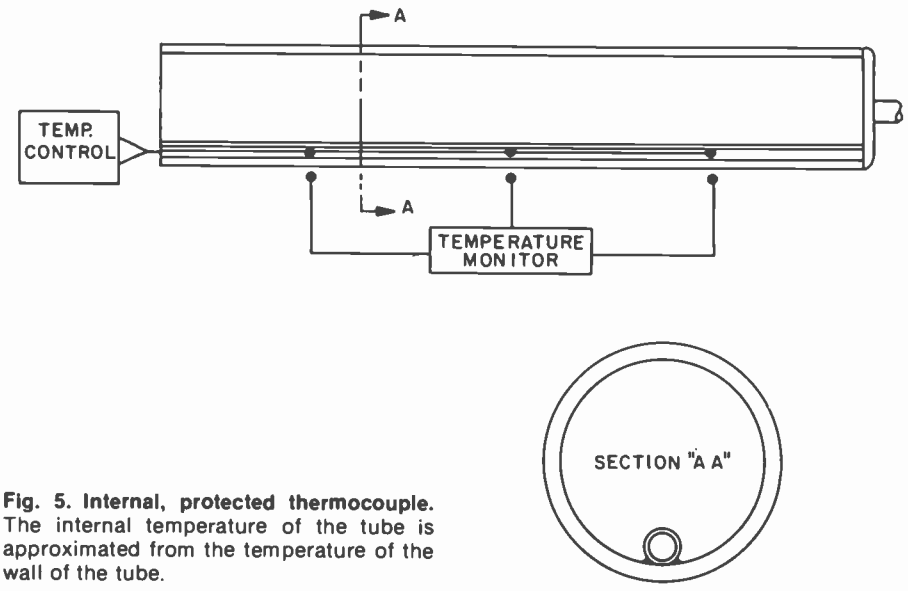

Fig. 5. Internal, protected thermocouple. The internal temperature of the tube is approximated from the temperature of the wall of the tube.

Reference

1. For a greater insight into, and specific detail concerning, the computer software and hardware areas of CAM, the reader is referred to the Process Monitoring and Control (PMC) organization located in the Solid State Technology Center in Somerville, New Jersey, Mr. John Gaylord, Manager. Also see "Process Monitoring and Control — A Computer-Based System for Manufacturing," J. Gaylord, *RCA Engineer*, Vol. 24, No. 6 (April May 1979); and "ERIC: A Process Monitoring and Control System," J. Gaylord, *RCA Engineer*, Vol. 25, No. 4 (Dec. 1979/Jan. 1980).

L.M. Rosenberg

The evolution of design automation toward VLSI

The incremental historical growth of design automation at RCA will continue as VLSI design becomes imminent. We will see improved approaches to logical and physical design to reduce front-end costs, cost-effective design-for-testability approaches, and more.

Abstract: *This paper presents the author's opinion of the major problems confronting design automation (DA) for VLSI and how DA may evolve to meet these challenges. The paper first takes a historical look at the driving forces for DA development by analyzing the evolution of DA at RCA. It looks at some successful and unsuccessful development efforts and attempts to isolate some of the criteria necessary for success. It reviews RCA's current LSI DA abilities and compares them to the challenge of VLSI. The major challenges — layout, design verification and testing — are discussed along with possible achievable solutions.*

Introduction

The challenging question posed by VLSI is: how can we cope with the continuing explosion in complexity of ICs? Although the challenges facing technology development are substantial — lithography, both imaging and registration, etching fine lines, implantation, multilevel fine-line interconnect, and so on — we have no evidence that any fundamental physical barrier will prevent IC complexity from continuing to grow exponentially in time. Device-count per chip may double every two years or so for the next decade or more until design rules of one-quarter to one-half micron are achieved.[1]

Many observers, including myself, believe that the rate-limiting factor constraining the growth of IC product complexity may well be the design automation (DA) tools required for design (system, logic, circuit and process) and its verification, for physical implementation (layout) and its verification, for test generation and its verification (fault coverage) and for test data analysis. These substantially challenge the design automation tool-builders and their users because of the large and growing amount of data involved. For the purposes of this paper, allow me to operationally define VLSI as the IC complexity of the near future, that is, one-to-two orders of magnitude more complex than our design automation systems can comfortably handle today.

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Some history

I start in 1970 — the year of the Seventh Annual Design Automation Conference (DAC) (then called a workshop) — clearly not at the beginning. Extensive work had gone on in areas such as interactive graphics, automatic layout, and circuit and logic simulation. At this time, however, most of the enthusiasm for DA came from the DA tool-builders at large corporate research centers, not from the design community.

I suspect circuit designers *themselves* built the most useful DA tools at custom facilities such as system houses. This is because the low volume and quick turnaround required of custom designs forced designers to find computerized solutions that gave them design leverage. The newly developed techniques such as standard-cell automated layout substantially increased chip size (and hence incremental cost), but were not an issue because low production volumes were required. This penalty justifiably discouraged commercial semiconductor houses — the main focus of this paper — from pursuing automated layout. IC complexity was modest enough (perhaps 100-150 devices) so that layout aids, logic simulation and circuit simulation were not viewed as crucial or even necessary. These tools were considered too inaccurate and expensive to be cost-effective.

The commercial semiconductor house could do — quickly, simply and inexpensively — rubylith cutting for photomask generation. Although work was going on in interactive graphics, what

could one do with the resulting digitized mask-artwork polygons except use computerized ruby-cutters?*

Digitizing these polygonal shapes was tedious and time consuming. Worse, editing these computer representations was either tedious if done on a source-language format, or expensive because interactive graphics systems were extremely costly and only CAD researchers could afford them. The advent of and necessity for the pattern generator really made DA viable for the commercial semiconductor manufacturer. It was the first true DA necessity — because manufacturers needed to cope with MSI complexity from a manufacturing point of view. Let me explain.

What is the limiting practical complexity for the rubylith? If the largest practical ruby sheet is approximately ten feet on a side, if the smallest practical ruby grid-step is close to 0.1 inch, and if the required silicon grid step is 0.1 mil (2.5 micron to support 7-10 micron design rules), then we need a ruby scale factor of 1000X and a maximum chip size of about 100 mil on a side. As MOS complexity pushed past these limits, pattern generation of a 10X reticle became necessary.

But, how were we going to feed the pattern-generator "beast"? How were we to get the artwork into a computer? At RCA Labs an English-like language called PLOTS[2] was developed. Examples of this language are shown in Figs. 1 and 2.

*Photoplotters, making up to 80X foils, were used at various government installations such as RCA's Government Systems Division as far back as 1967 or so. These photoplotters were fed by the DA system which automatically laid out standard cell chips. But I know of no semiconductor house using them at that time.

Although easy to learn and use, especially for regular structures such as memories, it soon outgrew its ability to conveniently support random logic designs when complexity reached the MSI level. DA system-builders had to come up with a low-cost system to capture hand-drawn designs in the computer. We therefore developed a simple, inexpensive interactive graphics system (based on a PDP-8 with 4K memory, a Calcomp digitizer plotter — hence, the name, digitizer plotter system (DPS) — and a hand-held joystick[3] (see Fig. 3). By today's standards, its "interactive" editing abilities were as primitive as its hardware configuration. But mask artwork could now be quickly and accurately captured by a computer. One element of human error was eliminated.

The state-of-the-art DA problem now was to develop pattern-generation software which could translate a general, all-angle polygonal shape into a minimal covering-set of rectangles with the further constraint of minimal overlap at the edges of the polygon. This problem required three generations of production software at RCA before we finally achieved an optimal solution. We did not limit ourselves to orthogonal or 45-degree geometrics (nonacute) because certain technologies, such as bipolar with lateral complementary transistors, require all-angle polygons.

This latter constraint — support of many technologies — has had other effects on our DA strategy at RCA. DA at RCA deals with metal and silicon-gate MOS, CMOS/SOS, "Linear" Bipolar, I^2L, High-Speed Bipolar and various power transistor technologies. Because of this diversity, we have endeavored to keep our software as technology-independent as possible.

Concurrently with this work, the feasibility of a computerized design rule checking (DRC) facility was investigated. Initially, it was too difficult in the general case; there were too many special cases. Additional data from the designers was essential. But as complexity continued to increase, the number of digitized design-rule violations became a major problem. Furthermore, continuing growth was rapidly moving us past that awesome level of integration now called MSI. DRC had to be developed — even if it only solved a subset of the problem — and it was.[4]

DRC was the first truly new capability that storing the artwork in a computer brought us — the pattern generator resulted in the same functional reticle we could get from rubylith. Now the computer could do something truly new: automated design-rule verification. We also discovered we could do more verification with the data at hand than we originally guessed.

At this point, it was dramatically clear that DA possibilities were unlimited. Researchers quickly conceived techniques such as connectivity verification, device extraction from the artwork layout, automated artwork geometry modification and a common data base linking all these to circuit and logic simulation. Allow me to focus on this.

Common data base

Many of us at this point clearly saw that computer-aided design and verification

PLOTS POLYGON EXAMPLE

```
M5
   P  X20Y20 TO X100Y20 TO X100Y100 TO X80Y100 TO ...
OR P  X20Y20 TO X100    TO     Y100 TO X80     TO ...
OR P  X20Y20    R80             U80     L20        ...
```

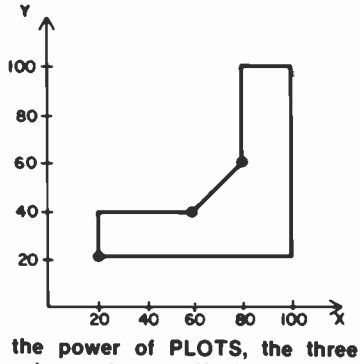

Fig. 1. Because of the power of PLOTS, the three different statements shown can be used to specify this polygon on mask-level 5. The first explicitly gives all vertices; the second eliminates the specification of duplicate coordinates and the third gives relative movements.

PLOTS CENTERLINE EXAMPLE

```
M 7
W 10
L X20Y20  R40(R20U60) R20   AND R100
```

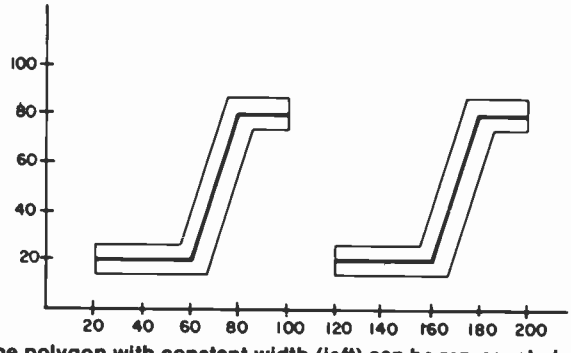

Fig. 2. The polygon with constant width (left) can be represented, using PLOTS, simply by giving the coordinates of its "centerline" and its width. The polygon 100 units to the right was specified simply by appending the phrase "AND 100."

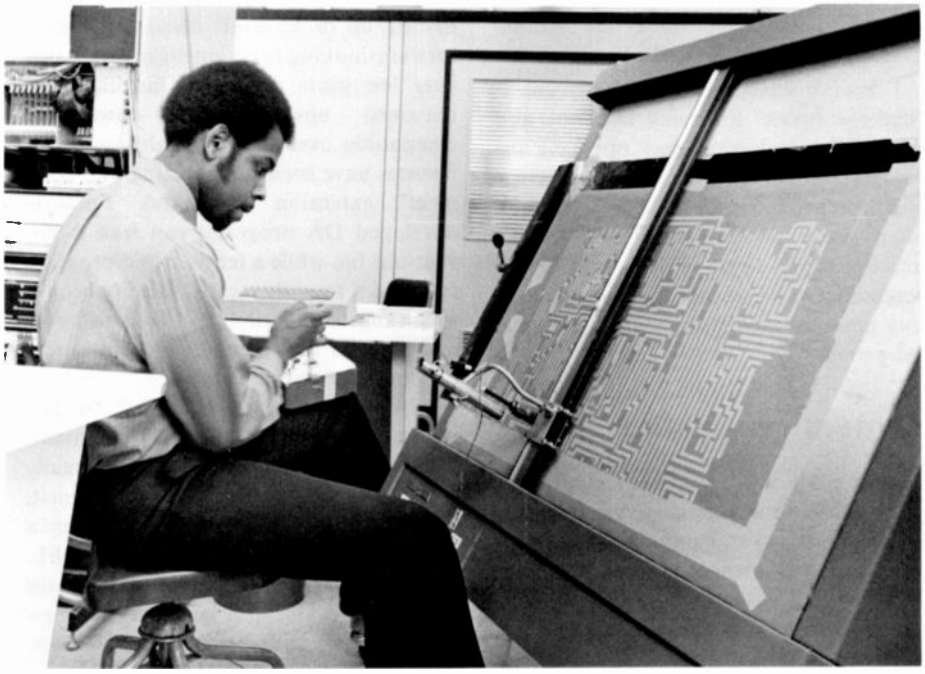

Fig. 3. Using the RCA-designed digitizer-plotter system (DPS), the operator can quickly capture artwork into the computer.

systems had an important role to play in the future of IC design. First, automated DRC proved that it was possible and achievable. Second, we began to internalize the fact that IC progress was relentless, and that the next year would bring even more complexity. We all felt that our DA tools were barely adequate for our needs that year, let alone the next. Hence, the DA systems we then envisioned had to cope with chips far more complex than those existing at the time. A new systems-approach had to be taken. We had to confront increased circuit complexity and we had to unify the worlds of circuit, logic and physical design. In addition, we had to cope with the problem of data integrity.

We decided that we needed a centralized, "strongly-coupled" design data base, hierarchical in structure, to solve all these problems. We called this the computer-aided design data base (CADDB).[5] A system diagram is shown in Fig. 4. This strategy "solved" many problems. The existence of only one copy of the design (centralization) ensured data integrity; "strong coupling" between the physical and logical design representations guaranteed they would remain in sync. The "common" data base also guaranteed that only one conversion program had to be written for each existing or new CAD tool, for example, logic simulation, circuit simulation, system simulation, automated layout and so on—the tool's input data structure needed only to communicate with the data base, not with N other programs, which implies N^2 conversion programs in the worst case. The hierarchical structure would solve the complexity issue. Finally, we could characterize the overall design process and postulate a new unified, disciplined methodology. This would require a substantial effort and would lead to a quantum leap in capability. The CAD project team set their sights on success in three-to-five years. In contrast, most of the remaining CAD effort continued to focus on incremental progress, based on specific needs, with these new tools going into production in one-to-three years.

The CADDB system was developed in the expected time frame. Hopes were high for its successful introduction into the production system. It was successful to the extent that it worked on all our test cases. However, it was not accepted by our design community, although many of its concepts and some of its software components have been adopted. What went wrong?

I am not really sure, but I suspect the following problems contributed. It is a complex system unifying many different applications-programs—which support both logical and physical designs—and hence presents a steep learning curve to designers. In addition, it requires a significant amount of preliminary work, such as labeling functional blocks and identifying and naming their electrical pins. This one-time cost is particularly significant for a test case. In addition, although the data-base management system we chose is highly efficient for commercial applications, it is not efficient for certain CAD applications-programs. It requires too many I/O events and too much memory.

As it was a totally new system, experimental cases encountered a significant number of bugs. Unfortunately, it is a

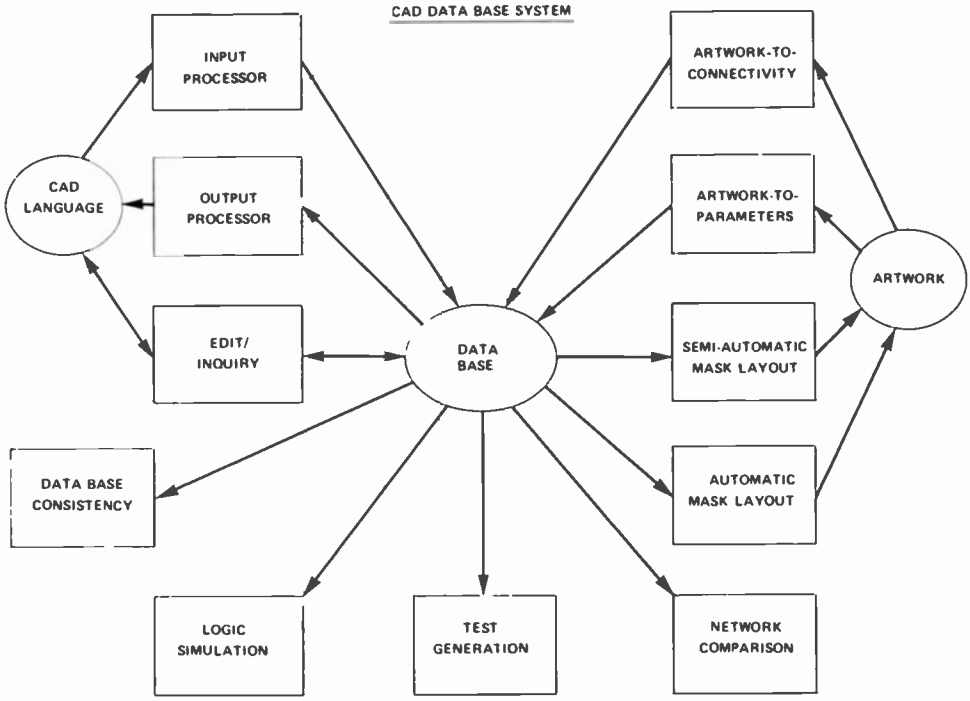

Fig. 4. The common "data base" is at the center of the CAD system and is designed to tie together all the capabilities shown.

highly integrated design system: one could not select the single benefit of the system that was desired, such as connectivity verification, and ignore the rest. It is an all-or-nothing system. Finally, although it was a system designed to unify the worlds of logical and physical design, designers were not using logical simulation extensively at that time and hence much of this benefit was not immediately evident. For these and other reasons, this quantum leap in capabilities was simply too high for our design community to achieve.

Meanwhile, the CAD development effort — which defined needed, incremental capabilities — continued to expand our set of design tools into the highly successful system it is today. Data from our software-usage monitoring system show that in 1979, over 30 of these CAD programs were accessed over 100,000 times by over three dozen engineering organizations throughout the RCA Corporation.

Based on these and many other experiences in DA software development — some quite successful, some not — can we discover any general principles to help us to succeed in the future? This is not an easy challenge. Here are a few of my own observations.

Criteria for success

First of all, I define a successful DA tool to be one which is used actively by many different design teams on a variety of designs, not simply one which has been tested successfully on a single, benchmark test vehicle. I believe that several criteria must be met before a DA tool can be successful.

1. The design community must perceive that the DA tool will cost-effectively result in a tangible benefit.
2. The approach must be technology-independent.
3. There must be close communication between the DA tool-builders and the designers.
4. Ninety percent of a DA tool's "paper" capabilities can be developed with approximately fifty percent of the total effort. This implies that it takes "forever" to finally get the last few bugs out and to add the last few "bells and whistles" required for user acceptance. It also implies that the creative DA developers who got it to the 90-percent point are probably bored with the whole project and are eager to move on to the next challenge, and to let the "second team" finish the project.

I believe that the last 10 percent is "make-or-break" for many DA tools and that the second team may not have the perspective or experience to make the compromises required for success. In fact, often some of the most challenging problems — involving designer acceptance — occur during the introductory phase of the development — the "last ten percent."

Current capabilities

At this point, I would like to describe LSI DA at RCA, equate this system to the complex designs and point out where I feel our greatest challenges will be on the road to VLSI and beyond. I will then use some of our historical perspectives to project the future evolution of DA.

Artwork

At the heart of RCA's artwork system, shown in Fig. 5, is an artwork representation called Design File Language (DFL).[3] It is an efficient, compact, program-readable language. Its primitive components include general-shaped (all-angle) polygons, orthogonal polygons, center lines with width, general purpose "comments" (to permit new extensions to work with old versions of software), and a general "definition" (building-block) function with an instance-specification (with nesting up to 12 levels deep). All this is forward-looking for a language developed over ten years ago. This language has remained upward- and downward-compatible over the years, although new features have been added (using the "comment" extension capability). Recently developed DA programs can read a ten-year-old file while a ten-year-old program can read a recently created file. We believe long range compatibility of both software and data is an essential issue in a real production environment.

Although DFL is "friendly" to DA software, it is not really friendly to humans. Therefore, the PLOTS language[2], already referred to, was created as a free-format, textual language for designers, which has a one-to-one function equivalence to DFL. One may view PLOTS as a source language (for example, assembly language) and view DFL as its machine-language counterpart.

This language is useful for designing *simple* structures or ones that are highly repetitive (such as memories). The arrows between DFL and PLOTS in both directions in Fig. 5 indicate that both a PLOTS compiler and decompiler were developed.

In order to design more complex structures we developed, during the late 1960s, the digitizer-plotter system (DPS) that directly works with DFL. By the mid-1970s, growing IC complexity made the DPS systems obsolete. We considered upgrading them and we also evaluated turnkey systems. Our analysis clearly showed that purchasing would be more

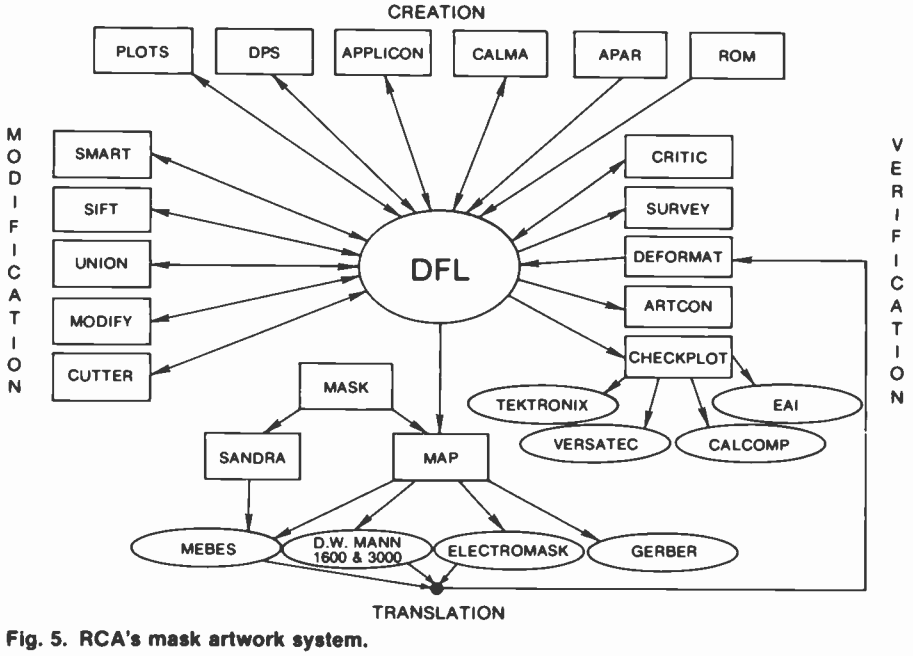

Fig. 5. RCA's mask artwork system.

economical than upgrading, so we purchased our first vendor-supplied interactive-graphics system. One such system (Applicon) is shown in Fig. 6. In Fig. 5 the arrows in both directions between the interactive graphics systems and the DFL boxes indicate that we developed conversion software to translate from their internal artwork representations to DFL and vice-versa. Hence, these systems became an integral part of our overall DA system. A design generated on these systems could use any CAD routine such as PG and DRC and designs generated using DPS or any other routine could be edited on these systems.

Another method to create DFL is via an automatic layout program. RCA has developed a family of these programs generically called automatic placement and routing (APAR)[7]. APAR refers to the automatic placement of predefined standard cells into regular rows of cells that are then automatically routed (interconnected). The first generation of this software was called placement routing and folding (PRF), while the second was placement and routing in 2-dimensions (PR2D). The third generation called multi-port 2-dimensional (MP2D) now is being used. The MP2D program has been highly successful in automatically laying out well over one-hundred chips. In fact, over the last ten years RCA's APAR programs have generated over 1000 custom-LSI devices.

Typically, a layout can be performed in weeks (from logic diagrams to PG tape). If the logic is simulated by our MIMIC logic simulation program, its connectivity description can be automatically translated to MP2D format. Automated layout is highly useful for making prototype chips (to quickly develop a custom IC for insertion into a system breadboard) and low-volume custom designs. It trades-off increased chip size to gain shorter design time and lower front-end cost.

After creating the computerized artwork, the next step is to verify it. This can be done in a variety of ways. The most basic is to generate a checkplot of all the features for visual inspection. Software exists to communicate to a variety of penplotters, to graphic terminals or to high-speed electrostatic plotters. Figure 7 shows one such system, our 72-inch-wide Versatec™ electrostatic checkplotter.

More powerful than the visual inspection provided by a checkplot is the CRITIC (Computer Recognition of Illegal Technology in Integrated Circuits) design-rule checking program[4] already mentioned. The designer may describe the geometrical rules of his technology in an English-like language to CRITIC. The designer usually does this once for a new technology and this description, contained in a user-named "CRITIC control file," is simply invoked when CRITIC is executed. An example of such a file is shown in Fig. 8. User-named CRITIC control file holds the geometrical rules of the designer's technology. CRITIC generates a listing that, for each violation, describes: what topological condition (for example, disjoint, contain, inside, overlap, abuts) or tolerance (width, notch, clearance or enclosure tolerance value) was violated; a PLOTS listing of the offending features and what definition they came from; and a DFL "error" file containing these offending features and tolerance "tic marks" for generating an error-checkplot.

Fig. 6. Using the Applicon interactive graphics system, the operator can easily and quickly make numerous changes to the IC artwork.

The artwork-to-connectivity extraction program (ARTCON)[6] extracts logical connectivity directly from the physical artwork for a subset of design styles. These include ones using predefined standard cells or other more general artwork building blocks. This program is used for all RCA's gate-universal-array (GUA) designs (including metal-gate, silicon-on-sapphire (SOS) and closed-cell logic (C^2L)

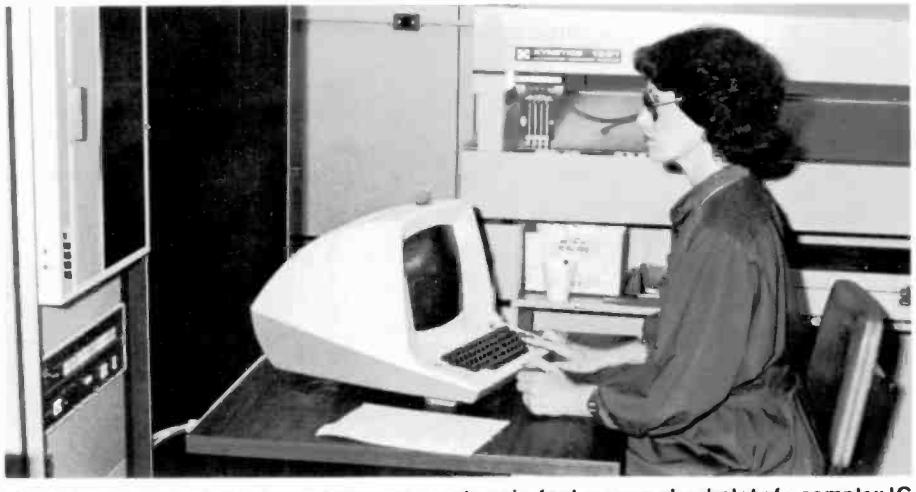

Fig. 7. This electrostatic checkplotter can create a six-foot-square checkplot of a complex IC in less than 10 minutes.

technologies) to automatically extract the connectivity for a variety of logic simulators. The circuit is again simulated to verify functionality and look for possible logic hazards. The truth-table output is then automatically translated by the AFTER (Automatic Functional Test Encoding Routine) program to a variety of automatic tester languages to provide a functional test program. This is highly useful, especially for quick turnaround designs such as GUA and APAR.

Another important function of the artwork system is automated modification of the artwork. The SMART (Selective Modification of Artwork Regions and Topologies) program[5], based on the Baird algorithms[8], provides many essential abilities. On a primitive level, it can do the Artwork Boolean Operators (AND, OR, NOT), oversizing and undersizing of features, and translation.

SMART can dimensionally "bias" (undersize) features to compensate for variations that occur during the mask-making and semiconductor processing operations.

It automatically can notch down the channel region of polysilicon gates, without narrowing the interconnect portion, to increase performance of critical parts. It automatically can generate new mask levels from existing mask levels under a number of conditions and do other automatic modification tasks.

At the working end, the MAP (Mask Artwork Program) translates the general polygonal shapes described in the DFL language into a format that drives a mask-making machine such as a D.W. Mann or Electromask pattern generator (to make a 5-or-10X reticle), a Gerber photoplotter (to make an 80X foil) or a manufacturing electron-beam exposure system (MEBES) (to make a fully step-and-repeated mask). The step-and-repeat array (SANDRA) program generates the required chip-location information, including dropouts and test inserts, and also labeling information.

Over the years we have found the DEFORMAT program to be highly useful. This decompiler-like program translates the data contained on a mask-making control tape back into DFL. This permits us to generate a shaded electrostatic checkplot of this data before the mask is made (for designer sign-off). This invaluable verification procedure tends to detect gross errors and otherwise obvious ones (improperly generated borders, improperly positioned or chosen library elements, missing alignment keys, an opaque "hole," and so on) before expensive masks are made.

The MASK system is another valuable facility at RCA. This software greatly simplifies the task of specifying MEBES or optical masters. It interactively requests all the information required to make a master. It gets chip information such as step-and-repeat distance and chip corners to generate borders automatically and it requests wafer size, chip dropout locations (or a standard code) and test-insert patterns to create the chip array. Since much of this information is common to a technology, we may specify it in a dataset called the Technology File which may be invoked for future circuit types of the same technology family.

After assimilating all this information, and performing syntax and semantics checks, MASK generates an "exec" file to run the following programs automatically and independently. First MAP translates a DFL file to a PG tape. Then SANDRA is run to make the step-and-repeat array. Then DEFORMAT converts the PG tape back to DFL. Finally, the checkplot software is run, which produces magnetic control tapes to generate the electrostatic checkplots.

We have found this type of system to be extremely valuable for automating standard procedures because it reduces effort, time and, most importantly, the chance of procedural errors.

A similar system to MASK is AUTOROM. It automatically generates a PG control tape and an automated tester tape from an input file consisting of the "1s" and "0s" desired for a custom mask-programmable read-only memory (ROM). All permanent data required for a specified ROM type, (for example, step-and-repeat distance) is stored in a permanent file, and so we need not respecify it to generate a new custom variant of that type. In addition, AUTOROM does over a dozen obvious validity checks on the customer supplied bit-pattern-and-option file before generating the PG and tester tapes. AUTOROM automatically invokes over a half-dozen CAD programs.

Simulation

We also have sophisticated circuit and logic simulation software tools. These tools verify the performance of an IC before manufacture.

Our recently developed MIMIC logic simulator[12] is state-of-the-art. We can use it in either interactive or batch mode. It is a four-level simulator (1, 0, X, Z). It permits a hierarchical building-block specification. It uses the CADL language developed for the CADDB system but not the data base itself. It has built-in models for primitive elements such as NANDs, NORs, ANDs, ORs, and a variety of flip-flops (both clocked and not). It properly models bilateral transmission gates including an arbitrary network of these. It supports inertial delay models for all gates: separate rise-and-fall delays may be automatically derived from tables of delay vs. either fanout or capacitive loading. A flexible hazard-detection facility exists. A large variety of interactive facilities are supported: different time intervals may be simulated, breakpoints may be inserted, desired outputs may be respecified, NET states may be displayed or reset. The network may start in the unknown (X) or an initialized state. The designer may request detailed timing information (show-

CRITIC CONTROL LANGUAGE

N^+	IS	LEVEL	4	WIDTH		
METAL	IS	LEVEL	6	WIDTH	5	
CONTACTS	ARE	LEVEL	13	WIDTH	2	AREA 9
XYZ	IS	LEVEL	28	WIDTH	5	NOTCH 3
METAL	CLEARS	XYZ	BY	2		
METAL	CLEARS	METAL	BY	5	IGNORE	BUTT
CONTACTS	INSIDE	METAL	BY	1		
N^+	OVERLAPS	XYZ	BY	2	ALLOW	BUTT
N^+DEV	IS	DEFINED	N^+	INSIDE	PWELL	
P^+DEV	IS	DEFINED	P^+ NOT	INSIDE	PWELL	
ABC	IS	DEFINED	XYZ	OVERLAPS	IMPLANT	
POLY-CONTACT	IS	DEFINED	CONTACT	INSIDE	POLY	

Fig. 8. A typical user-named CRITIC control file.

ing all the intermediate activity in response to an input change) or just stable-state results (the final state resulting from a new input state).

Our TESTGEN Logic simulator[9] can simulate up to 512 "faulty" networks in parallel and can help determine the "stuck-at" fault coverage of a set of test vectors. Another significant capability allows the designer to automatically translate from MIMIC input description format to APAR format (and the other way). This is not only fast and convenient, but eliminates translation errors. To further aid this process, a library of MIMIC subnetworks is being developed to functionally model each of the standard cells in APAR's library. Furthermore, MIMIC output format is directly compatible with the AFTER program which allows automatic translation of test vectors (network inputs and simulated outputs) to automatic tester format. This greatly simplifies functional test generation.

Our R-CAP circuit simulation program[10] is similar to well-known programs such as SPICE in its capabilities. It employs a highly efficient direct-current algorithm, has standard transient response and small-signal-alternating-current capabilities and has sensitivity to passive components and has noise-modeling capabilities.

The program's short-channel MOS transistor model is accurate to 3μm and is being extended further. It employs an extended Ebers-Moll bipolar-transistor model and also, optionally, a Gummel-Poon model which truly models base charge (unlike many other implementations). The user may choose an economical background batch mode or a highly interactive foreground mode. We can plot all state variables, such as node-or-branch voltages, component current including device-pin current and component power. Significantly, R-CAP has a correlated-component capability which allows the designer to specify any parameter (such as a resistance, capacitance or any model parameter such as threshold voltage or beta) in terms of a general algebraic expression. This supports design for manufacturability, (that is, meeting electrical specifications in the face of processing variations).

We have developed the very sophisticated, cost-effective and easy-to-use TDAS (Test Data Analysis System)[13]. The system's basic primitive abilities — histograms, wafer maps, trend diagrams and so on — may be custom-assembled for a specific application. This system is used on a daily basis to support six different processing lines at three different RCA manufacturing locations. Process, type and design engineers automatically get the reports.

Under active development is a general parameter correlation capability. This will provide graphical tools such as scatter diagrams, and analytic tools such as regression analysis. This will further aid the goal of design for manufacturability.

The challenges of VLSI

Major questions before us are: What are the compelling challenges to DA as we move toward VLSI? Where must we expend most of our future efforts to enable VLSI to become a reality? I see vast challenges ahead, especially in layout, design verification and testing. I can envision solutions to these problems just as many of my co-workers in this field can.

As I think back to my early days in DA, I have this strong feeling of *deja vu*. In the early 1970s, we clearly saw some of the problems of complexity and outlined elegant and achievable solutions. But many of the more elegant and far-reaching solutions never took hold in our design communities. However, whenever we added a new (but *incremental*) capability that solved a real problem, and that cleanly fit into the existing structure, it was accepted. Our DA system evolved to where it is today through the addition of incremental capabilities. Therefore, as I try to project the evolution of DA to serve the needs of VLSI, my optimism is for growth modes that I have seen work first-hand already.

Without a doubt, I believe the major problems to be solved on the way to VLSI are in layout, testing and design verification, in that order. Moore[14] predicted that the design problem — product definition, design and layout — will be the rate-limiting process constraining VLSI use. First, he thinks that this cost ("front-end-cost") is growing exponentially with time (and thereby tracking complexity growth) such that the front-end cost-per-function is remaining roughly constant. Second, he thinks that as we move toward the system level of complexity on a chip, product uniqueness increases, thereby decreasing potential volume. This increases the front-end cost of a function per unit IC. Meanwhile, technology advances are decreasing dramatically the per-unit-manufacturing-cost of each function. Clearly, front-end cost will soon dominate the total cost of a VLSI IC.

Physical design

Clearly, design and layout techniques that dramatically improve productivity in the front-end areas are a major challenge to DA developers. I do not believe this is an impossible problem. In fact, I am confident that we are evolving, slowly, to a solution of the productivity and cost-per-function issues.

The fundamental reason why front-end cost per function is not declining is because we are still designing mostly at or near the device or gate level. I believe that the way to reduce front-end cost in IC design is to design and layout VLSI chips using higher-level functional building blocks that may be of SSI, MSI or even LSI complexity. For each product group, these blocks will include universal functions (such as clocked flip-flops, shift registers, ALU, RAMs, ROMs, encoders, decoders, expandable PLAs, comparators, A/Ds, D/As) and specialized proprietary application-oriented (yet often reusable) elements.

In addition, we must develop higher level, more productive techniques, such as symbolic layout[15], to create these functional blocks. Furthermore, these blocks must be assembled within a structured, hierarchical design environment to allow design verification to remain tractable.

However, is this "apple-pie" technique achievable both technically and by the crucial criterion of designer acceptance?

I am particularly encouraged in the practicality of this approach by our large success in using the APAR techniques (already described) in our semiconductor commercial product areas. As indicated, it has been highly successful in the systems area for over 15 years. At this time, the acceptance of this technique for a subset of commercial designs is growing rapidly, precisely because of the necessity to reduce front-end cost and design time for system-type components for which hand-packed layout techniques are uneconomical.

No automatic-layout approach will result in minimal area. For standard cell approaches, I believe the major cause of the area penalty is the use of fixed-height standard cells and their algorithmic placement. Fixed-height cells are rarely optimal in size — simple cells tend to be too narrow and complex ones too wide. Also, rigid pinout requirements tend to reduce cell density. And algorithmic placement is never optimal because computers lack global perspective — local optimums are usually found. This leads to larger-than-

required routing surfaces and affects overall chip size and sometimes even performance (long interconnects with too many tunnels add excess series resistance and capacitance to ground). Fortunately, CMOS technology is quite tolerant of these problems.

I believe the advantages of APAR can be extended to dense VLSI while minimizing its limitations by adopting a semiautomatic technique which cleverly elicits designer guidance. We are developing one such approach called FLOSS (Finished LayOut Starting from Sketch)[16]. This approach allows us to use arbitrary-sized cells that can be SSI, MSI or LSI in complexity. The key insight of FLOSS is that it uses the global perspective of the human to get a rough, initial layout (the sketch within which the designer optimizes placement and wireability) and then uses the computer to do the tedious compaction. The rough layout is equivalent to the chip plan required before handcrafted layout begins.

This process can be optimized by allowing extensive but rapid iterations. The loose initial sketch is modified by insights gained from subsequent compaction. Another benefit of this approach is that the designer can do future modifications (which occur more often than we would like to admit) on the loosely packed sketch, not on the densely packed, final layout. We plan to further optimize the iteration part of this approach by developing a distributive computer system tying together an interactive graphics system with a fast processor.

The logic and layout designers can vastly improve productivity by using this building block technique to design at a much higher level of complexity. The challenge is to develop a set of "macrocells" that have reasonably high complexity (which is the source of productivity gain), but that are not too functionally unique (which would require designing a large library of macrocells, and each, of course, must be accomplished at the device level). Other challenges are to develop a design style that flexibly addresses aspect ratio, pinout-location and power-bussing issues.

A highly promising technique for the design of macrocells — but not VLSI chips — is symbolic layout such as a STICKS approach[15] The challenge here is that the "compiling" of a STICKS diagram into silicon-mask features is highly technology-dependent. As technology evolves, we may have difficulty enhancing the compiler for optimal density. Of course, design-rule parameterization may be hugely advantageous in the face of rapid process evolution. One hope is that most of the parametrized designs will be readily scalable to tighter design rules — this, of course, assumes that design rules will only change quantitatively *not* qualitatively, that is, topologically. Or, if there are a few qualitative changes, we must be able to readily modify the software compiler.

The FLOSS approach is advantageous because it is not vulnerable to the above risks but can readily capitalize on whatever benefits symbolic layout can offer. When it is judicious, a macrocell can be designed at the device level.

Design verification

Other crucial issues are both logic and circuit verification and the crucial issue of physical design verification. As described, we and other companies have excellent circuit and logic simulation tools. Our MIMIC logic simulator is hierarchical in nature. We can thereby develop a library of logical models for the predefined physical building blocks (macrocells) described in the previous section. This lets the logic designer achieve the same type of productivity leverage as the layout designer, that is, working with high-level primitives.

This approach, however, will be inefficient as complexity increases. Although it will be simple for the designer to specify and analyze rather complex systems by designing them in a top-down, hierarchical structure, the simulator itself must perform a complete macro-expansion of the system, as it simulates on the gate level.

Clearly, a general, transparent high-level, macromodel ability must be developed to improve simulator efficiency — this is crucial for fast, economical interaction with the designer. This will be relatively straightforward for simple functional blocks such as ROMs, RAMs, PLAs, counters and shift registers. However, many subtle problems do exist with, for example, detailed timing accuracy, hazard detection and intelligent (minimal) propagation of the unknown (X) logic state. It will be even more challenging for more general functional blocks such as ALUs and decoders.

On the positive side, it is obvious that we can incrementally solve this problem, by adding additional functional models (macromodels), one at a time, focusing on those that most heavily affect simulator cost.

In general, to simulate VLSI circuits, or subsystems, we will need even higher levels of analysis, such as register transfer level (RTL) and behavioral-level simulation. Although these types of simulators exist, I believe the challenge will be to structure a hierarchical simulation capability involving multilevels of simulation that communicate *efficiently* with one another. This will permit system-level simulation to verify lower-level block design as top-down design proceeds. Impressive work[17] has occurred in this area, but I believe the efficiency challenge remains to be solved.

There are many challenges in physical design verification. Many of these can be met if we develop structured design techniques. These techniques extensively use hierarchical layout implementation — nested building blocks with clearly defined design rules governing their proximity and interconnection. Clear definition is crucial if currently available design rule and connectivity verification techniques are to be extended to VLSI. I believe this challenge facing physical design verification will require strong coordination between CAD tool developers and the design community.

Testability

Another huge challenge to the successful use of VLSI is the ability to test the devices we design. This is already a significant problem for many designs of LSI complexity. A number of techniques for design for testability (DFT) have been proposed including scan techniques[18], on-board test circuitry including use of signature analysis, behavioral-level test development[19] and designs using high visibility of all internal sequential logic to either probeable pins or the bus structures. In addition, I believe CAD testability aids such as controllability/observability measures[20] will help the designer who is incorporating DFT.

There is the obvious trade-off, however, between testability and unit cost. The whole industry has traditionally emphasized silicon real estate above DFT for unit-cost reasons. Our studies have shown that DFT, using currently understood techniques, can be quite expensive — more so than their proponents acknowledge. In addition, conventional testability measures, such as "stuck-at" fault-coverage monitors (used by all known parallel and concurrent fault simulation programs) do not address the issue of pattern-sensitive faults. Nor do the scan techniques test for them. These may become more significant as design rules shrink and inter-electrode couplings

become more significant. This may also be crucial in the reliability area where migration of metal interconnections, after stress testing, may accentuate pattern-sensitivity (or lead to failure). As this will be a function of process evolution, built-in DFT techniques may be essential for even mature VLSI devices.

I believe the development of cost-effective design-for-testability approaches and their supporting DA tools remain a large challenge.

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A system for the automated design of complex integrated circuits

The automated layout of an LSI circuit is only part of the story — circuit simulation programs at RCA give the customer assurance that the circuit meets expectations.

Abstract: *The authors describe the design flow leading to successful, rapid automated circuit layout using automated placement and routing (APAR) and, moreover, they cover computer simulation programs and the assortment of checking and conversion programs needed to assure correct circuit performance — before fabrication.*

Introduction

Amazing advances have occurred in the field of semiconductors during the last fifteen years. Things that were complex in 1965 are almost mundane today. The difficult tasks of that year are commonplace — the impossible has become ordinary. Circuits that were beyond the comprehension of most people in 1965 are being manufactured in large numbers today.

The most complex circuit types available at that time included single bit storage elements, monostable multivibrators, and quad, two-input gates. One need only look around one's own home or office to see examples of today's complex circuits. The quartz wristwatch, pocket calculator, electronic automotive controls, advanced pacemakers, electronic toys and personal computers would all have been impossible without the development of Large Scale Integrated (LSI) and Very Large Scale Integrated (VLSI) circuits.

The development of, and demand for, these circuits has created a new problem. The complexity of the circuits requires teams of skilled individuals working over extended periods of time to produce the first working circuit. One recently designed microprocessor required a team of from two to sixteen people working together for three years before the design was successfully completed. This span of time is clearly not responsive to the needs of customers who are trying to impact the marketplace.

One solution to this problem is the use of the Automated Placement And Routing (APAR) of standardized circuitry to form structures tailored to the requirements of a customer. When a circuit is designed with APAR techniques the time required for the simulation, design, fabrication and test of a new circuit can be as short as seventeen weeks. This time will, of course, vary with the complexity of the particular task.

The basic APAR approach utilizes a computer program to place standardized cells of circuitry and the associated interconnections on a relative surface. The use of standardized cells eliminates the need to design new circuitry and allows the performance of the finished circuit to be more accurately predicted. Once the cells have been placed on the surface, the same computer program can calculate the interconnections required for those cells. The computer, by means of its excellent bookkeeping ability, can operate with an error rate that is orders of magnitude better than even the most experienced circuit designers'. This virtue vastly increases the probability that a new circuit will be completed correctly and in a timely manner.

The automated layout of an LSI or VLSI circuit is only part of the story. To be truly successful, the customer must be assured that the finished circuit will meet his expectations before he commits large sums of money to the layout and fabrication of that circuit. This assurance is provided through the use of the circuit simulation programs available at RCA. Detailed analog simulations of circuit cells accurately predict the performance of those cells before they are manufactured. This information can then be utilized with a digital simulation of the entire circuit to provide the customer with an accurate prediction of how well his circuit will (or will not) perform. If the simulation reveals design deficiencies, they can be corrected prior to the manufacture of any circuits. This feature alone can save six months to a year in the development of a new circuit type.

Simulation of the overall circuit serves an additional function — the results of the simulation can provide the truth tables necessary for the testing of completed circuits.

To make these design tools truly useful, it is absolutely necessary that manual intervention be minimized. Every time a person has to retype or reformat data, the possibility for error is present. For this reason software programs have been developed to provide the interface among each of the design tools. Once a simulation has been successfully completed utilizing standardized cells and data, that data base can be converted to the format required by the APAR programs. This same conversion program can be utilized to convert the output of the APAR program to the format required by the circuit simulation software, and thereby to provide a check on the accuracy of the APAR program. Another conversion program is capable of reformatting the output of the APAR program into a form that is compatible with various means of displaying the completed design. The displayed data can be in

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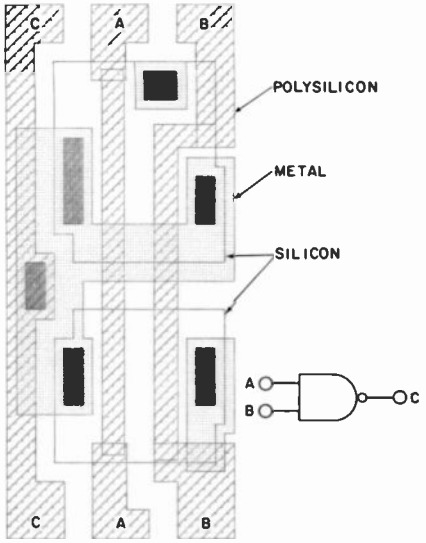


Fig. 1. Two input NAND gate.

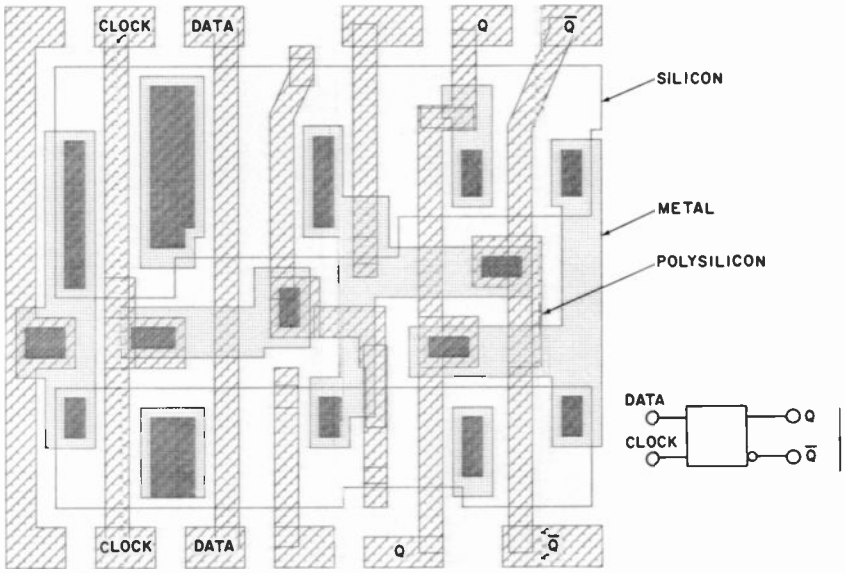


Fig. 2. D-type flip-flop.

the form of video signals at a graphics display or hard copy on any one of several styles of plotters. Finally, the data can be converted into the format required by the photomask generation equipment.

Standardized cell libraries—the first step

Virtually all modern integrated circuit designs make use of a cellular approach to circuit layout. Groups of transistors are designed as units that can be placed on a surface. Interconnections are then defined among the various groups. The design and redesign of these groups for every new circuit can provide extremely dense results, but the probability of error is ever present and the design cycle is often lengthy.

A much more practical approach makes use of a library of standardized cells of circuitry. The libraries for bulk CMOS and CMOS/SOS technologies provide the circuit designer with the wide range of functions (NAND, NOR, Exclusive-OR, storage elements, etc.) required to complete his assigned design task. Because new cells are the exception, rather than the rule, they can be added to the appropriate library without placing an undue strain on the scarcest resource in the integrated circuit industry — manpower.

In order to be compatible with the APAR software, each of the cells has been designed on a coherent grid. In addition, all of the cells in a particular library are of a consistent height and have accessibility to each input and output on both the top and bottom of the cell. Figures 1 and 2 are illustrations of the topology for a two-input NAND gate and a D-type Flip-Flop, respectively.

Simulation—a necessity for success

All circuit designers are familiar with the feeling of depression that occurs if their circuit does not work when it is finally built. In the case of a circuit built on a printed circuit board, the problems can often be corrected with some jumpers and a few days of effort. Integrated circuits, because of the inaccessibility of signals, may require weeks of effort just to locate a problem. Corrections must be made at the photomask level, and a new run of wafers fabricated. Often, secondary problems are then discovered, requiring one more iteration of the design. Complete debugging of a complex design can consume six months of engineering time.

The solution to this problem is computer simulation of the circuit before it is fabricated. Analog simulation of critical portions of the proposed circuit can reveal several types of design deficiencies or provide characterization data prior to fabrication. RCA's circuit analysis program (R-CAP) is used to perform these functions for the individual cells and larger groups of circuitry.

R-CAP does have some finite limits beyond which detailed simulation is no longer practical. Complex integrated circuits would be extremely expensive to simulate with a component-based simulator, because of the vast amounts of computer memory and the large number of computations required to perform this task. Complex circuits can be simulated with a new logic simulator developed at the Solid State Technology Center (SSTC) in Somerville, New Jersey. The MIMIC program utilizes logical descriptions of the functions of each of the standardized cells, along with the propagation delay characteristics predicted by R-CAP (or measured on previously fabricated devices) to model circuits with complexities up to 3000 equivalent gates.

When a circuit is simulated using MIMIC and the standard descriptions of characterized logic elements, the probability of success, from a logic design view point, is limited only by the thoroughness of the truth table utilized for that simulation. A secondary advantage of complete simulation is the generation of a logical pattern that can be utilized to test the finished circuit.

APAR—the key to topological success

The simulation routines, when exercised fully, ensure that the logic used in a new design is correct but they do nothing to enhance the topological layout of that design. The computer program that can ensure the success of a new layout is the Multi-Ported, Two-Dimensional (MP2D) program developed at the Advanced Technology Laboratories in Camden, New Jersey.

MP2D utilizes physical descriptions of standardized circuit cells and nodal connection lists to design the finished circuit. The program places the cells with respect to one another in a manner that minimizes the interconnect requirements among the cells. It then determines the paths that must be defined to interconnect the circuitry. Finally, it compresses the interconnections and the placement of the cells to minimize the circuit size consistent with the appropriate design rules. MP2D, when properly used,

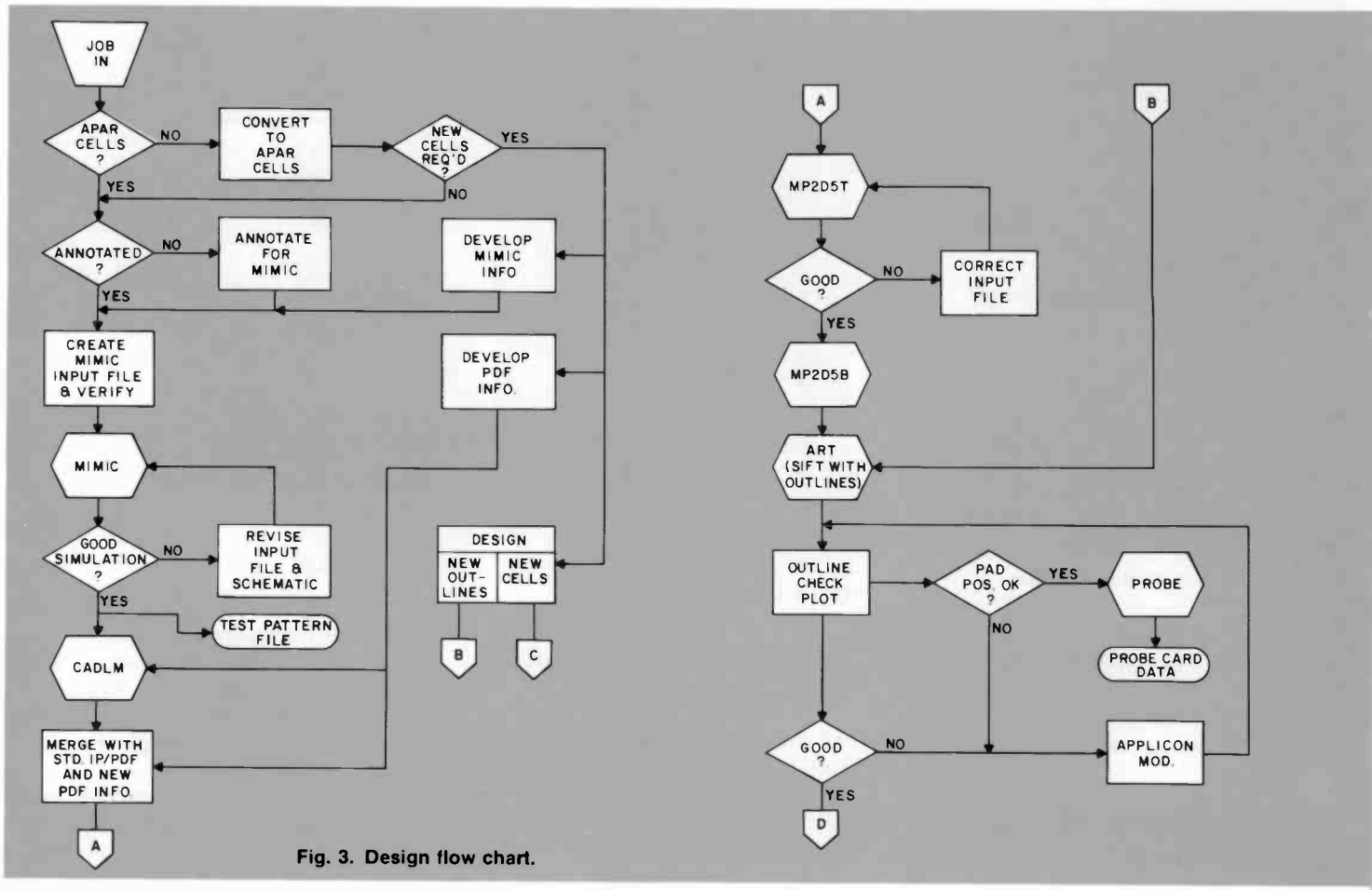


Fig. 3. Design flow chart.

can generate circuit designs with reasonable densities in less than one month, rather than in the one-to-two years required for custom circuits.

Conversion programs—the "glue" that holds the system together

Logic simulation and automated layout are each valuable tools, but they cannot be truly effective if they operate with independently generated inputs. One of the conversion programs developed at SSTC utilizes the MIMIC logical descriptions and nodal net list to generate an MP2D-compatible description of the circuit. In this way, human intervention (with the associated probability of error) is almost completely eliminated, and the circuit designer is assured that the circuit being designed is identical to the one that was simulated. This same program can be used to convert an MP2D design into a MIMIC data base and allow a simulation of the completed design, thereby adding one more level of confidence.

Once the MP2D design is complete, another conversion program provides the interface between MP2D and the various means of displaying the design. These means include, but are not limited to, the Applicon graphics system, pen plotter, Versatec electrostatic plotter and Tektronics video display. Once the description is formatted in the Design File Language (DFL), the design can proceed in the same manner as any other integrated circuit. The remaining steps include checking (the human eye is still a highly valuable tool in integrated circuit design), mask fabrication, wafer fabrication, testing and packaging.

A recently developed conversion program (PROBE) can provide advanced data relating to the placement of probing pads on the circuit. The PROBE program decodes the position of each of the input and output cells on a design and generates all of the information necessary to fabricate a probe card that can be used to test the finished wafer.

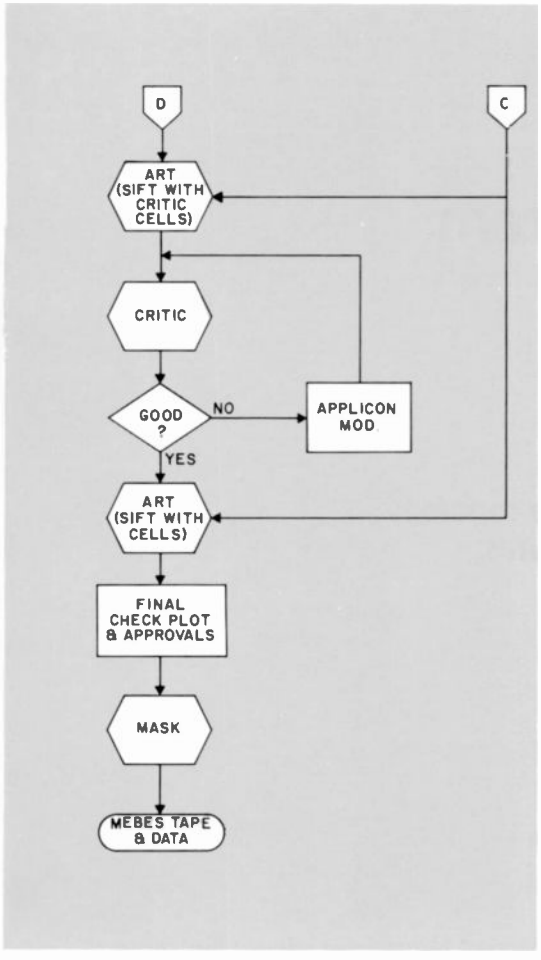
The design flow—an overview

Now let's follow the flow of a typical job through the design procedure. The path involving no new cell designs will be considered. Reference to the Design Flow Chart (Fig. 3) will be helpful.

The first task is to annotate the logic drawing with APAR cell type members and MIMIC part names. Cell type numbers correspond in general, to single logic functions such as inverters and two-input NOR gates, although some cells may contain multiple logic functions and should be so indicated. Part names may be numeric, alphabetic or alphanumeric, but must be unique to each part (cell) in the logic. Cell pin numbers should also be indicated on the drawing to facilitate later checking.

When the logic diagram has been completely annotated, the MIMIC input file may be created. A printout of the file should then be obtained and checked back against the logic drawing to ensure accuracy. The design engineer then interactively exercises the logic using the MIMIC program until satisfactory results are obtained. All changes incurred during the above interactive exercise must be noted on the logic drawing. The resulting MIMIC files then become the basis for developing an APAR input file and a test pattern file for later testing of the chip.

The next step in the design procedure is to create an APAR input file. Invoking the CADLM program with the MIMIC input net file and an APAR standard Pin Data File (PDF) as inputs will result in the creation of a file containing all the elements



unique to the subject task, namely an MP2D element-to-pattern assignment table and net list. For the typical job, the above file is then merged into a file containing standardized run data (MP2D5 program switches, PDF data, etc.). After a few simple edits to enter the chip name, number of cell rows and number of pads on each side of the chip, the file is ready for MP2D.

To ensure that the input file is acceptable to the APAR program, a foreground syntax checking program, MP2D5T (est) should first be run. This procedure will very often uncover syntax errors and will greatly enhance the feasibility of obtaining a successful first run through MP2D5B(atch). A background job may be entered for MP2D5B, once MP2D5T has been successfully run.

The output of MP2D5B is a Design File Language (DFL) file containing all the interconnect metal and tunnels as well as reference calls to cells and tunnel-ends. With the aid of the ART program, this file is combined with a file containing outlines of all cells. The resulting file may be plotted either in black-and-white shading on a Versatec plotter on in color on a pen plotter. This check-plot should be very carefully checked back to the logic diagram. Modifications to the DFL design file are accomplished through use of the Applicon interactive design system. Modifications should of course, be check-plotted and checked until correct.

If no modifications are required, or when the required modifications will no longer affect pad locations, the DFL design file is run through the PROBE program. The output of the PROBE program is a list of pad-center coordinate points and an edge sensor location suitable for obtaining a probe card for wafer probe testing.

Once a satisfactory check-plot has been obtained, the design file is then exercised by the design rule checking program, CRITIC. Design rule violations indicated by CRITIC are located and corrected by use of the Applicon. When CRITIC has indicated that the design file is free of design rule errors, a final check-plot is obtained, reviewed and approved.

The design file, now ready for masking, is combined with the APAR cells using ART. It is then entered into the MASK program which outputs a magnetic tape containing the design file in ETEC language and input command data for the MEBES mask plotter. Thus, having started with an unverified logic diagram, we find ourselves some four-to-six weeks later ready to obtain masks for a simulation-verified integrated circuit that has excellent possibility of first-shot success.

The final step of the design flow now remains — the generation of a test sequence. In order to ensure that the truth table utilized in the test sequence corresponds to the desired implementation of the logic, the MIMIC simulation results are reformatted through the use of the AFTER program. This method eliminates the need for debugging the truth table when finished wafers are first tested, but it also requires that the circuit designers do a thorough simulation of the logic. Thus, the MIMIC simulator will help to ensure that the logic is correct and will provide a sequence that can be used to test the finished circuit.

Summary

A design system has been described that provides a logic designer with an assurance that his design is correct. The system can then be used to convert the simulation data base into an integrated circuit design, with maximum probability of success on the first iteration. This system is fully operational and is being used at the SSTC in Somerville, New Jersey.

Fred Heath joined RCA in 1953 at Government Systems, Camden where he was involved with printed wiring design and fabrication for 18 years. In 1971 he transferred to SSTC. He is principally involved in the design of large-scale integrated circuits for Advanced Applications using APAR and Custom Techniques. He is also responsible for the design and maintainance of the standard APAR cell files.

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Richard Lydick started with RCA in 1965 at Aerospace Systems Division in Burlington, where he worked on the system and detailed design of military electronics and was responsible for the design of PMOS arrays. After an absence of seven years, he joined SSTC in 1979 where he has been involved in the design and application of LSI circuits using APAR and Custom Techniques.

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B.S. Wagner

A multi-technology checking program for large-scale integrated circuits based on standard cells*

In some cases an experienced, senior-level engineer must take approximately seven hours to do the LSI checking that the topology and connectivity checking (TACC) program can do in 15 minutes.

Abstract: *Designers who use the multi-port two-dimensional (MP2D) computer-aided design program for large-scale integrated (LSI) circuits need an inexpensive way to check the correctness of these designs. The checking program described in this paper is inexpensive, handles many technologies and is easy to use.*

Background

Since its introduction in 1972, the multi-port two-dimensional (MP2D) computer program has been distributed to approximately 30 companies. A fully automatic placement and routing program based upon the standard cell technique, MP2D quickly and inexpensively helps the designer to make LSI arrays for various applications. Many users of custom LSI arrays need MP2D because artwork, masks and initial design are major equipment development costs.

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The standard cell technique for producing very large scale integrated (VLSI) arrays depends on a library of custom circuits or standard cells. Each of these standard cells has a unique identification or pattern number. An engineer implements a logic design by specifying the standard cells he needs and the way in which the cells will interconnect.

The designer must give the MP2D program specifications for the standard cells to be used, the way in which the cells will interconnect and a box-outline representation library of standard cells. The MP2D program automatically places and interconnects these standard cells.

MP2D generates a completely finished array design, but sometimes the designer must manually edit it. Typically, manual editing is done when unusual power distribution requirements exist in certain areas of the chip. Although the designer usually edits on an interactive graphics system that has some very powerful commands for rapidly manipulating graphical elements, the manually-directed editing often corrupts areas or layers of the array.

Even if the output of the MP2D program is not modified, an error could exist in either the connectivity or topology of the output because designers naturally tend to select designs that tax the abilities of the program. Thus, chip designs must be checked before being released for fabrication. Customarily, engineers have scrutinized magnified (100X), multi-color "check plots" — approximately 20 inches on a side — of the MP2D-generated chip designs. This is a slow, error-prone, expensive and difficult method for checking chip designs. Over the last few years, both the device densities of chips and the sizes of the chips have increased. Consequently, manual checking has become more expensive and undetected errors have become more probable.

Automatic checking of MP2D-implemented arrays began in 1975, when a program was written to check chip designs implemented by a predecessor to the MP2D program. This predecessor program was called two-dimensional placement and routing (PR2D) and the checking program was called automatic placement and routing artwork integrity survey (APRAIS). Tony Scialdone, who worked for the Palm Beach Division of RCA, wrote APRAIS. The program was successful both at the Palm Beach, Florida and Camden, New Jersey locations of RCA.

When the new MP2D program was introduced in 1972, the APRAIS program could not be used to check the new MP2D-implemented chip designs. The APRAIS program needed major changes. In 1977, an upgraded APRAIS program became

the topology and connectivity checking (TACC) program.

TACC program functions

The TACC program can:

- Check the topology and connectivity of MP2D-implemented chip designs;
- Check chips designed using any one of four different standard-cell families;
- Provide diagnostic messages and a minimum of false-error messages;
- Provide graphic representation of error conditions on an Applicon interactive graphics system; and
- Require a few user-inputs for program execution.

Basic assumptions of the program

MP2D-implemented chip designs use a set of previously designed custom circuits or standard cells. The basis of TACC is that these standard cells, while being designed, are carefully checked. Any errors are corrected before the standard cells are put into the library. Therefore, the TACC program checks for topology and connectivity errors up to and including the input-output pins of these standard cells.

Topology and connectivity checking

The TACC program checks for: short-circuited signals; open-circuited signals; unconnected pins; and spacing violations. One input to the TACC program specifies all of the signals on the chip and their destinations. As data about each signal is read in, the program assigns a sequential number to the signal and prints out both the signal and its sequential number. Any time the program detects (from a comparison with the artwork tape) that, in fact, two supposedly distinct electrical signals are connected inadvertently, it prints an error message containing the sequential numbers of the two signals that are short-circuited. Similarly, whenever the program detects an electrical open circuit in any signal, it prints an error message containing the sequential number of the signal. If the signal is electrically open in more than one location, the program prints an error message for each location.

The program also checks to ensure that all of the pins connected to the various signals are actually connected. If the program finds that a pin is not connected, then it prints an error message giving the X and Y coordinates of the pin and the signal that the pin should be connected to.

The program checks for various edge-to-edge spacing violations. On these chips, connections are made via conducting paths that exist on either a metallization level, a polysilicon level or a combination of these levels. The program checks for minimum metal-to-metal spacing, and minimum polysilicon-to-polysilicon spacing. It checks, not only between the various paths that interconnect the pins, but also between the paths and the standard cells. When the program finds a spacing violation, it writes an error message that states the level where the violation occurred, the types of components involved in the violation, and the locations of the two components involved in the violation.

Multi-technology flexibility

The program can check chip designs in any of the following four cell families: 4.2-mil silicon-gate silicon-on-sapphire (SOS); 6.3-mil radiation-hardened silicon-gate SOS; 11.4-mil closed-cell logic (C^2L) and 12.6-mil C^2L. The TACC program holds lists of internal control parameters. These lists correspond to the cell technologies that the program can accommodate. Once the relevant technology is specified, the program can find the proper parameter list to be used. While the program currently handles only these four technologies, expansion of the program to other technologies is readily accomplished.

Diagnostic and other messages

The program prints three classes of messages.

The first class of messages is informational. These messages either repeat some of the required or optional input information or denote that the program will use a default parameter. These messages give a comprehensive set of information in one printout for documentation purposes. Samples of these messages are listed in Table I.

The second class of messages tells the user when the input data is incorrect, incomplete or unrecognizable. Under many of these circumstances, an attempt to complete the checking of the design would be wasteful. These messages prevent such an action. Samples of these messages are given in Table II.

The third class of messages consists of the actual diagnostic messages. The first possible group of diagnostic messages to occur are the connectivity-error messages. Topology checking is performed after connectivity checking, therefore spacing error messages are the last possible messages to be printed. Some possible diagnostic messages are shown in Table III.

One of the greater challenges in writing artwork checking programs is to eliminate false error messages. A potential user will tolerate only a very small number of false alarms before he stops using the program. This program has given false alarms very infrequently , and the program has been changed as these messages have appeared.

Table I. Sample informational messages generated by TACC

1. **"The Process Technology Key Is X"**
   . This is the process technology key that was specified on one of the input parameter cards.
2. **"The Specified Metal-To-Metal Spacing (In Centimils) = XX"**
   . This is the metal-to-metal spacing (edge-to-edge) that was specified on one of the input parameter cards.
3. **"The Default Metal-To-Metal Spacing Will Be Used"**
   . No metal-to-metal spacing was specified on the input parameter cards and the following spacing will be used by the program:
   SOS = 0.25 mil (edge-to-edge)
   C^2L = 0.30 mil (edge-to-edge)
4. **"The Specified Poly-To-Poly Spacing (In Centimils) = XX"**
   . This is the poly-to-poly spacing (edge-to-edge) that was specified on one of the input parameter cards.
5. **"The Default Poly-To-Poly Spacing Will Be Used"**
   . No poly-to-poly spacing was specified on the input parameter cards and the following spacing will be used by the program:
   SOS = 0.30 mil (edge-to-edge)
   C^2L = 0.20 mil (edge-to-edge)

Graphic representation of error conditions

For each topology or connectivity error that occurs, a graphic representation of the

Table II. Sample TACC messages caused by incorrect, incomplete or unrecognizable input data.

1. **"Illegal Process Technology Key"**

   An illegal process technology key was specified on the input parameter card.

2. **"Unrecognizable NOTO55 Record: XXX...XXX"**

   XXX...XXX is the 80 character record (on the artwork instruction input tape) which the program does not recognize. The record is skipped and processing continues. This error generally indicates that the user made a mistake in manual modification of the chip.

3. **"Illegal Diagonal Line Set Pair. See NOTO55 Record With Subject Sequence Number NNNNN."**

   The TACC program has found a non-orthogonal line set pair. The TACC program can handle only orthogonal line sets.

4. **"XXXX Pattern Undefined In Pin Data File"**

   Information on this particular pattern number is missing from the pin data file.

error is also generated. This is done through the generation of a magnetic tape in the design file language (DFL) format. The magnetic tape information then is converted into a format compatible with an Applicon interactive graphics system, and loaded onto the graphics system. Then the user may view and correct the errors on the graphics system.

When the graphic representations of the errors are generated, they are placed into one of several possible display levels, depending on the class of error. This grouping of errors into various display levels also facilitates the analysis of the program's output.

User inputs to the program

Inputs to the TACC program can be divided into two classes — required and optional. The inputs to the program are:

1. *A pin data file*. This file describes the external characteristics of each circuit or cell in the standard cell library — pin locations, cell width, etc.
2. *A node list*. This list describes the destinations of the signals.
3. *An element-to-pattern assignment list*. This list identifies, by a unique element number, each occurrence of a pattern in the design.
4. *The output tape from the MP2D program*. This tape eventually is used to generate the artwork masks for the chip.
5. *Various control cards*.

Input items 2 and 3 (node list and element-to-pattern assignment list) are optional outputs from the MP2D program. Input item 1 (pin data file) is a required input to the MP2D program. A node list and an element-to-pattern assignment list also are part of the MP2D program's required input. But, these two lists are not identical with input items 2 and 3 for the TACC program because MP2D, in the course of its execution, may make modifications to the two lists. For example, MP2D may interchange logically equivalent pins on a cell. In order to check correctly, TACC must use only updated lists from the MP2D program.

Examples of program output

The TACC program is written in the IBM System/360 Basic Assembly Language. Versions of the program currently exist on a Univac Series 70/55, an IBM 370/158 and an IBM 360/65 computer. On the Univac computer, the executable code requires approximately 210,000 bytes of

Table III. Sample diagnostic messages generated by TACC.

1. **"Nodes MMM And NNN Are Shorted"**

   The node numbers show the relative positions of the nodes in the input node list.

   Exception: Ground and V_{DD} show as *GND* and V_{DD}.

2. **"Node NNN Is Open"**

   Not all of the pins in the node are tied together.

3. **"Pin at SXXX.XX, SYYY.YY In Node NNN Is Unconnected"**

   . The pin is not touched by a metal or tunnel polygon.

4. **"Spacing Violation Between (A) MMMMMMMM And (B) NNNNNNNN On Level X"**

   The two rectangles (A) and (B) are too close. The rectangle coordinates are given in two following messages. "MMMMMMMM" and "NNNNNNNN" identify the types of rectangles involved as follows:

   UNUSED PIN, PIN, CELL OUTLINE,
   TUNNEL END, SHAPE SET, POLY RECTANGLE
   or METAL RECTANGLE

   . *Level X* defines the mask level involved.

5. **"The LLLLLLL Rectangle's Diagonal Is: SXXX.XX, SYY.YY-SXXX.XX,SYYY.YY"**

   The message always appears in conjunction with, and immediately following, another message. LLLLLLL identifies the type of rectangle in question. The coordinates identify the corner of the rectangle closest to the chip origin and the corner furthest from the origin.

6. **"Pin At SXXX.XX, SYYY.YY In Node MMM Is Shorted To Pin At SXXX.XX, SYYY.YY In Node NNN"**

   Two pins are located too closely together, probably due to misplacement of a component (pattern, cell).

memory. The amount of memory required to run the program varies according to the complexity and density of the chip. To date, all of the chips run through the program have required less than 500,000 bytes of memory.

Representative program execution times are given below for the Univac Series 70/55 computer. The 70/55 is a relatively slow computer having a register-to-memory fixed-point add-time of 2.5 microseconds. In Table IV, the column labeled *Number of artwork records* denotes the number of records on the output tape from the MP2D program. It indicates the density and complexity of the chip.

If a cost for computer time on a 70/55 computer is estimated at $200 an hour then, from the preceding table, the cost of running the TACC program on a chip A is $50. An experienced, senior-level engineer must take approximately seven hours to perform the identical amount of checking. Compared with the present cost of engineering labor, the cost of the TACC program is significantly low.

The execution time in the table is actual elapsed time from the initiation to the termination of program execution. Actual processing time (as opposed to I/O time) constitutes most of the running time.

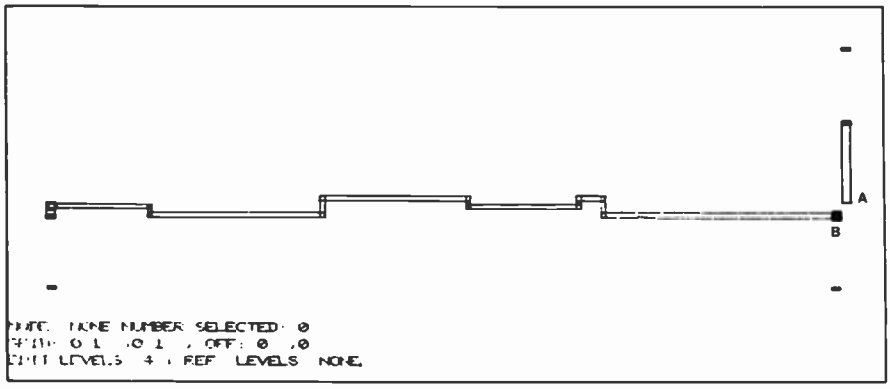
Figure 1 is a checkplot of a chip that was run through the TACC program. This chip uses the SOS cell family and was produced by the MP2D program. The checkplot contains one connectivity error and two topology errors.

Figure 2 shows the printout that was generated by the TACC program. The first group of lines indicates the parameters that were specified to the program, and the second group of lines represents the actual

Fig. 1. Checkplot of chip containing topology and connectivity errors.

```
                                        TACC01
                                TOPOLOGY AND CONNECTIVITY CHECK
                                -------------------------------
DATE:  05/16/78
-------------------------------------------------------------------------------

   THE PROCESS TECHNOLOGY KEY IS 5
   THE SPECIFIED METAL TO METAL SPACING( IN CENTIMILS)= 25
   THE SPECIFIED POLY TO POLY SPACING ( IN CENTIMILS)= 30
   THE SPECIFIED CELL HEIGHT( IN DECIMILS)= 042
   THE LOWEST NUMBER FOR NON-CELL RUN CELLS IS 8000



   NODE 132 IS OPEN.

   SPACING VIOLATION BETWEEN (A) METAL RECTANGLE  AND (B)   CELL OUTLINE   ON LEVEL 6 ..
        THE   "A"   RECTANGLE'S DIAGONAL IS:  014.92, 042.62 -->  015.08, 043.18
        THE   "B"   RECTANGLE'S DIAGONAL IS:  016.08, 042.63 -->  025.92, 040.17

   SPACING VIOLATION BETWEEN (A) METAL RECTANGLE  AND (B)   CELL OUTLINE   ON LEVEL 6 ..
        THE   "A"   RECTANGLE'S DIAGONAL IS:  015.52, 042.02 -->  016.08, 043.18
        THE   "B"   RECTANGLE'S DIAGONAL IS:  016.08, 042.03 -->  025.92, 040.17

   END OF SURVEY FOR:   APAR REMBASS TCC132 CHIP
```

Fig. 2. Program printout.



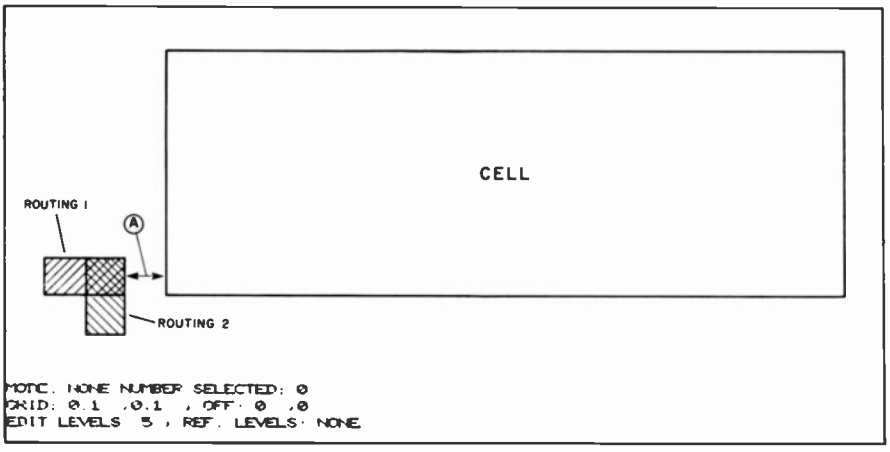


Fig. 4. Topology errors. The width of space A is less than the minimum allowable 0.25 mil metal-to-metal spacing.

error messages. In this example, node 132 was open-circuited. The program detected this error and generated a picture on the Applicon of all of the segments of node 132 (Fig. 3).

In this chip design, two segments of routing on mask level 6 are too close to one of the cells. The minimum metal-to-metal spacing was specified as 0.25 mil (25 centimils). The program detected and printed out these errors. Figure 4 shows the graphic representation of these errors.

Program algorithm

Overall program organization

The TACC program has four major program routines (Fig. 5):

- Input parameter processing routine;
- Main topology and connectivity processing routine;
- SOS connectivity determination routine; and
- C^2L connectivity determination routine.

The input parameter processing routine is the program routine in which execution of the TACC program begins. In this routine, various required and optional parameter cards are read in. Based upon the parameter values read in, various control parameters are initialized for ultimate use by the three other major program routines. Following this initialization, control is passed along to the main topology and connectivity processing routine.

The main functions of the main topology and connectivity processing routine are:

- Read in and process the various required card decks.
- Read in and process the artwork instruction tape.
- Determine the connectivity of the chip and report any errors.
- Determine the topology of the chip and report any spacing errors.
- Control the execution of the SOS and C^2L connectivity determination routines.

The SOS connectivity determination and C^2L connectivity determination routines are similar in function but different in detail. Their function is to assist the main topology and connectivity processing routine in determining the electrical connectivity of the chip design. Their algorithms are based upon the separate sets of rules for establishing connectivity in the SOS and the C^2L technologies.

The main topology and connectivity processing routine prints out all error messages related to the actual chip design, and normal program termination occurs within this module.

Detailed program description

Input Parameter Processing Routine— Execution of the TACC program begins in this routine, which sets up internal control parameters for the entire TACC program. The routine initially reads in a value (from cards) for the process technology key and, based on this value, initializes various internal control parameters.

Some internal control parameters can be specified by the user. The routine also prints out messages that denote the parameters that have been specified by the

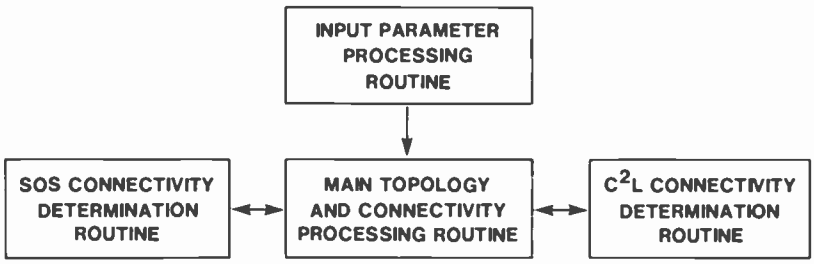


Fig. 5. Major program modules of the TACC program (arrows indicate flow of program control).

user and the specified values. Next, control is passed to the main topology and connectivity processing routine.

Main Topology and Connectivity Processing Routine — This routine begins by reading the remaining cards in the input card file: the pin data file cards, the element-to-pattern assignment cards and the net list cards. From the pin data file cards, the routine builds a pin data file list in memory, with one entry for each pin data file card. From the element-to-pattern assignment cards, the program builds an element-pattern list in memory, with one entry for each assignment on the cards. From the net list cards, the program builds a node list in memory, with one entry for each pin in the net list.

Upon reading the end-of-file on the card reader file, the program sorts the various lists for later processing. It then reads the component records (which specify instances of standard cells in the chip design) from the artwork instruction tape, and builds an entry in the core pattern list for each record. Next, the program reads the rest of the tape records and builds a record in the core rectangle list for each rectangular shape, and for each orthogonal line. The rectangular shapes and orthoganal lines are used to specify the interconnection paths between the standard cells.

Upon reaching the end of the artwork instruction tape, the program builds one or two rectangle list entries for each pin in the node list. If the pin exists on both sides of a cell, then the program builds two rectangle list entries. Otherwise, it builds only one rectangle list entry. If two rectangle list entries are built, these two entries are called "sister pins," and whatever processing is performed on one of the sister pins must also be performed on the other sister pin. Each sister-pin pair is assigned a unique number that is part of the rectangle list entry.

Since I/O pad pins are not defined (physically) as rigorously as pins in other cells, the preceding process is not perfectly accurate for I/O pad pins. Therefore, through the use of a table built into the program, an attempt is made to find the pattern's actual pin descriptions for any I/O pad. If the pattern is not represented in the table, then the program builds the pin's rectangle record in the same way used for other patterns. Note also that unused pins (since they do not appear in the node list) are not processed at this point. The rectangle list is now sorted on lower-left-hand X-coordinate, lower-left-hand Y-coordinate, and upper-right-hand Y-coordinate.

At this point, the rectangle list is sifted through for intersecting rectangles. Eventually, a group of disjoint trees evolves, each consisting of at least one rectangle. As a matter fact, N rectangle trees are initially used, where N is the number of rectangles in the rectangle list. Each of these trees is numbered J, where J is the index (position) of the rectangle in the rectangle list. The relationships between rectangle index and tree number are recorded in the tree list. Each time the program finds a pair of intersecting rectangles, it picks their tree numbers out of the tree list. If the tree numbers are unequal, it searches the tree list for each occurrence of the higher tree number of the two. Each such occurrence is replaced with the lower tree number. At the end of rectangle intersection processing, the tree number of any given string (tree) of rectangles will be the index of the rectangle that appears closest to the front end of the rectangle list.

An intersection of two rectangles is considered significant if, on the actual chip, such an intersection would provide a path that a signal could traverse. Not all rectangle intersections are important — it depends on the technology involved. Whenever the main topology and connectivity processing routine finds a pair of intersecting rectangles, it transfers control to either the SOS connectivity determination routine or the C^2L connectivity determination routine. The SOS connectivity determination routine or the C^2L connectivity determination routine determines the important intersections.

SOS Connectivity Determination Routine — Table V lists some of the rectangle intersections that are significant for the SOS technology and that are the basis of the algorithm for this routine. Each time this routine receives control, it determines whether the two intersecting rectangles match any of the significant rectangle intersections listed in Table V. If the intersection is found to be significant, then the tree list is updated. Pin-to-pin intersections are errors and cause an error message. Any time a pin rectangle is part of a significant intersection, the routine flags both that pin rectangle record and its sister pin rectangle record (if one exists) as connected.

C^2L Connectivity Determination Routine — Table VI lists some of the rectangle intersections that are significant for the C^2L technology and that are the basis of the algorithm for this routine. Each time this routine receives control, it determines whether the two intersecting rectangles match any of the significant rectangle intersections listed in Table VI. If the intersection is determined to be significant, then the tree list is updated. Pin-to-pin intersections are errors and cause an error message. Any time a pin rectangle is part of a significant intersection, the routine flags both that pin rectangle record and its sister pin rectangle record (if one exists) as connected.

Main Topology and Connectivity Determination Routine — After the routine checks all possible rectangle intersections, it attempts to assign one or more node numbers to each tree. The computer looks at each rectangle record in a tree and picks node numbers out of those that are pin rectangles. The results of this process appear in the tree-node list. If no pin rectangle is found in a given tree, then

Table IV. TACC program execution times.

Chip identification	Number of artwork records	Execution time (min.)	Computer charge ($)
A	6037	15	50
B	14435	64	204

Table V. Sample significant rectangle intersections for SOS.

No.	Type of intersection
1	Poly routing with pin on a cell
2	Poly part of tunnel end with pin on a cell
3	Pin on a cell with pin on a cell
4	Pin on an I/O pad with pin on a cell
5	Metal routing with metal routing
6	Metal part of tunnel end with metal routing
7	Pin on an I/O pad with metal routing

Table VI. Sample significant rectangle intersections for C^2L.

No.	Type of intersection
1	Metal routing with pin on a cell or I/O pad
2	Metal part of tunnel end with pin on a cell or I/O pad
3	Pin on a cell or I/O pad with pin on a cell or I/O pad
4	Metal routing with metal routing
5	Metal part of tunnel end with metal routing

the program builds an entry in the tree-node list with the tree number and a node number of 0. If more than one node number is found for a tree, then the program builds multiple tree-node list entries for that tree.

Next, the program sorts the tree-node list by tree number, then node number. It compresses the list to get rid of any redundant entries. It finds short-circuited nodes by identifying adjacent tree-node list entries whose tree numbers are equal and whose node numbers are different. The program puts all rectangles in the shorted nodes on level 1 of the DFL output tape.

After re-sorting the tree-node list on node number, the routine looks at adjacent entries again, reporting those whose node numbers are equal but whose tree numbers are different as open nodes. It puts these rectangles on level 4 of the DFL output tape.

The connectivity processing portion of the routine is now done. In preparation for the topology processing (spacing check) portion of the routine, both the tree list and the tree-node list are used to propagate node numbers through trees by marking the rectangle list records. Then the rectangle list is written to a work file.

The topology processing begins with the rectangle records being read in from the work file and new rectangle list records being generated from them. Each new rectangle list record is slightly larger (half of the appropriate spacing parameter minus 1/100 mil) than the original rectangle list record. In this way, the routine can tell if spacing rules have been violated by looking for intersections of rectangles whose node numbers are different. It checks only polysilicon-to-polysilicon and metal-to-metal intersections.

For each entry in the pattern list (i.e., for each cell on the chip), two things happen. First, for each unused pin in a cell (checked against the node list), the program produces a polysilicon-level rectangle (SOS) or a metal-level rectangle (C^2L). Second, it generates outline rectangles on both the polysilicon and metal levels for the body of the cell. Special handling is again required in generating outlines of I/O pads. This is accomplished by using a table built into the program.

Finally, the rectangle list is again sorted (on lower-left-hand X, lower-left-hand Y, and upper-right-hand Y, and the program makes a pass through it, looking at polysilicon-polysilicon and metal-metal intersections. If it finds an intersection and the node numbers of the two rectangles are different, then the computer prints a spacing violation message, and puts the two rectangles on level 5 of the DFL output tape. The program terminates by printing the contents of an optional title card from the input card file.

Conclusions

The TACC program has been very successful since its inclusion into RCA's group of design automation programs. TACC has reduced the costs of checking a chip by reducing the number of persons who manually check the design, and by enabling less-experienced persons to check a design.

Acknowledgment

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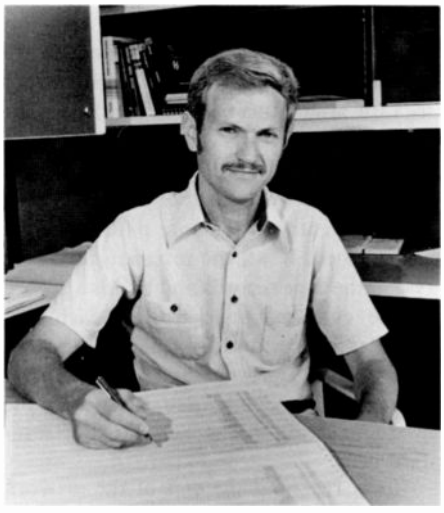

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LSI testing methods and equipment

Design automation has dramatically shortened design development time, so now the focus must be on effectively and rapidly testing the complex LSIs with innovative methods and equipment.

Abstract: *The authors examine methods and equipment needed to test complex LSI devices, and delve into the functional test vectors portion of the electrical test specification, the design-for-testability issue, the SSTC test facility's effort to maintain compatibility with its customers and a review of SSTC's test equipment acquisition plans.*

Introduction

The Solid State Technology Center gives the major operating units of RCA the opportunity to develop and incorporate custom digital LSI devices into their equipments for certain competitive advantages — size, weight, power, cost and reliability. The systems-activity designer typically specifies and designs the LSI device and generates the test specification for the device.

The electrical test specification consists of two basic parts. The first part, the electrical test limits, includes power-supply voltage, load conditions, input/output signal swing, delay and repetition-rate tests. The second part is the functional truth table (test vectors) to be applied to the inputs of device for testing and the equivalent expected output-response truth table. This article addresses the truth-table part of the electrical test specification — the functional test vectors, and how compatibility with the SSTC test facility can be maintained in an environment of rapidly increasing test complexity.

Test program generation

The LSI-array designer is responsible for generating a test program so that his fabricated devices can be tested. Obviously, he wants to define a test program that completely tests every function and device on the array. When semiconductor devices were simple (a few gates or flip-flops) this task was trivial and did not materially affect schedule, array design, cost and so on. But as device complexity increases (logic arrays of 300 - 2000 gates and memory arrays of 1000 - 64,000 bits are currently being designed or used), the efforts required to design test programs increase dramatically. Also, the length of the resultant test vector sequence has grown. Some devices require 100,000 to 1-million test vectors. The far-reaching consequences of such developments are that schedule and cost goals for array development may be missed because of generation complexity, possible difficulties in installing the complex test program on existing SSTC test equipment, or prohibitively long device testing time at wafer probe and final test.

For example, the chart below shows the trade-off between device test time and throughput of the tester for a range of device test times.

Test time vs. volume.

Test Time/Device	*Devices/Month/Shift*
2 sec.	77,500
20 sec.	7,750
5 min.	516
1 hr.	43

Assumptions: 10% probe yield
0.25 time-factor for yield
70% F.T. yield

If the test time exceeds 10-20 seconds there will be a major impact on tester throughput.

RCA's fine complement of design automation (DA) tools has dramatically reduced complex array development time. This time-reduction means that the test-vector-sequence design efforts, if approached improperly, can be the limiting step in a custom design cycle. Let us look at the test sequence generation procedure in some more detail.

Classification — combinatorial or sequential

Combinatorial logic has no internal storage elements (flip-flops, shift registers, counters, or more complex internal logic loops) and the state of the logic is completely and uniquely defined by the state of its inputs. Look-ahead adder-logic, decoders and multiplexers are good examples. Combinatorial logic is simple to test. A complete test of the logic can be done with (2^N) test vectors, where N is the number of logic inputs to the array. This test is complete and may be used to verify that the logic is exactly as specified on the logic diagram, but it contains many tests that are not required for production-LSI testing of verified parts.

As a minimum, the test pattern should include functional verification of each node of the logic, including tests for all gate inputs and outputs stuck at "1" (SA1) and stuck at "0" (SA0). For example, to test a three input AND gate we must test for the output stuck at "0" (SA0), the output SA1, and the inputs SA0 and SA1. To test for the output SA0 requires, in this case, all inputs in the "1" state. This test also detects any input SA0. To test for the output SA1, we can use one of many tests where at least one

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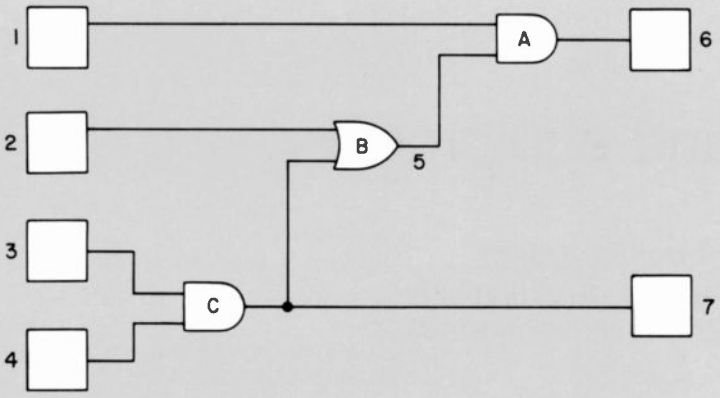

	INPUTS				OUTPUTS		
	4	3	2	1	5	6	7
1	0	0	0	0	0	0	0
2	0	0	0	1	0	0	0
3	0	0	1	0	1	0	0
4	0	0	1	1	1	1	0
5	0	1	0	0	0	0	0
6	0	1	0	1	0	0	0
7	0	1	1	0	1	0	0
8	0	1	1	1	1	1	0
9	1	0	0	0	0	0	0
10	1	0	0	1	0	0	0
11	1	0	1	0	1	0	0
12	1	0	1	1	1	1	0
13	1	1	0	0	1	0	1
14	1	1	0	1	1	1	1
15	1	1	1	0	1	0	1
16	1	1	1	1	1	1	1

GATE	INPUTS	TEST	VECTOR
A	11	SA0	14
A	01	SA1	10
A	10	SA1	3
B	00	SA1	10
B	01	SA0	14
B	10	SA0	8
C	11	SA0	14
C	01	SA1	10
C	10	SA1	8

Fig. 1. The simple logic structure is shown (above), together with a 16-states truth table (bottom left) as well as tests for SA1 and SA0 faults (bottom right).

input is in the "0" state. A test for inputs SA1 requires that the tested input be in the "0" state, and all other inputs be in the "1" state. In this case, then, three tests are required to detect inputs SA1 and output SA1: 011, 101, 110, and the state 111 completes the stuck-at test sequence. Therefore we need to use $N+1$ inputs to test an N-input gate. Observability is an additional requirement. For each of the tests described, we must have a way to monitor the output state of the device. If the gate is buried inside a complex logic network, paths must be sensitized so that the gate's response can be monitored at the output pins of the device.

Consider the simple logic structure shown in Fig. 1. The circuit has four inputs, three logic gates and two outputs. The figure shows a complete exercising of all combinations of inputs (16-states truth table) as well as the set of four states that tests all gates for SA1 and SA0 faults, with all tests observable at the outputs (test vectors 3, 8, 10, 14).

Software programs can automatically generate test programs for combinatorial logic. TESTGEN can examine logic to determine percent of SA1 and SA0 coverage in a supplied test program.

Sequential logic contains storage elements internal to the array (flip-flops, counters, shift registers) and the exact state of the logic depends on the current state of the inputs to the array, and on the past history of those inputs (the number of times a clock line has been activated, and so on). In theory, we can exhaustively test a sequential logic device by applying 2^{N+M} test vectors, where N equals the number of inputs and M equals the number of internal storage states. Obviously, for arrays currently being developed with, for example, 30 inputs and 70 internal storage states, $2^{N+M} = 2^{30+70} \cong 10^{32}$, and the number of test vectors becomes prohibitively large.

We need a way to generate an adequate but minimum set of test vectors. This compromise involves a complex set of trade-offs. In the past, designers have approached this problem from one of several ways. First, they have used simple functional verification. The concept is one whereby the designer, being intimately familiar with his design and the intended use in the system, generates a sequence of input patterns that puts the logic through its intended paces and generates outputs required for systems-use. These test patterns may come from logic simulation that is done to verify that the logic has been properly designed. Such patterns may use tester memory space inefficiently and they often do not check for undesirable modes of operation or possible logic failure mechanisms.

A more rigorous method of generating test patterns is to configure them from a fault-coverage point of view. As mentioned previously, we can use TESTGEN to analyze test programs for coverage of nodal testing. Once a test program with adequate coverage has been generated, minimization techniques may be used to reduce the number of test vectors to fit into practical test equipment requirements and keep production-test costs low. One powerful way to minimize test-pattern requirements for a given logic function is to design testability features into the logic. Often, at the expense of a pin or two plus a few gates, we can substantially reduce the test pattern length.

It is imperative that the designer consider test requirements early in the design phase. Test requirements may well affect the partitioning of the logic and definitely have to be resolved before the logic is firmed. Initialization must be considered. The logic should be able to be initialized with a small set of test vectors. Schemes for accomplishing this requirement include designing master resets for all counters and registers, partitioning long counters into sections for test purposes and adding control elements to break up large sequential networks during initialization. Also, it is sometimes possible to isolate sections of the logic so that the sections can be tested simultaneously. This technique is specially useful for highly sequential logic structures.

The chart[1] shown in Fig. 2 puts into perspective the economic implications of the investment in testability. This investment includes development efforts and usually requires additional gates and pins that affect manufacturing costs. This total investment is shown to increase linearly and is the investment in testability. The reward for this investment is a substantial reduction in initial testing cost followed by decreasing gain. The total cost therefore has a minimum and any further investment in testability will not result in proportionate testing savings.

What is the future of design for testability? Clearly, a larger investment will be made in this area. Some microprocessor-based chip designs already include a self-test capability[2] and this feature will show up with increasing frequency. Another self-test technique called signature analysis[3] is appearing in some of the more complex logic devices. In this approach the addition of a test register and small amount of logic allows the chip to

sequence through a complex test sequence using a pseudo-random-like test sequence. At the conclusion of the test, results are automatically compared with the correct result for a 100-percent functional device.

A third approach is the serial-scan technique.[4] Here, all master-slave register elements, counters and shift registers are connected in serial fashion via special test connections on the array. Means are provided for loading all of these elements via external data and clock inputs. This approach requires from 5-to-20-percent additional logic, and several pins. This serial-scan technique, however, reduces the test pattern generation problem to the task of serially loading and unloading the register string and running combinatorial tests on the balance of the logic in-between. Therefore, all logic structures can be reduced to the equivalent of testing combinatorial logic, a straightforward problem that can be solved with computer algorithms.

Which of these techniques is going to succeed? Which will fade away with time? The answers are not clear. Perhaps all three techniques will be used to some degree. What is clear, however, is that some form of design for testability is required for future LSI devices.

Interfacing with SSTC

With the testability problem being so interactively related to the array design, how does a design activity interface with SSTC to provide an efficient transfer of test requirements that will allow quick turnaround sampling of design verification parts?

Logic simulation is the key to solving this problem. The MIMIC logic simulator should be used as a design tool to verify basic logic function. For more information on SSTC's new logic simulator, MIMIC, contact Aaron Ashkinazy or Henry Hellman at SSTC in Somerville, New Jersey. SSTC will supply delay versus fan-out tables for logic cells used in both universal array and automatic placement and routing (APAR) design approaches. These tables will allow the designer to analyze and optimize his design from a delay and timing point of view. This effort will lead to a verified logic design that will operate over required environmental ranges and process variations and will provide adequate margins.

The simulator effort will also provide a set of test vectors (inputs and expected outputs) in standard format (TESTGEN) that can be used to test the device.

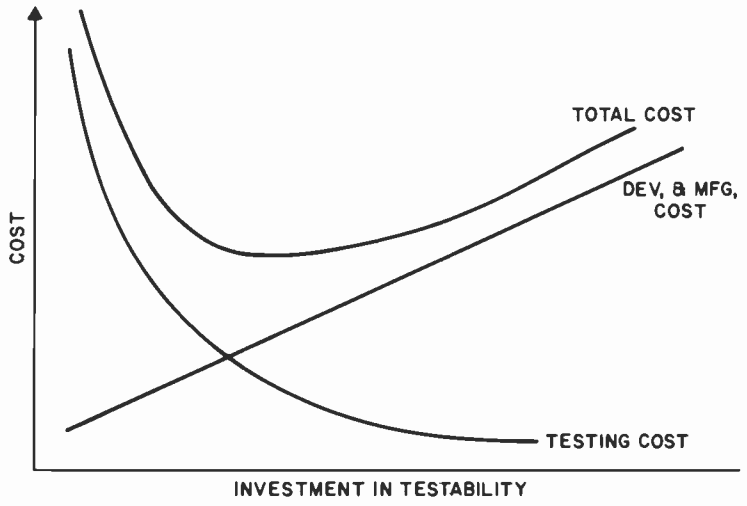

Fig. 2. Economic implications of investment in testability.

The design review—a critical step in array design

An essential part of the design review prior to release to SSTC is the review of the test package for adequacy of test and for compatibility with existing test facilities.

Where the application has been defined as a universal array, SSTC will digitize the layout and extract the logic connectivity of the layout with software techniques. SSTC will then resimulate the logic with MIMIC to verify capture of the correct function through the layout and digitizing cycle. Work is in progress to enhance this program to include interconnect load capacity as a part of the simulation effort after digitizing. This will allow layout dependent delays to be included in the simulation effort. For APAR designs, the logic is not resimulated at SSTC since there is no manual layout and digitizing cycle. Once proper operation has been verified, SSTC will generate the dedicated test tape (Datatron) from the standard simulation format.

This method of interfacing has been used for over two years and, when followed, has resulted in a smooth transfer of design information and a high probability of first-time success with design verification samples. During this period fifteen universal array designs were handled with seven customers. In almost every case there was some adjustment to the logic or layout made to improve performance margins when resimulated at SSTC. In many cases the customer used a different logic simulator and this caused some difficulty in translating between simulators. Of these fifteen designs, fourteen worked the first time into device fabrication, giving excellent proof of the value of simulation in verifying the design and test program.

Test equipment

The Solid State Technology Center's present test equipment consists of two medium speed (50-kHz) systems, the Datatron 44 and 4400 functional and parametric testers used for design verification and production testing of LSI arrays, a high-speed (10-MHz) Datatron 45 functional tester used for device characterization, and a low-speed Keithley LPT-2 parametric tester used for wafer acceptance testing. Table I summarizes the characteristics of these testers.

The medium speed Datatrons are parallel parametric and functional testers that measure all input and output terminal parameters simultaneously while applying the functional test vectors. These testers can either force a voltage and measure a current or force a current and measure a voltage. The terminals of the device under test are sampled at the 80-percent point of the data-bit period and the values are compared with the programmed minimum and maximum acceptable limits. Out-of-limit values are detected as bit errors, which are indicated on a display panel or which can be data-logged. The current or voltage value of any device terminal can be monitored on the display panel. During production testing, devices are rejected when the first error is detected.

The high-speed Datatron 45 is a functional tester that can supply bursts of functional test vectors, up to one kilobit in length, at a 10-MHz data rate. The outputs can be sampled at any point in the bit period with a 10-nanosecond strobe width. The tester can measure rise and fall times, pulse widths and propagation delay.

The Keithley LP-2 is a sequential parametric tester that measures the device terminals one at a time. It can apply voltages up to 172 volts and currents up to

Table I. SSTC test systems.

	DATATRON 45	*DATATRON* 44	*DATATRON* 4400	*KEITHLEY LPT-2*
Tester type	High speed functional	Medium speed functional and parametric	Medium speed functional and parametric	Parametric
Maximum repetition rate	10 MHz	50 KHz	50 KHz	100 Hz
I/O pins	96 pins	100 pins	50 pins	58 pins (includes 8 low level pins)
Test stations	1 package test	1 package test 1 wafer probe	1 package test 2 wafer probe	2 wafer probe
Maximum voltage	30 volts	30 volts	30 volts	172 volts
Slew rate	1 v/ns	20 v/μsec	20 v/μsec	2 v/μsec
Current measurement accuracy	—	±1 nA	±200 nA	±1 pA
Voltage measurement accuracy	±50 mv	±50 mv	±50 mv	±1 μv
Rise and fall time measurement accuracy	±3 ns	—	—	—
Propagation delay measurement accuracy	±5 ns	—	—	—
Pulse width measurement accuracy	±5 ns	—	—	—

100 ma. It has measurement accuracies of ±1 pA and ±1μV.

The present SSTC test equipment for functional testing is limited to a maximum of 100 test terminals for the Datatron 44 and 50 test terminals for the Datatron 4400. Both systems are limited to a maximum data rate of 50 KHz. The maximum functional truth-table length for this equipment is limited by the tester in increments of 16 pins. Table II shows this limitation. Longer test patterns can be generated by using groups of truth tables with clocking and jumps between truth tables.

Test programs are generated on the Datatron equipment using the following steps.

1. Generate a Value Table that contains, line-by-line, all of the desired voltage forcing values (normally, inputs V_{IH}, V_{IL} and power supplies V_{DD}, V_{SS}) for a logical "1" and "0" with corresponding acceptable maximum and minimum current values (I_H max., I_H min., I_L max., I_L min.) and all of the current forcing values (normally outputs I_{OH}, I_{OL}) for a logical "1" and "0" with the corresponding acceptable maximum and minimum voltage (V_H max., V_H min., V_L max., V_L min.).
2. Generate a set of pin tables where each table assigns a value from the Value Table to each pin.
3. Load a set of Truth Tables that assign a logical "1" or "0" or "don't care" to each pin.
4. Assign leading edge and trailing edge timing to desired pins.
5. Generate an instruction table that combines the above steps with desired clocking and jump routines, and binning of test results to perform in sequence all of the tests desired.

Table II. Truth table length.

Maximum No. of Pins	*Maximum Length (masked with "don't cares")*
16	10,000
32	5,000
48	3,333
64	2,500
80	2,000
96	1,666
100	1,428

A typical test program would perform the following tests:

- Contact test;
- Terminal leakage test;
- Functional test at nominal voltage;
- Functional test at maximum voltage with input noise and output loads;
- Functional test at minimum voltage with input noise and output loads;
- V_{DD} or V_{SS} leakage tests.

Future test equipment requirements

The high speed Datatron 45 can operate at a data rate of 10 MHz with a maximum of 96 test terminals, but at the time of this writing, the high-speed tester shares peripheral equipment with the Datatron 44, and the two systems can be used only one at a time. Present plans call for the separation of the Datatron 44 and 45 in order to provide a stand-alone 10-MHz Datatron 45 in the third quarter of 1980. Additionally, an off-line system used for the generation of Datatron test programs and data reduction has been recently added to the SSTC test equipment.

The advent of newer, more complex LSI arrays with high input/output pin count and higher operating speed requires the aquisition of newer and more advanced test equipment for SSTC.

High-speed testing is required not only for testing devices at their specified maximum test frequency but also to minimize the total time required to test wafers and packaged devices containing complex arrays with long test programs in a pilot production test environment.

The SSTC Test Technology Activity performs a dual role. It operates in an engineering mode when providing test debugging and design verification for new LSI arrays in development and, secondly, it operates in a production mode when providing testing for previously designed

arrays while they are in pilot production. Each year, the activity typically verifies the design of 60 new arrays and provides wafer and packaged-device testing for more than 50,000 commercial and Hi-Rel screened devices consisting of over 200 array types.

Many of these devices provide RCA major operating business units with competitive advantages, new capabilities and new markets. For example, SSTC-processed devices are used in the Van Nuys weather radars, GCS TENLEY/SEELEY secure communications systems and Survival Avionics System, broadcast TV cameras, Meadowlands TAC TEC radios, MSR AEGIS and Sandia systems, ASD GVS-5 laser rangefinders, AED satellite computers, ATL ATMAC microprocessors, fault-tolerant computers, advanced autonomous arrays and numerous other development programs, SSD microprocessors, memories and other custom devices and in many other applications.

The SSTC Test Technology operation participates in the following activities:

- Wafer testing of bulk-silicon and SOS arrays and memory devices for SSTC engineering, RCA major operating units and other customers;
- Wafer testing of bulk-silicon and SOS custom arrays and memory devices to obtain prototype quantities and establish the producibility and yield levels of products planned for production in the Solid State Division;
- Final testing of commercial and Hi-Rel packaged devices;
- Supporting engineering in the design verification and array debugging;
- Characterizing and evaluating arrays to determine design margin, sensitivities, process stability, and related testing requirements for SSTC and its customers;
- Supporting reliability and quality engineering by testing devices for process monitoring, reliability verifications, and device qualification programs;
- Providing input to Design Engineering on matters pertaining to designing devices for testability as they relate to existing methods and equipment used for test; and
- Interacting with tester companies and other RCA organizations on test-related matters and testing technology. The efforts to keep pace with the changing technology should be incorporated into the Technical Center operation in an organized and timely manner.

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Authors Tom Mayhew (left) and Richard Bergman (right).

Table III. Forecast of VLSI requirements.

	Year		
	1980	1982	1985
Maximum number of pins	84	120	250
Maximum frequency (MHz)	10	20	50
Maximum voltage	15	15	15
% Digital circuits	100	90	90
% Digital/analog circuits	0	10	10
A-D converters			
Number of bits	10	10-12	12 or 8
Maximum sample rate (MB)	2	2	5 or 20
Memory			
Number of bits	4K	16K	64K
Organization	1K x 1	4K x 4	16K x 4
(Words x bits per word)	4K x 1	16K x 1	8K x 8
Access time (ns)	100	50	20
Cycle time (ns)	150	100	100
Design for testability	Develop	Essential on chip provision	Standardized self test and error correction

A forecast of device configurations and complexity for very large scale integrated circuits has been made based on inputs from SSTC and GSD personnel. These include requirements for Advanced-AEGIS, Banville, VHSIC, SEELEY, GVS-5, JPL, Sandia, AVS-Weather Radar, Thornton, Manufacturing Methods programs with WPAFB, Fault-Tolerant Computer and others. The following test requirements (Table III) are anticipated for 1980 through 1985.

SSTC is presently considering the aquisition of a new high-speed high-pin-count tester in 1981. The leading contender for this equipment is the Fairchild Sentry Series 22 test system with 120 input/output pins and a 20-MHz functional test data rate. This equipment will be software compatible with test programs used on the Solid State Division Fairchild Sentry VII 10-MHz test equipment and will aid in the smooth transfer of newly designed arrays into production in SSD.

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G. Skorup

The gate-universal-array for digital CMOS

Since the first application of the CMOS universal array was begun in 1973, seventy-two new gate-universal-arrays (GUA) have been implemented in commercial and military systems.

Abstract: *The author reviews the applications for and theory behind the CMOS gate-universal-array (GUA). He shows that both commercial and military logic systems from a variety of RCA divisions use the GUA; he shows the various approaches to a flexible design process allowed by the concept; and he shows how GUA advantages make this a cost-effective, quick and efficient way to make logic systems.*

A gate-universal-array (GUA) consists of a fixed placement of *p* devices, *n* devices and tunnels in a repetitive, ordered structure on a silicon or sapphire substrate. All device nodes (gates, drains, sources and tunnel ends) are accessible for logical interconnect. All the mask definition levels, except the metal mask, are fixed. The metal definition mask uniquely defines the device interconnect metal for each application.

Figure 1 shows a typical SOS gate-universal-array layout. The interior area consists of internal cells of *p* and *n* devices that are intended for most of the logic circuitry. The peripheral areas contain larger devices for use as input or output buffers. Bond pads, of course, are located on the periphery of the chip. Two rings surrounding the internal cells distribute the power.

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The GUA technique provides the following attractive features:

- Quick turnaround
- Cost-effectiveness for small-volume applications
- High reliability
- Excellent probability of initial success
- Rapid implementation of design changes
- All the usual advantages of complementary metal-oxide semiconductors (CMOS)

During the past ten years GUA design techniques have improved significantly. In particular, we can implement a design with a high probability of success on the initial effort. For example, 14 of the last 15 GUA designs completed "worked right the first time." Additionally, as a result of the one problem-causing design, simulation techniques have been refined to avoid future problems.

The GUA has been used extensively for both commercial and military applications. Commercially, it has been used in such applications as airborne radar, heart pacers, watches, TV cameras and communications control. Military applications have included space computers, missiles and rangefinders. Many LSI circuits have been delivered for laboratory development and prototype evaluation.

Importance to RCA

The first application of the CMOS universal array was begun in 1973. It used the 168-gate member of the metal-gate family. Since then, 72 GUAs have been implemented. They are listed by RCA location in Table I. Of these, 37 are currently active in that they are either in continuing production or are being developed. GUA applications have been implemented in all three technologies. Table II gives a breakdown by technology. Currently, the SOS GUAs account for most of the newer applications because of their superior performance.

Table I. CMOS GUA applications summary.

RCA Location	*Number of GUA Types*
Somerville (SSD)	42
Van Nuys (AVS)	9
Camden (GCS)	3
Burlington (AS)	4
Lancaster (PTD)	4
Hightstown (AE)	4
Meadowlands (MCS)	1
Moorestown (MSR)	1
Princeton (Labs)	4
Total	72

Table II. GUA applications by technology.

Metal Gate	30
C^2L	15
SOS	27

Several million dollars worth of GUA ICs have been delivered to the Solid State Technology Center (SSTC) and the Solid State Division (SSD) customers during the last two years. Table III gives areas of application. GUAs are used in commercial and military products. Every RCA broadcast-TV camera, both studio and remote units, contains a universal TV sync generator that is compatible with a variety of TV system broadcast standards. It is a unique proprietary design, and provides RCA with a performance/cost/size advantage over the competition. Figure 2 is a photograph of the TK-76C broadcast quality color TV camera.

RCA Avionics Systems at Van Nuys, California, uses several GUAs in their PRIMUS color weather radar. Commercial aviation uses this product to observe unfavorable weather patterns and thereby avoid them. The GUA's ability to provide low power, compact size and reduced cost together with additional performance features has contributed to the success of the weather radar product line.

The GVS-5 Hand-Held Laser Rangefinder is a versatile product being manufactured by RCA Burlington. The unit is shown in Fig. 3. Artillery and infantry forward observers can use the

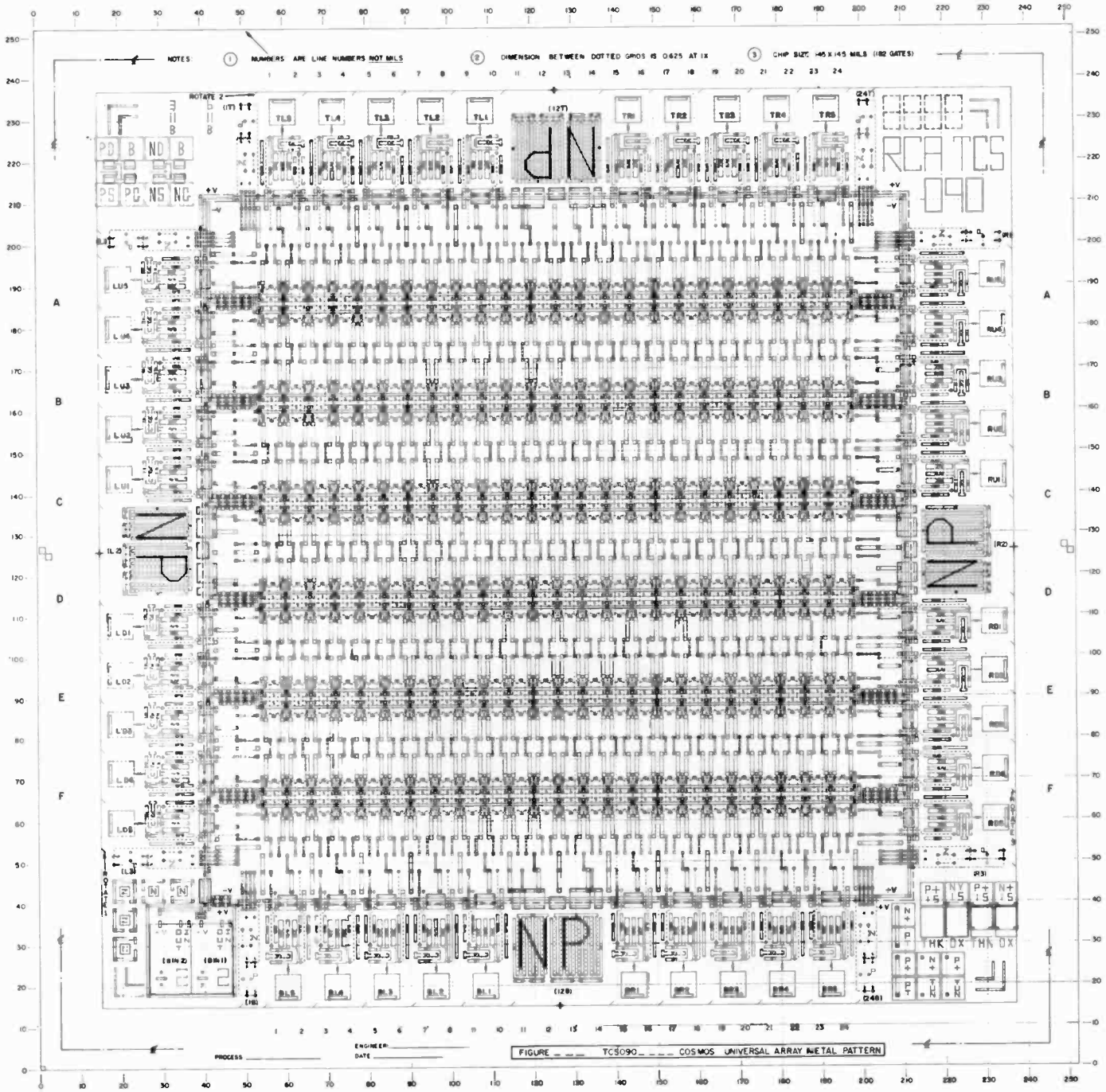

Fig. 1. A typical SOS gate-universal-array layout.

Table III. Significant applications.

Application	*RCA Business*
Broadcast Color TV Camera	GCS
CCD Closed-Circuit TV Cameras	PTD
Classified Military Application	SSD
Global Positioning System	MSR
Laser Rangefinder	AS
Military Computer (Navy)	SSD
Missile Fuze Timer	SSD
NASA Space Computer	SSD
PRIMUS Color Weather Radars	AVS
Standard Space Computer	AE
Stinger Missile	SSD
Telephone Station Circuit	SSD
Vidicon Closed-Circuit TV Cameras	PTD
Weather-Scout Weather Radars	AVS

laser rangefinder. The operator aims and fires an invisible laser beam at the target. Then the beam's round trip travel time is measured, converted to target range, and "instantaneously" displayed in the rangefinder eyepiece. RCA Burlington is now developing an improved version of this binocular-sized unit that will pinpoint targets up to 10,000 meters away with 5-meter resolution. The SOS UA in the improved unit operates at 30 MHz.

Revenue from the sale of GUA devices during the next five years, from programs now under development, is projected to be several million dollars per year.

Present GUA design vehicles

GUA types

Digital CMOS logic designs are now implementable in the metal-gate (MG), closed-cell logic (C^2L) and silicon-on-sapphire (SOS) processes. The metal-gate CMOS, sometimes referred to as the "bulk process" or bulk CMOS, uses metal gates on *p* and *n* devices that are diffused into a silicon substrate. The C^2L process uses donut-shaped *p* and *n* devices diffused into a silicon substrate, but uses polycrystalline-silicon for the gate material rather than metal. Silicon-on-sapphire (SOS) contains silicon gates on *p* and *n* silicon islands that are formed on a sapphire substrate. Since sapphire is an insulator, the *p* and *n* devices are electrically isolated from each other.

Table IV lists the types of GUA design vehicles now available.

Because of their greater complexity, the C^2L and SOS GUAs are being used in most new applications. But metal-gate technology has the greatest maturity and reliability history, so bulk CMOS is still being usefully applied. Design turnaround time from layout to working parts for GUA applications has been as short as six weeks, but more typically approaches eighteen weeks, and depends upon the design's complexity, the accuracy of customer-supplied information and the scheduling requirements.

Customer interfacing

Customers submit a logic design to the SSTC at any of the three levels noted below.

Level I — General Logic

The customer supplies: (1) a general logic diagram that has been simulated by RCA's MIMIC (or other acceptable equivalent) software simulation program; (2) a MIMIC-verified test pattern; and (3) other necessary specifications. The SSTC delivers packaged units that have been tested to the supplied test pattern and other standard or agreed-upon specifications.

Level II — Annotated Logic

The customer supplies: (1) a logic diagram annotated in GUA logic cells (as defined in the *CMOS Universal Array* (UA) *User's Manual*)* that has been simulated by the MIMIC software program; (2) a MIMIC verified test pattern; and (3) other necessary specifications. The SSTC delivers ten packaged units that have been tested to the supplied test pattern and other standard or agreed-upon specifications.

Level III — Layout

The customer supplies all the information of Level II, plus a layout of the logic on the 125 x Mylar sheets (copies of the GUA format of Fig. 1 at 125 times actual chip size) provided. The MIMIC-verified test pattern must be of the logic from which the layout was made.

Interfacing at Level I or II is recommended when implementing only one or two designs. If the customer

* Two universal array user's manuals are now available. For metal gate and C^2L applications the *COS/MOS Universal Array User's Manual* is to be used. The *SOS COS/MOS Universal Array User's Manual* is available for SOS applications.

Fig. 2. TK-76C broadcast quality color TV camera.

Fig. 3. GVS-5 hand-held laser rangefinder.

Table IV. Universal-gate-array types.

Technology	*Type*	*Array Size (Mils)*	*Internal *Gates*	*Total *Gates*	*Total Pads*
Metal-Gate CMOS (MG COS/MOS)	TCC 040	189 x 188	138	168	40
	TCC 051	229 x 232	240	276	48
Silicon-Gate CMOS (C^2L COS/MOS)	TCC 220	156 x 155	138	168	40
	TCC 221	186 x 188	240	276	48
	TCC 222	216 x 220	370	410	48
	TCC 223	245 x 252	528	576	64
Silicon-Gate CMOS (SOS COS/MOS)	TCS 090	150 x 150	144	182	40
	TCS 091	180 x 180	256	300	48
	TCS 092	210 x 210	400	452	64
	TCS 093	240 x 240	576	632	64
	TCS 094	270 x 270	784	848	80

* A gate consists of two *p* and two *n* devices and is the equivalent of a two-input NAND or NOR gate.

Table V. Technology comparison at room temperature and 10-volt operation.

Attribute	*MG*	*C^2L*	*SOS*
Specification	Mil/Com	Mil/Com	Mil/Com
Maximum Binary with reset (1)	10 MHz	20 MHz	40 MHz
Average Pair Delay (2)	16ns	8ns	4ns
Mask Compatibility (3)	yes	yes	no
Voltage Range	1.1 - 20	3 - 12	4 - 11
Power Dissipation	low	low	10w
Gate Complexity	168- 276	168 - 576	182 - 848
Number of Pads	40 - 48	40 - 64	40 - 80

anticipates several GUA designs and wants to minimize his cost, he may use the Level III interface. Although the layout procedure is straightforward and described in detail in the *COS/MOS Universal Array User's Manual,* accurate and effective interfacing at Level III requires some training.

Customers who want to interface at Level III can take three to five days and attend a GUA design course given at RCA (several have done this).

Technology selection

We select the technology for any specific application after comparing the application requirements with the attributes of the three technologies available. See Table V for some of the more significant attributes. These general guidelines provide some quantitative feel for the tradeoffs between competing technologies.

1. Metal gate (MG) and C^2L vehicles can operate at somewhat higher frequencies when used without set or reset. The SOS GUA has two custom binary stages which do not have set or reset and will operate up to 100 MHz. These stages are quite useful for pre-scalers, where only the input stage must operate at the highest frequency. The above values are typical and they reflect a realistic comparison of overall speed for combinational (non-clocked) logic as well. In other words, C^2L is twice as fast and SOS is four times as fast as MG CMOS.
2. Average pair delay is the averaged value of inverter, two-high NOR, and four-high NOR gates with a fan-out (each gate is considered a load or fan-out of one) of one and no series tunnel resistance. Actual on-chip delays will be increased by fan-out, series tunnel-resistance and coupling capacities.
3. A metal pattern defined for use on a metal-gate UA may be applied to its C^2L counterpart (and vice versa) without any change in layout. New advances in bulk technology and continued progress is SOS promise increased performance and greater density in both technologies.

GUA procedures

Design

The design cycle begins with the customer creating a logic diagram of the intended system. Logic to be implemented with universal arrays is annotated using the universal-array cell library listed in the *COS/MOS Universal Array User's Manual*. An operator then enters a logic net list of all logic functions and their interconnect into a software file, and the list is exercised by a simulation program for circuit evaluation.

The SSTC has recently developed a software program for logic simulation called MIMIC. This program is compatible with universal-array implementations of LSI digital logic and we have used it effectively for both pre-layout and post-layout circuit performance evaluations.

After verification, the complete logic configuration is partitioned into one or more universal arrays. Array sizes are chosen to achieve the least number of inter-chip connections, as well as to minimize the number of different chips. Where possible, we specify more chips per system, but fewer types. This minimizes the number of chip designs.

Once specific chip logic is defined, the test pattern is generated. In the past, the chip was designed and implemented before the test pattern was generated. This approach can be costly in time and resources. As chips become increasingly complex, the testing aspect becomes paramount because testing is becoming increasingly expensive and it is possible to design a chip that cannot be tested. Tester time should be used primarily for testing chips with proven test patterns, and not for troubleshooting. Troubleshooting needs to be done off-line with software as much as possible.

A chip must be designed for testability. Good design practice includes adding sets or resets to all counter states (for initialization purposes) and sectionalizing long counter chains into shorter ones (for reduced test time).

The test pattern is generated to exercise the logic of the chip's intended use, or it may be generated to exercise all inputs and outputs. In either case, we use the test pattern to exercise the software logic prior to chip implementation. After completion of the software evaluation, the customer will then layout the universal-array chip.

Implementation

The procedures for implementing a GUA design (Fig. 4) presume interfacing with the customer at Level III. Blocks A through E are the inputs received from the customer. These are the input test pattern, the logic diagrams (in UA logic cells), the UA layout (125 x Mylar), the expected output test pattern and other test specifications.

The Mylar layout (C) is a 125X representation of the given universal-array (Fig. 1). The design is implemented by applying logic decals and manually drawing logical interconnections on the layout. This com-

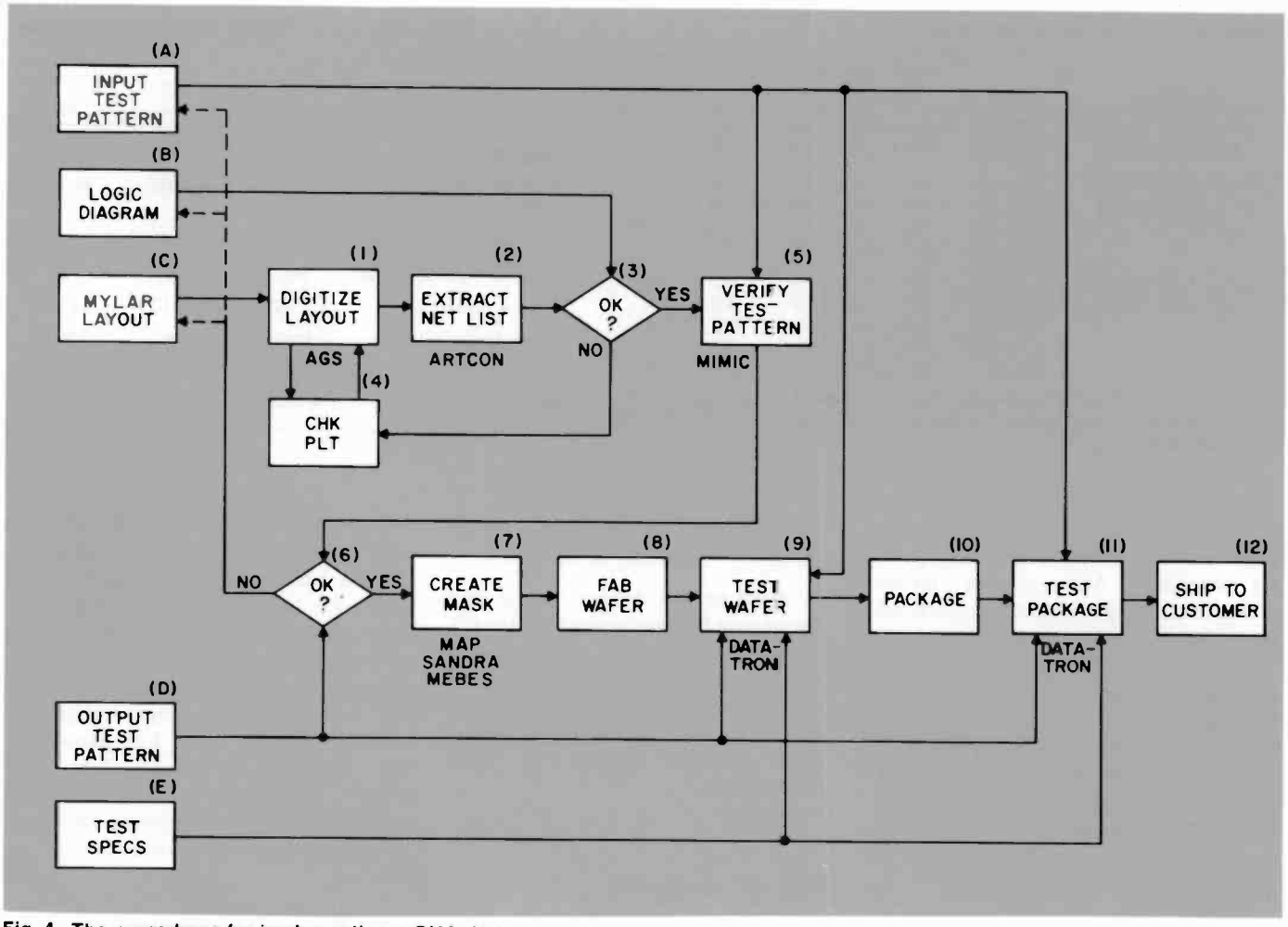

Fig. 4. The procedures for implementing a GUA design.

pletely specifies the custom metal of the design. Using the Applicon Graphic System (AGS), the designer digitizes (1) the layout. This step captures metal pattern geometries into a software file. A computer program (ARTCON) (2), creates a logical net list from the custom metal, device and tunnel-location information. It essentially creates a logic diagram of the actual IC layout and presents it in net-list format. The program compares (3) the ARTCON net list with the customer-supplied logic diagram. Concurrently, a Xynetics plotter creates a checkplot of the digitized information directly from an Applicon-generated magnetic tape. Any discrepancies made obvious by ARTCON are located on the checkplot and corrected. This cycle is repeated until the AGS design file is exactly the same as the logic diagram. With this procedure, one is assured that the logic of the actual chip design is exactly the same as that of the customer-supplied logic.

Subsequently, an operator enters the net list (2) and the customer-supplied input test pattern (A) into MIMIC (5) for test-pattern verification. The MIMIC program will exercise the actual chip logic with the supplied input test patterns.

Any discrepancy between the two output patterns is due to an error in either the input test pattern, the output test pattern, the logic diagram or the mylar layout. The error, wherever found, is corrected and the previous cycles repeated (as required) until compare (6) is correct.

At this juncture, the actual chip design has been tested and verified (by software) before any costly mask-making or wafer-fabrication expense occurs. The engineering phase is complete. All unique aspects of the design are complete. The remaining steps involve repetitive proven processes. This is not to say that mask-making, wafer-fabrication, testing and packaging are trivial operations. On the contrary, they involve sophisticated equipment and complex processing operations. But the procedures described here assure, with high probability, that the finished parts will perform as intended.

A manufacturing electron-beam equipment system (MEBES) makes photographic plates (masks) for wafer fabrication (7). MEBES is driven by a magnetic tape derived from the verified AGS design file. Additional software programs such as MAP and SANDRA are used for this purpose (to create the tape). MOS wafer fabrication (8) requires finished masks. Finished wafers are tested (9), and output test patterns (D) and other test specifications (E) are applied to the Datatron for wafer test. Good pellets are packaged (10) and retested (11) and shipped to the customer.

Future plans

Future GUA development will emphasize the following areas:

- Higher device count and density with a goal of approximately 2000 gates.
- Use of computer-aided placement and routing to reduce layout time and cost.
- Development of design for testing techniques and design vehicles that will reduce test time from an exponential to a linear function of logic complexity.

For years, the GUA has been designed conservatively to ensure ease of manufacture, predictability of performance and high reliability, making it applicable to both military and commercial products. Current improvements in process engineering will allow greater device density, higher gate-count and improved performance without sacrificing a conservative design.

Increasing logic complexity per chip demands that we develop more efficient means for logic placement and interconnect routing. Significant progress has been made. The Advanced Technology Laboratories (ATL) of GSD has progressed significantly toward this goal by developing an automatic placement and routing program for a universal array (AUA). Efforts are being made to apply the results of the ATL program to the development of an operational AUA vehicle.

Again, LSI testing has become the most difficult, time-consuming, and costly aspect of LSI design. The number of required test patterns or vectors increases exponentially with LSI complexity. Device testing is expensive for the component manufacturer, the equipment manufacturer and field service personnel. The IC industry recognizes this problem. Current solutions involve placing the logic at the design level so as to simplify the testing problem. This means using more circuitry for the same logic function, and increasing the chip size for a given design. But we expect that the additional costs of chip fabrication will be more than offset by the savings in initiating and using test patterns. This is especially true for the GUA, where the cost of developing and verifying a test pattern is a large part of the design cost and is amortized over a relatively small volume of product.

Gordon Skorup, Senior Member of the Technical Staff, Solid State Technology Center, joined the Home Instruments Division of RCA in 1946 where he was engaged in the design of both tube and transistor TV receivers until 1960. He then transferred to the Missile and Surface Radar (MSR) division where he had project engineering responsibility for the design and development of prototype optical-correlation equipment for undersea warfare. From 1966 to 1969 he was responsible for all PMOS applications and proposals in the MSR division, during which time he was awarded the Chief Engineers' Technical Excellence Award. Since 1970, as a member of the Monolithics Applications group of Government Communications Systems, and later SSTC, he has been responsible for the design and application of PMOS and CMOS universal arrays. For these efforts, he was recently awarded the Princeton Laboratories Outstanding Achievement Award.

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Conclusions

The gate-universal-array concept is a cost-, time- and resource-effective means for the implementation of both commercial and military logic systems. The concept will continue to assist the RCA divisions in using in-house CMOS LSI technology to compete more effectively in the marketplace.

E.J. Mozzi | C.A. Schmidt

Custom LSI: an effective tool for digital communications equipment design

Why LSI? When LSI? How LSI? Here's what RCA's TENLEY/SEELEY program is doing to answer these applications problems.

Abstract: *Practical, applications-oriented examples from the TENLEY/SEELEY program to develop cost-effective, military, digital communications equipment show how LSI and computer-aided design can actually be used.*

Introduction

A major thrust in military systems is to use complex digital communications equipment. This is economically possible only if modern LSI technology is employed. The TENLEY/SEELEY program is an outstanding example of the development of cost-effective military equipment by the successful application of custom LSI technology. This program proved out a family of LSI design automation and a rigorous LSI design discipline. The results, from concept formulation to equipment field deployment and test, have been outstanding.

The TENLEY/SEELEY program began at RCA in 1972. It was obvious that the equipment performance and complexity could only be realized through the use of LSI. A total of 60 LSI array types were designed and developed, and more than 50,000 arrays have been produced to date. No arrays required redesign due to functional deficiencies. The technology used was bulk CMOS in both custom and standard cell configurations. All cost, delivery and performance commitments were met or exceeded, and a contractual delivery incentive award was earned. Equipment reliability tests fully substantiated the anticipated LSI performance. A total of 1500 equipments of 29 different types were delivered during the R&D phase.

A primary factor in program success was the design methodology employed. Computer-aided design (CAD) played a vital role in design, simulation, layout and testing efforts. Also significant, automatic test equipment and compatible complex test patterns were developed for LSI and printed wiring assembly design verification and failure diagnostics.

A final ingredient to the success of TENLEY/SEELEY was the skill and effectiveness of the Government-contractor team. The program was conducted by RCA's Government Communications Systems (GCS) of Camden, New Jersey. Key support was provided by other RCA units: Advanced Technology Laboratories (ATL) also of Camden, and the Solid State Technology Center (SSTC) and Solid State Division (SSD) both of Somerville, New Jersey. This collective team, bringing to bear a synergism of technology, device, equipment, systems and dedicated design personnel, represents a total design and fabrication capability. Finally, the Government customer served as a full member of the team, providing guidance and direction to all elements of the program, and sharing in the rewards and (few) disappointments.

Why LSI?

In general, the advantages of LSI hinge on those characteristics most important to today's equipments — size, weight, power, reliability and cost. A decision to use LSI must also weigh the practicality — the ability to design LSI devices that will satisfy the particular application within contractual budget and schedule constraints. The design of new LSI devices obviously introduces an element of risk which when recognized and addressed properly can be retired effectively.

In the case of TENLEY/SEELEY, deployment of the equipment would not have been possible without the use of LSI. The functional performance requirements coupled with the size, weight, power and cost constraints dictated a high-logic-density, low-cost, high-reliability technology.

Table I compares the significant design factors of LSI with those of a CMOS SSI/MSI CD4000 implementation. The logic speed, although a strong point for

Table I. Design factors.

Design parameter	*Ratio of CD4000 to LSI*
Area	37.8
Weight	128
Volume	74
Power	25
Life cycle cost	5.8
MTBF (Mean time between failures)	0.048

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Table II. Why LSI?

Design advantages from Table I
• Size and weight
• Cost
• Power
• Reliability
Factors bearing on practicality (design risk factors)
• Design automation availability
• Radiation hardening
• Customer acceptance
• Producibility
• Military environment compatibility

LSI, was not a critical consideration — the specified maximum clock frequency was 1 MHz and maximum data rate was on the order of 64 kHz. Note that LSI offers outstanding advantages in all the factors listed. In developing the ratios shown, the effects on the total equipment design were analyzed, not just the specific components involved. For example, the weight, area and volume take into account the wiring, printed board area, and overall equipment design. Equipment quantities of 150 were used in the analysis for life cycle cost.

Table II highlights the major reasons for using LSI specifically for the TENLEY/SEELEY program. Included are the design factors from Table I, plus certain factors bearing on practicality or design risk. Design automation for design support, and performance verification are two factors that call for special emphasis. A driving force for CAD has been the practical need for LSI. The CAD tools available in RCA and the industry for LSI are incomparably better than during the early years of SSI and MSI development. Radiation hardening for survivability in a tactical nuclear environment was achieved basicallly by the technology selected (bulk CMOS) and the active device size and processing. Enhanced producibility was an inherent result of the reduced assembly labor and component-part count. The ultimate result was meeting the performance requirements in an implementation configuration that was highly acceptable to the customer.

Figure 1 is a typical wirewrap board which was used to breadboard and test the LSI logic prior to committing to a final design. This particular wirewrap board contains 67 CD4000 SSI and MSI devices, which were ultimately replaced by the single LSI chip shown in the figure. The size reduction is impressive, but just as

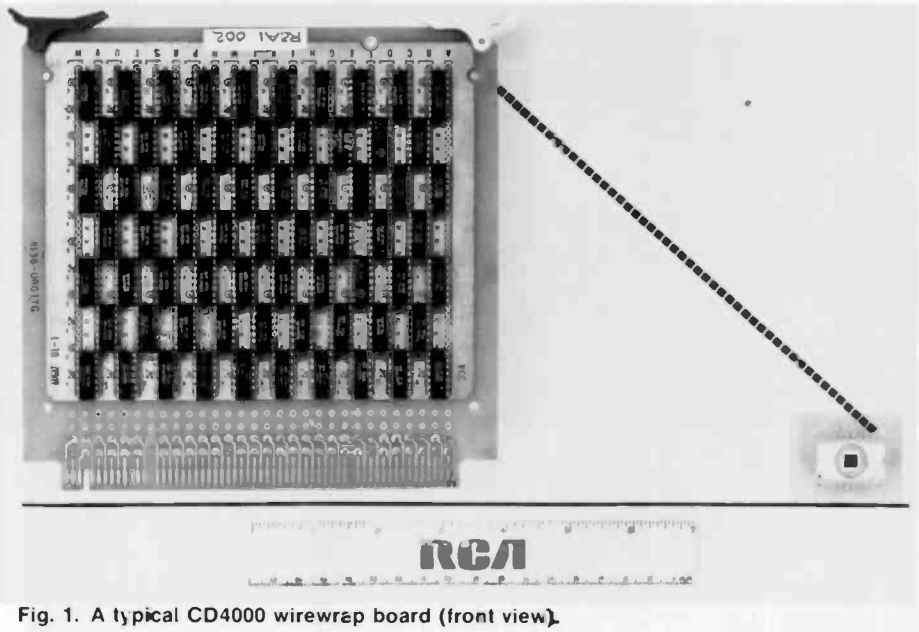

Fig. 1. A typical CD4000 wirewrap board (front view).

significant is the elimination of the approximately 600 wires on the reverse side of the wirewrap board (Fig. 2). This reduces cost and enhances producibility and reliability.

The TENLEY/SEELEY breadboard equipment was assembled using several wirewrap boards to implement the functional logic, as partitioned into LSI arrays. Figure 3 illustrates one typical breadboard equipment composed of 16 wirewrap boards, 11 of which are functionally equivalent to the LSI displayed immediately next to them. As a direct result of the application of LSI to this equipment design, the total equipment final configuration was realized on basically one multilayer printed wiring assembly as shown in Fig. 4.

When LSI?

One of the most important questions asked concerning the application of LSI is, "When does custom LSI application to equipment design and development become cost-effective?" A critical examination was made of both recurring and non-recurring costs for a typical CD4000 design and its equivalent LSI implementation. Table III compares the non-recurring costs for the two design configurations, assuming a printed circuit board assembly for

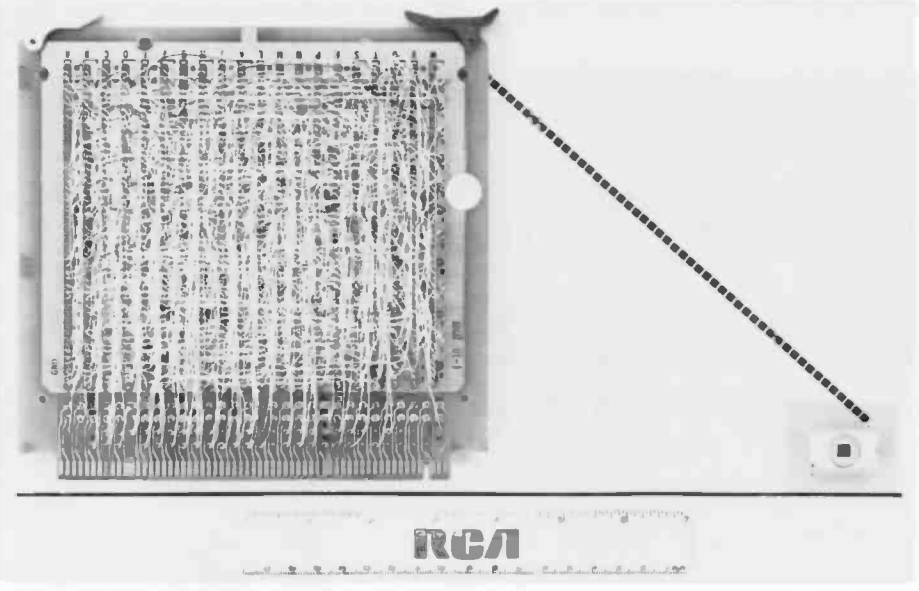

Fig. 2. A typical CD4000 wirewrap board (rear view).

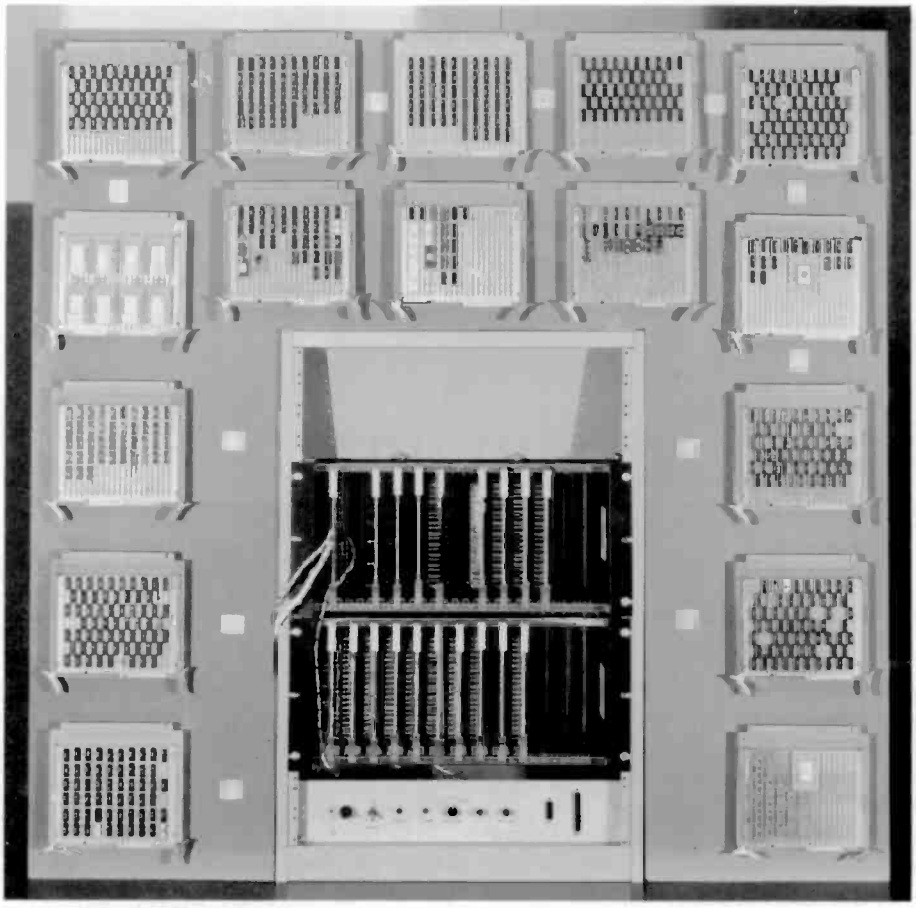

Fig. 3. A typical breadboard equipment.

each of them. As expected, the non-recurring LSI costs are considerably higher (greater than 2 to 1) than the CD4000 configuration. The significant costs for the LSI are in the simulation and automatic placement and routing (APAR) layout and the fabrication costs.

Table IV lists the recurring costs for the two techniques and obviously the LSI costs are lower. In this example, the lower costs for LSI must amortize non-recurring cost differences. Quantities of 150 were used for developing these costs.

Once the recurring and non-recurring costs are established, the cost crossover can be determined (Table V) by dividing the difference in non-recurring by the difference in recurring costs per unit. The somewhat unexpected result is that the cost crossover occurs at 49 units, which is considerably lower than commonly referenced. In fact, this cost crossover point would be even lower if life cycle cost factors were considered: e.g., logistics (sparing one part versus several parts, etc.), training of service personnel, reliability, cost of ownership, etc.

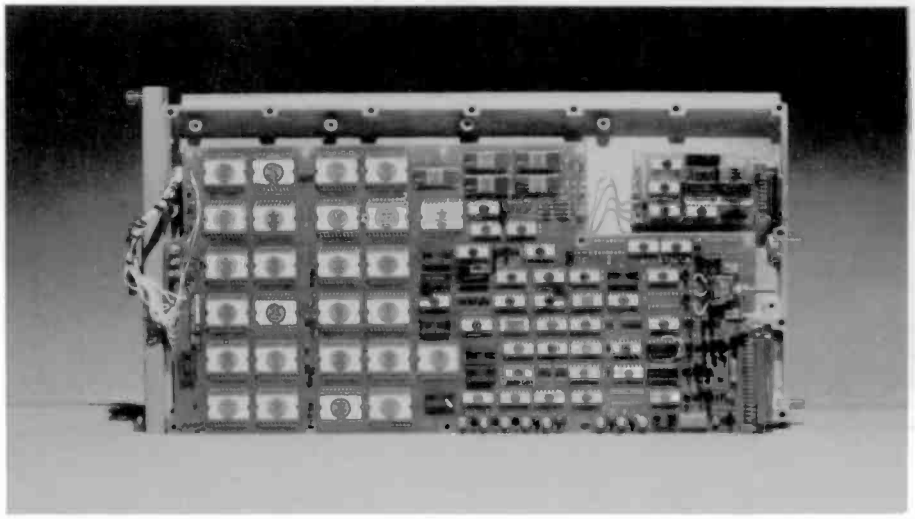

Fig. 4. An LSI equipment.

Table III. Non-recurring costs.

Non-recurring tasks	*CD4000*	*LSI*
PCB drafting	$ 8,000	$ 400
PCB artwork	2,100	210
PCB board test fixture	2,000	160
PCB assembly process	1,800	90
PCB test process	2,400	120
PCB assy/test fixtures	1,700	85
Initial fabrication*		11,600
Simulation/APAR		16,500
Computer cost		2,250
Reticle fabrication		1,000
Data coordination		1,500
Qual test		3,000
Δ = 18,915		
Total	$18,000	$36,915

*Compensated for sample chips

How LSI?

No design or implementation technology, whatever its promises and illusions of grandeur, is worth its weight in salt (or silicon) without a useful methodology to serve as a proven guide to successful application. It is no accident of fortune that this methodology does exist for LSI array development. Many years of study and practical experience within RCA (specifically TENLEY/SEELEY) and the industry have resulted in the methodology described in Fig. 5. The importance of this methodology cannot be overemphasized, and although it cannot guarantee success 100 percent of the time, it certainly can avoid correctable disasters.

The primary keys noted in Fig. 5 are the four reviews, which serve as toll gates in a mainstream serial fashion prior to design release for device fabrication. The initial step in the design cycle is the system concept review (1) which establishes the functional performance and detailed system interface required. Subsequently, the logic partitioning and design is accomplished followed by a preliminary logic review (2). For this review, the designer prepares a detailed design review package

Table IV. Recurring costs.

Recurring	*CD4000*	*LSI*
Active parts	$327.0 (67 CD4000 DIPS)	$70.00
PC board	45.0	3.75
Connector mounting pair	38.00	3.16
Assembly	26.25	1.74
Test troubleshoot	16.00	1.25
QC/PMI	14.00	.70
Δ = 386.65		
Total	$466.25	$80.60

Table V. Cost crossover.

Non-recurring = $36,915 − 18,000 = 18,915/LSI

Recurring = $386/CD4000

$$Crossover = \frac{18,915}{386} = 49 \text{ units}$$

which specifies the requirements, the design to satisfy these requirements, worst-case circuit and timing analyses, and design for testability. Testing of an LSI chip is not an afterthought, but rather a very important part of the design process. Present at the review are representatives of the customer as well as all design disciplines necessary (such as reliability, test process, nuclear survivability, parts application, system, logic and circuit engineers, etc.). Action items generated at the reviews must be answered prior to design finalization.

Following the preliminary logic review, a very critical phase is entered where computer-aided-logic simulation and test-pattern development is initiated, in parallel with the CD4000 equivalent breadboard development. The results of both of these efforts are compared and analyzed repeatedly, and brought to the final logic review (3), together with action item responses from the preliminary logic review. Pending design approval at the final logic review and/or satisfactory responses to any action items generated, the array layout effort is started, followed by a layout review (4). At this point, we are starting to "pour the concrete," and any residual errors will prove costly in subsequent artwork generation and chip fabrication.

Once the layout review is completed and all action items are resolved, the device fabrication cycle (5) is initiated, leading to packaged, tested samples (6). These samples are put into the same breadboard that was used to test their CD4000 counterpart as a functional replacement. The packaged LSI arrays are then tested both functionally and parametrically, as applicable. This testing serves as a most critical design verification prior to final wafer production release. Now the concrete has been poured, but in a form which has passed through a series of critical toll gates to develop a high degree of confidence in the final result. There is a distinct thrill of victory in completing a disciplined methodology and realizing military qualified parts meeting all the functional requirements of the total design. Without the disciplined approach, the almost certain alternative is an agony of defeat.

The time scale at the bottom of Fig. 5 identifies approximate schedules for accomplishing the milestones. Elapsed times should be taken as typical, and can be improved or worsened, depending upon the difficulty of the design, the size of the array and the fabrication cycle queueing.

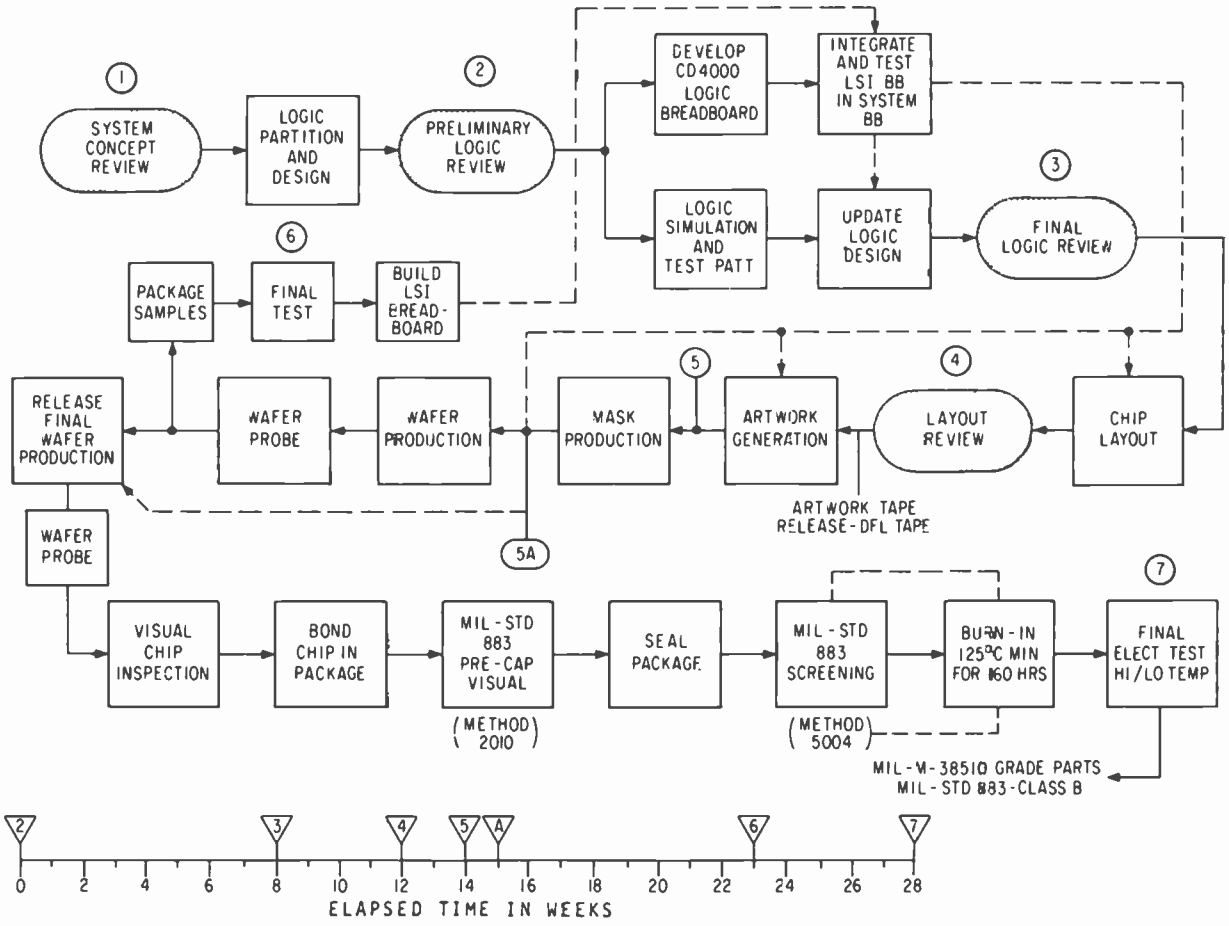

Fig. 5. LSI array development methodology.

Table VI. LSI CAD design tools.

Design tool	*Function*	*Where available*
1. TESTGEN	Logic simulation	Time share (CMS)/Prime
2. LOGSIM	Logic simulation	Time share (CMS)
3. APAR (MP2D)	Chip layout	Prime
4. CRITIC	Layout rule violations check	Time share (TSO)
5. ARTGEN	Artwork generation programs	Time share (TSO), Prime
6. RCAP	Circuit analysis	Time share (CMS)
7. Applicon (DFL translation)	Manual layout Mod.	ATL
8. TACC (SOS)	Routing & interconnect rules	ATL Comp. CTR.
9. APRAIS (Bulk CMOS)	Routing & interconnect rules	ATL Comp. CTR.
10. CALCOMP	Layout plotting	ATL Comp. CTR.
11. SPICE	Circuit & failure analysis	Prime
12. Data conversion programs	Data format translations	Prime
13. MIMIC	Logic simulation	Time share (CMS TSO)

In summary, the successful application of LSI depended on the design process, which in turn was made possible by the use of the CAD tools available within RCA. Table VI lists thirteen design tools which constitute an impressive capability for supporting design, development and testing of LSI arrays. Comprehensive programs are available covering all the necessary design elements: logic simulation, array layout, circuit analysis, design and layout rules checking, failure analysis and layout plotting. Table VI also lists the source for these tools. Some of the tools were used on TENLEY/SEELEY, some were not necessary, since some of the tools are design options presented to the user for specific design optimization compatibility. It should be borne in mind that these tools are continually being updated and improved, based on user feedback, and that new tools are also being developed as the need arises.

Testing the results

Almost as critical as the design itself is the testing methodology and the development of the necessary techniques and tools for the testing of LSI arrays and the assemblies and equipments in which they are used. During the TENLEY/SEELEY program, every design review included intensive attention to testability. Manual testing of individual devices which include thousands of gates in complex logic functions, with multiple inputs and outputs, is not practicable. Such testing would require a vast number of very highly skilled testers with infinite patience, who would be willing to spend many hours with a complex assortment of test equipment trying to verify the performance of an LSI array to extremely demanding functional and parametric specifications. If there were such talents in the numbers required, there certainly would not be enough money around to pay for them.

The basic problem escalates when 20 or 30 of these LSI devices are assembled onto a printed board, and escalates again when multiple assemblies are integrated into a functional equipment. If the basic design is conducted properly, the logic is functionally partitioned into testable groups such that, as the degree of integration increases, the testing complexity decreases. Furthermore, the basic logic elements are designed to be testable, that is, registers are settable to known states, counter states are deterministic, outputs are predictable, etc.

On TENLEY/SEELEY, special automatic test equipment was developed for the depot, intermediate, and organizational level equipment maintenance levels; techniques were also developed for individual part testing on standard equipment. Significantly, the equipment maintenance functions were required to include both go/no-go acceptance and failure diagnostics functions. The two areas where LSI testing is of primary importance are (1) at the depot level maintenance area, where test equipment must be capable of isolating faults in a defective assembly to the bad component, and also to verify corrective action prior to returning a repaired assembly to the field, and (2) at the LSI fabrication area, where performance of individual devices to a specification must be verified.

On TENLEY/SEELEY, designers developed LSI array test patterns for the DATATRON 4400 equipment; complexities were as great as 2000 test patterns each 42-bits wide. For the printed wiring assemblies, greater than 60,000 test patterns up to 160-bits wide were necessary per printed wiring assembly. These assembly test patterns were not only capable of doing go/no-go testing, but they were also required by specifications to detect greater than 95 percent of the faults on the assembly, and to isolate greater than 85 percent of these faults to a single node. Both of these specifications, for fault detection and isolation, were met or exceeded.

The LSI assemblies used on TENLEY/SEELEY were multilayer printed wiring boards with a maximum of fourteen layers. The LSI devices were inserted into the boards with through-hole lead insertions and one-time wave soldering was used for the integrated assembly. No problems were observed with the printed wiring boards or in implementing a reliable LSI component interface. The TENLEY LSI printed wiring assembly shown in Fig. 6 includes twelve custom 42-lead CMOS LSI arrays plus some discrete components. The obvious advantages of using LSI are evident, as are the problems of testing a board of this complexity and isolating faults to a single node.

The special automatic test equipment was developed to accomplish fault diagnostics for printed wiring assemblies (PWA). This equipment used a minicomputer processor in conjunction with an X/Y movable table and fixed single and multiple pin probes. For go/no-go testing, the probes were in general not necessary, since all tests were accomplished through the board connector. The basic principle used for the automatic test equipment (ATE) is to apply input patterns to a known good PWA and record output responses on a disk. These responses are subsequently compared with the responses of a board being tested. Any differences are noted and recorded as a failure or no-go condition. Once a no-go or fault condition is found, a diagnostic program is entered where nodes are probed in a sequential pattern from the fault until the faulty node is discovered. The special ATE developed was capable of applying input patterns at a 10 kHz rate, and diagnostic and go/no-go testing was rapid and extremely cost-effective.

The conclusive facts

Now that we have covered the why, when and how of custom LSI design and application, and the testing methodology, we can

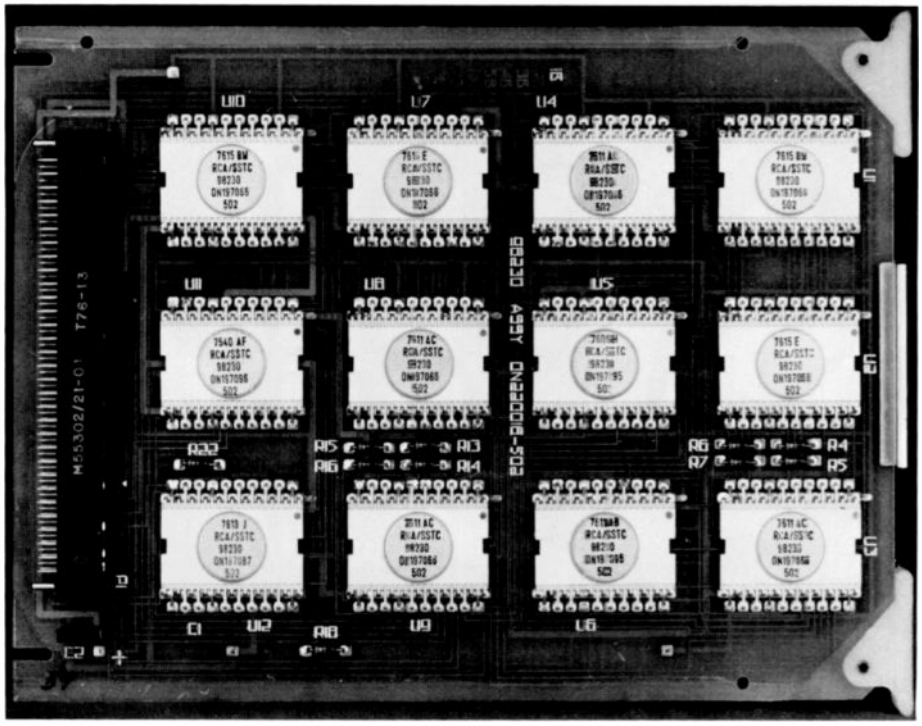

Fig. 6. An LSI printed wiring assembly.

turn to the conclusive results on the TENLEY/SEELEY program. These establish beyond question the advantages of LSI in military systems and environments.

The technology used was proven metal-gate bulk CMOS, primarily in standard cell designs, using totally custom implementation only where dictated by the design complexity, or where obvious design improvements were possible (such as in regular repeated functions). The standard cells used were developed by RCA in conjuction with the necessary associated CAD (largely by ATL, on Government funding as well as extensive internal support).

There were 60 LSI types developed, with no reworks necessary to achieve the required functionality. This was a first-time achievement for both the customer and RCA on any program of comparable complexity. Of the 54 types developed early in the program, 37 were developed in 23 months on TENLEY, and 17 on SEELEY in 11 months. There were 19,000 chips of 37 types produced on TENLEY in six months, primarily at RCA's SSTC facility in Somerville. The total number of chips produced to date is greater than 50,000, the majority of which were supplied by RCA's SSTC facility supported by SSD and two external sources (Hughes and Solid State Scientific, both qualified by RCA for the TENLEY/SEELEY program).

Table VII lists the TENLEY/SEELEY LSI array statistics, the range of complexity and size further attest to the design flexibility. The largest chip shown (213 x 231 mils) was a custom design which used a specially designed large cell (not a part of the standard cell library) to produce a cost-effective functional partitioning within a then practical large physical size. At the time that the TENLEY/SEELEY chips were designed, 1972-1977, greater than 200 mils on a side was considered a large array.

Table VIII sets forth the complexity of the LSI arrays developed. These complexities represented the state of the art at the time, and are still compatible with good processing yields for high quantity production.

Extensive reliability testing was accomplished in functional equipment qualification for military environments. On the TENLEY effort, 1200 LSI arrays of 36 different types were tested in three operational equipments per MIL-STD-781B Level E over a temperature range of −45°C to +65°C. A total of 2,160,000 device hours were compiled with zero failures. Reliability testing conducted on the SEELEY effort demonstrated conformance of the two high usage LSI equipments to mean time between failure (MTBF) requirements of greater than 5000 hours. During this equipment testing, over 1,000,000 LSI device hours were accumulated. The equipments were operational during the testing, which included temperature and vibration stressing.

At the present time, all of the TENLEY equipments (which include 31,261 chips) have been delivered and are being used in the field. To date, the equipment and assembly depot repair effort at RCA has reported 18 LSI failures repaired in defective hardware. This represents a small percentage of the equipment failures recorded, and is an extremely small number considering the quantity of devices deployed in field service.

A specific requirement on the TENLEY/SEELEY program was equipment survivability in a nuclear environment. The equipment test results showed no failures during electromagnetic pulse (EMP), gamma total dose, gamma transient dose or neutron fluence attributable to LSI devices. In addition, individual device tests on LSI arrays demonstrated the relative inherent hardness of the CMOS LSI devices for a tactical nuclear environment.

A representative custom bulk CMOS standard cell LSI array developed on the program is shown in Fig. 7. This array measures 211 x 209 mils, contains 1482 devices, 188 cells, and uses 1348 linear mils. The regular pattern and physical layout characteristic of a standard cell design configuration is evident.

Table VIII. LSI array complexity.

	Minimum	*Maximum*
No. of cells (STANDARD)	51	188
No. of devices (XSTRS)	341	1554
Linear mils	335	1359

*Largest LSI was a custom design 213 x 231 (49.2K mil^2) containing 2348 devices.

Table VII. LSI array statistics.

Program	*No. of types developed*	*Largest chip (mils)*	*Smallest chip (mils)*	*Quantity produced to date (9/79)*	*Technology used*
TENLEY	41	(213 x 231)	(128 x 148)	31,261	Bulk CMOS custom and standard cell
SEELEY	19	(208 x 225)	(167 x 158)	19,312	Bulk CMOS standard cell

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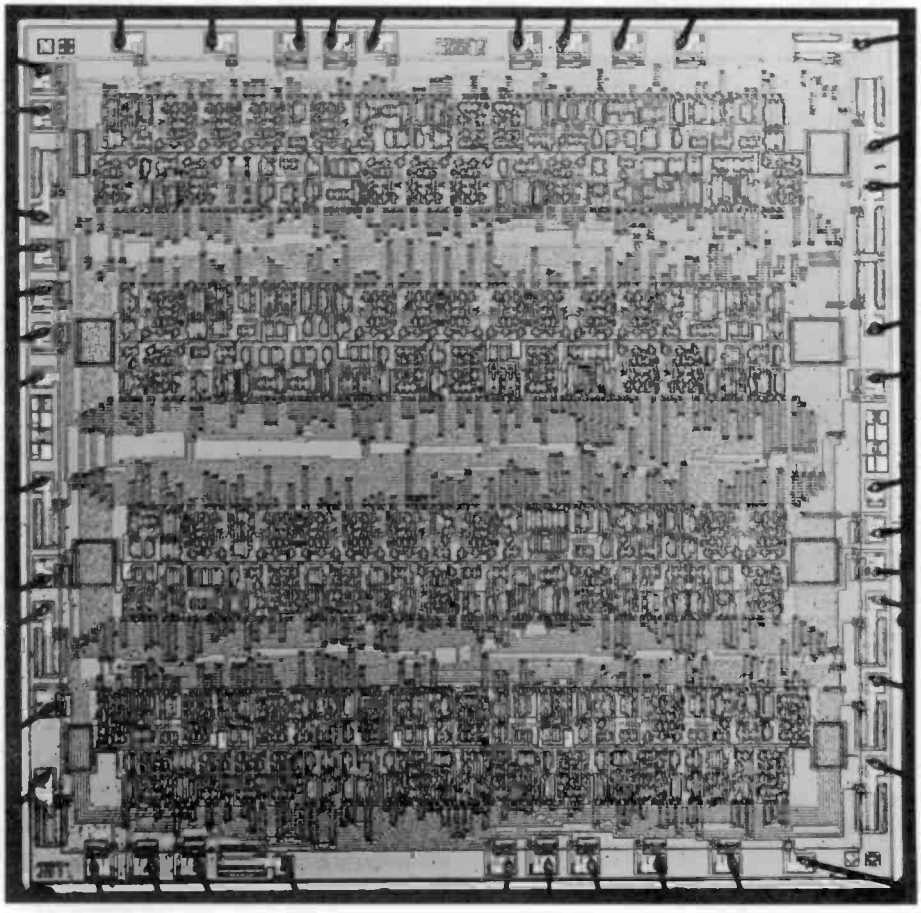

Fig. 7. A representative standard cell array.

Concluding remarks

The TENLEY/SEELEY program represents a significant achievement in the application of custom LSI to military digital communications equipment. Successful results were achieved through the use of a disciplined design methodology, coupled with close attention to the total design problem and emphasis on testability and intelligent logic partitioning. Computer-aided design was a major contributor, without which it is doubtful that the program objectives would ever have been met. The design techniques and methodologies developed have served and are continuing as guidelines for many new programs. The equipment status has gone from R&D to the anticipated near-future initial production. The essential role of collective achievement, based on the intelligent use of the required skills available in ATL, SSTC, SSD and GCS as well as the active participation of the Government customer, was a major factor on the program. Although there was considerable skepticism at the program outset, particularly regarding the LSI development schedules, the team dedication never faltered. In the end, TENLEY/SEELEY made "believers" out of many of us, both Government and RCA personnel.

R.E. Stricker|A.G.F. Dingwall

Advances in CMOS static memory development

RAMs contribute a lion's share to the overall memory/microprocessor total business and RCA locks horns with the competition by improving circuit densities and access times in bulk CMOS and CMOS/SOS static memories.

Abstract: *The historical development of CMOS RAMs, together with a summary of the general modifications and trends in device structure, interconnect topology and access times, leads to projections for future developments in LSI and VLSI.*

Recent advances in very large scale integration (VLSI) have brought about major gains in the size and performance of metal-oxide semiconductor (MOS) memories. Using dynamic NMOS memory techniques and a one-transistor cell, the semiconductor industry has pushed beyond the 16K level, is delivering small quantities of 64K random access memories (RAMs) and has fabricated a few 256K devices in the laboratory. With these developments, we believe the semiconductor market could exceed one billion dollars by the mid-1980s.

Semiconductor memories have historically been at the leading edge of technology providing the driving force for technology advancement. Any intelligent control system, data acquisition system or data manipulation system is rich in semiconductor memory content. For example, a typical microprocessor-based system for engine control in the automobile industry uses one microprocessor or microcomputer for data manipulation and instruction execution, one read-only memory (ROM) for resident program storage, an input/output (I/O) circuit for interface with various sensors and one to sixteen RAMs for intermediate data storage and calculation. As system complexity increases, the memory content of the system increases drastically. Thus, RAMs contribute a lion's share to the overall memory/microprocessor total business.

While much of the memory market will be served by the lowest-cost, largest-capacity dynamic NMOS memory chips, an important section of the market will require the performance advantages afforded by static memory that complementary metal-oxide semiconductor (CMOS) technology can provide. Among the advantages provided by static memory are shorter access times, lower standby power, easy interfacing, improved reliability, and the ability to operate over a wide range of temperatures and power-supply voltage levels. The advantages will provide a significant performance edge in industrial and military systems, in automobiles where extreme temperature conditions are encountered, in cash registers where protection of data against power-supply failure is critical, and in hand-held portable systems where low battery-drain levels must be maintained.

High density CMOS/SOS RAMs

RCA has participated actively in both the bulk CMOS and CMOS/silicon-on-sapphire (SOS) memory markets which have also achieved circuit density improvements in recent years. Figure 1 compares recent trends for both CMOS and dynamic NMOS memories. Dynamic RAM density has been doubling approximately every two years. Due principally to the larger number of transistors employed per cell, static RAMs are typically a factor of five-to-six times smaller in capacity than dynamic RAMs at any given time. We can infer from this trend that static RAM designs lag their dynamic RAM counterparts by four years. Assuming trends of Fig. 1 remain valid, the CMOS suppliers will want to be prepared to make 64K RAM chips in 1983.

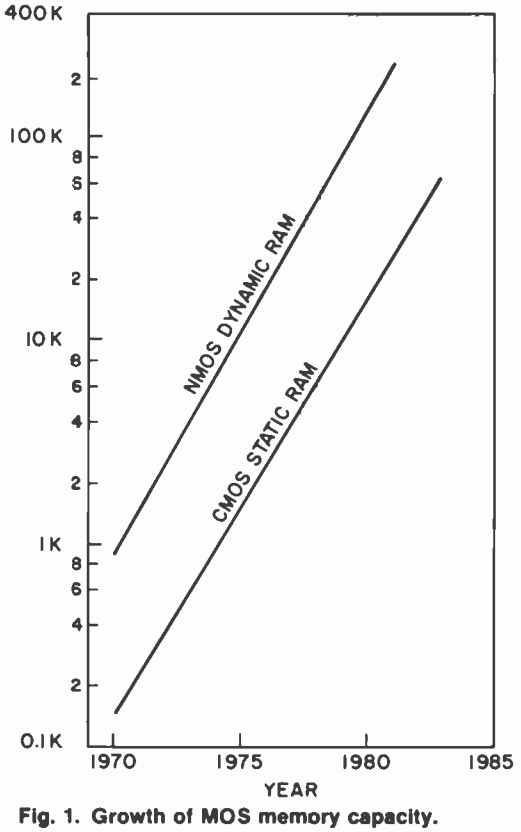

Fig. 1. Growth of MOS memory capacity.

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We should, at this point, examine the historical development of CMOS RAMs. The two major driving forces behind RAM development, so far, are the cost per bit of memory storage and performance. Although the cost of any product is governed by many complex relationships, we assume that the cost is strongly related to the number of bits of storage of memory per given circuit. Simply stated, improved circuit density, or the ability to pack more transistors into a given area, is the driving force behind low cost memory development.

There are two fundamental methods of increasing density: reduction in feature sites in order to produce smaller transistors; and changes in the topological device structures and the fabrication sequences to obtain higher density. Reduced feature sizes, and the fabrication equipment required to produce these small features, is discussed in another article in this issue ("Advanced Process Technology at the Solid State Technology Center" by E.C. Douglas). A summary of the general modifications to device structures and interconnect topology is presented here.

Since memory cells typically occupy 40-to-60 percent of the active area in CMOS LSI RAM chips, cell sizes must shrink to achieve needed gains in density. The basic six-transistor CMOS memory cell with two cross-coupled inverters and two access transistors is shown in Fig. 2. Implementation of this cell using the RCA Metal-Gate CMOS Technology (the basis of the standard RCA CD4000 product series) presents an area-consuming topological nightmare to the integrated circuit layout designer. Interconnection of the metal gates and device source/drains in the single plane of an integrated circuit is difficult at best. The addition of an independent interconnect level, namely polysilicon, was used only as a means of routing signals under metal lines and resulted in a 256-bit RAM with a cell area of 36,000 square microns (Table I).

Table I. Past and projected evolution of high density CMOS and CMOS/SOS processes for high density static RAMs.

Typical process	*Minimum RAM cell size (sq. microns)*	*Typical dimension (micron)*	*RAM size (K)*
Metal gate	36,000	8	.25
C^2L Si-gate	9,000	6	1
CMOS/SOS Si-gate	3,000	5	4
CMOS/SOS + buried contact	1,200	5	16
CMOS-I Isoplanar + buried contact	2,600	5	4
CMOS-II Si-gate	1,500**	3	16**
CMOS-II buried contact + 2 levels poly	800**	3	32**
CMOS-II with poly loads	360**	3	64**
VLSI CMOS	150**	2	128**
VLSI CMOS/SOS	80**	1.5	256**

**Projected developments

The self-aligned silicon-gate technology led to the next improvement in RAM density. Here, poly-Si is used both as the MOS gate electrode and as an additional level of interconnect. The TC-1024, a 1K-bit CMOS RAM,[1] was one of the first devices produced using this technique. A 1K-bit RAM was made with a cell area of approximately 9,000 square microns. Another application of the self-aligned silicon gate technology on bulk silicon is the closed-cell logic (C^2L) technology.[2] Here, a closed-transistor structure was used to improve device performance and resulted in the basic technology of the RCA CDP1800 series of microprocessor products.[3]

Silicon-on-sapphire (SOS) fabrication techniques contributed significantly to memory development, as shown in Table I. The basic density improvement inherent in CMOS/SOS results from minimum area requirements for device isolation, and the ability to place PMOS and NMOS devices without regard to a p-well, as in bulk silicon. RAM density improved by a factor of 12 over C^2L RAMs because of the CMOS/SOS technology.

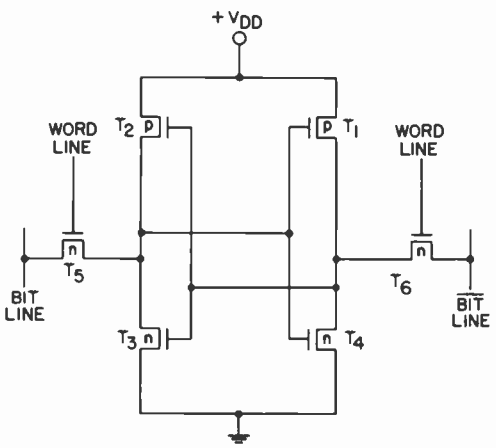

Fig. 2. Ideal circuit model for six-transistor CMOS memory cell.

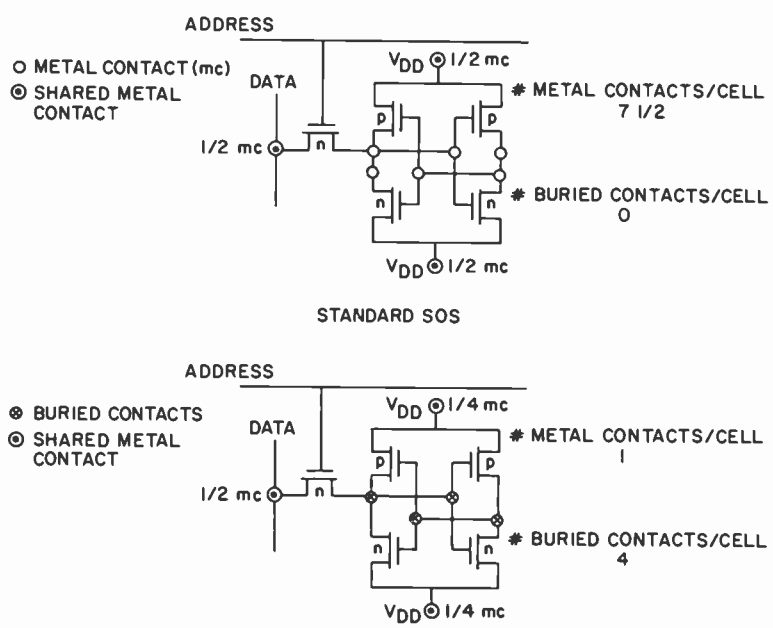

Fig. 3. Comparison of standard SOS and buried-contact five-transistor static memory cell.

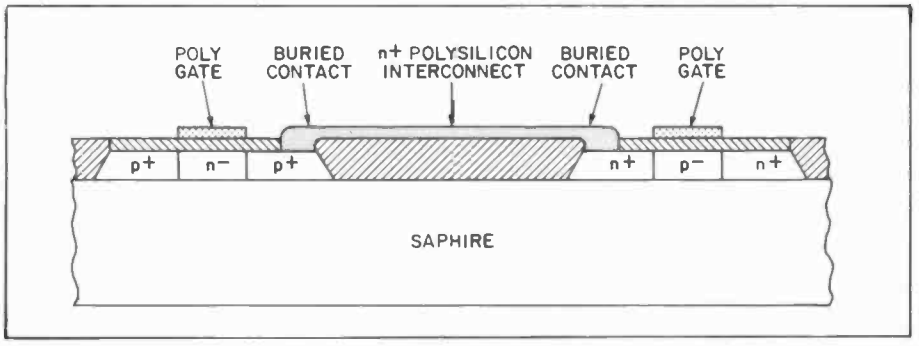

Fig. 4. Cross-section of buried-contact structure in SOS showing direct contact between polysilicon and drains of two MOS transistors.

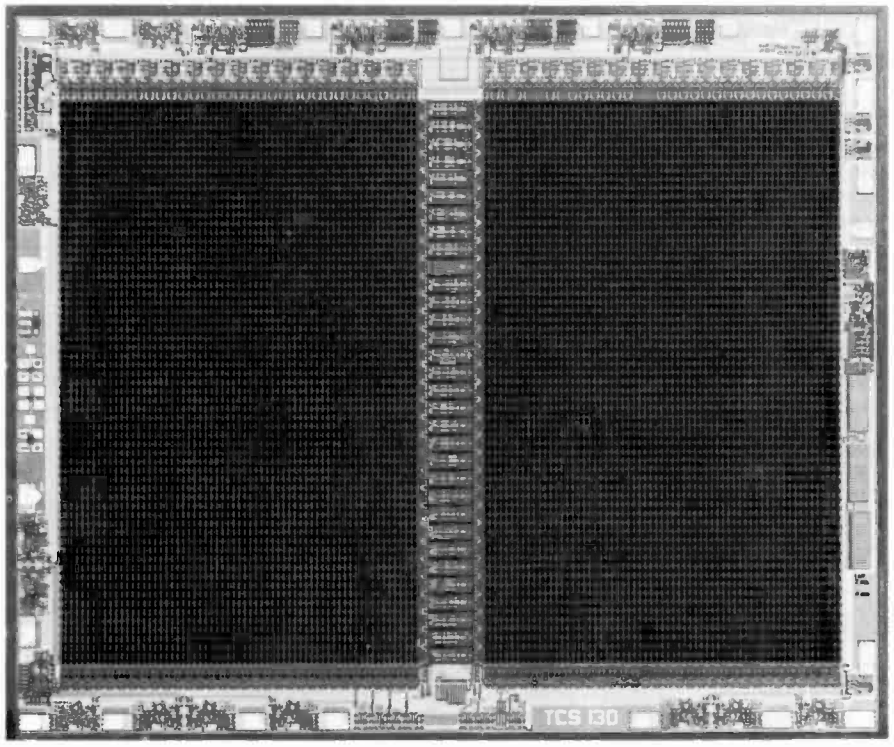

Fig. 5. TCS-130, 16K static CMOS/SOS RAM.

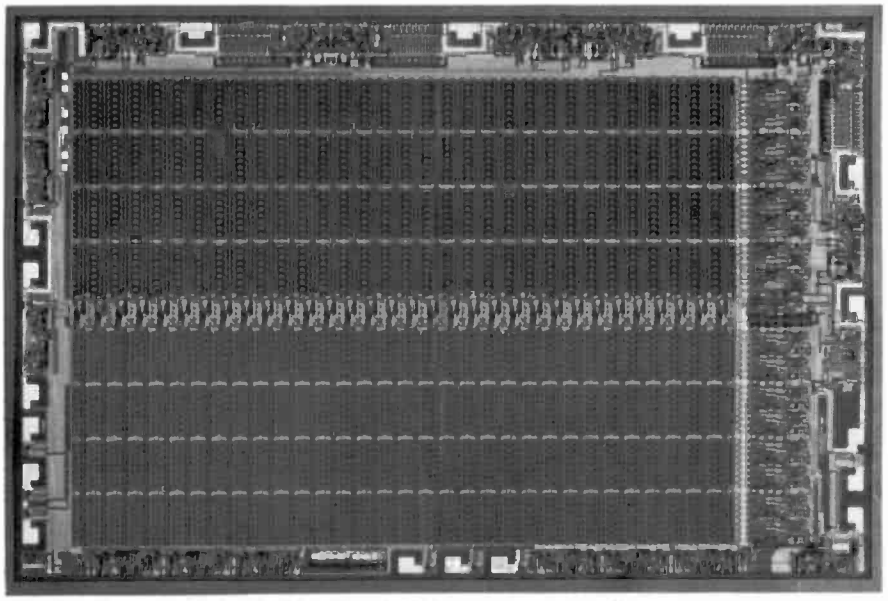

Fig. 6. 4K static CMOS RAM with a 2600-square-micron cell area.

Now new circuit design techniques in conjunction with a structural change in the CMOS/SOS device have led to the first 16K Static RAM.[4] This 87,000 transistor circuit has a cell area of 1,200 square microns. Advances in circuit design techniques let us use a five-transistor memory cell—a one element reduction over the standard cell of Fig. 2. The five-transistor cell, shown in Fig. 3, also makes use of a "buried contact," or direct contact between the polygates and the source/drain diffusion. The buried contacts allow complete interconnection of the internal memory cell without wasting space with metal contacts. The buried contact physical structure is shown in Fig. 4 and the TCS-130, 16K static CMOS/SOS RAM (a research application) is shown in Fig. 5.

The buried contact approach has also been applied to bulk silicon CMOS/LSI. Isoplanar oxidation, an approach which replaces the junction isolation of devices with insulation or silicon-dioxide isolation, coupled with buried contacts, has led to a 4K static CMOS RAM with a 2600 square micron cell area[5] (Fig. 6). This technology, called CMOS I, is thirteen times more dense than C^2L, which is approximately equivalent to CMOS/SOS. Although not as dense as buried contact CMOS/SOS, CMOS I is a relatively low-cost technology because sapphire-wafer substrates cost much more than bulk-silicon substrates.

The remaining items in Table I show memory cell areas as low as 80 square microns that will support RAM designs of up to 256K bits. More innovations in device design will be required. For example, additional levels of polysilicon interconnect, level-to-level buried contacts, and high-resistivity as well as low-resistivity loads will be needed. But clearly, static CMOS RAM density will continue to increase throughout the 1980s.

Future industry RAM efforts to increase density will rely heavily on shorter channels and tighter designs. The RCA CMOS-II process with three-micron design rules and even more difficult VLSI CMOS processes with design rules of two-micron or less are projected in Table I, to allow up to 256K RAMs on a single chip.

Memory circuit design

Parasitic capacitance is the major factor controlling the access time of MOS semiconductor memory. As the size of MOS memories has increased, internal parasitic capacitance has also increased because larger numbers of cells now share

the common sense lines. Although this effect is somewhat offset by the use of smaller cells, the net result would have been distinctly slower memory chips without the innovative memory circuit developments which accompanied the IC process developments.

Table II summarizes recent trends in access time for CMOS/SOS RAM designs. Access time has decreased up to an order of magnitude in the past years, while memory capacity has increased 64 times. Increased speed requires significantly more sophisticated and larger amounts of peripheral circuitry. The net trend has been that the peripheral circuitry continues to occupy a constant 40-to-60 percent of the total chip area, even in the large-capacity RAMs with small cells.

Several circuit techniques and strategies have been employed to reduce internal circuit delays. CMOS/SOS designs are faster than bulk CMOS designs. With shorter channels and finer geometry, new MOS transistors have been helpful, especially for bulk designs, because of reduced parasitic capacitance and higher drive currents. Important speed gains have also been achieved through the development of noise-rejecting regenerative sense amplifiers. Internal signals of 50 to 100 mv are now sensed rather than full logic swings of 2.5 to 5 volts as in the earliest designs. Extremely large output drivers are routinely used throughout to minimize delays. Early CMOS output drivers were typically 500 ohms. Modern designs now have output drivers in the 20 to 50 ohm range, while critical internal nodes use 100 ohm drivers. Finally, changes in input address lines can be sensed and dynamic precharging and 'lookahead' pulses can set up critical signal propagation logic at their "toggle" points to enhance the rate at which on-chip signals propagate.

Table II. Trends in speed performance of RCA CMOS RAMs.*

Year	Type	Technology	Access time $V_{DD} = V_{DC}$	Size
1970	CD4061	Metal gate bulk	300ns	.25K
1974	TC1024	Si-gate bulk	600	1.K
1976	TC1190	C^2L	200	1 K
1978	5114	CMOS/SOS	450	4 K
1978	TCS151	CMOS/SOS	130	4 K
1979	TCS165	CMOS/SOS	60	4 K
1979	TCS130	CMOS/SOS	120	16 K
1980	TCS241	CMOS/SOS	50	4 K

*TC signifies Tech Center research device. When the part goes into production, the number is changed.

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Electro-optical techniques for measurement and inspection

Small, state-of-the-art lasers and solid-state optical scanning arrays make possible a whole new generation of electro-optical measurement and inspection systems.

Abstract: *The authors discuss a number of new techniques and some developing technology for electro-optical measurement and inspection. To date, most of these have been applied to problems of the RCA Picture Tube Division, but their flexibility allows them to have wider impact. Current work aims to increase the speed of these systems and to incorporate them in on-line process control. One example of this is hand-eye coordination for industrial robots, a fast-emerging field in manufacturing research.*

Introduction

In response to consumer demands for higher quality in the products they buy, manufacturers have instituted more and better in-process-control systems. But these systems cannot be allowed to decrease productivity if the manufacturer wishes to remain in the marketplace. One answer to this quandary is to use more automatic and programmable on-line inspection and measurement systems, often incorporating sophisticated electro-optical technology.[1]

The use of optical methods in the production environment is by no means new; visual inspection, for example, abounds. But the pressure for increased speed and accuracy has driven us to exploit non-contact, flexible, optics-based techniques in new ways. Recently, inexpensive, reliable, small lasers and a range of solid-state sensors have made our task easier.

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We wish to discuss a number of electro-optical methods which we have been investigating as they relate to the needs of the RCA manufacturing divisions. The emphasis will be mainly on applications for which no suitable commercial systems exist.

We will divide our discussion of measurement systems into two main areas: planar methods, in which the measurements are made by scanning in the image plane; and out-of-plane methods, in which measurements are made along the line-of-sight or optic axis of the system. We will also discuss exploratory work on a new inspection system which mimics an aspect of the human visual process. While we will not discuss any Princeton work on coherence-based optical methods, several such instruments developed at the Zurich laboratory were described in a recent *RCA Engineer* article.[2]

Planar methods

Most of our work in the planar measurement and inspection area has made use of a linear, self-scanning, diode-array from EGG-Reticon. Such linear arrays come with up to 2048 elements; we typically use 512, 1024, or 1728 element scanners. In addition to linear arrays, matrix arrays such as those used in the popular "Optomation" cameras from GE are also available, but with decreased linear resolution (typically 128 x 128). The dimensional stability offered by such solid-state scanners gives them a significant advantage over conventional vidicons which, at best, have one percent linearity. In contrast, the combination of a high-resolution linear array with mechanical motion in the orthogonal axis can yield accuracies of better than one part per thousand.

We have built two prototype measurement instruments using the Reticon scanner, a device for measuring the widths of the openings in the shadow mask and a similar apparatus for measuring the widths

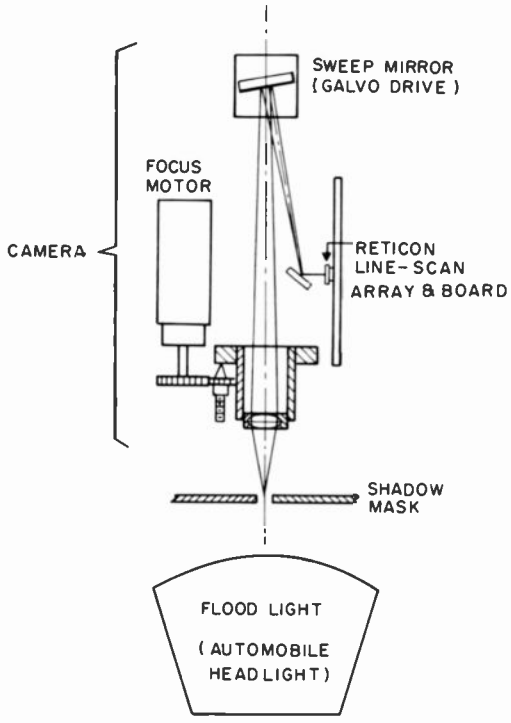

Fig. 1. Schematic drawing of the basic Reticon camera system.

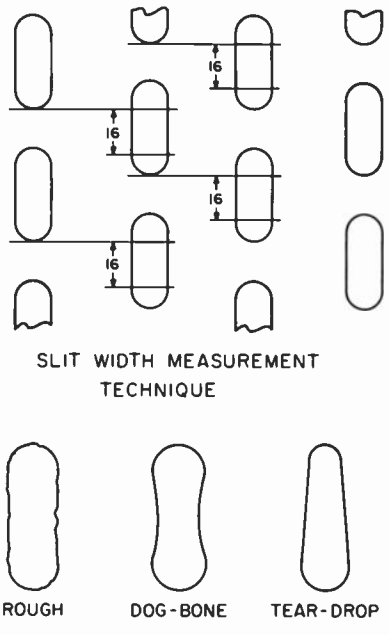

Fig. 2. Diagrammatic representation of the slit-width measurement system showing the scan pattern and slit-shape problems.

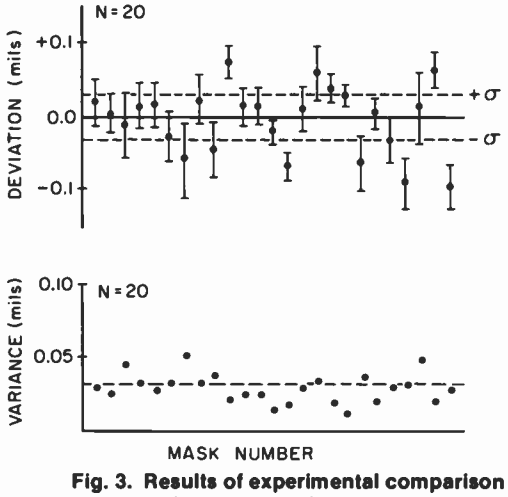

Fig. 3. Results of experimental comparison between visual and machine measurements of slit width. The upper graph shows the deviation between the average visual measurement and the machine data. The σ-values shown are average visual variances; machine variances are shown by bars. The lower curve compares the variances only.

of the matrix lines on a kinescope cap. The camera which we used is shown schematically in Fig. 1. In addition to the line scanner, it has a focus motor which is driven by auto-focus circuitry and a galvanometer-type scanning mirror to allow sweep in the direction perpendicular to the linear scan. Both units use back illumination provided by an automobile headlight.

The scanning pattern on the shadow mask is shown in Fig. 2. As the galvo mirror sweeps downward, the electronics recognizes the end of one slit and automatically makes measurements of the slit-width in the adjacent slit. An average of four such slit readings gives a representative reading of the center mask openings. The problem with such measurements is that the slits may suffer from a range of maladies such as those depicted in the bottom of the figure. These effects often make an accurate comparison between a machine and a human measurement difficult as judgments must be made in the process. One may legitimately question what a human observer measures in such a case.

In spite of these difficulties, however, machine and human measurements can agree. In a test run, twenty 19-inch shadow masks were measured with a Vickers translated-image microscope and by the slit-width measuring device. The entire set of masks was rotated through the machine 20 times and statistics were gathered. Figure 3 shows the difference between the machine and average visual readings; the bars indicate the standard deviation. Note that an occasional difference of up to 0.1 mil occurs which may result from the judgment factor mentioned above. If one compares the variances of the machine and of a human (bottom of Fig. 3), however, we find them both to be about 0.03 mils, indicating similar accuracy in both cases.

The prototype for an on-line instrument designed and built for measuring the widths of matrix lines on a kinescope screen is shown in Fig. 4. The camera is located below the table in this case and the light source swings out over the cap during measurement (Fig. 5). The electronics and a printer are located on the side. In operation, the cap is placed face-down against the camera. Upon removal of the mask, the lamp comes forward, the cap is automatically centered, the measurement is made and the light returns to its original position. The whole cycle takes about 10 seconds.

A serious visual inspection problem faced by PTD is the checking of the large glass plates which are used to expose the shadow mask pattern. Before actual use, these plates are subjected to a detailed microscopic examination to search for defects, a process which takes up to three hours. After 250 masks are exposed, the plate is checked against a negative plate to find major defects. The entire process is time-consuming and fraught with error. We are currently testing a third system developed to automatically locate plate defects in which a line-scan camera mechanically scans the surface of the working plate, identifies potential defects and marks the reverse side of the plate so that the operator need only inspect these regions for the suspected defect. We still depend upon a person to categorize the defect as to whether it is meaningless, repairable, or fatal, but this task, too, can eventually be automated.

The algorithm used by the scanner to detect a defect is described in Fig. 6. The upper portion of the figure depicts the negative of the shadow-mask slits. As indicated, the region of the line scan includes a particulate defect. The resultant digitized video from the scanner is shown in the lower part of the figure. A simple approach to finding defects would be to delay the scan by one period of the mask and to compare the results with the next scan (autocorrelation). If the pattern were truly repetitive, this technique would allow the adjacent area to serve as a template for the inspected one. However, the shadow masks made by RCA have a variable period or A-spacing which causes shifts in the pattern between adjacent areas. Although the resultant offsets encountered within one period are unimportant, the accumulated error over several periods causes a large number of erroneous defect indications, as shown schematically in the figure.

Making the algorithm adaptive by changing the delay to correspond to the previous A-spacing overcomes this problem. To do this, the electronics aligns the leading edges of each slit pattern as shown. Note that the particle shows up twice in the scan, once when its region is compared to the previous one and again when it is compared to the following region. In the actual machine, an error must be present on two successive linear scans to define a defect.

The line-scan applications we have outlined so far have a lot in common. Their implementation, however, took a significant amount of time since all the logic had to be hard-wired. In a new approach, we have developed a special interface board between the camera proper and a microcomputer data bus. The board allows the computer to set digitizing thresholds, clock rates, data acquisition formats and much more. This results in a software-based system which should be easy to modify and to program for a wide range of tasks. It should eventually allow anyone familiar with the Intel microcomputers to set up their own inspection system tailored to their needs.

Fig. 4. Overall view of the matrix line-width reader showing the light source, the side-mounted electronics and the cap positioning mechanism.

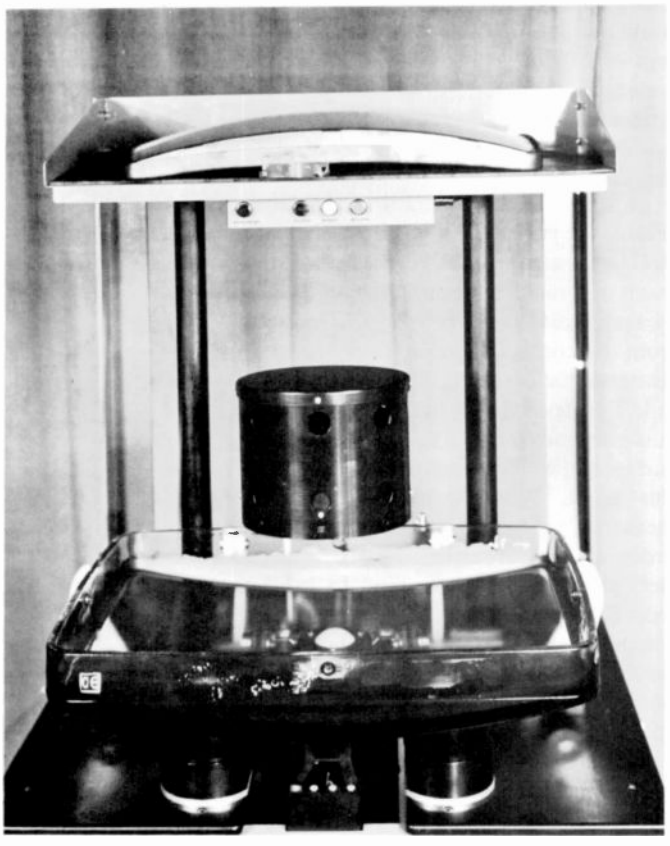

Fig. 5. Close-up view of the matrix reader showing the cap and light source in the reading position. The camera is mounted below the cap. Note the shadow mask on the tray above.

Out-of-plane methods

One of the more difficult problems to solve optically is to measure distances along the optic axis of the system (out-of-plane measurements). Two techniques are typically used: focus sensing and optical triangulation. One form of focus sensing is that used in the line-scan camera described earlier: an electronic filter isolates the high-frequency components of the video signal and a servo system moves the lens to maximize this signal component. This technique works well but it tends to be slow and requires an area with sufficient structure to produce the required high frequencies. However, where it can be used, it is relatively easy to implement and can be very accurate.

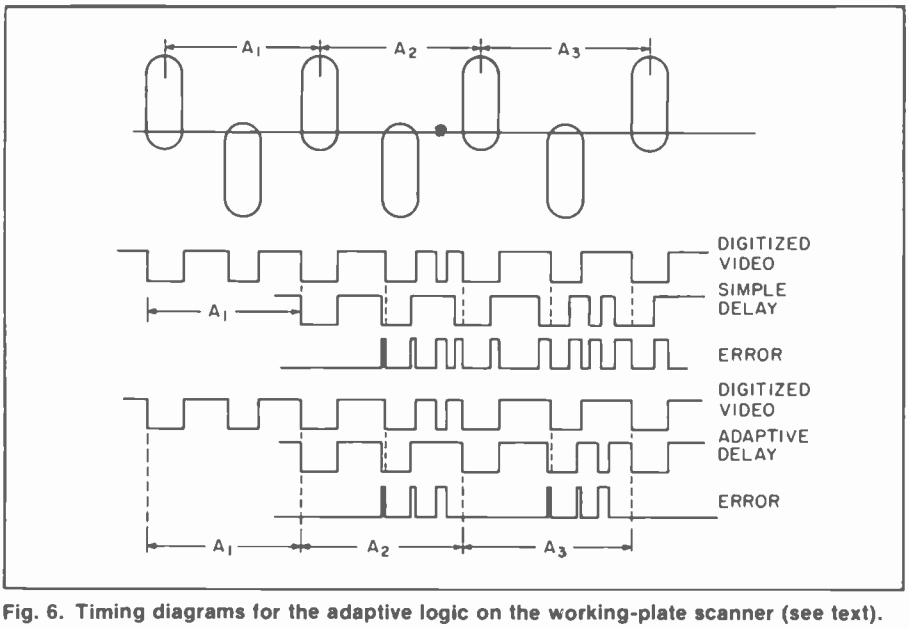

Fig. 6. Timing diagrams for the adaptive logic on the working-plate scanner (see text).

Figure 7 shows an alternative form of focus sensor on which we have been working for some time which has the potential of being very fast, is relatively insensitive to angle, and uses a small spot size. (The spot is produced by a laser coupled into the system via a beam splitter which has been left off the figure for clarity). In the original balanced state, the position of the spot image is equidistant from the near and far detectors, yielding equal outputs S_N and S_F respectively. Displacement of the surface by a distance x moves the image a distance amplified by an amount equal to the square of the lateral magnification M. As a result, the signal S_N increases because more light passes through its aperture while S_F correspondingly decreases. These two signals are passed through sum and difference amplifiers to yield the characteristic curves shown at the upper right. Clearly, these outputs could be used to control a feedback loop which would

keep the sensor locked at a given height above the surface; the resultant motion could be measured to give a surface height profile of the part. For small height variations, the linear portion of the difference characteristic can also be calibrated to yield a direct-reading profilometer.

As a test of the accuracy of the focus sensor, the surface of a one-inch diameter steel ball was measured. Figure 8 shows the result of a radial scan out to about 80 mils as compared with the curve calculated from the nominal ball diameter. The total scatter of the points has a variance of ±0.1 mil. The deviation of the points from the curve beyond 60 mils results partially from surface tilt, which is about seven degrees at this point. When a perfect mirror is measured, the scatter in the data is of the order of 50 microinches or less. Pressed steel electron gun parts tend to exhibit from 0.1 to 0.2 mils due, we feel, to surface roughness and, possibly, speckle noise. The results are clearly encouraging and development is continuing to improve both speed and accuracy.

Another form of out-of-plane measurement is the technique of optical triangulation shown schematically in Fig. 9. A light beam, either from a laser or a line source, is projected onto the surface at an angle. The line-scan camera system views the spot normal to the surface such that, when the surface is moved, the camera sees a lateral motion proportional to the line-of-sight

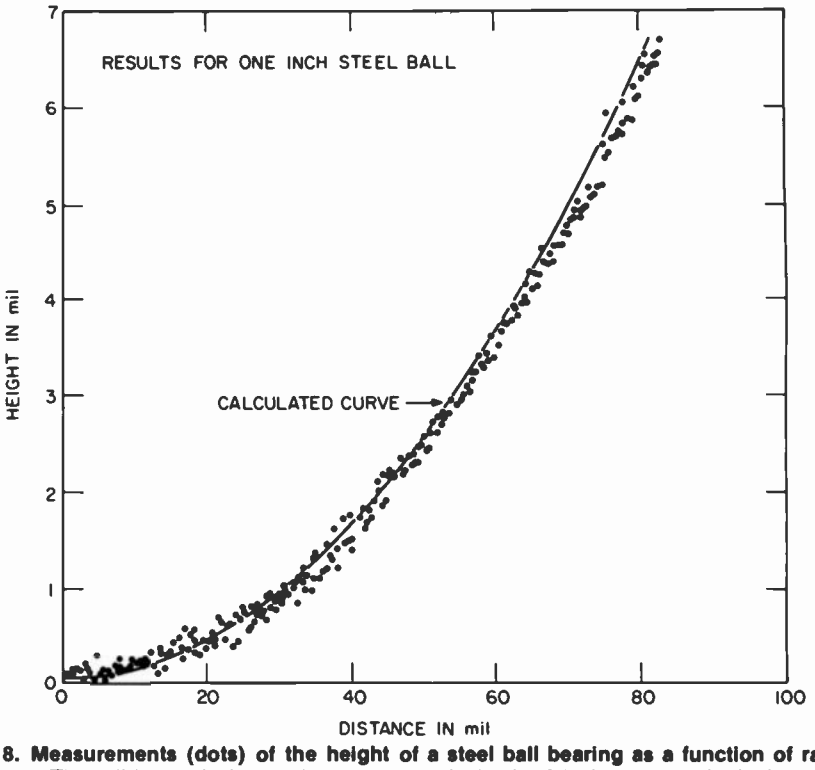

Fig. 8. Measurements (dots) of the height of a steel ball bearing as a function of radial distance. The solid curve is the result expected on the basis of the known one-inch diameter.

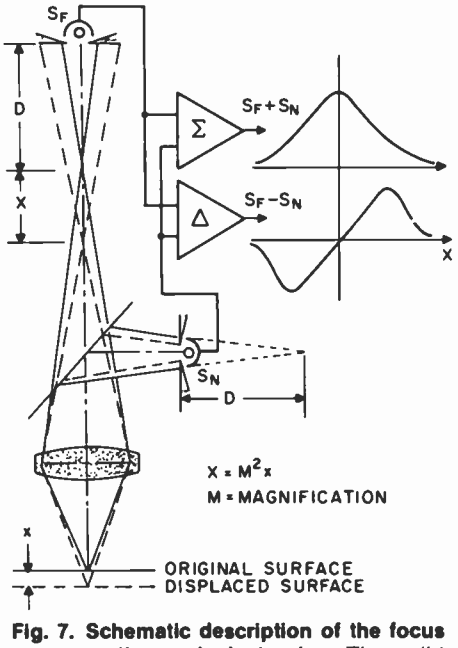

Fig. 7. Schematic description of the focus sensor optics and electronics. The solid lines indicate the light path in the balanced state; dotted lines correspond to a displaced surface.

displacement. This technique requires that the surface scatter sufficient light into the camera to obtain a signal. A highly reflecting, specular surface cannot be measured by such a system. If the surface is truly perpendicular to the camera axis and is planar over the region traversed by the light beam, the instrument can be made direct reading. More typically, the displacement signal is used to drive a servo system as was done in the focus sensor.

An extension of the optical triangulation technique is optical sectioning in which "sheets" of light are used in place of the single light spot or line, generating a series of lines on the surface which, when viewed normally by a matrix array camera gives the profile over a reasonable area very quickly. The sharpness with which the spot or line edges can be defined determines the ultimate limit to the accuracy of both triangulation methods.

Inspection methods

As a final example, we would like to discuss an ongoing experimental program which involves the inspection of shadow masks for point defects and so-called general non-uniformities. The human eye is very sensitive to slight variations in brightness. Note your ability to distinguish subtle changes in surface texture. As a result, all shadow masks are subjected to a critical visual evaluation to eliminate those which would cause any objectionable variations in picture quality. Most of us would be hard pressed to find the defects which trained personnel routinely weed out, at least those which they do when they are fresh and alert.

The new technique is based on results obtained in a multi-year investigation of the psychophysics of human vision at the Labs which shows that one can quantify a person's ability to distinguish differences between various displays by taking localized transforms of the scene, each of which selects spatial frequencies lying with an octave frequency band. A non-linear response function is then applied to each transform to determine its visibility to the observer. When properly summed, the response, so defined, gives a number which uniquely describes the perceived deviation from uniformity.

Using the above results as a starting point, we are investigating a mask scanner which appears capable of sorting out good from bad masks. As shown in Fig. 10, a series of scans is made across the shadow mask, 25 in this case. Recorded is the shadow mask transmission as measured through a Gaussian smoothing filter which eliminates the periodic effect of the slit openings. Were this not done, the "noise" from the individual slit openings would

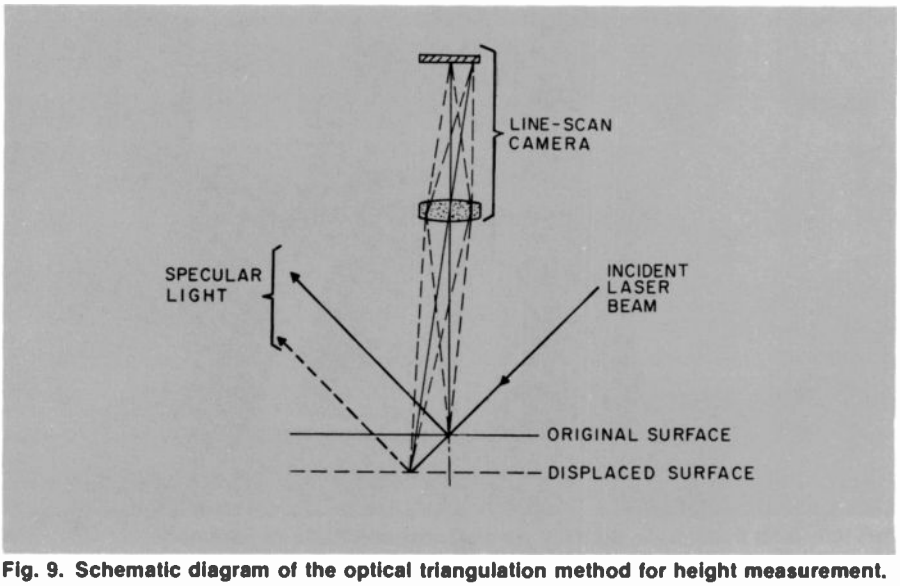

Fig. 9. Schematic diagram of the optical triangulation method for height measurement.

swamp the desired overall transmission response. Note that the scan for the bad mask shows a mottled effect when compared with the rather regular nature of the pattern for the good mask.

The data are analyzed by dividing the mask area into about 400 separate regions and calculating the perceivable non-uniformity in each region. The histograms plot the number of regions having different degrees of non-uniformity. The histograms are superposed on the left to emphasize the difference between good and bad masks. The single area with very high non-uniformity on the good mask corresponds to the partially blocked aperture visible in the middle of the scan.

When these data are properly weighted and summed, a quality factor can be defined which is capable of distinguishing

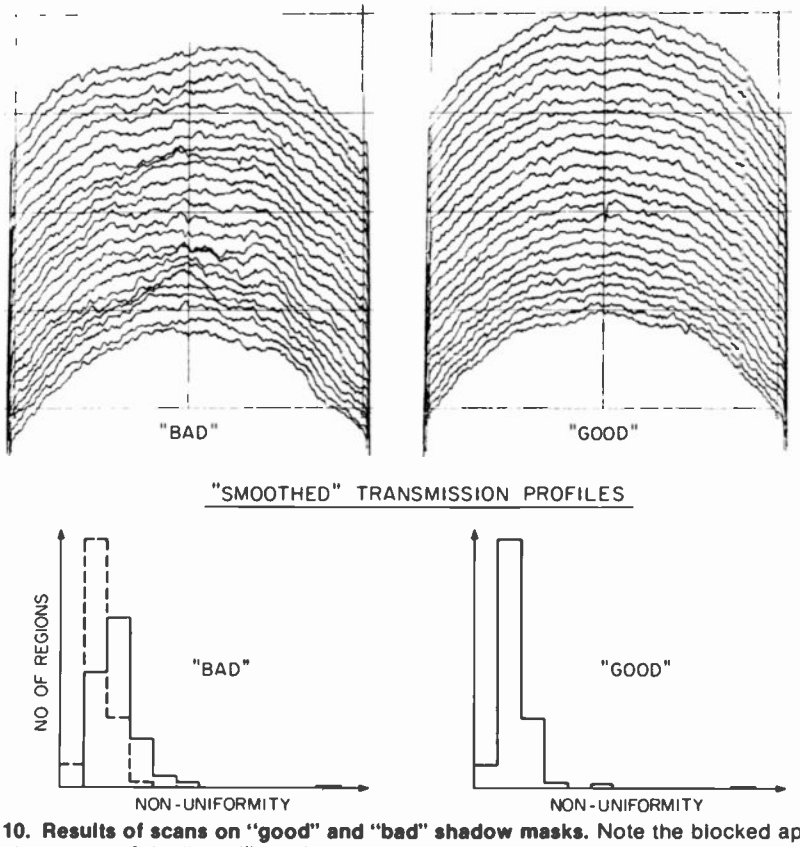

Fig. 10. Results of scans on "good" and "bad" shadow masks. Note the blocked aperture near the center of the "good" mask.

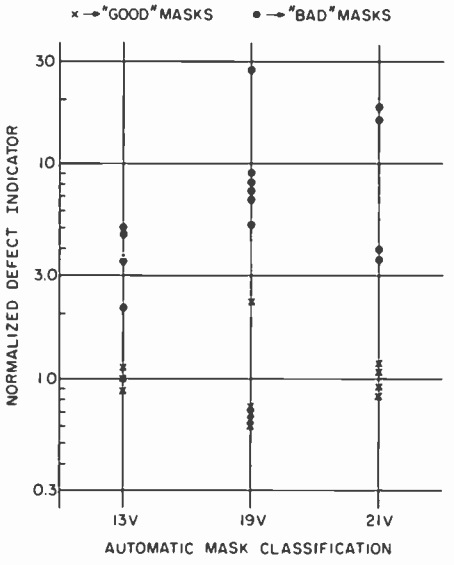

Fig. 11. Classification of "good" and "bad" masks for three different sizes.

between good and bad masks (Fig. 11). Note that the masks fall into separate "good" and "bad" groups. If these preliminary results hold up and means can be found to speed up the scanning and computing processes, this could be a significant new inspection technique. Its success is directly relatable to the fact that it uses an accurate model of the human visual decision process to define what will or will not be acceptable. This serendipity between the needs of manufacturing and research into the human visual system will hopefully yield other useful inspection devices in the future.

Summary

Prototype instruments have been designed and built at the Princeton Labs which use Reticon line-scanners to measure the widths of openings in a shadow mask; the widths of lines on a matrix kinescope cap; and to inspect the working plates used in mask exposure. Techniques are being developed to measure height variations of the metal parts used in electron guns to an accuracy of ±0.1 mil using auto-focus or optical triangulation methods. An ongoing program applies the results of psychophysical investigations of human vision to the automated inspection of shadow masks for non-uniformities in transmission.

Acknowledgment

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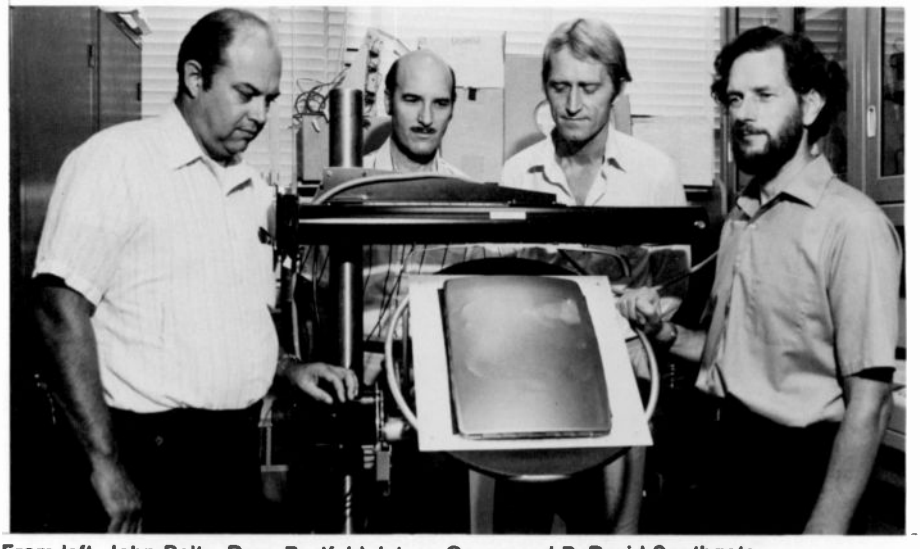

From left, John Beltz, Dave Bortfeld, Istvan Gorog and P. David Southgate.

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John Beltz joined RCA EDP Division in June, 1958 with the optical character recognition group. In 1968, John joined the Graphic Systems Division and helped to develop graphics capability on the photocomposition system. He has been an MTS at Princeton Labs since 1977 working on contact inspection systems and digital circuit design for manufacturing applications in PTD and VideoDisc.

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A. Schnapf
20 years of weather satellites—where we have been and where we are going—17th Annual Space Congress, Coca Beach, FL (5/80)

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M.J. Cantella|H. Honickman
J.D. Johnson|J.J. Klein|F.F. Martin
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J.C. Phillips
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Laboratories

R. Crandall
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H. Staras|L. Schiff
Efficient data transfer in an SS-TDMA system with a non-uniform traffic distribution—reprinted from *International Conference on Communications*, (6/80)

L.C. Upadhyayula
GaAs MESFET comparators for gigabit-rate analog-to-digital converters—*RCA Review*, Vol. 41, No. 2 (6/80)

J.L. Vossen|J.J. O'Neill, Jr.|G.W. Hughes
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Laboratories, Zurich

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Electric conduction in amorphous polymers—*Colloid and Polymer Science*, Vol. 258, No. 3 (1980)

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Investigation on the doping of polyacetylene films—*Journal of Electronic Materials*, Vol. 9, No. 4 (1980)

Missile and Surface Radar

C.N. Campopiano|R.S. Berkowitz*
Comparison of phase-only and conventional monopulse in thermal noise—*RCA Review*, Vol. 41, No. 2 (6/80)
*Univ. of Pa., Phila.

W.C. Grubb, Jr.
Mini computers and microprocessors for non-electrical engineers and solid state electronics for non-electrical engineers—ASME Meeting, San Francisco, CA (8/80)

D.R. Higgs
Technology quiz-written communications—*TREND*, Vol. 20, No. 3 (7-80)

W.J. O'Leary
SEASCAPE—A methodology for shipboard sparing strategy—Society of Logistic Engineers Annual Symposium, Pasadena, CA (8/80)

R.W. Ottinger
AEGIS technology program (U)—Tri-Services Radar Symposium, West Point, NY (7/80)

Engineering News and Highlights

Staff Announcements

Consumer Electronics Division

D. Joseph Donahue, Division Vice-President, Operations, announces the appointment of **James R. Smith,** as Director, Product Assurance.

Perry C. Olsen, Manager, Product Design Engineering, announces the appointment of **James J. Kopczynski** as Manager, Project Engineering; and the appointment of **Robert D. Altmanshofer** as Manager, Engineering, Juarez.

Bennie L. Borman, Director, Manufacturing Engineering and Technology, announces the organization of Manufacturing Engineering and Technology as follows: **Edward J. Byrum,** Manager, Manufacturing Programs; **Alfred Crager,** Manager, Test Technology; **Robert E. Fein,** Manager, Manufacturing Planning and Services; **Horst E. Haslau,** Manager, Equipment Development; **Charles J. Limberg,** Manager, Manufacturing Technology Center; and **Robert R. Russo,** Manager, Process Development.

P.G. McCabe, Manager, Plant Manufacturing Engineering, Bloomington, announces the organization of Plant Manufacturing Engineering as follows: **B.J. Caughlin,** Manager, Assembly Process and Tool Design; **J.V. Keith,** Manager, Test Engineering; **R.D. Orman,** Manager, Assembly Process and Tool Design; **A.M. Tinsley,** Manager, New Methods and Equipment Development; and **Q.O. Watkins,** Manager, Standards, Indirect Studies, and Material.

Laboratories

Robert D. Lohman, Director, VideoDisc Systems Research Laboratory, announces the appointment of **Paul W. Lyons** as Manager, VideoDisc Testing Center.

David Richman, Director, Materials and Processing Research Laboratory, announces the appointment of **Robert J. Ryan** as Head, Polymer Processing Research.

Brown F. Williams, Director, Display and Energy Systems, Research Laboratory, announces the appointment of **Thomas L. Credelle** as Head, Advanced Display Systems Research.

Bernard Hershenov, Director, Solid State Devices Laboratory, announces the appointment of **John P. Russell** as Head, Optical Device Concepts Research.

RCA Service Company

Raymond J. Sokolowski, Division Vice-President, Consumer Services, announces the appointment of **Joseph E. Steoger** as Director, Engineering Support.

Solid State Division

Carm J. Santoro, Division Vice-President, Integrated Circuits, announces the organization of Integrated Circuits as follows: **Marvin B. Alexander,** Manager, IC Operations Analyses; **Larry J. French,** Director, Photomask Technology; **Carm J. Santoro,** Acting Manager, Offshore Manufacturing; **Heshmat Khajezadeh,** Director, Bipolar and MOS Logic Operations; **Donald W. Laird,** Manager, IC Administration & Offshore Support; **John P. McCarthy,** Director, Government & Hi-Reliability Operations; and **Carm J. Santoro,** Acting Director, Memory, Microprocessors and Timekeeping Operations.

Heshmat Khajezadeh, Director, Bipolar and MOS Logic IC Operations, announces the organization of the Bipolar & MOS Logic IC Marketing as follows: **Andrew J. Bosso,** Manager, Marketing—Industrial Bipolar ICs; **James L. Magos,** Manager, Product Marketing—C-MOS Logic ICs; **Seymour Reich,** Manager, Product Marketing—Consumer Bipolar ICs.

Promotions

Americom

Raymond E. Dombroski, from Associate Member to Member, Engineering Staff, Technical Operations.

Robert Lukach, from Associate Member to Member, Engineering Staff, Technical Operations.

Laboratories

Arthur L. Greenberg, from Associate MTS to Member of Technical Staff.

Louis A. DiMarco, Macy E. Heller, and Joseph Zelez, from STA to Associate MTS.

Mark D. Jacobs, from TA to Senior Technical Associate.

John H. Morewood, from RT to Technical Associate.

Barbara J. Banko, from Managing Analyst to Manager, Business Systems Development.

Ralph DeStephanis, from Associate Member of Technical Staff to Administrator, Manufacturing Technical Programs.

Jeffrey R. Eldridge, from Technical Associate to Administrator.

Morris Chazin, Anthony R. Cooke, Walter M. Janton, John A. Kopen, Jr., Henry F. Milgazo, and Donald B. Wenner, from Technical Associate to Senior Technical Associate.

Picture Tube Division

Raymond L. Muenkel, from Member Technical Staff to Engineering Leader, Product Development.

RCA Service Company

Thomas J. Barry, from Manager of Systems Engineering to Division Vice-President, Field Operations.

John M. Leopold, to Manager of RCA Systems Engineering.

Professional Activities

Redfield appointed to energy unit

Dr. David Redfield, a scientist with RCA Laboratories in Princeton, has been appointed to a one-year term on the Solar Photovoltaic Energy Advisory Committee of the U.S. Department of Energy. The committee, which includes representatives from industrial, academic, and professional groups, advises the Secretary of Energy on research and development projects and on economic, technological and environmental consequences of the use of solar photovoltaic energy systems.

Dick Landers honored

Dr. Richard R. Landers has been presented a "1980 Annual Merit Award" by the Chicago Association of Technological Societies. Dick, who is presently RCA Satcom Product Assurance Administrator, was cited for his research in reliability, maintainability, and availability of complex systems (such as mine safety, missile, navigation, ocean, and space systems) and for his pioneering studies in self-repairing and self-sustaining systems.

GCS presents Technical Excellence Awards


Crowley


Lisowski

The Technical Excellence Committee at Government Communications Systems has presented two awards for outstanding and innovative accomplishments. The award winners and brief summaries of their citations are given below.

A.T. Crowley—for his highly innovative work in the design and development of the digital phase-locked-loop tracking system of the Survival Avionics DME. Al was responsible for both tracking loops in the system, the transponder loop, and the interrogator measuring loop. He wrote the track loop section of the proposal, including a theoretical analysis of the phase-locked-loop required to give the specified performance, designed and built the all-digital system on the resulting contract and made it work as predicted by his calculations. This tracking system required a measuring distance accuracy of 14 feet, had to use a narrowband signal compatible with standard military voice radios and have a round-trip measurement time of less than one second. The half duplex, interrogate/transpond system had to measure the signal frequency to an accuracy of 10^{-7} and phase to within 28 ns. In addition to meeting the significant technical challenge, Al beat a very optimistic program schedule by one month.

R.M. Lisowski—for his outstanding work in the design and development of the Distance Measuring Equipment of the AF Survival Avionics System. Bob evolved systems concepts for PSK/AM signal correlation to a realizable range determining system, designed and developed the control system required to perform the specified interrogate/transpond range measurement and peripheral functions, and was responsible for integration of the DME system components, including other contractors' radio equipments, into a fully operational developmental model system. His successful completion of the system concept verification, breadboard and developmental model stages in nine months was an extraordinary accomplishment. Bob's insight and creativity brought many novel solutions to the digital implementation problems to minimize the circuitry, reduce the size of custom LSI chips and realize a package meeting the maximum size requirement of two cubic inches.

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* Technical Publications Administrators, responsible for review and approval of papers and presentations, are indicated here with asterisks before their names.

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