RCA Engineer

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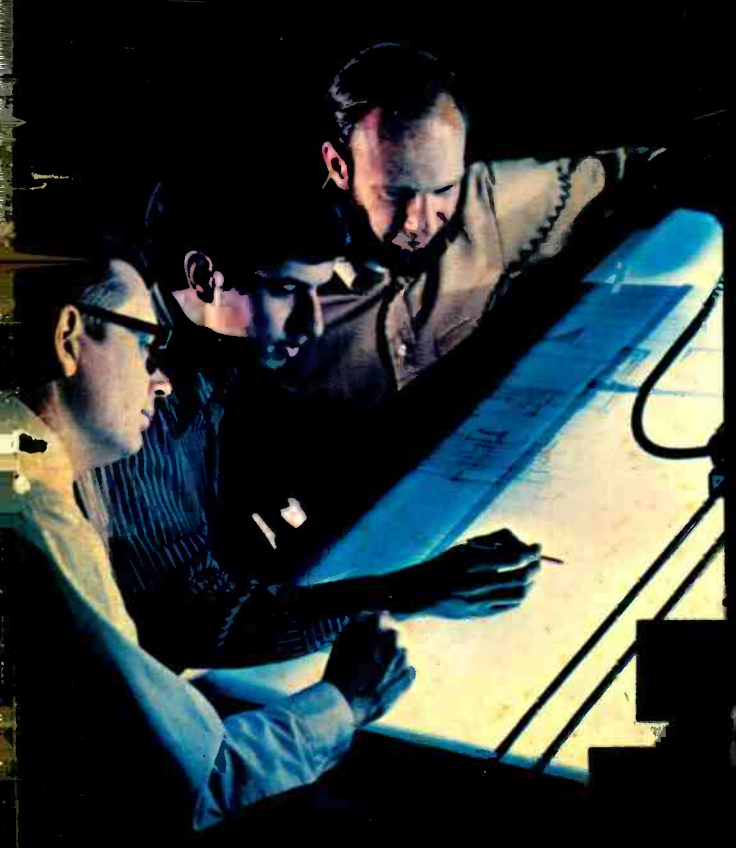

The computer — a design tool

For years, man has been using tools to increase his physical power. Steam engines, gasoline engines, electric motors, plus all their attachments and accessories for years increased man's productive capability.

Today, the computer is helping man to expand his intellectual power. The design of modern aircraft depends on computers for a stress analysis of the structures and engines; automotive engineers use graphic terminals on computers for styling designs; and modern complex integrated circuits depend on computer aids for circuit analysis and pattern generation.

Just as it took special training for workers to learn to use their physical power multipliers, it requires special training for engineers to learn to use computer design aids. It seems to be generally true that the more powerful a design aid tool, the more difficult it is to learn to use. Valiant efforts have been made by computer programmers to reduce the training needed to use their programs, but as in all compromises, something is lost in the process, either some of the capability of the tool or some of its economic effectiveness.

The papers in this issue are authored by people who have made special efforts to expand their intellectual capabilities through the use of computers. The tools that these papers describe are extremely important to RCA's electronics business, and to the engineers that have to deal with the design and use of electronic systems. While some of the papers may be difficult reading for those not familiar with the field, the reward is proportional to the effort expended. The authors are to be congratulated for the important contributions they are making.

Because these programs can only be used effectively by persons with some degree of special training, various groups in RCA have made efforts to provide that training. Advanced Technology Laboratories of G&CS in Camden has prepared valuable training tapes with assistance from the Corporate Engineering Education group. The SSTC Design Automation group in Somerville has given special courses on their Design Automation programs and has prepared a video tape that gives an overview of design automation. As a service group for the Corporation on I.C. design automation, this group in the SSTC can be helpful to all parties interested in using such tools.

G.B. Herzog
Staff Vice President
Technology Centers
Princeton, N.J.

Our cover

...pictures several steps in the computer-aided design process used at the Solid State Technology Center in Somerville, N.J.

Front cover: (upper left) Carole Benbassat; (lower left, l. to r.) Don Fraipont, Satya Agarwal, Chris Davis; (lower right, l. to r.) Steve Greenberg, Hans Schnitzler, John Forte.

Back cover: (top) Larry Rosenberg; (bottom, l. to r.) Dennis Polk, Dave Ressler, Barbara Korenjak.

All are members of the Design Automation group, Solid State Technology Center in Somerville, N.J. The activities shown are described in several papers in this issue (see Ressler, p.8; Rosenberg and Benbassat, p. 16; Korenjak, p. 20; and Benbassat, p.24).

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RCA Engineer

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• To disseminate to RCA engineers technical information of professional value • To publish in an appropriate manner important technical developments at RCA, and the role of the engineer • To serve as a medium of interchange of technical information between various groups at RCA • To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions • To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field • To provide a convenient means by which the RCA engineer may review his professional work before associates and engineering management • To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

Contents

Emphasis — Computer aided design

editorial input

computer aided design

Glancing back to the last CAD issue of the *RCA Engineer* (Oct-Nov 1968) adds a fresh perspective to the present issue. Beyond the differences in technology, the present issue shows a striking improvement and maturity in CAD concepts and methods.

The most significant trend has been toward making the interface between the computer and the designer easier to use and understand. Six years ago, Fortran was the key to many CAD packages. Today, high level languages allow the designer to communicate most design information to the computer *in design terminology*. Also, there has been a marked increase in the number and the quality of CAD packages available (some are listed below).

Another difference, perhaps more apparent to the Editors, is the amount of material available on the subject. Six years ago we had to "beat the bushes" to come up with the 60 pages devoted to CAD. The present issue devotes almost 80 pages to the subject, but many more papers were submitted than could be published because of space limits; these will be published in future issues.

One bothersome aspect of this comparison is that CAD is not yet being applied as widely as it should be. However, training programs have been developed (see Herzog, inside cover, and Friedman, p. 5), and CAD activities have been established throughout the Corporation to advise and assist designers in using the computer to improve design performance.

This issue identifies many such concentrations of CAD expertise. Use them.

--J.C.P.

Computer aided design programs

AEUP
AUTODRAFT engineers users program which minimizes the engineering effort in the development and verification of logic diagrams, schematics, and hybrid artwork designs.

AEWRAP
An automated logic wiring rule and backplane wiring program

AGAT
A program designed to generate complete tests for a combinatorial logic net.

ALACARTE
A system for entering IC or PC board artwork into a computer. (See Benbassat paper, this issue.)

APAR
Automatic placement and routing system which consists of several computer programs to aid in design validation, routing and testing, of digital logic. (See Zieper, DeMeo paper, this issue.)

APPLICON
An interactive graphic system for design and graphic editing of component layout, placement, and routing. (See Bauer paper, this issue).

ARTCON
Artwork-to-connectivity program which examines artwork looking for metal or diffusion tunnel connections.

ARTWORK
Software sequences which are required to produce artwork tapes or drive a checkplot facility.

AUTODRAFT
An automated drafting system which produces logic drawings on a flat-bed plotter from coded engineering sketches.

CRITIC
A design-rule checking program. (See Rosenberg, Benbassat paper, this issue.)

DFL
Design file language

ECAP
An electronic cirucit analysis program.

FETSIM
A batch program, written in FORTRAN IV, for dc and transient analysis of MOS circuits.

LECAPX
An interactive time-sharing program for rapid determination of circuit output parameters.

LOGSIM
A program which validates digital logic by dynamically simulating logic operation at the element level.

MANMOD
A software system which enables the user to intervene in the automatic placement of cells.

MAP
D.W. Mann tape preparation program.

OS ART
Artwork manipulating utility program on same machine as used for TSO ART (batch processing in background).

PLOTS
A data-capture language for CAD artwork. (See Korenjak paper, this issue).

PR2D
Two-dimensional placement and routing program which is used to place standard cells in various rows on the surface of the proposed chip and determine routing of connections.

R-CAP
A program for simulating the detailed electrical responses of electronic networks.

RECAL
Program which allows ac, dc, transient, and worst case analysis of linear circuits.

SIFT
A data-manipulation facility.

TESTGEN
An interactive program which tests sequential logic.

TICCIT
A time-shared interactive computer-controlled information tv system developed by MITRE Corp.

TSO ART
Time sharing option ART (see OS ART).

Future issues

The next issue of the *RCA Engineer* emphasizes engineering at RCA Parts and Accessories in Deptford, N.J., and also contains representative papers from other divisions. Some of the topics to be covered are:

Mini-State antenna
Car stereos
Indoor tv antennas
Four-channel sound
Solid state optical recording
Space Mountain
Building management systems
TWT's

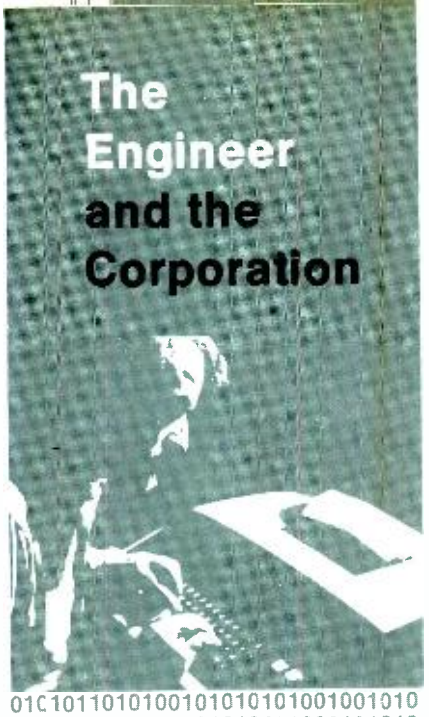
Discussions of the following themes are planned for future issue:

Automatic testing
Automated manufacturing systems
Manufacturing/Engineering design
Palm Beach Division engineering
Meadowlands engineering
NBC engineering

Meeting the computing needs of the engineering community

Dr. J. T. O'Neil, Jr.

This article discusses a 1974 study to establish a plan leading to more effective data processing utilization in RCA and summarizes the benefits that the initial stages of that plan will provide to the engineering community.



THE RCA Corporate Staff Computer Systems Planning department is presently concluding a study for developing a long-range data processing usage plan for the company. This effort was undertaken in response to many things including: 1) the multiplicity of relatively small and often overloaded computers in the company — seventy-two computers at forty-eight different sites, 2) the lack of a corporate-wide computer growth plan, 3) high EDP costs relative to RCA sales, 4) large and rapidly increasing use of outside computing services, and 5) the recent growth in the use of programmable calculators.

The study

The study began by developing a detailed questionnaire which was distributed early in 1974 and returned in March. This questionnaire covered current and projected workloads as perceived by the MIS community. Separately, assessments were made of the impact of future requirements in the manufacturing, operations research, and engineering communities. For example, instances where a sophisticated, powerful computing environment is required are described in this issue of the *RCA Engineer*.

Alternate plans for future optimal computer configurations were then developed, called Plan A and Plan B. Plan A proposed consolidation of almost all of RCA's continental U.S. computing operations into two large centers, one in the Midwest and the other in New Jersey. Plan B proposed that the computing operations of each major operating unit (MOU) be consolidated into a single center within that operating unit. The alternate configurations involved, for the subset of the RCA sites considered, two central sites and twenty-six remote sites (principally high-speed remote job entry, or RJE, equipment) for Plan A, and twelve MOU-centered sites and 16 remote sites for Plan B. The proposals did not consider a continuation of the current approach.

Also, no redistribution of the MIS department's essential applications support staffs was proposed. These groups plan and implement new or enhanced applications systems in close conjunction with the operating departments of the MOU; and this function is generally better served by being in close proximity to these departments. In fact, one major company is currently embarking on a "decentralization" program in which it is creating MIS departments at major locations, but retaining the centralized computer operations.

Following the development of Plans A and B, a Request for Quotation (RFQ) was prepared (more properly called a request for information) and a benchmark assembled and submitted to the major computer vendors for bids.

On June 17, 1974, proposals were received from Burroughs, IBM, and Univac. In spite of many specific constraints and configuration formalities in the RFQ, and the questions that followed, the responses were at wide variance. The details of the proposals, covering thousands of pages, are too voluminous to go into here, as are the details of our subsequent analysis and normalization, but many factors of general interest have surfaced and can be discussed here.

Findings

The findings cover several interrelated issues, including those of centralization versus decentralization, economy of scale, application centralization, and

some surprising facts regarding the dramatic erosion of cost effectiveness of the RCA Spectra 70 versus modern large-scale computing systems.

In resolving the centralization versus decentralization question, both Plan A (regional consolidation) and Plan B (MOU consolidation) were found to offer large savings over the current approach regardless of vendor. These savings could exceed $22 million over the seven-year period analyzed, including costs for converting programs to run in the new environment (estimated to exceed $10 million), plus additional costs for remote job entry equipment and high-speed communications which come to over $1 million annually.

Also, the cost differences between the responding vendors affected the results much less than the differences between Plans A and B. It is noteworthy that these cost differences significantly understate the actual value to RCA of the new approach since many intangible and indirect benefits over continuation of the Spectra approach were not quantified. These benefits would include the "value" of having more reliable equipment, of having easy access to a wide variety of applications packages, of being able to attract, develop, and retain top-notch computer professionals, and many others which ordinarily would be sufficient in themselves to justify a data processing decision. Engineers regularly wrestle with such justifications in the use of the corporate procedure for computer acquisitions, resulting occasionally in some highly creative efforts. In the corporate computer study, however, no such requirement arose since a new approach presented both an opportunity to save money and an opportunity to "do things better."

Thus, it seems that economy of scale favors large-scale equipment, at least for RCA's mix of computing requirements. This is indeed true in general of most applications now done on Spectra 70. But, there is another end of the computing scale, called variously, "smart terminals", microprocessors, minicomputers, programmable calculators, etc. These devices have not yet achieved much penetration in RCA, except for some research and engineering activities, but are projected to be the fastest area of growth in the future.

These devices are forerunners in what is believed to be an evolving "distributed computing" concept, in which computer usage occurs in a wide variety of specialized applications remote from central data processing, but connected over communications links to central data bases and high-speed data processing. Such an environment requires powerful and sophisticated computer equipment with a capable and responsive systems support staff. One conclusion of the study is that RCA's increasing use of shared data processing will provide exactly this environment and computing economies as well.

Another discovery is that some of the former differences between engineering (or scientific) computing and commercial (MIS) computing are disappearing within RCA. Scientific computing applications are benefitting more from access to large, up-to-date, and perhaps structured data bases (as seen in this issue); and commercial applications will, in turn, benefit from access to powerful central processors. None the less, engineering does continue to play a leadership role in RCA, first in the use of minicomputers, then with electronic calculators, and now, somewhat suprisingly, in the use of modern data base management techniques. This desire for and acceptance of change is a key factor in the generation of productivity improvements in engineering.

Action

Many items emerged from the study, resulting in vendor policy and other internal policy changes. In summary we have:

1) Fundamentally, a multi-vendor policy with internal standards,
2) A strong management commitment to explore the shared processing opportunity,
3) Agreement to upgrade the Cherry Hill data center to the status of a corporate shared-data processing center by adding large-scale IBM equipment, in addition to continuing use of the current Univac equipment, and
4) Initial participation in the new facility by the Missile and Surface Radar Division of Government and Commercial Systems and the RCA Laboratories.

This initial combination of users will provide both strong MIS and engineering thrust to enhance the capabilities of the center and will provide a hospitable environment for the additon of either major user groups or individual users who wish to use the center.

Dr. John T. O'Neil, Jr., Director, Computer Systems Planning, Corporate Staff MIS, New York, received the AB in Mathematics from Princeton University, Princeton, New Jersey in 1960, and the PhD in Computer Science from the University of Pennsylvania in 1970 after completing his dissertation on "An Interactive Language Design System". Dr. O'Neil joined Honeywell in July of 1960 and then came to RCA Laboratories in March 1963, where he worked in the Applied Math Research Group in numerical analysis. In 1964 he was awarded a David Sarnoff Fellowship and spent the 1964-1965 academic year at the University of Pennsylvania. For the next five years he worked in various areas of systems programming research. In 1966 he received a Laboratories Achievement Award for the design and implementation of an E.O. Simulator and Assembler. His subsequent research was centered around the theory and implementation of compiler and compiler writing systems. In 1968 his META PHI compiler writing system led to another RCA Laboratories Achievement Award. For this work he received the David Sarnoff Outstanding Team Achievement Award in Science in 1969. In the following year he became head of the Languages and Mathematics Research group, which subsequently was enlarged and became the Advanced Systems Research group. In his present capacity as Director of Computer Systems Planning, he is responsible for computer planning, software planning, and division plans and administration for Corporate Staff MIS.

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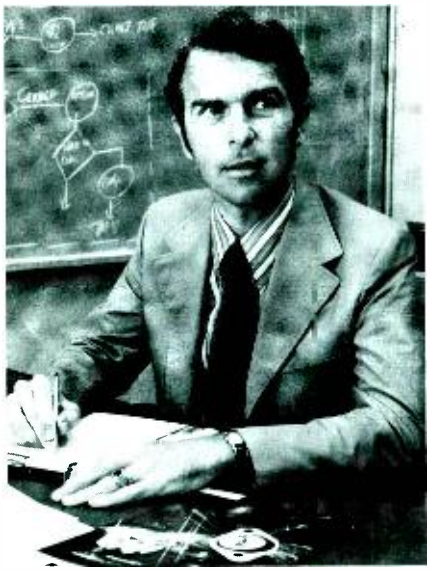
Final manuscript received October 21, 1974.

Computer aided design training courses

J.E. Friedman

The computer is now recognized as a cost effective aid to engineering design.[1] A lesser known component of computer aided design is the effort underway at RCA to formalize the learning process of the engineer in his interaction with the computer. An appreciable amount of the growth of computer aided design is effected by a series of training courses. These range from "hands on" sessions with equipment to video supplemented classroom environments.

THE PARTICULAR FORM of the training activities in computer aided design changes from year to year to reflect developing technology. Thus, a major requirement of any training course must be relevance. The following courses were selected for discussion because they should be viable at the time of printing for this issue.



Reprint RE-20-4-12
Final manuscript received August 15, 1974.

John E. Friedman, Leader, Engineering Communications, Advanced Technology Laboratories, Camden, N.J., received the BS in Engineering Physics from Lehigh University and has pursued further engineering and communications courses at RPI, NCE, St. Joseph's College, Fairleigh Dickinson University, and Rutgers University. Prior to joining RCA in 1966, he worked for the Bendix Corporation as a gound support systems project engineer for four years and for the General Electric Company as a technical editor at the Valley Forge Space Sciences Laboratory for six years. During his active service with the U.S. Army, he served as a junior physicist at the Fort Monmouth Electronics Command. Mr. Friedman has written articles on communications problems for the IEEE Transactions on Professional Communications and the STC Technical Communication journal.

APAR system

At the large-scale integrated circuitry level for this type of training is the course on the automatic placement and routing (APAR) design automation system. This system was developed by Advanced Technology Laboratories, Camden, to make more immediately available to RCA engineers the metal gate CMOS technology (in LSI form) of the Solid State Division. The course is structured around six video tape lessons, a volume including the lesson visuals and text of the spoken commentary, a set of recommended supplementary readings, and a laboratory workshop. The course begins with a treatment of the user's perspective, noting that the design of computers is no longer the only objective of this type system. A broad spectrum of RCA products exists that can now utilize this technology. These include digital communications and security devices, automotive electronics, and data bus systems for aircraft and submarines.

In the product design cycle, the basic beginning elements are a concept, production needs, and technology rules. This leads into system design and finally to the point of subsystem identification. The designer is then ready to identify plug-in cards and LSI chips. These chips are the equivalent of a rack of discrete equipment. At this time the APAR cycle comes into the process (see Fig. 1). As to implementation of LSI hardware, APAR stands opposite the totally customized approach in which the engineer specifies placement of each element on the array.

Following the overview and user's perspective session, succeeding lessons treat designer fundamentals, circuit simulation aids (FETSIM), logic simulation aids (LOGSIM), generating of test sequences to evaluate the arrays (AGAT, TESTGEN), and the two-dimensional placement and routing program and the artwork programs which translate designer information into process instructions (PR2D). See Fig. 2. Further discussion on APAR is given in the article in this issue by H. Zieper and A. DeMeo.

Applicon system

Operation

In cooperation with Applicon, Inc., RCA has video taped an Applicon instructor giving a brief classroom and "hands on" course in operation of this computerized graphic design system. A *User Study Guide* is also available. The Applicon method is a minicomputer-based ap-

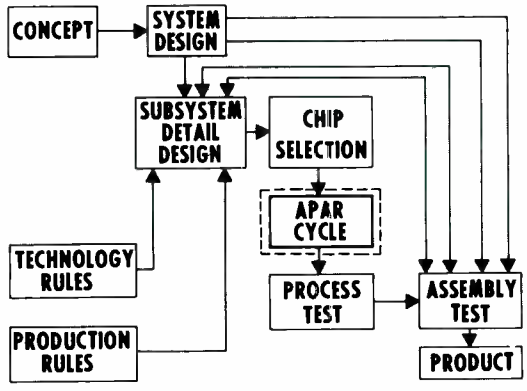


Fig. 1 — Product cycle and APAR.

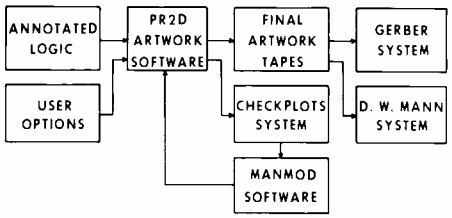


Fig. 2 — System structure.

proach to handling engineering drawings. The Applicon system is organized so that the user, either engineer or draftsman, can operate four basic modules of work performed in the design-drafting cycle. *Input* is the creation or conversion of drawing information. *Processing* is the changes, calculation, and connections performed on a drawing. *Data base* is the method of automatically storing and retrieving both active and inactive drawings. *Output* is the producing of finished drawings, artwork, or data. Special software requirements can be fulfilled by a programming option that allows the user to utilize either FORTRAN or assembly language to work with the drawing data. Typical input modes include digitizers, data table and stylus (sketchpad), and digital data stored on punched cards, paper tape, or magnetic tape. Once drawing data has been entered into the system it is automatically stored as a self-contained file.

The interactive capability of the Applicon System allows the designer to work directly at an editing station to call up drawing details and give new input via the console keyboard or the hand-held data stylus. The designer can get instant computation or check and approve work being processed. Once processing has been completed on a drawing it is returned to the data base for storage—either on line or off line. On-line data can be stored on a disk system for fast access to a full library of drawings. Off line, magnetic tape systems or cassette units can be used. In addition to conventional drawings, Applicon system output also can take the form of film positives or negatives as artwork masters or silk screen originals, microfilm or microfiche, magnetic tape, or paper tape. With the training programs which include the video tape, average time for operator training is two weeks.

RCA applications

The Applicon system has been installed and operating at locations such as Somerville, Moorestown, and Princeton for over a year.

An ever increasing number of personnel have been trained from all the Government and Commercial Systems divisions and the Solid State Division. A new course has been incorporated in the 1974/1975 Engineering Education catalog Applied Program section, "AC1 — Interactive Graphics for Design Engineers." As noted in the catalog, any RCA location can make additions to this basic user course for their specific applications.

An AUTODRAFT Engineers Users Program (AEUP) has been developed to establish the Automated Backplane DA System for engineers as an economical design tool. It can be used to minimize the engineering effort in the development and verification of logic diagrams, schematics, and hybrid artwork designs. It can also identify the cost effectiveness of inputing data by utilizing a set of standard formatting rules. The Automated Backplane Design Automation System has two possible raw data inputs with outputs of AEWRAP net lists, interconnect lists, routing lists, manufacturing documents, and Applicon checkplots. This training program has been presented to more than fifty engineers at the Missile and Surface Radar Division. AUTODRAFT has since been utilized for data capture and logic diagramming on two major radar systems.

Design directly by the operator at the terminal has been developed for small to medium assemblies and has been implemented at MSRD for thick-film hybrids, printed circuit boards, and microwave structures. The libraries for each have been developed at MSRD. The thick-film hybrid techniques and library have been demonstrated to all divisions and distributed to the Solid State Technology Center and to Burlington Operations of Government Communications and Automated Systems Division.

Complex printed circuit boards for interconnecting ECL 10,000-series circuits have been developed by fixed matrix layout given by the engineer and copied on Applicon. Editing of automated routed logic diagrams and hybrids and digitized entry of data has also been implemented in conjunction with Burlington Operations, Astro-Electronics Division, and Solid State Technology Center. More detail on Applicon is given in this issue in the article, "Experience with Interactive Graphics," by J. Bauer.

Design automation artwork systems

The Design Automation group of the Solid State Technology Center has assembled a series of sequential courses which were first presented in February and March of 1974. These courses provide user training for the DA Artwork Systems. Also, course participants are expected not only to utilize the systems efficiently but also to help train new members of their respective departments. The courses included in this set are PLOTS, ALACARTE, CRITIC, Operating the Digitizer-Plotter System, EAI Plotter Operators Course, and Advanced Digitizer-Plotter System.

The Basic Artwork Entry (PLOTS) course familiarizes the user without computer experience with the PLOTS language and syntax. Users are taught how to apply the basic concept of translating IC artwork patterns into a form necessary for computer interpretation and processing, how to write and edit artwork files of PLOTS language statements, and how to use the specific options of each PLOTS statement as applicable to their group's IC technology. The course consists of an overview and explanation of Design File Language, familiarization with basic PLOTS language statements and rotation, application to actual artwork, basic editing of data files, advanced usage of PLOTS, and review of formal usage of

each PLOTS command type. About one-third of this course is spent in "hands on" laboratory time using the NTSS (new time sharing system) at Princeton. The text for this three-day course is the PLOTS Users Manual.

The next course in the sequence, ALACARTE, enables the user to create artwork files using a digitizer (Graf/Pen) supported by the ALACARTE program, transfer these files to other systems for error checking or further processing, and use the ART program to checkplot, SIFT (a data manipulation facility), or modify an artwork file. The course time is divided equally between instruction in the principles of operation and laboratory time entering and editing artwork. Prerequisites for this course are a working knowledge of PLOTS and/E (interactive editor) on NTSS.

The brief course (1/2 day) on CRITIC, a design rule checking program, provides the basic instruction necessary to apply CRITIC to the user's particular technology. The user learns to identify particular pathologies or pattern situations of his design, to write the proper CRITIC test or control file descriptions for a circuit, and to interpret the results of a CRITIC output.

The course in operation of the digitizer-plotter system is structured to train the user without computer experience to be a production digitizer. The user learns to operate the PDP-8 console and peripheral devices that compose a DPS system, to digitize and edit artwork files, to create and place library elements, to modify existing artwork files, (to check plot and error check them), and to utilize the basics of SIFT. In this 5-day course, training is divided about equally between classroom instruction and laboratory time.

In the EAI Plotter Operators course, the objective is to provide detailed instruction in the operation and maintenance of the EAI/430 flatbed plotter. A working knowledge of PLOTS and the SIFT command is a prerequisite for this one-day course.

A three-day refresher course, Advanced Digitizer-Plotter System, is also offered for previous DPS operators.

A more comprehensive treatment of these systems is given in the article in this issue by D. Ressler.

Table I — Contacts for further information about specific courses.

Course	*Contact*	*Location*	*Phone*
APAR	H. Ingraham	Central Engineering Bldg. 17A3-1 Camden	PC-3335
Applicon	G. DiGirolamo	Engineering Education Bldg. 204-2 Cherry Hill	PY-5141
DA Artwork	L.J. French	SSTC Somerville	2371

Perennials

For many years, the engineering education programs in various divisions have offered CAD-related courses in their catalogs. Most recently in Camden and Moorestown for example, two widely used computer aided circuit design programs were treated in an after-hours course. LECAPX is the latest revision of an interactive time-sharing program for rapid determination of circuit output parameters. ECAP is more versatile and can handle nonlinear devices as well as more complex transient situations. Also in the perennial category are the software courses such as FORTRAN Programming. This type of course provides the engineer with the skills required to plan, flow chart and code simple Fortran programs for the solution of engineering problems, or to formulate a complex engineering program into terms suitable for transmission to a professional computer programmer.

Courses of this kind should be available well into the future with no sign of abatement in their value to engineers at appropriate levels of experience.

For further information and administrative details on running the specialized courses discussed in this article, refer to Table I which lists appropriate contacts.

Future of CAD training

Immediately related areas of expansion planned for course work include a silicon-on-sapphire technology application of APAR, additional DA Artwork courses in TSO and OS ART System, TSO and OS CRITIC, MAP (D.W. Mann tape preparation program), PDP-11 ART System, R-CAP, and Test Data Analysis.

At the time of this writing, many of the Design Automation courses were scheduled to be video taped in the Fall of 1974. They should be available throughout the corporation now from Engineering Education or in the near future.

Several of the courses discussed here can be loosely classified as computer-assisted instruction (CAI). However, in the strictest definition, CAI is a technique of individualized instruction with the main feature of learner control. Although learner-controlled instruction does not require a computer, M.M. Loftin claims it reaches its greatest level of efficiency with the computer.[2] One future possibility then is the combination of the presently developing CAD techniques with the CAI systems which are transferring from campus to industry. The first step in RCA has already been taken toward automated instruction in the form of video tapes. Applicon, with its interactive designer/editor console, is not very far removed from TICCIT, a time-shared interactive computer-controlled information television system developed by MITRE Corp. Implementing the mechanism to bring this instruction to a greater number of engineers and designers at low cost, with learner control, may be the next decade's challenge for the computer in RCA.

Acknowledgment

The author wishes to thank Dr. W. Underwood and Mr. D. Higgs for supplying materials helpful in the assembling of this article and Mrs. B. Korenjak and Mr. J. Bauer for technical comments.

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Simple computer-aided artwork system that works

D. G. Ressler

A complete, computerized artwork processing system for integrated circuits and printed-circuit boards includes digitizers, plotters, a design-rule checker, and a pattern generator command program. Its success depends on simplicity, consistency, and technology independence.

David G. Ressler, Ldr., Artwork Systems, Design Automation, Solid State Technology Center, Somerville, N.J., received the BS in Chemistry in 1960 and the BSEE in 1963 from Rutgers, and the MSEE from the University of Pennsylvania in 1965. He joined RCA Laboratories in 1963 as a participant in the Research Training Program, where he studied light deflection in electrop-optic crystals. After developing several computer programs for circuit analysis at the Laboratories, Mr. Ressler joined the Solid State Technology Center in 1969. Mr. Ressler is a member of Phi Beta Kappa, Phi Lambda Upsilon, Tau Beta Pi and Eta Kappa Nu

Reprint RE-20-4-11
Final manuscript received August 21, 1974.

THE NEED for computer assistance in handling precise, complex artwork for various industrial processes has spawned a number of different systems designed to input, edit, and prepare artwork with varying degrees of human interaction during the process. The system described here for processing integrated circuit artwork was begun when there were fewer commercial systems available than there are now. In the five years since its introduction, this system has matured such that the Solid State Division of RCA uses it in the production of its COS/MOS circuits, as well as for many of the other solid state devices it manufactures.

The initial objectives in our system development work were:

- Reduce turnaround time for integrated-circuit design from that for the manual strip-film photoreduction method of preparing artwork;
- Handle large circuits while maintaining good image definition in all areas of the mask.
- Handle and remain abreast of several rapidly-developing technologies.
- Develop a system usable by many different people with varying backgrounds and training levels;
- Make available error-checking facilities beyond those techniques used in a manual system; and
- Allow easy expansion into different areas of artwork processing — for example, printed-circuit board artwork.

Using as guidelines a precise set of principles — simple data base, consistent user commands and procedures, and generality instead of technology dependence — we were able to develop a system that has met these objectives. In its present form, the system is characterized in Fig. 1 where the major components and their various functions are indicated.

To further explore the system, let us consider first the system command language and data base upon which it operates. Then we'll discuss the various system components, focusing on the Digitizer-Plotter System, which is the main data input device used. Finally we will discuss why such basically straightforward system concepts result in a successful system.

Basic PLOTS-DFL artwork language

The entire artwork system is based on a very simple text-oriented language called PLOTS and its computation-oriented counterpart called Design File Language (DFL). The human operators of the system always think and act in terms of PLOTS language statements, which are the same on all the different computers involved in the system. The artwork processing programs, however, operate on the information in the PLOTS language only after it has been converted into DFL. This conversion is done to ensure computational efficiency for each type of machine upon which the programs are run.

The PLOTS language[1] is used to describe the figures comprising the artwork for an integrated circuit or printed-circuit board. These figures are expressed in a rectangular coordinate system. Reference can be made to absolute coordinates and to relative coordinates in the directions Right, Left, Top and Bottom. For example, consider the PLOTS statement

P X2Y2 TO X6Y3 T5 L4 B6

This describes a polygon with one corner at (2,2) and another at (6,3), T5 means Top for a relative distance of 5, so a third corner would be at (6,8). Similarly L4 (Left 4) puts a corner at (2,8) and the B6 (Bottom 6) brings the side back to the starting corner. In the finished artwork described by this statement, the interior of the polygon would be dark on a light field.

PLOTS can describe many-sided Polygons with sides going in any direction, as in this example. Also included in its repertoire are Orthogonal polygons, whose sides are parallel to the x- or y-axes; and fixed-width segmented Lines which can go in any direction. The various layers (or levels) needed in the

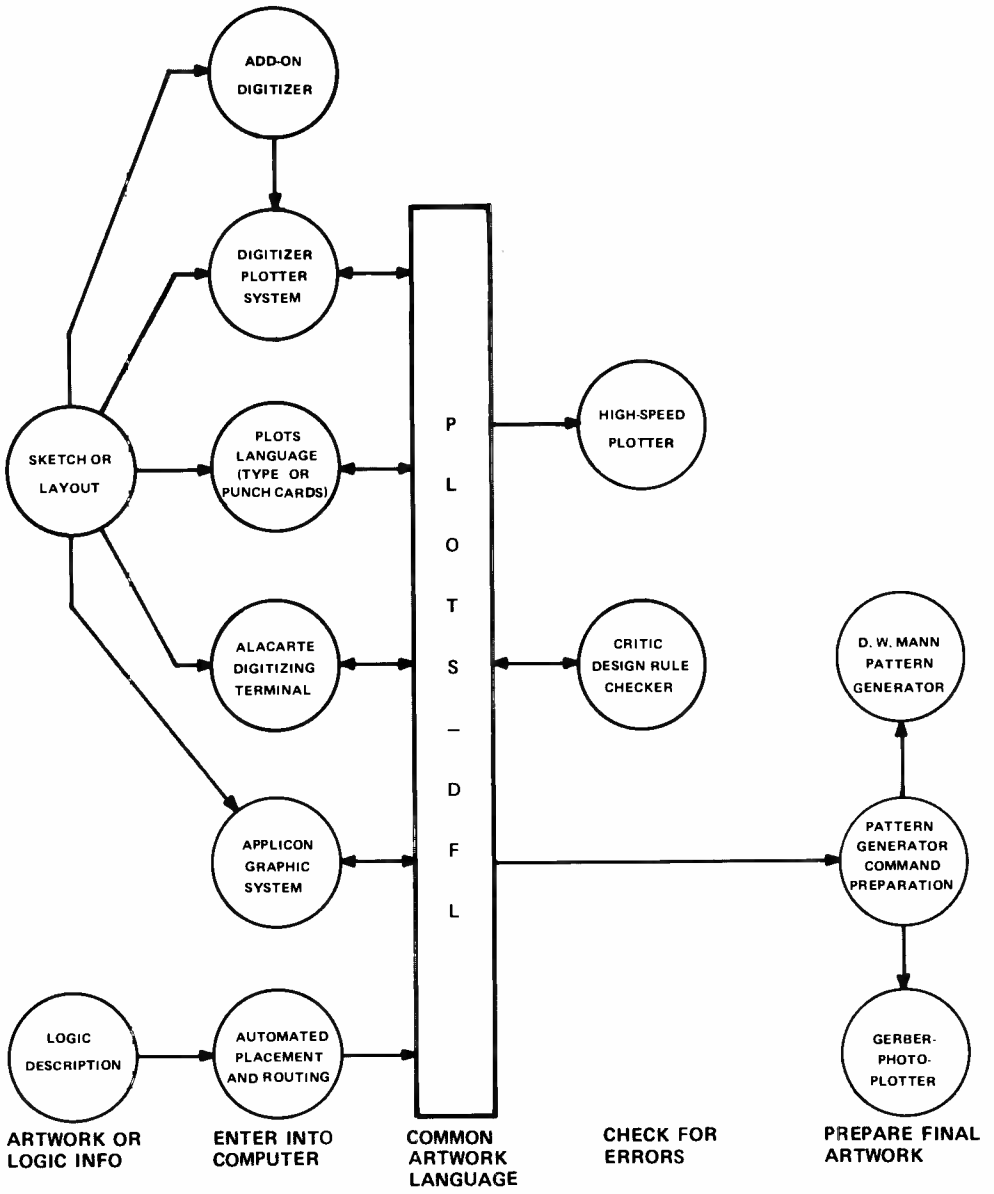


Fig. 1 — Components of RCA automated artwork system.

production of integrated circuits or printed-circuit boards can be kept separate using Mask level statements.

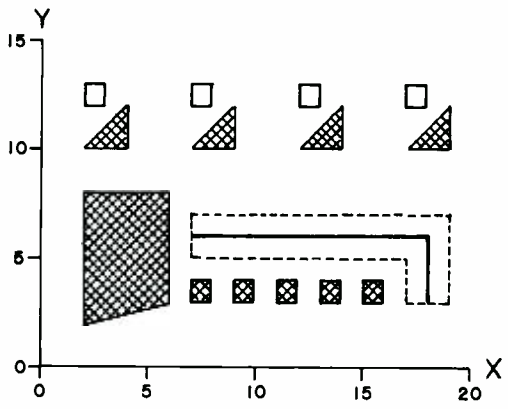
An important feature of PLOTS is the library structure, a structure somewhat like Fortran subroutines calls. It is used to replicate a given set of PLOTS statements one or more times. To invoke a library call, the operator initially enters a series of PLOTS statements to be replicated and encloses the statements within a Definition statement and End statement. Then Q statements can be entered to specify — for each replication — the location, the rotation (one of eight possible 90° rotations and reflections) and the scale factor. Fig. 2 is an example of the artwork generated by a series of PLOTS statements.

System description

The PLOTS language and DFL serve as the basis for all the various computer systems involved in automated artwork. These systems can be classed according to their general function.

Input and editing

Three different digitizers and two CRT graphical editors comprise the means for initially describing artwork to the automated artwork system and subsequently modifying the digitized artwork; in addition, a direct keyboard entry of PLOTS statements may be used for artwork description. Of the three digitizers available, the workhorse is the minicomputer-based Digitizer-Plotter System (DPS). The two other are digitize-only systems and are lower cost alternatives to the DPS; one of these systems, ALACARTE, is described in Ref. 2. Of the two graphical editors, one is a refresh display device developed at RCA Laboratories; the other is a commercially purchased storage tube system which was interfaced to PLOTS-DFL



Plots statements	*Explanation*
M 1	Beginning of Mask Level 1
P X2Y2 TO X6Y3 T5 L4 B6	Polygon explained in text
O X7Y3 R1 T1 L1 B1 AND 4R2	Square appearing 5 times
M 2	Beginning of mask level 2
W 2	Sets width of lines to 2
L X7Y6 R11 B3	Line shown with width dashed around it
D 1 X0Y0	Start of definition No. 1 — reference at (0,0)
M 1	Start mask level 1 inside definition
P X0Y0 R2 T2 TO X0Y0	Triangle — relative to definition reference
M 2	Start mask level 2 inside definition
O X0Y2 R1 T1 L1 B1	Square above triangle
E	End of definition No. 1
Q 1 X2Y10 AND 3R5	Calls definition No. 1 four times and puts definition reference at (2,10), (7,10), (12,10) and (17,10)

Fig. 2 — Artwork generated by PLOTS statements (level 1 crosshatched).

with some considerable but worthwhile effort.

Checkplotting

Any DFL file can be plotted on one of several plotters available to the users. Since the DPS has complete plotting software, two systems are connected to large, fast flatbed plotters which produce most of the plots used for visual inspection (but never final artwork preparation). Magnetic tapes to drive off-line plotters can also be produced by system programs operating on large computers in batch mode. No matter which program a user runs to produce a checkplot, the command he gives is the same for all programs.

Error checking

Error checking is one function of an automated artwork system where the improvement over a manual system is dramatic. With limitless patience, the computer can find errors in drawing files which have escaped the scrutiny of an experience human checker.

The CRITIC error-checking program[3] processes DFL files and tests each figure according to a given plan defined in a control file. The possible tests are:

- Minimum width of a single figure.
- Minimum separation between two figures, subject to various qualifications (most common of which is "touching or overlapping is acceptable").
- Several different "coverage" criteria, where one figure should be covered by another on a different layer of artwork.

Pattern generating

The physical result of all the previous functions is a set of photographic patterns used to manufacture a device. These patterns are produced on a pattern generator from commands created from the contents of a DFL file. The transformation from DFL to the commands required by a particular pattern generator requires some sophisticated processing, since DFL describes corners of figures but generators must fill these figures in. This is not a difficult task in the case of constant-width lines and figures with orthogonal sides. However, when sides are not at right angles, computational complexity and pattern generator running time skyrocket. As a solution to this problem, a special algorithm developed at RCA Laboratories has permitted efficient handling of such figures.

Another complexity occurs because non-simple polygons are allowed (holes inside otherwise-solid figures). These must be specially processed before filling is begun. The steps followed by the processing program in preparing pattern generator commands from DFL are:

1) Produce a temporary file with all library calls (Q statements) fully expanded according to the appropriate definitions.
2) Separate the orthogonal part of Polygons from the part with slanted sides for more efficient filling.
3) Break down all figures containing inner holes into two or more simple figures without holes.
4) Fill all figures, producing commands for D. W. Mann Pattern Generator or Gerber photoplotter. Use a simple fill algorithm for orthogonal figures; a more elaborate one for non-orthogonal figures to optimize pattern generator running time.
5) Sort pattern generator commands for further optimization of pattern generator running time.

Digitizer-plotter system

The Digitizer-Plotter System (DPS) was the first artwork system to be developed using DFL and PLOTS. It has served as the model for all other artwork systems since it contains the capability for all essential functions: input, editing, checking, plotting, and file manipulation. The configuration is shown in Fig. 3.

The digitizing table used is a CalComp 502 30×34-inch flatbed plotter, on whose pen assembly is mounted a small light which projects a cross-hair on the drawing near the pen position. A closeup of this is shown in Fig. 4. The entire hardware system is under control of a program which runs on a PDP-8 computer. The program causes the pen-crosshair assembly to move in response to a user-operated joystick for digitizing, or from disk-stored data for plotting. A storage tube display with movable cursor is also available to the user as an alternative digitizing-plotting device. The program constrains coordinates to a grid of the user's choice, and a digital display

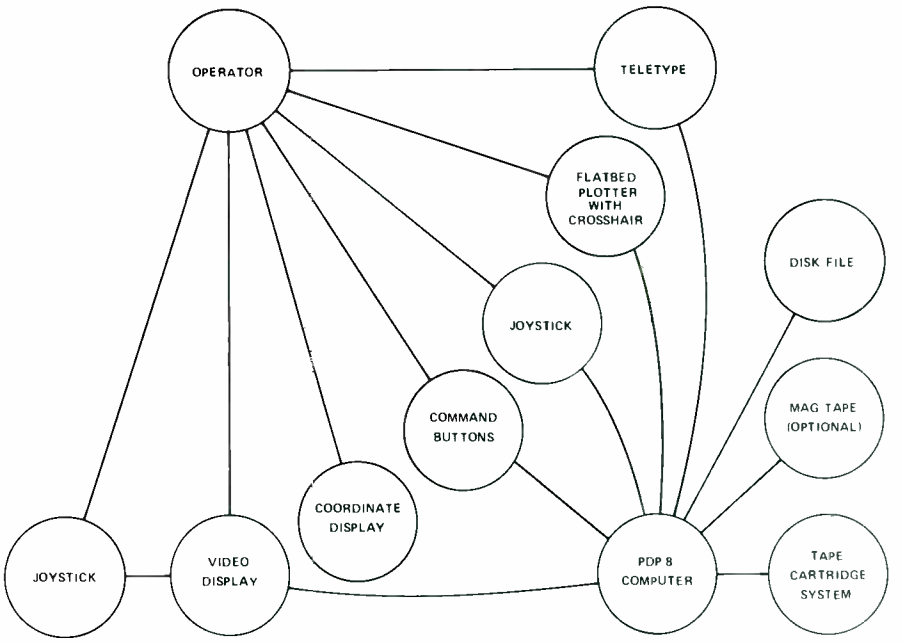


Fig. 3 — Digitizer-plotter system configuration.

shows the current location of the digitizer pointer.

In typical operation, the user mounts his sketch or drawing on the bed of the plotter and uses several Teletype commands and the joystick to register the drawing position with the computer. He then uses Teletype commands, appropriate command box buttons, and the joystick to digitize the data. For example, pointing the crosshair at a point and pushing a button on the joystick enters the coordinates of the point into the computer.

As each figure is digitized, the user may plot it back to check for correctness. In addition, he may change the digitized data using a complete set of editing commands. He can also plot the complete file or any subset of it on the flatbed plotter or on the storage tube display.

Keys to success

The strength of the artwork system described here does not depend upon pushing the state of the art, software sophistication, or unique hardware configuration. Rather, we feel that the success of the system stems from three principles which have guided its development: simplicity favored over computational complexity, consistency of language and command structure, and independence from specific user technology.

Before discussing these principles in detail, we should point out that their importance depends on the environment in which the system is used. In our case, many users with widely-differing talents operate the various programs for many different purposes. Some design tightly-packed integrated circuits for large volume production using standard technologies. Some are developing new IC technologies. Some are occasional users with simple functions to be performed; others are fulltime operators with a considerable amount of practice. Among the technologies represented are bipolar, MOS, COS/MOS integrated circuits, power devices, hybrid circuits, special solid-state devices, and discrete components.

Simplicity *vs.* elegance

Nothing is so pathetic as a powerful tool unused for lack of an understanding of how to use it. We discovered early in the development that a confusing command structure and language layout would render a system impotent. People would simply ignore the capability associated with the confusion. We therefore adopted some guidelines for the commands used to operate the programs: they are in the form

Verb Filename(if any) Arguments(if any).

The verb is chosen to be as descriptive of the function as possible. Abbreviations of verbs and arguments are always the first few letters of the full word. Blanks delimit; special non-alphabetic and non-numeric characters are avoided. Some typical commands are given in Table I (using person's names for filenames):

Fig. 4 — Digitizer-plotter system light pointer and joystick.

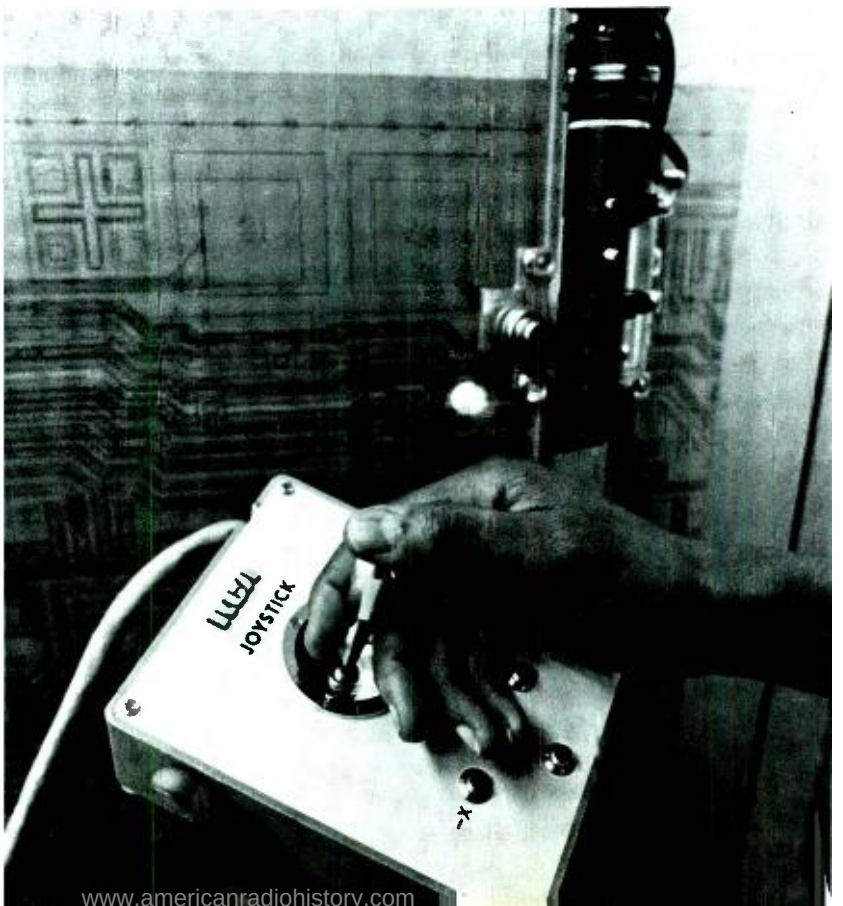


Table I — Typical commands.

Typical commands	*Explanation*
EDIT JOE	Edit the file named JOE.
CHECKPLOT FRED 3,4	Plot level 3 and 4 only from file FRED.
PREVIEW JUDY	Expand library call on plotter for inspection. Find definitions in file named JUDY.
SCALE 500	Set plotter scale factor to 500:1.
SEARCH POINT X3Y5 (M 1)	Search for figure with point at (3,5) on Mask Level 1.
SURVEY .1 JOHN	Type out vital statistics of file named JOHN. Notify if any points are not on a grid of 0.1 unit.

A question-and-answer format was ruled out because, in an elaborate system, the questions would be too complicated. We felt that using a system this complex would require an operator skilled enough to give commands without prompting.

Similarly, the PLOTS language used to describe artwork was designed for simplicity of use rather than sophisticated power. This precluded elaborate data structures and powerful but mystic abbreviations in favor of a straightforward, easy-to-comprehend structure. PLOTS was cast in a format easily handled by the user. The statements are sequential and their syntax is tightly controlled and consistent throughout. Only one kind of hierarchy is allowed: library calls, and these may be nested to a depth of nine layers.

These constraints are not without their cost. We estimate that about 80% of the effort by the programmers is spent making life easy for the user as opposed to actually processing artwork. The response by the users has vindicated our judgment, however—especially when our diligence lapses and we watch users back away from what we have made too complex.

Language and command consistency

The artwork system now consists of seven major programs operating on four completely different types of processors — some minis and some maxis. Some of these programs run on all four processor types in more than a dozen separate installations. Although some minor variations are dictated by the limitations of particular systems, a command to perform a particular function is the same no matter which system is being used. For instance,

```
CHECKPLOT JOE 3 INFRAME X3Y10X15Y30
```

will produce a plot of mask level 3 from file JOE, limited to figures inside a rectangle with diagonal corners at (3, 10) and (15, 30). On the Digitizer Plotter System, the plot will be on the flatbed plotter or storage tube; the PDP-11 system will display the plot on the graphic terminal. The time-sharing system will send commands over the phone line to a terminal plotter, and the batch version of the program will produce a magnetic tape for an off-line plotter—all in response to the same command. This approach aids users in moving from one system to the next. It also means documentation is consistent over all systems.

Technology independence

Aside from demands for more system time, the most frequent requests from users are for quick ways to support some specific technology being developed. These requests are hard to resist, especially since they usually involve an appealing programming challenge. We weigh each request initially, but have found that most are never implemented on the system because the users generally find some other way to accomplish their purpose within the existing framework of the system. Of course, if the ground rules call for large number of similar designs in a stable technology, the decision could swing the other way.

Conclusion

No single portion of the artwork system described here represents a new concept. To be sure, the CRITIC and MAP programs do contain relatively sophisticated routines for optimization, but the system is really successful mainly because the components all "hang together". The simple data structure allows users to get the feel of working with the system relatively quickly. However, the skilled user can almost always get what he wants by putting together the right tools and techniques. Training is simplified because all the different systems are covered by a course in any one of them.

What is said about the users is also true about the system programmers. Eight people are actively programming within the system. A great deal of interaction is possible because everyone is using the same set of library routines and the same simple data base. New programmers become accustomed to the system quickly, and special-purpose programs can be put together easily because of a large store of common routines.

The development of the principle on which the system is based was in some ways as much good fortune as good judgment. In our case, this system was the first project of a new and growing group, so the basic concepts were formulated by two individuals. This naturally avoided simultaneous development of system components which didn't fit together. For the same reason, since manpower was limited, straight-forward computational approaches were the only way results could be obtained in a reasonable amount of time. Further, the system designers were not pulled from the community of potential users, so the system design did not follow the natural tendency toward technology dependence.

The success of the system is evidenced by the fact that in the past four years integrated circuits in a half dozen different technologies have passed through the system. Since 1972, RCA's COS/MOS line has used the system for quick turnaround, accuracy, and reliability.

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Unified CAD data base system

A.H. Teger

To integrate existing CAD programs as a nucleus for future growth, a unified CAD data base has been implemented for storing the design data needed by many different types of CAD programs. This paper describes the data base, and an IC-oriented design system that integrates the data base with a new common input language and existing logic simulation, test generation, placement and routing, and artwork programs. Approaches for using the system and initial reactions from experimental users are described.

COMPUTER AIDS are dramatically enhancing the design process by providing engineers with more cost-effective tools for creating and evaluating their designs. However, as the number and complexity of such design aids grow, problems arise. Each CAD program usually has a unique input language, library, and internal data storage. Thus, the designer must take the time to learn each input language and, even worse, must specify the particular design (often with much redundancy) for each program he desires to use. This is quite a common occurrence; for example, circuit connectivity (*i.e.*., net information) must be given in different forms for logic simulation, test generation, and placement and routing programs.

If the results of one program are to be used as input to others, a new interface program could be written for each program to be run. As the number of CAD programs increases, the number of these interface programs becomes unreasonable. Furthermore, engineering changes to a design cannot be reflected back through programs run earlier in the design process to determine the validity of earlier results without respecifying the design to each such program.

To alleviate these problems, the Advanced Systems Research group at RCA Laboratories has been designing and implementing a unified data base capable of storing the design data needed by many different types of CAD programs, as well as a common input language to capture input data for all these programs.

CAD data base

The data base has been designed to be technology independent and, therefore, could be the nucleus of CAD systems aimed at printed circuit boards, backplanes, and hybrid circuits, as well as IC chip designs. To test the data-base

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Alfred H. Teger, Head, Advanced Systems Research, RCA Laboratories, Princeton, New Jersey, received the AB and BSEE from Columbia University in 1961 and 1962 respectively. He joined RCA Laboratories as a Member of the Technical Staff in 1962. RCA awarded him a David Sarnoff Fellowhsip for 1964-65, and he received the MS in Computer Science from the University of Pennsylvania in 1965. Mr. Teger has been involved in various facets of computer-aided design since 1965. He received an RCA Laboratories Achievement Award in 1966 for contributions to the development of automated artwork generation for integrated circuits, one in 1969 for a team effort in creating an interactive graphic system for CAD, and another in 1973 for a team effort on hierarchical data base structures. He assumed his present position in 1973, and is currently directing research in industrial and scientific computer systems and applications, including computer-aided-design systems, microprocessor-based data communications systems, and several minicomputer application systems.

concepts and their cost effectiveness in a production system, we have implemented a system aimed at integrated circuits and, in particular, at COS/MOS LSI design. Keep in mind that many of the programs are already applicable to other technologies, although they are described here in terms of the initial IC-oriented system.

The heart of the data base lies in its ability to store information related to a circuit's logical structure and to its physical realization. In terms of logic structure, a design consists of a group of logic functions (gates, flip-flops, *etc.*) and the interconnections between them (logic connectivity). Net lists are an example of this connectivity information specified in terms of the pins of the logic elements. The data base is capable of storing the connectivity hierarchically — *e.g.*, designing a register from gates and flip-flops, then using the register as an element in a counter, then combining the counter with other elements in a yet larger design, *etc.* A given element (*e.g.*, a register) need be entered and stored only once, although it may be used many times.

The physical realization of the circuit can be stored in the data base in a similar way. The design consists of a group of physical parts, each of which is an occurrence of a standard integrated-circuit cell from a library accessed by the data base, plus the interconnections between these standard cells (physical connectivity). The standard cells and the interconnections are usually given in terms of the artwork needed for the IC masks, as opposed to a symbolic net list as used in the logic representation. The physical design can also consist of hierarchically defined members in order to permit a building-block approach to design.

A flexible and efficient data base management program called IDMS (Integrated Database Management System) was purchased from B.F. Goodrich Company to aid in data storage and retrieval. IDMS provides mechanisms for defining the various data types needed for the CAD application, and for describing the relationships between them. It also contains a data manipulation language for accessing or modifying the data from an application program. We have found IDMS to be an effective tool for creating a data base tuned to CAD, although it has applicability to other areas as well.

IC data base system

The IC-oriented data base system integrates existing logic simulation, test generation, and placement/routing programs developed by G&CS, the artwork and design-rule checking programs developed by SSTC, and the new CAD Data Base and Language described here.

Two basic kinds of design approaches are readily handled by the new system: one in which the system is used before mask artwork is generated, and one in which artwork is the main input to the data base.

In the first case, the designer enters the connectivity for his circuit in the CAD language. If he starts from a logic diagram, he enters logic connectivity using the language. If he is beginning a design that will use the automated placement and routing program, PR2D, his logic diagram is already partitioned and annotated in terms of PR2D physical cells, and he specifies the connectivity between the pins of the PR2D cells (physical connectivity). In addition, the language gives him a macro-like definitional capability for hierarchical design. With either physical or logical connectivity, the CAD language statements are fed to the Language Processor and the connectivity is stored in the data base (see Fig. 1).

The data base has access to the appropriate standard cell library (*e.g.*, the PR2D library), augmented with the logic function equivalent of each standard cell. After the connectivity has been captured in the data base, the user can request extract programs to create input files for LOGSIM, TESTGEN, and PR2D. The output artwork from PR2D can be processed by the checkplotters, editors, high-accuracy plotters, and design-rule checking programs available through SSTC. An inquiry program can be called to produce net lists from either logic or physical connectivity for checking purposes or for documentation. Note that the designer need enter his circuit description only once, yet he has access to any of the above programs; as a result, much redundant error-prone input is eliminated.

In the second design approach, artwork has been manually generated. It is desired to input the artwork to the data base to verify that it performs the intended logic function, or to generate a sequence of test patterns for the IC testers. The data base is initialized with an appropriate standard cell library including the logic function equivalent for each standard cell and, in addition, including labels for the input and output pads of the standard cells.

The user enters his artwork file (in SSTC's DFL format) to the ARTCON (artwork-to-connectivity) program, which examines the artwork looking for metal or diffusion tunnel connections between the standard cells. The program accumulates these connections, and stores the complete physical connectivity in the data base.

The connectivity captured in the data base can be verified by using this inquiry program to output net-lists. In addition, LOGSIM and TESTGEN can be run under user command. In some cases, this will permit hardware simulation to be replaced by software simulation driven directly from mask artwork.

For some COS/MOS standard cell designs, it may be desirable to use a combination of both approaches. First enter the logic connectivity via CAD language statements, and verify the logic by using LOGSIM and TESTGEN. Then, if desired, the layout can be done manually with the resulting artwork entered to ARTCON to produce the physical connectivity. All that is then necessary to validate the artwork is to have a program compare the physical and logical connectivity and see if they are identical. We are currently developing a comparison program to perform this function.

Operational status

All programs in the data base system are currently operational in an experimental mode on SSD's IBM 370/158 computer, under TSO (time-sharing) and VS2 (batch). Where possible, the user is given the choice between quick turn-around time-sharing and lower cost batch. Most portions of the system are relatively inexpensive to use. The cost of running the extract programs and language processor are insignificant compared to the cost of using PR2D or LOGSIM. The one exception is ARTCON, where we are

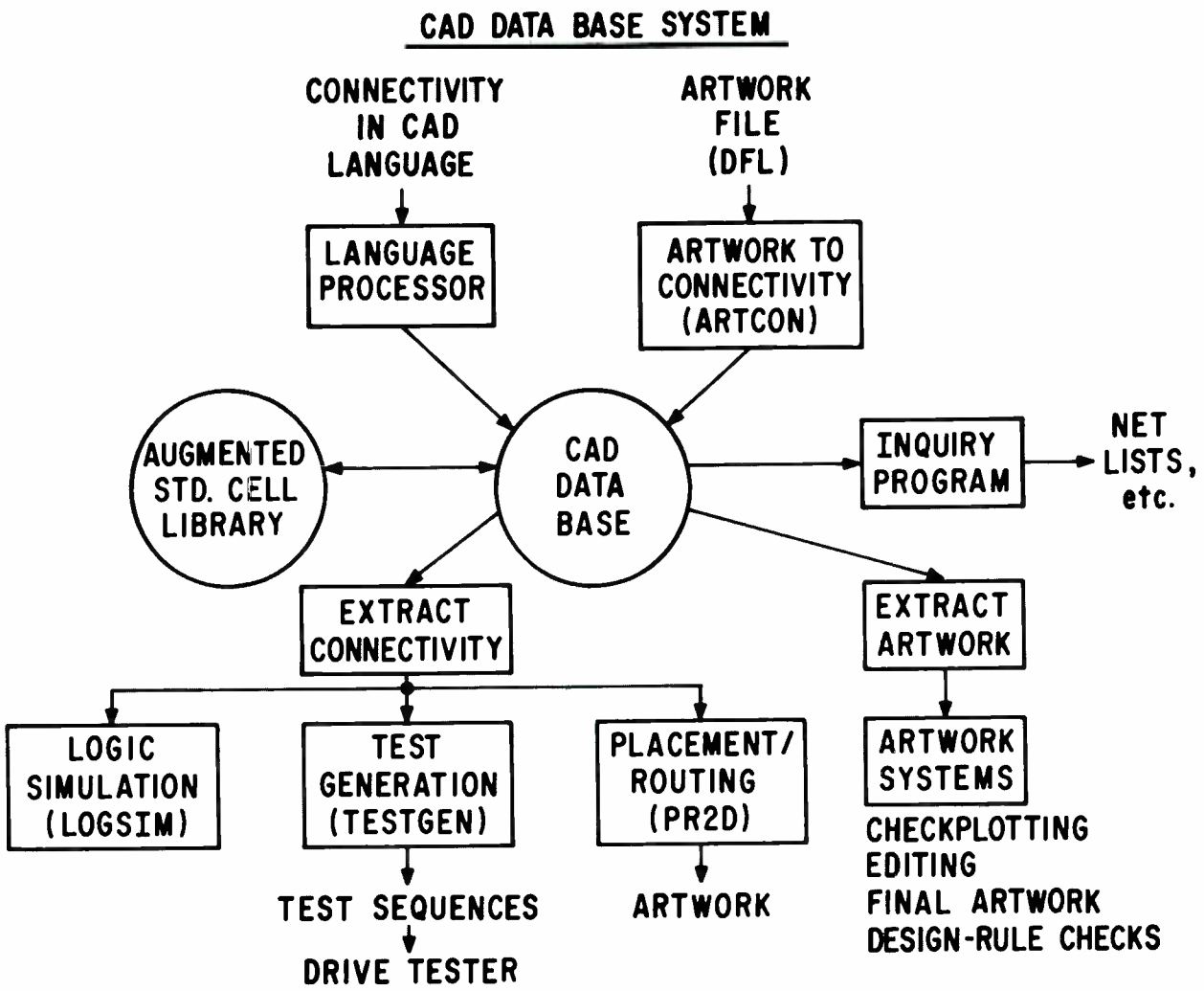

Fig. 1 — CAD data base system concept.

still optimizing the program to reduce running costs. At this point we are hoping to achieve ARTCON runs in the $100 to $200 range for a COS/MOS Universal Array TCC040. A full evaluation of the cost effectiveness of the system is currently being conducted.

From a human engineering viewpoint, we have received positive comments on the system from our experimental users. The language, in particular, appears easy to learn and to use.

Conclusions

The CAD data base system described here is meant to be only an initial system. However, it does demonstrate the feasibility of using a unified data base with a flexible data structure. Redundant input, with its additional costs and errors, can be eliminated. Multiple interface routines between programs can be reduced dramatically.

As production usage of the system grows, more programs will be added to the basic group described here. For example, capturing and storing the artwork for a logic drawing would require no changes to the data base structure. With connectivity stored in the data base as well as artwork, many new kinds of design validation checks are possible, and will be included as they are developed.

The data base should become a nucleus for growth of new CAD programs, providing the design engineer with tools that are easier to use; it should also give him greater flexibility in his design, and produce error-free results faster than previously possible

Acknowledgments

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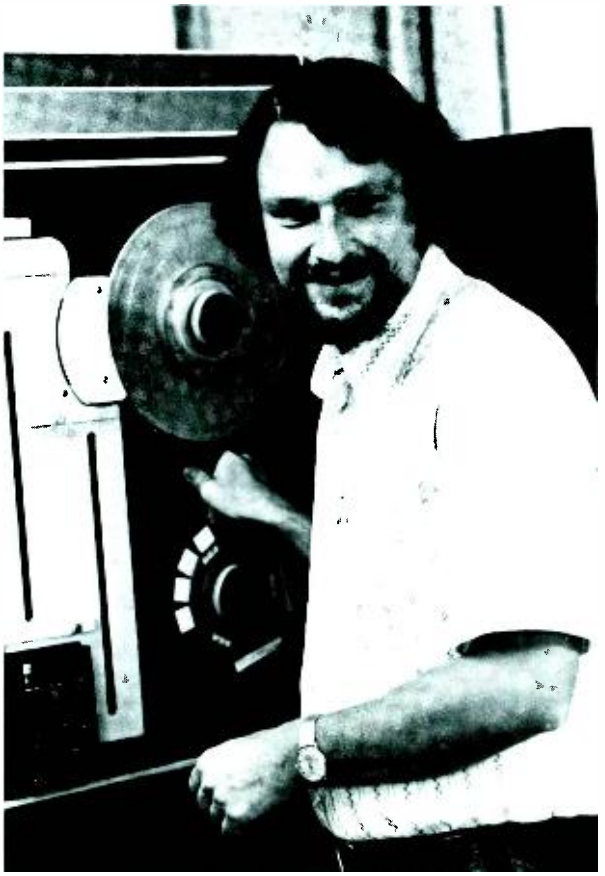
CRITIC: a program for checking integrated-circuit design rules

Dr. L. M. Rosenberg | C.A. Benbassat

CRITIC is a production-proven design-rule checking program which can perform minimum width, minimum clearance, minimum enclosures, and other geometrical relationship tests for artwork figures on the mask level or between different mask levels.

Dr. Lawrence M. Rosenberg, Design Automation, Solid State Technology Center, Somerville, N.J., received the BSEE (*summa cum laude*) from the Polytechnic Institute of Brooklyn in 1964 and a PhD from the Device Physics Group of the Electrical Engineering Department of Princeton University in 1970. His dissertation subject was the "The Detectability of the Quantum Size Effect by Tunneling Spectroscopy." Mr Rosenberg co-authored the paper "Double Injection in Insulators: Further Analytic Results" with Professor M. Lampert of Princeton University which appeared in the *Journal of Applied Physics* in January, 1970. He has had various summer projects involving Device Physics at Brookhaven National Laboratories (1964), General Electric Research & Development Center (1965) and Xerox Research Center (1966). He joined the Design Automation Group in RCA's Solid State Technology Center in October, 1970 and is concerned with transistor circuit analysis programs, MOS and bipolar transistor modeling, and with automated integrated circuit design rule checking. He is a member of IEEE, Tau Beta Pi & Eta Kappa Nu.

Carole Benbassat's biography and photo appear in her other article in this issue.



THE GROWING COMPLEXITY of integrated circuits has motivated the development of CAD programs to help pinpoint potential errors in the integrated-circuit artwork. This has become extremely important because of the large loss of time and money that occurs when an artwork error is found after an IC is manufactured. More subtle and perhaps even more serious is an undetected non-castastrophic violation of a design rule that reduces IC manufacturing yield and therefore needlessly increases cost over a long period of time.

A computer-aided approach is quite natural for this application because of the huge amount of tedious work involved in IC artwork checking by human eye and the relative geometrical simplicity of most design rule checks. Experience has proven that even the most careful checking of artwork by eye misses many potential errors.

A design rule checking program called CRITIC (Computer Recognition of Illegal Technology in Integrated Circuits) has been in active production use at RCA for over two years, particularly for COS/MOS, PMOS and SOS integrated circuits and also for high-speed bipolar IC development. CRITIC is capable of checking design rules involving geometrical properties of figures (such as minimum width) and interrelationships (such as minimum clearance, minimum enclosure, and one figure inside another). It can perform these checks for figures on any number of single mask levels or between figures on different mask levels. It should be pointed out that the program is general and could also be applied to technologies other than integrated circuits, such as printed-circuit boards.

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CRITIC is very valuable in a dynamic IC production environment, because specific design rules applicable to a particular technology are not "built into" the program. Instead, the program has the capability of performing a number of general geometrical tests which can be combined in different ways to perform the required design rule check. Specific sets of design rules can be specified in a compact manner and stored in a data file called a control-file. A user need only specify the name of a control-file to CRITIC to invoke that set of design rules. Alternatively, the user can specify a customized set of design rules for a special application by means of an interactive question-and-answer session.

It is also noteworthy that CRITIC runs on a DEC PDP-11 minicomputer with 28k 16-bit words of core. The economics of a minicomputer is particularly appealing because of the large CPU time required for performing design-rule checks on artwork for large ICs. The program was designed to employ heavy use of integer arithmetic to take advantage of the PDP-11's fast integer arithmetic capability. Recently the program has been converted to run on Univac Series 70 computers (70/45, 46,60,61) under the TDOS batch system and VMOS time sharing operating system and also on IBM series 370 computer (models 158, 165) under OS and TSO.

For persons not intimately familiar with computer-aided design rule checking, two problem areas should be identified. Since each artwork figure is usually represented by a set of coordinate pairs, it is not easy to gain perspective about spatial relations from these numbers and therefore it is not obvious, at first glance, how to perform geometrical tests such as minimum width and minimum clearance using only this list of numbers. This point may be appreciated by noting that humans almost never think in terms of rectangular coordinates. Another problem is created by the large number of figures, in the order of $N = 10{,}000$, in a typical IC. Further, it should be noted that a single minimum-clearance design-rule check could involve on the order of N^2 individual clearance tests. Clearly the algorithms employed must be very efficient in addition to having spatial perspective.

A number of different approaches are possible, and different ones have been employed in other programs.[1,2] We shall describe here those employed in CRITIC.

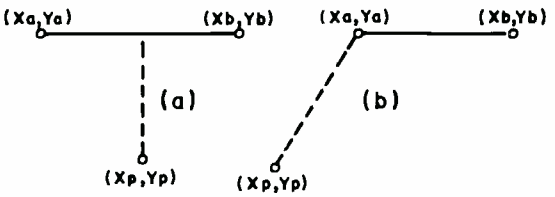

Fig. 1 — Test for minimum distance from a point to a line segment.

CRITIC's capabilities

CRITIC is written in a modular building block structure in which two basic geometrical functions are combined in different ways to create more sophisticated checking capabilities.

There are two routines at the heart of CRITIC. The first calculates the shortest distance from a point to a line segment (see Fig. 1). The second determines whether a point lies inside of, on a side of, or outside of a figure. Using these as building blocks, the program has other routines to calculate minimum width of figures, minimum clearance between figures and to test for certain geometrical relationships between figures such as whether one figure is inside of, outside of, or touching another figure. These capabilities may be used separately or combined in various ways to perform a desired test. These various checking capabilities will now be described.

Minimum-width checks

CRITIC can check that all figures on a given mask level have at least some specified minimum width. This test can be performed for any number of different levels. The user specifies each level to be checked and its associated minimum width criteria.

The program checks for minimum width by calculating the distance from each vertex of a figure to all its other sides and compares this calculated distance to the specified minimum. The thin line segments in Fig. 2 show some of the calculated distances. This algorithm will rigorously discover all minimum width situations if the sides of the figure are straight lines. The fact that many of the distances calculated have little to do with "width" does not affect the rigor of determining the minimum width as these "spurious" distances are generally greater than the minimum width. The exceptions can be easily eliminated and will be discussed later. In addition, special techniques can avoid most of the spurious calculations.

Note that a minimum-width check involves only one figure at a given time.

Relation checks

CRITIC is capable of performing a number of different tests involving two figures at a time. These are referred to as "relation checks". The most basic relation check is to test for clearance between figures and report those violating some

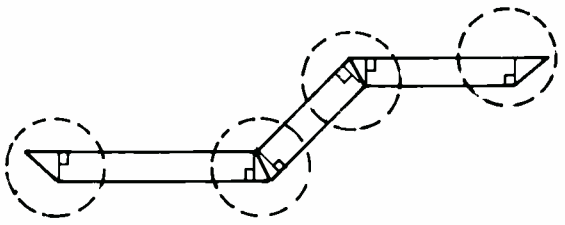

Fig. 2 — Minimum width check.

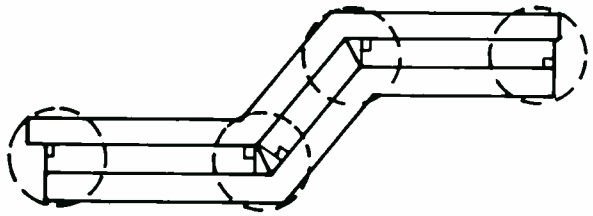

Fig. 3 — Calculation of the distance from each vertex of one figure to all the sides of the other.

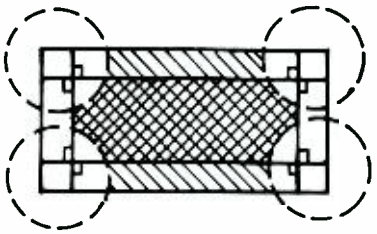

Fig. 4 — Clearance checks.

prescribed minimum. CRITIC calculates clearances using a technique similar to its width calculations. It calculates the distance from each vertex of one figure to all the sides of the other and then switches the role of the figures. (See Fig. 3 for some sample distances calculated.) This test can be performed between all figures on a single mask level or between figures on two different levels. This algorithm can rigorously find the minimum separation between all disjoint figures consisting of straight-line sides. It can also be useful for non-disjoint figures. Some examples appear later.

Another basic relation capability is to check that all figures on some level are contained inside of (or conversely, contain) some figure from another level (*e.g.*, all contacts must be inside oxide openings). It does this by checking if all the vertices of one figure are contained inside the other figure. This criterion is not strictly rigorous, but has been found to be adequate for all current needs. Exceptions will be discussed later.

A number of other checks consist of variations and/or combinations of the above checks. CRITIC can:

- Require that two "nearby" figures are exactly separated by some prescribed distance (*e.g.*, source and drain by the channel length).
- Report clearance violations less than the prescribed minimum but greater than zero (allowing the special case of zero separation).
- Check that every figure on a given level contain (or be contained in) some figure from another level.
- Test for one figure inside another and only then perform a "clearance" check. Note that it is essential to keep in mind how "clearance" is calculated (see Fig. 4) to understand this option. The result is essentially a minimum enclosure check.
- Perform a clearance check only if two figures don't touch (metal runs commonly consist of a number of touching figures which would generate many false error indications).

All of these features use the two basic geometrical functions described. There are more specialized capabilities and still others are being added.

Output: design rule violations

It is of course necessary that CRITIC communicate to the designer those "errors" that it has discovered. It is also desirable that these be in a form which allows the designer to quickly evaluate the nature and severity of the error. Therefore, CRITIC has two different forms of output.

The first form of output is a file consisting of the computer representation (DFL)[3] of all the figures involved in design rule violations. In addition, there are line segments added indicating the precise location of minimum width and clearance violations (similar to those drawn in Figs. 2 and 3). This can be used to generate a checkplot of these figures.

Visual inspection of this checkplot can often indicate the type, location, and significance of the reported errors. Using this checkplot alone, the designer can often evaluate most of CRITIC's findings — especially when some of the figures flagged are not true violations or are judged as acceptable by the designer.

The second and most complete form of output is a computer listing describing all the significant details of the design rule run. This includes:

- An "echo" of the command session, listing all questions, the user's responses, and the contents of the control-file selected, if any.
- A heading before each new design-rule check describing the test, any minimum distance criteria, and the mask level(s) involved.
- For each specific violation a statement indicating: the type of violation found; significant coordinates of the figure(s) involved; its (their) mask level(s); and the minimum distance found for a width or clearance test.
- Some statistical summaries and timing information are presented at the end of each check. These allow monitoring where the program is spending its time and is of great value in efforts to speed up the program.

False alarms and pathological situations

One of the basic problems involved in performing design rule checks using simple geometrical tests is that the design rules are not always exactly specifiable in these terms. Often, if the rule is specified conservatively enough to catch all possible design rule violations, it will also flag a number of acceptable situations. This can occur for a variety of reasons which will be discussed.

Experience has indicated that the number of spurious errors flagged by CRITIC can be kept to an acceptable level if the layout designer takes proper precautions in creating the IC artwork and in specifying the geometrical tests to be performed. Obviously, if the number of false alarms is very large, the time required to analyze CRITIC's results will increase and, more significantly, some true design-rule violations may be overlooked.

Spurious errors can occur for a number of reasons. Some common examples are:

- A test is improperly or unjudiciously specified or encoded. This is easy to rectify.
- There are special situations which are permissible exceptions to the design rule. If CRITIC can recognize these exceptions, they can be locked out. However if the

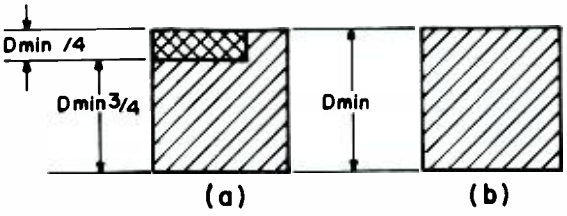

Fig. 5 — The polygons in (a) may cause an error indication in CRITIC, although their final form (b) is acceptable.

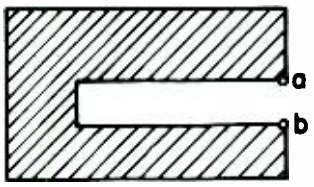

Fig. 6 — These types of potential "false alarms" are automatically eliminated.

Fig. 7 — Exception to criterion used to determine whether one figure is inside the other.

number of these is relatively small, they can be visually eliminated by the designer from the error checkplot. If they can not be locked out and are not few in number, judgment is required to decide if the particular test is still worthwhile.

- There are geometrically "pathological" situations. This type of problem is encountered often enough that it is worthwhile discussing it in detail.

These can be divided into a number of classes. One large class is related to the precise manner in which the figures were digitized. Consider the two metal runs (rectangles) shown in Fig. 5. Although they would result in identical shapes on the final mask, they are treated very differently by CRITIC.

CRITIC treats all polygons as distinct figures. The two polygons in Fig. 5a would be flagged as not only violating minimum width (one .75*Dmin, the other .25*Dmin) but could also lead to a zero clearance violation. Therefore it is important that each individual figure obey all the specified design-rule checks. Layout designers try to obey this rule as much as possible to minimize false alarms from CRITIC. This problem will be alleviated when a routine to calculate the geometrical union of figures is added to CRITIC.

There are a number of such situations that occur so often that special provisions have been included in CRITIC to handle them. For example, it is quite common for long metal runs to consist of a number of individual figures which could violate the minimum clearance test. Therefore, there is an option in CRITIC to ignore this particular situation; *i.e.*, when this option is selected, CRITIC will first check if two figures touch or overlap, and if they do, it will skip the clearance check. Note that selecting this option implies that the designer accepts, as a consequence, the assumption that if two figures touch, they were intended to. Although this could overlook an error involving a short circuit, it should be noted that an artwork short circuit falls into the realm of a connectivity error, not a geometrical one. CRITIC is designed to point out a potential short circuit arising from a minimum clearance violation, but not a true connectivity error. Another program is being developed to handle connectivity errors. The fact that a logical connectivity list is not included as part of CRITIC's input implies this limitation.

Another class of pathologies involves special cases for which the algorithms employed are not rigorously applicable. A post-process check by CRITIC is usually sufficient to eliminate these cases. As an example, consider applying the minimum-width algorithm to the polygon shown in Fig. 6. It would flag the "notch" separation, *a-b*, as a violation if it were less than the prescribed minimum width. This distance is clearly not a minimum width but rather what might be called a minimum "self-clearance". This situation is eliminated by a special post-process test which determines that the segment *a-b* lies outside the figure.

Another set of pathologies is due to the criterion used to determine whether one figure is inside another or whether two figures overlap. The algorithm simply tests whether all the vertices of one figure are inside the other (to determine whether the former is inside the latter) or whether any of the vertices of either are inside the other (to determine overlap). Fig. 7 shows one example of an exception for each of these cases. This particular type of pathology has not caused any problems in practice and could be eliminated completely by also looking for possible intersections between sides of the figures.

Experience has demonstrated that the pathologies that do arise can be handled with post-process tests, by the designers being more judicious in their layout techniques or by visual elimination from the error checkplot. Note that we can computationally afford a fairly complicated post-process test to a validate a flagged situation, as these occur much less frequently than the actual check.

Summary

We have discussed the CRITIC design rule checking program which has been in production usage at RCA's Solid State Division for over two years. It runs on DEC PDP-11 minicomputers, Univac Series 70, and IBM System/370 computers at the Solid State Division and at other RCA division locations.

CRITIC has the capability of performing a user-specified set of design rule checks involving such geometrical properties of artwork figures as minimum width, minimum clearance, minimum enclosure and one figure inside, covering, or touching another. It can perform special checks based on the outcome of a previous test.

It has a library of encoded design rule checks for various technologies such as COS/MOS, PMOS silicon gate, SOS, and high speed bipolar.

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PLOTS: a user-oriented language for CAD artwork

B.J. Korenjak

An easy-to-use data-capture language, called PLOTS, has been developed by the Design Automation activity of the Solid State Technology Center to allow effective man-machine communication in a computer-aided design system for integratred circuits.

A COMPUTER-AIDED DESIGN facility is vital to a high volume, quick-turnaround integrated-circuit operation. The precise and repetitive geometries representing integrated-circuit masks must be accurately maintained throughout photographic processes to insure success in delicate wafer-making processes — deposition of chemicals, diffusion, and etching. A single integrated circuit might require a separate mask for each diffusion or etching stage and some circuits require as many as fifteen separate masks.

Numerous machines have been developed for economically producing precision photo-plots of masks, and systems have been developed to capture and translate the basic integrated-circuit artwork description into computer data to ultimately be used to drive these precision photo-plotters. Such systems are available commercially and others have been developed within RCA.[1]

An essential element in any successful CAD artwork system is human engineering — particularly important in the data capture and data checking process. A CAD artwork system must be easy to learn and use and must be technology independent for the purposes of reducing cost, turnaround time, and design errors.

The computer-aided artwork system developed and implemented by the Design Automation activity of the Solid State Technology Center uses a well-defined, easy-to-learn and technology-independent set of rules for artwork description. Following these rules, the user can describe artwork to the system through a simple language, called PLOTS. Even if a digitizer is used for data capture, the user will see its output in the PLOTS language. The point is that the user always deals with artwork descriptions in a common language. This is illustrated in Fig. 1.

Barbara J. Korenjak, Design Automation, Solid State Technology Center, Somerville, N.J., after attending college and serving in the U.S.A.F., was employed at Applied Logic Corporation in Princeton, N.J. as Technical Services Coordinator and diagnostic programmer. In 1970 she was named Administrator to Vice President of Budgets and held that position until joining RCA in 1971. She is currently responsible for the design and implementation of a user-oriented documentation program for Design Automation systems. She is also providing the supportive services of user instruction and customer relations for Design Automation.

Since this paper was written, Ms Korenjak has left RCA.

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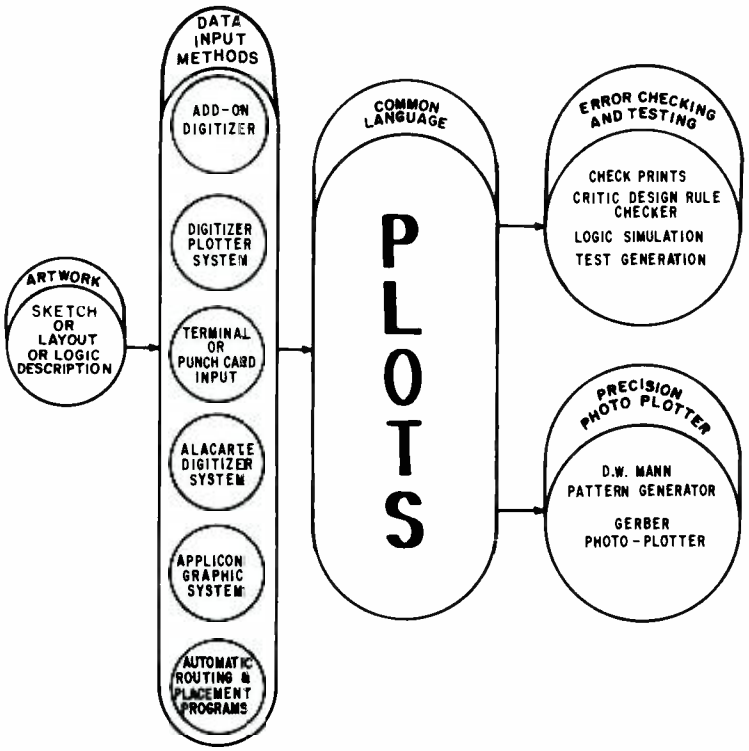


Fig. 1 — PLOTS language is central to the artwork system.

PLOTS language

The PLOTS language is simple enough to accommodate the casual user, yet sophisticated enough that inter-related cell libraries can be handled easily. The descriptions are brief, yet meaningful enough that the same circuit description can be passed from one user to another. The important user features of the PLOTS language are summarized below:

Easy to use

- Simple readable syntax
- Flexible coordinate description
- Convenient shorthand notation

Easily modified

- Can be edited with any text-editor

Technology-independent

- Purely geometric
- No characteristics of particular mask-making machines are assumed
- Knowledge of the mask-making process is not required

An artwork description can be taken from a scaled hand-drawn sketch if the coordinate locations of the geometric figures are specified.

Polygons

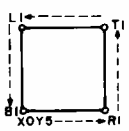
The geometric shapes are all closed plane figures with straight sides. These polygons are usually described as opaque figures on a clear field, although this can be easily reversed during the processing of the design file.

A rectilinear coordinate system is used to describe the polygons, either in terms of an absolute vertex location or as relative vertex coordinates in the directions left, right, top and bottom from the previous vertex.

The basic PLOTS language statement for a polygon includes the name of the polygon type and a specification of its vertices. For example, the PLOTS language statement

0 X0Y5 R1 T1 L1 B1

represents the orthogonal polygon shown below.

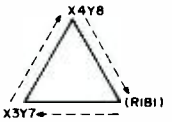


The figure is an orthogonal polygon with a starting vertex at x-axis location 0 and y-axis location 5; the next vertex is found by moving Right a distance of 1; then Top 1 from the previous vertex; then Left 1 from the previous vertex; and finally, to close the figure and return to the starting location, Bottom 1.

The "O" or Orthogonal polygon is one of seven fundamental PLOTS language statements. It identifies a figure having all sides parallel to either the x- or y-axis; it may contain up to 127 sides.

To describe a figure, some of whose sides are not parallel to either the x- or y-axis, a "P" or general Polygon statement is used. The triangle below can be described as follows:

P X3Y7 TO X4Y8 (R1 B1) TO X3Y7



This P statement describes a general polygon with the starting coordinate of X3Y7; the next vertex is found by moving TO X4Y8; the next vertex is located relative to the previous one and is described as being Right 1 and Bottom 1 from it; the figure is closed by returning to X3Y7.

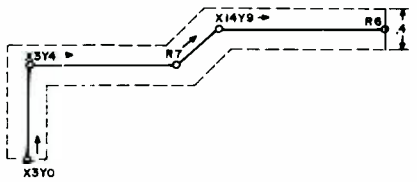
Notice that the user has the option of using either the relative or absolute coordinate notation, or both. The use of spaces within a PLOTS statement is also optional. These features provide maximum flexibility for user convenience and readibility.

Certain types of polygons may be described in a manner other than the O or P statements. These polygons may be thought of as lines with a constant width. These types of polygon are common on metal masks where they are used as wires to connect components. The following statements describe such a polygon:

W .4
L X3Y0 TO X3Y4 R7 TO X14Y9 R6

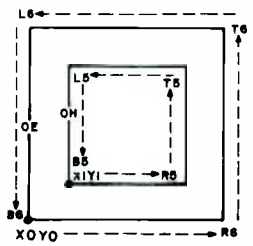
Two PLOTS language statements have

been written; the first is a Width statement that assigns a width of .4 to *all* following L-type polygons. The centerline of the polygon is then described in the L statement. The beginning of the centerline is at X3Y0; then the turning points are successively described by either absolute or relative notation — X3Y4, Right 7, X14Y9; finally the end of the center line is defined by a relative move of Right 6 from the previous turning point. When processed after the Width statement, an L statement is expanded into a closed polygon as follows: two lines are drawn parallel to each portion of the centerline, half the width distant from it; the ends are squared off; other vertices are determined by the intersections of the parallel lines just drawn, except that the outside of an acute angle is rounded off.



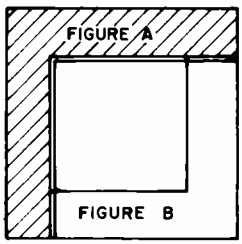
In addition to the basic orthogonal polygon form described above, a special orthogonal polygon form is available to define a clear area inside an opaque polygon. This situation is handled by the Orthogonal Exterior and Orthogonal Hole statements.

```
OE X0Y0 R6 T6 L6 B6
OH X1Y1 R5 T5 L5 B5
```



The outside boundary of the opaque area is described as an orthogonal exterior polygon beginning at vertex X0Y0 and forming a 6×6 square. The outside boundary of the clear area is similarly described in the orthogonal hole statement.

Note that this particular figure could also be described using basic PLOTS statements, such as two O polygons or as an L statement with a Width of 1.



Definitions

An important feature of PLOTS is the standard cell or definition concept. The D (Definition) statement and the E (End-of-definition) statement are used to establish a boundary around other PLOTS statements for the purpose of later placing the artwork described by this group of statements in more than one place without repeating the PLOTS statements. A definition may contain any number of PLOTS statements, perhaps representing a complete multi-layer device. A definition may contain any other PLOTS fundamental statement — O, P, L, Q, OE, or OH — and the control statements M and W. Definitions are self-contained; therefore control statements (M or W) that are issued inside a definition apply only to that definition. The format for a D statement is:

D*n* X*x*Y*y*

The *n* is an integer (name) which is chosen to uniquely identify the group of PLOTS statements. Two definitions with the same number may not be used in the same artwork description. The definition number is followed by an absolute coordinate that serves as a reference point for the coordinates that appear within the definition.

To describe a definition named 55, with reference point at X0Y0, the following D statement is written:

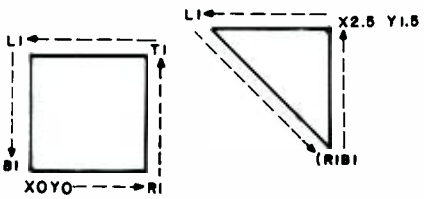
D55 X0Y0

A definition does not actually cause artwork to appear on the mask. It must be placed by a Q statement. The coordinates of the Q statement specify where the reference point of the definition is to be placed on the mask. All other points in the definition are then placed in their proper relative position.

The E (End-of-definition) statement marks the end of the PLOTS statements included in a definition.

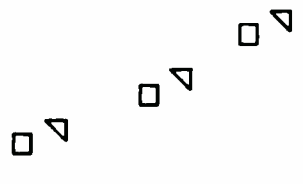
The following illustrates the use of the definition statement for two figures to be placed on mask level 1:

```
D55 X0Y0
M1
O X0Y0 R1 T1 L1 B1
P X1.5Y1.5 L1 (R1 B1) T1
E
```



To place these figures repetitively on the mask, the user simply writes a Q statement. Thus, the three Q statements would place definition 55 on mask level 1 as:

```
Q55 X0Y0
Q55 X7Y15
Q55 X3Y9
```



The Q statement indicates the location where the reference point of the definiton is to be placed. If desired, one of eight possible rotations or mirrorings can be applied to the definition as it is placed. In addition, the definition may also be scaled as it is placed. This provides flexibility, minimizing artwork description and encouraging the use of predefined cell libraries.

Notation for ease of use

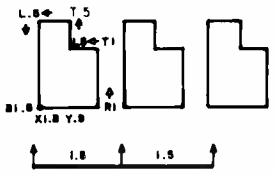
If a single geometric pattern or row of devices appears frequently on the mask, such as a memory array, the user may employ the AND feature to reduce the amount of data entry required. An option

of the O,P,L,Q, OE, and OH PLOTS language statements, the AND statement is used to repeat a pattern by simply indicating its placement rather than repeating all the coordinates. The format of the option is

AND *n* <coordinate string>

The integer *n* indicates the number of times the pattern is to be repeated. This is followed by a coordinate string to place the figure. Any number of AND options are permitted in one PLOTS statement:

The following three figures are the same pattern that have reference points spaced 1.5 units apart along the X-axis:



A single O statement with the AND option that represents all three figures is:

O X1.8Y.9 R1 T1 L.5 T.5 L.5 B1.5 AND 2R1.5

An important convenience of PLOTS is the ability to describe a figure in any continuous description moving either clockwise or counterclockwise from any known corner. All PLOTS language statements are free format and may use a continuation character if more than one line in length. Comments are also permitted.

Summary

A sample PLOTS language file and corresponding artwork are shown in Fig. 2. The PLOTS language statements use either absolute notation, relative notation or both. Definitions, the AND statement, and Q-calls are all tools available to the user for minimizing the number of PLOTS statements necessary to describe the artwork. The figures can be described in more than one way. For example, polygons 13 and 14 can be written as two Orthogonal polygons, or as Orthogonal Exterior and Orthogonal Hole polygons, or as a line statement with a .4 width. All examples in the sample PLOTS language statement file have been described in their most common representation; however, the versatility of PLOTS allows the user to select a valid alternate approach.

```
10 M1
20 O X2.8Y12 R1.6 T.5 L.6 T.5 L1 B1 ;FIGURE 1
30 O X6.2Y5 T.6 L.4 T.4 R1 T1 R1 B2 L.5 T.6 L.5 B.6 L.6 ;FIGURE2
40 P X8.8Y14.8 R1.6 B1.6 L1 TO X8.8Y13.6 T1.2 ;FIGURE 3
50 P X2.8Y5 TO X3.3 TO X3.8Y5.5 TO X4.3 TO X4.8Y5S
60 TO X5.3 TO Y6.6 TO X3.7 TO X2.8Y5.6 TO Y5 ;FIGURE 3A
70 W .4
80 L X7.8 Y4.4 TO X8.2 TO X8.6Y4.8 TO Y7 ;FIGURE 4
90 D1 X0Y0 ;DEFINITION 1
100 M1
110 P X1.2Y0 R.5 T1.6 L1.5 B.6 TO X1.2Y0 ;FIGURE 6
120 W .4
130 L X2.6 Y0 T1.6 TO X2.2Y2 TO X0 ;FIGURE 7
140 E ;END OF DEFINITION
150 Q 1 X2.8Y7.5 ;PLACES FIGURE 5 AT FIGURE 8
160 Q 1 X8.8Y10 ROTATE 2 ;PLACES FIGURE 5 AS FIGURE 9
170 Q 10095 X6.8Y13.1 ;PLACES FIGURE 16 AS FIGURE 10
180 OE X1.4Y3 TO X10.4 TO Y12.4 L4.4 T2 L4.6 TO Y3 ;FIGURE 11
190 OH X2.4Y4 TO X9.4 T7.4 L2 B1 L2.5 T3 L2.5 TO Y4 ;FIGURE 12
200 OE X6.8Y.8 TO X9.8 T1.6 L3 B1.6 ;FIGURE 14
210 OH X7.2 Y1.2 T.8 R2.2 B.8 L2.2 ;FIGURE 13
220 O X1.8Y.9 R1 T1 L.5 T.5 L.5 B1.5 AND 2R1.5 ;FIGURES 15,15A,15B
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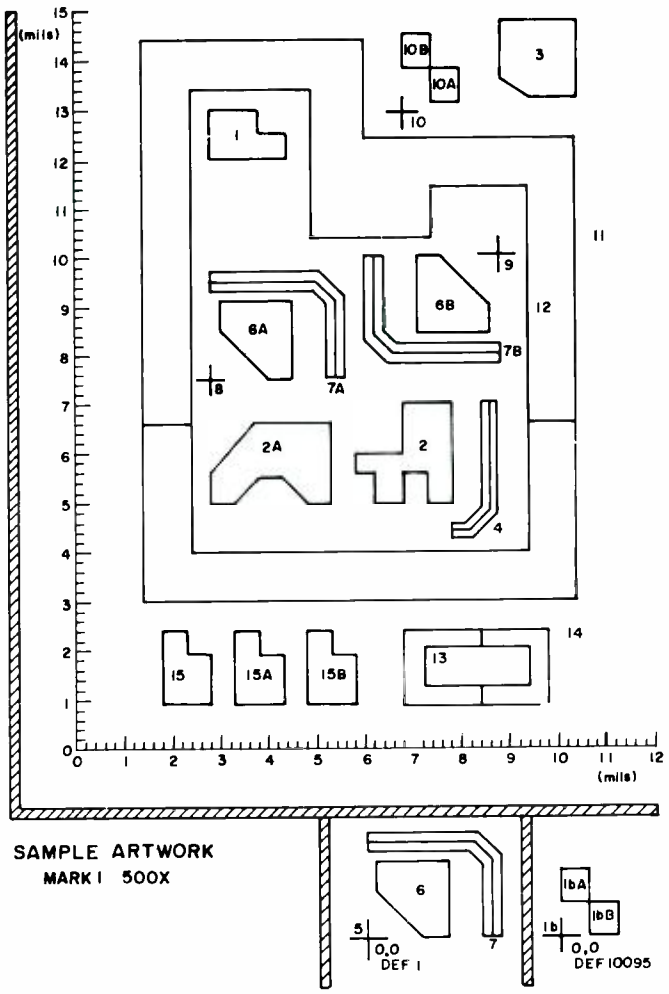

Fig. 2 — Sample PLOTS language statement and artwork. The "FIGURE" numbers that follow the PLOTS statements (separated by semicolons) correspond to numbered shapes on the artwork.

Presently, PLOTS language statement files may be created and processed on UNIVAC Series 70, IBM/370, and PDP-11 systems, as well as the stand-alone systems shown in Fig. 1.

The PLOTS language has received wide acceptance within RCA since it was introduced in the late 1960's. Because of its flexible technology-independent approach, many RCA product lines are using this design automation tool to produce their circuit artwork at a considerable savings in time and cost.

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ALARCARTE: a computer-artwork entry system

C.A. Benbassat

The major task involved in producing integrated-circuit masks automatically is to obtain the geometrical description (artwork) of a circuit in a computer. One system for easily entering the artwork into the computer is ALACARTE (A Low-cost Augmentable Computer ARTwork Entry). The artwork can then, under computer control, be checkplotted, be edited, be checked for design rule errors, and be used to generate the necessary integrated-circuit masks.

MAJOR FEATURES of the ALACARTE system are:

- *Low cost* — the entire digitizing system (including a graf/pen and two Sykes cassette recorders, not including a terminal) costs $15K.
- *Easy to learn* — a person can be taught to use the system in 3 days.
- *Expandable by user to optimize digitizing* — this involves the use of a personalized menu facility which is discussed later.
- *Compatible with all other artwork systems* — any of the Solid State Technology Center Design Automation systems can be used at any point in the design loop.

Carole A. Benbassat, Design Automation, Solid State Technology Center, Somerville, New Jersey, attended Goucher College in Baltimore, Md. from 1964 to 1966. She received the BS from Tufts University in 1968 with a major in Mathematics. In 1971 to 1972 she attended graduate school at Washington University in Experimental Psychology. In the fall she will commence taking graduate courses at Rutgers University in Computer Science. From 1968 to 1970 she worked as a computer programmer at Lincoln Laboratory. In 1970 to 1971 she was on the staff of Barnes Hospital in St. Louis. Ms. Benbassat joined RCA in 1972, working in the Design Automation Group of SSTC at Somerville, N.J., where she has worked on ALACARTE and CRITIC.

- *A remote system* — the digitizing system can be used anywhere there is access to NTSS.

The users enter their artwork into the computer using PLOTS, which is a text-oriented language useful for describing geometrical shapes.[1] PLOTS is common to all systems designed by SSTC Design Automation.

Starting with a drafting layout of the circuit, the task is to capture information on the drawing and to express the information as digits in the computer — *i.e.* to digitize the data. The drawing is mounted on the graf/pen™ [Science Accessories Corp.; Southport, Conn] which is the digitizer presently being used. A pen (or cursor) is used to identify the points to be digitized. The digitized points then are stored either on tape cassette, in computer file, on cards, or on some other medium for later processing. Presently, data points are stored on a Sykes cassette tape and interfaced with ALACARTE as shown in Fig. 1. In this configuration, circuits can be digitized at any hour, whether or not NTSS is running — and at the digitizer's speed (since the hardware records at 1200 baud). Then when the user is ready, the data are sent into a file on NTSS from the cassette via a Hazeltine terminal at 1200 baud. ALACARTE is executed with this file as the input: it interprets the coordinates and converts them into PLOTS statements, and it generates a file consisting of these resulting PLOTS statements. From this step, any of the Design Automation artwork programs can be used on the file. A usual first step is to have the file checkplotted, either on the Calcomp plotter interfaced to the Hazeltine, or to use a cassette tape to directly run the plotter, or to use a large flatbed plotter.

Digitizing errors can be corrected by using the NTSS text editor via a time-sharing terminal (part of ALACARTE) or by using any of the other SSTC design-automation editing systems such as the Digitizer Plotter System or the Applicon[2] Interactive Graphical System. The next step is to run the CRITIC computer program which checks for geometrical design rule violations.[3] Errors uncovered by this program can be corrected by any of the editing systems. After the data has been corrected, it is submitted to another program named MAP which produces pattern generator commands on magnetic tape. The magnetic tape drives the precision plotter to produce the masks. Any of the Design Automation tools can be used at any point in the design of a circuit. ALACARTE is one means of interfacing the design to the tools of Design Automation.

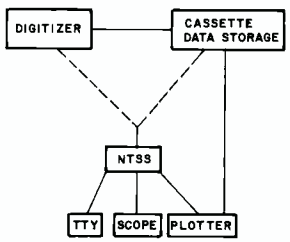

Fig. 1 — ALACARTE system.

ALACARTE operation

All of the Design Automation systems, including ALACARTE, require that the user know the PLOTS artwork language, since all digitizing is done by creating PLOTS statements. Artwork can be entered in any number of ways. It can, for instance, be entered via a remote computer terminal. However, unless the artwork is quite small, this method quickly becomes tiresome and error prone. The ALACARTE system may, in its simplest use, function exactly like a terminal used in creating PLOTS files.

The ALACARTE system, though, also offers aids to the user that make it easier and quicker than a terminal. The first aid which the ALACARTE system provides is that of entering coordinate information. When using a remote computer terminal, the user must read the coordinates off of the drawing and enter them into the PLOTS line by typing the keys that represent that number. With the ALACARTE system, the user may simply point to the coordinate on the drawing and it will automatically be converted to the proper characters and entered into the PLOTS line. So, for the PLOTS statement

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P X127.5Y49.6 TO X143.2Y52.8 TO X115.7Y50.6 TO X127.5Y49.6

the user would use the appropriate square from the set of squares located along the right edge of the table (Fig. 2). This set of labeled squares is called the "menu". The user would need only touch the "P" square in the top half of the menu. Then, instead of reading off all of the points and then entering all of the characters into the PLOTS statements, the user would touch the coordinates on the drawing in the order they are to be entered.

A second aid to the user is the set of PLOTS keys and keywords located in the lower right portion of the menu. Touching one of the keys (D, M, P, O, OE, OH, W, L, E, Q) will end the previous statement and start a new line beginning with the key touched. Here the equivalence of a "return" is generated when touching one of the appropriate PLOTS keys of the menu. Thus, PLOTS statements are created by touching squares in the menu intermixed with coordinates. For example, the user would touch the "O" on the menu and then touch the corners of the figure on the drawing.

Line Editing capability similar to that available on a terminal is provided by the "back arrow", DEL (Delete), and RET (Return) squares. Touching the "back arrow" square will cancel everything created by the last pen or cursor movement. Successive "back arrows" will cancel previous pen movements. Touching the DEL square will delete the entire current PLOTS statement which is being created. Touching the RET square indicates the end of the current PLOTS statement. As on a terminal, these capabilities apply only to the current line. This means that while digitizing, one could not delete more than the current line without some extra effort.

A major aid to the user is the TXT facility. This facility aids the user in putting text on the drawing. "Text on the drawing" refers to lettering which is to appear on the drawing, as opposed to characters in the PLOTS file. The user merely enters the text mode, indicates the location on the drawing of the lettering, and then indicates the letter in the text or string of text.

Finally, the ALACARTE system provides a personalized menu ("pers menu" key) facility which allows the user to add menu items which will speed the digitizing. The personalized menu squares may be defined by the user to contain any desired string of characters. It is usually a string that recurs often in the file, so that having it as a personalized menu box provides a shorthand function. When that square is touched, those characters will be entered into the PLOTS line. For instance, a user who is digitizing Q-calls to a set of standard cell definitions spends much time pointing to to the "Q" square and the characters which make up the definition number. For example, the statement, Q1904 X5Y97, requires six pen movements. With the Personalized Menu facility, the user may define an additional portion of the menu which contains squares for each Q-call he has in the standard cell library. The squares might be labelled Q 1904, Q 1905, Q 1906, *etc.* Now to call out a cell, the user need only touch the Q 1904 square and the coordinate at which it is to be positioned (2 pen movements). In this way, the personalized menu allows the user to greatly reduce the amount of digitizing by making common functions only one movement of the pen or cursor.

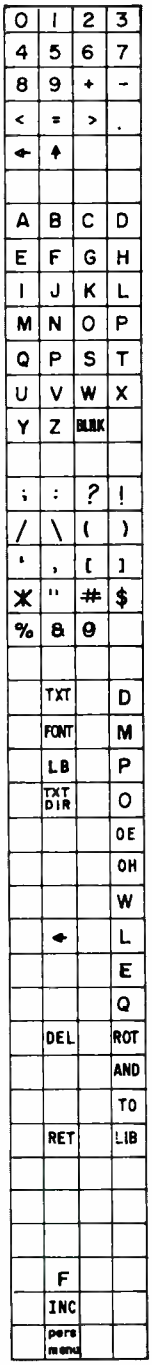

Fig. 2 — ALACARTE "menu".

ALACARTE has been used by the SSTC Custom Monolithics Group in Somerville, the Photomechanical Group in Princeton, the Computer Aided Design and Test Group in Hightstown and the West Palm Beach Group. The reliability of the hardware has been a problem, particularly that of the graf/pen. The system has been used quite successfully by groups requiring an accuracy of 0.1 inch on the 40 × 40 inch digitizing table. Standard dimensions in COS/MOS require a 0.1 mil grid at 500 magnification, which means 0.05 inch accuracy is needed by a digitizer. The graf/pen cannot meet that requirement. As hardware improvements for digitizers are reported and at the same time costs are held down, then the new equipment will be incorporated into ALACARTE. In the meantime, RCA groups not requiring more accuracy than 0.1 inch will continue to enjoy ALACARTE's benefits of low cost, ease of learning, expandability by the user, compatibility with other SSTC Design Automation artwork systems, and remote digitizing.

For more detailed directions for using the system, see the "ALACARTE User's Manual".[4] For a demonstration see members of SSTC Design Automation.

Acknowledgment

I wish to thank G.D. Held for his important contributions to the project.

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Reliability and computer aided design

J.G. Smith

Reliability of an electronic product starts with design assurance and process assurance. Subsequent history and analysis serve the purpose of either validating the reliability expectations or identifying additional design or process constraints that must be observed, but these tactics do not establish reliability directly. This paper discusses the role that computer aided design can play in increasing design assurance.

AN ELECTRONIC EQUIPMENT can be reliable only if the design processes and fabrication processes have been carried out correctly. Screening, testing, and failure analysis, while essential to a reliability program, do not add reliability to the product. Rather, they increase the confidence that design and fabrication have been executed properly. To say that a design has been carried out properly is to say that all of the requirements placed on the design by the intended application and all of the constraints imposed on the design by the fabrication processes have been met. If the fabrication process is carried out correctly, then equipment will meet the performance parameters specified by the designer.

Reliability at the expense of design complexity

Over the last twenty years there has been a dramatic reduction in the number of individual pieces making up electronic assemblies. Equipments of the early 1950's which required thousands of vacuum tubes, crystal diodes, and passive components, have been replaced today by equipments which typically use several hundred integrated circuits. Mean time between failure (MTBF) calculations for those earlier machines predicted failure-free intervals of several hours, as contrasted with current estimates of thousands of hours for the newer equipment.

Table I illustrates the contrast between a digital equipment as implemented with the discrete transistor technology typical of the years 1955-60 and the same equipment as implemented with four LSI chips. Reliability calculations show an improvement of two to three orders of magnitude. The improvement is due to the reduced parts count and the accompanying reduction in connections.

An examination of the design methodologies being applied to current products which use LSI parts reveals that the disciplines of semiconductor physics, precision mask making, systems and logic design, and packaging have all become inextricably woven together. Consider the problem of designing an equipment which uses several PMOS LSI chips. The selection of buffer circuits to drive from one chip to another is primarily affected by the capacitive loading represented by the length of the wiring path between the chips. Since buffers use considerable chip area, it is desirable to select them to be near the required values. Therefore, the proximity of the chips ideally should be established before committing to a final chip design. As technology progresses the trend will be toward greater design complexity. Computer aided design is a

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James G. Smith, Staff Technical Advisor, Government Engineering, Moorestown, N.J., received the BS from Randolph-Macon, Ashland, Va., in 1950. From 1951-1952, he took advanced courses at Tulane University, New Orleans, La. Mr. Smith joined RCA in 1953 to work on logic design of the Bizmac Computer. From 1955 to 1958, he directed the design of RCA's first transistorized computer, the RCA 501. In 1960, Mr. Smith was named Manager of Product Planning - Small Scale Systems. From 1962-1963 he held the Technical Liaison post for International Computer Operations. He became Manager, Computer Research in 1964, a position he held until 1970 when he assumed his present position.

Table I — The effect of LSI on equipment reliability (1000-gate complexity).

	Discrete transistor technology	*LSI technology*
Resistors	5,600	—
Capacitors	2,400	—
Transistors	1,200	—
Diodes	1,200	—
Solder connections	37,064	160
P.C. boards	143	1
Submodule boards	1,200	—
Sockets	143	1
Separable connections	2,288	100
Cables	7	1
Bonds	9,600	320
LSI arrays	—	4

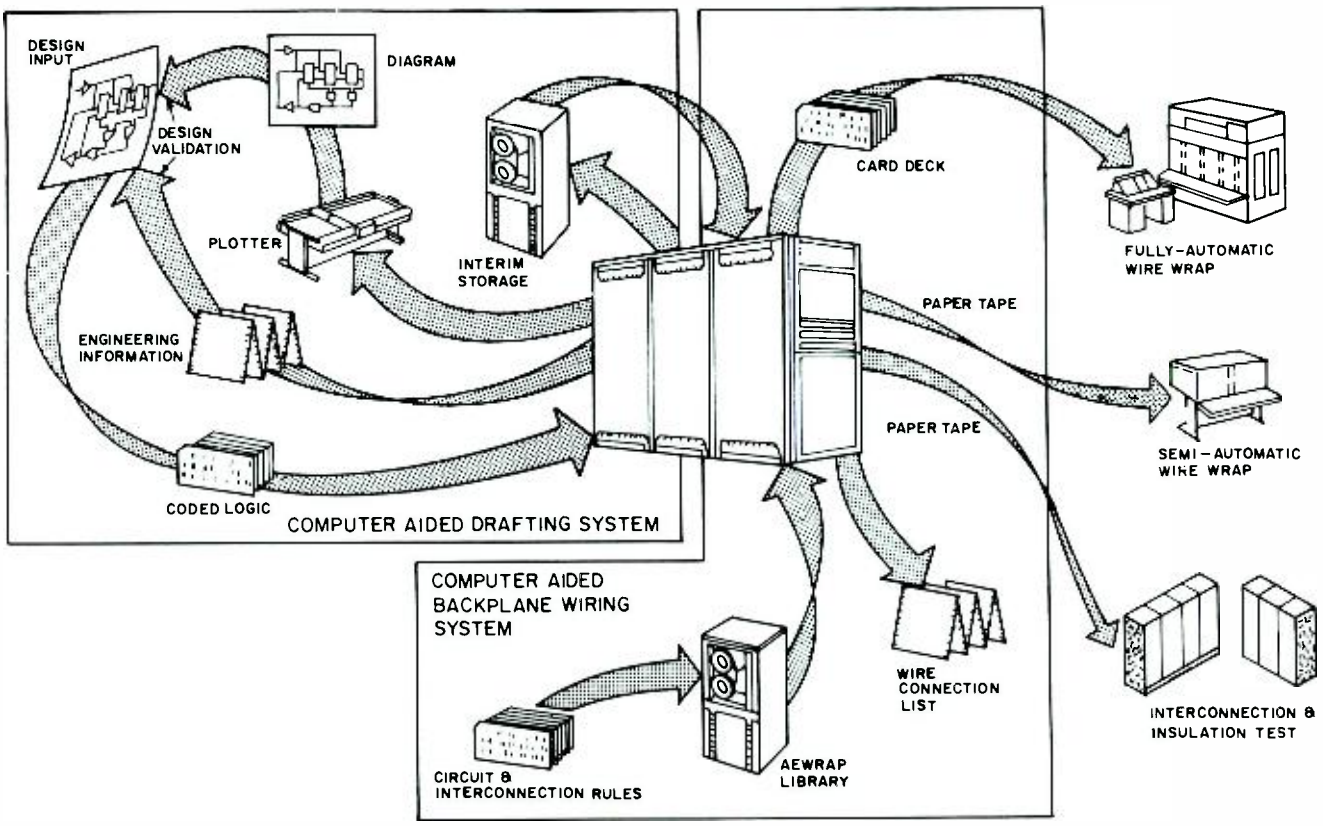

Fig. 1 — Work flow through a CAD system for designing backplanes.

means of coping with this growing complexity (see Fig. 1).

Standard cell automation

For many years designers of digital equipment have made use of circuit libraries. These libraries generally contain gate circuits, inverter circuits, flip-flops, counters, shift registers, etc. Each circuit is carefully designed, characterized, and documented to specify its application parameters. Usually a circuit standards activity controls the drawings of the circuit to curb unauthorized changes. The creation of the circuit library achieves many things: only skilled circuit designers who know the technique of worst-case design participate in the circuit design process; each circuit is analyzed by a review committee to ensure that no detail has been overlooked; there is an economy of design; there is design protection; and there is frequent usage so a history of performance can be quickly accumulated. This concept of the circuit library has carried over to LSI circuit technology. The standard circuit has now become the *standard cell*. The way in which standard cells are accessed and used by design engineers is discussed in the article in this issue titled, "The APAR Design Automation System — an Overview," by A. DeMeo and H. Zieper.

Several comments can be made about the standard cell technique for generating LSI arrays as it relates to design assurance and ultimately to product reliability. The integrated circuit layout rules for the cells and the accompanying process parameters are chosen to be identical with those being used to produce standard products. This permits the user of the custom LSI array to tie in to the reliability base which has been established for standard products. As a cell is successfully used in an increasing number of designs, confidence grows that the cell has been properly designed. Another benefit is derived in the artwork generation phase. A typical COS/MOS circuit array containing 250 gates of logic requires a mask set with the equivalent of 40,000 scribed lines. Because of size restrictions of manual scribing equipment, an array of this complexity would have to be divided into several sections and recomposed photographically. The time and cost because of errors and also the final mask quality would be unacceptable by current standards. The computer aided design approach eliminates this error-prone manual procedure by storing cell geometries on magnetic tape. These parameters are then assembled by the computer and used to generate an artwork tape containing commands that control an artwork generator in the creation of mask artwork.

Computer aided circuit design and simulation

Since LSI circuit design has become intimately involved with semiconductor processing and layout, these parameters are important in circuit simulation. In the design of a standard cell implemented in MOS technology, transistors can differ in their dimensions. Therefore, the simulator is designed to accept transistors which are defined in terms of geometry. A digitized layout of the standard cell provides the data needed to compute actual metal and tunnel areas so that accurate values for capacitive effects can be included in the simulation. Moreover, process parameters such as gate oxide thickness, mobility, lateral diffusion, and estimates of the variation in these parameters which are due to process variations, are incorporated in the simulation. Mask alignment tolerance is also a factor in determining the worst case for the circuit design and is included in the analysis.

A circuit analysis program that has been enhanced by incorporating features similar to those just described becomes a valuable design tool that permits computer breadboarding of standard cells. The accuracy of such simulation comes within 20% of observed results. One reason for such good agreement is that experiments using test chips are performed, and the results are fed back into the circuit models. These test chips are readily generated by the same layout programs used to make custom arrays.

A logic simulation program provides a design engineer with a capability to analyze a complex logic network. In such a simulator, the inputs and outputs of all elements are represented by ones or zeroes, and the state of any element is determined by its inputs and its delay response.

Underlying the structure of the simulation program is the method of representing gate delay times. In a physical logic gate, the output response to an input change is displaced in time and degraded in shape. These changes are shown in Fig. 2, where the total response time consists of a delay, t_d, before any change is noted in the output waveform and a fall or rise transition time, t_f or t_r. Logically, the gate is considered switched when its output waveform reaches some critical threshold. In Fig. 2 this critical level is α for a fall delay and β for a rise delay.

In the computer representation, any gate being simulated will normally have either a HIGH or a LOW logic level (an indeterminate level is present when neither a HIGH nor a LOW level can be found). When the output level is to change in response to an input change, the gate enters a transistion region represented in the program by a delay time and an instantaneous change of state. The delay times T_f and T_r in Fig. 2 are interpreted as the total response times for this particular gate, that is, the amount of time that elapses before an input change is reflected in the output state of the gate. These two delays represent the timing data supplied by the user for any given gate in the simulation. The user may elect to operate every gate in his logic net from the same rise and fall delay times, or he may assign different delay times to each gate. The user may also elect to specify delay limits and have the computer assign delays between these limits according to a probability distribution function typical of the range of values that result from process variations.

The delays assigned to any given gate can be made to account for the variations in fabrication, for wiring delays encountered in the partitioning and packaging of the logic, and even for the variation in response time of the gates. By increasing the delays, the user can account for both the gate response to a slow input risetime and wire length propagation time. By decreasing the delays, he can account for both faster input risetimes and asymmetrical switching thresholds of the gates. Thus, by assigning appropriate delays, the user can receive a trial simulation or a detailed analysis of the timing on the same logic.

After delay times have been assigned to all the gates, the logic network is exercised by generators which represent square wave sequences defined by the user. The results of the simulation can be observed by recording any or all gate output changes as functions of time as the simulation proceeds. Fig. 3 illustrates the concept of simulation with generator inputs, the user's logic, and an n-channel recording oscilloscope.

Timing is superimposed on the simulation by an internal clock. The clock starts at zero and is incremented appropriately as the simulation progresses until the value of the internal clock matches that of the user specified stop-time. The relationship of the internal clock to real time is determined by scaling the delay times assigned to each gate in the logic network. After an input change occurs which changes the output value of a given gate, the change of the gate output is delayed in the simulator until the appropriate transition delay has elapsed. At that time, the output value instantaneously changes state. Thus, by assigning a gate delay of 10 units of time to a gate which has a real delay of 10 ns, the user has scaled the internal clock of the simulator so that one unit of simulator time represents 1 ns.

There is an obvious tie between logic

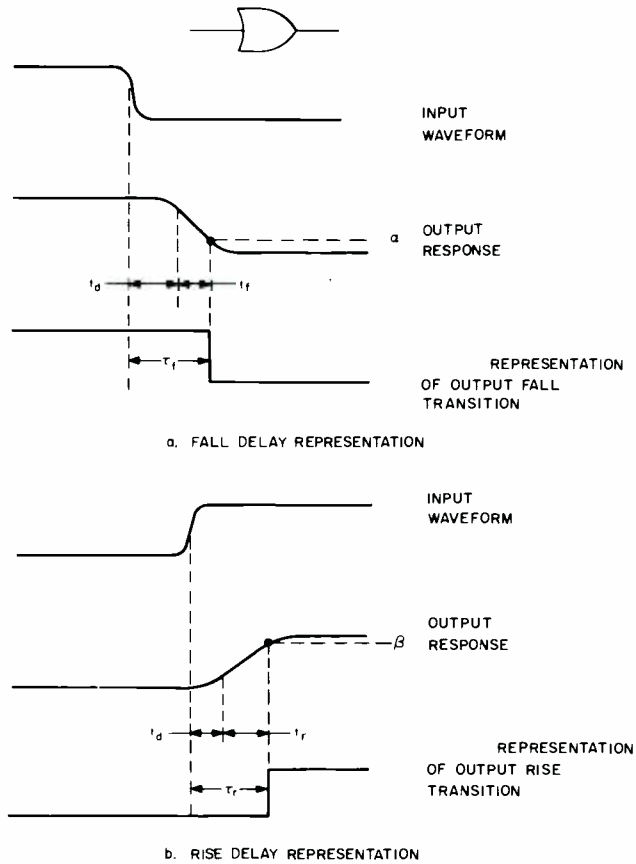

Fig. 2 — Representation of gate delays.

simulation and circuit analysis. The delay characteristics used in logic simulation are direct inputs from the circuit analysis program. Additional loading on the circuit board can be derived directly from statistics developed by the LSI array layout programs or the printed circuit layout programs. The progressive buildup of design assurance which enhances the reliability of the final product is a central theme of a well thought-out computer aided design system. Design verification, using computer aids, is a more realistic approach than trying to breadboard a design. In the LSI chip environment the very small capacitance values and the variations in process are virtually impossible to model in discrete circuit form. This is especially true of internal logic elements whose inputs and outputs are not brought out to bonding pads.

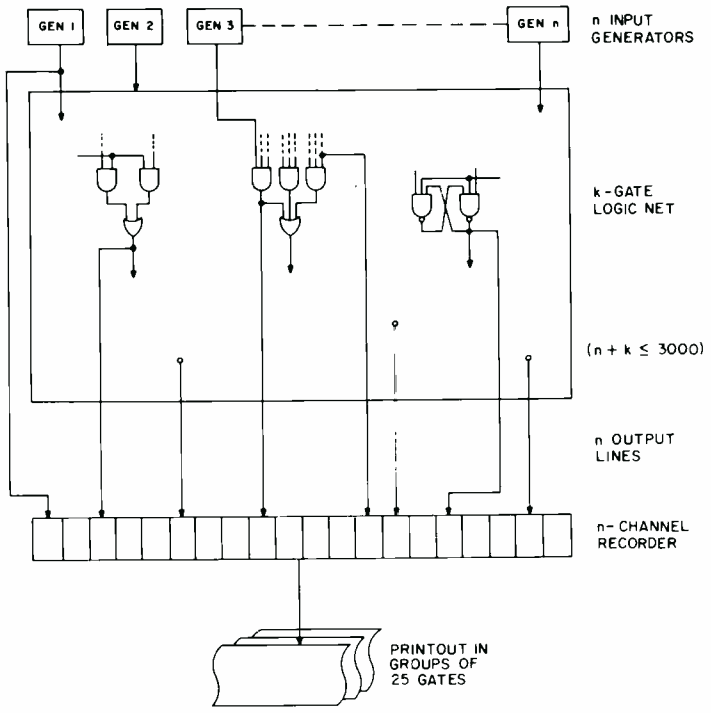

Fig. 3 — Concept of logic simulation.

Backplane wiring design automation

In any large-scale wiring system, interconnection of high-speed digital logic circuits is complex. The calculation of permissible circuit loading and the design of wiring to minimize reflections and cross talk and to provide for reproducible manufacture and test require many thousands of decisions that demand costly engineering effort. The density, circuit speed, and large dimension of backplanes carries this problem to such a level of complexity that computerized design, manufacture, and test are essential to a practical solution. Programs have been developed that achieve automated interconnection of backplanes with the same high degree of reliability that is designed into the basic circuitry.

Circuits are categorized into many wire routing classes according to interconnection limit factors such as wiring delays, capacitance, and circuit loading. Parallelism limits, specifying maximum wire lengths between adjacent nets of both single wires and twisted pairs, are established for each circuit class to control cross talk between nets. All of these conditions are then entered into tables which may be stored in the memory of the computer.

The first computer operation validates incoming data against circuit rules set into this library. The computer then maps connections for as many as 12,000 wires into groups of signal trees, which are calculated to reduce wire length, and selects a wiring path to reduce noise to a minimum, in accordance with circuit rules. If allowable noise is exceeded by the best available path, the wire type to be used is automatically changed from a single wire to a twisted pair. The last section of the program assigns wiring to either the fully automatic (single-wire) or semiautomatic (twisted-pair) wiring machines, produces direction tapes and cards for their control, and generates a complete numerically controlled program for connection and insulation tests of the wired backplane. Fig. 1 shows the work flow through the Backplane Design System. (See "Automated Design for Backplanes and Modules," by DeVecchis and Smiley, in this issue.)

Computer aided design of backplane wiring has a major impact on product reliability. One way to illustrate this point is to first consider a backplane where the wiring paths have been chosen at random. Noise problems resulting from this procedure will be handled during testing by rerouting wires. We then ask—how much noise margin have we provided in the design of the backplane wiring? The answer is that we do not know. If two printed circuit cards are exchanged, or if a circuit ages slightly, the noise threshold will be exceeded and result in a failure. The direct attack on this problem is to adopt a design procedure which establishes a total noise budget, a portion of which is assigned to the backplane wiring. Wiring rules are then established which assure that the budget will not be exceeded. For backplanes with many thousands of wires, computer aided design is an essential design tool.

A look to the future

The main thrust of this paper has been to show that an integrated system of design aids raises the level of design assurance and its corollary, reliability. A fruitful area for endeavor, in the writer's opinion, would be an increase in the level of automation in the area of fabrication processes. Controls are required to establish precise and reproducible processing. Monitoring of the processes is required for analytical studies to determine reasonable limits of control. There also must be a continued search for fabrication processes which meet the requirement of being free from inherent failure mechanisms.

Electronic products with near infinite lifetimes are on the horizon. Computer aided design has and will continue to contribute to that goal.

APAR design automation system —an overview

H.S. Zieper| A.R. DeMeo

The Automatic Placement and Routing (APAR) system was created originally to use metal-gate CMOS technology in LSI form, but it now has been extended to SOS, and will continue to evolve with the growth of this extraordinarily flexible technology. The key purpose of this article is to introduce the terms and procedures of the APAR design technique. Further involvement in more detailed aspects of APAR requires use of the references listed, plus personal involvement in an LSI design.

H. S. Zieper, Advanced Technology Laboratories, Camden, N.J., received the BSEE in 1955 and MSEE in 1959 from Worcester Polytechnic Institute. In 1956, Mr. Zieper joined the faculty of Worcester Junior College, where his responsibilities included development and extension of the entire course of electronics study. Mr. Zieper joined RCA in 1959, being initially assigned to the BMEWS project to develop a digital checkout system for the display information processor. Subsequent assignments involved system and preliminary logic design for a number of general-purpose processors. He was a key member of the group that conceived and developed the RCA 4100 series of central processors; this work involved the specification, design, and checkout of software operating systems for the RCA 4000 series of equipment, and consulting work during the system design of the RCA 3301 family. In 1965 Mr. Zieper was promoted to Group Leader, with responsibility to direct research programs in areas such as the use of large-scale bipolar arrays in high-speed machine organization. Since that time, Mr. Zieper has been directly responsible for the development of a family of logic simulation systems ranging from the gate level to the system level. Mr. Zieper assumed the position of Manager, Computer Systems Research and Applications, in 1970. This group has a wide range of activity, covering the design of LSI microprocessors using CMOS technology through software studies, including a variety of digital-system and logic-simulation efforts. As manager of the Applied Computer Systems Laboratory, he was responsible for the enhancement of the CMOS D/A system, development of hybrid techniques, and the implementation of the SUMC-DV hardware. In 1973 Mr. Zieper was appointed Staff Engineer to P.E. Wright, Director of the Advanced Technology Laboratories.

Anthony R. DeMeo, Advanced Technology Laboratories, Camden, N.J., received the BS in Physics (*magna cum laude*) in 1965, and the MS in Physics (*summa cum laude*) in 1967, both from Fairleigh Dickinson University. From 1967 to 1970, he worked as a Research Physicist for the St. Regis Paper Company at their Technical Center in West Nyack, N.Y. At St. Regis, Mr. DeMeo conducted research on the photoconductive nature of Zinc Oxide and its behavior in relation to the parameters affecting Electrofax base papers. At this time, he also conducted the development of papers for use in electrostatic facsimile systems. In 1970, Mr. DeMeo was employed by the Pearl River Public Schools in Pearl River, New York as a teacher of I.P.S. Physical Science. At Pearl River, he developed a Career Education course for middle school students and participated in the development of a Career Education training program for teachers. During his tenure at Pearl River, Mr. DeMeo was employed on a part time basis by E.G.&G., Inc. at Bedford, Mass. where he was involved in satisfying paper requirements for the Weatherplotter Facsimile System as well as a newspaper facsimile system. In October 1973, Mr. DeMeo joined the RCA Advanced Technology Laboratories where he is a member of the Engineering Communications Group.

RCA has led in the development of processes for CMOS technology, and has also pioneered the design techniques necessary to reduce the initial cost of using the CMOS in one of its most attractive forms — Large Scale Integration (LSI). The Automatic Placement and Routing System, termed APAR, is one RCA-developed approach to LSI design using CMOS technology. The key component of the APAR system is a computer program which determines circuit placement and wiring interconnection on the surface area of an integrated circuit. The viability of this approach was demonstrated in the design, fabrication, and delivery of four computers (each different in nature) and the use of APAR by the Government Communications and Automated Systems Division in a major DOD project.

Definition of terms

Starting at the top level of the system, a primary goal of the system is a working LSI chip (Fig. 1). Some of the terms used in the APAR system to describe LSI chips are highlighted in Fig. 2. Such chips may be procured from the Solid State Division (SSD) or the Solid State Technology Center (SSTC) either as single chips or as dual-in-line packages or flat packs ready for assembly.

LSI chips may be square or somewhat rectangular, have dimensions up to 250 × 250 mils using the metal gate MOS technology, and contain the equivalent of 200 to 600 logic gates. The SOS technology extends the gate count upward toward 400 to 800 gates. Depending on the packaging practice involved, the chip may have as many as 100 I/O connecting pads.

The size of the chip, as well as the number of I/O pads used for connection to outside systems, depends upon the user engineer's proficiency in the assignment of functions to the chip (partitioning) and his skill at using the options provided by the APAR system. These factors usually depend upon his experience with the system.

As can be seen from Fig. 2, within the chip area are rows of pairs of small rectangles (or "cell row pairs"). These

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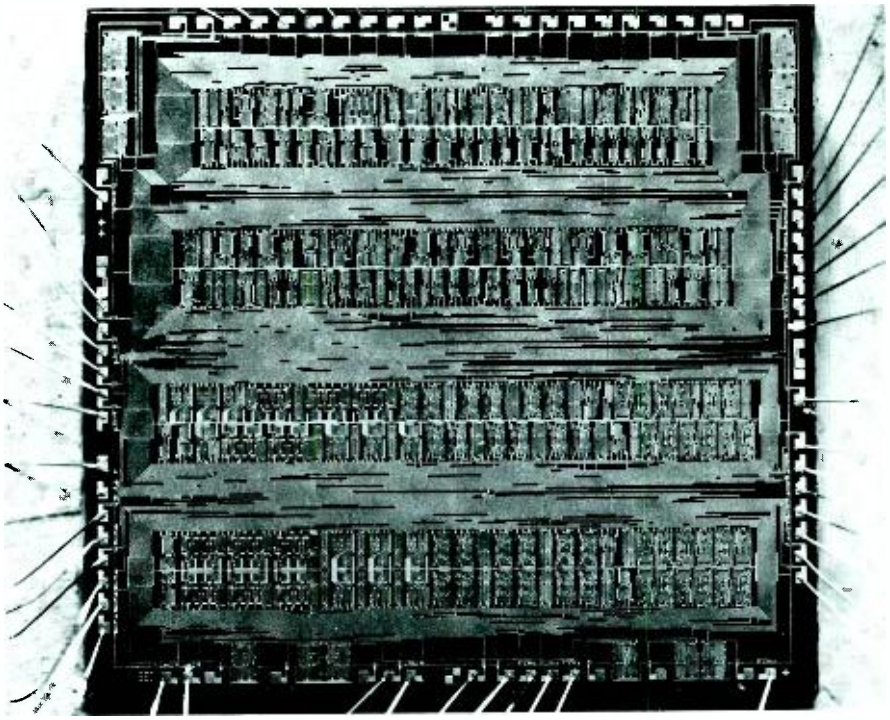


Fig. 1 — Microscopic photograph of a typical chip.

rectangles are devoted to circuitry. Each circuit is a custom layout of a basic logic function typically containing the transistor configuration required to implement a specific function (*e.g.* 4-input NAND or an exclusive OR).

The cells may contain virtually any function required by the designer. A catalog of available cells is contained in Ref. 1 of the Supplementary Materials listed at the end of this article. This "CMOS Standard Cell Library" contains the current set of cell functions. However, new cells may be added by means of a well documented and proven method, if the economics of the design warrants it. Hence, the catalogue of cells is continually updated as new cells are designed and subjected to approval cycles to guarantee that they are qualified for use in rigorous environments. The Standard Cell Library data for a given cell consists of a standard cell number, a logic symbol, a schematic, and a truth table. Information pertaining to propagation delay versus output-node capacitance is also presented as well as the logic equation for the function.

Each cell is an optimized circuit layout which minimizes area, subject to the constraints of the process rules. However, for the convenience of computer programs, the outline topology of the standard cell is standardized and all interconnect points are at the bottom of the cell. Fig. 3 is an outline drawing of a standard cell. Also, for the convenience of the design automation programs, the standard cell is a constant height. Various functions are then accommodated by changing the width.

As shown in the outline sketch of the chip (Fig. 2), the interconnections between cells are done by what is effectively a two-layer system. Most interconnections are made by deposited metal. However, some connections are made by a diffused layer which is not metal and thus has a larger resistance that tends to reduce system speed. Connection between the diffused layer of wiring, and the metal layer of wiring is accomplished by means of the "tunnel ends" shown on the sketch. Because some designs contain critical timing paths, the APAR system provides flexible manual intervention techniques to make any path all metal, and in some cases shorter in length.

An immediately obvious feature of an APAR chip is the unusual location of the cells (circuits). These cells are placed end-to-end in rows and then pairs of rows by the key part of the system — the Placement and Routing programs. As mentioned previously, such cell organization is a necessary compromise between hardware and computer programs to achieve a working system and an effective design. This organization also helps reduce chip area and thus maximize yield.

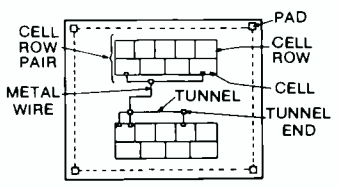


Fig. 2 — Terms used in describing a typical LSI chip.

It should be noted here that the APAR system is designed to minimize initial design cost while providing a high level of integration. Trade-offs between design costs and the level of integration must be constantly evaluated in order that the most appropriate RCA design approach is used for a specific volume of parts.

Goals and targets

As noted above, a primary concern in LSI implementation is a fast turnaround cycle for new designs or design changes. Thus, APAR has been designed to provide a simple engineer-to-manufacturer interface for a wide pool of engineers. To prevent obsolescence, APAR has been developed to be applicable to all forms of the MOS technology and to grow with these technologies.

Initial specifications are usually changed during prototype design. Consequently, the design automation system must be able to accommodate new functional requirements quickly and efficiently. Such an ability is built into APAR.

Furthermore, ATL is committed to make APAR amenable to all forms of digital logic, not just to a specific subset (such as computers). The APAR system is designed for digital logic design in its broadest sense. Therefore, the plan is to extend APAR (*e.g.*, to linear and analog functions) as necessary for total product applicability.

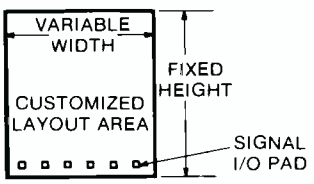


Fig. 3 — Outline of a typical APAR cell (metal gate technology).

Design fundamentals

The APAR design process starts with the creativity of the engineer and the tools that are at his disposal. These tools include computer programs and the resultant logic diagrams. The design automation computer programs, listed below, are at the heart of the APAR system.

LOGSIM — a program which validates digital logic by dynamically simulating logic operation at the element level.

FETSIM — batch program, written in Fortran IV, for dc and transient analysis of MOS cirucits.

AGAT — a program designed to generate a complete set of tests for a combinatorial logic net.

TESTGEN — interactive program which tests sequential logic.

PR2D — two-dimensional placement and routing program which is used to place standard cells in various rows on the surface of the proposed chip and determine routing of connections.

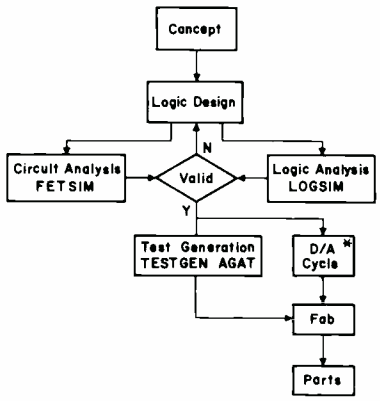
ARTWORK — software sequences which are required to produce artwork tapes or drive a checkplot facility.

MANMOD — a software system which enables the user to intervene in the automatic placement of cells.

These programs are used in the order shown in the design flow chart of Fig. 4.

In executing the concept phase of the design project, the user must always bear in mind that his end product will be built of LSI chips. Consequently, even though the designer is mainly concerned with system function, some of his thoughts must reflect the constraints of pin/gate ratios, chip size, second-level packaging, *etc.* Such balanced design considerations will enormously simplify the problems of hardware implementation when that phase of the project is reached. Following this conceptual phase is the step of traditional logic design.

Detailed design begins with the creation of functional logic. Here it is important for the user to keep in mind the segmentation of logic according to function, since these segments will turn out to be individual cells. Gate and pin count are clearly vital considerations at this point. Also, one must begin to consider the problem of testing by making sure that there are lines available in the logic for setting initial conditions. This takes up a pin or two, but saves a great deal of



*This box refers to the use of the PR2D, ARTWORK, and MANMOD programs.

Fig. 4 — Design flow using the APAR system.

trouble later on when debugging the system. During this stage of design, critical timing paths must be defined, since, once a part is made, it is impossible to add a gate or remove a delay. As one performs detailed design, consultation should be held with experienced circuit designers and semiconductor manufacturing people to be sure the capabilities of the technology are not exceeded in terms of speed, drive capability, *etc.* Finally, there are cases where a particular system must interface with parts that are not implemented in CMOS technology. Where this is a consideration, thought must be given to the mechanization of technology interfaces.

Let us now consider the logic process. Normally the designer develops his logic in terms of ANDs, NORs, flip flops, *etc.* The APAR system deals with cells, some of which combine several logic functions. Therefore, the designer must make the translation from his "engineering" logic to "cell level" logic.

As shown in the flow chart (Fig. 5), FETSIM and LOGSIM provide a complementary pair of design analysis tools. These simulation programs are a computerized way of doing what the engineer normally would have done with a bread-

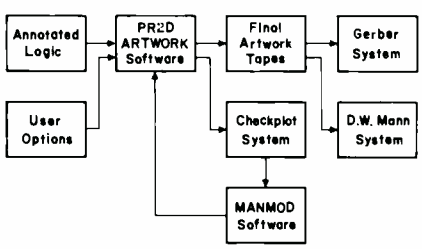


Fig. 5 — System structure for the use of PR2D, MANMOD, and ARTWORK programs.

board and pencil and paper to analyze a prototype design. Basically, it tells the engineer how his circuit or logic design behaves — relative to his own definition. Hence, simulation is only valuable to the extent that the engineer asks the important and relevant questions. The amount of simulation to be performed on a design depends on the degree of confidence expected. When working with LSI, a rather generous amount of time should be allocated for the use of simulation aids.

LOGSIM

LOGSIM is the logic design simulation tool. It enables the engineer to interpret the requirements of the user and to test the logic before any hardware has been built.

LOGSIM was developed independently of the standard cell library. Hence, the design engineer has two alternatives. After he has designed his logic, he can go from functional logic directly into LOGSIM symbology and then into a standard cell translation. The other alternative is to do his logic design directly in terms of standard cells and then translate to LOGSIM symbology. It is important to note that the latter alternative has many equivalent translation forms and great care should be exercised in its use. This problem arises because the standard cell library contains functional forms not available in LOGSIM. Eventually an automatic translation between standard-cell notation and LOGSIM symbology will be provided.

LOGSIM has three basic features of interest to the designer. First, LOGSIM replaces the physical breadboard; it is, in a real sense, a simulated breadboard of the logic being designed. Second, LOGSIM has an easy-to-use English input coding. Finally, it produces an output which is recognizable and related to the goals of the designer.

One of the primary tasks of LOGSIM is the analysis of gate interconnection. This is an area in digital logic where a great deal of difficulty is usually encountered. Interconnections are inadvertently made in the wrong fashion. For example, a particular control line may not be distributed to all the places it ought to go. LOGSIM provides an output which lists the source of every signal and tells precisely where it goes in the logic network.

Another function of LOGSIM is timing verification. LOGSIM generates a print-out of waveforms on a convenient scale.

Next, LOGSIM contains an option which causes the program to look for race conditions in the logic. As signals change in any digital network, there is a lack of stability in the outputs of the gates until the rise and fall times of the gates pass. Hence, there is potential for a race condition. LOGSIM identifies where such conditions exist and how big they are. The engineer must then decide whether a particular race condition is allowable.

Thus, LOGSIM helps the logician finalize the logic design, capture it in writing, and spot errors before part fabrication. In addition, LOGSIM provides a hard copy output that can be updated on a continual basis. Such output contains the connectivity lists and timing data that are needed when checking out the logic system after hardware has been built. Use of this tool relates to the initial goals of the APAR system in that it provides the most current design data in an organized form and significantly helps to lower error design rates.

FETSIM

The FETSIM program is a circuit analysis tool which has a number of uses. The first use is validation of cell operation at the device level. The second is characterization (*e.g.* gate delay as a function of output-node capacity, temperature, or process variation). The use of the FETSIM program in this case also enables the user to define a set of worst-case conditions which provides characterization for the circuit design. The third use of FETSIM, and perhaps the most important for the user, is in the analysis of critical timing chains in the logic. For example, in an adder circuit, the amount of time required for a carry to propagate through the circuit is critical. With FETSIM, the particular paths of the adder network can be simulated in detail, and the results presented to the logician. The logician then could use this information to help define system clock needs.

The actual mechanics of using the FETSIM and LOGSIM computer programs, along with the information and materials required, is rather lengthy and therefore will not be presented here. The reader is referred to Ref. 2 for an extensive discussion FETSIM and LOGSIM.

Translation programs

As indicated in the flow chart (Fig. 4), once the designer is satisfied with the nature of his logic organization in terms of function and speed, he is faced with two parallel tasks:

1)Use the procedures to transform a logic diagram into the documentation required to make a chip, and

2)Generate test patterns to verify that the manufactured parts conform to the design.

The translation from logic diagrams to the kinds of documentation that are required by the process groups requires the use of the Two-Dimensional Placement and Routing Program (PR2D).

The system structure for the use of the PR2D program set is shown in Fig. 5. There are two inputs to the program: the original annotated logic and a combination of user options. In the very simplest case, the annotated logic is taken and used as is. The PR2D system takes the original annotated logic, places the cells in various rows on the proposed chip surface, and determines the routing of connectors. This information is then stored in final artwork tapes and may be plotted (as discussed in the section on artwork generation and part fabrication).

However, in the usual case the layout of the chip is analyzed before generating the final artwork tapes. Hence, the usual procedure is to run through the PR2D program and those artwork sequences required to drive the checkplot facility. The checkplot shows the layout of the final chip for a particular logic (see Fig. 6). Here one can see the outline of cells, the projected chip size, the interconnecting wires, and the locations of I/O pads. This piece of information tells the engineer what he is going to see when the part is finished and enables him to evaluate system economics.

The checkplot system actually used should be keyed to the complexity of the project. Checkplot systems range from laboratory plotters, requiring 6 to 8 hours to produce a plot, to production level plotters which are 30 to 40 times as fast as the laboratory plotters.

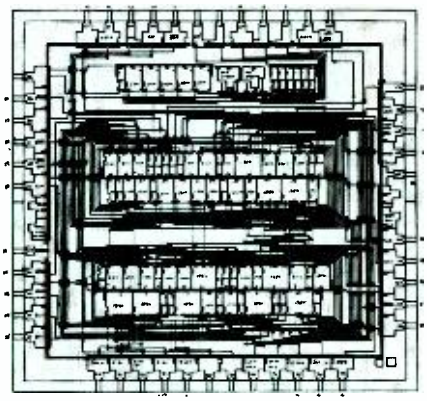


Fig. 6 — Sample checkplot.

With the checkplot at hand, the engineer can make whatever manual modifications seem appropriate. Manual modifications are usually made when dealing with sophisticated chips and are carried out according to the loop (at the center of the diagram in Fig. 5) which passes through the MANMOD software system. In utilizing MANMOD, the engineer tells the program where to place specific cells. This is usually done to minimize the length of wiring between individual cells, but also leads to minimum chip size (while allowing the greatest amount of logic on the chip) and to a system which operates at the fastest possible speed. Manual placement also allows the designer to put buffers or output circuits at places which he feels are most appropriate. The program, in automatic mode, might not choose these optimum patterns.

Many chip designs do not require manual modifications. There are several user options which can be employed to give the automatic placement program some guidance. This additional guidance may be in the form of specific rules that will optimize chip performance. Specifically, the engineer can tell the program where to put rows of cells, or even specific cells. However, if the position is specified, then there is really no placement to be done by the program. Since different plotters are used, there is a user option which allows the engineer to give the system some dimensional scale control. The engineer can also, when necessary, specify the location of critical I/O pads on the chip. This is done to maximize response time of some circuits. The user also has the option of telling the program how many pairs of rows of cells will be placed. These are just some of the basic user options,

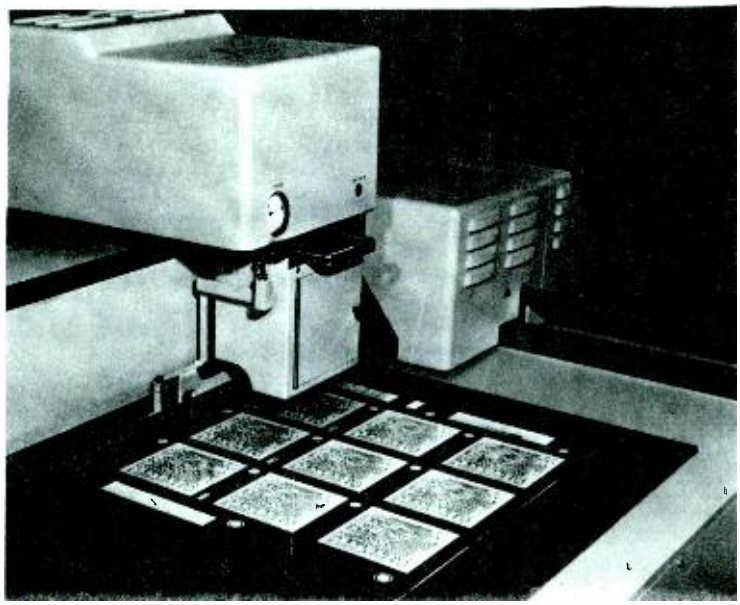


Fig. 7 — Gerber plotter.

there are many others. A detailed discussion of the mechanics of utilizing the PR2D program is contained in Ref. 1. It will suffice here to mention that the PR2D system is programmed to stop at a point where the total net wiring length for the entire chip is a minimum.

Artwork generation and part fabrication

The output of the PR2D program is a series of artwork tapes which contain the necessary data for precision plotter control. Two examples of precision plotters are the Gerber plotter (Fig. 7) and the D.W. Mann plotter.

Once the precision artwork exists, it must be reduced to a size that is usable in the fabrication process. Artwork from a Gerber plotter is usually 80 to 100 times actual part size, and hence must be reduced by a photo-reduction process. The result of the photo-reduction process is a glass plate called a reticle. The glass reticle is about 4 to 10 times actual part size. The output of the D. W. Mann plotter does not require a photo-reduction step, since it is already in the form of a reticle at 10X size.

Next, the artwork must go through a step-and-repeat process. The result of this process is another piece of glass called a mask. The step-and-repeat process takes the reticle from the 10× size down to the final size required for chip fabrication, and repeats this pattern several times on a single piece of glass (Fig. 8).

The masks thus produced are used to produce array of chips, such as that shown in Fig. 9. The chips contained on this wafer must be separated from the array, inspected, packaged, and tested.

To complete the entire APAR design process, the engineer must have the capability to test the chips which have been fabricated. There is always the possibility of an error in logic, or perhaps a flaw in the physical construction of the chip. Hence, the creation of test sequences is a particularly important aspect of APAR.

The concern here is with functional part acceptance tests in terms of quality, as opposed to dynamic part tests in terms of speed. However, when new array types are generated, it is vital to supplement functional part testing by evaluating good chips to determine such things as leakage, sensitivity, and speed.

Fig. 10 is an overall view of the test process. The input to this test process is the final logic design which is going to be implemented on the chip. First, the engineer must develop criteria for acceptance. He must decide what kind of performance constitutes acceptable behavior.

In generating tests to be used on chips, there are two kinds of logic networks of concern. The first kind contains logic which is totally combinatorial. Such logic might consist of adders, encoders, switches, AND gates, and OR gates. For this type of logic, the AGAT program has been developed. The second kind is sequential logic, which contains flip flops or flip flop networks. The program suitable for sequential logic is TESTGEN.

Fig. 8 — A mask produced by the step-and-repeat process.

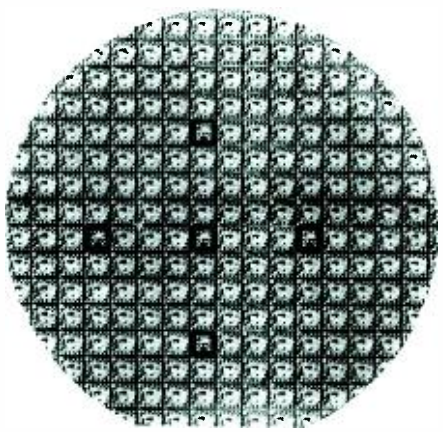


Fig. 9 — Wafer containing newly fabricated chips.

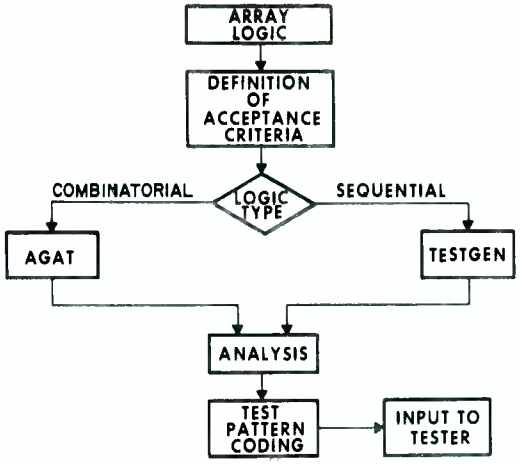


Fig. 10 — The test process.

The task of both AGAT and TESTGEN is the generation of tests which are appropriate for a given logic configuration. The result of using either of these two programs is a series of tables which give "1" and "0" patterns which are then presented to a chip tester to measure a chip's performance.

These programs provide functional tests as opposed to logic analysis. It is also important to mention that both AGAT and TESTGEN are capable of helping the user determine whether a particular failure is a yield problem or a design error. AGAT and TESTGEN also aid in the definition of mechanisms for specifying acceptance testing for large volume production.

A more detailed discussion of Test Generation may be found in Ref. 3 and 4.

Applications

Design automation was originally developed with the design of computers in mind. However, a broad spectrum of RCA products exists which can utilize this technology. Some examples are communications systems, automotive electronics, and government needs such as secure communications systems and data bus systems for aircraft, submarines, and land-based vehicles. Some real examples of the utilization of APAR are shown in Figs. 11 through 13.

Future developments

APAR is expected to grow with the technological developments of SSTC and SSD. In keeping with this intention, several of the computer programs mentioned above are constantly being updated to improve their effectiveness. New programs are being generated in an effort to broaden the applicability of APAR to all forms of the MOS technology.

Acknowledgments

The authors take pleasure in recognizing the efforts of the ATL Applied Computer Systems Laboratory which developed APAR as a team and built the initial working hardware. Furthermore, recognition is made of the efforts of Dr. T. Reboul in helping to distribute information in the form of video tape series, and to Dr. J. Hillibrand for establishing a standardizing system for the basic cells.

References

1. *Standard Cell User's Guide* — Section I of this volume presents a preliminary version of the Standard Cell User's Guide including a catalogue of the basic standard cells which are available for use. A short introduction as to how the user can interpret data is presented. Section II contains a series of user notes relevant to the most efficient use of the PR2D program, as well as artwork, checkplot, and manual modification.
2. *Simulation Aids-FETSIM, LOGSIM* — This volume of user guides presents the operational data required to use the logic and circuit design aids.
3. *APAR COS/MOS LSI Techniques* — This volume contains the entire set of visuals used in the six video tape lessons including a text version of the spoken commentary.
4. *Test Generation — AGAT, TESTGEN* — This volume presents a series of deatailed user manuals relating to the generation of testing sequences for LSI arrays.
5. *APAR Technological References* — This is a volume of supportive documentation containing technical reports and contract reports which detail some of the hardware experience of the Advanced Technology Laboratories in implementing a number of metal gate COS/MOS arrays. Although this material is dated, it nevertheless provides a view of the kinds of performance which can be obtained.

Note: These supplementary materials are proprietary and only available to RCA employees who have a need for their use.

Fig. 11 — The Space Ultrareliable Modular Computer Demonstration Vehicle (SUMC/DV) which was developed for NASA. SUMC/DV is a 16-bit general purpose computer with approximately 35 instructions in its instruction set. Its logic subsystem consists of well over 6,000 logic gates. SUMC/DV was designed, debugged, and delivered in slightly less than one year.

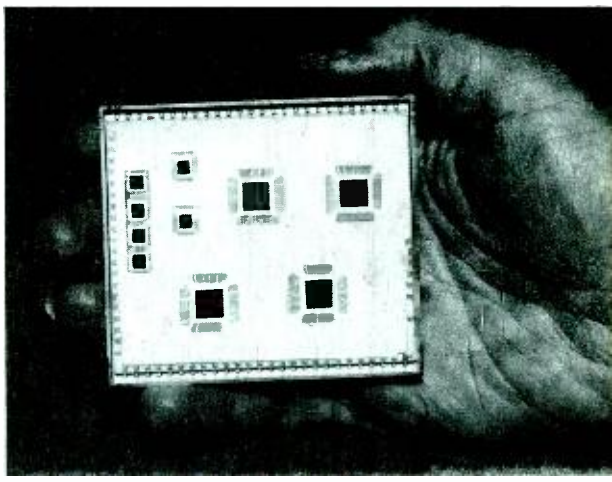


Fig. 12 — A 12-bit general purpose computer which consists of 5 LSI arrays. This computer, known as "B-12", has been reduced to a hand held, single hybrid module.

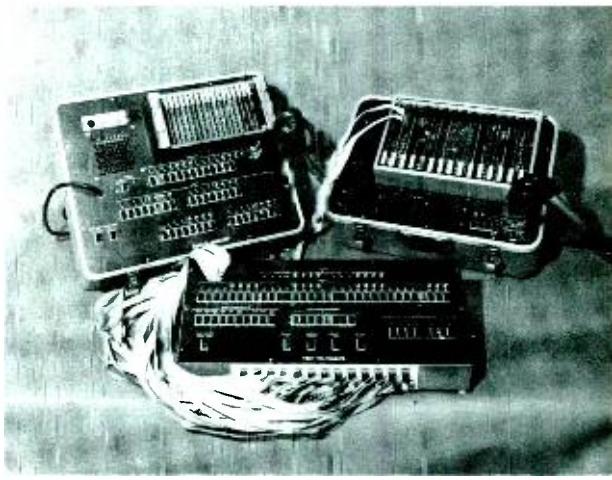


Fig. 13 — A further advance in the utilization of APAR. This device, known as SUMC/Baseline, is 32-bit computer packaged in a pair of suitcases. SUMC/B has a powerful functional capability which has been developed and delivered to NASA under the on-going work which they are supporting.

High speed CMOS-SOS LSI using standard cells

A. Feller | A. Smith | P. Ramondetta | T. Lombardi | R. Noto

Advanced Technology Laboratories in Camden have developed a standard-cell approach for generating low-cost, quick-turnaround custom LSI arrays using silicon gate CMOS-SOS technology. SOS technology, with its extremely high speeds, high densities, and low power dissipation, was developed by the RCA Laboratories and is now in pilot line status at the Solid State Technology Center in Somerville. ATL is presently building the first LSI CMOS-SOS 32-bit computer (SUMC-CVT) for a NASA multiprocessor application to demonstrate the effectiveness of this approach.

THE STANDARD CELL approach for generating low cost, quick turn-around LSI arrays was developed from 1966 to 1968 by Advanced Technology Laboratories in Camden. This system used the automatic placement and routing program (PRF) developed by ATL and became one of the most widely used methods for generating custom LSI arrays for low volume military applications. With NASA support in 1969 and 1970, ATL extended this capability from the PMOS to the CMOS technology. A new automatic placement and routing program was developed, the PR2D program, for the CMOS technology. Using the CMOS standard cell technology, ATL designed and delivered the first CMOS LSI 16-bit computer (SUMC-DV) to NASA. ATL later used this technology to build the first CMOS LSI 32-bit general purpose micro-programmed computer (SUMC-BL) which was also delivered to NASA.

The flexibility of the standard cell approach was demonstrated when ATL designed and delivered the world's first CMOS LSI - microprocessor (B-12) to customers in the automobile industry and a similar version to the U.S. Army Electronics Command, Fort Monmouth. The B-12 microprocessor is a 12-bit microprogrammed general purpose computer designed for real time application.

All of the aforementioned capabilities have widespread use in RCA and have been unofficially collected under the designation of APAR which is now the

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A. Feller, Ldr., LSI Circuits & Applications, Advanced Technology Laboratories, Camden, N.J., received the BSEE and MSEE from the University of Pennsylvania in 1951 and 1957, respectively. He has also pursued graduate studies toward the PhD in EE. From 1951 to 1958, he worked as a design and development engineer in the Broadcast Television activity of RCA. In 1958, Mr. Feller transferred to the Computer Advanced Development Activity. In this capacity he developed high speed circuits and interconnection techniques for proposed new computers. Since 1964, he has been active in applying computer-aided techniques to circuit design. Mr. Feller was promoted to his present position in 1968. In recent years, Mr. Feller directed the design and fabrication of an advanced LSI ultrareliable computer using arrays generated by a design automation technology developed under his responsibility. Mr. Feller has been awarded three patents in high speed switching circuits.

A. M. Smith, Applied Computer Systems Laboratory, Advanced Technology Laboratories, Camden, N.J., received the AB in Physics from Temple University in 1955, and the MSEE from the University of Pennsylvania in 1965. Since joining ATL in 1966, Mr. Smith has been a major contributor in the system design of a large-scale, high-speed general-purpose processor and in the specification of the bipolar LSI arrays that were used to implement this system. He has also participated in several MOS integrated circuit design and development programs. Mr. Smith had prime responsibility for the successful completion of the PMOS standard cell family program. Mr. Smith was also responsible for the development of the aluminum-gate CMOS standard cell family and for the development of 10 arrays using these cells to implement a 16-bit minicomputer. He was also a major contributor to the design of the silicon-gate cell family and its test array development. Mr. Smith has three patents and has submitted several additional patent disclosures.

P. Ramondetta, Applied Computer Systems Laboratory, Advanced Technology Laboratories, Camden, N.J. received the BSEE from the City College of New York in 1966 and the MSEE from the University of Pennsylvania in 1970. He has completed part of the requirements toward the PhD in Electrical Engineering. In 1966 he joined the ATL, becoming involved in the design and development of communication devices employing solid state microwave sources and microwave pumped photoconductors. In 1969 he joined the Computer Systems Research and Applications group where he has been responsible for the design, computer simulation and evaluation of the (standard) CMOS circuit library portion of the "APAR" design automation system. More recently his responsibilities have included designing and evaluating new families of standard circuits for the LSI design automation systems. Mr. Ramondetta is a member of Eta Kappa Nu.

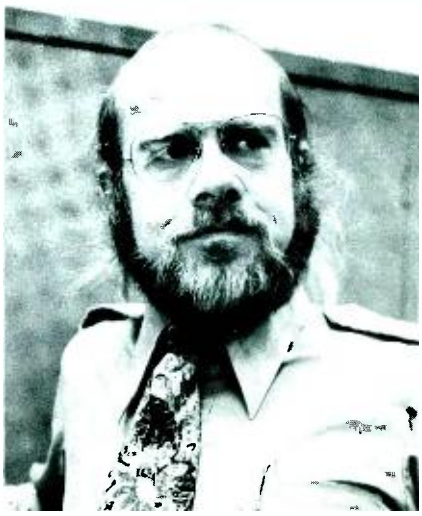


Table I — Comparison of standard cell areas.*

Standard cell technology	Standard cell dimensions Width (mils)	Height (mils)	Area (mils)	Cell area reduction ratio normalized to standard CMOS
Standard metal gate bulk CMOS	9.5	14.0	133.0	1
Dynamic 2ϕ PMOS	6.4	10.8	69.1	1.93
Si-gate CMOS-SOS	5.5	7.0	38.5	3.5

*Standard of comparison: 4-input NOR

basic technology for several major programs.[1]

System design

The development of this system required three distinct but extremely interdependent components:

1) The development of the standard cell circuit topology including the design of a family of standard cell circuits,
2) The design automation programs; and
3) The design of the LSI array topology.

T. Lombardi, Applied Computer Systems Laboratory, Advanced Technology Laboratories, Camden, N.J., received the BSEE in 1971 from Drexel University. Upon graduation he joined ATL, where he has participated in the development of both the bulk CMOS and CMOS/SOS Standard Cell families used for the design automated generation of LSI arrays. Mr. Lombardi has participated in the chip development for three LSI computers. He has also developed a Radiac meter — an application of a special purpose microprocessor to monitor gamma radiation dose and rate. Mr. Lombardi is a member of Eta Kappa Nu.

Basic technology

The basic technology used in this program is the self-aligned silicon-gate CMOS-SOS technology. This technology has the basic ingredients for the almost ideal technology — virtually zero quiescent power, extremely high speed, and high density. The data discussed later in this paper are based on measurements made on a test chip fabricated with this technology.

R. Noto, Applied Computer Systems Laboratory, Advanced Technology Laboratories, Camden, N.J., received the BSEE from UCLA in 1957 and MSEE from Drexel Institute of Technology in 1963. He has also completed work toward the PhD in Engineering at the University of Pennsylvania. Mr. Noto joined RCA in 1961 and was responsible for computer simulation design of control logic, and computer analysis and design of a nonlinear log compression network. In 1966, he joined the Advanced Technology Laboratories as Project Coordinator (Camden) for the 4101C Integrated Circuit Computer Project, a joint effort of six RCA divisions. Mr Noto received an RCA Professional Excellence Program Individual Award for this work. Recently he has contributed heavily to the RCA design automation system for LSI-MOS arrays, and received an RCA Technical Excellence individual award for his LSI-MOS array programs. Mr. Noto also has written other programs in the field of design automation. He has published two technical papers and is a member of Phi Eta Sigma, Tau Beta Pi, and the IEEE.

Cell topology design

The principal design objective in defining the basic cell topology was to determine, within practical limits, those geometrical relationships that would provide the maximum speed with highest device density of minimum chip area. Were it not for the crossover or coupling capacitance between metal and polysilicon interconnection lines, the circuit speed of the SOS technology would be virtually independent of the geometry of the devices. To determine (and then include) the effect of coupling capacitance, an analysis was made of the average number of signal-line crossovers normally encountered in a random logic LSI array. A large number of LSI arrays were statistically analyzed with the result that the average number of crossovers in a typical random LSI array is approximately 40. With this input and some other considerations, a height of 7 mils for the standard cell was determined. Because no guard bands are required (as in the case of CMOS bulk technology), the spacing between input and output pads is reduced to 1.1 mils, compared to 1.9 mils for the metal-gate bulk silicon CMOS technology, resulting in a dramatic area reduction. Table I gives an area comparison for three standard cell technologies including the single channel PMOS technology. The geometries given in Table I describe cells with devices whose basic drive capabilities are about the same. As seen in the Table, with area normalized to the standard metal gate CMOS bulk technology, the PMOS technology (using a dynamic two-phase design) has about twice the density while the area required by the silicon gate CMOS-SOS technology is reduced by a factor 3.5.

Fig. 1 shows the topological layout of a simple four-input NOR circuit. The seven-mil height, as shown, is measured from the center of the ground bus, which passes through the bottom of the cell to the center of the *Vdd* bus. The cells are placed back to back on the array with the *Vdd* bus overlapping so that there is a common *Vdd* supply for two rows of cells. This is a concept similar to the metal-gate standard-cell approach. However, unlike the metal gate bulk standard cells whose input and output

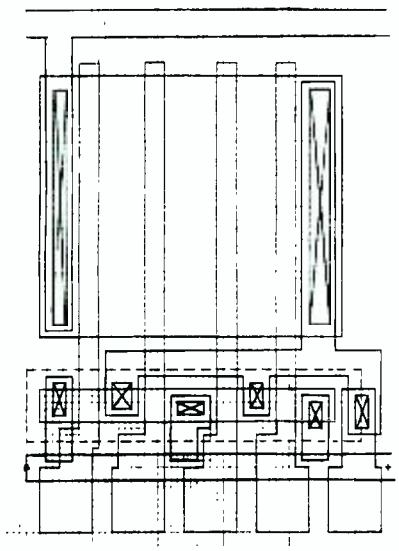


Fig. 1 — Four-input NOR.

connections contained pads or contacts, the input and output connections of the SOS design are padless. This means that if the routing program runs metal to the polysilicon cell input or output connections, it must automatically make provisions for inserting the appropriate levels for a contact. If the external connections happen to be polysilicon, then no further action by the program is required. This capability is but one of the several differences that exist in the SOS placement and routing program (PR2D) as compared to the standard metal gate version. [SSTC has adapted the acronym APAR for the actual program name PR2D].

As can be seen in Table I, the area of the 4-input NOR SOS standard cell is 38.5 square mils. The corresponding area for the metal-gate bulk CMOS 4-input NOR is 133.6 square mils. Thus, the use of the SOS technology has resulted in a cell area reduction by a factor of 3.5. This factor, however, cannot be applied to all the cells nor can it be extended to chip area comparisons since the wiring area is so significant. Nevertheless, it demonstrates the achievable potential of the SOS technology.

CMOS-SOS automatic placement and routing program

Simultaneously with the development and validation of the standard cell circuits and chip topology, a series of modifications were made to the PR2D computer program in order to generate a CMOS/SOS version of the automatic placement and routing program.

Many of these changes are directly technology, circuit, and layout oriented. Changes to the wiring program were made because of padless type standard cells, changes in the power and ground distribution system to replace the bulk technology's conductive substrate, the increased use of buffer driver pads, and the elimination of certain components as a result of the absence of a guard band requirement.

Chip topology

An example of a CMOS-SOS standard cell LSI array is shown in Fig. 2. This is the metal level artwork of an adder chip and is one of 14 chips that are used in the 32-bit SOS SUMC-CVT computer. The adder chip used 65 pads, which determined the chip size of 229 mils×229 mils. It has 279 cells equivalent to 481 gates and contains 1722 devices.

Since the chip is implemented with SOS technology, there are many differences between it and a standard metal gate bulk silicon CMOS array which are not obvious in Fig. 2. However, some differences can be identified. The thick pair of busses around the perimeter of the chip are the basic means of distributing *Vdd* and ground. From these busses, in a fork-like fashion, the ground is delivered to each row of cells from the inside busses on the right hand side and *Vdd* from the inside bus on the left hand side.

To provide a high speed off-the-chip power driver, an output pad was designed that includes a large buffer driver, and as shown in Fig. 2, over twenty are used. This feature not only increases the gate density on the chip because it uses the normal pad area for logic circuits that would normally increase the internal active area, but also it insures the high speed of the buffer by providing to all drivers a metal connection from the output of the drivers to the output pad.

One of the chief advantages of the padless type cells is that the channel adjacent to the cell inputs and outputs is used extensively (under program control) for

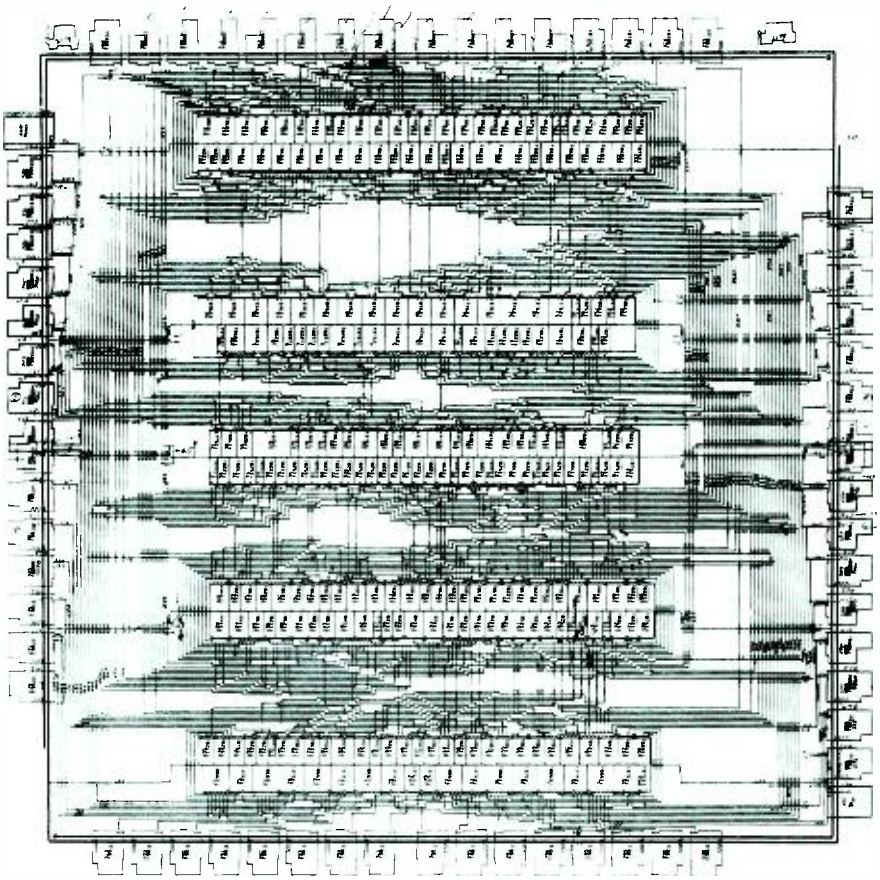


Fig. 2 — Metal level of SUMC-CVT SOS adder.

intercell connections. This saves a considerable number of channels. In addition, because of the elimination of guard bands, the metal-to-metal spacing on the side routing is reduced to 1.1 mils compared to the 1.9 mils required in its metal-gate standard CMOS counterpart. Nevertheless, in spite of these improved wiring techniques and the fact that 10 standard cell rows are used to accommodate more than 1700 devices, the area occupied by the active circuits is less than one-third of the total chip area. This reflects the huge reduction in cell area that the SOS technology permits.

Standard cell data

An extensive family of silicon gate CMOS-SOS standard cells has been developed and data sheets containing propagation delay and appropriate design and circuit characteristics also have been generated. Fig. 3, the data sheet for the 5120 two-input NOR, is an example.

Test chip

A test chip containing nearly 50 unique test circuits was designed to evaluate the basic cell and chip design concept, the actual circuit configurations, the dynamic performance characteristics of the cells, and the extensive changes in the placement and routing algorithm. (See Fig. 4.) Another important objective of the test chip was to validate and update the parameter values of the device model used in the simulation techniques upon which the original designs were based.

In essence, the test chip contains almost 30 cell types of two CMOS-SOS standard cell families. One of the cell families is the seven-mil height family which is the principal subject of this paper. The other family is a 5-mil height family of cells especially designed to meet the special needs of a military contract. Many of the cells exist individually with the input and output leads brought out. This permits individual characterization, leakage measurement, and cell data accumulation. In addition, many of the cells appear, as shown in Fig. 4, in a logic chain. The logic chain is the principal means by which on-chip propagation delay was determined and, as a consequence, became the principal technique for validating the values of the simulation parameters of the device model.

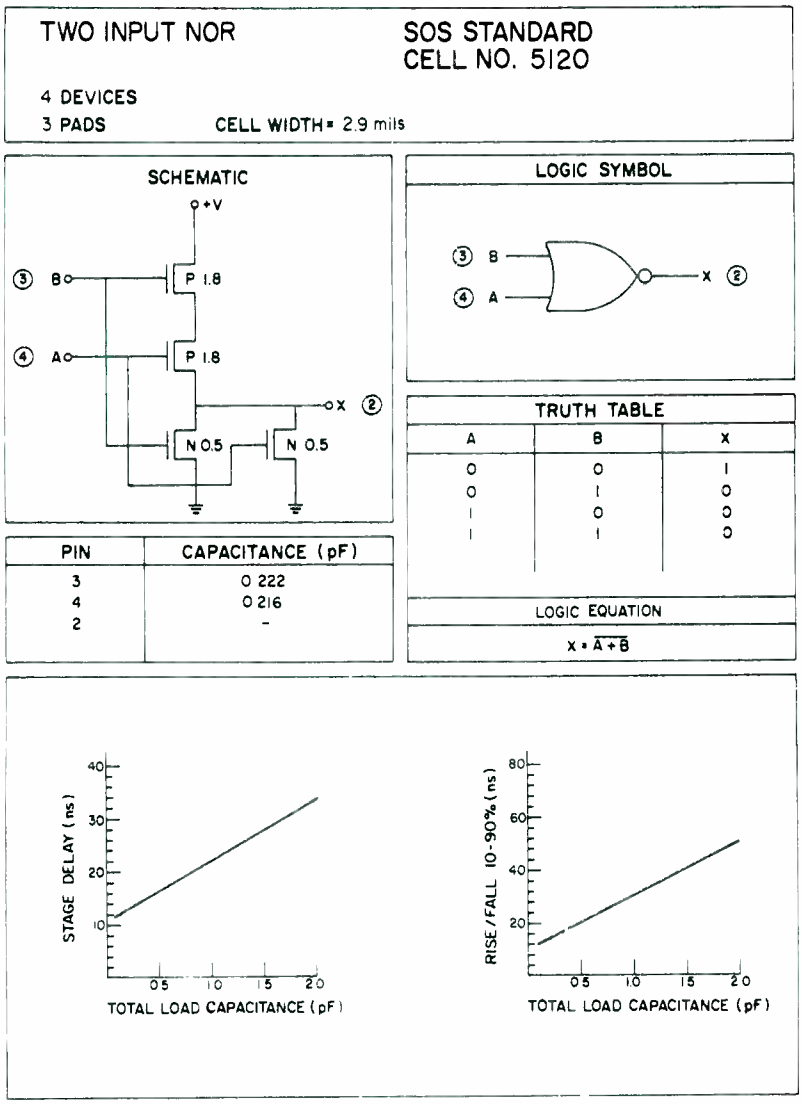


Fig. 3 — Data sheet for the 5120 two-input NOR gate standard cell.

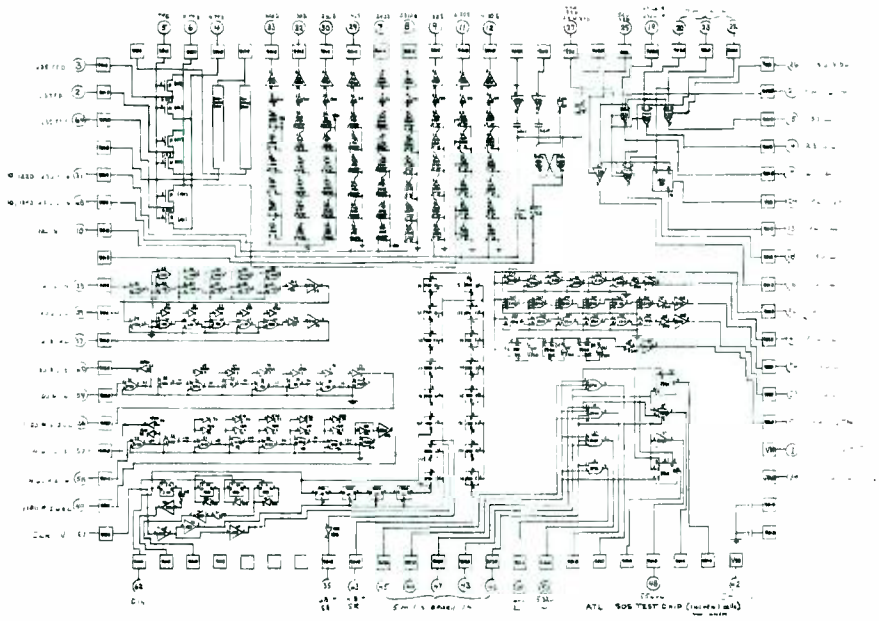


Fig. 4 — CMOS/SOS standard cell test chip.

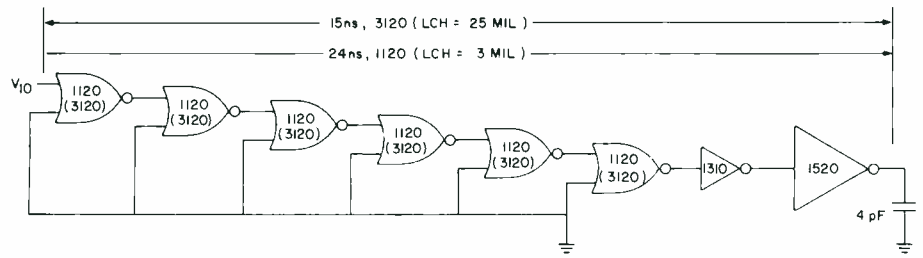
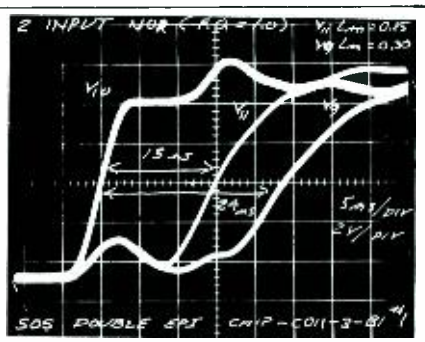


Fig. 5a — 1120 and 3120 logic chain test circuit.



Fib. 5b — 0.25 mil gate and 0.3 mil gate two-input NOR measured delay.

The test data and results discussed in this article reflect measurements made on test chips fabricated at Somerville.

Highlights of test results

This section contains only a few of the highlights of the extensive series of tests and measurements made on more than 50 test chips.

Propagation delay

The propagation delay was measured through the 8 stages of the 1120 and 3120 logic chains; see Fig. 5. The input-output pins for these logic chains are identified on Fig. 4. As shown in the scope photograph (Fig. 5b), the delay for the 0.25-mil channel logic chain is 15 ns while for the 0.3-mil channel logic chain, the measured delay is 24 ns. Note that the 1310 and 1520 inverter buffers are 0.3-mil channel devices in both chains. It is only the two-input NOR cells whose gate widths differ in the two tests. Allowing a 6-ns delay through the two inverter buffers (a conservative estimate considering that the 1520 buffer is driving an off-the-chip external load of 5.5 pF) the delay through six 0.25-mil two-input NORs is 9 ns (or 1.5 ns/stage delay). For the 0.3 mil two-input NOR chain, the delay is 18 ns or 3 ns per stage. These delays correspond to a fanout of one. Based on 0.3-mil cell measurements, the average stage delay is 6 ns for the 0.25-mil two-input NOR stage for a fanout of three, including the effects of an 1800-ohm series interconnection resistance.

Three-stage counter performance

Another good measure of the performance potential of the CMOS-SOS technology can be obtained from the dynamic measurements made on the divide-by-8 counter test included on the test chip and shown in Fig. 6a. It must be emphasized that the principal reason this counter was incorporated into the test chip was to provide a convenient way of verifying that the flip-flop standard cell was operating normally. This cell was not designed for high-speed operation.

Nevertheless, the maximum clocking rate of the divide-by-8 counter varied from 65 to 80 MHz (as shown by the table in Fig. 6b and the waveforms of Fig. 6c). Conservatively, it is estimated that had a special effort been placed on the design of a high-speed counter, clocking rates of 140 MHz or greater could be expected.

Future work

As indicated earlier in this paper, extensive effort is planned in developing and implementing new approaches to improve the efficiency of the wiring algorithms and techniques to significantly reduce the area occupied by the wiring.

Acknowledgment

The authors gratefully acknowledge the contributions of W. Rauch who did much of the analysis, simulation and measurements of the test chip and demonstration chip. The authors also acknowledge the valuable contribution of the design automation coordinators, F. Bertino and J. DeLuca who had the responsibility of generating artwork tapes from initial engineering designs and T. Sullivan who contributed both in the design and checking cycle and the testing phases.

In addition, the contributions of the following people are gratefully acknowledged: H. Borkan, D. Woo and S. Policastro of SSTC for processing of the first test chip; T. Athanas, H. Clarach, and S. Eaton of SSD for processing the test second test chip; and T. Mayhew, K. Long, and A. Woodhall of SSTC for the dicing and packaging of the test and demonstration chips.

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1. Zieper, H. and DeMeo, A: "APAR design automation system — an overview," *this issue*.

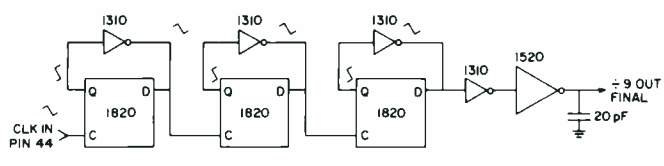

Fig. 6a — Divide-by-eight counter test circuit on test chip.

Chip No.	*Max. Clock Freq. (MHz)*
TC101	75
TC102	66.7
TC103	78.1
TC106	80

Fig. 6b — Maximum clocking rate at Vdd = 10V.

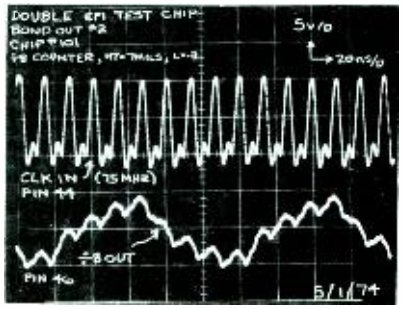

Fig. 6c — Measured clocking rate.

Computer-aided design at AED

F. Gargione| T.P. Murphy

Computer-Aided Design techniques presently in use at AED are described — including a novel approach to data capture, which has been mechanized using a Digitizer and supporting computer programs. It also details the flow of work from data capture through interactive graphic manipulation on the Applicon to the generation of ComputerAided Design manufacturing tape for the production and test of welded-wire boards. A group formed within AED has the objective of assisting the design engineers with their CAD endeavors.

COMPUTER-AIDED design (CAD) has been used at AED for the past several years for electronic-circuit hardware, supported by programs developed by the Scientific Programming activity. The status of CAD has recently been formalized by the establishment within AED of a group to carry out all related aspects of the work needed for electronic design.

The aim of the group is to provide the design engineer with tools that reduce non-creative work required to design and produce equipment. Design engineers are consulted in defining the system, so that their particular needs can be taken into account; accordingly, programs are structured to shift as much work as possible to the computer, while giving the engineer control of the key design decisions at each step of the way.

One stumbling block that prevents wider usage of CAD techniques is the difficulty of specifying the input — an operation often required several times for each design, since various programs (having different input characteristics) are needed.

RCA, as a corporation, has recognized this problem and is investing in the development of a unified CAD data base and associated input language. The intent is to convert all CAD programs to accept inputs from, and return outputs to the data bank.

Until this system is available, AED has chosen to mechanize the capture of data so that design engineers are not burdened with the vagaries of various input languages. The task of specifying the inputs can now be carried out by supporting personnel.

The first function to be mechanized is the specification of schematic-diagram input data. The scheme chosen hinges on the use of a Digitizer, a device composed of a flat table, a pointing device, and circuitry to indicate the location of the pointing device on the table surface (see Fig. 1). This approach is an outgrowth of the system developed by SSTC for capturing graphic data for LSI designs.

Fig. 1 — The Digitizer equipment.

The Digitizer is structured so that part of the table surface indicates commands to be executed and the rest of the table area accomodates the input sketch to be specified. The command area, or *menu*, contains all the electrical, electronic symbols needed to draw schematic diagrams, alphanumeric characters, and other control characters. Once the sketch is mounted on the table, the lower left and upper right corners are indicated and then *menu* symbols can be specified to be drawn within the specified area of the sketch.

Positional data resulting from digitizing the sketch is converted by an AED-developed program to input code for *Audodraft* — a system of M&SR programs used to generate schematic diagrams and net lists. An input to the Digitizer and the resulting output are shown in Figs. 2 and 3.

Frank Gargione, Manager, Computer-Aided Design and Test, Astro-Electronics Division received the BSEE in 1961 from Drexel Institute of Technology and the MSEE in 1965 from the Moore School of Electrical Engineering, University of Pennsylvania. He joined AED in 1967 and was responsible for the specification, design, test, and production follow-up for digital, analog, and data processing equipment for spacecraft. Later, as applications engineer in Microelectronics Technology, he was responsible for selection, design, evaluation and test of thin-film hybrid circuits manufactured in the AED facility, and participated in the evaluation of vendors for circuits procured outside of AED. His previous experience at Vector Division of United Aircraft Corp and at General Electric Company encompassed thick-film hybrid circuit techniques, aerospace equipment design, and systems engineering. At the present, he is responsible for the integration of CAD techniques in the design of spacecraft electronic hardware from data capture to test. Mr. Gargione has authored several papers in the field of hybrid technology and has contributed to the RCA Thick-Film Hybrid Handbook and to a CEE video tape course on thick-film circuits. He is a member of Eta Kappa Nu.

Thomas P. Murphy received a BS in mathematics from St. Francis College in 1966. After graduation he served in the Air Defense Command where he developed computer programs which provide monthly missile readiness reports to the Department of the Army. In 1974, he received an MS degree in computer science from New York University. Prior to joining RCA in 1973, he was a senior systems specialist for the data services division of Control Data Corporation. While at CDC he was responsible for the maintenance of the SCOPE operating system and the FORTRAN EXTENDED compiler, the development of several improvements to SCOPE's console-display subsystem, and an extension to the EXPORT/IMPORT communication handler which provides a separate tape status display station to facilitate magnetic tape operations. He is currently the lead programmer of the CAD software development effort at AED. He is responsible for the specification, design and implementation of new software to assist hardware design engineers and manufacturing, for studying existing RCA programs available at other divisions to determine their applicability to the requirements of AED, and the maintenance and improvement of existing AED programs. He is a member of the ACM and its Special Interest Group on Operating Systems.

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Authors Gargione (left) and Murphy.

The approach can be extended to provide input for any type of CAD program. When the CAD Data Base becomes a reality, AED will change the program to generate CAD input language so that the same technique can be followed, using the same type of input from the engineer and following the same digitizing approach now used.

Electrical design cycle

The flow discussed in this section is not unique to AED; it is described as a means of introducing the topic. The design cycle begins with the engineer generating a schematic diagram for each board in his black box and a connection diagram (net list) that specifies how the boards are interconnected. The schematic is the culmination of the engineer's effort in interpreting the specification and is usually backed up by either analysis, laboratory data, or both.

When the initial work is completed, the packaging effort begins. At AED the two alternatives available are printed circuit boards (usually multilayer) and welded-wire boards. The printed-circuit board packaging follows the conventional approach, but packaging of the welded-wire boards is believed to be unique to AED, at least within RCA. In this approach, pins are inserted into relatively thick PC board laminates carrying a copper ground and power plane, to which the appropriate pins are soldered. The remaining connections are made by welding thin nickel wire to the pins as specified in the net list. Components are attached to the reverse side by either welding or soldering. This approach is usually chosen for high-density circuitry, especially logic designs where it is difficult to design a PC board having a small number of layers; this approach also facilitates the removal and addition of wires as necessary, a highly desirable feature.

After fabrication, the boards are subjected to test to insure proper operation. PC boards require only functional testing, but in the case of welded-wire boards, a continuity/isolation test performed after wiring and before component installation ensures that no connection errors exist. This continuity test is carried out on automatic, tape-controlled equipment described later.

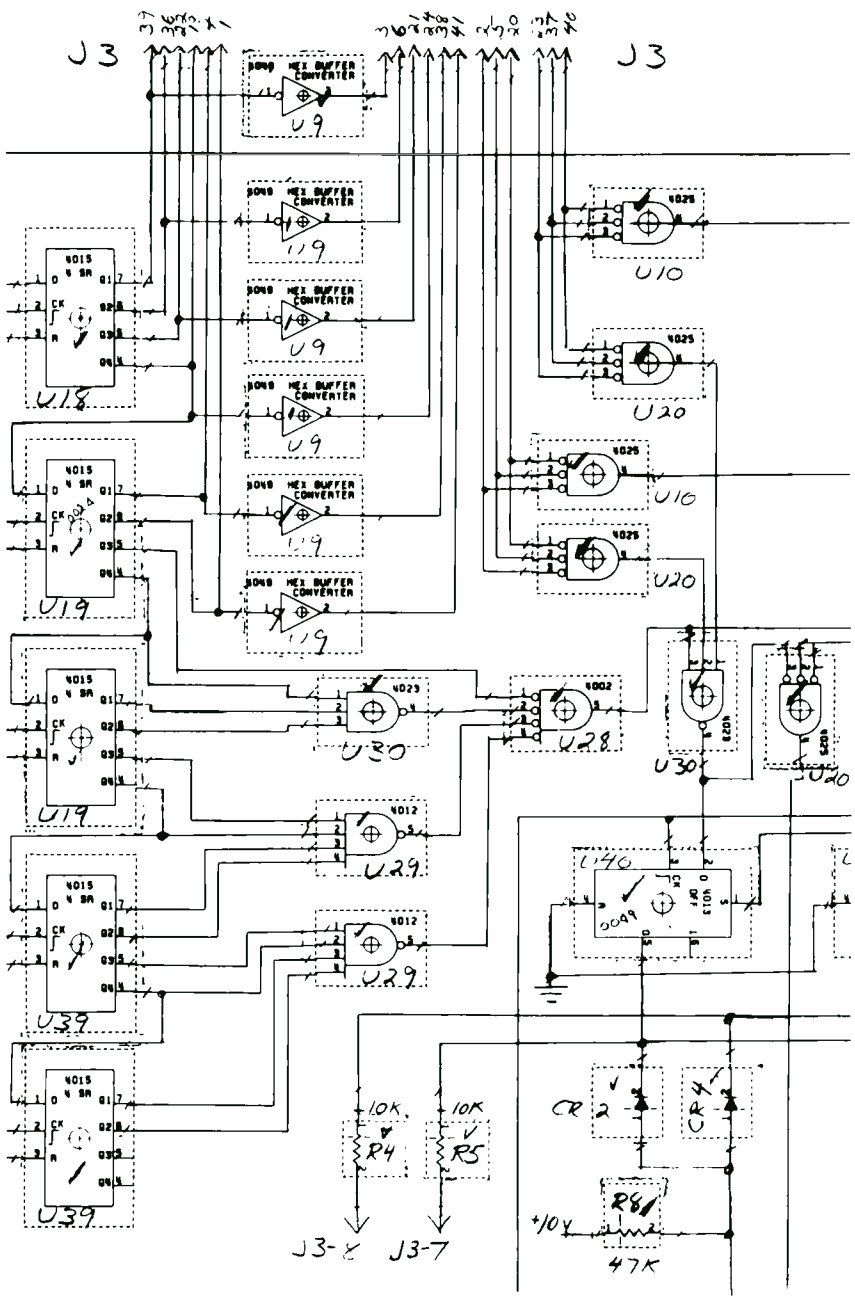

Fig. 2 — Portion of a typical input sketch using the stick-on symbols. The bull's-eye on each symbol indicates its center for the purpose of digitizing. The dotted line is the clearance diagonal indicating the space that is forbidden to the router in running interconnecting lines. In the case of discrete components, the bull's-eye is replaced by a simple center line.

Functional testing is dependent on the circuitry, rather than on the fabrication technique, and therefore can be considered the same whether the board is a PC or welded-wire type. Tests are carried out either on a computer-controlled tester or on specially built test equipment (STE), depending on particular project or scheduling requirements. The computer-controlled test equipment is described later in this paper.

Present status of CAD at AED

Having described the aim of the CAD group and the work to be accomplished, we will briefly survey the areas where CAD techniques are presently used and how they are implemented.

Circuit analysis

All designs used aboard spacecraft are

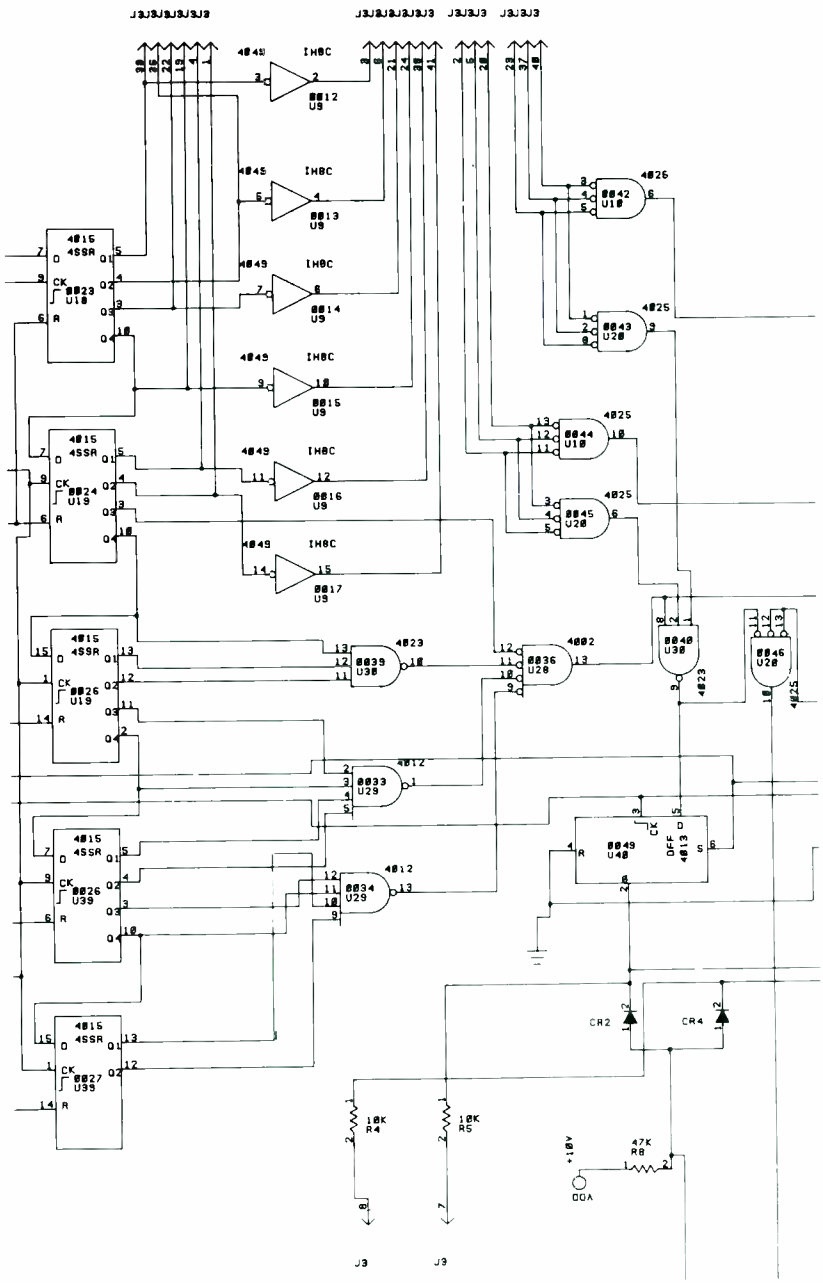

Fig. 3 — This shows the output of the Autodraft system for the input of Fig. 2. Note that the component pins have automatically been renumbered and the routing of the connecting lines has been accomplished. Some work on routing remains to be done to avoid unnecessarily cumbersome paths, such as may be seen at component U 29.

worst-case analyzed to determine end-of-life performance. The analysis is usually carried out on individual circuits, rather than entire boards, using commercially available programs on timesharing systems. The program used most for linear circuit analysis at AED is RECAL 11 by *Rapidata*, since this system allows ac, dc, transient, and worst-case analysis from the same input. The program is somewhat more expensive to run than some competitive systems; but, since it was the first one to gain acceptance, there is a reluctance on the part of the engineers to switch to something else, especially when the program is not used continuously by any one engineer.

RCA's R-CAP has been used for LSI chip design both on NTSS (the Laboratory's time-sharing system) and the batch version on the MIS Series 70/45 at AED.

For logic circuitry, CAD techniques are not used as much, but at least two programs have been used: RCA's *Testgen*, for simulation and fault isolation, and *Rapidata's Logic*, for simulation and timing checks. *Testgen* has been used very effectively in generating test patterns for some in-house designs of LSI chips.

Schematic generation

Schematic diagrams are processed by using the M&SR *Autodraft* system. At AED we have departed from the conventional approach by using a Digitizer to capture the data. Schematic inputs are prepared by the engineer at half-scale, using stick-on symbols on gridded,C-size paper. The half-scale size makes the schematic inputs easier to prepare on a standard desk pad; precise symbols are needed since program searches for the pins (component connection points) depend on exact relationships of the pin locations to the center of the symbols.

When digitizing, first, the location of each element is specified in order to derive the *Autodraft* placement. Next, the nets are digitized by indicating the center of an element and related pin — and then the pin and center of the second element in the net — and so on until all elements in the net are specified. The reversal of the center-pin relationship is done to make digitizing more natural — since, as the net line is followed, the pin on the second and subsequent entries is encountered first. During placement, in addition to the element type and location, the Digitizer specifies unit number, logic name or component value, net names as required; and deletes from the symbol any pins not connected.

When starting to digitize, the drawing can be placed anywhere on the table, but the lower left and upper right corners must be indicated; in addition, the grid increment must be specified so that all entries can be placed *on grid* to correct for positional errors resulting from digitizing.

Needless to say, the data, when digitizing, must be entered in a prescribed sequence, so that it can then be placed in the appropriate field and end up at the desired point on the final output.

The positional data from the Digitizer is presently stored in NTSS files; it is then formatted and written to magnetic tape. The tape is the input to the *Autodraft front end* (AFE) program which

Fig. 4 — The Applicon equipment.

generates *Autodraft* input code: both placement and net statements. The program also produces a list of unused elements in multiple-element packages and a parts list of all electrical parts in the schematic.

The AFE program automatically assigns package pin numbers to replace the sequential pins used on the stick-on symbols. In the case of multi-element packages, pins for each element are entered in order, unless a specific set is specified in digitizing.

The output of the program is a listing and a deck of cards. The listing contains information on a statement-by-statement basis about any incomplete or inconsistent set of data, along with information about pin numbers that could not be found. The output listing is given both in terms of the stick-on symbol pins and the corresponding package pins. In addition, to aid in finding the affected area, the x-y coordinates are printed for pins not located. Corrections required are made on the card deck before submission to the *Autodraft* system.

At the present time we have a *menu* that contains all discrete components, approved linear IC's in use at AED, and approved COS/MOS logic elements.

The system can be easily adapted to digitize other logic lines by simply using a different parts library that specifies the part number and pin numbers corresponding to a given gate or flip-flop; however, in the case of MSI chips, new symbols may have to be added since there is not necessarily any correspondence between competing logic familites. The *Autodraft* system produces a graphic file and a net list. The graphic data is edited on the *Applicon* graphic interactive system, if necessary, and then plotted to produce the final diagram. A view of the *Applicon* equipment is shown in Fig. 4. The net list is used as input to the programs that generate the welded-wire tapes or to programs that produce PC board layouts. Since the net list reflects the schematic diagram, it reduces the need for the point-by-point checking required for manually generated net lists.

Welded-wire board design

The welded-wire system requires a key-pin list and a net list as inputs. The key-pin list specifies the component type and its placement on a standard matrix, and the net list indicates how the components are interconnected. The information that makes up the key-pin list has a one-to-one correspondence with the mechanical assembly drawing, just as the net list corresponds to the schematic diagram.

The component footprint is stored in the system data bank; thus it is only necessary to specify a physical code (p-code) which indicates the footprint and the key-pin location (usually pin 1); and the welded-wire programs then generate the drill pattern for all the pins required.

The key-pin list allows the specification of two additional fields to indicate the pin soldered to the ground and the pin soldered to the power planes, both of which cover the board. The planes are etched around the remaining package pins to provide isolation from power and ground.

The preparation of the key-pin list, associated assembly, and marking drawings are presently done manually. We are now looking at approaches to utilize our present equipment to automate this process and expect that, by the end of 1974, we will have a system that, given a schematic and a placement sketch, can produce the complete set of inputs required by the welded-wire system. Additional information on the welded-wire system, both the manufacturing and software aspects, was published in a paper by Eastwood and Baran (RCA Engineer, Feb/March 1974 issue.)

Printed circuit board design

PC boards are used at AED generally in the power supply and other analog signal-processing circuitry. At the present time, the artwork masters and assembly drawings are prepared manually, but we expect in the coming months to be using CAD techniques. The advantages we expect to obtain from CAD techniques are higher accuracy, better control of artwork to reflect process needs, the use of a standard placement to reduce start-up cost, and finally, easier checkout of final artwork (since it should be free of omissions and process violation errors). The adaptation to our needs of available RCA programs, such as DSGCAR and COMPAS, will be investigated.

We expect that much of the data capture work that we have done and are doing for the welded-wire boards will be directly applicable to PC boards, thus greatly reducing the time necessary to develop a working system.

Testing

Computer-controlled testing techniques have been in use at AED at all levels from circuit boards to entire spacecrafts. However, this discussion is limited to the board and black-box level.

The circuit boards are subjected to continuity and functional tests. In the case of welded-wire boards, a complete continuity/isolation test of all points on the boards is performed on a DIT-MCO 660B circuit continuity tester. This paper-tape-controlled tester ensures that the welded wiring is free of errors prior to the installation of components, greatly simplifying the task of functionally testing the board later. In the case of printed-circuit boards, the continuity test is performed manually on some of the more dense nets. The reason for the reduced amount of PC board testing is due to the greater confidence that can be placed in the printed board accuracy,

since it is manufactured using precise photolithographic techniques as opposed to the welded-wire board, which is manufactured in part on manually controlled equipment.

The functional test at the board and box level is mostly performed on a computer-controlled automatic test station. The input to the test station is ATLAS, a higher-level language that can specify test equipment, connection to the box under test, the parameter to be measured and its relative tolerance; and also can branch to different steps, depending on the results of a given test. The ATLAS program can be checked both on the test equipment or offline in the software development facility, which has the same computer and has been configured to interpret and syntax-check ATLAS programs. The use of this automated test equipment has not been devoid of problems, however. Both hardware and software difficulties have been encountered in the past, in addition to scheduling problems — the latter arising from the fact that only one machine exists and when a test is failed, there is no way to get off-line and troubleshoot the board or box under test on some other piece of test equipment. The availability of simple off-line testing facilities would make the use of the automated test equipment more appealing to schedule-conscious project engineers.

Hybrid circuit design

CAD techniques have been used for several years in the designs of hybrid circuit masks for the AED thin-film facility. At present, hybrid layouts are digitized using the ALACARTE program from SSTC. The artwork is checked on the *Applicon* to verify its accuracy. At this stage, the facilities of the Laboratories are used to produce the Gerber tape, the 10-times-actual-size Gerber output, and the final glass masks.

LSI design

AED has used LSI designs in several programs. Both custom and universal array chips have been employed depending on the application in question. Generally, AED has done the circuit design and Gated Universal Array (GUA) layout and used the Automatic Placement and Routing (APAR) system for custom chips, but the generation of the artwork masks has been left to the SSTC groups involved in the given technology.

Future plans

There are many areas in the design cycle that are not covered by the present CAD system and others that require improvements before AED will attain a complete CAD system to assist the design engineer in performing his task. The areas we will concentrate on are detailed below.

Welded-wire system

The generation of the net list at present requires manual intervention in the areas of power and ground distribution. Plans are to improve the system so that the net list program can access the key-pin list files, identify the connections to the power and ground planes, and automatically enter them into the net list. Other improvements are strictly of a software nature, to make the system more flexible, more easily changed, and such that only one area has to be changed and the new information will propagate through all the programs in the system.

PC boards

This area will be investigated in the near future to determine what programs are available within RCA and how they can be utilized in the designs at AED that are presently manufactured by PC techniques. In adapting the PC programs, it is desirable to make full use of the data capture techniques developed to satisfy the welded-wire system, since the same basic information, although in different form, is needed in both processes.

Placement algorithms

Both the welded-wire system and the available RCA programs for PC boards designs require manual specification of component location. This is desirable in some types of circuitry, but there are many cases where an automatic placement of components on a predetermined standard grid would aid in the design process, at least to produce the first approximation. This could then be refined as required by the design engineer. It is planned to explore this area to see if any real advantages can be obtained by making use of CAD techniques.

Test language generation

This paper has described, so far, how AED circuits are analyzed, built and tested by CAD techniques. Inherent in this is all the information to define a meaningful test for them. The analysis programs contain information about the input stimuli and expected worst-case responses; the welded wire or PC board designs pinpoint the physical location of the signals; it should then be possible to generate in ATLAS language, appropriate test programs that can exercise the boards to verify that they work and meet the expected design goals. This task is similar to the generation of *Autodraft* input code from the digitizer output. Determination of the feasibility of this approach will be investigated within the not too distant future.

RCA's CAD data base

Close liaison has been maintained with this effort; when it is operational, we will attempt to interface AED programs to the data base so that one single data capture will permit all the CAD programs to work. This is an area where close coordination and cooperation among various divisions of RCA can lead to a very powerful and complete Corporate CAD system — one that can run efficiently, smoothly, and be extremely useful in maintaining a competitive position in the industry.

Conclusion

Much progress has been made at AED since early in 1974 in CAD; we are indebted to other RCA Divisions for advice, assistance, and the use of their programs which have been developed over long periods of time.

We especially acknoledge the assistance of J. Bauer and his group from M&SR for *Autodraft* and related *Applicon* programs, and of L. French and his group from SSTC for the artwork generation and related *Applicon* programs. AED expects to continue cooperation with them and is ready to assist other Divisions interested in mechanizing data capture of CAD data.

CAD expectations of an engineering graduate

C. Strasberg

A recent graduate recounts his views on a year of CAD work at RCA and the college training that prepared him for it. He begins with an assessment of computer science in engineering schools.

AS WITH MOST engineering feats and scientific knowledge, computer science in college appears to lag developments in industry. Today, the computer field has expanded so rapidly that most engineering schools have already set up separate and extensive departments for computer science where thorough treatments of programming languages and information storage and retrieval are available. Extensive computer facilities also are available to the student—commonly a System 360 for batch processing, keypunch machines, and often a minicomputer for control in real-time laboratory experiments.

Engineering schools, in general, have realized the significant amount of aid computers have to offer to the engineer in industry. In many schools, engineering students get much of their knowledge of computers from a required course in a higher level language, such as FORTRAN. The ability of solving both computational problems and non-numerical ones on a computer is cultivated. From this initial exposure to programming, the student obtains a basic idea of the type of problems a computer can and cannot solve. The mystery of how computers compute is unveiled by an understanding that numbers are represented in binary form which can be physically shown by electronic on-and-off switches. The computer is revealed simply as a machine which must be informed of every step in the implementation of a solution; and the method of solution must be specified by the human.

An engineering student may directly apply simulation programming for circuit analysis in one of his courses. A simulation program used in school, called PCAP (Princeton Circuit Analysis Program), is similar in principle to RCAP (RCA Circuit Analysis Program) in use at RCA. The program is simple to learn and is typical of the different simulation programs used in industry.

However, as is often the case with most engineering concepts, design and analysis techniques, and problem-solving abilities developed in school — learning to use a simulation program is merely an added skill that is educationally satisfying in itself. There is little realization of the extent and occasion for its usage in industry, thus producing an application gap. The available elective courses on simulation are not adequate for bridging this application gap, since they treat simulation as a separate entity and not in the problem-solving context that the student will be faced with in industry. I feel that the needs of students and industry could be best met through the expansion of existing engineering courses to include computer simulation as an alternate method in solving design and analysis problems. In this way, the student's ability to use simulation programs will improve as he progresses in his courses solving problems in dc, ac, transient analysis, and problems in linear and nonlinear circuits. The importance of these programs will become more apparent to him with such an expanded use over an extended period of time.

Academic anticipation

My personal background and interest in computers became rooted in high school. Enjoying a strong predilection for mathematics, I was increasingly curious to explore machine computation. Simple tutorial books on computers and programming have satisfied some of my curiosity. My decision to embark on an electrical engineering program in college could be attributed to an interest in applying mathematics to physical problems, and a hope of learning computer design, and not just a desire to be an electronic hobbyist. In fact, when it comes to wiring up hardware, I have two left hands.

My first college course with computers was in FORTRAN programming. I was very much impressed by the logical nature of programming a computer. This aroused me to further delve into and understand the internal mechanism of computing itself. Subsequent elective courses in switching theory, logic design, and the formal design of a hypothetical minicomputer gave me the feeling (illusion perhaps) of competence and mastery in computer design. I had hoped to be designing a computer for a senior project, but as it turned out I was limited to using a PDP-8 computer in simulating an algorithm for overshoot suppression in signal transmission by delta-modulation.

At the time, computer simulation of circuits and the modeling of physical processes on a computer seemed to me to be only theoretically significant. I understood that the main use of computers was for commercial applications such as for bank records and for processing payroll checks. The extent of computer applications in scientific work seemed small. Computers, I thought, were used in industry mainly for monitoring and control. My expectations were that in industry computers would be readily available when needed. And the programming for these computers would be done by programmers. As far as the actual design of computers was concerned, I believed that building a computer entailed only the hardware design without any consideration for programming feasibility. Software seemed to me to be entirely independent of the actual hardware design.

Industrial reality

My ambition of being able to design a computer has been realized in the Applied Computer Systems Laboratory of Advanced Technology Laboratories in the design of SUMC/CVT, a CMOS/SOS LSI multiprocessor system.

Between my knowledge of high-level programming and logic design, I discovered something of a gap. In addition to system architecture and microprogramming that are understandably pertinent to computer logic design, such software-related items as operating systems, assemblers, and compilers do affect the philosophy of design and need more than casual attention.

Contrary to previous impressions, the number of simulation and application programs used in industry is enormous. Simulations are done on all levels of design. In building complex systems, simulation is essential for verification of

design; otherwise, some costly mistakes could be made. With the advent of LSI circuits, design would be chaotic without standard procedures for simulation. Computer-aided design offers orderliness, control and much greater speed.

A prime example of how computers and application programs aid can be seen in the design of a computer. In the selection of the technology for the machine — TTL, CMOS, or SOS — standard cells such as NAND, NOR, or EXCLUSIVE OR must be characterized. Information of the time delay through the gate versus load must be obtained; the longest path through such gates determines the speed of the machine. FETSIM and RCAP programs model these gates and simulate the response time versus load.

The machine adder unit can be built on a single LSI chip, which may consist of about 400 logic gates. One mistake in the logic could make the chip useless. With the high cost of processing chips, chances for such a mistake must be minimized by verifying the logic by computer simulation. LOGSIM both verifies the logic and calculates the logical delays.

Once the logic of a chip has been designed, it has to be in turn converted to the actual layout design of the chip. The PR2D program specifies the location of each cell on the chip and the wires interconnecting the cells. The layout of each cell is modeled on the computer so that the artwork for the entire chip is specified and generated by the computer.

In a microprogrammed computer, all the microinstructions that specify the algorithms for implementing various machine instructions and internal housekeeping are stored in a read-only memory (ROM). ALSIM and MICROSIM programs exercise algorithms on a model of the computer hardware in order to verify that the algorithms are correct and that the separate functional units in the computer together implement the instrutions correctly.

In general, we try to simulate every step of the design process using various computer models: the cell definitions, the logic design, the artwork for chip fabrication, and the microprogramming.

Everything's great but —

Actual computer simulation, although sounding interesting, is usually the most uninteresting task for the engineer. Simulation normally requires detailed specifications of models. In LOGSIM, the specification requires a long, routine listing of all the elements in the nets and interconnectivities between elements. Even more detailed information about each element is required in calculating the total output capacitance on each element. The computer data printouts for LOGSIM are "painful" to read; they consist of lengthy arrays of one's and zero's. Perhaps an additional shorter table that specifies the output only when there is a generator change can serve as a simpler immediate check of the results.

It would be beneficial to the engineer to have an aide to do much of the routine work required to model a circuit for simulation. The engineer would then be freed to use this time for planning and design.

Application programs should be made as efficient as possible—requiring the simplest form for the user to model his circuit. This simplification will eliminate much work and reduce the possibility of error in the model. In the LOGSIM program, the calculation of total output capacitance on each gate could have been easily done by the computer. A program recently developed, named KADIN-1, that will serve as a data-base for LOGSIM and PR2D programs, eliminates the need for the calculation of capacitances. This data-base program is simple to use and requires one common model for both LOGSIM and PR2D. A similar program could be developed for LOGSIM and the wire-list program to test the logical connections for chip-to-chip on a hybrid and the input-output functions of the hybrid itself. Certainly, any additional programs which help verify an engineer's design or automate his design will contribute to the faster development of more complex systems with a design less prone to error.

I have found numerous application programs readily available at the ATL Computation Center. These highly valued programs have been written in-house to suit specific applications.

The computer facilities at RCA are adequate for processing programs, yet a faster turnaround time would certainly be welcome. The batch processing turnaround time of 2 or 3 hours is a long time to wait when debugging or experimentally adjusting program parameters. The timesharing terminals available in some locations of RCA are slow in response and often overloaded.

Conclusion

As a new engineer, in reflecting upon my engineering studies, I was impressed with the power and logic of programming and was so led to examine the computing mechanism itself. I believe that the direct impact of simulation as a design aid is not adequately felt in school, and present courses should be expanded to teach simulation in its proper context. Since joining RCA, I have realized my ambition to participate in the logic design of a computer — an LSI multiprocessor system. As a designer as well as a user of computers, I have noted both good and bad points in computer-aided design at RCA. It is good that so much power for design verification is available in simulation and application programs. It is bad that so much dog-work (subject to inadvertent error) goes into input-output. On a hopeful note, I observe that some attention is being given to relieving this input-output burden. Also, time-sharing response is getting better and is an avenue of escape from the restrictions of batch processing turnaround time.

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Chaim Strasberg, Associate Member, Engineering Staff, Advanced Technology Laboratories, Government and Commercial Systems, Camden, N.J., received the BSEE from City College of New York in 1973. He is pursuing the MS in Computer and Information Sciences at the University of Pennsylvania. Mr. Strasberg joined the RCA Engineering Rotational Program upon graduation and has now accepted permanent assignment with ATL. He is currently involved in design of the central processing unit for the NASA space ultrareliable modular computer for concept verification and test (SUMC-CVT), a CMOS/SOS multiprogramming computer. Mr. Strasberg is a member of Tau Beta Pi and Eta Kappa Nu.

The RCA "SelectaVision" VideoDisc System —a status report

Editor's note: This status report on the SelectaVision VideoDisc System was prepared to provide general descriptive information for worldwide use by International Licensing. Although several technical papers on SelectaVision are planned for future issues of the *RCA Engineer*, this report serves as an early introduction; it is published in this issue because of its timeliness and because of the obvious interest in the subject by the technical staff.

THE RCA "SelectaVision" VideoDisc is a prerecorded video storage and playback system suitable for the home environment. To be suitable for the consumer market, the VideoDisc system was designed to be reliable, easy to operate, provide a high quality color picture on a standard color tv receiver, have a wide selection of program material, and be low in cost.

Three key design decisions led to the simplicity and low cost of the system:

1) The use of a grooved disc to permit the disc itself to provide positive tracking of a stylus along the signal path by purely mechanical means, eliminating the need for any expensive servo loops.

2) The use of capacitance pickup from a metallic electrode deposited on the stylus to retrieve the signal. The advantage here is that the stylus is easy and inexpensive to fabricate in comparison to any other technique for retrieving recorded signals from the disc. (The capacitance pickup is capable of resolving signal elements smaller than the wavelength of visible light, permitting high-density recording using the RCA-developed electron-beam recording technique).

3) The choice of a lower rotational speed of 450 r/min. Important advantages are: Effects of vibration due to unbalance of the disc or rotating parts of the player are significantly reduced. Errors in signal timing that might result from warp or eccentricities of the disc occur at a frequency that is easier to compensate for in the television receiver. More importantly, a simple and inexpensive electromechanical device, the "arm stretcher," can be used at this lower rotational speed to reduce time-base errors, thereby permitting playback into receivers with the relatively slow horizontal synchronizing circuits typical of most U.S. and European made receivers, without requiring modification of those receivers. A disadvantage is that there are four tv frames recorded during each revolution of the disc, making it less suitable for stop-action and slow-motion effects.

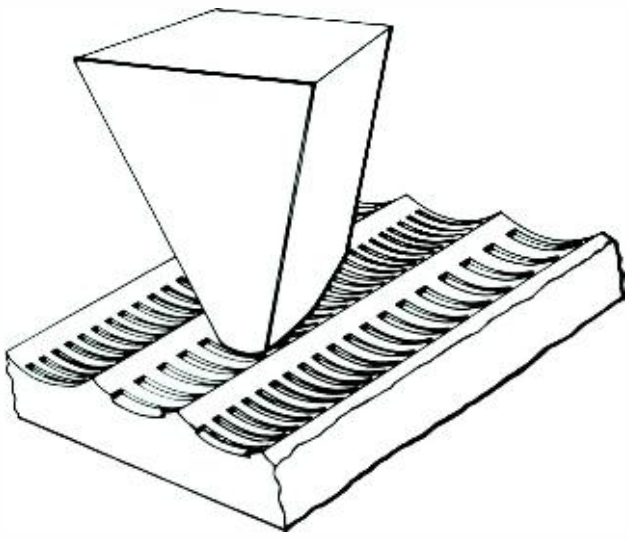


Fig. 1 — Stylus tip and VideoDisc surface.

With the exception of the stylus, the RCA VideoDisc player is fabricated almost completely from conventional components that have been in production for many years in consumer products.

Each disc is capable of reproducing a full hour of recorded program, 30 minutes on each side. Virtually any feature-length movie can be sold in this form as a two-disc album. The disc itself is familiar in form. It is a 12-inch disc composed of vinyl copolymer materials of the type used in an audio disc. The metallic and dielectric coatings necessary for playback by means of a capacitance pickup give the disc a distinctive shiny appearance and can be inexpensively applied in an automatic continuous process.

The discs have routinely exhibited playing life in excess of 500 plays before visible signal degradation. The life of the sapphire stylus is expected to be 300 to 500 hours of playing time. The stylus and stylus arm are housed in an inexpensive cartridge, easily replaceable by the user in the home.

Information on the disc

The disc has a spiral groove of roughly circular cross section with a pitch of 5555 grooves/inch. The information is recorded as transverse slots of varying width and separation recorded into the bottom of the otherwise smooth groove and is read out by a stylus which rides in the groove and detects the passage of the relief pattern under it as the disc turns. Fig. 1 shows a model of the record surface and the tip of the stylus riding in the groove. In playback, the disc turns at a constant speed of 450 r/min. Luminance, chrominance, and audio signals are encoded in the zero crossings of the relief pattern pressed into the disc.

As will be described in more detail later, an electron beam is used to record the signal slots. The stylus is composed of a main body of sapphire shaped to fit the groove and a thin metal electrode perpendicular to the groove. As shown in Fig. 2, the stylus detects the relief pattern in the record by changes in capacitance between the tip of the electrode and the metallic coating on the record surface.

To conserve bandwidth, the chrominance signal is combined with the luminance signal in a system which we call *buried subcarrier color encoding*. To a large extent, a television video signal repeats at horizontal line rate and thus has an energy spectrum with peaks at multiples of line frequency. Such a signal can be passed through a comb filter with peaks at multiples of line frequency with little degradation. The luminance signal is passed through such a comb filter as indicated in Fig. 3. This leaves nulls in the energy spectrum, at odd multiples of half line frequency, into which the chrominance is encoded. One of the nulls (1.53 MHz) is chosen for the suppressed subcarrier frequency for quadrature modulation by *R-Y* and *B-Y* chrominance signals. Since these signals also repeat at line frequency, the resulting sidebands occur at multiples of line frequency away from the carrier and thus also fall on the nulls of the luminance comb filter. The modulated chrominance signal is passed through a comb filter with transmission peaks at odd multiples of half line frequency, which are interspersed between the peaks of the luminance filter. The comb filter luminance and chrominance signals are added together to provide a composite video signal with a total bandwidth of 3 MHz which is recorded on the disc as an fm signal, peak whites recorded as 6.3 MHz, black as 5.0 MHz, and sync tips as 4.3 MHz as indicated in Fig. 4. On playback, after suitable demodulation, the chrominance and luminance are separated by appropriate comb filters and then recombined into a standard NTSC color signal.

The audio is included in the recorded signal by duty-cycle modulation of the composite video fm signal. Without the

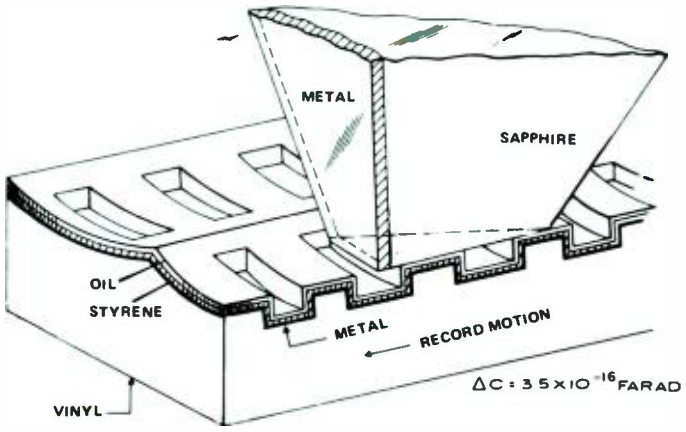


Fig. 2 — Stylus tip and VideoDisc surface cutaway view.

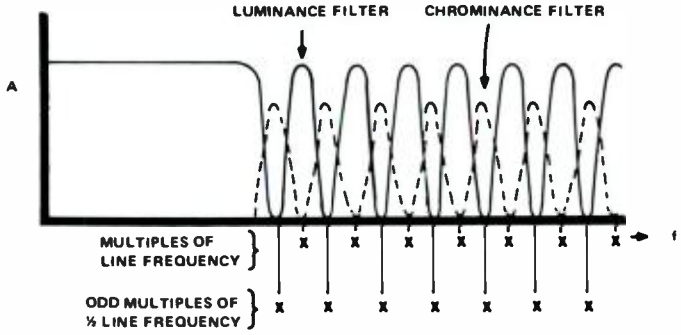


Fig. 3 — Buried subcarrier comb filter.

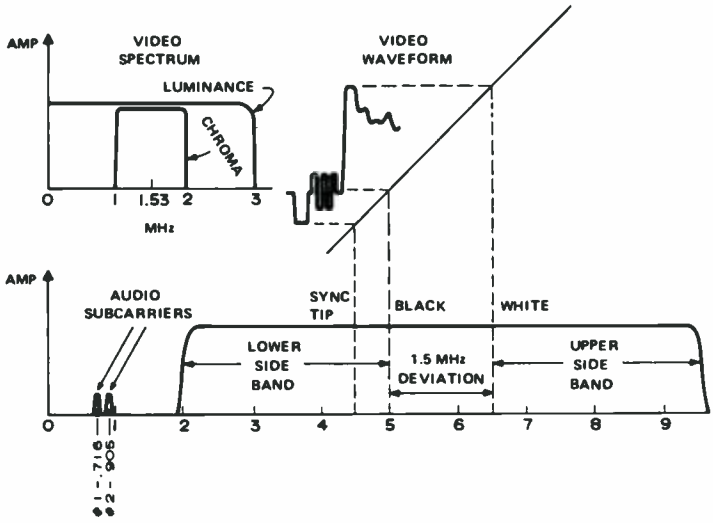


Fig. 4 — VideoDisc spectrum — MHz.

audio, the composite video fm signal has a duty cycle of 50%; *i.e.*, the lands are as wide as the slots. The audio is included by deliberately modifying the video fm signal so that the duty cycle is not 50%, *i.e.*, by making the lands periodically wider and narrower than the slots. This is accomplished by frequency modulating suitable carriers with the audio signals, adding the frequency-modulated sound carriers to the composite video fm signal and passing the sum signal through a limiter. The result is the duty-cycle-modulated composite video fm signal which is recorded on the VideoDisc.

With the parameters that have been chosen for the RCA VideoDisc (450 r/min, signals as high as 6.3 MHz, and an inner groove radius of 3.28 in.), the shortest recorded wavelength is about 0.6 μm. When duty-cycle modulation is added, the narrowest recorded slots are about 0.25 μm. It has been found convenient to record slots of this width by means of a finely focused beam of electrons impinging upon electron-beam sensitive material (similar in many respects to the more conventional photoresists).

The disc master upon which recording is done is made by mechanically cutting trapezoidal cross-section grooves in a copper-coated aluminum disc, applying electro-beam-sensitive material in dilute solution to this disc, and letting the sensivitve material sag into the grooves as the solvents evaporate as shown in Fig. 5. The net result is a disc coated with electron-beam-sensitive material with the desired spiral groove pattern in its surface.

The coated disc is mounted on a turntable in a vacuum in an electron-beam disc recorder so that it can both rotate and translate under a modified scanning electron microscope column, as shown in Fig. 6. The electron microscope gun and lenses provide a finely focused beam of electrons at the surface of the master disc. Both deflected pencil beams and undeflected fan shaped beams have been used for this purpose. In either case, the beam is turned *on* and *off* to provide the exposure required. Positive-acting sensitive materials are used, which is to say that those portions of the material which are struck by the electron beam can be removed by subsequent development.

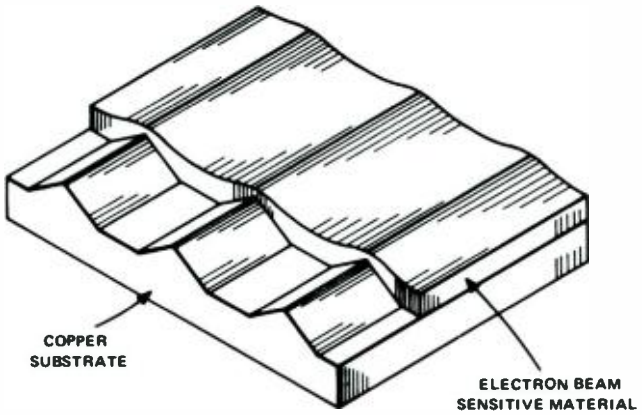


Fig. 5 — VideoDisc groove formation.

Rotation of the turntable is achieved by directing a jet of oil at its periphery and causing it to turn as a turbine. Speed of rotation is measured by an optically interrogated tachometer disc. Speed is controlled by supplying more or less oil to the turbine drive.

As the turntable rotates, it is also translated by a lead screw so that the electron beam remains centered on the pre-cut grooves of the master disc. The position of the groove relative to the electron beam is determined by electrons back scattered from the groove walls and collected by suitable groove tracking sensors. An unbalanced condition in the groove tracking sensors causes corrective signals to be applied to beam-deflection circuits and the lead screw drive.

Limitations imposed on the recording system by less-than-desired beam energy and less-than-desired resist sensitivity have dictated that recordings be done at rates which are less than real time. Most RCA records, to date, have been recorded at 20× below real time, several have been recorded at 5× below real time, and a few have recently been recorded at real time. The increase in recording speed has been achieved mostly by modifications in the electron-beam source and its utilization so that more energy is available for exposure. Currently, the Laboratories is refining the real-time exposure capability so that recording will be done at real-time speed at time of product introduction.

After exposure and development, the master disc has the relief pattern which is desired in the final records (Fig. 1). Metal parts are made for stamping records by the same methods as used for audio records. Electroless plating of the recorded master plus further buildup by

electroplating produces a negative metal master. This is replicated by electroplating to provide a positive copy (variously called a mold or a mother). The mold is replicated by electroplating to provide a stamper which is used to press records. While fanout numbers are not yet fully established, it is estimated that one recorded master will produce 10 stampers, and each stamper will produce 1250 records. Thus, each recording operation may result in 125,000 records.

The final step in the manufacture of the records is the application of metal (by vacuum sputtering), styrene (by glow discharge), and oil (by an evaporation process). The metal and styrene enhance the electrical capacitance variations experienced by the stylus-record interface, and the oil provides lubrication to increase both record and stylus life.

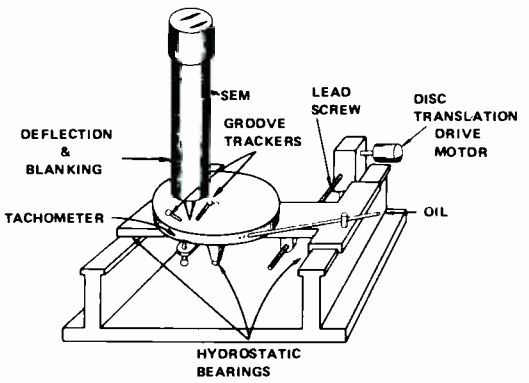


Fig. 6 — Electron-beam disc recorder.

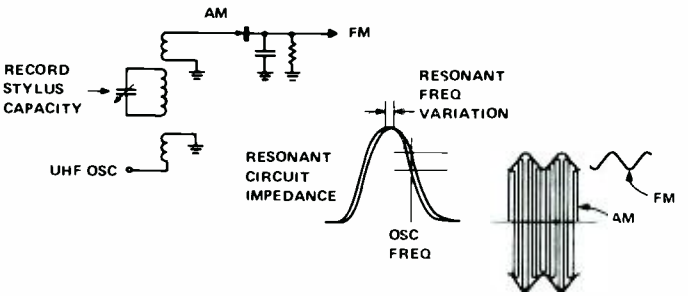


Fig. 7 — Capacitance-stylus playback circuit.

Playback of recorded information

The recorded information is played back by means of a stylus, riding in the groove, which experiences a change in capacitance as the relief pattern of the record passes under the tip of the stylus. The stylus-record capacitance is made part of a resonant circuit (at about 915 MHz), the tuning of which is varied by the stylus-record capacitance variations as indicated in Fig. 7. When driven by an oscillator of suitable frequency (on the skirt of the resonant curve), the variable frequency resonant circuit will provide a variable impedance and thus a variable amplitude of the oscillator signal as it passes through the resonant circuit. The amplitude modulation is stripped by a diode detector to provide a signal which rises and falls with the passage of the slots in the record under the stylus. This fm signal is demodulated to provide the composite video signal mentioned earlier. The audio signals are recovered by appropriate filtering followed by fm detectors.

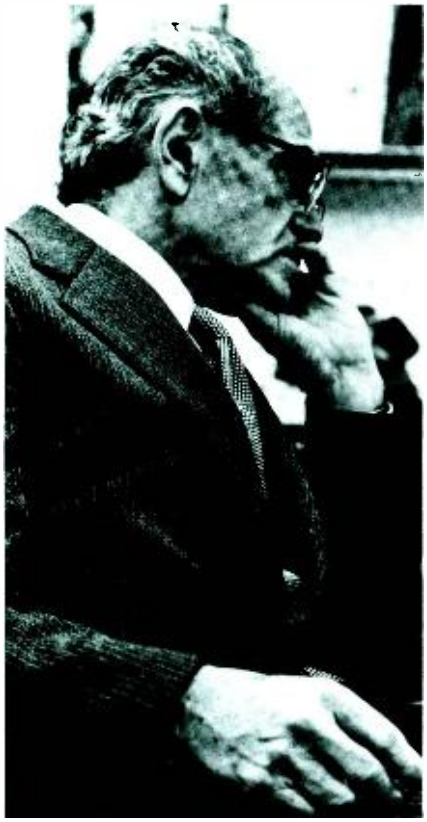
Average speed control of the playback turntable is achieved by driving with a synchronous motor locked to the power line. Small perturbations in playback speed, due to synchronous motor hunting, record off-centering, *etc.* are corrected by an arm stretcher. This unit consists of a small electromechanical transducer (similar to a moving-coil loudspeaker element) which drives the stylus arm back and forth along its long dimension, parallel to the record groove. If the record tends to run too slowly, the stylus is pulled toward the transducer to increase the relative speed between stylus and record; and if the record runs too fast, the stylus is pushed away from the transducer to reduce the relative speed. Error signals to control the arm stretcher are derived from measurements of the color-burst frequency as the record is played.

Defect compensation is provided by a 1-H delay line, appropriate sensing circuitry, and video switches to substitute the video from a previous line whenever defects occur on the present line.

System parameters

A summary of the pertinent parameters of the RCA VideoDisc system follows:

Record diameter	12 in.
Record thickness	0.07 in. (at center and outside rim)
Rotation rate	450 r/min.
Center-hole diameter	1.5 in.
Recorded band	2.44 in. wide (5.72 to 3.28 in. radius)
Play time	60 min. (30 min. each side)
Recorder fm signal	4.3 to 6.3 MHz
Luminance bandwidth	3.0 MHz
Chrominance bandwidth	0.5 MHz
Video signal-to-noise ratio	>40 dB
Audio carriers	716 and 905 kHz
Audio bandwidth	15 kHz
Audio-signal frequency deviation	±50kHz
Audio-signal-to-noise ratio	60 dB(approx.)



A versatile, determined approach to innovative engineering — an interview with W. Rex Isom

This interview pictures Warren Rex Isom, Chief Engineer of RCA Records, a man whose career follows a seemingly paradoxical path. Why would a man plan a career as a college professor and turn into a Chief Engineer? Who would study political science before becoming one of RCA's finest engineers? How could Rex excel in applied research and advanced development — and then turn abruptly into record manufacturing processes involving esoteric chemical mixtures and machinery? Or you might ask — how could Rex always maintain his drive at a high pitch pursuing such a wide range of contrasting projects? Perhaps the answer is that Rex possesses the versatility and the determination of an Indiana Farmer (which he is) and demonstrates this in successfully answering every challenge presented to him. Though not apparent in his easy manner, successes have been achieved — on the job and after-hours — through painstaking consultations with associates...and by studying the various branches of knowledge required to solve problems.

THIS INTERVIEW with Warren Rex Isom was conducted by W.O. Hadlock, Editor, *RCA Engineer* and F.J. Strobl, Editor, *RCA TREND*. Mr. Isom holds degrees from Butler University, The George Washington University, and Harvard University. Mr. Isom was on the faculty of LaSalle College, Butler, and Harvard. He joined the engineering department of RCA in 1944 and became Chief Engineer of RCA Records in 1966. His professional career has encompassed the field of recording by work on wire, film, magnetic, kinescope, satellite, and disc recording. He holds twenty United States Patents in the field.

Mr. Isom is a Governor of the Audio Engineering Society and is Chairman of its Committee on Standards and Vice-Chairman of the Admissions Committee. He is Chairman of the engineering committee of the Recording Industry Association of America. Mr. Isom is a member of the United States National Committee of the International Electrotechnical Commission and is its Technical Advisor on sound recording matters. With the American National Standards Institute he is the Chairman of the committee on Sound & Acoustics (S-4) and a member of the Acoustical Technical Advisory Board. In the Electronics Industries Association, he is Chairman of the S-4 Standards Committee and a member of the International Standards Committee. He is a member of the Standards Council of the Institute of Electrical & Electronic Engineers and past Chairman and a Director of its Central Indiana Section. Mr. Isom heads the Audio Executive Technical Committee of the International Tape Association and is a member of the National Quadraphonic Radio Committee, Panel 6. Mr. Isom is a member of Phi Kappa Phi and is a fellow of the IEEE, the Audio Engineering Society, and the Society of Motion Picture and Television Engineers. He has been named by the Engineers Joint Council as an Engineer of Distinction.

The Editors share with the readers this discussion concerning Rex's years of experience at RCA in the hope that the interview gives some insight into Rex's rise from a young political scientist to the post of Chief Engineer and Technical Advisor. Rex seems to know how and where (some call it serendipity) to find the exact nugget of intelligence in each associate needed to carry a project to a successful conclusion. In his approach to people, the Editors find it to be much like that of Will Rogers...Rex Isom "never met a man he didn't like."

Early engineering at RCA

Rex, you have been Chief Engineer of RCA Records since 1966. *How was your career guided toward this position?*

Actually, my initial formal technical training was rather brief. It consisted of one semester of a high-school course in physics. I originally had the idea of being a college professor of government, and when the war came in 1939, I all but had my PhD from Harvard. Then, I got the number-one draft number in the draw of 1939. And that ended things for a while.

So, when I went to RCA in 1944 to be interviewed by Dr. Edward Kellogg and Max Batsel, Chief Engineer, I had to tell them that I really didn't know too much about technical affairs. But, I felt that there was a great similarity between technical and governmental affairs. They asked me what I meant, and I said it was really very simple: There are three-way relationships in government. More or less, power in a democracy lies in public opinion, or the people themselves, and the Legislature directs the power and the Executive uses it — and that's a three-way relationship. Or, again, there's the legislative, executive, and judicial branches, each related to the others. It is the same way in technical affairs. In mechanics, we have *force equals mass times acceleration.* In electricity *E equals IR.* In optics it is something else, etc.

They are all three-way relationships, and the derivatives of all these relationships, first-order and second-order derivatives, are exactly the same — just different notations.

In government we call it checks and balances and separation of powers. In scientific affairs we call it sensors, servos, and feedbacks. We have oscillations in such systems, and we have oscillations in government too. In both, delaying actions (damping) curtail the excursions. After I had talked this way for about five minutes, Dr. Kellogg looked over at Mr. Batsel and shook his head, and Mr. Batsel said "let's don't stop this conversation, but you're hired." In fact, I was hired as a Class A engineer.

This approach seemed unorthodox, yet was that the Batsel style ?

Yes, I view this as one sign of greatness in Batsel. For example, two or three days after I'd started working, he came around to see me and said "Look, I don't want you to try to be the best mechanical engineer, or the best electrical engineer; don't do that. If you need help from a mechanical engineer, ask for it. We've got lots of them. If you need help from an electrical engineer, or a mathematician, do the same thing. I want you to continue to observe things, such as you did in my office, rather than just do bench work."

What did he mean ?

Well, I think he wanted me to be more comprehensive in my work. Yet, I've done a lot of bench work. A lot of people don't see the forest for looking at the particular trees. If your responsibilities are specific, you'd better look at your tree. But, after being directed that way too long, you lose the ability to look at the forest. The other thing that impressed me was that I never was given an assignment (for the first ten years anyway). I always generated my own assignments. Of course, I got approval for them. But, nobody ever came to me and said "Do this or do that." To me, Max Batsel was great because he let this happen.

Then you were in a unique position in having such opportunities ?

I felt that I not only had the opportunity, but also the obligation to do that. And it was underscored in my particular case by the fact that Dr. Kellogg, to whom I reported, became suddenly ill, and was away from his desk for practically a year. So I looked around and decided to work on something that nobody seemed to be doing anything about; namely, a 16-millimeter projector. There was one in our place. I took it apart to see what I could do to make it better.

I started with the RCA-201, and with certain improvements it then became the RCA-400. I was responsible for that transition in development, not in design. I was able to get not only a great improvement in sound but also a great increase in the light output. We had the best machine in the industry for a number of years, and sold on the average of 20,000 per year from about 1946 to about 1965.

Next, a need arose for a television projector so that 16-millimeter movies could be used as a source of television programs. It was an opportunity for me; others had tried to do it without a satisfactory solution. My basic solution was to introduce the idea of elliptical gears. Elliptical gears, of course, have been known for ages, but it was a new technique in manufacturing at RCA. Everybody thought they were difficult to manufacture. I showed how they could be manufactured, and so they were used.

What came next ?

The next step after projector work was kinescope recording...recording television pictures on film, and then rerunning the film over tv at a later time—much the same function that is now being done by video tape. I developed the first cameras to do that. In fact, when I first came to Camden, to show what could be done on kinescope recording, I photographed (with three movie cameras) the Paul Whiteman.tv show over in a studio in Philadelphia. We then spliced the film together for showing on tv.

What do you consider your most satisfying project ?

The thing I probably got the most satisfaction out of was putting together the concept of the ideographic composing machine. This is one of the very best examples of the work other people did with me and for me, and I'd like to regard it as *with* me. At the beginning of the Vietnam War, the U.S. needed a system by which we could communicate with the Chinese people generally—and this was through ideographs. IBM and CBS had been working on a mechanical monstrosity for years and spending a lot of money and not getting too far. I went up to Massachusetts and discussed with the Army Quartermaster Corps what was needed. I came to the conclusion that we had all the elements and just needed to put them together. We had computers, we had television, we had an optical tunnel, and we had memory drums. Most of all, we had people who knew and who could do. So I conceived a way to put them together. Harold Haynes and Fred Shashoua and I made a mock-up of the equipment with the help of Tony Lind's department.

We demonstrated the performance we

...heritage affects my thinking a great deal. The great heritage of RCA is customer confidence.

could obtain; we wrote a twelve-page proposal; we showed pictures of what we could do and guaranteed that our result would be better than that which they regarded as good; we asked for $750,000; and three days later we got the contract. We guaranteed that we would have an operating unit is less than 18 months. Our competition was saying "three years" and instead of $750,000 they were saying a couple of million dollars for a whole van of equipment. Fred Shashoua, the project leader, worked it out to be a wonderful thing. It was demonstrated for President Kennedy, who gave a presidental commendation to the Quartermaster Corps' project manager.

What was your most exciting technical challenge ?

I guess the greatest technical honor that was ever paid me was a visit by Dr. Valdimir Zworykyn, the Director of the Laboratories, Dr. George Brown, Glen Dimmick, Elmer Trouant, and Merrill Trainer. That was in the days when we were trying to get approval for compatible color tv. They came in unannounced to my little laboratory and asked me to build a projector for use with color television...to derive a color video signal from 16-mm color film. This was in July, 1954, and we had to be on the air before the end of the year to get approval. They wanted me to devote 100% of my effort to the assignment and offered me the full weight of RCA's resources.

Dimmick, my boss, said, "Will you accept the assignment?" I replied, "Yes." Then Dr. Zworykyn said, "Will you explain to us how you are going to do it?" I said "I can't because I don't know just now how it will be done, but I will stop everything else and think about it, and when I get a plan, I will let you know." That was on Tuesday; I was numb on Wednesday. Thursday, I had to go up to NBC in New York to attend to some prior business.

On the train up to New York, I conceived an approach to the problem. And on the way back, I wrote up the plan. The next morning I dictated it and, at a meeting Friday afternoon, presented my ideas. They approved. Because of the good support I had, we went to an operating engineering model directly without a hitch. On Christmas Eve, the first coast-to-coast network show of color television from film was from that projector. It was Jack Webb's "Little Lord Jesus." I watched the show and heard the claw advance every frame of film during that thirty minutes. Talk about sweating it out! I have seen the show on Christmas Eve ever since and each time I have the same cold chills running up my back as I had the first time it was shown.

You have numerous patents. Do you have a favorite ?

Out of around 20 or 22 patents, I consider some more important for one reason or another. But there are people who have really great and important patents, and I'm not really one of them. I got five or six patents on the color television projector that were important at the time, but the art has moved away from them. The vidicon tube more or less obsoleted everything I did. We had to do it the hard way, but the vidicon tube made many of these problems much, much easier, not only for film but for everything else. Progress often does that.

The most important, recent thing I did moneywise, is to invent the plastic pressure roller used in the Stereo-8 cartridge. So far, we have used maybe 100 million of these rollers and at the rate of 30 million a year. Before the invention, we were paying about 8 cents apiece for them; now they cost less than 1 cent. Multiply that out and it's a big saving. Best of all, it justifies my lathe in the basement—so I tell my wife.

The value of personal contact

Let us change the subject and ask you about the atmosphere at RCA in early days ?

I felt from the very beginning that I had all of the heritage of RCA behind me simply because I worked for Dr. Kellogg, the inventor of the loudspeaker we know today. Also because of our position in advanced development, we had contact with people who had made RCA... people like Merrill Trainer, Ted Smith, Art Malcarney, Wally Poch, Larry Sachtleben, H.E. Roys, Art Vance, Ray Kell, Hank Kozanowski, Art Curtis, Elmer Engstrom, George Brown, Harry Olson, many many others and Mr. Sarnoff himself. We saw them everyday. We didn't bow on the street when we met them because they were part of the team.

But this business of heritage affects my thinking a great deal. The great heritage of RCA is customer confidence. This means, we have to maintain allegiance to our customers—whether it be commercial or government. We owe our customers our best efforts. If we lose that emphasis, we've lost something important. Then it becomes a smart operation based on alertness and wit rather than a basic operation of substance. Of course we need both, especially both. The very best we can do, under the restraints we have to live with, is hardly good enough.

Now that the company is larger, do you think that contact made at the Chief Engineers' meetings keeps alive the atmosphere of unity in RCA ?

Yes, the thing that I think is important about these meetings is that they are well-established and well-recognized as being essential. They should be repeated within each of the divisions. All the engineers in a division should get together for two or three days a year in an appropriate place and go through the same exercise of principally concentrating on their business affairs. Also, Corporate leaders and experts should be featured at these general meetings.

For example, three or four months after I came with RCA, I got a letter from the head of our division which stated: "We have invited some of our key personnel to attend a dinner to review our status in the competitive arena in which we do business." I remember what an impact that had on me. This told me that I was in on it. It made me know I was part of the organization.

How about the value of 'bull sessions' with associates in advancing your work ?

A lot of discussions with associates have been valuable—lunchtime discussions, carpool discussions, and discussions within the professional organizations. These keep the mind in turmoil and the cobwebs out of the corners. With Harry Woll, Harold Haynes, Murlan Corrington, Nels Crooks, and Paul Wright in our carpool, every aspect of engineering and other things that came to our attention were worked over.

This is particularly true of IEEE and AES and the other professional groups of our

industry. Through professional shoptalking you find that the man on the outside has a different slant, both technically and managerially. Engineering is not a "loner" profession. You've got to pull all the available resources together to go forward. In this way, it's a very interesting and very enjoyable humanistic profession.

The value of communications

Do you think group problem-solving meetings are beneficial?

Yes, I think these are very, very important. But, they are important in my mind in a way other than is usually meant. You have a problem-solving meeting, not necessarily to get the problem solved, but to find out what the problem is. *You can't solve any problem without knowing what it is.*

Invariably, in such meetings somebody acts as a catalyst and puts things together. He may not necessarily contribute anything directly, but one sign of a really great leader is for things to happen in his presence.

Defining the problem is one element. How about the time element?

You let a person know the important aspects of the problem — what it is, and when an answer is needed — so that someday he doesn't say, "Gee, I had no idea you wanted this so soon." Timeliness is often the most important aspect of the problem.

A lot of engineers lose patience with the fact that occasionally top management wants to look in and see what they're doing. Managers have a real need for doing this because they have to plan the future of the Corporation, and they have to be reassured that they are making the right investment. If it is right, all is well. But the sooner management finds out that the investment is wrong, the quicker they can redirect the effort into something that can be right.

Once I was trying to solve a television projector problem. We were redoing a new approach invented by Bell Laboratories and spending much money. Even with all the refinements, we came to the conclusion that it wouldn't solve the problem. So, we arranged a demonstration for General Sarnoff and topside to attend. I was asked, "What are you going to tell them?" "Well," I answered, "I am going to tell them that we have done everything we knew how to do but that this approach is wrong. It's almost good enough, but it's wrong. It won't really stand up."

I was told, "Are you sure you really want to do that, because you're opening yourself up to dismissal." At the demonstration, it was pointed out, "As you can see this is very promising, but this is about as far as it will go. This approach is wrong."

Almost immediately, General Sarnoff jumped up and said, "That's the kind of answer we need, a definite answer. Now we can redirect this effort and look for the real approach!" This attitude was certainly one of the elements of greatness in Sarnoff, but it also points up that topside needs to know the answers just as soon as they come available.

How did you handle the feeling of "encroachment by staff on the line operation? There always has been this problem in communications where one feels that the other is infringing on his territory.

You might say this question is for the birds, because the birds have this same kind of feeling. They stake out their territory, and they fight off encroachments. We have to understand the staff man, the factory man, and the research man, and each has to understand the others' role. If we understand each other, then we can communicate with each other. Find out what a man's function is, and we can help him to fulfill it. In other words, welcome him rather than ward him off. I think that you are perfectly willing to help and extend yourself for someone that you understand and know. I have never known an S.O.B. All the S.O.B.'s I've heard about are people that I have never known.

You are saying that we need more people who understand their roles?

The answer is "Yes." A relationship between two people is like an equation. You are one element of the equation in our relationship, and I'm another element. In engineering, there are many people and many elements in the equation. Some of these people are in applied research, some in pure research, some in factory engineering and some in just hard-nosed production. All of these must be related together to equal the final product. If the different roles of the different groups can be understood by each to be elements of the equation, they can operate together beautifully. This business of saying we pay a man to think, and then we lock him in a room, and he supposedly thinks without being distracted is nonsense. Nothing will come from that, or very little related to what we're doing.

Profits are sometimes frowned upon and a man thinks it is beneath his dignity to work for money. Actually money is a measure of our achievement, and we should regard it as such. I don't want to do anything in which nobody else has an interest. If they have an interest, they'll pay for it, and it has value. If no one is willing to pay for it, it has little or no value.

There is another key to good communications, isn't there? You seem to be mentioning many occasions where a practicing engineer was brought in touch with top people. That shows him the importance of a project.

Yes, that's a good way to let people know the importance of it. Also, a fact of the business of communication is to *never* assume that people know what they are supposed to know or to be doing. Tell them! And even tell them over again. They don't resent it. There is no harm in this. But if you assume that they know what they are supposed to be doing, and later find out they did not, that is an inexcusable disaster.

How can we maintain close and informal communications in a big company like RCA?

I think that the interdepartmental engineering conferences that we have, say, at the managerial level are wonderful. They give to the people who attend an idea of what the total business of the company is and how diverse it is and where the sources of information are and this sort of thing. I make great use of it, and other people call me and they make use of it. I think in each of our departments and divisions it would be well worth the investment to have a meeting of the total engineering force two or three days a year, once a year, or once in 18 months so people will get to know what they are doing. Somebody said..."Oh, we have staff meetings once a week or once a month," but a staff meeting is not the same thing. You're looking at the trees, or only at the roots of

the trees at a staff meeting, not at the total business. Get all the engineers together, and have the dignitaries there too for they represent overall Corporate interest and commitment. Now the engineers can find out what the total business is and the objectives and the interest of the projects they are working on.

But this must be added; as wonderful as these meetings are, they are only the beginning. The permanent and lasting value comes from man-to-man and engineer-to-engineer relationships.

From tape to records

When did you get in on records ?

From the very beginning, I had a casual concern about records, and I had people coming to me and asking what I would suggest, etc., because tape recording related closely to records. I guess the interest was kind of an osmosis proposition because I had such a close friendship with Ed Roys, whom you might say was the Father of the RCA Records Engineering Department.

You mentioned Ed Roys. What do you recall of him ?

The thing I remember about Ed Roys is that Ed knew every facet of the mechanical and electrical aspects of recording. But he didn't know it to the exclusion of the other things. He knew his territory, as the Music Man would say, and *more*. The *more* relates, among other things, to this depth of conception in human relations, and humans are the most important part of the details.

Was he a systems man ?

Yes! Truly yes! But you just have to know the details of your business and Ed did. I shudder when I hear a young fellow say, "I'm going into systems." If he gets into systems without knowing the actual working level basis of a system, he will get lost and the system will not relate to that function to be performed. This is important. A systems approach must be build on a solid technical and practical base.

When you became Chief Engineer of RCA Records, how did you take the change from tape to disc recording ?

The transition from magnetic recording to disc recording is not very great, because all the original recordings for music are made on magnetic tape anyway. The disc is just the final form the product takes. It takes a while to bring about changes, because the previous technology is so well-entrenched and cast in steel in the form of many presses and expensive tooling. To make a change takes a long time and lots of money. You can not make a change in the shape of a record (profile) in less than a year. To change all the molds for 200 presses and at the same time keep all the presses going is a progressive job, not an abrupt thing. But we have made, since I have been in the record division, an impressionable change in records. The records are thinner, taking maybe 30% less compound materials and this is important today. When you make a change like that, it takes a while to get the change stabilized. We are doing a good job with our Dynaflex record, and it has been copied throughout the industry. Its adoption was certainly a coincidental stroke of good fortune for all of us in the light of the current shortages.

Did you find any differences in your Chief Engineer responsibility from that of Manager in advanced development ?

Yes, there is a difference, because in a sense, records comprise a single product line. Of course we could say that we have in our inventory a selection of 3,000 products, but these are selections—not products. On the face of it you could say that it is a very narrow activity. But on the other hand, records involve mechanics, electronics, chemistry, plating, plastics, physics in general, and acoustics. On top of that, I include music appreciation, as well as the appreciation for the significant sounds of recorded music, *i.e.*, frequency, dynamic range, and noise. Thus, while it is a single operation, it is probably more complex than many multi-product lines.

Then record engineering brought you even closer to the product ?

Oh, yes, very, very much closer. Not only to the product, but to every aspect of the product. The creative aspect of record engineering is outside of engineering, that is, in the realm of the artist. So there you find yourself a servant to the artist by providing him with the equipment by which his contribution can be more readily revealed to others. In the recording studios, we constantly provide better recorders, better microphones, and better monitoring speakers to permit artists to hear exactly what they have on the tapes before record production is undertaken. Artistry is really the creative aspect. Engineering, of course, has nothing to do with the musical score, except to see to it that it is faithfully reproduced.

As Chief Engineer, what did you see as your role at that time ? What was the state of the business at that time ?

We had predominance in the classical and popular music markets. Of the Grammy awards that year, we got 26 out of 31, which was much more than all of the rest of the industry put together.

When I went to Indianapolis, I decided that the theme of my activity would be "engineering for profit." We increased the profitability of manufacturing of records and tapes tremendously. Of course, progress was inevitable no matter who was in charge.

We were just starting the Stereo-8 cartridge manufacturing, and we were paying for molded parts about $1.45. The cost is 15 cents now. I had my hand in a lot of it, but most of the work has been done by other people. I gave direction and sometimes had an idea, but the work was done by others. The same way with the new automatic record press which is being updated and improved.

Would you say that we are poised now for exploiting cost savings in record manufacturing ?

Oh yes. For record manufacturing, cost savings mainly relates to materials. We have reduced the quantity of material and reduced the cost of material and at the same time bettered the material. So we are in a good position to become number one in quality.

More than a year ago you wrote an article for the RCA Engineer on the CD-4 or discrete 4-channel system. Have you seen any changes since that time ?

Well, of course, I'm looking through biased eyes but I predicted that because of the pseudo nature of the matrix 4-channel record, people would tire of it. It seems to be happening. The first impression is that

I was helping people achieve their objectives, and this is a very pleasant thing to do.

The things I look for in a new engineer are personal initiative and confidence.

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First of all, an engineer must want to do engineering

pseudo 4-channel records are wonderful. But, the more you listen to matrix sound the more you hear the manipulation by electronics. That's not music. But with the discrete 4-channel system, we record and reproduce the entire acoustical environment. People appreciate it. It is real—not processed. There's no question in anybody's mind that discrete 4-channel is the way to go.

Engineering and supervision

When did you first get into supervision ?

Actually being titled as supervisor came about five or six years after I joined RCA. But I think I really got into supervision in 1946, in deciding whether I would stay with RCA or go back to teaching in college. My rationale for making the final decision was this: College teaching appealed to me because I was in a position to help people to achieve their objectives and their goals. But then it occurred to me that I could and was doing the same thing in RCA. I was helping people achieve their objectives, and this is a very pleasant thing to do. Also, the more you know about what a person is doing, the more of a satisfaction it is. One thing I found out is that you make a commonality between the goals of others and your goals. And the reason I find it easier to say I worked with so-and-so rather than say he worked for me, is that I don't consider people working for me.

How do you match the people to the jobs ?

My good luck with RCA has been the quality of people I had the good fortune to select and recruit. I recruited Fred Shashoua. I recruited John Rittenhouse, Marty Levine, Paul Wright, and helped recruit Don Parker and Don Kell, and many other great engineers; I had what I called a Vice President's Club. I called the people I worked with Vice Presidents because they were in charge of their jobs.

What do you look for in recruiting prospective employees ?

I look for achievement in candidates. I remember one man I interviewed. He is no longer with RCA, but head of mechanical engineering at a top college. I knew he had a PhD and I said, "You have a PhD, so what do you think that entitles you to do here at RCA?" He said, "Well, I think it really entitles me to begin to learn what engineering is all about." And, remembering what Batsel once said to me, I replied, "Well you're hired, but let's not stop the conversation at this point."

I interviewed Ray Warren and selected him because he was a man of great achievement, but in another field. He had become a first-class guitar player. He had toured the Far Eastern forces during the war, playing for the soldiers. He'd had his training in engineering (Georgia Tech). But Ray is a foremost example of my feeling that men who achieve in one line will achieve in another. And, it just worked exactly that way. Again, you look for achievement in the candidate. You don't pit his intelligence or knowledge against yours. You don't second guess his record of accomplishments.

From your experience in advanced development, what are your thoughts on how much advanced development should be done in a product division vs. how much can be done in research ?

This is an interesting question, but also an insolvable one. I have some ideas. I think that developments will come about by people who see the need for such developments or conceive the need. No matter what happens it will get done by such people regardless of where they work. They may have to do it in direct opposition to their own management. It takes a man with stature or stubborness. He has to go through the tight squeeze of either being respected or being fired. The opportunities for doing that are scarce. But it is easier for him to do it in an advanced development section than in a product section.

Advice to the new engineer

As a Senior Engineer, what is your message to an engineer entering the field today ?

The things I look for in a new engineer are personal initiative and confidence. So, new engineers, don't hide your talents. The fact that a man comes looking for a

If you have noteworthy aspirations, even if you cannot achieve them, you can at least leave for others a trail to achievement behind you.

job is a good recommendation. But as for the man who has been referred to me, I have some questions about him. First of all, an engineer must want to do engineering. He must have pride in his profession and pride in himself. That supplies the element of drive. If he has that, then he can recognize the significance of things. The one who says, "Oh, I'm doing engineering work here, and when this project is over, I'll get assigned to something else...." Well, we need those people too, but they are not the ones who get us where we want to be.

Isn't loyalty to a job and a profession looked upon, by some contemporaries, as being square ?

Yes, there are those who believe that their loyalty to their profession is a higher loyalty than to their job. They feel that if they are good engineers they don't have to worry about their jobs. Maybe they don't, but they are not making many jobs for others with that attitude. I've always considered a productive man's responsibility is not only to do his own job, but to create jobs for others and to keep those jobs going. You see how easy it is to get from that attitude to what we denote as company loyalty or as product loyalty.

Then pride in company, pride in product, pride in achievement—these are really compatible ?

That's right! Your company is in part, only an extension of yourself. RCA is composed of people. You can spell a company with a big letter or a small letter. Your company is not only a reflection of yourself, but an extension. You must have pride in yourself or pride in what you attempt to do. I have pride in my accomplishments, but much more pride in my aspirations. That is where you can have real pride. If you have noteworthy aspirations, even if you may not achieve them, you can at least leave for others a trail to achievement behind you.

How do you encourage bright young people in a company ?

One thing management has to do with genius-type people is let them know in the beginning that they are wanted and are accepted as a part of the organization. They ought to be told that, "I want you to know that I regard you as having it and capable of going all the way." Often managers are afraid to tell people things like that.

I found a unique way of doing that. This Indian Head penny tie-tac is part of the story. In ATL in Camden, many young engineers came into my organization. When they made the grade in a year or so, I recognized it by giving them the tie-tac. Often it was at a luncheon when they were leaving my group to follow a successful development of theirs on through the product stage. This tie-tac became an alumni badge for them and denoted that continued contributions to engineering were expected from them.

Why the Indian Head Penny tie-tac ?

I found early that there is a general residual interest in the American Indian. To exploit this interest, I have for years converted all tellable stories into Indian stories. Before I knew it, I became known as an Indian story teller! What better badge could there be for having been a part of my group than an Indian Head penny tie-tac.

How do you inspire confidence in your associates ?

Helping a man achieve is always important. The Sarnoff-Toscanini story concerning the clarinet player is a story in point. Toscanini hesitated a long time to take conductorship of the NBC orchestra because it had an undistinguished woodwind section. Attempts to recruit a clarinet player to strengthen it never found one that Toscanini would accept as good. Finally, Toscanini took the job anyway. And after the first rehearsal, General Sarnoff, as he told the story, wanted to stick around to hear what was going to be said. He feared for the clarinet player. Toscanini called the clarinet player and said, "In playing your clarinet, I would like for you to do this." And the player did as he was instructed. He became one of the world's greatest clarinet players because he got the help he needed. Toscanini helped him rather than condemned. That's exactly what we are talking about. We've got to help people achieve what they want to achieve. If you help them, you contribute to their confidence.

Rex, to windup our interview, consider this question. Suppose a high school senior came to you and asked you about entering the engineering profession: what would be your response ?

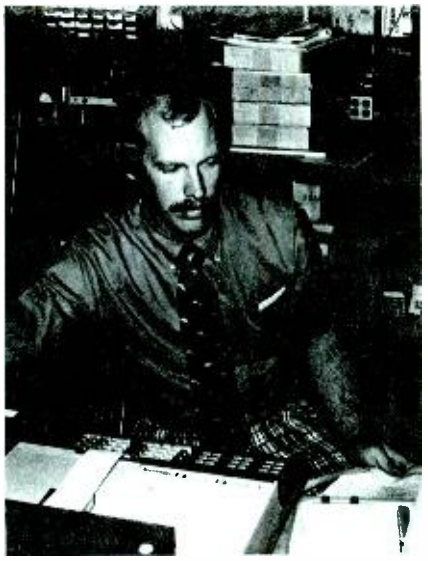
My advice to prospective college freshmen is to ask no one for advice. Accept the responsibility for making your own decisions and remember you are going to have to live with them. Get information, but don't ask anyone for advice, because that is your own thing. Now if a freshman should come to me and ask me "What do you think of my going into engineering?" I would reply, "It's the most wonderful thing to do, if you want to do it, but don't go into it because you think it's a good opportunity...Go into it if that is what you want to do." I used to be an advisor for college students. The students would come to me and ask me to help them make out their program for next year. And I said, "No! You go sit out there in the hall and make out your program; bring it in here to me, and I will go over it with you. You've got to make it out, because the responsibility has to be yours." If a man really wants to be an engineer, he can make engineering a wonderful career for himself, barring bad luck. But if he does it because he doesn't know what else to do, well, he's lost. He might later develop the interest in it. But that's like marrying the girl and hoping that you'll fall in love with her later.

But, one warning to all college freshmen: In these dynamic times, never be so sure of what you want to do that you concentrate on it to the exclusion of all other interests to the extent that you disqualify yourself from doing what you may later wish to do or may be required to do.

CAD program for rf amplifiers

D.F. Medendorp

An rf amplifier is designed by use of a CAD program, a desk-top computer, and a few necessary peripherals. Impedance matching and capacitance and resistance values can be determined for any number of circuit elements in series or parallel combinations. The resultant rf amplifier circuit design exhibits good performance with only minor adjustments in capacitor values.



Dale F. Mendendorp, Mobile Radio Engineering, Commercial Electronic Systems Division, Meadow Lands, Pa., received his BSEE in 1968 from Michigan State University. He worked for the Magnavox Co., Government and Industrial Division designing military oriented broadband rf power amplifiers prior to joining RCA in 1971. Since then he has been involved in the design of high-power broadband rf amplifiers, filters, and control circuits, and is currently Engineering Group Leader responsible for the design of a new series of transmitters for Mobile Radio applications.

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A GOOD SHARE of large-signal rf amplifier design usually centers around the matching of two impedances at one frequency or a band of frequencies. When working at a single frequency or very narrow bandwidth, a Smith Chart can be a very handy tool.

However, when designing broadband amplifiers it becomes necessary to match two impedances over a range of frequencies. Even when using a Smith Chart or other graphical aid, the procedure becomes laborious and time consuming. Most computer programs made available to aid the designer with problems like these fall into two main categories. Either they are an optimization type which requires an initial circuit which the computer then refines, or it is too specific in nature (e.g. assigns values to capacitors and inductors in a ladder network such that two resistances are matched together with a given circuit Q).

CAD program description

The CAD program described in this paper fulfills several requirements. It does not require a large computer system. This program is used with a desk-top computer with a few peripherals (H-P 9820 with 417 storage registers, math

Fig. 1 — Listing of program for HP9820 computer. File 1 is the mainline program. File 2 is the sub-program for series transmission lines; file 3 is the sub-program for shunt transmission lines; file 4 for series and shunt capacitors; file 5 for series and shunt inductors; and file 6 is the sub-program for series and shunt resistors.

File 1

```
0:
FXD 4;SCL -1;1;-
1;1⊢
1:
ENT "DATA IN FIL
E()";A⊢
2:
IF FLG 13=0;LDF
A;5→P34;GTO "P"⊢
3:
CFG 13;1→A⊢
4:
"O";ENT "ZL=",R3
1,"+J",P32,"AT F.
(MHZ)=",R33⊢
5:
IF FLG 13=1;A-1→
P34;GTO "P"⊢
6:
IF A=1;R31→R0;R2
2→P1;P33→R2⊢
7:
IF A=2;P31→R3;P3
2→R4;P33→R5⊢
8:
IF A=3;R31→R6;R3
2→P7;P 3→R8⊢
9:
IF A=4;P31→R9;R3
2→R10;P33→R11⊢
10:
IF A=5;P31→R12;P
32→R13;P33→R14⊢
11:
1→M→A;IF A=6;5→A
34;GTO "P"⊢
12:
GTO "O"⊢
13:
"P";CFG 13;PRT "
STARTING ZL"⊢
14:
PRT "RE,IM,FIMHZ
)"⊢
15:
PRT P0,P1,R2,P3,
R4,P5,P6,R7,R8,P
9,P10⊢
16:
PRT R11,P12,R13,
P14;ENT "NORM CH
ART TU";E⊢
17:
PRT "PLOT NORM T
O",B,"OHMS"⊢
18:
1→P15;IF R15=1;
GTO "A"⊢
19:
"M";ENT "SER=1;S
HUNT=2",R16⊢
20:
IF FLG 13=1;GTO
"I"⊢
21:
ENT "A=1;C=2;L=3
;TL=4",R17⊢
22:
IF R17=1;GTO 63;
LDF 6⊢
23:
IF R17=2;GTO 63;
LDF 4⊢
24:
IF R17=3;GTO 63;
LDF 5⊢
25:
IF R16+R17=5;
GTO 63;LDF 2⊢
26:
IF R16+R17=6;
GTO 63;LDF 3⊢
27:
"A";CLR DATA⊢
```

File 2

```
0:
ENT "Z0=",R35,"W
VLNGTHS=",R36,"A
T F(MHZ)=",R37⊢
1:
PRT "SERIES STRI
PLINE"⊢
2:
PRT "Z0=",R35,"W
VLNGTHS=",R36,"A
T F(MHZ)=",R37⊢
3:
1→A⊢
4:
"AA";IF A≠1;GTO
+2⊢
5:
R0/R35→R38;R1/R3
5→R39;R2→R40⊢
6:
IF A≠2;GTO +2⊢
7:
R3/R35→R38;R4/R3
5→R39;R5→R40⊢
8:
IF A≠3;GTO +2⊢
9:
R6/R35→R38;R7/R3
5→R39;R8→R40⊢
10:
IF A≠4;GTO +2⊢
11:
R9/R35→R38;R10/R
35→R39;R11→R40⊢
12:
IF A≠5;GTO +2⊢
13:
R12/R35→R38;R13/
R35→R39;R14→R40⊢
14:
R40→R36/R37→R41⊢
15:
IF R41=0.25;1E40
→R42⊢
16:
IF R41=0.75;1E40
→R42⊢
17:
IF R42=1E40;GTO
"AB"⊢
18:
TAN (360*R41)→R4
2⊢
19:
"AB";1-2*R39+R42
+R39↑2*R42↑2-R38
↑2+R42↑2*R38↑2+
2*R42↑2*R43+R43
↑2+R42↑2+R43⊢
20:
IF R43=0;GTO "AG
"⊢
21:
R38*(1+R42↑2)/R4
3→P44⊢
22:
IF R39-R39↑2+R42
-R39*R42↑2-R38
↑2*R42↑2*R38↑2
```

File 3

```
0:
ENT "Z0=",R35,"W
VLENGTHS=",R36,"
AT F(MHZ)=",R37⊢
1:
ENT "0 TERMINAL
L=",R46,"+J",R47
⊢
2:
PRT "SHUNT STRIP
LINE","TERMINAL
 2=",R46,"+J",R4
7⊢
3:
PRT "Z0=",R35,"W
VLNGTHS=",R36,"A
T F(MHZ)=",R37⊢
4:
R46/R35→R46;R47/
R35→R47⊢
5:
1→A⊢
6:
"BA";IF A≠1;GTO
+2⊢
7:
R0/R35→R38;P1/R3
5→R39;R2→R40⊢
8:
IF A≠2;GTO +2⊢
9:
R3/R35→R38;R4/R3
5→R39;R5→R40⊢
10:
IF A≠3;GTO +2⊢
11:
R6/R35→R38;R7/R3
5→R39;R8→R40⊢
12:
IF A≠4;GTO +2⊢
13:
R9/R35→R38;R10/P
35→R39;R11→R40⊢
14:
IF A≠5;GTO +2⊢
15:
R12/R35→R38;R13/
R35→R39;R14→R40⊢
16:
R40→R36/R37→R41⊢
17:
IF R41=0.25;1E40
→R42⊢
18:
IF R41=0.75;1E40
→R42⊢
19:
IF R42=1E40;GTO
"BB"⊢
20:
TAN (360*R41)→R4
2⊢
21:
"BB";1-2*R47+R42
+R47↑2*R42↑2+R46
↑2*R42↑2+R43⊢
22:
IF R43=0;GTO "BC
"⊢
23:
R46*(1+R42↑2)/R4
3→P44⊢
24:
(R47-R47↑2*R42+R
42-R47*R42↑2-R46
↑2*R42)/R43→R45⊢
25:
GTO "BD"⊢
26:
"BC";1E99→P44;1E
99→P45⊢
```

File 4

```
0:
ENT "C(PF)=",R35
,"W/SERIES L(NH)
=",R36⊢
1:
IF R16=2;GTO "CA
"⊢
2:
PRT "SERIES C(PF
)=",R35,"W/SERIE
S L(NH)=",R36⊢
3:
GTO "CE"⊢
4:
"CA";PRT "SHUNT
C(PF)=",R35,"W/S
ERIES L(NH)=",R3
6⊢
5:
"CE";1→A⊢
6:
"CB";IF A≠1;GTO
+2⊢
7:
R0/B→R37;R1/B→R3
8;R2→R39⊢
8:
IF A≠2;GTO +2⊢
9:
R3/B→R37;R4/B→R3
8;R5→R39⊢
10:
IF A≠3;GTO +2⊢
11:
R6/B→R37;R7/B→R3
8;R8→R39⊢
12:
IF A≠4;GTO +2⊢
13:
R9/B→R37;R10/B→R
38;R11→R39⊢
14:
IF A≠5;GTO +2⊢
15:
R12/B→R37;R13/B→
R38;R14→R39⊢
16:
(2*π*R39+R36*1E-
3-1/(2*π*R39*R35
*1E-6))/B→R40⊢
17:
IF R16≠2;GTO "CC
"⊢
18:
R37→R41;R38→R40+
R42⊢
19:
IF R16=1;GTO "CD
"⊢
20:
"CC";R37↑2+R38↑2
+R40↑2+2*R38*R40
→R43⊢
21:
R37*R40↑2/R43→R4
```

ROM, X-Y plotter, and cassette deck). It will plot and print incremental impedance data. It will accept any number of circuit elements in any combination of series or shunt resistors, capacitors, inductors or transmission lines.

As mentioned before, this program required the cassette deck and associated ROM with the H-P 9820. This is because of limited storage capability. The tape is used to store sub-programs which are called up by a main line program in much the same way as subroutines would be. If the computer had a greater storage capacity, it would be advantageous to use subroutines because of the relatively long cycle time required for the tape deck.

Operation of the program

Figs. 1 and 2 explain the operation and use of the program. The program initially asks for the starting ZL. This information consists of the real and imaginary components of the starting *ZL* and the frequency (in MHz) at which these impedances are measured. Such data may be called from a data file or may be entered manually from the keyboard. As many as five frequencies and corresponding *ZL's* may be entered from the keyboard, but five *must* be entered if data is loaded from the tape. When all of the data has been entered, the printer prints it out.

The computer then asks for the resistance to which the Smith Chart plot is to be normalized. When this has been entered, the value is printed out and the plotter plots the starting *ZL*.

Series or shunt configuration

The next question asked by the computer is whether the component to be added is in a series or shunt configuration and then whether it is a resistance, capacitance, inductance or transmission line. The appropriate sub-program is called up and loaded in the computer. It then asks for the value of the component. In the case of an inductor or resistor, it asks for inductance in nano-henries or resistance in ohms respectively. In the case of a capacitor, it asks for capacitance in pico-farads and internal series inductance in nano-henries. For a series transmission line, it needs characteristic impedance in ohms, length in wavelengths, and the frequency in MHz at which this length applies. For a shunt transmission line, the program also requires the complex load terminating the line. When the data has been entered, the component value and configuration is printed and the new input impedance is plotted on the Smith Chart.

The operator is now given the option of adding a new component, repeating the last one, or terminating the run (by punching RUN PROGRAM without entering data). If the program is terminated, the final input impedance is printed out.

Step-by-step approach

Figs. 3 thru 6 illustrate the use of the program in the design of impedance matching networks for the base and collector of a class-C, common-emitter broadband vhf amplifier. Fig. 3 shows the printout and Figs. 4 and 5 are the corresponding Smith Chart plots.

Step (1) shows the real and imaginary components of the input impedance of the transistor and the frequency at which

Note: Only portions of the CAD programs are shown in Fig. 1. Contact the author for the complete program.

```
1⊢
22:
(R37↑2+R40+R38↑2
+R40+R38*R40↑2)/
R43→R42⊢
23:
"CD"↓IF A≠1↓GTO
+2⊢
```

File 5

```
0:
ENT "L(NH)=",R35
⊢
1:
IF R16=2↓GTO "DA
"⊢
2:
PRT "SERIES-L(NH
)=",R35⊢
3:
GTO "DB"⊢
4:
"DA"↓PRT "SHUNT
L(NH)=",R35⊢
5:
"DB"↓1→A⊢
6:
"DC"↓IF A≠1↓GTO
+2⊢
7:
P0/ →P36↓P1/B+R3
7↓R2→R38⊢
8:
IF A≠2↓GTO +2⊢
9:
P3/B+P36↓R4 B+R3
7↓P5+P38⊢
10:
IF A≠3↓GTO +2⊢
11:
R6 B+P36↓P7/B+R3
7↓R8+P38⊢
12:
IF A≠4↓GTO +2⊢
13:
P9/B+R36↓R10/B+R
37↓R11+R38⊢
14:
IF A≠5↓GTO +2⊢
15:
R12/B+R36↓R13/B+
R37↓R14+R38⊢
16:
2**R38+R35*1E-3
/B→R39⊢
17:
IF R16=2↓GTO "DD
"⊢
18:
R36+R40↓R37+R39+
R41⊢
19:
IF R16=1↓GTO "DE
"⊢
20:
"DD"↓R36↑2+R37↑2
+R39↑2+2+R37*R39
+R42⊢
21:
P36+R39↑2/P42+R4
0⊢
22:
(R36↑2+R39+R37↑2
+P39+R37*P39↑2)/
R42→R41⊢
23:
"DE"↓IF A≠1↓GTO
+2⊢
24:
P40+R18↓P41+P19⊢
25:
IF A≠2↓GTO +2⊢
26:
P40+P20↓P41+R21⊢
27:
IF A≠3↓GTO +2⊢
```

File 6

```
0:
ENT "R(OHMS)=",R
35⊢
1:
IF R16=2↓GTO "EA
"⊢
2:
PRT "SERIES R(OH
MS)=",R35⊢
3:
GTO "EB"⊢
4:
"EA"↓PRT "SHUNT
R(OHMS)=",R35⊢
5:
"EB"↓1→A↓R35/B→R
35⊢
6:
"EC"↓IF A≠1↓GTO
+2⊢
7:
P0/B→P36↓P1/B→P3
7⊢
8:
IF A≠2↓GTO +2⊢
9:
P3. B→P36↓R4. B→P3
7⊢
10:
IF A≠3↓GTO +2⊢
11:
R6/B→P36↓P7/B→P3
7⊢
12:
IF A≠4↓GTO +2⊢
13:
R9/B→P36↓R10/B→R
37⊢
14:
IF A≠5↓GTO +2⊢
15:
R12/B→P36↓R13/B→
R37⊢
16:
IF P16=2↓GTO "ED
"⊢
17:
R36+R35+R40↓R37+
P41↓GTO "EE"⊢
18:
"ED"↓P36↑2+R35↑2
+P37↑2+2+P36+R35
+R38⊢
19:
(P36↑2+R35+R36+P
35↑2+P35+R37↑2)/
R38→R40⊢
20:
R35↑2+R37/P38+R4
1⊢
21:
"EE"↓IF A≠1↓GTO
+2⊢
22:
R40+R18↓P41+R19⊢
23:
IF A≠2↓GTO +2⊢
24:
R40+P20↓P41+R21⊢
25:
IF A≠3↓GTO +2⊢
26:
R40+R22↓R41+P23⊢
27:
IF A≠4↓GTO +2⊢
```

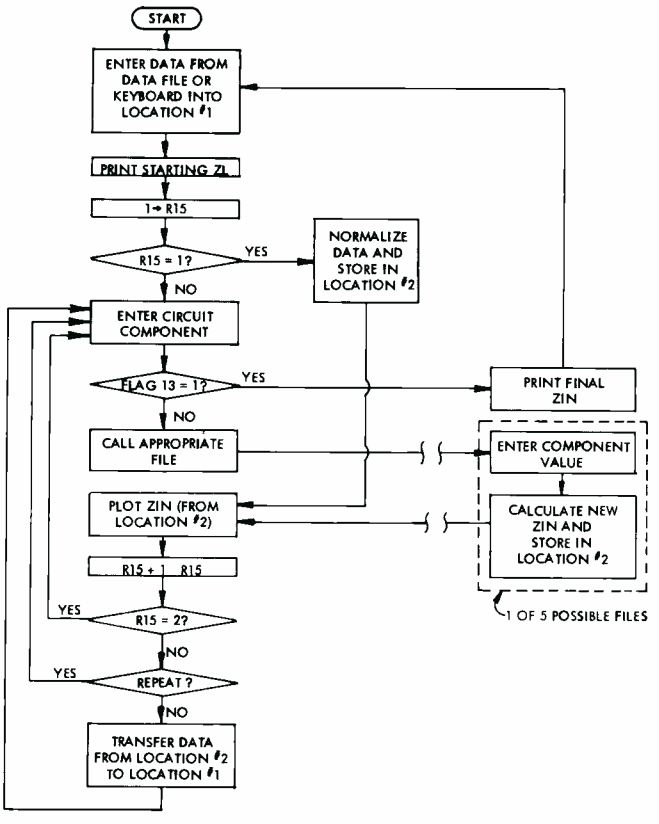

Fig. 2 — Flow chart for network design program.

the data applies. The resistance to which the Smith Chart plot is normalized is entered next. The next 11 steps are quite self-explanatory, but it should be pointed out that the success of the circuit arrived at is solely dependent on the expertise of the designer in that the program does not decide what type of component should be used or its value, but merely tells and shows the programmer the effect his choice has on the impedance transforming properties of the network.

The starting ZL of step (13) is the input impedance of the particular balun transformer used. The example illustrates working from the load back to the collector but it could just as well have been in reverse (i.e., starting from the collector and working up to the load).

Conclusion

The resulting circuit shown in Fig. 6 produces very good rf amplifier performance. The final circuit required only slight capacitor value changes. A more accurate design would have been accomplished if series and shunt resistance had been added to the circuit to simulate component losses.

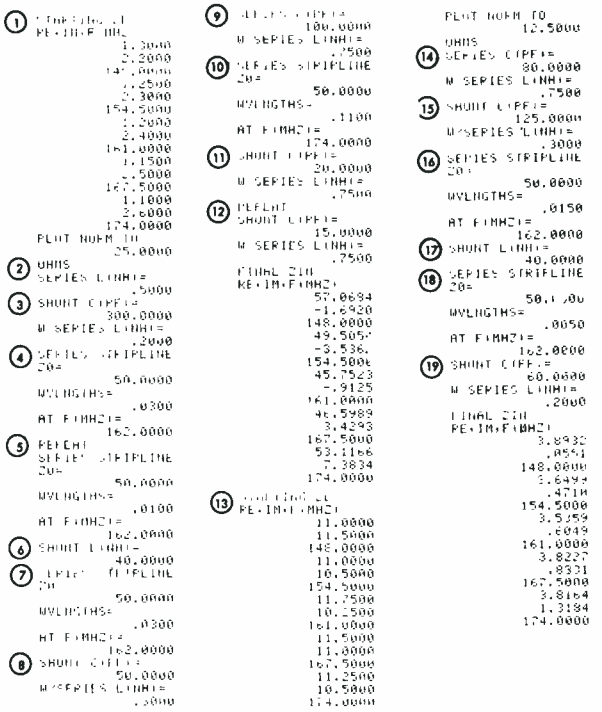

Fig. 3 — Computer printout for input and output matching networks for the circuit shown in Fig. 6.

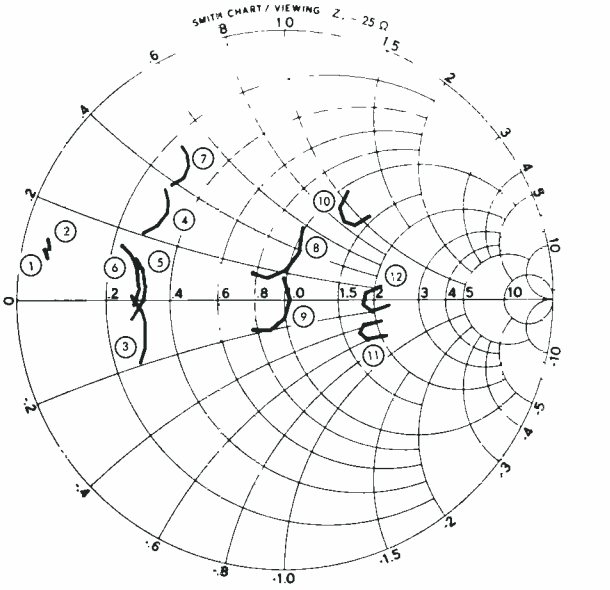

Fig. 4 — Computer plot on a smith chart of the input circuit impedance after each step of the program — The numbers related to those in Figs. 3 and 6.

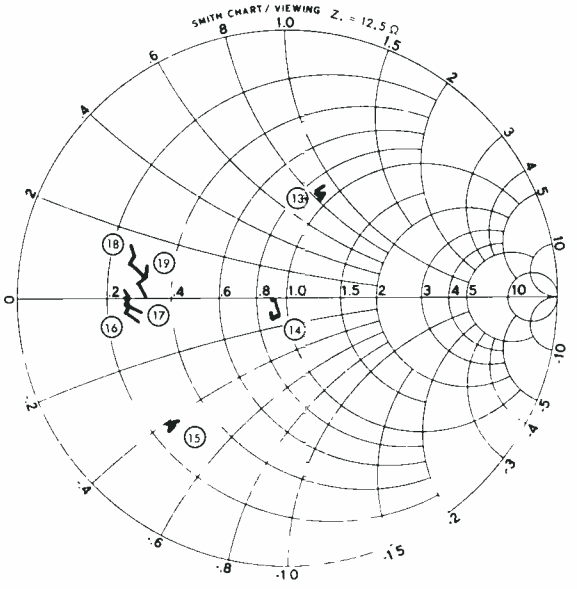

Fig. 5 — Computer plot on a Smith chart of the output circuit impedance after each step of the program — The numbers related to those in Figs. 3 and 6.

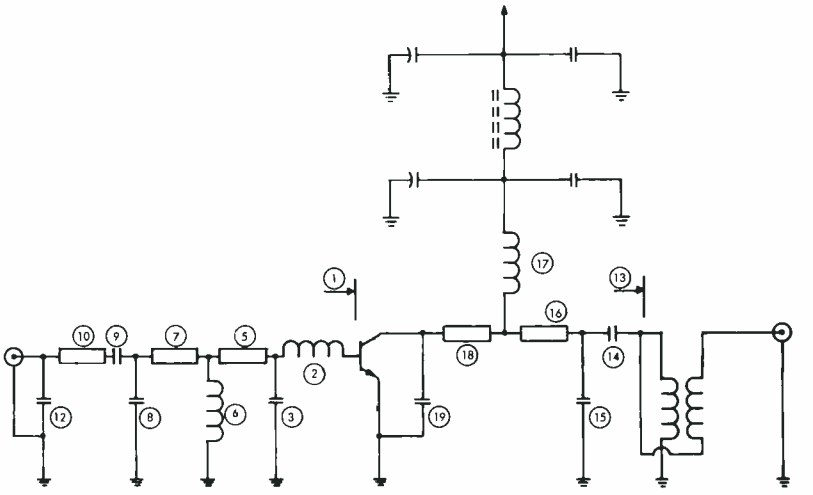

Fig. 6 — Schematic of amplifier designed using the program described.

Experience with interactive graphics

J.A. Bauer

Full automation of the design process for complex circuitry can often produce a chasm between the designer and his end product that reduces his control of the output. Interactive graphics systems have reintroduced a direct interface between the designer and his design, and in many cases have simplified the design process. This paper describes one such system in terms of its design functions and highlights a number of areas of application in present and future design problems.

COMPUTER AIDED DESIGN (CAD) techniques developed over the past decade are now finding widespread use in the design, manufacture, and test of electronic assemblies. Production use of these techniuqes has produced time and cost savings for devices ranging in size from integrated circuits up to multiple-layer hybrid and printed-circuit-board designs, and all the way to large backplanes with data derived from over a hundred logic diagrams.

Much of the production effort has existed on computer coding sheets, internal computer programs, printouts and final documentation, and machine control results. The result is little or no direct, visible interface between the designer and the end product. Recently, however, the development of Interactive Graphic (IAG) equipment and the increasing maturity of related programs have been combined to provide a cost effective, natural, and easy interchange of data between the human design capability and computer memory and manipulation.

The resultant Interactive Graphic System, properly interfaced with design automation programs, provides highly visible and graphically clear results. It has become, in effect, the visible tip of the design automation iceberg, focusing attention of even the most casual observer on the power of CAD to perform design effort more efficiently and effectively.

John A. Bauer, Mgr., Advanced Circuits Development and Technology Labs., Missile and Surface Radar Division, Moorestown, N.J. received the BSEE from Virginia Polytechnic Institute in 1947, and subsequently took courses at the U. of Pa., UCLA, and Bell Telephone Laboratories. He is presently responsible for design automation and advanced circuit design within MSRD. The current standard circuit module packaging system "MICROPAK" utilizing the data capture and documentation program "AUTODRAFT" and the automated wire wrapping programs "AEWRAP" were developed in his group. Previously, Mr. Bauer was head of the advanced data systems department of the Instrumentation Facility, Bendix Corporation, Pacific Division, where he was responsible for design of military and commercial digital data transmission and data handling systems. As a research engineer at Franklin Laboratories, between 1948 and 1952, Mr. Bauer participated in electronic design and development of analog computer circuits, fm data transmission, noise signal sources, and photoelectric circuits. He holds several patents in the digital and control fields.

MSRD installation

The Interactive Graphic System used for design and graphic editing at MSRD is shown in Figs. 1 and 2. It is similar to a number of installations at other RCA Divisions. The system was manufactured and installed by the Applicon Corporation of Burlington, Massachusetts, and programs in use have been generated by Applicon and several groups at RCA, including MSRD, GCASD, AED, and SSTC.

The system (see Fig. 3) includes both keyboard and electrostatic-tablet manual control with extensive macro-instruction capability, plus character recognition via the electrostatic tablet. A storage CRT and hard copier supply the real-time display and fast copy output at both operating stations. With the fast core (1-μs access time) and the large disc memory provided, the operator can control both installation and operation of sophisticated graphic libraries and motion programs. A full set of input/output devices provides excellent interfaces to other systems.

Fig. 3 also shows the real-time operator input/output devices, hard copy outputs for engineering review, interfaces between batch computer programs, precise artwork generators and numerically controlled manufacturing and test machines, and the necessary program development interfaces.

As might be expected, the first experiences with less complete equipment were only marginally productive. Currently, however, the full system implementation is in continuous, productive use for a variety of tasks.

Modes of operation and utilization

Four major modes of operation have been developed for a range of design tasks. Selection of the most effective mode for a given task depends on the availability of design automation (DA)

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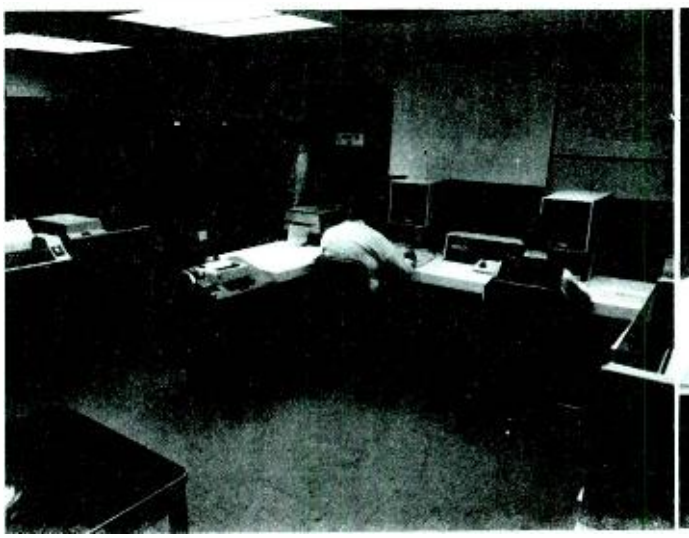

Fig. 1 — Interactive graphic design-editing facility at MSRD.

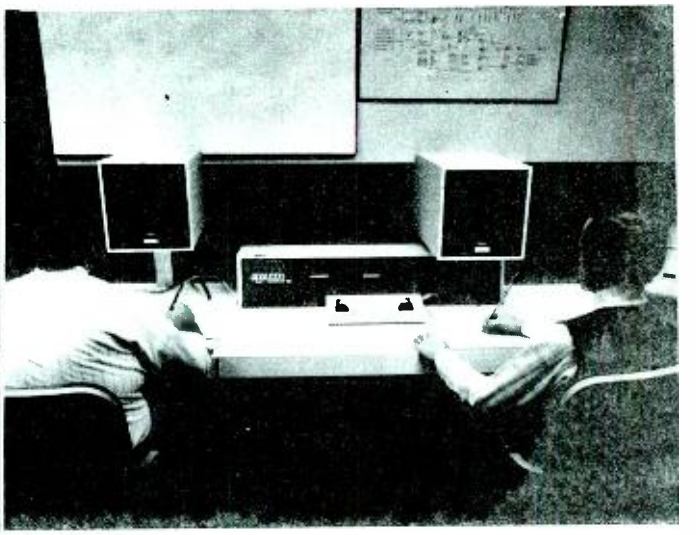

Fig. 2 — Close-up view of editing stations.

programs capable of performing the task. As automated programs mature and expand to take over what are currently manual tasks, they will be used. Conversely, new design rules required by a new circuit family can outpace the development of automated programs, thereby necessitating a reversion to more manual operations with the computer-aided interactive graphic system. For instance, an automated routing program for multiplayer printed circuit boards (with some editing using an interactive graphic system) may be currently cost effective: tomorrow, however, the engineer may require a higher speed circuit family with tighter interconnection wiring rules for which no DA programs exist. In that case, it is more cost effective to design with a CAD system in which the engineer implements wiring rules as he selects and places the components and lays out the wire routing.

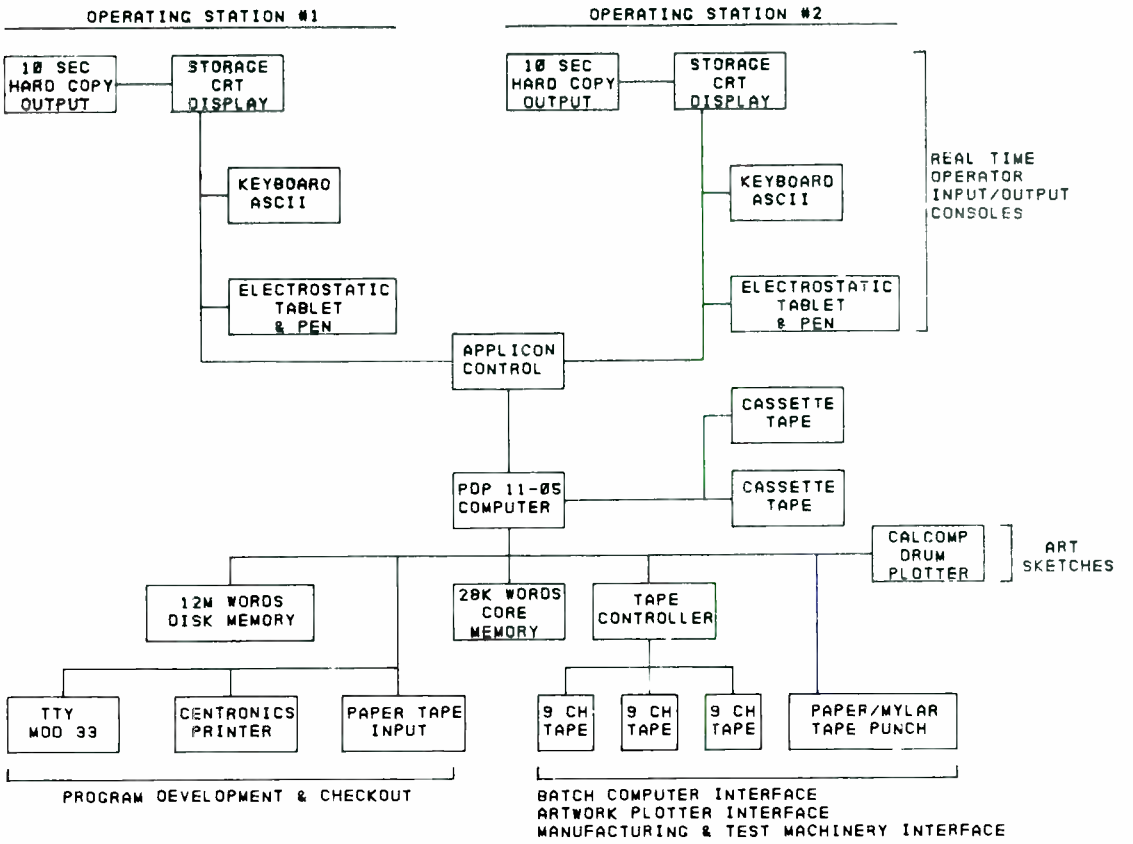

Fig. 3 — Interactive graphic system block diagram (this artwork produced directly on the Interactive Graphic System).

A very high-speed circuit layout requires that additional driving components be added if placement and routing cannot be completed within very restrictive rules. Such a case occurred for the layout of a seven-layer printed circuit board with ECL-10000 circuits. This task was accomplished with high cost effectiveness by CAD techniques using the Interactive Graphic System. The resultant composite layout of four microstrip (controlled wiring impedance) layers, a ground layer, and two voltage layers, is shown in Fig. 4. In this case, after an industry survey failed to produce a DA program which would implement the desired wiring rules within the computer programs, it was determined to be more cost effective to implement the wiring rules visually on the Interactive Graphic System rather than to automate the rules.

Mode 1 — complete design by operator at the interactive graphic unit.

Component layout, placement, and routing are determined on the CRT by the designer. This mode is most cost effective for small- to medium-complexity assemblies and is in current use for design of simple to medium-complexity thick-film hybrids, printed circuit boards, chassis and microwave stripline units. As the libraries of components are made more complete, and as the designer's skills and familiarity with the design types improve, the work is speeded up. A fairly complete group of library elements for thick-film hybrids and printed circuit-board designs is available, and the chassis and microwave libraries are growing. Documentation control is also being added, with RCA drawing formats as library elements. Examples of typical components designed with this mode of operation are shown in Figs. 5 and 6.

Mode 2 — layout copy and editing of rules

Complex layouts with detailed engineering rule implementation can best be prepared on matrix layouts by the Interactive Graphic unit operator (Fig. 4). The matrix copy given to the engineer is returned with his initial component placement. The operator then copies the placement information into the Interactive Graphic system and applies detailed routing in accordance with known interconnection rules produced by the engineer. This procedure makes best use of the skilled operator, and the engineer produces results with minimum turnaround time. It would not be used if every engineer could develop the manipulation skills to the degree of a skilled operator. Since operator training and skill level development require continuous application to develop efficient speed, it is impractical to train most design engineers to that level. Likewise, the IAG operator cannot be conversant with all of the newly developed design rules. In time, it is expected that this type of operation will be supplanted by a DA program, or operator training in the design rules.

Mode 3 — editing of automatically routed logic diagrams and hybrids

Complex thick-film hybrid layouts are difficult to keep track of, and system logic designs depend on accuracy of interconnections to produce useful results.[1,2] It has been found more cost effective to control the interconnection or "net" list, especially in relatively large system designs in which the information depicted on a hundred logic diagram "sheets" provides thousands of connections to hundreds of different circuits that are to be interconnected. Therefore, data entry of net lists directly to a large DA control, and an automatic routing program such as AUTODRAFT, accurately preserve the interconnections even though the automated routing program may be blocked from completing the graphic routing or the resultant routing is not esthetically pleasing.

In these cases, results of the batch-run, automatically routed program are entered via magnetic tape into the Interactive Graphic system, where routing completion and editing are performed by the operator. It is usually relatively easy to complete routing of two-layer connections such as those used in drafting convention, or two-layer hybrids where simple blockage can be corrected by rerouting. Usual experience with the AUTODRAFT program used for logic diagrams is 100% completion (with esthetic changes required), and 98% completion on two-layer hybrids. These programs work within predetermined rectangular limits as demanded by the usual predetermined formats. It is more difficult to change diagram size radically, since both placement of components and interconnection routing must be changed.

Mode 4 — engineering change operation

The process of graphic design includes

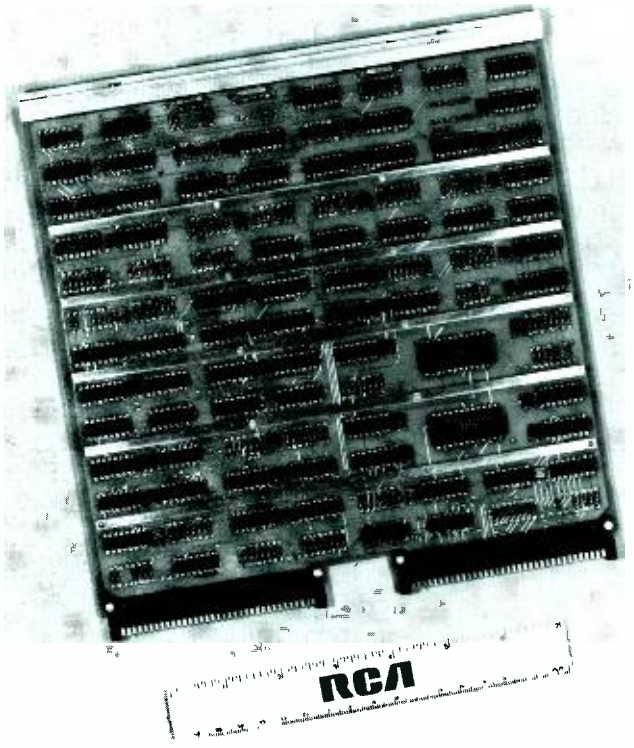

Fig. 4 — Seven-layer printed-circuit board containing and interconnecting high-speed digital circuitry (9 x 9.3 in.).

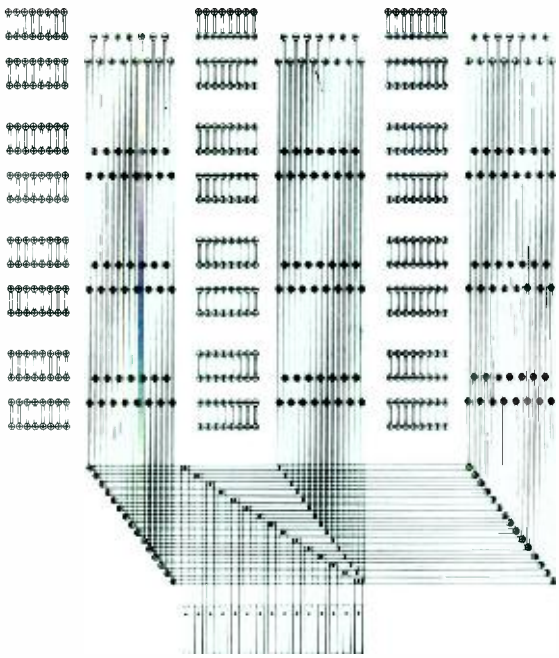

Fig. 5 — Typical two-layer printed-circuit board with repetitive patterns.

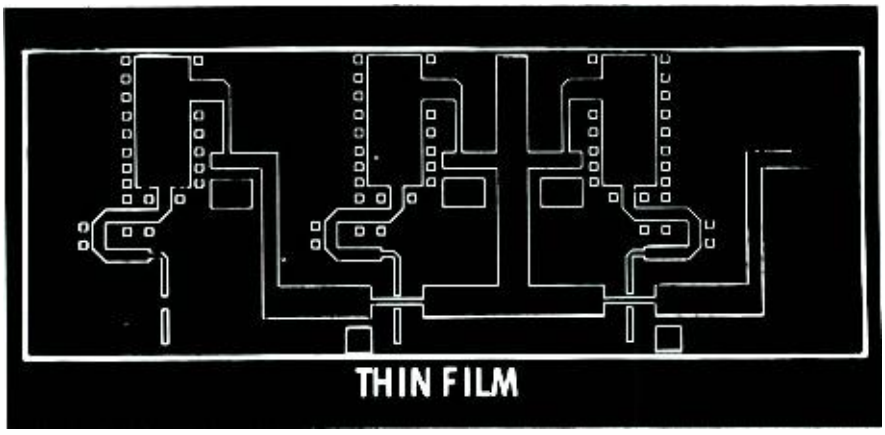

Fig. 6 — Typical two-layer stripline microwave assembly.

engineering and manufacturing design review modification which can be implemented rapidly during the design process. It is also important to structure the system for convenient data retrieval of old filed information resulting from engineering change revisions as a result of engineering test debugging or model modifications.

To facilitate this operation, two major items have been programmed into the system. The first is the ability to index, find logic or other graphic information sections, and read and display computer records of logic diagrams generated before the interactive system was put into use (several thousand of which may be on active file on magnetic tape). The second is the capability of modifying data-producing cards, refiling graphic data, and re-entering the data into subsequent programs. This latter point, although it appears to be a trivial problem once the graphic data is available, is one of the more difficult tasks in actual practice — especially where a large amount of alphanumeric data is contained within the graphic representation and where the data (through graphic editing) is rotated, moved, and reoriented. Separate but coherent control is imperative in providing readability of graphic data that is combined with alphanumeric data. A rotated or flipped graphic symbol is readable as long as the alphanumeric data remains right side up and is readable from left to right. In addition, the alphanumeric data must remain pointed to the correct graphic spot if it is to be read into subsequent programs.

Growth potential of interactive graphics

Expanded use of Interactive Graphic systems will depend on time and cost tradeoffs with effective use of available DA programs. An additional factor in Interactive Graphic utilization is the level of engineering, programming, and design training required for those designers who are capable of generating new ideas and uses. To aid in the specialized training area, MSRD has developed (along with other RCA activities and the Applicon Corporation) a video training course on *basic* operating factors. This series, produced in MSRD, consists of twenty-one 20-minute lectures by T. Lucas of the Applicon Corporation.

It is anticipated that additional major growth will be provided through interaction of RCA operating units solving specific local problems which have applicability to other operating units by virtue of equipment commonality. As an example of this interaction process, we have already seen almost complete circuit libraries for standard-cell COS/MOS-SOS custom integrated-circuit designs which will be adapted by other operating groups at very little cost.

Some specific areas of growth potential are identified here in light of work already in progress:

- Integrated-circuit design and checking
- System flow and timing documentation
- Three-dimensional mechanical drawings
- Scheduling data and updates

Additional growth may be directed toward high-speed communications interconnections, with more powerful computer facilities to perform large simulation and test routines. Although the time/cost economics have not yet been justified, and although substantial work remains to be accomplished, there seems little doubt of the continued rapid growth and expansion of Interactive Graphics use.

References

1 R.F. Kole, "Design Automation for Multiplayer Thick Film Hybrids," *this issue*

2 J.A. DeVecchis and J.W. Smiley, "Automatic Design System for Backplanes and Modules, *this issue*.

Automated design for backplanes and modules

J.A. DeVecchis| J.W. Smiley

Two related automated systems are described in terms of their application to current and future problems of intricate backplane and module design for large radar data processors. The systems carry through the entire design process, beginning with initial logic sketches and finally producing complete programs for automated fabrication and wire wrap. Also included are simulation programs for complete checkout of circuit logic prior to manufacturing.

AUTOMATED DESIGN of both backplanes and modules was inevitable. Consider the amount of data required to construct a standard cabinet of radar signal processing equipment. To mount and interconnect 12,000 high-speed integrated circuits contained on 1200 modules and interconnected with 40,000 wires on four backplanes requires data capture from approximately 400 logic diagrams each measuring 2 × 3 feet. The handling of 10-million pieces of information concerning circuit type, interconnection types, and location is also required, as is the calculation of wire routing and control of machines for automated production and test.

Conventional methods for performing these tasks are extremely time consuming, and there are countless chances for human error. Automation is the logical solution to the problem. Therefore, the evolution of two such systems—an automated design system for backplanes (ADS-B) and modules (ADS-M) — is discussed is this paper, along with descriptions of the systems developed.

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James A. DeVecchis, Marketing Department, MSRD, Moorestown, New Jersey, received the BSEE degreee from Drexel University in 1966. He joined the Communications Systems Division in Camden upon graduation, engaged in design and development effort in the Magnetic Recording and Television group. In 1968 he was transferred to MSRD where he became associated with systems integration programs and later in design effort on a variety of signal processing and data processing assemblies for major systems. In recent years his efforts have been devoted to development of design automation systems, with particular emphasis on automating complex hybrid layouts. As part of this effort he prepared an extensive operating manual detailing a basic automated design system for hybrids. In 1974 he transferred to the MSRD Marketing Department where he is currently a sales representative for the Strategic Systems business area. Mr. DeVecchis is a member of the IEEE and Eta Kappa Nu.

John W. Smiley, Advanced Technology Engineering, MSRD, Moorestown, New Jersey received the BSEE degree from Lafayette College in 1952. After a tour in the U.S. Army as a Signal Corps Officer, he joined the Communications Systems Division at RCA in Camden in 1953, involved with military television applications. Then, in Digital Applications Engineering, he was active in the design, development, fabrication, and test of the AN/GRA-5 digital communication system, part of the Sage system. In 1961 he was assigned to the Micropac computer program which was to be a test vehicle for the newly developed micromodules. In 1964 he was assigned computer programming tasks and developed a memory diagnostic program for fault isolation to the component level for the MICRORAC computer system. From 1967 to present, he has been responsible for program development, maintenance and operation of design automation programming systems. At present, he is engaged in upgrading the AEGIS-EDM-1 system, revamping some programs and replacing others with more cost effective software.

Background

Development of a wire-wrap automatic design system for backplanes (ADS-B) was begun in 1970 to support the design and fabrication of large radar data processing systems, such as the AEGIS and AFAR Systems. Typically, these systems use 4000 to 6000 plug-in modules which contain approximately 50,000 integrated circuits.

As initially developed, the system contained about 170,000 source cards with 430 routines or programs. Even while in use, it was reviewed and modified for cost effective improvements. In some cases, complete program modules were replaced by redesigned modules.

The AEGIS and AFAR systems contain primarily T^2L circuitry which requires extensive wiring rules. The ADS-B system was designed to check for rule violations, flag them when found, and to implement other rules during the automatic wiring design in the AEWRAP part of the ADS-B system.

Later, the automatic design system for modules (ADS-M) was developed as a spinoff of the ADS-B system. The ADS-M system was created by combining a

Authors DeVecchis and Smiley at the Applicon terminal.

number of programs with the ADL Programs of ADS-B. The basic purpose of this system is automatic generation of the artwork necessary to produce complex thick-film hybrids.

Backplanes (ADS-B)

Autodraft

The automatic design system for backplanes (ADS-B) accepts logic sketches from the engineer and supplies him with validation information, logic drawings in MIL 806B format, and wire wrap fabrication information (Fig. 1). The first major block in this system flow diagram is *Autodraft*, *Input*, and *Autoroute*, known as ADL. In this particular block, raw logic sketches are prepared by the engineer, using guidelines referenced in the *Autodraft* User's Manual. These sketches are then coded by a data processing group for the *Autodraft* program.

The program *Autodraft-Input* examines and stores the input data, comparing it against stored symbol library definitions. If discrepancies exist in the input data, they are corrected and the program is rerun.

Next, the *Autodraft-Autoroute* program is run. By using a modification of Lee's routing algorithm, this program takes the symbol locations, orientations, pins and connectivity information, and routes the interconnecting nets. A logic sketch could be plotted at this point.

Next, program AAIFT is run to convert the *Autodraft* data to the Interactive graphic (IAG) format. The data tape containing the logic sketches is then loaded into the interactive graphic system. The sketch is edited on the display to improve the drawing layout, to correct all known errors, and to make all changes required. When the sketch is satisfactory, is it copied for an updated logic sketch file for subsequent processing. CalComp logic drawings are now available.

When all the logic sketches of a panel have been processed through IAG, program AAIFT2 translates the IAG data structure back to the *Autodraft* data structure. Then *Autodraft*-net list program is run. The purpose of this program is to group all the nets of a backplane panel into a single net list. A net report is printed which may list net inconsistencies; if inconsistencies exist, flags occur and changes are required. They are entered into the IAG and the program is rerun until all inconsistencies are resolved or corrected.

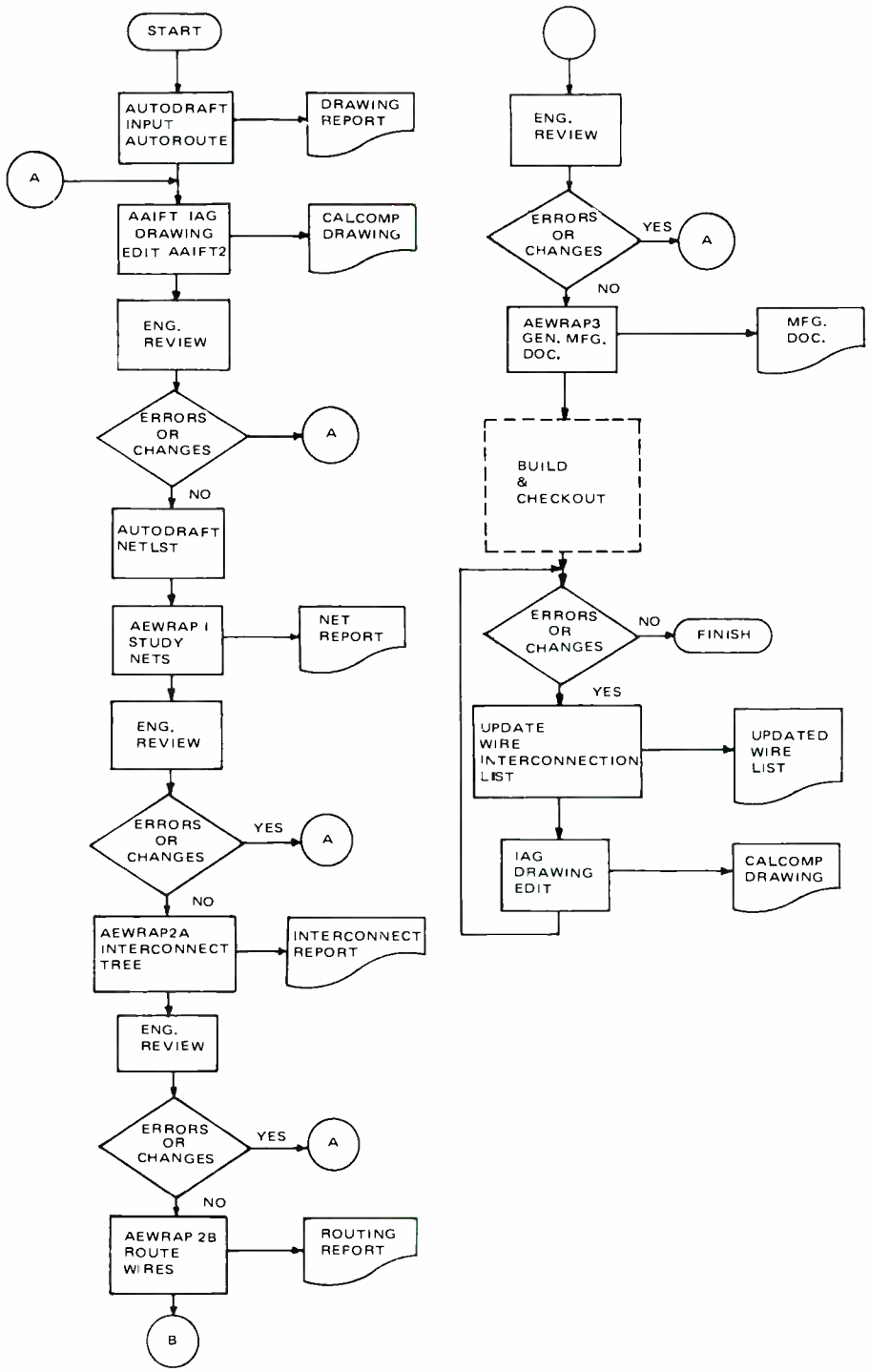


Fig. 1 — Wirewrap-backplane-automated design system.

AEWRAP

The next major portion of the ADS-B system is AEWRAP. In the most general sense the AEWRAP system takes in sets of pins that are destined to become interconnected and, through access to circuit detail and wiring rules, performs such interconnections and produces the appropriate documentation and media for automatic fabrication machinery. Examples of such machinery are the Gardner Denver wire wrap machine, the PIC semi automatic wire wrap machine, and

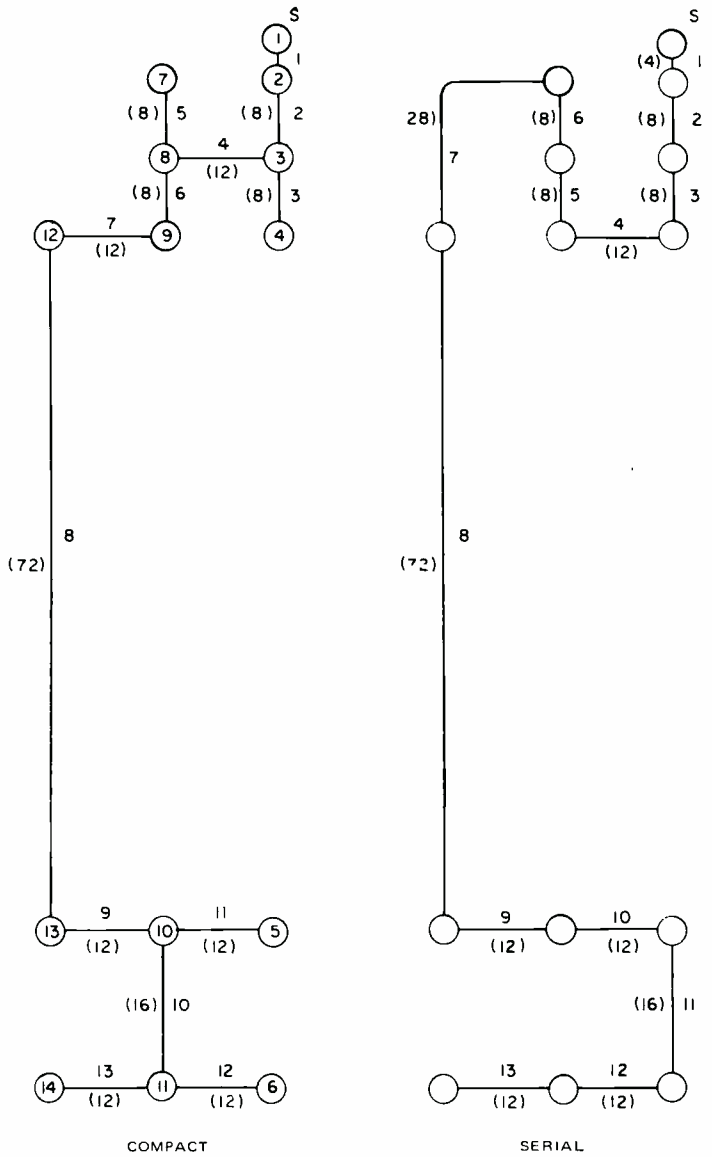


Fig. 2 — Example of two tree-construction algorithms: serial tree, and compact tree.

the DITMCO automatic interconnection tester.

At its highest level segmentation the AEWRAP system is divided into three distinct phases:

1) Phase I: AEWRAP → (Preprocessing)
2) Phase II: AEWRAP 2A (Wiring Design) and AEWRAP 2B (Routing)
3) Phase III: AEWRAP 3 (Post Processing)

Each of these phases is briefly outlined in the paragraphs which follow.

Phase I — AEWRAP 1

The AEWRAP I preprocessing consists basically of preparation and validation of some of the important files required by the process.

1) The *circuit board file* represents one copy of each circuit board or module which is encountered in the modern systems. Every module used in the implementation of the digital equipment is represented once and only once in this file. This one file is common to all backplanes and is developed only once.

2) The *geometry file* is unique to each backplane and basically represents which circuit module plugs into which slot on the backplane. Every slot (connector) is accounted for in this file.

3) The *frame file* is basically a combination of the board file and the geometry file. This file represents all the wiring pins on a backplane and the appropriate circuit characteristics behind each pin. In addition to all the physical pins, the frame file actually represents every point of a tenth-inch grid pattern of a backplane. All physical pins are part of this basic grid pattern of a blackplane.

4) The *Wire File* is derived from the *Autodraft* net list which is the basic input to AEWRAP. A net is a set of pins with a common name (logic signal or logic function) signifying that such a set of pins will be physically interconnected into the "tree" or "copper path." During processing in Phase I, the net list as received from *Autodraft* is converted into the wire file "from-to" format. Each net is basically "wired" into a single string according to pin number sequence. The wire file at this point does not reflect actual wiring.

In summary, Phase I basically contains the tools for creating and maintaining the fundamental systems files described above, and at several points in the process there are feedbacks in the form of error listings to the engineer responsible for the equipment being processed. The last program in Phase I provides the engineer with an assessment of how his wire file adheres to loading and wiring rules. Although the Wire File does not reflect the actual wiring yet, such an assessment is of high diagnostic value as trouble spots can be identified before the serious processing in Phase II.

Phase II — AEWRAP 2A and AEWRAP 2B

In AEWRAP 2A, program CONTRE, the wire file is broken down to the basic nets. All possible wires and their lengths are created from such nets. Thus a net with N pins will create N (N-1) 2 possible wires.

When the file of all possible wires is created, it is used in two tree construction algorithms which, for each net, construct actual trees with fundamentally different characteristics; these are:

1) The *serial construction* utilizes a single string; (*i.e.*, only two connections per pin) with the additional requirement that the source pin be at one end and the terminator (if any) be at the other end. The serial tree may be modified when clusters of pins are detected.
2) The *compact construction* is less restrictive and simply requires the use of minimum overall wire length.

The electrical character of both types of tree construction is tested, the final selection is made, and the wire file is modified accordingly. Fig. 2 shows an example of both a serial and a compact tree. The wire file, at this point, reflects actual wiring;

i.e., the end points of each wire will not change; however, the routing of each individual wire is yet to be accomplished.

On AEWRAP 2B, program BROUTE, each wire of a tree is routed on the backplane taking into consideration the routing of all other wires or trees. Also, it considers the acceptable routing patterns of the Gardner/Denver wire-wrap machine and switches wires to twisted pairs if there is no direct solution to crosstalk problems.

Initially, the wire-file record is read completely through and all ground-pin usage is inserted into the density map. Predescribed routed wires are added to the channel map.

After the wire file is rewound and read again, each of the presorted nets is routed for the "best" route, wire-by-wire. The best route is examined to determine if it violates the maximum allowable parallelism rule for the net being routed. When there is a parallelism violation, the wire (if single), will be assigned as a grounded twisted pair and a ground wire assigned to the wire. If the tree is serial, a switch is set so this wire and all subsequent wires of the net are assigned twisted pairs. Wire lengths less than 1.5 inches are not assigned as twisted pairs.

Once the BROUTE program is completed, the wire file is basically complete in that all electrical connections and their routines are contained in the wire file.

Phase III — AEWRAP 3 (post processing)

In AEWRAP 3 the basic preparation of manufacturing data and documentation takes place. The first step determines what wires can be passed to the Gardner/Denver automatic wire wrap machine for handling on a fully automatic basis. In the first program the entire wire file is passed through a set of validation criteria which checks each wire for an appropriate wiring pattern acceptable to the Gardner/Denver machine.

The next step is the assignment of an actual wiring level to each pin. Since each pin has only room for three wraps, it is important that different types of wires are leveled correctly. At several points in prior processing, a check has been performed to ensure that only three wires are connected to each pin. In the level program one final check is made and all wires are put into the manufacturing wiring sequence; the wire categories are:

1) Gardner Denver wiring;
2) Semiautomatic or PIC machine wiring, basically twisted pairs; and
3) Manual wiring - basically special cases.

The PIC wiring is leveled first and from the top down (level 3) — and subsequently from the bottom up (level 1). Subsequent to leveling, the wire file is split into the three individual files relative to the categories defined above.

The file containing the Gardner/Denver wiring is now processed through several programs to perform respectively; the Gardner/Denver tooling and coordinate conversion, translation to the binary Gardner/Denver language, and punching of cards to drive the actual Gardner/Denver machine.

The semiautomatic or PIC wiring undergoes a similar although not nearly as complex processing in another program. Since the PIC machine is driven by paper tape, the last program in this chain produces the actual paper tape. The file containing the manual wiring is simply printed in a legible manner for the wireman. This list is generally very small; ideally it would be nonexistent.

After the fabrication data has been produced, the three categories of wiring information are merged in a program to produce the final wire-connection list (FWCL) issued through the drawing number system. This file can be maintained through yet another program.

The purpose of merging these different kinds of wiring information into file is to produce one single paper tape with *all* electrical connections on it. This tape drives the DITMCO tester, which checks every electrical connection on a fully wired backplane.

Aside from regular maintenance of the wire connection list, the production of the DITMCO tapes is the last step in the AEWRAP automation process.

Logic integration (LOGIN) and Logic simulation (LOGSIM)

Prior to fabrication of a backplane the associated logic may be checked out functionally by a simulation program. The programs *Login* and *Logsim* have been developed for this particular purpose. The *Login* program provides an automated interface between *Autodraft* and *Logsim* programs. The *Login* library, specified once, contains a logical description of each *Autodraft* logic symbol representing an electric circuit or logical function in terms of *Logsim* logic elements. The user specifies the drawings to be simulated, the driving signals to exercise the logic, and the nodes of the logic network to be monitored. *Login*, reading the *Autodraft* data base file for those drawings, extracts the pertinent logic network data, converts to *Logsim* elements, and generages an input tape for *Logsim*.

Logsim is a logic simulation program which generates the output of one or more gates in a logic network, based on the specified network description, delay characteristics, and input driving generators. *Logsim* presently recognizes 20 basic logic functions and can be

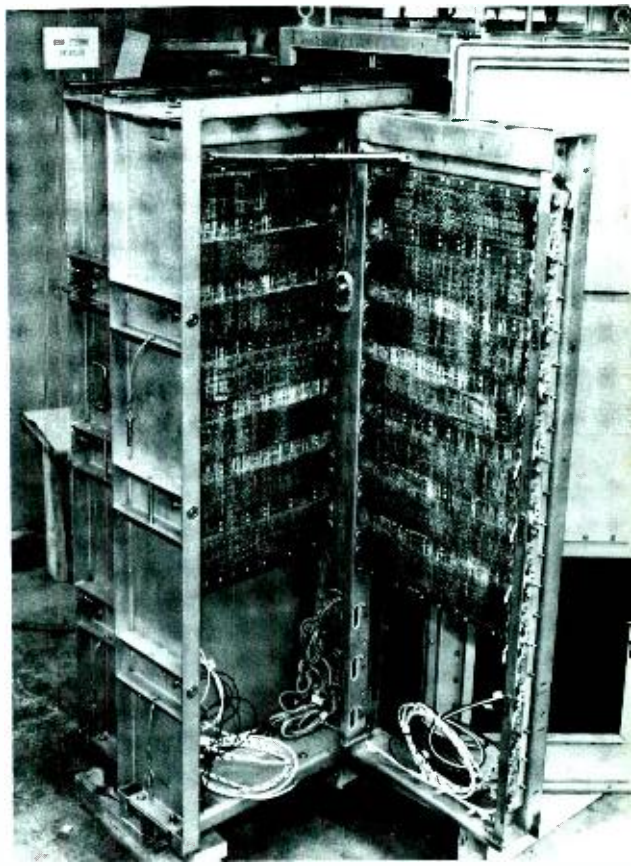


Fig. 3 — Photo of an AEGIS cabinet containing a number of backplanes.

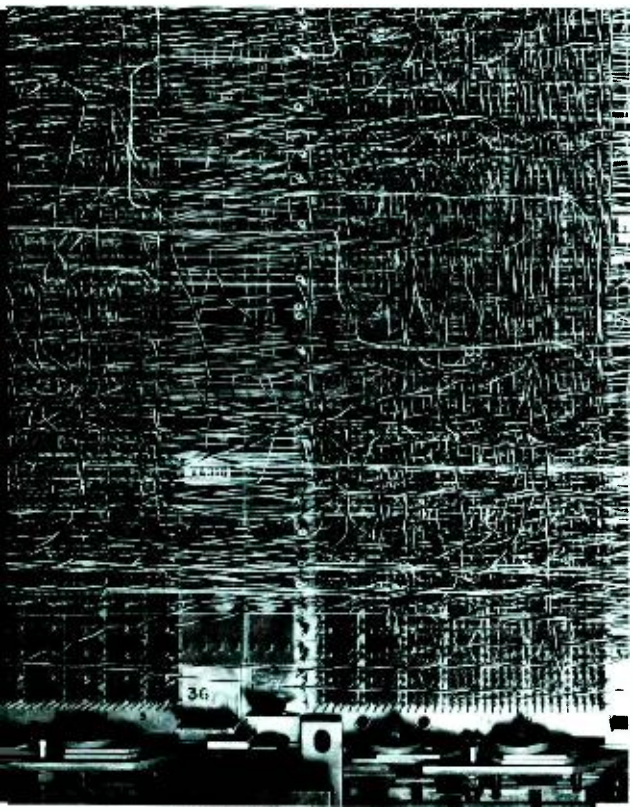


Fig. 4 — An AEGIS backplane that has been automatically wired.

expanded with user-defined functions. Logic element delays can be described as fixed, a function of number of loads, or randomly distributed. *Logsim VI*, the most recent version, allows combinatorial logic devices (such as ROM's) to be defined as truth table functions. The *Logsim* program verifies the input data and net list, initializes the logic, and produces the simulation output.

The basic output of the simulation is a timing diagram listing binary output levels of selected gates during the time intervals specified by the user. An optional output is the comparison of selected gate outputs specified by the user with those outputs generated by *Logsim*. Diagnostic messages are printed whenever errors in input data or unusual operating conditions are encountered.

This simulation capability results in paper breadboarding and worst-case component substitution before actual hardware implementation, thus providing substantial cost savings by proving the design before fabrication. It also generates the necessary response data for testing of the hardware. The logic simulation capability is designed to run on the Spectra 70 Computer. On a system with 262,000 bytes of memory, the system is capable of simulating networks containing more than 3,000 logic gates.

The automated design system for backplanes (ADS-B) has been used effectively in the manufacture of signal processors for two major systems. Fig. 3 is a photograph of a typical cabinet with a number of backplanes. Fig. 4 is a close-up view of one of the automatically wired backplanes.

Modules (ADS-M)

Specifically, the concept of the automated design system for modules was created to handle the layout design for a complex hybrid module with a manufacturing output. The philosophy was to develop a time-and cost-effective system that utilized existing technology. To achieve this objective, a system was developed incorporating the automatic design language (ADL) with an interactive graphic system (IAG) and supplying manufacturing outputs. Fig. 5 is a flow diagram of this ADS-M system.

The ADL programs have been described under the ADS-B system; to utilize these programs, the following information is required:

1) Overall Net Interconnection List,
2) Chip types with physical dimensions, and
3) Module and substrate dimensions.

With these data, the chips are located on a scaled grid and a placement study is made. Once the chips are located, interconnection symbols are defined and positioned around the periphery of the integrated circuit chips. The symbol placement and net information is coded and processed. If placement is not acceptable, the symbol location is readjusted until a desirable placement is found. A line plot and a listing of net information is now available.

After ADL-Autoroute has been run, program THK-FLM reads the ADL file and develops *line* and *via* information in a PLOTS program format. All horizontal lines are assigned as metallization on level 1, vertical lines on level 3, and connector dots as *vias* on level. At the end of each line segment a *via* is assigned on level 2.

The following succession of steps to place a drawing on the IAG system was developed by SSTC, Somerville, and is part of their artwork design automation system. Program ARTS reads the PLOTS file on tape and converts it to a DFL file on tape. The PLOTS format is analogous to source statements and the DFL format is analogous to the compiled output of a routine. An IAG program UCMD3 converts the DFL format to an IAG format and the data is entered into the interactive graphic system. The drawing is now available for editing; the editing includes the following:

1) Placement of electrical components in the desired location,
2) Addition of termination pads around the chips for wire bonding, and
3) Removal of excess *vias* and extended interconnection routes.

It should be noted that the termination pads and electrical components are predefined in the IAG library. Once the editing is completed, the final nets are validated against the original input. Once the net validation is completed, data can be available for manufacturing as a Cutter or Gerber output.

The ADS-M has been successfully utilized in the layout of the ATL-B12 complex hybrid.

Conclusions

The utilization of the ADS-B concept in the development of a complex, high-package-density system has provided a 40-to-1 time advantage over older design and assembly techniques.

The application of the ADS-M concept in the development of complex hybrids has reduced the size of the package by 25%, the number of metallization layers from three to two, and the layout design time by at least 50%.

These design automation systems are clearly effective design and manufacturing tools. Moreover, these design automation systems are by no means limited to T^2L technology. Currently these programs are being reviewed and updated to handle system designs which will utilize LSI, ECL 10,000 and CMOS/SOS circuit types. The design automation programs in use today are of such flexibility that all new circuit technology presently known and anticipated, can be handled without difficulty.

Acknowledgments

Development of the systems described in this paper results from a joint effort involving many contributors. In particular, the contributions of the following are acknowledged: Charles Brumbaugh of the Solid-State Technology Center, for his assistance with ADS-M; John Douglas of MSRD, a principal designer of ADS-B; David Drumheller of MSRD, for his development of IAG routines; Howard Edels of MSRD, for his help in planning ADS-B, and ADS-M; Bernard Wiegand of MSRD, for his development of ADL-AUTOROUTE; Arnold Kress of CSD, for his encouragement in the design of AEWRAP; the Samuel Neiss and Harvey Saunders of Palm Beach Division, for their review and recommendations for AEWRAP.

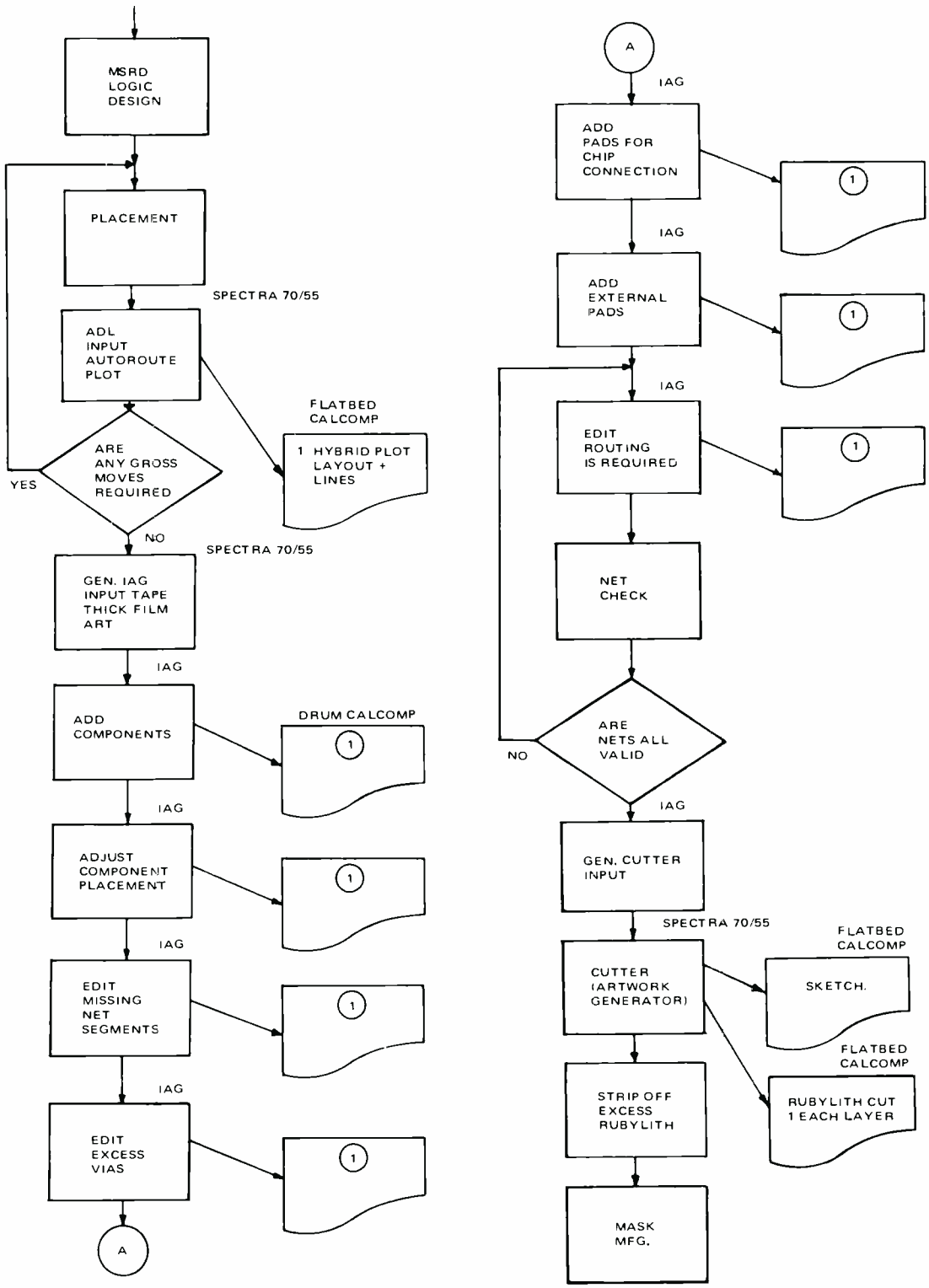


Fig. 5 — MSRD automated design system for modules (ADS-M).

Design automation for multilayer thick-film hybrids

R.F. Kolc

Manual design and layout techniques are clearly too costly and inefficient to meet the needs of present-day complex hybrid circuits incorporating hundreds of interconnection points. This paper describes the variety of design approaches available, providing successive levels of automation to meet specific requirements of individual circuit designs.

THE TREND in hybrid microcircuits has been one of increasing density and higher operating speed for complex digital hybrids. This speed and density requirement resulted in the need to interconnect many LSI chips onto a ceramic substrate. Conventional manual design and layout techniques are rapidly becoming unacceptable because of the associated costs, elapsed times, and the general technical inferiority of the process on more advanced systems.

With the increased availability of LSI devices in bipolar, CMOS, and CMOS/SOS technologies, and the increased utilization of custom chips (with as many as 64 pads per chip), many hybrid with 10 or more chips may contain 500 or more points that must be interconnected. Manual design and layout techniques for these hybrids of this complexity become very inefficient, costly, and generally provide a design that is, at best, less than optimum. Literally, man-months of effort can be expended on the design and layout of one of these complex hybrids. By any reasonable standard, the utilization of manual techniques, even for simple hybrids, has become patently inefficient in comparison with design automation techniques.

To provide a better understanding of the MSRD Hybrid Design Automation System and the improvement it provides, this paper briefly describes a completely manual system, a modificaiton of the manual system by inserting a degree of design automation, and finally, a fully implemented automated system currently in use at MSRD.

Manual artwork system

The primary functions of the design and layout cycle for hybrids are:) to provide the artwork from which screens are manufactured for use in the fabrication of hybrids, and 2) to provide assembly information on the hybrid, and 3) to form the basis for documentation control.

Assuming one has gone through all the necessary design rule considerations prior to starting the layout of a hybrid (*i.e.*, establishment of substrate size, power dissipation considerations, resistor sizing, component sizes, *etc.*), a number of basic steps are required in the generation of the artwork, as delineated in Fig. 1.

Starting with a schematic for analog and RF circuits — or a logic diagram for digital circuits — a design is initiated

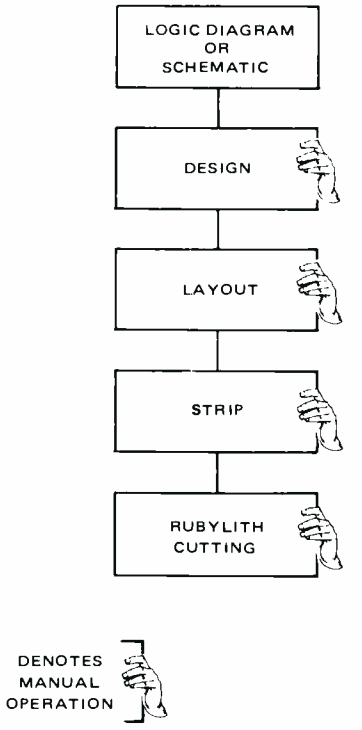


Fig. 1 — Major steps in manual generation of artwork.

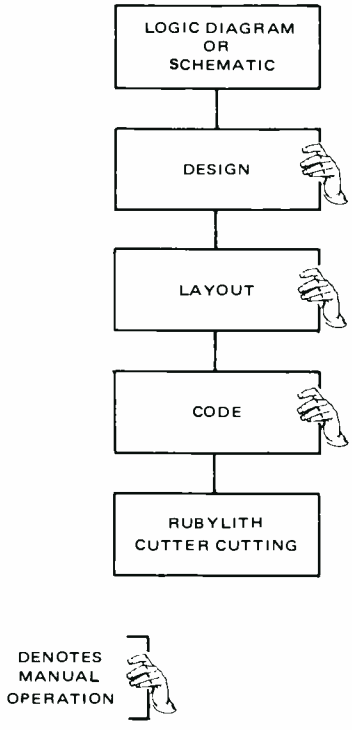
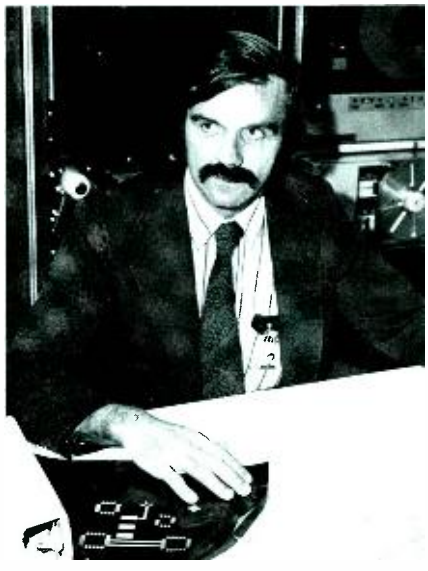


Fig. 2 — Manual artwork with automatic rubylith cutting.

Ronald F. Kolc, Leader, Technology Laboratories, Advanced Technology Engineering, MSRD, Moorestown, N.J., received the BSEE from Carnegie Institute of Technology in 1960, the MSEE from Drexel University in 1966, and an MBA from Drexel University in 1973. Since joining RCA in 1970, he has been actively engaged in the design, fabrication, and testing of hybrid microcircuits. He has also been involved in the implementation of interactive graphics techniques for use in the design, artwork, and documentation of complex thick film multilayer hybrids. Projects have included implemenation of a thick film facility capable of producing hybrids to the requirements of MIL-M-38510A and testing hybrids to the requirements of MIL-STD-883. Prior to joining RCA, Mr. Kolc was employed at Tele Dynamics, Division of Ambac Industries, in the capacity of section head in charge of Telemetry Products and Hybrid Microcircuits.



which will be concerned with component placement and interconnections. The initial design generally provides information on the number of conductor layers, line widths, and spaces. Normally, the design is laid out on gridded paper with a scale factor 10 to 20 times final size; centerlines on conductors are utilized to minimize the time spent in this phase. When the design appears to be satisfactory, a circuit layout is detailed using the proper line widths and spaces, on accurately gridded paper. In very complex designs it may be necessary to strip off each individual layer separately, *e.g.*, the first conductor, first dielectric, *etc.* This becomes necessary because the master layout with all the layers superimposed may be too complex to use for cutting the rubylith master. After the layouts are completed the rubylith artwork is cut on a light table using the stripped layers as masters.

Manual artwork with automatic rubylith cutting

The block diagram of this partially automated system is shown in Fig. 2. This system is essentially the same as the manual system shown in Fig. 1, except that the cutting of the rubylith becomes an automatic rather than a manual function. This automatic system is called CUTTER. To enter CUTTER, the layout is coded with commands designating directions of the cutting blades and the *start* and *stop* X-Y coordinates as well as line widths.

CUTTER provides many advantages over a manual system, particularly on medium to complex hybrids; it also provides a time and cost saving. For example, the system has the capability to do a repeat function. When a given pattern is repeated on the hybrid (*e.g.*, beam lead patterns, connector bonding pads, capacitor mounting pads), the program will cut this pattern, automatically, without coding of the repeated pattern. Prior commands can be restructured in rotated or mirror-image form for use in subsequent patterns, and other commands are available which have also proved useful in the generation of artwork.

Computer aided design

A significant improvement over the previous system is demonstrated by the system depicted in Fig. 3. With the aid of the interactive graphic (IAG) system, design and layout are generally accomplished together on an electronic pad with the results displayed immediately on a cathode ray tube. The IAG system, as structured for hybrids, uses system commands developed specifically for hybrids, and includes a library with virtually all the common hybrid elements (*e.g.*, standard beam lead patterns, conventional bipolar devices, chip capacitors, stretchable resistors, various line widths and spaces, standard *vias*, *etc.*). As an indication of the power of the system, it is feasible to construct a 32×32 inch hybrid with 16 levels and 1-mil resolution. For hybrids this appears to be more than adequate for many years to come. A simplified block diagram of the IAG/CUTTER system is shown in Fig. 4.

As mentioned above, a variety of library elements are called into the drawing by the appropriate system and hybrid commands. The library elements are interconnected, manipulated, moved, rotated, repeated, *etc.*, until the required design has been generated. In the design, the appropriate levels for conductors, dielectrics, resistors, and assembly information are assigned. These levels may be viewed singly, in any combination, or in their entirety. Accurate plots may also be made from the system onto a drum CalComp plotter for accurate checking. Some very significant features of this system are:

1) The design and layout are accomplished simultaneously. When the components are inserted and interconnected the layout is automatically complete.
2) Many iterations can be made very simply on the design to enhance producibility. For example, if a design could be enhanced by moving a group of elements and their interconnections by 10 or 20 mils, this change is a simple matter with the system. In the manual process, movements of this type are time consuming and expensive.
3) Design modifications are very easy to accommodate.
4) Process information can be included in the drawings because one of the 16 levels is generally assigned for assembly information. This assembly information automatically tracks the design and all subsequent modifications.
5) Design rules can be incorporated into the system during the construction of the library elements and by various system checks on the artwork. For example, if 10-mil lines are specified in the library a designer could not use a 6-mil line without consciously violating this rule.
6) Documentation - Much of the documenta-

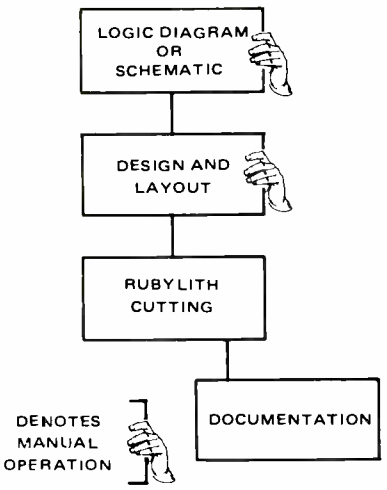


Fig. 3 — Computer-aided design.

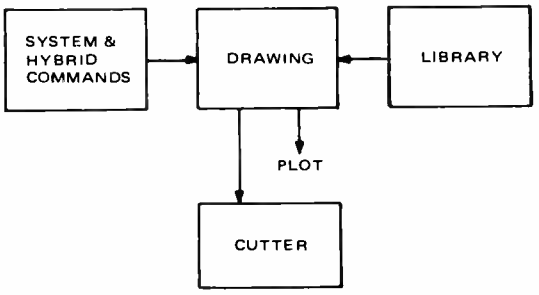


Fig. 4 — The interactive graphic CUTTER system.

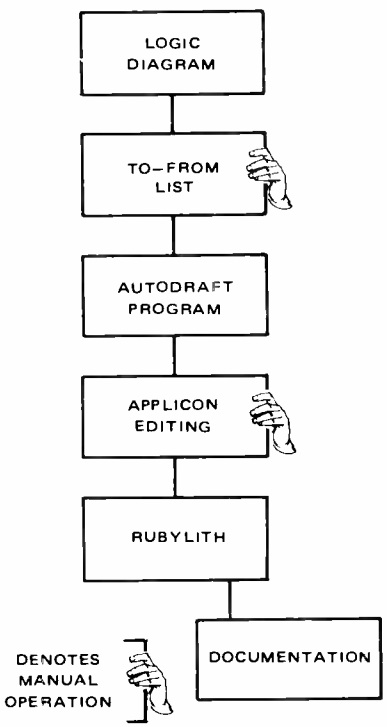


Fig. 5 — Fully automated design.

Fig. 6 — Hybrid circuit design by automated system.

tion is automatically available as a by-product of the design and layout phase. This subject is discussed in more detail in the next section.

7) Elapsed time and cost are significantly improved over manual approaches, by a factor of 3 to 1 in the generation of artwork and the documentation.

Documentation

In the first two systems described, all documentation must be generated manually except the rubylith masters, which are cut by the CalComp in the second system. The hybrid outline drawing and its parts list as well as the substrate assemblies and their parts list, must be available for inclusion in the documentaiton system (the substrate assemblies also include a drawing or a photo reproduction of each layer).

In the CAD system, standard RCA drawing formats are included as part of the library. When a design is complete, the RCA format is called from the library into the drawing, text is added by the system alphanumeric keyboard, and appropriate drawing numbers and revisions are assigned. Since each layer of the hybrid is available separately, this documenation requirement is available. The system is outputted onto the CalComp on high-quality reproducible paper for inclusion in the system.

Automated design

The logical extension of the design automation process has been to eliminate the design and layout phase on the IAG and to generate a fully automated routing system. Such a routing system is particularly useful for the design of complex digital hybrids with 500 or more interconnection points. The system developed as MSRD is shown in Fig. 5.

An example of a design generated by means of this system is shown in Fig. 6. The "to-from" list was generated from the original logic diagram. Component geometries and placement were assigned and the modified *Autodraft* program run. Hybrids, unlike printed wiring boards, are well suited to programs of this type because center-to-center spacing of conductors can be maintained even in the presence of *via* holes. Routing is orthogonal for adjacent layers in the program. The program will generally contain more *vias* than are required, and every change in line direction will require another *via*; editing on the IAG is utilized to eliminate these excess *vias*. After this editing, the design process follows the same procedure as the computer-aided system.

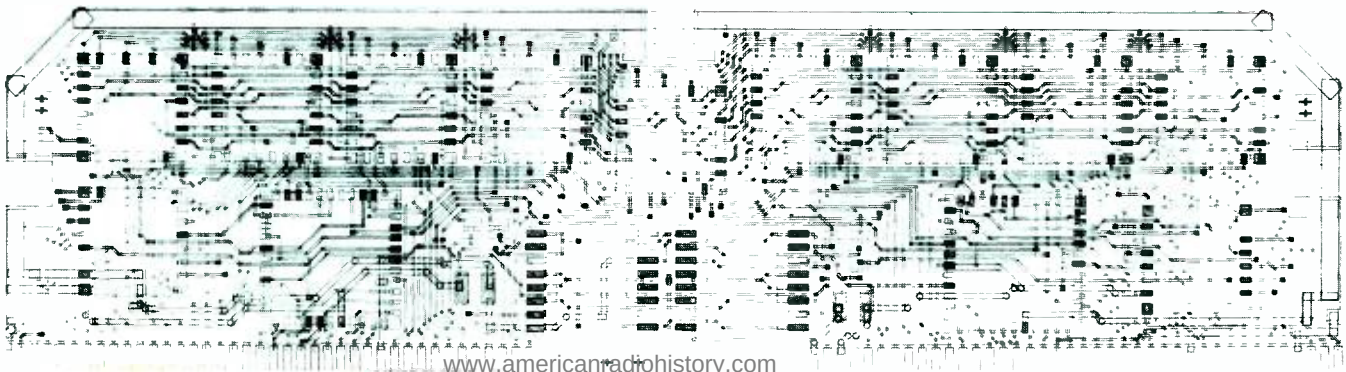
Large, complex hybrids

The layout of a very large substrate (5 × 1.4 inches) shown in Fig. 7 appears to be an indication of things to come. This hybrid contains 13 leadless hermetically sealed carriers, of which two are 48-pin devices and eleven are 28-pin devices. In addition, the design contains two 16-pin flatpacks, five chip capacitors, and five chip resistors. The design, performed on the IAG, contains 435 interconnection points, with two interconnect levels and a single dielectric level.

Conclusion

There is a continuing, indeed growing trend toward higher speed and complexity in hybrid microcircuits. The cost-effective fabrication of these hybrids in reasonable quantities demands stringent control of nonrecurring design and documentaiton costs. Without design automation programs the manual effort and the resultant elapsed time would result in prohibitive costs on many designs. The designer, then, must initially select the approach that best suits his immediate and long-term design goals, choosing either a computer-aided approach or the fully automated system on the basis of time and cost. In either event the use of design automation programs must increase as circuit complexity grows; otherwise the cost of traditional manual design techniques could compromise or even negate the effective application of hybrids.

Fig. 7 — Complex substrate design (actual size) performed on the interactive graphic system.



Laboratory automation in the Microwave Technology Center

Dr. B.S. Perlman

The Microwave Technology Center uses automation as a laboratory tool in several data-acquisition-and-control (DAC) and computer-aided-design (CAD) applications. Minicomputers are often appropriate as dedicated processors for real-time as well as non-real-time experiments. Multiprogramming characteristics of a disk operating system, operating as a Real-Time Executive (RTE), can be applied to run several tasks concurrently. Several important applications to microwave-device characterization are given with emphasis on the unique capabilities afforded by dedicated real-time computer control. Areas investigated include network characterization and analysis; infrared scanning microscopy; power transistor load contouring; capacitance-voltage measurements; pulsed dc and temperature characterization; and numerous other parametric and functional testing capabilities.

Abbreviations

ANA	Automatic Network Analyzer
ASCII	8-bit code (e.g., paper-tape format)
BTSS	Basic Time Sharing System (RCA)
CAD	Computer-aided Design
COSMIC	Computer Optimization of Simple Microwave Integrated Circuits
CPU	Central Processing Unit
D/A	Digital-to-Analog Converter
DAC	Data Acquisition and Control
DMA	Direct Memory Access
DUT	Device Under Test
EBCDIC	8-bit Code (e.g., IBM mag-tape format)
FET	Field-effect Transistor
FMGR	File Manager
GNAP	Generalized Network Analysis Program
GNOP	Generalized Network Optimization Program
IRSM	Infra-red Scanning Microscope
LADN	Ladder Network Analysis Program
MIC	Microwave Integrated Circuit
MTC	Microwave Technology Center
NTSS	New Time Sharing System (RCA)
RTE	Real-Time Executive
SYMOD	System Modelling Program
TDOS	Total disc operating system (RCA-Univac)
TTL	Transistor Transistor Logic

AUTOMATION in the microwave laboratory evolved from the need to perform highly complex design and measurement tasks usually too difficult to perform manually. In many measurements, automatic testing techniques provide self calibration by systematically controlling system hardware. This facility mathematically removes intrinsic hardware errors to accurately characterize a device under test. Beyond increased acquisition speed and decision-making resources of a computerized control system, the capabilities of laboratory instrumentation may be greatly extended to perform increasingly more difficult tasks.

In computer-aided design (CAD) of networks using active and passive circuit elements, the exclusive use of analytical methods may be supplemented by introducing measurement data to represent certain complex elements. The latter approach to CAD has evolved as a necessary procedure in the design of microwave integrated circuits (MICs) and other microwave components where it is often essential to eliminate the need for empiricism and redesign by accurately predicting circuit performance prior to circuit fabrication. The need for accurate characterization data has led to the use of automatic test equipment such as the ANA to assist in the measurement process [The Automatic Network Analyzer (8540 series) is manufactured by the Hewlett-Packard Company.] The results of using such a hybrid CAD procedure (*i.e.*, combining mathematical simulation with discretely measured device data) have proved successful in numerous applications. The use of interactive CAD disciplines becomes an exciting possibility as algorithmic advances and increased machine speeds permit the designer to utilize his computerized resources more effectively. The latter capability becomes a practical tool in those cases where computing costs are minimal permitting the use of interaction as a teaching as well as a design tool.

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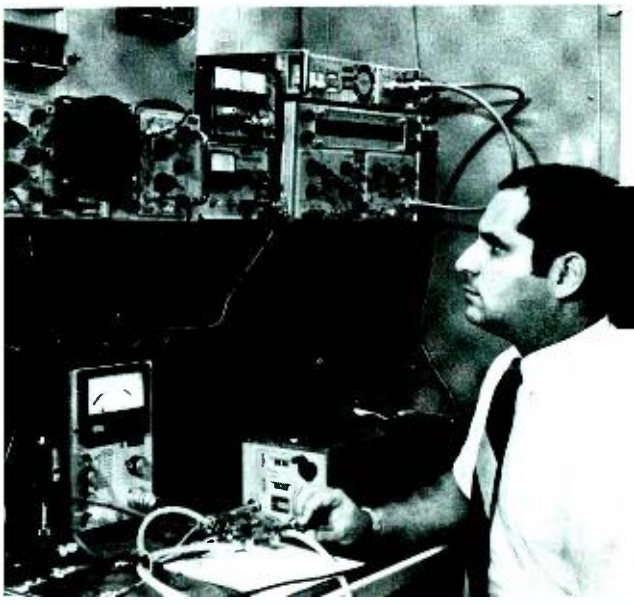
Barry S. Perlman, Microwave Technology Center, RCA Laboratories, Princeton, N.J. received the BEE from the City College of New York in 1961 and the MSEE and PhD in Electrophysics from Brooklyn Polytechnic Institute in 1964 and 1973, respectively. From 1961 to 1968, he was a member of the staff of the RCA Advanced Communications Laboratory in New York City, becoming a senior member of the technical staff in 1966. In June of 1968 he joined the Microwave Technology Center as a member of the technical staff, where he is presently working on the microwave applications of active GaAs semiconductors, computer-aided design (CAD) and advanced measurement techniques. He has published more than 30 technical papers in the field of solid-state devices, microwave networks and CAD; he submitted fifteen patent disclosures and holds four patents and has two pending. In 1969 he received an engineering achievement award for his part in the development of advanced microwave devices, and in 1970 he was a recipient of the RCA Laboratories Outstanding Achievement Award for a team effort in the development of wideband GaAs transferred electron amplifiers. Dr. Perlman is a member of Sigma Xi, the IEEE, PGMTT, PGED, and NYSSPE. He is a member of both the Technical Program Committee and Editorial Staff of the Microwave Theory and Techniques Group of the IEEE. He is also chairman of MTT-1, a committee concerned with advancing computer practices with the same IEEE group.

Many of the advantages of laboratory automation have been realized in the Design and Measurement Automation Laboratory at the Microwave Technology Center in Princeton. By employing a variety of computer-controlled measurement devices, operating at frequencies from dc to microwaves, accurate data can be obtained on both active as well as passive devices and components, linear and nonlinear high power as well as small signal, for use with CAD routines or for component characterization and evaluation. In each case, the use of computer control provides for measurement repeatability



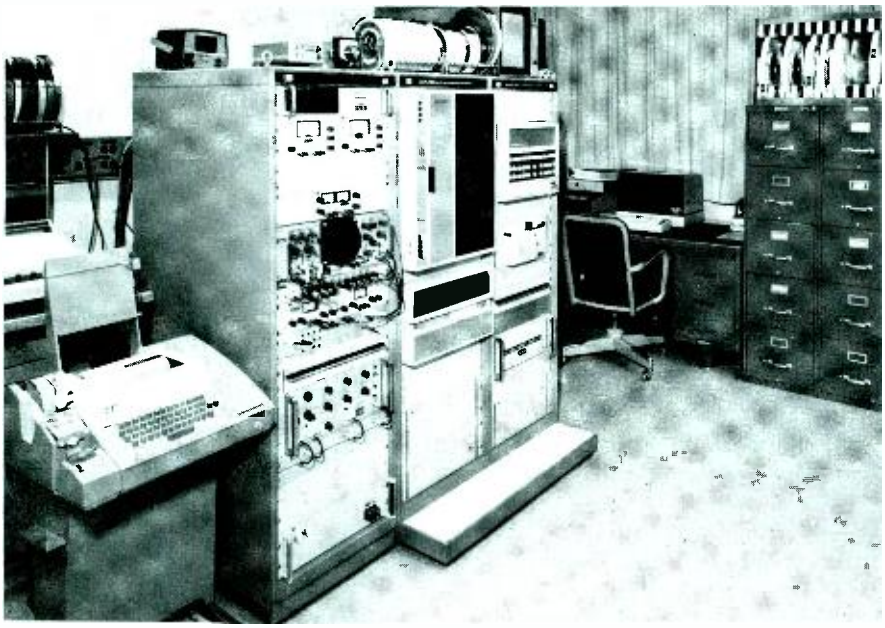


Fig. 1 — Realtime executive (RTE) computer system.

and systemization, allowing the use of self-calibration techniques to characterize the system hardware which, in turn, extends the measurement capability improving accuracy while maintaining a relatively high speed for the overall acquisition procedure. The advantage of using powerful data reduction algorithms to process the data allows the end user to achieve an effective interpretation of results, in either tabulated or graphical format.

Measurement automation

The Microwave Technology Center (MTC) in Princeton maintains a comprehensive automatic measurement facility designed to provide a high level testing capability for discrete devices as well as system components. This facility offers a new approach to solving numerous classical measurement problems, while providing the means to develop more imaginative procedures than would have been attempted before.

The automation laboratory at MTC has acquired or developed several important systems and pieces of apparatus that provide a wide range of automatic measurement capabilities. The major items are described below:

Real time executive (RTE)

The primary purpose of this computer system is to provide for the simultaneous real-time execution of a variety of automatic measurement tasks. Several programs are able to operate concurrently, each program executing during a time that the central processor is not being used. In particular, the use of equipment such as an automated IR microscope or a contour mapping load pull apparatus — where parameters such as voltages, currents, powers, or temperatures may be computer controlled while analog readings are digitized and recorded — does not necessarily preclude the concurrent operation of unrelated measurement and computer-related tasks. Individual programs are scheduled for execution in accordance with previously assigned priorities. Low priority programs acquire CPU time when the higher priority tasks are suspended waiting for an event to occur. This flexibility is achieved by subdividing main memory into a foreground area (for use in real-time applications) and a background area (for use in batch applications).

The RTE system hardware (Fig. 1) is basically an HP-2100S 64-kbyte (16-bit word) microprogrammable minicomputer. All floating point arithmetic routines, including double precision, are microcoded in hardware, providing computational execution speeds that are 5 to 20 times those of conventional mini's. Coupled with an interface I/O extender unit, a total of 45 I/O slots are provided for use in interfacing peripheral equipment. An HP-7900 dual cartridge disk system with a 5 Mbyte storage capacity operates interactively with the CPU, providing for real-time program swapping in addition to randomly addressable program and data storage. An IBM-compatible 9-track magnetic tape transport is available for very large data storage. Translation software to convert EBCDIC to ASCII and vice-versa allows compatibility with large-scale systems. In this way, software and data can be transferred between the RTE and other computer systems. Paper tapes, such as those produced by a teleprinter, can be read at high speed (500 cm/s) by means of a photoreader. Operator control is achieved primarily by means of several terminals distributed throughout the laboratory. Large volume printing is performed by a 360-line/min. line printer (Versatek 1600A) which also serves as a high speed, high resolution matrix plotter (0.75 in./s paper speed). More conventional line plotting is provided by an X-Y 10-in. × 15-in. digital plotter. Both plotters are supported by an extensive software library, allowing them to provide alphanumeric symbols in addition to line and point plotting. Auto scaling software is available for labeling of graphs.

The RTE is a multilingual system, supporting several languages by providing individual compilers for Fortran IV, Fortran II, Algol and Assembly. Several routines written in any combination of these languages may be intermixed and loaded as a single program. With this flexibility, sophisticated data processing is possible, using a high level language like Fortran for computation while using code-optimized mnemonic assembly for instrument and other DAC routines (*e.g.*, drivers). In all cases, programs may be readily edited using a fully interactive text editor. An extensive file-management (FMGR) routine is initiated either from the operator's console or dynamically under program control. Disc data files are created conveniently, allowing for extremely rapid writing speed under DMA control.

The important features and advantages of the RTE as a laboratory DAC system are:

a) *In the foreground*:

1) A real-time interactive multiple measurement and control capability.
2) Priority scheduling of interruptable programs.
3) Programs requesting a non-buffered I/O transfer are suspended, I/O is initiated, and execution of next highest priority schedule program is begun. When the I/O transfer is

complete, RTE reschedules the suspended program for execution.

4) A swapping feature is available which allows disc resident programs to be suspended and swapped out of core (unless I/O suspended) if a higher priority program needs the area.

5) Integrity of all programs and associated data is maintained.

6) The operator retains ultimate control over his program through the terminal keyboard, allowing programs to be turned on or off, suspended or status checked.

b) *In the background*:

1) Unlike real-time disc resident programs, background programs are *never* swapped; they occupy core until completion or abortion. [Using a new revised operating system (RTE-II), background disk resident programs may also be swapped. In this way, multiple compilers, editors, loaders and other batch operations may be executed concurrently. A new Batch Spool Monitor is also available for continuous job stream operations.]

2) Batch processing capability may be applied to data reduction and report preparation concurrent with running of foreground DAC programs.

3) On-line editing, compiling and loading of new programs can be accomplished while the real-time area is handling external events.

4) There is an extensive file management system for organizing and systematizing files. The FMGR package provides easy-to-use access methods in the form of operator commands entered from a terminal or dynamically from a user program.

Several important peripheral devices, interfaced with the RTE, lend themselves to the purpose of control and data acquisitoin. Among these are: a high-speed low-level A/D with a 50-channel analog scanner with a switched encoding time of 1 ms, a bidirectional 12-bit multiprogrammer with 15 channels of I/O, and a high speed digital communication link to an 8-channel coupler controller. The latter device is used to extend the RTE's control over a completely independent subsystem which itself contains numerous DAC functions. Among these are 10 channels of high-level analog scanning with an autoranging A/D, a digital capacitance bridge, a 16-bit digital voltage source (± 100 V), a 10-V staircase generator linked to a set of VCOs operating from 1 to 18 GHz, a programmable network analyzer, a 15-channel multiprogrammer with a variety of relay, and D/A and TTL logic outputs.

The HP-6940-multiprogrammer interfaced directly with the RTE is used to control a variety of instruments. A 16-bit bidirectional word transfer to and from the CPU provides interfacing as many as 240 12-bit logic cards. Four of the 16 bits are used to address up to 15 cards in any of up to 15 possible logic frames. The importance of this device is the fact that a wide variety of specialized hardware can be distributed and controlled via *one* I/O slot in the computer main frame. Each of the 12-bit devices may be addressed independently under software program control while using only one instrument I/O driver routine.

For the purpose of instrument control, the present RTE multiprogrammer provides:

1) 12-bit D/A converters which each provide an output range of ± 10 V with a resolution of 5 mV.

2) 12-bit TTL/DTL logic for use with 5 V, 12 V or any voltage up to 30 V.

3) 12 independent relays on each of several boards.

4) Stepper motor control through the use of a programmable pulse train at a preset frequency.

5) An event sense capability for use in comparing an external 12-bit logic state with a programmed condition.

For use in interfacing instruments and devices requiring more than ±10 V or additional drive power, each of the D/A's may be interfaced to a power operational amplifier. This capability extends the available output to a peak value of ±100 V at 1 A for repetition frequencies up to 20 kHz. This combination is used effectively to drive VCOs, provide constant current or voltage for device characterization, control servos and control temperature.

Specific applications and use of the RTE are described in reference to several of the DAC and CAD routines which follow.

Computer-controlled IR scan and temperature mapping apparatus

A new approach to acquiring the temperature profile of relatively small planar electronic devices has been developed. The technique provides for automatic emissivity calibration and 2-dimensional scanning using a Barnes infrared microscope interfaced with, and under the control of, the RTE computer system. Calibrated temperature data is presented graphically on a hard-copy plotter.

The present infrared scanning microscope configuration (Fig. 2) consists of a Barnes IR microscope with an optical resolution of 1 to 1.5 mils focused onto a precision mechanical substage which is programmable with regard to X-Y position as well as surface temperature. By incorporating a pair of stepper motors linked via micrometers to the substage, a mechanical position resolution of 1/16 mil step is readily achieved. The substage includes a heating element coupled to a temperature controller with an externally programmable set point. Radiometer signals are converted from analog to digital code and stored in an appropriate data file.

By providing the means for automatic DAC for an otherwise *manual* IR scanning microscope, the task of recording accurate thermal maps on numerous devices has been simplified dramatically. The primary advantage of this approach over noncomputerized methods is the ability of the computer to compensate for variations in material emissivity by systematically recording radiation from the unknown structure at several preset

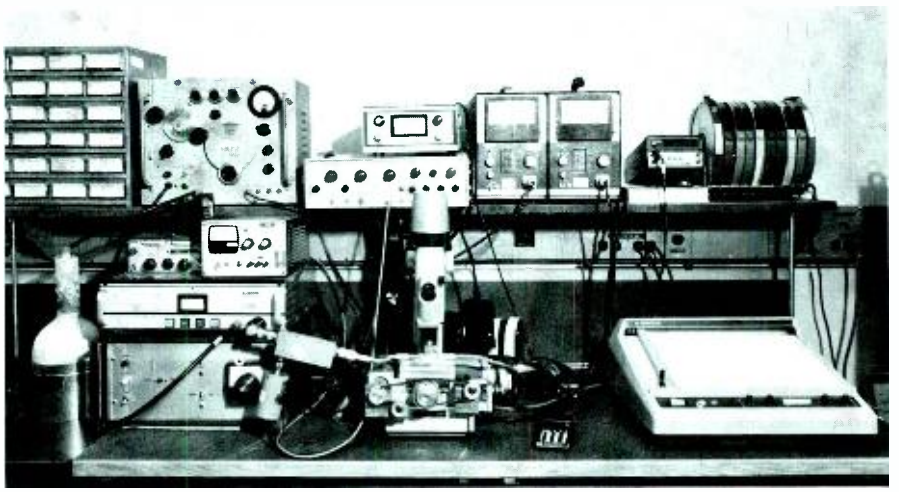


Fig. 2 — Computer-controlled infrared scanning microscope (IRSM) and temperature plotting system.

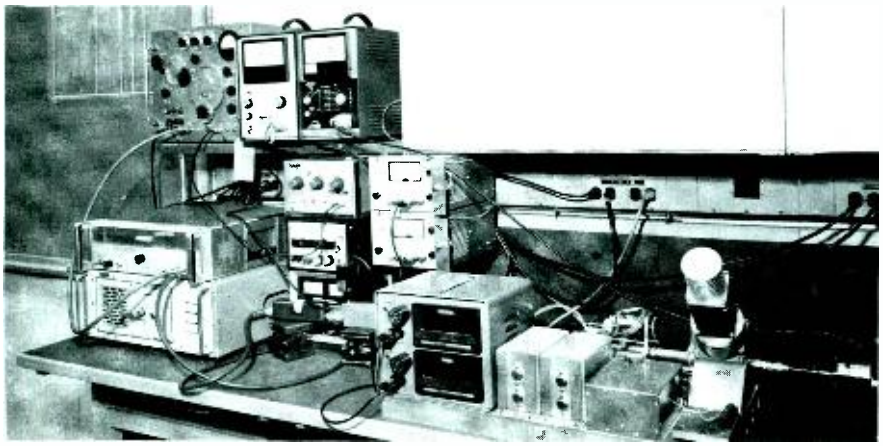


Fig. 3 — Automatic power-load contour mapping (load-pull) apparatus.

calibration temperatures. Radiation from a 'live' device can then be corrected for emissivity variation and converted to actual temperature and plotted automatically. A conservative estimate of the accuracy of this method is ±1°C.

The IRSM apparatus is remarkably effective in the study and diagnosis of microwave power transistors as well as LSI circuits. Under the influence of both bias and rf excitation, the dynamics of power sharing between different cells of a bipolar device can be studied. Discrepancies in the thermal distribution can be correlated with efficiency degradation. In many cases, thermal moununiformity can be attributed to mechanical failure (*i.e.*, heat sinking, bond failure, etc.). Likewise, thermal imbalance can be detected for a poor design and corrected by a redesign of the ballasting networks. The IR data derived from a scan of a device characterized by a well-balanced power and thermal distribution has also been shown to be an excellent indication of device reliability.

Automatic load-contour mapping (load-pull apparatus)

An electronically controlled impedance tuning apparatus has been developed for use in the large signal characterization of microwave power transistors. In effect, the automatic impedance tuner is used to present a variable load (or source) impedance to a device under test for the purpose of characterizing the nonlinear device as a function of its circuit impedance. Operating under computer control, the tuning apparatus is presently being used to map contours of constant power and efficiency on a Smith Chart for dynamic matching of both the input and output circuits associated with a microwave power transistor amplifier, operating with either *cw* or *pulsed* excitation. Other applications where the apparatus could be used are

1) Noise figure contouring of low noise transistors,
2) Load sensitivity (pulling) measurements, and
3) Pulsed oscillator characterization (Trapatts).

Basically, the impedance tuning apparatus consists of a precision GR-874 slotted air-line which has been modified by adding a pair of dielectric slugs which can be located electromechanically. A pair of servo motors, operating under the control of the RTE, are used to position the slugs with respect to each other and with respect to the input reference plane associated with the slotted line. In effect, both the magnitude and phase of the load reflection coefficient may be varied under computer control by utilizing a pair of D/A converters contained in the RTE multiprogrammer to drive two high-gain servo amplifiers which in turn drive the position of the slugs. A photograph of the complete assembly is shown in Fig. 3.

The present configuration was designed to operate over the 1 to 4 GHz band with minimal power limitations. For this reason, the use of power and frequency sensitive microwave control devices was avoided in favor of the electromechanically tuned air-line. The power limitation of the load used is largely responsible for the power limitation of the tuner as an assembly. The restriction of frequency is strictly due to the mechanical range over which the pair of slugs could be moved to effect a desired VSWR. In principle, the same air-line could be readily modified to operate at frequencies through X-band.

By including the electronically controlled tuner in a microwave test system capable of measuring the directional power characteristics of a working transistor amplifier, either pulse or cw, the information necessary to derive power-load contours can be obtained. The multichannel A/D, interfaced with the RTE, is used to measure, digitize, and record analog data from the servo control system as well as from the microwave hardware such as any of the power meters or power supplies. By monitoring both the servo command and feedback voltages, a closed-loop control system has been realized.

Conceptually, the method used for power transistor amplifier characterization is an extension of the technique of tuning the active device in a working circuit to a specific operating condition, removing the tuning network, and using a network analyzer to characterize the tuner alone. The primary objective of maintaining a condition of constant power or efficiency over a range of load impedances sufficient to produce a closed contour on a Smith Chart can be an overwhelming task when attempting to use manual techniques. The same effort performed at several discrete frequencies can be prohibitive. To reduce the measurement time, a self-optimizing search algorithm controlled by the RTE was developed which permits the automatic plotting of constant power output contours directly on a Smith Chart. These graphs proved to be a very effective tool in the characterization, design, and evaluation of nonlinear microwave circuits operating under large-signal conditions. A detailed description of the acquisition procedure, use and interpretation of the power-load contours has been published.[1]

Capacitance-voltage measurement

A popular measurement technique for characterizing semiconductor materials and devices involves the acquisiton of capacitance-voltage data. To facilitate the required task, a digitally controlled ± 100 V voltage source with an accuracy of 0.01% has been interfaced with a 1-MHz Boonton digital capacitance bridge. Both instruments are interfaced with the coupler/controller which in turn can be controlled by either the RTE or by an HP 9100B/9125B desk calculator/plotter combination.

A variety of programs has been written to control the measurement apparatus. Many of these programs are specifically written for the 9100B where raw C-V data can be plotted on either linear or logarithmic scales. Similar programs are available for use with the RTE with the the advantage of speed and programming versatility. The latter programs permit the measured data to be interpolated using a 3-point Spline technique in order to obtain derivative information. This data is then used to derive depletion width profiles for the impurity distribution of abrupt junction devices.

Automatic waveform sampling technique and its application to pulsed I-V measurements

To perform pulse-height and other related measurements, a Tektronix 3S2 3T2 dual-channel 25-ps sampling scope was interfaced to the RTE. By addressing a 0 to 10-V D/A loacted in the multiprogrammer, the external horizontal input may be used to position the sampling gate with respect to its time position. The A or B channel vertical output can then be digitized and used to record the time-dependent amplitude of the displayed waveform. The technique is primarily used to record pulse height information, although it is applicable to the Fast-Fourier analysis of arbitrary waveforms.

At the present time, the primary use of the automated sampling scope is in the pulsed I-V characterization of power transistors. This type of measurement, although tedious to perform manually, can be greatly simplified by letting the RTE control the pulse amplitude output from a generator, and measure the I-V response of the device. By utilizing relatively low duty factors, the resulting information is independent of the effects of internal device heating and can therefore be used effectively in developing diagnostic models.

A pulsed I-V test set has been developed for the purpose of determining the β vs. logI_c and V_{be} vs. logI_c characteristics of microwave power cells. A photograph of this equipment, interfaced with the RTE in Fig. 4, is included just to the left of the RTE. In its present configuration, a high impedance op-amp probe is used to monitor the pulse voltage across the input of the transistor, while a current probe is used to monitor the collector current (I_c). Both signals are digitized for various programmed levels of pulse excitation. A series input resistor connected betweeen the input signal source and the device is used to sample base current (I_b). The programmable horizontal time position is used to determine the base-line offset voltage and compensate the apparent pulse amplitude for this error. A precalibration routine is provided for accuractely determining the amplitude of the incident pulse with respect to a maximum value of 50 V (1 A). All mesurement data is written to mag tape for latter processing and or plotting.

The aforementioned I-V measurement technique has been used to acquire parametric β,I_c and V_{be} pulsed data for the LA 8407 transistor over an ambient temperature range from 25 to 140°C. Saturation and other nonlinear effects were clearly observed.

High-power reflection-type network analyzer

The high-level characterization of either 1-port or 2-port devices is feasible by using a network analyzer which includes a reflectometer capable of operating at the required power level. For this purpose, a manual analyzer was interfaced with the appropriate microwave and data acquisition hardware. The latter system provides a programmable 0-to-81dB attenuation of the incident power up to at least 20 W in 1-dB steps. This facility may be controlled by either the 9100B calculator or the RTE. The advantage of the RTE is its ability to provide a hardware calibration and an extended data-reduction capability. A photograph of some of the equipment used for this experiment (exclusive of TWTAs) is shown in Fig. 5.

By determining the terminal immitance variation with respect to the rms terminal voltage across the input of a device under test, one may utilize this information in the modelling and simulation of the performance of a variety of nonlinear circuits. A case in point is the characterization of negative conductance devices such as Gunn, Impatt, tunnel diode, *etc.*, for use as reflection type amplifiers or oscillators. By determining

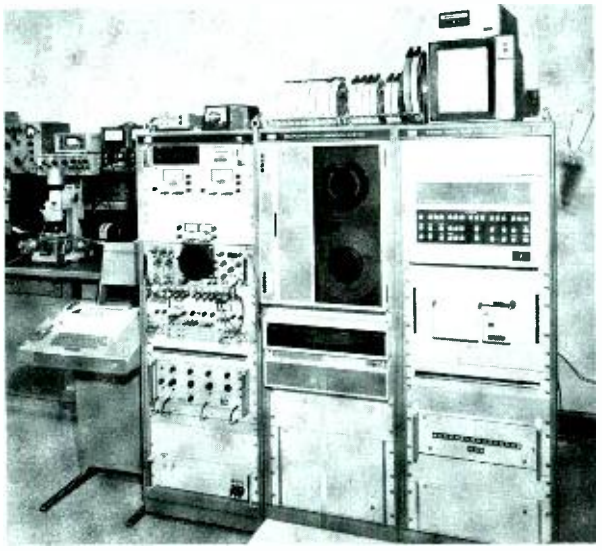


Fig. 4 — Pulse and waveform sampling test set (left) is shown interfaced with the RTE system (right).

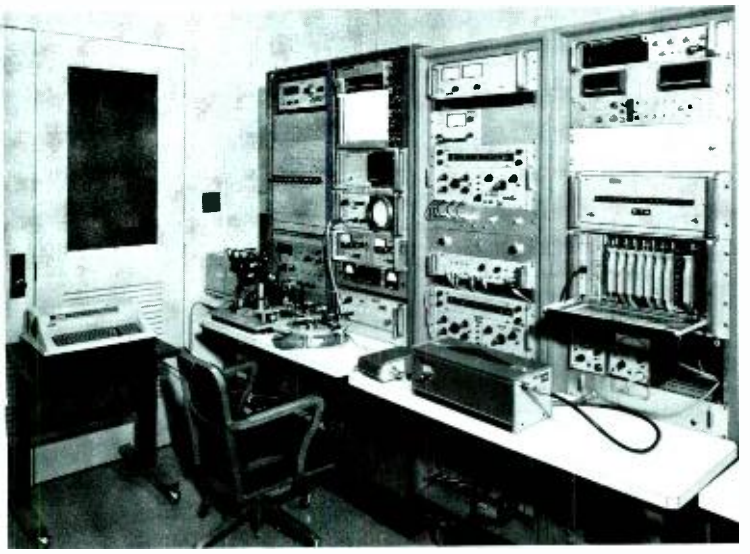


Fig. 5 — General-purpose A/D subsystem. Capacitance-voltage test set is at the extreme left end. High power network analyzer and frequency generators are in the middle. Computer interface hardware is at the extreme right.

the variation of the negative conductance $|-G|$ and susceptance B with respect to the mean squared terminal voltage $|V|^2$, one can compute the effective power available, $|V|^2 G$, at resonance. In this manner, the required circuit components needed to sustain optimum efficiency and performance may be determined.

Another application, although not requiring the same order of power level, is the characterization of mixer performance for use in tv receivers. By detemining the input impedance of a tv mixer as a function of the applied signal, one may more effectively model a tuner front end in order to simulate tuner performance.

By rearranging the reflectometer hardware it has been possible to extend its high-power measurement capability to two-port devices. This capability provides for the characterization of amplifiers, *etc.*, with regard to the nonlinear behavior of gain saturation and a.m./pm conversion.

General-purpose dc measurements

A facility for programming numerous power supplies and other D/A related devices is available. Voltages as high as ±100 V may be controlled with accuracies between 0.01 and 0.1%. Currents as large as ± 1 A can be similarly controlled. Larger power levels are achievable by using appropriate amplifiers. By taking advantage of the various plotting routines and equipments available, one may readily acquire I-V and other dc-related data rapidly and efficiently in graphical form, on a wide variety of devices.

Automatic network analyzer (ANA)

By combining a dedicated 16-kbyte minicomputer with a network analyzer and its associated hardware, rapid and accurate measurements can be performed on a variety of microwave devices. The primary purpose of the dedicated mini is to systematize, control, and process data derived from a relatively complex test system, in order to increase measurement accuracy and speed significantly over that afforded by a manual configuration. In its present configuration, the ANA operates independently without the RTE. Ultimately, a high-speed digital communications interface will be established between the two systems. This capability will permit both program and data swapping, thereby increasing the capabilities of the ANA.

A photograph of the ANA is shown in Fig. 6. Using a programmed frequency stimulus, from 0.1 to 12.4 GHz, the ANA test set characterizes the device being tested by a set of S-parameters or by any other linearly related parameters. By means of a self-calibration technique, hardware and interconnection errors are virtually eliminated, thereby achieving high measurement accuracies.

Once measurement data is acquired and corrected for errors, it may be displayed graphically on a refreshed scope display or written in tabulated format in terms of a wide variety of parameters.

One of the outstanding features of the ANA is its ability to mathematically process its corrected measurement data. Aside from its ability to convert *S*-parameter data into other forms (*i.e.*, *Z*, *Y*, *H*, *etc.*), it can also adjust data to be consistent with any set of reference planes. This facility is valuable when calibration fixtures are not readily located at the desired reference planes, which is often the case with semiconductor devices where physical constraints make fixturing difficult. By means of accurate fixture characterization techniques, equivalent line lengths may be determined between the calibration planes and those of the unknown device under test. Rapid rotation to a known position, or to any other, if facilitated by dynamically displaying the rotated vectors on the real-time display.

Computer-aided design

Numerous CAD programs have been written for use with a variety of computers, ranging from desk calculators to time-shared NTSS and batched TDOS.[2,3] With the implementation of the RTE, most programs have been rewritten to take advantage of the RTE's data management system and unique peripherals. Specifically, measurement data acquired through the use of the RTE's automatic DAC system can be stored on tape or disc and retrieved for interactive design, simulation and optimization of the performance of microwave networks employing the tested device(s). Some of the more general CAD programs used at MTC and their applications are described below.

COSMIC

This program, familiar to most for use with either BTSS or NTSS, has been extensively revised for use with the RTE. Representing our most complex network analysis and optimization program, COSMIC permits virtually any form of microwave network topology to be assembled and analyzed mathematically. An autosearch algorithm provides design iteration capability by assisting the user in his decision process by automatically tailoring constrained element values to satisfy some performance criteria. Coupled with discrete measurement data, this program provides a powerful tool in the realization of complex microwave circuits through the use of interactive computerized performance analysis simulation.

FET

This program is used to model equivalent lumped circuits for field-effect

Fig. 6 — Automatic network analyzer (ANA).

transistors. Lumped-element values specified by the user are assembled into a circuit model which includes a controlled current source. The *S*-parameters set for this network is calculated and compared against the *S*-parameter set measured on the ANA.

GNAP

This program provides a general purpose network analysis for 1-port ladder networks which are comprised of distributed as well as RLC lumped elements. It may be run on any of the minicomputers at MTC, including the 9100B desk calculator. Its main feature is a hard or soft copy plotting option allowing the user to interact more directly with the program. In addition, it supports a feature for representing complex termination by a mathematical power series expression determined from a least-square fit to measured data.

GNOP

This program, which includes GNAP as a subprogram, provides a modified grid search algorithm to automatically seek an optimal network to satisfy a specified reflection gain (return loss) condition. Its primary attribute is convenience and simplified formatting, with plotting, for use in the design of ladder-type impedance equalizers.

LADN

Representing one of the more popular network analysis programs, LADN is actively used to model 2-port ladder-type microwave networks. One of its special features is the use of measured *S*-parameter data to represent active and other real devices. An interpolative feature allows the network frequencies to be specified in between the measured *S*-parameter data. *S*-parameter data files can be created, maintained or retrieved.

SYMOD

The most recent addition to MTC's network analysis repertoire, SYMOD is designed to model system type networks. Its primary role is to utilize *S*-parameter data files derived by LADN or specified by the user, and assemble them to represent a complete network of up to 120 elements at up to 16 frequencies. The representation of complex source and load terminations is not facilitated by most CAD programs. The significant feature of SYMOD is its ability to 'split' a network into as many as three contiguous subnetworks and derive the S-parameter, terminal immittance, and transducer gain data for each subset. In this manner, any network can be analyzed with respect to the source and load impedance presented by its terminating networks. By determining the voltage gain to a specific reference plane, relative to the generator, nonlinear effects can be predicted. By including a voltage dependent load, such as in the form of measured data for a mixer, realistic design information (*e.g.*, tv tuner front end) may be obtained. In this manner, tradeoffs in overall system response may be determined.

These programs represent present CAD capability at MTC. Many other programs, including data acquisition and instrument control routines, mathematics packages for curve fitting, root extraction, smoothing and derivative extraction, fast Fourier transforms, *etc.*, are also available.

New automation projects and future plans

It has already been demonstrated that automation can dramatically influence our ability to perform experiments by controlling instrumentation and by acquiring, processing, and interpreting data. Coupled with the use of CAD techniques, these capabilities can be remarkably effective.

New applications for laboratory automation are being considered with particular regard to taking advantage of the RTE system. Some of these are related to ongoing experiments. The following are examples:

- Effort is being directed at improving the IR scanning algorithm to allow for an extrapolation of emissivity calibration data to higher operating temperatures, circumventing the need to heat the device undergoing test to those temperatures. In addition, pulsed IR measurements will be made possible by modifying the existing hardware and interfacing it with the sampling data acquisition system.
- A redesign of the load-pull apparatus is underway, with effort directed at using a more reliable and accurate stepper-motor indexing system coupled with an improved and more flexible slug configuration. The new design will permit measurements from 500 MHz through X-band. Another type of electronic tuner is planned for use at lower frequencies. The latter tuner will be used for both noise and large signal characterization of VHF devices.
- Process control applications requiring the real-time capabilities of the RTE are under development. The RTE has been interfaced with an ion-milling system and used to monitor the dc characteristic of the device being milled and control parts of the process. The feasibility of automating a Silane deposition system for epitaxial growth is being studied. The implications of a successful venture into these areas is obvious.
- A tv-tuner test set is planned which will provide for computer controlled channel selection. L.O. and preselector tracking, in addition to other tuner characteristics, will be measured on-line.
- Several specialized uses of the RTE have been developed by non-MTC staff. These include testing and diagnostics on CMOS and ion-implanted MOS devices with emphasis on the flexibility, speed and accuracy associated with the RTE.

Many of the applications of the RTE extend into product development areas, permitting concepts developed at MTC to be considered for possible use in the factory. By exploiting the advantages of the computer resources at MTC, numerous cost-effective applications requiring a systemized approach to testing and control can be developed.

Acknowledgment

The successful acquisition, adaption, and utilization of minicomputers in the Microwave Technology Center is the result of the imagination and innovative thinking of a team of researchers. Prime factors in the conception, realization, and application of many of the capabilities described in this paper are the multidisciplinary talents and dedication of J. Cusack, F. Sechi, S. Perlow, G. Theriault, and W. Schroeder. The author is also indebted to F. Sterzer and E. Belohoubek without whose cooperation and foresightedness the implementation of an automation laboratory would not have been possible.

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Display control/storage and retrieval equipment for tactical military use

P. T. Frawley | E. H. Miller

The Tactical Information Processing and Interpretation (TIPI) System (WS-428A) is a land-based system that can be transported by mobilizer, truck, helicopter, aircraft, and ship. The system is designed to increase the capability, improve the timeliness, and increase the accuracy of intelligence information by automating certain combat intelligence tasks. The Display Control/Storage and Retrieval (DC/SR) segment of TIPI consists of shelter-mounted equipment, computer software, trained personnel, information, intelligence data and facilities. This segment is designed for use by the United States Marine Corps and the United States Air Force, and will interface with other segments of the TIPI System and other existing field systems. The prime contractor for the development models of the DC/SR segment is the System Development Corporation, Hampton, Virginia. RCA's Government Communications and Automated Systems Division ir Burlington, Massachusetts, is the equipment system integrator.

E.H. Miller, Mgr., Advanced Programs, Government Communications and Automated Systems Division, Burlington, Mass. received the EE in 1952 through the cooperative program of the University of Cincinnati, and has completed numerous graduate level courses at the Universities of Pennsylvania, California, and Northeastern. He joined RCA in 1947 as a cooperative student working in advanced development. As a Development Engineer, Mr. Miller worked on electrostatic storage devices for automatic-track-while-scan systems, and the application of semiconductors to digital computers, telephone multiplex equipment, and was Project Engineer on a classified high-speed digital data communication system. Mr. Miller was Leader of the design and development of the Display Information Processor for BMEWS. He also had responsibility for BMEWS data processing equipment at NORAD and SAC installations. Mr. Miller later had project management responsibility for the RCA 604 High Speed Arithmetic and Control Unit. Mr. Miller was also responsible for application studies of the PACCS-ADA and TIPI-DC/SR Systems. He is currently responsible for conceptual studies of tactical and strategic operations and intelligence data processing requirements. Mr. Miller is a member of IEEE, ACM, Sigma Xi, Old Crows, and is a Registered Engineer in Ohio.

P. T. Frawley, Mgr., TIPI Project, Government Communications and Automated Systems Division, Burlington, Mass. received the BA in physics and mathematics from St. John's University in 1952 and the MS in physics from Drexel University in 1957. Mr. Frawley has been employed by RCA since 1952 and his assignments included design and development of precision navigation systems for the Navy and Air Force. Subsequent project engineering responsibilities included the TALOS control computer and monitor console subsystems, the BMEWS detection radar data takeoff and missile impact predictor subsystems and satellite attitude and translation control and guidance equipment. He was project Engineering Leader for the attitude, translation, and descent engine control equipments for the Lunar Excursion Module and Program Manager on the Airborne Data Automation project. In his present capacity as TIPI Program Manager, he has responsibility for assuring that all contractual requirements are met. He is a licensed Professional Engineer in Massachusetts.

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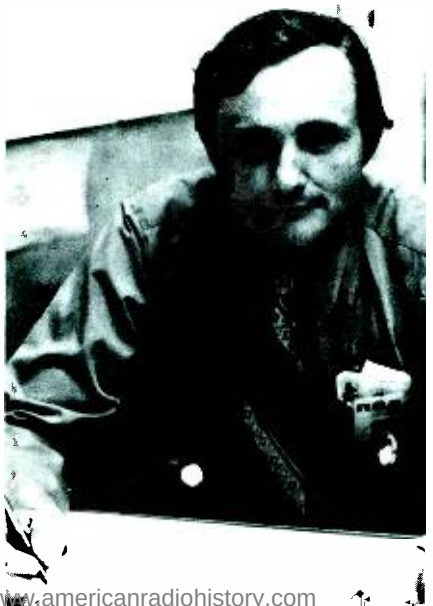


SUCCESS in tactical warfare depends greatly upon knowledge of the friendly and enemy situation. This situation information includes identification, location, movement, and time of report on each military unit or vehicle. The high-speed mobility of today's tactical weapon systems adds a critical time factor which can grossly alter the situation status in a relatively short period of time. A mass engagement can involve thousands of items that must be tracked almost continuously. The old manual methods employing pencils, paper, and maps are no longer adequate to keep intelligence data-base information up to date.

To solve this problem, RCA is implementing an automated system to assist the intelligence analysts in their enormous task of keeping the tactical intelligence data base up to date. This automated system — the Display Control/Storage and Retrieval (DC/SR) Segment of the Tactical Information Processing and Interpretation (TIPI) System WS-428A — provides each of up to 23 intelligence analysts with a Query Response Unit (QRU) which enables him to retrieve various categories of information from a 2.4 billion bit data base with the aid of a large central processing computer. To provide this capability, RCA's Government Communications and Automated Systems Division developed a system which can be rapidly deployed and used in the tactical field environment, and which rivals the size of some of the largest information storage and retrieval systems found in the non-military environment.

Setup of the DC/SR segment of the TIPI system is shown in Fig. 1. In general terms, the DC/SR segment performs the following functions:

- DC/SR segment management, including logging and journalizing
- Intelligence analysis and data base management
- Threat assessment and objective area planning
- Targeting and target data analysis
- Defense situation analysis
- Collection management and evaluation
- Basic intelligence and summary reporting

The flow of information within the DC/SR segment is shown in Fig. 2. The equipment is divided into the functional areas of communications, non-digital

materials and automatic data processing, as shown in Fig. 3.

Configuration

The TIPI DC/SR segment is configured in a set of 20-ft-long, 8-ft-high, 8-ft-wide shelters arranged as shown in Fig. 1. Interior views of four basic types of shelters are shown in Fig. 4. The USAF configuration consists of eleven shelters, with three basic shelters for automatic data processing, random access memory, and communications equipments. Also, there are six intelligence analyst station shelters and two non-digital shelters. The USMC configuration consists of seven shelters: the same three basic shelters as the USAF, three intelligence analyst station shelters, and one non-digital shelter.

The interface between the DC/SR segment and other elements is via the communications shelter (Fig. 4d). It provides the capability to handle digital data, teletype, and voice information. Security is maintained for all three types of information and, in addition, there are clear voice interfaces. Within the TIPI system, interfaces are provided to the Imagery Interpretation, the Image Processing, and the Tactical Electronic Reconnaissance Processing and Evaluation segments. There are also interfaces with

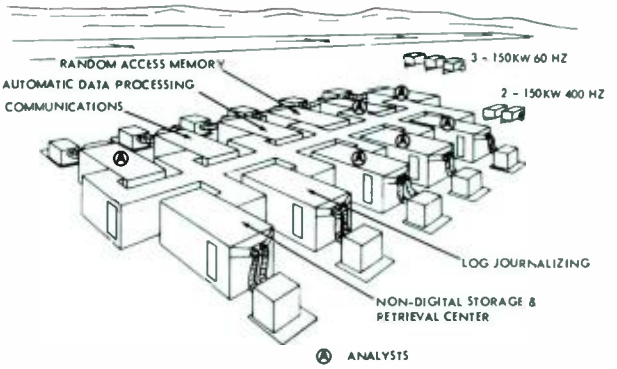


Fig. 1 — Plan view of the Display Control/Storage and Retrieval segment of the TIPI system.

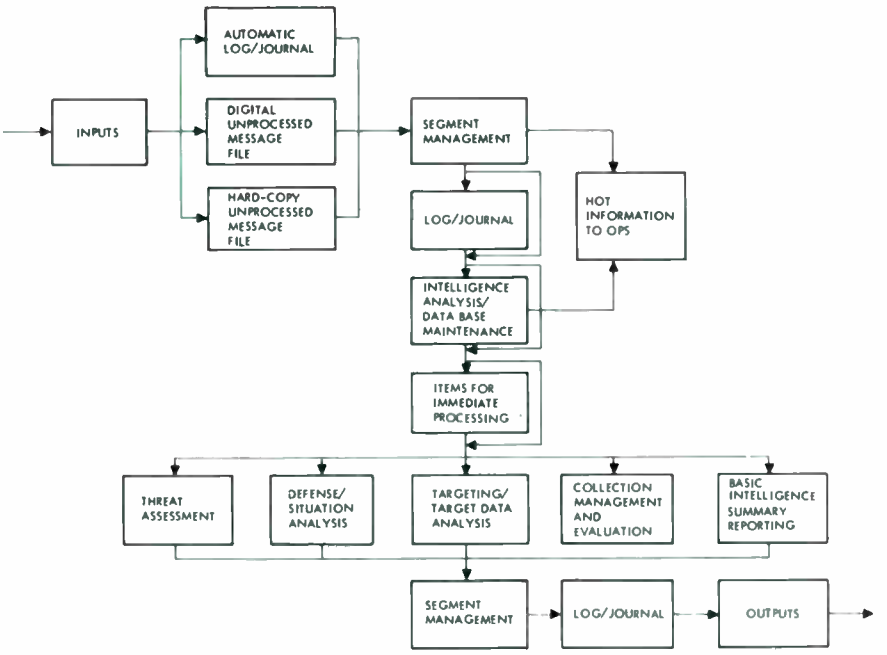


Fig. 2 — Flow of information within the DC/SR segment.

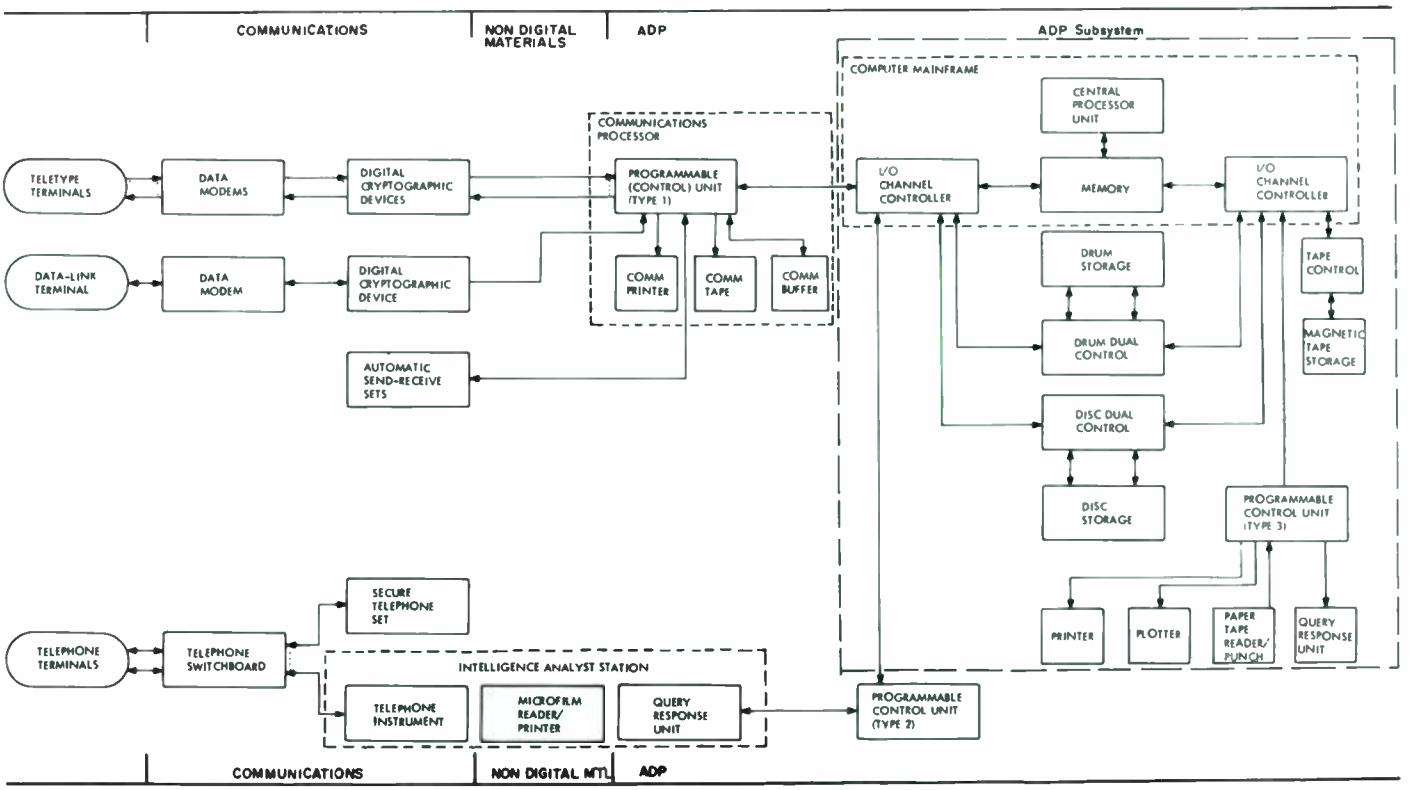


Fig. 3 — Relationship of DC/SR functional areas (prime items).

a. Automatic data processing.

b. Random access memory.

c. Intelligence analyst station.

d. Communications.

Fig. 4 — Inside views of the DC/SR shelters.

wing remote terminals. External to TIPI, there are interfaces with the following systems:

- Naval Intelligence Processing System
- Marine Tactical Command and Control
- Command Reconnaissance Technical Group
- Tactical Air Control System
- Battlefield Information Centers Battlefield Information and Control Centers
- Military Intelligence Battalion, Aerial Reconnaissance Support
- RFDCOM Command and Control System
- Weather Observing and Forecast System

The digital data and teletype messages are processed by the telecommunications and teletype control subsystem which includes a programmable control unit, a disc buffer, line printer, and a 9-track magnetic tape unit.

The data processing shelter (Fig. 4a) houses the AN UYK-7 computer mainframe with one central processor unit and two input output control channels, two 7-track and two 9-track magnetic tape units under control of a magnetic tape controller, and a paper tape reader, paper tape punch, line printer, query response unit, and a vertically mounted flat-bed plotter, all under control of a programmable control unit. The RAM shelter (Fig. 4b) contains two magnetic drums under control of a dual drum control unit and six disc units under control of a dual disc control unit.

In each of the six USAF and three USMC IAS shelters (Fig. 4c), there are three or four intelligence analyst stations under control of a programmable control unit, and a teletype automatic send receive unit. Each intelligence analyst shelter includes a query response unit, microfilm reader printer, and a black telephone. For the USAF, there are two shelters used for non-digital storage and retrieval while the USMC uses one shelter.

In addition to the eleven or seven shelters in a DC SR segment, there is a set of environmental control units, auxiliary power generation units, and pallets for transporting cables and other ancillary equipment.

A major consideration in the selection of the equipment for the DC/SR segment was that it was of available on-the-shelf design and could be integrated into the DC SR segment with virtually no risk. Some of the equipment was already qualified. Other equipment was an enhancement, expansion, or modification of equipment which had already been qualified. In some cases, the design had been proven in commercial systems and repackaging was required to meet the TIPI requirements.

Environmental qualification

RCA, as the system integrator, specified the complement of DC SR equipment to assure that when installed within the shelter, the configuration survive the complete range of military mobility hazards. An auxiliary environmental control system maintains the shelter environment within a range which enables the operators to work full shifts on a 24-hour a day basis. It also assures the proper operating environment for magnetic storage equipment which may be adversely affected by humidity. Humidification is provided where required so that a minimum of 20±5% RH is maintained.

RCA is responsible for assuring that the equipment will meet the specified performance and environmental capabilities in the configured shelters. RCA selected equipment which is used or is planned to be used on other Government programs. RCA or its vendors conduct the qualification testing either on the individual equipment or the equipment as installed in the shelter, or on a part of the equipment where appropriate. In all cases, the qualification testing is in accordance with Government approved specifications.

Reliability and maintainability

To assure that the selected equipment performs its mission in the military environment, RCA specified the reliability requirements in terms of apportioned mean-time-between-failure (MTBF).

For the DC SR segment, RCA performed a system availability analysis which is in consonance with the user requirements. Redundancy was applied on a selective basis only where required. Reliability data on the system is routinely collected and analyzed to monitor reliability performance, and to determine if product improvements are required.

The equipment has been designed for maintenance by military personnel in the field. Front and or top access is provided and modular construction enables rapid

repair by replacement of plug-in assemblies for 95% of the repair actions. Automatic error detection and fault isolation is provided by either hardware or software. Maintenance is enhanced by illuminated operational status panels, equipment status indicators, and auxiliary maintenance controls.

Compatibility

Compatibility is the capability of the system to perform its mission in the environment and in conjunction with other systems.

Electromagnetic interference and susceptibility requirements were a prime consideration in the design. The system is designed and integrated to provide proper shielding and bonding; e.g. shelters and interconnecting cables provide at least 70 dB shielding. All TEMPEST signal security requirements were met. TEMPEST, which is military terminology applied to the control of compromising electromagnetic emanations, dictates design criteria for minimizing unwanted radiation and requires a Government team to run a specific test. The TEMPEST test determines whether any intelligence data can be obtained from any detectable electromagnetic emanations.

Data security is maintained by eliminating compromising emanations, by data base access control via software and hardware lock-out techniques, and by the use of cryptographic devices. Several security control levels may be established and maintained to assure information security. Data destruct mechanisms are available to purge critical data from the system during routine moves or in emergency situations. Safe storage compartments are provided for the storage of removable media storage records and cryptographic keys.

Survivability and vulnerability requirements are a measure of systems compatibility with the hostile tactical environment. The system must survive the ordinary hazards of natural phenomenon such as weather, and the induced hazards due to transportation, operation, and maintenance.

Each requirement was established to suit the user need, and several alternatives are available. For example, sand bag revetments and roof covers can be substituted for armor plate against enemy small arm and mortar fire.

Interoperability is a measure of the system's ability to interface with other systems. The communications shelter is designed to comply with Military Communications Standards, American Standards for Communications Information Interchange Codes, and use standard cable connectors to assure compatibility with other military systems. Specific message formats, error detection and correction techniques, and other information interchange standards such as the Naval Tactical Data System (NTDS) standard are met by the basic equipment described here when operating under suitable control software.

Human engineering

The equipment was designed in conformance with Human Engineering Design Criteria. Human factors design requirements are employed to design operator interfaces which are anthropometrically correct for height, arrangement, illumination, legibility and accessibility. Environments are maintained which are conducive to good operator performance and reduced fatigue. Functional operator areas are designed to provide a low acoustic noise level to enable operators to maintain efficiency.

Safety is designed into the system such that no chassis or assembly with potentials in excess of 70 volts rms is exposed, and appropriate lightning protection is provided. There are no hazards from implosion, gases, acids, alkalis, or fumes. Equipments are designed for two-man carry wherever practicable.

Legibility of displays, printed pages, and control panels is designed to be compatible with normal vision and normal viewing distances in the ambient illumination provided within the shelter. Nonreflective cathode ray tube shields are used to reduce unwanted reflections. Control colors are designed to simplify operation and maintenance.

Accessibility is designed into the shelter configurations to assure operation and maintenance procedures. Equipment controls and indicators are located on the front of the equipments. External cable connection terminal boxes are located on the outside of the shelters to enable rapid set-up and dismantling operations.

Size, weight, volume, power

For the TIPI DC/SR segment, the 20-ft × 8-ft × 8-ft shelter was selected with a maximum gross weight of 10,000 pounds (less trailer). However, the equipment could also be installed in standard military shelters such as the 12-ft × 8-ft × 8-ft S-280 type shelter with a 5000-lb. maximum total weight for small helicopter lift and M-35 truck-mounted transport. Expandable shelters could also be provided which, in the transport mode, measure 12-ft × 8-ft × 8-ft, but when shelters are placed side by side, a floor area can be obtained which is 12-ft × 24-ft.

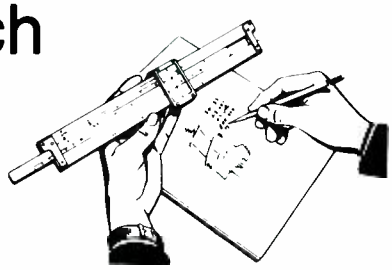
Shelter equipments are configured to keep the center of gravity within 2 ft of the horizontal center of the shelter, and below 4 ft above the bottom of the skids to prevent unbalanced loading and upset during handling.

To minimize size and weight, the equipment is designed to operate from 400 Hz, 208-volt, 3-phase, 4-wire power sources. Electrical overload protection is afforded by circuit breakers or fuses. EMI filters are provided to prevent conducted interference and susceptibility. Separate grounds are maintained for prime a.c. power neutral, signal, and chassis grounds. Signal and chassis grounds are connected in each equipment by a 3.16 kilohm power resistor to prevent shocks from a.c. power leakage. The effects of prime a.c. power interrupts are minimized by assuring nonvolatility of data on all storage and recording media.

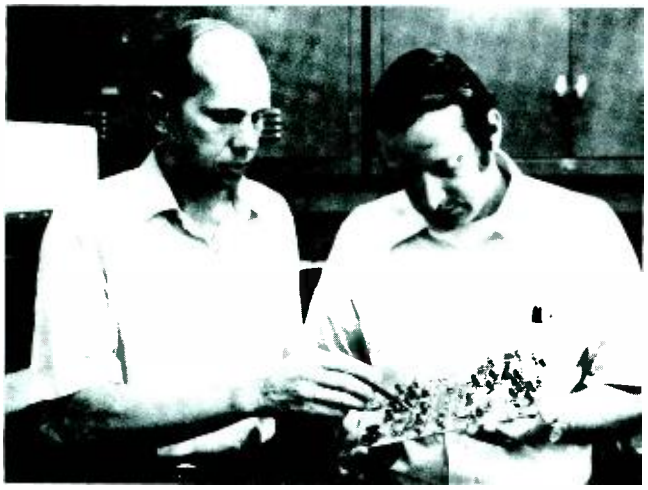
Status

As of April, 1974, the equipment for DC/SR segment of the TIPI system was tested and integrated into the four basic shelter configurations, which are completing their qualification testing. Segment-level test for reliability, maintainability, TEMPEST, and performance were performed in the first half of 1974. As of November 1974, the DC/SR segment of the TIPI system has successfully completed all of its hardware performance, environmental qualification, reliability, and TEMPEST testing. It was shipped to Langley Field, Virginia in July for functional software test.

Engineering and Research Notes



Light-pen editor for silicon storage tube display system



D.P. Dorsey| W.E. Rodda
RCA Laboratories
Princeton, N.J.

The storage target of a silicon storage tube consists of an etched SiO_2 insulating film on a silicon substrate for dividing the target into 600,000 insulated storage elements/cm^2 on the substrate. Scanning of the target with an intensity-controlled scanning electron beam, from an electron gun included in the silicon storage tube, selectively charges or discharges each element. In this manner, a full television frame of information can be written on the target and then continuously read out nondestructively to derive a video signal which may be displayed on a standard television monitor. When desired, the stored image on the substrate may be erased in no more than one-third of a second.

In the proposed system, a light-pen is coupled to the storage target substrate and beam control grid of the electron gun in such a manner that charge placed on the insulating surface is selectively removed. To do this under normal READ bias conditions, with the television monitor displaying the stored image, the light-pen is placed against the monitor's protective-faceplate and directed at any illuminated spot of the image. The circuitry shown in the drawing then generates a narrow pulse every time the electron beam of the monitor passes the "pick-off" point of the light-pen. Using the system's synchronizing system as X and Y coordinates, the light-pen signal can be spatially located with respect to the corresponding insulated storage elements of the target of the silicon storage tube. The light-pen signal is fed to the substrate and beam control grid through special networks to thereby remove the insulator charge from only the storage elements corresponding to the illuminated area selected by the light-pen. In this manner, the positive charge of such area is selectively removed by discharging the area to cathode potential.

The light-pen circuity consists of a photodetector followed by a preamplifier. The photodetector is a photo sensitive n-channel FET, chosen because of its speed and low-noise characteristics; the preamplifier is a high-gain video amplifier.

As the scanning electron beam of the monitor passes the photodetector of the light-pen, the photodetector generates a minute signal current. This low level signal is amplified by a high-gain wave-shaping amplifier, which has its gain controlled so that variations in absolute brightness of the raster illumination of the monitor produces substantially the same level of video output signal from the light-pen. The waveform of the output signal amplifier is dc-restored so that it is directly adaptable to TTL logic circuits.

TTL logic modules drive a specially developed beam-control network which incorporates a first amplifier and a target substrate biasing amplifier. The beam control network supplies only enough current to remove insulator charge. The substrate biasing amplifier determines the X-Y position of the sensed light-pen signal forwarded thereto. In addition, the substrate biasing amplifier increases the substrate bias of the target of the storage tube so that the selected incremental insulating area is positive with respect to the storage tube's cathode. The effect of increasing the beam current and adjusting the substrate's biasing will remove the selected insulator charge from the target elements corresponding to the areas of the monitor display contacted by the light-pen.

Reprint RE-20-4-24| Final manuscript received February 21, 1974.

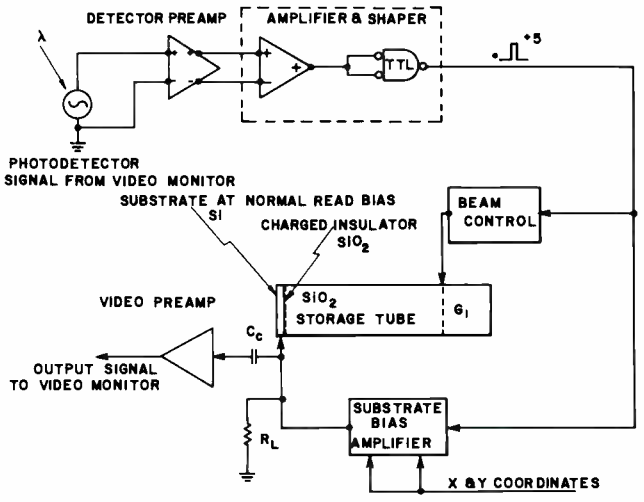


Fig. 1 — System block diagram.

Cutter-clincher for component leads

Eddy H. del Rio
Palm Beach Division
Palm Beach Gardens, Fla.

The apparatus described is for the high-speed cutting of wire leads of components assembled on a printed circuit board, and then if desired, for bending or clinching the leads against the board.

Referring to Figs. 1a and 1b, which show respectively side and bottom views of a cutter-clincher tool, it is seen to consist basically of two parts: a rotatable sleeve (10) surrounding a stationary rod (12), having on its free end a flange (14). The upper portions of both sleeve (10) and rod (12) are shown broken away. The power source for the rotating sleeve may be any conventional means (not shown), such as a high speed motor or pneumatic power source capable of rotating the sleeve approximately 500 to 1,000 rotations per minute in the direction indicated by the arrow (16).

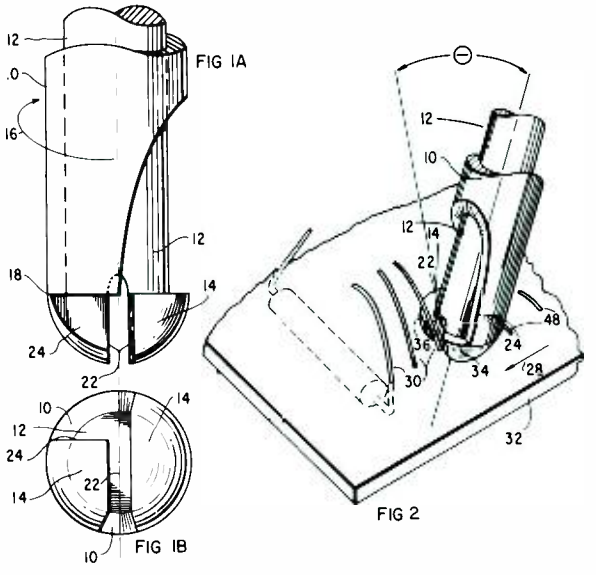


Fig. 1 — Cutter-clincher tool. **Fig. 2 — Operation of cutter-clincher tool.**

The sleeve has a portion removed extending circumferentially 180° near its base (18). A slot (22) in flange (14) extends normal to and through the axis of rod (12). In addition, almost one quadrant of flange (14) beginning at slot (22), is removed as illustrated at (24) in Fig. 1b.

Operation of the tool is shown in Fig. 2. While the sleeve is caused to rotate, the tool is directed as indicated by arrow (28), so that the leads in the printed circuit board pass serially into slot (22) of flange (14). Because of the shearing action between edge (34) of sleeve (10) edge (36) of flange (14), the leads are cut off. Then, because the tool is held so as to be tilted back from a position normal to the direction of travel of the tool at an angel θ [*i.e.*, toward cut leads (28)], edge (34) of sleeve (10) serially strikes the top portion of the cut leads (48), forcing them downward against the printed circuit board. Missing portion (24) of rod (12) prevents any interference between the leads and flange. If it is desired only to cut the leads and not bend them, the tool is held vertical to the printed circuit board (32) or tilted slightly forward (*i.e.*, toward the non-cut leads). In this manner, the edge does not strike the cut leads on the side of the flange opposite edge (36), and therefore, no bending action takes place.

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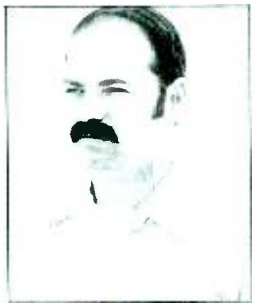
Remote accessory turn-on circuit

Paul Joseph Smalser
Parts and Accessories
Deptford, N.J.



The circuit shown in Fig. 1 allows a secondary device to be turned-on in response to a switch located on the primary device; the circuit requires no changes in the circuitry of the primary device. The primary device, for example, may be a stereo tape player for an automobile and the secondary device an auxiliary power amplifier for the tape player.

As shown in Fig. 1 the circuit includes a relay coil in series with the emitter-to-collector path of the transistor Q. The transistor normally is off. When the switch of the primary device is closed, current flows from the primary power terminal through a diode (14) to the primary device. The voltage which thereby develops across the diode is sufficient to forward bias the transistor so that current flows in its emitter-to-collector path and energizes the relay. This causes the relay contacts to close, allowing current flows to the secondary device. The resistor in the base circuit of the transistor limits the base current to a safe level.

An advantage of the present circuit, in addition to the one discussed above, is that the voltage across the diode is relatively small (approximately 0.7 V) so that the voltage available for the primary device remains relatively high and, for practical purposes, is unaffected by current variations in the primary device.

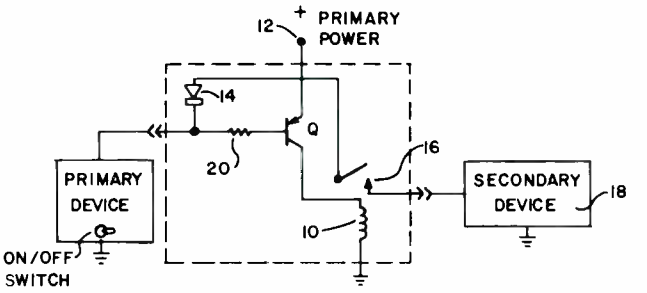
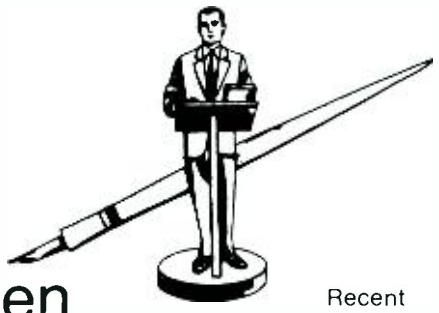


Fig. 1 — Remote accessory turn-on circuit.

Reprint RE-20-4-24| Final manuscript received February 20, 1974.



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FRITLESS METALLIZATION, Characterization of Thick Film — R.H Zein (SSD,Som) International Micro-electronics Symposium 10/21/74

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110 Earth and Space Sciences

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180 Management and Business Operations

organization, scheduling, marketing, personnel.

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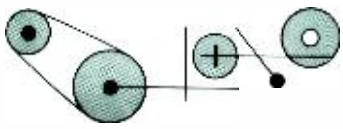

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Storage Tube Control Apparatus for a Telephone Image Transmission System — W.E. Rodda & D.P. Dorsey (Labs, Pr.) U.S. Pat. 3848084, November 12, 1974

Semiconductor Delay Lines Using Three Terminal Transferred Electron Devices — F. Sterzer (Labs, Pr.) U.S. Pat. 3848141, November 12, 1974

Broadband Trapatt Diode Amplifier — H. Kawamoto, E.L. Allen, Jr., S. Weisbrod (Labs, Pr.) U.S. Pat. 3848196, November 12, 1974

Microwave Transmission Line and Devices using Multiple Coplanar Conductors — R.E. Debrecht & L.S. Napoli (Labs, Pr.) U.S. Pat. 3848198, November 12, 1974

Vertical Convergence Circuits — R. Peter & H.P. Lambrich (Labs, Zurich, Switzerland) U.S. Pat. 3849696, November 19, 1974

Collision Prevention — D.S. Bond (Labs, Pr.) U.S. Pat. 3849782, November 19, 1974

Method of Densifying Silicate Glasses — W. Kern (Labs, Pr.) U.S. Pat. 3850687, November 26, 1974

Method of Making a Quasi-Monolithic Integrated Circuit Structure — C.P. Wen (Labs, Pr.) U.S. Pat. 3850710, November 26, 1974

Temperature Dependent Voltage Reference Circuit — C.F. Wheatley, Jr. (SSTC, Som.) U.S. Pat. 3851241, November 26, 1974

RCA Limited

Method for Rendering Cathode-Ray Tube more Resistant to Implosion and Product Thereof — R.B. Platt (Ltd., Midland) U.S. Pat. 3845530, November 5, 1974

Method for Separating Sulfide Phosphor Particles from Mixtures — B.B. McCue (Ltd., Midland) U.S. Pat. 3846328, November 5, 1974

Special Contract Inv.

Control Unit for an Antenna Rotator — R. Kaysen (Special Contract Inv.) U.S. Pat. D233668, November 19, 1974

Government Communications Systems Staff

Bagger Station or Similar Article — J.D. Hunt (GCS Plans & Sys., Cam.) U.S. Pat. D233496, November 5, 1974

Advanced Technology Laboratories

Label Writing Apparatus — R.E. Fulton (ATL, Cam.) U.S. Pat. 3839644, October 1, 1974

Graphic Systems Division

Optical Scanner Control System — R.M. Carrell (GSD, Dayton) U.S. Pat. 3848087, November 12, 1974

Computer Systems Division

Track Following Servo System — G.V. Jacoby & S.P. Woodsum (CSD, Marlboro) U.S. Pat. 3840893, October 8, 1974

Dates and Deadlines

As an industry leader, RCA must be well represented in major professional conferences . . . to display its skills and abilities to both commercial and government interests.

How can you and your manager, leader, or chief-engineer do this for RCA?

Plan ahead! Watch these columns every issue for advance notices of upcoming meetings and "calls for papers". Formulate plans at staff meetings—and select pertinent topics to represent you and your group professionally. Every engineer and scientist is urged to scan these columns; call attention of important meetings to your Technical Publications Administrator (TPA) or your manager. Always work closely with your TPA who can help with scheduling and supplement contacts between engineers and professional societies. Inform your TPA whenever you present or publish a paper. These professional accomplishments will be cited in the "Pen and Podium" section of the *RCA Engineer*, as reported by your TPA.

Dates of upcoming meetings —plan ahead

Ed. Note: Meetings are listed chronologically. Listed after the meeting title (in bold type) are the sponsor(s), the location, and the person to contact for more information.

FEB. 25-27, 1975 — **Computer Conference (COMPCON SPRING),** Jack Tar Hotel, San Francisco, Calif. **Prog info:** L. D. Amdahl, Compata, Inc., 6150 Canoga Ave., Woodland Hills, Calif. 91364.

MARCH 12-14, 1975 — **Particle Accelerator Conference,** NAP, NBS, APS, USAEC, NSF, Shoreham Hotel, Washington, DC **Prog info:** F. E. Mills, Nat'l Accel. Lab., POB 500, Batavia, IL 60510.

MARCH 17-19, 1975 — **First Annual Conference and Exposition,** American National Metric Council, Washington Hilton Hotel, Washington, DC **Prog info:** Lou Perica, American National Metric Council, 1625 Massachusetts Avenue NW, Washington, DC 20036.

MARCH 20-21, 1975 — **Seventh Annual Southeastern Symposium on System Theory,** IEEE Groups: Circuits and Systems Society, Computer Society, Control Systems Society, Systems, Man and Cybernetics Society, and Power Engineering Society, and School of Engineering, Auburn University, Auburn, Alabama and the School of Engineering, Tuskegee Institute, Tuskegee, Alabama, **Prog info:** H. Troy Nagle, Jr., Associate Professor of Electrical Engineering, Auburn University and Michael R. A. Erdey, Professor of Electrical, Tuskegee Institute.

APRIL 6-9, 1975 — **Southeastcon 75,** Region 3, Sheraton Ctr., Charlotte, NC **Prog info:** Frank Jenkins, POB 2178, Charlotte, NC 28242

APRIL 7-8, 1974 — **Rubber & Plastics Ind. Technical Conference,** IA, Akron, Ohio **Prog info:** R. L. Bock, B. F. Goodrich Co., 500 S. Main Street, Akron, OH 44311.

APRIL 8-11, 1975 — **IEEE INTERNATIONAL CONVENTION (INTERCON),** IEEE, Coliseum & Americana Hotel, New York, NY **Prog info:** W. C. Weber, Jr., IEEE Hdqs., 345 E. 47th St., New York, NY 10017.

APRIL 13-16, 1975 — **1975 Institute of Environmental Sciences Annual Technical Meeting and Equipment Exposition,** IES, Disneyland Hotel, Anaheim, CA **Prog info:** Robert Geminder, Technical Program Chairman, Mechanics Research, Inc.,9841 Airport Boulevard, Los Angeles, CA 90045.

APRIL 15-17, 1975 — **Advances in Automatic Testing Technology,** IERE, IEEE UKRI Section, et al, Univ. of Birmingham, Birmingham, England **Prog info:** Conf. Dept., IERE, 8-9 Bedford Square, London WC1B 3RG, UK England

APRIL 20-23, 1975 — **International Circuits & Systems Symposium,** CAS, Marriott Motor Hotel, Newton, Mass. **Prog info:** John Logan, Computer-Aided Analysis Dept., Bell Labs., N. Andover, Mass. 01845.

APRIL 21-23, 1975 — **Radar International Conference,** AES, Washington Section, Washington, DC **Prog info:** Merrill Skolnik, Naval Res. Lab., Code 5300, Washington, DC 20375.

APRIL 22-24, 1975 — **Reliability Software International Symposium,** C, R, ACM et al, International Hotel, Los Angeles, Calif. **Prog info:** James King, IBM Res. POB 218, Yorktown Heights, NY 10598.

MAY 3-8, 1975 — **Ceramic Resources - Challenges and Opportunities,** Nuclear Division - American Ceramic Society, 77th Annual Meeting & Exposition, Sheraton-Park and Shoreham Americana Hotels - Washington, DC **Prog info:** E. T. Weber, Program Chairman, Nuclear Division, Westinghouse Hanford Company, Box 1970, Richland, WA 99352.

MAY 4-7, 1975 — **Offshore Technology Conference,** TAB Oceanography Coor Comm. et al, Astrohall, Houston, Texas **Prog info:** OTC, 6200 N. Central Expressway, Dallas, Texas 75206

MAY 12-14, 1975 — **Electronic Components Conference,** PHP, EIA, Statler Hilton Hotel, Washington, DC **Prog info:** J. Barrington, DuPont Co., Electronic Pdts. Div., Wilmington, Del. 19898.

MAY 13-15, 1975 — **1975 Electrical and Electronic Measurement and Test Instrument Conference —** Ottawa Section of the IEEE, IEEE Group on Instrumentation and Measurement, The U.S. Commission I of URSI, Ottawa, Ontario, Canada **Prog info:** Mr. Richard F. Clark, Conference Chairman, National Research Council, Division of Physics, Montreal Road, Bldg. M-36, Ottawa, Ontario, K1A OS1, Canada.

MAY 19-21, 1975 — **Aerospace Electronics Conference (NAECON),** AES, Dayton Section, Sheraton Dayton Hotel, Dayton, Ohio **Prog info:** IEEE Office, 345 East 47th Street, New York, NY 10017.

MAY 28-30, 1975 — **1975 IEEE/OSA Conference on Laser Engineering and Applications,** Washington Hilton Hotel, Washington, DC **Prog info:** Dr. A. Stevens Halsted, Hughes Aircraft Company, P.O. Box 2999, Torrance, California 90509 Telephone: (213) 534-2121, ext. 247.

JUNE 9-11, 1975 — **1975 Power Electronics Specialists Conference, IEEE,** Los Angeles, Calif. **Prog info:** Program Chairman: Frank F. Oettinger, National Bureau of Standards, Electron Devices Section, Washington, DC 20234, (301) 921-3622.

JULY 1-3, 1975 — **Theory and Applications of Walsh Functions,** IEEE UKRI Section, IEE, Hertfordshire, England **Prog info:** P.D. Lines, Department of Electrical Engineering, The Hatfield Polytechnic, P.O. Box 109, Hatfield Herts.

JULY 14-18, 1975 — **Third Intersoicety Conference on Transportation,** ASME, Hyatt Regency Hotel, Atlanta, GA **Prog info:** Lawrence P. Green (General Conference Chairman) Assistant for Aeronautical R&D, Office of the Secretary (TST-7), Dept. of Transportation, 400 7th St., S.W., Washington, DC 20590.

Calls for papers —be sure deadlines are met

Ed. Note: Calls are listed chronologically by meeting date. Listed after the meeting title (in bold type) are the sponsor(s), the location, and deadline information for submittals.

MAY 7-9, 1975 — **Region Six Conference & Exhibit "Communications Technology"** (Region 6, Utah Section) Salt Lake City, Utah **Deadline info:** (ms) 2/7/75 **to** Stan Moss, Utah Biomedical Test Lab., Univ. of Utah, Salt Lake City, Utah 84112.

MAY 20-23, 1975 — **2nd ISPRA Nuclear Electronics Symposium** (IEEE, Nuclear and Plasma Sciences Society and North Italy Section) "Palazzo dei Congressi", Stresa, Lago Maggiore, Italy **Deadline info:** (abst) 1/25/75 **to** Prof. Luciano Stanchi, CCR EURATOM, 21020, Ispra (Italy).

MAY 21, 22, & 23, 1975 — **Thirteenth Symposium on Electron, Ion, and Photon Beam Technology** ((IEEE Group Electron Devices & EE, & AVS) Antlers Plaza Hotel, Colorado Springs, Colorado **Deadline info:** 12 copies of 200-300 (abst) 2/17/75 **to** Dr. R. F. W. Pease, Bell Telephone Laboratories, Murray Hill, NJ 07974.

JULY 20-25, 1975 — **1975 IEEE Power Engineering Society Summer Meeting** (PE) San Francisco Hilton Hotel, San Francisco, Calif. **Deadline info:** (ms) 2/1/75 **to** E. G. Lambert, Pacific Gas & Elec. Co., Rm. 2551, 77 Beale St., San Francisco, CA 94106.

SEPT. 22-24, 1975 — **Sixth International Congress on Instrumentation in Aerospace Simulation Facilities** (IEEE) Ottawa, Canada **Deadline info:** (abst) 4/25/75 & (papers) 7/18/75 **to** Dr. E. S. Hanff, General Chairman, 6th International Congress on Instrumentation in Aerospace Simulation Facilities, c/o National Research Council of Canada, Ottawa, Canada K1A 0R6.

SEPT 22-24, 1975 — **OCEAN '75** (Marine Tech. Society & IEEE Oceanography coordinating Committee) El Cortez Hotel, San Diego, CA **Deadline info:** (abst) 250 to 300 words 2/3/75 **to** OCEAN '75 Conference Program Chairman, Marine Physical Laboratory, Scripps Institution of Oceanography, San Diego, CA 92132.

NOV. 10-13, 1975 — **Third Joint Conference on Sensing of Environmental Pollutants** (IEEE) Las Vegas, Nevada **Deadline info:** (abst) 4/30/75 **to** Program Chairman, Dr. Henry Freiser, Dept. of Chemistry, Univ. of Arizona, Tucson, AZ 85721.

Engineering News and Highlights

Brandinger appointed Division VP, Television Engineering

Roy H. Pollack, Vice President and General Manager, Consumer Electronics, has appointed **Dr. Jay J. Brandinger** Division Vice President, Television Engineering. Dr. Brandinger had been head of Television Systems Research at RCA Laboratories since 1971.

Dr. Jay J. Brandinger has 23 years in Research and Development at RCA Laboratories in the fields of television and communications. He received the BEE from Cooper Union in 1951, MSEE and PhD from Rutgers University in 1962 and 1968, respectively.

In 1951 he joined RCA Laboratories in Riverhead, Long Island as a member of the Technical Staff working in the field of radio communications. In 1959 he moved to the RCA Laboratories in Princeton where he helped organize a research group to develop new computer data communication systems and techniques.

In 1966 he was made head of Systems and Display Research and was involved in the development of new television display and camera devices.

He is widely known in his field through publications, presentations, and active participation in national and international technical society meetings. He is Editorial Board Chairman of the Society of Information Display Proceedings and has chaired technical sessions at IEEE and SID Conferences. He holds three patents and has a number of others pending. He is also joint author of a chapter in a book on color television camera systems.

He has received three Outstanding Achievement Awards from RCA. He was elected a member of the Honorary Science Society Sigma Xi in 1962. He is a Senior Member of the IEEE and a member of the Institute of Mathematical Statistics, Society of Information display and the New York Academy of Sciences. He is listed in *American Men and Women of Science*, *Community Leaders of America*, and *Who's Who in East*.

First Acoustical Society Silver Medal goes to Olson

Dr. Harry F. Olson, retired Staff Vice President, RCA Laboratories, received the first Silver Medal of the Acoustical Society of America—"For his innovative and lasting contributions in microphones, loudspeakers, sound reproduction, and electronic music, his many publications, and his constructive editing."

Dr. Olson attended the University of Iowa, Iowa City, where he received the BE in 1924, the MS in 1925, the PhD in 1928 and the EE professional degree in 1932. He also received the honorary DSc from Iowa Wesleyan College, Mt. Pleasant, in 1959.

In 1928, he joined RCA as a member of the Research Department. After being placed in charge of acoustical research in 1934, he continued as head of RCA's acoustic research activities during the ensuing years, retiring as Staff Vice President, Acoustical and Electromechanical Laboratory, RCA Laboratories, in 1967. He continued as Advisor to RCA Laboratories until 1972.

An early and important contribution of Dr. Olson's long career was the development of the velocity and cardioid unidirectional microphones. He has also made pioneering contributions to loudspeaker development, improvement of phonograph pickup and recording equipment, underwater sound equipment and motion picture sound and reinforcement systems. In addition, he has guided and contributed substantially to such novel systems as the music synthesizer, speech processing and the phonetic typewriter.

Promotions

Solid State Division

A. Hom from Sr. Member, Tech. Staff to Ldr., Tech. Staff, Product Assembly, Equipment Technology Department (R.A. McFarlane, Som.)

Missile and Surface Radar Division

W. Mays, Jr. from Mbr., Engrg. Staff to Sr. Mbr. Engrg. Staff, Design Engineering TRADEX Press Site (T.A. Martin, Mrstn.)

J. Sivils from Mbr., Engrg. Staff to Sr. Mbr. Engrg. Staff, Real Time Computer Design (S. Steele, Mrstn.)

Staff announcements

RCA Limited

G. Denton Clark, President RCA (Canada) has announced the following appointments: **Morrell P. Bachynski,** Director, Research and Development Laboratories and **Roy A. Phillips,** Vice President, Consumer Relations.

RCA Service Company

Julius Koppelman, President, RCA Service Company has appointed **Joseph W. Karoly,** Division Vice President, Consumer Services.

RCA Global Communications, Inc.

Eugene F. Murphy, Executive Vice President, Operations has announced the following organization appointments: **James H. Muller,** Manager, Government Communications and Joint Network Management; **Allan E. Schwamberger,** Director, Regulatory Affairs and Operating Arrangements; and **Henri P. Touanen,** Manager, Telephone Operations and Administration.

John Christopher, Director, Satcom Project has announced the following appointments in the Satcom Project organization: **Peter Plush,** Manager, Launch Vehicle Integration and **Sydney Shrage,** Manager, Spacecraft Engineering.

Lee Wilson, Director, Computer Systems has announced the Computer Systems activity as follows: **Russell Blackwell** as Manager, Systems Programming and **Fred Danziger** as Manager, Computer Systems Customer Services and Leased Computer Operations.

Laboratories

Joseph H. Scott, Jr., Director, Integrated Circuit Technology has announced the appointment of **Norman Goldsmith** as Head, Integrated Circuit Process Research.

Government and Commercial Systems

Irving K. Kessler, Executive Vice President, Government and Commercial Systems has announced the appointment of **David Shore,** Division Vice President, Advanced Programs Development.

Commercial Communications Systems Division

Jack F. Underwood, Division Vice President, Mobile Communications Systems has announced the appointment of **George J. Mitchell,** as Manager, Mobile Communications Product Management.

Government Communications and Automated Systems Division — Camden

James M. Osborne, Division Vice President and General Manager, RCA Government Communications and Automated Systems Division has announced the appointment of **David A. Miller** as Manager, Sales, Advanced Systems and Techniques.

— Burlington Operations

Stanley S. Kolodkin, Division Vice President, Burlington Operations has announced the following appointments: **Ruth J. McNaughton** as Manager, Management Information Systems and Engineering Programming Services and **Joseph L. Gotthelf** as Manager, Radar Systems Marketing.

Eugene M. Stockton, Chief Engineer, Engineering Department has announced the organization as following: **Anthony Amato,** Manager, Products Engineering; **Richard T. Cowley,** Manager, Non-Electronic Test Engineering; **Donald J. Cushing,** Manager, Data Systems Engineering; **Richard J. Monis,** Manager, Automatic Test and Monitoring Systems Engineering; **Kenneth E. Palm,** Manager, Engineering Staff Operations; **Harry K. Schlegelmilch,** Manager, Radiation Systems Engineering; **Fred E. Shashoua,** Manager, Electro-Optical Systems Engineering; **Albert J. Skavicus,** Manager, Engineering Services and **Lawrence B. Smith, Jr.,** Administrator, Manpower and Budgets.

Astro-Electronics Division

C. S. Constantino, Division Vice President and General Manager has announced the organization as follows:

Wilbur B. Botzong, Manager, AED West Coast Operations; **Leonard V. Fox,** Manager, Operations Control; **C. Robert Hume,** Manager, Space Communications Systems; **Joseph L. Mackin,** Manager, Product Operations; **Warren P. Manger,** Chief Engineer, Engineering Department; **Philip J. Martin,** Director, Marketing and Advanced Planning; **Mark Sasso,** Manager, Program Management; **Abraham Schnapf,** Manager, Program Management; **Maurice G. Staton,** Division Vice President, Advanced Space Programs; **Warren W. Wagner,** Manager, Industrial Relations; and **Herman L. Wuerffel,** Manager, Product Assurance.

Consumer Electronics

Donald S. McCoy, Division Vice President, Development Engineering has announced the appointment of **H. Robert Snow** as Manager, Video Disc Operations.

Solid State Division

Carl R. Turner, Division Vice President, Solid State Power Devices has announced the organization as follows: **James A. Amick,** Manager, Materials and Processes; **Dale M. Baugher,** Director, Thyristor and Rectifier Operations; **Fred G. Block,** Manager, Mountaintop Operations Support; **Martin Geller,** Director, High Reliability & RF Product Operations; **Ralph S. Hartz,** Director, RF Module Programs; **George W. Ianson,** Manager, Operations Planning & Administration; and **James C. Miller,** Director, Power Transistor Operations.

Ben A. Jacoby, Division Vice President, Solid State Marketing has announced the appointment of **Arthur M. Liebschutz** as Manager, Special Product Marketing.

Harry Weisberg, Division Vice President, Solid State MOS Integrated Circuits has announced the organization as follows: **Donald R. Carley,** Manager, Microprocessors, **John A. Kucker,** Manager, Palm Beach Gardens, Start-up Operations; **Henry S. Miiller,** Director, MOS IC Products; **Norman C. Turner,** Director, COS/MOS IC Operations; and **Michael Zanakos,** Manager, Operations Planning & Administration.

Henry S. Miiller, Director MOS IC Products has announced the organization as follows: **Terry G. Athanas,** Manager, Circuit Design & Technology — NMOS & SOS and Acting Leader, Technology — NMOS & SOS; **George J. Waas,** Leader, Circuit Design — NMOS & SOS; and **Michael V. D'Agostino,** Manager, Marketing & Applications — NMOS & SOS.

Norman C. Turner, Director, COS/MOS IC Operations has announced the organization as follows: **Robert P. Jones,** Manager, Manufacturing — COS/MOS IC: **Thomas J. McInerney,** Manager, Production Control & Planning — COS/MOS IC; **Loren C. Weber,** Administrator, Production Control; **George A. Riley,** Manager, Market Planning — COS/MOS IC; and **Alexander W. Young,** Manager, Engineering.

Alexander W. Young, Manager, Engineering — COS/MOS IC has announced the organization as follows: **Edward C. Crossley,** Leader, Test Technology — COS/MOS IC; **Richard P. Fillmore,** Leader, Custom Circuit Design; **Robert C. Heuner,** Leader, Standard Circuit Design; **David S. Jacobson,** Manager, COS/MOS technology; and **Russel D. Knapp,** Leader, Product Support Engineering — COSMOS IC.

David S. Jacobson, Manager, COS/MOS Technology has announced the organization as follows: **Martin A. Blumenfeld,** Leader, Process Technology; **David S. Jacobson,** Acting Leader, Assembly Technology & Package Development; **William N. Lewis,** Manager, Model Shop — MOS IC; and **Bernard B. Levin,** Leader, Model Shop Engineering.

Howard honored as Distinguished Alumnus

William A. Howard, NBC Engineering Department, was honored recently by Howard Payne University as a Distinguished Alumnus.

Mr. Howard received the BA in Mathematics and Physics from Howard Payne in Brownwood, Texas in 1939 and did graduate work at Baylor University 1940-42. He joined the NBC Engineering Development Group in New York in 1946 and was involved with the development of studio and film camera chains used in New York and Washington during the late 40's. He was later involved in the engineering and installation of the original television facilities of NBC, Cleveland, Ohio and transferred there as Maintenance Supervisor of the television station in 1949. In 1952 he was made Supervisor of Technical Operations for WNBK and WTAM, NBC, Cleveland. With the transfer of NBC stations from Cleveland to Philadelphia in 1956, he was made Manager of Technical Operations for WRCV and WRCV-TV, Philadelphia. In 1960 Mr. Howard returned to NBC Engineering in New York as Manager of Technical Standards and Practices. At present he is a Senior Engineer in this department. He is a Senior Member of the IEEE and a Member of SMPTE. He has served as an Editorial Representative for the *RCA Engineer* since 1961.

Dr. J.S. Donal, Jr.

Dr. J.S. Donal, Jr., formerly of Princeton, died October 29 in Sun City, Arizona, where he and his wife had been living for the past six months. Dr. Donal retired in 1970 from RCA Laboratories, where he was Administrator, Technical Relations, after thirty-four years with RCA. He joined the Research Department of the RCA Electron Tube Division in Harrison, N.J., in 1936 and transferred to Princeton when RCA Laboratories was established in 1942. From 1936 to 1953 Dr. Donal's work was in the fields of television light valves and magnetron tubes for radar equipment. On these subjects he published a number of papers and contributed chapters to books. A graduate of Swarthmore College, he received the MS and PhD in Physics from the University of Michigan. After his retirement from RCA, he taught physics classes at Trenton State College. Dr. Donal was a member of Sigma Xi and the American Physics Society. A Senior Member of the IEEE, he had been extremely active in the IEEE Princeton Section. He had also served as a member of the Board of Technical Advisors of RCA Institutes.

Awards

Missile and Surface Radar Division

Six MSRD engineers received Technical Excellence Awards. The accomplishments that resulted in these awards are summarized below:

James W. Cole and **Harry C. Irion** — for their roles as test conductors during the AEGIS EDM-1 at-sea Category II test phase.

Joseph J. Mark and **Dr. Stephen R. McCammon** — for their roles as software engineers on the IR&D program for Drone Control and Data Retrieval System command and control display equipment.

Duard L. Pruitt — for advancing the state of the art of solid-state device application to multi-megawatt power handling.

Richard J. Smith — for the development and practical implementation of digital Fast Fourier Transform (FFT) signal processors.

Government Communications and Automated Systems Division — Camden

Bob Walker received a Technical Excellence Award for his outstanding accomplishments in design support engineering for the URC-78 tactical radio family.

Al Kaschok received a Technical Excellence Award for his achievement in the design and development of a high stability frequency synthesizer for uhf satellite communications.

Advanced Technology Laboratories

Donald Herzog was cited recently by *Aviation Week and Space Technology* as part of the team that successfully developed and demonstrated the first helicopter with a completely fly-by-wire control system.

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	DOMESTIC	FOREIGN
1-year	$6.00	$6.40
2-year	10.50	11.30
3-year	13.50	14.70

Palm Beach Division

Charlie Jones of Data Interconnect Design received a Professional Achievement Award for the development of a time-division-multiplex electronic-resource-management system using CMOS LSI techniques, for applications requiring 30 to 130 telephone interconnects.

SMPTE Journal Award

The Journal Award for 1974 is being presented by the Society of Motion Picture and Television Engineers to **Bill Hannan, Michael Lurie, Robert E. Flory,** and **Robert J. Ryan** for their paper entitled "Holotape: a low-cost prerecorded television system using holographic storage," published in the November 1973 issue of the *Journal of the SMPTE*, Mr. Hannan is Chief Engineer at the Palm Beach Division; Lurie, Flory, and Ryan are at the RCA Laboratories.

Professional activities

RCA Laboratories

Dr. Harold Veloric of the Microwave Technology Center has been elected chairman of the North Jersey chapter of the IEEE Microwave Theory and Techniques Group.

Staff

Herbert W. Hutchison, Director, Materials — Government, Commercial, and Solid State, was chairman of a recent Electronic Industries Association seminar on "The Economy of the Future and its Impact on Materials used by the Electronic Industries." **Ben Jacoby,** Division Vice President, Solid State Marketing, presented the manufacturer's viewpoint, as part of a presentation entitled the "Semiconductor Industry Outlook — One Year Later."

Service Company

Engineers at the Missile Test Project, Patrick Air Force Base, Fla. recently participated in an "On-Axis Radar" symposium. Contributing RCA authors were **A. E. Hoffman-Heydan, R. Pepple, D. F. Riordan, M. C. Coommer, J. V. Copp, W. H. Cooke, J. T. McKnight, Jr., J. A. Ward, Jr., and O. J. W. Christ.**

Degrees Granted

Martin B. Forton of RCA Global Communications, Inc. received the Bachelor of Engineering (EE) from the City College of the City University of New York.

William Schulte of Data Interconnect Design, Palm Beach Division, received the Master of Science in Electrical Engineering from Florida Technological University.

Editorial Representatives

The Editorial Representative in your group is the one you should contact in scheduling technical papers and announcements of your professional activities.

Government and Commercial Systems

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Commercial Communications Systems Division

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R. E. WINN Broadcast Systems Antenna Equip. Eng., Gibbsboro, N.J.
A. C. BILLIE Broadcast Engineering, Meadowlands, Pa.

Mobile Communications Systems
F. A. BARTON* Advanced Development, Meadow Lands, Pa.

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Government Communications and Automated Systems Division
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M. R SHERMAN Solid State Technology Center, Somerville, N.J.

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Entertainment Tube Division
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J. H. LIPSCOMBE Television Picture Tube Operations, Marion, Ind.
E. K. MADENFORD Engineering, Lancaster, Pa.

Industrial Tube Division
H.K. JENNY Industrial Tube Operations, Lancaster, Pa.
H. J. WOLKSTEIN Solid State Product Development Engineering, Harrison, N.J.

Consumer and Solid State Electronics

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J. STARK Color TV Engineering, Indianapolis, Ind.
P HUANG Engineering, RCA Taiwan Ltd., Taipei, Taiwan

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RCA Service Company
M. G. GANDER* Consumer Services Administration, Cherry Hill, N.J.
W. W. COOK Consumer Service Field Operations, Cherry Hill, N.J.
R. M. DOMBROSKY Technical Support, Cherry Hill, N.J.
R. I. COGHILL Missile Test Project, Cape Kennedy, Fla.

Parts and Accessories
C. C REARICK* Product Development Engineering, Deptford, N.J.

RCA Global Communications, Inc.

W. S. LEIS* RCA Global Communications, Inc..New York, N.Y.
P. WEST* RCA Alaska Communications, Inc., Anchorage, Alaska

NBC, Inc.

W A HOWARD* Staff Eng., Technical Development, New York, N.Y.

RCA Records

J F. WELLS* Record Eng., Indianapolis, Ind.

Corporate Development

C. A. PASSAVANT* International Planning, New York, N.Y.

RCA Ltd

W. A. CHISHOLM* Research & Eng. Montreal, Canada

Patent Operations

M. S. WINTERS Patent Plans and Services, Princeton, N.J.

Electronic Industrial Engineering

J. OVNICK* Engineering, N. Hollywood, Calif.

*Technical Publications Administrators (asterisked * above) are responsible for review and approval of papers and presentations

RCA Engineer

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