RCA Engineer

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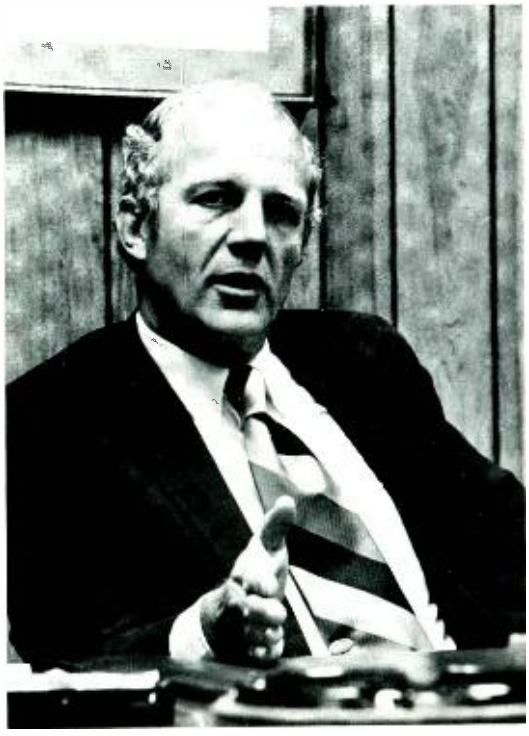
Dec|Jan
1972|73

COS/MOS–a unique product line

In today's highly competitive semiconductor industry, it is a distinct advantage to have a popular product which the user instinctively associates with one particular supplier. There have been very few opportunities for this to happen in recent years because of the large number of producers throughout the world who aggressively seek to neutralize any momentary advantage of a competitor who introduces a new product to the market.

RCA has been able to build and sustain product association with COS/MOS (Complementary-Symmetry/Metal-Oxide-Semiconductor) integrated circuits. Beginning with the first commercial announcement in 1968, RCA has been associated with the development of this unique product line and with its ever-expanding capability. Initially there were many skeptics among both competitors and users who felt that the market for this technology would be limited to a few highly specialized applications which required extremely low power consumption. Consequently, it took considerable time and effort to expand the product line, educate customers, and thereby develop a general awareness that COS/MOS is a highly attractive, broadly usable product. Our success in the world marketplace is now very real and growing rapidly, as circuit and equipment designers have been convinced that they can make important advances in their products with COS/MOS. Other semiconductor makers, once skeptical, are now entering the market to participate in its exciting possibilities.

The papers in this issue illustrate the breadth of RCA effort. Contributions have been made by many individuals, only a few of whom are represented here. It is the high quality of this expanding activity which will retain our association with one of the most rapidly growing segments of the semiconductor industry.



William C. Hittinger
Executive Vice President
Consumer and
Solid State Electronics
Somerville, New Jersey

Our Cover

. . . features the rapidly expanding COS/MOS product line. "Pouring" forth are some of the many COS/MOS device packages; printed in the background are a few of the myriad applications. **Cover photo:** John Semonish, Commercial Engineering, Electronic Components, Clark, N.J.

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Jan 1973

RCA Engineer

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• To disseminate to RCA engineers technical information of professional value • To publish in an appropriate manner important technical developments at RCA, and the role of the engineer • To serve as a medium of interchange of technical information between various groups at RCA • To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions • To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field • To provide a convenient means by which the RCA engineer may review his professional work before associates and engineering management • To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

Contents

ex-RCA'ers pioneers in electronics

J. P. Dunn | F. J. Strobl*

The editors had the privilege of taking a peek at a unique organization of former RCA radio and TV pioneers. This South Jersey group is unique in that it has no official name, rules, or regulations. Nor are there elected officers, dues, or formal agenda. But in spite of transgressing organizational theory, the group is functioning well.

This group, with the unofficial title of "the ex-RCA'ers," meets monthly. No serious business is conducted at these luncheon meetings. The members gather to renew old friendships and to swap tales of their activities during retirement. The most recurring topics heard at one meeting dealt with golf and travels.

Although loosely knit, the club has a common thread bonding the members. They have all had a stake in RCA's growth; and sometimes the talk turns to the business of the Corporation today.

The idea of a club composed of retired RCA people had its beginning in July, 1970. T. A. (Ted) Smith, after attending a retirement dinner for M. A. (Merrill) Trainer, wrote to Merrill: "Your luncheon yesterday was such a pleasant affair, with the opportunity to see people who had once been joined by the common bond of an early interest in television, that it seemed to me that there should be other times for getting together. I doubt that it would be possible to count on other retirements and so some other agency would be needed." Such an "agency" was soon to come into being.

*Mrs. Dunn is Art Editor for the *RCA Engineer*; Mr. Strobl is Editor of TREND and Consulting Editor on the *RCA Engineer*.

Top photo shows a group of old timers in the David Sarnoff Library discussing "current RCA events." Photo directly above shows the club members enjoying a new-products demonstration by Harry Cooke.

Rufus Applegarth (left) and Dr. Irving Wolff meet at the recent club meeting in Princeton.

Left, Ted Smith (unofficial president) addresses the ex-RCA'ers: seated at Ted's right is Dr. V. K. Zworykin. Photo at right shows members intrigued by a display in the Princeton auditorium.

Above (unofficial Vice President) Merrill Trainer during a pause that refreshes (ed. note thanks to Merrill for supplying much of the information contained in this editorial). At right, during dinner when conversation picks up.

Herman Gihring (center) and John Volkmann inspect the Holocard reader.

Stu Pike, Felix Cone and Ray Kell inspect mementos in the Sarnoff Library.

Sam Watson, Merrill Trainer, and Frank Strobl exchange ideas.

A group of electronic pioneers try out the Holographic identification System.

Steve Walton, Stan Cochran and Loren Jones exchange greetings.

David Sarnoff Library, alive with ex-RCA'ers.

R. Ballard and Ralph Holmes ir "after dinner conversation."

Dinner served at the David Sarnoff Research Center.

Ted Smith at first envisioned "an informal, educational, non-profit organization to be known as the RCA System Video Pioneers, or RSVP." The purpose of RSVP would be "to hold a luncheon or a dinner once or twice a year in the South Jersey area at which time the advantages of the RCA Television System can be discussed, yarns can be swapped, and little known events of the early days of television can be revealed. Other projects might include preparing and distributing notes relating to the pioneering TV period."

After some discussion amongst Ted, Merrill, and Mul Brandt, they decided to start off with a luncheon at the Lorann House Restaurant in Westmont, N.J., on December 7, 1970. At this first meeting, there were 15 members present: T. A. Smith, M. A. Trainer, M. M. Brandt, K. B. Russell, J. E. Young, V. E. Trouant, L. E. Anderson, H. E. Gihring, S. W. Pike, C. D. Kentner, W. L. Lyndon, F. C. Blancha, J. E. Beezer, A. H. Turner, and N. M. Brooks.

As news of the club's formation spread (mostly by word-of-mouth) and the membership increased, the luncheons were moved to Compton's Log Cabin in Haddon Township. Again as the membership continued to grow, the meetings progressed in steps from the smallest private dining room at Compton's into their largest.

Generally, the club meets the second Monday of each month except for July and August. The May 1972 meeting was held at the David Sarnoff Research Center in Princeton, N.J. A sizeable group of the Princeton area residents shows up at all of the club's meetings. (One member even comes from Delaware.)

The membership roster has over 150 names, representing every RCA activity. At the September 1972 meeting, 90 members were present. Now,

Roster of ex-RCA'ers

H. Albrecht
H. E. Allen
L. E. Anderson
A. Rufus Applegarth
R. C. Ballard
Jay Barth
Harry Becky
A. V. Bedford
G. L. Beers
J. E. Beezer
G. C. Bingham
F. C. Blancha
E. G. Bowman
Harlan Brelsford
N. M. Brooks
J. M. Brumbaugh
W. W. Bullock
Leonard B. Bureau
E. C. Campbell
C. O. Caulton
S. W. Cochran
F. E. Cone
D. R. Creato
E. L. Clark
Thomas Consalvi
A. N. Curtiss
L. H. Davis
E. T. Dickey
E. A. Dodelin
C. A. Dorner
E. G. Dornfield
Thomas T. Eaton
A. E. Ertner
D. J. Finn
C. A. Fish
N. Fisher
L. E. Flory
E. C. Foreman
L. T. Fowler
F. A. Fuhrmeister
H. E. Gihring
G. S. Gilchrist
M. S. Gokhale
Paul E. Goley
E. Dudley Goodale
C. A. Gunther
E. T. Hamilton
Robert L. Harvey
K. P. Haywood
Roland S. Hemingway
Roy A. Henderson
J. Hertzberg
Harold Hoffer
Hollis Hoffman
K. R. Hollister
R. H. Holmes
R. S. Holmes
Walter Holt
R. L. Holtzheimer
A. R. Hopkins
R. T. Huntington
Alfred E. Jackson
L. F. Jones
W. L. Jones
H. S. Kalyn
A. S. Karker
M. E. Karns
H. M. Kearney
R. D. Kell
J. P. Kerrigan
H. D. Knapp
H. N. Kozanowski
George Kraft
G. A. Kumpf
Walter L. Lawrence
C. Lealg
F. S. Leroy
George Lindner
J. E. Love
W. L. Lyndon
H. T. Macauley
Guy Manviller
A. F. Maugeri
F. H. McCarthy
W. P. Mercer, Jr.
Benjamin Miller
A. B. Mills
F. W. Millspaugh
C. C. More
Harold D. Newton
N. J. Oman
S. W. Pike
W. J. Poch
J. E. Ploucher
R. B. Prunty
Charles Rammer
S. Read, Jr.
H. E. Reeber
W. R. Reeves
F. Rettenmeyer
M. D. Riefler
John H. Roe
J. Roff
C. A. Rosencrans
E. W. Russell
K. B. Russell
J. W. Sanborn
J. W. Sanderson
J. N. Sanville
Harvey Schock
H. J. Schrader
J. D. Seabert
C. R. Sharpless
Fred F. Shorys
C. M. Sinnett
R. H. Slimm
J. P. Smith
Paul V. Smith
Ted A. Smith
Charles S. Stickney
B. D. Streeter
A. C. Stocker
A. H. Super
E. F. Sutherland
J. P. Taylor
H. W. Taylor
R. H. Teare
W. M. Tomlin
Merill A. Trainer
V. E. Trouant
R. J. Tullar
A. H. Turner
C. D. Tuska
John Volkmann
S. A. Walton
Albert Ward
S. H. Watson
H. R. Wege
R .R. Welsh
F. W. Wentker
R. P. Wetherald
T. J. Whitney
W. A. Willard
G. H. Williams
R. C. Willman
George Wilson
L. J. Wolf
I. Wolff
R. W. Wythes
M. J. Yahr
J. E. Young
W. J. Zaun
Carl W. Zemke
V. K. Zworykin

the membership requirements have been relaxed to include anyone (ex-RCA) that had some early connection with RCA radio or television. Thus, engineers are in contact with their former associates in manufacturing, sales, marketing, and all other diverse activities that make a corporation function.

Since the members are old friends, no particular ceremony is followed at the meetings. Sometimes, there is a guest speaker. Often, a member will relate some interesting experience he has undergone. The informality of the club extends even to the method of paying for the luncheon tabs. A basket is passed around, and each member pays for what he eats plus gratuity and tax. This honor system not only works, but the basket usually contains enough left over to pay for postage and other items needed for meeting announcements.

Sociologists and psychologists today are emphasizing the problems that can arise with retirement. The transition from the working life is a shock to many retirees. But at the ex-RCA'ers meetings, the members seem more concerned with squeezing their many activities into each day. As one member said: "I think the reason we keep busy is that basically we have had interests all our lives. Our jobs kept us busy but we were always able to find other interests." This advice we should all consider carefully. The proof is there.

But the feeling that most pervades the club membership is that of pride —pride in knowing that their contributions have helped RCA become a giant in the electronics industry. After all, they have a grand total of over 4,500 years of experience.

Future Issues

The next issue of the RCA ENGINEER, Vol. 18 No. 5, will contain representative papers devoted to radar and antenna engineering. Some of the topics to be covered are:

Television receiving antennas

Communication antennas for Viking

G & CS antenna range

Advanced receiver techniques

Phase shifter design

Phased array design

Computer-aided antenna design

Discussions of the following themes are planned for future issues:

Transportation

Global communications

Broadband information systems

SelectaVision systems

Command and control

Broadcast and mobile communications

Engineering at RCA Ltd.

Engineer and the Corporation

MOS—an RCA pioneered technology; COS/MOS—RCA's thrust in digital logic

H. Weisberg

Several of the advantages and applications of COS/MOS circuits are described in other papers in this issue. This paper reviews the development of COS/MOS logic circuits and projects some of the extensions of these circuits through 1975.

Harry Weisberg, Manager
COS/MOS IC and Liquid Crystal Operations
Solid State Division
Somerville, N.J.
received the BSCE from City College of New York in 1944 and the MS in chemistry from Brooklyn Polytechnic Institute in 1960. He studied electronics at the University of Scranton. Upon graduation from C.C.N.Y., Mr. Weisberg joined E. I. DuPont where his work involved the engineering aspects of industrial chemical products. He subsequently directed the developed of a line of new cellulose derivatives. Mr. Weisberg joined RCA in 1959, where he has worked in various design and process-development areas. He has contributed significantly to the design concepts incorporated into RCA's high-reliability and military-approved rectifier types. The RCA Thyristor and Power Rectifier Activity functioned under his design leadership from 1961 to 1965. During this time, he supervised and participated in the design of RCA's thyristor line. Mr. Weisberg was appointed Manager, Thyristor Product Development, in 1965. In early 1969, he assumed responsibility for COS/MOS design and technology. In 1971 he was appointed Manager of MOS IC and Liquid Crystal Products. In this capacity, Mr. Weisberg has responsibility for engineernig, manufacturing, and marketing. Mr. Weisberg holds three U.S. Patents and several foreign Patents involving new polymeric materials. He also holds five patents in semiconductor technology. Several additional patents are pending. He has contributed to *Solid State Design* and is a member of IEEE and American Chemical Society. Mr. Weisberg received the RCA Engineering Achievement Award in 1964.

Reprint RE-18-4-12 (ST-6110)
Final manuscript received September 25, 1972.

TEN YEARS AGO, at the IRE Electron Devices Meeting in Washington, D.C., Drs. Steven R. Hofstein and Frederick P. Heiman presented a paper describing the forerunner of today's vast variety of MOS logic circuits. Working under the direction of Thomas O. Stanley at the RCA Electronic Research Laboratory in Princeton, Drs. Hofstein and Heiman succeeded late in 1962 in developing a modest 50-by-50-mil array of 16 MOS transistors.[1]

The complementary-symmetry concept for switching had intrigued RCA researchers as early as the 1950's, when T. O. Stanley experimented with unipolar complementary pairs. Significant contributions were also made by P. K. Weimer, *et. al.*, in work with complementary TFT's. The advent of IC MOS technology paved the way for the practical application of complementary techniques to digital switching.

The basic building block for MOS is the inverter pair shown in Fig. 1a. Comparison of the switching characteristics and load lines for various combinations of complementary pairs shown in Fig. 1b and 1c clearly demonstrates why RCA's early research effort was directed toward the development of COS/MOS technology.[2]

History and organization

G. B. Herzog and other researchers at the RCA Laboratories, recognizing the advantages that the p-channel/n-channel complementary pair would provide for switching as compared to the p-MOS load-resistor combination, pushed hard toward the practical development of this technology. The task was later picked up in Lloyd Day's newly formed Microelectronics activity in Somerville in the form of Princeton Applied Research projects. This effort resulted in the breadboarding of a COS/MOS flip-flop assembled from discrete inverters in June of 1963. With support from R. B. Janes' Advanced Development activity under the direction of P. D. Gardner, the team of R. D. Lohman and I. S. Kalish produced in 1964 what

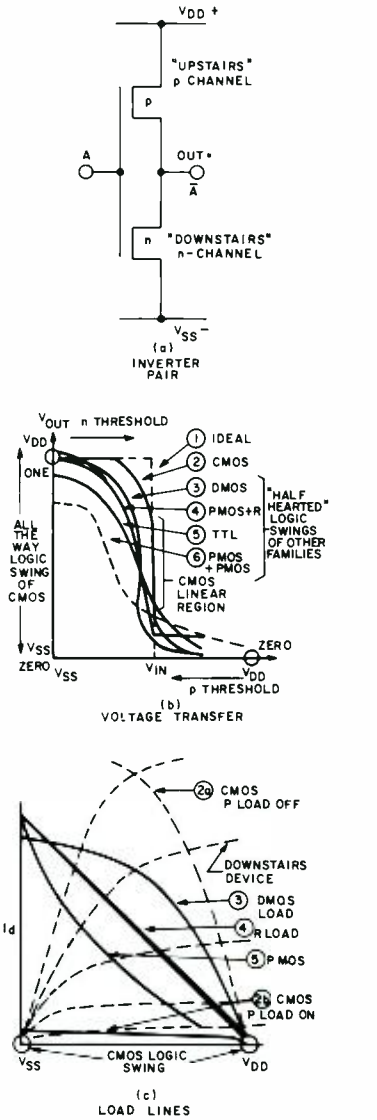
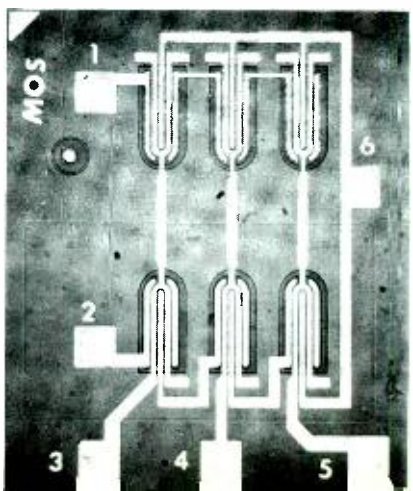


Fig. 1—COS/MOS inverter pair (a), and comparison of switching characteristics (b) and load lines (c) for various combinations of complementary pairs.

Fig. 2—Three-input COS/MOS NAND/NOR Gate developed in 1964.



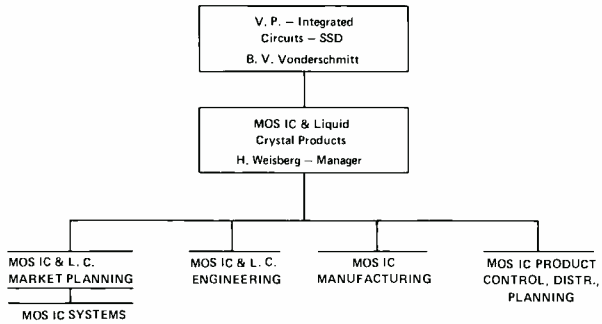
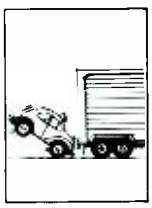


Fig. 3—Present organization of COS/MOS IC activity.

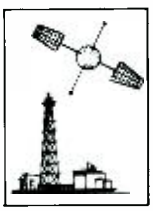
Fig. 4—Applications of COS/MOS integrated circuits.

AUTOMOTIVE



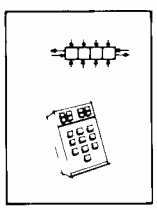
ELECTRONIC LOCKS
TACHOMETER/ SPEEDOMETER
FUEL-INJECTION CONTROL
SPARK-ADVANCE CONTROL
WIPER PAUSE CONTROL
CLOCKS
ADAPTIVE BRAKING
VEHICLE SAFETY CHECK
DRIVER CHECK
ELECTRONIC TRANSMISSION
ANTI-WHEEL-SPIN AND SPEED CONTROL

DATA ACQUISITION



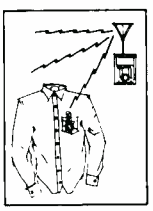
INDUSTRIAL MONITORING
SATELLITE READOUT
UTILITY-METER READING
AIRCRAFT FLIGHT-DATA SYSTEM
PROCESS CONTROL
TRAFFIC CONTROL
ECOLOGY MONITORING
D/A AND A/D CONVERTERS

COMPUTERS



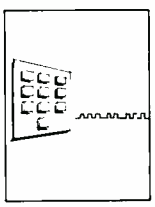
PARALLEL/SERIAL COMMUNICATIONS BUFFERS
COMPLETE AEROSPACE COMPUTERS
REMOTE TERMINALS
PERIPHERAL BUFFERS
POCKET CALCULATORS
SERIAL CONTROL COMPUTERS
SCRATCH PAD MEMORIES
MAIN MEMORIES

COMMUNICATIONS



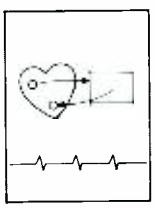
POCKET PAGERS
SELECTIVE CALL
FREQUENCY SYNTHESIZERS
DIGITAL FILTERS
PULSE-PAIR DECODERS
PRESET CHANNEL MEMORY
PHASE-LOCKED OSCILLATORS
REMOTE TUNING
CATV CONVERTERS

TELEPHONE



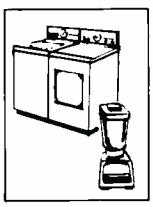
TONE SYNTHESIZING
TONE DETECTION
SOLID-STATE CROSSPOINTS
DIAL-PULSE CONVERTERS
REPERTORY DIALER
DIGITAL PBX
DELTA-MOD CONVERTERS
AUTOMATIC REDIAL

MEDICAL



BLADDER CONTROL
LUNG STIMULATION
HEART PACERS
PROSTHETIC CONTROL
PORTABLE INSTRUMENTATION
AUTOMATIC PATIENT MONITORING

APPLIANCES



SPEED/TIME CONTROL
HEAT/TIME CONTROL
INDUSTRIAL SEQUENCERS
WASHER AND DRYER TIMERS
AUTOMATIC COOKING CONTROLS
DIGITAL CLOCKS
TOUCH CONTROLS

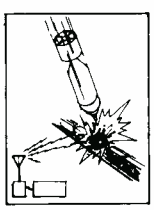
ADDRESSING

DEMOLITION-FUZE DETONATION
INTERROGATION OF SATELLITES
RESOURCE MONITORING BY SATELLITES

CLOCKS AND TIMERS

WRIST WATCHES
AUTO CLOCKS
DIGITAL CLOCKS
BATTERY WALL CLOCKS
NAVIGATION CLOCKS
ENVIRONMENTAL SAMPLING TIMERS
INDUSTRIAL TIMERS
DOWN-TIME CLOCKS

FUZES



FREE-FALL COUNTER
VAR-TIME FUZE
SELF-DESTRUCT FUZE
ELECTRONIC LOCKS FOR WARHEADS
DEMOLITION RECODER

was probably the first COS/MOS IC, a three-input NAND/NOR gate (Fig. 2).

The significance of this technological achievement was not lost on Art Liebschutz, who was then reporting to Ben Jacoby in his capacity as digital marketing manager. The Microelectronics group in 1965 was hard at work on the development of a low-power DTL circuit for the digital market.

In 1966, the forerunner of the present COS/MOS activity combined both bipolar and MOS digital functions under J. Ritcey (followed by E. E. Moore in 1968) as engineering manager, F. J. Rohr and A. J. Bosso in marketing, and B. V. Vonderschmitt in design and applications for both digital and linear. The present organization, shown in Fig. 3, follows the product-line concept introduced by W. C. Hittinger with the formation of the Solid State Division in 1970. The liquid-crystal activity has been incorporated into the COS/MOS product line in recognition of the strong interaction and interdependence of the two technologies.

Advantages of COS/MOS

The micropower dissipation, high noise immunity, wide operating-voltage range (3 to 15 V), and temperature range (−55°C to +125°C for ceramic and −40°C to 85°C for plastic) are well known advantages of COS/MOS. Also important is the ease of converting and implementing logic functions in integrated-circuit form to system applications.

These attributes have resulted in a versatility of applications, some of which are better or more economical because of COS/MOS and some of which wouldn't be possible with any other technology. Some of these applications are illustrated in Fig. 4.

Standard vs. custom

RCA's announcement of the availability of commercial COS/MOS circuits in 1968 resulted in about 15 standard circuits by 1969. This small selection, compared with more than 200 bipolar standard logic circuits, and the lack of second sourcing for COS/MOS resulted in difficulties in getting product acceptance. Today, RCA's CD4000 series consists of over 60 standard circuits,

virtually all of which are second sourced by major solid-state integrated-circuit manufacturers.

From the beginning, the feasibility of MSI and LSI using COS/MOS technology was an attractive feature. Early support by NASA resulted in the development of custom LSI circuits. The CD4057A began as a NASA-funded custom circuit development, the TA5716. It is primarily a four-bit central processor which contains a shift/store register in addition to the arithmetic and control circuits. Sixteen separate processing and logic operations can be performed, including the logical AND, EXCLUSIVE OR, and OR. The processing operations include COUNT UP, COUNT DOWN, SUBTRACT, ADD, and SHIFT (left and right). Applications include portable-battery-operated compact computers, or equipment in which noisy environments are encountered.

More than 50 custom circuits have been developed since the TA5716, and about as many are presently in various stages of development. Custom COS/MOS circuits are being sold for various watch and clock applications, heart pacers, satellites, pocket pagers, fuzes, and many other functions.

To participate in this vast and varied systems world, RCA must interface with customers at many levels. Accommodating the many and varied needs of customers is perhaps the greatest challenge to continued success. It is no longer possible to sell devices and simply provide applications assistance in the traditional manner; IC manufacturers must be prepared to do that and much more. Participation in the wide spectrum of supplying system support can range from processing wafers with fully designed masks to designing a system on a chip with only function parameters provided and specifying outboarded components as well. RCA, like other manufacturers, is being challenged to develop a far greater breadth of skills than has traditionally been the component-suppliers' contribution.

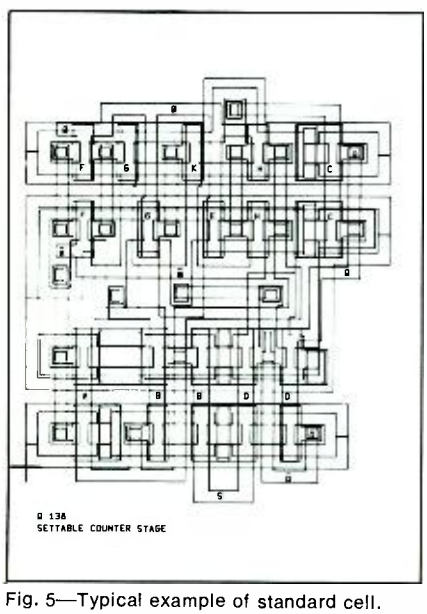


Fig. 5—Typical example of standard cell.


Fig. 6—Beam-lead version of CD4013A.

RCA's design automation facility and capabilities have been described elsewhere.[3] This activity has progressed from a drafting and digitized mask-generation facility to a sophisticated CAD facility with an extensive library of standard cells, such as that shown in Fig. 5. The combination of standard cell and metal routing routines allows the designer the full gamut of compromise between time optimization and maximum efficiency of packing density. RCA will continue to develop and expand the repertoire of standard circuits to meet customers' demands and serve their specific custom needs.

Extension of COS/MOS technology

Using the complementary MOS inverter shown in Fig. 1a as the basic functional-cell building block, new technology will develop to enhance COS/MOS as a desirable and economical digital integrated-circuit form. Currently under development is the modification and adaptation of beam-lead techniques to MOS. The Solid State Technology Center has already produced experimental beam-lead designs for the CD4000A, the CD4007A, the CD4013A (shown in Fig. 6), and several others. The first beam-lead circuits for commercial applications were delivered this year, and the technology will be extended into the standard product line in 1973.

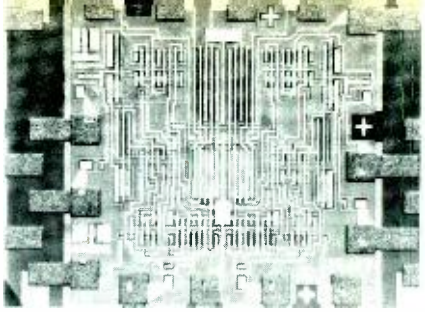


Fig. 7—Chip used in COS/MOS timing circuit.

The main thrust of new technology will be to increase function density, speed/power capability, voltage range, and LSI capability, as shown in Table I. This improvement will have to be accomplished at planned cost reductions. To aid in packing-density improvement, multilayer metallization utilizing polycrystalline silicon, ion implantation, and self-aligning silicon gate techniques are being evaluated. Fig. 7 shows the layout of a timing circuit comprising an oscillator inverter, a counter divider from 32-kHz to 1-Hz output, a divide-by-60 stage for minutes, a divide-by-12 stage for hours, and a BCD-to-seven-segment output stage for digital display of hours, minutes, and seconds.

Polycrystalline silicon gate circuits have been produced for use in watch circuits that will operate from a single-cell mercury battery to an end-of-life rating of 1.1 V. It is theoretically possible to design COS/MOS to operate from power sources as low as 0.5 V. COS/MOS on sapphire, commonly known as SOS, will allow higher speed power values of 1 pJ to be reached with propagation delays of 5 ns.

COS/MOS has undoubtedly achieved a place in the designer's collection of circuit logic forms for systems development.

References

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Table I—COS/MOS present capabilities and future plans.

	1968	*1972*	*1975*
Gate complexity	40	500	3000
Maximum chip size (mils)	80 x 80	150 x 190	300 x 300
Maximum clock frequency (MHz)	5	15	50
Voltage-range capability (V)	6 to 15	1.0 to 20.0	0.5 to 25

COS/MOS markets

A. J. Bosso

The market for COS/MOS integrated circuits is as broad as the spectrum of logic applications. The advantages of complementary-symmetry logic have long been known and desired; it remained for the Solid State Division, with its COS/MOS line of circuits, to make these advantages economically feasible and, therefore, available to the full range of electronic-equipment manufacturers.

THE PRIMARY ADVANTAGES of complementary-symmetry circuits, and of COS/MOS in particular, are:

Circuit advantage	User benefit
Wide operating-voltage range (3V to 15V)	Less regulation of power supply required. Immunity to power-supply or ground-line noise.
Extremely low power dissipation (typically 10nW/gate)	Makes possible operation of large logic systems from battery power supply. Substantially reduces conventional power-supply size and regulation requirements and, therefore, total power-supply costs. Lower power dissipation reduces substantially or eliminates auxilliary cooling systems and, therefore, the associated weight, space, and costs. Lower power dissipation permits closer packing of circuits and, therefore, increases packing density of equipment.
High noise immunity (typically 4.5V at a V_{DD} of 10V, theoretically $V_{DD}/2$)	The COS/MOS circuits are ideal for applications in which external electrical noise ambients are encountered. Relatively low speed of COS/MOS circuits does not generate noise. Noise immunity of COS/MOS circuits is virtually constant over the full temperature range.
Tolerance of COS/MOS to its total environment (tolerance to supply voltage, noise, temperature, transistor parameters)	Facilitates system design and saves engineering time. Lack of criticality and "fine tuning" requirements means COS/MOS "works the first time." Absence of criticality means smoother-running production lines. COS/MOS tolerance to its total environment means better operating reliability.
Only one power-supply voltage and one clock phase is required	Easier and more reliable system design.

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received the BSEE from Penn State in 1957 and joined RCA's Solid State Division in the same year. He worked as an applications engineer for digital-switching transistors until 1960 when he was made Engineering Leader of digital-switching-transistor applications. In 1967, Mr. Bosso was made Market Planner for COS/MOS IC's, and in 1971 was made Manager, MOS-IC Market Planning.

With advantages such as those listed above and with the economy provided by high yields, MSI/LSI functions (both standard and custom), and plastic packaging, it is easy to understand why COS/MOS is extending the spectrum of electronic logic to applications which were not electronic previously. One of the primary examples is the watch and clock market. It is now possible to wear a wristwatch that is accurate to a minute a year and that runs continuously for a year on a single 1½-volt cell for a price far lower than that of a conventional mechanical chronometer.

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Clock and watch market

Truly, the COS/MOS watch is a secondary time standard on your wrist. Before the advent of COS/MOS, this kind of performance was limited to laboratory instruments at prices of hundreds to thousands of dollars. By 1975, a significant number of watches will be built using quartz crystals and COS/MOS, and the retail price will be under $50. By 1980, 50 to 75% of watch production will be electronic

with retail prices comparable to any in the industry. In addition to watches having motor-driven conventional hands, digital watches using a single COS/MOS LSI chip and either liquid crystal or LED displays will be available shortly.

Automotive market

Federal pressure for control of emissions and for increased safety provisions on automobiles, some of it in the form of legislation, is increasing. To meet the federal requirements, more logic circuits will be used in automobiles. With its wide operating voltage range (almost exactly matching the excursions of the automobile "12-volt" supply) and high noise immunity, COS/MOS is a natural for automotive applications, and is being used extensively for programs which will mature in the near future as well as for advanced-systems work.

Aerospace and military markets

But it is not only in new markets that the advantages of COS/MOS are attractive. Certainly COS/MOS has proven very attractive in aerospace applications. The very low power dissipation, together with the packing density which it permits, have provided a much needed means of accomplishing a greater number of tasks per satellite within given power and weight constraints than was possible previously. For space applications and for critical military and industrial applications, the Solid State Division is currently in the process of qualifying the COS/MOS line to MIL-M-38510. The qualification process should be complete in the fourth quarter of 1972, and qualified

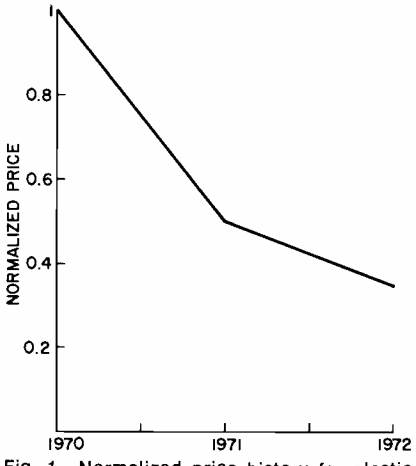

Fig. 1—Normalized price history for plastic-packaged COS/MOS circuits.

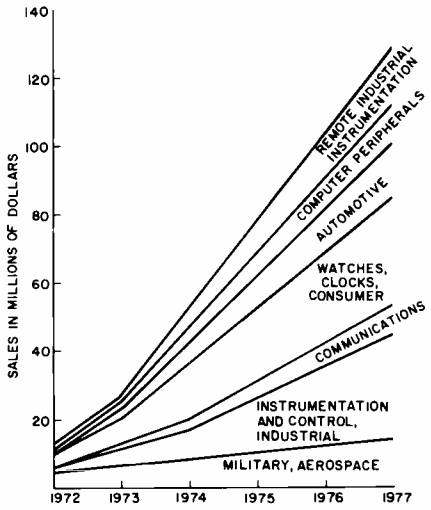

Fig. 2—Projected COS/MOS sales by market category.

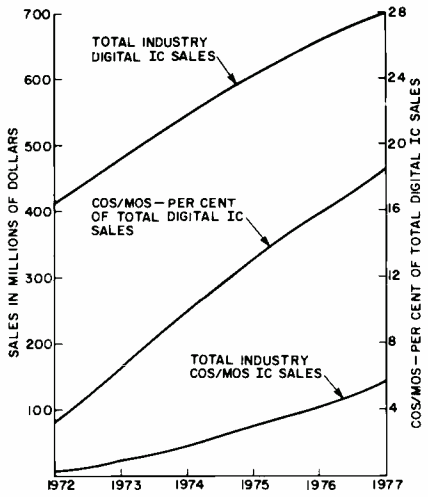

Fig. 3—Comparison of total COS/MOS sales with total industry sales for all digital IC's.

parts to MIL-M-38510 specifications should be available beginning in the first quarter of 1973.

In military applications, COS/MOS is being used very extensively in munitions-fuze applications, in avionics (navigation, fire control, communications equipment, etc.), in ground communications (frequency synthesizers for both portable and base-station equipment), and for intrusion systems.

Industrial and consumer markets

In the industrial and consumer markets, COS/MOS is proving itself cost effective, as well as operationally attractive, when compared to such technologies at TTL and HTL. RCA's introduction, in 1970, of economical plastic-packaged COS/MOS IC's was a major breakthrough in COS/MOS IC production costs. Fig. 1 shows the normalized price history for plastic-packaged COS/MOS circuits. Customers are now beginning to report back that, in many systems, the savings in power-supply costs, as well as the space and weight savings resulting from the elimination of blower fans and heat sinking, have given them a total cost savings and made their equipment more competitive. In many instances, the wide choice of COS/MOS circuits and/or custom circuits also has helped to reduce package count. But the best feedback is perhaps the simplest, that is the comment, "This stuff is great to work with. My system worked the first time." What better way to describe the advantage of the great tolerance of COS/MOS to its total environment?

In 1972, 70% of the COS/MOS circuits sold will go into non-military applications. This percentage will increase rapidly in the next few years. Some typical non-military applications are personal remote pagers, modems, process control and other specialized computers, data-buoy instrumentation, test and measurement instruments, telephone control logic, remote utility-meter-reading equipment, industrial controls, commercial avionics, and commercial communications equipment. In the not too distant future, the price of COS/MOS circuits will permit their use in home-entertainment applications, such as frequency synthesizers for FM radios and TV sync circuits. Fig. 2 shows projected COS/MOS-IC sales by market category for the years 1972 through 1977.

Conclusion

The exact manner of implementing the circuits will change, and increases in speed performance will occur, but the basic operating advantages and cost effectiveness of COS/MOS circuits will continue to earn their place in the logic-circuit market. Fig. 3 shows total industry sales for all digital IC's and COS/MOS together with COS/MOS sales as a percentage of the total. Both the COS/MOS technology and the RCA Solid State Division will be major factors in the total logic circuit market by 1975.

Fundamentals of COS/MOS integrated circuits

R. A. Bishop | D. R. Carley

The development of the technology that makes possible simultaneous fabrication of n-channel and p-channel metal-oxide-semiconductors (MOS) transistors on the same semiconductor pellet has given rise to a new family of monolithic integrated circuits, i.e., the RCA series of complementary-symmetry/metal oxide semiconductor (COS/MOS) devices. This paper discusses the MOS transistors used in COS/MOS integrated circuits, describes basic COS/MOS building-block elements, and explains the built-in protection against high-voltage transient and inherent high noise immunity of RCA COS/MOS integrated circuits. In addition, the major performance characteristics of COS/MOS devices are compared with those of other commercially available digital integrated circuits.

THE BROAD LINE OF RCA COS/MOS integrated circuits includes more than 50 standard types. In addition, almost one hundred custom types are in various stages of design, development or production. These devices feature extremely low quiescent dissipation with wide voltage tolerance, excellent noise immunity, single-phase clocking capability, and moderate speed performance. Moreover, RCA COS/MOS integrated circuits are capable of operation over a supply-voltage range of 3 to 15 V and over an operating-temperature range of −55°C to +125°C for types supplied in ceramic packages or −40°C to +85°C for plastic-package types.

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COS/MOS transistors

In metal-oxide-semiconductor (MOS) transistors, the metal gate electrode that controls the conduction between the two ohmic contacts (called source and drain) is separated from the semiconductor conduction channel by an oxide insulation layer. The two basic types of MOS transistors are enhancement types and depletion types. All MOS transistors used in COS/MOS integrated circuits are enhancement types. The enhancement type of MOS transistor remains in the *off* state for an input gate bias of 0 V with respect to the source. Conduction must be "enhanced" by the application of a bias voltage to the gate electrode in the proper polarity to turn *on* the transistor.

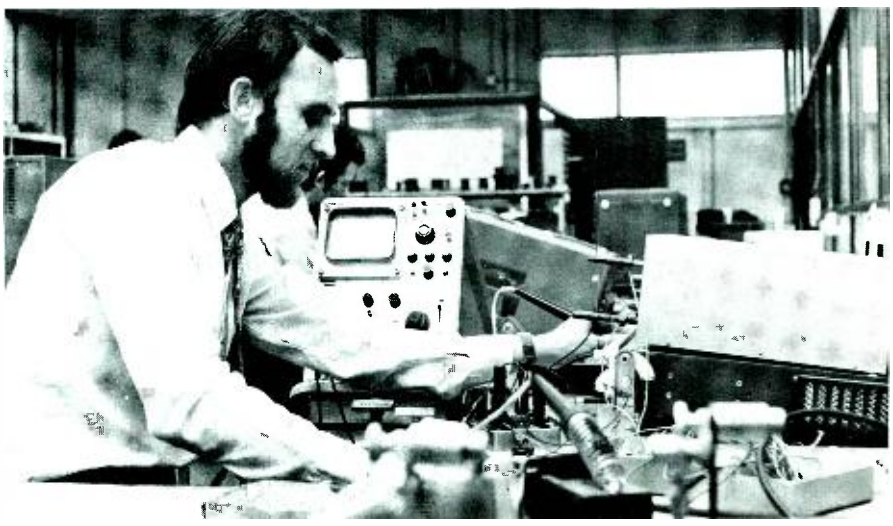
Fig. 1 shows cross-sectional diagrams of an n-channel enhancement type of MOS transistor for both *off*-state and *on*-state conditions. The source and drain regions are formed by n-type diffusions in a p-type substrate. In the *off* state (*i.e.*, when the gate-to-source voltage V_{GS} is 0 V, shown in Fig. 1), a high degree of isolation exists between the source and the drain (typically 10,000 megohms for a drain-to-source voltage V_{DS} of 10 V). As the gate is made positive with respect to the source and the substrate, electrons are attracted to the p-type area between the source and the drain beneath the insulating oxide.

If the gate is made sufficiently positive with respect to the source, *i.e.*, becomes greater than the threshold voltage V_{TH} the number of electrons attracted to the semiconductor region between the source and the drain is large enough to change the surface conduction of this region from p-type to n-type, and an n-type conduction channel is provided from source to drain, as indicated in Fig. 1b.

Fig. 1c shows the schematic symbol for an n-channel enhancement type of MOS transistor. The enhancement-mode feature is indicated in the symbol by the dashed line (channel) that connects the source and drain electrodes. The interruptions of this line are used to show that the channel is "open" unless conduction is enhanced by application of a forward gate bias.

The operation of a p-channel enhance-

Ed. Note: Mr. Carley's biography and photograph are included in his other article in this issue.



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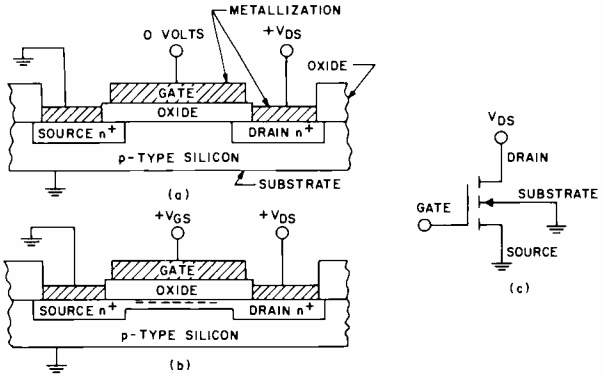


Fig. 1—N-channel MOS transistor: (a) OFF-state condition; (b) ON-state condition; (c) schematic symbol.

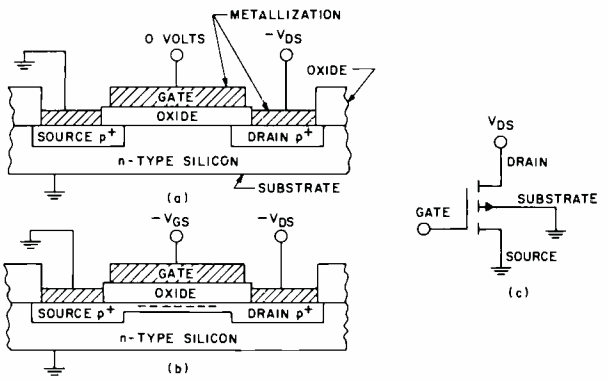


Fig. 2—P-channel MOS transistor: (a) OFF-state condition; (b) ON-state condition; (c) schematic symbol.

ment type of MOS transistor is the same as that of the n-channel type except that n- and p-type regions, voltage polarities, and directions of current are reversed. In p-channel MOS transistors, positive charges (holes) are the current carriers in the channel, rather than electrons as in n-channel devices. Figs. 2a and 2b show the *on*- and *off*-state conditions for a p-channel enhancement type of MOS transistor, and Fig. 2c shows the schematic symbol for this type of transistor. As the gate-to-source voltage V_{gs} is made more negative, a low-resistance (p-type) conduction channel develops between the p-type source and drain regions.

The polarity type of the MOS transistor is indicated in the schematic symbol by the orientation of the arrow at the junction between the channel and substrate. The arrow points to the more negative terminal (channel in n-channel devices or substrate in p-channel devices) of the substrate-to-channel junction.

Basic COS/MOS circuit elements

Inverter

One of the most basic circuit elements used in COS/MOS integrated circuits is the inverter. The COS/MOS inverter consists simply of a complementary pair of n- and p-channel transistors connected in series. In addition to the inverter, there are three other basic circuits that are used extensively in COS/MOS devices. These include the transmission gate, the NOR gate, and the NAND gate. Almost all COS/MOS integrated circuits, regardless of complexity, are implemented by use of one or more of these four basic elements.

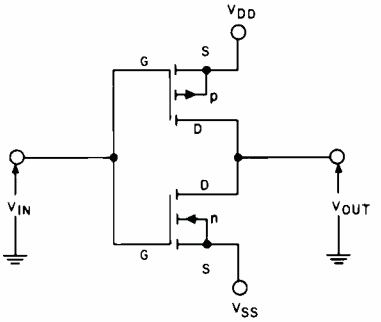
Fig. 3 shows the circuit diagram for the basic COS/MOS inverter. The notations S, D, and G indicate the source, drain, and gate connections, respectively, for each transistor. The p and n notations indicate p-channel and n-channel devices. The voltage V_{DD} is the most positive voltage in the circuit, and the voltage V_{SS} is the lowest or most negative voltage, usually ground.

When the input to the inverter is at zero volts (logic 0), the p-channel transistor is turned *on*, and the n-channel is turned *off*. Under these conditions, a low-impedance path exists from the output to $+V_{DD}$, and a very high impedance exists between the output and ground (V_{SS}). The output voltage, therefore, approaches $+V_{DD}$ (logic 1) under normal loading conditions. When the input is at $+V_{DD}$ (logic 1), the situation is reversed, and the output approaches zero (logic 0). In either state, under normal loading, the output levels are within 10 mV of the $+V_{DD}$ or ground (V_{SS}) voltages; the logic swing, therefore, is virtually equal to the power-supply voltage.

In either logic state, one MOS transistor is *on* while the other is *off*. As a result, the quiescent power consumption, which is equal to the product of the supply voltage and the *off*-unit leakage current, is extremely low. With a supply voltage of 10 V and a typical *off*-unit leakage of 0.5 nA, the quiescent power dissipation is only about 5 nW in either logic state.

During switching transitions, the power dissipated in the COS/MOS inverter increases. Both the p-channel and the n-channel transistors are partially *on* during the transition time; therefore, some current can flow through the channels from the supply voltage (V_{DD}) to ground. Also, any output load capacitance must be charged through the p-channel transistor as the output switches to the high level. Similarly, the stored energy must discharge through the n-channel transistor during the transition to a low output. The power dissipated during switching is usually the power required to charge the capacitance of the subsequent stage and is equal to $C_o V_{DD}^2 f$, where C_o is the output capacitance, V_{DD} is the supply voltage, and f is the operating frequency in Hertz.

The dynamic power consumption increases linearly with increasing frequency and node capacitance. Fig. 4 shows a typical curve of dynamic power dissipation as a function of frequency. At 1 MHz, the dissipation for a simple COS/MOS gate is in the order of 1 mW.



VIN	p	n	VOUT
VSS	ON	OFF	VDD
VDD	OFF	ON	VSS

Fig. 3—COS/MOS inverter

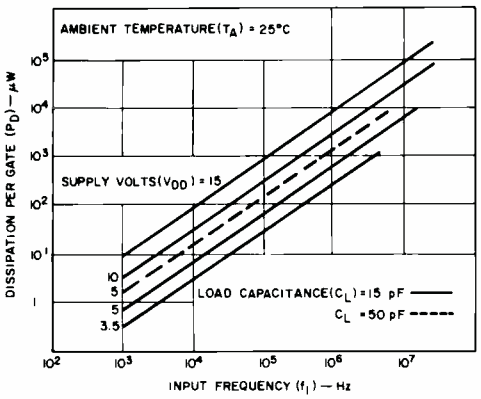


Fig. 4—Typical dissipation characteristics of a COS/MOS gate circuit as a function of frequency.

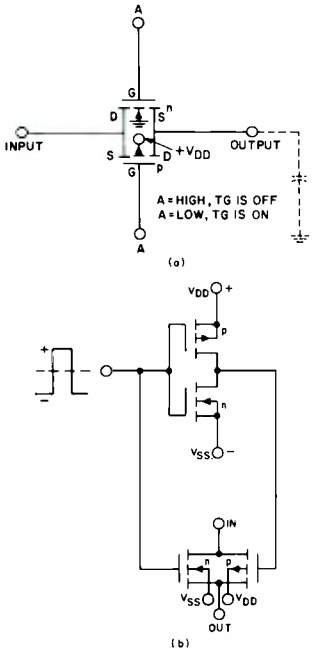


Fig. 5—Transmission-gate circuits: (a) basic COS/MOS transmission gate; (b) combination of transmission gate and inverter to form a basic switching circuit.

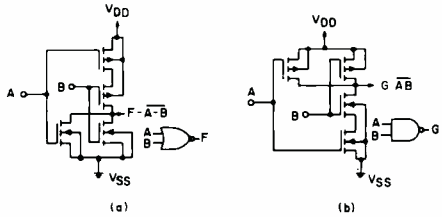


Fig. 6—COS/MOS logic gates: (a) two-input NOR gate; (b) two-input NAND gate.

Transmission gate

The transmission gate, basically, is a single-pole single-throw switch that has a very high off-to-on resistance ratio (typically, in the order of 10^9). This circuit is formed by connecting two complementary MOS transistors in parallel, as shown in Fig. 5a. When the control signals are applied as indicated, the circuit functions as a bidirectional switch and provides either low *on* or high *off* impedance to input signals between ground and $+V_{DD}$. The transmission gate, together with an inverter which provides the appropriate control inputs, is used extensively as a coupling element in latches, flip-flops, shift registers, and counters and to provide a three-state output circuit. It is also used as an analogue switch with high linearity in audio and video switching applications. Fig. 5b shows the combination of a transmission gate and an inverter to form a basic switching circuit.

NOR and NAND logic gates

A NOR gate is formed by connection of two or more paralleled n-channel transistors in series with two or more series-connected p-channel transistors. Fig. 6a shows the circuit diagram for a two-input NOR gate. A negative output is obtained from this gate circuit when either input A or input B is positive. For each condition, the n-channel transistors are turned on and the p-channel transistors are turned off so that the output is connected to V_{SS} (or ground).

A NAND gate consists of two or more series-connected n-channel transistors in series with two or more parallel-connected p-channel transistors. Fig. 6b shows the circuit diagram for a two-input NAND gate. The output of this circuit is low (V_{SS}) only if both inputs are high (V_{DD}), because only in this way are both n-channel transistors turned on to connect the output to V_{SS}.

Multiple-input NOR and NAND gates are implemented by adding more transistors. For instance, a four-input gate would have four n-channel transistors and four p-channel transistors. More complicated devices are composed of many devices. A basic D flip-flop has eight p-channel transistors and eight n-channel transistors, a JK flip-flop has fifteen n-channel transistors and fifteen p-channel transistors, and a static RAM memory cell has two n-channel transistors and two p-channel transistors plus two additional p-channel types for cell selection. In general, the COS/MOS chip area needed for these complicated circuits is considerably less than the area required by the popular TTL technology. For example a COS/MOS D flip-flop cell is 2½ times smaller than the TTL version. Complex COS/MOS circuits with many hundreds of gates on a single chip are being manufactured.

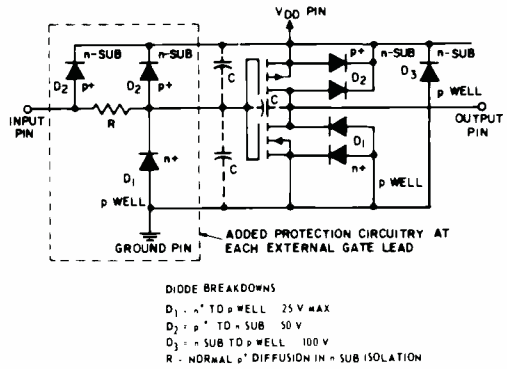


Fig. 7—Input protection circuit used with RCA COS/MOS integrated circuits.

Input protection

The input impedance of COS/MOS integrated circuits is extremely high because of the insulating oxide layer at the gate input. Like all MOS circuits, if a COS/MOS device is out of circuit or if an input is unconnected, a static charge can be built up on the input parasitic capacitance. If the input is allowed to exceed 100 V, the gate oxide layer will be damaged. RCA COS/MOS integrated circuits have a built-in diode protection network at all inputs. This input protection network clamps transient voltages to safe levels. Fig. 7 shows the network used in RCA CD-4000A series devices. The

Table I—Logic characteristics.

Logic type	DC power dissipation (mW/Gate)	Prop delay (nS)	DC noise immunity (V)	DC fan out	Logic swing (V)
RTL	19/5	12	0.1	5	1
DTL	11	30	1	8	2.8
TTL					
74	10	13	1	10	3.3
74L	1	35	1	10	3.3
HTL	44/13	110	6.5	10	12.5
ECL	25	2	0.27	25	0.9
COS/MOS	0.00001	25	45% of V_{DD}	>500	up to 15 V

distributed input resistor provides current limiting and together with the parasitic capacitance of the protection diodes forms an integrating network which slows down very fast transients so that sufficient time is allowed for the protection diodes to perform their voltage clamping function. Normal switching operation of the COS/MOS device is unaffected by this network.

Noise immunity

The complementary structure of the inverter results in a near ideal input-to-output transfer characteristic. The switching point is typically midway (45 to 55%) between the 0 and 1 logic levels. As a result, the inverter has high DC noise immunity because the output does not switch until the input voltage rises to nearly half the supply voltage V_{DD}. This behavior is shown in Fig. 8 for V_{DD} voltages of 5, 10, and 15 V. This figure also shows the insensitivity of the transfer characteristic to changes in ambient temperatures over the range from −55°C to +125°C.

The switching-point voltage depends on the match in the impedances of the n-channel and p-channel transistors rather than on absolute transistor threshold voltages. Transistor characteristics are matched by the design of appropriate size devices and by controlling transistor threshold voltages. Normally, the channel width of p-channel transistors is twice that of corresponding n-channel transistors because of the lower charge-carrier mobility of p-channel types. Fig. 8 shows that, in the typical case, the switching point is maintained at 45% of the supply voltage V_{DD} over the supply range of 3 to 15 V because of this dependence on the matching of the two transistors rather than an absolute transistor threshold.

In production of COS/MOS integrated circuits, a range of maximum and minimum transfer characteristics results among different devices of the same type because of normal manufacturing-process tolerances, as shown in Fig. 9. The actual spread in switching point provides a guaranteed DC noise-immunity value equal to 30% of the supply voltage. Noise immunity increases as the input noise pulse width becomes less than the propagation delay of the circuit. This condition is often described as AC noise immunity. Standard COS/MOS circuits have moderate switching speed (in the order of 35 ns at a V_{DD} of 5 V) and good DC noise immunity; AC noise immunity, therefore, is excellent.

COS/MOS vs. other logic types

The basic characteristics of COS/MOS integrated circuits compare very favorably with those of other integrated-circuit logic families. Table I compares the static power dissipation, noise immunity, and other characteristics of COS/MOS devices with those of other familiar types of digital integrated circuits. A prime advantage of COS/MOS devices, as compared to TTL devices, for example, is low power dissipation. Because the power consumption of COS/MOS devices decreases linearly with frequency, as shown in Fig. 10, these devices offer a considerable power saving for many logic systems in which a large proportion of the logic operates at relatively low frequency.

The wide supply range of 3 to 15 V can allow operation from simple, wide-tolerance, low-current power supplies or inexpensive batteries. In addition, the moderate switching speed avoids many of the noise and transmission line reflection problems associated with faster forms of logic. The high noise immunity is a desirable feature in many applications. In general, these characteristics simplify the design of logic systems and can provide performance improvements in many general- and special-purpose applications.

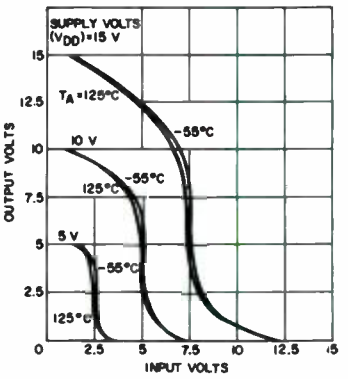


Fig. 8—Typical voltage transfer characteristics for a COS/MOS inverter.

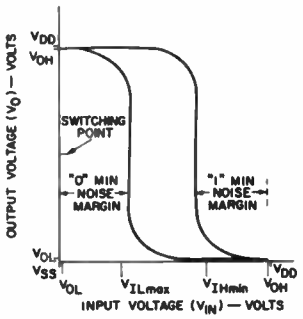


Fig. 9—Minimum and maximum transfer characteristics for a COS/MOS inverter.

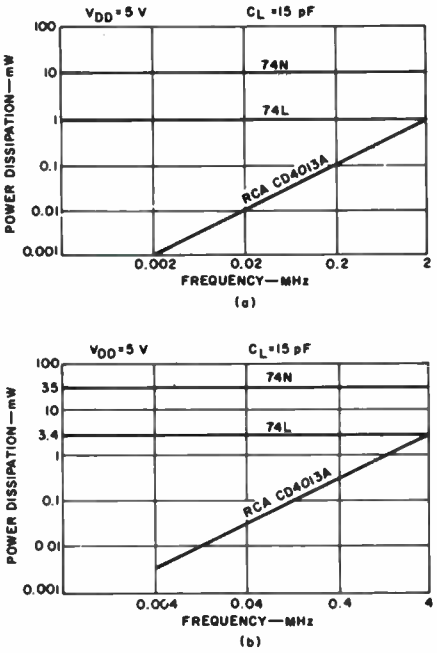


Fig. 10—Speed-power product of COS/MOS and TTL devices: (a) quad gate; (b) flip-flop.

COS/MOS standard-parts line comes of age

R. Heuner

A major advantage of COS/MOS is the ability of the circuit to perform well in single gates and flip-flops as well as in complex MSI and LSI configurations. Much information is available on the unique characteristics and advantages of the COS/MOS circuit configuration.[1,2] This paper illustrates the broad foundation of COS/MOS standard parts and explains why COS/MOS is the correct circuit configuration for such a broad-based line of parts.

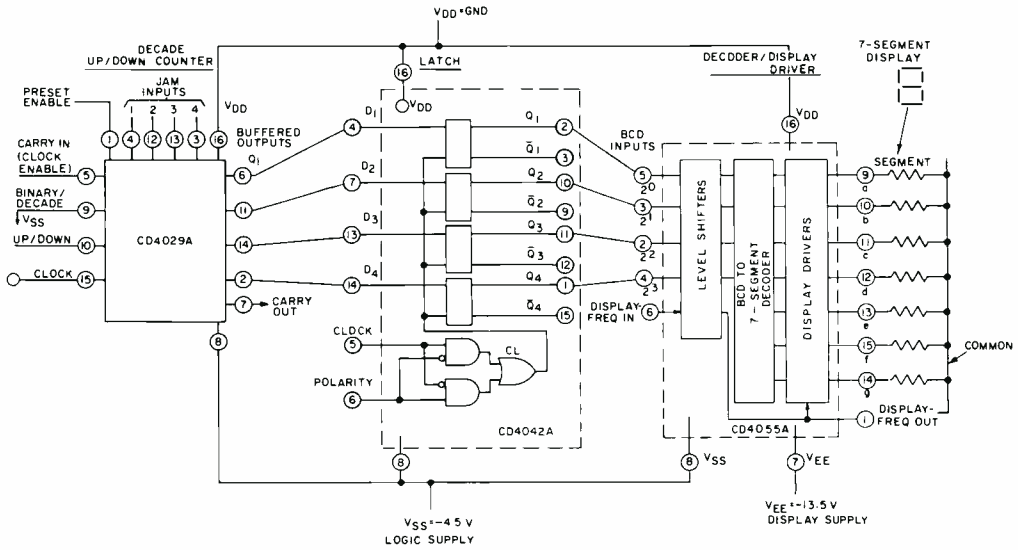


Fig. 1—A general purpose counter/latch/decoder/liquid-crystal-display driver system.

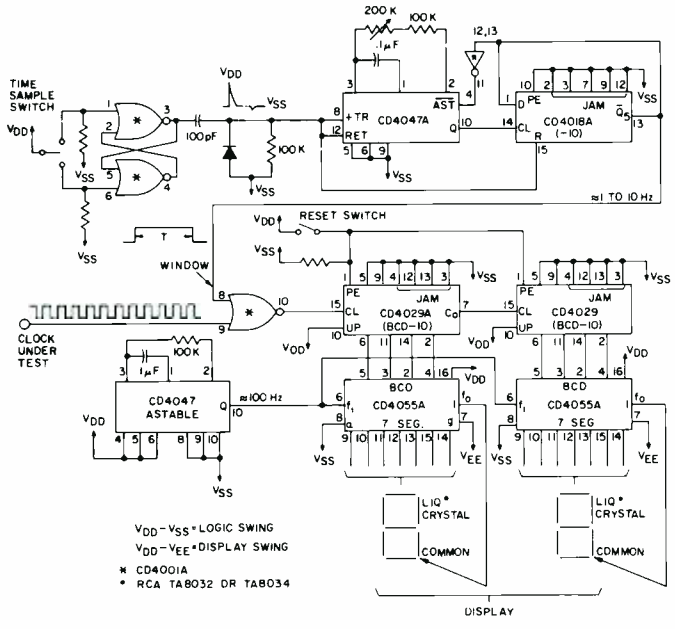


Fig. 2—Functional diagram of a liquid-crystal-display rate indicator.

THE RCA LINE OF COS/MOS standard parts has grown to include 50 commercially announced types with some 20 additional types to be announced over the next quarter. An expanding list of gate, flip-flop, counter, register, and general-purpose subsystem functions make up these 70 types. The availability of standard-part, static-logic, COS/MOS building blocks that operate from a single power supply and that are characterized by V_{DD}-to-GND (1-and-0) signal swings, wide operating-voltage (3 to 15V) and temperature (−55 to +125°C) ranges, high noise immunity (30% of V_{DD}), low dissipation (5 μW typical per MSI package), and high input/low output impedances make COS/MOS circuits ideal for the breadboarding and evaluation of complex system functions. In the final system implementation, such breadboards may serve as the production prototype from which only packaging and form factor are changed or as the basis on which single or multiple COS/MOS custom chips are designed. Many systems, in fact, are finally implemented using a mixture of custom-designed and standard parts. Table I categorizes the available standard parts and indicates major operational characteristics. The contents of the table underscore the capability of the RCA COS/MOS CD4000A line. With COS/MOS, breadboarding, evaluation, and modification of prototype systems before commitment to a final design has become an economic and practical reality. The breadboard circuits act as ideal supplements to computer simulation of dynamic criteria, such as critical speed paths.

Sample subsystem applications

The CD4000A series of standard COS/MOS parts is described in detail in the CD4000A data sheets.[3] Summary information is presented in the quick-reference guides.[4] As a means of illustrating the flexibility of the CD4000A series, a set of sample applications are given below. These samples are not aimed at a particular system use; they do, however, highlight unique features of some of the individual parts and demonstrate overall capability of the combined COS/MOS line.

Fig. 1 illustrates a general purpose

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Table I—COS/MOS "A" series standard-parts family (3- to 15-V operating-voltage range).

Category	Description	Pkg.	Performance/ comments
Basic building blocks			
	CD4007A—dual complementary pair and inverter	14 pin	MOS device evaluation, and basic breadboarding
	CD4016A—quad bidirectional switch	14 pin	Transmission gating, analog switch
Gates			
NOR	CD4001A—dual 3-input NOR + Inverter	14 pin	Micropower quiescent dissipation—0.01 μW (typ.) at 10V Medium speeds—25ns (typ.) at 10V, 15pF loads
	CD4001—quad 2-input NOR	14 pin	
	CD4002A—dual 4-input NOR	14 pin	
	CD4025A—triple 3-input NOR	14 pin	
NAND	CD4011A—quad 2-input NAND	14 pin	
	CD4012A—dual 4-input NAND	14 pin	
	CD4023A—triple 3-input NAND	14 pin	
Other	CD4019A—quad AND-OR select gate	16 pin	
	CD4037A—triple AND-OR bi-phase pairs	14 pin	
	CD4048A—multifunction expandable 8-input gate	16 pin	
	CD4030A—quad exclusive OR gate	14 pin	
Buffers/level converters			
	CD4009A—hex buffer/converter-inverting	16 pin	COS/MOS—TTL level conversion, 2TTL load drive
	CD4010A—hex buffer/converter-non inverting	16 pin	
	CD4049A—hex buffer/converter-inverting	16 pin	Similar to CD4009A/10A with—single supply No supply sequencing requirements
	CD4050A—hex buffer/converter-non inverting	16 pin	
	CD4041A—quad true/complement buffer	14 pin	2TTL load drive high source- & sink-current capability
Flip-flops/latches/monostable-astable multivibrators			
Clocked-master slave	CD4013A—dual "D" flip-flop with set/reset	14 pin	Toggle freq. is 8MHz (typ.) at 10V, 15 pF loads
	CD4027A—dual JK flip-flop with set/reset	16 pin	
Latch	CD4042A—quad clocked "D" latch	16 pin	3-state output capability
	CD4043A—quad 3-state NOR R/S latch	16 pin	
	CD4044A—quad 3-state NAND R/S latch	16 pin	
Monostable/ astable	CD4047A—low-power monstable/astable multivibrator	14 pin	*Astable*—Dissipation = 500μW (typ.) at *f* = 5kHz, 5 volts *Astable/Monostable*—<5% variation in time periods within operating range
Registers			
Static	CD4015A—dual 4-stage serial in/parallel out	16 pin	
	CD4014A—8-stage synchronous parallel in/serial out	16 pin	
	CD4021A—8-stage asynchronous parallel in/serial out	16 pin	
	CD4034A—8-stage bidirectional parallel/serial "D" input/output bus register	24 pin	Enable control Bidirectional signal capability
	CD4035A—4-stage parallel in/parallel out shift register	16 pin	JK serial input
	CD4006A—18-stage static shift register	14 pin	4 or 5 stage sections
	CD4031A—64-stage static shift register	16 pin	Recirculation, delayed clock
	TA5956A—200-stage dynamic shift register (developmental)	16 pin	1-phase or 2-phase clocking

Category	Description	Pkg.	Performance/ comments
Memories			
	CD4036A—4-word by 8-bit random-access NDRO memory-binary addressing	24 pin	Voltage sensing COS/MOS compatible input and output signals
	CD4039—4-word by 8-bit random access NDRO memory-direct word line addressing	24 pin	
	TA6335—256-word by 1-bit random-access NDRO memory with 3-state ouputs (developmental)	16 pin	
Arithmetic functions			
	CD4008A—4-bit full adder	16 pin	Fast carry—45ns (typ.) at 10V, 15 pF loads
	CD4032A—triple serial adder-positive logic	16 pin	
	CD4038A—triple serial adder negative logic	16 pin	
	CD4057A—bit arithmetic array	28 pin	Register on-chip 4-bit 16-instruction capability—arithmetic/logical/count/shift
Counters			
Ripple clocking	CD4024—7-stage binary counter	14 pin	
	CD4040A—12-stage binary counter	16 pin	
	CD4020A—14-stage binary counter	16 pin	
Synchronous clocking	CD4045A—21-stage binary counter	16 pin	Oscillator inverter, dual inverter outputs
	CD4017A—decade counter/divider + 10 decoded outputs	16 pin	
	CD4022A—divide-by-8 counter/divider + 8 decoded outputs	16 pin	
	CD4018A—presettable divide-by-N counter	16 pin	Fixed or programmable divide-by-2 through 10
	CD4029A—presettable up/down counter binary or BCD decade	16 pin	Ripple or parallel carry
Counter + 7 segment display outputs	CD4026A—decade counter/divider + 7-segment display output & display enable	16 pin	
	CD4033A—decade counter/divider + 7-segment display output & ripple blanking	16 pin	
Decoders			
	CD4028A—BCD-to-decimal decoder	16 pin	BD to decimal or binary to octal
Liquid-crystal display decoder drivers	CD4054A 4—line liquid-crystal display driver	16 pin	4-line up-level conversion Separate logic and display supply-voltages permitted
	CD4055A—single-digit liquid-crystal 7-segment decoder/driver with "display frequency output"	16 pin	
	CD4056A—single-digit liquid-crystal 7-segment decoder/driver with strobed-latch function	16 pin	
Multiplexers/analog switches			
	CD4016A—quad bidirectional switch	14 pin	$R_{ON} \simeq 50\Omega$ (typ.) at $V = 15$ volts Permits single-ended control supply and bipolar signal supplies
	CD4051A—single 8-channel multiplexer	16 pin	
	CD4052A—differential 4-channel multiplexer	16 pin	
	CD4053A—triple 2-channel multiplexer	16 pin	
Phase-locked loop/comparator/voltage-controlled oscillator (VCO)			
	CD4046—micropower phase-locked loop	16 pin	*VCO* + 2 phase comparators

counter/latch/decoder liquid-crystal-display driver system using the CD4029A Counter, CD4042A Quad Latch, and CD4055A Decoder/Display Driver. Note that the CD4055A permits use of separate logic and display voltages. Figs. 3 and 4 illustrate digital display applications that utilize the general counting/latch/decoder-display function of Fig. 1.

Fig. 2 shows a functional diagram of a liquid-crystal-display rate indicator. As shown, the reset switch resets the display counters to zero, and the manual time-sample switch allows generation of a time-window T which allows clock input pulses to be counted and displayed. The CD4047A (monostable multivibrator)-CD4018A (programmable counter) combination permits generation of a time-window T well within a 5% accuracy. A variable RC time constant can be used to continuously vary T while the programmable feature of the CD4018A could be used to modify the range of T. The second CD4047A is used as an astable multivibrator to generate an AC (100 Hz) drive signal for the liquid-crystal display. Additional display logic could be added to increase display capability above 99. Additional logic could also be added to make the sampling procedure repeat automatically.

Fig. 3 shows a functional diagram of a liquid-crystal-display time-lapsed meter. The accurate crystal-oscillator time reference is counted down to Hertz and then further divided by using the CD4018A counters of 10 or 6 to obtain

0.1-Hz, 1-minute, 10-minutes, 1-hour, and 10-hour time-pulse rates. A 6-position control switch selects the desired time-pulse-rate input to the counter/latch/decoders display logic. An up/down control switch on the CD4029A permits up counting from 0 to 9 or down counting from 9 to 0 at any of the 6 selectable time rates from 1 second per count to 10 hours per count. In applications in which 5% tolerance is permitted, the CD4047A astable multivibrator may be substituted for the crystal oscillator and initial countdown sections.

Fig. 4 shows a functional diagram of a liquid-crystal-display, reversible, time-lapsed scorekeeper. The scorekeeper is reset and started by placing the start-game switch first in the preset position and then in the start position; the scorekeeper now indicates count 0. Up counting or down counting is initiated by closing team-score switch 1 or 2, respectively. Once up counting or down counting is initiated by a team-score switch, the direction can only be changed by closure of the other team-score switch. The rate of up or down counting can be varied and is established by the frequency setting of the CD4047A astable-multivibrator and the action of the subsequent counting chain comprising three CD4029A decade counters. With the mode switch in the 4-up/6-down mode, the scorekeeper advances up to 4 or down to 6 and then stops until counting is reinitiated through the use of the start-game switch. For example, if the team-1 score switch is closed, the scorekeeper counts down until the team-2 score switch is closed. Upon closure of the team-2 score switch, up counting begins. Subsequently, the direction of counting will be dictated by the last team-score switch closed. If the scorekeeper reaches 4 in the up-counting mode or 6 in the down-counting mode, the display will be frozen and no longer affected by the team-score switches. In other words, a 4 indicates that team 2 wins, and a 6 indicates that team 1 wins.

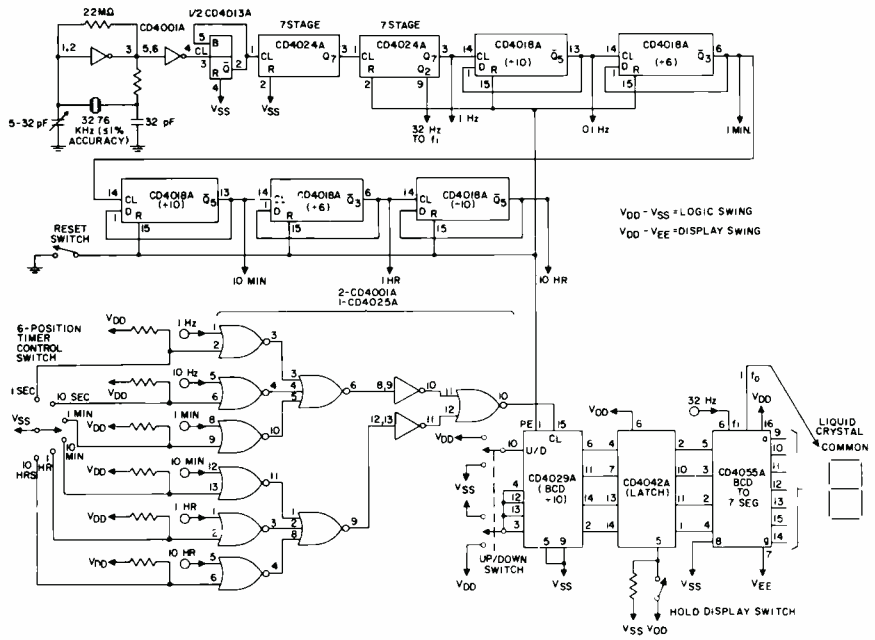


Fig. 3—Functional diagram of a liquid-crystal-display time-lapsed meter.

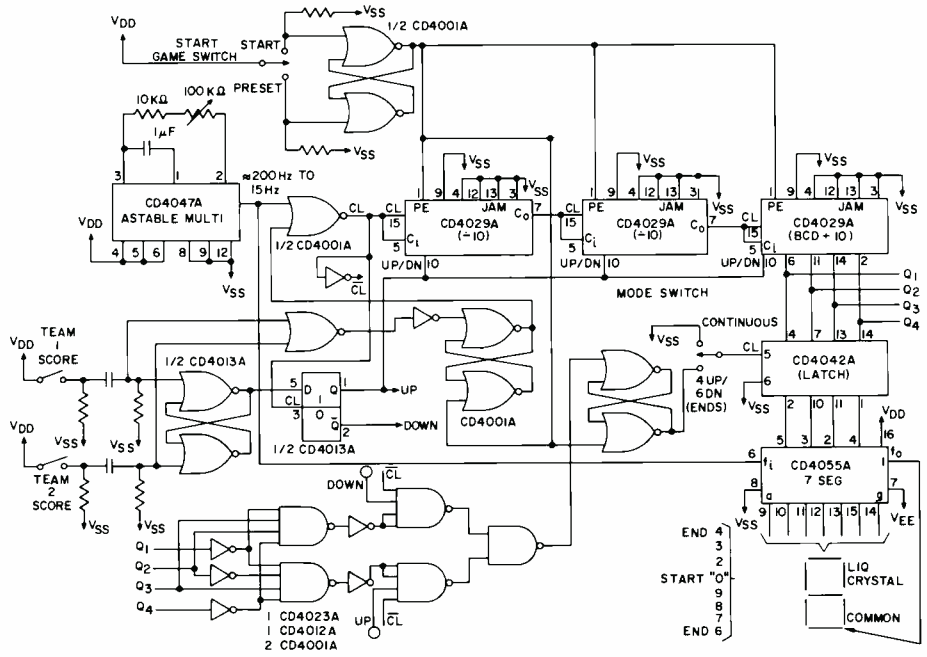


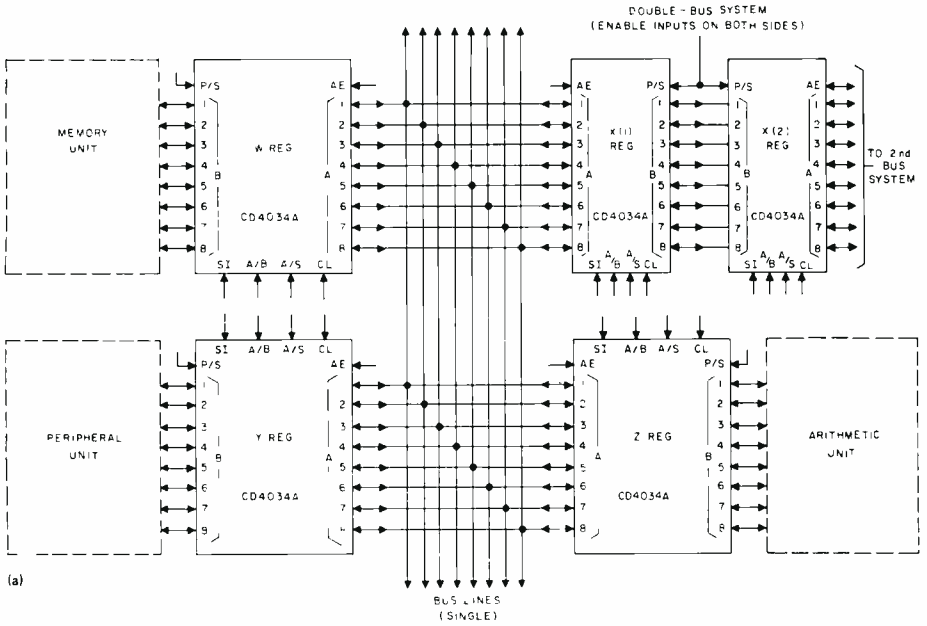
Fig. 4—Functional diagram of a liquid-crytal-display, reversible, time-lapsed scorekeeper.

With the mode switch in the continuous mode, the scorekeeper will not stop, but will continue to run in the direction indicated by the last team-score switch closed. In this case, the indicator will count through 0 to 9 in the up mode and 9 to 0 in the down mode. Therefore, to interpret scorekeeper-indicator meaning, the counting direction must also be observed.

Fig. 5 illustrates the use of the CD4034A (8-stage, static, bi-directional, parallel/serial, input/output bus register) in an 8-line information-transfer bus system. The combined bidirectional and A-enable capability of the CD4034A data lines permit selective information transfers to be made to or from any register to or from any other register linked to the bus system. Additional CD4034A control lines permit parallel or serial (p/s) register operation and asynchronous or synchronous (a/s) parallel data entry.

The simplicity and flexibility of the COS/MOS inverter and transmission-gate functions permit the varied CD4034A modes to be readily realized.

Fig. 6 illustrates the use of the CD4031A (64-stage, static shift regis-



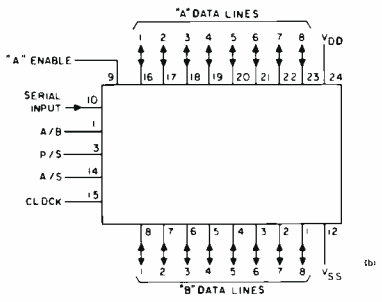


Fig. 5 (above and left)—The CD4034A in an 8-line information-transfer bus system (a) and functional diagram of the CD4034A (b).

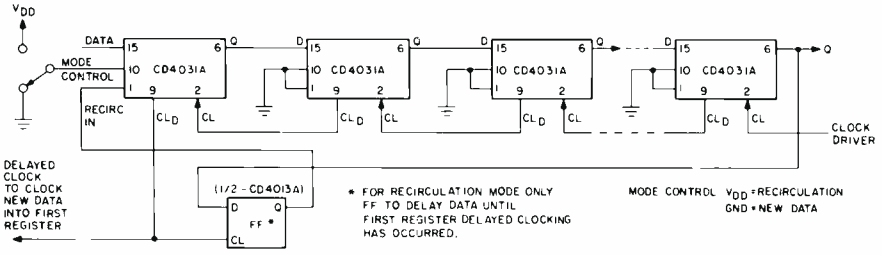
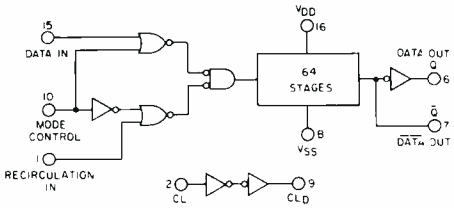


Fig. 6 (below)—The CD4031A in a cascaded shift-register application (a) and functional diagram of the CD4031A (b).



ter) in a cascaded shift-register application. The delayed clock output of the CD4031A permits long register functions to be realized without stringent clock-driver requirements. Note that the clock driver drives only the last CD4031A register package. The delayed clock subsequently drives the previous CD4031A in the cascaded-register system, thus avoiding any possible data race condition.

Note that in applications in which speed dictates, direct clocking of all cascaded CD4031A's may be used.

Fig. 7 illustrates the use of the CD4039A (4-word by 8-bit, random-access, NDRO memory with direct word-line addressing) as a "channel preset memory" in a three-decade, programmable, divide-by-*N* counter/frequency-synthesizer subsystem. CD4039A controls permit counter preset switch information to be stored in memory until requested, or counter states to be controlled directly. All CD4039A inputs and outputs are cos/MOS-voltage compatible, and, hence, require no special driver or output sensing devices. Expansion in both word and bit directions is readily achieved. The CD4036A is similar to the CD4039A but has binary addressing, chip inhibit, and separate read and write lines instead of individual word adress lines.

Fig. 8 shows the CD4046A, a cos/MOS IC containing a voltage-controlled oscillator and two phase comparators, used in a low-power, phase-locked-loop subsystem. The CD4046A typifies the extension of cos/MOS technology to circuits and applications requiring a combination of digital and linear techniques.

Fig. 9 illustrates the CD4051A, single, 8-channel multiplexer, in an analog-switch application in which ± 5-volt analog-input signals are controlled by standard 0-volt to + 5-volt digital address-control inputs. The level-shift capability built into the CD4051A, CD4052A, and CD4053A multiplexer types permits varied amplitude analog swings to be controlled by means of standard single-polarity address-control inputs.

Standard parts under design and potential applications

Cos/MOS standard-parts design has taken two directions: The first is backing and filling the many gate/flip-flop/general-purpose MSI functions that are required to satisfy the myriad of applications now being implemented by cos/MOS circuits. The second is implementing the subsystem functions which constitute the next level of complexity to the general-purpose MSI counters, registers, etc. now available. Design options regarding operating-voltage range are also taking hold, as, for example, in the single-cell-powered IC circuitry in watches.

Evolution in the ripple-carry binary-counter area has moved the 7-stage CD4024A through the 14-stage CD4020A to the 21-stage CD4045A. Watch, clock, and automotive-time requirements have resulted in the CD4045A being layed out with masking options for varied metal and/or voltage-range options or to modify the number of counting stages, output shaping, output drive currents, etc. Some options will eventually be added

to the standard parts line while others will remain custom in nature.

In the analog switch/multiplexer area, the TA6191 has been developed as a low-impedance version of the CD-4016A. The *on* resistance of the TA6191 switch is flat for the entire signal-voltage range and is similar in nature to that of the CD4051A, the CD4052A, and the CD4053A multiplexer circuits.

Fig. 10 shows a functional diagram of a 4-decade, programmable, divide-by-*N*, LSI counter design. This IC is useful in digital frequency-synthesizer applications covering varying frequency ranges as well as in general purpose divide-by-*N* counters. Fig. 11 shows the use of the counter as both the divide-by-*N* and divide-by-*R* counting sections in a VHF frequency synthesizer phase-locked loop. Evolution of the device has progressed from the single-decade CD4018A, presettable divide-by-*N* device, through the CD4029, a BCD presettable up/down version.

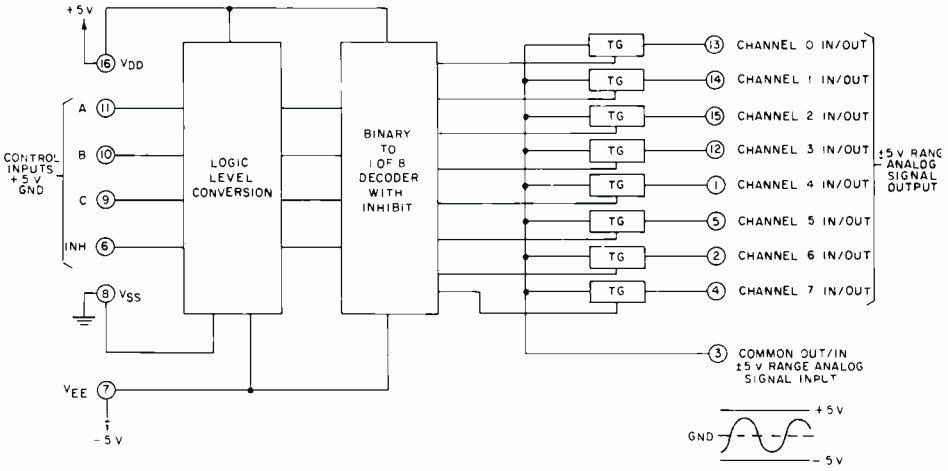


Fig. 9—The CD4051A in an analog-switch application.

Fig. 12 shows a functional diagram of a digital liquid-crystal driver LSI design for watches and clocks. The logic will operate below 1.4 V with display voltages in excess of 15 V. Evolution of the driver has progressed from the 7-segment CD-4026A, CD4033A counter types through the CD4029A counter and CD4054A, CD4055A, and CD4056A liquid-crystal drivers used in various prototype timing applications.

Conclusion

In 1967 RCA was the only supplier of commercial COS/MOS parts. The standard line consisted of seven parts, the most complex of which was a 125-

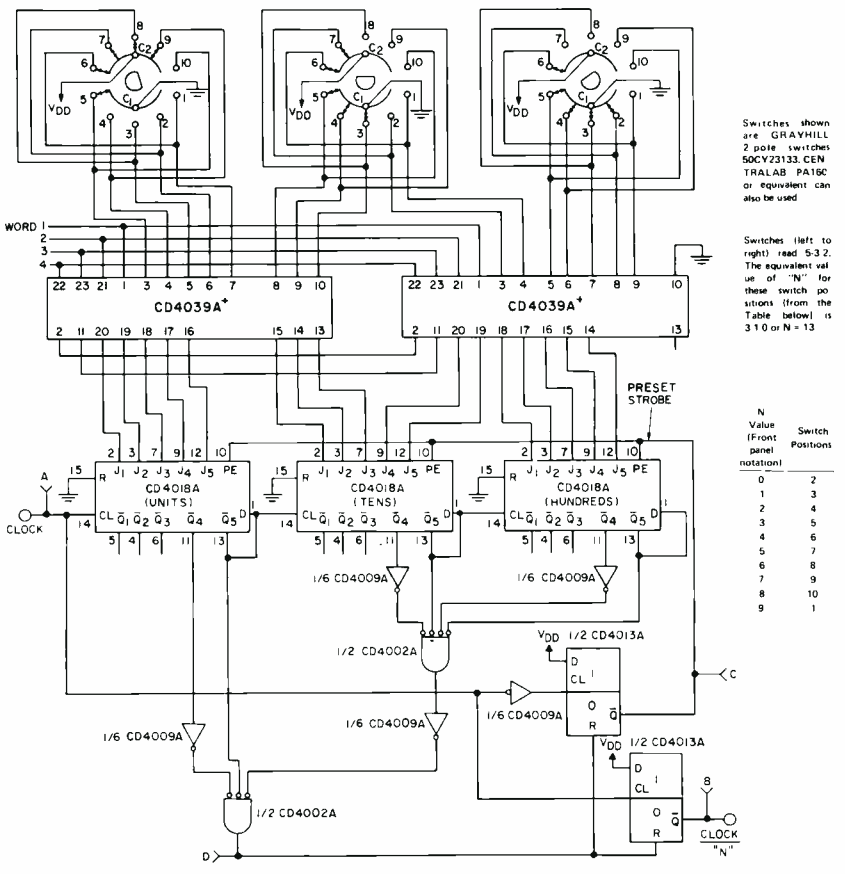


Fig. 7a—The CD4039A used as a "channel preset memory" in a three-decade programmable, divide-by-*N*, counter/frequency-synthesizer subsystem.

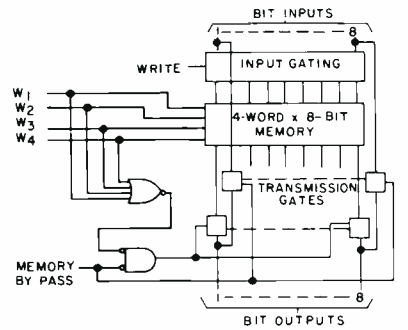


Fig. 7b—Functional diagram of the CD4039A.

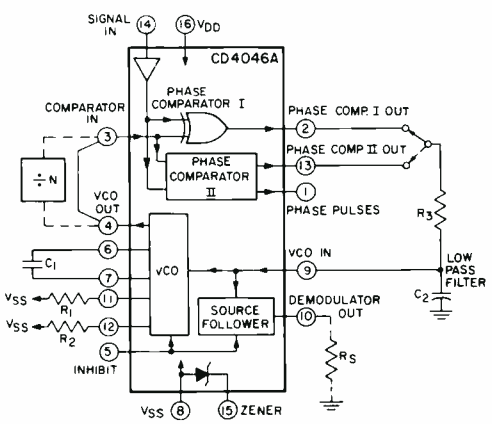


Fig. 8—The CD4046A in a low-power, phase-locked-loop subsystem.

device 7-stage counter. Annual sales volume was less than $1 million. Applications were limited to military, portable systems. No second sources existed and customer reaction to cos/MOS was skeptical.

In 1972, there are seven commercial suppliers of cos/MOS. Standard parts available total aproximately sixty, and this number is increasing rapidly. Custom parts are as numerous as standard parts; the complexity of both standard and custom types is approaching 2000 devices. Industry sales volume is estimated at about $15 million. Second sources are actively climbing aboard and customer interest is overwhelming in both standard and custom-chip areas. Applications have expanded to include practically all equipment where portability and power dissipation are factors: watches, wall clocks, medical electronics, paging systems, automotive metering and controls, industrial applications where noise immunity is important, and many DTL/TTL- and p-MOS-oriented systems in which cost and simplicity are the sole considerations.

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2. *COS/MOS Digital Integrated Circuits*, RCA Solid State DATABOOK Series, SDD203A, (1973)
3. RCA CD4000A—Series Data Sheets
4. RCA COS/MOS Quick Reference Guide, COS-278B, 1972

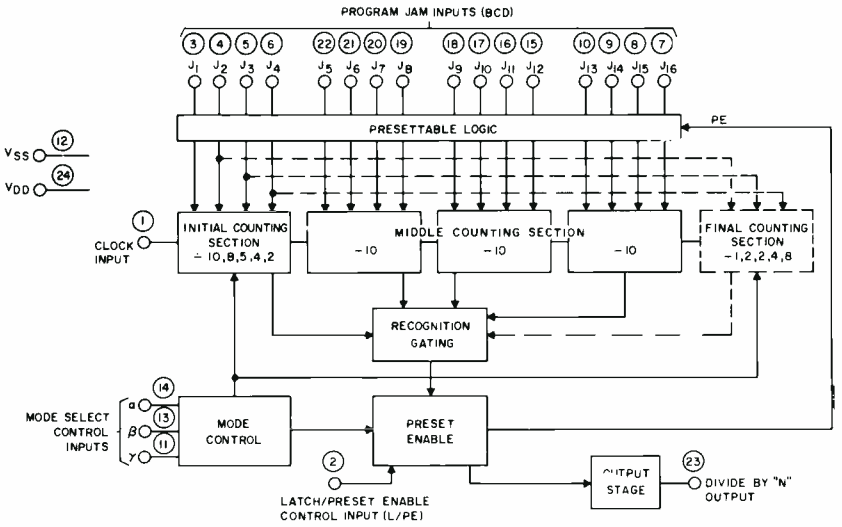

Fig. 10—Functional diagram of the TA6006, a 4-decade, programmable, divide-by-*N*, LSI, counter design.

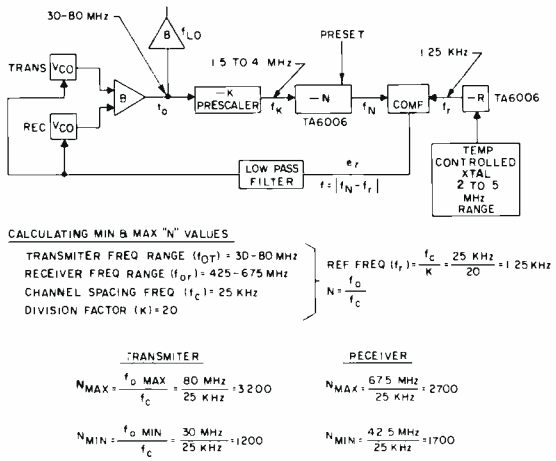

Fig. 11—The TA6006 as both divide-by-*N* and divide-by-*R* counting sections in a VHF frequency-synthesizer phase-locked loop.

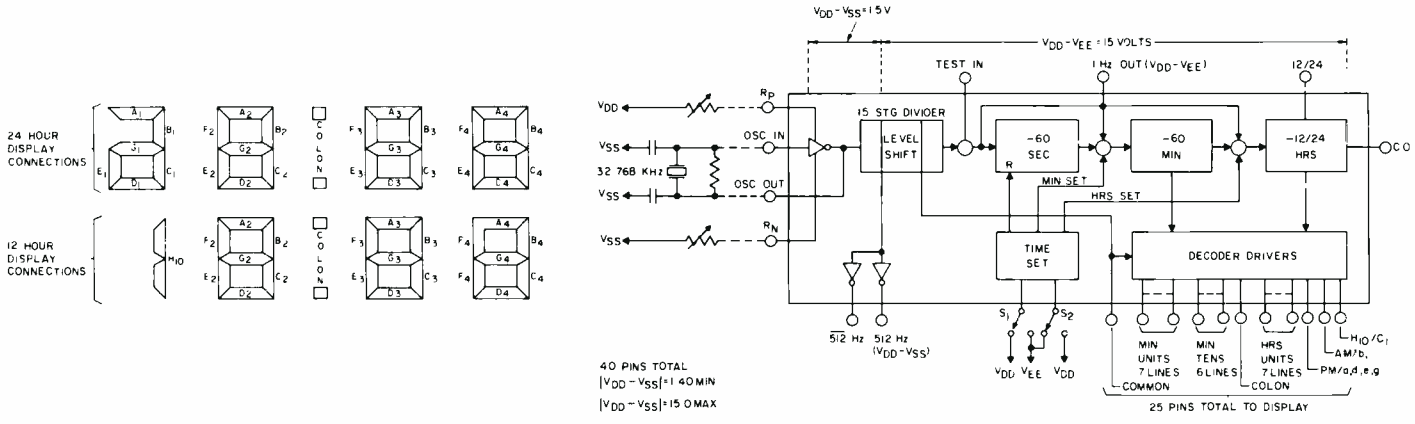

Fig. 12—Functional diagram of the TA6343, a digital, liquid-crystal, watch-display driver.

COS/MOS simplifies equipment design

R. E. Funk

Five characteristics of COS/MOS are of major importance to the logic-system designer: current-drain and power-consumption; input characteristics; switching-transfer performance; output characteristics; and switching-speed. These characteristics are discussed in detail. Specific values and ranges are given; value variations with temperature, power supply, and capacitive loading are also given. The broad range of system-applicable COS/MOS characteristics is illustrated with reference to quantitative data gathered on a random selection of COS/MOS NAND gates—gates that were selected from a variety of manufacturing lots. The quantities given are not necessarily the data-book minimum/maximum limits for NAND-gates, but they do represent the COS/MOS product line.

IT IS COMMON to hear a COS/MOS user state, "Your COS/MOS makes my system design job too easy." After years of rigorous equipment design using bipolar integrated circuits, the logic designer now has a set of complementary-MOS digital integrated circuits that truly make his job almost too easy compared with TTL. Table I illustrates why COS/MOS logic-system design is so easy. For example, note the fanout of 1,000 rather than less than 10, and the switching-spike generation of under 3 mA instead of 40 mA or more. Note also that it is possible now to design a multivibrator with an input impedance greater than 1,000 megohms rather than the less than 5,000 ohms of TTL logic. Consider too all those industrial and automotive applications in which a switching-noise immunity of 30 to 45% of the power supply is needed rather than less than 20%. And not to be forgotten is a gate current drain of 1 nA rather than the 2×10^6 nA of TTL gates, and a power-supply regulation of 3 to 15 V rather than a very tight 4.5 to 5.5 V.

System design with MOS wasn't always easy; for example, commercial MOS started with single-channel p-MOS back in the mid sixties. What happened then

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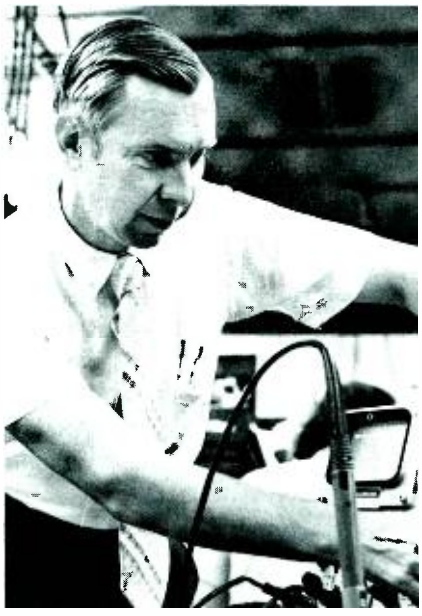

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received the BSEE and MSEE from Drexel Institute of Technology in 1956 and 1961 respectively. Mr. Funk initially joined RCA as a co-op student in 1953 and designed circuits for Airborne Radar Systems in Camden. He specialized in analog-computer circuit design from 1956 to 1959. In 1959 he began his digital-logic design career with responsibility for Data Link system logic in the era of RCA 2N404 discrete logic. In the early 1960's Mr. Funk was responsible for high speed code-generator logic design for real time digital communication systems. In the mid 1960's, he employed saturated logic digital IC's in Minuteman modular test systems. Between 1966 and 1970, he was responsible for logic and circuit design for digital frequency-synthesizer and control functions in the Defense Communications Systems Advanced Technology section in Camden. In 1968, Mr. Funk began working closely with Electronic Components, Somerville, in pioneering use of the new ultra-low-power RCA COS/MOS logic for the next generation of man-pack and hand held radios. In early 1970, Mr. Funk joined the Solid State Division as a group leader in application of MOS IC's.

Table I—Comparison of COS/MOS with bipolar digital logic circuits.

Characteristic	*COS/MOS*	*Bipolar (TTL)*
Fan out	>1000	<10
Switching spike generation	<3 mA @ 5 V	>40 mA @ 5 V
Power supply		
—Regulation	3 V to 15 V	4.5 V to 5.5 V
—Gate drain (DC)	1 nA	2×10^6 nA
Input impedence	>1000 megohms	<5 kHz
Switching voltage noise immunity	30 to 50% of V_{DD}	10 to 20% of V_{DD}

was that the system designer jumped from the rigors of bipolar logic right into the nightmare of system design with p-channel MOS which required not one but two power supplies, and not a nice +5 V but a nasty −12 or −28 V. Interfaces of p-MOS with bipolar logic usually required a third power supply and external pull-up resistors. Also, p-MOS logic presented the designer with two-phase clocked logic with plenty of system overhead cost. It was soon determined that although p-MOS offered good packing density on a semiconductor chip and was easy for the semiconductor manufacturer to make, it presented no end of frustration for the users. Now, for the first time, digital-equipment designers have a digital-circuit semiconductor technology that puts the burden on the chip through, not one, two, or three, but several outstanding characteristics.

Current drain and power consumption

Quiescent (leakage) current

Fig. 1 shows the 15-V leakage-current population of 100 CD4011A units; actual values range from as low as 1 pA to 47 nA. The figure shows that the leakage current has its major population for values under 100 nA, i.e., 67% of the units tested. Production test equipment resolution limits the commercial data maximum to 100 nA. This quiescent current is the standby current of a quad COS/MOS NAND gate when not switching. It is the same quiescent condition under which four normal-power TTL gates would draw 8 mA at 5 V or a low-power TTL quad-gate IC would draw 800 μA. Thus, typical COS/MOS devices draw 8 million times less current than a low-power TTL gate. It is not very hard to understand why COS/MOS is truly ultra-ultra low power. The leakage current is measured by placing a picoammeter in the V_{SS} or ground-return line; all gate inputs are tied to either the positive power supply or ground, respectively, to get the maximum leakage current.

Since leakage current results from leakage of back-bias junction diodes or surface leakage across MOS transistors that are non-conducting, the quiescent current rises rapidly with rising temperature as shown in Fig. 2. In the figure, the current drain for a 4-NAND-gate unit with a leakage current of 3 nA at 25°C is plotted at 5, 10, and 15 V for temperatures ranging from −55°C through 125°C. Fig. 2 indicates that the quiescent current increases to 330 nA at 125°C; the current doubles approximately every 11°C, a useful rule of thumb to remember.

The leakage current of an MOS device can be a good indicator of quality and long life. For this reason, leakage-current limits and shifts are critical in high-reliability products. Measurements of leakage current are taken before and after a 125°C burn-in, and the amount of change is computed. For a NAND gate, allowed movement is 10 nA for MIL-STD-38510 qualified parts.

Switching current

When a COS/MOS device switches, it goes through a transition region in which both p-MOS and n-MOS transistors are *on* simultaneously; a transient current curve is shown in Fig. 3. Minimum/maximum switching current is plotted for 5, 10, and 15 V. For 10 V, when each MOS transistor has a gate-to-source bias of 5 V, the minimum current drawn from the power supply is 1.25 mA for a 100-unit sample, and the maximum current is 2.95 mA; the mean value of the current is 1.92 mA. This is certainly a lot less than the 40-to-100 mA peak switching current drawn by a TTL device at only 5 V.

Fig. 4 shows the peak switching current drop as temperature rises from —55°C to +125°C, just under the typical 0.3% per °C called out in the COS/MOS data bulletin.

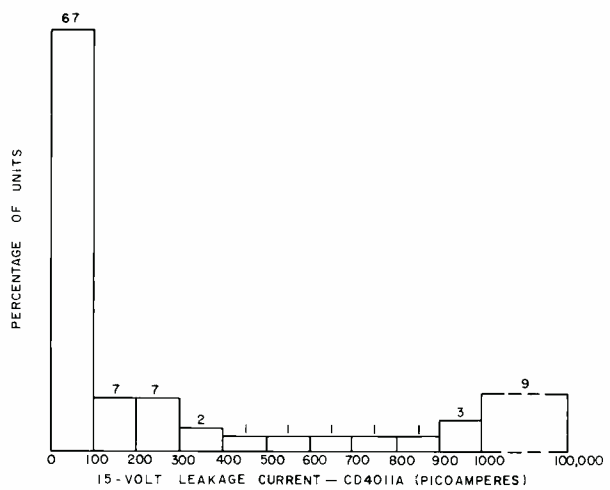


Fig. 1—NAND-gate leakage-current population.

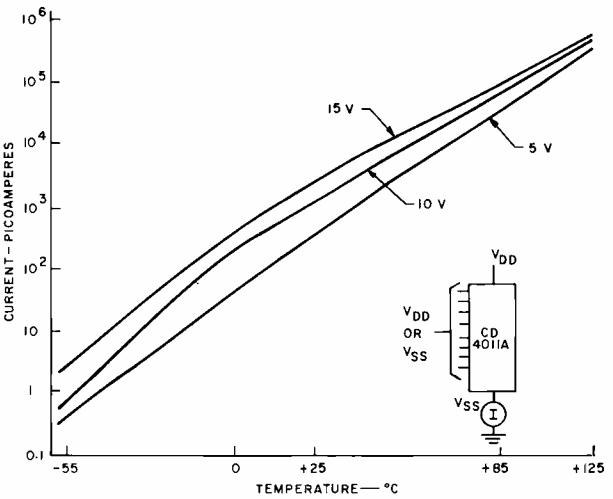


Fig. 2—Leakage current *vs* temperature.

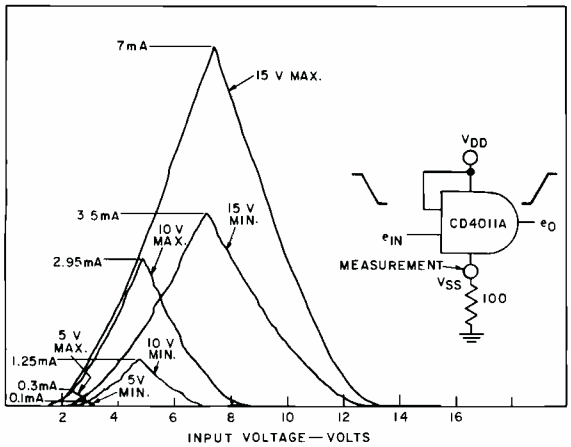


Fig. 3—Switching current.

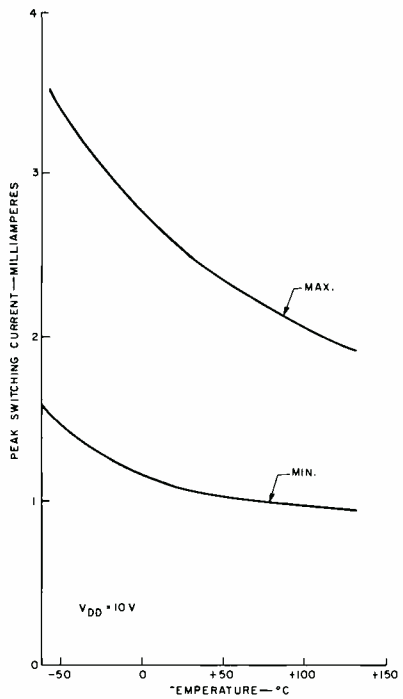


Fig. 4—Peak switching current *vs* temperature.

Dynamic power consumption

Since a COS/MOS device does draw a few milliamperes when it switches, measurable power consumption in a COS/MOS digital system is primarily a function of dynamic switching frequency and loading capacitance; COS/MOS draws a succession of peak switching currents. The integral of these peak switching currents is the average dynamic current drain, the average dynamic power consumption of the COS/MOS device is this current multiplied by the voltage. Fig. 5 illustrates published typical dynamic power consumption for the COS/MOS NAND gate (D4011A). The curves closely approximate $P = CV^2$, where C is the total output-node capacitance; V is the power-supply voltage, and f is the output frequency. Dynamic power consumption (Fig. 5) holds for input rise and fall times up to approximately 100 ns. However, as the input rise or fall times increase beyond 100 ns, particularly at higher voltages, a higher current drain is expected because the devices are dwelling longer in the region in which both the p-MOS and n-MOS devices are *on*. Fig. 6 illustrates this condition where, for 10-kHz operation, current drain goes from a low of 3 μA at less than 100 ns up to 100 μA for a 10-μs transition time at the input. The dotted curve in Fig. 6 shows that for 125° operation the dynamic consumption is extremely close to +25°C ambient curve. The proximity of the curves illustrates another important COS/MOS characteristic: dynamic power consumption is essentially constant with changes in operating temperature. The lower curve in Fig. 6 illustrates another very important factor: as the device threshold voltage is approached, the increase in power consumption is substantially less for the longer input rise and fall times.

This concludes what the equipment designer has to know about COS/MOS characteristics to specify or design a small, low-cost power source. To summarize:

1) Standby quiescent currents are extremely low, nanoamperes per gate or a few milliamperes per system;
2) The power source is going to be called upon to draw small peak switching currents that are only 2 or 3 mA per gate in most cases,
3) Dynamic power is going to be well below 1 mW per gate up to approximately 1 MHz.

All the difficulty has vanished from the power-source design whether it be a battery or a simple half-wave rectifier from a 60-Hz source. The designers of high-quality power supplies simply aren't going to be taxed on COS/MOS digital equipment designs.

Input characteristics

Input current

Measured device input current for 38 test devices ranges from a low of 1.5 pA to a high of 280 pA. Fig. 7 is a histogram of the input current measured at 15 V for the 38 representative NAND gates. The population is peaked at less than 10 picoamperes. Fig. 8 shows the increase in input current for one device (as temperature is varied from −55°C up to +125°C). With an input current of 10 pA for 15-V operation, input resistance is typically 1500 megohms. This very high input resistance gives the equipment designer a wide

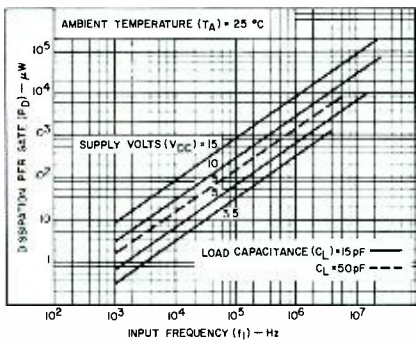


Fig. 5—Dynamic power consumption.

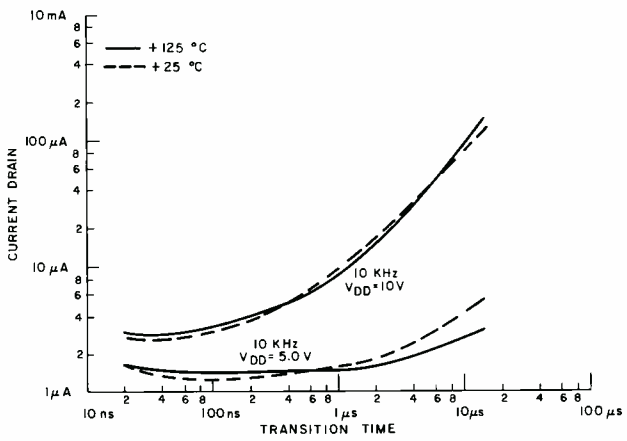


Fig. 6—Current drain *vs* input rise and fall time.

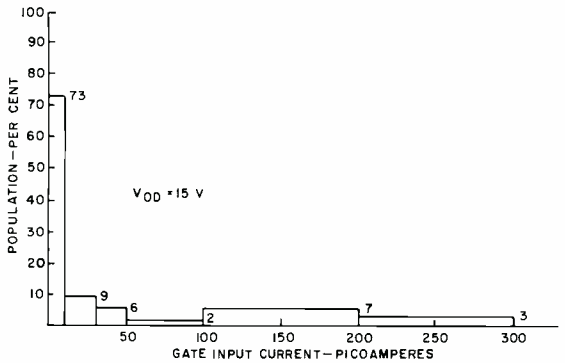


Fig. 7 (above)—Histogram of gate input current.

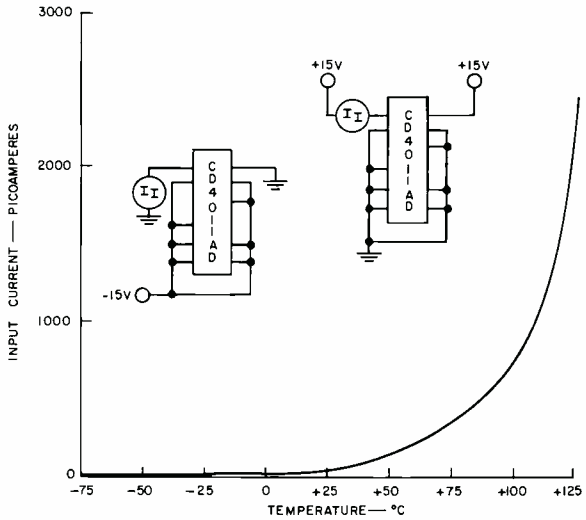


Fig. 8 (right)—Input current *vs* temperature.

choice of time-constant component values in designing RC delays, one-shots, or astable multivibrators. The high input impedance facilitates the design of phase-lock loops, Schmitt triggers, and other linear circuits. The high input impedance is also a big plus for cos/MOS compared with bipolar logic, the old-fashioned kind of logic device which has an input impedance of less than 10 kilohms.

Input capacitance

Fig. 9 is a plot of cos/MOS input capacitance versus temperature; shown is a minimum input capacitance of 4.24 pF at +25°C and a maximum of 5.3 pF. The range of expected input capacitance is narrow and is indeed very flat with temperature. The typical input capacitance of 5 pF noted in the RCA cos/MOS data bulletins is a reliable design guide. The cos/MOS system designer, if he knows precisely the input capacitance and the fixed wiring capacitance, can add 5 pF per cos/MOS input (load) to determine total output-node capacitance, a critical factor in estimating device speed. Speed is discussed further below. The input capacitance is not flat because the input voltage varies as a result of the effect. Fig. 10 shows that the input capacitance can increase from 4.2 pF up to 11.5 pF as the input is switched through the 5-V transition point.

DC switching (voltage-transfer) characteristics

Fig. 11 shows the cos/MOS switching characteristics for 3, 10, and 15-V operation. Notice the symmetry and the high noise immunity, *i.e.*, how the devices switch at approximately 45% of the power-supply voltage. These characteristics were plotted at 25°C and represent the minimum/maximum characteristics for 38 randomly sampled NAND gates. Published data guarantees switches between 30 and 70% of the supply voltage. Close examination of these curves shows that cos/MOS devices can be operated over a wide power-supply voltage range. Satisfactory switching is solely dependent upon overcoming the threshold voltage of the n- or p-type devices and not upon DC-bias consideration, as in bipolar logic or single channel (p-MOS) logic. The curves of Fig. 11 are skewed slightly to the lower voltage range; *i.e.*, the range of switching characteristics is between approximately 4 and 5.5 V for a 10-V supply because the n-channel thresholds tend to be less than the p-channel thresholds. The stability of cos/MOS DC transfer characteristics is outstanding. For example, as the temperature shifts from −55°C to +125°C (a 180° rise) the DC switching characteristic of the 38 units shifted a mere

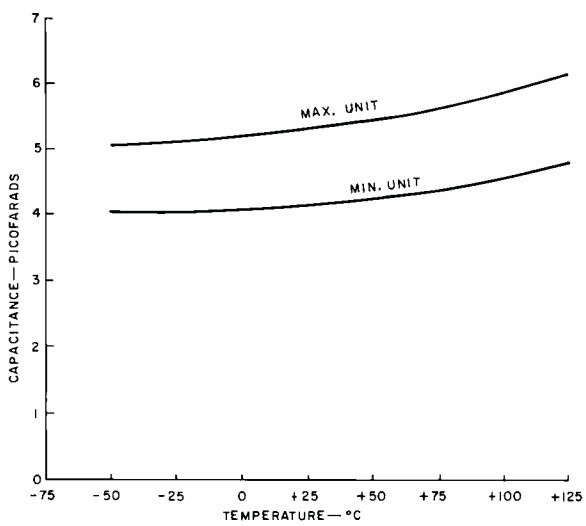


Fig. 9—Input capacitance *vs*. temperature.

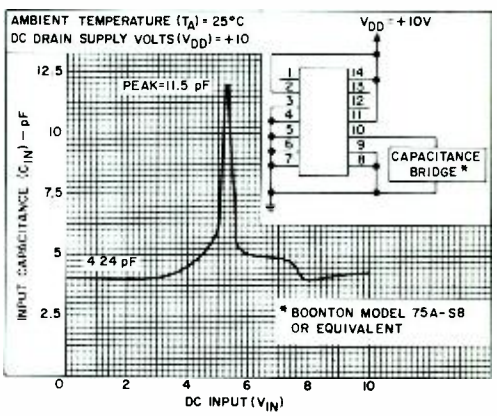


Fig. 10—Input capacitance *vs* input voltage.

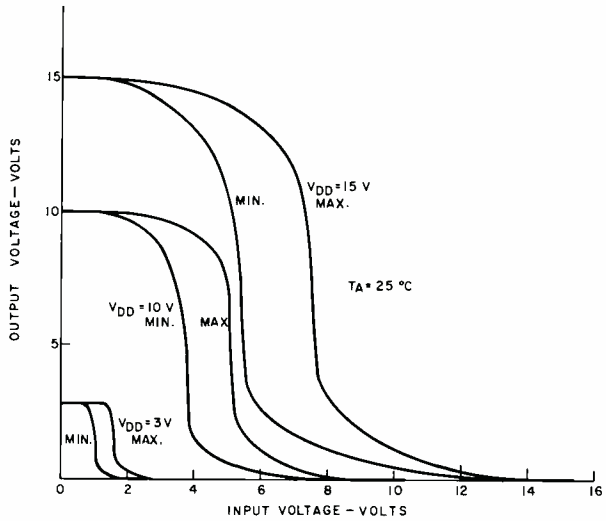


Fig. 11—Switching transfer characteristics *vs* supply voltage.

70 mV to the left. In the published data sheets a conservative 200 mV of shift is indicated.

Output characteristics

Output current

A legitimate question might be, "What use are output-current considerations when the input (load) current of a device is a few picoamperes when driving other cos/MOS devices?" The answer is that, in order to achieve reasonable speed, sufficient output current is required to charge and discharge the load capacitance. Thus, it is valuable to know the output source- and sink-current capability. Also, since cos/MOS can operate at 5 V, a designer must know about the interface of cos/MOS with other logic forms, such as TTL; output drive current is of great interest in this respect.

Figs. 12 and 13 show, respectively, the minimum and maximum n-device and p-device drain characteristics for the 38 sample NAND-gates. Minimum and typical output sink and source current is specified in every cos/MOS data sheet. By using these characteristics, the designer can choose his output voltage drop for a given load current. The current available for directly driving the base of a p-n-p or n-p-n bipolar transistor or for sinking inputs to DTL or TTL can then be determined. Output source and sink current typically drops off 0.3% per °C.

Output capacitance

The output-node capacitance of the CD4011A NAND gate ranges from 2.13 pF to a maximum of only 3.5 pF in the 38 devices when measured at 25°C with a 10-V supply. The ranges of input and output capacitance are very narrow for cos/MOS devices.

Switching speed

Switching-speed characteristics are explained in terms of propagation delay and transition time for NAND gates. In switching-speed tests, input rise and fall times are 20 ns. Propagation-delay measurements range from the 50% point of the input to the 50% point of the output, and rise and fall times as well as transition times are measured from 10% to 90% of the voltage transition. Fig. 14 shows the decrease of the propagation delay as the power-supply voltage is increased from 5 to 15 V. The figure illustrates that speed can be altered by choosing the power-supply voltage, when power dissipation is to be minimized through the use of the lowest possible power supply consistent with a given desired speed. The generated switching current transients are minimized in the system, thereby improving its noise immunity. At 10 to 15 V, the NAND gates operate in the 15- to 25-ns switching propagation-delay area; this time is sufficiently fast for 70% of all digital equipment. The range of propagation delay at a 5-V power supply for the 38 devices is 30 to 60 ns. Fig. 15 shows the increase in propagation delay as the total output capacitance ranges from 15 to 100 pF; at 100 pF, propagation delay is 86 ns with a 10-V power supply at 25°C. Thus, it is very easy to increase propagation delay by adding 20 to 30 pF to the output mode of a cos/MOS device. A great deal more capacitance would have to be added to slow down a bipolar type of digital circuit. Fig. 16 demonstrates a 22% increase in propagation delay as tem-

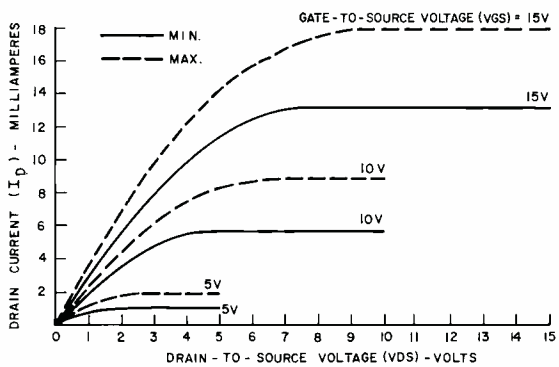


Fig. 12—Drain current characteristic for the CD4011AD; gate-to-source voltage is 15 V.

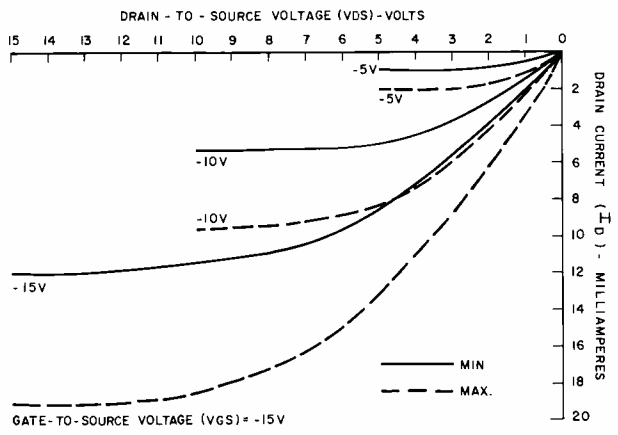
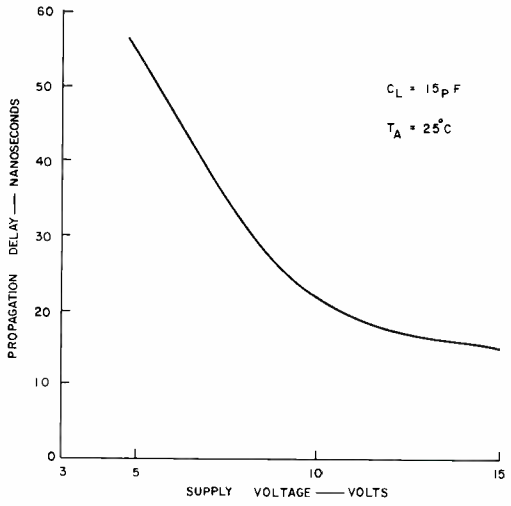


Fig. 13—Drain current characteristic for the CD4011AD; gate-to-source voltage is 15 V.



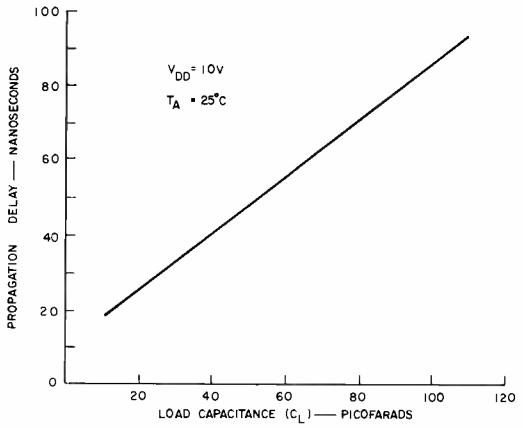


Fig. 14 (left)—Propagation delay *vs* supply voltage. Fig. 15 (above)—Propagation delay vs load capacitance.

perature is increased from 25°C to 125°C. This increase of propagation delay is caused by the drop off of the gain or the g_m of MOS transistors.

Fig. 17 is a plot of transition time versus supply voltage. Note that for 10-V operation, the transition time of the given device is 28 ns, the propagation delay for this same device is 23 ns. When transition time exceeds propagation delay, as in COS/MOS logic circuits, the inherent system noise immunity is much improved over the same system using TTL where propagation delays are greater than transition times.

What can be deduced from the switching characteristics of COS/MOS devices? First, COS/MOS devices are fast, but not so fast that noise generation becomes a problem. Second, fast operating rates, 15 to 20-ns propagation delays or 5- to 10-MHz clock rates, can be obtained with a 15-V supply. Third, by operating in the 3- to 5-V range, power dissipation can be minimized while clock speeds are maintained in the 200-kHz range. It should be added here that lower-threshold silicon-gate COS/MOS devices will operate at much higher speeds for low-voltage operation. SOS complementary-MOS logic will operate considerably faster as a result of the absence of substrate capacitance effects.

Summary

TTL may have outstanding speed/power characteristics; it is indeed difficult to match 50 MHz for a gate at 50 mW power dissipation, but that's about all TTL has to offer. The advantage of P-MOS is not really in characteristics at all but in the economy realized through its high packing density. However, this feature is used only in a limited number of large machines in which multiple power supplies, low output drive, and multiple clock phases required by TTL can be tolerated. On the other hand, the ultra-low and very loose power-supply requirements, the typical 45% noise immunity (45% of the power supply) that can only be matched by the high power MSI-limited high-threshold bipolar logic, and the high ratio of input-to-output resistance must all be listed as outstanding characteristics of devices produced through the use of COS/MOS technology. The significance of these characteristics can be summed up in three words of great importance to the designer: *simplified equipment design.*

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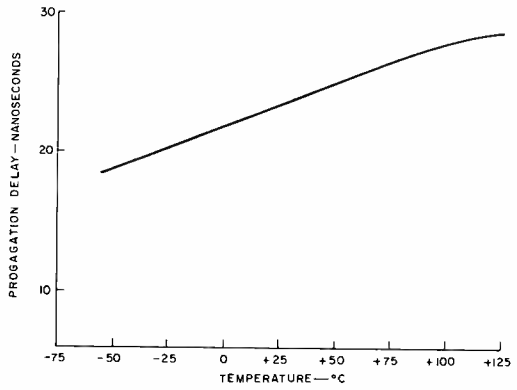

Fig. 16—Propagation delay *vs* temperature.

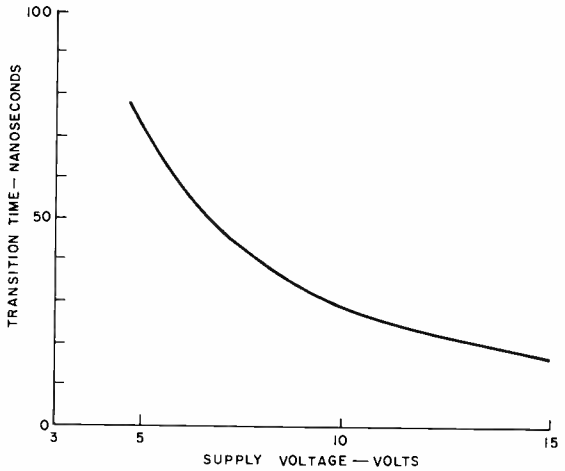

Fig. 17—Transition time *vs* supply voltage.

Development of COS/MOS technology

T. G. Athanas

Developments during the past few years have substantially alleviated the extreme difficulty that previously characterized monolithic fabrication of complementary MOS transistors; reliable and economical COS/MOS integrated circuits are now readily produced in large quantities. This paper explains basic design and processing of COS/MOS integrated circuits and the recent technological advances that have made these circuits a production reality with an assured bright future in solid-state circuit applications.

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received the BS in Engineering Physics from Tulsa University in 1957. He attended Oklahoma University in 1957-58 as a graduate assistant before joining the RCA Semiconductor Division in June 1958 as a Design Engineer in the Commercial Design Department. His projects included germanium alloy audio transistors, germanium alloy-drift transistors covering the audio, RF, FM, and VHF frequency ranges, and germanium, UHF, stripe mesa transistors. In January 1964, Mr. Athanas joined the MOS transistor activity and was responsible for developing several MOS devices for switching and amplifier applications. In January 1969, he joined the COS/MOS IC design and technology group where he was responsible for the development of low-voltage technology. In his present position, Mr. Athanas is responsible for the development of the silicon-gate, LSI silicon interconnect, and COS/MOS beam-lead processes. He has published on the subject of low-voltage COS/MOS technology, and holds five U.S. patents on MOS technology with several others pending

COMPLEMENTARY-SYMMETRY/METAL-OXIDE-SEMICONDUCTOR (COS/MOS) integrated circuits offer well-known advantages, such as negligible power dissipation and an inherent high noise immunity, that have led to the increasingly wide-spread use of these devices, particularly in digital circuitry. The successful emergence of COS/MOS devices as practical and highly effective circuit elements is directly attributable to several breakthroughs achieved at RCA Solid State Division during recent years. For example, recent technological advances have made possible oxide and metal layers that are free of positive-charge (sodium) impurities and uniform low-concentration diffusions that can be reliably and precisely controlled. These developments have greatly facilitated achievement of the low values of threshold voltage that are essential for operation of COS/MOS devices from low supply voltages.

The ability to operate from low supply voltages is particularly important when COS/MOS devices are directly interfaced with other integrated-circuit logic families, such as DTL and TTL types. In such applications, COS/MOS devices are required to operate from a supply voltage V_{DD} of less than 5 V. Low threshold voltages are also beneficial when COS/MOS devices are operated from a single-cell battery supply. For this type of operation, threshold voltages of less than 1.0 V are required for both n-channel and p-channel transistors. An additional benefit of low threshold voltages in COS/MOS integrated circuits is that increased switching speed can be obtained at higher supply voltages.

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In the evolution of COS/MOS technology, the basic low-voltage process has been augmented by more recent developments, such as the silicon-gate, LSI silicon-interconnect, and beam-lead processing techniques. The successful effort to make these new processes compatible with the basic low-voltage process has resulted in the efficient and speedy implementation of them into the overall COS/MOS manufacturing process.

Basic COS/MOS design considerations

COS/MOS integrated circuits consist mainly of enhancement types of n-channel and p-channel MOS transistors. The enhancement type of MOS transistor does not normally conduct until a voltage of sufficient magnitude and correct polarity is applied to the gate electrode. The voltage applied to the gate electrode must exceed some threshold value in order to create a conduction channel between the source and drain electrodes.

Threshold voltage

The threshold voltage V_{TH} is determined by the background impurity concentration of the substrate, the difference in the work functions of the gate material and the channel semiconductor material (silicon), the thickness of the oxide insulation layer beneath the gate, and the surface state density in the channel region. The following equation expresses this relationship:

$$V_{TH} = \psi_{inv} + \phi_{ms} - \frac{qN_{ss}}{C_{ox}} \pm \frac{Q_n}{C_{ox}} \quad (1)$$

where ψ_{inv} is the surface potential of silicon at the onset of strong inversion

Table I—Usable range of substrate concentration for aluminum-gate COS/MOS integrated circuits (V_{TH} range: 0.7 to 2.0 V for both n- and p-channel types)

N_{SS}	*n-type Si*	*p-type Si*	*tox*
10^{11}/cm²	9.5 x 10^{15}		950A
10^{11}/cm²		1.6 x 10^{16} (min.)	800A
10^{10}/cm²		2.8 x 10^{16} (max.)	950A

($\psi_{inv}=2\phi_F$ where ϕ_F is the Fermi level of the semiconductor); ϕ_{ms} is the difference in the work functions of the gate material and silicon; q. is the electronic charge; N_{ss} is the surface state of the semiconductor per square centimeter; C_{ox} is the capacitance of the channel oxide per unit area ($C_{ox}=E_{ox}/t_{ox}$ where E_{ox} is the dielectric constant of the channel oxide, SiO_2, and t_{ox} is the thickness of the channel oxide); and Q_B is the substrate charge. This charge may be defined as follows:

$$Q_B=[2E_{si}(q)/N_A-N_D/(2\phi_F)]^{1/2} \quad (2)$$

where E_{si} is the dielectric constant of silicon and N_A-N_D is the net semiconductor impurities per cubic centimeter. The term Q_B/C_{ox} in Eq. 1 is positive for n-channel MOS transistors and negative for p-channel MOS transistors, as determined by the N_A-N_D difference for each type of transistor.

The curves shown in Fig. 1 provide graphic representations of Eq. 1 for a channel-oxide thickness t_{ox} of 800 Å and of 950 Å. These curves show the threshold voltage V_{TH} as a function of the background substrate concentration C_B for both silicon-gate and aluminum-gate MOS transistors. It is apparent from the curves that when the background concentration rises above 10^{16} atoms per cubic centimeter the threshold voltage increases rapidly. Because of this rapid variation in threshold voltage, control of the p-well diffusion becomes highly critical. For substrate concentrations less than 10^{16} atoms per cubic centimeter, the threshold voltage becomes very small and may even reverse in polarity.

Threshold voltage is also a function of the surface state density. For high values of surface state density ($N_{ss}\geq 10^{11}$ states per square centimeter), any significant decrease in the p-well concentration C_B may cause n-channel MOS transistors to cross over to the depletion mode, and an increase in the substrate concentration may cause the threshold voltage of p-channel types

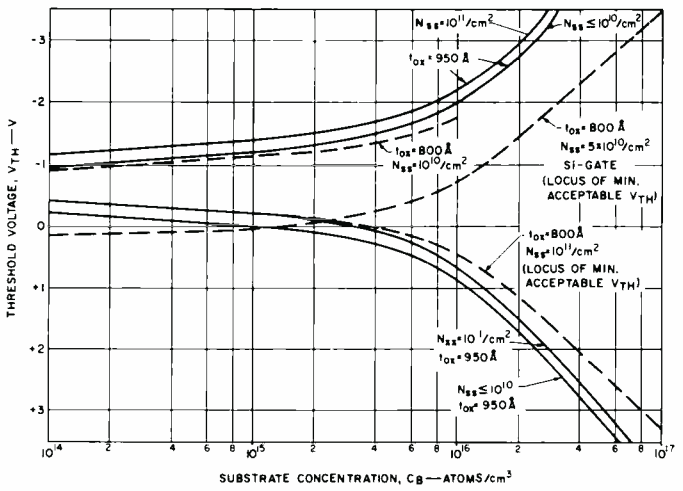


Fig. 1—Threshold voltage as a function of background substrate concentration for both silicon-gate and aluminum-gate MOS transistors.

to increase beyond acceptable levels. At high surface state densities, therefore, the usable range of substrate concentration is substantially reduced.

Table I indicates the allowable variation in substrate concentration C_B, under worst-case conditions, for threshold voltages in the range from 0.7 to 2.2 V. The two design values for threshold voltage, 1.8 V and 2.2 V, used in the processing of standard RCA COS/MOS devices are included in this range. The 1.8-V processing and the 2.2-V processing differ in the degree of substrate concentration and in the thickness of the channel oxide.

The surface states introduce a positive charge in the channel oxide that results in an increase in the threshold voltage of p-channel MOS transistors and a decrease in the threshold voltage of n-channel types. In COS/MOS devices, however, the threshold voltages of the n- and p-channel transistors should be matched in order to decrease propagation delay and to achieve a high noise immunity. The surface-state density, therefore, must be minimized. Low-voltage processing techniques drastically reduce the surface state density to the extent that surface-state effects become negligible.

As shown in Fig. 1, the threshold voltage of n-channel transistors can be easily reduced to zero, or even made negative so that the transistor operates in the depletion mode. The threshold voltage of p-channel transistors, however, can be decreased substantially only by use of a gate material that has an improved work function. Use of a p-type silicon gate instead of the conventional aluminum gate results in a significant improvement in gate-material work function. The use of silicon gates in p-channel transistors that have a channel-oxide thickness of 800 Å and a substrate concentration C_B of less than 2×10^{16} atoms per cubic centimeter result in threshold voltages less than 1.0 V, and circuit operation from a supply voltage V_{DD} of 1.1 V is then possible.

COS/MOS integrated circuits that are directly interfaced with TTL and DTL systems require a drive capability, typically, of 1 mA per gate at low drain-to-source voltage. Fig. 2 shows the transfer characteristics of an n-channel transistor fabricated by 1.8-V process that has a channel width of 6 mils. Devices that will operate at frequencies as high as 1 MHz at 1.5 volts have been fabricated by the 1.8-V process.

Typically, the maximum frequency of

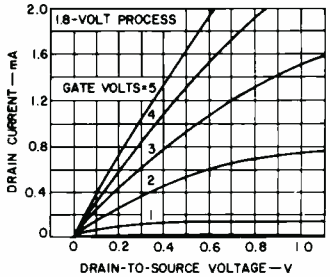
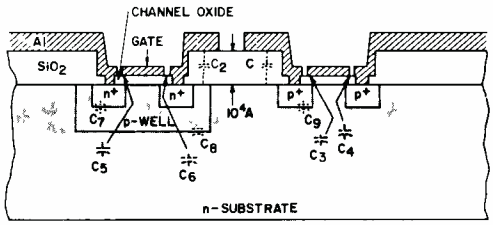


Fig. 2—Transfer characteristics of an n-channel MOS transistor fabricated by the 1.8-V process.



	2.2-VOLT PROCESS	1.8-VOLT PROCESS
C_1	0.02 pF/mil^2	0.02 pF/mil^2
C_2	0.02 pF/mil^2	0.02 pF/mil^2
C_3	0.25 pF/mil^2	0.30 pF/mil^2
C_4	0.26 pF/mil^2	0.33 pF/mil^2
C_5	0.26 pF/mil^2	0.33 pF/mil^2
C_6	0.065 pF/mil^2	0.078 pF/mil^2
C_7	n+ TO p WELL	FOR VALUES SEE FIGS. 4 & 5
C_8	p WELL TO n SUBSTRATE	
C_9	p+ TO n SUBSTRATE	

Fig. 3—Cross section of a COS/MOS integrated circuit showing internal capacitance.

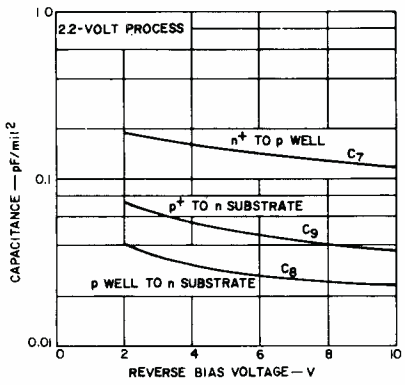


Fig. 4—Junction capacitance as a function of reverse-bias voltage for COS/MOS devices fabricated by the 2.2-V process.

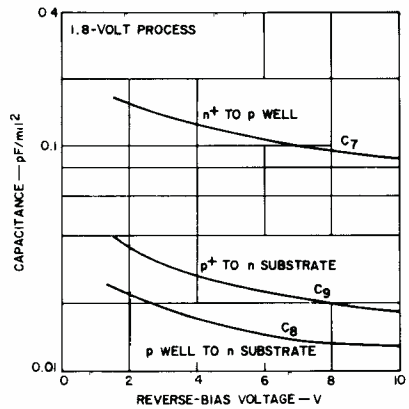


Fig. 5—Junction capacitance as a function of reverse-bias voltage for COS/MOS devices fabricated by the 1.8-V process.

silicon-gate COS/MOS circuits fabricated to date is 1 MHz for operation at 1.1 V and 24 MHz for operation at 10 V.

Physical design parameters

The drain-to-source current I_D of an MOS transistor is significantly affected by the relative magnitude of the drain-to-source voltage V_{DS} with respect to the difference in the magnitudes of the gate-to-source voltage V_{GS} and the threshold voltage V_{TH}, as follows:

1) When $0 < V_{DS} < (V_{GS} - |V_{TH}|)$, the drain-to-source current is given by

$$I_D = \frac{W}{L}\left(\frac{E_{ox}\mu_{eff}}{2t_{ox}}\right)[2V_{DS}(V_{GS} - |V_{TH}|) - V_{DS}^2] \quad (3)$$

2) When $V_{DS} \geq (V_{GS} - |V_{TH}|)$, the drain to-source current becomes

$$I_D = \frac{W}{L}\left(\frac{E_{ox}\mu_{eff}}{2t_{ox}}\right)(V_{GS} - |V_{TH}|)^2 \quad (4)$$

where W is the channel width; L is the channel length; and μ_{eff} is the effective mobility of the charge carriers (holes or electrons).

Good performance and the most economical utilization of space require a judicious choice of the channel length-to-width ratio (W/L). The true channel length L and the K factor ($K = E_{ox}\mu_{eff}/2t_{ox}$) must be known to determine the required W/L ratio. The true channel width L is determined from a knowledge of processing conditions and of the effects of high-temperature exposure on the n$^+$- and p$^+$-type dopant during and after their diffusion cycles. Lateral diffusion has been determined. The true channel length L may be determined as follows:

$$L = L_{measured} - 2\chi_0 \quad (5)$$

when $L_{measured}$ in the measured value of the channel length and χ_0 is the total lateral diffusion.

The K factor can be readily calculated by use of Eq. 2 or Eq. 3 if the channel width is known. For this calculation, the drain-to-source current I_D is determined by measurement, the true channel length L is determined as indicated in Eq. 5, and the threshold voltage V_{TH} is obtained from a curve of gate-to-source voltage as a function of the square root of the drain current I_D. Table II and Figs. 3 through 5 show process constants for RCA COS/MOS integrated circuits.

Basic processing

For COS/MOS integrated circuits designed to operate from a supply voltage V_{DD} in the range from 3 to 15 V, the starting material is n-type silicon that has a resistivity of 1 to 2 ohm-centimeters and 100-axis crystallographic orientation. Fig. 3 shows a cross section of a typical device. A controlled low surface concentration p-type diffusion is carried out in selected regions to provide the p-type well. The n-type silicon is the substrate for the p-channel transistors; the p-type well serves as the substrate for n-channel transistors. The surface concentration of the p-type well is controlled according to the threshold voltage requirements.

Masking oxidations, photoengravings, and diffusions of n$^+$- and p$^+$-type regions are then carried out. These diffusions provide all source and drain regions, as well as guard bands, tunnels, and resistors. A new oxide is then formed to a thickness of 10,000 Å. This oxide is then removed from all the active-device regions, and an ultra-clean (free of positive-charge contamination) oxide is grown. The thickness of this oxide is controlled to achieve the required level of threshold voltage. Contact windows are then opened, and a clean aluminum metalization, which is also free of positive charge contamination, provides the gate material and interconnection system. The chart shown in Fig. 6 outlines the basic operations involved in the processing of standard COS/MOS integrated circuits.

In MOS technology, diffusion depths and doping levels of the source and drain regions do not require the tight control that is necessary in bipolar technology. Diffusion depths are only critical to the extent that they may affect channel length. Doping levels are generally high in order to assure low-resistance tunnels and good contacts. The only diffusion in COS/MOS processing that is very critical and that must be tightly controlled is the p-well

Table II—Typical process constants for standard COS/MOS integrated circuits.

	$X_{o(n^+)}$ (mils)	$X_{o(p^+)}$ (mils)	$R_{s(n^+)}$ (ohms/sq.)	$R_{s(p^+)}$ (ohms/sq.)	K_N (μA/V^2)	K_P (μA/V^2)
			2.2-V process			
$V_{DS} \geq (V_G - V_T)$	0.055	0.048	14	6	6	3.5
			1.8-V process			
$V_{DS} \geq (V_G - V_T)$	0.06	0.064	14	60	10	5

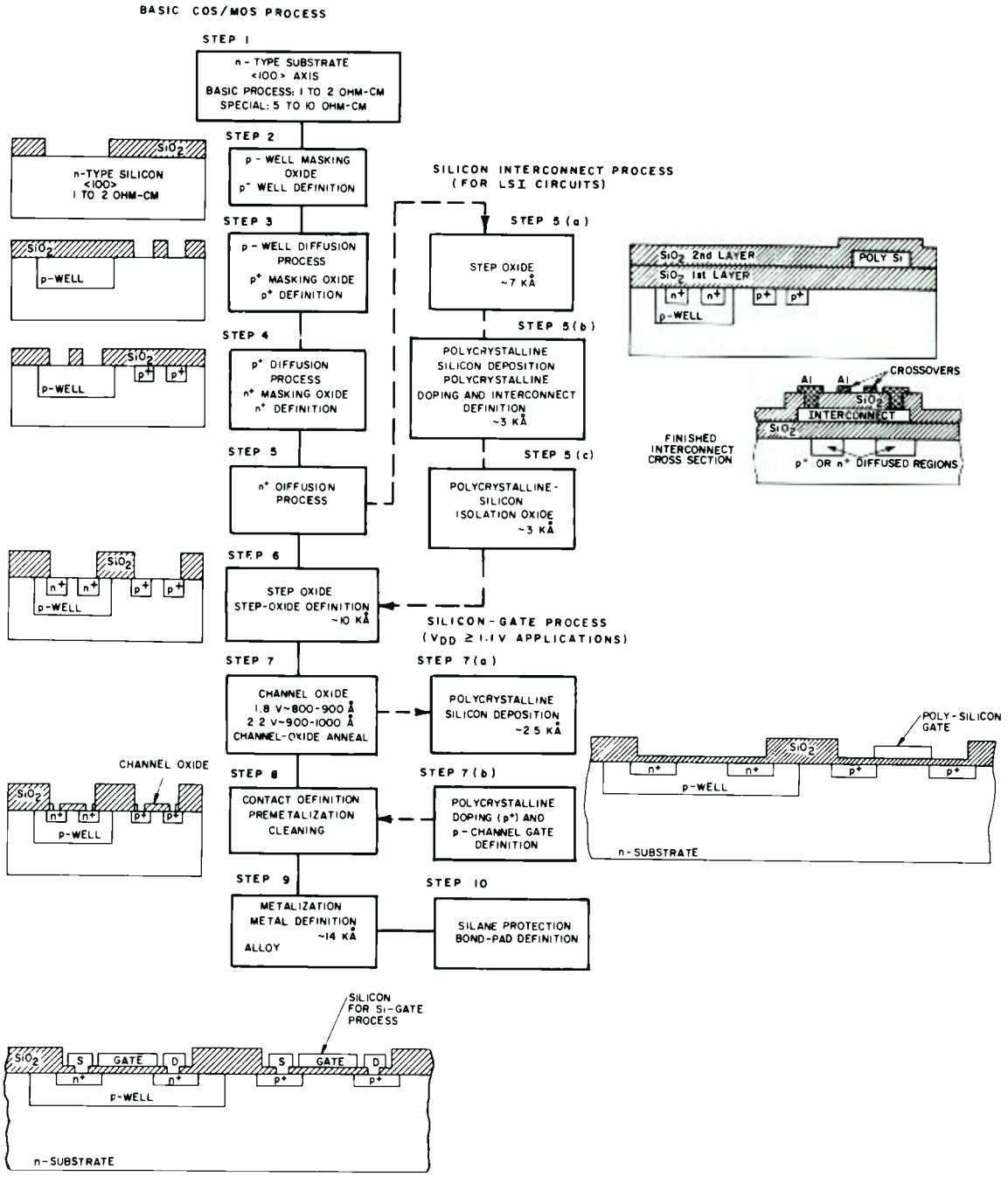


Fig. 6—Basic operations in the fabrication of COS/MOS integrated circuits.

diffusion. For process control, sheet resistance measurements usually suffice. However, control of the channel oxide is of great importance. As a result, capacitance-voltage (*C-V*) curves are used extensively for process control and evaluation. Fig. 7 shows *C-V* curves of COS/MOS capacitors fabricated on the same pellet by the 2.2-V process. Accurate capacitance measurements yield accurate determination of oxide thickness. The *C-V* curves all provide information used to determine the substrate concentration as well as the contamination level. Bias temperature stressing of the capacitors is used to determine the stability of the channel oxide. When the stress applied is ± 10 V at 300°C, the typical shift of the flat-band voltage is 0.1 V.

Silicon interconnect processing for LSI circuits

LSI COS/MOS circuits that use silicon interconnects are fabricated by the basic COS/MOS process with the excep-

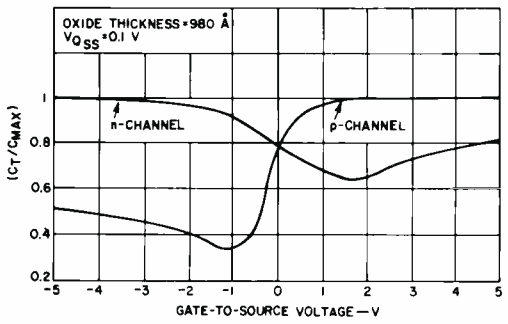


Fig. 7—Capacitance-voltage characteristics for n- and p-channel capacitors on the same COS/MOS pellet.

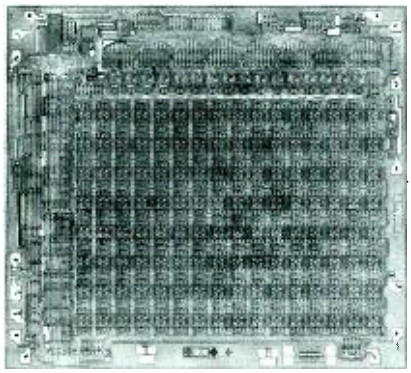


Fig. 8—Typical COS/MOS LSI circuit (256-bit memory), RCA Dev. No. TA6335.

tion that additional steps (shown in Fig. 6) are required to provide the interconnects. After the n^+ diffusion processing is completed, a portion of the field oxide, a layer 7000 Å thick, is formed. The polycrystalline silicon layer, approximately 3500 Å thick, is then deposited, doped, and defined. Additional field oxide is then deposited to insulate the interconnects. The wafers are then returned to the basic COS/MOS processing sequence for completion. The interconnects are doped with p^+-type dopants to obtain a sheet resistivity of 80 to 120 ohms per square. Fig. 8 shows a photograph of a typical LSI COS/MOS circuit. The photograph shown in Fig. 9 indicates the excellent continuity achieved by use of specially sloped field-oxide techniques and p^+-type-doped interconnects.

Silicon-gate COS/MOS process

COS/MOS integrated circuits in which p-type-doped silicon is used as the material for the gate electrode of the p-channel MOS transistor can be operated from a supply voltage V_{DD} as low as 1.1 V. At present, the most common application for silicon-gate COS/MOS integrated circuits is in wrist watches although their ability to provide higher speeds at higher supply voltage will result in widespread application of these devices. Silicon-gate COS/MOS integrated circuits are fabricated by the basic COS/MOS process with the exception that additional steps (shown in Fig. 6) are required to form the silicon gates.

After the channel oxide is grown, a 2000-Å-thick polycrystalline silicon layer is deposited, doped with a p^+-type dopant, and defined. The polycrystalline silicon layer covers the channel region of the p-channel transistors only. The wafers are then returned to the basic COS/MOS processing sequence for contact opening and metalization. The metal is defined to serve as gate material for the n-channel transistors and as the interconnection system. Fig. 10 shows a photograph of a timing circuit that uses silicon-gate COS/MOS devices.

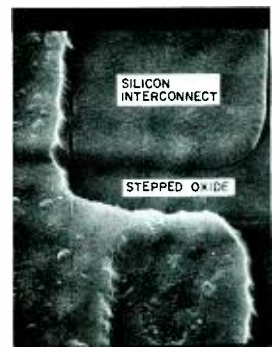


Fig. 9—LSI pellet with sloped field oxide and silicon interconnects.

Beam-lead COS/MOS processing

In the fabrication of beam-lead COS/MOS devices, a thin layer, approximately 300 Å thick, of silicon nitride is deposited on basic COS/MOS wafers after the channel oxide (usually 800 Å of SiO_2) is grown. Contact windows are opened, and a metal layer of either aluminum or palladium is deposited. Sintering of either metal provides good contact regions, and all excess metal is then removed. A titanium palladium-gold metalization is then deposited on the wafer. The metal pattern is defined and etched, and the beams are plated. Conventional beam-lead separation follows. Fig. 11 shows a photograph of a typical beam-lead type of COS/MOS pellet.

Fig. 10—Silicon-gate COS/MOS integrated circuit (RCA Dev. No. TA6062) used in timing applications.

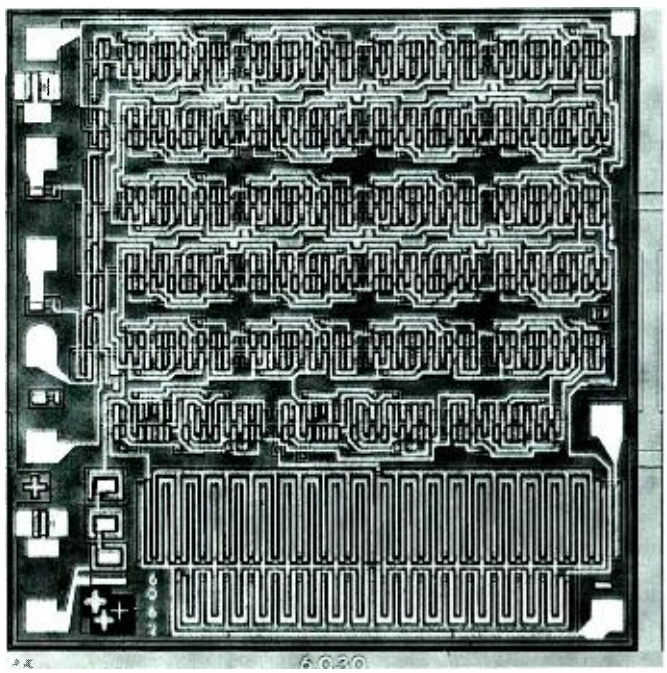
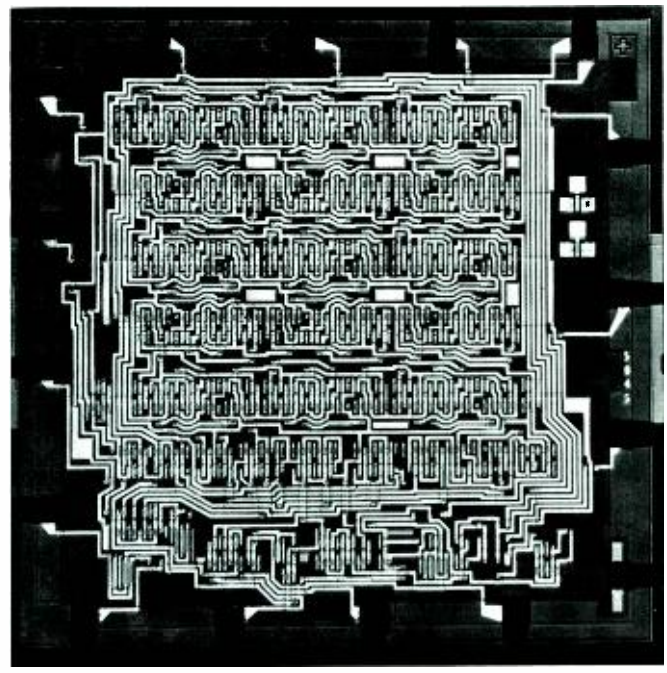


Fig. 11—Typical beam-lead COS/MOS pellet.



COS/MOS circuits for consumer applications

D. R. Carley

This paper describes the development of low-power digital integrated circuits for consumer applications. Several applications are described, including time-keeping applications (watches and clocks), digital tuning techniques for FM and television, and pocket pagers. The main technology discussed is complementary-symmetry MOS.

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received the BS in Physics in 1957 from the University of Michigan. Upon graduation, he joined the Semiconductor Division of RCA in Advanced Development where he worked on an all-diffused germanium transistor for horizontal deflection circuits. In 1959 he was promoted to Engineering Leader in Industrial Transistor Design. In this position he concentrated on the development of high-power, high-frequency transistors, and was responsible for the development of a family of transistors utilizing the overlay design. Mr. Carley received the 1964 Engineering Achievement Award from RCA Electronics Components and Devices for his contributions to high-frequency power transistors, and he received he David Sarnoff Engineering Achievement Award in 1965 for the design and development of the overlay transistor. Mr. Carley was promoted to Manager, Industrial RF Transistor Design in 1965, and in January 1966 was promoted to Manager, High-Frequency Device Engineering. In this position he was responsible for design and application of VHF and UHF transistors and for hybrid integrated circuits for microwave applications. In September 1971, Mr. Carley was appointed to his present position with responsibility for all phases of engineering on the RCA family of COS/MOS integrated circuits. In early 1972, engineering responsibility for RCA liquid-crystal products was added.

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THE CURRENT "buzz word" among digital designers is COS/MOS. COS/MOS has a number of unique advantanges that make it ideally suited for consumer applications. The basic CD-4000 family features a wide operating range; any supply voltage from 3 to 15 V may be used. Therefore, well-regulated power supplies are not needed. This feature makes COS/MOS well suited for automotive applications and other applications in which costly supplies are not feasible. Even more important than the supply-voltage range, perhaps, is the exceedingly low quiescent power consumption. Entire LSI circuits containing 1000 to 2000 active devices may have maximum leakage currents of 1μA and are typically in the nanoampere range.

Noise immunity

Consumer applications are notorious for their high electrical noise. These high noise levels are a major reason for the conversion of many applications from analog to digital operation. The complementary structure of the inverter leads to a nearly ideal input/output transfer characteristic with a switching point typically midway (45 to 55%) between the 0 and 1 logic levels. Therefore, the inverter has high DC noise immunity because the output does not switch until the input voltage rises to nearly half the supply voltage (V_{DD}).

Noise immunity increases as the input-noise pulse width becomes less than the propagation delay of the circuit. This condition is often described as AC noise immunity. Standard complementary-symmetry MOS circuits have moderate switching speeds of approximately 50 ns at 5 V; therefore, they are not affected by high-speed noise pulses.

Even more important is the very low energy generated by COS/MOS switching circuits at narrow bandwidths. Use of COS/MOS circuits in consumer radio equipment has proven superior to TTL logic in this regard. For example, TTL circuits generate noise transients of 40 to 60 mA with harmonics ranging from 20 to 200 MHz. COS/MOS circuits operating from a 10-V supply generate noise transients of only 1 to 3 mA with a bandwidth of only 3 to 30 MHz. With a supply voltage of 3 V, such as that used in pocket paging receivers, COS/MOS digital selectable address logic generates transients of less than 100 μA at bandwidths of 50 to 500 kHz.

Time-keeping applications

One of the most important and widespread uses of low-power digital integrated circuits is in timing applications. The advantages of low power inherent in COS/MOS circuits are particularly important for timing because many applications involve a limited power supply. In addition, COS/MOS has good LSI capability so that even the most complex timing functions can be implemented by use of a single package with a cost low enough for high-volume consumer applications.

Most timing circuits consist of three basic parts: an oscillator or main frequency source, some logic (usually in the form of frequency-dividing circuits), and buffer or decoder logic needed to drive the mechanical or electrical output display. Of the three sections, the oscillator is perhaps the most important because the accuracy of the timing unit is entirely dependent upon the accuracy of the oscillator. COS/MOS timekeeping circuits are discussed in detail in the paper, "Timekeeping advances through COS/MOS technology," by S. S. Eaton elsewhere in this issue.

Wristwatches

The use of digital circuits in wristwatches poses some special problems, almost all of which relate to the small size of the watch. For instance, the battery size is extremely limited. A typical battery geometry is a cylinder 0.205 in. in height and 0.450 in. in di-

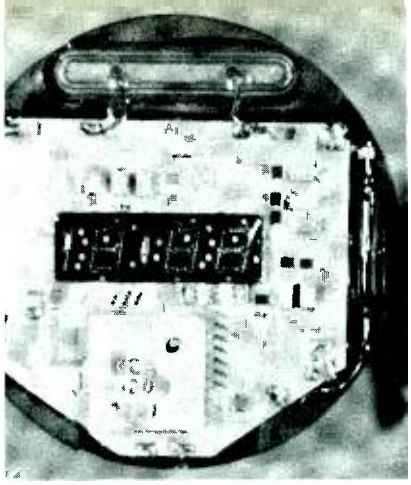


Fig. 1 (left)—Works of a quartz wristwatch. Fig. 2 (right)—Table clock that employs COS/MOS circuitry.

ameter. Such a battery can supply approximately 19μA for a year. The battery size and capacity restrict the oscillator and divider current to approximately 6 μA, and allow approximately 8 to 10 μA for the motor. Again, because of size constraints, a crystal with a frequency of at least 32 kHz is generally chosen because such a crystal offers the best compromise between stability, ruggedness, size, and power consumption. Crystals with much higher frequencies, such as 4 MHz, would be used except for the power limitation. The high-frequency crystals are much cheaper, have better temperature and frequency stability, and are more rugged because they are AT cuts; the only problem is the power limit imposed by battery size. Because the current consumption of the circuit would increase in direct proportion to CV^2f, the current would be in the 200-μA range.

Fig. 1 is a photograph of a quartz wristwatch; the LED display is pulsed *on* to conserve battery power. The digital display is bright, but consumes a great amount of power. The cos/MOS IC contains the oscillator amplifier, digital divider, and display decoder. The operating power for the IC is less than 10 μA. The cos/MOS chip pictured measures 0.150×0.150 inches and contains over 1300 transistors.

Wall clocks

Size and power limitations are not as severe in wall clocks as in watches. Generally one or two *C* cells are used, depending on the voltage required. A *C* cell can supply 250 μA for more than a year while still maintaining an end-of-life voltage of 1.1 V. This larger battery capacity permits the use of crystals of higher frequency. The range used at present is 131 to 524 kHz, the most common frequency is probably 262 kHz.

Motors for driving the clock hands are typically of the balance-wheel or continuously-rotating synchronous types. Sensitivity to vibration is usually not a restriction, and the balance-wheel motor can be successfully used in place of the more expensive stepping motor. Clock motors typically require about 300 to 450 μW of power or average currents of 200 to 300 μA at 1.5 V.

Automobile clocks

The design of an automobile clock must take into account the following requirements:

1) The automobile supply can vary from 0 to 22 V, and is nominally between 11 and 13 V. The auto clock must be accurate when the automobile supply is in the range of 5 to 16 V.
2) The automobile supply can contain a high-energy transient of +120 V and a low-energy transient of −75 V with time constants of 45 to 80ms and an accidental reverse bias of −18 V.
3) The automobile thermal environment varies from −40°C to +50°C, and the humidity can be as high as 90 to 95% at a temperature of 50°C. Vibrations in the automobile can be as high as one g at frequencies varying from 30 to 90 Hz.

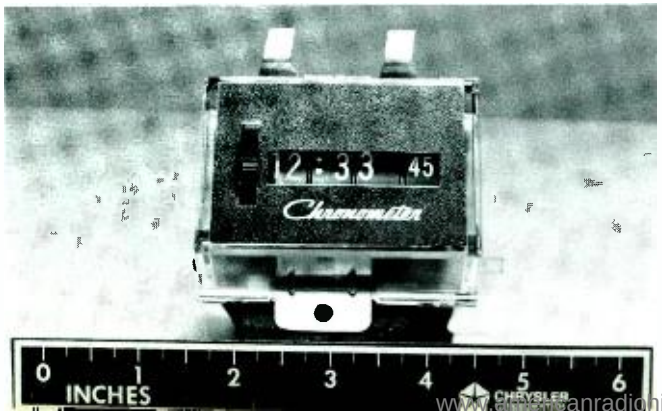
Both digital and analog automotive clocks have been developed. Digital clocks have been constructed using several display techniques: Numitrons, light-emitting diodes, and liquid crystals. Elsewhere in this issue, an article by D. K. Morgan, "RCA cos/MOS integrated circuits in the automobile environment," describes cos/MOS circuitry for automotive electronics, including clocks.

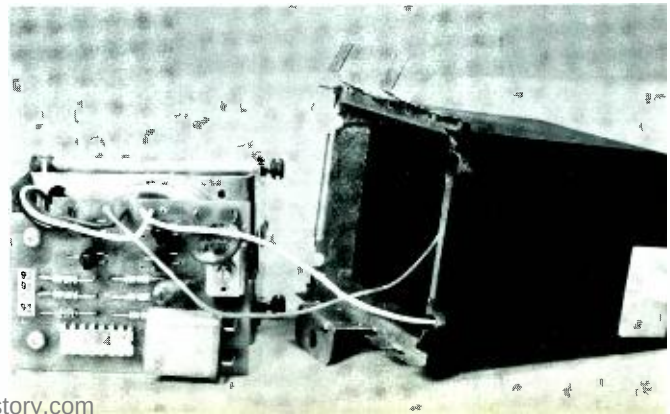
Fig. 2 is a photograph of a cos/MOS and liquid-crystal, digital, table clock using standard parts. Fig. 3(a) is a mechanically driven, digital, automotive clock. The 4-MHz crystal oscillator, 21-stage frequency divider, and push-pull motor driver are contained in the RCA cos/MOS IC shown on the clock electronic assembly in Fig. 3(b).

Pocket pager

A pocket pager consists of a small pocket radio receiver with added timing, address, storage, and address/recognition logic circuits. The logic synchronizes itself to incoming messages, and compares the received address information. If it finds a match between the two, a tone is sounded to alert the user

Fig. 3—(a, left) Mechanically driven, digital, automotive clock; (b, right) clock electronic assembly showing COS/MOS IC. (Photographs courtesy of Chrysler Corporation, Huntsville, Alabama)





that he is being paged. The product is being offered to the public by telephone companies which provide the transmitters to cover their service area.

The most common code-modulation techniques are multi-tone and diphase. In the multi-tone method, tones of different frequency are transmitted, usually one at a time; the frequency of each transmitted tone determines the value of the message digit. The diphase transmission consists of a two-level digital signal in which each binary digit is coded as a low and a high level with a transition between the two levels at the center of the bit. If a zero is coded by a low followed by a high level, then a *one* is represented by a high followed by a low level.

Two of the most important requirements for pocket pagers are small size and long battery life. Units should fit easily in a shirt pocket; battery life of one year is desirable. Good range with reliable reception and a near-zero false-alarm rate are also essential. In addition, the system must supply a large number of addresses (enough digits in the address) with an adequate transmission rate to avoid queueing problems. Some systems provide more than one address in the same receiver.

The low-power requirement points to COS/MOS as the natural technology for implementing pocket-pager logic circuits. Because the data rates are generally low, the logic is essentially idle most of the time, and the low static current drain characteristic of COS/MOS leads to long battery life. Typically, a complete COS/MOS logic system operates at a current of 100 μA or less.

Synchronization of internal timing in pocket-paging systems can be efficiently accomplished by use of low-power COS/MOS phase-locked-loop (PLL) circuits. The high input impedance and large dynamic range of MOS voltage-controlled oscillators make COS/MOS ideal for PLL applications up to 500 kHz.

Because some of the system requirements for pocket pagers tend to conflict, there is a considerable room for ingenuity in design. COS/MOS allows a high degree of logic complexity on a single chip at the cost level necessary for widespread use.

In addition to the paging systems offered to the general public by telephone companies, there are other applications both for pocket pagers and for related equipment. For example, pocket pagers may be used in restricted areas such as hospitals and other businesses. Also, because the addresses have a large number of bits, the chance of triggering on noise is very low. Therefore, the same devices can be used in remote-control applications with signals transmitted either by radio or by wire. In the latter case, several instruments could be controlled over the same wire provided they are assigned different addresses. As a result, logic circuits can be used to replace extensive wiring.

Fig. 4 shows a modern, low-power, digital, pocket-sized, paging receiver. Two RCA, custom COS/MOS IC's are used for digital-signal synchronization and data processing. Over 1400 transistors are contained in the two COS/MOS chips shown.

Frequency-synthesizer applications

Digital tuning, control, memory, and numeric frequency-channel displays have been well established as integral parts of a superior tuning vehicle for reliable military communications sets. The advent of digital IC's opened up this application. Bipolar MSI was used initially, but the high power levels,

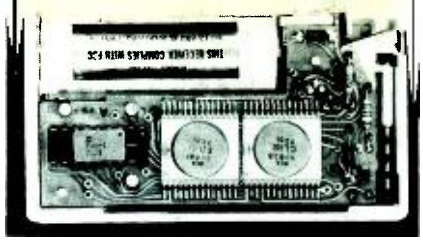


Fig. 4—A modern paging receiver. (Photograph courtesy of Martin Marietta Communications and Electronics, Orlando, Florida.)

great number of IC's, tight power-supply regulation requirements, and non-LSI chip complexity kept the cost high until recently.

Heathkit has introduced a tuner that utilizes a frequency synthesizer, a memory, and a digital frequency readout. The tuner has three tuning modes: a number can be punched to select the frequency of the desired station, the tuner can be set to scan and stop at all stations or only at stereo stations, or up to three stations can be selected by a front-panel button that accesses preprogrammed cards. The tuner also utilizes a digital discriminator and a phase-locked loop as a multiplexer demodulator. A block diagram of the receiver is shown in Fig. 5. The tuner makes extensive use of digital integrated circuits; it contains more than 50 TTL and ECL circuits.

The use of COS/MOS devices in the tuner can lead to improvements in performance and lower production costs. A block diagram of an AM/FM set is shown in Fig. 6; the set features:

1) FM manual frequency selection by means of switches;

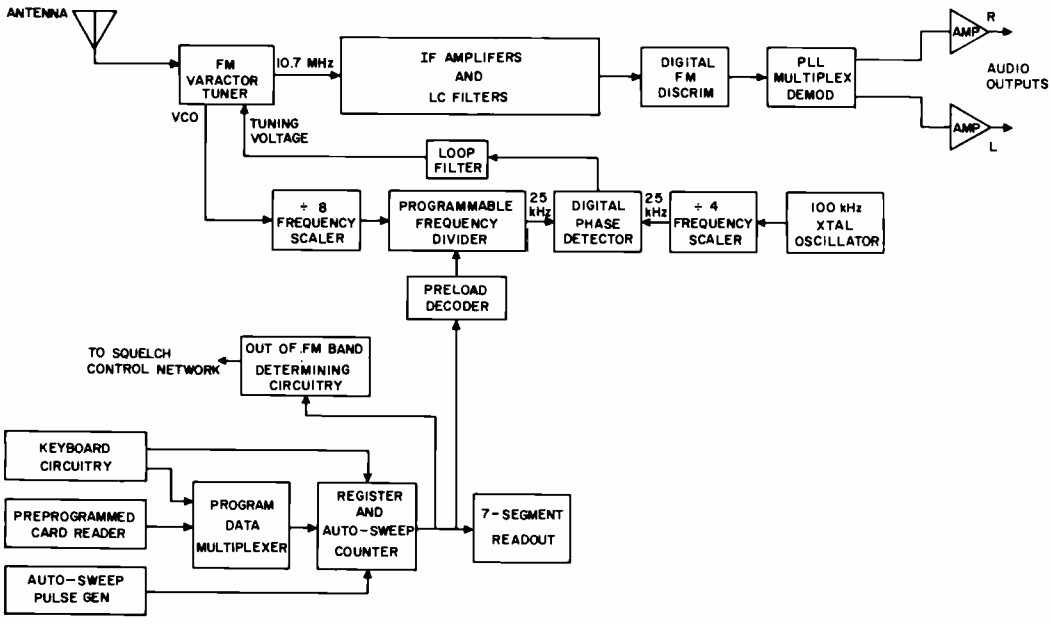


Fig. 5—Block diagram of Heathkit digital FM tuner.

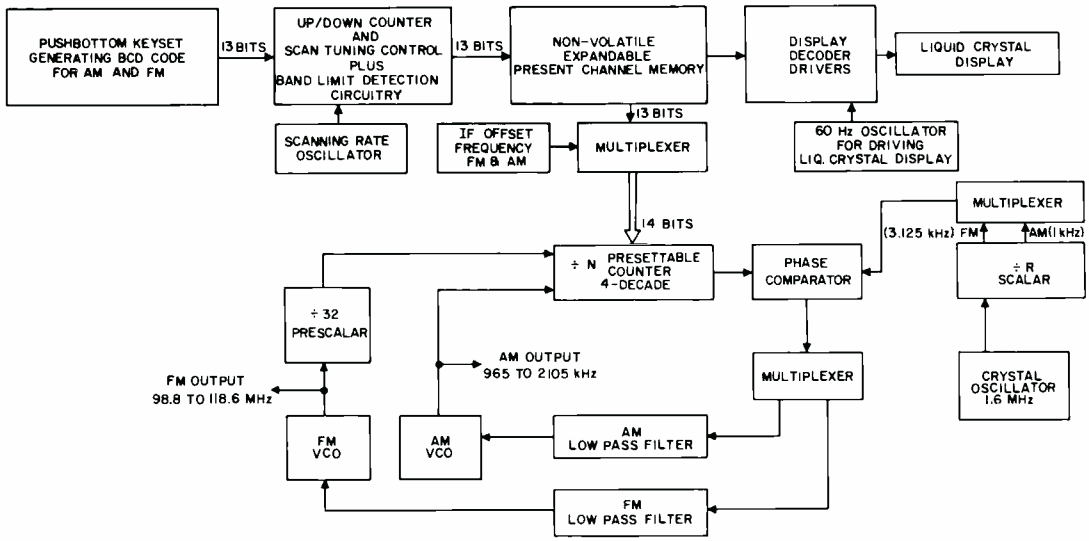


Fig. 6—Block diagram of FM/AM tuner using frequency synthesizer.

2) Step-scan tuning control in AM or FM, up or down (scan-rate control optional);
3) Four-word AM or FM all-electronic preset channel memory, loadable from front-panel switch;
4) Liquid-crystal display;
5) Digital frequency synthesizer;
5) Easy adaptation to remote control.

Cos/Mos digital logic has several outstanding advantages for synthesizer tuning, including the following:

1) LSI complexity with the required speed capability;
2) Low noise generation to minimize digital switching intereference in the rf bandwidth;
3) Necessary low power (less than 500 mW for entire digital tuner) for battery radios;
4) Low-cost and small-size non-volatile preset channel memory using a small holding battery, as shown in Fig. 7.

It is practical to integrate the entire synthesizer and control logic system of Fig. 5 on 3 or 4 chips. The divide-by-*N* counter is already being designed into one general-purpose four-decade presettable counter chip which will be a standard cos/Mos circuit. This degree of LSI and high cos/Mos yields will lead to pricing that will soon put digital tuning into TV and automobile receivers, as well as military radios and high-quality AM/FM sets.

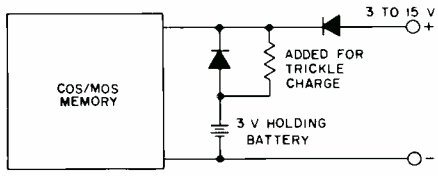


Fig. 7—Non-volatile COS/MOS memory.

Calculators

The consumer calculator field is perhaps one of the greatest opportunities for Mos digital integrated circuits. The number and rate of introduction of new models at constantly decreasing prices is reminiscent of the development of transistorized radios. However, standardization of approach has not yet been developed even in four-function calculators. Early machines utilized P/Mos technology and required many devices. Perhaps four arrays were used in the arithmetic unit, with eight or more devices to drive the display; the display usually consisted of gas-discharge of fluorescent devices. These machines were usually AC powered because of the relatively high power needed.

More recently, light-emiting diodes and liquid crystals have begun to be used in displays, and demands have been placed on IC designers for simpler and less expensive integrated circuits to drive them. The trend is clearly toward smaller and cheaper machines that can be carried in a pocket. The dozen or more packages used in the past are being replaced by one P/Mos and cos/Mos array. Probably one of the best examples of a single-chip calculator is one manufactured by Texas Instruments that provides the complete arithmetic function plus decoder drivers for the display. Future four-function calculators will combine cos/Mos devices and liquid-crystal displays to provide portable machines with many months of life from throw-away batteries.

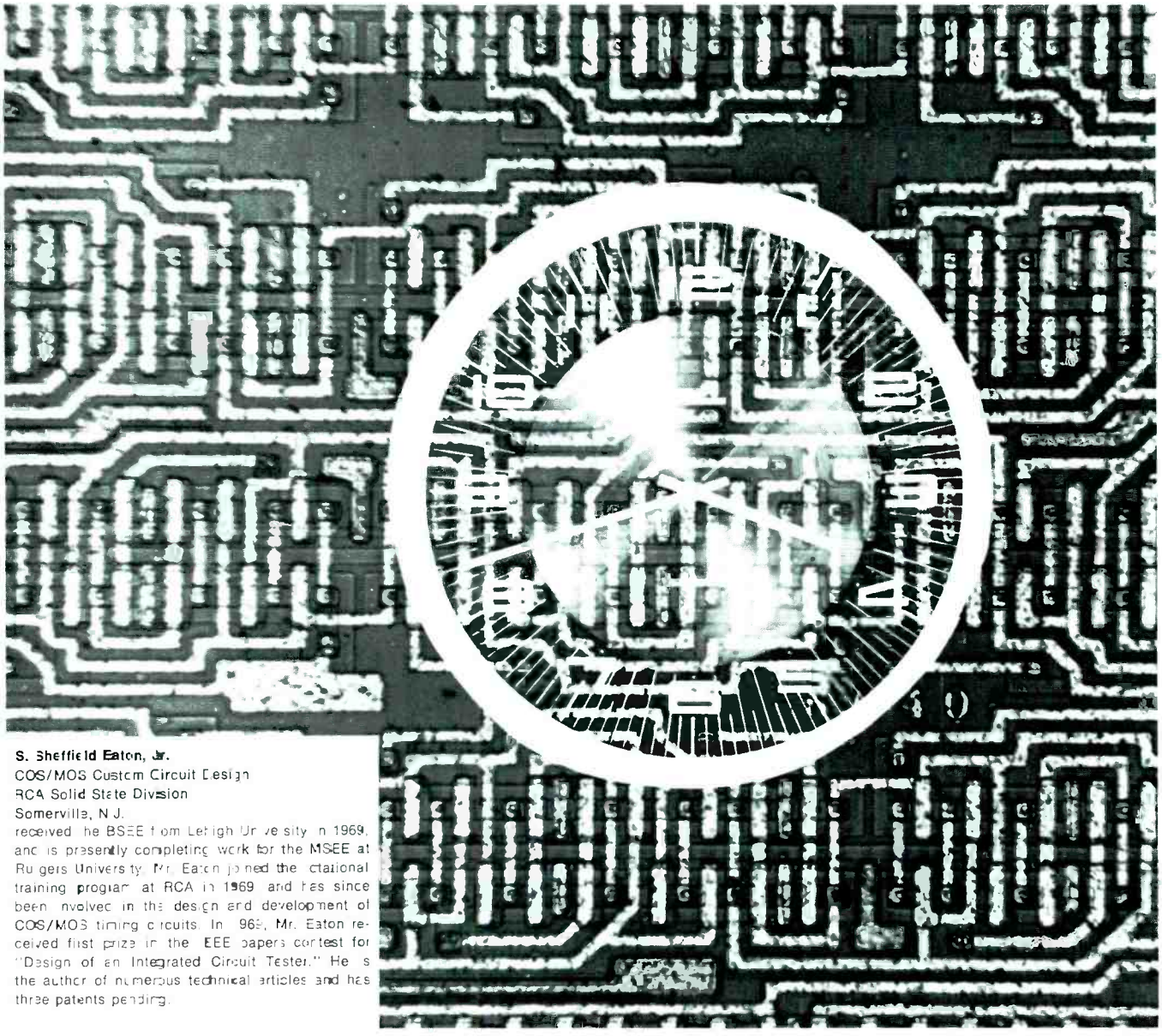
Conclusion

Other programs are underway that will provide more opportunities for the use of digital integrated circuits in consumer equipment. Some additional functions presently being performed digitally are coin changing in vending machines, meter reading, and, perhaps the ultimate in consumer applications, heart pacing. An *RC* oscillation and a frequency-division circuit like those used for timekeeping provide the required stimulus to maintain the proper heartbeat. Many other possibilities exist in automotive applications; some current programs are digital adaptive-braking systems for anti-skid and shorter stopping distances in emergency stops, digital control of the transmission rather than analog or hydraulic control, digital control of combustion and spark advance for pollution control, digital speed controllers, and sequential seat-belt logic. Cos/Mos is ideal for automotive applications because of its wide power-supply tolerance, excellent noise immunity, and low power consumption. Low power consumption is particularly important in seat-belt logic because that logic must operate continuously.

These applications and others on the horizon show that digital integrated circuits will be an important part of consumer electronics.

Acknowledgments

The author gratefully acknowledges the contributions made by his colleagues at the Solid State Division.



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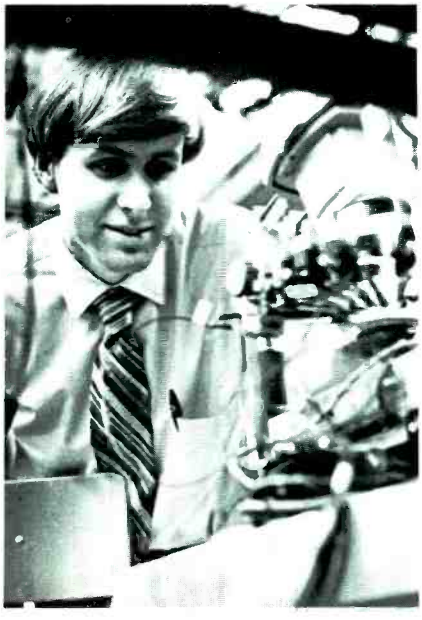
received the BSEE from Lehigh University in 1969, and is presently completing work for the MSEE at Rutgers University. Mr. Eaton joined the educational training program at RCA in 1969 and has since been involved in the design and development of COS/MOS timing circuits. In 1969, Mr. Eaton received first prize in the IEEE papers contest for "Design of an Integrated Circuit Tester." He is the author of numerous technical articles and has three patents pending.



Timekeeping revolution through COS/MOS technology

S. S. Eaton

In today's fast-moving society, applications for timekeeping devices seem almost endless. Modern wristwatches and clocks have become indispensible items, and housewives enjoy the conveniences of oven, washing-machine, and blender timers. Farmers rely on automatic sprinkling and feeding systems, photographers on exposure timers, and the military on timers for modern weapons. At present, most of these applications employ some form of mechanical timing element. The development of COS/MOS integrated circuits and their usefulness in electronic timing circuits promise to revolutionize the timing industry. The reasons are made clear in the discussions of various COS/MOS timing circuits and systems provided in this paper.

Table I—Typical component values for common cuts of quartz oscillator crystals.

Frequency	*32 kHz*	*280 kHz*	*525 kHz*	*2 MHz*
Cut	XY bar	DT	DT	AT
R_S (ohms)	40K	1820	1400	82
L (Hy)	4800	25.9	12.7	0.52
C_1 (pF)	0.00491	0.0125	0.00724	0.0122
C_0 (pF)	2.85	5.62	3.44	350
C_0/C_1	580	450	475	4.27
Q	25000	25000	30000	80000

MOST COS/MOS TIMING CIRCUITS consist of three basic parts:

1) An oscillator, or main timing standard;
2) Digital processing logic, usually in the form of frequency-dividing circuits; and
3) Logic-circuit drivers for mechanical or electrical output devices controlled by the digital processing logic.

The oscillator is perhaps the most important because the accuracy of the total COS/MOS timing system depends on the accuracy of the oscillator.

Basic oscillator design considerations

A basic oscillator circuit consists of an amplifier and a feedback section, as shown in Fig. 1. For oscillation to occur, the gain of the amplifier times the attenuation of the feedback network must be greater than one. In addition, the total phase shift through the amplifier and feedback network must be an integer multiple of 360°. These conditions imply that oscillations occur in any system in which an amplified signal is returned in phase to the amplifier input after being attenuated less than it was originally amplified. In such a system, any noise present at the amplifier input causes oscillation to build up at a rate determined by the loop gain, or the $\alpha\beta$ product, of the circuit.

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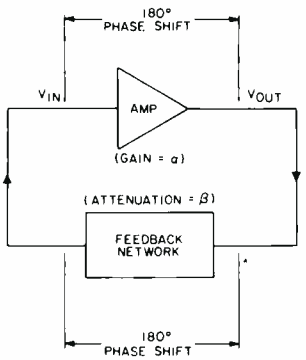


Fig. 1—Basic oscillator circuit.

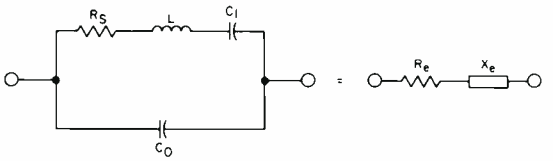


Fig. 2—Equivalent circuit for a quartz oscillator crystal.

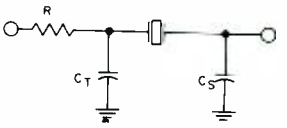


Fig. 4—Crystal pi-type feedback network.

The frequency stability of an oscillator is primarily dependent upon the phase-changing properties of the feedback network. For high stability, quartz crystals and tuning forks are commonly used as feedback network elements. The quartz crystal is the more popular because of its higher Q, or greater inherent frequency stability.

Selection of crystal operating mode

Fig. 2 shows the equivalent circuit of a quartz crystal, and Table I lists typical component values of the elements included in the equivalent circuit for different crystal cuts and operating frequencies. The basic circuit can be resolved into equivalent resistive (R_e) and reactive (X_e) components. Fig. 3 shows curves of these components as functions of frequency for a typical 32.768-kHz crystal. Fig. 3b shows two points at which the crystal appears purely resistive, (*i.e.*, points at which $X_e=0$). These points are defined as the resonant (f_r) and antiresonant (f_a) frequencies. Series-resonant oscillator circuits are designed to oscillate at or near f_r. Parallel-resonant circuits oscillate between f_r and f_a, depending upon the value of a parallel loading capacitor, as discussed later. In contrast to series-resonant circuits, parallel resonant-circuits work best with amplifiers that have high input impedances. The parallel-resonant circuit, therefore, is most applicable to crystal oscillators that employ COS/MOS amplifiers.[1]

Feedback-circuit configuration

A feedback circuit suitable for use with a parallel-resonant oscillator circuit is shown in Fig. 4. This circuit, known as a crystal pi network, is intended for use after an amplifier that provides a 180° phase shift. The pi network is designed to provide the additional 180° phase shift required for oscillation. The phase angle for this type of feedback circuit is extremely sensitive to a change in frequency, a condition necessary for stable oscillation. If the equivalent

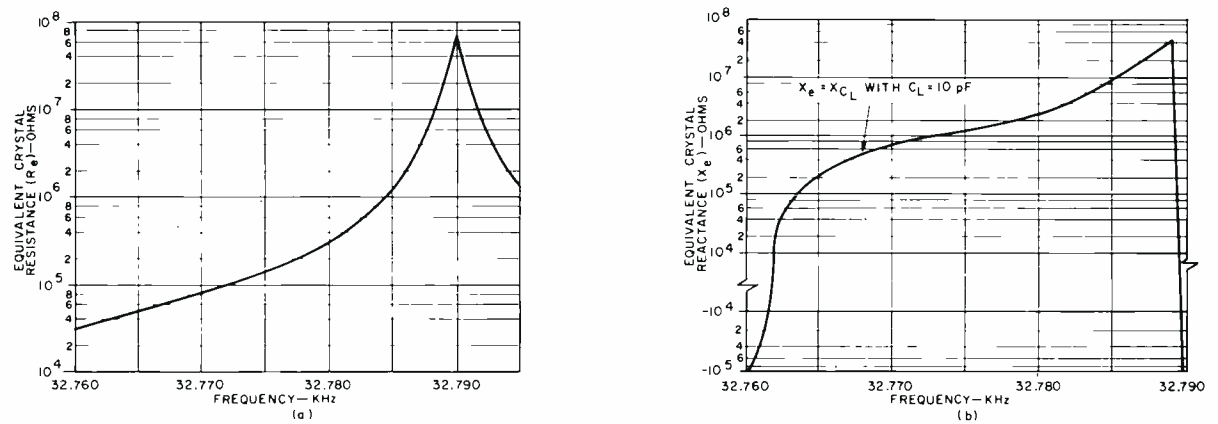


Fig. 3—Impedance characteristics of a quartz crystal: (a) equivalent crystal resistance as a function of frequency; (b) equivalent crystal reactance as a function of frequency.

resistance of the crystal were in fact zero (infinite Q), a change in the phase angle of the feedback circuit would not cause any change in oscillator frequency; the oscillator, therefore, would be insensitive to any phase change in the amplifier. Though practical crystals allow only a slight change in frequency for large variations in phase angle, the amplifier phase angle should, to the extent possible, be made independent of temperature and supply-voltage variations in order to minimize the phase compensation required of the feedback network. Any required phase compensation will, of course, dictate a corresponding change in the frequency of oscillation consistent with practical values of crystal Q. For this reason, the equivalent resistance of the crystal should be maintained as low as possible, and the amplifier should be designed to roll off at frequencies greater than the crystal frequency.

Oscillator amplifier

Fig. 5 shows a COS/MOS amplifier circuit that may be used to provide the amplification function in a crystal-controlled oscillator. The amplifier is biased so that the output voltage V_{out} is equal to the input voltage V_{IN} or typically is equal to one-half the supply voltage V_{DD} (*i.e.*, $V_{OUT}=V_{IN}=V_{DD}/2$). Biasing is accomplished by means of a resistor that has a value high enough to prevent loading of the feedback network, yet that is low in comparison to the amplifier input resistance. Resistor values of 10 to 500 megohms will satisfy these criteria; however, lower values in the order of 15 megohms are generally used to allow greater input leakage without any severe change in bias point. The gain of the amplifier varies with supply voltage, the size of the n- and p-channel MOS transistors, and the sum of the threshold voltages of the n- and p-channel transistors. When an oscillator amplifier is designed to roll off at frequencies greater than the crystal frequency, care must be taken to assure that the transistor sizes are large enough for the particular supply voltage used and range of threshold voltage expected. For any circuit, though, the sum of the threshold voltages of the n- and p-channel transistors must always be less than the supply voltage.

The oscillator amplifier governs, to a certain extent, the selection of the components for the feedback network. The amplifier current consumption is strongly dependent upon the attenuation across the feedback network. As the attenuation becomes greater, the signal at the amplifier input becomes smaller, which, in turn, increases the amplifier current consumption. Large voltage swings at the amplifier input cause little current to flow because the resistance of either the n- or p-channel transistor is high during a large portion of the cycle. On the basis of power considerations, it is best to design the feedback network for a small attentuation.

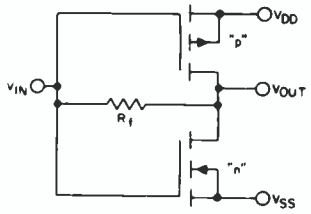


Fig. 5—COS/MOS amplifier.

Equivalent crystal resistance

The equivalent resistance R_r of the crystal should be maintained as small as possible in order to obtain minimum attenutation across the feedback network. For any given circuit, the oscillator current always increases with a rise in crystal resistance. This factor and stability considerations provide strong arguments for the purchase of crystals that have low series resistance, although the usual cost tradeoffs prevail.

Crystal load capacitance

Another factor that influences the over-all power consumption is the size of the pi-network capacitor at the amplifier output. For minimum current consumption, this capacitor, obviously, should be kept small. This condition, however, does not always imply high frequency stability. The choice of the capacitor value first involves a determination of the over-all crystal load capacitance. The phase angle of the feedback network approaches 180° when the crystal equivalent reactive component X_r is equal to the reactance (X_{C_L}) of a capacitor placed in parallel with the crystal, Fig. 4 shows that the effective capacitance across the crystal consists of the two pi-network capacitors in series. If the values of the equivalent reactance X_r at the crystal frequency, as may be determined from Fig. 3b, is equal to the reactance of the crystal load capacitance C_L, then the equivalent value of the two series-connected pi-network capacitors can be calculated from the following relationship:

$$C_L=1/\omega X_r \qquad (1)$$

The value of the load capacitance C_L, in general, is chosen first, and the crystal manufacturer is required to cut the crystal to oscillate at the desired frequency for the specified value of load capacitance.

The choice of a load capacitance is important in terms of over-all power consumption and frequency stability. Higher values of C_L generally improve frequency stability, but also increase power dissipation. The timing industry presently seems to have standardized on values of C_L between 10 and 20 pF.

The choice of the total equivalent load capacitance C_L only fixes the series sum of the two pi-network capacitors. The individual capacitors themselves can be found from the following equations:[1]

$$C_T=4C_L/(1-5fR_rC_L) \qquad (2)$$

$$C_S=4C_L/(3+5fR_rC_L) \qquad (3)$$

The actual value of C_S used in the feedback circuit should be about 3 pF less than the calculated value to allow for the amplifier input capacitance. The value of the amplifier output capacitor C_T should not normally be fixed. A trimmer capacitor should be placed in parallel with, or used in place of, a fixed output capacitor to allow for variations in stray capacitance and circuit components. The mid-range value of the output capacitor combination should be equal to the calculated value of C_T.

Frequency-trimming capability

The required capacitance range for the oscillator trimmer capacitor is determined by the variation in oscillation frequency with a change in load capacitance.[2] The total frequency-trimming range of a crystal-controlled oscillator circuit is mainly a function of the crystal characteristics, or more explicitly, is inversely proportional to

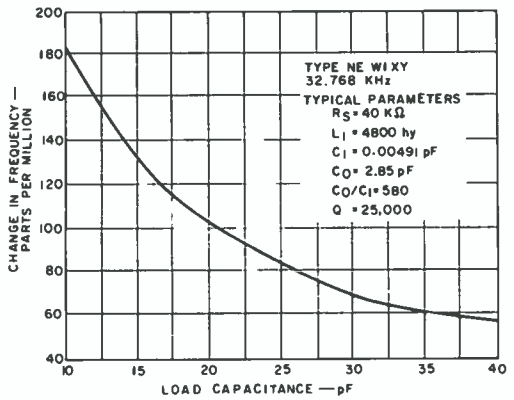


Fig. 6—Frequency as a function of load capacitance for a typical 32-kHz crystal.

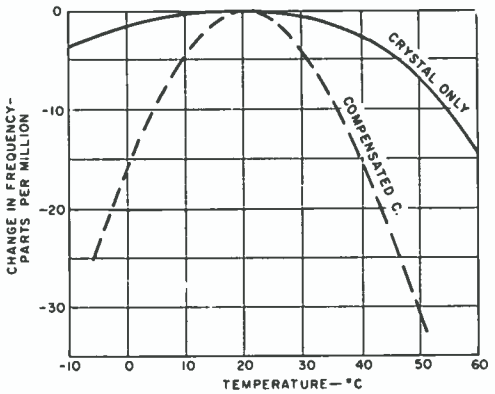
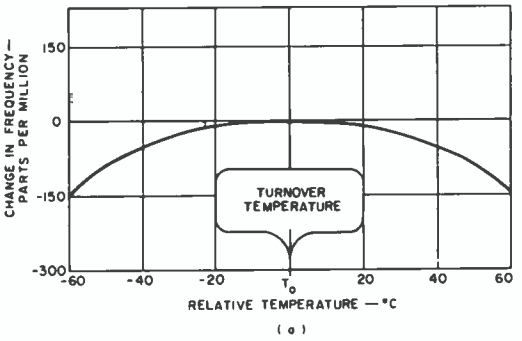
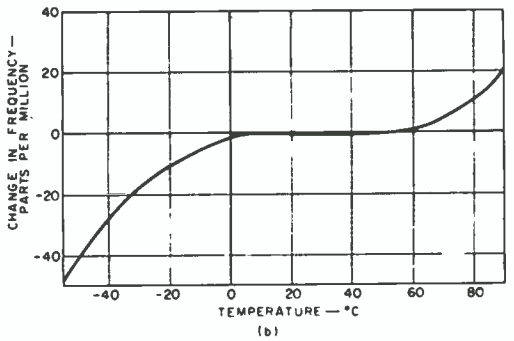


Fig. 7—Effect of temperature on crystal frequency.



(a) XY-Bar and NT cuts.



(b) AT cut.

Fig. 8—Frequency-temperature characteristics for various crystal cuts.

Table II—Trimming data for a typical 32-kHz quartz oscillator crystal.

Trim	*Load capacitance, C_L*			
	5 pF	11.5 pF	20 pF	32 pF
±20 PPM	$^{-0.45}_{+0.51}$ pF	$^{-1.6}_{+2.0}$ pF	$^{-3.7}_{+5.5}$ pF	$^{-8.0}_{+14.7}$ pF
±25 PPM	$^{-0.55}_{+0.65}$ pF	$^{-1.9}_{+2.6}$ pF	$^{-4.5}_{+7.3}$ pF	$^{-9.4}_{+20.5}$ pF
±30 PPM	$^{-0.66}_{+0.79}$ pF	$^{-2.3}_{+3.3}$ pF	$^{-5.2}_{+9.3}$ pF	$^{-10.7}_{+27.9}$ pF

the slope of the crystal reactance curve, shown in Fig. 3b. The slope of this curve is a function of the difference between the resonant frequency f_r and the antiresonant frequency f_a. This frequency difference, in turn, is a function of the crystal capacitance ratio C_0/C_1, where C_0 and C_1 are the inherent shunt and series capacitances, respectively, of the crystal structure, as shown in Fig. 2. The slope of the reactance curve is also a function of the total external crystal load capacitance C_L. As shown in Fig. 3b, this slope decreases as the equivalent reactance increases (*i.e.*, for smaller values of the capacitance C_L). Fig. 6. and Table I show trimming-range data for a typical 32.768-kHz crystal that has a capacitance ratio C_0/C_1 of 580. These data show that smaller values of load capacitance result in greater trimming-range capability.

Temperature stability

Another important oscillator consideration is temperature stability. Most crystals have a negative parabolic temperature coefficient.[2] Fig. 7 shows a typical curve of the variation in crystal frequency as a function of temperature. The frequency of the total oscillator circuit also exhibits a similar temperature dependence. Temperature compensation of the over-all oscillator circuit can be achieved by use of a capacitor that has a negative parabolic temperature coefficient in the pi feedback network.[3] For comparison, Fig. 7 also shows a typical resultant curve for the over-all circuit.

The temperature characteristics of a crystal are determined to a large extent by the crystal cut. Popular low-frequency cuts include the NT and XY bar. The XY bar is the more popular of the two types because it can be made smaller for a given Q and is easier to trim. The disadvantage of a slightly lower shock resistance of XY-bar crystals is compensated by the superior aging characteristics of this type. AT-cut crystals, when used at frequencies greater than 1 MHz, are characterized by excellent temperature stability and ruggedness. Temperature characteristics for this type of crystal cut as well as for the XY bar and NT types are shown in Fig. 8.

Crystal dimensions

Size is also an important consideration in the design of oscillator crysals. The length of quartz required for any given cut is inversely proportional to the square root of frequency. Dimensions for a typical packaged 32-kHz, XY-bar crystal are 0.6×0.2×0.11 in. The smallest XY-bar crystals currently available have dimensions in the order of 0.53×0.2×0.11 in. A 1-MHz AT-cut crystal is significantly larger; however, dimensions again decrease with frequency. Crystal manufacturers are currently working to develop wristwatch-size AT-cut crystals with the anticipation of circuit improvements that will allow low-current operation at high frequencies.

Crystal shock resistance and aging rate

A prime concern of the timing industry today is that of crystal shock resistance and aging. The aging of a crystal results primarily from aging of the mounting material rather than from aging of the quartz itself. The mounting material enters into the crystal equivalent circuit, and the slowest aging rate results when the mount consists of the least amount of supporting material. This condition of course, results in lower shock resistance, and an optimum tradeoff must be achieved. At present, 32-kHz crystals can be made that can withstand a mechanical shock of about 1500 G's applied for 0.5 ms and that have aging rates that result in a frequency change of 2 to 5 parts per million for the first year and essentially no aging thereafter. Any mechanical or thermal shock, however, will interrupt the normal aging process. The aging rate of 2 to 5 parts per million presently appears acceptable

to the timing industry, although, shock resistances of 3,000 to 5,000 g's are desired. This shock level corresponds approximately to the shock experienced by dropping the crystal from a height of one meter onto a hardwood floor.

Practical oscillator circuits

The basic amplifier, feedback-network, and crystal considerations discussed in the preceding paragraphs can be combined in the design of cos/MOS oscillator circuits. In the circuits, the crystal selected has an equivalent resistance R_e of 50 kilohms and is cut to operate at a frequency of 32.768 kHz with a load capacitance C_L of 10 pF. The values of pi feedback-network capacitors C_T and C_S can be calculated by use of Eqs. 2 and 3 as C_T=43 pF and C_S=13 pF. The value of the feedback-network resistance R can be calculated as follows:

$$R=\frac{(3X_e+0.27\,R_e)\ (X_e-0.8\,R_e)}{16\,R_e}$$
$$\approx 1\text{ M}$$

This value is the maximum value of resistance allowed for a minimum feedback-network attenuation of 0.75, a value chosen on the basis of power and stability considerations. The calculated value of R includes any fixed resistance plus the amplifier output resistance. Because the output resistance is often appreciable and varies with supply voltage, transistor size, and threshold voltages, it is generally best to add resistance experimentally until the desired power consumption and frequency stability are reached. The effect of this resistance on operating current and frequency stability can be predicted from data given in Table III for the three different cos/MOS crystal oscillator circuits shown in Fig. 9. In each circuit, the pi-network capacitors C_T and C_S are 39 pF and 10 pF, respectively. These capacitances are slightly less than the calculated values because of stray and amplifier capacitances.

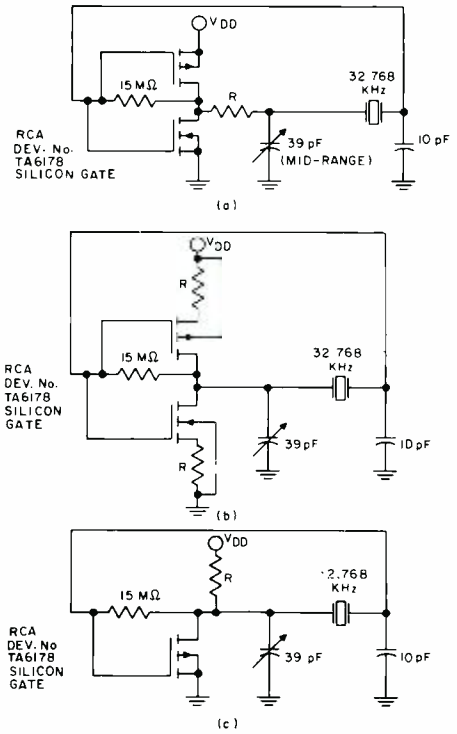


Fig. 9—Typical COS/MOS crystal-oscillator circuits.

Table III—Typical oscillator data.

Circuit (Fig.)	Value of R (ohms)	V_{DD} (V)	Current (μA)	Frequency stability V_{DD}=1.45V ± to 1.6V
9a	0	1.60	4.0	2.8
"	0	1.45	3.1	
"	100 k	160	3.1	2.6
"	"	1.45	2.4	
"	200 k	1.60	2.9	2.6
"	"	1.45	2.1	
9b	100 k	1.60	2.3	0.3
"	"	1.45	2.0	
"	"	1.1	1.5	
"	150 k	1.60	1.8	0.2
"	"	1.45	1.6	
"	"	1.1	.95	
9c	200 k	1.60	5.0	0.6
"	"	1.45	4.4	
"	300 k	1.60	3.5	0.5
"	"	1.45	3.0	

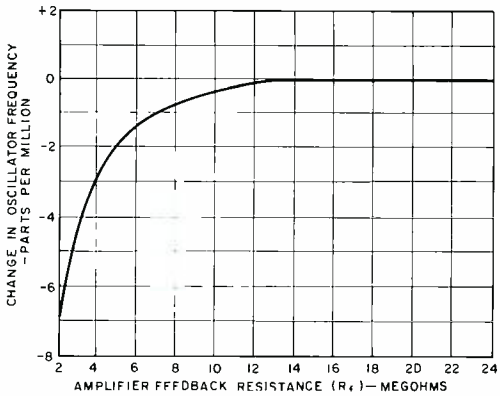


Fig. 10—Oscillator frequency as a function of amplifier feedback resistance

The circuit shown in Fig. 9a combines the amplifier and feedback circuits shown in Figs. 4 and 5. Although theory predicts that an increase in the values of the feedback-network resistor R will result in increased frequency stability, the circuit performance data given in Table III show no significant improvement in this characteristic. This result indicates that the circuit instability can be attributed almost entirely to phase instabilities of the amplifier. This assumption is verified by data taken from the circuits shown in Figs. 9b and 9c in which the required feedback-network resistance is incorporated into the amplifier as a fixed value. The resistors essentially fix the amplifier phase shift so that greater stability results. As the data show, use of these resistors also results in a decrease in the total current consumption. Because of the two fixed resistors, the circuit of Fig. 9b shows the least current consumption and also the greatest stability.

As mentioned previously, the amplifier feedback resistor should not significantly load the crystal feedback network. The resistor value at which loading begins to occur can be determined from a curve of circuit operating frequency as a function of feedback resistance. Fig. 10 shows such a curve for the circuit shown in Fig. 9b. This curve indicates that 15 megohms is a suitable value for the feedback resistor.

Frequency dividers

Because of restrictions on crystal size and cost, oscillator frequencies of 8192 Hz, or higher, are generally used for electronic timing circuits. The use of such high crystal frequencies usually requires division of the oscillator frequency to a more convenient value. Synchronous motors, for example, are often driven by frequencies between 0.5 Hz and 64 Hz. Numeric readouts for digital clocks or wristwatches require pulses at least every second, minute, and hour. The necessity for frequency division becomes clear if one considers the wide variety of timing intervals that may be required for certain applications.

The basic frequency-dividing circuit, shown in Fig. 11, consists of a master-slave D-type flip-flop connected as a binary counter stage. N stages may be cascaded with the final output frequency equal to 2^{-N} times the input frequency. Division by integers other than powers of 2 can also be accomplished by use of gating techniques. For example, a divide-by-60 counter implemented as shown in Fig. 12, can be used to obtain minutes from seconds.

A basic block diagram of a typical digital clock that employs divide-by-60

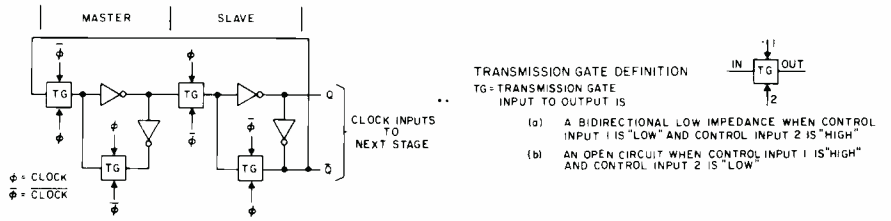


Fig. 11—Basic frequency-dividing stage.

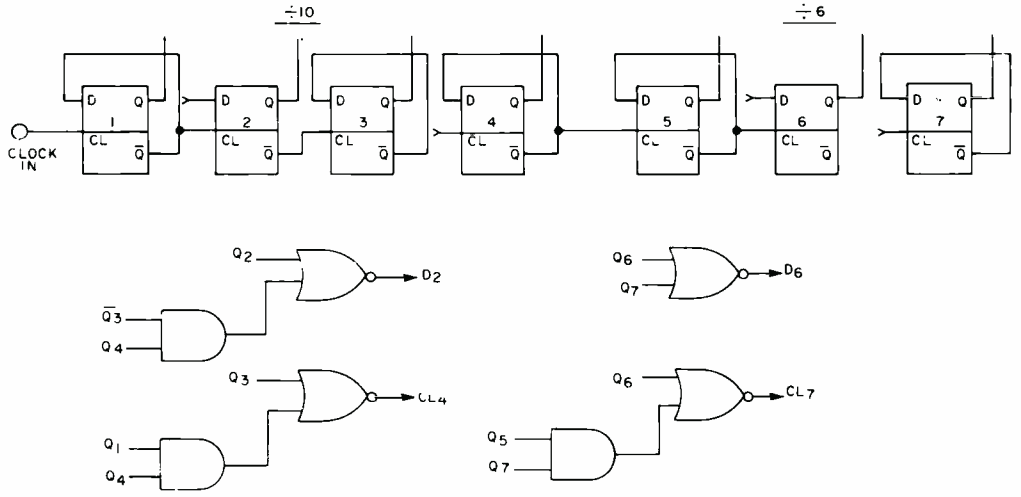


Fig. 12—COS/MOS divide-by-60 counter.

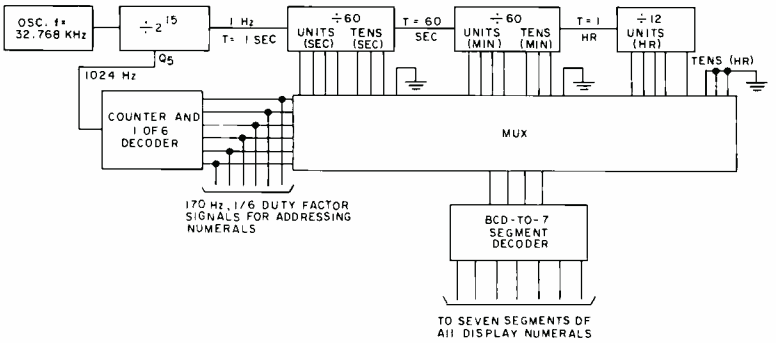


Fig. 13—Typical COS/MOS digital clock.

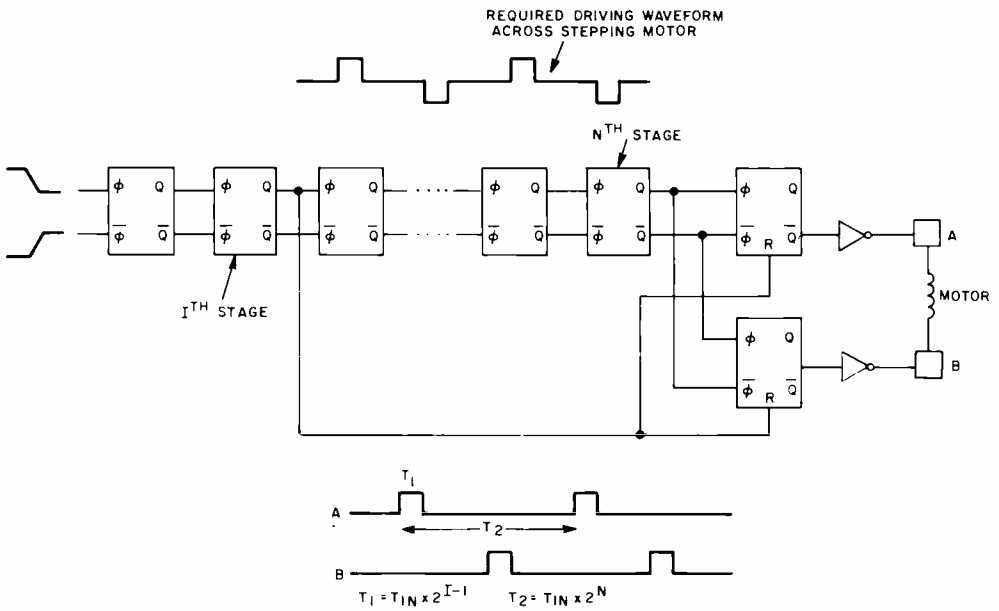


Fig. 14—Generation of required stepping-motor waveforms: (a) required driving waveform across stepping motor; (b) COS/MOS driving circuit and output waveforms applied to motor control winding.

counters is shown in Fig. 13. This display for the clock is designed to be multiplexed in that new information is provided to only one of the six readout characters, while the eye itself holds the previous state of the other five. The multiplexing unit consists of COS/MOS transmission gates controlled by a six-stage ring counter that also addresses each character sequentially. This type of circuit is particularly applicable for driving light-emitting diode displays.

Light-emitting diodes, as well as other readout devices, require some form of driving circuitry which is often unique to the driven device. Other typical readout devices include stepping motors, balance-wheel motors, tuning-fork motors, and liquid-crystal displays.

Motors are frequently driven by low impedance MOS transistor drivers. The waveforms required depend upon the particular type of motor. Rotary stepping motors require a pulsed waveform such as that shown in Fig. 14a. The motor advances one position (*e.g.*, 180°) on each pulse. Fig. 14b shows a COS/MOS circuit that may be used to generate this type of waveform. The crystal frequency and the number of countdown stages for this circuit determine the pulse frequency. The duty factor is controlled by two resettable flip-flops that are clocked inversely by the last counting stage and reset by an intermediate stage. The output waveform from this circuit will have a duty factor that is exactly given by 2^{I-1-N}, where I is the number of the intermediate stage used to reset the shaping flip-flops and N is the total number of frequency-divider stages.

A tuning-fork motor consists of two coils wired in series and wound on either side of the fork. A subdivision of the crystal frequency drives the coils which electromagnetically vibrate the fork. The fork can be linked to an index wheel that, in turn, can drive the hands of a watch.

A balance-wheel motor consists of a coil fixed near the periphery of a pivoted balance wheel. Permanent magnets are attached to one side of the wheel and counterweights to the other. The coil can be energized by pulses supplied to the gate of an n-channel MOS transistor with the coil connected between the drain and the supply volt-

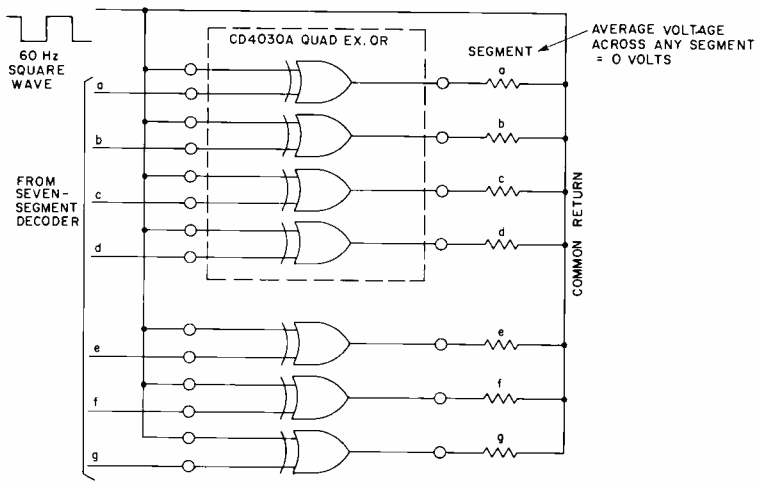


Fig. 15—COS/MOS liquid-crystal driving circuit.

age of the transistor. When the coil is energized, the balance wheel swings toward the coil. The momentum of the wheel moves it beyond the coil, and spring action then forces it back. Repeated cycles generate a back-and-forth type motion which can be linked to a wheel for driving the hands of a watch or clock.

Seven-segment liquid-crystal numerals can be driven as shown in Fig. 15. An AC voltage is required across each segment of the display to assure long life. For this purpose, a 60-Hz square wave is applied to one input of each of seven exclusive-OR gates. The logic state present at the other input determines whether the segment will transmit or scatter light.

Liquid-crystal displays can be made for operation in either transmissive or reflective modes. The transmissive-mode type requires a light source behind the display. The light will either be transmitted or not depending upon the voltage across the segment. In the reflective-mode type, ambient light can be scattered by the liquid crystal material, or reflected from a mirrored surface placed behind the numeral. If displayed correctly, excellent contrast between *on* and *off* segments can be obtained when reflecting or scattering only ambient light.

The light scattering property of liquid-crystal displays offers two major advantages. First, the problem of washout in high intensity light is prevented. Washout has always been a problem with light generating displays. Second, because the displays do not generate light, they require negligible power. In fact, liquid crystals require the least amount of power of any currently available type of display.[4]

Light-emitting diodes are somewhat simpler to drive than liquid crystals because signals to individual segments and/or numerals can be easily multiplexed. Fig. 16 shows a typical multiplexed driving circuit. The n-p-n transistor, which is common to the cathode of all segements in each numeral, can be turned on to address only one particular numeral. The eye will hold the reading from all off segments long enough for at least six numerals to be multiplexed.

COS/MOS timing-circuit applications

The choice of a readout device depends, of course, upon the application involved and to a certain extent upon the individual characteristics of the device itself. Special considerations for readout devices are perhaps best treated in a discussion of special requirements for three important timing-circuit applications, namely, wristwatches, wall clocks, and automobile clocks.

Wristwatches

In any wristwatch application, size and total operating current are perhaps the two most important considerations. The total timing circuitry, together

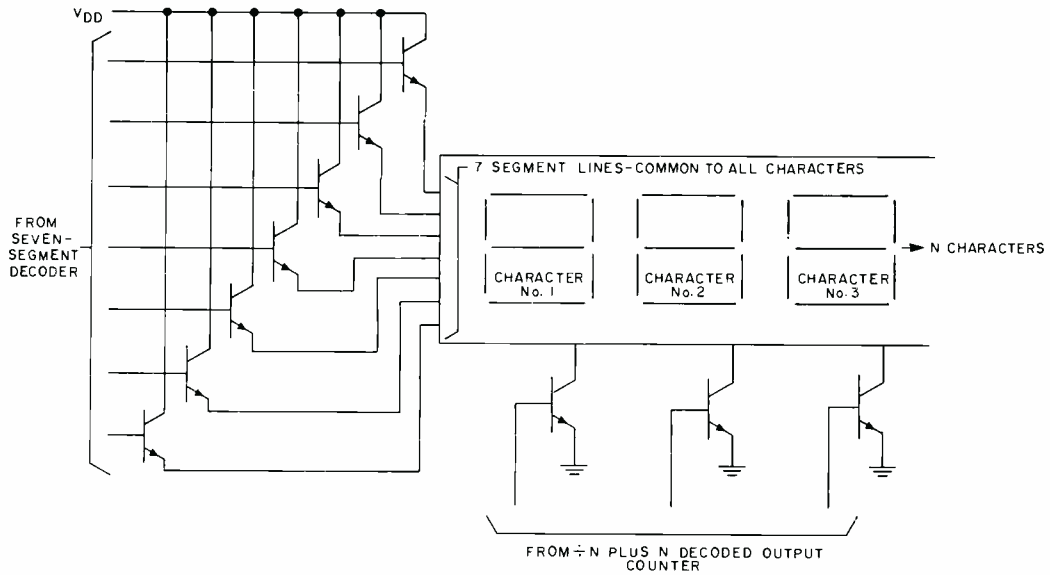


Fig. 16—Multiplexing driving circuit for light emitting diodes.

with the battery and readout device, must fit into a relatively fixed size and have a current consumption small enough to allow at least one year of life. Size and power considerations also become important in crystal selection. The size and cost of a crystal decreases with increases in frequency up to about 1 MHz. The power consumption of the oscillator and counter increases with frequency. On the basis of these considerations, the most popular crystal frequency for wristwatches, at present is 32.768 kHz. Typical packaged sizes for this crystal and various available crystal oscillator circuits were discussed in an earlier section of this paper.

The choice of a readout device also involves considerations of size and power as well as, of course, marketing considerations. If conventional hand movements are chosen, a motor type of drive must be selected. No great size advantage exists over any of the various motor types used in this type of application. In addition, all types can be designed to operate from 1.1 to 1.6 V with average current consumptions of about 10 μA. Sensitivity to vibration, however, is one separating characteristic. Although balance-wheel motors can be designed to compensate to a certain extent for speed variations produced by vibrations, the stepping motor, which is relatively insensitive to vibration, remains superior in this respect. At present, however, the stepping motor is the more expensive of the two types.

Light-emitting diodes require a minimum of two battery cells for proper operation. The required current can be kept to about 2 mA per segment when the diodes are pulsed from a six-stage ring counter, as shown in Fig. 13. A duty factor of 16% is achieved with this arrangement. Because of the high current, however, a continuously-operating battery-powered display is not possible, and a "readout on demand" watch is then necessary.

Table IV—Typical data for Mallory watch cells.

Type	*Voltage* (V)	*Capacity* (μA yrs.)	*Height* (in.)	*Diameter* (in.)
WH3	1.35	25	0.208	0.455
WS 14, Type A	1.55	19	0.210	0.455
W4	1.35	11	0.139	0.455
WS 11	1.55	11	0.164	0.455
10 R 101, (exp.)	1.35	36	0.190	0.610
10 L 19 (exp.)	1.55	27	0.190	0.610
WD 4	1.36	14	0.149	0.594
WD 5	1.36	23	0.110	1.003

Table V—Typical data for 262-kHz oscillator and counter circuits.

Product	V_{DD} (V)	*Oscillator current* (μA)	*Counter current* (μA)	*Freq. Stability* (ppm)
Silicon-gate	1.1	7	7	—
"	1.3	9.5	9	2.0
"	1.5	11.5	10	—
"	1.6	12.5	11	1.4
Low-voltage	2.2	21	10	—
"	3.0	35	13	1.2
				—
				1.8

Continuously-operating liquid-crystal displays are possible and practical. RCA wristwatch displays employ liquid-crystal material having resistivities of about 5×10^9 ohms/cm which at a 0.5 mil spacing results in a resistance of 6.3 megohms/cm^2. With all segments energized, the display only consumes about 1 μA of current at 15 V. Liquid crystals, however, require a minimum supply of 12 V to assure good contrast between *on* and *off* segments. For single-cell operation, a DC-to-DC converter must be used to step the voltage up to the required 12-to-15-V level. Transformer and capacitor voltage-doubling circuits with conversion efficiencies of about 75% are typically used for this purpose.

Since current consumption is such an important consideration for wristwatch circuits, the careful consideration given to the choice of a battery is easily understood. Small silver-oxide and mercury cells are presently popular for wristwatch use. Pertinent information on these types of Mallory cells is shown in Table IV. Most of the cells listed will last at least one year with a motor current of 10 μA, and a total oscillator and divider current less than 5 μA at an oscillator frequency of 32.768 kHz. The voltage for both types of cells is relatively constant during the active life listed and falls off rapidly thereafter. Typical end-of-life voltages are 1.1 V for mercury cells and 1.45 V for silver-oxide cells. Either type of cell works equally well with RCA silicon-gate COS/MOS circuits which operate from supply voltages as low as 1.1 V.

Wall clocks

Size and power limitations for clocks are not as restrictive as those for wristwatches. For this reason, lower-cost, higher-frequency crystals may be used. The optimum range of crystal frequencies presently appears to be from 131 kHz to 524 kHz. All the oscillator considerations given previously for operation at 32 kHz apply equally well to this higher frequency range. The oscillator circuit configuration shown in Fig. 9b is still the optimum type; however, the value of the source resistors must be decreased to assure adequate gain at the higher frequencies. Source resistors are often best chosen experimentally by gradually increasing the resistance until an output voltage swing of 30 to 70% of the supply voltage V_{DD} is reached. Data taken from a typical 262-kHz oscillator circuit that employs two 10-kilohm source resistors and a DT-cut 262-kHz crystal are shown in Table V. The table also shows typical counter current.

The most popular readout devices for clocks are conventional hand movements and liquid-crystal displays. Continuously operating light-emitting-diode numerals consume too much current even for long life of C- and D-size batteries. In contrast, a typical RCA four-digit liquid-crystal display, having a 0.4×0.6-in. numeral consumes only 100 μA of current with all segments energized.

Motors for driving the clock hands are typically of the balance-wheel or continuously rotating synchronous types. Sensitivity to vibration is usually not a restriction; hence, the balance wheel motor can be successfully used in place of the more expensive stepping motor. Clock motors typically require about

Table VI—Life data for typical batteries.

Eveready type no.	*Mallory type no.*	*Size*	*Type*	*Life (days)*
915	M 15 F	AA	Carbon-Zinc	150
E 91	MN 1500	AA	Alkaline	200
935	M 14 F	C	Carbon-Zinc	385
E 93	MN 1400	C	Alkaline	575
950	M 13 F	D	Carbon-Zinc	800
E 95	MN 1300	D	Alkaline	1100

All life data assumes a continuous drain of 250 μA and an end-of-life voltage of 1.1 V.

300 to 450 μW of power, or average currents of 200 to 300 μA at 1.5 V.

These currents, together with the oscillator and counter currents given in Table V, can now be compared with typical battery capacities. Battery information extrapolated from published Eveready data on popular AA-, C-, and D-size cells is listed in Table VI.[5] Most of the battery current is consumed by the motor, and if a total current of 250 μA is assumed, the data show a carbon-zinc C cell as the minimum size battery required for one year of life.

Auto clocks

Auto-clock circuits are somewhat unique in that power considerations are not nearly as restrictive as in other portable applications. Although the low-power feature of cos/MOS circuits is helpful, the main advantages obtained from the use of cos/MOS in automobile clocks, or in any automotive application, are those of wide operating voltage and temperature range and high noise immunity.

With little restriction on power, the choice of a crystal depends mainly on cost. Crystals typically used for automobile timing applications are AT-cut types that operate at frequencies between 1 MHz and 4.2 MHz. The oscillator considerations discussed earlier also apply to these frequencies; however, as the frequency increases, it becomes increasingly difficult to mantain a low starting voltage at a low current. At high frequencies, the starting voltage and current are inversely proportional and are controlled mainly by the values of the capacitors in the pi-type feedback network and the size of the cos/MOS amplifier transistors. For minimum starting voltage, relatively small capacitors should be used in the pi-feedback network, and no source resistors should be added to the amplifier. As indicated by data taken on the circuit shown in Fig. 9b and shown in Table VII, low power can still be maintained even when the source resistors are not used.

The upper limit of the crystal frequency depends not so much on power consumption as on the minimum supply voltage allowed for circuit operation. The minimum automobile battery voltage is generally considered to be 5 volts; however, the supply voltage for the timing circuit can be considerably less than this value depending upon the design of the transient protection circuit[6]. Table VIII lists minimum cos/MOS supply voltages for typical oscillator circuits. The values shown permit design at two temperatures. The lower temperature is often considered adequate by auto companies with the opinion that the minimum battery voltage of 5 V rarely, if ever, occurs at high temperatures.

Table VII—Typical high-frequency data for COS/MOS oscillator and counter circuits (low-voltage product).

V_{DD} (V)	Freq. (MHz)	Oscillator current (mA)	Counter current (mA)	Motor current (mA)
5	1	0.28	0.125	2 to 5
12	1	1.3	0.275	
5	2	0.37	0.250	5 to 10
12	2	1.5	0.550	
5	3	0.40	0.375	3 to 8
12	3	1.9	0.825	
5	4	0.43	0.500	8 to 20
12	4	2.3	1.1	

The oscillator in a typical auto clock circuit is followed by a number of frequency-dividing stages, the last stage of which is frequently used to drive a motor. Long counter chains are required because of the high oscillator frequency; however, the power dissipation of cos/MOS circuits is so low that the number of stages is only restricted by chip-size limitations. Because cos/MOS circuits consume current only during switching transitions, each counter stage averages one-half the current of the previous stage. The first counter stage, therefore, consumes as much current as all of the following stages combined for a counter of infinite length. Little difference, then, exists between the power consumption of a ten-stage or thirty-stage cos/MOS counter. Table VII lists, in addition to the oscillator current, typical values of counter current, as well as some typical ranges of peak and average motor currents.

Other applications

Although wristwatches and clocks of various types are important applications of cos/MOS timing circuits, they are certainly not the only timing applications which can benefit from the unique features of cos/MOS logic. Applications such as fuze timers, feeding systems, automatic sprinklers, incubator timers, and other similar systems can be designed from information provided on the oscillator and counter with only the output device unique to the particular application. Automobile applications for cos/MOS circuits are almost endless. One can think of speed controllers, digital speedometers, miles-per-gallon indicators, and perhaps even estimated-time-of-arrival indicators that, on the basis of the given total mileage, would update the time on a dynamic basis from information provided by the speedometer, odometer, and clock.

Table VIII—Minimum operating voltages for COS/MOS integrated circuits.

	Low-voltage product				Silicon gate product			
Frequency (MHz)	1	2	3	4	1	2	3	4
Min. voltage at 25°C	2.9	3.1	3.5	4.0	1.6	2.0	2.6	3.0
Min. voltage at 82°C	3.0	3.3	4.0	5.0	1.8	2.6	3.4	4.0

Conclusions

The primary advantage of electronic timing circuits over conventional mechanical methods of timekeeping lies in the greatly increased accuracy permitted by the highly stable crystal-controlled oscillator circuit. Although crystal oscillator circuits have existed for some time, their usefulness in portable applications has been somewhat limited because of the high current consumption required by the following digital logic. The advent of cos/MOS integrated circuits now permits the design of complete low-power timing systems. The impact of cos/MOS on timing applications is perhaps equalled by the recent development of liquid-crystal displays and DC-to-DC converters that allow low-power continuously operating digital displays. Certainly, no great technological barriers now exist for the use of electronic timing circuits in a wide variety of applications. The search, no doubt, will always continue for the ideal timekeeping device; however, it should be apparent from the information presented that the ideal timekeeping unit can now be more closely approached.

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Doing your own thing— COS/MOS custom design

G. J. Waas

There comes a time in the course of a product design when the engineer must choose between designing-in a custom circuit or fabricating with off-the-shelf standard parts. This is not a trivial decision. The reasons for choosing COS/MOS as the circuit technology are adequately covered elsewhere[1,2]; it suffices to say that COS/MOS offers the high packing density of MOS with logic speeds approaching that of TTL. It is this high packing density and low power that often makes COS/MOS a candidate for custom designs. This article delineates some of the reasons for choosing either a standard circuit or custom approach and briefly discusses the steps necessary to move from a design concept to a finished custom device. An understanding of the capabilities and limitations of COS/MOS circuit development is necessary to exploit the full potential of custom design.

WITH OVER 50 STANDARD PARTS AVAILABLE, there are still a number of occasions when a custom design is the only way to go. The most pressing reason is a space limitation. Usual applications falling into this category are watches, clocks, heart pacers, fuzes, pocket pagers, and aerospace equipment. In these applications, a unique design results in the minimum number of transistors exactly designed for the specific task. This approach results in the minimum package count for the final design with a reduction in interconnections. Miniaturization and reduction of mechanical connections are positive steps toward increased reliability.

Another advantage of the custom approach is that special technology can be applied. Silicon-gate circuitry will operate down to 1.1 V. If required, special pin-outs and non-standard packages can be used. In some circumstances, chips for wire bonding and non-hermetic beam-leaded chips have been supplied. In the near future, nitride-passivated, hermetic, beam-leaded chips will be available. If required, resistors, capacitors, and zener diodes can be integrated on special order.

All of the advantages stated above must be weighed against the potential disadvantages of a custom design. The major drawback is a lack of flexibility. Situations have occurred in which a change in specification requires a circuit or logic change in the custom chip. In almost every instance, it has been necessary to go through a complete redesign. This change is not only expensive but time-consuming. Another disadvantage is the time delay involved in the design and implementation of the custom device. The time can range from three to seven months for initial samples, depending upon complexity. Production quantities can take an additional three months.

The use of standard circuits is recommended for fastest turn-around time from design to hardware. Standard circuits permit complete flexibility if future changes are contemplated. If volume requirements are small, the use of standard circuits eliminates the design charge for a custom circuit. A custom circuit is the recommended approach when additional time exists for design; a large production volume is usually a prerequisite, and a proven design specification is an absolute necessity.

Years of experience in developing COS/MOS circuits have resulted in a number of interface options between the customer and RCA. In general, it is desirable to establish the interface with RCA in the early stages of the program. The COS/MOS group is prepared to interpret the customer's requirements in terms of the available technology and to make a major contribution toward reaching the customer's equipment design objective. Not only will an early interface bring RCA's capabilities to bear sooner, but the customer will be able to apply the available technology more efficiently. If the user's designers are thinking in terms of cell functions rather than individual gate functions, a more efficient equipment design will result. However, because of the complex nature of LSI and the requirements for an extremely close customer vendor relationship, RCA will consider alternate contact points and procedures if desired by the customer.

Implementing a custom design

Customers have different preferences for the method and manner of interaction with RCA in the development of their circuit. To establish prefer-

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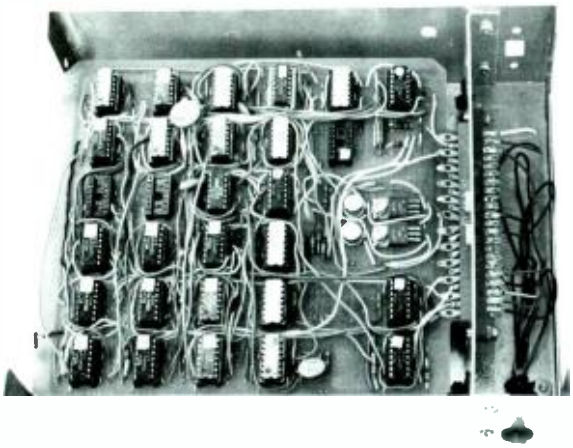

Fig. 1—Typical breadboard of COS/MOS circuits.

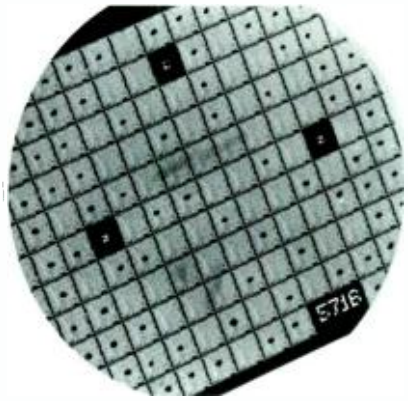

Fig. 3—Rejected pellets are marked with an ink dot after testing.

ence, it is necessary to examine the discrete steps in the development of any COS/MOS circuit:

1) *Logic design using COS/MOS standard-cell elements*—Logic design for custom circuits must have a goal other than minimization of gates. The new goals are minimization of chip area and external pins.
2) *Breadboard construction and verification against specification*—The fabrication of a broadboard with COS/MOS circuits, as shown in Fig. 1, is the best way to illustrate the advantages of the technology. The breadboard built with standard components is an accurate logic representation of the final circuit.
3) *Generation of electrical test program*—The testing of a complex logic array is a tedious and time-consuming task, but unless a proper and exhaustive test program is written, the custom design is incomplete.
4) *Drafting of the design of the composite layout*—Drafting the layout consists of interconnecting standard cells to satisfy the detailed logic design. Care is taken to minimize area, simplify fabrication, and maximize production yields.
5) *Digitizing of the layout*—The digitizer is an electromechanical device that translates the composite layout into coordinates (spaced 0.1 mil) that are stored on magnetic tape. The tape is used to drive the automatic drafting machine.
6) *Verification of digitizer check-plot*—The information stored on magnetic tape during digitizing is fed to a drafting table that reproduces (usually at 500×) the different mask levels needed to produce the design. These levels are verified for accuracy and checked against each other. At present, part of this checking is performed by computer and part by the responsible project engineer. If any errors are found, the tape is corrected and a new check-plot is drawn.
7) *Reduction of digitizer tape to 10× reticle*—After the check plot is verified, the contents of the magnetic tape are transferred to glass reticles. These reticles are the master print for the generation of final masks. They are reproduced ten times larger than normal and are visually checked by microscope for imperfections.
8) *Generation of final mask levels by step-and-repeat*—The reticles are reduced ten times and the final masks made by step-and-repeat procedures.
9) *Wafer processing in model shop*—Initial wafers are run in the Engineering Model Shop, shown in Fig. 2, under carefully controlled conditions.
10) *Wafer electrical test*—Test transistors at specific locations on the wafer are checked to monitor the diffusion and other fabrication steps during Model-Shop processing.
11) *Pellet electrical test and inking*—The wafers are tested for leakage and functionality through the expected operating-voltage range. The test program used is the one generated in step 3 above. Reject pellets are marked with an ink dot, as shown in Fig. 3.
12) *Wafer scribing, separation, and pellet sort*—The tested wafer is scribed, cracked, and the pellets separated into unmarked good pellets and inked reject pellets.
13) *Mounting and bonding in package*—The good pellets are mounted in the appropriate package and wire bonded to the pin terminals. Some customers do not wish to have packaged devices; they buy pellets for assembly in specialized arrays.
14) *Visual inspection, final sealing, and hermetic leak testing*—The mounted and bonded pellets are visually inspected before sealing. The sealed, packaged unit is tested to assure that it is hermetically sealed.
15) *Final electrical testing on packaged units*—A stringent electrical test is performed on the packaged units to limits somewhat tighter than the cus-

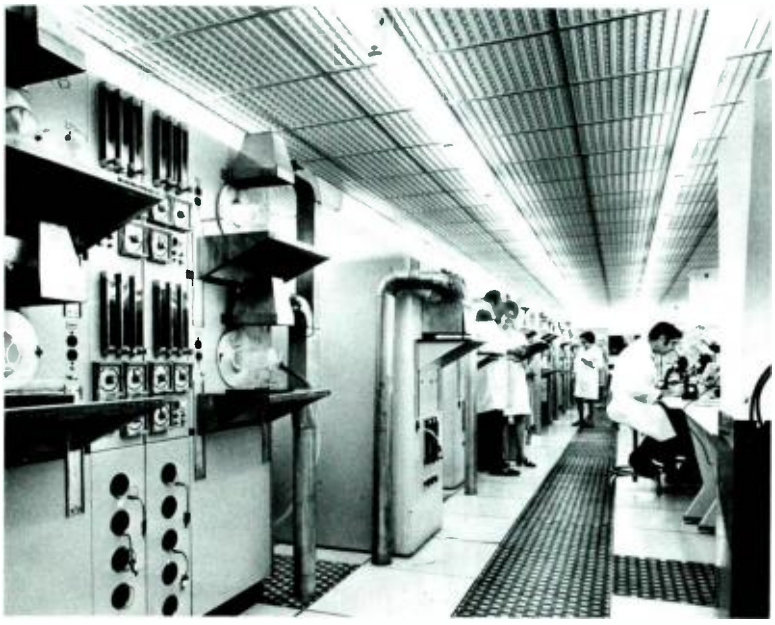

Fig. 2—Initial wafer processing is done under carefully controlled conditions in an Engineering Model Shop.

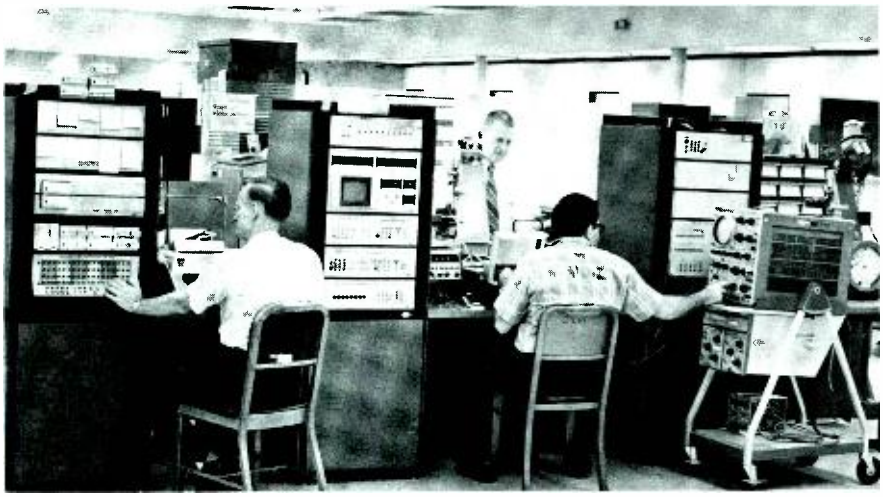

Fig. 4—Automatic high-speed tester for final electrical tests.

tomer has specified; the automatic high-speed tester shown in Fig. 4 is used.

16) *Shipment to customer for approval*—The units are shipped to the customer for his final approval.

17) *Release for production*—Upon receipt of the customer's approval, all engineering prints and procedures are reviewed, updated, and made ready for production.

The Solid State Division is prepared to be completely flexible in choosing where the customer may participate in the design. If a customer is completely familiar with RCA COS/MOS layout rules and is prepared to assume responsibility for logic design and final mask generation, RCA will process and deliver wafers with guaranteed threshold limits and test-transistor performance. In this method of operation, RCA acts only as a model shop. A number of options exist for areas of interface and, in general, the manner and method of interface is a function of the capabilities of customer and vendor. The usual circumstance is that RCA assumes complete responsibility for the overall task.

Custom LSI limitations

To efficiently implement an LSI design, RCA must understand the customer's equipment requirements and design procedures, and the customer must become familiar with LSI design tradeoffs. For larger systems using more than one package, it is desirable that the customer:

- Use conventional packages.
- Maximize gates per pin in a single package.
- Partition such that high data rates are internal to a chip while low-frequency signals are transmitted between chips.
- Order logic design to reduce the problem of on-chip interconnection; irregular logic generally requires lengthy and space-wasting metal runs.
- Minimize the number of pins by using serial data transfer, encoded control signals, or by multiplexing of pins.

A major consideration in any chip design is the size of the pellet: pellet size has a direct bearing on yield and cost. While it is desirable to reduce the system cost by minimizing the number of chips, it is necessary to recognize that an optimum cost per gate can only be achieved by the proper chip size and complexity. Fig. 5 shows the classic curve that demonstrates this concept. To a first approximation, chip size is a function of the number of devices contained on the chip. However, this approximation can be misleading because the interconnecting metal runs for a random logic array can consume much more area than the active devices. An example of the extremes of packing density can best be illustrated by the fact that, with an orderly logic layout minimizing metal runs, it is possible to pack up to 2000 devices on a chip measuring 150 by 150 mils. With a random logic layout requiring extensive metal interconnecting runs, it may not be possible to pack 750 devices on the same 150 by 150-mil chip.

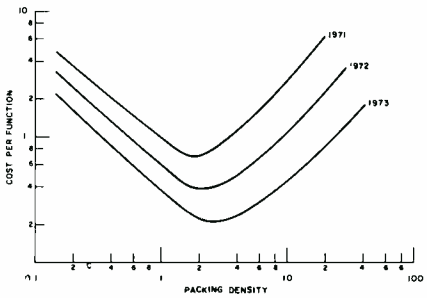

Fig. 5—Tradeoff between chip complexity and cost.

Table I—Cell area for some typical logic elements.

Logic Elements	*Cell Area (Square Mils)*
Inverter	20
2-input NAND	23
8-input NAND	67
8-input NOR	67
R-S flip-flop	49
Binary counter with reset	185
D flip-flop with set-reset	210
3 to 1 multiplexer	120
Exclusive OR gate	95
AND/OR gate	56

A tabulation of cell area for some typical logic elements is given in Table I. It should be noted that the Table is incomplete, and that an examination of the full arsenal of logic elements will show that certain elements are preferred for minimum cell area. The interconnection area required for metal runs can be considerable, and chips with random logic will be large; in general, for a complex chip, the metal-run area can approach three times the area of the active logic elements.

Conclusion

While no mention has been made of development time or cost, it should be obvious that both are highly dependent upon the job complexity and the amount of customer participation. In all cases, full advantage is taken of advanced computer-aided design methods developed by RCA. Design-automation programs and man-machine interactions are combined to provide maximum flexibility, fast turn-around, and minimum cost. This total capability provides complete and efficient development of prototypes.

While the techniques exist to implement larger scale designs rapidly and economically, it is necessary that a close customer vendor relationship be established to assure highest efficiency. The interface between RCA and customer is extremely flexible, and coupling can be established at many levels, but it is axiomatic that the customer is most familiar with his system requirements, and RCA is most familiar with COS/MOS LSI design trade-offs. The optimum situation will take maximum advantage of the knowledge and skills of both parties.

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2. *COS/MOS Digital Integrated Circuits*, RCA Solid State Databook Series SSD-203.

COS/MOS integrated circuits in the automobile environment

D. K. Morgan*

A variety of functions required in typical automobile systems can be readily implemented by COS/MOS monolithic integrated-circuit technology. The main emphasis of this paper, however, is placed on system approaches to the use of COS/MOS integrated circuits with light-emitting diodes, incandescent display devices (Numitrons), and liquid crystals in digital-display automobile clock systems.

ANY COMPONENT or system used in an automotive application must be capable of reliable performance under the following operating conditions:

1) The DC operating voltage supplied by the automobile battery can vary from 0 to 22 V and is nominally in the range of 11 to 13 V.
2) The automobile supply may contain high-energy positive-voltage transients that have peak values of up to 120 V and low-energy negative-voltage transients that can extend to −75 V. In addition, improper system installation can result in an accidental reverse bias of −18 V.
3) The temperature varies from −40°C to +75°C.

Basic features of COS/MOS integrated circuits

The COS/MOS integrated circuits produced by RCA have a guaranteed noise immunity equal to 30% (45% typically) of the operating supply voltage for both high and low logic states. For example, if the supply is 10 V, a COS/MOS device will not change from a high state (logic-1) to a low state (logic-0) when the input decreases to 7 V. Similarly, if the input is at 0 V (logic 0), the device will not change logic state for noise signals up to 3 V. Under maximum rated conditions, the power dissipated by a COS/MOS device, typically, does not exceed 200 mW. In addition, COS/MOS integrated circuits have an operating supply-voltage range of 3 to 15 V and an operating temperature range of −55°C to +125°C.

The inherent high noise immunity, extremely low power dissipation, and broad tolerance to wide variations in supply voltage and operating temperature make COS/MOS integrated circuits particularly well suited for use in automotive applications. Except for the high-voltage transients that may be encountered in the automotive supply, COS/MOS devices could be operated directly from the automotive electrical system.

Transient voltages in an automotive supply may be produced by field decay and "load dumping" from the alternator. The field-decay transient is a negative-going exponential pulse produced in automobiles that are equipped with an alternator warning light. Whenever the automobile ignition switch is turned *off*, a negative-going pulse is generated as a result of the interruption of the alternator field current by the voltage-regulator relay. The energy stored in the alternator field at that time is dissipated in the field-discharge resistor, the alternator warning lamp, the relay coil, and any load impedance connected to the accessory terminal of the ignition switch. Analysis shows that, under worst-case conditions, the peak value of this transient may reach −75 V and that the voltage will decay to ~0 V in 300 ms.

The load-dump transient results from accidental removal of the load from the alternator, such as may occur with a loose battery cable. If the battery were being charged at the maximum rate and a battery cable suddenly became disconnected, the output of the alternator would seek its open-circuit value. The open-circuit value of the alternator output voltage is determined by the engine speed, the alternator field current, and the number of loads still connected to the alternator. The load-dump condition results in a positive-going transient-voltage surge that may have a peak value as high as 120 V. The time constant of this transient is the same as that of the field-current transient (300 ms).

The low power consumption of COS/MOS integrated circuits makes possible the use of relatively simple schemes to isolate and protect these devices from excessive automobile power-supply variations and transients. The type of protection scheme used varies with the application. Several types are discussed subsequently in this paper.

Automotive applications

Extensive evaluations are currently being made of the use of COS/MOS devices in automotive clock applications. The RCA-CD4045A COS/MOS 21-stage ripple counter has been used in the electronics section of an experimental automobile clock. The CD4045A circuit transforms the stable pulsating output of a quartz-crystal oscillator into a control signal for an electric motor that drives a mechanical readout such as a conventional dial-and-hand unit or a digital counter. The quartz-crystal clock surpasses current production units with respect to both accuracy and reliability.

Experiments are also being conducted on the use of COS/MOS devices to provide the electronic functions for a sophisticated clock system that can be used as the master timing standard for the entire automobile. This clock system must supply the time reference for many different automotive functions and is required to provide fixed-time control signals that do not vary with changes in supply voltage and operating temperature. The following types of circuit functions, which can also be provided by COS/MOS devices, would be time-controlled by the master clock system:

Emergency flashers;
Delayed headlight shutoff;
Frequency control of DC-to-AC inverter;
Turn-signal flashers;
Control signals for multiplexed "one-wire automobiles";
Timing standard for comparison of vehicle speed or engine rpm;
Time delays after starting of engine;
Windshield-wiper speed and pause control.

The following list indicates other types of automotive functions that can be provided by COS/MOS integrated circuits:

Antiskid braking control;
Seat-belt interlock control that prevents the engine from starting unless the seat belts are properly fastened;
System-performance indicators and monitors—including fuel-quantity indicator, odometer, physiological driving-fitness index, and brake-fluid sensors; and
Automatic transmission control.

The functions listed above are but a small sample of potential applications.

*Mr. Morgan's photograph and biography appear in an article he has co-authored on page 69.

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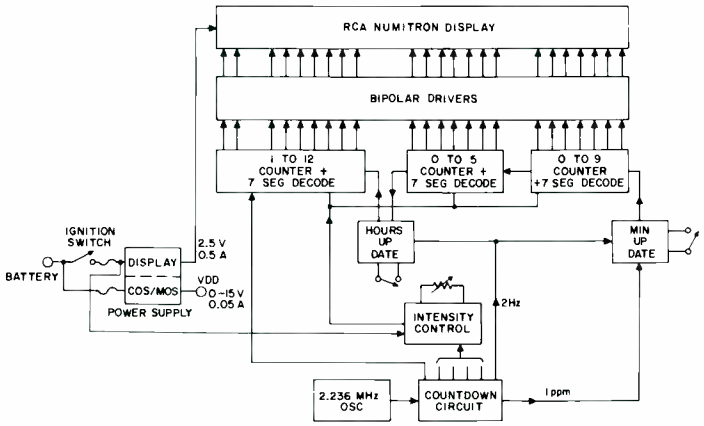


Fig. 1—Block diagram of Numitron clock.

Digital-display automobile clock systems

Consideration is being given to the development of digital-display automobile clock systems in which the electronic circuitry required to convert the signal from a quartz-crystal oscillator into the drive signal for a numeric display can be integrated into one or two MSI COS/MOS chips. This type of clock system includes four basic sections:

DC power supply;
Logic-and-display-driver circuitry;
Display system; and
Frequency standard.

The circuit requirements for the digital-display clock are determined, to a large extent, by the types of display devices to be used. Prototype models of digital-display clocks were designed and constructed to evaluate the feasibility of three types of display devices:

Incandescent readouts (RCA Numitrons);
Light-emitting diodes (Monsanto MAN-1 types); and
RCA liquid crystals.

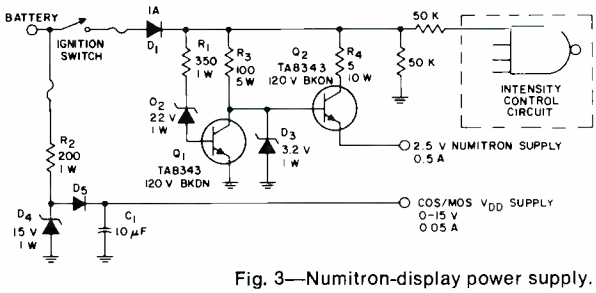


Fig. 3—Numitron-display power supply.

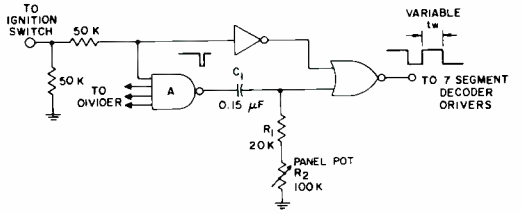


Fig. 4—COS/MOS intensity control for Numitron clock.

These types of display devices were selected for the evaluations on the basis of their compatibility with the range of supply voltage available in an automobile.

Clock system with Numitron display

Fig. 1 shows a block diagram that illustrates the interconnection of the basic functional sections of a digital-display automotive clock that uses Numitron display devices. Fig. 2 shows a photograph of the prototype unit.

Power-supply section

The power supply used in the Numitron clock is designed to protect the COS/MOS devices and the Numitron displays against the +120-V and −75-V transients and the accidental −18 V of reverse bias that may be associated with the automobile supply.

Fig. 3 shows the circuit diagram for the clock power supply. A voltage regulator circuit—resistor R_2, zener diode D_4, capacitor C_1—controls the V_{DD} supply voltage. The V_{DD} is voltage unregulated when the input voltage is within the range from 0 to 15 V. Because of the wide operating voltage range of COS/MOS devices, a rather simple regulator is adequate. When the input to the regulator is greater than 15 V, zener diode D_4 conducts, and the COS/MOS V_{DD} supply is maintained at approximately 15 V. Zener diode D_4 and the value of resistor R_2 were selected for their ability to handle the energy contained in the +120-V transient. When the input to the regulator is driven negative by the −75 V transient, diode D_4 conducts and diode D_5 becomes reverse-biased. Capacitor C_1 maintains a voltage supply to the COS/MOS devices so that the clock does not lose time. If the supply to the clock should be reversed in polarity, diode D_5 will protect the COS/MOS devices.

Fig. 2—Photograph of the Numitron clock.

Diodes D_1, D_2, and D_3, transistors Q_1 and Q_2, and resistors R_1, R_2, R_3, and R_4 form the Numitron-display regulated supply. As shown in Fig. 3, zener diode D_3 and transistor Q_2 conduct when the input voltage is between 4 and 22 V. The Numitron-display voltage is maintained at 2.5 V, or approximately 3.2 V minus the V_{BE} drop across transistor Q_2. The 2.5-V value is used for the Numitron display voltage because this value provides for optimum life expectancy of the Numitrons and sufficient brightness of the display. The Numitron supply is regulated to approximately 2.5 V when the input voltage is between 4 and 22 V and will follow the input between 0 to 4 V. When the input to the Numitron regulator is greater than +22 V, zener diode D_2 and transistor Q_1 conduct to turn *off* transistor Q_2. At the same time, the Numitron supply voltage decreases to zero volts and turns *off* the Numitron display. This feature protects the Numitron displays from the +120-V transient. It should be noted that transistors Q_1 and Q_2 are high-voltage types that have breakdown ratings greater than +120 V. Diode D_1 protects the Numitron regulator from the −75 V transient and an accidental reverse bias. The regulator maintains a fairly constant output over the automobile temperature range to assure uniform Numitron brightness.

Logic-and-display-driver section

Fig. 2 shows the COS/MOS logic devices that form the heart of the digital clock. Although the clock is shown constructed from standard available parts, all of the COS/MOS logic used could be realized from one or two custom COS/MOS MSI chips.

The COS/MOS circuitry consists of an oscillator amplifier that provides the frequency reference;

A countdown chain that divides the oscillator frequency down to 1 cycle per minute;
A divide-by-60 counter with 7-segment

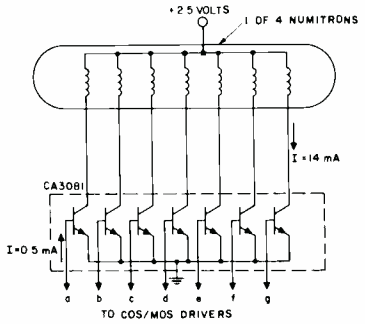


Fig. 5—COS/MOS-to-Numitron-display interface.

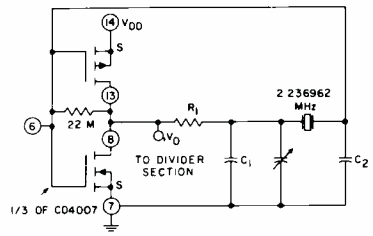


Fig. 6—Crystal oscillator circuit using RCA type CD4007.

decoders and driver outputs for the minutes display;
A divide-by-12 counter with 7-segment decoders and driver outputs for the hours display;
Associated updating circuitry for the hours and minutes counters, and
An intensity control that regulates Numitron brightness by means of an external panel potentiometer.

Fig. 4 shows the intensity-control circuit for the Numitron display. This circuit consists of a NAND gate and the RC network formed by the 0.15 μF capacitor C_1, the 20-kilohm resistor R_1, and the 0-to-100-kilohm potentiometer R_2. The NAND gate A shapes three consecutive frequency outputs from the divider section into a narrow, pulsed, low-frequency signal. The narrow pulsed signal is fed into the variable RC network which controls the duty factor of the 7-segment decoder and drivers. The duty factor can be varied from approximately 50 to 100%. The intensity control is incorporated at the logic level to reduce display power requirements. If the regulator were used to vary the intensity of the Numitron display, additional power would be consumed in dropping the additional voltage.

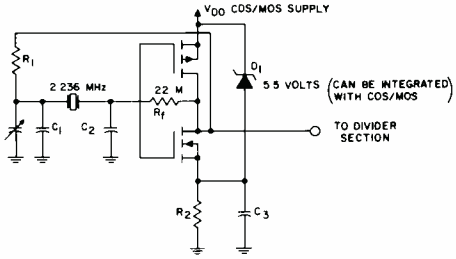


Fig. 7—Alternate COS/MOS oscillator circuit for Numitron clock.

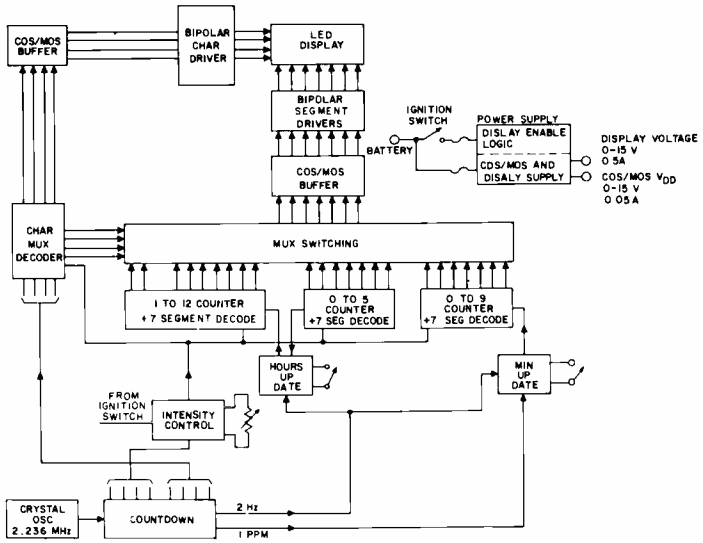


Fig. 8—Block diagram of the LED clock.

The cos/MOS-to-display interface is accomplished with bipolar drivers, as shown in Fig. 5. The cos/MOS devices are unable to drive Numitron current levels directly; therefore, bipolar integrated-circuit drivers are utilized. Four RCA CA3081 integrated circuits, each of which provides seven driver transistors, are used for this section of the clock.

Display section

Of the various incandescent display types, the Numitron family (DTF137) is most practical with respect to brightness, temperature compatibility, size, life expectancy, and ruggedness. Items to be further considered, however, are cost, diode isolation for multiplexing, power drain, and supply regulation requirements.

In the prototype evaluation model, the Numitron display was designed to operate at an output intensity of 4000 foot-lamberts per segment (typical). The Numitron clock is designed to save power when the display is not *on*; the Numitron regulator is turned *off* whenever the ignition switch is in the *off* position. The ignition switch also turns *off* the base current to the bipolar drivers; therefore only the oscillator and logic portions of the cos/MOS circuitry dissipate power when the ignition is *off*. Multiplexing was not used in the prototype because of the diode isolation required for each segment.

Frequency-standard section

Fig. 6 shows the oscillator circuit used for the Numitron clock. The oscillator provides maximum temperature stability because of the temperature-compensated components in its feedback network. An AT-cut crystal, one of the more economical crystals available, is used in the oscillator circuit. This crystal has excellent temperature and frequency characteristics in the automobile thermal environment; its frequency does not vary by more than 20 ppm in the temperature range considered. Crystal cost was minimized by selection of a crystal frequency of 2.23 MHz. Excellent oscillator stability and tuning range can be assured by proper selection of the values for R_1, C_1, and C_2.

Currently being considered are zener regulation of the oscillator section and voltage stresses affecting the aging process of the crystal. Fig. 7 shows a possible zener-regulation scheme for the oscillator circuit. The oscillator-amplifier voltage is regulated to 5.5 V by zener diode D_1 which can be integrated for possible additional voltage stability. The oscillator circuit and several counting stages could be operated at the 5.5 V zener level, and the following stages could be level shifted to the V_{DD} supply.

Clock system with LED display

Fig. 18 shows a block diagram of a digital-display automobile clock that uses light-emitting diodes (LED's) as

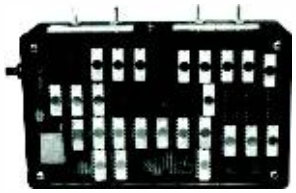


Fig. 9—Photograph of the LED clock.

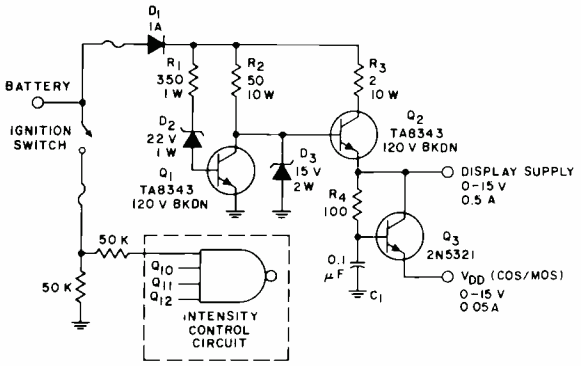


Fig. 10—LED (MAN-1) automobile clock power-supply regulator.

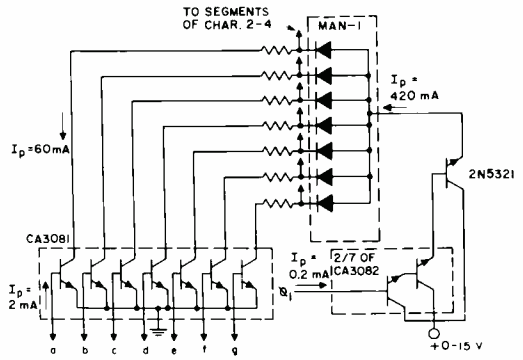


Fig. 11—LED (MAN-1) bipolar interface.

display devices. Fig. 9 shows a photograph of the prototype model.

Power-supply section

Fig. 10 shows the voltage-regulator section for the prototype LED clock. The cos/MOS and display-device supplies are unregulated when the auto supply voltage is in the range from 0 to 15 V. As with the Numitron clock, the cos/MOS supply can be unregulated because of the wide operating-voltage range of the cos/MOS devices. Further, the supply can be unregulated because the multiplexed LED display can tolerate fairly wide current variations. The regulator circuit for the LED display uses an inexpensive transistor Q_3 instead of the high-power zener diode D_3 shown in Fig. 3. When the input voltage is greater than 15 V, the LED and cos/MOS supplies clamp at approximately 15 V. When the auto supply voltage goes higher than 22 V, zener diode D_2 and transistor Q_1 conduct to turn *off* transistors Q_2 and Q_3. This scheme protects the LED displays and the cos /MOS devices from the +120-V transient. Diode D_1 protects the LED display, the cos/MOS devices, and the regulator from the −75-V transient and any accidental reverse bias of −18 V. When the display is *off*, the only power drain results from the cos/MOS oscillator and logic sections.

Logic-and-display driver section

RCA cos/MOS devices perform the following functions:

Oscillator-amplifier for the frequency reference,
Countdown chain which divides the oscillator frequency down to 1 cycle per minute,
Divide-by-60 counter with 7-segment decoders for the minutes display,
Divide-by-12 counter with 7-segment decoders for the hours display,
Multiplexer for the 7-segment output drivers,
Character and multiplexer decoder/driver,
Updating circuitry for the hours and minutes counters, and
Intensity control which regulates the LED brightness by means of an external panel potentiometer.

The multiplexing circuitry provides a 25% duty-factor *on* time for each LED character. The intensity-control circuit is identical to that described for the Numitron clock except for minor differences in external component values.

As with the Numitron clock, the LED clock is constructed from standard available cos/MOS devices; however, the cos/MOS logic could be realized from one or two custom cos/MOS MSI chips.

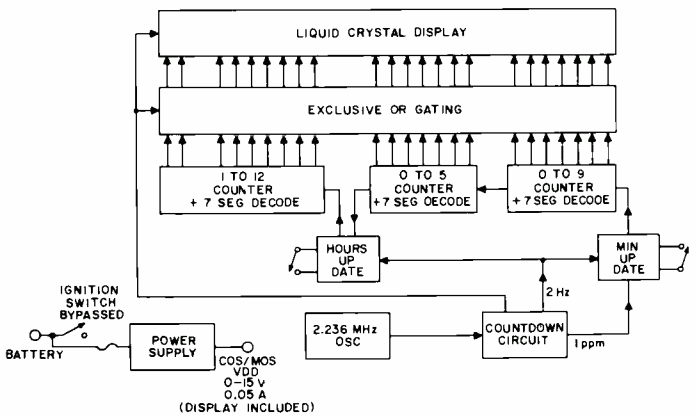
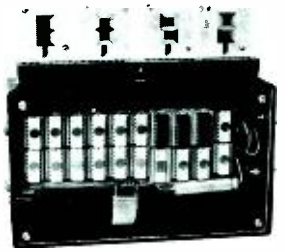


Fig. 12 (left)—Block diagram of liquid-crystal clock.

Fig. 13 (below)—Photograph of liquid-crystal clock.



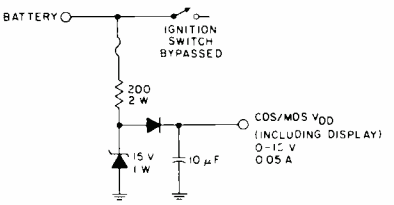


Fig. 14—Power-supply regulator for liquid-crystal clock.

The cos/MOS-to-display interface is accomplished by use of bipolar drivers, as shown in Fig. 11. As with the Numitron display, current levels are such that bipolar drivers are needed for the 7-segment outputs and the character drivers. The bipolar drivers reduce the current output requirements on the cos/MOS output driver devices. One RCA CA3081 integrated circuit, which includes 7-transistors, is used for the 7-segment driver, and two CA3082 bipolar integrated circuits plus four discrete transistors are used for the four bipolar character drivers.

Display section

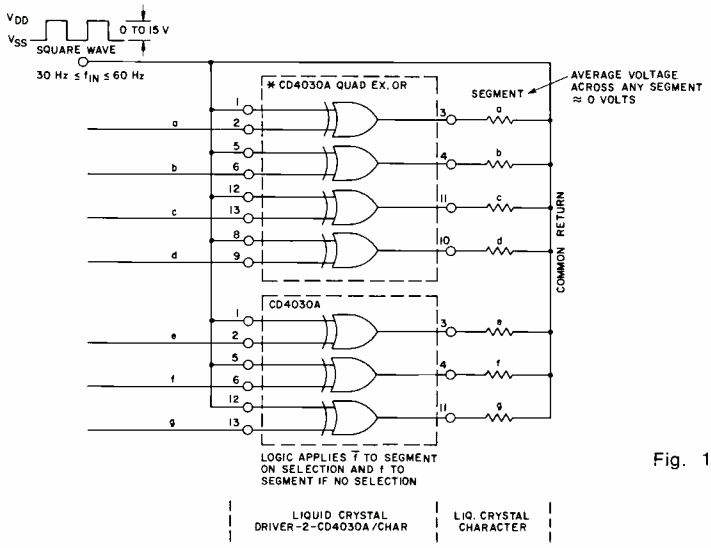
The Monsanto (diffused planer *GaAsP*) light-emitting diode display is one of the many LED types of displays considered. LED displays are easily multiplexed, reliable, and rugged; however, the cost and power drain of the LED's are possible deterrants to their use in automobile digital clocks.

The peak current through the LED display was designed to be 60 mA per segment for good brightness at a supply voltage of 12 V to the regulator. Because the supply voltage is normally somewhat higher than 12 V when the ignition switch is *on*, the LED supply voltage was designed to follow the input voltage. When the ignition switch is *off*, the base drive to the bipolar 7-segment drivers and the 4-character drivers are turned *off*. The display, therefore, is also turned off with a resultant saving of power.

Resistors were added in series with the LED segments to limit the peak current through each segment, provide uniform brightness between characters, and reduce the affects of temperature on LED brightness.

Frequency-standard section

The LED-clock oscillator is identical to that illustrated in Figs. 6 and 7 for the Numitron clock.



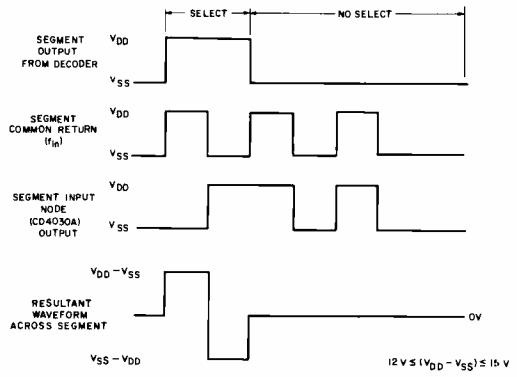


Fig. 15—COS/MOS driver circuitry and waveforms for a single digit.

Clock system with liquid-crystal displays

Fig. 12 a block diagram, and Fig. 13 a photograph of the prototype model for a digital-display clock that uses liquid-crystal displays.

Power-supply section

The power-supply regulator for the liquid-crystal clock is shown in Fig. 14. The cos/MOS V_{DD} supply is designed to follow the input voltage from 0 to 15 V. The cos/MOS V_{DD} supply clar .ps at approximately 15 V. The zener-diode and resistor ratings are designed to handle the +120-V and the −75-V transients. The supply input to the regulator can also be reversed to −18 V without damage to the cos/MOS devices. The regulator circuit for the liquid-crystal clock is very simple in comparison to the LED- and Numitron-clock regulators.

Logic-and-display-driver section

The RCA cos/MOS devices perform almost exactly the same functions in the liquid-crystal clock as they do in the Numitron clock; however, in the liquid-crystal clock, the intensity control is not used; the liquid-crystal segment drivers are different and smaller in device size; and the display is *on* full time. All the other functions are identical to the Numitron clock.

The cos/MOS-to-liquid-crystal-interface drivers for one of the four liquid crystal characters is shown in Fig. 15a. The first thing that stands out upon inspection of Fig. 15b is that no bipolar devices are required. The liquid-crystal segments are driven directly by thecos/MOS devices. When a segment is selected, an alternating low-frequency voltage of $\pm V_{DD}$ volts appears across the segment, as shown in 15b. When a segment is not selected, the voltage across the segment is zero.

Display section

RCA liquid crystals are an ideal match to RCA cos/MOS devices in automobile digital clocks because of their ultra-low-power dissipation and potentially low cost. However, the state-of-the-art, multiplexing capability, viewability, temperature limitations, and reliability are possible shortcomings at the present time.

The liquid-crystal display drivers follow the V_{DD} supply voltage. When the cos/MOS supply falls below 8 V, the liquid-crystal display turns *off*. Because liquid crystals consume negligible power, the only significant power dissipation in the liquid-crystal clock is in the oscillator-amplifier.

Frequency-standard section

The crystal-oscillator considerations for the liquid-crystal clock are the same as those for the Numitron and LED clocks, (shown in Fig. 6).

Performance evaluation

RCA cos/MOS integrated circuits feature low power dissipation, high noise immunity, and display-device interfacing capability, together with an easy adaptability to the automotive environment. Many automotive circuits, several of which are currently available, can be implemented by use of cos/MOS devices.

The three prototype models of automotive digital-display clock systems that used Numitron, light-emitting-diode, and liquid-crystal display devices were evaluated. The power-supply circuitry in each clock system is designed to protect the cos/MOS devices and the display devices from the severe voltage transients frequently encountered in automotive systems. Table I summarizes the performance of the three clock systems.

It is predicted that, in the future, the liquid-crystal clock will be the least costly of the three types. This prediction is based on the fact that the power-supply requirements for this type of clock are simpler and that, potentially, liquid crystals make possible a lower-cost display system, particularly if a practical multiplexing scheme can be implemented.

Table I—Performance summary for prototype models of digital-display automotive clock systems.

Clock type	*Numitron*	*LED*	*Liquid crystal*
Display off Power at 12 V	2.0 mA	2.0 mA	N.A.
Display on Power at 12 V	400 mA	250 mA	2.0 mA
Operating temperature range	−55°C to 125°C	−55°C to 100°C	+5°C to 55°C
Clock timing operating-voltage range	5 to 22 V	5 to 22 V	5 to 22 V
Clock time storage voltage minimum	3 V	3 V	3 V
Clock display operating-voltage range	5 to 22 V	7 to 22 V	8 to 22 V
Display brightness at 12 V	4000 ftL	400ftL (unmultiplexed)	—
Bipolar drivers	yes	yes	no
Bipolar regulator	yes	yes	no
Multiplexing	no	yes	no

Liquid crystals and COS/MOS offer minimal-power digital displays

R. C. Heuner

Liquid crystals driven by complementary-symmetry, metal-oxide-semiconductor integrated circuits offer the potential for low-cost, minimal-dissipation, digital display systems. An understanding of the capabilities and limitations of the liquid-crystal and COS/MOS technologies is necessary to successfully realize that potential. Interface requirements and drive circuitry, including implemented multiplexing techniques, are discussed; sample applications are outlined.

Table I—Typical single and 4-digit liquid-crystal display characteristics.

Characteristic	*Single-digit*	*4-digit*
Nominal dimensions (in.)		
Digit height	0.750	0.400
Digit width	0.450	0.600
Segment width	0.110	0.120
Electro-optical principal	Dynamic-scattering transmissive or reflective	
Operating temperature range	+5°C to +55°C	+5°C to +55°C
Equivalent circuit (segment)	Parallel R and C	
Segment resistance (megohms)	3	4
Segment capacitance (pF)	50	41
Response times (ms)		
Risetime	20	20
Decay time	50 to 100	50 to 100
Drive requirements	AC equivalent for good lifetime (sine wave, square wave, etc.) 50V RMS > V_{DD} > 12V RMS	
	30 Hz to 400 Hz	30 Hz to 400 Hz

THE MAJOR CHARACTERISTICS of assembled, single- and four-digit, seven-segment, liquid-crystal displays are summarized in Table I.[1,2] Note that for physically smaller displays, segment resistance can be raised from 3 megohms to over 100 megohms, while segment capacitance can be lowered from 50 pF to less than 5 pF.

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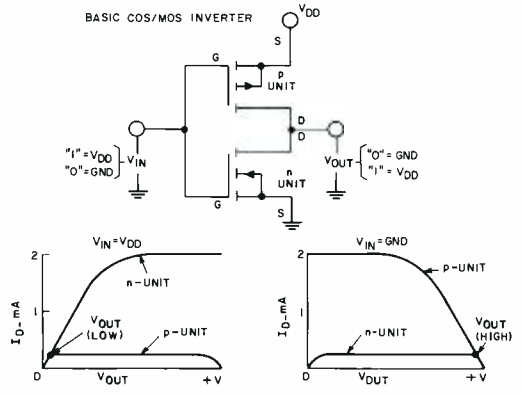

Fig. 1—COS/MOS inverter circuit and waveforms.

The basic COS/MOS inverter configuration is shown in Fig. 1. Table II indicates the major operating characteristics of the COS/MOS technology.[3,4]

Non-multiplexed displays

Fig. 2 illustrates the logic and associated waveforms for driving a single-digit, 7-segment display using two COS/MOS quad exclusive-OR gates, type CD4030A. Only a single, 12- to 15-V power supply is required. Segment line information *a* to *g*, equal to a fixed 1 on selection and 0 on no selection, acts as one input to each exclusive-OR gate. A square-wave input frequency (f_{in}) in the 30-Hz to 60-Hz range acts as the second input to each exclusive-OR-gate. In effect, this input converts the segment information at the exclusive-OR-gate outputs to a square-wave format out of phase with f_{in} on select and in phase with f_{in}

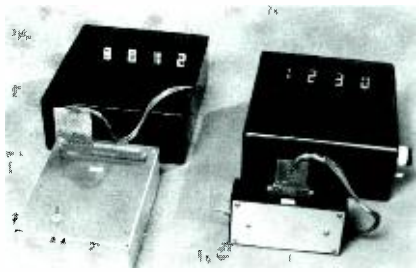

Photo shows examples of minimal-power digital displays Above, V-select to V/2 non-select (right) and V-select to V/3 non-select multiplexing schemes. Below, a digital clock using COC/MOS circuits and a liquid crystal display.

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received the BSEE from the City College of New York in 1959. He received the MSEE from Newark College of Engineering in 1967. Prior to coming to RCA, Mr. Heuner worked at International Telephone and Telegraph Laboratories on the logic design, debugging, and system testing of an electronic digital-switching center. He later worked in the circuits group on the design of discrete saturating and nonsaturating logic circuits, memory-driver circuits, drum and tape circuits, and other digital circuits. Mr. Heuner joined the RCA Defense Microelectronics Activity of DEP in 1964. He was responsible for the circuit design, analysis, and evaluation of a low-power family of bipolar monolithic logic circuits now in production at Electronic Components. Mr. Heuner became Group Leader of the Defense Microelectronics Integrated Digital Circuits and Subsystems Group in 1965. In this capacity, he was responsible for the design and development of new monolithic digital logic families intended for use by the DEP divisions of RCA. Mr. Heuner was made Group Leader of MOS Circuit Design and Applications in the Solid State Division of RCA in 1968. In this position he has had prime design and application responsibility for the CD4000A COS/MOS Logic/MSI/LSI line as well as for several custom COS/MOS integrated circuit products. In 1969, Mr. Heuner was co-receiver of the Solid State Division "Significant Achievement" award for engineering contributions to the design, application and manufacture of integrated circuits. Mr. Heuner has 15 patents issued or pending and is a member of the IEEE.

Table II—Typical COS/MOS logic characteristics.

Characteristic	*Value*
Operating voltage range	3 to 15V
Operating temperature range	−55°C to +125°C
Logic capability	Gate/flip flop/MSI building block to complex LSI functions
Speed range	DC up to 10 MHz
Quiescient dissipation	Less than 10 μW
Drive capability	Sink or source up to 10 mA depending on allowed 1- or 0-level deviation.
Input impedance	10^{12} ohms
Output impedance	Design range: 100 ohms to > 10 kilohms for both 1 and 0 states
Noise immunity	30% of V_{DD}

on no select. Input frequency f_{in} is now applied to the common return of the liquid-crystal display, while the exclusive-OR-gate outputs are applied to corresponding liquid-crystal segments as shown. As a result, a $\pm V_{DD}$, peak-to-peak square wave is impressed across the selected segments, and zero volts is impressed across the non-selected segments. The average voltage across any segment is zero. Note that the select time of the characters is synchronized with f_{in}, and would actually last much longer than one cycle of f_{in} as shown.

Fig. 3 illustrates the logic for the display section of an hours/minutes/seconds digital clock using a COS/MOS single-digit-BCD-to-7-segment decoder/liquid-crystal driver, CD4055A. Provision is made on the COS/MOS unit to permit separate logic- and display-supply values to be utilized. For example, logic- and display-supply values of 5 V and 15 V, respectively, are shown. Logic- and display-supply lines may also be tied together and driven from a single supply. The effective drive characteristics across the display are equivalent to the exclusive-OR-gate drive illustrated in Fig. 2.

Fig. 4 illustrates the logic for the display section of a 3-½ digit meter using a COS/MOS single-digit-BCD to 7-segment decoder/liquid-crystal driver with strobed latch, CD4056A, as well as a 4-line liquid-crystal driver with strobed latch, CD4054A. Again, separate logic- and display-supply values may be utilized.

Multiplexed displays

The basic RC equivalent circuit of the liquid-crystal segment provides no built-in isolation diode, such as is the case with light-emitting-diode displays. Therefore, conventional multiplexing schemes cannot be utilized. In addition, the AC, equivalent-drive requirement of liquid-crystal displays rules out provision of simple diode isolation.

Figs. 5, 6 and 7 illustrate three implemented multiplexing schemes using COS/MOS logic-driver circuitry and liquid-crystal displays. Fig. 5 shows a two-frequency V-select to $V/2$-non-select scheme. Only a single power supply is required; V_{DD} is 15 V. Frequency f_1, at 64 Hz, is well below the frequency response limit of the liquid crystal. Frequency f_2, at 4096 Hz, is well above the frequency response limit of the liquid crystal, and is an even multiple of f_1. As shown in Fig. 5, an f_1 of 64 Hz and an f_2 of 4096 Hz are

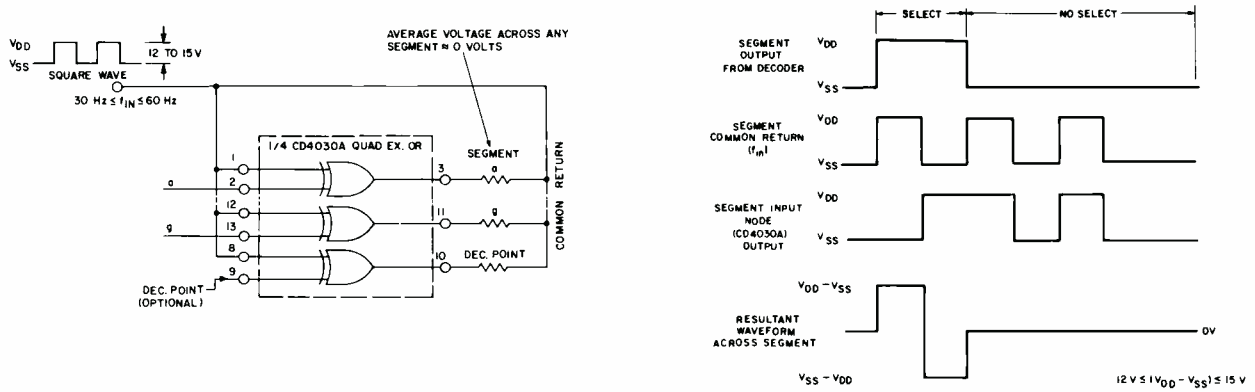

Fig. 2—Single-digit exclusive-OR drive circuitry and waveforms.

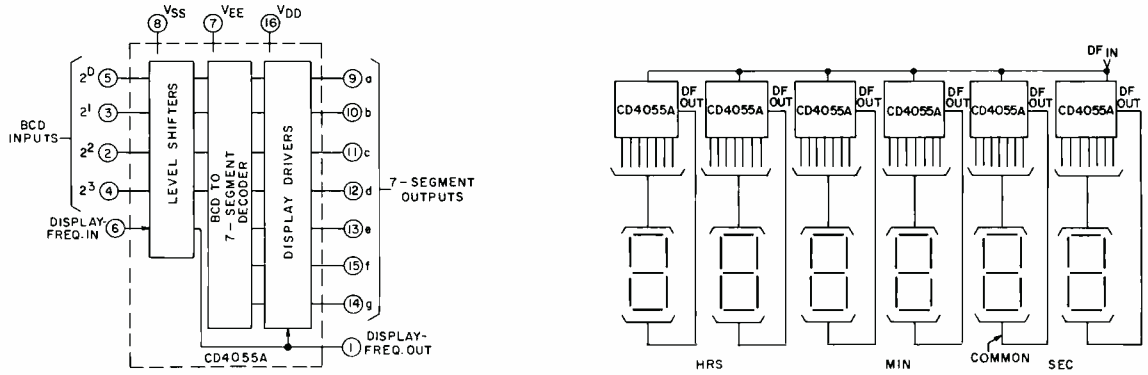

Fig. 3—Single-digit BCD-to-7-segment decoder/liquid-crystal driver (CD4055A) used for hours/minutes/seconds display. V_{DD}=0V, V_{SS}=−5V, V_{EE}=−15V, DF_{IN}=30Hz.

applied to the character lines (rows) at character select and non-select respectively. For example, during selection of character 1 ($\phi_1=1$), 64 Hz is applied to character one (row 1), while 4096 Hz is applied to characters 2, 3, and 4 (rows 2,3,4). Simultaneously the *a* to *g* segment lines (columns) are gated via exclusive-OR gates with the 64-Hz signal. The resultant liquid-crystal segment voltages, as shown in Fig. 5, are ± 15 V on character select-segment select, O V on character select-segment non-select, and + 15 V to 0 V at 4096 Hz to 0 V to −15 V at 4096 Hz on character non-select-segment select or non-select. Since the liquid-crystal segments cannot respond to the 4096-Hz signal, the scattering voltage across the liquid crystal during character non-select becomes the effective average of the 4096-Hz signal, or + 7.5 V and then −7.5 V for two half-cycles of the 64-Hz wave, as shown. Thus, full selection is $\pm V_{DD}$ (± 15 V), while half or no selection is either $\pm V_{DD}/2$ (± 7.5 V) or zero volts. Note that for all conditions the average voltage over a 64-Hz cycle is zero volts. Hence, to extinguish the unselected segments, the threshold voltage for significant scattering must be maintained above $\pm V_{DD}/2$. In addition, to adequately turn *on* the segments on selection, the ϕ_1 character-select time must be equal to, or greater than, the crystal turn-on time (delay + rise time). A comparatively long crystal-decay time will aid in holding the character-1 display *on* during ϕ_2, ϕ_3, and ϕ_4 times. A long decay time will, however, also slow the response to new segment information. To avoid flicker-effect to the eye, each character select must be repeated at a rate above 25 Hz. Although subjective, the 16-Hz rate utilized results in a small but acceptable degree of flicker. Present limitations of crystal on time combined with flicker-effect limit the two-frequency *V*-select to *V*/2 non-select scheme to four characters. In addition, unit-to-unit variation as well as roundness in contrast-ratio versus drive-voltage characteristics restrict overall supply range and variation. For the four-character multiplex-unit fabricated, a supply range of 12 to 15 V appeared satisfactory.

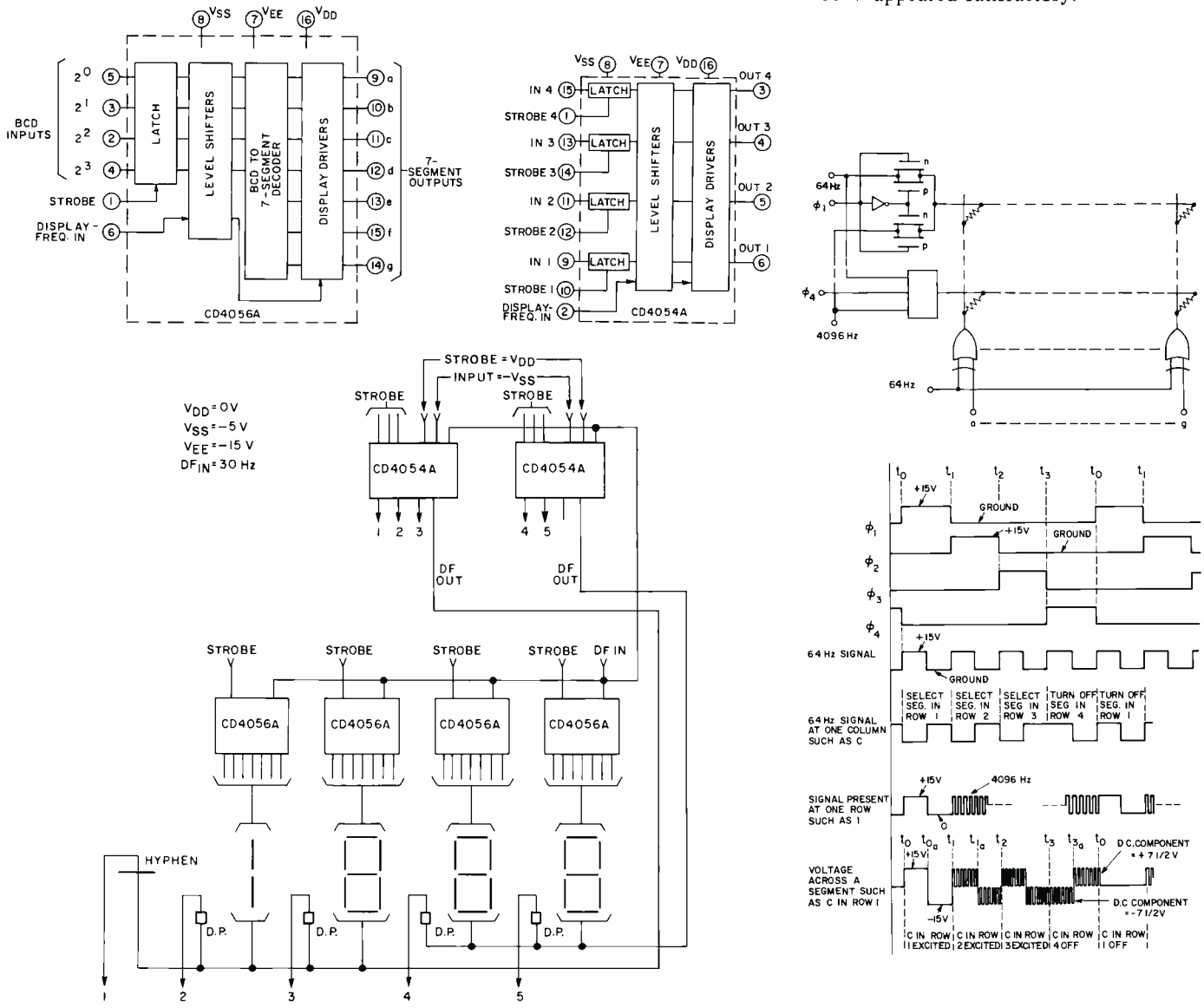

Fig. 4—Single-digit BCD-to-7-segment decoder/liquid-crystal driver with strobed latch (CD4056A) and 4-line liquid-crystal driver with strobed latch (CD4054A) used in a 3½-digit meter display.

Fig. 5—Two-frequency V-select to V/2-select multiplex scheme and waveforms.

Fig. 6 shows a shaped two-frequency V-select to $V/3$ non-select scheme. Only a single power supply is required; V_{DD} is 15 V. Again, f_1 is below and f_2 is above the frequency response of the liquid-crystal material. In this case, however, the 4096-Hz signal is shaped to a 33% duty cycle, and is gated to both the character (rows) and segment (columns) lines; the shaping provides a ration of $\pm V_{DD}/3$ in all non-selected conditions. The improvement to a V select to $V/3$ non-select ratio offers several advantages: *on*-to-*off* contrast ratio is improved, supply tolerance and unit-to-unit variations and provides a ratio of $\pm V_{DD}/3$ in all non-drive voltage are not critical, and drive voltage can be increased, thus reducing rise time and making expansion to eight characters possible. Some increase in logic complexity is required to realize the shaped 4096-Hz signals, as shown in Fig. 6.

Fig. 7 shows a dual-supply V-select to $V/2$ non-select scheme. Only a single low-frequency drive signal is required. One disadvantage, however, is the requirement for two power supplies. As in the two-frequency V-select to $V/2$ non-select scheme, constraints of crystal *on* and *off* time and flicker-rate limit the multiplexing to four-character sets. Similarly, unit-to-unit variation and rounding in contrast ratio versus drive voltage restrict the supply range.

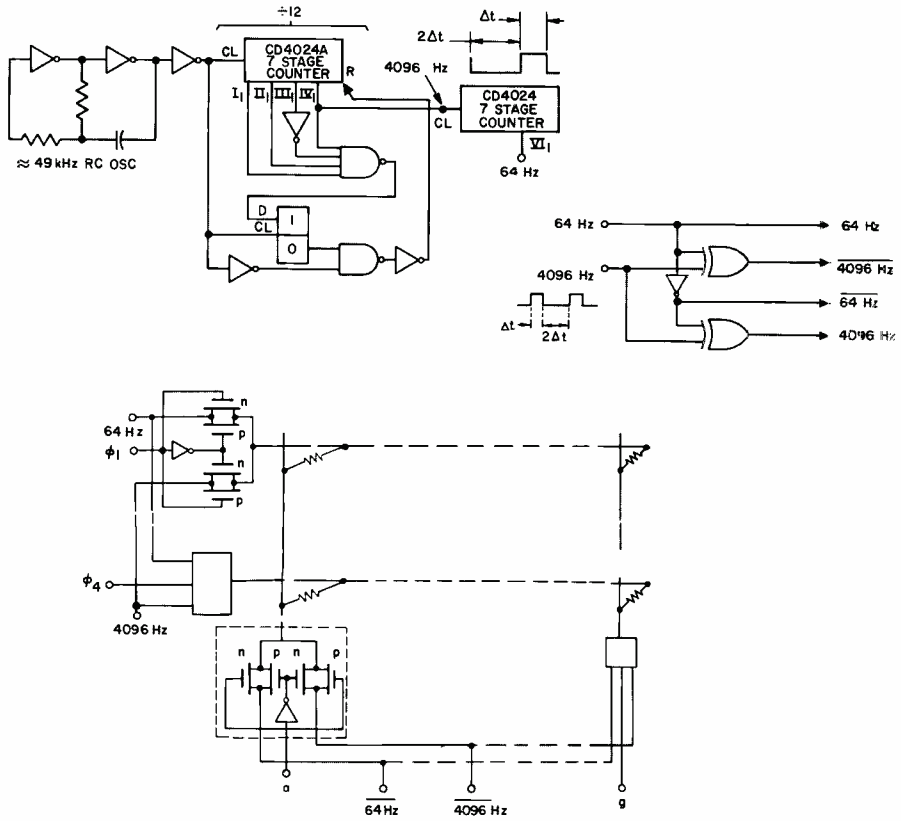

Fig. 6—Shaped two-frequency V-select to V/3 non-select multiplex scheme using COS/MOS logic-driver/liquid-crystal displays.

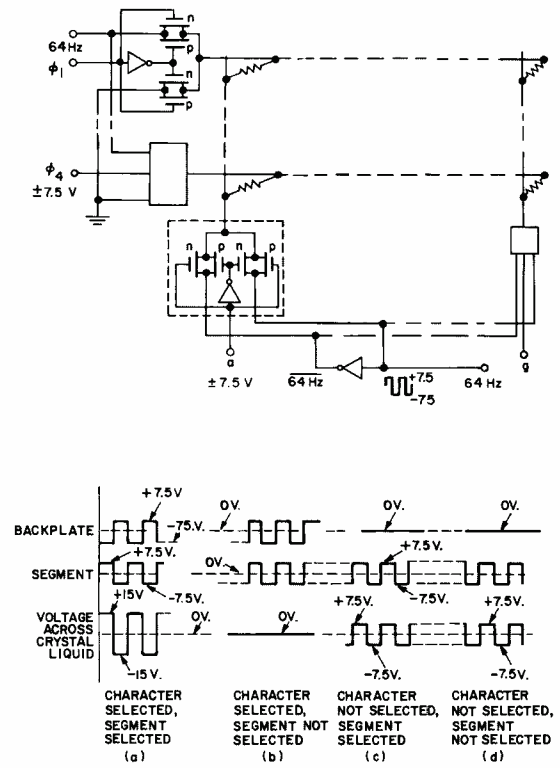

Fig. 7—Dual-supply V-select to V/2 non-select multiplex scheme using COS/MOS logic-drivers/liquid-crystal displays, and waveforms.

Future work

Quantitative measurements of frequency response, delay, rise and decay times, and contrast ratio versus drive voltage are being taken for existing liquid-crystal displays in an effort to more exactly define optimum operating conditions of the multiplexing schemes outlined. Implementation of COS/MOS two-frequency approaches utilizing different signal amplitudes is under investigation. Performance criteria, such as power dissipation, voltage range, etc., are benig evaluated in the various multiplexing schemes.

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2. RCA Liquid-Crystal Data Sheets: TA8032, TA8034—Single-Digit 7-Segment Types; LC-7001R, LC 7001T, LC7002R, LC7002T—Four Digit, 7-Segment Tyes, 1972.
3. RCA Solid State Databook "COS/MOS Digital Integrated Circuits," SSD-203A (1973).
4. RCA COS/MOS Integrated Circuits Manual. Technical Series CMS-271, 1972.

Keeping up with the times through computer-aided design

J. Litus, Jr.

Computer-aided design allows quick realization of new designs and produces efficient and error-free designs at low cost. This paper discusses computer-aided design—specifically artwork generation, simulation, and testing—as presently practiced in the Solid State Division in the design of COS/MOS integrated circuits.

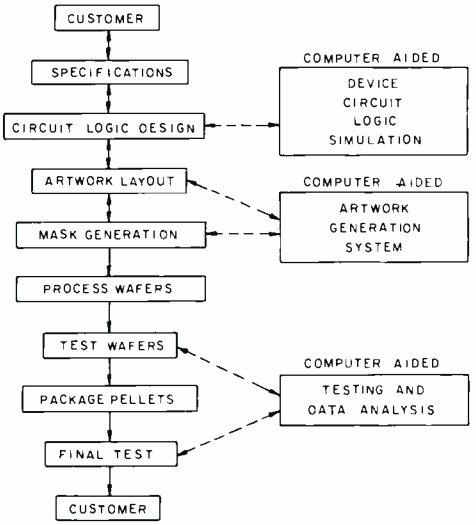

Fig. 1—Steps in the design of a COS/MOS integrated circuit.

COMPUTER-AIDED DESIGN comprises several processes: simulation, artwork generation, testing, and data analysis. *Artwork generation* is the term applied to the process of preparing masks or templates that are used in the manufacturing process to define the physical shapes of the elements and their interconnections. *Simulation* can be defined as the reproduction of certain aspects of the behavior of a system by means of some auxiliary system. *Testing*, which has become a major challenge with the advent of LSI, determines the ability of a circuit to meet its design requirements through the analysis of data gathered while the circuit is in operation.

The flow chart of Fig. 1 describes the steps necessary to design a COS/MOS integrated circuit. As depicted, computer-aided design helps the engineer predict the performance of his proposed design, provides detailed patterns for the manufacture of the design, and verifies the success of the design and processing steps.

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Artwork

The artwork defines the geometrical patterns necessary to implement the circuit elements (transistors, diodes, resistors, capacitors, etc.) and their interconnections so that the desired circuit function is attained. Historically, the major steps in the artwork-generation process have been as shown in Fig. 2. A composite layout would be generated manually by an engineer-

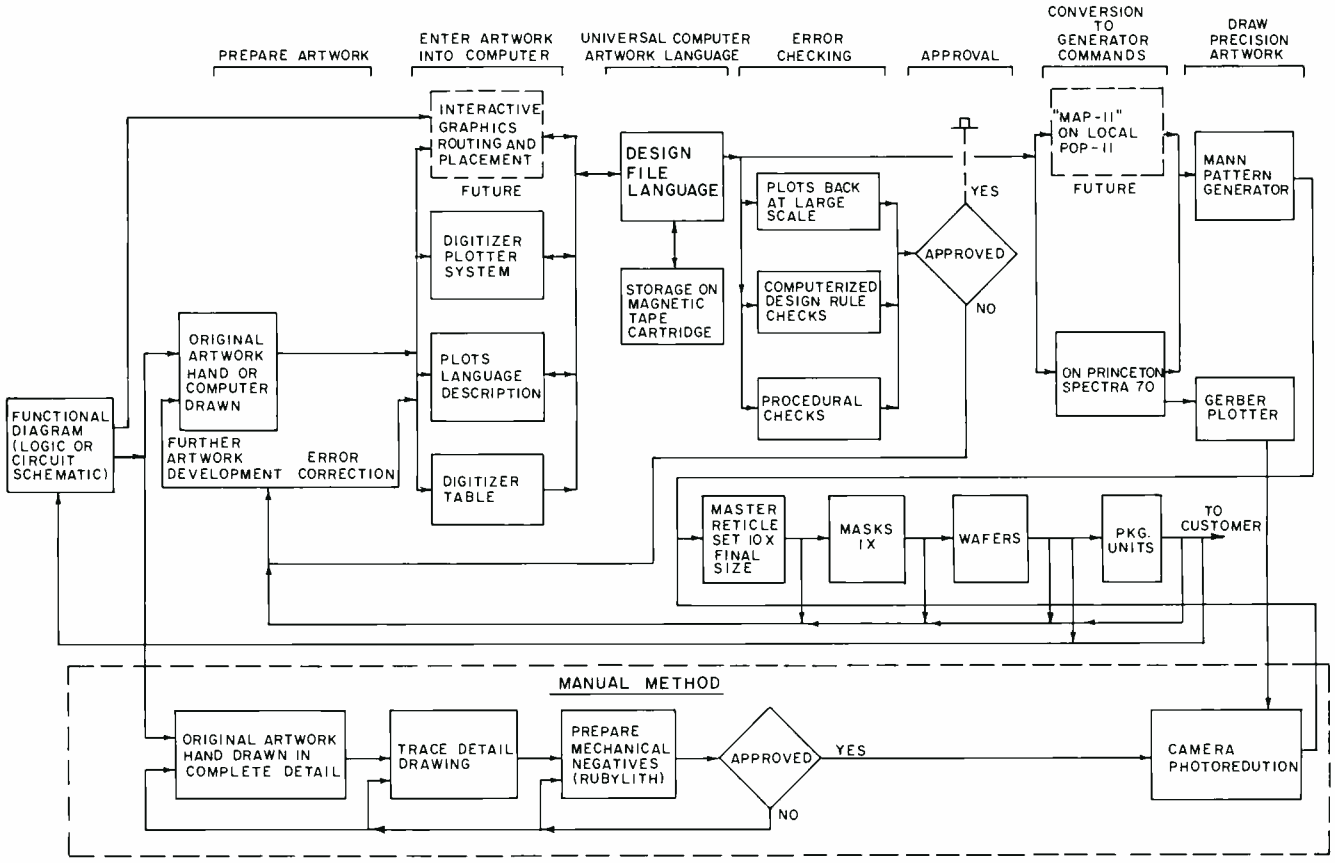


Fig. 3—Improved computer-aided artwork-generation system presently in use.

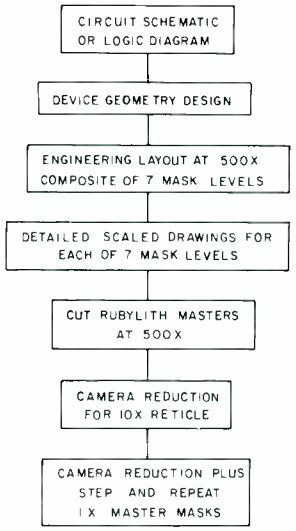


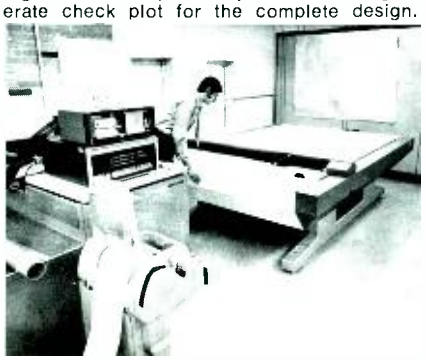
Fig. 2—Historical artwork-generation process.

draftsman team. The composite is a scale drawing at 500X of the final mask set using different colors to denote the mask levels. From the composite, a set of detailed drawings was made, one for each mask level. These drawings were used as a guide by the technician who cut the shapes out on Rubylith and removed the excess, leaving the desired opaque sections. The Rubylith masters at 500X were camera reduced to the final masks from which the circuits were made. Overall, the procedure was very slow and error prone, resisted changes, and had accuracy limitations.

The improved computer-aided artwork-generation system used presently is shown in Fig. 3. The digitizer/plotter shown in Fig. 4 is the workhorse of the artwork system. The plotter uses an interactive digitizing approach to capture composite layout information and generate a computer file containing all of the necessary data to create a set of masks. The digitizer/plotter system (DPS) is controlled by a mini-computer, and has the necessary I/O equipment to create, modify, error check, and plot designs. The hardware consists of a mini-computer, disk storage, digitizer/plotter, joystick control, teletype, cassette-tape unit, push-button box, storage-tube display, and coordinate display module. The digitizer/plotter system provides the user with meaningful feedback. Because of its flexibility it can be used extensively with a library of standard cells to modularize the layout and build on previous design efforts. Standard cells can range from very simple patterns to a complete design. The cells offer the layout equivalent of functional building blocks, thus shortening layout times and reducing errors. Additionally the use of standard cells permits the designer to predict the performance of his design. A large flatbed plotter system, shown in Fig. 5, is used to generate check plots for the complete layout.

Fig. 4—Digitizer/plotter system.

Fig. 5—Flatbed plotter system used to generate check plot for the complete design.



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received the BSEE from Newark College of Engineering in 1965 and the MSEE from the University of Pennsylvania in 1969. Mr. Litus joined RCA in 1965 on the Design and Development Training Program. Upon completion of this program he joined the Digital Integrated Circuits Group of Defense Microelectronics, Somerville, New Jersey. In this position he contributed to the design and development of high-speed, digital, integrated, emitter-coupled, logic circuits and arrays including automatic artwork generation. In 1968 Mr. Litus joined the MOS Integrated Circuits Activity of the Solid State Division. In this capacity he was responsible for logic and circuit design, evaluation, testing, and applications of many standard and custom COS/MOS integrated circuits. In early 1972, Mr. Litus was appointed to his present position.

Standard-cell arrays

The standard-cell array concept for

Table I—COS/MOS standard cells.

No.	*Description*
Q00	Main alignment key
Q01	Metal, special metal, n^+ and protective alignment key
Q02	Metal, special metal, silicon-gate, p^+ and protective alignment key
Q03	p^+, n^+ and contact alignment key
Q04	p^+ and stepped-oxide alignment key
Q05	Beam-lead alignment key
Q06	Reserved alignment key
Q07	#1 Bond pad with semicircular end
Q08	Standard (4 x 4 mils) bond pad
Q09 to Q39	Reticle alignment key, border key and other alignment keys
Q40	Input protective resistor with provision for 1-line crossover
Q41	Input protective resistor with provision for 2-line crossover
Q42	Input protective resistor with provision for 3-line crossover
Q50	p^- (p-well)/n^+ diode with large contact
Q51	p^- (p-well)/n^+ diode with small contact
Q52	p^+/n^- (n-substrate) diode with large contact
Q53	p^+/n^- (n-substrate) diode with small contact
Q54	p^+/n^- zener diode
Q55	p^+/n^+ zener diode
Q60	1-line p^+ tunnel
Q61	2-line p^+ tunnel
Q62	3-line p^+ tunnel
Q63	4-line p^+ tunnel
Q64	5-line p^+ tunnel
Q70	1-line n^+ tunnel
Q71	2-line n^+ tunnel
Q72	3-line n^+ tunnel
Q73	4-line n^+ tunnel
Q74	5-line n^+ tunnel
Q75	6-line n^+ tunnel
Q76	7-line n^+ tunnel
Q77	8-line n^+ tunnel
Q78	9-line n^+ tunnel
Q70	10-line n^+ tunnel
Q80	n-channel transistor (minimum size)
Q81	n-channel transistor (size #2)
Q82	n-channel transistor (size #3)
Q83	n-channel transistor (size #4)
Q90	p-channel transistor (minimum size)
Q91	p-channel transistor (size #2)
Q92	p-channel transistor (size #3)
Q93	p-channel transistor (size #4)
Q100	Inverter (minimum size)
Q101	Inverter (size #2)
Q102	Inverter (size #3)
Q103	Double inverter
Q110	2-input NAND gate
Q111	3-input NAND gate
Q112	4-input NAND gate
Q113	8-input NAND gate
Q120	2-input NOR gate
Q121	3-input NOR gate
Q122	4-input NOR gate
Q123	8-input NOR gate
Q130	R-S flip-flop using NAND gates
Q131	R-S flip-flop using NOR gates
Q132	Binary counter stage (T flip-flop) without set & reset
Q133	Binary counter stage (T flip-flop) with reset
Q134	D flip-flop without set or reset
Q135	D flip-flop with reset
Q136	D flip-flop with set and reset
Q137	Front end of J-K flip-flop
Q150	Basic transmission gate
Q151	Analog switch
Q152	High sink-current driver
Q153	2-to-1 multiplexer
Q154	3-to-1 multiplexer
Q155	Exclusive-OR gate
Q156	AND-NOR gate
Q157	OR-NAND gate
Q158	Functional gate ($D=A+BC$)

producing LSI arrays begins with the definition, design, and layout of a group of custom circuits called "standard cells." These cells are given an identification number and permanently stored for future use. To obtain one of these cells for use in a logic design, the user calls for the desired cell by pattern number. The stored data of a standard cell is a collection of polygons on each of the seven mask levels; the polygons represent the layout of the circuit elements and the interconnections required to have the elements perform the desired function.

The standard-cell library is an open-ended collection of logic circuits; the definition and design of new cells to meet future requirements is possible. The present family of standard cells, listed in Table I, consists of more than 100 cells; this family is growing daily. In addition to logic circuits the family includes alignment keys, bond pads, borders, input-protection circuits, diodes, resistors, tunnels, and transistors. The numbers allow the cells to be retrieved from memory.

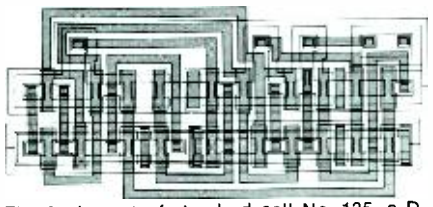


Fig. 6—Layout of standard cell No. 135, a D flip-flop with reset.

The standard-cell library approach can be viewed as a cross between the fully automatic approach, in which the computer implements everything including placement of devices and routing of interconnections, and the conventional approach, in which most of the work is done manually. The fully automatic approach, while fast, yields a very inefficient chip layout, a layout not preferred for high-volume production. The inefficient layout results from formal layout rules (such as fixed cell height, fixed input/output locations, all cells aligned in rows), structured interconnect schemes (such as north-south metal runs, east-west tunnels), and limitations of layout programs.

In the standard-cell approach utilized in the COS/MOS engineering activity, each cell is laid out in the minimum area possible for the function to be implemented. No restriction is placed on cell height or width or on the location of inputs and outputs. The placement of the cells is performed by an engineer-draftsman team. The result is an efficient layout at minimum cost. Cell No. 135, a D-type flip-flop with reset, is an example of one of the cells in the standard-cell library. The layout of this cell is shown in Fig. 6. A data sheet (Fig. 7) provides the system and logic designers with the design information for the cell: circuit configuration, logic symbol, boolean equation, truth table, cell number, and various parameters (e.g., capacitance, delays, transition times, and power) applicable to the cell.

All standard cells are available for standard-line COS/MOS products—3 to 15 volts, CD4000A Series. The same functions are also available in silicon-gate versions.

A typical logic diagram is shown in Fig. 8; the numbers on the logic sym-

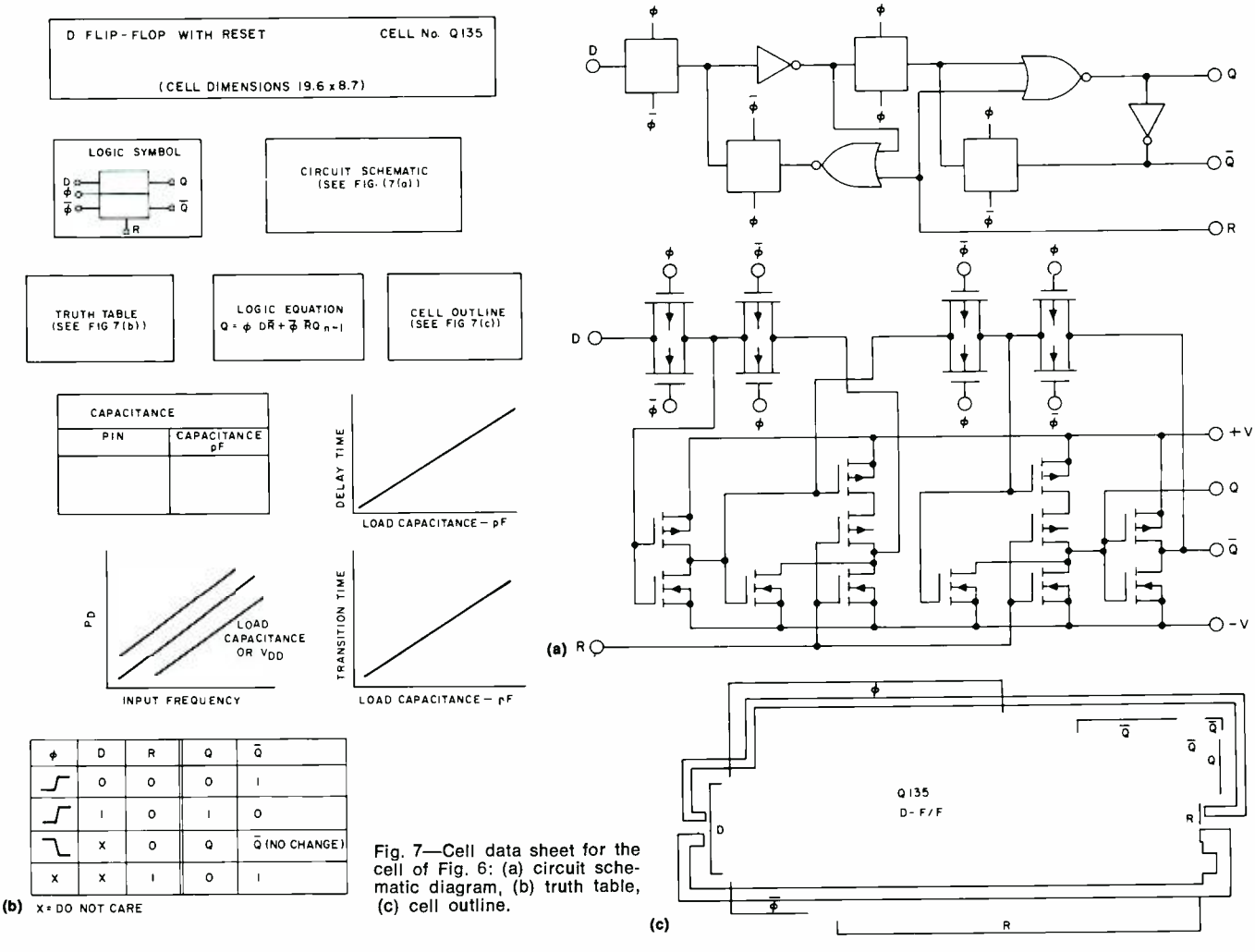


Fig. 7—Cell data sheet for the cell of Fig. 6: (a) circuit schematic diagram, (b) truth table, (c) cell outline.

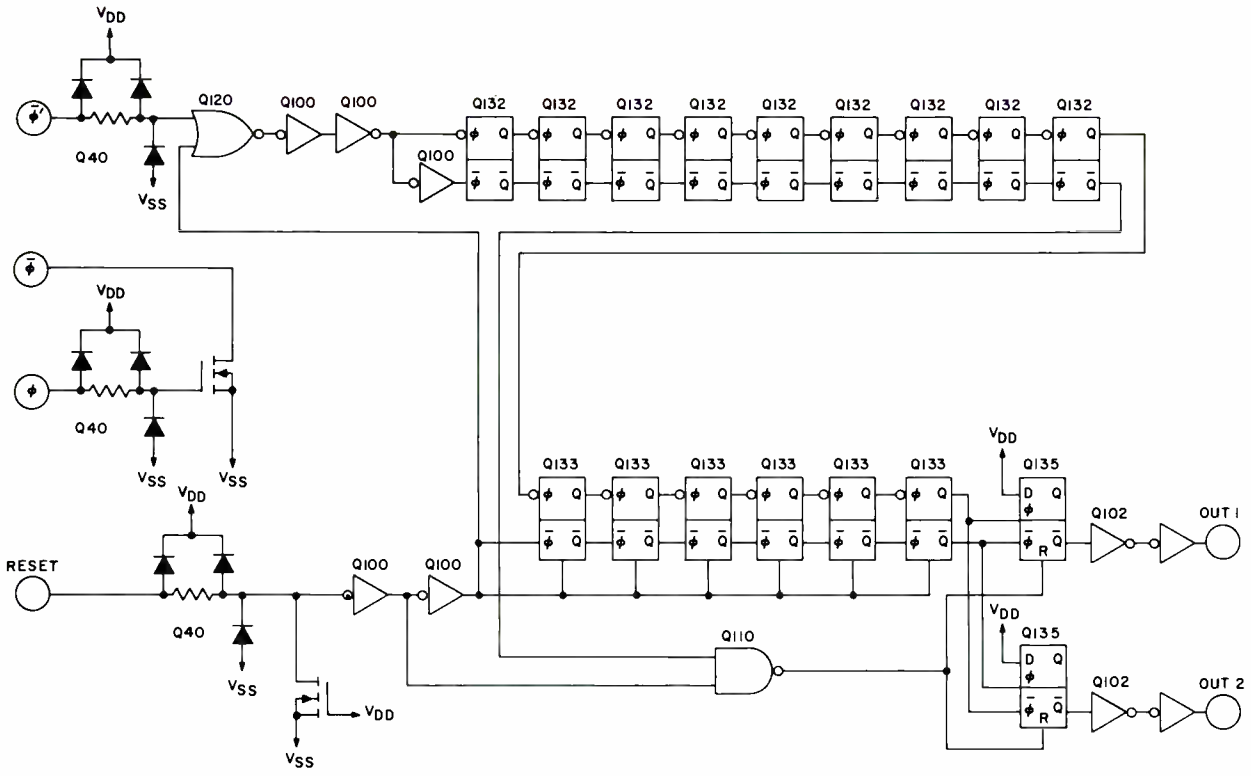


Fig. 8—Typical logic diagram.

bols represent the standard cells capable of performing the function required. The diagram shown is the input for the artwork generation stage. An engineer-draftsman team lays out the circuit using the composite layout of standard cells. The cells are placed and then interconnected to perform the desired function as described by the logic diagram.

Fig. 9 shows the 500X layout for the circuit of Fig. 8. There is no need to hand draw the internal parts of a cell as this information is stored in the computer library; only the interconnections from the cell boundaries need be made. The layout of Fig. 9 is used as input information for the digitizer/plotter system. The cell placement and rotation is entered on the teletype. The explicit information is digitized and placed in the file with the Q-calls.

The polygons are digitized by tracing the figure, using a "joystick" control and cursor; the coordinates of the tracing are stored by the digitizer. The shape of the polygon is then plotted out for verification or modification. If the read-out shows that the information in storage is correct, the cell is made part of the library.

When digitizing is complete, the resultant information is stored on magnetic tape. The tape is then used to generate a check plot of the entire circuit at 500X or any other desired scale. The checkplots consist of a composite drawing (Fig. 10) and detailed plots of various levels of the circuit. The finished layout is checked for accuracy manually and by computer. The computer automatically checks design rules, such as metal width and spacing on all COS/MOS circuits; this is an extremely difficult task to do by hand. Additions to the automatic design rule checks are presently taking place so that eventually manual checks will be minimized.

After the checkplots have been approved, the information stored on magnetic tape is converted to a format (Mann Artwork Program) acceptable to the Mann Pattern Generator, a computer-controlled light source that transfers the necessary patterns or polygons for each of the circuit levels onto a photosensitive glass plate, to make the 10X reticles. The 10X reticles are then reduced to 1X and transferred onto a glass plate by a step-and-repeat process to form a 2x2-inch array; this plate becomes the master mask for one of the seven circuit levels. Prints made of these masks or levels are used to locate the desired

Fig. 9—Composite layout of the circuit of Fig. 8 at 500X.

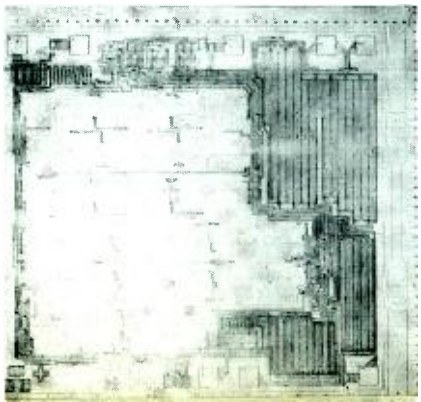


Fig. 10—Composite check plot (500X) reticle, and mask.

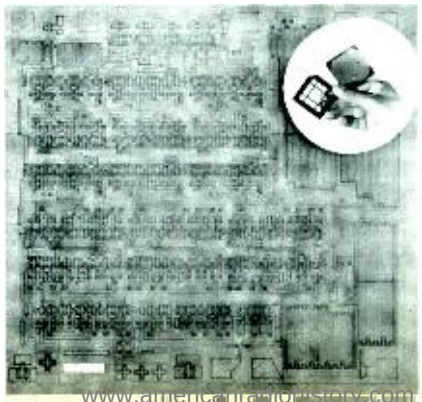
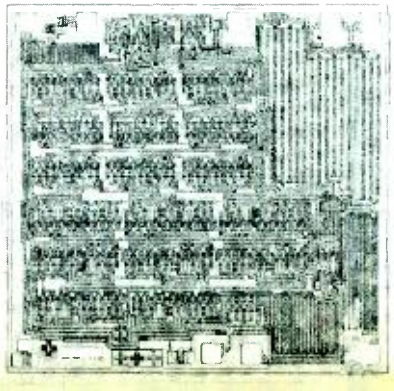


Fig. 11—Photomicrograph of finished chip.



patterns on the wafer so that processing can be accomplished in selected areas only. A photograph of a finished pellet is shown in Fig. 11.

Cell characterization

A COS/MOS standard-cell test array is fabricated so that performance data can be measured directly. In this way, the cells can be completely characterized in terms of on-chip parameters. This test vehicle also provides data useful in verifying the accuracy of the computer circuit-simulation technique of cell characterization. The test array contains at least one circuit type out of each of the basic groups of standard-cell circuits.

The logic content of the test chip is shown in Fig. 12. Each circuit type used is identified by cell number so that reference can be made to the data sheets. The test chip can be utilized to obtain DC as well as transient response information. The on-chip delay characteristics of the various cells are measured and the results compared with the cell data provided by the circuit simulation. The comparison of actual with calculated data establishes the accuracy of the automatic simulation technique. Thus, it is possible to characterize the other cells without having to construct additional test chips.

Since all new designs are not necessarily high-volume types, and quick turn around is necessary, the all computer approach to cell placement and routing enhances the COS/MOS engineering capability.

Simulation

It is often easier, cheaper, and quicker to test design modifications through simulation than to make physical changes to the actual system under study.

At the present time, the RCA Circuit Analysis Program (RCAP) available on the Basic Time Sharing System (BTSS) is used to aid design of COS/MOS circuits. This program is capable of analyzing circuits containing up to 30 nodes and either MOS or bipolar transistors; it is designed to compute both the DC operating point and transient response of bipolar and MOS transistor circuits.

A computer printout of a transient analysis run on BTSS for a two-input NOR gate is shown in Fig. 13. The

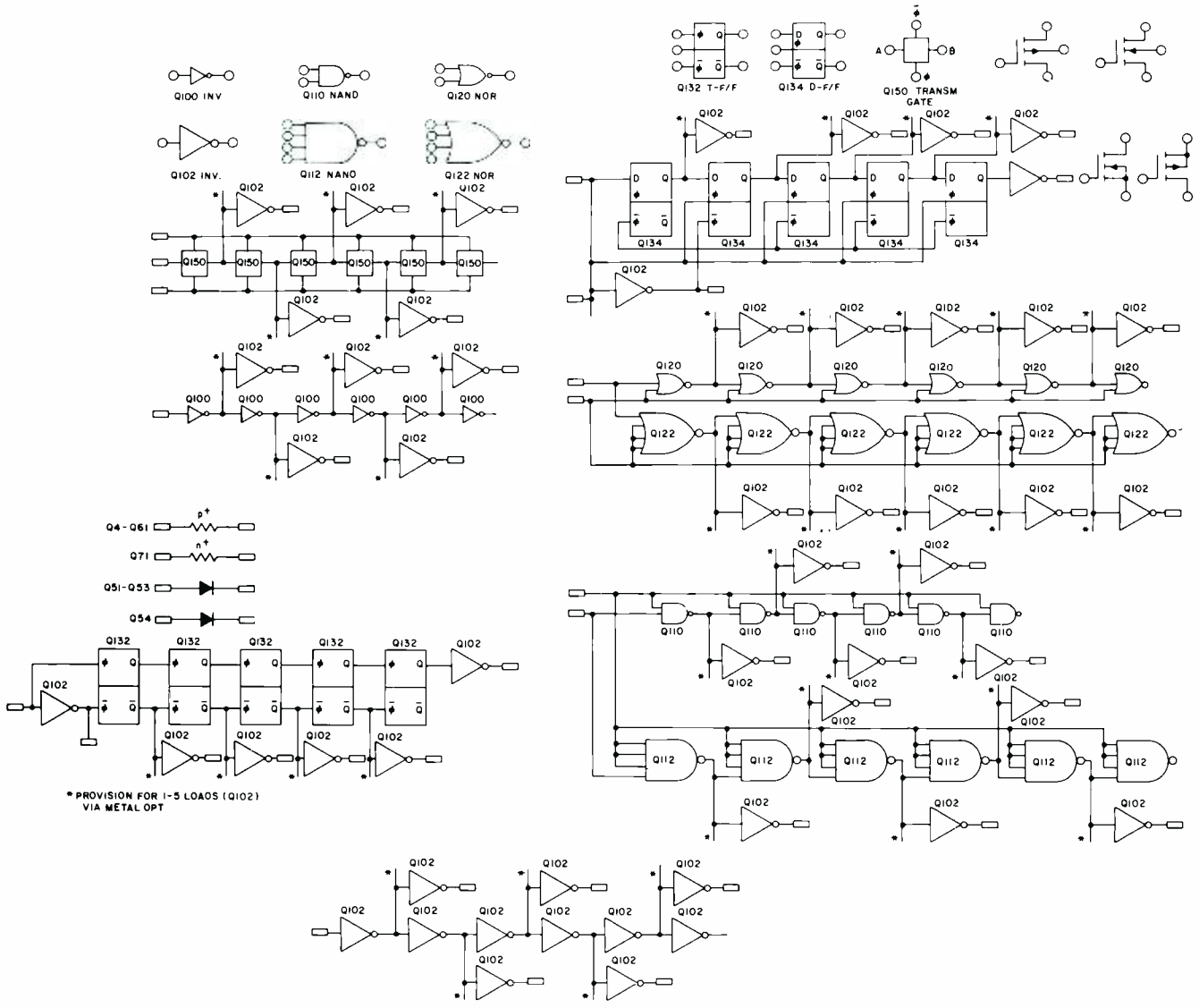
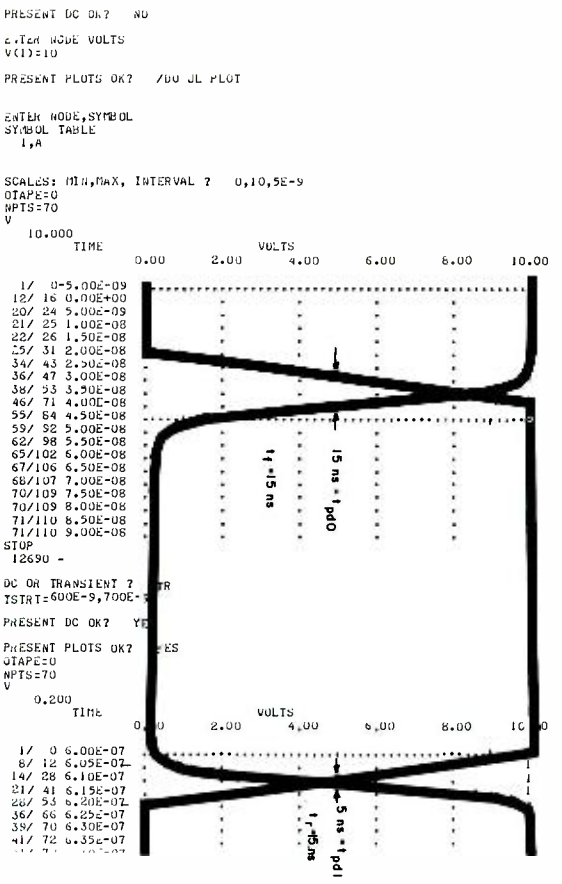


Fig. 12—Logic diagram of standard-cell test chip.



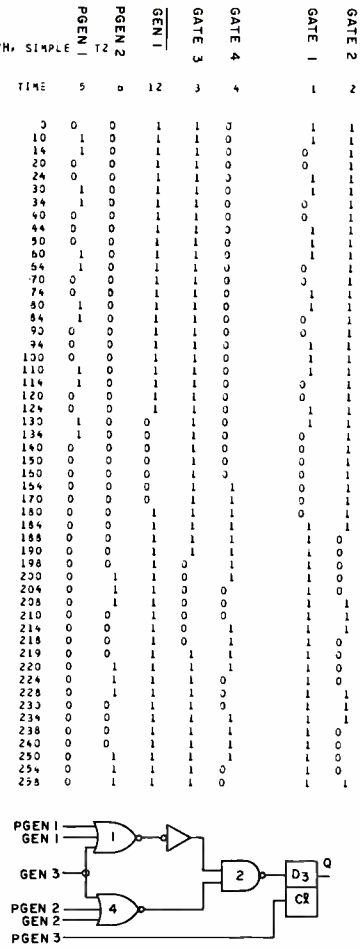


Fig. 13 (above)—Output of RCAP.
Fig. 14 (right)—Output of LOG/SIM.

input to the program consists of a description of the circuit components and their interconnections and supply voltages; some pertinent chip and device parameters are also input. On the basis of the description of the input signals, a plot can be obtained of output voltages (all dependent nodes) as a function of time.

Because a change of any parameter can be input and another run made as necessary, the designer is offered far more flexibility in parameter selection and instantaneous feedback with the simulation system than he is with the more traditional, breadboard approach. However, when using the simulation system, chip and device parameters used for inputs must be known along with any variations that may occur in the values of these parameters.

A second area of simulation is that of logic simulation. A logic-simulation program, LOG/SIM is available in the batch mode on the Spectra-70 Computer at RCA Laboratories. A logic interconnection list is input to the computer along with the corresponding delay of each element. The system is stimulated with input waveforms and a printout of selected output levels as a function of time is obtained; Fig. 14 shows the output of LOG/SIM. Hazards, races, or spike conditions are pointed out in the printout. It is possible with LOG/SIM to analyze or try various logic configurations at minimum cost. Such simulation might also lead to the discovery of unwanted conditions that could remain undetected with the use of the more traditional breadboard approach in which typical off-the-shelf units are used. With LOG/SIM, the user has complete control over the selection of the delay values of the logic elements; this degree of selectivity is not possible when breadboarding. This selectivity may aid in providing more accurate data in worst-case design where breadboarding provides only a typical analysis at best. Both systems are employed where necessary to obtain the most effective results.

Testing and data analysis

At present, computer-controlled test systems are being used to test all COS/MOS products at the wafer-probe and final-test stages. By thorough testing of finished products, a large amout of information can be obtained that could lead to possible processing refinements. A loop will thus be formed in which data on final product is used in the design stage to improve the manufactured product.

A computer may also help the design engineer to generate a good set of tests for a given design or process. At present, all test programs are manually generated, and can be inadequate in LSI testing. Although methods do exist to assist the engineer in checking the completeness of a set of functional-test sequences for digital circuits, a method of automatic generation of functional tests is needed to reduce test-program preparation time and cost and to increase program reliability, completeness, and accuracy. Some computer-aided design techniques are presently being used by engineers to debug newly-created test programs, additional techniques are being developed and should soon be available.

Summary

Up to the present time, most of the development effort in computer-aided design has been centered on artwork generation, a major source of error and time in the design process because of the enormous amount of detail involved. With the creation of the open-ended standard-cell library and the computer-aided artwork-generation technology, the problems of artwork generation are becoming manageable. It is now possible to more actively pursue other areas in the manufacturing process, such as simulation, testing, and data analyses, in which computer-aided design can significantly improve the performance of the final product.

Acknowledgments

Because past and present programs have involved many contributions from several RCA divisions, it is not possible to properly acknowledge all of them. Nevertheless, credit is given to Fred Hunter and Pat Lam of the Solid State Division, MOS IC Design Automation Activity, for their outstanding contributions to the artwork-generation effort, and to the Technology Center, Design Automation Activity personnel who developed most of the programs presently used.

COS/MOS is a high-reliability technology

M. N. Vincoff Dr. G. L. Schnable

This paper describes the manufacturing steps and the reliability features of the COS/MOS product lines. The various, constantly updated, quality-conformance criteria, including Groups A, B, and C testing, that assure control of the entire product series are discussed. The high-reliability programs of MIL-STD-883 screening tests and the new quality and testing constraints of MIL-M-38510 are also covered, as are the failure mechanisms of MOS devices and reliability advantages of COS/MOS devices. Calculated reliability figures of failure rate and MTTF for COS/MOS devices are presented along with histograms on thousands of hours of operating life tests covering significant parameters.

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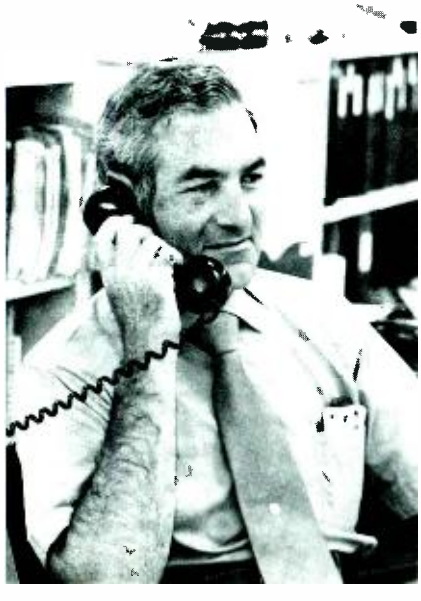

THE COS/MOS TECHNOLOGY was developed initially in support of military and aerospace programs in which the low-power and high noise-immunity characteristics of COS/MOS IC's provided distinct advantages. From the outset, those programs also required high-reliability integrated circuits. One aspect of reliability was met by the low-power-dissipation feature of COS/MOS devices; little or no heat is generated during operation. This important inherent characteristic, along with the reliability constraints imposed on the manufacturing process makes COS/MOS a proven producer of high-reliability devices.

Before proceeding with the description of the product flows of the various COS/MOS product lines, it should be noted that, basically, the complementary MOS technology at RCA consists primarily of a single process and set of design rules that are imposed on all types in the standard line of devices.[1] Therefore, the same standarization of process and design exists in basic gate types as in MSI and low-density LSI types. All three logic-density groups exhibit essentially the same reliability, as demonstrated by test results of failure rate and MTTF.

Since one set of design rules and one process is used throughout the product lines, differences in completed devices are primarily the result of variations in the testing, packaging, and screening sequences used to provide products for different applications and reliability requirements. RCA COS/MOS devices are provided in the following series: chip types CD4000AH series, industrial plastic CD4000AE series, military full-temperature-range ceramic CD4000AK or CD4000AD series, and the high-reliability ceramic CD4000AK or CD4000AD series in four levels for MIL-STD-883 parts and three classes, A, B, and C, for MIL-M-38510 parts. Each product series is a separate product entity; the chips used are processed through the same wafer-processing sequence in each case except for the different electrical tests and visual inspections determined by customer usage requirements.[2,3]

COS/MOS wafer processing

All COS/MOS wafer processing is performed in clean rooms and laminar

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Fig. 1a—Scanning electron microscope at 1000X magnification shows excellent conformity of conductors over wafer contours, assuring continuity and reliability of metal interconnects.

Fig. 1b—6000X magnification shows excellent metal coverage over an oxide step.

flow areas; stringent quality controls insure against device contamination at any step in the fabrication sequence. A total of five test chips are fabricated on each wafer. Tests are applied to these devices to assure that the electrical properties of the silicon-silicon dioxide interface are controlled within close limits and that electrical characteristics are stable at high temperature with an electric field applied. The test chips, biased at 300°C for a specified time, are effective in determining the level of alkali ion instability, and thus provide a measure of the stability attained in each production lot.

MOS circuits contain many locations at which conductor lines cross topographic oxide steps in the underlying dielectric. If proper processing conditions are not employed, the metal lines at the oxide steps tend to be constricted in cross-sectional area, and are susceptible to the formation of electrical opens during temperature cycling or as a result of electromigration effects. In the fabrication of RCA COS/MOS devices, particular attention is given to sloping the oxide edges to assure high-quality metallization paths. The processing techniques used produce wafers in which the edges of the oxide exhibit controlled slopes that can be repeated from lot to lot. Inspections of the metallization runs over the oxides are provided on military and aerospace programs in the form of scanning-electron-microscope (SEM) inspections to NASA specification GSFC-S-311-P-12 A. Fig. 1 shows two photographs taken with the SEM during the inspection. The SEM is also being used as a quality and engineering tool to continually improve and check the metallization quality of the standard COS/MOS product lines not requiring the NASA inspection.

All RCA COS/MOS devices are coated with an amorphous oxide layer that is chemically deposited from a silane-containing gas. This passivation layer effectively reduces susceptibility to metalization scratches and to failure due to electromigration, reduces surface-ion migration effects (by increasing the distance between the dielectric-ambient interface and the silicon), and eliminates the possibility of bridging between adjacent metal lines by external conductive particles. The presence of a small percentage of phosphorus oxide in the passivating glass layer can provide additional reliability benefits, including ability to getter any alkali ions.

High-reliability COS/MOS (MIL-STD-883)

The ceramic CD4000AK and CD4000AD series are available in high reliability types screened in accordance with MIL-STD-883 Method 5004, Class A, B, and C requirements. The units are used in satellites and other aerospace, military, and critical industrial applications in which maintenance is extremely difficult.[4] RCA COS/MOS circuits are provided in four screening levels (/1,/2,/3,/4), as shown in Table I. These levels are marked on the parts following the AK or AD series designation. The four types meet the mechanical and

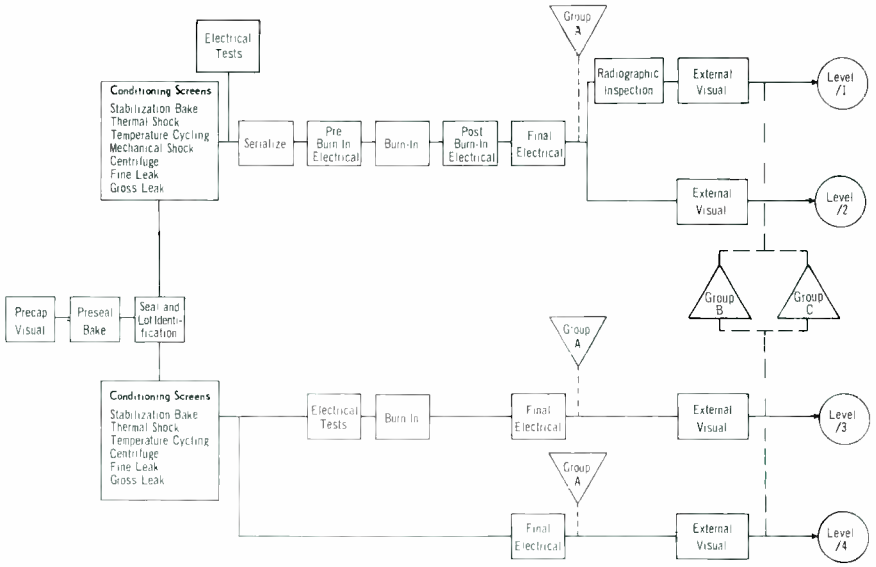

Fig. 2—CD4000AK and CD4000AD high-reliability series product flow chart.

Table I—RCA high-reliability integrated-circuit screening levels.

RCA Level	*MIL-STD-883*	*Application*	*Description*
/1	Class A	Aerospace & missiles	For devices intended for use where maintenance and replacement are extremely difficult or impossible and reliability is imperative.
/2	Class A (without radiographic inspection)	Aerospace & missiles	For devices intended for use where maintenance and replacement are extremely difficult or impossible and reliability is imperative.
/3	Class B	Military & industrial For example, in airborne electronics.	For devices intended for use where maintenance and replacement can be performed but are difficult and expensive.
/4	Class C	Military & industrial For example, on ground-based electronics.	For devices intended for use where replacement can readily be accomplished.

Table II—Description of total lot screening.

Test	Conditions	MIL-STD-883 Method	MIL-STD-883 Conditions	Screening levels /1	/2	/3	/4
1. Precap visual	–	2010.1	B	×	×	×	×
2. Preseal bake	2 hrs (min.) at 200°C	–	–	×	×	×	×
3. Seal & lot identification	–	–	–	×	×	×	×
4. Stabilization bake	48 hrs at 150°C	1008	C	×	×	×	×
5. Thermal shock	15 cycles	1011	C	×	×	–	–
6. Temperature cycling	10 cycles	1010	C	×	×	×	×
7. Mechanical shock	5 pulses, Y_1 direction	2002	B	×	×	×	×
8. Centrifuge	Y_2, Y_1 direction	2001	F	×	×	–	–
	Y_1, direction only	2001	F	–	–	×	×
9. Fine leak	–	1014	A	×	×	×	×
10. Gross leak	–	1014	C	×	×	×	×
11. Electrical tests	–	–	–	×	×	×	–
12. Serialize	–	–	–	×	×	–	–
13. Pre burn-in electrical	–	–	–	×	×	–	–
14. Burn-in	240 hrs	1015	–	×	×	–	–
	168 hrs	1015	–	–	–	×	–
15. Post burn-in electrical	Delta requirements	–	–	×	×	–	–
16. Final electrical	–	–	–	–	–	–	–
a) 25°C	–	–	–	×	×	×	×
b) −55 and +125°C	–	–	–	×	×	S	S
17. Radiographic inspection	1 view	2012	–	×	–	–	–
18. External visual	–	2009	–	×	×	×	×

electrical screening requirements of MIL-STD-883, imposed before the devices are sealed, and the screening test required on packaged parts. RCA offers a /2 part which meets Class A requirements of MIL-STD-883 less radiographic inspection since the aluminum metalization and bonding wires do not show up under this inspection.

The product flow again utilizes the same COS/MOS chips, but tighter electrical and visual inspections are invoked, and more extensive mechanical and electrical tests are performed after sealing, as shown in Fig. 2. After wafer processing, special visual inspections are performed to MIL-STD-883, Method 2010.1, condition B or A at both chip and pre-seal inspections to insure a packaged chip of high reliability. In the case of Class A product (RCA levels /1 and /2), parts are tested functionally, and then receive a DC parameter test; significant parameters are recorded. A 240-hour burn-in at 125°C is performed on all parts. All readings are repeated and delta shifts calculated; the customer is provided with printouts of these parameters identified by the serial number on the part. The parts then go through 100% high- and low-temperature testing under functional and DC operating conditions. Next, 100% AC testing is accomplished followed by Group A, sampling of all test conditions. The Class A product is branded, visually inspected, and retested both functionally and to DC parameters prior to packaging and shipment to the customer. The screening tests for Class B (RCA level /3) and Class C (RCA level/4) product are reduced as shown in Table II in which *X* designates where a test is performed 100% while *S* indicates that the test is a screen. For Class-B product, the main difference is that burn-in is for 168 hours with GO-NO/GO parameter readings made before and after burn-in. Temperature testing is done on a sampling basis, and visual inspection prior to sealing is not as critical. Class-C product is tested similarly to Class-B product less the burn-in, temperature, and AC tests.

Table III—MIL-M-38510 additional requirements.

Requirements	Class A	Class B	Class C
Product assurance plan	×	×	×
Line certification	×	–	–
SEM inspection GSFC-S-311-P-12A	×	–	–
Radiographic	×	–	–
Two bias burn-in 36 hrs	×	–	–
Operating burn-in 240 hrs	×	–	–
Operating burn-in 168 hrs	–	×	–
Tighter DC electrical	×	×	×
Tighter AC electrical	×	×	×

Table IV—COS/MOS devices for which specification sheets have been written.

Detailed electrical specification MIL-M-38510	Device covered
MIL-M-38510/050	
01	CD4011A
02	CD4012A
03	CD4023A
MIL-M-38510/051	
01	CD4013A
02	CD4027A
MIL-M-38510/052	
01	CD4000A
02	CD4001A
03	CD4002A
04	CD4025A
MIL-M-38510/053	
01	CD4007A
02	CD4019A
MIL-M-38510/054	
01	CD4008A
MIL-M-38510/055	
01	CD4009A
02	CD4010A
MIL-M-38510/056	
01	CD4017A
02	CD4018A
03	CD4020A
04	CD4022A
05	CD4024A
MIL-M-38510/057	
01	CD4006A
02	CD4014A
03	CD4015A
04	CD4021A
05	CD4031A
MIL-M-38510/058	
01	CD4016A

No other detailed electrical specifications have been defined by NASA or military agencies at this time. RCA plans to qualify the entire COS/MOS line in the future.

Table V—All product production testing.

Temperature	Test	Test Criteria Hi-rel levels /1, /2	Hi-rel /3 level	Hi-rel level /4	STD ceramic	STD plastic
+25°C	All static parameters	100%	100%	100%	100%	100%
+125°C	Specified static parameters	100%	LTPD=5	—	—	—
−55°C	Specified static parameters		LTPD=5	—	—	—
+25°C	Specified dynamic parameters	100%	100%	—	—	—

Table VI—Group-A electrical-sampling inspection.

Sub group	Test	Condition	Hi-rel levels /1, /2	LTPD Hi-rel level /3	Hi-rel level /4	STD ceramic	STD plastic
1	All static parameters	T_A=+25°C	5	5	5	5	5
2	Specified static parameters	T_A=+125°C	5	7	10	*	*
3	Specified static parameters	T_A=−55°C	5	7	10	*	*
4	Specified dynamic parameters	T_A=+25°C	5	5	5	*	*

*10 devices per month per type tested or testing related to high-reliability product.

High-reliability COS/MOS MIL-M-38510

Since 1970, RCA has been working closely with various aerospace and military agencies to qualify and provide COS/MOS to MIL-M-38510 specifications.[5] Among these agencies are the NASA Goddard Space Flight Center, NASA Marshall Space Flight Center, NASA Headquarters Center in Washington, Rome Air Development Center, and the Defense Electronic Supply Center at Dayton (DESC), a branch of the Defense Supply Agency.

Table VII—Group-B environmental-sampling inspection.[1]

Sub group	Test	MIL-STD-883 Reference	Conditions	Hi-rel levels /1, /2	Hi-rel level /3	LTPD Hi-rel level /4	ceramic	plastic
1	Physical dimensions	2003	Test cond. A per applicable data sheet	10	15	20	20	20
2	Marking permanency	2008	Test cond. B per Par. 3.2.1.			4 devices (no failures)		
	Visual and mechanical	2008	Test cond. B 10× mag.			1 device (no failures)		
	Bond strength	2011	Test cond. D 10 devices minimum	5	15	20	20	—
3	Solderability	2003		10	15	15	10	10
4	Lead fatigue	2004	Test cond. B2 any 5 leads	10	15	15	20	20
	Fine leak	1014	Test cond. A	10	15	15	20	none
	Gross leak	1014	Test cond. C					
5	Operating life critical elec. tests	1005	T_A=125°C, 1000 hrs. test circuit[2]	5	5	10	15	15

[1]Group B tests limited to a production period not to exceed 6 weeks.
[2]Operating life circuits are included in specific type bulletins.
1: Group B tests limited to a production period not to exceed 6 weeks.
2: Operating life circuits are included in specific type bulletins.

Table VIII—Group-C environmental-sampling inspection.*

Sub group	Test	MIL-STD-883 Reference	Conditions	Hi-rel levels /1, /2	Hi-rel levels /3	LTPD Hi-rel level /4	Ceramic	Plastic
1	Thermal shock	1011	Test cond. C	10	15	15	20	20
	Temperature cycling	1010	Test cond. C					
	Moisture resistance	1004	No voltage applied					
	Critical elec. tests							
2	Mechanical shock	2002	Test cond. B, 0.5ms	10	15	15	20	20
	Vibration, var. freq.	2007	Test cond. A					
	Constant elec. acceleration critical tests	2001	Test cond. F					
3	Salt atmosphere	1009	Test cond. A omit initial conditioning	10	15	15	20	20
4	High temp. storage critical elec. tests	1008	Test cond. C, 1000 hrs	7	15	15	15	15
5	Steady-state bias critical elec. tests	1015	Test cond. A, 72 hrs. at T_A=.150°C	7	—	—	—	—

*Group C tests performed at 3-month intervals.

MIL-M-38510 is the general specification for integrated circuits and the top document for MIL-STD-883. This general specification, introduced a year after MIL-STD-883 was in existence, adds a number of quality constraints not included in MIL-STD-883, which is a specification of test methods, procedures, and screening tests. Parts are provided to MIL-M-38510 under a series of /50 numbers of which nine are in existence. These nine numbers cover twenty-five cos/MOS types. Parts meet requirements similar to those of Classes A, B, and C of MIL-STD-883, Method 5004 screening, except that additional requirements, including more test conditions and tightened limits, are imposed. The additional criteria for each class of product is designated by an *X* in Table III. Also provided in MIL-M-38510 tests are PDA's (Percent Defective Allowed) of 10% for the three burn-in operations performed on Class-A product, and 10% for the one burn-in of Class-B product. Table IV provides a list of the cos/MOS devices for which MIL-M-38510/50-number specification sheets have been written.

Production and group A, B, and C testing

All cos/MOS product lines are subjected to 100%-production electrical tests after packaging and group A, B, and C quality testing.[6] Table V shows the test criteria for all product series. At a temperature of 25°C, all product series are 100% functionally tested at voltage extremes to guarantee 3- and 15-V operation. Parametric tests are performed at 5 and 10 V. High and low temperature plus dynamic (AC) testing is performed on high-reliability product. Data from this testing is used as acceptance information for the standard ceramic and plastic product series.

Table VI presents the group A electrical sampling criteria which is used to retest a portion of the product to assure that the 100% or other test parameters meet guaranteed limits. The prime factor is LTPD (lot-tolerance-percent-defective); the referenced numbers specify the required sample size. Again, for special tests of temperature extremes and dynamic (AC) tests, either small quantities are tested or high-reliability test data is used as judgment information for standard ceramic-or plastic-series product.

Group B and C testing is similar to that of MIL-STD-883 for all cos/MOS product series. The purpose of group B and C tests is to show quality conformance of the product being manufactured over specific periods of time. Tables VII and VIII present the ten subgroup tests referenced to MIL-STD-883, the test conditions, and acceptance criteria for all cos/MOS product lines. The tables show that identical tests are performed for high-reliability ceramic and even the plastic series of product with the main difference in the LTPD acceptance test criteria. Identical testing allows a customer to use standard ceramic- or plastic-series product and be assured that it will meet most of the requirements of MIL-STD-883.

Reliability advantages of MOS

Mos integrated circuits have a number of reliability advantages over bipolar

integrated circuits.[7] It is easier to attain high chip complexity with MOS, and thus high gate-to-pin ratios can be attained. Since wire-bond failures are a significant factor in limiting the reliability of small-scale integrated circuits, MOS offers the possibility of significant improvements in equipment reliability by reducing the number of wire bonds, packages, and external interconnections. Moreover, MOS offers the possibility of lower power dissipation per function, which in turn improves device reliability by producing lower chip temperatures during operation. As an approximation, reliability of both MOS and bipolar integrated circuits is an order of magnitude better at 45°C than at 125°C.[8]

MOS IC's also have an advantage over bipolar devices in that the high impedance of MOS devices does not result in high current densities in the metal interconnections; thus electromigration (current induced mass transport) is rarely a problem in MOS devices. Also, high current density problems at metal-silicon contacts are less common.

Since localized defects in silicon are a factor in integrated-circuit reliability, one advantage of MOS compared to bipolar circuits is that no epitaxial layer is required for conventional monolithic MOS devices. Mos devices are thus fabricated in silicon of high crystalographic perfection and there is no possibility of stacking faults or of epitaxial spikes which cause device problems and damage the masks used for photolithography.

Finally, MOS processing is simpler than bipolar processing, and requires fewer steps.[8] The possibility of manufacturing errors which adversely affect reliability is lower in simpler processes.

Complementary arrays have an advantage over other MOS types in that they dissipate considerably less power. The COS/MOS devices also have the advantage of high noise immunity and operation over a wide range of power supply voltages. An added benefit of the complementary-MOS process is that it provides, without additional process-steps, both n^+ and p^+ channel stops.

The complementary MOS technology is currently one of the most widely used process technologies; predictions indicate even wider use in the next several years.[9]

Table IX—High reliability data on 2000 level-two circuits tested for 400 hours each.

	Life performance	
Device tested:	2,000 from the CD4000 family	
Specification:	high-reliability level-2 per data sheet RIC-102	
Test hours:	400 hours each device (10V, 125°C, operating)	
Total device hours:	800,000 hours	
Inoperable failures:	none	
125° failure rate=	0.115%/1000 hours	at 60% confidence
MTTF=	870,000 hours	
55°C failure rate*=	0.017%/1000 hours	at 60% confidence
MTTF=	5,900,000 hours	
25°C failure rate*=	0.005%/1000 hours	at 60% confidence
MTTF=	20,400,000 hours	

*Using acceleration factors from 125°C.

Table X—Long life reliability data on 75 CD4001D circuits tested for 16,000 hours each.

Specification:	RCA Commercial, full-military-temperature range (−55°C to +125°C) per RCA Data Sheet RIC-101A	
Test hours:	16,000 hrs (10V, 125°C, operating)	
Total device hours:	1,200,000 hrs	
Inoperable failures:	none	
125°C failure rate=	0.076%/1000 hrs	at 60% confidence
MTTF=	1,300,000 hrs	
55°C failure rate*=	0.012%/1000 hrs	at 60% confidence
MTTF=	9,000,000 hrs	
25°C failure rate*=	0.0034%/1000 hrs	at 60% confidence
MTTF=	31,000,000 hrs	

* Using acceleration factors from 125°C.

Failure rates and MTTF of COS/MOS

Since COS/MOS devices became available in the standard and high-reliability ceramic and plastic series, several reliability reports have been issued to demonstrate reliability through failure rate and MTTF figures.[4,10,11] These reports present reliability figures, product flows, mechanical and environmental data, reliability test data, and histogram data on significant test parameters.

In addition to the reliability data presented in these reports, reliability data on integrated circuits based on p-channel MOS transistors have been given in a number of publications.[12,13] The reliability of COS/MOS compares favorably with this data. Recent data has been compiled on two significant tests of COS/MOS product: high-reliability level-2 product, Table IX, and standard ceramic product, Table X. The testing of high-reliability circuits involves taking 2000 parts, operating them 400 hrs each in a 10-V oscillator circuit at a temperature of 125°C, and making measurements at 25°C only. No inoperable failures were experienced; the failure rate was calculated to be 0.115%/1000 hrs at 125°C (60% confidence level), and 0.005%/1000 hrs at 25°C. These figures demonstrate expected long-term reliability using short-time performance data.

Table X presents long-life reliability data on 75 standard ceramic parts operating 16,000 hrs each, again in an oscillating circuit at a temperature of 125°C.[14] All measurements were made at a temperature of 25°C and no inoperative failures were experienced. The failure rate calculated at 125°C was 0.076%/1000 hrs, and at 25°C, 0.0034%/1000 hrs, both for a confidence level of 60%. The reliability figures calculated on actual device-hours of operation show that COS/MOS parts exhibit an inherent reliability that compares favorably with or is better than other logic technologies.

COS/MOS histograms of significant parameters

Histograms of significant parameters measured over accumulated operating hours show stability of integrated circuit characteristics. The important device parameters that are monitored during operating- or storage-life tests or extended-operating-life testing are: n- and p-channel leakage current and n- and p-channel threshold-voltage changes. Devices that operate with little parameter change from zero hours to some extended period of time provide an indication of device stability during customer operation over a long period of time.

Histograms of the CD4001AK present parameter data to 2000 hrs.[15] The histograms for n- and p-channel leakage current, Fig. 3, indicate that all devices are well within a 0.1-μA limit, with the lot distribution well within 0.025 μA. The histograms for n- and p-channel

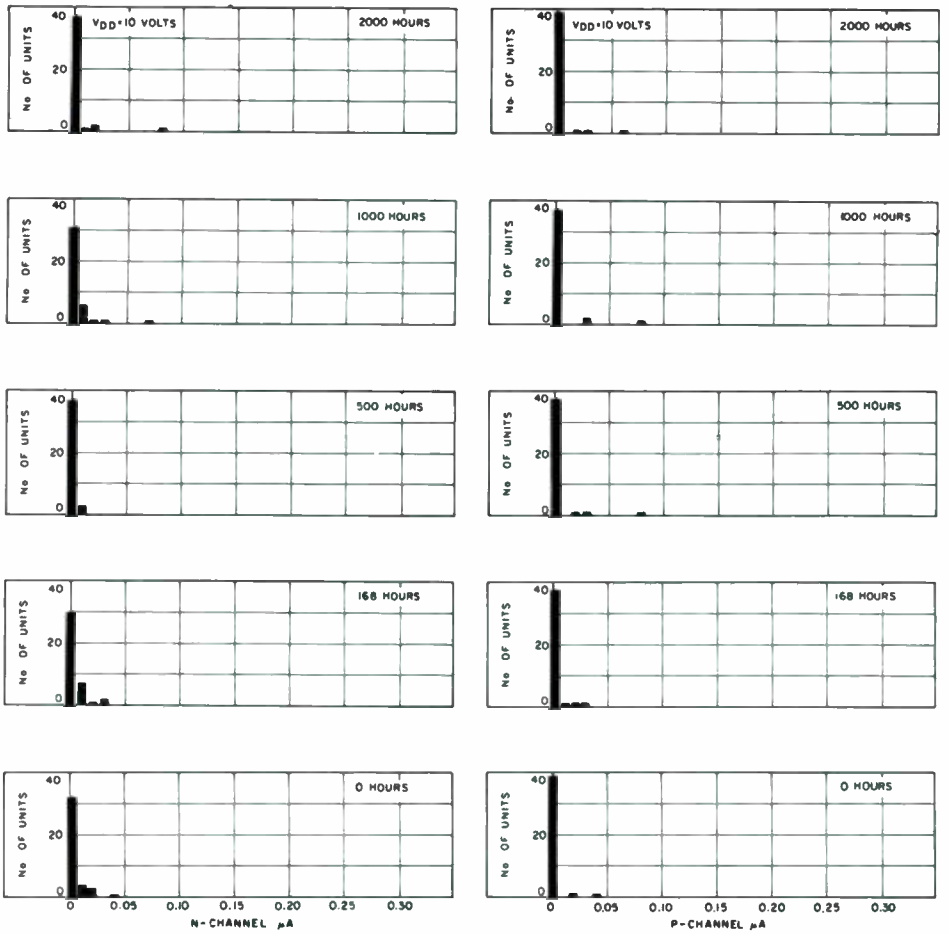

Fig. 3—CD4001AK histograms of n- and p-channel leakage currents.

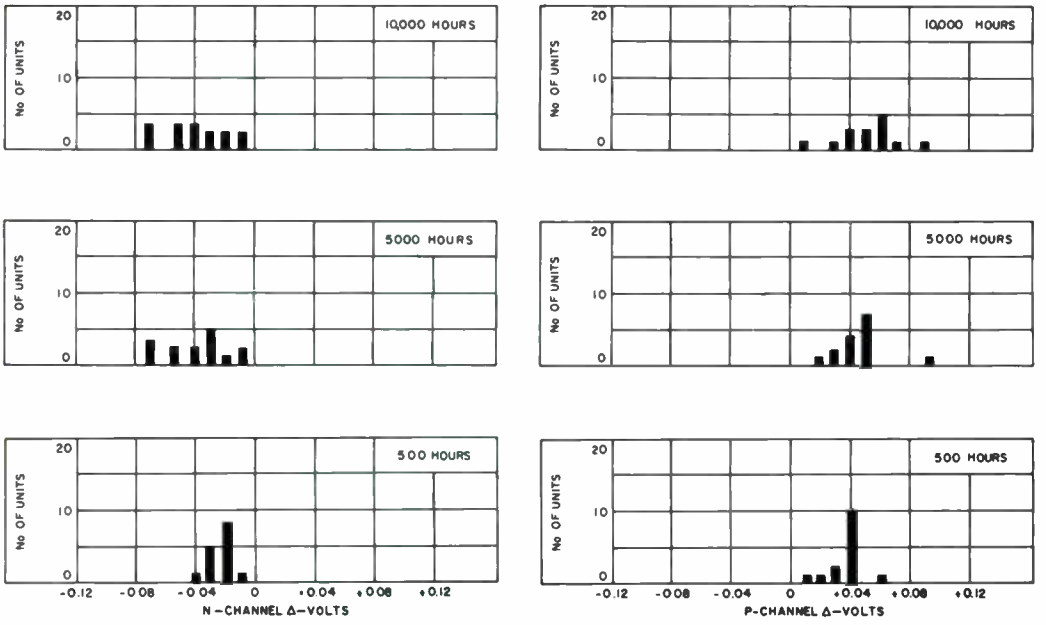

Fig. 4—CD4001AK histograms of n- and p-channel threshold voltages.

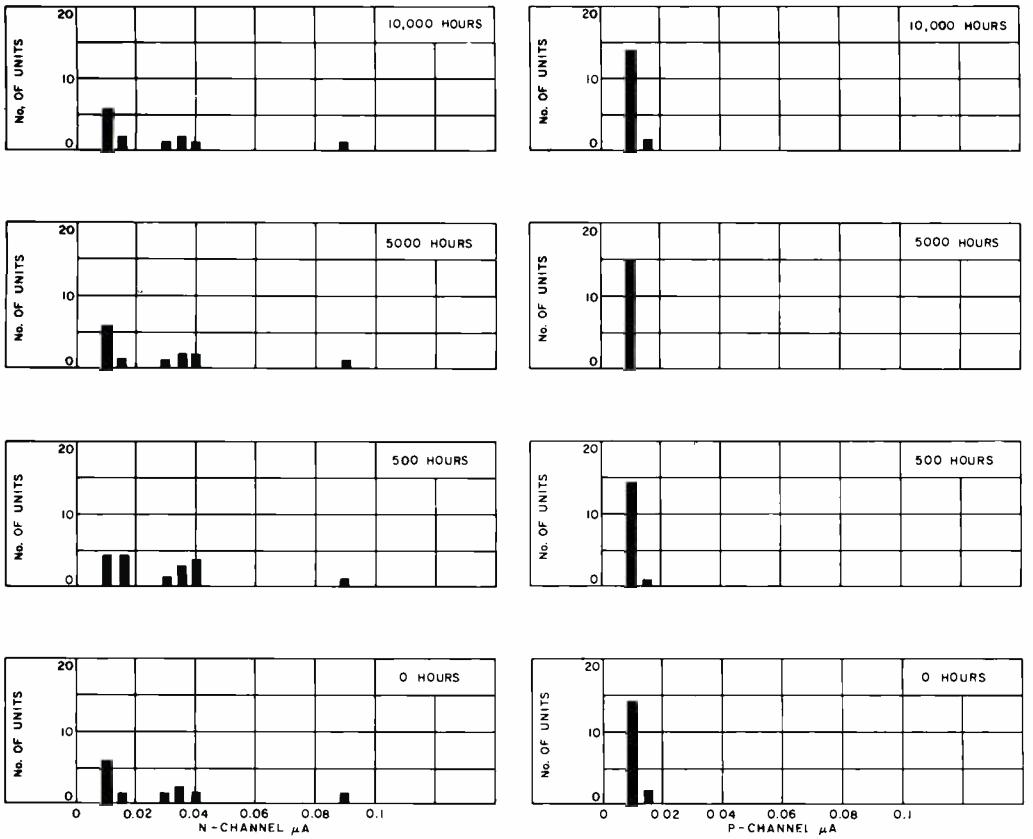

Fig. 5—CD4001AE histograms of n- and p-channel leakage currents.

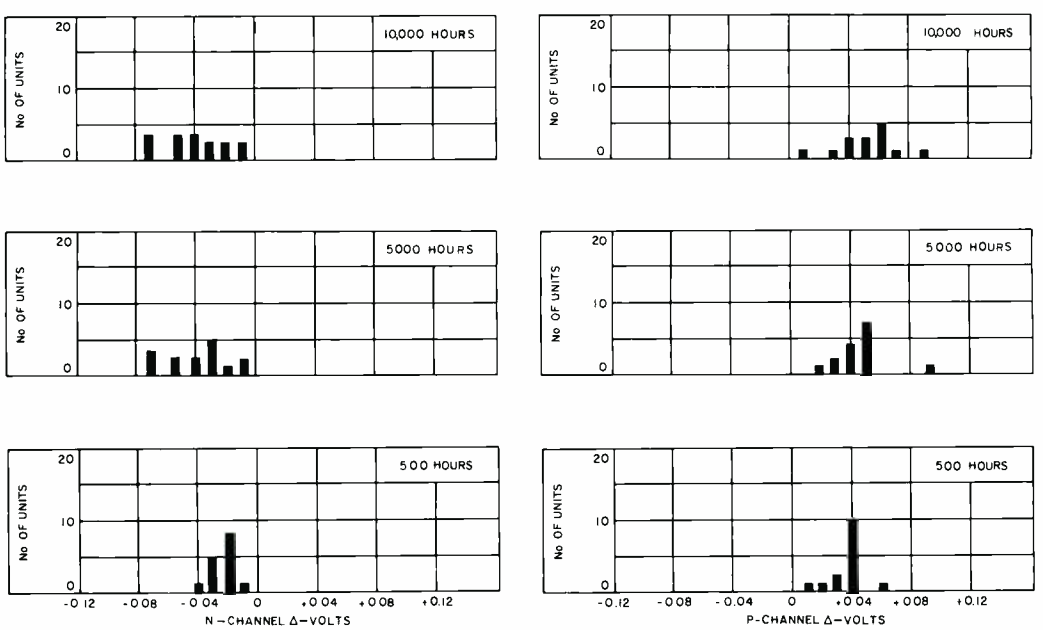

Fig. 6—CD4001AE histograms of n- and p-channel threshold voltages.

threshold voltage, Fig. 4, indicate that delta values remain within ±0.04 V for most of the devices, with a limit of ±0.3 V.

Histograms for a group of plastic CD4001AE parts present long life parameter data to 10,000 hrs.[15] The n- and p-channel leakage currents in Fig. 5 show that most parts exhibit leakages below 0.05 μA, well within the limit of 0.5 μA. The n- and p-channel threshold voltages of Fig. 6 show threshold voltage deltas in the 0- to 0.06-V range, well within the ±0.3-V limit.

The histograms of threshold voltage indicate excellent stability. The detected, very slight shifts are attributed to a very low concentration of alkali ions in the gate oxide; the observed decrease in p-channel-device threshold voltage is attributed to a net negative-charge effect. Observed slight increases in leakage current are attributed to surface effects, the motion of charges in or on the gate dielectric.

Conclusion

The data reported indicate that the reliability of COS/MOS products is good, and reflects the possibilities for a continued improvement in reliability with increased manufacturing experience and volume. The factors that must be controlled if consistently reliable devices are to be fabricated are well understood and are being used during the production process. Moreover, certain process modifications and refinements now being investigated are expected to result in additional improvements in both performance and reliability of future COS/MOS products.

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COS/MOS phase-locked-loop —a versatile building block for micro-power digital and analog applications

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Phase-locked-loops (PLL's), especially in monolithic form, are finding significantly increased usage in signal-processing and digital systems. Signal conditioning, FM demodulation, FSK demodulation, tone decoding, frequency multiplication, clock synchronization, and frequency synthesis are some of the many applications of a PLL. The PLL described in this paper is the COS/MOS CD4046A, which consumes only 600 μW of power at 10 kHz; a reduction in power consumption of 160 times when compared to the 100 mW required by similar monolithic bipolar PLL's. This paper discusses the basic fundamentals of phase-locked-loops, and presents a detailed technical description of the COS/MOS PLL as well as some of its applications.

A QUALITATIVE ANALYSIS of a PLL system is presented here to familiarize the reader with the fundamental principles of phase-lock techniques; the detailed description and analysis of phase-lock techniques is beyond the scope of this paper. The basic phase-lock-loop system is shown in Fig. 1; it consists of three parts: phase-comparator, low-pass filter, and voltage-controlled oscillator (VCO)—all are connected to form a closed-loop frequency-feedback system.

With no signal input applied to the PLL system, the error voltage at the output of the phase comparator is zero. The voltage, $Vd(t)$, from the low-pass filter is also zero, which causes the VCO to operate at a set frequency, f_o, called the center frequency. When an input signal is applied to the PLL, the phase comparator compares the phase and frequency of the signal input with the

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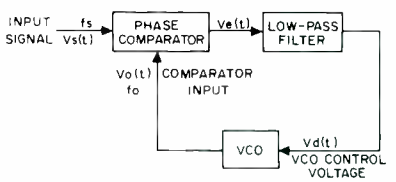

Fig. 1—Block diagram of PLL.

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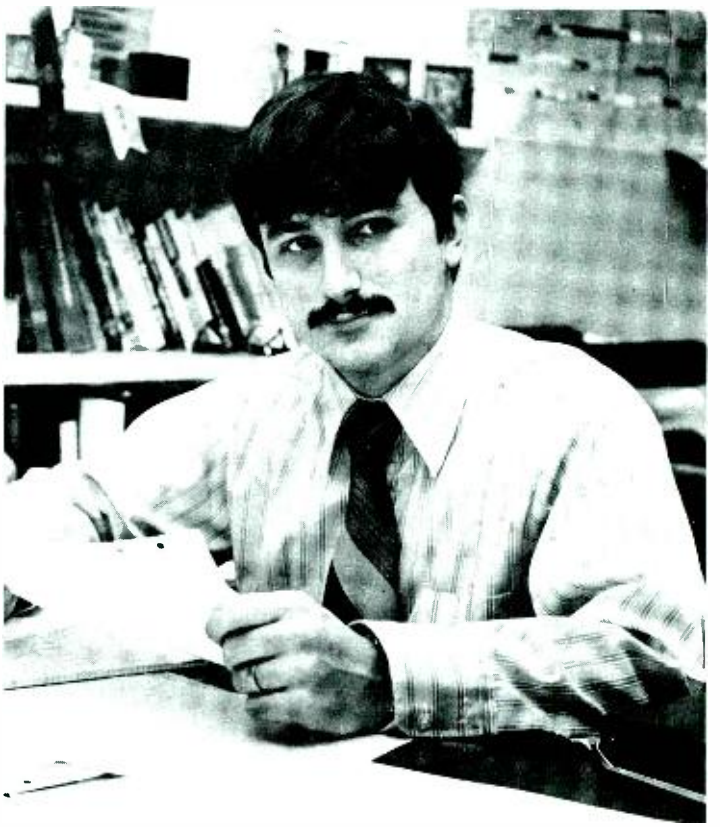


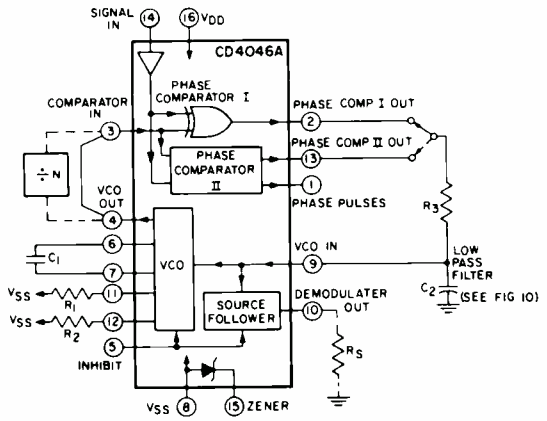


Fig. 2—COS/MOS PLL block diagram.

vco frequency and generates an error voltage proportional to the phase and frequency difference of the input signal and the vco. The error voltage, $Ve(t)$, is filtered and applied to the control input of the vco; $Vd(t)$ varies in a direction that reduces the frequency difference between the vco and signal-input frequency. When the input frequency is sufficiently close to the vco frequency, the closed-loop nature of the PLL forces the vco to *lock* in frequency with the signal input; *i.e.*, when the PLL is in lock, the vco frequency is identical to the signal input except for a finite phase difference. The range of frequencies over which the PLL can maintain this locked condition is defined as the *lock range* of the system. The lock range is always larger than the band of frequencies over which the PLL can acquire a locked condition with the signal input. This latter band of frequencies is defined as the *capture range* of the PLL system.

Technical description of COS/MOS PLL

The COS/MOS CD4046A has been implemented on a single monolithic integrated circuit, as shown in Fig. 2. The PLL structure consists of a low-power, linear, voltage-controlled oscillator (VCO), and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.4-V zener is provided for supply regulation if necessary. The vco can be connected either directly or through frequency dividers to the comparator input of the phase comparators. The low-pass filter is implemented through external parts because of the radical configuration changes from application to application and because some of the components are non-integrable. The CD4046A is supplied in a 16-lead, dual-in-line, ceramic package (CD4046AD); a 16-lead, dual-in-line, plastic package (CD4046AE); or a 16-lead flat-pack (CD4046AK).

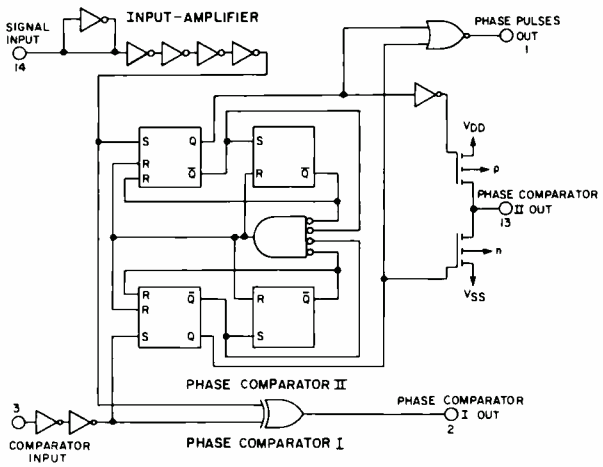


Fig. 3—Schematic of COS/MOS PLL phase-comparator section.

Phase comparators

Most PLL systems utilize a balanced mixer composed of well-controlled analog amplifiers for the phase-comparator section. Analog amplifiers with well-controlled gain characteristics cannot easily be realized using COS/MOS technology. Hence, the COS/MOS design shown in Fig. 3 employs digital-type phase comparators. Both phase comparators are driven by a common-input amplifier configuration composed of a bias stage and four inverting-amplifier stages. The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within COS/MOS logic levels [logic $0 \leq 30\%$ $(V_{DD}-V_{SS})$, logic $1 \geq 70\%$ $(V_{DD}-V_{SS}]$. For smaller input signal swings, the signal must be capacitively coupled to the self-biasing amplifier at the signal input to insure an over-driven digital signal into the phase comparators.

Phase-comparator I is an exclusive-OR network; it operates analagously to an over-driven balanced mixer. When using this phase comparator, the signal- and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase-comparator I supplies the averaged voltage to the vco input, and causes the vco to oscillate at the center frequency (f_o). The frequency range over which the PLL remains locked to the input frequency (lock range) is close to the theoretical limit of $\pm f_c$. The range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the vco center-frequency. A second characteristic is that

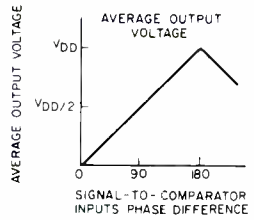


Fig. 4—Phase-comparator I characteristics.

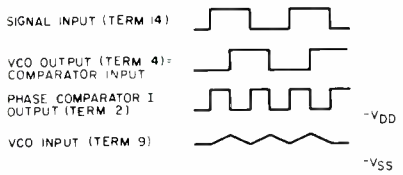


Fig. 5—Phase-comparator I waveforms (waveforms not to scale).

the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig. 4 shows the typical, triangular, phase-to-output, response characteristic of phase-comparator I. Typical waveforms for a cos/MOS phase-locked-loop employing phase-comparator I in locked condition of f_o is shown in Fig. 5.

Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-state output circuit comprising p and n drivers having a common output node as shown in Fig. 3. This type of phase comparator acts only on the positive edges of the signal- and comparator-input signals. The duty cycles of the signal and comparator inputs are not important since positive transistions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON continuously. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON continuously. If the signal- and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal- and comparator-input frequencies are the same, but the signal input lags the comparator in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator input are equal in both phase and frequency. At this stable operating point, both p- and n-type output drivers remain OFF, and the signal at the phase-pulses output is a 1, indicating a locked condition. Thus, for phase-comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. It should be noted that the PLL lock range for this type of phase comparator is equal to the full VCO range. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase-comparator II. Fig. 6 shows typical waveforms for a COS/MOS PLL employing phase-comparator II in a locked condition.

In the state diagram for phase-comparator II (Fig. 7), each circle represents a state of the comparator. The number at the top inside each circle represents the state of the comparator, while the logic state of the signal and comparator inputs, represented by a 0 or a 1, are given by the left and right numbers, respectively, at the bottom of each circle. The transitions from one state to another result from either a logic change on the signal input (*I*) or the comparator input (*C*). A positive transition and a negative transition are shown by an arrow pointing up or down, respectively. The state diagram assumes that only one transition on either the signal input or the comparator input occurs at any instant. States 3, 5, 9, and 11 represent the condition at the output of phase-comparator II when the p-device is ON, while states 2, 4, 10 and 12 determine the condition when the n-device is ON. States 1, 6, 7, and 8 represent the condition when the output of phase-comparator II is in its high impedence state; *i.e.*, both p- and n-devices are OFF, and the phase-pulses output (terminal 1) is high. The condition at the phase-pulses output for all other states is low.

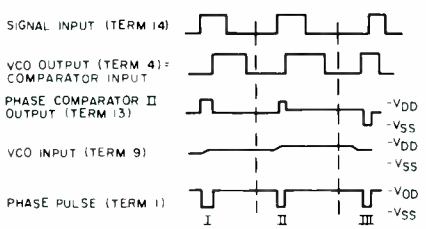


Fig. 6—Phase-comparator II waveforms (waveforms not to scale).

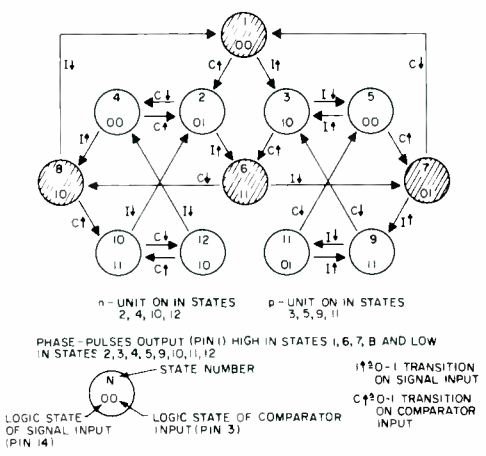


Fig. 7—State diagram of phase-comparator II.

As an example of how one may use the state diagram shown in Fig. 7, consider the operation of phase-comparator II in the locked condition shown in Fig. 6. The waveforms shown in Fig. 6 are broken up into three sections: section I corresponds to the condition in which the signal input leads the comparator input in phase, while section II corresponds to the same conditions as section I, but with a smaller phase difference. Section III depicts the condition when the comparator input leads the signal input in phase. These three sections all correspond to a locked condition for the cos/MOS PLL; *i.e.*, both signal- and comparator-input signals are of the same frequency but differ slightly in phase. Assume that both the signal inputs begin in the 0 state, and that phase-comparator II is initially in its high-impedence output condition (state 1), as shown in Figs. 7 and 6, respectively. The signal input makes a positive transition first, which brings phase-comparator II to state 3. State 3 corresponds to the condition of the comparator in which the signal input is a 1, the comparator input is a 0, and the output p-device is ON. The comparator input goes high next, while the signal input is high, thus bringing the comparator to state 6, a high-impedence output condition. The signal input goes to zero next, while the comparator input is high, which corresponds to state 7. The comparator input goes low next, bringing phase-comparator II back to state 1. Phase-comparator II will go through the

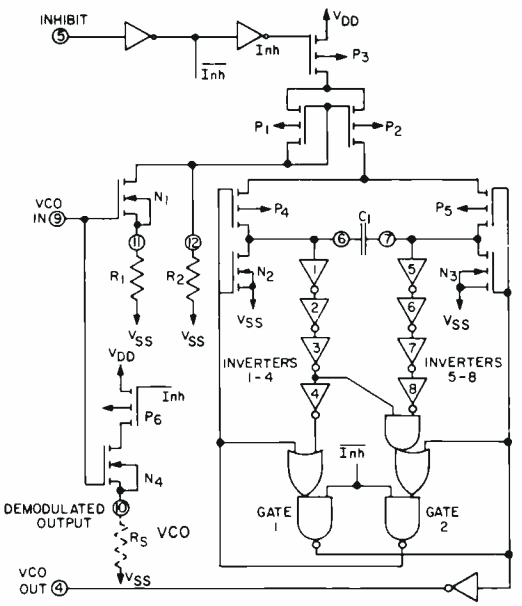


Fig. 8—Schematic of COS/MOS VCO section.

same state-transitions for section II as those that occurred for section I of Fig. 6. As for sections I and II, the p-device stays ON for a time corresponding to the phase difference between the signal input and the comparator input. Starting in state 1 at the beginning of section III, the comparator input goes high first, while the signal input is low, bringing the comparator to state 2. Following the example given for section I, the comparator proceeds from state 2 to states 6 and 8 and then back to 1. The output of phase-comparator II for section III corresponds to the n-device being ON for a time corresponding to the phase difference between the signal and comparator inputs.

The state diagram of phase-comparator II completely describes all modes of operation of the comparator for any input condition in a phase-locked-loop.

Voltage-controlled oscillator

Fig. 8 shows the schematic diagram of the voltage-controlled oscillator (VCO). To assure low system-power dissipation, it is desirable that the low-pass filter consume little power. For example, in an *RC* filter, this requirement dictates that a high-value *R* and a low-value *C* be utilized. The VCO input must not, however, load down or modify the characteristics of the low-pass filter. Since the VCO design shown utilizes an n-MOS input configuration having practically infinite input resistance,

Table I—Maximum ratings and general operating characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage Temperature Range	−65°C to +150	°C
Operating Temperature Range:		
Ceramic Package Types	−55°C to +125	°C
Plastic Package Types	−40°C to +85	°C
DC Supply Voltage Range ($V_{DD} - V_{SS}$)	−0.5 V to +15	V
Device Dissipation (Per Pkg.)	200	mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$	
Recommended DC Supply Voltage ($V_{DD} - V_{SS}$)	5 to 15	V
Recommended Input Voltage Swing	V_{DD} to V_{SS}	

General Characteristics (Typical Values at $V_{DD} - V_{SS}$ = 10 V and T_A = 25°C)

Operating Supply Voltage ($V_{DD} - V_{SS}$)		5 to 15 V
Operating Supply Current		
Inhibit = "0" @ C_1 = 0.0001 μF	f_0 10 kHz, V_{DD} 6 V	100 μA
	f_0 = 10 kHz, V_{DD} = 10 V	220 μA
	f_0 = 100 kHz, V_{DD} = 6 V	350 μA
	f_0 100 kHz, V_{DD} = 10 V	630 μA
Inhibit "1"		10 μA

Table II—VCO electrical characteristics.

VCO Characteristics (Typical Values at $V_{DD} - V_{SS}$ = 10 V and T_A = 25°C)

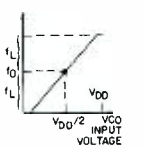
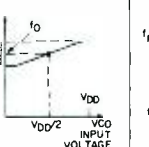
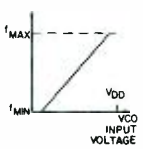
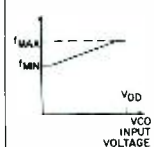
Maximum Frequency	500 kHz
Temperature Stability	500 ppm/°C
Linearity ($V_{VCO\ in}$ = 5 V ± 2.5 V)	1%
Center Frequency	Programmable with R_1 and C_1
Frequency Range	Programmable with R_1, R_2, and C_1
Input Resistance	10^{12} Ω
Output Voltage	10 $V_{p\text{-}p}$
Duty Cycle	50%
Rise & Fall Times	50 ns
Output Current Capability	
"1" Drive @ V_O = 9.5 V	1 mA
"0" Sink @ V_O = 0.5 V	−1.5 mA
Demodulated Output Offset Voltage ($V_{VCO\ in}$ = $V_{DEMOD\ out}$) @ 1 mA	1.5 V

Table III—Comparator electrical characteristics.

Comparator Characteristics (Typical Values at $V_{DD} - V_{SS}$ = 10 V and T_A = 25 C)

Signal Input	
Input Impedance	500 kΩ
Input Sensitivity	
ac coupled	250 mV
dc coupled	"0" ≤ 30% ($V_{DD} - V_{SS}$); "1" ≥ 70% ($V_{DD} - V_{SS}$)
Comparator Input Levels (term. 3)	"0" ≤ 30% ($V_{DD} - V_{SS}$); "1" ≥ 70% ($V_{DD} - V_{SS}$)
Output Current Capability	
Comparators I (term. 2) and Comparator II (term. 13)	
"1" Drive @ V_O = 9.5 V	1 mA
"0" Sink @ V_O = 0.5 V	−1.5 mA
Comparator II Phase Pulses (term. 1)	
"1" Drive @ V_O = 9.5 V	0.7 mA
"0" Sink @ V_O = 0.5 V	−1 mA

Table IV—Phase-locked-loop design equations.

CHARACTERISTICS	USING PHASE COMPARATOR I		USING PHASE COMPARATOR II	
	VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET	VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET
VCO Frequency				
Resistor R_1 and R_2 Approximations	$R_1 \approx \frac{K_1}{f_0 C_1}$	$R_1 \approx \frac{K_1}{f_L C_1}$; $R_2 \approx \frac{2K_1}{(f_0 - f_L) C_1}$	$R_1 \approx \frac{2K_1}{f_{max} C_1}$	$R_1 \approx \frac{2K_1}{(f_{max} - f_{min}) C_1}$; $R_2 \approx \frac{2K_1}{f_{min} C_1}$
Center Frequency, f_0	$f_0 \approx \frac{K_1}{R_1 C_1}$	$f_0 \approx \frac{K_1}{R_1 C_1} + \frac{2K_1}{R_2 C_1}$	Not applicable – for no signal input VCO is adjusted to lowest possible comparator frequency	
Frequency Lock Range, f_L	$f_L \leq \pm f_0$	$f_L \leq \pm \frac{1}{1 + 2\frac{R_1}{R_2}} \cdot f_0$	f_L = full VCO frequency range	
Frequency Capture Range, f_C (see Fig. 3)	$f_C \leq f_L$; $f_C \approx \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{R_3 C_2}}$		$f_C = f_L$	
Phase Angle between Signal and Comparator	90° at center frequency (f_0), approximating 0° and 180° at ends of lock range (f_L)		Always 0° in lock	
Locks on Harmonics of Center Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	

a great degree of freedom is allowed in selection of the low-pass filter components.

The vco circuit shown in Fig. 8 operates as follows: when the inhibit input is low, P_3 is turned full ON, effectively connecting the sources of P_1 and P_2 to V_{DD}; and gates 1 and 2 are permitted to function as NOR-gate flip-flops. N_1 together with external-resistor R_1 form a source-follower configuration. As long as the resistance of R_1 is at least an order of magnitude greater than the ON resistance of N_1 (greater than 10 kilohms), the current through R_1 is linearly dependent on the vco input voltage. This current flows through P_1, which, together with P_2, forms a current-mirror network. External resistor R_2 adds an additional constant current through P_1; this current offsets the vco operating frequency for vco input signals of 0 V. In the current-mirror network, the current of P_2 is effectively equal to the current through P_1 independent of the drain voltage at P_2. (This condition is true provided P_2 is maintained in saturation; in the circuit shown, P_2 is saturated under all possible operating conditions and modes). The set/reset flip-flop composed of gates 1 and 2 turns ON either P_4 and N_7, or P_5 and N_6. One side of the external capacitor C_1 is, therefore, held at ground, while the other side is charged by the constant current supplied by P_2. As soon as C_1 charges to the point at which the transfer point of inverters 1 or 5 is reached, the flip-flop changes state. The charged side of the capacitor is now pulled to ground. The other side of the capacitor goes negative, and discharges rapidly through the drain diode of the OFF n-device. Subsequently, a new half-cycle starts. Since inverters 1 through 5 have the same transfer points, the vco has a 50% duty cycle. Inverters 1 through 4 and 5 through 8 serve several purposes:

1) They shape the slow-input ramp from capacitor C_1 to a fast waveform at the flip-flop input stage;
2) They maintain low power dissipation through the use of high-impedance devices at inverters 1 and 5 (slow-input waveforms); and
3) They provide four inverter delays before removal of the set/reset flip-flop triggering pulse to assure proper toggling action.

In order not to load the low-pass filter, a source-follower output of the vco input voltage is provided (demodulated output). If this output is used, a load resistor (R_8) of 10 kilohms or more should be connected from this terminal to ground. If unused, this terminal should be left open. A logic 0 on the inhibit input enables the vco and the source follower, while a logic 1 turns OFF both to minimize standby power consumption.

Performance summary of COS/MOS PLL

The maximum ratings for the CD-4046A COS/MOS PLL, as well as its general operating-performance characteristics are outlined in Table I. The vco and comparator characteristics are shown in Tables II and III, respectively. Table IV summarizes some useful formulas as a guide for designing a COS/MOS phase-locked-loop system. When using Table IV, one should keep in mind that frequency values are in kilohertz, resistance values are in kilohms, and capacitance values are in microfarads. Fig. 9 should be referred to for vco conversion gain, K_1, values. To provide for fine tuning of the exact frequency of the vco in a PLL system, R_1 or R_2 can be made adjustable resistors ($R_1 \geq 10$ k, $R_2 \geq 10$ k, $R_8 \geq 10$ k, $C_1 \geq 50$ pF). Fig. 2 shows where the external components outlined in Table IV should be connected in a COS/MOS PLL system. Frequency capture range (f_c) and lock-in speed can be improved by using the two-pole low-pass filter shown in Fig. 10 instead of the low-pass filter shown in Fig. 2. The use of Table IV in designing a COS/MOS PLL system for some familiar applications is discussed below.

Applications of the COS/MOS PLL

The COS/MOS phase-locked-loop is a versatile building block suitable for a wide variety of applications, such as FM demodulator, frequency synthesizer, split-phase data synchronization and decoding, and phase-locked-loop lock detection.

FM demodulation

When a phase-locked-loop is locked on an FM signal, the voltage-controlled oscillator (VCO) tracks the instantaneous frequency of that signal. The vco input voltage, which is the filtered error voltage from the phase detector, corresponds to the demodulated output. Fig. 11 shows the connections for the COS/MOS CD4046A PLL as an FM demodulator. For this example, an FM signal consisting of a 10-kHz carrier frequency was modulated by a 400-Hz audio signal. The total FM signal amplitude is 500 mV; therefore the sig-

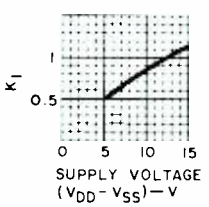


Fig. 9—Typical VCO K1, conversion gain versus voltage.

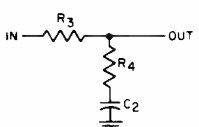


Fig. 10—Frequency capture range and lock-in speed can be improved by using a two-pole LPF instead of LPF shown in Fig. 2. See F. Gardner *Phase Lock Techniques"* (Wiley, N.Y., 1966).

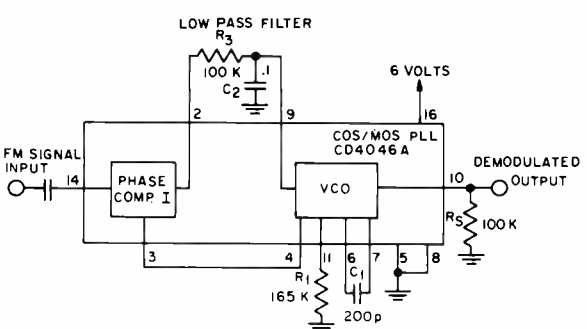


Fig. 11—FM demodulator.

nal must be AC coupled to the signal input (terminal 14). Phase-comparator I is used for this application because a PLL system with a center frequency equal to the FM carrier frequency is needed. Phase comparator I lends itself to this application also because of its high signal-input-noise-rejection characteristics.

The formulas shown in Table IV for phase-comparator I with $R_2=\infty$ are used in the following considerations. The center frequency of the vco is designed to be equal to the carrier frequency, 10 kHz. The vco center frequency is adjusted experimentally as follows:

1) From Fig. 9, find the typical vco conversion gain, K_1, at the supply voltage at which the PLL system will be running.
2) Arbitrarily choose the timing-capacitor C_1 ($C_1 \geq 50$ pF) to determine the approximate value of R_1 by the formula:
$$R_1 = K_1/(f_o C_1)$$
3) Connect an adjustable resistor close to the value of R_1 calculated from the equation above between terminal 11 and ground.
4) Adjust the vco input voltage to $V_{DD}/2$.
5) Adjust the value of R_1 until the exact center frequency is obtained from the vco output (terminal 4).

With the above five simple rules in mind, and using the formulas for phase-comparator I ($R_2=\infty$) in Table IV, the external components for the sample application under discussion were found to be:

$R_1 = 165$ kilohms
$C_1 = 200$ picofarads

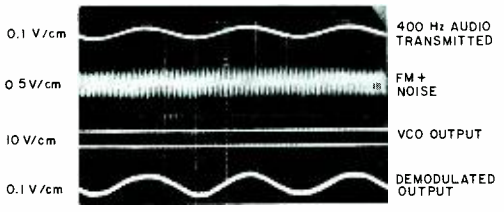


Fig. 12—Voltage waveforms of FM demodulator.

These values determined the center frequency:

$$f_o = 10 \text{ kHz}$$

The PLL was set for a capture-range of

$$f_c \approx \pm \frac{1}{2\pi}\left[\frac{2\pi f_L}{R_3 C_2}\right]^{1/2} = \pm 0.4 \text{ kHz}$$

to allow for the deviation of the carrier frequency due to the audio signal. The components shown in Fig. 11 for the low-pass filter ($R_3=100$k, $C_2=0.1$ μF) determine the above capture frequency.

The total current drain at a supply voltage of 6 V for this FM-demodulator application is 132 μA for a 10 dB S/N on the signal input, and 90 μA for a 10 dB S/N ratio. The power consumption decreases because the signal-input amplifier goes into saturation at higher input levels.

Fig. 12 shows the performance of the FM-demodulator circuit of Fig. 11 at a 4 dB S/N-ratio. The demodulator output is taken off the vco-input source follower using a resistor ($R_S=100$ k). The demodulation gain for this circuit is 250 mV/kHz.

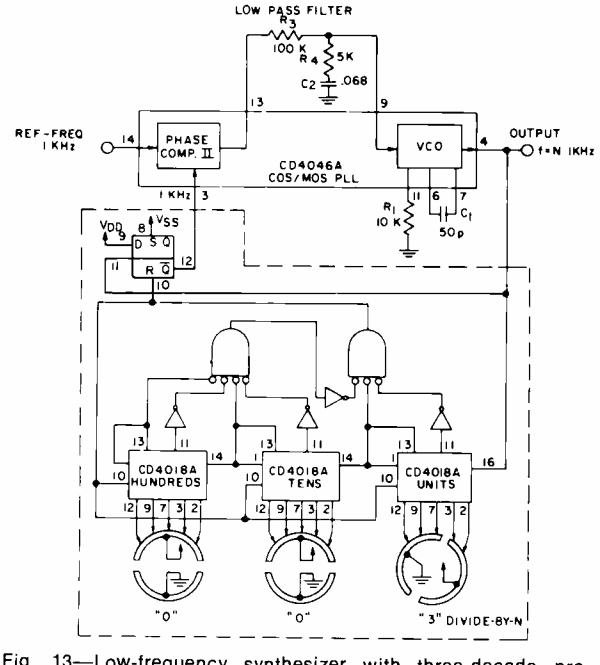


Fig. 13—Low-frequency synthesizer with three-decade programmable divider.

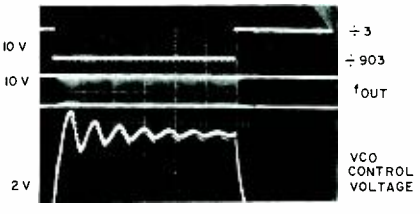


Fig. 14—Frequency synthesizer waveforms.

Frequency synthesizer

The PLL system can function as a frequency-selective frequency multiplier by inserting a frequency divider into the feedback loop between the vco output and the comparator input. Fig. 13 shows a COS/MOS low-frequency synthesizer with a programmable divider consisting of three decades. N, the frequency-divider modulus, can vary from 3 to 999 in steps of 1. When the PLL system is in lock, the signal and comparator inputs are at the same frequency and

$$f = N \times 1\text{kHz}$$

Therefore, the frequency range of this synthesizer is 3 to 999 kHz in 1-kHz increments, which is programmable by the switch position of the divide-by-N counter.

Phase-comparator II is used for this application because it will not lock on harmonics of the signal-input reference frequency (phase-comparator I does lock on harmonics). Since the duty cycle of the output of the divide-by-N frequency is not 50%, phase-comparator II lends itself directly to this application.

Using the formulas for phase-comparator II shown in Table IV, the vco is set up to cover a range of 0 to 1.1 MHz. In this case, the steps for choosing the vco external components are the same as those outlined in the previous section on FM demodulation, with the following exceptions;

2) $R_1 = 2K_1/f_{max}C_1$
4) Adjust the vco input voltage to V_{DD}.

The vco components ($R_1=10$ k, $C_1=50$ pF) shown in Fig. 13 were chosen using the five steps in the previous section with the two exceptions listed above.

The low-pass filter for this application is a two-pole, lag-lead filter which enables faster locking for step changes in frequency. Fig. 14 shows the waveforms during switching between output frequencies of 3 and 903 kHz. The

figure shows that the transient going towards 3 kHz on the VCO control voltage is overdamped, while the transient to 903 kHz is underdamped. This condition could be improved by changing the value of R_3 in the low-pass filter by means of adjustment of the switch-position hundreds in the divide-by-*N* counter.

Split-phase data synchronization and decoding

Fig. 15 shows another application of the COS/MOS PLL: split-phase data synchronization and decoding. A split-phase data signal consists of a series of binary digits that occur at a periodic rate, as shown in waveform A in Fig. 15. The weight of each bit, 0 or 1, is random, but the duration of each bit, and therefore the periodic bit-rate, is essentially constant. To detect and process the incoming signal, it is necessary to have a clock that is synchronous with the data-bit rate. This clock signal must be derived from the incoming data signal. Phaselock techniques can be utilized to recover the clock from the data. Timing information is contained in the data transitions, which can be positive or negative in direction, but both polarities have the same meaning for timing recovery. The phase of the signal determines the binary bit weight. A binary 0 or 1 is a positive or negative transition, respectively, during a bit interval in split-phase data signals.

As shown in Fig. 15, the split-phase data-input (A) is first differentiated to mark the locations of the data transitions. The differentiated signal (B) which is twice the bit rate, is gated into the COS/MOS PLL. Phase-comparator II in the PLL is used because of its insensitivity to duty cycle on both the signal and comparator inputs. The VCO output is fed into the clock input of FF1 which divides the VCO frequency by two. During the ON intervals, the PLL tracks the differentiated signal (B); during the OFF intervals the PLL remembers the last frequency present and still provides a clock output. The VCO output is inverted and fed into the clock input of FF2 whose data input is the inverted output of FF1. FF2 provides the necessary phase shift in signal (C) to obtain signal (D), the recovered clock signal from the split-phase data transmission. The output of FF3 (E) is the recovered binary information from the phase information contained in the split-phase data. Initial synchronization of this PLL system is accomplished by a string of alternating 0's and 1's that precede the data transmission.

Phase-lock-loop lock detection

In some applications that utilize a PLL, it is sometimes necessary to have an output indication of when the PLL is in lock. One of the simplest forms of lock-condition indicator is a binary signal. For example, a 1 or a 0 output from a lock-detection circuit would correspond to a locked or unlocked condition, respectively. This signal could, in turn, activate circuitry utilizing a locked PLL signal. This detection could also be used in frequency-shift-keyed (FSK) data transmissions in which digital information is transmitted by switching the input frequency between either of two discrete input frequencies. one corresponding to a digital 1 and the other to a digital 0.

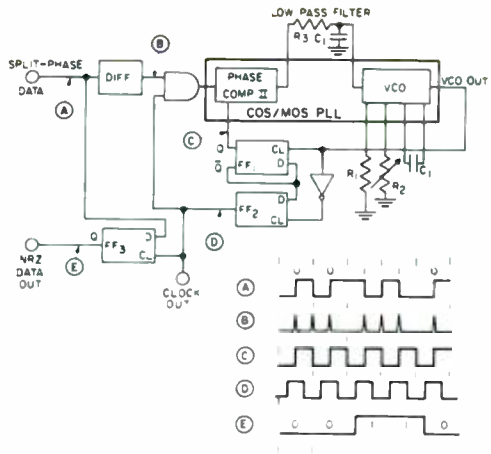


Fig. 15—Split-phase data synchronization and decoding.

Fig. 16 shows a lock-detection scheme for the COS/MOS PLL. The signal input is switched between two discrete frequencies of 20 kHz and 10 kHz. The PLL system uses phase-comparator II; the VCO bandwidth is set up for an f_{min} of 9.5 kHz and an f_{max} of 10.5 kHz. Therefore, the PLL locks and unlocks on the 10-kHz and 20-kHz signals, respectively. When the PLL is in lock, the output of phase-comparator I is low except for some very short pulses that result from the inherent phase difference between the signal and comparator inputs; the phase-pulses output (terminal 1) is high except for some very small pulses resulting from the same phase difference. This low condition of phase comparator I is detected by the lock-detection circuit shown in Fig. 16. Fig. 17 shows the performance of this circuit when the input signal is switched between 20 and 10 kHz. It can be seen that after about five input cycles the lock detection signal goes high.

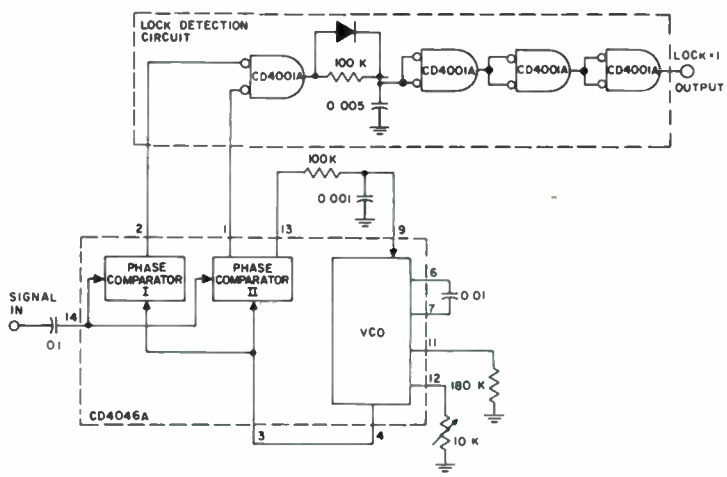


Fig. 16—Lock-detection circuit.

Conclusion

The application of COS/MOS technology to the design of phase-locked loops allows a significant reduction in power consumption over comparable bipolar circuits. This power saving is particularly beneficial in the design of portable battery-powered equipment.

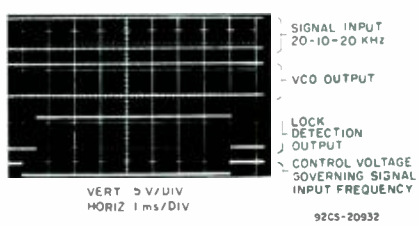


Fig. 17—Lock-detection-circuit waveforms.

A multilayer, hybrid thin-film 1024x3 COS/MOS memory module

F. Gargione | W. Keyzer | G. Noel

A 1024×3 COS/MOS read/write memory hybrid was developed at AED to support various digital equipment applications. Thin-film multilayer techniques were used in fabricating the memory module because they yield extremely high interconnect density.

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received the BSEE in 1961 from Drexel Institute of Technology and the MSEE in 1965 from the Moore School of Engineering, University of Pennsylvana. He joined AED in 1967 and was responsible for the specification, design, test, and production follow-up work for digital, analog, and data-processing equipment for spacecraft. Before joining AED, Mr. Gargione was a microelectronics engineer for the Vector Division of United Aircraft Corporation, where he was responsible for the design, development, and prototype fabrication of oscillators. His previous work was with the General Electric Company as a design engineer for aerospace ground equipment and as a systems engineer for aerospace development systems. He is presently an applications engineer engaged in work on thin-film hybrid circuits. Mr. Gargione is a member of IEEE and Eta Kappa Nu. His publications include the General Electric Technical Information Series Reports: "The Evaluation Program for Digital Integrated Circuits at MSD," and "Flip-Chip Assembly Development." At AED, he contributed to the *Thick-Film Hybrid Handbook*, and he contributed material on thick-film hybrid circuits to the CEE course. This latter material also was presented as a paper at the 1969 ISHM Hybrid Microelectronics Symposium.

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received his early college education in the Netherlands and was awarded the BA in Chemistry from Rutgers University in 1969. He joined RCA in 1959 at the Semiconductor and Materials Division, Somerville, N.J., where he worked in the Polymer Laboratory on solid and liquid encapsulants, coatings, and adhesives for the micro- and mini-module programs. He transferred to AED in 1963, where he worked in the Materials Engineering Group on the development and physical testing of polymer systems for unmanned orbital and space-probe vehicles. During 1966 and 1967 he worked on the development of a thin-film infrared mosaic sensor at the AED Physical Research Laboratory of the David Sarnoff Research Center. He is presently responsible for the vacuum deposition of thin films, electroplating, and chemical-vapor deposition of SiO_2 for hybrid circuits. Mr. Kezer is a member of the American Electroplaters Association.

G. T. Noel*
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received the BS in Physics from Drexel Institute of Technology in 1961. Upon graduation, Mr. Noel joined RCA. He received the MS in Physics from Temple University in 1966 and has since continued his studies beyond this level. Upon joining AED, he was involved in research and developmental work on large-area thin-film *CdS* photovoltaic cells as a member of the Technology Development Group. Later, he participated in investigations of thin-film cells formed from III-V compounds and was actively involved in studies for developing controlled techniques for depositing both polycrystalline and single-crystal gallium phohphide and gallium-arsenide films, as well as the fabrication of various types of photovoltaically active barrier structures on the films. More recently, Mr. Noel has been the principal investigator on a research program to develop sensitive materials for use in infrared detection, imaging, and storage devices. He participated in a NASA-funded study to analyze all previous work in the field of solar cell development and to generate new ideas and recommendations for improving cells in the future. Mr. Noel has co-authored four papers in the field of photovoltaics.

* Mr. Noel recently left RCA to join the research staff of the University of Pennsylvania.

A THREE-LAYER, THIN-FILM, MULTI-LAYER INTERCONNECT STRUCTURE was used in developing the high-density COS/MOS read/write hybrid memory unit. The unit is packaged in a 1x1-in., thirty-two-lead flat pack and contains twelve 256-bit COS/MOS memory chips in a 1024-word by 3-bit configuration. The design and test of the module makes extensive use of computer-aided design.

Electrical design

Specific design goals for the memory module included the following:

1) The required memory had to be organized in groups of 1000 words of 16 bits each plus parity. The memory was designed with a developmental 256-bit read/write random access memory chip, designed and built by the Solid State Division in Somerville, N.J.

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Authors Gargione, Noel and Keyser (left to right).

2) The optimum packaging for hybridization had to take into account size, weight, and complexity, as well as minimizing unused memory cells. The optimum approach resulted in a configuration containing 12 of the 256-bit chips. The resulting package had minimum wasted bits (one per word) and maximum packaging density (equivalent to 150,000 gates/in^3), while its complexity was not overwhelming.
3) Maximum packaging density at the next level of assembly was to be achieved. To accomplish this, certain functions are brought out on adjacent pins. This permits stacking two packages on top of each other, with common address lines on the mother board. The functions with two pins are the D_{in} and D_{out} lines.

Fig. 1 is a schematic diagram showing the memory organization. A rough sketch of the layout is shown in Fig. 2.

Three items are notable in the layout

1) The chips have pads on only two sides, thus permitting very close spacing.
2) The center row of chips is turned 180° so that similar pads on each chip face the same corridor, thus reducing the number of busses needed to interconnect them.
3) All like address lines are tied together, for simpler trouble-shooting.

The interconnect lines are 4 mils wide, with a minimum spacing of 2 mils where a line is adjacent to a "via hole" that permits interconnection through the insulator. The via hole is in most cases 8 mils square with 10-mil pads above and below it. In some cases where via holes are adjacent to each other, the size was reduced to 6-mil vias with 8-mil pads.

The artwork for the etching masks was obtained using a computerized artwork generation system. This system uses a simple language to code the graphics, has a CRT display that permits easy debug and/or interactive design, and prepares magnetic tapes that

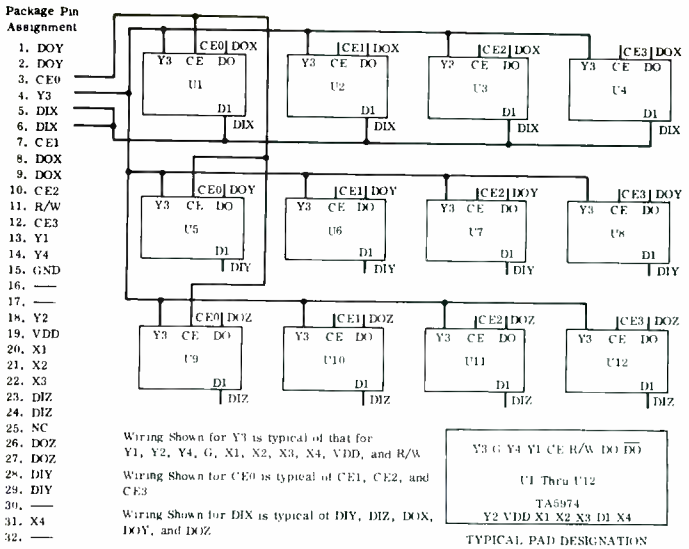

Fig. 1—1024×3 memory organization.

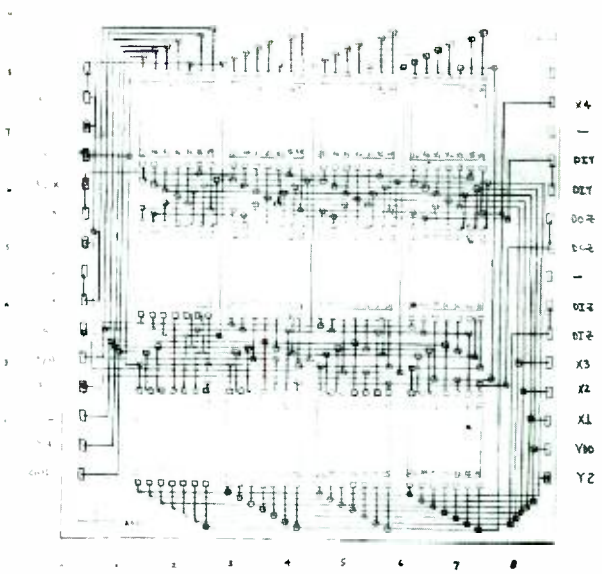

Fig. 2—Layout for hybrid read/write memory array (10× magnification).

control a Gerber flat-bed plotter designed for use with photographic film. The final output of the Gerber is 10X artwork. Fig. 3 is a composite of a group of CRT displays used in making the artwork. The final masks on 2x2-in. glass are prepared at the David Sarnoff Research Center. Fig. 4 is a composite showing the three mask levels required to make the circuit.

Fabrication Processes

The multilayer technique used in constructing the memory module is illustrated in Fig. 5. The thickness of this type of structure, as fabricated in thin-film form, is extremely small. The thickness of the three-layer structure shown in Fig. 5 is typically less than 0.5 mil (exclusive of the substrate thickness). The substrates used in this work were 10-mil-thick alumina, polished to give a surface finish of 1 to 2 microinches.

Fig. 6 illustrates the multi-layer structure fabrication process. The bottom conductive layer (Fig. 6a) consists of three layers of metallization—a layer of copper, sandwiched between two layers of chromium. The chromium serves as an adhesive interface between the copper layer and the substrate and between the copper layer and the silicon dioxide insulating layer. All three of these layers are formed by vacuum evaporation. The thickness of the chromium layers is of the order of 400Å to 500Å, while the copper layer is approximately 1-μ thick. Line widths are 4 mils and the closest spacing is about 2 mils. Pattern definition is accomplished by photoresist masking and chemical etch.

The silicon dioxide insulating layer is formed by the following pyrolytic decomposition process:

$$SiH_4(g) + 2O_2(g) \rightarrow SiO_2(S) + 2H_2O(g)$$

Substrates with the bottom metallization pattern previously defined are placed in an enclosed chamber and

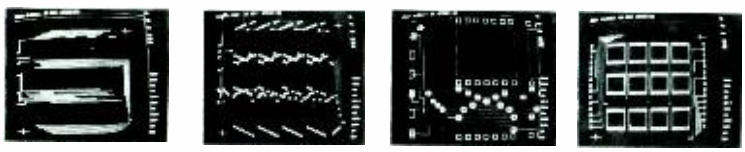

Fig. 3—Interactive artwork generation displays.

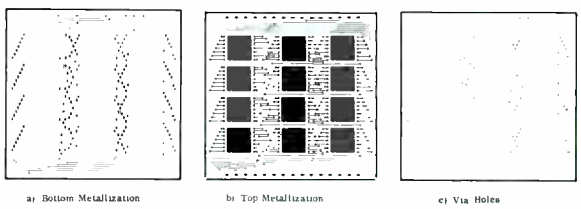

Fig. 4—Final artwork composite of the three mask levels.

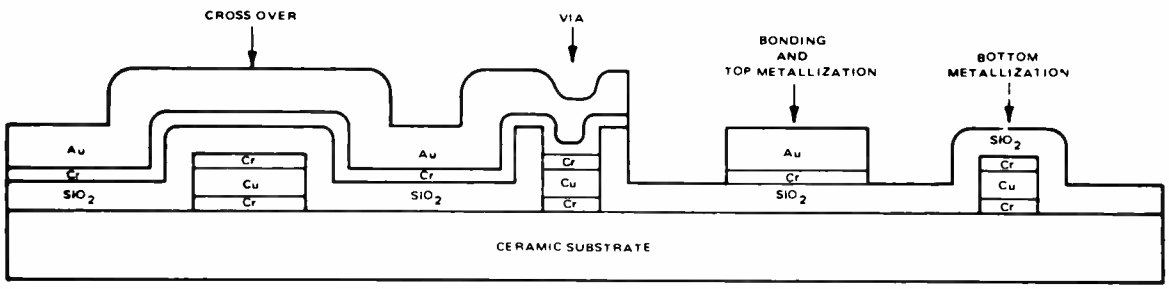

Fig. 5—Multilayer circuit metallization

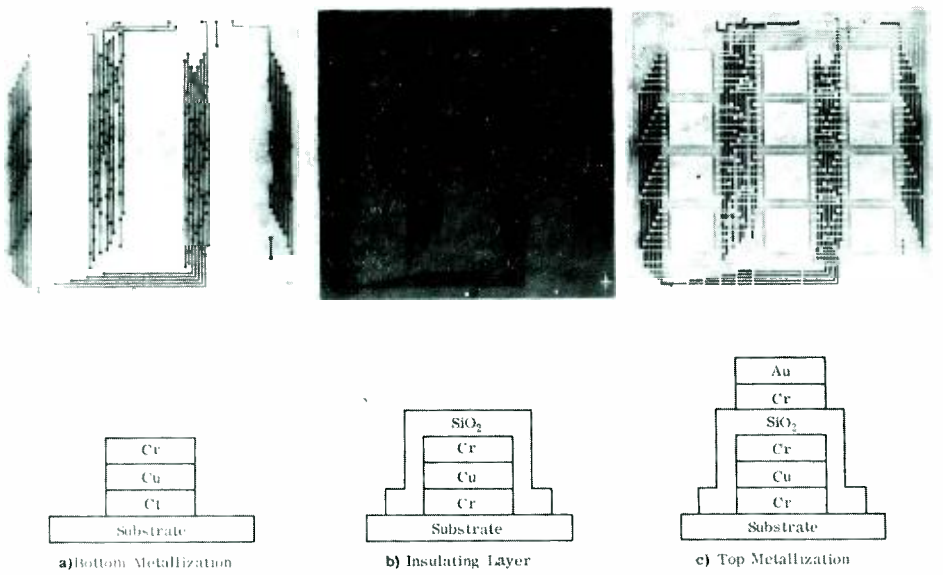

Fig. 6—Substrate processing.

heated to approximately 450°C in an atmosphere of silane, oxygen, and nitrogen. The silicon dioxide layer forms over the entire substrate at a rate of about 1600Å/min. A total silicon dioxide film thickness of 10,000 to 12,000Å is used in the multi-layer structure. Measurements of voltage breakdown characteristics on these films show that field strengths of greater than 7×10^6V/cm can be withstood. After deposition, holes are opened up in the silicon dioxide at appropriate locations to provide for interconnection between the upper and lower metallization layers. In general, the via holes are 8x8-mil squares, although in a few special cases a size of 6x6 mils has been used to adjust for space limitations. Fig. 6b shows a substrate with the bottom metallization and the silicon dioxide layer deposited and with the via holes etched through the silicon dioxide layer. The silicon dioxide layer is transparent and hence not readily discernible.

The top conductive layer also consists of three layers of metallization. An initial thin layer of chromium is vacuum-deposited onto the substrate, again to provide an interfacial adhesive layer. This is followed by a 1-μ-thick vacuum-evaporated gold layer. The gold thickness is then increased to 6 to 7 μ by electroplating, using a selective plating technique which plates up only those areas where a conductive trace or bonding pad is required. Line width is again 4 mils, with a minimum spacing of 2 mils. Gold is used as the top conductive layer because of its bondability, corrosion resistance, and high conductivity. Fig. 6c shows a completed substrate ready for package mounting, die bonding, and wire bonding.

The mounting of the substrate in the flat pack and the attachment of the COS/MOS chips to the substrate are both accomplished by epoxy bonding. Interconnection between the chip and the substrate metallization and the flat pack leads, is accomplished by ultrasonic ball bonding using 1-mil gold wire. Fig. 7 shows a typical epoxy-bonded chip with wire bonds.

The completed circuit (Fig. 8) is mounted in a 1x1-in., 32-pin flat pack, which is hermetically sealed using a parallel-seam welder.

Testing

Testing of the completed module has been performed, first by using a computer programmed to load predetermined patterns into its own memory and into the module and then comparing the module output against the computer memory contents. Several patterns are used to fully test each 256x3 block.

During process, tests were carried out at the substrate level for shorts between levels and for insulation resistance.

No tests were performed on the chips prior to assembly. But chips were wired in groups of three and each 256x3 block tested, so that if a failure occurred on any of the address lines it would be easier to locate the faulty chip and replace it.

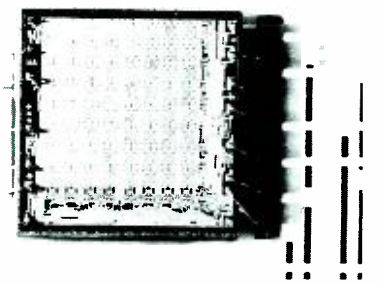

Fig. 7—Substrate detail illustrating die and wire bonding.

Conclusion

This module has demonstrated that this thin-film, multilayer technology can provide extremely high packaging density because of the narrow line widths and large crossover capabilities. The package has an equivalent gate density of approximately 150,000 gates per in.^{3} and contains 622 crossovers. It also points to the need for computers both in the design and test phases when dealing with highly complex circuitry.

Acknowledgments

We would like to express our appreciation for the support of other AED Microelectronics Technology Group personnel, particularly Ray Wondowski for assembly and wire bonding. In addition, we would like to acknowledge the contribution of Marv Novick and Ken Boilen of AED for sealing and developing the computer test programs, respectively; and Fred Teger, Larry French and Hans Schnitzler of RCA Laboratories for their guidance in the use of the computer-aided artwork generation system.

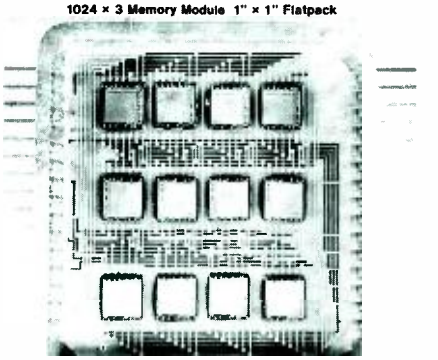

Fig. 8—1024×3 memory module, 1×1 inch flatpack.

Magnetic bubble technology

Dr. A. Akselrad | L. S. Onyshkevych | Dr. R. Shahbender | C. Wentworth

The "bubble" technology is concerned with the creation and manipulation of cylindrical magnetic domains in single-crystal-garnet (or orthoferrite films) for the realization of a wide variety of digital systems. Specific bubble devices such as generators, annihilators, and bubble sensing techniques are described. Experimentally determined margins for these devices are shown. A brief description of bubble materials and materials growth is included. Mass memory system designs are considered and performance characteristics estimated. Some representative characteristics are a capacity of 4 x 10^6 bits in a volume of 1.44 cubic inches with a power consumption of 20 watts at an effective serial rate of 40 Mbps.

THE "BUBBLE" (cylindrical magnetic domain) technology is anticipated to have a promising future, initially for digital data storage, and later for other diverse applications. The objectives of the Laboratories research program are:

1) To define the technology, *i.e.*, determine the materials and processes required for fabricating bubble devices;
2) To determine operating characteristics of bubble devices and subsystems, *i.e.*, determine the operating parameters such as bit density, bit transfer rate, signal-to-noise ratio, power consumption, weight, volume, etc. that may be realized in bubble memory subsystems;
3) To exploit the versatility of the bubble technology (storage, switching, and logic on the same chip) to realize novel memory system organizations; and
4) To exploit the magnetic and magneto-optic properties of materials suitable for bubble devices for other diverse systems and devices.

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To meet these objectives the effort has encompassed both materials and device research. Chronologically, orthoferrites were found to be useful for bubble devices prior to the development of the uniaxial garnets. In our work we have accomplished considerable device testing and experimentation on orthoferrite platelets, because of their availability, and have also synthesized orthoferrite compositions suitable for magneto-optic applications. With the development of the uniaxial garnets, we expanded the research effort to include work on garnets. We hope to demonstrate the realization of high density bubble systems with single-crystal liquid-phase-epitaxial garnet films.

Device and systems description

Magnetic domains in the shape of cylindrical "bubbles" may be readily produced in thin platelets, or films, if the direction of magnetization is perpendicular to the plane, as shown in Fig. 1. Bubbles may be generated, propagated anywhere in the plane, and destroyed by the activation of appropriate thin-film permalloy and conductor circuits. Detection of bubbles may be accomplished by sensing the magnetic flux from the bubble or by sensing the change in the state of polarized light transmitted through the bubble material.

In a device, bubbles are propagated serially along well-defined channels (registers). This property leads naturally to a block-oriented memory organization, similar to a magnetic disc memory. However, with a bubble memory there are no moving parts and access is completely electronic. A block diagram of a possible bubble memory organization is shown in Fig. 2, with each channel being equivalent to an all-electronic shift register. The presence of a bubble may represent a binary "1" and the absence of a bubble may represent a binary "0".

In practical devices, a desired bubble diameter d may be achieved in platelets or films of thickness t, such that:

$$d/2 < t < 2d. \qquad (1)$$

Bubbles may be packed in an $nd \times nd$ array such that $n > 3$. Thus the bubble density in the plane may be as high as $10^{-1}/d^2$. For a bubble diamter of 1/3 mil, or about 8 μm, the bubble density is about 10^6 bubbles/in^2. Even higher densities have been achieved in available materials. The present limit, set by lithography, is about 10^7 bubbles/in^2.

The propagation speed of bubbles is determined by the bubble mobility, μ, which is related to the bubble velocity,

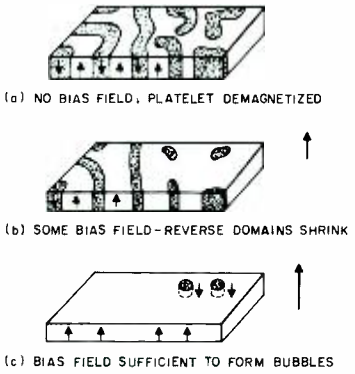

Fig. 1—Formation of "bubble" domains: a) No bias field—platelet demagnetized; b) Some bias field—reverse domains shrink; c) Bias field sufficient to form "bubbles".

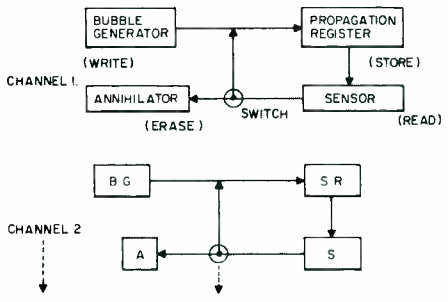

Fig. 2—Possible bubble memory organization.

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Authors Wentworth, Onyshkevych, Akselrad and Shahbender (left to right).

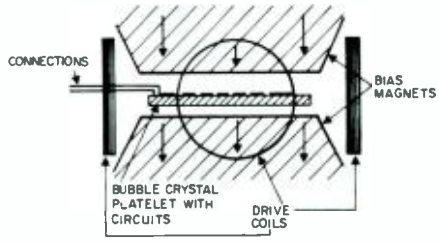

Fig. 3—Bubble-memory chip with bias magnets, drive coils, and circuits.

V, and the applied vertical field gradient, ΔH, by the expression:

$$V \simeq \frac{1}{2}\Delta_{\mu}\Delta H. \qquad (2)$$

The bubble propagation rate is, therefore:

$$r \simeq \frac{V'}{nd} \qquad (3)$$

where V' is the average bubble velocity, Practical values of μ, ΔH and d, which depend on the material used, are such that bit rates r of more than 1 Mbit/sec are possible.

The construction of a bubble memory device requires a number of components external to the bubble platelets, as shown in Fig. 3. A DC bias magnetic field normal to the platelet must be applied to define and maintain a characteristic bubble diameter. This bias field (of ~30 to 60 Oe) can be supplied by permanent magnets.

Bubble motion is produced by the activation of thin magnetic film patterns by an AC magnetic drive field, of ~20 to 30 Oe, which rotates 360° within the plane of the platelets. The AC magnetic drive field may be applied either synchronously or asynchronously, as desired, by two sets of orthogonal coils as shown schematically in Fig. 3. The coils may be driven in a resonant mode to minimize power dissipation.

Generation of bubbles and bubble steering between alternate propagation paths require the use of conductor patterns in addition to the magnetic films. Current pulses must be applied to the conductors by external pulse generators in synchronism with the rotating drive field.

Many bubble shift registers may be driven simultaneously in one set of coils, with thin-film circuitry for encoding and decoding addresses on the bubble platelets. Alternatively, more than one set of drive coils may be used

such that some, or all, coding is accomplished by selectively switching the drive currents among the coils.

Circuits

Circuit fabrication

Bubble circuits are fabricated on chips, as shown schematically in Fig. 4. Orthoferrite crystals, which have relatively large bubbles and are thick, are usually used in conjunction with circuits fabricated on a glass or plastic overlay (Fig. 4a). Garnet crystal films (on appropriate substrates) have small bubbles, so the circuit-to-crystal spacing is more critical. In this case, the circuits are usually deposited on the garnet film, with an SiO_2 spacer layer, as shown in Fig. 4b. This layer is used to avoid pinning of bubbles by the permalloy.

In both cases, the circuits are deposited by vacuum evaporation and then etched by photolithographic techniques. Circuits with lines as fine as ~3 μm can be fabricated by this technology; this accomodates bubbles down to 6 μm in diameter (bit density $>10^6$ bits/in.^{2}). For smaller bubbles, techniques such as electron-beam or ion-beam etching may have to be used.

At least two layers of circuitry (permalloy and conductors) have to be fabricated. Contacts are made to the conductor loops by ultrasonically bonding fly-wires, or using beam leads.

Propagation circuits

In bubble memories, information is stored in shift registers. Many different register circuits are available for memory design. The most promising are of the field-access type, that is, circuits in which motion of bubbles is accomplished by interaction of the bubbles with permalloy film elements, which in turn are driven by an external rotating magnetic field.

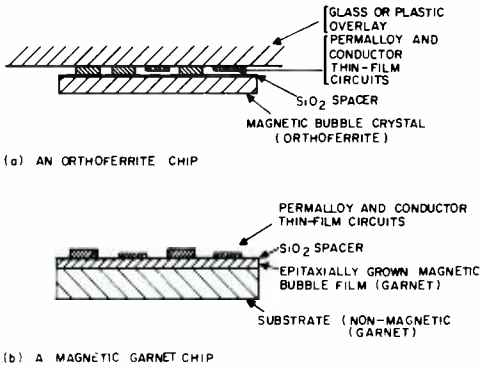

Fig. 4—Bubble circuits—crossection of a chip: a) An orthoferrite chip; b) A magnetic garnet chip.

Three types of field-accessed permalloy patterns are under consideration: T-bar[1] (Fig. 5), Y-bar[2] (Fig. 6), and chevron[3] (Fig. 6). We have constructed and tested propagation patterns up to 100 bits long of the T-bar and Y-bar types. Operating speeds up to 100 kb/s were achieved with small closed T-bar and Y-bar loops, where the speed was limited by the inductance of the driving coils and not by the patterns themselves. Closed-loop T-bar patterns (equivalent to 8 bits) have been fabricated for use with orthoferrite and garnet crystals with bubbles of 3, 1, ½, ⅓ and ¼ mil diameter.

Fig. 7 shows typical operating margins of a Y-bar memory register on *SmTb* orthoferrite. The bias field has to be held within a range of approximately ±10%. If the field is too high, bubbles collapse, if it is too low, bubbles strip out. The driving field has to be at least 15 Oe for this case, otherwise the permalloy elements are not sufficiently magnetized to cause bubble motion. The margins get smaller as the operating speed increases.

The register patterns shown in Figs. 5 and 6 are folded many times to achieve maximum packing density. The corners have to be designed carefully to prevent operating margin degradation. The corners shown in Figs. 5 and 6 have operating margins only slightly narrower than those of the straight sections.

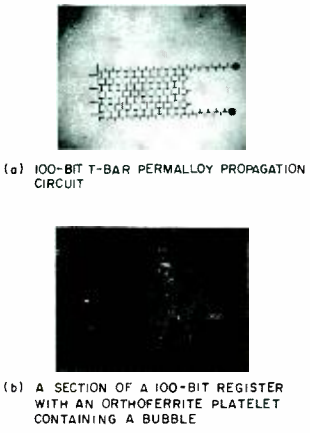

Fig. 5—T-bar 100-bit shift register: a) 100-bit T-bar permalloy propagation circuit; b) Section of a 100-bit register with an orthoferrite platelet containing a bubble.

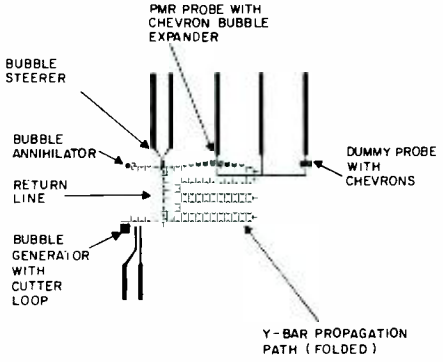

Fig. 6—Photolithographic artwork of an 80-bit Y-bar shift register, with a bubble generator, annihilator, steerer circuit, a chevron expander, and a PMR probe.

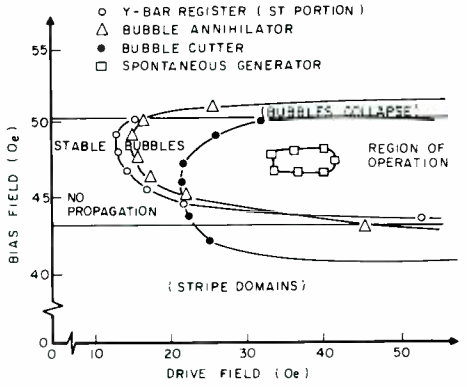

Fig. 7—Typical operating margins of a Y-bar shift-register, bubble annihilator, and two different types of bubble-generators (cutter-type and "spontaneous" generator).

Bubble generators

Bubbles have to be selectively created to write information. Two types of bubble generators are available: spontaneous generators, which generate a bubble on every cycle, and bubble cutters, which use a current loop to cut a bubble in two if a binary "1" is to be written.

The spontaneous generator has to be used in conjunction with a bubble-steering current loop to steer unwanted bubbles (binary "0"'s) into a short side-register, where the bubbles are annihilated. The operating margins that we realized with this type of generator are very tight as shown in Fig. 7.

With the bubble-cutter type of generator, we have realized much wider operating margins, equivalent to the margins of the propagation section of a register (see Fig. 7). However the current required to *cut* a bubble is higher (0.7 to 1.2A) than that used to *steer* a bubble (20 to 50 mA).

The advantages of the above two types of generators have been combined into a generator that minimizes the required cutting current and maximizes the operating margins. The cutting loop of this generator has been further optimized by a computer calculation. This generator (see Fig. 6) was operated with cutting currents of only 200 mA, and yet had margins of operation actually wider than those of a straight propagation section.

Bubble annihilators

It is necessary in a memory to annihilate bubbles to erase information (clear operation). The annihilate function can be very conveniently performed in an annihilator circuit, as shown in Fig. 6. This annihilator has very wide operating margins (see Fig. 7) and does not require any conductor loops.

Sensing

Among the many methods that have been proposed[4] for sensing magnetic bubbles, two show greatest promise: 1) magnetoresistive probes and 2) optical sensing, using Faraday rotation of transmitted light.

The former method depends on sensing the magnetic flux from a bubble domain and thus requires that the sensing element be in close proximity to the bubble film. By comparison, optical sensing allows the light source and light detector to be at some distance from the bubble film. The magnetoresistive probe depends only on the bubble material, whereas optical sensing requires that the magneto-optical properties of the bubble material be suitable for optical detection. Only a few bubble materials satisfy the latter requirement.

Magnetoresistive method

A planar magnetoresistive probe (PMR)[5,6] produces a voltage due to the change in resistance that occurs when the magnetization of the active element is rotated in the plane of the element. Devices of this type use the same technology and the same *Ni-Fe* permalloy that is used for bubble propagation patterns. It is found that

1) The permalloy detection element must be 500Å thick, or thinner, for the bubble field to overcome demagnetizing effects;
2) The elements are sensitive to the rotating in-plane drive field and to the stray fields from other permalloy elements which produce common mode noise voltages;
3) The detection element must be carefully positioned with respect to the bubble to maximize the sense signal voltage;
4) The signal levels generated by a PMR probe for a 6-μm bubble are about 200 μV/mA of DC current in the probe (to get the above signal, the small bubbles in garnet crystals have to be expanded a few diameters at the detection location)[3,6].

Fig. 8 shows some possible designs of magnetoresistive probes, with dummy probes for common-mode noise cancellation. Fig. 6 shows a different design, with a chevron-type bubble expander.

The magnetoresistive probe, coupled to an expander pattern, appears to show promise of being a practical sensing method for bubble domains less than 10 μm in diameter.

Optical sensing

Optical sensing requires assembling a light source, polarizer, analyzer, and light detector on the bubble chip. Fig. 9 illustrates schematically the design of such a detector. Experimentally, we have obtained sense signals in excess of 1 mV from 25-μm-diameter bubbles in *SmTb* orthoferrite platelets using a *He-Ne* laser with an output of 1 mW at 6328Å and a silicon photodetector (PIN diode). Light-emitting diodes (LED) are expected to be suitable for use instead of lasers in an all-solid-state detection scheme.

Our analysis indicates that 1-mV sense signals may be obtained from selected garnet compositions with bubbles having a diameter in the range of 5 to 10 μm. Table I lists the magneto-optic

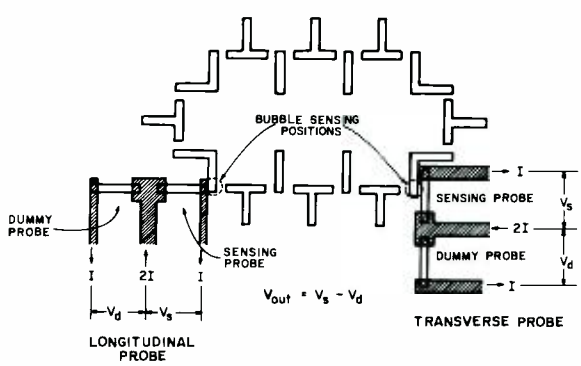

Fig. 8—Rectangular PMR probes with dummy probes for common-mode noise cancellation.

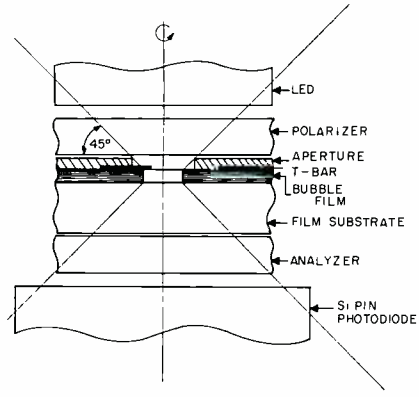

Fig. 9—Solid state optical detector design for use in bubble devices.

Table I—Optical sensing of bubbles in garnet films

Material	Wavelength (A)	Faraday Rotation (degrees/mil)	Percent** transmission factor of 12-μm-thick film	Required LED power density (μW/mil²)
$Bi_{3-2x}Ca_{2x}V_xFe_{5-x}O_{12}$	7500	16.6	24	300
($x \simeq 1.06$)	6328	34	11	650
$Y_{3-2x}Ca_{2x}V_xFe_{5-x}O_{12}$	7500	2.7	4	1800
($x \simeq 1$ to 1.1)	6328	4	2.2	3400
$Y_{3-x}Bi_xGa_yFe_{5-y}O_{12}$	7500	3.75*	5.2	1380
($x \simeq 0.4, y = 1.0$ to 1.3)	6328	8.2*	5	2860
$Y_3Fe_{3.7}Ga_{1.3}O_{12}$	7500	Negligible	—	—
	6328	1.3	1.3	6000

*Calculated values.
**Polarizer-analyzer adjusted to maximize the optical signal.

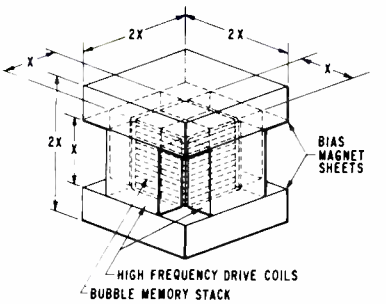

Fig. 10—Schematic diagram of a memory module.

parameters of some garnets and the power density required from an LED to generate a 1 mV signal from a bubble of 6-μm diameter. For these calculations, the garnet film thickness is assumed to be 12 μm, and the bubbles are not expanded at the detector position.

The LED's now under development at RCA show promise of narrowband emission of more than 500 μW/mil² under CW operating conditions over a fairly wide wavelength range. Expanding the bubble diameter by a factor of three reduces the required LED power density, given in Table I, by an order of magnitude.

Both of the above sensing methods produce signals that are roughly proportional to the volume of the cylindrical bubble domain. In both cases, the sense signals obtained from a small bubble might be too small. Expansion of the bubble by a factor of three to ten might be necessary to obtain adequate signal amplitude and S/N ratio. Such expansion can be performed either by a bar-type stretcher, by a chevron-type stretcher (shown in Fig. 6), or by a current lop, which requires a 50- to 200-mA current pulse.

Logic and steering

There are three available methods for performing logic with bubbles:

1) Bubble-bubble interactions,
2) Bubble interactions with permalloy films, and
3) Bubble interactions with fields from current-carrying loops.[7]

One of these methods must be employed if on-chip decoding is desired.

Logic gates employing bubble-bubble interactions have very tight margins of operation and do not perform well at high repetition rates. Therefore this method is not recommended.

Bubble-magnetic film interactions can be utilized to a limited extent. Gates built on this principle steer a bubble stream into one of two channels, depending upon the direction of rotation of the drive field. Such gates have operating margins that are only slightly tighter than the margins of the propagation section of a register.

Bubble-current loop interactions are simplest to achieve in practice. Very small currents (20 to 50 mA) are required to steer a bubble into one of two propagation channels. Fig. 6 illustrates a simple "bubble steerer." The operating margins of these circuits are equal to those of the Y-bar patterns. Such steerers can be combined into binomial decoders[8] or other arrays for performing necessary bubble logic. The only drawback of these circuits is the necessity of connections to the current loops.

The complete memory register illustrated in Fig. 6 includes an 80-bit Y-bar (and chevron) propagation section, a bubble generator for writing information, a steering gate for either recirculating the stored information or erasing it in a bubble annihilator, and a chevron-type 5X bubble expander for a PMR probe. A dummy PMR probe (with dummy chevrons) is also included for cancellation of common-mode noise.

Stack construction

Fig. 4 shows two arrangements of layers on a bubble memory chip, including bubble material, substrates, conductors, and permalloy circuits.

Many such chips may be stacked in a memory module, which also includes a bias magnet and drive coils, as shown schematically in Fig. 10. For example, a memory module may be constructed using garnet-film chips, 250×250 mils in size. With 6-μm bubbles, each such chip contains ~10^5 bits. Four such chips may be assembled on a plane (ceramic substrate or P.C. board), with planes stacked on 50-mil centers. Ten such planes would go into a module, which would thus have 40 chips, or 4×10^6 bits. The active volume of such a module would be 0.5×0.5×0.5 in. With a bias magnet and driving coils, as shown in Fig. 10, the complete module would have a volume of 1.2×1.2×1 = 1.44 in.³ and weigh ~100 g.

The bias magnets have to provide a steady magnetic bias field of 30 to 60 Oe, depending upon the bubble material. Either Barium Ferrite or Alnico magnets may be used to provide the bias field. The bias magnets, together with a return path, provide a magnetic shield for the module.

Orthogonal driving coils provide a rotating magnetic field of 20 to 30 Oe. For high frequency operation (1 MHz or higher), the coils have to be designed to minimize the requirements on the driver circuitry. Computer programs have been written to design coils for this purpose. Two intersecting solenoidal coils, as shown in Fig. 10, provide the largest volume of uniform field for the smallest coil inductance. The required fields for 1-MHz operation can be obtained from drivers supplying ~1.5 A at 50 V. Resonating the coils

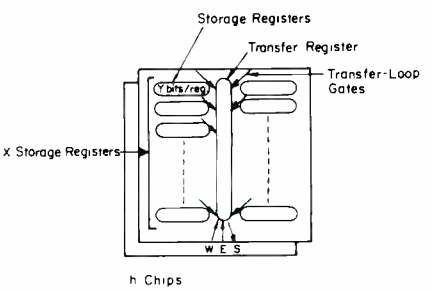

Fig. 11—Recirculating transfer loop system chip design.

with a capacitor can provide drives at even higher fields and lower back voltages.

Fig. 11 illustrates schematically one possible chip layout in the above memory module. Data are stored in storage loops, and transferred in and out of the memory via a central transfer loop. Only one bubble generator (for writing), bubble sensor (for reading), and bubble steerer-annihilator (for clearing) need be provided per chip. This design thus minimizes the number of connections and external circuitry, at the cost of a somewhat longer access time (approx. 100 μs to 1 ms). Many other chip layouts have been proposed and analyzed to meet particular design requirements. Fig. 12 shows a simplified block diagram of a possible system design with 10^9 bits capacity.

Bubble materials

The key to developing bubble devices is the ability to make large, uniform platelets or films of single crystal magnetic materials with few defects. The bubble materials presently being studied are the rare earth orthoferrites: $RFeO_3$ and the rare earth iron garnets: $R_3Fe_5O_{12}$, in which substitutions for the rare earth ion and the iron ion are sometimes appropriate.

Orthoferrites

Orthoferrites[9] have been grown from *Pb* fluxes, and by the floating zone technique. The latter method appears more promising and is currently being emphasized. A floating zone system has been built and orthoferrite boules up to 0.5 in. in diameter have been grown.

The orthoferrites $YFeO_3$ and $Sm_{.55}Tb_{.45}FeO_3$, supporting operating bubble diameters d of approximately 3 mils and 1 mil respectively, have been prepared by both growth techniques. They are used in test devices, such as those described in the previous section.

Orthoferrites of the type $Nd_xPr_{1-x}FeO_3$, $Sm_xPr_{1-x}FeO_3$ and $Sm_xLa_{1-x}FeO_3$ which have low birefringence have been also prepared by both the flux and the floating zone techniques.[10,11] These materials look promising for magneto-optic devices where bubbles are detected optically by the Faraday rotation of transmitted light. Useful bubble diameters as small as 3 mils are realizable in some of these materials.

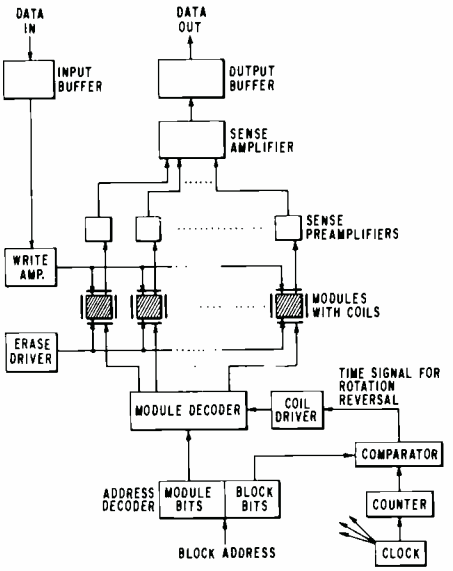

Fig. 12—Simplified block diagram of a sample system design.

Platelets of orthoferrite for use in devices are prepared by cutting slices from a bulk crystal which has been x-ray aligned, thinning the slices with a diamond lap, and polishing them with commercially available colloidal silica (Quso). Platelets thinner than 0.5 mil have been prepared by this method. To relieve polishing strains, the platelets are annealed in oxygen at about 1150°C for more than two hours. The platelets are then examined for imperfections and used in device testing.

Garnets

Two approaches are under development for the preparation of garnet films for bubble devices. These are: liquid phase epitaxy (LPE), and chemical vapor deposition (CVD). In both approaches, a magnetic garnet film is formed on top of a non-magnetic garnet substrate.

The non-magnetic garnet substrate, typically $Gd_3Ga_5O_{12}$, usually referred to as *GGG*, is cut from a Czochralski grown boule. The substrate is polished and one surface is Quso-finished to remove all work damage.

In the LPE process, the substrate is dipped into a supersaturated solution, of the desired magnetic garnet, *e.g.*, $Eu_1Er_2Ga_{0.7}Fe_{4.3}O_{12}$. Epitaxial growth at ~920°C occurs at a rate of approximately 1 μ/minute or typically about 10 to 20 minutes for a 10-μ-thick layer.

In the CVD process, the desired magnetic garnet constituents, *e.g.*, $Y_3Fe_{5-x}Ga_xO_{12}$, for x in $0.9<x<1.2$, are transported in a reactor tube by halogen gases to react and form the garnet phase on top of the substrate. Typical deposition temperature is 1200°C, and deposition rate is 0.1 μ/minute.

A prerequisite for the formation of bubble domains is the existence of a uniaxial magnetic anisotropy. Orthoferrites which are orthorhombic, have a large, uniaxial magnetic anisotropy. In the case of garnets, their cubic symmetry leads to four equivalent easy axes of magnetization. Certain magnetic garnets, when grown at temperatures below 1000°C, display a large uniaxial anisotropy in addition to their cubic anisotropy.[12,13,14] This is referred to as growth induced anisotropy. Alternatively, a uniaxial anisotropy may also be induced by the application of stress. This is referred to as strain induced anisotropy.

For the CVD process, the high growth temperature permits strain anisotropy only. For the LPE process, films with both types of anisotropy have been successfully prepared.

Garnet films capable of supporting densities in excess of 10^6 bubbles per square inch have been grown. The bubble domain mobility in these films is consistent with data rates in excess of 1 Megabit per second in a single channel shift register configuration. An operating temperature range of 0° to 50°C seems feasible, assuming that the bias field is temperature compensated. The storage temperature range (non operating) without loss of data is wider.

Conclusions

The bubble technology, especially that based on the use of liquid-phase-epitaxial garnet films, is simple and involves only one high temperature processing step, viz: the growth of the garnet film. The remaining steps are performed at near room temperature and utilize standard deposition and photolithographic techniques. The technology is both versatile and flexible. It can be used to realize storage, switching, and logic devices. These devices can be realized on the same chip with all fabrication steps being compatible.

For the bubble memory chips considered to date, *e.g.*, a storage register that includes a write generator, bubble annihilator, steerer, and sensor, at most three metallization-photofabrication steps are involved in laying down the permalloy and conductor patterns. For some of the contemplated chips, only two metallization-photofabrication steps may be necessary. In addition to these metallization-photofabrication steps, deposition of an SiO_2 spacer layer (or some other insulating layer) on top of the epitaxial garnet layer is needed.

In general, the definition required in the fabricated patterns is related to the bubble size. The smallest dimension to be realized by photofabrication in a bubble device is approximately one half to one third the bubble diameter. Thus, for a storage density of 10^6 bits per square inch, the required bubble diameter is approximately 0.3 mil, and the smallest dimension to be resolved in the photolithography is 0.15 mils. Perfection in the patterns for propagating bubbles is not essential for reliable operation. However, some of the other components in the system, *e.g.* logic gates, or bubble sensors, may require perfection in the photofabricated patterns to permit wide operating margins. Normally, these devices have minimum dimensions that are on the order of a bubble diameter as opposed to those required for a propagation pattern.

Many different bubble mass memory system organizations have been conceived and discussed in the literature. Some of these organizations utilize bubble propagation paths arranged in minor loops that are coupled to a major loop by means of bubble logic gates. These configurations are aimed at attaining a large-capacity block-oriented random-access memory with short access time to the blocks.

We have considered such systems organizations and carried out a preliminary design based on the use of garnet films that can support 6-μm-diameter bubbles. With present stack construction techniques, the module capacity is 4×10^6 bits in a volume of less than 2 cubic inches including drive coils and a set of permanent magnets for the bias field. The bit rate in such a memory is determined by the frequency of the rotating magnetic field multiplied by the number of parallel channels. For operation at a frequency of one MHz, the total power dissipation under continuous operating conditions is 20 W. For this preliminary design, the number of connections per chip could be as few as five with possibly ten being needed to avoid ground loops.

Access time to a block of 10^3 bits is on the order of 10^{-4} seconds. The operating temperature range for such a memory (based on the extrapolated temperature characteristics of the storage material) can be made fairly wide, *e.g.*, ±25°C around room temperature.

Possibly the largest application for bubble memories is replacement of electromechanical storage devices such as magnetic drums and head-per-track discs. Other possible system applications that are being considered at various industrial laboratories include telephone repertory dialers in which all the required operating power is derived from the telephone line. Very long shift registers, on the order of 10^6 to 10^7 bits, with one input and one output circuit, that are compact and can operate at very low power levels and do not require stand-by power (non volatile), are under consideration for replacement of tape recorders for special purpose applications.

Character recognition algorithms exist in which identifying parameters are derived by introducing a coordinate transformation in the matrix representative of a character. This coordinate transformation is easily produced with a set of input and output transducers geometrically positioned along the edges of a bubble device. Another application that is being investigated is the use of bubble devices as scan converters.

For digitized video signal processing, storage of a single frame is considered desirable. A bubble store is possibly the most economical approach for realizing such a system. Similarly in the case of terminals with video display capabilities, a refresh store is required. A bubble device is possibly compatible with this requirement.

Acknowledgments

The authors wish to acknowledge the contributions of J. Druguet, C. Horak, L. Lucas, R. Noack, S. Schor, and T. Ward to the experimental work. I. Gordon, R. Novak and S. Bolin supplied many of the crystals and films used for the experimental work.

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Books by RCA authors

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Space simulation

Balzer

Lake

Daniel L. Balzer | Ralph J. Lake (contributors)
Astro-Electronics Division
Princeton, New Jersey

This volume was developed from papers presented at the Sixth Space Simulation Conference held in New York City in May 1972. The technology covered encompasses all aspects of simulating the space environment and the effects of this environment upon man and matter. Much of this technology is applicable to ecological studies and to the development of methods to control pollution of the environment. The book contains full or abbreviated versions of papers on a range of topics, which include High Energy Light Sources, Contamination, Thermal Techniques in Solar Simulation and Radiation, Thermal Control Materials, Spacecraft Tests and Test Facilities, Novel and Unique Facility Utilization, Ablative Reentry Materials, Predictive Testing, Physical and Mechanical Properties, Computer Simulation, Mass Spectrometry and Vacuum Measurements, and Solar Constant and Solar Simulation Testing. Also included are two "standards," Recommended Practice for Solar Simulation for Thermal Balance Testing of Spacecraft, and Engineering Standards for the Solar Constant and Air Mass Zero Solar Spectral Irradiance. Messrs Balzer and Lake contributed the paper on "Low-g Simulation Testing of Propellant Systems Using Neutral Buoyancy." *(Published by NASA Scientific and Technical Information Office, Washington, D.C., 1972 (NASA SP-298). Available from Supt. of Documents, U.S. Government Printing Office, Washington, D.C. 20402; 1071 pages.)*

Daniel L. Balzer received the BSCE from Montana State University in 1958. He joined RCA in 1970 in his current position as Manager, Propulsion Systems, at the Astro Electronics Division. In this capacity he is responsible for the analysis and design of spacecraft propulsion subsystems and the development of propulsion related technology for existing and future spacecraft applications. Prior to joining RCA he was associated with the Martin Marietta Corporation, specializing in studies of low gravity propellant behavior, and the Rocketdyne Division of North America Rockwell, gaining experience in all aspects of rocket propulsion systems. He is a member of AIAA.

R. J. Lake of the Propulsion Systems Group at the Astro-Electronics Division received the BSME from City College of New York in 1969. Mr. Lake joined RCA upon graduation and has been involved with spacecraft propulsion system preliminary design. In addition he has performed as project engineer on research and development programs involving capillary propellant management techniques and various phases of advanced propulsion technology. Mr. Lake has authored or co-authored several technical publications and patent disclosures in the field of spacecraft propulsion technology.

Phase-locked and frequency-feedback systems

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RCA Globcom
New York, New York

This book discusses the theory and design of phase-locked and frequency-feedback systems with special emphasis on applications in low-threshold FM communications. It begins with a brief review of the theory of noise and linear systems and then discusses system components with emphasis on limiter-discriminator operation. This is followed by chapters on the principles of frequency-modulation feedback and the phase-locked loop. The design of these systems is then covered in detail with inclusive examples covering the above-threshold, threshold-limited, and the distortion-limited regions. The book also provides in-depth treatments of advanced systems, such as compound and multiple loops, and extended range phase detection techniques. The application of phase-locked loops and the threshold theory to digital FM demodulation is then discussed along with a number of other applications for the phase-lock principle. The book concludes with a chapter on testing and evaluation of the loops, loop components, and the systems. An extensive bibliography on all phases of the subject covering the years 1932 through 1970 of papers and reports is appended. Much of the theory and techniques discussed in the book were developed while the authors were with the Advanced Communications Laboratory, RCA Communications Systems Division, DEP, in New York City. Intended primarily for electrical engineers in satellite and space communications, commercial and military communications, instrumentation, telemetry, data communications, and control, this book is also suitable as a graduate level textbook in electrical engineering. *(March 1972; 412 pp.; Academic Press, N.Y.; price, $19.50)*

Dr. Jacob Klapper received the BEE from the City College of New York in 1956, the MSEE from Columbia University in 1958, and the Eng ScD on a David Sarnoff Fellowship at New York University in 1965. He has the PE license in New York State and the PA license from the U.S. Pat. Office. From 1956 to 1959 he was a Lecturer in Electrical Engineering at the City College of New York. From 1959 to 1960 he was a Project Engineer with the Federal Scientific Corporation, working on spectrum analysis and related problems. Concurrently, from 1957 to 1960 he was a Staff Engineer and Consultant to the Electronics Research Laboratories of Columbia University doing research on speech synthesis and filtering. Dr. Klapper joined the Advanced Communications Laboratory of RCA in 1960. While with this laboratory, he twice won the David Sarnoff Fellowship. Dr. Klapper joined Newark College of Engineering in 1967 where he is now Professor of Electrical Engineering.

John T. Frankle received the BSEE in 1958 from the Massachussetts Institute of Technology and the MSEE in 1964 from the Polytechnic Institute of Brooklyn; while at the Polytechnic he held, in succession, a Teaching Fellowship and Research Assistantship. From 1960 to 1968, while a Member (and later Senior Member) of the Technical Staff at the Advanced Communications Laboratory of the RCA Defense Electronic Products Division, Mr. Frankle was responsible for research and development in the areas of advanced FM demodulators, electronic countermeasure, and digital data transmission. From 1968 to 1970, he was a Member of the Technical Staff (Acting Group Leader) at the Bayside Research Center of General Telephone and Electronics Laboratories where he was responsible for research projects in automatic speech recognition, ultrasonic acoustical communications, and facsimile. In 1970, Mr. Frankle returned to RCA and is presently a Senior Engineer in the Engineering Department of RCA Global Communications where he is actively engaged in the RCA Videovoice development project.

Topics in solid state and quantum electronics

Coulton

Wojtowicz

Martin Caulton | Peter J. Wojtowicz (contributing authors)
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This book, edited by W. D. Hershberger of the University of California at Los Angeles, is based on a statewide lecture series sponsored by UCLA in March, 1970.

Dr. Caulton contributed Chapter 11, "Microwave Integrated Circuits," which presents a survey of microwave integrated circuits. The types of integration, the circuits forms, and the material technology (substrates, conductors, dielectrics, and resistors) are described. A discussion of circuit design and performance is followed by fabrication techniques. Some circuit techniques particular to microwave integrated circuits are developed. Examples of circuits are presented but no discussion of active devices. Throughout, the attempt is to point out the areas in which MIC technology differs from that pertaining to lower-frequency circuits.

Dr. Wojtowicz contributed Chapter 12, "Magnetic Materials" which emphasizes *materials*, their magnetic and other physical properties, and the phenomena on which new devices and systems are likely to be based. The discussion centers on those materials that offer the possibility of optimizing the performance of devices and systems utilizing magnetic phenomena. The chapter is divided into three independent sections, describing magneto-optic materials, materials for use in domain-wall devices, and future trends in magnetic material development. The last section emphasizes materials in which strong interactions between the magnetism and other physical properties exist; the magnetic semiconductors and materials for the photomagnetic effect are featured. *(John Wiley and Sons, Inc.; New York, London, Sydney, Toronto; 1972; 506 pp., $23.50)*

Dr. Martin Caulton pursued his undergraduate and graduate studies in physics at Rensselaer Polytechnic Institute, completing his doctoral research in high-energy nuclear physics under a fellowship at Brookhaven National Laboratories in 1954. He pursued post-doctoral work as a Fulbright scholar at the Imperial College of Science and Technology, University of London. A member of the technical staff (1955-1958) at Bell Telephone Laboratories, Murray Hill, N.J., he worked on low-noise traveling wave tubes and aided in the achievement of significantly lower noise figures using positively-biased electron guns. From 1958 to 1960 he served in the Physics Department at Union College, Schenectady, New York, and co-authored the senior-graduate textbook, *Physical Electronics*. At RCA Laboratories, he experimentally demonstrated (1961) and quantitatively verified (1965) the existence of Landau damping of waves in multivelocity electron beams and plasmas. In 1962 he served as a consultant on traveling-wave tubes with the Relay satellite program. He contributed to the achievement and verification of transistor power beyond the cutoff frequency, utilizing the collector-base capacitance as a parametric frequency multiplier. Since 1966 he has helped to establish a laboratory and the technology for the fabrication of microwave integrated circuits, and was the recipient of an RCA Laboratories achievement award for this work in 1968. Dr. Caulton is also adjunct Professor of Electrical Engineering at Drexel University. He is a member of Sigma Xi, the American Physical Society, the American Association of Physics Teachers, and the IEEE.

Dr. Peter J. Wojtowicz received the BSc in chemistry (with highest honors) from Rutgers University in 1953. He received the MS in chemistry in 1954 and the PhD in physical chemistry in 1956 from Yale University. He was a National Science Foundation Predoctoral fellow while at Yale, 1953-56. Dr. Wojtowicz joined the RCA Laboratories in 1956. He is a Member of the Technical Staff of the Physics and Chemistry of Solids Group of the Physical Electronics Research Laboratory. His research effort while at RCA has been directed chiefly toward the theory of magnetic materials including the quantum and statistical mechanics of the thermal, structural, and magnetic properties of these substances. His recent work involved the statistical mechanics of magnetic interactions and phase transitions. He is currently engaged in the theory of granular ferromagnetic metals. Dr. Wojtowicz is the recipient of two RCA Laboratories Achievement Awards for the years 1962 and 1966. He is a fellow of the American Physical Society and a member of Sigma Xi and Phi Beta Kappa.

Lasers

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In Lasers, edited by A. K. Levine and A. DeMaria, Dr. Kressel contributed Chapter 1, "Semiconductor Lasers". This chapter concentrates on developments in semiconductor lasers since 1967. Although diode lasers receive most of the attention in this chapter, a review of the state of the art in electron beam and optically pumped semiconductor lasers is also given. However, no attempt was made to cover these subjects exhaustively. *(Marcel Delker; New York; 1971; 384 pp; price $22.50.)*

Dr. Henry Kressel received the BA in 1955 from Yeshiva University, the MS in 1956 from Harvard University, the MBA in Industrial Management and the PhD in Materials Science and Metallurgy from the University of Pennsylvania in 1959 and 1965, respectively. From 1959 to 1963 and from 1965 to 1966, he was with the Solid State Division where he worked initially on the development of high frequency silicon transistors and later supervised a group responsible for the development of high power microwave diodes. From 1963 to 1965 he was a David Sarnoff Fellow at the University of Pennsylvania. He transferred to the RCA Laboratories, Princeton, N.J., in 1966 and became Head of the Semiconductor Optical Devices Research group in 1969. He pioneered in the field of (AlGa)As-GaAs heterojunction devices and has been actively engaged in the study of luminescent process in various III-V compound materials. He is the recipient of three RCA Achievement Awards. Dr. Kressel is a member of the IEE, the American Physical Society and Sigma Xi.

Conductors and Semimetals

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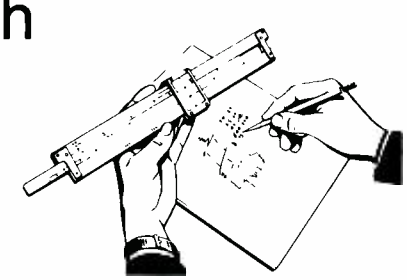
In *Conductors and Semimetals*, edited by R. K. Willardson and Albert C. Beer, Drs. Enstrom and Kressel collaborated with L. Krassner on Chapter 10, "High Temperature Power Rectifiers of $GaAs_{1-x}P_x$." The chapter describes design considerations of high temperature $GaAs_{1-x}Px$ rectifiers, the materials preparation techniques that have yielded large-area junctions relatively free of imperfections affecting electrical behavior, and, finally, the detailed fabrication processes. The design and packaging considerations are general in their application to materials. The detailed expitaxial fabrication technology is more specific in its application to $GaAs$ or $GaAs_{1-x}Px$ devices. *(Academic Press, Inc.; New York and London; 1971; 371-746 pp; price approximately $20-25).*

Dr. Donald Enstrom received the SB, SM, and ScD in metallurgy from the Massachusetts Institute of Technology in 1957, 1962 and 1963, respectively, and has had extensive experience working on various materials. From 1957 to 1960, he worked at Union Carbide and Nuclear Metals, Inc., on materials for high temperature oxidation resistance and nuclear fuel elements, respectively. At RCA Laboratories, he was instrumental in making Nb-Sn ribbon a highly successful high-field magnet material. More recently, Dr. Enstrom has worked on the vapor phase synthesis and characterization of GaAs and GaAs-GaP alloys for high power rectifiers and solid-state microwave oscillators, and on the vapor-growth of GaAsInAs alloys for infra-red sensitive negative electron affinity photocathode applications. Dr. Enstrom is a member of Sigma Xi, AIME, the American Physical Society, and the Electrochemical Society.

Engineering and Research Notes



Photomultiplier sensors with a continuously variable field of view

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Rapid acquisition of point sources in space navigation requires sensor scanning with a fairly large instantaneous field of view. Once the point source is acquired, it may be tracked but accurate tracking requires a narrow field of view. Sandercock[1] describes a method whereby the active photocathode area of a photomultiplier may be made very small. This method may be used to produce a variable field of view suited to the requirements of both acquisition and tracking. The low photomultiplier track count rate, described by Sandercock, is especially attractive, and should allow the design of an extremely sensitive and versatile star tracker using a normal photomultiplier.

Tracking problem

Navigation in space often requires the use of star-tracking sensors. Detection of satellites, space debris, and subsequent rendezvous are related tasks requiring rapid search and acquisition and subsequent optical tracking. Active illumination may

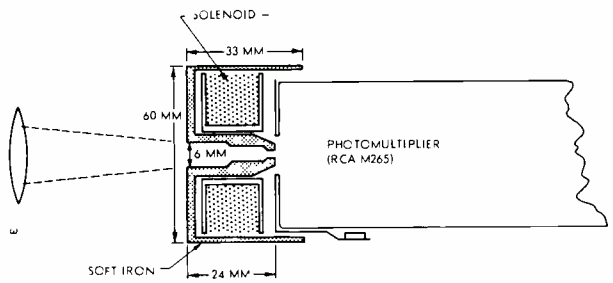

Fig. 1—Sensor description.

be used for short-range detection and ranging. Detection against a space background of faint sources often requires recognition of single photoelectrons, hence a sensor having a low background count is required.

Description of sensor

Construction of the active area of a photomultiplier photocathode, as described by Sandercock[1] is accomplished through using an axial coil mounted in front of the photocathode (Fig. 1). The fringe field produced by the coil and soft iron core deflects any electrons which are not moving axially. Dark current electrons originating outside the central area are reflected and do not reach the electron multiplier. When the solenoid current is high, only a very small central area of the photocathode can cause an input to the electron multiplier. As the current is reduced, this area gets successively larger. The effective field of view of a sensor using this arrangement may thus be changed by changing the current through the solenoid.

Tracking

To perform the tracking function, the instantaneous field of view must not only be small, but the direction in which the star image is off center must be determined. This may be done by using field deflection coils arranged to deflect the axial field slightly in the X and Y directions. Application of a suitable current 90° out of phase in these coils will move the sensitive spot in a small circular path. Phase comparison of the photomultiplier output with the deflection current will yield a signal input for the X and Y tracking devices, so that the star image is steered toward the center of the photocathode.

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Transformerless full-wave rectifier

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United States Patent No. 3,573,645 describes a transformerless phase-splitter integrated circuit as shown within the dotted line in Fig. 1. When the diode-connected transistors Q1, Q2 are made with much larger base-emitter junction areas than transistors Q3, Q4, Q5, the common-emitter amplifier transistor Q5 conducts on positive portions of the AC source that is coupled to its input terminal; and the common-base amplifier transistor Q3 conducts on negative portions. The current gain of the common-base amplifier transistor Q3 is unity during full conduction. The current gain of the common-emitter amplifier transistor Q5 during full conduction is also unity because of the diode-connected transistor Q4 connected in parallel with its base-emitter junction. Each of the transistors Q3 and Q5 accordingly provide half-wave rectified currents in response to the AC input signal, at equal current gains. These half-wave rectified currents when summed and applied to a load resistor R2 provide a full-wave rectified voltage at the output, having a peak amplitude related to the peak amplitude of the input signal at the AC source by the ratio of the resistance of resistor R2 to that of resistor R3. This circuit is useful in deriving the absolute value of analog or ternary digital signals.

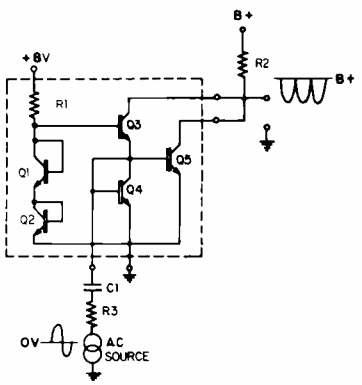

Fig. 1—Transformerless phase-splitter integrated circuit.

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Pen and Podium

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electromagnetic field theory, quantum mechanics, basic particles, plasmas, solid state, optics, thermodynamics, solid mechanics, fluid mechanics, acoustics.

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production techniques for materials, devices & equipment.

CABLE/CONNECTORS Used in AEGIS AN/SPY-1 Radar System, Flat Conductor—B. R Schwartz (M&SR, Mrstn) Flat Conductor Cable Application Symp. MSFC, Huntsville, Alabama; 10/10-12/72

CABLING DESIGNS for Phased Arrays—I D Kruger L Jurkiewicz (M&SR Mrstn) FCC Symp at MSFC; 10/10-12/72

LSI PHOTOLITHOGRAPHY - EQUIPMENT Process and Inspection (abstract)—R. A. Geshner (Labs, Pr) Institute for Graphic Communications Ipswich Ma ;) 11/72

PACKAGING, Military/Aerospace—J S. Furnstahl (ASD, Burl) *Packaging and Production Magazine*; 8/72

TIN SENSITIZER Solutions, The Effectiveness of —N. Feldstein, J. A Weiner (Labs, Pr) *Plating*, Vol. 59, pp 140-141; 2/72

175 Reliability, Quality Control & Standardization
value analysis, reliability analysis, standards for design & production

CONNECTOR STANDARDIZATION Effectiveness for the AEGIS Program—H. Plofker, W Alexander, B. Schwartz (M&SR, Mrstn) Fifth Annual Connector Symp Cherry Hill, N.J.; 10/21/72

OSHA and the Research Laboratory—E. V. Fitzke (Labs, Pr) Standards Engineers Soc Annual Conf., Boston, Mass.; 9/25/72

PRODUCIBILITY for Aerospace Electronics—S Patrakis, F. P. McGurk (ASD, Burl) Presented at WESCON Mtg., Los Angeles, Calif.; 9/72

STANDARD PACKAGING for AN/SPY-1 Radar Signal Processor, Micropak—A. A. Blatz (M&SR, Mrstn) *Electronic Packaging and Production*; 8/72

180 Management & Business Operations
organization, scheluling, marketing, personnel.

CONTROL SYSTEMS, Management—L. M. Krugman (CE, Ind) IEEE Engineering Management Technical Meeting, Indianapolis, Indiana; 10/18/72

DECIDE—A New Management Tool for the Systematic Evaluation of Project and Business Risks—M. W. Buckley, Jr. (M&SR, Mrstn) Fourth Annual Seminar/Symp. Project Management Inst. 10/18-21/72; Philadelphia, Pa.

PERFORMANCE, Measuring Business—H. N. Garber, S. A. Kitchener, A. K. Nigam (Labs, Pr) Operational Research Soc., (UK), Birmingham, England; 9/72

PROJECT MANAGEMENT—Future Developments—M. Buckley (M&SR, Mrstn) AMA Seminar—N.Y.C. "Basic Project Management Planning, Scheduling and Control", 8/24/72

SERIES 200 MATERIALS, DEVICES, & COMPONENTS

205 Materials (Electronic)
preparation & properties of conductors, semiconductors, dielectrics, magnetic, electro-optical, recording & electromagnetic materials.

ALKALI-CONTAINING GLASSES, Electrode "Polarization" in—D. E. Carlson, K W. Hang, G. F. Stockdale (Labs, Pr) *J. of the American Ceramic Society*, Vol 55, No. 7, pp. 337-341; 7/72

GaAs and (Al Ga) As on Gap, Solution Growth and Characterizaton of—M. Ettenberg, S. H. McFarlane, S. L. Gilberg (Labs, Pr) 4th International Symp. on Gallium Arsenide and Related Compounds, Boulder, Colorado; 9/25-27/72

GaN, Luminescence in—J. I. Pankove (Labs, Pr) Symp. on the Physics and Technology of Seminconductor Light Emitters and Detectors, Bari, Italy; 9/4-10/72

GaN, Luminescence in—J. I. Pankove, E. A. Miller, J. E. Berkeyheiser, P. E. Norris (Labs. Pr) 4th Int'l Symp. on GaAs and Related Compounds, Boulder, Colorado; 9/25-27/72

GaP on Insulating Substrates, Epitaxial Growth and Characterization of—C. C. Wang, S. H. McFarlane III (Labs, Pr) *J. of Crystal Growth*, Vol. 13/14, pp. 262-267; 1972

GARNETS, Growth Induced Anistropy in —A. Akselrad (Labs, Pr) Bubble Memory Technology Review, Washington, D.C.; 9/27-28/72

In Ga P ALLOYS, Influence of Gas-Phase Stoichiometry on the Properties of Vapor-Grown—R E. Enstrom, C. J. Nuese, V. S. Ban, J R Appert (Labs, Pr) 4th Int'l Symp. on Gallium Arsenide, Boulder, Colorado; 9/25-27/72

PZT FILMS, RF Diode Sputtered—T. Hattori, T. Oka, F. Okamoto (Labs, Pr) Mtg. of Japan Applied Physics, Hokkaido Univ., Japan; 9/29-10/1/72

YTTRIUM, EUROPIUM AND GADOLINIUM, Atomic Absorption Spectrometric Determination of—K. Ametani, F. Okamoto, Y. Wada, S. Harada (Labs. Pr) 21st Annual Mtg. of Japan Soc. of Analytical Chemistry, Miyagi, Univ. of Sendai, Japan; 9/13-15/72

ZnO FILMS by Sputtering, Preparation of Oriented—H. W Lehmann, R. Widmer (Labs. Pr) German Soc. Mtg. for Crystal Growth, Freiburg, Germany; 9/72

210 Circuit Devices & Microcircuits
electron tubes & solid-state devices (active & passive), integrated, array, & hybrid microcircuits, field-effect devices, resistors & capacitors, modular & printed circuits, circuit interconnection, waveguides & transmission lines.

ACOUSTIC SURACE WAVE DEVICE Performance in Microwave Communications Systems—G. D. O'Clock, D. A. Gandolfo, J. R. Loose (EASD, Van Nuys) Ultrasonics Symp. Digest; 10/72

ELECTRON EMITTERS of (AlGa) As-GaAs, Heterojunction Cold-Cathode—H. Kressel, H. Schade, H. Nelson (Labs, Pr) Symp. on the Physics and Technology of Semiconductor Light Emitters and Detectors, Bari, taly; 9/4-10/72

IMPATT DIODE Noise Properties, A Comparative Study for—P. A. Levine, V W. Chan (Labs, Pr) *Proc. of the IEEE*, Vol 60, No. 6, pp. 745-746; 6/72

MNOS MEMORY TRANSISTOR Characteristics and Failure Mechanism Model, Degradation of—J. W. Tuska, M. W Woods (Labs, Pr) GOMAC Conf., San Diego, Calif.; 9/72

SWITCH, L-Band High Power Silicon PIN Diode—V. Stachejko (M&SR, Mrstn) *Proc. of the IEEE*; 9/71

215 Circuit & Network Designs
analog & digital functions in electronic equipment: amplifiers, filters, modulators, microwave circuits, A-D converters, encoders, oscillators, switches, masers, logic networks, timing & control functions, fluidic circuits.

OSCILLATORS, Improved Diode and Circuit Procedures for High-Efficiency S-Band—A. S. Clorfeine, H. J Prager R. D. Hughes (Labs, Pr) *Proc of the IEEE*, Vol. 60, No. 6; 6/72; pp. 729-730.

POWER-CONTROL Circuits, Adaptive Thyristor—J H McCusker, S. S. Perlman (Labs, Pr) *IEEE J of Solid-State Circuits*, Vol. SC-7, No. 4, pp. 282-287; 8/72

225 Antennas & Propagation
antenna design & performance feeds & couplers, phased arrays, radomes & antenna structures, electromagnetic wave propagation scatter, effects of noise & interference.

ANTENNA, A New Circular Polarization TV and FM Panel—O Ben-Dov (CSD, Camden) IEEE Fall Symp.

"BUTTERFLY" ANTENNA at CBKST, Saskatoon—D Macaulay (RCA Ltd., Mont) Mtg. of the Western Association of Broadcast Engineers, 5/2-4/72; Regina, Sask.

GROUND CONDUCTIVITY Considerations —C. A. Martin (Labs, Pr) IEEE Int'l Conf. on Engineering in the Ocean Environment, Newport, R. I.; 9/13-15/72

PHASED ARRAYS, A Broad-Band, Wide-Angle Scan Matching Technique for Large Environmentally Restricted—J. Campbell/B Popovich (M&SR, Mrstn) IEEE Trans.; 7/72

240 Lasers, Electro-Optical & Optical Devices
design & characteristics of lasers, components used with lasers, electro-optical systems, lenses, etc. (excludes: masers).

CHARGE-COUPLED IMAGER for L TV—W. F. Kosonocky, J. E. Carnes (Labs, Pr) Electro-Optics Systems Design Conf., NYC.; 9/12-14/72

He-Ne LASER LIGHT in GaP Junctions Outside the Waveguide Regime, Modulation of—H. P. Klenknecht (Labs, Pr) European Solid State Device Research Conf., Lancaster, England; 9/72

LASER MODULATORS, An Automatic Optical Bias Control for—A. Waksberg, J Wood (RCA Ltd., Mont) *The Review of Scientific Instruments*, Vol. 43, No. 9; 9/72

METAL VAPOR Lasers CW—K. G. Hernqvist (Labs, Pr) 1st European Electro-Optics Technical Conf. Geneva, Switzerland; 9/12-15/72

245 Displays
equipment for the display of graphic, alphanumeric, & other data in communications, computer military, & other systems, CRT devices, solid state displays, holographic-displays, etc.

IMAGE QUALITY Evaluation in High-Contrast Processes—H. E. Haynes (Corp. Staff, Camden) SPSE Symp. New Methods for Converting Original Copy to Plate, Washington, D.C.; 10/25-28/72

250 Recording Components & Equipment
disk, drum, film, holographic & assemblies for audio, image, & data systems.

LASER SIGNAL Recording, High Dynamic Range—J. A. Calabria (ATL, Camden) Electro-Optical System Design Exhibition & Conf.; 9/12-14/72; New York

255 Audio Components & Applied Acoustics
microphones, loudspeakers, earphones, etc., sound transmission & control, ultrasonic equipment (excludes: sonar & audio recording equipment).

LOUDSPEAKERS, Gradient—H. F. Olson (Labs, Pr) Audio Engineering Soc., NYC; 9/12-15/72

REPRODUCED ACOUSTIC FIELD, A Relation Between the Number of Audio Channels and the Angular Resolution of a—J. J. Gibson (Labs, Pr) Audio Engineering Soc., Conf., NYC, 9/12-18/72

270 Materials (Mechanical)
preparation & properties of structural, adhesive, protective, hydraulic, & lubricant materials.

PACKAGING, Military Aerospace—J. S. Furnstahl (ASD, Burl) *Packaging and Production*, 8/72

SERIES 300
SYSTEMS, EQUIPMENT, & APPLICATIONS

310 Spacecraft & Ground Support
spacecraft & satellite design, launch vehicles, payloads, space missions, space navigation.

MULTISPECTRAL TV CAMERA, High-Resolution System for ERTS A&B—B. P. Miller (AED, Pr) XXIII Int'l Astronautical Congress, Vienna, Austria; 10/15/72

315 Military Weapons & Logistics
missiles, command & control.

WEAPON SYSTEM, The AEGIS—F. G. Adams (M&SR, Mrstn) Electronics Group, Camden, N.J.; 10/16/72

340 Communications Equipment & Systems
industrial, military, commercial systems, telephony, telegraphy, & telemetry, (excludes: television & broadcast radio).

COMMUNICATIONS, International — An Overview—P. B. Silverman (GlobCom, N.Y.) Wescom/72 Convention Center at Los Angeles; 9/20/72; *Wescon/72 Digest*

COMMUNICATIONS SATELLITES and the International Communications Industry—C. R. Hume, D. S. Bond (AED, Pr) British Interplanetary Society Symp. on Communications Satellites Univ. of Southampton, England; 9/19-20/72

DATA TRANSMISSION over FM Modems and Radio—K. Feher (RCA Ltd., Mont) Midwest Symp. on Circuit Theory; Univ. of Missouri; 5/4-5/72

DIGITAL COMMUNICATIONS, Mobile—An Essential Capability—W. Painter (CSD, Camden) 1972 APCO Conv.; Boston, Mass.

DISTRESS SIGNALLING by Disabled Motorists, A Microwave System for—L. Schiff, H. Staras (Labs, Pr) WESCON Conf., Los Angeles, Calif.; 9/19-22/72

FM BROADCASTING of Panoramic Sound, Compatible—R. M. Christensen, J. J. Gibson, A. L. Limberg (Labs, Pr) Audio Engineering Soc., Conv., NYC, 9/12-18/72

14/12 GHz TRANSPONDER for the Communication Technology Satellite, Design of—V. O'Donovan, Dr. G. Lo, A. B. Bell; C.A.S.I.-A.I.A.A. Mtg., Ottawa; 7/10/72

MICROWAVE SYSTEMS, Hybrid Transmission in—K. Feher, J. E. H. Elvidge (RCA Ltd., Mont) 6th Biennial Symp. on Communication Theory and Signal Processing, Queen's Univ., Kingston, Ont.; 8/28-30/72

345 Television & Broadcast Systems
television & radio broadcasting, receivers, transmitters, & systems, television cameras, recorders, studio equipment, closed-circuit, spacecraft, & special purpose television.

INCIDENTAL PHASE MODULATION of TV Transmitters, or other Circuits, on TV Signals, Effects of—W. L. Behrend (CSD, Camden) IEEE Fall Symp.

TELECINE CAMERA, A Second Generation Color—J. J. Clarke (CSD, Camden) Inst. of Radio & Electronic Engineers Australian National Univ.; Canberra, Australia; 8/28/72

VIDEO MIXING, A Novel Approach to Multi-Channel—J. A. Killough (CSD, Camden) IEEE Fall Symp.

360 Computer Equipment
processors, memories, & peripherals.

BUBBLE DOMAINS, Magneto-Optic Detection of—R. Shahbender (Labs, Pr) Bubble Memory Technology Review, Washington, D.C.; 9/27-28/72

BUFFER MEMORY for Microprograms, Microcache:—A. D. Robbi (Labs, Pr) COMPCON 72, San Francisco, Calif.; 9/12-14/72

COMPUTER SECURITY Management at Walt Disney World—E. D. Wyant (ASD, Burl) 7th Annual Conf., Soc. of Logistics Eng., Long Beach Calif.; 8/21-23/72

HOLOGRAPHIC READ ONLY MEMORY, Card Changeable—P. L. Nelson, R. H. Norwalt (EASD, Van Nuys) Conf. on Laser Engineering and Applications; Washington, D.C.; 5/73

MAGNETIC MEMORIES, A Survey on—J. A. Rajchman (Labs, Pr) *Ferrites: Proc. of the Int'l Conf.*, 7/70; Japan; pp. 409-417

OPTICAL MEMORIES, Promise of—J. A. Rajchman (Labs, Pr) *J. of Vacuum Science and Technology* Vol. 9, No. 4, pp. 1151-1159; 7-8/72

OPTICAL MEMORY Technology—R. D. Lchman (Labs, Pr) Nat'l Science Foundation Workshop on Optical Computing, Pittsburgh, Pa.; 9/14-15/72

365 Computer Programming & Applications
languages, software systems, & general applications (excluding: specific programs for scientific use).

RESOURCE UTILIZATION in a Batch Computer System, Hardware Measurements of—P. M. Russo, A. D. Robbi (Labs, Pr) IEEE Computer Soc. Conf., (COMPCON) San Francisco, Calif.; 9/12-14/72

Author Index

Subject listed opposite each author's name indicates where complete citation to his paper may be found in the subject index. An author may have more than one paper for each subject category.

Dates and Deadlines

As an industry leader, RCA must be well represented in major professional conferences . . . to display its skills and abilities to both commercial and government interests.

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Plan ahead! Watch these columns every issue for advance notices of upcoming meetings and "calls for papers". Formulate plans at staff meetings—and select pertinent topics to represent you and your group professionally. Every engineer and scientist is urged to scan these columns; call attention of important meetings to your Technical Publications Administrator (TPA) or your manager. Always work closely with your TPA who can help with scheduling and supplement contacts between engineers and professional societies. Inform your TPA whenever you present or publish a paper. These professional accomplishments will be cited in the "Pen and Podium" section of the *RCA Engineer*, as reported by your TPA.

Calls for papers—be sure deadlines are met.

Date	Conference	Location	Sponsors	Deadline Date	Submit	To
MAY 15-17, 1973	**1973 Electrical & Electronic Measurement & Test Instrument Conference**	Ottawa, Ontario, Canada	Ottawa Section IEEE	**12/31/72**	**abst sum**	Chairman of Technical Program Committee Dr. Pieter G. Cath Keithley Instruments, Inc. 28775 Aurora Rd. Cleveland, OH 44139
MAY 30-JUNE 1, 1973	**1973 IEEE/OSA Conference on Laser Engineering and Applications**	Washington Hilton Hotel, DC	IEEE Quantum Electronics Council & Optical Society of America	**Immed.** **1/5/73**	**35-wd. abst** **500-wd. sum papers**	Mr. David R. Whitehouse Raytheon Company, LADC 130 Second Avenue Waltham, MA 02154
JUNE 11-13, 1973	**1973 IEEE International Conference on Communications**	Seattle, Washington	Communications Society & Seattle Section of IEEE	**1/1/73**	**ms**	Dr. S. Tashiro, ICC '73 P. O. Box 648 Bellevue, WA 98009
JULY 10-12, 1973	**Joint Space Mission Planning and Executive Meeting**	Denver, Colo.	AIAA/ASME SAE	**1/19/73**	**draft or abst**	James E. Long, 180-400 Jet Propulsion Lab. 4800 Oak Grove Drive Pasadena, CA 91103
JULY 10-12, 1973	**Space Science Conference: Exploration of the Outer Solar System**	Denver, CO	AIAA	**1/29/73**	**drafts or abst**	Rolf Faye-Petersen Martin Marietta Aerospace Mail-No. S8943 Denver, CO 80201
JULY 15-20, 1973	**1973 IEEE Power Engineering Society Summer Meeting and EHV/UHV Conference**	Vancouver, B.C., Canada	S-PE	**2/15/73**	**ms**	D. G. McFarlane British Columbia Hydro & Pwr. Auth., 970 Burrard St. Van 1 B.C. Can.
AUG. 12-18, 1973	**1973 Fifth Pan American Congress of Mechanical, Electrical, & Allied Engineering Branches**	Bogota, Columbia		**12/15/72**	**abst sum**	T. W. Hissey, Manager of Electric Power for Int'l. Operations Leeds & Northrup Co. Sumneytown Pike North Wales, PA 19454
AUG. 13-17, 1973	**1973 Intersociety Energy Conversion Engineering Conference**	Univ. of Penna Philadelphia	AIAA, ACS AIChE, ASME SAE	**1/15/73**	**abst**	Daniel Mager, Technical Program Chairman 8th IECEC, POB 443 Lexington, MA 02173
SEPT. 17-19, 1973	**Petroleum & Chemical Industry Technical Conference**	Regency Hyatt Hotel, New Orleans, LA	S-IA	**5/15/73**	**ms**	R. H. Cunningham Atlantic Richfield Co. POB 2451 Houston, TX 77001
SEPT. 24-27, 1973	**1973 Intersociety Transportation Conference**	Brown Palace Hotel, Denver, CO	Intersociety Comm. on Transportation AEA, AIAA, ASME, EIC, IEEE, ORSA, SAE, SNAME, TIMS	**12/15/72** **4/1/73** **(abstracts for prospective papers will be reviewed and invitations will be extended by February 1, 1973. Abstracts and papers will not be returned)**	**abst** **paper**	ICT Technical Program Chairman, Thomas P. Woll U.S. Dept. of Transportation 400 7th Street, S.W. Room 5408 Washington, DC 20590
OCT. 8-11, 1973	**Annual Meeting IEEE Industrial Applications Society**	Pfister Hotel, Milwaukee, WI	IAS	**3/15/73** **6/1/73**	**abst** **papers**	Technical Papers Chm: Karl F. Hoelzel Allen Bradley Co. 680 East Market St. Room 307 Akron, OH 44304
APR. 1-5, 1974	**IEEE Power Engineering Society Conference on Underground Transmission & Distribution**	Dallas Conv. Ctr. Dallas, TX	S-PE	**3/1/73**	**abst**	N. E. Piccione L I Lighting Co. 175 E. Old Country Rd. Hicksville, NY 11801

Dates of upcoming meetings—plan ahead.

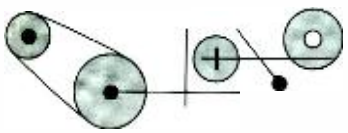
Date	Conference	Location	Sponsors	Program Chairman
JAN. 23-25, 1973	**1973 Annual Reliability and Maintainability Symposium**	Philadelphia, PA		AIAA Editorial Offices 1290 Ave. of the Americas New York, NY 10019
JAN. 23-25, 1973	**Reliability & Maintainability Symposium**	Bellevue-Stratford Hotel Phila., PA	G-R, ASQC, IES, et al	L. R. Webster, Radiation Inc. POB 37, Melbourne, Fla. 32901
JAN. 28-FEB. 2, 1973	**IEEE Power Engineering Society Winter Meeting**	Statler Hilton Hotel, New York, NY	S-PE	J. W. Bean AEP Service Corp., 2 Broadway New York, NY 10004
FEB. 13-15, 1973	**Aerospace & Elec. Systems Winter Convention (WINCON)**	Int'l Hotel Los Angeles, CA	G-AES, L.A. Council	J. M. Wuerth Autonetics 1630 Lindendale Ave. Fullerton, CA 92631
FEB. 14-16, 1973	**Int'l Solid State Circuit Conference**	Marriott Hotel, Phila., PA	SSC Council Phila. Section, Univ. of PA	V. I. Johannes Bell Tel. Labs., Rm. 3E-331 Holmdel, NJ 07733
FEB. 27-MARCH 1, 1973	**Computer Conference (COMPCON)**	San Francisco, CA	S-C	Rex Rice Fairchild Sys. Tech. Div. 974 E. Arques Ave. Sunneyvale, CA 94086
MARCH 5-7, 1973	**Particle Accelerator Conference**	Sheraton Palace Hotel, San Francisco, CA	G-NS, NBS, et al	R. B. Neal, Stanford Linear Accelerator Ctr. Stanford, CA 94035
MARCH 6-8, 1973	**Conf. on Diagnostic Testing of High Power Apparatus in Service**	London, England	IEE, IEEE, UKRI Section	IEE, Savoy Place London W.C. 2R OBL, England
MARCH 7-9, 1973	**3rd Sounding Rocket Technology Conference**	Albuquerque, NM	AIAA	AIAA Editorial Offices 1290 Ave. of the Americas New York, NY 10019
MARCH 19-21, 1973	**Conf. on Optical Storage of Digital Data**	Denver, CO	QEC, S-MAG, OSA	Adam Kozma, Electro-Optics Ctr., Radiation Inc., Box 1084, Ann Arbor, MI 48106
MARCH 19-20, 1973	**Dynamics Specialist Conference**	Williamsburg, VA	AIAA	AIAA Editorial Offices 1290 Ave. of the Americas New York, NY 10019
MARCH 20-22, 1973	**14th Structures, Structural Dynamics and Materials Conference**	Williamsburg, VA	AIAA/ASME/SAE	AIAA Editorial Offices 1290 Ave. of the Americas New York, NY 10019
MARCH 26-29, 1973	**IEEE International Convention (INTERCON)**	Coliseum & Americana Hotel, New York, NY	IEEE	J. H. Schumacher, IEEE 345 E. 47th St. New York, NY 10017
MARCH 28-30, 1973	**Tactical Missile Meeting**	Orlando, FL	AIAA/AOA	AIAA Editorial Offices 1290 Ave. of the Americas New York, NY 10019
APRIL 1973	**Conference on Applications of Aerospace Technology to Medicine**	New York, NY		AIAA Editorial Offices 1290 Ave. of the Americas New York, NY 10019
APRIL 4-6, 1973	**Southwestern IEEE Conference & Exhibition (SWIEEECO)**	Astroworld, Houston, TX	SWIEEECO, Houston Section	W. C. Bean, EE Dept. Lamar Univ., Beaumont, TX 77710
APRIL 9-11, 1973	**Frontiers in Education**	Purdue Univ., Lafayette, IN	G-Education Central Ind. Section ASEE, Purdue Univ.	J. M. Biedenbach Hershey Medical Center Hershey, PA 17033
APRIL 10-13, 1973	**Conf. on Propagation of Radio Waves at Frequencies about 10GHz**	London, England	IEE, IERE, Inst. of Phys. IEE, UKRI Section	IEE, Savoy Place, London W.C. 2R OBL England
APRIL 11-12, 1973	**Joint Railroad Tech. Conf.**	Chase Park Plaza Hotel, St. Louis, MO	S-IA, ASME	Tom Woll, Fed. Railroad, 400 7th St., S.W., Rm. 5408 Washington, DC 20591
APRIL 11-13, 1973	**Conf. on Signal Processing**	Erlange, Fed. Rep. of Germany	IEEE German Section, NTG	W. Schuessler, Inst. fur Nachrictentechnik Univ. Erlangen-Nurnberg, 8520 Erlange, Egerlanstrabe 5
APRIL 16-18, 1973	**Symp. on Applications of Walsh Functions**	Catholic Univ., Washington, DC	G-EMC, NRL Catholic Univ.	H. C. Andrews, Dept. of EE, Univ. of Southern Calif. Los Angeles, CA 90007
APRIL 16-18, 1973	**Computer Network Conference**	Huntsville, AL	AIAA	AIAA Editorial Offices 1290 Ave.of the Americas New York, NY 10019
APRIL 24-27, 1973	**International Magnetics Conference (INTERMAG)**	Washington Hilton Hotel, Washington, DC	S-MAG, Washington, DC Section	J. M. Lommel, Gen'l. Elec. Res. & Dev. Ctr., POB 8 Schenectady, NY 12301

Dates of upcoming meetings (continued)

APRIL 29- MAY 2, 1973	**Offshore Technology Conference**	Astrohall, Houston, TX	TAB Ocean- ography Coor. Comm. et al	J. R. Jackson, Jr. Humble Oil & Refining Co. POB 2180 Houston, TX 77001
APRIL 30- MAY 2, 1973	**Southeast-Con**	Galt House, Louisville, KY	Region 3	R. D. Shelton, Univ. of Louisville, EE Dept. Louisville, KY 40202
MAY 1-2, 1973	**Electron Device Techniques Conference**	United Engrg. Ctr., New York, NY	G-ED	Hayden Gallagher, Res. Labs., 3011 Malibu Canyon Rd. Malibu, CA 90265
MAY 1-4, 1973	**Pulp & Paper Industry Technical Conference**	Jacksonville Hilton Hotel, Jacksonville, FL	S-IA, Jacksonville Section	C. E. Greene St. Regis Paper Co. Gulf Life Tower Jacksonville, FL 32207
MAY 2-4, 1973	**Region Six "Mini-Computers and Their Application"**	Sheraton-Waikiki, Honolulu, Hawaii	Region 6 Hawaii Section	Don Grace, KEMS Inc. 239 Puuhale Rd., Honolulu, HI 96819
MAY 13-17, 1973	**Industrial & Commercial Power Sys. Conference**	Regency Hyatt House, Atlanta, GA	S-IA, Atlanta Section	R. G. Henderson, Georgia Power Co., Ind. Sales Dept., POB 4545 Atlanta, GA 30302
MAY 14-16, 1973	**Electronic Components Conference**	Statler Hilton Hotel, Washington, DC	G-PHP, EIA	W. E. Parker, Airco Speer Elec., Packard Rd. at 47th St., Niagara Falls, NY 14302

Patents Granted

to RCA Engineers



As reported by RCA Domestic Patents, Princeton

Aerospace Systems Division

An Exposure Control Circuit for an Electrically Shuttered Image Tube—D. F. Dion (ASD, Burl.) U.S. Pat. 3689770, September 5, 1972; Assigned to U.S. Government.

Advanced Technology Laboratories

Holographic Multicolor Technique—B. P. Clay (Adv. Tech., Burl.) U.S. Pat. 3695744, October 3, 1972

Astro-Electronic Division

Method of Alloying Two Metals—F. J. Papiano (AED, Htsn.) U. S. Pat. 3690943, September 12, 1972

Apparatus for the Automatic Navigation of a Sailing Vessel—D S. Bond (AED, Htsn.) U.S. Pat. 3691978, September 19, 1972

Nutation Damping in Dual-Spin Spacecraft—K. J. Phillips (AED, Htsn.) U.S. Pat. 3695554, October 3, 1972

Missile & Surface Radar Division

Transmission Line Filter—T. U. Foley (M&SR, Mrstn.) U.S. Pat. 3659232, July, 1972

Printed Circuit Balun—O. M. Woodward (M&SR, Mrstn.) U.S. Pat. 3678418, July, 1972

Flexible and Slidable Waveguide Feed System for a Radiating Horn Antenna—N. R. Landry, R. J. Mason, W. H. Schaedla, W. T. Patton (M&SR, Mrstn.) U.S. Pat. 3698000, October 10, 1972

Communications Systems Division

Automatic Registration of Color Television Cameras—C. L. Olson, R. A. Dischert (G&CS, Cam) U.S. Pat. 3692918, September 19, 1972

Time Delay Circuits—W. R. Walters (G&CS, Cam.) U.S. Pat. 3693030, September 19, 1972

Laboratories

Photocolorable Vacuum Sublimed Xanthene Dye—S. E. Harrison, R. Drake (Labs., Pr.) U.S. Pat. 3690889, September 12, 1972

Electroless Nickel Plating Method—N. Feldstein (Labs., Pr.) U.S. Pat. 3690944, September 12, 1972

Solid State Microwave Heating Apparatus—K. K. Chang (Labs., Pr.) U.S. Pat. 3691338, September 12, 1972

Method and Apparatus for Depositing Epitaxial Semiconductive Layers from the Liquid Phase—D. P. Marinelli (Labs., Pr.) U.S. Pat. 3692592, September 19, 1972

Method of Forming Semiconductor Device with Smooth Flat Surface—F. Z. Hawrylo, H. Kressel (Labs., Pr.) U.S. Pat. 3692593, September 19, 1972

Method of Forming an Epitaxial Semiconductive Layer with a Smooth Surface—V. M. Cannuli (Labs., Pr.) U.S. Pat. 3692594, September 19, 1972

Method of Radio Frequency Sputter Etching—J. L. Vossen, Jr. (Labs., Pr.) U.S. Pat. 3692655, September 19, 1972

Electrostatic Printing—H. G. Greig (Labs., Pr.) U.S. Pat. 3694275, September 26, 1972

Method of Making Light Emitting Diode—H. Nelson (Labs., Pr.) U.S. Pat. 3694275, September 26, 1972

Shottky Barrier Diode—A. N. Saxena (Labs., Pr.) U.S. Pat. 3694719, September 26, 1972

Signal Transfer System for Panel Type Image Sensor—P. K. Weimer (Labs., Pr.) U.S. Pat. 3696250, October 3, 1972

Method of Projection Printing Photoresist Masking Layers, Including Elimination of Spurious Diffraction-Associated Patterns from the Print—E. C. Douglas (Labs., Pr.) U.S. Pat. 3697178, October 10, 1972

Method of Metallizing an Electrically Insulating Surface—N. Feldstein (Labs., Pr.) U.S. Pat. 3697319, October 10, 1972

Character Generator Utilizing a Display with Photochromic Layer—D. R. Bosomworth (Labs., Pr.) U.S. Pat. 3700791, October 24, 1972

Method of Improving Cathodochromic Sensitivity—P. M. Heyman (Labs., Pr.) U.S. Pat. 3700804, October 24, 1972

Deflection and Pincushion Correction Circuit—P. E. Haferl (Labs., Zurich, Switz.) U.S. Pat. 3700958, October 24, 1972

Schottky Barrier Diode and Method of Making the Same—A. N. Saxena (Labs., Pr.) U.S. Pat. 3700979, October 24, 1972

Computer with Probability Means to Transfer Pages from Large Memory to Fast Memory—J. G. Williams (Labs., Pr.) U.S. Pat. 3701107, October 24, 1972

Electronic Components

Cathode Ray Tube Implosion Protection System and Method—A Hildebrants (EC, Marion) U.S. Pat. 3697686, October 10, 1972

Photocathode Comprising Layers of Tin Oxide, Antimony Oxide, and Antimony—R. G. Stoudenheimer, R. P. Dourte (EC, Lanc.) U.S. Pat. 3697794, October 10, 1972

Solid State Division

Variable Tuning Arrangement for a Strip Transmission Line Circuit—A. Presser (SSTC, Pr.) U.S. Pat. 3693118, September 19, 1972

Method for Forming Isolated Semiconductor Devices—R. R. Speers (SSD, Som.) U.S. Pat. 3695956, October 3, 1972

Avalanche Diode—J. M. Assour (SSD, Som.) U.S. Pat. 3696272, October 3, 1972

Method of Making Semiconductor Devices—M. F. Lamorte (SSD, Som.) U.S. Pat. 3697336, October 10, 1972

Signal Generating Circuit Including a Pair of Cascade Connected Field Effect Transistors—W. J. Donoghue (SSD, Som.) U.S. Pat. 3697777, October 10, 1972

Method of Making a Semiconductor Device Including a Polymide Resist Film—R. N. Epifano, E. L. Jordan (SSD, Som.) U.S. Pat. 3700497, October 24, 1972

Method of Making Complementary Insulated Gate Field Effect Transistors—L. A. Murray (SSD, Som.) U.S. Pat. 3700507, October 24, 1972

Semiconductor Laser Devices Utilizing Light Reflective Metallic Layers—S. Caplan, M. F. Lamorte (SSD, Som.) U.S. Pat. 3701047, October 24, 1972

Color Picture Tube Beam Convergence Apparatus—J. W. Mirsch (SSTC, Pr.) U.S. Pat. 3701065, October 24, 1972

Consumer Electronics

Remote Controlled Television Tuner Motor Switching Circuit—L. B. Juroff, L. M. Lunn (CE, Indpls.) U.S. Pat. 369144, September 12, 1972

Television Image Control Circuit—J. K. Allen, M. N. Norman (CE, Indpls.) U.S. Pat. 3692931, September 19, 1972

Horizontal Oscillator Disabling Circuit Control Apparatus—P. C. Wilmarth (CE, Indpls.) U.S. Pat. 3692932, September 19, 1972

Mixer Circuit—D. J. Carlson (CE, Indpls.) U.S. Pat. 3694756, September 26, 1972

Fabricating Relatively Thick Ceramic Articles—F. E. Richter (CE, Indpls.) U.S. Pat. 3695960, October 3, 1972

High Voltage Hold Down Circuit—J. J. McArdle, R. L. Rauck (CE, Indpls.) U.S. Pat. 3697800, October 10, 1972

Mounting Attachment for a Modular Substrate—J. M. Yongue (CE, Indpls.) U.S Pat. 3697817, October 10, 1972

Automatic Frequency Control Circuits—J. Avins, J. Craft (CE, Som.) U.S. Pat. 3697885, October 10, 1972

Deflection Yoke Mount—E. W. Christensen, II, R. D. Eudaly (CE, Indpls.) U.S. Pat. 3697909, October 10, 1972

Web Transport Apparatus—H. R. Warren (CE. Indpls.) U.S. Pat. 3700152, October 24, 1972

Peak-to-Peak Detector—J. Craft (CE, Som.) U.S. Pat. 3701022, October 24, 1972

Electronic Signal Amplifier—S. A. Steckler (CE, So.n.) U.S. Pat. 3701032, October 24, 1972

Engineering News and Highlights

Hittinger

Kreuzer

Kolodkin

Hittinger heads Consumer Electronics; Kreuzer to move to Corporate Headquarters

Anthony L. Conrad, President and Chief Operating Officer of RCA, has announced that **William C. Hittinger** is Executive Vice President, RCA Consumer and Solid State Electronics.

In this new post, Mr. Hittinger is responsible for RCA's Consumer Electronics operations, including the RCA Sales Corporation and the RCA Distributing Corporation, concerned with the manufacturing and marketing of television sets, radios, stereo phonographs, and other consumer electronic products. In addition, he continues to direct the Solid State Division. Mr. Hittinger has been Vice President and General Manager of that Division since 1970.

Mr. Hittinger succeeds **Barton Kreuzer** as head of Consumer Electronics. Mr. Kreuzer will continue as an RCA Executive Vice President, and will move to Corporate Headquarters in New York until his retirement in early 1974. He also will continue on the Boards of Directors of RCA's Canadian and Mexican subsidiaries.

"Mr. Kreuzer has played an important role in RCA for 44 years, and for the past three years has directed our Consumer Electronics operation through a key period of product development and innovation," Mr. Conrad said. "He now will work closely with me on the development of new consumer electronics activities in both the domestic and foreign fields."

Commenting upon Mr. Hittinger's qualifications to lead RCA's Consumer Electronics operations, Mr. Conrad pointed to the executive's more than 25 years in electronics, and especially his success in developing solid state products for consumer applications.

"Mr. Hittinger has a proven record of successful leadership in an intensely competitive and technically dynamic segment of the electronics industry," Mr. Conrad said. "He has demonstrated an unusual ability to anticipate demand in the marketplace, and then to direct the development and marketing of products that respond to that demand."

Under Mr. Hittinger's direction, the RCA Solid State Division has become the industry's number one supplier of linear integrated circuits for consumer electronic products. The unit also is a leading supplier of transistors and integrated circuits for other consumer products such as automobiles, wristwatches, and clocks.

Before joining RCA in 1970, Mr. Hittinger was President of General Instrument Corporation, a post he had held since March, 1968. Prior to that, he had held a number of top executive positions with affiliated companies of the Bell Telephone System, which he joined in 1946.

Mr. Kreuzer has been with RCA since 1928. He was appointed Executive Vice President, Consumer Electronics, for RCA in 1969. He formerly was Executive Vice President, Commercial Electronics Systems, Camden, N.J. Before heading that operation, he was Division Vice President and General Manager of the Astro-Electronics Division, Princeton, N. J.

Herzog receives outstanding achievement award

Gerald B. Herzog recently received a University of Minnesota alumnus award for outstanding achievement. The award was presented by Elmer Andersen, Chairman of the University's Board of Regents at the annual Institute of Technology alumni meeting in Minneapolis.

Herzog, a 1950 graduate of the University, is Director of the Solid State Technology Center for RCA Laboratories. As a researcher, he helped design and construct the first transistorized television receiver.

In the past, he has been awarded two RCA achievement awards and the David Sarnoff Outstanding Team Award in Science. He is the author of many papers and the holder of 22 patents for semiconductor devices and applications.

Kolodkin appointed Vice President and General Manager, ASD

Irving K. Kessler, Executive Vice President, Government & Commercial Systems, has announced the appointment of **Stanley S. Kolodkin** as Vice President and General Manager of the Aerospace Systems Division, Burlington, Massachusetts.

Prior to his appointment, Mr. Kolodkin was serving as Manager, Space Systems Programs, a position he had held since September, 1971.

Mr. Kolodkin received the BSEE from MIT in 1954, and the MS from the same institution the following year. He has completed MIT's Senior Executive Program.

Mr. Kolodkin joined Aerospace Systems Division in July, 1955, as a Senior Project Member and Member of the Technical Staff. He held that position until January, 1961, when he was promoted to Leader, Technical Staff, in charge of guidance engineering. The following year, he was again promoted to Group Manager with extended responsibility for guidance and control equipment. In February, 1963, Mr. Kolodkin was appointed Group Manager, Control Systems Engineering, where he was responsible for the engineering design of the Apollo Lunar Module Rendezvous Radar, Descent Engine Control Assembly, and the Attitude Translation Control Assembly. In 1965, he was appointed Section Manager, Guidance and Control Engineering; he held that position until he was appointed Manager of Space Systems Programs.

Prior to joining RCA, he was associated with the Servomechanisms Laboratory at the Massachusetts Institute of Technology, Cambridge, Massachusetts.

Mr. Kolodkin is the author of several technical articles and publications on guidance and space navigation. He also holds two U.S. patents on gravitational sensors and rate gyro cross-coupling compensation. Mr. Kolodkin holds memberships in Tau Beta Pi, Eta Kappa Nu, Sigma Xi, AIAA and the SAE Spacecraft Committee. He is also President of Temple Isaiah, Lexington, Massachusetts.

Staff announcements

Marketing

James J. Johnson, Vice President, Marketing has appointed **Joseph W. Curran** Staff Vice President, Consumer Marketing and Marketing Services.

Richard W. Sonnenfeldt, Staff Vice President, Systems Marketing and Development has appointed **Holmes Bailey,** Director, Consumer Information Systems Development. The consumer Information Systems Development organization will be as follows: **Henry Duszak,** Manager, Systems Planning; **Patrick S. Feely,** Manager, Business Planning, and **James D. Livingston,** Manager, System Marketing.

Laboratories

Donald S. McCoy, Director, Consumer Electronics Research Laboratory has announced the following organization: **Jay J. Brandinger,** Head, TV Systems Research; **Paul K. Weimer,** Fellow, Technical Staff; **H. Nelson Crooks,** Manager, High-Density Recording Project; **Eugene O. Keizer,** Head, Video-Systems Research; **J. Guy Woodward,** Fellow, Technical Staff; **Charles B. Oakley,** Head, Electro-Optic Systems Research; and **John A. van Raalte,** Head, Displays and Device Concepts Research.

Electronic Components

Lucien P. DeBacker, Manager, Market Planning, Power Products, has announced the appointment of **Philip H. Vokrot** as Manager, Market Planning—Lasers.

Entertainment Tube Division

Joseph H. Colgrove, Division Vice President and General Manager, Entertainment Tube Division, has announced the appointment of **Donald R. Bronson** as Director, International Operations for the Entertainment Tube Division.

William G. Hartzell, Director, Television Picture Tube Operations Department has announced the following appointments: **Richard E. Meyers** as Plant Manager of the color television picture tube plant in Marion, Indiana; and **Alan R. Zoss,** Manager, Industrial Relations at the RCA color television picture tube plant in Scranton, Pa.

Government and Commercial Systems

Nicholas J. Cappello, Division Vice President, Industrial Relations has announced the appointment of Gerald P. Wixted as Administrator, Training and Organization Development.

K. K. Miller, Manager, Systems Development has announced the appointment of **Bernard F. de Gil, Jr.,** as Manager, Systems Programs (Advanced Tactical Systems).

F. Paul Henderson, Manager, Requirements Planning has announced the appointment of **Milton Collier** as Manager, Requirements Planning, Air Force.

Electromagnetic and Aviation Systems Division

Frederick H. Krantz, Vice President and General Manager, has announced the following appointments: **James F. Gates** as Manager, SECANT Program and **George F. Fairhurst** as Manager, Product Assurance.

Joseph F. McCaddon, Division Vice President, Aviation Equipment Department, has announced the appointment of **J. Lawrence Parsons** as Manager, Aviation Program Operations.

Robert Haak, Manager, Field Service has announced the appointment of **Kenneth L. King** as an Avionics Field Engineer for the RCA Aviation Equipment Department.

John P. Mollema, Manager, Marketing has announced the appointment of **Dan Northrop** as Manager, Central Region Sales for RCA's Aviation Equipment Department.

Promotions

Electronic Components

J. T. Gote from Sr. Eng. Prod. Dev. to Eng. Ldr. Prod. Dev., Imaging Systems Engineering (H. R. Krall, Electro-Optics Systems)

Government Communication Systems

R. E. Jansen from Ldr., Engrg. Staff to Mgr., Airborne Programs (F. D. Kell, Recording Equipment Engineering)

G. T. Rogers from Ldr., Engrg. Staff to Mgr., Instrumentation Programs (F. D. Kell, Recording Equipment Engineering)

B. F. Wheeler from Ldr., Engrg. Staff to Mgr., Systems Engr. (M. C. Myers, Electronic Warfare Engineering)

Electromagnetic and Aviation Systems Division

F. C. Easter from Principal Member, D&D Eng. Staff to Adm. Producibility Evaluation, Data Processing Engineering (P. Korda, Engineering Technical Assurance)

Licensed engineers

When you receive a professional license, send your name, PE number (and state in which registered), RCA division, location and telephone number to: *RCA Engineer*, Bldg. 2-8, RCA, Camden, N. J. As new inputs are received they will be published.

Missile and Surface Radar Division

Dr. J. E. Mulholland, M&SR, Moorestown, New Jersey. PE 18899-E; Pennsylvania.

J. R. McAllister, Dead at 53

John R. McAllister, 53, Division Vice President and General Manager of the Aerospace Systems Division, Burlington, Mass., died suddenly on October 28, while visiting in Sugarbush, Vt. His home was in Concord, Mass.

Mr. McAllister joined RCA in 1961 as Purchasing Agent in the company's Camden, N.J. facility. As a member of the RCA staff, he was Director, Purchases, for RCA's Defense and Data Processing organizations before being named Plant Manager at Burlington in 1966.

Before joining RCA, Mr. McAllister was with the Philco Corporation in Philadelphia for 14 years. A native of Philadelphia, Mr. McAllister attended the University of Virginia and the Wharton School of the University of Pennsylvania. He served in the U. S. Navy during World War II and left the service with the rank of Lieutenant Commander.

He is survived by his father, Albert T.; his wife, Elizabeth, and two daughters, Mrs. John E. Baker, and Holly.

Professional activities

Government and Commercial Systems

F. Pfifferling is a member of the 1973 IEEE International Convention Technical Program Committee, responsible for organizing sessions on Multiplexing, Television, and Automatic Testing. He also is serving as the chairman of a session entitled "Instruments for Computer Controlled Test Systems," and is an invited panelist in an ATE Applications Session.

Electronic Components

Robert L. Kelly, Staff Manager, Quality and Reliability Assurance, Electronic Components, Harrison, N. J., was presented the Outstanding Accomplishment Award of EIA's Engineering Department at the Annual Convention. Presented periodically to persons active in EIA technical and engineering areas, the award recognizes Mr. Kelly for participation going back to World War II days.

Flemming elected SMPTE Fellow

The Board of Governors of the Society of Motion Picture and Television Engineers, upon the recommendation of the Fellow Membership Award Committee, has conferred the distinguished grade of Fellow Member upon Frank L. Flemming, Vice President, Engineering, NBC Television Network.

Mr. Flemming's citation reads: "Because of his stature and the important and responsible position now held by Mr. Flemming at NBC, he brought to bear a significant influence in the broadcasting engineering field."

A Fellow of the Society is one who is no less than 30 years of age and who has, by his proficiency and contributions, attained an outstanding rank among engineers or executives of the motion picture, television, or related industries.

Mr. Flemming graduated in electrical engineering from the University of Buffalo. Moving from Sylvania to CBS in 1954 he became Director, Plant Systems Engineering and was responsible for engineering of many new TV equipments and systems. He was Chief Engineer, Visual Electronics Corp., from 1967-1969. At NBC he has responsibility for design, specification, installation and costs of technical equipments and systems plus architectural design for NBC Television Network and NBC Radio Network.

Richard Coalter admitted to practice

Richard G. Coalter a member of the Patent Department, has passed the Texas Bar examinations and admitted to practice law in September 1972.

Mr. Coalter received his Juris Doctor degree from University of Texas in May 1972 and his BSEE from the same school in August 1964. He joined the **RCA** Patent Staff in July 1972.

Awards

Missile and Surface Radar Division

Nine M&SR engineers received Technical Excellence Awards for the First and Second Quarters of 1972. The award winners were cited as follows:

W. J. Beck for outstanding performance in directing the AN/FPS-95 site technical effort, involving the successful Category II demonstration and selloff of the entire system (antenna, RF hardware, transmitter, and low level electronics).

E. G. Lurcott for developing, defining, and documenting functional interrelationships leading to an overall functional analysis of the Command, Control (C,C) system of AEGIS.

R. P. Perry for major contributions in digital signal processing technology with application to high performance radar systems—specifically, a new digital signal processing approach called the Step Transform method which conservatively reduces the amount of matched filter hardware by a factor of three over competing pipeline FFT techniques.

K. Berkowitz for outstanding performance on the development of the precision guidance subsystem of the AN/TPQ-27 system and his special contribution in a quick turnaround rework of guidance loops to accommodate unscheduled changes in aircraft performance.

E. Dixon for a unique personal contribution to the completion of the AN/SPY-1 radar beamformer waveguide assembly, in terms of both technical performance and timely completion.

J. Grabowski for outstanding technical contributions in the redesign of the TRADEX dual-frequency L/S-band antenna feed system.

D. Olivieri for continuing contributions in the area of mechanical design studies related to solid-state transmit-receive module development.

D. V. Wylde for demonstrated systems engineering excellence and ingenuity in helping M&SR dvelop a level of expertise required for a competitive position in the field of high energy laser devices.

L. O. Upton, Jr. for creativity and resourcefulness in developing high-density digital memory techniques employing MOS and p-MOS devices, as well as an adaptive clutterlock MTI cancellation system utilizing these techniques.

Aerospace Systems Division

The team of **Lawrence B. Blundell; James W. Boyd, Jr.; Edmund F. Duratti; Richard B. Elder; Eldon M. Fisher; Donald G. Gionet; John Hallal; Demetrios Lambropoulos; Ernest A. LeBlanc; James A. McNamee; Herbert L. Slade; John Thornhill, Jr.;** and **Edgar W. Wallace** received a Technical Excellence Award for its excellent work on the SOD phase-C program. This program involved the delivery of 44 units packaged in two different configurations. The design tasks were to provide sensitivity improvements for X-band, reduced cross channel coupling, and new packaging to meet extremely tough environmental specs. The program included field tests of six weeks on two breadboard units and thirteen weeks on ten complete systems. "Drop Tests" were included. The team performed all design, development, factory follow, module assembly, electrical test and field support. Manufacturing provided the individual PC board fabrication and assembly, and mechanical fabrication.

Max Lehrer, Division Vice President and General Manager, M&SR, and Dudley Cottler, Chief Engineer, honor Technical Excellence Award winners. Left to right: J. Grabowski, E. Dixon, D. Olivieri, M Lehrer, R. P. Perry, K. Berkowitz, E. G. Lurcott, L. O. Upton, Jr., and D. M. Cottler.

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