Future directions

RCA's withdrawal from the general-purpose computer business intensifies the need for us to seek and achieve leadership in new fields of electronics and information technology. This is essential if we are to sustain a high long-term growth rate for RCA.

At the same time, in withdrawing from the commercial computer market, RCA is not turning away from computer technology. To the contrary, the engineering skills and knowledge that we have developed in this field over the past two decades must now support intensified research and development in data communications, specialized computer systems, and new information processing concepts and techniques for consumer as well as commercial and government applications. All of these constitute important areas of business which promise significant long-term profit growth for an alert and technically competent company.

Creative engineering is more essential today than ever in advancing RCA's position in all of our continuing operations—global communications, government and commercial systems, consumer products, components, and technical services across the entire spectrum of electronics. It will be a long time before the prospects are exhausted for substantial rates of business expansion in any of these fields.

Despite our structural changes in recent years, RCA is still a technology-based company, deriving over two-thirds of its volume and profit from electronic communications and information handling. We are, and intend to remain, a pace-setter in an electronics industry which should achieve a record domestic volume of more than $26 billion in 1972—and even more if the economy regains its full health.

While we occupy a strong position in this industry, we cannot be complacent about it. We must reexamine our technological resources in the light of our new situation. We must then focus them more effectively than ever on development programs that will enable us to open new markets and enlarge our share in those we already serve.

Anthony L. Conrad
President
RCA

Our cover

. . . depicts a portion of the memory cells in silicon-gate PMOS beam-lead memory array. The array appeared on our last cover and is being repeated in different colors because of the large number of papers dealing again with solid state technology. **Photo credit:** John Semonish, Electronic Components, Clark, N.J.

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• To disseminate to RCA engineers technical information of professional value • To publish in an appropriate manner important technical developments at RCA, and the role of the engineer • To serve as a medium of interchange of technical information between various groups at RCA • To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions • To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field • To provide a convenient means by which the RCA engineer may review his professional work before associates and engineering management • To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

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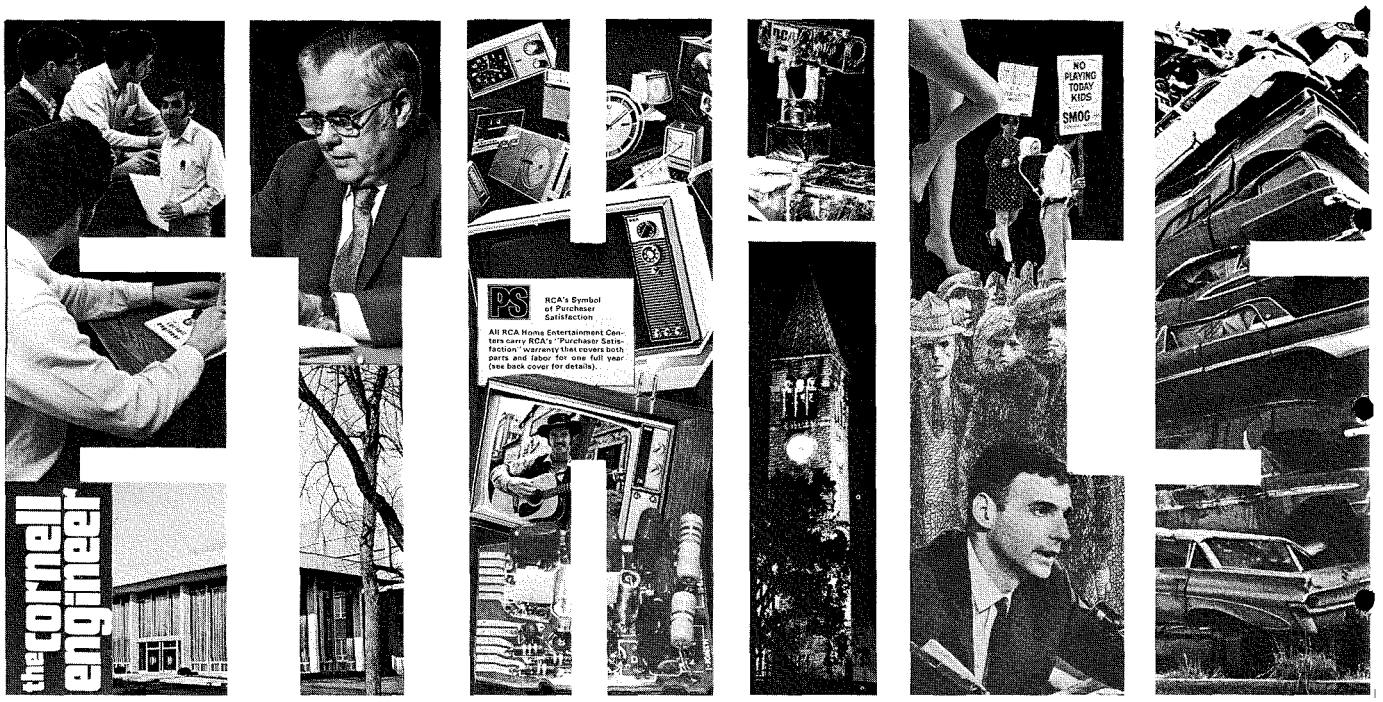


Engineering ethics and the consumer

Dr. James Hillier

I firmly believe that the lots of the consumer and the engineer have been steadily improving in the past 25 years because of natural correcting forces that have become built into our "system." I am worried that the present emphasis on "consumerism" will disrupt the natural correcting forces by replacing them with various forms of regulation. Again, I have no illusions regarding the fact that the absolute number of faulty products is too high. But the method of attacking the problem without completely understanding the system or the variations in it and by assuming that all industry is equally guilty, can only work to the detriment of the consumer in the long run.★

Editor's note: In this era of the "consumer movement," the accusations leveled at industry have ranged from complaints of shoddy products to collusion in the suppression of advanced developments and even to the charge that potentially hazardous merchandise is knowingly put on the market. These indictments have even carried implications of a deeper, moral issue—that they are the result of corporate suppression of the professional integrity of engineers.

To examine the role of "engineering ethics" in industry, *The Cornell Engineer*, an undergraduate magazine, conducted a survey to get views, opinions, and perspectives on the "real world" of business. A thought-provoking reply to this survey (published in the March 1971 issue of *The Cornell Engineer*) came from Dr. James Hillier, Executive Vice President, RCA Research and Engineering, Princeton, N.J. The questions in the survey and Dr. Hillier's responses are presented in this article.

In evaluating the queries, Dr. Hillier expressed his concern about the nature of the questions themselves. They could be construed "to be 'loaded' to the extent that 'knocking' the system would appear to be the only possible response." Or, "if the questions are 'straight' and prepared in innocence, they expose a naivete, or worse, create a fear about the education, image, or propaganda mechanisms that give students such an incomplete and distorted view of the business world."★

Although the Cornell survey results are directed toward Cornell's engineering undergraduates, the issues are real and fundamental, and Dr. Hillier's perspective of the business world will be of interest to RCA's research and engineering community.

The questions asked in the survey are italicized.

RCA Reprint RE-17-4-23

★ From a letter by Dr. Hillier to the editorial staff of *The Cornell Engineer*.

The dictionary defines ethics as "the standards of conduct and moral judgment of a group." What is your definition of engineering ethics?

My view of proper engineering ethics requires that an engineer have as his basic objective the designing of a product that gives the customer the best possible value for his money. In so doing the engineer must be concerned with the following:

a) Providing the best possible performance in a product to accomplish its intended purpose consistent with economic and other constraints.
b) Achieving a manufacturing cost of the product that is low enough to enable the manufacturer to provide reasonable pay for all his employees and a reasonable profit for the owners of the business so that the enterprise can continue to serve its customers and can continue to provide employment.
c) Taking every reasonable precaution to be certain that the product is not and will not become hazardous in any way or present an undue safety problem.

Does your company's selection process try to determine the "ethics" of prospective engineers? Why or why not?

Our company's selection process for prospective engineers concentrates on trying to determine their competence and creativity in the engineering fields related to our needs. We assume that a prospective engineer has acceptable engineering ethics. The total hiring process—application forms, reference checks, etc.—that is quite standard for most industry has evolved over many years and has many implicit checks on ethics such as honesty, forthrightness, responsibility. We do not knowingly hire people when dishonesty or irresponsibility has been revealed in their past.

Does your company have seminars on engineering ethics? Does your company have codes or guidelines for engineers?

RCA does not have seminars on the specific subject of engineering ethics. However, we do have seminars and training courses on subjects that have an engineering ethics connotation such as Value Engineering and Analysis, Product Assurance, Product Safety, Product Reliability, and Product Quality.

The Company has a comprehensive and continually evolving set of policies, procedures and guidelines that apply to all employees including engineers. Included in these are many that are specific to engineers.

When your company decides to manufacture a new product, how does it analyze its cost versus its quality? (For example: if for an increase in cost, your company can produce a superior product, what factors will go into choosing alternatives?)

Technology-dependent manufacturing companies fall into two distinct categories.

a) Those providing consumable materials.
b) Those providing products that, in turn, provide service to their customers.

RCA falls into the latter category for which the question is over simplistic and probably naive.

The fundamental and ultimate determinants of "quality" are the total service provided to the customer . . . and the total cost.

The fundamental and ultimate determinants of "quality" are the total service provided to the customer by the product and the total cost per unit time to the customer for that service. Thus life expectancy of the product and the frequency and cost of maintenance have to be included in "quality" in addition to technical level of performance. There are many other factors that also must be included.

The price the customer is willing to pay for the product is very dependent on the value he places on the service provided relative to his need for it. The price he must be charged is sensitively dependent on the number of customers willing to pay it. Thus the analysis of cost (manufacturer's) versus quality is only a small part of the total analysis that must be made.

. . . best "value" for the customer is usually the best business for the manufacturer . . .

Some of the relationships to be considered are:

a) Volume versus price to customer.
b) Manufacturing cost versus volume.
c) Technical performance versus cost.
d) Life expectancy versus cost.
e) Volume versus technical performance at given customer price.
f) Fixed initial investment in engineering versus the product-price times volume.
g) Competitive offerings, etc.

It is to be noted in most of these relationships that the challenge transmitted to the engineers from management is always to provide the best possible quality at the lowest cost.

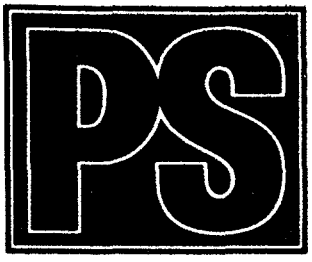
The specific example quoted can be used to illustrate the traps in simplistic thinking. Consider the case of a product that has a life expectancy of five years and a "superior product" that has a life expectancy of ten years but requires a price that is double or nearly so. We shall assume all other things are equal. From the customer's point of view the alternatives appear nearly equal. The cost per unit time for the service is the same in each case. The inconvenience of having to buy a second unit after 5 years is balanced by the added flexibility and the possibility of technical improvements occurring in the first five years. From the manufacturer's point of view the alternatives also appear nearly equal. The profits over the ten-year period are equal. The high immediate double profit on the ten-year product being balanced against cost reductions and competitive reactions that could occur when the five-year products have to be replaced.

All of this is correct in a fundamental and theoretical sense. In the "real world" the double price of the "superior product" would drastically cut the volume. The cost of production would be increased to such an extent that the increased life expectancy would have to be cut back to the point where it might not be significantly greater than the five-year product. Then the cost per unit time of service to the remaining customers would be considerably higher than if only the five year product had been offered at the original price.

This very elementary example illustrates what I believe is a more general principle—what is best "value" for the customer is usually the best business for the manufacturer, and the best "value" for the customer is not necessarily that provided by the "superior product" in a conventional engineering sense.

Similarly, when your company decides to manufacture a new product, how does it analyze production or process cost versus percent that will be defective and not "caught" before shipment?

I do not like the inference in this question. While it is true that statistical testing methods are used in our company for the testing of many components that go into our products, the manufacturing process is always designed to give the final product a 100% test for operation within specifications. The output is further checked, this time statistically, by a quality control group that is administratively independent from the production group. This general procedure has been used in every large company with which I have been familiar.



Symbolic of RCA's commitment to purchaser satisfaction, the "PS" on RCA color televisions assures customers that defects in the set will be repaired free of charge by RCA within one year from the date of sale.

Any time a company "plays games" with a product to raise sales, there is always a competitor waiting to play the other side of the game.

Every manager knows that the direct cost of repairing a defect after a product is sold is 20 to 50 times greater than detecting and repairing it in the factory. The additional and indirect cost arising from customer defection is much higher.

This does not mean that none of our products ever have defects. They are still designed by human beings, built by human beings, inspected by human beings, transported by human beings, and used and mis-used by human beings none of whom is perfect.

. . . the positive approach of designing, producing and testing products that are absolutely safe and not prohibitively expensive presents many extremely challenging engineering problems.

The same question for products that are potentially harmful if defective (such as car brakes).

The inference here that any large responsible manufacturer would knowingly permit potentially hazardous defects to exist in its products as a cost saving measure is incredibly naive. There is enormous economic incentive to do exactly the reverse. Any such cost savings are invariably trivial compared to the liability costs of the hazard and the concomitant loss of customers.

On the other hand, the positive approach of designing, producing and testing products that are absolutely safe and not prohibitively expensive presents many extremely challenging engineering problems.

Industry sometimes finds that its products are too good, that they do not wear out or fail for years. Therefore, the company finds sales falling as people only need buy the item once (case in point, the original run-proof nylon stockings.) The company then decides to shorten the life of the product to raise sales, a form of planned obsolescence. Who decides this in a corporation and what factors enter into this decision?

I disagree strongly with the basic premise implied in this question. It again shows a sad lack of understanding of the realities of the business world. Any time a company "plays games" with a product to raise sales, there is always a competitor waiting to play the other side of the game.

In spite of many statements to the contrary, competition in our business (and, in fact, in most businesses) is very intense and very real. This is the strongest and best form of protection the consumer has. As I have indicated elsewhere, outside regulation often tends ultimately to work to the disadvantage of the consumer.

Obviously the wrong inference is drawn from the example given. Sheer but fragile nylon stockings have replaced the heavy run-proof ones not because of any ethical or non-ethical decision by an engineer, but because a majority of women like the way sheer stockings look on them and are willing to accept the penalty of shorter life. Certainly one cannot sensibly argue that it is an engineer's ethical concern to insist that his customer buy what the engineer considers is technically, economically, or for that matter, spiritually best for the customer, no matter what that "best" product may do to the customer's id, ego, or super ego. Certainly, if women wanted the original run-proof versions, a competitor would have grown big supplying them.

Seriously though, we do feel it is both ethical engineering and good business to make yesterday's product less desirable by putting today's technical achievements in our products and thereby make them more desirable to our customers. Again, if we did not, a competitor would.

A case in point is the rectangular tube that replaced the round tube in color TV receivers. It took some solid, costly engineering to perfect that tube so that it could be made available commercially at a reasonable price. It provided the customer with a better looking TV set that had a better picture, and it increased the sales of color TV receivers. The overall result was more value for the customer, more profit for the business owners, and more stable employment for the engineers.

I am not trying to say that all the products of all large companies are always perfect or even good values.

As with people, ethics and other characteristics vary from one corporation to another.

As with people, ethics and other characteristics vary from one corporation to another. However, in general, customer consciousness is good business and it tends to be highest with large corporations (one of the reasons they grow to be large) and lowest for the "schlock" or "fly-by-night" houses. Yet, it is still possible to pay more and get a "lemon" from a large company and pay less and get a real "buy" from a small one.

If your answers indicate that you feel that industry regards the consumer as king, how do you explain the great number of faulty products, the shoddy construction, fraudulent claims and other forms of what we consider consumer fraud present today?

In my answers I have tried to indicate that to consider the consumer as king is simply good business. Speaking as a consumer, I have observed a steady improvement in the performance and quality of the manufactured products I buy. I agree that faulty products and shoddy construction still exist, but I believe it is on a relatively smaller scale.

As I indicated in the preceding question, there is a range of customer consciousness that can be very low in some types of organizations. However, I do not believe all manufacturers should be "tarred with the same brush."

Similarly there is a range of selling approaches that runs from putting one's product "in the best light" to outright misrepresentation. Here, too, for whatever reason, I have observed a steady improvement.

If your answers indicate that you feel that industry holds a "consumer be damned" attitude, how can the situation be improved or do you feel it should be?

Dr. James Hillier
Executive Vice President
Research and Engineering, RCA
studied at the University of Toronto, where he received a BA in Mathematics and Physics in 1937, MA in Physics in 1938, and PhD in Physics in 1941. Between 1937 and 1940, while Dr. Hillier was a research assistant at the University of Toronto, he and a colleague, Albert Prebus, designed and built the first successful high-resolution electron microscope in the Western Hemisphere. Following this achievement, Dr. Hillier joined RCA in 1940 as a research physicist at Camden, N.J. Working with a group under the direction of Dr. V. K. Zworykin, Dr. Hillier designed the first commercial electron microscope to be made available in the United States. In 1953, he was appointed Director of the Research Department of Melpar, Inc., returning to RCA a year later to become Administrative Engineer, Research and Engineering. In 1955, he was appointed Chief Engineer, RCA Industrial Electronic Products. In 1957, he returned to RCA Laboratories as General Manager and a year later was elected Vice President. He was named Vice President, RCA Research and Engineering, in 1968, and in January 1969 he was appointed to his present position. Dr. Hillier has written more than 100 technical papers and has been issued 40 U.S. patents. He is a Fellow of the American Physical Society, the AAAS, the IEEE, an Eminent Member of Eta Kappa Nu, a past president of the Electron Microscope Society of America, and a member of Sigma Xi. He served on the Governing Board of the American Institute of Physics during 1964-65. He has served on the New Jersey Higher Education Committee and as Chairman of the Advisory Council of the Department of Electrical Engineering of Princeton University. Dr. Hillier was a member of the Commerce Technical Advisory Board of the U.S. Department of Commerce for five years. He was elected a member of the National Academy of Engineering in 1967 and is presently a member of its Council.

Most engineers, including myself, welcome continued pressure for improvement in both these areas. However, the pressure should be intelligent and realistic rather than a sequence of crusades, often politically motivated. The consumer should also recognize that ultimately he has to pay for all the advances in quality and safety. As I indicated in the earlier questions, this could lead to the customer obtaining less value per dollar and, ultimately, to less employment.

Are the "ethics" or policy of a company forced upon its engineers? Please give examples if possible.

Any large company with integrity requires that its engineers abide by its standards of ethics. There is no other way for it to provide the customer with products that meet its standards of quality and value.

I object to the word "forced" and the implications that a company's "ethics" and policy are always distasteful to engineers. This again shows a lack of understanding for the "real world." Large companies that are dependent on technology and have grown during the past twenty-five years have done so in a long period of extreme shortage of good engineers. It goes without saying that no engineer had to work for a company with whose ethics and policy he disagreed. While the situation is generally different today, it really has not changed for the best engineers who are still in short supply.

In other words, on problems of ethics, policy and freedom it has been "good business" for a company to have policies acceptable to the majority of engineers. Here again, I have to recognize that this situation varies from company to company. However, I doubt if any company that has grown large in a period that covers several generations of engineering graduates could have done so with distasteful engineering ethics and policies.

. . . pressure should be intelligent and realistic rather than a sequence of crusades, often politically motivated.

If an engineer feels that a project he is working on is "unethical" and he therefore refuses to continue working on it, will he be fired? Please give examples if possible.

No—we respect individual's desires. If an engineer in our company is doing work on a military project and decides that his project has taken a turn that he considers unethical, he will certainly be replaced on that project. Whether he would be retained by the company would depend on the availability of a suitable opening on a project acceptable to the employee.

During World War II several "conscientious objectors" refused to work on military projects. Other projects were found; all the individuals I knew about are still with the company nearly thirty years later.

Do you feel that an outspoken advocate of ecology can get a job in industry?

Speaking for our own company, it depends on whether the "outspoken advocate of ecology" is destructive or constructive. The outspoken advocate of ecology who simply vilifies the "establishment" for the pollution mess, would not be welcome. On the other hand the outspoken advocate of a solution to the pollution mess would be welcome if the solution were relevant to our business.

Referring back to the four responsibilities an engineer should feel, which would you place first in importance and why? (Viz "moral responsibility to themselves, the engineering profession, then eventual employers, and their society.) Secondly, in a given situation, how do you evaluate what to do?

I think the engineer's primary feeling of moral responsibility has to be to himself. I do not want anyone working for me who feels that what he is doing is morally wrong. If a man is not honest with himself, then he will not be honest with his employer, his profession, nor, I believe, with society.

. . . convincing oneself that a true "ethical conflict" exists is often the most difficult part of the problem.

A man's moral responsibility should be to society next, and then to the two specific segments of society you mention, his eventual employer and his profession, and I don't see much point in trying to order the importance of the last two. A man who is morally responsible to himself and to society will be morally responsible to both his profession and his employer.

Presumably the "given situation" mentioned in this question refers to one of ethical conflict between the engineer and his employer. Perhaps the most difficult step in evaluating what to do is to first determine that it is truly an ethical conflict.

Is your employer really asking you to design an inferior product or do you have a hang-up because he's doing some judicious cost-cutting that eliminates some of your sophisticated engineering that unfortunately the customer is not willing to pay for? (As an aside, I would like to emphasize that sophisticated engineering does not necessarily mean safer or even better engineering.)

In practice, convincing oneself that a true "ethical conflict" exists is often the most difficult part of the problem. Value judgments have many shades of gray and the paycheck and all it represents have been known to warp men's judgments.

But if a man is honest with himself and is truly convinced that he is being asked to do something that is morally wrong, his path along the following lines should be clear.

a) Attempt to convince his superior and the management of the company that the company is asking for something unethical and that it should change to an acceptable ethical practice or procedure.
b) Failing this, the engineer should either ask to be transferred or resign his position, depending upon his conscience.
c) If he has a good reason to believe the company is doing something that is illegal as well as unethical, he should report this to the proper governmental authorities.

Simulation study for a circuit and message switch communication network

K. Weir | P. Boehm

Simulation of complex electronic switching systems requires the use of many variables in the mathematical model which represents a particular system. The complex structure of the model dictates the use of a computer to facilitate calculations. This paper describes such a simulation which provides for an examination, evaluation, and manipulation of the system without any direct action on the system itself or on a physical model of the system.

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received the BSEE from Pennsylvania State University and the MSE from the University of Pennsylvania. Mr. Weir joined RCA in 1958 and has worked in various activities mainly concerned with Systems Assurance (i.e. Reliability, Maintainability, Availability; Systems Effectiveness, Safety, and Life Cycle Costing). Mr. Weir has worked on Techniques Development during study contracts, implementation of these techniques on small equipment and large system contracts, and administration of the implementation of these techniques during Project Management Office assignment. He is currently working in a Systems Engineering Activity as part of Information Processing and Control Systems. He is a member of Tau Beta Pi, Sigma Tau, and Eta Kappa Nu.

Paul Boehm
Government Communications Systems
Communications Systems Division
Camden, New Jersey
received the BEE from Ohio State University in 1951. At RCA, Mr. Boehm has been active in the field of data processing systems and communication systems. He has participated in both a supervisory and working capacity in the generation of system concepts, the generation of functional and design specifications, the implementation of designs to meet these specifications, and the preparation and conduction of system tests on completed machines to verify performance. Mr. Boehm spent one year in Canada as a consultant for the Canadian government assisting in the specification of a large, multi-node digital communication system. Mr. Boehm participated in the development of the requirements for a highly-parallel computer of the ILLIAC IV-type for use in an adaptive phased-array radar environment. In a one-year study and investigation of a combined circuit switch and/or store-and-forward switch for digitized voice or digital data, Mr. Boehm was responsible for the implementation of the system requirements on the software and hardware of the central control computer(s). As one part of the extension to the study, Mr. Boehm simulated a communication network on an RCA Spectra system using the FLOW SIMULATOR language.

Authors Boehm (left) and Weir.

THE PAYOFF for every technological system comes when the user is able to operate it in its intended manner. This settles beyond doubt that the system requirements have been satisfied. The design is a success. If this does not happen, the system is a failure. It must be redesigned or re-configured with associated added costs. When this happens, the additional cost may be such that the system loses its value to the user. He may want such a system, but cannot afford it.

An aircraft is well designed when it is loaded, becomes airborne, and flies to its destination. But the risks involved in proving out the design at this point are horrendous. Consequently, in the course of the aircraft design, various scale models are constructed which are subjected to scaled-down stresses in an endeavor to determine how this model will react. The accuracy built into this model to simulate what the actual aircraft will be like and the accuracy of the stresses imposed on it determine the probability of the test simulating the actual aircraft. Every aircraft is subjected to such simulated tests, but sometimes aircraft fail in actual flight. This is simply because the accuracy of the simulation is not very good. This type of simulation is a physical model of the intended design and is a step to a more generalized type of simulation—the mathematical model. A mathematical model is simply a mathematical equation which represents the

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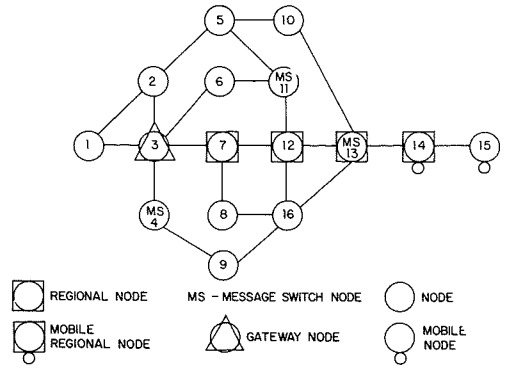

Fig. 1—16-node network.

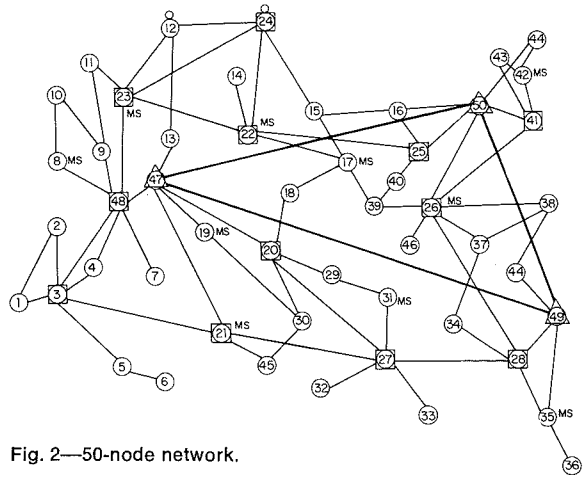

Fig. 2—50-node network.

strengths and stresses of the system to be proven. Thus, in its simplest terms, simulation is an endeavor to imitate mathematically what is actually the system design.

Stated more precisely, simulation is a problem solving technique which structures a mathematical model and observes model changes with time. It can derive new information as to performance by manipulating relationships between variables. In some technological systems, such as a complex electronic switching system, the simulation would require many variables to represent the system and it would be necessary to use a computer to facilitate calculations.

Consider a communications switching system which is capable of handling voice or data lines and can accept circuit-switched (CS), message-switched (MS), or optional messages (MSO). Circuit-switched messages cannot be stored and, therefore, are lost when a connection cannot be made. Message-switched messages are stored at least once and can be stored and forwarded in the event a connection cannot be made. Optional messages are either circuit switched or message switched. They are handled as circuit-switched messages unless a connection cannot be made at which time they are handled as message-switched messages. The model which will simulate the operation of this communication switch will produce outputs such as delay times for signalling, lost call statistics, summary statistics for circuit-switched messages, and the time in the system for message-switched messages. The mathematical model for the switching system is programmed using the RCA FLOWSIM Simulation Language and has been run on an RCA Spectra 70/45 computer.

The work performed in the simulation study is divided into four parts. The structuring of the simulation model is described, program flow diagrams are shown, the simulation runs are identified, and finally the results obtained from the work already completed are given.

Simulation model

The system operating parameters used in the simulation model include:

Network size
Trunk capacity
Message priorities
Message destination percentage
Traffic
Message types
Message routing
Trunk and node outages
Mobile subscribers and nodes

Each of these parameters is described separately below and their relationship to the simulation model is given.

Network size

A 16-node network and a 50-node network (Fig. 1 and 2, respectively) were simulated. These networks were entered as input data in the form of connectivity matrices rather than as part of the program structure. Each node in each network simulates a communication switch.

Trunk capacity

Trunks are the connecting paths between nodes and consequently limit traffic flow between nodes depending on their size. Signalling is "in-band,"* hence, signalling and supervision data will utilize part of the network trunk capacity. Trunk capacity is specified in terms of the number of simultaneous voice, data, and supervision signals that can be handled. Simulations are run with unlimited trunk capacity to measure trunk utilization. Having measured trunk utilization, further simulations are run at that utilization level.

Message priorities

Since a communication switch will always have call priorities, such priorities will be assigned for simulating a real situation. Five priorities were used; the percentage of messages assigned to each of the priorities is as follows:

Priorities	*Percent of messages*	*Cumulative percent of messages*
5 (highest priority)	1	1
4	3	4
3	15	19
2	31	50
1 (lowest priority)	50	100

These priorities are based on previous experience and will be used throughout the simulation.

Message destination percentages

Messages are categorized as to their destinations and from this each destination will be assigned a numeric which gives its percentage of the total messages transmitted. To facilitate simulation, the message destination

* In-band signalling is a term used to describe the use of the same frequency band for both signalling and supervision information and voice and data information transfer.

percentages will be assumed to be as follows:

- Messages local to originating node (25%)
- Messages to immediately adjacent nodes (15%)
- Intra-net messages (35%—split equally by nodal distance from originating node)
- Messages to mobile subscribers (5%)
- Messages to mobile nets (10%)
- Inter-net messages (10%)

With normal traffic of 0.25 erlangs** per subscriber, it will be assumed that 25% of all attempted calls will get SUBSCRIBER BUSY.

Traffic

Traffic refers to the rate that messages are generated and introduced into the node processing program. Four variations in traffic are included in the simulation runs:

- Normal traffic
- Reduced traffic (0.8 x normal)
- Increased traffic (1.2 x normal)
- Variable traffic (normal traffic with occasional peak loads)

Normal traffic is further defined as:

- All messages will be generated by subscribers
- All subscribers will generate the same traffic
- The number of subscribers per node will be rectangularly distributed between 200 and 500
- The mean time between message originations will be 200 seconds per subscriber with an exponential distribution
- Voice messages will have a mean duration of 180 seconds
- Data messages will have a mean duration of 15 seconds
- Message durations will be exponentially distributed.

Message types

There will be seven message types with a percentage of messages assigned to each type for all simulation runs. These are:

Data Messages (70.0%)
- Multiple address circuit switched (2.0%)
- Single address circuit switched (22%)
- Multiple address message switched (2.0%)
- Single address message switched (22%)
- Single address optional (22%)

Voice Message (30.0%)
- Conference calls (6.0%)
- Two party calls (24%)

** Erlang is a unit of measurement for traffic intensity and is equal to total circuit usage during an interval of time divided by the time interval.

Additionally, multiple address messages including conference calls involve 3, 4, or 5 subscribers each having a probability of occurrence of ⅓. This means that one third of the multiple address messages will involve three subscribers; one third, four subscribers; and one third, five subscribers.

Message routing

Message routing is concerned with the route a message will follow from its origination node to its destination node. In the simulation, fixed message routes are utilized. There is one primary path and one or two secondary paths established for communication from any node to any other node. If a connection cannot be made using a primary path, the secondary path(s) is tried. If a connection still cannot be made, the message is stored and forwarded later or lost depending on the message type. Adaptive routing schemes are planned for future simulation runs. With adaptive routing the message route may be modified at any time based upon the then extant system operating conditions.

Trunk and node outage

Trunk/node outages will be simulated in some of the simulation runs by providing additional input information which will indicate which trunk/node(s) are to be removed from the net. The simulation program will take trunk/node outages into account when calculating message routes or paths.

Mobile node and subscriber

Within the system concept, a mobile node is one which moves geographically,*** taking most or all of its subscribers with it. (A mobile subscriber is a subscriber who does not stay associated with a particular node.) The relative location of all nodes and subscribers is known and stored in regional nodes. When a subscriber or node moves, the new location is transmitted to regional nodes rather than to all nodes. Some simulation runs include mobile subscribers and nodes to evaluate transient conditions between the stable system periods before and after the moves.

*** A mobile node which moves geographically is typically a communication van in the front lines or a ship at sea. A mobile subscriber would typically be the President, or a general.

Program Flow diagrams

Since the simulation of the switching system is logically subdivided into traffic generation and nodal processing, it was decided that separate programs should be written to handle traffic generation and node processing. The output of the traffic generation program will serve as the input to the node processing program. Separating the two programs allows the traffic generation program to be run once, the results stored on tape, and these results used with almost all node processing program runs. This approach, therefore, reduces the computer processing time and cost when compared with several system simulations using a single program. Traffic generation and node processing program flow diagrams are shown in Figs. 3 and 4, respectively.

The traffic generator

The traffic generation program provides an output which is a list of transactions representing messages or traffic to be handled. As shown in Fig. 3, transactions are initiated in "generate blocks," each representing a system node and each transaction representing a message. Each node has an assigned number of subscribers rectangularly distributed between 200 and 500. It is assumed that each subscriber generates the same traffic. Therefore, the number of messages (transactions) per unit time initiated at each node "generate block" is directly related to the number of subscribers. Each subscriber generates messages in accordance with the exponential distribution with a mean of 200 seconds. A fixed percentage of messages are assigned as voice or data messages; as circuit-switched, message-switched, or optional messages; and as single-address (two party call for voice messages) or multiple-address messages (conference calls for voice messages). Message destinations are also assigned on a fixed percentage basis. The traffic generator then determines, based on network connectivity, a primary transmission path from the originating node to the destination node. Additionally, the path to the nearest regional and gateway nodes are identified. Message priorities are then established which completes the required information concerning messages.

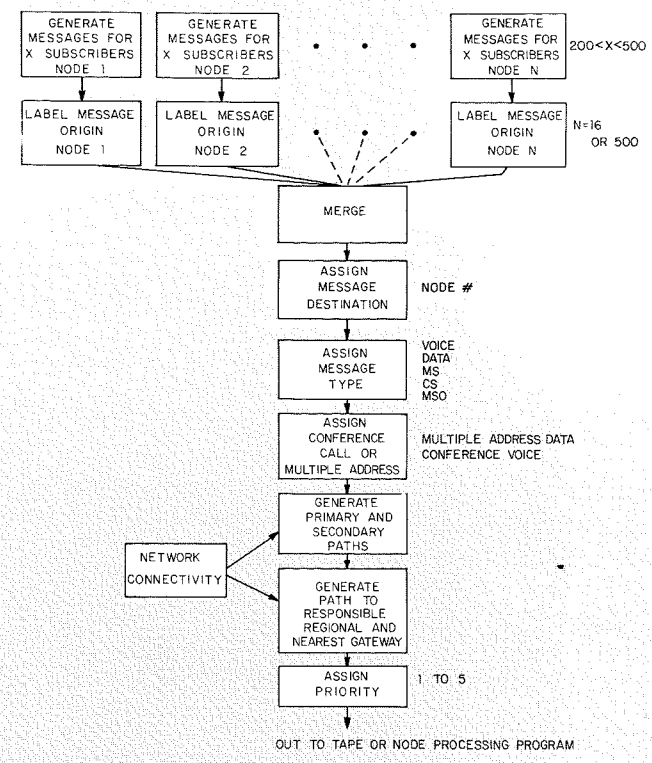

Fig. 3—Traffic generation flow chart.

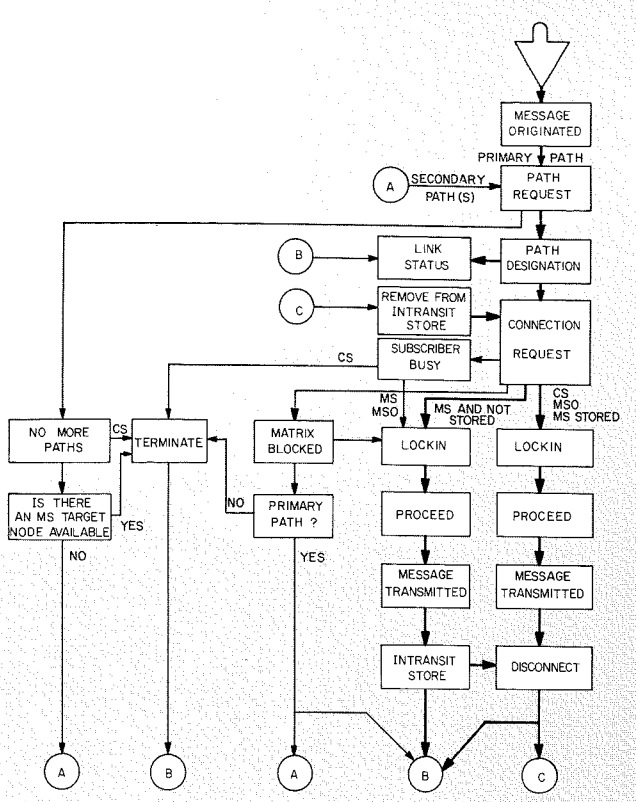

Fig. 4—Node processing flow chart.

Node processing

Fig. 4 presents a node processing flow diagram or the sequence of signalling required for a single transaction from its initiation to its completion. The paths indicated with heavy arrows represent normal operation and the other paths represent contingency paths which include:

a) Matrix blocked (insufficient node crosspoints or node outage).
b) No more paths (insufficient trunk lines or trunk outage).
c) Subscriber busy.

Normal operation

When a message has been originated, the PATH REQUEST is made to the appropriate regional node (see Fig. 4). This regional, after determining a primary path considering the existing status of the network, transmits the PATH DESTINATION to the originating node and updates the LINK STATUS (reserves the path designated for transmission). At the originating node, the path information is modified to become a CONNECTION REQUEST and is transmitted. When the terminating node receives the CONNECTION REQUEST and it is a CS or MSO message, a LOCKIN is transmitted back to the originating node, which in turn signals the subscriber to PROCEED. Following the information transfer (MESSAGE TRANSMITTED), a DISCONNECT breaks down the matrix connections and another housekeeping message is transmitted to update the LINK STATUS. For an MSO message, DISCONNECT also releases another message from INTRANSIT STORE if a message has been stored.

For MS messages, the CONNECTION REQUEST is transmitted to the responsible MS node. Upon receipt of the CONNECTION REQUEST, A LOCKIN is transmitted back to the originating node, who in turn signals the subscriber to PROCEED. The message is transmitted to the responsible MS node, stored, and placed on INTRANSIT STORE (a permanent record is made). It remains there until the completion of another call (DISCONNECT). At DISCONNECT, the oldest message is removed from INTRANSIT STORE and now represents a new CONNECTION REQUEST. This request is handled as though it were a CS or MSO message unless it encounters a MATRIX BLOCKED or BUSY SUBSCRIBER.

Contingency paths

There are three contingency paths or exceptions to normal operation; namely MATRIX BLOCKED, NO MORE PATHS, and SUBSCRIBER BUSY.

When a MATRIX BLOCKED condition occurs, the next action depends on the type of message. For CS messages or for other type messages that are blocked before an MS node, a request for a secondary PATH REQUEST is initiated. If a secondary PATH REQUEST has already been tried, the message will be lost. If the message was not a CS message and an MS node was reached, a LOCKIN is obtained and the message is transmitted from the originating node to the furtherest MS node from the originating node. The message is then stored and placed on INTRANSIT STORE.

When the termination node is reached and a SUBSCRIBER BUSY is obtained, CS messages are lost. MS and MSO messages are transmitted to the closest MS node to the termination node along the designated path. The message is stored and placed on INTRANSIT STORE. INTRANSIT STORE messages are taken out of storage and an effort is made to transmit them every time another message is completed. These messages are handled as CS messages unless problems are encountered.

When NO MORE PATHS are available, CS messages are lost. MS and MSO messages request a path to a "target" MS node. A target MS node is any MS

Table I—Simulation runs

Simulation run	Network size (note A) 1	2	Trunk capacity Limited	Unlimited	Fixed message priority percent	Fixed message destination percent	Traffic (note B) 1	2	3	4	Fixed message type percent	Message routing (note C) 1	2	Outages None	Trunk	Node	Mobility None	Subs.	Node
	System operating condition																		
A	X			X	X	X					X	X		X			X		
B		X		X	X	X	X				X	X		X			X		
C		X	X		X	X	X				X	X		X			X		
D		X	X		X	X		X			X	X		X			X		
E		X	X		X	X			X		X	X		X			X		
F		X	X		X	X	X				X	X			X		X		
G		X	X		X	X	X				X	X				X	X		
H		X	X		X	X	X				X	X		X				X	
I		X	X		X	X	X				X	X		X					X
J		X	X		X	X				X	X	X		X			X		
K		X	X		X	X	X				X		X	X			X		

Notes

A. Network size
1—16 Nodes
2—50 Nodes

B. Traffic
1—Normal
2—Reduced
3—Increased
4—Variable

C. Message routing
1—Deterministic
2—Adaptive

node in the path closer to the destination node than to the originating node. Moving the message toward the destination node tends to reduce the blocking probability and message delay in the system. If there is no available target MS node, the MS or MSO message is stored at the originating node until a path is available. If a path to a target MS node is available, the message is transmitted to the target MS node, stored, and placed on IN-TRANSIT STORE.

Simulation runs

The system operating conditions are varied in the various simulation runs to determine the effect of those changes on selected performance parameters. Table I depicts the planned simulation runs indicating the specific operating conditions to be varied. The system performance parameters which are examined in each simulation run are shown in Table II.

Results of simulation study

The results of the work described are not complete in themselves. They do, however, give useful immediate results and also permit general conclusions to be drawn.

The traffic generation program works. It is currently being used in conjunction with other programs to estimate the R-100 processors traffic handling capability. Its input variables are readily changed to represent difficult systems and operating conditions. Its output provides a chronological list of messages with all associated pertinent information as follows:

Time of message initiation
Message priority
Message type
Message origin
Message destination
Primary and secondary paths from origin to destination
Path to the nearest gateway node
Path to the responsible regional node

A signalling and supervision concept for a message- and, circuit-switched communication system was developed. The sequence and specific signalling and supervision messages utilized in control, management, and connection of subscribers are delineated. Hence, this concept is of use in the design of both hardware and programs for communication systems.

Table II—System performance parameter

Standard output

1. System operating conditions or simulation run designation (as in Table I)
2. Number of lost calls (grade of service)
3. Data Message delay time (mean and standard deviation)
4. Data Message total time thru system (mean and standard deviation)
5. Voice message total time thru system (mean and standard deviation)
6. Percent of system trunk utilization

Optional output

1. Tabular data of distributions of items in standard output
2. Lost calls versus type message
3. Traffic volume at any node
4. Message delay versus priority
5. Transit time (mean and standard deviation) from origin to destination for each type message
6. Size and distribution of queues
7. Percent occupancy of various facilities
8. Percent of messages using primary route, secondary route
9. Time after check-in when mobile subscriber or node can be located (available only on selected runs)
10. Increased traffic or increased delay as a function of routing method (available only on selected runs)

The path generation subroutine has immediate utility also. It is a routing scheme and in addition to determining paths for communication between terminals is of use in related fields such as setting up distribution systems and analyzing PERT networks. In its application here, it takes input data in the form of a matrix and generates a primary path (shortest path) and secondary paths between any two nodes. Provisions are incorporated to include an MS node in the path if required and also provisions are included to generate all paths if desired.

From the foregoing, one can conclude that the following additional results will be forthcoming:

A generalized operational program which simulates communication networks allowing the user to vary parameters and evaluate system performance.
Verification of the signalling and supervision concept.
Identification of figures of merit for the communication networks as delay times for signalling, lost call statistics, etc.

The completion of all the work will yield:

A tool to facilitate the design of communication networks (number of trunks, operational discipline)
A vehicle to demonstrate compliance or lack of compliance of communication networks with their requirements.
A guide to the solution of related problems, e.g., setting up a multiple processor configuration with its associated operational discipline and communication problems.

Basic time-sharing programs for business and long range plans

R. R. Lorentzen

A series of programs using the RCA BTSS capability can determine how changes in an individual product program will affect both that program and the entire product line. Product development programs and investments and proposed financial strategies can be evaluated for optimization of business plans and long range plans.

MUCH HAS BEEN WRITTEN[1,2,3] and spoken[4] about the concepts and practices of business planning. Kotler,[5] Dove,[6] and others have described what planning is or should be, and occasionally someone (*e.g.* Drucker[4]) comments on what planning is not. A paper by Gilmore and Brandenburg[7] gives an example of one good planning model and repeatedly suggests that the plan can be optimized by asking key questions which are intended to uncover opportunities for synergy. But there is very little in the literature to facilitate the financial analysis and evaluation of these plans. Furthermore, when one piece of data is changed (as a result of a change in the plan, or the forecasts), it is difficult to track all the ramifications of this change. The problem is compounded when several inputs are changed.

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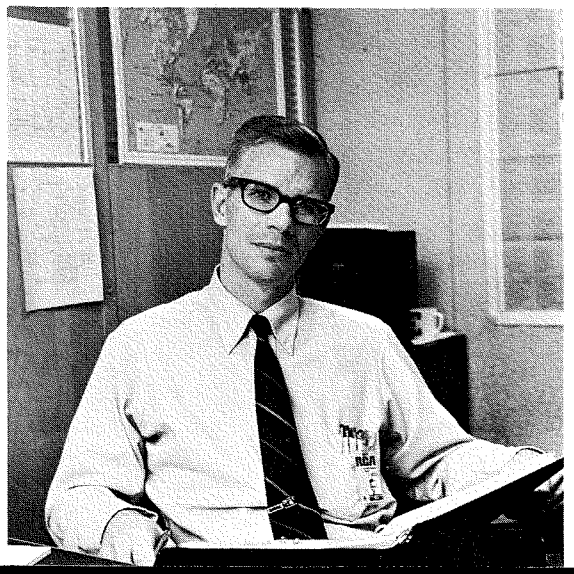
received the BSEE in 1961 and the MSEE in 1965 from Newark College of Engineering. He has also done a year of graduate work at Rutgers University. After working at Western Electric, Hewitt-Robins, and Federal Telephone and Radio, he joined what is now the RCA Microwave Devices Operations Department (MDOD) in 1956, in Equipment Development. In 1957, he entered the Microwave Applications Engineering Activity where he was responsible for resolving the technical interface problems between RCA devices and customer systems. From 1963 to 1969 he held a variety of assignments in engineering program planning, R&D Marketing, and Microwave Solid-State Engineering. Since July 1969, Mr. Lorentzen has been responsible for engineering projects planning. Mr. Lorentzen has written papers on rocketsonde transmitters and microwave solid-state sources, and is a member of Eta Kappa Nu, Tau Beta Pi, and the IEEE.



In order to deal with this situation, a series of four complementary computer programs has been developed to aid the Microwave Devices Operations Department to prepare and financially optimize its business plans and long range plans (BP/LRP). Other RCA operations within the Industrial Tube Division have also found these programs useful for this purpose.

The five key elements of this system are (See Fig. 1):

PROGRAMS—a computer program to calculate a financial analysis of individual product development programs in the BP/LRP, *i.e.* to show the relationships between the market forecast, the engineering and capital investment, the external R&D funding, and the hardware costs and margin. This program also prepares, on request, a cumulative margin to engineering ratio analysis of all programs, or any of several one-page summary reports of specific individual parameters (*e.g.*, sales, margin, or cost-to-sales ratio), showing all programs over the total time span.

PROFITS—a program to assemble all the costs and income from the product development programs, together with those not related to specific individual product programs, and to calculate and print out a Profit and Loss (P&L) analysis of the entire product line based on this data. This program also calculates the "liquidation factor" (to be discussed below) which is used to calculate the profitability of individual product programs as a function of the entire product line P&L. Hence, this program makes it possible to determine what effect a single change in any parameter will have on the product line P&L and on the P&L of each individual product program.

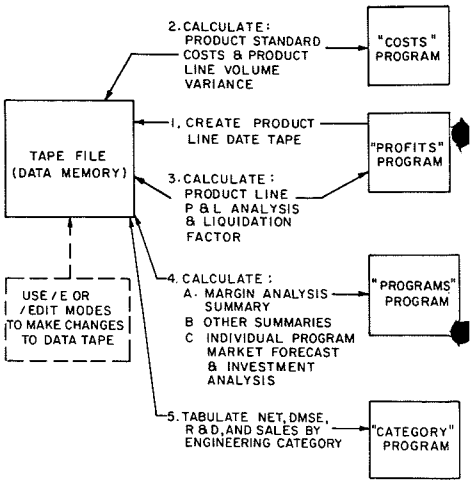


Fig. 1—The system of programs.

COSTS—a program to calculate the present and future "standard" costs of individual product programs and the volume variance (under- or over-liquidation of fixed expense) for the product line. There are three optional methods (discussed later) for calculating product costs, depending on the nature of the product and its state relative to the product life cycle.

CATEGORY—a program which tabulates the various sales and engineering investments by engineering category.

DATA MEMORY—a tape file used as the data memory to store all input data, plus the calculated data (*e.g.*, the liquidation factor or volume variance). The present data memory, has capacity for the product line data plus the data for 40 individual product programs for six years.

Purpose

Work on the development of PROGRAMS was started in 1969 in an attempt to reduce the manual arithmetic effort—and the errors—that went into putting together a financial analysis of the returns on individual product development engineering investments. These analyses related sales to investment in order to evaluate engineering projects, and also described the multi-year investment often necessary for a product development.

Additional work on engineering budgets and business plans led to an expansion of the data base to include the

non-product development aspects of a gross engineering budget in terms that were compatible with and complementary to the RCA accounting practice.

This expansion of the data base made it possible to calculate the product line P&L, and thus made it possible to analyze investments in specific product programs relative to all other programs to optimize the long range P&L for the entire product line.

Today, although these programs have undergone several major revisions to expand the purposes or to improve the algorithm, they are not in a completed final form. We in Microwave are still improving our ability to use this tool and are improving the tool in the process; the programs are a dynamic thing, constantly being improved. To fully grasp what the programs can do today, we must delve into the more intricate details of the construction of the data memory and then take a closer look at the computer programs themselves.

"Microwave disguised" example

The business programs, data, and calculations used as illustrations in this paper are taken from the author's imagination and are purposely not intended to describe the real Microwave Operation. (It is for this reason that the title chosen for the illustrative product line is "Microwave (8)—Disguised." The figure 8 represents an imaginary issue number).

Data memory

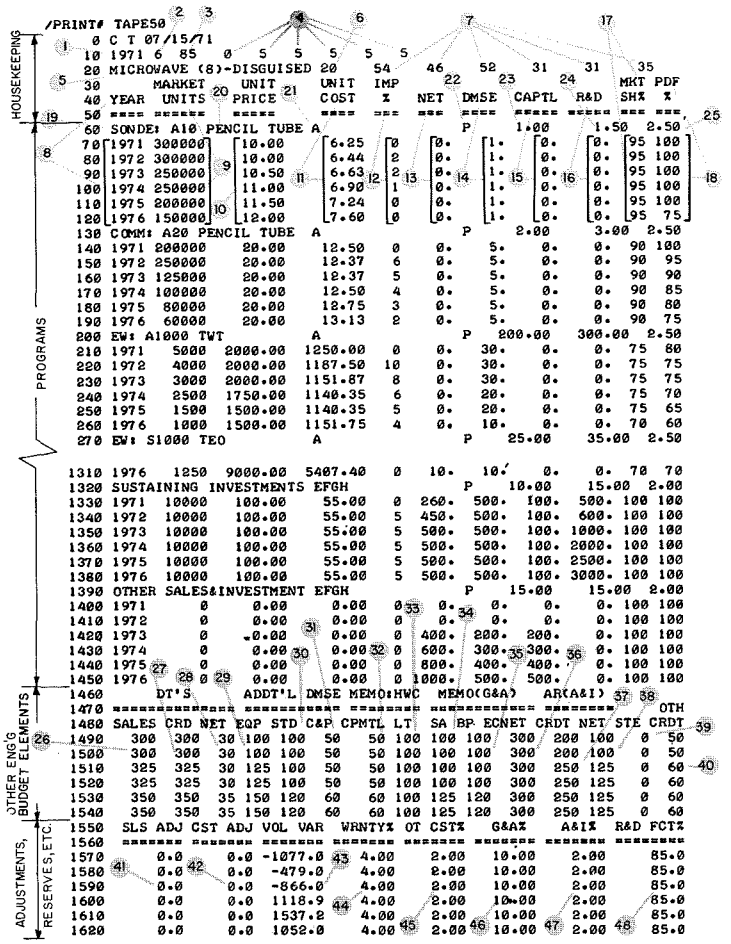
A data memory (tape file) should be constructed for each business for which we want to calculate a P&L analysis, by building up from the detail of individual product programs (a section of the PROFITS program is used to create a new data tape).

The data memory can be better visualized if we divide it into four sections (see Fig. 2):

—Housekeeping and general data.
—Programs.
—Other engineering budget elements.
—Adjustments, reserves, assessments, and R&D factor.

"Microwave disguised" example

The tape file sentinel (line 0 in Fig. 2) is the date that the data memory was created or revised. Line 10 contains




```
/PRINT# TAPE50
  0 C T 07/15/71
 10 1971 6 85   0   5   5   5   5   5
 20 MICROWAVE (8)-DISGUISED 20      54     46     52     31     31     35
 30        MARKET      UNIT            UNIT   IMP      22     23     24     MKT PDF
 40 YEAR    UNITS 20   PRICE 21        COST    %    NET   DMSE   CAPTL   R&D   SH%   %
 50 ==== ======  =====  =====  ====  ===  ===  ====  =====  =====  ===  ===
 60 SONDE: A10 PENCIL TUBE A                          P      1.00          1.50  2.50
 70 1971 300000          10.00          6.25    0     0.     1.     0.     0.   95 100
 80 1972 300000          10.00          6.44    2     0.     1.     0.     0.   95 100
 90 1973 250000          10.50          6.63    2     0.     1.     0.     0.   95 100
100 1974 250000          11.00          6.90    1     0.     1.     0.     0.   95 100
110 1975 200000          11.50          7.24    0     0.     1.     0.     0.   95 100
120 1976 150000          12.00          7.60    0     0.     1.     0.     0.   95  75
130 COMM: A20 PENCIL TUBE  A                         P      2.00          3.00  2.50
140 1971 200000          20.00         12.50    0     0.     5.     0.     0.   90 100
150 1972 250000          20.00         12.37    6     0.     5.     0.     0.   90  95
160 1973 125000          20.00         12.37    5     0.     5.     0.     0.   90  90
170 1974 100000          20.00         12.50    4     0.     5.     0.     0.   90  85
180 1975  80000          20.00         12.75    3     0.     5.     0.     0.   90  80
190 1976  60000          20.00         13.13    2     0.     5.     0.     0.   90  75
200 EW: A1000 TWT                       A              P    200.00         300.00  2.50
210 1971   5000  2000.00  1250.00    0     0.    30.     0.     0.   75   80
220 1972   4000  2000.00  1187.50   10     0.    30.     0.     0.   75   75
230 1973   3000  2000.00  1151.87    8     0.    30.     0.     0.   75   75
240 1974   2500  1750.00  1140.35    6     0.    20.     0.     0.   75   70
250 1975   1500  1500.00  1140.35    5     0.    20.     0.     0.   75   65
260 1976   1000  1500.00  1151.75    4     0.    10.     0.     0.   70   60
270 EW: S1000 TEO                       A              P     25.00         35.00  2.50

1310 1976   1250  9000.00  5407.40    0    10.    10.     0.     0.   70   70
1320 SUSTAINING INVESTMENTS EFGH                       P     10.00         15.00  2.00
1330 1971  10000   100.00    55.00    0   260.   500.   100.   500.  100  100
1340 1972  10000   100.00    55.00    5   450.   500.   100.   600.  100  100
1350 1973  10000   100.00    55.00    5   500.   500.   100.  1000.  100  100
1360 1974  10000   100.00    55.00    5   500.   500.   100.  2000.  100  100
1370 1975  10000   100.00    55.00    5   500.   500.   100.  2500.  100  100
1380 1976  10000   100.00    55.00    5   500.   500.   100.  3000.  100  100
1390 OTHER SALES&INVESTMENT EFGH                       P     15.00         15.00  2.00
1400 1971      0     0.00     0.00    0     0.     0.     0.     0.  100  100
1410 1972      0     0.00     0.00    0     0.     0.     0.     0.  100  100
1420 1973      0     0.00     0.00    0   400.   200.   200.     0.  100  100
1430 1974      0     0.00     0.00    0   600.   300.   300.     0.  100  100
1440 1975      0     0.00     0.00    0   800.   400.   400.     0.  100  100
1450 1976      0     0.00     0.00    0  1000.   500.   500.     0.  100  100
1460          DT'S      ADDT'L  DMSE MEMO:HWC    MEMO(G&A)    AR(A&I)                OTH
1470 ============ ========== ======= ========== ========== ========
1480 SALES CRD NET EQP STD C&P CPMTL LT  SA BP ECNET CRDT NET STE CRDT
1490  300  300  30 100 100  50   50 100 100 100  300  200 100   0  50
1500  300  300  30 100 100  50   50 100 100 100  300  200 100   0  50
1510  325  325  30 125 100  50   50 100 100 100  300  250 125   0  60
1520  325  325  30 125 100  50   50 100 100 100  300  250 125   0  60
1530  350  350  35 150 120  60   60 100 125 120  300  250 125   0  60
1540  350  350  35 150 120  60   60 100 125 120  300  250 125   0  60
1550 SLS ADJ CST ADJ VOL VAR  WRNTY% OT CST%   G&A%     A&I%  R&D FCT%
1560 ======= ======= ======= ======= ======= ======= ======= ========
1570      0.0     0.0 -1077.0    4.00    2.00   10.00    2.00   85.0
1580      0.0     0.0  -479.0    4.00    2.00   10.00    2.00   85.0
1590      0.0     0.0  -866.0    4.00    2.00   10.00    2.00   85.0
1600      0.0     0.0  1118.9    4.00    2.00   10.00    2.00   85.0
1610      0.0     0.0  1537.2    4.00    2.00   10.00    2.00   85.0
1620      0.0     0.0  1052.0    4.00    2.00   10.00    2.00   85.0
```

Fig. 2—The data memory (tape file) for "Microwave Disguised"—example.

the first year for the data **1**, the number of years **2**, the slope of the learning curve used in cost calculations **3**, and the inflation factors used for each year **4**, (0% in 1971, 5% per year thereafter). Line 20 contains the product line title (including the issue number) **5**, the number of programs contained in the data **6**, and the liquidation factors calculated for each year **7**. Lines 30 thru 40 contain column headings to aid the user in reading the following data within the individual programs: the year **8**, the most likely market units **9**, planned unit price **10**, calculated unit standard cost **11**, the factory's estimate of the productivity improvement factor to be applied to the previous year's standard cost **12**, the RCA product development, IR&D, or NET engineering **13**, the Direct Manufacturing Support Engineering (DMSE) or sustaining effort necessary for the program **14**, the capital investment in facilities required **15**, the (plant level) R&D credits expected **16**, the RCA share of the total market in the most likely market units **17**, and the program discount factor **18**—essentially an overall confidence factor that the events identified in that year will, in fact, happen as described by that line. Most of these terms should be self-explanatory. Further discussion of the Productivity Improvement Factor and the Program Discount Factor (PDF) is postponed until more appropriate sections of the text below. Now let's look at the business programs themselves.

Product programs

In the example, each product program contains seven lines of data—a title/cost data line and six lines representing six years (in this example) of the data described above. These programs are the heart of the data memory and the plan.

A typical program, No. 9, is found in sequence numbers 620-680 (see Fig. 3). The Title/Cost data line, line 620, contains the market **19**, the product

```
620 RADAR: SS MODULES      B                    L   500.00   500.00  4.00
630 1971     0     0.00     0.00    0   250.    0.   100.   500.    0 100
640 1972  1000  5000.00  3487.82    0   200.  100.   100.   400.  100  60
650 1973  1500  4500.00  2535.80    0    20.   50.     0.   250.   80  60
660 1974  2000  4000.00  2289.53    0     0.   20.     0.     0.   80  60
670 1975  2500  4000.00  2150.80    0     0.   20.     0.     0.   80  50
680 1976  2500  4000.00  2078.44    0     0.   20.     0.     0.   80  50
```

Fig. 3—Program No. 9 as contained in the Data Memory—example.

20, the engineering category* A thru H, **21**, as defined by Dr. Hillier and his staff; the cost basis, **22**, or method to be used in calculating unit standard costs (see below), the material content ($) of the cost **23**, the labor content ($) of the cost **24**, and the overhead rate **25**—*i.e.*, ratio of expense to labor, associated with the cost. Both the material and labor are in today's dollars. Items **22** thru **25** will be discussed under the COSTS program.

As we proceed into the year-by-year data of our typical program, we should become aware of the relationships between the sales and the investments. First, the product development effort ($250K NET—1971), and in this case substantial capital investment and external R&D funding (also product development), precedes the first hardware sales. (Unfortunately, we can't see 1970 in this data, but there was probably some product development effort in 1970 also). Analyses conducted by the author suggests that the engineering investment in specific product development typically leads the resulting hardware sales by one to three years and sometimes as much as five years. As the production builds up, the planned NET engineering decreases, but factory support engineering expenditure ($100K in 1972 to $20K in 1976) is planned to transfer the design to production and to provide for production engineering and cost reduction effort.

Also note that the "most likely" sales —the sales that will happen if everything goes according to our plan—are obtained by multiplying the total market units, the unit price, and the market share.

In addition to the specific product programs which are already identified in the business plan, additional product programs can be entered for other "present," "next generation," or "future generation" product sales and their associated investment. Investments which are in addition to those specifically related to product development, *i.e.*, those investments which are of a "sustaining," "general support technology," or "feasibility development" nature can be entered as separate programs with appropriate titles (these programs would show no product sales).

Other engineering budget elements

Lines 1460-1540 in our example (Fig. 2) represent six years of data for additional elements of the engineering budget. The first three columns are the sales **26**, credits **27**, and NET engineering for the Developmental Type (DT) product **28**. DT's are small quantity items, generally variants of existing designs, which require some engineering, and are therefore built in engineering rather than manufacturing. The next three columns, equipment development engineering **29**, standardizing **30**, and chemical and physical laboratory analysis **31** are additional services which are elements of Manufacturing Support Engineering. The chemical and physical material analysis for the purchasing activity **32**, and the life test expenditure **33** are entered into the hardware cost and therefore are shown as memos. In a similar manner sales assistance to marketing **34**, Bids and Proposals preparation **35**, and division engineering **36** are memo items that appear in the General and Administrative divisional assessments. The Applied Research credits **37** are a memo which appears in corporate assessments and interest, but the NET engineering to support the applied research program **38** is included in the calculation of the product line P&L. The last two elements are special test equipment engineering financed external to RCA **39**, and other credits, *i.e.*, work for other activities within the Industrial Tube Division **40**.

Adjustments, reserves, assessments, and R&D factor

Lines 1570-1620 in our example (Fig. 2) represent six years of data.

The inputs are sales **41** and costs adjustments **42** to account for minor differences between other records such as actuals without having to go back and force the detail. Other inputs are the calculated volume variance **43**, the warranty reserve **44**, and other costs **45** as a percent of hardware sales; the divisional General and Administrative (G&A) Assessments **46** and corporate Assessments and Interest (A&I) **47** as a percent of total sales; and the R&D factor (credits, or costs, to sales ratio)

*The Engineering Categories are:
Product Sales and Engineering
A = Present product
B = Next generation product
C = Future generation product
D = New product ventures
Engineering only
E = Sustaining engineering
F = General support engineering
G = Feasibility development engineering
H = Unidentified

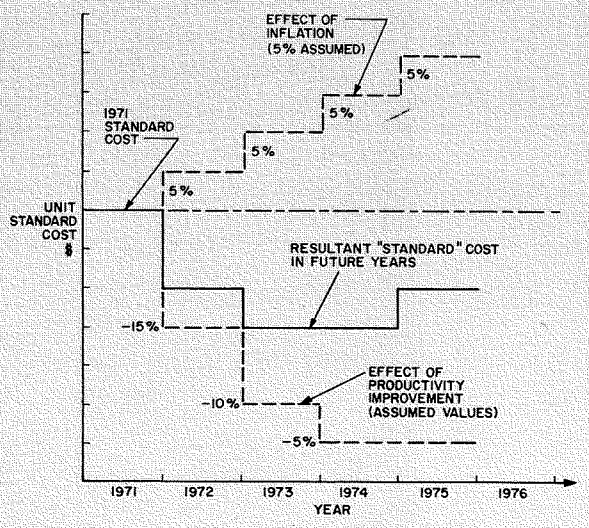


Fig. 4—Productivity improvement cost calculation.

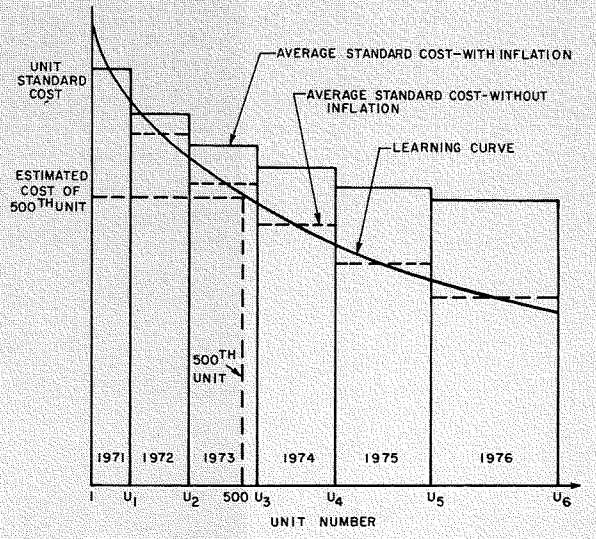


Fig. 5—Modified learning curve cost calculation.

48 which is used to calculate the R&D sales from the R&D Credits.

The data in this tape file are used in the computer programs.

COSTS

The COSTS program reads through the data memory and calculates the unit standard cost for each program, in each year. It stores these unit costs in the data tape and calculates the volume variance.

Standard cost calculations

As noted above, there are three methods of calculating the unit standard costs. The specific cost basis to be used for each program is recorded in the program title/cost basis line in the data memory (tape file). The three alternative methods are:

—Productivity Improvement Calculation. If the cost basis is shown as a "P", the material, labor, and overhead rate are combined to give the current year standard cost. The costs in future years are simply (Fig. 4)

$$cost(year\ N) = cost[year\ (N-1)] \times [1 + (inflation - productivity\ improvement)/100] \quad (1)$$

—Modified Learning Curve Calculation. If the cost basis is an "L", the material, labor, and overhead rate are the estimated values for the 500th unit, in today's dollars. The 500th unit is chosen to get away from the wide variations that often occur in the costs of the earliest units. The costs of individual units are assumed to follow the typical equation

$$Y = AX^B \text{ or (see Fig. 5)}\quad Costs = A \times unit^B \quad (2)$$

where

$A = cost\ of\ 500th\ unit/500^B$, a constant

$B = \log_{10}(slope)/\log_{10}(2)$, a constant

Thus the cost of the 500th unit is used to "calibrate" the cost (or learning) curve. The cost in the first year of production is obtained by going back on the learning curve to the first unit, adding up all the unit costs through the last unit in that year, and then calculating an average cost. The cost in next year begins with the cost of the first unit in that year, and so on through all the units in that year. Subsequent years follow the same approach. In addition to working with individual unit costs, the learning curve is further modified by the fact that each year beyond the current year the unit costs are increased from the learning curve by the compounded inflation factor, *i.e.*, the learning curve itself is assumed to be inflation-free.

Modified Learning Curve With Prior Experience Calculation. If the cost basis on the program title/cost data line is identified by an "E", then the unit standard cost is calculated in the same way as the Modified Learning Curve method, except that instead of going back to unit one, the first year cost calculation begins at the next unit after the "prior experience" in units. This prior experience number is recorded in the field immediately preceding the "E" in the program title/cost data line in the data memory.

This cost basis is used for new products which are similar to current products, *i.e.*, when the use of the early portion of the learning curve would produce rapid changes in learning which we know by experience will not happen.

Volume variance calculations

The philosophy behind the volume variance is simple. The unit costs calculated above assume an overhead rate, *i.e.*, an expense burden. Some portion of the actual expense is fixed and some portion is assumed to vary approximately linearly with load. If we can identify the portion of the expense that is variable, and manage our manufacturing centers to maintain this variable expense "standard" (ratio of expense to labor) independent of load fluctuations, then the expense portion of the manufacturing load after the variable expense has been subtracted is left to liquidate the actual fixed expense of the manufacturing activity. The difference between the fixed expense and the remaining "liquidating" expense is the *volume variance* (Fig. 6). Mathematically we have

$$\Sigma\ costs = \Sigma\ material\ \$ + \Sigma\ labor\ \$ + \Sigma\ liquidating\ expense\ \$ \quad (3)$$

where

$$\Sigma\ liquidating\ expense\ \$ = \Sigma\ variable\ expense\ \$ + \Sigma\ remaining\ liquidating\ expense\ \$ \quad (4)$$

but

$$\Sigma\ actual\ expense\ \$ = \Sigma\ variable\ expense\ \$ + \Sigma\ fixed\ expense\ \$ \quad (5)$$

therefore, if we let

$$volume\ variance = \Sigma\ liquidating\ expense\ \$ - \Sigma\ actual\ expense\ \$$$

then from (4) and (5).

MICROWAVE (8)-DISGUISED

YEAR	1971	1972	1973	1974	1975	1976
TOTAL COST $K	13327.	15748.	13899.	22238.	25152.	24685.
MATERIAL $K	2216.	2689.	2418.	4012.	4679.	4754.
%	0.17	0.17	0.17	0.18	0.19	0.19
LABOR $K	3196.	3568.	3087.	4583.	5096.	4975.
%	0.24	0.23	0.22	0.21	0.20	0.20
EXPENSE $K	7915.	9491.	8394.	13643.	15377.	14957.
%	0.59	0.60	0.60	0.61	0.61	0.61
EXPENSE/LABOR	2.48	2.66	2.72	2.98	3.02	3.01
VARIABLE EXPENSE $K	6392.	7135.	6173.	9167.	10193.	9949.
REMAIN.LIQUID.EXP $K	1523.	2356.	2221.	4476.	5184.	5008.
FIXED EXPENSE	2680.	2835.	3087.	3357.	3647.	3956.
VOLUME VARIANCE $K	-1077.	-479.	-866.	1119.	1537.	1052.
ACTUAL EXPENSE/LABOR FOR ZERO VOLUME VARIANCE	2.81	2.79	3.00	2.73	2.72	2.80

Fig. 6—Volume variance calculation—example.

$$volume\ variance = \Sigma\ remaining\ liquidating\ expense\ \$ - \Sigma\ fixed\ expense\ \$ \quad (6)$$

The fixed expense is entered in today's dollars and is then marked up in the program by inflation in future years.

PROFITS

The PROFITS program takes the revenue, cost, and investment information contained in the data memory, in all the programs, and in the additional detail, and calculates a Profit and Loss Analysis (Fig. 7) for the entire product line. It picks up the contribution of each element in the data and adds it to the proper place in the P&L.

The sales, costs, DMSE, and capital investment of each program in each year are factored down by the associated "program discount factor."

Program discount factor

It is well known that in most busi-

PRODUCT LINE: MICROWAVE (8)-DISGUISED

YEAR	1971	1972	1973	1974	1975	1976
HARDWARE INCOME	22805.	24192.	20960.	29279.	36618.	37100.
R & D INCOME	3353.	2800.	2294.	2706.	2941.	3529.
TOTAL INCOME	25558.	26992.	23254.	31985.	39559.	40630.
HARDWARE COST	13627.	16047.	14223.	22564.	25503.	25035.
R & D COST	2850.	2380.	1950.	2300.	2500.	3000.
TOTAL COST	16477.	18427.	16173.	24864.	28003.	28035.
HARDWARE MARGIN	8577.	8145.	6736.	6715.	11115.	12065.
% TO HRDWE SALES	38.6	33.7	32.1	22.9	30.4	32.5
R & D MARGIN	503.	420.	344.	406.	441.	529.
"GROSS MARGIN"	9080.	8565.	7080.	7121.	11556.	12595.
VOLUME VARIANCE	-1077.	-479.	-866.	1119.	1537.	1052.
NET ENG	1500.	1495.	1485.	1415.	1560.	1670.
% TO TOTAL SALES	5.9	5.5	6.4	4.4	3.9	4.1
DMSE(SUSTAINING)	797.	1067.	1870.	1423.	1465.	1483.
% TO HRDWE COSTS	5.8	6.7	8.9	6.3	5.7	5.9
TOT ENGINEERING	2297.	2562.	2755.	2838.	3025.	3153.
WARRANTY	888.	968.	838.	1171.	1465.	1484.
% TO HRDWE SALES	4.0	4.0	4.0	4.0	4.0	4.0
OTHER COSTS	444.	484.	419.	586.	732.	742.
% TO HRDWE SALES	2.0	2.0	2.0	2.0	2.0	2.0
GROSS MARGIN	4374.	4072.	2202.	3645.	7871.	8267.
% TO TOTAL SALES	17.1	15.1	9.5	11.4	19.9	20.3
G & A	2556.	2699.	2325.	3199.	3956.	4063.
% TO TOTAL SALES	10.0	10.0	10.0	10.0	10.0	10.0
CORPORATE A & I	511.	540.	465.	640.	791.	813.
% TO TOTAL SALES	2.0	2.0	2.0	2.0	2.0	2.0
PRETAX PROFIT	1307.	833.	-589.	-193.	3124.	3392.
% TO TOTAL SALES	5.1	3.1	-2.5	-0.6	7.9	8.3

Fig. 7—Microwave profit and loss analysis—example.

MICROWAVE (8)-DISGUISED

MEMOS:

GROSS ENG'G	6377.	6172.	6020.	6453.	6925.	7553.
PROGRAM DMSE	547.	617.	995.	1148.	1135.	1153.
CAPITAL	515.	543.	559.	561.	520.	605.
LIQUIDATION F. %	54	46	52	31	31	35
LIQUIDATION C/S	0.65	0.68	0.66	0.76	0.76	0.74
BREAKEVEN RATE %	45	37	39	23	24	27
BREAKEVEN C/S	0.69	0.73	0.72	0.81	0.81	0.79

Fig. 8—Memos report—example.

YEAR: 1974

PROGRAM		TOTAL MKT $K	RCA SH%	RCA SALES	STD MARG	NET	DMSE	CAP	PDF %	CUM M/E
SONDE: A10 PENCIL TUBE	A	2750.	95	2612.	974.	0.	1.	0.	100	
.994E+03										
COMM: A20 PENCIL TUBE	A	2000.	90	1800.	675.	0.	5.	0.	85	
.634E+03										
EW: A1000 TWT	A	4375.	75	3281.	1143.	0.	20.	0.	70	76.0
EW: S1000 TEO	A	2000.	70	1400.	677.	0.	5.	0.	55	79.9
NAV: A30 PT XPNDR	A	1000.	60	600.	-25.	0.	10.	0.	70	16.5
RADAR: A2000 MAGNETRON	A	3150.	100	3150.	76.	0.	5.	0.	90	
.273E+03										
MISSILE: SS LOCAL OSC	B	3600.	80	2880.	1248.	0.	25.	25.	65	5.2
COMM: A3000 TWT	B	900.	50	450.	73.	0.	20.	0.	60	0.2
RADAR: SS MODULES	B	8000.	80	6400.	2737.	0.	20.	0.	60	6.9
EW: A4000 TWT	B	2900.	80	2320.	568.	10.	20.	0.	60	2.5
NAV: A40 PT XPNDR	B	450.	70	315.	13.	0.	10.	0.	70	-0.2
SONDE: SS MODULES	B	500.	90	450.	296.	0.	20.	20.	70	0.8
EW: PHASED ARRAY MODULE	C	800.	80	640.	278.	50.	50.	0.	80	1.1
EW: NEW SUBSYSTEM	C	5000.	100	5000.	-1409.	20.	100.	20.	70	-2.5
COMM: SS LOCAL OSC	C	500.	75	375.	93.	10.	30.	30.	70	0.4
RADAR: DOPPLER MODULE	C	400.	70	280.	59.	20.	40.	40.	65	0.2
NAV: SS XPNDR	C	400.	80	320.	70.	0.	20.	0.	70	0.4
MISSLE: GUIDANCE LO SS	C	10000.	70	7000.	1503.	50.	100.	100.	70	1.6
SUSTAINING INVESTMENTS	E	1000.	100	1000.	450.	500.	500.	100.	100	0.5
OTHER SALES&INVESTMENT	E	0.	100	0.	0.	600.	300.	300.	100	0.0
DT'S	B	325.		325.	0.	30.				
ADJUSTMENTS		0.		0.	0.					
TOTALS-SALES:		50050.		40599.	9498.					
-INVESTMENTS:						1290.	.130E+04	635.		
3.7										

Fig. 9—Long range plan data summary—margin analysis report—example.

LONG RANGE PLAN DATA SUMMARY MICROWAVE (8)-DISGUISED 07/23/71

COSTS/SALES

YEAR:		1971	1972	1973	1974	1975	1976
SONDE: A10 PENCIL TUBE	A	0.62	0.64	0.63	0.63	0.63	0.63
COMM: A20 PENCIL TUBE	A	0.62	0.62	0.62	0.62	0.64	0.66
EW: A1000 TWT	A	0.62	0.59	0.58	0.65	0.76	0.77
EW: S1000 TEO	A	0.59	0.56	0.53	0.52	0.51	0.51
NAV: A30 PT XPNDR	A	0.60	0.73	0.99	1.04	1.09	1.15
RADAR: A2000 MAGNETRON	A	0.59	0.69	0.81	0.98	1.10	1.25
MISSILE: SS LOCAL OSC	B	0.00	0.83	0.59	0.57	0.53	0.50
COMM: A3000 TWT	B	0.00	1.23	0.86	0.84	0.80	0.79
RADAR: SS MODULES	B	0.00	0.70	0.56	0.57	0.54	0.52
EW: A4000 TWT	B	0.00	0.86	0.79	0.76	0.74	0.73
NAV: A40 PT XPNDR	B	0.00	1.77	1.14	0.96	0.94	0.77
SONDE: SS MODULES	B	0.00	0.56	0.37	0.34	0.53	0.58
EW: PHASED ARRAY MODULE	C	0.00	0.00	0.91	0.57	0.67	0.92
EW: NEW SUBSYSTEM	C	0.00	0.00	0.00	1.28	0.79	0.75
COMM: SS LOCAL OSC	C	0.00	0.00	1.09	0.75	0.70	0.66
RADAR: DOPPLER MODULE	C	0.00	0.00	1.12	0.79	0.80	0.83
NAV: SS XPNDR	C	0.00	0.00	0.95	0.78	1.01	1.01
MISSLE: GUIDANCE LO SS	C	0.00	0.00	1.57	0.79	0.62	0.60
SUSTAINING INVESTMENTS	E	0.55	0.55	0.55	0.55	0.55	0.55
OTHER SALES&INVESTMENT	E	0.00	0.00	0.00	0.00	0.00	0.00
TOTALS		0.61	0.66	0.68	0.77	0.70	0.67

LONG RANGE PLAN DATA SUMMARY MICROWAVE (8)-DISGUISED 07/23/71

COSTS/SALES

YEAR:		1971	1972	1973	1974	1975	1976
SONDE: A10 PENCIL TUBE	A						
COMM: A20 PENCIL TUBE	A						0.77
EW: A1000 TWT	A						
EW: S1000 TEO	A						
NAV: A30 PT XPNDR	A		0.73	0.99	1.04	1.09	1.15
RADAR: A2000 MAGNETRON	A		0.69	0.81	0.98	1.10	1.25
MISSILE: SS LOCAL OSC	B		0.83				
COMM: A3000 TWT	B		1.23	0.86	0.84	0.80	0.79
RADAR: SS MODULES	B		0.70				
EW: A4000 TWT	B		0.86	0.79			
NAV: A40 PT XPNDR	B		1.77	1.14	0.96	0.94	0.77
SONDE: SS MODULES	B						
EW: PHASED ARRAY MODULE	C			0.91			0.92
EW: NEW SUBSYSTEM	C				1.28	0.79	0.75
COMM: SS LOCAL OSC	C			1.09			
RADAR: DOPPLER MODULE	C			1.12	0.79	0.80	0.83
NAV: SS XPNDR	C			0.95	0.78	1.01	1.01
MISSLE: GUIDANCE LO SS	C			1.57	0.79		
SUSTAINING INVESTMENTS	E						
OTHER SALES&INVESTMENT	E						
TOTALS		0.61	0.66	0.68	0.77	0.70	0.67
LIQUIDATION C/S		0.65	0.68	0.66	0.76	0.76	0.74

Fig. 10—Long range plan data summary—cost/sales reports—example.

nesses, not all product investments prove successful.[8,9] Every program will not have the market develop as described, or have complete success in the product development or manufacturing programs, or meet all its sales, margin, and profit objectives.

A program discount factor weights some of the inputs to the P&L analysis; this factor describes the contribution that each program makes to the total sales and costs of the business plan/long range plan. The PDF is not applied to the NET engineering based on the rationale that if NET funds are committed to a product development program they will be spent. Since there is less certainty that the sales and the other related costs and investments will actually occur, the PDF is applied to these terms. In other words, if the product is developed but the order doesn't get booked, the production-related costs won't be incurred. Admittedly this is an over-simplification, but over many programs it makes reasonable allowances for uncertainties.

Liquidation factor

In the PROGRAMS program, the profit of individual product programs is calculated by marking up the hardware cost to break even and then substracting this break-even cost from the program income (*i.e.*, from the hardware sales). The factor used to mark up the hardware cost (without DMSE) to break-even is called the liquidation factor, LF. The term "break-even factor" has been purposely avoided because this term is often reserved for a different base—hardware standard cost plus DMSE. The break-even factor is also calculated in this program. Thus the liquidation factor answers the question—"What must the hardware sales be as a function of the hardware cost for the product line to break even?"

From the P&L Analysis we can now derive an expression for the LF.

$$Pretax\ Profit = \Sigma\ income - \Sigma\ costs \tag{7}$$

$$\Sigma\ income = R\&D\ sales + hardware\ sales \tag{8}$$

$$\Sigma\ costs = R\&D\ costs + hardware\ standard\ costs - volume\ variance + NET + DMSE + warranty + other\ costs + G\&A + A\&I \tag{9}$$

At break-even we have

$$Pretax\ Profit = 0. \tag{10}$$

$$Hardware\ Sales = (1 + LF/100) \times hardware\ standard\ cost \tag{11}$$

From (7) and (10) we have

$$\Sigma\ income = \Sigma\ costs \tag{12}$$

or

$$R\&D\ sales + (1 + LF/100) \times hardware\ standard\ cost = R\&D\ cost + hardware\ standard\ cost - volume\ variance + NET + DMSE + warranty + other\ costs + G\&A + A\&I \tag{13}$$

or, since

$$R\&D\ sales = R\&D\ cost + R\&D\ margin$$

we have the desired expression for the LF:

$$(LF/100) \times hardware\ standard\ cost = NET + DMSE + warranty + other\ costs + G\&A + A\&I - volume\ variance - R\&D\ margin \tag{14}$$

Memos

The liquidation factor and the break-even rate (using hardware standard cost plus DMSE as a base), are printed out as memo reports (Fig. 8) since they do not enter directly into the P&L analysis. Also available is a summation of the portion of DMSE (weighted) contained in the individual business programs (*i.e.*, excluding the services such as equipment development), a summation of the gross engineering (including all credits), and a summation of the "weighted" capital investment. Both the DMSE and capital are "weighted" by the program discount factors.

The calculated liquidation factor is stored in the data memory for use in PROGRAMS.

PROGRAMS

This program has three sections, each producing a different report with a specific purpose:

- —A "Margin Analysis" summary report for all programs.
- —Other "Long Range (*i.e.* multi-year) Plan Data Summary," reports of individual parameters, or results, for all programs.
- —"Microwave Market Forecast and Investment Analysis" reports for individual programs.

Long range plan data summary—margin analysis report

The margin analysis report (Fig. 9) tabulates the sales without the program discount factor applied, margin, and investment of all programs in a given year and calculates a weighted, cumulative, margin-to-engineering ratio according to the expression

$$\text{Cumulative}\frac{\text{Margin}}{\text{Eng'g}} = \frac{\Sigma\ (\text{RCA sales} \cdot \text{PDF}/100)}{\Sigma\ \text{Net} + \Sigma\ (\text{DMSE} \cdot \text{PDF}/100)} \qquad (15)$$

following the philosophy and logic discussed earlier.

The report therefore gives a convenient way of beginning to rank and select programs to optimize the business plan/long range plan.

Other long range plan data summary reports

Whereas the "margin analysis" report prints several pieces of related information for a given year on each page, the other summary reports all print only one parameter in a matrix of all programs versus all years in the plan. They are therefore useful for quickly looking at trends. The reports currently available are

- —Sales—BP/LRP (RCA share×program discount factor)
- —Sales—RCA Share
- —Sales Potential—total market
- —Costs—BP/LRP (RCA Share×program discount factor)
- —Units—RCA share
- —Units—BP/LRP (RCA Share×program discount factor)
- —Unit cost
- —Costs/sales ratio
- —Costs/sales ratio (suppressed printout)
- —Standard margin—RCA share (hardware income—standard cost without DMSE)

Each of these has its own purpose, of course. The cost/sales ratio (Fig. 10) and the suppressed printout cost/sales ratio reports are the same, except that the latter report tests the cost/sales ratio against the liquidation (*i.e.*, break-even) costs/sales ratio, and prints out only those values that exceed this test—the poorest programs—in order to highlight those areas that need attention first.

Microwave market forecast and investment analysis

This analysis gathers together all of the data on a given individual program in a one page summary (Fig. 11). The first section describes the "most likely" market conditions and the RCA market share goal; this is followed by the expected *hardware procurement* schedule, if all goes as planned, and price and cost information. The *financial analysis* then reports the margin and pretax profit (using the liquidation factor). This is followed by the *investment* section. These investments are not modified by the program discount factor; they describe the investment necessary to support the "most likely" sales shown above. (This factor is applied later).

In the *ratio/program discount analysis* section two fundamental ratios are calculated, and the analysis using the program discount factor is presented. In essence the PDF is used to "weight" the non-discounted results shown in earlier sections of the report. (As a general rule, when the program discount factor appears in a report, the data presented before is "free" of the PDF, while the data appearing after it will be discounted by this factor).

The final section of the report states the planned R&D funding expected from non-RCA sources.

This comprehensive report gives a good financial summary of the merits of a given program and provides a starting point for improving the performance.

PRODUCT LINE: MICROWAVE (8)-DISGUISED

PROGRAM TITLE: RADAR: SS MODULES B PROG. NO. 9

YEAR	1971	1972	1973	1974	1975	1976
TOTAL MRT-UNITS	0	1000	1500	2000	2500	2500
TOTAL MARKET $K	0.0	5000.0	6750.0	8000.0	10000.0	10000.0
RCA SHARE %	0	100	80	80	80	80
HARDWARE PROCUREMENT SCHEDULE						
UNITS	0	1000	1199	1599	1999	1999
AVG PRICE ($)	0.00	5000.00	4500.00	4000.00	4000.00	4000.00
AVG MFG COST ($)	0.00	3487.82	2535.58	2289.53	2150.20	2078.44
FINANCIAL ANALYSIS ($000'S)						
TOTAL INCOME	0.0	5000.0	5400.0	6400.0	8000.0	8000.0
TOT COST WO DMSE	0.0	3487.8	3043.0	3663.2	4300.4	4156.9
STANDARD MARGIN	0.0	1512.2	2357.0	2736.7	3699.6	3843.1
LIQUIDATION F. %	54	46	52	31	31	35
TOT BRKEVEN COST	0.0	5092.2	4625.3	4798.5	5633.5	5611.6
PRETAX PROFIT	0.0	-92.2	774.7	1601.1	2366.5	2388.2
CUM INCOME	0.0	5000.0	10400.0	16800.0	24800.0	32800.0
CUM COST	0.0	3487.8	6530.8	10194.0	14494.4	18651.3
CUM MARGIN	0.0	1512.2	3869.2	6606.0	10305.6	14148.7
CUM PTP	0.0	-92.2	682.5	2283.6	4650.1	7038.3
INVESTMENT ($000'S)						
NET(PRODUCT) ENG	250.0	200.0	20.0	0.0	0.0	0.0
DMSE(SUSTAINING)	0.0	100.0	50.0	20.0	20.0	20.0
ENG'G (NET+DMSE)	250.0	300.0	70.0	20.0	20.0	20.0
CAPITAL	100.0	100.0	0.0	0.0	0.0	0.0
CUM ENGINEERING	250.0	550.0	620.0	640.0	660.0	680.0
CUM CAPITAL	100.0	200.0	200.0	200.0	200.0	200.0
RATIOS/PROGRAM DISCOUNT ANALYSIS						
COST/SALES	0.000	0.698	0.564	0.572	0.536	0.520
CUM COST/CUM INC	0.000	0.698	0.628	0.607	0.584	0.569
PROG DISC FCTR %	100	60	60	60	50	50
STANDARD MARGIN	0.0	907.3	1414.2	1642.0	1849.8	1921.6
PRETAX PROFIT	0.0	-55.3	464.8	960.7	1183.2	1194.1
ENG'G (NET+DMSE)	250.0	260.0	50.0	12.0	10.0	10.0
CAPITAL	100.0	100.0	0.0	0.0	0.0	0.0
CUM MARG/CUM ENG	0.000	1.779	4.146	6.929	9.989	13.066
CUM PRFT/CUM CAP	0.000	-0.346	2.559	8.564	15.959	23.488
R & D FUNDING SCHEDULE ($000'S)						
R & D FUNDING	500.0	400.0	250.0	0.0	0.0	0.0

Fig. 11—Microwave market forecast and investment analysis—program no. 9—example.

Conclusions

The series of four programs described use the RCA BTSS computer capability to optimize a business plan or long range plan. The programs make it possible to evaluate the effects that changes in an individual product program have on that program and on the performance of the entire product line. This capability is valuable not only for evaluating product development programs and investments, but also for evaluating financial strategies suggested for proposals and quotations.

The programs depend on rather simple models of the business, and because of the many revisions probably do not use the most efficient programming approach. But they do perform a task that was not possible before, and they are constantly being improved as new elements of the business are added, debugged, modified, and optimized.

A word of caution is in order, however. The results obtainable with this tool are only as good as the input data, the strategy, and the commitment to that strategy. Financial manipulation is no substitute for decisive, timely, well-planned action, but it *can* be a healthy complement to such action.

Acknowledgments

The author wishes to acknowledge gratefully the valuable contributions of W. G. Hartzell (on business models) and J. F. Kucera (on program plans/investment analysis) from the Microwave Devices Operations Department, in Harrison, and from C. C. Simeral (on business models) and W. T. Kelley (on application and prove out of the programs and for learning curve suggestions) from the Industrial Tube Division, Lancaster.

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Low-power COS/MOS memory system design

J. R. Oberman|G. J. Waas

COS/MOS devices can provide reliable, high-speed memory systems with low power dissipation. Two specific applications show the trade-offs that must be considered in designing such systems.

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received the BSEE and the MSEE from the University of Pennsylvania in 1958 and 1965, respectively. Mr. Oberman, joined RCA in 1958, as a specialized trainee and eventually was assigned to Central Engineering in Camden. Here, he was engaged in the development of packaging concepts for electronic equipment. In 1960, he transferred to Computer Systems, where he was associated with the memory design for many of RCA's commercial computers. Mr. Oberman was the project engineer responsible for the RCA Spectra 70/45 ROM's design. In 1970, he joined the Solid State Technology Center at Somerville.

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received the BSEE from City College of New York in 1949 and the MSEE from the University of Pennsylvania in 1964. Prior to joining RCA, Mr. Waas worked for Teletone and CBS-Columbia. In 1957, he joined the Computer Systems and in 1961 was named Manager of the Memory and Circuits Group. In this capacity, he was responsible for the memory design of the RCA 501 computer and the memory and circuit designs for the RCA 301, 601, 3301, and Spectra 70 computers. In 1966, Mr. Waas was appointed Manager, Computer Equipment Engineering and assumed responsibility for memories, packaging, and power supplies for te Spectra 70 computer series. In 1968, he was named Manager, Memory System Coordination at the David Sarnoff Research Center. In 1970, Mr. Waas joined the Solid State Division in Somerville. Mr. Waas is a Licensed Professional Engineer in the State of New York.

Authors Waas (left) and Oberman.

SEMICONDUCTOR MEMORY STORAGE is a rapidly growing segment of the total memory market, and the reasons for acceptance of this new storage medium are as varied as the applications. COS/MOS (Complementary-Symmetry/Metal-Oxide-Semiconductor) devices are new candidates for memory use. Prime attributes of COS/MOS memory devices are low power dissipation, high speed operation with static memory cells, no refresh logic requirement, single power supply operation, wide temperature range, good noise immunity, insensitivity to power supply variation, and compatibility with TTL voltage levels. A figure of merit (the product of access time and power dissipation) shows COS/MOS to its full advantage (Table I).

Four RCA COS/MOS arrays are available: the CD4005, and RCA Dev. Nos. TA5577, TA6042 and TA5974. When choosing an array, a designer must consider storage capacity, speed, and power dissipation. Arrays with current outputs provide faster system access times when interfaced with bipolar sense amplifiers and bipolar address drivers, but arrays with voltage output sensing, although slower, make possible a low-power all-COS/MOS system. All devices can be directly driven with TTL devices, and the TA5974 can drive a single TTL load.

Table I—Figure of merit for typical memory devices.

Type	Capacity (Bits)	Access Time (ns) T_A	Access Power P_D (mW/Bit)	Figure of merit $T_A \cdot P_D$ (pJ/Bit)
COS/MOS Current Mode	256	500	.0012	0.6
TTL	64	7	6.2	43.4
TTL	256	90	2.5	225.0
TTL P-MOS	64	40	6.0	240.0
Static P-MOS	256	650	1.5	975.0
Refresh	1024	400	0.4	160.0

High reliability is a major attribute for a COS/MOS memory system. The extremely low power dissipation causes a minimum temperature rise for the memory rack. The resultant low junction temperature together with the non-destructive read out (NDRO) static memory cell provides dependable system operation. Moreover low power dissipation permits a very compact memory system.

System organization

The basic elements of any memory system are a memory address register, address decoder, buffers (to provide the necessary power for the large fan-outs required of the address lines), storage array, sense amplifier (with wire OR capability), data register, and the necessary timing and control logic (Fig. 1). When the memory system is partitioned into its hardware elements,

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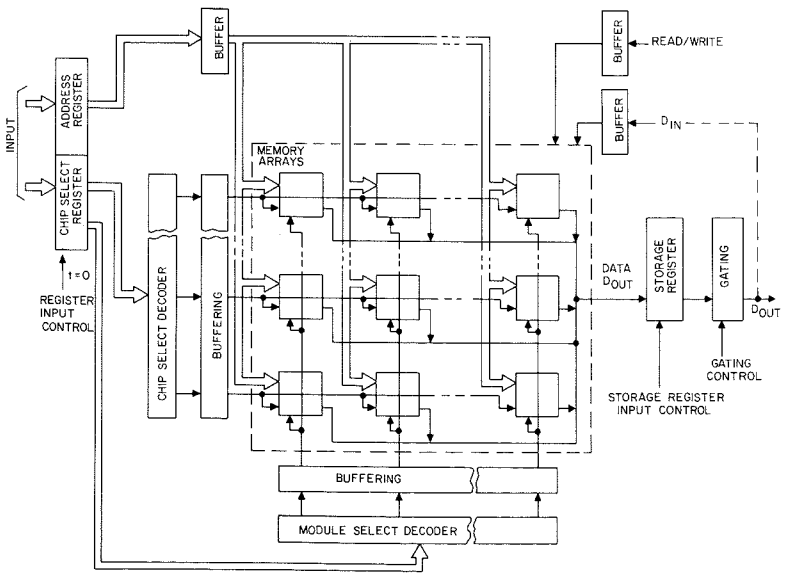


Fig. 1—Implementation of a large memory.

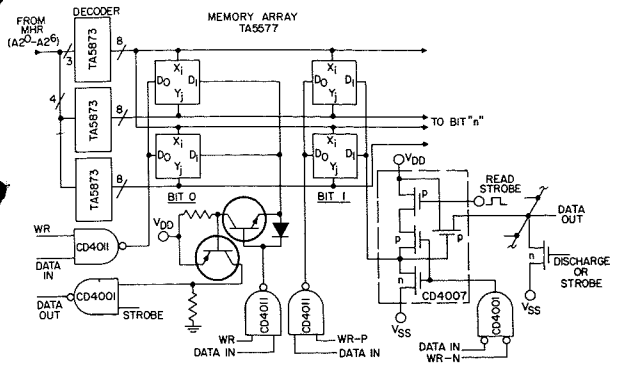


Fig. 2—COS/MOS memory systems: 128 words by 2 bits.

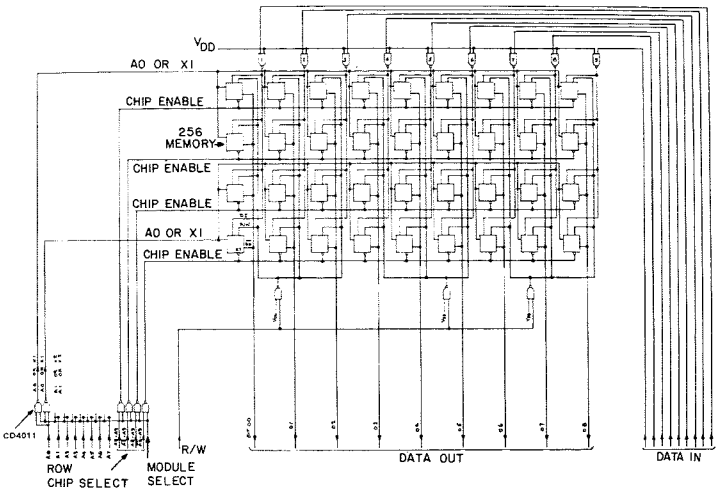


Fig. 4—Memory system: 1024 words by 9 bits, containing 36 TA-5974 memory chips and six CD4011 NAND gate chips.

a single printed circuit card usually contains the storage arrays, the sense amplifiers associated with these arrays, and the necessary buffers to drive the arrays. This printed card is the basic system module, and cards are paralleled in bit and word direction to provide the total storage capacity required of the memory system. Address registers, control logic, additional buffers, and perhaps some decoding are placed on additional cards which are usually unique to a system and represent a small percentage of the overall board count. Depending upon system size, the data register may be mounted separately or on the storage array card. Generally these support logic cards are special purpose cards without regularized logic.

Power

In an all COS/MOS memory system, dynamic power is the prime source of power dissipation. Quiescent dissipation is primarily due to device leakage and is quite low: selected units have demonstrated quiescent dissipation as low as 1.0 nW per bit. But dynamic power dissipation is proportional to CV^2f, where C *is* capacitance, V is voltage, and f is frequency. It is therefore necessary to partition the system so that a minimum number of long lines are energized at one time.

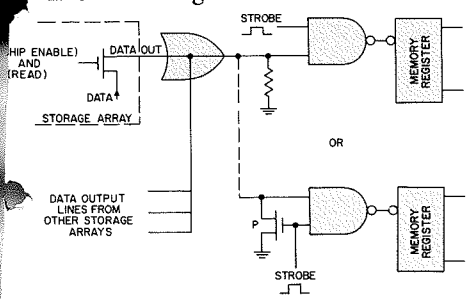


Fig. 3—Data bus terminations for RCA Dev. No. TA5974.

In memory systems using storage arrays with internal decoding, the outputs of the memory address register must be distributed to every memory array in the system: outputs of the memory address register must appear on every memory card. If the cards are bit oriented, address lines are switched on every card and charging and discharging the large total capacitance dissipates power. Power requirements could be reduced by placing several bits on a card and developing a card-select command that would enable address buffers so that lines would switch only on necessary cards. This approach is similar to sending chip-enable to only those arrays from which data is actually required.

In the extreme case where power dissipation must be minimized, the complete system can be operated at a reduced power supply voltage with a proportionate speed loss. Reducing power supply voltage to a minimum in arrays not being accessed can further reduce power dissipation.

Speed

Minimizing capacitance on the array sense output lines maximizes speed. Hence, cards should be bit oriented; all words associated with a bit should be on the same card to minimize wire capacitance and to make arrays with sense current outputs immune to backplane noise coupling or sense line oscillations.

Error detection

Most memory systems include parity checking to detect memory errors. Parity is usually maintained on a byte basis: nine bits, eight for information and one for parity. But the use of parity without error correction does not increase the reliability of the memory system.

For large capacity, long word-length memory systems, an error correcting code is economically feasible because it increases reliability and requires the same number of bits as parity. Single bit error correction will rectify errors in the storage array or sensing circuitry although it will not correct for malfunctions in address buffering or decoding circuitry. But any error correction method should be tailored to fit the specific system configuration and the system itself should be so well-organized that a bad socket pin or open wire will not cause an undetected malfunction.

Small buffer memories

The TA5577, a 64-bit memory, is intended for use in small memories. For efficient use word capacity should be less than 256, but word length is limited only by the driving capability of the address driver. A COS/MOS decoder, TA5873, will decode one out of eight input lines and serve as the address driver of the array. In a system, the TA5873 also replaces the address buffer.

The organization of a 128-word, two-bit storage card is illustrated in Fig. 2. This memory can be expanded in the bit direction by adding memory arrays. The TA5577 dissipates power whenever an "X" address line is selected, regardless of the state of the "Y" address lines. This "half-select" power dissipation can be minimized for larger systems by expanding in the "Y" direction. Therefore, for minimum power dissipation, systems should be organized so that Y is greater than X and the X decoder is inhibited when the memory is not accessed.

Two sensing techniques are illustrated in Fig. 2. One utilizes bipolar devices and the other employs cos/MOS units. The bipolar sense-digit interface has a typical delay time of 50 ns from storage array input to bipolar sense transistor output while the cos/MOS interface has a typical delay of 200 ns and is heavily dependent upon load capacitance. Bipolar interfaces can be designed compatible with cos/MOS or bipolar logic.

Medium capacity systems

The TA6042 and TA5974 are fully decoded medium capacity systems with eight address bits selecting one of the 256 storage cells. A chip enable allows selection of an individual array within a large system and permits low power system operation by eliminating half-select power loss. A non-selected device remains in a standby condition and only dissipates that power caused by leakage. Reducing power supply voltage on non-selected devices might reduce dissipation further.

Separate sense and digit lines permit faster system operation but require the proper read/write command input to identify the operation. The storage array must possess a wired OR capability to permit expansion of the memory in the bit direction, and the chip-enable command must disconnect non-selected memory arrays from the data bus to prevent them from interfering with the selected array output.

If no array is selected, the data bus tends to float and seeks a potential determined by leakage currents. But the selected array must charge or discharge the data bus from the potential the line assumes in the quiescent state; a floating data bus potential makes access time uncertain.

In the current-sensing version (TA6042), a low impedance sense amplifier discharges the line capacitance. The voltage sensing version (TA5974) has a high impedance cos/MOS gate as the sense amplifier and the bus floats unless a discharge resistor or active cos/MOS pull down is used (Fig. 3).

A typical storage card arrangement is shown in Fig. 4. The card is organized as 1024 words by 9 bits. To minimize power requirements, a module-select signal enables the address line buffers of the selected module only.

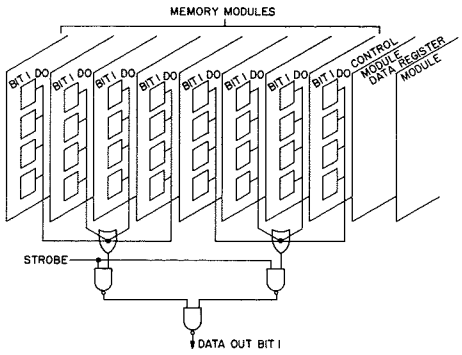


Fig. 5—Memory system: 8192 words by 9 bits.

An 8192 word system is formed by interconnecting the module as shown in Fig. 5. The complete memory can be contained on ten cards, including two cards for address and data registers, decoders and control logic, making the total system no bigger than a cube six inches on a side. Cards are approximately 5.5×5.0 inches and hold 42 dual-in-line packages.

There are two types of power dissipation: quiescent and dynamic. The storage array is the major source of quiescent power dissipation: a 256 bit array typically dissipates 300μW at 10 volts while the cos/MOS logic dissipates only 10 nW per gate. Premium devices can be selected for lower dissipations.

Dynamic power dissipation is a function of the number of lines switched during a memory cycle. For a typical calculation, consider 6 pf to be an average node capacitance exercized at 10 MHz with a 10 volt pulse. From the CV^2f calculation we see that the dynamic power dissipation is 0.6 mW per node. The storage card of Fig. 4 has eight address lines distributed to 36 memory arrays with a total of 304 nodes. Assuming that half the nodes will switch during any cycle, 152 nodes will dissipate 91.2 mW. And this calculation includes only address lines; data lines, common signals and internal switching within arrays have been excluded. Obviously, to minimize power dissipation the capacitance of the system must be minimized. This implies word slice organization, high packing density and minimum address line switching.

System access time for an 8K by 9 memory utilizing the TA5974 is typically 1.0 μs, and sixty-five percent of this delay occurs on the memory card. Faster operation can be obtained by utilizing the TA6042, but the bipolar sense amplifiers increase power dissipation.

Since the input signal to the memory need only be equal to half the power supply voltage, the TA5974 and TA6042 arrays are TTL compatible at 10 volts. Differential sense amplifiers improve system signal-to-noise ratios, eliminating common mode noise coupling and presenting a greater dynamic signal to the amplifier. A memory system utilizing a cos/MOS storage array with bipolar logic and interface circuits has been developed; a picture of a printed circuit card module is shown in Fig. 6. The card measures 4.5×5.0 inches and contains 21 integrated circuit packages organized as 1024 words by 3 bits.

Conclusions

The systems illustrated above demonstrate some of the attributes of cos/MOS when applied to memory design. The final product is a system that is extremely tolerant of variations in temperature, power supply voltage, and interface signal amplitude. These advantages combined with low power dissipation and a static memory cell design result in a straight-forward, reliable memory subsystem.

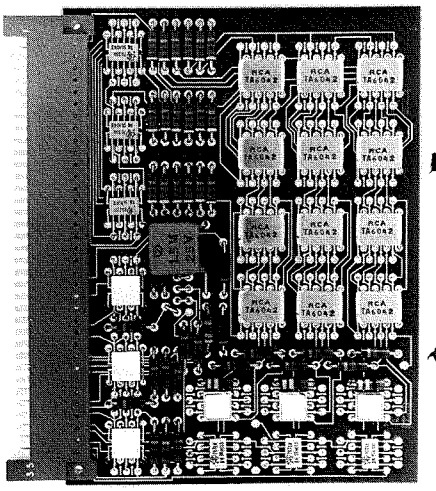


Fig. 6—Printed-circuit card module.

P-MOS technology for quick turnaround custom LSI

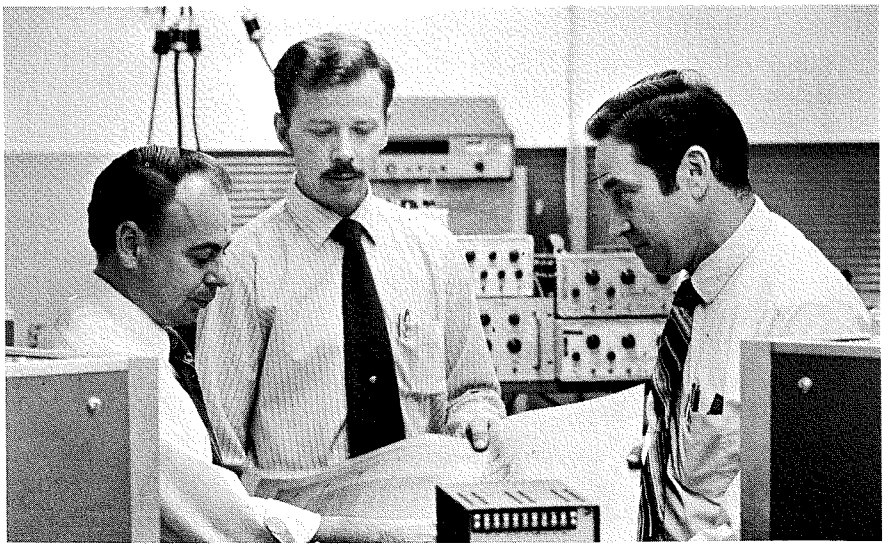
T. R. Mayhew | K. R. Keller | H. Borkan

Designers frequently require small quantities of large scale integration (LSI) circuits but cannot afford the time or money necessary for conventional custom design. The Quick Turnaround facility in Somerville can develop and deliver LSI arrays in as little as two weeks, using P-MOS technology and design techniques adapted to economical, quick turnaround.

T. R. Mayhew, Eng. Ldr., Monolithic Circuit Technology, Microelectronic Technology, Government and Commercial Systems Division, Somerville, New Jersey received the BEE degree from the University of Florida in 1956 and his MSEE degree from the University of Pennsylvania in 1962. He joined the Industrial Advance Development section of RCA in 1956 and was assigned to the development of automatic inspection equipment for the paper and glass industries. Since 1967 he has been involved in the application of MOS arrays in electronic systems and since 1966 he has been involved in the design and development of LSI arrays utilizing MOS technology. His designs include a PMOS 52 gate universal array and a 100-gate universal array. In December, 1968 he was promoted to Engineering Leader responsible for circuit development of PMOS arrays and packaging and for PMOS pilot production facility. Mr. Mayhew is the coauthor of five papers on memory systems and holds nine U.S. patents. He is a member of Sigma Tau, Cross Keys, and IEEE.

Kenneth R. Keller, Eng. Ldr., MOS Fabrication Techniques, Microelectronic Technology, Government and Commercial Systems Division, Somerville, New Jersey received the BSEE in engineering physics from Rutgers University in 1961 and received the MSEE in 1963 from the same university. In 1961 he joined the technical Staff of the RCA Laboratories where he studied impurity scattering of phonons and the solid and acoustic properties of Nb_3Sn using microwave ultrasonic techniques. In 1966 he transferred to the Electronic Components and Development division to work on the development of complementary MOS integrated circuit processing, and in 1968 he began work on advanced processing techniques for PMOS array fabrication in the Microelectronic Technology facility. Mr. Keller became an Engineering Leader in 1970 with responsibility for PMOS pilot production and development programs. Mr. Keller is a member of IEEE, Tau Beta Pi, Eta Kappa Nu, Pi Mu Epsilon, and Sigma Xi.

Harold Borkan, Mgr., Monolithic Subsystems, Microelectronic Technology, Government and Commercial Systems Division, Somerville, New Jersey received the BSEE with high honors from Rutgers University in 1950 and the MS degree from the same university in 1954. In 1950 he joined RCA Laboratories in Princeton as a member of the Technical Staff where he did research on electronic devices and circuits. In March, 1965 Mr. Borkan transferred to RCA's Microelectronics Technology activity at Somerville, New Jersey and in January, 1968 his responsibility was expanded to include circuit development, process development, and complete pilot production of PMOS integrated arrays. In October, 1968 he was promoted to Manager, Monolithic Subsystems, and his responsibilities were expanded to also include development of image sensor arrays for the IR and Visible spectra. Mr. Borkan is the author of over twenty technical papers and holds seven patents in the areas of television camera tubes and semiconductor devices. He is a Senior Member of the IEEE, a member of Eta Kappa Nu, and is the recipient of two RCA Laboratories Achievement Awards. He is a member of the team that received an outstanding paper award from the 1964 IEEE International Solid State Circuits Conference.



Authors Mayhew, Keller, and Borkan (left to right)

MILITARY EQUIPMENT DESIGNERS often require large scale integration (LSI) of their logic subsystems because of size, weight, power, reliability, and cost requirements. However, the number of systems that are requested may not be large, the time permitted for the design phase may be short, and the funds available for the design may not be adequate for a conventional custom design. To satisfy these severe demands the Government and Commercial Systems Division has established a custom LSI QTA (quick turnaround) facility in the Microelectronic Technology (MET) organization located in Somerville, New Jersey.

The p-channel metal-oxide-semiconductor (P-MOS) transistor technology is best suited for quick turnaround because of the relatively simple fabrication requirements, and because it affords very high array density. In addition, the universal array, a MET-originated LSI concept, provides for low-cost design and quick turnaround because it requires that only one photomask be customized to implement a logic subsystem. (The universal array approach is described in detail in the article titled "Monolithic Applications —Divisional Interface," in this issue.) Combining the P-MOS technology with the universal-array concept has given RCA an effective QTA LSI facility that to date has produced over 150 different array types quickly and economically. The QTA LSI facility has successfully produced more than one array type per week from new artwork and has produced large numbers of those array types which have achieved wide utilization.

P-MOS fabrication

The integrated-circuit designer has a wide range of device fabrication technologies available to him. These include bipolar, single-conductivity-type MOS, complementary MOS, silicon-gate MOS, and silicon-on-sapphire, as well as hybrid combinations of these. P-MOS dominates applications that require low cost, because the fabrication simplicity gives high wafer-processing yields and high density devices, resulting in low cost per logic function. P-MOS integrated circuits are simple to fabricate because only one diffusion and only four masking steps are re-

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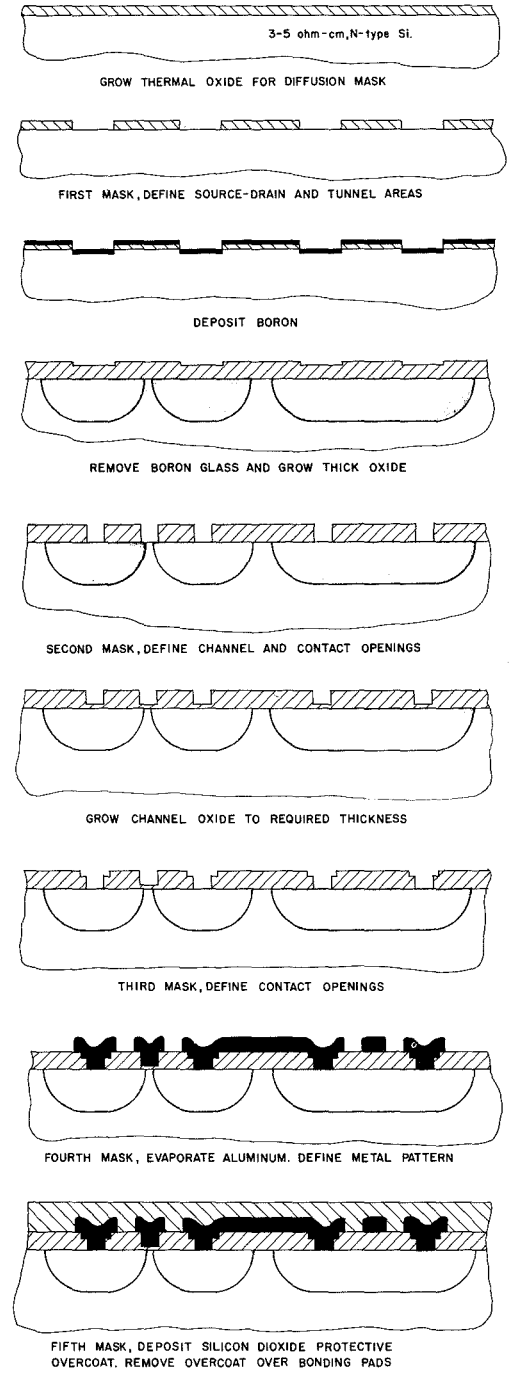


Fig. 1—PMOS process outline.

quired. (An optional additional masking step may be used in any of the IC technologies to provide a protective overcoat on the chip.)

The process sequence, including the optional masking step, is outlined in Fig. 1. Starting material is 3 to 5 Ω-cm, n-type silicon wafers. After growth of a diffusion masking oxide, the first photomask is applied using standard photolithographic techniques. This masking oxide is etched away in the source, drain, and tunnel areas. The tunnels form conductors which cross under metal lines, and a boron diffusion creates diodes in the areas not protected by oxide. The portion of the masking oxide that has been contaminated by the boron and the boron glass over the unmasked regions is then removed.

At this point, the thick field oxide is grown; the thickness of this oxide determines the turn-on voltage of parasitic transistors. Thermal oxidation is preferred to deposited SiO_2 because of its relative cleanliness and low pinhole density, but greater lateral and longitudinal diffusion take place during the oxidation. To compensate for the additional diffusion during growth of 13,000 Å of oxide, the source-to-drain spacing is appropriately defined in the first photomask.

The second mask pattern allows removal of the oxide in the channel regions and defines the contacts. The use of separate channel and contact patterns, rather than a single pattern which allows oxide removal over the entire transistor area, on the second mask allows thick oxide to remain over the diffused region between the channel and contact and reduces the gate-to-drain capacitance.

Channel oxide is then grown to a thickness determined by the required threshold voltage range as specified in Table I. The third mask, defining the metal-to-silicon contact areas, is applied. The contact openings on this mask are larger than those on second mask, resulting in a double step in the oxide. Thus, metal lines do not have to go over a large oxide step.

Aluminum is evaporated and the fourth masking and etching step is performed. This mask pattern defines transistor metal electrodes, device interconnections, and bonding pads. Finally, the entire chip is covered with a protective layer of deposited silicon dioxide. A fifth masking step is then used to remove the silicon dioxide over the bonding pads.

Table I—MET P-MOS Specifications

Process	*D*	*F*	*G*	*H*
Threshold voltage range (Volts)	1.0-1.8	1.6-2.6	2.2-3.4	3.5-4.5
Channel oxide thickness (A)	1100	1100	1500	1700
Silicon orientation	<100>	<111>	<111>	<111>

An example of a P-MOS array is the MET 256-bit fully-decoded RAM with sense amplifier on a chip 157 × 147 mils. The basic memory cell, consisting of six transistors, occupies an area of only 32 mil². Device size for this array is at a minimum determined by processing capability. Because of its geometrical simplicity and the requirement of a single diffusion, the P-MOS device is smaller than other device types.

Isolation diffusion or the use of diffused channel stoppers are not required, thereby reducing the area required for a cell. An MOS transistor, which requires less area than a diffused or thin-film resistor, is used as a load, further reducing the area requirements. Of the integrated-circuit fabrication technologies available, the P-MOS approach gives the highest number of logic gates per unit area.

The use of an active load in MOS circuits provides a degree of flexibility to the user. The load may be used as a resistor by fixing the gate potential or the gate may be clocked to reduce power consumption or to provide special functions. The MET approach enhances this flexibility by offering P-MOS in one of four threshold voltage ranges, as shown in Table I. The two lowest voltage ranges are compatible with T^2L circuits so that P-MOS arrays may be directly interfaced with bipolar circuits.

The fewer process steps required for P-MOS technology results in higher yields at the wafer fabrication step than achieved in other technologies, as well as higher reliability. These factors coupled with the higher gate density result in lower cost per logic function. In addition, the fewer process steps and higher yield give reduced processing time so that turnaround time is minimized.

Design approaches

There are three basic approaches to the design of P-MOS LSI arrays, differing from each other in their artwork-generation requirements. These approaches are custom-designed arrays, standard-cell arrays, and universal arrays.

Custom arrays

In the custom-array approach, each

circuit component is analyzed in terms of circuit performance and chip area consumed.

The primary objective is to minimize chip area within the restrictions of the layout design rules while still satisfying the circuit performance requirements. Each photomask is tailored to the specific subsystem being implemented. This approach results in the most compact chip; however, it is the most difficult to design and requires more engineering time than the other methods.

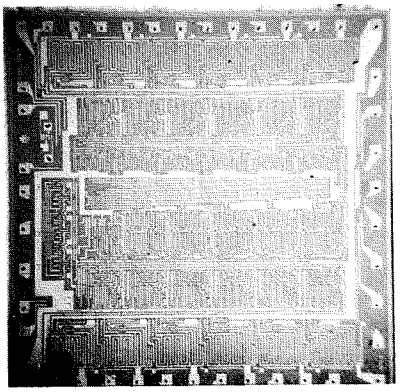
An example of a custom-designed array is illustrated by the character buffer shown in Fig. 2. Note that there is very little unused area within the chip. This array is 138 × 137 mils, has 43 bonding pads, and contains two sets of six-bit static registers with versatile data-steering logic. Data may be entered and retrieved either serially or in parallel, and additional control is provided to vary the lengths of the registers. There are twelve high-conductance output transistors located on two sides of the chip. These are required for T^2L compatibility and high speed operation, and have been interdigitated to minimize area.

Standard-cell arrays

The standard-cell approach seeks to reduce the design effort required for new arrays through the maximum use of design automation. A set of basic cells, such as a three-input NOR gate, a dynamic shift register stage, and a logic inverter has been designed and placed in a computer library. The library is held in memory and contains the information needed to generate the artwork for all masks. The designer, working from a logic diagram, specifies the required basic cells, and the computer goes through a cell placement and interconnection routine. The final array size depends upon the efficiency of the interconnection routine.

An example of a standard-cell array is illustrated by the sixteen-bit correlator shown in Fig. 3. The array contains three sixteen-bit shift registers, a data register, a pattern register and a masking register. The outputs of the pattern register and data register are compared under control of the masking register in 16 exclusive-OR gates whose outputs are summed. There are two additional sixteen-bit delay lines on the array. The correlator chip is 133 × 109 mils and is a relatively compact design for a standard cell array because of the serial flow of data.

Fig. 2—Custom designed character buffer chip.



Universal arrays

A universal array is a design in which the first three photomasks are defined and remain fixed for all applications. The fourth mask (metal mask) is custom-designed for each application. The basic array consists of P-MOS transistors and p^+ tunnels; the metal pattern interconnects the transistors forming the individual logic elements. Combining these into the complete subsystem mask is the only change from one application to the next. This mask alone defines the specific interconnection pattern and the functional operation of the particular chip.

The primary advantages of this approach are low cost and quick turnaround time. These result because each application requires the definition and fabrication of only one mask. In addition, each application uses a proven set of three masks having fixed device geometries. The cost saving arises because wafers can be processed through metalization and stockpiled awaiting the metalization pattern.

A number of universal array families, tailored for different applications areas, have been completed. These include a 52-gate logic array (GUA-1), a two-phase dynamic register array (RUA), a four-phase array (FUA), and a 100-gate logic array (GUA-3). More than 150 logic variations of these basic types have been implemented and used by design engineers in various RCA divisions.

Fig. 4 illustrates an implementation of the 100-gate universal array. The chip is 127 × 122 mils; it contains 500 transistors and 40 bonding pads. The application shown was designed for use in an aircraft transponder and provides the complex encoder/decoder function. It contains a 22-stage shift register with parallel loading capability at 14 preselected locations. The front end of the shift register has an asynchronous pulse retimer circuit. Logic circuits decode certain register states and provide external output indications.

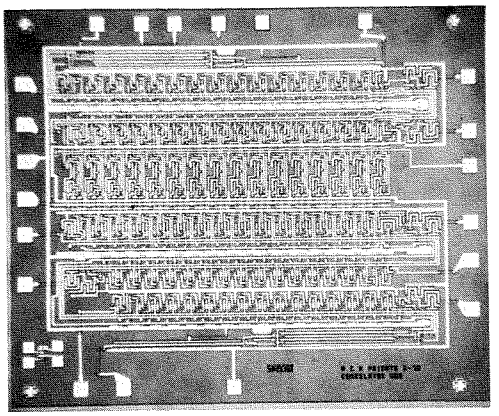


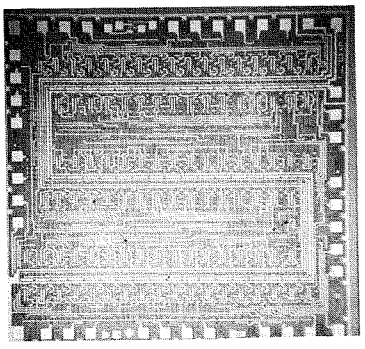
Fig. 3—Standard cell array; 16-bit correlator.

Conclusions

The MET P-MOS pilot facility provides a quick turnaround capability for both development and follow-up work requiring LSI arrays. Development work demands many different types of arrays, typically one or two new types per week, in relatively small quantities (less than 100 per type). These array types may be custom designed, standard-cell, or universal arrays. Most applications require universal arrays because the turnaround time from logic to delivered arrays is shortest (typically seven to nine weeks) and can be as short as two weeks on a crash program. The standard-cell and custom designs generally take longer, with complicated custom designs sometimes requiring as much as six months.

Quick turnaround capability in the development phase may lead to a high volume add-on contract. One example is a program which initially required small quantities of four logic variations of the GUA-3 for low-power applications. The successful and timely qualification by RCA for the design and production of modules utilizing these arrays led to additional contracts. Thus the universal-array concept implemented with the P-MOS technology is an effective means of achieving quick-turnaround time for large scale integration of logic subsystems.

Fig. 4—GUA-2 transponder encoder/decoder.



Monolithic applications-divisional interface

R. H. Bergman | F. Borgini | L. Dillon, Jr. | G. E. Skorup

The Monolithic Applications Group of Microelectronic Technology acts as a link between the wafer fabrication facility and its potential users, assisting the user in designing arrays, preparing and checking artwork and masks, and guiding the fabrication shop in processing the wafers.

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received his BS in Electrical Engineering from Rutgers University in 1953. He joined RCA and worked in the Advanced Development Section. He served as an officer in the U.S. Army Signal Corps from 1954 until 1956. He returned to the Advanced Development Section of RCA where he engaged in the design of an accurate shaft-to-digital encoder, and a magnetic-drum computer clock-timing system. Following this, he worked for Commercial Advanced Development. Since 1965, he has been the Leader of a group in the Microelectronic Technology Activity engaged in the application of LSI arrays to digital systems. This work includes the design of standard array configurations with limited customizing capability, logic design and partitioning for custom array application, circuit analysis, array layout, array specifications and standardization, and array testing techniques. The technologies include bipolar P-MOS, and C-MOS. Under his direction, his group has designed, fabricated, and tested more than 150 different array types. He is a member of Tau Beta Pi and Eta Kappa Nu.

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received the BS in Electrical Engineering from the University of Missouri, Rolla, in 1959 and the Masters Degree in Electrical Engineering from Drexel Institute of Technology in 1966. He joined RCA in 1959, and after completing the Trainee Program he was assigned to the Advanced Development Group of EDP to work on Project Lightning. He worked on the development of a computer subsystem using phase locked oscillators. He was then assigned the responsibility of assembling and testing a Memory Exerciser using tunnel diode logic circuits. He is currently engaged in the application of MOS array technology. He has been responsible for the design of a number of P-MOS arrays to meet specified logic or systems requirements. This work includes the implementation of digital modem, delta modulator, crosspoint switch, and other logic functions associated with frequency synthesizers for multichannel radios. This responsibility includes conversion to MOS logic and circuits, layout on standard forms, test specification preparation and artwork, mask, process and test follow. Mr. Borgini is a member of Etta Kappa Nu.

IN THE LAST FEW YEARS there has been a rapid growth in the use of complex integrated circuit design vehicles in electronic equipment. In many cases the arrays contain over 100 logic gates and over 500 active devices. While off-the-shelf functions can be used in many applications, specially customized arrays are often needed due to function, size, power, cost, or weight requirements. The design engineer working with complex IC arrays is charged with several size-

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graduated from the Milwaukee School of Engineering in 1959 with a BSEE degree and from Drexel University in 1966 with a MS degree. Upon completion of the RCA training program he was assigned to the Consumer Electronics Division as an Engineer in color TV and TV remote control. In 1961 Mr. Dillon transferred to the Information Systems Division to work on Project Lightning. As a design and development engineer he worked on high speed tunnel diode memory systems, and also investigated low power tunnel diode, high speed magnetic, and associative memory systems. During 1963 the group in which Mr. Dillon was working transferred to the Advanced Technology section of Government and Commercial Systems. His work in memories was expanded to include integrated circuits as applied to scratch-pad memories. With the advent of P-MOS Large Scale Integration, he began investigating applications to communications, and he assisted in the design of a P-MOS clock recovery system. In the fall of 1966 the group was transferred to Microelectronic Technology to handle LSI applications. His responsibilities since then have been in the design of P-MOS, complementary MOS bipolar integrated circuits. Mr. Dillon holds one patent in the area of large scale integrated circuits.

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received the BSEE degree from Milwaukee School of Engineering in 1945 and an Associate Degree in Business Administration from the Evening Division of the Wharton School of Finance and Commerce in 1963. He has done work toward an MSEE at Drexel Institute of Technology. Mr. Skorup joined the receiver design section of the RCA TV Division in 1947, and worked on the design and development of both vacuum tube and transistorized television receivers. In 1961 the T.V. Division was relocated and he was assigned first to the Projects Section of M&SR Division and then to the Advanced Technique Development section, where he investigated solid state and semiconductor laser modulation, transmission, detection and signal processing. From 1964 through 1965 he was the project engineer responsible for the development and design of prototype optical correlation equipment for undersea warfare. From 1966 to the present he has been responsible for all P-MOS applications and proposals in the M&SR Division, and he is currently engaged in the design of P-MOS and C-MOS integrated circuit arrays and array vehicles for use by other RCA divisions. Mr. Skorup received the M&SR Chief Engineer's Technical Excellence Award in April, 1968.

able tasks. He must select from such available technologies as P-MOS, C-MOS, and bipolar. He must also consider the circuit approach, functional partitioning, interfacing, packaging, environmental specifications, and in some cases the design and processing of active and passive components contained on the array. These decisions are further complicated by the rapidly changing technology which quickly obsoletes past reference points and tradeoff factors.

To assist the G&CS engineer in making the optimum decisions in these areas, the MET Monolithic Applications Group has been working with the engineers in each of the five G&CS Divisions, providing not only guidance and consultation services, but also access to customized complex arrays on a quick turn-around basis. From 1964 to the present, the activity has assisted in the implementation of over 150 complex array designs using P-MOS, C-MOS, and bipolar technologies. During this period, over 15,000 functioning arrays have been delivered for many developmental and production programs. Some typical functions which have been implemented with complex arrays are listed in Table I.

Table I—Complex array applications.

Function	*Application*
Control logic shift register/counters	Data buffer
Driver/remote storage/ programable counter/ divider/control	Phased array beam steering
ROM/code generator	Hand held radar
Arm and fire logic	Fuze timer
Analog cross point/link alotter/line select	Switchboards/data switch
Encoder/decoder	IFF/transponder
ROM character store	Data display
VSD/compander	Communications
Bit timing and decision logic	MODEM
Freq. synthesizer control/lock det./scaler	Multi-channel radio
Register/control/ sequencer/clock	Electronic drum
Programmable filter module	EW
Encoder, decoders	Intrusion device
Analog multiplexer/ serial and parallel digital	Data monitor and test
Arithmetic and control/ ROM	Special computers
Video sync. generator	TV/IR scanning

Table II—Artwork and mask dimensions and tolerances.

	Artwork	*Masks*
Pattern size	34 in	170 mil
Scale	200 ×	1 ×
Line size	40 mil	0.2 mil
Accuracy	±4 mil	±20 microinches
Registration	±4 mil	±50 microinches
Defect density	——	25/in²

Complex array design cycle

The block diagram of a typical design cycle for an array is shown in Fig. 1.

The total effort is divided into five areas: specification, design, artwork, masks, and fabrication and test. During the specification and design phases, the function to be implemented is first defined and described in detail as a circuit function and then carefully laid out according to the rules of the process to be used. The composite product is an overall layout which identifies from five to ten mask definition steps required to process the devices. Typically these steps are diffusions, oxide cutouts, and metal pattern definition. The information derived from the overall layout forms the basis for the preparation of an equivalent number of layers of precision artwork fabricated at a convenient scale. This artwork is reduced to final size and the array pattern is duplicated by a step-and-repeat exposure process on a glass mask large enough to cover the wafer to be processed. Typical dimensions and tolerances for artwork and masks are shown in Table II. The final masks are sent to the Process Shop for the fabrication of wafers.

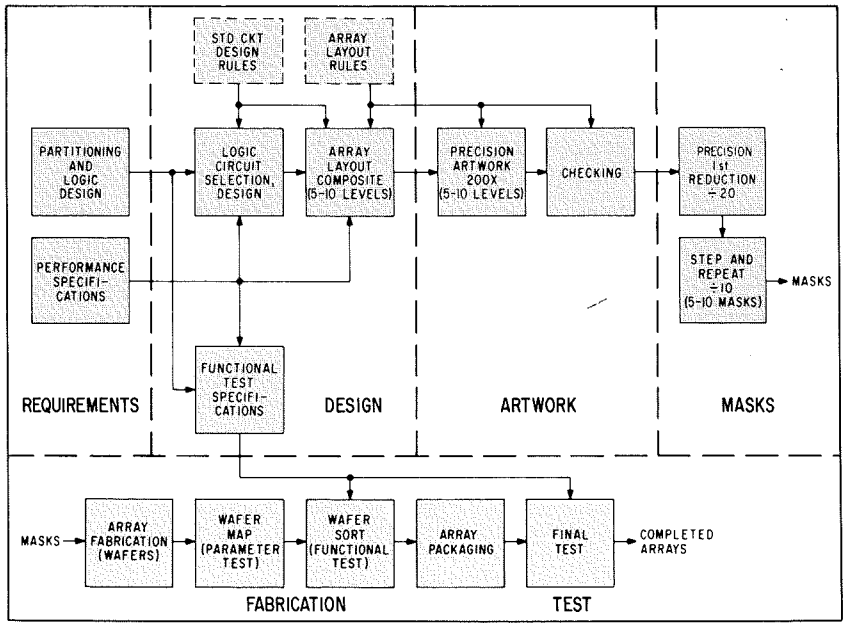


Fig. 1—Design cycle for a typical complex array.

Testing

An important part in the design of an array involves translating the performance specifications into the functional test specification used to test the array both at wafer sort and after final packaging to assure proper operation. For complex digital devices containing sequential logic nets (*i.e.*, flip-flops and other types of storage) the task is formidable and requires special purpose test equipment capable of generating 100 bits or more of test patterns on 40 or more lines. To meet this need, computer controlled test systems are now being used. For nondigital circuits, additional parameters often have to be measured. A typical array has 10 to 20 inputs and a similar number of outputs. The test specification requires operation at worst case power supply and input signal limits. Test patterns often contain initialization pattern sequences to preset internal counters and registers to a state where proper operation can be observed at the array outputs. In many cases frequency, loading, and rise time tests have to be performed as well as power supply current and leakage measurements.

Universal arrays

The tremendous quantity of detail contained in a custom array design incurs a high probability of error. Even with careful checking at several steps in the cycle, the device may not operate correctly at the wafer sort stage.

After identification of the problem, a redesign and rework cycle is required. A complex array design may require several rework cycles and take six months or longer to complete. To reduce turn-around time and simplify design, the universal array concept has been used extensively in G&CS applications. A universal array is an IC vehicle upon which the device locations are fixed on the substrate; various functions are implemented by specifying unique interconnection patterns for the fixed devices. With this approach, only a portion of a single mask (metal pattern definition) need be changed for each application. The basic mask layers and, therefore, device geometry, pad location, and power bus configuration do not vary between applications. This approach greatly reduces design time and cost, and the probability of error. It typically allows for the simple change or addition of logic (for ECN purposes) at a later time. Designs have been processed to sample parts (meeting full military or commercial specifications) in a best case time of a few weeks, with ECN's processed to sample parts in one week. For a detailed description of the fabrication of a P-MOS universal array, refer to the article "P-MOS Technology for Quick Turn Around LSI" in this issue.

The rules for the use of the universal array are much simpler than those for the completely customized design and can therefore be easily learned by the engineer who has an application.

The Applications activity issues users manuals for the universal arrays and conducts training sessions at the location where use is anticipated. A convenient layout form and functional test format is provided so that the user can implement his function. Typical logic function layouts and application data are distributed to interested engineers. The families of universal arrays which have been implemented with P-MOS technology is shown in Table III with pertinent characteristics.

The universal array family currently consists of the Register Universal Arrays (RUA), Four-Phase Universal Arrays (FUA), Gate Universal Arrays (GUA), and the Read Only Memory (ROM). The most widely-used type is the GUA because it is best suited for general purpose logic and can implement either static or dynamic logic. At the present time there are three versions of the GUA; they are referred to as GUA-1, GUA-2, and GUA-3 array vehicles. The GUA-1 is equivalent to 52 two-input gates, while the GUA-2 and -3 are equivalent to 100 two-input gates. The only difference between the GUA-2 and GUA-3 is the physical dimensions of the load transistor. The GUA-3 is the low power (lower speed) version of the GUA-2.

Effective utilization of the GUA approach requires knowledge in three basic areas: 1) general understanding of P-MOS transistors, circuits and logic, plus a more detailed knowledge of the capability of the transistors on the array; 2) basic rules that must be followed when layout of the custom metal is performed to produce the desired logic functions; and 3) the ability to produce a test package to conform to standard testing procedures. MET gives consultation and assistance in these areas to the divisions. The most desirable working interface between the divisions and MET comprises a metalization form of the customized metal (to implement the required function), and test specifications to validate the design.

A composite drawing of a section of the GUA-2 array is shown in Fig. 2. This section shows four of the total of 100 cells on the array. All cells are uniformly placed along a group of bus

Table III—Universal array summary.

	Type			
	GUA-1	*RUA*	*FUA*	*GUA-2*
Number cells	52	112	72	100
Number gates	52	208	(72)	100
Number transistors	204	656	252	500
Array size	82×90	100×108	114×114	116×124
Array area (mil²)	7400	10,000	11,900	14,480
Active area (mil²)	80	145	376	384
Number pads	22	22	40	40
Power dissipation typical (mW)	50	150	100	250
Speed (Megabits/second)	1	1	5	2

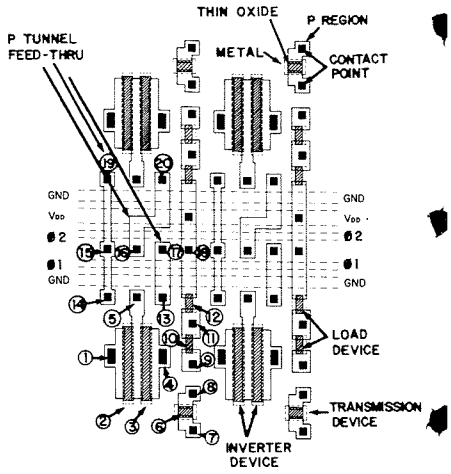


Fig. 2—Gate Universal Array (GUA-2) cell.

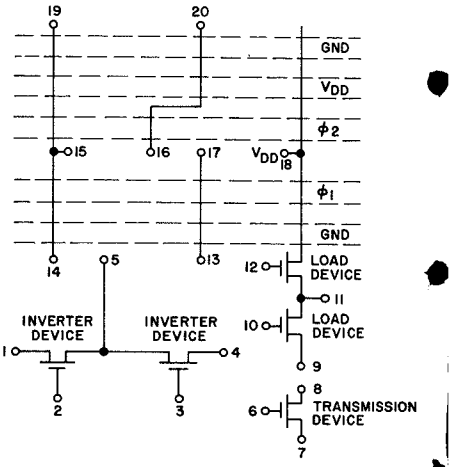


Fig. 3—Gate Universal Array (GUA-2) devices.

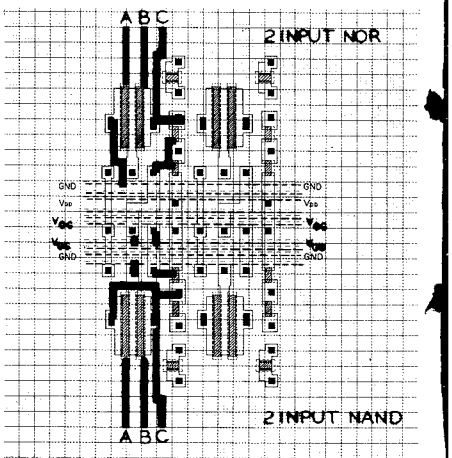


Fig. 4—Customized metal required to interconnect a two-input NAND and a two-input NOR gate.

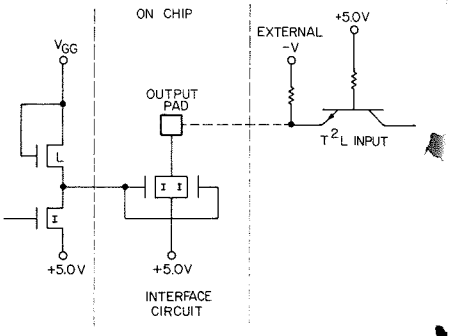


Fig. 5—Simple T²L interface circuit.

lines. The important points in a cell are numbered, and Fig. 3 shows the corresponding devices. Figure 4 shows examples of the customized metal required to interconnect a two-input NAND and a two-input NOR gate. The fact that GUA transistors are designed to be used as ratio type devices must be considered in a typical design. For example, the GUA-2 must be used such that only one pull down transistor (inverter) is used in series with a load device. If both load devices are used, two pull down devices can be stacked in series. With the GUA-3 eight inverter devices can be stacked in series with the load transistor and the transmission device (with impedance equivalent to five inverters) can be used as a pull-down making the GUA-3 equivalent to 100 three-input gates.

Very efficient use of the GUA-3 can be accomplished by functional gating techniques where devices are used in series-parallel combinations to perform a logic function. From the basic NAND, NOR gate structures, various types of flip-flops can be constructed to perform shifting and counting operations. With these design features, a logic design can be implemented by staying below the limit of 100 cells and 40 input-output pads available on the array. But attempting to fully utilize all of the 100 cells can make layout extremely difficult; as a rule, 80 to 90 percent cell utilization should be planned to allow flexibility and room for changes. Input/output interface circuits for bipolar compatibility can be implemented on the array when using low threshold devices. A typical output circuit using a single cell with an external resistor to sink 1.6 mA of current is shown in Fig. 5. GUA applications must fall within the speed capability of the present arrays, presently 1 MHz for static logic and 2 MHz for dynamic logic.

Devices can be easily interconnected with customized metal by using 0.4-mil wide metal lines and 0.4-mil spacing between lines. The metalization form provided has guide lines to facilitate proper spacing. With a little practice, the designer becomes familiar with the GUA structure and can implement his unique function. The GUA provides a two-layer interconnection capability. One layer is the metal on top of the thick oxide and the second layer consists of the p-tunnel crossunders. In addition, the designer must learn the testing requirements. A functional test pattern should be prepared that completely tests the logic. For convenience, test patterns should be less than 100 bits long. Standard forms are provided for preparing test specifications, and special AC and DC tests can be added when required.

The completed layout and test specification are turned over to MET for review and implementation. The following steps are taken by MET to fabricate working P-MOS devices. The layout on the 200× metalization form is used to generate 200× artwork. This can be either a rubylith cut by a coordinatograph and manually peeled, or a film artwork generated by digitizing the *x*-, *y*-coordinates of the layout and using this information to drive an automatic plotter. The logic is then simulated by patching the interconnections on a 200× scale version of the array. The simulation provides three important features: it verifies the logic design, it helps detect any errors made in transferring the layout to artwork, and it verifies the test pattern-written to test the array. Eliminating errors at the simulation step is significant as it reduces the probability of fabricating wafers that are incorrect and simplifies wafer probing. The artwork is then sent to the MET Photomask Lab where 1× working glass plates are made. At present, 2.5-inch glass plates are produced by a step-and-repeat camera to process two-inch wafers. The working masks (metalization only) are sent to the Process Shop where parts are processed to produce the final packaged units for the customer.

Design example—P-MOS gate universal array

The availability of vehicles such as the P-MOS GUA-2 and -3 has allowed system designers to define new concepts for telephone switchboards. For example, the GUA implementation of a function called "line circuit" described below has enabled the system designers to reduce the common control circuitry as well as the multiplexing requirements. This design provides greater reliability, since much of the common control is now in the line circuit chip. With the reduction of common control circuitry, there is less chance of a failure completely disabling the switchboard: a failure in a line circuit chip only disables the line associated with that chip and replacement of the chip quickly solves the problem.

Fig. 6 is a logic diagram of the line circuit which has been implemented on the GUA-3 array; this array contains two of the line circuits shown. The line circuit function is being used in the development of a cordless semi-automatic tactical switchboard by the CSD-G Division. The line circuit basically consists of line termination circuitry, a ring detector, tone gates, and control logic. The control logic is activated by the line and function push buttons on a front panel and by the ring detector. Outputs from the line-circuit logic control the line-circuit indicator on the front panel, gate signals to the subscriber, and select and operate signal crosspoints. Table IV summarizes the logic functions and number of each type on the array.

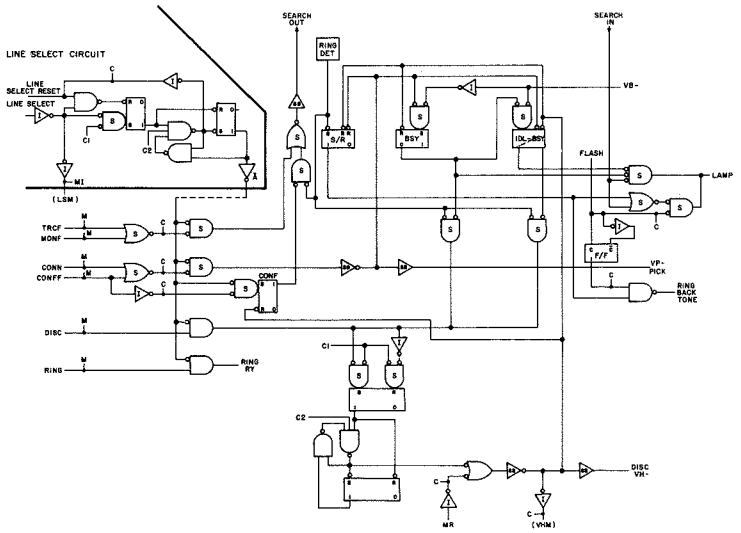


Fig. 6—Logic diagram of the line circuit for the GUA-3 array.

Table IV—Logic function count-line circuit array.

Logic type (Positive Logic)	*Number on array*	*54/74T²L equivalent*	*Number of cells*
Two-input NAND	8	2 IC's	8
Three-input NAND	6	2 IC's	9
Two-input NOR	18	5 IC's	18
Inverters	15	3 IC's	15
S/R flip-flop	20	10 IC's	40
Toggle flip-flop	2	1 IC's	8
Push-pull buffer	6	1 IC's	18
Total		24 IC's	116

The cell count was determined by considering the use of inverter (pull-down) transistors exclusively. However, since the low-power GUA-3 array was used in this application, extra logic could be incorporated by using the transmission device as a logic element; the function was implemented with 100 GUA-3 cells.

The line circuit described above is a typical example of a Division application which MET coordinated. The typical turnaround time for such an application is nine weeks from receipt of layout and test package. An application of a complex array which has a longer turnaround time—the custom bipolar array—is described in the following design example.

Design example—custom bipolar

All the G&CS bipolar applications processed through MET to date have been custom designs, where requirements and circuit design have been generated by the divisions. MET provides consulting services during the design phases of these programs to assure that the circuitry is compatible with on-line silicon processing capabilities at SSD. After the circuit design phase is complete, layout, artwork generation, and mask fabrication tasks are usually handled by the MET Monolithic Application Group. However, the task interface varies on some applications. SSD provides the wafer fabrication capabilities. Wafers are accepted on the basis of probing uncommitted circuit components on "test keys" located in five places on the wafer. Final test and packaging has been done in SSD, MET, or the division, as desired.

The phased array radar phase-shifter dual power amplifier circuit developed by MSRD is an example of a custom bipolar integrated circuit development program that has resulted in a cost-effective approach that met or exceeded design goals. A detailed explanation of the system is given in Reference 1. Fig. 7 shows a circuit schematic of the amplifier and a photomicrograph of the resultant integrated circuit called the TA 6121. This portion of the total phase-shifter driver was partitioned into one IC on the basis of voltage and power considerations.

First samples usually have some operational difficulties which may be due to layout errors or parasitic effects which were not uncovered during the breadboard phase of the program. Sometimes several iterations of the process are necessary during the development program. As an example, in an early version of the power amplifier, the input circuit was configured as in Fig. 8. The diode CR1 provided a disconnect function during the negative inductive kick. Normally diodes are implemented with the base-emitter junction of a transistor, but in this case reverse voltages in excess of BV_{EBO} were encountered and a collector-base diode was used to avoid reverse breakdown. Every npn collector-base junction has associated with it a parasitic pnp transistor with its collector at the substrate. The parasitic transistor has an h_{fe} ranging from three to ten and can shunt appreciable currents to the substrate. Since the substrate of the power amplifier is returned to a negative voltage, standby power dissipation was greater than originally anticipated.

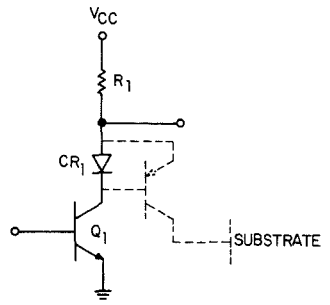
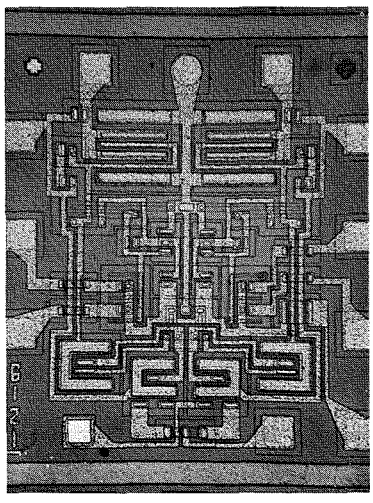


Fig. 8—Input circuit.

The present version of the dual power amplifier (TA 6121) also uses npn collector-base diodes but they are arranged so as not to conduct during quiescent operation. This brings up an important point: circuits intended to be implemented with custom bipolar arrays cannot be reliably breadboarded with discrete active components. Many characteristics, such as R_{sat} or additional active and passive parasitics to the substrate can cause side-effects that grossly impair circuit operation.

The TA 6121 evolved from a previous developmental IC, the TA 5954. When interface and system specifications firmed up, the TA 5954 metal mask



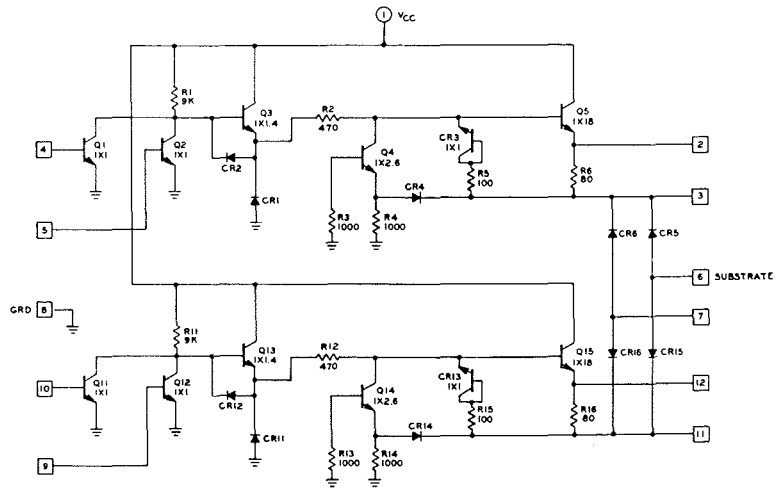


Fig. 7—Phased array radar phase-shifter dual power amplifier circuit. At left is a photo-micrograph of the IC.

was modified to reflect the latest changes and mated with wafers that were in the fabrication cycle at that time. Sample parts were evaluated at MSRD where is was decided that recovery time margin could be improved by increasing the current-carrying capacity of transistors Q_4 and Q_{14}, and diodes CR4 and CR14 by adding the deep n^+ collector diffusion (already used in the output transistors Q_5 and Q_{15}) to these components. The deep n^+ collector diffusion substantially reduced the resistance through the epitaxial collector region to the top contact.

With these changes incorporated, the new design was put through the layout, mask, and parts fabrication cycle. The entire development, which included going through this cycle twice, was completed in less than three months.

Design example—computer designed C-MOS

Another approach to simplifying array design uses computer aided design based on a standard logic cell developed by ATL. This technique is being applied to the design of a low-power processor for spacecraft application. At AED Hightstown, the logic for this MARC (MOS Array Computer) has been partitioned into a number of C-MOS arrays. The logic is being implemented with a family of logic building blocks which have been laid out, digitized and stored in a computer file. A computer routine selects the cells as specified by the input logic network listing and composes the array by placing the cells along a power bus and routing the interconnections from cell to cell and to input and output pads. The output from the program is a tape which can drive a large scale artwork generator (Gerber) which generates artwork at an 80× scale. Manual layout modifications are required to meet practical requirements such as output impedance limitations and package bonding. The resulting artwork is processed in the normal manner. An example of artwork designed in this manner is shown in Fig. 9. This array is 120 by 120 mils. It implements an arithmetic and shifting function.

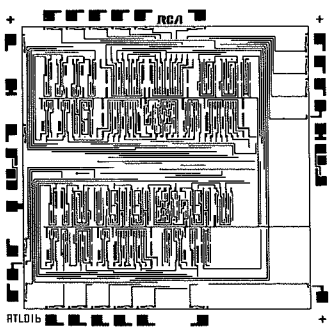


Fig. 9—Artwork for a 120×120 mil arithmetic and shifting array.

The logic cell approach offers the advantages of standardized cell layouts and computer array design, although the inherent accuracies of the computer are to a degree sacrificed by the need for manual changes in the design. One disadvantage is that a complete set of unique masks must be supplied for each design, and design changes may require a completely new set of masks. The efficiency (fraction of array area required for a design) is determined by the computer algorithms for placement and routing and the extent of manual modifications made to improve the computer layout. The computer-designed C-MOS program is being implemented jointly: AED and ATL perform logic and device design; MET fabricates masks, tests wafers, dices, packages, and does final testing; and SSTC fabricates wafers.

New developments

As the technology matures, arrays of increasing size and complexity can be fabricated on a cost competitive basis. In line with this increased capability a new family of P-MOS gate universal arrays—the GUA-4 family—has been developed with increased use of computer aids for design. The largest member of this family is a 170- by 170-mil array with 160 universal cells and 48 pads. A summary of the characteristics of the family is shown in Table V. This family of arrays has been designed using a highly standardized format. Two basic circuit cells are used: a high speed version and a low power version. Both occupy the same space on the arrays. The arrays were designed by digitizing the layout of the basic cells and associated peripheral structure (pads, protective devices and test devices) and using the SSTC PLOTS programs to step and repeat the cells into the proper locations. The same basic cells were used in designing all arrays. A regular grid structure was used to simplify interconnections between cells and reduce the chance of a layout error. Standard layouts for logic functions (*e.g.*, gates, flip-flops, and counters) will be published to aid the designer in his application. To assist further in the design of the arrays, a number of computer programs are being developed. These are described in the article titled "Digital Simulation as a Design Tool" in this issue.

Table V—GUA-4 family.

Name	*Number of cells*	*Size (mils)*	*Speed (Mb/s)*	*Type*
GUA-4	160	170×170	2.0	High speed
GUA-5	160	170×170	0.3	Low power
GUA-6	120	170×133	2.0	High speed
GUA-7	120	170×133	0.3	Low power
GUA-8	84	132×133	2.0	High speed
GUA-9	84	132×133	0.3	Low power

Important features of the arrays are:

—Ease of layout,
—Computer design compatibility,
—Elimination of metal-to-metal spacing errors,
—TTL compatibility,
—On-chip clock generation capability,
—Choice of array size,
—Alternative artwork methods,
—Device level logic flexibility,
—−55 to +125°C operation, and
—Worst case designed.

Summary

The concept of quick reaction LSI Model Shop has been verified in G&CS and utilized in several contracts requiring deliverable hardware on a tight design schedule. In these programs, the Applications Group has served as the link between the users and the wafer fabrication facilities; assisting the user in designing his arrays, being responsible for the preparation and checking of artwork and masks, and guiding the fabrication shops in processing wafers according to the required performance. In conjunction with SSTC these services are being extended to all RCA major operating units.

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Hybrid packaging for high performance

H. Fenster

Hybrid packaging of microcircuitry is both a new packaging concept and a new approach to systems design. Hybrid assemblies, in addition to being smaller, often yield more reliability, cheaper production, and better performance than comparable discrete package devices.

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received the BS in Chemical Engineering in 1948 from Pennsylvania State University and did graduate work at Drexel Institute of Technology. After graduation, he was employed by the U.S. Government performing test and development work on adhesives and synthetic resins. In 1951, he joined the International Resistance Company where he worked on electroplating processes and on inorganic coatings for resistors. From 1952 to 1955, he worked for Univac on magnetic plating for computer memories. He worked for the American Leonic Manufacturing Company from 1955 to 1959. He was vice-president in charge of electroplating fine wire and developed a patented process for the electroplating of aluminum wire. Mr. Fenster joined the RCA Semiconductor Division in 1959 where he developed and placed into pilot-scale production processes for the fabrication of "Micro-Modules." in 1961 he joined the Vector Division of United Aircraft where he was the hybrid microcircuit engineering supervisor responsible for the materials and process engineering of thick film hybrid microcircuits. In 1968 he became a member of the RCA manufacturing engineering staff for Government Engineering. Mr. Fenster assumed his present position in 1969 and is responsible for the development of advanced processes for the fabrication of thick-film hybrid circuits. Mr. Fenster is Chairman of the Keystone Chapter of ISHM. He has published and presented six technical papers and been granted two patents.

THE VERSATILITY OF hybrid packaging of microcircuitry offers the circuit designer numerous ways to package a circuit. The optimum package is determined by the environmental and system parameters required of the circuit. The hybrid microcircuit is not merely another component that can be plugged into a system; if it is properly designed and applied it is a complete subsystem.

Any electronic circuit that cannot justify a monolithic approach is a candidate for a hybrid package. Moreover, hybrid packaging complements monolithic designs as a second level system of integration. No matter how complex a monolithic chip is, it is always possible to extend its performance by adding more chips and passive components to form the hybrid subsystem package. One of the key advantages in the hybrid approach is design and packaging flexibility. This article will describe several unique packaging methods which were designed to perform some unusual electronic functions requiring high performance and small dimensions.

Laser pulser TO-5 package

Gallium arsenide injection lasers are well suited for a wide variety of military applications including optical bomb fuzes, range finders, altimeters, target designators, and intrusion and communication systems. In many of these applications both high performance and compactness are desirable. For example, the fast-response-time pulses of high-peak radiant power needed in ranging applications require compact drive circuitry for the GaAs laser diode to minimize lead length. Inductance associated with long leads degrades both the rise time and the magnitude of the current pulse and, consequently, the optical pulse output. Unnecessary lead length, as well as overall size, is minimized by incorporating the laser and the associated drive circuitry in a common package.

In applications where very fast response time and compactness are not essential, it is still convenient to incorporate as much of the peripheral circuitry as possible in the same package with the laser diode. In addition,

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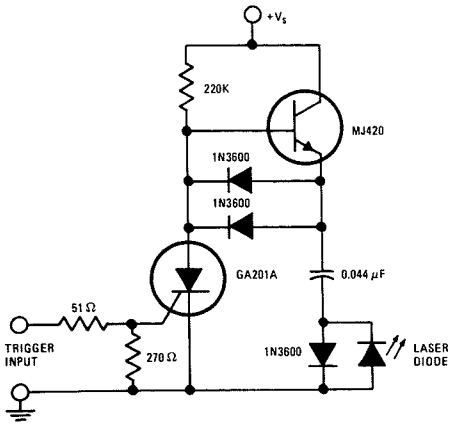

Fig. 1—Hybrid laser pulser, schematic diagram.

a hybrid laser pulse power supply is economically attractive.

A schematic diagram of the circuit which incorporates a high-speed SCR, is shown in Fig. 1. All the hybrid chips were contained in a modified TO-5 package consisting of two decks or substrates. The package was sealed by resistance welding a cap with a transparent glass lid to the header. A single RCA GaAs laser diode, with a 16-mil-emitting width, was mounted on a small block. A photomicrograph of the experimental hybrid laser pulser appears in Fig. 2. The evaluation of the hybrid circuits indicates that both good performance and high yield could be obtained, as well as small size.

The hybrid pulser exhibits typically a peak radiant power output of 17 W at room temperature with the power supply V_S at 90 V. This corresponds to a peak drive current of about 60 A. The optical output pulse duration is 40 ns at the half-power point, with 20 ns rise- and fall-time.

The advantages of stacking ceramics in a TO type package are:

—Existing discrete circuits can often be readily converted to thick film assembly and the resulting TO package can be assembled to the PC card with normal hand- or wave-soldering procedures.
—A stacked TO-5 circuit is approximately equivalent to the circuitry contained in 0.375 in square flat pack. The 12 pin TO-8 approximates a 0.625 in square package and the 16 pin TO-8, a 1 in square package.
—The stacked circuit can be divided into segments so that each wafer can be tested independently.
—The stacked technique minimizes the problem of heat degradation since particularly sensitive devices can be spread over several wafers, reducing the total exposure time for any one device.
—The high heat dissipation section of the circuit can be located directly on the header.
—Sealing the stacked TO circuit is an extremely high yield assembly operation.
—The stacked TO package is extremely rugged and can withstand considerable handling through electrical and environmental testing without damage.
—Stacked TO's are ideally suited to a high level of standardization in raw materials inventory and electrical and environmental test fixturing.
—TO packages, can result in as much as a 6:1 cost reduction over flat pack equivalents.

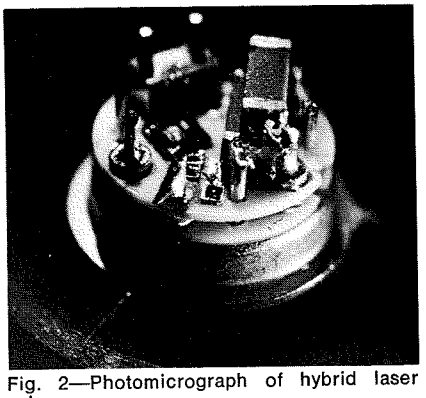

Fig. 2—Photomicrograph of hybrid laser pulser.

P-MOS cache memory—1 in by 1 in flat pack

A simplified, practical approach to the fabrication of a semiconductor memory is thick film hybrid technology, in which a number of LSI chips are interconnected on a multilayer ceramic substrate. Chips of moderate complexity may be used to increase chip yield and reduce cost. If the chips are too simple, complex interconnections are required. To achieve the desired operating speed, reliability, economy and packing density, the memory array is interconnected using hybrid circuit techniques. Since an electrical signal propagates at approximately one ft/ns, the distance of 0.250 in between the chips becomes significant. High operating speed derives from close chip spacing with short, low capacity interconnections. Compared to assembly of discrete packaged devices, hybrid assembly offers increased reliability by eliminating a whole strata of connections: those from package to printed circuit board. High speed printing techniques make production of thick film substrates economical.

A 256 by 4-bit cache memory module, built with four custom designed RCA P-MOS LSI array chips mounted on a thick film multilayer alumina ceramic is shown in Fig. 3. The ceramic substrate contains a complex multilayer pattern to interconnect the four P-MOS arrays. Each array contains 1600 transistors—thus there are 6400 transistors all interconnected in a 1 in by 1 in 60-lead flatpack. By using this hybrid technique, chips of moderate complexity may be used to increase yield and reduce cost. The number of memory array chips in each package was selected for compatibility with available package leads, and to obtain acceptable assembly yields.

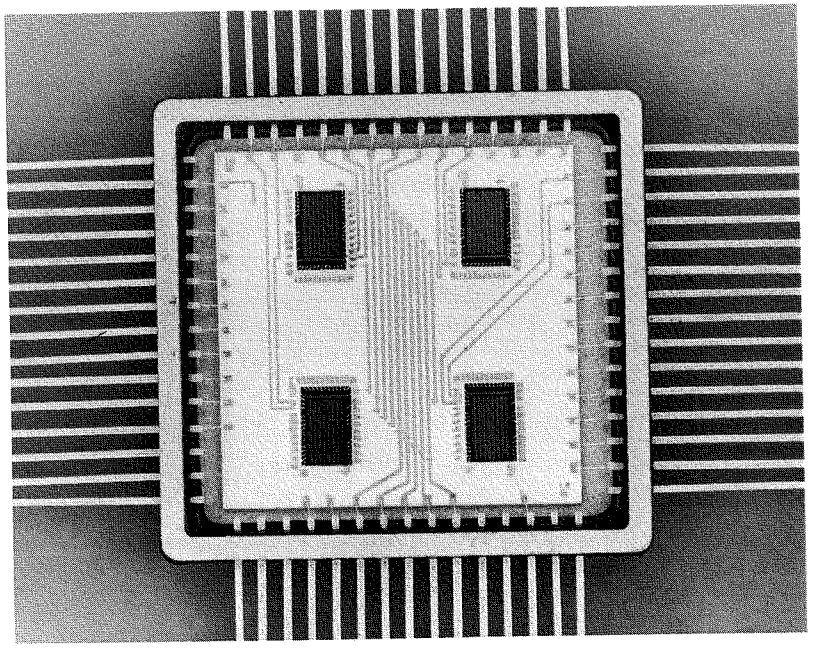

Fig. 3—256 x 4 bit code memory module.

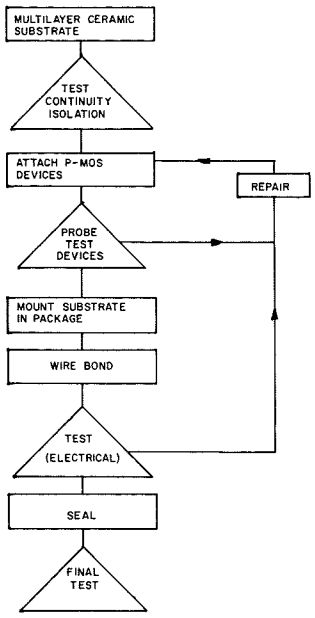

Fig. 4—Fabrication process for LSI.

The P-MOS chip is a 256-bit random access memory matrix which is bit organized (256 words of one bit each). The design details of the memory array were determined by computer simulation. The memory is compatible with T^2L logic levels and operates with external decoders and sense amplifiers, yielding an access time of 100 nsec.

The substrate contains a complex interconnect pattern with three metalized conductor layers of screened and fired thick-film inks. The fabrication process includes the following areas of technology: (See Fig. 4).

—Printing and firing of three-conductor multilayer substrates.
—Obtaining high yields of void-free insulator coatings.
—Use of screen printing for fine lines, five mils wide with five mil space.
—Printing vias in insulators with openings of ten mils × ten mils.
—Probe testing of individual chips.
—Testing of multilayer ceramic substrates.
—Replacement of chips on substrates.
—Circuit testing techniques for trouble shooting.

A 265 word by 12 bit memory module has been formed by stacking three 60-lead 1 in by 1 in flatpacks and welding the leads. The height of this stack is less than 0.5 in. These modules may be interconnected in a two dimensional array to form memories with larger word capacity or longer words.

The P-MOS Cache Memory demonstrates the advantages of thick film hybrid techniques for interconnecting LSI chips. The packing density and reliability coupled with the low cost and short lead time give thick film technology an unmatched combination of features which are certain to see increased application in the near future.

Hybrid voltage regulator module

Power supply designs have been greatly enhanced in the last several years by the many IC voltage regulators that have become available. However, these IC's have most often been used in series, shunt, and switching regulators which provide a single regulated output voltage. A small, efficient power converter with multiple outputs has been designed and developed utilizing blocking oscillator circuitry. It operates from a 28 VDC (MIL-STD-704B) primary power source and requires only a single power transistor switch and transformer. Hybrid packaging techniques have been used to reduce the size of the converter and make it applicable to compact microelectronic systems.

The power converter circuitry has been divided into four functional areas. Three of the modules were housed in a conventional 1 in by 1 in 30-lead flatpack while the hybrid voltage regulator module was packaged in a 1.375 in by 1.875 in by 0.10937 in hermetically sealed package as shown in Fig. 5. This package contains an individually mounted power transistor building block in addition to a conventional thick film alumina substrate and it contains the necessary circuits for performing the regulation function for the power converter. The ceramic substrate is 1.0 in by 1.0 in and contains 16 thick film resistors, eight ceramic chip capacitors, one operational amplifier IC chip, four transistor chips, four zener diodes and three diodes. The conductors are formed by two levels of gold thick-film ink separated by an insulating ceramic ink which acts as a low dielectric crossover material.

The individually mounted transistor is a standard RCA "building block" 2N5038 transistor, that had been modified by cutting the connection posts so that the device fits the package. The basic isolated-collector building block consists of the semiconductor chip solder-bonded to a metalized area on a beryllium oxide heat spreader. A single post is also bonded to the metalized area to provide external connections to the collector. The heat spreader is bonded onto a copper substrate. Also bonded on each end of the copper substrate are thin ceramic insulators with double connection posts solder bonded to the other side. Self-jigging ("Tinnerman" nut style) emitter and base contractor tabs are pressed over one of each of the double posts and the other end of the tabs are appropriately positioned over the solder tinned emitter and base metalizations of the transistor chip. The remaining two posts are for external connection to the emitter and base. The unit is reflow soldered at a controlled temperature to make the emitter and base connections.

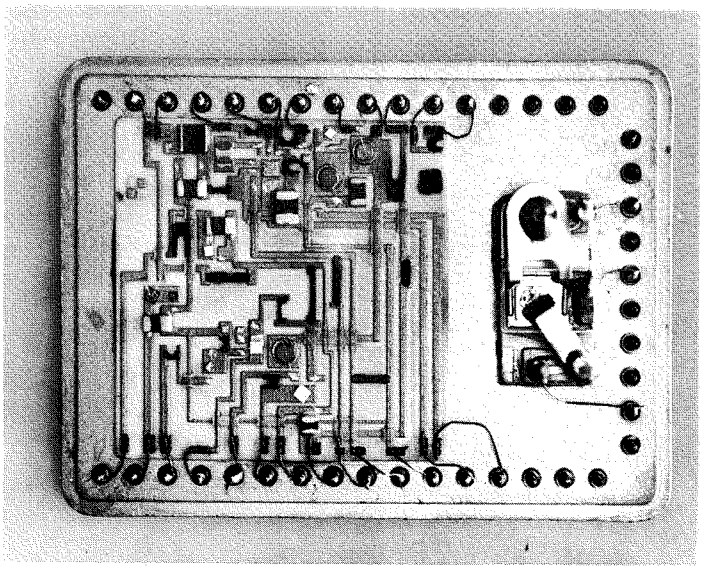

Fig. 5—Regulator module.

For the regulator circuit, the "building block" 2N5038 transistor is mounted on a package header along with a ceramic substrate containing the other circuit elements as shown in Fig. 5. The entire package is then covered and hermetically sealed. This hybrid has demonstrated that a large "building block" power transistor can be incorporated within a hermetically sealed hybrid package.

Solid state camera

The solid state camera hybrid shown in Fig. 6 is a developmental circuit which illustrates the extensive versatility and flexibility of hybrid packaging. The package contains eight P-MOS LSI self-scanned optically sensitive chips (DME 054), eight beam leaded monolithic bipolar differential amplifiers, and 16 thin film chip resistors.

Hybridization of the camera chip is necessary because the video sensors are digitally scanned in an inherently noisy system. Hybridization eliminates some of the coherent noise sources or at least causes them to be nearly identical on the four video sense lines. Care has been taken to isolate the video circuitry from all pulsed buses.

The circuitry requires a minimum of inputs. Both complementary video signals from each amplifier are brought out of the hybrid package.

The photo-sensitive array is a 138×91 mil P-MOS LSI chip containing both a photo sensitive matrix and scanning circuitry. The scanning circuitry is of the two-phase dynamic ratioless shift register type. The photo matrix is composed of four rows of 128 light sensitive elements on one mil by four mil centers. The light sensitive elements (LSE) are each configured of a pn diode connected to an MOS switch. Each LSE in a row is connected to a common 1+ diffused bus. This bus contributes appreciable impedance (16 KΩ) so provision has been made for double end connections.

Video sensing is accomplished by scanning the four rows of LSE in parellel, one LSE at a time per row from left to right across the chip. There are, therefore, four parallel video signals. However, since the array is digitally scanned, a significant amount of fixed pattern noise (FPN) is introduced on the video bus. To eliminate the FPN, one of the four rows of LSE is maintained non illuminated so that only FPN and dark current signal is present on that video bus: this signal is utilized as a reference to reject similar signals on the remaining three video buses by differential sensing. Thus there are three video signals from four rows of LSE.

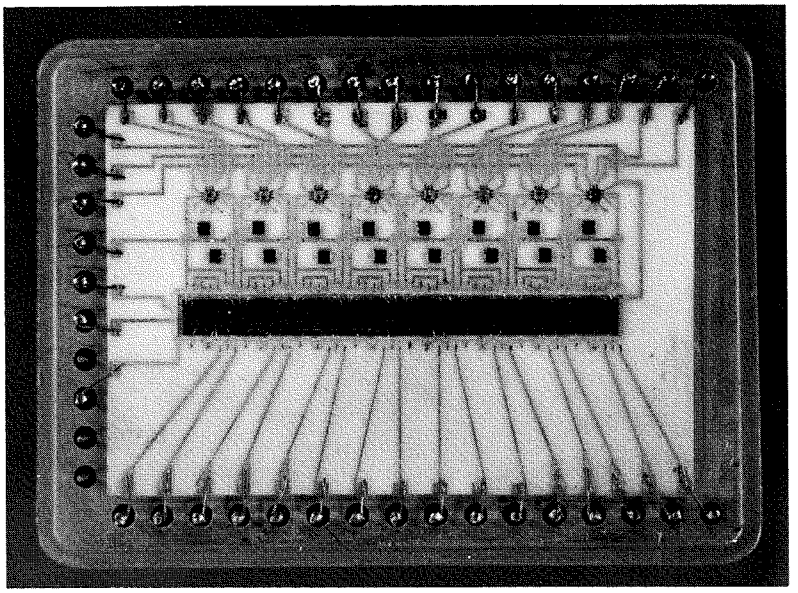

Fig. 6—Solid state camera.

The eight-chip hybrid assembly has been designed to utilize these chips in serial configuration creating a video sensor line of 1024 elements. These chips are mounted and aligned in the package within a tolerance of ±1.0 mils.

The thin film chip resistors are nichrome deposited on silicon. They are used instead of thick film screened-and-fired resistors because of their low noise contribution: approximately −40 db with 1 μV/V at 0 db over Johnson and thermal noise.

The gold thick film metalization is screened to obtain five mil wide lines and five mil spaces which are required for the beam lead devices. The beam lead amplifiers are readily mounted to the metalized substrate by wobble bonding, and the 1.0 in by 1.50 in alumina substrate is mounted on a Tek-form platform package 1.40 in by 1.90 in. The package can be hermetically sealed with a special cover containing an optically transparent lid.

Conclusion

The hybrid microcircuit may be considered as a packaging concept, an interconnection scheme or a new approach to systems design, all with unlimited possibilities. To take full advantage of these capabilities the circuit designer should be aware of the materials and processes involved in fabricating a hybrid circuit. Improved circuit performance rather than reduction in size is the chief justification for hybrid technology. The advantages of bipolar and MOS devices and thick and thin film techniques can be all combined in one package.

For cache memory applications, MOS storage elements offer low power and high packing density to the computer designer. When combined with high speed bipolar interface circuits, MOS memories fill the gap between scratch-pad and main frame memories both economically and efficiently. Future developments appear certain to widen the application of LSI MOS memories.

Acknowledgments

The Laser Pulser circuits were fabricated in cooperation with W. F. De Vilbiss of the Optical Electronics Group. The P-MOS Cache Memory was sponsored by the Princeton Research Labs under ARP 459. The Hybrid Voltage Regulator was developed for ATL of Camden with the assistance of R. B. Gordon and S. Goldfarb. The Solid State Camera hybrid circuits were conceived by E. Hermann of MET.

Digital simulation as a design tool

C. B. Davis | Dr. J. C. Miller | Dr. L. M. Rosenberg

Digital computer simulations of IC transistor circuits offer a designer far more flexibility in parameter selection than the more traditional breadboard models. Although such simulations were at one time prohibitively expensive, a currently available routine can simulate a 50 node network to within 0.1 percent accuracy for less than $100 worth of computer time.

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received the BS in electrical engineering in 1962 from Pratt Institute and the MS in electrophysics from Polytechnic Institute of Brooklyn in 1964. In 1962 he joined RCA Laboratories as a research trainee and studied the use of optical absorption properties of gaseous plasmas as a diagnostic tool. In 1965 he joined the Applied Mathematics Group at the Laboratories and worked on the application of digital computers to the solution of scientific problems. This work emphasized development of general purpose software for the computer analysis of electron optical systems. The programs developed were applied to the DC analysis of the space charge transport problem in high power klystrons. In 1967 he received an RCA Laboratories Achievement Award for work which culminated in the automated design of tools for the fabrication of magnetic deflection systems. In 1968 he received an RCA Laboratories Doctoral Study Award for a year's study toward the Ph.D in mathematics at N.Y.U. Upon returning to the Laboratories he initiated research on adaptive finite difference methods for approximating solutions to singular perturbation problems. This work led to investigation into and analysis of implicit numerical integration formulas and sparse matrix algorithms. In 1971 he transferred to the Design Automation group of the Solid State Division, Somerville and worked on developing software for transient and DC analysis of nonlinear solid state networks. Mr. Davis is a member of Tau Beta Pi, Sigma Xi, Eta Kappa Nu and ACM and is the author of several technical papers.

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received the BSEE, Summa Cum Laude, from the Polytechnic Institute of Brooklyn in 1964 and a Ph.D. from the Device Physics Group of the Electrical Engineering Department of Princeton University in 1970. His dissertation subject was "The Detectability of the Quantum Size Effect by Tunneling Spectroscopy." Mr. Rosenberg co-authored the paper "Double Injection in Insulators: Further Analytic Results" with Professor M. Lampert of Princeton University which appeared in the Journal of Applied Physics in January, 1970. He has had various summer projects involving Device Physics at Brookhaven National Laboratories (1964), General Electric Research & Development Center (1965) and Zerox Research Center (1966). He joined the Design Automation Group in RCA's Solid State Division in October, 1970 and is concerned with transistor circuit analysis programs, MOS and bipolar transistor modeling and with automated integrated circuit design rule checking. He is a member of IEEE, Tau Beta Pi & Eta Kappa Nu.

Authors Davis, Rosenberg, Miller (left to right).

DIGITAL COMPUTER SIMULATION of electronic circuits has become a viable design tool for circuit designers due to recent improvements in the numerical algorithms used to approximate network transient response. These enhanced algorithms are particularly applicable to bipolar transistor circuits, but the mathematical techniques discussed are also generally applicable (*e.g.* to cos/MOS circuit analysis) provided device models are available. Here we will pay particular attention to the measurement procedures required for accurate parameter selection for the bipolar transistor model. A similar treatment concerning cos/MOS modeling can be found in the work of J. Meyer.[1]

Our current algorithms save computation time by capitalizing on the sparseness (mostly zero structure) of the matrices associated with typical network topologies and by circumventing numerical instability-imposed constraints on the time step-size. The selection of time step is performed automatically by the algorithm to maintain its local truncation error below a threshold chosen by the user. Accuracies cited here assume that the engineer's actual circuit and devices are perfectly characterized; the only inaccuracies are those engendered by the numerical algorithms.

The two new programs written by the authors which are now available to RCA engineers employ the latest numerical methods for approximating the transient response of non-linear bipolar transistor networks. The first program is a batch FORTRAN IV program called FASTRAC (based upon improvements to the program TRAC[2]), which has a maximum capacity of 60 dependent

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nodes; the second is a FORTRAN PI program called RCAP whose capability is 15 nodes in the time-shared version and 60 nodes in the batch version. Each of these programs is serviced by a common user-oriented language which makes data input simple, fast, and error-free.

For present purposes, simulation is defined as the reproduction of certain aspects of the behavior of a system by some auxiliary system (the model). As a part of the design process, simulation often provides an easier, cheaper, and quicker means of testing design modifications than the actual system under study.

A model for a digital computer program must be numerical, but an analysis program should deal with quantities that are familiar to the user. It is therefore most convenient to define a few basic elements quantitatively and then model the components in a real system by an appropriate combination of these building blocks. For example, a circuit simulation may define circuit building blocks such as ideal resistors, capacitors, or inductors mathematically. A real component capacitor can be represented by an ideal capacitor with series and shunt resistors, and an IC (integrated circuit) resistor may be modeled to include the effects of capacitance between the resistive channel and substrate. Even a complicated device such as a bipolar transistor can be modeled in this way, as shown in Fig. 1.

Computer simulation

Digital computer simulation allows a high degree of flexibility in the selection of model parameters. This flexibility brings many benefits which ultimately mean quicker turnaround time and less overall cost.

Some of the advantages of simulation are:

—In a computer simulation, the proper reactive elements are simply specified as they exist in the proposed IC. Breadboard simulations, on the other hand, inevitably include parasitic elements. A few picofarads of stray capacitance or a few nanohenries of lead inductance can significantly distort the performance of nanosecond devices.

—A proposed IC containing proposed transistors can be simulated. This simulation, of course, is possible because the transistor model parameters can be selected by estimating the values for the proposed device.

—A better understanding can be obtained of the relation between circuit performance and component values. The engineer can vary any parameter of interest with all other parameters fixed. Such an operation is often difficult on a breadboard, especially when device parameters are involved. Moreover, the engineer can find the cause of any unexpected behavior because he knows all the ingredients built into the simulation and can vary them at will.

—It is possible to perform certain types of variational analysis simply and to predict the effect of processing spreads on crucial performance parameters. For example, resistors can be scaled up or down to determine the effect on DC and transient solutions.

—Results are equivalent to those of ideal voltage and current probes at all points in the circuit, even inaccessible internal points of devices. The engineer has, in essence, complete knowledge of circuit performance.

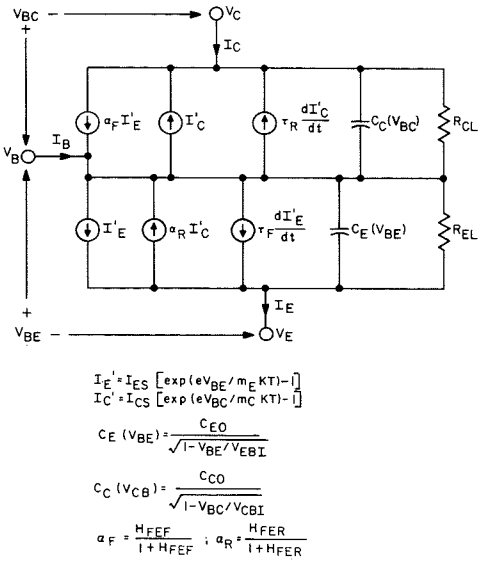


Fig. 1—Extended Ebers-Moll model of n-p-n bipolar transistor.

Limitations of computer simulation

There are two basic considerations which limit the cost-effectiveness of digital simulation: (1) model validity and parameter determination and (2) computational efficiency of algorithms used in approximating the solution to the modeling equations. In some fortunate circumstances, when the modeling equations are of a sufficiently general mathematical class, these two facets of the simulation problem can be attacked independently. Such is the case in the transient nonlinear network analysis problem where the mathematical statement of the problem is a system of first-order nonlinear ordinary differential equations with prescribed initial conditions. The engineer is insulated from the intricacies and annoyances of computational methods and forced to concentrate his efforts on model validity and parameter determination.

Model validity

The nonlinear lumped-network model is generally formulated in terms of the nodal network equations, implying that nonlinear device terminal characteristics are "built-in" features of the analysis program. Typically, the model selected for bipolar circuits is a modified Ebers-Moll model (Fig. 1) which depends on approximately 14 parameters which, in turn, are functions of the processing variables and geometric structure of the IC. Because the latter functional relationships are not explicitly known from first principles, measurements must determine model parameters for a particular class of device. Hopefully, this function will be incorporated as a standard feature of future automated product testing facilities; a library, including spread data, will be accumulated for a spectrum of device types. But currently this task is done by engineers interested in simulating. Examples in this paper illustrate how effective model parameter selection can lead to accurate simulation results and relieve the need for breadboarding. The designer, however, should be as critical of such "ersatz" breadboard results as he would be of an actual breadboard, particularly where new device structures are being modeled.

Computation cost

After the question of model and parameter determination, the cost of computation is the remaining major limitation of digital simulation. The network analysis problem is formulated as a system of first-order ordinary differential equations where the node voltages are the unknowns whose values are sought as functions of time, given the DC operating point (initial conditions) of the system.

In standard mathematical notation we can represent this system as

$$F(v', v, t) = 0 \qquad (1)$$

with the initial condition $v(t_0) = V_o$. Here the vector-valued function F has n components (for n dependent nodes),

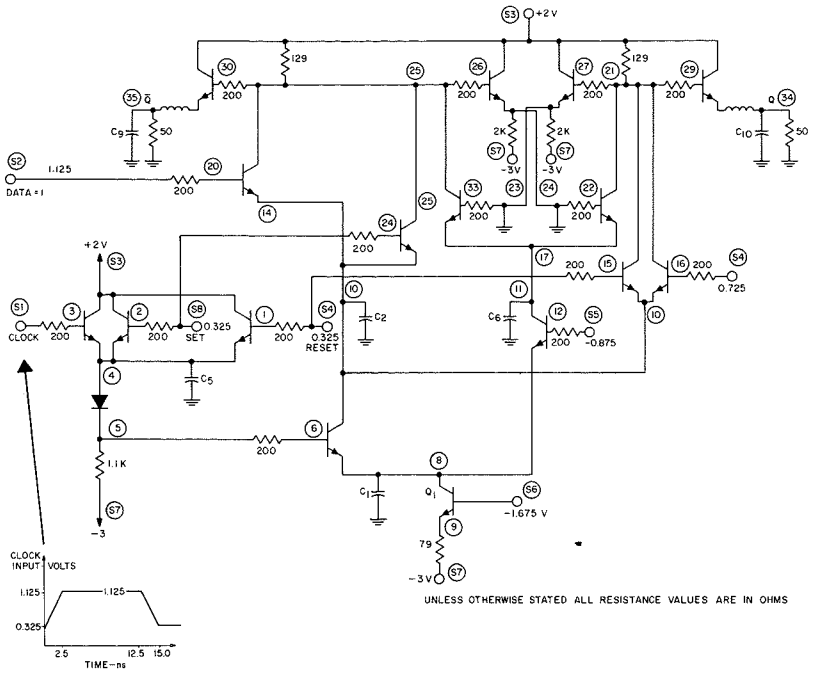


Fig. 2—Schematic of 35-node ECL set-reset flip-flop with nodes and sources numbered for computer simulation. Missing node numbers allow for addition of breadboard parasitic inductances.

each of which is the expression for net current at a node. The arguments of the components of F are the set of node voltages (the n-vector v), and their component-wise derivatives with respect to time (the n-vector v'). The system described by equation (1) has two salient features. First, each of its members does not usually depend on all the components of v and v' because typically each node is not connected to all others. And second, some members do not depend on v' because reactive elements are not connected to all nodes. These two properties lead to significant savings in programming and computational effort if properly handled by the transient analysis program.

The first programs (such as SCEPTRE[3] and ECAP[4]) devised to approximate solutions to systems in equation (1) were extremely cost-ineffective. The high cost of simulation was caused by the stability characteristics of the difference formulas used in obtaining approximate solutions. Typical electronic networks have large spreads in their time constants but the time steps of the difference formulas were limited for reasons of numerical stability by the smallest time constant present in the network regardless of whether components of the solution corresponding to this time constant were indeed active in the simulated response. Consequently, computation time estimates ran as high as 1000 hours for a transient analysis on even a powerful batch computer. Recent advances in numerical methods (A-stable difference formulas) have essentially removed these restrictions from circuit analysis algorithms.[5,6]

Numerical instability, as it is understood in the context of linear problems, is a consequence of the "parasitic" roots associated with high-order (more accurate) difference formulas. In essence, A-stable formulas damp errors which propagate by means of the parasitic roots of the difference formula. These roots if allowed to persist, would totally mask out the true solution. Difference formulas of the conventional type (so called "explicit" formulas) require that the time step be on the order of "the smallest time constant in the circuit" in order to sufficiently damp the effects of the parasitic roots. Further detailed discussion of the analysis of numerical instability may be found in the work of Klopfenstein and Davis.[7]

Using A-stable difference formulas, the program may select the time step-size dependent only on the active components of the solution and the accuracy requested, with no contraints imposed by the numerical algorithms used to approximate the solution. As might be expected, gains from such enhancements are not fully realized: these methods require as part of their execution the iterative solution of a system of nonlinear equations of dimension equal to the number of dependent variables. Still, this trade-off results in a total net gain of several orders of magnitude over the numerical instability-limited algorithms formerly used.

The gains cited are contingent on

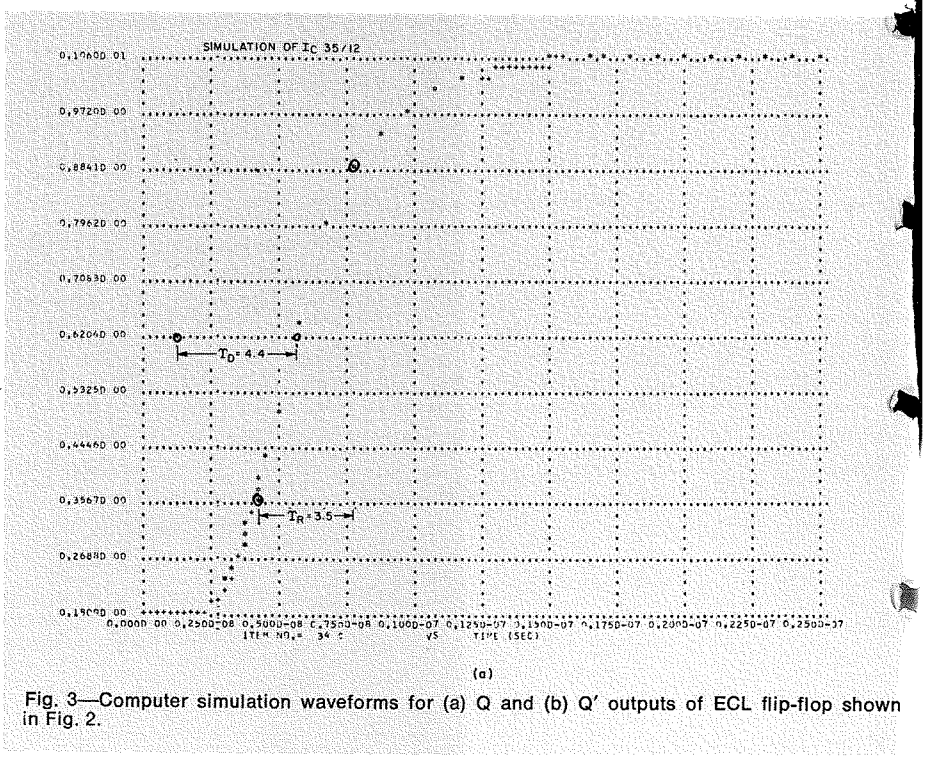


Fig. 3—Computer simulation waveforms for (a) Q and (b) Q′ outputs of ECL flip-flop shown in Fig. 2.

efficient manipulation of the sparse matrices[6] which arise in solving the systems of equations iteratively by Newton's method. In networks, because every node is not connected to every other node, the associated incidence matrices have many (usually a preponderance of) zero elements. To illustrate the savings attainable, sparse-matrix computations sped the simulation of one 35-node ECL circuit by a factor of six. At present, reasonably large (50 node) networks can be simulated to within 0.1 percent accuracy, assuming accurate modeling, on the Spectra 70/45 for under $100. Substantial gains are also anticipated from improvement of the algorithm's automatic step-selection procedures.

These increases in computational efficiency make computing more attractive than breadboarding in a number of situations, especially if some unnecessary IC fabrication cycles can be avoided. However, even with the recent advances, engineers using digital simulation tools must carefully partition a network into computable lumps (less than 50 nodes) whose interfaces can be readily modeled for loading effects. Only then can the computer resource be used efficiently.

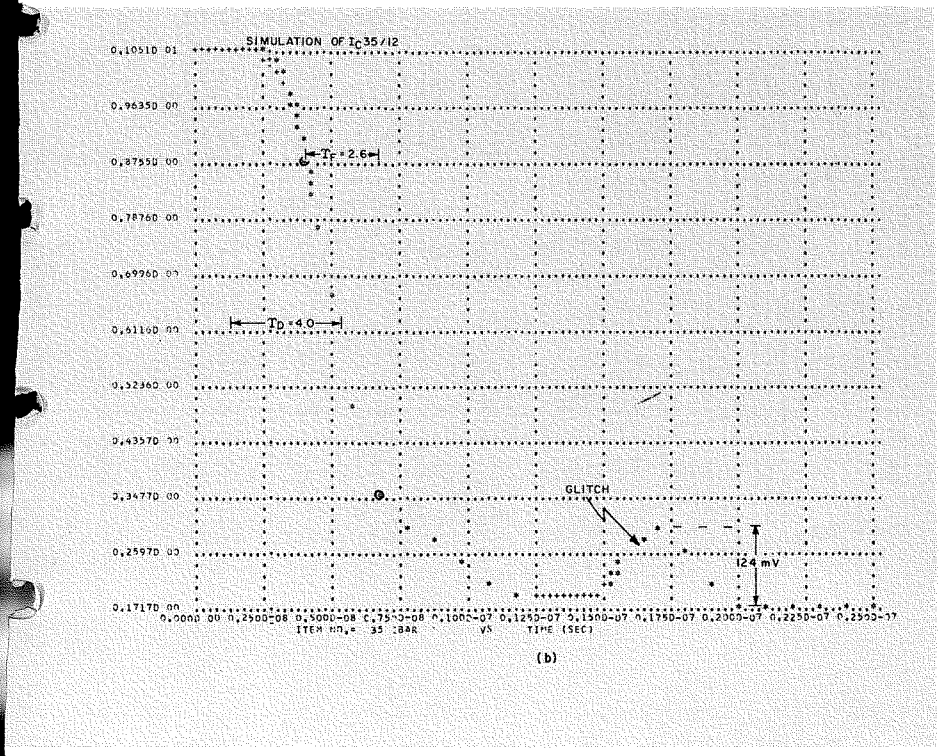
Example

As an example of computer simulation, consider an analysis of the transient response characteristics of a bipolar circuit. All computations for this case were done on the Spectra 70/45 computer. The device model used is shown in Fig. 1. As a test vehicle for this study, the transient response of the double-latch ECL flip-flop IC has been simulated using FASTRAC. This study was performed by the authors in conjunction with the Digital Bipolar Applications and Design group at RCA, Somerville. The discrete-component circuit model of the IC array considered is shown in Fig. 2 after it was simplified from a more complex network.

A series of computer simulations were run to study the effect of certain critical circuit parameters on the performance of this flip-flop. In this example, the bistable flip-flop is initially set to the logical *zero* state. The data input is fixed at logical *one*. The clock input is as sketched in the Fig. 2 schematic. This input is chosen to simulate both the "clocking in" of the data *one* and the effect of removing the clock pulse which leads to a spurious "glitch" pulse at the output. The resulting output waveforms, shown in Fig. 3, can be analyzed to yield the values of the output pulse delay, rise and fall times, and the amplitude of the "glitch."

Table I—Performance characteristics of an integrated circuit and related breadboard and computer simulation results.

Model	Emitter follower components		Parameters		Q		Q		Glitch
	L_O nH	C_O pF	C_E pF	C_L pF	τ_{Delay} ns	τ_{Rise} ns	τ_{Delay} ns	τ_{Fall} ns	mV
Breadboard	30	5	—	—	3.6	2.6	3.6	2.0	45
SIMI	30	5	—	—	3.0	3.0	2.88	2.5	64
BREDSIM	50	20	—	—	3.75	2.75	3.57	2.24	52
ICSIM	40	20	2	2	3.32	2.58	3.25	2.32	47
ICSIM2	40	20	6	2	3.4	2.5	3.0	1.8	115
IC	—	—	—	—	3.3	2.5	3.0	2.0	115



(b)

The results of this simulation (SIMI) compared reasonably well with the breadboard response (Table I). The discrepancies were eliminated by remodeling the parasitic elements in the emitter-follower output circuit, and the results using this modification (BREDSIM) were in excellent agreement with those of the breadboard for the various response times, amplitude of the "glitch," and the output pulse waveshapes.

The model for the actual IC simulation (ICSIM) is identical to the final version of the breadboard simulation BREDSIM, except that the 10 nH lead inductances are eliminated and the stray capacitances used are only those associated with the IC transistors and diodes. This simulation predicts slightly smaller delay and rise times, essentially un-

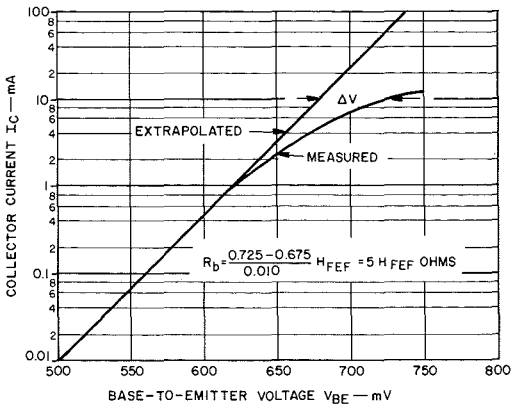


Fig. 4—Measured and linearly extrapolated curves of Log I_C as a function of V_{BE}. This plot allows evaluation of I_{ES}, m_E and R_B (upper limit). An example of R_B evaluation is shown.

changed fall time, and slightly smaller "glitch" for the IC as compared to the breadboard (Table I). The effect on IC response times and "glitch" amplitude were found as a function of a number of circuit parameters including emitter capacitance C_E and latch capacitance C_L. Results showed that the "glitch" amplitude sensitivity is 17 and 4 mV/pF for C_E and C_L respectively. These values compare with 15 and 7 mV/pF found for the breadboard. The apparent discrepancy in the values for "glitch" sensitivity on C_L is probably due to the suspected leakage current in the breadboard because this sensitivity really depends on stored charge CV and not on capacitance alone. These and other results are in good agreement with what has been observed on the breadboard.

Near the end of this study, a prototype of a slightly different IC became available. To compare the simulation to this circuit, ICSIM was modified to reflect a significant difference between these circuits. For this purpose the capacitance at node 7 was increased to 6 pF (the major difference between the circuits is the number of emitters connected at node 7). The results of this simulation (ICSIM2) and the performance of the IC (IC2) are also shown in Table I.

The circuit under study (35 nodes) requires about 15 minutes of Spectra 70/45 computer time (about $50) using FASTRAC. A similar run using the original TRAC package would require about 1.5 hours. This study demonstrates the feasibility of using a computer breadboard as a design tool.

Problems associated with computer simulation have been the inconvenient and error-prone requirements of inputting data to the simulation program. This problem has been alleviated with a time sharing front end program which accepts a free-format conversational language. It generates the data required by the FASTRAC program and also checks for errors. A simple time-sharing command submits these data to the batch computer. The use of this front end significantly reduces the time and effort required to perform simulations.

Modeling and parameterization

A significant aspect of circuit simulation involves the nature of the models used for the circuit components and the determination of the parameters for these models. In fact, given the type of numerical algorithms now available, it is generally true that the accuracy of any simulation will depend solely on the applicability of the models used and the proper determination of their parameters. This aspect of simulation will be discussed for the modified Ebers-Moll model used to simulate bipolar transistors in the TRAC and FASTRAC programs. But first, the meaning of each of the components of this model shown in Fig. 1 will be described.

The current source I'_E represents the current flowing across the emitter junction in response to the voltage across that junction and is given by

$$I'_E = I_{ES}\,[exp(eV_{BE}/m_E kT) - 1] \quad (2)$$

where I_{ES} is the emitter saturation current, e is the electron charge (1.60×10^{-19} coulombs), m_E is an empirically determined constant, k is the Boltzman constant, and T is the temperature in kelvins. Transistor action occurs because a fraction α_F ($\alpha_F < 1$), of this current diffuses across the base into the collector. This fraction is represented by the controlled current source $\alpha_F I'_E$. Therefore, the current gain of an active-state transistor is given by

$$H_{FEF} \equiv I_C/I_B = \alpha_F/(1-\alpha_F) \quad (3)$$

Similarly, I_C is the current across the collector junction due to the voltage across that junction, and α_R is the fraction that diffuses to the emitter. For a transistor biased in its active state, I'_C is a small saturation current, I_{CS}, and can generally be neglected. These four current sources comprise the DC portion of the model. The leakage resistances, R_{EL} and R_{CL}, can be used to model deviations in the saturation current from the ideal diode law.

The transient response portion of the model consists of two physically distinct types of capacitances associated with each of the p-n junctions in the transistor. The transition (or depletion) capacitance arises from the change in the depletion region charge (fixed ionized impurities) due to a change in junction voltage. Its dependence on junction voltage is given by

$$C(V) = C_0/(1 - V/V_{BI})^p;\ V < V_{BI} \quad (4)$$

where p is the junction grading constant and V_{BI} the so called built-in junction voltage. The constant p is ½ for an abrupt junction and ⅓ for a linearly graded one. Actual devices usually have values of p in the above range but are not generally constant with voltage. TRAC assumes $p = ½$.

The second type of capacitance, the diffusion capacitance, is due to the storage of excess mobile charge on both sides of the depletion region. This charge forms the diffusion profile of minority carriers caused by the flow of current in the device. If the relation

$$Q = I'_E \tau_F \quad (5)$$

equates stored charge Q to the product of the number of carriers flowing through the base per unit time (I'_E) and the average time in the base per carrier (τ_F), the derivative of this expression ($dQ/dt = \tau_F dI'_E/dt$) represents the capacitive current which flows to change the amount of storage required by different values of I'_E. In this expression, τ_F is approximately equal to the minority carrier lifetime in the base, or the base transit time, whichever is smaller. A similar derivation yields the collector diffusion capacitive current, $\tau_r dI'_C/dt$. Two transition capacitances and two diffusion capacitances constitute the transient portion of the Ebers-Moll model.

Generally, the most significant problem to solve before performing a specific simulation is to properly determine the parameters for the device models. These parameters can be ob-

tained from standard device characterization measurements in a rather straightforward manner.

The required measurements are I_C as a function of V_{BE}, H_{FEF} as a function of I_C, cutoff frequency f_T as a function of I_C, and transition capacitance as a function of junction voltage for the emitter and collector junctions (an IC simulation also requires measurement of substrate capacitance as a function of substrate collector voltage). The first three measurements should be performed with a reasonable reverse bias on the collector junction for all measured points. The parameters I_{ES} and m_E can be obtained by fitting a plot of log I_C *versus* V_{BE} with a straight line (by eye) in the region of device operation, Fig. 4. Then any two points on this line can be inserted into equation (2) to yield I_{ES} and m_E. The constant α_F can be obtained from equation (3) using the value of H_{FEF} in the region of interest from the curve H_{FEF} as a function of I_C. An upper limit for the base resistance can be obtained from the deviation of the curve log I_C as a function of V_{BE} from the straight line at high current levels

$$R_B=[(V_{curve}-V_{line})/I_C]\times H_{FEF} \quad (6)$$

where R_B is the base resistance.

The parameters C_o and V_{BI} in equation (4) can be determined by plotting $1/C^2$ against V and fitting this curve with a straight line in the voltage range of interest. Then clearly C_o is the capacitive intercept on the $1/C^2$ axis and V_{BI} is the intercept on the voltage axis. The time τ_F can be estimated by inserting the maximum value of f_T from the curve of f_T as a function of I_C in the expression

$$\tau_F=2\pi\alpha_F K_\theta/f_T \quad (7)$$

where K_θ is an empirical constant that depends on the doping profile and is usually about 0.7 or 0.8.

The reverse characteristic parameters, I_{CS}, m_C and τ_R can be found in a manner completely analogous to the procedure just described for obtaining the forward characteristic parameters. However, the actual value of these parameters are relevant only if the transistor simulated becomes saturated. In the non-saturated case, the crude estimate that I_{CS} and τ_R are ten times I_{ES} and τ_F respectively, and that $m_C=m_E$ is generally an adequate procedure.

This simple parameterization procedure for the Ebers-Moll model gives accurate DC and reasonable transient-response results in the simulations we have performed. A more detailed description of this parameterization procedure, including a discussion of limitations and special considerations, can be obtained from the authors.

Possible extensions to circuit simulation capability

After consultations on engineering needs it has been concluded that the next major area of algorithm and program development will be that of sensitivity and statistical variances of circuit DC operating points as a function of spreads in circuit component values.

In addition, changes in the transistor model will be made to increase its range of applicability. This step is desirable because there are effects that are not properly modeled by the Ebers-Moll model. Some of these effects are base and collector resistance, emitter crowding, normal heating effects, avalanching, second breakdown, the Early effect (*i.e.* dependence of H_{FEF} and τ_F on V_{CB}) and high-injection effects such as base push-out. Gummel and Poon[8] have recently proposed a model which properly describes many of the effects related to high injection. However, it is not easy to determine the parameters for this model, especially when the processing parameters are not known. In addition, the physical interpretation of these parameters are not obvious and it is therefore hard to estimate appropriate value for a new device.

Most of the effects cited can be modeled empirically by allowing the model parameters to be a function of operating point, *e.g.*, functions of I_C. Other effects can be modeled similarly. Each user will have to decide for himself which parameters he would like to vary because there is a trade-off between the accuracy of the model and the ease of characterization and computing cost.

One other modeling change anticipated is to recast the basic model from an injection (Ebers-Moll) to a transport formulation. The equivalent circuit models resulting from these two approaches appear quite similar but the latter formulation more accurately models what occurs in real transistors for those regions where the models differ.[9]

Conclusion

The ideas that have been discussed in this paper have been incorporated into a new circuit analysis program called RCAP written by the Design Automation and Test Technology Department of SSTC. RCAP exists in both a time-shared and batch version. The time-shared version is particularly suited for interactive design of modest sized networks (approximately 15 nodes). These programs are available from the authors for use within RCA. Support and maintenance for RCAP is also provided by the Design Automation Department. It is expected that RCAP will supplant the earlier programs TRAC and FASTRAC.

The authors wish to emphasize that their goal is to write user-oriented programs. They would therefore appreciate suggestions from users and potential users concerning improvements and additions to their current programs, what types of new programs would be useful, and how the user-program interface should be improved.

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Radiation-resistant COS/MOS devices

L. A. Murray | Dr. J. M. Smith

MOS devices are only slightly damaged by neutron irradiations, but have in the past been extremely susceptible to damage from ionizing radiation. A number of techniques can be used to "harden" devices, i.e. to make them more radiation resistant. Of these, the radiation-resistant COS/MOS process employing an alumina-silica sandwich as a gate dielectric seems to be the most acceptable.

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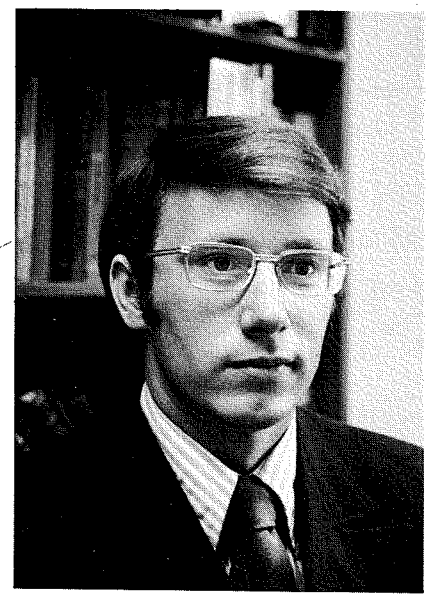
received the BS in physics from Notre Dame in 1953. After discharge from the Signal Corps in 1955, he joined ITT as a Research and Development Physicist where he grew and measured the properties of various semiconductor crystals for solid state applications. After participating in research on a microwave-infrared optical maser program in 1961, he joined RCA. Since then he has been an engineering leader heading up an assortment of diverse groups working on III-V crystal growth, laser crystal research, development of non-destructive measurement of crystal properties, fabrication of LED solid state displays, development of improved processes for MOS devices and the fabrication of COS/MOS integrated circuits. In the latter capacity, he was responsible for the development of a beam-led COS/MOS process and for the fabrication of radiation resistant COS/MOS devices among other assignments. Mr. Murray is the author of over twenty technical papers and presentations.



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AT THE INCEPTION of the MOS technology it was thought that MOS devices should have superb radiation resistance and that displacement radiation (*e.g.* neutrons) should have little effect on them because of their majority carrier nature. In contrast, radiation seriously effects minority carrier substrates and causes the beta degradation which plagues bipolar transistors. Under the action of ionizing irradiation such as X-rays, the passivating oxide is also a source of degradation in bipolars, but the level of degradation is not serious and saturates at low dosage levels.

Complementary Symmetry MOS (cos/MOS) devices offer the same radiation resistance as the MOS devices and in addition provide two more features. The first is that TREE (Transient Radiation Effects in Electronics) photocurrents for cos/MOS are smaller than those for p-channel MOS, because photocurrents generated in the n-channel MOS and the p-channel MOS drains are subtractive. And the second is that cos/MOS inverters possess a high noise immunity to both positive and negative sense voltages.

But MOS and cos/MOS devices possess their own peculiar radiation failure mechanism. This peculiarity was first brought to attention when the life expectancy of oxide passivated circuits in early satellites such as Telstar[1] turned out to be far shorter than expected. The "Achilles Heel" of the devices was found in the gate oxide which changed its character under ionizing irradiation; the resultant device parameter changes were radical and seldom saturated even at extreme doses. Among the characteristics which change under radiation are threshold, transconductance, leakage, and breakdown voltage, listed in the order of seriousness. In this article particular attention will be paid to threshold.

Both n- and p-channel MOS thresholds are strongly affected by ionizing radiation, which is defined as radiation that produces an electron-hole or ion pair as it penetrates the material. Gamma, X-rays, electrons, and protons fall into this category and their effectiveness in producing these pairs, *i.e.*, dosage, is measured in rads.

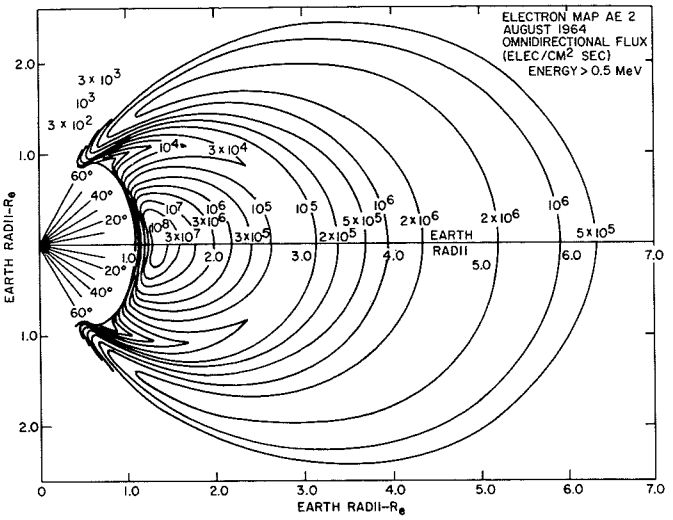

Fig. 1—The electron and proton density around earth in August, 1964.

A rad is a unit of energy deposited in a given medium (10^{-2} J/kg of medium) by ionizing radiation. Almost all of the energy deposited creates ion pairs (deposited energy can also cause displacement or excitation). The dose deposited in the medium by a given radiation flux is a function of the particle (or photon) incident upon the surface, its energy, and the material being irradiated. This latter condition is emphasized by the convention of expressing dose with the irradiated medium in parenthesis, *e.g.*, rads (Si). However, for radiation fields of intermediate energies and for material of practical interest (*i.e.*, that with low and intermediate atomic number), the dose is not a strong function of material. Therefore, in this paper, the term "rad" is unqualified by parenthesis. Dosages for a few radiation fluxes are given in Table I.

Because the first three particles shown in Table I exist in moderately high densities in the belts around Earth, they are a serious problem for satellites containing MOS devices.

As an example of the number of particles found in Earth orbit, the electron density is shown in Fig. 1 and the accumulated effect on devices is given in rads in Fig. 2. It must be emphasized that these illustrations are approximate representations of the radiation belts at a given time in the past. The present and future distributions are governed by the kinetics of loss in the Earth's atmosphere, solar activity, and cosmic rays. From the figures it can be seen that in some polar orbits annual dosages above 10^7 rads can be expected if shielding is not employed. But normally fabricated cos/MOS devices cannot withstand doses much above 10^5 rad due to a shift in threshold voltages towards a more negative value (although recent tests of the new low-voltage RCA cos/MOS indicate a substantially improved radiation tolerance). The reason for damage was first determined by Zaininger[2] and Snow.[3]

In cos/MOS devices the threshold volt-

Table I—Dosages for a few radiation fluxes

Particle	*Energy-MeV*	*Particle Fluence/Rad* ($rad^{-1}cm^{-2}$)
Electron	1	3×10^7
Proton	2	5×10^5
Proton	20	3×10^6
X-ray	2	1.5×10^9
Neutron	2	2×10^{10}

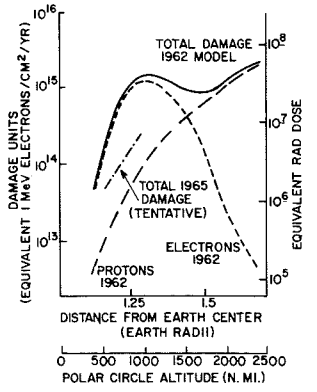

Fig. 2—Variation in device damage with distance from earth in various orbits.

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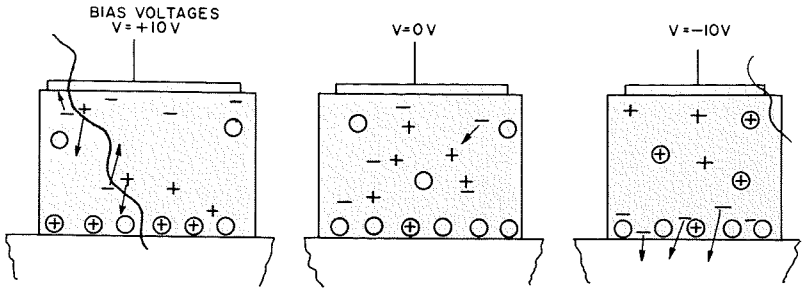

Fig. 3—Kinetics of charge trapping under various voltages in a MOS gate.

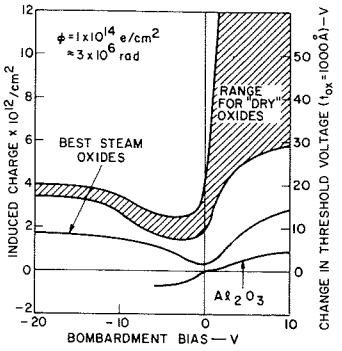

Fig. 4—Relative behavior of MOS devices under various bombardment biases.

ages for p-channel and n-channel devices respectively are given by

$$V_{TP} = -Q_{ss}/C_o - Q_{sub}/C_o - \phi_{MSP} - 2\phi_{FP} \quad (1)$$

$$V_{TN} = -Q_{ss}/C_o + Q_{well}/C_o - \phi_{MSN} + 2\phi_{FN} \quad (2)$$

$$Q_{sub,well} = (4\pi q N_{sub,well} \varepsilon \phi_{FN,FP})^{1/2}$$

Where C_o and ε are the capacitance and the permittivity of the gate oxide, respectively, q is the charge on an electron, ϕ_{MS} is the work function difference between the metal and silicon, ϕ_F is the Fermi level as measured from the midgap potential, Q_{ss} is the surface state density at the oxide-silicon interface, $Q_{sub,well}$ are the charges in the depletion layer of the substrate or well, and $N_{sub,well}$ are the doping levels of the substrate and well, respectively. The Q_{ss} arises in part from bonding discontinuities at the interface where an abrupt change from silicon to silicon dioxide is not physically possible so that a transition region develops. Within this disturbed layer a number of defects including hole traps, probably due to non-bridging oxygen atoms, are incorporated.[4] It is the capture of holes by these traps and others which are distributed throughout the oxide during irradiation which causes the threshold voltage to change as shown in Fig. 3.

At a 10 V bias on the gate, the radiation-generated pairs are separated by the field and the electrons swept into the gate metal. The holes left behind are permanently captured by those hole traps at the interface and in the body of the oxide. These trapped holes effectively increase the surface-state density, Q_{ss}, in equations (1) and (2), causing the p-thresholds to shift to more negative voltages (towards increased enhancement) and also the n-thresholds to move negative (toward depletion).

Under zero bias, the electron hole pairs are not forced to separate by drift, and the carriers tend to recombine before they can effectively diffuse to the hole traps. Thus, thresholds change only minimally.

Under a negative bias, the pairs are separated, and, although it is now the electrons that are drifted to the hole traps, a sufficient number of holes find their way to traps in the body of the insulator. The thresholds once more move negatively, although usually not to the extent that they would shift under positive bias. Fig. 4 quantitatively shows the variation of threshold with bias at a fixed dose for various insulators. The range of threshold shift is broad because the quality of the insulator is strongly process-dependent. Some process factors influencing radiation resistance are: growth rate, post-oxidation treatment, OH^- content, impurity content, and interfacial order. Neither the silicon doping level nor orientation significantly affect the radiation resistance.

Even under the optimum oxide preparation conditions used in today's production facilities, the resulting MOS devices are not adequately radiation resistant. For the improvement of radiation resistance, a number of approaches lie open as inferred from Figs. 3 and 4. These approaches include:

—Improvement of the silicon dioxide processing to lower the trap density;
—Introduction of an impurity which acts with the hole trapping species, preventing ionization;
—Addition of an electron trapping component to the gate dielectric to counter the hole traps;
—Interception of the holes before they reach the traps;
—Operation of the devices at low voltage (hence low speed);
—Operation of the devices intermittently; and
—Replacement of the SiO_2 with another insulator compatible with silicon, meeting device requirements but having fewer hole (and electron) traps.

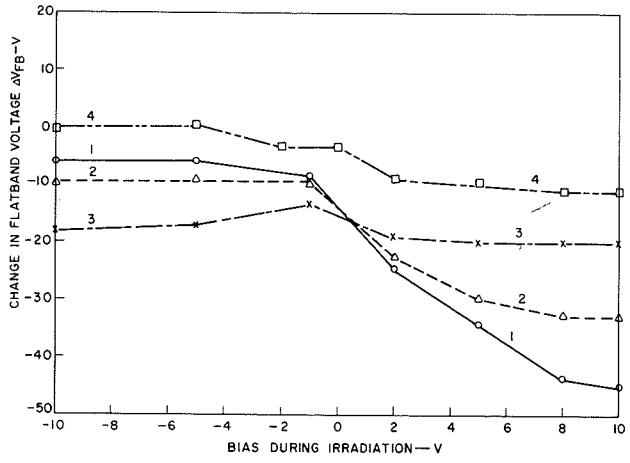

Fig. 5—Change in flat-band voltage, V_{FB} with electrode bias during electron irradiation. For curves 1, 2, and 3 the Al/Si ratios are 0.001, 0.01 and 0.1, respectively. Curve 4 shows the behavior of a Si-Al_2O_3 structure.

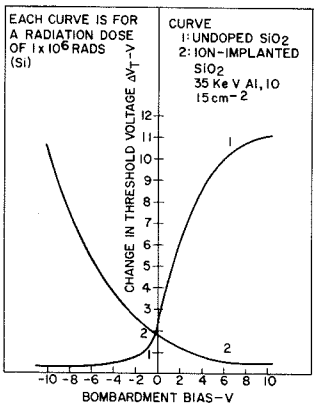

Fig. 6—Plot of change in threshold voltage vs. bombardment bias for aluminum doped SiO_2 gates (ref. 18).

Great emphasis has been given to the first approach; however, orders of magnitude decreases in trap density have not been achieved. Hole trap densities have been lowered only from the usual $3\times10^{18}/cm^3$ interfaced trap density value of commercial devices to a $10^{17}/cm^3$ value in laboratory devices.[5] The rest of this article will outline the relative successes of the other approaches listed.

Radiation hardening approaches

If a small amount of impurity is caused to enter the transition region either by diffusion or during the oxide growth, the hole trap sites are a potential bonding site. To this end aluminum,[5] molybdenum[8] and chromium[6,9] have been successfully used to heighten radiation resistance. Aluminum can be incorporated during growth and the relative change of flatband voltage with the percentage of aluminum was measured as a function of bias, as shown in Fig. 5a.

The data in Fig. 5 indicate that aluminum so incorporated into silicon dioxide makes the structure more sensitive to radiation damage (compare Fig. 5 with Fig. 4). In addition, the initial thresholds of the devices for low aluminum concentrations are more negative than for normal devices. More recent data on the effect of ion-implanted aluminum indicate that such aluminum concentrations greatly improve device resistance under positive bias (n-channel MOS) but impair it under negative bias (p-channel MOS). This effect is shown by Fig. 6.

On the other hand, chromium has been shown to significantly reduce the sensitivity of p-channel MOS structures to radiation damage, as Fig. 7 shows. Unfortunately, it only reduces the damage to p-channel MOS transistors which normally operate between zero and negative bias voltages and does not improve the performance of n-channel MOS devices, which operate between zero and positive gate voltages. The behavioral difference between the two MOS types is brought sharply into focus by Fig. 8.

Because COS/MOS circuits employ both n- and p-devices in the enhancement mode, as shown in Fig. 9, chromium doping will be useless because it is the n-channel MOS devices which change most rapidly under irradiation. Moreover, the n-channel MOS devices are driven to depletion, destroying the operation of the COS/MOS circuit, whereas the p-channel MOS move only to greater enhancement operation. The chromium process is, however, of significant value in the production of radiation resistant p-channel MOS devices, where the threshold voltage change in sharply reduced at the price of only a small increase in initial threshold voltage. Boron[6] has also been tried as a hole trap modifier but acted as neither a hardener or softener for the silicon dioxide.

A different approach towards hardening the devices has been the construc-

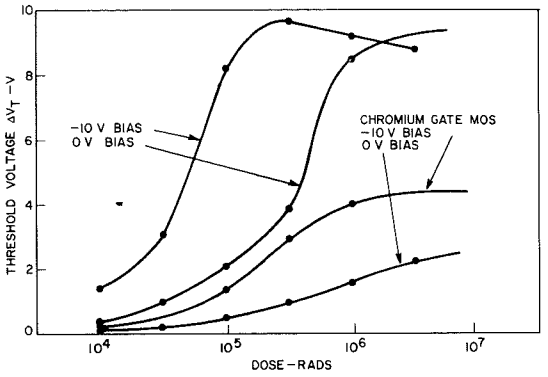

Fig. 7—Ionizing radiation damage in chromium gate and conventional MOS transistors.

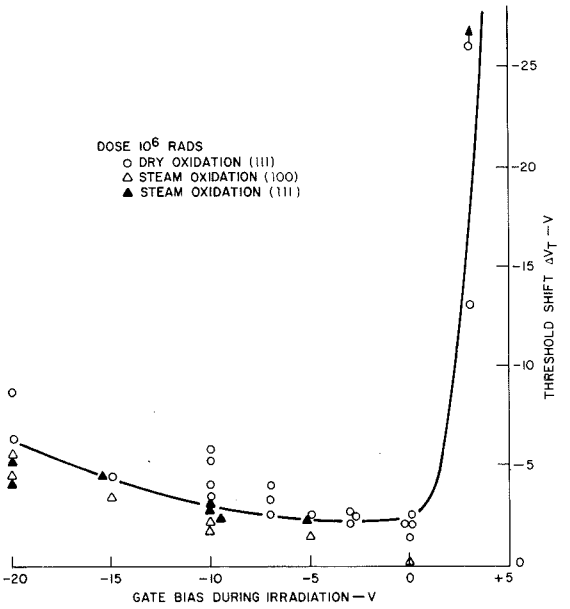

Fig. 8—Bias dependence of radiation-induced threshold shift in chromium gate MOS devices. The data scatter represents different runs.

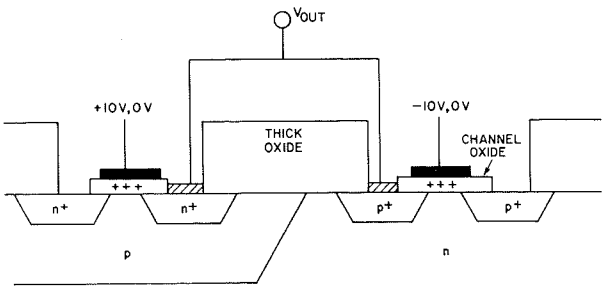

Fig. 9—Cross sectional COS/MOS inverter showing voltages applied during radiation.

tion of a composite or sandwich layer from two different materials: a silicon dioxide underlayer to provide a clean and stable interface to the silicon and a cap layer which acts counter to the silica layer during irradiation. Such a layer is phosphosilicate glass.[8,9] In contradistinction to silica, this layer either acts as a barrier impeding the exit of electrons or contains electron traps so that during irradiation the trapped electrons and holes tend to cancel the effect of each other on the device. The threshold shifts should thus be a function of the thickness and quality of the phosphosilicate layers as well as the quality of the silica layer. The dependence on thickness is indicated qualitatively by Fig. 10, which emphasizes that the radiation-hard n-channel MOS devices under positive biases can only be achieved by radiation softening of the p-channel MOS under negative biasing.

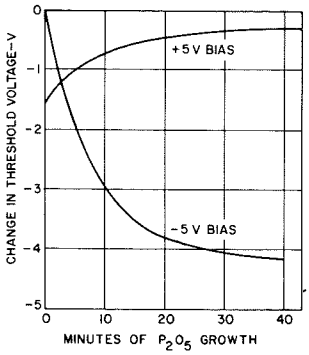

Fig. 10—Stability of MOS devices under positive and negative bias as a function of thickness (in units of growth time) of the capping layer.

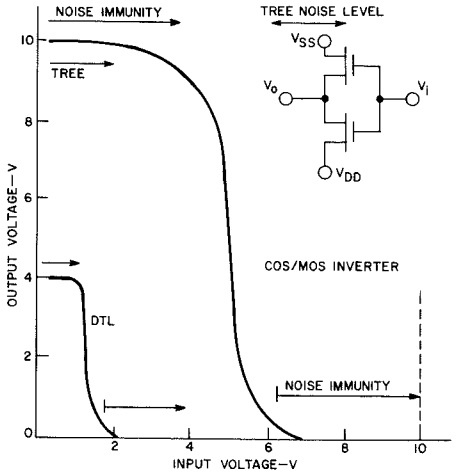

Fig. 11—Transfer characteristics of a COS/MOS inverter operating at a supply voltage of 10 V (for comparison, transfer characteristics of a DTL circuit are shown).

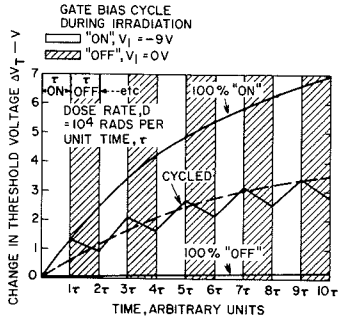

Fig. 12—Threshold shift of a typical p-channel MOS transistor with gate bias applied intermittently during irradiation.

Some improvement in radiation hardening can be achieved by considering the system rather than the oxide. For example, the threshold dosage can be increased by:

—Fabrication of n-channel units with high initial thresholds,
—Operation of the devices at low voltage, or
—Intermittent operation.

The transfer characteristic[9] of a COS/MOS inverter operating at a supply voltage of 10 V is given by Fig. 11. Because this circuit has an inherent noise immunity of 4 V, it can tolerate a −4 V change and still operate, provided threshold is above +4 V. Because normal n-channel MOS thresholds in COS/MOS are 2.0 V, the well surface concentration must be raised to secure such characteristics.

Low voltage operation (V_{SS} = 5 V) also increases the threshold dose, as was proven in Fig. 4.

Finally, if the circuit is intermittently operated[10] during irradiation, some of the damage done while the units are on is annealed while the units are off (Fig. 12).

Such operational constraints are only regarded as stop gap actions, however, and COS/MOS awaits the development of a truly radiation resistant gate dielectric.

Radiation resistant gate dielectric

Three dielectrics have recently been shown to fit into the semi-conductor processing technology: silicon nitride,[8,11] aluminum oxide,[12,13] and silicon oxynitride.[14] All show promise of being radiation resistant.

Silicon nitride has been used to fabricate MNS transistors whose threshold behavior under irradiation is superior to silica devices. An example of such behavior is given in Fig. 13.

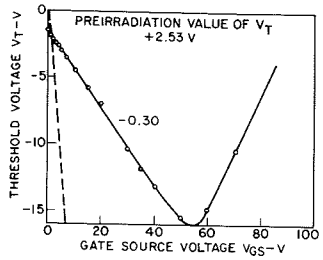

Fig. 13—Behavior of MNS transistors under irradiation.

Although radiation resistant, it has been found that silicon nitride deposited on bare silicon introduces a large number of surface states causing high p-channel thresholds, hysteresis, and instabilities, which preclude its use.

Silicon oxynitride has also been shown to be highly radiation resistant (Fig. 14, but the flatband and the surface charge are so high that p-channel MOS thresholds are in the neighborhood of −10 V. Consequently, its use is precluded.

Aluminum oxide recently has been advocated for fabrication of MAS transistors. Its variation of threshold with radiation under bias, which was shown in Fig. 4, compares very favorably with silicon oxide. When deposited upon bare silicon, aluminum oxide behaves in a manner opposite to that of SiO_2, Si_3N_4, and SiON. The charge at the interface is negative so that the threshold voltages are shifted

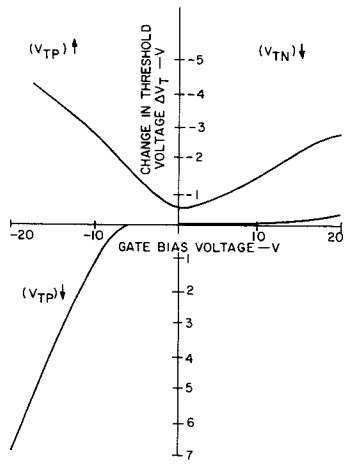

Fig. 14—Behavior of MOS transistors with silicon oxynitride gates as a function of bias voltage during irradiation.

to more positive values. The n-channel devices made from such an insulator having a 1000-Å thickness have thresholds in the range 4 to 10 V and p-channel thresholds operating in the depletion mode. A recent study[15] has indicated that under proper deposition, aluminum oxide flatbands can be achieved such that both n- and p-devices operate in the enhancement mode. An additional problem with alumina is that for voltages above a critical value, charges tunnel into the insulator and cause the threshold to change permanently.[16]

For these reasons a more conservative approach[17] to fabrication of radiation-resistant devices from alumina has been examined as an alternative to single-layer alumina. A thin underlayer of silicon dioxide (300Å) was employed between the alumina (500Å) and silicon to minimize the threshold shift and to eliminate the tunneling phenomenon. Fabrication of COS/MOS devices with such a sandwich gate results in enhancement devices having thresholds in the neighborhood of one volt. Fig. 15 shows the result of irradiating such devices under zero bias; Fig. 16 lists the device threshold shifts of a series of COS/MOS integrated circuits under various biases at a dose of 10^5 rad. The radiation shifts of similar devices made from a standard silicon dioxide are shown for a comparison value.

Until radiation resistant silicon nitride, silicon oxynitride, aluminum oxide or another more suitable gate dielectric can be deposited in a manner compatible with the high quality of present-day COS/MOS and MOS devices, the alumina-silica gate appears to be a most promising dielectric for the mating of radiation resistance with present day processing technologies.

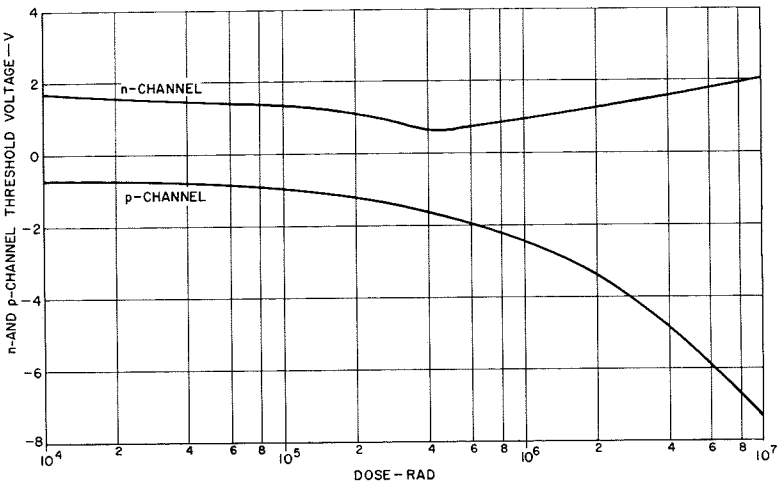

Fig. 15—Change in threshold of NMOS and PMOS transistors under zero bias as a function of radiation dare.

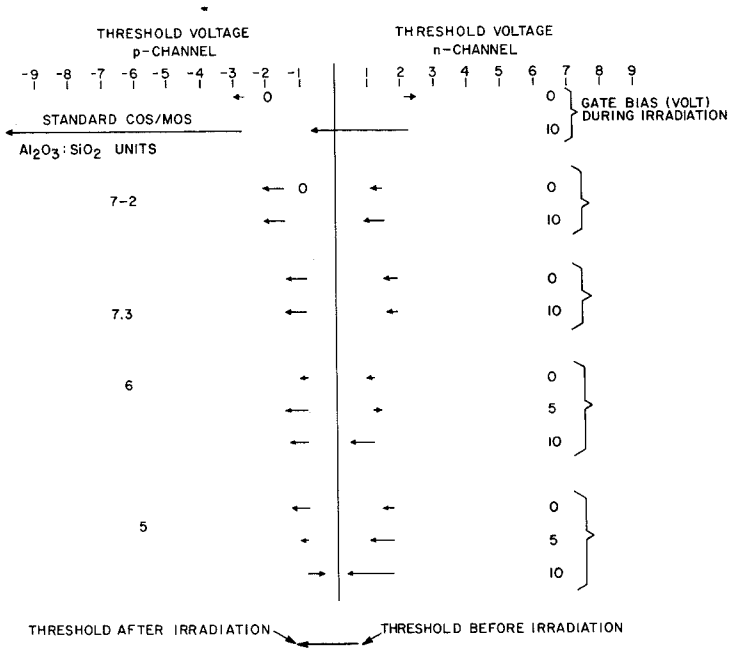

Fig. 16—Threshold shifts of various runs of CD4007 at a dose of 10^5 rad. These runs were made consecutively over a period of months. Shifts for the SiO_2 controls are shown in the upper portion of the graph.

Acknowledgements

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Determining manpower for in-process inspection by use of queuing theory

J. Davin

The Brigham model is applied on an inspection station for television picture tubes, with the object to determine the optimum number of inspectors required. The solution is obtained graphically by plotting the average number of arrivals versus cost. In a broader scope, the Brigham model is useful to determine the optimum cost of service on any queuing system where arrivals follow a Poisson distribution, service time follows an exponential distribution, and the product to be serviced is selected at random.

CONVENTIONAL LABOR STANDARDS are frequently applied to a manufacturing schedule to determine manpower requirements. Usually, in converting a manufacturing schedule into manpower requirements, additivity of labor standards is assumed; however, in certain special cases where unavoidable delays or idle time and other factors are part of the daily operations, the assumption of additivity of the labor standard may not be tenable.

One such operation is the inspection of television picture tubes as they are transferred from one conveyor line to another, during the course of manufacture.

This paper is based on a similar application designed by Sespaniak[1] and deals specifically with the manner in which queuing theory has been applied to determine the optimum number of inspectors needed to meet a given schedule. This application minimizes the total costs of inspection and inspector idle time caused by production delays.

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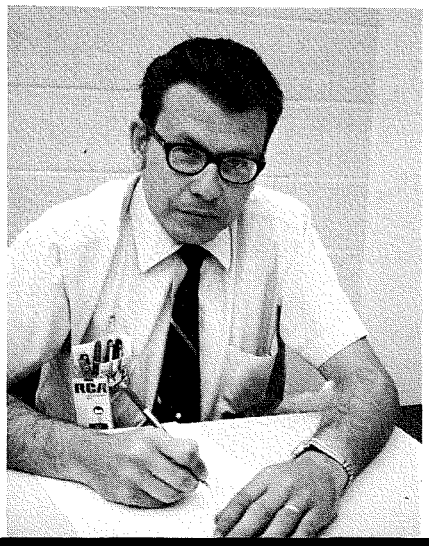

Inspection

Inspection process

In-process inspection is defined as an inspection operation which occurs while the product, in this case television picture tubes, is in the manufacturing process. Inspection takes place at several points, and the inspection must be completed before the picture tube may proceed to the next process.

There are several types of picture tubes, with each type having its own set of specifications; this results in a considerable variation in inspection requirements and causes the inspection time to vary according to some statistical distribution. Tubes of different types arrive at the inspection station in a random manner.

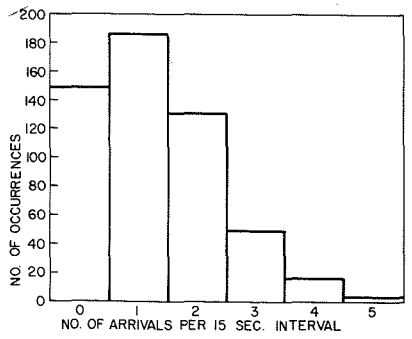

Fig. 1—Poisson distribution of arrivals.

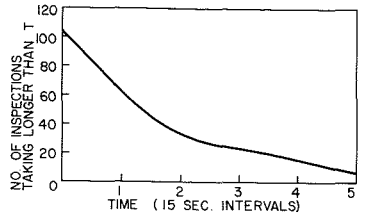

Fig. 2—Exponential distribution of inspection times.

Samples of arrivals for inspection and duration of inspection times were taken and recorded.

Arrivals for inspection

Intervals of 15 seconds were used for convenience. The frequency distribution of arrivals, shown in Fig. 1, is:

N	F
0	149
1	186
2	130
3	49
4	16
5	3

where N is the number of arrivals per 15 second interval and F is the number of occurrences.

Inspection time

Again, using 15 second intervals, the cumulative frequency distribution of inspection time, shown in Fig. 2, is:

T	F
0	105
1	65
2	33
3	25
4	16
5	6

where T is the 15 second time interval and F is the number of inspections taking longer than T.

Selection for inspection

The selection for inspection is not necessarily performed on a "first-come, first-served" basis; since tubes ride around on a conveyor line, one is picked at random, inspected, and then transferred to another conveyor line; then, another tube is selected at random from the incoming conveyor line, and the same inspection and transfer process is repeated. Therefore, the selection for inspection is essentially random since two subsequent tubes on the inspection are not always subsequent tubes on the conveyor line.

Fitting distribution to data

Distribution of arrivals

A Poisson distribution was assumed for the arrivals, compared to the theoretical Poisson distribution, and the Chi-Square test for goodness of fit was applied.

Poisson distribution: $f(x;\lambda) = e^{-\lambda}\ \lambda^x / x!$ for $x = 0,1,2 \cdots$. As determined from our sample distribution, λ is approximately 1.3. Using Poisson probabilities from Poisson distribution function tables, the following data was tabulated:

Number of arrivals/ 15 sec.	Observed frequencies	Poisson probabilities	Expected frequencies
0	149	.273	145.5
1	186	.354	188.7
2	130	.230	122.6
3	49	.100	53.3
4	16	.032	17.1
5	3	.009	4.8

Test of the null hypothesis that the data come from a population having a Poisson distribution (against the alternative that the population has some other distribution) was based on the statistic:

$$\chi^2 = \sum_{i=1}^{k} \frac{(f_i - e_i)^2}{e_i}$$

where f_i and e_i are the corresponding observed and expected frequencies.

Application of this test showed $\chi^2 = 1.72$ which is less than 9.4888, the value of $\chi^2_{.05}$ for $6-2=4$ degrees of freedom, and the conclusion was reached that the Poisson distribution provided a good fit.

Distribution of inspection times

An exponential distribution was assumed for the inspection times and essentially the same procedure as for the Poisson distribution was followed.

Exponential distribution:

$$G(>T) = 105\ e^{-T/h}$$

where h is the mean inspection time and was determined from the sample distribution to be 1.933. By use of a computer, the theoretical exponential distribution was generated and the following data was tabulated:

15 sec. time interval	*No. of inspections taking longer than T.* *Actual*	*Expected*
0	105	105.0
1	65	62.6
2	33	37.3
3	25	22.2
4	16	13.3
5	6	7.9

Using the same test statistic as for the Poisson distribution, $\chi^2 = 1.66$. This again is less than 9.4888, the value of $\chi^2_{.05}$ for $6-2=4$ degrees of freedom, and the conclusion was reached that the exponential distribution provides a good fit.

Queuing model

The queuing model used by Brigham[1] fits the conditions described above. The assumptions are Poisson arrival distribution, exponential inspection time distribution, and random selection for inspection. The data and the Chi-Square tests support the assumption of the Poisson distribution for arrivals and the exponential distribution for inspection times. Actual observations revealed that the selection for inspection was performed at random.

The Brigham model, based on the forementioned assumptions, is the following:

$$P = \frac{a^c}{(c-1)!\,(c-a)}\left[1 + \frac{a}{1!} + \frac{a^2}{2!} + \cdots + \frac{a^{(c-1)}}{(c-1)!} + \frac{a^c}{(c-1)!\,(c-a)}\right]^{-1}$$

for $c > a$ and

$$C' = (c-a) + raP/(c-a)$$

where a is the number of arrivals per mean inspection time; c is the number of inspectors; r_a is the cost of delaying the inspection station per unit time; r_c is the cost of idle time for the inspector per unit time; $r = r_a/r_c$ is the ratio of the costs of times; P is the probability of an inspection station being delayed; and C' is normalized cost.

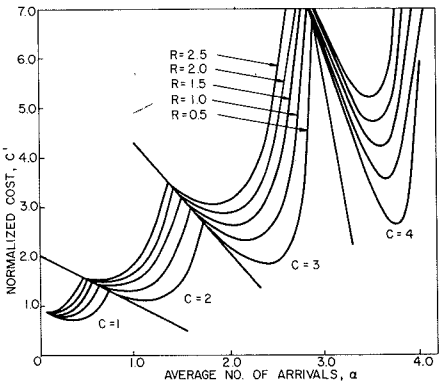

Fig. 3—Normalized total cost of waiting times, C', as a function of average number of arrivals per mean inspection time.

Determining the number of inspectors

Application of above equations to several combinations of average number of arrivals per mean inspection time and ratios of costs of times for several numbers of inspectors produced the results shown in Fig. 3. The average number of arrivals per mean inspection time can be calculated by multiplying the expected number of inspections per day by the mean inspection time and dividing by the working time per day. Once the average number of arrivals per mean inspection time and the appropriate ratio of the costs of times is known, the optimum number of inspectors can be determined from the graph.

To use the graph, select the family of curves with the appropriate ratio of the costs of times. Find the average number of arrivals per inspection time a on the horizontal axis and project a line vertically to the appropriate ratio of the costs of times curve. Read the c number between the oblique lines. The c number is the optimum number of inspectors for the calculated average number of arrivals per mean inspection time a and the ratio of the costs of times r.

Conclusions

The method of using queuing theory as outlined here does not necessarily have to be confined to determine optimum manpower requirements, but can be used on such applications as evaluation of inspection performance over a period of time, or can be used on test inspection, shipping and receiving, and maintenance and repair.

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Books by RCA authors

Presented here are brief descriptions of technical books which have recently been authored by RCA scientists and engineers, or to which they have made major contributions. Readers interested in any of these texts should contact their RCA Technical Library or their usual book supplier. For previous reviews of other books by RCA authors, see the August-September 1969 and August-September 1970 issues of the RCA ENGINEER. RCA authors who have recently published books and who were not cited in these listings should contact the editors, Bldg. 2-8, Camden, Ext. PC-4018.

Photoelectric Imaging Devices
Vol. I: Physical Processes and Methods of Analysis
Vol. II: Devices and Their Evaluation

L. D. Miller
(contributor)
RCA Industrial
Tube Division
Lancaster, Pa.

E. M. Musselman
(contributor)
RCA Industrial
Tube Division
Lancaster, Pa.

This two volume series, edited by Lucien M. Biberman and Sol Nudelman, is an instructional guide in the field of photoelectronic image devices, covering optical physics and engineering and offering detailed discussions and judgements on components, existing devices, and research. The two volumes together cover the bulk of significant information now available on image-forming photoelectronic devices.

Mr. Miller contributed a chapter on "Transfer Characteristics and Spectral Response of Television Camera Tubes" to Volume I while Mr. Musselman wrote a chapter covering the "New Image Isocon—Its Performance Compared to the Image Orthicon" for the second volume. *(Plenum Press, New York, 1971; price $25.00 one volume, $40.00 two volumes).*

L. D. MILLER received his BS degree in Electrical Engineering from the University of Delaware in 1952, after which he joined RCA's specialized training program. After completing this program, he was assigned to the Tube Division in Lancaster, Pa., working on the tri-color kinescope in the Tube Development Shop. In September 1955 he joined the Camera Tube Design Group working on vidicons. From 1959 to 1970 he worked on the development of an infrared sensitive vidicon. For the past year he has worked principally on the development of improved magnetic focus and deflection assemblies for television camera tubes. He received an MS degree in Physics from Franklin and Marshall College evening graduate division in 1965. Mr. Miller is a member of IEEE, Tau Beta Pi, Sigma Pi Sigma and IRIS. He served on the IRIS working panel on determining methods of making measurements for infrared camera tubes.

E. M. MUSSELMAN received the BSEE from the University of Pennsylvania in 1948. He joined RCA Lancaster in 1948 as a manufacturing engineer. He was promoted to Manager, Camera Tube Factory Engineering in 1956. In 1959, he was made Manager, Developmental Types and Facilities for the Pickup Tube Factory. Mr. Musselman was assigned to Storage Tube Product Development in 1960. In this capacity, he was responsible for the design of scan converters, including transmission type. He is co-holder of a US Patent for "Insulated Mesh Assembly for Vidicons", and also holds a patent on an improved target support structure for pickup tubes. Mr. Musselman is a member of Eta Kappa Nu, Tau Beta Pi, Sigma Tau and IEEE.

Value Analysis to Improve Productivity

Carlos Fallon
Value Analysis
Corporate Staff
Camden, New Jersey

Value analysis is one of the best ways to improve the personal productivity of industrial employees, from top management on down. *Value Analysis to Improve Productivity* presents a strategy of behavior leading to better decisions on product value and to better patterns of individual performance. In an anecdotal way, the author emphasizes the validity of the source, usefulness, selective power and predictive potential of information. He describes value analysis (what it is, who does it, and how) and gives the reader step-by-step outlines for analyzing value, directing the work of value task groups, and for planning, organizing and conducting multiple-task value analysis workshops. Three appendices discuss mathematics, measurement, and professional foundations. Purchasing, product, or cost reduction managers as well as industrial buyers, product, manufacturing, or industrial engineers will all find this book useful. *(Wiley Interscience, New York, 1971; 345 pp.; price, $14.95)*

CARLOS FALLON received his education as a Columbian naval officer at the *Escuela Militar de Cadetes* and under the British and U.S. naval missions to Columbia. He served as technical advisor to the minister of war, supervisor of naval construction and repair, and finally as chief of staff of the small but relatively modern Colombian navy. In 1941 he came to the United States as a naval architect and mechanical engineer. After Pearl Harbor he served in the Army Air Corps as a combat intelligence officer. Mr. Fallon's engineering experience encompasses missile-borne and ground telemetry equipment, nucleonics instrumentation, and missile launching system design. In addition to his work in RCA's plants throughout the world, he has lectured on value analysis in England, Norway, Sweden, and Denmark. In September 1968 Mr. Fallon gave the invited address at the international meeting of the Scandinavian Society of Value Analysis. He is a member of the Society of American Value Engineers, American Society of Mechanical Engineers, Mathematical Association of America, and the Canadian Mathematical Congress.

Purification of Inorganic and Organic Materials: Techniques of Fractional Solidification

Werner Kern
(contributor)
David Sarnoff
Research Center
Princeton, New Jersey

In recent years, research chemists and physicists have been increasingly concerned with the investigation of ultrapure inorganic and organic materials of hitherto unattainable purity. One of the most powerful and flexible preparative techniques of ultrapurification is fractional solidification. In this volume, edited by M. Zief of J. T. Baker Chemical Company, a number of researchers have written chapters on the purification and analysis of specific compounds by techniques including zone melting, progressive freezing, column crystallization and zone melting chromatography.

Mr. Kern contributed a chapter on the application of radioactive isotopes as analytical tools in zone-melting investigations to yield accurate data on the segregation behavior of impurities present in a column of solid material at extremely low concentrations. He discussed a novel nondestructive method based on the use of radioactive tracers that emit gamma radiation, exemplifying it with one specific research application. The chapter is entitled "Investigation of Zone-Melting Purification of Gallium Trichloride by a Radiotracer Method". *(Marcel Dekker,*

Inc., New York 1969; 318 pp.; price: $17.75.)

WERNER KERN received a certificate in chemistry in 1944 from the University of Basle, Switzerland, and a diploma in chemical technology in 1946. He published a thesis on the chromatographic isolation and characterization of fluorescing polynuclear hydrocarbons which he discovered in soil. He was analytical research chemist with Hoffman-LaRoche in Switzerland, and in 1948 transferred to their research division in New Jersey to develop new radiochemical methods. In 1955 he received an AB degree in chemistry from Rutgers University and in 1958 joined Nuclear Corporation of America where he became chief chemist directing research in nuclear and radiation chemistry. He joined RCA Electronic Components and Devices Division in 1959 primarily to investigate semiconductor contamination and surface passivation by radiochemical methods. Since 1964 he has been at RCA Laboratories as a Member of the Technical Staff, where his activity has centered in semiconductor process research in the areas of device passivation, new methods of chemical vapor deposition of dielectric films, and the development of associated analytical methods.

Mr. Kern is a member of the American Chemical Society, the Electrochemical Society, the Society of Sigma Xi, the AAAS, the Geological Society of New Jersey, and is listed in American Men in Science. He is author or co-author of about 40 scientific publications and U.S. Patents and is the recipient of an RCA Achievement Award in 1966.

Checklists for Management, Engineering, Manufacturing, and Product Assurance
Vol. I: Management Checklists

Raymond D. Black (contributor)
Missile and Surface Radar Division
Moorestown, New Jersey

This volume contains twenty-two checklists, each covering a different aspect of management—engineering, labor relations, manufacturing, marketing, financial, program management, product assurance, and more. The "checklists," concise lists of detail items, are written by recognized men in various fields of management. They form a comprehensive, useful reference manual for a wide range of management techniques in the aerospace, military, and commercial industries as well as in government agencies. The wide range of vital subjects contains a proper balance between details and the management approach to the full scope of commercial and defense industry problems.

Contained in this volume is a "Program Management Checklist" by Raymond D. Black. This checklist is designed to provide a concise, comprehensive guide to assist program managers to successfully fulfill their broad responsibilities. It addresses the major disciplines in which a Program Manager exercises his responsibility: organization, marketing policy, planning and scheduling, financial control, purchasing and subcontracting policy, and others. The checklist can be used for every program, military or commercial, regardless of size, scope or complexity, to assure that every aspect of the program receives appropriate consideration. *(Spartan Books, New York and Washington, 1971; price $14.00)*

RAYMOND D. BLACK received the BSEE degree from West Virginia University in 1952 and has since taken graduate courses at the University of Pennsylvania. He is presently Manager, System Interface Projects as a part of the AEGIS Program Management team. He has been with RCA for 19 years and has held a wide range of managerial positions. Most recently, he was Manager, Tactical Radar Systems, and responsible for the development of new lightweight surveillance radars. Prior to that he was Manager, Microcircuits Marketing, where he established a nationwide sales operation for a printed circuit component product line having application in both industrial and government equipment. Up to that time, Mr. Black had spent 13 years in various radar and missile system program management positions covering the full range of engineering development, production, field installation and support. He is the author of several technical papers and holds one patent.

Optical Processes in Semiconductors

Dr. Jacques I. Pankove
RCA Laboratories
Princeton, New Jersey

This book deals with the interactions between photons, electrons, and atoms in semiconductor crystals. These interactions comprise the absorption, transformation, modulation and generation of light.

To make the reader familiar with all the phenomena involving light in semiconductors, Professor Pankove has combined a variety of source material, journal research material, and many years of experimental research. And he has woven together all this information into a coherent form, adding new concepts collected from the current literature and from recent conferences. In the process of writing this book he evolved new insights which are published here for the first time. *(Prentice-Hall, Inc., Englewood Cliffs, N.J., 1971; price $21.00).*

DR. JACUES I. PANKOVE received the BSEE in 1944 and the MSEE in 1948, both from the University of California. In 1948 he joined the RCA Laboratories; in 1956 he received a David Sarnoff Fellowship to study at the University of Paris, where his doctoral topic was infrared radiation from surface processes in germanium. Since his return to RCA Laboratories, he has worked on superconductivity, where he has evolved several new device concepts and has done research on silicon carbide. He has investigated the optical properties of degenerate germanium and the electrical properties of tunnel diodes in germanium. Currently, he is concerned with interjection luminescence and the laser action in gallium arsenide and other compounds. Dr. Pankove has published over 20 papers and has over 30 issued patents. In addition to IEEE, he is a member of the APS, the Electrochemical Society, and Sigma Xi. During the 1968-69 academic year he was Visiting Mackay Lecturer at the University of California at Berkeley, where he presented a series of lectures on optical processes in semiconductors.

Handbook of Modern Manufacturing Management

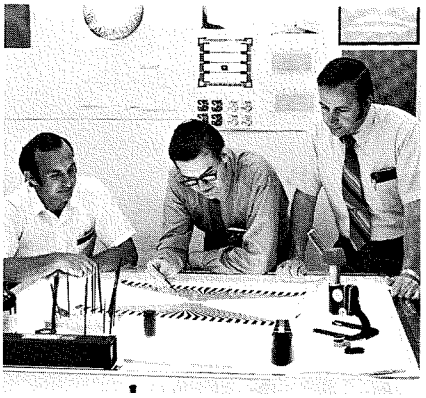
Edwin S. Shecter (contributor)
Government and Commercial Systems
Camden, New Jersey

In this handbook, a number of selected authors present various aspects of manufacturing management methodology. Subjects include manufacturing methods, training and motivation, cost controls, and other related subjects.

Mr. Shecter's chapter, "Developing a Quality-minded Workforce," deals with behavioral sciences principles and means of implementation. Experiences are related to a particular RCA facility and deal with motivational concepts in manufacturing, engineering, and clerical operations. *(McGraw-Hill Company, New York, 1970; price, $24.50)*

EDWIN S. SHECTER received the BSEE from the City College of New York in 1949 and the MS in industrial engineering from Columbia University in 1950. He also obtained the MS in applied statistics from Rutgers University in 1962. Mr. Shecter has been teaching statistical quality control and quality management at Rutgers since 1963. He is presently manager, G&CS Quality Assurance, responsible for providing quality assurance support to all G&CS divisions. He is a member of the Quality Assurance G&CS Hybrid Council and represented RCA on the Aerospace Industries Association Quality Assurance Committee. He is also an associate member of the Society of Sigma Xi and a Fellow of the American Society for Quality Control, in which he has held several section and national offices.

Handbook of Materials and Processes for Electronics



From left to right, authors Davidson, Hook, and Ryan.

Robert J. Ryan
(contributor)
Dr. E. B. Davidson
(contributor)
Harvey Hook
(contributor)
RCA Laboratories
Princeton, New Jersey

Editor Charles A. Harper of the Westinghouse Electric Corporation Aerospace Division has assembled a handbook of data, basic principles, and applications guidelines for the whole range of materials and processes used in the electronic and electrical industries. Twenty-one specialists have contributed authoritative papers on such topics as "Elastomers" "Semiconductor Materials," and "Metallic and Chemical Finishes on Metals and Nonconductors." The book should be a useful working tool for engineers and technical personnel in the electronics and electrical industries and for persons supplying or marketing to those industries.

Mr. Ryan, Mr. Hook, and Dr. Davidson contributed a chapter on "Photofabrication" which gives data and guidance on the important photofabrication materials and processes. *(McGraw-Hill Book Co., New York, 1971, 1344 pp., ill.; price $33.50).*

ROBERT J. RYAN received the BA degree in 1952 from LaSalle College of Philadelphia, and the MS degree in Chemistry from Drexel University in 1963. Mr. Ryan joined the Electrochemical Group of the RCA Semi-conductor and Materials Division in 1957 and contributed to the investigation of N-Halogen organic compounds for use as cathode materials in reserve batteries. He received the RCA Engineering Achievement Award in 1963 in recognition of his efforts in developing an electrochemical system for use in missile applications. In 1964, Mr. Ryan joined the RCA Laboratories Process Research and Development Laboratory as a Member of the Technical Staff. He was engaged in the development of interconnection processes for electronic components and subsystems. Mr. Ryan received Laboratories' Achievement Awards in 1965 and 1969 for development of additive multilayer printed circuit fabrication processes and materials. He is presently engaged in the development of processes and materials of holographic recording and replication of recorded information. Mr. Ryan is a member of the American Chemical Society, Sigma Chi, and the International Society for Hybrid Microelectronics and is listed in American Men of Science.

DR. EDMUND B. DAVIDSON graduated from Brooklyn College with a BS degree, *cum laude,* in 1956. He received his Ph.D in polymer chemistry from Polytechnic Institute of Brooklyn in 1961. Dr. Davidson was employed by Esso Research and Engineering Company as a polymer chemist engaged in synthesis and modification from April, 1961 through December, 1965. He joined RCA Laboratories in December, 1965 and has been working since that time on photopolymer synthesis and applications. Dr. Davidson is a member of Sigma Xi, Phi Lambda Upsilon, and the American Chemical Society.

H. O. HOOK received the BA in chemistry from Elon College in 1947, and the BEE from North Carolina State College in 1949. In 1950, he received the MSEE from the same college. Mr. Hook has been with the RCA Laboratories since 1950, where he is presently Manager of the Photomechanical and Chemical Processing Group. He holds several patents relating to display devices. As a member of the technical staff, he worked on opto-electronic computer components, vacuum technology, color picture tubes, and the optics of displays. Mr. Hook is a Senior member of IEEE and a member of the Instrument Society of America and the American Vacuum Society.

Modern Methods of Surface Analysis

Dr. Jules D. Levine
RCA Laboratories
Princeton, New Jersey

Prof. Peter Mark
Princeton University
Princeton, New Jersey

This book constitutes the proceedings of a one-day symposium held at Bell Telephone Laboratories, May 14, 1970 and sponsored by the Greater New York Chapter, Thin Film Division, American Vacuum Society. J. D. Levine was chairman. The seven papers were originally published in the journal *Surface Science.*

The first four papers deal with electron probe diagnostics (electrons in and electrons and X-rays out of the surface, as in LEED and Auger electron spectroscopy). The next two papers deal with ion diagnostics (ions in and ions out of the surface). These diagnostics help to provide a physical, chemical, and structural understanding of a wide variety of surfaces. The last paper uses this information plus electrical and optical information to infer the collective properties of electronic surface states. *(North Holland Publishing Company, Amsterdam, 1971, 223 pp.; price $12.00).*

JULES D. LEVINE received the BSME degree from Columbia in 1959 and the Ph.D. degree, specializing in surface physics, from M.I.T. in 1963. After joining RCA, he continued his theoretical and experimental surface physics investigations with particular emphasis on metallic adsorption on metals and nonmetals, and on electronic surface states on semiconductors and insulators. He has authored 30 papers and 2 books in this discipline, and has given 18 technical presentations, of which half were invited talks. Most recently, he has been developing field emission arrays for application as cold cathodes. He has been active in several planning committees for the IEEE and the American Vacuum Society.

Solid State Physics, Vol. 25

Dr. Jules D. Levine
(contributor)
RCA Laboratories
Princeton, New Jersey
and
Prof. S. G. Davison
(contributor)
University of Waterloo
Ontario, Canada

"Surface States" is an extensive review article which constitutes one third of this volume of the well-known book series. The review describes the established quantum mechanical relativistic and nonrelativistic theories of surface states as well as the more familiar semiclassical aspects such as dangling bands and Madelung sums. Special attention is given to intrinsic surface states at the semiconductor-vacuum interface for the Group IV, III-V, and II-VI semiconductors. In a lengthy chapter devoted to "Comparisons of Theory and Experiment", the major experimental techniques of surface state determination are reviewed, and the available data is correlated as far as possible with existing surface state theory. *(Edited by H. Ehrenreich, F. Seitz, and D. Turnbull, Academic Press, N.Y. 1970, 420 pp.; price $26.00).*

Silicon mosaic target—blending semiconductor and camera tube technologies

A. D. Cope

The silicon mosaic target is the first application of a semiconductor integrated array to a TV camera tube. As such, it is a replacement for the various insulating photoconductor layers which were the basis of the vidicon product line. The inherent advantages of the mosaic diode target guarantee an ever expanding list of applications. Perhaps the most dramatic evidence to date is the success of this device on the Apollo 15 moon mission.

A VIDICON CAMERA TUBE employing an image transducing target consisting of a mosaic of silicon photodiodes was reported by Bell Telephone Laboratories several years ago.[1,2] This development was directed toward meeting the requirements in Bell's proposed Picturephone system. At RCA, however, work on this type of photosensor concentrated on another basic question. That is, how well could a photodiode array satisfy the requirements for a television camera tube which could be operated in a conventional TV system with its demands of greater video bandwidth (5 MHz vs 1 MHz) and higher picture information content? To guide the development of such a tube, performance characteristic objectives based upon the requirements of TV systems engineers were defined. Also, modification of geometric and electrical parameters of the original silicon target was required to achieve the needed static and dynamic signal handling capability.

In a related development, a new quality level in low-light-level television was achieved with the introduction of the Silicon Intensifier Target (SIT) line of camera tubes.[3,4,5] Here, amplification and integration of low-level photoelectron currents are obtained from the silicon mosaic target as a result of impact ionization. The SIT tube approaches the fundamental limits for low-light sensing.

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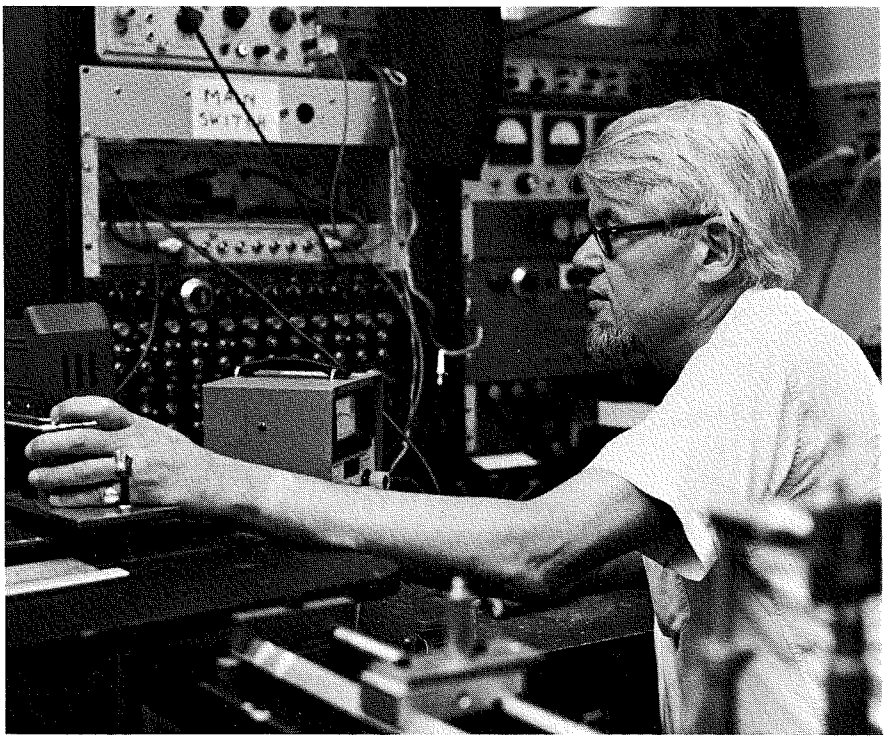
A. Danforth Cope, Electro-Optics Laboratory, Electronic Components, David Sarnoff Research Center, Princeton, New Jersey

received the BA degree from Colgate Universtiy in 1938 and continued in graduate study at Yale University. He joined RCA in 1941 as a manufacturing process and development engineer working with gas-filled phototubes and TV camera tubes at the Harrison, N.J., and Lancaster, Pa., plants of the Electron Tube Division. Mr. Cope served as liaison engineer in carrying the image orthicon from research into production during 1943 and 1944. In 1949, he transferred to RCA Laboratories, Princeton, N.J. From 1949 to 1960, Mr. Cope was engaged in research related to TV camera tubes, particularly the photoconductor problems related to the vidicon. He was involved in the initial conception and experimental verification of the phototape idea. Late in 1960, Mr. Cope joined the Physical Research Group of the Astro-Electronics Division to continue work on photoconductor materials and their application in image sensing systems. In 1966, he joined the Electro-Optics Laboratory of Electronic Components which is maintained at the David Sarnoff Research Center. Mr. Cope served as project engineer in a research study of electron optics of the Image Isocon. More recently, he has been part of the team concerned with the development of the silicon mosaic target for the vidicon and the Silicon Intensifier Target (SIT) tube. Effort at the Electro-Optics Laboratory in Princeton has been concerned with improving techniques and adapting the silicon target for special applications. Mr. Cope has a number of patents and publications in the pickup-tube field. He is a member of Sigma Xi and the Optical Society of America. He was the recipient of RCA Laboratories Achievement Awards in 1950, 1957, and 1968.



Included among the several inherent advantages of the silicon mosaic target are:

1) Improved efficiency in the conversion of light to an electrical signal. The quantum conversion efficiency is 70 to 80% in the near ultra-violet and visible portions of the spectrum. In addition, there is useful sensitivity in the near infrared beyond one micron,
2) Freedom from photoconductive trapping effects—the major cause for image lag in other vidicon targets,
3) Greater signal handling capability with minimal damage from illumination overloads, and
4) Useful lag-free impact gain in excess of 2000 without loss of resolution or the introduction of detectable noise. In the SIT tube, a photoemitter is the primary sensor for the light image. At the lowest operating levels, the statistical noise of the low flux of primary photoelectrons is observable.
5) In situations where large extremes of scene illuminations are encountered, it is possible to maintain a fixed value for the target output current by varying the gain of the image section. The advantages of this unique versatility were demonstrated in the performance of the RCA-built Apollo 15 TV camera.

Mosaic diode action

Fig. 1 illustrates the energy band model as related to the geometric cross-section through one diode of the silicon target mosaic. In the vidicon, electron-hole pairs are generated in the n-region by the absorption of light photons with an energy of 1.1 eV or greater. In the SIT tube, photoelectrons accelerated to 1 keV or greater energy generate pairs in the silicon by impact ionization. In either case, the holes which by diffusion reach the depletion region surrounding an individual diode are drawn by the electric field into the p-region where they remain until neutralized by electrons deposited by the scanning beam. Efficient utilization of the energy in the light image incident on the photosensor of a camera tube requires that all the transduced charge be integrated during the interval between one contact by the scanning beam and the next contact one frame time later. In conventional television, this interval is 1/30 s.

The beam deposits electron charges sufficient to neutralize the accumulated positive charge at the diode thereby restoring the p-side to cathode potential (0 V). The n-side is held at a fixed positive potential, typically 8 V to 10 V. A pulse of signal current is passed through the capacitive coupling between the target and the video amplifier each time a diode is recharged by the beam. This beam is an imperfect probe that has a sizable series impedance which increases by more than an order of magnitude as the potential of the contacted element approaches within a few tenths of a volt of the beam cathode potential. With a dwell time on an individual diode of approximately 1/10 μs and a limited current density in the beam spot, both the range and the time constants associated with dynamic changes in signal level are dependent upon the diode capacitance.

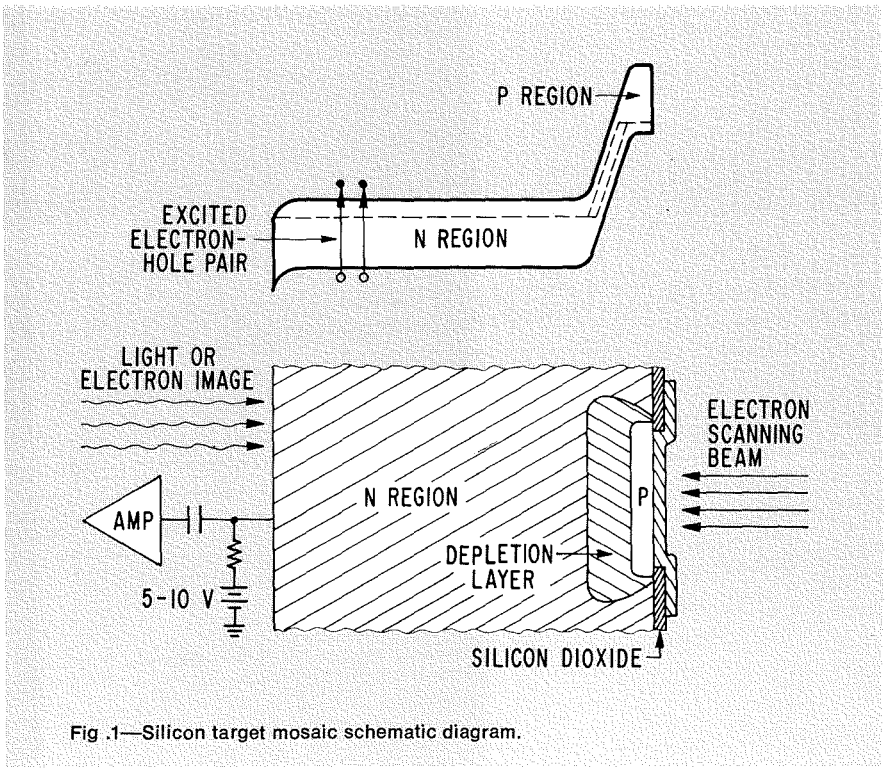


Fig .1—Silicon target mosaic schematic diagram.

Structural requirements

Viewed as a form of integrated circuit, the silicon target may seem rather simple; a mosaic of p-islands formed on an n-type wafer in a regularly spaced two-dimensional array of p-n junctions is all that is needed. However, when the requirement is added that there should be between 5×10^5 and 10^6 such diodes per square centimeter, *all* of which must function within a narrow range of characteristics, the task appears more formidable. Any diode having excess dark conductivity (high back-bias current) or any inoperative diode is visible in the video display as either a white or black spot. Thus, continued upgrading of the cosmetic quality of silicon targets is a major challenge in satisfying the requirements of broadcast television.

Fabrication of the target mosaic requires the formation of a uniform sheet of oxide on the prepared surface of the n-type silicon wafer. After photoresist printing of the diode pattern and subsequent etching of diode openings in the oxide sheet, a p-type layer of silicon is deposited and diffused into the wafer. This layer must then be cut into areas to define the individual diodes, a process which employs a second photoresist printing in conjunction with a grid pattern that is carefully aligned with the diode pattern. Following this process, material is removed from the face situated opposite to the mosaic to form a uniform lamina no thicker than 20 μm. This surface is then given additional doping to form an N^+ skin. Typically, targets having diode spacings of 12 to 14 μm are being produced, although experimental mosaics with 8 μm spacing have been worked with. Beam acceptance is enhanced by maximizing the p-area and minimizing the exposed oxide area. The dimensions of this repetitive pattern are such that optical diffraction effects create serious problems with photoresist printing, an increasingly

troublesome matter when the mosaic area is enlarged from approximately one square centimeter to several square centimeters. Fig. 2 is a micrograph of an RCA target mosaic.

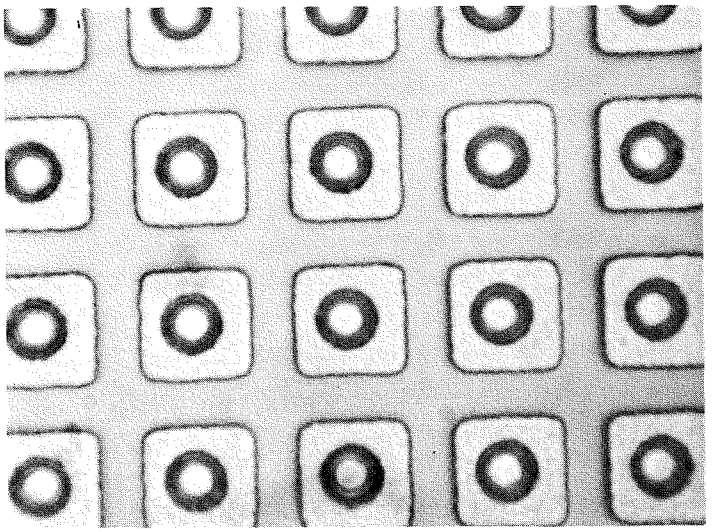


Fig. 2—Microphotograph of silicon mosaic target.

Mix of technologies

The many technologies required for the successful development of the silicon mosaic target design adopted by RCA were not to be found in any one group or location. A unique effort was mounted involving Electronic Components, the Solid-State Division, and RCA Laboratories personnel from three locations: Lancaster, Somerville, and Princeton. Under the general coordination of Dr. Ralph Simon, who at the time was Manager of the Electro-Optical Devices of EC housed at the David Sarnoff Research Center, a year's effort by the individuals listed below in (A) had evolved a basic silicon target fabrication process. Basic development continued into the second year with the addition of Lancaster personnel listed below in (B) who were charged with the responsibility for transferring to Lancaster the techniques that were being established at Princeton.

A. Original Task Group for Silicon Mosaic Target Development
Electro-Optics Technology Laboratory
Electronic Components, Princeton
Dr. Ralph E. Simon
A. D. Cope
R. L. Rodgers, III
Advanced Development Laboratory, Semiconductor Division, Somerville
Dr. E. Cave
F. Duigon
Dr. A. Blicher
Dr. R. B. Janes
J. Doyle
Semiconductor Devices Group, RCA Laboratories, Princeton
Dr. C. W. Mueller
Dr. F. Heiman

B. Prototype Target Development Task Group
Electronic Components, Lancaster
Dr. G. S. Briggs
W. H. Henry
R. L. Van Asselt
P. W. Kaseman
T. W. Edwards
Electro-Optics Technology Laboratory
Electronic Components, Princeton
J. P. Carroll

This transfer required the establishment of a base procedure and planning for the purchase, construction, and erection of the facilities needed in the clean room areas of the Lancaster plant. By the end of the second year, a pre-production line had been established at Lancaster. Meanwhile, the initial work on the SIT tube and various improvements in mask preparation and photoresist printing procedures were being continued by the three divisions. The result was an efficient and productive merging of RCA's capabilities in the development of a new product.

Performance requirements

For a camera tube to operate efficiently, certain performance criteria should be tailored to suit the planned usage. Dark current in particular controls the rate of discharge of non-illuminated diodes and, therefore, the maximum integration time allowable. Typically, at the normal bias of 8 V, the diode dark current should be less than 2×10^{-4} A (10 nA/cm^2 at normal TV scan rate). Typical target currents range from 3 to 500 nA with incandescent illumination incident on the tube face varying from 5×10^{-4} to 10^{-1} fc. Resolution in the present product is equivalent to that of other vidicons with a raster $\frac{1}{2}\times\frac{3}{8}$ in. The response is 50% at approximately 350 TV lines, with limiting resolution of 700 to 800 lines. Individual diodes are not resolved by the normal vidicon beam. The diode capacitance controls both the dynamic range of the signal current and the maximum signal storage capability of the target. The most useful range of signal charge integration per diode lies between 3×10^2 and 3×10^5 electron charges. Performance tradeoffs between speed of response and dynamic range must be made in determining the desired diode capacitance. There is no one camera tube which satisfies all operating conditions; significant improvement can be achieved by matching the target design to the system operating conditions.

Conclusion

The silicon mosaic target has been improved in diode uniformity and cosmetic quality. Increased diode density targets and simplified processings are being developed as the result of continued inputs of technology from the Solid State Division. The most troublesome fault remaining to be overcome is the spreading of small area highlights in an image when the illumination at these points is more than 100 times the maximum signal handling capability of the target. There is still room for ingenuity in furthering this significant development. However, there is every indication that the momentum developed over the past few years will be sustained.

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Automated design operations: a profile

J. P. Le Gault

To bridge the gap between concept and realization, today's design engineer must rely heavily on automated design aids. For its computer designers, RCA has established automated design operation groups at the Palm Beach Gardens and Marlboro computer plants. These groups develop an engineer's logic sketch into all the data necessary to document, manufacture, test, and maintain a design within the constraints of packaging and circuit technology.

ADVANCES IN technology bring new product requirements. To design these products requires new generations of automated design software operating in ever more complex environments. Without automated design aids, today's design engineer would be unable to implement his concepts in the real world. Between design concept and realization lies a realm of computers, graphics, operating systems software, and automated design software systems. To open this realm to the computer designer, RCA has organized Automated Design Operations groups committed to the art of design processing at the Palm Beach Gardens and Marlboro plants.

Let us define design processing as the process of transforming an engineer's logic sketch or other source document into the mass of data required to document, manufacture, test, and maintain a design. These data represent the optimum solution to the packaging problem constrained by the rules of the applicable packaging and circuit technology.

The data base is initiated by defining the physical, logical, and electrical characteristics of components used in a design and is therefore the beginning of the design processing cycle. This data base grows as analysis of the design determines the mounts, the interconnections, and the electronic elements which together form a suitable assembly.

Structure

The Automated Design Operation Group supports a continuous flow of production jobs through a human communication network which determines the plan of action required to produce the end product. Fig. 1 portrays this activity in one step of a design processing cycle. The authority relationships of the organization structure are shown in Fig. 2. The organization is designed to ensure internal coordination vertically and horizontally, and to promote teamwork.

The activities of the organization are partitioned into a series of groups, and each group contributes material or human resources to accomplish certain planned steps in a job's design processing cycle.

Production planning and control

Planning for effective handling of projected workloads, keeping records of production status, and gathering statistics useful in future planning are the primary services of the production planning and control group. This activity must develop reliable estimates of each group's capabilities for each type of design processing job.

The group audits manpower and computing time from time to time. Reliability data from the audit and actual cycle time needed to process production units are invaluable indicators of how well the organization is meeting its goals. When translated to dollars, the data become valuable in business control, cost determinations, budgeting, and billing. Although the production planning and control activity is an internal service to the organization, the reports it produces are useful to such external departments as accounting, design engineering, and facilities or services organizations.

Computer Aided Design (CAD)

The computer aided design group supports engineering by continually searching for computer aids, exploring advanced technology, and searching for new kinds of information. It provides such services as requirements analysis, software acquisition, and time-sharing terminals.

A program being added to the Computer Aided Design Library at the time of this writing is a typical example of the value of CAD to the Palm Beach facility. The program, TESTSIM, written by C. H. Kraft of RCA's Solid State Division, evaluates the effectiveness of a functional test of a logic network. The logic network and the input test waveforms are described by the user; the program simulates the network under every possible single fault condition and determines which

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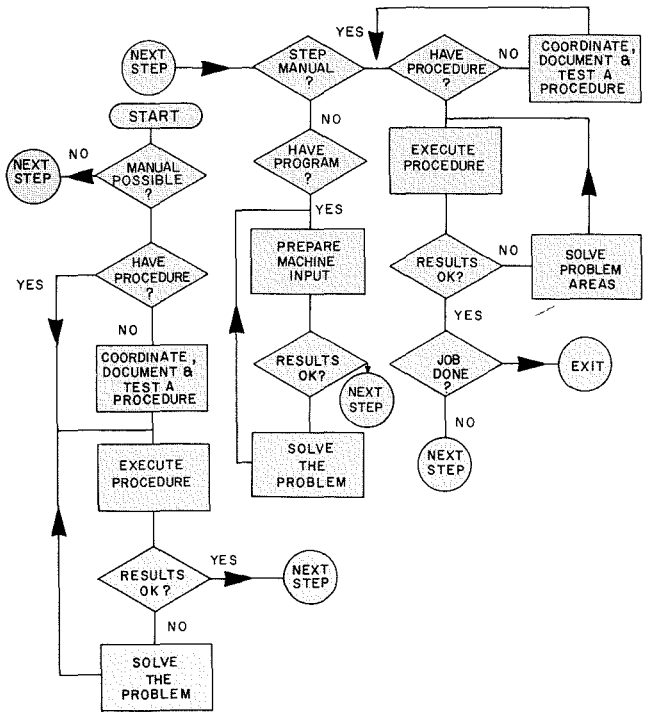

Fig. 1—A step in design processing.

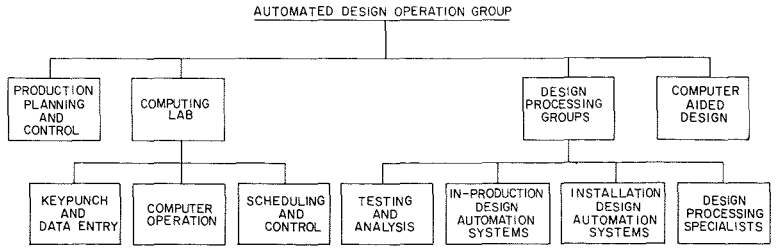

Fig. 2—Organization of the Automated Design Operation Group.

faults could be detected by examining the output points. The program is interactive, allowing the user to modify his tests and receive an immediate scoreboard showing the test's effectiveness, and is thus useful in designing functional tests, selecting output pins and test points, and evaluating and comparing tests.

Mr. Robert Singleton of CAD in PBG demonstrated the usefulness of the program to design engineers by a BTSS TESTSIM run in which the functional test for a shift register was evaluated. The program detected errors in the test input description and also exposed gates in which a fault would go undetected. The simplicity and effectiveness of this demonstration has increased utilization of computer aided design programs at PBG.

Computing laboratory

The computing lab is responsible for effective utilization of computing equipment and operating software and services all libraries and card, tape, or disc data files. It is the computing center for engineering design, and automated design systems development. On the production side, the main users are the design processing groups within Automated Design Operations. To service these users, job scheduling and quality control procedures within the lab ensure that valid output products are delivered on schedule. The lab differs slightly from most commercially operated computing laboratories; each shift of the RCA laboratory is covered by experts in the lab's primary application and by special skill 'source-to-keypunch' service.

Design processing

Design processing is rather difficult to define because teams are organized according to several factors to meet varying needs. They may group together:

—All processing utilizing production-tested software systems,
—Teams engaged in installation of new automated design software systems,
—Teams engaged in testing services for new designs, hardware or software, and in experimental services to engineering, or
—Specialists who can serve the other groups.

A description of the activities within each grouping defines this segment of Automated Design Operations.

Production group

If we are dealing with an operationally installed design automation software system, design processing is a simple operation of standard procedurized activities for any circuit board or wiring panel processed. Although design processing personnel use the software system, the real users are members of the design, test, or manufacturing engineering staffs. They are served through a production operation in which manpower, computing time, and in-house calendar time requirements are predictable. The production statistics, when combined with production planning data, serve as a constant refinement to capacity determination. A 'unit' input (*e.g.* a circuit board or wiring panel) to the group is assigned to an analyst who is responsible for monitoring the unit through the proper procedures and providing the 'exception processing'. Where the exceptions require interaction with the drafting department, the programming department, or the responsible engineer, the analyst makes the contacts to resolve the problem. An analyst may follow several production units undergoing engineering changes. New designs usually require his full-time attention even when they are not large, complex assemblies.

Fig. 3 is a process flow of Design Automation System 7 (DAS7), a typical Automated Design software system in production use at Palm Beach for approximately four years. The system services TTL circuits and Spectra 70 backplane packaging. Given the characteristics of the plug-ins and parameters describing the backplane, the system will document a design and produce wire schedules and auto-wire-wrap equipment data.

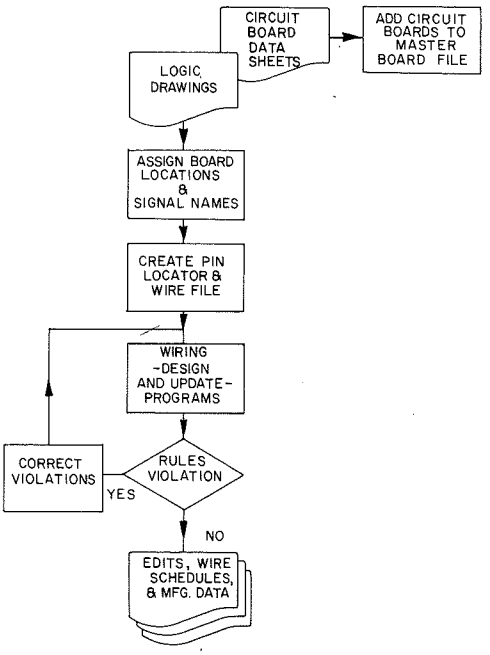

Fig. 3—The DAS7 wire generation system.

There is an interesting though primitive level of man-machine symbiosis in the DAS7 system. It occurs when wire generation is complete. The system does not observe cross-talk rules during the calculation of the wiring paths; after the routing is complete the total number of linear units of parallel wires between nets is computed, and violations are reported when this total exceeds a predetermined value. Each movement of wires by the design processing analyst to correct a violation may create new cross-talk problems which are subsequently uncovered by the system. The analyst and the system must work together to find an acceptable solution.

DA software installation

The Software Installation group is responsible for installing newly developed Automated Design software systems for the design automation system development team. When the system is installed design processing becomes a maze of new activity to determine

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if the system will perform without degradation of any of its parts. A comprehensive mass of 'live' data processed through each program of the system produces results that can be evaluated against product design specifications. As momentum increases during this system shakedown, design process analysts develop an operational capability for system usage and a sense of responsibility for system performance. Problem solving eventually settles at the lowest possible levels, *i.e.* analysts become increasingly capable of solving problems without the assistance of more highly-trained experts. New parts to the system and changes in response to requests or corrections are continually tested and placed into operation throughout the life of the system. The feedback loop that initiates these processes may continue throughout the service life of the product line the system supports.

Testing lab

Testing and analysis activities in design processing were conceived as support useful to: (1) the systems engineers whose decisions must accommodate conflicting demands of circuit and package engineers, and (2) the design automation software developers who must implement suitable algorithms once the packaging ground rules are firm.

Using prototype software, canned software packages, and home-made quick-reaction routines, the behavior of hardware designs subjected to automated partitioning, placement, and wiring can be studied. Performance testing of automatically produced numerical control data can be carried out in the manufacturing environment long before actual production usage of the automatically produced data is due. Anticipated problems in any design, hardware or software, can be tested under controlled conditions. Improvements or degradation in the design can be evaluated for selected trade-offs. A team of specialists in design processing uses automated design, graphic, and quick-reaction software packages for testing designs. One such effort in the Palm Beach design processing group was a wireability study of a T^3L circuit-board design. The software used was a combination of the PENTA3 Siemens Automated Design System, an RCA Maze Routing Program, and a quickly-coded vector-ordering routine. As a result of this particular study, the wireability of the plug-in was enhanced by rotating the integrated circuit packages 90°.

The testing and analysis activities at both Palm Beach and Marlboro have been intense during the early utilization of the newly installed DANPL automated design system. Many of the time consuming bugs in the processing mechanism must be identified through 'usage' of a new system. Practical solutions to the problems which are acceptable to the user may not always be easy to implement.

Such is the case with the wiring problem on the medium speed circuit boards. The DANPL system-generated wiring must often be rearranged in order to place the wires rejected by the routing system. A practical solution to this problem uses a simple interactive graphic system. Systems for solving this problem can evolve into entirely new levels of man-machine symbiosis in the next generation of automated design software. In the meantime, liveable solutions are analyzed, tested, and implemented using the conventional man-machine interaction and data entry techniques.

Function of the organization

The Automated Design Operations organization makes plans to support projected work loads, to process and validate a product's files, and to deliver the output data products (manufacturing data and engineering documentation) on schedule. The organization supports continuous maintenance of a product's files against engineering changes throughout the life of a product. Each group is responsible for specified activities in a distinct area. Groups support each other when production backlogs require relief. This internal coordination is readily achieved. Although the proficiencies vary, aptitudes and skills are basically the same in all the groups: data processing aptitudes, and design automation skills. Each activity, therefore, may function independently or play a role in an integrated group of activities to accomplish immediate objectives or projected plans.

Building the organization

Building the Automated Design Operations organization requires selecting and training key people to achieve the following capabilities:

—Production design-processing for each operational automated design system supporting current product lines,
—Software installation to place new automated design software systems into a production environment,
—A computing laboratory with a through-put sufficient to support design processing and other engineering computing requirements,
—Testing and analysis to effectively support engineering experimental work, and
—Computer aids via time-sharing terminals.

The key people and their working teams must possess skills to launch new activities: a new line of services and new concepts in design processing require people who can implement new services effectively. The steady workers who can handle these jobs smoothly over the long pull will eventually take over the services and software systems that settle into routine procedures; they keep existing activities alive while the key people forge ahead once more.

At both Palm Beach Gardens and Marlboro, the Automated Design Operations organizations have undergone a rapid build-up. At this writing, the transition between building the organization and putting it into operation is taking place. If the homework has been diligently prepared, the transition will be smooth and successful. The workload scheduled will indeed 'field test' the organizational structure.

Conclusion

To automate the process of deriving manufacturing data and engineering documentation from a logic sketch assumes a 'solution' to all the problems associated with the process. As long as computers can do no more than represent these solutions, the problem-solving talent of people must interact with whatever parts of the process are solved and programmed. Such is the role of our people in processing the designs for new products and engineering changes for old products. Involved and committed to our common goal—a quality-assured product in the customer's laboratory—our people process each design with this common goal as their driving force.

High-voltage laminated overlay power transistors

R. Amantea | H. Becke | P. Bothner | J. White

Power transistor design engineers have long sought to incorporate into their devices such features as individual emitter ballasting; double heat sinking, high thermal stress resistance, bonding areas with minimum parasitics, and effective area utilization to improve overall device performance and reliability at a reasonable cost. One device—the laminated overlay transistor—allows the simultaneous realization of all of these advantages. This paper presents device structures, characteristics, and performance for several types of laminated overlay transistors spanning a frequency range from audio to 200 MHz and a power range from 10 watts to 2.5 Kw.

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received the BSEE from the City College of New York in 1965 and an MS in electrophysics from the Polytechnic Institute of Brooklyn in 1969. He joined the RCA Laboratories in that year as a member of the research training program. His initial research was in the area of solid state high frequency devices, and in 1966 he joined the technical programs laboratory at Somerville. Since 1966 he has been working in the area of high-frequency, high-power devices. Among these devices are charge storage diodes, avalanche diodes, Schottky barrier diodes, high frequency laminated overlay transistors and high frequency power MOS transistors. His recent work is concerned with fundamental device studies such as ultra-linear operation for CATV, improvement of load pulling characteristics, and study of second breakdown phenomenon. Mr. Amantea has one patent and has co-authored several technical papers. He is a member of Eta Kappa Nu, Tau Beta Pi and the IEEE.

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From 1953 to 1959 Mr. Becke was associated with Sueddeutsche Telefon-Kabel-und Drahtwerke, A. Gr., Nuremberg, Germany where he developed telecommunication equipment, mainly filters and transistorized negative resistance repeaters. He worked in HF transistor design at Tung-Sol Electric, Inc. from 1959 to 1961 and he joined Advanced Development Group of RCA Semiconductor Division in May 1961. There he engaged in the development of gallium arsenide technology and devices. In his capacity as Engineering Group Leader, Mr. Becke is currently responsible for the development of high power, high frequency transistors, gate turn-off SCR's and power integrated circuits. He is co-author of numerous papers dealing with semiconductor devices and technology and he holds several patents in this field.

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Authors Bothner, White, Amantea, and Becke (left to right).

NORMALLY, A HIGH-POWER TRANSISTOR means a high-current device. But for power levels above the order of 100 W, increasing pellet size to cope with increasing current demands does not aid thermal dissipation. Packaging techniques already limit thermal resistance, and increased area necessitates more uniform processing over larger wafers, thereby decreasing pellet yield. Thus, fewer devices per wafer and lower yield drastically push up the cost per watt.

Such considerations have led to the investigation of high-voltage high-power transistors. However, high voltage gives rise to such difficulties as forward and reverse second-breakdown, surface effects, and heat removal problems. The advantages of small pellets and high impedances that accompany high voltage are offset by disadvantages such as second-breakdown and unstable collector current leakage.

Techniques established in the course of development of the laminated-overlay transistor deal effectively with these disadvantages. Individual emitter site ballasting gives uniform current distribution and prevents hot spots. Moreover, this ballasting provides forward second-breakdown protection up to 16 A at 150 V and has permitted collector-to-emitter sustaining voltages as high as 700 V at 0.2 A.

Passivation and glass sealing applied to the laminated-overlay transistor

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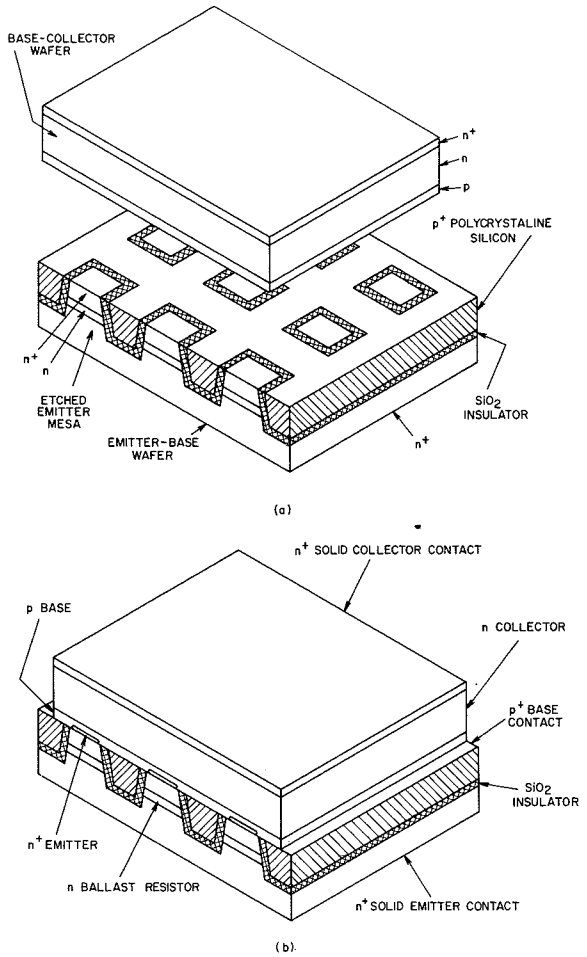


Fig. 1—Device construction (a) before lamination and (b) after lamination.

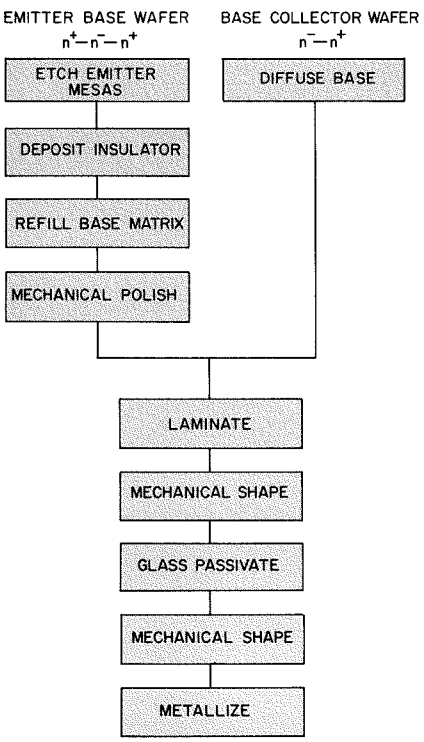


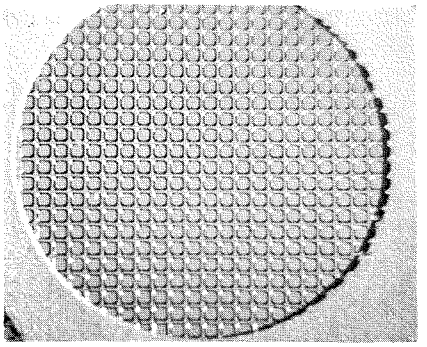
Fig. 2—Basic laminated overlay process.

minimize the effects of surface leakage. The glass sealing also allows novel packaging techniques which provide true double heat-sinking and simplify paralleling of pellets. Thermal resistance has been reduced to 0.14°C/W. No device process incorporates the above features as simply and efficiently as the laminated overlay process.

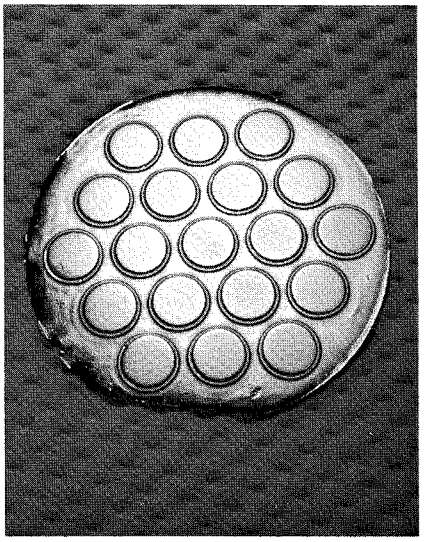
Technology and device construction

The laminated overlay device is formed from two component sections: the emitter-base wafer and the base-collector wafer. These wafers are shown in detail in Fig. 1a. All of the developmental effort has been on n-p-n transistors; therefore the processing is described for an n-p-n structure. The base-collector wafer is fabricated by conventional techniques but the emitter-base wafer fabrication utilizes new processes.

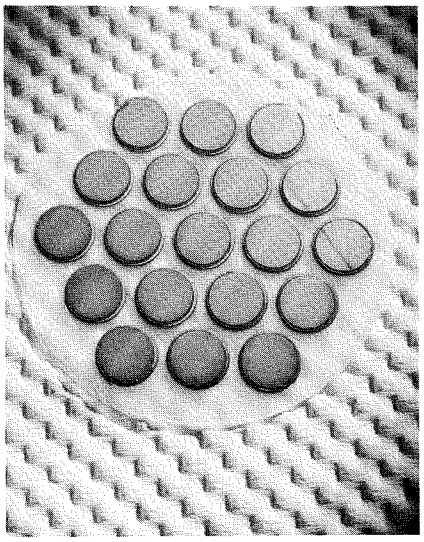
The basic laminated-overlay process flow is shown in Fig. 2. In addition to



(a) Preferentially etched emitter mesas (single unit)

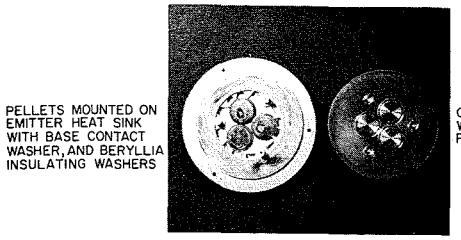


(b) Laminated wafer after mechanical cutting to define individual devices (19) and each peripheral base contact



(c) Glass-passivated wafer after mechanical processing to define base contact and expose emitter (bottom) and collector (top) contact areas.

Fig. 3—Device processing.



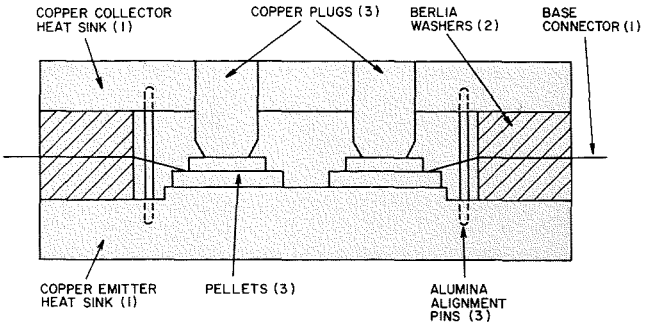


Fig. 4—Parallel packaging.

standard process techniques, such as epitaxy, diffusion, deposition of insulators, and metallization, five processes are used which are not normally encountered in conventional power transistor manufacturing. These are: preferential etching, epitaxial polycrystal refilling, lamination, mechanical shaping, and glass pressing.

Individual emitters are preferentially etched into an epitaxial silicon wafer, with the layer providing individual emitter ballast resistors. An insulator (SiO_2 and Si_3N_4) is deposited over this structure, sealing off the n-type regions. The remaining volume is refilled by polycrystal epitaxial silicon doped heavily with boron. The wafer is then mechanically polished back to reveal the n^+/p^+ matrix, as shown by the bottom wafer of Fig. 1a. The bottom surface (n^+) becomes the solid emitter contact, the isolated squares (n^+) form the emitter contact to the base layer, and the refill matrix (p^+) forms a base contact surrounding the insulated emitters.

The two component wafers are placed face-to-face in a hydraulic press and are fused into a monolithic semiconductor structure. This lamination is done in vacuum under heat and pressure. At elevated temperatures, two important diffusions take place. A donor diffusion front advances from the n^+-type emitter columns into the p-type base region, the boundary of which is the emitter-base junction. This advance locates the metallurgical emitter-base junction away from the highly dislocated and distorted laminated interface.

Simultaneously, an acceptor diffusion front advances from the highly doped p^+-matrix into the base layer, forming a low-resistivity base contact adjacent to the emitter-base junction. This greatly reduces the base spreading resistance. Thus, in a single operation an intricate overlay transistor structure is formed in the center plane of the semiconductor laminate. This complete structure is shown in Fig. 1b. Wafers at various stages of processing are shown in Fig. 3. Fig. 3a shows the etched emitter pattern of a single unit.

Following lamination, the wafer is mechanically processed to expose the individual pellets and their base contact ledges as shown in Fig. 3b. The exposed collector-base junction is passivated by a suitable deposition of an insulating material and the wafer is hermetically sealed in glass. Finally, the wafer is mechanically processed to expose the emitter, base, and collector contact areas, as shown in Fig. 3c, and the individual pellets are separated and metallized to form the finished transistor.

Several of the unique processes developed for this device have been applied in other areas including power integrated circuits, high-voltage rectifier stacks, and power MOS transistors. Passivation and glassing techniques as developed for these transistors are being used on rectifiers and avalanche diodes.

Unfortunately, laminated overlay technology deviates drastically from conventional semiconductor manufacture in several processing steps (e.g. high temperature lamination and mechanical shaping). New equipment and machine design would be required to mass produce the transistor. However, many of the operator-oriented processes such as photoresist, which are expensive in conventional technology are replaced in the laminated overlay process by mechanical processes with rather loose tolerances that are compatible with mass production.

Packaging

Because the device pellets are hermetically sealed in glass with the active region imbedded in the center portion of the pellet, a simple, inexpensive package can provide both mechanical support and an additional thermal path through the top of the pellet for more efficient heat removal. The basic package is composed of emitter and collector copper heat sinks, beryllia insulating washers to provide electrical isolation with low thermal resistance, and a thin phosphor-bronze washer for base contacting. Three pellets are paralleled as shown in Fig. 4. In this package, alumina alignment pins locate the collector heat sink and copper plugs make actual contact with each pellet, thus permitting nonuniformities in pellet thickness. The vertical dimensions of the copper, beryllia, and silicon are designed to cancel vertical stresses during temperature cycling. Pellets are soldered directly to the copper heat sinks with a high lead-content alloy which provides longitudinal stress relief during thermal cycling.

When pellets are paralleled it is advantageous to have them as close together as possible to provide good thermal coupling (the pellets are actually touching in this package configuration). This arrangement will increase the thermal resistance slightly more than the configuration where the pellets are far apart because of the overlapping heat spreading in the copper. With the pellets in close proximity, the thermal resistance is approximately that of a single large-area pellet. Reduced packaging costs and close matching of characteristics for paralleling are possible because each hermetic, metalized pellet can be extensively tested prior to mounting. Hermetic pellets are also very desirable for low-cost plastic encapsulation and for hybrid circuit applications.

Design and applications

The laminated-overlay process has been adapted to suit three basic design ranges: high-power audio frequency, high-power medium frequency (30 MHz), and medium-power high frequency (200 MHz). The geometrical design parameters are shown in Table I.

The 30-MHz device was the first power transistor developed using this technology. Improvements in processing techniques of the emitter-base wafer resulted in an enormous increase in area utilization for the audio laminated-overlay transistor as the ratio of emitter area to collector area shows. A pellet the same size as the 30 MHz unit (.25 in. diameter) provides more emitter area and emitter periphery. Consequently, current capabilities are much greater for the audio device.

The 200-MHz laminated-overlay transistor was geometrically scaled from the 30-MHz design to extend the frequency performance while keeping the frequency-power product (FPP) constant. Smaller emitters minimized the effects of emitter-current crowding, and the base width was reduced to 0.7 μm to increase the beta cutoff frequency. Special lamination techniques requiring fine control of temperature and pressure effectively controlled the base width.

The laminated overlay process utilizes pellet area two- to four-times as effectively as conventional processes. The degree of emitter subdivision can be chosen to yield the proper balance of emitter area and periphery to optimize the device characteristics for particular operating conditions: on low-voltage, low-frequency devices, larger emitters increase area utilization, while on high-voltage, high-frequency devices, smaller emitters provide more emitter periphery and better second breakdown protection.

Table II—Performance data.

Parameter	Symbol	High frequency devices 30 MHz	200 MHz	Audio devices Single	Triple
Collector-emitter voltage (V)	V_{CEO}	300	150	650	650
Static forward current transfer ratio	h_{FE}	15 @ 8A	20 @ 1A	20 @ 10A	20 @ 20A
Maximum current (A)	I_{max}	10	1.5	14	32
Collector-Emitter Voltage B=10 (V)	$V_{CE(sat)}$	10 @ 6A	10 @ 1A	8 @ 5A	6 @ 10A
Collector-cutoff current (Base open) (mA)	I_{CBO}	1.0 @ 200V	1.0 @ 100V	1.0 @ 200V	5.0 @ 200V
Gain bandwidth product (mHz)	f_T	50	300	30	12
Max power dissipation T_c=25°C (W)		500	100	600	1,250
Second breakdown collector current (50 ms)	$I_{S/B}$	—	—	4	10
Power out (W)		120 @ 30 mHz	15 @ 200 mMz	1,000[1]	2,500[1]
Power gain (db)		10	6	—	
Efficiency (%)		39	35	67[2]	67[2]

[1] Calculated power out—$V_{pp}I_{pp}/8$
[2] 67% efficiency assumed for class B amplifier.

By modifying the emitter etch pattern internal structure can be changed without changing the external structure of the pellet. Device characteristics can be closely tailored within a single product family.

Second breakdown

Second-breakdown, a direct result of hot-spot formation and current crowding, occurs in either the forward-or reverse-bias modes of operation. A bias applied to the base-emitter junction produces a lateral potential gradient under the emitter, as shown in Fig. 5. In the forward bias state, this potential gradient makes the emitter periphery more forward biased than its central portion, and therefore causes a high current injection density (current crowding) along the emitter perimeter. Localized hot spots develop within the high-resistivity collector depletion region because of the high power density (J_cV_c) in this small volume (see Fig. 4) If severe enough, these hot spots start a thermal regenerative process which can result in a local collapse of the depletion region and the ultimate destruction of the transistor. The severity of the hot spots is inversely proportional to the rate of lateral diffusion of the injected emitter current within the base of the transistor. Any condition which increases the magnitude of the injected current, decreases the effective base width, or shortens the minority carrier travel time through the base causes a proportionate decrease in forward bias ($I_{s/b}$) second-breakdown capability. In other words, an increasing base-emitter bias, base drift field, collector-base reverse bias, or gain-bandwidth-product (f_T) decreases a transistor's $I_{s/b}$ capability.

The second breakdown capability of a transistor is usually extended by optimizing heat removal with various packaging techniques, incorporating some form of ballasting (usually emitter ballasting, which spreads the current distribution uniformly along the emitter periphery), and maximizing the emitter periphery to keep current crowding at a minimum. The laminated-overlay transistor uses double-sided copper heat sinking, emitter ballasting, and multiple emitters

Table I—Geometrical and structural data

Design Range	*Emitter area* (mil²)	*Collector area* (mil²)	*Emitter periphery* (in)	*Number of emitters*	*Size of emitter* (mil)	*Base width* W_B (μm)	*Ratio of emitter area to collector area*	*Collector thickness (mils)*	*Region resistivity (ohm−cm)*
High power 30 MHz	8600	46700	4.9	222	7	3	0.184	1.2	10
Medium power 200 MHz	870	6000	0.778	55	4.5	0.7	0.145	.8	10
High power Audio laminated overlay transistor	15400	31400	6.85	190	9	7	0.49	4.0	40

which maximize emitter periphery and insure good thermal mapping over the entire pellet.

Although laminated overlay transistors are used primarily in high-power linear amplifiers and modulators, possible applications include high-current switching amplifiers and inverters where highly reactive loads are encountered. Because normal operation for circuits of this type requires repeated application of reverse-bias to the base-emitter junction, reverse-bias second breakdown ($E_{s/b}$) is an important consideration.

The $E_{s/b}$ has basically the same failure mechanism as $I_{s/b}$: the collector depletion region collapses when current-crowding causes hot-spots and subsequent thermal run-away. But the polarity of the lateral potential gradient in the reverse-bias mode is reversed, causing the central portion of the emitter to be more forward-biased than the perimeter. This condition constricts the current to an even smaller area than in the forward bias case, making current densities orders of magnitude larger. The energy level at which breakdown occurs is substantially lower. But since conduction after application of a reverse bias is usually of very short duration (on the order of a few microseconds), $E_{s/b}$ does not necessarily cause breakdown.

The probability of $E_{s/b}$ occurring increases as the magnitude of the injected emitter current or the reverse bias of the emitter or collector base junctions increases. And $E_{s/b}$ is also a function of the recombination rate of stored charge in the base: as the recombination rate increases, $E_{s/b}$ capability increases. The methods employed to increase the $I_{s/b}$ capability can also be used to increase $E_{s/b}$. Multiple emitter sites in the laminated-overlay transistor design further enhances its $E_{s/b}$ capability.

Device performance

Typical performance data for the three types of laminated overlay transistors are shown in Table II. The RF data for the high-frequency devices were measured using a class B continuous-wave amplifier. The maximum capabilities of the 30-MHz design showed an FPP of 5.7 GHz-W, and the maximum capability of the 200-MHz design showed an FPP of 4.6 GHz-W. The fall-off characteristic for the FPP of the laminated overlay transistor reveals that devices designed to operate beyond several hundred MHz are impractical. This limitation is dictated by the minimum emitter size (~.001 in) and base width (0.3 μm).

Two types of audio devices were evaluated. The first device has an individually packaged 0.250-inch diameter pellet. The second device is composed of three of these pellets mounted together in a single paralleled package (Fig. 5). Typical thermal resistances for the triple unit and single unit were 0.14°C/W and 0.29°C/W respectively, giving the triple device about twice the dissipation capability (1,250 W). These two devices were developed as a driver-output pair for use in sonar amplifiers. The calculated output power for the pair in a class B amplifier is approximately 2.5 kW. The devices have typical beta cutoff frequencies of 30 MHz for the single pellet and 12 MHz for the triple pellet, and could be used effectively for RF applications with slight modification towards narrower base width and lower voltage capability.

A graph of h_{FE} as a function of collector current, shown in Fig. 6, demonstrates the effectiveness of paralleling with the ballasted pellets. The dotted graph depicts an ideal paralleling by multiplying the current capability of a single unit by three. The peak current capability is not impaired by the parallel mounting, although the h_{FE} falls off at a more rapid rate.

Paralleling conventional devices has not substantially improved forward second-breakdown of power transistors, but paralleling laminated-overlay transistors has caused substantial improvement. Individual emitter site ballasting of the devices counteracts the regenerative mechanism responsible for forward second-breakdown. The $I_{s/b}$ capability of a single audio laminated-overlay transistor is typically 4 A at 150 V (50 ms pulse), but when three of these devices are paralleled in a triple package, forward second breakdown typically increases to 10 A at 150 V; a value in excess of 16 A at 150 V was measured on one device. This improvement is attributed to effective emitter ballasting and close thermal coupling between pellets.

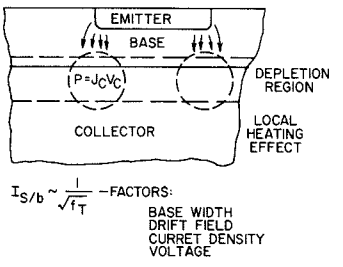


Fig. 5—Forward-bias second breakdown.

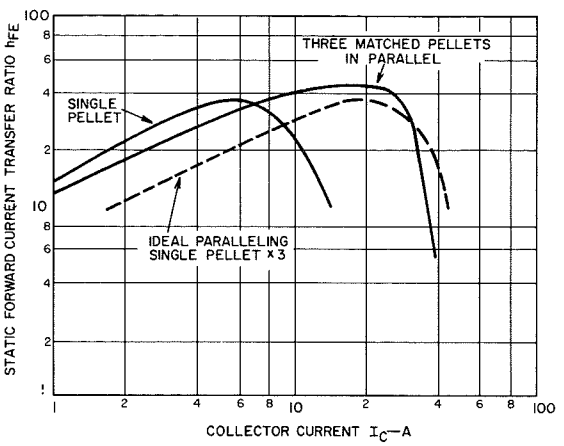


Fig. 6—Effectiveness of paralleling with ballasted pellets.

The ease of parallel packaging and the attainment of true parallel operation without significant characteristic degradation demonstrates that laminated-overlay transistor pellet structures could be the basis of a family of high power devices. Furthermore, the fact that these devices can be operated in the RF range shows that this family has a wide range of applications.

Acknowledgments

The authors thank Dr. A. Blicher, Manager, Power Technology for his advice and guidance on this project. The contributions in packaging techniques and tooling for many phases of the process by Mr. P. Del Priore are greatly appreciated. Further, the authors thank Messrs. D. Koch, D. Bergman, Mrs. A. Marshall, Mrs. D. Jacukowicz and Mrs. J. Ward and Arthur Ott for their help in fabricating and testing devices.

Trends in reliability engineering

V. Lukach

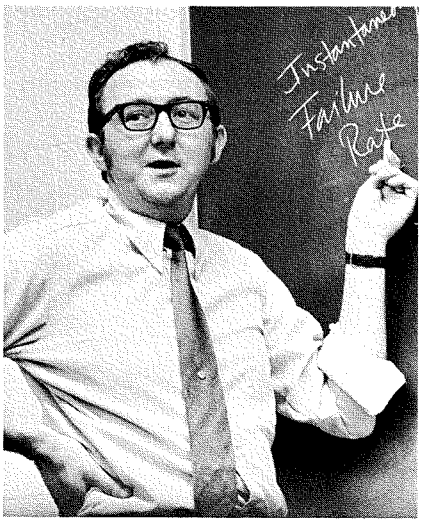
The solid state industry is demanding greater reliability in virtually all product areas. To meet this demand, reliability engineers are placing new emphasis on a variety of techniques. This paper describes these techniques and indicates probable areas of future emphasis.

WHAT IS HAPPENING in reliability engineering? Reliability engineers in development engineering at the RCA Solid State Division are currently emphasizing areas closely tied with the changing market demands. The reliability engineer must emphasize accelerated testing as never before, must pay strict attention to potential pitfalls in design cost reduction, and must react to customers who are becoming more and more reliability conscious. He must initiate new approaches in evaluations of more complex devices, must help develop new ways of quantifying reliability (*e.g.*, thermal cycling rating charts on power transistors), and must prove out and utilize newer techniques in reliability improvement, specifically, overstress burn-in.

Emphasis on accelerated testing

More diversified and faster response

Accelerated testing techniques are widely used in the laboratory and in product evaluation centers to detect failure mechanisms and predict product life. Perhaps, because these techniques are such powerful tools, their use has extended to related quality and reliability areas. There is practically no mechanical, environmental, life, or combined stress test where accelerated testing techniques cannot be beneficially applied. Although accelerated testing was initially used in life testing only, the concept is now being fruitfully applied in all phases of reliability testing. Table I lists various tests with recommended direction for acceleration.



But the creative engineer does not limit himself to only these tests. Consider for example, the problem of conducting humidity studies on certain package materials or platings where resistance to electrolytic migration between external lead members is the area of concern. In typical standard tests, the device spends hundreds or even thousands of hours in a humidity chamber with bias applied. An accelerated technique was devised: a few volts bias was applied across adjacent leads and a water droplet placed between these leads along the body of the device. Evidence of migration could be observed under a microscope in a matter of minutes. Significant differences observed among various experimental test groups were later confirmed by long-term traditional humidity tests.

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received his BS in industrial engineering from Penn State University in 1957 and an MS from Rutgers University in Applied Statistics in 1964. He has taught courses in statistics and quality control and presented papers at various conferences such as the American Society for Quality Control (ASQC). Prior to joining RCA, Mr. Lukach worked for the Western Electric Company for six years. He was instrumental in developing and installing a system of controls and experimental procedures on a high volume diffused silicon mesa transistor line that has been as high as 70% of the plant's dollar volume. Mr. Lukach joined RCA in 1963 in the Test and Reliability Department. His initial efforts were in the device reliability field and government contracts on reliability improvement. He was made Project Leader of the Reliability and Quality Assurance Group in January 1966, where he continued efforts in reliability evaluations of newly-developed transistors. He was promoted to Manager of the Quality and Reliability Engineering Department in 1968. In this capacity he is responsible for reliability evaluations of all developmental products in the Solid State Division, including power transistors, integrated circuits, optical products, thyristors, HF transistors, power modules, and microwave integrated circuits.

*Since this paper was written, Mr. Lukach was appointed Quality and Reliability Assurance Manager for the Mountaintop Plant.

Real-time indicators

When accelerated testing was initially used in evaluation studies, the reliability engineer tended to keep his testing concepts separate from the factory production floor. But in production, certain failure mechanisms can not be completely eliminated; the reliability of the device depends on controlling the effects of these mechanisms. To do this, accelerated tests are used in a routine manner on the factory production floor. The response time of these tests is so fast they have been called "real time indicators."

For example, the RCA Mountaintop plant (Mountaintop, Pa.) has been equipped with 12 accelerated thermal fatigue racks to test each lot of the plastic power TO-66 package (Versawatt) transistor types for contact degradation. The test is conducted under an overstress delta case-temperature range of 120°C and helps control a production family of over one million net devices per month. Fig. 1 shows the acceleration in terms of time and temperature range in comparison with the standard test, while Fig. 2 shows the acceleration in terms of results.

Reliability assurance tests

The vendor often finds himself in a dilemma. On one hand, he wants to use Group B tests, which are routine reliability tests, to trigger detrimental process changes. Test conditions are made moderately severe, at or above maximum ratings. On the other hand, customers frequently request reliability data; it could be embarrassing and misleading to explain anything other than zero failures. The question is how to separate the two with one set of tests.

Although the trend has not gathered momentum, separation is destined to occur. Accelerated tests will be uti-

lized more as an extra safeguard on product integrity in the Group B portion of the specification.

External publication of reliability data will follow two approaches. In the first approach, the vendor uses the accelerated test results, applies meaningful acceleration factors, and inform the customer. Qualitative explanations accompany each report. In the second approach the vendor establishes closer feedback loops with the user to gather and interpret pertinent reliability data from the customer. The customer will play a larger role and use mathematical failure rate models based on product design and product history. As vendors and users demand extremely low device failure-rates, these approaches will be accepted as more logical than those presently used.

One word of caution on using accelerated testing techniques: failure analysis and data analysis should verify that a true acceleration exists, and that failures which have no bearing on practical applications have not been created. In other words, no new failure mechanisms should be induced.

Design cost reductions

Cost reduction pressures are everywhere and are generated both internally and externally. The reliability engineer should not react negatively to change; that would be too easy and would do a disservice to his company. However, the engineer must be alert to the possibility that changes may have detrimental effects on product reliability. It is erroneous to assume that all design and process changes reduce design margins, but some changes require a recognition, study, and control of specific classes of problems. Many changes actually improve reliability while reducing costs. The reliability engineer must take multi-lot samples to minimize the possibility of prejudice before he approves proposed changes.

As an example, consider wire bonds in a dual-in-line plastic (DIP) integrated circuit package. Differences in the thermal coefficients-of-expansion of various materials within the plastic unit result in stresses against the bond during temperature cycling. RCA's DIP product has been the target of continuous experimentation to improve this capability; as a result, substantial gains have been made.

Table I—Acceleration Directions

Tests (1)	*Direction of stress acceleration*
Mechanical	
Lead fatigue	Increase bends to package destruction
Lead pull	Increase weight to package destruction
Lead torque	Increase torque to package destruction
Centrifuge	Increase G-force
Impact shock	Increase G-force
Vibration	Equipment limited
Solderability	Increase preconditioning stress, *e.g.*, 3 hrs. in steam
Environmental	
Moisture resistance/relative humidity	Increase time; use pressure cooker/autoclave; use moisture with bias
Salt atmosphere	Increase time
Temperature cycling	Increase cycles; increase $\Delta T_{Ambient}$
Thermal shock	Increase cycles; increase ΔT_{Liquid}
Life Tests	
Operating life	Increase $T_{junction}$; increase time
Storage life	Increase T_j; increase time
Thermal fatigue	Increase ΔT_{case}; increase cycles
Reverse bias	Increase $T_{Ambient}$; increase voltage; increase time

(1) MIL-S-750B (Transistors) and MIL-S-883 (IC's) define test procedure for most of these tests.

However, the reliability engineer must recognize the effect of processing variations and consequently place additional emphasis on lot control and in-process control. With DIP's the original control consisted of a rigorous and time-consuming cycling program. One problem that prevented quick feedback necessary for routine control was the length of the test: approximately two weeks. To reduce this testing time, liquid thermal shock was used daily on samples right from the molding press (thermal shock is more severe than temperature cycling). As a result, the time per cycle has been reduced from one hour to one minute; the resulting feedback and corrective action are more efficient.

Wearout mechanisms

If DIP's are placed in a high-humidity high-temperature chamber for thousands of hours, the aluminum metallization on the chip corrodes. If a power transistor is thermally cycled over a fairly wide temperature range by turning the power on and off, contacts open after tens or hundreds of thousands of cycles. But what does it mean? It may mean that reliability testers have become so skilled at their trade that any device can be made to fail (in fact there is no semiconductor that can withstand one mighty blow from a sledge hammer). But in certain key areas, the reliability engineer must (1) establish where the wearout phase is, (2) determine the relationship between accelerated conditions and typical use conditions, and (3) estimate the possibility, however remote, of wearout within the system life.

Greater customer reliability awareness

The reliability input is an increasingly important aspect in all phases of user/vendor contacts. There are many reasons for this tendency.

Tougher specifications

Many commercial and consumer specifications have conformance requirements far in excess of the military. It is ironic that in many cases the "com-

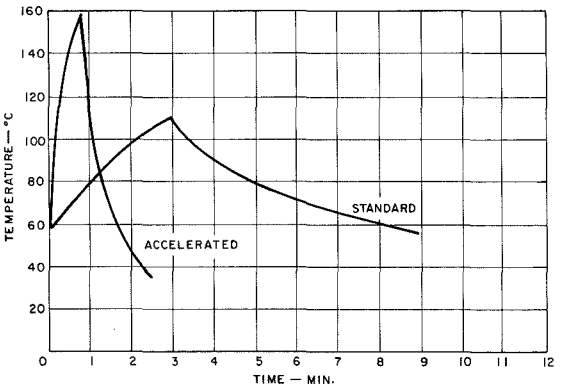

Fig. 1—Accelerated thermal fatigue test—Versawatt power transistor.

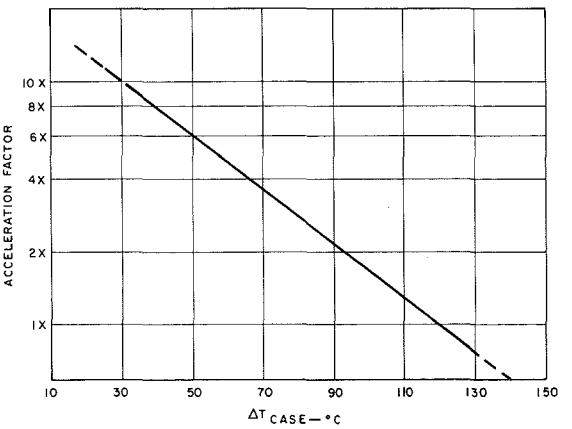

Fig. 2—Thermal fatigue acceleration factors —Versawatt power transistor referenced to $\Delta T_c = 120°C$.

mercial" device has tighter reliability specifications than the high-reliability, or so-called, "hi-rel" devices. For example, one customer wanted to impose a rigorous temperature cycling test on samples of hundreds units for hundreds of cycles with no failures permitted. This specification was not accepted for practical reasons. The test was extremely severe and, the statistics of the sampling plan made it one of the most stringent requirements of its kind. For comparison, Fig. 3 shows the operating characteristic (OC) curves for commercial RCA devices, C; hi-rel devices, (A); and devices meeting the customer's standard, (B). If a lot submitted for sample testing is 1.5 percent defective, the standard RCA plans show a very high probability of acceptance: 0.97 and 0.89, commercial and hi-rel products, respectively. Curve B, the OC curve for the customer's specification, depicts a very low probability of acceptance of 0.05. This example is almost a case of guaranteed acceptance versus guaranteed rejection.

There are other examples. Bell Telephone Laboratories and Western Electric impose minimum 250°C junction temperature burn-in and life requirements on many of their incoming purchased components. Central Engineering at RCA Camden imposed a 2000-hour, high-humidity, temperature-cycling, power-switching test on all dual-in-line plastic component contenders.

Failure rate information

The equipment designer is under pressure to project reliability performance of sometimes very complex systems. Failure-rate estimates of component parts are the inputs for his mathematical model. Derating estimates (temperature, voltage, power) are attached to failure rate estimates, adding to the total error variance. The customer sometimes transfers his problem to the reliability engineer of the vendor who must understand the customer's problem and provide responsible professional help.

But customers are requesting less actual reliability failure-rate data on parts; their systems have vastly more data. Mathematical failure-rate models, using everything but actual test data on the device in question, are becoming more common. The vendor is still asked for data, but inquiries tend to be verification-type and of a less consequential nature; the user will generate the part failure-rate estimate himself. The user should still, however, depend on the vendor for consultation, analysis, and corrective action, which may be either design- or circuit-oriented.

Mixed reliability objectives

Getting accurate and complete information from a series of reliability tests is an accomplishment in itself, but it is only the initial portion of the reliability engineer's job. He must provide an independent and objective appraisal of the reliability characteristics of the device under study, for which he needs some yardsticks. He sometimes finds he has mixed reliability objectives, dictated by diverse standards:

Internal specifications. Traditional conformance criteria are usually included here for mechanical, environmental, and life-test stresses.
Customer application. The engineer must ascertain the mechanical, environmental, and electrical requirements of the device which may be used in more than one application.
Customer specification. The customer has his own qualification and lot-control reliability tests to consider.
Competitors' capability. Many times it is a buyers' market and a potential buyer considers a vendor whose device has the greatest overstress capability.

It takes a well-seasoned, mature reliability engineer to weigh all these reliability objectives, to formulate an opinion, and to instigate improvement proposals when the situation demands it. Mixed reliability objectives are becoming more common in several key stress areas, and tests conducted just to meet internal specifications are becoming less meaningful. Competitors' evaluations are also growing more common.

Warranties and safety hazards

There has been increasing activity in the area of warranties and safety hazards. Vendors are being asked to share replacement costs for consumer equipment that suffers field problems, and litigation based on inferior quality claims is becoming more commonplace. Moreover, devices must be evaluated to assure virtual safety-hazard-free components. The reliability engineer can do a tremendous service to his company by being constantly alert and searching and pinpointing potential problems. Reliability evaluations of developmental products will include, in addition to mechanical, environmental, and life tests, tests of increasing severity assessing product safety with respect to flammability, explosion, toxicity, radiation, and high-voltage isolation on selected product designs. In addition customers using RCA products must be made aware that safety-conscious equipment design is mandatory at RCA.

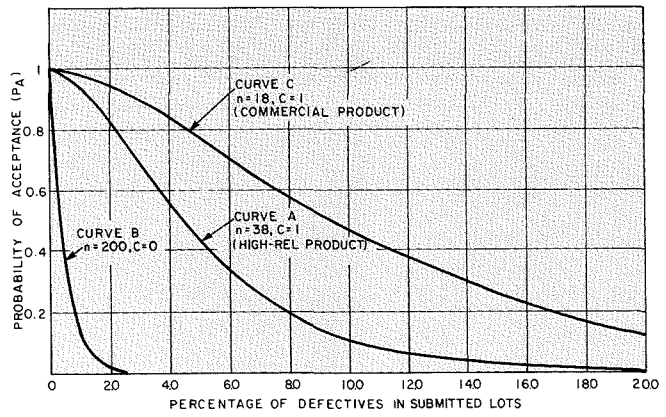

Fig. 3—Operating characteristic curves.

More complex devices

Increasingly sophisticated device design (such as MSI/LSI, power modules and MIC's) offers new challenges to the reliability engineer. He must develop logical techniques to cope with the evaluation and assurance problems.

New approaches

An initial reliability evaluation of a discrete device or bipolar integrated circuit typically requires 300 pieces to be subdivided into 15 groups for reliability tests. But such an approach is impractical for many products, such

Table II—Reliability program, MIC IF-amplifier.

Sample Construction	Test	Conditions	Down Period Parameters	Sample
A. Substrates only; 12 lead TO-5 package; resistor check configuration	1. Temperature cycling	−65°C to +150°C; read at	Resistors	10
	2. Storage life	0, 5, 20, 100, 200 cycles		
	3. Mechanical	200°C; read at 0, 50, 200,	Resistors	10
	(a) Impact shock	500, 1000 hours		
	(b) Vibration Variable Frequency	750A/2016.1, 500G	Resistors	5
	(c) Vibration fatigue	750A/2056		
	(d) Centrifuge	750A/2046		
	Step stress storage	750A, 20,000g		
		150°C start; 25°C/24 hr. intervals	Resistors	10
B. Substrates only; 12 lead TO-5 package; capacitor check configuration	1. Same as A.1-A.4	1. Same as A.1-A.4	Capacitors	10
	2.	2.		10
	3.	3.		5
	4.	4.		10
C. Substrates with good transistor chips; 12 lead TO-5 package; transistor contacts check configuration	1. Same as A.1-A.4	1. Same as A.1-A.4	V_{EBF} and V_{CBF}	10
	2.	2.		10
	3.	3.		5
	4.	4.		10
D. Completed MIC	1. Same as A.1-A.4	1. Same as A.1-A.4		10
	2.	2.	Functional parameters	10
	3.	3.	Functional parameters	5
	4.	4.	Functional parameters	5
	5. Operational test	5. (see life test circuit)	Functional parameters	10
	6. Accelerated Operational test	6. To be defined	Functional parameters	10
E. Standard 4-lead package; MOS capacitors mounted on top of leads and wire bonded to header surface	1. Same as A.1-A.4	1. Same as A.1-A.4	Capacitors	10
	2.	2.		10
	3.	3.		5
	4.	4.		10

as developmental microwave integrated circuits (MIC's). There are three problems: lack of devices (approximately 20 are produced per month), expense ($600 per unit), and the absence of sensitive problem-detection parameters on down-period tests. By measuring only noise figure and gain, degradation can go undetected until it causes catastrophic damage. Consequently a new approach has been developed and successfully used. This method relies on subcomponent evaluation of individual packages: resistors, capacitors, transistors, plus the complete MIC's, used in conjunction with a symmetrical design-of-experiment matrix (Table II). Subassembly and shrinkage parts are economically used to achieve the evaluation objectives. To generalize, complex devices mean:

- Traditional reliability assessment and quality assurance practices built around volume parts are of little value.
- Statistical qualification and lot acceptance testing of complete production items will decrease in importance.
- Reliability tests will concentrate on specially designed test elements. Screening will remain important.
- Reliability assurance practices will emphasize controls.
- Customer and field date will be better utilized.

New failure modes and mechanisms

New technologies bring new failure modes and mechanisms to detect and control. Large-scale integration (LSI) circuits containing multi-level metalization must be tested for a wide variety of open circuits at steps and feed-throughs, intra/inter level shorts, and high resistance metal. New packages bring hermeticity and mechanical strength considerations. Smaller geometries bring possible ion migration and corrosion problems, electromigration, shorting, and leaking.

More manpower per unit of data can be spent on down-period testing, stress testing, data analysis, and failure analysis. Performing a thorough failure analysis on a power module is an order of magnitude more complex and time-consuming than the same analysis of a discrete device.

Sophisticated Equipment

Such sophisticated analytical equipment as scanning electron microscopes (SEM's) and infrared scanners has become commonplace in reliability testing labs because it is necessary to perform analytical and failure-analysis functions. Voltage contrast studies on the SEM will undoubtedly be perfected and used on memory failure analysis to take advantage of the side-by-side redundancy of the memory matrix that will pinpoint failure cells and areas.

Thermal cycling rating charts on power transistors

Thermal fatigue occurs in silicon power transistors. Repeated temperature cyling caused by changes in power dissipation or ambient temperature differences results in fatigue failure of the interface between the silicon pellet and the mounting surface. Quantitative characterization of this phenomena allows the equipment designer to predict and maximize practical field reliability.

The reliability engineer works intimately with development engineers to design experiments to yield needed information, conduct tests under rigorously-controlled conditions, analyze results, and project end results on a quantitative thermal-cycling rating chart to aid the circuit designer. This rating chart projects an estimated safe-area response (in terms of cycles to failure) from such inputs as change in case temperature (ΔT_c) and power dissipation (P_D); see Fig. 4.

In a single thermal-cycling test, the variables include change in case temperature, (ΔT_c); maximum junction temperature, ($T_{j(max)}$); power dissipation, (P_D); heat-sink size and cycle time. Some of these variables are independent and some dependent: with the physical test rack setup held constant, changing P_D increases T_c and $T_{j(max)}$. The test design matrix becomes a modified factorial design.

The interdependency of some of the variables dictates a complex preliminary set of experiments before a single thermal fatigue test can be run. This procedure is called "scaling the environment". When the bounds of the above-mentioned five "variables" are set, this procedure on one transistor study consists of determining 150

Table III—Scaling the environment: tests for thermal fatigue ratings

Power (W)	ΔT_c (°C)	$T_{j\ Max}$ (°C)	*Heat Sink #*	*On/off time (s)*	*Cycles per day*	*Tentative* I_c (A)	*Elec* V_{CE} (V)
15	155	210	H_0	100/200	288	1	15
27	155	230	H_0	50/100	576	1	27
55	150	220	H_1	50/100	576	2	22.5
50	125	191	H_1	50/100	576	2	25
22	125	200	H_0	50/100	576	1	22
70	125	190	H_3	600/600	72	2	35
60	100	150	H_3	600/600	72	2	30
27	100	150	H_2	150/300	192	1	27
100	100	180	H_3	100/150	288	3	33.4
32	175	270	H_0	50/100	576	1	32
13	175	270	H_0	180/180	240	1	12
110	75	117	H_3	50/100	576	3	37

practical test (sampling) points that naturally exist. From this set, a dozen or so well-spaced test points are chosen for the thermal cycling rating chart. Table III shows a sprinkling of these 150 possible test conditions, empirically derived. The expected response from data collected at strategic points follows Fig. 4.

Transistor units may fail in various ways. Soft-soldered (lead or other low-temperature solders) transistors usually fail from degradation of the joint between the silicon and the metal package. Some transistors may fail when the bond between emitter, bar clips, or wires and the top of the silicon die fractures. Hard-soldered units usually fail by fracture of the silicon. Careful failure analysis procedure is important to determine all failure mechanisms and to verify that feedback information for device and process improvement is obtained.

The result, a rating chart for a power transistor, accurately tells the designer whether he is within the thermal cycling capabilities of the transistor. Many power transistors will someday be rated for thermal cycling capability, and a test program such as the one presented here will be necessary.

Overstress screening levels and life prediction models

Bell Telephone Laboratories initiated the all-important concept of overstress screening levels and life prediction models, a concept all reliability personnel should understand both for its mathematical foundations and for its practical applications. The industry will see more of this approach, triggered partially by hi-rel custom orders from knowledgeable customers who demand burn-in levels at greater than 250°C. This technique has been initiated at RCA. The Mountaintop plant, for example, is currently doing a 100% burn-in for 16 hours at 270°C on the 2N5038 transistor.

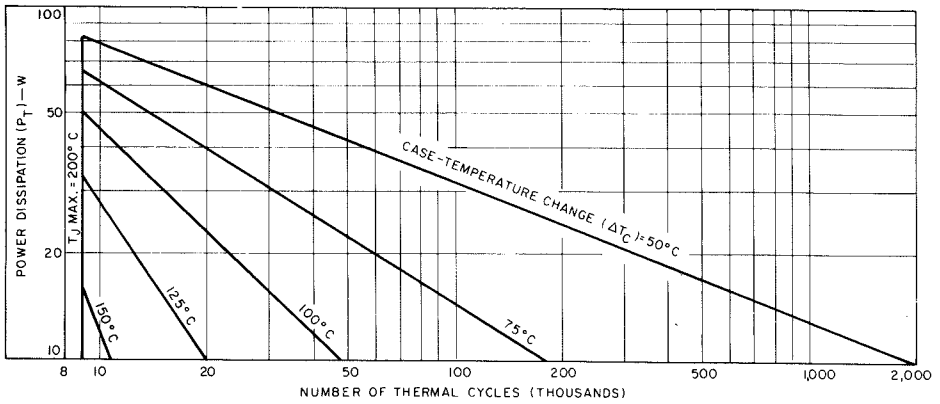

Fig. 4—Thermal cycling rating chart.

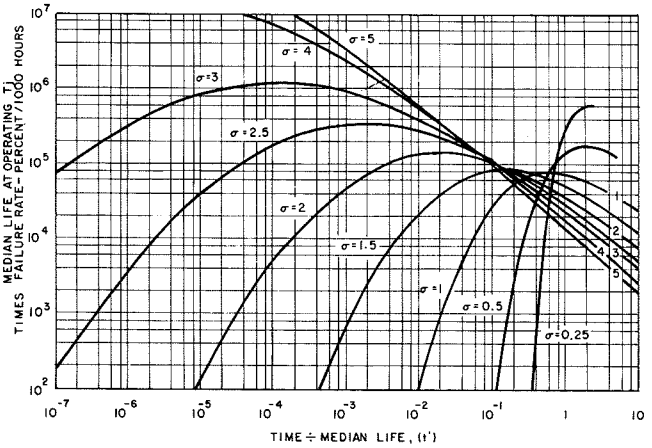

Fig. 6—Log-normal failure rates.

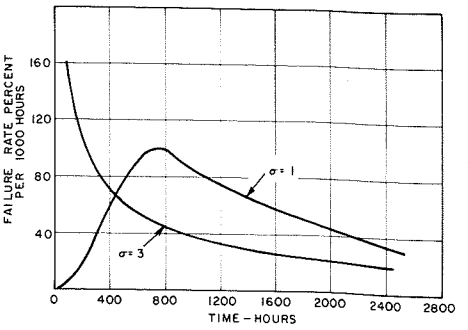

Fig. 5—Log-normal distributions.

For a small investment in sample size and test equipment, the investigator can determine on a given type (a) estimated failures of the population (called freaks, early life failures, or process-variation type failures), (b) central population values, used to predict attainable device capability, and (c) the optimum screening level and its predicted effect on population failure rate. Explanation of the theory with an example is outlined as follows:

Failure modes and mechanisms. The relevant failure mechanisms are those associated with semiconductor surfaces, typically detected on transistors by observing leakage current, breakdown voltage, or beta changes with life.

Failure distribution. For practically all silicon transistors and integrated circuits, Bell labs has found a log-normal distribution of time to failure to be valid. (see the $\sigma=1$ portion of Fig. 5). Proper screening should reject individual devices that constitute the left side of the "hump". After screening, the equation for the log-normal distribution is mathematically defined and useful. If the failure rate is known for a given σ and a given median life, then the failure rate function can be determined as shown in Fig. 6.

Degradation activation energy

The Arrhenius equation, generally used as a model for temperature-dependent failure mechanisms, sets

$$D = A \exp(-E/RT)$$

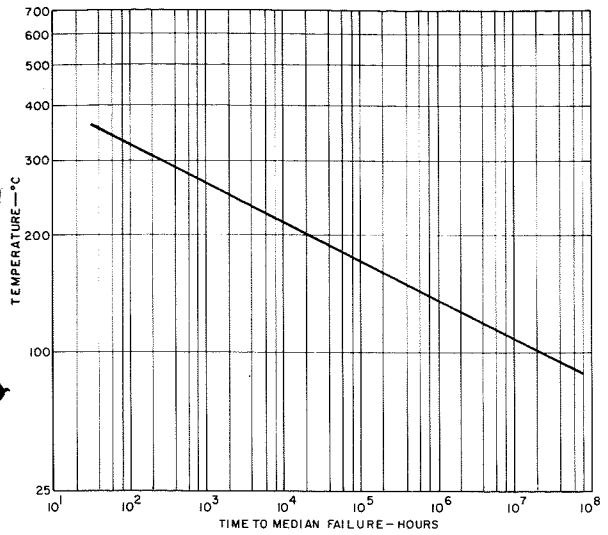

Fig. 7—Acceleration factor—1.1 eV slope.

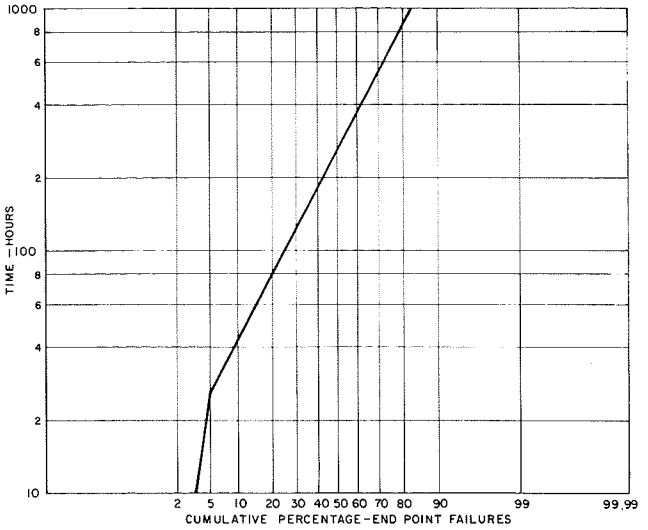

Fig. 8—Log-normal plot.

where D is the diffusion coefficient, A is a temperature-independent constant, E is the activation enerty, T is the temperature in kelvins, and R is the gas constant. According to Bell Telephone Labs, an activation energy of 1.1 eV is representative of the degradation rate of greater than 95% of silicon transistors and IC devices. This indicates a similarity of the dominant failure mechanisms in silicon devices. The acceleration curve, Fig. 7, has a defined slope of 1.1 eV/R and particular devices will have acceleration curves parallel to the one shown. Note that this technique does not depend solely on this particular Arrhenius acceleration model, but in the absence of a well-explored alternative the 1.1 eV slope is usually assumed valid.

Sample calculation

An accelerated DC operating life test is conducted at 300°C junction temperature on a power transistor. The results are plotted in Fig. 8 on log-normal paper. From this graph, the median life (50th percentile) is read directly as 260 hours. The standard deviation (σ) is calculated as ln (time to 50% failures /time to 16% failures) = ln (260/641 = 1.5. If more than one overstress test is performed, the central population regression slopes are examined for possible failure-mechanism differences. The percentage of freaks can be readily estimated from the break in slopes and is estimated at approximately five percent.

Using Arrhenius-type paper as in Fig. 7, a curve with a slope corresponding to 1.1 eV is drawn through the median life (260 hours). If 100°C application point is the objective, the median life at T_j = 100°C can be read directly as 2.2×10^7 hrs.

Assume a trial screening time of 16 hours at 250°C. The median life at 250°C is 2×10^3 hrs.

Calculate "equivalent age" which is a function of all high temperature processing following sealing. Assume a 250°C bake for 24 hours (although bake operations at other temperatures can be used with these curves).

The equivalent age at 250°C is 16 hours + 24 hours = 40 hours.

For failure rate estimate of screen survivors use Fig. 6. Abscissa values = 40 hour (equivalent age at 250°C) / 2000 hour (median life at 250°C) = 2×10^{-2}.

Ordinate value (Fig. 6) for σ = 1.5 is 4×10^4.

Estimated failure rate = Ordinate value/Median life at 100°C = $4\times10^4/2.2\times10^7$ = 0.0018%/1000 hr.

Other trial screening times and conditions can be applied. It is noted that the log-normal distribution has been conveniently characterized with easy-to-use charts that enable rapid estimation of (a) time of maximum failure rate as a function of σ, (b) maximum failure rate as a function of σ, and (c) cumulative percent failures at the maximum failure rate as a function of σ.

Conclusions

Table IV summarizes the six areas in reliability engineering and indicates the engineer's approach in each area.

This paper has discussed some significant areas of growing importance and scope that directly involve reliability engineering. The reliability engineer's job within the RCA Solid State Division is becoming more complex and dynamic due to the greater emphasis on reliability in virtually all product areas, from early development through factory production and customer utilization. Quality and reliability levels that were satisfactory in the past decade must be improved for the marketplace of the 70's.

Table IV—Summary of six areas of reliability.

Item	*Reliability Engineer's Approach*
I. **Accelerated Testing Techniques**	I. Faster response tests; use for control of factories; real-time indicators, group B tests.
II. **Reduction of Design Margins** A. Processing variations magnify reliability response	II. Potential hazard; recognize, investigate, and control. A. Emphasize in-process control.
III. **Customer Reliability Awareness** A. Tougher specifications B. Mixed reliability objectives C. Warranties and safety hazards D. Failure rate and information from vendor	III. More customer/vendor involvement. A. Determine best test for specific failure mechanism. B. Strive for device to pass severest objective. C. Be alert, conduct proper tests in development and production. D. Consult with customer and verify estimates.
IV. **More Complex Devices—(LSI, Modules)** A. Manpower B. Facilities	IV. Develop new reliability approach A. Recognize more manpower needed per unit of data. B. Larger use of sophisticated analytical equipment.
V. **Thermal Cycling Rating Charts on Power Transistors**	V. Design and optimize experimental procedure and conduct tests with proper data analysis.
VI. **Overstress Screening Levels and Life Prediction Models**	VI. Understand both mathematical foundation and practical application. Recommend technique, in specific cases, and quantify expected results.

Schottky barrier devices

R. T. Sells

RCA Computer Systems recently investigated the suitability of monolithic bipolar integrated circuits fabricated with Schottky barrier devices for use in computer equipment. This paper presents some of the conclusions of that study and discusses the theory and application of Schottky barrier diodes in integrated circuits.

RECENT ADVANCES in processing technology have made possible batch production of Schottky barrier devices. Such devices include high- and low-power rectifiers, photo-transistors and diodes, and monolithic collector-to-base clamped transistors for integrated circuits. The integrated circuits are of particular interest to Computer Systems because of the possible reductions in machine cycle time with the wireability and noise immunity equivalent to *TTL*.

The first Schottky diodes manufactured were mesa structures which were frail and had soft (leaky) junctions. As a result, the devices had non-predictable current-voltage characteristics and low reverse breakdown voltages. Recent studies have proven that the non-predictability resulted from unclean surfaces which combined with "edge effects" to cause channeling and inversion layers in the semiconductor material. Once this discovery was confirmed, it became a simple matter of using the techniques of planar transistor technology to eliminate these problems and provide almost ideal current/voltage characteristics.

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received the BSEE from the University of Tennessee in 1965. He has completed graduate courses at Polytechnic Institute of Brooklyn and the University of Florida. Prior to joining RCA Mr. Sells was employed as an integrated circuits design and applications engineer on IFF transponder research and development programs. In 1967, he joined Computer Systems and worked in various component evaluation areas, specializing in semiconductor technology and processing studies. His efforts were instrumental in the establishment of a Components Engineering group. Presently Mr. Sells is responsible for evaluating reliability of the new semiconductor technologies being considered for use in RCA's new computer lines.

* Since this article was written, Mr. Sells has left RCA.

Theory of Schottky devices

Given an arbitrary metal deposited on the surface of any semiconductor, the result has a high probability if being a rectifier. This section explains the theory of this phenomenon.

Band structure

The electron energy diagrams in Fig. 1 are ideal and show energies of free electrons in the metal and n-type semiconductor under various bias conditions. At ZERO bias, there must be an electronic equilibrium between the two materials. This is indicated by a constant Fermi level through the metal-semiconductor contact.

The bottom of the conduction band in the semiconductor, relative to the Fermi level, can be represented to be at a potential ψ_{ms} adjacent to the metal and at a potential ψ_{ns} further into the semiconductor. The potential ψ_{ms} *(barrier potential)* is a barrier to electron flow from the metal to the semiconductor and depends on the type of metal and semiconductor used, and on the reverse voltage applied. Potential ψ_{ns} depends on the semiconductor doping level. The difference between ψ_{ms} and ψ_{ns} (*built-in* or *diffusion potential* $\varnothing'$) presents a barrier to the flow of electrons from the semiconductor to the metal.[1]

When the depletion region width is large, the only means of electron transport at the interface is by thermionic emission over the barrier. Thus, the mechanism of electron flow is analogous to emission from a hot cathode into vacuum: the semiconductor acts as a cathode and the metal as a vacuum. The zero-bias flow of electrons from the semiconductor to the metal results in a current I_s *(diode saturation current)*. This current is a function of junction area, barrier potential, and temperature. Since, in electronic equilibrium, net current must be zero, I_s has a counterpart flowing from the metal to the semiconductor.

When FORWARD biased, as in Fig. 1, the barrier height is decreased permitting electrons to be injected into the metal. These electrons are injected with a large kinetic energy or temperature, compared to the metal's equilibrium electrons, hence the name *Hot Carrier*.

The forward bias voltage reduces the potential barrier on the semiconductor side. This reduction in barrier height results in an increase in the current from the semiconductor to the metal which is exponentially dependent on applied bias. Since ψ_{ms} remains unchanged, current due to the electron flow from the metal to the semiconductor does not change.

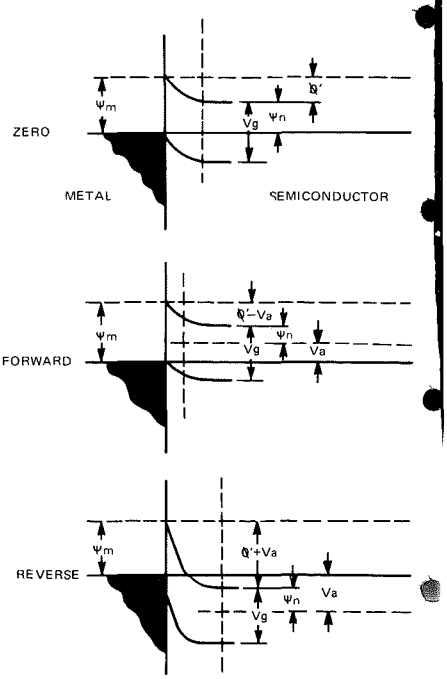

Fig. 1—Band structure for different bias conditions.

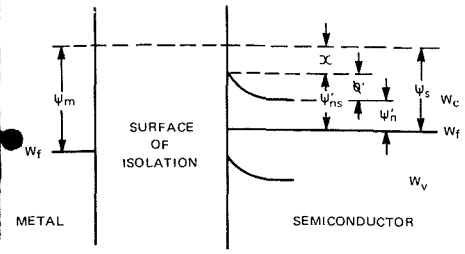

Fig. 2—Band diagram before joining.

For the REVERSE-bias condition (Fig. 1) fewer electrons in the conduction band of the semiconductor have sufficient energy to surmount the barrier. A reverse bias of a few millivolts is sufficient to make the electron current from the semiconductor to the metal negligible compared with the I_s current from the metal to semiconductor. Therefore, for reverse biases of greater than a few millivolts, one would expect the reverse current to be constant. However, this does not happen since devices exist in a real rather than an ideal world.

In addition to a small reverse leakage current which behaves as though a resistor is in parallel with the junction, an effect due to the dependence of ψ_{ms} on reverse voltage is also observed. This dependence is extremely small and is negligible for forward bias, but is very important for reverse bias. The effect, called *image force effect* has been experimentally established as the primary mechanism for reverse current in Schottky diodes. As reverse voltage increases, the diode encounters avalanche multiplication and breakdown in the same manner as diffused diodes.

Barrier height determination

The theory is correct, but the diagrams in Fig. 1 are ideal and not totally applicable to physical devices. Fig. 2 presents the actual band structure of an isolated metal and semiconductor at equilibrium before they are joined. The skew in their Fermi levels (Fig. 2) indicates that the metal and semiconductor are not in equilibrium before joining. ψ_m is the *work function of the metal* and χ *(electron affinity)* is the analogous work function for the semiconductor (Table I). When the two materials are brought into contact and equilibrium, both work functions ψ_m and χ are conserved; the energy diagram is shown in Fig. 3. The resulting difference in the vacuum energy is adjusted by the contact potential, given by $\Delta=\psi_m-\psi_s$.

Table I—Work functions of metals and semiconductors.[2]

Metals	ψ_m
Al	3.74
Mo	4.27
Ti	3.76
W	4.50
Au	4.58
Semiconductors	χ
Si	4.10
Ge	4.56

If one performs the imaginary experiment of bringing a clean metal plate closer and closer to a clean semiconductor surface, an electric field between these surfaces is established and defined by their contact-potential difference divided by their separation. This electric field requires an electric charge in the two surfaces which increases as the separation decreases. In the semiconductor, this charge can arise in two ways:

1) Ionized impurity atoms, causing a space charge layer much like that in a diffused p-n junction.
2) Surface charge induced in surface states which arise because of the termination of the crystal lattice.

There are two broad classes of barriers: one in which the surface charge is dominant, and one in which the surface charge is negligible.

In the latter case, as the metal is brought closer to the semiconductor, the induced charge in the semiconductor will increase; the space charge layer will widen; an increasing fraction of the contact-potential difference will appear across the space charge layer; and less will appear across the gap. In the limit, the entire potential drop is within the semiconductor. In this case, the barrier energy should depend directly upon the work function of the metal. In many semiconductors, such a dependence is a good approximation. However, one additional complication exists. The work function is composed of two parts: one is related to the chemical electronegativity of the metal, and the other to a surface dipole layer caused by a distortion of the electron cloud at the surface. The surface dipole layer is certainly not present in the same form when the metal is in intimate contact with a semiconductor (as when the metal faces a vacuum).

This potential difference gives rise to an electric field (E-field) of magnitude Δ/δ between the two surfaces, where δ is the interfacial gap distance (Fig. 3). The region is similar to a surface oxide which is trapped underneath the metal and typically is less than 50 Å thick.[10]

If δ is small enough, the interfacial gap will be transparent to tunneling electrons. Therefore, the tunneling barrier height is small and can be neglected. This results in the following equation for metal-semiconductor barrier height as seen by the semiconductor carriers.[5]

$$\psi_{ms}=\psi_m-\chi-\Delta \qquad (1)$$

The following relationship was pointed out by Mead and Spitzer for Group IV and III—V materials.[3,4]

$$\psi_{ns}=w_c-w_f=2/3\ E_g \qquad (2)$$

where W_c is conduction-band energy, W_f is the Fermi energy, and E_g is the band gap of the semiconductor.

Conley and Sze[5] have derived the following empirical barrier height expression which accounts for surface states, χ, and image force.

$$\psi_{ms}=A\psi_m+B \qquad (3)$$

The parameters A and B are defined in Table II.

Table II—Experimental values of barrier height ψ_{ms} by the Cowley-Sze relation $\psi_{ms} = A\psi_m + B$.[5]

n-type Semiconductor	*A (volts)*	*B (volts)*
Si	0.27±0.05	−0.55±0.22
GaP	0.27±0.03	−0.01±0.13
GaAs	0.07±0.05	+0.49±0.24
CdS (vacuum cleaned)	0.38±0.16	−1.20+0.77
CdS (chemically (cleaned)	0.84±0.05	−3.3 ±0.23

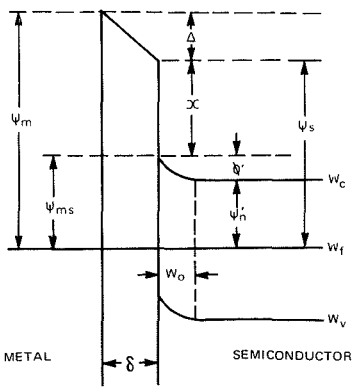

Fig. 3—Band diagram after joining.

Table III—Barrier energies of metals on semiconductors—measured by *I-V* characteristics, capacitance intercept *(cap)*, or photoresponse *(photo)*. (Samples are at room temperatures unless otherwise noted.)

Semiconductor	*Metal*	*I-V*	*Cap*	*Photo*
p *Si*[2] (chem)	*Mo*		0.42	
	Au		0.30	
	Ti		0.60	
	Pt-Si		0.25	
n *Si*[22] (chem)	*Au*			0.78
n *Si*[23] (chem)	*Au*	0.79		
n *Si*[23] (chem; 200)	*Au*			0.82
n *Si*[17]	*W*	0.67	0.65	0.65
n *Si*[2]	*Ag*	0.69		
	Al	0.67		
	Cu	0.71		
	Pt	0.85		
	Ni	0.66		
	Ti	0.50		
	Mo	0.70		

Table III shows more recent values for ψ_{ms} for various metals on n-type and p-type semiconductors.

As shown in Fig. 1, barrier height is a function of applied voltage (V_a). Charge carriers in the semiconductor near the junction experience two kinds of forces: one arises from the field in the depletion layer, the other from image charges in the metal. As an electron moves relative to the barrier, it induces on the metallic interface an opposite *(image)* charge which attracts the electron and thus lowers the effective barrier height. If the height is lowered sufficiently, tunneling will result. Therefore, the image effect plays an important role in avalanche breakdown (i.e., at some fixed reverse bias the junction current will rise due to impact ionization by the tunning electrons.

The image charge correction to the barrier height, $\Delta\phi(V)$, is given by[2]

$$\Delta\phi(V) = \{[q^3 N_{da}/8\pi^2 e^3 e_o^3 e_d^3]\,[\phi + V_a - (KT/q)]\}^{1/4} \quad (4)$$

where e_o is the permittivity of free space, e the static dielectric constant, e_d the image-charge dielectric constant, and N_{da} is the number of carriers (p- or n-types). The terms e_d and e will be equal if the transit time of an electron from the metal to the potential energy maximum is sufficiently long to allow the buildup of dielectric polarization in the semiconductor.

Schottky vs. ohmic contact

So far the Schottky barrier theory has been treated in a general, simplified manner. In its most simplified version, an integrated circuit hot-carrier diode is metal (p-type) evaporated on an underlying n-type-doped piece of silicon to form a rectifying contact. The question arises: Why are the emitter, base, collector, and resistor contacts ohmic instead of Schottky diodes?

When two metals are joined and heated toward their eutectic point, atoms of each metal begin diffusing at the interface. When the eutectic point is reached, a very thin liquid layer forms at the interface, and rapidly dissolves both metals in the appropriate proportion to form a large volume of eutectic alloy. If a limited amount of one of the two metals is available, the process will continue until the limited material is consumed. Therefore, when a thin film ($\leq 1\mu$m) of aluminum is deposited or evaporated on a piece of silicon several microns thick and subsequently heated to 576°C, all the aluminum present is rapidly consumed by the liquid phase.

If such a system is heated higher than its eutectic point, more silicon will be dissolved in the liquid phase. If the temperature is subsequently lowered below the eutectic point, the additional silicon will be rejected from the liquid, forming a regrowth layer of silicon in the interface. This regrowth layer contains a small percentage of aluminum, as determined by the solid solubility of aluminum in silicon (~0.001%). The liquid aluminum-silicon alloy will freeze and form an ohmic contact to the silicon (aluminum silicide), provided the original silicon is either p-type or heavily doped n-type. If it is p-type, the segregated aluminum tends to make it more p-type. If the original material was n-type, the n-type species must be present in the regrowth layer in excess of the solid solubility of aluminum in silicon (5×10^{18}/cm^3) or else a rectifying (p-n) contact will be formed.

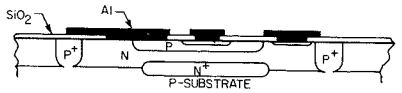

Fig. 4—Cross-section of a collector-to-base clamp.

The depletion width of a junction can be approximated by $W \sim N_D^{-1/2}$. Therefore when the doping of the semiconductor is heavy ($N_D > 10^{18}$ atoms/cm^3), the depletion width becomes quite small. In this case, in addition to the thermionic emission process, electrons can tunnel through the thin barrier. This component of current flow makes the current-voltage characteristics linear over a range of small bias voltages producing an ohmic behavior.

For the normal n-p-n integrated circuit transistor, phosphorus is normally used in surface concentrations of 10^{21} atoms/cm^3 as an emitter dopant so ohmic contacts to these regions are readily formed.

The normal collector consists of an isolated n-type epitaxial layer with doping concentrations in the order 10^{15} to 10^{16} atoms/cm^3. Direct ohmic contact to this region cannot be made without first diffusing a contact area. This is done during the emitter diffusion. Thus, by depositing aluminum directly onto the epitaxial collector layer, a metal semiconductor rectifier can be made. By extending the base contact metallization onto the collector region, a Schottky collector-to-base *(C-B)*-clamped transistor can be constructed as shown in Fig. 4.

Effect of surface states on performance

Schottky diode performance depends on the condition of the semiconductor surface and adjacent oxides. The electrical properties of a free semiconductor surface differ from those of the interior. This is expected since the surface represents an abrupt boundary for the outermost layer of atoms and disrupts the orderly energy distribution in the region.

From a practical point of view, of course, the surface is not perfect. Silicon is very active in air and forms oxide layers quite readily. These layers can absorb chemical ions, water, or gas molecules—depending on the environment to which the surface is exposed.

There are a number of surface energy states that fall within the forbidden band gap of the semiconductor. These surface states have been categorized into two types (*layer states* and *interface states*) each caused by different effects. The layer states are believed

due to the characteristics of the oxide layer and arise from absorbed ions or molecules or perhaps chemical imperfections. Experiments have demonstrated that the nature of the layer states is sensitive to the ambient to which the surface is exposed (e.g., moisture, gases, ionic compounds). The interface states are similar in behavior to the recombination centers of the Shockley-Read-Hall theory. The interface states are found to be independent of ambient, but apparently reflect the quality of the initial surface treatment before the oxide layer is formed. Thus, they are dependent on the kind of chemical or electrolytic etching treatment to which the semiconductor was subjected. Any etch imperfections beneath the oxide layer cause departures from surface uniformity and drastically change the densities and energies of the interface surface states. Following oxidation and metal deposition, heat treatments are required to make contact with the silicon. These high temperature treatments can result in trapping (recombination) centers at the surface.

Therefore, any observed recombination of carriers at the surface is attributed mainly to recombination at the interface centers. Surface recombination is expressed in terms of a surface recombination velocity *s*, in centimeters per second. The magnitude of *s* for any surface is shown to be dependent upon the density of the interface states, the energy of the states, the capture probabilities, the surface concentrations of the holes and electrons, and the degree of occupancy of the interface states.

Thus, the density and energy levels of the interface states are determined by the method of initial surface treatment and are independent of any ambient effects. However, the ambient does affect the nature of the ionic charge in the oxide-layer states, which in turn alters the conductivity and type of the bulk layer just beneath the surface.

During the fabrication of integrated circuit structures, diffusion steps usually follow, or are accompanied by, the growth of a silicon-dioxide layer. The growth of these oxide layers has a pronounced effect on the distribution of impurities within the wafer, principally near the oxide-silicon interface.

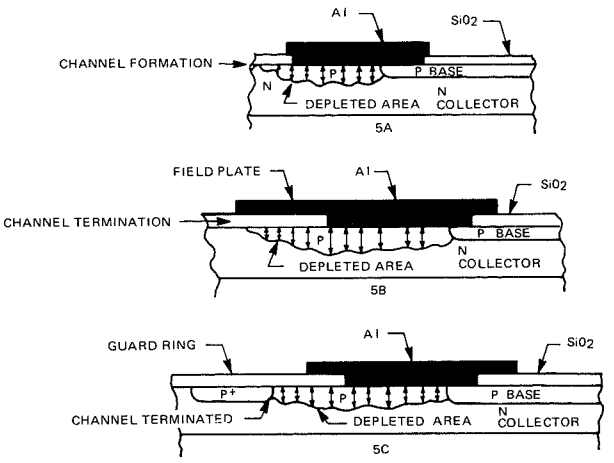

Fig. 5—Cross-section of clamp area.

A second mechanism can also change the conductivity of the silicon near the surface. Carrier concentrations near the surface can be decreased or increased by the presence of fixed charges associated with the oxide. In this case, carrier concentrations change, rather than impurity concentrations as in the previous case. This fundamental difference makes it possible in a practical sense to determine which effect is predominating in a particular situation. Both cases can coexist.

"Snowplow" surface conductivity perturbations are not affected by removing the oxide. On the other hand, if the surface perturbations are charge-induced, the surface tends to return to normal when the oxide is removed.

Inversion and depletion layers have pronounced effects on metal-semiconductor diodes. Early Schottky devices suffered from low reverse breakdown voltages. It was first believed the failures resulted from tunneling; recent experiments have proven they result from "edge" effects. Around the edges of the metal on a hot-electron diode are large fields. If surface or trapped oxide charges are present, the high fields will cause the underlying semiconductor to invert.

As shown in Fig. 5a, high fields at the edge will cause the underlying n-type silicon to deplete of carriers and become p-type. The amount of depletion spreading will depend on the field. If left unchecked, this inversion layer could spread to an adjacent circuit element. The resulting channel will resemble a high-current leakage path and the diode will avalanche; or the circuit will malfunction. Temperature will accelerate this action, and if the IC layout is marginal (i.e., close spacing of circuit elements), the device could operate properly at room conditions but malfunction at elevated temperatures. Thus, the problem would appear to be an intermittent failure.

There are two methods of combating this problem:

1) The metallization can be extended onto the oxide as shown in Fig. 5b. When reverse biased, the metal will act as a field plate and attract both the oxide and silicon charges, thus confining the depletion region to the metal's edge. This fact can be explained by considering an analogy between the Schottky and a normal p-n diode. During diffusion, the dopant not only travels vertically but also diffuses horizontally under the oxide. This lateral diffusion creates a curved radius at the junction's edge, thus reducing its depth. This, in turn, creates high edge fields and is the primary reason for junction breakdowns below those predicted by diffusion theory. The smaller the radius, the lower the reverse breakdown voltages. In essence, the edge of a Schottky diode's metal acts similar to the diffused-diode edge-curvature effect. By extending the metal over the oxide, the "edge radius" is effectively increased and thus more even distribution of the diode's field is obtained.
2) A guard ring can be diffused into the collector and left electrically unconnected (Fig. 5c). This impurity ring is of such high concentration ($\sim 10^{18}$ atoms/cm^3) that it is impossible for a channel to exist within its boundaries and also evenly distributes the diode field by reducing radius of curvature. The ring becomes an effective termination to the depletion region.

Either of these two techniques (or equivalent) must be used in integrated circuits employing Schottky diodes. In

the interest of speed, the extended-metal-over-oxide method should be used for *C-B*-clamped transistors in digital logic circuits, where reverse voltages are ≤ 3 volts. For those applications with reverse voltages ≥ 3 (e.g., diode arrays, diode logic, input clamps) the diffused guard ring should be used.

Electrical characteristics

The mechanism of current flow in a Schottky diode is thermionic emission. Therefore, the *I-V* properties can be analyzed by using the Richardson and Dushman equations.[27] A metal-semiconductor diode has no diffused regions and is a step junction going from a high ($\sim 10^{18}$/cm^3) to a low ($\sim 10^{16}$/cm^3) carrier concentration. By assuming 1) a constant donor density, 2) nondegenerate material, 3) Poisson's equation, and 4) $dV/dx = 0$ at the depletion edge, the depletion layer width and capacitance can be calculated by using existing equations for step junctions.

In the following paragraphs the mathematical expressions needed to design electronic circuits with Schottky diodes are derived.

Forward *I-V* characteristics

The low level *I-V* properties can be expressed by the following diode equation:[1]

$$I_F = I_S[\exp(qV_a/nKT) - 1] \quad (5)$$

where V_a is the diode voltage (volts); n is an ideality factor (Table IV); K is Boltzman's constant (8.62 x 10^{-5} ev/°K); T is the absolute temperature (°K); q is the electronic charge (1.6 x 10^{-19} coulombs); I_F is the diode current; and I_S is the reverse saturation current.

Table IV—Ideality factor n.[2]

n	Semiconductor (n-type)		Diffused guard ring
1.01	Si	Mo	yes
1.06	Si	Au	no
1.01	GaAs	Au	yes
1.04	GaAs	W	no
1.05	GaAs	Au	no
1.16	GaAs	Au	no

Remembering that a Schottky diode functions from thermionic emission, the following equation is used to define saturation current,[27]

$$I_S = A^*AT^2\exp(-q\psi_{ms}/KT) \quad (6)$$

where A^* is Richardson's constant (see Table V) and A is area.

Table V—Richardson constants under different experimental conditions for silicon.[2]

A^* (A/cm²°C²)	Resistivity (Ω-cm)	Barrier height (eV)	Temp (C°)
14—60	13.5	0.78±.02	Room
25—70	13.5	0.78±.02	100°
12—70	1.1	0.78±.03	Room
16—64	1.1	0.78±.03	100°
10—32	0.12	0.79±.02	Room
10—28	0.12	0.79±.02	100°
40	$N_d = 10^{16}$ A/cm³	0.79	Room

Eq. 5 and 6 assume the series resistance is zero which obviously is incorrect. However, the expressions can be modified to include the diode resistance as follows:

$$I_F = I_S\{\exp[(qV_a - I_FR_S)/nKT] - 1\} \quad (7)$$

Referring to Fig. 1, Φ' must be equal to ψ_{ms} before forward conduction can occur. The potential ψ_{ns} depends on the semiconductor doping level to the following equation:

$$\psi_{ns} = (KT/q)\ln(N_c/N_d) \quad (8)$$

where N_c is the effective density of states in the conduction band (i.e., intrinsic concentration) and N_d is donor density. Therefore, the "effective" point of forward bias (i.e., threshold voltage V_T) can be computed as follows:

$$V_T = \psi_{ms} - (KT/q)\ln(2.8\times 10^{19}/N_D) \quad (9)$$

where ψ_{ms} is in volts. Eq. 9 and Table III can be used to calculate V_T for common types of Schottky diodes.

Reverse I-V characteristics

The reverse currents of a Schottky diode are usually larger than those of its diffused counterpart. The total reverse current is made up of two parts: bulk and surface leakage.

The bulk leakage current is given by the following equation:

$$I_b = A^*AT^2\exp\{[-q/KT][\psi_{ms} - \Delta\phi(V)]\} \quad (10)$$

which is identical to Eq. 6 except that the image force lowering effect has been included.

The surface leakage is given by

$$I_{surf} = I_{sp}P_r \quad (11)$$

where I_{sp} is the saturation current per unit length and P_r is the length of the diode perimeter. The term I_{sp} is experimentally determined by measuring saturation currents on two or more diodes from identical fabrication processes but with varying perimeter lengths. Therefore, the total reverse leakage current is given by:

$$I_R = A^*AT^2\exp\{[-q/KT][\psi_{ms} - \Delta\phi(V)]\} + I_{sp}P_r \quad (12)$$

Depletion width and capacitance

Depletion width for a step junction diode is given by:[9]

$$d = 2e(\Phi' - V_a)^{1/2}/qN_D \quad (13)$$

where d is the depletion width; e is the dielectric constant; Φ' is the degree of band bending (neglected where V_a is large); and N_D is the donor density of semiconductor (n-type).

The sign convention chosen makes Φ' positive for a metal-n-type semiconductor diode.

By using Eq. 13, the capacitance per unit area can be expressed:

$$C/A = [eqN_D/2\Phi' - V_a)]^{1/2} \quad (14)$$

Under forward bias, the capacitance of a pn junction is determined by the stored minority carriers giving rise to a diffusion (storage) capacitance which dominates in the transition region. Since Schottky diodes theoretically have no minority carriers, diffusion capacitance is negligible.

From the capacitance law, the built-in voltage Φ' of the Schottky barrier can be determined. By rewriting Eq. 14:

$$1/C^2 = 2\Phi' - V_a/A^2\,eqN_D \quad (15)$$

and plotting $1/C^2$ vs. V_a, a straight line is obtained which intercepts at $V_a = \Phi'$.

Switching speed

The storage of minority carriers which must recombine accounts for a diffused diode's reverse recovery time. Since there are no minority carriers in Schottky devices, the reverse recovery (switching) time will be determined by its RC time constant.

By differentiating Eq. 5 and solving for dV/dI, the total series resistance can be obtained for currents much larger than I_s:

$$R_T = nKT/qI_F + R_s \quad (16)$$

The transition capacitance can be expressed as[28]

$$C_T = AC_o\left[\frac{\phi' - KT/q}{\Phi' - V_a - KT/q}\right]^{1/2} \quad (17)$$

where C_o is the capacitance at zero bias and Φ' and V_a are in volts.

Therefore, for Schottky diodes, the reverse recovery time is given by:

$$t_R = 4\tau = 4\,AC_o\left[\frac{\Phi' - KT/q}{\Phi' - V_a - KT/q}\right]^{1/2}\left[\frac{nKT}{qI_F} + R_s\right] \quad (18)$$

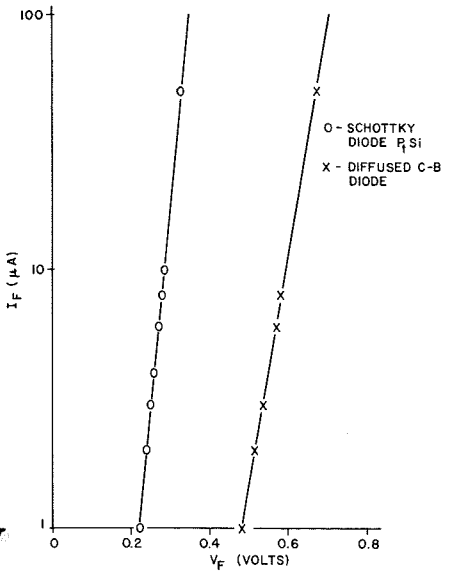

Fig. 6—Forward *I-V* curves.

I-V temperature sensitivity

The difference in forward voltage temperature coefficient between Schottky and diffused diodes is approximately 0.5 mV/°C for current densities less than 10^3 A/cm^2. This mismatch plays an important role in circuits utilizing *C-B* Schottky clamped transistors.

Circuit applications and performance

Since Schottky diodes exhibit approximately half the forward voltage drop of their diffused counterparts (Fig. 6), they make effective saturation prevention devices when used as *C-B* clamping diodes for bipolar integrated-circuit transistors.

Advantages

By using the diodes as logic elements or as *C-B* clamps, a logic circuit can be designed which offers the following general advantages:

1) Less sensitivity to temperature variations (since Schottky units can be used to offset transistor *B-E* variations);
2) Propagation delays through a logic gate can be reduced 50%.
3) Both slow and fast transistors can be manufactured on the same silicon substrate, thus making available a large number of speed combinations.
4) High-gain transistors can be used, thus increasing the fan-out.
5) Gold doping can be eliminated since transistor gain need not be lowered to reduce transistor storage time.

Disadvantages

Certain disadvantages of using Schottky diodes/transistors can also be recognized:

1) Output low voltages (logical 0) will be significantly higher since the output transistor does not saturate. This reduces noise immunity.
2) For each Schottky diode used in the forward path of transfer, the threshold voltage of the circuit will be lowered by approximately 0.3 V, thus further reducing noise immunity.
3) The process control requirements for these transistors are more stringent than for charge-storage devices.
4) A NAND/NOR gate constructed with Schottky transistors will generate more crosstalk noise than the same gate constructed with saturating units because the same amount of current is switched in half the time.

Concluding remarks

During the investigation of Schottky devices, several interesting conclusions were reached regarding their application and manufacture.

1) A Schottky integrated circuit, compared to its charge-storage counterpart, exhibits a 50% lower switching speed, lower AC and DC noise immunity, and higher crosstalk noise.
2) If appropriate precautions are taken during design and fabrication, the MTBF of Schottky integrated circuits should be comparable to that of their charge-storage counterparts.
3) Following metallization and annealing, subsequent heat treatment could be detrimental to the Schottky contact. Therefore, the IC package should require low sealing temperatures ($\leq$ 400°C).
4) Use of Schottky transistors eliminates the need for gold doping.
5) An aluminum-silicon (*Al-Si*) Schottky diode is the one most compatible with presently used *TTL* processing techniques and the least complicated of the various structures currently being investigated.

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Submitting to UL for safety

D. K. Obenland | F. E. Korzekwa

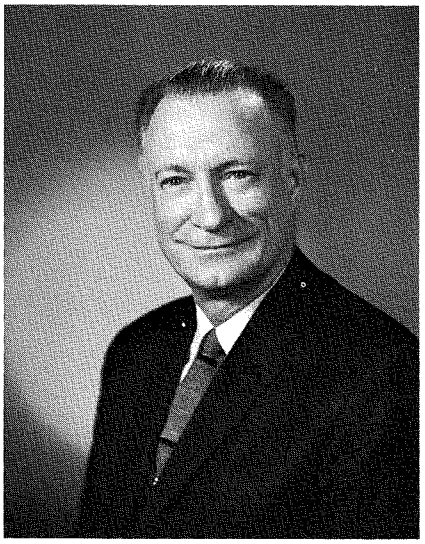
Every RCA consumer product that could involve a casualty, shock, or fire hazard qualifies for Underwriters' Laboratories, Inc. (UL) approval and is listed with the Laboratories prior to shipping. In the product year 1970 alone, over five hundred different basic models of televisions, phonographs, radios, tape recorders, and combinations were submitted to the Laboratories and eventually received Listing. This paper outlines the steps required to obtain UL approval and Listing.

UNDERWRITER'S LABORATORIES, INC., (UL) is an independent testing laboratory, self-described as a "nation-wide, not-for-profit organization testing for public safety". The Laboratories were established in 1894 by the insurance industry for the purpose of setting safety standards and safety testing methods for the budding electrical industry. Today, the Laboratories employ some 2,000 persons, and each year test over 30,000 items. In addition to household appliances, The Laboratories maintain safety standards for, and test such diverse items as, building materials; fire protection equipment; electrical construction materials; hazardous location equipment; accident, automotive, and burglary protection equipment; marine equipment; gas and oil equipment; and heating, air conditioning, and refrigeration equipment.

Currently, The Laboratories have offices and testing stations in Chicago and Northbrook, Illinois; Melville, Long Island, New York; Westwood, New Jersey; and Santa Clara, California. Due to its Indiana location, RCA Consumer Electronics obtains Listings through the Chicago office.

To qualify for listing with UL, RCA consumer electronic products must meet all the current requirements of the standard for safety for *Radio* and *Television Receiving Appliances,* UL 492, and subsequent proposals and revisions in effect on the date of manufacture of the model.

The procedure for obtaining Listing is essentially as follows (with exceptions). First, as early as possible and prior to production, a representative sample of the model, along with certain key spare parts and schematics, is delivered to UL. Extra spare parts are necessary to replace parts destroyed during routine testing, testing for possible hazards, or while investigating abnormal conditions. This sample could represent only one model or any number of similar models. The sample is then tested by UL engineers to the pertinent UL standard. If any item does not comply with the Standard, UL officially notifies RCA, and changes are made accordingly. During this time a complete file containing descriptions, UL test data, and other information about the model is established at UL. During the first few days of production of the model, the UL engineer visits the factory for a factory production inspection. His inspection verifies that this model is, indeed, being built to the Standard, and that items not complying in the initial submission have been corrected. If the inspection is successful, RCA is notified in a few days that the model is "acceptable for Listing". An "authorization to ship" is then signed by the Manager, Underwriters' Laboratories Coordination, Consumer Electronics and the Listed model may then be shipped.



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graduated from RCA Institutes, Inc., (Chicago) in 1935, and is a registered professional engineer in the state of Illinois. From 1935 to 1948, he was actively engaged in the design of AM, FM, and short wave receivers at E. H. Scott Radio Laboratories in Chicago. He joined RCA in 1948, working first with the "Berkshire Line" of custom AM, FM, short wave, and television receivers. In January, 1950, he joined the early RCA color television development effort, where he worked on high voltage generation and instrumentation of the first color television instruments. Beginning in 1951, he was involved in the manufacture by RCA of proximity fuses, ARC-21 components, and A4 depth charge fuses for the military. From 1952 to 1956, he was manager of the Cannonsburg, Pennsylvania, factory manufacturing artillery shell proximity fuses. In 1956, he again transferred to RCA Home Instruments, and in 1961, he was assigned the responsibility for Underwriters' Laboratories coordination and division standards for RCA Home Instruments (Indianapolis). In 1970, he was promoted to Manager, Underwriters' Laboratories Coordination. Presently, he is a member of the Underwriters' Laboratories, Inc., Industry Advisory Committee for Radio and Television Receivers, a member of various UL Ad Hoc Committees, and a member of the Electronic Industries R-1 Safety Committee.

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received the BSEE from the University of Texas in 1962, and has since taken graduate courses from Purdue University. In 1962, he joined RCA under the Technical Training Program and has worked as an audio design and instrumentation engineer in the Radio Victrola group until 1969. Since 1969, he has worked in UL Coordination.

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Before submission

Long before a model is submitted to UL for testing, the design is influenced by Underwriters' Laboratories requirements. The Safety Standard, UL 492, has been in existence since 1928 with the twelfth edition published in September, 1968, and RCA models have been meeting this standard since the early days. The design engineers are well aware of the general requirements and the impact of these requirements on the circuit design. Certain items not previously tested to the Standard or questionable items are discussed with UL engineers for guidance before the design is completed. A large number of parts used in a specific design are not totally new parts; that is, they have been tested previously by UL. Therefore, in reality, a large number of personnel and many Consumer Electronics departments are involved in this preparation. When a sample is finally ready for submission to UL, it is screened by electrical and mechanical design and by an engineer from the Underwriters' Laboratories Coordination group in Consumer Electronics (Fig. 1). In this manner, some items that might not meet UL requirements, or pass UL tests are changed in time to keep the design cycle intact.

Submitting for Listing

A sample is submitted along with a letter describing the model and any similar models and authorizing The Laboratories to do testing in behalf of the company. At the same time, certain key spare parts and schematics are delivered to the UL engineer who will supervise testing. A consultation (Fig. 2) with the engineer at this time (and a preliminary discussion of the schematic and sample) yields a list of additional parts that will be required for testing the instrument. Spare parts are needed because parts may often be destroyed due to the extreme stress placed upon the products and components during testing. Upon the completion of the preliminary consultation, the project is officially "established" at UL, a file is opened, tests required are defined, a cost limit is established, and testing to the Standard begins.

The standard

UL standards specify safety needs of a certain industry. The UL 492 Standard, for example, covers the majority of domestic radio, television, phonograph, and tape recorder manufacturers. The general requirement of UL 492 is stated in paragraph 24 as follows:

> ". . . The construction of the appliance shall assure that normal use and user servicing does not result in a shock, casualty, or fire hazard; that the materials and components are used within their electrical, mechanical, and temperature limits; and that the assembly will protect the components and wiring from being displaced or damaged."

In practice, this is accomplished by providing a "UL enclosure" (the cabinet) in which the electronic chassis is housed and protected. The cabinet is tested to ensure that user access to hazardous voltages inside is not easily attainable and that the cabinet cannot easily be broken. The electronics inside are subjected to tests intended to reveal any potential fire, shock, or casualty hazards. The Standard defines certain construction, material, assembly, accessibility, temperature, interconnection, and component-life requirements, as well as specific tests that help to ensure the above requirements.

The UL 492 Standard is updated and modified by the Industry Advisory Committee (IAC) of the Underwriters' Laboratories, Inc., which determines the committee membership and calls the meetings. This committee currently consists of ten representatives of domestic manufacturers, three foreign representatives, and a minimum of six representatives of the Laboratories. The thirteen industry representatives serve only in an advisory capacity and have no vote on the committee. The chairman of this committee is always a UL representative. The current chairman is also a UL Vice President and Chief Electrical Engineer. Mr. D. K. Obenland, Manager, Underwriters' Laboratories Coordination, Consumer Electronics, is one of the industry representatives on this committee.

Meetings are held periodically for the purpose of discussing the Standard and proposing changes. Proposed changes are circulated to representatives of all companies in the industry, UL personnel concerned, EIA representatives, government representatives, and others, as well as the com-

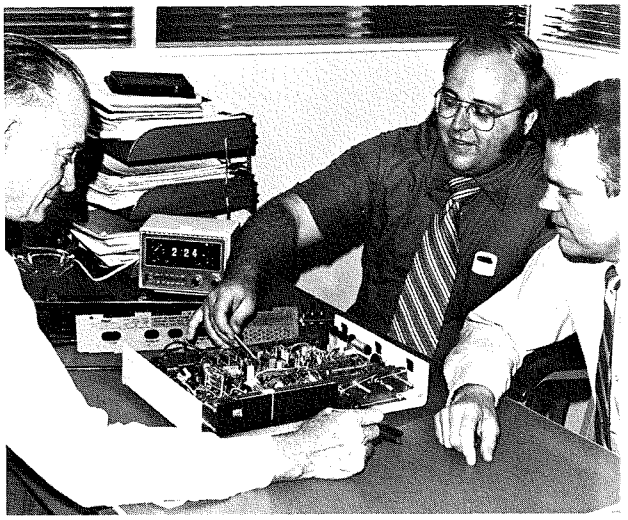

Fig. 1—Screening a model prior to submission to UL (D. K. Obenland, John Oman, F. E. Korzekwa).

Fig. 2—Paul Cassidy (right) and John Cristiano (center) of Underwriters' Laboratories, Inc. discuss a UL requirement with D. K. Obenland. (Photo courtesy of Underwriters' Laboratories, Inc.).

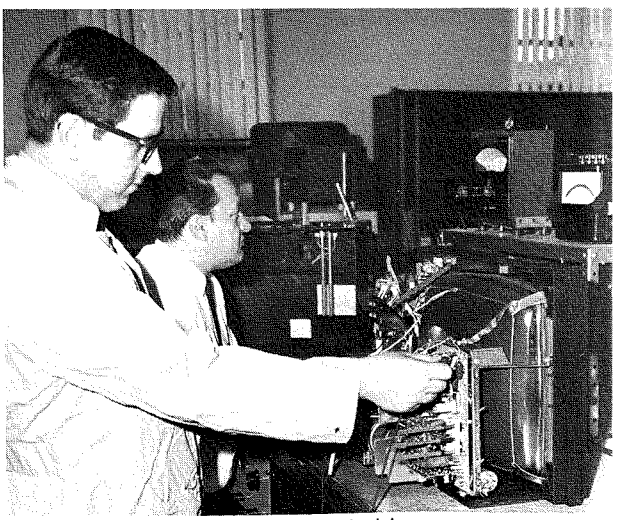

Fig. 3—An RCA black and white television receiver undergoes tests at Underwriters' Laboratories, Inc. (Photo courtesy of Underwriters' Laboratories, Inc.).

mittee members themselves. A deadline is set for receiving comments on the proposal or criticisms of it. At the end of this time, another meeting is called, if necessary, for the purpose of reviewing comments on the proposal. If accepted by UL, a date is set for its implementation (if not previously set); and the proposal becomes a part of the Standard on that date.

Testing to the Standard

The basic requirements are stated in UL 492, but models must pass specific tests, and requirements must be interpreted as to their meaning in some instances. To supplement the Standard, many requirements are written as test procedures that are easier for a laboratory technician to follow. Certain interpretations are established and followed as precedent.

Once the tests required are determined by the engineer responsible, testing begins (Fig. 3). The test laboratory (at Chicago) is set up in such a manner that a model can be moved from one test station to another with designated tests performed in order at each test station. The destructive tests are normally performed last.

First, input power, temperature, AC dielectric, and x-ray radiation tests are performed and the results recorded. The model is checked for correct identification and rating labels and for all required warning and informative markings.

Certain components, such as AC line switches; across-line, line by-pass, and antenna coupling capacitors; and/or resistors, fuses, circuit breakers, overload relays, power-cord connectors, power cords, wire, sleeving, tape, insulating systems, and insulating materials are already recognized (Listed) by UL and have been tested to the particular standard that applies to the component. For example, power cords are normally tested to the standard for *Cord Sets and Power Supply Cords,* UL 817. If a component is already Listed by UL, the engineer determines that the component is being used within its previously established ratings in this new application, and verifies that the component is suitable for that application. This separate "yellow card Listing" by UL saves considerable time, effort, and duplication.

Tests are performed on the cabinet to ensure that it meets the requirements of a "UL enclosure". A tapered probe of exactly specified dimensions is inserted in all openings to see if it might contact hazardous voltages. A hazardous voltage (shock hazard) is defined by the Standard (for antenna terminals) as one greater than 42.4 volts, if the current available from it through a 1500-ohm load is more than 1 mA. Plastic cabinets are also subjected to an elevated temperature of either 60°C (operating at 130-volt line) or 90°C (non-operating) for seven hours. After this test, the cabinet must again pass the same probe access test.

Points on the top, sides, back, and front of television cabinets are subjected to twenty pounds of pressure through a ½ inch rounded rod for one minute. The bottom is subjected to fifteen pounds of pressure in the same manner. For other types and sizes of instruments, this standard varies somewhat. The television cabinet is also impact tested in various places on the bottom, front, top, and sides with a two inch diameter steel ball weighing 1.18 pounds. This ball is dropped from a height of 4.5 feet which results in a five foot-pound impact on the cabinet surface. The cabinet back is subjected to a four foot-pound impact in the same manner. For this type of test, the ball must not make an opening in the cabinet which allows accessibility as judged by the probe, and no other type of hazard must result. As before, this test varies somewhat for other types and sizes of instruments.

The fifty-watt test points are determined by the use of a variable high power resistor and wattmeter. These are the points where fifty watts can be obtained in addition to the power already being used by the circuit(s). A new proposal scheduled to go into effect on January 1, 1972, requires that the one-hundred-fifty-watt tests be superseded by fifty-watt tests making the testing requirements more consistent. In succession, starting with the lowest power points first, these points are then subjected to a short-circuit, maximum-power-overload, and limited-power tests for seven hours or until failure occurs. Each test is repeated two additional times with damaged parts (blown fuses, opened

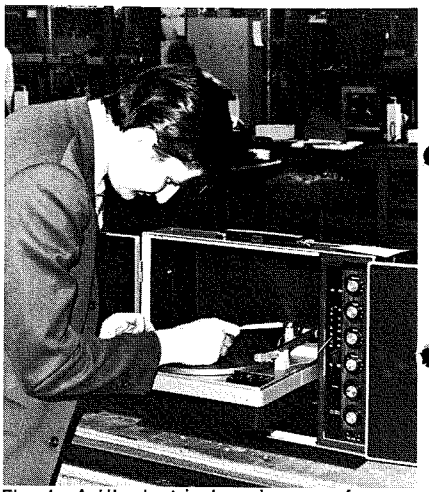

Fig. 4—A UL electrical engineer performs a factory inspection of a model prior to listing.

resistors, etc.) replaced before each test. No shock, fire, or casualty hazard must result from any of these tests.

This is not intended to be a complete listing of all tests performed but most of the basic tests are mentioned, and they convey the basic intent. Components, such as transformers and motor-transformers are also tested to well-defined standards. Test results are recorded on standard forms which become part of the complete report. Complete descriptions of all critical components and construction features directly affecting the tests are requirements and are written into the report. The basic idea is that if any of these items were to change, the test results obtained might differ and possibly not meet the Standard. This information is used by UL for factory inspections and follow-up by local inspectors and for a reference.

Review

Upon completion of testing and after the report is written, the project is thoroughly reviewed by the UL engineer responsible and a UL supervisory engineer. This review verifies that

1) all applicable tests were conducted.
2) UL approved materials are being used,
3) all questions are resolved,
4) the report is complete and accurate, and
5) all requirements are being fairly applied to all manufacturers.

All items not complying with the Standard are recorded on the appropriate page of the report and a letter listing these items and the status of the project is sent to this office. If this model is to begin factory production

in the near future, plans are made for a UL engineer to conduct a factory production inspection of this model. Otherwise, the project is put into an inactive status pending the factory inspection.

Factory inspection and afterward

During the first few days of production of the model, a UL engineer visits the factory for a factory production inspection (Fig. 4). There are many reasons for his visit.

1) He checks production models to verify that production is identical to the model submitted and tested and that the items not complying initially have been corrected.

2) He verifies that certain production requirements of the Standard are met.

3) He verifies that a "hi-pot" test which is intended to identify accessible parts that might accidentally become live is being performed on the production line (Fig. 5).

4) He notes if cable assemblies and hook-up wire are manufactured of UL-labelled wire as required by the Standard.

5) He checks solder bath temperatures and dwell to ensure that printed boards are being soldered within their limits as established by another UL standard.

6) He monitors several other items such as x-radiation tests and/or records and

7) Finally, he verifies the accuracy of the report itself.

As a continuous check to see that the Standard is being observed in production, Underwriters' Laboratories maintains a world-wide system of local inspectors known as the Follow-Up Service which is required to make at least four additional inspections every year of any factory assembling listed models. This inspector uses descriptions in the report to verify that unauthorized changes have not been made and that recognized (yellow card) components are used in specified applications. In general, he verifies essentially the same items as covered in the initial production inspection.

Fig. 5—UL-required "Hi-Pot" test equipment in use on an assembly line (Indianapolis).

Listing and release

If the model passes the factory production inspection just described, the UL engineer, upon return to his office, issues a "notice of acceptability for Listing" for the model or models in question. This is the official *UL approval*, or more correctly, *Listing*, and is formal notification that the subject models meet the requirements of the Standard and authorizes the use of a UL label.

Fig. 6—The UL listing mark on a tape recorder signifies compliance to a UL safety standard.

The certification mark is normally the letters UL enclosed by a circle as shown in Fig. 6. This symbol may appear anywhere on the instrument where it is visible, and may be molded in, stamped in permanently, or appear on a non-transferable permanent label secured with adhesive. The UL mark or label *is* the certification that the model is Listed; i.e., it serves as the agent identifying the Listing. Until recently, the mark did not have this significance; its use was optional with the manufacturer, and it did not have to appear on the instrument—even though the instrument was Listed. Prior to that time, the only evidence of Listing was the appearance of the model number on a "white card" which was not generally accessible to the consumer.

Once notification of Listing is received by the Underwriters' Laboratories Coordination office at Consumer Electronics, an "authorization to ship" these models is signed by the Manager of the activity and the products then may be shipped from finished goods stock.

Conclusion

Obtaining Listing is not simply a matter of "asking and receiving". It is normally a lengthy procedure involving the careful coordination of many individual and departmental efforts within Consumer Electronics and the Underwriters' Laboratories. Coordination and follow-up of the submission cycle is critical since any of numerous possible bottle-necks can hold up Listing indefinitely.

Once listing is obtained, the task of assuring that the Listing remains valid begins. The design engineer, if he initiates changes that affect the Listing, must resubmit these changes as "alternate constructions" for approval before they are used in production. All departments concerned must ensure that all additions or changes of the Standard are incorporated in the design by their effective date. Purchasing, among other responsibilities, must ensure that these changes are reflected in purchased materials and that UL labeled wire and Listed components are purchased for use by the factory.

The factory assures that the "hi-pot" test is continuously being performed correctly and the other production requirements are always met. RCA Resident Engineering is in a position to help ensure that Design Engineering and factory UL responsibilities are met. The Vendor Liaison activity obtains and oversees the approval of material and parts that meet the Standard and changes in the Standard. Component Engineering designs components to meet the Standard and acts to incorporate changes as they apply. RCA Quality Control and the Consumer Acceptance Laboratory monitor the product at various stages of assembly. The Scheduling activity keeps the RCA UL Coordinator (and hence UL) informed of certain key production starts. Other departments also are involved in this effort to keep the Listing valid. Finally, the Underwriters' Laboratories Coornidation office is responsible for the coordination of this entire effort.

Models change every year and the cycle must be repeated all over again. All in all, it is a never-ending job.

There's more to typesetting than setting type

P. E. Justus

Typesetting was until very recently the work of skilled artisans and craftsmen; justification (the process of spacing lines uniformly to the same length) and page layout were largely dependent on the taste and esthetic judgment of the typesetter. But today many modern shops use computers to perform these important tasks. This paper outlines the basic problems and considerations of line justification and page composition and outlines a few of the alternative solutions.

EARLY USE OF THE COMPUTER to solve typesetting problems applied primarily to line justification and word hyphenation. Because computers have been used successfully in these areas for over a decade it is often assumed that justification and hyphenation can be taken for granted; but knowing general techniques is not equivalent to having a program thoroughly checked out and operating. This is particularly true in justification programs where logical subroutines (which combine to make up the justification process) may be scattered throughout a larger program.

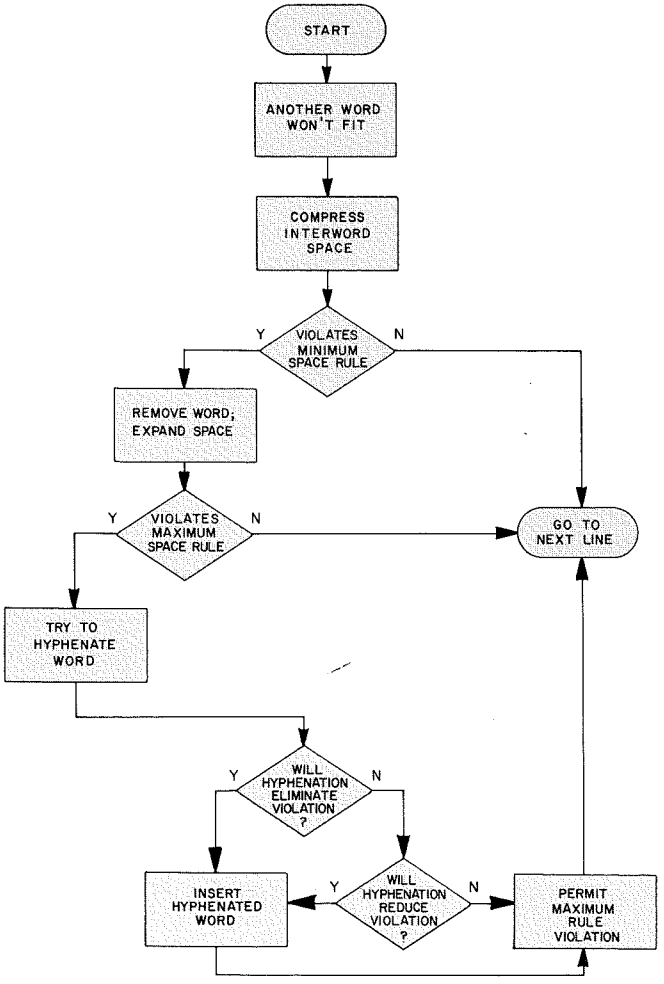

Fig. 1—Flow diagram of the justification process.

Justification

The purpose of justification is to set a line of type to a predetermined width. This would appear to be quite simple. The width of the line is known, and the width of each word on the line can be determined by accumulating the individual widths of the characters in the word (these character width values are available from "set-width" tables). Interword spaces can be expanded or contracted to force an exact fit. In addition, a few simple rules must be observed:

To achieve justification, the spaces between words should be adjusted consistently across the line. In most cases, this rule applies equally to spaces between words and sentences.

Normally, interletter space in a word is not subject to adjustment (narrow column widths may sometimes warrant exceptions).

Very small interword spaces are not permitted—distinct separation of words is essential for ease of reading.

"Loose lines" (lines with excessively wide interword spaces) are to be avoided.

To maintain good spacing when justifying by computer, three values of interword space are used for each space character: a minimum, a maximum, and a basic or ideal value (used tentatively in the process of assembling a line). It is possible for different interword spaces on the same line to have different width values which may depend on type size or even style.

When the computer assembles a line and another word will not fit, an attempt is made to compress the interword spaces on the line to accommodate the overset word. If this should violate a minimum space value, the word is temporarily removed from the line (along with the preceding interword space) and an attempt is made to justify the remaining line by interword space expansion.

If a maximum space violation occurs, hyphenation is attempted and the compression/expansion process is applied to each of the possible partial words with an added hyphen character. If all preceding attempts fail, the maximum space is violated. If possible, a word is broken and hyphenated

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Thefirstsyllableofchurchman poses a problem in this example.

The first syllable of churchman poses a problem in this example.

Fig. 2—Undersetting is preferred to oversetting.

to minimize this violation. The justification process is illustrated in Fig. 1.

In the sample paragraph (Fig. 2) the word *churchman* oversets the first line. If one more syllable is forced onto the first line, the minimum space value is violated. If not, the maximum space value is violated. The second solution is preferred in spite of the loose line which results.

A word is a word

We have discussed justification in terms of words and spaces. If it seems unnecessary to examine what is meant by the term "word," consider the fact that in the computer, characters are processed one at a time. Characters may be collected into words, but established rules must determine when the collection process is complete. Obviously, the letters from one space character to the next form a word. They may also form two words.

Fondly do we hope—fervently do we pray—....

Hope and *fervently* must be treated separately for purposes of justification as well as hyphenation. Moreover the embedded *em* dash (long dash) can be treated much like a word and may appear at either end of a line, subject to the typesetting conventions in force. Not so with the hyphen of a compound word. For example, if "shorthanded" must be broken into the component words for purposes of justification the hyphen obviously can not appear at the beginning of a line.

Clearly, punctuation can not be considered as part of a word when hyphenating; but punctuation must be included with the word when justifying.

(Why is punctuation justified with the word ?) That's why!

Footnote citations must be treated much like punctuation in this respect.

A sample footnote citation shows why [10]!

The process of assembling a word involves more than searching for a space, an *em* dash, or some other word-terminating character. In the footnote example there may be intervening typesetting instructions such as commands to change the size of type, the vertical setting position or other factors. In fact, the footnote citation itself may be generated within such typesetting instructions. These examples illustrate only a few of the complexities involved in separating text into words.

Hyphenation

The usual approach to hyphenation by computer is to program an algorithm which can find hyphen positions within any word by analysis of the letters which make up the word. Many different techniques have been used, none of them perfect. To facilitate comparisons, there are various means for measuring the success of individual hyphenation algorithms. One simple index of an algorithm's accuracy is the ratio of the number of incorrect hyphens to the total number of hyphens found by the algorithm in a large collection of representative words. However, this measure overlooks efficiency, gauged by the number of hyphens the algorithm should have found but missed. Inaccurate algorithms result in badly placed hyphens. Inefficient algorithms have a telling effect on justification, causing many unnecessarily loose lines.

To compensate for the deficiencies of "logical" hyphenation an "exception dictionary" is usually incorporated. It

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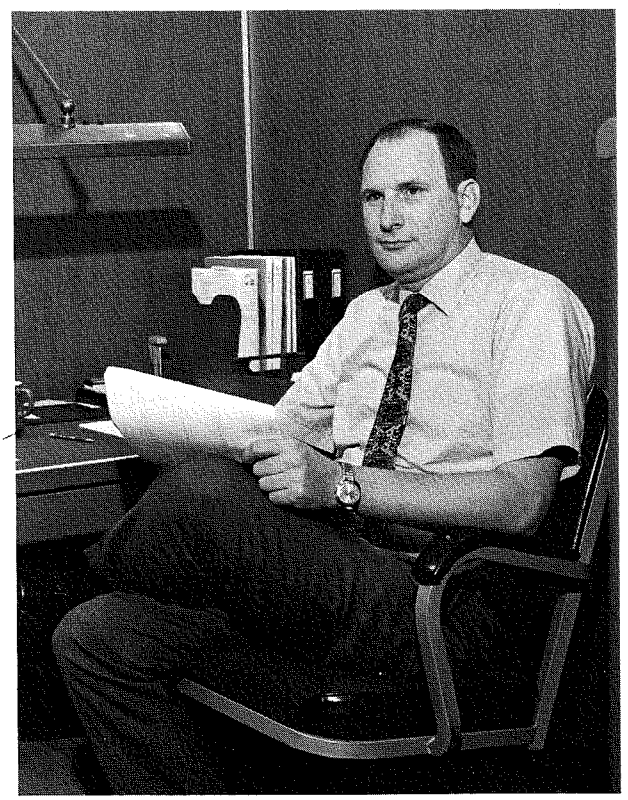
received the BA in mathematics from Kansas State University in 1961. He was employed as a programmer by Eastman Kodak Company and by Honeywell, Inc. before joining RCA Graphic Systems Division in 1966. At RCA he became responsible for the design and programming of system support programs for the PAGE-1 system and was later given responsibility for the entire PAGE-1 system and then for design and development of PAGE-2. Both PAGE-1 and PAGE-2 perform text composition for the RCA VideoComp typesetter. Mr. Justus is currently responsible for a composition system being developed for the RCA 1600.



contains a list of words known to be incorrectly hyphenated by algorithm. This exception dictionary may be stored on a peripheral medium such as a disc and consulted each time hyphenation is attempted. Even if a "perfect" logical hyphenation routine were available, it is likely that an exception dictionary would be needed to accommodate differences of opinion among authorities.

If all problems of hyphenation have not been solved, at least some progress has been made since that night, when according to legend, an RCA Marketing manager received a phone call from a disturbed customer. His 301 had just hyphenated "God"!

Page make-up

When the role of computer typesetting was enlarged beyond line composition to include "makeup" of complete book pages a new dimension in complexity was added. Though there are many variations of rules applying to justification and even to hyphenation, conventions associated with page makeup are considerably less universal. Many of the problems associated with full page composition—whether performed manually or by program—derive from composition rules and conventions developed over a period of many years. Publishers and typesetters adopt different variations and combinations of these conventions for their own standards. But even within a framework of standards, there are conflicts between rules which require compromise. When makeup is performed manually the typesetter can make these compromises based on experience and esthetic judgment. Since computer decisions must be anticipated when the program is being prepared, it is useful to examine some of the general constraints within which page composition decisions are made.

Book design

"Book design" involves many elements of style. For example, typefaces (or styles of type) to be used are designated in the design specification. Distinctions between typefaces are sometimes obvious; sometimes subtle, but the choice of typeface is an important factor in the appearance of the book and in the selection of other style parameters. Sample characters from four different, commonly used typefaces are shown in Fig. 3.

10 Point Video Gothic Bold — **ABCDEFGabcdefg**

10 Point Video Times Roman — ABCDEFGabcdefg

10 Point Video Technica Medium — ABCDEFGabcdefg

10 Point Video Gael Italic — *ABCDEFGabcdefg*

Fig. 3—Four commonly used typefaces.

Fig. 4—Different typefaces in the same point size may have different heights.

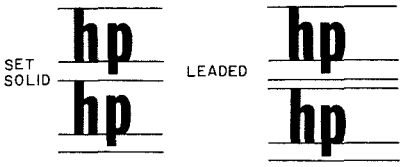


Fig. 5—Leaded and unleaded lines of type.

Point sizes (or type sizes) are also designated in the design specification. A *point* is a unit of measure which is approximately 1/72 of an inch. A definition of *point size* is more difficult. Though point size is a measure of character height in points, characters from different typefaces but having the same point size may be of different heights. (See Fig. 4.)

In practice, the physical size of a character depends on point size, typeface and other factors.

Sometimes text is *set solid;* that is, the vertical distance from a given line to the line which follows is equal to the point size. Text is said to be leaded (pronounced leded) if space is added between lines. The amount of leading is determined by the style specification (Fig. 5).

Book design also determines the overall page size and layout. The body (or reading matter) of a page may be arranged in one or more columns. The width and depth of each column and its location on the page must be specified. Rules must be defined for handling figures, illustrations and tables. Treatment of running heads must be specified for left-hand (even-numbered) pages and right-hand (odd-numbered) pages. Folios (page numbers) may be handled specially or may be included in the running heads. Treatment of footnotes must specify the location of the footnote relative to body text, the typeface, point size and leading, the prescribed method for handling footnotes which carry over to a following page, and many other factors.

How not to set type

The elements of book design mentioned above represent only a few of what might be called "do's" for the typesetter. Some of the "dont's" may not be quite so obvious, but what one doesn't see in a book contributes in large part to the quality of the book.

For example, one "don't" prohibits using interline leading below the last line in a column. This might seem to be a trivial detail. However, the effect of breaking this rule would be to obscure the position of the bottom of the column and this is an important visual boundary.

Consider an example in two-column work where extract text is set at the bottom of one of the columns (Fig. 6). Extract text is material which is quoted from another source. It is often set in a smaller point size and sometimes with less leading than the main body of text.

The last lines of the columns do not align because of the difference in leading below the last lines. Because it is a "don't," this is an example of what one doesn't see in a book.

Another "don't" relates to justification of footnote text. The pertinent typesetting convention does *not* permit the spaces between footnotes to be modified when the line to be justified contains text from two or more footnotes. All other spaces are involved in the justification process in the normal manner. Clearly, this rule is alien to

This example represents the bottom of a page which is set in two columns. Extract text appears at the bottom of the first column and continues to the top of the second column (which is not shown). The return to primary text would occur someplace within the second column. Primary text is set in a larger point size and with more leading. Note that the leading associated with each kind of text is included below the last line of

Fig. 6—The last lines of the column don't align because they are leaded differently.

the usual method of justification in which all interword spaces are adjusted. However, the normal justification technique will still be required when there are not "two or more" footnotes in one line. Fig. 7 illustrates lines justified by both techniques.

It was previously mentioned that hyphenation is employed to avoid setting loose lines. However, there is another typesetting "don't" which may prevent the use of hyphenation: three consecutive lines may not end with hyphens. Because enforcement of this rule would sometimes result in excessively loose lines, it may be modified for certain classes of work. For example, in very narrow columns where good spacing is especially difficult to achieve it may be permissible to hyphenate three consecutive lines, but not four, as a normal occurrence. In particularly difficult cases, the rule may be ignored altogether. This is an excellent example of a modifiable rule which may vary among typesetters, among typesetting jobs, or even within a job.

Typesetters avoid setting the last (usually short) line of a paragraph at the top of a column or page. This is one of several conditions which are termed *widows*. Sometimes the short line itself is called a widow. Other widow rules may require that the last line of the paragraph be preceded by at least *two* full lines in the column. In some cases, the first (indented) line of a paragraph is not permitted to end a column or page. Another related restriction prohibits a widow line of only one word, no matter where it occurs on the page.

Returning to the first classification, consider three alternatives which avoid leaving a widow on the first line of a page.

1) Recompose the previous page, making small changes to the spacing parameters, until at least one paragraph on the page becomes a line shorter or longer.
2) Add the widow line to the bottom of the previous page.
3) Shorten the previous page by one line and move the displaced line ahead of the widow.

The first solution often requires more effort than the others and may result in badly spaced text. This cure may be worse than the disease. In other cases, the revised spacing may be acceptable. Nevertheless, this treatment cannot always be relied upon to provide a quality solution.

The last two solutions require changing the number of lines on a page. Though not always true, we will assume that the design specification permits such a change. However, it is almost always required that facing pages are composed to the same depth. Thus, when moving lines to avoid a widow which would otherwise occur at the top of a left hand page, at least the preceding two pages are affected. In adjusting the makeup of these pages one naturally runs the risk of creating new widows. Often, these adjustments will ripple backward for several pages.

A simpler solution lies in either approach 2) or 3) in combination with vertical justification. It is sometimes acceptable to change the number of lines on a page and the vertical distance between lines if the distance from the top line to the bottom line can be maintained. Thus, on a page of thirty-nine lines spaced 12 points apart (about 6½ inches deep) a decrease of 2½% in the vertical spacing (from 12 to 11.7 points) will provide room for one additional line. Note that the 3/10 of a point adjustment per line is a movement of only 0.004 of an inch!

However, vertical justification is difficult to achieve with certain typesetting equipment and is not always accepted even when justification can be achieved easily. In multiple-column work, where solutions to the widow problem are especially difficult because columns are narrower, vertical justification is often prohibited. Designers often argue that lines in adjacent columns should be aligned. In the final analysis, the best solution may prescribe that one or more rules be bent or broken.

1. Footnote one. 2. Footnote two. 3. Footnote three. 4. Footnote number four requires more than one full line, and is justified as usual.

Fig. 7—Footnote justification.

Conclusion

The topics touched upon above represent only a small sample of the many typesetting considerations which could be examined. The typesetting requirements relating to only one dimension —horizontal justification and word hyphenation—involve a vast number of rules and conventions. The two-dimensional aspect of page makeup involves many additional practices. The combination is a complex composite of interacting and sometimes contradictory regulations. This large variety of rules and exceptions and the abundance of conflicts between rules give evidence that "there is more to typesetting than setting type."

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Central computer system—a manufacturing cost saver

S. V. Cianfrone

The Central Computer System (CCS) has been designed and implemented at the RCA Computer Systems plant in Palm Beach Gardens. Built around the RCA 1600 computer, CCS provides a common data base for testing computer units. The advantage of a common-data-base system over the multiple-data-base system previously in use are explained, and the management benefits (among them, measurable cost savings, better control, updated status data) are highlighted. Although the system is presently being used to test central processor units, its superior operating characteristics make the CCS equally effective in testing peripherals.

Author, Silvio Cianfrone (left) and project analyst G. E. Naramour discuss CCS program listing.

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began his data processing career in 1960 with the Scientific Applications Group at Pratt & Whitney Aircraft in West Palm Beach, Fla. where he developed a program to predict afterburner performance and blowout margins on a high-performance military engine. He participated in the design and development of a mathematical model used to predict theoretical performance over the complete spectrum of turbojet engine operating conditions. Mr. Cianfrone joined RCA in 1964 as a systems analyst at Palm Beach Gardens. His first assignment was to design and develop engineering design checks for the newly announced Spectra computer product line. He was subsequently promoted to Leader, Test Programming, with responsibility for field and factory test routines for the 301, 3301, and the Spectra 70/15 and 70/25 systems. More recently Mr. Cianfrone's group has undertaken the development of engineering design checks and factory tests for new systems developed at PBG as well as total responsibility for all 1600 software. His latest assignment has been the design and development of the Central Computer System.

A CENTRAL COMPUTER SYSTEM (CCS) was designed to provide the Palm Beach plant with a common data base of test programs for checking computer subsystems, such as central processing units and peripheral devices.

Before CCS was implemented, test routines were provided via magnetic tape equipment located at each test bay. This involved a multiple data base, relatively slow access, tape-equipment maintenance, and considerable dollar investment in equipment and floor space. The CCS provides a common data base of all test routines, revision level control, lower maintenance costs, and faster access. Test-bay status is printed on-line and recorded on magnetic tape for subsequent data reduction.

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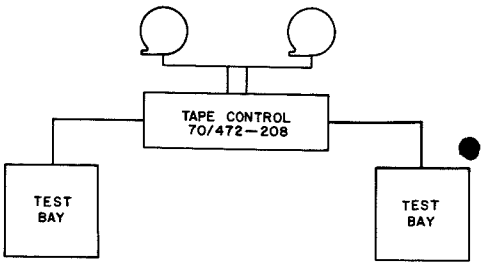

Fig. 2—Tape hardware required to support two test bays.

Hardware

The CCS (Fig. 1) consists of:

RCA 1600 Processor 65k bytes
Tape control (MT-9)
4 Magnetic tape drives
Disc control
2 Disc drives
Typewriter control (TYCE)
Console typewriter
Standard interface control electronics (SICE)
High-speed printer
Time control
23 Data exchange controllers (DXC)

The system is capable of storing 15,000,000 bytes of high-speed-access data and 60,000,000 bytes of low-speed-access data. The CCS will support testing of any combination of the following computers:

70/35	70/55	RCA 2
70/45I	70/60	RCA 3
70/45II	70/61	RCA 6
70/46		RCA 7

In addition, the CCS will support testing of all Spectra peripherals on any of these processors.

Cost savings

Fig. 2 represents a typical tape equipment configuration required to sup-

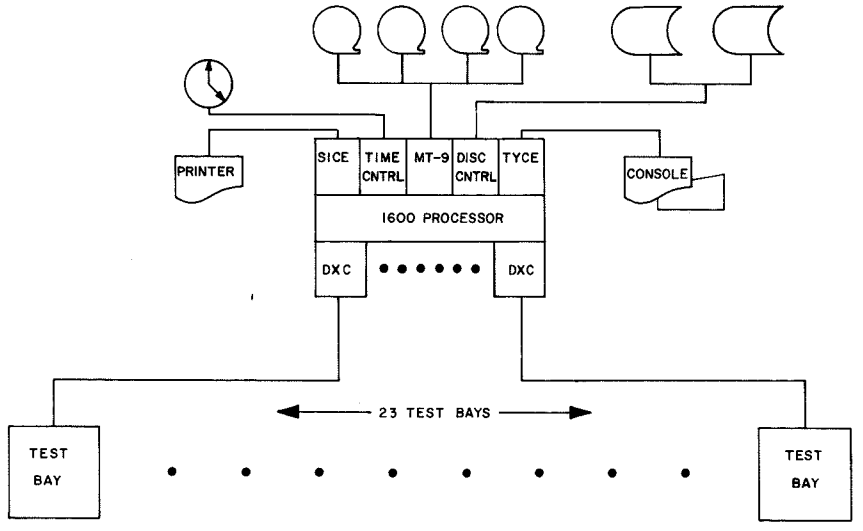

Fig. 1—CCS Hardware.

port two test bays. The support (seed) equipment consists of a 70/472-208 tape controller and a 70/442-2 tape drive. Supporting the two bays with tape equipment costs $135,930.

The basic cost of the ccs is $276,465 with an incremental cost of $3,780 for each test bay supported, plus $6,770 for each expansion rack required. Where the real economies of the ccs begin is shown in Fig. 3 which compares the cost per test bay for tape equipment vs. a ccs; ccs cost savings begin at about six test bays. When 23 test bays are supported, the savings amount to $1,186,250; at 30 bays, over $1,600,000.

Maintenance costs

Maintenance cost of test equipment is directly proportional to the complexity of the equipment. The elimination of tape equipment from the test bays reduces maintenance costs and increases reliability. A tape controller containing some 400 plug-ins is replaced by a DXC with only 40. The tape station—an electromechanical device requiring adjustments, cleaning, and other maintenance—is eliminated.

Fig. 4 compares annual field maintenance costs for tape equipment vs. those for the ccs. Cost savings for ccs start at about six test bays.

More than $5,400 per year can be saved using 1/10 of standard field maintenance charges as a basis. Since the system life is planned for eight years, the saving is over $43,000; this brings the total savings thus far to $1,229,250. Moreover, software written for the ccs dynamically reconfigures as hardware errors occur, and provides continued service even though a device (such as the printer, disc, DXC, or tape station) may be inoperative.

Increased throughput

The access and availability of the ccs, as opposed to magnetic tape, saves a minimum of 4 hours for each unit tested.

Approximately 16 units can be tested in a given test bay per year. Therefore, one bay represents a savings of 64 hours per year or about $89,200 for the 23 bays over the projected life of

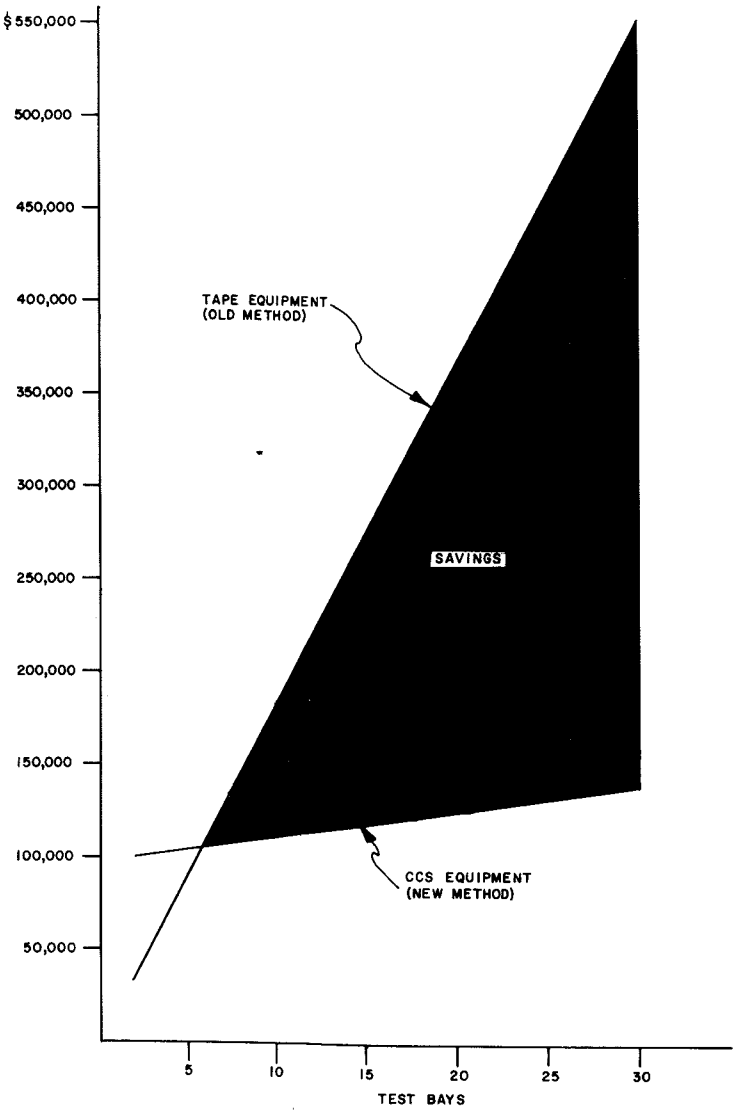

Fig. 3—Cost comparison per test bay, tape equipment vs. CCS equipment.

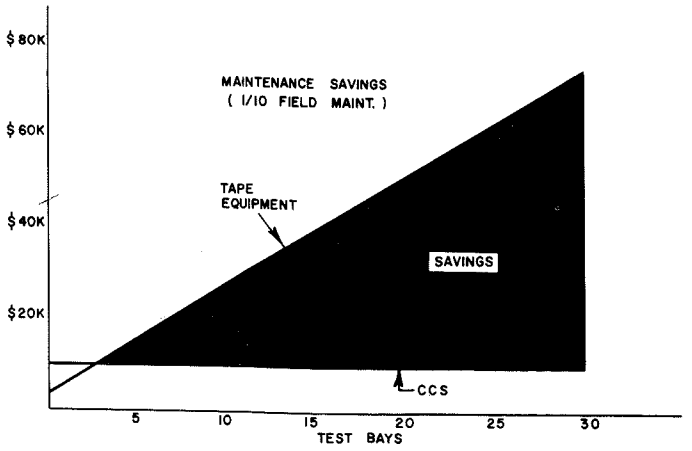

Fig. 4—Field maintenance costs—CCS vs. tape equipment.

the system. This raises the total savings to $1,318,450.

Floor space

Floor space in the manufacturing environment represents critical dollars. The CCS begins to save space (Fig. 5) as the test bays approach five positions.

Besides floor space, each tape controller requires power drops. In contrast, the DXC's draw their power from the 1600 Central Processing Unit and the 1600 expansion racks.

Operational characteristics

The response time to service a request from a test bay averages 0.115 second. Theoretical worst-case response time for 23 bays would be a maximum of 2.65 seconds. Data gathering over a period of 14 weeks indicates that this "worst-case condition" (2.65 seconds) would happen only once every two years.

The best case for tape operation is approximately 0.216 second and worst case approaches 15.20 seconds. Additional delays incurred by tape operation, but not experienced in the CCS approach, are:

1) Locating the appropriate tape (5 min.);
2) Mounting tape on tape device (1 min.);
3) Rewind time when reloading is required (18 sec.);
4) Tape errors—mechanical failures, as well as media failures; and
5) Sharing of tape controllers by two bays.

The 70/442-2 tape drive operates at a data transfer rate of 60,000 bytes/sec. The DXC, on the other hand, operates at a variable data rate depending on the type of processor and input/output channel utilized. This variable data rate provides a more comprehensive check of I/O channels, since data transfers may approach 330,000 bytes/sec.

With tape equipment, software must search the tape for a specific program and provide tape-error recovery routines. These features (search and recovery) require more hard core logic in the processor under test than in the case of a DXC. ("Hard core" is that logic which must be operative to accomplish the loading and execution of test routines.) For instance, using tape the following functions are performed to load a specific design check on an RCA 2:

1) The tape is unwound 2 tape marks.
2) A read-tape command is issued.
3) Status bytes are checked for read errors and recovery performed if errors occurred.
4) Data are compared to determine if the requested program has been located.
5) Steps 2), 3), and 4) are repeated up to 100 times until the requested program is located.

The burden of search and recovery is placed on the CCS which is fully operational and tested. In the case of the DXC, identification of the desired program is sent to the 1600 (via the DXC). Only one write and read command need be executed by the processor under test.

Software characteristics

The software developed for the CCS utilizes the Input/Output Driver System (IODS) developed in Palm Beach Gardens. The software (Fig. 6) consists of DXC-EXECUTIVE, DISC-MODULE, and STATUS-LOGGING routines.

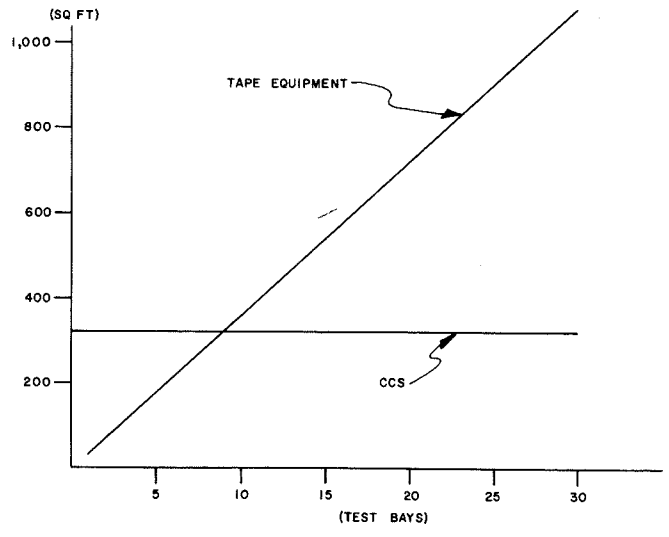

Fig. 5—Floor space requirements—CCS vs. tape equipment.

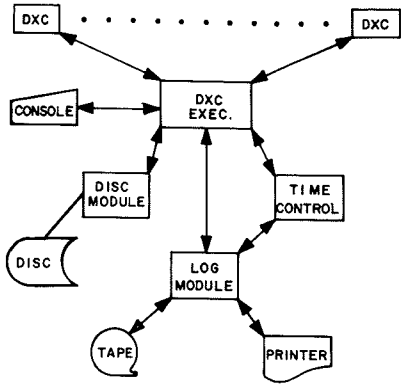

Fig. 6—CCS software.

The DXC EXECUTIVE scans the interrupt line of each DXC to determine if any test bay requires servicing. The service may consist of the following:

Case 1) The tester has requested a program from the disc.
Case 2) A status message has been received from the test bay.
Case 3) The tester has requested a data block from the SSK tape. (SSK is a magnetic tape of snapshot constants used to validate Read Only Memory.)

Case 1

If a program is requested from the disc, the request is first "time stamped," then logged to tape as statistical information. Control is then given to the DISC MODULE. The DISC MODULE uses a directory cylinder to search for the program on the disc. After the requested program has been located, control is returned to the DXC EXECUTIVE. The DXC EXECUTIVE then transfers the desired program to the appropriate test bay and continues scanning (Fig. 7).

Case 2

If a status message is received from the test bay, it is "time stamped" and logged to tape as statistical information; the DXC EXECUTIVE continues scanning.

Case 3

If a data block is requested from the SSK tape, the request is "time stamped" and logged to tape as statistical information. Control is then given to the Tape Module which performs the desired tape operation.

After the requested tape operation has been completed, control is returned to the DXC EXECUTIVE. The DXC EXECUTIVE then provides the test bay with either the desired data or an indication that the tape operation was successfully completed.

The CCS software provides automatic on-line data gathering of:

1) The number of requests made by each test bay, totaled and displayed every half hour.
2) All CCS transactions (including test bay, date, time of day, device type, serial number of test device, and nature of the transaction) in a permanent log on magnetic tape.
3) System status and failures—recoverable and unrecoverable errors.
4) Unused computer potential of the CCS displayed every 30 minutes.

The data can be used to spot trends for planning and scheduling:

1) Preventive maintenance periods,
2) Expansion to additional bays,
3) Addition of new functions, or
4) Monitor peak loading.

The remaining information gathered can provide:

1) Average test time per device type
2) Average run time by tests performed

The software system provides for automatic start-up from power failures and for normal restarts following preventive maintenance periods by continually updating the status of the system on disc. System restart restores the system status by retrieving the disc status record. The status record identifies equipments presently logged on the system: the device type, serial number, and test bay.

Significantly, the software system functions around-the-clock and unattended. Periodic status reports are automatically displayed on the console typewriter. System failures, such as a faulty DXC, are flagged and displayed on the console; processing continues on the remaining operable DXC's without operator intervention.

All of the programs required to test Spectra 70/35, 45, 46, 60 and 61 processors; Spectra peripherals; and RCA 2, 3, 6, 7 Series processors are stored on-line via a 70/564 disc drive. This method of storing the text routines provides one common data base for all test bays serviced by the CCS. As new test routines are developed, they are added to the CCS, and all test bays

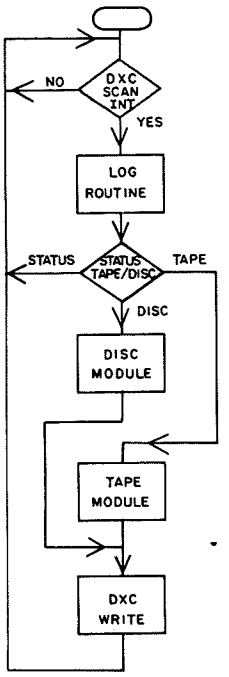

Fig. 7—Processing flow for cases 1), 2), and 3).

have immediate access to them. Previously, new test routines were supplied via magnetic tape, requiring the distribution of multiple reels and presenting revision-level control problems.

General-purpose off-line routines were developed for the RCA 1600 to provide the most efficient disc storage, with multiple program libraries compressed on a single disc. Since access time is critical, a trade-off had to be reached which would optimize both disc storage and access time while providing minimal head switching. The solution was to use a "dictionary-page track system" recorded on cylinder 101. The more frequently used routines were recorded alternately on either side of the dictionary cylinder followed by those less frequently used. Sector 19 of every track was left blank to facilitate head switching when handling multi-record files. The result, in practice, is an average access and retrieval time less than 1/10 of a second. Future plans for the CCS call for the capability to provide actual test stimuli and monitor responses directly or through a remote 1600.

Test Engineering has been designing a Computer Controlled Tester (C^2T) which will, in conjunction with special software, provide the means to test new systems as they are developed. These C^2T testers will interface between the 1600 processors and the equipment under test and will allow testing without the old problem of hard core failures.

The C^2R complex will enable the operator to communicate with an operable system. In the past, a considerable amount of hard core logic was required in the system under test to provide operator communication with various test program options. With the C^2T concept, control of the test program will reside in the 1600, not in the system under test—a substantial saving in the hard core logic required for program execution, operator communication, and modular testing.

The C^2T is intended to test units during the subassembly phase of manufacturing. Sub-modules, such as memory systems and power supplies, will be tested at the module level. This will facilitate failure detection prior to systems-level testing where corrections become more costly.

Other plans for the CCS include gathering failure data and producing subsequent failure analysis reports, and expanding the management information capability.

Summary

The CCS will save RCA over $1,000,000 over the next eight years in tangible costs alone. In intangible savings, the system provides a better and more professional means for Manufacturing to test and deliver a quality product faster and with lower manufacturing overhead.

Acknowledgments

The author thanks L. D. Osborne for his assistance in calculating data pertaining to cost saving estimates. Participating directly on the project were G. E. Naramor, J. P. Maguffey, and R. L. Magers. Appreciation is due to them also. All are members of Systems Manufacturing at the RCA Palm Beach Gardens plant.

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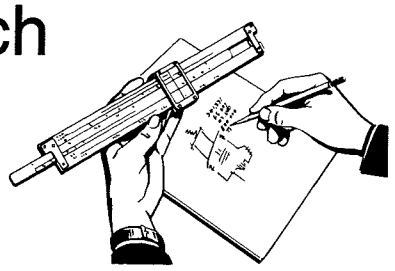

Single-transistor regulated fluorescent inverter

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In a typical single-transistor ringing choke inverter, the peak operating current is directly related to the Beta parameter, of the transistor and the supply voltage. In automotive applications where a 12 volt supply is available, it may be anticipated that the supply voltage will vary between 11 and 15 volts. The circuit disclosed provides for the operation of a fluorescent lamp from a 12-volt automobile battery by the use of a single transistor inverter, where the Beta of the transistor may also vary over a wide range.

In Figure 1, a standard 15-watt fluorescent lamp L is powered from a 12-V battery through a modified ringing-choke circuit which utilizes the positive temperature coefficient of resistance of the lamp filament of the fluorescent tube for regulation purposes.

The drive for transistor Q_1 is supplied through capacitor C_2. The voltage level stored by capacitor C_2 is controlled by the value of the resistance of the lower filament of the lamp, which is typically 3 or 4 ohms when hot. Resistor R_2 is in parallel with the resistance of the filament, and is used to set the proper operating point for the lamp.

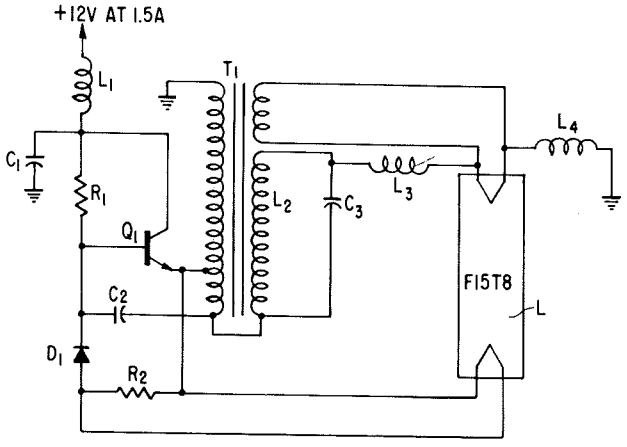

Fig. 1—Single transistor fluorescent inverter.

Reprint RE-17-4-24 | Final manuscript received June 21, 1971.

When the power to the lamp increases, the temperature of the filament will rise and hence the resistance of the filament will increase thereby reducing the drive to transistor Q_1. In this manner, the circuit provides regulated operation of the lamp for Beta variations of three-to-one and for supply voltages from 11 to 15 volts.

Capacitor C_1 and inductor L_1 provide a line filter for the circuit, and resistor R_1 provides a small forward bias to start the circuit operation. Diode D_1 is provided to avoid having the filament short circuit this small forward bias during startup.

Capacitor C_3 and roughly 500 turns of the secondary of transformer T_1, L_2, provide a tuned circuit at a frequency of 25kHz. Inductor L_3 provides a ballast for the lamp. Inductor L_4, provides some loading for the inverter during warm up to avoid extreme frequency variations of the inverter from initial start-up to the normal operating condition.

Measuring input impedance of ECL devices

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Computer Systems
Palm Beach Gardens, Fla.

Fig. 1—Author Ron Au at test setup.

Input impedance (Z_{in}) of an emitter-coupled logic (ECL) device is readily measured using a vector voltmeter. The technique described here saves time, is repeatable, and provides a hard-copy plot of test results. The technique is also applicable to impedance measurements of other active nonlinear devices and passive devices.

The real part of Z_{in} *must be positive* (≥ 0 ohms) to avoid oscillations since the equivalent circuit of the ECL device is an oscillator. From the readings obtained, Z_{in} is calculated and plotted on a teletype keyboard, using RCA's Basic Time Sharing System (BTSS).

Z_{in} is calculated by measuring the phase angle (θ_p) between the incident (channel A) and the reflected (channel B) waves, using the equation:

Reprint RE-17-4-24 | Final manuscript received June 7, 1971.

$$Z_{in}=Z_o(1+p')/(1-p') \quad (1)$$

where the reflection coefficient, p', is

$$p'=(E_{reflected}/E_{incident})\underline{/\theta_p}$$
$$=p\underline{/\theta_p}=B/A\underline{/\theta_p}$$

Substituting p' into Eq. 1,

$$Z_{in}=Z_o[(1-|p|^2)/(1+|p|^2-2|p|\cos\theta)$$
$$+j(2|p|\sin\theta)/(1+|p|^2-2|p|\cos\theta)] \quad (2)$$

so

$$R_{real}=Z_o(1-|p|^2)/(1+|p|^2-2|p|\cos\theta)$$
$$X_{complex}=Z_o(2|p|\sin\theta)/(1+|p|^2-2|p|\cos\theta)$$

These measurements were made using the test setup shown in Fig. 1 and the following Hewlett-Packard equipment:

Model 8405A	Vector Voltmeter
" 8745A	S-parameter Test Set
" 11600B	Transistor Fixture
" 8717A	Transistor Bias Supply
" 3200B	VHF Oscillator

To provide the readings necessary for computing the impedance, the test setup must be calibrated with a good short as follows:

1) Insert the short, supplied with the accessory kit, into Transistor Fixture ports A and B.
2) On the S-parameter Test Set, press buttons A-Input Port and S22-S parameter.
3) On the Oscillator, adjust the RMS volts and the frequency desired until the Vector Voltmeter voltage scale indicates 10 mV (Channel in the A or Reference position). Channel B (Test) should indicate 10 mV, so that $p=B/A=1$.
4) On the S-parameter Test Set, adjust the line stretcher until the Vector Voltmeter phase meter indicates $-180°$. Now $p'=p\underline{/\theta_p}=1\underline{/-180°}$.
5) Remove the short and insert the ECL device into the Transistor Fixture (see Fig. 2). Then connect
   a) Ground pin into ground
   b) Vee pin into port A
   c) Z_{in} pin into port B
6) Adjust the Transistor Bias Supply as follows:
   a) Transistor to Bipolar
   b) Type to npn
   c) Oper Config to CC (common collector)
   d) Lead Config to EBC
   e) V_{ce} ampl to indicate -5.00 volts
   f) I_e ampl for a V_{cb} voltage indication of $-.800$
7) Read the Vector Voltmeter with the ECL device in the Transistor Fixture for A, B, and phase angle. Now $p'=B/A\underline{/\theta_p}$.

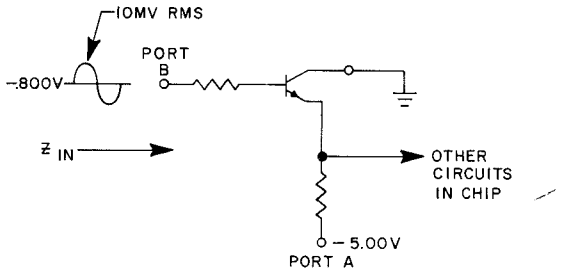


Fig. 2—Test circuit for ECL device.

With the measurements of A, B, and $\underline{/\theta_p}$ at the desired frequencies, type the data into the program (Fig. 3) to produce the results shown in the printout. In Fig. 3, Graph #3 shows a desired waveshape as the Z_{in} is positive from 100 to 250 MHz.

Acknowledgment: J. Griffin, A. A. Key, R. S. Singleton of the Palm Beach Product Laboratory, Systems Development Division, Computer Systems.

```
/DOT DEA

NUMBER OF SETS TO BE ENTERED = 4

NUMBER OF FREQUENCIES TO BE ENTERED= 5
TITLE= GRAPH #1
ENTER FREQ(MHZ),A(MV),B(MV),THETA(DEG)
FREQ(1,1)=100,19.5,21,-16.5
FREQ(2,1)=150,20.5,22.5,-36.5
FREQ(3,1)=175,4.5,5.3,-48
FREQ(4,1)=200,15.8,13.3,-54
FREQ(5,1)=250,12.9,5,-82

GRAPH #1

FREQ(MHZ)    RHO    THETA(DEG)   R(OHMS)    X(OHMS)

   100.00     1.08     -16.50     -84.43    -323.22

   150.00     1.10     -36.50     -23.25    -148.35

   175.00     1.18     -48.00     -23.87    -107.93

   200.00     0.34     -54.00      20.96     -94.47

   250.00     0.38     -82.00      40.76     -36.22

NUMBER OF FREQUENCIES TO BE ENTERED= 5
TITLE= GRAPH #2
ENTER FREQ(MHZ),A(MV),B(MV),THETA(DEG)
FREQ(1,2)=100,19.4,20.6,-17
FREQ(2,2)=150,20.5,22.2,-34
FREQ(3,2)=175,4.5,5,-45.3
FREQ(4,2)=200,16.3,14.5,-60.6
FREQ(5,2)=250,12.7,6,-80

GRAPH #2

FREQ(MHZ)    RHO    THETA(DEG)   R(OHMS)    X(OHMS)

   100.00     1.06     -17.00     -66.00    -321.31

   150.00     1.08     -34.00     -22.90    -160.56

   175.00     1.11     -45.30     -17.47    -117.62

   200.00     0.39     -60.60      11.37     -94.43

   250.00     0.47     -80.00      36.67     -43.93

NUMBER OF FREQUENCIES TO BE ENTERED= 5
TITLE= GRAPH #3
ENTER FREQ(MHZ),A(MV),B(MV),THETA(DEG)
FREQ(1,3)=100,16.3,18,-22
FREQ(2,3)=150,13.5,16.5,-38.5
FREQ(3,3)=175,4.9,3.9,-47.5
FREQ(4,3)=200,16.1,10.2,-55.5
FREQ(5,3)=250,13.8,5.3,-53.8

GRAPH #3

FREQ(MHZ)    RHO    THETA(DEG)   R(OHMS)    X(OHMS)

   100.00     0.98     -22.00      10.74    -256.79

   150.00     0.89     -38.50      25.60    -133.99

   175.00     0.30     -47.50      32.34    -105.15

   200.00     0.63     -55.50      43.79     -76.37

   250.00     0.38     -53.80      61.43     -44.67

NUMBER OF FREQUENCIES TO BE ENTERED= 5
TITLE= GRAPH #4
ENTER FREQ(MHZ),A(MV),B(MV),THETA(DEG)
FREQ(1,4)=100,16.2,20.2,-17
FREQ(2,4)=150,20,20.2,-35
FREQ(3,4)=175,4.6,4.3,-44
FREQ(4,4)=200,16.4,13.3,-58.5
FREQ(5,4)=250,13.2,5.9,-69

GRAPH #4

FREQ(MHZ)    RHO    THETA(DEG)   R(OHMS)    X(OHMS)

   100.00     1.05     -17.00     -56.46    -324.97

   150.00     1.04     -35.00     -18.80    -157.91

   175.00     1.04     -44.00      -7.56    -123.36

   200.00     0.81     -58.50      21.13     -85.34

   250.00     0.45     -69.00      45.50     -47.45

NUMBER OF SETS TO BE ENTERED = 0
STOP AFTER *650
READY
```

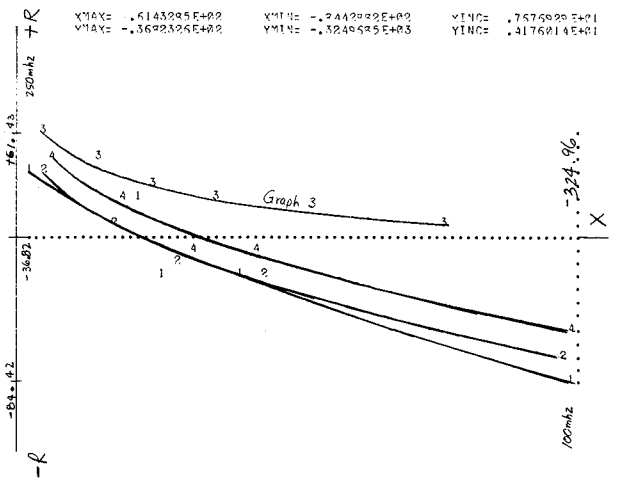
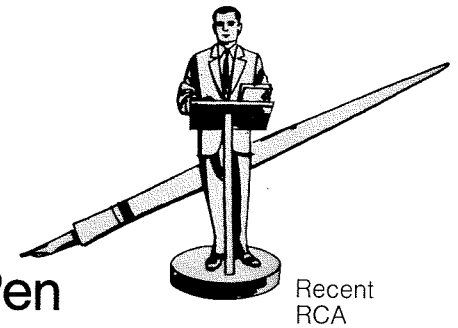


Fig. 3—Program inputs and outputs to calculate input impedance over the RCA Basic Time Sharing System.



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. . . design & chracteristics of lasers, components used with laser, electro-optical systems, lenses, etc. (excludes: masers)

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COMMUNICATION SYSTEM The Application of Solitons to a—K. Suzuki, K. Yoshikawa (Labs, Pr) Joint Mtg. of Electrical Institutes, Gifu Pref., Japan Oct. 14-15; 1971

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Astro-Electronics Division

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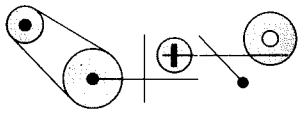

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Method of Branding Silicon Plastic Surface—J. R. Zuber, H. Foxman (EC, Hrsn) U.S. Pat. 3,617,326; November 2, 1971

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Date	Conference	Location	Sponsors	Deadline Date	Submit	To
MAY 15-17, 1972	**1972 Electronic Components Conference**	Statler-Hilton Hotel, Washington, D.C.	EIA, IEE	3-1-72	ms	Harold Sobol, Program Chairman ECC, RCA Corporation, David Sarnoff Research Center, Princeton, N.J. 08540
MAY 21-24, 1972	**IEEE Power Engineering Society Tech. Conf. on Underground Transmission**	Pittsburgh Hilton Hotel, Pittsburgh, Penna.	IEEE Power Engrg. Society	1-7-72	papers	E. D. Eich, Anaconda Wire & Cable Co., Hastings-on Hudson, N.Y. 10706
MAY 22-24, 1972	**IEEE G-MTT International Microwave Symposium**	The Arlington Park Towers Hotel, Chicago, Illinois	IEEE, G-MTT	1-7-72	sum & abst	Dr. Peter P. Toulios, Co-Chairman Technical Program Comm. IIT Research Institute 10 West 35th Street Chicago, IL 60616
JUNE 19-21, 1972	**International Conference on Communications**	Marriott Motor Hotel, Phila., Penna.	G-ComTech., Phila. Section	1-1-72	ms	A. W. Weinrich, App. Info. Ind., 345 New Albandy Rd., Moorestown, N.J. 08057
JUNE 26-28, 1972	**AIAA 5th Fluid and Plasma Dynamics Conference**	Boston, Mass.	AIAA	1-7-72	abst	Don Wendling, Director—Technical Programs, AIAA, 1290 Ave. of the Americas, New York, N.Y. 10019
JUNE 26-29, 1972	**Conference on Precision Electromagnetic Measurements**	Nat'l Bur. of Standards, Boulder, Colo.	G-IM, NBS, USNC/URSI	1-15-72	sum	H. S. Boyne, Radio Bldg., Rm. 4075, NBS, Boulder, Colo. 80302
JULY 4-6, 1972	**Conference on Radio Receivers and Associated Systems**	Univ. College of Swansea, South Wales	IERE, IEE, IEEE UKRI Section	11-19-71 2-18-72	syn ms	IERE, 8-9 Bedford Sq., London WC1B 3RG England
JULY 9-14, 1972	**IEEE Power Engineering Society Summer Meeting**	Fairmont Hotel, San Francisco, Calif.	IEEE Power Engineering Society	2-15-72	ms	W. R. Johnson, Pacific Gas & Elec. Co., 245 Market St., Rm. 1122, San Francisco, Calif. 94106
JULY 17-19, 1972	**AIAA/NAVY Advanced Marine Vehicles Meeting**	Annapolis, Md.	AIAA	12-weeks before meeting 6-weeks before meeting	abst ms	Don Wendling, Director—Technical Programs, AIAA, 1290 Ave. of the Americas, New York, N.Y. 10019
JULY 25-27, 1972	**1972 Conference on Advances in Marine Navigational Aids**	London, England	IEE, IN, IERE, UKRI Section of IEEE	11/71	syn (250-word)	Manager, Conference Department, IEE, Savoy Place, London WC2R OBL
AUG. 14-16, 1972	**AIAA Guidance and Control Conference**	Stanford, Calif.	AIAA	12-weeks before meeting 6-weeks before meeting)	abst ms	Don Wendling, Director—Technical Programs, AIAA, 1290 Ave. of the Americas, New York, N.Y. 10019
AUG. 21-26, 1972	**13th International Congress of Theoretical and Applied Mechanics**	Moscow, USSR		3-15-72	sum (5 copies) (500 words)	Professor G. F. Carrier, Pierce Hall, Harvard University, Cambridge, Mass. 02138
SEPT. 4-8, 1972	**International Broadcasting Convention**	Grosvenor House, London, England	IERE, IEE, IEEE UKRI Section et al	1-3-72	syn	The Secretariat, IBC IEE, Savoy Place, London W. C. 2R, OBL, England
SEPT. 10-14, 1972	**Jt. Power Generation Tech. Conference**	Sheraton Boston Hotel Boston, Mass.	IEEE Power Engrg. Soc., ASME, ASCE	4-28-72	ms	General Chairman: G. O. Buffington, Stone & Webster Corp., 225 Franklin St., Boston, Mass. 02107
SEPT. 26-29, 1972	**Conf. on Metering, Apparatus and Tariffs for Electricity Supply**	London, England	IEE, IERE, IEEE UKRI Section	3-24-72	syn	IEE, Savoy Place, London, W. C. 2R, OBL, England
JAN. 28-FEB. 2, 1973	**IEEE Power Engineering Society Winter Meeting**	Statler Hilton Hotel, New York, N.Y.	IEEE Power Engineering Society	9-15-72	ms	IEE Hdqs., 345 E. 47th St. New York, NY
JULY 15-20, 1973	**IEEE Power Engineering Society Summer Meeting**	Vancouver Hotel, Vancouver, B.C. Canada	IEE Power Engineering Society	2-15-73	ms	IEE Hdqs., 345 E. 47th St. New York, NY

Dates of upcoming meetings—plan ahead.

Date	Conference	Location	Sponsors	Program Chairman
FEB. 3, 1972		Pacific Grove, Calif.		Palo Alto, Calif. 94305
FEB. 8-10, 1972	**Aerospace & Elec. Sys. Winter Convention (WINCON)**	Biltmore Hotel, Los Angeles, Calif.	G-AES. L.A. Council	Gerry Goldenstern, L.A. Council Office, 3600 Wilshire Blvd., Los Angeles, Calif. 90010
FEB. 14-15, 1972	**Conference on the Psychology of Technical Communications**	Phila., Penna.	G-EWS	J. C. Phillips, RCA Bldg., 2-8, Front & Cooper Sts., Camden, N.J. 08102
FEB. 14-16, 1972	**AIAA Strategic Offensive/Defensive Missile Systems Meeting**	Monterey, Calif.	AIAA	AIAA, 1290 Ave. of the Americas, New York, N.Y. 10019
FEB. 16-18, 1972	**Int'l Solid State Circuits Conference**	Sheraton Hotel, Univ. of Penna., Phila., Penna.	SSC Council, Phila. Section. Univ. of Penna.	A. V. Brown, T. J. Watson Res. Ctr., Box 218, Yorktown Heights, N.Y. 10598
MARCH 1-3, 1972	**Scintillation & Semiconductor Counter Symposium**	Shoreham Hotel, Washington, D.C.	G-NS, USAEC, NBS	G. L. Miller, Bell Labs., Rm. ID-440, Murray Hill, N.J. 07974
MARCH 9-14, 1972	**Int'l Symposium on High Voltage Technology**	Munich, Germany	IEEE Power Engrg. Society, VDE	Int'l Symp. on High Voltage Tech. Hochspannungsinstitut TU Munchen 8 Munchen 2, ArcisstraBe 21 Germany
MARCH 15-17, 1972	**Zurich Integrated Sys. for Speech, Video & Data Communications**	Fed. Inst. of Tech., Zurich, Switzerland	G-AE, IEEE Computer Soc., Switzerland Sec., SEV et al	A. E. Bachmann, PTT Res. Lab., Speichergasse 6, CH-3000 Bern, Switzerland
MARCH 20-23, 1972	**IEEE INTERNATIONAL CONVENTION (INTERCON)**	Coliseum & N.Y. Hilton Hotel, New York, N.Y.	IEEE	J. H. Schumacher, IEEE Hdqs., 345 E. 47th St., New York, N.Y. 10017
MARCH 21-23, 1972	**Int'l Medium Voltage Earthing Practices**	Inst. of Elec. Engrs., London, England	IEEE, IEEE, UKRI Section et al	IEE Office, Savoy Place, London, W. C. 2R OBL Eng.
MARCH 27-28, 1972	**AIAA Man's Role in Space Conference**	Cocoa Beach, Fla.	AIAA	AIAA, 1290 Ave. of the Americas, New York, N.Y. 10019
MARCH 27-31, 1972	**2nd Symposium on Meteorological Observation and Instrumentation**	San Diego	AIAA	AIAA, 1290 Ave. of the Americas, New York, N.Y. 10019
APRIL 4-6, 1972	**Symp. on Computer-Communications Networks and Teletraffic**	New York. N.Y.	PIB, G-Com Tech., coop. of Computer Society	IEEE Hdqs., 345 E. 47th St., New York, N.Y. 10017
APRIL 10-12, 1972	**Int'l Symposium on Acoustical Holography**	Univ. of Calif., Santa Barbara, Calif.	G SU, Univ. of Calif.	Glen Wade, Univ. of Calif., Dept. of EE, Santa Barbara, California 93106
APRIL 10-12, 1972	**Region III Convention**	Univ. of Tenn., Knoxville, Tenn.	Region III, E. Tennessee	W. L. Green, Univ. of Tenn., Dept of EE, Knoxville, Tenn. 37916
APRIL 10-13, 1972	**Int'l Conference on Magnetics (INTERMAG)**	Kyoto Int'l Conf. Hall, Kyoto, Japan	G-MAG, Japanese Soc. for Promotion of Science et al	C. D. Mee, IBM Corp., Bldg. 015, Monterey & Cottle Rds., San Jose, Calif. 96115
APRIL 11-13, 1972	**Conf. on Industrial Measurement & Control by Radiation Techniques**	Univ. of Surrey, Guildford, Surrey, England	IEE, IERE, IPPS, IMC, IEEE UKRI Section et al	IEE Office, Savoy Place, London W. C. 2R OBL Eng.
APRIL 11-13, 1972	**Conference on Digital Processing of Signals in Communications**	Univ. of Tech., Loughborough, Leicestershire, England	IERE IEEE UKRI Section	Secretary, IERE, 8-9 Bedford Square, London, WC1B, England
APRIL 16-21, 1972	**11th SMPTE Technical Conference and Equipment Exhibit**	New York Hilton Hotel, New York, N.Y.	SMPTE	Society of Motion Picture and Television Engineers, 9 East 41st Street, New York, N.Y. 10017
APRIL 19-21, 1972	**International Symposium on Circuit Theory**	Sheraton-Universal Hotel, Universal City, Calif.	G-CT	G. C. Temes, Univ. of Calif., Dept. of Elec. Sci. & Engrg., Los Angeles, Calif. 90024
APRIL 19-21, 1972	**Region Six Conference**	Hilton Inn, San Diego, Calif.	Region Six	D. E. Atkinson, Pacific Tele., 525 B. St., Rm. 1458, Box 524, San Diego, Calif. 92112
APRIL 19-21, 1972	**Southwestern IEEE Conference & Exhibition (SWIEEECO)**	Baker Hotel & Dallas Mem. Aud., Dallas, Texas	SWIEEECO, Dallas Section	R. L. Carrel, Electrospace Sys. Inc., POB 1359, Richardson, Texas 75080
APRIL 24-26, 1972	**Int'l Conference on Speech Communications and Processing**	Kresge Aud., MIT Campus, Cambridge, Mass.	G-AE, AF Cambridge Res. Lab.	C. F. Teacher, Philco-Ford Corp., 3900 Welsh Rd., Willow Grove, PA 19090
APRIL 24-26, 1972	**Frontiers in Education**	Ramada Inn, Tucson, Arizona	G-Education Tucson Section, Univ. of Ariz.	G. R. Peterson, Dept. of EE, Univ. of Ariz., Tucson, Arizona 85721
APRIL 25-28, 1972	**Conference on Computer Aided Design**	Univ. of Southampton, Southampton, England	IEE, EEA, IEEE UKRI Section	IEE, Savoy Place, London WC2R OBL England
APRIL 30-MAY 3, 1972	**Offshore Technology Conference**	Astrohall, Houston, Texas	TAB Ocean. Coor. Comm. et al	Offshore Tech. Conf., 6200 N. Central Expressway, Dallas, Texas 75206
MAY 6-11, 1972	**Second Symposium on Advanced Materials: Insulation**	Sheraton-Park Hotel, Washington, DC	American Ceramic Society	Dr. Alan D. Miller, 325 Roberts Hall, Univ. of Washington, Seattle, Washington, 98195
MAY 7-10, 1972	**Int'l Semiconductor Power Converter Conference**	Baltimore Hilton Hotel, Baltimore, Maryland	G-IGA, Baltimore Section	S. P. Jackson, Jackson Assoc., 4663 Executive Dr., Columbus, Ohio 43220
MAY 7-11, 1972	**Int'l Quantum Electronics Conference**	Queen Elizabeth Hotel, Montreal, Quebec, Canada	G-ED, G-MTT, AIP, OSA	B. P. Stoicheff, University of Toronto, Toronto, Ontario, Canada
MAY 7-12, 1972	**SPSE Annual Conference**	San Francisco Hilton, San Francisco, Calif.	SPSE	Raymond A. Eynard, Public Relations Chairman, SPSE, P.O. Box 2001, Teterboro, N.J. 07608
MAY 15-18, 1972	**Spring Joint Computer Conference**	Convention Ctr., Atlantic City, New Jersey	IEEE Computer Soc., AFIPS	AFIPS Hdqs., 210 Summit Ave., Montvale, NJ 07645
MAY 21-24, 1972	**IEEE Power Engineering Society Tech. Conf. on Underground Transmission**	Pittsburgh Hilton Hotel, Pittsburgh, Penna.	IEEE Power Engrg. Society	E. D. Eich, Anaconda Wire & Cable Co., Hastings-on-Hudson, NY 10706
JUNE 21-23, 1972	**Joint Measurements Conference**	Nat'l Bur. of Standards, Boulder, Colo.	G-IM et al	P. K. Stein, Arizona State Univ., Tempe, Arizona 85281

Engineering News and Highlights

Schnapf named Fellow of AIAA

Abraham Schnapf, Manager of Program Management at the Astro-Electronics Division, Princeton, N.J., has been elected a Fellow of the American Institute of Aeronautics and Astronautics (AIAA).

Mr. Schnapf was cited for "important contributions to the technology of satellite weather forecasting, culminating in his management of the TIROS series of satellites."

With RCA since 1950, Mr. Schnapf has been associated with the meteorological satellite program since its inception in 1958 when he joined AED as Assistant Project Manager for TIROS. Two years later he became Manager of the program.

In 1970, under Mr. Schnapf's guidance, RCA introduced a new series of larger, more sophisticated meteorological spacecraft known as ITOS (Improved TIROS Operational Satellite). To date, the TIROS and ITOS series have returned more than 1,700,000 television pictures of the earth's weather for analysis and forecasting. (See *RCA Engineer,* Vol. 17, No. 1, June/July 1971, p. 32).

In his present post, Mr. Schnapf is responsible for the Atmosphere Explorer satellite program, subsystems development for the NIMBUS experimental meteorological spacecraft and the Earth Resources Technology subsystems, as well as the ITOS program.

Earlier this year Mr. Schnapf received the David Sarnoff Outstanding Achievement Award, RCA's highest technical honor. He also received the National Aeronautics and Space Administration's Public Service Award in 1969 and the American Society of Quality Control's annual award for systems performance in 1968.

Sperry Rand and RCA Reach Agreement in Principle

Sperry Rand Corporation and RCA, on November 19, announced they had reached an agreement in principle under which Sperry Rand's Univac Division will assume responsibility for RCA's existing general purpose computer customers in the United States, Canada, and Mexico. The agreement also involves maintenance and service agreements.

The announcement by **J. Frank Forster,** Sperry Rand's Chairman and Chief Executive Officer, and **Robert W. Sarnoff,** Chairman and Chief Executive Officer of RCA, stated they have set December 17, 1971 as the date for completing negotiations and execution of the final agreement. Once approved by both companies the anticipated closing date for the entire transaction is December 31, 1971.

Tentative terms of the agreement involve a payment of approximately $70 million by Sperry Rand on January 7, 1972 plus a varying percentage of future revenues over a five-year period. Current estimates are that the total value of these succeeding payments will amount to between $30 million and $60 million.

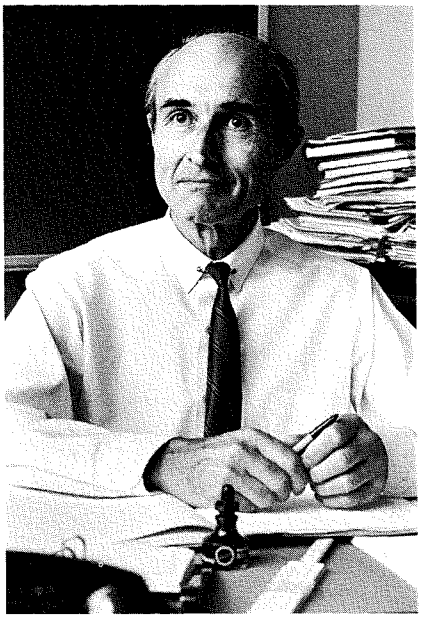
Both executives expressed confidence that the agreement would lead to a mutually beneficial relationship for the RCA customers and Univac. Speaking for RCA, Mr. Sarnoff said that RCA's computer customers could be assured of continued full utility from their RCA equipment, and in addition would benefit from Univac's vast experience, broad computer base, and worldwide marketing and service organization.

To assure continuing quality of service to RCA customers, some 2500 RCA computer personnel, including engineers, systems analysts, programmers, and sales representatives will be given an opportunity to join the Univac organization. Univac will also have access to certain existing RCA test and checkout facilities as well as to spare parts inventory necessary to service the RCA users.

As presently projected, Univac will assume by January 1, 1972, all of the specified RCA lease and maintenance commitments. This involves over 1000 installations and in excess of 500 customers, primarily in the United States.

Mr. Forster added that the agreement would allow Univac to increase its share of the computer market not only numerically, but in certain specific application areas where it is anxious to broaden its market share. These include state and local governments, manufacturing, and education, where the RCA installations are most heavily concentrated.

Univac today is a worldwide operation manufacturing a full range of computer systems. As the largest single division of Sperry Rand Corporation, Univac enjoys annual sales in the area of $700 million, and has been continually profitable since 1965. Total value of Univac computing systems installed worldwide at the end of 1970 was approximately $3.2 billion, to which acquisition of RCA systems is expected to add approximately $1 billion.



Ramberg to receive David Sarnoff Award

Dr. **Edward G. Ramberg** of the Physical Electronics Research Laboratory, RCA Laboratories, Princeton, N.J., will receive the 1972 David Sarnoff Award of the Institute of Electrical and Electronics Engineers (IEEE).

The David Sarnoff Award is presented annually by the IEEE for outstanding contributions to the field of electronics. Dr. Ramberg was cited "for outstanding contributions to electron physics, electron optics, and television."

Dr. Ramberg received the AB from Cornell University in 1928 and the PhD in theoretical physics from the University of Munich in 1932. After working on the theory of x-ray spectra as research assistant at Cornell, he joined the Electronic Research Laboratory of RCA in Camden in 1935. He has been associated with the RCA Laboratories in Princeton since their establishment in 1942. He has worked primarily on electron optics as applied to electron microscopy and television, various phases of physical electronics, thermoelectricity, and optics. In 1949, he was visiting professor in physics at the University of Munich and, in 1960 and 1961, Fulbright Lecturer at the Technische Hochschule, Darmstadt. Dr. Ramberg is a Fellow of the IEEE and the APS and a member of Sigma Xi and the Electron Microscope Society of America.

Staff Announcements

Marketing

James J. Johnson, Vice President, Marketing has announced his organization as follows: **Martin F. Bennett,** Vice President, Distributor and Commercial Relations. [In this capacity, Mr. Bennett will continue his present responsibilities for Distributor and Commercial Relations activities.] **Robert C. Bitting,** Staff Vice President, SelectaVision, Business Development. **Joseph W. Curran,** Staff Vice President, Marketing Services. [In this capacity, Mr. Curran will continue his present responsibilities for Corporate Advertising, Corporate Identification and Exhibits, Sales Promotion, and Media Services and Controls. In addition, Mr. Curran will assume Product and Marketing Planning staff responsibility for the following organization units: Hertz Corp., RCA Service Company, and Parts and Accessories.]. **Donald P. Dickson,** Staff Vice President, Special Marketing Projects. **Robert J. Eggert,** Staff Vice President, Economic and Marketing Research. [In this capacity, Mr. Eggert will continue his present responsibilities for Economic and Marketing Research activities. In addition, Mr. Eggert will assume Product and Marketing Planning staff responsibility for the following organization units: Banquet Foods Corp., Random House, Inc., Coronet Industries, Inc., Cushman and Wakefield, Inc., and Education Systems.] **Joseph R. Hogan,** Director, Marketing—Europe, Middle East and Africa Region, RCA International, Ltd. **Edward J. Homer,** Manager, Marketing Administration; **James J. Johnson,** Acting, Consumer Marketing. [In this acting capacity, Mr. Johnson will assume Product and Marketing Planning staff responsibility for the following organization units: Consumer Electronics, RCA Records, and Electronic Components.] **Thomas J. McDermott,** Staff Vice President, SelectaVision Special Projects. **Richard W. Sonnenfeldt,** Staff Vice President, Systems Marketing and Development. [In this capacity, Mr. Sonnenfeldt will continue his present responsibilities for Systems Development and State Liaison. He will also assume responsibility for Consumer Information Systems, and in addition, Mr. Sonnenfeldt will assume Product and Marketing Planning staff responsibility for the following organization units: Government and Commercial Systems, RCA Global Communications, Inc., Solid State Division, and Computer Systems.]

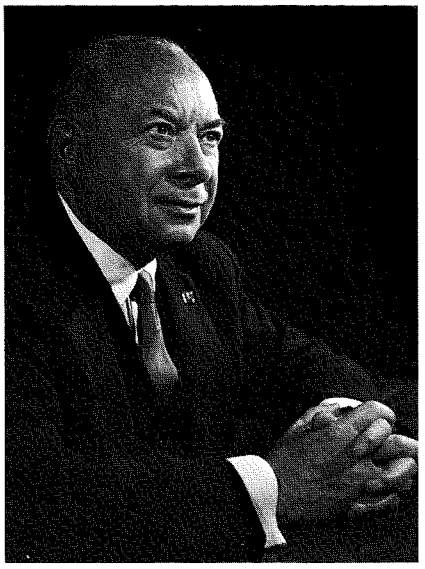
Research and Engineering
Finance and Administrative Services

John F. Biewener, Director, Finance and Administrative Services has announced the Finance and Administrative Services organization as follows: **Vincent M. Bartholomew,** Manager, Graphics Services; **Craig Havemeyer,** Manager, Management Information Systems; **Erick M. James,** Manager, Facilities; **Carl E. Kurlander,** Manager, Materials; **Jerome Kurshan, Manager,** Marketing; **Donald J. McCarty, Jr.,** Manager, Accounting; and **Ralph H. Myers,** Manager, Financial and Capital Planning.

RCA Laboratories

William M. Webster, Vice President, Laboratories has announced the organization as follows: **George D. Cody,** Director, Physical Electronics Research Laboratory; **Nathan L. Gordon,** Director, Systems Research Laboratory; **Gerald B. Herzog,** Director, Solid State Technology Center; **Joseph H. Scott, Jr.,** Head, Integrated Circuit Technology and Applications; **Donald S. McCoy,** Director, Consumer Electronics Research Laboratory; **Kerns H. Powers,** Director, Consumer Electronics Research Laboratory; **Jan A. Rajchman,** Staff Vice President, Information Sciences; **Paul Rappaport,** Director, Process and Applied Materials Research Laboratory; **James J. Tietjen,** Director, Materials Research Laboratory; **Charles A. Hurford,** Manager, Industrial Relations and **Richard E. Quinn,** Manager, Technical Services.

David Sarnoff is dead



David Sarnoff, Honorary Chairman of RCA and one of the dominant figures in the world of communications for more than 50 years, died December 12, 1971 at 11:50 a.m. in his home in New York City after a lengthy illness. He was 80 years old. Born on February 27, 1891, in the small village of Uzlian, near the city of Minsk, Russia, he was brought to the United States by his parents in 1900.

General Sarnoff is survived by his wife Lizette (nee Hermant); three sons—Robert W. Sarnoff, of New York, Chairman of RCA; Edward Sarnoff, of New York, Chairman of the Board, Fleet Services, Inc., and Thomas W. Sarnoff, of Beverly Hills, Calif., Staff Executive Vice President, West Coast, of the National Broadcasting Co. Also surviving are two brothers Morris Sarnoff of Hollywood, Fla. and Lew Sarnoff of New York; a sister, Mrs. Herbert (Ede) Baer of Beverly Hills, Calif., and nine grandchildren.

As a young wireless operator at the Marconi station atop Wanamaker's store in New York, General Sarnoff and wireless were thrust before the attention of the United States and the world. On the night of April 12, 1912, Sarnoff was on duty when the S. S. Titanic, enroute to New York on her maiden voyage, struck an iceberg and sank with the loss of 1,517 lives. The young telegrapher picked up the message reporting the Titanic's distress signal and promptly made the news available to the world. From the rescue ship, Carpathia, he received a list of survivors and other important messages related to the disaster. He remained on duty continuously for 72 hours, during which time President William Howard Taft ordered every other wireless station along the East Coast to maintain silence to prevent interference.

The Titanic disaster focused world-wide attention on the potential of radio and as the new medium advanced, so did Sarnoff. In 1915, he wrote a famous memorandum proposing a "radio music box" that would receive programs broadcast for public information and entertainment. His memo read in part, "I have in mind a plan of development which would make radio a household utility in the same sense as a piano or phonograph. The idea is to bring music to the home by wireless."

In 1919, when Radio Corporation of America was formed at the request of the U.S. Government, Sarnoff was named Commercial Manager of the new company. He became General Manager in 1921 and Vice President the following year. As early as April 3, 1923, Sarnoff foresaw the possibility of television as a parallel service of radio broadcasting. In a report, he wrote, "I believe that television, which is the technical name for seeing as well as hearing by radio, will come to pass in due course . . . It may be that every broadcast receiver for home use will be equipped with a television adjunct by which the instrument will make it possible for those at home to see as well as hear what is going on at the broadcast station."

In 1926, Sarnoff organized the National Broadcasting Company as a subsidiary of RCA, "to provide the best programs available for broadcasting in the United States." This first national network did much to expand the usefulness and public interest in broadcasting.

General Sarnoff was elected President of RCA in 1930 and in 1947 was elected Chairman of the Board and Chief Executive Officer. In 1966, he relinquished the post of Chief Executive Officer, continuing to serve actively as Chairman. He retired, Dec. 31, 1969, at which time he was elected the company's first Honorary Chairman.

In addition to his scientific and industrial activities, General Sarnoff achieved wide recognition for his efforts in military communications, especially during World

War II. He served as special consultant on communications at Gen. Dwight D. Eisenhower's SHAEF headquarters in Europe and was promoted to the rank of Brigadier General on Dec. 6, 1944. He was decorated by both the U.S. and French governments.

He served on several special Presidential commissions, being Chairman of two. He was active in numerous civic and cultural organizations and received 27 honorary degrees from American colleges and universities. He also received scores of honors and awards from scientific, industrial, military, civic and cultural associations both here and abroad.

Promotions

Electronic Components

T. C. Loser, Jr. from Eng. Equip. Dev. to Eng. Ldr., Equip. Dev. (**W. R. Miller,** Lancaster)

K. D. Scearce from Eng. Prod. Dev. to Mgr., Interplant Support Equipment Eng. (**C. E. Shedd,** Lancaster)

R. A. Lambert from Eng. Equip. Dev. to Eng. Ldr., Equip. Dev. (**M. R. Weingarten,** Lancaster)

R S. Goldberger from Sr. Eng., Equip. Dev. to Eng. Ldr. Equip. Dev. (**K. D. Scearce,** Lancaster)

W. R. Menges from Eng. Product Dev. to Eng. Ldr. Product Dev. (**A. J. Torre,** Lancaster)

W. R. Miller from Adm., Equip. Eng. CPT to Mgr., Electrical Design and Development (**C. E. Shedd,** Lancaster)

Astro-Electronics Divisions

Larry P. Yermack from Mgr., Equip. Eng. to Mgr., NAVASAT Project (**C. H. Hume,** Hightstown)

Television Picture Tube Division

D. L. Roberts from Eng. Ldr., Mfg. to Mgr., Prod. Eng. (**N. Meena,** Marion)

Communications Systems Division

W. G. Herold from Ldr., Eng. Staff to Mgr., Minute Man Programs (**T. Sheridan,** Camden)

M. I. Stricker from Ldr., Eng. Staff to Mgr., Telex & Autodin Programs (**T. Sheridan,** Camden)

Note: In last issue's listing of "Promotions," the effective date of Mr. J. S. Griffin's promotion to Manager, Recording Equipment Projects, Government Communications Systems, should have been given; his promotion was effective December 5, 1969.

In the photo (left to right) are Dr. George H. Brown, Executive Vice President, Patents and Licensing; Henry Schantzer; Robert Williams; Charles Brodsky; Joseph Tripoli; and John Regan, Staff Vice President, Patent Operations. Carl Wright was not available when the photo was taken.

Five patent attorneys admitted to practice in N. J.

Charles I. Brodsky, Henry I. Schanzer, Joseph Tripoli, Robert P. Williams, and **Carl M. Wright** recently passed their New Jersey Bar examinations and have been admitted to practice law. All of the attorneys are members of Patent Operations, Princeton, N. J.

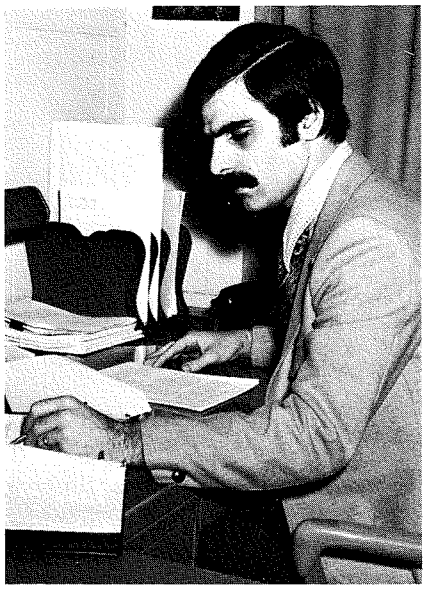
Charles I. Brodsky had previously been admitted to practice before the Courts of New York State, the U. S. Court of Customs and Patent Appeals, and the United States Patent Office. He received the BEE in 1960 and the MBA in 1966 from the City College of New York University. After working for the Hazeltine Corporation, Mr. Brodsky joined RCA's Patent Department in 1965. In 1969 he joined the law firm of Ostrolenk, Faber, Gerb, and Soffen—returning to RCA in August of 1970 as a Patent Counsel.

Henry I. Schanzer had previously been admitted to practice before the Courts of New York State and the United States Patent office. He received the BEE from the City College of New York in 1968, the MSEE from Columbia University in 1963, and the LLB from New York Law School in 1967. Mr. Schanzer was an Electronic Engineer with Bell Aircraft in 1958 and 1959, joining Fairchild Camera and Instruments as a Senior Electronics Engineer in 1959. He joined RCA in 1967 as a Patent Counsel in the Information Systems Group in residence at Solid State Division.

Joseph Tripoli received the Juris Doctorate from the Temple University School of Law on May 27, 1971. During his law school career, he received the Barenkopf Scholarship Award for the graduating senior in the Evening Division with the highest scholastic rank, the Joseph E. Gross Memorial Award for honors in Estates and Future Interests, and five American Jurisprudence Awards for honors in various courses. Mr. Tripoli joined the RCA Missile and Surface Radar Division in Moorestown as an electrical engineer in 1965, following his graduation from the City College of New York. In 1969 he transferred to Patent Operations at the David Sarnoff Research Center as a member of the Engineering Products group.

Robert P. Williams had previously been admitted to practice before the U. S. Patent Office, The Supreme Court of Minnesota, The Federal District of Minnesota, and the Eighth Circuit Court of Appeals. Mr. Williams received the Bachelor of Science in 1961 and the JD in 1965, both from American University. From 1963 to 1965, he was a Patent Adviser of the U. S. Naval Ordnance Laboratory. In 1965, he entered private practice in Minneapolis, Minnesota, joining RCA in 1966 as a Member of the Patent Staff. He was a Patent Counsel from 1967 to 1969, and has been Resident Patent Counsel at Somerville since 1969. Mr. Williams received the Lawyer's Cooperative Publishing Co. prizes for Property (1962) and Trade Regulation (1965).

Carl M. Wright received the BS in 1951 from the U.S. Merchant Marine Academy. He served in the U. S. Navy for four years, mostly as a Lieutenant in the Submarine Service. He joined RCA Service Company in March, 1959, as a Computer Engineer. He was the manager of the CIA installation of RCA computers; later was promoted to EDPS Area Manager; and in January, 1962, was promoted to EDPS District Manager. Mr. Wright returned to EDPS headquarters in the Cherry Hill offices in December, 1965, as manager of EDPS Special Projects. In August, 1967, he transferred to Patent Operations of RCA Patents and Licensing. In May, 1969, he was registered to practice before the U.S. Patent Office as a Patent Agent. He received the JD from Temple University in May, 1971. He has four patents in the computer field and three pending, and has had articles published in professional magazines. He is a member of the American Bar Association.



Akillian is new TPA for Aerospace Systems Division

Norman L. Laschever, Chief Engineer, Aerospace Systems Division, recently appointed **Michael A. Akillian** Technical Publications Administrator for Aerospace Systems Division, Burlington, Mass. In this capacity, Mr. Akillian is responsible for the review and approval of technical papers; for coordinating the technical reporting program; and for promoting the preparation of papers for the **RCA Engineer** and other journals, both internal and external.

Mr. Akillian received the BA in Liberal Arts from Northeastern University in 1968. In February 1969, he joined Aerospace Systems Division as a technical writer in the Documentation activity, and worked on technical documentation for the LCSS systems. Currently, he is persuing the MS in Science Communication at Boston University's School of Public Communication and, as an honor student, is working on directed studies under the auspices of the program chairman. He is an active member in the Society for Technical Communications and has received several awards for his independently published works.

RCA phasing out its magnetic products business

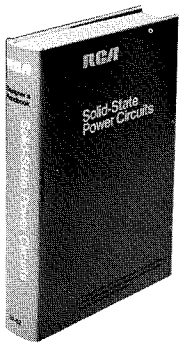
RCA announced it is phasing out its magnetic products business, which includes computer tapes and disc packs as well as audio and video recording tape.

This action was taken as part of RCA's withdrawal from the general purpose computer field. Prior to undertaking the phase out, discussions were initiated with various firms regarding the possible sale of the magnetic products business. The estimated costs associated with the phase out of RCA's magnetic products business are included in the $250 million extraordinary charge related to the company's withdrawal from the general purpose computer business.

Solid-state power circuits designer's handbook issued by RCA

The *RCA Solid-State Power Circuits Designer's Handbook,* an authoritative up-to-date reference on the design of solid-state power circuits, is now available from RCA Solid State Division.

The 704-page *RCA Solid-State Power Circuits Designer's Handbook,* Technical Series SP-52, contains detailed design information on the use of power transistors, thyristors (SCR's and triacs), silicon rectifiers, and power hybrid circuits. This Handbook, which is the successor to the popular RCA Power Circuits Manual (SP-51), describes the basic theory and technology of these devices, explains electrical and environmental factors that affect their operation in power-circuit applications, and provides detailed information on current techniques and procedures employed in the design of a variety of popular power circuits.



RCA Review, December 1971

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Contents

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Detailed explanations are provided of the basic physical theory, fundamental design concepts, operating parameters, structures, geometries, electrical characteristics, and maximum ratings for power transistors, thyristors, silicon rectifiers, and power hybrid circuits. Specific design criteria and procedures are supplied for circuits that use such devices in the amplification, rectification, conversion, control, and switching of electrical power. Design examples are given, and practical circuits are shown and analyzed for the following types of applications:

DC power supplies—Design details are given for half-wave and full-wave rectifiers for both single-phase and multi-phase systems and for linear and switching voltage regulators. Various types of current-limiting techniques are analyzed, and the effect of capacitive-load circuits is explained.

Power converters and inverters—The design of various types of inverter and converter circuits is described. Practical examples of both transistor and SCR types are shown.

Ballasts for mercury-arc lamps—Procedures and techniques employed in the design of solid-state switching-regulator types of ballast circuits for mercury-arc lamps are explained. Examples are given of circuits for both 120-volt and 240-volt operation.

Thyristor AC line-voltage controls—Circuit designs are provided for heat controls, lamp dimmers, light flashers, traffic-signal-light controls, motor speed controls and AC voltage regulators. Basic thyristor power-control methods triggering techniques and isolated control circuits are also explained.

RF power amplifiers—General concepts, criteria, and circuit design techniques for RF power amplifiers are explained. Design examples are shown of practical RF power amplifiers for single-sideband systems, military communications systems, mobile and marine radio, commercial-aircraft radio, and CATV systems.

Microwave power amplifiers and oscillators—Circuit techniques employed in the design of power amplifiers, oscillators, and frequency multipliers intended for operation at microwave frequencies are described. Applications of such circuits in microwave relay links and air-traffic-control systems is discussed.

Audio power amplifiers—The basic design criteria for audio power amplifiers are explained, and conventional, complementary-symmetry, and quasi-complementary-symmetry designs of audio power amplifiers are examined. Two "universal" design configurations for a series of audio power amplifiers and a unique bridge circuit configuration are analyzed.

Ultrasonic power sources—Design criteria are outlined for power oscillators, inverters, and power amplifiers employed in ultrasonic applications. The basic principles of ultrasonic transducers are also explained.

TV deflection systems—The basic principles and current practices involved in the design of horizontal and vertical deflection systems for television receivers are explained. The use of both power transistors and SCR's in the design of horizontal circuits is described. Different types of vertical output stages are compared.

Ignition systems—The basic principles and design concepts for solid-state ignition systems are analyzed. Design examples and practical circuits are shown for both inductive-discharge and capacitive-discharge types.

Copies of the *RCA Solid-State Power Circuits Designer's Handbook* can be obtained from RCA distributors, or by sending $7.50 to RCA Solid State Division, Box 3200, Somerville, N. J. 08876.

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