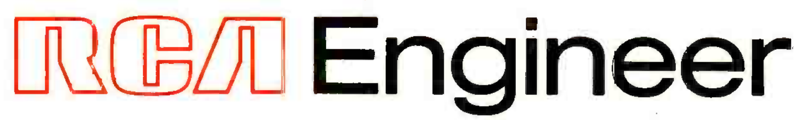

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1971

Solid state technology

I have on my desk or in my briefcase a small electronic calculator. Its "works" consist of four minute silicon chips (the latest design has only one) using large scale integration. Essentially, all of its weight and volume, its mechanical structure and the power it uses are for the purpose of enabling two-way communications between the chips and the user—a human being.

I find instantaneous elementary arithmetic extremely useful. However, to me the real significance of this calculator is as a constant reminder that electronic engineering is in the midst of a major revolution.

The old interface between components technology and apparatus and systems design has suddenly been modified so that the engineering of all information handling functions must be critically involved with solid state technology.

The Solid State Technology Center that provides the central theme of this issue of the *RCA Engineer* was established as an urgently needed corporate response to the resultant changes in our engineering philosophy.

In the interval between the planning of this issue and its delivery, RCA announced its decision to withdraw from the general purpose computer business and to concentrate its computer efforts in the development, manufacture and marketing of specialized data communication systems and specially designed business systems. This decision is requiring substantial restructuring of the long range strategies and business plans of all related RCA activities including the Solid State Technology Center.

The philosophy of the Center outlined in Mr. Englebrecht's article and the rich sampling of its technical activities described in the other articles constitute a valuable information resource for this planning process.

Dr. James Hillier
Executive Vice President
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Princeton, N.J.

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Our cover
. . . depicts a portion of the memory cells in a silicon-gate PMOS beam-lead memory array. The array is described in some depth by Reddy, et. al. (p. 28); the beam-lead process is covered by Rose, et. al. (p. 56). **Photo credit:** John Semonish, Electronic Components, Clark, N.J.

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RCA Engineer

• To disseminate to RCA engineers technical information of professional value • To publish in an appropriate manner important technical developments at RCA, and the role of the engineer • To serve as a medium of interchange of technical information between various groups at RCA • To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions • To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field • To provide a convenient means by which the RCA engineer may review his professional work before associates and engineering management • To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

RCA Engineer articles are indexed annually in the April-May Issue and in the "Index to RCA Technical Papers."

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editorial input

experience and education

Our minds are often trapped within the confines of traditional thinking because we inherit established definitions and jargon as part of a discipline. The jargon of education is particularly misleading. The term "continuing education" evokes an almost Pavlovian response: instantly, we tend to place it below formal higher education, ranking it as less structured, less significant, less recognized, and generally less important. Intuitively we feel that "real" education must be synonymous with academic or formal education, conducted in or by an educational institution.

The truth is that most of an individual's effective knowledge, particularly for an engineer or scientist, is acquired in the years following completion of the so-called academic education. If this is what we really mean by continuing education, we must clearly be on guard against our preconditioned responses. It is seldom recognized that the practicing scientist or inventor is himself a scholar who is in effect teaching himself and others as well. For these individuals, work experience is truly continuing education, and is probably the highest form of education in terms of effectiveness.

Many engineers, perhaps most, choose to exercise their talents in other ways: following a job to completion, meeting cost and schedule limitations, getting along with others, and deciding when to build and when to buy. This pragmatic experience builds a wealth of invaluable skills, but does not of itself provide a full measure of continuing technical education that will allow such an engineer to stay technically abreast of his profession.

There is a wide range of needs for continuing engineering education, made still wider by the ever-increasing numbers of recognized branches of specialization. The concept of educational half-life, introduced in the 1960's by James Killian, had not occurred to earlier educators when the conventional pattern of formal technical education became fixed. It is nevertheless a useful concept, and researchers are in remarkable agreement that the half-life of applicable technical knowledge in the field of electronics engineering is about 5½ years and declining. This implies a staggering burden in continuing education for any individual, and legitimately raises the question of feasibility. Here researchers tend to disagree. Some claim the job cannot be done cost-effectively, others argue that it can. They agree, however, that to remain current any technical man must be dedicated to a major uninterrupted program of post-professional education.

Basically, the time an engineer spends on educational pursuits depends on his own background and motivation, the demands of his job, and the possibility of future benefit. The key is to strike a good balance between formal educational pursuits and on-the-job experience . . . and between courses of immediate value and those that provide a broad foundation for the future.

As professionals, most engineers recognize their responsibility to maintain and improve their competence level and supplement their work experiences by some combination of formal educational programs and self-guided study. RCA also recognizes its responsibility for the professional development of the technical staff.

RCA's support of the formal educational process is evident in such activities as the Tuition Loan and Refund Plan, Continuing Engineering Education Program,[1] David Sarnoff Fellowship Program, Graduate Study Program, and after-hours courses at various divisions.

RCA also supports a significant part of the self-guided study. To help the engineer acquire information and perspective from others in the field, society participation is encouraged.[2] The flow of information within the company is aided by various communications channels—proprietary (Technical Reports, Meetings, and Symposia) and non-proprietary (*RCA Engineer* and *Trend*).

At RCA technical libraries, reference sources as well as newly published documents of value are available. To assist in information transfer and retrieval, the *Technical Abstracts Bulletin*, distributed monthly, contains abstracts of newly generated RCA documents. For notifications of new documents being published in the open literature, the ALERT service is available on a subscription basis.[3]

Thus, a great deal of help is available to the engineer who wishes to supplement his experience and up-date his education. How often and how effectively he uses this help contributes, to a large extent, to his long-term development as a professional.

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1. Biedenbach, J. M., "The RCA Continuing Engineering Education Program," *RCA Engineer*, Vol. 15, No. 3 (Oct/Nov 1969) p. 3.
2. Seideman, I. M., "The Engineer and Professional Societies," *this issue*, p. 78.
3. *RCA Engineer*, Vol. 16, No. 4 (Dec 1970/Jan 1971) p. 96.

Future issues

The next issue of the *RCA Engineer* contains selected papers from various areas of RCA, including several papers on solid state technology. Some of the topics to be covered are:

PMOS technology

Reliability of solid state products

Digital simulation

COS/MOS memory systems

Schottky barrier devices

Power transistors

Hybrid packaging

Discussions of the following themes are planned for future issues:

Mechanical engineering

Displays

Advanced technology

COS/MOS integrated circuits

Mathematics

Solid State Technology Center—purpose and plans

R. S. Engelbrecht

The Engineer and the Corporation

The Solid State Technology Center serves RCA's diverse needs for advanced development of solid state devices and integrated circuits. This paper describes the general climate that led to the establishment of the Center in early 1970 and highlights the Center's present objectives and programs. In relating the Center's many areas of effort to other activities in RCA, Mr. Engelbrecht guides the reader to other papers in this issue and next which provide in-depth coverage on specific topics.

THE INTEGRATED CIRCUIT, more than any other invention in the history of electronics, has revolutionized both the internal structure and the interfaces of traditional technical institutions.

To provide the student with the necessary multidisciplinary background, universities have established new curricula which straddle the natural sciences, mathematics, and the various specialized branches of electrical engineering. To exploit the IC profitably in the market place, electronics companies have restructured their organizations along more functional lines. To match its technological potential better to man's needs, society is beginning to re-examine the relative roles and relations between the contributing academic, industrial, and government organizations—in this country as well as abroad.

RCA, like other major electronics-based corporations, has traditionally been organized into independent, relatively autonomous components and systems divisions. Vacuum tubes, transistors, and passive devices were engineered, manufactured, and sold by the components division. Circuits and assemblies using these devices were developed and tested separately in the systems divisions for particular markets: consumer, industrial, government. The relative roles of the "component engineer" and the "circuit engineer" were well defined. The flow of technical information between the two was limited to type specifications provided by the component supplier, guided only by the general notion that "higher frequencies" or "more power" would always be in demand.

Integrated electronics changed that relationship drastically. Active and passive components and circuit interconnections could now be fabricated simultaneously on a common substrate as an inseparable unit. This capability encouraged component manufacturers to "integrate upward"; i.e., to make complete IC assemblies available as standard building blocks, replacing their previous discrete components. Simultaneously, the circuit engineer found that he could obtain better results by designing his specific systems objectives into the IC beforehand, making optimum use of the tradeoffs between the various active and passive components in the circuit. This possibility encouraged electronics systems companies to "integrate downward"; i.e., to become their own IC manufacturers. The tendency of both systems and components divisions to expand into IC's was enhanced by the traditional difficulties of organizational communications and the long development time for a successful circuit, requiring several iterations of the design-fabrication-test cycle.

Establishment of SSTC

In 1968, RCA Chief Executive Officer Robert W. Sarnoff appointed Dr. James Hillier, Executive Vice President, Research and Engineering, as chairman of a committee to review RCA's objectives in the solid-state business and to propose ways to maximize corporate opportunities in this field. In its final report, the committee noted two basic conclusions:

1) RCA's future leadership in elec-

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Rudolf Engelbrecht
Operations Director
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Solid State Division
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joined RCA in 1970 as Operations Director of the Solid State Technology Center. Prior to this appointment, he had been a Member of Technical Staff at Bell Laboratories since 1953, most recently as Head of Electroacoustics Department, Holmdel, N.J. During this period, he was responsible for a variety of exploratory development programs in high-frequency and high-speed solid-state electronics. He has published numerous papers and has been granted over fifteen U.S. and foreign patents related to parametric amplification, microwave integrated circuits, and transferred-electron devices. Mr. Engelbrecht received the MSEE degree in 1953 from Georgia Tech. A Fellow of the IEEE, he is chairman of the Professional Group on Electron Devices and past chairman of the International Solid State Circuits Conference.

Program selection and general policy guidance is provided by a Board of Directors comprising high level technical representation from each major operating unit and chaired by Dr. James Hillier, Executive Vice President, Research and Engineering. This photo, taken during a recent Board meeting, shows, clockwise from left, R. S. Engelbrecht, Operations Director, Solid State Technology Center; Dr. H. J. Woll, Division Vice President, Government Engineering; L. R. Kirkwood, Chief Technical Advisor, Consumer Electronics; Dr. W. M. Webster, Vice President, RCA Laboratories; Dr. Hillier; V. O. Wright, President, Systems Development Division, Computer Systems; and C. H. Lane, Division Vice President, Technical Planning, Electronic Components.

tronics depends strongly on achieving leadership competence in integrated circuits.

2) The IC needs of individual RCA systems and apparatus divisions are too small to support the required facilities in each separate organization.

Based on the committee's recommendations, the Solid State Technology Center (SSTC) was formed early in 1970 to:

Provide a central pool of shared engineering know-how and modern facilities, serving all of RCA's needs in solid state components and integrated circuits;

Establish and maintain capability for supplying operating divisions with samples and prototype quantities of IC's on a quick-turnaround basis, using the most advanced design, fabrication, and testing techniques available;

Reduce to practice the research results of the David Sarnoff Research Center in selected solid state technology areas of broad future interest to RCA systems divisions and to the Solid State Division for its OEM market.

Because of the obvious operational parallels, and to permit close interaction with the Solid State Division, SSTC was administratively attached to SSD and located at its Somerville, N.J., headquarters. To provide communications between SSTC and the Engineering Departments of the systems divisions, resident groups from each major operating unit were established and located at Somerville, participating in the design of IC's for their parent divisions and in the evaluation and assembly of completed units.

After a year's buildup by consolidation of existing advanced development efforts and initiation of new programs, SSTC has now reached the level of a viable organization. The Center is guided in its program selection and general policy matters by a Board of Directors, chaired by Dr. Hillier. Each major operating unit in the corporation has high-level technical representation on the Board.

Areas of effort

About eighty engineers and a similar number of technicians work on SSTC's programs in five major areas:

Materials and Processes
Semiconductor IC Technology
Hybrid and Packaging Technology
Power Technology
Design Automation and Test Technology

In the Materials and Processes department, studies on semiconductors, metals, insulators and plastics are aimed toward future solid state components having improved performance, reliability, or lower cost. Closely coupled to these materials studies are investigations of IC fabrication process steps such as epitaxy, diffusion, passivation, and metallization.[1] A substantial portion of the effort supports ongoing projects in the operating areas of the Solid State Division, aimed at yield or reliability improvements, or at cost reductions on products currently in manufacture.[2] Other programs are conducted jointly with advanced engineering groups in other divisions, for example, on the silicon vidicon camera tube developed by Electronic Components and used in the TV camera for Apollo 15.[3]

The Semiconductor IC Technology department develops new MOS and bipolar IC's in accordance with the long-range needs of SSD product areas and the systems and apparatus divisions. Substantial effort is directed toward COS/MOS devices and circuits because of their low-power requirements and superior noise immunity.[4] Another major program during the past year was directed toward high density semiconductor memories and associated interface circuits for computers.[5] Of growing importance are new device structures, such as silicon-on-sapphire, for future improvements in speed or power consumption.[6] In addition, considerable effort is directed toward components and IC's for linear applications in consumer and communications electronics.[7]

In the Hybrid and Packaging Technology department, advanced development is directed toward high-reliability IC systems using beam-lead metallization of semiconductor chips and their attachment to thin or thick-film passive circuits.[8] In close cooperation with hybrid technology groups of other divisions, extensive support on device packaging is provided to the product areas in both SSD and other major operating units.[9]

High-power and high-voltage applications require constant improvements in heat dissipation, voltage breakdown, and other characteristics affecting device reliability and life. In the Power Technology department, efforts are concentrated on transistor and IC designs permitting substantially higher voltage and power levels than presently available.[10] Other projects range from low-frequency power switching

and control devices to high-frequency solid state power oscillators.

A major future responsibility of the Technology Center is to supply SSD and other RCA divisions with samples and prototype quantities of IC's on a quick-turnaround basis, using modern, established fabrication techniques. The designs of these IC's typically originate in the user division, often through its resident engineering group located in Somerville. The designs are then translated into photomasks which are used to fabricate the circuit. At present, many requirements can be met by a PMOS process line operated by the Microelectronics Technology (MET) group in Somerville, which is certified under Military Specification STP-883.[11] New process lines will be added as the needs develop. Another important service of the department is to advise users from other divisions on potential applications of IC's and to aid in their design.[12]

Another supporting activity provided by the Tech Center and vital to RCA's future in solid state electronics is the use of the computer for automating or deskilling the many steps required for the development of IC's wherever technically feasible and economically attractive. The Design Automation and Test Technology department focuses on both long-range advances and immediate applications in computer-aided circuit design, artwork generation, mathematical circuit simulation, and test automation.[13] These activities are coordinated with other computer-aided design efforts in RCA to facilitate the transfer of programs and design information.[14]

A major objective of the Design Automation and Test Technology department is to reduce, wherever possible, the time required for carrying an IC from initial conception to final manufacture. In a field where technology is rapidly advancing, where the marketplace is highly dynamic and volatile, and where several design cycles are usually required before a new circuit is fully developed, time—in a very real sense—is money.

Summary

During SSTC's first year of full operation, it has made substantial progress toward its overall objective—to serve efficiently and responsively all of RCA's needs in advanced and applied solid state technology.

With its dedicated team of highly skilled engineers and technicians, aided by modern equipment and facilities, the Center is becoming a technical leader in its chosen areas of expertise. With the help of the resident engineering groups from other RCA divisions, the old barriers between research, component, and systems engineers are rapidly disappearing. RCA now has in place a workable mechanism for coupling its technological and equipment design skills and for supporting a healthy leadership position in the electronics industry.

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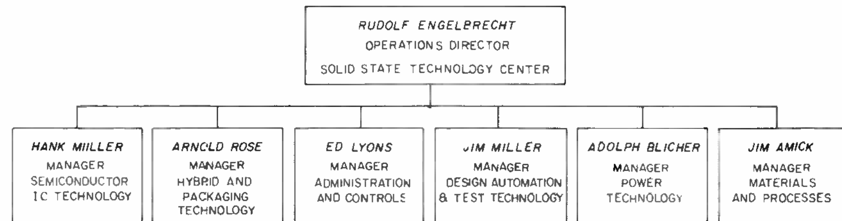
1. J. Amick describes several programs presently underway in the "Materials and Process Laboratory" (p. 42).
2. See V. Lukach, "Present trends in reliability," planned for publication in the next issue of the *RCA Engineer* (Dec 1971-Jan 1972).
3. A. D. Cope of EC describes "The silicon mosaic target—a blending of semiconductor and camera tube technologies," in the next issue of the *RCA Engineer* (Dec 1971-Jan 1972).
4. COS/MOS technology is covered in this issue by A. Dingwall, et al., "COS/MOS memory array design" (p. 34). In the next issue (Dec 1971-Jan 1972), J. Smith and L. Murray discuss "Radiation resistant COS/MOS and J. Oberman and G. Waas treat a "COS/MOS memory system."
5. The digital semiconductor IC program is described in general by H. S. Miiller in "Semiconductor advanced IC technology" (p. 16) and, more specifically, by N. Reddy, et al., in "Semiconductor arrays for mass memories" (p. 28) and by H. Beelitz and N. Ditrick in "Interface circuit design technology" (p. 38).
6. E. Boleky, et al, discuss "Silicon-on-sapphire, the ultimate MOS technology" in this issue (p. 46).
7. R. Dawson, L. Jacobus, and R. Brader describe the communications application in "Linear MOS design" (p. 21).
8. See A. Rose, et al, "Packaging concepts for beam-lead devices" (p. 56) and L. Murray and B. Richards, "Beam-lead COS/MOS integrated circuits" (p. 50).
9. H. Fenster of MET deals with "Hybrid packaging for high performance" in the next issue (Dec 1971-Jan 1972).
10. In this issue (p. 62) J. Gaylord, J. Olmstead, and A. Blicher discuss "Trends in the development of low and medium-frequency power transistors." In the next issue, R. Amantea, et al., discuss "High-voltage laminated overlay power transistors."
11. See H. Borkan, et al. of MET "PMOS technology for quick turnaround custom LSI," in the next issue of the *RCA Engineer* (Dec 1971-Jan 1972).
12. R. Bergman, et al. of MET cover "Monolithic applications—divisional interface" in the next *RCA Engineer* issue (Dec 1971-Jan 1972).
13. See (p. 6) E. Helpert, J. Miller, and D. Ressler, "Design automation—promise and practices."
14. See (p. 10) A. Feller, et al. of G&CS "Computer-generated custom COS/MOS arrays."



Organization Chart—Solid State Technology Center.

Staff Management Meeting of the Solid State Technology Center. In the photo (left to right) are Adolph Blicher, Arnold Rose, Jim Amick, Rudolf Engelbrecht, Ed Lyons, Hank Miiller, and Jim Miller.

Design automation—promise and practice

E. P. Helpert | Dr. J. C. Miller | D. G. Ressler

Considerable recent progress has been made in Design Automation through better understanding of the design process itself, availability of new computer hardware, and willingness on the part of the designers to try new techniques. This paper discusses the Design Automation process as practiced at the Solid State Technology Center, giving primary emphasis to artwork-preparation and testing phases. Simulation will be covered in the next issue.[1]

Edward P. Helpert, Design Automation and Test Technology, Solid State Technology Center, Solid State Division, Somerville, N.J., received the BSEE in June 1961 from Rutgers University, and the MS in Engineering in June 1963 from Princeton University. He is currently engaged in thesis research for a PhD degree in Mathematics from the Courant Institute of Mathematical Sciences, New York University. Mr. Helpert joined RCA Laboratories in June 1961 and has worked in the areas of pattern recognition, semiconductor device fabrication, and mathematical problems associated with numerical control. He joined the Solid State Division in November, 1970 and is currently a project leader in the Design Automation and Test Technology activity. Mr. Helpert was the recipient of an RCA Laboratories outstanding achievement award in 1969. He is a member of Tau Beta Pi, Eta Kappa Nu, and the Association for Computing Machinery.

Dr. James C. Miller, Mgr., Design Automation and Test Technology, Solid State Technology Center, Solid State Division, Somerville, N.J., received the BEE (1953) from Rensselaer Polytechnic Institute and the M Eng (1958) and PhD (1962) from Yale University. His doctoral thesis was on switching mechanisms in ferrites, for which he received the Honeywell Award from Yale University. In 1958 he joined the technical staff of RCA Laboratories where he remained until 1969. During this period Dr. Miller did research on a wide variety of computer related topics. Since 1969, he developed and led the Design Automaton Program for Solid State Division. In his current position he has active interests in all aspects of the application of computer technology to the design of solid state devices. Dr. Miller has received the Honeywell Award, the Adler Fellowship ,the David Sarnoff Fellowship, the David Sarnoff Outstanding Achievement Award in Science, and three RCA Laboratories Research Acrievement Awards. He holds twenty-five patents. He is a senior members of the IEEE, a member of Sigma Xi, Tau Beta Pi, Eta Kappa Nu, and the American Association for the Advancement of Science. He is active in community affairs with the Boy Scouts and other civic groups.

David G. Ressler, Ldr., Design Automation and Test Technology, Solid State Technology Center, Solid State Division, Somerville, N.J., received the BS in Chemistry in 1960 and the BSEE in 1963 from Rutgers, and the MSEE from the University of Pennsylvania in 1965. He joined RCA Laboratories in 1963 as a participant in the Research Training Program, where he studied light deflection in electro-optic crystals. After developing several computer programs for circuit analysis at the Laboratories, Mr. Ressler joined the Solid State Division, where he is now Engineering Leader, Artwork Systems in the Design Automation and Test Technology department. Mr. Ressler is a member of Phi Beta Kappa, Phi Lambda Upsilon Tau Beta Pi and Eta Kappa Nu.

Authors (left to right) Miller, Ressler, and Helpert.

A design engineer types some commands into a computer, pushes the GO button, and relaxes over his cup of coffee. A few minutes later, the machine begins to produce yards of complicated descriptions, parts lists, blueprints, and building instructions for a finished product. This is Design Automation—in the ideal.

In practice, the achievements of Design Automation (DA) have been more modest. The goal of DA is to provide quick turnaround and lower cost designs by placing the burden of routine design work on the computer. However, this has proved difficult to achieve because of the complexity of the design-manufacturing problem, and because human designers often have difficulty adjusting to such a radically different approach to their jobs.

Actually, considerable progress has been made. A better understanding of the design process itself, coupled with new generations of computer hardware and a willingness of designers to try something new, has lead to functioning computer systems turning out workable designs with acceptable speed and minimum human intervention. Indeed, many of today's complex designs could not be attempted economically without such systems.

The traditional approach to DA has been to divide the design process into two steps: 1) cut and 2) try. Either a human or the computer proposes an initial design. The computer then simulates the design, predicting how the design would behave if it were actually built. Using these results, the design is modified as necessary and again the computer simulates it. This process continues until a satisfactory design has been reached. Considerable progress has been made in the field of simulation since the early days of computer-aided design; a companion paper to be published in a future issue describes SSTC's accomplishments in the field of electronic circuit simulation.[1]

Besides simulation, the computer helps the design work in other ways. At the Design Automation and Test Technology department of SSTC, two other aspects of DA are being developed to aid in the design of integrated circuits: artwork and testing.

Artwork is the term applied to the masks or templates used in the manu-

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facturing process which define the physical shapes of the elements and their interconnections. This discussion is limited to the artwork required for the manufacture of solid state devices, although one will recognize many similarities between this problem and printed-circuit-board layout, backplane wiring, etc. The details of a particular mask may be quite complex and represent a delicate integration of circuit functions, design economics, and the manufacturing process. It is a matter of much judgment and skill to balance these factors into a cost-effective design.

Testing examines the output of the manufacturing process and asks: Does the circuit chip meet the design requirements? Traditionally not a part of the design automation problem, testing has become a major challenge in the past few years. Increased circuit complexity, such as large scale integration (LSI), more lengthy and exhaustive test specifications, and better device performance have combined to make testing an expensive and crucial part of the manufacturing process. The advent of elaborate computer-controlled electronic test equipment makes the testing area a natural for DA.

As summarized in Fig. 1, design automation parallels the human design process and provides computer tools to:

1) Predict the performance of a proposed design—simulation;
2) Provide detailed patterns to manufacture the design—artwork;
3) Verify the design and process—testing.

Artwork

Computer artwork generation was first developed to manufacture printed-circuit boards and interconnect these boards into a system. Components from various technologies were mounted on the board and interconnected. In the jargon of design automation, the components were "placed" and "routed". Computer aids were desirable because the sheer number of decisions required made this procedure tedious and error-prone for humans. It quickly became apparent that the human could usually lay out a "better" mask, but the computer was faster and more accurate. It was not

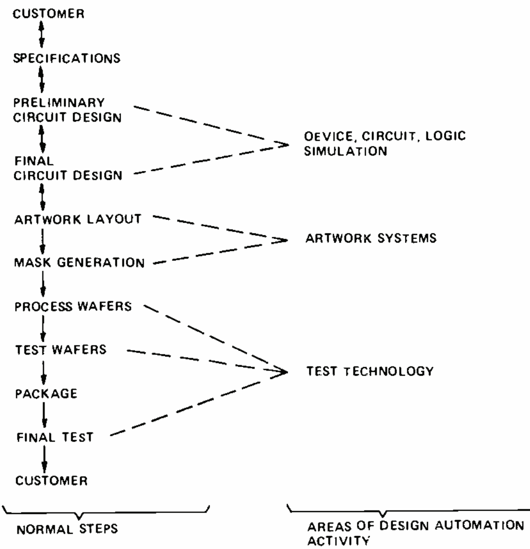

Fig. 1—Design flow chart.

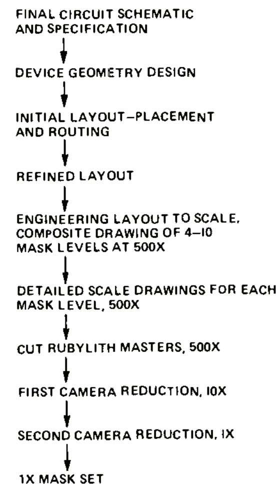

Fig. 2—Conventional IC artwork cycle (extensive error occurs at each step).

enough to create a layout that did the job. It had to be also a superior design in terms of cost or performance, preferably both. This is particularly important in design of solid state components where chip size is an important figure of merit in a layout.

Fig. 2 shows the key steps in the conventional artwork cycle as used in the semiconductor industry. A composite layout is manually generated by an engineer-draftsman team. The composite is a scale drawing (typically 200X—1000X) of the final mask set drawn in shape outlines and using color codes to denote the separate mask levels. From this composite, a set of detailed drawings are made, usually one for each mask. These drawings are used to guide the technician who cuts the shapes on Rubylith and peels the opaque sections. The Rubylith masters are camera-reduced to produce the tiny glass-plate master from which the circuits can be made. Certain parts of the process can be automated, such as cutting the Rubylith. Overall, the procedure is slow and error prone, has accuracy limitations, and resists changes.

Two broad computer approaches have been popular, each with many subvariants. Design Automation designers frequently structure the artwork problem into two subtasks—placement and routing—and develop algorithms to do each separately. Given a circuit schematic it is translated manually into

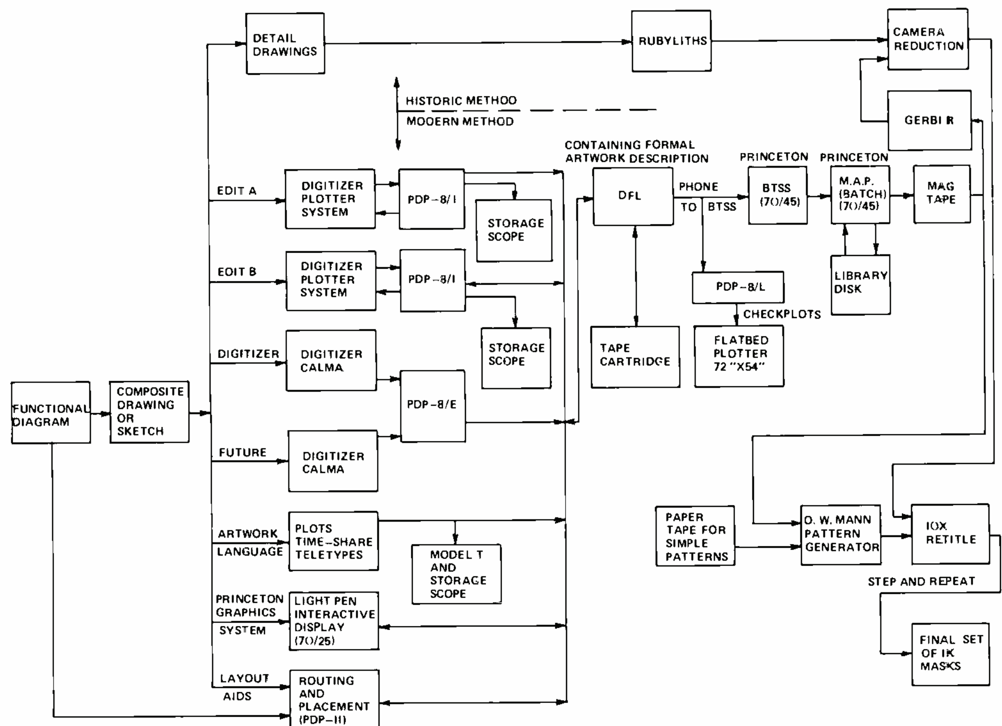

Fig. 3—SSTC art system block diagram.

available geometrical blocks (called cells or library elements). Each cell has known geometrical and electrical characteristics. The placement problem consists of sliding the cells about until a positioning is reached which looks promising and which one hopefully could be routed or interconnected by the subsequent program. Actually, a given placement may not be one which can be routed, and changes are required to permit an overall solution. A human approaches the layout problem more deftly, intertwining placement and routing to a degree not possible in the present design automation art.

The approach, just outlined, relies on standardized cells, formal layout rules (such as all cells aligned in rows), and structured interconnect schemes (such as north-south metal runs, east-west tunnels). Some procedures guarantee a workable layout without human intervention, but most require some reworking by manual means—frequently a painful process; the more automatic the procedure, usually the more advanced the reworking or editing process. Advantages of this approach include fast turnaround, error-free masks, and a reasonable likelihood that the design will work. Among the disadvantages are inefficient chip layout, awkward human-computer interface for editing, the necessity to design and characterize the standard cell library, and limitations to certain process technologies (e.g., MOS, bipolar) and performance levels.

A second approach which has received wide publicity is the use of computer-refreshed displays which are used as powerful drafting machines guided by human designers. Here, great flexibility is afforded the human as he interacts with the computer through pictures on the display. This technique can use cells or not, and usually achieves a better layout because of the high degree of interaction possible. The key disadvantages are the large investment required for each installation and the surprisingly large software system necessary.

On balance, it has been difficult to effectively juggle cost of design (including time) and design performance with either method. No one system is suited for all applications. This has led the design automation group at SSTC to consider an intermediate approach, placing more stress on the ability to interact with humans and to support *any* design technology, rather than a highly automatic, rigid system. Each artwork approach has merit and a choice can be made only after considering the local needs and resources.

The block diagram of the SSTC artwork system is shown in Fig. 3. The system is devised to have modular units with clear and logical software interfaces. A considerable variety of input is employed, allowing the user flexibility in choosing the tool most appropriate to the design at hand. The two major tools are the PLOTS language and the Digitizer-Plotter System. A few words will be said about each.

PLOTS[2] (Plotting Language On Time Sharing) is a software approach especially suited for the creation of library elements and designs characterized by a high degree of regularity. Examples would be memories, shift registers, and the universal array. Using PLOTS, the designer types simple statements into a file in BTSS III, the RCA time-shared system. Examples of PLOTS statements and the corresponding layout is shown in Figs. 4a and 4b. The PLOTS system performs certain logical checks on the data to detect common errors and sends signals back over the telephone line to drive a simple storage tube display.[3] This procedure gives immediate graphic response to the user and permits him to take remedial action to change errors detected. At this point the designer can request a large scale checkplot or if he wishes, go directly to MAP (Mann Artwork Program) which generates the control tape for the computer-driven reticle generator. No further human steps are required. PLOTS is a highly user-oriented language and can be used by engineers and technicians having little skill in the computer art. Despite its seeming simplicity, it has been used to design complex arrays, as shown by the 1024-bit memory in Fig. 4. Quick turnaround, remote access, and limited capital investment are other advantages of this approach.

The Digitizer-Plotter System (DPS) shown in Figs. 5 and 6 is the workhorse of the artwork system. This uses an interactive digitizing approach to capture composite layout information and generate a computer file containing all of the data necessary to create a mask set. The DPS is controlled by a PDP-8/I computer and is supported by a series of user aids to create, modify, error-check, and plot designs. The DPS hardware contains a minicomputer, disk, plotter, joystick, printer, cassette tape unit, and data-set interface. It is capable of transferring files to BTSS for subsequent processing. These features are especially valuable for complex irregular designs which are difficult to visualize without a physical layout. Major stress is placed upon rapid, meaningful feedback to the user—so that he can choose between multi-color checkplots, storage tube pictures, and teletype printouts.

A major advantage of the artwork System is the compatible interface between *any* of the input tools. A design can be started with one technique, say PLOTS, then brought over to the DPS for checkplotting, edited on the DPS, and passed back to MAP. Either method allows extensive and flexible use of library elements to modularize the layout and build on previous design efforts. Library elements can be

```
/PRINT#
  10 *C/27 XOYO
  20 *M/1
  30 *P/XOY1.5 R2 T.7 TO XOY1.5;TRIANGLE
  40 *O/X2.2Y1.5 R.3 T.3 L.3 B.3 AND 1T.5; TWO SQUARES
  50 *W/.5
  60 *L/XOYO T1 R.3 B.3 L.5;START RCA TITLE
  70 *L/XOY.7 TO X.3YO
  80 *L/X1Y1.1 B.1 L.4 B1 R.4 T.1
  90 *L/X1.2 YO TO X1.7Y1 TO X2.2YO
 100 *L/X1.4Y.5 R.4
 110 *E/
 120 *M/2
 130 *O/X1Y4 R.6 T.5 L.2 T.2 L.2 B.2 L.2 B.5 AND 5R1 AND 1T1 AND 5L1
 140 *Q/27 X1Y1 AND 2R3
 150 *Q/27 X9Y9 ROTATE2 AND 2L3;ROTATE 180 DEG
 160 *Q/27 X9Y4 ROTATE 3;ROTATE 270 DEG
```

Fig. 4—Example of use of PLOTS language to describe artwork: (above) typical statements and (right) photograph of resulting figures on a storage scope (minor closure errors due to display drift).

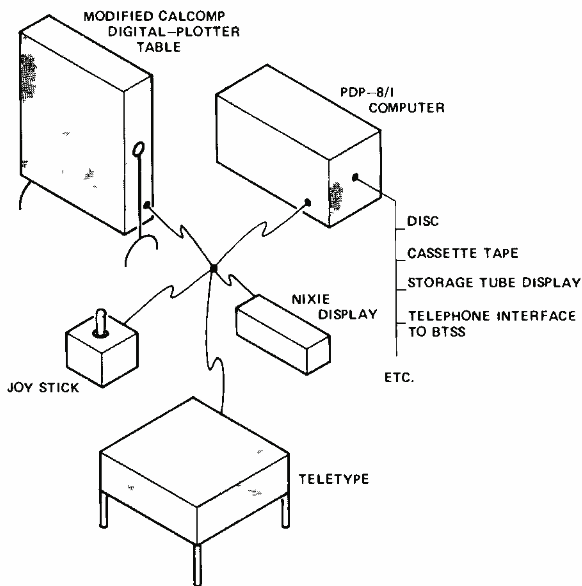

Fig. 6—Design automation area showing digitizer-plotter system.

Fig. 5 (left)—Digitizer-plotter system used to capture manually generated artwork from sketches or precision layouts to create a computer file describing the artwork, to edit or change the layout through the computer, and to prepare a check plot for human verification. All subsequent steps are computerized.

very simple, such as a rectangle on mask layer, or can be as complex as a complete design. Up to 32,000 library elements can be maintained by the system, each containing an arbitrary number of mask layers; in addition, library elements can be defined in terms of other elements. This concept, called "nesting," permit up to 10 levels and allows the designer a powerful hierarchical tool to build upon previous successful designs. The use of library elements is akin to use of shorthand; it is a symbolic way of representing stages of designs. Properly used, library elements shorten layout times, reduce errors, and offer the layout equivalent of functional building blocks; a powerful tool of the logician.

Testing

The present design automation testing effort in SSTC centers on four major problem areas:

1) What is a good set of tests for a given design and/or process?
2) How can computer-controlled IC test equipment be most effectively programmed?
3) What information can be gleaned from the test measurements?
4) How can this information be used to improve the design and/or monitor the manufacturing process?

All of the areas described are in their initial development. The first area has more than passing interest when one considers that for most sequential digital networks, manual test generation accounts for half the test-programming cost. In addition, human methods are often error prone, and some circuits are so complex that manual test generation is impractical. Thus, a viable method of automatic functional test generation will have enormous impact on reduction of test programming cost, increased testing reliability, and completeness and accuracy of the test sequence. That this problem is important and difficult is evident from the industry-wide interest it has received. As part of this project, TESTSIM, a BTSS program to check completeness of functional test sequences for digital circuits was written and is now used by several RCA divisions.

The great amount of flexibility that computer-controlled test equipment (CCTE) has makes the programming task difficult. Because the computer acts both as a controller and calculator, it is necessary to understand both of its functions for most efficient usage. This places a difficult burden on the test engineer. High-level languages have been successfully used on some equipment in an attempt to ease this burden, but the power of programming languages for other testers is distressingly low. Our work in this area concentrates on relieving the test engineer from some of the programming burden by allowing him to specify his test requirements in a tester-independent format. In addition, test program debugging aids are being developed, with emphasis on semiconductor memory testing. Again, we adhere to the philosophy that engineers with little skill in computer programming should be able to use this specialized equipment easily.

Areas three and four deal with data analysis. Traditionally, engineers have not fully utilized the data gathering and analysis capabilities of CCTE for several reasons;

1) Limited on-line computing capability of CCTE.
2) Test engineer's unfamiliarity with scientific programming techniques necessary for data analysis.
3) Inconvenience of using additional data processing equipment.
4) Lack of, and difficulty in using, available data analysis programs.
5) Hardware and software incompatibility between CCTE and data processor.

Our initial work in the area of the data analysis is an attempt to get the test and design engineers to realize the power and potential of the computer as an analysis tool. With their cooperation, we are developing a rapid turnaround system for various aspects of test data analysis, such as failure pattern analysis, graphical presentation of test results, etc., that attempts to cope with all of the aforementioned problems.

In the future, the area of data analysis will provide the key that opens the door to process control. It is the mechanism by which the design-manufacturing loop will ultimately be closed.

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Computer-generated low-cost CMOS custom arrays

A. Feller | A. M. Smith | R. Noto | P. W. Ramondetta
R. L. Pryor | J. N. Greenhouse

The Advanced Technology Laboratories, Government and Commercial Systems, is currently generating large-scale integrated CMOS custom arrays using a computer-automated system. This system, developed and implemented by ATL during the past 5 years, is primarily intended to provide a low-cost, quick-turn-around capability for low- and medium-volume users. Using the CMOS standard cell array technique, partitioned logic is accepted as computer input data and precision mask artwork is provided as output. The components of the system include the basic computer programs, the circuits that comprise the standard cell family, and the standard cell CMOS array topology.

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attended California Institute of Technology and Iowa State University. He was graduated from the Missouri School of Mines and Metallurgy with the BS in Physics in 1955. In 1955, he joined Advanced Technology Laboratories and is presently working on the design of new cell families for P-MOS and C-MOS computer-aided large-scale-array technology. His engineering experience at RCA has included analog computer circuit design, developmental work on a glass inspection machine, a metal detector, and circuit design for a magnetic drum memory. For the past four years, he has done sytem developmental and circuit design work on various types of ferrite random-access memories, where techniques were being sought in advance of the state-of-the-art. Mr. Pryor is the co-holder of two patents in the ferrite memory area, and the co-author of a paper on high-speed microferrite memory.

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received the BSEE from the City College of New York in 1966 and the MSEE from the University of Pennsylvania in 1970. In 1966, after completing the rotational training program, he joined the Advanced Technology Laboratories. While on the Graduate Study Program, he was involved in the design and development of such communications devices as those employing solid state microwave sources and microwave pumped photoconductors. In 1969, he joined the Computer Systems Research and Applications group. Since that time he has been responsible for the design, simulation and evaluation of the standard CMOS circuits employed in the ATL design automation system. Mr. Ramondetta has been involved in MOS transistor modeling. Mr. Ramondetta is a member of Eta Kappa Nu.

A. M. Smith
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received the AB in Physics from Temple University in 1955 and the MSEE from the University of Pennsylvania in 1965. He joined RCA in January 1966 and was a major contributor in the system design of a large-scale, high-speed general-purpose processor and in the specification of the bipolar LSI arrays that were used to implement this system. More recently, he has been engaged in several MOS integrated circuit design and development programs. Prior to joining RCA, Mr. Smith designed the teletype buffer system for the Burroughs 8500 computer. He also conducted a study of error detection and correction codes and their implementation. At Philco Corporation, as a member of the Advanced Computer Design and Development Group, he was the major contributor to the redesign of the Model 211 Computer.

J. N. Greenhouse
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received the BSEE from the University of Illinois in February 1969. Following graduation, he joined RCA as an Engineer in Training on the Rotational Program. As one of his rotational assignments, Mr. Greenhouse was assigned to the CMOS array group at RCA Somerville to assist in a project to increase the switching speed of a CMOS functional gate. He made extensive use of the CASMOS computer program in this effort which resulted in a speed increase of 50%. Mr. Greenhouse joined the Advanced Technology Laboratories on a permanent basis in June and has been working with the computer-aided circuit design programs such as ECAP and LOGSIM.

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received the BSEE from the University of Pennsylvania in 1951 and the MSEE in 1957. He also earned 12 credits toward the PhD in EE. With the RCA Broadcast Television Group since 1951, Mr. Feller worked as a design and development engineer. In 1958, he transferred to EDP Advanced Development Engineering and became a member of Advanced Technology Laboratories in 1963. Recently, Mr. Feller has been applying design automation techniques to the generation of mask artwork for bipolar integrated circuits. In the area of MOS arrays, Mr. Feller has been involved in MOS model specifications and in MOS circuit design. In this connection, he has written a program for transient analysis of P, N or CMOS circuits. He worked on the design and characterization of the PMOS circuits that comprise the PMOS standard cell family. He also designed a special purpose test chip and was responsible for its experimental measurements and evaluation. He has authored and co-authored numerous papers and presentations on computer-aided circuit analysis and design.

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received the BSEE from UCLA in 1957 and the MSEE from Drexel Institute of Technology in 1963. He has also completed work toward the PhD in Engineering at the University of Pennsylvania. He joined RCA in 1961 and has been responsble for computer simulation of the A/D Differential PCM Unicom system, design of the control logic portion of a classified system, and computer analysis and design of a nonlinear log compression network. In 1966, he joined the Advanced Technology Laboratories as Project Coordinator (Camden) for the 4101C Integrated Circuit Computer Project, a joint effort of six RCA divisions. Most recently, he has contributed heavily to the RCA design automation system for MOS arrays and to the P-MOS Standard Cell Family program. Mr. Noto has written several other programs in the field of design automation. He has published two technical papers and is a member of Phi Eta Sigma, Tau Beta, Pi, and the IEEE.

Authors (from left to right) Pryor, Ramondetta, Smith, Greenhouse, and Feller. Mr. Noto was not available for the photograph.

ALTHOUGH the first CMOS standard cell array was produced in the last quarter of 1970, the system represents an extension of a PMOS capability developed by ATL under government contract from 1966 through 1968.[1,2] Versions of these PMOS programs, adopted by many other companies, have produced thousands of PMOS chips. For the present, the ability to produce CMOS standard-cell arrays is unique to RCA.

Standard cell LSI array concept

The standard-cell array concept for producing large-scale integrated (LSI) arrays begins with the design, layout, and validation of a group of custom circuits called *standard cells.* Within the framework of the standard-cell topology, all the inherent efficiency of a custom design may be incorporated into these individual circuit cells. Once validated, these cells are given an identification or pattern number and permanently stored. To use one of these stored cells in a logic design, the user calls for these cells by pattern number. The computer retrieves the cell data from the stored library in a way such that individual cells are represented by a collection of polygons on each of the seven mask levels. The computer programs automatically generate the metallization and/or tunnels to interconnect the standard cells into the required function.

It is characteristic of this computer approach that the interconnections will almost always be successfully completed. The program virtually guarantees successful interconnection by increasing the roadbed used for the signal interconnection. Thus, this computer approach results in a quick-turn-around and low-cost method for generating the mask artwork for complex LSI CMOS arrays. This is of primary importance to the multi-type, low-volume user since artwork, masks, and initial costs are his major costs. Thus, the low-volume user can optimize his designs and products by making full use of LSI CMOS custom chips in such a way that the design of the chips are under his control for a significant portion of the design cycle.

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Therefore, changes and modifications can be made more efficiently.

The advantages of the standard cell array approach are:

Individual cell custom designed for high density and efficiency
Reliability of using tried and tested circuits
Computerized accuracy and reproducibility
Flexibility of logic and storage
Open ended for new cells in same family
Open ended for extension to analog, majority logic . . .
Prompt incorporation of improvements in process and layout rules
Super cell efficiency
Quick turn-around time
Ease of corrections due to change and errors
Efficiencies of late and consolidated chip releases
Low cost
Utilization of semiskilled personnel
Circuit performance characterization
Node capacity printout.

CMOS standard cell custom array approach

The three basic ingredients of the CMOS standard cell custom array approach are:

Design automation computer programs
Standard-cell circuit library
Standard-cell array topology.

Design automation computer programs

The primary task of the family of the standard cell computer programs is to accept the user's input in the form of a properly identified logic net list and produce as an output a magnetic tape that will result in the production of the seven-mask artwork by an automatic plotter. The heart of these programs are the *Placement, Routing* and *Folding* (PRF), and *Artwork* (ARTWRK) programs.

The *Placement* routine locates each of the cells required to implement the overall logic in accordance with an algorithm that minimizes crossovers and total wire length as well as other constraints. The user can exercise some control over the placement by the proper assignment of weighting factors available for the *Placement* routine.

The *Routing* routine interconnects all the cells (and pads) in accordance with the logic net list. The routine uses either metal or tunnel interconnects to accomplish the signal interconnection. The decision as to exactly which type of interconnections will be used is automatically determined by the routine. If the routine mechanizes a particular signal line with a tunnel, it will automatically establish all the levels associated with the tunnel, the appropriate guards bands, and the tunnel ends.

Closely allied with the *Routing* routine is the *Folding* routine which automatically helps arrange these cells in rows in such a way as to make the overall aspect ratio of the chip as close to unity as possible. Various aspects of the cell placement and orientations are discussed in more detail in the discussion on the CMOS array chip topology.

The ARTWRK program takes the output of the *Placement, Routing,* and *Folding* program, combines it with the circuit and cell data relating to those stored cells which are used in the particular logic, and generates a magnetic tape

Table I—CMOS standard-cell logic family.

Cell No.	*Circuit function*
1110	Inverter
1120	Two-input NOR
1130	Three-input NOR
1140	Four-input NOR
1210	n and p transistor
1220	Two-input NAND
1230	Three-input NAND
1240	Four-input NAND
1260	Begin shift (D flip-flop)
1270	Middle shift (D flip-flop)
1280	End shift (D flip-flop)
1290	Free shift (D flip-flop)
1300	Non-inverting buffer
1310	Buffer inverter
1320	Transmission gate
1330	2×1 multiplexer (single clock, dual transmission gate)
1350	3×1 multiplexer (triple clock, triple transmission gate)
1420	Set-reset flip-flop
1430	Three-input multiplexed data register
1500	Three-input multiplexer data register (custom MDD)
1510	Three-input multiplexer data register
1520	Double-buffer inverter
1530	Double-buffer/buffer inverter
1620	Two-input AND
1630	Three-input AND
1640	Four-input AND
1720	Two-input OR
1730	Three-input OR
1800	2, 2, 2, 2 AND—4 NOR
1810	Buffer (inverting)
1820	Master/slave flip-flop, Q out
1830	Data flip flop
1860	2, 2 AND—4 NOR (2/4×1 multiplexer)
1870	2, 2 AND—2 NOR (2×1 multiplexer)
1880	Two-bit carry anticipate
1890	2, 2, 2 AND—3 NOR (3×1 multiplexer)
2000	D flip-flop, Q & Q
2100	Multiplexer/data selector (4 MUX—3 cont)
2200	Multiplexer/data selector (3 MUX—2 cont)
2300	Exclusive-OR/buffered exclusive-OR
2310	Exclusive-OR
2400	Special custom network
2500	Special custom network
2600	Functional OR net
2700	AND/OR
2800	Two-input NAND/buffered AND

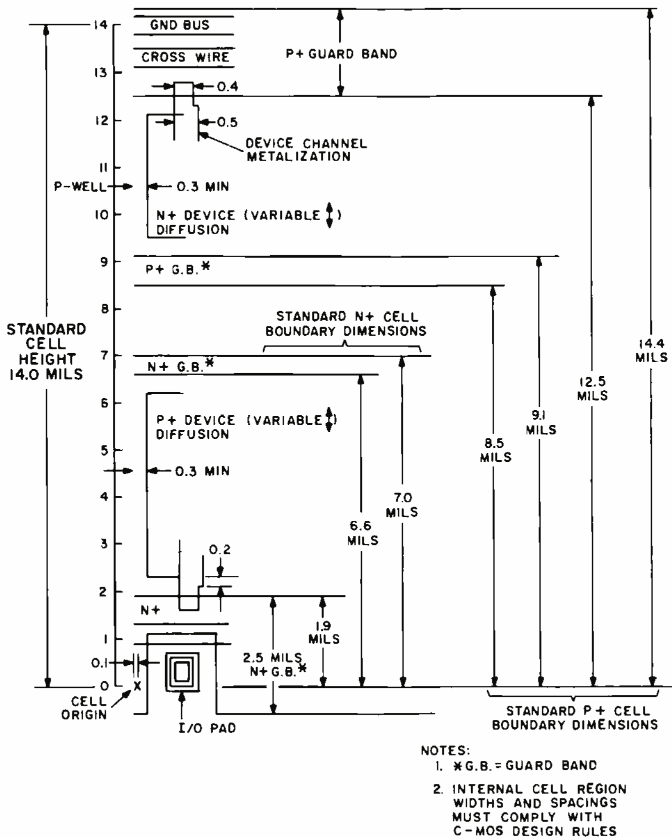
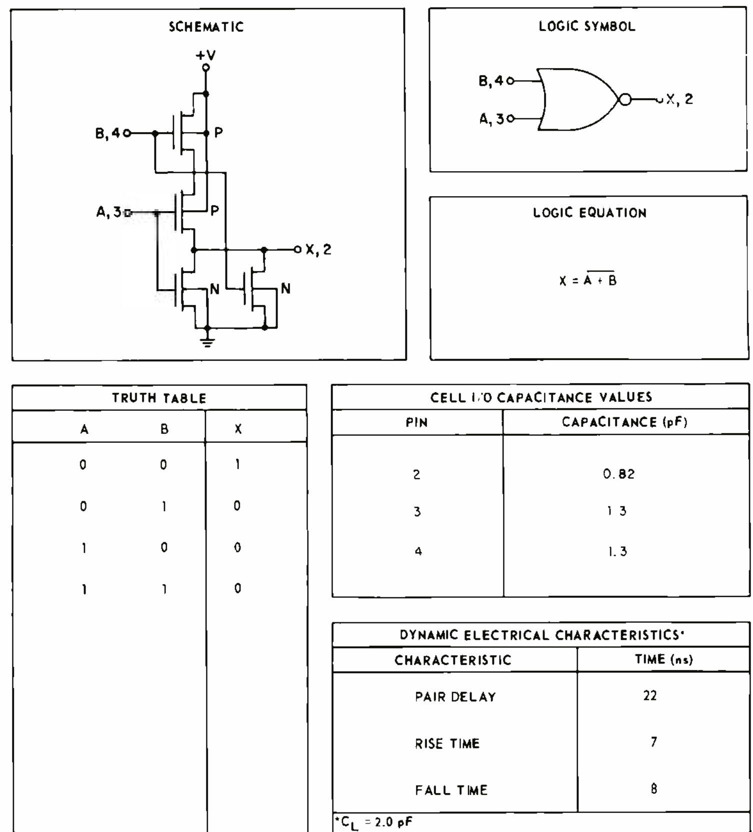


Fig. 1—CMOS standard cell dimensions.



TRUTH TABLE

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	0.82
3	1.3
4	1.3

DYNAMIC ELECTRICAL CHARACTERISTICS*

CHARACTERISTIC	TIME (ns)
PAIR DELAY	22
RISE TIME	7
FALL TIME	8

*C_L = 2.0 pF

Fig. 2—Two-input NOR cell No. 1120 data sheet.

that contains all the necessary instructions and information that results in the generation of the seven-level mask artwork (usually at 80X) using a Gerber automatic plotter.

Standard-cell circuit library

The standard-cell circuit library is a set of logic circuits that have been defined, configured, designed, topologically laid out, checked, analyzed, simulated,[3,4] validated, and then stored permanently. The cells range in complexity from a 2-device inverter to complex super cells having more than 20 devices. These cells are identified with a pattern number that can be used to automatically retrieve the cell from the library tape for use in a particular logic application.

The present standard cell family, shown in Table I, consists of 46 cells. The family is expected to grow to more than 50 logic cells by the end of 1971. All of the cells listed in Table I, except 1860 and 1870, have been designed into standard-cell LSI arrays that have been fabricated and tested.

The "standard cell" designation is used because all cells in the family must be multiples of a standard height as shown in Fig. 1. All input and output connections to each cell are made via the I/O cell pads, shown at the bottom of Fig. 1. The computer program determines whether connections to these I/O pads are either tunnels or metal. The two-input NOR member of the standard cell family is an example of one of the simpler cells. The data sheet for this cell (Fig. 2) provides the system and logic designer with basic design information for the cell. This format is followed for all cells that have been characterized and validated.

The identification (or pattern) number assigned to the two-input NOR cell (No. 1120) permits it to be automatically retrieved from memory when required. As shown in Fig. 2, the data sheet contains the circuit configuration, the logic symbol, the boolean equation, and the truth table. The remaining information on the data sheet gives the capacitance at each input and output

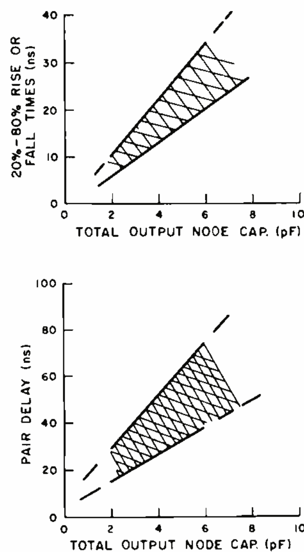


Fig. 3—Performance data for two-input NOR cell No. 1120.

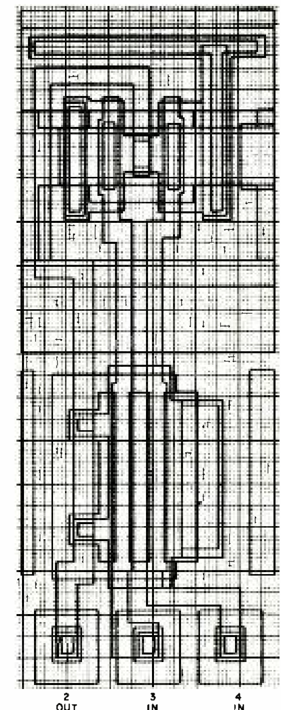


Fig. 4—Composite topology layout for two-input NOR cell.

cell pad and the dynamic performance that includes the pair delay and the rise and fall times when driving 2½ unit loads. A unit load is defined in terms of the standard inverter and represents a capacitance of approximately 1 pF. These dynamic characteristics are typically average values that permit the designer to make initial preliminary delay estimates. The cell-characterization data shown in Fig. 3 for the two-input NOR cell provides the designer with average delay information over a range of capacitance load values. The composite for the two-input NOR cell topological layout is shown in Fig. 4.

An integral part of the standard-cell approach centers on the design and layout of the standard-cell array or chip topology. The topological layout of the chip must be compatible with the Solid State Division's factory process and design rules while allowing the design automation computer programs to automatically layout an optimized topology.

To facilitate a description of this topology, the layout is shown in Fig. 5. This particular layout has four rows of standard cells. The number of rows can vary from chip to chip depending on size and complexity. Within each row, the dotted lines define a unique standard cell. As shown in Fig. 5 on the bottom row, all the n devices and p devices in each row are completely enclosed by a common guard band. This results from the technique used to custom design the guard band structure during the design of each standard cell.

The function block on the left side of the chip contains the test devices, the power pads, and mask alignment keys. The ground pad (identified in Fig. 5) connects to a ground bus which runs between the row of cells and around the perimeter of the chip. The perimeter ground is laid out to provide a ground connection for the protective diodes associated with all input pads connecting to gate inputs. The supply bus is distributed completely through the n⁺ diffused area. Therefore, except for two ground strips, the metallization level is used exclusively for signal interconnections.

CMOS standard-cell test array

The CMOS standard-cell test array, produced in 1970, had several objectives.

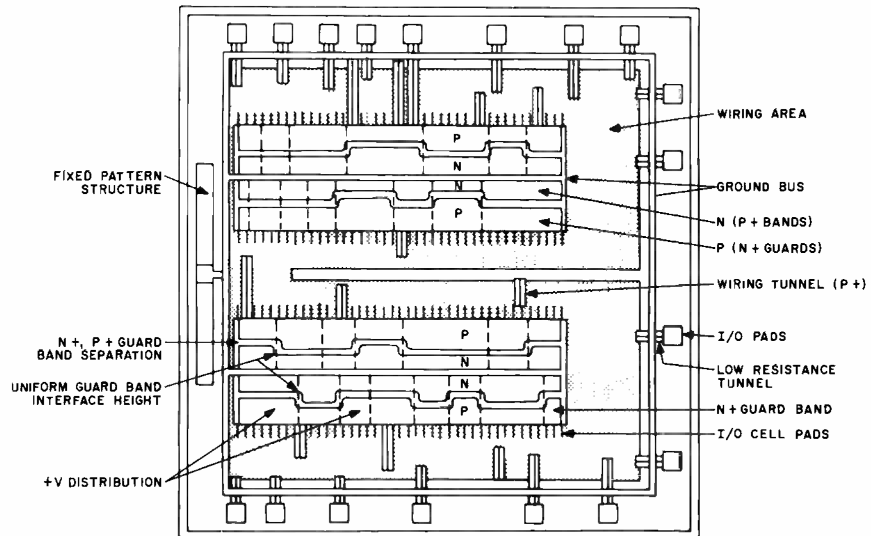


Fig. 5—Layout of CMOS standard cell array.

The primary objective was to validate the design automation computer programs and the design concepts and techniques developed in connection with the standard-cell technique. A second objective was to provide a test vehicle from which performance data could be measured directly. The test vehicle provided data which was used to verify the accuracy of the computer circuit-simulation technique that was used in the original circuit design. To achieve these first objectives, at least one circuit type out of each of the basic groups of the standard-cell circuit complement was incorporated into the fabricated test chip. A third objective was to provide the test patterns and circuits to verify that the chip design was compatible with the various fabrication and process constraints, and to allow these fabrication and processing parameters to be determined to within an acceptable level of accuracy.

The logic content of the test chip is shown in Fig. 6. Each circuit type used has been identified by the cell number so that ready reference can be made to the data sheets of the type shown in Fig. 2. In addition, the pad (**P**) designations are listed so that they may be easily located on the metallization level mask artwork shown in Fig. 7.

Extensive measurements were made on all of the circuits shown in the test chip. Before fabrication an on-chip pair delay (see Fig. 2) of 22 ns (11-ns stage delay) was predicted for the two-input NOR circuit, cell No. 1120. Measurement made on the NOR configuration used on the test chip indicated a 6-stage delay of 86 ns (14-ns stage delay). The 3-ns difference between the

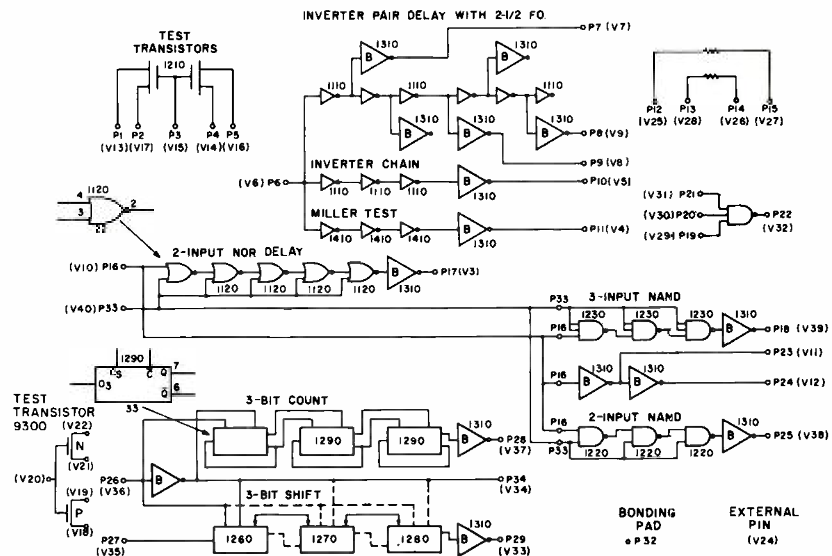


Fig. 6—CMOS standard cell test chip (level 6).

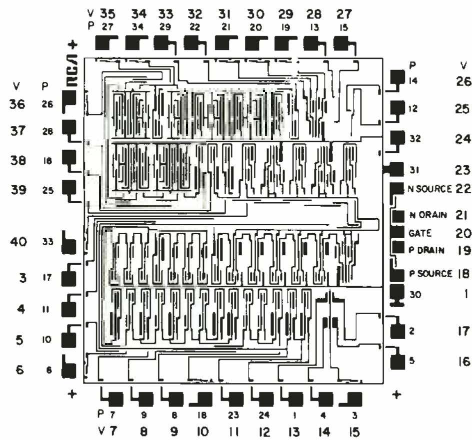


Fig. 7—CMOS test chip, logic diagram.

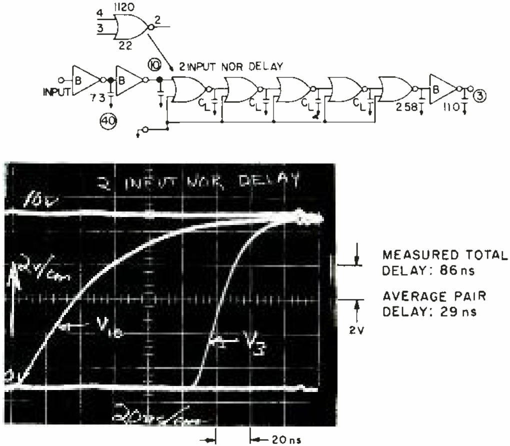


Fig. 8—Standard Cell 2-input NOR measured delays.

measured and predicted performance results in part from the differences that existed between the measured and assumed threshold voltages for the p- and n-type devices. The NOR test circuits and actual measured waveforms are shown in Fig. 8.

Applications

The CMOS standard-cell LSI array technology is now being used in the design and fabrication of more than twenty custom chips which are in various phases of the design and fabrication cycle. Nine of these chips have been fabricated and functionally tested. Ten of these chip types are being designed for the SUMC-DV computer which is an ultra-reliable modular computer being built by Advanced Technology Laboratories in Camden under contract. This LSI-array computer, which uses an instruction set selected from the set available with the RCA and IBM ground-based systems, and which has an operation code compatible with the RCA 215 aerospace-purpose computer, is a 16-bit parallel processor containing almost 20,000 transistors (equivalent to more than 5000 gates), not including its main memory, scratch pad, microprogrammed read-only memory and input-output interface circuitry. The complete computer system is packaged in a housing 12×10×10 inches. Table II contains a list of the chip types used in the SUMC-DV computer as well as their current status (Sept. 20, 1971).

Table II—CMOS arrays for LSI computer

Chip function	*No. of chips*	*No. of transistors*	*No. of gates*	*Status*
Microprogram ROM data register	14	300	126	Fabricated and tested
Multiplexer product remainder REG-MUX memory address system	8	350	111	Fabricated and tested
Multiplexed multiply-quotient register	4	300	112	Fabricated and tested
Adderlogic unit	10	400	147	Fabricated and tested
Scratch pad address and interrupt register	1	364	137	Fabricated and tested
Condition code-interrupt status register	6	448	178	Wafer probing
Adder logic and B operand multiplexer control	2	324	116	Masks completed
A operand MUX-control B operand MUX-control	6	220	71	Masks completed
Sequence control and iteration counter	2	336	115	In artwork cycle
Control for sequence counter	1	390	70	In artwork cycle
Total	54	18,282	6,519	

Fig. 9 shows the logic diagram for the 140×140 mil ALU chip, which performs both arithmetic and logic function in the computer. The diagram shows the logic partitioned into 70 standard cells, the equivalent of over 140 gates, as shown in the logic diagram. The dotted outline defines a standard-cell type plus the pattern number which appears in the dotted box. This partitioned logic, plus the net list showing connectivity, completes the preparation for the logic to proceed through the automatic artwork generation process using the design automatic programs. Fig. 10 is a microphotograph of one of the fabricated ALU chips. Fig. 11 shows the logic diagram for one of the multiplexer-register chip types which contains 50 standard cells and the equivalent of over 110 gates. Forty of these chips, each in a dual-in-line package, were delivered by EASD to a government agency under a contract. Twenty, type ATL002 multiplexed multiply-quotient registers' were also delivered to the government agency under the same contract. Fig. 12 shows a microphotograph of this chip. Fig. 13 is an oscilloscope presentation of the propagation delay from *clock-in* to *data-out*, as well as the minimum pulse width required to set the master-slave flip-flop. Loaded with a total of 20 pF, including the scope and package capacity, the average stage delay is about 13 ns with a minimum pulse width of about 26 to 30 ns required to latch the master-slave. These measured delays are consistent and predictable from the delay measurements made on the CMOS standard-cell test chip fabricated last year.

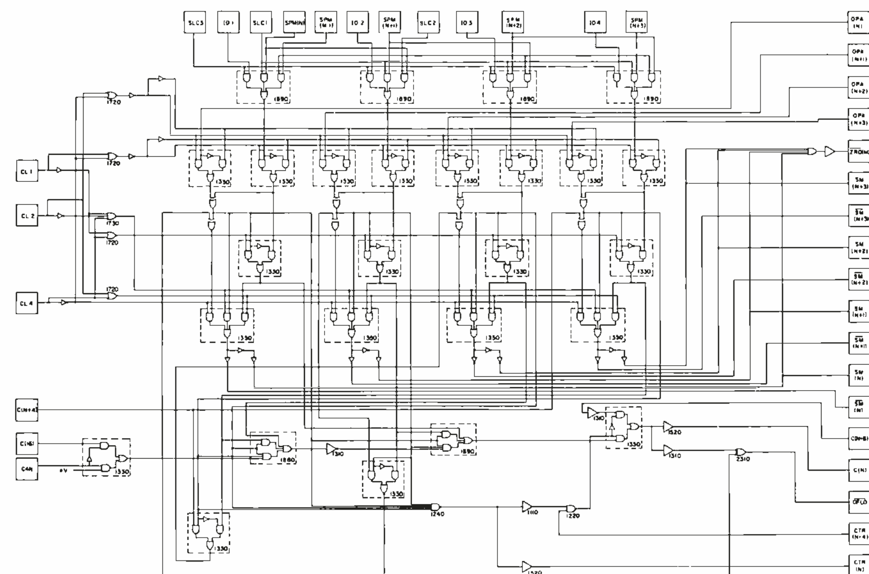


Fig. 9—ALU partitioned logic diagram.

Fig. 10—Microphotograph of fabricated ALU chip.

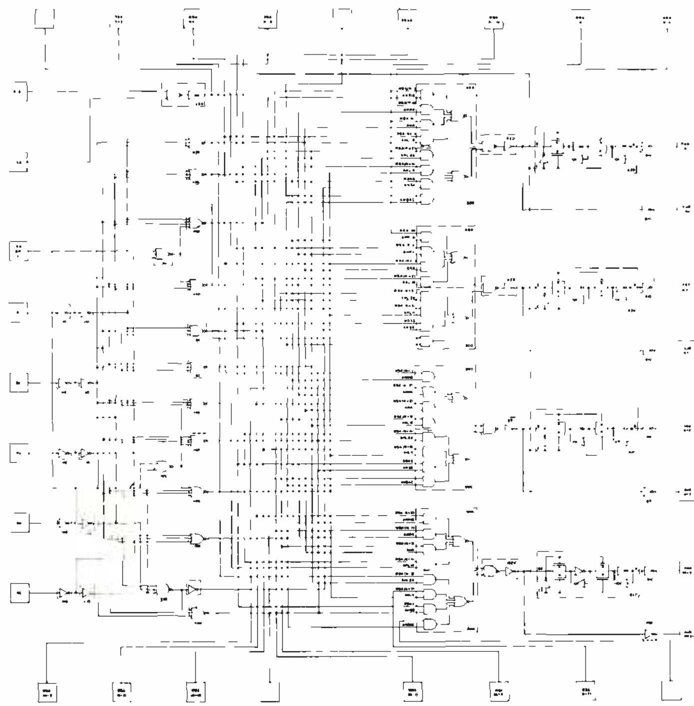


Fig. 11—Partitioned logic diagram for partitioned multiplexer register chip.

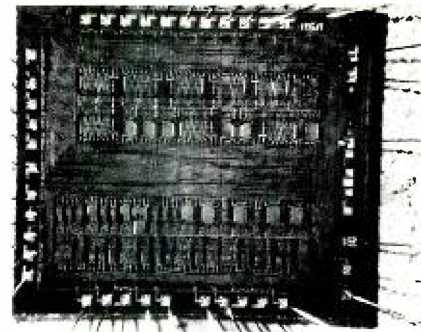


Fig. 12—Microphotograph of multiplexer register chip.

Improved program

At present, a new two-dimensional automatic placement and routing program is being developed that will significantly increase the efficiency and flexibility of these programs. This new program will incorporate automatic aids to reduce the need to make manual modifications in the area of pad and tunnel reassignments.

To generate CMOS arrays using the standard-cell technique, the user is required only to partition the logic in terms of the standard-cell family presented in Table I. Since this list is already extensive and rapidly growing, it is expected to satisfy most requirements. Therefore, once the user has partitioned the logic in terms of the standard cells according to the logic symbols shown in the data sheets for these cells and has properly defined a net list, the logic is then ready to pass through the CMOS standard array design cycle. More details are available by contacting the authors in ATL. Additional technical information is available.[7,8]

Conclusion

The standard-cell approach for generating CMOS custom cells was described. Using partitioned logic input, the system produces the mask artwork on Gerber automatic plotters using magnetic tape data developed primarily by the series of computer programs that constitute part of the standard-cell capability. The orientation of the pad location is optimized by manual modification to facilitate bonding and to move some wiring and/or tunnels that could influence electrical performance or have a dramatic effect on the area.

In general, however, the objective of the standard-cell technique is to provide low-cost, quick-turn-around artwork and arrays to make the cost of MSI and LSI custom CMOS arrays economically advantageous to the low-and medium-volume user. In addition, the capability for generating the artwork can be gained by the various divisions in a reasonably short time, giving the designers more effective control over the generation of the artwork containing the logic.

Over twenty custom CMOS chips, involving four RCA divisions, are now being designed by the standard-cell array approach. Nine of these chip types have been fabricated and tested. Ten are custom designed chips for a 16-bit parallel general-purpose LSI-array computer being built by ATL in Camden under a government contract.

Because standard-cell technology is an open-ended capability, present plans include expanding the cell family to include silicon gate CMOS capability, beam leads, and silicon-on-sapphire technology.

Acknowledgments

Because the past and present programs have involved so many different contributors from the several RCA locations, it may not be possible to properly acknowledge all who should be. Nevertheless, the authors would like to acknowledge the excellent cooperation of H. Weisberg, B. Levine and most especially F. Hunter of Solid State Division for his valuable assistance in providing fabrication and design guides to make this program possible. We also would like to acknowledge the excellent cooperation and performance of J. Scott of the RCA Laboratories who fabricated the wafers for the first test chip and I. Kalish, W. Lewis and C. Mulford Jr. of Solid State Division who processed subsequent wafers. A special note of thanks to R. Bergman, R. Geshner, H. Borkan, and T. Mayhew of the Government Microelectronics Technology group in Somerville for fabricating the masks and dicing, probing, and packaging the tested CMOS arrays.

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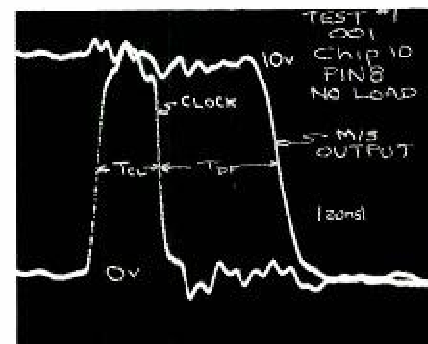


Fig. 13—Measured propagation delays on register chip.

Semiconductor IC technology

H. S. Miiller

The basic IC technologies being developed in the Solid State Technology Center at Somerville, N.J. are all within the framework of sealed-junction beam-lead structures, thereby enabling intermixing of IC technologies to achieve cost/performance system objectives. Not only is this optimization important in semiconductor memories, but the cost/performance advantages will impact in other areas of electronic systems such as cable-TV components, micropower electronic subsystems for space applications, hybrid UHF assemblies, and complex custom logic functions.

A MAJOR DETERMINATE of cost effectiveness and profit potential of large electronics systems is the speed with which the newest technologies can be applied in a meaningful and reliable manner. Toward this end, the role of the Solid State Technology Center, functioning in close cooperation with the major operating units of the corporation, is not only to develop advanced semiconductor devices and technologies but also to accelerate their implementation in advanced systems designs.

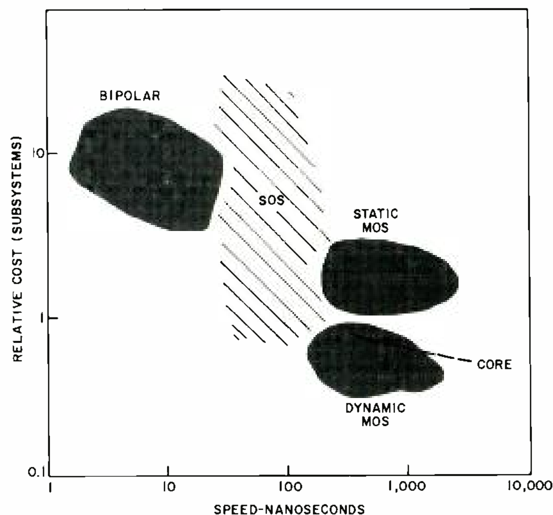
The basic approach adopted by the Semiconductor IC Technology Activity in achieving the required cost effectiveness and profit potential is to develop a technology for the fabrication of a wide variety of devices in the beam-lead, sealed-junction form. The beam-lead form permits the systems designer to maximize packing density for speed and cost and. more importantly, to optimize system performance.

For example, the realization of beam-lead MOS semiconductor arrays for computer memories is one of the major economic and technological advances awaiting exploitation. Beam-lead subassemblies[1] offer the technical advances of higher performance through higher packaging density and increased reliability. In terms of the total computer system, beam-lead subassemblies portend economic and system advantages not otherwise achievable. Some of the basic technologies that are being developed by the Semiconductor IC Technology activity in the beam-lead form include

1) Complementary MOS,
2) P-channel MOS with particular emphasis on main memories,
3) Silicon-on-sapphire, a low-power, high-performance MOS technology,
4) Bipolar, for high-speed digital and linear applications,
5) Schottky transistors, for custom circuit requirements, and
6) Linear MOS, for VHF and UHF applications.

This paper places these technologies in relative perspective, notes their unique attributes, and briefly reviews progress to date. Implications for future beam-lead systems are discussed.

Fig. 1—Memory technologies, 1973-1975



Memory technologies

The regularity of memory structures provides a convenient framework for comparing various semiconductor IC technologies. A comparison with regard to cost and speed is shown in Fig. 1. The MOS technology, because of the ideal, zero real-energy control characteristics of the field effect transistor, permits a wide range of memory applications. Fig. 2 illustrates some of the basic static and dynamic memory cells that can be fabricated.

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Table I—Simplified cost model for a typical main memory subsystem (K=1024).

	Subsystem	
Array size (bits)	1024	1024
Subsystem size (bits)	1024K	1024K
Individual storage array (Relative unit cost)	2	1
	Percentage cost	
Storage arrays	58	46
Array interface circuits	15	19
PC card and assembly	13	17
Interconnection platter	14	18
Total subsystem	100%	100%
	Relative subsystem cost (per bit)	
	1.3	1.0

Static MOS

Static cells, particularly those of the complementary MOS circuit form, provide the system designer with capabilities not achievable with dynamic cells. Complementary-symmetry MOS (COS/MOS) arrays can perform over wide extremes of temperature and power supply voltage with high noise immunity because the COS/MOS circuit form exhibits a sharp transition region in the transfer characteristic due to the push-pull operation of the complementary MOS transistors. Two COS/MOS 256-bit static memory arrays are being developed; RCA Dev. No. TA6042 provides for high performance applications using current sensing while the TA5974 exhibits a voltage sense output compatible with T^2L logic circuits.[2,3]

With the static circuit form of complementary MOS encompassing both the decoder and read-write control circuitry, these arrays exhibit a simplicity in system timing and electrical interface not presently obtainable with the dynamic MOS designs. Interface simplicity is assured by the single control signal required to operate the memory in either a read-write or read-modify-write mode.

Semiconductor main memories

In large main-memory applications, system economics require maximum utilization of storage array overhead. This overhead includes the array interface circuits, the printed circuit plug-in card, the interconnection platter, and the address and data bus distribution logic. In cooperation with Karl Mayer of the Memory Products Division, some simplified cost models of semiconductor main memories were developed.

As Table I indicates for one particular main memory organization, the storage arrays themselves contribute nominally only 52% of the total cost of the 10^6-bit memory subsystem. If power supplies, racks, memory timing and control units, etc., had been included within the bounds of Table I, the nominal percentage cost contribution of the storage arrays would have been diminished even further. Therefore, the greater the array storage densities are, the more efficiently the system overhead is utilized, and the lower the cost per bit of the subsystem. Table II illustrates this simplified economic principle, wherein the socket capacity of the printed circuit plug-in card, platter, etc., remains essentially constant while the number of bits contained in each dual-in-line package is varied from 64 to 2048. The systems modeled in Table II are projected as economically mature, normalized to the 1024-bit MOS array.

Dynamic MOS

Because fewer MOS transistors are utilized, the dynamic memory cells shown in Fig. 2 offer an immediate circuit approach to increasing the storage densities in main memories and thereby minimizing the cost per bit. With dynamic cells, the information is stored as either the *presence* or *absence* of charge on a capacitor and, because the MOS transistors are subject to small ($\sim 10^{-13}$ amperes) leakages, a periodic refreshing of the stored charge is required. Hence, the term *refresh memory* is derived.

Both the four- and three-transistor cells utilize charges stored in the parasitic capacitances of the MOS transistors (gate capacitance plus source and drain diode capacitance and the cell interconnect wiring). With the four-transistor cell, complementary charges are stored in the two node capacitances of the flip-flop, while with the three- and one-transistor cells, information is stored in a single capacitor as either presence or absence of charge.

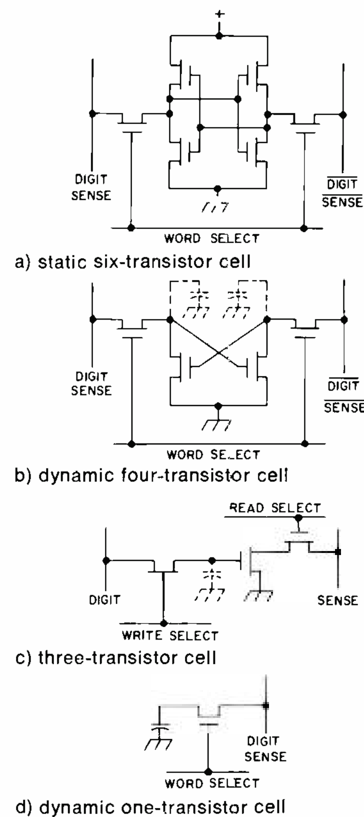


Fig. 2—MOS static and dynamic memory cells.

Two 1024-bit p-channel MOS dynamic memory arrays (RCA Dev. Nos. TA-6127 and TA6150) currently are being developed for main memory applications.[4] This effort is a joint program with the Memory Products Division of Computer Systems and is an excellent example of how the major operating units of the corporation can utilize the capabilities of the technology center.

The TA6127 employs dynamic address decoding to minimize power dissipation and is superior in performance, while the TA6150 employs a more

Table II—Simplified model illustrating the effect of storage density upon the per-bit cost of a main memory subsystem (K=1024).

	Subsystem			
Array size (bits)	2048	1024	256	64
Subsystem size (bits)	2048K	1024K	256K	64K
	Percentage cost			
Storage arrays	55%	46%	44%	26%
Array interface circuits	17	19	20	24
PC card and assembly	13	17	17	24
Interconnection platter	15	18	19	26
Total subsystem	100%	100%	100%	100%
	Relative subsystem cost (per bit)			
	0.63	1.0	3.8	11.1

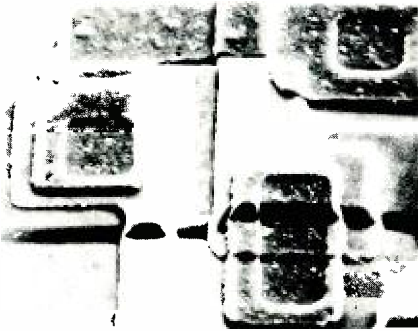


Fig. 3—Scanning electron microphotograph of the self-aligned, polycrystalline silicon MOS gate structure.

conventional static decoder. With static address decoding, the TA6150 is interchangeable with other 1024-bit refresh-memory arrays.

The three-transistor cell was selected for both designs over the four-transistor cells because of the higher sense output current and lesser sensitivity to processing parameter variations.

Fig. 3 is a scanning electron photomicrograph of the self-aligned, polycrystalline silicon gate structure being developed for these high-density MOS memory arrays. The length of a polysilicon gate structure is 0.2 mils; the resulting channel length is 0.14 mils, and a gate oxide is typically 1300 Å thick. Dynamic, three-transistor cell sizes range from 7.6 to 5.4 mils^2 as a function of design rules (mask alignment tolerances, metal widths and spacing, size of source/drain, and poly-silicon contact windows). In contrast, a COS/MOS static cell requires 19 to 15 mils^2 using the same self-aligned polysilicon gate design rules. The three-transistor dynamic MOS cell design retains a factor of two to three in storage density.

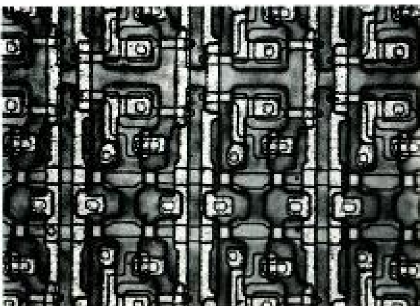
MOS silicon gates

The major attributes of the silicon gate MOS technology is both increased speed and circuit packing density. The speed advantage comes from the reduction of the overlap capacitance between the MOS gate metal and the source/drain regions. The self-aligned silicon gate structure eliminates this gate-source/drain overlap as well as minimizing mask alignment problems.

The packing density of MOS circuits using silicon gates is increased by virtue of having two levels of interconnection available. The polysilicon gate itself, typically doped to 35 ohms per square, can be extended up over the field oxides to form actual circuit interconnects. An additional 5000 Å of insulating oxide over the poly-silicon interconnects readily allows the use of second-layer metal interconnects.

Hermeticity, as required for the beam-lead arrays, is accomplished by a few thousand angstrom overcoat of silicon nitride prior to application of the beam-lead metal system.[5] Fig. 4 shows a PMOS memory array using the beam-lead metal interconnection system; 0.3-mil width and spacings are readily obtained.

Fig. 4—Beam-lead, silicon-gate PMOS memory array.



SOS technology

Silicon-on-sapphire (SOS) technology is being explored for its unique attributes of exceptionally low capacitance effects. With sapphire as an insulating substrate in place of the conducting silicon of bulk MOS, the source and drain device capacitance, parasitic wiring and inter-device capacitances, and the substrate gating effects are removed. Complex logic involving large series gating functions as well as higher MOS circuit performance can be achieved with SOS.

For example, the reduction in the source/drain capacitance of MOS transistors by a factor of 10-to-20 with SOS corresponds to a speed increase of 4-to-10 depending upon the circuit fanout (loading). Circuit speeds in ring counter configurations have been observed in the 1-picojoule, 2-ns stage delay range[6].

In illustrating the cost/performance enhancements to be achieved with SOS technology, a T^{2}L-compatible 256-bit complementary MOS/SOS memory array, RCA Dev. No. TA6142, is being developed in cooperation with RCA Laboratories. Functionally equivalent to the 256-bit COS/MOS array (TA-6042), this COS/MOS array has a factor of four increase in speed with a typical access time of less than 50 nanoseconds. Another CMOS/SOS array in development is the RCA Dev. No. TA6140, a seven-stage counter.

With low parasitic and device capacitances, SOS technology offers interesting potentials for exploring implementation of very high speed, very high-density, low-power memory and logic arrays not otherwise obtainable with bulk MOS technology.

Bipolar technology

Motivated by the need to increase packaging density, the bipolar technology is being directed towards higher performance, lower power circuits. For example, nearly 70% of the stage delay of a typical ECL logic gate within the computer environment is associated with wiring (capacitive loading, transmission line reflections, etc.). First efforts directed towards establishing circuit concepts and technologies required to overcome computer environmental delays and achieve 100-gate ECL logic arrays were worked on jointly by RCA and the Air Force in 1966; accomplishments were demonstrated with 144-gate arrays in the LIMAC computer in 1970.[7,8]

Table III summarizes the basic characteristics of the bipolar technology. The rate of improvement in the speed-power capabilities has been directly related to advances in photoengineering (diminished device geometries) and in a manufacturing capability to achieve increasingly stringent requirements on quality and control of the epitaxial layer. Major emphasis is being directed towards these improved materials and process techniques.

Circuit speeds are directly related to the various RC time constants present in basic device structures. For example, the base-emitter capacitance depends upon the emitter area and the width of the emitter-to-base junction depletion region. Smaller emitter areas and a decreased impurity concentration in the base region under the emitter are methods of decreasing this emitter capacitance.

Even though these process advances have been made, calculations indicate

Table III—Epitaxial bipolar technology characteristics

Year	*Technology*	*Characteristics*	*Speed-Power Products (picojoules)*
1966	LIMAC	0.5 ohm-cm 7-8 μm thick Reoxidized emitters	40-45
1970	Thin-epi	0.3 ohm-cm 3-4 μm thick Both reoxidized and non-reoxidized emitters	25-30
1971-72	Optimized thin-epi	1.0 Ω-cm 2-3 μm thick Non-reoxidized emitters	10-20
1973-74	Advanced thin-epi	1.0-2.0 Ω-cm 1-2 μm thick Non-reoxidized emitters	5-10

that the RC time constant associated with the epitaxial collector still dominates circuit transient time response and contributes nearly 70% to the delay and speed-power product. Further improvements will require a decreased thickness of the epitaxial layer and possible development of device isolation techniques other than a diffused p-n junction. The result is more stringent requirements on quality control of the epitaxial material and pocket diffusions.

Schottky bipolar transistors

The Solid State Technology Center has been engaged in the development of Schottky diode technology and device applications since its inception in 1970. This development program was coordinated with the RCA Laboratories, Princeton.[9,10] The bipolar sense amplifier (RCA Dev. No. TA6148) and the T²L/MOS level shifter (RCA Dev. No. TA6147) being built for dynamic MOS memories are first applications of this Schottky technology.[11]

A "saturating" circuit from such as T²L or T³L implemented with Schottky transistors offers significant improvement over a comparable circuit using the more familiar gold-doped technology. Gold doping has been used to control device saturation delays by forming recombination centers in the silicon, but at the cost of diminished β and increased leakage currents. In addition, the storage time of gold-doped transistors typically increases with temperature, whereas with Schottky transistors storage time remains essentially constant.

A convenient technique in constructing a Schottky transistor is to build the Schottky barrier diode across the base-collector junction as an integral part of the transistor structure. The diode clamps the base-collector junction so that the transistor cannot become forward biased sufficiently to inject minority carriers into the base and cause storage saturation. However, the increased base-collector capacitance resulting from the Schottky structure does increase somewhat the rise and fall times. But, when compared with the decreased storage time, Schottky T²L or T³L circuits exhibit an appreciably better ratio of delay time to rise time, leading to a more favorable system noise condition with Schottky than with gold-doped circuits at comparable system speeds.

The Schottky technology is a simple extension of conventional bipolar technologies; the base-collector clamp is formed as a rectifying metal-semiconductor contact by extending the base metallization over the high-resistivity ($N_d < 10^{17}$ atoms/cm) collector region. Aluminum metallization has a low metal-semiconductor work function (0.68 eV) and is ideal for Schottky transistors. Beam-lead metals, platinum and palladium, also can be used; the work functions are 0.85 eV (platinum silicide) and 0.75 eV (palladium silicide). Palladium silicide permits a wider range of clamping of the bipolar transistor at elevated temperatures than does platinum silicide. The TA-6147 and TA 6148 Schottky memory interface circuits are designed for fabrication with aluminum or beam-lead metallization.

Schottky barrier diodes are relatively insensitive to normal process parameter variations and impose no major deviations from the existing standard bipolar digital and linear processing.

Linear MOS technology

The MOS transistor is being used increasingly in conventional linear systems to perform the functions of RF amplification, mixing, demodulation, and oscillator signal sources. The MOS transistor exhibits better "linearity" than other solid-state transistors for processing signals in the presence of large interference basically because of improved square-law characteristics.

For example, the MOS dual-gate transistor exhibits a 10- to 20-dB greater tolerance to interfering signals in TV and FM broadcast receivers over a gain attenuation range of 40 dB in comparison to the performance of small-signal bipolar transistors under equivalent minimum noise conditions. A second example is the use of MOS transistors for quadrature mixing in the 30 to 80-MHz range, where extremely high dynamic range has been realized in prototype ECOM military receivers.

Typical performance characteristics of two VHF MOS dual-gate transistors are compared in Table IV. The 3N200 is

Table IV—Comparison of typical characteristics for the 3N200 transistor and the improved MOS dual-gate transistor RCA Dev. No. TA7801

Characteristic	*3N200*	*TA7801*
at 200 MHz		
Power gain	18 dB	22 db
Input resistance	1,000 ohms	600 ohms
Input capacitance	6 pF	9.5 pF
Output resistance	2,700 ohms	6.000 ohms
Output capacitance	1.5 pF	3.0 pF
Transadmittance	13 ∠−30° mmhos	20 ∠−33° mmhos
at 400 MHz		
Power gain	12.5 dB	16.5 dB
Input resistance	250 ohms	125 ohms
Input capacitance	6 pF	9.5 pF
Output resistance	1,700 ohms	3,000 ohms
Output capacitance	1.5 pF	3.0 pF
Transadmittance	12 ∠−60° mmhos	19 ∠−72° mmhos

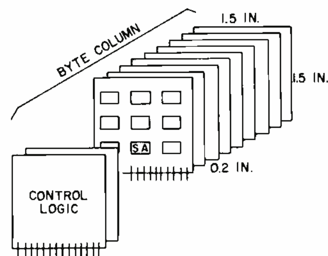


Fig 5—Byte column memory organization concept using beam-lead ceramic storage planes.

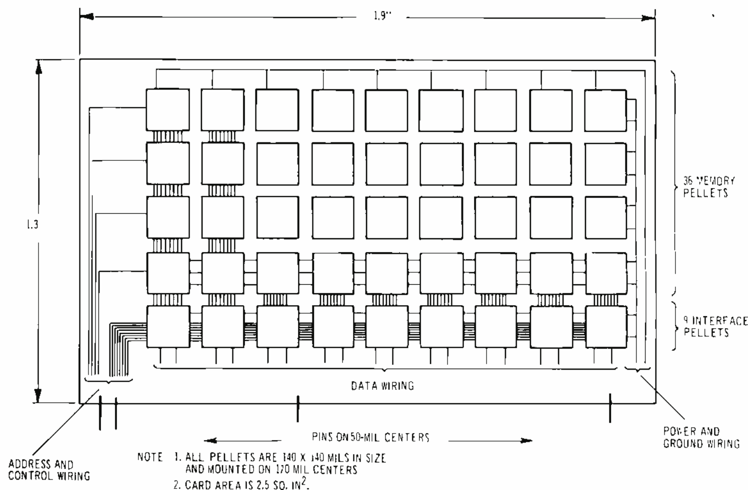


Fig 7—A ceramic memory plane being developed under joint sponsorship with the U.S. Air Force

a commercial product and is used for VHF TV and FM receivers as a replacement for high quality nuvistors. The RCA Dev. No. TA7801 dual-gate MOS transistor exhibits increased output resistance, lower input resistance, higher transconductance, and better high-frequency gain. It also has a potential for applications in the low UHF band. Both the 3N200 and TA7801 transistors have integrated back-to-back diodes for gate protection.

Recent RCA developments in the range of frequencies from 1 to 2 GHz with 1- to 2.5-micron channel length MOS devices indicate useful performance through the full range of microwave frequencies up to 10 GHz.

Characteristics of the RCA 2.5-micron channel length UHF MOS dual-gate transistors are shown in Table V. These structures are being developed in beam-lead form.

In addition to these discrete device applications, MOS linear IC's are being developed for use in the RF receiver field as well as to perform more complex functions in linear systems.[12]

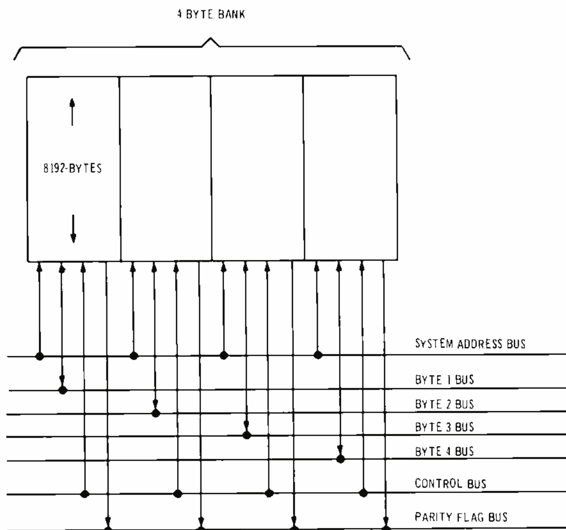


Fig. 6—Memory system modularity using beam-lead byte columns.

Beam-Lead Subassemblies

Beam-lead technology forms the literal bridge in combining the various IC technologies to achieve an optimum in cost-performance effective systems. For example, Fig. 5 schematically illustrates an organization for semiconductor memories wherein MOS storage arrays and Schottky bipolar sense amplifiers have been combined on beam-lead ceramic substrates to produce a 8192-word by 9-bit module. In Fig. 5, each 1.5-in^2 ceramic storage substrate contains eight 1024-bit arrays and one bipolar sense amplifier. A configuration of nine such storage substrate planes together with control electronics (address register, fan-out amplifiers, parity logic, etc.) comprises a logically self-contained memory module nine bits (one byte) in width; i.e., a *byte column.* For the byte column illustrated in Fig. 5, the storage density is 12,000 bits per in^3 and an entire column occupies 8 in.^{3} Fig. 6 illustrates how larger systems can be constructed by taking advantage of the modularity of the byte column.

Higher storage densities can be achieved. Fig. 7 illustrates a complementary MOS memory storage plane being developed under joint sponsorship with the Air Force.[13] Each RCA Dev. No. TA6234 storage plane consists of thirty-six 256-bit arrays plus MOS interface circuits, mounted on a 170 x 170 mil grid. The storage plane is organized as 1024 words by 9 bits, and a byte-column packaging density in excess of 20,000 bits per in^3 is achieved. With 1024-bits per array, the packing density conceivably can approach 100,000 bits per in^3. Thus, beam-lead subassemblies will permit semiconductor logic arrays and memories to achieve the maximum in storage densities with subsequent performance and cost benefits.

Table V—Typical characteristics of UHF MOS dual-gate transistors

Characteristics at 1 GHz	*Conventional bonded*	*Beam-lead bonded*
Power Gain	18 to 20 dB	14 dB
Bandwidth 3 dB	30 MHz	80 MHz
Noise figure	3.5 dB	—
Input resistance	800 ohms	800 ohms
Output resistance	5000 ohms	5000 ohms
Input capacitance	1.5 pF	1.5 pF
Output capacitance	1.5 pF	1 pF

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MOS devices for linear systems

R. H. Dawson | L. A. Jacobus
R. H. Brader

This paper discusses applications and the design theory of high-frequency MOS transistors and certain aspects of the design of linear MOS integrated circuits. In most of the applications discussed, the development of discrete MOS devices and IC's has taken place in an environment of interchange among circuit designers and designers at the Solid State Division. Over a period of approximately six years, these engineers have built a fundamental background and have become thoroughly familiar with the capabilities and limitations of MOS technology.

THE MOS TRANSISTOR, the solid-state analog to the vacuum tube, is being used increasingly in conventional linear systems for RF amplifiers, mixers, demodulators, and oscillator signal sources. The MOS transistor is attractive in these applications because it exhibits better "linearity" than other solid-state transistors for processing small signals in the presence of large interference. For example, the MOS dual-gate transistor exhibits a 10-dB to 20-dB greater tolerance to interfering signals in TV and FM broadcast receivers over a gain attenuation range of 40 dB in comparison to the performance of small-signal bipolar transistors under equivalent circuit conditions.[1] A second example is the use of MOS transistors for double-balanced mixing in the 30-MHz to 80-MHz range, where an extremely wide dynamic range has been realized in prototype broadband military receivers.[2]

Although current applications are in the VHF and low UHF range, recent RCA developments in the range of frequencies from 1 GHz to 2 GHz with 2.5-μm-channel-length beam-lead

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Authors Jacobus (left) and Dawson.

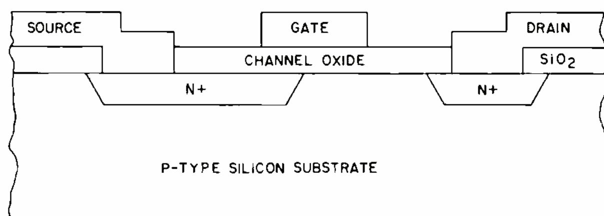


Fig. 1—Offset-gate MOS transistor.

MOS devices,[3] together with reported performance for 1-μm-channel-length devices with $f_{max}>10$ GHz,[4] indicate a remarkable potential through the full range of microwave frequencies. A combination of excellent high-frequency performance and linear transfer characteristics of these narrow-channel saturated-velocity devices should result in dynamic-range performance advantages for broadband systems, an area of application not heretofore addressed by MOS FET's. The use of beam leads for UHF MOS transistors results in effective and direct interface between strip lines and UHF circuit components such that parasitic elements are minimized, mounting and bonding are simplified, and maximum flexibility in use of substrate area can be obtained. These factors combine to provide an economically effective approach for obtaining high performance UHF integrated-circuit amplifiers.

In addition to discrete MOS devices, MOS integrated circuits are being developed for use in receivers as well as to perform complex functions in other linear systems. Many of these functions interface between digital and analog sub-systems. Two such examples are an MOS TV sync separator[5] and an MOS monolithic phase comparator[6] for frequency synthesizers. These examples demonstrate that a wide range of linear functions can be performed by MOS IC's acting as amplifiers, resistors, diodes, voltage dividers, threshold bias networks, DC-level controls, signal clamps, and current regulators. The ability of MOS transistors to perform so many complex functions stimulates demand for use of MOS IC's, particularly in applications where the unique properties of MOS transistors are advantageous; for example, to perform the sample-and-hold functions in the phase comparator circuit.

Discrete transistors

Historically, RCA has been a leader in MOS technology and MOS discrete devices. Starting with the work at RCA Laboratories where the first MOS transistors with passivated silicon surfaces were fabricated in 1963, RCA Somerville quickly developed a line of MOS triodes for linear-signal processing. The first of these discrete metal-oxide-semiconductor (MOS) transistors for high-frequency applications, the 3N98, was introduced by RCA in 1964. The early devices were useful up to 60 MHz and were fabricated using the offset-gate technique shown in Fig. 1. This type of structure substantially reduces the drain-to-gate capacitance below that obtained with a conventional, full gate structure. The 3N98 led to the development of the original 3N128 VHF amplifier device which was used at frequencies up to 200 MHz.

In spite of the attractively low feedback capacitance of the 3N98, difficulties with regard to surface-charge migration and power dissipation under AGC were experienced with the offset-gate approach. These early difficulties led to the implementation of a new technology (doped oxide)[7] and a new device (the dual-gate MOS transistor)[1], both of which were RCA contributions. The doped-oxide technology can be most clearly illustrated by its application to fabricate a full-gate triode with reduced feedback capacitance.

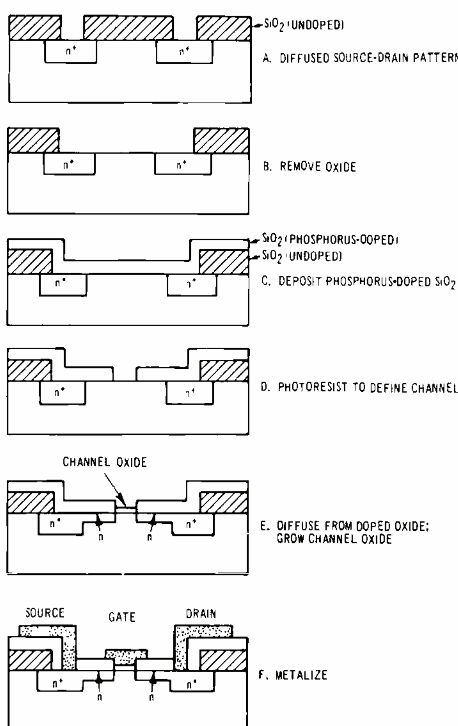
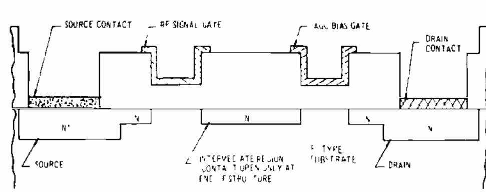


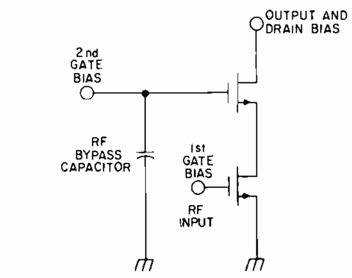
Fig. 2—Fabrication of doped-oxide MOS triode.

The fabrication steps for a doped-oxide MOS triode are outlined in Fig. 2. The essential feature of this process is that the channel pattern is defined (i.e., cut out from the doped-oxide, as shown in step D of Fig. 2) such that thick oxide steps align automatically to the channel edges. A shallow, controlled drive-in diffusion then is accomplished by using as a doping source the doped-oxides that abut the geometric channels. This diffusion from the doped oxide connects the edge of the channel to the heavily diffused contact regions, as shown in step E. The oxide step at the drain edge of the channel reduces feedback capacitance in accordance with the thickness of the oxide step relative to the channel-oxide thickness. Feedback capacitance typically is reduced by an order of magnitude. Implementation of this technology has led to development of full-gate MOS transistors with electrical characteristics equivalent to those with an offset gate. In fact, the 3N128 was redesigned to take advantage of the new technology and is still manufactured using this basic process.

The most significant development to date in the MOS linear field has been the MOS dual-gate transistor. This device (3N140), first introduced to the market by RCA in 1965, exhibits characteristics analogous to those of the vacuum-tube pentode. It has consequently been developed to replace high-performance nuvistors for TV and FM receivers. The dual-gate transistor is essentially composed of two MOS triodes integrated in tandem as shown by Fig. 3a. It is fabricated by the doped-oxide process, for which this process was first introduced to minimize parasitic gate capacitance as well as to minimize the junction area required to join the two MOS triodes. By using a narrow diffusion stripe and stepped oxides, the center-point capacitance of the structure is kept to a



a) Cross section



b) Cascode circuit

Fig. 3—Dual-gate MOS transistor.

minimum. In cascode circuits constructed of discrete devices, this capacitance, which becomes very large due to stray package capacitance, must be neutralized by tuning; however, in the integrated structure, its value is kept small enough so that an extra tuning element is not necessary.

When operated in the cascode mode as shown in Fig. 3b, the dual-gate transistor exhibits exceptionally low feedback capacitance, eliminating the need for neutralization. It also provides improved cross-modulation performance under gain control because the gain can be attenuated by reverse bias applied to the second gate. The input swing can be large without excursion into the cutoff region where severe nonlinearities occur. Due to its multi-gate control feature, the MOS dual-gate device can also be used for mixer and demodulator applications, where advantages are realized due to isolation between injection terminals.[8]

The extremely high input impedance of MOS transistors makes them susceptible to damage from static discharges which rupture the dielectric material insulating the gate from the channel. In most applications, the input circuitry provides considerable protection because only the in-band component of energy can cause damage. However, to allow for various handling conditions, and for ultimate in-use reliability, gate protection becomes clearly necessary for market acceptance. Protection from static discharges is accomplished by connecting a protective diode structure from the gate to ground to limit voltage transients to a value below the dielectric breakdown voltage of the channel oxide.[9] The basic requirement for the protective diode is that it should provide adequate protection from transient over-voltages while not significantly degrading the high-frequency performance of the MOS device.

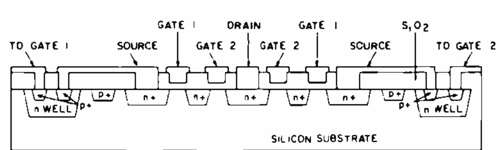


Fig. 4—MOS transistor-chip structure with protective diodes.

One approach to integrating protective diodes into an MOS structure is shown in Fig. 4. In this approach, the p-type silicon substrate required for an n-channel MOS device is the starting material. The n-type wells are diffused into the silicon to provide pockets for the protective devices. The surface concentration and depth of these wells are carefully controlled because both of these factors are important in determining the diode characteristics.

The p^+ regions are diffused into the n-type wells to form the diodes and around the periphery to isolate the diode structure from the rest of the device. The size of the diodes is determined by the desired current-handling ability and the amount of capacitance that can be tolerated across the gate of the MOS transistor. After the diode structures are formed, they are covered by a protective oxide. The rest of the MOS device is then fabricated by conventional means.

Fig. 5 shows a photograph of a completed monolithic diode-protected dual gate MOS transistor (3N200). The back-to-back diode structure allows operation of the device in either the depletion or enhancement mode, which gives the circuit designer an added degree of flexibility. It also provides minimum nonlinear influence due to nonlinear-capacitance-cancellation effects of the back-to-back diodes.

Device design

In the design of both MOS discrete devices and integrated circuits for linear application, equivalent-circuit modeling plays a very important role. The conventional representation of the MOS triode is by an RC input network, an output current-generator controlled by the gate-to-channel voltage, an output resistor, and, finally, feedback and other parasitic capacitances. This model is shown in Fig. 6a, where certain parasitic elements have been omitted for simplicity. The model describes quite well many of the high-frequency properties of MOS triodes, particularly with regard to the input parameters. Very good correspondence has been obtained when values evaluated by transmission-line analysis are utilized for these input elements.[10]

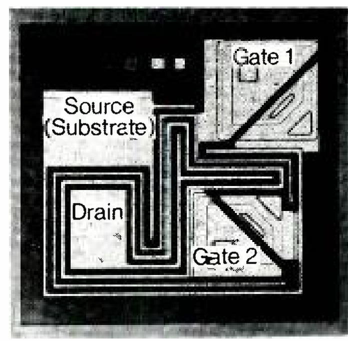
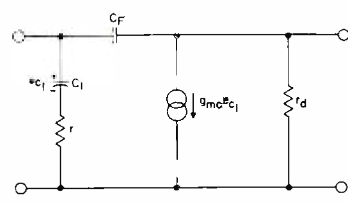
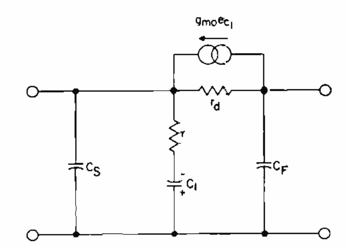


Fig. 5—Monolithic-diode-protected dual-gate MOS transistor as completed.

This simple model has been used to gain a great deal of insight to the properties of the MOS dual-gate transistor. To develop the dual-gate model, the common-source equivalent circuit of Fig. 6a is rearranged to represent the common-gate mode as shown in Fig. 6b. It can then be placed in tandem with the original common



a) Common source



b) Common gate

Fig. 6—MOS triode, equivalent-circuit models.

source model. One parasitic element, C_s, has been explicitly added to the common-gate model. This parasitic capacitance corresponds to the central-island diffusion capacitance of the MOS dual-gate transistor. Admittance parameters formulated give the essential properties of the cascode MOS dual-gate transistor. Even when these relations are determined in terms of the idealized equivalent circuit elements, they are generally unwieldy. A simplifying approximation that $(\omega C_g r_c) \ll 1$ limits the range of applicability to well below the cutoff frequency of the transistor; however, the VHF range is within the range of validity. It was further assumed that the triode distributed-channel resistance, r_c, is related to the transconductance by $r_c = 1/\alpha g_m$ where α is typically equal to 4 (ref. 10). Only the input and output conductances, g_{11} and g_{22}, the forward transadmittance y_{21}, and the feedback susceptance b_{12} are given here, because these parameters are most commonly used for tuned amplifier design. These parameters are summarized in Table I. The separate identities of common-source and common-gate elements are retained by using primed parameters for the common-gate elements.

The capacitance, C_T, contained in the expressions of Table I, is that capacitance to ground from the joining point of the common-source and common-gate components with the input short-circuited. C_T can be called a center-point capacitance, and it is composed of central-island capacitance, gate-overlap capacitance, and distributed second-gate active capacitance.

The low-frequency behavior, as well as some important high-frequency characteristics, can be determined from these expressions. The low-frequency input conductance, g_{11}, and the magnitude of the forward transconductance, y_{21}, are principally determined by the common-source unit; while the feedback susceptance, b_{12}, and the output conductance, g_{22}, are reduced from those of the common-source stage by the voltage amplification factor $g'_m r'_d$ of the common-gate stage. These characteristics lead to much greater low-frequency voltage gain than that obtainable with a single device. At high frequencies, the admittance parameters are influenced by center-point susceptive loading. The effect is first seen in the output conductance which increases in proportion to ω^2 at the corner frequency f_1 given by:

$$f_1 = g'_m / 2\pi C_T (g'_m r_d)^{1/2} \qquad (1)$$

The high frequency terms illustrate the effect of center-point capacitance. Minimization of this capacitance is a crucial design goal for optimum performance at high frequencies. A graphic representation of this loading effect is shown in Fig. 7 for the normalized output resistance of a MOS dual-gate transistor similar to the 3N200.

In addition to the inherent rolloff in output impedance and gain due to the effect of C_T, other parasitic elements play a crucial role in degrading the performance of high-frequency MOS devices. The major parasitic element is the drain-diode capacitance which must be charged through a substrate-spreading resistor[11] as indicated in Fig. 8. If the output charging is a simple time-constant system, then the device output conductance is given by:

$$G_O = g_{22} + \omega^2 C_d^2 r_{sd} / 1 + \omega^2 C_d^2 r_{sd}^2 \qquad (2)$$

where g_{22} is the ideal term of Table I, C_d is the drain diode-depletion capacitance, and r_{sd} is the substrate-spreading resistance. The effect of diode loading is represented in Fig. 7 by the dashed curves. There, diode loading dominates output resistance at high frequencies. With reference to Eq. 2, the output parasitic loading is, first of all, proportional to the square of diode capacitance; hence, reduction in diode area is highly desirable. The output parasitic load is, secondly, independent of homogeneous substrate acceptor concentration as detailed analysis indicates. Thirdly, it is a double-valued function of substrate spreading resistance, r_{sd}. The effect of r_{sd} can be reduced by using either an insulating substrate or a heavily-doped base, both having a thin, lightly-doped layer. With an insulating substrate, which can be obtained with silicon on sapphire, the diode capacitance can be reduced orders in magnitude while r_{sd} ideally approaches infinity. In practice, however, a layer of semiconducting material under the channel introduces a resistive element which prohibits realization of the full potential of this technique. In bulk silicon, a heavily

$$g_{11} \cong (\omega C_g)^2 r_c + \frac{\omega^2 C_{gd}\left[g_m C_T + g'_m\left(\frac{C_g}{a} + C_{gd}\right)\right]}{g'^2_m \left[1 + \left(\frac{\omega C_T}{g'_m}\right)^2\right]}$$

CONTRIBUTION FROM FIRST TRIODE DEVICE — CONTRIBUTION FROM SECOND DEVICE VIA FEEDBACK (C_{gd}) OF FIRST DEVICE

WHERE $C_T = (1 - \frac{1}{a}) C'_g + C_s + C_{gd}$

$$b_{12} = -\frac{\omega C_{gd}}{g'_m r'_d} \cdot \frac{1}{1 + \left(\frac{\omega C_T}{g'_m}\right)^2}$$

DC REDUCTION IN C_F BY μ' — VERY HIGH-FREQUENCY EFFECT

$$|Y_{21}|^2 = \frac{\left[g_m^2 + \omega^2\left(\frac{C_g}{a} + C_{gd}\right)^2\right]\left[g'^2_m + \omega^2\left(\frac{C'_g}{a}\right)^2\right]}{g'^2_m\left[1 + \frac{\omega^2 C_T^2}{g'^2_m}\right]}$$

$$g_{22} = \frac{1}{r_d (g'_m r'_d)} \left\{ \frac{1 + \left(\frac{\omega C_T}{g'_m}\sqrt{g'_m r_d}\right)^2}{1 + \left(\frac{\omega C_T}{g'_m}\right)^2} \right\}$$

Table I—MOS dual-gate admittance.

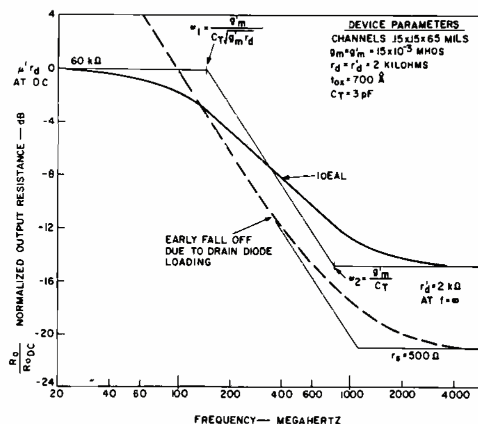


Fig. 7—Normalized output resistance vs. frequency for MOS dual-gate transistor.

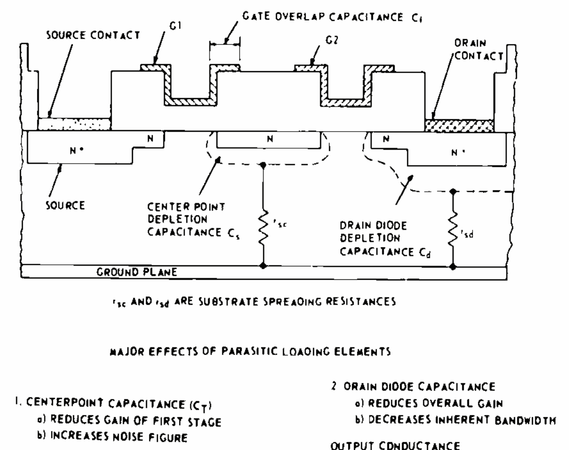
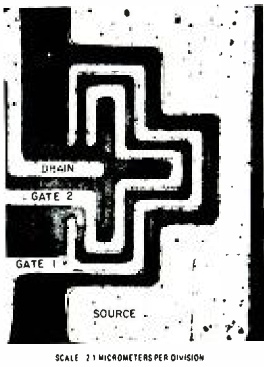


Fig. 8—Parasitic loading elements.



SCALE 2.1 MICROMETERS PER DIVISION

Fig. 9 (above)—Structure of dual-gate MOS transistor.

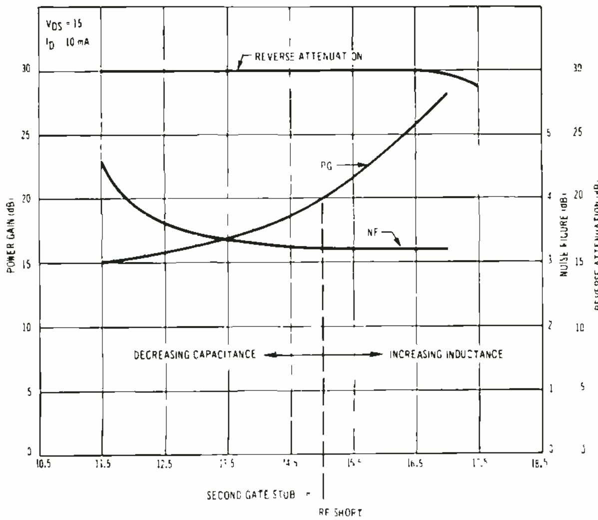


Fig. 10 (right)—Maximum available gain, reverse attenuaion, and minimum noise figure as a function of second-gate tuning at 1 GHz.

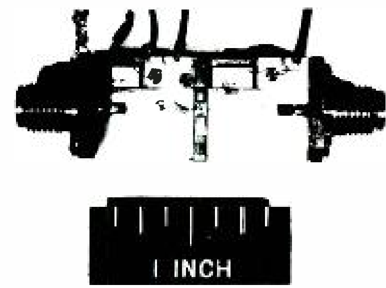


Fig. 11—Demonstration amplifier.

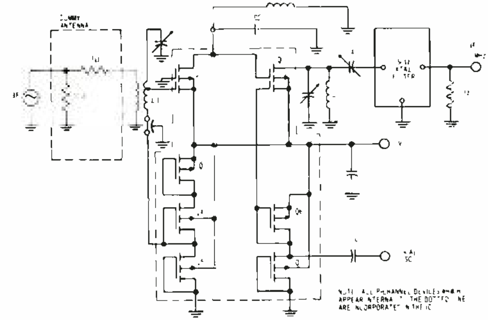


Fig. 12—Integrated MOS RF amplifier-mixer circuit.

doped substrate base reduces r_{sd} orders in magnitude, while C_d is held constant with proper choice of thickness and doping of an epitaxial layer. This latter technique has been used to make diode loading a negligible factor.

UHF dual-gate transistor

In accord with the discussion above, a UHF MOS dual-gate transistor was designed and fabricated. The basic structure is shown in Fig. 9. The features of this design are:

Small drain area,
Epitaxial substrate,
Reduced gate overlap capacitance,
Reduced central island capacitance,
Charge plane under electrode leads.

In addition to the design factors previously discussed, it has been found that a highly conductive region under the gate and drain electrode leads to substantially reduced input and output loss; this feature was incorporated. These design changes resulted in 1-GHz performance figures of 18- to 20-dB power gain with 3-dB bandwidth at 30 MHz with 30-dB reverse attenuation. Noise figures are 3.1 to 4.5 dB. These performance figures compare quite favorably to those of conventional structures which exhibited a power gain of 8 dB and a noise figure of 6 dB at 1 GHz. Measured performance is shown in greater detail by Fig. 10. These devices are packaged in TO-18 headers.

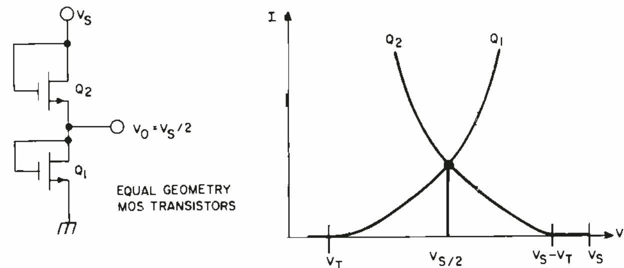
Relatively-high stray capacitance and very-high output resistance of 5000 Ω contribute to narrow bandwidth. Subsequent work has been directed toward utilizing beam leads on the UHF MOS structure to reduce parasitic capacitance by effecting direct interface between the device and the ceramic stripline UHF circuits. A microwave integrated-circuit amplifier which incorporates a beam-lead UHF MOS dual-gate transistor is shown in Fig. 11. This amplifier gives a 14-dB power gain with a 3-dB bandwidth of 85 MHz at a center frequency of 1.03 GHz. Although bandwidth is still relatively narrow, designs are being considered to increase the size of the structure, to lower the impedance values, and to increase device capacitance relative to parasitic capacitance.

MOS linear IC's

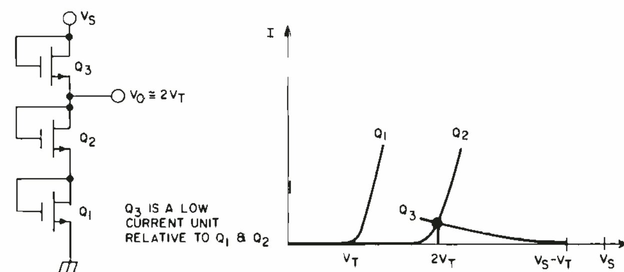
RF amplifier-mixer

The integrated RF amplifier-mixer shown in Fig. 12 serves to bridge the gap between MOS discrete devices and monolithic IC's. This IC was designed as an experimental circuit for the U.S. Army Electronics Command (ECOM) for 30-MHz to 76-MHz high-dynamic-range FM receivers.[12] The frequency band is divided into three channels (an IC for each), while each front-end circuit is narrowband tunable with external high-Q varactors and coils. The circuit, which consists of seven MOS devices, uses MOS dual-gate structures for both RF amplification and mixing. The necessary gate biases are obtained through two MOS bias networks. This circuit illustrates use of a number of attractive MOS features:

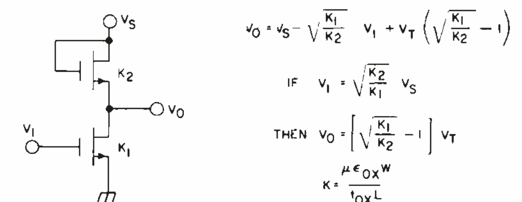
The dual-gate devices can be used for multiple functions (i.e., amplifier and mixer),
Excellent RF performance: high gain, low noise, excellent RF stability without



a) Voltage divider.



b) Integral threshold-voltage multiplier.



c) Non-integral threshold-voltage multiplier.

Fig. 13—MOS bias-produced networks.

neutralization or degenerative feedback,
Relatively simple fabrication,
Ease of DC coupling and biasing,
High packing density.

The first type of bias configuration used is a simple MOS voltage divider shown in Fig. 13a. It is composed of two equal-sized MOS devices in series with the gate of each tied to its drain; it simply divides the supply voltage in half. This network is used to bias the first gate of the MOS dual-gate mixer where the oscillator signal is injected. This type of mixer can tolerate a wide bias range for nearly constant conversion gain; therefore, variation in supply voltage does not strongly influence conversion gain. Furthermore, injection of the local oscillator signal through the midpoint of the bias network does not lead to distortion because the nonlinearities of these two high-impedance bias devices cancel.

The second type of bias configuration is the threshold bias circuit of Fig. 13b, which biases the first gate (signal input) of the dual-gate RF amplifier. This network supplies a bias voltage of two threshold-voltage increments (independent of supply voltage variations), and it ensures relatively constant current and gain for moderate variation in threshold voltage due to oxide thickness variations. Significantly, the RF amplifier and mixer are directly coupled, with identical drain and second-gate voltages, resulting in circuit simplicity. This direct coupling is possible as a consequence of the use of enhancement-MOS transistors.

The experimental RF amplifier-mixer integrated circuit has been evaluated in a typical military FM receiver between 30 MHz and 76 MHz. The circuit exhibits a sensitivity of 0.35 μV at both 30 MHz and 76MHz for a 10-dB signal-plus-noise/noise ratio at the audio output. The power gain and dissipation are 34 dB and 100 mW respectively for a 9-V supply at both 30 MHz and 76 MHz; power gain and dissipation are 31 dB and 35 mW with a 6-V supply. Interfering signals, removed by 10% from the desired channel frequency, of at least 122 dB above the reference level are required to degrade the 10-dB signal-plus-noise/noise ratio to a 6-dB value. Although this simple circuit provides relatively good performance, greater dynamic range is desirable for military receivers.

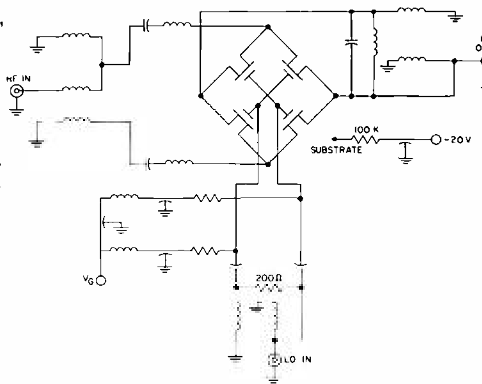


Fig. 14—Double-balanced mixer circuit.

Double-balanced mixer

A significant improvement in the dynamic range of mixer circuits has been achieved using MOS field-effect transistors in the double-balanced switching mixer circuit[13] shown in Fig. 14. The local oscillator signal alternately turns the opposite pairs of transistors *on* and *off*. This circuit is a double-pole double-throw reversing switch that changes the direction of flow of the RF signal through the load at the local-oscillator rate, causing the formation of the sum (RF + LO) and difference (RF − LO) frequencies. One of these signals is the IF frequency.

The advantages of the MOS/FET in this circuit stem from its being a three-terminal bilateral device. The symmetry requirement of the switching device is apparent because the source and drain terminals effectively exchange positions in the reversing switch process. The three-terminal nature of the device allows separate handling of the RF, LO, and IF signals, which is convenient for adapting the design to various applications.

Operation of the mixer for low conversion loss and high dynamic range requires a large local-oscillator signal on the gates of the MOS devices. Low conversion loss is essential to obtain adequate sensitivity for use as a front end without a preceding amplifier stage. Square-wave switching is desired so that the switches spend a very short period of time in the transition region between *on* and *off*. A sinusoidal drive is most easily obtained and will approximate square-wave switching if the signal has an amplitude of 10 volts or greater. This large local-oscillator drive is essential to realize the dynamic-range advantages of this circuit. The LO signal must be larger than the largest RF signal which must be handled linearly, because extremely large RF signals will tend to interrupt the local oscillator switching rate and degrade performance. The mixer also displays excellen intermodulation, cross-modulation, and spurious-response performance; this excellent performance is attributable to the constant off-state capacitance (i.e. no voltage dependence) that is brought about by the back-to-back diodes appearing across the signal paths.

This mixer has largely been limited to low-frequency applications because high-switching-rate MOS devices have not been available. In attempting to extend the operable frequency range of this circuit to 100 MHz and possibly above for the 30 MHz-to-80 MHz ECOM application,[2] certain factors about improved MOS device performance were intuitively obvious:

1) The device should be symmetrical so that the source and drain can be interchanged.
2) Input and output capacitances, as well as other parasitic capacitances, should be minimized to give optimum switching speeds.
3) The substrate terminal should be accessible for reverse biasing to prevent forward-bias of the MOS source and drain diodes under negative voltage.
4) The transistors should be closely matched in device characteristics to maximize circuit balance.

Additional requirements on the devices have been established in the course of developing a suitable transistor and include:

1) Channel-*on* resistance should be much less than the load impedance of the circuits to minimize conversion loss.
2) The drain-source breakdown voltage should be high to minimize degradation of dynamic range due to device breakdown.
3) The gate-input impedance should be high to minimize local-oscillator power drain for applications where power is a restriction. The gate circuit can be LC tuned to give maximum voltage for a small LO power.

Table II—Measured performance of MOS FET front end.

Frequency range	30 to 80 MHz
Noise figure	7.0 to 9.6 dB
Third order IM distortion	94.5 to 108 dB referenced to −112 dBV
2-db compression level	25 to 34.5 dBm
Pump power	4 to 6mW
DC power	192 to 285 mW, includes: 44 mW for IF 35 to 45 mW for VCO 112 to 200 mW for tuned pump amplifier

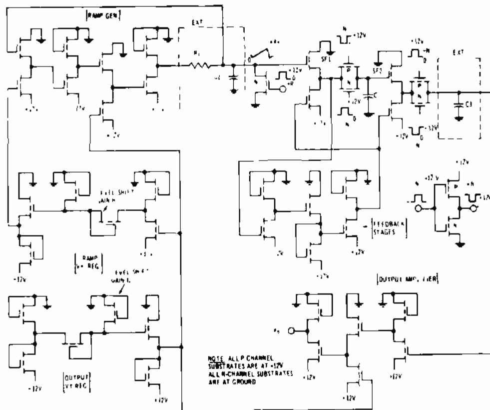


Fig. 15—COS/MOS phase-comparator circuit.

4) The gate capacitance should be minimized to maximize the LC tuning ranges of the gate circuits.

An MOS transistor was developed that exhibited a very good combination of the characteristics identified. A complete VHF electronically tuned FM front end was developed using this device in the double-balanced mixer circuit. The model included the mixer, preselector filtering, low-noise IF amplifier and voltage-controlled oscillator. The performance of this tuner is given in Table II. This performance represents at least a 20-dB increase in dynamic range over previous receiver front ends. Subsequent work has been directed toward development of an IC approach to enhance device balance and to simplify assembly.

Monolithic phase comparator and TV sync separator

Many of the conventional analog functions of linear systems are increasingly being digitized, such as control circuits and in-line signal processing, through use of sampling and statistical reconstruction. There is, therefore, an increasing need for circuit functions to interface between analog and digital subsystems. The MOS IC's will play a formidable role in this area as well as in the purely digital functions.

An example of this type of interface is the MOS phase comparator designed for use in a phase-locked loop in UHF digital frequency synthesizers developed for the U.S. Air Force.[6] The circuit of a monolithic MOS phase comparator is shown in Fig. 15. This circuit is used to control precisely the local oscillator frequency to desired channels in a transmitter/receiver. The design of the phase comparator circuit makes use of the following principles:

COS/MOS transmission sampling gates for low feedthrough sampling pulses and zero offset.
Capacitor storage for sample-and-hold functions,
MOS constant-current source for ramp generation,
MOS bias networks (threshold, level shifting, voltage dividers),
MOS DC voltage level networks,
MOS unity-gain amplifiers,
MOS amplifier with gain functions determined by computer aided design.

The phase comparator circuit, which is in the design stage, is an excellent vehicle for illustrating the complexity of functions that can be performed using linear MOS design principles.

The scope of linear functions that can be performed by MOS IC's is illustrated by a prototype TV sync separator shown in Fig. 16. In addition to functions previously described, this circuit uses MOS transitors to act as resistors, diodes, and signal clamps. One particular bias network used is illustrated in Fig. 13c. This network provides a technique for establishing non-integral multiples of threshold voltage. Implementation of MOS transitors whose threshold voltages vary with processing and temperature requires design of networks that track with threshold.

Conclusions

The MOS transistor has been used to advantage for linear signal processing in relatively narrowband systems. Exploratory work to extend bandwidth and field of application is being continued. The MOS IC's have shown a potential to perform complex functions similar to their bipolar-IC counterparts. Consequently, where the unique properties of MOS transistors can be used to advantage, the linear IC designer will find the MOS transistor a useful tool.

Acknowledgments

The authors are grateful for the work of many of their colleagues who have contributed to development in the linear MOS field. In particular, J. O. Preisig, S. Katz, and W. Donoghue have formulated many of the circuit designs discussed. L. S. Baar and S. Reich have done much of the application work with commercially available MOS transistors. P. Delivorias designed the double-balanced mixer-transistor photomasks. Strong support in receiver techniques was given by C. T. Shelton and E. D. Menkes of Government and Commercial Systems, and support with microwave IC's was given by Dr. D. Stevenson, RCA Laboratories. Most of the development work discussed was supported by the Air Force Avionics Laboratory, Air Force Systems Command, U.S. Air Force, and by the Integrated Electronics Division and the Communications and Data Processing Laboratory of the U.S. Army Electronics Command; the continued support of these agencies is gratefully acknowledged.

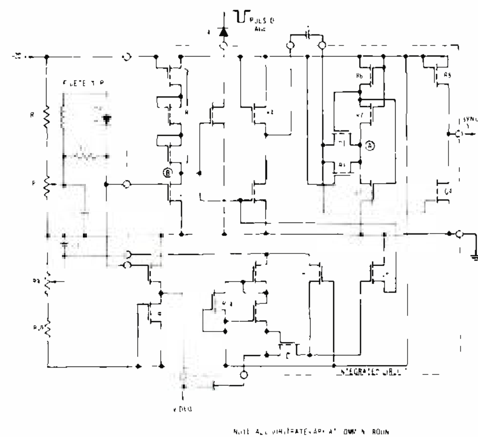


Fig. 16—TV sync separator.

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Semiconductor arrays for mass memories

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Silicon gate P-MOS technology has a direct application in the design of random-access memories. Solid state memory systems can be built from 1024-bit RAM chips which use P-MOS three-transistor cells as their basic storage units. As advances in processing technology and design techniques make more complex chips economically feasible, solid state memories will provide a formidable economic and performance challenge to present ferrite memories.

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Recent advances in solid state technology have made possible semiconductor memory devices which, for large memories, are competitive at the systems level with ferrite-core memories on the basis of price, performance, and freedom of organization.

MOS memories use either static or dynamic storage cells. Static cells generally utilize feedback-type latching circuitry for storage, whereas dynamic cells use charges stored on low-leakage parasitic capacitances within the cell. Because some capacitor leakage is inevitable, it is necessary periodically to restore, or "refresh", the logic state of a dynamic MOS storage cell.

Dynamic MOS memory devices usually are faster and dissipate less power than do static devices. In addition, the number of cells in a given area of silicon is significantly greater for dynamic storage devices, thus providing an inherently lower cost per bit at the component level. Although dynamic memory devices do require refresh-support circuitry and clocking for proper operation, this disadvantage becomes less important as the size of the memory system increases.

Selection of a memory cell

The bistable flip-flop, made up of two cross-coupled inverters, has been the most widely used basic storage cell for static MOS and bipolar circuits. The circuit of a static P-MOS storage cell is shown in Fig. 1. This cell works as follows. Transistors Q_1, Q_2, Q_3, and Q_4 form the flip-flop. Storage cells are accessed through transmission gates Q_5 and Q_6 which are controlled by the row-select line. When the cell is to be read, the row-select line turns on Q_5 and Q_6, transferring the stored bit from the flip-flop to the data lines. To write, Q_5 and Q_6 are turned on and the data lines are forced to the logical value desired, thereby overriding the contents of the cell. For P-MOS transistors, supply voltages to V_{DD} and V_{GG} are negative with respect to V_{SS}. These first two voltages can be identical or different, depending on the particular design, but V_{GG} is always equal to or greater than V_{DD}. The use of a common V_{GG} supply results in smaller cells but necessitates greater standby power in the period when the cell is not being accessed. The major disadvantages of a static bistable flip-flop are high power dissipation and the relatively large silicon area required per cell. The latter disadvantage limits the number of chips that can be economically produced on a single silicon wafer.

Numerous new storage cells have been developed to overcome the shortcomings of the basic static-storage flip-flop. The simplest way to reduce power dissipation in a static cell is to replace V_{GG} with a clock. Thus, Q_3 and Q_4 of Fig. 1 are on during the negative period of the clock pulse. But when the clock is positive the load elements Q_3 and Q_4 turn off, thereby reducing power dissipation. Junction and gate capacitances of the cross-coupled flip-flop act as a storage element. This storage of a charge on a parasitic capacitance in dynamic memory cell operation achieves low power dissipation and high packing density. A parasitic leakage path through the reverse-biased p-n junction, however, will eventually degrade the stored bit. Hence, the charge stored in the cell must be refreshed periodically.

Dynamic three-transistor cell

The use of a charge stored on parasitic capacitance makes a flip-flop unnecessary in a memory cell. A single transistor, whose gate is used as a storage node, can be used as a memory cell. Two additional transistors are needed to write information and read the logic state as shown in Fig. 2a. Thus, three transistors are sufficient for a basic memory cell. In the figure, transistor Q_1 acts as a storage element, and transistor Q_2, whose gate is connected to the read-select line, couples Q_1 to the read-data bus. The READ-SELECT signal then permits sensing of the logical state of the cell. The inverted state of the charge stored at the gate of Q_1 appears on the read-data bus. Q_3 is a transmission device which connects the write-data line and the gate of Q_1. The gate of transistor Q_3 is connected to the WRITE-SELECT signal, and a bit is written into the cell by turning on Q_3. Transistor Q_3 also helps in refreshing the memory bit periodically. Some

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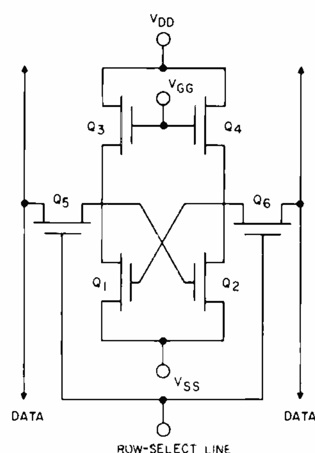
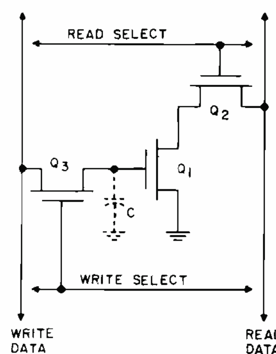
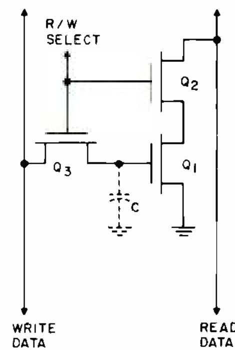


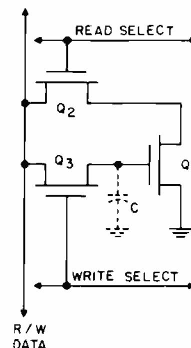
Fig. 1—Six-transistor static memory-cell circuit.



a) Cell for individual function buses.



b) Cell for common read/write-select bus.



c) Cell for common read/write-data bus.

Fig. 2—Three-transistor dynamic memory-cell circuits.

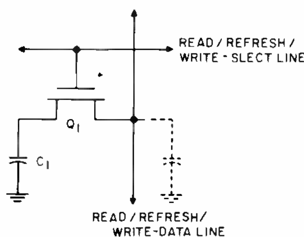


Fig. 3—One-transistor dynamic memory cell.

of the major advantages of this three-device memory cell are:

—Small cells,
—Low power dissipation,
—High speed, and
—Fewer contacts per cell.

Some alternative three-device cell configurations are shown in Figs. 2b and 2c.

Dynamic single-transistor cell

Fig. 3 represents a basic dynamic charge-storage cell consisting of a single p-channel MOS device and a single small capacitor used to store a bit. Parasitic capacitance of the read/write/refresh-data line and the storage capacitance are coupled by transistor Q_1, whose gate is connected to the read/write/refresh-select line. Turning on Q_1 permits reading, writing, and refreshing the stored bit. The bit stored is lost during read and refresh operations by charge redistribution on the data bus because, at the beginning of each cycle, the read/write/refresh-data line is discharged. The low-level signal on the read/write/refresh-data line is amplified and fed back to the memory cell. Hence, a special non-inverting data amplifier is needed. Moreover, the value of C_1 is restricted by the cell size and the need for high packing density.

1024-bit RAM

The RCA Dev. No. TA6127 dynamic RAM shown in Fig. 4 is organized in a 1024-word by one-bit configuration and uses the three-device storage cell shown in Fig. 2a. As shown in Fig. 5, the storage elements are arranged in a 32-row by 32-column matrix, and cells are accessed by coincident selection of one of 32 rows and one of 32 columns. Each of the rows and columns is driven by a dynamic decoder/driver circuit utilizing the basic NAND/NOR circuit shown in Fig. 6. The input to the decoder portion of the circuit of Fig. 5 is obtained directly from the address input or from the address complement derived from the output of the address inverter. Address inputs A_0 through A_4, and their complements, are dedicated to row selection, whereas the remaining five most significant addresses control the column selection. In addition to the ten address inputs, the device requires three power-supply connections and three control or clock inputs which are designated *CE* (chip enable), *R/W* (read/write), and *P* (precharge). Bits are entered to the individual cells via the D_{in} line and output current sensing is performed at the D_{out} terminal.

P′ clocking is sufficient for dynamic operation of the row-decoder/driver, but both *P′* and *CE* clocks are necessary to operate the column-decoder/drivers. A *P′*-clock signal is required for each memory cycle in order to perform read, write or refresh operations. *CE* clocking and *R/W* clocking, in addition to *P′*, are required for the write operation, whereas the read operation requires only *P′* and *CE*. The refresh cycle is identical to the write operation except that the *CE* line is inhibited during refresh. Because the column-decoder/driver requires *CE* for proper operation, column decoding does not occur during a refresh cycle. During a write cycle, the cells in the selected row and unselected columns are refreshed. During a single refresh period, the 32 cells in the selected row are refreshed simultaneously. In refreshing the entire chip, each of the 32 rows is accessed at 60-μs intervals by changing the logic state of the row-address inputs A_0 through A_4.

The TA6127 is designed so that device dissipation may be reduced to essentially zero in an idling, or standby, mode. In the standby mode, the *P′* and address inputs are held in an *off* state. Troublesome bipolar injection in the MOS circuits is controlled by substrate biasing.

Single-cell size achieved by the silicon-gate technology is 7.5 mil². The chip size is 141 mil x 145 mil. The chip can be sealed in a standard 18-pin dual in-line package.

Circuit operation

The RCA Dev. No. TA6127 utilizes dynamic on-chip decoder/drivers for row and column selection. The circuit diagram of the row-decoder/drivers in Fig. 7a shows that the five-input NOR gate is driven by an address or address complement. At the start of a cycle, the *P′* clock goes into the *off*, or most positive state, turning off Q_{15}. *P* is applied to the gate of Q_9, thus charging the node at the source of Q_9 as well as other circuitry controlled by *P*. In addition, the node at the drain of Q_1 will also charge if the row-address is in the *off* state. In practice, the address inputs must be valid before *P′* goes to the *on* state to ensure that the node at the source of Q_2 has sufficient time to charge to a full on-level. When *P′* goes negative, Q_{15}, Q_{10}, and Q_8 turn on; Q_2, Q_{13}, and Q_9 turn off; and drain voltage is applied to Q_{12}. If one or more of the decoder transistors, Q_3 through Q_7, is on because of an address or address complement, the node at the drain of Q_8 will discharge, preventing turn-off of source-follower Q_{12} and thus inhibiting access to that particular row. If decoder transistors Q_3 through Q_7 are off, Q_{12} will turn on, and the read-access voltage is applied to all the cells in the row. Writing to a selected cell is accomplished through source-follower Q_{11}.

The column-decoder/driver, shown in Fig. 7b, operates in a similar fashion except that *CE* acts on the drain voltage for source-follower transistor Q_{16}. Each of the three operating modes of the memory—read, write and refresh—is described below.

Read cycle

The TA6127 may be operated in a continuous read cycle by inhibiting the READ/WRITE pulse. The bit movement from one memory cell to Data Out is as follows in Fig. 8.

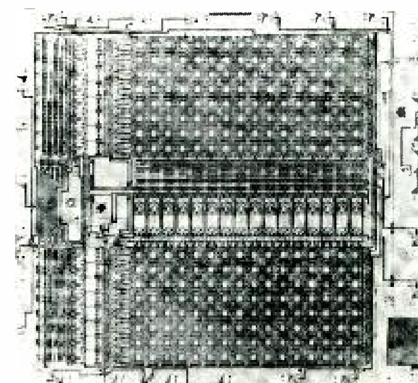


Fig. 4—Photomicrograph of 1024-bit RAM.

1) The charge stored on parasitic capacitance C determines the state of Q_1.
2) The PRECHARGE signal turns Q_4 and Q_5 on at the beginning of the cycle. Parasitic capacitances associated with the read- and write-data lines are charged.
3) The PRECHARGE signal turns off, allowing the row-select line to turn on transistor Q_2.
4) The logical state of the memory capacitance C determines the state of the read-data line. (Only if C is charged does the read-data line discharge).
5) The read-data line couples the inverted cell bit to the sense-amplifier input through Q_{10}.
6) Q_{11} and Q_{12} are turned on by the column decoder and by CHIP ENABLE; the logical state stored in the cell is nondestructively transferred to Data Out.

The READ timing diagram is shown in Fig. 9a.

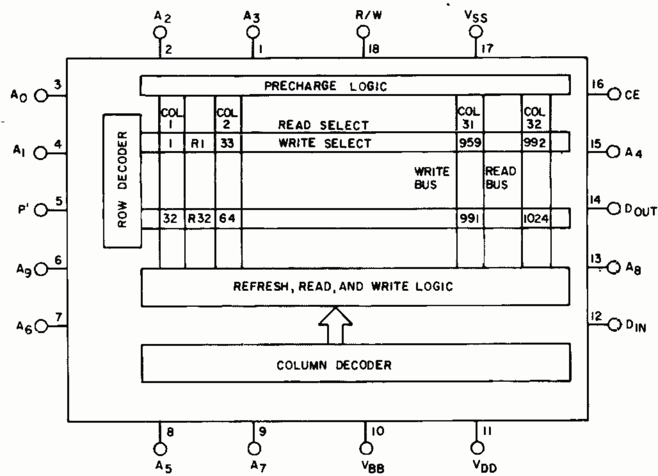
Refresh cycle

Dynamic MOS circuits take advantage of the very low leakages of the gate and junction capacitances. In the three-transistor cell, a bit is stored on the Q_1 gate parasitic capacitance, which usually exhibits time constants ranging from a few milliseconds to seconds. Hence, a periodic refreshing is needed to restore the bit stored in a cell. Under worst-case voltage conditions, and at an elevated ambient temperature of 70°C, a bit will remain stored for a minimum of 2 ms. Thus, the refresh cycle must occur at least every 2 ms.

A refresh cycle must be performed for each of the 32 rows of cells; a total of 32 refresh cycles is needed, therefore, to completely refresh the chip. CHIP ENABLE is inhibited during the refresh cycle. The REFRESH timing diagram is shown in Fig. 9b.

Bit flow from a memory cell (Fig. 8), and back to the memory cell, is as follows:

1) The stored bit is inverted and transferred to the read-data line, as in the read cycle.
2) The READ/WRITE control pulse turns Q_7 and Q_3 on. The write-data line discharges if C is not charged; otherwise, it will remain charged if C is charged. Discharge of the write-data line occurs through Q_6 and Q_7.
3) Because Q_3 is on, the bit stored in the cell is refreshed.
4) CHIP ENABLE is inhibited during the refresh operation; hence, a bit can neither be written into nor read out of the cell. In the WRITE cycle, only the



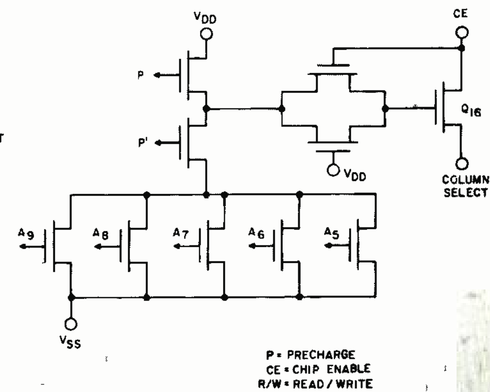


Fig. 5 left)—1024-bit memory organization.
Fig. 6 (above)—Basic NAND/NOR-gate decoder circuit.

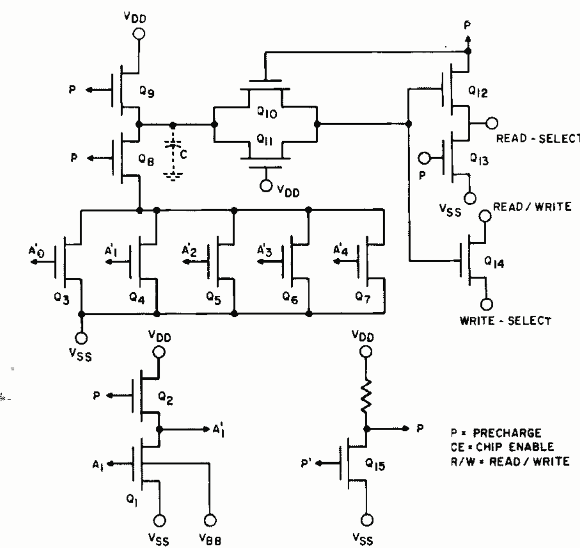


Fig. 7a (left)—Row-decoder/driver.

Fig. 7b (above)—Column-decoder/driver.

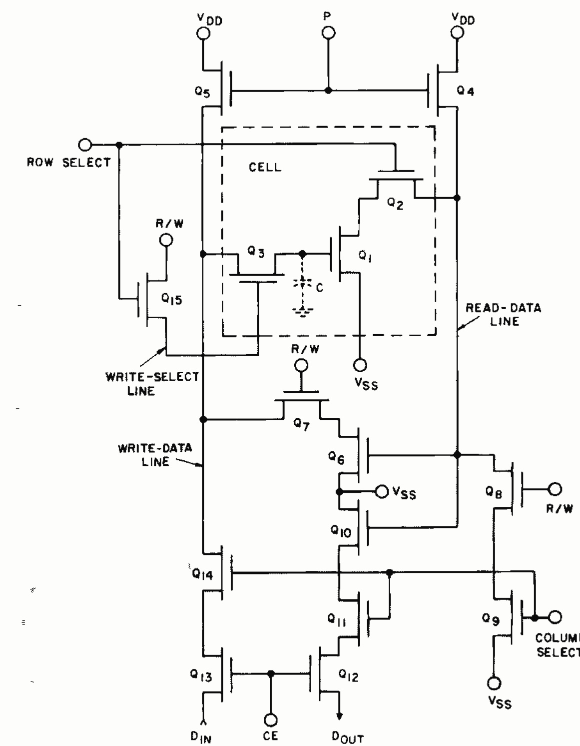


Fig. 8—Memory cell and auxiliary circuits.

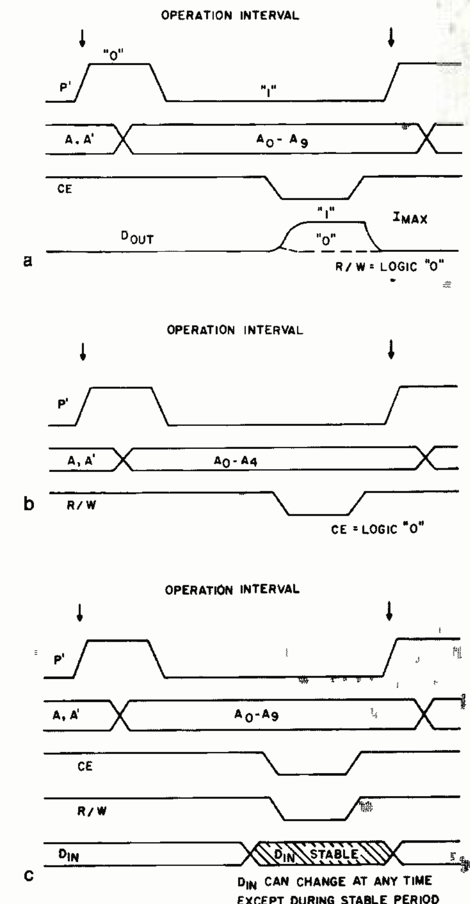


Fig. 9—(right) Function-cycles: a) read, b) refresh, c) write.

cell in the selected column is not refreshed; the other 31 cells in a particular selected row are refreshed.

Write cycle

The WRITE cycle is basically the same as the REFRESH cycle for non-addressed columns. Chip enable is performed during the write operation. Timing for the WRITE cycle is established by the PRECHARGE, CHIP ENABLE and READ/WRITE signals. The WRITE cycle timing diagram is shown in Fig. 9c. The input bit flows to the selected cell (Fig. 8) as follows:

1) The PRECHARGE signal turns on Q_4 and Q_5. Parasitic capacitances on the read- and write-data lines charge.
2) PRECHARGE turns off Q_4 and Q_5 and then activates the row-select line, turning on Q_2. Conditional discharge of the read-data line occurs, depending on the state of C.
3) The READ/WRITE pulse turns on Q_7, Q_8, and Q_3.
4) The chip-enable and column-select lines are activated and turn on transistors Q_9, Q_{11}, Q_{12}, Q_{13}, and Q_{14}. Thus, the read-data line is discharged through Q_8 and Q_9, keeping Q_6 and Q_{10} off during the write cycle.
5) The input bit overpowers the logical state of capacitor C in the selected cell.
6) The READ/WRITE pulse is returned to the logical-"0" state, the row or the column address is changed, and the sequence is repeated for the new address.

System organization

A basic decision in the use of P-MOS memory devices in a memory system is the number of chips that should be mounted on a printed-circuit storage card. The list of factors influencing this decision must include:

—The drive capability of the interface circuit which will convert the signal levels of the memory logic circuits to the levels required for operation of the chip.
—The input capacitance of the memory device and the distributed inductance and capacitance of the lines on the storage card.
—The allowable storage card dissipation.
—Efficient subdivision of the main memory.
—Cost-factor trade-offs associated with use of standard or custom hardware.
—Compatibility of circuits interfacing with the storage-card organization. (The aim is to maximize the number of memory devices relative to the number of interface devices.)

These factors are not independent. Characteristics of the interface level shifter/driver determine the maximum number of devices it can drive. The total load is also a function of the line capacitance on the plug-in card. If the interface circuit is to be designed to drive several memory devices its power dissipation may limit the number that can be driven. The problem of heat dissipation becomes serious as the number of on-card memory devices increases.

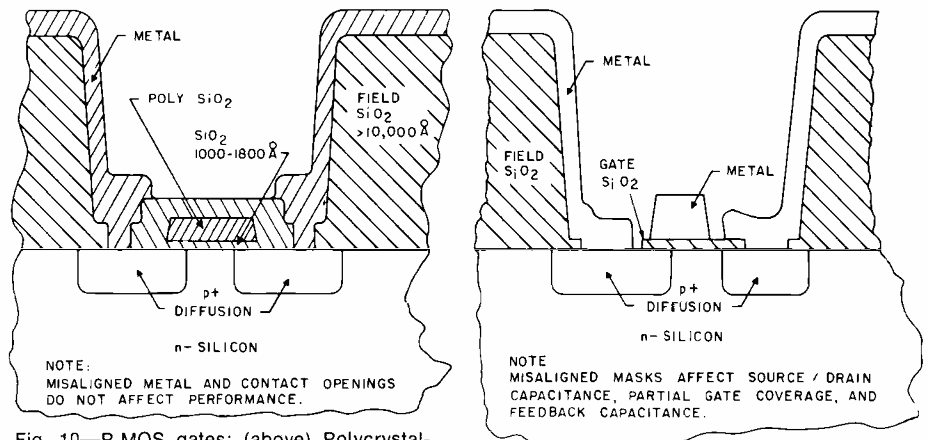


Fig. 10—P-MOS gates: (above) Polycrystalline silicon; (right) Metal.

Two major contributors to the power figure, other than the storage device itself, are the peripheral-circuit steady-state power and the capacitance-charging power CV^2f. Power can be reduced significantly by minimizing the number of transitions per cycle and the length of the period during which the interfacing level shifters are in the high-dissipation logic state. A card-select signal prevents the switching-on of unselected cards and thereby eliminates unnecessary switching transients, and the DC power may be significantly reduced by locking the interface level-shifters in the low-power logic state.

A large memory in which many boards are accessed at the same time would have undesirable local-temperature rises if the boards were too close to one another. Thus, careful attention should be given to the placement of the array cards.

Storage-card dissipation during refresh is approximately the same as during write. The extremely short duty cycle, however (one refresh every 60 μs), reduces the effective average dissipation to a negligible figure.

The need to refresh the memory information every 60 μs while providing maximum service to a processor requires careful planning of the refresh control. The simplest approach calls for (1) a counter of 5-bit length to accommodate all addresses to be refreshed, (2) logic to multiplex the address lines from the normal address register with lines to the refresh register, and (3) interlocking logic to prevent computer access during refresh. This refresh system requires commands between memory and processor to signal the availability of the memory, but the memory availability will be high because the refresh duty cycle is short. Other refresh systems can be designed which, although more complicated, can make the refresh partially or completely transparent to the processor.

The remainder of the control logic is similar to that for other memories and consists of a command register, an address register, a data register, and timing logic. But study of the P-MOS memory chip has shown that failures which lose data can occur. Logic failures of the clock, control, or I/O lines while the memory is cycling will result in writing and reading wrong information and inability to refresh. Therefore logic control or error correction should be included, even though it may not completely eliminate the possibility of loss.

System design utilizing the P-MOS refresh-type memory chip requires little more effort than any other semiconductor memory. Care and thought in system packaging and signal distribution should yield an acceptable, fast, cost-effective memory.

Device technology considerations

P-MOS circuits have been commercially

available for some time. They exhibit the excellent threshold stability and threshold values consistent with good noise-immunity. Because of their lower majority-carrier mobilities, P-MOS circuits are slower than N-MOS circuits. P-MOS speed can be improved, however, by lowering the threshold voltages and increasing the supply voltages.

Recently, the well-established technology of depositing thin silicon layers has been used to apply polycrystalline layers on top of thin silicon dioxide layers. These layers can be made conductive enough by incorporating impurities that have sheet resistances on the order of 10 Ω to 60 Ω per square. Therefore, the polysilicon layers can be used as the gate material for MOS transistors and still have a sufficiently small RC time constant to charge the gate capacitance. Fig. 10 shows the differences between the two basic configurations. The self-aligning feature of the silicon gate structures results in lower Miller feedback capacitance and permits smaller source-to-drain spacings because these spacings do not require tight successive photoresist alignment steps. Because of this polysilicon gate, P-MOS circuits have reached or exceeded the speed of conventional N-MOS circuits.

Refresh-type memories, with their inherently small cell and storage capacitances, put an additional burden on the capabilities of the MOS devices used. These memories require extremely low leakage currents (less than 10^{-13}A at room temperature) to permit long intervals between refresh cycles. At room temperature information will remain stored for tens of seconds; at a 125°C junction temperature, the leakages are increased and retention time decreased by a factor of 10^4.

The attainment of both threshold stability and low leakage requires extremely clean processing conditions. In addition, large-scale integration offers an economic challenge: to make a large number of chips per wafer without defects. Because the chip size is large and the wafer-connection pattern complex, additional requirements are placed on the metalization technology. The metal has to run over fairly high steps of silicon dioxide and polysilicon, steps that are substantially higher than in other integrated circuits.

The basic process selected should be as simple as possible. Economic considerations are important in the selection of the process.

Basic process

In Fig. 11 a chart of the processing of polycrystalline silicon-gate P-MOS circuits is given. n-type silicon wafers are used as starting material. In the first steps, a heavy layer of silicon dioxide (thicker than 10,000Å) is grown, and windows for active devices are defined and cut by photoresist techniques. A thin layer of silicon dioxide (1000Å to 1800Å) is grown in these areas. Then a layer of polycrystalline silicon is deposited over the whole wafer by a chemical reaction employing the pyrolytic decomposition of silane (SiH_4) at temperatures from 600°C to 800°C. The temperature determines the grain size and deposition rate.

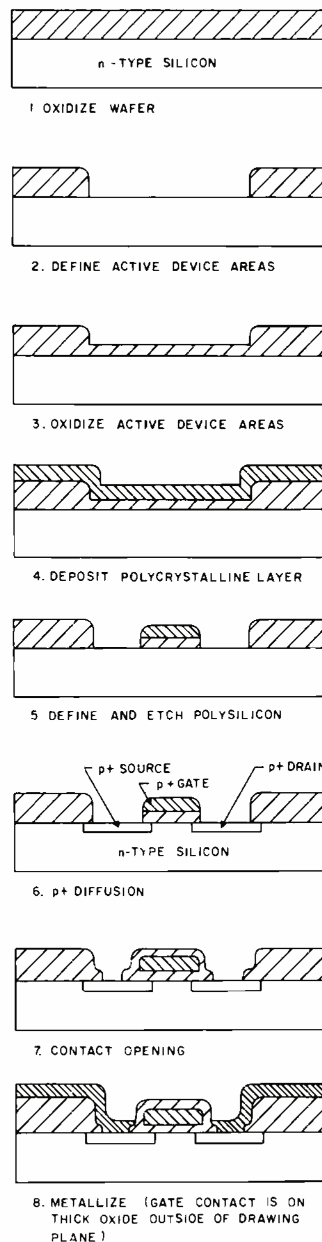


Fig. 11—Processing of polycrystalline-silicon-gate PMOS circuit.

Afterwards, the polycrystalline silicon layer is defined and etched by photolithographic techniques with an intermediate etch-resistant mask of SiO_2 on top of the polysilicon. Line widths of five μm are practical when using polysilicon.

A boron diffusion creates the p-n junctions for the source-drain regions. Lateral diffusion narrows the source-drain spacing. Simultaneously, the polycrystalline layer is made more conductive, and therefore useful for wafer interconnections and crossovers. For the latter, another layer of silicon dioxide is necessary. Then, contact holes are defined and cut.

For individual 1024-bit arrays, aluminum is used as the metal; the large step heights require a heavy layer. The interconnection patterns are again defined by photoresist, and a protective layer of silicon dioxide is then applied. Finally, the circuits are mounted into packages and ultrasonically bonded to the leads.

Summary

The application of the P-MOS silicon-gate technology has made possible the design of a solid-state memory system utilizing a 1024-bit RAM chip as its basic building block. As advances in processing technology and design techniques make more complex chips economically feasible, solid state memories will provide a formidable economic and performance challenge to present memories.

Acknowledgement

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COS/MOS memory array design

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Random-access memory devices fabricated with complementary-symmetry MOS (COS/MOS) provide the system designer with capabilities not achievable with other circuit forms. The unique properties of COS/MOS make possible the design and development of extremely low power, non-destructive readout random-access memory systems capable of high-speed operation. This paper reviews the basic design consideration involved in the development of these memories.

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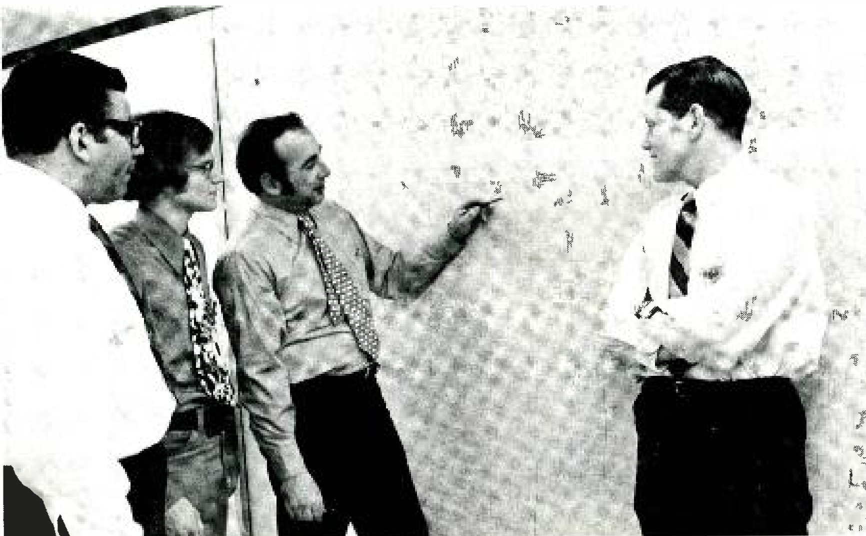

Authors (left to right) Waas, Jorgensen, Oberman, and Dingwall.

Among the advantages of COS/MOS memories is the ability to perform over wide extremes of temperature and power supply variations with high noise immunity. Thus, COS/MOS memories can operate in environments where single-channel MOS or bipolar devices cannot.

Economies in system design are obtained by the requirements for a single non-critical power supply voltage. Furthermore, the memories are static and do not require high-power clock pulses or preconditioning pulses for proper operation. Therefore, system power and complexity are substantially reduced, when compared with other technologies. Also, system noise problems are eased, because large transient currents are not developed.

Typically, memory systems utilizing COS/MOS circuitry can achieve access times faster than 500 ns with a quiescent power dissipation of 1 μW per bit and a dynamic power drain of less than 25 μW per bit.

The flexibility of COS/MOS is such that, in applications where minimum power dissipation is not a pre-requisite, the same arrays can be operated in the 100 to 150-ns range by increasing the power supply voltage and using bipolar interface circuits.

RCA has developed and is currently expanding a family of COS/MOS memory devices. Table I indicates the characteristics and status of these devices.

COS/MOS memory storage cell

The characteristics of the memory device size, power, speed, and stability are all dependent upon the design choice of the storage cell. The general requirements for a storage cell are small area, low power, and insensitivity to slight variations in processing or fabrication.

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The memory storage cell common to all RCA COS/MOS memories consists of two COS/MOS inverters cross-coupled to form a flip-flop. This circuit configuration is extremely stable and dissipates negligible power. Power dissipation is due primarily to the leakage currents of the p- and n-channel transistors in the off state on opposite sides of the flip-flop. The circuit exhibits excellent noise immunity and a sharp transition region, as a result of the threshold voltages of the COS/MOS transistors and the push-pull operation of the back-to-back inverters.

Single transistor transmission gates are employed as a simple and efficient means of performing the logic functions associated with storage cell selection, combining it with the sensing and storing operations (Fig. 1).

Addressing is accomplished by energizing X and Y word lines that turn on the transmission gates on both sides of the selected flip-flop. (In this case, because p-channel transmission gates are shown, a ground level is required for selection). A current path is then provided from the most positive DC supply voltage, V_{DD}, through the p-channel transistor which is on in the flip-flop and the transmission gates to the sense digit lines, D_o, and D_1. There will be current flow in only one of the digit lines, depending upon the state of the flip-flop.

The write operation is performed by addressing a cell, then changing the state of the D_o or D_1 line, from ground to V_{DD}. As one side of the flip-flop is charged to V_{DD}, the opposite side is held to ground potential, i.e., the voltage at A is forced to that of D_1; correspondingly, the voltage of B is forced to that of D_o. This push-pull drive scheme results in a high-speed and reliable write operation and low power dissipation.

Table I—COS/MOS Memory Characteristics

Designation	Type	Capacity (bits)	Stand-by (nW/bit)	Selection (mW) P_{pk}	Selection (mW) P_s	Access time (ns)	Sense current*** (μA)	Status
CD4005	Non-decoded (4x4x1)	16	6.2	—	10	15**	1000	In production
TA5577*	Non-decoded (8x8x1)	64	450	20	24	50**	800	Limited production
TA5870*	Non-decoded (16x16x1)	256	1200****	32	33	80**	300	Available for experimental use only
TA6042*	Full decode 256x1	256	1200****	—	33	200**	300	Limited sample quantities available
TA5974*	Full decode 256x1	256	1200****	—	33 —	450	Voltage output	Limited sample quantities available 4th quarter

*RCA Dev. Nos.
**Current sensing
***$V_{DD}-V_{SS}$=10 Volts
****Premium devices can be obtained with 10-nW power dissipations.

The geometry of the transistors in the storage cell is chosen to insure that under worst-case conditions, the state of the cell remains stable, the read operation is nondestructive, and the write operation is reliable and does not disturb unselected cells. Constraints are placed on the ratios of transistor geometries to insure reliable operation; the absolute size of transistors is a design trade-off primarily involving sense current magnitude and chip area.

An example of the transistor cell operation is shown by the circuit in Fig. 1. In this circuit, the transistor geometries of the transmission gates Q2, Q7, Q1, and Q8 must be such that during a read operation with Q3 and Q6 on, the voltage at point B is maintained greater than the threshold of the Q5, Q6 inverter. The amount that point B is positive compared to the Q5, Q6 junction determines the stability. Transistors Q7 and Q8 will have no influence upon the potential at Point A, because they are both on and returned to the same ground potential as point A. Similar stability considerations are required if transistors Q4 and Q5 are in the conducting state.

During the write operation, the state of the flip-flop is changed by raising the potential in one of the D lines to V_{DD}. If D_1 were raised to V_{DD} and D_o remained at ground, the transistor geometries must insure that the potential at point A exceeds the threshold at the junction of Q3 and Q4, turning Q3 off and Q4 on. Turning Q3 off will move point B towards ground. This effect will initiate a feedback action between the cross-coupled inverters, insuring a rapid and reliable write operation.

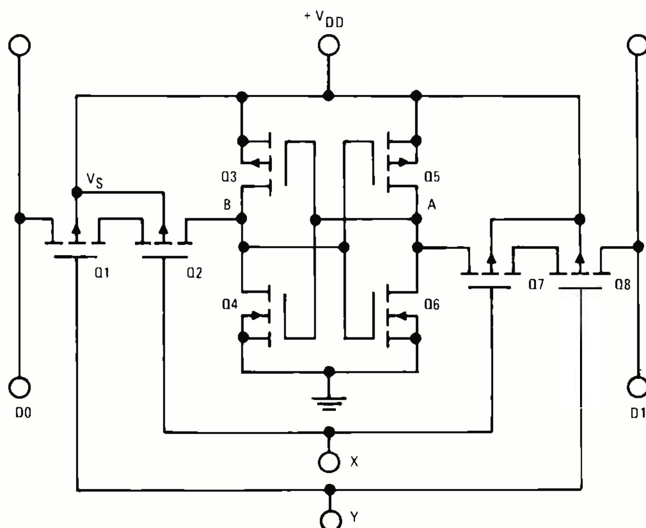

Fig. 1—Bit-organized memory cell.

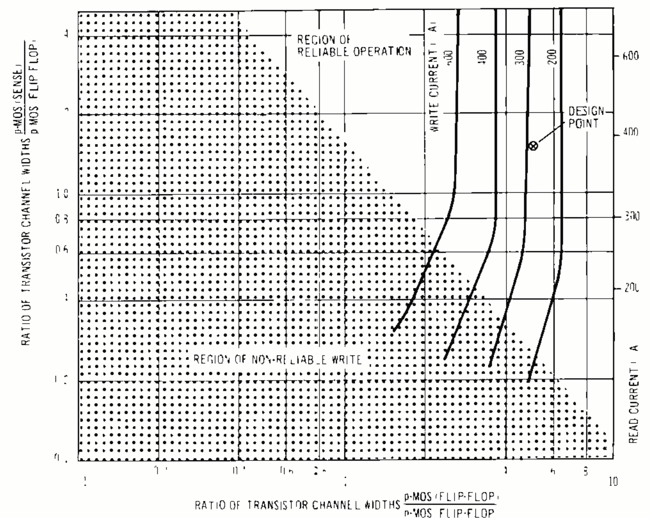

Fig. 2—Computer-calculated regions of reliable memory cell operation showing proper centering of cell design point (T=25°C).

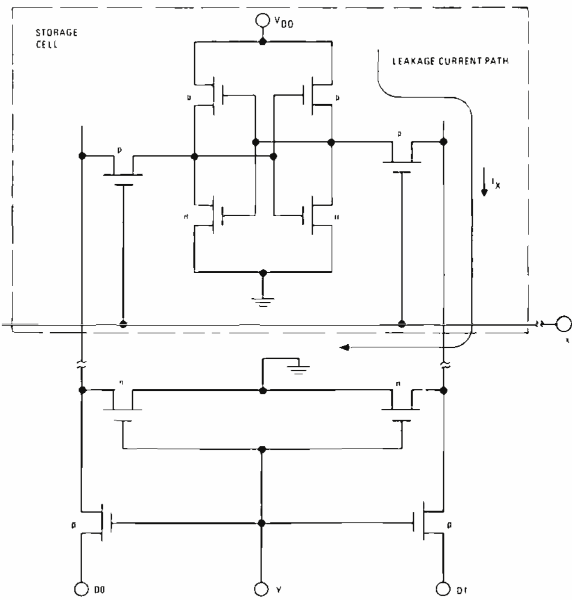

Fig. 3—Typical memory cell with D-line decoding.

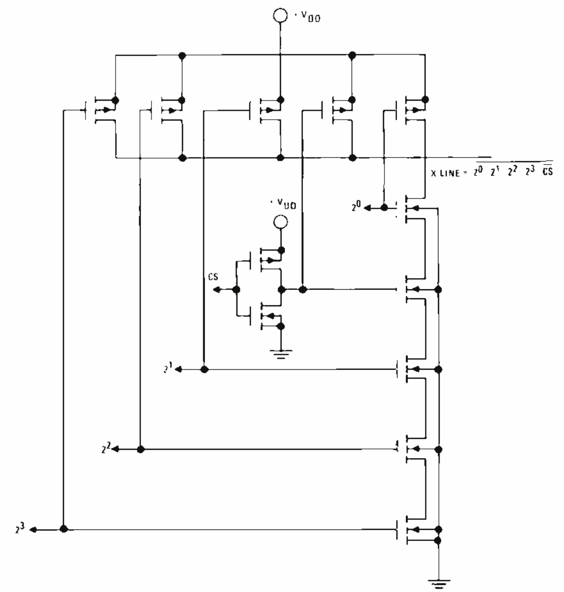

Fig. 4—Address decode.

As is the case with flip-flop circuitry, the design considerations for set and reset tend to be mutually exclusive, and it is important that the transistor conductance ratios be suitably centered in a region of reliable read and write operations.

Fig. 2 summarizes the results of a typical analysis at 25°C, showing how the design point is suitably centered in a region of stable operation. The X coordinate is the ratio of widths of the p-channel to the n-channel transistors in the flip-flop. The Y coordinate represents the ratio of the width of the smaller p-channel MOS transistor in the flip-flop. For analysis, a grid of points is measured on the breadboard and simulated on the computer. Contours are then plotted for read and write currents, and failure boundaries are located. A design point is chosen and variations in current and voltages around this point are then plotted for changes in various parameters such as mobility, doping, etc. In general, the basic design considered has a safety factor in excess of 5, in that the conductance of any transistor can be off by a factor of 5 and still permit reliable operation. The centered design permits a wide margin of safety even over the combination of all worst-case conditions studied.

The RCA CD4005 uses an eight-transistor bit-organized cell such as the one shown in Fig. 1. A reduction in transistor count can be made by a slight modification in decoding technique. This method is used in the design of the 256-bit memory and is illustrated in Fig. 3. In this design, the Y-select transistors are common for each column of storage elements instead of appearing in each cell as previously illustrated. This configuration reduces the transistor count to slightly over six per memory cell. This technique, called D-line decoding, is used in the more recently designed COS/MOS memories, i.e., RCA Dev. Nos. TA5577, TA5870, TA6042, and TA5974.

D-line decoding requires one additional transistor for each column bus to insure that unselected column buses are clamped to a known potential and are not free to assume a random voltage. An unclamped bus will assume a potential determined by leakage currents, stored data, and previous operations. This situation can result in sufficient energy being stored in column bus capacitance to switch the state of a storage cell when only an X address is selected. This half-select problem is solved in the circuit of Fig. 3 by the n-channel transistors being placed in parallel with the column section (Y-address) transistors. By connecting the gate of the n-channel transistor to the Y-address line, a clamp is lifted whenever its column is selected; therefore there is no interference with full-selection operation.

The use of the clamp does increase the power dissipated in the array during selection. When an X-address line is

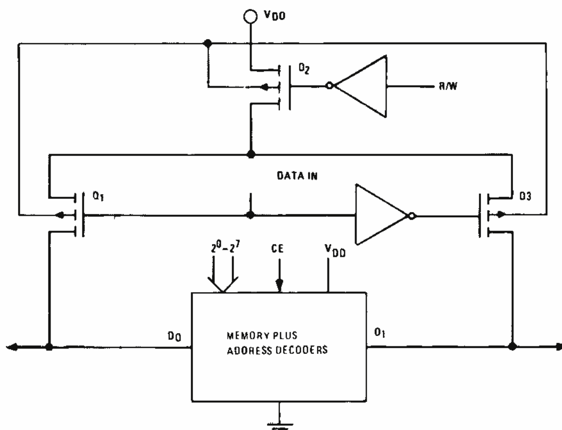

Fig. 5—Write circuitry.

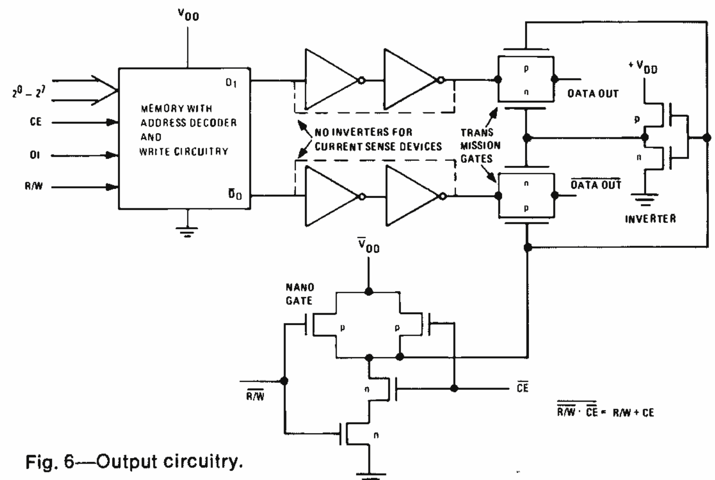

Fig. 6—Output circuitry.

selected, a current (I_x) can flow from V_{DD} through the flip-flop p-transistor to ground by way of the unselected column n-channel clamp transistors. This current adds to the overall power dissipation but has no effect on the sensing operation. The array dissipations can be represented as:

$$P_{Partial\ Select} = \sqrt{n} \times V_{DD} \times I_X$$

(X address selection only) and

$$P_{Selected} = \sqrt{n-1} \times V_{DD} \times I_X + V_{DD} \times I_{Sense\ (One)}$$

(For both X and Y selection), where n is the number of storage bits.

Address decoding

Some of the available COS/MOS arrays are non-decoded, giving the system designer direct access to the address and sense-digit lines of the array. This design permits speed and power tradeoffs, as the system application requires.

The decoded arrays have incorporated binary decoders which are connected to the address lines, thereby reducing the number of external chip connections. The 32 address lines of a 256-bit memory are reduced to 8 binary address lines. The array is arranged in a 16 by 16 matrix requiring 4 X- and 4 Y-address bits. The Y decoder is composed of 16 four-input NAND gates. The X decoder has 16 five-input gates. The fifth input on the X decoder is for the chip select signal. If the chip is not selected the X address decoders are inhibited setting the 16-X address lines to V_{DD}. Therefore, the row transmission gates are not selected, and partial select current cannot flow.

A typical X decoder is shown in Fig. 4. When the decoder output is at ground potential, the addressing transistors turn on because they are p-channel devices. The Y decoder is similar in design with the exception of the chip enable input.

Read/write operation

The memory cell on-chip has common shared lines for sense and digit write

Table II—Operational modes.

Operation	Signal lines Read/ write	Chip enable	D_I	Sense lines D_O	D_O
Chip inhibited	X	H	X	F	F
Read	L	L	X	Q	Q
Write "1"	H	L	H	F	F
Write "0"	H	L	L	F	F

Legend:
E: floating (data output disconnected from output terminal)
X: don't care
L: low level—logic "0"
H: high level—logic "1"
Q, Q: data output

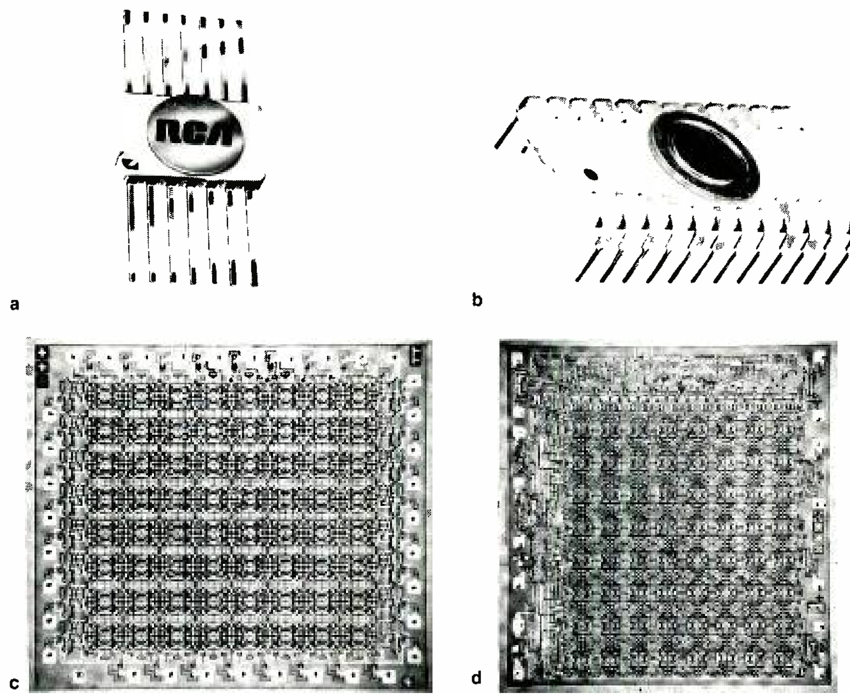

Fig 7—Evolution of COS/MOS memory arrays: (a) CD4005 16-bit non-decoded—70x70 mils, (b) TA5577 64-bit non-decoded; (c) TA5870 256-bit non-decoded—110x128 mils; and (d) TA6042 256-bit full decoded—121x124 mils.

(D_o and D_I in Fig. 3). To simplify chip interfacing, these functions are separated on the chip and brought out to different terminals. A read/write command input is required to control the functional operation of the chip.

When the read/write input is low or at the most negative *DC* supply voltage, V_{SS}, the memory will read out the information of an addressed cell. When the read/write input is high or at V_{DD}, the information, as determined by data-in logic level, is written into the addressed cell. The writing circuitry is shown in Fig. 5. When the read/write input is at V_{DD}, transistor Q2 turns on providing a voltage (V_{DD}) that can be applied to either D_o or D_I as determined by the state of data-in. If data-in is at V_{DD}, Q3 turns on applying V_{DD} to D_I. If data-in is at V_{SS}, Q1 turns on applying V_{DD} to D_o. The actual voltage applied to the memory cell is somewhat less than V_{DD} due to a voltage divider effect of the addressing transistors.

To prevent spurious output signals, it is necessary to have an output control pulse that inhibits an output from appearing on the data lines while writing or while the chip is unselected. This condition is accomplished by a transmission gate at the output that turns off, blocking the data lines, when the chip enable or read/write control lines are at V_{DD}. This circuit is illustrated in Fig. 6 and uses a 2-input NAND gate and an inverter with two transmission gates. The two inverters in each of the data lines are used as sense amplifiers to obtain a voltage output. When these inverters are missing the memory is a current output device. A truth table of the TA5974 is shown in Table II.

Conclusion

COS/MOS memory devices have evolved over a three-year period from a non-decoded 16-bit array to a fully decoded 256-bit device. This evolution is illustrated in a series of photographs in Figs. 7(a), (b), (c), and (d) which indicate the relative complexity and size of the different memory chips. The current 256-bit memory devices have a chip area of approximately 15,000 mil^2. This area corresponds to a transistor density of over 150,000/in^2.

As new techniques and technologies are developed, these COS/MOS devices will be employed to further increase chip storage capacity and decrease power dissipation. A 1024-bit COS/MOS memory chip is certainly realizable in the near future.

Current programs in COS/MOS memory include the development of sealed-junction beam-lead COS/MOS memory arrays. Hybrid packaging techniques will enable the fabrication of high density, reliable, and exceptionally economical memory systems. The key word for COS/MOS memory is high reliability and therefore the future holds a great promise.

Bipolar/MOS interface circuit design and technology

H. Beelitz | N. Ditrick

Semiconductor memory systems promise improved performance and reliability at costs equal to or lower than core memory systems. To meet the challenge of this promise, a marriage of MOS memory technology and bipolar interface logic technology has proven effective, but there are areas of incompatibility. This paper discusses the bipolar/MOS interface problem as seen from the viewpoint of the bipolar interface circuit technologist, and details possible circuit technology solutions.

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received his BS and MS degrees in Physics from the Ohio State University in 1952. He joined RCA as a specialized trainee in June of 1952 and was later assigned to the Receiving-Tube Advanced Development Activity of the Electron Tube Division. He was transferred to the Semiconductor Advanced Devices Development Activity in April of 1953. He has made major contributions in the development of a number of devices including point contact transistors for switching and high frequency oscillation, intermediate and radio frequency transistors for portable radios, drift transistors, thyristors, germanium mesa transistors, germanium and gallium arsenide tunnel diode, gallium arsenide switching and power transistors, MOS triodes, tetrodes and integrated arrays and high speed ECL bipolar integrated circuits. Mr. Ditrick is now an Engineering Leader in the Solid State Technology Center and is working primarily on high speed integrated digital circuit fabrication and process development. Mr. Ditrick is a member of Sigma Pi Sigma, Tau Beta Pi, and the Institute of Electrical and Electronic Engineers.

"WHY INTERFACE CIRCUITS?" is a most appropriate question since one of the early claims made by semiconductor memory advocates was that semiconductor memories, being made of the same "stuff" (silicon) as logic circuits, could interface directly with logic. In general, this claim has proven to be true for those memories fabricated with the same technology as the logic.

As an illustration, RCA's bipolar ECCSL RAM (CD2155D) readily interfaces with standard emitter-coupled bipolar logic. In a similar way, RCA's developmental COS/MOS RAM (TA-5974) directly interfaces with standard COS/MOS logic without intermediate buffers.

Buffer circuits are needed in many cases, however, when we try to intermix fabrication technologies for memory and logic. Such intermixing is often desirable to more fully exploit

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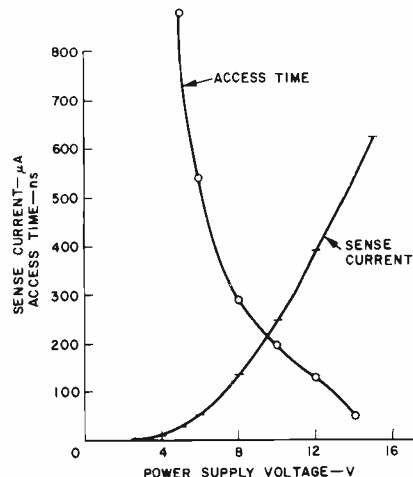


Fig. 1—MOS memory array performance as a function of supply voltage.

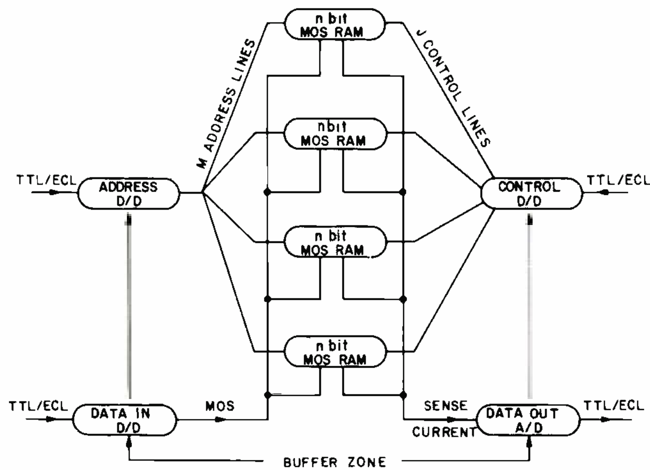
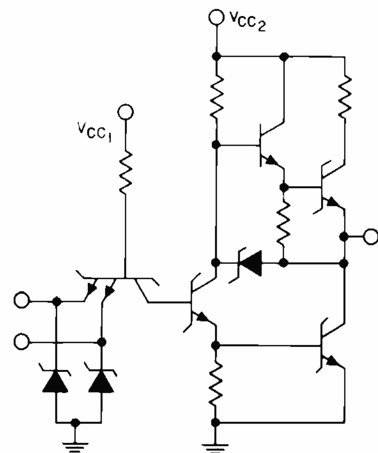
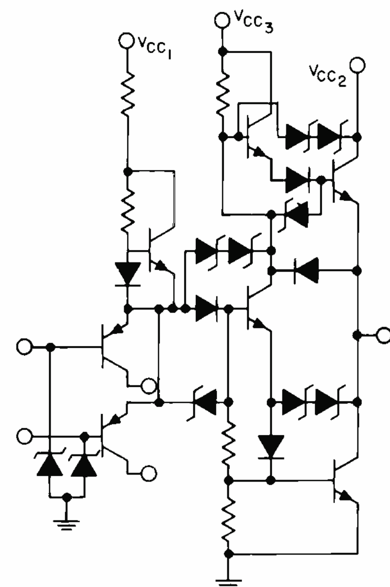


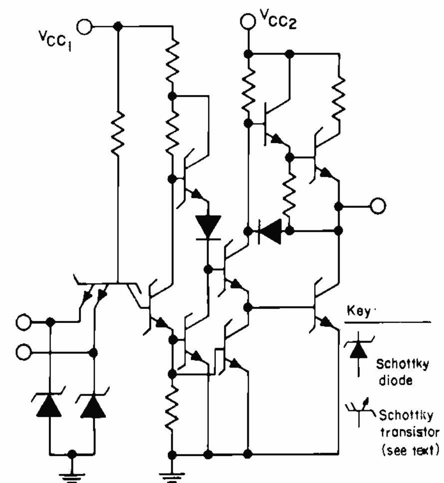
Fig. 2—Memory-logic interface.



a) High voltage processing, integral Schottky transistor; T²L input, MOS output.



b) High-voltage processing, non-integral Schottky transistors; T²L input, MOS output.



c) Low voltage processing, integral Schottky transistors; T²L input, MOS output.

Fig. 3—TTL (T²L)/MOS level shift circuits.

the particular attributes of each technology: the MOS technology for high density, low power memories and the bipolar technology for high speed, high load-drive logic. It is an efficient and effective marriage.

Fig. 1 illustrates the advantages of operating a typical MOS memory array at, increased power-supply voltages. The array is an RCA developmental 256-bit fully decoded COS/MOS RAM (RCA Dev. No. TA6042) with output current sensing. Note that very substantial improvements in both access time and sense current occur with higher supply voltages. This radical improvement in performance provides the major justification for introducing expensive custom interface circuits to buffer between logic and memory.

One possible arrangement of memory arrays with supporting interface buffers is illustrated in Fig. 2. In this scheme utilizing current-sense MOS RAMS such as TA6042, essentially two types of buffers are required. One type provides a digital-to-digital (D/D) transformation (TTL/ECL to MOS) whereas the other type performs an analog-to-digital (A/D) transformation (sense current to TTL/ECL).

The level shift problem

Level-shift interface circuits perform the necessary function of boosting the voltage levels and swings of standard ECL or TTL logic circuits to the much higher (2 to 20 times) values at which typical MOS memory arrays perform most efficiently.

Frequently, these custom circuits also must provide sufficient power gain to drive the high capacitance loads (100 to 300 pf) usually associated with paralleled memory arrays. Because of this high load-drive requirement, the level shifter output circuit must necessarily take on some form of the "totem-pole" active pull-up and pull-down usually associated with standard TTL circuits.

The high-voltage breakdown requirements (15-25 V) on the interface circuits used with p-channel MOS RAM's dictate either more sophisticated circuit techniques or processing modified from that of the standard TTL or ECL.

Design approaches: TTL/MOS level shifters

There are three separate approaches to the design of TTL/MOS level-shift interface circuits. These circuit technology approaches are described below with the aid of sample circuits shown in Fig. 3 which are used for illustrative purposes. The actual circuit designs differ from the illustrated circuits according to the particular optimization required.

The most obvious and straightforward approach for the circuit designer is to adopt a process capable of accommodating both the switching speed of the TTL logic circuit and the voltage swing of the MOS memory. A standard factory process should be specified if a suitable one is available. This permits the fabrication of the circuits with a minimum development cycle time at a minimum cost.

Fig. 3a shows a typical circuit that might be used as an interface between

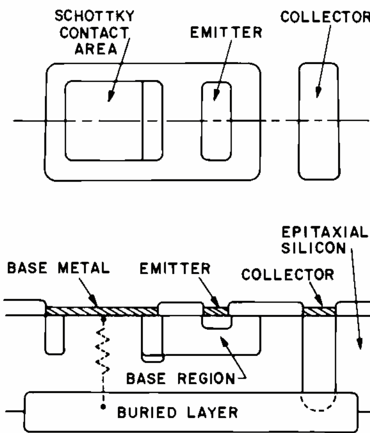


Fig. 4—Schottky clamped transistor structure.

TTL logic and MOS memory. This circuit uses Schottky diodes built across each saturating transistor collector-base junction as an integral part of the transistor structure. Each diode clamps the collector-base junction so that the collector cannot become forward-biased enough to inject current into the base. This Schottky diode clamp can be built with only minor changes in processing and eliminates the need for gold doping to reduce storage time.

The breakdown voltage requirement V_{CEO} (collector-emitter voltage, base open) for the circuit in Fig. 3a might be as high as 25 V. This breakdown voltage is easily achieved with standard processes involving the use of a 10-μm epitaxial layer of about 1 ohm-cm resistivity. There is a problem, however, in making a suitable Shottky diode on such an epi layer. The combination of relatively high resistivity and thick epitaxial layer results in a Schottky diode with a high forward resistance, as shown in Fig. 4.

The Schottky diode is the contact between the base metallization and the epitaxial silicon. The figure shows that the collector-base resistance in a Schottky transistor is primarily due to the region between the buried layer and the silicon just under the base metallization.

This resistance, shown by the dotted line, can be more than 100 ohms in a typical Schottky transistor. Such a large resistance in series with the Schottky diode severely reduces its ability to prevent current injection from the collector into the base of the transistor. Fig. 5 shows the forward characteristic of a normal p-n (base-collector) junction, an ideal Schottky diode, and real Schottky diode. The actual forward characteristic observed is the composite shown. The Schottky diode is completely ineffective as a clamp for preventing saturation at any current level above the intersection of the curves representing the base-collector junction and the real Schottky diode.

There are a number of possible solutions to this problem of diode series resistance. One possible solution is a reduction of both the thickness and the resistivity of the epitaxial layer, an increase in the size of the Schottky diode, and a careful optimization of the fabrication process in an attempt to maintain an acceptable breakdown voltage. Possibly a better solution is to use a circuit "trick" such as that shown in Fig. 3b. With this circuit, the Schottky diode, rather than being connected directly between collector and base of the transistor, is connected from the collector of the transistor back to its base (or other control point) through an appropriate offsetting element. Such an element might be a suitably connected resistor, diode, or transistor. This technique is analogous to that of the familiar "Baker clamp" which had proven successful in discrete circuits prior to the introduction of gold doping for storage time control. There are, however, several shortcomings to this approach:

—It is somewhat more difficult to set the circuit output to low voltage than in standard saturating TTL. This difficulty exists because of the more complex interaction between devices in the feed-back loop of the pull-down device.
—There are possible stability problems associated with a feed-back loop around two active devices. Care should be taken when transistors are employed as offsetting means.
—The circuit is somewhat more complex than that in Fig. 3a.

Another circuit solution is illustrated in Fig. 3c. This circuit is configured such that the high-voltage devices always see, both in on and off states, a sufficiently low return impedance such that V_{CER} operation (where the base is connected to the emitter through a fixed resistance) is encountered rather than V_{CEO}. This circuit requires about half the breakdown voltage of the other two. Because of the reduced breakdown voltage requirements, trade-offs can be made in processing to achieve a much lower series resistance for the Schottky diode. Al-

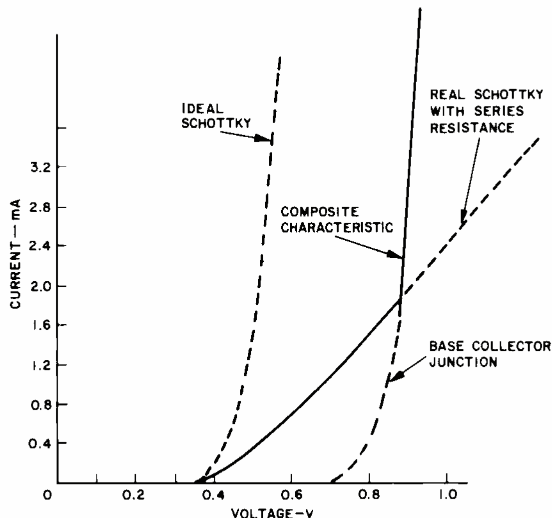


Fig. 5—Composite forward current-voltage characteristics of base-collector junction.

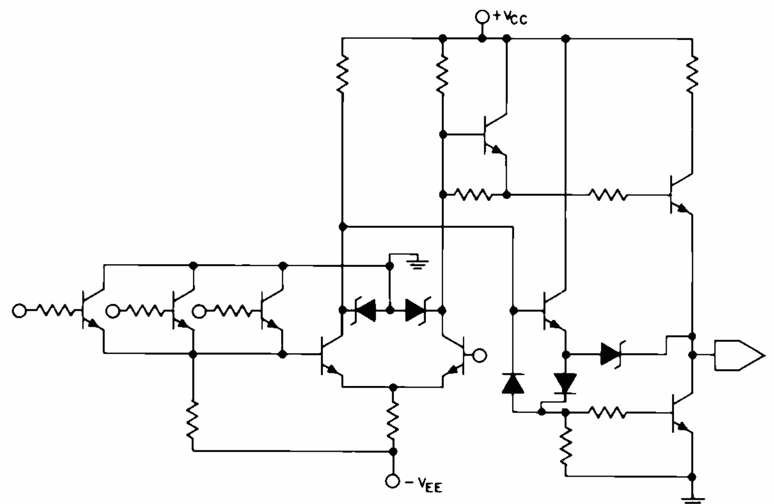


Fig. 6—ECL/MOS level shifter.

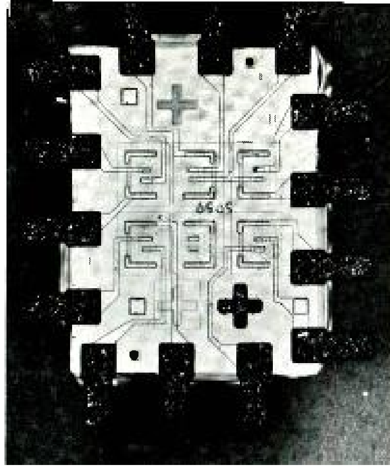


Fig. 7—Photomicrograph of a developmental quad ECL/MOS level shifter.

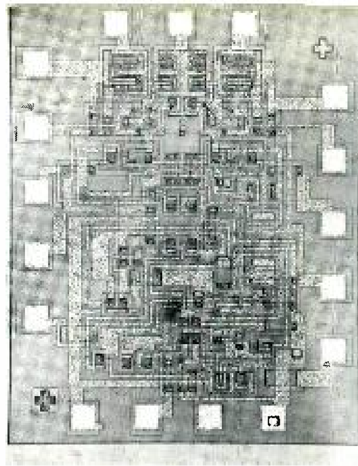


Fig. 8—Combined dual digit driver and current sense amplifier.

though this circuit requires more components, the transistors in particular are generally smaller, and the overall physical size of the circuit may not be much larger than the others. The circuit in Fig. 3c is particularly promising because of the lower breakdown voltage requirements.

ECL/MOS level shifters

A relatively straightforward approach employing conventional processing technology is possible for the design of ECL/MOS buffers. Because the phase splitter is essentially a non-saturating current mode logic (CML) switch, preventing saturation of the active pull-down transistor of the output totem-pole is the only problem. Such saturation can be prevented by using either Schottky diodes or collector-base junction diodes as in the TTL/MOS level shifter. The Schottky diodes are preferred, of course, because they are predominantly majority carrier devices and their storage time is essentially zero, while base-collector diodes have relatively long storage time. Base-emitter diodes cannot be used because of their low breakdown voltages.

Fig. 6 illustrates a simple circuit for implementing the ECL/MOS level shifter. It can drive a load capacitance of several hundred picofarads at moderate standby power dissipation.

A photomicrograph of a developmental quad ECL/MOS level shifter, RCA Dev. No. TA5995, based upon the described circuit techniques, is shown in Fig. 7. The device dissipates nominally 450 mW and will drive 10 V COS/MOS arrays. Rise and delay times are typically 15 ns with 100 pF load capacitance.

The sense amplifier problem

The sense amplifier transforms a small sense current developed by the MOS memory device into a (TTL/ECL) logic-level voltage suitable for driving standard logic IC's.

The primary circuit design problem revolves about the particular input-output (I/O) circuit chosen for the MOS memory array Specifically, if a common data-in, data-out channel is decided upon, the sense amplifier must be capable of sustaining and recovering from the digit drive signals. These signals are typical of the same high level as the memory array power supply and are developed by level shift interface circuits.

If, however, separate channels are employed for data-in, data-out, then the sense amplifier need merely boost the small sense signal current (typically 0.1-1.5 mA) and develop the appropriate signal (TTL/ECL) and drive capability (fan-out). This requirement is relatively straightforward.

From this discussion it is readily appreciated that separate I/O channels are preferred on the MOS memory device, as long as the additional MOS circuitry and the requirement of one more pin are not too burdensome.

ECL/MOS sense amplifier

A photomicrograph of a combined dual digit driver and current sense amplifier integrated circuit is shown in Fig. 8. This developmental device is intended for use with single-channel I/O current sensing p-channel MOS and COS/MOS memory arrays. Both digit level shift and current sense amplifier functions have been combined in a single IC which efficiently accomplishes channel separation.

Technology for interface circuits

Considering the various circuits discussed, a need for two basically different processes becomes evident: one with a relatively high breakdown voltage necessary for circuits in Fig. 3a and 3b, and another with a relatively high speed but lower breakdown voltage suitable for circuits in Fig. 3c and 6. The higher voltage process is basically a standard linear process giving a breakdown voltage of about 25 V for V_{CEO}. The high-speed process is a modification of a high-speed digital ECL process with minor changes to improve the breakdown voltage.

Table I shows the processing sequence for two proposed processes. The major differences are:

Epitaxial layer thickness and resistivity,
Order of base and contact diffusion, and
A non-reoxidized emitter in the high-speed process.

The addition of the Schottky diodes for storage time control requires no additional processing steps but does require care in wafer metallization and also requires tighter tolerances on process parameters. This need arises because of the severe requirements for both breakdown voltage and low series resistance. Present Schottky transistors use aluminum (or silicon-aluminum alloy) contacts. Similar transistors have also been made using beam-lead metallization with platinum silicide or palladium silicide contacts.

Conclusions

The design and fabrication of bipolar interface circuits for MOS semiconductor memory systems is readily accomplished by combining careful circuit design and optimization with the proper choice of processing technology.

Schottky diode technology, superimposed over existing high-voltage high-speed processing technology, provides the key for fabricating high-performance special-purpose bipolar circuits at commercial costs.

Table I—Interface circuit processing sequence.

High-speed process	*High-voltage process*
Epi layer growth 7-10 μm	Epi layer growth 3-5 μm
Pocket diffusion	Pocket diffusion
Isolation diffusion	Isolation diffusion
Deep collector diffusion	Deep collector diffusion
Base contact diffusion	Base diffusion
Base diffusion	Base contact diffusion
Emitter diffusion	Emitter diffusion
Open all contacts	Open base and resistor contacts
Metallization	Open emitter contacts with n- and p-contact mask
	Open Schottky contacts with Schottky and p-contact mask
	Metallization

Materials and Processes Laboratory

Dr. J. A. Amick

Improvements in the materials and processes used in fabricating semiconductor devices generally lead to increased profits. To assist in reaching this goal, the Materials and Processes Laboratory of the Solid State Technology Center provides RCA with a wide variety of materials, processes, and techniques related to the fabrication of solid state devices. This paper describes the organization and programs of the six major research groups within that Laboratory.

In large measure, the yield and the reliability of semiconductor devices are controlled by the processing techniques and the materials used in their preparation. Improvements in processes or materials usually translate directly into increased profits. Accordingly, the primary goals of the Materials and Processes Laboratory are to maintain and control the underlying technology used in the manufacture of solid-state devices and to develop improvements that will advance RCA's competitive edge, especially in the area of silicon technology. This laboratory also serves as an evaluation center for new commercially available apparatus and materials useful for semiconductor device fabrication and offers technical consultation and analytical services to RCA's manufacturing facilities.

Organization and programs

The Laboratory is divided into six major areas of activity, each having approximately four staff members and a similar number of support personnel. These areas are 1) Crystal Growth, headed by U. Roundtree, 2) Diffusion and Passivation, headed by K. Strater, 3) Photoresists and Polymers, headed by R. Epifano, 4) Metalization, headed by R. Soden, 5) Metallurgy and Bonding, headed by C. Horsting, and 6) Analytical Techniques and Device Failure Analysis, headed by A. Stoller. Each of these activities will be described in turn.

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received the AB in Chemistry from Princeton in 1949. He spent a year as a predoctoral fellow at Brookhaven National Laboratory, Upton, Long Island, and returned to Princeton for an MA and Ph.D. in Physical Chemistry in 1951 and 1952, respectively. In 1953 after a postdoctoral year at Princeton, Dr Amick joined RCA Laboratories. In 1956-57 he spent a year at Laboratories RCA, Ltd., in Zurich, Switzerland. On returning to Princeton, he was assigned to the Materials Research Laboratory where he engaged in research on the stabilization of semiconductor surfaces and the epitaxial growth of semiconductor elements and III-V compounds. Late in 1963 he joined the Process Research and Development Laboratory, which subsequently was incorporated into the Process and Applied Materials Research Laboratory. Currently he is Manager of the Materials and Processes Group. Dr Amick is a Fellow of the American Institute of Chemists and a member of the American Chemical Society, the Electrochemical Society, AAAS, and Sigma Xi. He is listed in Leaders in American Science.

Crystal growth

The Crystal Growth group is primarily responsible for the deposition of single-crystal silicon layers on silicon substrates by the chemical vapor deposition process commonly referred to as "epitaxial growth". This process is employed in the fabrication of many types of discrete transistors and of most integrated circuits and has become an important "building block" in the design and manufacture of the new, more sophisticated devices and arrays.

One goal of this group is the evaluation of alternative types of epitaxial growth apparatus. For this purpose, two new, commercial "pancake" style reactors have recently been installed. (Fig. 1). These units are being compared with the RCA designed "vertical epi" units to determine which configuration permits the most uniform and the most economical deposition of silicon, both for silicon growth on silicon substrates and for silicon growth on sapphire substrates.[1] Analysis of the gas flow patterns in the two types of apparatus should lead to an improved understanding of the process and subsequently to new apparatus designs that will give even tighter control over the deposition reaction.

Surface quality

The surface quality of deposited silicon layers is critically dependent on the cleanliness and perfection of the substrate on which growth takes place. A second goal of the Crystal Growth group is therefore to investigate the surface perfection of substrates and to devise improved cleaning and handling techniques that eliminate or minimize defects which would spoil the deposited layers. A new technique for determining surface perfection has resulted from research carried out at RCA.[2,3] This technique employs the thermal oxidation of silicon, followed by removal of the oxide layer and etching in Sirtl etch[4] to reveal imperfections that are difficult to detect by any other method. With the help of this technique and other analytical methods, the quality of substrates for epitaxial growth can be greatly improved, and the quality of epitaxial layers grown on these substrates can be better controlled.

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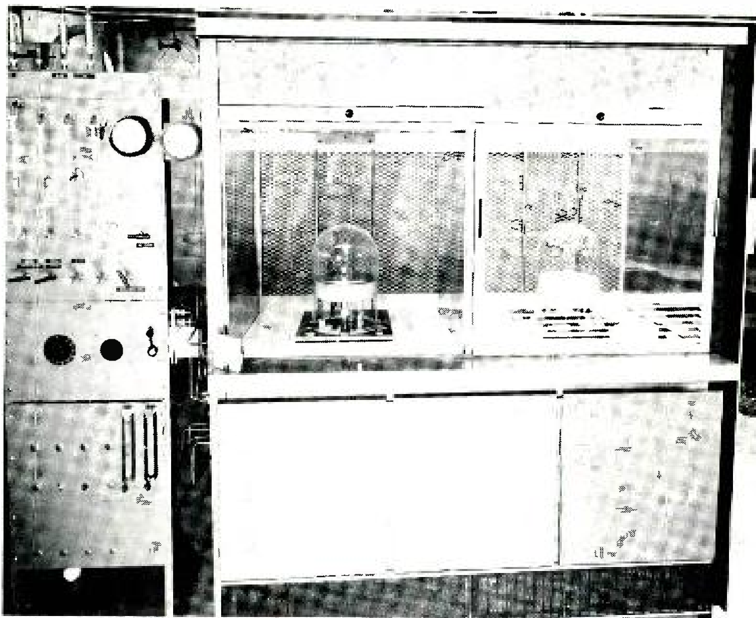

Fig. 1—One of the newly installed "pancake" type epitaxial growth reactors.

Analytical techniques for determining the thickness and resistivity of epitaxial layers, especially when several layers of differing resistivity are grown one on top of another, must be improved so that these multiple layers can be produced controllably. Accordingly, a third goal of this group is the development of improved methods of characterizing epitaxial layers. Methods that are rapid and simple enough to be used readily in a production location are particularly needed.

Because the processes and the apparatus are the same as those employed in epitaxial growth, the deposition of polycrystalline silicon is carried out in the crystal growth group. Polycrystalline silicon layers are finding application in the preparation of "silicon gate" MOS devices and in the fabrication of certain discrete devices such as high-frequency transistors.

Finally, the Crystal Growth group is responsible for improving and controlling the growth of single-crystal gallium arsenide ingots used in the preparation of light-emitting diodes and lasers.

Diffusion and passivation

Diffusion is one of the oldest and passivation one of the newest of the processes used in semiconductor device preparation. Improvements in processing in both of these important areas are now taking place with the advent of improved chemical vapor deposition techniques for forming dielectric layers.[5]

The basic diffusion process remains unchanged. The novelty is in the materials employed as diffusion sources: layers of silicon dioxide containing appropriate dopants are formed directly on a silicon wafer for this purpose. A material relatively new to semiconductor processing, silane (SiH_4), is used as a source of silicon in the preparation of these layers. In special apparatus devised at RCA[6] (Fig. 2), this reagent can be mixed with oxygen to deposit layers of silicon dioxide on almost any desired substrate at modest temperatures (in the 300° to 450°C range). With proper admixture of other hydrides, such as diborane (B_2H_6) or phosphine (PH_3), layers of mixed oxides are formed. Boron and phosphorus are the two most common dopant impurities used in semiconductor device fabrication. The deposition of a mixed oxide thus provides a solid diffusion source for these dopants. The oxide layer (deposited at 400°C) becomes a source of the appropriate dopant (phosphorus or boron) which diffuses into the underlying silicon wafer when it is subsequently heated to temperatures in the 1000°C range. Since the diffusion source is deposited at a relatively low temperature and covers the silicon wafer during the high temperature diffusion step, the wafer is protected during diffusion and problems of contamination are minimized. In addition, this process is much more readily controlled and gives more reproducible results than earlier diffusion techniques. Additional applications for this new technology, which is already employed in the manufacture of RCA semiconductor devices, are now being investigated. Other solid diffusion sources are being evaluated in the diffusion and passivation group and problems encountered with earlier diffusion techniques are being examined so that the broadest possible range of technology will be available to device designers.

Passivation

Passivation of a device implies that it is treated in some manner to make it insensitive to handling and to oxygen, water vapor, and other impurities in the environment. Early semiconductor devices were packaged in hermetic metal "cans" which provided this protection.

Recently, new processes have been developed that form a passivating layer directly on the surface of the device itself. For such passivated devices, the requirements placed on the outer package are relaxed, and less expensive packages—for instance those made of plastics—can be employed. As passivating layers, relatively thick layers of borosilicate glass can be used.[7] Such layers can be deposited from silane and diborane, as described above. Lay-

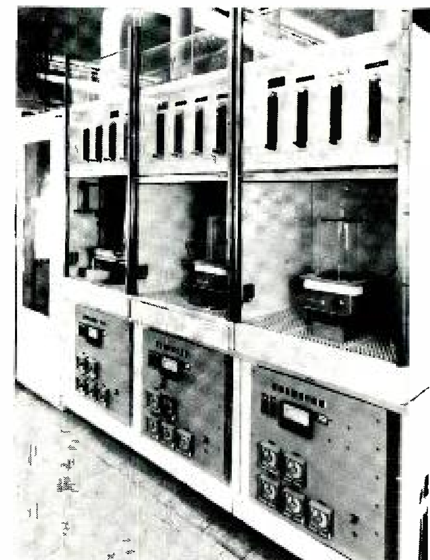

Fig. 2—Apparatus for the chemical vapor deposition of silicon dioxide layers from silane.

ers of silicon nitride are also used for passivation because this material is impervious to alkali metal ions. Silicon nitride can be deposited on a substrate by a variety of techniques such as the reaction of silane and ammonia. Even in layers only about 100 nm thick, silicon nitride provides a remarkable degree of passivation; the stability of "beam-leaded" semiconductor devices[8] depends on these layers. The Diffusion and Passivation group is investigating these and other potential passivating layers such as aluminum oxide, as well as combinations of two or more insulator layers to determine what materials and processes will passivate a given device structure.

Photoresists and polymers

Photoresists are probably the most "arty" and the least understood and controlled of the materials used in semiconductor manufacture. Organic rather than inorganic, they tend to be thermally unstable and their properties are relatively difficult to control.

Since they are light sensitive, photoresists are employed to create patterns in silicon dioxide and other insulating layers, in silicon, and in the metals used in the construction of semiconductor devices. Photoresist patterns are employed when exceptionally fine detail is required, as in the preparation of integrated circuits and overlay transistors.

Commercially, many photoresists are available, each with its own particular advantages and disadvantages. On of the principal goals of the Photoresists and Polymers group is to characterize these photoresist materials and to recommend photoresists for a given application. In addition, the group evaluates commercially available apparatus for the exposure of photoresists (aligners). RCA #1 photoresist, a development of the Laboratories at Princeton, is prepared by this group and made available at nominal cost to RCA users.

Polymer materials evaluated in the photoresist group include junction coatings and encapsulants. A wide variety of commercially available epoxy and silicone materials have been tested and, through close working relationships with the manufacturers, special formulations of plastics have been supplied for testing by RCA. The materials now used for plastic encapsulation of linear integrated circuits, for example, were formulated especially for RCA's use through the efforts of this group. As our understanding of the parameters that govern the suitability of an encapsulant (*e.g.* thermal expansion coefficient, adhesion to the die or metal lead frames, optimum curing times and temperatures) improves, the polymer materials can be better controlled, and standards for testing incoming materials can be set up.

One by-product of this work is the development of two new screenable molybdenum inks. These inks, prepared with new binders, give increased bond strength and finer line definition on screening than conventional molybdenum metallizer inks. Currently, these inks are used in the preparation of ceramic packages at Findlay. They are available to other RCA locations at nominal cost.

Metalization

As integrated circuits become larger and more complex, the quality of the metalization that interconnects individual transistors, resistors and capacitors in a circuit becomes more and more important in determining performance and reliability. For integrated circuits manufactured by RCA, either aluminum or the newer "beam lead" metalizations — *e.g.*, titanium-platinum-gold—is employed. These materials are deposited by vacuum evaporation or sputtering, the equipment for both of these processes being closely related. Improvements in the combinations of materials and in the deposition techniques are being sought by the Metalization group. A major goal is to apply the beam lead metalization concept, originally developed for bipolar integrated circuits, to MOS field effect transistor arrays, a technology area in which RCA has pioneered.[9] A second goal is to devise a multilayer metalization scheme for beam leaded devices. To help understand the limitations of the various metalization materials, a program to understand and control failure modes, particularly failure by "electromigration," is being pursued.

The Metalization group is also responsible for scaling up the new technology of aluminum evaporation with an RF bias[10] and taking it from the Princeton Laboratories into manufacturing areas. For this purpose, production prototype equipment has been designed and built at the Solid State Division (Fig. 3).

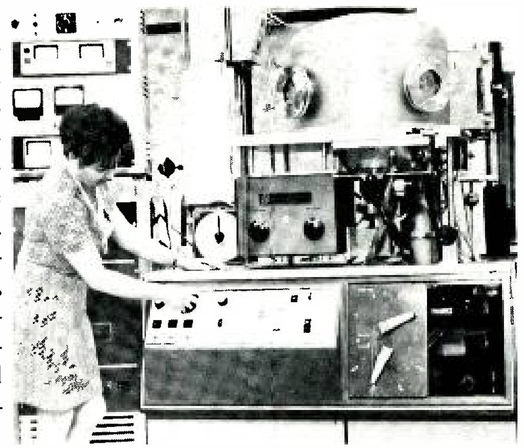

Fig. 3—RCA modified apparatus for the deposition of aluminum with an RF-bias..

Sputtering techniques are useful not only for the deposition of almost any material—insulator, semiconductor, or metal—but also for the removal of almost any material by "sputter etching". With appropriate photoresists, such as RCA #1 mentioned above, extremely fine patterns having vertical walls can be defined in silicon dioxide and other materials such as chromium. Although the use of sputtering in the processing of semiconductor devices is relatively recent, it promises to become an important new manufacturing technique.

Metallurgy and bonding

The Metallurgy and Bonding group's primary concern is with the metallurgy employed in fabricating discrete power transistors. Many of RCA's power devices are metalized with nickel rather than with aluminum. These nickel-metalized chips are subsequently mounted and connected in a package by solder reflow techniques. This type of construction is simple and inexpensive.

New electroless nickel baths have been devised both at the Princeton Laboratories and in the Metallurgy and Bonding group.[11, 12] These baths give improved control over the nickel deposition process and permit satisfactory plating even of polished silicon

Fig. 4—Scanning electron microscope used in the diagnosis of faults in solid-state devices and integrated circuits.

surfaces, thus eliminating a roughening step required in conventional wafer processing. With these nickel deposits, delamination problems are minimized and bonding ability is improved. The purity of the baths can be closely controlled because they are formulated in-house.

In addition, the nature of the failure occurring during thermal cycling of soldered-down chips is under investigation. New solder systems offer the promise of greatly improved thermal cycling capability compared with the solders previously employed.

The Metallurgy and Bonding group also performs failure analysis of various types of packages for semiconductor devices, and provides the cross-sectioning and metallurgical polishing services necessary for this analysis. Another service provided in the group is the plating of a variety of piece parts by new electroless and electroplating methods.

The Metallurgy and Bonding group also possesses expertise on ultrasonic and thermo-compression bonding techniques. They evaluate bond strengths and recommend the most appropriate bonding equipment for a given application.

Analytical techniques and device failure analysis

The newly formed Analytical Techniques and Device Failure Analysis group brings together a wide variety of physical and chemical analysis techniques used to define failure mechanisms, particularly failure mechanisms related to processing. A recent major acquisition is the scanning electron microscope shown in Fig. 4. With this instrument, it is possible to examine samples up to 1 inch across with no change in the sample chamber. With slight modification, samples up to 3 inches across can be accommodated. Besides serving as a high-resolution microscope, this instrument permits a determination of the chemical composition in a given area by analysis of the X-rays emitted during electron bombardment. Examination of infrared radiation emitted by the sample during bombardment is also possible. With this flexibility, the instrument will add significantly to the group's ability to diagnose failure mechanisms in semiconductor devices.

Other analytical techniques available in this activity include X-ray diffraction, X-ray fluorescence, X-ray shadowgraph, gas chromatography, atomic absorption, infra-red and ultraviolet absorption spectroscopy, emission spectroscopy, wet chemical analysis, and thermogravimetric analysis. Additional analytical techniques, including mass spectrometry of gasses and solids, X-ray topography, etc. are available through the courtesy of other RCA divisions, particularly the Laboratories at Princeton and Electronic Components in Harrison.

One of the goals of this group is to provide water analyses on a regular basis for divisional locations requiring the highest purity water. Techniques for carrying out these analyses have been devised at the Princeton laboratories. With these techniques, the quality of water purified by various methods, including ion exchange, filtration through micropore filters, and reverse osmosis, is being determined. Recommendations concerning the type of equipment needed for a given application will be available upon completion of this study.

A future goal of the group is to provide ultra-pure reagents, particularly hydrofluoric acid which is widely employed in silicon device processing. The group is seeking new purification techniques for reagents and improved methods of analyzing incoming materials.

Device failure studies

The device failure analysis program involves a study of the processes currently employed in silicon device manufacture. With the help of chemical analysis techniques such as solids mass spectrometry, and techniques for determining crystalline defects, such as X-ray topography, the "quality" of a silicon wafer can be monitored at various stages in its processing. From these studies, imperfections introduced by individual processing steps can be defined, and the process can then be modified to minimize or eliminate these imperfections. In addition, mechanisms for understanding the failure of silicon devices during life testing are developed in this group. With the aid of appropriate models based on these mechanisms, processes can be changed to eliminate the failure modes.

Summary

A wide variety of materials, processes and diagnostic techniques related to the fabrication of solid state devices is available in the Materials and Processes Laboratory of the Solid State Technology Center. These technologies are available to all RCA technical personnel. Requests for information can be addressed either to the author or to the appropriate leaders named above.

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Silicon-on-sapphire, the ultimate MOS technology

E. J. Boleky | Dr. P. A. Crossley | J. E. Meyer | S. G. Policastro | Dr. W. C. Schneider

To date, MOS arrays have been characterized by relatively slow operating speeds because of harmful parasitic capacitance. Silicon-on-sapphire technology virtually eliminates parasitic capacitance which seriously degrades the performance of bulk silicon MOS circuits, and MOS/SOS transistors with performance comparable to that of bulk silicon. MOS transistors can be fabricated in a thin single crystal silicon film grown on the insulating sapphire substrate. Fullest advantage of the low capacitance is realized in complementary symmetry circuit configurations which give the highest speed with minimum power and circuit complexity.

Authors Meyer, Policastro, Boleky, Crossley, and Schneider (left to right).

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received his BSEE from Rutgers University in 1961, and the MSEE degree from the University of Pennsylvania in 1964. He is presently completing his work for the Ph.D. in Electrical Engineering at Rutgers University. From 1961 to 1963, he worked as an engineer in the Missile and Space Vehicle Department at General Electric, where he was engaged in the design of attitude control systems. From 1963 to 1964 he worked in the Physics Department at Princeton University as a member of the technical staff where he designed RF and digital instrumentation for the cyclotron group. Mr. Meyer joined RCA Laboratories in 1964 where he was engaged in research on integrated circuits in both the silicon and thin-film technologies. He has received two RCA Laboratories Achievement Awards—in 1966 for his work on a solid state image sensor and in 1969 for his part in a team effort to develop complex silicon-on-sapphire integrated circuits. Mr. Meyer has published five papers, holds one U.S. Patent, and has several others pending.

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received the AB in chemistry, in 1953, from Rutgers University and the MS in physical chemistry in 1960 from Seton Hall University. After two years in military service he worked in the chemical field from 1955 to 1959 when he joined RCA in Solid State Division. At RCA, he has been responsible for developing many of the techniques used in the chemical analysis of semiconductor materials. He has done extensive work on the control of leakage currents in alloy devices using desiccants for which he received a team engineering award in 1961. He has also done extensive work in designing and developing silicon devices and has been involved in the development of pilot operations for RCA's COS/MOS line. After spending two years with Ragen Semiconductor, he returned to RCA in 1970 where he has been involved in the process development of silicon-on-sapphire technology.

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received the BSEE from the University of Pennsylvania, in 1966, and the MSE from Princeton University, in 1968, specializing in semiconductor device physics. He has also taken graduate courses in physics at Rutgers University. Mr. Boleky joined the staff of RCA Laboratories in June, 1966, and has engaged in research on MOS device modeling, the computer analysis of CMOS decoders, and the design of harmonic multipliers for UHF synthesis. His present responsibilities include the development of fabrication techniques to optimize the performance of CMOS silicon-on-sapphire transistors and the development of a high-speed programmable read-only memory using silicon-on-sapphire diodes. He was the recipient of an RCA Achievement Award in 1969 for his contributions to high-speed silicon-on-sapphire integrated circuits. He has published two technical articles and has six patents pending on the fabrication of semiconductor devices. Mr. Boleky is a member of Tau Beta Pi, Eta Kappa Nu, and the IEEE Electron Device Group.

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received a Scholarship to Emmanuel College, Cambridge, in 1959, and received the BA degree from the University of Cambridge in 1962. He received the PhD. degree from the same institution in 1965, having done thesis research on the formation of thin films of GaAs under vacuum. He joined RCA in December 1965, as a Member of the Technical Staff of RCA Laboratories. He worked in the Physical Research Laboratory of the Astro-Electronics Division, in the area of photovoltaic devices for solar energy conversion. In July 1968 he joined the Integrated Circuit Facility of RCA Laboratories, where he has worked on methods for fabricating complementary bipolar integrated circuits, and on silicon-on-sapphire epitaxy. He is a member of IEEE and Mensa.

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THE ADVANTAGES OF THE MOS TRANSISTOR as a basic element in large scale digital arrays have been extensively described. Chief among these are processing simplicity, large packing density, and low power dissipation, all of which enable fabrication of complex arrays with high yields and low cost. To date, however, MOS arrays have been characterized as well by relatively slow operating speeds due to harmful parasitic capacitance. In spite of this, it can be shown[1] that on the basis of transit time considerations, the MOS device is capable of high frequency performance previously thought attainable only by the bipolar transistor. A comparison of the respective transit time expressions for a representative n-p-n bipolar transistor and a NMOS transistor, as shown in Fig. 1, indicates that the NMOST should switch as fast as the n-p-n bipolar.

Approaching the upper limits of the bipolar transistor in digital systems has necessitated the use of high-power, nonsaturating current-mode logic. Comparable high speed performance at comparable supply voltages with nanowatts-per-bit of standby power dissipation can be obtained from the MOS transistor only by utilizing a technology which combines the best features of thin-film and monolithic silicon technologies in the environment of large scale integration. The silicon-on-sapphire (SOS) approach comes closest to realizing these desirable features since MOS/SOS devices with effective mobilities comparable to those of bulk silicon MOS devices can be fabricated in a thin single crystal silicon film grown on the insulating sapphire substrate.[2] The use of the thin-film silicon virtually eliminates the parasitic capacitance which seriously degrades the performance of bulk silicon MOS circuits. Fullest advantage of the low capacitance is realized in complementary symmetry circuit configurations which give the highest speed with minimum power and circuit complexity.

Complementary symmetry circuits are most easily assembled by fabricating the MOS transistors and crossovers in thin films of single-crystal silicon grown on an electrically insulating substrate, such as sapphire. All unused silicon is removed from the substrate, leaving perfectly isolated islands of silicon for transistors and crossunders, as shown in Fig. 2. Note that the silicon is one μm thick, allowing the source and drain regions of the transistors to be through-diffused to the sapphire. This reduces the capacitance of the source and drain regions by a factor of 20 over bulk silicon devices. Since the devices are isolated by the sapphire, no thick oxides are needed for isolation. All metalization and crossunders sit directly on the sapphire, eliminating all wiring capacitance and diffused crossunder capacitance found in bulk silicon MOS circuits. It is therefore clear that one of the most obvious advantages of silicon-on-sapphire (SOS) MOS technology is the tremendous reduction in parasitic capacitance.

There are also several less-obvious advantages of SOS. Normally each isolated channel region of the MOS transistors in the arrays is left floating i.e. no electrical contact is made to it. The floating results in two benefits: first, the source-bias effect on the threshold voltages is eliminated because the channel always floats at 0.7 V above the source voltage and second, all parasitic bipolar transistor action is eliminated because the base (channel) region is floating. Finally, SOS technology allows greater flexibility in reducing the carrier concentration in the channel silicon because the field inversion problem has been eliminated.

Fabrication

Great difficulty has been experienced and reported by workers[3] attempting to build high-quality active silicon devices on sapphire substrates by the straightforward application of standard bulk silicon technology to heteroepitaxial films. These difficulties can be traced, in general, to two problems.

The first is the contamination from the substrate, epitaxial system, or handling procedures, and the second is the disorder in the epitaxial layer caused by the growth interface. Silicon processing must be adjusted to account for these deviations in properties if devices and circuits are to be fabricated in heteroepitaxial material.

Table I is a comparison of some of the physical characteristics of the components of the heteroepitaxial system that must be taken into account if high quality silicon-on-sapphire devices are to be built. From these data, it is evident that some physical stress and dis-

Table I—Physical characteristics of heteroepitaxial system components.

	Silicon (Si)	Sapphire (Al_2O_3)
Crystal Unit cell (A)	face-centered cubic a=5.4301	r=4.758 a=12.991
Density (g/cc)	2.33	3.98
Hardness (Mohs)	7	9
Melting point (°C)	1412	2030
Dielectric constant	11.7 (500 Hz–30 MHz)	9.4 (⊥ to C-axis) (100 Hz–100 kHz)
Dissipation factor tan δ		10^{-3}–10^{-4}
Refractive index	3.4975 (at 1.357 μm)	1.7707 (at .5461 μm)
Thermal conductivity cal/cm-sec•°C at 25 °C	0.30	0.065 (60° to C-axis)
Thermal expansion coefficient 1/ °C (25–800°C)	3.59×10^{-6}	8.4×10^{-6} (60° to C-axis)

$$T_{MOS} = \frac{4}{3}\,\frac{L^2}{\mu(V_{gs}-V_T)} \qquad T_{BIPOLAR} = \frac{W_B^2}{2.4\times\mu\left(\frac{kT}{q}\right)}$$

FOR TYPICAL VALUES

L = 8 micrometer; μ = 350 cm²/v-sec; $V_{gs}-V_T$ = 10v

W_B = 1 micrometer; μ = 600 cm²/v-sec for npn ρ_B = 1 Ω-cm; $\frac{kT}{q}$ = 26 mv @ 300K

T_{MOS} = 0.26 ns $\qquad$ $T_{BIPOLAR}$ = 0.27 ns

Fig. 1—Comparison of typical MMOST and n-p-n bipolar transit times.

Silicon
SiO_2 (Thermal)
Al Metal

Fig. 2—Typical SOS transistor and crossover.

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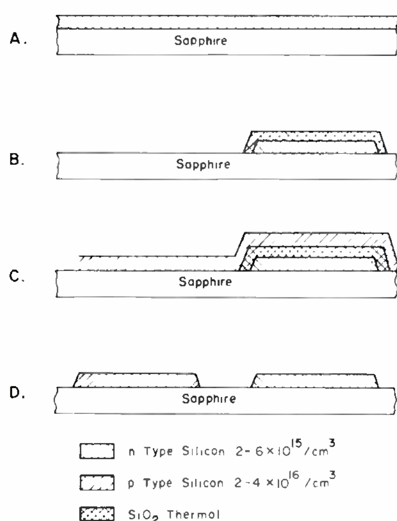


Fig. 3—Two-stage epitaxial process substrate preparation.

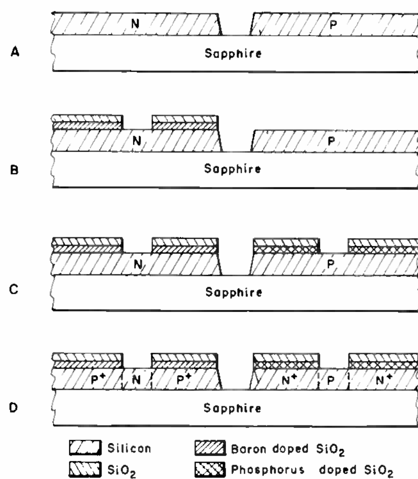


Fig. 4—Two-stage epitaxial CMOS/SOS process.

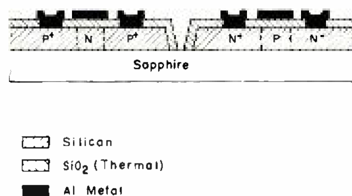


Fig. 5—Completed CMOS/SOS structure.

order due to the mismatch of these characteristics is inevitable.

Comparison of what is known to occur in bulk silicon and what is observed in silicon-on-sapphire yields some insight into the processing considerations. The change of diffusion coefficient in bulk silicon is a function of surface concentration and dislocation density. The distribution of disorder sites in silicon-on-sapphire has been shown to be highest at the silicon sapphire interface and decreases as the thickness of the film increases.[4] Due to this distribution, there is a change in diffusion coefficient causing impurities to move faster as they penetrate the film. In addition, SOS has no bulk silicon substrate to dilute the fast diffusing contaminants since the substrate can contribute to the contamination (Al, O_2, etc.), much greater care must be taken in handling and substrate preparation. This consideration is especially important because contaminants have an affinity for disorder sites.

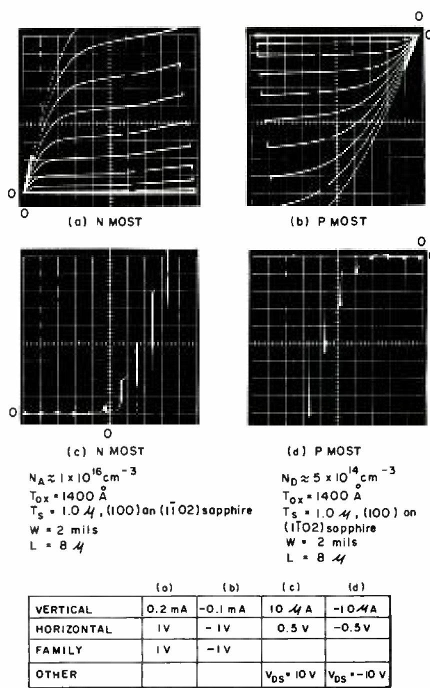
From the previous discussion it is apparent that bulk silicon technology is not directly applicable to the fabrication of high quality complementary MOS devices on sapphire substrates. Oxidation must be eliminated where possible, and the time that the wafer is exposed to high temperatures must be minimized[5].

CMOS/MOS transistors

To fabricate a CMOS/SOS transistor pair, a process has been developed which utilizes two heteroepitaxial growth steps to provide opposite conductivity-type SOS for enhancement-type CMOS transistors. The PMOST is a p^+-n-p^+ structure and the NMOST an n^+-p-n^+ structure as in bulk silicon CMOS technology. The process sequence and finished device structures are shown in Fig. 3, 4 and 5. In this two-stage epitaxial CMOS/SOS process, the p-type silicon is doped at a level of $N_A = 2\text{-}4 \times 10^{16}$ cm^{-3} and the n-type silicon is doped at a level of $N_D = 2\text{-}6 \times 10^{15}$ cm^{-3}. Both films are nominally one μm thick. The first two steps (Fig. 3) involve the epitaxial deposition of an n-type starting substrate material and its definition into islands for the PMOS transistors. This is then followed by a second epitaxial deposition of p-type material and its subsequent definition into islands for the NMOS transistors. As shown in Fig. 4b and 4c, the channel regions of the NMOST and PMOST are defined by etching gaps in the boron and phosphorus doped-oxide diffusion sources in two separate steps. All diffusants are driven in simultaneously by a single high-temperature step. The resulting cross section is shown in Fig. 4d. The process is continued by removing all oxides and growing a uniform clean channel oxide. Finally, contact holes are defined in the oxide, and aluminum is deposited and defined for gates and interconnections. The structure is then as shown in Fig. 5. This process requires six masks.

Typical aluminum-gate CMOS/SOS transistor characteristics are shown in Fig. 6, for the device and material parameters listed. The current-voltage characteristics are virtually identical to those of similar bulk silicon MOS transistors.

These structures are metalized with evaporated aluminum which can pose some problems in continuity due to the



	(a)	(b)	(c)	(d)
VERTICAL	0.2 mA	-0.1 mA	10 μA	-10 μA
HORIZONTAL	1 V	-1 V	0.5 V	-0.5 V
FAMILY	1 V	-1 V		
OTHER			V_{DS} = 10 V	V_{DS} = -10 V

Fig. 6—Typical characteristics of CMOS/SOS transistors.

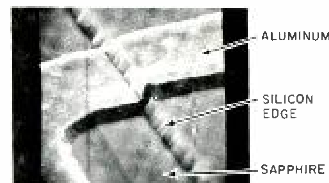


Fig. 7—Discontinuous aluminum at SOS step.

Fig. 8—Continuous aluminum at SOS step.

relatively large silicon steps the metal is required to pass over (≈one μm). Moreover, the silicon removal step can create a reverse tapered edge. Fig. 7 is a photomicrograph which clearly shows this problem. By carefully controlling the temperature and ingredients of the etch this problem can be minimized as shown in Fig. 8.

Testing

The initial evaluation of the silicon-on-sapphire technology for integrated circuits was done using the RCA CD-4007 (TA5388) COS/MOS Dual Complementary Pair Plus Inverter transistor configuration. This circuit comprises three n-channel and three p-channel enhancement-type MOS transistors on a single sapphire chip. Although these transistors are relatively large (W_N=7.5 mils, W_P=20 mils) compared to the transistors designed into the more complicated SOS circuits for memory applications, the CD4007 circuit has provided a base for rapid evaluation of SOS processing changes. The DC electrical characteristics of the individual devices can be conveniently measured using the in-house RCA Spectra 70 integrated-circuit tester.

Histograms were plotted and averages were calculated for the results of the oxide stress tests, leakage currents, threshold voltages, and transconductance (*gm*) measurements. Figs. 9 and 10 show normalized threshold voltages for NMOS and PMOS devices, respectively, on a CD4007 COS/MOS/SOS wafer. CD4007 SOS chips mounted in 14-lead dual-in-line ceramic-and-metal packages are presently on lifetest at RCA, Somerville.

Past, present, and future applications

High performance has been realized and demonstrated on complex circuit vehicles containing hundreds of complementary MOS transistors fabricated in silicon-on-sapphire films only one μm thick.

Following is a list of CMOS/SOS arrays and their important features that have been successfully fabricated to date:

256-Bit SOS diode ROM
- 18-ns access time in 4096 bit ECL system

16-Bit CAM (Content Addressable Memory)[6]
- 77 mils × 53 mils
- 224 MOS devices
- 10-ns write time at 10 V
- 14-lead flatpack package

50-Stage dynamic shift register[7]
- 72 mils × 105 mils
- 420 MOS devices
- 90 MHz speed at 20 V
- Total power (at 50 MHz and 10 V) = 7mW
- f_{min} = 200 kHz

Dual 8-stage correlator
- 92 mils × 124 mils
- 384 MOS devices
- 50 MHz speed at 10 V
- 28-lead flatpack

A photo-micrograph of the 50-bit shift register is shown in Fig. 11.

Present efforts on SOS technology are aimed at establishing a pilot line operation such that complex arrays can be fabricated in volume for yield evaluation. Vehicles for this evaluation will include a 256-bit CMOS/SOS static random access memory. This array will be TTL compatible at all inputs and will have performance comparable to presently available bipolar arrays at a fraction of the power dissipation. Future MOS/SOS integrated circuits will include self-aligned silicon-gate technology and shorter channel spacings making sub-nanosecond delays and extremely small power-delay products possible[8]. The extremely high performance, low power nature of SOS technology make it possible to trade-off some performance to provide lower voltage TTL-compatible MOS arrays. This would eliminate the need for special (expensive) high voltage TTL-MOS level shifters and thus minimize overall system cost.

Acknowledgment

It is a pleasure to acknowledge the contributions of A. C. Ipri and D. W. Flatley to the development of SOS fabrication technology. We also wish to thank G. W. Cullen, G. E. Gottlieb and J. F. Corboy for their contributions to the preparation of high-quality SOS films. The dual 8-bit correlator was designed and tested by W. F. Gehweiler of RCA's Advanced Technology Laboratories in Camden, N.J.

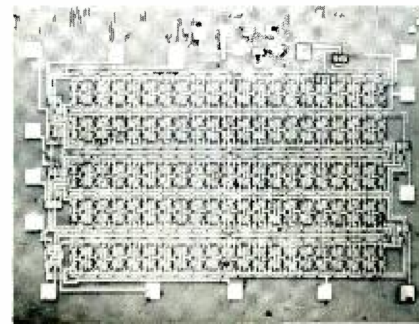


Fig. 11—Photomicrograph of 50-bit CMOS/SOS Dynamic shift register.

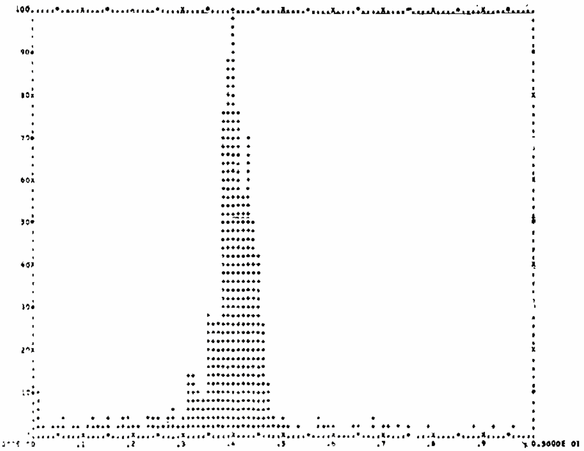


Fig. 9—Histogram of NMOS/SOS transistor threshold voltage. The average threshold voltage for the 831 devices tested (on 277 chips) was 1.949 V.

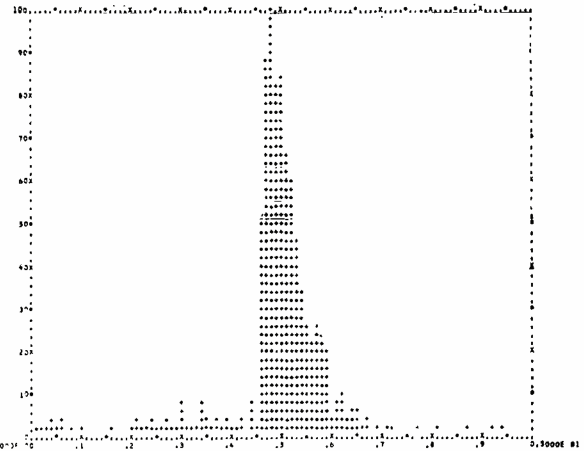


Fig. 10—Histogram of PMOS/SOS transistor threshold voltage. The average threshold voltage for the 831 devices tested (on 277 chips) is −2.449 V. The histogram does not indicate the sign of the threshold voltage.

W. R. Lile of RCA Laboratories was responsible for the testing of the 50-bit dynamic shift register. The program to develop high-performance SOS digital circuits is under the supervision of J. H. Scott, Jr.

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Beam-lead COS/MOS integrated circuits

L. A. Murray | B. W. Richards

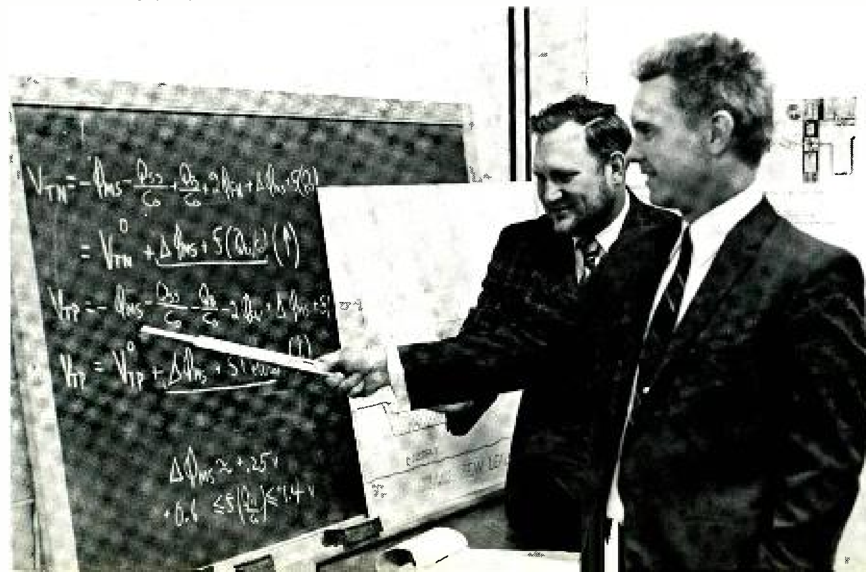
Complementary symmetry MOS (COS/MOS) circuits have been beam-lead interconnected and hermetically sealed using a process analogous to that of the bipolar beam-lead circuits. Outstanding differences between these techniques lie in the method used to deposit the hermetic layer, the silicide (Pd_2Si) employed as a low resistance contact to the source and drain regions, the metal (Pd) between the titanium and gold layers, and the metal deposition method used (evaporation). This paper discusses the advantages of these variants and the characteristics of the devices produced by this beam-lead process. In addition, this paper summarizes a palladium silicide contact resistance study and discusses the relationship between composite gate dielectric and device threshold and stability.

PERHAPS the most publicized advance in the semiconductor industry is the development of large-scale integrated (LSI) circuits. Such circuits bring the semiconductor manufacturer directly into the fabrication of subsystems and a few steps away from complete system construction. There are two ways of reaching the goals of the large-scale integration: one is by placement of all the circuits on a few very large chips, another is by use of a large number of smaller integrated circuits, beam-lead bonded onto a single ceramic substrate. While the first approach seems the more reasonable, it has the shortcoming in that the yield of useful circuits drops drastically as the chip areas increase, so that, beyond a certain chip size, LSI becomes economically infeasible. The maximum length and width of an economically producible chip increases each year and is presently in the 0.15 to 0.20 inch range. Even with use of densely packed MOS devices, these sizes cannot accommodate the required number of circuits. For this reason, smaller beam-lead chips represent the more practical processing alternative. Because semiconductor complexity and system demands continually increase, it is likely that the beam-lead approach will be more practical, even as the chip area increases manifold.

Lawrence A. Murray, Ldr., Solid State Technology Center, Solid State Division, Somerville, N.J., received the BS in Physics from Notre Dame in 1953. After discharge from the Signal Corps in 1955, he joined ITT as a Research and Development Physicist where he grew and measured the properties of various semiconductor crystals for solid state applications. After participating in research on a microwave-infrared optical maser program in 1961, he joined RCA. Since then he has been an engineering leader heading up an assortment of diverse groups working on III-V crystal growth, laser crystal research, development of non-destructive measurement of crystal properties, fabrication of LED solid state displays, development of improved processes for MOS devices and the fabrication of COS/MOS integrated circuits. In the latter capacity, he was responsible for the development of a beam-lead COS/MOS process and for the fabrication of radiation resistant COS/MOS devices among other assignments. Mr. Murray is the author of two dozen technical papers and presentations.

Bennett Richards, Jr., Materials and Processes, Solid State Technology Center, Solid State Division, Somerville, N.J., received the BS in physics from Penn State in 1957 and joined the RCA Laboratories. In 1964 he transferred to the Advanced Development group at Somerville, New Jersey, where he worked on a variety of MOS projects including a 30-MHz, 5-watt device, and an early medium-scale COS/MOS integrated circuit, a counter-decoder. He is a charter member of the Technology Center at Somerville, and has worked on beam lead COS/MOS integrated circuits since the time of the creation of the center.

Authors Murray (left) and Richards.



Background

Because MOS devices can be made much smaller than bipolars and hence many more devices can be put in a given area, MOS technology is receiving the full thrust of LSI. Of the various MOS technologies, the complementary (COS/MOS) variation possesses a number of unique advantages—such as low power drain, flexibility, and high noise immunity—which cause it to be eminently suitable for beam leading for LSI use.

The electronic system chosen as a demonstration vehicle for beam-lead COS/MOS is an 8192-byte memory plane. Such a unit will contain beam-lead memory chips and beam-lead logic chips. The former is a decoded 256-bit chip and the latter include an octal two input NAND gate (TA6082), quad-three input NOR gate (RCA CD-4000), and the dual-D flip flop (RCA CD4013). However, to apply beam leads to these chips, new processes must be developed because the existing beam-lead processes are not compatible with MOS devices. The present technology fails in two cases:

1) In beam-lead bipolar integrated circuits,[1] the wafer is sealed with silicon nitride following the final diffusion and the nitride is opened up to expose the contact areas. Because the purpose of the nitride is to hermetically seal the chip from the influence of the ambient and not to take part in the electronic operation of the device, little care needs to be taken to ensure that the deposition be clean or reproducible. For bipolars then, the usual quartz-tube

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Table I—Insulator properties.

Property	Silicon Nitride Si_3N_4	Aluminum Oxide Al_2O_3	Silicon Dioxide SiO_2
Dielectric constant	6.9	9.4	3.8
Refractive index	2.05	1.74	1.46
Deposition rate	150A/min	100A/min	—
Etch rate (in 180°C phosphoric acid)	~100A/min	100A/min	negligible
Deposition temperature	1050°C	950°	—
Typical thickness of seal	350A	450A	—
Breakdown field strength	$6x10^6$V/cm	10^7volt/cm	$8x10^6$volt/cm

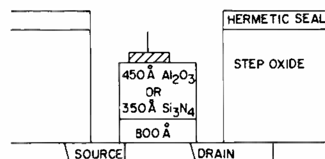


Fig. 1—Structure of a typical gate dielectric sandwich.

furnace may be employed. In MOS and COS/MOS devices, however, the silicon nitride layer is deposited over the channel oxide so that it becomes an integral part of the gate dielectric and strongly influences the electrical characteristics of the device. Any fixed or mobile charge in the nitride[2] thus leads to threshold voltage variation and instabilities.

2) Bipolar devices employ platinum for making a low-resistance contact to silicon and for the intermediate or blocking layer in the titanium-platinum-gold multi-layer metallization scheme. Because platinum must be heated considerably above 2000°C before appreciable evaporation occurs, standard methods are unsuitable and sputtering is substituted for filament evaporation. The sputtering process may not be used in MOS manufacture because high-energy electrons, X-radiation, and sputtered atoms introduce charges into the gate oxides causing the threshold to shift to more negative voltages. These charges cannot be totally removed in annealing. In COS/MOS, this results in the p-channel MOS devices becoming heavily enhanced and in the n-channel MOS devices becoming depleted.

To circumvent these difficulties, the methods used to deposit the hermetic seal and the metal have been changed. Instead of using a quartz-tube globar-type furnace to deposit the seal, an RF system is used. Because the walls of the RF deposition apparatus are cold, impurities do not diffuse through them from the external ambients, and any contaminants on them are not easily introduced into the deposition chamber ambient. In addition, the apparatus can be easily and routinely cleaned.

The problem of high evaporation temperature is resolved by substituting palladium for the platinum metal. For the most part, these two metals behave in an identical manner with silicon both chemically and electrically, but palladium can be easily evaporated from tungsten filaments in the neighborhood of 1600°C.

Deposition of the hermetic seal

A sandwich or composite dielectric seal is used in beam leads in place of a simple silicon dioxide gate. The purpose of the upper layer is to act as a hermetic seal to prevent sodium from diffusing through the silicon dioxide interface and to prevent the diffusion of water vapor and other ambients through to the semiconductor surface. The use of a single layer of some dielectric in place of silicon dioxide is precluded at this time because all suitable dielectrics in the technology interact with the silicon surface to form interface states. These states cause such phenomena as tunnelling, threshold shifts, and instability, which work to the detriment of MOS devices. The dual objectives of providing a gate with good electrical characteristics and hermeticity is best achieved by growing a clean silicon dioxide layer and capping it with a hermetic layer, thus forming a sandwich type of gate.

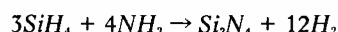
Two different insulators have been successfully used as seals for COS/MOS devices: silicon nitride and aluminum oxide. Both are put down in RF-heated systems and both are reproducibly clean. Before deposition of either of these seals, a clean channel oxide is thermally grown to a thickness of 800Å. The thickness of the hermetic seal layer is so chosen as to produce a composite channel having an effective thickness of 1000Å. Table I lists some insulator properties which affect MOS performance.

Silicon nitride

Silicon nitride[3] is an effective barrier to diffusion of sodium, which is a prime cause of failure of MOS gates. A layer as thin as 200Å suffices to seal the device. Unfortunately, the silicon nitride can be easily contaminated during growth and give rise to instabilities.

These problems surface most strongly for films grown in furnaces because of contaminants on, and diffusants through, the hot furnace walls. For this reason, an easily demountable and cleanable cold-wall RF deposition system was constructed to put down the silicon nitride. By careful cleaning of the gas lines, use of clean gases, and routine preventive maintenance, reproducibly clean nitride films have been regularly obtained.

To deposit such a film, device wafers are placed on a silicon-carbide-coated carbon susceptor and heated up to 1050°C in a forming gas atmosphere, and silane and ammonia are introduced into the chamber. These gases react to form silicon nitride as follows:[3]



$$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2$$

The silicon nitride deposits onto the wafer at the rate of 100 to 200Å/min. Residence time at the 1050°C temperature is kept to a minimum to prevent excessive lateral diffusion and excessive diffusion of the source and drains which would lead to narrow channel lengths and premature breakdowns. After deposition, a thin layer of silicon dioxide is deposited over the wafer to use as a mask to etch contact holes through the silicon nitride. Holes are cut into the SiO_2 mask, and the wafer is placed in a phosphoric acid-water mixture which boils at 180°C and attacks the nitride at the rate of 100Å/min. A buffered hydrofluoric acid etch completes the contact opening sequence by both etching through the rest of the silicon dioxide mask. The geometry resulting from such a procedure is shown in Fig. 1.

A positive charge occasionally is found at the interface between the thermal oxide and the silicon nitride. This charge is denoted as Q_{ii}. Because the charge is positive, it tends to shift the p-channel MOS thresholds towards more enhancement and the n-channel MOS thresholds towards more depletion values than would be calculated for a single silicon dioxide gate dielectric.

The use of a double-layer dielectric has some secondary advantages which

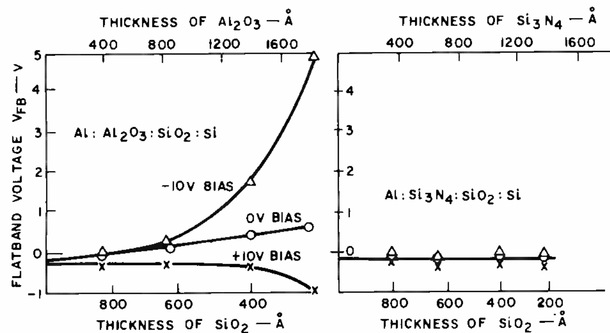


Fig. 2—Stability of the hermetic seals under capacitance-voltage-bias temperature as a function of sandwich thickness for *Al* metal.

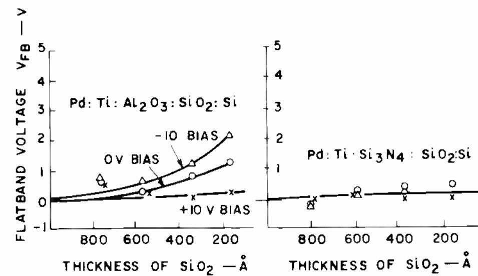
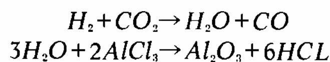


Fig. 3—Stability of hermetic seals under capacitance-voltage-bias temperature as a function of sandwich thickness for *TiPd* metal.

include: the Si_3N_4 layer prevents contamination of the devices during metallization so that rigid controls on this process can be relaxed, and the Si_3N_4 layers are redundant so that pinhole protection is excellent. For these reasons, very thin gate dielectrics can be used without excessive danger of failure due to pinholes. This feature is enhanced by the larger dielectric constant of the nitride which permits the use of a comparatively thick nitride layer. These considerations will apply as well to the alumina-silica seal.

Aluminum oxide

Alternatively, Al_2O_3[4] can be used in place of Si_3N_4. This layer is also put down in an RF system but at a comparatively low temperature of 925°C so that lateral diffusion is negligible even in protracted runs. The alumina is deposited through a two-step reaction of hydrogen, carbon dioxide, and aluminum chloride, as follows:



$$H_2+CO_2 \rightarrow H_2O+CO$$
$$3H_2O+2AlCl_3 \rightarrow Al_2O_3+6HCL$$

The first reaction takes place at elevated temperatures so that the water vapor forms only in the region of the heated silicon-carbide-coated carbon susceptors. The reaction between aluminum chloride and water vapor is rapid and the alumina forms on the wafer as soon as the water molecule forms. Aluminum chloride is a solid at room temperature, and its introduction into the deposition chamber is by sublimation; the process needs to be controlled by continually flushing the chamber with hydrogen to avoid any atmospheric leak that could result in immediate conversion of the chloride to the oxide. The sublimator is heated to a temperature at which the vapor pressure of the chloride is appreciable (between 105 and 115°C). Palladium-diffused hydrogen is used as a carrier gas to transport the sublimed material to the deposition chamber. The tube through which the $AlCl_3$ flows must be kept heated to prevent the gas from plating out as a solid and eventually plugging the system. Gas flow rates are set up so as to deposit the aluminum oxide at the rate of 100Å/min.

The contacts through the alumina-silica sandwich layer are defined with exactly the same procedure used in defining the nitride-silica sandwich. The major difference between these types of sandwiches is that the Q_{ii} (or ϕ_{ii}) found for the alumina silica sandwhich is negative and reproducible. [Some data have indicated that the shifts in threshold and flatband in Al_2O_3:SiO_2 are in part or in whole caused by a potential difference at the interface rather than a charge; for a fuller discussion see Ref. 5.] In practice, the flatband characteristics of capacitors made from alumina-silica sandwich layers are so reproducible as to lead to speculation that the Q_{ii} is inherent to the system and not merely a contaminant as was found to be origin of similar changes in SiO_2 and Si_3N_4[6,7]. The magnitude of this charge is approximately 1.3×10^{11} cm^{-2} and is *negative*. This condition causes the flatbands of the *Al* metal oxide capacitors to fall routinely in the −0.1 to +0.1V range; the p thresholds to move towards depletion; and the n thresholds toward more enhancement. The flat-bands of capacitors using titanium palladium metal are about 0.25 volt more positive, indicating that beam-lead metallization work function is more positive by this amount. Typical thresholds for devices produced by alumina-silicon nitride and thermally grown silica are given in Table II. Representative threshold values for single-layer alumina and silicon nitride are also included.

These data show that alumina-silica shift the thresholds and the devices to more positive values and the nitride silica to more negative values. In addition, pure alumina shifts so far positive and the pure silicon nitride so far negative that fabrication of enhancement p- and n-MOS COS/MOS devices is impossible with present standard processing. However, these shifts are not endemic to all alumina and nitride layers, so that in the future it is possible that more useful insulators may be deposited. The ability to shift or "dial in" thresholds by suitable dielectric selection should prove very useful in designing future MOS generations.

Data in Table II were specifically developed from the noted dielectric thicknesses and ratios. When the hermetic seal thickness is increased or the interface is brought nearer to the silicon substrate, different sets of thresholds occur.[8]

A set of experimental test matrices was investigated to determine the relationship between oxide thickness and threshold stability. Both Al_2O_3 and Si_3N_4 were investigated. The relative

Table II—Complementary MOS thresholds for various gate dielectric structures.

Gate dielectric	*Thickness (A)*	*n-threshold (V_{TN}) (volt)*	*p-threshold (V_{TP}) (volt)*	*Remarks*
SiO_2	1000	2.1	−1.8	*TiPdAu Metal*
Si_3N_4:SiO_2	350/800	1.9	−2.4	*TiPdAu Metal*
Al_2O_3:SiO_2	450/800	+2.5	−1.5	*TiPdAu Metal*
Si_3N_4	1000	(depletion)	−6.0	*Al* Metal
Al_2O_3	1000	+5.0	(depletion)	*Al* Metal

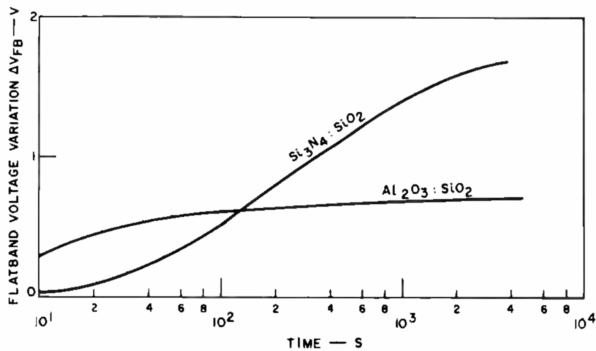


Fig. 4—Variation of flatband voltage with time at 300°C and −10-V bias using aluminum gate metal.

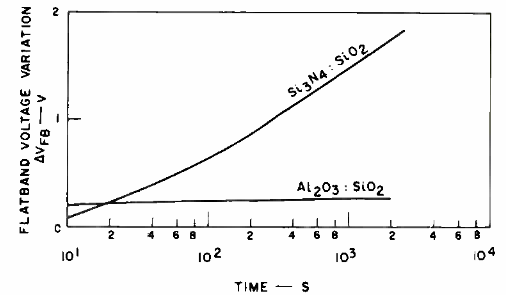


Fig. 5—Variation of flatband voltage with time at 300°C and −10-V bias using titanium-palladium gate metal.

thicknesses of the dielectrics making up the sandwich were so selected as to make composite layers having an effective thickness equal to 1000Å for SiO_2. The results of these studies indicate that gates with thick SiO_2 underlayers are stable for both Si_3N_4 and Al_2O_3 whether the metal system used is aluminum or titanium palladium, as can be seen by Figs. 2 and 3. On the other hand, the alumina sandwiches having thin SiO_2 underlayers are unstable while the comparable nitride layers are stable.

A further investigation of these layers involved prolonged testing at 300°C under −10-volt bias as shown in Figs. 4 and 5 which indicate the alumina tends to shift threshold at short testing times but the shift saturates early. Noticeable nitride shifts occur only after long testing times, but the voltage shift saturates at much higher values. It will be shown later that 125°C life test data indicate that these high temperature instabilities are not reflected by any change in device characteristics.

Beam-lead metallization

Because of the refractory nature of platinum, palladium is used as a substitute in manufacturing beam-lead COS/MOS devices. The palladium is employed twice. It is first evaporated to form palladium silicide contacts to the silicon, and then evaporated on top of the titanium layer. In both cases, the differences between the platinum and palladium layers is minimal save for the technique used for deposition.

Palladium silicide contacts

The palladium film is evaporated by the procedure discussed later in the section on Titanium-Palladium-Gold Metallization. To make low-resistance contacts to silicon, the evaporated palladium must be sintered to form a palladium silicide. The silicide that forms in the usable sintering temperature range is Pd_2Si. On extended heating, the palladium diffuses out of the silicide and further into the silicon, causing the contact resistance to increase. Thus, at each temperature, a broad resistance minimum is found for some sintering time where the resistance value at each minimum is approximately the same for every temperature. The relationships between sintering time and temperature are given in Figs. 6 and 7. In practice, any sintering temperature between 400 and 600°C may be chosen. Contact resistances were measured on 1-by-1, 0.5-by-0.5, and 0.3-mil openings and translated into units of ohm-cm².

The palladium silicide contact is not as resistant to chemical attack by etches as the platinum silicide contact. In fact, prolonged immersion in standard cleaning solutions tends to remove palladium silicide. This procedure causes the contact resistance to increase. However, a 1000Å layer of palladium is not affected as seriously by the cleaning solutions. This value (1000Å) is held as an upper limit to prevent the palladium silicide layer from penetrating the thin diffused source and drains.

To circumvent this attack of palladium silicide, the device wafers are etched after sintering mainly with water and hydrofluoric acid. These steps followed by a short SC1 etch (10s) with the SC2 etch being specifically excluded.

Titanium-palladium-gold metallization

A great advantage of the beam-lead system is that gold metallization is employed, so that highly reliable gold-to-gold bonds can be used in packag-

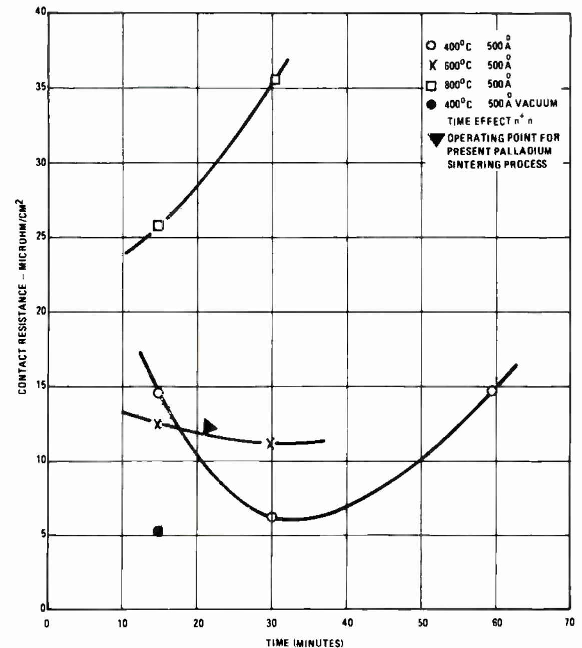


Fig. 6—Contact resistance as a function of sintering time —isothermal.

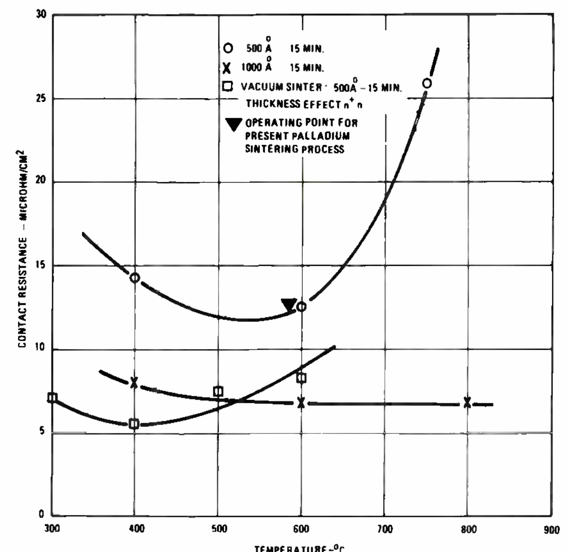
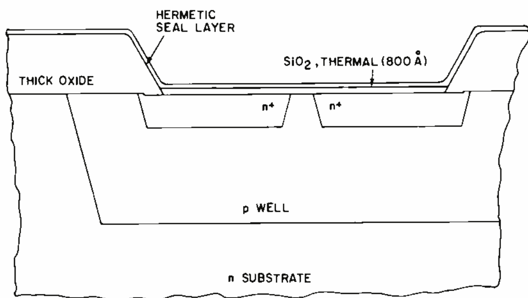
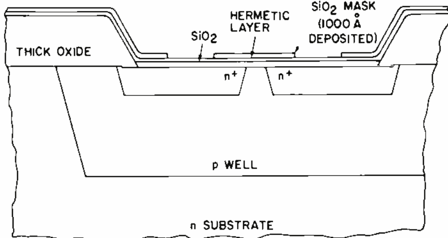


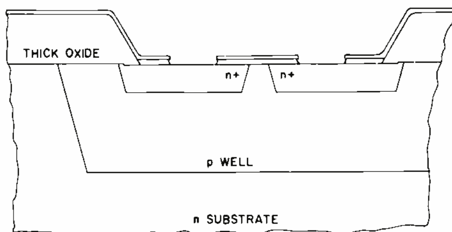
Fig. 7—Contact resistance as a function of sintering temperature.



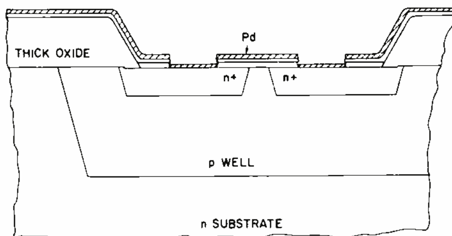
a)—Channel oxide grown and Al_2O_3 or Si_3N_4 deposited.



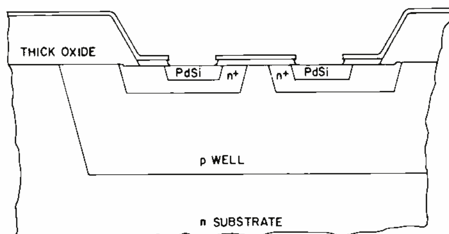
b)—SiO_2-etch mask deposited, photolithographically defined, and etched in contact area.



c)—Contact area etched through channel oxide.



d)—Palladium deposited.



e)—Palladium sintered into contact area and removed from oxide.

Fig. 8—Sequence used to deposit and define the hermetic seal and to form Pd_2Si for ohmic contact to the silicon.

ing. Because gold in direct contact with silicon or titanium degrades device performance, it must be separated from these materials by a barrier metal, a function served by both platinum and palladium. Because neither platinum nor palladium adhere strongly to oxide, an intermediate layer of titanium performs this function.

Both titanium and palladium are evaporated from tungsten filaments around which the metals are wound. Evaporation of a 1500Å layer of titanium from the first filament is followed by a 1500Å palladium layer evaporation from the second filament. Intermixing of the two metals is to be avoided to prevent the formation of an etch-resistant titanium-palladium alloy. The third metal layer, gold, can be evaporated at this point.

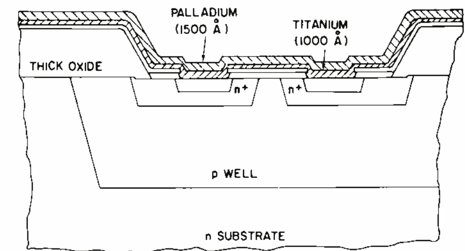
Alternatively, the gold can be electroplated. In this operation, the metal pattern is first defined in the palladium (leaving the titanium to act as a shorting path to carry the plating current), and then the wafer is coated with photoresist and the metal pattern is opened up for the plating operation. The gold plate thickness is kept below one micrometer to prevent shorts from developing between the gate and drain lines. Following this step, the beam leads are defined in photoresist and the leads are plated up to a thickness of 10 micrometers.

Extensive testing of this metallization system has indicated that the only difference between the titanium palladium gold, and titanium platinum gold is that the resistance of the interconnect metal lines in the former increase with heating at temperatures in excess of 300°C.

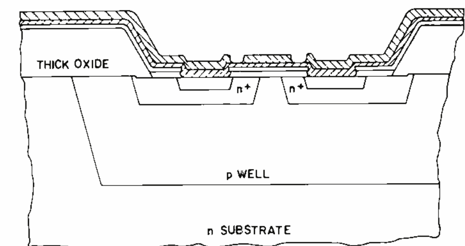
COS/MOS beam-lead process

Beam-lead bonding of COS/MOS integrated circuits has been accomplished through the introduction of a number of additional photoresist and processing steps. However, the processing is identical for both the standard and the beam-lead COS/MOS through the field-oxide step.

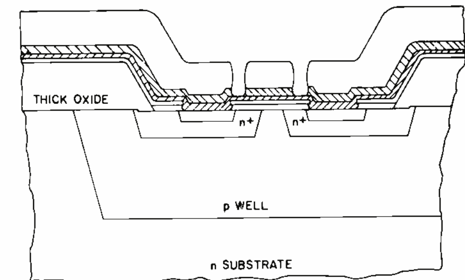
The masks required are listed in Table III along with a list of the masks used for standard processes. One beam-lead mask is eliminated (No. 7) if a three step *Ti-Pd-Au* evaporation is used. The sequence of steps used for beam-lead COS/MOS is illustrated in Figs. 8 and 9. Note that, contrary to bipolar processing, a grid-protect mask is not required in MOS.



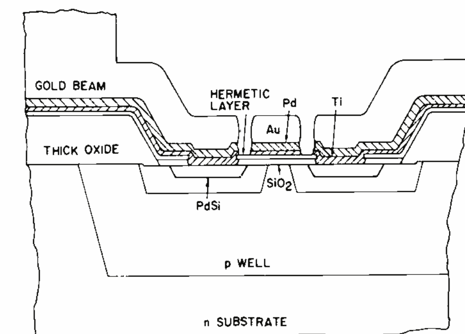
a)—Titanium and second pallidum layer deposited.

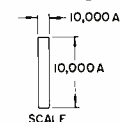


b)—Palladium layer defined into interconnection pattern.



c)—First layer of gold electroplated.





d)—Gold beams plated up and titanium removed.

Fig. 9—Sequence used to deposit and define beam-lead metal for interconnection and beam-lead patterns.

Table III—Masks required for standard and beam-lead COS/MOS integrated circuits.

Standard process	Beam lead process
1. Well diffusion	1. Well diffusion
2. p+ transistor and guard-band diffusion	2. p+ transistor and guard-band diffusion
3. n+ transistor and guard-band diffusion	3. n+ transistor and guard-band diffusion
4. Field-oxide diffusion	4. Field-oxide definition
5. Contact definition	5. Contact definition
6. Metal pattern (Al Definition)	6. Metal pattern (*Pd* definition)
7. Protective oxide	7. Reverse metal pattern (*Au* plate)
	8. Beam-lead pattern and protective oxide
	9. Separation

Fig. 10 is a photograph of the RCA CD4007, commonly called the sampler, which was the first beam-lead COS/MOS device. Each of the six p- or n-MOS devices can be individually addressed and monitored, thus this pattern makes an ideal test vehicle. The data developed in the article were measured on this test vehicle. Fig. 11 is a photograph of the RCA Dev. No. TA6082, an actual two-input NAND gate, and Fig. 12 shows the CD4000, a dual three-input NOR gate. These three integrated circuits have been fabricated using the beam-lead processes described. Fig. 13 shows a microbridged substrate to which various beam-lead chips have been bonded.

Device test results

Extensive parametric and diagnostic tests have been performed on the sample beam-lead chips. These tests indicate that the COS/MOS devices fabricated with the beam-lead process have essentially the same electrical and parametric characteristics as standard COS/MOS product except for threshold (see Table II). Leakages, transconductances, voltage breakdown, and contact resistance for devices processed in both ways are comparable, and average data of these parameters are the same as for the standard-processed COS/MOS devices. Although both the silicon nitride and the aluminum oxide can be employed in this process, some fine tuning of the COS/MOS process is required for either insulator to achieve matched n and p thresholds.

Life-tests

The CD4007 was tested with time at 125°C and under ±10-volt biases; measurements were averaged over 30 devices. The test results show that the electrical characteristics of sealed-junction beam-lead devices for both Al_2O_3 and Si_3N_4 are as stable as devices made with standard processing when tested to the 125°C specification. These devices prove superior when tested more severely at 300°C or when subjected to junction-seal integrity tests and pressure-cooker tests.

Summary

A sealed-junction beam-lead process has been developed for COS/MOS devices. The process has been applied to five RCA production circuits and is being extended to a number of more complex circuits such as a 256-bit memory. Computer controlled testing, yield analysis, parametric analysis, and life tests indicate the utility of the beam-lead process. With the implementation of beam-lead COS/MOS, the door is opened to the manufacture of multichip integrated-circuit subsystems. As an example, 8192-byte memory boards made up of beam-lead 256-bit memory chips and beam-leaded octal two-input NAND gates are presently being fabricated. In addition, mixed-technology beam-lead systems such as a frequency synthesizer are being developed.

Acknowledgements

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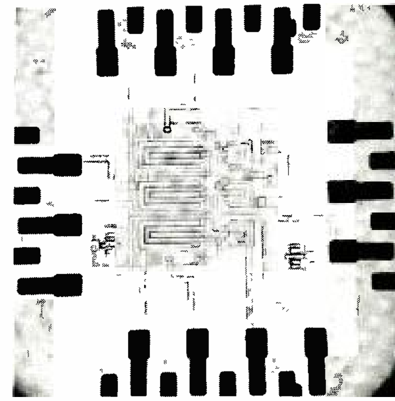

Fig. 10—The beam-lead version of CD 4007.

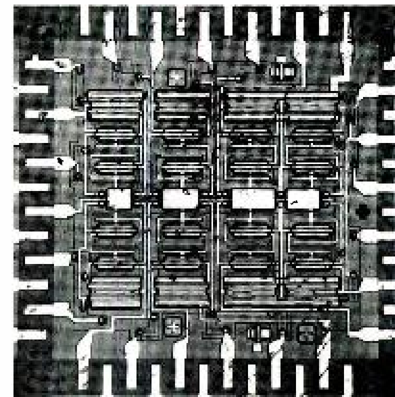

Fig. 11—The beam-lead version of the RCA Dev No TA 6082.

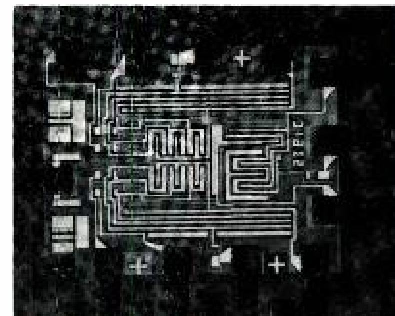

Fig. 12—The beam-lead version of CD 4000.

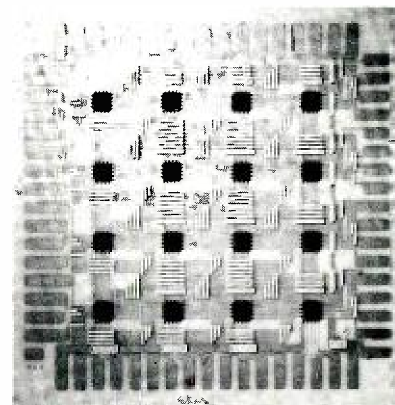

Fig. 13—A microbridged substrate to which various beam-lead chips have been bonded.

Packaging concepts for beam-lead devices

A. S. Rose | W. D. Bailey | H. Fenster | W. J. Greig

The use of precious-metal conductor-beams and leads in integrated circuits has led to greater reliability and more cost-effective packaging of individual chips as well as large-scale hybrid arrays. In addition, beam-lead technology allows greater design complexity in simple packages that can be handled by high-volume production equipment with more effective quality control.

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SEALED-JUNCTION, BEAM-LEAD INTEGRATED CIRCUITS offer the system designer a new freedom of package selection with greater versatility and cost effectiveness complemented by increased reliability. The characteristics of beam-lead devices, fabricated as shown in Fig. 1, that permit this freedom are:

> Leads are bonded to the substrate metallization by thermocompression of mating gold surfaces using commercially available equipment to make multiple connections simultaneously.
>
> The surface passivation layer of silicon nitride, applied as an integral surface layer, resists penetration at high temperatures by channel-inducing alkaline-ion impurities.
>
> Precious metal structures, such as that shown in Fig. 2, provide interconnection networks on the device and peripherally extended gold beams, as shown in Fig. 3. The elimination of aluminum as an ohmic contact and as a bonding pad has removed the potential for electromigration, hillock formation, spiking, and other debilitating mechanisms which accompany high temperatures and currents.

Principally as a result of the elimination of corrosion-susceptible aluminum, precious-metal beam-lead sealed-junction chips may be packaged in non-hermetic enclosures. This liberation from hermetic sealing has opened vistas for innovative packaging concepts readily adaptable to the most complex electronic systems.

Packaging

Customers for integrated circuits generally have requirements in two classifications: single chips, or multichip hybrid assemblies.

Single-chip utilization

It is common practice to insert single-chip dual in-line packages into printed-

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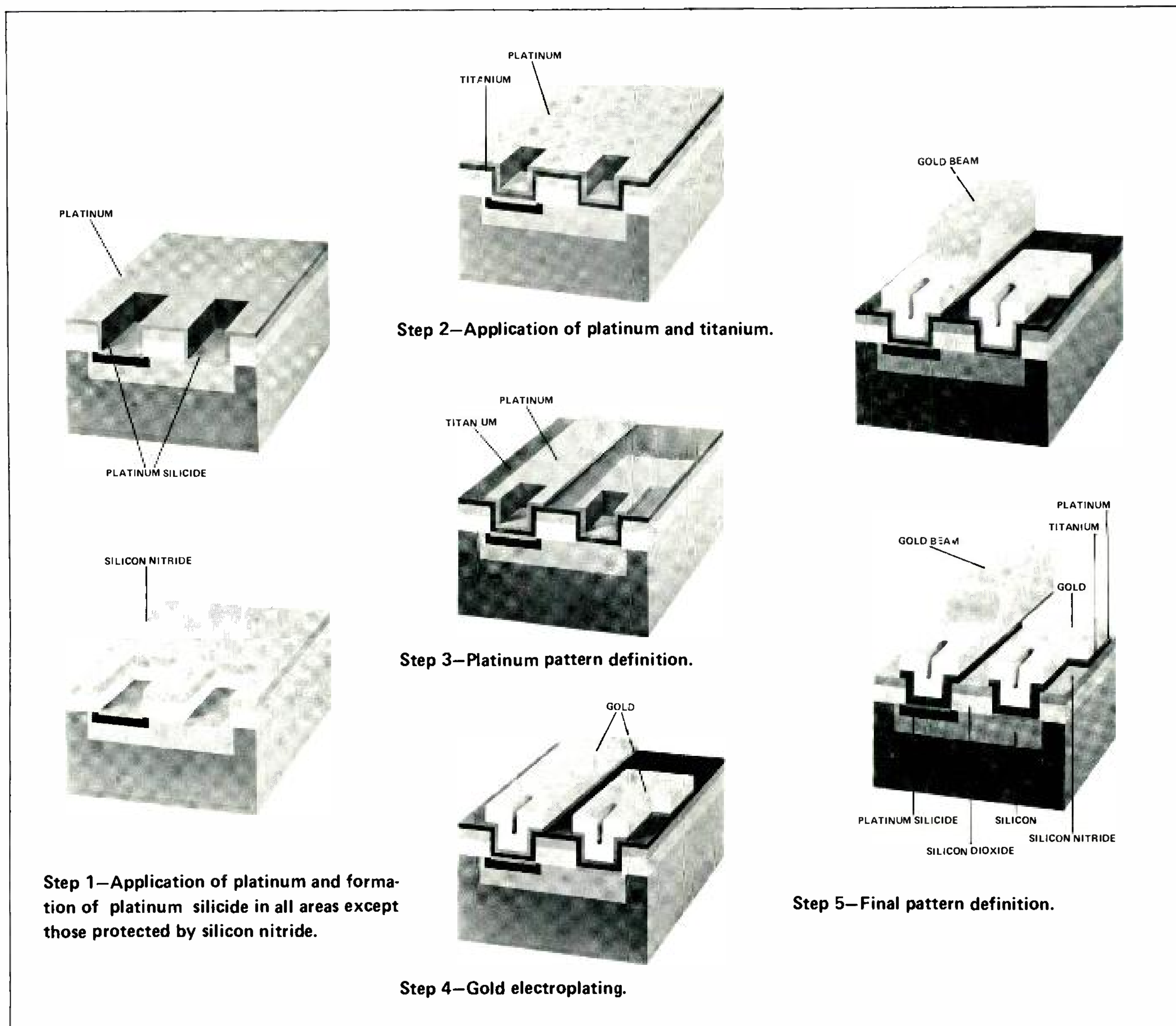


Step 1—Application of platinum and formation of platinum silicide in all areas except those protected by silicon nitride.

Step 2—Application of platinum and titanium.

Step 3—Platinum pattern definition.

Step 4—Gold electroplating.

Step 5—Final pattern definition.

Fig. 1—Process steps in forming contacts and interconnections.

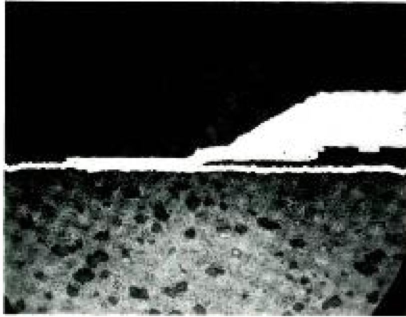


Fig. 2—Cross-section of beam-lead device bonded to thin-film metallization.

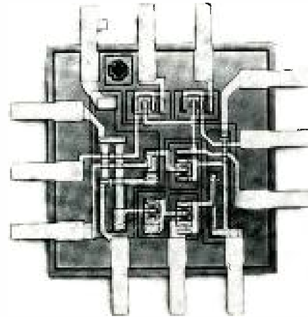


Fig. 3—Beam-lead device with gold connecting beams.

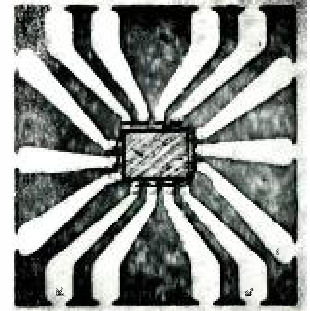


Fig. 4—Beam-lead device bonded to foil.

circuit boards by highly automated, complex, and volume-oriented handling equipment. Various packaging methods have been developed to make beam-lead devices compatible with that equipment:

Bonding the beam-lead device directly to an etched or stamped lead-frame. Conventional molding practice for plastic encapsulation in dual in-line package format then follows.

Bonding the beam-lead device to a miniature etched or electroformed foil as in Fig. 4; the foil conforms to the device beams at its inner dimensions and acts as a space transformer to match the device to the coarser dimensions of a standard lead frame. This miniature spider-like foil may be self-supporting or, in special cases, may be affixed to a plastic film such as polyimide to support the foil during assembly.

Bonding the chip to a ceramic substrate with appropriate metallization and a brazed lead frame, as in Fig. 5. Mechanical protection is provided by a lid—there being no need for hermeticity.

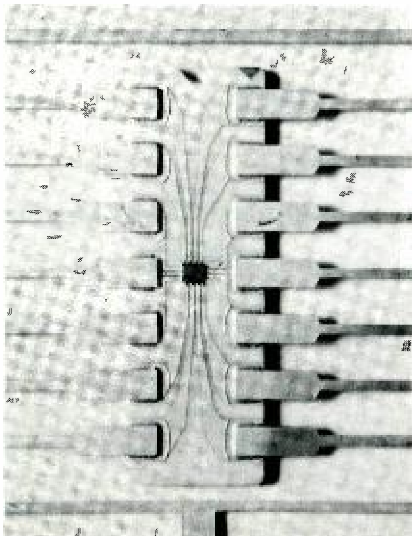


Fig. 5—Beam-lead chip bonded to substrate with brazed lead-frame.

The ceramic can be conventionally pressed and fired, or it can be fabricated by laminations of tape ceramic layers with intervening printed refractory metallization networks. This type of ceramic assembly is identical with the plastic package and is readily handled by the same assembly facility as that for plastic IC packages.

Hybrid array assembly

A logical extension of the single-chip package is to incorporate beam-lead chips in hybrid arrays. Various considerations prevail:

Small-scale arrays—The dual-in-line configurations lend themselves to use of several beam-lead chips bonded to a ceramic substrate with a lead frame. Mechanical protection is provided by a non-hermetic cap or lid.

Large/medium-scale arrays—The application of many chips to a substrate with intricate metallization may require a unique approach because the value of the assembled devices can outweigh the intrinsic value of the metallized substrate. Additionally, because the requirement for computer- and military-grade reliability of the finished assembly is a principal concern, large-scale arrays are usually made by bonding beam-lead devices directly to the metallized ceramic. As an alternative to direct chip bondings, a variant of the previously described etched foil is feasible. The device is thermocompression-bonded to the foil, as in Fig. 6, and encapsulated with a plastic resin to protect the chip and maintain the regular configuration of the fragile extended leads. The leads may be radial, as shown in Fig. 7, or in-line. This package can be accommodated in tape or magazine/carrier format and is readily soldered to thick-film metallizations by conventional passage through an infrared- or resistance-heated furnace. This technique also relieves the beam-lead-chip user of the need to obtain the fine-line thick-film metallization to mate with the beams etending from the chip.

It is apparent, in view of the foregoing, that device usage may be of four general types:

Chips,
Dual in-line plastic packages,
Plastic encapsulated radial arrays,
Multichip hybrid arrays.

This list can be augmented, for custom requirements, by assemblies with beam-lead IC chips bonded simply, or in multiple arrays, to brazed-lead-frame dual in-line ceramic substrates. Brazed-pin plug-in ceramic packages are also available. The substrate assemblies may be provided with lids for mechanical protection of the chips and metallization networks.

Systems handling concept

Beam-lead devices are separated from their wafer by backgrinding and etching to expose the device beams, while the wafer is firmly affixed to an infrared-transparent disc. Following electrical probing, the chips are bonded to the substrate metallization, lead-frame, or radial array. Direction to selected chips comes from test-computer memory storage, which maintains precise characterizations of acceptable chips. Because it is not feasible to test-probe an intricate integrated circuit fully while it is in the interdigitated wafer array, there is an intermediate test

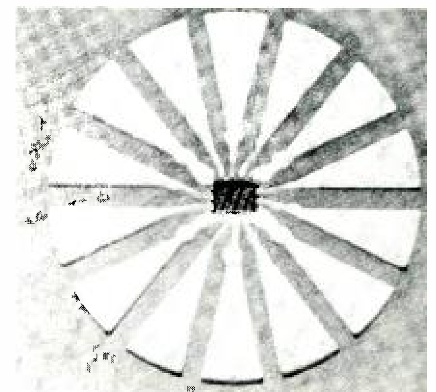


Fig 6—Beam-lead chip bonded to radial foil.

station during chip transport. The third step of the transfer-test-store-bond sequence depends upon the use of the chip. If electrically categorized chips are to be stored for on-site bonding, or for shipment to other locations, they may be deposited in close-tolerance arrays by means of precise stepping-motor-controlled tables for insertion into the bonding-machine sequence. They can also be bonded to the substrate without intermediate storage following test characterization.

Equipment of considerable sophistication has been in use for the handling, testing, and application of conventional chips; extremely high chip-handling rates have been maintained in production. Only machine modifications were needed to adapt this equipment to handle beam-lead devices in commercial quantities.

Feeding at high rates does require accurate alignment of the substrate with respect to the heated bonding tool. The precisely-located chips are picked up by a heated hollow vacuum tool. Precision alignment of the carrier permits rapid pickup of the chips, with minimal operator participation, and makes feasible the rapid and accurate alignment of chips with the bonding pads on the substrate. A feeding mechanism capable of high-rate presentation of accurately aligned heated substrates to the bonding tool is attached to the mechanism.

Bonding

Bonding of the gold beam to the metal pad on the substrate is performed at temperatures near 300°C; tool pressures are adjusted to deform each beam uniformly. Upon satisfactory alignment of chip and pad, the tool is actuated. The heated tool revolves around its axis at a slight angle so that each beam is deformed against each pad sequentially. This mode of bonding is generally called "wobble-head" bonding, characterizing the motion of the bonding tool (Fig. 8).

Alternately, a technique for compliant bonding is commercially available. As in Fig. 9, an aluminum or plastic foil is interposed between the bonding tool and the beams. The chip is aligned with a high degree of accuracy over the foil so that the body of the chip is over a foil opening, while the foil itself bears directly against the chip beams. The heated tool compresses the foil (with no wobble action of the tool). The foil deformation around the beams restrains them from excessive lateral movement and, because of certain hydraulic attributes of the foil, the beam-lead device is strongly bonded to the pad.

Bonds achieved by each technique are shown in the comparison photograph, Fig. 10. Where excess deformation of extremely close-spaced beams may cause potential electrical shorting, compliant bonding is preferred. Other than for this consideration, there is little to distinguish between the two techniques. Both are readily adaptable to high-rate production bonding with a minimum of operator control, and each may be easily systematized to accept chips in regular arrays which have been fully characterized.

Metallization

There are three general types of metallization that are bonded to a substrate. These are generally characterized as thick, thin, and refractory metallizations. They are distinguished from one another by thickness and method of application.

Thick films

Application of thick films depends upon the complexity of the circuit to be fabricated. In the simplest form, a ceramic-metallic "ink" is screened onto a prefired ceramic. High-temperature firing of this cermet ink provides adherence to the substrate and also a surface with metallic characteristics to which the gold beams can be bonded. The state of the art in screen-printing thick-film inks is such that lines 0.005 in. wide on 0.010-in. cen-

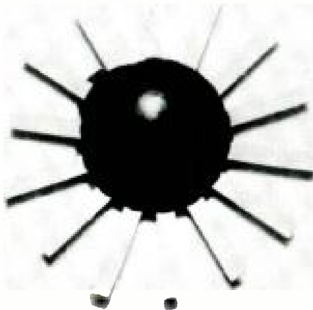


Fig. 7—Plastic-encapsulated radial-foil array.

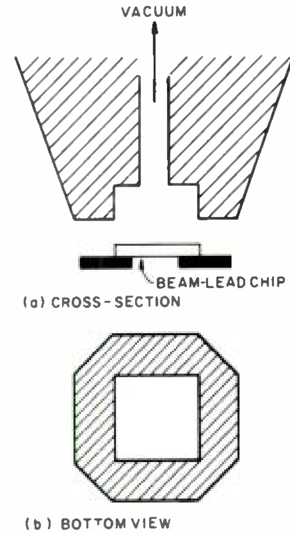


Fig. 8—Wobble-head bonding tool.

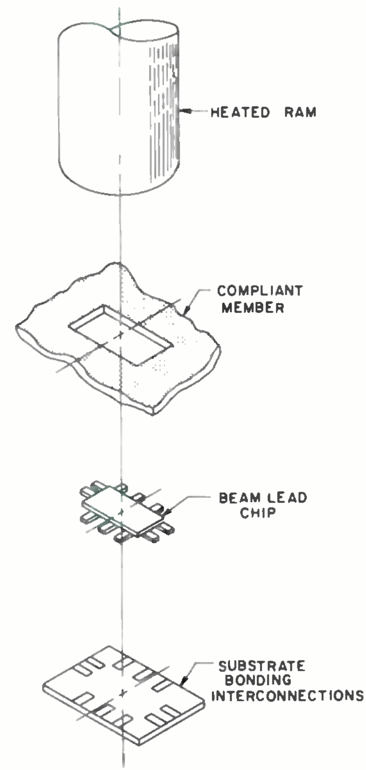


Fig. 9—Compliant bonding.

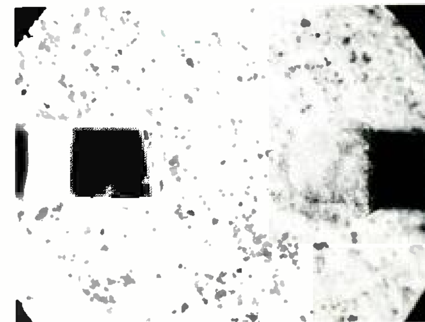


Fig. 10—Compliant bond (on left) and wobble-head bond.

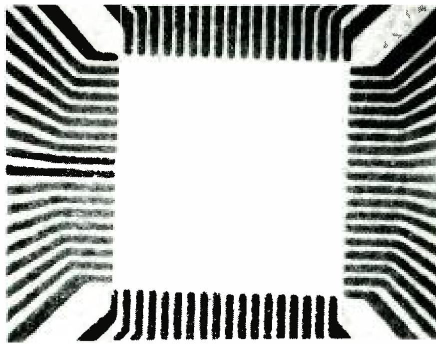


Fig. 11—Appearance of refractory-metal pattern prior to gold plating.

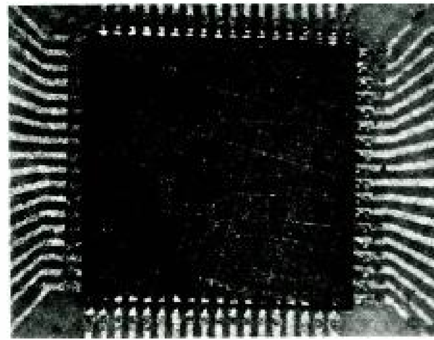


Fig. 12—Seventy-two-beam chip bonded to gold-plated refractory-metal pattern.

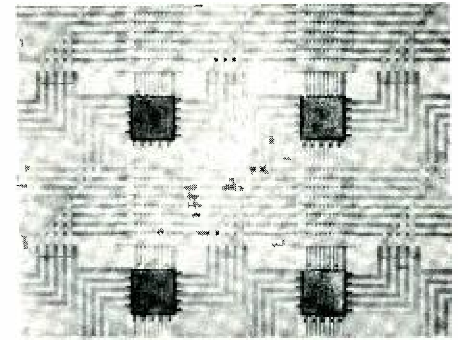


Fig. 13—Bonded chips with air-isolated beam crossovers and conductors crossing under elevated chips.

ters are considered routine practice. To achieve this line definition, however, the flow qualities of the ink are extremely critical. The characteristics of the ink must be such that the ink will readily flow through a 325-mesh screen, when squeeze pressure is applied, without clogging the screen. Further, there should be no additional flow of the ink, after it has been deposited on the substrate, during the drying and firing cycles.

To maintain quality of the beam-lead bonds to the thick-film inks, it is essential that the printed lines have a uniformly rectangular cross-section to provide flat surfaces for the beam bond. Thickness of the fired film may vary between 0.0005 in. and 0.001 in., and minimization of edge-chamferring is desirable. Guide rules pertaining to thick-film patterns for bonding may be summarized as follows:

All thick-film deposits, components, and other objects must remain completely clear of the area surrounding the chip to allow room for the bonding tool.
Printed conductor leads to all beams must be on the same plane.
Individual conductor fingers should be used for each beam lead.
All available beams should be bonded to a conductor finger whether electrically required or not.

Extensive investigation of the parameters of temperature and presure indicate that reliable beam-lead bonding to a variety of conductive thick-film compositions can be achieved. The material has to be carefully selected for its metallizing characteristics, and the bonding conditions are specific for each type of ink.

Under the conditions shown in Table I, beam-lead bonds with over 99% beam breaks (less than 1% beam lifts) have been obtained. These results indicate that the bonding to silver and gold is less critical than the bonding to such alloys as *Au-Pt, Pd-Au* or *Pd-Ag*.

Solder-coated conductors have also given good bonding results and are readily repairable; uniformity and thickness do not appear to be critical. The heat required to make such a bond is localized at the bonding tool and, therefore, does not disturb other soldered areas. When circuitry is assembled having standard add-on components bonded by solder, the ability to bond beam-leads onto solder is a necessity. It offers:

Fewer processing steps (e.g., solder stop-offs);
Fewer screen-printing artworks;
Relaxed design geometries;
Reduced overall fabrication costs.

Table I—Bonding conditions for thick-film conductors.

Thick-film conductor	*Substrate holder temp. (°C)*	*Bonding tool temp. (°C)*	*Bonding weight (g)*
Silver-4400 Cermalloy	300-330	225-300	280
Gold-8380 DuPont	300-360	225-300	360-520
Gold-Platinum 8553 DuPont	340	325	520
Palladium-Gold 8227 DuPont	340	325	520
Palladium-Silver 9623 ESL	360	325	520

Refractory-metal patterns

A modified form of thick-film pattern application is used for finer conductor delineation than is possible with conventional frit-based thick-film inks. This process involves the screening of a fine micron-sized particle suspension of molybdenum or molybdenum-manganese powders directly to the ceramic surface and the subsequent firing in a reducing atmosphere at about 1600°C. Application may be to a previously unfired ceramic structure so that both metal and ceramic are fired simultaneously, or alternatively, to a previously high-temperature-cured ceramic composition. With this technology, it is possible routinely to attain line-widths of 0.004 in. and line spacings of 0.002 in. Gold is electroplated over the pattern to allow bonding to the pads shown in Fig. 11.

This technology has been applied, for example, to make a plug-in package for a 0.120x0.120-in. beam-lead chip with 72 beams. The package is 1.225 in. square, with a maximum package thickness of 0.125 in. not including leads. Leads protrude from the bottom surface of the package, two rows on each side on a 0.100-in. grid, to facilitate attachment to a socket or for direct insertion into circuit boards.

During assembly of the package, using unfired ceramic tapes, the following advantages have been observed.

The ceramic cards upon which the metallization patterns are screened are pliable, ensuring perfect screen-to-ceramic contact for high metallization yields and sharp pattern definition.
The metallizing screens are expanded approximately 17% to allow for the dimensional shrinkage during firing. This larger size is a definite advantage when fine pattern detail is required.
The refractory metal pattern has exceptionally good electrical conductivity because of high metal density. The density is developed by an ink formulation which shrinks with the ceramic body during firing and by sintering the metal ink particles at a very high temperature.

The 72 Kovar pins are brazed into blind holes on the bottom ceramic with silver-copper eutectic BT solder at 850°C in a reducing atmosphere. Finally, gold is plated over nickel to a thickness of approximately 100 μin. to provide corrosion resistance

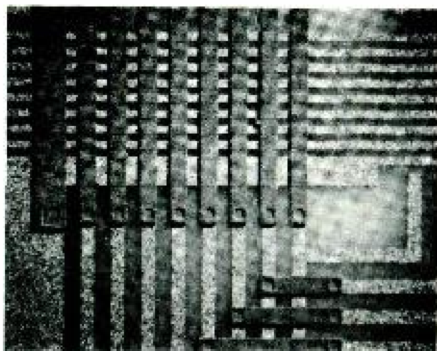


Fig. 14—500X magnification of air-isolated beam crossovers.

and beam bondability. Fig. 12 shows the appearance of the substrate following chip-bonding.

Thin films

The deposition of thin metal film (1000Å to 40,000Å thick) on the ceramic substrate is performed by evaporation from a filament, by an electron beam, or by sputtering. In general, an adhering layer of approximately 1,500Å of titanium is deposited over the entire surface, followed by an intervening layer of palladium to provide an integral barrier of approximately 1500Å between the titanium and the thicker, superimposed gold layer. The gold may be vapor-plated to its required thickness, between 30,000Å and 40,000Å, or it may be partly vapor-plated and subsequently electroplated to build up to the thickness required. Delineation of the circuit pattern is performed conventionally by photolithographic techniques, and extremely fine patterning is obtained.

Multichip packages of varing complexity can be constructed with thin-film technology. By employing air-insulated beam crossovers, multilevel wiring can be used to meet the requirements of many multichip arrays. Additionally, by taking advantage of device-elevation during bonding, the multilevel wiring capability can be further enhanced. Fig. 13 illustrates air-isolated beam crossovers and bonded beam-lead chips.

Inspection of Fig. 2 reveals the structure of a bonded chip in which a thin-film conductor approximately 50,000Å thick crosses under the raised chip. A highly magnified view of the structure of beam crossovers is shown in Fig. 14.

Quality control

An outstanding feature of beam-lead chip bonds is that they can be inspect visually. The primary concern for bond-to-pad alignment is readily satisfied by visual inspection to easily specified tolerances. The deformation of the beam, which is the essential indicator of the bond quality, is also visible for inspection.

Process control of the bonding operation is provided by destructive testing of chips and bonds on a periodic basis. A simple test on the chips is to bend each beam from a horizontal to a vertical position—through 90° —to indicate beam ductility. Fracture of the beam or separation of the lead from the chip is cause for rejection.

An additional measure of beam ductility, and of consequent ability of the beam to deform and bond to the underlying pad, is offered by a simple microhardness measurement, either on a Vickers or Tukon scale. Typical acceptable values are indicated in Table II. Another test for the integrity of the gold beam is provided in elementary fashion by simply heating the chip in air to 300°C. Discoloration of the gold beams is clear evidence of contamination of the gold electroplating bath.

Normal process-control procedures call for the setup of bonding-machine conditions for inspection purposes to determine uniformity of beam deformation. A test procedure to ensure

Table II—Beam-lead microhardness.

Lot No.	*Sample No.*	*Hardness on diamond pyramid scale**
A (*Aver.* 67)	1	68
		82
		76
	2	67
		65
		62
		62
	3	64
		54
B (*Aver.* 45)	1	52
		50
		32
	2	49
		47
		38
	3	49
		52
		38
C (*Aver.* 51)	1	61
		55
		55
	2	61
		49
		49
		49
	3	45
		45
		Measurements taken with 136° diamond indenter

*Microhardness extension of Vickers Scale.

satisfactory results entails, first, the bonding of chips directly over a hole in the substrate. A test fixture holds the substrate, and a small-diameter rod is then inserted into the hole and brought to bear upon the underside of the bonded silicon chip. By means of a dynamometer, the load required to cause failure is determined. A certain minimum value of grams/beam for nominally-12-μm-thick beams indicates acceptability. Unacceptable are the separation of the anchor pad from the chip or lifting of the deformed beam from the metallization. Acceptable failures at adequate strengths are the breaking of the beam at the necked portion, immediately adjacent to the bond, and the destruction of the silicon chip at stresses above the minimum acceptable load.

Repair

Particularly for complex multichip hybrid assemblies, a procedure for chip removal and replacement that does not affect adversely the reliability of the assembly is essential. For the types of metallized substrates, foils, and frames mentioned previously, the procedure to be described is well adapted. When electrical testing of a finished circuit has disclosed the location of a defective chip, removal of the offender is performed simply by scraping it from the substrate. A wedge-shaped tool is brought against the chip by a micromanipulator, and the chip and the major portions of the beams are scraped off. Directly after this operation, replacement of the offending chip by another fully-tested one is feasible by conventional bond procedures. Inspection criteria applicable to new bonds apply as well to replacement chips.

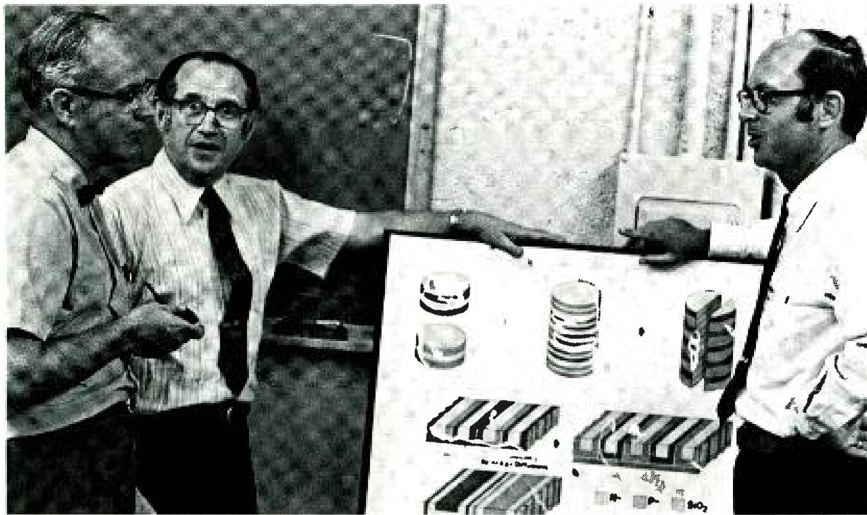
Conclusion

The superior electrical and physical characteristics of beam-lead devices offer the designer more package options in balancing the trade-offs of reliability compactness, hermeticity, and repairability. These considerations are, in turn, related to economic factors in circuit assembly where the advantages of the beam-lead technology make feasible advances in device complexity, production-line automation, and product design heretofore impossible with the outmoded chip-attach and flying-wire bond techniques.

Development of low- and medium-frequency power transistors

J. Gaylord | J. Olmstead | Dr. A. Blicher

Power transistors are continually improving in quality and power-handling capacity; it is now possible to design a transistor that will handle close to one kilowatt. Phenomena which are unimportant in the design of small-signal transistors ultimately limit the performance of such high-power devices, and make trade-offs in certain important design parameters inevitable. This paper describes some of these trade-offs in detail, and indicates power-device developments that may be possible in the near future.



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In the past few years, the successes of small-signal integrated-circuit technology have diverted the attention of many engineers from the advances in the field of semiconductor power devices. This temporary lack of glamour should not be construed, however, as an indication that the power field has become stagnant and devoid of technological challenges. Power technology continues its march towards higher power outputs, improved efficiencies and frequency responses, and integration in the form of hybridized circuit functions or monolithic circuits.

Limiting phenomena in power transistors

Power transistors have many features in common with small-signal transistors, but what distinguishes power transistors is their ability to handle currents up to a few hundred amperes, voltages up to a few thousand volts, large power dissipations, and drastic current and voltage surges.

Several phenomena which are of minor significance in small-signal bipolar transistors become important as currents and voltages are increased, and ultimately they limit performance. These phenomena include: base widening, emitter debiasing, second

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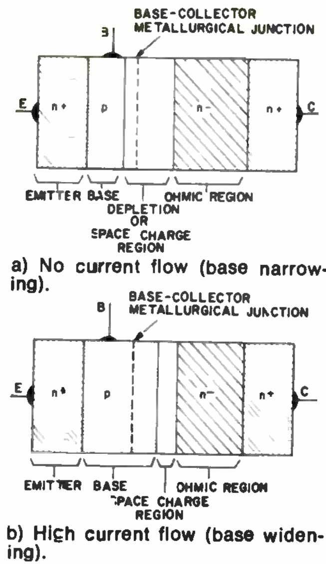
breakdown, high-voltage surface effects, and thermal fatigue.

Base widening

Base widening[1] (Fig. 1) occurs in all bipolar transistors having a lightly doped collector region. It is caused by the mobile carrier flow within the unit, which modifies the electric field distribution so that the effective positions of the base-collector junction and the collector depletion region are different from their positions when there is no current flow.

Consider an n⁺-p-n-n⁺ transistor with no current flowing and a fixed base-collector reverse bias. Under these conditions, the depletion region penetrates the base and the lightly doped collector body. Equal fixed total donor and acceptor charges are uncovered on both sides of the metallurgical junction. Initiating current flow (mobile charge) has three effects. First, the mobile charge carriers in the base are of the same sign as the uncovered fixed charge; the depletion region in the base shrinks and the base widens. Second, the mobile carriers in the collector are of the opposite sign and thus subtract from the fixed charge. This condition tends to cause the depletion region in the collector to expand to uncover the requisite charge. Third, the current flow in the transistor introduces an ohmic voltage drop in the lightly doped n^- part of the collector body. Because this voltage drop subtracts from the applied collector-to-base potential, less voltage is available for the depletion region, and the base becomes wider again.

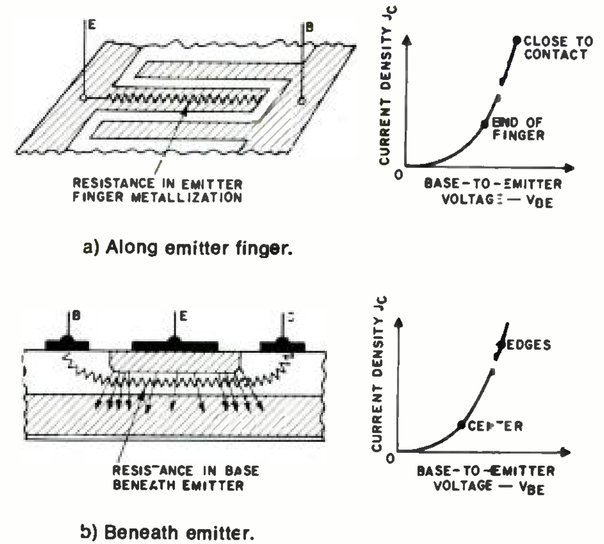
At high current densities and low collector voltages, the transistor-base widens beyond the metallurgical base-collector junction and approaches the n^+ collector region. In this condition, the current gain and gain-bandwidth (f_T) decrease and the device approaches the performance of a simple three-layer (n^+-p-n^+) transistor. Base widening with its resultant decreases in current gain introduces a quasi-saturation region into the common emitter static characteristics (Fig. 2). Operation in this region significantly increases stored charge, rise, and fall times (τ_S, τ_R, τ_F). Fig. 3 shows the influence of base widening[2] on the gain bandwidth f_T.



a) No current flow (base narrowing).

b) High current flow (base widening).

Fig. 1—Base width modulation in power transistors.



a) Along emitter finger.

b) Beneath emitter.

Fig. 4—Resistive debiasing phenomena.

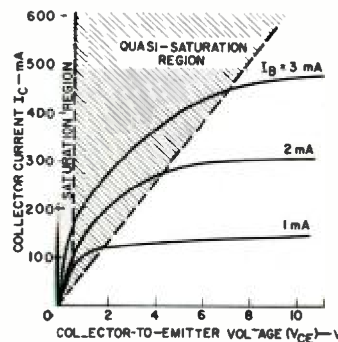


Fig. 2—Quasi-saturation in power transistors (n⁺-p-n-n⁺ doping profile).

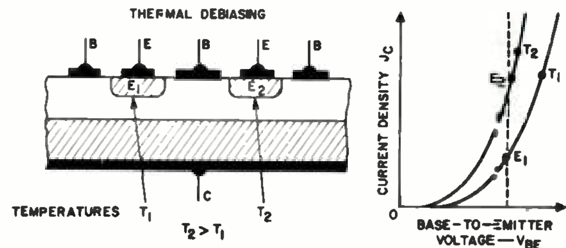


Fig. 5—Thermal debiasing.

Debiasing

There are two debiasing phenomena of significance in bipolar power transistors. The first, resistive debiasing (Fig. 4), is due to voltage drops along resistance in emitter and base fingers and in the base region beneath the emitter. These voltage drops result in heavier injection from the edges of the emitter and in emitter regions closest to the emitter contact.

Resistive debiasing beneath the emitter due to voltage drop in the base resistance can be minimized by making the emitter fingers narrow, the base wide, and the base resistivity beneath the emitter as low as possible. Metallizing the emitters so that the contact is locallized toward the finger center inserts a lateral emitter voltage drop which tends to offset the base resistance drop.

Thermal debiasing (Fig. 5), the second debiasing phenomenon, is a consequence of unintentional temperature differences between various locations of the emitter. Forward current from the emitter is strongly dependent on the temperature of the emitter-base junction as illustrated in Fig. 5. For example, a temperature of 12°C between two regions of the emitter-base junction results in 3.8 times more current from the hotter region. Because unequal injection results in unequal dissipation, the hot region tends to become hotter and injects more.

Thermal debiasing can be minimized in two ways. First, the emitter can be separated into a number of discrete emitters and a ballast resistance placed

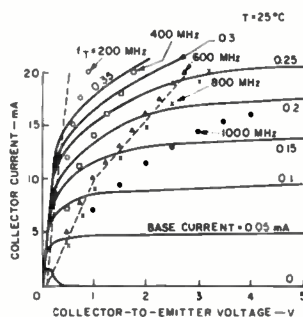


Fig. 3—Effect of base widening on gain-bandwidth product f_T.

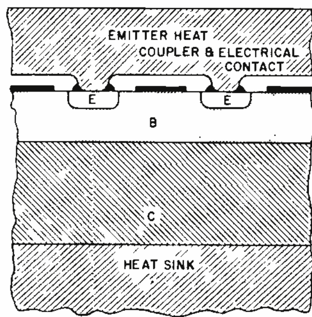


Fig. 6—Isothermal emitter technique.

in series with each discrete emitter. These resistors insert a voltage drop in each emitter proportional to the current being passed through the emitter, thus inserting current feedback and equalizing the currents between emitters. A second method utilizes a low thermal-resistance coupler between emitters. The emitters are made isothermal and, therefore inject equally. This technique is illustrated in Fig. 6.

Second breakdown

A bipolar transistor operated at high power densities is subject to a failure mode termed "second breakdown" in which the emitter-collector voltage suddenly drops, usually 10 to 25 V. Unless the power is rapidly removed, the transistor is destroyed or materially degraded by overheating. Second breakdown (S/b) is a thermal hot spot formation phenomenon within the transistor pellet. It has two phases of development. First is the constriction phase where, because of thermal regeneration, the current tends to concentrate in a small area. The second phase is the destruction phase. In this second phase, local temperatures and temperature gradients increase until they cause permanent device damage.

The constriction or regeneration phase of S/b may be initiated in any number of ways. One section of the emitter-base junction need only be higher in temperature than the others. Such a hot spot might be caused by, resistive debiasing, divergent heat flow to the device heat sink, an inhomogeneity in the thermal path, or other irregularities or imperfections within the device. Once a slightly hotter emitter-base region is present, positive thermal feedback begins: the hot region injects more and therefore gets hotter. If the available power is limited or the effective thermal resistance of the hot spot is sufficiently low, the peak temperature remains below a critical temperature and stable operation continues. When the peak temperature reaches a value such that local base-collector leakage currents reach base current magnitude, the device regenerates into second breakdown often very rapidly.

Second breakdown occurs when the device operates with a forward biased emitter-base junction Fig. 7 and during the application of reverse bias. In the forward-biased form of second breakdown, the current $I_{S/b}$ above which the device switches into S/b is specified as part of the "safe-operating area" rating system developed by RCA for power transistors. Emitter and base resistive ballasting effectively increase forward-biased $I_{S/b}$ of a device. Emitter ballasting equalizes currents by inserting in each emitter region a voltage drop proportional to the current passing through the junction. Base ballasting inserts a voltage drop proportional to base current in the various base regions thus equalizing drive conditions within the device and maintaining uniformity. Thermal coupling between emitter regions may also be used to improve the forward biased $I_{S/b}$ performance of a transistor. This previously illustrated design approach tends to hold all regions of the emitter-base junction at the same temperature and same forward bias, thus maintaining uniform current flow.

Second breakdown is also observed when a transistor operating with an inductive load is turned-off, (Fig. 8). When the emitter-base junction is reverse biased, the edges of the emitters are quickly turned-off by the voltage drop caused by the reverse flow of the base current through the base resistance under the emitter. Collector current tends to be rapidly reduced; however, the inductive load responds to the decrease in collector current by driving the collector-emitter voltage to a value at which breakdown can occur in the collector-base space charge region (BV_{CEX}). The multiplied current resulting from the breakdown is focused towards the emitter centers, keeping the centers on for a longer time. When all center sections of the emitters behave alike, the power is dissipated uniformly by all emitters. If, however, a hot spot exists or develops, the energy stored in the load inductance is dumped into this region. The central region of this "hogging" emitter rapidly rises in temperature, reaching a value where the hot spot sustains itself and second breakdown occurs. Emitter ballasting is not effective in protecting against reverse-biased second breakdown because the hogging portion of the emitter is fed internally from a current source, and this current source is insensitive to the relatively small differences in emitter potential. Ballasting against reverse-biased second breakdown is best done in the collector by the addition of a resistive layer which decreases the internal collector-emitter voltage in the affected region. The maximum energy that may be stored in the load inductance before second breakdown ($E_{S/b}$) is specified for most RCA power transistors intended for switching applications.

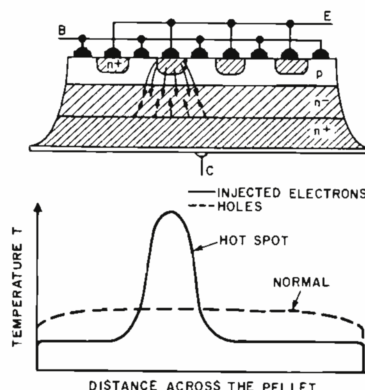


Fig. 7—Forward biased second breakdown.

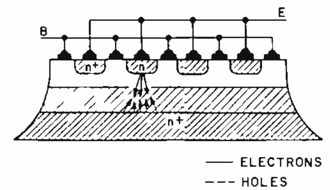


Fig. 8—Reverse biased second breakdown.

High-voltage surface effects

As the voltage ratings of a power transistor are increased, it becomes more difficult to achieve theoretical bulk breakdown values. Furthermore, both the breakdown voltage and junction leakage currents may vary under operating conditions. The problem is usually due to surface phenomena.

High-voltage transistors require large depletion widths in the base-collector junction. This requirement suggests that at least one side of the junction must be lightly doped. Fig. 9 shows what happens in a normal mesa-type

device. The external fringing electrical fields terminate on the silicon and modify the depletion regions at the surface. If these fringing fields are large and configured as shown, a local high field condition is established at the surface and premature breakdown occurs. High-intensity fringing fields exist well outside the junction and contribute to the movement of ions external or internal to the applied passivation layers, leading to instabilities.

The state-of-the-art "cures" for these problems are: junction contouring to reduce the magnitude and the shape of the fringing fields; empirical determination of the proper surface etch and the optimum organic encapsulant; or glassing of the junctions to contain the fringing fields. The latter two solutions do not usually yield breakdown voltages equal to the bulk values, but they do lessen the surface instability.

To achieve breakdown voltages approaching the bulk values it is necessary that the fringing field be properly shaped, and once properly shaped it must be kept in this condition. Field electrodes are being investigated to accomplish this objective.

Thermal fatigue

A power transistor is often used in applications where the power in the device is cycled; the transistor is heated and cooled many times. Because the transistor is constructed of materials that have different thermal expansion coefficients, stress is placed on the chip, the metallurgical bond, and the heat spreader. If the stress is severe enough and sufficient cycles are encountered, the device fails. Usually the chip separates from the heat spreader or one of the contact connections opens. The stress is proportional

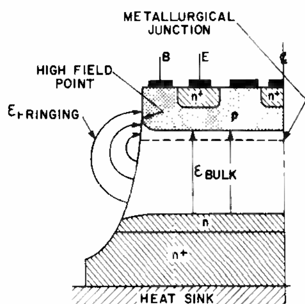


Fig. 9—Electric field distribution in high-voltage "mesa" n-p-n transistor.

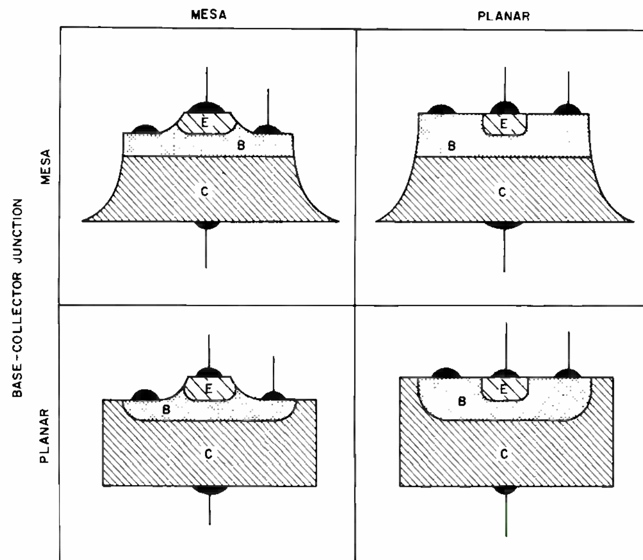


Fig. 10—Junction delineation techniques used in power transistors.

to the size of the pellet, the temperature variation, elasticity of the connecting members, and the differences in thermal expansion coefficients. Anything which concentrates the stress, such as voids in the mounting system, aggravates the condition.

The rate of degradation of a metallurgical bond under stressed conditions is also proportional to the average and peak temperature excursions of the bond. The failure-rate dependency of thermal fatigue and other phenomena can be as much as double for every 10°C increase in average and peak temperature. The most economical way to buy reliability in power transistor application is, therefore, to reduce these temperatures by careful consideration of heat flow during equipment design.

Several techniques are used to improve thermal-fatigue capability within power transistors. One method is to mount the chip on a metal such as molybdenum, whose thermal expansion coefficient is similar to silicon, and to braze this metal to the package. In this way stresses are evenly distributed, as in a graded glass seal. Another method, applicable on units using the lead solder mounting technique, uses a controlled solder process in which the thickness and composition of the lead solder are carefully controlled at all times.

Structures and geometries

Many design variations are used to reduce the limitations imposed by base widening, emitter debiasing, second breakdown, high voltage surface effects and thermal fatigue. Each design is replete with compromises, both subtle and obvious.

A power transistor may have its base-collector and emitter-base junctions delineated by two methods (Fig. 10). First, selective etching may be used to create a multi-level "mesa" outline, where the junctions terminate at the edge of the mesa. Second, masked impurity diffusion may be used to convert selected areas to "planar" type junctions. A power transistor may be produced by using one or both of these techniques for the two junctions. The choice between the two is described below.

Planar junctions can be produced with much finer dimensions than mesa junctions while the surface oxide remains covered and ostensibly flat. These characteristics are necessary in high frequency and multi-element types. Mesa junctions are dimensionally inferior but produce junctions with higher breakdown voltages: absense of the radius effect eliminates local internal high electric-field regions. For voltages greater than approximately 300 V, the mesa junction is the most economical fabrication technique. Mesa type emitter-base junctions also eliminate edge injection and thus result in better high-current current gain.

A power transistors doping profile may consist of three to six layers obtained by impurity diffusion and/or epitaxial

Table I—Qualitative relationships between physical and electrical parameters.

Physical Parameter		Electrical Parameter									
		$f_{(T)}$*	τ_d, τ_R τ_f, τ_S	$V_{CE(MAX)}$ (LV_{CEO})	$V_{CE(SAT)}$	V_{BE}	h_{FE} (peak)	$I_{C(MAX)}$ $(h_{FE}=10)$	$I_{S/B}$	$E_{S/B}$	Radiation Hardness
Base width (W_B)	↑	↓	↑	↑	↑	↑	↓	↓	↑	↑	↓
Base resistivity (ρ_B)	↑	—	↑	—	↓	↑	↑	↓	↓	↓	↓
Collector width (W_C) (n^- region)	↑	↓	↑	↑	↑	↑	—	↓	—	↑	↓
Collector resistivity (ρ_C) (n^- region)	↑	↓	↑	↑	↑	↑	—	↓	↓	↓	↓
Emitter width (X_E) (finger)	↑	↓	↑	—	—	↑	—	↓	↓	↓	↓
Emitter ballast (R_E) (resistive)	↑	↑	↓	—	↑	↑	—	↑	↑	—	—
Collector ballast (R_C) (resistive)	↑	↓	↑	—	↑	—	—	↓	—	↑	—

Notes:
*$f_{(T)}$ measured at high currents and low voltages (power corner, worst case point).

techniques. The basic three-layer profile shown in Fig. 11 is preferred because of its simplicity, but it necessitates a compromise between voltage and response-time capability. This compromise is required because the collector depletion region forms mostly in the transistor base; consequently the base must be wide for higher voltage capability. The addition of a lightly doped collector layer (Fig. 11b) allows the collector depletion region to expand into the collector rather than into the base, and the base can be kept thin. In this way the voltage capability is increased without lowering the device response time if base widening is not encountered. The additional layers shown in Fig. 11c and 11d control base widening, improve voltage breakdown through control of the fringing field which surrounds the device, or provide ballasting against second breakdown.

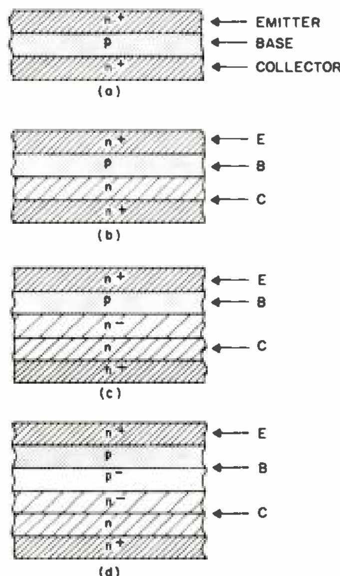


Fig. 11—Basic power transistor doping profile (n-p-n used for illustration): (a) n^+-p-n^+ (b) n^+-p-n-n^+, (c) n^+-p-n^--n-n^+, (d) n^+-p-p^--n^--n-n^+.

A power transistor may be considered a composite of many unit transistors in parallel. The emitter-base geometry is designed so that each unit transistor is operating efficiently and that, in parallel, all unit transistors operate together, sharing the load current. Fig. 12 shows some of the emitter-base geometries used. In most cases, the emitter-base geometry is complex to maximize the emitter periphery-to-area ratio (E_P/E_A) and often consists of a number of separate emitters to minimize resistive and thermal debiasing effects.

Power transistors are assembled and packaged in many different ways, and packaging power transistors present unique engineering challenges. Designers must achieve efficient heat removal, freedom from material fatigue failure under cycling operation, and high-current, low-resistance contacts. In many cases, these considerations dictate the pellet design, overriding other considerations.

Interrelation of parameters and design trade-offs

Good engineering is the art of profitably trading off individual parameters without compromising total system performance, and power transistor design makes good use of this art.

Table I shows qualitatively the relationships between the major physical device design parameters and the major electrical parameters. Table II shows how the parameters of second breakdown, voltage, radiation resistance, and cost relate to the more conventional device electrical parameters. An examination of these tables indicates that a large number of compromises can be made in the design of the circuit-transistor system to optimize its cost effectiveness. Some of the more

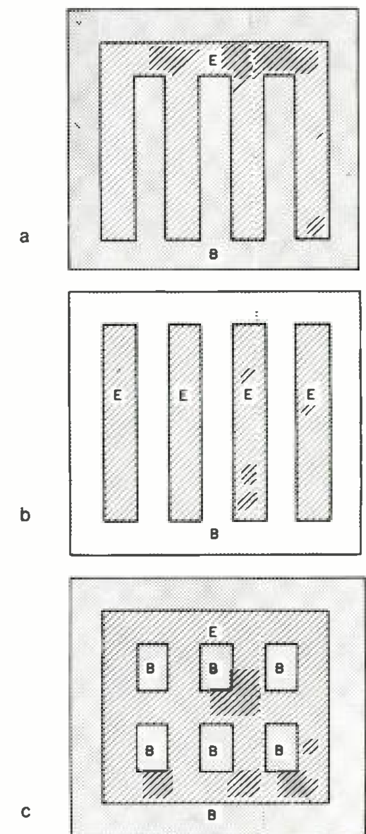


Fig. 12—Basic power transistor emitter geometries: (a) interdigitated, (b) multiple discrete (overlay), and (c) perforated emitter.

Table II—Qualitative relationships between some important parameters.

Specific Electrical Parameters	Conventional Electrical Parameter					
	$f_{(t)}$*	τ_d, τ_R, τ_f, τ_S	$V_{CE(SAT)}$	h_{FE} (peak)	$I_{C(MAX)}$ $h_{FE}=10$	Cost
$I_{S/B}$ ↑	↓	↑	↑	↓	↑	↑
$E_{S/B}$ ↑	↓	↑	↑	↓	↓	↑
$V_{CE(MAX)}$ ↑	↓	↑	↑	—	↓	↑
Radiation resistance	↑	↓	↓	↓	↓	↑

Notes:
*$f_{(t)}$ measured at high currents and low voltages (power corner, worst case point).

Symbols for Tables I and II

f_t—current gain-bandwidth
τ_d—delay time
τ_R—rise time
τ_f—fall time
τ_S—storage time
$I_{S/B}$—forward second breakdown current
h_{FE}—DC current gain
V_{CE}—collector to emitter voltage
$V_{CE(sat)}$—collector to emitter saturation voltage
I_C—collector current
$E_{S/B}$—reverse second breakdown energy
↑ Increase
↓ Decrease

salient physical reasons behind the inter-relationships are described below.

The time responses of a power transistor are basically related to the transit time of a free carrier from the emitter to the collector and to the rate at which charge can be built up or decayed within the structure. Obviously, devices having short conduction spaces minimize the transit time; the base must be kept thin. Thin, low-resistivity collector material keeps the space charge region short and limits base widening. These factors also limit the amount of stored charge, thereby reducing switching times. Narrow, highly interdigitated ballasted emitters keep current flow and stored charge more uniform and allow faster charge removal from the base. All of the above factors contribute to a low saturation voltage in the transistor. A compromise in saturation voltage ($V_{CE(sat)}$) must be made, however, if lifetime reduction techniques, such as gold doping, are used during manufacture or if lifetime decreases because of radiation damage. High collector-emitter voltage must be traded against time response, because such devices depend on wide, high resistivity collector and base regions. Furthermore, because lifetime reduction techniques are not completely applicable, switching times are longer.

To achieve high-current capability the emitter must have a large area, be highly efficient, and inject uniformly. An emitter with many thin fingers meet these conditions and gives a high emitter periphery-to-area ratio. Emitter ballasting also helps. But base widening must be avoided because it limits the current density within a device for any reasonable current gain, and thin, low-resistivity collector material used to prevent base widening is inconsistent with high collector-emitter voltages.

High current gain necessitates high emitter efficiency, narrow base widths, and high minority carrier lifetime. High emitter efficiency requires a lighter doped base. Thin, high-resistivity base regions aggravate emitter debiasing effects; narrow, uniformly injecting emitters are desirable to maximize high-current current gain. Again, because base widening effects must be avoided, low-voltage devices have the advantage.

The ability of a transistor to withstand high transient energy dissipation (second breakdown) is enhanced by keeping the base wide and its resistivity low. This condition conflicts with time response and current gain objectives. A design for uniform injection using narrow emitter fingers and incorporating ballasted emitter sites counters thermal or electrical debiasing effects but tends to increase $V_{CE(sat)}$. Collector regions should be thick and the resistivity as low as possible without losing collector ballasting resistance. Multi-resistive layers in the collector are beneficial but add to the cost. In general, techniques used to assure high second breakdown capability slow time response, increase saturation voltage, and add to cost. For a given volt-ampere product, extremes in voltage or current aggravate the second breakdown problem. In some cases, input regulation and transient control to an entire system is economical because lower-cost power transistors can then be utilized.

Future design trends

It is now possible to design and fabricate transistors having power outputs close to one kilowatt. But there are many applications where considerably more power is required and where electron tubes are currently used. Such applications include induction and dielectric heating equipment (with power output of tens of kilowatts), high-power broadcast transmitters, and ultrasonic generators.

With improvement of the quality of available silicon crystal, the advent of improved passivated surfaces and structures capable of breakdown voltages above 2000 V, and with superior thermal management, transistors with powers on the order of 10 kw will be available before the end of this decade.

With improved pellet passivation, chips will be enclosed in plastic and in hybrid circuit modules with greater reliability than is now possible with discrete power transistors in expensive hermetic packages.

Because cost reduction is always a prime objective, power transistors will be integrated monolithically with dielectric isolation capable of withstanding high voltages. The integration techniques will no doubt make possible some properties that cannot be achieved today even in discrete devices. Thus entirely new markets will be created beyond the realm of today's reality.

Computer microelectronics resident facility

D. E. Kowallek

Computer Microelectronics (CME) reports to the Systems Development Division of Computer Systems of Palm Beach Gardens, Florida, but is located in Somerville, New Jersey for liaison with the Solid State Division. CME monitors semiconductor developments of potential application to computer equipment, and provides the Systems Development Division with semiconductor technological information as a basis for decision making.

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received the BSEE in 1960 from Case Institute of Technology and tre MSEE in 1967 from Purdue University. Mr. Kowallek joined the RCA specialized trainee program in 1960 and was assigned to Radio Victrola Engineering in Home Instruments. His responsibilities included the design of Audio, IF and RF Circuits, their integration into FM and AM receivers, and the development of associated computer aided design techniques. In 1968, Mr. Kowallek joined ceramic circuits in Consumer Electronics and was subsequently named leader, electrical engineering. There he was responsible for the development of ceramic circuit products for consumer electronic equipment and for the design of computer controlled test systems for the engineering and production activities of ceramic circuits. In 1970, Mr. Kowallek transferred to Systems Development Division as Manager of the Computer Microelectronics resident facility in Somerville. In this capacity, he is responsible for serving the Microelectronic need of Systems Development Division.

Computer Microelectronics (CME) was organized because a close tie-in of the Systems Development Division with the Solid State Division was needed. The CME resident group was therefore officially formed early in 1970, and subsequently, expanded to meet the increasing needs of Computer Systems activities. Presently it consists of three engineers, two technicians, one secretary and a manager. CME is located near the Solid State Technology Center which is the advanced development arm of the Solid State Division.

Charter

The concept of a resident group and how it should best interface with the divisions concerned (Fig. 1) is still evolving. The group is flexible and is acquiring a broad base of knowledge in semiconductor technology and computer applications. In accordance with its charter commitments the CME group is:

—Fostering the development and use of RCA IC devices by providing a custom circuit design capability utilizing up-to-date technology, procedures, and facilities available at Somerville,
—Providing a facility to work with the Solid State Technology Center in design projects and in the evaluation of advanced technologies potentially useful in computer applications,
—Providing the Systems Development Division with information on semiconductor technology and projected trends so that technical decisions can be made,
—Providing direct communication between the Systems Development Division and the Solid State Division at various levels but especially on an engineer-to-engineer basis, and
—Providing inputs from the Systems Development Division to guide the Solid State Division in formulating advanced development plans for future computer applications.

Implementation

Computer Microelectronics fulfills its charter either with direct cooperation or with aid from other activities within the Solid State Division. Al-

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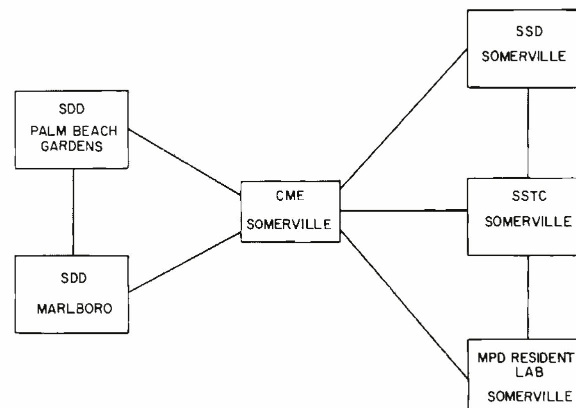


Fig. 1—CME interface relationship.

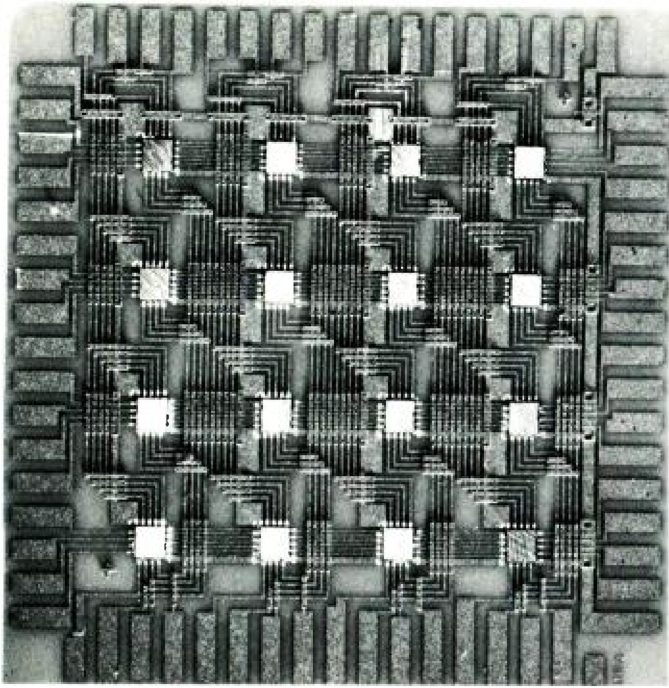


Fig. 2—Hybrid packaging concept.

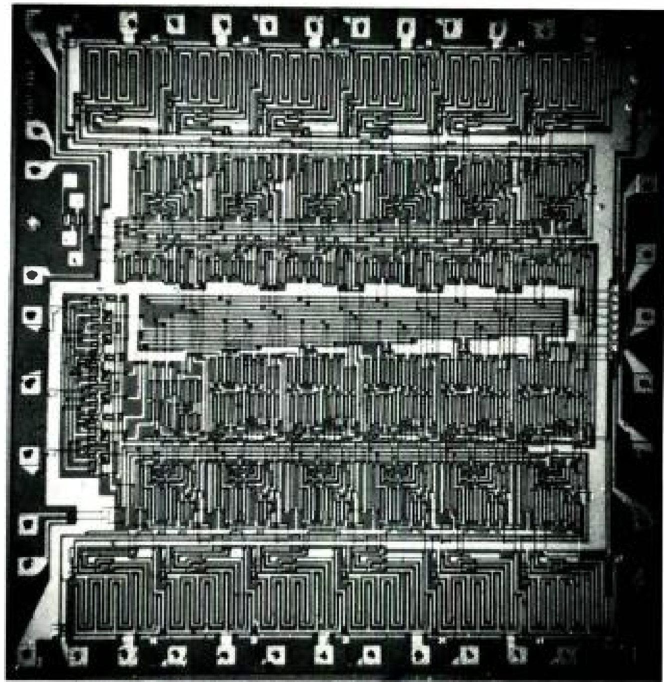


Fig. 3—PMOS character buffer chip.

though CME is closely tied to the Solid State Technology Center, projects have been carried on with other groups, including the COS/MOS and the Microelectronics Technology activities. In addition, information is gathered from many of the other Solid State Division elements at the Somerville location.

In carrying out its charter, CME concentrates on:

Custom circuit development. Design, simulation, layout, fabrication, packaging and testing for both MOS and bipolar integrated circuits.
Advanced technology projects. Cooperative studies with the Technology Center on circuit techniques and advanced development projects.
Studies involving IC design. Integrated circuit design techniques for both bipolar and MOS applications.
Studies involving IC simulation and analysis. Simulation and analysis programs to aid in circuit design and logical simulation.
Services to the Systems Development Division (SDD). Presentation of educational courses; distribution of technical materials, reports, and studies to SDD.

The following are examples of design projects, studies and services completed or in progress. For the most part, they were accomplished through close association with the Solid State Division and in particular with the Technology Center.

High speed bipolar circuit and package development

Requirements for advanced high speed low power circuits, and for new packaging techniques have dictated the need for a continuing program of cooperation between the Systems Development Division, the Technology Center, and CME. Basic new concepts for partitioning and implementing logic functions are being studied. A current program includes the development of bipolar chips using advanced semiconductor technology and a compatible new packaging scheme. One of the schemes under consideration is shown in Fig. 2. The program goal is to coordinate advanced technological developments to achieve performance improvements consistent with future computer packaging trends.

Design of MOS output buffers

Small MOS devices suitable for high density LSI are relatively high in impedance and therefore have limited current sinking capability. Driving a T^2L load or a T^3L load (2.5 mA at 0.4 V) requires relatively large output devices. This drive capability is somewhat more difficult to obtain in a PMOS than a COS/MOS circuit; therefore PMOS output buffering methods were studied.

In the study report, a number of circuit configurations were proposed to satisfy the requirements. For each configuration, figures of merit were tabulated for chip area, power, delay and input capacitance. The report was circulated to the SDD design centers to assist them in designing output buffers for future MOS circuits.

Design of MOS character buffers

Various technologies for MOS LSI are available, but the capabilities and limitations of each must be intensively studied. A relatively complex circuit suitable for MOS LSI was selected for comparing PMOS and COS/MOS technology.

The selected circuit is a dual six bit buffer register usable in communication terminals. The register circuit can accept two independent sets of serial or parallel data, and output from each register or transfer data from one register to the other. Each register is capable of independent serial transfer, and the length of one register is electrically programmable. The circuit is required to be input-compatible with T^2L and output-compatible with either T^2L or T^3L. Although traditionally MOS LSI circuits are relegated to slow speed applications, these circuits could be used at clock rates up to 2.5 mHz.

A photograph of the PMOS circuit layout (Fig. 3) shows the twelve large areas devoted to output buffering for

T^3L compatibility. The decode circuit for programming the register length can be seen along the left side. Also visible is the complexity of random logic interconnections required for bussing the control signals and power.

The important performance parameters obtained on the PMOS circuit are compared with specifications in Table I. Special techniques were used in the circuit design to achieve the required speed and T^3L compatibility. By carrying this circuit through design, layout, fabrication and evaluation in both a PMOS and a COS/MOS version, information on the development of MOS LSI circuits was obtained. This information was assimilated and forwarded to the Systems Development Division design centers.

Presentation of MOS technology and applications course

The increasing advantage of MOS LSI dictates that this technology be considered in future computer systems. To this end seminars on MOS technology have been prepared for presentation to the SDD design centers. The first seminar included a review of basic MOS technology, operating theory, logic circuit configurations, electrical characteristics, and circuit design. Subsequent seminars dealt with the implementation of MOS LSI and covered such topics as static and dynamic logic, MOS interface requirements, and MOS design techniques.

Implementation of a technical information retrieval system

This system has been implemented on the RCA BTSS time sharing facility. The system consists of an information file and a servicing/retrieval program. The file contains technical information relating to semiconductor technology potentially applicable to computer and peripheral equipment. It is generated from published literature, technical reports and other sources and is categorized according to subject. After entry into the system, items are retrieved by a computer search of the data file for a match of the subject matter code or key words and phrases. Although it has been implemented as a coherent means of filing and retrieving technical information for CME, the system is being expanded and should become an important source of semiconductor technology and application information for the Systems Development Division.

Distribution of SSD summaries

Activities in the Solid State Division, particularly advanced developments in the Technology Center, are closely monitored for potential application to Computer Systems. Reports from various activities are screened, summarized, condensed, combined with other pertinent information, and distributed to various Systems Development Division activities. These reports help bridge communication gaps between the two divisions.

Distribution of the Microelectronic Newsletter

Through close association with the Solid State Division in particular, and with the semiconductor industry in general, CME keeps updated on state-of-the-art technology and developments throughout the semiconductor industry. Information of potential application to computer and peripheral equipment is condensed and distributed in a newsletter to the Systems Development Division. Newsletter items cover new devices available from semiconductor manufacturers, devices in development and scheduled for announcement, and semiconductor technology trends. The information is obtained from the Solid State Division, other semiconductor manufacturers, technical periodicals, published reports, and technical conferences.

Miscellaneous

By working closely with the Technology Center, using facilities at Somerville, and maintaining close contact with the Systems Development Division, CME can recognize any technical shortcomings and make recommendations affecting microelectronic technology and applications. Positive recommendations for the development of techniques, consideration of applications, and improvement of aids and facilities have resulted from this close association.

Some of the more important proposals and recommendations have dealt with:

—Universal logic arrays to perform complex combinational and sequential logic.
—A universal set of COS/MOS gates to perform any logical combination of two inputs,
—Modification of COS/MOS gates to improve noise immunity when driven from T^3L or T^2L,
—Future use of specific LSI packages based on semiconductor industry trends,
—Development of improved input protection circuits for COS/MOS to avoid potential destruction when driven from T^2L, and
—An experimental laboratory method of determining MOS device parameters for use in Computer Aided Design programs.

Conclusions

During its first year of operation, the CME group has shown direct benefit from close association with the Technology Center, the Memory Products Division resident group, and other Solid State Division activities. CME participates in the design of SDD equipment and keeps the Systems Development Division informed on semiconductor technology and trends. The resulting technical information exchange has been particularly helpful to the Systems Development Division in formulating technical plans and implementing compatible development programs. The operation of the CME resident group has stressed direct engineer-to-engineer contact which has improved the technical interface between the divisions.

Acknowledgments

The author wishes to express appreciation to C. Neitzert, R. L. Giordano and K. A. Stephenson of the CME group for their technical assistance in the preparation of this article.

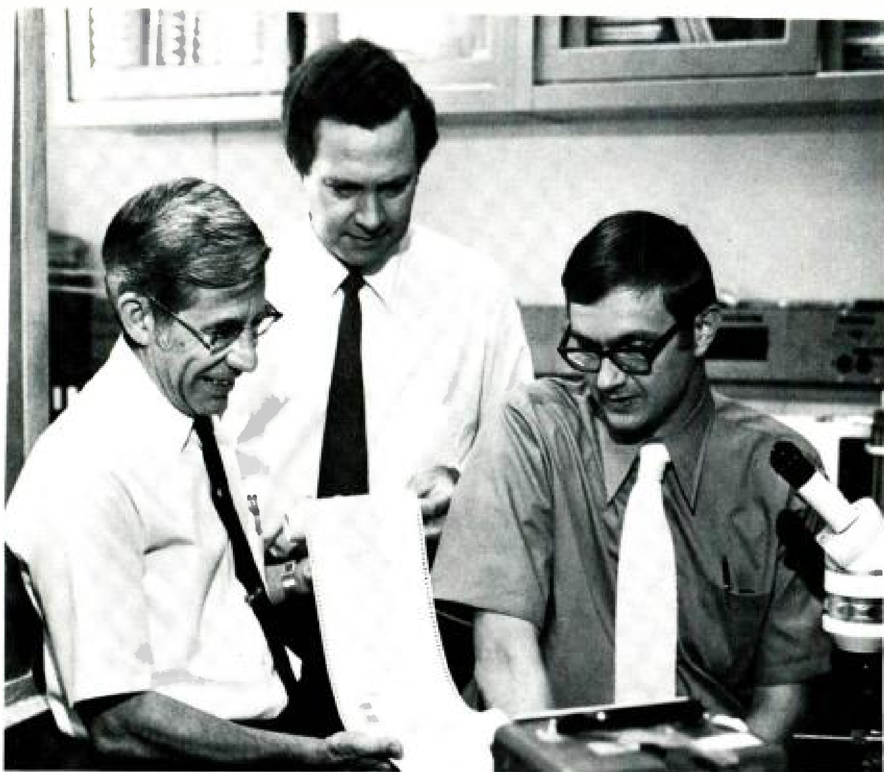
Table I—PMOS Character Buffer Performance

	Spec.	*Worst measured value*
Propagation delay clock to output	400 ns	290 ns
Data setup time	200 ns	119 ns
Parallel transfer setup time	400 ns	264 ns
Shift rate (min)	2.5 MHz	4.25 MHz
Clock pulse width (min)	200 ns	106 ns
Clock pulse width (max)	>5 μs	>5 μs
V_{OL} (DC) (I_{OL}= 2.5 mA)	0.800 V	.229 V
V_{OH} (DC) (I_{OH}= −200 μA)	3.800 V	4.140 V

Breakdown measurements of insulating films

Dr. J. E. Carnes | Dr. M. T. Duffy | Dr. C. W. Mueller

The breakdown strength of thin film insulators is an important design and production control parameter in MOS transistors, integrated circuits and capacitors. This paper describes a rapid method of obtaining the statistical data necessary to establish minimum and average breakdown values of thin film insulators. Breakdown values of aluminum oxide and silicon dioxide are given, and factors giving improved breakdown values are discussed.



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received a B.Sc. degree (*Magna Cum Laude*) from Notre Dame University in 1934, an MS in electrical engineering and an Sc.D. in physics from Massachusetts Institute of Technology in 1936 and 1942, respectively. Since 1942 he has been with RCA Laboratories and is presently head of the Storage and Computer Memory Devices Group in the Semiconductor Device Research Laboratory. Dr. Mueller developed the first alloy junction transistor for higher-frequency operation, and developed the thyristor type switching transistor. He also supervised the work leading to a parametric diode and the development of a low inductance ceramic enclosure for diodes. He received tne David Sarnoff Team Achievement Award in Science for his participation in the development of tunnel diodes. More recently he has been working on the growth of single-crystal silicon films on sapphire and the use of these films for electron devices and integrated circuits. Dr. Mueller has contributed to the recent developments of silicon vidicons and storage tubes, and holds many patents in the fields of electron tube and solid state devices In 1961-62 Dr. Mueller held the RCA European Study Fellowship and spent the year on special studies in the field of solid state physics at the Swiss Federal Institute of Technology in Zurich, Switzerland. Dr. Mueller was awarded the David Sarnoff Outstanding Achievement Award in Science in 1969 for outstanding contributions to semiconductor devices and circuits. He is a Fellow of the Institute of Electrical and Electronic Engineers, a Fellow on the RCA Laboratories Staff and a member of the American Physical Society and Sigma Xi.

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Breakdown strength of thin film insulators is an important consideration in the design of such devices as MOS transistors, integrated circuits, interconnections, and capacitors. The thickness of the insulating film can vary from nanometers to hundreds of nanometers, and the operating field strength is frequently near the breakdown value. The electrical properties of the thin film insulator must be carefully characterized and continually monitored. Designers must know minimum breakdown voltage, which should be specified with a safety factor. Scientists trying to develop an exact physical theory want to know the maximum breakdown voltage. Production or quality control engineers are interested in the average value of the breakdown voltage. Production engineers struggle continually to keep all these values as constant as possible.

Measurement technique

Since high voltage breakdown is usually destructive, collecting meaningful data about dielectric strength is often tedious. In the usual procedure, the material to be studied is sandwiched between two electrodes and the ap-

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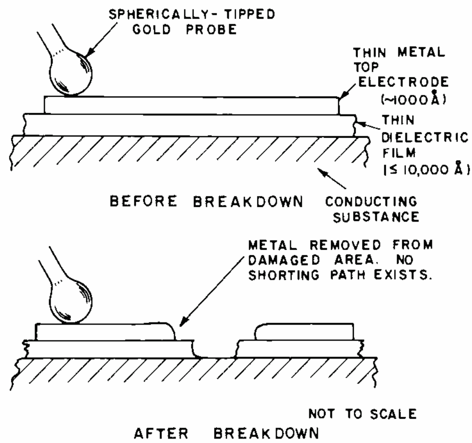

Fig. 1—Cross sectional view before and after a self-healing breakdown event on an MIS capacitor. Top metal electrode is removed from damaged area so no shorting path exists. Size of damaged area is out of proportion—typical damage is 5μm across.

plied voltage is increased. Breakdown creates a low resistance path through the material, preventing further measurement on the same sample. Each measurement therefore requires a new sample; breakdown occurs at the weakest point, and the measured dielectric strength is just an average corresponding to the weakest spots in a series of samples.

But the so-called self-healing breakdown technique (SHBD), introduced by Klein[1,2] permits many measurements of a single sample. This technique uses a thin (≤ 100 nm) metal electrode on a thin (≤ 1000 nm) dielectric film. When a voltage is applied across the film and breakdown occurs, the explosive action of the breakdown event removes the thin metal electrode from the region of destruction, thus eliminating possible formation of a conducting path or short. The test capacitor is still a "good" capacitor with slightly smaller area. Fig. 1 shows a schematic of the cross-section of a capacitor before and after a SHBD event. The damaged area is typically only several μm in diameter so that thousands of SHBD events can occur on one capacitor. The initial breakdown events occur at the weak spots in the dielectric film, but as the process continues these weak spots are destroyed and eventually the "intrinsic" or final breakdown strength is reached.

A ramp voltage technique, hereafter referred to as the ramp mode, is particularly useful for studying self-healing breakdown. A ramp voltage with variable rise time (1—100 V/sec) is applied across the sample. The voltage increases until breakdown occurs. At the onset of breakdown the increasing sample current fires an SCR, returning the sample voltage to zero (see circuit in Fig. 2). When the voltage drops below the holding voltage of the SCR, another ramp sequence begins. Only one breakdown event occurs per sequence. The voltage across the sample is recorded on a chart recorder producing a trace similar to that shown in Fig. 3. The breakdown voltage at each successive breakdown event (represented by the top of each vertical line in the trace) increases as weak spots are sequentially removed by the self-healing breakdown action. The fact that each peak of the trace always corresponds to only one breakdown was verified by observing the breakdown events with a high power microscope. It was experimentally shown that to insure this one-to-one correspondence gold was the best contacting metal and its thickness had to be controlled to 100±20 nm.

The value of the ramp mode technique is especially evident in Fig. 3. The trace evaluates the intrinsic breakdown voltage of the system being studied after all weak spots have been removed, this information is essential in fundamental studies of breakdown processes. And the trace also indicates the initial breakdown voltage—the only one which would be observed in normal thick electrode measurements. Further, the weak spot profile provides information about the density of weak spots in the sample. Thus, the technique is well-suited to technologically-oriented studies aimed at improving the dielectric performance of insulators in a variety of applications.

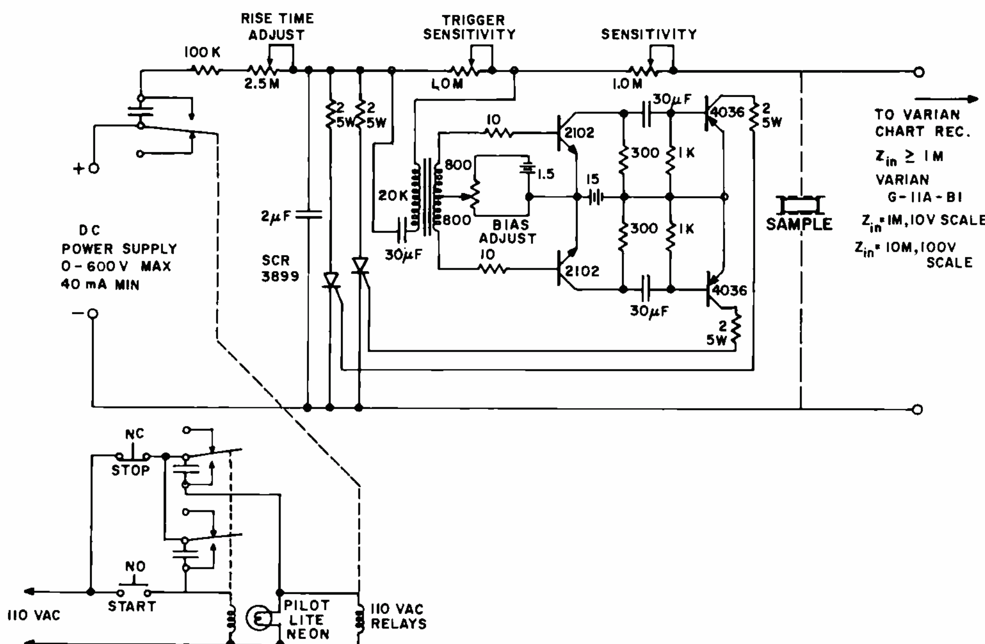

Fig. 2—Circuit used for ramp mode self-healing breakdown measurements.

Measurement of Al_2O_3 films

Thin films of aluminum oxide pyrolytically deposited on silicon substrates from an aluminum isopropoxide source have been studied extensively using this technique. The study of the intrinsic breakdown strength as a function of temperature, thickness, and electrode material provides insight into the basic cause of destructive breakdown, while the investigation of weak spot breakdown has resulted in techniques that can virtually eliminate this type of failure in these films.

Fig. 4 shows scanning electron micrographs of typical breakdown damage on Au-Al_2O_3-Si samples. The intrinsic breakdown strength for Si^+ on p-type material was 7.5×10^6 V/cm, and 6.9×10^6 V/cm for Si^{-4} on n-type. It was found to be temperature and thickness independent, strongly suggesting that a tunneling mechanism at one or both interfaces controls the breakdown process.

Surface preparation

Of more technological interest was an improvement by a factor of two in the

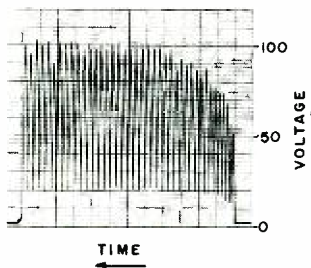

Fig. 3—Typical self-healing breakdown recorder trace for ramp mode. The tip of each line is the voltage at breakdown. Each successive breakdown has a higher breakdown voltage until all weak spots are removed.

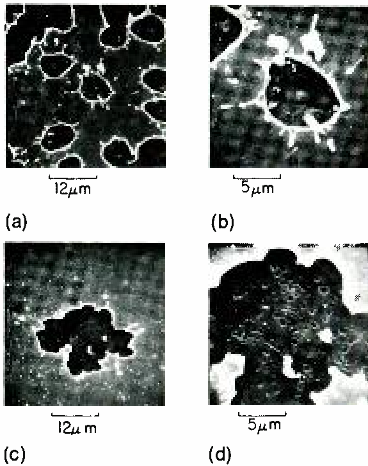

Fig. 4—Scanning electron micrographs of typical damage on p-type wafers (a) and (b) are both for Si^+; (c) and (d) for Si^-.

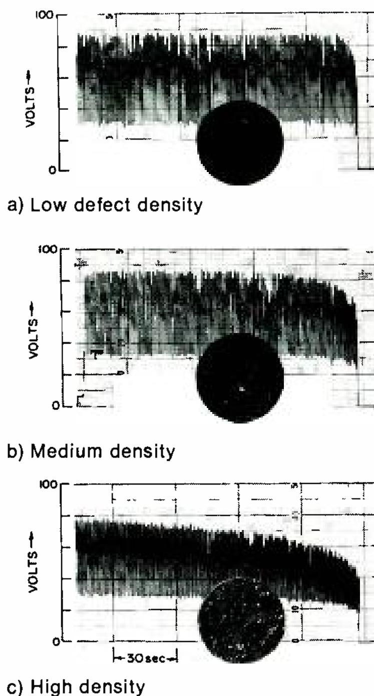

Fig. 5—Recorder traces for self-healing breakdown showing the weak spot profile for three different Au electrodes with different defect densities Au electrodes before breakdown are shown at 50X magnification in the inset on each trace.

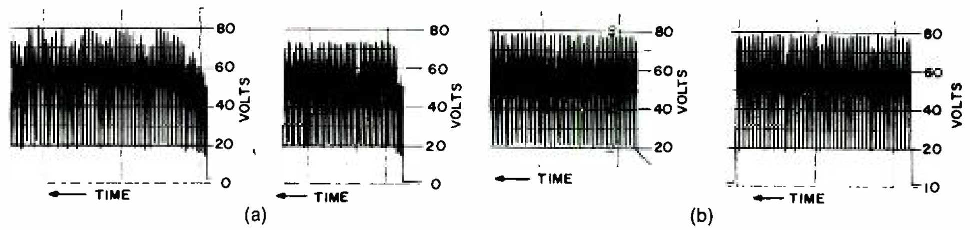

Fig. 6—Recorder traces for self-healing breakdown. (a) No HCl present during Al_2O_3 deposition. (b) HCl present during deposition. Si^+ on p-type, Al_2O_3 1000A thick, Au gates, area= 33 × 10^{-2} cm^2.

initial (weak spot) breakdown. Small surface imperfections on the silicon wafers as received from the supplier were found to cause weak spot breakdown. These defects, probably due to a polishing residue, were visible as white spots under dark field illumination and could not be removed using standard cleaning procedures or etches. Fig. 5 shows three different breakdown traces for three different densities of these spots. The spots clearly influence the weak spot profile shown in the breakdown trace, and they can be positively identified as breakdown nucleation sites by comparing "before and after" breakdown photographs.

Incorporation of HCl gas during the deposition of the Al_2O_3 has eliminated weak spot breakdown in these films and has approximately doubled the initial breakdown strength (Fig. 6).

Other film results

Other thin insulating films studied by this technique include thermally-grown SiO_2 and deposited silicon oxide, both before and after densification. A summary of the initial and final breakdown strengths obtained is shown in Table I. It is interesting to note that densification of the deposited SiO_2 actually decreased the measured dielectric strength on p-type wafers. The amount of data was limited, however, and wide variations in breakdown strength might be expected for this material depending upon the deposition facility and wafer preparation.

Table I—Initial and final breakdown strengths.

Insulator	*Si^+ on p-type initial/final MV/cm*	*Si^- on n-type initial/final MV/cm*
Al_2O_3 (Pyrolytic)		
w/o HCl	5.0/7.5	– /6.9
w/o HCl	7.5/7.5	– /6.9
SiO_2 (Steam @ 1080°C)	8.1/9.6	no data
SiO_2 (Steam @ 800°C)	7.4/10.1	7.6/10.7
deposited silicon oxide		
before densification	10.2/11.6	5.8/7.4
after densification	8.0/10.1	6.1/8.4
(15 min at 1100°C in He or N_2)		

Summary

In summary, the ramp mode self-healing breakdown measurement technique provides a rapid and straightforward determination of weak spot as well as intrinsic breakdown strength of insulating layers one μm or less in thickness. The technique is useful in both fundamental studies of dielectric breakdown as well as in more technologically-oriented investigations where production methods are developed or controlled.

Acknowledgements

We wish to thank G. Mark and R. Soltis for their assistance and efforts in sample preparation and measurements. The groundwork provided by J. Dunse in equipment construction and preliminary measurements has been invaluable.

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Hunting in hysteresis motors and new damping techniques

S. P. Clurman

Hunting, or small random phase excursions of the rotor in synchronous motors, may cause objectionable time displacement errors in video headwheel drives and other precision scanning systems. The causes of these excursions are discussed, and several completely electrical damping techniques are described.

When a synchronous motor drives a constant-torque load, its rotor motion may deviate slightly from the steady synchronous speed: the rotor phase angle may meander slightly about the constant-speed field vector angle. This meandering is called *hunting*. Excursions are usually oscillatory, with a characteristic period, but amplitude and phase vary randomly. In small-hysteresis synchronous motors used in timing and recording devices, and especially in video head wheel motors, the consequent time displacement error may be objectionable. But the exact nature of hunting in hysteresis motors has been a minor mystery: it is not uniformly present in all applications, and where present, its nature is often ambiguous.

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Behavior of classical synchronous motor

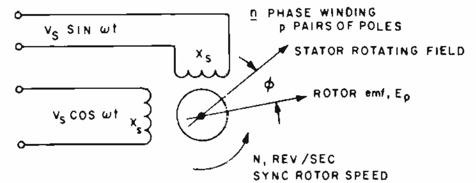
An analytic discussion begins with the elementary theory of classical synchronous motors. If we assume negligible resistance in the stator windings, the conventional equation for torque developed by a cylindrical rotor in separately excited rotor field (Fig. 1) is:[1]

$$T = (n/2\pi N)\,(V_s E_p/X_s)\sin p\phi \quad \text{(joule/radian)} \qquad (1)$$

where: n = number of phases; N = rotor speed in rps; p = the number of pairs of poles; ϕ = the mechanical phase angle, radians; E_p = peak value of rotor EMF; X_s = magnetizing reactance of stator in ohms; and V_s = peak line voltage.

The developed torque includes friction, windage, and slot loss (a virtual mechanical loss). When $\sin\phi \approx \phi$, the rotor stiffness is:

$$k_T = T/\phi \approx 1.412\,(np/N)\,(V_s E_p/X_s) \quad \text{(in-lb./radian)} \qquad (2)$$



TORQUE, $T = 1.412 \frac{n}{N} \frac{V_s E_p}{X_s} \sin(p\phi)$, INCH-LB

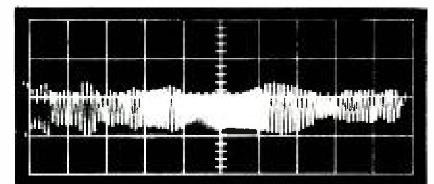
ROTOR STIFFNESS, $k_T = \frac{T}{\phi} \approx 1.412 \frac{np}{N} \frac{V_s E}{X_s}$, IN-LB/RADIAN

Fig. 1—Schematic of two-phase synchronous motor.

k_T may be regarded as the stiffness of an equivalent torsion-spring coupling the total rotor inertia, J, to the stator field. After a transient torque displaces the rotor angle from its steady-state value, the rotor returns to, overshoots, and oscillates about the steady-state position with a resonant frequency, $\omega_n = (k_T/J)^{1/2}$. The decay of this oscillation depends upon the damping inherent in a given motor.

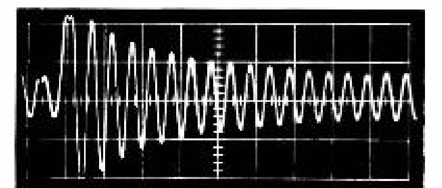
Rotor oscillations were measured with a phase detection circuit which compared the driving waveform with a pulse train generated by a tonewheel

VERTICAL SCALE:
4.8 μSECONDS/DIV.
(0.54 ROTOR DEGREES/DIV.)



HORIZONTAL SCALE:
2 SECONDS/DIV.

a) two samples of absolute TDE over 20 seconds;



VERTICAL SCALE:
24 μSECONDS/DIV
(2.7 ROTOR DEGREES/DIV.)
HORIZONTAL SCALE:
0.5 SECONDS/DIV.

b) recovery from a torque transient.
Fig. 2—Undamped motor oscillations.

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on the shaft. A sample rotor oscillation for a highly underdamped hysteresis motor after a torque disturbance is shown in Fig. 2b. The resonant frequency is 3.8 Hz.

Time displacement error

Under steady-state conditions the rotor drives against a steady torque, T_o, and assumes a steady phase angle, ϕ_o. When the torque is increased by an increment ΔT, the rotor phase angle increases by $\Delta\phi = \Delta T/k_T$. If the incremental torque is a sinusoidal function, the rotor displacement response at resonance increases over the DC value ($\Delta T/k_T$) by the ratio of $Q = 1/2\zeta$ where ζ, is the critical damping ratio, C/C_c.[2]

In a precision device there may be low level random torque variations (e.g. head-tape friction). Such disturbances will appear as a series of torque pulses, of very short duration compared to the natural period of rotor oscillation. One impulse will disturb the rotor and cause it to oscillate. If the motor is underdamped, the rotor will still be "ringing" when a second impulse occurring in some random phase relationship, either increases or decreases the amplitude of motion. This sequence of events is a continuing one.

In another approach the random torque is considered to have an effective power spectral density, W_M. If the motor is underdamped and the torque spectral density is relatively uniform, the mean square rotor displacement will be:

$$\phi^2 = (\pi/4\zeta)\,(\omega_n/k_T^2)\,W_M \qquad (3)$$

Two samples of hunting in an underdamped motor running at no-load are shown in Fig. 2a.

In timing devices and recorders, the angular position of a shaft establishes a time base and any perturbation of the nominal angular rate will affect this time base. Assume that a motor is running with an average angular velocity Ω_o, and hunting with a peak angular excursion ϕ_P at the resonant frequency ω_n. When the deviation of the instantaneous speed is small (for the relatively severe hunting shown in Fig. 2a, the peak deviation was only ±.00022) the maximum time displacement error

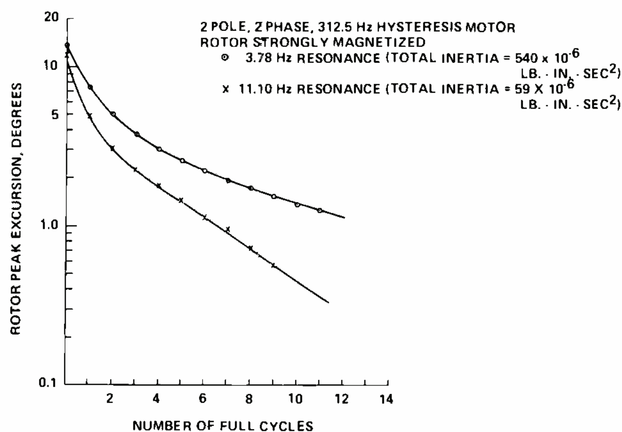


Fig. 3—Logarithmic decay of rotor oscillation.

can be accurately expressed[3] as $\Delta t \approx \phi_P/\Omega_o$.

The nature of hunting in hysteresis motors

The behavior of underdamped hysteresis motors so far appears consistent with linear theory. The recovery from a torque transient superficially resembles that of a lightly damped mass-spring system. Closer examination of the damping characteristics, however, reveals a departure from linear behavior.

The oscillation shown in Fig. 2 has nonconstant logarithmic decrement. To show this more explicitly, logarithmic plots of peak angular excursions were made for other similar oscillograms. By changing the flywheel we obtained two plots for the same motor at two different resonant frequencies (Fig. 3). Both plots are straight lines when rotor excursions have peak values of less than about 2°, but above this value the plots are non-linear.

Non-linear damping was explored for three different motors. Two techniques were used to determine the value of Q as a function of peak rotor excursion: a) measurement of decaying free oscillations, and b) recording the velocity response of the motor to an FM input. These values are plotted in Fig. 4. In all plots Q varies inversely with rotor excursion. The data indicate that Q approaches a constant value below some minimum value of ϕ.

A simplified qualitative theory is offered to explain the variable Q.

The magnetic torque developed in the hysteresis rotor is proportional to the area of its cyclic **B-H** loop.[4] For an oscillating rotor, the **B-H** loop area varies between a minimum and maximum so the torque fluctuates about a mean value T_o, with peak excursions of $\pm\Delta T$. The locii of **B-H** values for the various elements in the rotor are considered recoil permeability paths with elliptical minor hysteresis loops (Fig. 5).

The simplifying assumptions will be made that the rotor flux density and

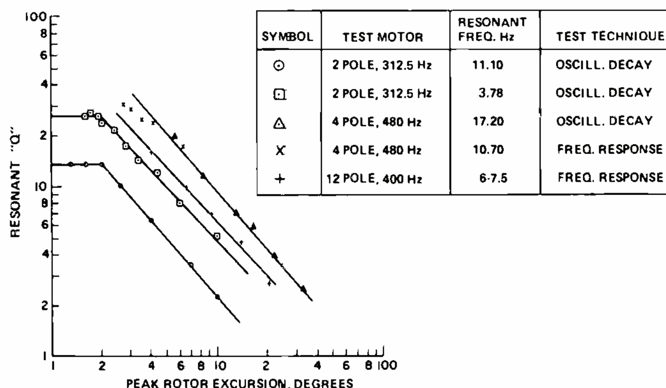


Fig. 4—Resonant amplification vs. rotor excursion.

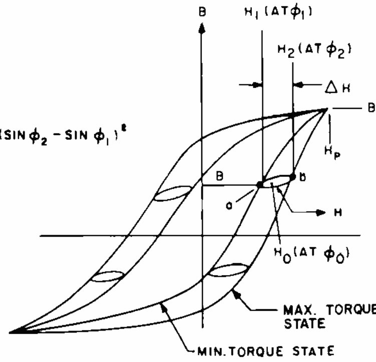


Fig. 5—B-H loops at peak rotor excursions.

the stator magnetic field have sinusoidal distributions with peak values of $\mathbf{B}_P$ *and* $\mathbf{H}_P$, respectively, and that $\mathbf{B}_P$ does not change significantly with torque. This makes the area of the **B-H** loop equal to $\mathbf{B}_P\mathbf{H}_P \sin\phi$.

At any point of the rotor, having a reference angle β, **H** will vary between $\mathbf{H}_1 = \mathbf{H}_P \sin(\beta - \phi_1)$ and $\mathbf{H}_2 = \mathbf{H}_P \sin(\beta - \phi_2)$. The energy dissipated by each element during the oscillation is represented by the areas of the minor hysteresis loops. If we make the assumption that each minor loop is an ellipse with an aspect ratio which doesn't depend on $\Delta\mathbf{H}$, then the energy dissipated per cycle, W_H, will be proportional to $\int(\mathbf{H}_2 - \mathbf{H}_1)^2\, d\mathbf{B}$.

$$W_H \propto \mathbf{H}_p^2 \int_0^{2\pi} [\sin(\beta - \phi_2) - \sin(\beta - \phi_1)]^2 d\mathbf{B} \quad (4)$$

$$W_H \propto 2\pi\mathbf{H}_p^2 [1 - \cos(\phi_2 - \phi_1)] \approx \pi\mathbf{H}_p^2 (\phi_2 - \phi_1)^2 \quad (5)$$

The total variation of magnetic potential energy, $(2\ W_E)$, *is* $\mathbf{B}_P\mathbf{H}_P(\sin\phi_2 - \sin\phi_1)$. The value of Q for this oscillation is $2\pi(W_E/W_H)$.

$$Q \propto 2\pi[\tfrac{1}{2}\mathbf{B}_p\mathbf{H}_p(\phi_2 - \phi_1)] / [\pi\mathbf{H}_p^2(\phi_2 - \phi_1)^2] = \mathbf{B}_p/(\mathbf{H}_p\Delta\phi) \quad (6)$$

In a simple synchronous motor, the peak air gap mmf is proportional to the voltage, V, applied to the stator windings.

$$Q \propto \mathbf{B}_p/(V\Delta\phi) \quad (7)$$

This relationship confirms our experience with the three parameters involved:

1) Q varies inversely with $\Delta\phi$, as shown in Fig. 4.
2) When the rotor flux level is increased, Q is increased.
3) Raising the voltage moderately appears to decrease Q.

The above analysis considers hysteretic damping only. There are, of course, eddy current effects which are believed to be linear. At larger rotor excursions, hysteresis is the dominant effect and the Q varies inversely with $\Delta\phi$. When the excursions become small, hysteresis decreases rapidly, leaving eddy current effects as the dominant factor, limiting the value of Q.

Development of a damping action

To damp oscillations: (a) the oscillatory velocity must be detected and (b) an incremental torque must be developed which is 180° out of phase with this velocity. These tasks might be performed by existing techniques for sensing errors and torquing shafts, but performing both tasks electronically within the motor driving circuitry, without special transducers, provides a simpler, cheaper, more elegant solution.

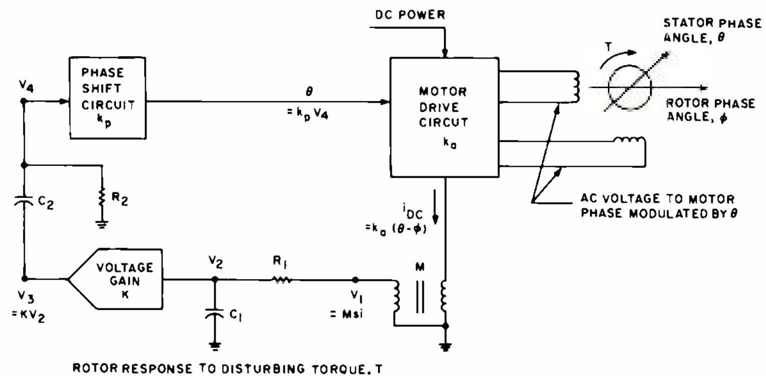
The foregoing discussion is valid for motors driven from any power source, but the techniques yet to be described are oriented toward AC voltage sources derived from DC power supplies through switching type inverters (as opposed to DC powered linear amplifiers). At constant voltage, the DC current in hysteresis motors of even moderate efficiency is a relatively linear function of torque. For constant voltage and frequency drive, the change in DC current is nearly proportional to the change in rotor phase angle and $\Delta i = -k_a\Delta\phi$.

A momentary torque increment, ΔT, may be induced in the motor by modulating the phase angle of the motor drive frequency by $\Delta\phi$, or by modulating the voltage level to the motor by ΔV. Either of these effects can influence the DC current.

For small perturbations these two functions are described by:

$$\Delta T \approx -k_T\Delta\phi + K_T\Delta\theta + (T_o/V_o)\Delta V \quad (8)$$

$$di/dt = -k_a(d\phi/dt) + k_a(d\theta/dt) + (\partial i/\partial V)(dV/dt) \quad (9)$$



$$\phi(S) = \frac{\left[\left(1 - \frac{U}{\tau_1}\right)S^2 + \left(\frac{\tau_1 + \tau_2}{\tau_1\tau_2}\right)S + \frac{1}{\tau_1\tau_2}\right]\frac{\omega_n^2}{k_T} \times T(S)}{\left(1 - \frac{U}{\tau_1}\right)S^4 + \left(\frac{\tau_1 + \tau_2}{\tau_1\tau_2} + 2\delta_o\omega_n\right)S^3 + \left[\omega_n^2 + \frac{2\delta_o\omega_n(\tau_1 + \tau_2) + 1}{\tau_1\tau_2}\right]S^2 + \left[\frac{2\delta_o\omega_n + \omega_n^2(\tau_1 + \tau_2)}{\tau_1\tau_2}\right]S + \frac{\omega_n^2}{\tau_1\tau_2}}$$

WHERE: k_T = ROTOR STIFFNESS
ω_n = UNDAMPED NATURAL RESONANCE
$\tau_1 = R_1C_1$
$\tau_2 = R_2C_2$
$U = K \times k_p \times k_a \times M$
δ_o = OPEN LOOP NATURAL DAMPING RATIO

MINIMUM REQUIREMENT FOR LOOP STABILITY: $U/\tau_1 < 1$

Fig. 6—Block diagram damping loop using phase shift.

The equation of motion of a rotor with natural damping, ζ_o, is:

$$d^2\phi/dt^2+2\zeta_o\omega_n(d\phi/dt-d\theta/dt) = (\omega_n^2/k_T)\Delta T \quad (10)$$

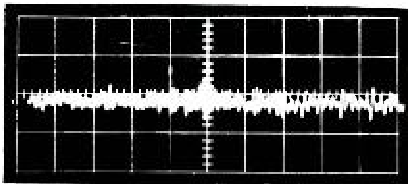
When the damping circuit has a suitable transfer function, $\Delta\phi=f_1(\Delta i)$, or $\Delta V=f_2(\Delta i)$, the simultaneous solution of the above three equations will lead to an equation for a damped oscillatory system.

Active damping circuit using phase shifting

Fig. 6 shows a block diagram for an active damping loop which shifts the driving phase, θ. Using the notation of Fig. 4, $\theta=k_pV_4$. For a DC-coupled amplifier, $\theta=Kk_pV_2$. The inductor in the DC line develops a voltage $V_1=M(di/dt)=[U(dV_2/dt)-Mk_a(d\phi/dt)]$, and the desired velocity signal will be $-Mk_a(d\phi/dt)=[V_1-U(dV^2/dt)]=V_2$. Expressed as a Laplace transform, this becomes $V_2=V_1/(U\mathbf{S}+1)$. This, however, is exactly the transform of the R_1-C_1 lowpass when its time constant, τ_1, equals U: the amplifier thus receives a virtual velocity signal. The R_2-C_2 highpass is not basic to the damping concept, but is included for practical circuitry reasons.

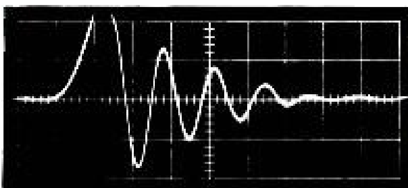
When this loop is closed, the transform of the rotor response to a torque $T(S)$ is as shown in Fig. 4. The minimum requirement for loop stability of this system is $U/\tau_1<1$.

Fig. 7 shows the damping action of such a loop: Fig. 7a shows the long term hunting excursion, Fig. 7b shows the recovery from a torque transient. The motor is the same one whose undamped behavior was described in Fig. 2. The long-term hunting peak excursion has been reduced from as high as 20 μs, pp to less than 2 μs, pp.



VERTICAL SCALE:
2.4 μSECONDS/DIV
(0.27 ROTOR DEGREES/DIV.)
HORIZONTAL SCALE:
2.0 SECONDS/DIV.

a) absolute TDE over 20 seconds



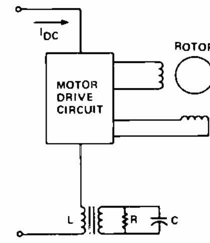
VERTICAL SCALE:
24 μSECONDS/DIV
(2.7 ROTOR DEGREES/DIV.)
HORIZONTAL SCALE:
0.2 SECONDS/DIV.

b) recovery from a torque transient
Fig. 7—Damped motor oscillations

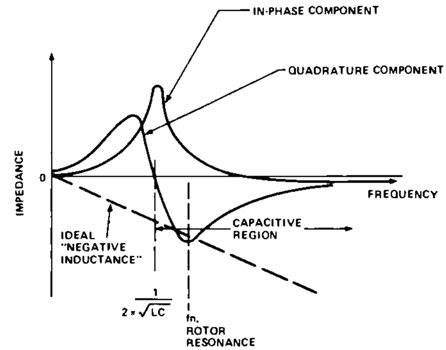
Other types of damping circuits

Two voltage control techniques which have been breadboarded successfully will be described very briefly. Equations (8), (9), and (10) were employed to obtain the equation of motion. This is a non-linear differential equation, but can be linearized for small perturbations. An active voltage control loop was constructed to feed a damping signal to a power amplifier whose output was transformer-coupled back into the DC line. The block diagram of the active loop resembled Fig. 7, but the power amplifier replaced the phase shift circuit.

Placing an impedance in series with the the DC line yielded a passive damping circuit: the damping voltage was due to the volt drop across the impedance. An active damping circuit can be designed theoretically to have an ideal action, but the ideal impedance of a passive circuit would be a "negative inductance" in parallel with a "negative resistance." Fig. 8a shows a motor and drive circuit with a parallel L-C-R transformer-coupled into the DC line. In Fig. 8b, the impedance of the ideal negative inductance is plotted against frequency, along with in-phase and quadrature components of the real L-C-R impedance. Values that make the quadrature component negative, or capacitive, in the vicinity of the rotor resonance create a damping voltage in a narrow frequency band around mechanical resonance. This is precisely the band where a linear damper does most of its useful work (a significant corollary: when the DC source impedance is inductive at the resonant frequency, hunting is accentuated). The breadboard version of this technique was quite satisfactory, reducing the undamped time displacement error by an order of magnitude.



a) L-C-R damping circuits.



b) components of parallel L-C-R impedance.
Fig. 8—Passive damper circuit

Generally speaking, voltage control techniques involve heavier, power-handling components. In contrast, the phase shifting circuit described used small, low-power components which occupied a section of a printed circuit board measuring about 3" by 2".

Conclusion

Time displacement errors in undamped hysteresis motors can be reduced when suitable damping is added. The natural damping of the motor is a variable effect which depends upon the rotor angular excursion, the level of rotor magnetization, and the driving voltage. Low power damping circuits have been developed which require no motion sensing transducers, significantly reduce the hunting excursion, and cause no loss of motor power or efficiency.

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The Engineer and Professional Societies

I. M. Seideman

A new field of science or technology usually fosters a new professional society. The need is apparent to the pioneers, but an engineer entering the field later may ponder the advantages of joining. With the proliferation of societies, he may also ponder his selection of those available to him. Societies differ widely in their goals, size, complexity, and services. This article discusses society problems in general and presents examples of societies that typify the differences or extremes. These organizations range from the multidiscipline IEEE to the small, specialized Society of Vacuum Coaters, and the "umbrella" American Institute of Physics. All societies of interest to RCA engineers are not mentioned here. Comprehensive listing and descriptions of societies are contained in several publications.[1,2,3,4]

Professional societies of the 1970s are most receptive to suggestions from their members for modernizing goals and updating services. Traditions are being reevaluated; roles are changing. Many societies publish papers on social and economic issues, and some have started to engage in activities that implement changes in these areas. Thus, as members of these organizations, RCA engineers may, as always, contribute to the advancement of a specific technology and, at the same time, participate in and expedite those changes that work toward the general social betterment.

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Current role of societies

Professional societies provide a forum for the interchange of information within a professional field or across several. The major services of these societies are:

1) Dissemination of new information throughout the field and archival storage of such information.
2) The establishment of definitions and standards for the profession and its associated technology.
3) Public acknowledgment of significant contributors to the various professional fields.
4) Consultation and planning with government and industry on practical directions for new research and development.

Most societies maintain an administrative and service staff at some central headquarters, but the majority of the work toward achieving the societies' goals is performed by volunteer committees. Although the "committee system" is regarded by some as inefficient, a society committee is most frequently democratic and productive, and may be properly defined as "a select group of competent specialists who integrate their diverse backgrounds and experience into practical recommendations for the solution of the problem."

Publications and meetings

Information is disseminated through published journals containing papers that describe significant work in the field, more general surveys of developments over a period of time, and the effect of technological development on our society and its culture. Most societies hold at least one major meeting per year at which significant papers are presented. A dinner speech discussing the effect of general trends in the nation upon the future of the technology (or vice versa) is given by a prominent speaker; and often, new equipment related to the technology concerned is exhibited.

Local meetings of society "chapters" are held at more frequent intervals to maintain technical and social relations among professionals working in the area, to present talks on pertinent topics, and to discuss issues relating to the whole society.

Standards

Most societies work to standardize informational material common to their field, such as specifications for equipment characteristics, parameters, and testing; specifications for materials; and standard terms, abbreviations, and definitions.

Awards

Outstanding work in a field is acknowledged by citations and awards, the latter often including honorariums that range as high as the $10,000 Goddard Award, established in 1963 by the AIAA and United Aircraft Corporation. The membership grade of Fellow has been established in many societies for those who have made exceptional contributions to their profession.

Scope

Fields of interest of professional societies range from the broad coverage of the IEEE (some 27 special-interest groups) to the highly specialized field of the 300-member Society of Vacuum Coaters (concerned with metal deposition under vacuum). Interests also range from the highly theoretical of the member societies of the American Institute of Physics to the intensely practical of the American Society for Testing and Materials.

Professional societies often apply the analytic approach inherent to engineering in examining the broad implications of government actions and economic phenomena. The factual results are made available to the scientific community, the industry concerned, and the government interests involved. When technological problems requiring immediate attention are recognized, military and civilian organizations often seek initial advice from a professional society. Although the contact may be made with the society's headquarters or with an *ad hoc* committee, the society's journal, by publicizing the problem and any proposed solutions, engages the attention of an entire scientific community.

Recently, members have become interested in having their society assume

a broader social role; however, according to some societies, reorganizations along this line involve more of a change than would first be apparent, and the effectiveness of the society in a new role would await the gaining of experience and sophistication. However, a trend is observable. Several societies recently have published papers on the sociological effects of technical development. Society interest in "portable pensions" is growing. One society now has arranged to manage this type of pension plan for interested organizations and also to provide industry with standardized plans to make possible interaction among organizations managing their own funds. Some societies provide a job-placement service, some society publications list available jobs and available personnel, and several societies are holding educational sessions to assist unemployed engineers in reestablishing their careers.

Societies are beginning to recognize the value of fresh and creative viewpoints of younger engineers. A veteran leadership is not always quick or responsive to change necessary for effective society operation. Not that societies are unaware of the need to modernize; more likely, they need the bolder guidance of younger members not as inhibited by convention and tradition.

RCA and professional societies

RCA encourages its engineers to join professional societies. Corporate Engineering Services, through the Staff Manager of Technical Publications, has set up an organization to assist engineers with papers intended for society meetings and publications. Each RCA Division or Major Operating Unit designates a Technical Publications Administrator who operates under the aegis of the Staff Manager to obtain reviews of each paper, to ensure that it is of acceptable quality, and to assist the author in preparing and placing his paper. Supervisors cooperate by promptly reviewing papers and providing constructive advice.

Society membership should be more than paying dues and scanning the monthly journal. Membership can be beneficial to the individual, his technical field, and his company. At society meetings, the engineer exchanges ideas which could prove beneficial to his own activity; he may also discover parallel activity in his own field, which could call for a reevaluaton of his work.

Should he be appointed to a committee, he will quickly learn the virtues of restraint and compromise. Here the principles of leadership can be developed: the stimulation of others and the inspiration to action.

Many RCA engineers serve as officers, committee chairmen, session organizers for conventions, or journal editors. With their understanding of the needs of industry, government, and the public, these RCA engineers can help formulate society goals and activities to best serve the profession.

As an example, standardizing is a welcome activity for a society in a new technical field. As the field grows and overlaps other fields, an organization specifically formed for the establishment of standards should become the publishing agency. Alert society members will see that early cooperation is established and, particularly, that conflicting standards are avoided.

The engineer's ethical responsibility to his company, the government, and the public is a subject of much current debate. Precipitous individual action, as a result of apparent conflict, is not the way to bring about change. In this sense, too, the technical society may be a source of broader information, a forum for other points of view, and a base for more-effective, cooperative action.

Within RCA, the *RCA Engineer* carries news of professional society meetings and activities in its "News and Highlights," "Pen and Podium," and "Dates and Deadlines" sections.

The Institute of Electrical and Electronic Engineers (IEEE)

IEEE is one of the largest professional engineering societies in the world, with a total membership of about 160,000. It also ranks among the oldest; one of its predecessors, the American Institute of Electrical Engineers (AIEE) was founded in 1884. In 1963, AIEE merged with the Institute of Radio Engineers (IRE) to form the present Institute. It is a "transnational" organization, with members in many foreign countries.

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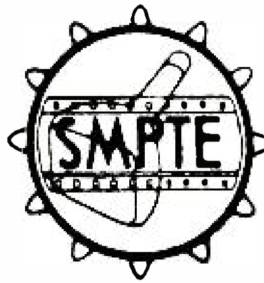
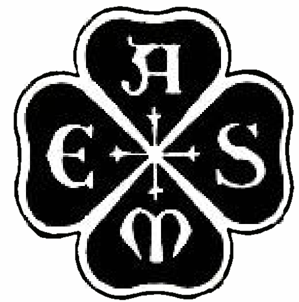
received the BS in Physics from Carnegie Institute of Technology (now Carnegie-Mellon University) in 1941. After graduation, he joined RCA Victor Company at Camden as an engineering writer and has been at RCA ever since, except for a short period of time when he was engaged in industrial sales and advertising. In 1962, he became a Group Leader and, a few years after, Manager of an engineering documentation group at AED. In his present capacity he assists in the publication of professional papers; acts as divisional representative for corporation-sponsored technical and scientific journals; and administers the given policies for formal interchange of technical information throughout the corporation. Mr. Seideman is a member of the administrative committee on Professional Communications (formerly Engineering Writing and Speech) of IEEE and is Editor of the *Transactions*.





In addition to 195 Sections, located throughout the world, IEEE has three "Societies" and twenty-seven "Groups," each concerned with a specialized field, operating within the framework of the Institute. These are listed in Table I. IEEE holds an International Convention and Exhibit in March of each year as well as several regional meetings. The Societies and Groups hold national meetings, and many local chapters hold monthly meetings. Various educational seminars and tutorial lectures and workshops are scheduled each year.

Table I—IEEE Societies and Groups.

Societies
- Computer
- Control Systems
- Power

Groups
- Audio and Electroacoustics
- Broadcasting
- Antennas and Propagation
- Circuit Theory
- Nuclear Science
- Vehicular Technology
- Reliability
- Broadcast and Television Receivers
- Instrumentation and Measurement
- Aerospace and Electronic Systems
- Information Theory
- Industrial Electronics and Control Instrumentation
- Engineering Management
- Electron Devices
- Microwave Theory and Techniques
- Engineering in Medicine and Biology
- Communication Technology
- Sonics and Ultrasonics
- Parts, Materials and Packaging
- Education
- Engineering Writing and Speech
- Electromagnetic Compatibility
- Systems, Man, and Cybernetics
- Geoscience Electronics
- Electrical
- Magnetics
- Industry and General Applications

IEEE publishes its general-interest journal, *Spectrum*, and its more technical journal, the *Proceedings*, each month. Thirty-one *Transactions* and two *Journals*, most of which appear bimonthly or quarterly, are published by the Groups and Societies. In addition, many Groups publish their own convention Records or Proceedings. Recently, IEEE Headquarters started production of magnetic-tape cassettes, containing information on the latest developments in IEEE fields of interest.

Some 300 *Standards* have been published, including Specification Formats, Test Procedures, Recommended Measurement Practices, Definitions of Terms, Symbols, and Abbreviations.

In a most recent development, the IEEE and the National Society of Professional Engineers (NSPE) have reached an agreement to permit nonregistered engineers who are members of the IEEE to join the NSPE. The President of IEEE, Dr. J. H. Mulligan, Jr., stated:

> "The leadership is well aware of the increasing interest of many of its members in matters of economic, social, and political involvement. IEEE has traditionally limited its activities to the dissemination of technical information . . . In contrast, the NSPE has . . . developed programs and accumulated expertise in many areas in which IEEE members are presently expressing concern."

President Harry C. Simrall, P. E., of the NSPE further explained:

> . . . many IEEE members have expressed a desire for greater participation in the nontechnical problems facing our profession—areas in which the NSPE has been involved for many years. [These] include government liaison, both in the legislative process and the administrative decisions, and at the Federal, state, and local levels. They are concerned with the broad employment problems, ranging from [those] they have as individuals to such things as portable pensions, patent rights, and registrations."

Thus, IEEE members participate in a society that consolidates the broad, general interests of engineers in many fields, and one that is mature in its operations relating to the social and economic scene.

The American Society of Mechanical Engineers (ASME)

This Society was founded in 1880 as an educational and technical society. It now has more than 63,000 members, including 10,000 of Student grade. ASME's business is directed from a national headquarters in New York City; the organization structure includes both the conventional "Sections" and Professional Divisions, each of the latter specializing in a technical area of mechanical engineering. The Professional Divisions are listed in Table II.

The Society holds two general business meetings each year. Division Conferences, sponsored by one or more of the Professional Divisions, feature technical programs, inspection trips, and committee meetings relating to a single area of interest, such as Aviation and Space, Heat Transfer, or Design Engineering. *Transactions of the ASME* are published in a series of seven quarterlies:

Journal of Engineering for Power
Journal of Engineering for Industry
Journal of Heat Transfer
Journal of Basic Engineering
Journal of Lubrication Technology
Journal of Applied Mechanics
Journal of Dynamic Systems, Measurements, and Control

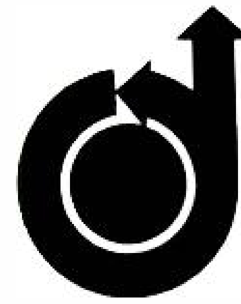
The Society also publishes the monthly *Applied Mechanics Reviews*, which presents critical reviews of books and articles published on applied mechanics and related sciences. Another monthly, *Mechanical Engineering*, contains accounts of the Society's meetings and conferences, condensations of technical papers, and articles of general interest.

ASME, within five years of its inception, undertook the formulation of standards and codes. Notable among these are the standard screw threads. It has published work in standardization, industrial safety, boiler codes, and performance test codes. The Society also sponsors engineering research projects, the results of which are useful to large segments of industry and which also increase the effectiveness of its members. Funds for such projects are solicited from industry; the work is contracted to some research organization, under ASME committee supervision; and the results are published. ASME actively cooperates with national and international organizations through joint conferences, joint research, and the development of international standards.

Table II—ASME Professional Divisions.

Air Pollution Control	Metals Engineering
Applied Mechanics	Nuclear Engineering
Automatic Control	Petroleum
Aviation & Space	Plant Engineering & Maintenance
Biomechanical & Human Factors	Power
Design Engineering	Pressure Vessels & Piping
Diesel and Gas Engine Power	Process Industries
Energetics	Production Engineering
Fluids Engineering	Rail Transportation
Fuels	Rubber & Plastics
Gas Turbine	Safety
Heat Transfer	Textile Engineering
Incinerator	Underwater Technology
Lubrication	
Management	
Materials Handling	

There is also one group concerned with Solar Energy Applications.



American Institute of Aeronautics and Astronautics (AIAA)

This society is devoted to science and engineering in the fields of space technology, rocket systems, aeronautics, and marine systems. It was formed in 1963 from a merger of the American Rocket Society (founded in 1930) and the Institute of Aeronautical Sciences (formed in 1932). The total membership is approximately 39,000.

AIAA holds an Annual Meeting and Technical Display, and typically holds nearly 30 national technical meetings each year in various parts of the country, some co-sponsored with other professional societies. In addition to the presentation of papers, meetings include visits to governmental aerospace facilities as well as exhibits of aircraft, space, and marine vehicles and associated R and D hardware.

Publications include five journals, the best known of which are the *Journal of Spacecraft and Rockets* and the basic archival publication, *AIAA Journal.* Each member also receives the monthly magazine *Astronautics and Aeronautics.* A continuing education service is provided in the form of the AIAA Professional Study Series, intensive two-day seminars on the basics of various subjects. There are four of these each year.

AIAA is a member of the International Aeronautical Federation (IAF), made up of 54 professional societies in 34 countries. The IAF acts as Secretariat for the International Council of the Aeronautical Sciences, and is a co-sponsor of the Anglo-American Conference in conjunction with the Royal Aeronautical Society and the Canadian Aeronautics and Space Institute. A bi-annual conference on subjects of mutual interest to the three societies is held alternately in the United Kingdom and on the North American continent.

The AIAA is working with organizations such as the Engineers Council for Professional Development (ECPD) at the regional and state levels to establish guidance programs which will assist students in selecting one of the many engineering fields as a career. A long range planning group has been set up to establish plans for the projected developments in the aeronautical industry over the next 10 years.

On a national basis, special committees interact with other professional societies and groups outside the aeronautical field; for example Section Members who are experts in the fields of ecology and systems planning in urban environments are freely contributing their know-how to local government agencies.

The American Society for Quality Control (ASQC)

ASQC celebrates its 25th anniversary in 1971 with approximately 25,000 members. It is a world-wide organization with sections located in major cities throughout the United States, Canada, Mexico, and Japan. Members in other countries belong to an international chapter. Its interests range through the fields of quality control, reliability, inspection, statistics, engineering, and research and development.

The Society publishes a monthly news magazine, *Quality Progress,* a quarterly periodical, *Journal of Quality Technology,* and (sponsored jointly with the American Statistical Association) the quarterly journal *Technometrics.*

ASQC sponsors a professional certification program for quality managers, engineers, and technicians, which is designed to prevent obsolescence and enhance their positions in the professional field.

This and other courses and seminars are conducted by the Society's Education and Training Institute. Cooperative efforts with colleges and universities are making available courses and curricula leading to undergraduate and graduate degrees in quality control.

The Society of Motion Picture and Television Engineers (SMPTE)

This society was founded in 1916 as the Society of Motion Picture Engineers, and later expanded its scope (and changed its name) to embrace the related field of television. Presently, there are nearly 6500 members. Semiannual technical conferences are held, usually one on the West Coast and the other on the East. These meetings are a major source for the papers published in the *SMPTE Journal.* More frequent meetings are held by the 16 chapters or sections of the Society, located throughout the United States.

The Society also plays an important role in standardization. As a rule, a standard generated by SMPTE becomes an American Standard and is accepted as such by the motion picture and television industry in this country. The dimensional standards for 8, 16, and 35 mm film, for example, were set in this manner. The Video Tape Recording Committee has been particularly active in recent years, establishing dimensional and operational standards for video tape.

The SMPTE standardizing activities also include the development and distribution of test slides and films. For example, films are available to aid in the alignment of the sound systems of film projectors and in the measurement of overall frequency response. For television applications, a series of test slides is available.

The American Institute of Physics (AIP)

The Institute was founded in 1931 as a federation of leading societies in the field of physics. It is essentially a service organization for its member societies, having no exclusive individual memberships or meetings. It combines into one operating agency those functions on behalf of physics that can best be done by the societies jointly. Its purpose is the advancement and diffusion of the knowledge of physics and its application to human welfare. The constituent societies are listed in Table III. Their total membership is almost 48,000, exclusive of student and Corporate mmebers.

The Institute publishes nine journals for the constituent societies, six archival journals, and *Physics Today,* a journal of general interest. It "encourages and assists in the documentation and study of the history and philosophy of recent physics; cooperates with local, national, and international organizations devoted to physics; and fosters the relations of the science of physics to other sciences and to the arts and industries."

Manpower and statistical studies relating to education and employment are conducted and reported. The Institute also maintains a personnel placement service at its New York headquarters.

Table III—Member Societies of the AIP.

The American Physical Society
Optical Society of America
Acoustical Society of America
Society of Rheology
American Association of Physics Teachers
American Crystallographic Association
American Astronomical Society

Association for Computing Machinery

The ACM was founded in 1947 as the society of the computing community. Presently there are more than 26,000 members of the Association operating in every branch of the computing sciences —from design and construction of computing machinery to development of programming theory and languages, and to utilization of computers in scientific investigation, industrial control, management data processing, and the humanities. The aim of the ACM is the development of information processing as a discipline, and the responsible use of computers in an increasing diversity of applications.

The Journal of the Association for Computing Machinery (quarterly) is primarily devoted to research and technical papers reporting basic advances in the computing sciences. It is considered the publication of record for basic papers.

The Communications of the ACM (monthly) covers topics of immediate interest to the computing profession, news and notices, official reports of the Association, guest editorials on professional problems, discussions of proposed standards, as well as timely technical material.

Computing Reviews (monthly) comprehensively covers the literature on computing and its applications. Selected specialists from the United States and abroad serve as volunteer reviewers to provide critical evaluations of books, technical papers, popular articles, films and video tapes on every aspect of computing.

Computing Surveys (quarterly) is the survey and tutorial journal of the ACM.

The annual ACM conference and the semi-annual AFIPS conference (of which ACM is a major sponsor) offer members opportunities to attend seminars, hear papers being presented, and discuss mutual interests. These national meetings cover the full spectrum from hardware and software to diverse extensions of information processing theory and practice in industry, government, science, and the humanities. Manufacturers' exhibits at national meetings present the newest in computer systems and auxiliary equipment, and offer previews of significant developments.

ACM Regional and Chapter Meetings are held more frequently, responding most flexibly to the immediate professional needs of the computing community.

National Society of Professional Engineers (NSPE)

The National Society of Professional Engineers has grown from the founding group of four societies in 1934 to 54 affiliated state organizations, approximately 500 local chapters, and 67,000 members. The basic requirement for the (top) Member grade is registration as a professional engineer under one of the state registration laws, while other grades include highly qualified but nonregistered graduate engineers, registered surveyors, and students.

NSPE does not cencentrate its interests in any one technical field. From its founding, it has pursued the economic, social. and professional aspects of all engineering. These include programs in the areas of legislative and governmental liaison, employment practices, ethics, public relations, and career guidance and development. Four sections develop and implement special programs in the fields of private practice, government, industry, and education.

The Society's monthly publication is the *Professional Engineer;* it also publishes the *Legislative Bulletin* and a newsletter in each of the fields of private practice, industry, government, and education. These are supplemented by numerous special publications and reports.

The national offices of the NSPE are located in Washington, D.C. There, the Society maintains an effective liaison with Congress and is regularly consulted in the drafting of legislation affecting the engineer. State societies maintain liaison with their state legislatures on legislation affecting engineers. State societies maintain liaison with their state legislatures on legislation affecting engineers.

National Engineer's Week, which has been observed for the past 21 years, is under the general sponsorship of the Society.

American Society for Testing and Materials

This society was started in 1898 as the American Section of the International Association for Testing Materials. Four years later, the 70 members incorporated as an independent American organization: the American Society for Testing Materials. In 1961, the official name was changed to the American Society for Testing *and* Materials, emphasizing that ASTM is vitally concerned with materials in general (not solely in testing) and, more important, that its activities are not limited to materials but include products of all kinds. There are now about 16,500 members.

The Society achieves its objectives essentially through the activities of more than 100 technical committees (and approximately 2500 subcommittees). These are responsible for development of standard specifications and methods of test for materials and for products for both industrial and consumer use.

The Society has conducted investigations and research leading to a better knowledge of the properties of materials and to the development of more than 4200 widely used standards—specifications and methods of testing for materials. These are applicable to design, manufacturing, construction, and maintenance. ASTM provides the focus for U.S. participation in many technical committees of the International Organization for Standardization (ISO), the International Electrotechnical Commission (IEC), and the Pan American Standards Commission (COPANT). In 1964, ASTM embarked on an extensive program of introducing metric units throughout its 30,000 page annual book of ASTM *Standards.* It also published the *ASTM Metric Practice Guide* to assist in making American-to-metric unit conversions.

ASTM issues the *Journal of Materials* as its archival publication, as well as a publication of more general interest: *Materials Research and Standards.* The Society has a program of continuing studies to find ways to speed up the standardization process to meet the needs of the rapid expansion of technical frontiers. New technical and administrative committees are continually being formed. Current committee activities include work on materials for exploration of space, atomic energy, surgical implants, modern housing and construction, highways, heavy industries, and durable consumer goods.

The Society of Vacuum Coaters

This society was organized in 1957 "to provide a common medium of intercommunications for the many and widely separated persons and groups interested in the vacuum coating process." The fields of interest include vacuum deposition of metallic coatings for both decorative and functional purposes, the latter including treatment of optical elements, architectural glass (as a thermal barrier) and thin-film electronic circuits.

Concluding remarks

Membership in a society may be considered an important part of an engineer's professional development; recognition for service to the society or to the related field is a reward he can attain in no other way. The invitation to support . . . the challenge to redirect the professional society of his field cannot be lightly ignored by any engineer who recognizes the dependency of his future career on the future of his professional field.

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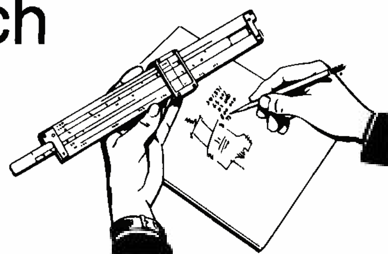
Engineering and Research Notes



Brief Technical Papers of Current Interest

Editor's note: The three Engineering and Research Notes that follow were originally submitted as part of "Laboratories RCA Ltd.—a profile" which appeared in the last issue of the *RCA Engineer* (Vol. 17, No. 2) p. 66. These three notes complete the profile of the Zurich Labs.

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Preparation of single crystals and thin films

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Materials Synthesis and Evaluation Research

Modern electronic systems are making increasing use of single-crystalline solid materials for a wide range of applications. As a result, research laboratories must continue to find new ways to grow existing materials and to apply known methods to the fabrication of new, electronically-interesting compounds.

An example of the latter is the growth of crystals by vapor-phase transport in a closed system. It applies especially well to the investigation of ternary and quaternary compounds which either melt incongruently or have very high vapor pressures at their melting points. (e.g. $HgCr_2Se_4$ or $CdIn_2S_4$). In this method, the component compounds of the desired material are loaded into one end of a sealed and evacuated quartz ampoule together with a small amount of a halogen (e.g. Cl_2 or Br_2). The ampoule is placed in a furnace with a temperature gradient where a reaction occurs between the halogen and the starting material. The resulting volatile compounds "transport" the starting components to the other end of the ampoule where they can be made to back-react forming single crystals of the desired material. The enthalpy change for such reactions is usually positive, meaning that transport occurs from the hotter to the cooler end of the ampoule.

In this manner, we have succeeded in preparing a large number of sulfides, selenides and oxides in single crystal form for the first time.[1] Table I lists some properties of a small selection of materials grown by this method at the Zurich Laboratory during the past few years.

The method is well illustrated by the preparation of $CdIn_2S_4$ crystals. The starting materials are a stoichiometric mixture of CdS and In_2S_3 with a a small amount of I_2 as the transport agent. The ampoule (16-mm diameter, 100 to 200-mm long) is placed in a furnace so that the end with the starting materials is at 850°C. The crystals grow as octahedra at the other end, which is at 750°C.

As the crystals grow more-or-less freely and nucleation is poorly controlled, the above technique is not well suited to the production of crystals of a specified size, shape, or doping. The growth of epitaxial layers on single-crystalline substrates, for example, is better done by vapor-phase transport in an open system. This method, originally developed at the Princeton Laboratories, has recently been applied in Zurich to the preparation of GaP and CdS layers. Its main advantage is that the rate of growth and the doping can be externally controlled.

Table I—Materials grown by vapor-phase transport in a closed system.

Compound	*Crystal shape*	*Max. dimensions (mm)*	*Properties*
β-ZnS (cubic)	Pyramid	13 x 13	Electrooptic
GaP	Boule	7 x 30	Electroluminescent
$ZnTe$	Boule	12 x 33	Electroluminescent
ZnO	Platelets	2 x 8 x 2	Electrophotographic
$MgNb_2O_6$	Prisms	5 x 2 x 1	Large dielectric constant
$CdIn_2S_4$	Octahedra	8 x 8 x 8	Photoconducting
Cu_3TaSe_4	Plates	5 x 5 x 2	Electrooptic
$HgCr_2Se_4$	Octahedra	3 x 3 x 4	Ferromagnetic-semiconductor
$CdCr_2S_4$	Octahedra	3 x 3 x 4	Ferromagnetic-semiconductor

GaP is prepared in the following way. A gas stream of H_2/HCl reacts with molten Ga at 850°C forming the volatile compound $GaCl$. This subsequently reacts with a separate stream of phosphine (PH_3) diluted in hydrogen in a second furnace resulting in GaP. Under suitable reaction conditions, the GaP can be made to grow as a single-crystalline layer on a properly prepared substrate. By premixing the PH_3/H_2 stream with other gaseous hydrides one can introduce dopants (e.g. H_2S) during growth. Although these layers have excellent electrical properties, they yield poor electroluminescent diodes.

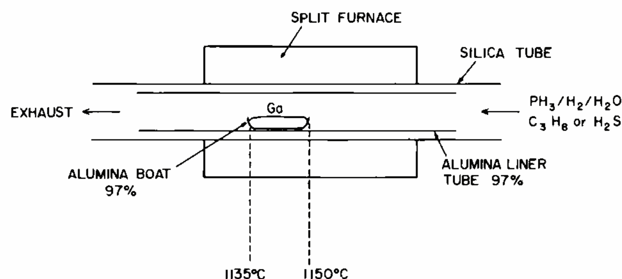

Fig. 1—Schematic representation of the growth of GaP from Ga solution.

The investigation of photoluminescence in GaP requires material with either very high purity or a specified low doping concentration. In addition, the crystals must be free from internal strain. These requirements are best met by growing from Ga solution in the apparatus shown schematically in Fig. 1. The reaction tube and the boat are made of aluminum oxide because it has been shown that the use of quartz leads to an undesired Si doping of the crystals. A gas stream of $H_2/H_2O/PH_3$ is passed over the molten Ga which is at 1150°C. The PH_3 decomposes at this temparture and the phosphrous reacts with the Ga to form GaP. Once the solution becomes saturated with GaP, the compound begins to crystallize in platelet form at the cooler end of the boat.

It is often not possible to use halogen transport as in the two above techniques either because the metal halogenides react with the quartz (e.g., $AlCl$) or because undesired doping of the crystals by the transport agent will result (e.g., I_2 in CdS). In such cases, volatile organometallic compounds can serve as the source of the metal. As before, a vapor-phase reaction with another gas at elevated temperature can be used to produce the desired compound. We have recently grown thin layers of epitaxial AlP on sapphire at 750°C by reacting Aluminumtrimethyl ($Al(CH_3)_3$) with PH_3. The growth of ternary oxides by the same technique is currently under investigation.

Sputtering offers the possibility of preparing thin films of an almost unlimited number of elements and compounds. Sputtering is very similar to the vacuum evaporation process except

that the source material is not heated but rather bombarded with energetic ions. As a rule of thumb, this energy must be at least four times the sublimation energy of the substance, which means about 100 eV. The arriving ions knock out particles of atomic dimensions from the target which cross the chamber and are deposited as a thin film on the substrate. The bombarding ions, in practice usually argon, are created in a glow discharge at a pressure of about 0.01 torr. While metals and semiconductors can be sputtered in a DC discharge, insulators require an RF discharge. If this is not done, a charge layer forms immediately on top of the insulator and sputtering is stopped. When oxygen is substituted for argon as the ion source, it is possible to make metallic oxides directly by using a target of the desired metal. Using this method of reactive sputtering, we have been able to prepare thin films of ZnO which are very good piezoelectric transducers. They also show interesting electrophotographic properties.

For practical applications, crystals with a size of the order of centimeters are often desirable. Such single crystals of metals, semiconductors, and insulators can often be grown from the melt by pulling (Czochralsky method). This method requires that the vapor pressure of the compound at the melting point is not excessive and that the melt does not react with the crucible. The growth starts either on a rod or on a seed (i.e., a small crystal) which is dipped into the melt. The crystal is then slowly pulled out from the melt while rotating at a constant speed. For *Si*, typical pulling rates are 40mm/h. Oxides must be pulled considerably slower, of the order of a few mm/h. The diameter of the growing boule can be changed during growth by slight temperature variations. We are currently growing $Bi_4Si_3O_{12}$ (Eulitine) and isomorphous materials. The crystal growth of such SiO_2-rich compounds is rather difficult because of the glassy nature of the melt. We have been able to grow $Bi_4Ge_3O_{12}$ crystals with a length of a few centimeters as well as smaller ones of the *Si* isomorph. The electro-optic and acoustic properties of these materials are currently under investigation.

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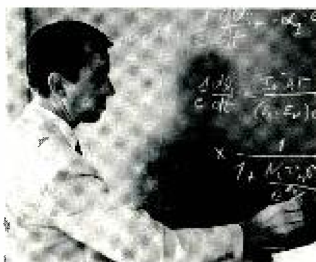
Electrophotography



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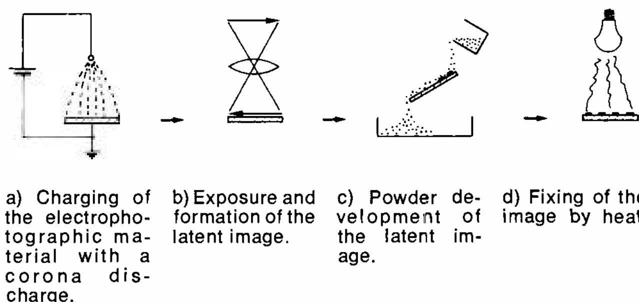
In electrophotography a combination of static electricity and photoconductivity is used to produce images, prints, and copies. In contrast to conventional photography in which chemical processes dominate, electrophotographic images are formed through purely physical means. Thus, electrophotography has becomes important in applications, such as office copiers, where fast reproduction is required. The conventional technique is still overwhelmingly preferred in those cases where high light sensitivity and long lifetime of the latent image are necessary. (The sensitivity of sliver halide films is 100 to 1000 times greater than that of present electrophotographic media.)

The most common materials used in electrophotography are ZnO powder and amorphous *Se* films. The former is generally dispersed in an organic binder and applied as a thin ($\sim 15 \mu m$) layer on a paper substrate. When ZnO is used as the photosensitive material the process is known as Electrofax.



a) Charging of the electrophotographic material with a corona discharge. b) Exposure and formation of the latent image. c) Powder development of the latent image. d) Fixing of the image by heat.

Fig. 1—Schematic representation of the steps in electrophotography.

For simplicity, the steps of the process will be discussed in a one dimensional representation (see Fig. 1). The ZnO layer is charged in the dark by a corona discharge. Such a discharge occurs in a gas around surfaces of very small radius, at which the electric field is so high that the surrounding gas molecules are ionized by impact. The resulting ions are deposited on the photosensitive medium. Under subsequent illumination, the charge in the exposed areas is removed due to the photoconducting properties of the electrophotographic layer. What is left forms an invisible (latent) image which can be developed by strewing a colored powder on the layer. In those cases where the picture is not subsequently transferred to normal paper the powder particles are fixed directly to the layer, as is the case for the ZnO-binder types.

The requirements on the electrophotographic material are not very restrictive in principle: it must be sufficiently insulating in the dark so that it can be charged electrostaticly, and it must be photoconducting so that the charge can be dissipated under illumination. In practice, however, the production of highly sensitive electrophotographic layers is a serious problem. Therefore it appears desireable to clarify the charging properties of and charge transport mechanisms in these layers.

Since the Electrofax layers are a mixture of the inorganic ZnO and the organic binder, a clear assignment of the respective roles is difficult. To complicate matters further, commercial layers usually include a dye to increase the sensitivity in the visible. It was known that ZnO is a photoconductor and that the binder itself is a very good insulator. One could then ask if perhaps the charge were stored on the binder and if the ZnO simply played the role of a photoconductive dissipator.

It seemed obvious that measurements on ZnO alone should give the answer. We found that, while the ZnO powder could not be charged, single crystals could be charged easily in a corona discharge. More surprising was the finding that conducting ZnO crystals stored the charge longer than insulating ones. The fact that conducting crystals can be charged at all indicated that an insulating barrier of 0.1 to 1 μm thickness is formed during the charging process, the resistivity of which is comparable to that of the best insulators.

To bridge the gap between the nearly ideal ZnO single crystals and the powder layers (without binder), polycrystalline layers produced by reactive RF-sputtering were investigated. In contrast to the powder layers, the crystallites in the sputtered layers are closely packed. Since the electrophotographic process could be performed on this material, it seems justified to assume that the binder is not needed to store the charge. Rather it serves to bring the ZnO particles into mutual contact and protects them from detrimental effects of the environment. By its simple presence, of course, the binder can affect the charging and discharging characteristic greatly depending on its specific electron acceptor density.

It was considered justified to study the basic phenomenon of

electrophotography on *ZnO* single crystals alone. The simplicity of this system in comparison to the powder-binder layers should alleviate the difficulties of experimental interpretation. The two examples which follow indicate how such experiments lead to a better physical understanding of the process. In their present mode of use, the Electrofax layers are physically limited in their sensitivity. However, the theoretical analysis omitted one possibility which could, in principle, increase the sensitivity: the multiplication of the photoelectrically generated charge carriers by impact ionization. A model investigation was carried out using *ZnO* single crystals in contact with an electrolyte which showed that the effect cannot be observed in *ZnO*. Such an experiment would be impossible with powder-binder layers.

It is also of interest to know which physical processes are responsible for the decay of the charge pattern which forms the latent image. Experiments on crystals show that, in the dark, the charge is dissipated according to a logarithmic time law, as is also observed for Electrofax layers. The results obtained on the single crystals indicated that the energy of the negative charges on the *ZnO* surface is characterized by a continuum of surface states. It was also found that the pretreatment of the crystals is a decisive factor in determining the decay time, i.e. the density and the position of the charges depend strongly on the quality of the crystal surface.

Future investigations are aimed at clarifying the details of the charge decay mechanisms and at finding where and how the ions from the corona discharge are sorbed on the surface.

Thyristor horizontal deflection and high-voltage circuits for dual-standard 819/625-line television

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Horizontal deflection circuits capable of operating at two different line-frequencies are still required in certain parts of Europe—notably in France and surrounding regions. For wide-angle color kinescopes this imposes severe conditions on the active devices. Operation on the 819- and 625-line standards adds the further requirement of short retrace time since horizontal blanking in the 819-line system has a duration of only 9.8 μs.

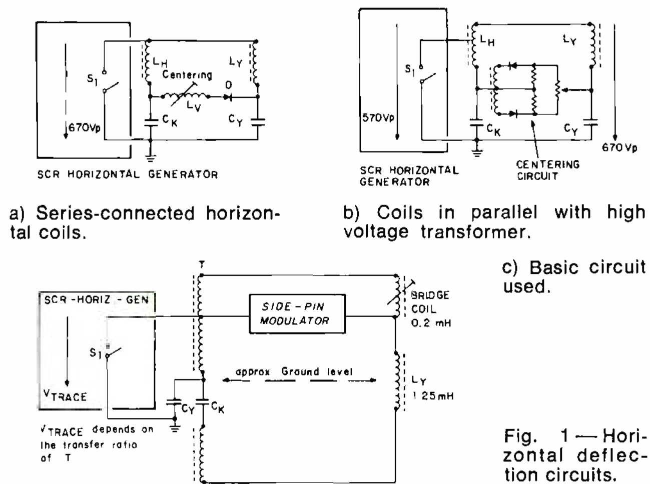
Circuit design

Two types of circuit designs are considered: a) horizontal deflection coils having an impedance of 1.25 mH when series-connected or b) those having an impedance of 0.31 mH, parallel connected.

Basic circuits of this types are shown in Figs. 1a and 1b. There are several proposals for horizontal picture centering and E-W pincushion correction circuits that can be applied in these cases. A centering circuit is outlined in Fig. 1a (L_V, D). A further possibility is shown in principle in Fig. 1b. All the known types of linearity correction circuit are also usable here:

1) Saturable inductor in series with the yoke.
2) Addition of a phase-shifted sinewave to the voltage on the S-correction capacitor.
3) Diode-switched saturable inductor.

In case a), where the horizontal coils are series-connected, the impedance can be matched via the primary of the high voltage



a) Series-connected horizontal coils.

b) Coils in parallel with high voltage transformer.

c) Basic circuit used.

Fig. 1 — Horizontal deflection circuits.

transformer. In this case, any desired retrace voltage on the trace switch can be obtained by suitable choice of the transformation ratio. Since the deflection energy, which is essentially reactive, must be handled by the transformer primary, a somewhat larger core size is required. The usual color receiver core size U 59/36 is used here. The basic circuit is shown in Fig. 1c. The same picture-centering and linearity correction circuits as indicated above for case b) can be employed.

In case b) the coils can be driven directly with the high voltage transformer in parallel. The transformer then only handles the high-voltage power; thus, a small ferrite core as typically used in monochrome receivers is adequate. At nominal deflection current and 11.8 μs retrace time, the peak retrace voltage is then 670 V.

To reduce this retrace voltage, the trace switch can be connected to a tap on the high voltage transformer primary. The usual monochrome transformer core (UI 57) is then still usable for peak voltages down to some 570 V.

In both circuits, the regulation in respect of power-line voltage variations can be improved by feeding information on B+ variations directly to the control circuit via resistive feedback. If the loop gain of the system is sufficient, however, this resistance should be omitted since in certain conditions it can cause oscillations in the control system.

Circuit version a) has the advantage that the retrace voltage pulses at the yoke are practically symmetrical relative to ground. This is due to the high ratio between the two arms (ratio of inductances in the two bridge-arms is 1.25 : 0.2 mH, or 6.2 : 1) of the bridge circuit in the active E-W pincushion modulator. In consequence of the symmetrical yoke voltages, spurious radiation of horizontal frequency harmonics from the yoke is practically negligible.

For both cases a) and b), there is the further possibility of operation with a stabilized B+ supply. The regulation transformer and control system can then be eliminated from the deflection circuit. Stability against beam current variations is then obtained by an optimized use of the principle of retrace-time variation in function of high-voltage load, which is always present in the thyristor deflection circuit.

When using a stabilized B+ supply, the voltage can again lie within the range of about 140 to 300 V. Since in this case the effects of hum are not attenuated in the deflection system, the peak-to-peak hum-voltage should not exceed 0.8% of V_B, as is usual in all-solid-state deflection circuits. The total power consumption will be somewhat reduced since the losses of the regulation system are eliminated.

E-W pincushion correction circuit

The thyristor deflection system allows any of the well-known pincushion correction circuits to be used. Some very simple

circuits give good results and can only be employed successfully with thyristor deflection because of the low internal impedance and the built-in regulation system. This refers particularly to circuits 1) and 2) below. The following four circuits have been investigated.

1) Pincushion correction via the regulation transductor. This modulates the primary voltage of the high-voltage transformer, but provides a very economical circuit.
2) Correction with a single pincushion transductor. This has the the advantage that the primary voltage is not modulated, it is still a simple and economical circuit that provides good quality correction.
3) Correction by means of the "diode modulator" system, which essentially provides linear modulation of the deflection current, but imposes a constant load of at least 18 W on the deflection output stage. The thyristor circuit will tolerate this additional load, and the power can be used to provide the B+ supply for other parts of the receiver. The diode modulator also produces no undesired modulation of the primary voltage.
4) Correction by means of an active deflection current modulator. This system will now be described in detail. It is easily switched between 625 and 819-lines and also produces no modulation of the primary voltage.

This active correction circuit—4) above—uses a bridge configuration to avoid modulation of the high-voltage transformer primary voltage. In the design of the bridge, attention should be paid to the following points:

1) The pulse voltages at opposite ends of the yoke should not be too unsymmetrical, as this can increase spurious radiation.
2) In case of bridge unbalance due, for example, to core-saturation occurring in one arm during picture tube arcing, the unbalanced voltages at either of the arms containing the generators (main deflection generator and pincushion generator) should not be too great.
3) The maximum permissible voltage between horizontal and vertical windings of the yoke (700 V peak-to-peak) must not be exceeded.

These conditions are fulfilled by the bridge shown in Fig. 2c, which has a high ratio (6.6) between arms. The voltages on the horizontal coils have +650 V and −680 V peak values, and are therefore nearly symmetrical.

The pincushion correction is free of the "moustache effect" or of "corner stretching" (decrease of pincushion correction in the corners of the raster at high beam current). The pincushion current generator adds about 5% to the total deflection current without affecting the high-voltage, and can therefore be used to provide a picture width adjustment. The values of peak current and voltage in the circuit are relatively low so that the safety factors are very generous (factor 2 for voltage and 3 for current). Further, the use of germanium devices ensures low losses because of the short turn-off time and the low forward voltage drop. The power requirements of the pincushion generator, which are supplied entirely by the main deflection circuit, are therefore modest and in consequence up to some 20 W of auxiliary power can still be taken from the high voltage transformer to provide the B+ supply of other parts of the TV receiver.

The modulator circuit is entirely immune to damage from picture tube arcing. A "floating" B+ supply derived by rectification of the trace voltage from an insulated winding on the high voltage transformer is used for the pincushion modulator. The entire circuit is isolated from ground, and the input signals are coupled via transformers, which must have adequate instulation between windings.

Switching for dual-standard operation

Dual-standard system requires three switching operations in the output circuit. Since neither high currents or voltages have to be switched, severe requirements are not imposed on the switches or relays. In addition, the oscillator frequency and the S-correction capacitor of the pincushion modulator circuit must also be switched. One further switch section is needed which, during the time that the other switches are completing their functions, must short-circuit the gate of the commutation thyristor to emitter (ground). If a relay is used, contact bounce must be avoided, since the short-circuiting of the gate is necessary to avoid false triggering of the thyristor by spurious oscillator pulses during the other switching operations. It is preferable to arrange that this switch section closes first and opens last by means of a delay circuit. The retrace time is kept the same for both line-frequencies and has a value of approx. 9.6–9.7 μs.

The performance as regards high-voltage regulation, picture-width, change in function of beam current, and other parameters is essentially the same at both frequencies because of the individual set-up for each standard of the commutating frequency and regulator circuit. The gate pulse-shaping circuit for the trace thyristor is not switched since a compromise adjustment that is satisfactory at both frequencies is possible. However, care must be taken to ensure that the gate current becomes negative before the anode current starts to decrease due to application of the commutating pulse in the anode circuit. In Fig. 2 incorrect and correct conditions are shown. Here in both cases, the gate current is correct at 625 lines, but in the upper 819-line waveform it can be seen that a positive gate current of some 60 mA is still flowing when the anode current starts to turn off.

Future trends

The use of the thyristor deflection system also in black and white TV receivers offers interesting technical and economic possibilities, since a single basic circuit can be used in all types of receivers.

Future solid-state bidirectional switches (thyristor plus diode) may be combined into single integrated elements which will offer further economies in assembly, price and inventory.

Although the circuit has now been used very successfully for several years in 90° and 110° color receivers, this work has indicated that variations of the basic system for dual standard operation are possible.

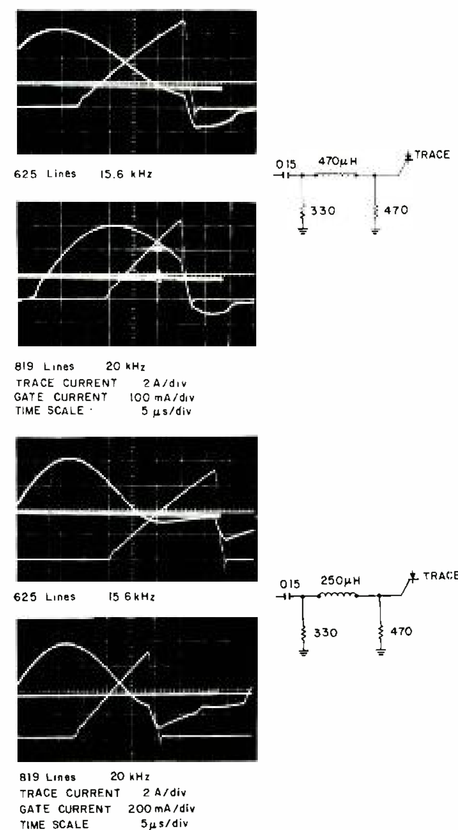


Fig. 2—Correct and incorrect conditions of switching for dual - standard operation.

Editor's note: This Engineering and Research Note is not part of the complement of Zurich Labs Notes.

LCRU optical sight

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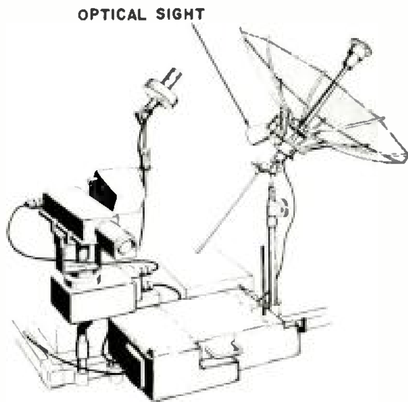


Fig. 1—Optical sight mounted on LCRU antenna.

A unique optical sight was designed under contract with NASA to allow the Lunar Communications Relay Unit (LCRU) antenna to be aligned with earth, as shown in Fig. 1. This sight was developed by Advanced Technology Laboratories in cooperation with both the LCRU program office in Communication Systems Division and the Antenna Pedestal and Structures Group, Radiation Equipment Design Section of the Missile and Surface Radar Division. The sight (Fig. 2) provides a non-inverted image of the earth on a diffusing viewing screen with a reticle to allow accurate alignment of the antenna. A lens cover/filter, which can be moved out of the way easily by a gloved astronaut, protects the lens of the sight from dust, and allows the astronaut to view the sun and thereby align the antenna when the sun is within the central 4° of the field-of-view of the sight.

An *f/10* lens with a 5-in focal length focuses the earth. A butterfly-shaped front-surfaced roof or Amici mirror (Figs. 3 and 4) deflects the line-of-sight by 45° and re-inverts and re-reverts the image from the lens to provide an upright, properly oriented image on the viewing screen. A 3° inner circle on the reticle allows the antenna to be aligned with the earth to within approximately 0.8°. A rotatable sector mask over the viewing screen blocks the image of the sun when it is within the field-of-view but no closer than an angle of 4° to the center of the screen. A retractable sun shield provides shielding of the viewing screen to improve image contrast when back-lighting conditions are present. Baffles at two locations in the sight prevent spurious images from being focused on the viewing screen.

Fig. 2—LCRU optical sight showing viewing screen/reticle and sector mask.

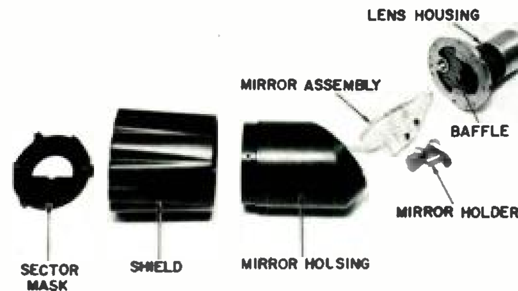


Fig. 3—LCRU optical sight, exploded view.

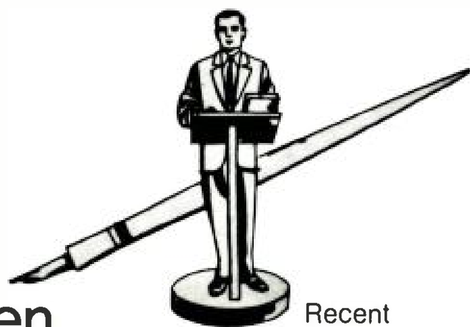
The roof mirror functions the same as a roof or Amici prism, which could not be used because of light scattering. However, this mirror presented construction difficulties because of the requirement to put together two mirrors at a precise angle of 90° (within 5 minutes of arc). The mirror (Fig. 4) is formed of two V-shaped quartz prisms optically joined to within a roofline accuracy of 0.001 in. and held within the sight on Invar supports to match the coefficients of thermal expansion.

The sight is designed to withstand the shock and vibration of launch (in a stowage container) and a skin temperature range of from −73°F to +208°F.

To align the antenna with earth, the dust cover/filter is moved to uncover the lens barrel and the image of the earth is centered in the center circle of the viewing screen/reticle.

Fig. 4—Roof or Amici mirror. This butterfly-shaped, quartz, front-surfaced mirror deflects the line-of-sight by 45° and re-inverts and re-reverts the image from the lens to provide an upright, properly oriented image on the viewing screen.

When the sun is within the central 4° of the field-of-view of the sight, the dust cover/filter is allowed to remain over the lens, and the antenna is aligned so that image of the sun is at a calculated position on the viewing screen/reticle. If the angle between the sun and the earth is greater than approximately 4°, the mask is rotated until the image of the sun is blocked. The dust cover/filter may then be moved to uncover the lens and adjustments made, if necessary, to center the image of the earth in the center circle of the viewing screen/reticle.



Pen and Podium

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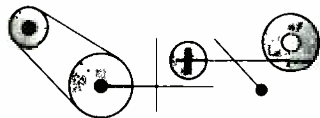

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Method of Constructing a Magnetic Core Memory Plane—T. P. Fulton (EC, Needham Hts.) U.S. Pat. 3,594,897; July 27, 1971

Method for Preparing Zinc and Zinc-Cadmium Sulfide Phosphors—J. S. Martin, Jr. (EC, Lanc) U.S. Pat. 3,595,804; July 27, 1971

Method for Preparing Oxide-Coated Cathodes—J. J. Moscony (EC, Lanc.) U.S. Pat. 3,598,646; August 10, 1971

High Power Electron Discharge Device Having Anode with Improved Heat Dissipation Capability—F. G. Hammersand (EC, Lanc) U.S. Pat. 3,601,647; Augst 24, 1971

Method for Making an Electron-Tube Grid Assembly—I. E. Smith (EC, Lanc.) U.S. Pat. 3,604, 080; September 14, 1971

Flexible Heat Pipe—S. W. Kessler, Jr. (EC, Lanc.) U.S. Pat. 3,604,504; September 14, 1971

Electrical Connector Assembly Having Cooling Capability—R. A. Freggens, W. E. Harbaugh (EC, Lanc.) U.S. Pat. 3,605,-074; September 14, 1971

Radial Heat Flux Transformer—R. J. Buzzard, A. Basiulus (EC, Lanc.) U.S. Pat. 3,603,382; September 9, 1971; Assigned to U.S. Government

Consumer Electronics

Noise-Cancelling Circuits—J. N. Pratt (CE, Indpls) U.S. Pat. 3,595,993; July 27, 1971

Apparatus for Controlling the Operating Potential of a Midicon—J. A. Cooksey (CE, Indpls) U.S. Pat. 3,600,511; August 17, 1971

Noise Immune Pure Carrier Detector Circuit—L. B. Juroff (CE, Indpls) U.S. Pat. 3,602,821; August 31, 1971

Television Electronic Control Circuit for Channel Selections—J. B. Bean, Jr., W. W. Evans (CE, Indpls) U.S. Pat. 3,602,-822; August 31, 1971

Electronic Switching of Tuned Circuits—G. W. Carter (CE, Indpls) U.S. Pat. 3,602,823; August 31, 1971

Instant-On Circuitry for Solid State Television Receivers—J. B. George (CE, Indpls) U.S. Pat. 3,603,732; September 7, 1971

Power Supply Utilizing a Diode and Capacitor Voltage Multiplier for Tracking Focusing and Ultor Voltages—N. W. Hursh, J. J. McCardle (CE, Indpls) U.S. Pat. 3,609,446; September 28, 1971

RCA Laboratories

Optical Semiconductor Device with Glass Dome—A. G. Fischer (Labs, Pr) U.S. Pat. 3,596,136; July 27, 1971

Electro-Optic Light Modulator—J. A. Castellano (Labs, Pr) U.S. Pat 3,597,044; August 3, 1971

Photochromic Image Device—W. Phillips (Labs, Pr) U.S. Pat. 3,598,750; August 10, 1971

Object-Positioning System and Method—L. A. Rempert (Labs, Pr) U.S. Pat. 3,598,978; August 10, 1971

Apparatus Including a Wire Tipped Probe for Testing Semiconductor Wafers—W. L. Oates (Labs, Pr) U.S. Pat. 3,599,093; August 10, 1971

Electrostatic Printing System Employing a Replaceable Cartridge to Provide a Supply of a Recording Element and Processing Means Therefor—M. A. Leedom (Labs, Pr) U.S. Pat. 3,600,083; August 17, 1971

Decade Counter Employing Logic Circuits—R. O. Winder (Labs, Pr) U.S. Pat. 3,600,561; August 17, 1971

High Power Avalanche Diode—S. Liu, J. J. Risko (Labs, Pr) U.S. Pat. 3,600,649; August 17, 1971

Holographic Storage and Retrieval of Information—W. J. Hannan (Labs, Pr) U.S. Pat. 3,601,465; August 24, 1971

Apparatus for Making Annular Holograms—D. L. Greenaway (Labs, Zurich) U.S. Pat. 3,602,570; August 31, 1971

Color Display for Computer Terminal—B. J. Lechner (Labs, Pr) U.S. Pat. 3,603,-962; September 7, 1971

Panel Structure for Matrix Addressed Displays—G. H. Heilmeier, L. A. Zanoni (Labs, Pr) U.S. Pat. 3,603,984; September 7, 1971

Radiation-Sensing Device Comprising an Array of Photodiodes and Switching Devices in a Body of Semiconductor Material—J. M. Assour (Labs, Pr) U.S. Pat. 3,604,987; September 14, 1971

Fluid Variable Light Deflection—G. W. Taylor, P. Goldstein (Labs, Pr) U.S. Pat. 3,606,523; September 20, 1971

Multilayer Circuit Board Techniques—R. J. Ryan (Labs, Pr) U.S. Pat. 3,606,677; September 21, 1971

Light Deflection System—G. W. Taylor (Labs, Pr) U.S. Pat. 3,609,004; September 28, 1971

Binary Light Beam Deflector Using Acoustic Waves—R. D. Lohman, G. A. Alphonse, W. F. Kosonocky (Labs, Pr) U.S. Pat. 3,609,009; September 28, 1971

Electro-Optical Image Forming System—W. J. Howarth (Labs, Pr) U.S. Pat. 3,609,222; September 28, 1971

Pattern Recognizer—I. H. Sublette (Labs, Pr) U.S. Pat. 3,609,687; September 28, 1971

Solid State Division

Phase Shift Circuits—L. A. Harwood (SSD, Som) U.S. Pat. 3,597,639; August 3, 1971

High Current Semiconductor Device Employing a Zinc-Coated Aluminum Substrate—J. Rivera (SSD, Som) U.S. Pat. 3,597,658; August 3, 1971

Protection Circuit Including a Thyristor and a Three Terminal Device—J. M. S. Neilson (SSD, Som) U.S. Pat. 3,600,635; August 17, 1971

Power Transistor—N. W. Brackelmanns, J. Ollendorf (SSD, Som) U.S. Pat. 3,600,-646; August 17, 1971

Radial High Frequency Power Transistor Employing Peripheral Emitter Contact Ring and High Current Base Contact Layer—D. S. Jacobson (SSD, Som) U.S. Pat. 3,602,780; August 31, 1971

Inverter Including Complementary Transistors—W. D. Williams, D. A. Moe, C. R. Turner (SSD, Som) U.S. Pat. 3,602,839; August 31, 1971

Automatic Chroma Control Circuits—L. A. Harwood (SSD, Som) U.S. Pat. 3,604,-842; September 14, 1971

Amplifier Circuits—L. A. Harwood, E. J. Wittmann (SSD, Som) U.S. Pat. 3,604,843; September 14, 1971

Power Transistor Having Ballasted Emitter Fingers Interdigitated—J. Ollendorf, F. P. Jones (SSD, Som) U.S. Pat. 3,609,-460; September 28, 1971

Aerospace Systems Division

Frequency Synthesizer Having a Plurality of Cascaded Phase Locked Loops—A. Orenberg (ASD, Burl) U.S. Pat. 3,600,699; August 17, 1971

Communications Systems Division

Color Television Signal-Generating Apparatus—R. A. Dischert (CSD, Camden) U.S. Pat. 3,601,529; August 24, 1971

Memory System—J. A. Weisbecker (CSD, Camden) U.S. Pat. 3,601,812; August 24, 1971

Color Television Video Signal Processing Apparatus—J. J. O'Toole (CSD, Camden) U.S. Pat. 3,609,224; September 28, 1971

Missile and Surface Radar Division

Keyboard for a Computer or Similar Article—J. T. Kindley (M&SR, Mrstn) U.S. Pat. 3,221,951; September 20, 1971

Elimination of Mode Spikes in Microwave Ferrite Phase Shifters—N. R. Landry (M&SR, Mrstn) U S. Pat. 3,555,460; June, 1971

Constant Velocity Vector Generator—S. A. Raciti (M&SR, Mrstn) U.S. Pat. 3,576,-461; July, 1971

Automatic Impedance Matching Circuits for Variable Frequency Source—W. I. Smith (M&SR, Mrstn) U.S. Pat. 3,581,244; July, 1971

Electromagnetic and Aviation Systems Division

Clock Pulse Generator—L. R. Motisher, E. Engel (EASD, Calif) U.S. Pat. 3,609,-408; September 28, 1971

Constant Time Stroke Generator—R. C. Vandenheuvel (EASD, Calif) U.S. Pat. 3,609,444; September 28, 1971

Dates and Deadlines

As an industry leader, RCA must be well represented in major professional conferences . . . to display its skills and abilities to both commercial and government interests.

How can you and your manager, leader, or chief-engineer do this for RCA?

Plan ahead! Watch these columns every issue for advance notices of upcoming meetings and "calls for papers". Formulate plans at staff meetings—and select pertinent topics to represent you and your group professionally. Every engineer and scientist is urged to scan these columns; call attention of important meetings to your Technical Publications Administrator (TPA) or your manager. Always work closely with your TPA who can help with scheduling and supplement contacts between engineers and professional societies. Inform your TPA whenever you present or publish a paper. These professional accomplishments will be cited in the "Pen and Podium" section of the *RCA Engineer*, as reported by your TPA.

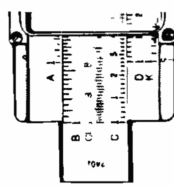
Calls for papers—be sure deadlines are met.

Date	Conference	Location	Sponsors	Deadline Date	Submit	To
MAY 7-11, 1972	**Int'l Quantum Electronics Conference**	Queen Elizabeth Hotel, Montreal, Quebec, Canada	G-ED, G-MTT, AIP, OSA	1-10-72	papers	B. P. Stoicheff, University of Toronto, Toronto, Ontario, Canada
MAY 15-17, 1972	**1972 Electronic Components Conference**	Statler-Hilton Hotel, Washington, D.C.	EIA, IEE	3-1-72	ms	Harold Sobol, Program Chairman ECC, RCA Corporation, David Sarnoff Research Center, Princeton, N.J. 08540
MAY 21-24, 1972	**IEEE Power Engineering Society Tech. Conf. on Underground Transmission**	Pittsburgh Hilton Hotel, Pittsburgh, Penna.	IEEE Power Engrg. Society	1-7-72	papers	E. D. Eich, Anaconda Wire & Cable Co., Hastings-on Hudson, N.Y. 10706
JUNE 19-21, 1972	**International Conference on Communications**	Marriott Motor Hotel, Phila., Penna.	G-ComTech., Phila. Section	1-1-72	ms	A. W. Weinrich, App. Info. Ind., 345 New Albandy Rd., Moorestown, N.J. 08057
JUNE 19-21, 1972	**Int'l Symposium on Fault-Tolerant Computing**	Marriott Hotel, Boston, Mass.	IEEE Computer Soc., MIT	12-1-71	papers	Gernot Metze, Coor. Sci. Lab., Univ. of Ill., Urbana, Ill. 61801
JUNE 26-28, 1972	**AIAA 5th Fluid and Plasma Dynamics Conference**	Boston, Mass.	AIAA	1-7-72	abst	Don Wendling, Director— Technical Programs, AIAA, 1290 Ave. of the Americas, New York, N.Y. 10019
JUNE 26-29, 1972	**Conference on Precision Electromagnetic Measurements**	Nat'l Bur. of Standards, Boulder, Colo.	G-IM, NBS, USNC/URSI	1-15-72	sum	H. S. Boyne, Radio Bldg., Rm. 4075, NBS, Boulder, Colo. 80302
JULY 4-6, 1972	**Conference on Radio Receivers and Associated Systems**	Univ. College of Swansea, South Wales	IERE, IEE, IEEE UKRI Section	11-19-71 2-18-72	syn ms	IERE, 8-9 Bedford Sq., London WC1B 3RG England
JULY 9-14, 1972	**IEEE Power Engineering Society Summer Meeting**	Fairmont Hotel, San Francisco, Calif.	IEEE Power Engineering Society	2-15-72	ms	W. R. Johnson, Pacific Gas & Elec. Co., 245 Market St., Rm. 1122, San Francisco, Calif. 94106
JULY 17-19, 1972	**AIAA/NAVY Advanced Marine Vehicles Meeting**	Annapolis, Md.	AIAA	12-weeks before meeting 6-weeks before meeting	abst ms	Don Wendling, Director— Technical Programs, AIAA, 1290 Ave. of the Americas, New York, N.Y. 10019
AUG. 14-16, 1972	**AIAA Guidance and Control Conference**	Stanford, Calif.	AIAA	12-weeks before meeting 6-weeks before meeting)	abst ms	Don Wendling, Director— Technical Programs, AIAA, 1290 Ave. of the Americas, New York, N.Y. 10019
AUG. 21-26, 1972	**13th International Congress of Theoretical and Applied Mechanics**	Moscow, USSR		3-15-72	sum (5 copies) (500 words)	Professor G. F. Carrier, Pierce Hall, Harvard University, Cambridge, Mass. 02138
SEPT. 4-8, 1972	**International Broadcasting Convention**	Grosvenor House, London, England	IERE, IEE, IEEE UKRI Section et al	1-3-72	syn	The Secretariat, IBC IEE, Savoy Place, London W. C. 2R, OBL, England
SEPT. 10-14, 1972	**Jt. Power Generation Tech. Conference**	Sheraton Boston Hotel Boston, Mass.	IEEE Power Engrg. Soc., ASME, ASCE	4-28-72	ms	General Chairman: G. O. Buffington, Stone & Webster Corp., 225 Franklin St., Boston, Mass. 02107
SEPT. 11-15, 1972	**Conference on Gas Discharges**	London, England	IEE, IEEE UKRI Section, IPPS, IERE	11-22-71	syn	IEE, Savoy Place, London, W. C. 2R, OBL, England
SEPT. 26-29, 1972	**Conf. on Metering, Apparatus and Tariffs for Electricity Supply**	London, England	IEE, IERE, IEEE UKRI Section	3-24-72	syn	IEE, Savoy Place, London, W. C. 2R, OBL, England
OCT. 10-11, 1972	**Conference on Electrical Variable Speed Drives**	Savoy Place, London, England	IEE, IEEE UKRI Section	12-20-71	syn	IEE, Savoy Place, London W. C. 2R, OBL, England

Dates and Deadlines

Dates of upcoming meetings—plan ahead.

Date	Conference	Location	Sponsors	Program Chairman
DEC. 6-7, 1971	**Fall Radio Conference on Broadcast & TV Receivers**	Sheraton-O'Hare Motor Inn, Chicago, Ill.	G-BTR, G-ED	D. W. Ruby, Zenith Radio Corp. 6101 W. Dickens Avenue Chicago, Ill. 60639
DEC. 6-9, 1971	**Ultrasonics Symposium**	Carillon Hotel Miami Beach, Florida	G-SU	Herbert Matthews, Sperry Rand Res. Ctr. 100 N. Rd., Sudbury, Mass. 01776
DEC. 7-8, 1971	**Vehicular Technology Conference**	Sheraton-Cadillac Hotel Detroit, Mich.	G-VT	A. E. Marshall, Ford Motor Co., 23400 Michigan Ave., Dearborn, Mich. 48124
DEC. 7-10, 1971	**Conference on Applications of Simulation**	Waldorf Astoria Hotel, New York, N.Y.	IEEE Computer Soc., G-SMC et al	Joseph Sussman, MIT, 77 Mass. Ave., Rm. 1-131, Cambridge, Mass. 02139
DEC. 10-11, 1971	**AIAA Professional Study Seminar on The Fluid Physics of Pollution (second presentation) conducted by Dr. James A. Fay, Dr. David P. Hoult, and Dr. John B. Heywood, Massachusetts Institute of Technology**	Philadelphia, Pa.	AIAA	AIAA, 1290 Ave. of the Americas, New York, N.Y 10019
DEC. 15-17, 1971	**Decision and Control Conference (Including 10th Symp. on Adaptive Processes)**	Americana of Bal Harbour, Miami Beach, Florida	IEEE Computer Soc., G-IT, G-SMC, Univ. of Florida	S. K. Mitter, MIT, Cambridge, Mass. 02139
DEC. 26-31, 1971	**American Association for Advancement of Science Annual Meeting (2 AIAA Sessions)**	Philadelphia, Pa.	AIAA	AIAA, 1290 Ave. of the Americas, New York, N.Y. 10019
JAN. 17-19, 1972	**AIAA 10th Aerospace Sciences Meeting**	San Diego, Calif.	AIAA	AIAA, 1290 Ave. of the Americas, New York, N.Y. 10019
JAN. 25-27, 1972	**Annual Reliability and Maintainability Symposium**	San Francisco, Calif.	AIAA	AIAA, 1290 Ave. of the Americas, New York, N.Y. 10019
JAN. 25-27, 1972	**Symposium on Reliability**	Sheraton Palace Hotel, San Francisco, Calif.	G-R, ASQC, IES	J. H. Simm, Beckman Inst. Inc., 2200 Wright Ave., Richmond, Calif. 94804
JAN. 30— FEB. 4, 1972	**Power Engrg. Society Winter Meeting**	Statler Hilton Hotel, New York, N.Y.	IEEE Power Engrg. Society	J. W. Bean, AEP Service Corp., 2 Broadway, New York, N.Y. 10004
JAN. 31— FEB. 3, 1972	**Symposium on Information Theory**	Asilomar Hotel, Pacific Grove, Calif.	G-IT	Thomas Kailath, Stanford Univ., Palo Alto, Calif. 94305
FEB. 8-10, 1972	**Aerospace & Elec. Sys. Winter Convention (WINCON)**	Biltmore Hotel, Los Angeles, Calif.	G-AES, L.A. Council	Gerry Goldenstern, L.A. Council Office, 3600 Wilshire Blvd., Los Angeles, Calif. 90010
FEB. 14-15, 1972	**Conference on the Psychology of Technical Communications**	Phila., Penna.	G-EWS	J. C. Phillips, RCA Bldg., 2-8, Front & Cooper Sts., Camden, N.J. 08102
FEB. 14-16, 1972	**AIAA Strategic Offensive/Defensive Missile Systems Meeting**	Monterey, Calif.	AIAA	AIAA, 1290 Ave. of the Americas, New York, N.Y. 10019
FEB. 16-18, 1972	**Int'l Solid State Circuits Conference**	Sheraton Hotel, Univ. of Penna., Phila., Penna.	SSC Council, Phila. Section, Univ. of Penna.	A. V. Brown, T. J. Watson Res. Ctr., Box 218, Yorktown Heights, N.Y. 10598
MARCH 1-3, 1972	**Scintillation & Semiconductor Counter Symposium**	Shoreham Hotel, Washington, D.C.	G-NS, USAEC, NBS	G. L. Miller, Bell Labs., Rm. ID-440, Murray Hill, N.J. 07974
MARCH 9-14, 1972	**Int'l Symposium on High Voltage Technology**	Munich, Germany	IEEE Power Engrg. Society, VDE	Int'l Symp. on High Voltage Tech. Hochspannungsinstitut TU Munchen 8 Munchen 2, ArcisstraBe 21 Germany
MARCH 15-17, 1972	**Zurich Integrated Sys. for Speech, Video & Data Communications**	Fed. Inst. of Tech., Zurich, Switzerland	G-AE, IEEE Computer Soc., Switzerland Sec., SEV et al	A. E. Bachmann, PTT Res. Lab., Speichergasse 6, CH-3000 Bern, Switzerland
MARCH 20-23, 1972	**IEEE INTERNATIONAL CONVENTION (INTERCON)**	Coliseum & N.Y. Hilton Hotel, New York, N.Y.	IEEE	J. H. Schumacher, IEEE Hdqs., 345 E. 47th St., New York, N.Y. 10017
MARCH 21-23, 1972	**Int'l Medium Voltage Earthing Practices**	Inst. of Elec. Engrs., London, England	IEEE, IEEE, UKRI Section et al	IEE Office, Savoy Place, London, W. C. 2R OBL Eng.
MARCH 27-28, 1972	**AIAA Man's Role in Space Conference**	Cocoa Beach, Fla.	AIAA	AIAA, 1290 Ave. of the Americas, New York, N.Y. 10019
MARCH 27-31, 1972	**2nd Symposium on Meteorological Observation and Instrumentation**	San Diego	AIAA	AIAA, 1290 Ave. of the Americas, New York, N.Y. 10019
APRIL 4-6, 1972	**Symp. on Computer-Communications Networks and Teletraffic**	New York, N.Y.	PIB, G-Com Tech., coop. of Computer Society	IEEE Hdqs., 345 E. 47th St., New York, N.Y. 10017
APRIL 16-21, 1972	**11th SMPTE Technical Conference and Equipment Exhibit**	New York Hilton Hotel, New York, N.Y.	SMPTE	Society of Motion Picture and Television Engineers, 9 East 41st Street, New York, N.Y. 10017
MAY 7-12, 1972	**SPSE Annual Conference**	San Francisco Hilton, San Francisco, Calif.	SPSE	Raymond A. Eynard, Public Relations Chairman, SPSE, P.O. Box 2001, Teterboro, N.J. 07608



Engineering News and Highlights

Dr. J. G. Woodward is New President of Audio Engineering Society

Dr. **J. Guy Woodward** was installed as President of the Audio Engineering Society at its 41st Convention in New York. The Society, which is dedicated to advancing scientific knowledge and applications in the field of audio engineering and its allied arts, has a membership of over 5000 in 41 countries.

Dr. Woodward, a Member of the Technical Staff of RCA Laboratories in Princeton, has been engaged in research on electroacoustical and recording systems since joining RCA in 1942.

A Fellow of the Audio Engineering Society, he has served on its Board of Governors and its Editorial Board. In 1968 he was its Eastern Vice President and Chairman of the 35th Convention. In 1970 he was elected Executive Vice President. Dr. Woodward was the recipient of the Society's Emile Berliner Award in 1968 in recognition of his research in electroacoustical devices, musical acoustics. and recording systems. Dr. Woodward is a Fellow of the Acoustical Society of America and the Institute of Electrical and Electronics Engineers.

He was graduated from North Central College, Naperville, Illinois, with the BA in 1936. He received the MS from Michigan State College in 1939, and the PhD in Physics from Ohio State University in 1942.

Alfred Schroeder receives IEEE award for contributions to color television

Alfred C. Schroeder received the 1971 Vladimir K. Zworykin Award of the Institute of Electrical and Electronics Engineers (IEEE) for his "outstanding technical contributions to television and particularly his leadership in the development of color television."

Mr. Schroeder, a Member of the Technical Staff of RCA Laboratories, started his televison research in 1937 when he joined RCA. His work led to the invention in 1946 of the shadow-mask color tube utilized in a vast majority of color television receivers manufactured throughout the world. In all, he has received 65 U.S. Patents for his inventions in television and allied fields.

After finishing high school in Westfield, N.J., he attended the University of Berlin during the 1932-33 school year. He then enrolled in MIT and received the BSEE and MSEE in 1937.

He has been with RCA Laboratories since it was established in Princeton in 1942. He has received six RCA Laboratories Achievement Awards for his television research, and in 1954, he was made a Fellow of the IEEE. The Society of Motion Picture and Television Engineers presented the David Sarnoff Gold Medal to him in 1965 for his contributions to television.

Leverenz elected Life Fellow Member of Franklin Institute

Humbolt W. Leverenz, Staff Vice President and Chairman, Educational Aid Committee, was recently elected to Life Fellow Membership in The Franklin Institute.

Mr. Leverenz was graduated from Stanford University with the BA in Chemistry in 1930. He studied physics and chemistry as an Exchange Fellow of the Institute of International Education at the University of Muenster, Westphalia, Germany, in 1930-31. In 1958, he participated in the Advanced Management Program of Harvard University Graduate School of Business Administration.

Mr. Leverenz joined RCA in 1931 and has held several research and management positions. He was named to his present position in 1968 and was previously Staff Vice President, Research and Business Evaluation, at RCA Laboratories since June, 1966.

Mr. Leverenz pioneered in the development of superior silicate, sulfide, and selenide-type phosphors for kinescopes and fluorescent lamps, and has been issued 67 patents for his inventions, including the cascade luminescent screen for radar indicators.

Mr. Leverenz is a Fellow of the American Physical Society, the Optical Society of America, the Institute of Electrical and Electronics Engineers, the American Association for the Advancement of Science, and the American Institute of Chemists. He is a member of the National Academy of Engineering, the American Chemical Society, the Swiss Physical Society, the American Society for Engineering Education, Sigma Xi, and Phi Lambda Upsilon.

Degrees Granted

B. J. Robbins, SDD, Palm Beach ....MBA in Finance, Florida Atlantic Univ., 8/71
A. D. Gallagher, MPD, Needham ....MSEE, Northeastern Univ., 6/71
D. Espinal, MPD, Needham ....BSEE, Northeastern Univ., 6/71
J. A. Ierardi, MPD, Needham .....BS-Industrial Technology, Northeastern Univ., 6/71

Awards

Missile and Surface Radar Division

The following engineers received Technical Excellence awards for their performance during the second quarter of 1971. They were cited for their contributions as follows:

H. Goodrich developed the basic subsystem and theoretical circuit concepts for the metered-flux phase-shift drivers for the MFAR steerable array radar system. He provided the technical leadership during the critical advanced development phase that led to a successful solid-state integrated subsystem and a basic phase-shift driver technology for steerable array systems.

F. Gorman has been responsible for the thermal analysis of the temperature control system that resulted in analytical proof that the array will be able to operate in a hot or cold environment.

C. Hughes developed advanced computer methods of analysis to define and optimize the non-linear MFAR processor for AEGIS using applicable discrete probability theory instead of the more usual gaussian approximation methods. Through these analyses it has been possible to define accurately the three-step detection matched filter and equipment constraints.

H. Inacker developed monolithic circuits for phase shift drivers on the AEGIS/MFAR program and KREMS proposal, achieving higher reliability simultaneously with a 50% cost reduction.

G. Jacobson led the team that developed a replacement for the AN/FPS-49 radar front end. When the Air Force approved RCA's proposal for an improved version, a contract was awarded to M&SR to design and install the replacement unit on an extremely accelerated basis. A profit incentive of $500/kit/week was established. The team delivered technically superior kits 63 kit-weeks early, enabling M&SR to collect the maximum profit incentive of $30K.

W. Mays designed and built a Laser Range Measurement System (LRMS) for operation with the AN/FPQ-6 Radar at Wallops Island, Va. He also integrated the tracker with the radar. This low-cost design, subsystem checkout, and radar installation effort was unusual because Mr. Mays was the only engineer assigned to the job. He performed his design task based on an earlier system study, and required a minimum of consultation.

G. Ross, in the capacity of Site Team Leader, installed, checked out, and completed work at site on the Coherent Signal Processor for the Point Pillar AN/FPQ-6. Despite the fact that this unit had to be shipped in an untested condition due to the 1970 15-week strike, he corrected all wiring errors, and performed design changes as required. His work was instrumental in obtaining a high degree of performance from this equipment.

R. Tomsic carried forward the advanced development of the MFAR phase shift driver circuits to the point of a demonstrated working model of an advanced steerable array phased antenna subsystem. He advanced the basic system and circuit concepts of a novel flux metered driver circuit through a productizing phase in the form of thirty hybridized working units using advanced microelectronic and hybrid techniques.

Electromagnetic & Aviation Systems Division

F. W. Coble received the Individual Award in the Professional Excellence Program for his outstanding performance on the THOR Timer program. As Program Director, Mr. Coble developed procedures, located and evaluated materials, trained support personnel, and brought the program to a successful conclusion with a favorable gain variance. Impressed by the division's performance on this contract, the USAF is directing all future THOR Timer work to EASD.

The Professional Excellence Program Team Award was presented to the SECANT Hardware Development Team for their outstanding technical contribution to this important program. Under severe schedule restrictions, the team provided technically excellent hardware that allowed flight tests originally scheduled for a two-week duration to be completed in one week. The equipment design proved the validity of the correlation technique theory which is a fundamental concept of the SECANT system, and which has made RCA a viable competitor in the collision-avoidance market.

Aviation Equipment Department

Aubrey W. Vose of the RCA Aviation Equipment Department, Van Nuys, was presented with the Airline Avionics Institute Outstanding Achievement Award for 1971 at the summer general session of the ARINC Airline Electronics Engineering Committee (AEEC) at Kansas City, Mo.

Communications Systems Division

Robert E. Holston of Communications Equipment Engineering, Government Communications Systems, received a Technical Excellence Award for his participation in the LCRU program. Mr. Holston has been the lead mechanical engineer on the Lunar Communications Relay Unit. He participated in the original proposal effort to NASA, supplying concepts for the LCRU design and antenna assemblies which contributed materially to the acceptance of RCA as a contractor for the LCRU. He was responsible for the detailed packaging and structural design of the LCRU to meet the lunar environment and coordinated and directed the mechanical design for the other items of the LCRU subsystems.

Licensed Professional Engineers

When you receive a professional license, send your name, PE number (and state in which registered), RCA division, location, and telephone number to: *RCA Engineer*, Bldg. 2-8, RCA, Camden, N.J. As new inputs are received they will be published.

Consumer Electronics

L. A. Cochran, CE, Indianapolis, Ind. PE-14208; Ind.

J. A. Yongue, CE, Indianapolis. Ind. PE-14201; Ind.

Systems Development Division

W. Rolke, SDD, Marlboro, Mass., PE-24858; Mass.

Astro-Electronics Division

W. Cable, AED, Princeton, N.J., PE-18814; N.J.

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The Acoustoelectric Effects and the Energy Losses by Hot Electrons Part V—Physical Concepts in Energy-Loss Processes . A. Rose

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Static Negative Differential Resistance in Bulk Semiconductors .... F. Sterzer

The *RCA Review* is published quarterly. Copies are available in all RCA libraries. Subscription rates are as follows (rates are discounted 20% for RCA employees):

	DOMESTIC	FOREIGN
1-year	$6.00	$6.40
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3-year	13.50	14.70

Sarnoff reports on third-quarter operations

RCA's continuing operations registered an overall advance during the third quarter of 1971, but an extraordinary charge of $250 million related to the company's withdrawal from the general purpose computer field produced a net loss for the period and for the first nine months of the year, Chairman **Robert W. Sarnoff** has announced.

During the quarter, RCA earnings from continuing operations, exclusive of the extraordinary charge, were $28.5 million, up 52 percent over the strike-affected third quarter of 1970. Sales were a record $872 million compared to $818 million a year ago.

In the first nine months, RCA earnings from continuing operations, exclusive of the extraordinary charge, were $96.7 million, compared to $63.4 million a year earlier. Sales reached a record $2.56 billion, compared to $2.39 billion in 1970.

Losses from operations being discontinued were $9.6 million on revenues of $60 million for the third quarter and $34.5 million on revenues of $182 million for the first nine months of 1971. After inclusion of the extraordinary charge, RCA had a net loss of $231.1 million for the third quarter, and $187.8 million for the first nine months of 1971.

On September 17, Mr. Sarnoff announced RCA's decision to withdraw from the general purpose computer field and to concentrate its computer efforts in specialized data communications systems and in the servicing of computers through an expanding third-party maintenance program.

At that time, he said preliminary estimates indicated there would be an extraordinary one-time charge for 1971 that could reach $250 million after tax, placing RCA in a substantial loss position this year. However, he said no material adverse effects from this action are anticipated in future years.

"In recent weeks," Mr. Sarnoff said, "RCA's management has had preliminary discussions with a number of firms concerning the possible sale of all or parts of our general purpose computer business. These discussions are continuing, and we intend to pursue every possibility in this area.

"At the same time, RCA representatives have met with our computer customers and assured them of our intention to fulfill all contractual commitments to them. A substantial majority of our customers have indicated a desire to continue with their present RCA equipment."

Mr. Sarnoff said plans were being developed rapidly for implementation of the reoriented computer program, which was unanimously endorsed by the RCA Board of Directors on September 17.

"We are moving aggressively to reduce costs in the Computer Systems Division and to assist affected employees in job relocation either within or outside the company" he added. Mr. Sarnoff reaffirmed that "a greatly strengthened" RCA would result from the computer decision.

Turning to other operations, the RCA Chief Executive Office noted a substantial pick-up in color television set sales in the third quarter, as RCA continued its traditional industry leadership. He said there had been good acceptance of RCA's new solid-state color line by distributors and dealers.

Among RCA's subsidiaries, Mr. Sarnoff reported improved operating revenues by Global Communications, the Hertz Corporation, Random House, Banquet Foods, and Coronet Industries.

Electronic Components and RCA Records also showed improved third-quarter sales, as did RCA's government business as a result of billings on previously booked contracts. Current government bookings were also up.

NBC sales were below the same 1970 period, reflecting the loss of cigarette advertising, lagging commitments by major advertisers, and softness in sales at the local station level. Operating results in RCA's solid state business continued to be adversely affected by severe price competition within the industry and by general economic conditions.

EASD develops advanced drum memory system for Navy

A lightweight, high-capacity drum memory system has been developed and qualified to military specifications (MIL-E-5400) by RCA for an advanced antisubmarine-warfare-aircraft development and experimentation program. The system was developed by the Electromagnetic and Aviation Systems Division of G&CS, Van Nuys, Calif., for the U.S. Navy. The drum memory system stores 8.8-million bits of data in one cubic foot of space. It has a data transfer rate of 3.8 MHz and an access time of 9.1 milliseconds. The large storage capability of the small-volume drum results from a unique form of phase modulation pioneered by RCA. The technique reduces error rates while permitting packing densities in excess of 2,000 bits per inch.

Special proprietary design techniques also reduce weight of the drum rotor to approximately two pounds. Along with other construction features, this enables the drum to function in rugged environments associated with airborne, seagoing, and land-based military applications.

Versions of the drum memory system also are being produced for the Army's Tacfire system and the Navy's Message Processing and Distribution System.

New York and Tokyo linked by Datel

International Datel service which permits businessmen in the United States and abroad to exchange computer data on a call-up basis was inaugurated recently between New York and Tokyo. The new service was opened by RCA Global Communications, Inc. in conjunction with Kokusai Denshin Denwa Co., Ltd. (KDD), Japan's international communications carrier. Japan now joins overseas points in Europe, the Pacific, and the Caribbean which use Datel service.

Datel is designed particularly for those businesses which have moderate amounts of data to exchange with computers abroad but which cannot economically utilize a full-time dedicated circuit.

The New York and Tokyo Datel circuit, operating at speeds up to 1200 bits per second, is available around the clock and also offers subscribers other service options when not being used for data communications.

Subscribers pay for Tokyo-bound Datel calls at $4 a minute on a use-basis in one minute increments with a three-minute minimum. The Datel unit comes equipped with a handset that provides voice control when initiating and completing a Datel exchange.

In the United States, RCA Globcom provides direct Datel service for subscribers in the gateway cities of New York, Washington and San Francisco. For users outside the gateway cities, Datel is available to subscribers of Western Union's Broadband Exchange Service who dial RCA numbers and reach their overseas computer destination through the international facilities of RCA Globcom.

RCA to study vehicle-monitoring system for Army

Aerospace Systems Division, Burlington, Mass. has received a $100,000 contract from the U.S. Army to study the feasibility of designing a monitoring system for military vehicles. The study will investigate a cost-effective system with the capability of alerting a driver to such malfunctions as low coolant or oil levels, and carburetor, electrical system, or brake inadequacies.

Under terms of the contract, ASD will provide the Army with a report on selected technical approaches and with demonstration systems installed in Army ¼-ton and 2½-ton trucks.

The eight-month study contract was awarded to RCA by the U.S. Army Tank Automotive Command, Warren, Mich.

Promotions

RCA Service Company

R. M. Haggerty from Installation & Modification Engr. to Mgr., Command Control Stations (W. E. Grundy, Atlantic Fleet Weapons Range—Puerto Rico)

W. R. Slye from Engr. to Ldr., Engineers (J. A. Haik, NASA/STADAN Project Lanham, Maryland)

Government and Commercial Systems

J. S. Griffin from Ldr., Des. & Dev. Engr. to Mgr., Rec. Equip. Projs. (F. D Kell, Recording & Television Equipment, Camden)

Astro-Electronics Division

R. Gottlieb from Adm. Mfg. Sys. Develop. to Mgr., Production & Material Control (M. Sasso, Mfg. Opers., Hightstown)

Staff Announcements

Missile and Surface Radar Division

Dudley M. Cottler, Chief Engineer of RCA's Missile and Surface Radar Division, Moorestown, N.J. has announced the appointment of Dr. **Samuel J. Rabinowitz** as Manager, Systems Engineering.

Astro-Electronics Division

C. S. Constantino, Division Vice President and General Manager of Astro-Electronics Division, Princeton, N.J. has announced the appointment of **John Boning** as Manager, Advanced Programs Requirements.

Aviation Equipment Department

Joseph F. McCaddon, Division Vice President, RCA Aviation Equipment Department, Van Nuys, California has announced the appointment of **Thomas H. Devlin** as Manager, Avionic Systems Engineering.

ATL developing micro-computer

Under a $587,000 contract from NASA, Advanced Technology Laboratories of Government and Commercial Systems is developing a test model of a microprocessor that could be the forerunner of a small, light computer system for use in future manned and unmanned space vehicles such as the Space Shuttle and the Earth Orbiting Space Station.

The heart of the computer will be 15 large-scale integrated (LSI) arrays—one-eighth-inch square chips each containing up to 600 electronic elements. Although the computer will weigh just 10 pounds, occupy one-half cubic foot, and require only 15 watts, it will be capable of processing functions equivalent to room-size commercial computers.

The system, called the Spaceborne Ultra-reliable Modular Computer (SUMC), also can be expanded in segments to meet data processing requirements of a wide variety of space missions during the 1975-85 time period.

The large-scale-integrated CMOS array chips to be used in the SUMC will be designed, manufactured, and tested with RCA's computerized design automation system (see page 10 of this issue). The system makes a possible major savings in time and costs and improvements in reliability.

The SUMC demonstration model will be a 16-bit word length, fixed-point machine. However, expansion capabilities provide for a full 32-bit, floating point design. It will have an operational speed of 100,000 operations-per-second. Semiconductor memories will be employed for micro-program read-only memory and scratch-pad memories.

Beyond its uses in spacecraft, the SUMC also could find wide applications in test equipment, communications, navigation, and other areas of industry and military data processing.

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RCA Engineer

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Eleanor McElwee is TPA for Solid State Division

Eleanor M. McElwee has been appointed Technical Publications Administrator for the Solid State Division at Somerville, N.J. In this capacity, Miss McElwee will be responsible for the review and approval of technical papers; for coordinating the technical reporting program; and for promoting the preparation of papers for the *RCA Engineer* and other journals, both internal and external.

Miss McElwee is presently Manager, Solid-State Power Devices Commercial Engineering, at RCA, Somerville, N.J. She received the BA in English and Mathematics from Ladycliff College, Highland Falls, N.Y., in 1944, and has taken additional courses at the Cooper Union Evening School of Engineering, the Technical Publications Center of Fordham University, and the Graduate School of Business Administration of New York University. She worked for Western Electric as an assistant engineer of manufacture from 1944 to 1947, for Sylvania as a test engineer and technical editor from 1947 to 1951, and has been with RCA since 1951 working on engineering papers, technical manuals, data sheets, and brochures. She is a Senior Member of IEEE, and was one of the organizers of Group on Engineering Writing and Speech (now Professional Communications). She served on the Administrative Committee from 1957 to 1965, and was Secretary from 1957 to 1964 and from 1967 to 1968. She has taught courses in technical report writing and editing at Fordham University and at RCA, and has had several papers published in IEEE and other journals.

Assistance with Patent Disclosures at M&SR

D. M. Cottler, Chief Engineer, Missile and Surface Radar Division, recently announced that one of the programs setup by the Chief Engineer's Technical Excellence Committee (CETEC) will make it easier for M&SR engineers to file Patent Disclosures. Through CETEC, RCA Patent Operations is making available the services of a patent attorney in Moorestown on a regular schedule.

Editorial Representatives

The Editorial Representative in your group is the one you should contact in scheduling technical papers and announcements of your professional activities.

Group / Division	Location
Government and Commercial Systems	
Aerospace Systems Division	Engineering, Burlington, Mass.
Electromagnetic and Aviation Systems Division	Engineering, Van Nuys, Calif. Engineering, Van Nuys, Calif.
Astro-Electronics Division	Engineering, Princeton, N.J. Advanced Development and Research, Princeton, N.J.
Missile & Surface Radar Division	Engineering, Moorestown, N.J.
Government Engineering	Advanced Technology Laboratories, Camden, N.J. Defense Microelectronics, Somerville, N.J. Advanced Technology Laboratories, Camden, N.J. Central Engineering, Camden, N.J.
Government Plans and Systems Development	Engineering Information and Communications, Camden, N.J.
Communications Systems Division	
Commercial Systems	Chairman, Editorial Board, Camden, N.J. Mobile Communications Engineering, Meadow Lands, Pa. Professional Electronic Systems, Burbank, Calif. Studio, Recording, & Scientic Equip. Engineering, Camden, N.J. Broadcast Transmitter & Antenna Eng., Gibbsboro, N.J.
Government Communications Systems	Engineering, Camden, N.J.
Computer Systems	
Systems Development Division	Palm Beach Product Laboratory, Palm Beach Gardens, Fla. Marlboro Product Laboratory, Marlboro, Mass. Systems Programming Product Laboratory, Riverton, N.J.
Data Processing Division	Service Dept., Cherry Hill, N.J.
Magnetic Products Division	Development, Indianapolis, Ind.
Memory Products Division	Engineering, Needham, Mass.
	Graphic Systems, Dayton, N.J.
Research and Engineering	
Laboratories	Research, Princeton, N.J.
Electronic Components	Chairman, Editorial Board, Harrison, N.J.
Entertainment Tube Division	Receiving Tube Operations, Woodbridge, N.J. Receiving Tube Operations, Cincinnati, Ohio Television Picture Tube Operations, Marion, Ind. Television Picture Tube Operations, Lancaster, Pa.
Industrial Tube Division	Industrial Tube Operations, Lancaster, Pa. Microwave Tube Operations, Harrison, N.J.
Solid State Division	Manager, Solid State Power Devices, Somerville, N.J. Solid State Power Device Engrg., Somerville, N.J. Semiconductor and Conversion Tube Operations, Mountaintop, Pa Semiconductor Operations, Findlay, Ohio Solid State Signal Device Engrg., Somerville, N.J.
Consumer Electronics	Chairman, Editorial Board, Indianapolis, Ind. Engineering, Indianapolis, Ind. Radio Engineering, Indianapolis, Ind. Advanced Development, Indianapolis, Ind. Black and White TV Engineering, Indianapolis, Ind. Ceramic Circuits Engineering, Rockville, Ind. Color TV Engineering, Indianapolis, Ind. Engineering, RCA Taiwan Ltd., Taipei, Taiwan
Services	
RCA Service Company	Consumer Products Service Dept., Cherry Hill, N.J. Consumer Products Administration, Cherry Hill, N.J. Tech. Products, Adm. & Tech. Support, Cherry Hill, N.J. Missile Test Project, Cape Kennedy, Fla.
RCA Global Communications, Inc.	RCA Global Communications, Inc., New York, N.Y. RCA Alaska Communications, Inc., Anchorage, Alaska
National Broadcasting Company, Inc.	Staff Eng., New York, N.Y.
RCA Records	Record Eng., Indianapolis, Ind.
RCA International Division	New York, N.Y.
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*** Technical Publication Administrators listed above are responsible for review and approval of papers and presentations.**

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