RCA Engineer

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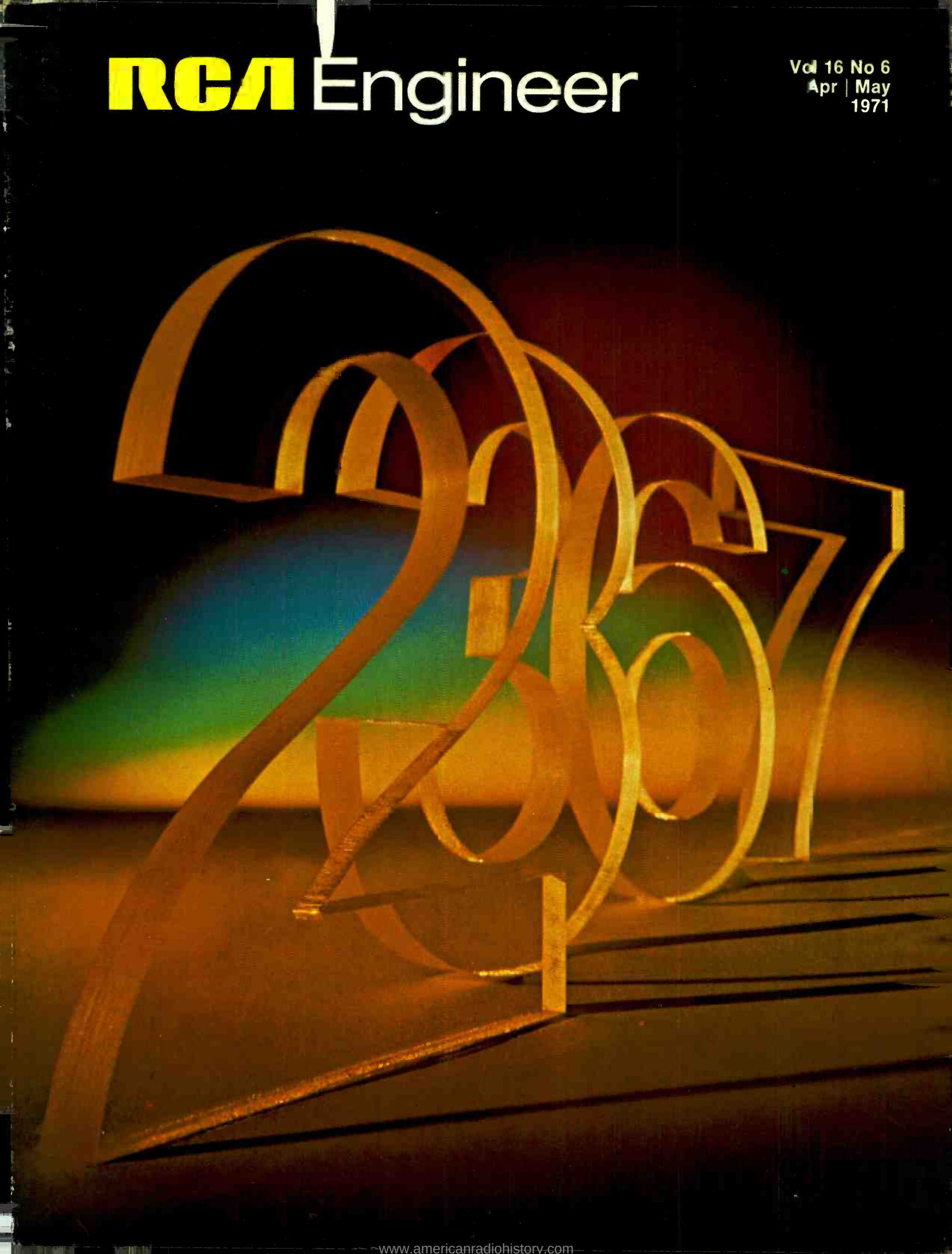

Digital computers come of age

For the last two decades, we have seen a vibrant, moving, almost revolutionary growth and change in the digital computer field. We have progressed through three generations of equipment. RCA's first commercial machines utilized vacuum tubes; then in 1957 we shipped the first commercial all-transistor computer, the RCA 501 System. Again with the RCA Spectra 70 we were first—this time introducing monolithic integrated circuits in business computer systems.

Also, during the past two decades we have witnessed tremendous increases in the speed, power, and capacity of computer systems. Faster speeds and more memory have opened greater opportunities for the development of more sophisticated software, and these two factors have combined to open entire new areas of applications. Dramatic improvements in system reliability have made possible commercial "real-time" communications-oriented systems. RCA is right at home in this field. Last year, RCA booked more sales in communications-oriented systems than ever before.

What does all this mean to the engineer?

Performance and costs that were adequate and even considered good only a few years ago, are completely unacceptable today! Our continued thrust into these sophisticated systems makes our reliability goals a moving target. Reliability at competitive price is the key challenge. You will see this theme reflected in many of the articles in this issue. We intend to remain "the Company easy to do business with" by excellence in engineering from the smallest component to the largest systems. Tops in reliability and performance and a competitive price is our plan for RCA computers.

This all starts with you—the RCA engineer.

H. N. Morris
Manager
Palm Beach Product Laboratory
Computer Systems Division
Palm Beach Gardens, Florida

Our cover

. . . represents RCA's new series of computers —the RCA 2, RCA 3, RCA 6, and RCA 7. The new series offers significant cost/performance improvements over existing RCA models as well as those of the competition. These new computers are described, within the context of RCA's position in the domestic computer market, by L. E. Donegan in this issue (p. 3). **Photo credits:** Joan Dunn (concept), Tom Cook (photography).

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RCA Engineer

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RCA Engineer articles are indexed annually in the April-May Issue and in the "Index to RCA Technical Papers."

• To disseminate to RCA engineers technical information of professional value • To publish in an appropriate manner important technical developments at RCA, and the role of the engineer • To serve as a medium of interchange of technical information between various groups at RCA • To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions • To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field • To provide a convenient means by which the RCA engineer may review his professional work before associates and engineering management • To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

Contents

editorial input

Engineers as Environmentalists

Recently, there has been a great deal of table-thumping and fist-brandishing on the part of angry environmentalists. Unfortunately, their wrath is too-often justifiable. Pollution problems confront us daily with every noise, every drink of water, and every breath of air we take.

In many cases, however, inflated statistics, doomsday publications, and angry invectives have hidden the truth of a situation to the point where rash, stop-gap solutions result in significantly more waste than would have been created if the problem went "unsolved."

DDT, for instance, was a hero of World War II and a villain of the 1960's. Today, it is considered a necessary evil, simply because there is no suitable alternative. Substitute chemicals (developed during DDT's reign as "supreme environmental villain") were often found to be much greater spoilers —some were actually watered down by-products of chemical warfare laboratories.

New York State banned DDT in their state parks, and last year their forests were blighted with tent caterpillars and gypsy moths, causing, in a single summer, the destruction of woodlands that took hundreds of years to grow. At present, there is no proof that DDT is directly harmful to man or most other mammals, but it must eventually be banned—if for no other reason than the existence of reasonable doubt concerning its safety. But we should not counter reasonable doubt with unreasonable action.

And this is where the engineer can render an invaluable service. In the midst of confusion surrounding angry protests, a good measure of analysis and evaluation is necessary to separate fact from fiction, and solution from stop-gap.

Engineers have always played a significant part in the satisfaction of human needs, but today the demands are greater than ever before. In the questions of product safety; privacy for the individual in a computer-oriented society; air, water, and noise pollution; urban poverty and overcrowding; and transportation, technology has become the whipping boy—receiving an inordinate share of blame for problems that have been created and perpetuated by the body politic, some that have been with us for centuries.[1]

However, engineers—as the strong right arm of technology—must be willing to accept a lion's share of the responsibility (for themselves and their predecessors) to turn the situation around.

Engineers are uniquely qualified by education, inclination, and experience to cut through to the heart of a problem, to recommend useful solutions, and to see a task through to completion. The ability to innovate and present new ideas clearly (with full consideration of their consequences) are the forces that engineers can bring to bear on contemporary problems.

We hope that RCA engineers will look upon the *RCA Engineer* as a medium for documenting their ideas and making responsible recommendations. The pages of the *RCA Engineer* are open to your comments, suggestions, and reactions.

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1. For example, urban overcrowding has been a problem for some time:

   "... the crowded tenements of a struggling and restless population differ only from the tents of the Arab or the Gypsy by their less healthy openness to the air of heaven, and less happy choice of their spot of earth, by their sacrifice of liberty without the gain of rest, and of stability without the luxury of change."

   John Ruskin (1849)

Future issues

The next issue, the sixteenth anniversary of the *RCA Engineer*, will contain representative papers from most areas of RCA. Some of the topics to be covered are:

Ceramic circuit developments

COS/MOS integrated circuits

Holographic information storage and retrieval

The inventor and his patent attorney

Piezoelectric device applications

Schottky diodes

Speech bandwidth compression

Central Telex Network Exchange

High impedance interphone amplifier

Discussions of the following themes are planned for future issues

Optics

Solid state technology

Computer peripherals

Displays

Advanced Technology Laboratories

Systems Programming

Semiconductor memories and COS/MOS circuits

L. E. Donegan, Jr., was elected RCA Vice President and General Manager, RCA Computer Systems, by the Board of Directors on January 6, 1971. In this post, he is responsible for the four operating divisions comprising RCA Computer Systems—Data Processing, Systems Development, Memory Products, and Magnetic Products—as well as the Computer Systems Staff group and the Systems Manufacturing Operations organization.

Mr. Donegan joined RCA in January 1969, as Division Vice President, Marketing Operations, for what was then the Information Systems Division. In this capacity he was responsible for all field and home office computer marketing functions.

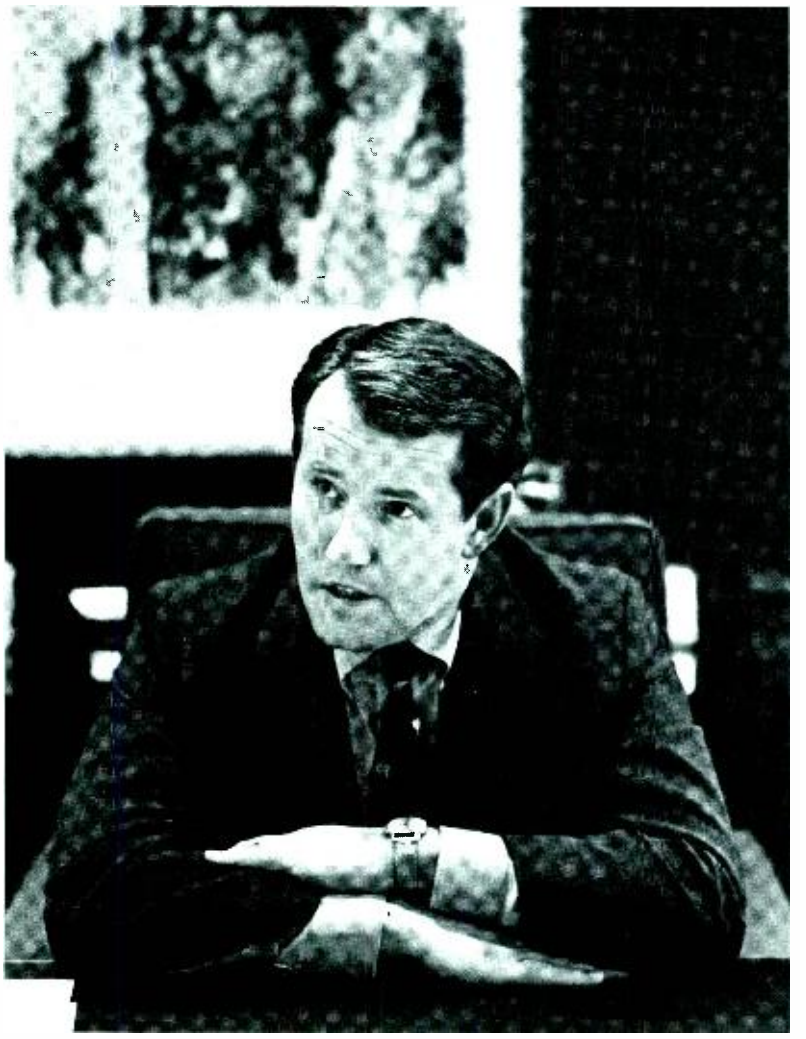
In January 1970, he was appointed Division Vice President and General Manager of the Computer Systems Division in which he directed overall operation of marketing, field engineering, systems programming, product engineering, manufacturing and administrative functions.

A 20-year veteran in data processing and a leading authority in the remote computing field, Mr. Donegan spent 18 years with IBM, serving as Vice President of the Service Bureau Corporation before moving to RCA.

He joined IBM in 1951 as a marketing representative in the Data Processing Division. He later moved up to various staff and managerial positions before being appointed in 1965 as executive assistant to the IBM Group Vice President responsible for IBM's total computer business.

Subsequently, Mr. Donegan was named Director of Information Marketing, responsible for the planning, development and operation of on-line time-shared services. In 1968, he was elected Vice President of the Service Bureau Corporation, a wholly-owned IBM subsidiary.

Mr. Donegan graduated with honors from the University of Nebraska in 1950, and holds the BS in business administration.



The Engineer and the Corporation

RCA and the computer industry in the 70's

L. E. Donegan, Jr.

RCA President Robert W. Sarnoff sees the corporation "poised for the decade of information" as the 70's unfold. For RCA Computer Systems, this means achieving two major goals in a hotly competitive environment marked by new product announcements, merger, and intensive activity across the board. By mid 1970's, RCA is targeted to secure a firm number two place—behind IBM—in the domestic computer market, along with a 10% share of that market.

EXACTLY what do these mandates mean for RCA's computer operations in this new decade? First, to give you an idea of the size of the market, there are approximately $20 billion worth of computer systems installed and operating in the U.S. today. Industry net shipments during 1970 were approximately $3 billion. By 1975, the installed value of domestic shipments will rise to an annual level of $6.4 billion.

This is the size and rate of growth of the industry in which RCA expects to achieve a 10% market share within a relatively few years.

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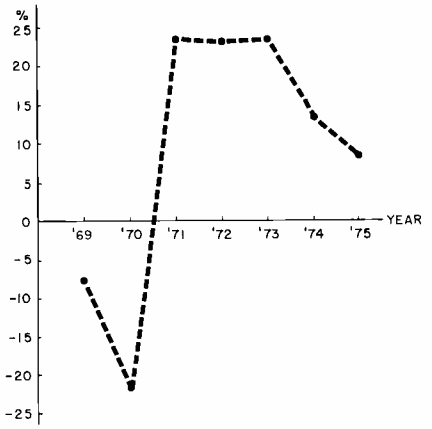


Anticipated annual growth of the domestic computer market. During 1970, industry net shipments were approximately $3 billion; by 1975, the installed value of domestic shipments will rise to an annual level of $6.4 billion.

A look at the order books shows us moving fast down the track toward our objectives. Computer bookings for 1970 have exceeded the same period last year by more than 15%. Also, computer shipments in 1970 were up considerably—more than 55% over the same period last year. Much of this growth stems from a sharp increase in new accounts, or customers coming to RCA for the first time. During 1970, our total of new computer accounts was up almost 300% over the comparable period of 1969.

Marketing strategy

Now what are our strategies for achieving our stated long-range goals? In developing a marketing strategy for the 70's. RCA Computer Systems has worked with outside consultants on a series of in-depth marketing studies. These took into consideration factors which we believed would exert the strongest influence on both manufacturers and users during the decade.

Our studies were predicated on the belief that the industry was mature enough to make predictions truly meaningful, particularly in the area of technology. Today, it is difficult to scoop competition with radical hardware innovations. The constant interchange of technical information, the increase in journals devoted to the computer industry, and the development of professional organizations dealing in information systems concepts, make the computer technology of the 70's highly forecastable. This couldn't be said 10 years ago.

1970's—the decade of the user

The basic conclusion distilled from our studies shows the 70's favoring the user more than ever before. We believe the next 10 years will be marked less by technological breakthroughs than by advances in system design and software, and innovations in the relationship between manufacturers and customers geared towards enabling the computer user to better adapt the technology of the sixties and the new technology of the 70's to meet his particular needs.

Technology

At least 50% of third generation computers are memory bound.

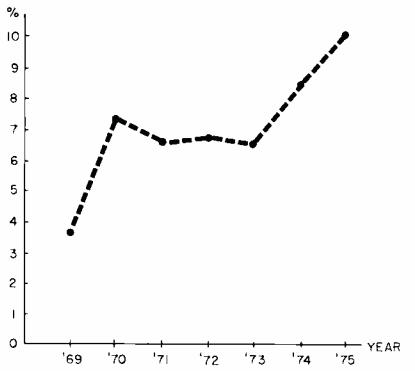
That is not to say that there won't be technological advances. There will, of course. But it is my belief that none of these technological advances will, at least in the early 70's, be as revolutionary as those that took place during the 60's.

Several factors led us to this "decade of the user" conclusion. Based upon our studies, we have developed several key assumptions about the industry's development during the 70's.

First, we are convinced that the so-called "fourth generation" of computers will be evolutionary in nature. The recollection of IBM's introduction of System 360 is painfully fresh for many users. It required them to reprogram virtually all operations to take advantage of the new-found speed and power of these machines. That will not be the case this time around, either on our new machines or on IBM's.

The second basic assumption is that the greatest technical advances will come in memory design and electronics. We foresee a gradual phasing out of ferrite cores in favor of semiconductor electronics, with semiconductors becoming the predominant computer memory elements by 1975. In terms of design, we anticipate a strong trend towards vastly increased memory size and speed. Both are needed to meet user requirements for larger programs as well as for running the computers in several modes simultaneously with many different programs.

Our investigations indicate that at least 50% of existing third generation computers are "saturated." This means



RCA share of the domestic computer market. RCA expects to achieve a 10% share of the domestic computer market within a relatively few years. In 1970, RCA's market share was $202 million.

they employ every available byte of memory to handle normal workloads and are, in effect, memory bound.

Virtual memory—a key route to meet user needs

Of course, the simplest solution to this problem is to increase main memory size. IBM has done this on its new System 370, and we are also offering larger memories with our new systems. However, a relatively new technique gives the user virtually unlimited memory capabilities without increasing main memory size, and consequently the cost of his computer. This technique is called virtual memory. It represents a key route which RCA has taken to meet user needs for larger memories in our new computer series. Incorporating main memory, auxiliary memory (backing store), and operating system software, virtual memory provides users with a large, logical extended memory capable of handling segments of many programs at the same time. As such, it lends itself to extensive multiprogramming, and to concurrent processing of local and remote batch programs and interactive tasks.

Simply put, a virtual memory system is one which automatically, through a combination of hardware and software techniques, allocates program segments to their proper place in either main memory or auxiliary memory in a multi-programmed computer environment.

A virtual memory computer, therefore, automatically breaks programs into segments or pages and dynamically moves these program pages between main memory and auxiliary memory

as they are needed to perform each portion of each computing task.

In this type of system, program segments, or pages, are constantly being swapped back and forth between real memory and auxiliary memory as needed.

Under the virtual memory concept, a computer with a main memory of, say, 262,000 bytes of storage space can be dynamically linked to an auxiliary storage device with as many as eight million bytes of storage space. Since the program pages are being constantly swapped back and forth between the main memory and the auxiliary memory, the user has virtually unlimited memory capacity using this system.

Now what does the virtual memory concept and a virtual memory computing system mean to the user?

To begin with, it represents a tremendous saving in human resources, that is programming time and energy. When programming for a virtual memory system, a programmer has only to write those instructions required to get his job done properly. The computer and its virtual memory operating system automatically allocate program segments to their proper place in either main or auxiliary memory and move them back and forth as needed. Since programming is still one of the major expense items in any data processing operation, simplification of programming tasks has a direct result in greatly reduced programming costs and considerably increased programmer efficiency, both highly desirable from a user's point of view.

A virtual memory system also frequently reduces the user's system costs, because auxiliary memory devices are considerably less costly than main memory. And, since the user has up to eight million bytes of auxiliary memory available in a virtual memory system, he can in most cases get along with a much smaller main memory, with consequent reduction in overall system cost in relation to the amount of work performed.

Additionally, the virtual memory user achieves more efficient utilization of his system, because virtual memory allows him to perform local batch, remote batch, and interactive, time-shared computing at the same time, and with greater efficiency, without concern for memory management.

It is our strong belief that virtual memory systems are the computer operating systems of the future and that by 1975 few computer systems will be on the market that do not offer virtual memory capabilities.

RCA has for several years been a leader in virtual memory systems. Both our Spectra 70 Model 46 and 61 computers utilize the virtual memory concept. The considerable experience gained through the development of these virtual memory systems, plus the enhanced virtual memory capabilities offered on our new series of computers, promise to maintain RCA's position of leadership in this area of advanced computer technology.

Data communications—RCA's strength

Another major trend in the computers of the 70's will be increased communications capabilities. One of the best barometers of expanding computer usage is the increased number of terminals—such as teletypewriters and video displays. A study by RCA shows there were 20,000 terminals of this type in use in 1965. This year there will be 90,000. Five years from now a half million.

RCA has a reputation for leadership in computer-communications. To offer our users a broader, more efficient communications capability, we have developed a front-end communications processor. This small, specialized, digital computer (Model 8660) operates in a bisynchronous mode. It can be used in conjunction with a host main processor to relieve the host of the many housekeeping tasks associated with a complex data communications network.

The 8660 represents an enhancement of our basic model 1600 message switching computer with new software added to meet today's advanced data communications requirements.

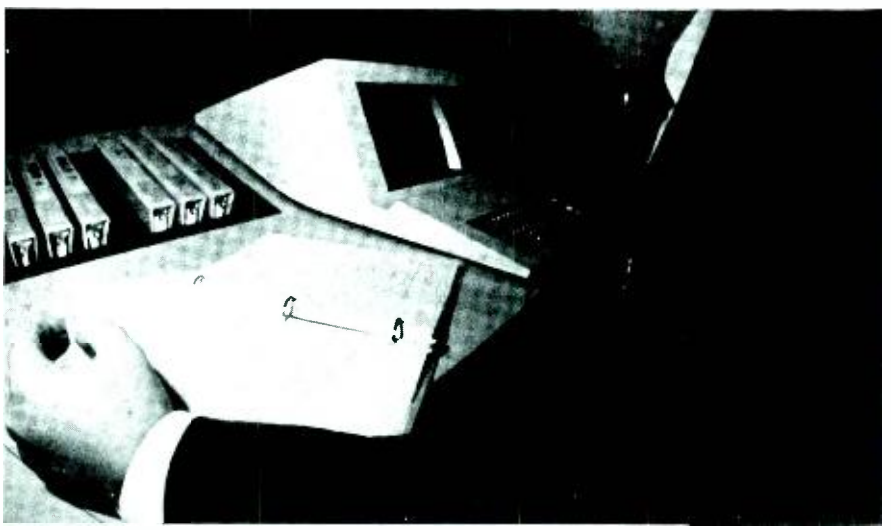
As a result of the introduction of this new front-end communications processor, RCA now offers a total communications interface capability with virtually all types and classes of data communications terminals.

The Model 8660, for instance, interfaces perfectly with the IBM 360/20, which is frequently used as a terminal in large remote computing systems. In addition, it interfaces with the IBM 1130 processor, the IBM 2780 data transmission terminal, the IBM 2701 and 2703 transmission control units for other IBM processors, and the Burroughs TC 500 data terminal.

We are certain that the great flexibility and efficiency of the 8660 will be warmly welcomed by computer users, particularly users of large-scale communications-oriented systems.

High density data storage

Another key area of development in the 70's will be higher speed, higher density data storage units. With growing user pressure for larger data bases and faster methods of data retrieval, no manufacturer wishing to compete in the market of the 70's can content himself with present storage and retrieval methods. That is why we intend to announce in the near future an



RCA high-speed, high-density disc storage system comparable to IBM's 3330, a highlight of the new IBM System 370 series computers.

As you can see, all of the projected technological advances noted above are in response to existing, and clearly defined, user needs. While they will utilize advanced engineering and design techniques, these will not be utilized simply because the technology is there, but because the user requirement is there.

New RCA computer series

Now, let's see how RCA's new computer series is meeting user needs of the 70's and bringing us closer to achieving our business goals.

The new RCA computer series (the RCA 2, RCA 3, RCA 6, and RCA 7) offers significant improvements in cost/performance over our existing models as well as those of competitors. Two (the RCA 3 and the RCA 7) have virtual memory capability not offered by our principal competitor—IBM. All are compatible with RCA and IBM equipment, a vital consideration in any upgrading move.

RCA's new series does not compete with IBM's 370/165, and only to a limited extent with the 370/155. They do compete directly with IBM's 370/145 and 370/135.

Their principal significance is that they offer existing RCA users and IBM 360/30, 40, and 50 users greatly increased memory and power at little, or no, increase in cost. Since these IBM machines constitute more than 50% of all installed third-generation computers, RCA is addressing a broad segment of an important market.

Compatibility

Compatibility is an especially important feature in attracting new customers and extending our base. Back in 1964, RCA wisely decided to model its instruction set after IBM's. Today, programs written for IBM's 360 computers have the same basic 134 instructions as those written for RCA's Spectra 70 family and the new product line series.

Emulation

We are also strong in emulation. Each of the new computers can be optionally equipped with emulators for comparable RCA or IBM second generation computers, such as IBM 1401, 1440 and 1460, and RCA 501 and 301 systems. Thus, either through direct program compatibility or emulation, almost any RCA or IBM second or third generation program can be run on the new RCA computer series.

Standard memory modules

As I have said earlier, greater memory size and speed—along with lower cost—are among the most important features of the new RCA computers. One of the major reasons we can offer our customers these memory improvements is because we have developed standardized memory modules—a feature unique in the industry.

Because they are standardized, RCA memories are now easily expandable, switchable from processor to processor, and interchangeable with two or more processors. The flexibility of modularized memories is especially important in multi-system installations for gaining maximum throughput and enhanced cost/performance. Also, switchable memories are vital in on-line installations where backup is required. No longer is it necessary to provide identical backup systems. Thus, a data center with two 360/50's back-to-back can function perfectly with either RCA 2's and 3's backing up either RCA 6's and RCA 7's at considerable reduction in overall system cost.

Virtual memory

In addition to standardized main memory modules, we also offer users virtual memory capabilities on our RCA 3 and RCA 7. It is important to note, in this connection, that RCA virtual memory technology—especially in the area of operating system software—continues to lead the competition.

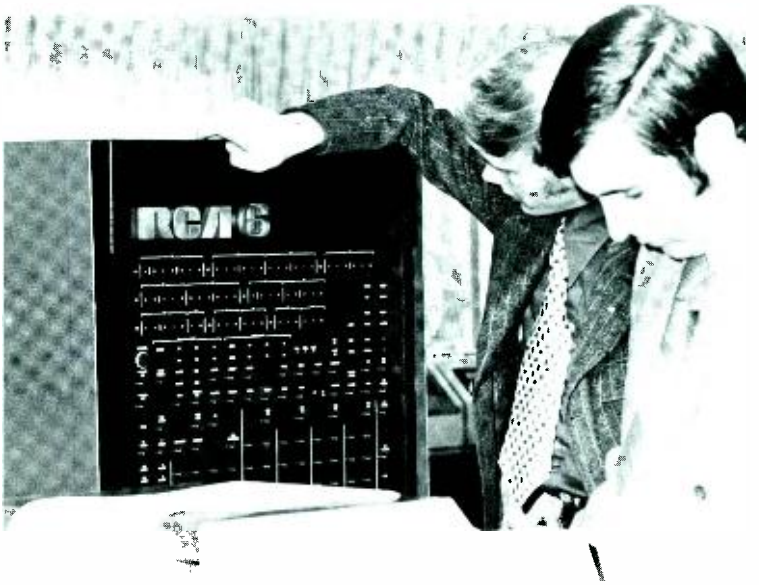
We believe that a very large number of computer users would rather have virtual memory, with all the added capabilities and reduced programming costs it brings them, than an unnecessary leap in processor power.

To sum up, we have designed our new computer series with the customer's real information requirements in mind—as well as his pocketbook—as the decade of the 70's begins.

Customer anxiety in the computer purchase decision

As part of the marketing study already discussed, we asked the Arthur D. Little organization to analyze the computer purchase decision process for us. One of the words that occurred most frequently was *anxiety*—in this case customer anxiety. The net impact of these anxieties is that subjective criteria turn out to be the determining factors in the computer decision-making process once the field of competitors has been reduced to two or three vendors.

This is totally contrary to the conventional view of this process, which has



held that it was essentially objective. For this reason, we feel it extremely important to understand and deal with these anxieties.

What are these anxieties that play such an important role in the computer selection process, and what is RCA doing about them?

The first anxiety is the users' fear of losing that which is known, in terms of hardware, software, and people. It takes a long time to get used to a computer, and once acquainted with it and comfortable with its operation, it is hard to get people changed.

The second anxiety is that in the event of a massive systems failure, a vendor other than IBM might not be able to mount a successful rescue operation. All but the most powerful and sophisticated users have this fear.

The third anxiety—one also experienced by all but the largest organizations—is that because of limited internal resources the user will not be able to handle the changeover to a new vendor system.

The fourth anxiety is the fear that there may be a "hidden" flaw in the system. Even after an objective evaluation indicates that a non-IBM computer is superior, many users still do not believe their own eyes and their own evaluations.

And the final anxiety is that if IBM is not chosen, and the system runs into trouble, those who made the decision can expect reprisals from top management for not doing the "safe and sure" thing.

While these anxieties exist in varying degrees in varying situations, and may not exist at all in others, our research indicates that they are all too important in the decision-making process to be ignored.

Guaranteed conversion

RCA took a major step towards alleviating the anxiety problem when we introduced our new RCA computer series last year by announcing our unique "guaranted conversion" policy. I am convinced that it represents one of the most significant business innovations in the history of the computer industry from the user's point of view, and that it will have a major effect on the industry during this decade.

Representing a dramatic change in the traditional user-manufacturer relationship, "guaranteed conversion" offers qualifying purchasers or leasers of RCA 2, RCA 3, RCA 6, RCA 7 computer systems the opportunity to enter into a contract with RCA guaranteeing that their existing system programs will operate on the new RCA computers by a specific date—and, if desired, within mutually agreed upon performance specifications.

Based upon mutually agreed upon specifications, terms, and conditions, RCA and the customer agree on a fair price for this conversion service. From that point on, it is RCA's responsibility to complete the conversion. In the event that RCA does not substantially complete the conversion as specified, the corporation will pay liquidated damages for each day's delay.

Under this new policy, we are offering qualified customers two types of conversion contracts: 1) A guaranteed conversion contract that provides for conversion of a defined number and class of programs within a determined period of time, or 2) A guaranteed conversion/performance contract that additionally provides that converted programs will operate within defined performance parameters.

Since this represents a totally new concept, we have initially limited these contracts to present IBM 360/30, 40 and 50 installations. However, this still represents more than 50% of existing IBM System/360 computer installations, and therefore a significant portion of the overall market.

What does "guaranteed conversion" mean to the customer? Other manufacturers have for many years offered a wide variety of aids to assist their customers in converting over from competitor's systems or from one generation of computers to another. However, the significant difference between RCA's guaranteed conversion policy and traditional conversion arrangements is that up until now no manufacturer has offered customers contractual guarantees of successful conversion, and attached specific financial penalties to fulfill these obligations. In addition to being a powerful tool for expanding RCA's customer base, "guaranteed conversion" is designed as a profitable business venture. It also represents the first time in the history of the computer industry that users can know exactly what their program conversion costs will be when moving up from one system to another before signing their lease or purchase contracts.

In effect, with RCA's guaranteed conversion options, qualified computer customers now have an "insurance policy" for successful conversion from their systems to an RCA system much stronger than IBM previously offered them with bundled computers.

We are convinced that these new contract options will go a long way towards alleviating the anxieties of existing IBM customers in doing business with RCA. By minimizing risks in the computer decision-making process, we have taken a step which I am certain all computer users will strongly welcome.

Concluding remarks

Again, let me review the steps we've taken to meet the objectives of second place position in the domestic computer market and a 10% share of market by the mid-70's.

First, we have announced a new series of computers offering enhanced technical features and highly competitive cost/performance ratios. The RCA 2, RCA 3, RCA 6 and RCA 7 provide a logical and desirable upgrading path for many users, especially those with IBM 360/30, 40 and 50 systems.

Second, with guaranteed conversion RCA has made a concentrated effort to allay subjective user anxieties and insure IBM customers against risks in changing to our new series of computers.

We believe that the new computers, in conjunction with other recent business policies and guaranteed conversion, represent major landmarks in answering the users' real information needs during the decade of the 70's. With these tools we believe we can capture an increasing share of IBM customers, and thus achieve, and perhaps even exceed, the goals we have set for ourselves.

A new look at semiconductor cooling packages

J. Chisholm

This article describes a forced-air cooler for single or multiple solid-state devices used in the power supply of modern computer systems. Transpiration cooling is the heat transfer mechanism. Cooling is accomplished by forcing air through a metal matrix, thereby cooling the matrix and its attachments. Limited testing indicates that transpiration cooling is a promising area for further development. The development will hopefully be pursued and described in a sequel to this article.

Editor's Note: This paper does not conflict with water-cooling systems work currently underway at Palm Beach Gardens. Transpiration cooling appears to offer advantages in certain applications (e.g., in distributed load situations). This paper, then, simply offers a "let's cover all the bases" approach, describing transpiration cooling as an alternative method to convective cooling.

Various problems inherent in transpiration cooling are recognized, but—because this technique is still in its infancy in the application discussed here—are not dealt with in this paper. One such problem is loss of air-flow through the sink, which would result in device failure. Another problem relates to cleanliness requirements for air supply. The size of particles and the presence of contaminates in the air, and the resultant effect on performance of the sink are specific areas of concern. These problems may be more effectively dealt with in a sequel to this article. Such a sequel is contemplated as the development of transpiration cooling progresses.

John Chisholm
Manufacturing Engineering
Systems Manufacturing
Computer Systems
Palm Beach Gardens, Florida

studied mechanical engineering at Northeastern University, Boston, Massachusetts and later electrical engineering at the Graduate School of Engineering, Harvard University. Mr. Chisholm has been with RCA since 1967 and has carried out various assignments in manufacturing engineering and test process. He was formerly employed by Pratt & Whitney Aircraft as Assistant Project Engineer of the Temperature and Combustion Groups where much of his experience was in the field of instrumentation for heat-transfer studies as related to aircraft propulsion systems. He is a registered professional engineer in the State of Massachusetts.

THE MODERN COMPUTER has power requirements which tax the ingenuity and resourcefulness of heat transfer technologists to an ever increasing degree. With the trend toward microelectronics and higher density modules, there seems to be no end in sight to the severity of the cooling problem for the computer manufacturer. This paper proposes an unusual approach to semiconductor cooling—transpiration cooling. The principle is old but it has apparently not been considered for solid-state requirements. Transpiration cooling results from passing a fluid (liquid or gas) through a porous medium to remove heat.

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Final manuscript received June 15, 1970.

Convective vs. transpiration cooling

For more than ten years, the popular engineering approach to cooling electronic equipment has involved the heat-sink coupled with some form of convective cooling. The semiconductor case itself is often made to serve as an initial heat-sink, constituting the first of a series of steps calculated to limit a temperature buildup at the internal junction. The small thermal capacity of the case necessitates a comparatively massive sink intimately attached to the semiconductor body. As the power demands on the system rise, it is necessary to increase the space allotted to the convective process until the sheer mass of auxiliary cooling hardware compels the designer to seek other means of cooling.

Forced-air convection coolers are well established as the routine solution to cooling requirements. Numerous manufacturers offer extruded aluminum fins in a multitude of shapes and sizes to meet industry's endless needs. To a lesser degree, liquid cooled heat-sinks are also offered for the more severe dissipation requirements.

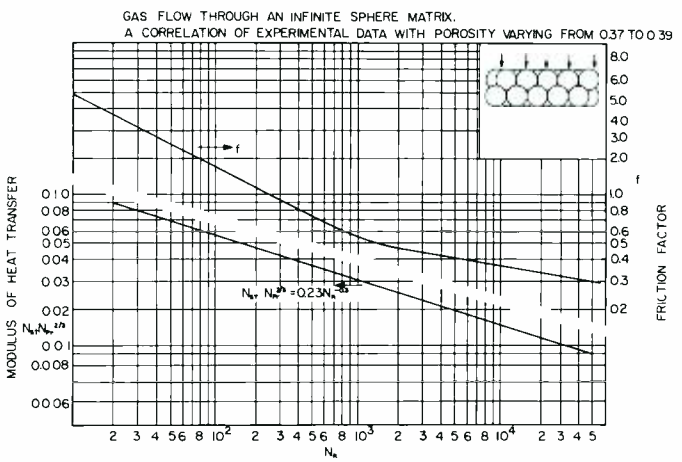

Fig. 1—Performance data for basic heat transfer and flow friction. (Ref. 1; Reproduced with permission of McGraw-Hill Book Co., N.Y.)

Fig. 2—Transpiration cooler with blower fan.

Fig. 3—Transpiration cooler with boxer fan.

Fig. 4—Transpiration cooler showing internal view.

Transpiration cooling is an alternative mechanism of heat transfer. Cooling is accomplished by forcing air through a metal matrix to remove heat from the matrix surface and the various components mounted on it. Transpiration cooling is more effective than convective cooling for at least two reasons:

1) The abundance of cooling surface characteristic of a metal matrix.
2) The comparatively low velocity at which the matrix gas stream breaks into turbulent flow.

Both these characteristics are reflected in Reynolds Number (RN) of fluid mechanics. The matrix surface is characterized by turbulence at low values of RN and an associated good mixing in which the gaseous boundary layer is continually broken. The familiar smooth-fin extrusion of convection cooling will display an RN of a few thousand in air while the matrix surface will often display an RN less than 100. Reynolds Numbers, of course, pertain to flow conditions and are dimensionless. A plot of the basic heat transfer and flow friction performance data for randomly stacked sphere matrices is shown in Fig. 1.[1]

Transpiration cooling dates back at least to 1800. One of the first users was the English scientist Sir Humphry Davy (1778-1829), who invented the Miner's Safety Lamp. Basic chemistry shows that a flame will not propagate through a copper screen due to the cooling effect of the screen. Observation of this phenomenon was, of course, of great significance to a world not yet acquainted with the incandescent lamp and still struggling with the safety of the carbide gas flame.

Lately, aircraft manufacturers have shown great interest in transpiration cooling for turbo-jet engines. Afterburner liners and combustion chambers have been successfully fabricated of porous metal to meet the structural requirements of an extremely hostile environment.

Mechanical aspects of transpiration cooling

Transpiration cooling could be used for high-power rectifiers and regulation systems with a net improvement in packaging density over the more conventional cooling schemes. The physical aspect of the envisioned cooler is like an empty box with porous sides on which the semiconductors are mounted. A blower-type fan pumps air into the box. The transpiration zones are made of porous sintered metal of favorable thermal conductivity—copper or, to a lesser degree, bronze. These materials are readily available as metallic filters and are made in various forms including sheet.

The semiconductors are mounted on the inside plane of the cooling sheet and are thus immersed directly in denser air moving through the plenum. Details of the design allow detachment of any side of the box to facilitate semiconductor servicing. Five sides of the box-like cooler are available for transistor mounting. Many departures from the box concept are possible; the packaging engineer is not limited by the usual geometry of the impact extrusion. Figs. 2 through 4 show a developmental transpiration cooler.

The heat transfer rate of the cooling material can be matched (within limits) to the heat load of the particular components by proper selection (pore size) of the permeable material. A further detail of the design allows each cooling panel to be electrically isolated.

Practical consideration of sealing voids between the cooling surface and its supporting frame makes it necessary to gasket the interface. Teflon tape is satisfactory as a sealer.

Transpiration cooling allows mounting the semiconductors directly on the porous surface, thereby providing a thermal path of minimum length from heat source to cooling air. Transpiration cooling also minimizes induced temperature rise on adjacent components.

Cooling panels should probably be at least ⅛-inch thick for structural reasons. Special consideration for stud-mounting rectifiers and SCR's requires thicker transpiration surfaces. In these cases, the porous members must carry a tapped thread deep enough to envelop the mounting stud, as this stud will be the primary conduction path for transferring heat from the semiconductor to the porous sink. Additional panel thickness does not significantly affect air flow except at very high flow rates.

Attachments to porous material

Porous material allows considerably less than intimate contact between its

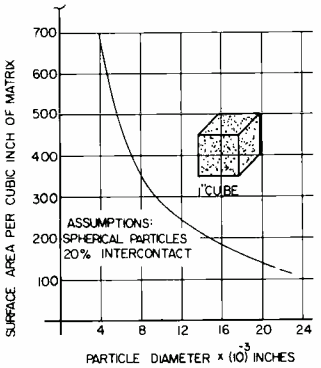

Fig. 5—Internal surface as a function of particle diameter in sintered elements (calculated).

surface and smooth-faced attachments such as transistors. The degree of surface contact is ordinarily proportional to the size of the constituent particles; fine particles offer more dense areas of conductance than do coarse particles. However, the pebbly character of a powder metallurgy surface can be reduced by machining areas where attachments are to be made. Of course, machining destroys the local porosity to a great extent; it distorts surface particles although ultimately yielding a fairly smooth surface with only occasional small fissures. Clearly, this is an engineering tradeoff of great significance as good thermal contact is essential at the interface of the heat source and the cooler.

Heat transfer of porous metals

A plot of available cooling surface versus particle size for a powder metallurgy matrix is shown in Fig. 5. This plot assumes an arbitrary 20% loss of internal area due to particle contact.

Of course, the large cooling areas associated with small particle size are available only at the expense of considerable pressure drop across the plenum; this pressure drop exceeds the capabilities of many commercial fans or blowers designed for present electronic system requirements. However, additional cooling area can also be realized by increasing the panel thickness; this approach has minimal attendant friction penalty.

Mathematical analysis of the heat transfer characteristics of porous metals is complex and almost completely empirical. Engineering texts treat the subject under the general heading of Compact Heat Exchangers and specifically as Packed Bed Systems—a carry-over from the chemical processing industry. Formal mathematical analysis is complicated by the number of independent variables. Porous materials are non-homogeneous and cooling is a strong function of the details of the gas flow through the porous materials. Transfer conditions are further complicated by the usual application of thermal compounds to improve the transfer of heat energy across the metal-to-metal interface. This complexity indicates that considerable laboratory work is needed to establish empirical relations and provide adequate design confidence.

Acoustical properties

Porous metals are inherently quiet. In certain applications, this could be a significant factor. The reason for the quietness is that the outflowing air is moving slowly and is uniformly diffused over a large surface; consequently, the usual fan noise is almost imperceptible.

Packaging design aspects

To the Packaging Engineer, transpiration cooling affords a new dimension of freedom in shaping cooling surfaces with substantial possibilities for increasing the density of his package. Nevertheless, caution in new design is required because the Packaging Engineer no longer has the degree of protection afforded by the thermal inertia of the usual extended finned surface.

Transpiration panels are largely voids and generally thin; consequently, the thermal capacity is small. The ability to cool is almost completely dependent upon the amount of air passing through, resulting in a diminished short-time overload capability. Loss of air flow could result in device failure. Size of particles and presence of contaminates in the air must also be considered as a factor in performance of the sink.

Fabrication

Transpiration surfaces are made by various techniques. Each technique produces a porous material displaying characteristics peculiar to the particular formulation. Two common techniques involve sintering compressed wire or metal felt. The product of these processes has pronounced strength advantages. A third process involves sintering compressed metal powders. This process is inexpensive and has been widely used for machine parts and metallic filters.

The transpiration surfaces used in the cooling package described in this artimetallurgy process. Here, metal particles are screened for size and then cle are manufactured by the powder vibration-packed in a suitable form. The sintering is performed at elevated temperatures, under a controlled environment, and results in contact-point bonding of the particles. The process yields both simple and complex shapes. However, not all metals are readily susceptible to sintering (aluminum is not), and some manufacturers have difficulty with pure copper as opposed to bronze, a copper/tin alloy. In short, there seems to be some measure of art mixed with the metallurgical science of sintering; development work in this field seems desirable.

Copper purity is a definite requirement for maximum thermal conductivity.

The following tabulation[2] illustrates this fact:

Thermal conductivity of metals and alloys
BTU/hr/sq. ft/deg. F/ft)

Pure Copper	224
Aluminum	117
Bronze (90%Cu/10%Sn)	109

Conclusions

In semiconductor applications, transpiration cooling appears to offer marked savings over convective cooling in cost, weight, and space—as well as significant advantages in design flexibility. These favorable factors appear substantially to outweigh problems of material and fabrication:

1) Large pores in a matrix degrade thermal conductivity but small pores restrict the passage of cooling air.
2) The pebbly character of the porous matrix necessitates machining to assure good thermal contact.

Limited testing indicates that transpiration cooling is a promising area for development. This development will hopefully be pursued further and described in a sequel to this article.

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Massproducibility—the implications for the computer engineer

P. M. Woolley

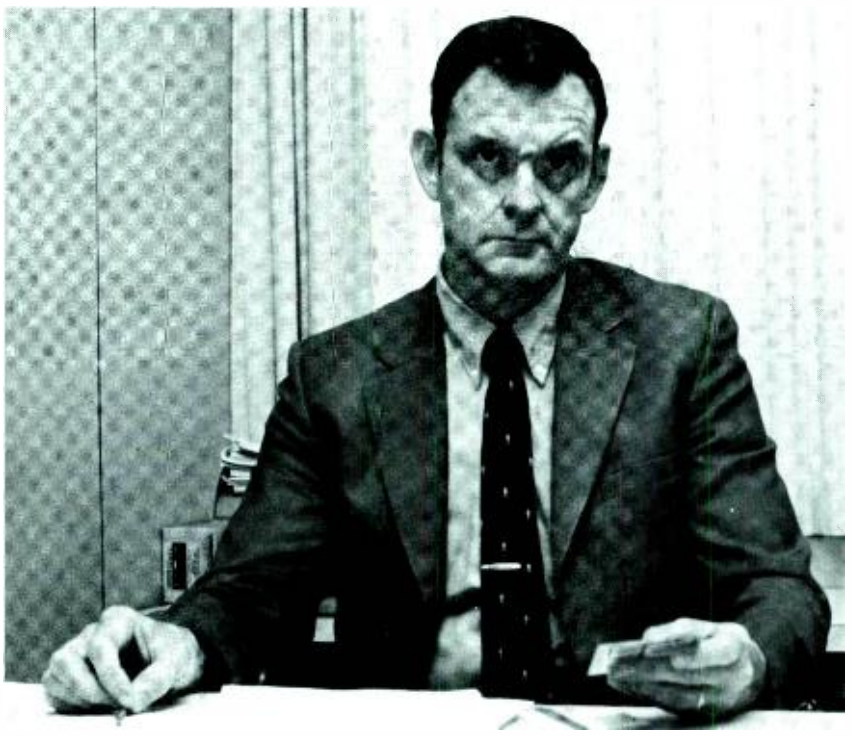
Certain aspects of mass production are strongly oriented to the computer industry, if not actually peculiar to the industry. Engineers newly assigned to RCA's Computer Systems organization may find themselves initially handicapped in the role of inexperienced computer-designers attempting to cope with the often-unique aspects of computer mass production. This paper provides guidelines to help bridge the gap in dealing with these computer production aspects, which are here grouped as *-ibilities*.

THE DESIGNER must first establish what *mass production* means as related to his design task. It is as serious a judgment error to design for high production, when a specific design is application-limited and production potential is low, as is the reverse condition.

Producibility

Once established that mass production techniques are to be utilized, the designer should familiarize himself with the manufacturing capabilities (both planned and already available) at the location where his design is to be produced. In addition to his design team, he should establish who are to be the key manufacturing and test personnel involved in his design. It also is vital that he not overlook the people responsible for design-check software generation as well as factory tests, especially if existing standard test routines require modification to accept his design.

Once the production team members have been identified and the basic concepts of the project outlined, the engineer must lead serious team planning to segment his design for ease and simplicity of assembly, accessibility for test, and processing into modular subassemblies, configurations, etc. Since a computer system is composed of a true conglomerate of functioning equipments, an outstanding advantage is derived for mass production if major portions of a design can be clearly defined, built, tested and literally stocked until the remainder of this product is required for final assembly. This is especially significant if subassemblies are usable on other designs or within the family of similar products. This multi-use characteristic further benefits a product which is to be manufactured in low or intermediate quantity rates that do not justify continuous production. Design maturity



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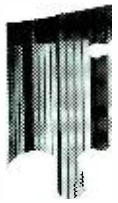
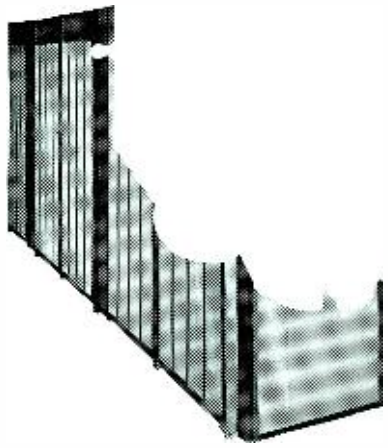




and segmentation not only permit assembly to proceed confidently using regular process operations at standard production rates, but also allow scheduling as people and material are available. These benefits contribute to plant load balance and subsequently minimize production costs. The engineer should realize that much of the assembly labor for large data processing systems is characterized by operators who perform a great variety of assembly tasks and who must be able to swing efficiently from one assignment to the other.

Flexibility

The RCA computer designer must consider that the primary product is information processing *service* and that the hardware itself is secondary. Since the computer market is highly volatile, any design faces rapid obsolescence unless it can be revised economically to variations not originally defined, such as a "high speed" version, increased capacity (or even decreased), and multi-purpose performance. To scrap one design in midstream and begin a completely new development to meet competitive systems may be self eliminating because of time or cost. *Convert, expand, reconfigure, upgrade* are standard to the vocabulary of Marketing, Manufacturing, and Engineering in Computer Systems. If adequately considered in original design concepts, such words may be applied economically.

Since most electronic data processing equipment is leased, it is almost certain to be rotated from site to site and often returned to its point of manufacture for updating, refurbishing, converting (or often just a well-earned bath.) This realization should restrict the engineer from custom-designing for a particular site or application.

To meet time requirements of the marketplace, designs often find their way down the assembly line without a complete evaluation of the design or software. Therefore, frequent changes to these designs may be expected and must be simply, yet accurately, defined and implemented to assure an accurate base for future changes. This is true for all equipment but is especially significant in the computer logic area. Control of signal paths and data flow is often complex, but the engineer must design a strict and retraceable control system. Minor wiring or logic errors may exist for long intervals undetected in normal factory testing since the possible number of test permutations and system configurations far exceeds practical test-time limits. As in most commercial divisions, RCA Computer Systems is in a highly competitive market, and customer needs may pre-empt an ideal production line balance or production test environment. Therefore, change and custom reconfiguration of a computer system often is the rule rather than the exception and must be provided for in the design.

Once the engineer understands this market environment, he can incorporate into his design the ability of his equipment to be so modified. In logic design, for example, providing minimum spare logic expansion area is standard practice. A successful design, however, is measured by the degree to which expansion capability was maintained throughout the life of the equipment. The mechanical engineer has a similar challenge and must provide flexibility in his own art but unfortunately cannot implement this as simply as can the logician. The same need and concepts apply to all skill areas involved.

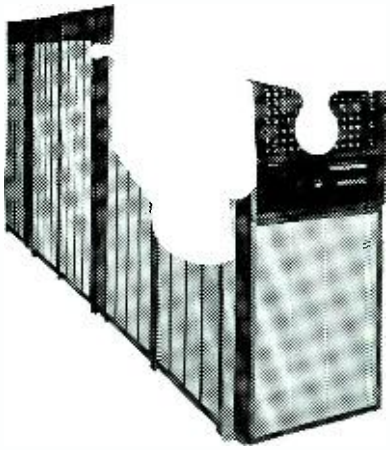
Repeatability

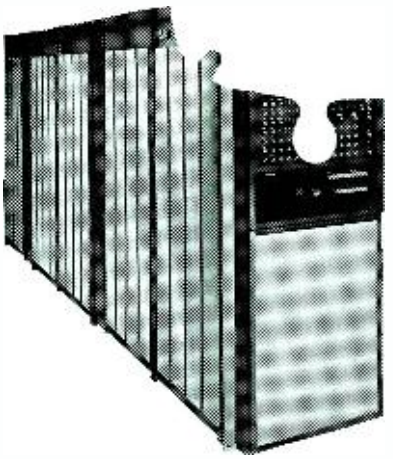
In a design that requires functional repeatability, the use of complex assemblies often results in a large accumulation of individual wires and components; therefore, functionally repeatable assemblies should be designed for simplicity. This approach is even more crucial in designs where assembly time extends over several production shifts; multi-shift production of complex assemblies fosters component omissions and mis-located assembly elements—which may pass assembly undetected.

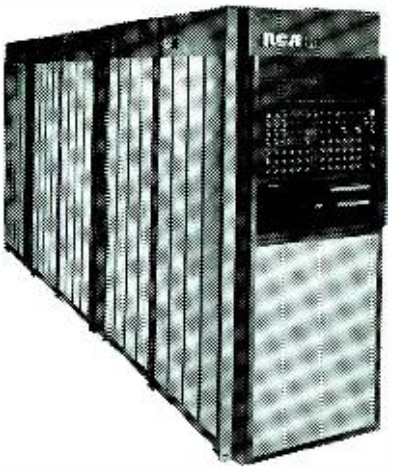
The engineer should carefully review his design concept to make certain that 1) all functions are indeed required, 2) the actual number of components specified is necessary, 3) the assembly can be no better segmented, 4) components can economically be mechanically keyed into their correct location or at least rapidly verified, 5) individual components can be easily identified and functionally examined for quality in the assembly (to facilitate troubleshooting and repair). Having implemented these foregoing ideas the designer may still find problems of functional repeatability. The basic design must then be examined and corrected early in pilot production to eliminate wide variability in operable performance.

Adjustability

A design may require elaborate or precise adjustment or alignment, often with copious instructions and procedures. A design in which the alignment is super-critical is almost certain to generate communication barriers, loss of production, constant re-testing, or re-adjusting—inevitably retarding final product development.







The designer is tempted to require the Manufacturing Operation to optimize a given function of his design to extract ultimate performance—sometimes referred to as a "marginless" assembly. This should normally be avoided but, if essential, there are ways to approach this condition and still provide usable manufacturing margins. Before the designer develops a masterpiece in narration, he should review the design to determine if such critical alignment can be obtained automatically by changing to a cast or pre-aligned assembly controlled by machinery (rather than depend on the dexterity and control of low-skilled manual assembly). The designer must consider total cost-effectiveness in light of purchase costs of valuable assembly tooling versus the potential of skilled-labor assemblies which either cannot be consistently adjusted or which cannot hold critical alignment. Perhaps the greatest loss is the test time wasted in repeated attempts to certify this assembly. The designer has a responsibility to avoid designs which foster such waste.

Reliability

In this article, the term reliability refers to characteristics of specified materials of the design, such as dimensional stability, electrical integrity, shelf life, fragility, and repairability.

This is an area where the designer will most easily stumble without realizing it until production has begun. Unless he is personally familiar with a specific material, he should seek expert guidance (not necessarily from a vendor's sales engineer) to be certain he is specifying materials that have the following characteristics:

1) *Availability in production quantities*—For example, the designer may find it easy to obtain a special compound or special-deposited multilayer device for prototype construction—only to discover later that either this material is proprietary or vendor manufacturing facilities cannot meet the ultimate quantity requirements.

2) *A proven performance history*—If the materials specified by the engineer have not been applied in either production quantities or environment, the engineer may well find himself busy solving basic but detailed vendor problems, instead of focusing attention on his own design; and he may even find it painfully necessary to change basic material during early production.

3) *Ability to withstand normal production handling and storage*—Material handling and storage in a mass production assembly plant are far different than in a development shop or small scientific instrument laboratory. Therefore, if the engineer specifies materials which require specialized packing (such as moisture-proofing or oil-vapor retainers), if he specifies custom-made padded containers to prevent breakage and chipping, or if he specifies special finishes which are subject to rapid oxidation, he can anticipate many hours of follow-up in developing unique handling techniques and custom storage facilities with rigorous stock controls. Not only is his time diverted from his design development but he is seriously jeopardizing his design integrity because such special considerations may be abandoned during the future life of the device.

4) *Ability to maintain dimensional stability*—Numerous materials are prone to absorbing moisture, out-gassing, attack by normal industrial solvents, self-stress relieving in storage and normal temperatures, developing surface growths, crazing, etc. Many of these materials are valuable to Engineering because they possess outstanding desirable characteristics; thus, the engineer must identify to the vendor (by notes on the purchase specification) any special treatment, coatings, or normalization cycling which a vendor must employ to eliminate these hazards after these materials are received for production. If he cannot specify how to eliminate the hazards, the engineer is obligated to consider alternate or modified materials without these hazards.

The last three of these main characteristics have one common problem particularly dreaded at a high-production facility: the acquisition of large quantities of components which originally met specification but later, in storage, were found to be unstable and outside acceptable limits. The result is painful decisions as to material rework or complete scrap to be made by engineering and manufacturing while production itself is halted.

Testability

Severe problems may arise if the designer provided limited (or no) verification of the design and its subassemblies. If a design does not readily permit Manufacturing to verify performance of a major subassembly or assembly, the factory must depend on a final systems evaluation to detect weaknesses or errors located at lower levels.

Inability to test at sub-levels is often untenable and invites costly tear-down, repair, re-testing, delay, and resulting poor quality. Any reliable design must provide for meaningful and accessible testing at the lowest possible assembly level. It is equally important that a design provide for elementary and non-argumentative testing. One very simple check the engineer can make is to determine the estimated cost of factory test equipment and testing time required as compared to total production costs of his design. This data will give him a common sense indicator of whether he should give this area further development or not.

Conclusion

If the inexperienced computer engineer applies the foregoing *ibilities* as guidelines along with his own *abilities* for traditional textbook Engineering design, he should achieve design proficiency sooner and with considerably less frustration.

Thermal analysis of air-cooled integrated circuit systems

D. Wray | S. Nanda

This analysis provides a better understanding of heat transfer in T^2L and T^3L integrated-circuit-package (ICP) systems. Multiple heat sources are considered, and their interactions are determined. Several formulas are developed to determine air and junction temperatures of any ICP in a channel, knowing temperature of the incoming air, physical configuration, and power dissipation of the ICP.

ALL ELECTRONIC CIRCUITRY dissipates heat due to inevitable losses. The internal temperatures of the components influence, and ultimately limit, component performance. If the heat cannot escape from its enclosure, the temperature of the component will rise until failure occurs.[1] Thus, performance depends on external ambient conditions and on heat generation within the component. To prevent a heat-generating component from reaching excessively high temperatures, heat transfer must be facilitated and low resistance provided for the heat flow.

The problems of heat transfer in T^2L and T^3L ICP systems can be divided into four parts:

1) The thermal impedance of chip and leads;
2) The thermal impedance of the copper path and circuit board;
3) The thermal impedance of the chip with board and copper path; and
4) The temperature rise in a *channel* of 32 chips with forced air convection. [Fig. 2b defines a channel.]

In this paper, the principle of superposition[5] is applied, multiple sources are considered, and interactions between sources are determined.

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Steady-state condition

If a component that does not generate heat is placed in an environment of uniform and constant temperature, heat will flow in the direction of lower temperature. This heat transfer will continue until both the component and the environment have reached a constant (steady) temperature. On the other hand, if there were no heat transfer and heat was being generated within the component, the temperature of the component would rise without limit. Therefore, to obtain an ultimate steady-state condition, the component should be cooled continuously and the heat should flow from the component to the ambient. Steady-state problems are characterized by boundary conditions being specified over the entire domain of solutions. Such solutions are sometimes called *jury* solutions because they must satisfy a jury composed of boundary conditions.[4]

Finite-difference equations and computer solutions

The essence of finite-difference methods consists of replacing pertinent differential equations by finite-difference equations. Physically, this is tantamount to replacing a continuous system by a network of finite elements, called a "lumped parameter network."[4] The device to be analyzed should be broken up into finite incremental volumes (nodes) and a difference equation (heat balance) written for each node.[5] The effects of conduction, free and forced convection, radiation, heat sinks, or sources can then be considered for each node.

After the thermal equilibrium of a system has been established, a process of heat transfer begins, and it continues until the steady state is reached.

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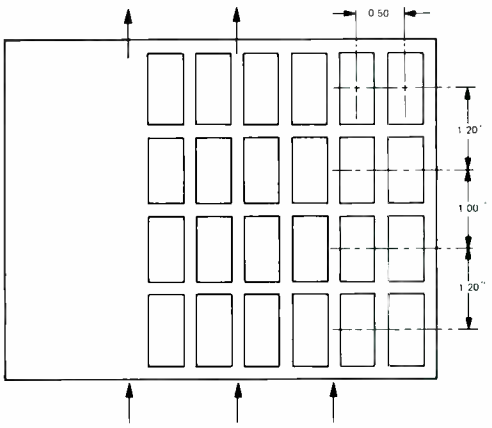

Fig. 1—Direction of air flow over a typical printed-circuit board.

The parameters are the thermal resistances, which may be considered as forming a network equivalent to an electrical network. Electrical circuit theory is usually the easiest way of determining the steady-state behavior of the system.

Application of the finite-difference method to each node results in a set of algebraic equations which are solved simultaneously for the unknown temperatures. Initial temperatures are assumed for each node. Repeated iterations then are performed by the computer until all the conditions are satisfied. A computer program written in FORTRAN IV was used.[5]

Thermal resistance

Thermal resistance (impedance) is analogous to electrical resistance.[2] In fact, a one-to-one correspondence can be established, and Ohm's law applied:

Electrical Current (amperes) is comparable to q, thermal heat flow (BTU/hour);
Electrical voltage is similar to ΔT, thermal temperature difference (°F).
Electrical resistance (ohms) is similar to R, thermal resistance (°F·hr./BTU).

Then $q = \Delta T/R$.

Design considerations

If the components are intended for continuous operation, the design should provide efficient heat transfer from the heat source to the ambient.

There are a number of formulas to calculate the heat transfer by conduction, convection, and radiation. However, prior to calculations, several assumptions were made while analyzing the problem in its different phases:

A. ICP Analysis

1) Chip was considered to be a constant heat source.
2) Chip was bonded to the case with eutectic gold.
3) Heat flow through the gold wires connecting the chip to the frame was neglected because of the small cross-sectional area.
4) The material of the case was assumed to be aluminum oxide (Al_2O_3).
5) The two halves of the case were sealed with glass.
6) The case and leads of the ICP were considered to be an isothermal boundary and were held at 0°F to obtain a temperature differential between the chip and the ambient.

B. Copper Path

1) The heat flowing from the lead frame was considered to pass through the ground and voltage pins.
2) Boundary was held at 0°F, to obtain ΔT as explained in A6).
3) Steady-state condition.
4) No radiation and convection.
5) Negligible heat conduction through printed circuit board connectors.

C. ICP copper path and board

Same assumptions as in *A* and *B* with the addition of ICP's on 0.5-inch centers.

D. Channel with forced-air convection

Same assumptions as in *A*, *B* and *C* plus the following:

1) Inlet air temperature is 43°C.
2) The required air volume is available.
3) The air flow is considered to be turbulent (Reynolds Number more than 3000).

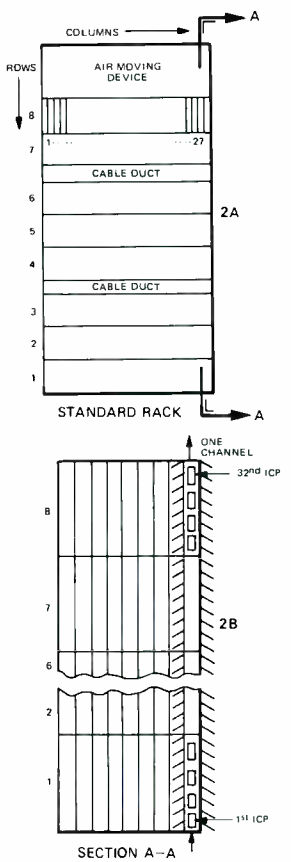

Fig. 2—Rack and channel configuration.

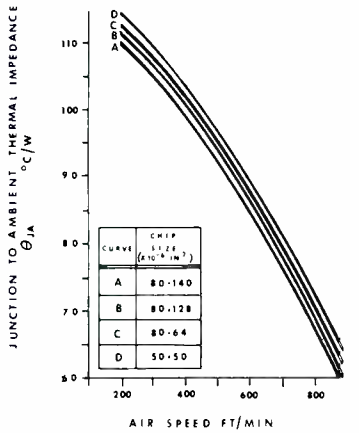

Fig 3—Junction-to-ambient thermal impedance vs. air volume.

4) The velocity is averaged over 27 columns.
5) Non-functional spaces are filled with dummy cards.

Thermal analysis

Using the configuration and dimensions shown in Fig. 1 and 2 as a model, a thermal analysis of the package environment was performed with a finite-difference-equation computer program. Also for this model, it was possible to express a junction-to-ambient thermal impedance (θ_{ja}) as a function of chip area and air speed. Junction-to-ambient thermal impedances for four typical chip areas are plotted in Fig. 3. The curves, however, do not present a complete picture. The air absorbs heat as it passes over the devices on the board; therefore, the first package in the row receives the coolest air (43°C) and the last package receives the hottest.

Results and discussion

The ceramic package was divided into nodes and the chip was considered to be the heat source. Thermal coefficients were calculated in BTU/hr.°F. Sample methods for performing these calculations are given in Appendixes I and II. The boundary was held at 0°F. The analysis yielded ΔT at each node, including the chip. Then the thermal impedance was calculated by adding all the ΔT's in one particular path and dividing by the total input watts.

Other analyses were made the same way: dividing the path or the element to be analyzed in different nodes, calculating their coefficients, and inputting the values to the computer. When all necessary thermal impedances had been calculated, a combined thermal impedance of chip, leads, copper path

and the board was computed. This combined impedance was then used to calculate the temperature rise in air and the junction temperature of any package using forced convection. The results show that the rise in air temperature/ICP (ΔT_n) and the rise in junction temperature of an ICP ($\Delta T_{(jn)}$) depends on the power dissipated by the package and the θ_{ja}. The air (T_n) and the junction ($T_{j(n)}$) temperatures of an ICP in a particular channel can be determined as follows:

$$\Delta T_n = \sum_{i=1}^{n} \Delta t_i n_i \qquad (1)$$

Where T_n is the total rise in air temperature for n ICP's (°C); Δt_i is the rise in air temperature/ICP for i^{th} package (°C); n_i is the number of packages with the same power dissipation.

And

$$T_n = T_a + \Delta T_n \qquad (2)$$

where T_a is ambient temperature
Also,

$$\Delta T_{j(n)} = T_{j(n)} + T_{n-1}$$

or

$$T_{j(n)} = (\theta_{ja(n)} P_n / 1000) + T_a + \sum_{i=1}^{n-1} \Delta t_i n_i \qquad (3)$$

where $T_{j(n)}$ is the rise in junction temperature above ambient (°C); $T_{j(n)}$ is the junction temperature of n^{th} package (°C); $\theta_{ja(n)}$ is the junction-to-ambient thermal impedance of the n^{th} package (°C/W); and P_n is the power (mW) dissipated by the n^{th} package.

Consider a configuration of ICP's as shown in Figs. 1 and 2 and having the following dissipation, size, and temperature conditions:

Row	*Chip size (mil²)*	*Power dissipation (mW)*
1	50 x 50	160
2	50 x 50	160
3	50 x 50	160
4	50 x 50	160
5	50 x 50	160
6	50 x 50	160
7	80 x 128	550
8	80 x 128	550

Air speed = 550 ft/min
Ambient temperature, $T_a = 43°C$

The number of ICP's in a channel dissipating 160 mW, $n_{1\text{-}24} = 24$, and the number of ICP's in a channel dissipating 550 mW, $n_{25\text{-}32} = 8$. Then from curve D of Fig. 3, the junction-to-ambient thermal impedance for 50 × 50-mil chip, $\theta_{ja(1\text{-}24)} = 94°C/W$ and from curve B, the junction-to-ambient thermal impedance for 80 × 128-mil chip, $\theta_{ja(25\text{-}32)} = 91°C/W$. From curve F of Fig. 4, the rise in air temperature per ICP for the 160-mW packages, $\Delta t_{1\text{-}24} = 0.3°$, and from curves B and C, the rise in air temperature per ICP for 550-mW chip, $\Delta t_{25\text{-}32} = 1.1°C$.

Using Eq. 1, the rise in air temperature per channel

$$T_n = \sum_{i=1}^{n} \Delta t_i n_i = (0.3)(24) + (1.1)(8) = 7.2 + 8.8 = 16.0°C$$

Eq. 3 gives the junction temperature at n^{th} ICP. Calculating junction temperature at 1^{st}, 24^{th}, 25^{th} and 32^{nd} ICP's:

$$T_{j(n)} = \frac{\theta_{ja(n)} P_n}{1000} + T_a + \sum_{i=1}^{n-i} \Delta t_i n_i$$

$$T_{j(1)} = \frac{(94)(160)}{1000} + 43 + 0 = 58.05°C$$

$$T_{j(24)} = \frac{(94)(160)}{1000} + 43 + (0.3)(23) = 64.95°C$$

$$T_{j(25)} = \frac{(91)(550)}{1000} + 43 + (0.3)(24) = 100.2°C$$

$$T_{j(32)} = \frac{(91)(550)}{1000} + 43 + (0.3)(24) + (1.1)(7) = 107.9°C$$

Thus, the highest junction temperature is 107.9°C, and the rise in temperature of air between inlet and outlet 16.0°C.

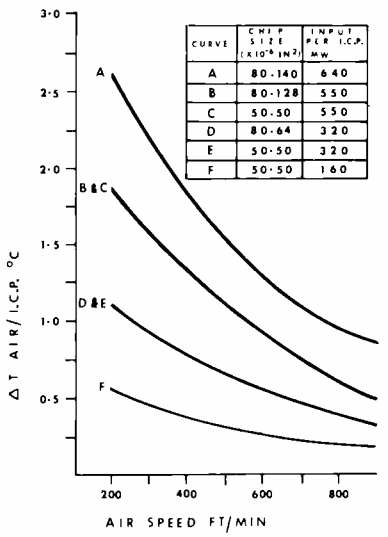

Fig. 4—Rise in air temperature per ICP vs. air flow.

Conclusion

Several formulas have been developed to determine the air and junction temperatures of any ICP in a channel for a given air flow, knowing temperature of incoming air, and the physical configuration and power dissipation of the ICP.

Appendix I—Determination of coefficient for conduction

The following thermal conductivities are considered:

Material	*Conductivity (BTU/hr. °F.ft.)*
Al_2O_3	11.705
Gold	169.00
Kovar	9.636
Glass	0.630
Solder	29.27075
Copper	224.0909
Board (epoxy laminate)	0.159

Usually the units for coefficient of conduction are in BTU/hr.ft.°F. However, the computer program requires the coefficient in BTU/hr.°F. To eliminate feet from the former unit, the coefficient is multiplied by cross-section area and divided by the length of the path between two particular nodes.

Appendix II—Determination of coefficient for forced-air convection

Reynolds Number, $N_{RE} = \rho VD/\mu$ where ρ is air density; V is the velocity of the air; D is the hydraulic diameter of the channel (defined in Fig. 2b).

Fanning friction factor, $f_e = \dfrac{0.3164}{N_{RE}^{1/4}}$

Surface coefficient, $h = (K/32.8D)\ N_{RE}\ f_e^{1/2}$, where K is the thermal conductivity of the unit.

For air at 150°F,

$K = 0.0169$ BTU/hr.°F.ft
$\mu = 0.0489$ lbs/hr. ft
$\rho = 0.0603$ lbs/ft³

As in Appendix I, the units of h for the computer program are BTU/hr.°F; so the surface coefficient is multiplied by the cross-section area of the path between two particular nodes.

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The RCA 1600—a versatile computer

J. Leppold | J. Raij

The 1600 computer provides a versatile means of dealing with a wide variety of applications that cannot be readily or economically handled by other products of RCA's computer line. Thus, it is an integral part of RCA's commitment to a total systems approach in data processing. In this paper, the 1600's wide acceptance is demonstrated through brief descriptions of specific applications. Hardware and software available with the system are explored, with emphasis on the 1600's open-ended design concept.

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received the BSEE in 1965 and the MSEE in 1968 from the University of Miami (Florida). He has completed courses in statistical communications at the Universtiy of Florida. Mr. Raij is currently working toward the MBA at Florida Atlantic University in Boca Raton. From 1966 to 1968, he was employed by IBM at Cape Kennedy, where he worked on hardware maintenance and later on system software support of Apollo/Saturn V ground computer systems. While with IBM, Mr. Raij also served as an instructor in computer programming. He was subsequently a part-time instructor in computer science at the Florida Institute of Technology (FIT) in Melbourne, Florida. He joined RCA at Palm Beach Gardens in 1968. Mr. Raij was assigned as a Senior Diagnostic Programming Specialist. He was recently promoted to Leader, Test Programming. He is a member of Eta Kappa Nu.

James H. Leppold
Test Programming
Systems Development Division
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received his early experience in computer technology and computer switching networks during his four years in the U.S. Air Force. His experience began as an instructor in the 412L (SAGE) System. From 1962 to 1964, he was lead instructor in the 465L project, a command-control system for Strategic Air Command, teaching the theory of operation of AN/FSQ-7 message switching processor. Mr. Leppold received the BA in Mathematics from the University of South Florida at Tampa in 1966. He joined Computer Systems in 1967 where he served as diagnostic programmer on the RCA 1600 processor. In 1968, Mr. Leppold's prime responsibility was detailed analysis of operating and communications systems for 1600 applications. Presently he is assigned as a Senior Project Leader of the front-end communications processor project.

In 1966, the Graphic Systems Division had assembled sufficient data to define a requirement for a small, special purpose machine to control their photocomposition unit. Additionally, other divisions of RCA had requirements for small, general purpose processors; Instructional Systems required an intelligent line concentrator in their computer-aided instruction system; Global Communications required a processor to function in message switching and store and forward applications; Consumer Electronics required a machine to automatically test and qualify integrated circuits that would be used in consumer products. What evolved from these needs was the RCA 1600 Processor—a small but flexible machine using the concepts of Elementary Operations (EO).[1] The concept of allowing the programmer to execute instructions at the EO level provides the capability of tailoring instructions to efficiently perform a desired task. This solution resulted in an extremely versatile machine capable of operating in many diverse applications.

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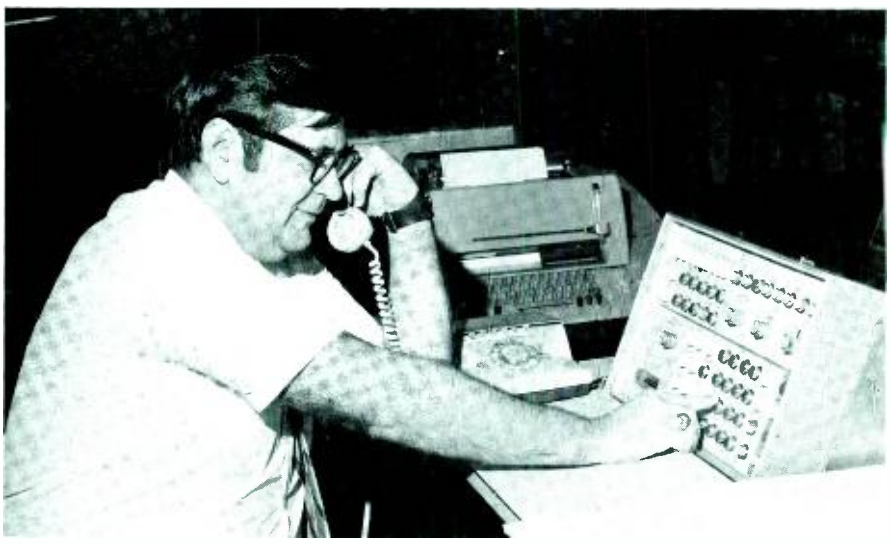
Sales audit system (SAS)

Figure 1 outlines the hardware configuration of the 1600 system operating in Miami, Florida, for a nationally known airline. At the customer's revenue accounting office, the 1600 receives, verifies, and stores on magnetic tape one million ticket sales a month. Input to this data entry application is the Sanders 720 Video Display System. Data for various ticket formats are accepted and verified concurrently by this system. Interfacing to the Sanders 720 Video Display System required no hardware modification to the 1600 system. In this application, the 1600 solved for the airline a critical ticket backlog problem at a substantial cost saving. And for RCA, the 1600



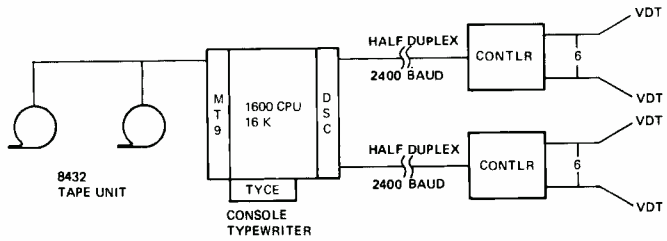


Fig. 1—Sales audit system (SAS).

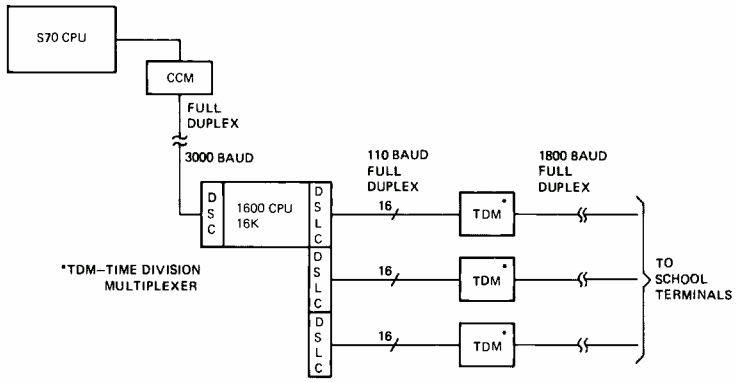


Fig. 2—Computer-aided instruction system I-70.

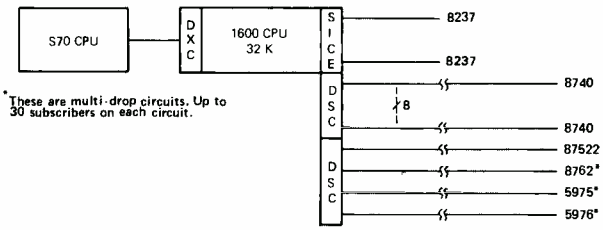


Fig. 3—Front end communication processor.

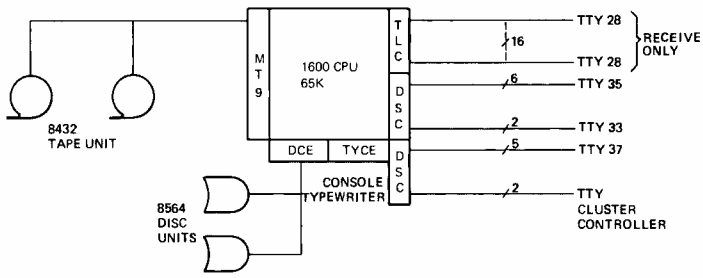


Fig. 4—Service-order processing system.

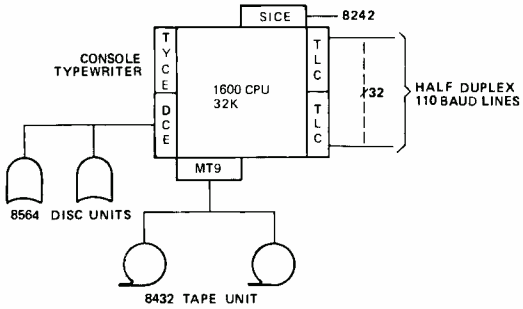


Fig. 5—Car rental control system.

gave Computer Systems a "foot in the door" to a potentially large computer systems customer.

Computer-aided instruction I-70

Fig. 2 illustrates the 1600 hardware configuration for RCA's I-70 Computer Aided Instruction System. In this application, the 1600 processor performed as a remote, intelligent line concentrator for the Spectra processor. The response time (i.e., the amount of time for the system to respond to a student's answer) is important in this environment. A response time of 1.5 seconds is not tolerable in a teaching situation. With 44 of the 48 student terminals on-line and active, the 1600 has an average response time of 0.9 second. In addition to sending messages to the student terminals, the 1600 validates each response received from the students and compares their response with the expected answer. If a student's response is incorrect, a message is transmitted to the student indicating a wrong answer. In addition, the wrong response is transmitted to the Spectra processor which maintains the student's performance on a lesson.

Front-end communications processor (FECP)

Fig. 3 describes the 1600 system configuration that the Government Marketing Office of Computer Systems is currently testing for a large government contract. Data to and from the front-end processor are controlled by the Spectra 70/60 on a poll/select option; that is, the Spectra processor requests data from specific subscribers and, in turn, selects subscribers individually. All polling, selection, and line-control functions are performed by the 1600 computer. Devices connected on the multi-drop circuits are polled sequentially, and are only selected when there are data for that subscriber. Effectively utilizing subscriber status tables and table look-up methods, 251 subscribers can be serviced by this 1600 FECP.

Store and forward-inquiry response

Service-order processing system (SOPS)

Currently, the RCA 1600 system is operating the service-order processing system for several telephone companies across the United States. Basically, SOPS provides the involved depart-

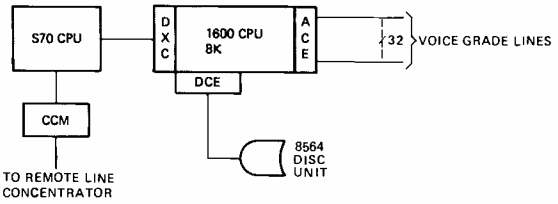


Fig. 6—Special-purpose controller I-71 (CAI).

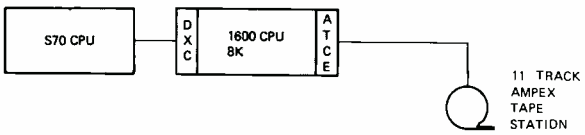


Fig. 7—Special-purpose controller for tape conversion.

ments of the telephone company with the paperwork necessary to carry out customer requests for new installations of telephone equipment.

In the past, service orders had been handcarried or, at best, transmitted by teletype to the appropriate departments. The previous system was subject to several disadvantages. Transmission of information was slow, extensive paper-tape handling was required, and manual logging was necessary to ensure that each affected department received all its orders.

The RCA 1600 system (Fig. 4) eliminates these problems. The service order is entered via a video communications terminal and is transmitted to the 1600 computer for validation and disc storage. The 1600 acknowledges acceptance of the order to the operator. On the day before the order is to be processed, pertinent information is transmitted to the various departments by teletype. After the order is completed, the computer is notified via teletypewriter and the order is updated, if changes are necessary. At the end of the day, all completed orders are written to magnetic tape for subsequent billing. Directory information is extracted and transmitted to a remote printer. Completed orders are purged from the disc files within three days after the completion date of the service order.

Inquiry response

The 1600 computer (described in Fig. 5) is being used by a car rental corporation to maintain a status file on each car entered into the Car Control System. Among the data stored on each car are its characteristics, history, and availability. Any change in the status of a vehicle is entered into the system via the remote terminal. With its associated data base, large amounts of information are available for other processors to digest and produce current statistical information for management. In addition, the customer receives fast and accurate billing information whenever the vehicle is returned. Rate information and total time the vehicle was used are calculated by the system and are relayed to the requesting data terminal.

Special-purpose controller

The following two examples of the 1600 processors operating in a limited environment illustrate the effectiveness of this small computer in solving specialized problems.

Computer-aided instruction I-71

As an integral part of RCA's I-71 computer-aided instruction (CAI) system, a small processor is required to transmit questions and/or audio responses to a selected student. Fig. 6 illustrates the 1600 hardware configuration used for this application. Control information is received from the Spectra 70 processor through the data exchange control (DXC). The 1600 analyzes the data; obtains the required word or words from the 8564 disc unit in digital form; and sends the data to the selected student via the audio control electronics (ACE). The ACE converts the digital data into an analog signal and sends the signal, via phone lines, to the headset of the selected student (1 of 32 lines). This technique of storing the vocabulary in digital form permits the storing of 2,000 different words on one 8564 disc unit.

Tape conversion

During a transition period of several years, a large bank and trust company in New York State had a requirement of translating, editing, and updating data files that were stored on 11-track magnetic tape to industry standard 9-track tape. RCA met this customer's needs by supplying them with three identical 1600 systems as described in Fig. 7. Data and control information is exchanged between the Spectra 70 processor and the 1600 via the data exchange control (DXC). The control information is decoded and the appropriate command or function is executed by the 1600. Code conversion and all tape commands are performed by the 1600 processor. On completion of the command, the 1600 notifies the Spectra processor of its status and the status of the tape controller.

Computer-controlled test

To gain on competition, a manufacturing plant in a dynamic industry must continually improve its manufacturing methods, building processes, and testing techniques. At the RCA Palm Beach Gardens facility, the 1600 is proving to be an effective tool in helping to cope with manufacturing test problems.[2] Two of the 1600 applications at this RCA plant warrant attention.

Central control processor

The central control processor for testing is shown in Fig. 8. This system is capable of loading processors of various types in 23 different test positions. Loading of design checks, diagnostics, and test routines is accomplished by utilizing the multiplexor or selector

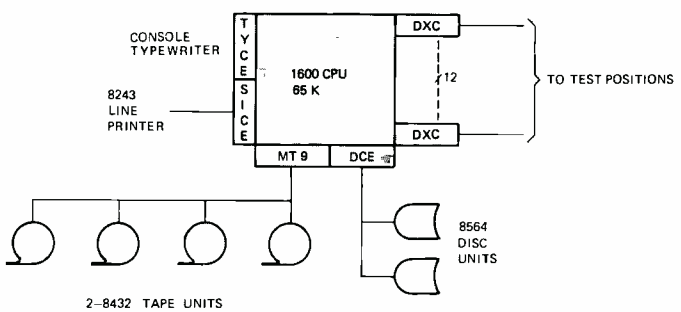


Fig. 8—1600 central control processor.

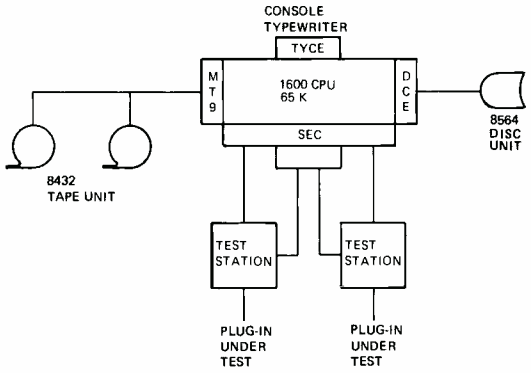


Fig. 9—NTS plug-in test system.

channels of the processor under test. Reduction of test equipment, effective control of released factory test routines, and current status information for management are among the benefits derived from this system.

Plug-in test system

Fig. 9 shows the configuration of the plug-in test system. This test system is capable of performing DC functional, DC parametric, and coarse propagation-delay tests on 90-pin plug-ins. The logic circuits may be either ECL, T^2L or T^3L, or combinations of these. Design Automation, using Roth's *D*-cube algorithm and Seshu's sequential analyzer, generates tests and diagnostics for the plug-ins. An auxiliary program converts the output from Design Automation to formats compatible with the 1600 plug-in test system. During production, data logging is accomplished on magnetic tape and/or the station console. In addition, test engineers may manually write tests using a test language tailored to this application.

Remote job entry

Versatility of the RCA 1600 computer operating in a remote job entry environment is demonstrated in the applications described below.

Spectra 70 to 1600 processor

Fig. 10 shows the 1600 being remote to a Spectra 70/55 processor located in Murray Hill, New Jersey. Line control between the Spectra 70 and the 1600 processor closely follows the 8740 line control procedures. Data compression and decompression techniques are used to utilize the communication facility effectively.

RCA 6 to 1600

A large supermarket chain has on order twenty-seven 1600 processors to operate as satellite computers for collection of divisional summary data. Fig. 11 outlines the typical hardware complement for a satellite installation. During the day, inventory data are collected, sorted, updated and stored on the 8564 disc units. In the evening, a data link is established with the RCA 6, and the accumulated data are sent to the central facility. From this information, daily and weekly reports are generated and are transmitted back to the satellite processor for printing.

IBM 360 to 1600 processor

Fig. 12 shows the 1600 interfacing to an IBM 360/65 for a textile manufacturer in North Carolina. The 1600 processor is replacing an IBM 360/20 acting as a satellite processor. Line control between the processors is binary synchronous communication in EBCDIC transparent mode. In addition to data compression and decompression routines, multi-leaving of input and output transactions from the 1600 is available.

Data communications

Most of these applications solve customer problems that could not be readily or economically handled with other products of the RCA computer line. The 1600 processor has an attractive price/performance ratio in applications involving data communications and special purpose controllers.

In the data communications environment, the 1600 performs exceptionally well with the group of control electronics outlined below:

Data set control (DSC)—enables the 1600 processor to exchange data, on a character interrupt basis with a maximum of 8 EIA standard data sets.

Data set line control (DSLC)—enables the 1600 processor to exchange data, on a bit interrupt basis with a maximum of 16 EIA standard data sets.

Telegraph line control (TLC)—enables the 1600 processor to exchange data, on a bit interrupt basis with a maximum of 16 direct current circuits.

RCA's 1600 computer may control in excess of 80 low-speed half-duplex lines (300 baud or less) via the data set line control (DSLC) electronics (EIA interface) and/or the telegraph line control (TLC) electronics (direct current interface). Utilizing the data set control (DSC) electronics, high speed circuits up to 50,000 baud may be serviced by the 1600 processor. Also, the 1600 can control a maximum of forty 1200-baud half-duplex circuits or twenty 2400-baud half-duplex circuits. Communication data links up to 230,400 baud can be serviced by the 1600 via the 8656 single channel communication controller. Outlined below are some of the remote devices currently interfaced by the 1600 processor via its communication control electronics.

RCA devices

5975—Low Speed Card Punch
5976—Low Speed Card Reader
8653—Communication Controller, Single Channel
8656—Communication Controller, Single Channel
8668—Communication Controller, Multichannel
8762—Data Terminal

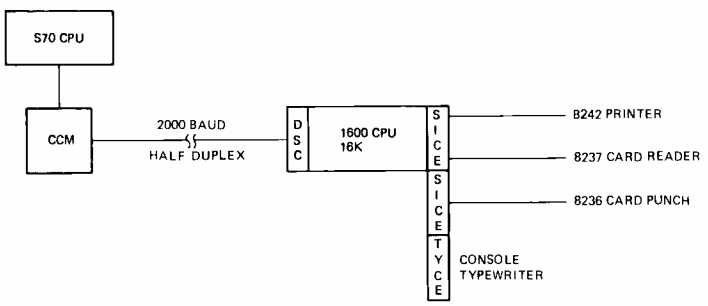


Fig. 10—Remote job entry—Spectra 70 to 1600.

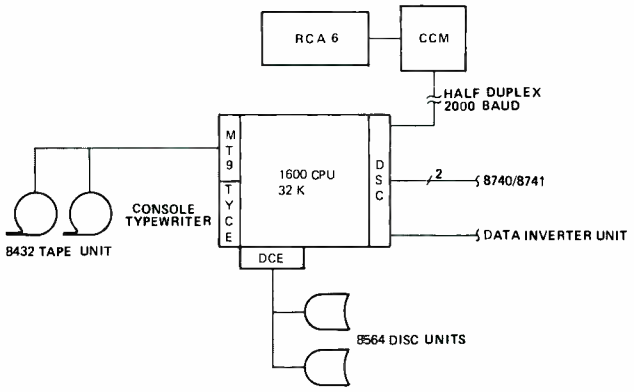


Fig. 11—Satellite processor—RCA 6 to 1600.

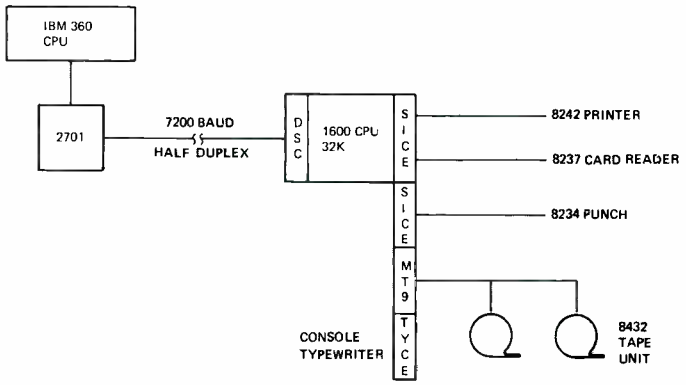


Fig. 12—Remote job entry—IBM 360 to 1600.

87522—Video Data Terminal
8752—Video Data Terminal
8740—Remote Printer
Modular Video Display System
RCA 1600 to RCA 1600

Foreign devices

Teletype Corporation Model 28 TTY
Teletype Corporation Model 33 TTY
Teletype Corporation Model 35 TTY
Teletype Corporation Model 37 TTY
Teletype Corporation Video Cluster Controller
Univac Data Communication Terminal 2000
IBM 360/50 BSC USASCII Non-transparent
IBM 360/65 BSC EBCDIC Non-transparent and transparent
Sanders 720 Video Display System

Control electronics

As other requirements developed, the 1600's open-ended design permitted RCA to respond quickly to these potential markets. Flexible, low-cost control electronics (listed below) were designed and added to the 1600's system complement of support peripherals:

Audio Control Electronics	ACE
AMA Paper Tape Reader	AMA
Ampex Tape Control Electronics	ATCE
Disc Control Electronics	DCE
Data Line Control Electronics	DLC
Fixed Head Disc Control Electronics	DRUM
Data Set Control Electronics	DSC
Data Set Line Control Electronics	DSLC
Data Exchange Control Electronics	DXC
9-Level Magnetic Tape Control Electronics	MT9
9-Level Magnetic Tape Control Electronics (200/800 BPI)	MT9M
7-Level Magnetic Tape Control Electronics	MT7
Special Equipment Control Electronics	SEC
Standard Interface Control Electronics	SICE
Synchronous Line Adapter (AUTODIN)	SLA
Terminal Control Panel (AUTODIN)	TCP
Telegraph Line Control Electronics	TLC
Timer Control Electronics	TCE
Console Typewriter Control Electronics	TYCE

Software

Appropriate system and maintenance software to support the open-ended design of the RCA 1600 system was required. Accordingly, a modular input/output driver system (IODS) was developed by the Test Programming Group at the Palm Beach Product Laboratory to be used in the hardware check routines for testing the different control electronics that may be connected to the 1600 processor. The IODS was made available to customers as a physical level language for input/output control, when it became apparent that standard operating software for the 1600 would not provide support for all 1600 peripherals. The IODS utilizes the macro capabilities of the 1600 macro assembler, XMAP, to generate a tailored software system at assembly time. The IODS is an assortment of modules or I/O drivers that control and issue I/O commands to the control electronics used on the RCA 1600 computer. Similar to the open-ended concepts used in the design of hardware, IODS, at program assembly time, selects only those I/O drivers that are required for a given system. As new control electronics are designed, a new I/O driver is written and is included in the IODS library.

To meet Communications Systems' and Planning's request for a general purpose communications operating system for the RCA 1600, a second software system was developed. This system is called the multi-function communication system (MFCS). The primary building block for this system is IODS. The MFCS is used primarily in a data communications environment and allows the application programmer to execute I/O at the logical level. Dynamic memory allocation techniques are used by MFCS. Line-control operations (polling, selection, error reporting, etc.) are performed by the separate line programs required for a given system. Each line program is self-contained and completely modular. The user is required to perform header analysis, code translation, and/or data processing that may be required for a given application.

Concluding remarks

The RCA 1600 processor has been widely accepted as a versatile machine in aiding RCA customers find practical solutions to their data communication and special purpose applications. Communication control procedures, processing requirements, and input/output facilities must be evaluated for each application. Based on the "customer appeal" of the 1600, Computer Systems Marketing is using this computer to establish a "beach-head" with customers that utilize larger computers in their data processing applications.

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Computer-aided design engineering—why and how

R. S. Singleton

Computer-aided design engineering at the Computer Systems plant in Palm Beach is discussed in terms of its purposes, applications, advantages, organization and operating practices.

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received the BSEE from the University of Florida in 1959 and the MSEE from New York University in 1961. He joined Bell Telephone Laboratories at Murray Hill, New Jersey after graduation. Two years later he joined the Martin Company, Orlando, Florida where he worked in various areas of computer magnetics. Mr. Singleton joined RCA in 1964 as a member of the Memory Engineering group. In 1970 he was promoted to his present position at the Palm Beach Gardens plant. This is his fifth published technical paper. He holds one patent.

COMPUTER-AIDED DESIGN (CAD), broadly defined, is the use of computer systems to aid the engineer in any portion of his design process. The computer because of its speed and precision provides significant advantages:

1) It frees the design engineer from much of the drudgery of routine calculations so that he may focus his skills on more creative work.
2) It allows him to make investigations in greater detail than possible by manual methods.
3) It directly reduces costs by making existing design methods more efficient.
4) It enables the automation of complex designs with reliability and repeatability of results.
5) It engenders new capabilities in areas where conventional methods are simply impossible.

These advantages of Computer-Aided Design may be illustrated by the following examples taken from existing CAD programs used by the design engineering group at Palm Beach Gardens.

Better utilization of engineering resources

Freeing the design engineer from the more routine aspects of his design and allowing more time for creative design can be illustrated by CAD programs which 1) analyze and statistically reduce the large amounts of data which come from the laboratory for the engineer's evaluation and 2) perform mean-time-between failure (MTBF) calculations for his proposed designs. Fig. 1 shows the computer output of a data reduction program in which 100 measured data points (transistor beta's) have been reduced for an almost instant evaluation. The 2000 calculations required for this particular reduction could have been performed manually in about two days; using CAD, the time was reduced to five minutes. Fig. 2 shows the dialogue of an interactive program which calculates failure rates and MTBF's for electronic circuits. Again, the tedious job of normalizing, entering tables, interpolating, etc., done manually requires days; the CAD program cuts the time to minutes.

In both of these cases, the engineer obtained extra days within his design schedule to examine his work and seek an improved approach through better components or more reliable application of components. The cost savings in this case were twofold. First, the engineer's time is better utilized. He is highly paid to think, and is now able to spend more time thinking. Second, a better product results. The improved reliability of the design results directly in lower field maintenance cost and better customer acceptance. More equipment in the field with lower maintenance cost is our Division's objective for adding to Corporate revenues.

More detailed analysis aids decision-making

The computer's capacity for detail allows analysis of design alternatives with such precision and rapidity that the engineer may now compare dozens of options where in the past he was often forced to make decisions by "rule of thumb" and experience alone. As an example of CAD's capacity for depth, Fig. 3 shows a portion of the circuit analysis of an entire voltage distribution system. So complex a task was approached hesitantly (if at all) in the past, yet the computer accomplished it in a run time of six minutes.

In this particular case, by running many variations, it was found that an expensive rectangular bus which had

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been "assumed" necessary by past experience, was indeed *not* needed and could be replaced by an open cable at a considerable cost saving.

Direct savings by automating existing jobs

Many existing jobs are essential in basically their present form. Nevertheless, the application of CAD programs in these areas can directly provide labor-cost savings, particularly in areas of bookkeeping. A specific example is accounting for, and cross-referencing of, the prodigious wire lists that must accompany every computer system. The man-hours of work that are saved by the computer doing this at the Palm Beach Plant are enormous.

More complex design capability

Until recently, engineers were limited to a relatively low level of complexity in the design of large systems. Although the theoretical basis of most of these systems was long understood (Newton 1670, Joule 1840, Maxwell 1870, etc.), the application of these theories to all but relatively small systems was limited by mathematical intricacy. Large systems had to be built before their performance could be measured. Engineers, conservative by nature, usually overdesign any sectors where uncertainty exists. This habit results in unnecessary expense. With the computer now able to examine these complex systems in toto, we are able to eliminate rough edges and manufacture a more sophisticated, reliable product at lower cost.

An example is a recently run thermodynamic model of the heat rise in a computer system. Rule of thumb had restricted the allowable temperature rise through the system to 12°C. A CAD program, analyzing a model of 120 simultaneous non-linear difference equations, showed that we could actually allow a 37°C rise without endangering performance. A relaxation of this magnitude will result in a direct manufacturing cost saving due to reduced requirements for cooling.

New capabilities for competitive markets

The precision and reproducibility of computerized design provides new capabilities which have no counterpart in manual design. An example is the computer-generated artwork for multi-layer printed circuits. It is simply beyond human capability to create manually these intricate patterns to the accuracy necessary for reproducible manufacturing.

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N          99          RANGE        17.99979    COEF.VAR.      0.07120
MEAN       50.53937    VARIANCE     12.94783    SKEWNESS      -0.01146
MEDIAN     50.25000    STD.DEV.      3.59830    NO.OF CELLS   19
L3DEV           39.744766      H3DEV          61.333954
L2DEV           43.342972      H2DEV          57.735754

CELL.MID.     FREQ.

   41.2022        1.  XXX
   42.1999        1.  XXX
   43.1777        1.  XXX
   44.1656        4.  XXXXXXXXXX
   45.1555        1.  XXX
   46.1444        4.  XXXXXXXXXX
   47.1333        6.  XXXXXXXXXXXXXXXX
   48.1221        9.  XXXXXXXXXXXXXXXXXXXXXXXX
   49.1110       16.  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   50.0999       10.  XXXXXXXXXXXXXXXXXXXXXXXXX
   51.0888       11.  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
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   54.0554        4.  XXXXXXXXXX
   55.0443        5.  XXXXXXXXXXXXX
   56.0331        4.  XXXXXXXXXX
   57.0220        3.  XXXXXXXX
   58.0109        2.  XXXXXX
   58.9998        1.  XXX
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Fig. 1—Statistical data reduction of transistor beta's.

The advantages of CAD in creating new capabilities are less directly measured. The ability to compete effectively by providing new products in the changing marketplace is certainly essential to the life of the Division, and the public image of the Corporation as an innovator has strong influence on price/earnings ratios, bond yields, etc., all which can result in significant revenues.

Organization of CAD facilities

Decentralized vs. centralized facility

Computer-Aided Design facilities may be organized to allow individual engineering groups to access the computer and do their own programming, or as a centralized group which provides programming and other service for all design groups.

The primary advantage of individual groups doing their own programming is that the engineer most knowledgeable about the subject will perform or direct the work. The disadvantages of an operation based totally on this method are that much of the time savings and design enhancement discussed earlier are lost to the programming effort; and it is unlikely that the engineer is a very good or productive programmer when programming is only a part of his effort.

The centralized facility benefits from highly efficient program production by full-time engineer-programmers; it provides an overview of the needs of all Engineering so that duplication is avoided; and it enables control of standardization so that programs may be interconnected into larger operating systems.

Computer Systems at Palm Beach has organized CAD as a centralized facility in support of all design engineering groups.

CAD programmer selection

The essential value of CAD programs is their usefulness to the engineer. This means that an engineer must be involved in their creation. Because individuals with both design engineering *and* programming experience are scarce, it is normally necessary to train one or the other. It has been demon-

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M. FARADAY          CURRENT SWITCH          65 DEG. C

  COMP          QTY     TOT.FR      MESSAGE
  199029-1        1     0.1364
  199401          4     3.1800
  82283-35        3     0.0112
  9545425-        2     0.1100
  99206-14        6     0.0356
  19941G          1     0.1430        N.P.

   TOTAL FAILURE RATE =      3.6163/MILLION HOURS

          M.T.B.F. =         276526.0 HOURS
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Fig. 2—MTBF calculation for electronic circuit.

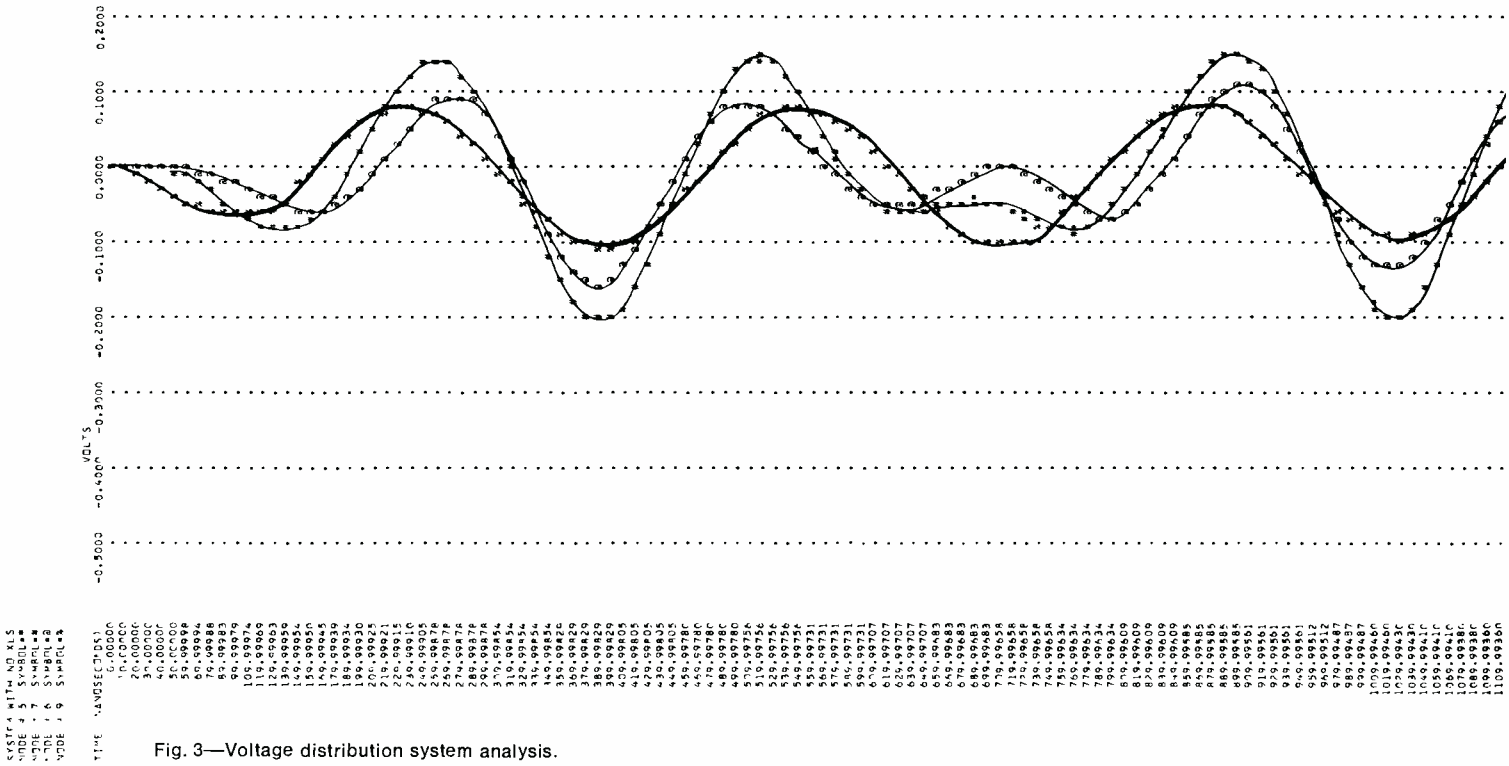


Fig. 3—Voltage distribution system analysis.

strated that engineers generally have a high aptitude for programming[1] and because programmers normally lack sufficient technical background, it is better to staff a CAD group with engineers who have aptitude and interest in programming. (As CAD systems become more complex, however, some highly skilled programmers and systems analysts are essential). Staffing with engineer-programmers has an additional benefit of ready rapport with engineers in the design groups.

Financial accounting

The charges of a CAD group may be allocated in several ways. One method is to operate a job shop, where each user contracts his CAD jobs and pays for them on his shop order. Another method is to consider CAD an overhead facility and distribute the charges over the entire Division budget. Other variations may combine aspects of these two extremes. The cost to the Division of establishing a CAD capability of a given level is, of course, reasonably constant regardless of accounting. The selection of the accounting method is determined by its influence on CAD operating effectiveness.

The job shop allows more user control over the selection of work, but deters the long-term establishment of a system of CAD programs most efficient for the Division. Each user looks at his own needs and is generally unwilling to extend programs for general use at his expense. This philosophy would force CAD personnel into a "sales" role which may adversely affect their morale.

The primary advantage of a complete overhead accounting is the ability to select programs that best serve Division objectives. The main difficulty lies in establishing priorities for programming and computer use.

At Palm Beach, we account for CAD programming services on our own engineering shop order, but we charge users for their operations expenses. This combination method enables CAD to control system efficiency by constraining individual users within their budgets from monopolizing machine time.

CAD operating practices

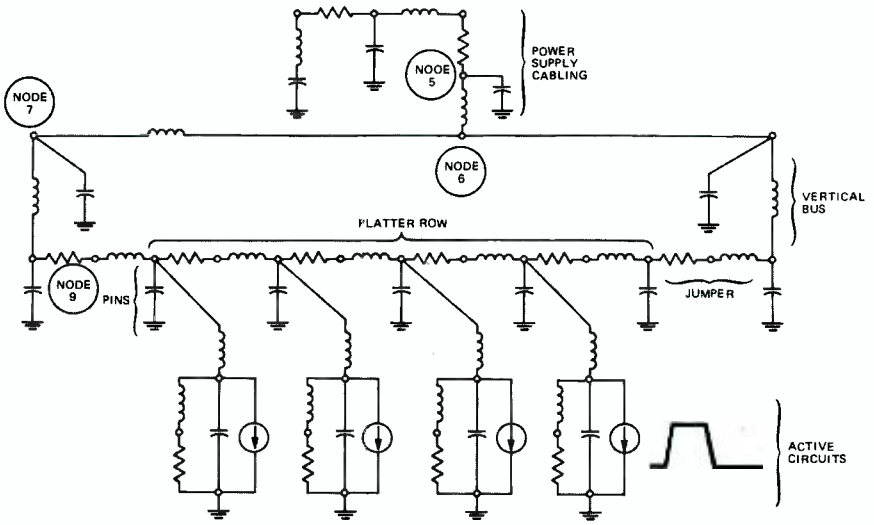
User considerations

The success of a CAD group depends on acceptance by its users. Operating practices must reflect this criterion, with equipment, usage rules, documentation, etc., providing the engineer with an easy-to-use tool.

Equipment providing for batch processing service, as well as remote time-sharing terminals, are available at Palm Beach. Although efficiency is often lower with programs written by user engineers, a "hands on" system is important in encouraging engineers to use CAD and in developing engineering empathy toward the CAD system. Engineers thus have the necessary machine priority and disc storage capacity to allow them to create and run programs of their own making as well as to use CAD-created library programs. Indeed, many of the design engineer's programs will eventually find their way into the general purpose library.

Complete, uniform documentation of all CAD library programs is required. Each program is referenced by the following documents, which are accessed through a keyword index to provide the user with the necessary details for program use:

1) *Descriptive title.* This is a brief but contains key words which a user would associate with the program. When contracted, it retains as much description as possible.



2) *User's guide.* This describes input and output formats, error messages, file names, memory requirements, peripheral device requirements, and operating restrictions.
3) *Program description.* This explains in detail the theoretical basis of the program and any restrictions in its application.
4) *Flow chart.* The flow chart of the functional execution of the program is made at a level of gross detail sufficient for analysis.
5) *Program listing.* This is a complete listing of all program statements in a logical sequence.
6) *Glossary of variables.* This is an alphabetic list defining all symbolic variables used in the program, their formats, array sizes, etc.
7) *Sample run.* This run is selected to demonstrate important program features.

To complement these features, the CAD group provides user education by distributing information bulletins, holding short seminars, and serving generally as a central source of CAD information.

Program selection

"Computers don't solve problems".[2] The solution of a problem requires intuition, which today's computers do not possess. The computer's total capability is to take the necessary and sufficient set of input data and map it into an answer by using the solution already set forth by the programmer. Thus, if a problem is to be resolved by CAD techniques, its solution must be known in extreme detail. With this basic restriction, the selection of CAD programs is governed by three considerations:

1) The need to demonstrate quick and direct cost savings to management,
2) The priority of urgent design schedules, and
3) The utility of the program in the overall CAD system plan.

This plan is to develop an overall CAD system based on the integration of small utility programs into an encompassing system program.

The ideal CAD system would be a program package so complete that it would require only the most general inputs to produce design details of a total system. In fact, programs approaching this level are already in existence.[3] To initiate such a monolithic system from scratch, however, ignores the premise that "no job is so large or so complex that it can't be run away from".[4] The CAD facility must, then, select small free-standing programs with the overall system in mind as an integration of these modules. For example, a program that outputs temperature data may later provide input to a program calculating failure rates. With this modular concept in mind, data formats, languages, etc. must be standardized as programs are generated.

Common to almost all programs in a CAD system is a data base of engineering components. This is essentially a storage and retrieval system housing basic data essential to all engineering designs: cost, design parameters, source, delivery, etc. The establishment of this data base consequently has a high priority in the program selection plan.

Source of programs

To avoid reinventing the wheel, a CAD operation must relinquish some of its creative luxuries and examine other sources of programs which are available more economically. Other than the essential programs written in-house by the CAD group, programs may be obtained from other engineers in-house, sources within the public domain, commercial software houses, universities, user societies, and equipment suppliers. The evaluation of programs from these sources must address the effort necessary to tailor them to specific needs, modify to common language, document, etc. These factors often outweigh low initial costs.

Conclusions

The ultimate justification of the expenditure of Corporate funds into the area of Computer-Aided Design is a financial one. Saving design time, improving quality, simplifying decision-making processes, etc., are all elements whose final measure is displayed on the balance sheet and the income statement. In order to attain this justification, the Palm Beach Computer-Aided Design group has been organized to provide efficient and effective utilization of computers for design in a manner which best serves the overall needs of the Division.

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4. Schultze, Charles, *Peanuts* (cartoon).

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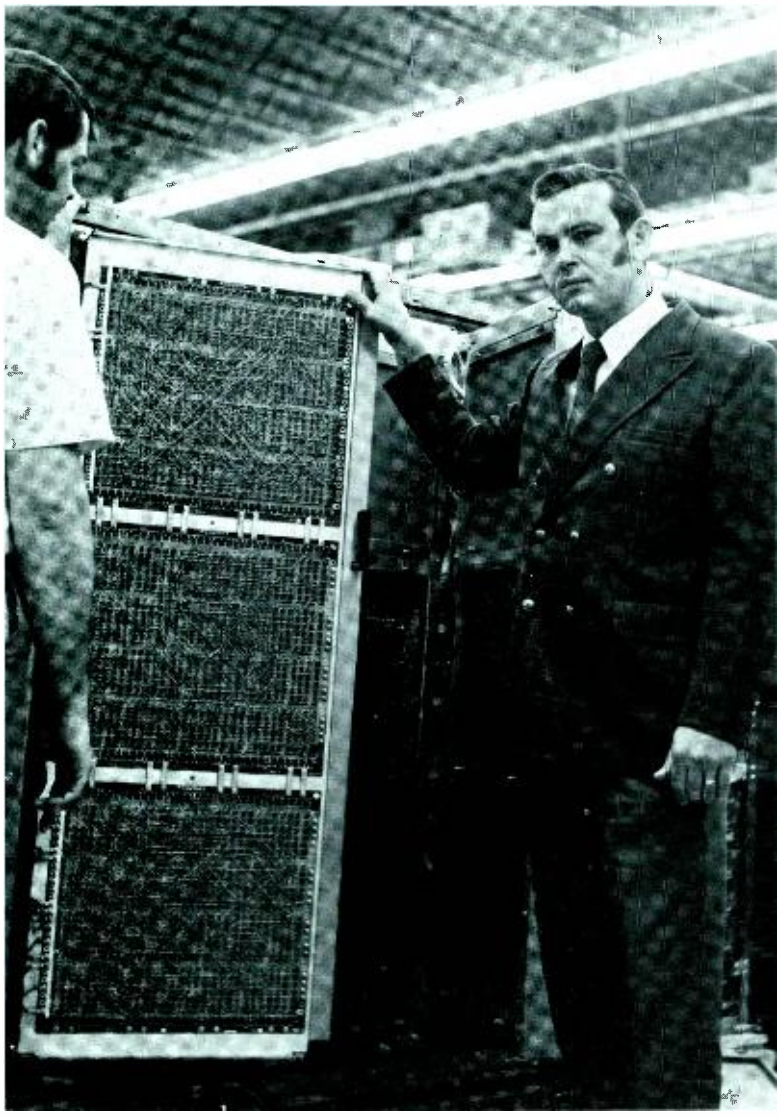
joined RCA in April, 1961 as a Test Technician and has advanced through various technical positions including Unit Test Technical Coordinator and Leader, Test Engineering Systems within Manufacturing Engineering. He was recently promoted to Manager of New Technology Systems (NTS) Manufacturing Engineering after serving as Manager of Test Engineering during 1970. His talents were utilized in solving 301, 3301, and Spectra 70 Central Processing Unit and Memory problems in a joint Palm Beach Gardens/Needham effort. Mr. Clary has designed various input output and memory test units during his tenure with RCA. In his present position, Mr. Clary is responsible for recommending and providing test methods and test equipment and for deciding on design, build, or buy of related test equipments for all phases of component, subassembly, plug-in circuit, subsystem, and unit development. Prior to joining RCA, Mr. Clary spent one year in the U.S. Army Electronics School at Ft. Monmouth, New Jersey. Subsequently he was assigned responsibility for maintenance of computer-controlled communications and microwave equipment at Owada, Japan for two years. He is a member of AIIE.

The case for peripheral simulation in computer testing

John P. Clary

Computer manufacturers may accomplish apparent 100% checkout of *positive* operational aspects of a system before delivery to the customer—but failure to explore the *negative* aspects of computer operation may result in early breakdown on site. "Positive" and "negative" (self-test capability) performance aspects are defined. This paper describes the Spectra 70 I/O and its interface, the test device and the test program. The test program is evaluated. A prime conclusion drawn is that the I/O interface tester program bridges the gap between Design Engineering and Test Engineering on CPU testability, maintainability, and producibility; this helps insure the compatibility of design and production which is essential to a quality product.



MAXIMUM BIT COMPUTER CORPORATION has just shipped a Super Time Sharing (STS) Extra Sensitive and Perceptive (ESP) Computer System to Multi-Bucks Banking Corporation. This computer was virtually faultless in its checkout phase from the manufactured central processor and peripheral devices through final systems test. This was a revolutionary feat for Maxi-Bit since the turn-around time to produce this complete system was minimum and all dates and commitments were on time.

Dedication Day at Multi Bucks; the manufacturer, salesman, and the vice president from little-known Half Byte Corporation are on hand for the ceremony. Half Byte has installed a new lightning-fast microfilm printing system to accompany the peripheral complement supplied by Maxi Bit. Half Byte debugged this new sensation previously on a leased STS-ESP system with nothing less than ultra positive results.

Speeches are made and short phrases of exuberant optimism concerning reliability, revolutionizing the industry, etc. are expressed as time approaches for power-on.

The flag is dropped. START is pressed. Tapes move, discs whirr, and the

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mechanical printer spits out jargon by the ton. Suddenly, tapes stop; discs stop; the microfilm unit sputters and dies as red lights flash and jaws drop.

The Data Processing Manager at Multi Bucks points at Maxi Bit. Maxi Bit and Half Byte blame each other. Pandemonium ensues.

What went wrong? Sorts, multiprocessing routines, operating systems, selected customer routines, test and maintenance routines, factory tests and manual tests were performed on the individual units and the entire system prior to the shipment to Multi Bucks. The *positive* operational aspects of the system were apparently checked to the fullest. The question arises as to how thorough a job was done on the *negative* aspects of the computer's operation.

Perhaps the illustration is a bit dramatic, but shades of realism can be recognized by any manufacturer of computers for today's market. Before shipments to customers, manufacturers have been able to discover such problems as minute shorts, slow circuits, and missing wires, even after the best available tests were performed. Excluding early-life component failures, many of these problems can be attributed to bypassing the *negative* performance aspects of a system.

The case

For the purposes of this article the definition of positive and negative operation for computer systems is as follows:

> *Positive* performance in a computer system is that performance which utilizes the normal processing functions designed within a system to attain the philosophical and conceptional goals of real work. More specifically, the error free *modus operandi* exclusive of parity errors, interrupt priority search, and sudden death in the form of idle cycling or program loops.
> *Negative* performance in a computer system is that performance which produces no real work for the customer but provides information for maintenance and error interpretation. These operations provide priority interrupt servicing, priority channel servicing, secondary error analysis, and provisions for bringing the system to orderly halts after errors. They also provide the scheme for use of information stored in scratch-pad memories, in hidden or shaded portions of main memory, and in I/O status registers for interpretation and resolution of error conditions.

To guarantee a check of all error-reporting functions associated with the internal logic or input-output channels of a central processor, the error conditions must be created manually. Under normal testing, these errors would be created manually during a subroutine written to handle the particular condition. For example, the interlock switch on a tape station door would cause an inoperable condition reported by a secondary status byte from the peripheral controller, or a parity error may exist on the input lines from a device controller to the central processor. Other error or status conditions might be generation of a manual interrupt by a remote device operator, delay of operable condition reported by a device controller, and loss of device input power.

Additional conditions that require checking and control by the central processor are interrupt and device service priority and exercise of an input-output channel to its designed throughput capability. No peripheral device designed to date, with the possible exception of a Data Exchange (Processor to Processor Conversation), can approach exercising an I/O channel to its design limitations with regard to data rate on a sustained basis (this assumes that all manufacturers limit the types of devices that can be handled by the marketed CPU).

Assuming that work-in-process peripheral devices are to be used at the factory for checking the central processor's response to the described conditions, the number of devices would be prohibitive. No single customer configuration would be adequate because all devices do not report the same type of error conditions and only a certain percentage of customer systems would require Data Exchange Units. It would be extremely difficult to check true priority of hardware because two devices cannot be made to request service at exactly the same time or at a prescribed point in a program sequence. The same situation applies to interrupt conditions requiring priority servicing.

The Test Engineering Department of Computer Systems, in conjunction with the Product Design Engineering Department, specified and developed a program to automatically deal with testing the negative operating functions of the third generation Spectra 70 Basic Processors. The Spectra systems are IBM 360 compatible and have emulation capability for a number of second generation computers. The Spectra 70 Central Processor Units now being manufactured are 70/15, 70/25, 70/35, 70/45, 70/46 and 70/55. The 70/60 and 70/61 are part of the 1970 product line.

The total program consists of an input-output tester (hardware), special test routines oriented toward factory testing (software), comprehensive test procedures, and trouble-shooting guides with technical aids (manual software) to assist skilled and semi-skilled test personnel in the debug phase. The basic logic design of the prototype test unit was contracted to the Product Design Engineering Department and the operating software to Test Programming. The final version for the higher order processors, such as 70/35, 45 and 46, was designed by the Test Engineering Department utilizing the best features of the prototype with added options and enhancements.

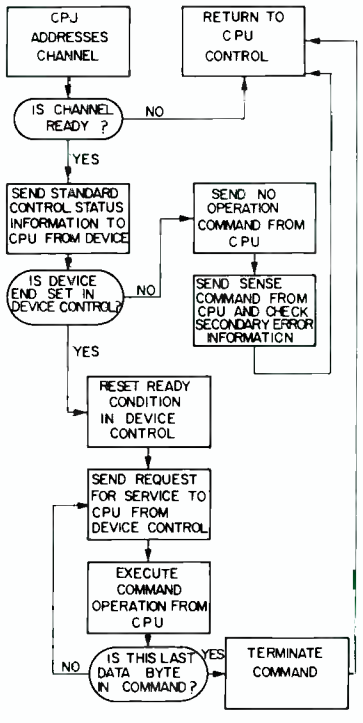

Fig. 1—Basic flow for single channel operation in Spectra 70.

The prime goals established for the total project were:

1) Test the CPU interface and all associated logics to a level less than and greater than the throughput data limits established by the Product Specification.
2) Provide necessary logic and test sequencing to check all negative processing functions which may be stimulated through the I/O interface channels.
3) Simulate peripheral operations relating to timing, status reporting, speeds, and interaction.
4) Provide comprehensive test routines to aid the technician in detection and correction of problems as they occur in test sequence.
5) Save test floor space and depreciation costs of work-in-production peripheral equipment which may be required to perform I/O channel testing.

The I/O and I/O interface

The interface for the Spectra 70 computers is labeled STANDARD and applies to all CPU's in the Spectra line. The only differences in operation are timing and whether certain modes such as *burst* or *chaining* of commands and data can be utilized. Multiplexing features are available on all but the smallest Spectra and operate the same as other channels except for the reporting procedure.

The basic flow for single channel operation in Spectra 70 is shown in Fig. 1. The sequence for multiplex (MUX) operations is generally the same except that the device address is returned to the CPU for recognition before transfer of each byte of information to or from the CPU. Fig. 2 shows the CPU controlled functions for I/O.

The BURST mode is a function which allows a multiplex channel to operate as a single channel. The MUX channels have a total throughput capability which may not allow a fast device to operate on only one of the MUX trunks. The BURST feature is controlled strictly by the CPU and is used to run fast devices such as a drum or magnetic tape station on a MUX channel.

Command chaining permits the sending of commands to a device without readdressing it and waiting for a READY signal. This speeds up the interface for back-to-back commands to the same device.

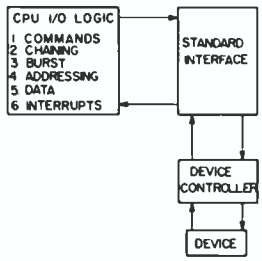

Fig. 2—Block flow showing CPU controlled functions for input/output.

Data chaining permits data transfers on fixed byte counts set up in the CPU to continue without a terminate of the device. This command is controlled by a flag in the CPU.

Both command and data chains are controlled by the CPU. If a device is chaining data on a read or write, any new commands to the controller for that device will be ignored.

The commands to the interface are separated into categories of primary or secondary importance. The difference is that secondary importance commands do not reset the READY condition of a controller, hence requiring further operations from the device. The primary commands that are controlled by the central processing unit are:

1) *Sense controllers secondary conditions*—The controller sends a byte which tells the CPU the status of the controller and its device or devices. If a certain bit is set in the byte, the CPU is required to further interrogate the device. The action taken based on the secondary indications is controlled jointly by software and hardware within the CPU.
2) *Read data in reverse order*—Data is transferred from a device to the CPU in reverse order and placed in memory in forward order. If a parity error occurs (data check bit), the CPU must interrupt the device and either reread the information or place the device inoperable.
3) *Write data to a device*—This command transfers data from the CPU to a peripheral device.
4) *Write to erase information in device*—This instruction will erase information in the device according to the number of bytes of data transferred from the CPU to the controller.
5) *Read data from a device*—This instruction will transfer information in forward order from a device to the CPU.
6) *Send status of controller and device*—This command will reset the termination interrupt pending condition that exists in a controller and transfer its status byte to the CPU. This begins the interrogation procedure controlled jointly by hardware and software.
7) *Write to control the device*—This command is used to transfer data to a controller to set up special conditions such as rewind a tape, pick a card pocket, or address a sector in a drum.
8) *Not operable*—This command is used by the CPU to reset the READY signal if conditions as reported by the status byte show the controller cannot accept other commands.

There are four secondary importance commands known as *who are you?, switch the reported end condition, set interrupt to hold off controller,* and *reset the reported end condition.*

The *Who Are You?* command asks the device reporting an interrupt to send its address to the CPU and reset the interrupt condition. The CPU then services the interrupt in order of reporting.

This brief description of the interface operation provides a fleeting glance at the functions the CPU may handle under normal and abnormal conditions. When a secondary indicator is set in the status byte and the CPU issues a *sense* instruction to read the sense bytes, the operation is quite normal; but the action a CPU must take on each of the eight bits within the sense bytes (up to two) may be quite abnormal and all of these conditions may involve separate hardware.

To send a read instruction to a controller from the CPU is quite normal. But what if (e.g., on the 30th byte transferred) a bit is dropped at the interface? Will the parity checker work properly? Will the bad byte be placed in memory? Will the CPU substitute a non-printable character with good parity in memory? What if other bits are dropped or picked up at other times?

What if a device causes an interrupt to occur and the CPU will not service it? What happens to a customer's routine if the interrupt is not serviced due to hardware problems with interrupt priority? The same question can be asked about service request priority.

Will the CPU bang on the interface channel continuously whether device input power is present or not? What will the CPU do about a service-request not-honored indication in the sense byte?

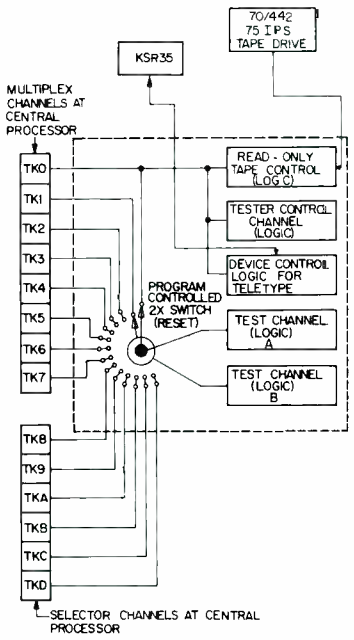

Fig. 3—Block diagram of I/O interface tester.

Many more questions could be asked, but the point is that each one of these functions is controlled by the CPU, and these functions are not normal operating sequences.

The test device

The solution to checking these functions rests in a device termed *I/O interface tester,* but whose capability lies far beyond mere channel testing (Fig. 3).

The device contains a *2X switch* allowing two channels to operate simultaneously. The logic functions consist of *tester control channel* logic to set up test conditions by program command; a *test channel A* logic to store the commands and perform the functions on an assigned trunk; and a *test channel B* logic to perform test functions on any other trunk that is being checked by channel A logic.

The *read-only tape controller* is used to read the program information from a standard product line tape station (70/442). The *teletype control* is used to run a KSR35 for option input and error printouts.

A teletype controller, read-only tape controller, and the control channel logic for testing are always connected to channel 0 of the central processor. Each channel may have more than one trunk, but the processor can only handle one device at a time through a channel. Each channel can operate simultaneously and independent of the normal processor operation.

The control channel logic is commanded by the CPU with an instruction previously termed *write to control device.* This instruction consists of four bytes of information. The first byte of the instruction states the operation code of information. The second byte addresses the channel with one nibble and the device address with the other nibble (one nibble equals one-half byte). The third and fourth bytes designate a base plus a displacement address in memory to transfer the control information. The number of control bytes transferred is determined by a CPU byte count.

The first byte of information transferred from the CPU to the control channel logic in the tester determines the following:

1) Test channel A or B to be set up;
2) Device address or command byte to be transferred following this byte; or
3) Leave trunk assignment as is or modify trunk assignment.

The second byte will be either a command or device address as determined by the first byte configuration. Bytes 3, 4, 5, ..., *N* are used for further commands.

This sequence is used by the CPU and software program to set up the testing conditions to be performed by test channels-A and -B logic via the control-channel logic. If a response from a future I/O command to test channels A and/or B does not match expected results, an error routine will list all pertinent information on the teletypewriter so the technician can exercise a series of options to aid in troubleshooting. A typical tester control channel flow is shown in Fig. 4.

As soon as the test channels are set up by the control channel, operations on the control channel cease, and the CPU begins to work with the test channels A and B.

Test channel A may be assigned to any trunk and device address, but test channel B is restricted from selection on trunk 0. Test Channel B is permitted on all other trunks of I/O Interface. Test Channel A and B are capable of performing all instructions that can be performed on an input or output device.

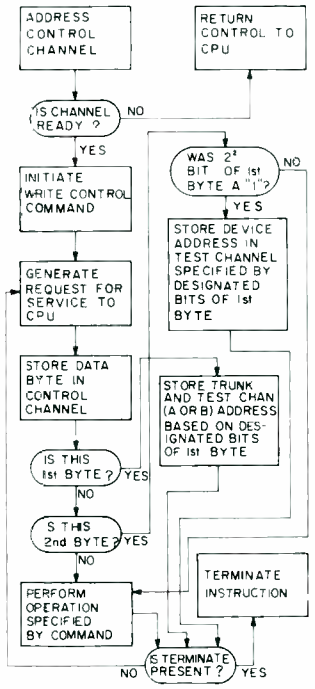

Fig. 4—Typical tester control channel flow.

There are thirty-two commands that may be sent to the control channel to set up test conditions in test channels A and B. Some of the more important commands are as follows:

1) *Simulate status indication of device (A or B)*
2) *Generate a manual interrupt automatically at a designated time (A or B)*
3) *Generate parity error (A or B)*
4) *Generate a delay of ready condition by the test channel*
5) *Set inoperable condition*
6) *Set the secondary status conditions*
7) *Generate high speed requests for service*
8) *Generate low speed requests for service*
9) *Check the request for service priority*
10) *Drop device input power signal*
11) *Simulate multiplexor operation*
12) *Simulate burst (multiplexor channels only)*

Combinations of these instructions plus normal I/O instructions plus the other twenty special write control instructions are coded together to provide tests on the interface control and interface logic of the CPU.

The programs

The programs were designed to help the technician as much as possible in troubleshooting the I/O problems as they occur. Diagnostic hardware is an aid in some of the Spectra 70 CPU's but the program provides a certain amount of standard information re-

gardless of the diagnose capability of the CPU.

All errors that occur during test result in a typed listing which contains information about conditions in the CPU at the time of error. This information includes:

1) Program segment number
2) Problem number
3) Error number within the problem
4) Brief description of the error
5) I/O error instruction and memory location
6) Data bytes of the write to control device instruction used to set up test channel A
7) Same as item 6), for test channel B.
8) Condition or situations present in the test unit at error instruction time.
9) Various condition codes and register status in the CPU at error time.

The description of the segment number provides additional information about previous operations and checks so that the technician can determine at what level his CPU is operable.

Additional aids in the program permit (at the technician's option) cycling on the instruction which caused the error, inhibit the printout, and inhibit the error idle by the CPU.

When the error is corrected, a recovery system is available to continue the program at that point without previous instruction re-try. When each segment is complete with no errors, the CPU prints out a segment number indicating lack of errors to the technician. Each program segment is read in from the product line tape station via the read-only tape controller. The printout device is a standard product line typewriter.

The read-only-controller (part of the tester) is specially designed so that a work-in-process tape station controller is not required to read in programs from a magnetic tape station. The magnetic tape station is a standard product line device.

Additional program options for the tester are: modifying the return address to any problem or segment; loading the scratch pad memory in the CPU; dump scratch pad or main memory; load main memory; and delete or add trunks on the CPU to the test level.

The problems within the program are divided into tests. Each problem may have several tests within it, and all problems are exercised on every trunk connected to the I/O test unit. Up to fourteen problems are located within a segment and as many as twelve tests in each problem.

A description is given in the program instructions of all problems and tests. As an example, the thirty-seventh test in the program is service request priority. The basic set of instructions for checking service request priority works up as follows:

1) A *check-the-request-for-service-priority* instruction is sent to either test channel A or B.
2) An instruction is initiated to the B test channel. This instruction must be read with the termination determined by the CPU. The complement-read-of-data option cannot be used. No requests for service are raised until the A test channel is initiated.
3) An instruction is then initiated to test channel A. The same rules apply to the instructions to A channel as were outlined for B channel.
4) The initiation of the A instruction will cause both test channels to leave a request for service to the CPU present.
5) When either instruction terminates due to CPU register 1, CPU register 2 equality (processor control) the other trunk will be terminated. Normal operation is for A test channel to terminate first.
6) The checks are made on the number of services to each test channel to see if priority was correct. The number of services done on each trunk is dependent upon CPU hardware and the type of trunks to which the test channels are connected.

The program test is divided into two parts. The first part checks the request for service priority between pairs of trunks; the second part checks priority of interrupts between pairs of trunks. The first problem of the test assigns trunk 0 to test channel A of the I/O tester. Trunks $1_{(16)}$ through $D_{(16)}$ are assigned in succession to channel B of the tester. All detected or non-connected trunks are automatically skipped.

After the trunk assignments and device numbers are made, a special command is issued to the I/O tester which will delay the request for service on both channel A and channel B until a Start the Device Reading Command is issued to both channels. The high priority trunk should receive all requests for service from the CPU, while the low priority channel receives none. To insure this condition, the CPU counts bytes.

Due to this special command, both channels will terminate with a pending interrupt condition. A check is made to verify the proper priority of interrupt. The status of channel and standard reporting byte on both channels are checked for correctness. This test is then repeated on all trunks resident in the Central Processing Unit.

Conclusions

The advantages of a test system such as described are evident from a production and quality standpoint. The ultimate objective is to be able to approach a 100% test of the basic processor as defined in the product specification with minimum manual intervention. This objective also reduces the need to provide specific customer-oriented or acceptance testing prior to shipment.

The disadvantages are in the evaluation of eventual obsolescence. If the new generation of computers (which may be conceived in a period of six- to ten-year intervals) encompasses new concepts in relation to input/output architecture and speeds, the equipment may become worthless from a production standpoint. The present philosophy in the industry of providing software continuity from generation to generation reduces the potential obsolescence.

One of the prime results of the I/O interface tester program is the bridging of the gap between Product Design Engineering and Test Engineering on CPU testability, maintainability, and producibility. The newer CPU's designed by RCA will encompass most of the features used in the I/O test units as standard diagnostic and testability hardware. This gap-bridging alone makes the I/O tester concept worthwhile, since product design and production must be compatible to provide a quality product.

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3. Bragdon, J. H. (Designer of Prototype #1), *unpublished communications to author.*
4. *Original Product Specification—RCA Standard I/O Interface C-1135* (June 1, 1965)
5. Klerer, Melvin and Korn, Granino A. *Digital Computer Users Handbook* (McGraw-Hill, N.Y., 1967).

Electrically-alterable read-only memory

J. L. Freeman

A read-only memory (ROM) is often used in the control section of a computer processor (mainframe). This paper describes the function of the read-only memory and differentiates between the mechanically-alterable ROM and the newer electrically-alterable ROM (called EAROM). An EAROM designed at Computer Systems plant in Palm Beach Gardens, Florida, is described in some detail. It is shown that the EAROM costs less and is more versatile than the older mechanically-alterable type.

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was graduated in 1958 from St. Joseph's College, Philadelphia with the BS in Electronic Physics. During the college co-op program as well as after graduation, Mr. Freeman worked for RCA in Camden designing airborne microwave radar transmitters. In October 1958, he was assigned to RCA in Moorestown where he worked on the design of surface radar transmitters and associated equipment. In October 1963, he returned to RCA in Camden where he designed radio broadcast transmitters. Mr. Freeman entered the data processing field in April 1964 with a move to the EDP division at Camden, working on memory circuit design. He has continued in this type of work since moving in July 1969 to the Computer Systems plant at Palm Beach Gardens. He has one patent award.

GENERALLY computer processors (mainframes) are composed of three sections: *memory* (storage), *control*, and *arithmetic*. Some RCA computer systems use a *read-only memory* (ROM) in the control section. This type of memory is designated read-only because data cannot be written into it by the programmer: the contents of the ROM are fixed by the computer design, as a series of elementary operations. Ordinarily these elementary operations become computer programs by being grouped into instructions which in turn are assembled into a computer program. In an RCA computer using a ROM, these elementary operations are used by the processor control logic to condition (*inhibit* or *enable*) the logic gates which transfer data in the processor.

Data stored in the ROM are usually mechanically alterable; that is, the contents of the memory can be altered by changing wired connections between its address input and the data output.

The memory described in this paper is electrically alterable. Its data are stored in ferrite cores; the magnetic state (magnetically saturated or demagnetized condition) of these cores is represented by binary *one* or *zero*. Thus the data can be changed by applying suitable electrical pulses to the wires threaded through the array of cores.

EAROM design

This electrically-alterable read-only memory (EAROM) utilizes two cores per bit of data stored. Use of two cores instead of one core provides specific

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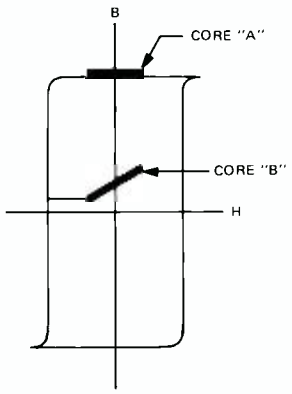

Fig. 1—Core flux states.

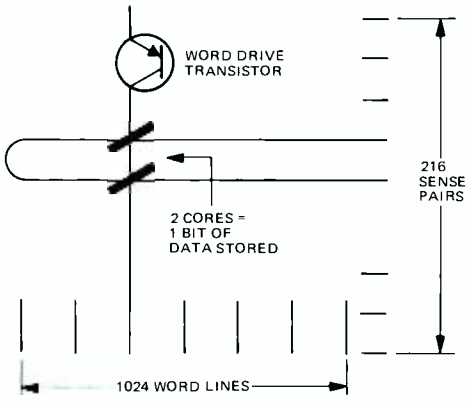

Fig. 2—Core array.

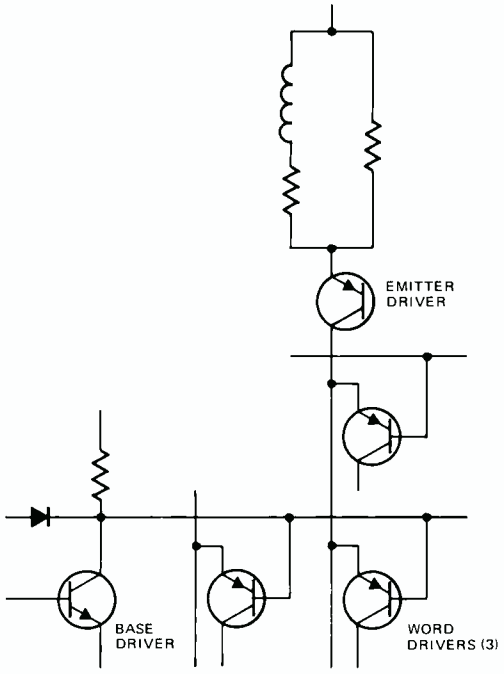

Fig. 3—Word driver decoding.

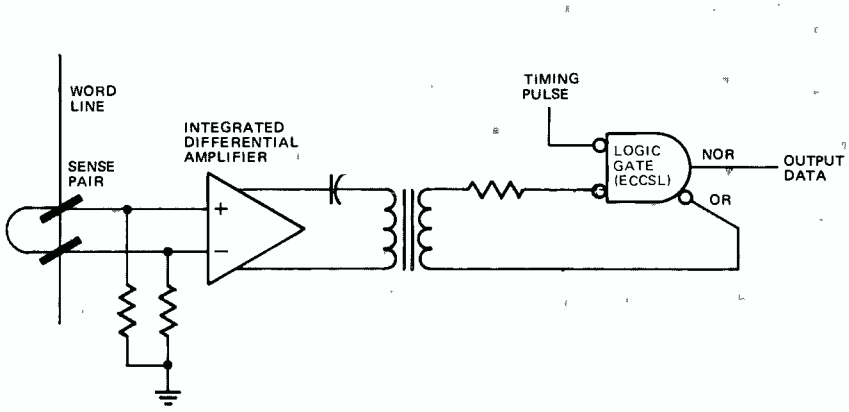

Fig. 4—Sense amplifier (patent applied for).

advantages: drive line inductance is independent of the stored data-pattern; and signal-to-noise ratio is improved. Core size is 30 mils (0.03 inch) outside diameter, 18 mils inside diameter, and 10 mils height. To store a bit in a core pair, both cores are first magnetized by a long-duration, large-amplitude pulse. Then one of the two cores is demagnetized by a smaller pulse. This completes the *writing* operation.

To *read* the stored data, a small current with a fast rise time is used. The sensed core output depends on the slope of the **B-H** loop for each core (see Fig. 1). This slope is somewhat greater for the demagnetized core (core B) than for the saturated or magnetized core (core A). The output voltages of the two cores are subtracted by use of a differential sense amplifier; the output of this amplifier is either positive or negative, denoting a binary zero or one, respectively (depending on which of the two cores was demagnetized during the *write* operation). The amplitude of the read current is kept so small that it does not switch any irreversible flux; hence, this is a *non-destructive readout* system.

A core array consists of 1024 x 432 cores; that is, 1024 words by 216 bits per word (see Fig. 2) with two cores per bit. The array is mounted on a printed circuit groundplane which has "pads" around its periphery. These pads, used for connecting word and sense wires, are connected by printed lines to "fingers" along the edges of the printed circuit board; each set of 64 fingers constitutes one connector, double-sided. Cables from the sense amplifiers are attached to the sense connectors. On each drive connector is mounted a printed-circuit board which contains either word driver transistors, or diodes, for isolating the word lines.

As shown in Fig. 3, fast PNP transistors are used as word drivers (one transistor per word line). One of these 1024 transistors is selected by a base-emitter decoding scheme. The 1024 transistors are divided into 8 groups of 128; then sixteen base drivers and eight emitter drivers are used to select one out of the 128 transistors in the group. The base drivers and emitter drivers are essentially level-shifters which amplify the 0.8-volt swing of the emitter-coupled current-steering logic (ECCSL) circuits to the levels appropriate to drive the transistor array. The emitter drivers also contain an inductance-resistance network which determines the amplitude and shape of the word current pulse.

An integrated high-gain differential amplifier circuit is used as a sense amplifier (Fig. 4). Its output is transformer-coupled to one input of an ECCSL logic gate, and a timing pulse is connected to the second input of this gate; thus the gate is enabled only during the time the sense signal occurs. The NOR output of the gate drives the memory data output bus to the processor. The OR output of the gate is connected back to the secondary of the coupling transformer; this positive or regenerative feedback connection provides additional gain for a negative-going "one" signal.

As described, the memory size is 1024 words by 216 bits. However, the basic

processor is set up to use a read-only memory of 3072 words by 72 bits. Thus, the outputs of two out of every three sense amplifiers are inhibited, and only the third output is sent to the processor. This one-out-of-three selection is made by a decoder which is driven by the two most significant bits of the 12 bit memory address register. The other ten bits of the register are decoded by the base and emitter drivers, to select one of the 1024 word-driver transistors. The memory also contains a timing pulse generator, which uses a group of delay lines and gates to time the word drive current and the sense amplifier output selection pulses, in response to commands from the processor.

The timing circuits, address register, sense amplifiers, and base and emitter drive circuits are built on printed circuit cards which are plugged into a printed backplane (Fig. 5). Four sections of printed backplane (A through D) are used, and they are mounted on a chassis adjacent to the memory core array (E). As previously described, the word driver transistors are mounted on printed circuit cards (F, typical) which are plugged into the connectors formed by the edges of the memory core array groundplane.

Writing data into the memory

To write data into the memory for Engineering prototype tests, a piece of special test equipment called a *loader* was built. The loader contains the circuits required to

1) Clear the memory by fully switching all the cores to saturation;
2) Read a memory address and its associated data from a punched paper tape; and
3) Activate the memory to write the 72 bits into the specified address.

To do all this, the emitter driver plug-ins (normally used for reading) are replaced by plug-ins which supply the higher-amplitude current needed for writing; and the sense amplifier plug-ins are replaced by bit driver plug-ins which drive a current down the sense line. This current down the sense line either aids or opposes the word write current, to demagnetize the appropriate cores. The loader also contains a tester to read the memory and check its data output against the paper tape.

This memory operates at an access time (from the read command input to the data output) of 100 nanoseconds, and a cycle time (between successive accesses) of 250 nanoseconds. An Engineering prototype has been operated in the Spectra 70/60 processor; this prototype ran all the design check programs, testing the processor's data flow paths and control circuits.

Mechanically-alterable ROM

The mechanically-alterable ROM uses a thick-film resistor deposited on a glass substrate, as its memory element. The resistor is permanently connected to the word line; and it is either connected or not connected (binary *one* or *zero*, respectively) to the sense line, under control of a photomaster.

Advantages of electrically-alterable ROM

Economy

The electrically-alterable ROM is less expensive than the resistor memory. For example, the electrically-alterable memory uses one-half as many sense amplifiers and one-third fewer drive transistors than the resistor memory.

Versatility

The 70/60 and 70/61 computers contain an optional feature called an *emulator*. This is a read-only memory which also performs the processor control functions, but is programmed to accommodate the instruction set of certain older RCA or IBM computers. Using a resistor memory as an emulator necessitates making a new set of photomasters for each individual emulator. But if the electrically-alterable memory is used, the same memory can be utilized for any emulator; the only difference is in the paper tape used to "load" the data into the memory.

Conclusions

Use of the electrically-alterable memory provides substantial cost savings (up to 50%) as well as economies in production and stocking of parts.

Acknowledgements

The research for this project was performed at Princeton Laboratories by Dr. R. A. Shahbender and K. Li using cores supplied by E. Schwabe of Memory Products Division, Needham, Mass. The memory core array was designed by W. H. Smith of Memory Products Division. The memory was developed by the Memory Engineering Group under W. E. Salzer at the Computer Systems plant in Palm Beach Gardens, Florida.

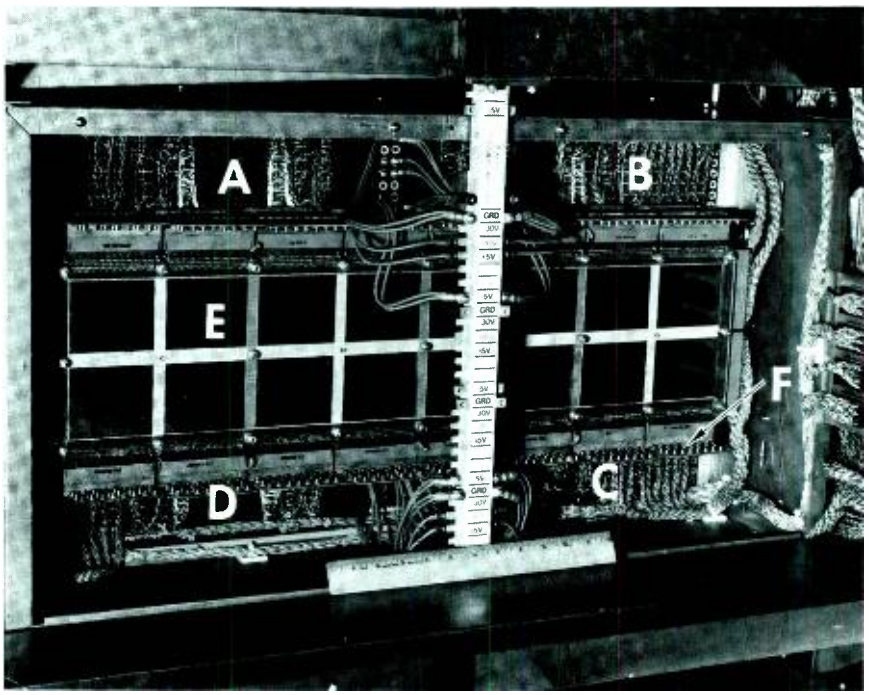

Fig. 5—Photograph of the EAROM.

MOS random-access memory systems

C. L. Jones

In memory systems applications, MOS arrays provide systems designers with a new spectrum of capabilities to exploit; in addition cost projections for MOS memory systems appear favorable. This paper discusses the feasibility of MOS memory systems, and compares available vendor devices in a concise, tabular survey of MOS memory arrays.

THE MEMORY SYSTEMS DESIGNER now has alternate approaches that he can take to satisfy his various memory requirements. Because of improved yield and intensive competition, both MOS and bipolar memory arrays are becoming attractive alternatives to a core design. The bipolar memory array is already being used extensively in high performance buffer and cache memories where the required fast access and cycle times cannot be achieved with a core memory. Mos memories are natural solutions to storage problems in computer peripheral equipment and data terminals. Previously, small, low-performance core buffer memories were used to fill these storage needs. The cost per bit of these small core memories is high because there are so few bits over which to amortize the cost of the support electronics. Mos memory arrays can already be justified, on the

Fig. 1—Survey of MOS-bipolar hybrid memory systems and MOS memory chips.

Vendor	*Size*	*Speed*	*Op. power*	*(vol) cost/bit*	*Voltage Req'd*	*Comments*
Memory Systems						
Company #1	Modular from 512x8	Access/cycle (max.) = 250/300 ns	(typ) 0.42 mW/bit	(10 cards) 5¢ (1971) (10 cards) 2¢ (1974)	+5V, +10V −7V	T^2L interface. System or card level. Card select input provided. Collector OR′ capability.
Company #2	1024x4 1024x2 1024x1 2048x2 2048x1 4096x1	Access/cycle (max.) = 400/600 ns	(max.) 0.47 mW/bit	(1-9) 3.9¢ (1971) (10-24) 3.42¢ (25-99) 2.93¢ (100-499) 2.54¢	+5V, +10V	T^2L interface. Sell in 26-lead package. No collector OR′ capability. Chip select can be achieved with external gating.
Memory Chips						
Company #2	256x1	Access=1.5 μs	2 mW/bit 50 μW/bit @ standby	1971 (1-24) 15.6¢ (25-99) 12.7¢ (100-999) 10.0¢ (10k) 3.9¢	+5V, −10V −7V	Static, T^2L interface. Chip select provided. Collector OR′ capability.
Company #3	64x2	Max. read & write rate=1 MHz	1.05 mW/bit @ 1 MHz	(10k) 12.8¢	−12V, −26V	High voltage T^2L interface. Dynamic, refresh in parallel once/0.1 ms. Chip select provided. Collector OR′ capability.
Company #4	256x1	Read cycle= 1.5 μs Write cycle= 1.0 μs	2.0 mW/bit	Nov. 1970 (1-24) 15.6¢ (25-99) 12.7¢ (100-999) 10.0¢ (1k-4.99k) 8.6¢ (5k-9.99k) 7.2¢ (10k up) 6.3¢ Third quarter '71 4.7¢	+5V, −7V −10V	Static. T^2L interface. Chip select provided. Collector OR′ capability.
	1024x1	Access/cycle =390/580 ns		Nov. 1970 (1st 5000) 2.7¢ (next 10k) 1.47¢ (next 25k) 1.17¢ (next 50k) .78¢ Third quarter '71 0.5¢	+5V, +20V +17V	Chip select provided. Collector OR′ capability. Packaged in 18-pin plastic DIP. Dynamic, refresh 32 addresses. Once in 2 ms. High voltage interface requires sense amp.
	1024x1	Access/cycle =150/300 ns		Nov. 1970 1st 5000) 3.0¢ (next 10k) 1.62¢ (next 25k) 1.29¢ (next 50k) 0.86¢	+5V, +20V +17V	Production qty. First quarter '71. Devices selected for low access time.
Company #5	32x1	Read & write cycle=1.5 μs	2.82 mW/bit (typ)	19.8¢ ('70) 14.4¢ ('72)	+5, −12V −7V	T^2L interface. Static.
	256x1	cycle=700 ns	0.29 mW/bit	3.92¢ ('70) 2.05¢ ('72)	−24V, +2V	High voltage interface. Dynamic, 4 clock phases required. Refresh 16 wds., once/ms. Collector OR′ capability. Chip select input provided.
Company #6	1024x1	Access/read cycle/write cycle= 350/500/800 ns	0.1 mW/bit (max) 50 μW/bit average	Ceramic (Dec. '70) (1-24) 4.1¢ (25-99) 3.3¢ (100-999) 2.7¢ (1k-4.9k) 2.05¢ (5k) 1.46¢ (next 10k) 0.98¢ 1972 (100k) 0.66¢ Plastic (100k) 0.56¢	+18V +21V	Requires special interface ckt. Dynamic, refresh 32 words, once/1.0 ms. Collector OR′ capabiltiy. Chip select input provided.

basis of cost, to fill most of the requirements for these small memories. However, the area in which MOS memories offer the greatest potential is in the design of large main memory systems. Here, the MOS memory is rapidly becoming cost competitive with core memory and its performance can exceed that of a core memory of equal size.

Advantages

The major advantages of MOS memory systems are their low cost potential, reduced size and weight, relatively low power dissipation, and high reliability.

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received the BSEE in 1963 and the MEE in 1967 from the University of Florida. He was employed in 1963 by Radiation, Inc. of Melbourne, Fla., in their Ground Support Equipment Department where he performed logic and system design of telemetry systems. After receiving the MEE, Mr. Jones returned to Radiation, Inc. as a circuit designer in the Aerospace Department. In this capacity, he was responsible for the design of U-Biax and MOS memory systems. Mr. Jones joined the Memory Group at Palm Beach Gardens in 1969. His major effort to date has been in the area of MOS memories.

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Vendor	*Size*	*Speed*	*Op. power*	*(vol) cost/bit*	*Voltage Req'd*	*Comments*
Company #7	512x1	Access/cycle= 200/250 ns	0.293 mW/bit @ 5 MHz	10.¢ (Dec. '70)	+12V, +10V	Dynamic. Each word must be refreshed once/1.0 ms. High voltage T^2L interface, sense amp. req'd. Collector OR' capability. Chip select input provided.
Company #8	256x1	<200 ns	0.5 mW/bit	1971 (10k) 6.4¢ (100k) 5.4¢ (500k) 5.3¢ 1972 (10k) 3.6¢ (100k) 3.1¢ (500k) 3.0¢ 1973 (10k) 2.5¢ (100k) 2.1¢ (500k) 2.0¢	−18V	High voltage interface. Sense amp. required.
Company #9	256x1	Access=1 μs	1.56 mW/bit (typ)	Nov. '70 (5k) 4¢	−27V −13V −12V to −29V	Static. 4 chip selects decoded. Output inhibit with collector OR' capability. Inputs = high level T^2L, Outputs = T^2L. 24-pin package. Separate or common data inputs & outputs.
	16x4	Access=200 ns	6.0 mW/bit (max)	Nov. '70 (10k) 6.7¢	−27V −15V	Static. High voltage T^2L interface.
Company #10	256x1	Access=1.5 μs	1 mW/bit 50 μW/bit standby	Nov. '70 (1-24) 15.6¢ (25-99) 12.7¢ (100-499) 10.0¢ (500-999) 8.6¢ (10k-24k) 5.5¢	+5V, −10V, −7V	Static, T^2L interface. Chip select provided. Collector OR' capability.
Company #11	16x16x1	Access=80 ns	1.2 μW/bit standby	1971 (high volume) 2.5¢	5 to 12V	CMOS, static, nondecoded. High noise immunity. 38-pin package. Samples avail. First quarter '71.
	256x1	Access=200 ns	1.2 μW/bit standby	(high volume) 2.5¢	4.5V to 12V	CMOS, static, current sense. 18-pin package. Fully decoded. T^2L compatible. Samples avail. Second quarter '71.
	256x1	Access=450 ns	1.2 μW/bit standby	(high volume) 2.5¢	5V to 12V	CMOS, static. Voltage sense. Fully decoded. Samples available. Second quarter '71.
Company #12	256x1	Access=1.5 μs	1 mW/bit	Dec. '70 (100) 10¢ (10k) 5.9¢ 1971 (100k) 4.3¢ 1972 (100k) 3.5¢	+5V, −10V, −7V	Static, T^2L interface. Chip select provided. Collector OR' capability.
	1024x1	Access/cycle 390/580 ns		Dec. '70 (100) 2.5¢ (10k) 1.5¢ 1971 (100k) 0.9¢ 1972 (100k) 0.7¢	+5V, +20V. +17V	Similar to Company #4 1024x1 device.

Notes:
Prices and data presented were obtained from vendors and are subject to change.
For additional information on the products listed, contact the author.

Low Cost

The low cost potential is inherent in the integrated-circuit technology and is directly related to rapidly improving wafer-processing techniques. The price of IC's has been decreasing at the average rate of 50% per year. This low cost potential is even more apparent in MOS integrated circuits for the following reasons:

1) A much higher density of devices can be achieved per unit of chip area than can be achieved with conventional bipolar devices. This is because an MOS transistor requires one square mil of chip area whereas a bipolar transistor requires 25 to 35 square mils.
2) The MOS devices, enhancement type, are self isolating and therefore require no special provisions to insure isolations between adjacent devices.
3) The MOS device requires only one (relatively less critical) diffusion; bipolar devices require two or three. Thus MOS IC's require fewer processing steps than bipolar IC's.

Size and weight

The size and weight advantages can be illustrated by one commercially available MOS dynamic RAM, which consists of 1024 bits of storage in an 18-pin dual in-line package. This can be compared to a 160×9-core buffer memory in which the memory stack alone fills two card positions. Another example is a bipolar-MOS hybrid memory system. This memory consists of 147,456 bits of storage on a 7.9×8.8-in. card. The card contains all the necessary memory electronics except the power supply. In contrast, the core memory module used in Spectra 70/60 main memory contains 131×9 kilobits of storage. The physical dimensions of the 70/60 module are 20×7.5×21 in. The same memory module, made with the bipolar-MOS card mentioned, would be approximately 5.5×8.8×8.9 in.

Power dissipation

The power dissipation per bit for MOS memories varies extensively depending upon the cell and system design. Extremely low dissipation per bit can be achieved with a CMOS cell design, but the cells require so much chip area that relatively few bits can be placed on a chip. A static PMOS cell consists of four MOSFET's connected as a flip flop. A dynamic PMOS cell differs from the static PMOS cell in that the dynamic cell requires only three MOSFET's per cell and the charge on the gate to substrate capacitance of one of the devices determines the state of the cell. This charge must be refreshed periodically to keep the cells in the correct state. At a chip level, the arrays made with static cells dissipate more power than those made with dynamic cells; but the power dissipation should really be compared on a system basis, since the dynamic memory requires extra support electronics to manage the refresh operation. A hybrid memory is one that combines the low power advantages of MOS storage cells with the fast switching capabilities of bipolar decoders and sense circuits. The bipolar support circuits improve the performance of the memory, but at the cost of increased power dissipation.

Reliability

The reliability of semiconductor devices is high because the silicon junctions in the devices have no known failure mechanisms over the full range of normal operating conditions. Tests indicate that integrated circuit reliability is almost independent of the number of devices in the circuit. Since the MOSFET allows high component density per unit area, the MOS integrated circuit should provide highly reliable performance. The major sources of MOS integrated circuit failures are the metalizations, oxides, and bonds.

Disadvantages

The major disadvantages of MOS memory systems today are as follows:

1) Very little standardization has evolved in the field of MOS memories (Fig. 1). Thus, it is difficult to obtain second sources for many of the MOS arrays. This problem should be solved as customer usage begins to define the standards.
2) Data retention is a problem in case of power failure. The question that a system designer must answer is whether his system can tolerate this loss of data each time a power failure occurs. A possible solution is battery backup.
3) A learning period is required for the memory systems designer, since MOS memories are a new technology. He will need to carefully weigh this new approach to memory design against the classic approach and select the best storage medium for his new designs.

Survey of MOS memory arrays

Some currently available MOS memory arrays are compared in Fig. 1. The capabilities of the available products vary extensively. The performance of the MOS-bipolar hybrid memory system equals or exceeds that which could be achieved by building up a memory array of equal size with any of the other available MOS memory chips. The cost per bit appears higher for the MOS-bipolar hybrid memory than for the 1024-bit dynamic memory chips, but the two approaches really must be compared on a system basis.

The dynamic memory chips (from Companies 4 and 6, Fig. 1) are the most desirable component building blocks for main memory storage. The cost per bit is low because the number of bits per chip is high. Also, the large number of bits per package reduces the system complexity and increases the system reliability. The power dissipation per bit is less at the chip level for the dynamic memory chips than for the static memory chips.

The 256-bit static memory chips offered by Companies 4, 2, and 10 are pin-compatible memory arrays. These arrays are useful in small buffer memories where access time may exceed 1.5 μs. Because they are static and T^2L compatible, their application is straightforward. Their use is limited to small memories because of their high power dissipation per bit and because (with so few bits per chip) a prohibitive amount of support electronics would be required for a large memory.

Possible design approach

A block diagram for a 4k×18 main memory module is shown in Fig. 2. The storage devices used are 1024×1, dynamic memory chips; 72 memory chips are required for this module. The timing and control logic is designed to make the memory appear as static as possible. The input control signals from the processor, entitled READ and WRITE, initiate the

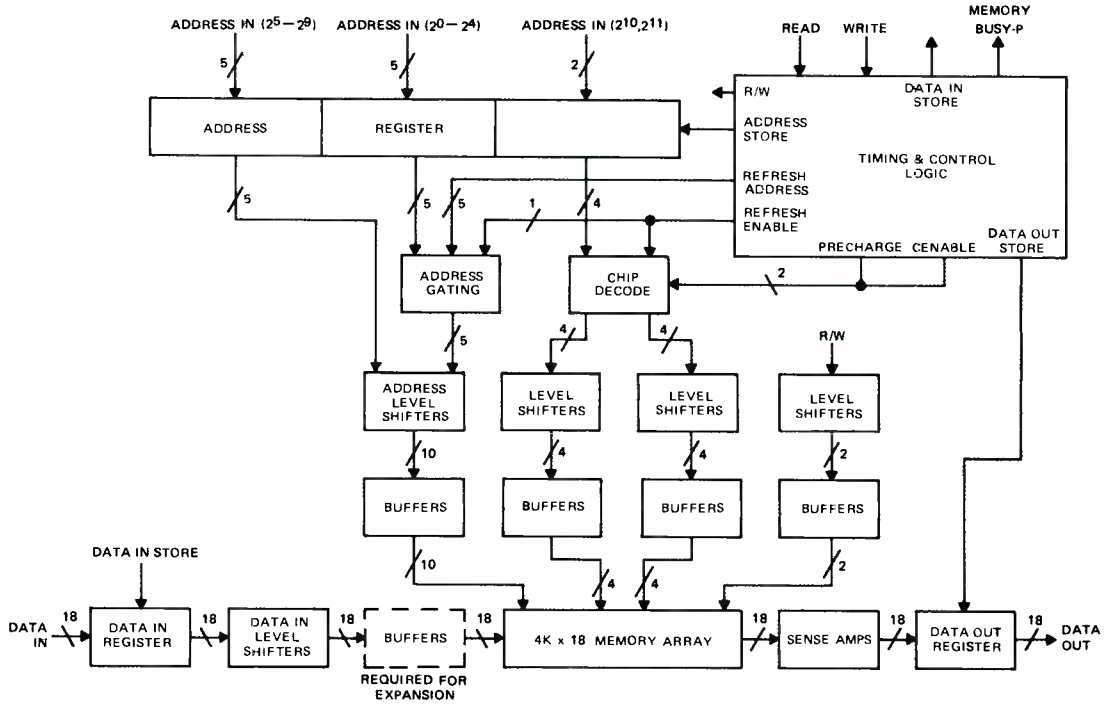

Fig. 2—Possible design approach—a 4k×18 main memory.

read and write cycles, respectively. A refresh cycle is automatically initiated every 60 μs., if the memory does not already have a cycle in process. If a read or write cycle is being performed when a refresh request is made, the refresh will be performed only after that cycle has been completed. When a read, write, or refresh cycle is initiated, the memory busy signal that goes from the memory to the processor changes to its true state. The processor will then lock out all memory requests until the memory busy becomes false.

The memory module receives 18 bits of data and 12 bits of address from the processor in addition to the read and write signals. This address and data information is shifted into the address register and data-in register when the address store and data-in store, respectively, becomes true. The data-out register supplies 18 bits of output data from the memory to the processor each time the data-out store goes to its true state.

Level shifters are required to provide the proper voltage swings for all signals that go to the MOS memory chips. In addition, high current buffers must be used for all inputs to the memory array except the data input terminals, to charge and discharge the input capacitance. These buffers have active pull-up and pull-down capability to minimize the rise and fall times of the input signals.

The address gating circuit serves to multiplex the refresh address in as address bits 2^0 through 2^4 at refresh time. Refresh enable is the control signal for this operation.

The chip decode circuit decodes the two highest address bits and activates the precharge and cenable control inputs of only one out of the four blocks of 1k×18 memory bits. The precharge input is decoded as well as the cenable input to minimize the power dissipation of the memory.

The sense amplifier must be capable of detecting a signal with minimum amplitude of 50 mV. The sense amplifier used in this design has an uncommitted collector output and has an enable input which makes memory expansion simple to achieve.

The cost of the memory at this writing would be 1.11¢/bit for a volume of 560 modules. The cost of the memory exclusive of the memory chips is 0.33¢/bit. Since the memory chips are projected to cost 0.5¢/bit by the 3rd quarter of 1971, this module should cost approximately 0.8¢/bit at that time.

The module power would be 42.2 watts, worst case, which is approximately 0.57 mW/bit. The access time would be 540 ns. with a cycle time of 650 ns. The time required for refreshing will result in a 1% loss in processor time.

The memory could be packaged on 6 standard plug-ins, 5.6×5.0 in., but a more desirable packaging scheme could probably be achieved by using a board similar to the one used for the RCA "lean mama" core memory, 10×12 in. The larger plug-in would allow the buffers, level shifters, and storage elements to be located on the same board. This would keep these high voltage swings off the connector and back plane and thus minimize the system noise.

Conclusions

The new challenge facing the memory system designer will be to decide when and how to apply this new technology. He must carefully weigh each of the considerations mentioned earlier with his particular design requirements in mind. In light of the projections now being made for MOS memory in the next few years, cost and reliability considerations will make an MOS design desirable for many applications.

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1. *Integrated Circuits*, Notes from Engineering Summer Conference, University of Michigan (June 1970) pp. 17, 18.

Research in optical memories

Dr. J. A. Rajchman

The inventions of the laser and holography have permitted us to conceive a mass memory with capacity measured in gigabits that can be written-in and read-out at electronic speeds and which, at the same time, provides permanent records for archival shelf storage. This "optical memory" operates without any mechanical motion and approaches a long-wished-for ideal all-electronic mass store. In the last two years we, at RCA Laboratories, have been able to devise a solution for every physical means required to realize this memory concept, and also to comprehend the main limiting factors. We believe that we are engaged in a research venture of enormous potential payoff: it may well provide the most significant hardware advance in the architecture, operation, and economics of data processing systems. This paper is a short account of the concepts, the progress, and the expectations.

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received the Diploma in Electrical Engineering in 1934 and the degree of Doctor in Technical Sciences in 1938 from the Swiss Institute of Technology, Zurich, Switzerland. He joined RCA in 1935, and has been engaged in research since 1936, first in Camden, N. J., and since 1942 in Princeton, N. J., with the RCA Laboratories. In 1961, he became Director, Computer Research Laboratory; in 1967, Staff Vice President, Data Processing Research, and in 1969 was appointed Staff Vice President, Information Sciences. He is responsible for directing a number of exploratory ventures in the information sciences as well as assisting RCA Laboratories management in guiding RCA's overall program in this and related fields. He first worked in electron optics and is directly responsible for the development of the electron multiplier tube. Later, he worked on the betatron for which he became co-recipient of the 1947 Levy Medal of the Franklin Institute. During World War II he was among the first to apply electronics to computers. After the war he worked chiefly with memory devices for computers. He developed the selective electrostatic storage tube, the magnetic core memory systems that are now standard in modern computers, a number of magnetic switching circuits, the transfluxor, the ferrite aperture plate memory, and the transfluxor controlled display panels. He is responsible for a broad-spectrum program of research in digital computers involving magnetic, cryoelectric, semiconductor and optical techniques, input and output devices, computer theory, computer applications and automated design. Dr. Rajchman received the 1960 Morris Liebmann Award from the IEEE "for his contributions to the development of magnetic devices for information processing". Dr. Rajchman is a Fellow of the IEEE, and the American Association for the Advancement of Science; a Member of the American Physical Society, the Association for Computing Machinery and Sigma Xi. He was elected to the National Academy of Engineering in 1966. He holds 105 U.S. Patents, and is the author of many technical papers.

Editor's Note: This paper was written and submitted for publication early last year but was not used at that time because of its relevance to several of the product-oriented papers in this issue. Although the material in this paper is still correct and provides a good insight into optical memory research and development, several papers have been published in the interim reporting additional information of value. Interested readers are referred to:

Rajchman, J. A., "Promise of Optical Memories," *Journal of Applied Physics* Vol. 41 (Mar. 70) pp. 1376-1383.
Rajchman, J. A., "An Optical Read/Write Mass Memory" *Applied Optics* Vol. 9, No. 10 (Oct. 1970) pp. 2269-2271.
Cosentino, L. S., and Stewart, W. C., "Optics for a Read/Write Holographic Memory" *ibid* pp. 2271-2275.
Mezrich, R. S., "Magnetic Holography" *ibid* pp. 2275-2279.
Keneman, S. A., Miller, A., and Taylor, G. W., "Phase Holograms in a Ferroelectric Photoconductor Device," *ibid* pp. 2279-2282.

STORAGE of large amounts of information that can be manipulated electronically is the basis of all modern data processing systems. This is accomplished today by a hierarchy of storage devices: punched cards, reels of magnetic tape on one end, through magnetic card memories, magnetic disk packs, drums, extended core, main core, film or wire memories, and semiconductor memories, to registers within the processor on the other end. Typical storage capacities and access times of most commonly used storage devices and memories are shown on Fig. 1. Although, remarkable information systems are being designed with the proper combination of large and slow with small and fast storage devices, the state-of-the-art has many shortcomings. Large storage capacity is obtained only in devices with mechanical motion—making them not only slow but, as it turns out, relatively expensive, bulky, and unreliable. The hierarchical organization has a considerable price. It entails great loss of time in block transfers between memories with wide disparity of sizes and speeds, a loss of time particularly severe when randomly searching a large file. There is need for elaborate software for internal housekeeping, which, in addition to its own high cost in intellectual effort, requires "overhead" storage capacity often preempting much of the memory's capacity.

An ideal, instinctively wished for by many since the very inception of electronic computers, is a single electronic random-access memory or some other, perhaps optical, nonmechanical equivalent, which would replace the hierarchy and greatly simplify the architecture and operation of data processing systems. Just how large would such a single unit have to be to really accomplish this? The minimum useful capacity can be estimated to be as low as 10^9 bits, but for the purpose of a goal it is safer to assume 10^{10} bits —a size corresponding to about 200 10-disk-pack stations or 200 tape stations (each with a 2400 foot reel, 800 bytes/inch, 25% utilization). The exact capacity that is meaningful to aim at first, as well as the range to which it should be extensible, will depend, of course, on the usual trade-offs of accessibility, cost, initial completion date, etc.

To replace a large portion of the present storage hierarchy, as depicted in

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Fig. 1, the proposed idealized mass memory, besides having a sufficient capacity, must have some provision for storage extensibility and adequate effective speed to match the processor.

Principle of the proposed optical memory

The memory is based on three concepts: 1) compounded selection, 2) holographic storage on an erasable medium, and 3) an internal electrically- and light-addressable storing-matrix array. Random-access addressing is split into two parts: selection within a block of bits or a page of $P=w.d$ bits, and a selection of one out of $N=x.y$ pages (see Fig. 2).

Write mode

For writing, first a page is electrically "composed" in an array of $P=w.d$ storing cells, each associated with a light value which lets light through or shuts if off according to the state of the cell (Fig. 2). Next, coherent light from a laser impinging on the array, and thereby patterned as an object beam carrying an optical equivalent of the page information, is caused to interfere with a "write" reference beam W at some particular location of an extended storing medium. The particular location of coordinates x, y is selected by the direction of illumination of the page composer and is obtained by deflecting the laser beam in two directions at right angles proportional to x and y, respectively.

A hologram of the page is now recorded on the storage medium. This medium is light sensitive and can be selectively erased; that is, any selected area comprising a page can be erased and used for subsequent write-ins.

Read mode

To read out any desired storage hologram page, a "read" reference beam R is directed on it. If the direction of that beam R is conjugate to that of the writing beam W, the real image will appear precisely on the page composer by reflective diffraction. Exactly the same size image could be made to appear at a symmetrical position on the other side of the storage medium. These two readout images appear always at the same location irrespective of the location of the hologram. An array of photosensors of exactly the same size, and with exactly the same number $P=w.d$ of sensors as the page composer, can be placed in either position to read out the information.

Storage element

The proposed optical memory would use the reflectively diffracted images and superpose the sensor array on the page composer. This leads to an array of elements each comprising

1) A one-bit electric storage cell, such as a flip-flop, which can be set electrically through coincidence of W and D signals;
2) A light valve controllable by the cell; and
3) A photosensor capable of setting the storing cell.

We dubbed this array LATRIX (light accessible transistor matrix) as the most likely implementation will involve transistor integrated circuits.

Feasibility of the optical memory

There is real promise in the three concepts for the realization of the mass memory idealized above for the following reasons:

1) High storage density
2) Economy of addressing circuits
3) High-speed access capability
4) Extensibility to higher capacities

High storage density

Storage is obtained in an unstructured continuous medium in which very high bit-storage density (inherent in optical techniques) can be realized by holography by simple means without demagnifying lenses and alignments of high precision. Densities of more than 10^6 bits/cm^2 can be achieved with practical optics, and the theoretical limit due to diffraction is more than an order of magnitude higher. Therefore, 10^{10} bits can be stored on a fraction of a square meter—an area small enough to be accessible by a deflected light beam. Areas of many square meters would almost dictate mechanical motion of the medium. Furthermore, the redundancy of holographic storage allows considerable tolerance in the perfection of the storing medium. It is sufficient to demand that the imperfections do not impair completely areas of the order of the page, that is of the order of a mm^2, while imperfections as big as many tens of microns can be tolerated. This tolerance is in contrast to the perfection required from the surfaces of disks or

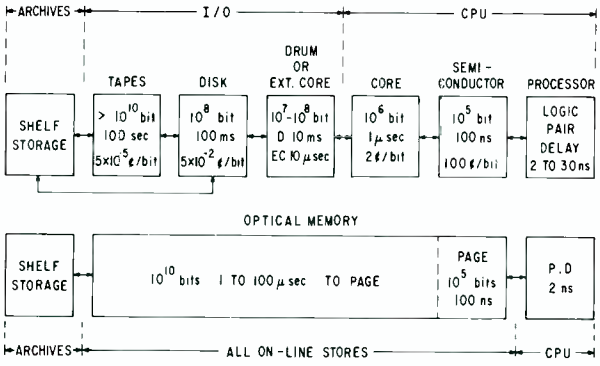


Fig. 1—Present hierarchy of storage devices and memories contrasted to possible use of proposed optical memory.

tapes, which cannot tolerate imperfections of the size of a single bit.

Economy of addressing circuits

Compounded access selection of the page and bits within the page, has the effect that each bit is selected by quadruple coincidence (w, d, x, and y). This leads to great economy of addressing circuits, as $(w+d+x+y)$ circuits give access to $w.d.x.y.$ bits. For example, if $w=d=x=y=2^8=256$, $w.d.x.y.=2^{32}\approx 4.3\times 10^9$ so that only about a thousand circuits are necessary to access several billion addresses.

The LATRIX (or page composer and sensor array considered separately) is (are) composed of $w\times d$ elements, which must all be perfect, with no single tolerable defective element as is the case in conventional random access matrix memories. Similarly, the page deflection has to be perfect in the sense that it must be reproducible (but with some tolerance, as any part of the page hologram reached by the beam will read out its full content). However, the key point is that whatever skills are deployed to make a large LATRIX are multiplied by, not merely added to, whatever skills are deployed to achieve a large deflection array.

The net result of compounded selection and holographic storage is that the number of accessible bits on a not-necessarily-perfect continuous medium is proportional to the fourth power of the number of access chan-

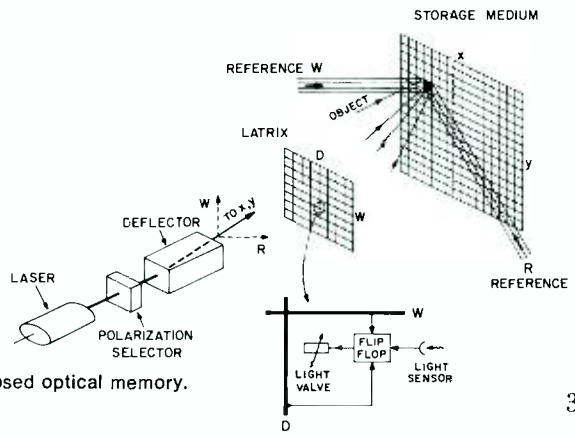


Fig. 2—Principle of proposed optical memory.

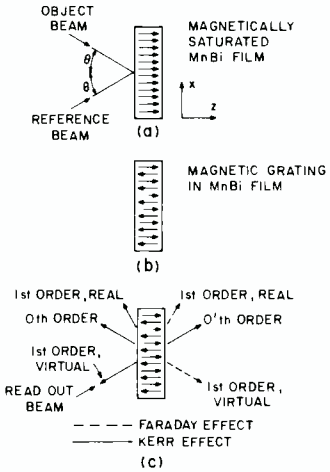


Fig. 3—Magnetic holography: (a) situation for writing a hologram; (b) magnetic state of formed hologram; (c) readouts using Faraday and Kerr effects.

nels, whereas the number of elements that must be fabricated with perfection is related only to the square of that number. In our example, there are about a thousand access channels, and a LATRIX of about 65-thousand perfect elements controlling more than 4-billion elements stored on a not-necessarily-perfect medium.

High-speed access capabilities

Admittedly, the proposed optical memory has an internal hierarchy resulting from splitting the address into selection of a page and a selection within a page. In reading, access to any word or bit is random or, more exactly, pseudorandom since the time between consecutive readouts can be shorter if they are within the same page than if the additional time to access different pages must be added.

Writing on the other hand, requires that a whole page be composed before it can be holographically recorded. When the page composer and sensor array are separate, random writing of a word or a bit requires that the contents of the page at the selected page address be read out into a buffer memory by scanning words or bits and then rewriting from the buffer, by similar scanning, into the page composer changing only the desired word or bit. This is a lengthy operation which it is tempting to avoid.

The physical combining of the page composer, sensor array, with an internal memory into a LATRIX, makes writing of a word or a bit essentially random. Indeed to write a word or bit, the contents of the desired page at the desired address are first read into the LATRIX by a single parallel exposure of all its sensors, then (or simultaneously) the input word or bit is written in electrically at the desired LATRIX address, and finally the contents of the LATRIX are rerecorded by a single parallel exposure of the whole LATRIX. This procedure, replacing lengthy scanning by single-shot parallel transfers, renders writing of a word or bit essentially random—or pseudorandom as with reading, since somewhat faster access is possible for two consecutive write-ins in the same page than in different pages.

The concept of the LATRIX has a much wider implication than allowing pseudorandom writing within the entire memory. The LATRIX contains a high-speed electrically addressable memory, which with its light valves and sensors disabled or else in the dark, can be used as any conventional memory, and in particular as the main internal memory of the computer. The situation can then be viewed as follows: The computer operates normally in and out of memory. When it runs out of writing capacity, its content can be "photographed" instantly into a holographic record at any chosen location, and it becomes free to accept more information. Similarly, this memory can be filled instantly by a single exposure of any desired hologram. The situation is somewhat similar to that of a high-speed semiconductor "cache" memory combined with a core memory, with the essential differences that transfers from LATRIX-to-hologram are single-shot events with myriads of parallel optical paths operating simultaneously while cache-to-core transfers are through scanning of words.

If the response times of the photosensors and light valves, the deflection time, as well as the permitted repetition time between successive laser pulses, are as short as the time required to access electrically a word in the LATRIX, the total access time to any word in the entire memory will vary only two-to-one between the cases involving and not involving a transfer from or to holographic storage. In that case, the entire memory is pseudorandom or truly random at half the speed of its fastest part. It represents then, the idealized memory postulated.

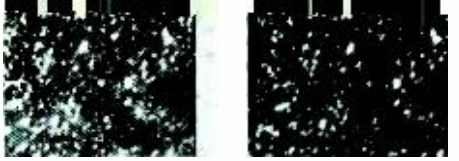
It is very likely, however, that with the first techniques that may provide a realistic implementation of the optical memory, the response time of the light valves and the minimum time between pulses of laser light will be two to three orders of magnitude longer than the access time of a word within the LATRIX (and the deflection time will be several times longer than that access time). Under these circumstances, it may not be advantageous to combine the page composer and detecting array into the LATRIX. In any case, the optical memory becomes a more conventional mass store. Its merits, besides the elimination of all mechanical accessing, will depend on just what the page size and page access time are; on the fact that the mass store has its own internal buffer; and on the overall cost. We believe that these merits will be sufficient, as compared to disk memories, to justify an optical memory product. We are convinced also that techniques will be forthcoming that will shorten all the limiting times and lead to the more ideal memory. There is thus room for gradual evolution.

Extensibility to higher elements

Finally, consider the extensibility to higher capacities. For on-line processing, the optical memory is sufficient by itself for a majority of users, if its capacity is greater than some critical value—estimated to be about 10^{10} bits. On-line processing requiring more capacity can simply use more units or bigger ones in an obvious extension involving well-known tradeoff advantages and disadvantages. Extensibility of archival capacity is very simple, as the plate carrying the erasable medium can be removed for shelf storage and another unit inserted instead. This operation is much simpler than that of changing reels of magnetic tape and may involve bringing in about two orders of magnitude more information.

Implementation

A great deal of work has been reported in recent years on light deflection, light modulation, storage media, detector arrays, holographic techniques, and improvements in lasers. Also, several read-only memories[1-6] with compounded selection and holographic storage have been described, as well as a proposal for an optical memory with read-write capability similar to the present proposal in many respects. We will discuss in order: deflection of the beam, the erasable medium, the LATRIX, and the total optical system.



HOLOGRAPHIC GRATING AFTER ERASURE PULSE

Fig. 4—Photograph of film of MnBi: (a) recorded hologram, (b) erased hologram.

Deflection

Deflection of a light beam by nonmechanical means has been achieved chiefly in two types of devices: electro-optic and acousto-optic. Electro-optic deflecting devices depend on the rotation of the plane of polarization that occurs in certain materials, typically KDP, as a result of an applied electric field. A 90° change in direction in polarization can be translated into a displacement of the beam by several means, notably by birefringent crystals, such as calcite, through which the ordinary ray passes undeviated while the extraordinary ray is displaced parallel to the ordinary ray. A cascade of stages with displacement proportional to increasing powers of two are used in both x and y directions. Random access to 256×256 positions in $10\mu s$ was reported.[8] The approach is promising, since it depends on purely electronic phenomena that are capable of submicrosecond response, but so far there are difficulties in obtaining adequate crystals of sufficient size, efficient transmission through multiple elements, sufficient contrast, and in keeping power requirements to practical levels. Progress toward electro-optic deflectors of high speed and resolutions is to be expected from active work in many laboratories.

In an acousto-optic deflector, an acoustic wave through a transparent solid or liquid produces periodic variations in index of refraction and thereby a grating that can deflect light by diffraction. The acoustic wave is generated by a transducer whose frequency controls the grating spacing, and thereby the deflection. Two successive devices at right angles provide the x and y deflections. There is a number of inherent tradeoff relations between the number of resolvable deflected spots, the access time, the ratio of transmitted-to-incident intensity, and the power requirements. With water, deflected arrays of 16×16 with access time of $6\mu s$, 80% light transmission efficiency, and only one-watt power requirement are typical and much higher resolution has been reported in the literature.[9] However, sound absorption limits the center frequency to about 30 MHz which results in milliradian angular deflections requiring very large throwing lengths. In solid alpha iodic acid[10] and lead molybdate crystals, frequencies up to 1 GHz can be used, resulting in angular deflections of 7°. Reported results include a 64×64 deflected array accessible in $2\mu s$[11]. At the Laboratories, we have gained enough proficiency to duplicate published results and have also devised a number of original improvements. Much progress can be expected from better materials and ingenious device designs aimed at improving upon possible tradeoffs.

Deflection of light is the object of intensive research in many laboratories, and there has been great progress in recent years. The acousto-optic approach is leading at present, but the purely electronic, electro-optic, as well as magneto-optic approaches have a greater speed potential. In any case, it is not unrealistic to think of arrays of 256×256 or even 1024×1024 reachable randomly in $1\mu s$. The location reached in electro-optic (or magneto-optic) deflectors depends solely on the geometry of the crystals, not on the exact values of control voltages (or currents) and therefore it is easy to guarantee reproducibility of deflection. Reproducibility is also easy to guarantee in acousto-optic deflection as it depends on frequency, the most easily controllable analog quantity which can also be digitally synthesized.

Erasable medium

Read-write operation requires an erasable medium. We have studied four approaches: photochromics, thermoplastics, ferroelectrics, and magnetic films. All are possible candidates for the proposed memory. We have found, however, that the magnetic film is the most promising at present, and have devoted most of our recent efforts to it. We have developed films of manganese bismuth, *MnBi*, which were first described for non-holographic bit storage,[12] to give us hologram storage with all the qualities of permanence, indefinite reversibility, high resolution of thin-storing medium, the convenience of writing and erasing by the same beam, and relatively high speed.[13]

Thin films, about 700 Å thick, of manganese bismuth, *MnBi*, are deposited on a substrate with their C-axis normal to the surface.[13] In operation, the film is first magnetized to saturation, normal to the surface over the entire area. To write a page, the selected area is exposed to an intense pulse of light carrying the holographic pattern (see Fig. 3). Absorption of light in the film creates a corresponding temperature pattern. With a sufficiently intense light, the illuminated regions are heated over the Curie temperature and consequently lose their magnetism. Upon cooling, these regions, in the presence of the demagnetizing field of the adjacent unheated regions, become saturated in a direction opposite to that of their neighbors. The hologram is now stored permanently in terms of a magnetic pattern, until the region is deliberately erased. To read, light from a reference beam is directed on the magnetic hologram. The light transmitted through the film experiences a phase variation corresponding to the magnetization pattern as a result of the Faraday effect. Therefore, the magnetic hologram behaves as an ordinary phase hologram and is reconstructed without the need for polarizers or analyzers. The light reflected from the film also acquires phase variations, as a result of the Kerr effect, and similarly yields a reconstructed image.

To erase a particular hologram at a specified x-y location without erasing any other holograms, a very strong, well-localized magnetic field could be used. It is much more convenient, however, to illuminate the particular hologram by a reference beam and uniformly heat it over the Curie temperature. Upon cooling, it will assume a direction of saturation dictated by the direction of a field that can be much smaller than the coercive field which therefore can be present over the whole array without erasing any other hologram.

The successful recording of the holograms by Curie point writing depends on a very intensive and short pulse of heat such that the illuminated regions exceed the Curie temperature, which is 360°C for *MnBi*, and yet such that the non-illuminated regions remain well below the Curie temperature despite their sub-micron close proximity to the hot regions. It was found[13] that 15-ns pulses with an energy of 2×10^{-4} joules/mm^2 produce good holograms. Their existence proves spacings between regions of reverse magnetization of about half a micron (or 1000 lines pairs/mm). The photographs[13] of Fig. 4 made in a polarizing micro-

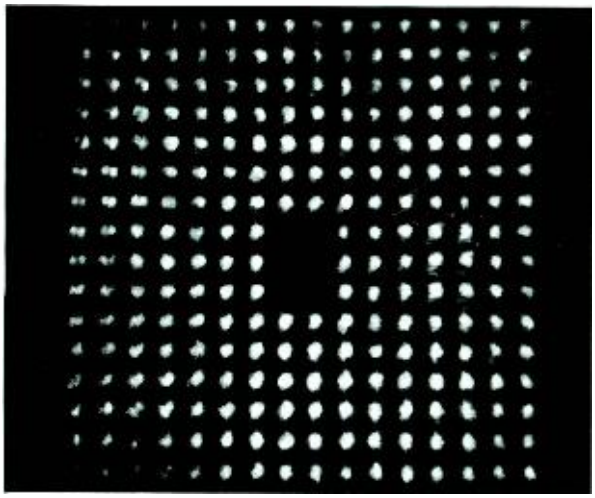


Fig. 5—Image readout from magnetic hologram representing an array of 16 x 16 dots with 250 "ones" and 6 "zeros".

scope show a typical *MnBi* film with its holographic gratings as well as the effect of erasure. Fig. 5 shows a reconstructed image from a magnetic hologram representing a 16×16 pattern of dots, with 6 spots black and 250 white. The reconstruction is faithful, despite the defects of the film apparent on Fig. 4, illustrating the redundancy of holographic storage.

How reasonable is the requirement for high instantaneous power for Curie point writing of holograms? Combining the requirement of 2×10^{-4} joules/mm^2, with a maximum allowable illumination time of 15 to 20 ns, and fundamental bit densities attainable with reasonable aperture in attendant lenses which turns out to be about 2×10^4 bits/mm^2, the peak power required turns out to be about one watt/bit. This means that page composers of 10^4 bits require an instantaneous power of 10 kW, a power peak which is becoming available at reasonable repetition rates. However, reasonably high repetition rates with larger pages will result only from significant reduction in peak power requirements.

The efficiency of readout through the Faraday effect was found to be 0.001% and through the Kerr effect to be 0.01%. Despite this low efficiency of the Kerr effect, the energy required in the readout beam to give a ten-to-one signal-to-noise ratio on the photodetectors turns out to be 2×10^{-6} joules/mm^2 or 100 times less the energy needed for writing. Considering also that readout need not be limited to 20 ns but can occur over any time tolerable in operation, such as 1μs, the readout power can be 3 to 4 orders of magnitude less than the write power. Consequently, there is no danger of heating the *MnBi* film over the Curie temperature on readout, and indefinite nondestructive readout is possible.

Latrix

The LATRIX is a physical combination of an array of photosensors, a transistor memory, and an array of light valves (i.e., a page composer). Practically all work was devoted thus far to these three devices separately.

Photosensitive readout arrays have been developed for holographic read-only memories. In these memories, a particular one of an array of permanently made hologram pages is illuminated by a deflected laser beam, or by the illumination of one light-emitting diode in an array, and the reconstructed image appears on the photodetecting array. For fast operation, rapid response of photosensors and rapid selections of words within the array are desired. Integrated arrays of photodiodes and switching diodes have been reported[14] to give a full cycle time of less than 1μs with illuminations less than one microwatt /bit. Improved integrated silicon arrays 16×16 were recently reported[15] using PIN photodiodes in combination with MOS selecting switches in which the readout time was reduced to as much as 100 ns. In this array, the light energy required per bit was 10^{-13} joules, with 300-ns readout, which is only about ten times more than the absolute minimum required by signal-to-noise considerations.

In these arrays, there is no bit storage, and the electrical signals produced by light must be large enough to be easily distinguished from the switching signals. When the photosensor array is combined with a transistor memory, it is only necessary for the light-produced signals to set a flip-flop. Since local-per-bit amplification can be used, higher sensitivities can be expected than in non-storing switched sensor arrays. The present integrated silicon technology makes it very reasonable to expect that the addition of a photosensor, such as a phototransistor, and possibly another local amplifier to every bit of a transistor memory can be accomplished without any change in technology other than more complex artwork. In fact, we have made (in cooperation with Defense Microelectronics in Somerville) small samples using the MOS technology.

As far as the transistor memory itself, one can simply depend on the semiconductor industry which is gearing itself toward the memory market and expects in a few years to challenge magnetic memories with low-cost/bit memories of large capacity. These expectations need only be realized partially to still make the modified transistor memory LATRIX economically justifiable as the main memory, since, in effect, its value is multiplied manyfold by its power to access myriads of holograms.

The page composer is, at this time, the least well developed; indeed a simple fast light valve is conspicuously lacking among the many versatile electronic devices that can be used by the thousands. Electro-optic, magneto-optic and liquid crystals offer the best avenues. Ferroelectric materials in crystalline (e.g., barium titanate) and ceramic (e.g., lead-zirconium-titanates) forms combine storage properties with a strong electro-optic effect; applications as storing light-valves have been reported.[16,17] Unfortunately, ferroelectrics are prone to depoling effects and fatigue and, furthermore, their electro-optic control tolerates an angular variation of the incident light which is so small as to greatly complicate their use as a page composer. Magnetic materials such as yttrium garnets and orthoferrites, tolerate larger angular incidence variations, but operate in the red and infrared only. Moreover, there are considerable technological difficulties in combining electro-or magneto-optic devices with silicon devices.

The recently described[18] electro-optic effect of dynamic scattering in nematic liquid crystals is most likely to give the first solution for a page composer than can easily be incorporated in a LATRIX. In nematic materials—which have rheological properties of liquids but optical properties of crystals—rod-like molecules are in parallel alignment and the material is transparent. Upon application of an electric field, the molecules rotate, and the material scatters light. Therefore, within a given solid angle of observation, the light can be made to vary by a large factor. Using this principle, a liquid crystal matrix display has been reported[18] in which electronic control

of the elements was demonstrated. It should be possible to apply the nematic liquid directly on integrated circuits. This would provide a very attractive LATRIX in most respects except for speed. The response time of liquid crystals is measured in milliseconds.

Memory system

A possible optical memory is shown schematically in Fig. 6, which illustrates total operation of the system. Light starts from a laser which can deliver a high instantaneous power. It passes through a polarizer, such as KDP, which can be set electrically to one (*W*) or the other (*R*) of two orthogonal directions of polarizations. Next the beam is deflected by two successive acousto-optic deflectors in *x* and *y* directions. After a long throw, which can be compacted by folding mirrors or a multiface prism, the beam strikes a lens from which it emerges parallel to the lens axis for all angular incident angles. The beam strikes next a birefringent prism. If it has a *W* polarization, it goes straight through the prism and strikes a beam splitter. One part of the beam passes straight through, and, after two inverting lenses, strikes a "hololens". The other part is directed to the storage medium and provides the writing reference beam.

The hololens is a fixed hologram image of the LATRIX pattern which can be fabricated by bleaching a conventional photographic emulsion or by using dichromated gelatin.[20] Being a thick-phase hologram, it can diffract theoretically all of the incident light; efficiencies of 80 to 90% have been reported.[20] Furthermore, the hololens splits the diffracted beam into a myriad of beamlets precisely directed at the apertures of the LATRIX. Some of these beamlets are shut off by the LATRIX, and the others are concentrated by a lens into a small area of the storage medium. The location of that area is exactly symmetrical to that at which the beam strikes the hololens. The other part of the writing beam emerging from the beam splitter is directed to the same location on the storage medium through appropriate mirrors. It strikes the storage medium at the same angle as the beam strikes the hololens, and therefore there is perfect tracking of the object and reference beams for all *x*, *y* positions.

To write-in a hologram, the laser is first pulsed for a relatively long time (e.g., 100 ns) so that the entire area under reference beam and object beam illumination becomes heated over the Curie temperature and the previously recorded hologram is erased. Then the laser is shut off and the area is allowed to cool off in the presence of a small magnetizing field. Finally the laser is turned on for the short period of 15 to 20 ns necessary for Curie point writing.

To read, the polarizer is set to the *R* polarization direction, and the birefringent prism totally refracts the beam, which passes through appropriate mirrors and strikes the storage medium at the selected *x-y* position at an angle precisely conjugate to the angle of the writing reference beam. A real image of the desired page now appears on the LATRIX and is read out. Of course the intensity of the readout beam is reduced so as to not erase the selected page.

Conclusion

The concepts of holographic storage on an erasable medium and compounded selections offer, for the first time since the advent of electronic computers, a realistic approach to mass memory randomly accessible at electronic speeds and of sufficient capacity to be the sole on-line store. Sufficient progress has been made to visualize a complete system and to define most of the limiting factors. Therefore we are convinced that the optical memory can be made and we appreciate that this will take some time. We have no doubt of the enormous importance of such a memory and of its eventual realization. A shorter-range possibility is a read-only memory using an array of permanent holograms selected randomly by an acoustically deflected laser beam. We have made a unit of 64 pages of 256 bits that can be selected in one microsecond. An extrapolation from that small unit shows that practical memories with capacities of 10^8 to 10^9 could be built in the near future with sufficient engineering effort.

Acknowledgment

In this paper, the author has depended on many ideas and results contributed by a number of Members of the Technical Staff of RCA Laboratories, including G. A. Alphonse, J. J. Amodei, J. M. Assour, D. I. Bostwick, L. S. Cosentino, S. A. Keneman, W. F. Kosonocky, G. W. Leck, R. D. Lohman, R. S. Mezrich, W. C. Stewart, G. W. Taylor and D. H. R. Vilkomerson.

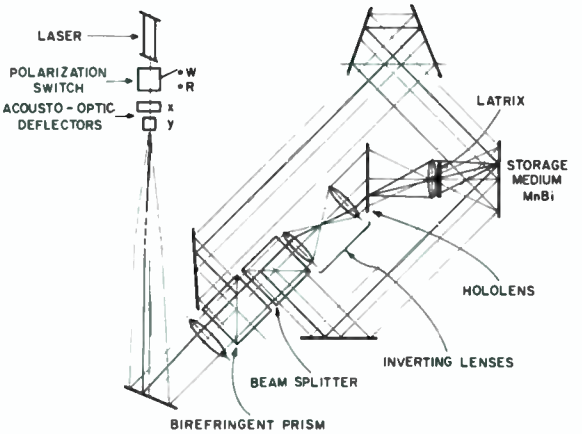


Fig. 6—Proposed optical memory.

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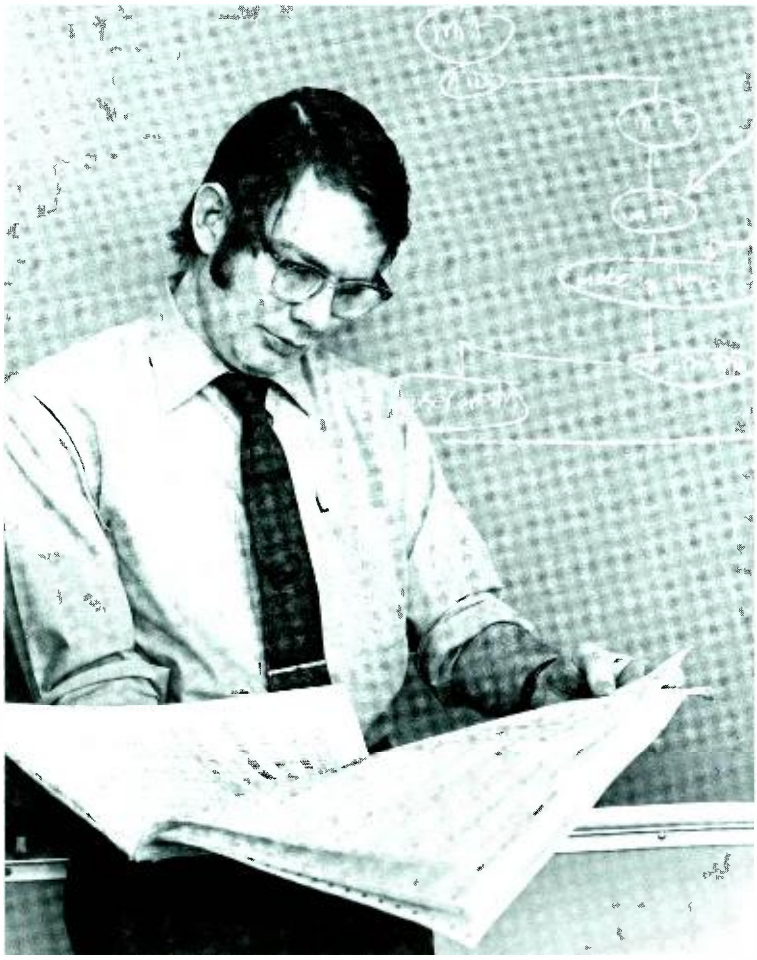
Data base for computer performance evaluation

R. O. Winder

The RCA Laboratories initiated a team project in 1968, generally aimed at predicting the performance of future computer system architectures being considered within RCA. The cache-system or slave memory idea was the principal subject of the project, and this has led to the most useful results within RCA. However, many other problems have been studied, and the data base that was collected has been found useful in analysis as well as prediction of performance, and in obtaining fundamental data for modeling purposes.



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received the AB from the University of Chicago in 1954, the BS from the University of Michigan in 1956, the MA and PhD from Princeton University (Mathematics Department) in 1958 and 1962. In 1957, Dr. Winder joined RCA at Camden and worked on a small computer design and automatic programming. Since joining the RCA Laboratories in 1958 he has investigated a variety of subjects in computer systems, logic, and circuit design, with main emphasis in threshold logic—both theory and application. He has published numerous technical papers and holds 13 U.S. Patents. His work in threshold logic and computer systems simulation was recognized by three RCA Laboratories Achievement Awards. In 1969, he was appointed Head, Computer Design Research. He has been visiting lecturer at the University of Pennsylvania, the University of California (Berkeley), Stevens Institute of Technology, Ohio State University, and LaSalle College. Dr. Winder is a member of the Association for Computing Machinery, the IEEE, Phi Beta Kappa, and Phi Kappa Phi.

THE approach taken in establishing a data base for computer performance evaluation is a conventional one, proceeding in three steps: First, a program was written to record, on magnetic tape, the instruction-by-instruction behavior of arbitrarily selected or "typical" programs. This trace program was then used to create a large collection of such *trace tapes*, spanning various RCA customer applications and language-translating activities. Finally, several analysis programs were written to read these tapes and provide appropriate simulation output, statistics, or profiles of program behavior. This paper emphasizes the trace program and library, with brief discussions of its applications.

Trace programs

The first trace program written has the following characteristics: It runs under RCA's principal batch system, TDOS (tape disc operating system), and is able to record about 2½ million instructions onto a reel of tape in about 15 minutes, representing about one-half minute of Spectra 70/45 real instruction-executing time. The trace program must be link-edited with the object program being traced, and only user-state instructions are recorded.

The information recorded (see Fig. 1) is as follows (instruction format is identical to the IBM 360 instruction formats):

1) The op-code half-word, which provides, besides the op-code, information on indexing, type of supervisor call, and lengths of data fields;

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2) The instruction's address (after indexing and base register calculations); and
3) The address of each data field accessed by the instruction—there may be 0, 1, or 2 such addresses, depending on the instruction.

In the case of a supervisor call, certain information appropriate for that call is recorded, such as the I/O command being issued with nominal buffer size, and the addresses of data used by that call. Since designing this trace tape format, no serious omissions were discovered; strongly data-dependent processor activity is fairly rare, and the effort required to trace the I/O activity beyond initiation still seems too great—hardware monitoring is being used instead.

The moderate slow-down of execution under tracing, only 20:1 to 30:1, is obtained by use of special hardware in the Spectra 70 computers—the test mode interrupt. This permits the trace program to inhabit one machine state (P2) while executing a user program in P1. The hardware in effect gives control back to TRACE after each single P1 instruction; the principal overhead incurred is in address calculation and making up the trace tape buffers. One consequence of using this technique is that the supervisor code, which runs in states P2 and P3, cannot be traced without great complication and slowing down of the tracing. Thus, the trace was not extended into P2 and P3, because the largest part of code under TDOS is executed in P1, and because the P2-P3 code was expected to change most drastically in future generations of computers anyway. Thus the occurrence of a supervisor call on a trace tape signifies a known hiatus—the next instruction recorded is the first subsequent instruction executed in the user state, P1. (There are also asynchronous gaps in the trace—servicing of I/O termination interrupts is not traced, nor is any record kept of a task-switch to another program; tracing is simply suspended until the original program resumes.)

The TDOS trace program also provides a mechanism for *skip tracing*: a series of recipes each specify an alternating sequence of n intervals of tracing with n intervals of running free. The interval durations are specified by two times given in each recipe. Essentially

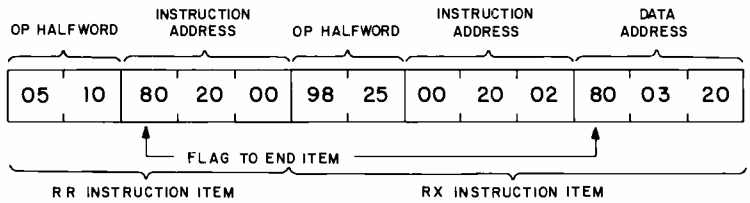

Fig. 1—Example of two instruction items on a trace tape.

no use of this facility was made in the studies completed so far, but experiments on recipes are being carried out now, and skip tracing will be used in the tracing of benchmarks. This program will be modified so that it runs as a program parallel to the subject program, to avoid the need for a link-editing step.

Recently, a trace program has been written which runs under RCA's principal time-sharing operating system, TSOS. It has been written in such a way as to run in a parallel multiprogramming slot, and provides output compatible with the TDOS trace. Virtual addresses are recorded. Because of internal properties of TSOS, an interactive job can be traced with no perceptible degradation in response time, but a compute-bound job is slowed down approximately 200:1. This trace program is also presently limited to P1 code. In this case this is a serious limitation; typically a user executes proportionately more supervisor code than he does under TDOS, especially in interactive jobs with large amounts of file-accessing and terminal I/O. This problem will be corrected, and trace programs will be written for new generations of RCA operating systems.

Trace library

Our collection of trace tapes has grown in a series of steps, each relatively ad hoc, in a general "dragnet" manner rather than by scientific sampling. That is, a wide representation of many different program types has been collected, without precisely weighing any given type by its frequency of occurrence in the field. In future work, with enhanced tracing programs, operational systems of various customer "arch-types" will be sampled randomly. One advantage of our dragnet approach is that data needed for unanticipated experiments is often to be found already present in the library. The disadvantage is a matter of confidence in extrapolations to future machines; intuitive arguments have usually been used to pick a "representative" sample of trace tapes to drive the simulators.

Almost half of the library is the result of requests sent to RCA Management Information Services departments and to customer sites, asking for representative COBOL programs; the request was signed by a high-ranking manager, and got good response. However, due to the obvious problems in the manner of response, in running unfamiliar programs, and in some cases in providing suitable data, only 23 of the 50-odd programs sent in were actually traced. This, and the natural tendencies of the site representatives in choosing programs, has probably biased this COBOL sample towards relatively short and simple jobs. For example, only one sort program is included.

Our "dragnet" approach has also resulted in the following TDOS trace tapes: an instance of COBOL compilation, an instance of assembling an unknown program, a hand-written meta-assembler run, hand-written programs for simulation of a character-recognition system and for simulation of a cache system, an instance of FORTRAN IV compilation, a FORTRAN zero-locating program, an instance of FORTRAN PI compilation (PI for *Princeton Interactive*, but run in background mode), a FORTRAN PI hashing-simulation program, a SNOBOL compilation-interpretation run (doing an assembly), and two runs of RCA's Multichannel Communications System with test drivers. Under TSOS, interactive FORTRAN sessions under two different language systems, an editing session, and an interactive assembly have been traced.

Presently, several additional TDOS COBOL and FORTRAN compilations and executions are being skip-traced, with plans to compare the resulting statistics with those taken from the earlier collections. The TSOS tracing facility

has just begun being used; a BASIC session will be next. As mentioned above, a more statistically rigorous sampling of customer programs will be conducted, and new programs will be collected on a continuing basis, to allow tracing the evolution of program characteristics through time.

Analysis programs

Cache system

The principal application for the trace library has been to drive *cache system* simulators. A cache system is a form of memory hierarchy, such as has been implemented on IBM's 360/85 and 195, 370/155 and 165, where the two levels of the hierarchy have cycle times on the orders of 1 microsecond (main memory) and 100 nanoseconds (cache) respectively, where search, allocation, and replacement in the cache are handled by fast hardware rather than by software, and where the processor waits during acquisition of a block from slower memory rather than switching to another task. The performance of such a system is determined by the tendency of programs to reuse words and/or to use words sufficiently near previously used words. Blocks are on the order of 16 bytes in size (this defines *near*). Clearly, simulation—based on actual address streams—is the only appropriate means of evaluating cache systems.

The Spectra 70/IBM 360 instruction repertoire is a rich one; single instructions are able to generate considerable memory activity. For this reason we made a preliminary pass, transforming all trace tapes into "address" tapes, containing a coded representation of all addresses accessed. The code provided a starting address, a field length, and an item descriptor—whether an instruction or supervisor call was accessed, and whether a data access was for read or write. This transformation required a certain degree of approximation, since the trace programs do not record data: byte-string-compare instructions and translate instructions are important examples. Separate measurements would be necessary to justify the approximations that were made; these have not yet seemed worthwhile.

The cache simulations are reported elsewhere by K. R. Kaplan;[1] the basic idea is to keep track of which blocks would occupy a cache if it were present, under various allocation and replacement algorithms, using various block sizes and word sizes, and handling write traffic in various ways. The most useful numerical output of this simulation is a count of the average number of back-up memory requests generated per instruction executed. (0.3 is a typical such number.) It is then straightforward, in serial machines, to make a first-order estimate of instructions/second performance P by the formulae $P = 1/A$; $A = B + \mu M$, where A is the average instruction execution time; B is the average execution time (under a suitable instruction mix) assuming all references are satisfied by the cache; M is the access time to the backup memory, and μ is the aforementioned miss/instruction rate.

The cache simulation project has been received well by RCA Computer System. The main lesson we learned was that design teams continually modify their plans, so that clean and modular programming is essential. Also, we encountered substantial unhappiness over our restrictions to P1-code only; many simulation runs were made "worst-case" by flushing the cache every time a supervisor call was encountered, and other stratagems have also been employed, but a concern persisted that the supervisor code itself might behave substantially differently. We are considering studying this problem by means of an "all-state" trace program, mentioned earlier, and by hardware monitoring.

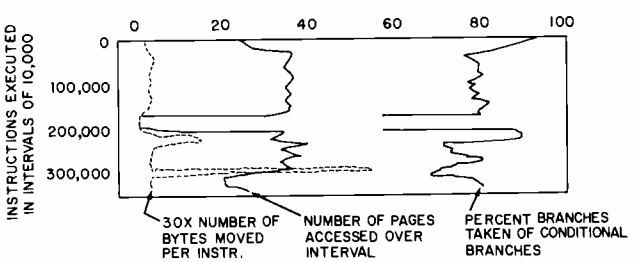

Fig. 2—Example of profile output (stylized).

Paging analysis

A second area of application for our trace library is in *paging analysis.* Here, the two levels of the simulated memory hierarchy cycle are on the order of 10msec and 0.5μsec; traffic is handled by software; and the "page" is thousands rather than tens of bytes in size. We have capitalized on the basic similarities of a cache system with a paging system to study certain questions, such as the optimal size of a content-addressed memory to bypass table lookups in address translation, and we have made static analyses of the overall usage of the pages which constitute given programs. But the bulk of the work in this area has so far been done elsewhere in RCA, by C. S. Warren, et al, of Computer Systems, running simulators remotely over our trace library at Princeton. Some modeling of paging behavior is being planned for the near future.

Process evaluation

A detailed SIMSCRIPT simulator of a family of proposed processors has been written, allowing experimentation with a variety of architectural ideas: multiple banks of memory with a variety of cache organizations, multiple processors, instruction lookahead schemes, and flexible microprogram timing. The simulator is driven by trace tapes, and accurately models overlapping of the various activities, at a machine cycle level. It runs quite slowly, so we have generated "sample" tapes, each of which consists of pieces sampled from many tapes. In addition to its main use to evaluate specific ideas, this simulator is used to cross check other simulators and to confirm certain points in statistical models; it also is useful in predicting the overall instruction-executing rate of proposed processors.

Program statistics

A fourth area of application is the derivation of basic *program statistics.* A program has been written which abstracts statistics from a given trace tape, as follows:

1) The number of instructions traced;
2) The number and frequency of each type of instruction executed (branch on condition, move characters, etc.);
3) The number of each type of supervisor call;

4) The number of each type of I/O command issued (only the first command of a chain is counted);
5) The frequency of chaining in I/O commands;
6) The distribution of nominal buffer sizes for recorded I/O commands;
7) The distribution of conditions used by the two branch-on-condition instructions;
8) The frequency of a branch being successful, for each of six branch instructions;
9) The frequency of indexing;
10) The distribution and averages of argument lengths for each of 13 one-argument and 9 two-argument instructions which use data whose lengths are specified by fields in the instruction; and
11) The number of words moved by store-multiple and load-multiple instructions.

These numbers have been of considerable help in understanding the programs that have been traced. The designers of several new RCA computers have made use of the instruction frequencies in optimizing microprograms, and miscellaneous use has been made of others of the statistics. Presently, the separate sets of statistics are being organized onto a single tape to facilitate the abstraction of averages across selected subsets of the trace library (e.g., all COBOL objects, all language translators); these results will be published soon.

Several special-purpose programs have also been written to abstract data relevant to specific design problems, such as the distribution of alignments of moved byte strings, certain instruction-pair statistics, and address-generating behavior of programs. This will probably remain a fertile type of application in the future. Generally speaking, the trace library should be used as an empirical source of data for building models of program behavior.

Executing behavior through time

The final class of applications for the trace library have been three programs for exhibiting the *executing behavior through time* of the traced programs, for purposes of debugging, code optimization, and better understanding generally. With one program, a single instruction per line can be printed, from the m^{th} instruction to the n^{th}, of a given trace tape. This facility has been useful in detailed study of anomalies pointed out by the other analyzing programs.

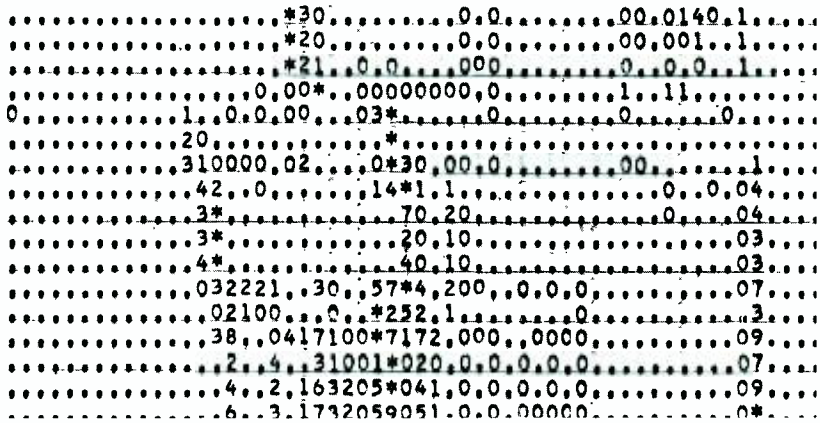

Fig. 3—Portion of output of Page Map. Page size is 2048 bytes. [*denotes maximally used page].

The other two programs provide "activity profiles" and "page maps," as follows: Each program is run over a selected *m*-to-*n* instruction interval. Each gathers a set of statistics for a user-specified interval of *k* instructions, prints a line, resets the statistics, gathers statistics again, etc. The activity profiler's statistics are plotted as a set of graphs, with time running along the printer sheet; the statistics chosen are the percent of branch instructions, the percent of branches taken, the percent of unconditional branches, the percent of move-character instructions, the number of bytes moved per instruction executed, and the number of pages accessed (of user-specified size). Each statistic can be multiplied by user-specified scaling factors. (See Fig. 2.)

The page map program provides, for a user-specified page size and selected region in core, a space-time chart, with each column representing a specific page in core, and printed characters denoting no access, maximum number of accesses, or a numeral from 0 to 9 to denote a corresponding fraction of the maximum for that line. (See Fig. 3.) An alternate mode of output provides numerical output for each *k* instructions (page count, separate data and instruction page counts, new pages since last interval, and pages used in last interval but not this one), as well as a multi-line map of page usage (distinguishing between instruction, data, and combined pages).

These analysis programs show very clearly the phases in a program's behavior. The passes of a compiler, and variations of activity within a given pass, show up clearly, as well as anomalies such as a drop to a mystifying two-instruction loop for 50 thousand instructions in one program. The page map program is being used to develop better models of paging behavior, as well as to study specific programs.

Conclusion

A suitably designed trace facility and an active trace library project have a large number of important applications. Initially, the goal was to study cache systems, for which the trace library was essential, but we have since then used it to study paging, to drive processor simulators, to abstract a large class of statistics useful in computer design and modeling, and to study dynamic program behavior. Most of the latter applications were not originally anticipated and still more can be expected. The creation and maintenance of the library has required substantial effort; however, we believe it to be a very worthwhile investment.

Acknowledgments

Participating directly in the project as described here were the following: K. R. Kaplan, J. L. Kodner, S. Y. Levy, A. R. Marcantonio, N. F. Maxemchuk, A. D. Robbi, J. A. Weisbecker, and C. T. Wu of RCA Laboratories, and C. S. Warren of Computer Systems. E. J. Gaudion, S. Pan, and S. Stimler, also of Computer Systems, provided essential help in the generation of the trace library. Work is continuing in the Computer Design Research Group at RCA Laboratories in most of the areas described in the paper.

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Cache system studies

Dr. K. R. Kaplan

The disparity in speed between computer memories and logic circuits has led computer designers to the use of a variety of system enhancements, such as fetch/execute overlap and generalized lookahead, multiple-bank memories, multiprogramming, multiprocessing, etc. A hierarchy of memories provides another approach, of great current interest. "Paging" as used in multiprogrammed or time-sharing systems, the IBM "cache" memory, and the two-level optical memory system under study at RCA Laboratories are examples of such systems. Specific research in cache memory systems was begun at RCA Laboratories in 1968. The purpose was to provide the means for evaluating the cache memory concept, and to produce statistics, information, and ideas useful to the designers of cache-based systems.

THE EFFECTIVENESS OF MEMORY HIERARCHIES has traditionally been studied in two categories: paging systems or cache systems. In *paging* systems, the intent is either to provide the programmer with an apparently inexhaustible address space, or (as in multiprogramming systems) to arrange for several programs to reside simultaneously in memory. Thus, the hierarchy is designed to move fragments of programs from a large backing-store to the high speed memory. This allocation of program fragments, or pages, is performed dynamically in the course of program execution, and is under the control of an *operating system*. Since backing-store memories are generally rotating devices offering pseudo-random access to large blocks of information, the units of transfer are pages of several thousand bytes.

In contrast, the local memory, "slave store" *cache* concept is typified by the interaction of two random access memories—one small and fast, the other larger and relatively slower. Additionally, the blocks of information allocated to the cache are small (under 100 bytes) and the cache is *hardware controlled*.

Central to the study of cache/paging systems is an investigation of the way programs behave while they are being executed. The extent to which instructions are fetched in long sequences, the frequency of branching, the movement of data fields, etc., are key factors in the performance of the hierarchy. Gibson[2] published results on block-oriented program management in 1967, based on extensive trace and simulation studies at IBM; studies which influenced the design of the cache in the Model 85.

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received the BEE in 1956 from Polytechnic Institute of Brooklyn. He received the MEE and PhD in EE in 1958 and 1964, both from P.I.B. His dissertation was on Markov chain models of adaptive processes. From 1957 to 1960, as a doctoral candidate, he taught in the EE Dept., and was a member of the Control Systems Research group under Dr. J. G. Truxal. This group produced an advanced text, *Adaptive Control Systems*, McGraw-Hill, 1961, with Dr. Kaplan authoring a chapter on non-linear control systems. He joined RCA Laboratories in 1960, and has since worked on high-speed memory and logic circuitry, theory of adaptive systems, synthesis of threshold logic networks and programs for interactive design, simulation of I/O buffering, and most recently, extensive simulation studies in the area of memory hierarchies, for which he received two RCA Achievement Awards. He is also a lecturer in Computer Science at Livingston College, Rutgers University, where he presents courses in modeling and simulation.

Cache fundamentals

A cache is (typically) a small, high-speed (100 to 300ns) semiconductor memory, interposed between the processor and backup memory (1 to 2μs core, say). Its function is to accumulate instructions and data used by the processor as it executes a program. Generally, much of this information is required many times during the course of the program, and the quicker access offered by the cache permits a faster overall execution rate.

Processor *read* requests for instructions and data are presented to the cache control logic, which initiates a search of the cache "table of contents" to determine if the addressed word is currently contained in the cache. If the search is successful (hit), normal program execution continues. If not (miss), a transfer of information from main memory to cache is initiated, and the processor is supplied with the word specified by the address reference. Since successive program references are, for the most part, highly localized, (by reason of the contiguity of sequential instructions, contiguous data words, and re-use of instructions in tight loops) the information brought to cache typically consists of *several* words *adjacent* to (and including) the referenced word. This transfer unit is called a *block*. And in fact, the aforementioned "table-of-contents" search actually looks for the appropriate block in cache.

Processor *write* requests can be handled in two ways. In the *"store-through"* technique, main memory is *always* written to (on a *word* basis) and the cache is also updated if the pertinent block is present. An alternate strategy is to write *only* to cache; if a block is purged in cache (to make room for the current reference) a check is made to determine if the block was written to during its residency. If so, the block is written out to main memory, and the new block is then read into cache. For consistency, this *"swapping"* or *"write-accumulate"* strategy should be augmented by a *"write-allocation"* procedure, i.e., one wherein blocks are allocated to the cache on write "misses" as well as read "misses". Thus a processor store request which cannot be satisfied by the cache causes an allocation of the required block to cache, accompanied by an updating of that block in cache.

The *read-allocate, store-through* mechanism is implemented in the 360/85. The model 195 allocates on write

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misses as well, although store-through is still employed. Our studies indicate that the "read-hit" performance is only marginally improved by allocating cache equivalently for reads and writes. To our knowledge, the write-accumulate strategy has not yet been implemented, although we feel that it offers an attractive inexpensive way of reducing main-memory traffic—of exploiting the experimentally verified fact that a block, once written-to, will be changed many more times before it leaves the cache.

To "telescope" a large address space into a small cache, some sort of associative mapping of addresses is required. The various schemes which accomplish this mapping may be distinguished by the degree of associativity required. A *fully* associative method (denoted CAM) partitions address references into two fields: 1) The rightmost field addresses a byte within a block; for example, this field would be 6 bits wide for a 64 byte block. 2) The remaining address bits are used as a *tag* or key; this tag is used to search the cache tables (probably a separate associative memory) for a match, which indicates that the addressed block is present. A no-match condition causes a block to be displaced from cache (in accord with some replacement algorithm) and the new tag assigned to that slot in the tag table. And, of course, the block would be transferred to the cache.

The CAM method of cache allocation is the most flexible. If the tag field is T bits wide, then any of 2^T main memory blocks can map into any of the cache blocks. But this flexibility is balanced by the cost/time penalty of a large associative search.

The 360/85[3] employed a hybrid allocation scheme: Associative mapping of 1024-byte sectors is performed (the cache is 16 sectors "big") but the sixteen 64-byte blocks contained in each sector are directly (congruently) addressed. This method proves to be wasteful of cache space, and is eclipsed in efficiency by another method called BANKS.[4] This has been studied the most of all the allocation algorithms, and it is presently being configured in New Technology Systems (NTS) specifications.

BANKS partitions cache into independent units (called banks) each of which contains a fixed number of blocks. Each bank is directly addressed by the block field (an interior field of bits) of the memory reference. The tags associated with the addressed blocks are then compared against the high-order bits of the memory reference.

This simple scheme has many virtues, not the least of which is the ability to access the addressed word simultaneously with the tag comparison. (Should the comparison fail, the data acquisition can be suppressed.) Cache efficiencies (read references satisfied by cache/total read references) in excess of 85% can be obtained over a wide range of program types with very modest cache sizes.

In this discussion most areas relevant to cache performance for which we have obtained quantitative results have been mentioned. As a summary and guide to the remainder of this paper, these areas are as follows:

Parameters
- cache size
- block size
- number of banks
- cache-processor buswidth

Allocation
- on read "miss" only
- on all misses—read/write

Deallocation
- replace least recently *referenced* block (RCNC)
- replace least recently *allocated* block (FIFO)

Write strategy
- store through (with consequent main memory interleave requirement)
- accumulate writes-block swap

Environment
- multiprogramming-task switching
- multiple processor

The "environmental" studies have attempted to determine, through simulation, how the cache efficiency is affected by the presence of more than one program stream. The difference between multiprogramming and multiprocessors (from the viewpoint of these studies), is as follows: When a single processor is being shared by several programs, each program "feels" the others to the extent that some of the information it has accumulated in the cache (during the time-slice for which it claims the processor) is invalidated when the processor is taken over by another program. (This is true of executive intervention-system programs as well as another user program.) When the processor is regained, the lost contents may have to be restored, thereby impairing the cache efficiency as seen by each program. In a multiple-processor environment—two (or more) processors executing independent programs through the same cache—each program has effectively less cache available to it relative to the uni-processor case. We have modeled and simulated these situations in a simple, worst-case fashion.

Trace methodology

At the outset of this project, we *rejected* the notion of using pseudo-randomly generated address sequences as the stimulus for the simulators. The very components of programs which were least known—locality of reference, and re-use of information—would be the critical factors in determining the success or failure of the cache hierarchy scheme. Hence, it seemed clear that to produce an accurate *quantitative* measure of cache performance, *real* program address streams would be required. Consequently, a trace program was written by R. O. Winder.[5] The program produces a *trace tape* of "items"—op code, instruction address, operand address(es)—which characterize the behavior of an object program executing on the 70/45 under TDOS. The trace program "lives" in P2 state; as a result, only the P1 component of the object program is traced. Supervisor Calls (svc's) are "noted" on the trace tape, but actual tracing resumes when the object program returns to P1. This aspect of the trace tape gives rise to a convention regarding simulation of svc's in the cache simulators. The cache tables are either cleared—"flushed", or not, when an svc is encountered in the input stream to the simulator. The "flush" option represents a worst case; it as as though the executive code completely displaces the user code in the cache, and when the user (P1) program resumes, it must restore its instructions and data from "scratch".

Recently, we have attempted a more sophisticated simulation of supervisor intervention.[6] *Two* P1 address streams drive the simulator: one is the "foreground" (user) program, the other represents the system code. When a foreground svc is detected, the cache is given over to the svc simulator

Table I—Instructions and memory space allocations for trace samples.

	Number of traced instructions	*Memory space†*
COBOL obj	1,040,979	24,624
FORTRAN IV obj	325,635	24,520
Assembly obj (A)	317,891	24,760
Assembly obj (B)	1,003,925	184,424
FORTRAN PI obj	900,980	111,920
FORTRAN IV comp (A)	344,136	79,880*
FORTRAN IV comp (B)	1,288,979	79,880*
COBOL comp	210,231	35,656
Assembly	974,047	70,000**
FORTRAN PI comp	1,574,898	201,696
SNOBOL	1,877,187	199,328
MCP (A)	114,236	
MCP (B)	421,077	

* largest segment
** estimated from subsequent processing
† The amount of memory required by the traced program when loaded.

stream (but *not* "flushed"). When the latter subsequently issues an SVC, control is returned to the user stream. (User and system code are *not* shared.)

In collaboration with Computer Systems, some three dozen programs have been traced. This trace library includes:

- 23 COBOL objects
- 1 FORTRAN IV object
- 2 Assembly objects
- 1 FORTRAN PI object
- 2 FORTRAN IV compilations
- 1 COBOL compilation
- 1 Assembly
- 1 FORTRAN PI compilation
- 1 SNOBOL compilation & interpretive execution
- 2 traces of TDOS MCP (communications)
- 1 trace of PLASM—a meta-assembler

Recent acquisitions include traces of programs executing under TSOS.

Two principal characteristics of the trace samples are given in Table I. The entries for COBOL objects are for a COBOL program considered "typical" (described later). The COBOL objects traced range in size from 7000 to 37,500 bytes. Instruction counts range from 17,000 to 2.3 million. There exists a terse description of each COBOL program, including program function, input requirements, and output production.

The COBOL programs (and certain of the non-COBOL traces) were classified in accordance with the hit ratios they produce in a 1024-byte, 2-bank, 32-byte-block cache, under the "flush" option, and with FIFO replacement. This calibration run is shown in Table II. The COBOL program presented as a prototype in Table I is RCA #18; its cache efficiency falls close to the median for all COBOL programs. Table II gives the frequency of writes for each of the programs, the density of SVC's, as well as the cache efficiency in "no-flush" mode. Note that, in general, the programs producing low hit ratios have a high incidence of SVC's and their performance improves markedly when the cache is not flushed.

Our recent experiments with two-stream simulation (wherein supervisor code is "approximated" by a P1 stream) suggest that the "flush" view is much too extreme. Table III shows the variation in read miss ratios—the ratio of read *miss* references to total read references—as the SVC treatment is altered. The "background" address stream for these results is COBOL object RCA #3 (Table II), chosen on the basis of its average SVC density—1 every 125 instructions. Thus the "user" program "loses" the cache for about 125 instructions whenever it issues a supervisor call.

In other respects, the use of RCA #3 is a poor one. It contains a disproportionately high number of character-handling instructions. We are planning experiments with a P1 stream more "typical" of system code.

Simulation

Our current cache simulator reads tapes directly derived from trace tapes, and produces statistics about the processor cache main-memory performance, as follows:

Totals

1) Number of read references
2) Number of (instruction) read references satisfied in the instruction register (assumed the same width as the processor-cache bus—no "prefetch" is simulated)
3) Number of read references found in cache
4) Number of read references found in memory

Table II—COBOL Library calibration run: 1024-byte, 2-bank, 32-byte-block, 4-byte-bus, FIFO.

RCA Tape #	*% SVC (instructions)*	*% writes (references)*	*Read hit ratio*	
			Flush	*No flush*
1	0.9	25.69	0.789	0.810
2	1.0	25.03	0.760	0.794
3	0.8	28.00	0.785	0.801
4	0.0	25.01	0.838	0.840
5	0.1	22.18	0.817	0.829
6	0.2	28.67	0.859	0.867
8	1.2	23.13	0.727	0.796
9	0.0	25.98	0.820	0.822
11	1.9	23.79	0.725	0.812
12	1.0	24.62	0.851	0.859
13	0.2	24.82	0.832	0.842
14	0.1	11.23	0.959	0.968
15	0.1	22.23	0.879	0.884
16	0.2	20.97	0.817	0.829
17	1.5	21.37	0.734	0.806
18	0.0	18.77	0.835	0.839
19	0.2	28.99	0.851	0.861
20	1.0	26.73	0.759	0.816
21	1.0	28.03	0.787	0.833
22	0.5	18.94	0.812	0.838
23	0.0	16.35	0.918	0.821
24	0.0	8.90	0.945	0.952
25	0.5	24.80	0.839	0.858

Table III—% read misses; 4-k, 2-bank, 16-byte-block (read-allocate, FIFO).

Program	FLUSH	SVCSIM	NO FLUSH
COBOL 3	27.14	5.8	5.66
COBOL 11	38.41	15.75	1.02
COBOL 15	8.19	6.26	5.24
COBOL 18	11.19	4.3	2.69
FORTRAN Compiler	9.94	8.3	7.16
COBOL Compiler	9.07	6.67	4.84
Assembler	6.53	4.94	4.03

5) Number of write references
6) Number of write references found in cache
7) Number of write references found in memory
8) Number of first writes (first time that blocks in cache are altered)
9) Number of replacements of written-to blocks

Items 1) through 9) are also output normalized to:

a) Number of instructions
b) Number of total references
c) Number of read or write references. That is, 1) through 4) are presented normalized to total read references; 5) through 7) are normalized to total write references.

Item 3) normalized to read references is the cache "hit" ratio. Items 4) and 7), normalized to number of instructions, and added together, give a measure (miss/instruction) of the number of main memory cycles per instruction required to process the address stream. If a write-allocate, write-accumulate strategy is under consideration, item 9) (instruction-normalized) must be added to the miss count, since the replaced (written-to) block must first be written to memory for updating. That is, item 9) represents the "swapping" overhead incurred by the write-accumulate strategy.

Also present in the output are the cache parameters and the simulation options, all of which are specified as run-time data input. These are:

Parameters

1) Cache size (bytes)
2) Number of banks
3) Block size (bytes)
4) Cache-processor bus-width

Options

1) FIFO (first-in-first-out) or RCNC (recency) replacement algorithm
2) Allocate only on read miss, or on any miss (read or write)
3) Load the cache only with:
   a) instructions (write references and data references are skipped)
   b) data (instruction references are skipped)
   c) reads (writes are skipped)
   d) instruction fetches and writes (data reads are ignored)
4) FLUSH, NO FLUSH, or SVCSIM implementation of supervisor calls.

When option 4) calls for SVCSIM, output is produced for both the "user" and "supervisor" programs.

TABLE V—Cache performance data.

Cache size	Block size	# of banks	% Ref. which are WRITES	% READS found in . . . Instr. reg.	Cache	Main memory
COBOL object: 1,040,979 instructions, 25,000 bytes						
4096	16	1	16	23.4	68.4	8.15
		2	16	23.4	68.8	7.75
		4	16	23.4	69.	7.58
	32	1	16	23.4	69.3	7.26
		2	16	23.4	70.8	5.78
		4	16	23.4	71.	5.57
8192	16	1	16	23.4	68.8	7.73
		2	16	23.4	69.0	7.51
		4	16	23.4	69.1	7.45
	32	1	16	23.4	70.4	6.1
		2	16	23.4	71.2	5.3
		4	16	23.4	71.4	5.16
COBOL compiler: 210,231 instructions, 35,000 bytes						
4096	16	1	13.8	23.2	64.0	12.7
		2	13.8	23.2	66.5	10.1
		4	13.8	23.2	67.0	9.57
	32	1	13.8	23.2	66.8	9.93
		2	13.8	23.2	69.5	7.2
		4	13.8	23.2	69.9	6.77
8192	16	1	13.8	23.2	66.2	10.53
		2	13.8	23.2	67.6	9.08
		4	13.8	23.2	67.9	8.83
	32	1	13.8	23.2	69.0	7.06
		2	13.8	23.2	70.6	6.11
		4	13.8	23.2	70.8	5.85

Results

For a 2- or 4-bank cache, with FIFO replacement, in the range of 1024 to 4096 bytes, with block sizes of 8 to 64 bytes, on a 4-byte-bus machine, under the flush assumption:

The cache efficiency is relatively insensitive to the choice of replacement algorithm. Replacing the least recently referenced block [as compared to the least recently allocated block (FIFO)] improves the efficiency by 1 to 2%. Read hit ratios range from about 40 to 95%, with 85% an approximate median. (The range at 2 banks, 4096-byte, 32-byte block is 73 to 96%.)

In the FLUSH mode, performance tends to level off at a cache size of 4k bytes. Increase in cache size is marginally effective beyond that point. In NO FLUSH mode, however, performance improves with larger caches, approaching 100%. It is important to remember that FLUSH and NO FLUSH are *simulated* extremes. In actuality, some variable portion of the user code will be displaced by the supervisor code. Experiments with the new SVCSIM option should illuminate this area.

A two-bank cache is 3 to 5% better than 1 bank, and only marginally poorer than 4 banks. In fact, the difference in performance between 2 banks and complete associativity (1 block per bank) is on the order of 2-3%.

Block sizes in the 16 to 32 byte range appear to be most effective. Too large a block causes superfluous information to displace needed information. An eight-byte block is probably too small; it cannot contain enough "local" information.

The fraction of references which write to memory ranges between 1/8 and 1/4 (4 byte transfer/reference.) On a per-instruction basis (2 to 3.5 references/inst is the observed variation) with 2.5 references per instruction assumed, the write overhead runs from about 0.3 to 0.6 writes/inst.

The number of cache misses (backing-store accesses) per instruction is relatively insensitive to cache-processor buswidth.

Multiprocessor interference in cache—a median degradation of approximately 5% is observed when two trace tapes make alternate references through a common cache.

Table IV was prepared by R. E. See of Computer Systems at Marlboro, running an older version of the BANKS simulator through the remote job entry facility at the RCA Laboratories. The Table illustrates most of the conclusions (above) and demonstrates that the cache performance is influenced mostly by program material. The last two columns were generated to determine if written-to blocks accumulate in the cache (rather than drift back to memory as a consequence of replacement) and thus present extensive overhead at task switching time (represented by an SVC) in a multiprocessing environment.

Table V gives more performance data for two programs at a possible design center. This data was generated for a cache-processor buswidth of 8 bytes. (A multiplexed transfer over a physical 4 byte bus.)

Conclusions

The trace tape data base, the raw program statistics derived from the tapes, and the cache simulator results have greatly increased our understanding of dynamic program behavior and static cache performance, and have assisted design evaluation of cache alternatives.

Acknowledgment

The cache memory system research has been characterized by a stimulating and effective interaction with J. N. Marshall's engineering group, C. S. Warren's measurement and evaluation group (both at Computer Systems, Marlboro) and with Product Planning. Instrumental to the success of the study, in addition to the above, were: R. O. Winder, J. A. Weisbecker, and A. Robbi, of RCA Laboratories, and G. Smith, J. Page, and R. E. See, all at Computer Systems, Marlboro.

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Table IV—Cache performance; 4096-byte cache, 2 banks, 16-byte block 4-byte bus, FIFO, FLUSH.

Program	% SVC (inst)	% writes (refs)	% read hits (read refs)	% write hits (write refs)	% main memory refs. (all refs.)	% read misses (all refs.)	% write misses (all refs.)	% misses (all refs.)	FW/Tot. Miss	% FW/ref	Cache Writes/ FW (re-use)	Written-to-blocks at SVC time Avg.#	%(#/256)
Read allocate													
FORTRAN IV	0.110	15.22	90.0	63.9	23.60	8.38	5.50	13.88	.10	1.39	7.01		
COBOL	0.209	14.84	90.9	75.3	21.60	7.75	3.66	11.41	.12	1.37	8.16		
Assembly	0.093	22.75	93.5	90.3	27.77	5.02	2.20	7.22	.18	1.30	15.78		
COBOL 3	0.876	26.71	72.9	78.7	46.51	19.80	5.69	25.49	.21	5.35	3.92		
COBOL 11	1.979	23.56	61.6	45.4	52.94	29.38	12.85	42.23	.11	4.65	2.30		
COBOL 14	0.145	11.18	95.0	80.5	15.62	4.44	2.19	6.63	.15	0.99	9.09		
COBOL 15	0.106	21.57	91.8	57.1	27.99	6.42	9.24	15.66	.07	1.10	11.50		
COBOL 18	0.092	18.24	93.3	92.6	23.72	5.48	1.35	6.83	.15	1.02	16.58		
R/W allocate													
FORTRAN IV	0.110	15.22	90.9	91.4	11.30	7.71	1.31	9.02	.25	2.26	6.15	21.0	8.2
COBOL	0.209	14.84	91.6	90.6	10.86	7.15	1.40	8.55	.27	2.31	5.82	16.6	6.5
Assembly	0.093	22.75	94.1	96.3	7.22	4.55	0.84	5.39	.34	1.83	11.95	36.8	14.4
COBOL 3	0.876	26.71	74.8	91.0	28.20	18.47	2.40	20.87	.35	7.30	3.33	28.5	11.1
COBOL 11	1.979	23.56	63.8	80.3	41.00	27.67	4.64	32.31	.27	8.72	2.17	12.2	4.76
COBOL 14	0.145	11.18	95.4	89.2	6.91	4.08	1.27	5.35	.29	1.55	6.42	18.3	7.15
COBOL 15	0.106	21.57	92.4	90.6	10.78	5.95	2.03	7.98	.35	2.79	7.00	52.6	20.6
COBOL 18	0.092	18.24	93.9	96.8	6.74	4.99	0.58	5.57	.21	1.17	15.10	25.2	9.85

A profile of the Palm Beach Gardens plant—Computer Systems

A. R. Harris

A major part of the Computer Systems organization, RCA Systems Development Division has facilities at Palm Beach Gardens, Fla.; Marlboro, Mass.; and Cherry Hill, N.J. This profile thumbnails the Palm Beach Gardens operation: the plant—its history, functions, products, organization—and the outlook for the future. The Palm Beach Gardens operation is concerned essentially with the design, manufacture, and test of computer main-frames (central processor units, or "CPU's", as opposed to peripherals).

TRACING ITS BEGINNING in computers to the pre-World War II years, RCA developed circuitry and logic for the first digital electronic multiplier—ENIAC. Jumping from 1950 when RCA initiated its first market study of data processing—through the first generation tube-type computers (BIZMAC, 1955), the second generation semiconductor-type computers (RCA 301, 501, 601), and the most recent Spectra series—Computer Systems today employs more than 13,000 people engaged in the design, manufacture, marketing, and servicing of computers and associated peripheral equipment. RCA computers are presently used in batch data processing, high-speed data communications, remote batch, and interactive (time-sharing) applications.

A decisive part of RCA's growth over the past decade, the computer plant in Palm Beach Gardens was completed in January 1961. Its first computer system, a 301, was delivered on May 25, 1961—the day the buildings were dedicated.

Several of the milestones in computer history in which the Palm Beach plant was directly involved are:

1960—RCA announces the large-scale RCA 601 and the small-to-medium-range RCA 301, thus becoming a full-line supplier of automatic data processing equipment

1964—RCA introduces Spectra 70 series of computers which pioneer the use of monolithic integrated circuits

1969—RCA brings out the new large-scale Spectra 70/60-61 computing systems that triple throughput capacity over the smaller 70/45-46 systems

1970—RCA introduces its new series of computers, starting with the RCA 2 and the RCA 6 with real memory systems, and the RCA 3 and RCA 7 with virtual memory systems.

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The decision to establish an RCA plant in the Palm Beach area was helped along by leading citizens of Palm Beach County. They were anxious to develop the economy but insisted on "clean, quiet" industry that would not despoil the Florida environment. Computer production was a "natural" to meet these requirements.

In a 115-acre setting of rare natural beauty, the RCA plant blends with its surroundings. A lagoon (photo, p. 52) is framed by offices, the factory, and the plant cafeteria. The cafeteria side of the lagoon is home to an overfed baby alligator and an assortment of fish and turtles among the vari-colored water lilies. This lagoon is one of several created on the site from excavations that provided soil compaction for the plant foundations. Now these same excavations, filled with water, not only enhance the natural beauty of the RCA plant's setting but provide an ample auxiliary water source for fire or other emergencies.

Functions

In contrast to the plant's rather serene exterior, the factory interior is a model of industrial efficiency reflecting the latest in automated development of quality products. An innovative technique of in-process, on-the-spot correction of defects is instrumental in maintaining this plant's exceptional level of product quality along with associated benefits in time and material savings, as well as increased production—and profits.

Actually the Palm Beach Gardens plant has three basic functions: to design, to assemble, and to test computer hardware.

The design function is a sizeable effort encompassing design automation; data entry systems; standards and design support; logic and special circuits; mechanical and electrical packaging; memory devices; power supplies and systems; communications systems; and product engineering. Computer-aided design programs are developed and the techniques are used extensively.

Systems Development Division, Palm Beach Gardens Plant, also has responsibility for programs being carried on at Somerville, Van Nuys, and Marlboro.

The assembly function involves memory devices; semiconductors (transis-

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received the BA in Writing from Southern Methodist University in Dallas; the BJ in Journalism (Advertising) from the University of Missouri, and the MBA in Engineering Management from Rollins College, Florida. He was a Senior Technical Editor with the RCA Service Company at Cape Kennedy, Florida, from 1956 to 1964. He was subsequently with The Boeing Company at Kennedy Space Center, Florida and Seattle, Washington as Lead Technical Editor. He rejoined RCA at Palm Beach Gardens as Technical Publications Administrator in June 1970. He is a Senior Member of the Society of Technical Writers and Publishers (STWP).

Mechanical subassembly area.

Semi-automatic wire-wrap machine.

Engineering computer room. Stan Lester of Palm Beach Gardens and Nick Garaffa of Marlboro are processing a new-product-line design task on a Spectra 70/45.

The Quality Engineering Analysis Lab performs sample disection analyses (electrical and chemical) of all incoming lots of small discrete components. In the photo, Ada Nave is taking a photomicrograph of a component.

tors and integrated circuits); magnetic tape heads; sheet metal items (frames, doors, etc.); printed circuit boards; mass storage units and video consoles. The Palm Beach plant builds (i.e., performs complete fabrication, as distinguished from the assembly function) processors, control units, card readers, and communication buffers. Other elements—card punches, printers, console typewriters—are built into completed units from basic mechanism subassemblies furnished from other sources. The heart of this fabrication is a delicate balance of automatic, semi-automatic, and manual interconnecting of the miles of electrical wiring which determines the final computer logic. Printed circuit boards are assembled, soldered, and tested at Palm Beach, using printed and etched boards from other RCA sources.

The third major function—testing—covers units *and* systems. Not only are units tested to their own specifications; complete systems are tested to prove internal compatibility, timing, and interaction—virtually duplicating the customer's "real world" environment.

Customers

RCA's computer customers include public utilities, financial establishments, educational institutions, insurance firms, and state and local governmental agencies. The Palm Beach operation depends upon government contracts for a relatively small percentage of its business.

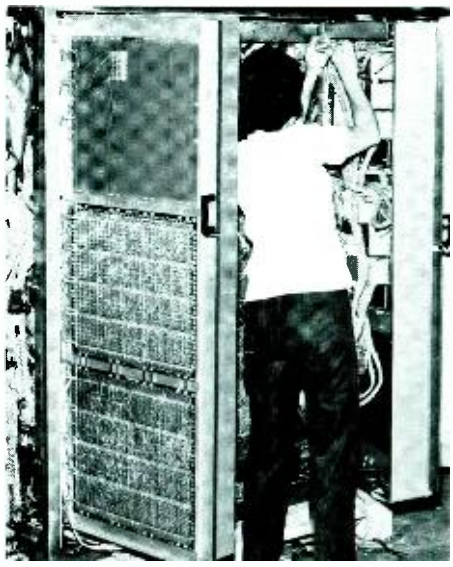
Product line

As previously mentioned, the Palm Beach facility is primarily concerned with producing computer mainframes (processor units). The major activity for handling electro-mechanical peripherals is assigned to the Marlboro Product Laboratory at Marlboro, Mass. (to be described in a subsequent issue of the *RCA Engineer*).

Initially producing the 301 computer system, the Palm Beach plant subsequently began manufacturing the larger 3301 system. In 1964, the Spectra series was introduced. The new product line of RCA 2, RCA 3, RCA 6, and RCA 7 was announced in 1970. The RCA 3 and RCA 7 systems feature virtual memory, a concept pioneered for the Spectra 70/46 and Spectra 70/61. Virtual memory is highly significant in the computer industry as a means of greatly increasing the effective memory size and flexibility of a computer without greatly increasing its cost.[1]

Engineering organization

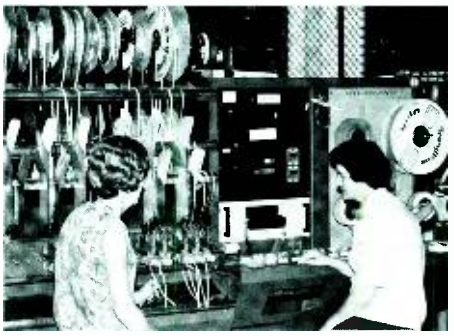
Today—ten years after the Palm Beach Gardens plant opened its doors—the work force has grown from 30



The profusion of wiring harnesses in a central processing unit (CPU) make it a "nightmare" assembly task.

Bob McLaughlin in the Mechanical Packaging Engineering Lab setting up life tests on switches. The carousel-type tester in the foreground was developed in this Laboratory.

Plug-in module assembly area.



Insertion Machine automatically selects the right components (from reels at upper left) and correctly sequences them on printed circuit boards. Selection and sequencing are controlled by a punched paper tape (shown here running through small "black box" between the operators).

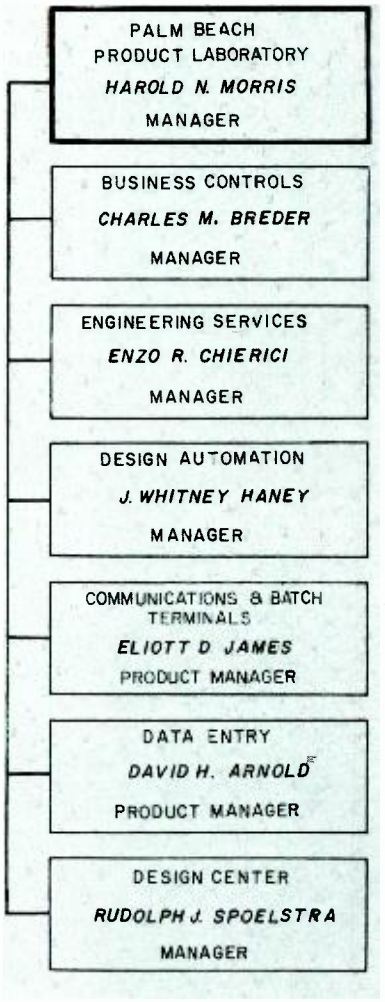


Fig. 1—Organization, Palm Beach Product Laboratory.

to about 3,500 employees. Of these the Systems Development Division (Palm Beach Gardens) accounts for about 580.

Effective October 30, 1970, all technical product-line planning, design, and development operations of Computer Systems were combined into a single Systems Development organization. This new organization brings together Engineering, Systems Programming, and Product Planning; all these functions were realigned into logical groups for systems, hardware, and software products. Under this concept, each group operates under entrepreneurial management. Systems and product managers head profit centers and are responsible for developing a specific part of the product line, and for assuring that this assigned part of the product line produces the planned revenue, profit, and share of the market.

An outline of the Palm Beach Product Laboratory organization is shown in Fig. 1. The Manager, H. N. Morris, reports to P. A. Beeby, Vice President, Technical Operations. Mr. Beeby reports to V. O. Wright, President, Systems Development Division.

Also recently activated at the Palm Beach Gardens Plant are the Small Systems and the Medium Systems Groups. Managers of these systems groups report directly to Mr. Wright. Each Systems group is made up of Systems Planning, CPU Engineering, and Business Controls organizations.

The Small Systems Group under N. N. Alperin (See "News and Highlights", this issue) is a profit center responsible for the 301, 70/15, 70/25, 70/35, 70/45, 70/46, 1600, RCA 2, RCA 3, and NTS-100 systems.

The Medium Systems Group, under R. Sayford, is a profit center responsible for the 501, 3301, 70/55, 70/60, 70/61, RCA 6, RCA 7, and NTS-250 Systems.

The Manufacturing Operations activity of the plant, headed by K. L. Snover, is under Systems Manufacturing.

Future

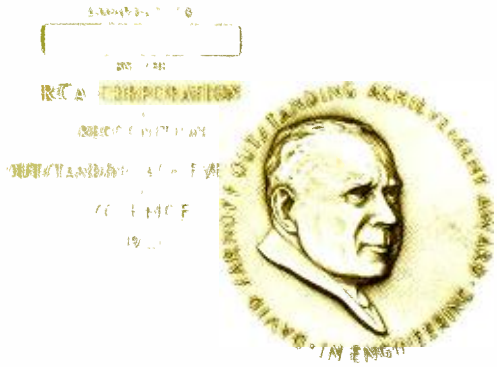
The outlook is excellent for the RCA Palm Beach Gardens operation. A visible evidence of growth is the addition of a 32,000-square-foot Engineering wing completed in October 1970 to supplement the existing 370,000 square feet of plant space. Pilot production of the new series of RCA 2, RCA 3, RCA 6, and RCA 7 systems is under way and on schedule. First delivery to customers is anticipated late in 1971.*

And the end is not in sight!

Reference

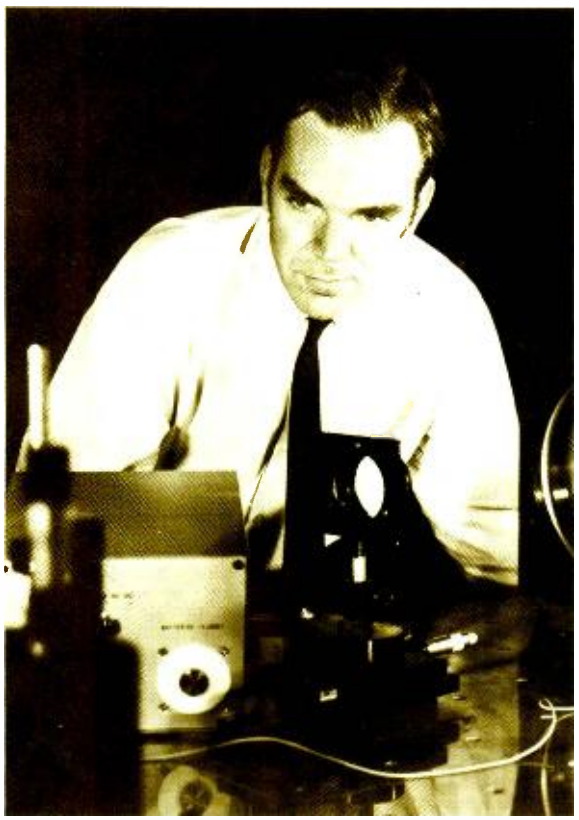
The virtual memory concept is explained in more depth by L. E. Donegan, "RCA and the computer industry in the 70's," *this issue.*

*Since this article, the scheduled delivery for the first RCA 2 was moved up to mid-May 1971.



The David Sarnoff

The 1971 Individual Award in Science



David L. Greenaway received the David Sarnoff Outstanding Achievement Award in Science **"for scientific exploration of holography and the conception and implementation of numerous applications."**

Dr. Greenaway has conceived and implemented several practical applications of holography which promise significant commercial returns. He initiated the Holotape project which led to the SelectaVision development. He has worked on mask storage in the form of a hologram for the production of integrated circuits. Dr. Greenaway has also devised a holographic approach to replace the step-and-repeat process for integrated-circuit production. The Holocard and Holokey systems for identification and security applications which he initiated have been built and tested and have been installed in the new building of Laboratories RCA, Ltd., at Zurich, where Dr. Greenaway and his group of several scientists and technicians continue their work on various aspects and applications of holography.

The 1971 Team Award in Science

Howard R. Beelitz, Henry S. Miiller, Peter D. Gardner, and **Dr. Andrew G. F. Dingwall** received the David Sarnoff Outstanding Team Award in Science **"for outstanding team research leading to the effective use and fabrication of large scale integrated arrays for logic and memory."**

Messrs Beelitz, Miiller, Gardner, and **Dr. Dingwall** have put RCA in a leadership position in the MOS array business. Working together on a LSI program, partly funded by the Air Force, this team developed a unique complementary MOS fabrication process. Other semiconductor manufacturers are trying to match our capability in this area, but this team has given a head start of two years to RCA's COS/MOS line of devices and LSI arrays. The advances in LSI technology have also instilled confidence in the company's ability to make LSI arrays of emitter-coupled-logic gates for a new computer line. The essential technique for depositing and etching two layers of metal for interconnections, and the array design techniques, were perfected to satisfy the goals established by this team. This effort was recently culminated by the completion, satisfactory operation, and delivery to the Air Force of an experimental computer as complex as an RCA 301, but with logic-gate speeds equivalent to those used in the Spectra 70/45 and 70/55. Noteworthy is the fact that the 144-gate arrays used in the experimental computer require less than one-tenth the power of the equivalent number of Spectra 70 gates. This computer also employed a 512-byte complementary MOS memory with a cycle time of under 100 nanoseconds. The experience and patents gained by this effort put RCA in a favorable position to exploit its advanced technology in the semiconductor memory field.

Outstanding Achievement Awards

RCA's highest technical honors, the annual David Sarnoff Outstanding Achievement Awards, have been announced for 1971. Each award consists of a gold medal and a bronze replica, a framed citation, and a cash prize.

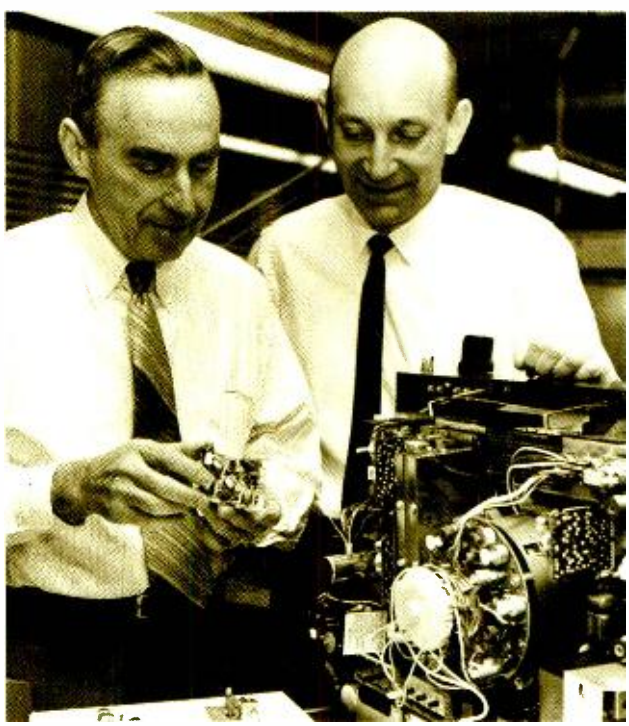
The Awards for individual accomplishment in science and in engineering were established in 1956 to commemorate the fiftieth anniversary in radio, television and electronics of David Sarnoff. The awards for team performance were initiated in 1961. All engineering activities of RCA divisions and subsidiary companies are eligible for the Engineering Awards; the Chief Engineers in each location present nominations annually. Members of both the RCA engineering and research staffs are eligible for the Science Awards. Final selections are made by a committee of RCA executives, of which the Executive Vice President, Research and Engineering, serves as Chairman.

The 1971 Individual Award in Engineering

Abraham Schnapf received the David Sarnoff Outstanding Achievement Award in Engineering **"for outstanding engineering leadership of the TIROS meteorological satellite team."**

Mr. Schnapf, as Program Manager of the ITOS/TIROS Program, has provided technical and managerial leadership for the world's most successful unmanned spacecraft. ITOS-I (formerly TIROS M) launched on Jan. 23, 1970, and still fully operational as of April 13, 1971, was the 20th consecutive orbital success in the program's 10-year history (1960-1970). The TIROS M design provided RCA with its first large three-axis space-stabilized platform capable of precise earth-orientation of a mixed group of earth-observation sensors for daily global mapping. This satellite, in orbit, can maintain all axes stabilized within 1° at all times. By combining the functions of two of its predecessors (the ESSA/TIROS Operational Satellites) into the TIROS M, overall program costs were reduced. Additional features provided global coverage every 12 hours, increasing quantity and quality of meteorological observations. Under Mr. Schnapf's direction, the ITOS/TIROS Program has been continuously setting records in aerospace technology: First global operation and satellite system; operational success which surpasses mission requirements for all spacecraft launched; day and night 12-hour global operation with ITOS; no interruption of the U.S. meteorological satellite orbital operations service since its inception in 1966.

The 1971 Team Award in Engineering

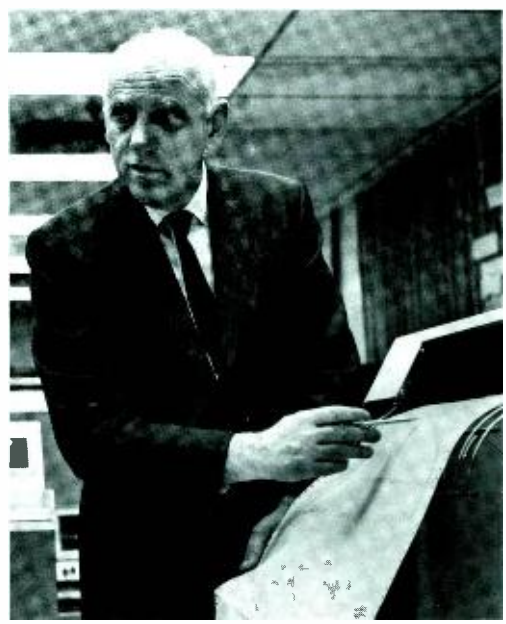


Jack Avins and **Bernard V. Vonderschmitt** received the David Sarnoff Outstanding Team Award in Engineering **"for excellence of team effort and leadership in the timely development of superior integrated circuits for use in television receivers."**

Messrs Avins and **Vonderschmitt** have made a truly significant contribution in adapting numerous scientific disciplines to enable the timely development of integrated circuits for use in television receivers. Since 1965, when RCA pioneered the first use of a monolithic silicon integrated circuit in a television receiver, outstanding progress has been made in developing other IC's for use in the signal processing circuits of a color television receiver. This significant achievement is exemplified by RCA's new solid state color TV receivers which use a minimum of five monolithic silicon circuits each. This extension of monolithic IC technology into substantially all the signal processing functions of a color TV receiver has been brought about by a team effort which has effectively utilized the engineering resources of both the Consumer Electronics and Solid State Divisions. The integrated circuits which are now available for use in television receivers are the complete picture and sound IF system, the Automatic Fine Tuning Function, the Complete Chroma Amplification and Color Synchronization Circuit, the Color Demodulation and Tint Control, and the Intercarrier Sound Function. These products of a team effort are an excellent example of what can be achieved when the extensive technical skills and creative interaction of numerous engineering disciplines available within different groups of RCA are directed by a concerted team effort, working toward new areas of mutual corporate benefit.

M. Robert Paglee, Ldr
Signal Processing Engineering
Missile and Surface Radar Division
Moorestown, N.J.
received the BSEE from Purdue in 1944 and joined RCA after graduation. He became associated with range instrumentation programs of M&SR in 1956, and has been active with range projects since that time He subsequently directed project engineering for a variety of AN/FPS-16 mod kits, which led to development of AN/FPQ-6 and AN/TPQ-18 radars. He was also associated with the pulse doppler program applied to the AN/FPS-16 and was responsible for the development of the first coherent pulsed beacon which was tested with that radar He subsequently directed the design of the first pulse doppler tracking capability for AN/FFQ-6 and AN/TPQ-18 radars at Wallops Is. and Vandenberg AFB He also led the extensive modification of two Pacific Missile Range radars which provided digital range tracking and pulse doppler velocity data capability. His group performed the design of the AN/MPS-36 radar velocity extraction subsystem which provided pulse doppler velocity data for the first time in a newly designed instrumentation radar. He was also responsible for the overall integration of the AN/MPS-36 and AN/TPQ-27 Radars signal processing and data handling designs. His group recently performed designs for the AN/FPS-95 radar exciter CEI, and the AEGIS MFAR Exciter. He is a member of Tau Beta Pi. Eta Kappa Nu, Sigma Delta Chi, IEEE, and the Delaware Valley Council. He currently holds two U.S. Patents and is a Licensed Professional Engineer. N.J. No. 17679.

D. R. Crosby
Central Engineering
Government Engineering
Camden, N.J.
received the BSEE from Rensselaer Polytechnic Institute in 1934 and the MS from Harvard University in 1935. From 1935 to 1941 he was employed as an engineer by the International Telephone and Telegraph Company. Since joining RCA in Camden, New Jersey, in 1941, he has been engaged in development work on high powered transmitters, RF transmission lines, antennas, microwave devices, modulation theory, circuit analysis, computer-aided design and computer applications to defect reporting in manufacturing operations. His part time teaching has included 14 courses at RCA and at Rutgers University in field theory and in mathematics. Five patents have been issued to him, and eight of his papers have been published in professional journals. Among his memberships are the IEEE and the Mathematical Association of America, also he is a Registered Professional Engineer.



John D. Mosley
Missile and Surface Radar Division
Moorestown, N.J.
received the BS in Eng. Physics from the Alabama Polytechnic Institute in 1952. He then joined the Missile and Surface Radar Division, designing range servos and other instrument servos for several radar systems. He developed a state-of-the-art magnetic drum drive system for BMEWS, with a synchronizing accuracy to the radar master clock of 1 part in 500,000. Subsequently he served as a design review chairman on all servo systems including magnetic disc, tapes and drum drives for all development projects at M&SR. He then served as semiconductor parts application specialist responsible for establishing preferred parts for M&SR designs and determining design practices for these parts across all programs. In 1964, he moved to RCA Commercial Systems where he was responsible for developing specifications and designing portions of a new line of solid-state commercial radars In 1970, he moved back to M&SR and joined the Signal Processing Engineering Group, where he performed development work on a practical derivative phase code frequency generator for the MFAR radar. He was also responsible for the development of a state-of-the-art 10-MHz digital clock driver and the low-impedance stripline system described in this paper.

High-speed stripline digital-clock distribution system

M. R. Paglee | J. D. Mosley | D. R. Crosby

As the need for processing digital information at higher speeds becomes more widespread, a method for distributing timing (clocking) pulses with great precision becomes mandatory. The stripline clock distribution system described in this paper feeds a 10-MHz timing square wave to logic gates in four parallel channels of digital processing equipment having a total of 288 loads spread fairly evenly over eight module nests, each 19 inches wide. The timing at corresponding logic gates must be maintained within ±3 nanoseconds from channel to channel.

DISTRIBUTION of 10-MHz timing signals over a wide area to a large number of devices requires either a small number of high-power drivers, or the *treeing* of a large number of low-power drivers, each having independent phase-shift adjustments to compensate for the timing errors introduced by the branching structure.

The choice of a few high-power clock drivers was made because of the excessive propagation delays, the multitude of adjustments, and the cumulative effects of switching tolerances which result from the use of many low-power devices. Furthermore, the high-power driver design permits use of non-saturating devices which allow closer control of differential delays, while introducing minimal absolute delays. It was concluded that four high-power drivers would be required; each driver would supply timing signals to a pair of module nests.

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Alternate distribution schemes

To distribute the timing pulses from each driver, several approaches were considered before selecting the stripline system. The possibility of using pre-cut matched lengths of twisted pair or coax cables was examined but rejected because of inherent inflexibilities.

Coax cables were disqualified because of the bulkiness of many parallel paths, complications in the end connections, cost, and excessive lengths required to traverse an entire nest. The latter difficulty contributed to the disqualification of long multiple twisted pairs, as did also their relatively high characteristic impedance. The possibility of extensive noise interference from signal leakage caused by incomplete field cancellation along the paths of lengthy twisted pair lines was also considered a disadvantage.

By comparison, the stripline offers significant advantages:

1) It provides a low characteristic impedance for efficient energy transfer at practical voltage levels both for source and loads.
2) It offers good shielding characteristics for minimizing crosstalk where high-energy transmission is required; and
3) It can be mounted conveniently between the nests and branching to the loads accomplished with short twisted pairs, thus minimizing the possibility of interference.

This arrangement is illustrated in Fig. 1. Because of the requirement to maintain highly precise timing (±3 ns) for each corresponding reclocking function in the four identical channels, the stripline is tapped at points convenient to every module location, and timing signals are branched from corresponding taps for each channel. This provides accurately matched delays at corresponding loads in the identical parallel channels.

Computer modeling and design

Implementation of the above concept poses several practical problems. To handle the total energy required, the

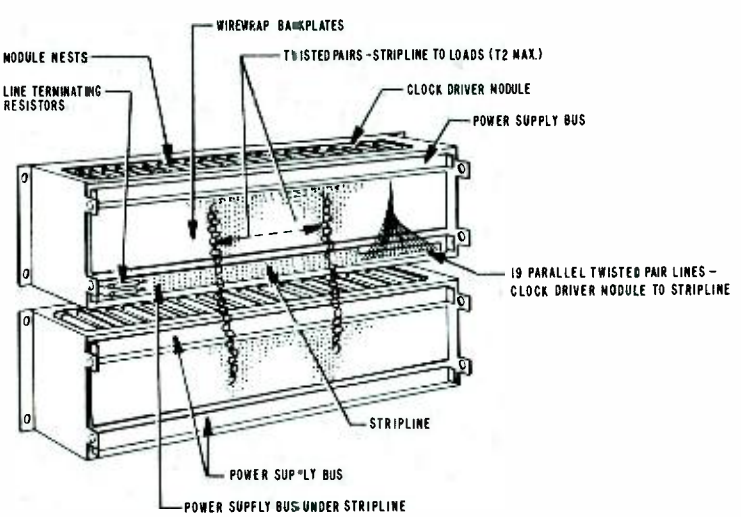

Fig. 1—Stripline clock distribut on system.

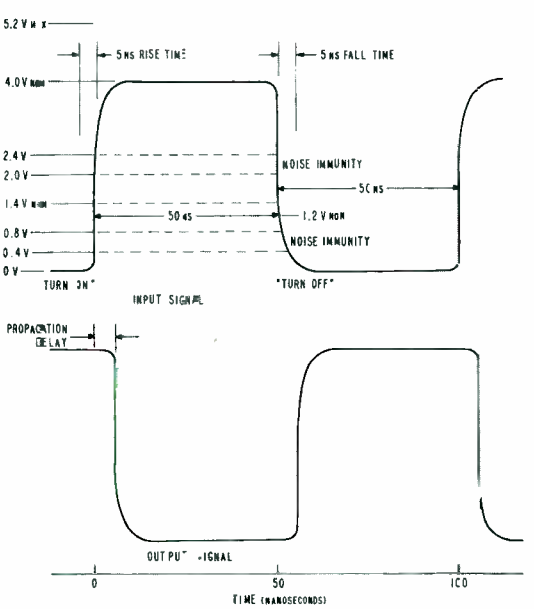

Fig. 2—Idealized TTL device waveforms.

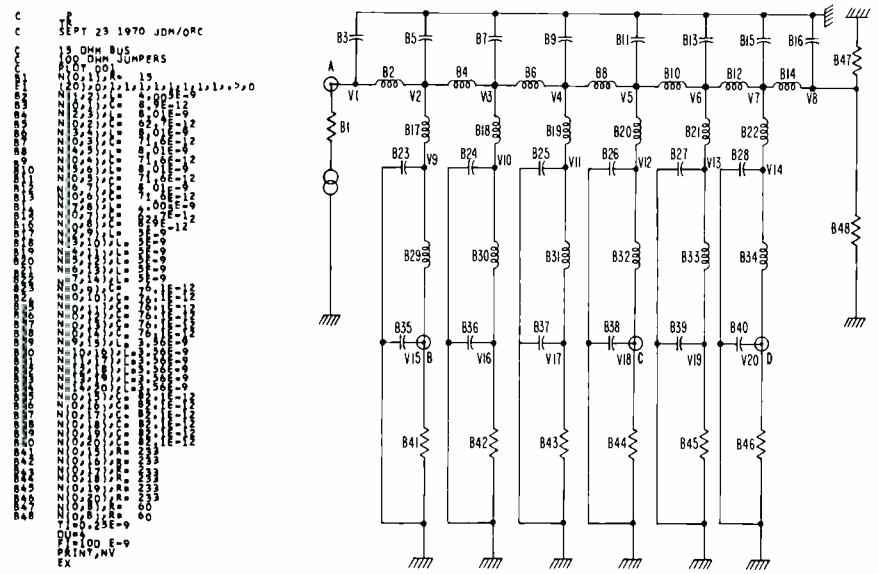

Fig. 3a—Computer input model for first computer run.

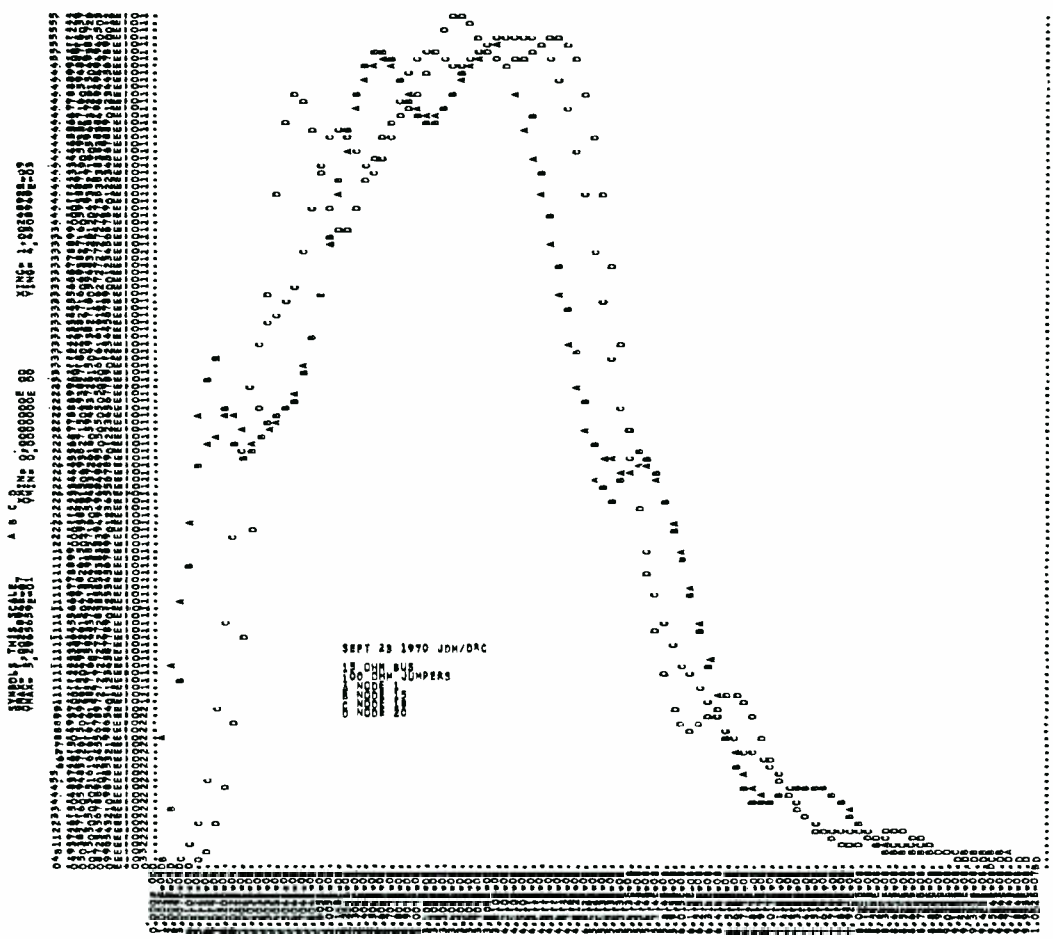

Fig. 3b—First computer plot waveforms.

stripline impedance must be comparatively low. The twisted pair represents the most appropriate means for branching, but as its characteristic impedance is comparatively high, its connection at the stripline presents a discontinuity. The loads of the logic gates represent a much higher impedance than the twisted pair characteristic. Terminating the lines with matching resistors would require excessive drive power, and matching them to each load through an impedance transformation would be costly, bulky, and difficult. The reflections from the impedance discontinuities cannot be ignored in the system design, yet their number is so large as to make manual design calculations completely impractical.

The proposed structure was modeled for computer analysis. Variable parameters included the source impedance, the stripline impedance and dielectric constant, the load impedances, the end terminating impedance, as well as an intermediate isolation impedance which was later found to be necessary. The waveform was assumed to have a risetime of 5 ns, a flat top which was varied between 35 and 40 ns, and a falltime which was varied between 10 and 5 ns.

Fig. 2 shows an idealized waveform at the input of any individual TTL device load. Note that the minimum turn-on and turn-off level is 0.8V, while the maximum is 2.0V. A noise immunity margin of 0.4V is allowed for each case as shown. Fig. 3 is a set of plots from the first computer run (001) and predicts unacceptable system performance (for the initial parameters chosen) due to a possible uncertainty of the time of "turn on" and "turn-off," particularly the latter.

The parameters assumed for this first computer run were: source and stripline impedance 15 ohms, terminated in 30 ohms; twisted-pair impedance 100 ohms; terminating impedance at one gate of 2800 ohms in parallel with 3.5 pF, for each of 72 gates. To simplify the modeling, the loads were arranged into six groups of 12 each, and distributed uniformly along the lines. The equivalent circuit is also shown on Fig. 3, and the one-twelfth values of all equivalent components are tabulated. The nodes corresponding to the plot letters (A, B, C, D) are also indicated on the circuit.

Fig. 3 indicates that for the assumed parameters, reflections from the various discontinuities result in summations at the various loads (B, C, D) which distort the desired waveform with unacceptable ringing. Nine additional sets of plots were made with many combinations of varied parameters. The stripline impedance was tapered and lowered, its dielectric constant increased, the source impedance lowered, and terminating impedances applied at the loads.

Although lowered source impedance and lowered line impedance yielded significant improvements, the system still appeared to be inadequate.

A computer analysis was then made of the waveforms produced by the reflections from a single logic gate. Through this analysis, it was deduced that the mismatch represented by the gate does not materially degenerate the waveform there, but merely produces a large, undistorted reflection. Therefore the effort to optimize impedance matching at the gates was put aside in favor of a study of the bus parameters, presuming that an optimum choice could render reflections from the gates relatively harmless. A means for isolating the loads from one another was also considered essential.

Eight additional computer analyses were then made for buses of 2-, 5-, 10- and 20-ohm characteristic impedance. Series isolation resistors between stripline and twisted pair jumpers were varied from 1.2 ohms to 100 ohms. The optimum results for practical parameters were achieved as shown in Fig. 4. In this case, the source impedance, the stripline impedance, and the stripline terminating impedance were each 5 ohms; the isolation impedance was 50 ohms, and the gates had no auxiliary termination. Note the prediction of acceptable pulse shape, and particularly the clean appearance of the leading and trailing edges.

Breadboard verification

As the computer modeling progressed, a parallel effort for breadboard verification was begun. A stripline was built having a characteristic impedance of 13 ohms tapered to 26 ohms, in accordance with the parameter chosen for early computer runs. The

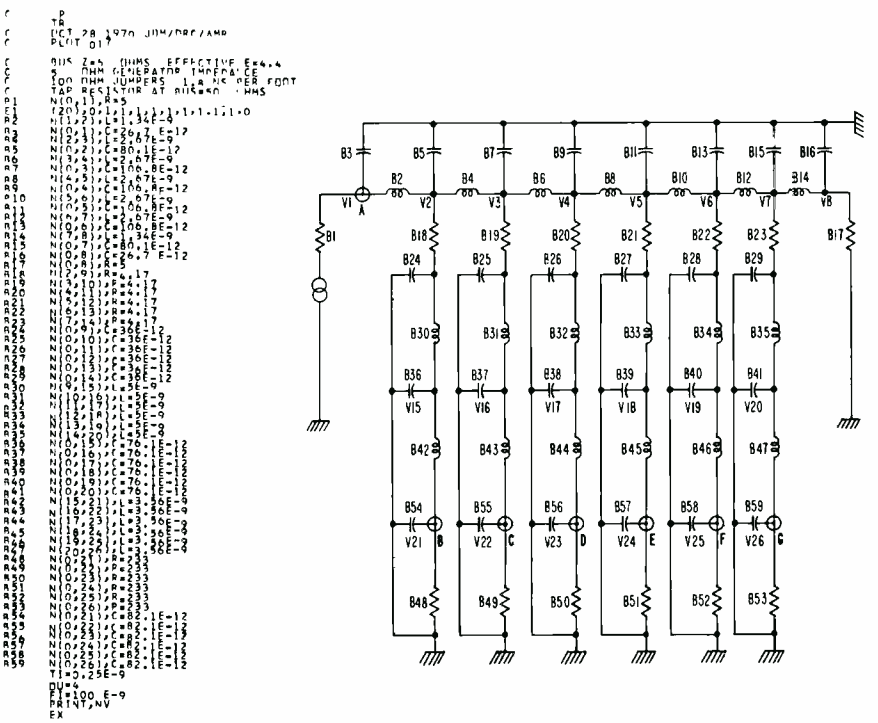

Fig. 4a—Computer input model for later computer run.

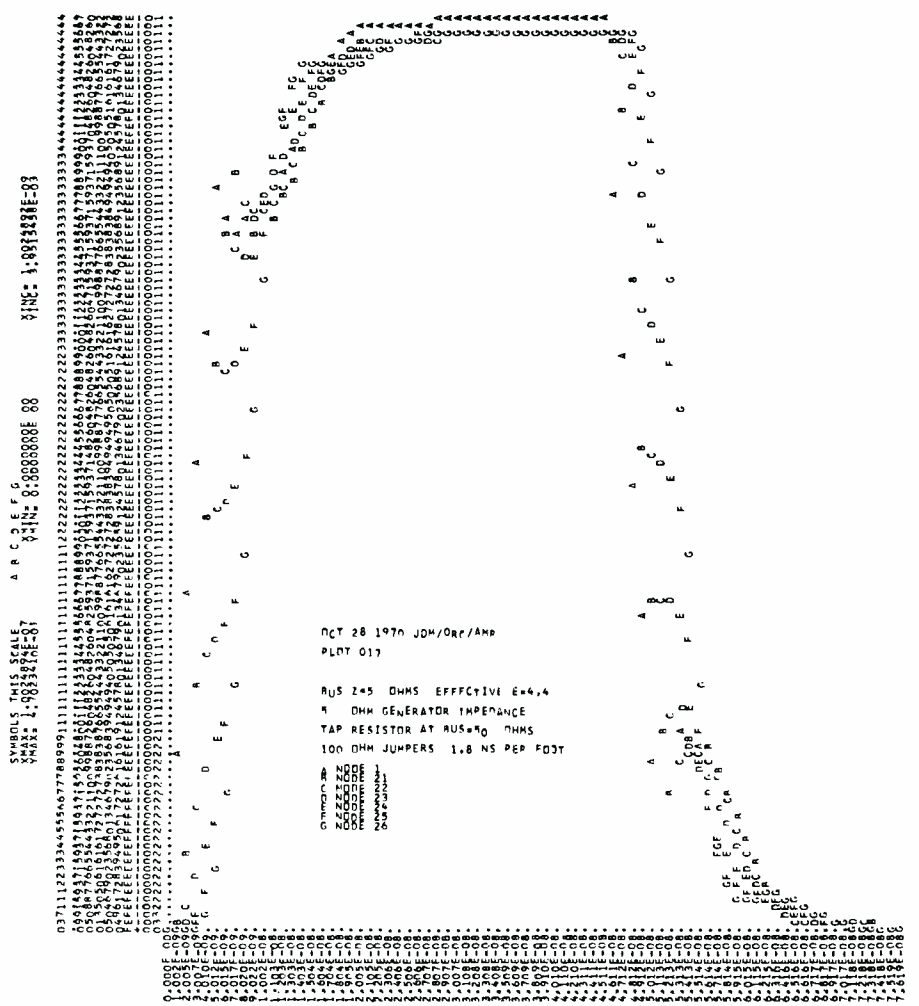

Fig. 4b—Revised computer plot waveforms.

stripline was interconnected with up to 72 gate loads using short twisted-pair lines spaced along the bus. It was terminated in 30 ohms.

In contrast to the ease of performing computer simulations, certain parameters of the breadboard system (such as the characteristic impedance of the stripline) could not easily be varied, so only a limited number of computer runs could be verified with breadboard data. Whenever such verification was possible, the test results appeared to be remarkably similar to the computer predictions.

When subsequent computer runs indicated the desirability of a lower stripline impedance, a spare 13-ohm bus was added in parallel to the first, yielding a composite breadboard line whose impedance tapered from 6½ to 13 ohms. The end of this line was terminated in 10 ohms.

The 72 loads were driven through the same short twisted-pair branches. However, 50-ohm isolation resistors were inserted in series with each tap on the stripline, because subsequent computer runs indicated significant improvement would thus be achieved. Test data verified this expectation, but it was noted that depending on the number of loads to be driven through any particular branch, the DC level would be shifted slightly, thus placing a limitation on the difference in the number of loads which could be driven from any two taps.

This objection was overcome through substitution of the isolating resistors with ferrite beads, one threaded on each tap to the center conductor of the stripline. Each bead couples a resistance into its threading conductor whose effective value is a function of frequency. The beads were chosen for their stated characteristics of 10 ohms at 10 MHz and 30 ohms at 100 MHz. Breadboard test results indicated performance of the beads was equivalent to that of the isolating resistors, yet the DC level shift was reduced at least by a factor of five, to the point where it was considered negligible.

The intermediate value of isolation impedance provides little attenuation to the forward signal passing from the low impedance stripline to the high impedance load, so most of the signal divides across the load. However, the energy reflected from the impedance mismatch at the load divides across the isolation impedance and the low-impedance stripline, with most of the reflected energy being dissipated in the effective resistance of the ferrite bead.

The choice of value for the isolation impedance represents a compromise between attenuation of the driving signal's high frequency components (slower risetime) and damping of undesirable reflections. Risetime for the signal at the devices depends on the number of loads to be driven from a single twisted-pair branch. The breadboard tests indicate that with up to six loads per circuit, risetime can be maintained between 5 and 8 ns over the entire system.

The breadboard was again reworked, substituting two non-tapered 13-ohm striplines connected in parallel to yield a characteristic impedance of 6 ohms. The terminating resistor was varied between 6 and 30 ohms, while other properties of the breadboard system remained unchanged. The performance of the tapered line was noted to be slightly superior to that of the untapered line, particularly when the terminating resistor did not match the impedance of the untapered line.

The use of a tapered line was therefore favored because less power need be wasted in a resistive termination which matches the impedance at its end. This was an important consideration for the design described because of the practical power limitation of available transistors which are suitable for the application.

Fig. 5a shows the waveform measured at the input to a gate near the source end of the 6-ohm tapered stripline; Fig. 5b shows the same waveform at a gate near the center of the stripline; and Fig. 5c shows the waveform at a gate near the end of the stripline. Note the presence of a "front porch" appearing at about 2.5 volts, and a "back porch" at about 0.5 volts. The similarity between breadboard results and computer plots is apparent from a comparison of Figs. 4 and 5. The small variations in level at the peak of the waveform are unimportant, because they do not affect turn-on or turn-off time.

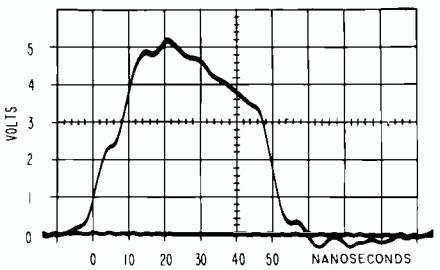

Fig. 5a—Device input waveform—beginning of line.

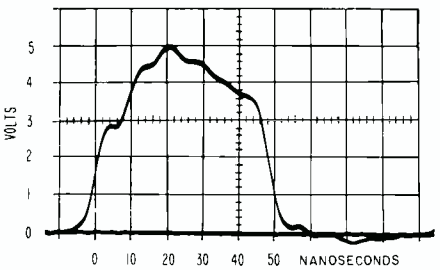

Fig. 5b—Device input waveform—center of line.

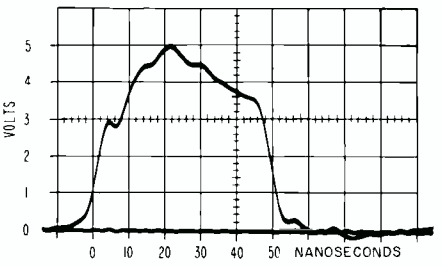

Fig. 5c—Device input waveform—end of line.

Application criteria

This stripline clock distribution system has application whenever the number of loads to be driven from a single source is between 30 and 75. It is particularly useful if clock pulse crosstalk can present a noise problem, or if constant controlled delays are required between parallel channels. It also has application if high load currents require a low transmission impedance, or if the spatial location of loads which must be driven from a single source is too widespread to permit compliance with high-speed circuit wiring rules.

In cases where only 15 to 30 loads must be driven, the stripline driver circuit can be used with twisted pairs or coax, omitting the stripline, provided crosstalk does not exceed acceptable levels, and line lengths are not excessive.

Because the clock driver is DC coupled, the clock distribution system can be used over a very wide range of frequencies. The breadboard system was operated satisfactorily from 10 kHz to 16 MHz. The maximum range of frequencies over which it could operate is even greater, but its limits have not been evaluated.

Large-core storage in perspective

Dr. J. G. Williams

Large-core storage is discussed, both in terms of how it has been used in the past and how it might be used in the future. In the past, memory hierarchies composed of large-core and core storage have proven to be more effective in certain applications than the more traditional drum and core storage hierarchies. In the future, a hierarchy composed of large-core and cache is likely to be even more effective.

A MEMORY DEVICE called *large-core storage* has been available for several years on certain third-generation computer systems. This device is similar in operation to other core memories, only it is designed to have a greater access and cycle time, and consequently it is less expensive per bit. This allows a larger memory to be built for a given cost, so that large-core storage may be considered for applications which are not suitable for a faster and more expensive core-storage device.

Thus, large-core storage is basically quite similar to other core-memory devices. What makes it unique is the way in which it is used. To understand this distinction, we must first discuss the idea of a memory hierarchy.

For a given cost, memory systems exhibit a trade-off between speed and size. Thus, a computer may be equipped with several memories, which are used together in a coordinated way to form a hierarchy. At *level 1* in this hierarchy, we will find a relatively small, fast store which is intimate with the processor. At *level II* we will find a larger and slower store which is cheaper per bit, and so on. It is the task of hierarchy management to make all of these levels appear as one store with the fastest possible average access time. This is achieved by moving information around in the hierarchy in a judicious fashion, so that the right information is at the right level at the right time.

Large-core storage is defined as a core memory device used at level II of a hierarchy. Thus large-core storage is a backing store, and is used in a coordinated fashion with the main memory at level I.

Table I ranks various memory devices by increasing level number, although not all of these devices would be available on any one computer system. A cache or main-core memory might be classified at level I and large-core or drum at level II. Table I is intended to be typical or representative of those memories which might be found on larger, third-generation computer systems. The cycle times for main-core and large-core storage have been specified as 0.75 and 4.0 μs, respectively, although on some systems main-core might be as slow as 2 μs while on other systems large-core storage might be this fast. The purchase prices are the third-generation prices as paid by the end user, and do not necessarily reflect current or projected manufacturing costs.

Type of memory device	Cycle time or mean latency	Size in bytes	Purchase prices in cents/byte
Cache	0.08 μs.	10^4	900
Main core	0.75 μs.	10^5-10^6	150
Large-core storage	4 μs.	10^6-10^7	25
Drum	8 ms.	10^6-10^7	2.5
Moving-head disc system	80 ms.	10^7-10^8	0.25

Table I—Typical third-generation memories.

In the following discussion we will consider some of the ways in which large-core storage may be utilized. At the present time, we are between the third and fourth generation of computer systems, and this will be our point of perspective. We will look backwards to the third generation, and see why large-core storage first came to be used. We will then look forward to the fourth generation, and consider how large-core storage might be used in the future.

Uses in the past

The drum/core hierarchy versus the large-core/core hierarchy.

At the start of the third-generation, which we will mark as the time when solid-state machines began to be used in a multiprogramming mode of opera-

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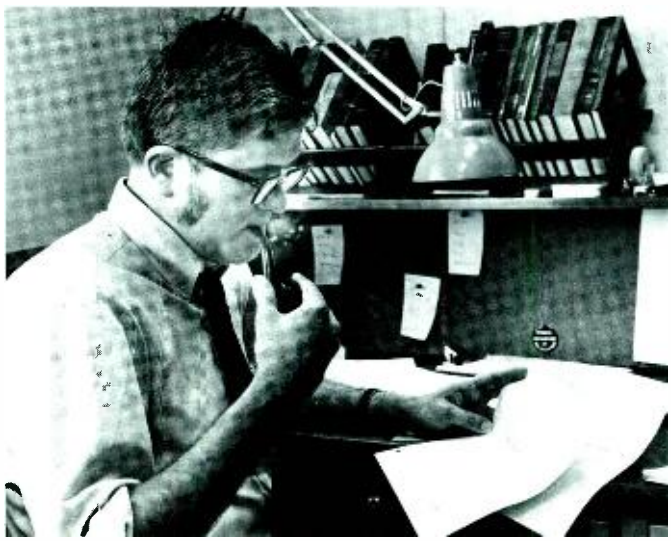

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tion with peripherals on line, a typical computer system might have included a hierarchy with main-core memory at level I, drum memory at level II, disc memory at level III, and tapes at level IV. In this case, only level I is directly addressable, since information at the other levels of the hierarchy must be moved to the main-core before it can be used by the processor. Level II, the drum, is used as a backing store to shuttle information in and out of the main core. Let us consider such an arrangement in more detail.

The drum is a rotating device, so there may be a waiting period until a particular block of information passes under a read head. This waiting period is called *latency*, and as shown in Table I, this time may average about 8 ms. If a program needs information from the drum to continue, then the program must be suspended until this information arrives. Since 8 ms is a relatively long time to wait, normal procedure is to initiate another program in the interim. This mode of operation is called *multiprogramming*, indicating that there may be a good deal of switching between a group of programs before any of these programs are finished.

The effectiveness of such a multiprogramming scheme can depend in a very critical way upon the drum latency time. This effect has been discussed at some length from both an experimental and a theoretical standpoint,[2, 14, 16] so we will limit ourselves here to an intuitive explanation.

When a program is suspended while waiting for information from the drum to arrive in main-core, there is a choice to be made: should the information already in main-core for this program be retained, or should this space be made available to the other programs which may execute in the interim? If this main-memory space is not made available, the number of programs which can be run to "mask" the suspension of the original program may be severely restricted. Since any one of these other programs may itself require information from the drum and hence require suspension, it is possible that no program could be run, and the machine must idle. If, on the other hand, we do make the main-memory space of the original program available to other programs, then the original program may not run when we attempt to continue it. In this case the drum may be needed to reinstate the canibalized information, which means that the corresponding drum latency must also be masked by the execution of other programs, and so on. It can be seen that such a scheme could depend in a very critical way upon the drum latency time, as indeed it does.

	Hierarchy with Level II: drum Level I: cache	Hierarchy with Level II: large-core Level I: core
Page size	4096 bytes	4096 bytes
Mode of page movement	Combination of hardware and software	Combination of hardware and software
Page access time	8 ms. mean latency +4 ms. transfer time=12 ms.	0 latency +2 ms. transfer time=2 ms.
Level II size	$2 \cdot 10^6$ bytes	$2 \cdot 10^8$ bytes
Level II purchase price	$50,000 (2.5 cents/byte)	$500,000 (25 cents/byte)

Table II—The drum/core hierarchy versus the large-core/core hierarchy.

All of this is well understood now, but only as the result of experience with certain third-generation systems which did not perform as expected. In many cases the drum/core hierarchy was found to be effective. In fact, there are many instances in which a disc/core hierarchy has been effective, when properly used. However, on other systems, and particularly on larger systems with real-time commitments, it was found that the drum latency time was simply too long. Since this problem was not fully appreciated until after the complex hardware and software of these systems was well under way (or, in some cases, completed) it was extremely valuable to have a pure hardware solution which would not interact strongly with the existing system design. The solution was to replace the drum at level II or the hierarchy with large-core storage.

Table II compares the drum/core and the large-core/core hierarchies, using representative third-generation values. Note that information is moved between levels of the hierarchy in fixed-size units called *pages*. The time required to move a page between level I and level II is called the *page access time*. It is composed of the time required to find the location of the information in level II (the *latency time*) and the time required to move the information between levels (the *transfer time*). For the large-core/core hierarchy we see that there is no latency and that the transfer is typically less than for the drum/core hierarchy. Taken together, this means that the typical page access time for the large-core/core hierarchy is only one-sixth that of its drum/core counterpart.

This advantage does not come cheaply. Large-core storage costs about ten times as much as drum storage of the same size. However, for certain larger-scale systems, it may make the difference between poor performance and desired performance. Further, on these larger systems the added cost of the large-core storage is a smaller fraction of the total system cost. Thus, large-core storage first found application on systems of this class.

A smaller page access time is not the only advantage of large-core storage. Another advantage is that large-core is *directly addressable* by the processor. This means that instructions may be executed from large-core storage and that data may be accessed and stored in large-core storage, and that all of this may take place without moving the pages in question from the large-core storage to the main-core memory at level I. The large-core, at level II in the hierarchy, may simply be made to appear as a continuation of the main memory space at level I. With this capability the following question presents itself: should a page be moved from the large-core to the main-core when it is needed, or should it be addressed in the large-core directly?

In a way, this question resolves itself quite simply. There is a certain overhead associated with moving a page from large-core to the main-core storage. However, once a page has been moved it may be addressed by the processor in a shorter time. Thus a page should be moved if it is addressed often enough that the shorter cycle time of the main-core more than defrays the overhead costs associated with moving the page. In other words, those pages which are addressed more often (termed the more *active* pages) should be moved. The problem is to determine, prior to their use, which pages will be the more active.

Within the context of existing operating systems, there have been several

experimental attempts at page activity estimation. Some of these attempts will be discussed in more detail later. The general problem of page activity estimation has also been the subject of a theoretical investigation at RCA Laboratories.[10] As a result of this study, a method of detecting the higher activity pages has been developed. This method assumes no knowledge of the page activity prior to processing; rather, it uses the activity of the pages themselves to determine which pages will be the more active.

As an example of this method in use, it was found for the several programs studied that the 50% of the pages which are the most active account for about 95% of all the activity. Using this algorithm, one can move 50% of the pages from large-core to main-core, while directing about 80% of all the addressing references to the main-core. Since any random selection of 50% of the pages would account for an expected 50% of the activity, it can be said that this algorithm is about $(80-50)/(95-50)=2/3$ as effective as it possibly can be.

We have discussed the two main advantages of large-core storage with respect to drum: the shorter page access time and the ability to address information directly. We now turn our attention to several installations where large-core storage is in use, and see how these advantages have been exploited.

For the first example, consider the computer complex used by NASA in Houston for the real-time monitoring and support of the Apollo missions.[8, 9, 18] This complex, which uses five System 360/75 machines, is certainly an example of a large-scale system which must meet stringent real-time commitments. Each of these machines has a hierarchy with 1024κ (κ=1024) bytes of 0.75 μs main-core memory at level I, 4096κ bytes of 8 μs large-core storage at level II, and disc storage units with a mean latency of about 90 ms at level III.

This complex is under the control of a special operating system called Real-Time Operating System (RTOS), which is a modified version of the standard operating system OS/360. Under the management of RTOS, large-core storage is used to give the disc units the appearance of a faster access time. When a data or program module is copied from disc to the main-core memory, a copy of the module is also entered in large-core. If the module is requested from the disc again, it will actually be supplied from the large-core storage at a greatly reduced access time. As is always the case with such schemes, there is a mechanism for moving modules back to disc when the large-core becomes crowded.

All of these manipulations can be made "transparent" to the user of RTOS, who simply sees the arrangement as an extremely fast disc. There are, however, several facilities which allow a knowledgeable user to aid the system in utilizing the large-core efficiently. For example, a module can be loaded from disc to large-core prematurely. This facility is valuable when the system must meet a stringent real-time commitment, since the module will already be in large-core when it is first required. Modules which are known to have a low frequency of use can be marked to never reside in the large-core. Alternatively, a module with a high frequency of use can be made permanently resident. This latter facility can be applied to certain modules of the operating system itself, which are known to be used frequently.

It is asserted[8] that the system simply would not meet its real-time commitments without large-core storage. Since the use of large-core storage is an integral part of RTOS, it is not possible to run the system without large-core for comparison. As an experiment, however, a 360/75 was run in a job-shop environment with and without using large-core for the residence of certain operating system routines. With the routines resident, the throughput time for a stack of representative jobs was reduced by more than one half. Further experimental and simulation results confirm this result.

The Triangle Universities Computation Center (TUCC), which is the central facility of a network which provides computation services to universities and colleges throughout North Carolina, is an installation of more modest size. At TUCC, there is one System 360/75 machine with a memory hierarchy consisting of 512κ bytes of 0.75-μs main-core memory at level I, 2048κ bytes of 8 μs large-core storage at level II and disc storage with a mean latency of about 90 ms at level III.[5, 6, 7] Thus, at levels I and II in the hierarchy, there is exactly one-half of the memory to be found on each of the five machines used by NASA at Houston.

The TUCC machine is under the control of a modified version of OS/360. These modifications allow large-core storage to be used in several ways. A small portion of large-core (about 80,000 bytes) is given over to low-usage subroutines from the operating system itself. These routines are executed directly from large-core, without first being moved to the main-core memory. Although execution in large-core storage is about ten times slower, this mode of operation has been found to be effective since the overhead in moving these subroutines to main-core memory is not incurred. Of course, this strategy works because these subordinates are run often enough that their execution characteristics have been studied and are well understood.

The largest portion of large-core (about 1,350,000 bytes) is used for what is called the *hyperdisc*. This arrangement, which is similar to that implemented by NASA, allows the most recently used disc tracks to reside in large-core storage. In operation, it has been found that only one or two percent of the disc requests require a retrieval operation from the real disc, the remainder are satisfied by obtaining disc images from large-core.[7]

The large-core storage is also used in other ways. Small portions are used for job control information, operating system tables, checkpoint information, and accounting data. There is also a technique whereby over one million bytes of large-core may be made available to programmers who must manipulate large data arrays.

Taken together, all of these facilities have greatly improved the throughput of the TUCC system. It is reported[5] that the unmodified disc-oriented operating system spent 85 to 90% of its clock time in the CPU-WAIT state. With the modified, large-core oriented system, this figure was reduced to 30 or 35%. Said another way, the processor activity had been increased by a factor of four or five.

At the computation center of Carnegie-Mellon University, large-core storage

has been installed on a System 360/67 time-sharing system. The memory hierarchy is the same as that of the TUCC machine, except that 4096K bytes of large-core storage are available instead of 2048K.

Most of the reported work at Carnegie-Mellon has been concerned with using large-core storage as a directly addressable device.[3, 12, 17] As discussed, the central problem here is that of determining which pages should be addressed in the large-core directly.

On the Carnegie-Mellon system, the shorter access time of the main core memory will more than defray the overhead cost of moving a page, provided that the page is to be addressed more than about 1700 times.[17] For convenience, let us call those pages which are addressed more than 1700 times *high activity pages*; the others, *low activity pages*. Thus we wish to address the high activity pages in the main-core and the low activity pages in large-core storage. The problem is to discriminate between these two classes of pages.

At Carnegie-Mellon a series of experiments have been conducted to this end. In one of these experiments, all of the system pages were assumed to be of high activity and all of the user pages were assumed to be of low. A version of the operating system TSS/360 was modified to implement this decree. The user response time with this modified system was reduced by a factor of two or three. As of the latest report,[17] the operating system is being modified so that any page can be designated to be of high or of low activity, and treated accordingly. It will also be possible to designate pages dynamically, although it is not clear how the information required to perform this dynamic designation will be developed. It is suggested that special-purpose hardware may be required.

Uses in the future

The large-core/core hierarchy versus the large-core/cache hierarchy.

We have discussed large-core storage as it has been used in the past, and we have seen that it has been especially valuable for improving the performance of certain larger-scale, third-generation computer systems. We have also noted that large-core storage was somewhat of an afterthought, so that it was necessary for the device to find its place within an existing system design. But if we were to design a system from the start, knowing what we know now, would we use large-core storage in the same way? There is considerable evidence that we would not, as we shall now see.

With the benefit of hindsight, let us consider some of the parameters of the large-core/core hierarchy. For a start, consider the page size, which is typically 4096 bytes. This size is a carry-over from the drum/core hierarchy, where paging schemes were first developed.[4, 11] With a drum, the rotational delay (latency) is not a function of the page size, so a larger page is reasonable. Having paid for the rotational delay, it is desirable to obtain a relatively large block of information. With large-core storage this problem does not arise. There is no latency, so page access time is simply proportional to transfer time, which is proportional to page size. Thus, from the standpoint of the hardware page access time, there is no reason to prefer one page size over another.

There is experimental evidence that programs tend to use certain "natural" blocks of program and data, and that these blocks tend to be considerably smaller than 4096 bytes.[1] This means that many of these "natural" blocks must be packed into one 4096-byte page—a process which can cause both excessive page traffic and the loss of memory space which is called *internal fragmentation*.[15] All of this suggests that a smaller page size might be appropriate. Let us call these smaller pages *mini-pages*, and, for the sake of discussion, let us assume that they are 32 bytes large.

The use of mini-pages offers other advantages. In a large-core/core hierarchy with 4096-byte pages, the page access time is still about two ms, which is too long for the processor to remain idle. Thus, the system must be able to switch to another program in the interim. This is implemented through a system of hardware interrupts and software routines, all of which take time and add complexity to the operating system. This arrangement also requires the operating system to always have another program to run, which is, in itself, an added burden. With mini-pages, all of this can be avoided for the interaction between large-core and main-core, although, of course, it will still be required for the interaction with slower devices such as discs and tapes, where mini-pages are not appropriate.

Suppose that we take a large-core storage device with a bus width of 8 bytes, which is interleaved 4 ways. Then it is possible to obtain a 32-byte mini-page in one memory cycle. With this arrangement, we can afford to wait for a mini-page from large-core to arrive. In fact, we can afford to delegate the handling of the mini-page traffic between large-core and main-core completely to the hardware, since the complexity of initiating another program to "mask" the page movement is avoided. With this function in the hardware, the main-core at level I can even be made "transparent" to the programmers who implement the operating system, who can then use the memory space of the large-core storage with no thought as to how the movement of mini-pages in and out of the main-core will be accomplished. Of course, a little thought on their part might be helpful, but the point is that by delegating these functions to the hardware once and for all the operating system design can be simplified.

Assuming that mini-pages are moved in and out of level I, consider some of the other parameters of the large-core/core hierarchy. In particular, consider the size of the level-I memory.

When a 32-byte mini-page is brought to level I, it is likely that a large portion of its information will be needed in the near future. By contrast, when a 4096-byte conventional-size page is moved in, it may contain information which is not required in this particular part of the program at all. As noted earlier, a large page may be packed with various "natural blocks" of information which, from the standpoint of the logic of the program in question, may have little to do with one another. Thus, when using mini-pages, there is no reason to assume that the level I memory must be as large as it would have to be when using pages of a more conventional size.

From the previous discussion of large-core/core hierarchies at NASA, Triangle Universities Computation Center, and Carnegie-Mellon University, recall that the main-core memories at level I were at least 512$_K$ bytes large. This means that there is room for at least 128 pages, with each page containing 4096 bytes. But 128 mini-pages, each containing only 32 bytes, would fit into a level I memory which is itself only 4096 bytes large. For the sake of discussion, let us assume that level-I memory is 8192 bytes large, providing room for 256 mini-pages.

With a small level-I memory, other advantages accrue. Since the memory is actually physically smaller, it may be brought physically closer to the processor, thereby reducing cabling delays. Also, since it is smaller, it is reasonable to make it much faster. For example, an 8192-byte level-I memory could be made using integrated circuits. A fast level-I memory is extremely desirable, since it can provide a much better match to the internal speed of the processor itself.

Assuming that all of these modifications are made, what do we have? We have a level-I memory which is now a cache, and we have a large-core/cache hierarchy.

The large-core/cache hierarchy has been in use for several years, with the first instance of its use being on the System 360/85.[13] A *cache* is simply a small, fast memory used at level I of a hierarchy, with hardware management of the mini-page traffic which flows in and out of the device.[10]

Table III compares the large-core/core and large-core/cache hierarchies, using representative third-generation values for the various parameters involved. At level I in the hierarchy, cache is more expensive than core per byte, but fewer bytes are required. On balance, the cache memory is likely to be less expensive. Although memory costs are decreasing rather rapidly at the present time, they are changing in such a way that this conclusion is likely to remain valid in the foreseeable future.

The large-core/cache hierarchy has been the subject of extensive investigation by Ken Kaplan, Toni Robbi, Joe Weisbecker, and Bob Winder at RCA Laboratories.[20] If we appear to have been a bit cavalier in modifying the parameters of the large-core/core hierarchy in the discussion above, it is because these studies have shown that the large-core/cache hierarchy can be quite effective. It offers the potential for a hierarchy which is less expensive, easier to use, and effectively faster than the hierarchy composed of large-core and core.

	Hierarchy with Level II: large-core Level I: core	Hierarchy with Level II: large-core Level I: cache
Page size	4096 bytes	32 bytes
Mode of page movement	Combination of hardware and software	Hardware, transparent to user at machine language level
Page access time	0 latency + 2 ms. transfer time = 2 ms.	One large-core cycle = 4 μs.
Level I size	262,144 bytes	8,192 bytes
Level I cycle time	0.75 μs.	0.08 μs.
Level I purchase price	$393,000 (150 cents/byte)	$74,000 (900 cents/byte)

Table III—The large-core/core hierarchy versus the large-core/cache hierarchy.

Summary and conclusions

This paper has dealt with large-core storage, both in terms of how it has been used in the past and how it might be used in the future. The way in which large-core storage first came to be used and the advantages which the large-core/core hierarchy has to offer over the hierarchy composed of drum and core have been placed in perspective. These advantages are the shorter page access time of the large-core and the ability to address the large-core directly.

While large-core storage has improved the throughput of certain third-generation systems, these systems were not initially designed with large-core storage in mind. With the freedom to manipulate all of the parameters of the large-core/core hierarchy, we have argued that the large-core/cache hierarchy may be used more effectively. Thus, in the future, we might expect to see large-core storage used primarily with cache. This is not really in the nature of a prediction, since large-core/cache hierarchies are already coming into increasing use.

Acknowledgments

Gratitude is expressed to Mort Lewin, RCA Laboratories, who suggested large-core storage as an area of investigation. Thanks are also etxended to Ken Kaplan, Toni Robbi, Joe Weisbecker and Bob Winder, also RCA Laboratories, for discussions concerning various aspects of memory hierarchies.

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Outguessing the technical future

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In the development of computer systems within RCA, certain constraints challenge the engineer to an unusual degree. Some of these constraints exist in the engineering work of other product lines, but the total combination, and the resultant problems, are unique to the commercial computer business. They create the need for the engineer, in making his design decisions, to consider a much larger slice of time than is required in most other areas. They make him much more conscious of the future and its hazards.

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*Since this article was written, Mr. Kleinberg has been named Manager, Corporate Standards Engineering, Corporate Engineering Services.

BRIEFLY LISTED, the following factors very strongly affect the computer engineer's work.

1) *Technologically the computer business is explosive.* New "generations" are born on a five- to ten-year cycle, and the curve of improved performance shows no sign of flattening.
2) *Lead times are long.* A cycle of 18 to 24 months from specification to first manufacturing delivery is not uncommon.
3) *The product life is long.* While this may seem to contradict the rapid change of technology, it does not. The fact that much of the product is leased means that corporate ownership goes on for many years, and many design decisions must be based, not only on initial manufacturing cost, but on a number of factors that will exist during the entire lease life of the system.
4) *The field is highly competitive.* Sales are made today mainly on the basis of a low cost-to-performance ratio.
5) RCA's percentage of the total business is growing on a healthy curve, but it is still relatively small. This means that RCA has not been able to set the technological pace.
6) *The product is complex.* In combination with software and with the great variety of possible peripheral and computer configurations, comparative performance of competing systems and the value of alternate choices in the same system are almost impossible to measure in the abstract.

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The combination of all these factors makes the engineer embarking on a new system design feel an affinity to a youngster riding a surfboard. If you've ever watched this being done, you'll have observed that the problem is for the rider to stay on the lifting wave front without getting too low or too high. If he drops too far, he loses lift and momentum and gets swamped by the wave coming from behind. If he gets too high, the turbulent peak spills him to an abrupt and undignified "wipe-out".

In much the same way, the computing system designer must carefully pick his spot on the wave of changing technology. If he is too cautious he will be swamped by onrushing competition. If he is too adventurous he will be spilled by the hazards of unproven techniques and components.

Technology

. . . remember that the design decisions made today will still be sold, manufactured, and installed six or seven years from now.

There are five areas in which these considerations give the design engineer problems that sometimes make him wish he had taken up a more placid occupation. The most immediate of these is choice of technology. New components, devices and materials are constantly coming onto the market. They pour out of the research laboratories at a steady rate, and every one of them offers potentially higher performance, or lower cost, or less power drain, or some other solution to a tough problem. In every case, the initial problems are great, but the promise of the classic learning curve holds out a future in which solutions are found, and the early hopes are realized. And in many cases, this vision comes true. But which solutions will they be? When should the present, well-known hardware be traded for the future, hopefully better, device?

Probably the most outstanding example of durability in this regard is the coincident-current core memory. It displaced the competing electrostatic tubes and sonic delay lines in the early 1950's, and today is still the major memory in production in the industry. It was constantly challenged during this time by a number of competing technologies, ranging through an assortment of ferrite plate devices, thin films, cryogenics, and plated wires. All of these were studied in RCA as possible successors to the core, and in each case, the decision (quite correct, as it turned out) was made to stay with the core.

Today another challenger—the integrated circuit, or solid state, memory —is on the scene. Will it be the technology that finally displaces the old core, or will it prove to be another one that fails to make it? And in making your forecast, remember that the design decisions made today will still be sold, manufactured, and installed six or seven years from now. They must remain competitive over at least that period of time.

Another example of this kind of problem was the transistor versus integrated circuit choice that had to be made in 1964, during the early development of the Spectra series. At that time computer transistor circuitry had been developed to a high degree, while the integrated circuit was a device of unproven performance on a production basis, and one to which no other computer manufacturer had yet committed. The decision to go with the new was a bold and, again looking with hindsight, a correct one.

Cost

There is a fairly dependable curve of how costs decrease with time, but it has validity only in a relatively large potential market with competing suppliers.

Closely related to the technology problem is the question of cost. This goes beyond the normal considerations of manufacturing cost, and must, as stated before, take into account the lease nature of the business. In most cases, the cost of maintenance is included in the monthly rental rate, so that an increase in factory cost to obtain a reduction in maintenance cost can be very good economics indeed. But there is a limit to which this trade-off can be carried. Unfortunately, there is no general equation for determining this limit. Judgment and experience are the major guides.

The cost of maintaining an inventory of spare parts is a problem closely related to maintenance, and it is a factor in many design decisions. For at least seventeen years that I am aware of, the debate over special versus general purpose logic plug-in has been one in which the spare parts problem has been central. With the advent of medium and large scale integration, the argument is moving from the plug-in to the chip, but it is not changing in its basics.

While the costs after installation are important, manufacturing cost cannot be neglected. It is one of the basic factors in the technology decisions previously discussed. The core memory has lasted as long as it has because it matched all competing technologies in performance, and bettered them in cost. There is a fairly dependable curve of how costs decrease with time, but it has validity only in a relatively large potential market with competing suppliers. It is here that RCA's relatively small share of the market comes to be a factor. We must be quite cautious, when choosing a new device, that we do not get caught in a backwater of technology in which, for lack of other large users, the device price will not come down as expected.

Manufacturing

. . . distance is the enemy of speed.

The third area in which problems must be anticipated is in manufacturing techniques. The rapid change in technology has carried along with it an equal change in the demands placed on manufacturing. This goes beyond the normal requirement that every industry faces today: to modernize and automate its production or else fail to remain competitive. In this case, the spiraling demands of system performance have forced the use of new assembly techniques, not because they are less costly, but because the demands can be met in no other way. The basic spiral starts with circuit speed. As speed goes up, of course, distance becomes an enemy. But as speed goes up, the system designer makes his computers increasingly more complex to achieve better balance between the very high internal speed, and the sluggish electro-mechanical world of the peripherals where some things take forever to happen, like maybe 5 milliseconds. But the greater complexity means more components, which means more wiring to interconnect them, both of which mean a bigger computer, which means more distance between components. But distance is the enemy of speed.

This cycle leads to an absolute requirement for greater packing density of components, and the density has arrived at the point where interconnections must be printed in several layers, and what "normal" wires there are must be handled as automatically as possible. The precisions required, and the massive documentation problems engendered by the wiring complexity, have led to the mandatory use of the computer as an interface between engineering and manufacturing. Both organizations have had to develop tools and disciplines to adapt to the change.

In case this brings to mind a picture of a robotized factory grinding out computers, let me hasten to explain that there is still a great amount of hand assembly in a computer, much of which will not be economically mechanized for a long time. My main point is that the pursuit of the nanosecond as a goal in itself is sterile. At every step, the designer must ask "Can it be built?" If it can't, what changes are required in the way of new equipment, new facilities, and new skills? And is the cost worth it?

Maintenance

Where in this maze of interconnected events did something happen that shouldn't have?

In much the same way that engineering technology can out-race the ability of a factory to produce, it can completely swamp the only technical member of the organization that most customers ever see—the maintenance man. His problems can be staggering. Look at the world the way he sees it.

In a fairly typical time-sharing system, users all over the country sit at a variety of terminals running an endless mixture of programs, tested and untested. Their communication with the computer is over telephone lines, and nobody knows how many miles of what kind of wire or microwave is being used this time. The lines come together, finally, in a computer room where dozens of complex devices are storing, retrieving, and processing the data. They contain tens of thousands of circuits, all responding logically and, hopefully, correctly to their inputs. In the core resides a "software" system of its own ghastly complexity, but known to have at least one "bug", and the whole is attended by a crew of operators who may or may not know what they are supposed to do. And then the whole thing stops.

What went wrong? Where in this maze of interconnected events did something happen that shouldn't have? The man who is expected to solve the problem—and quickly—is the Field Engineer. And he needs all the help he can get. Indeed, as system complexity increases—and it will—his job will rapidly become hopeless unless he gets a great deal more help from the computer itself.

Until now, the amount of hardware designed into a system to help the tester in the factory and the maintenance man in the field has been a matter of economic trade-off. In the future, it will, like production automation, be a matter of there not being any other way to do it. Ideally, a self-diagnosing black box or program would solve the problem, but we have no idea how to design them. There are, of course, less than perfect solutions which involve the normal kinds of engineering compromises between benefits and drawbacks. None of them is really satisfactory at this time. It is in this general area that the greatest challenge to the systems designer lies. It is difficult and largely unexplored, but the benefits to be gained are immense.

Reliability

. . . sound judgement has a great deal of validity.

The final area in which the future holds hazards for the designer is in reliability. The days have long passed when a computer user was happy and impressed that his wonder machine worked at all. And, while it is rarely a life or death situation in the commercial world that a computer be operating at a specific time, an unreliable computer cannot be tolerated. Many users have incorporated their systems deeply into the very heart of their business. Production scheduling, order processing, payroll, and many other vital operations no longer can be done manually. And production lines shutdown, orders not filled, or workers not paid because of a malfunctioning computer, are problems that a customer takes very seriously.

The changing technology, the long lead times and the long product life all conspire to make this a difficult area. What is the long-term reliability of a device that is being made for the first time? Does a 500-hour test of 100 units of a new component give a true picture of 10 units after 5,000 hours? Of what value is the "classical" reliability approach to component failure prediction in the world of large-scale integration and multiple layered printed circuits? These questions plague the computer engineer, and remember that he has time to go through the design only once (or maybe 1.5 times).

He is not completely at sea, of course. History of similar devices has some validity. Accelerated testing has some validity. And sound judgment has a great deal of validity. In general, the major defenses the designer uses are very conservative worst case design limits, and a conviction that all component vendors are rogues and thieves who must be carefully instructed and checked. As more and more of a system's logic becomes dependent on a vendor's process control, this suspicion will have to grow, and vendor inspection will become more rigorous.

Conclusions

These factors of changing technology, cost, manufacturing problems, maintenance, and reliability are the variables that must be optimized over a design life of six to ten years from start of design. While the primary discussion here has been with respect to the computer, the same problems exist in all associated system devices.

The peripherals, in fact, have additional problems in two areas—mechanical motion, and the diversity of media with which they must work. The first of these involves fighting the well-known enemies of inertia, friction and wear; but the second brings a wholly new set of problems. Magnetic tape, disks, paper, etc. vary widely from one vendor to another, and there is a long history of sudden problems in the field when a new magnetic tape turns out to have a soft oxide that gums up the head, a new paper tape is too heavily oiled and becomes transparent to the optical reading system, a new kind of paper generates too much static electricity and won't stack properly in the printer, and on and on. The designer learns each time, and incorporates his experience into his new designs; but the future has its ugly surprises which can only be handled as they arise.

The recitation of all these problems may give the impression that only a masochist would enter the field. But the gratification of successfully overcoming these challenges makes the effort well worth while, and leads to an enthusiastic anticipation of the next set of problems.

A 1-kHz power system for commercial computers

K. Hoffman | S. Kuo | R. Notaro | G. Schulze

Since 1964, series-regulated power supplies have been used exclusively by RCA Computer Systems to provide regulated DC power for computer devices. This technique affords excellent regulation, but problems of efficiency and size appear in the 2- to 10-kW range. To deal with these problems, the Power Systems group is studying a 1-kHz power system which offers increased efficiency with some loss in regulation. Cost and size at various power levels are other significant tradeoffs. In describing the 1-kHz system, this paper emphasizes that no single system is best for every application. A simple performance-measurement technique provides a quick comparison of the 1-kHz system against series-regulation devices in specific instances; hence, tradeoffs are readily identifiable in selecting the proper power system for a specific application.

FOR THE PAST SIX YEARS, Computer Systems has been using series-regulated power supplies exclusively to generate DC power for computer devices. While this technique provides excellent regulation, it has some serious drawbacks when applied to power systems in the 2- to 10-kW range. The most serious problem is efficiency: a 5-volt, 400-amp supply has an efficiency ranging from 25% to 35%. Thus, about three kilowatts of input power are required for each kilowatt of output. Accordingly, a customer must provide excessively large primary power distribution systems and additional air conditioning. A second objection in series-regulated supplies is size for high-power systems. While this is less serious than the efficiency problem, it can result in loss of a sale if too large a layout is required.

No single power regulating technique is best for all applications. However, to alleviate the two problem areas, a 1-kHz power system is being studied by RCA Computer Systems. While the 1-kHz system significantly improves efficiency and size, it does so with the penalties of poorer regulation and increased cost for small (below 2 kW) power outputs. The designer must weigh the various performance factors to determine if the 1-kHz system is proper for the intended application.

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Table I—Power module ratings (Amperes).

2-V SCR regulators	*5-V SCR regulators*	*12-V SCR regulators*	*36-V SCR regulators*	*Converter inverters*
25	25	25	10	25
110	110	50	25	50
300	250			
300	400			

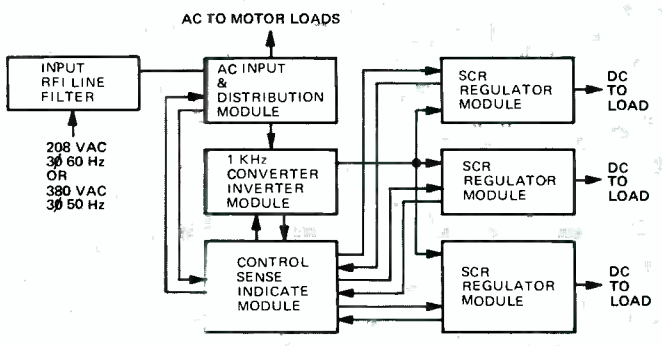


Fig. 1—1-kHz power supply block diagram.

A major feature of the 1-kHz system is the modular construction concept, which provides:

1) *Ease of manufacture.* Each module can be completely built and tested individually.
2) *Simplified system design.* Many different power systems can be created from the modules without a basic new design for each system.
3) *Better merchandising information.* Size and cost are immediately available for a supply as soon as power requirements are known.

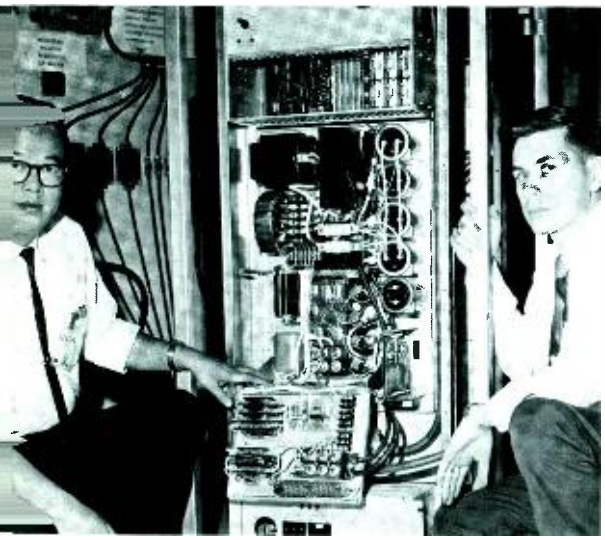
Power module output ratings are summarized in Table I.

System description

As shown in Fig. 1, the AC line input passes through an 80-dB RFI line filter to the AC input and distribution module. This module houses input protection breakers, contactors, and AC distribution terminal blocks. The AC is then fed to the converter-inverter module which converts the AC to 270 VDC and then back to 1-kHz, 270-V, peak, AC. The inverter output is then fed to phase-controlled SCR regulator modules where the AC is converted to regulated DC. The control-sense-indicate (CSI) module controls the turn-on/off of all modules, monitors all modules for failure conditions, indicates failure modes, and provides interface signals to the device being powered.

Converter-inverter module

A simplified schematic diagram of the converter-inverter is shown in Fig. 2.



S. Kuo (left) and K. Hoffman.

Sun L. Kuo
Power Systems Design
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received the BSEE from National Taiwan University in 1956 and the MSEE from Georgia Institute of Technology in 1963. He then joined W. L. Electric Company where he worked in solid state industrial control circuit design and test. He worked on designing photo-electric circuits and motor controller for Xerox Corporation in 1966. In October 1966, Mr. Kuo joined Research and Development Center, Westinghouse Electric Corporation to work on system analysis and design solid state high power and low frequency power conversion and switching. In the meantime, he attended the Graduate School of University of Pittsburgh as a part time student of mathematics. In September 1968, Mr. Kuo attended North Carolina State University on a Teaching Assistantship and completed course requirements for the PhD. Mr. Kuo joined RCA Computer Systems in Palm Beach Gardens in August 1969 and worked on NPL Power Systems design since then.

Karl Hoffman, Leader
Power Systems Design
Systems Development Division
Palm Beach Gardens, Fla.

received the BSEE from the University of Michigan in 1962. He joined RCA's Engineering Training Program after graduation and chose Computer Systems, Palm Beach Gardens, as his permanent assignment. He performed design and development work on germanium and silicon series regulated power supplies for small processors and peripherals until 1964 when he returned to the University of Michigan for graduate studies. Upon receiving his MSEE in 1965, he joined Bendix Reformed design work on photogrammetric equipment. formed design work on photogrametric equipment. He returned to RCA CSD Palm Beach Gardens in 1966 where he performed research and development work on new power regulating techniques. He became leader of the Power Systems Group in 1970 and is presently responsible for developing power systems for various processor and peripheral devices.

The circuitry can be divided into three sections: 50/60-Hz AC-to-DC converter, transistor inverter drive, and the SCR bridge inverter.

The basic components of the input section are the line rectifiers and an LC filter. In actual operation, a signal from the control-sense-indicate (CSI) module energizes K1 which applies AC to the input rectifiers CR1 through CR6. The rectified AC is then passed through R1 and filtered by L1, C1. (The purpose of R1 is to limit inrush current during the charging of C1. The resistor is shorted out by K2 after a sufficient delay period.)

When 3-phase, 208-VAC line-to-line is available, the input AC is full-wave bridge rectified (no neutral is used) and gives a nominal output of 270 VDC at the terminals of C1. When 3-phase 380-VAC line-to-line power (220-VAC line to neutral) is available, the input and neutral are 3-phase, half-wave connected, and a nominal output of 250 VDC is obtained. Because the rectified voltages for the two connections are so close in value, this power system is compatible with domestic and foreign input voltage requirements by simple jumper changes.

Another function of the converter section is to provide override capability for line voltage disturbances. This is accomplished by selecting a value for C1 that will hold the DC

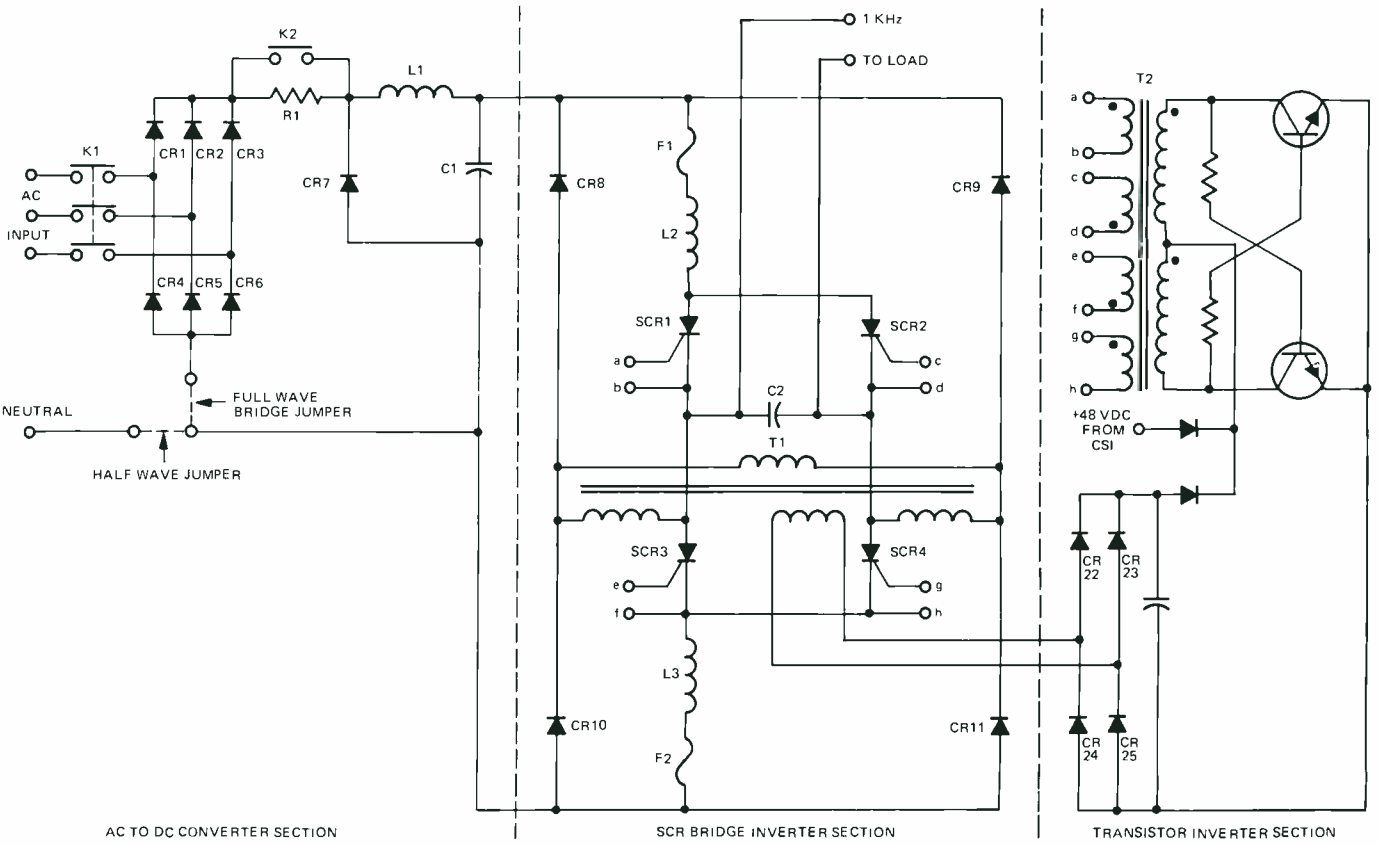

Fig. 2—Converter-inverter simplified schematic.

Gerald K. Schulze
Power Systems Design
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Palm Beach Gardens, Fla.
received the BA-Mathematics and BSEE from Texas A & M in 1961. He joined RCA in the same year where he designed the switched log network and other circuits for a four-bit log-differential PCM system for the BTL-Unicom Project. Transferring to the Tucson operation, he designed digital and analog circuits for various projects. One design responsibility was for a device for the silent transmission of low bit-rate digital information by FM audio sub carrier into a man-pack radio. In 1965, he transferred to the Astro Electronics Division where he designed the Vehicle Test Racks for powering and monitoring the Block IV Ranger spacecraft. He then worked on the design analysis of the VHF transmitters used on the Navy Navigational Satellite. In 1958, he transferred to Computer Systems where he presently is responsible for the design of the SCR Regulated Power Supplies for the new product line.

Ralph Notaro
Power Systems Design
Systems Development Division
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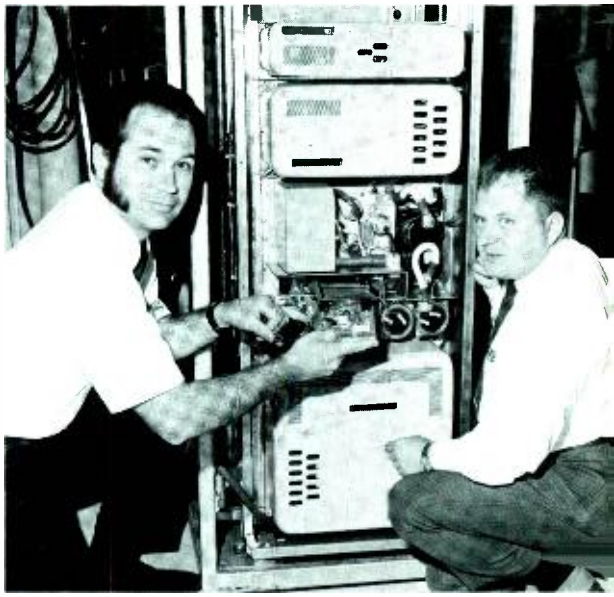
received the BSEE from Newark College of Engineering in 1962. In 1962 he joined the engineering staff of Industrial Control Products, Inc. where he designed a power supply system for the A.E.C. In 1964, he joined the Eclipse-Pioneer Division of the Bendix Corporation designing airborne power supplies. Between 1966 and 1969 he was a consultant to various aerospace electronics manufacturers including Lockheed Electronics, Bendix, and Kearfott Division of General Precision. He was also a consultant to RCA Harrison, where he designed special high voltage solid-state regulators used in life testing TWT's and magnetrons. He joined RCA Palm Beach Gardens in 1970 to design the Control-Sense-Indicate (CSI) Module for the 1-kHz converter/inverter power supply system.



G. K. Schulze (left) and R. Notaro.

output voltage above the minimum value needed for regulation during the desired hold-up period. Studies of line transients indicate that 8-millisecond line override is the optimum value. Longer periods of override are not beneficial unless at least 300 milliseconds override is reached. This amount of override is not practical using capacitor banks.

The transistor inverter section provides gate drive for the SCR bridge inverter and controls the operating frequency of the system. The inverter is a saturable core transistor inverter connected in a multivibrator configuration. This configuration was chosen because it provides fast risetimes at the secondary windings which are used to drive the bridge inverter SCR's.

At the beginning of turn-on, 48 VDC is fed to the transistor inverter from the CSI module to provide an operating voltage while the voltage at the converter section is building up. As the input voltage approaches nominal, rectifiers CR22 through CR25 will begin to conduct and will develop a voltage which overrides the 48 VDC from the CSI module. The overriding voltage is derived from transformer T1 and is therefore directly proportional to the DC input voltage. Thus, the operating frequency of the transistor inverter is directly proportional to the line voltage.

The final section is an SCR-bridge inverter with DC supplied from the converter section and gate control supplied by the transistor inverter. The secondary windings of T2 are phased so that SCR1 and SCR4 receive positive gate signals on one half cycle while SCR2 and SCR3 receive positive signals on the other half cycle.

On the first half cycle, SCR1 and SCR4 are turned on. The conduction path is from the +DC input thru L2 and SCR1 to the load and then back thru SCR2, L3 and to the −DC input. During the first half cycle, commutating capacitor C2 is at output voltage potential. At the beginning of the second half cycle, SCR2 and SCR3 are turned on, which forces C2 to reverse bias SCR1 and SCR4, thus turning them off. Commutating inductors L2 and L3 limit the rate at which C2 is charged to the opposite polarity and thus determine the turn-off time presented to the SCR's. The conduction path is then from +DC input through L2 and SCR2 to the load and back thru SCR3, L3 and to the −DC input. The cycle then repeats when SCR1 and SCR4 are turned on and SCR2 and SCR3 are turned off by the commutating capacitor and inductor. Diodes CR8 through CR11 are used to carry inductive load current and to provide a circulating path for excess current which builds up in the commutating inductors. Transformer T1 is used mainly to return the energy stored in the commutating inductors to the input filter capacitor and to the load.

SCR regulator modules

A schematic diagram of the SCR regulator module is shown in Fig. 3. The output of the converter-inverter is fed directly to the input terminals of the

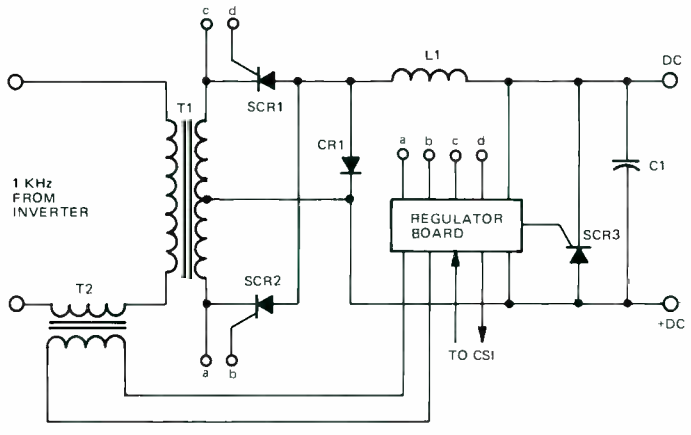


Fig. 3—SCR regulator schematic.

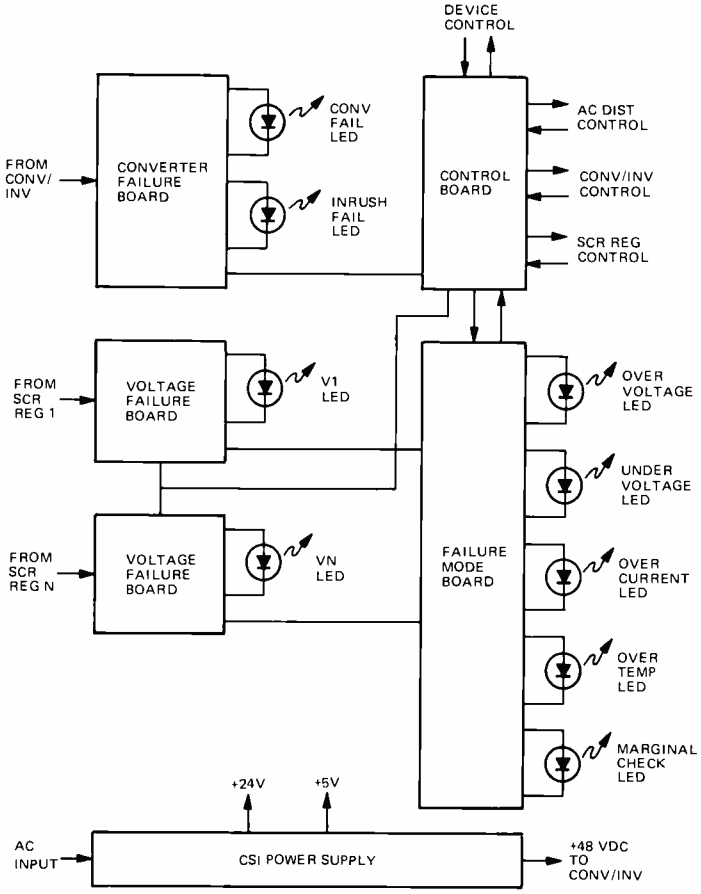


Fig. 4—Control-sense-indicate module.

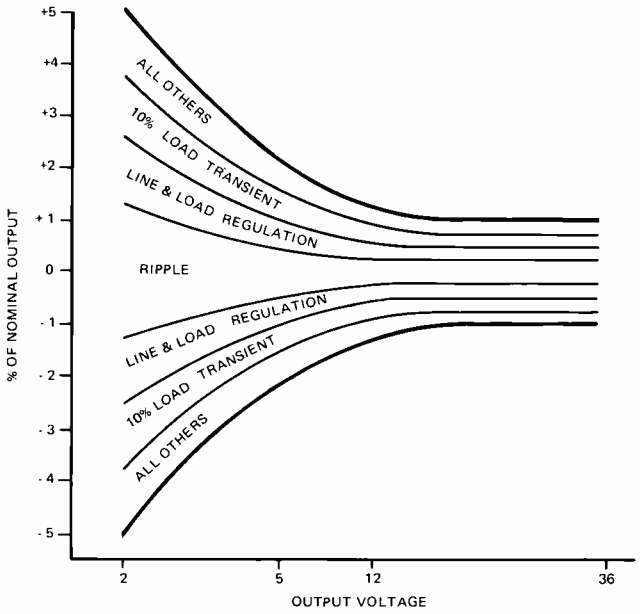


Fig. 5—SCR regulator DC output regulation.

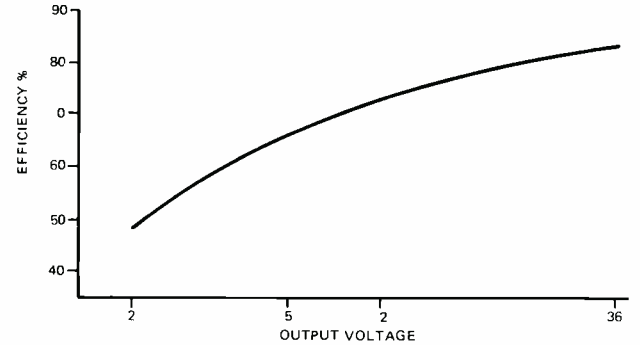


Fig. 6—Power conversion efficiency.

regulator module. The voltage is then stepped down by transformer T1 and applied to SCR1 and SCR2. The two SCR's are fired on alternate half cycles, and their output is then filtered by L1 and C1. Regulation is accomplished by varying the firing angle of the SCR's. The output of current sensing transformer T2 is rectified on the regulator board and is used to generate a turn-off signal during over-current conditions. SCR3 is used to short the output when a failure mode such as over-voltage has been detected. Diode CR1 provides a conduction path for the current in L1 when SCR1 and SCR2 are off.

The regulator circuitry utilizes a ramp and pedestal circuit. This type of circuit provides a good balance of firing angles for the two power SCR's. Without good balance, the output ripple voltage rises, and a large DC component of current is imposed on the power transformer.

As an additional feature, the regulator can be used for any voltage by changing a jumper on the plug-in connector. This is accomplished by dividing the output voltage to a common value with a resistor network and using the divided voltage as one input to the regulator differential error amplifier which compares it with a fixed reference voltage. By selecting the proper resistor in the network, the correct feedback voltage can be obtained for any output voltage from 0 to 100V.

Control-sense-indicate module

A block diagram of the CSI module is shown in Fig. 4. The control board interfaces with the device being powered and with all modules of the power system. It accepts turn-on/off signals from the device, sends logic signals to the device to indicate the operating condition of the supply, and also controls turn-on/off of all modules. The converter failure board monitors the output of the inverter and generates failure signals when the inverter is below minimum output. A light emitting diode (LED) on the board indicates an inverter failure. The voltage failure board monitors the SCR regulator over-temperature and over-current outputs and senses over- or under-voltage conditions at the regulator output. When a failure

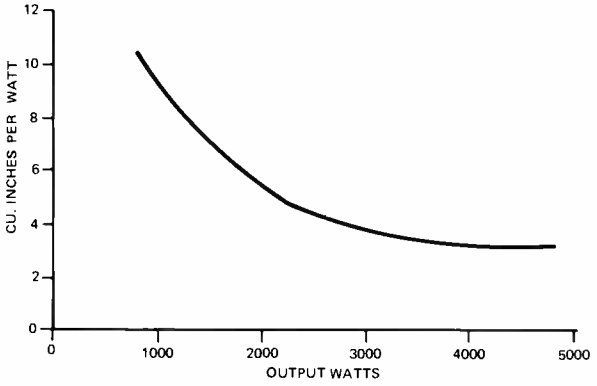


Fig. 7—Physical volume performance.

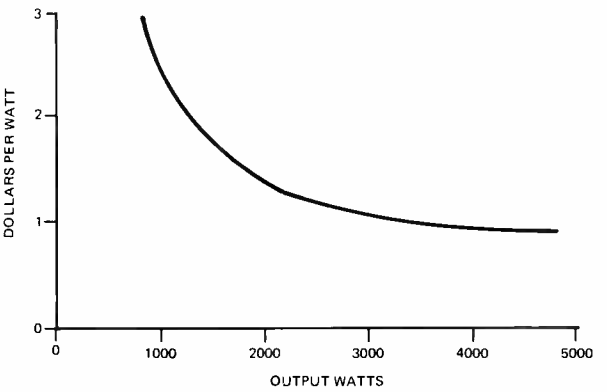


Fig. 8—System cost performance.

is sensed, a LED is turned on to indicate which module has failed. The failure signal is also sent to the failure mode board which has LED's to indicate the type of failure, i.e. over-voltage, under-voltage, over-current, or over-temperature.

System performance

In evaluating any power system, there are a number of performance factors which should be considered. Among the most important are output regulation characteristics, power conversion efficiency, volume, and cost. The 1-kHz power system has been specifically tailored for medium-scale commercial computers. Therefore, the performance curves (shown in Figs. 5 through 8) are a result of optimizing the design around the requirements for this application.

The regulation curves of the SCR regulator DC output are shown in Fig. 5. The heavy curves indicate the overall regulation band and the inner curves show the allocation for various regulation factors.

Fig. 6 shows the power conversion efficiency of the system. This includes the efficiency of the converter-inverter module and the SCR regulator module.

Fig. 7 shows the physical volume performance of the system vs. output watts. The volume includes one converter-inverter module, one CSI module, a number of regulator modules, and the associated cooling hardware.

Fig. 8 shows the cost per output watt for the system. Included in the total are costs of modules, cooling, assembly and test time.

Selecting the 1-kHz system

In deciding when to use the 1-kHz type of power supply, one must weigh the various performance factors. Once this is done, the decision to use, or not to use, the 1-kHz supply becomes fairly clear cut. The following decision-making process was applied to several devices in our new product line to determine whether a series-regulated supply or a 1-kHz supply should be used.

The performance factors of each type of supply are rated from 1 to 10, with 10 being excellent and 1 being poor. Next, a weight of 1 to 5 is assigned to the importance of each factor. Each device performance factor is then multiplied by its weight to yield a system performance factor. These factors are then added to produce a performance rating. The highest rating indicates which device to use.

The performance rating was first applied to a memory power system which required 2-kW of load power. In the rating process (Table II), it was recognized that regulation requirements for core memories require a good load transient response and a tight regulation band. Series regulators are unquestionably superior in this area. At 2-kW of output power, a series regulator is smaller and cheaper. Since the memory uses a higher voltage than a logic gate, the difference in efficiency between series and 1-kHz supply is not too great and is therefore relatively unimportant. From the summation of system performance factors, the resultant performance rating makes the choice of a series regulated system obvious.

The second power system to which the rating was applied was for a BPU which required 5 kW of load power. In this type of device, load transients are low and overall regulation is less stringent than in memories. The cost of the 1-kHz system is slightly lower than the series regulator. The efficiency of the 1-kHz supply is much better and is the most important factor because of implications in marketing and installation. The summation of system performance parameters, as shown in Table III, clearly shows the 1-kHz system to be the logical choice.

Table II—2-kW memory power system performance rating.

Performance factor	*Device performance*		*Weight factor*	*System performance*		
	Series	*1-kHz*		*Ideal*	*Series*	*1-kHz*
Regulation	10	7	5	50	50	35
Cost	7	4	4	40	28	16
Size	8	6	4	40	32	24
Efficiency	5	7	3	30	15	21
	Total performance rating			160	125	96

Table III—5-kW BPU power system performance rating.

Performance factor	*Device performance*		*Weight factor*	*System performance*		
	Series	*1-kHz*		*Ideal*	*Series*	*1-kHz*
Efficiency	3	7	5	50	15	35
Regulation	10	7	4	40	40	28
Size	5	8	4	40	20	32
Cost	6	7	3	30	18	21
	Total performance rating			160	93	116

Development of a voice-coil permanent-magnet force generator

R. L. Milamed

The voice-coil permanent-magnet force generator discussed here was developed as a magnetic suspension for accelerometers used in inertial guidance. It produces 48.6 grams of force at 100 mA voice-coil current, and is 1.03 inches in diameter by 0.70 inch long. It weighs 43.6 grams. This paper presents a method of analytical design and discusses materials, construction, and testing. This work is also of interest in the development of voice coil actuators for positioning read/write magnetic heads on the disc storage units of computer systems.

THE VOICE-COIL PERMANENT-MAGNET FORCE GENERATOR is similar in operation to the moving voice coil and stationary magnet structure of a dynamic loudspeaker (Fig. 1). In this design, a solid cylindrical permanent magnet is located inside the return path structure. By this means, the return path acts as a shield for leakage flux.

The voice coil moves within the annular airgap formed between the magnet polepiece and the return path. When current flows in the voice coil, the coil flux interacts with the permanent magnet flux to generate a force in line with the circular axis in accordance with Fleming's left hand rule. Force is reversed with current reversal.

Materials

Magnet

The permanent magnet is cast from "Columax," a variation of Alnico V, which is the trademark of the Thomas & Skinner Co., Indianapolis. This material was chosen because of its highest available maximum energy product, allowing a magnet of minimum volume. Maximum energy products for the nineteen magnets obtained ranged from 7.0 to 7.5×10^6 gauss-oersteds.

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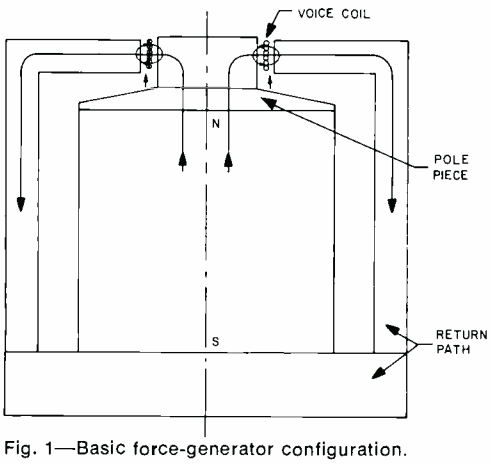

Fig. 1—Basic force-generator configuration.

Polepiece

The polepiece conducts flux from the magnet to the working airgap. It is machined from vanadium permendur, produced by the Arnold Engineering Co. Composition is 49% iron, 49% cobalt, 2% vanadium. This material was selected because of its very high saturation flux density (24,000 gauss) needed to prevent saturation at the airgap and help achieve minimum possible size. To obtain optimum magnetic properties, the polepieces were annealed after all machining was completed. They were annealed in dry hydrogen for two hours at 1400°F and then furnace cooled in dry hydrogen at the rate of 200 to 300°F/hour down to 400°F. The parts were then cooled to room temperature in still air. Some dimensions on the polepiece are held to ±0.0002 inch, and cooling was therefore carefully controlled to prevent distortion. All close-tolerance dimensions were rechecked after annealing. No dimensions had gone out of tolerance.

Return path

The return path consists of the cup which forms the outer diameter of the working airgap and the base to which the magnet is soldered. The material is Armco magnetic ingot iron, chosen for its low reluctance at design flux densities. With this material, annealing after finish machining is needed to obtain optimum magnetic properties. The heat treatment procedure used on all return-path parts was to anneal at 1500°F for 3½ hours in dry hydrogen and then furnace cool in dry hydrogen at the rate of 200°F/hour down to 400°F. Cooling from 400°F to room temperature took place in still air. As with the polepieces, cooling was carefully controlled to prevent distortion. Cooling rate was slower because the return-path parts are more fragile. No dimensions went out of tolerance during heat treatment. The tightest tolerance was a ±0.0001 internal diameter which remained within tolerance on all fourteen parts annealed.

Coil

The voice coil is wound with #42 (.0025-inch bare diameter) copper magnet wire having isonel 173 insulation. Isonel, developed by the Schenectady Varnish Company, was chosen as insulation because it possessed the best combination of temperature rating, minimum thickness, and facility for impregnation. Continuous temperature rating is 155°C.

Method of analytical design

The fundamental approach was to combine analytically a voice coil and permanent magnet structure to obtain a force generator having required output in minimum size. As noted previously, Fig. 1 depicts the general voice-coil permanent-magnet structural configuration for which this design work was done.

Beginning with the basic equation for the force acting on a current-carrying conductor in a magnetic field, $F = BIl/10$ where F is the force generated (dynes); B is the flux density in gauss (lines/cm^2); I is the current (amperes); and l is the length of conductor (cm).

To express force in terms of physical dimensions of the moving and stationary components, the voice coil is a good starting point, since its radial width will determine the airgap of the magnetic structure.

The temperature rise of the voice coil is vital to the derivation, since the upper limit of voice-coil current, I,

results from the maximum temperature which the insulation of the coil wire will take continuously.

H. C. Roters[1] derives the temperature rise of a cylindrical coil with thermally insulated coil end surfaces to be:

$$\theta_f = \frac{\rho}{2kft}\left(\frac{NI}{h}\right)^2 = \frac{I^2R}{2khP_M}$$

He also notes that $R = 4\rho P_M N/\pi d^2$, where θ_f is the final temperature rise (°C) between coil and still air; ρ is the resistivity of wire (ohm-inches); N is the total number of turns on coil; I is the coil current (amperes); R is the coil resistance (ohms); k is the heat dissipation coefficient (watts/inch²/°C temperature difference); P_M is the perimeter of mean turn (inches); D_M is the mean diameter of coil (inches); d is the bare wire diameter (inch); f is the space factor of the coil winding; t is the radial width of coil (inches); and h is the height of the coil (inches).

If the entire coil area, including both end surfaces of radial width t, is considered to be dissipating heat, the above equations for θ_f would be:

$$\theta_f = \frac{\rho (NI)^2}{2kfth(h+t)} \quad (1)$$

$$\theta_f = \frac{I^2R}{2kP_M(h+t)} \quad (2)$$

The next step is to obtain an expression for current times developed coil wire length in terms of the dimensions of the voice coil. This expression can then be set equal to a constant which is determined for any specific value of required force output and airgap flux density using the relationship $F = BIl/10$. Then $Il = 10F/B$. Note that only in this relationship is l in cm., whereas in the following equations L is in inches.

Substituting $R = 4\rho P_M N/\pi d^2$ into Eq. 2,

$$\theta_f = \frac{4I^2\rho P_M N}{2\pi d^2 k P_M (h+t)} \quad (3)$$

Substituting $L = P_M N$ (where L is the total developed length of wire in the coil in inches) into Eq. 3,

$$\theta_f = \frac{(IL)2\rho I}{\pi d^2 k P_M (h+t)} \quad (4)$$

From Eq. 4,

$$I = \frac{\theta_f \pi d^2 k P_M (h+t)}{2\rho (IL)} \quad (5)$$

Determining an independent expression for L based on the total volume of coil conductor,

$$\tfrac{1}{4}\pi d^2 L = htfP_M \quad (6)$$

and

$$L = 4htfP_M/\pi d^2 \quad (7)$$

Multiplying Eqs. 5 and 7,

$$IL = \frac{\theta_f \pi d^2 k P_M (h+t)}{2\rho (IL)}\left[\frac{4htfP_M}{\pi d^2}\right] \quad (8)$$

Simplifying Eq. 8 and substituting $\pi D_M = P_M$,

$$(IL)^2 = 2\theta_f k \pi^2 D_M^2 (h+t) htf/\rho \quad (9)$$

At this point it would be helpful to set an optimum proportion between coil height, h, and radial thickness, t. On one hand, t should be small and h large to obtain minimum airgap and maximum heat dissipation. Also, decreasing the number of layers of wire makes it easier to obtain a uniformly wound coil. On the other hand, the more nearly $t = h$ the greater will be the uniformity of the flux field through which the coil travels (since the height of the coil is less). In the absence of test data on which to evaluate the relative importance of these points, a ratio of $t/h = 0.25$ seemed reasonable. Substituting $t = 0.25h$ into Eq. 9 and collecting constants gives

$$(IL)^2 = 6.15\theta_f k D_M^2 h^3 f/\rho \quad (10)$$

The design conditions for the force generator were taken as follows:

1) Force output F = 32 grams = 31,400 dynes.
2) Coil temperature rise $\theta_f = 70$°C. This was based on a maximum hot spot coil temperature of 155°C, which is the maximum continuous operating temperature for isonel insulation. Assuming the maximum average temperature of the coil is 15°C less than the maximum hot spot temperature and taking a maximum instrument ambient temperature of 70°C gives θ_f = 70°C. At 140°C average coil temperature, the resistivity ρ for copper = 0.998×10^{-6} ohm-inch.

Tests to determine heat dissipation coefficient, k, for a coil of the order of size of the voice coil to be developed resulted in a value of 0.0208 watts/inch²/°C temperature difference.

Test data on k for various coils is given in Table I.

Substituting for θ_f, k, and ρ in Eq. 10:

$$(IL)^2 = 8.97 \times 10^6 D_M^2 h^3 f \quad (11)$$

When power, coil dimensions, and airgap flux density are constant, the output of the force generator is independent of the wire diameter d used to wind the voice coil. This can be shown by substituting expressions for I and length of wire l into the equation $F = BIl/10$, as follows: K, K_1, K_2, K_3, K_4 are constants. From $P = I^2R$, $I = P^{1/2}/R^{1/2}$. Then $F = BP^{1/2}l/R^{1/2}$; $R = Kl/d^2$, giving $F = BP^{1/2}ld/K^{1/2}l^{1/2} = K_1 l^{1/2} d$. For a coil of constant dimensions, $l = K_2/d^2$ or $d = K_3/l^{1/2}$.

Substituting this expression for d gives $F = K_4$, showing that force is independent of wire size under the assumed constant conditions.

The criteria which determine wire size are various practical considerations which require a prior knowledge of the other coil parameters. These are discussed in a later section. At this point in the development, the wire size must be estimated; 0.0020-inch diameter was chosen. At this wire diameter, the winding space factor f is 0.55, extrapolated from H. C. Roters.[2]

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received the BSME from Tufts University in 1946, and the MBA from Northeastern University in 1956. From 1946 to 1950 Mr. Milamed was an analytical engineer on fuel system development, axial flow compressor development, and engine performance analysis for United Aircraft Corp. During 1950 to 1959 he worked on development, design for production, and production engineering of aircraft instruments for the General Electric Co. Served as instructor for a G.E. course in mechanical engineering. In the period from 1959 to 1963, he was at RCA Aerospace Systems Division working on development of airborne inertial instrumentation. He joined the MIT Instrumentation Laboratory in 1963 and until 1969, was a staff engineer on the development of the stable platform for guidance of the Apollo vehicle, and other advanced electromechanical instrumentation projects. Mr. Milamed returned to RCA in 1969 in Computer Systems Marlboro, working on the 70/594 disc storage unit. He is presently working in Tape Equipment Engineering. He is a registered P.E. in Mass. and a member of Tau Beta Pi.

Design calculations

The two main variables of the force-generator design are airgap flux density and voice-coil mean diameter. Calculations of force-generator size over a range of these main variables were made to determine the minimum overall size.

Voice coil

The voice-coil mean-diameter range was taken as 0.150 to .500 inch. The airgap flux-density range in these calculations went up to 22,000 gauss. Based on the saturation flux density of 23,000 to 24,500 gauss for vanadium permendur polepiece material, the 22,000 figure was assumed to be the maximum achievable. Calculations were made with airgap flux densities as low as 500 gauss to determine the possibility of obtaining a smaller force generator by increasing voice-coil current. However, as airgap flux density is decreased, the linearity error of the force generator increases due to more leakage into the airgap of flux generated by the increased voice-coil current.

To show the method of calculation, let us take the case of airgap flux density B_g equal to 15,000 gauss and mean coil diameter of 0.500 inch. Starting with derived Eq. 11:

$$(IL)^2 = 8.97 \times 10^6 D_M^2 h^3 f$$

For $B = 15{,}000$ gauss and $F = 31{,}400$ dynes, $IL = 10(31{,}400)/15{,}000 = 20.9$ amp-cm or $IL = 8.24$ amp-inches.

Then $(8.24)^2 = 8.97 \times 10^6 \ (0.500)^2 \ h^3 \ (0.55)$; and $h^3 = 0.0000550$ or $h = 0.0380$ inch (ht. of coil) and $t = 0.0380/4 = 0.0095$ inch (radial width).

The length of wire in this coil is obtained from Eq. 7:

$$L = \frac{4htfP_M}{\pi d^2} =$$

$$\frac{(4)\ (0.0380)\ (0.0095)\ (0.55)\ (\pi)\ (0.500)}{\pi\ (0.0020)^2}$$

$$= 99.3 \text{ inches}$$

and, from this, the coil resistance at 140°C average temperature is 31.4 ohms. Current $= IL/L = 8.24/99.3 = 0.0830$ amp and power $= I^2R = (0.0830)^2\ (31.4) = 0.216$ watt.

Stationary magnetic circuit

The airgap in which the voice coil operates was taken as 0.014 inch larger than the radial width, t, of the coil. Since the length of the magnet is almost in direct proportion to the length of airgap, the airgap must be kept to the minimum possible. Airgap then equals $0.0095 + 0.0140 = 0.0235$ inch.

The magnetomotive force (MMF) needed for the magnet is equal to the MMF drop in the airgap plus the MMF drop through the polepiece and return path. For this particular condition, airgap flux density $B_g = 15{,}000$ gauss. Magnetizing force in the airgap is 15,000 oersteds, since the permeability of air is one. One oersted = 2.02 ampere-turns/inch. Then the MMF drop across airgap = (15,000) (2.02) (0.0235) = 712 amp.-turns.

The MMF drop through the polepiece and return path is calculated similarly, obtaining the magnetizing force from the *B-H* magnetization curves for the particular materials. This MMF was 21 amp.-turns.

Total mmf required of the magnet = 712 + 21 = 733 amp.-turns.

The height of the magnetic material about the voice coil was set so that at the extremes of assumed axial movement of the voice coils (±0.005 inch), the ends of the voice coils would still be 0.010 inch from the end of the stationary magnetic material. This was done to try to assure that the coil would always be subject to a uniform flux field, yet add a minimum to the force generator size. This size increase comes not only from the initial additional height of return path and polepiece, but the resulting decrease in B_g causes a compensating increase in magnet size.

The resulting mean area of airgap for this condition being calculated = (0.0380 + 0.010 + 0.020) (π) (0.500) (6.45) = .690 cm².

Based on the experience of Mr. John Bleazey of the RCA Laboratories in

Table I—Comparison of heat dissipation coefficient k at 70° C temperature rise for various test conditions.

	Coil #1 D_M = 0.150″ d = 0.0025″ n = 140 h = 0.125″ t = 0.016″	*Coil #2* D_M = 0.500 d = 0.0040″ n = 214 h = 0.120″ t = 0.028″	*Coil #3* D_M = 0.500 d = 0.0040″ n = 232 h = 0.125″ t = 0.041″	*Coil #4* D_M = 0.346″ d = 0.0025″ n = 345 h = 0.120″ t = 0.028″	*Coil #5* D_M = 0.434″ d = 0.0020″ n = 97 h = 0.056″ t = 0.014″
Air, room temp.	0.0173	0.0155	0.0131	0.0252	0.0555
Air, +70° C	0.0224	0.0204	0.0196	0.0336	0.0690
Silicone oil, 5 centistoke, +70° C	0.274	0.256	0.226		
Silicone oil, 50 centistoke +70° C	0.205	0.198	0.185		

Notes:

All wire insulation is single isonel, impregnated with isonel 31 varnish. All coils are self supported (no bobbin). Coils #1, #2 and #3 contact no solid material. Coils #4 and #5 are cemented on one side to a 3/32″ thick #2024 aluminum disc, of 11/16″ and 15/16″ diameter respectively. Coil #3 is aluminum others are copper.

Convection currents are visible in the 5-centistoke oil at the higher wattage inputs, but not in the 50-centistoke oil. D_M = mean coil dia.; d = bare wire dia.; n = no. of turns; h = coil height; t = coil radial thickness.

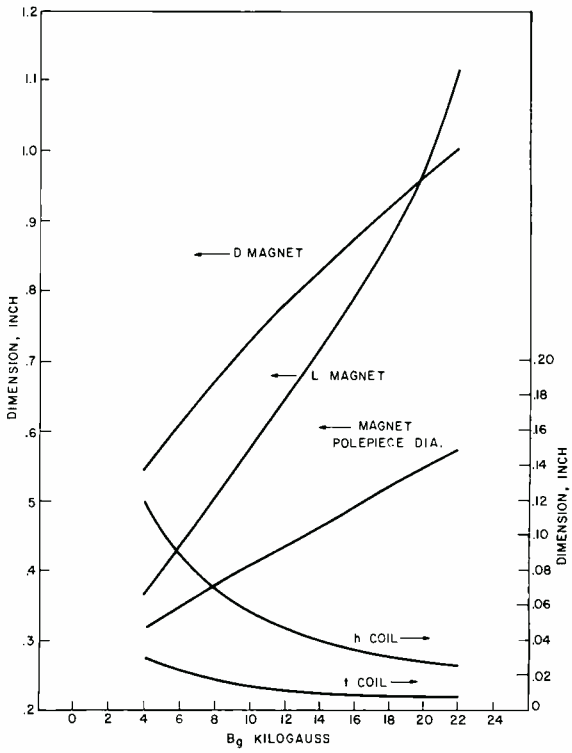

Fig. 2—Force-generator characteristics vs. B_g at 18,000 gauss B *magnet polepiece diameter.*

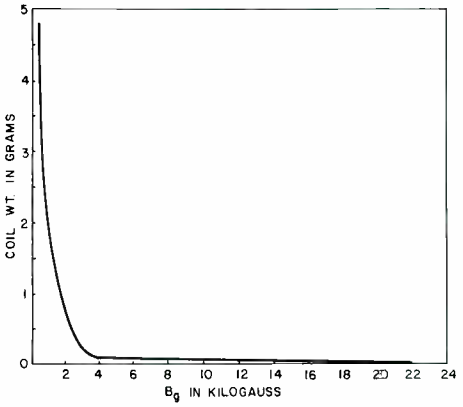

Fig. 3—Weight of copper voice coil vs. B_g with $B_{magnet\ polepiece\ dia.}$ = 18,000 gauss

Princeton, a leakage factor of four was used in calculating magnet area. That is, one fourth of the lines of flux produced by the magnet could be expected to appear as useful flux in the working airgap. The rest would be lost as leakage.

Then, the total flux in the magnet = (15,000) (0.690) (4) = 41,400 lines.

For minimum size, the magnet should be designed to operate at its maximum energy product. For "Columax," this point occurs at $B = 11{,}300$ gauss and $H = 660$ oersteds = 1332 amp.turns/inch. Optimum area of magnet = 41,400/11,300 = 3.66 cm², giving a diameter = 0.851 inch.

In calculating the length of the magnet a "reluctance factor" of 1.35 was used. This factor is intended to provide additional MMF to overcome MMF drops at joints, and also to compensate for the fact that the lines of flux in the airgap are curved, in effect making the airgap longer. Then, optimum length of magnet = 1.35 (733) / 1332 = 0.743 inch.

In this manner, the magnet and voice-coil calculations are made for each design condition. The data given in Table II summarize force-generator characteristics calculated versus airgap flux density B_g at various mean coil diameters.

With 18,000 gauss flux density in the cylindrical periphery of the vanadium permendur polepiece, the force-generator characteristic values are as shown in Fig. 2. 18,000 gauss was chosen as a maximum design value which would avoid saturation of the polepiece under all tolerance conditions.

A particularly interesting relationship —voice coil weight vs. B_g—is plotted in Fig. 3. This curve shows the gradual increase in coil size as B_g decreases to 4,000 gauss, and the very marked increase in coil size below 4,000 gauss, as the coil flux interacts with relatively sparse permanent magnet flux.

Coil heat dissipation coefficient k test data

As noted previously,[1] k is expressed in watts dissipated/inch² of coil area/°C temperature difference. Heat-dissipation data could only be found in the literature for coils very much larger than the order of size needed for this voice coil. Accordingly, values of k were determined in the laboratory for various coil sizes, aluminum and copper wire, room temperature and +70°C ambients, and in air and two viscosities of silicone oil. Average temperature rise was measured by coil resistance change. In Table I heat dissipation coefficients for the various conditions tested are compared for a 70°C temperature rise.

Flux leakage from voice coil

The proportionality between force output and voice coil current input requires that the airgap flux density B_g be constant. It is known that some of the flux generated by the voice coil will leak into the stationary magnetic structure and cause B_g to vary, depending on the magnitude and direction of the voice-coil current.

Error due to coil flux leakage may be compensated out by the use of two

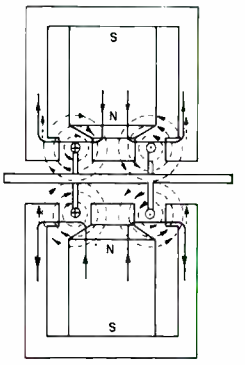

Fig. 4—Compensation for variation of B_g due to coil flux leakage by use of two force-generators with adjacent coils.

force generators with adjacent coils. If the units are arranged as shown in Fig. 4, automatic compensation takes place because the voice coil flux (shown by dashed lines) acts in the same direction for each unit, whereas the permanent magnet flux (solid lines) acts in opposite directions. Therefore, depending on current direction, the voice-coil flux leaking into the permanent magnet structure will increase airgap flux density for one force generator and decrease it for the other by an equal amount, maintaining constant the sum of airgap flux densities.

Practical considerations for voice coil

It has been shown that for constant power, coil dimensions, and B_g, force output is independent of wire diameter. The practical considerations which determine wire diameter are as follows:

Table II—Summary of force-generator characteristics calculated vs. airgap flux density B_g at various mean coil diameters.

B_g (gauss)	D_M Coil (inches)	h coil (inches)	t coil (inches)	I^2R coil (Watts)	Magnet length (inches)	Magnet dia. (inches)	Total magnet flux (kilolines)	B polepiece Dia. (kilogauss)
22,000	0.150	0.0656	0.0164	0.111	1.587	0.669	25.5	175
	0.500	0.0295	0.0074	0.168	1.140	0.963	53.0	23.0
	0.600	0.0263	0.0066	0.175	1.101	1.024	60.2	17.8
15,000	0.150	0.0849	0.0212	0.145	1.103	0.605	20.9	158
	0.200	0.0700	0.0175	0.159	0.989	0.651	24.3	85.2
	0.300	0.0543	0.0136	0.177	0.867	0.725	30.8	41.0
	0.400	0.0448	0.0112	0.196	0.792	0.798	36.4	25.6
	0.500	0.0380	0.0095	0.215	0.743	0.851	41.4	18.0
8,000	0.150	0.129	0.0322	0.220	0.767	0.520	15.45	141
	0.200	0.108	0.0271	0.234	0.679	0.555	17.60	68.9
	0.300	0.0828	0.0207	0.269	0.564	0.619	21.9	30.8
	0.400	0.0684	0.0171	0.296	0.516	0.669	25.5	18.5
	0.500	0.0588	0.0147	0.319	0.480	0.709	28.7	12.7
4,000	0.150	0.205	0.0513	0.349	0.542	0.447	11.41	156
	0.200	0.1722	0.0431	0.372	0.471	0.479	13.10	63.4
	0.300	0.1313	0.0328	0.431	0.387	0.525	15.70	24.2
	0.400	0.1082	0.0271	0.471	0.341	0.559	17.88	13.7
	0.500	0.0934	0.0234	0.505	0.313	0.588	20.0	9.26
2,000	0.200	0.268	0.0670	0.815	0.339	0.411	9.66	67.3
	0.300	0.205	0.0512	1.40	0.275	0.448	11.42	20.4
	0.400	0.169	0.0422	2.05	0.236	0.475	12.90	10.78
1,000	0.200	0.426	0.1066	1.29	0.255	0.359	7.38	
	0.300	0.325	0.0812	2.23	0.203	0.388	8.60	
	0.313	0.317	0.0791		0.201	0.391		
	0.320	0.312	0.0780	2.41	0.199	0.394	8.89	
500	0.311	0.504	0.1260	3.69	0.151	0.343		
	0.333	0.482	0.1204	5.23	0.145	0.348		
	0.350	0.465	0.1161	6.43	0.141	0.351		

Fig. 5—Voice coils built for heat dissipation, search coil, and force output tests.

1) An even number of layers is necessary in order to have both leads come out on the same side of the coil. With an odd number of layers, the working airgap must be increased just to allow clearance for one strand drawn across the coil.
2) Wire size should be as large as possible to:
   a) Increase winding space factor which increases with wire diameter.
   b) Lessen breakage and winding time.
   c) Hold the outside diameter of the coil to close tolerances more readily (fewer layers).
3) The current limitation of the external circuit.

Fig. 5 shows various voice coils built for heat-dissipation, search-coil, and force-output tests.

Force generators built

Two force generators were built for initial testing: one designed for B_g= 4,000 gauss and the other for B_g= 10,000 gauss. Below B_g=4,000, the voice-coil weight increases sharply, and at B_g=10,000, a fair compromise between overall size and estimated coil flux leakage error appeared to take place. Cross sections through both these assemblies and alternate return paths are shown in Fig. 6.

The purpose of testing with both types of return paths was to determine the increase in force output with increase in clearance between magnet and return path.

Fabrication development techniques

Voice coils

The bobbin-less voice coils which were the first to be wound and tested were made in the following manner. The coils were hand wound on a teflon arbor to prevent sticking of the impregnating varnish. Some slight sticking still took place at the coil ID but was overcome with the use of a teflon sleeve at one coil face to push the coil off the arbor.

The Isonel 173 coil wire insulation was impregnated with Isonel 31 varnish. The varnish was thinned in the proportion one part varnish to three parts xylol by volume, and was flowed on by brush between layers, and at the coil OD. After winding, the coil was baked on the arbor for 1½ hours at 310°F.

Voice coils wound on bobbins were made as follows. The bobbin diameter was insulated with 0.001-inch mylar adhesive-backed tape. Inside faces of the bobbin were insulated with mylar rings punched from 0.002-inch-thick adhesive tape. The windings were impregnated and cured in the same manner as for the bobbin-less coils.

Permanent magnet assemblies

To maintain optimum magnetic properties, the vanadium permendur polepieces and ingot iron return paths were annealed as described earlier after finish machining.

Before soldering the magnet assembly together, the oxide was polished off the vanadium permendur polepiece at the outside diameter and face which was to be soldered. Parts were degreased and individual heights measured. The return path base, magnet, and polepiece were then stacked together and overall height measured to be sure of seating. In this way, airgaps between parts were avoided.

The assembly was clamped with minimum pressure between two aluminum plates of ⅛-inch thickness. The only source of heat was a hot plate, with temperature about 500°F. Stainless steel flux was used with 60%-tin, 40%-lead solder. A ring of 0.040-inch-diameter solder was set at the soldering junction; 0.030-inch-diameter solder had been tried and found to supply an insufficient fillet. The hot plate was brought up to temperature before the work was applied to prevent the flux from boiling off too soon. The ingot iron base was soldered to the magnet first so that when the polepiece was soldered in place next, the base flange would act as a cooling fin and help prevent melting of the first joint. This procedure gave good results in joining materials which are inherently difficult to solder.

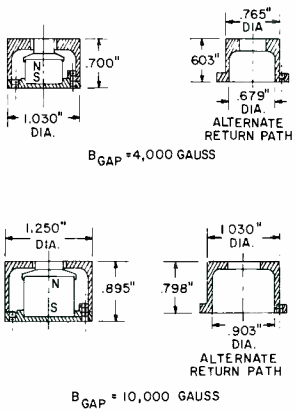

Fig. 6—Magnetic assembly stationary structures, cross-sectional views.

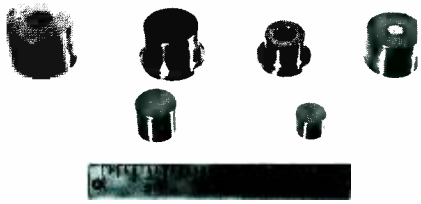

Fig. 7—Assembled 4000 (smaller components) and 10,000 gauss force generators, their magnets, and alternate return paths.

Fig. 7 shows the assembled 4000- and 10,000-gauss magnet assemblies together with their magnets and alternate return paths.

Magnetizing and stabilizing

All magnet assemblies were magnetized using the Varian V4007 magnetizer and V2200A power supply. Straight cylindrical polepieces of 6-inch diameter were used on the magnetizer. Gaps between polepieces were ¾-inch for the 4,000-gauss suspension and 1-inch for the 10,000-gauss suspension. The measured flux density between the magnetizer polepieces was 14,000 gauss in the 1-inch gap.

After magnetizing, the magnet assemblies are stabilized by a procedure based on information from the Indiana Steel Co. and a paper by R. J. Studders.[3] This procedure has the following sequence.

1) The airgap is shorted out three times by sliding a clean steel plate over the top surface of each assembly.
2) The assemblies are temperature cycyed six times between room temperature and 125°C.
3) The magnet is knocked down by a 60-Hz field until the total knockdown is 5%.

Temperature compensation

The temperature coefficient of the Columax magnets used in these force generators is about −0.025%/°C.

After the temperature cycling is performed, this decrease in flux with increase in temperature becomes reversible.

A well known way of achieving temperature compensation is with the use of a magnetic shunt, similar in principle to the means for compensating watt-hour meters.[4] In the force generator application, a cylindrical ring of compensating material could be placed around the magnet OD near the pole-piece. This gives a smaller airgap between magnet and return path at this point, shunting more flux away from the working airgap than would otherwise be lost by leakage. Due to the particular rate of change of permeability of the compensating material, as temperature increases and the magnet flux output is lower, less flux is shunted away from the working airgap. When temperature decreases, and the magnet flux output is higher, more flux is shunted away from the working airgap. In this way, the flux in the working airgap is kept constant as temperature varies.

Force generator tests

Search coil

The first tests run on both the 4,000- and 10,000-gauss force generators were to verify design airgap flux densities using search coils. The same voice coils used later for force-output tests were used here as search coils. The coils were attached to holders, and their leads connected to an oscilloscope. In testing, the search coil was placed in the airgap and then quickly removed. The trace of the voltage generated was seen on the oscilloscope and photographed. From these traces, e (the average induced EMF) and t (the flux cutting time) were determined. Then from $e = N\ (\Delta\phi/\Delta t)\ 10^{-8}$, the number of lines of flux in the airgap (ϕ) was calculated. Dividing ϕ by the mean area of the airgap gave the flux density for which we were checking.

For the force generator with external flange return path which was designed for 4000-gauss airgap flux density, the average of nine search-coil test readings gave 4750 gauss. For the force generator with external flange return path which was designed for 10,000-gauss airgap flux density, the average of eleven search coil test readings gave 11,800 gauss.

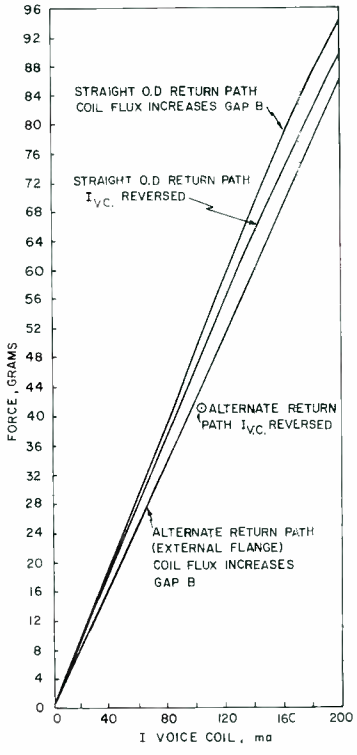

Fig. 9—Force output vs. voice-coil current for B_g=4000 gauss force-generator voice coil has 345 turns of #42 wire.

Force output

In testing the 4000- and 10,000-gauss units for force output versus voice-coil current, the voice coil was attached to the horizontal arm of an analytical balance, and force output was measured by this means. Fig. 8 shows the test setup. In Figs. 9 and 10, force-output data versus current are plotted for both force generators. The different slope caused by reversing the current is due to leakage of voice coil flux into the permanent magnet structure. In one current direction, the voice-coil flux increases the permanent magnet flux, and in the other current direction decreases it.

Mean airgap flux densities for the two force generators with external flange return paths were determined using the equation $F = BI\ l/10$. At 20 mA current, for the force generator designed for 4000-gauss, B was found to be 4240 gauss. For the 10,000-gauss design, B achieved was 9080 gauss. Due to the nature of this test and measuring equipment used, it was a more accurate means of determining flux densities than with search coils.

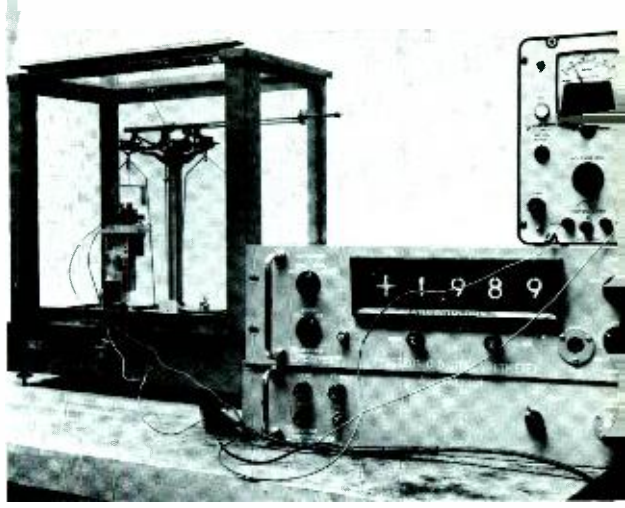

Fig. 8—Measurement of force generator output using analytical balance.

Return-path comparison

The force output of the 4000-gauss assembly was checked with both types of return paths. The radial clearance between magnet and return path was 0.068 inch for the external flange return path and 0.201 inch for the straight OD return path. With the increased radial clearance force output increased 18%.

Acknowledgment

I am indebted for their help to Messrs. J. C. Crowley, S. Waldstein, S. A. Bryngelsson, H. E. Fitch of Aerospace Systems Division, Burlington, Massachusetts, and to Dr. H. F. Olson, J. Bleazey, and J. Preston of RCA Laboratories, Princeton, New Jersey.

References

1. Roters, H. C., *Electromagnetic Devices* (John Wiley, New York) p. 186.
2. *ibid.* p. 172.
3. Studders, R. J., "Permanent Magnet Stability" *Product Engineering* (Nov. 1948).
4. Kinnard, I. F. and Faus, H. T., "Temperature Errors in Induction Watthour Meters," *Trans. AIEE* (May 1925).

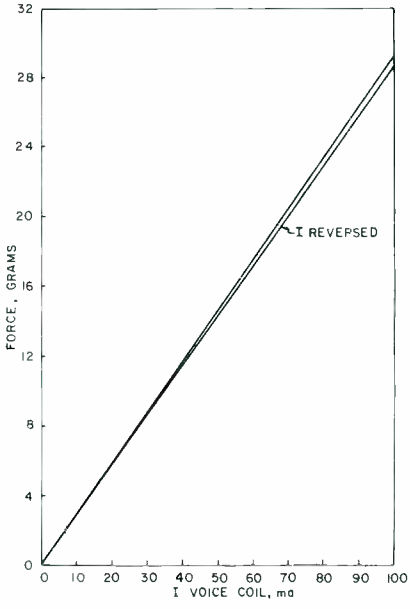

Fig. 10—Force output vs. voice-coil current for B_g=10,000 gauss force generator voice coil has 97 turns of #44 wire.

Model A—an inexpensive data coupler

Dr. M. J. Schindler

The Model A data coupler, designed as a companion piece to the Model T graphic display, facilitates the transmission of engineering test data to the RCA Basic Time Sharing System (BTSS). According to a program selected with the command switch of the Model A, the computer calculates derived quantities to be displayed by the Model T. Constructed from commercially available circuit cards, the materials for a Model A cost under $1000. The Model A, Model T, and a control panel are combined into a unit dubbed MATE (Manual/Automatic Test Equipment) which is capable of interfacing a wide range of engineering test equipment (from diode tester to network analyzer) with the BTSS computer, and of graphically displaying derived quantities. As the name indicates, MATE can also operate in a semi-automatic manual mode when the computer is not available.

THE MODEL A data coupler was designed to satisfy an ever-increasing need of the engineering community to feed test data directly into a digital computer. At present, test data are usually displayed either on meters or oscilloscopes. If additional manipulation of these data is needed, they must be recorded and either fed into a computer by hand or subjected to hand calculation. Obviously, this process not only constitutes a waste of costly manpower, but may also introduce errors and inaccuracies. Furthermore, and perhaps most significantly, the effort involved encourages the use of raw data rather than corrected or derived quantities.

These problems are particularly severe in the field of microwave engineering, because practically only power and voltage can be measured directly. All other parameters, such as impedance or phase, must be calculated. Furthermore, microwave measurements are inherently inaccurate. Errors of 10% or more are the rule, and calibration procedures are an essential part of every microwave measurement. Incorporation of calibration data is, however, frequently cumbersome if not altogether impractical. For these reasons, the advent of computer-coupled test equipment (such as the Hewlett-Packard Network Analyzer) has been hailed as the beginning of a new era in microwave engineering.

Unfortunately, the cost of progress is, in this instance, unusually high. Computerization of microwave test gear adds between $10,000 and $100,000 to its cost and frequently provides only very limited computational capabilities. Utilization of available time-sharing facilities thus becomes an economic necessity where a substantial number of test stations can benefit from computerization. Because this criteria fits a vast number of applications in many fields of engineering, one might logically expect data interfaces to be easily available. As a result of the wide range of specific requirements of the test equipment, as well as the computer systems, this development was, however, very slow and, at the beginning of the Model A program, no suitable equipment was found on the market. Although several firms now endeavor to fill the need for a data coupler along the lines described above, they are still far from a simple "plug-in and run" situation. The required modifications and debugging efforts on commercially available components, and the high cost of the more versatile units, will in many cases still favor the do-it-yourself approach. Although commercially available circuit cards were used in the construction of the Model A prototype, it may be advantageous to design and manufacture these basic building blocks in-house.

As the designation Model A suggests, the equipment was conceived as a companion piece to the Model T developed by J. Miller and C. Wine at the RCA David Sarnoff Research Center.[1] The Model T utilizes a storage oscilloscope as the display device to plot graphs, or present other graphic outputs obtained from the RCA Basic Time Sharing System. With some minor modifications, the

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received the MSEE in 1951, and the Doctor of Technical Sciences in Solid State Physics in 1953, both from the Technische Hochschule in Vienna, Austria. He joined the RCA Microwave Tube Operations in 1958, and has since worked on a number of basic technical problems related to the design of traveling-wave tubes, magnetrons, crossed-field devices and solid state devices. Among his major contributions are improvements in periodic-permanent-magnetic focusing structures and the formulation of an improved design technique for such structures. He has also made unique contributions in a study of thin magnetic films, and in the computer-aided analysis of crossed-field phenomena. His first assignment at RCA, which lasted about three and one-half years, was as an engineer in the Microwave Chemistry and Physics Laboratory where he worked on focusing structures and bulk attenuators for traveling-wave tubes. There followed, for a year and a half, an assignment as acting group leader of the Magnetron Design Group; his major work here was in the development of a hydraulically tuned magnetron. From 1963 to 1967, he has led groups working on the design and development of high-efficiency TWT's for communication satellites, and recirculating TWT's for ECM systems. Dr. Schindler joined the Microwave Applied Research Laboratory of the David Sarnoff Research Center in 1967, where he worked for two years on crossed-field delay devices and computer techniques for Microwave R&D. He is now assigned to Solid State Product Engineering in Harrison. Dr. Schindler has published many articles pertaining to magnetics and microwave tubes. He has also presented a number of papers and holds three patents in the magnetics field. He is a Senior Member of the IEEE and is active in the North Jersey Section. He is also listed in *American Men of Science*.

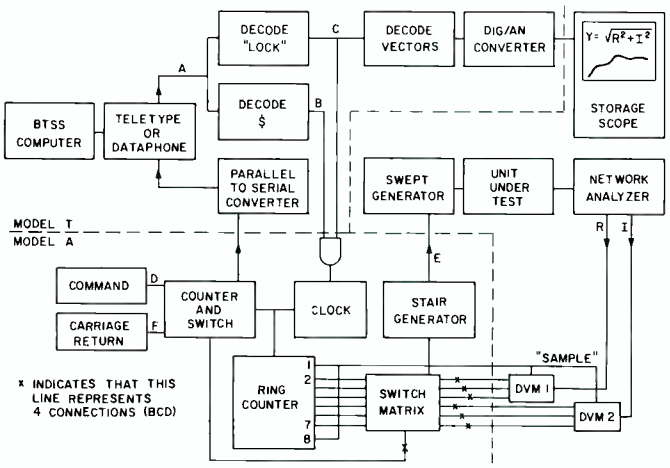


Fig. 1—The Model A/Model T computer interface.

```
 10   COMMONREAL R(40),I(40),A,X,Y,BUF(87)
 20   1FORMAT('$'N)
 30   2FORMAT(I1,40(2F3.0))
 40   (A=10;CALL MODELT(A);A=4;X=0;Y=0;CALL MODELT(A);)
 50   4PRINT 1
 60   READ2 KO,(R(J),I(J),J=1,10*KO)
 70   DO5 J=1,10*KO
 80   CALL CALC(J)
 90   X=J/KO
100   A=12
110   5CALL MODELT(A)
120   GOTO4
130   SUBROUTINE CALC(J)
140   Y=SQRT((R(J)/1000)**2+(I(J)/1000)**2)
150   RETURN
160   END
```

Fig. 2—A simple program for the Model A/Model T system.

Model T is also used to decode the command symbol which starts the Model A, and to convert the Model A output from parallel to serial form. The interaction of the major components is described in the following section.

Basic circuit

Fig. 1 shows a block diagram of the Model A/Model T interface system. Operation of this system can most easily be described by an example. The test equipment is assumed to be a network analyzer, fed from a sweep generator, so that frequency is the independent variable. The outputs are the real and imaginary parts of the reflection coefficient (RR and RI); the coefficient is available from the polar display unit of the network analyzer in the form of two voltages between −1 and +1 volt. For demonstration purposes, the magnitude of the reflection coefficient (RM) will serve as the quantity to be displayed on the storage oscilloscope at 10 frequencies.

The computer program for this test is shown in Fig. 2. During execution, when the symbol $ (hexadecimal 44) is printed on the teletype (Seq. No. 50), it also appears (in serial form) at point A (Fig. 1). This symbol is decoded and generates a logical 1 at point B. The Model T is still locked, so that another 1 appears at point C, and the AND gate turns on the clock. The clock is connected to a ring counter (RC) in which a logical 1 (+5 volts) is moved at every clock beat by one position. It may be assumed that this bit was loaded into position 6 (by means of a *Reset* button) before execution was started. The first clock pulse now moves the bit into position 7 and simultaneously closes a switch which connects the command digit (selected on a *Digiswitch*) at point D to the parallel-to-serial (P/S) converter. This digit is now read by the computer under the READ statement (Seq. No. 60, Fig. 2) as KO.

The next clock pulse moves the 1 into position 8=1, where it causes the step generator to feed the first test voltage, corresponding to frequency F(1), into the sweep generator (point E, Fig. 1). The unit under test (UUT) now generates the readings R(1) and I(1) at the outputs R and I of the network analyzer. Simultaneously the sample inputs of the two digital voltmeters are enabled, each of which has one binary-coded decimal (BCD) output for each of its three digits.

When the next clock pulse moves the 1-bit to position 2, the digital voltmeters (DVM's) hold their readings, and the first digit of the first voltmeter is connected to the parallel-to-serial converter, and thereby to the computer. This procedure is now repeated for the remaining 5 digits, thus completing the first set R(1) and I(1) of the READ statement. The next clock pulse raises the voltage in the stair generator to the second level, corresponding to F(2), and the 6 digits are scanned again. The whole cycle is repeated until the counter reaches a preset value, for example, 40. The counter now connects the parallel-to-serial converter to point F which provides the carriage return (hexadecimal 0D). When the computer receives the 0D, it continues execution of the program (Seq. No. 70, Fig. 2). The DO-loop, Seq. Nos. 70 to 110, calculates the values Y(I) to be displayed on the scope, by calling SUBROUTINE CALC. In the example, this quantity is simply the geometric sum of the R and I readings. When the array Y(I) is available, the MODEL T subroutine is applied; this subroutine is contained in the BTSS memory. Details of MODEL T operation and its application are discussed in reference 2. When the graph is completed, the whole cycle, starting with statement 4, repeats itself, while the operator may make adjustments for example, to minimize the reflection coefficient) on the UUT.

It should be noted that the number of frequency points covered by the READ statement is determined by the setting of the command switch. In this simple example, the value of KO would be restricted to values from 1 to 4, because only 40 frequency steps are available. A more general application of the command switch is discussed later.

Circuit boards

Datascan, Inc. circuit boards[3] were used in the construction of the Model A; their function is described briefly below. The complete schematic diagram shown in Fig. 3 identifies the boards by roman numerals, while letters and arabic numerals identify connector pins. Decoding of the start signal ($) and parallel-serial conversion of the output digits are performed by slightly modified Model T boards (not shown in Fig. 3).

The *Clockboard* (I) supplies the clock pulses for the Model A. This

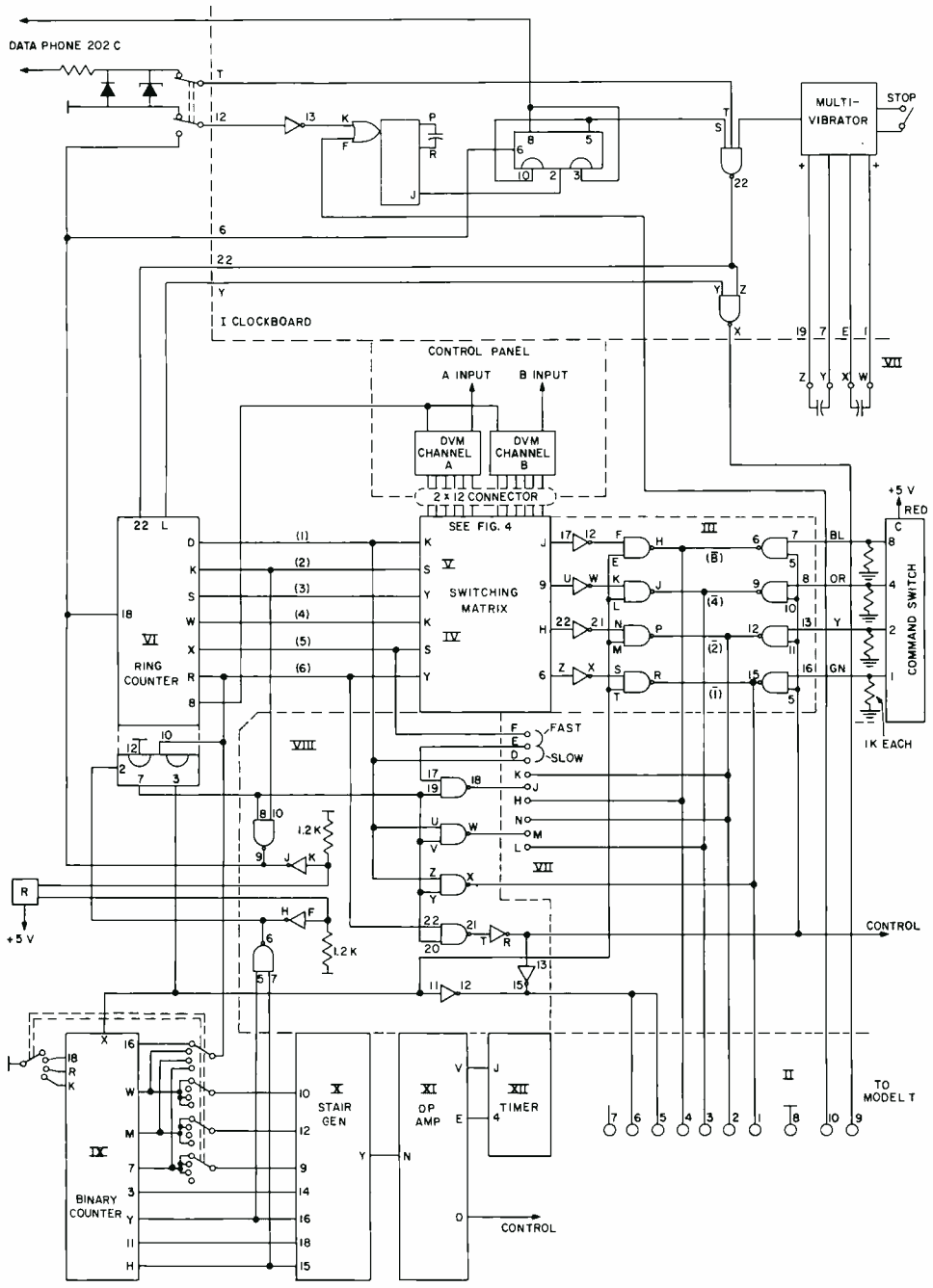


Fig. 3—Complete schematic of the Model A.

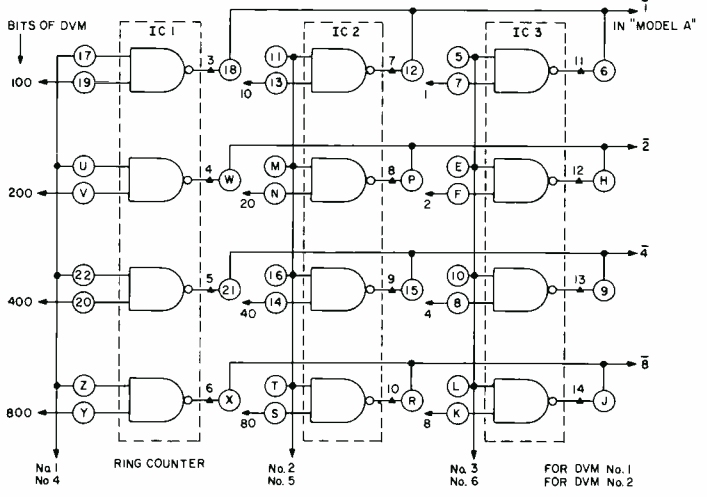


Fig. 4—Scanning matrix for 3 digits.

board was modified by bringing out additional outputs which are used to turn the clock *on* and *off* as needed, and to connect the appropriate capacitors which slow the multivibrator to the desired clock frequency. Either 10 or 120 characters per second can be scanned, depending on whether a teletype or Dataphone is used. The *Ring Counter Board* (VI) is an 8-bit shift register. Only seven of the flip-flops from the board are needed for the ring counter and the eighth is severed, as shown in the Fig. 3, to be used otherwise.

The *Binary Counter* (IX) is used to count to 10, 20, or 40 depending on where the ring-counter pulses are applied. After reading the desired count, this board terminates the scan cycle.

The *Stair Generator* (X) converts the binary outputs of the counter (IX) to an analog signal, thereby generating the stair function which represents the independent variable. This signal is converted from the range of 0 to +5 volts to a range of −10 to +10 volts by the *Operational Amplifier* (XI), which also supplies sufficient power to drive a 5000-ohm load.

The heart of the Model A are the *Switching Matrix Boards* (IV and V) shown in Fig. 4. Each of these boards multiplexes the three BCD digits from one DVM, depending on which of the inputs, RC No. 1 through 6, is high. The outputs labeled 1, 2, 4, 8 are paralleled with the same outputs of the second board. With different connections, the same board also connects the command switch onto the system (III) and supplies punctuation characters (VIII).

The *Timer Board* (VII) determines the speed of the clock by connecting the proper capacitors. The remaining connections select the appropriate punctuation, i.e., carriage return (hexadecimal 0D) at the end of a 10-characters-per-second transmission, and start of message (hexadecimal 02) and end of message (hexadecimal 03) at beginning and end, respectively, of a 120 characters-per-second transmission.

Because the internal circuits of the Model T and Model A work with 0, +4, and +5 volts, respectively, while the telephone circuits work with ±10 to 20 volts depending on model

and system used, interface circuits are needed. Except for the "handshaking" circuitry,[4] which turns around the telephone connection, all connections with the telephone system go to the Model T. Incoming signals are directly acceptable to the Model T while outgoing signals must be converted. For the slow speed, this conversion is performed with a reed relay because the teletype circuitry only requires contact closures. For the high speed (Dataphone 202C), a simple transistor circuit performs the conversion.

Circuit description

The functioning of the Model A circuit in Fig. 3 is best discussed in conjunction with the timing diagram in Fig. 5. The fast operating mode (120 characters per second) is assumed because it is somewhat more involved.

Before execution of the computer program is started, the Model A must be readied by depressing the reset button R, which zeroes the binary counter and loads a 1 into the appropriate position (point VI—S) of the ring counter. The start signal ($) is applied to I—F which, after a 50-millisecond delay, makes the flip-flop output (I—5) change to 1. This output is also connected to pin 4 of the Dataphone, model 202C. The positive voltage at this pin constitutes a *request to send*, which causes the carrier to be turned on in the Dataphone. When the Dataphone is *clear to send*, the voltage on its pin 5 turns from negative to positive. Thus, point I—T, which so far was held to 0 by a diode, goes positive, and the clock pulses appear at I—22. The time delay is required to give the telephone equipment time to stabilize, and the "handshaking" process is completed.

When the clock starts, flip-flop output VI—3 is a binary 0 (ground) which indicates the 00 condition of the Model A. This state occurs at the beginning and end of the scan cycle; it is used to apply punctuation characters.

When step 00 coincides with ring-counter position 5, the NAND-gate output VIII—18 goes low, and the complement of hexadecimal 02 is applied to the parallel serial converter of the Model T. This character signifies *start of message* (line 33, Fig. 5) to the computer, which, in the 120-characters-per-second mode, disregards all signals arriving before the hexadecimal 02. The next clock pulse activates ring-counter output VI—R, which connects the Command Switch to the parallel-to-serial (P/S) converter because III—5, 10, 11 and 16 go high.

The next clock pulse switches the flip-flop output VI—3 to 1, and the first step in the scan cycle begins. The stair voltage has not changed so far, and, therefore, the current state can be identified as step 0. Ring-counter position 7 now causes the DVM's to sample, while positions 1 through 6 connect the DVM digits to the P/S converter, as indicated in lines 6 through 12, Fig. 5. Because flip-flop output VI—3 (line 16), is now high, the binary counter is counting, and the next 1-to-0 transition from ring-counter position 6 raises the step voltage to step 1. Sampling and scanning proceed as before, until the stair has reached step 9.

When, at the end of step 9, the binary counter reaches 1010 . . ., NAND-gate output VIII—6 goes to ground, and the flip-flop output VI—3 follows (line 16, Fig. 5). Thus, the 00 condition is again obtained. When it coincides with ring-counter position 1, the NAND-gate outputs VIII—W and —X apply the complement of hexadecimal 03 to the P/S converter. This signal indicates *end of message*, which is equivalent to the *carriage return* in the teletype mode. The BTSS buffer is now emptied, while the Model A resets itself, as evidenced by lines 22 and 6 in Fig. 5, thereby becoming ready to respond to the next *start* signal.

Control panel

While the Model A is a self-contained unit, it does, in the described application, have to interact with other components, namely, the Model T, the DVM's, the Dataphone or teletype, and the test equipment. All of these interfaces are combined in the control panel; the schematic diagram for the panel is shown in Fig. 6.

To make the Model A as universally applicable as possible, two identical inputs (channel A and channel B) are provided with a variable offset voltage and variable voltage divider. As a result, the input can be adjusted to the range from 0 to +1 volt needed by the DVM's. A calibration switch permits quick checking of the offset voltage, which would normally be set to 0.5 volt. Similarly, the step-voltage output is adjustable and provided with an offset voltage.

The control panel provides one important convenience: by means of a *local* switch, the connected test equipment can be operated independent of the

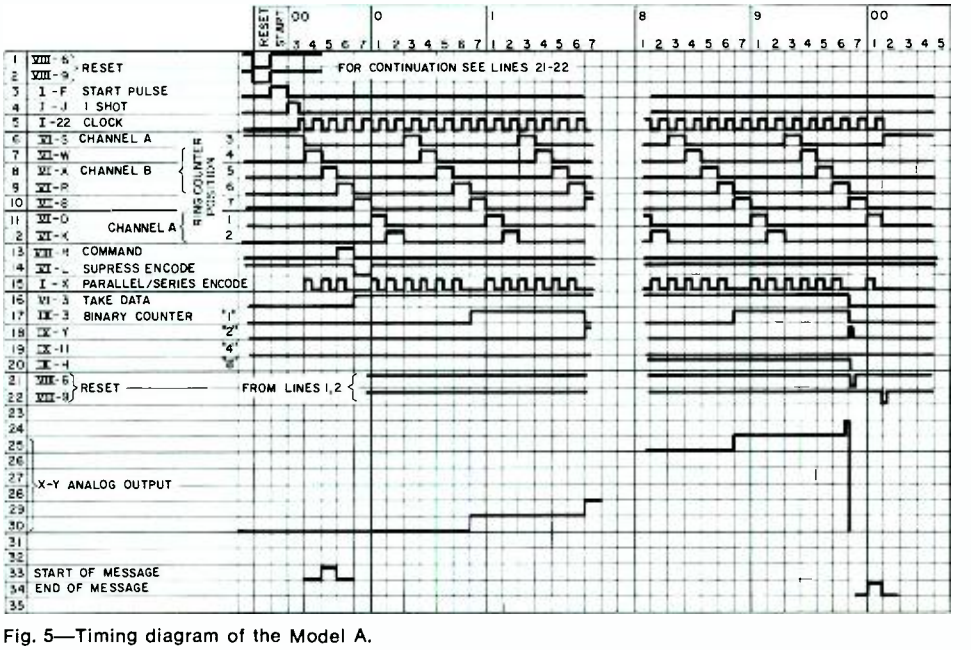
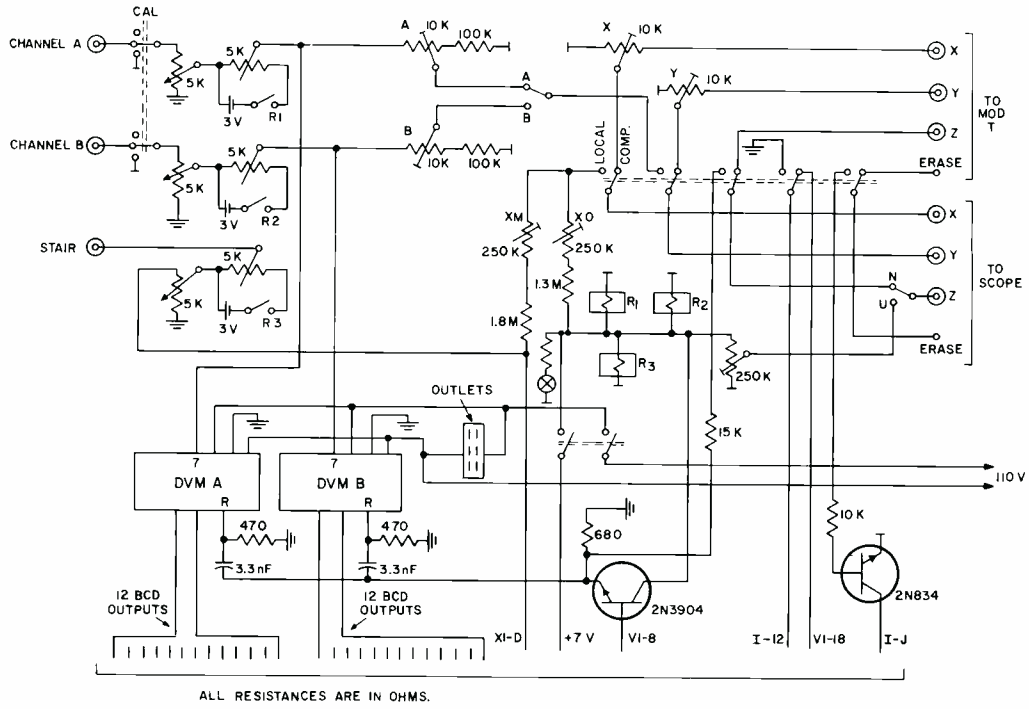


Fig. 5—Timing diagram of the Model A.



ALL RESISTANCES ARE IN OHMS.

Fig. 6—Schematic of the control panel.

computer. In this case, the horizontal scope deflection is taken directly from the step generator, and the vertical deflection from either channel A or B. At the end of the scan cycle the 1-shot pulse (line 4, Fig. 5) is used to erase the scope and start a new scan cycle. The *local* feature is not only insurance against the frequent computer failures, but also permits leisurely calibration of the test set and occasional reversion to the raw data when the display of the calculated quantity looks suspicious.

MATE = Model A + Model T + Control Board

As shown in Fig. 7, the modified Model T, the Model A, and the control board can be mounted in one rack to provide a self-contained piece of equipment which can be used to interface a wide range of test gear with the BTSS computer. For ease of reference, this combination is called MATE (Manual/Automatic Test Equipment) because it can operate engineering tests either automatically through a computer program or in the local mode under manual control.

Normally, the storage oscilloscope displays the Model T output in the computer mode, and the value of channels A or B at the moment of sampling in the local mode. During calibration, it becomes necessary to stop the clock on a given step and make adjustments until, for instance, a frequency meter indicates the correct settings. Because it may be desirable to also display the output of the frequency meter on the storage oscilloscope, the sampling circuit is overridden with an *unblank* switch, which turns on the electron beam and keeps it on continuously.

The *normal/locked* switch in the Model A is not only used in "freezing" any given step of the stair generator, but also prevents the occurrence of a hexadecimal 44 ($) from triggering a scanning sequence, for example, when the symbol $ appears in the COST message, or due to noise on the line.

Demonstration program

The demonstration program DEMON shown in Fig. 8 is useful in trying out MATE in the computer mode, and can serve as a model for other programs. The flow chart in Fig. 9 shows how, by setting the Model A control switch, different branches of the program with a different number of sample points, different display format, and different mathematical content can be selected.

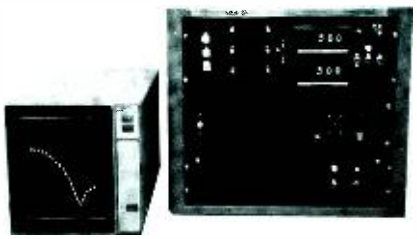


Fig. 7—Photograph of MATE and graphic display.

For convenience, the READ command in DEMON is at the end of the program, so that the scope display reflects the previous cycle. The *command* switch can be set at any time except at the very beginning of a scan cycle.

In the first position (KO=1), 10 points of both inputs (CHA and CHB) are displayed directly, one with dots, the other with pique marks. Switching of KO to 2 results in 20 test points, for CHA only; KO=3 displays 40 points of CHA, connected by a line while KO=4 produces the geometric sum $(CHA^2 + CHB^2)^{1/2}$ in the form of connected pique marks. Positions KO=5 and KO=7 display sin x/x (where x = CHA); setting 7 suppresses the ERASE command for the storage oscilloscope and permits integration over any desired length of time. This setting could be used, for instance, to observe equipment drift. The remaining switch positions produce the console printout BRANCH EMPTY.

A look at the future

Development of the Model A has shown that data couplers can be con-

```
 10 C DEMONSTRATION PROGRAM FOR MODEL A 1-23-70
 20 1 FORMAT(I1,40(2F3.0))
 30 2 FORMAT(' $',N)
 40 3 FORMAT(I4,2F10.0)
 50 4 FORMAT(//' THIS BRANCH IS EMPTY '///)
 60 REAL CHA(40),CHB(40)
 70 COMMON YA,YB,AT,XT,YT,BUF(87)
 80 COMMON INTEGER I,NM
 90 (KO=1;CX=9.6;CY=8.;C5=.01;NM=10;)
100 READ J
110 IF(J>0)GOTO7
120 DO 5I=1,40
130 CHA(I)=500
140 5 CHB(I)=1
150 6IF(KO=7)GOTO99
160  AT=101.
170 CALL MODELT(AT)
180 AT=4.
190 XT=0
200 YT=-1.
210 CALL MODELT(AT)
220 AT=2.
230 YT=0.
240 CALL MODELT(AT)
250 IF (KO=0) STOP
260 99CONTINUE
270 GO TO (11,12,13,14,15,11,15,19,19,19)KO
280 11 NM=10
290 DO  21I=1,NM
300 XT=I*CX/NM
310 YA=CHA(I)/1000*CY
320 YB=CHB(I)/1000*CY
330 CALL PLOT
340 21 CONTINUE
350 IF(KO=6)PRINT 3 (I,CHA(I),CHB(I),I=1,NM)
360 GO TO 20
370 12 NM=20
380 DO 22I=2,NM
390 XT=I*CX/NM
400 YT=CHA(I)/1000*CY
410 AT=12.
420 CALL  MODELT(AT)
430 22 CONTINUE
440 GO TO 20
450 13  NM=40
460 DO 23I=1,NM
470 XT=I*CX/NM
480 YT=CHA(I)/1000*CY
490 IF(I>1)AT=1;ELSE AT=2
500 CALL MODELT(AT)
510 23 CONTINUE
520 GO TO 20
530 14 NM=10
540 DO 24I=1,NM
550 XT =I*CX/NM
560 YT=SQRT(CHA(I)**2+CHB(I)**2)/1500*CY
570 IF(I=1)AT=12;ELSE AT=11
580 CALL MODELT(AT)
590 24 CONTINUE
600 GO TO 20
610 15  NM=20
620 DO 25I=2,NM
630 XT=I*CX/NM
640 YT=ABS(6.*SIN(C5*CHA(I))/C5/(CHA(I)+1))
650 AT=12
660 CALL MODELT(AT)
670 25 CONTINUE
680 GO TO 20
690 19 PRINT  4
700 PAUSE
710 20 AT=-1.
720 CALL MODELT(AT)
730 7PRINT 2
740 READ 1 KO,(CHA(I),CHB(I),I=1,NM)
750 GO TO 6
760 SUBR.PLOT
770 COMMON YA,YB,AT,XT,YT,BUF(87)
780 COMMON INTEGERI,NM
790 XT=I*9.6/NM
800 YT=YA
810 AT=12.
820 CALL MODELT(AT)
830 AT=2.
840 YT=YB
850 CALL  MODELT(AT)
860 AT=1.
870 YT=YT+.02
880 CALL MODELT(AT)
890 RETURN
900 END
```

Fig. 8—Program listing of DEMON.

structed easily and inexpensively if certain guidelines are observed. The general requirement for a data acquisition system is that a number of analog signals must be scanned, the readings must be converted to a digital system (usually BCD), and punctuation and alphabetic characters must be inserted. For the scanning, two basic approaches are possible: multiplexing of the analog signals to a common analog-to-digital (A/D) converter, or use of separate A/D converters followed by digital scanning as in the Model A. The first approach would be more economical, if the number of channels exceeds 5, but is disadvantageous in that the analog voltages to be monitored can vary in magnitude from microvolts to volts, and in accuracy from 2 to 6 significant figures. Also, increasingly fewer test data are available in analog form (for example, from frequency counters). A system of the second alternative is, therefore, more versatile, because an unlimited number of digits can be scanned and formatted.

In such a system, two kinds of switch matrices are needed, one with 4 bits for numbers, and one for symbols or letters with 7 bits. For a scan of the various positions, flip-flop chains are used; these chains can be severed for the transition from one DVM (or A/D converter) to the next. The Encoding Complete output from the converter or meter can then be used to enable the next flip-flop chain. The switch matrix boards should contain, in addition to the NAND gates, a set of optional inverters at the outputs to permit grouping of digits and signal regeneration; OR gates on the flip-flop board are also required for grouping, but, in addition are useful when the same symbol has to be inserted repeatedly.

At present, the circuit boards described can be obtained at $50 or less, with tooling charges well below $500. Thus, multiplexing will typically cost $7 per numeral and $15 for a symbol, plus $5 for either one to account for the driver chain. Aside from the DVM's or A/D converters, data acquisition for a test set monitoring 10 values with 30 digits would thus be possible for as little as $500, plus a one-time tooling charge of less than $1500. In view of the tremendous benefits of a permanent and error-free record, it appears obvious that data acquisition should be seriously considered, even if computer manipulations are not envisioned. A paper-tape punch (for example, from a teletype terminal) will serve as the most economical storage device.

Data acquisition systems similar to the one described above are now appearing on the market with prices ranging from several thousand to well above ten thousand dollars. Together with inexpensive digital multimeters (under $500) they could have a profound impact on the way engineering experiments will be conducted in the future. Unfortunately, the desire to make data acquisition equipment universally applicable keeps the price of most commercial units prohibitively high. Large engineering groups, as they exist within RCA, could benefit substantially from construction of equipment such as MATE, tailored to their specific needs.

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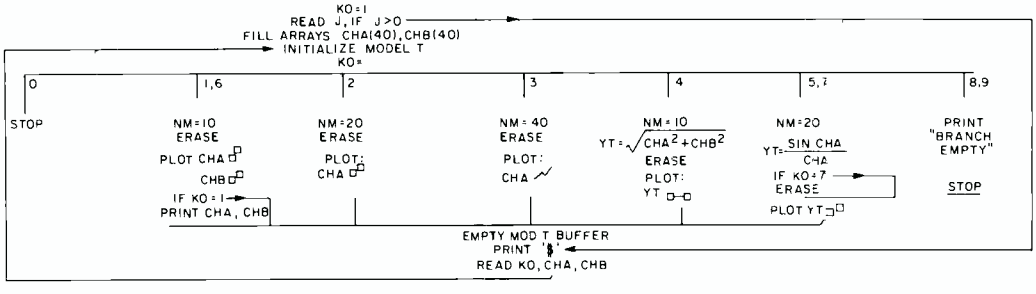

Fig. 9—Flowchart of DEMON.

Unique TV display controller for remote computer terminals

R. S. Lewis

This paper describes a controller for digitally-generated-video displays used in computer-assisted instruction at an elementary school level. The controller was developed by Electromagnetic and Aviation Systems Division, Van Nuys, California. The final design employs techniques which are of interest both for the specific task and for the general applications. Presently, the controller, several displays, and keyboards are being used experimentally as terminals to communicate with a Spectra 70/46 under the Time Sharing Operating System. The experiments are being conducted by the RCA Systems Programming Laboratory, Palo Alto, California.

THE FIRST GENERATION of RCA Computer-Assisted Instruction (CAI) systems is exemplified by a 192-terminal network operating in the New York City School System.[1,2] Each terminal is a teletypewriter linked by telephone lines to a Spectra 70/45 central processor. The network is divided into four 48-terminal groups, each group possessing a line concentrator which communicates over a high-speed (2400-baud) line with the central processor and over a low-speed (100-baud) line with each terminal. The dominant applications of the system are drill and practice in reading and math.

For a second-generation terminal, the ordinary home TV receiver is the logical choice for the following reasons: It is quiet, economically mass produced, and can display whatever is broadcast in addition to the necessary alphanumerics; it also has built-in audio facilities which are potentially useful. The nucleus of the new terminal then is a TV set and keyboard.

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Display requirements

The primary requirement of the display is to provide both upper- and lower-case alpha characters, numerals, and special symbols. In particular, for a student learning to read, these characters should be of high quality. The reading course also involves diacritical marks. Some limited capability for graphics is desired, i.e., horizontal vertical, and diagonal line segments. A few superscripts complete the symbol repertoire, from which the display format is derived.

The symbol repertoire and the human factors involving visual resolution determined a character set, examples of which are shown in Figs. 1a and 1b. Because of bandwidth limitations of the unmodified video driver in the TV receiver, a 5-MHz upper cutoff frequency was established for the video signal. A sense of proportion—caps to lower case, superscripts, diacritical marks, etc.—seemed to indicate a character space approaching that which was chosen—i.e., each character is formed within 28 interlaced lines (14 in each field) vertically and $\frac{1}{48}$ of the horizontal sweep horizontally (actually about $\frac{1}{32}$ of the visible portion of the sweep). Hardware considerations established these dimensions more firmly.

Memory

Of the several possible alternatives for supplying refresh memory, two devices were serious contenders: 1) a disc which would store the digital video for each terminal on one track or 2) a magnetostrictive delay line which, incapable of video response, would store the 8-bit (ASCII) code for each character. With the delay line, the contents could be slowly read, buffered, and applied to a character generator in real time. To some extent, cost considerations led to choice of the delay line. However, a major consideration was that the magnetostrictive delay line was probably more reliable than the rotating disc.

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received the BSEE from the University of California, Berkeley, in February 1959. Following graduation, he joined a digital systems group at Lockheed Missiles and Space Company, Sunnyvale, California. While at Lockheed, he designed logic and peripheral circuits for checkout and telemetry systems. Simultaneously, he completed requirements for the MSEE and received that degree at Berkeley in June 1962. In 1963, Mr. Lewis left Lockheed and joined the Electronic Engineering group at Stanford Linear Accelerater Center, where he completed several projects relating to information display, telemetry and instrumentation for physics experiments. In 1967, he joined the Advanced Development group of RCA Instructional Systems, Palo Alto. He contributed to the implementation of time-shared digitized video and audio facilities. Presently, Mr. Lewis is in the peripheral systems group of the Systems Programming Product Laboratory, Palo Alto, where he is working on aspects of remote interactive terminals.

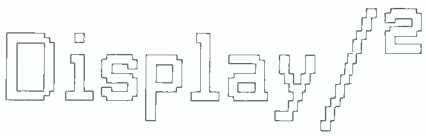

Fig. 1a—Part of a row of characters. Capitals use 14 (interlaced) sweeps. Each character space contains 6 additional sweeps above the top of the caps for superscripts and 8 additional sweeps below for "tails", underlines and graphic characters.

Use of a standard TV raster and choice of 1/45 horizontal sweep time for the width of a character means that a new code (8 bits) must be available every 1.32 μs. The delay line can be read at about 1 megabit/second. Therefore, buffering is necessary. Although a new character must be generated every 1.32 μs, it requires 14 sweeps to produce a single row of characters. Thus, a row of information may be read from the delay line slowly (over several horizontal sweeps) into a buffer. This code, which represents the entire row, is then applied to the character generator 14 consecutive times. The code is first interpreted to display the top line and so on. While, the character generator is producing the first display row (14 sweeps), the information is read from the delay line for the second row, and so on. The delay line must have an electrical length of 16.7 ms to conform to the standard refresh rate, i.e., both an odd field and an even field are displayed every 1/30 second.

In the final design, the delay line is packed more densely so that the code for an entire row is obtained in less than 6 horizontal sweeps. This allows one delay line to store information alternately for two terminals. The delay line contains, in time sequence: row 1 for terminal A, row 1 for terminal B, row 2 for terminal A, row 2 for terminal B, etc. Each terminal must have access to two dual-speed buffers, one reading slowly from the delay line; the other rapidly writing, i.e., applying code to the character generator. As will be described, the reading buffer can be, and is, shared between the two terminals on the same delay line; but both write buffers will usually be active simultaneously. In the present system, these buffers are each 32-characters (256-bit) shift registers. Thus, three storage areas are required for each pair of terminals.

Readout is accomplished as follows (Refer to Table I): During scan lines 1 through 7, row 1 for display A is read out from the delay line while displays A and B are blanked. During lines 8 through 14, row 1 for display B is read out from the delay line while row 1 of display A is written back into the delay line *and* while row 1 is interpreted for the first 7 (of a total of 14) sweeps. (Synchronization logic causes the "delay line periods" of 63.5 μs to effectively correspond to scan lines which are also 63.5 μs each.)

Discussion of the character generator, which follows, clarifies the above description.

Character generation

Assuming 14 horizontal sweeps in a character space, the stored ASCII code in memory must be encoded into a video bit stream 14 individual times (i.e., once for the first slice, once for the second, etc.). Therefore, there are 14 interpreters. (Actually in general there are 28 different interpreters; 14 used in the odd field and 14 used in the even field. However the routine is the same for the two fields.) A row of code is presented to each interpreter in sequence. From the discussion of memory, the routine would be as follows: For 6 sweeps, the read buffer slowly accumulates the code for row 1, terminal A. During the 7th sweep the read buffer empties to the write buffer for terminal A. At the 8th sweep time, the read buffer begins to slowly read row 1, terminal B, from the delay line and simultaneously row 1, terminal A is presented by the write buffer to the character generator, section 1, (or interpreter 1). Row 1, terminal B, is finished being read during the 13th sweep (while row 1, terminal A, is producing the 6th sweep or slice of its characters). During row 14, the read buffer transfers row 1, terminal B, to terminal B's write buffer. There has been a 14-sweep cycle and now the read buffer begins to fill with row 2, terminal A, and the cycle repeats. Note that during the 15th sweep, the character generator is producing the 8th sweep of row 1 for terminal A and the 1st sweep of row 1 for terminal B. Table I shows a complete cycle from the first to last TV sweep for the delay line.

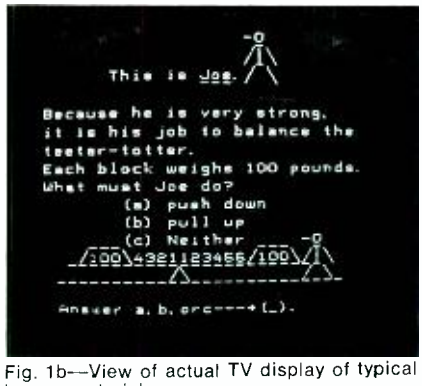

Fig. 1b—View of actual TV display of typical lesson material.

Now from the standpoint of section 1 of the character generator, what happens? It interprets for terminal A during one sweep, then is idle for 6 sweeps before looking at terminal B's code.

Table I—Simultaneity of memory and display activity for one delay line shared by two displays.

Delay-line periods (63.5 μs/ period)	READ row	READ for display	WRITE row	WRITE for display	A	Display scan lines	B	Display scan lines
1-7	1	A			Blank	1-7		
8-14	1	B	1	A			Blank	1-14
15-21	2	A	1	B	Row 1	8-21		
22-28	2	B	2	A			Row 1	15-28
29-35	3	A	2	B	Row 2	22-35		
36-42	3	B	3	A			Row 2	29-42
43-49	4	A	3	B	Row 3	36-49		
50-56	4	B	4	A			Row 3	43-56
57-63	5	A	4	B	Row 4	50-63		
64-70	5	B	5	A			Row 4	57-70
71-77	6	A	5	B	Row 5	64-77		
78-84	6	B	6	A			Row 5	71-84
85-91	7	A	6	B	Row 6	78-91		
92-98	7	B	7	A			Row 6	85-98
99-105	8	A	7	B	Row 7	92-105		
106-112	8	B	8	A			Row 7	99-112
113-119	9	A	8	B	Row 8	106-119		
120-126	9	B	9	A			Row 8	113-126
127-133	10	A	9	B	Row 9	120-133		
134-140	10	B	10	A			Row 9	127-140
141-147	11	A	10	B	Row 10	134-147		
148-154	11	B	11	A			Row 10	141-154
155-161	12	A	11	B	Row 11	148-161		

Of the 14 sections in the character generator, no more than 2 are busy at any instant. This suggests that 6 more delay lines, interleaved properly, could share the same character generator. Effectively, this is what has been done.

Seventy percent of the controller consists of the memory control, dual buffers for delay lines, complex interfaces for the delay lines, and the shared character generator. The sharing of the character generator is the unique feature of the controller.

Keyboard input

To allow information to enter the delay line from two sources (i.e., the keyboard or the central processor) the delay-line loop is actually broken and the buffers mentioned previously are placed in series with another read buffer to allow parallel access. Thus, each delay line brings data to the buffers, and the same data (or new data for the same location) is later written back into the delay line, whatever changes necessary having taken place in the buffer. We now describe the keyboard data path.

For a student, the philosophy of computer aided instruction is to allow him to enter a character directly into his display, at the same time sending it to the processor, which then echoes the same character. In this way, the student senses a quick response time; yet the final displayed character is what has been received by the processor, if the two should disagree.

For a curriculum author, the mode is pure echoplex, with nothing appearing in the delay line unless transmitted from the processor. The two modes (student and edit) are programmable for each terminal and are keyed by a bit in each processor-to-controller message.

To economize on communication lines, each terminal link to the controller is a coaxial cable which carries video to the terminal and keyboard data from the terminal. This is done by means of frequency division with keyboard data being FM encoded around a center frequency of 10.7 MHz (See Fig. 2).

Since the controller generates all timing and TV sync (compatible) signals, it is convenient to strobe keyboards with a horizontal sync pulse. Every horizontal sync pulse brings a bit from each keyboard into its own one-bit buffer located in the controller. Normally this bit is a binary zero. When a key is struck, the next strobe brings in a start (1) bit and the following eight strobes bring in the data bits. This data is then inserted into the keyboard memory [all mention of keyboard memory refers to a buffer portion of the controller, not some part of the keyboard] which contains for each terminal two bytes plus two bits—i.e., one data byte, one status byte and a four-state cyclic counter. The counter is present to detect errors and to distinguish multiple striking of the same key; it increments at each stroke. The status byte assists in accumulating data bits (serving as a counter) and sets flags indicating whether the data has been inserted into the delay line or output buffer message. The status byte also senses when a good message is received at the input buffer and causes an acknowledgment (ACK) to be put into the output message.

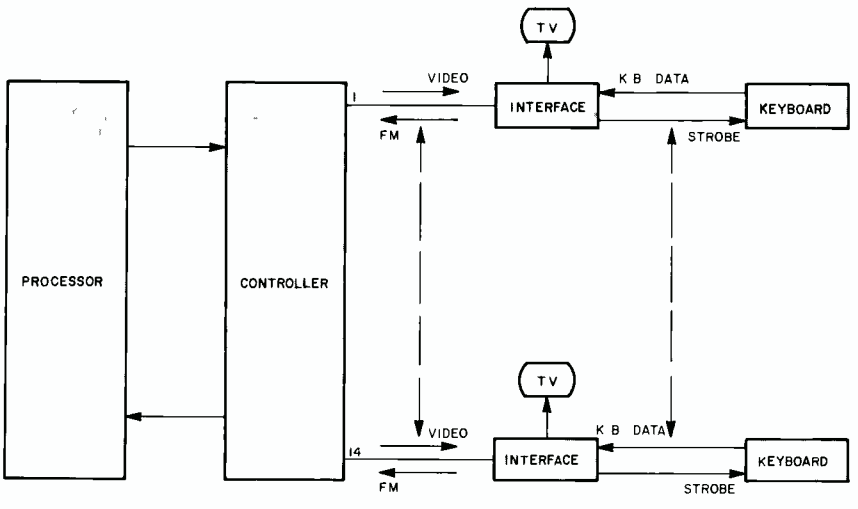

Fig. 2—System interconnection.

Input /output

Communication between controller and processor is synchronous, 2400-baud or slower, full duplex. The transmission from controller to processor is fixed length and format, always 26 characters (85.8 ms period) as follows:

SYN, SYN, SYN, SYN, STX;
Terminal 1 data, terminal 2 data, . . . , terminal 14 data;
Terminal 1-2-3 tag, terminal 4-5-6 tag, . . . , terminal 13-14 tag;
ETX, block parity.

In the tag characters, the least significant 6 bits represent the cyclic counters for three terminals, each pair of bits showing the same count as the corresponding pair in the keyboard memory. This entire 26-character format is transmitted continually.

Messages from the processor to the controller are of variable length. Each message is addressed to a single terminal only and has the following format:

At least four SYN characters;
STX, TERM, ROW, COLUMN;
CHAR 1, CHAR 2, . . . , variable up to 32 maximum;
ETX, block parity.

TERM represents the terminal addressed, ROW and COLUMN are the display coordinate, for the new message. The maximum number of new data characters is 32. The new message does not have to be entered into the display contiguously; there exists a skip code. However each skip code requires a new pair of coordinates (ROW, COLUMN) which must be temporarily stored in the input buffer as data; thus, one skip code reduces the maximum number of printables for that message to 29. Each message is sent until it is acknowledged.

Input messages arrive asynchronously with respect to the cycling of the delay line which is their destination. The longest time that an error-free message remains in the input buffer is about 30 ms. This case comes about when characters are to be inserted at the top of the display and at the bottom. The coordinates are compared sequentially and singly. Therefore, if the input has just missed the delay line *top of page*, then it must wait a full revolution be-

fore finding the first set of coordinates, after which messages are inserted until the *bottom of page* is reached. With such a scheme, skipping backward is not permitted. The coordinates of different segments of the same message must be arranged in time sequence.

The buffer capacity is sufficient to handle the case just described. At 2400 baud, during the wait period, at most 9 or 10 characters may arrive; the buffer provides the extra 10 characters of storage. However, if the controller were to try to accommodate higher speed by merely expanding the extra buffer, the 30-ms wait period would limit the rate to 7200 baud, after which the possibility for overflow exists no matter how many extra characters of storage are provided. The average wait after verification is likely to be some 10 ms in the present system.

Further considerations

The keyboard memory holds most of the information about the dynamic state of the controller, that is, everything except what is shown on the display.

When the input message has been checked for horizontal and vertical parity, the keyboard memory is signaled to provide an ACK in the output message of that terminal.

When the latest keyed character which has been stored is inserted into the delay line, a status bit in that terminal's satus byte reflects this. Similarly, when that same character has been placed in the output message for the first time, another status bit is set, and the two-bit cyclic counter is incremented. This so-called sequence count is also inserted into the output message. Storage in the delay line and insertion into the output message have no time relation. The keyboard memory can acquire bits from the keyboard at the horizontal-sync pulse rate. Therefore a new character is stored some 500 μs after key stroke. The entire keyboard memory is scanned and updated during every horizontal-sync-pulse period. A character may be delayed before entering the output buffer for 85.8 ms at most (one cycle of the output buffer). The average delay is one-half the cycle time, or 43 ms.

Each keyboard has its own parallel input to the keyboard memory. This means that if all 14 terminals keyed a character simultaneously, after 500 μs all those characters would reside in keyboard memory. A queue now develops, however, for entry into the respective delay lines. The memory is continually scanned until a terminal is found with data ready for insertion into the delay line (in this case *all* are ready). The character is then transferred to a holding buffer to await the position of the cursor or its delay line. When the cursor is found, the keyboard data replaces the cursor. Then the next ready terminal is found. Therefore, the expected wait for the 14th terminal, in the extreme case being described here, is 14 times one-half the delay line cycle or 112 ms.

Interface

As already stated briefly, the interface with the terminal consists of a coaxial cable. Drivers and receivers allow 2000-ft. length between controller and terminal. The cluster is meant to be contained within one building. At the controller end, the keyboard data is FM demodulated and sent to the keyboard memory. The video drivers transmit the mixed video signal to the terminal.

The computer interface provides for connection either to a data set 201B or directly to a 70/45 processor through the communications controller. As stated, however, without considerable expansion of the controller input buffer, the information rates are limited to 7200 bits/second.

Technology

We have described the terminal control unit from a functional standpoint. Some slight liberty has been taken with the description of the memory and shared character generation, in the interest of conceptual clarity.

Physically, the terminal control unit was assembled using 80-pin cards, each containing up to 30 integrated circuits. Every IC used was a standard off-the-shelf model. Over 70 cards were necessary, grouped in four rows. As noted, two-thirds of the cards were dedicated to the delay-line memory synchronization and interface together with the shared character generator.

Using presently available technology, the character generator could be reduced to a series of read-only memories and registers, such that 28 cards of logic might be reduced to two. The MOS memories available are becoming cost competitive with delay lines themselves and are especially so because the complex synchronization logic could be all but eliminated were MOS memories to be employed to store the 4 kilobits necessary for each display. Thus, a reduction from fourteen cards and seven delay lines to perhaps four cards and no delay lines is predictable.

It can reasonably be argued that for applications other than CAI, such a versatile and complicated character repertoire is unnecessary. A simplification of the repertoire implies a reduction in the size of the individual character space and an attendant increase in the number of characters displayable on the screen. (Naturally an increase in memory capability is also necessary to display more characters.)

There is a one-to-one correspondence between the number of character generator "sharers" and the number of horizontal sweeps in a character, assuming the technique already described. If, for example, only seven sweeps were sufficient for a character, then only seven terminals could share the character generator. One direction of expansion might be to slice the encoding time, i.e., to commutate the same read-only memory (ROM) such that, within one microsecond, it could encode several independent bit streams into video. This approach would entail a one-word buffer before and after each ROM, for each sharer, with commutating and decommutating logic of increasing complexity. The shared character generator must be evaluated with respect to economy in the light of the new technology.

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Interactive real-time audio data interface for Spectra computers

R. G. Chappell | A. C. Lechner | Dr. W. J. Utz

The RCA Instructional System Group has developed a computer-assisted instruction (CAI) system designated I-71. This system includes a computer controlled audio message generation subsystem which delivers sentences from a dictionary of digitized audio words to a group of 32 individual student terminals. Applying dictionary organization to CAI audio systems introduces new problems in audio recording. The dictionary creation requires attention to uniformity in the pronunciation of each entry so that it may be used in many different contexts without introducing unwanted prosodic features. A Spectra 70/45 digital computer with a real-time audio I/O interface is used to enter each word and to immediately play it in various grammatical contexts. This feature allows the speaker to interact with the system making corrections to pronunciation. The design of the real-time audio data control interface and processing software is described.

EXPERIMENTS with tape recordings confirmed linguists' fears that sentences composed of words spoken out of context would not have a natural sound. In fact, prosodic features such as variations in stress, intonation, and emphasis tend at times to break the sentence in the wrong places, and otherwise interfere with the intelligibility of the audio output.

Experiments were initiated on a Spectra 70/45 computer to deliver strings of words with controlled pauses on command from the console. Some improvement in naturalness was achieved by carefully trimming words to length and controlling pauses between them, but better control was needed in the pronunciation of each word to make it fit as smoothly as possible in the various contextual usages. For instance, the word "race" may be found in various contexts as an adjective, noun, or verb; at the same time it may occupy any physical location in the sentence structure.

To provide a facility to tackle these problems, a real-time computer interface was developed with which analog words could be digitized, played in various contexts, corrected, and re-entered until a usable pronunciation is achieved. Because data storage space on the digital audio disc is at a premium, other important software functions designed for the facility are provisions for the operator to trim excessive length from the ends of words, and remove redundant internal word segments to shorten them and minimize their storage requirements.

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Operation

A typical user cycle might consist of the following information flow. The analog audio data is converted to binary, placed on disc via the swapping technique, and then converted to a delta-modulated form. The newly converted word is output (played) immediately, and the user may, via teletype commands, repeat the audio output and display its waveform. He may also elect to have a continuous audio frequency output for spectrum analysis.

The user may edit the word by trimming the ends or bisecting sections from the center of the word. In each case, the word is re-converted to a delta form according to the new editing parameters.

A CONTEXT command plays the word being processed in a context sentence without permanently storing the word on the disc. This permits the user to evaluate the pronunciation and, if necessary, to re-enter the word without taking the time to write the word on the disc. This command allows an optimization of the word pronunciations at the sentence level.

When the user completes the word processing, he may store the word on the disc by providing a word label. The physical location of the word on the disc is maintained by a directory routine that is invisible to the user. The directory routine rejects duplicate labels, but permits the user to re-write an existing word. The program can play from 1 to 15 sentences with a variable pause from 0 to 800 milliseconds between each word. An entire sentence is assembled in core prior to actual audio output. Several punctuation marks (comma, semicolon, hyphen) specify various interword pauses which may be used to enhance the sentence intelligibility.

An "endup" routine reports the number of words in the directory, alphabetizes and lists the directory on a printer, and copies the words (stored on disc in the delta format) to tape. At present, digital tape provides the audio data transfer medium from the developmental program to the 1600 computer which writes its own directory, and places the words on a disc in a very compact format as specified by a deck of address control cards which are generated by another audio production utility routine.

Conversational mode control

An executive routine receives all audio operator teletype commands, formats them, and calls one or more subroutines to perform the required services. The command structure is designed to minimize the interface complexity which the user encounters as he processes an analog word to produce the digitized delta format. Each command may be entered as a word, or the first letter of the word (i.e., WRITE or W). The numerical parameters may be one to four digits in length, and their positions may vary. For example, PAUSE 40, P 40 or P 0040 change the basic unit of pause between words to 40 milliseconds. Ease of operation is paramount in a situation where words are being evaluated, edited, and prepared for use in a learning situation.

The program can be loaded in 55k of core. This permits operation on the Spectra 70/35 or Spectra 70/45 with parallel batch operation on the 70/45. One selector channel is used for all audio input/output operations; the program can be run on a minimum configuration of central processor, one selector channel, and two disc units.

Audio data processing software

The software is designed to operate under the TDOS or DOS system in order to permit assemblies and other batch jobs to be run while the audio program is on-line. The interactive nature of digital vocabulary development requires the audio operator to make many decisions on-line; the relatively slow speed of human interaction allows batch jobs to be run at a throughput rate that makes the audio processing overhead negligible.

Register-saving linkage conventions are used to provide a smooth interaction between subroutines, and it is possible for one subroutine to call another, if additional information is required. Error messages may be issued

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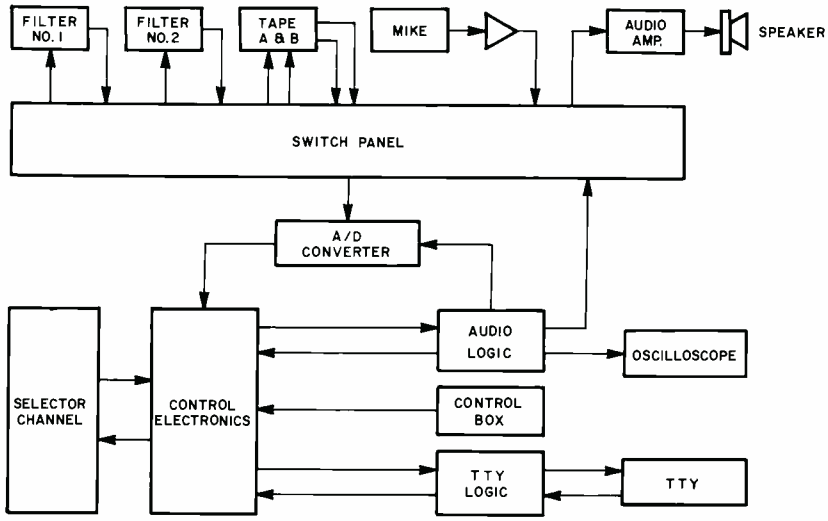


Fig. 1a—Audio data processing equipment.

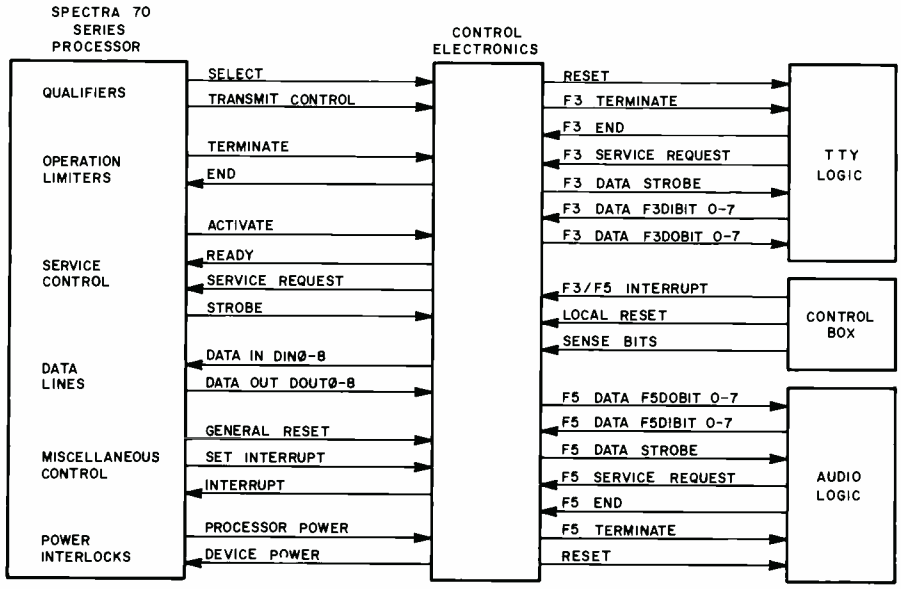


Fig. 1b—Standard Spectra I/O channel and device logic interface.

by any of the routines; the messages are in text form, and a default action is taken whenever possible.

Audio data input/output to a computer with a single selector channel in a limited core system poses a special problem during the input cycle. At this time, 30,000 bytes per second enter core via the selector channel. These bytes must be placed in core as there is no other channel to use for a simultaneous write operation. The problem is handled in this manner: a RECORD command to the executive routine calls a swap routine which transfers 50,000 bytes of program to a disc work area. The digitized audio information is placed in core during 1⅔ seconds (50,000-byte) input. Then the 50-000-byte digital audio sample is stored on the disc, and the 50,000 bytes of program are returned to core. The audio sample is read from the disc in 2,500-byte increments as the program finds the boundaries of significant amplitude audio data, and places this digital data in core. The length of the word (in milliseconds) is reported on the teletype to the audio operator.

The audio disc contains five separate directories to permit five users to maintain their own list of words. A large directory holds a maximum of 610 words while four smaller directories each hold 305 words. Each user can store words only in his directory, but he may listen to words from any directory on the disc. The words are stored one per disc track, and although optimum storage efficiency is not achieved, it is easy to change directory entries since maximum word length is limited to one disc track. Thus, there is always adequate space to store a new entry without need to justify the disc file.

A visual display of the delta-modulated word form is produced by a physical-level write command that initiates a continuous data flow over the selector channel at a high transfer rate. A software delay allows retrace time for the oscilloscope, and the write commands continue the data transfer until the audio operator terminates the display.

Archives

When a tape unit is included in the configuration, the digital sample (PCM) is stored on an archival digital tape, and the program ends by copying the delta-modulation forms to tape. The digital sample (PCM) may be read from the tape with the FIND command whenever the user wishes to begin with a copy of an original unprocessed digital word for further editing or later processing by modified delta modulation or other technique.

Audio data flow

The audio logic operates in three modes: read, write, and high-speed write (display). In the read mode, the analog input source selected by the switch panel is connected to the A/D converter. The A/D converter is driven by a 30-kHz clock to sample the analog input source. As each sample becomes available, the high-order eight bits are transferred into the processor. An encoded bandwidth of 240 kilobyte/second is necessary to accommodate the sample rate of 30 kilobyte/second with eight-bit resolution. In the write mode, a delta-modulated bit stream is transferred to the audio logic at a rate of 3.75 kilobytes/second of parallel data (the conversion from PCM to delta form is done by software as discussed later). The audio logic expands each byte to reconstruct the delta-modulation serial bit stream in real-time at a 30 kilobyte/second sample rate. The output bit stream is inte-

grated and filtered by the demodulator to produce the audio signal. In the high-speed write mode the interface transfer rate is 187.5 kilobytes/second, and the expanded bit stream is shifted at a 1.5 megabyte/second rate. This high-speed bit stream is demodulated and fed to an oscilloscope. The 1.5 megabyte/second rate provides a non-flicker display of the unfiltered audio waveform at a 50 frame/second refresh rate.

Real-time audio data interface

The data interface to a Spectra 70 series computer was designed to provide the following real-time functions: operator control of the on-line audio program and program communication with the operator via teletype, audio-data input to the processor in PCM format, audio-data output from the processor in delta modulation format for playback at the sampling rate, and audio-data output at an accelerated output rate for oscilloscope display. A secondary control of the program is available to the operator by setting the sense bits from an auxiliary control box. The sense bits may indicate an operator error, terminate the video display, or initiate the input of a spoken word from the A/D converter.

The data interface controls the teletype and digitized audio information. The teletype and the audio converters are handled as two different devices on the same controller; since their operation is mutually exclusive, no conflicts can occur. The device, and the mode of operation, are selected by the processor under program control. The primary part of the data interface logic is devoted to communicating with the selector channel by means of standard control signals. To do this, the data interface logic decodes, addresses, and mode codes to initiate the selected data transfer sequence. A block diagram of the processor-to-control-electronics interface and the control-electronics-to-device-logic interface is shown in Fig. 1. The control electronics minimize the number of signals required to transmit data between the device logic and the control electronics. A word about the interface control signals and their function will help to clarify this point.

Qualifiers and data lines

Since the data lines are used to transmit command codes, addresses, and data bytes from the processor (and addresses, status, and data bytes to the processor) the qualifiers—*transmit control* and *select* lines—determine how the information on the data lines is to be interpreted. Only the data bytes are transmitted through the control electronics to the device logic, all other signals are terminated in the control electronics.

Operation limiters

Terminate is a processor-generated signal indicating the complete transfer of a data block. This signal is passed to the device logic so that the device may indicate *end* at the completion of its operation.

Service control

Service Request is a device-generated signal indicating data is available or required by the device. *Activate* is processor initiated in response to *service request* and is terminated in the control electronics. *Strobe* is a processor signal and indicates data has been accepted and transmitted by the processor; this signal passes on to the device logic. *Ready* is generated in the control electronics and indicates status is available for the processor.

Miscellaneous control

Interrupt is a control signal indicating a device requires program service by the processor. *Interrupt* may be set locally by pushbuttons on the control box or by the processor by means of the *set interrupt* signal. *General reset* is processor generated and is used to set all devices to their quiescent state. A *local reset* is available on the control box for the same purpose.

Processor power and *device power* signals insure that both processor and device are in a power-on condition before any signals are transferred through the interface.

Sense bits can be set from the control box to indicate special servicing requirements of each device to the processor. The sequence of device selection and data flow is a programmed function selected by the operator through the interactive execution routine. Data transfer occurs in the following manner. In the read mode, the device presents the data on the DIBIT 0-7 lines and enables its *service request*. Upon acceptance by the processor, *data strobe* is sent to the device and the DIBIT lines are cleared. This sequence continues until the data buffer is exhausted and *terminate* is presented to the device: the device answers with *end* upon completion of its operation. *End* may also be initiated by the device under operator control. In the write mode, the device enables its service request indicating a need for data and the data is presented to the device on the DOBIT 0-7 lines with *data strobe*. As before, at data buffer exhaustion, the *terminate* line is enabled to the device. For a more detailed explanation of the selector-channel operation the reader is referred to RCA Standard Input/Output Interface Product Specification number C-1135.

For control and communication, the teletype operates in both a read and

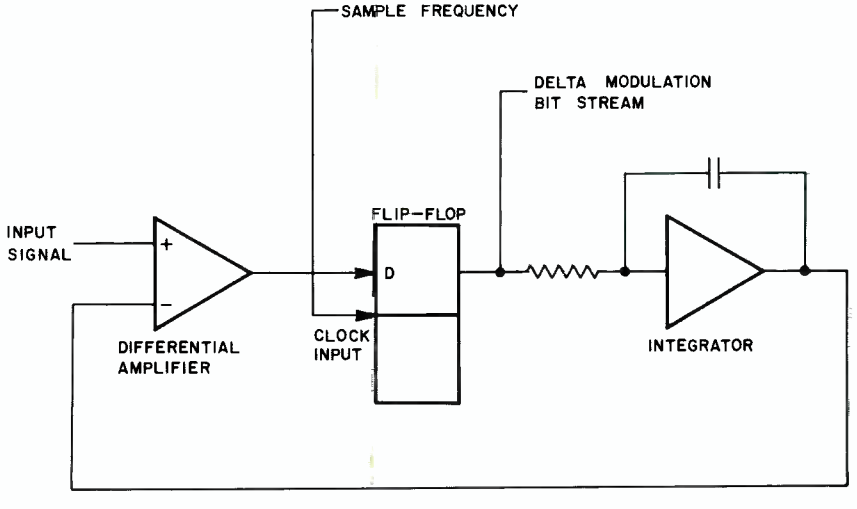


Fig. 2—Delta modulator.

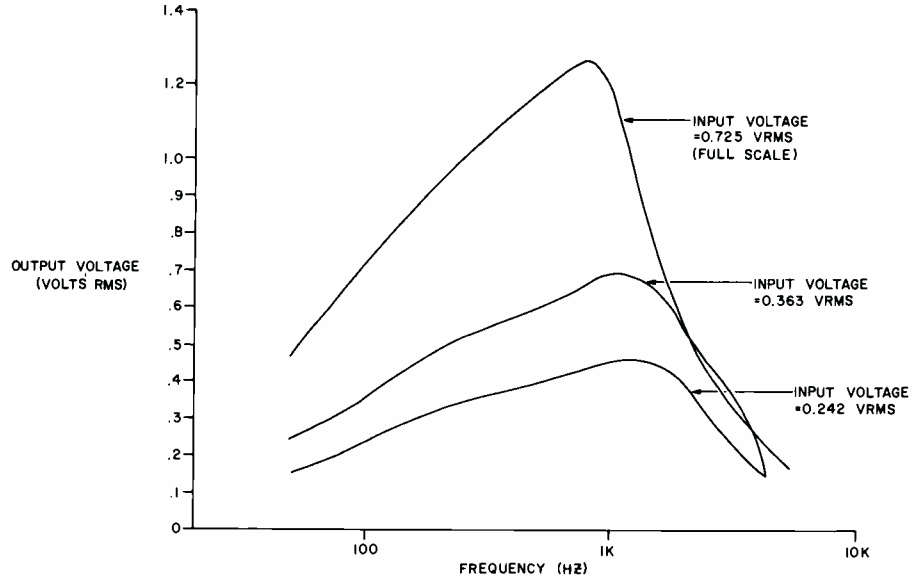


Fig. 3—Delta modulator/demodulator transfer characteristics.

write mode. Data-transfer rate for both modes is a maximum of 10 characters/second through the interface (8 bits parallel) and 110 bits/second serially to and from the teletype.

Digitizing process

The 8-bit PCM audio-data samples which have been transferred into the computer are converted to a delta-modulation form to provide for low cost demodulator hardware and flexibility to take advantage of future developments in the delta-modulation-process hardware and ease in varying bit rates and storage requirements. The delta-modulation bit stream is constructed in the processor by comparing the value of the audio waveform at the sample time to the value of a tracking integrator. The value of the integrator is adjusted to minimize the error between the sampled value and the integrator value by incrementing or decrementing the integrator value one step at each sample time. The direction of change of the integrator is determined by the comparison and the size of the step is an operator-controlled variable. The delta-modulation bit stream is a composite sequence of *ones* and *zeros*, each bit representing the sign of a comparison between the encoded audio and the integrator. A block diagram of the hardware simulated by this algorithm is shown as Fig. 2.

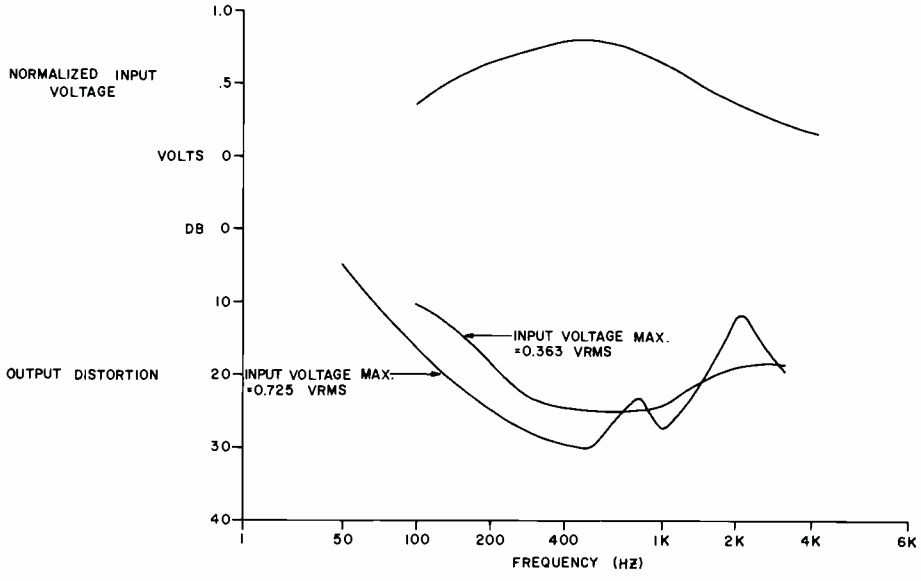


Fig. 4—Delta modulator signal and distortion.

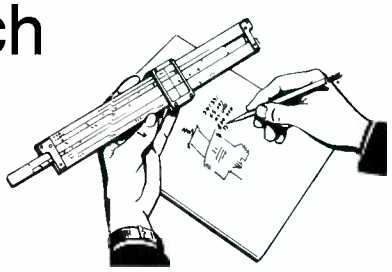
The amplitude response of the delta modulator versus frequency for a constant input amplitude is shown in Fig. 3. The low-frequency roll-off of approximately 5 dB over the decade from 1000 to 100 Hz is due to an audio low-pass filter characteristic. The high-frequency roll-off is due to a 6 dB/octave slope from the delta-modulation process which breaks at approximately 1000 Hz. Modulator slope limiting is also apparent in the 0.725-volt input signal characteristic, causing a drastic limiting of higher amplitude signals above 1000 Hz. The audio signals in the system are further limited by a low-pass filter having a 30 dB/octave roll-off at 3 kHz which is needed to reduce sampling noise. The signal distortion produced by the delta modulator in response to an average audio vocal spectrum is shown in Fig. 4. These curves show the reduced effective dynamic range due to the roll-off of natural voice spectra. The constant magnitude sampling products are therefore a larger percentage of the reduced signal. Pre-emphasis of the high frequency components is not practical because of slope limiting in the modulation process. In practice, the signals are boosted to the point of slope limiting which may account for the apparent superior intelligibility of the less complex waveforms of some female speakers using this system.

Summary

An on-line real-time data processing facility has been made to operate in conjunction with a computation facility to provide a sophisticated, interactive signal processing capability without significant degradation of the other ongoing software development activities. This is another example of a special interface which will enable a computer to be used as a unique and efficient tool which under the guidance of human supervision can accomplish tasks which would be difficult, if not impossible, using any other available technology.

This equipment demonstrates that using "off the shelf" technology, an interface can be made to couple a Spectra computer to the world of unique problems generated by the computer age.

Engineering and Research Notes



Brief Technical Papers of Current Interest

The 1600 multi-channel I/O computer

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The 1600 is a small, versatile, general-purpose processor driven with basic instructions (BI's). The BI's are like the elementary operations used in read-only memories, but BI's reside in the main core memory. Fast scratch-pad registers of integrated logic chips handle data and command manipulation and thereby increase computer speed, since main memory need not be accessed for each operation. Since the BI's reside in main memory, the macro-coding (string of BI's to perform a certain function) may be altered to adapt the 1600 to a particular application.

Most of the attached I/O devices are multiplexed; the interface from the 1600 to the device is driven predominately by programmed macro-coding and user coding. This arrangement provides maximum versatility; device addressing and transmission of strobe pulses in connection with device addressing, commands, and data are controlled by the program in main memory. This versatility is achieved at a penalty in speed, however; consequently a hardware-driven channel is available for high speed I/O devices. Data transfer is accomplished by automatic main memory cycle stealing. This arrangement saves the time required in multiplexing to access the macro-coding in main memory. Only one high-speed device may operate at a time.

This combination of versatility for multiplexed devices and high speed with the high speed I/O channel has been enhanced by the addition of two more high-speed channels (for a total of three).

The three channels are handled by hardware on a priority basis. They steal memory cycles for data transfer as with the single-channel 1600. Additional hardware registers were provided to maintain the data memory address destination and a character counter to keep track of the number of characters transferred. The two added high-speed channels required two more address registers and two more character-count registers in the IC scratch-pad registers.

The outputs of the added register chips tied to the outputs of the existing register chips form a logic "phantom OR." Register selection is now active for the previous set of registers which includes the address and byte count for channel 1, or the added set of registers which provides the address and byte count for channels 2 and 3. A new three-bit register called the *Y* register is added to the CPU. This new register is set by an added basic instruction. The register may be set to a binary value of 00, 01, 10, or 11. The value in the *Y* register determines selection of the previous set of registers or the new set. This arrangement contributes to the software compatibility of the multi-channel I/O 1600 CPU. All existing software for the single-channel 1600 CPU will function in the multi-channel I/O CPU. The *Y* register settings are used as shown in Table I.

Table I—Y register functions.

Y register value	*CPU basic instruction register select field (used to pre-load address and byte count)*	*High speed register select by device (device control electronics is plugged into one of three channel cable connectors)*
0 0	Old registers which contain address and byte count for 1st channel.	Device selects registers assigned to cable connector serving the device.
0 1	New register select for added 2nd channel.	Device selects registers assigned to cable connector serving the device.
1 0	New register select for added 3rd channel.	Device selects registers assigned to cable connector serving the device.
1 1	Select old registers for 1st channel.	Device selects 1st channel registers regardless of cable connection.

Table I shows that existing software programs written for the single-channel CPU would run in the multi-channel BPU if the *Y* register is set to 00 before the processor is started (assuming all high-speed I/O device control electronics connected to the plug for channel 1). However, a multi-channel CPU configuration could include several high-speed devices plugged into various high-speed channels. Therefore, the function for $Y=11$ was added. Now the basic instructions will still pre-load the old register set as specified by single-channel CPU software: but the various high-speed devices are forced to select the old register set as well. This allows software compatibility as described for the $Y=00$ function but does not require moving any high-speed-device connectors from their respective channels to channel-1. The function of $Y=01$ and $Y=10$ is to use the added registers for simultaneous high-speed I/O operation. These settings would never be in use when running programs written for the single-channel processor.

An additional compatibility consideration in the design of the multi-I/O CPU was the requirement that all existing device control electronics could continue to be used and without modification. In the 1600 interface from the processor to each device control electronics, a pre-set device address code $(00)_{16}$ is transmitted to inform the control electronics that a high-speed service-request response in on the interface. In the single-channel processor only, one high-speed device (such as data transfer) could be active upon detecting device address of $(00)_{16}$. Now up to three high-speed devices may be active at one time but each device control electronics is wired to recognize the same device address. This problem was resolved in the processor hardware by altering the logic gates which produce the strobe pulse for the device address. Instead of the strobe being broadcast to all channels, it is now gated to the channel which made the service request. All interface requirements were met by altering processor hardware along these lines, thus allowing continued use of all device-control electronics with either the single-channel or the multi-channel processor.

Adding the two high-speed channels to the 1600 opens the door for new applications which require simultaneous use of up to three high-speed devices (such as magnetic tapes and discs) in addition to multiplexed low speed devices.

Editor's Note: Further data on the RCA 1600 computer may be found in "Circuit concepts for the series 1600 computer" by J. W. Haney and D. B. Ayres, *RCA Engineer* Vol. 14, No. 5 (Feb/Mar 1969) Reprint RE-14-5-5; in "The Series 1600 Computer—a new solution to an old problem" by H. N. Morris, *RCA Engineer* Vol. 13, No. 6 (Apr/May 1963); and in "RCA's 1600—a versatile computer" by J. Leppold and J. Raij, *RCA Engineer, this issue.*

Author Grady Boswell at the control panel of the 1600 multi-channel I/O computer.

Method for light deflection in optical waveguides

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A novel method of producing laser light deflection and modulation has been demonstrated. The method uses simple conducting electrode patterns deposited on thin slabs or films of electro-optic crystals to produce voltage-controlled optical-phase or polarization gratings. This approach yields high diffraction efficiency and modulation depth with modest power consumption, and is readily adapted to deflect and modulate light traveling in thin-film optical waveguides.[1] In addition, a separate electrode pattern may be provided for each output light position to obtain digital control.

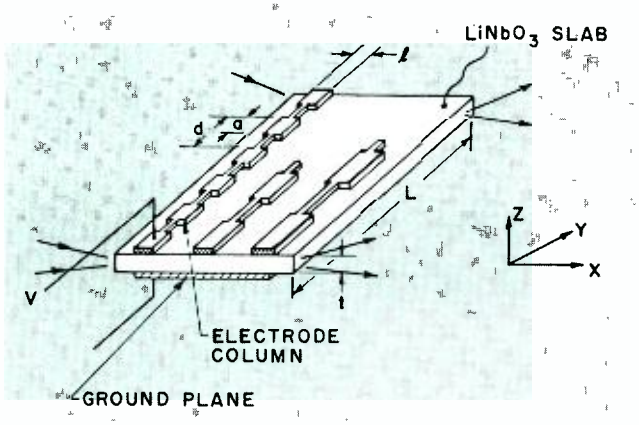

Fig. 1—Digital electro-optic grating. Three electrode columns are shown. Application of voltage to one of the columns diffracts the light parallel to the y direction. The intensities of the various diffraction orders are characteristic of the periodicity of the particular column and of the magnitude of the voltage.

The experimental arrangement is shown in Fig. 1. A z-cut [*001*] $LiNbO_3$ wafer[2] is provided with columns of electrodes on the top surface and a ground plane on the bottom. The elements of a single column are connected by a common bus. Voltage applied between a single column and the ground plane produces the grating characteristic of that column. The y-periodic electric field causes periodic variation in refractive index for a sheet of light traveling in the x direction. The z-polarization component of the light encounters a simple periodic phase change.

Thus, light is diffracted into grating orders along the y direction. The diffracted light is a sheet in the same plane as the undiffracted light.

For the case of rectangular electrodes spaced so that $a=d/2=t$ (see Fig. 1) the index variation in the y direction will be that of a "square wave" near the upper surface. Near the ground plane, the index will be uniform. In the mid plane, the index variation will approximate a sinusoidal function. By solving for the fields for each of these regions and taking a linear average of intensities, the relative far field intensity variation of the grating orders is estimated by Eq. 1:[3]

$$I/I_o=\begin{cases}[1+(J_o(\Phi))^2+(1+\cos\Phi)/2]/3; n=0\\ [(J_n(\Phi))^2+2(1-\cos\Phi)/n^2\pi^2]/3;\ n=1,3,5,\cdots\\ (J_n(\Phi))^2/3;\ n=2,4,6,\cdots\end{cases} \quad (1)$$

where Φ is the relative phase shift produced by the electro-optic effect. For a transverse linear electro-optic material with half-wave voltage $V_{\lambda/2}$ and applied voltage V,

$$\Phi=\pi\,(l/t)\ \ (V/V_{\lambda/2}) \quad (2)$$

In broadband pulse operation, it is difficult to match the load to the generator. Thus, the reactive power *(P)* is a realistic measure of the required operating power. Near optimum conditions are obtained when $\Phi=\pi$. Here $V=(t/l)\ V_{\lambda/2}$ and the reactive power may be shown to be:

$$P=\varepsilon_o\varepsilon_r(Lt/4l)\ V^2_{\lambda/2}f. \quad (3)$$

where ε_r is the relative dielectric constant; ε_o is the permitivity of space; L is the length of the optical aperture in the y direction; and f is the average pulse repetition rate. As a comparison, the voltage required to obtain N spots with a conventional isosceles electro-optic prism[4] deflector is $V_{\lambda/2}$ and the power is $\sqrt{3}/2\ \varepsilon_o\varepsilon_r tN^2V^2_{\lambda/2}f$. This represents a voltage increase by a factor of l/t over the grating. Also, the prism power requirements increase as N^2 while the grating power is independent of N.

Each angular position desired will be produced by a particular grating column. For example, the three columns shown in Fig. 1 each have a different grating space and thus provide three independent deflection angles. Similarly, N columns, each with a different grating space, would be required to obtain N positions. In order that each deflection position be resolved, the finest grating space d must be equal to or smaller than $d=L/N$ and the other spaces increased in suitable increments.

Measurements were made on an electro-optic grating with dimensions $d=3\times10^{-4}$m, $a=t=d/2$, $L=5\times10^{-3}$m, $l/t=3.67$. The gold electrodes were deposited on a z-cut $LiNbO^3$ wafer. The edges parallel to the z-y plane were optically polished. Light at 6328 Å from a *He-Ne* laser was focused through the wafer with a cylindrical lens. The emergent light was brought to a focus by a second cylindrical lens followed by a 1-m-focal-length spherical lens. A 60-Hz AC voltage was used to avoid electron trap effects.[5] Recorder plots of the intensity of the far-field pattern were obtained using a moveable 4-μ slit and detector.

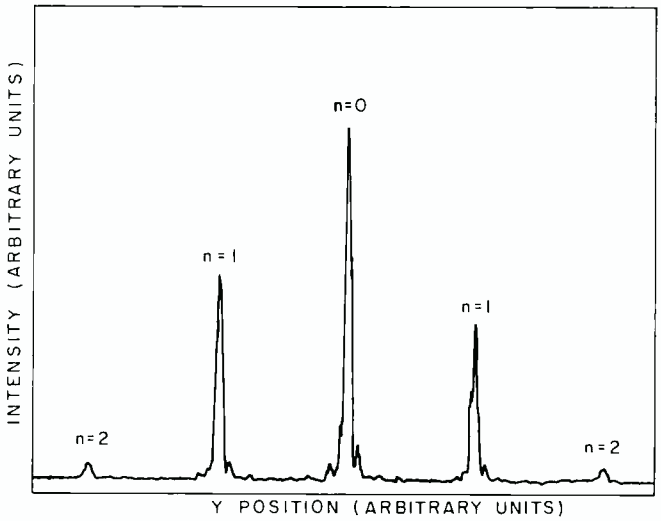

Fig. 2—Recorder tracing of the intensity of the focused far-field pattern. A 4-micron slit is moved parallel to the y direction to map out the pattern.

A typical recording is shown in Fig. 2. As would be expected from $d=L/N$, 16 spots with half widths equal to those shown can be fitted in the distance between the 0th and 1st orders. The measured and estimated (Eq. 1) intensities of the 0th, 1st, and 2nd orders are plotted against voltage in Fig. 3. There is fair agreement between the measured and estimated intensity. Approximately 17% of the incident light is placed in each lobe of the first order at 600 V. The 0th order is reduced by 60% at 600 V and 74% at 800 V.

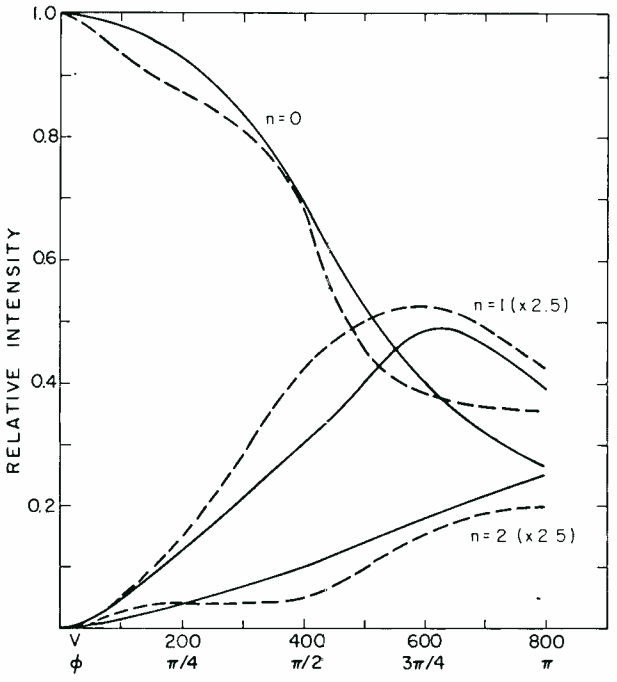

Fig. 3—Relative intensity of the orders n=0,1,2, as a function of voltage and phase shift. The phase shift is calculated[2] from Eq. 2 using $V_{\lambda/2}=2.94\times10^{3}$V. Solid line is the measured value; dashed line represents values estimated with Eq. 1.

Under pulsed operation, light pulse risetimes of less than 10 ns are observed and seem to be limited by the risetime of the applied voltage. The reactive power is calculated to be 0.73 W for 10^6 Hz average pulse repetition rate.

The digital electro-optic grating thus is useful for both light deflection and modulation. The observed 0th-order modulation depth of 64% and 1st-order intensity are limited by the fringing fields in the particular geometry studied. Reducing the thickness t to that of thin-film waveguides ($\sim$ 1 μm) would result in a lessening of the fringe fields and an approximately two orders of magnitude reduction in power. While operation of this device on a waveguide mode has not yet been experimentally shown, there is no theoretical reason to expect it to fail. In addition, the similar effect of diffraction of waveguide modes by acoustic waves has been shown.[6]

If the length l (in the x direction) is increased, a thick grating mode of operation is obtained. Here 100% of the light may be diffracted into 1st order by operating in a Bragg regime while the power required is reduced by a factor proportional to t/l.

Thus, a new method of laser light deflection and modulation based on diffraction by electro-optic phase gratings has been demonstrated. The method appears to be applicable to both plane-wave and thin-film-waveguide transmission, requires relatively little power for high speed operation, and is capable of high diffraction efficiency.

Acknowledgment

The author wishes to thank J. Minville for assistance in preparing the gratings.

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Self-peeling evaporated metal mask used in vacuum deposition work

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At times, it is desirable to deposit a particular metal on an insulating or semiconducting substrate without having to etch the metal to define the desired circuit pattern. Masks used for doing this have been: a) *mechanical masks*, whch have the advantage of withstanding high substrate temperatures yet the disadvantage of poor fine-pattern definition; and b) *photoresist masks*, which have the advantage of fine-pattern definition but are limited in temperature and can possibly contaminate a vacuum system. The metal mask described below has both advantages: fine pattern definition and broad substrate temperature capabilities.

This mask is fabricated by evaporating 1.0 micron of a non-adhering metal such as gold or copper on a substrate which is at room temperature. This results in a metal-substrate bond that can be peeled off—somewhat like tape off a piece of glass. The metal is then treated with a photosensitive material and, by using a photolithographic mask, a pattern is exposed by an appropriate light source. The pattern is developed (Fig. 1) and the exposed metal is etched away. The photoresist material is washed off and the exposed pattern of the substrate is thoroughly cleaned for the next evaporation.

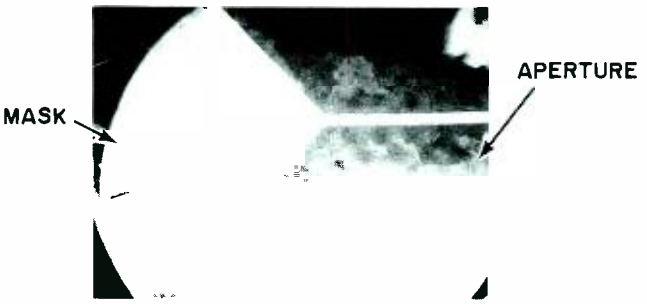

Fig. 1—Photograph of 1-μm-thick gold mask with aperture viewed on scotch tape after peeling.

For the second evaporation, standard techniques for good adhesion are used. For our sample, the substrate was heated to 300° C and a flash of chromium (250 Å) followed by 0.5 micron of gold was evaporated through the apertures etched in the mask. The substrate was removed from the vacuum system and the metal mask was peeled off leaving the desired pattern (Fig. 2).

Results

This technique has successfully been used to fabricate a 3dB directional coupler on a saphire substrate. In Fig. 2, a detailed portion of the coupler is shown to display the line definition possible using this technique.

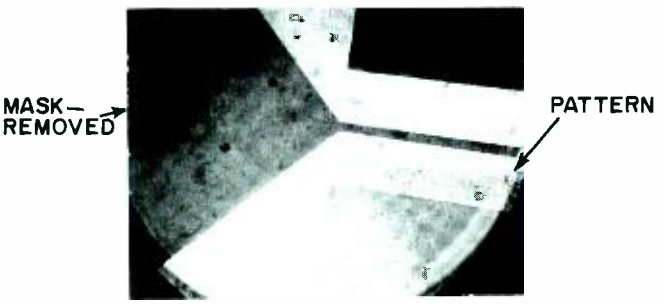

Fig. 2—Desired pattern with mask peeled off.

Pen and Podium

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. . . printing, photography, & typesetting, writing, editing, & publishing; information storage, retrieval, & library science; reprography & microstorage
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IDEOGRAPHIC PHOTOCOMPOSING Machine—W. F. Heagerty (ATL, Cam) Joint Seminar on Input/Output Systems for Japanese and Chinese Characters, Tokyo, Japan; 1/20-22/71

Author Index

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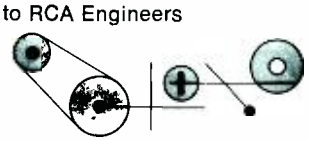

As reported by RCA Domestic Patents, Princeton

Astro-Electronics Division

Sailing Vessel—E. W. Schlieben (AED, Pr) U.S. Pat. 3,556,035; January 19, 1971

Gas Environment for Recorder-Reproducer Systems—L. J. Baun (AED, Pr) U.S. Pat. 3,569,637; March 9, 1971

Method of Erasing Target Material of a Vidicon Tube or the Like and Means Therefor—J. J. Hawley (AED, Pr) U.S. Pat. 3,431,460; March 4, 1969; Assigned to U.S. Government

Second Surface Mirrors for Solar Cell Array—R. R. Scott (AED, Pr) U.S. Pat. 3,532,551; October 6, 1971; Assigned to U.S. Government

Maximum Power Point Tracker—A. S. Cherdak (AED, Pr) U.S. Pat. 3,566,132 February 23, 1971; Assigned to U.S. Government

Aerospace Systems Division

RFI-Protected Flip-Flop—F. C. Hassett (ASD, Burl) U.S. Pat. 3,553,485; January 5, 1971

Computer Systems

Discontinuity Detector—J. P. Watson (CS, Marl) U.S. Pat. 3,566,084; February 23, 1971

Servo System Including Differential and Unbalance Amplifiers—D. W. Hall, II (CS, PBG) U.S. Pat. 3,566,295; February 23, 1971

Feedback Type Oscillator with Input Stabilizing Means—D. W. Hall, II (CS, PBG) U.S. Pat. 3,562,699; February 9, 1971

Reduction of Tape Stiction—J. P. Watson (CS, PBG) U.S. Pat. 3,568,907; March 9, 1971

Consumer Electronics

Television Integrated IF Amplifier Circuits—J. Avins (CE, Som) U.S. Pat. 3,564,125; February 16, 1971

Signal Translating Circuit Having First and Second Pairs of Semiconductor Devices with Matching Conduction Characteristics—A. L. Limberg (CE, Som) U.S. Pat. 3,564,438; February 16, 1971

Direct Coupled AM Detector—J. R. Harford (CE, Som) U.S. Pat. 3,560,865; February 2, 1971

Corner Edge Connector For Printed Circuit Boards—J. D. Ammerman (CE, Ind) U.S. Pat. 3,567,998; March 2, 1971

Color Subcarrier Oscillators—J. M. Kresock (CE, Ind) U.S. Pat. 3,569,613; March 9, 1971

Signal Translating System Providing Amplification and Limiting—J. Avins (CE, Som) U.S. Pat. 3,569,773; March 9, 1971

Electronic Components

Method of Mounting a Heater in a Tubular Cathode—C. L. Lundvall (EC, Lanc) U.S. Pat. 3,555,640; January 19, 1971

Method of Treating Semiconductor Devices—A. Mayer (EC, Som) U.S. Pat. 3,551,997; January 5, 1971

Methods for Electroless Plating and for Brazing—R. W. Etter (EC, Lanc) U.S. Pat. 3,551,997; January 5, 1971

Semiconductor Rectifiers Having Controlled Storage and Recovery Characteristics—J. M. S. Neilson (EC, Mtp) U.S. Pat. 3,553,536; January 5, 1971

Method for Producing a Graphic Image—E. E. Mayaud (EC, Lanc) U.S. Pat. 3,558,310; January 26, 1971

Beam Landing Error Control Apparatus for Magnetically Focussed Cathode Ray Tubes—R. A. Minet (EC, Lanc) U.S. Pat. 3,558,953; January 26, 1971

Color Tube Having Ground Plane Between Focus Electrodes and Screen Grids—C. E. Lilley (EC, Lanc) U. S. Pat. 3,558,954; January 26, 1971

Superconductive Magnet Construction—H. C. Schindler (EC, Hr) U.S. Pat. 3,559,127; January 26, 1971

Superconductive Magnet and Method of Constructing Same—E. R. Schrader (EC, Hr) U.S. Pat. 3,559,130; January 26, 1971

Display Device Including a Point Image—R. A. Bonnette, N. L. Lindburg (EC, Som) U.S. Pat. 3,564,325; February 16, 1971

High Input Impedance Amplifier—S. L. Knanishu (EC, Hr) U.S. Pat. 3,564,436; February 16, 1971

Shadow Mask Type Color Picture Tube with a Fine Mesh Flexible Particle Shield Between the Gun and Target Portions—H. L. May (EC, Som) U.S. Pat. 3,560,779 February 2, 1971

Integral Pulse Switching Systems—G. D. Hanchett (EC, Som) U.S. Pat. RE27072; February 23, 1971

Adhesive Mounting Means for a Cathode Ray Tube-Yoke Combination—M. G. Brown, Jr. (EC, Lanc) U.S. Pat. 3,566,321; February 23, 1971,

Semiconductor Device—R. J. Satriano (EC, Hr) U.S. Pat. 3,562,404; February 9, 1971

Memory Protecting Circuit—R. W. Ahrons (EC, Som) U.S. Pat. 3,562,555; February 9, 1971

Semiconductor Mounting Adapter—R. S. Berger (EC, Som) U.S. Pat. 3,568,761; March 9, 1971

Heat Pipe—W. E. Harbaugh (EC, Lanc) U.S. Pat. 3,568,762; March 9, 1971

Double Heat Sink Semiconductor Device—R. Amantea, H. W. Becke, P. J. Del Priore (EC, Raritan) U.S. Pat. 3,569,798; March 9, 1971

Temperature-Compensated Frequency-Voltage Linearizing Circuit—R. L. Ernst (EC, Pr) U.S. Pat. 3,569,867; March 9, 1971

Communications Systems Division

Phase Lock Loop—E. D. Menkes (CSD, Cam) U.S. Pat. 3,571,743; March 23, 1971

Optical Compensating Filter with Selective Absorption Distribution—K. C. Hudson (CSD, Cam) U.S. Pat. 3,558,208; January 26, 1971

Matrixing Apparatus—J. F. Monahan, R. A. Dischert (CSD, Cam) U.S. Pat. 3,558,806; January 26, 1971

Video Signal Switching Step Suppressor—A. J. Banks (CSD, Cam) U.S. Pat. 3,558,815; January 26, 1971

Pulse Width Modulated Solid State Regulated Power Supply—D. C. Bussard (GCS, Cam) U.S. Pat. 3,559,097; January 26, 1971

Coaxial Transmission Line—A. N. Schmitz (CSD, Cam) U.S. Pat. 3,564,108; February 16, 1971

Sync Regenerator—R. N. Hurst (CSD, Cam) U.S. Pat. 3,564,141; February 16, 1971

Tape Lifter—C. R. Horton (CSD, Cam) U.S. Pat. 3,564,158; February 16, 1971

Compensated Readback Circuit—G. V. Jacoby, J. D. Gleitman (CSD, Cam) U.S. Pat. 3,568,174; March 2, 1971

Current Regulator Utilizing a Floating Reference Voltage Supply—H. G. Seer, Jr., (CSD, Cam) U.S. Pat. 3,566,246; February 23, 1971

Multi-Processor Multi-Programed Computer System—A. T. Ling (CSD, Cam) U.S. Pat. 3,566,357; February 23, 1971

Automatic Video Signal Gain Controlling Apparatus—L. J. Baun (CSD, Cam) U.S. Pat. 3,569,620; March 9, 1971

Unit Distance Counter—F. H. Fowler (CSD, Cam) U.S. Pat. 3,562,551; February 9, 1971

Laboratories

Method of Treating Semiconductor Devices to Improve Lifetime—F. P. Heiman, P. H. Robinson (Labs, Pr) U.S. Pat. 3,556,880; January 19, 1971

Plasma Anodizing Aluminum Coatings on a Semiconductor—A. Waxman, K. H. Zaininger (Labs, Pr) U.S. Pat. 3,556,966; January 19, 1971

Vehicle Road Guidance System—G. W. Gray (Labs, Pr) U.S. Pat. 3,556,244; January 19, 1971

Photochromic Light Valve—Z. J. Kiss (Labs, Pr) U.S. Pat. 3,552,824; January 5, 1971

Bulk Semiconductor Light Radiating Device—S. G. Liu, K. K. N. Chang (Labs, Pr) U.S. Pat. 3,558,889; January 26, 1971

High Power, High Efficiency Silicon Avalanche Diode UHF and L Band Oscillator—H. J. Prager, S. Weisbrod, K. K. N. Chang (Labs, Pr) U.S. Pat. 3,559,097; January 26, 1971

Electronic Photocopy System—H. N. Crooks, R. L. Hallows, Jr. (Labs, Pr) U.S. Pat. 3,564,130; February 16, 1971

Spatially Modulated Halftone Dot Image Generation System—E. W. Herold, K. H. Fischbeck (Labs, Pr) U.S. Pat. 3,564,131; February 16, 1971

Integrated Display Panel Utilizing Field-Effect Transistors—P. K. Weimer (Labs, Pr) U.S. Pat. 3,564,135; February 16, 1971

Fabricating Semiconductor Devices—H. Kressel, F. Z. Hawrylo (Labs, Pr) U.S. Pat. 3,560,275; February 2, 1971

Electroetching of a Conductive Film on an Insulating Substrate—J. M. Shaw (Labs, Pr) U.S. Pat. 3,560,357; February 2, 1971

Gaseous Electric Discharge Tube Including a Plurality of Pucturable Gas Storage Cells—K. G. Hernqvist, J. R. Fendley, Jr. (Labs, Pr) U.S. Pat. 3,560,789; February 2, 1971

Directional Filter Comprising a Resonant Loop Coupled to a Transmission Line Pair—L. S. Napoli, J. J. Hugher (Labs, Pr) U.S. Pat. 3,560,887; February 2, 1971

Surface Strip Transmission Line and Microwave Devices Using Same—C. P. Wen (Labs, Pr) U.S. Pat. 3,560,893; February 2, 1971

Depositing Successive Epitaxial Semiconductive Layers From the Liquid Phase—H. Nelson (Labs, Pr) U.S. Pat. 3,565,702; February 23, 1971

Electrostatc Charging Apparatus with Means to Blow Elecrostatic Charge onto a Photoconductive Surface from a Remotely Located Corona Generator—R. G. Olden, H. C. Gillespie (Labs, Pr) U.S. Pat. 3,566,110; February 23, 1971

Light Deflection System—G. W. Taylor, A. R. Sass (Labs, Pr) U.S. Pat. 3,566,172; February 23, 1971

Microwave Oscillator Including Two Bulk Negative Resistance Devices in a Three-Terminal Cavity—R. D. Larrabee (Labs, Pr) U.S. Pat. 3,562,665; February 9, 1971

Correction of Block Errors in a Transmission of Data—C. V. Spinivasan (Labs, Pr) U.S. Pat. 3,562,709; February 9, 1971

Transcendental Function Generator—H. S. Miller, R. J. Linhardt (Labs, Pr) U.S. Pat. 3,562,714; February 9, 1971

Switching Mode Control Circuits—P. S. Carnt (Labs, Zurich) U.S. Pat. 3,553,357; January 5, 1971

Monitoring of PAL Signal Waveforms—P. S. Carnt, T. E. Bart (Labs, Zurich) U.S. Pat. 3,567,862; March 2, 1971

Nonreciprocal Microwave Devices Using a Semiconductor Element—K. Suzuki, R. Hirota (Labs, Japan) U.S. Pat. 3,569,868; March 9, 1971

Electromagnetic and Aviation Systems Division

Microsensing Network—F. C. Easter (EASD, Van Nuys) U.S. Pat. 3,553,500; January 5, 1971

De-Soldering Apparatus—J. B. Jones (EASD, Van Nuys) U.S. Pat. 3,557,430; January 26, 1971

Agitation Sensitive Alarm Circuit—J. R. Hall, P. B. Korda (EASD, Van Nuys) U.S. Pat. 3,559,203; January 26, 1971

Automatic Return-To-Center Deflection Circuit—G. F. Carroll (EASD, Van Nuys) U.S. Pat. 3,569,773; March 9, 1971

RCA Limited

Antenna Comprising Restraining Means for Resilient Support Members—T. Szirtes (Ltd, Mont) U.S. Pat. 3,553,731; January 5, 1971

Feed System—P. Foldes (Ltd, Mont) U.S. Pat. 3,560,976; February 2, 1971

RCA Service Company

Apparatus for Inspecting Microfilm—E. L. Klein (SvCo, Ala) U.S. Pat. 3,563,668; February 16, 1971; Assigned to U.S. Government

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Professional Meetings

Dates and *Deadlines

Be sure deadlines are met—consult your Technical Publications Administrator or your Editorial Representative for the lead time necessary to obtain RCA approvals (and government approvals, if applicable). Remember, abstracts and manuscripts must be so approved BEFORE sending them to the meeting committee.

Calls For Papers

SEPT. 19-23, 1971: **Joint Power Generation Technical Conference,** Chase Park Plaza Hotel, St. Louis, Missouri; IEEE Power Engrg. Society, ASME, ASCE. **Deadline Info: 5/7/71 (Ms) to:** R. L. Colt, Westinghouse Elec. Corp., Lester P.O., Philadelphia, Pa. 11913.

OCT. 25-29, 1971: **Jt. National Conference on Major Systems;** Disneyland Hotel, Anaheim, California; G-SMC, ORSA; **Deadline Info: 2/1/71 (Abst) 6/15/71 (Papers) to:** J. E. Olivares, Jr., Sysdyne Inc., 6911 Topanga Canyon Blvd., Canoga Park, Cal. 91303.

OCT. 30-NOV. 3, 1971: "Wonderful World of Ceramics"; American Ceramic Society, Disneyland Hotel, Anaheim, California; **Deadline Info: 6/1/71 (Papers) to:** Sydney Z. Gendel, Amtec Industries, Inc., 13313 E. Alondra Blvd., Santa Fe Springs, Calif. 90670.

OCT. 31-NOV. 4, 1971: **Engineering in Medicine & Biology Conference;** International Hotel, Las Vegas, Nevada; G-EMB, AEMB; **Deadline Info: 6/18/71 (Papers) to:** John Hanley, Brain Res. Inst., Univ. of Calif., Los Angeles, Calif. 90024.

NOV. 8-10, 1971: **Jt. Conference on Sensing of Environmental Pollutants;** Cabana Hyatt House, Palo Alto, Calif.; IEEE Committee on Environmental Quality et al; **Deadline Info: 5/14/71 (Papers or Absts) to:** Dr. Robert L. Chapman, Beckman Instrument Company, 2500 Harbor Boulevard, Fullerton, California.

NOV. 15-17, 1971: **2nd Symposium on Uranium Plasmas: Research and Applications;** Atlanta, Georgia; AIAA (Host Society), NASA, and Georgia Institute of Technology; **Deadline Info: 5/14/71 (Abst) to:** J. Richard Williams, Nuclear Engineering Dept., Georgia Institute of Technology, Atlanta, Ga. 30332.

DEC. 6-9, 1971: **Ultrasonics Symposium;** Carillon Hotel, Miami Beach, Florida; G-SU; **Deadline Info: 9/1/71 (Abst.) to:** Herbert Matthews, Sperry Rand Res. Ctr., Sudbury, Mass. 01776.

DEC. 7-8, 1971: **Vehicular Technology Conference;** Sheraton Cadillac Hotel, Detroit, Michigan; G-VT; **Deadline Info: 6/15/71 (Sum.) to:** A. E. Marshall, Ford Motor Co., 23400 Michigan Ave., Dearborn, Michigan.

JAN 30-FEB 4, 1972: **IEEE Power Engineering Society Winter Meeting;** Statler Hilton Hotel, New York, N.Y.; IEEE Power Engineering Society; **Deadline Info: 9/15/71 (Papers)** IEEE Office, 345 E. 47th St. New York, N.Y. 10017.

APRIL 11-13, 1972: **Conf. on Industrial Measurement & Control by Radiation Techniques;** Univ. of Surrey, Guilford, Surrey, England; IEE, IERE, IPPS, IMC, IEEE UKRI Section et al; **Deadline Info: 6/21/71 (Syn) 11/8/71 (Ms) to:** IEE Office, 2 Savoy Place, London W.C. 2, England.

Meetings

JUNE 1-3, 1971: **Electrical & Electronic Measurement & Test Instrument Conference (EEMTIC);** Skyline Hotel, Ottawa, Ontario, Canada; G-IM, Ottawa Section; **Prog. Info:** F. L. Hermach, B-162 Metrology Bldg., NBS, Washington, D. C. 20234.

JUNE 2-4, 1971: **Conference on Laser Engineering & Applications;** Washington Hilton Hotel, Washington, D.C.; IEEE Quantum Elec. Council, OSA; **Prog. Info:** D. E. Caddes, Sylvania Elec. Sys. Electro-Optics Organ., Mountain View, Calif. 94040.

JUNE 7-8, 1971: **Chicago Spring Conf. on Broadcast & TV Receivers;** Marriott Motor Hotel, Chicago, Illinois; G-BTR, Chicago Section; **Prog. Info:** Donald Ruby, Zenith Radio Corp., 6001 W. Dickens Ave., Chicago, Ill. 60639.

JUNE 7-8, 1971: **Symposium on Applications of Ferro-electrics;** IBM Res. Ctr., Yorktown Heights, N.Y. & Holiday Inn, White Plains, N.Y., G-SU; **Prog. Info:** L. E. Cross, Penn State Univ., State College, Penna. 16802.

JUNE 8-10, 1971: **Conference on Aerospace Antennas,** London, England; IEE, IERE, IEEE UKRI Section, **Prog. Info:** IEE Office, 2 Savoy Place, London W.C. 2, England.

JUNE 12-17, 1971: **American Automatic Control Council,** Paris, France, **Prog Info:** American Institute of Aeronautics and Astronautics, 1290 Avenue of the Americas, New York, N.Y. 10019.

JUNE 14-16, 1971: **International Conference on Communications;** Queen Elizabeth Hotel, Montreal, Quebec, Canada; G-Com Tech, Montreal, Section, **Prog. Info:** W. C. Benger, Northern Elec. Co. Ltd., POB 3511, Station C, Ottawa 3, Ontario, Canada.

JUNE 14-18, 1971: **AIAA 7th Propulsion Joint Specialist Conference;** Salt Lake City, Utah; **Prog. Info:** American Institute of Aeronautics and Astronautics, 1290 Avenue of the Americas, New York, N.Y. 10019.

JUNE 19-20, 1971: **AIAA Professional Study Seminar on Environmental Fluid Dynamics,** conducted by Dr. James A. Fay, Professor of Mechanical Engineering, Massachusetts Institute of Technology, Cambridge, Mass; **Prog. Info:** American Institute of Aeronautics and Astronautics, 1290 Avenue of the Americas, New York, N.Y. 10019.

JUNE 21-23, 1971: **AIAA 4th Fluid and Plasma Dynamics Conference;** Palo Alto, Calif.; **Prog. Info:** American Institute of Aeronautics and Astronautics, 1290 Avenue of the Americas, New York, N.Y. 10019.

JUNE 21-23, 1971: **Int'l. Congress on Instrumentation in Aerospace Simulation Facilities;** Von Karman Inst. of Fluid Dynamics, Genese, Belgium, G-AES; **Prog. Info:** IEEE, Office of: Technical Activities Board, 345 East 47th Street, New York, N.Y. 10017.

JUNE 28-30, 1971: **Design Automation Workshop;** Shelburne Hotel, Atlantic City, New Jersey; IEEE Computer Society, ACM, SHARE, **Prog. Info:** R. B. Hitchcock, Sr., IBM, Box 218, Yorktown Hgts., N.Y. 10598.

JUNE 28-30, 1971: **10th Reliability and Maintainability Conference;** Anaheim, Calif.; **Prog. Info:** American Institute of Aeronautics and Astronautics, 1290 Avenue of the Americas, New York, N.Y. 10019.

JULY 5-8, 1971: **8th International Shock Tube Symposium;** London England; **Prog. Info:** American Institute of Aeronautics and Astronautics, 1290 Avenue of the Americas, New York, N.Y. 10019.

JULY 7-9, 1971: **12th Anglo-American Aeronautical Conference;** Calgary, Canada; **Prog. Info:** American Institute of Aeronautics and Astronautics, 1290 Avenue of the Americas, New York, N.Y. 10019.

Engineering News and Highlights

V. Orville Wright appointed President, Systems Development Division

V. Orville Wright has been appointed President of the Systems Development Division, a major operating unit within RCA Computer Systems. In this post, he is responsible for the design and development of RCA computer systems.

Mr. Wright joined RCA on April 20, 1970, as Division Vice President, Government Marketing, of the former Computer Systems Division and directed the marketing of RCA computer systems to federal, state and local government agencies.

Prior to joining RCA, Mr. Wright was Group Director of Systems and Technology with IBM's Government, Education and Medical Group and held various sales and technical management positions. Mr. Wright received the BS in Government from the University of Kansas. He served 14 years with the U.S. Navy through World War II and the Korean War and attained rank of Commander.

Beeby appointed Division V.P. Technical Operations, Systems Development Division

V. Orville Wright, President of the Systems Development Division appointed **Patrick A. Beeby,** Division Vice President of Technical Operations.

In his new post, Mr. Beeby is responsible for the computer product laboratories in Marlboro, Mass., and Palm Beach Gardens, Fla., and the systems programming laboratory in Cinnaminson, N.J. These operations provide engineering and support services for hardware and software development.

Prior to joining RCA, Mr. Beeby spent 20 years with IBM in various product development and engineering positions, most recently as Systems Manager, Recognition Systems, IBM Systems Development Division.

Mr. Beebe received the BSEE and the BS in Business Administration from Kansas State University.

Alperin appointed Manager, Small Systems

Norman N. Alperin has been appointed Manager, Small Systems, at the Computer Systems plant at Palm Beach Gardens, Florida. Mr. Alperin reports to **V. Orville Wright,** President, Systems Development Division, Computer Systems.

Mr. Alperin received the BEE (Magna Cum Laude) from Syracuse University in 1952 and the SMEE from Massachusetts Institute of Technology in 1956. After graduating from Syracuse, he served as a staff member of the MIT Digital Computer Laboratory. There he participated in the logic design, development, and fabrication of computer terminal equipment until 1956 when he joined RCA Missile and Surface Radar Division. At M&SR he served successively as project engineer; Manager, Information Processing Systems Engineering; and Manager, Advanced Programs. From 1964 to 1967, he was with Ultronic Systems Corp. in Mt. Laurel, N.J. as Manager, New Products. He rejoined RCA in 1967 as Manager, Product Development, in the Instructional Systems Engineering Department at Palo Alto, California. In 1969, Mr. Alperin became Manager, Technical Operations, with engineering and software responsibilities for the division. With the merger of Instructional Systems into Computer Systems, he became Manager, Systems Programming Development. Mr. Alperin is a member of Tau Beta Pi, Eta Kappa Nu, Sigma Pi Sigma, Pi Mu Epsilon, and Sigma Xi honoraries and also a member of the ACM. He holds one U.S. patent.

RCA microwave symposium

About 200 scientists, engineers, and supervisory personnel from all areas of the Corporation participated in a two-day session covering microwave solid-state devices, technologies, subsystems and systems. The symposium was held at the David Sarnoff Research Center and was organized by **H. K. Jenny,** General Microwave Symposium Chairman, and **Dr. H. Sobol,** member of Corporate Staff responsible for microwave technology.

State of the art and corporate effort in the field was reviewed; several work sessions allowed discussion of problems in key areas. Demonstrations of advanced technologies by Princeton-based microwave activities concluded a very productive development of new contacts and interchange of knowhow. Follow-up effort in several areas of technology is underway. Summaries of the papers associated with the symposium were distributed after the meeting.

For additional information, contact H. K. Jenny, Harrison, or Dr. H. Sobol, Princeton.

Degrees granted

J. C. Beck, CE, Ind ..... MSEE, Purdue Univ; 1/71
A. Kleiman, AED, Pr ..... MSEE, Stevens Inst. of Tech; 2/71
P. C. Olsen, CE, Ind ..... MSEE, Purdue Univ; 1/71
J. C. Peer, CE, Ind ..... MSEE, Purdue Univ; 1/71

Staff Announcements

Government and Commercial Systems

Dr. Harry J. Woll, Chief Government Engineer for RCA's Government and Commercial Systems, has appointed **Safford K. Magee,** Manager, Central Engineering; and **Richard C. Willman,** Manager, Technical Planning.

S. N. Lev, Division Vice President of Manufacturing, has appointed **Arthur W. Camp,** as Manager, Facilities and Plant Engineering.

Nicholas F. Pensiero, Manager, Government Marketing Services and Public Affairs, has appointed **Edward J. Dudley,** Manager of News and Information for RCA Government and Commercial Systems.

George D. Prestwich, Division Vice President, Government Marketing, RCA Government and Commercial Systems, has appointed **Oliver M. Read,** as Manager, Proposals and Marketing Resources Development.

William V. Goodwin, RCA Division Vice President, Aegis Program, has announced the appointment of **Dan L. Cahill,** Manager, Technical Planning Liaison.

Electromagnetic and Aviation Systems Division

Frederick H. Krantz, Division Vice President and General Manager, has announced the organization of the Electromagnetic and Aviation Systems Division as follows: **Ramon H. Aires,** Chief Engineer, Engineering Dept.; **Milford E. Collins,** Manager, Product Assurance; **James F. Gates,** Acting Manager, Program Operations; **Frederick H. Krantz,** Acting Manager, Advanced Programs; **Joseph F. McCaddon,** Division Vice President, Aviation Equipment Department; **W. Robert McKinley,** Manager, Business Planning; **Neil A. Montone,** Manager, Marketing Department; **Robert B. Moses,** Manager, Operations Control; **Robert W. Stephens,** Manager, West Coast Personnel; and **Benjamin W. Tucker,** Plant Manager, Van Nuys Plant.

Communications Systems Division

James M. Osborne, Division Vice President, has announced the appointment of **Francis H. Stelter, Jr.,** Manager, Marketing; **Thomas R. Sheridan,** Manager, Data Communications Systems; **John D. Rittenhouse,** Manager, Radio and Transmission Systems; **Edmund J. Westcott,** Manager, Product Assurance; and **Robert S. Miller,** Manager, Contracts Management.

Research and Engineering

Dr. James Hillier, Executive Vice President, Research and Engineering, has announced the appointment of **J. F. Biewener,** as Director, Finance and Administrative Services. His organization is announced as follows: **J. F. Biewener,** Acting Manager, Management Information Systems; **V. M. Bartholomew,** Manager, Graphics Services; **Eric M. James,** Manager, Facilities; **Carl E. Kurlander,** Manager, Materials; **Donald J. McCarty, Jr.,** Manager, Accounting; and **Ralph H. Myers,** Manager, Financial and Capital Planning.

Howard Rosenthal, Director, Engineering, has appointed **Arnold S. Farber,** Staff Engineer, Engineering.

RCA Laboratories

William M. Webster, Vice President, Laboratories, has announced the organization of the Laboratories as follows: **Jan A. Rajchman,** Staff Vice President, Information Sciences; **Fred D. Rosi,** Staff Vice President, Materials and Device Research; **Thomas O. Stanley,** Staff Vice President, Systems and Research; **Allen A. Barco,** Staff Advisor; **Harry L. Cooke,** Manager, Information Services and Technical Relations; **Charles A. Hurford,** Manager, Personnel; **Jerome Kurshan,** Manager, Marketing; **Albert Pinsky,** Administrator, Scientific Information Services; and **Richard E. Quinn,** Manager, Technical Services.

Donald S. McCoy, Director, Consumer Electronics Research, has announced the organization of the Consumer Electronics Research Laboratory as follows: **Jay J. Brandinger,** Head, TV Systems Research; **H. Nelson Crooks,** Manager, High Density Recording Project; **William J. Hannan,** Head, Electro-optic Systems Research; **William D. Houghton,** Head, Consumer Information Systems Research; **James J. Gibson,** Fellow, Technical Staff; **Eugene O. Keizer,** Head, Video Systems Research; **John A. van Raalte,** Head, Displays and Device Concepts Research.

Corporate Engineering Services

A. Robert Trudel, Director, Corporate Engineering Services, has announced the appointment of **Harry Kleinberg,** Manager, Corporate Standards Engineering.

Astro-Electronics Division

Warren P. Manger, Chief Engineer, has announced the appointment of **Bertram Walker,** Manager, Microelectronics Technology.

International Development and Glass Operations

Alan M. Trax, Manager, Engineering, has appointed **Bruce N. Becker,** as Manager, Production Engineering.

Industrial Tube Division

C. Price Smith, Manager, Power & Electro-Optics Products Dept., has announced the organization of the Engineering Services Activity as follows: **Horace A. Kauffman,** Manager, Engineering Services; **Fred L. Dings,** Manager, Equipment Maintenance and Construction; **John B. Grosh,** Engineering Leader (Environmental Laboratory); **James C. Ottos,** Engineering Leader (Equipment Engineering).

Kihn named to Licensing Staff

Dr. George H. Brown, Executive Vice President, Patents and Licensing, has appointed **Harry Kihn,** Staff Technical Advisor, Domestic Licensing, reporting to **Jerold J. Benavie,** Staff Vice President, Domestic Licensing. In this capacity, Mr. Kihn covers the entire spectrum of RCA interests and provides guidance for both Domestic and International Licensing in the selection of RCA-developed products which can be licensed advantageously. He also provides technical guidance in all areas of the licensing activity.

Harry Kihn holding a liquid crystal display —one of the products that is being examined for possible licensing.

Harry Kihn received the BSEE from the Cooper Union and the MSEE from U. of Pa. He joined RCA in 1939 and transferred to Princeton with the formation of the RCA Laboratories where he engaged in research on X-band receivers, crystal detectors, FM and doppler radar, automatic bombing devices, altimeters, television receiver circuitry, air navigation systems, and television data transmission systems. With the advent of color TV, he engaged in the development of the compatible color system and the design and operation of color receivers for FCC demonstrations. In 1953, he transferred to the Systems Research Laboratory where he was responsible for a wide variety of systems research programs. While in the Laboratories he won two awards for unique technical developments and a commendation for work in color TV. He has 23 issued patents and has authored numerous papers. From 1960 to 1970, he was a member of the Corporate Staff of the Executive Vice President of Research and Engineering with responsibilities covering information processing, solid state devices (particularly integrated circuits), electronic displays, magnetic tape, and data communications.

He is a Fellow of the IEEE, and a member of Sigma Xi, American Association for the Advancement of Science and The American Ordnance Association. He is a registered Professional Engineer of the State of New Jersey.

Awards

Communications Systems Division

Robert A. Risse of Communications Equipment Engineering, Government Communications Systems, received an individual Technical Excellence Award for his contributions to the advancement of the state-of-the-art in high-power solid-state power amplifiers.

Aerospace Systems Division

Virginia K. Brenton of Systems Development and Applications received the Technical Excellence Award for January for her many contributions to the software effort on information retrieval for the design automation project at Marlboro.

Harry R. Wagg of System Design Support Engineering was cited as the March Engineer of the Month for his outstanding design and implementation of a Laser Altimeter Qualification Solar Energy Simulation Test Facility.

The team of **Michael E. DeFlumere, Robert F. Dearborn, Paul A. Mednis,** and **Norman L. Roberts** received a Team Engineering Excellence Award for a Laser Measurement Equipment which was successfully designed and fabricated on a tight customer schedule. The system was built under contract with NASA Goddard Space Center and was completed within the cost budget. It is to be used by the U.S. Forestry Service for evaluation as an aid to surveying national forests.

Computer Systems

Terry D. Moyer, Production Engineer, Systems Manufacturing, Palm Beach Gardens, has been cited as the Test Engineer of the Month of February for the system and software development of the Digital Plug-in Test System (DPTS).

Fifty-four RCA scientists honored for research achievements in 1970

Fifty-four scientists on the staff of the David Sarnoff Research Center in Princeton have received RCA Laboratories Achievement Awards for outstanding contributions to electronics research and engineering during 1970. Recipients of the awards and brief descriptions of the work for which they were honored are:

Juan J. Amodei for contributions to the develment of novel media for the storage of volume holograms.

Richard S. Crandall for contributions to the understanding of electron-phonon interactions.

Raymond H. Dean for resourcefulness in developing a novel two-port solid-state microwave amplifier.

Dennis G. Fisher for the development of surface activation techniques leading to superior III-V photocathodes.

Robert E. Flory for research on optimized methods of recording video luminance and chroma information by means of an electron-beam recorder.

Allan A. Guida for fundamental investigations and contributions to data-detection schemes in communication systems involving magnetic surface recording components.

Helmut Kiess for studies of electronic mechanisms in ZnO crystals and layers as they relate to electrophotographic processes.

Charles J. Nuese for contributions to the fabrication and understanding of III-V device structures leading to improved performance in electroluminescent and transistor devices.

Peter J. Zanzucchi for unusual resourcefulness in applying various spectroscopic techniques, in particular, infrared, to thin-film problems in many important areas.

Frank I. Zonis for outstanding contributions toward the development of a Fortran IV compatible compiler system on the RCA Time Sharing Operating System.

Brian W. Faughnan, Igal Shidlovsky, and **Philip M. Heyman** for a team effort leading to improvements in electro-optic device technology, in particular, the fabrication of superior cathodochromic targets.

Irwin Gordon and **Robert L. Harvey** for a team effort in the development of improved ferrite and garnet materials for microwave devices.

Jerome B. Halter, Loren B. Johnston, Robert W. Jebens. and **William H. Morewood** for a team effort in the development and use of sophisticated techniques and apparatus for high-resolution electron-beam recording and electromechanical recording.

Kenneth R. Kaplan, Anthony D. Robbi, and **Joseph A. Weisbecker** for a team effort involving imaginative experimentation, tool-building, modeling, and simulation of cache-based computer systems.

Nicholas F. Maxemchuk and **Hugh E. White** for a team effort in developing software techniques to accomplish link control and error detection in binary synchronous data communications.

Robert W. Paglione, W. W. Siekanowicz, and **Reynold Steinhoff** for a team effort in the development of a new class of high-power microwave ferrite limiters.

Thomas M. Stiller and **Ivan H. Sublette** for a team effort in the conception and implementation of a generalized hierarchical data-management system.

Marvin S. Abrahams and **Joseph Blanc** for a team effort in developing an understanding of the origin of structural defects in III-V compounds, and in developing methods for controlling or removing them.

Lucian A. Barton, Orville E. Dow, Dennis L. Matthies, Richard W. Nosker, and **Leonard P. Fox** for a team effort in devising and improving the processing of storage media for high-density recording.

Jay J. Brandinger, Gordon L. Fredendall, Alfred C. Schroeder and **Dalton H. Pritchard** for a team effort in the development of a new high-performance single-tube color television camera system.

Martin Caulton, Robert E. DeBrecht, Richard E. Chamberlain, Robert R. Goodrich, and **Albert F. Young** for a team effort in the development and successful completion of an advanced solid-state lumped-element microwave transmitter.

Jon K. Clemens, Marvin A. Leedom, and **Richard C. Palmer** for a team effort in the conception and development of signal systems and playback mechanisms for high-density recording systems.

Louis S. Cosentino and **Wilber C. Stewart** for a team effort leading to important innovations in holographic optical memory systems.

Katsuhiro Kato and **Yasuo Wada** for a team effort in research on the growth of stoichiometric single crystals of magnetic halochalcogenide spinels.

Barry S. Perlman and **L. C. Upadhyayula** for a team effort in the development of a new class of high-power wide-band microwave amplifiers utilizing the transferred-electron effect in gallium arsenide.

Fairhurst receives special award

George F. Fairhurst, Manager of Engineering Support and Logistics for Electromagnetic and Aviation Systems Division received a "Special Recognition—Engineer of the Year-1971 Award" from the San Fernando Valley Engineers Council "For outstanding contributions to the professional engineering community, recognized national leader in the field of logistics, and unselfish contributions to the urban community.

1971 Fellowships awarded

Nine RCA employees have been awarded David Sarnoff Fellowships for graduate study in the 1971—72 academic year. The David Sarnoff Fellowships, established in 1956 to commemorate General Sarnoff's fifty years in radio, television, and electronics, are awarded annually to outstanding employees of RCA for study toward graduate degrees. The Fellowships are the top educational awards available to RCA employees. Each Fellow will be compensated at full base salary—up to maximum policy limits—during the period of his attendance at school. RCA will also pay full tuition and make a $1,000 unrestricted contribution to the university he attends.

The new 1971—72 David Sarnoff Fellows are **Christopher P. Ausschnitt,** Missile and Surface Radar Division, Moorestown, who plans to work for a Ph.D. in Applied Physics at Harvard University; **Robert H. Dawson,** Solid State Division, Somerville, N. J., who will work for a Ph.D. in Electrical Engineering at Cornell University; **W. Leigh Wilson,** NBC News Division, New York City, who plans to attend the University of California at Los Angeles, where he will work for a Master's degree in Journalism; and **Robert D. Wright,** Computer Systems, Marlboro, Mass., who will seek a Master's of Business Administration degree at Harvard University.

Five of this year's Fellows are receiving extensions of previous awards. They are **Gary R. Barton,** RCA Service Co., Springfield, Va.; **Terry J. Donofrio,** Aerospace Systems Division, Burlington, Mass.; **James B. Feller,** Communications Systems Division, Camden, N.J.; **Aldo R. Neyman,** Consumer Electronics, Indianapolis; and **Charles E. Profera, Jr.** Missile and Surface Radar Division, Moorestown, N.J.

Promotions

to engineering leader and manager

As reported by your Personnel Activity during the past two months. Location and new supervisor appear in parentheses.

Computer Systems (Marlboro)

H. W. Robinson, from Senior Member, Technical Staff, to Leader, Technical Staff (S. L. Muir, Marlboro)

Computer Systems (Palm Beach Gardens)

W. E. Salzer, from Leader, Memory Engineering, to Manager, Memory Engineering (R. Oschmann, Needham)

R. W. Badgley, from Senior Member, Technical Staff, to Leader, Memory Engineering (W. E. Salzer, Palm Beach Gardens)

A. A. Key, from Senior Member, Technical Staff, to Leader, Memory Engineering (W. E. Salzer, Palm Beach Gardens)

L. E. Thompson, to Manager, CPU Engineering, Small Systems (Palm Beach Gardens)

O. A. Gwinn, from Principal Member, Technical Staff, to Leader, Technical Staff (Palm Beach Gardens)

D. F. Pothier, from Senior Member, Technical Staff, to Leader, Technical Staff (Palm Beach Gardens)

D. D. Anderson, from Senior Member, Technical Staff, to Leader, Technical Staff (Palm Beach Gardens)

Jose Raij, from Diagnostic Programming Specialist, to Leader, Test Programming (G. W. Plowman, Palm Beach Gardens)

Electromagnetic and Aviation Systems Division

P. Archbold, from Principal Member, D&D Engrg. Staff, to Leader, D&D Engrg. Staff (E. A. Cornwall, Van Nuys)

Communications Systems Division

C. R. Norton, from Senior Member, Engineering Staff, to Leader, Design & Development (J. S. Griffin, Camden)

RCA Service Company

S. B. Davis, from Leader, Engineers, to Manager, Telemetry Systems Engineering (K. F. Wenz, Cocoa, Florida)

Electronic Components

D. M. Weber, from Engineering, Manufacturing (Lancaster), to Manager, Production Engineering (N. Meena, Marion)

D. G. Garbini, from Supt., Super Power Products Mfg., to Manager, Mfg. and Production Engineering (Manager, Super Power Operations, Lancaster)

W. M. Sloyer, from Supt., Regular Power Products Mfg., to Manager, Mfg. and Production Engineering (Manager, Regular Power & Laser Operations, Lancaster)

Licensed Professional Engineers

A *Directory of RCA licensed engineers* was published in the Vol. 16, No. 5 (April/May 1971) issue of the *RCA Engineer*. The Professional Engineers listed below were not cited in that list, were listed incorrectly, or have received their license since the publication date. If you hold a professional engineering license in any state (regardless of where you may actually now work) and your name did not appear in the *Directory* or in subsequent citations, then send your name, PE number (and state in which registered), RCA division, location, and telephone number to: *RCA Engineer*, Bldg. 2-8, RCA, Camden, N.J. As new inputs are received, they will be published.

Computer Systems

R. Habermann, CS, Palm Beach Gardens; PE-27648, N.Y. PE-3730, Maryland. PE-10794, Fla.
W. R. Hall, CS, Marlboro, Massachusetts, PE-14429; Massachusetts.
M. Mooradian, CS, Marlboro, Massachusetts, PE-13068; Massachusetts.
H. N. Morris, CS, Palm Beach Gardens; PE-14528, Fla.
K. D. Peters, CS, Palm Beach Gardens, Fla., PE-043107; N.Y.
R. B. Resek, CS, Marlboro; PE-018180, Ohio.
J. P. Watson, CS, Palm Beach Gardens, Fla., PE-E1882; California.

RCA Service Co.

R. M. Dombrosky, Sv. Co., Cherry Hill, PE-14495; N.J.
J. S. Hill, Sv. Co., Va.; PE-9231; Ohio.
D. H. Rudd, Sv. Co., Holloman AFB, N.M., PE-4710; Minn. PE-4654; N.M.
P. Tokareff Jr., Sv. Co., Patrick AFB, Fla.; PE-5746; Oklahoma.

Aerospace Systems Division

J. H. Budiansky, ASD, Burl. Mass. PE-23562; Mass.
P. S. Dubroff, ASD, Burl. Mass. PE-EE7508; Calif. PE-41653; N.Y. PE-20442; Mass.
N. L. Laschever, ASD, Burl. Mass. PE-E-017327; Ohio.

Communications Systems Division

I. Joffe, CSD, Camden, N.J., PE-17847; N.J.
J. Noto, CSD, Camden, N.J., PE-05771; Connecticut.
D. H. Williamson, CSD, Camden, N.J., PE-2905; Delaware.

Consumer Electronics

H. W. McCune, CE, Indianapolis, Ind., PE-12038; Ind.

Corporate Staff

P. S. Ridley, Corp, Cherry Hill, PE-20904; Ohio.

F. W. Widmann, Corp, Camden, N.J., PE-8131; N.J.

Electronic Components

J. J. Kelley, EC, Cleveland, Ohio, PE-29742; Ohio.

J. F. Sterner, EC, Harrison, N.J., PE-15088; N.J.

Missile and Surface Radar Division

H. Berkowitz, MSR, Moorestown, N.J., PE-23101; N.Y.
J. F. Hobson, MSR, Moorestown, N.J., PE-2115E; Pa.
A. G. Hopper, MSR, Moorestown, N.J., PE-001540E; Pa. PE-041722; N.Y. PE-21322; Mass.
G. Scarpulla, MSR, Moorestown, N.J., PE-30772; N.Y.
M. D. Swartz, MSR, Moorestown, N.J., PE-13686; N.J.
Herbert L. Polak, NBC, N.Y., PE-042746; N.Y.

Patents and Licensing

M. DeCamillis, Patents and Licensing, Princeton, N.J.; PE-11692; N.J.

Solid State Division

R. T. Chu, SSD, Somerville, N.J., PE-17462; N.J.
S. Goldfarb, SSD, Somerville, N.J., PE-9324; N.J.
C. Lindsley, SSD, Somerville, N.J., PE-13355; N.J.
R. C. Pinto, SSD, Somerville, N.J., PE-13543; N.J.
M. Tuttle, SSD, Somerville, N.J., PE-12794; N.J.
H. Waltke, SSD, Somerville, N.J., PE-14483; N.J.

Dr. William M. Webster, Vice President, RCA Laboratories (left), congratulates Leslie E. Flory and his son, Robert E. Flory (right), on their being the first father and son to each receive an RCA Laboratories Achievement Award since the awards were originated in 1947. Robert E. Flory, a Member of the Laboratories Technical Staff, recently was presented with a 1970 Award for his research on video recording. His father, who retired in 1968 after a 38-year career with RCA, received three RCA Laboratories Awards for team research. In 1948, he was honored for his work on a letter recognition system; in 1950, simplified industrial television equipment; and in 1957, an experimental vehicle control system.

Computer Systems, Palm Beach Gardens, holds professional recognition dinner

Thirty-nine authors and inventors at Computer Systems, Palm Beach Gardens, were honored at a recognition dinner April 12 at the Professional Golfers Association (PGA) Clubhouse. The dinner was sponsored by the Systems Development Division, Palm Beach Product Laboratory. **H. N. Morris,** Manager, Palm Beach Product Laboratory, was the host and was also recognized as the author of a paper in an earlier issue of the *RCA Engineer* and of the "inside-front-cover" message in this issue. Master of Ceremonies was **S. B. Ponder,** Administrator Special and International Accounts.

J. P. Watson (second from right) accepting copy of an "early" patent from S. B. Ponder. Mr. Watson has been awarded 60 patents during his career with RCA. With Ponder and Watson are P. A. Beeby (second from left) and H. N. Morris (right).

Tops among the inventors was **J. P. Watson,** Staff Engineering Scientist, with more than 60 U.S. and foreign patents. **A. T. Turecki** ranked high as both inventor and author.

The complete list of honorees follows: **D. B. Ayres, G. C. Boswell, R. C. Calhoun, J. Chisholm, J. P. Clary, W. J. Davis, T. D. Floyd, J. L. Freeman, E. M. Fulcher, M. C. Guerrero, D. W. Hall, J. W. Haney, A. R. Harris, J. G. Hoehn, K. H. Hoffman, E. C. James, E. G. Jenney, C. L. Jones, H. Kleinberg, S. Kuo, J. Leppold, L. J. Limbaugh, C. Madrazo, R. A. Mancini, K. McDonagh, H. N. Morris, S. C. Nanda, R. Notaro, N. L. Perez-Stable, R. C. Peyton, A. Prieto, J. Raij, R. M. Rudys, R. G. Saenz, W. E. Salzer, G. K. Schulze, R. T. Sells, R. S. Singleton, R. Taynton, A. T. Turecki, J. P. Watson, W. D. White, P. M. Woolley, D. J. Wray,** and **J. J. Yorganjian.**

The guests were **P. A. Beeby,** Vice President Technical Operations, Systems Development Division; **W. O. Hadlock,** Editor, *RCA Engineer;* **J. C. Phillips,** Associate Editor, *RCA Engineer;* **H. Christofferson,** Manager, Patents, Information Systems, DSRC; **K. L. Snover,** Manager, Manufacturing Operations, Palm Beach; **R. J. Spoelstra,** Manager, Design Center, Palm Beach Product Laboratory; and **E. D. James,** Manager, Communications and Terminals, Palm Beach Product Laboratory.

Command and control systems training program

RCA Moorestown has made a commitment to strengthen its command and control systems capability to better perform and compete in the large-scale defense and commercial systems markets. As a means of achieving this, an after-hours training program entitled "Command and Control Systems" is being conducted to prepare employees for possible placement in this skill area.

The program started in mid-April and will continue for approximately six months, with participants attending classes two evenings per week. Subjects to be covered include: introduction to command & control systems; digital computer systems; real-time programming; functional analysis; system testing; and system simulation.

Workshop sessions will be conducted throughout the program to enable participants to apply systems concepts to the solution of actual problems.

At the conclusion of the program, qualified participants will be considered for available positions in the command and control systems groups at Moorestown, although completion of the program will not guarantee placement.

Dr. Hanak named Fellow by RCA Laboratories

Dr. Joseph J. Hanak has been named a Fellow of the Technical Staff of RCA Laboratories in Princeton, N.J.

In announcing the honor, **Dr. William M. Webster,** Vice President, RCA Laboratories, said the Fellow designation is comparable to the same title used by universities and technical societies. It is given by RCA in recognition of a record of sustained technical contributions in the past and of anticipated continuing technical contributions in the future.

Dr. Hanak, a member of the RCA Materials Research Laboratory, has done distinguished work in the fields of vapor deposition of superconducting materials for high-field magnets; fabrication of magnetic recording heads; novel RF sputtering techniques for exploratory materials research; and the chemistry and metallurgy of rare earth elements.

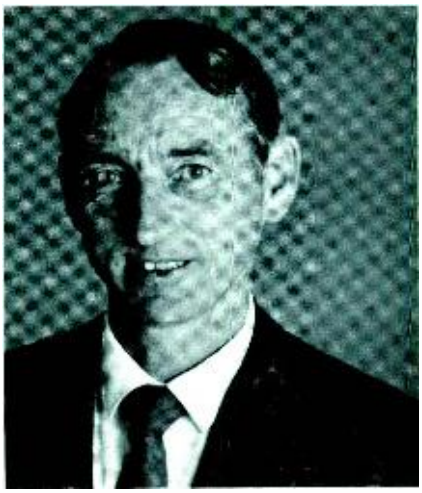
ATL authors, inventors, and speakers feted

All personnel of the Advanced Technology Laboratories who had articles published, filed patent disclosures or were awarded patents, and/or presented papers at meetings or symposia were honored at a reception/dinner on February 16, 1971 at the Cherry Hill Inn. **Drs. J. Vollmer** and **H. J. Woll** provided the welcome and opening comments. Both congratulated and praised the people present for their technical excellence and their contribution to the prestige of ATL.

Mr. A. F. Inglis, Division Vice President and General Manager, of the Communications System Division gave a viewgraph-accented talk about the building changes, additions, and improvements to be expected to the RCA complex in Camden.

The authors, inventors, and speakers who were honored are: **G. J. Ammon, D. Benima, A. S. C. Berens, W. A. Clapp, M. S. Corrington, M. S. Crouthamel, N. H. Farhat, B. R. Feingold, A. Feller, L. H. Fulton, W. F. Gehweiler, R. C. Gray, W. F. Heagerty, D. G. Herzog, M. W. Howell, E. Hutto, P. F. Joy, H. W. Kaiser, M. L. Levene, B. J. Levin, J. T. Martin, W. F. Meeker, D. J. Miller, E. J. Mozzi, L. J. Nicastro, R. L. Pryor, P. W. Ramondetta, C. W. Reno, P. B. Scott, R. D. Scott, E. G. Seybert, F. E. Shashoua, B. Shelpuk, B. W. Siryj, R. J. Tarzaiski, J. Vollmer, G. G. Weidner, H. M. Weiskittel, D. J. Woywood, P. E. Wright** and **M. Yamamoto.**

Sellers



Tanner

Sellers and Tanner are new Ed Reps

John D. Sellers has been appointed Editorial Representative for RCA Alaska Communications Inc., Anchorage, Alaska. **William D. Tanner** was appointed Editorial Representative for Communications Systems Division, Professional Electronic Systems, Burbank, California. Editorial Representatives are responsible for planning and processing articles for the *RCA Engineer*, and for supporting the corporate-wide technical papers and reports program.

Mr. Sellers is Chief Engineer of RCA Alaska Communications, Inc., Anchorage, Alaska. He received the BSEE from the University of Miami in 1950 and joined RCA with the Missile Test Project group in 1954, later serving as Manager of Communications Systems Projects. He transferred to the RCA International Division where he served as Area Manager in Iran for CENTO. From 1965 to 1969 he was an Engineering Supervisor for the RCA Service Company at the White Sands Missile Range.

Mr. Tanner studied physics at UCLA. Prior to World War II, he worked with the Army Signal Corps testing and maintaining communications equipment. In 1943, he joined the U.S. Navy and, after attending Radio Material School, taught electronics until discharged in 1946. In 1949, joined RCA Service Company as a technician, servicing TV receivers and mobile communications equipment. In 1952, he helped set up the RCA Service Company branch office in Hawaii. In 1954, Mr. Tanner joined NBC as a maintenance engineer. In 1960, he left NBC to help set up an independent mobile video taping unit. He returned to RCA in 1962 as a Systems Engineer at the Hollywood film recording facility. When the film recording facility moved to Burbank, Mr. Tanner became involved in writing documentation and compiling instruction books.

Comprehensive *RCA Laser* anthology available

A unique display of RCA's skills, abilities, and facilities for the design, development, and application of lasers and laser detectors is now available.

The *RCA Lasers* anthology presents the technical contributions of more than eighty RCA scientists and engineers to laser research and engineering. This 208-page work consists of papers selected from material published in the *RCA Engineer* over the past seven years; however, only those early papers of current value are included.

Copies of these reprints are $2.25; although single-quantity orders will be filled, minimum orders of five are preferred. To order send your name, location, and account number (if a personal order, send check or money order) to:

RCA Lasers
RCA Staff Technical Publications
Building 2—8
Camden, N. J. 08102

Professional Activities

Astro-Electronic Division

Dr. A. G. Holmes-Siedle has been invited to chair the Ionization Effects Session of the IEEE Nuclear & Space Radiation Effects Conference at Durham, N.H., July 1970.

R. Newell was elected Chairman, Aerospace and Electronic Systems group, N.J. Coast Section of IEEE, and he was named a member of the Satellite Systems Committee, Aerospace and Electronics Group, IEEE.

Communications Systems Division

James H. Goodman of Government Communications Systems was honored for his performance as Chairman of the IEEE Group on Reliability during the 1969-1970 season.

Government and Commercial Systems

Dr. Harry J. Woll, Chief Engineer, Government Engineering, received a Special Section Award from the Philadelphia Section of the IEEE "for inventive electronics engineering, technical management, and service to the IEEE."

Aerospace Systems Division

The IEEE has formed a Technical Meetings Committee, consisting of representatives of the Regional Activities, Technical Activities, and Convention Board. The committee consists of nine members, and is a permanent committee of the IEEE. **D. B. Dobson,** ASD has been named to the committee.

Missile Test Project

G. Denton Clark, Division Vice President, Range Projects, recently received a C.H.I.E.F. (Champions of Higher Education in Florida) Award from the fourteen presidents of the Independent Colleges and Universities of Florida.

RCA 3 to be featured at Spring Joint Computer Conference

The first RCA 3 virtual memory computer will be featured in RCA Computer Systems' 30-x-50-foot exhibit at the Spring Joint Computer Conference, May 18-20, in Atlantic City, N.J. The RCA 3 was designed and built by Computer Systems at Palm Beach Gardens, Fla. The Atlantic City exhibit marks the first time a complete RCA computer system will be demonstrated at a trade show.

RCA Review, March 1971

Volume 32, Number 1

Contents

The *RCA Review* is published quarterly. Copies are available in all RCA libraries. Subscription rates are as follows (rates are discounted 20% for RCA employees):

	DOMESTIC	FOREIGN
1-year	$6.00	$6.40
2-year	10.50	11.30
3-year	13.50	14.70

Index to RCA Engineer Volume 16

This index covers Vol. 16-1 (June-July 1970), 16-2 (Aug.-Sept. 1970), 16-3 (Oct.-Nov. 1970), 16-4 (Dec. 1970-Jan. 1971), 16-5 (Feb.-Mar. 1971), and the present issue, 16-6 (April-May 1971). Since *RCA Engineer* articles are also available as reprints, the reprint number (PE-000) is noted throughout. *RCA Engineer* papers are also indexed along with all other papers written by the RCA technical staff in the annual *Index to RCA Technical Papers.*

Subject Index

Titles of papers are permuted where necessary to bring significant keyword(s) to the left for easier scanning. Authors' division appears parenthetically after his name.

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