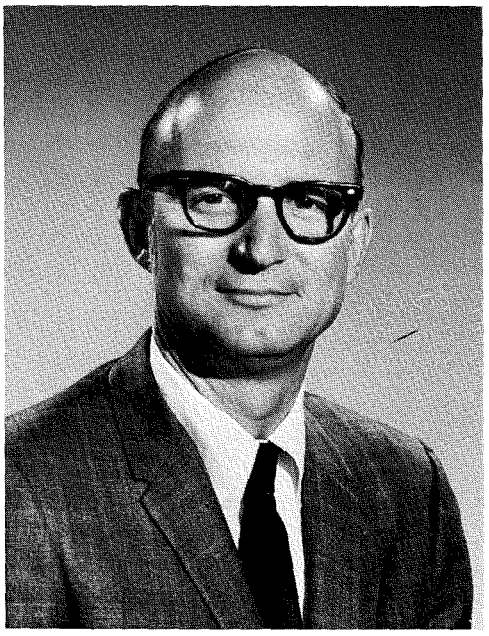
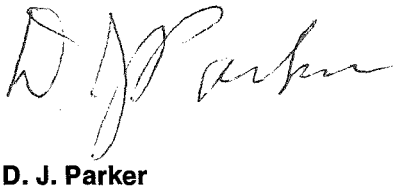
Communications, command and control

This issue of the *RCA Engineer* describes a number of recent RCA achievements in communications systems, and command and control. This field of endeavor includes RCA programs that have been vitally important to our national defense posture and prestige: Minuteman, Autodin, Apollo, and Sanguine. The Government Communications Systems contributions to these programs have been among our most satisfying and rewarding accomplishments.

RCA has established a traditional excellence in digital and RF equipment design, and our engineering investments are selected to maintain this superiority. In spite of this excellence, our success on major programs could not have been accomplished without exceptional systems strength. For example, the GCS contribution in command and control has been primarily the communications function. The communications function in command and control is required to be more reliable and more resistant to attack than the weapons system so as not to impose a limit on the system. In every case we had to anticipate and synthesize the overall systems requirements based on independent knowledge and analysis of the mission, the environment, and economic and political constraints.

RCA will continue to offer its customers a unique combination of advanced equipment design and thorough systems knowledgeability. The completeness of our technical competence will make RCA a favored partner for the major communications and command and control systems of the future.





D. J. Parker
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Our cover
. . . represents the growth of command and control systems over a 200-year span—from the relatively simple methods used by Paul Revere (one if by land, two if by sea) to alert his "minutemen" to the modern Minuteman complex represented in the photograph. Interestingly, human involvement is still crucial to mission success. **Photo courtesy** of The Boeing Company, Seattle, Washington.

Vol. 16, No. 3
Oct | Nov
1970

RCA Engineer

A technical journal published by
RCA Corporate Engineering Services 2-8,
Camden, N.J.

RCA Engineer articles are indexed annually in the April-May Issue and in the "Index to RCA Technical Papers."

• To disseminate to RCA engineers technical information of professional value • To publish in an appropriate manner important technical developments at RCA, and the role of the engineer • To serve as a medium of interchange of technical information between various groups at RCA • To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions • To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field • To provide a convenient means by which the RCA engineer may review his professional work before associates and engineering management • To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

Contents

editorial input

computers and communications

Not long ago, computers and communications were looked upon as distinctly different technologies. However, during the past decade, both have matured to the point where they can no longer be separated.

The computer must handle numbers that stagger the imagination —commercial inventories worth millions of dollars and comprising hundreds of thousands of individual items—banking and finance commitments in hundreds of billions of dollars—world-wide market projections in billions of consumers—and federal tax records in millions of returns annually; the list could continue indefinitely. Yet, the computer has proven to be a powerful tool for manipulating these numbers, and promises faster, more versatile input and output devices, virtually unlimited memory capacities, increased speed, and more hardware and software flexibility to cope with future demands.

However, there is a growing need to examine the interrelationships between the countless segments of information that comprise the masses of machine-readable data being collected each day. This is now being done only in isolated instances, and only by somewhat brute-force methods. It seems that there must be a trend toward the development of a massive "nervous system" that will ultimately extend into each warehouse, office, and factory to gather data which will be processed, correlated, appraised, and communicated to those that can make constructive use of such information. Ultimately, such a system may extend as far as the home and classroom.

However, such a closely linked system may become a reality only when some of the moral, economic, and political roadblocks are removed. But the trend is clear: computers and communications are becoming inseparable technologies, and industrial and government customers are already looking toward customized operational systems that will take advantage of both.

For example, with recent improvements in highway and airline transportation, goods are being moved point-to-point much faster than the necessary paperwork which must rely on the cumbersome and complex postal network. Astute businessmen are taking advantage of data communications to move inventory and billing information point-to-point to keep pace with the movement of goods, and thus obtain a distinct economic advantage.

Digital communications is already a technical reality, as demonstrated by the Datalex service of RCA Global Communications, Inc. or the Dataphone or Dataphone 50 systems currently offered by AT&T. However, these systems are only a start in the right direction, and they are already taxing the resources and capabilities of common communications carriers.

At this point, some sort of unifying force seems needed—a force that could combine strong systems design with proper measures of communications and computer expertise to establish operational modes and develop the necessary systems and equipment for data transfer.

RCA, with its traditional strengths in communications and systems engineering and its new and vigorous commitment in the computer industry, is in an excellent position to provide solutions to the technical problems, and also take advantage of a data communications market that is growing faster than the burgeoning computer market.

Future issues

The next issue of the *RCA Engineer* features RCA engineering activities centered in New York. Some of the topics to be discussed are:

NBC field operations

International and satellite transmission

NBC Radio Network facilities

Television studio for the Tonight Show

Audio consoles for TV networks

Data, Voice, and Television Services

RCA Hot Line Telephone/Data System

RCA Records

New RCA recording studio

RCA Institutes

Discussions of the following themes are planned for future issues:

Consumer electronics

Computers

Displays, optics, photochromics

Graphics

Advanced Technology Laboratories

Mathematics for engineering

Video playback systems

Impact of mini-computers on manufacturing

S. N. Levy

The use of computers—especially mini-computers—in the RCA factories has undoubtedly come of age. In the past four years, over fifty systems have been integrated into RCA's manufacturing operations. This paper briefly reviews the history of these small computer systems at RCA with particular emphasis on those growth patterns that will provide some perspective on the impact of the computer in the factory of the seventies.

EARLY PROCESS-CONTROL COMPUTERS were installed primarily for two reasons:

1) The user wanted real-time data analysis, and the only way of obtaining it was to have his own computer part of the test system.
2) The sophistication of the test set or sets had grown to the point where a wired controller or other programming methods such as paper tape or a magnetic disc were no longer adequate to perform the required functions with enough flexibility.

The earliest process-control computers were used for computer-controlled testing. Of the first four implemented by RCA, three were for engineering and one for manufacturing. In 1966, the Automatic Production Test Equipment (APTE) was installed at Electronic Components color kinescope plant in Marion, Indiana, to improve kinescope quality through comprehensive testing and statistical data analysis. Primarily a manufacturing application, it uses an SDS (Scientific Data System now Zerox Data Systems) 920 computer and controls five test stations.

Also in 1966, a computer-controlled integrated-circuit tested was implemented in the Somerville, New Jersey facility. The system is basically a DC tester controlled by a Spectra 70/15 computer. Primarily used by engineering to develop on-line statistical analysis of semiconductor wafers, the system allows rapid engineering evaluation of solid-state products.[2]

In 1967, two more computer-controlled test systems were installed. One system, utilizing Digital Equipment Corp. PDP-8 computer, was used in the Consumer Electronics Division, Indianapolis, Ind., to perform data analysis on several test sets and to control a DC integrated circuit tester. Another system using a Honeywell DDP 116 computer was a space satellite memory exerciser for the Astro-Electronics Division at Hightstown.

Since 1968, the Corporation has been acquiring small process-control computers at a high rate, until today there are over fifty systems in operation.

Availability of small computers

The use of computers in manufacturing during the last several years was spurred primarily by the availability of the now famous "mini-computer." The granddaddy of all mini-computers was the Digital Equipment Corporation PDP-8 computer announced in 1965. Prior to 1965 several small computer were available, but their cost was over $20,000. The PDP-8 was the first computer to sell for less than $20,000 thus starting the mini-computer race. Today there are more than 50 companies making and selling mini-computers for a variety of uses.

Since 1965 the architecture and price of mini-computers has evolved substantially. Mini-computers today start in price at $5,000. For $10,000 you can buy relatively powerful mini-computers capable of performing some fairly sophisticated tasks. A variety of options, peripherals, interfaces and software packages are available—many of which are tailored to manufacturing test and control systems.

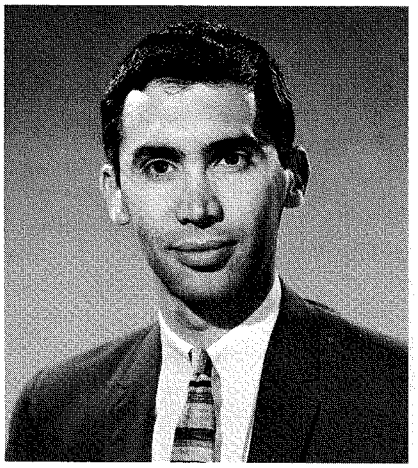
Growth patterns

Acquisition pattern

There has been no typical pattern of acquisition within RCA. Where appropriate, Divisions, would purchase a completely packaged system. In other cases, the Division would purchase all the parts and integrate the system themselves. In still other cases, one Division would serve as systems manager for another Division. It is expected this acquisition pattern will continue in the future, with system flexibility, availability, and cost as the

Reprint RE-16-3-6
Final manuscript received June 9, 1970.

The Engineer and the Corporation



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received the BEE from Cornell University in 1955. He was employed at Hughes Aircraft Company from 1955 to 1959 where, as a design engineer, he worked on pulse doppler radar systems and participated in the Hughes graduate engineering study program at UCLA. He joined the RCA Service Company in Riverton, New Jersey, in 1959, as a field engineer for the BMEWS project. He later went to Thule, Greenland, to work on the installation of the computer system for the BMEWS Radar. After the system became operational, Mr. Levy continued on as Manager, Technical Maintenance, of the site with responsibility for engineering and maintenance of the radar, data processing, and display equipment. After leaving Greenland, Mr. Levy was responsible for system evaluation of all three BMEWS radar sites. In 1964, he joined the newly oranized corporate staff group concerned with automatic testing in RCA. This group is responsible for implementing corporate policies, plans and programs relating to Automatic Test and Measurement Systems within RCA. Since that time he has been instrumental in implementing automatic test projects in several of the RCA divisions, with particular emphasis on computer controlled systems. Mr. Levy is a member of IEEE, Eta Kappa Nu and Tau Beta Pi.

primary forces affecting the mode of acquisition.

New applications

Although the early applications have been primarily test systems, the later uses in manufacturing have branched to other areas. Computers are now being used for numerical control machines, mask generators, and gauging equipment.

Another new area that could have a significant effect on the factory is data collection from factory workers. Two such systems have been installed solely for data collection. One system in the Consumer Electronic Division in the Rockville Plant uses the RCA Data Gathering System terminals for collecting product count data. Another system in the same Division in the Memphis Plant is collecting trouble-shooting data with specially designed input terminals.

As time progresses, the factory computer will be interfaced to more and more electrical and mechanical test and process equipment. Companies are now selling computer controlled insertion equipment, computer controlled wire wrappers, computer controlled resistor trimmers and so on. Each year new computer controlled manufacturing equipment enters the marketplace.

Evolution of computer configurations

Most process-control computer configurations developed over the past three years have fallen into either of two categories: one computer for each operation, or one computer controlling many operations. The former system provides simplicity of operation and relatively easy system integration. Also, it provides an extra measure of reliability since a computer failure affects only one operation. A computer controlling several operations, on the other hand, provides a cost savings in that computer hardware is shared; this often allows more money to be allocated for better peripheral equipment. A further advantage of this type of system is that data for an entire production line (or possibly a factory) can be integrated into one computer allowing rapid generation of management information reports.

Another pattern of configuration is beginning to develop. Some manufacturing users within the company and outside of RCA are beginning to utilize a hierarchy of computers. Within RCA, the Consumer Electronics Division, in one of their systems, will have two PDP 8's "talking" to an RCA 1600 computer.

Future

The future for manufacturing uses of mini-computers is excellent. A. D. Little predicts that by 1974, there will be over 100,000 mini-computers in operation.[3] Of these, it is estimated that over 35,000 will be used for industrial applications alone. Thus by 1974 just about every manufacturing plant will have one or more mini-computers.

Some examples demonstrating the range of industrial applications are

1) Production scheduling
2) Machine loading
3) Materials management
4) Machine control
5) Automatic testing
6) Production line control

To make these inroads in the factories, their use must be associated with cost

Table I—Sampling of process-control computers being used by RCA

Location	*Computer*	*Test Set*	*UUT*	*Remarks*
Hightstown	DDP-116	Memory Exerciser	Satellite Memory	
Hightstown	2 Varian 620I Computers		Satellites	
Hightstown	H.P.2116		Satellites	
Hightstown	H.P.2116	Data Acquisition	Satellites	
Hightstown	SEL 810A	Data Acquisition	Satellite	Used for data acquisition from environmental chambers
Moorestown	H.P.2116	Microwave Network Analyzer	RF Components	These are the H.P.8542A Automatic Network Analyzer Systems
Van Nuys	H.P.2116	Microwave Network Analyzer	RF Components	
Van Nuys	RCA 1600	Logic	Digital PC Boards	
Camden	RCA 1600	Logic Linear	Digital P.C. Boards Radio Sets	Will be capable of 500 MHz tests for communications systems
Burlington	Spectra 70/45	Analog test station	Modules	Plant MIS computer will run analog test station. Software package able to handle expansion to additional stations limited only by number of CCAT channels provided
Rockville	PDP-8	DC	Transistors, Capacitors and Resistors	This was an engineering prototype system

Location	*Computer*	*Test Set*
Rockville	MAC 16	
Rockville	RCA 1600	DC and
	PDP-8	Capacito Tester Process Control System
	PDP-8	Resistor Tester Process Control System
	PDP-8	Data Lo and bac
Rockville	RCA 1600	
Indianapolis	PDP-8	
Memphis	RCA 1600	
Marion	SDS 920	Shorts a Leakage Focus Breakdo Anode Breakdo PHI Cutoff
Marion	PDP-8	

savings and improved product quality. Some examples of how they can do this are:

1) Development of real time data and data reduction leading to improved yields and quality.
2) Controlling complex test and process equipment with maximum flexibility allowing for quick changeover.
3) Performing on-line diagnostic and fault locations thus saving labor costs.
4) Doing things never done before because of a lack of computer power.

As mentioned, a significant growth pattern is beginning to develop which many industrial sources indicate will be a continuing one, i.e. the hierarchy of computer systems. Fig. 1 depicts this showing three levels of computers. At the lowest level are the satellite computers. These are control computers with minimum memory and peripherals. Their function is to control one or two devices. This computer could also be collecting data from several sources.

At the next level, the factory or supervisory computer begins to integrate several satellite computers and possibly non-computer devices together. The factory computer loads programs into the satellite computers and receives data back. It reduces the received data, developing summary reports. These reports may be typed out directly on the factory floor or in the computer room. Factory personnel will also be able to query the computer for information.

This computer and possibly others will then feed into the Spectra 70 MIS computer. The Spectra 70 will serve as the general data storage machine generating longer range manufacturing performance reports.

Conclusions

RCA during the past several years has used mini-computers in manufacturing extensively. As indicated by the industrial mini-computer growth predictions, RCA is typical of what is happening throughout industry. As mini-computers go down in cost and as more people become capable of using them, they will continue to make substantial inroads in manufacturing. It is very likely that the application of mini-computers in the factories will have more of an impact on manufacturing in the 1970's than any other single factor.

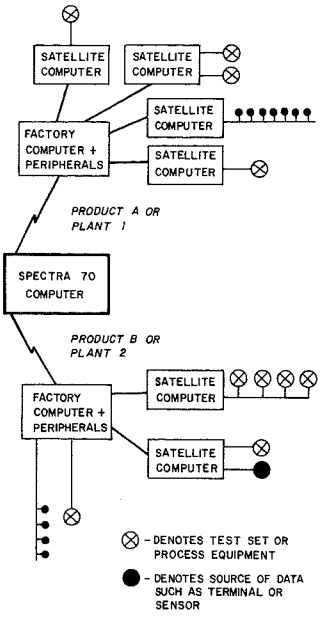


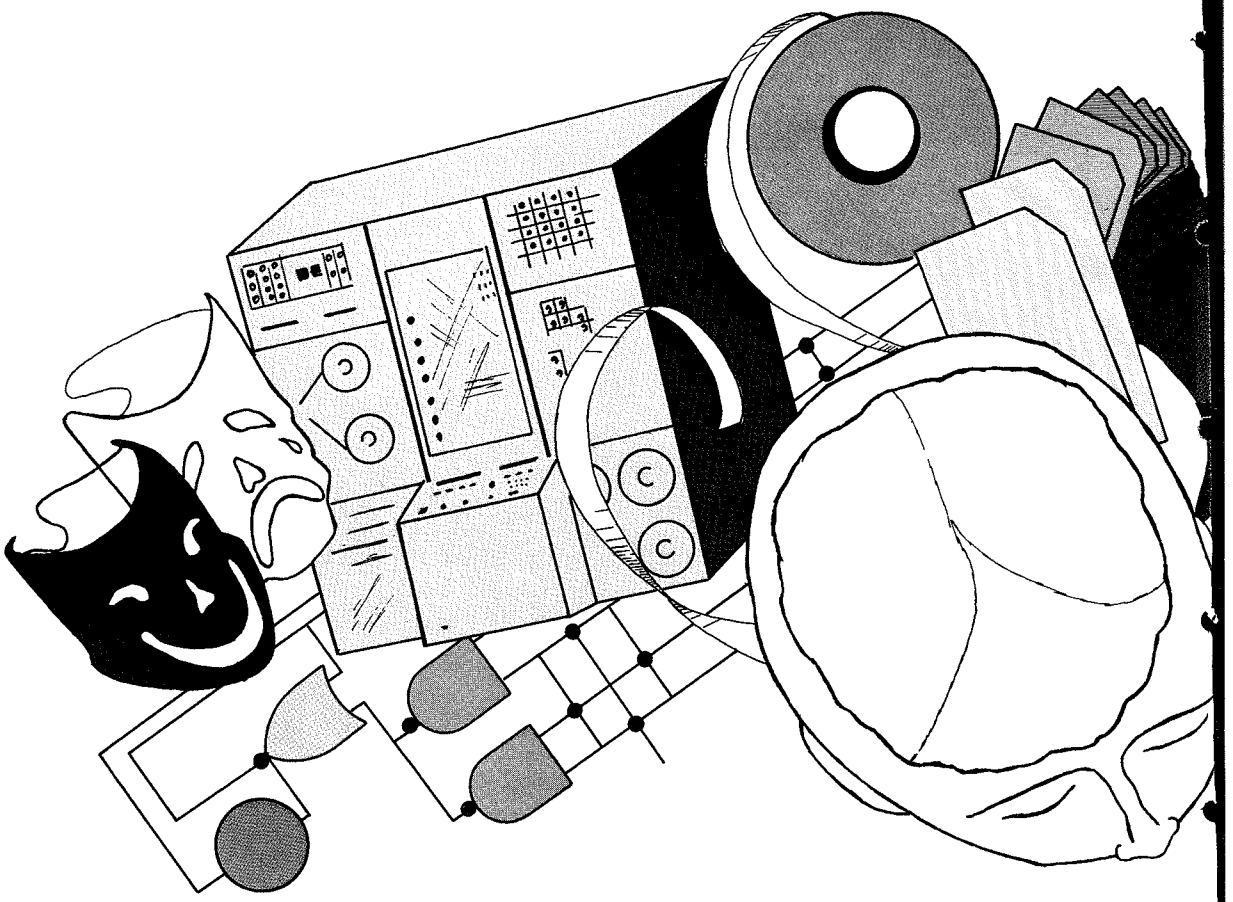
Fig. 1—Development of a heirarchy of computer systems.

References

1. *Automated Support Systems*, RCA reprint PE-403; *RCA Engineer*, Vol. 14, No. 2 (Aug-Sep 1968).
2. Wamsley, B. J., Crossley, E. C., Vonderschmitt, B. V., and Levy, S. N., "The RCA Computer-Controlled Integrated-Circuit Test System," *Engineering at RCA*, RCA reprint PE-361, *RCA Engineer*, Vol. 13, No. 1 (Jun-Jul 1967).
3. Little, Arthur D., *Outlook for Minicomputers* (March 1970).

	Remarks
	For control of tuner alignment stations
rids	Final AC/DC parameter test
een Printed pacitors	Data is collected and analyzed to adjust furnace belt speed for process control
ck Film istors	
	DGS Production count reporting
	For engineering development of a TV set tester
	Automatic Defect Diagnosis System (ADDS) for collection of defect data from trouble-shooters. Uses Personal Input Terminals
r scopes	Manufacturing system for process control
	Controls contour

Location	Computer	Test Set	UUT	Remarks
				gaging equipment for color kinescopes
Somerville	Spectra 70/15	DC Tester	I.C.	Engineering system produces statistical analysis of test results
Somerville	RCA 1600	DC	I.C.	Factory system
Somerville	PDP-8	Teradyne J259	IC	
Somerville	PDP-8			Controls a movable table for micro-positioning.
Somerville	PDP-8			Part of Mann Mask Generator
Somerville	PDP-8			Controls a plotter for design automation
Mountaintop	H.P.2116	Transistors	Transistors	Data Asquisition for 5 transistor test sets
Lancaster	PDP-9	Pulse Height Analyzer	Photo Multiplier Tubes	Used for real time process control in manufacturing
Lancaster	PDP-8			Controls contour gauging equipment for Color kinescopes
Marlboro	RCA 1600	Disc File Tester	2 Disc Storage Units are tested simultaneously	
Palm Beach	Spectra 70/15	Tape Station Tester	Tape Stations	This was a prototype tester for tape station testing.
Palm Beach	70/15, 25	Input/Output Interface test	70/15, 25	Tests I/O operation including intraction between trunks
Palm Beach	70/35, 45	Input/Output Interface Test	70/35, 45, 46	
Camden	RCA 1600	DITMCO 660B	P.C. Boards	For future computers



Computers and intellect

H. Kleinberg

One of the main problems with computers is that they were invented by a very articulate bunch of people. From his first awareness of these devices, Mr. Ordinary Man has been deluged with explanations, prognostications and elucidations of the implications of the "thinking machine". He has seen it guide spacecraft, predict elections, forecast markets, control traffic and sniff out flaws in his tax return. And all this time he is continually told "you ain't seen nothin' yet."

Is it any wonder that an ambivalent attitude, optimism mixed with fear, is generally held by the public toward these machines? I accept both these feelings as appropriate. Computers have a greater positive potential than even we in the business realize, but at the same time, they are one of the greatest potential friends that bureaucracy and power-wielders ever had. Our goal, then, must be to realize their vast social and technological benefits, without regretting at some later date that we ever allowed them to fall into the hands of government.

Unquestionably the major tool in keeping these factors balanced is an understanding of exactly what these machines are. I have read many such explanations, but have never come away with anything concrete. As a step toward filling this void, may I offer two proposals: a semantic lecture, and a theory of how to measure a job's intellectual content against the capability of a computer.

My sermon about words is very brief. Let us who work with these machines stop saying that computers solve problems. They don't. You don't put a problem into a computer; you put in a solution. A program is a statement of the steps of the answer, not of the question.

All this may sound like the fastidious hairsplitting of a bookish grammarian, particularly now that worrying about words is considered undemocratic, but I think that the distinction is an important one. I feel that many a hapless customer would have saved himself and his supplier uncounted hours and dollars had he realized that he would have to have solved his own problems before he could use a computer. Incidentally, the confusion between solutions and problems is epidemic in our society, and merits a study by itself.

So no computer built has ever solved a problem. This limitation is not caused by shortcomings in the speed or complexity of today's hardware or software. It is not something that will be changed by integrated circuits, new operating systems or time-sharing. It is implicit in the fact that computers are logic machines, capable of carrying out only those operations that can be reduced to a series of logic equations. And logic is not a creative problem-solving process.

This statement may be considered by some to be mildly controversial, and I guess it does run counter to the veneration of the "rational approach" that we have been taught for so long. But it brings me to my second point. You may feel free to call this "Kleinberg's Law of Intellect."

Intellect, as I use the term, is the sum of processes by which we humans mentally operate on an input to produce an output. Intellect is made up of three elements: Logic, Emotion and Intuition. For the sake of not abandoning

Reprint RE-16-3-18
Final manuscript received August 28, 1970.

good engineering practice, I'll call these L, E and I.

Being non-expert in all fields related to the measure and analysis of the mind, I have no fear at all in trying to define these three components. I hedge only in making them functional definitions, which is why I'm not afraid.

Logic is the process we use when we follow a given set of rules. This process existed long before the rules were stated by the Greeks or mechanized by computers, but the point is that the process *can* be stated as a set of rules against which operations can be measured as valid or not valid. Logic in this sense is quite restrictive, in that "being logical" is not the same as "being reasonable", or "being sensible." It is, of course, closely related to mathematics, and is completely abstract in nature. It provides no means for verifying the statements on which it is operating, and works with the same cold precision on the ridiculous as it does on the brilliant.

Emotion is the process that an engineer uses none of in reviewing his co-worker's design, but uses much of in defending his own. It is the process that dominates our reactions to other people and the formation of our basic assumptions about the kind of world we want. When either of these, or such things as esthetics, are involved in a problem, then emotion is, quite properly, a major part of our intellect. Its rules, if any, have never been codified. Psychologists and others have probed the elements that shape it, but the "how" of it has never been described. Unlike logic, it is very strongly tied to the real world, and to our individual experiences in that world. These experiences build upon our basic drives for survival and reproduction in some cumulative manner to produce the complicated adult. Maybe this component should be broken down into a number of others, but it would make my theory too complex.

Intuition is another uncodified process. It is the one involved when an engineer suddenly sees that he has been looking at a problem from the wrong angle, and things start to fall into place. It is the process by which a manager knows he is not being told the whole truth. It is a part of intellect much neglected by the experts, and the one that I feel is the creative one. I have no idea how it operates, except that it seems to be a highly developed system of recognizing patterns of events, and of being able to generate hypotheses that may make recognizable patterns where none exist. Its passwords are "I wonder what would happen if . . . ," and "Maybe if I . . . ," and "Something doesn't seem right about. . . ." Its coat of arms is the question mark—a symbol unknown to logic. Here is where assumptions are made that can be operated upon logically.

Further, none of these three components is, in absolute terms, superior as a thought process to the other two. The true measure of intellect, rather, is the judicious choice of the proportions in which they are used in a given situation. At any given time we mix certain amounts of Logic, Emotion and Intuition to do our thinking. Thus:

$$k_1\mathbf{L}+k_2\mathbf{E}+k_3\mathbf{I}=\text{Intellect}$$

This is in the form of a vector, and a word about vectors is in order. The characteristic of interest here is that they are made up of independent, orthogonal components, which is to say that any of the components may be changed arbitrarily without influencing the others. As an example for those not familiar with this part of mathematics, and for those who remember only in what year they studied it, take the case of locating your car relative to your house. It can be described as thirty miles to the northeast, and the arrow connecting the house to the car is a vector. It can be broken down into its components of twenty-one miles east and then twenty-one miles north. As the car moves relative to the house, the vector's length and direction change, and both its components change correspondingly. If the car is now restricted to an east-west direction, the length and direction of the vector will change, but the length of its north-south component will have to stay the same. No matter how you move east or west, you don't change your distance north.

And my argument is, that no matter how you operate with one of the com-

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received the Bachelor of Applied Science in Engineering Physics from the University of Toronto in 1951. From 1951 to 1953 he was a Research Engineer with Ferranti Electric in Toronto, working on a digital communication and display system. In 1953 Mr. Kleinberg joined RCA as an Engineer in Camden, New Jersey. He was assigned to the newly organized Commercial Computer activity which at that time was the New Business Department of Engineering Products Division. He was a logic designer on the Bizmac computer, RCA's first delivered commercial computer. Subsequently Mr. Kleinberg was appointed Engineering Group Leader on the RCA 501, first of the transistorized computers; later he became Project Manager of the RCA 301 computer. Transferring in 1962 to the Palm Beach Gardens plant as Manager, Engineering, he had responsibility for many elements of the Spectra Product Line, including three of the computers and much of the peripheral system. In 1969 Mr. Kleinberg returned to Camden as Manager, Camden Engineering with responsibility for the 70/60 computer design, communication systems, and design automation.

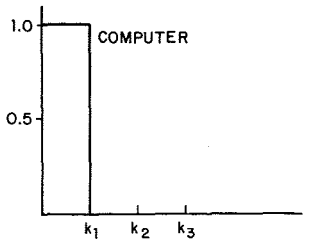

Fig. 1—Constants of Logic, Emotion, and Intuition for a computer.

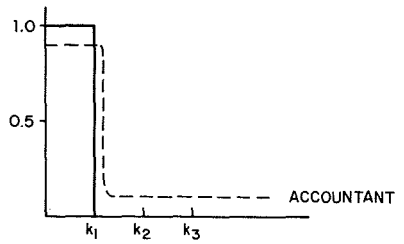

Fig. 2—Constants of Logic, Emotion, and Intuition for an accountant.

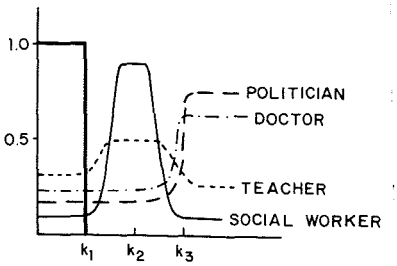

Fig. 3—Constants of Logic, Emotion, an Intuition for several professions.

ponents of intellect, you can't move on the other two. A computer program, no matter how complex, must eventually be run on hardware that is capable only of rigidly logical operations. It is activity strictly in that one component. You don't reach an intuitive conclusion using logical steps. You don't reach a logical conclusion using emotional steps.[1] But your intellect, as applied at any given time, is a vector sum of these components.

We will now attempt to use this simple concept to describe the intellect of a computer, and several types of people. Hopefully this will yield a measure of "computerizability" for each. Please bear in mind that we are concerned only with the intellect involved in carrying out one's work. During off-hours an entirely different set of values takes over.

One last constraint. We are not attempting to measure absolute intellect, but rather to indicate proportions, so we scale the size of the elements, such that the Logic, Emotion and Intuition components always add up to the same value—in this case, 1. So:

$$k_1+k_2+k_3=1$$

For those who care that the length of a vector has square roots of sums of squares in its equation—don't worry. Mathematical rigor is nice, but not when I'm operating on the Emotion axis.

First, the values for a computer. It is capable of performing only logical operations. Its emotional and intuitive components are nil. So the constants are obviously, $k_1=1$, $k_2=0$, $k_3=0$. This is shown in Fig. 1.

The constants that we now give for people are based on hundreds of months of studious, bewildered, fascinated, amused, horrified and, above all, interested observation. I invite argument, but have no scientific basis for defending them.

Accountants:

Logic (k_1) = 0.90
Emotion (k_2) = 0.05
Intuition (k_3) = 0.05

This is superimposed over the computer graph in Fig. 2. The close match indicates that much of an accountant's work is "computerizable". How about that?

To take another profession:

Engineer, inexperienced:

Logic (k_1) = 0.8
Emotion (k_2) = 0.1
Intuition (k_3) = 0.1

Engineer, experienced:

Logic (k_1) = 0.5
Emotion (k_2) = 0.1
Intuition (k_3) = 0.4

It is left as an exercise to the reader to determine whose work is more computerizable. And what else is "experience" but the proportional growth of one's intuitive ability?

As a sample of more such readings, the following chart is offered. These are plotted in Fig. 3.

	k_1 Logic	k_2 Emotion	k_3 Intuition
Social worker	0.05	0.90	0.05
Politician	0.15	0.15	0.70
Doctor (diagnostic)	0.20	0.20	0.60
Teacher	0.30	0.50	0.20

The implications here are that, by my reckoning, a computer can be used to do about 20% of a doctor's diagnostic work, and about 30% of a teacher's actual teaching work.

This test of our intellectual match with a computer is really a special case of the general question of communication. We take as a premise that no communication (do not confuse with "agreement") can exist if the communicators are on different axes. That is, if *A* is talking on the Logic axis, and *B* is listening on the Emotion axis, communication is zero. In more mathematical terms, maximum communication between two intellects is the *dot product* of two vectors, or the sum of the products of the components.

As an example, a politician and an engineer (experienced) have factors o 0.15, 0.15, 0.70 and 0.50, 0.15, 0.3 respectively. The communication be tween them can only be:

$$(0.15)(0.50)+(0.15)(0.15)+(0.70)(0.35$$
$$=0.08+0.02+0.25=0.3$$

They can communicate, at best, onl 35% of the time. Similar factors ca be worked out for any desired com bination.

The best communicators are those wh discard their own factors, and some how manage to recognize and adop those of the other person. In this case communication can approach the ideal of 1. But when you communicate with a computer, you had better stay on that logic axis!

Why bother to present this theory o computers and intellect? In an effort to jolt some simple thinking into an industry that has had too much of the complex, especially with regard to where our product can go, and what it's capable of doing.

Am I predicting that computers will always be logic machines and no more? As long as they are built on today's principles—yes. Any computer that goes beyond logic will be based on concepts, and devices not yet implemented, and probably not yet discovered. If the Emotion and Intuition components ever get mechanized, we'll be able to talk honestly about thinking machines. They'll be great, creative gadgets — unless they also become bored, forgetful, selective of the jobs they'll accept and restless when the moon is full.

Footnote

1. We often mask this truth by giving things names to suit our purpose. For example, "The Law of Supply and Demand" sounds detached, cool and rational, and obviously belongs on the Logic axis. But it is only a euphemism for "people are basically greedy," which sounds involved, judgmental and prejudiced—in a word, emotional. Whether it is true or false is not the issue, but it should be recognized as an assumption about people and it belongs on the Emotion axis. This is true of all ideological starting points.

Stored program circuit switching

W. Lawrence

Circuit switching systems such as the telephone network in this country and foreign exchanges abroad have existed for some time. It has only been in recent years, however, that control of these vast reliable communications networks is slowly progressing from electro-mechanical devices to special-purpose stored-program control equipment. This article describes a small stored-program shipboard telephone-circuit switch built for the United States Navy. A brief description of the system configuration is presented and a more detailed look is offered at some of the subscriber features and programs provided in the software package.

THE INTERIOR COMMUNICATIONS SYSTEMS (ICS) is the nerve system of a Naval ship. The effectiveness and efficiency of communication is of prime importance in contemporary shipboard operations. There is a constant flow of information and data which forms the basis for every decision and command at every organizational level. The combat effectiveness of every vessel in the fleet is profoundly affected by the quality and utility of the Interior Communication System.

Systems in current use consist of many independent circuits utilizing communication techniques and devices developed in the 1930's. These separate circuits can be classified into four basic devices:

Sound-powered telephones
Two-way intercoms
Dial telephones
General announce or one-way intercoms

Most of these devices are so interconnected so that all potential users of a particular function will have that function available to him in his normal workspace. To accommodate this, an enormous amount of cabling is required, ranging from 60,000 to 500,000 feet depending on class of ship. Such cabling systems have not changed substantially since the 1930's and are an inflexible and inefficient constraint of the constantly expanding ship's communications requirements. Such systems are completely inflexible to any refinements, modifications or improvements to the ship's communications needs, often involving major retrofit costs.[1]

Reprint RE-16-3-19
Final manuscript received September 9, 1970.

In late 1963, the Navy initiated a feasibility study with RCA to determine the overall communications requirements for Navy Ships with a goal toward developing a single integrated communication system. The study resulted in a feasibility model and later a development model of an Advanced Interior Communication System (AICS) utilizing a centralized switch controlled by a stored program processor.

The development model was delivered in early 1969 and is currently installed and operating on the *USS Bunker Hill* in San Diego. In November 1969, RCA was awarded a production contract for nine AICS Ship Systems.

Each system has over 700 subscribers. The advantages of this AICS system to the Navy are as follows:

1) Flexibility of operational features, such as net calls, line hunt, local calls, call forwarding, restricted calls, conference calls, automatic self-test, shore telephone calls, and priority override.
2) Up to 75% reduction in cables and cable installation.
3) Reduced number of terminals and personnel attendents.
4) Interface capability with several other communications systems, including shipboard CCTV, man-on-the-move, shore telephone, ship's radio system, and ship's general announce system.
5) System cost effectiveness when compared with a conventional hardware system.

The Interior Communications System has proven to give great performance advantages and cost savings above the conglomeration of systems presently in use because of the more efficient utilization of equipment.

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received the BSEE from Villanova in 1958 and the MSE from the University of Pennsylvania in 1965. Mr. Lawrence joined RCA in 1958, working in the automatic test equipment design activity. From 1962 to 1964, he designed communications test equipment and performed system integration for Dynasoar ground support equipment. From 1964 to 1965, as part of the Digital Communications Group, he designed digital transmitters, receivers, teletype buffers, and adapted computers to circuit switching applications. In 1966, he was the principal investigator on an IR&D program to adapt Spectra computers for circuit switching tasks. From 1967 to 1969, Mr. Lawrence was project engineer for the AICS circuit switch software package. In 1969, he became logic design project engineer for the LHA-ICS program and, in 1970, was named to his present position.

System Configuration

The Interior Communications System (ICS) is primarily a voice network with a reed-relay space-division matrix capable of passing DC to 100 kHz. Subscriber's terminals are touch-tone telephones with several variations in keysender panels corresponding to function and location.

The system consists of two centers (Fig. 1) physically separated for vulnerability considerations, each servicing approximately half of the subscribers on board. Under emergency conditions, each center is capable of accommodating other subscribers normally serviced by the other center. Each center operates independently and is connected to the other center via trunks and net "interties." A net is a common bus which may be accessed by subscribers with a common function. The net "intertie" is a dedicated hardware connection between centers allowing subscribers in both centers to access the same net. Trunk

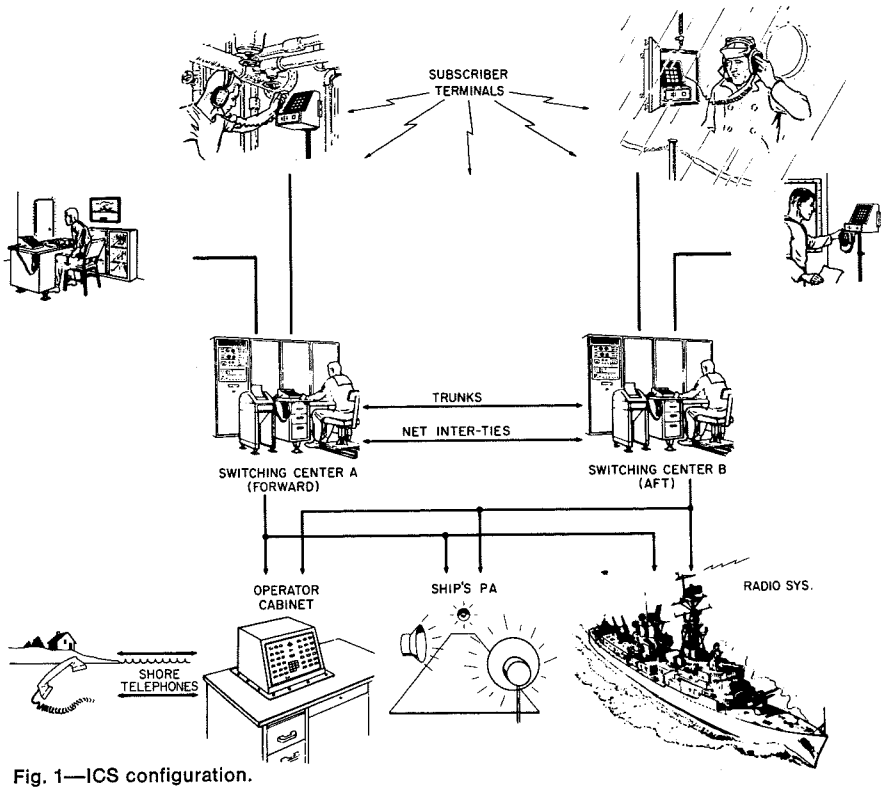


Fig. 1—ICS configuration.

lines are randomly selected on a per-call basis, for the duration of the call, and connect subscribers in both ends of the ship.

Each switching center (ICSC), Fig. 2, contains two RCA CSP-3 processors for reliability considerations, either one capable of controlling the center. The basic CSP-3 contains an 8192-word, 24-bit (with parity bit), 2-μs memory. Addressing of up to 32 kilobits of memory is provided. [The methods for synchronizing the two processors are described in detail in another paper in this issue.[2]]

Under emergency conditions (either center incapacitated) the operating center, via a single manual switch closure, may provide local service to preselected subscribers in the inoperative center over the trunk lines and net interties connecting the two centers.

Each switching center is supplied from ship's power but each contains dual power supplies and battery back-up systems allowing complete and uninterrupted operation for 1 hour in case of a ship's power failure or failure of either battery source. This duration can be extended with additional batteries; however, the Navy does not require it due to redundant prime power sources on board most ships. Switchover to battery power is automatic if ship's power fails.

Redundancy is provided for all critical common equipment. The two processors in each center provide control redundancy and reliability. Receiver/senders (R/S) are redundant by nature since the number supplied is based on traffic considerations. Should one fail, the other units can handle the traffic at reduced efficiency until the failed R/S is repaired. The matrix is also redundant by design since multiple paths are available to complete any call. Failure of circuitry in the matrix can cause loss of service to a single terminal or group of terminals but does not incapacitate the system.

The ICS uses common terminal equipment and cabling. In current shipboard communications systems, the equipment and cabling varies from subsystem to subsystem. Interface incompatibility of these subsystems limits the flexibility and overall efficiency of communications. The ICS is adaptable hardware wise and software wise to changing needs and technology.

Each switching center contains a paper (mylar) tape reader for program-tape or maintenance-test-tape loading. A teleprinter is also provided for maintenance, status, memory dump, and terminal table printouts. A single switchboard is supplied in one center providing a ship-to-shore interface when the ship is in port.

For smaller ships, where two centers and two processors per center are not economically feasible, designs are cur-

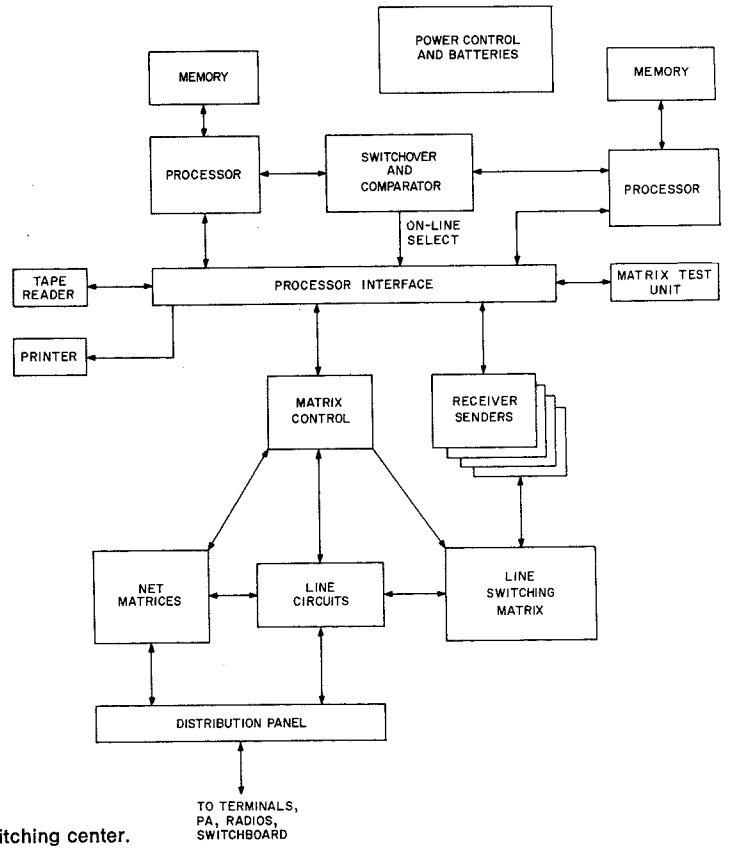


Fig. 2—Switching center.

rently underway to solve both the reliability and vulnerability problems. These include two centers, with only one processor per center, operating in synchronism and a single center with two processors operating in synchronism, with adequate fall-back capabilities to sound-powered nets and emergency intercom circuits in case of major battle damage.

Construction

Mechanically the system is housed in standard Navy racks (Fig. 3). The dual processors, switchover unit, control (maintenance) panel, tape reader, and peripheral interfaces are contained in the common control rack. Each matrix rack houses up to 256 lines in the current designs.

The processor

The CSP-3 (Fig. 4) is tailored specifically for circuit-switching applications. It is a single-address machine utilizing 26 instructions with a capability of expanding to 64 instructions. The instructions are bit orientated with variable-mask fields suitable for table interrogation and modification. The bulk of the instructions used in the operational programs consist of the load and store class plus the logical operations, such as AND, OR, NEGATION, etc., although certain instructions are specifically used for I/O comparisons and to aid in synchronism.

The processor I/O circuits are built to interface directly with circuit-switching hardware. Individual machine registers such as the data register output (DRO), command register (CR), and link register (LR) accept data over the major transfer bus (MTB) and pass it on to the matrix, R/S, etc. A special tape input register (TIR) and parallel-to-serial circuitry interface with the tape reader and teleprinter. Digital-transistor-logic (DTL) integrated circuits are used throughout the machine.

Subscriber features

In addition to providing a direct connection between any two telephone terminals on board ship the ICS stored program approach provides the following features:

Abbreviated addressing (AA)—The ability of selected subscribers to key a single button and be connected to any frequently called subscriber or net.

Four digit dialing—The ability to key four digits and be connected to any terminal on board ship.

Restricted access—The ability to limit selected terminals from calling other terminals thus providing executive right-of-way for high priority traffic.

Call forwarding—The ability of selected terminals to temporarily forward their calls to another destination.

Override—The ability of selected subscribers to override or "break-in" to existing connections on demand.

Radio and public announce access—The ability of selected terminals to connect directly to a ships radio or public address system via 4-digit dialing.

Conferencing—The ability of selected terminals to dial directly a number of random subscribers into a conference call.

Shore interface—The ability of selected subscribers to dial *O* and reach shore telephones when in port via the ship switchboard.

Hunt not-busy groups—The ability to automatically reach any idle terminal in a common location or functional activity of interest by dialing one 4-digit number.

Emergency reporting—The ability to receive automatic override service to predetermined locations when an emergency number is dialed.

Line load control—The ability to limit certain subscribers from generating calls, thus adding to system congestion, during abnormal traffic overloads.

Net access—The ability of selected terminals to dial, via abbreviated address or 4-digit dialing, into a net or "meet me" conference and converse with up to 30 other subscribers.

Command-net origination—The ability of selected subscribers to key in a command net code via abbreviated addressing or 4-digit dialing which will automatically ring and connect up to 30 preset subscribers into a net.

All of the subscriber permits, accesses, restrictions, etc., are contained in memory tables accessible in microseconds. These tables may also be modified "on-line" from a "maintenance terminal" which provides a dynamic man-machine interface for the system. Changes made by the maintenance terminal are accomplished via normal dialing, eliminate hardware modifications when terminal functions change due to a change in the ship's operational status, and provide a hardcopy record from the teleprinter.

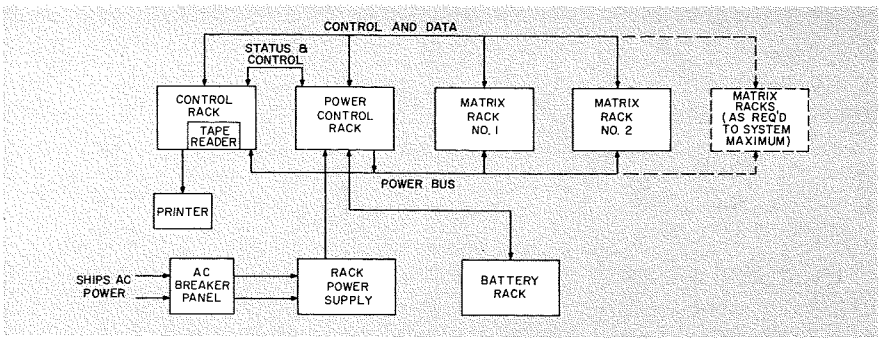


Fig. 3—ICS center rack configuration.

Software utilization

All decisions made by a switching center from the time a subscriber goes "off-hook" until he terminates the call are made by software. Hardware still provides hook status indication, tone generation and detection, and matrix connections, however, all of the hardware is controlled by software. All other hardware functions have been eliminated. Typical hardware functions now performed by software include:

1) Timing and counting functions—length of tones, length of dialing, number of digits dialed, etc.;
2) Hardware selection—idle paths in the matrix, common equipment, trunks, etc.;
3) Signaling tone validation—examination of the type and identity of keyed digits.
4) Number translation—correlation of a dialed number to an equipment location including AA, nets, and remote numbers.
5) Current status recording of all terminals and hardware;
6) Individual subscriber permits, accesses, etc.;
7) Generation of all I/O commands to operational hardware and utility equipment; and
8) On-line fault detection and status of all critical hardware.

Memory organization

The CSP-3 memory is divided into four functional areas:

1) *Work store*—current hardware and terminal status, print buffer, and scratch-pad memory;

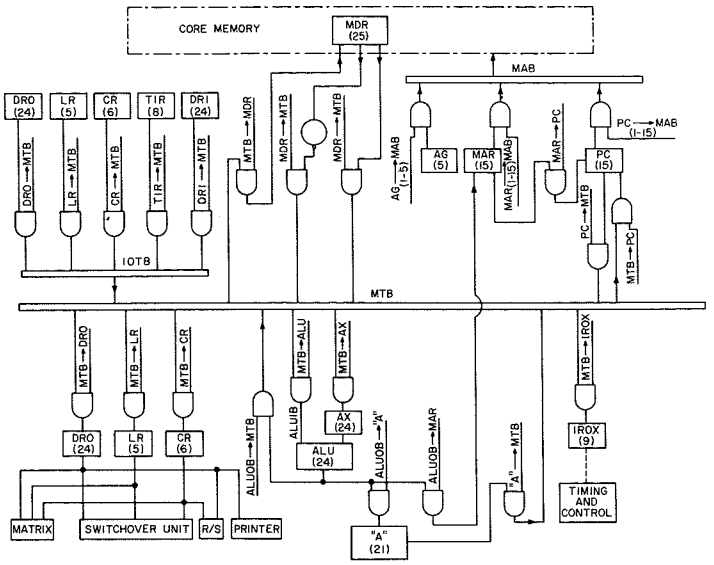


Fig. 4—The CDS-3 processor logic tailored specifically for circuit-switching.

2) *Terminal and equipment tables*—Directory numbers, permits, accesses, matrix location, etc—also AA tables, net access tables, HNB groups, etc.;
3) *Control program*—Program tables, conversion tables, constants, etc.—also all routines and subroutines required for operational control; and
4) *Test Program*—test programs required to semi-automatically or automatically exercize the hardware, change status or permits, make test connections, etc.

In the system delivered to the Navy, all the test programs supplied are located in core memory. An "on-line" tape-load routine is also provided, however, which enables storing additional tests, as required, on tape with automatic access from the maintenance terminal. This feature permits an almost unlimited test facility.

Control program organization

Executive routine

The executive routine (Fig. 5) controls the circuit-switch operation of ICS. The routine is basically an ordered sequence of events (questions) occurring constantly. High priority operational functions are performed first in a given pass through the routine prior to utility operations, testing, etc. The executive routine controls the entry into all other routines with the exception of the interrupt routine. The CSP-3 machine contains a single-level interrupt cycle occurring every 20 ms. At this time, the processor interrupts the normal routine and services all busy receiver senders (R/S). Receiver/senders are A-to-D and D-to-A devices connected to subscribers and trunks to receive or transmit dialed information and also contain supervisory-tone oscillators. When all busy R/S units are serviced, the program is re-entered at the point of departure.

Resynchronization routine

The resynchronization routine, first priority in the executive loop, is an apparent exception to the rule of operational functions before utility functions. However, resynchronization though it serves no direct useful subscriber demand, serves to bring a repaired machine "up-to-speed" with the "on-line" machine and transfers the work store or complete memory of the "on-line" processor (at the discretion of the operator) into the memory of the repaired machine. At the completion of resynchronization, the off-line machine, though still "off-line" is completely operational, running in synchronism with the on-line machine, and aware of all current switch activities due to the memory transfer. All other functions, including the interrupt cycle are temporarily postponed during resynchronization. The process requires approximately 400 ms when 8 kilobits of memory is transferred.

When a failed machine has been correctly repaired, the operator starts the machine in the resynchronization routine where the program will cause it to idle, waiting for the "on-line" machine. The operator then actuates a RE-SYNC switch on the system-status panel. In the next pass through the executive loop, the "on-line" machine will then recognize the request and initiate resynchronization. This procedure constitutes the utmost in simplicity and minimal operator intervention in bringing a center back to full operational capability.

Call-processing routine

The call processing routine processes all calls on an individual basis. Once the dialed data is received from a calling subscriber or trunk this routine determines the final disposition of the call and generates all commands accordingly. Most of the features which make stored program control superior and provide unrivaled flexibility to that of a wired programmed system are contained or performed in this routine.

Call processing examines the called number for a host of special cases such as operator requests, abbreviated addressing, test requests, emergency requests, call forwarding requests, and radio and PA requests. These tests are all preprogrammed and can be easily varied without hardware modification according to current procedures.

In the event one switching center is inoperative for any reason, the call processing routine in the operative center detects the condition. Trunk lines are recognized as extensions of remote subscriber terminal lines. These terminations are temporarily treated as local lines and afforded all the services (permits, etc.) they had in the other center for the duration of the emergency.

The call-processing routine translates all normal four-digit or AA dialing requests into the local hardware equipment location (location in the matrix). This includes line matrix appearances, net matrix identification, and idle hunt-not-busy group appearances. Any number not so located or not detected as remote (in the other switching center) causes the routine to send an unavailable tone to the calling party. Unavailable tone is also sent due to restricted calls. When the called party is busy and cannot be overridden call processing sends busy tone to the calling party.

For local calls that can be completed, call processing selects an idle path, initiates commands to make the connection, sends ring or override tone for the proper time, and updates all terminal and matrix status. For remote calls, call processing selects an idle trunk, connects the receiver sender involved to the trunk, and commands the unit to outpulse the dialed data.

At the termination of busy, override, and unavailable tones, the call-processing routine releases the receiver/sender and calling party connection and marks them idle in memory as well as the matrix path that was used. When any terminal or trunk does not dial, in the allotted time, the call processing routine generates commands to release the connection and updates the hardware status.

Any change in the handling of calls caused by a modification in the ship's operational procedure will usually affect the call processing routine. Changes to this routine or any other control routine can be made manually via the processor maintenance panel. These changes obviously can not be made while a machine is "on-line." Such changes require stopping the machine, altering memory (memory key lock enabled) and then restarting. This machine must now manually be switched to "on-line" so that the other machine can be loaded with the new program via the "resync" progress.

Scan routine

In a stored program machine line (terminal or trunk) call requests or release requests may not be recognized immediately. In ICS all lines are scanned every 200 ms. State changes are detected at these times and the proper action is taken. A request for service from an idle line will cause the scan routine to select an idle path in the matrix, select an idle R/S, generate commands for the connection, generate commands and timing data for the R/S to send dial tone, and mark the new status of all hardware in memory.

When a subscriber releases a call the scan routine interrogates memory to see who or what else was involved in the call and generates the proper release commands. All memory tables are updated.

Interrupt routine

The interrupt routine primarily handles the task of timing and validating dialed data. This includes recognition of tones received by an R/S, proper length of tone and interdigit intervals, table look-up for valid tone codes as opposed to noise, rejection of more than a two-tone combination (two buttons pressed at once), and insurance that dialing has been completed (proper number of digits, and/or buttons not continually depressed). This was previously done by hardware but the stored program control reduces an R/S to simply tone generators and detectors.

The routine generates and times duration of DTMF signalling tones when the R/S is outpulsing over a trunk and also the duration of supervisory tones. It recognizes requests for override and AA signalling and marks memory as required. When dialing is completed or aborted, as the case may be, the interrupt routine alerts the executive routine to enter the call processing routine on the next pass through the executive loop.

Test routines

The ICS contains a number of automatically and semi-automatically initiated on-line test routines. The tests are interlaced with traffic requests and lowest in priority. As mentioned previously, all tests are in core however the on-line tape load routine allows the test library to be expanded as required.

Automatic tests are initiated in two ways:

1) Confidence tests of the processor when a fault is detected or suspected.
2) Periodic timed tests of the common hardware such as the processor, R/S, switchover unit, and matrix.

The confidence tests are entered when the two machines fail to match an I/O instruction. Known answers are provided at the end of the test such that a processor failing to respond with the correct answer is thrown "off-line" with an audible alarm and print out. A detailed test and maintenance tape is provided together with manual diagnostic procedures in order to trouble-shoot the processor.

The periodic test routines are entered via the executive routine and submit the common hardware to a series of thorough step by step checks. Failure of any test generates the audible alarm and a printout of the test failure and symptoms.

Any of the automatic tests may be requested manually (semi-automatically) from the maintenance terminal as well as additional tests and status reports. "Dial-up" of tests requests is only recognized from the maintenance terminal. The procedure is similar to making any other type of call. Depending on the test requested the operator may re-dial up to three more times to feed enough information into the processor. All manual tests generate skip, error, and complete messages —depending on the status of the hardware at the time.

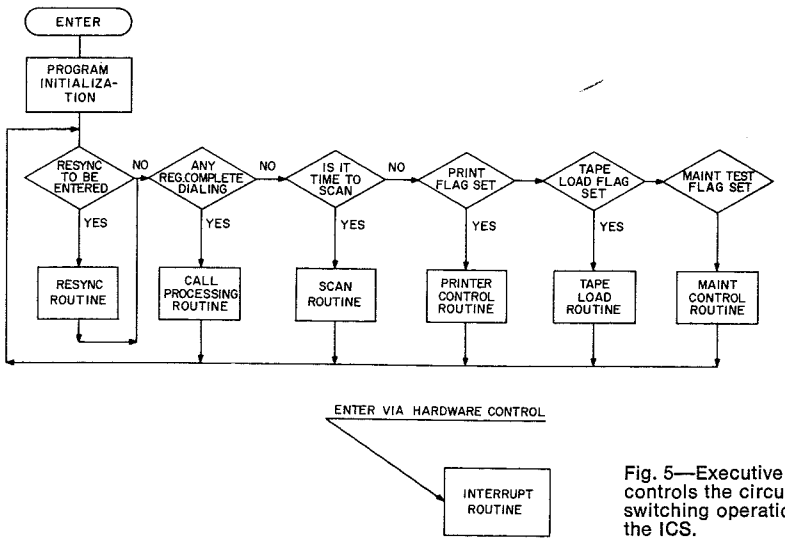


Fig. 5—Executive routine controls the circuit-switching operation of the ICS.

Conclusion

The advanced development model ICS system has been in the field undergoing customer evaluation for over a year now. Based on performance evaluation of this system, RCA now has the contract to provide ICS systems for the LHA class of ships. Proposals to further improve performance and interface features and to add the systems to new ship classes are in preparation.

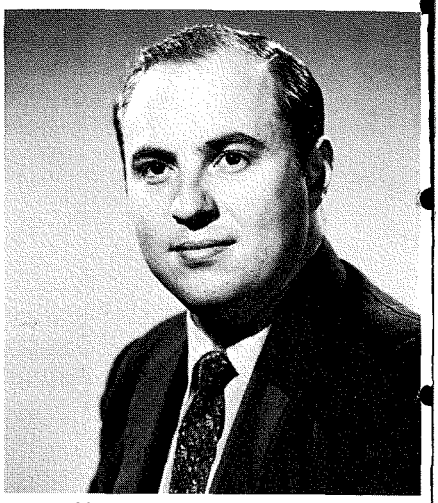
Reference

1. Humm, Paul F., "Interior Communications, Is It a Challenge?" *Naval Engineer's Journal* (Jun 1970).
2. Kleidermacher, M., "Synchronization of two processors," *this issue.*

Synchronization of two computers

M. Kleidermacher

In certain computer-controlled real-time systems, uninterrupted continuity of system operation is mandatory. An example is a computer-controlled telephone switching system for tactical military operations.[1,2] It would be unacceptable to permit a complete loss of telephone service when the control computer malfunctions. The system described in this paper uses a redundant computer operating in parallel with the on-line computer. In the event of a failure of the on-line computer, the redundant unit instantly assumes control of the switching system. The system provides a method of synchronizing the two processors, a method of detecting failures, and methods of preventing one processor failure from disabling both units.



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received the BSEE from the City College of New York in 1966 and has completed the course requirements toward the MSE at University of Pennsylvania. He joined the Digital Engineering group of the Communications Systems Division in 1966 and was involved in the design and test of the LFP processor for Minuteman. In 1967, he joined the telephone switching group where he was responsible for design of the CSP-3A processor for use on the Advanced Development Model of the Interior Communications System (ICS). Since 1969, he has been project engineer of the logic group developing the ICS processor for the LHA program. Mr. Kleidermacher has been involved with the Continuing Engineering Education program, lecturing in logic design and applications. He is a member of the IEEE.

TO PREVENT THE LOSS OF TELEPHONE SERVICE because of a computer malfunction, there are several approaches that can be taken. One RCA approach is to use a redundant computer which is provided with up-to-date information describing the current status of the system.

One method of providing the redundant unit with correct status information is to have it simultaneously execute the same program as the on-line processor. In this manner, its core memory is continuously updated to current data. Thus, in the event of a malfunction of the on-line unit, the redundant one can assume control immediately.

Description of the problem

Program synchronization and error detection

Two processors operating from independent clocks, but executing the same program will gradually drift apart. Therefore, it is necessary, at selected intervals, to insert a special function which delays the lead processor until the other catches up. Furthermore, if the redundant processor is to take over when the on-line unit fails, some means is required to automatically detect when a failure occurs.

A method of accomplishing both program alignment and error detection is to insert checkpoints at selected intervals. These *matchpoints,* are implemented so that:

a) A processor reaching a matchpoint will not proceed to the next instruction until the other processor reaches that point.
b) When both processors reach a matchpoint, certain data comparisons are made. If the two processors have independently produced the same answer, it may reasonably be assumed that both are functioning correctly. If they produce different results, an error has been detected.

Reprint RE-16-3-21
Final manuscript received September 9, 1970.

Interrupt synchronization

The processor (CSP-3) used by RCA has two types of hardware interrupts:

1) Memory interrupt, and
2) Program interrupt.

A memory interrupt occurs every millisecond, as determined by a hardware counter. When this interrupt occurs, the execution of program instructions is temporarily halted and a hardware cycle is started. The memory interrupt cycle fetches the contents of seven specific memory locations, increments their contents by one, and stores them back in the same specific memory locations. These memory words are used as elapsed-time counters by the operating program. At the conclusion of the memory interrupt normal instruction execution resumes.

A program interrupt occurs whenever the interrupt flag is set. The flag is set during the next instruction following a memory interrupt cycle, if the number-one elapsed-time counter reaches zero. A program interrupt causes the sequential execution of instructions to be stopped and a hardware cycle is entered. In the program interrupt cycle, the current setting of the program counter and several key indicators are stored. The program counter is then reset to the location of a special interrupt program. The interrupt program is then executed. When it is completed, the program counter is reset to the value previously stored during the program interrupt cycle, and normal program sequence is resumed.

Since the memory interrupt cycle occurrence is determined by a hardware counter, it is asynchronous with respect to program execution. That is, a memory interrupt may occur between any two instructions. Since the program interrupt cycle is initiated by the memory interrupt cycle, the program interrupt is likewise asynchronous with respect to the program. However, during the execution of the main program, decisions are made on the basis of the contents of elapsed time counters. The results of the decisions are, therefore, dependent on the exact point in the program at which the interrupt cycle occurs.

In the system under discussion, the two processors are operated in synchronism via the matchpoints. However, they may differ by a few instructions due to their independent clocks. Consequently, if they are always going to make the same decisions at program branch points, it is essential that the interrupt cycles occur at precisely the same point in the program instructions in both processors. However, since the two interrupts are asynchronous with respect to

the operating program, some means must be provided to control them.

The method devised for this system is to keep a counter of the number of instructions performed by each processor. When an interrupt occurs, the on-line processor is allowed to execute it. The off-line machine, however, is not permitted to execute the interrupt until the instruction counters indicate that the same point in the program has been reached.

Detail implementation

Master/slave relation

As explained above, interrupt synchronization requires that both processors enter interrupts from the same program point. However, the implementation requires that one processor be used as a standard against which the other is controlled. A master/slave relationship is established, with the on-line unit designated the master, and the off-line processor considered the slave. For control purposes, the hardware is arranged so that the master always performs its instructions and interrupt functions first. The slave is always slightly behind—but, at most, only by a few instructions.

The system is completely bi-directional; i.e.—when both processors are working, either one can be the master, and the other the slave. The decision is made by a selector switch on the system control panel. Fig. 1 shows a block diagram of the total control system. A switchover unit receives key inputs from each CSP-3 processor, and returns control signals to each to maintain synchronism.

Matchpoint implementation

The matchpoint function discussed previously is implemented by a special CSP-3 instruction designated MAT. When a processor reaches a MAT instruction, it sends a ready-to synchronize (RTS) signal to the switchover unit. In addition, the MAT instruction supplies data to both the switching matrix and the switchover unit for comparison and error detection. When both processors have arrived at a MAT instruction, the switchover sends back a signal indicating that the compared data is the same (GO) or different (NO GO).

The hardware of the MAT instruction allows a three-way branch:

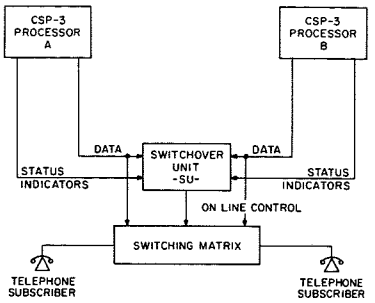

Fig. 1—System block diagram.

1) If a GO is received, the program counter is advanced by 2. This permits the processor to continue the normal program.
2) If a NO GO is received, the program counter is advanced by 1. This causes a jump to a diagnostic program, since it indicates an error.
3) If neither signal is received, the program counter is not advanced at all, causing the MAT instruction to be repeated. This condition arises when one processor reaches a MAT, but the other has not yet reached it. By repeating the MAT instruction, the on-line processor stalls until the off-line machine catches up.

The MAT instruction signaling between the processors and the switchover unit is illustrated in Fig. 2. If both RTS signals are present, the comparator indicates matched data, and a GO signal is generated. If both RTS signals are present, and the comparator indicates a mismatch, then the NO GO signal is generated, and diagnostic indicators are set.

Count-equal

As described previously, interrupt synchronization requires that a count of instructions performed be kept to insure that interrupts are entered from the same program point. For this purpose, the switchover unit contains an instruction counter-comparator as shown in Fig. 3. Each processor sends a pulse to the switchover unit indicating that a new instruction has been started. This pulse increments the counter for that processor (A or B). A stage-by-stage exclusive—OR comparator verifies whether an equal number of instructions have been started, resulting in a COUNT EQUAL signal. Initialization of the instruction counters is accomplished when a MAT instruction is reached. At that point, the concurrence of the RTS signals verifies that both processors are at the same instruction, and the counters are reset.

The comparator's function is to determine the difference between the

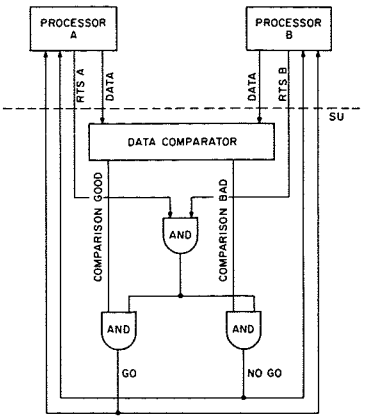

Fig. 2—Matchpoint control block diagram.

number of instructions performed by the two processors, rather than the absolute number performed by each. In this system, timing considerations showed that the differences would never exceed three instructions.

Interrupt synchronization

The essence of interrupt synchronization is that the off-line processor begins the interrupt only after it completes the same instructions that the on-line processor did when it entered the interrupt. For this purpose, interrupt synchronization logic is required in the switchover unit.

The control flip-flop is set when the on-line processor begins a memory interrupt. When the instruction counters indicate that the same number of instructions have been completed (COUNT EQUAL), the ENABLE INTERRUPT signal is sent to the off-line machine. Without this signal, the processor will not execute the interrupt. The enable signal for the on-line machine is always on. When the off-line machine begins the interrupt, it resets the control flipflop, thereby resetting the logic for the next interrupt.

The memory interrupt logic is shown in Fig. 4; similar logic is used to control entry into program interrupts.

Synchronization

Two problems remain with the synchronization implementation:

1) The master/slave relation requires that the off-line machine remain slightly behind. What happens if its master clock is slightly faster and it catches up?
2) When the on-line machine executes an interrupt, the off-line machine must wait for count equal. But if the on-line machine completes the interrupt before count equal is reached, then it will resume instruction execution and advance its instruction counter. This would destroy the count-equal reference for the interrupt.

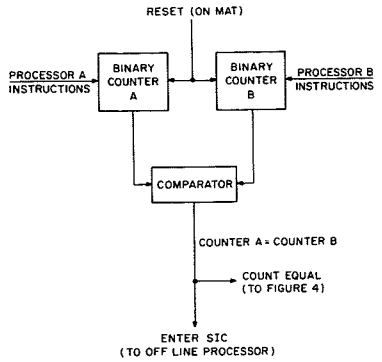

Fig. 3—COUNT-EQUAL logic.

To solve these problems, a new synchronization implementing cycle (SIC) was added to the processors. [In this context, machines cycles are sub-instruction functions such as instruction access cycle, instruction execution cycle, indexing cycle, etc.].

The synchronization implementing cycle is used as a non-function stalling cycle for synchronization timing. No computations are performed on this cycle. The cycle is entered at the end of an instruction if the switchover unit sends an ENTER SIC signal to the processor. The processor cannot begin another instruction until the ENTER SIC signal is removed. The processor can, however, enter a program or memory interrupt cycle if necessary.

The synchronization implementing function is used to solve the two problems stated above as follows:

1) If the COUNT EQUAL signal is present (Fig. 3), then the off-line processor has "caught up" and an ENTER SIC signal is sent to the off-line processor to prevent it from executing any further instructions. The off-line machine then enters the synchronization implementing cycle and remains there until the on-line processor begins the next instruction, thereby advancing its instruction counter and removing count equal. This, in turn, removes the ENTER SIC signal to the off-line machine which is now free to execute the next instruction.

2) When the interrupt control flip-flop (Fig. 4) is set, an ENTER SIC signal is sent to the on-line processor. When this processor completes its interrupt function, it stalls in the synchronizing interrupt cycles rather than continuing with the next instruction. This preserves the instruction-count reference at the point from which the interrupt was entered. When the off-line machine reaches this point, COUNT EQUAL will occur, enabling the off-line machine into the interrupt. This will reset the interrupt control flip-flop, thereby removing the ENTER SIC signal to the on-line processor, which is now free to resume instruction execution.

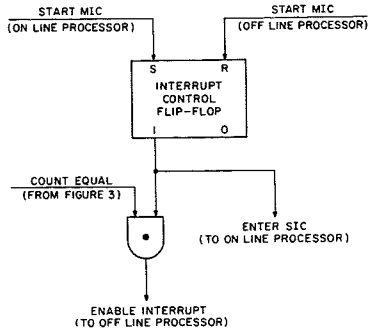

Fig. 4—Interrupt synchronization control.

Fault protection

The purpose of the system described above is to maintain continuous operation of the system by having a redundant processor ready to assume control. However, due to the synchronization, certain failure modes are able to cripple both processors. In particular, the synchronization implementing cycle is used to stop one processor until the other advances to some expected point. But suppose there is a failure, and the expected advance never comes? The working processor is stalled in the cycle, and neither processor operates the system.

Similarly, a matchpoint instruction causes one processor to wait for the other to "catch-up". If the 2nd processor never arrives at the matchpoint, again, one processor is defective and the other is stalled in waiting.

Finally, the interrupt mechanism requires that the on-line unit enter first. Suppose the on-line unit never executes an interrupt due to a failure. The processors will not be stopped, but no interrupt functions are being performed and the system is not being properly controlled. The good processor (off-line) would perform interrupt functions if it could, but it is prevented from doing so by the lack of an ENABLE INTERRUPT signal (Fig. 4.)

Synchronization timeout

To prevent the possibility of a single failure disabling both processors, timeouts are provided in the switchover unit. Whenever an ENTER SIC signal is sent, a timer is started in the switchover unit. If the timer expires, a fault alarm is registered; the fault is assigned to the processor that is not in a synchronization implementing cycle. For example, if the on-line machine is being held in a synchronization implementing cycle waiting for the off-line machine to reach an interrupt, and the timer runs out, then the off-line machine is deemed faulty since it failed to reach the interrupt. Once the fault is assigned, the other processor is put on-line (if it is not already on-line), and all *synchronization control signals* (ENTER SIC, ENABLE INTERRUPT, etc.) *are overridden.* This allows the working processor to operate the system independently without regard for the faulty redundant unit.

Matchpoint timeout

A similar timeout is begun whenever one processor signals it has reached a matchpoint instruction by the RTS signal (Fig. 2). If the second processor does not reach the matchpoint within a reasonable time, the timer expires and assigns a fault to the processor which has not reached the matchpoint. The good processor is now allowed to proceed independently as before, since all the matchpoint instructions automatically produce an instantaneous GO response once a failure has been registered.

Interrupt timers

To protect against failure of the on-line unit to interrupt at all, a timer is run for each interrupt memory and program. These interrupts are known to occur at regular intervals, hence a timer can be set. If the timer indicates an improper rate (high or low), of either interrupt function, a fault is assigned to that processor, and the other is put on-line.

Summary

The switchover and control scheme described here applies specifically to the CSP-3 computer. The matchpoint design can be applied to any general purpose computer. However, for machines with multiple interrupts, the scheme described here is costly since interrupt synchronization would be needed for every interrupt. For these machines, a different synchronization scheme would have to be implemented.

Acknowledgements

W. J. Lawrence, R. M. Zieve, M. Rosenblatt, and C. Magginiss were responsible for much of the design of the described system. In particular, the writer thanks R. M. Zieve who contributed parts of this paper.

References

1. Lawrence, W. J., "Stored program circuit switching," *this issue.*
2. Humm, Paul F., "Interior Communications. Is It a Challenge?" *Naval Engineer's Journal* (Jun 1970).

Rearrangement algorithm for switching systems

K. Weir

This paper presents an algorithm for rearranging connections in three-stage switching systems (rectangular or folded secondaries) so that additional desired connections can be accommodated or so that the system grade of service (probability of blocking for a given traffic density) is enhanced. The technique requires memory for storage of connectivity and the rearrangement algorithm itself; however, many current switching systems utilize computers and therefore the algorithm is amenable to those type systems.

SWITCHING SYSTEMS consist of terminations (or subscribers), control units, and switching matrices which, taken together, allow communication. Of specific interest is the switching matrices or the arrangements of crosspoints and transmission links which allow subscribers or sets of subscribers (in multiple-address messages or conference calls) to be interconnected in various combinations. Enough crosspoints can be provided in a switching system such that any idle pair of subscribers can be interconnected. Such a system is called a nonblocking system. However, because the probability of all subscribers making calls simultaneously is low and because the switching system cost is proportional to the number of crosspoints, real systems are designed with blocking, or they have a probability of blocking greater than zero. An alternate method to increasing crosspoints and thereby decreasing the probability of blocking is to provide for crosspoint rearrangement. The probability of blocking, or the fraction of calls that cannot be completed, is therefore an important parameter in switching systems and provides a basis for comparison of different systems.

Rearrangement requires memory (or knowledge of existing system connectivity) and it also requires an algorithm for rearranging connectivity. Since current switching systems utilize computers to establish connections and/or for the storage and forwarding of messages, rearrangement seems to offer several potential advantages. If a rearrangement algorithm exists, one could trade off the cost of the estimated programming effort and computer memory required for implementation versus the cost of increased crosspoints. This is because the same blocking probability can be achieved with less crosspoints through rearrangement.

Reprint RE-16-3-20
Final manuscript received September 9, 1970.

Example of rearrangement

A simple example of rearrangement for a three-stage folded matrix with eight subscribers is shown in Fig. 1. Before rearrangement, the existing connectivity is between subscribers B and C and between subscribers E and H (as indicated by the circled or activated crosspoints). If idle subscribers D and F wish to be connected, it is easily seen that there is no secondary switch crosspoint available to complete the connection. Part B of Fig. 1 shows that by rearranging the connection E-H in secondary switch 1, the blocking condition for connection D-F is removed and it can now be established on the mutually idle crosspoint of secondary switch 2.

It is interesting to note in this example that judicious selection of the secondary switches might have circumvented the rearrangement problem. If a procedure were followed of always trying to make a new connection on secondary switch #1 (packing) before trying to make a connection on secondary switch #2, rearrangement would not have been necessary in this example. However, once calls are in progress, requests for termination occur more or less randomly, thereby yielding all possible combinations of connections even though they may have been selected in a prescribed pattern. Therefore, if a selection scheme as described above were used, it would also be necessary to try to rearrange connections when calls were terminated.

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Rearrangement algorithm

The selected method of representing connectivity will be the following three numbers representing a call from primary switch Y to primary switch Z through secondary switch X:

X	Y	Z
secondary	primary	primary

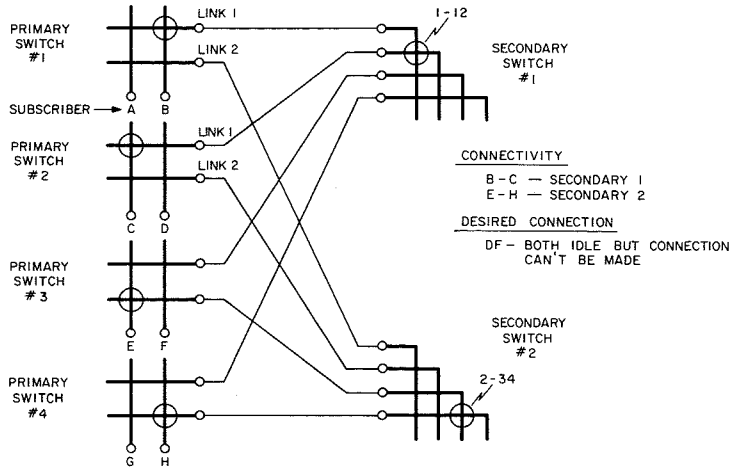
If at any time a desired connection cannot be made, try to rearrange connectivity using the algorithm described below:

Step 1) Determine whether or not rearrangement is possible. This is accomplished by the following steps:

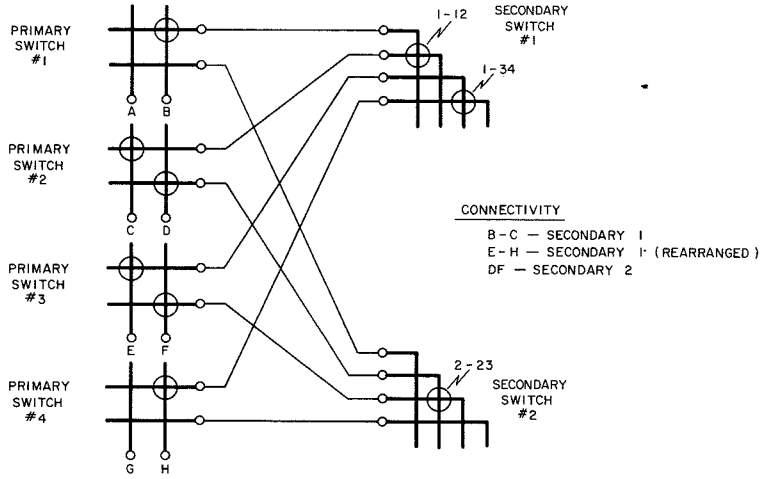
1a) Compare the number of current connections with the maximum possible number of connections; if they are equal, rearrangement is impossible because all secondaries are full. For an even number of links, (connections between primary and secondary matrices) the maximum number of connections, N, is

$$N = (kl + m)/2$$

where k is the number of links, l is the number of primaries, and m is the current number of intra-primary connections.



a) Before rearrangement



b) After rearrangement

Fig. 1—Example of rearrangement.

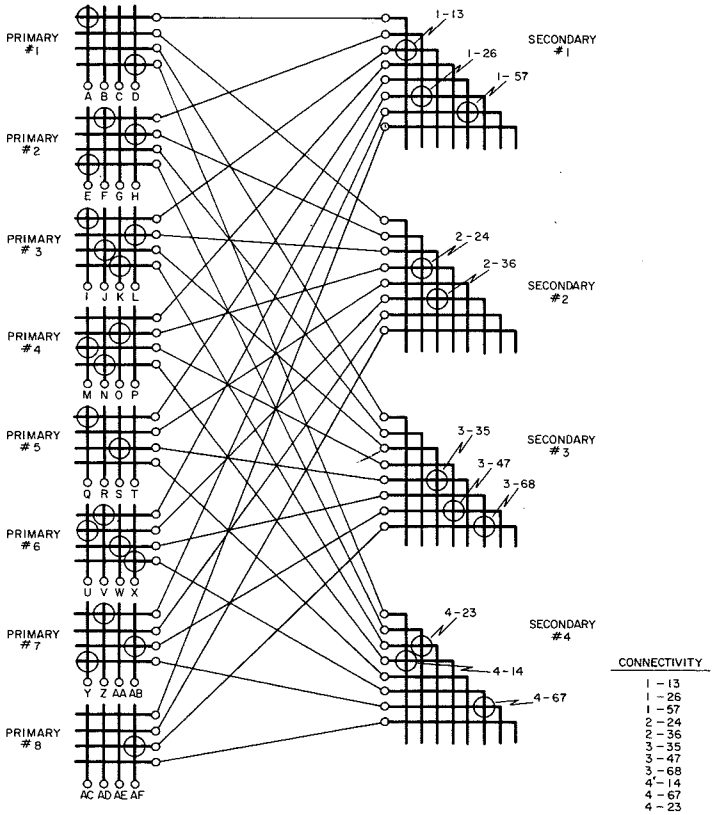
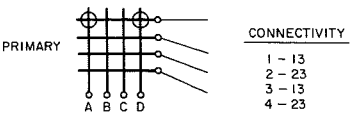
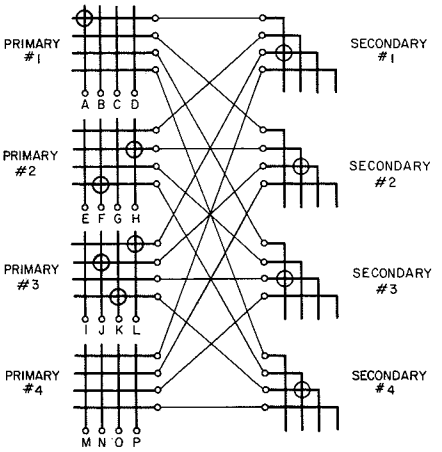


Fig. 3—Connectivity before rearrangement. *Desired connection:* X-14 (idle subscriber B to idle subscriber P) every secondary has either primary 1 or 4 blocked.



SUBSCRIBER A CONNECTED TO SUBSCRIBER D ON SAME PRIMARY

a) Intra-primary connection



b) Common-primary blockage

Fig. 2—Intra-primary connections and common primary blockage. *Desired connection:* X-12 (or idle subscribers C and E); there is a common primary (primary 3) to primary 1 or 2 on all secondaries; therefore, no connection can be made.

For an odd number of links, where $m \leq k$,

$$N = [l(k-1) + m]/2$$

For an odd number of links, where $m > k$,

$$N = [l(k-1)/2] + k + [(m-k)/2]$$

If the current number of connections is less than the maximum continue to step 1b.

1b) Determine whether either of the primaries in the desired call are blocked. If the number of current calls from either of the primaries which would be used in the desired call is equal to the number of links, rearrangement is not possible because of a blocked primary. If neither primary is blocked, go to step 1c.

1c) Determine whether an existing connectivity pattern blocks rearrangement. If there is a common primary to either of the desired primaries on all secondaries, the desired connection is blocked and rearrangement is impossible, as shown in Fig. 2. If there are more links than subscribers per primary, these checks are unnecessary.

If steps 1a through 1c above do not block rearrangement, rearrangement is possible.

Step 2) Select the lowest numbered secondary with the minimum number of connections and only one of the desired primaries in use.

Step 3) Make the desired connection, primary to primary, on the secondary selected in step 2 as follows:

selected secondary	primary	primary

At the same time, break the connection to that secondary which is now

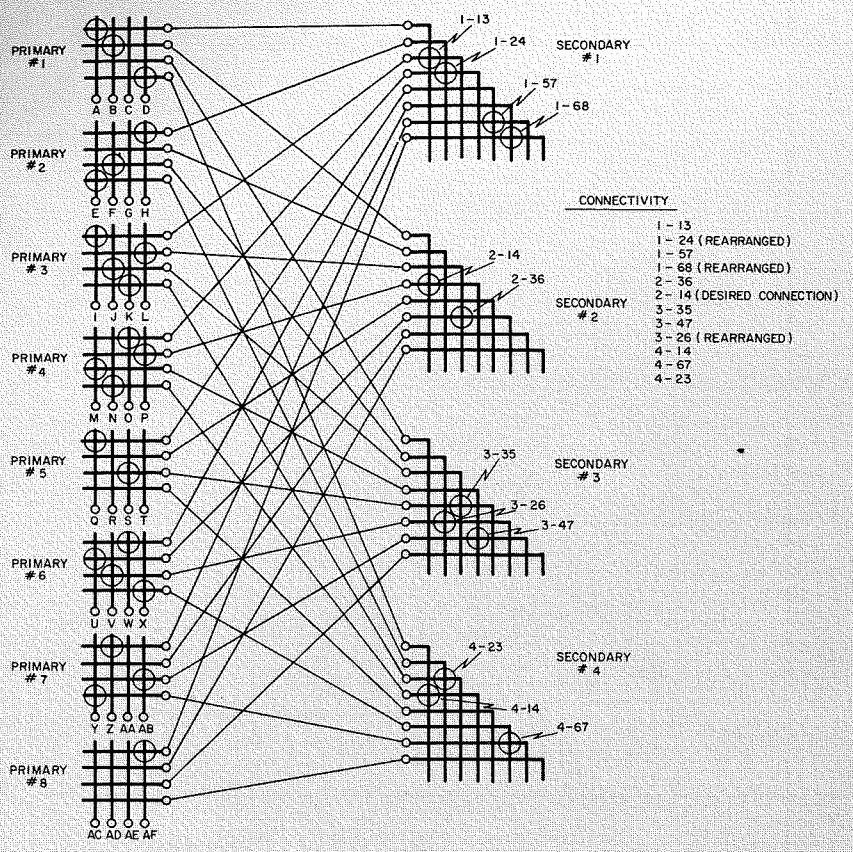


Fig. 4—Connectivity after rearrangement.

Table I—Sequence of rearrangement.

Original state	Step 2	Step 3	Step 3	Step 4	Step 5	Step 6	Step 6	Step 7	Step 5	Step 6	Step 6	Step 7
1-13						1-13	1-13					1-13
1-26						1-26	1-57					1-57
1-57						1-57	1-24					1-24
						1-24						1-68
2-24		2-24	2-36									2-36
2-36		2-36	2-14									2-14
		2-14										
3-35										3-35	3-35	3-35
3-47										3-47	3-47	3-47
3-68										3-68	3-26	3-26
										3-26		
4-14												4-14
4-67												4-67
4-23												4-23
want to make X-14	select secondary 2	make 2-14	break 2-24 4 is blocking primary	24 will not fit on any secondary	select secondary 1	Make 1-24	break 1-26 1 is blocking primary	26 will not fit on any secondary	select secondary 3	make 3-26	break 3-68	connection fits on secondary 1

REARRANGEMENT COMPLETE

blocked and note the blocking primary.
Step 4) Determine whether or not the connection broken in step 3 can be made to any other secondary. If it can, make it, and rearrangement is complete; otherwise, continue to step 5.
Step 5) Select another secondary with the minimum connections which does not contain the blocking primary of the broken connection (excluding the secondary where the connection was just broken).
Step 6) Reconnect the broken connection to the secondary determined in step 5, and disconnect the new blocked connection.
Step 7) Try all secondaries to see if the new blocked connection can now be directly connected. If it can, make it, and rearrangement is complete; if not, continue.
Step 8) Repeat step 5 with the exception that the currently blocked connection is not moved back to a secondary where a previously blocked connection came from unless that is the only secondary which does not contain the current blocking primary of the broken connection.

This algorithm will find a way to rearrange connectivity if rearrangement is possible. No case requires more than $(k-1)$ rearrangements (back to step 5).

Algorithm applied

Assume a switching system with eight primary switches, four secondary switches, and four inputs per primary switch with the current connectivity as follows 1-13, 1-26, 1-57, 2-24, 2-36, 3-35, 3-47, 3-68, 4-14, 4-67, 4-23 (Fig. 3). Subscriber B wishes to call Subscriber P, or a connection is desired from primary 1 to primary 4. As seen in Fig. 3, there is no secondary on which the connection may be made. Rearrange the connectivity to accommodate the desired connection.

Using the rearrangement algorithm, Step 1a (even number of links), the maximum possible connections = $(4 \times 8/2) + 0 = 16$. Only eleven connections are in use, so additional connections can be made. From step 1b, primary switch 1 has two connections out of a possible four; it is not blocked. Primary 4 has three connections out of a possible four; it is not blocked.

From step 1c, there is no common primary to either 1 or 4 on all secondaries. There is no common connection blockage. Rearrangement is possible by following steps 2 through 8 (See Table I). Fig. 4 shows the system after rearrangement.

Traffic analysis for command and control systems

R. W. Rostrom

A complete analysis of a command and control system will ordinarily require an analysis of the message traffic. Such an analysis may be required to specify the communication links, determine the communication equipment, size certain elements of a command and control processor, or contribute to other areas of a command and control study. Command and control messages can usually be clearly defined and are closely related to the operational scenario. This is not generally true for other types of traffic, and thus the approach to a command and control traffic analysis can be expected to differ somewhat from that for general traffic. This paper addresses itself specifically to command and control traffic analysis; however, many of the principles considered can be applied to more generalized analyses.

THE TRAFFIC ANALYSIS APPROACH considered here is one which allows for expansion and refinement of the analysis. Initial rough approximations are obtainable and these approximations can be refined as more and more data is accumulated. It anticipates the use of a computer to process the data, and while it is well suited to systems of even moderate complexity, it is not suitable for "quickie" analyses of simple systems.

Elements of traffic analysis

Fig. 1 shows the elements of a typical command and control traffic analysis. Major control centers (MCC) must exchange messages with a variety of originators and addressees over many communication systems. In a recently conducted traffic analysis, referred to throughout this paper as the *example analysis,* the following numbers of elements were involved:

5 major command centers (MCC)
130 message types
230 originators/addressees (O/A)
50 interfacing communication systems which interface directly with the MCC
50 relaying communication systems (RCS) which do not interface directly with the MCC

RCA Reprint RE-16-3-15
Final manuscript received February 3, 1970.

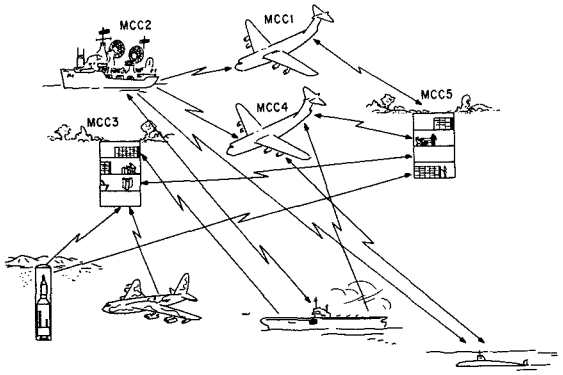


Fig. 1—Elements of a typical command and control traffic analysis.

The example analysis was conducted to specify the communication equipment required by each MCC and to determine the load presented by the message traffic to the MCC data processors. This required that peak traffic volume be determined for voice and data traffic on each of the MCC interfacing communication systems. The MCC data processor load was considered in three categories:

1) The total digital traffic, on which the data processor performed communication handling functions.
2) The formatted digital traffic, which entered the data processor directly for use in the command and control data base.
3) The voice and unformatted digital traffic whose information was to be manually entered into the data processor for use in the command and control data base.

Since the requirements of the example analysis were fixed by traffic on the interfacing communication systems, the relaying communication were not considered, except to list them for identification. Obviously if a requirement of the analysis had been to determine the loading of the relay communication systems then the analysis would have been conducted differently. This leads to the observation that each analysis must be uniquely tailored to accomplish its purpose. Two other significant characteristics of traffic analysis are 1) large amounts of data are involved, and 2) traffic analysis is best conducted as an iterative process.

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Data considerations

In its essentials a traffic analysis is simple. It involves a summary of messages from originators to addressees over a communication link. In practice a traffic analysis becomes complex because a large number of originators are sending many messages to many addressees over a variety of communication channels. The communication channels may be interconnected into a complex network. It has been noted that traffic analysis involves consideration of a number of elements such as major command centers, messages, originators/addressees, and communication systems. Each of the elements has a number of characteristics which may be significant in a traffic analysis. Typical characteristics of these elements are the following:

Message Type Characteristics
Name
Transmission mode (voice, teletype)
Security classification
Handling precedence
Origination rate (messages per hour)
Transmission rate (characters/second)
Message length
Single/multiple address indicator
Maximum tolerable delay
Grade of service

Originator/addressee characteristics
- Name
- Location
- Organizational relationship

Interfacing (and relaying) communication system characteristics
- Name
- Traffic modes carried (voice, teletype)
- Channel capacity
- Transmit, receive, two-way capability
- RF spectrum
- Modulation type

In addition to the characteristics listed above, the relationship between each of the elements must be identified. Thus, there must be matrices of:

- Major command centers (MCC) vs messages
- MCC vs originators/addressees (O/A)
- MCC vs interfacing communications systems
- Messages vs O/A
- Messages vs interfacing communications systems
- O/A vs interfacing communications systems

To specify the characteristics and relationships of the elements of the example analysis, 52,240 pieces of information were required. Additional information must be accumulated if any of the characteristics vary with time. It is almost always true that the rate of message origination varies with time, and it may be true that the message length varies with time. In the example analysis, both message rate and length varied significantly with time. Also, two complete scenarios had to be considered: one 48 hours long and the other 32 hours long. The rate and length profiles for these two scenarios required 10,340 additional information entries to specify length and rate on an hourly basis. Clearly, with 62,580 pieces of data, even this modest analysis is dealing with large amounts of information.

A standardized, systematic approach is required to accumulate such a large amount of data, and automatic processing is required to handle it. Because of the large amounts of data involved, the format for collecting the data should facilitate data accumulation and should permit compact data coding to minimize storage space. Formats given later meet these criteria. Data should be collected on computer coding sheets from the beginning of the analysis. This requires an initial effort for those conducting the analysis to become familiar with the data collection system, but this effort is repaid many times in standardization of procedures and avoiding the difficulties of later transcription to coding forms.

To handle such quantities of data a computer must be used. The use of a computer for traffic analysis is akin to its use in management information or business systems. Large amounts of data are subjected to sorting and simple computations. For the example analysis, two basic types of calculations were required, the channel loading calculations for voice and data traffic and the character loading calculations for the three categories of data processor load previously discussed. For each calculation, the appropriate messages and originators must be sorted from the files, and the contribution of all messages totaled. The final run of the example analysis required 17,600 calculations to be performed, calculations being made for all combinations of the following parameters:

1) Two of the five MCC,
2) The 48 hours of the first scenario and the 32 hours of the second scenario,
3) Transmit and receive traffic, and
4) The common user communications systems considered as a group, plus five satellite systems. For the satellite systems, two sets of calculations were required which considered the O/A directly subordinate to the MCC and those not directly subordinate.

The magnitude of sorting and calculation required clearly indicates the use of a computer.

The iterative process in traffic analysis

Fig. 2 shows the process involved in a traffic analysis. Five steps are shown, however, it is important to recognize that these steps are not performed sequentially in one pass, but that they are iterated until the traffic analysis reaches the state of perfection required. There are several reasons to plan a traffic analysis as an iterative process:

1) Data must be collected whose validity is often questionable. Good visibility and verification of the data may not be possible until the data is processed and printed out in appropriate format. Thus, the initial iteration would probably consist of rapidly accumulating as much data as possible, preparing programs to printout this data in visible format, and then reviewing the data for consistency and validity.

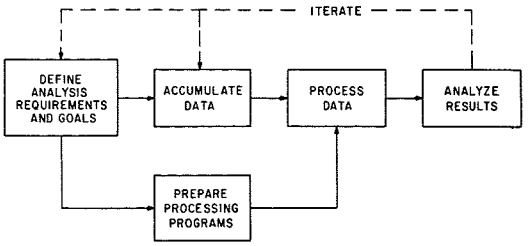


Fig. 2—Traffic analysis procedure.

2) The outputs of a traffic analysis are often required by other areas of a command and control study. To get initial outputs quickly, a good procedure is to make a number of simplifying assumptions, collect only a minimum of data, and make an initial set of calculations. For example, message length and rate might be considered to be constant with time and an estimate made of the average rates lengths. An initial calculation of channel loading could then be made using these averages.
3) Command and control system analysis, of which traffic analysis is a part, is itself an iterative process and the traffic analysis must iterate with it.
4) Since such large amounts of data must be collected, it is desirable to concentrate on the "significant" data early in the analysis. The most significant data can usually be identified only after a set of calculations are performed. Therefore, another iteration might be to process the data, calculating the channel loading from each message type and determining which message types, communication links, or other factors are most significant.

In addition to these planned types of iterations, circumstances often arise during the analysis which make additional iterations desirable. New and improved input data is often found during the analysis. Also the purposes of the analysis may be modified as aspects of a command and control system crystallize. In the example analysis, initial calculations were made of traffic on all 50 interfacing communication systems. It was found that on most of these systems, the traffic was immediately evident, and no calculations were required. Detailed calculations were required, however, of the traffic on a group of interfacing systems called common user systems, which carried a wide variety of traffic. The later iterations of the analysis concentrated on these systems. During the example analysis, approximately ten major iterations took place. This is considered typical and was made possible only by using automatic data processing.

Collecting the data

Since large amounts of data must generally be collected, at the outset of an

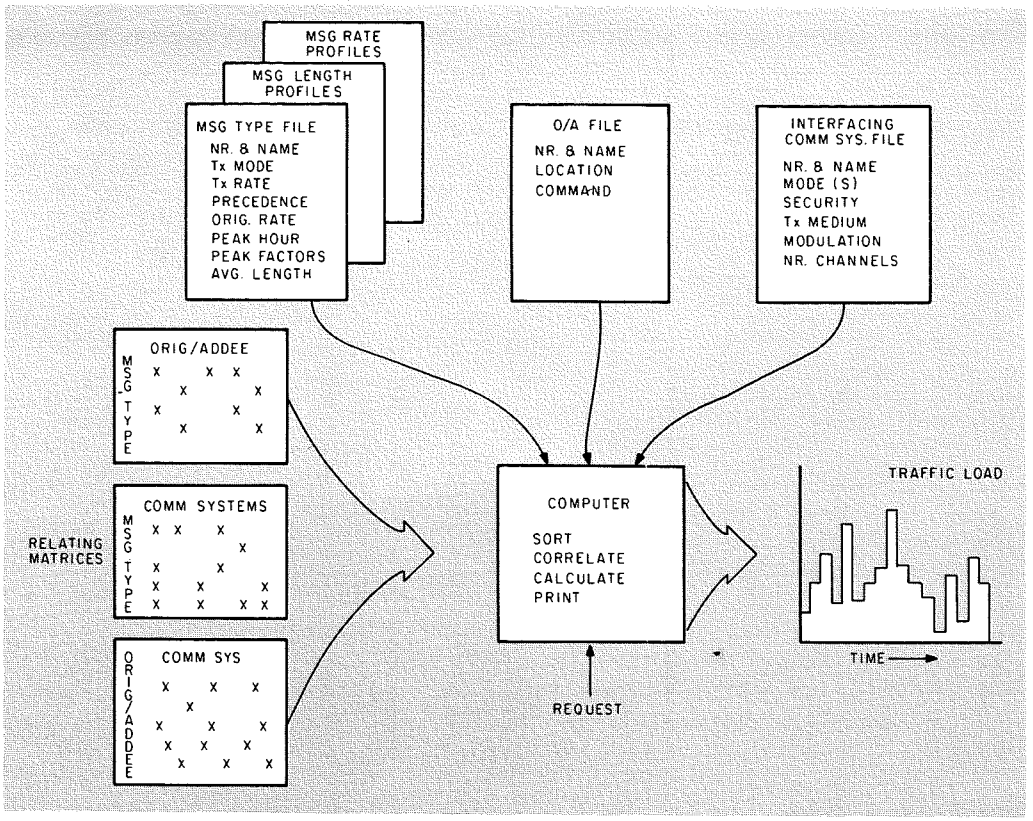


Fig. 3—Computer traffic analysis.

analysis, careful consideration should be given to what data is required and how it is to be collected and recorded. Just as "model shop" techniques are generally not suitable for mass production, so manual information handling techniques are generally not suitable for mass processing of information. Fig. 3 shows the data files used for a typical analysis and indicates generally how these files relate to solving the analysis problem. Segregating the data into the files as shown was found to be convenient for collecting and processing the data. This file organization also allowed the data to be highly compressed, minimizing storage requirements and the labor of collecting the data. To calculate traffic loading of a message, each of the files must be referenced. This would obviously be tedious to do manually, however a computer can easily extract the data from the appropriate files for performing a calculation. The files shown have been structured for mass processing by a computer.

Processing the data

The first phase of the example analysis was performed using time-shared computer terminals. While it was possible to conduct the analysis on these terminals, serious inconveniences associated with their use were found:

1) The large amounts of data involved required extensive linking of files. This complicated the programs and required continual reprogramming as the files expanded.

2) The low rate of input to the time-shared terminal necessitated leaving the data stored in the time-shared mass storage. This was costly.

3) The processing rate of the time-shared terminal was too slow. Sometimes it took a whole day to complete a portion of a run, and computer failures would often require re-runs.

4) The printing rate of the terminals was too low. The example analysis had 225 pages of computer printout in the final report. At the time-shared terminal rate of 100 wpm, this would have required 18 hours just to print.

For these reasons, a batch processing computer was considered better suited to a traffic analysis. Consequently the second phase of the analysis was conducted using the RCA Spectra 70 system in the Advanced Technology Computation Center in Camden, N.J. For the example analysis, a computer run on this system required about one hour of processing time and used about 150,000 bytes of core storage. The files were established on punched cards; these were convenient for making the numerous changes required during the analysis. Programming was done in FORTRAN IV, which was found to serve adequately. Probably more important than the specific programming language is that a qualified programmer be available to make changes to the program and expand it as required.

While a detailed discussion of the FORTRAN program used in the example analysis is beyond the scope of this paper, it is worthwhile to consider some aspects of programming a traffic analysis which might not be evident to the non-professional programmer:

1) Since the traffic analysis is an iterative process, the program will change throughout the analysis. Thus, it should be written with features which will facilitate change.

2) To avoid human errors, the program should include checks for consistency of the input data. For example, in developing message rate and message length profiles it is a common mistake to enter the length in hours different than those for which the rate was entered. The example analysis program included a check for such errors.

3) The computer should printout results in a form suitable for use in analysis and for the final report. The ingenuity of the programmer in providing good output formatting can make a significant contribution to the analysis.

Fig. 3 lists "printing" as one of the functions to be performed by the computer. This function deserves more consideration than perhaps is evident at first. As noted previously, the example analysis would require 18 hours of printout time on a time-shared terminal. The high-speed printer used in the second phase of the example analysis would print the same amount of data in about ten minutes. If consideration is given to typing such tables manually, 30 hours would be required to type the pages at 60 wpm. However, tables are notoriously tedious to type, and it is not unreasonable to expect that 60 hours might be required. Also manual typing of tabular data is likely to introduce errors which are difficult to uncover. The computerized approach accurately relieves typists of this time consuming and tedious task. It might be thought at first, that computer usage simply transfers the load from a typist to a key punch operator. However, because the input data is highly compressed, there is much less input key punching than output typing. In the example analysis, about 2000 cards were involved in the calculations producing 225 pages of output. This represents data compression of about 5 to 1. Thus the computer is a candidate for use even when computations are not extensive. The high-speed printout capabilities of the computer are, of course, not gotten "for free", but only after an appreciable investment in programming.

Data file descriptions

Figs. 4 and 5 give the formats of each of the data files. These formats can be used for a wide variety of traffic analysis; their use is not restricted to the example analysis, or even to command and control traffic analyses. One of the difficulties in accumulating data, is that communication system designers (for whom traffic analysis is performed) do not speak the same language as communication system users. The traffic analysis input data is generally obtained from system users, and it must be translated into terms usable by system designers. The formats include entries of both system user terminology and system designer terminology. Some of the entries may not be used explicitly in the calculations, but are useful for understanding of system requirements.

Data collection for automatic processing is quite different from that for manual processing. When calculations are to be performed manually, it is logical to do portions of the calculations as the data is collected. When a computer is to be used, it is logical to leave as many calculations as possible to the computer, and concentrate manual effort on accumulating raw data.

A detailed discussion of the formats is beyond the scope of this paper; however, the following discussion of some of the data fields shown in Fig. 4, will give a broad understanding of the rationale and use of these formats. Particular emphasis will be given to their use in the example analysis.

Message type file format

Field

1–3 *Message Number*—A three digit number was assigned to every message type and this number identified the message type throughout the analysis.

23 *Information Type*—The entries in this field refer to the functional information content of the traffic, i.e., whether the traffic is concerned with logistics, intelligence, command and control, etc.

24 *Communication Mode*—Indicates whether the information is transmitted as voice, teletype, data, or other mode.

27 *Multi-Address Symbol*—Indicates whether the traffic is single or multiple address; and if multiple address, whether it is broadcast, conference, multi-point, or store-and-forward multi-point.

28–32 *Contingency*—Refers to the politico-military situation(s) to which the traffic is peculiar. The example traffic analysis considered the contingencies of standby, alert, and war.

33–36 *Origination Rate*—Indicates the rate at which a message type is originated. It is expressed as messages per day per originator.

37–40 *Rate Profile Reference*—Designates the message rate profile applicable to the message. It may be used to designate one of a series of "standard" profiles. In the example analysis, it was simply used to indicate that a profile had been developed for the message. With this indication, the computer would take the rate from the profile rather than use the average origination rate.

41–44 *Peak Hour*—Designates the hour of peak traffic.

45–47 *Peak Factor*—Specifies the percentage of daily traffic occuring during the peak hour.

48–49 *Off-Peak Factor*—Specifies the percentage of daily traffic assumed to occur during an off-peak hour.

It will be recognized that the origination rate, peak hour, peak factor, and off-peak factor define a "square" traffic rate profile which can be used for preliminary calculations before more detailed profile information is accumulated. In the example analysis, a further simplifying assumption was made that the off-peak factor was 8% for all messages. In that analysis, calculations of channel requirements using the simplified "square" profile gave essentially the same results as the more complex calculations using the detailed profiles.

55–60 MCC *Indicator*—This field is used to indicate if the message is transmitted or received by a major command center. The five columns relate to the five MCC of the example analysis, and an "R", "T" or "D" is entered in the column to indicate that the MCC receives, transmits and receives the message.

61–65 *Sort Indicators*—These columns are used for sorting indicators of significance in a given traffic analysis. In the example analysis, each message was indicated as formated or non-formated. This was done so that messages automatically entered into a command and control processor could be distinguished from those not suitable for entry into the processor.

Originator/addressee file format

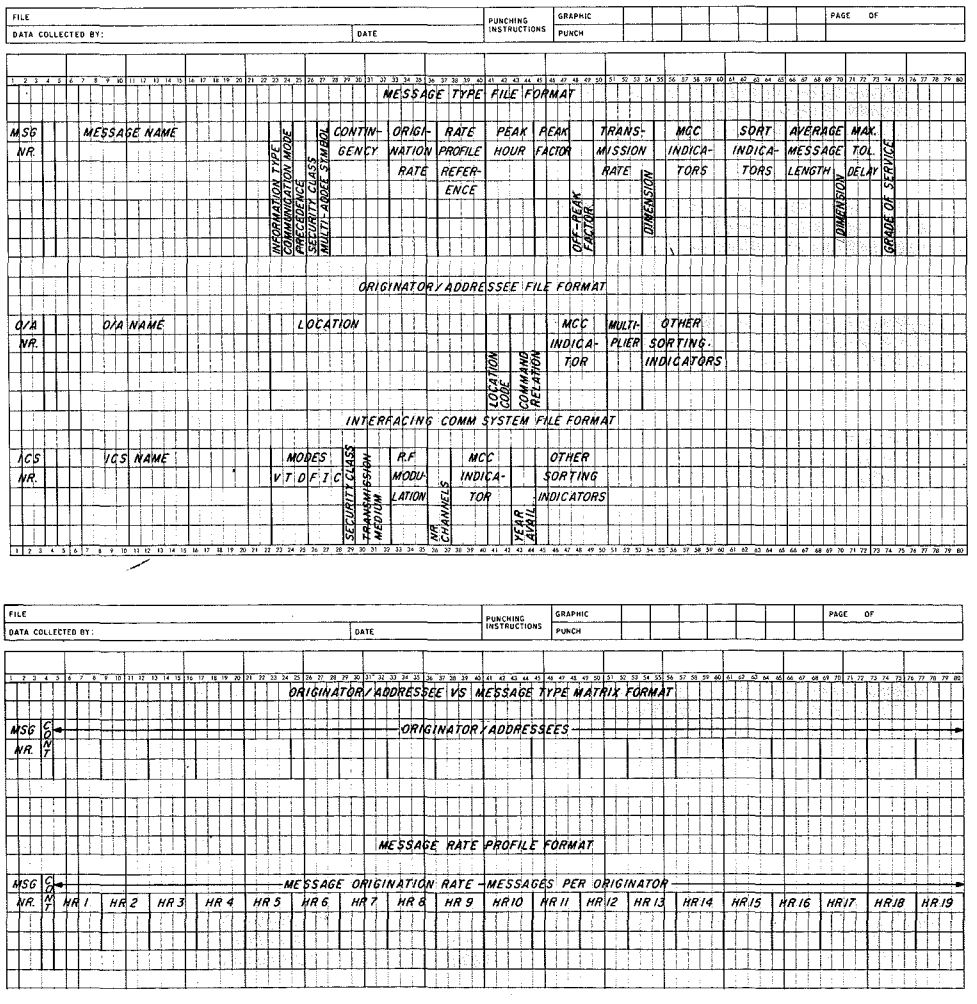
The purpose of most of the fields in this file will be evident from their titles in Fig. 4 and from the discussion of similar fields in the message type file. The following fields, however, deserve further consideration:

Field

41–42 *Location code*—this field is used to designate the location of the O/A in terms of regions significant for the analysis at hand. It might be used, for example, to indicate the Defense Communication Agency area. In the example analysis, it was used to indicate areas of communication satellite coverage.

43–45 *Command relation*—Used to indicate the immediate superior of the O/A in the command organization structure. The O/A number of the superior (columns 1-3) may be used to make the entry here. However, in the example analysis it was only required to show to which MCC the O/A was immediately subordinate. Thus a single column was used for entering the appropriate MCC indicator.

51–53 *Multiplier*—It will be found convenient to enter some groups of O/A as single entries in the O/A file. Examples of this might be bomber bases or Polaris submarines. In the message type file the origination rate was entered on a per originator basis and the traffic load calculation must multiply the origination rate by the number of originators. Thus either the origination rate entry must take into account the number of originators in the O/A group, or the number



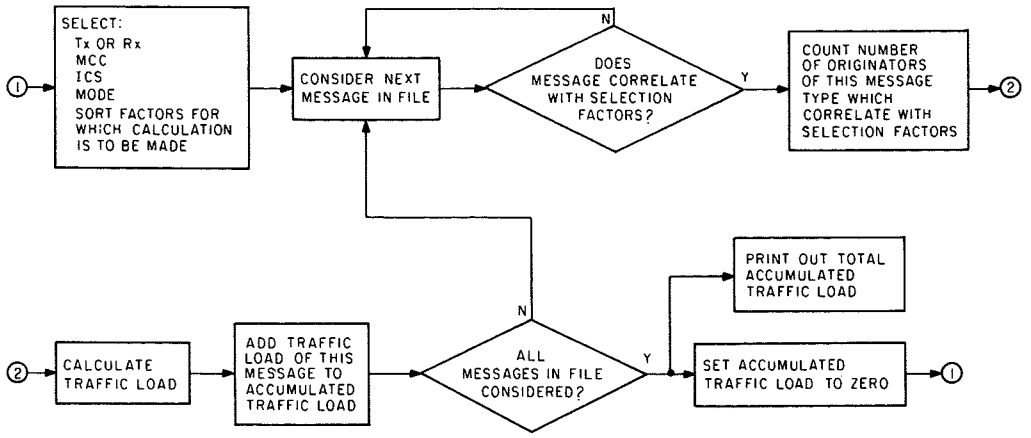


Fig. 6—Traffic analysis processing flow chart.

of originators must be explicitly stated. The multiplier field is used to explicitly state the number of originators in the O/A group.

Interfacing communications file format

Again the purpose of most fields in this file are evident from the titles shown in Fig. 4. However, the following fields deserve further examination:

Field

23-28 *Modes*—This field is used to indicate which modes of traffic are handled by the communication system. Entries are made in the appropriate columns with meaning as follows:

V = Voice	F = Facsimile
T = Teletype	I = Imagery (TV)
D = Data	C = Card

30/32 *Transmission medium*—Indicators are entered here of the transmission medium used by the communication system, such as coaxial cable, troposcatter, or radio. For radio systems, the entry might show the RF spectrum employed.

In the example analysis, it was originally intended to analyze the traffic loading on each interfacing communication system. As the analysis progressed, it was found that many messages could not be uniquely identified with one system, but rather could be handled by a number of interfacing systems. To account for this, some of the interfacing communications systems were grouped in what were called "ring-down groups". This terminology was used because the command and control communications system would automatically ring-down to put a message on a secondary communication system if the primary system were unavailable. The ring-down groups were entered on the interfacing communications system file in the same way as normal systems are entered. Traffic loading calculations were made for the ring-down groups in the same way as for the normal systems.

Relating matrices

Fig. 5 shows the format of the O/A vs message type matrix. This same format was used for all matrices. Columns 1-3 are used to enter the number of the message under consideration (see Columns 1-3 of message type file). The remaining columns are grouped in four column fields, which show which O/A handle the message. The O/A number is entered in the first three columns of the field while the fourth column contains an "R", "T", or "D" to show if the MCC receives, transmits, or both receives and transmits the message from (to) the O/A. Up to nineteen O/A can be recorded on one card for each message type. If more than nineteen O/A must be shown, multiple cards are used. The matrices of interfacing communication system vs message type and interfacing communication system vs O/A are formatted in the same way.

Attempts were made to format the matrices in an actual matrix form as they are shown conceptually in Fig. 3. This format proved difficult to use for data entry and was extremely difficult to read. It was also inefficient from a data storage standpoint since most of the matrix positions were blanks. Such a format appears to have application only if the matrix has entries in more than ¼ of its positions; it would then provide more efficient storage, although it would still be difficult to use.

Rate and length profiles

Fig. 5 also shows the format of the message rate profiles. Essentially the same format can be used for message length profiles. Columns 1-3 are used to enter the number of the message under consideration. The four column fields which follow are related to hours of the scenario and, in each field, entry is made of the number of messages per originator originated in the hour. One card can accommodate nineteen hours of the scenarios, and multiple cards are used if the scenario is longer than nineteen hours. Column 4 is used to indicate continuation cards for scenarios longer than 19 hours. For example, a "2" entered in column 4 would indicate that the following fields represent hours 20-38. If more than one scenario is to be considered, then profiles must be developed for each scenario.

Processing program description

As shown in Fig. 3, the computer performs the functions of sorting, correlating, calculating, and printing. Fig. 6 is a flow chart which shows the basic steps in calculating the traffic load applicable to any ICS. Note that separate calculations are to be performed for transmit and receive traffic for each MCC, for each ICS, and for each mode of traffic. Separate calculations may also be performed based on other sorting factors. The block labeled "Calculate Traffic Load" performs the type of calculations desired for the specific analysis. In the example analysis, two basic types of calculations were performed: character load calculations and channel load calculations.

Character load is found by multiplying together (orig. rate) (no. orig.) (message length). This calculation gives the number of characters occurring in the hour under consideration. Channel load is determined by the following:

$$\text{channel load} = \frac{(\text{orig. rate})\ (\text{no. orig.})\ (\text{message length})}{\text{transmission rate}}$$

which gives the number of minutes of channel time required during the hour under consideration (this unit of channel loading is commonly called an erlang). Obviously at least one channel is required for each 60 minutes of channel loading. A greater number of channels may be required if high precedence traffic is involved.

Summary

A traffic analysis of the type considered in this paper is an iterative process, often involving large amounts of data. It is best approached with a view to using a computer to do the repetitive sorting, correlating, and computing.

Acknowledgments

The author gratefully acknowledges the contributions of his colleagues in developing the traffic analysis approach presented in this paper. Particular recognition is given to H. Goodman who did the detailed programming for the example analysis, and S. Norris who gathered much of the input data for that analysis and thus aided in defining significant data parameters. T. B. Hodgson worked on the initial phase of the example analysis and made significant contributions to the analysis approach.

Tactical ground terminals for SHF satellite communications

R. S. Lawton

Synchronous earth-orbit satellites have emerged as a major form of electronic communications. Use of this communication media by the tactical military forces with their special requirements of mobility and flexibility is a natural application. RCA, under contract to the U.S. Army Satellite Communications Agency, has developed a family of lightweight, flexible SHF satellite ground terminals for tactical applications using the TACSAT I satellite. The five terminals of the family discussed in this paper encompass manpack, vehicular, and airborne configurations.

MILITARY USE of synchronous earth-orbit communication satellites has been under consideration since very early in this nation's space program. In recent years a number of experimental satellites have been launched to explore techniques for their use by the United States Military Services. In February, 1969, the experimental TACSAT I was successfully placed in synchronous orbit and subsequently maneuvered into an equatorial position near the Galapagos Islands off the Pacific coast of South America. The satellite contains repeater capability in two frequency ranges, UHF at 225 to 400 MHz and SHF at 7250 to 8400 MHz.

TACSAT I SHF system

Fig. 1 shows the satellite-earth relationship of the TACSAT I SHF system. The antenna pattern provides full earth coverage at the synchronous altitude of 22,500 miles. To facilitate simultaneous transmit and receive operations, separate frequency bands have been assigned for "downlink" (ground receive) and "uplink" (ground transmit). Downlink frequencies for TACSAT I lie in the range of 7252.5 to 7262.5 MHz; uplink frequencies are between 7977.5 and 7987.5 MHz. Transmit frequencies are always 725 MHz higher than the received frequency when using this satellite. Three satellite system bandwidths, selectable by ground command, allow improved noise performance when transmitting narrowband signals. The widest bandwidth designated "Band C" is 10 MHz. "Band B" provides 1 MHz and "Band A" 50-kHz bandwidth.

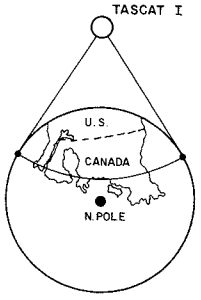


Fig. 1—Satellite/earth relationship for TACSAT I SHF system.

Reprint RE-16-3-17
Final manuscript received January 13, 1970.

The TACSAT I SHF ground terminals receive on one of four "RF channels" within the 10 MHz range as shown in Fig. 2. Channel 3 is centered at 7257.5 MHz while channel 1 is 4.1 MHz lower, channel 2 is 2.4 MHz lower, and channel 4 is 3 MHz higher. A fixed beacon signal used for frequency control of ground terminals is transmitted by the satellite at 7298.5 MHz. Actual carriers generated for any of these channels and the corresponding receive center frequencies are shown in Fig. 3.

Eight carriers are available for Band B channels while three are available for Band A. A signal designated "broadcast warning" is always located at a fixed frequency 7 kHz below center frequency for RF channel 3. Special carriers are generated 250 kHz above and below center for transmission of high-speed data, and both are used on opposite legs of the link for duplex operation. Because these carriers are generated by switching of oscillators in low-frequency sections of the equipment, they have been designated IF channels. The various members of the family generate only those carriers consistent with their functions.

The SHF terminal family

The smallest terminal is a manpack unit, AN/TRR-30, operating only as a receiver, and only at a fixed frequency. This unit (Fig. 4) at 63 pounds including all accessories and specially developed zinc-air battery, can be back-packed to remote locations.

The AN/TSC-79 shown in Fig. 5 is the smallest terminal providing full transmit and receive capability. It is zinc-air battery operated and, like the AN/TRR-30, is back-packable. A two-man team can transport it to almost any location accessible on foot.

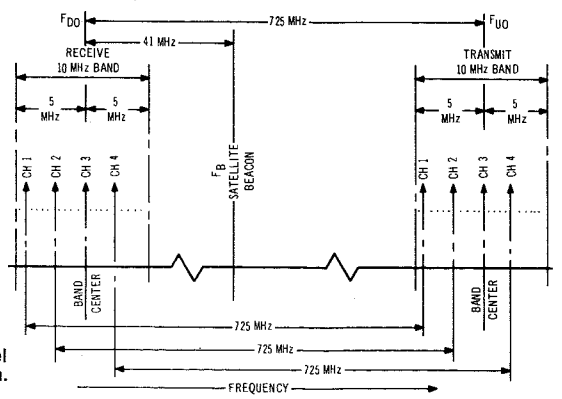


Fig. 2—Ground terminal RF channel frequency plan.

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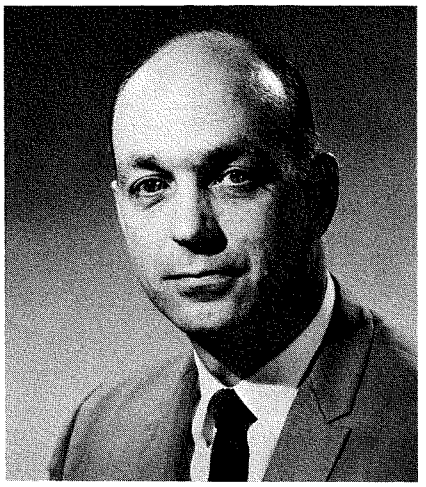


received the BSEE from Kansas State University in 1951 and the MSEE from Drexel Institute of Technology in 1956. He joined RCA in 1951 and was assigned to the Radiation Engineering activity working on military communications and navigation equipment design. He participated in design of the AN/AM-598 Amplifier/Power Supply and the AN/UPN-12 Loran and was responsible for the ground beacon for RCA's advanced Shoran system. He worked on the AN/FRC-39 and other troposcatter programs and in 1957, as an Engineering Leader, was responsible for the equipment package for the Army's ionospheric scatter system across the Pacific. From 1958 to 1960 he participated in the Air Force's 966L study program. Since 1960, Mr. Lawton has had major responsibilities for the AN/GKA-5 and AN/GKA-13 RF packages, communications studies for the AADS-70 (SAM-D) weapon system, the Lunar Orbiter Video Subcarrier Detector, Minuteman TAPS program, the AN/UCC-5 frequency division multiplex development and the Army's TACSATCOM program. He has also been responsible for ongoing production of AN/GRC-50 and AN/TRC-97 communication equipment. He is a member of the IEEE.

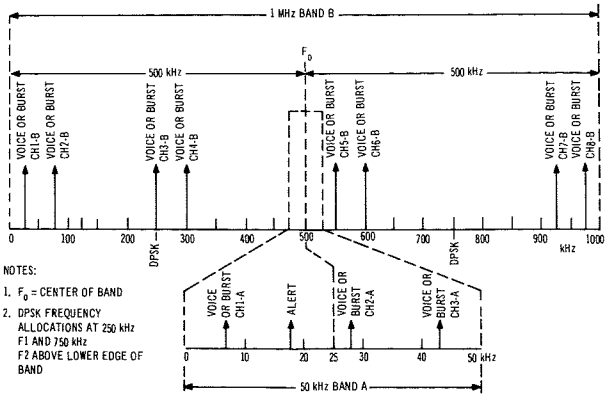


Fig. 3—Typical frequency allocation chart, showing band designations.

The most flexible of the five terminals is the AN/TSC-80 shelter terminal shown in Fig. 6. It is transportable by vehicle, helicopter, or fixed-wing aircraft and utilizes dual, 5-kW gasoline-engine-driven generators mounted in an accessory trailer as prime power.

The AN/MSC-57 is similar to the shelter unit but is mounted in a ¼-ton military vehicle. Lower transmitter power allows use of a 3-kW generator in the smaller trailer required for ¼-ton vehicle tow.

The AN/ASC-14 is for airborne installation. Aircraft motion dictates a tracking antenna, the OE-67(XA-1), and special circuitry to compensate doppler frequency shift effects.

Transmission modes

Four basic transmission modes are available within the equipment family as indicated in Fig. 7. The most conventional mode is analog frequency modulation providing a channel with nominal voice capability. This analog channel is also used for various low-rate data functions. An external four-wire interface to this mode allows

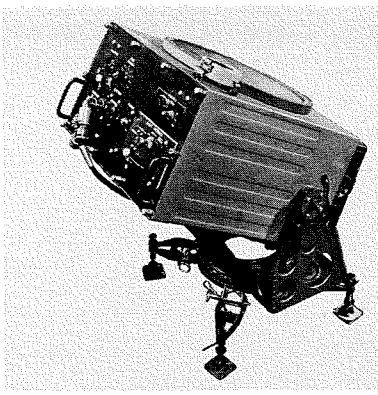


Fig. 4—AN/TRR-30 manpack equipment.

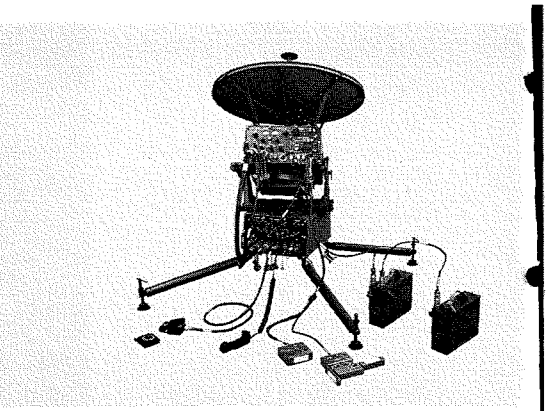


Fig. 5—AN/TSC-79 teampack terminal.

access by conventional communication line.

A second mode, called broadcast warning message, provides for transmission of a highly redundant, low-data-rate signal from a shelter terminal to all other ground terminals. These warning messages are displayed as one of 15 two-digit decimal combinations at the receive end. One of the terminal types, the AN/TRR-30, is devoted exclusively to receipt of these messages.

All terminals, except the receive-only manpack, accommodate the TATS modem—a band-spread frequency-hopping, modem system developed for the TACSAT I and providing multiple access and some immunity to interference. Both a 75 bit-per-second rate for teletype operation and a 2400 bit/second rate for data and vocoder processed voice are provided.

The fourth transmission mode provides for high-data-rate inputs and (DPSK) modem. The interface currently provided accommodates the 288-kilobit/second signal of the TD-660 time-division-multiplex equipment.

Frequency generation

A high degree of frequency stability for all elements of the system is obtained by using the satellite beacon signal as common reference for generation of all critical signals in the ground terminals. With the exception of the manpack which operates on the broadcast warning signal only, all members of the family have master frequency sources phase-locked to the beacon. Both transmit and receive frequencies are derived from the master frequency source. Placing the frequency control burden on the satellite in this manner allows considerable simplification of ground frequency sources and the phase-locking of master frequency sources minimizes long-term drift.

Short-term drift, or phase and frequency jitter, then becomes the key criteria in design of the frequency generation systems. Fig. 8 is a functional depiction of the frequency control concept. The limits shown are dictated by allowable jitter in the effective 100-Hz bandwidth of specialized modems used in the terminals for teletype operation. They represent approximately 5 Hz of RMS jitter for back-to-back operation.

Fig. 6—AN/TSC-80 shelter terminal.

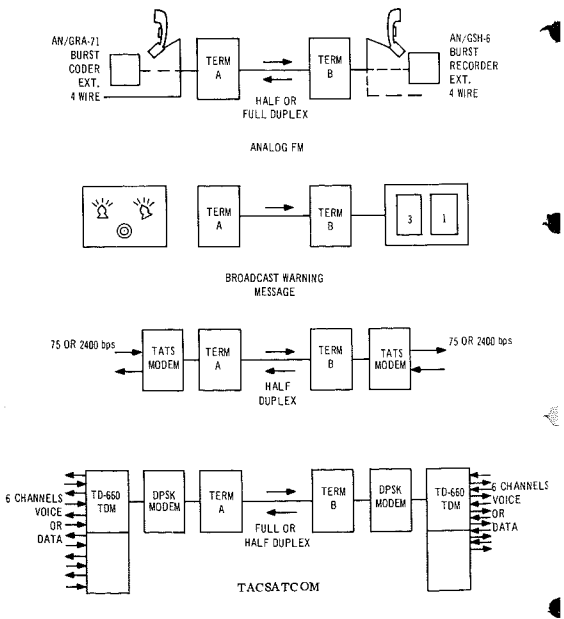


Fig. 7—Modem for TACSAT.

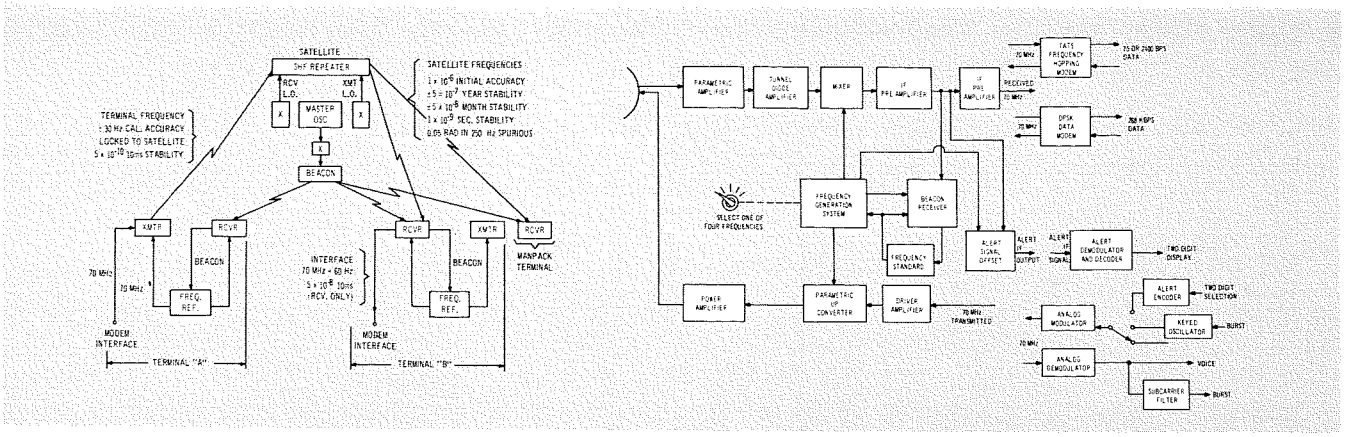


Fig. 8—System frequency control.

Fig. 9—TACSAT SHF ground terminal.

Fig. 9 shows the functional blocks of the terminal family. Parabolic antennas are used for all terminals: a four-foot dish for the shelter, a three-foot for vehicle and teampack, a 33-inch for airborne, and a 12-inch for manpack. Transmit-receive diplexing is integrally designed into the feed system by means of the circular polarization sense; right-hand sense for uplink, left-hand sense for downlink.

The high-performance terminals—shelter, vehicle, and airborne—utilize an uncooled paramp followed by a tunnel diode amplifier (TDA) giving about 32 dB total gain. Teampack and manpack use only the TDA. Loss in gain for this configuration is offset by added IF gain. The paramp yields noise temperature in the range of 160 to 190° K while the TDA gives about 815° K. First IF frequency for both transmit and receive is 70 MHz, but lower conversions are made in the various modems.

Transmitter power amplifier outputs range from 10 Watts for the teampack to over 1 kW for the airborne terminal. Shelter terminals provide 500 watts output while the vehicle terminal output is 100 W. All are adjustable down to 3 W or less to allow effective power sharing through the satellite.

The frequency generation system uses the direct synthesis method to generate coherent local injection frequencies from the locked master source in order to assure the low system jitter required for TATS teletype transmission.

Both the beacon and broadcast warning signals have fixed frequency positions. To avoid the need for separate receivers for these signals, the receiver front end is designed with sufficient bandwidth through the IF preamp to accommodate both these signals and the communication carriers shown in Figs. 2 and 3. This results in first IF translation of beacon and broadcast warning signals that change with RF channel settings; 65 to 75 MHz for the broadcast warning and 106 to 116 MHz for the beacon. To return these to fixed frequencies for processing, RF-channel-related offset signals are generated for use in beacon receiver and alert offset modules. Both the TATS frequency-hopping modem and the DPSK modem interface at 70 MHz.

The broadcast warning transmission consists of a 40-second preamble of alternate "ones" and "zeros" and ten repetitions of a binary serial 12-bit message. The first four message bits, all "ones," provide synchronization. The position of a "one" in the next five slots provides five "addresses" while the position of a "one" in the last three slots designates three "texts." Only sequences containing a single "one" in the "address" slots and a single "one" in the "text" slots are valid. Three consecutive validations are required for readout on the decimal dials. This sequence is applied to the analog FM modulator at a 40 bit-per-second rate with 50 Hz total shift. By transmitting the sequence f_1, f_2 for a binary "1" and the sequence f_2, f_1 for a "0", a symmetrical spectrum about the carrier is generated for any message sequence allowing AC coupling of signals.

Analog signals of voice channel bandwidth are transmitted as FM and demodulated using a phase-lock discriminator to achieve extended threshold performance. Two demodulation bandwidths are provided: one optimizes for a peak deviation of 4.8 kHz; the other optimizes for a peak deviation of 6.8 kHz with a resultant added FM improvement factor.

An 850-Hz oscillator allows transmission of on-off data with 1100-Hz peak deviation of the analog channel. An additional translation to 2 kHz is provided at the receive end for more convenient processing of this type data.

Differences in terminal types

Shelter terminal

The AN/TSC-80 Shelter Terminal incorporates all of the transmit and receive functions outlined in Fig. 9 and generates frequencies necessary for operation on all the carriers designated in Figs. 2 and 3. The broadcast warning signal is transmitted only by this terminal. The antenna system, including the SHF receiving amplifier containing both parametric and tunnel diode sections, mounts on the corner of the shelter using quick-release-pin hardware. The SHF amplifier, mounted in a box just to the rear of the antenna reflector, joins the antenna feed through a short section of bendable waveguide and pivots with it in the mounting cradle. Transmitter output signal is applied to the antenna feed through a section of twistable waveguide to allow elevation and azimuth adjustment. A crank-driven worm drive provides azimuth adjustment while a chain-drive mechanism provides elevation adjustment. Hand transits are used for initial setup and a remote beacon-strength indicating meter allows precise manual adjustment by the operator using these controls. Consistent setting accuracies of under ±0.5° have been experienced.

Acquiring the satellite has proven to be easy and straightforward on all terminals. Setup times with a two-man crew have run under 20 minutes, and it has not been necessary to stabilize the vehicle with jacks or blocks even with three or four people moving about on the vehicle tailgate and in the shelter.

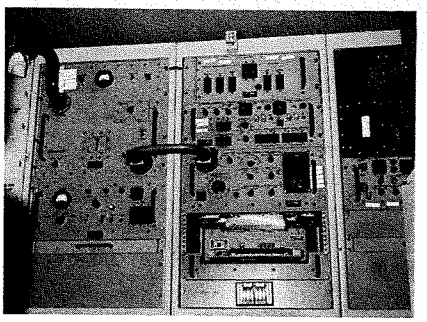


Fig. 10—Interior of shelter terminal.

Fig. 10 is an interior view of the shelter with major assemblies clearly visible. The power amplifier and its high-voltage supply are located in the left-hand rack. The power amplifier uses a five-cavity klystron delivering 450 to 500 W maximum power at the antenna flange. Output power is adjustable by front panel control down to 1.5 W.

The PA high-voltage power supply for the AN/TSC-80 converts nearly 2 kW of power from 115 volts, single-phase, 60 Hz to 5,000 VDC in a unit contained in a volume of less than two cubic feet and a weight of 52 pounds. Solid-state switching converter techniques with a switching frequency of 2500 Hz have been used to provide this significant size and weight reduction. At the same time, a substantial amount of voltage regulation has been achieved. Fig. 11 shows a fundamental block diagram of the supply.

The bottom unit in the left-hand rack is the DPSK modem. The center rack contains a power distribution panel; a patch and monitoring panel; the modulator/exciter; and a teletypewriter. In the right-hand rack are the vocoder, the TATS modem, and the receiver unit.

Vehicular terminal

The AN/MSC-57 vehicular terminal shares a large number of common units with the AN/TSC-80. However, the AN/MSC-57 uses a three-foot antenna reflector and a traveling-wave-tube power amplifier delivering 80 to 100 W at the antenna flange. As in the AN/TSC-80, solid-state switching converters are used allowing the entire 100-Watt amplifier and high-voltage power supply to be packaged in only 8¾ inches of rack space. The power amplifier can be operated from 115-V, AC power or directly from a high-capacity vehicular battery system at 22 to 30 VDC.

The frequency generation system for the AN/MSC-57 provides all four RF channels, all three Band A carriers, and broadcast warning receive, but allows for only channels 1, 3, 5, and 7 of Band B. It is equipped with the TATS modem and analog voice capability, but not the DPSK modem.

Teampack terminal

The AN/TSC-79 teampack terminal provides both transmit and receive capability in a small package weighing 139 pounds which can be dismantled into back-pack units for transport. The 17-pound zinc-air batteries, mounted on the receiver unit (the upper unit in Fig. 5) provide 24 hours operation on a 1 to 23 transmit-receive cycle. They are recharged by insertion of a new set of bicell plates and activation with almost any fluid.

The teampack transmitter, the lower unit in Fig. 5, uses a traveling wave tube providing a power output of 10 W. This output can be reduced to approximately 3 W by means of a front panel switch. The three-foot antenna reflector is made up in four separable segments for transport.

This terminal and the receive-only broadcast warning receiver employ a tunnel diode amplifier rather than the larger and heavier combination parametric/tunnel diode package used on the larger terminals. Although an external 70-MHz interface is provided, normal operation of this terminal is analog FM voice or burst and broadcast warning receive. Two IF channels are available in Band B (1 and 7), and two are available in Band A (1 and 3, plus broadcast warning receive).

Manpack terminal

The AN/TRR-30 broadcast warning receiver is the most portable of the SHF TACSAT ground terminal family. It can be back-packed by one man to provide the broadcast warning message receive function in remote locations. Its zinc-air battery provides power for 60 hours of continuous duty on one set of bicell plates.

In addition to the reduction in antenna size to 1 foot, the broadcast warning receiver differs from that in the teampack in several other respects:

1) Local frequencies are not locked to the satellite beacon. The beacon signal is, however, used for antenna pointing.

2) A radiometric technique provides a beacon received level indication to orient the unit for maximum signal from the satellite.

3) The local oscillator injection frequency for this terminal is derived by direct multiplication from a crystal frequency standard.

4) A front panel switch provides four frequency increments each side of nominal to compensate for both satellite and local drifts.

Airborne terminal

The airborne AN/ASC-14 terminal must cope with several factors not present on the fixed terminals: The antenna must track the satellite position at all times, and its maximum dimensions are restricted by the allowable projection of the radome from the aircraft fuselage. For EC-135 type aircraft a 33-inch antenna reflector provides a reasonable compromise in dimensions. Satellite signal acquisition and tracking involves both manual and automatic sequences operating with the beacon signal from the satellite. Acquisition is initiated manually by setting initializing controls to point the antenna in the approximate direction of the satellite. Then, an auto-

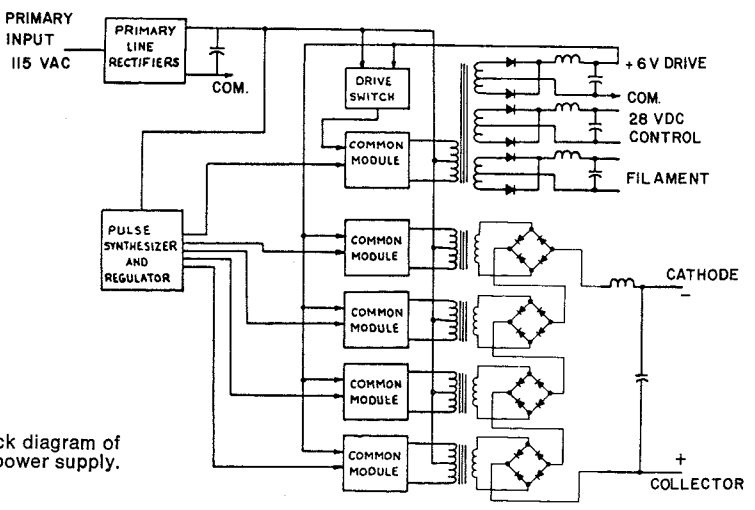


Fig. 11—Fundamental block diagram of solid state switching power supply.

Table 1—Summary of characteristics of SHF TACSAT ground terminals

Terminal	Maximum power (Watts)	System noise temperature (° K)	Antenna Size (in)	Antenna Rcvr. gain (dB)	Antenna Trans. gain (dB)	TATS modem	DPSK modem	FM analog modem	Broadcast warning trans.	Broadcast warning rcv.	Beacon rcvr.
AN/TSC-80 Shelter	470-500	230-315	48	36.5	37.5	X	X	X	X	X	X
AN/MSC-57 Vehicle	85-105	-325	36	33.5	34.5	X	—	X	—	X	X
AN/TSC-79 Teampack	10-10.6	-920	36	33.5	34.5	*	—	X	—	X	X
AN/TRC-30 Broadcast warning receiver	—	896-915	12	23.8	—	—	—	—	—	X	**X
AN/ASC-14 Airborne	***1300-1400	-325	33	33.1	34.1	X	—	X	—	—	X

*Interface provided but not part of present terminal
**Beacon used only for antenna pointing and initial frequency set
***At power amplifier flange

matic raster scan over a 20 by 20 degree segment of space is started. A gyro stabilization system maintains space orientation during this scan, and the search scan continues until beacon signal strength indicates that the satellite is within the antenna beam. The search is then terminated and the receiver allowed to lock to the beacon frequency. Rather than depend upon the gyro for subsequent space pointing, which would require very low drift in the system, a continuous horizontal "bow-tie" tracking scan is provided which generates a small modulation on the received signal to control the pointing servo.

Doppler frequency shifts occur with the airborne terminal and must be compensated for most of the communication modes. The frequency of the master oscillator locked to the beacon will be offset from the true beacon frequency by the amount of the doppler shift. For the transmitted frequency to be received at the satellite on the proper frequency, it must be originated with a frequency shift to just offset doppler. It is therefore transmitted at two times the doppler shift from the receiver frequency.

The method of obtaining this offset in the correct sense is shown in Fig. 12. Since a positive doppler shift pulls the receive master frequency source toward a higher frequency, doubling of the doppler shift and inversion are required for proper correction. This is accomplished by deriving the transmit frequency source from a mix of the second harmonic of the receive master frequency source which is phase-locked to the received beacon signal, and the third harmonic of the doppler reference oscillator which is set at the no-doppler frequency of the receive master source. The difference mix yields the required corrected frequency. The frequency of the doppler oscillator is set by manual adjustment for zero frequency difference between the two oscillators with the aircraft at rest. Doppler reference oscillator stability is sufficiently high to allow an 8-hour mission without readjustment.

Terminal characteristics and performance

Key characteristics of the terminals are listed in Table I. Fig. 13 illustrates a relative measure of the terminal performance. For simplicity this chart is based on single access to the satellite. Since power must be shared among all satellite users, the margins would be reduced; when more than one user is operating through the satallite, however, normal path losses are 6- to 7-dB lower than the worst-case used for the chart.

An example of performance is a 1¼-ton shelter terminal communicating in the FM analog mode with a teampack with the satellite in 50-kHz bandwidth. The shelter to teampack link gives a C/N_o of 57 dB which yields 31 dB S/N for 6.8-kHz deviation. This is limited by the downlink characteristics of satellite power, receiver antenna size, and receiver noise temperature. On the teampack to shelter link, C/N_o is only 53 dB and is uplink limited. The 10-W output and 3-foot antenna do not give sufficient level at the satellite to saturate it. Even though the shelter antenna is larger and noise temperature lower, a poorer C/N_o results.

Another significant example would be the use of DPSK modems between shelter terminals in the 1-MHz Band B satellite mode. Then C/N_o would be 65 dB, which is 1 dB short of that required for 1 in 10^5 bit error rate. Only single access would be practical in this mode.

Conclusion

Units of each terminal type are being employed by a tri-service task force to explore techniques for tactical use of satellite communication by military services and to develop more advanced technical and system concepts. This equipment family development has been a significant contribution to the emerging satellite communication art and provides a sound basis for further progress.

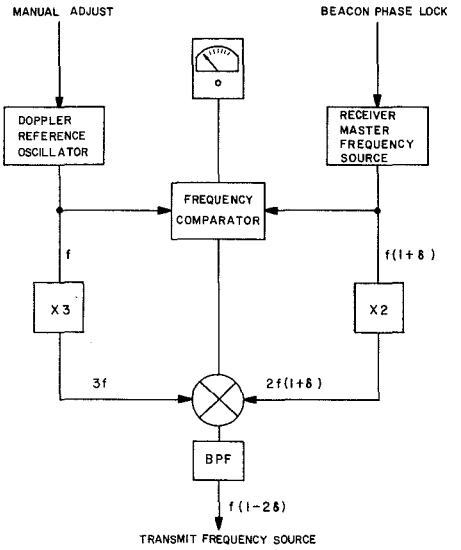


Fig. 12—Doppler correction system.

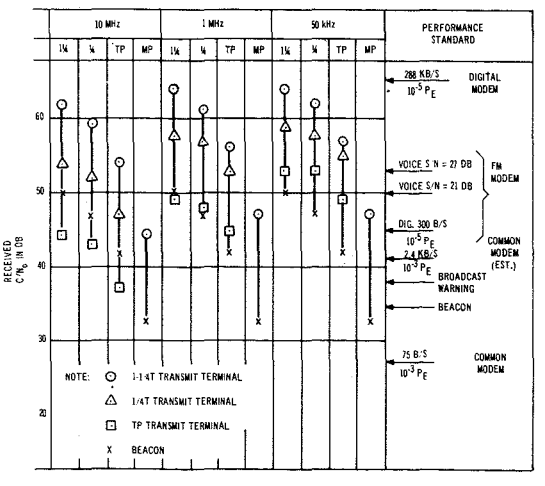


Fig. 13—Single access system performance.

A high-speed digital modem for tactical satellite ground terminals

W. Mergner

Transmission of PCM multiplexed voice and other high-speed digital signals through tactical satellite communication systems requires a highly efficient, flexible, and rugged modem which can be operated and maintained by military personnel. RCA has developed, under contract to the U.S. Army Satellite Communications Agency as part of the TACSATCOM SHF Ground Terminal Program, a differential phase-shift-keyed modem which allows transmission of six-channel PCM multiplexed signals through the TACSAT I satellite communication system with low error rate.

As the operational techniques for tactical military use of satellite communication have become more refined, the need for high-speed, low-error transmission of digital signals has increased. The differential phase-shift-keying modem (DPSK) developed by RCA for U.S. Army Satellite Communications Agency as part of the TacSatCom Ground Terminal Program meets this requirement. It is designed specifically to interface with the Army's TD 660 multiplex equipment, a six-voice channel PCM equipment operating at 288 kilobit/s. However, the circuitry and concepts are readily adapted to other bit rates.

Modern design considerations

Since system operation imposes low carrier-to-noise ratios in the modem's field application, engineering design approaches have been taken which ensure maximum performance. First, all transmitted energy is allocated to the data channel (an inherent feature of DPSK); second, a frequency reference scheme is used which provides minimal degradation of the received signal-to-noise (S/N) ratio, accomplished by generating the receiver reference through non-linear operations on the received phase modulated signal; and finally, post-detection matched filtering is utilized to maximize the output signal-to-noise ratio, implemented with dual RC integrate, sample, and dump circuits.

Fig. 1 shows the controls of the equipment, which have been minimized for ease of operation. A built-in test meter monitors critical parameters to allow rapid analysis of the unit's performance. The small (19 by 7 by 17-inch), lightweight (27 lbs.), rugged package is equipped for slide mounting in standard-width (19-inch) rack systems.

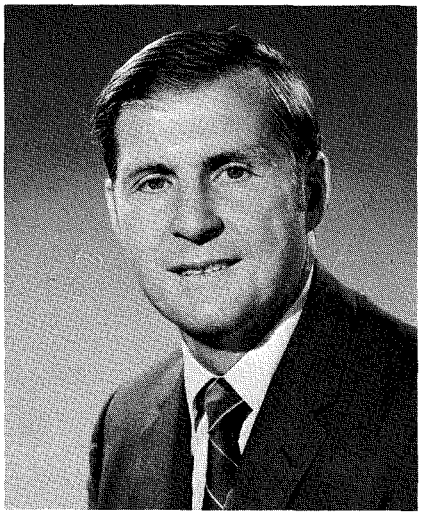
The application of the differential phase-shift-keying (DPSK) modulation technique in the modem permits all transmitted energy to by allocated to the data signal, none being required to convey carrier phase information or bit sync information to the receiver. This property (DPSK) is a key factor in the unit's efficient performance.

A simplified block diagram of the DPSK modem is shown in Fig. 2. The dashed line separates the unit into two functional areas: *transmit* and *receive*. On the transmit side (phase modulator), data flow is through the differential encoder into the modulator. The differential encoder output signal phase modulates a stable 12-MHz signal and the resultant output is up-converted to 70 MHz. On the receive side (phase demodulator), 70-MHz received signals are down-converted to 12 MHz and applied to both the 12-MHz reference generator and phase detector. The detected signal is then applied to the bit timing extractor and the sampled integrator signal processing circuits. The processed output of the sampled integrator is then decoded in the decoder unit, using timing signals from the timing extractor. Demodulator output is a fully conditioned and timed signal.

Modulation

Differential encoder

Data and timing signals from the pulse-code modulation (PCM) equipment



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received the BSEE from the University of South Carolina in 1958 and the MSEE from Drexel in 1965. Mr. Mergner first joined RCA in 1957 as a summer trainee with a design group working on the Air Force Time Division Data Link Program. Upon receiving the BSEE, he returned to that same group in 1958. He subsequently worked on projects such as the Army Preflight Test Set, Navy Data Link, Ranger, ARC-104, TAPS, Manpack Microwave Radio, and TACSAT. His current assignment is to design various sections of the Bench Test Equipment (BTE) for use with the ERTS tape recorder. Mr. Merger is a member of Tau Beta Pi.

Reprint RE-16-3-16
Final manuscript received 15 July 1970.

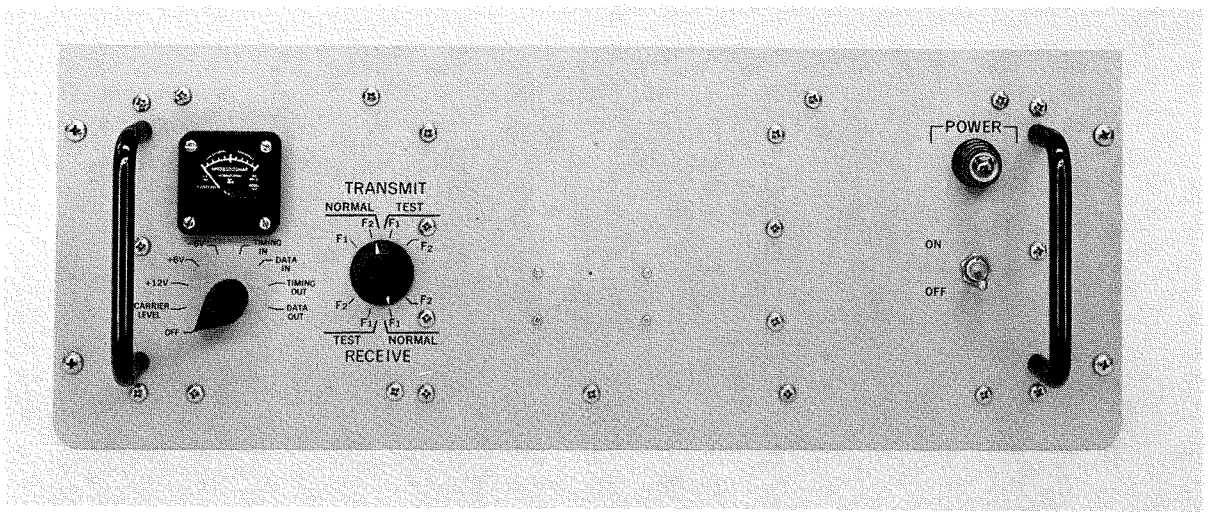


Fig. 1—High-speed digital modem.

are fed to the differential encoder. The encoder output changes state when the incoming data bit is a space. The data stream is fed to one input of an AND gate and timing pulses, delayed by approximately 0.4 of a bit period, are fed to the other input. The delay provides more reliable gating action since the 0.1-μs pulse then appears in the middle of the bit time slot. The output of this gate is a pulse each time the input data stream is a space.

The output pulses trigger a flip-flop which produces the differentially encoded waveform as shown in Fig. 3. The encoded signal is passed through a driver amplifier to the phase modulator.

Phase modulator

The phase modulator shifts the phase of the carrier 180° each time the differential encoder flip-flop changes state. It consists of a 12-MHz crystal-controlled oscillator and a double-balanced diode quad modulator. The 12-MHz oscillator ouput is fed to the modulator's input transformer. The encoded data is fed to the center-tap of the input transformer's secondary winding. A similar output transformer has a balancing bias applied to its center tap so that as the encoder flip-flop's output level changes, a different pair of diodes is caused to conduct. This changes the direction of current flow through the output transformer, and reverses the instantaneous phase of the carrier by 180°. This 12-MHz phase-modulated signal is up-converted to the 70-MHz range. The up-converter injection signal is in the 58-MHz range.

Demodulation

The signal flow following the 70-MHz interface with the receiver is depicted in Fig. 2. The 70-MHz phase-modulated signal is down-converted to 12 MHz. The AGC on the 12-MHz amplifiers maintains a constant level into the 12-MHz reference generator and into the data phase detector.

12-MHz reference generator

The reference generator extracts a 12-MHz phase reference signal from the received signal to allow synchronous detection of the modulation information by the data phase detector. The first stage of the reference generator is a frequency doubler. The doubler effectively removes phase information from the received signal. This 24-MHz carrier is then used as the reference

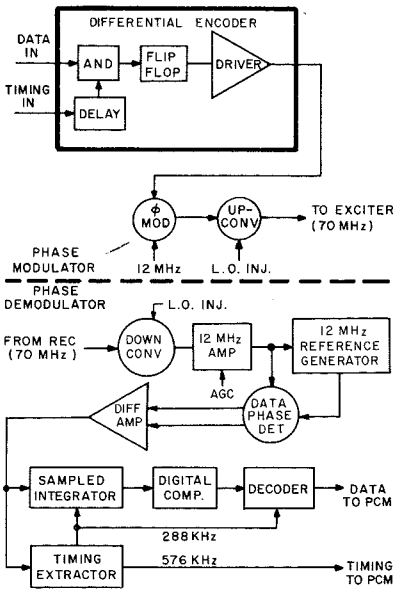


Fig. 2—DPSK modem simplified block diagram.

input in a phase-locked loop which has as its other input 24 MHz produced by doubling the frequency out of a 12-MHz voltage-controlled crystal oscillator (VCXO). The phase detector used in this loop develops a zero-volt error signal when the phases of the reference signal and the controlled oscillator's output signal differ by ±90°. By placing a 90° phase-shift-network in the reference generator loop, the VCXO is forced to lock up either in phase or 180° out of phase with the incoming phase-modulated 12-MHz signal. Either phase is acceptable due to the differential encoding used at the transmitter.

Sampled integrators

The two sampled integrators act as a narrow-band post-detection filter, improving the signal detection capabilities of the receiver. A given signal phase is associated with one integrator and the opposite phase is associated with the other. During each bit period, signals proportional to the two opposite phase conditions are fed separately to the two integrators. The desired signal has an average value which is integrated by one or the other integrator. The undesired noise present along with the signal has no average DC component so that the integral of the noise over one bit period tends to be zero. At the end of a bit period, a comparison is made as to which integrator has the higher voltage. As noise increases, the probability of a wrong decision being made increases. If an erroneous decision is made, a bit error results. At the same instant that the sampling takes place, the integrator capacitors are discharged, thereby

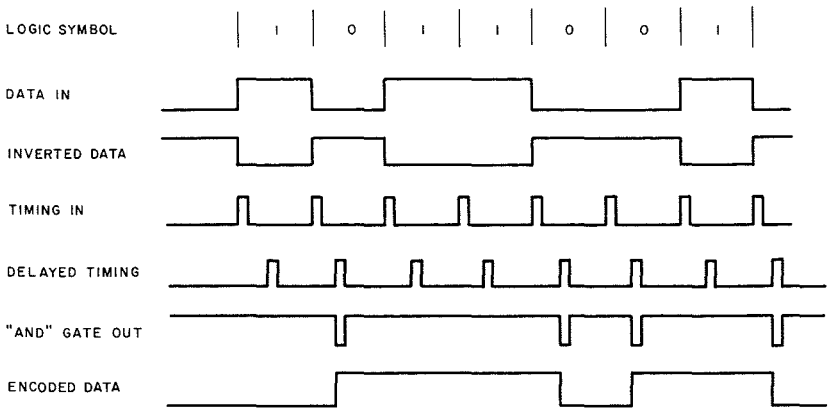


Fig. 3—Differential encoder timing diagram.

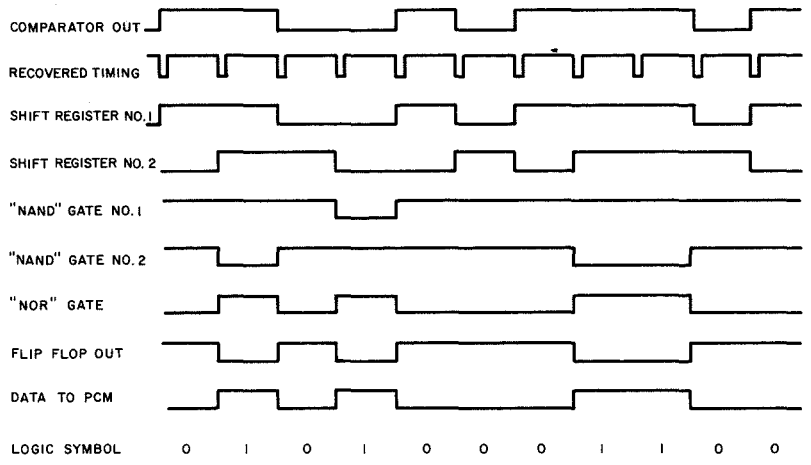


Fig. 4—Differential decoder timing diagram.

eliminating any integrator memory from one bit-period to the next.

Decoder

The digital comparator following the sampled integrators senses which integrator has the greater voltage build-up. A voltage difference of approximately 1 mV can cause the two-state output of the comparator to switch from one voltage level to the other.

The comparator output and its inverted output provide complementary steering signals for a two-bit shift register in the decoder. Shift pulses at 288 kHz advance the shift register in accordance with the steering levels. Thus, the condition of the first shift register stage reflects the phase of the present bit received while the condition of the second stage reflects the phase of the previous bit received. If there has been a change in phase between successive received bits, there is a difference in the two logic levels stored in the register. This corresponds to having received a space. Conversely, if the two logic states in the shift register are the same, a mark was received. The shift register drives two NAND gates; one having a low-level output if both stages of the shift register contain logic zeros and the other having a low-level output if both stages contain logic ones. When either of these logic AND conditions are satisfied, the output of a NOR gate is high, and a logic one is clocked into the final decoder flip-flop. Fig. 4 shows the timing involved in the decoding operation. A driver amplifier in the decoder conditions the signal to the proper levels for interfacing with the PCM equipment.

Timing extractor

The timing extractor generates clock pulses at both 288 kHz and 576 kHz with the proper phase relation to the incoming received signal. First, the complementary outputs of the differential amplifier are differentiated and converted to uni-polar pulses by full-wave rectification. These pulses contain a discrete component of the PCM timing information (288 kHz) regardless of the message structure. Applying these pulses to an amplifier tuned to 288 kHz restores the periodicity to the pulse train. This 288-kHz signal is then used as the reference input to the timing extractor phase detector. The other input is 288 kHz produced by the binary division of the output of a 576-kHz vcxo. The 576-kHz vcxo is locked to the 288-kHz component of the incoming data and, after binary division and shaping, provides 288-kHz timing pulses for squelching the sampled integrators and triggering the decoder. The 576-kHz pulse train is used for timing by the local PCM.

Performance

A true phase-coherent phase-shift-keying system has a theoretical error probability given by Eq. 1:

$$p_e = \tfrac{1}{2}\left\{1 - erf\left[(E/N_o)^{\frac{1}{2}}\right]\right\} \quad (1)$$

where p_e is the error probability, E is the energy per bit, N_o is the noise density, and erf is the error function, such that:

$$erf\left[(E/N_o)^{\frac{1}{2}}\right] = \frac{(4\pi)^{\frac{1}{2}}}{\pi}\int_0^{(E/N_o)^{\frac{1}{2}}} \exp(-y^2)\,dy$$

To derive an equivalent expression for the error probability in a system using differential encoding, it is necessary to take into consideration the dependency on the previously received bit in making a decision. Let p_e represent the probability of a bit being "bad" at the output of the digital comparator following the sampled integrator. Then $(1-p_e)$ represents the probability that the bit is "good". There are four cases that can occur as listed in Table I.

Table I—Error probability in a system using differential encoding.

Case	Previous bit	Present bit	Decoded bit	Probability of occurrence
1	Good	Good	Good	$(1-p_e)\ (1-p_e)$
2	Bad	Good	Bad	$p_e(1-p_e)$
3	Good	Bad	Bad	$(1-p_e)\ p_e$
4	Bad	Bad	Good	$(p_e)\ (p_e)$

P_e is the probability of error in decoded output and is equal to the sum of the probabilities for the 2nd and 3rd cases of Table I.
Thus,

$$P_e = p_e(1-p_e) + (1-p_e)\,p_e = 2(p_e - p_e^2) \quad (2)$$

where p_e is defined in Eq. 1.

Table II shows the relationship between p_e and P_e.

A plot of Eq. 2 for various values of E/N_o expressed in dB is shown in Fig.

Table II—Relationship between theoretical error probability and probability of error in decoded output.

p_e	P_e
0.5	0.5
0.4	0.48
0.3	0.42
0.2	0.32
0.1	0.18
0.05	0.095
0.01	0.0198
0.005	0.0099
0.001	$\approx 2 \times p_e$
0.0005	$\approx 2 \times p_e$
0.0001	$\approx 2 \times p_e$

5. Also shown is a plot of data taken on the modem using a specially designed test set and a setup for establishing E/N_o.

Test setup

The test set generates a repetitive 8-bit message with all possible formats. It compares the recovered data with the transmitted data and displays the number of bit errors made per sampling interval. The number of bits transmitted per sampling interval can be adjusted from 160 bits to more than 16 million bits.

Examination of Fig. 5 shows that for high values of $(E/N_o)_{dB}$ differences of as little as 1 dB can cause an order of magnitude change in the error rate. Therefore, the accuracy of the technique used to measure (E/N_o) is extremely important.

Fig. 6 shows the setup used to establish E/N_o. Flat, broadband, gaussian noise is generated by cascading two high-gain 70-MHz IF amplifiers. The noise is passed through a variable attenuator to an adder. The signal is also brought to the adder through another variable attenuator. The adder output goes to a bandpass filter whose response has been carefully measured and plotted in terms of power ratio relative to the response at the center or carrier frequency.

The filter bandwidth is chosen so that when fully illuminated with noise from the noise generator, the total noise power through the filter is in the same range as the signal power: approximately 0 dBm. This allows measurements to be made at the more accurate power meter ranges with a minimum of meter range changing. The signal or carrier power, and the noise power can be measured separately by inserting 40 dB in either of the attenuators.

To determine E/N_o, the following procedure is used:

E is found by dividing the signal power by the bit rate.
N_o is calculated by dividing the noise power by the equivalent noise bandwidth of the filter which is the area under the filter power ratio response curve.
$(\text{Bit rate})_{dB} = 10 \log 288 \times 10^3 = 54.59$ dB
$(\text{Filter noise BW})_{dB} = 10 \log 10 \times 10^6 = 70$ dB

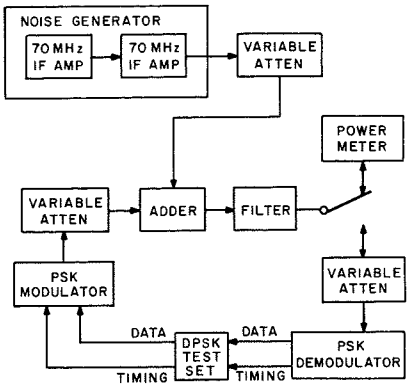


Fig. 6—Test setup to determine E/N_o.

A typical determination of $(E/N_o)_{dB}$ is as follows:

$(S)_{dBm}$ = signal power read on meter = −4.9 dBm
$(E)_{dBm}$ = −4.9 dBm − 54.59 dB = −54.49 dBm
$(N)_{dBm}$ = noise power read on meter = −0.2 dBm
$(N_o)_{dBm}$ = −0.2 dBm − 70 dB = −70.2 dBm
$(E/N_o)_{dB} = (E)_{dBm} - (N_o)_{dBm} = -59.49 - (-70.2) =$ 10.71 db

Test conclusions

Tests were also made to verify the ability of the timing extractor to maintain phase lock during a 100-bit period in which there are no phase transisitions: i.e., only binary 1's (marks) are transmitted. A 01010101 pattern is programmed into the test set. Normal operation is established with no errors being displayed due to lack of any noise being injected along with the signal.

By pushing a button on the test set, a sequence of 100 continuous marks is initiated. Since the bit comparator is referenced to a 01010101 pattern, error-free transmission during the period of 100 marks transmission will show as a numerical display of 50 on the error counter. Any variance from 50 indicates true transmission error caused by loss of phase lock in the timing extractor. Repeated testing has failed to yield a number other than 50 on the error counter.

Acknowledgment

The author acknowledges the contributions of several others to this project; in particular, Daniel S. Hall, B. E. Tyree, and George Cicero.

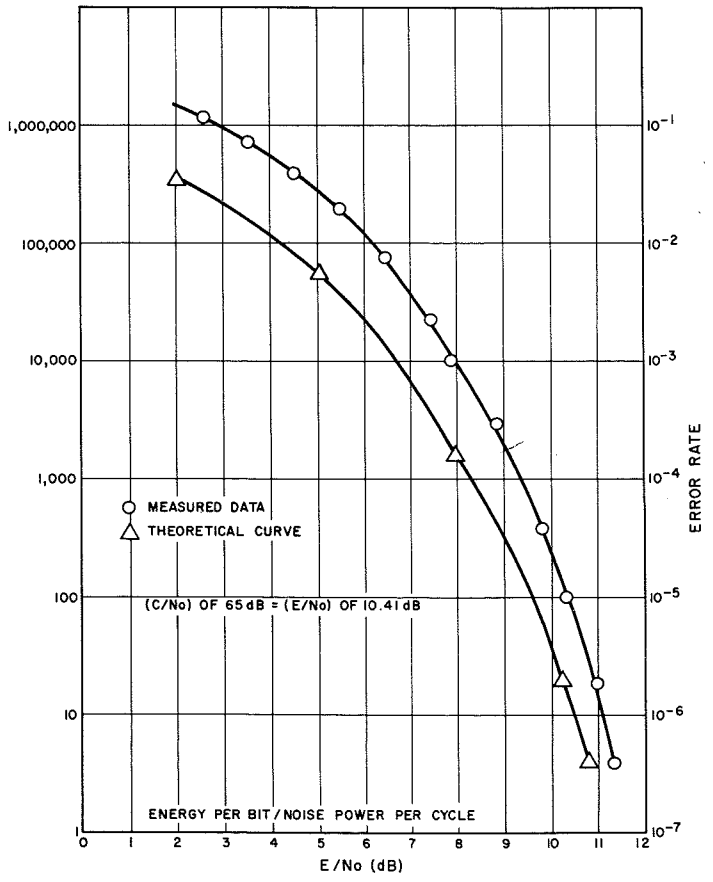


Fig. 5—Error rate vs. E/N_o.

Advances in threshold logic

D. Hampel | J. Beinart | K. Prost

This paper highlights advances made in threshold logic by the Defense Communication Systems Division over the past two years. The discussion starts with a brief background of the first integrated threshold gate. The approach to large-scale integration of threshold logic gates is shown, and some advanced LSI techniques, leading to even better performance, are discussed. A practical logic design is presented and compared with a conventional NAND-gate design. Improvements of 50% or greater were found in such factors as integrated chip area and *power-x-delay* product/logic function.

THRESHOLD LOGIC was given a boost during 1969 as a result of

1) The development of LSI amendable threshold gates,[1] and
2) The design study and evaluation parts of a NASA computer using these circuit techniques, including a comparison with a TTL implementation.[2]

Although threshold logic has been a rather obscure concept to most logic designers, Dr. R. O. Winder of the RCA Laboratories has recently brought the theory within the grasp of the logic designer and has related this theory to LSI threshold circuitry. Having an understanding of the theory as well as a circuit approach should allow the logic designers to put threshold logic to practical use.

Threshold gates, although they have binary input and output signals, have an internal analog summing point which measures the state of the weighted inputs. This feature allows the gate to distinguish input conditions other than all *lo* or all *hi*—which is all that a Boolean gate can do. This analog signal is "digitized"—to a 1 or 0—depending on whether the gate's threshold is exceeded. For example, a gate with 5 binary inputs can be specified to have a *hi* binary output for 2-out-of-5 of its inputs *hi*, 3-out-of-5 of its inputs *hi*, etc. The 1-out-of-5 case is simply an OR gate and the 5-out-of-5 an AND gate. By giving inputs different weights, their effects on the sum point are varied. The implication of all of this is that, in general, a threshold gate performs a wider range of logic functions than a Boolean gate.

In Fig. 1, the output of the 3-input gate is a function which would otherwise require three or four Boolean gates. As will be seen, the circuitry which does this preserves good noise immunity, is easy to integrate, results in the use of fewer components to do a given function and possesses a better *power-x-delay* product for a given function when compared to conventional implementations.

Reprint RE-16-3-4
Final manuscript received April 8, 1970.

Background

In 1966-67, Dr. Winder initiated and worked with Defense Communications Systems Division and Electronic Components in a company-funded program to design and integrate a dual threshold gate for use in a 14-pin package. This gate was compatible with existing families of emitter-coupled logic (ECL). Boolean logic designs at that time would have used dual four-input OR/NOR gates and would have compared to the threshold packs in the following manner; the threshold designs had

1) Fewer packages (½ to ⅓);
2) Fewer interconnections between packages (½ to ⅓);
3) Equivalent noise immunity and fan-out;
4) Equivalent or higher speed (depending on function);
5) Equivalent or lower power (depending on function); and
6) Slightly higher price per package (20%).

The logic schematic of the integrated circuit package is given in Fig. 1. One of the gates is a 3-input majority gate; the notation used to describe this gate is $(1,1,1;T=2)$ denoting a 3-input gate in which each input is weighted 1 and threshold is 2.

The other gate in Fig. 1 is a 5-input threshold gate $(2,2,1,1,1;T=4)$. The circuitry uses nonsaturating current switches; a summed current signal proportional to the number of *hi* inputs is compared to a signal proportional to the *lo* inputs. The threshold of the gates is the (sum of weights +1)/2. Before we had a chance to build equipment to prove this, the technology was already up to MSI and LSI. This presented a whole new ballgame for threshold logic, since any research and development on new logic circuits would have to incorporate the latest thinking on integration complexity. In 1968-69, the Air Force sponsored a program, in conjuction with the RCA Laboratories and Electronic Components, to explore new circuit techniques. The approach chosen is based on the intraconnection of current switches, summing resistors, and appropriate clamp and output devices to form a variety (as required) of threshold gates on a chip. Thresholds can be set at any value; the gates can then be interconnected to realize any given logic function.

Definitions

Threshold logic—the underlying theory on the analysis of logic functions and their synthesis with threshold gates.

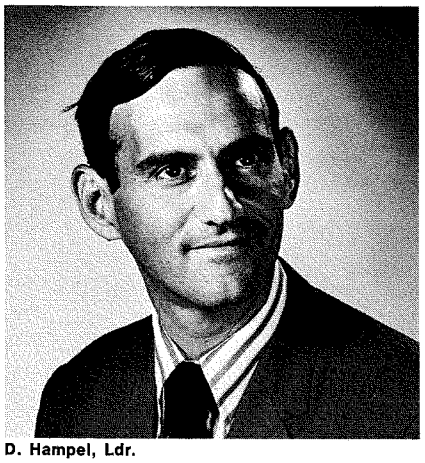
Threshold gate—a gate which accepts some number of binary inputs and gives a binary output. The inputs are weighted and the gate possesses a threshold. The output is representative of whether the sum of the weighted inputs exceeds the threshold or not.

Majority gate—a threshold gate in which the total number of inputs is odd, each possessing a unity weight; threshold = (the number of inputs + 1)/2.

Boolean gate—The NAND, NOR, etc. gates commonly used in logic design. In relation to threshold gates, the OR gate has all inputs equally weighted and has a threshold of unity; the *AND* gate has all inputs equally weighted and has a threshold set at its maximum (equal to the number of inputs).

The LSI threshold gate

This concept will now be explained in a little more detail. Fig. 2 shows the



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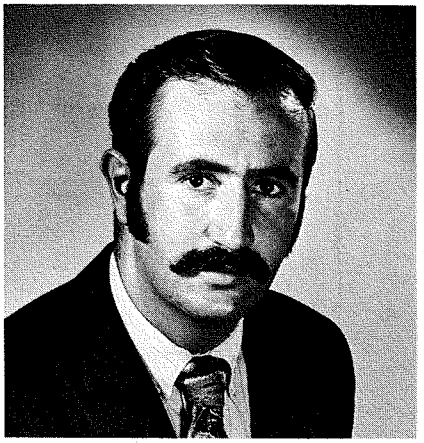
received the BSEE and MSEE from the Newark College of Engineering in 1953 and 1958. In addition, he graduated from the Communications Development Training Program at the Bell Telephone Laboratories in 1956. From 1953 to 1957, as a Member of the Technical Staff with the Bell Telephone Laboratories, Electronic Switching Systems, Mr. Hampel designed and developed circuits for application in the Electronic Central Office, including digital code translation, selection, and amplification circuits. As a Senior Engineer with ITT from 1957 to 1960, he worked on a program employing a digital computer and a special-purpose data processing system to perform correlations and statistical analyses of communications data. Mr. Hampel joined RCA in 1960, and until 1962 was a project engineer at the Nuclear and Scientific Services department of the Service Company where he designed computing circuits for data handling systems for nuclear experiments. Upon joining DCSD in 1962, Mr. Hampel worked on logic circuits for command and control systems. Mr. Hampel assumed his present position in 1967 and has been in charge of threshold logic development as well as circuit techniques for radiation hardening. Present programs include circuit design for integration and design of functional LSI circuits. Mr. Hampel is the author of several papers in the digital techniques area and is a member of Tau Beta Pi and IEEE.



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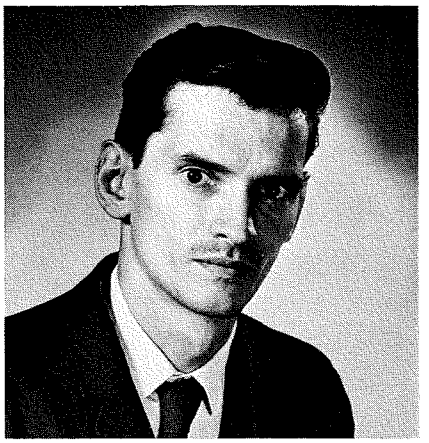
received the BSEE in 1965 from City College of New York and the MSEE in 1968 from the University of Pennsylvania. Upon joining RCA in 1965, he was a circuit design engineer in a digital techniques group in Camden. He designed numerous circuits for such government contracts as Minuteman II, Apollo VHF ranging/digital ranging generator, and air-borne launch control command; he has also been responsible for reliability and evaluation tests of various families of IC's. Starting with the Advanced Digital Techniques Group in 1968, he worked on the circuit theory and all the related areas of design which led to the integration of a family of threshold-logic circuits. This work consisted of optimization of circuits by computer analysis, design rules for the use of the circuits, and the construction of the masks and layouts used for the actual integration. Most recently, working with the RCA Laboratories he helped design and construct a 256-word MOS scratch-pad memory which was used for the LIMAC computer, and is now working on integrated drive and sense circuit for an MOS random access memory.



K. Prost
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attended RCA Institutes during 1947 and 1958. He studied at Hofstra University and City University of New York, evening session, from 1958 to 1962. From 1958 to 1963, Mr. Prost worked for the Arma Corp. in Long Island. During this time he worked on system test, quality control, and field engineering of the inertial guidance system for the Atlas Missile. From 1963 to 1965, he was with IBM Corporation, in the Test Equipment Engineering Department. Here he wrote test procedures for automatic checkout of digital circuits, and initiated changes for existing test equipment. Mr. Prost joined DCSD in 1966, and was assigned to the Advanced Digital Techniques Group. Since joining the group he has been involved in work on integrated threshold gates, logic design, and radiation effects testing. In these areas, Mr. Prost has assumed responsibility for breadboarding, testing, and layout for integration.

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schematic for a threshold gate composed of the basic modules referred to previously. Each input is compared to a locally generated reference potential via a differential (or current) switch. In this system of logic, the reference, V_{ref}, is precisely ½ the power supply voltage, V_{ps}, so that if $V_{ps} = -4$V, then $V_{ref} = -2$V. The inputs are regarded as *hi* (one) if they are more positive than V_{ref} and cause the input side transistor of the current switch to conduct; and they are *lo* (zero) if they are more negative than V_{ref} in which case the reference-side transistor would conduct.

The amount of current controlled by each input is determined by the weighting resistors $R_1, \cdots, R_n$. If 2 mA is decided upon for a weight of unity, then an R_i of about 600 ohms is used (assuming $V_{ps} = -4$). If a double weight is desired, the R_i can be halved to about 300 ohms, etc. Now, these currents are summed through resistors, R_{S1} and R_{S2}, connected to the sum points—the common collector connections of the input side transistors and reference side transistors. These points simply connect to output emitter followers which can then be used to feed other gates. The output is considered *hi* or *lo* depending upon whether it is above or below the V_{ref}. *The summing resistors determine the threshold of the gate.* Qualitatively, if R_{S1} is large, fewer *lo* inputs are required to pull the output below the reference—a high threshold. The converse is true if R_{S1} is small. The R_{S2} resistor provides an inverted output as well as enabling the double diode clamp with a source and current supply to limit the otherwise wide excursion of potential at the sum points. Only the signal swing immediately about the reference is important as long as it has reasonable noise immunity (a couple of hundred millivolts).

Hence for a n input gate, summing resistors can be chosen for any desired threshold—the output *hi* for m or more out of n inputs *hi* ($m \leq n$).

For example, for a unity weight-determining resistor, R, and for a total number of weighted inputs, n, the summing resistor R_{S1} for various thresholds is:

Theshold	R_{S1}	*Function*
1	$2R/(2n-1)$	OR
.		
.		
.		
$n/2$	$2R/n$	MAJORITY
.		
.		
.		
n	$2R$	AND

The output is centered at the reference for each particular input condition equal to the threshold, independent of power supply variations or temperature. If V_{ps} varies, V_{ref} varies accord-

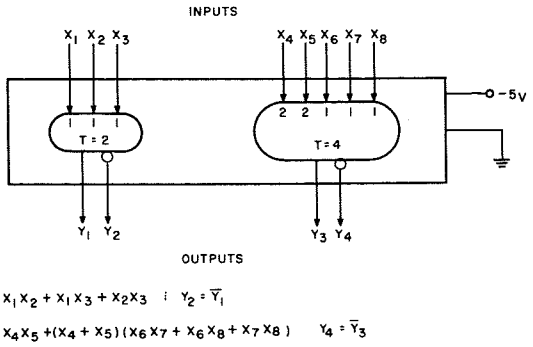


Fig. 1—First IC threshold gates (compatible with emitter-coupled logic).

ingly. If V_{be} varies due to temperature, the weighting current varies, but the output emitter follower provides an equal and opposite variation for compensation.

The prime fabrication requisite is the maintenance of a fairly good ratio among the weight and the summing resistors. Ratios of ±2 to 3% are adequate and are easy to achieve. Beta and V_{be} matching are also necessary and fall within required tolerance in monolithic integration without any special precautions.

Techniques for increased logic

Three other concepts applied to this circuit approach provide even more flexibility:

1) The use of the OR function in conjunction with any input to a threshold gate;
2) The use of different summing resistors for the complementary outputs to provide two different functions simultaneously; and
3) The use of double-level switching in combination with the threshold gate.

Use of the OR function

Additional inputs—parallel transistors on each current switch—can be superimposed as shown in Fig. 3. Thus, the OR function is provided for that switch —over and above the function of the threshold gate. One can then have OR-MAJORITY, OR-AND gates, and etc.

Double function threshold gates

In Fig. 4, the inverted-side summing resistor, R_{S2}, is specified for a 3-input majority gate (a minority gate in this case) while R_{S1} can be shared by other current switches, if desired, to provide for a different threshold. For the case where the 3 inputs represent the inputs to an adder, the inverted output is C_o'. If this feeds a double-weighted switch

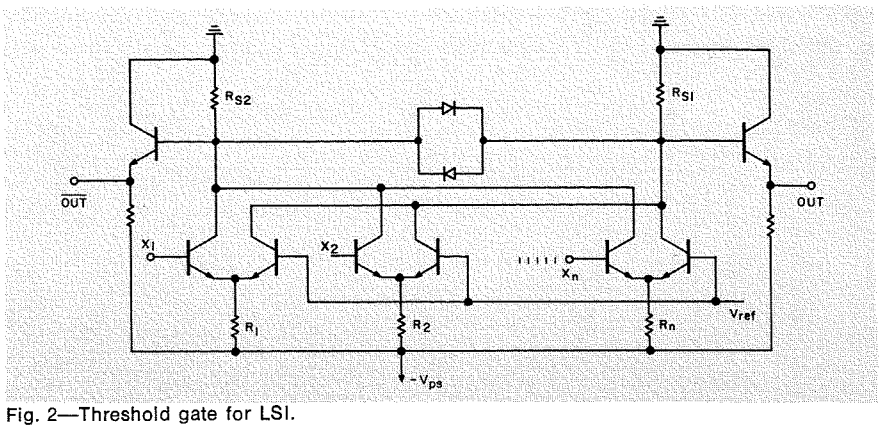


Fig. 2—Threshold gate for LSI.

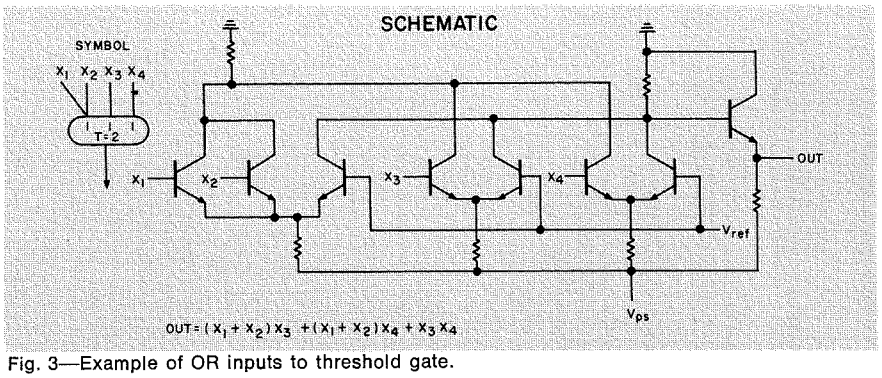


Fig. 3—Example of OR inputs to threshold gate.

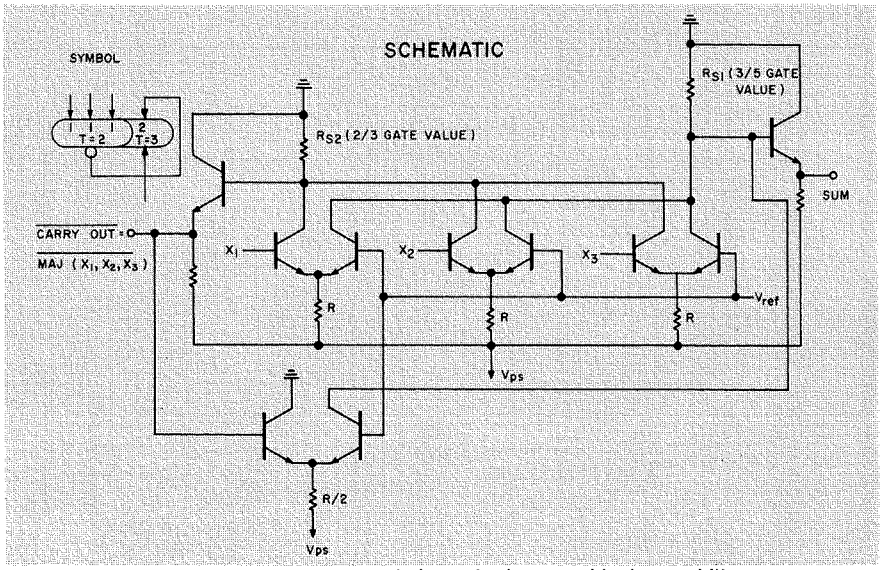


Fig. 4—Double-function threshold-gate techniques for increased logic capability.

	No. of components	*No. of connections*	*Avg. delay (ns)*	*Avg. power (mW)*	*Power×delay (mW−ns)*
8-bit parity					
Threshold logic	79	11	32	248	7,940
TTL	210 to 280	61	87	366	31,800
L1 character					
Threshold logic	1133	—	30 to 45	1820	54,600 to 81,000*
TTL	2100	—	60 to 90	3000	180,000 to 270,000*
Configuration assignment unit					
Threshold logic	68	24	30	124	3,720
TTL	154	41	86	186	16,000

*Depending on logic being performed

Table I—Summary of comparison between threshold logic implementation and TTL:

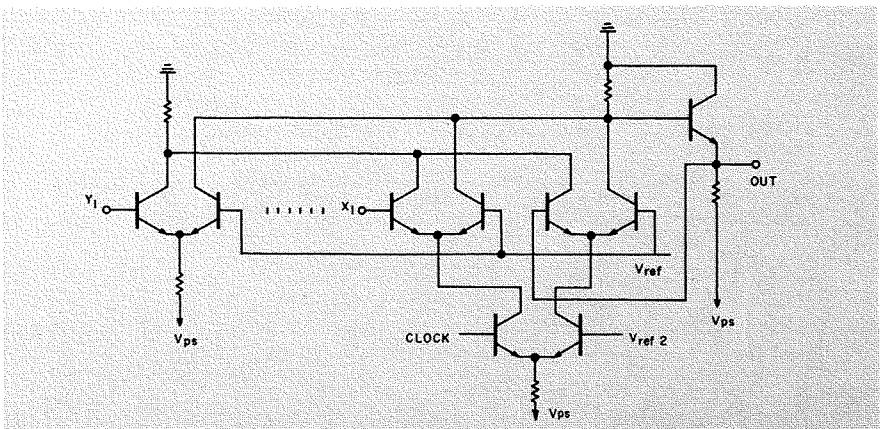


Fig. 5a—Double-level switching applied to threshold gate.

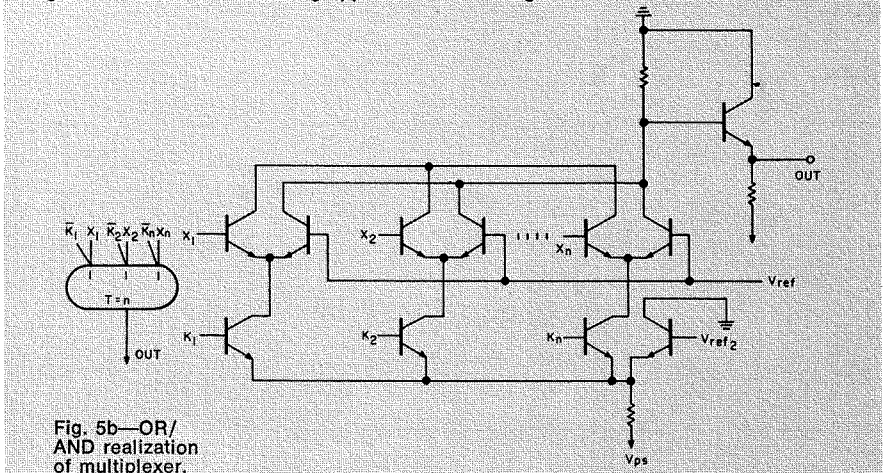


Fig. 5b—OR/AND realization of multiplexer.

Fig. 5c—Double-level multiplexer.

which then sums on R_{S1} as well, the output is the sum. The 3-input gate plus one additional switch replaces the two gates in the well-known adder as shown in the logic symbol of Fig. 4. Note that 3 connections are also saved in the process. The 3 inputs are not repeated for the lower gate in the conventional threshold logic adder.

Double-level switching

Double level switching, commonly applied to ECL circuits, can be applied to threshold circuits. One example of its advantage is shown in Fig. 5, a gateable flip-flop. A clock waveform controls the lower level switch while the threshold gate, formed by the upper switches, can perform logic in the regular manner.

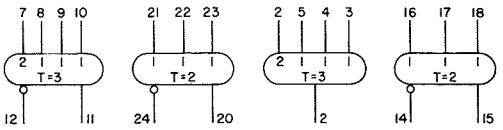
When the clock is *hi*, the inputs are in control; when the clock is *lo*, because of the feedback connection, the output is in control. A master-slave flip-flop contains two such units with the clock feeding opposite sides of the lower decision switch on each unit. This double-level technique is also useful for multiplexing and switching applications where it is desired to switch any one of X_n inputs under the control of K_n control lines.

Integration

The demonstration of the basic circuit technique was shown by alternately metallizing the components of an integrated circuit, containing about 50 transistors and 50 resistors, in a number of ways to form various threshold gates. The integrated chip was about 65x65 mils and was placed in a 24-pin dual-in-line package. The connection patterns resulted in the following packs:

1) A dual adder;
2) Three OR-AND gates plus an inverter
3) Two OR-MAJORITY gates and an OR-AND gate;
4) A 9-input gate with total weight of 11 and threshold of 6; and
5) A group of level shifters to work in and out of ECL integrated circuits.

The circuits switch in the 5- to 10-ns range, meet all design objectives, and show the feasibility of their uses in



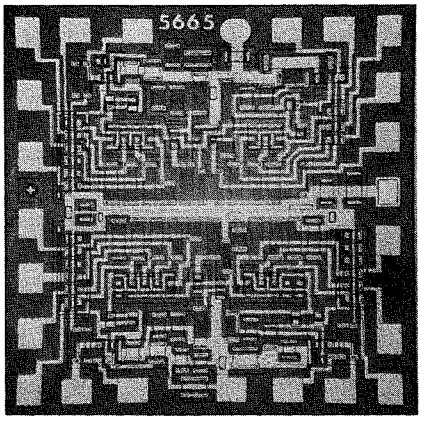


Fig. 6—Threshold logic dual adder chip.

LSI. Fig. 6 shows one of the integrated threshold logic chips with its logic diagram. Fig. 7 shows the schematic of the same chip.

Application to computer circuits

Parts of a computer were designed using the threshold gates and associated circuit techniques, and comparisons were made with existing designs based on the use of TTL logic. The comparisons for a particular function were made in the following areas:

1) *Number of components*—the total of all transistors and resistors to be integrated;
2) *Connections*—the inter-gate metallization requirements; and
3) *Power-x-delay*—a measure of the efficiency of the circuit in performing its function.

These parameters, in turn, relate to chip area requirements and circuit power for a given delay. For the functions studied, component layouts were made and delays calculated from experimental data on integrated threshold gates.

The computer circuits were part of the highly reliable developmental NASA Modular Computer (MC)[2]. This computer consists of triple redundancy modules which are connectable to form three parallel working computers; a single set of modules can be connected to form one computer.

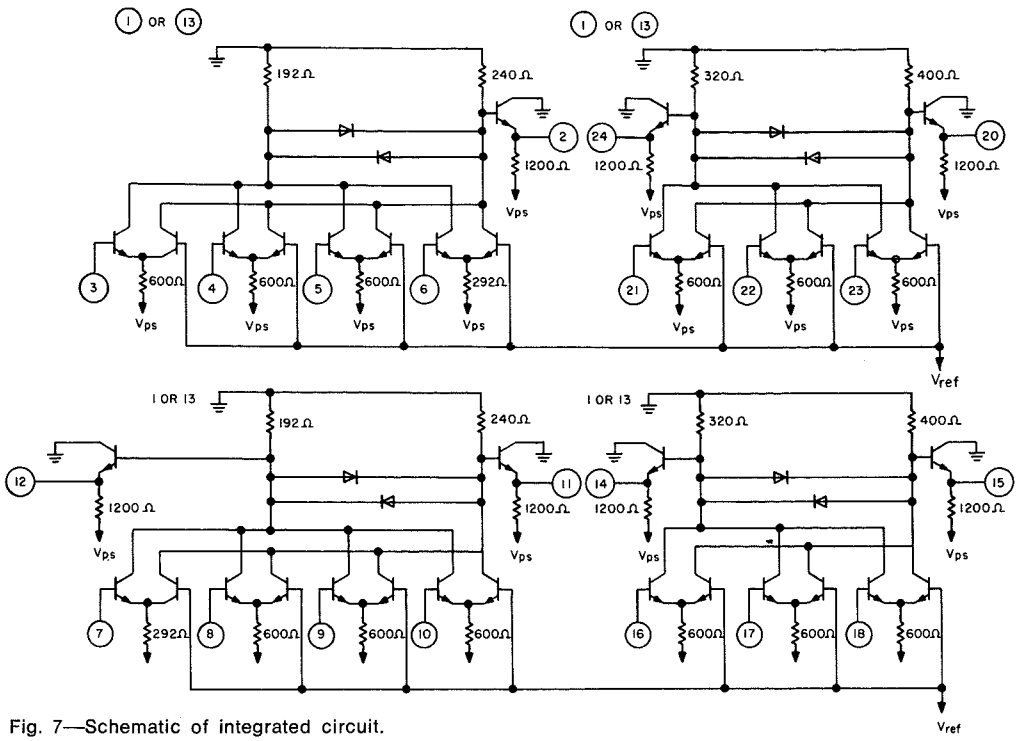


Fig. 7—Schematic of integrated circuit.

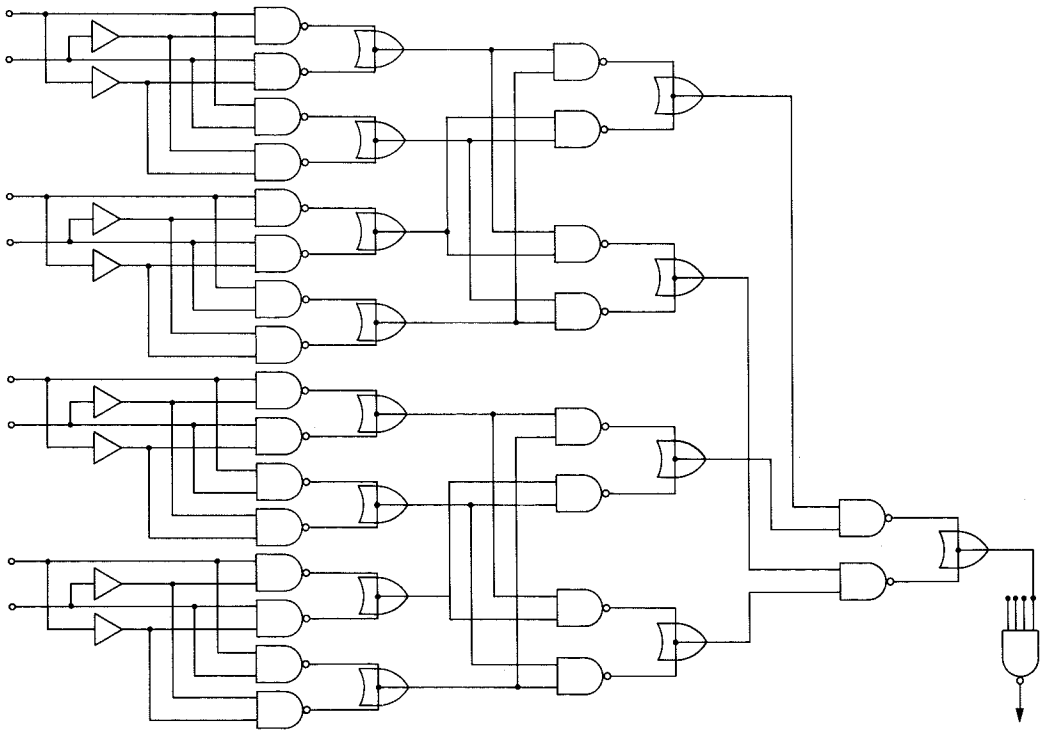


Fig. 8a—NAND gate logic for 8-bit parity.

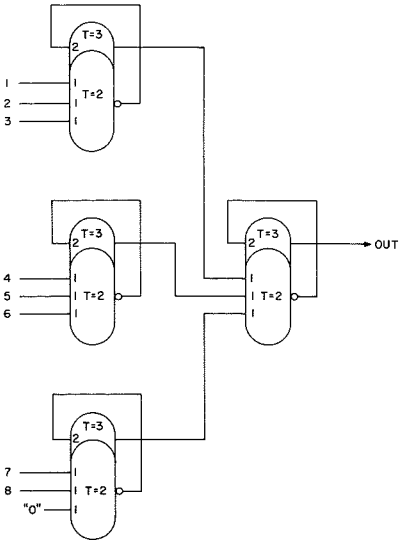


Fig. 8b—Threshold logic parity circuit (8-bit).

The various circuits of this computer which were studied in detail for threshold logic evaluation are the following:

1) Parity circuit (of possible use throughout the machines);
2) General logic character (one of the ten functional building blocks of whole computer); and
3) A portion of the configuration assignment unit (CAU—the unit which interconnects the modules of the computer).

Fig. 8 shows the optimum threshold gate realization and the NAND gate logic for the 8-bit parity.

Comparisons with NAND gates

The comparison of these three circuits is summarized in Table I. The trend is clear; threshold logic provides a significant savings in all important LSI characteristics. If comparisons were made with Emitter-Coupled Logic (ECL) rather than TTL, the savings would be comparable. Although the speed of ECL is higher, the *power-x-delay* product—a measure of the efficiency of a logic circuit—would be about the same. Level-shifting circuits can be added to make the inputs and outputs of the logic group compatible with ECL or saturated logic circuit families.

Conclusions

If custom chips were required for a particular job and if the threshold logic version needed half the area or used half as many chips, why not use it? This assumes, of course, that compatibility be maintained; with chips having a large gate to pin ratio—an existing goal in LSI—the added buffer requirements still result in improved circuits with the threshold gates.

In general, the approach can be viewed as circuit "tricks" which result in a more efficient way to realize most logic functions. Instead of being restricted to predefined blocks, performing basic Boolean functions, circuit components are intraconnected to do complex logic in what is defined as a threshold gate. The theory for doing this, coupled with a library of functional designs which are easily modified to suit particular applications can be readily applied by the logic designer.

References

1. *Integrated Threshold Logic,* AFAL-TR-69-195, RCA Final Report (June 1969).
2. *Threshold Logic Implementation of a Modular Computer System Design,* contract NAS12-2130, RCA Final Report (Oct. 1969).

Drive-point impedance of output networks for broadband power amplifiers

W. N. Parker

A frequent performance objective in the design of broadband power amplifiers is a specified minimum power output over a specified minimum band of operating frequencies.[1,2] A curve relating power output to frequency is known as a "response" curve. The effect of the output circuit on this response is closely related to the drive-point impedance because the *R* component of the impedance is equal to the load resistance presented to the modulated electron stream of the amplifier. Consequently, a plot of *R* as a function of frequency corresponds to the power-output response for a given AC plate current. A high-performance output-circuit design, therefore, is one in which *R* is high and relatively constant over the specified bandwidth. Such a design might also be said to have a high figure of merit, *F*, and a low response-variation factor (or ripple) *V*. These terms are described below and shown to be useful in comparing the response curves of various designs with each other and with the theoretical responses of "optimum" lumped-constant filter networks. Effects of the reactance component of the drive-point impedance are also discussed.

THE SPECIFIC FIGURE OF MERIT F used in this discussion is the ratio of the *actual* $R \times BW$ (resistance-times-bandwidth) product to the *maximum* $R \times BW$ for a simple parallel resonant output circuit utilizing the same amplifier output capacitance C. This product is similar to the power-times-bandwidth product referred to by Greene[3] except that the *minimum* power is used rather than the maximum. The minimum-power basis is more useful when the power output over the frequency band must equal or exceed a specified amount. The resistance R in the $R \times BW$ product corresponds to the height of a rectangle which just fits under the response curve, as shown in Fig. 1. The width of the rectangle is equal to the bandwidth BW. Obviously, a variety of such rectangles may be constructed, each having a corresponding $R \times BW$ product.

The resistance value used for the response curve is the real component of the drive-point impedance presented to the electrons moving across the active output region of the amplifier, e.g., the grid-plate region of a Coaxitron tube. For a given modulated electron current, I, this drive-point resistance value is proportional to the power output P according to the familiar relation $P = I^2R$. Consequently, the response curves correspond to power output as a function of frequency and measure the performance of the output circuit alone. The output circuit design which provides the greatest value of F also provides the greatest minimum power for a given bandwidth or, conversely, the greatest bandwidth for a prescribed power output.

Response-variation factor V

Another frequent specification for broadband power amplifiers is the maximum allowable variation of power output over the prescribed bandwidth. Because power output is proportional to the drive-point resistance, the response-variation factor

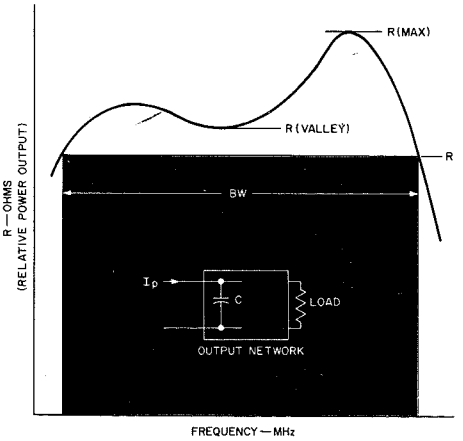
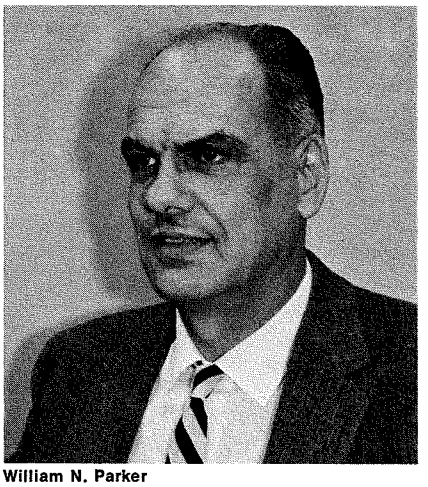


Fig. 1—Typical broadband amplifier output network response.

Reprint RE-16-3-11 (ST-4296)
Final manuscript received May 26, 1970.



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received the BSEE from the University of Illinois in 1928. At General Electric Co. Schenectady, N.Y., he participated in the Advanced Course in Engineering and in the testing of developmental power tubes. From 1929 to 1941 he pioneered in television development with Stewart Warner and the Western Television Corp., Chicago, Ill., and with Philco Radio and Television Corp. in Philadelphia, Pa. At Philco he directed the TV development and experimental broadcasting using novel high fidelity modulation and single sideband transmission. After two years with the U.S. Govt. Army-Navy Expediting Agency, Philadelphia, Pa., he joined RCA at Lancaster, Pa. in 1943, to assist in the development of super-power tubes and equipment capable of generating up to a megawatt of CW power, and high power UHF tubes. In 1953 he became manager of the super power department. As a Staff Engineer starting in 1955, his investigations included anode thermal stresses, design of the ultra high vacuum system for the "C" Stellarator, and the microwave processing and freeze-drying of foods. He was also directly responsible for the design of the first Coaxitron, a UHF triode whose bandpass circuitry is inside the vacuum envelope and whose dimensions are determined by computer. He holds 20 patents and is the author of numerous technical articles. He is a registered Professional Engineer in the state of Pennsylvania, a Senior Member of the IEEE, and a member of Eta Kappa Nu, Sigma Xi, Pi Mu Epilon, and Theta Tau. Mr. Parker is listed in *American Men of Science*.

V may be defined as the ratio of the maximum drive-point resistance $R(max)$ to the R used for the corresponding $R \times BW$ product, as shown in Fig. 1. The $R \times BW$ product is obviously a function of V for a given response curve. Some shapes of response curves provide larger values of $R \times BW$ (and thus F) for a given V than others, as discussed later and shown in Figs. 6 and 10.

Output-circuit design

The output-circuit configuration used in Coaxitron Amplifier tubes,[1,2] which is shown in simplified form in Fig. 2, is representative of UHF and microwave broadband devices. The equivalent circuit, shown in Fig. 3, consists

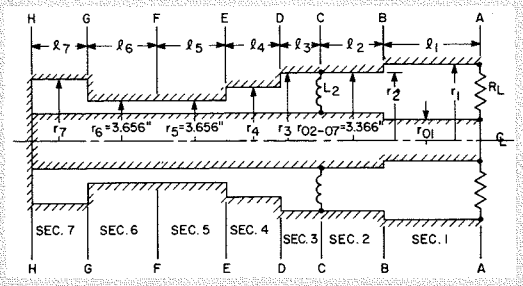


Fig. 2—Cross-section of generalized coaxial circuit for double-tuned cavity.

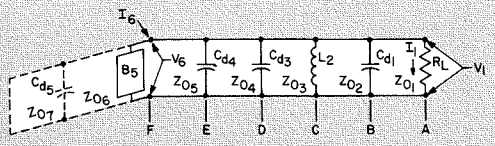


Fig. 3—Equivalent circuit.

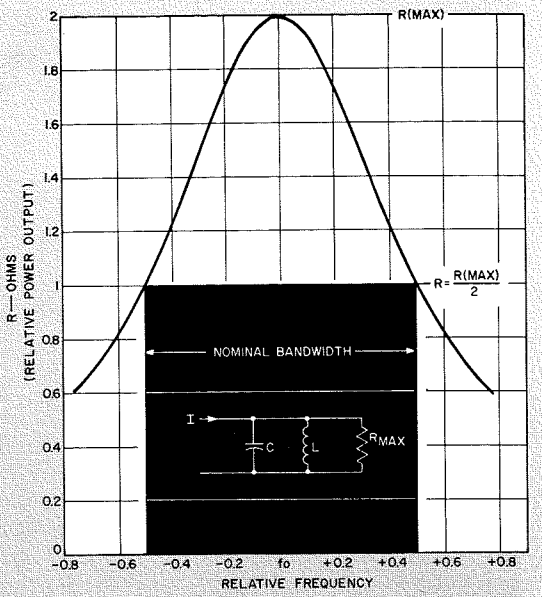


Fig. 4—Single-circuit response. The *R x BW* product at the nominal (3dB) bandwidth corresponds to unity figure-of-merit *F*.

of several sections of transmission line Z_o, discontinuity capacitances C_d, coupling inductor L_2, and load R_L. An electron current I_6 is assumed to be injected at a plane F at the center of the grid-plate region. One practical design procedure consists of selecting various sets of dimensions and calculating the drive-point impedance as a function of frequency at the plane F for each set. A convenient technique for calculation determines the complex voltages and currents at each point along the circuit, starting at the load and working back to the drive point. A computer program called DIPNET is especially suitable for calculating such transmission-line networks.[4] This cut-and-try procedure is repeated until an acceptable response curve is obtained. The design obtained may or may not be optimum in that the figure of merit F may or may not be the highest attainable for a given V and output capacitance C. For a complex circuit such as the one shown in Figs. 2 and 3, attempts at rigorous optimization usually lead to an awkward expression involving transcendentals. However, the degree of optimization achieved may be judged by comparison with standard response curves.

Standard response curves

Fortunately, modern filter theory[3, 5-7] provides "optimum" designs for lumped-constant networks which yield maximum values of F for a given degree of complexity and C, the effective capacitance of the output circuit. Each of these "optimum" designs has a corresponding standard response curve of a definite shape. It is believed that an output circuit consisting of a multiplicity of transmission lines and other components, such as that shown in Figs. 2 and 3, but having a response curve of the same shape as one of the standard response curves, will also be an "optimum" design. Although no attempt is made in this paper to prove this belief, experience with several Coaxitron output circuits seems to confirm this behavior.

The standard responses predicted by modern filter theory are classified as Type B or C. Another class of filters, the "Bessel"-response type, is optimized to provide the most linear phase shift (or flattest time delay). For each type, the response shape varies with the number of elements or complexity. Type C responses may be further classified by the amount of ripple or V. Type B and C networks and their corresponding responses are discussed later, after a brief review of the behavior of the single parallel resonant circuit used as a reference.

Single-circuit response

The simplest response shape for an RF amplifier consists of a single bell-shaped curve, as shown in Fig. 4. The capacitance of the tuned circuit is equal to the C of the amplifier active output region. For the shunt loaded circuit shown, $R(max)$ is equal to the load resistance. The response (drive-point resistance) drops to half value on each side of resonance when the susceptance of the circuit equals the load conductance. It should be noted that the half-resistance points on the response curve correspond to the 0.707 voltage amplitude points used by Green[3] and others. The bandwidth between these half-resistance (half-power) points is called the "nominal" bandwidth and may be expressed as follows:

$$\text{Nominal } BW = 1/2\pi CR(max)$$

At this same nominal bandwidth, the $R \times BW$ product is given by

$$R \times BW = 1/4\pi C$$

This $R \times BW$ product is used as a reference and is assigned an F value of unity because it can be shown to be the maximum $R \times BW$ that can be obtained for a single-circuit response. The relative variation in $R \times BW$ with V (i.e., $R(max)/R$) for the single circuit is shown later (reference curve for $n=1$ in Fig. 6). A broad maximum of F equal to unity occurs at $V=2$.

Type B response

The type B response, often called "Butterworth" or "maximally flat", is obtained by simple addition of circuit elements. As shown in Fig. 5, the typical response peaks are relatively broad and flat. One form of circuit consists of two or more tuned circuits in cascade with critical coupling be-

tween them. The capacitance for the tuned circuit at the drive point is made equal to the C of the amplifier active output region, as described previously. The other circuit parameters are then determined by modern filter-design methods[3, 5-7] to provide a type B response with optimum $R \times BW$ performance. The nominal bandwidth, used for Type B circuits is defined at the half-power bandwidth, as in the case of the single circuit.

Lumped-constant ladder networks of series-resonant series arms and parallel-resonant shunt arms may be used; these networks are equivalent to n coupled circuits, where n is equal to the total number of series plus shunt arms.

The $R \times BW$ products for type B responses are greater than those for the reference single-circuit response. Consequently, the F values are higher. As more circuits are added to the network, the F continues to rise (if circuit losses are neglected) to a maximum value of 3.14 for $n = \infty$, as shown in Fig. 5. The actual response in this case is a rectangle, i.e., $V = 1$.

Fig. 6 shows the variation of F with V for two-circuit ($n=2$) and three-circuit type B optimum networks. In each case, the maximum F occurs at a value of V considerably below 2 and, consequently, at a bandwidth less than the 3-dB bandwidth. As a result, a type B response yields a higher $R \times BW$ product if the network is designed for a nominal (3-dB) bandwidth greater than the bandwidth needed or utilized. The effect of circuit broadening is shown in Fig. 7.

Type C response

The type C, or Chebyshev, band-pass response is characterized by alternating peaks and valleys that form a "ripple", as shown in Fig. 8. The peaks are all the same height and the valleys all the same depth. The circuit is basically the same as that for a type B response, except that different values are used for the parameters. In particular, the coupling is increased; as a result, this type of response is sometimes called an "overcoupled response".

The number of peaks occurring over the pass-band (of a bandpass response) is equal to the number of tuned circuits in cascade; i.e., a pair of coupled circuits ($n=2$) provides the familiar double-humped bandpass response, and so on. For odd values of n, a peak occurs at the center frequency of the response.

The design bandwidth for type C responses is usually measured at the "valley" value of R. The highest value of $R \times BW$ is obtained when R is equal to R *(valley)* because the largest "rectangle" occurs at this point. No improvement in $R \times BW$ (and F) is obtained by use of less than the nominal or design bandwidth. In fact, F tends to drop proportionally, as shown by the various straight-line characteristics of type C responses in Fig. 7.

The maximum $R \times BW$ (and F) that can be obtained with type C responses depends upon the number of circuits n and the ripple factor selected, as shown in Fig. 9. These curves show, for example, that the best two-element network is a design having a 1.0-dB ripple, and the resulting F value is 2.0. The best four-element design is one having a 0.5-dB ripple, and so on.

Fig. 10 shows similar information in the form of F as a function of V for several values of n. In this case, V always corresponds to the ripple value. The single-circuit reference ($n=1$) is also shown as it was in Fig. 6.

Comparison of Fig. 10 and Fig. 6 indicates that, for a given complexity (n) type C responses provide a generally higher value of F than type B responses. For example, a two-element type C network designed for a ripple of 1.3 (or 1.1 dB) has an F value of 2.0, as compared to a maximum F value of 1.6 for a two-element type B network. The V values are nearly the same for the two networks. In addition, as with the type B responses discussed previously, the ideal rectangular response curve is approached as n is increased and the ripple decreased, i.e., the value of F becomes equal to 3.14, as shown in Figs. 8 and 9.

Lumped-constant ladder networks

The "optimum" network parameters that provide the "standard" response curves referred to above have been tabulated by Weinberg.[6, 7] The tablulated values pertain specifically to low-pass, lumped-constant ladder networks, although values for high-pass and bandpass networks may easily be obtained. All values are normalized to a nominal bandwidth of one radian per second. The response for a bandpass network is similar in shape to the corresponding low-pass response with the zero-frequency axis shifted to the mid-band frequency and a mirror image added on the low-frequency side. It is important to note that the *total* bandpass in hertz is equal to the *low-pass band* of the corresponding network for the same value of V and drive-end C. Consequently, the $R \times BW$ and F values are identical for low-pass and corresponding bandpass circuits.

For type C responses with even values of n, the factor F is simply twice the

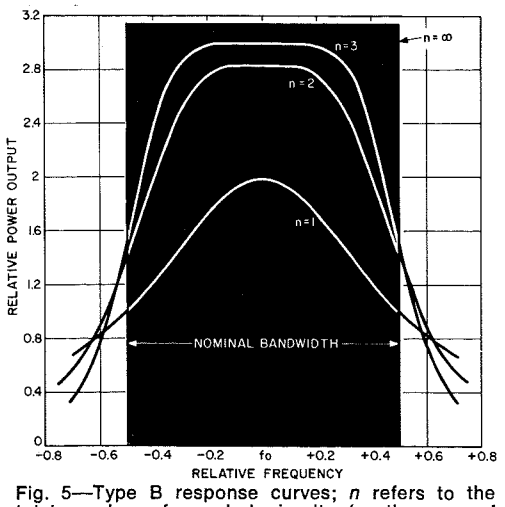


Fig. 5—Type B response curves; n refers to the total number of coupled circuits (or the sum of the series and shunt arms in a ladder network).

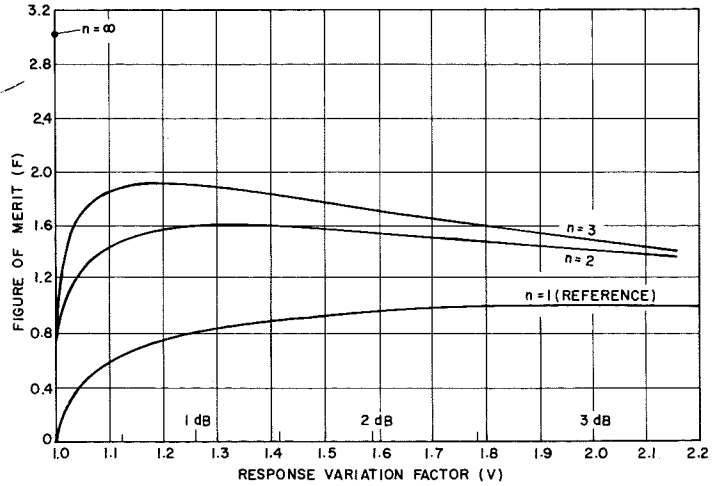


Fig. 6—Figure-of-merit vs response variation factor for type B optimum networks.

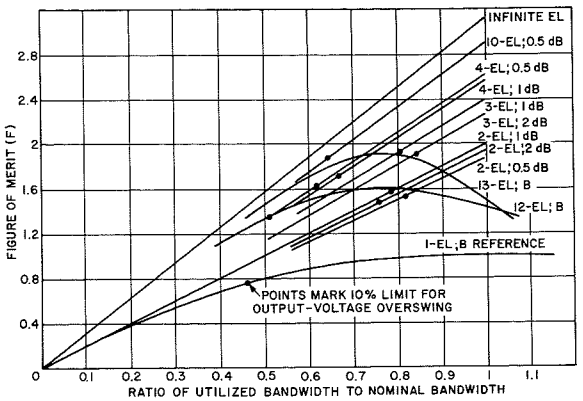


Fig. 7—Effect of circuit broadening on figure of merit, *F*.

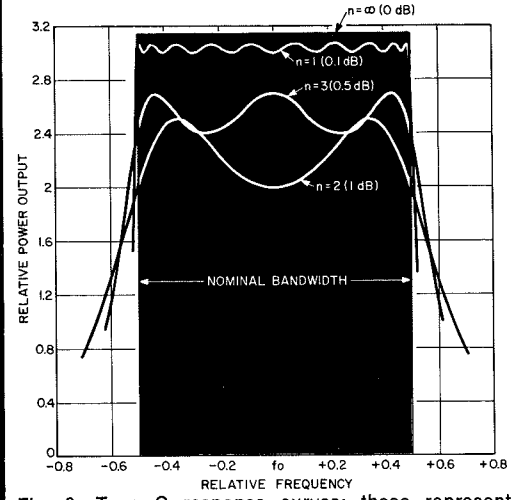


Fig. 8—Type C response curves; these represent but a few of the many combinations of *n* and response variation factor *V*.

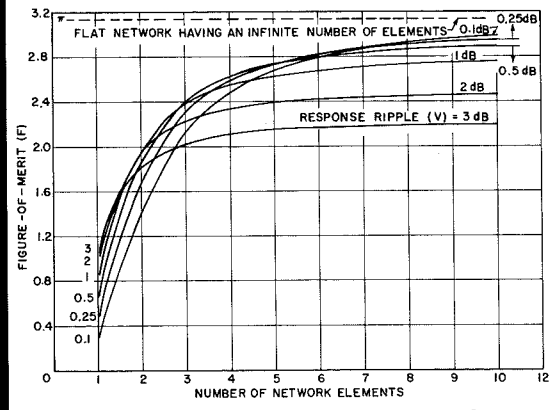


Fig. 9—Relative figure-of-merit, *F* for type C networks and small signal amplitudes.

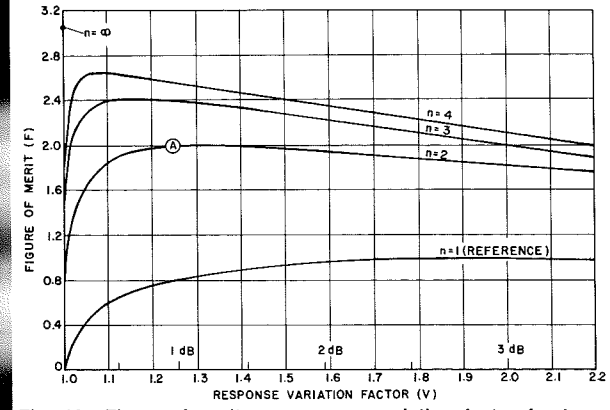


Fig. 10—Figure-of-merit vs response variation factor for type C optimum networks.

appropriate value of C_n listed in Weinberg's tables (for $r=0$ at the drive end) because C represents the drive-point capacitance which can be "tolerated", as compared with $C=1.000$ for the single-circuit reference. For odd values of n, the tabulated values for C_n must first be reduced by the amount of the ripple because a response peak occurs at zero frequency instead of a valley. This reduction has been considered in the data shown in Figs. 9 and 10.

For type B responses, the resistive component of the drive-point impedance was calculated as a function of frequency for ladder networks described by the appropriate Weinberg parameters. The $R\times BW$ products and F values were then determined from the response curves for various values of V and the results are shown in Fig. 6.

Use of figure-of-merit curves

The curves shown in Figs. 6 and 10 are useful in evaluating the degree of optimization of a given output-circuit design. The computed response of R as a function of frequency for the circuit is used to find pairs of F and V values. These pairs determine the location of points on the curve sheet which, in general, lie below the curve corresponding to the general shape of the response curve being evaluated. The closer the points approach this curve, the more nearly optimum the circuit design. As an example, a typical Coaxitron output circuit (such as those shown in Figs. 2 and 3) has a calculated double-humped response curve that provides a drive-point resistance at the valley of 27.2 ohms. At this resistance the bandwith measures 69.8 MHz, and the resulting $R\times BW$ becomes 1900 ohm-MHz. The calculated capacitance C for the active output region (l_5 and l_6 in Fig. 2) is 84.7 pF; therefore, the $R\times BW$ for a reference circuit is given by

$$R\times BW = 1/4\pi C$$
$$= 938 \text{ ohm-MHz}$$

The resultant figure of merit F becomes

$$F = 1900/938$$
$$= 2.02$$

The maximum R for the response curve is 33.8 ohms. Consequently, V is given by

$$V = R_{max}/R$$
$$= 1.24$$

Point A in Fig. 10 is the calculated point. The curve $n=2$ corresponds to the double-humped response. The fact that point A is essentially on the curve indicates an optimum design in this case. In general, point A tends to lie somewhat below the theoretical curves because of such factors as neglected stored energy in blocking capacitances. The figure of merit F for optimized integral output circuits is 10 to 30 times that obtained with typical external circuits designed for conventional tubes which employ the same electronic structure. The advantage of optimized integral circuits such as those used in Coaxitrons is especially important for wideband applications.

Effect of drive-point reactance

The reactance component of the drive-point impedance is also important in the performance of power amplifiers. At high levels of operation near the edges of the pass-band, the efficiency may suffer and/or voltage breakdown may become a problem. In either case, the cause of the difficulty is excessive RF voltage swing, as referred to by Green.[2] Simply stated, the RF voltage is equal to the product of the AC component of the plate current times the drive-point impedance. The impedance exceeds the required resistance by the amount of reactance (added in quadrature).

The efficiency is reduced as a result of higher DC power input because a higher DC plate voltage is needed to accommodate the excessive RF voltage. A certain minimum instantaneous plate voltage must be maintained to avoid decreasing the electron current. Current decrease as a result of space-charge effects in the grid-plate region is treated by Haeff.[8] At UHF, transit-time effects may also become important both in reducing the AC-to-DC ratio of plate current and in returning electrons to the grid.

A numerical example can be used to illustrate the reduction in efficiency to be expected in a typical case. Fig. 11 shows a portion of an amplifier plate-current pulse as a function of the time angle. The conduction angle is 180 degrees. The actual current is normalized to current density for convenience. The voltage required to support this current density is also shown, as well as portions of three typical waves of

instantaneous plate voltage for three cases having different-drive-point impedance phase angles, but the same resistance component. The DC plate voltage is adjusted in each case to just maintain the necessary support voltage. Because the same power output and DC plate current are assumed for all three cases, the efficiency is inversely proportional to the DC plate voltage.

The case of a 45° phase angle is representative of operation at the lower band edge of a single-circuit type of response, where the drive-point resistance and reactance are numerically equal. The voltage swing is thus 1.41 times that required if the reactance were absent, as illustrated by the zero-phase-angle voltage curve in Fig. 11. The efficiency in this case drops to 41.2% from the reference of 49.6%. The case of a 25° phase angle in Fig. 11 corresponds to a voltage overswing ratio of approximately 1.10 and indicates a reduction in efficiency to 47.5% from 49.6%. In this case, the reactance is only about half the resistance component of the drive-point impedance.

Voltage overswing

The voltage overswing ratios for several type B and C optimum networks are shown in Fig. 12 as a function of relative bandwidth; i.e., a value of 1.0 on the abscissa corresponds to the nominal or design bandwidth of the network. The one-element (single-circuit) reference shows the 1.41 overswing ratio at full bandwidth as expected. Many of the more "sophisticated" circuits (i.e., three-element type B) show a much greater overswing near the band edge than the single-circuit and might not be desirable for a high-power amplifier. Of the curves plotted, the one for the two-element type C network with a 0.5-dB ripple shows the least overswing at band edge. The two-element, 1-dB network is the next choice.

The behavior of the overswing ratios over the rest of the band does not conform to a simple pattern. It is conceivable that a special type of network could be optimized for minimum overswing ratio.

The data for the curves in Fig. 12 were calculated for optimum ladder networks having the Weinberg[6,7] parameters previously discussed. In the computation, a reference current of 1 ampere was assumed in the load and the successive complex voltages and currents were determined at each of several frequencies, working back toward the drive point. The drive-point impedance, phase angle, resistance, reactance, and overswing ratio were then calculated from the input voltage and current phasors.

The curves in Fig. 12 may be compared by assuming a 1.10 overswing ratio as an arbitrary limit and noting the fractional bandwidth for which each curve lies below this limit. The results of such a comparison are shown as dots on the corresponding curves of Fig. 7. Fig. 7 shows that the useful figure of merit F may be reduced if full efficiency is to be maintained over the utilized bandwidth for a power amplifier. In other words, the two-element 1-dB type C network would have to be designed for a *nominal* bandwidth of 1.27 times the utilized bandwidth in order to *operate* within 0.79 of the nominal band. The F factor accordingly drops to 1.58 (instead of the 2.0 predicted previously from Fig. 10).

This effect is more striking for the 10-element 0.5-dB case. Instead of an F value of 2.92 predicted at full utilized bandwidth, a useful value of only 1.88 results when the 1.1 overswing is applied. In fact, with such a limitation there seems to be a sort of ceiling on the useful F, regardless of how sophisticated the network may be.

Conclusions

The performance of optimized lumped-constant low-pass ladder networks designed according to modern filter theory can be used as a helpful guide in evaluating the bandpass performance of distributed-constant output networks. Bandpass output circuits for UHF power amplifiers can be designed to have power × bandwidth products approaching those for optimum filter networks. A double-humped response having a 1.15-dB ripple represents a good compromise between circuit complexity and power × bandwidth performance. An amplifier output circuit designed for a double-humped response having a 2- or 3-dB ripple provides *less* bandwidth for a given power output than if the ripple were only 1.15 dB. The drive-point impedance furnishes useful information for the design of output networks because a plot of the

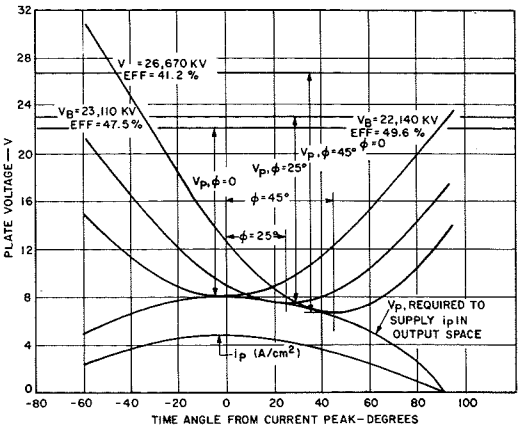


Fig. 11—Power amplifier operation with drive-point reactance; equal power outputs are assumed. The presence of reactance causes a phase shift and excessive plate swing. The attendant increase in supply voltage results in lower efficiency.

R component as a function of frequency corresponds to the power-output response. The full output efficiency of a power amplifier tends to fall off near the edge of a pass-band as a result of drive-point reactance and consequent excess RF plate voltage. Complicated (multi-element) output networks suffer more from drive-point reactance effects than the simple two-element network, which provides a double-humped bandpass response with a 1-dB ripple.

References

1. *The Development of an Experimental Model of High-Power, Broad-Band Coaxitron Amplifier* RADC-TR-60-94 (Jun 1960).
2. *The Continuation of the Development of an Experimental Model of a High-Power Broad-Band Coaxitron Amplifier* RADC-TDR-61-315 (Nov 1961).
3. Green, E., "Amplitude-Frequency Characteristics of Ladder Networks", Marconi's Wireless Telegraph Co., Ltd.
4. Parker, W. N., "Dipnet, A General Distributed Parameter Network Analysis Program", *IEEE Trans. on Microwave Theory and Techniques* Vol. MTT-17 No. 8 (Aug 1969) pp. 495-465.
5. *Reference Data for Radio Engineers* (4th Edition, International Telephone & Telegraph and Radio Corporation, 1956).
6. Weinberg, L. "Optimum Ladder Networks" *Jour. Franklin Inst.* (Jul 1957).
7. Weinberg, L., "Additional Tables for Design of Optimum Ladder Networks" *Jour. Franklin Inst.* (Aug 1957) pp. 127-138.
8. Salzberg, B., Haeff, A. V., "Effects of Space Charge in the Grid-Anode Region of Vacuum Tubes" *RCA Review* (Jan 1938) pp. 336-374.

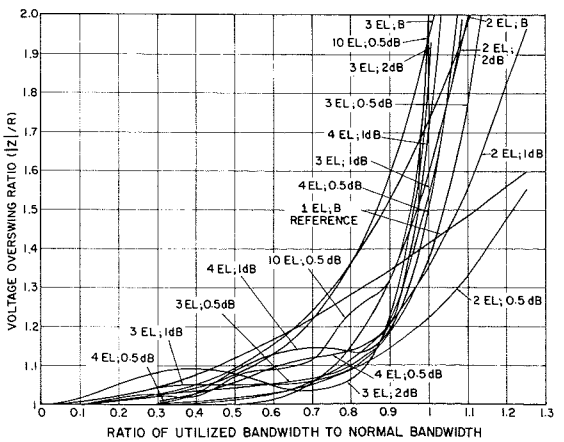


Fig. 12—Output voltage overswing vs utilized bandwidth for types B and C networks.

Stepper motors—application and selection

A. J. Bianculli

A typical common denominator of most advanced and sophisticated manufacturing equipment is a positioning system. Regardless of the positioning means employed, a part or workpiece must be brought into a predefined location envelope so that operations may be performed upon it. Since much of this type of manufacturing equipment is computer controlled, flexible positioning systems are necessary to derive all the advantages that the computer can provide. It avails us little to use a computer that can decide among alternative motions if the locating devices are unable to provide different outputs. Flexibility can be achieved via closed- or open-loop motor-driven systems, each offering distinct advantages. Stepper motors may be used in either case; however, for an open-loop system, a digital driving device such as a stepper motor must be used to maintain control.

STEPPER MOTORS convert digital pulse inputs to analog shaft output (or rotary) motions. Each shaft revolution can be expressed in terms of a number of discrete, identical steps, or increments. Each step can be triggered by a single pulse. Many devices that provide incremental rotary motion can serve as stepper motors. These include true motors, rotary solenoids, electromagnetic slip clutches, and linear-rotary actuators. True stepper motors are provided as permanent magnet or variable reluctance types.

Operating principles

Permanent magnet stepper motors

In these devices, the rotor is a cylindrical permanent magnet that is magnetized along a diameter and may have one or more pairs of poles. It rotates in a slotted stator containing windings. In operation, the rotor lines up with the stator magnetic field produced by applying DC voltages to the stator windings. By switching the polarity of the DC voltages, the stator field (and consequently, the rotor) is made to rotate.

Polarity sequencing to obtain 90° stepping is depicted in Fig. 1 and described as follows: When *S*1 is positive and *S*3 is negative a magnetic field is produced by the stator causing the rotor to line up with this field as shown in Fig. 1a. If positive is now switched from *S*1 to *S*2 and negative from *S*3 to *S*4, the magnetic field and rotor alignment shifts 90° as shown in Fig. 1b. Subsequent polarity changes (Figs. 1c and 1d) advance the stator field, and thus the rotor, through 360° in 90° steps. Table I lists the polarity sequencing format for this cycling.

Table I—Switching mode A (90° step angle)

Step position	*S*1	*S*2	*S*3	*S*4
1	+	0	−	0
2	0	+	0	−
3	−	0	+	0
4	0	−	0	+

It is also possible to obtain 90° stepping by using the resultant of two fields. This sequencing mode is shown in Table II. Since, in switching Mode B, both windings are energized at the same time, current and power input are 100% higher than in switching Mode A, but torque is only 41% higher.

Table II—Switching mode B (90° step angle)

Step position	*S*1	*S*2	*S*3	*S*4
1	+	+	−	−
2	−	+	+	−
3	−	−	+	+
4	+	−	−	+

By properly combining the two switching modes, a 45° stepping mode can be obtained, as shown in Table III.

Table III—Switching mode C (45° step angle)

Step position	*S*1	*S*2	*S*3	*S*4
1	+	0	−	0
2	+	+	−	−
3	0	+	0	−
4	−	+	+	−
5	−	0	+	0
6	−	−	+	+
7	0	−	0	+
8	+	−	−	+

Polarity switching delineated in the preceding tables is readily accomplished with mechanical switching devices but solid-state electronic switching is difficult because two polarities must be switched. To simplify electronic driving circuits, multiphase stepper motors with a center tap in each winding are generally employed.

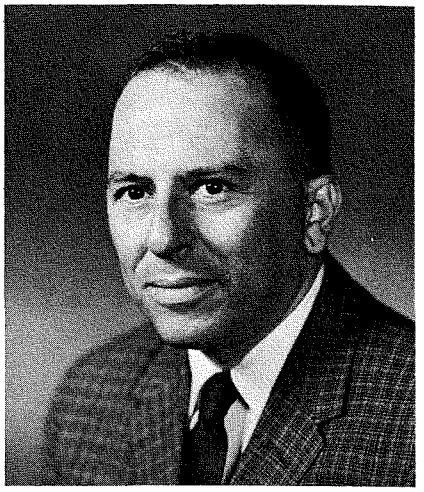
Variable reluctance stepper motors

In a variable reluctance stepper motor, stator-rotor phases are aligned on a shaft. The soft iron stators are magnetically and electrically independent and the non-magnetic rotors are all fixed to the shaft. Fig. 2 shows an arrangement consisting of three stator-rotor phases: A, B, and C.

Each stator and rotor have the same number of teeth, and all stator teeth in all phases are aligned with each other. Rotor teeth in each phase are slightly offset from teeth in adjacent phases, the amount of offset depending upon the number of phases. In the case illustrated in Fig. 2, the rotor teeth in each phase are offset by two-thirds of a tooth width. When one rotor is fully aligned with its stator, the other rotors are misaligned by two-thirds the width of a tooth, in opposite directions.

When phase A is energized, the teeth of rotor A and stator A will be aligned. Now, if phase A is de-energized and

Reprint RE-16-3-2
Final manuscript received March 10, 1970.



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phase B is energized simultaneously, the teeth of rotor B will adopt the position of minimum reluctance by moving into alignment with the teeth of stator B. In the arrangement shown in Fig. 2, the shaft will move one step in a clockwise direction each time the stators are energized, or pulsed, in the sequence A, B, C, A, · · · . Sequential pulsing A, C, B, A, · · · causes counterclockwise motion.

The index angle, or angular rotation of the shaft per step, in a variable reluctance stepper motor, is obtained by dividing 360° by the product of the number of teeth and the number of phases.

Other types of stepper "motors"

Other devices, some of which are described below, are also used for the stepper motor function. In general, they are not as fast-acting, have shorter life, are unidirectional, and are available in more limited step sizes than true stepper motors.

One stepping device employs an electrical coil mounted in a "stator" case having three inclined raceways. An "armature," capable of moving axially, has mating raceways. Steel balls separate the raceways. Activation of the coil pulls the armature toward the coil, and the applied linear force causes the armature plate to rotate because of the slope and arc of the raceways. A clutch engages the output shaft which turns and is detented at the end of the stroke. Deactivation of the coil returns the armature to the start position, ready for the next step.

A different device that consists of a solenoid coil and a spring-driven plunger is also available. Upon energization of the solenoid, the plunger is pulled into the coil against the force of the drive spring. On de-energization, the spring drives the plunger out of the coil, rotating a multi-step star-

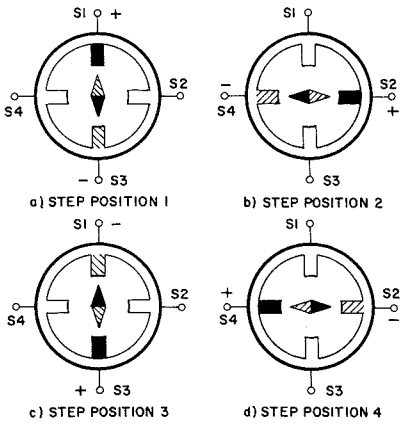


Fig. 1—Polarity-sequencing permanent-magnet stepper motor; the solid shading indicates a north pole.

wheel on the output shaft. An actuator prevents the shaft from moving any more than one step, and a stop pawl prevents movement in the opposite direction.

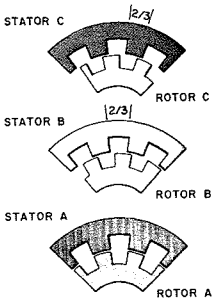
One manufacturer makes a "digital motor" with an armature that is similar to a DC motor armature except that it moves in a direction dependent upon which field coils are energized. When the armature moves, a number of pawls actuate a cylindrical starwheel having teeth on the outside and inside circumferences. The inside teeth drive the output shaft via other pawls. When the motor is de-energized the outer pawls lock the starwheel and motor shaft and the armature is spring-returned to its initial position.

Electro-hydraulic pulse motors combine a true electric stepper motor and a hydraulic torque amplifier. The electric motor drives a four-way pilot valve thus directing oil-admission to the hydraulic motor. The design provides a high-speed pulsed output at a very high torque level.

A unique way to achieve very high stepping rates with moderate to high torque outputs is accomplished by USM's Responsyn stepper motors. [Responsyn is a Trademark of the USM Corporation.] These motors employ an adaptation of the Harmonic Drive, a USM-patented power transmission system, that combines the functions of electric motor and speed reducer.

Stepper motor characteristics

As shown earlier in the discussion on permanent magnet steppers, when the rotor lines up with the stator field so that a rotor *N* pole(s) is aligned with an *S* pole(s) of the stator magnetic field, no motion occurs. Rotation of the stepper motor rotor is achieved by switching the polarities of the stator field to the next step position causing the rotor to follow. Obviously, switching of the stator magnetic field must precede rotor rotation and, in the dynamic condition, the rotor is always "behind" the stator field switching, trying to "catch up" and align itself, *N* to *S*, with the stator field. This situation is displayed graphically in Fig. 3. When the relative displacement between rotor and stator field is 0°, i.e., when *N* and *S* poles align, no torque and, subsequently, no motion occurs. As soon as an angular difference exists



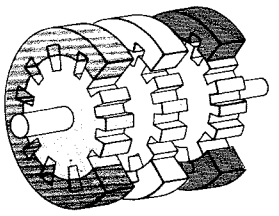


Fig. 2—Variable reluctance stepper motor. (Courtesy of Warner Electric Brake and Clutch Co.)

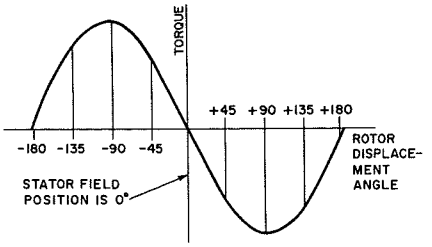


Fig. 3—Torque vs. motor displacement.

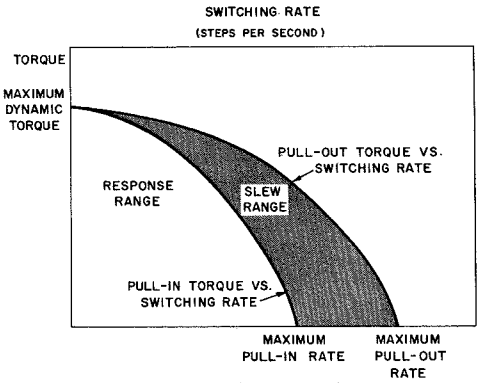


Fig. 4—Stepper-motor characteristics.

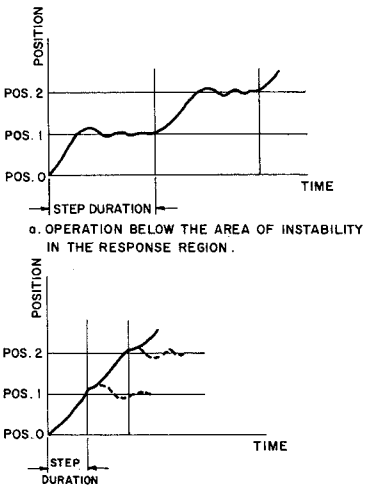


Fig. 5—Stable operation—switching rate effect.

between the two, a restoring torque is developed and rotor motion is produced. Maximum torque, called *holding torque,* is developed when the rotor and stator field positions are 90° apart.

The value of holding torque that is usually provided by the stepper motor manufacturer should be used only as

a figure of merit. The motor cannot drive a load requiring this amount of torque since this torque level is achieved at only one relative displacement position—at all other positions the developed torque is lower. A more meaningful indication of the loading capacity of the motor is the *pull-out torque,* or *running torque.* Referring to Fig. 4, pull-out torque is seen to vary with the switching rate. It is limited by inherent damping in the motor, and load inertia has little or no effect on it.

The lower curve of Fig. 4 describes the *pull-in torque.* It varies with the total inertia and is a measure of the switching rate at which a motor can start without losing steps. This curve is the upper boundary of the *response range,* or *start range.* A motor can start, stop, and reverse on command in the *response range;* in this range, therefore, a stepper motor can be successfully used as an open-loop positioning device. (A small nebulous range exists near the curve itself wherein the stepper motor can bring the load to synchronism, but not without losing some steps.)

The area between the two curves is identified as the *slew range.* The slew range is entered while the motor is running and within it the motor cannot start, stop, or reverse on command. However, the slew range is useful since the motor can run unidirectionally and follow the switching rate within a certain acceleration without losing steps while developing enough torque to overcome the load torque.

Within the response range there is a region where the stepper motor behaves erratically. Stepping occurs but with irregular step angles. Pull-out torque varies considerably and at certain switching rates can actually be lower than at higher rates. This unstable operation is caused by the combined inertia of load and rotor which cause overshoot, and an oscillatory motion, at the end of a step. Friction, eddy currents, and hysteresis dampen these step-end oscillations (Fig. 5).

Stable operation is achieved through proper selection of the physical and operational parameters of the system, viz., load inertia, damping, and switching rate. For example, if the step duration between pulses is sufficiently long, the next pulse comes after the oscillation has diminished (Fig. 5a). Operation in this mode occurs at a switching rate below the unstable region of erratic operation. Stability can also be achieved at a higher switching rate where the time duration between pulses is equal to, or shorter than, the initial period of the oscillation (Fig. 5b). In both cases, operation is within the response range.

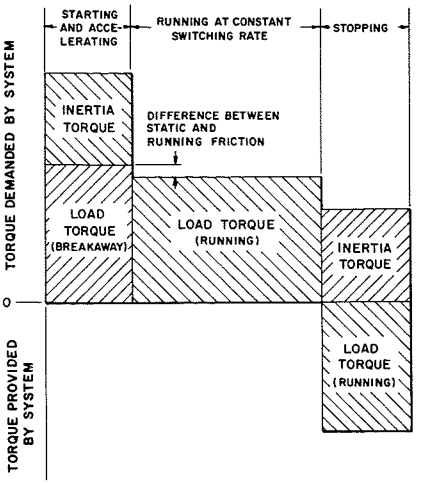


Fig. 6—System torque demands.

Stepper motor selection

To select the proper stepper motor for a given system, certain parameters of the system should be known. With this information, it is possible to make a judicious choice from the catalogs of most motor manufacturers.

The first, and most obvious, observation is that the motor must deliver sufficient torque to operate the system. The greatest torque demand on the motor is made when starting the system because, in addition to the torque required to drive the load, inertia effects must be overcome. The total torque requirement may be expressed as:

$$T_{total} = T_{load} + T_{inertia} \qquad (1)$$

This expression is presented graphically in Fig. 6, showing the torque demands of the system during the starting and acceleration stage, at constant switching rate, and for stopping. It is well to remember that the starting and stopping stage may involve only one step of the motor. The torque demand for stopping is dependent on the relative values of inertia and load torques. The load torque (friction, eddy currents, and hysteresis effects) aids the slow-down and stop process and, if it is larger than inertia torque effects, it is entirely possible to stop the motor, in synchronism, without providing a counteracting torque via an electrical input to the motor.

Ordinarily, if it is intended to operate the system "open loop," i.e., without positional feedback, the motor chosen must provide sufficient torque and stepping speed within the response range. It is only within this range that the motor can start, stop, or reverse on command "instantaneously."

The motor can be driven into the slew range by increasing the switching rate but, once in the slew range, the motor cannot be stopped or reversed instantaneously without losing synchronism. (If a deceleration schedule is preprogrammed into the motor driver, it is possible to maintain synchronism while reducing the slewing rate gradually. In this manner, the motor can be brought back to response range operation and stopped instantaneously.)

For closed-loop operation, maintenance of synchronism throughout the entire driving cycle is less important since the actual position of the system output is monitored constantly. Efficiency dictates that the system be started and driven as fast as possible, sometimes even with the probability that synchronism will be lost. Unless precautions are taken, the system output will overshoot at the end of travel because of inertial effects. A closed-loop system will automatically correct the overshoot but at the expense of time. Therefore, it may be desirable to anticipate the end of a run by keeping count of steps actually taken (or distance traveled by the output of the system) in order to provide a controlled deceleration and prevent overshoot.

As mentioned previously, the total maximum torque required of the motor is the summation of *load torque* and *inertia torque. Load torque* is defined as the torque required at the system input shaft to move the load. (The small difference between the *starting,* or *breakaway, torque* required to overcome stiction, or static friction, and the torque required to maintain dynamic operation—the *running torque*—is usually negligible.) Although the load torque may be calculated, if the system is available before the motor is selected, it is simpler (and probably more accurate) to mea-

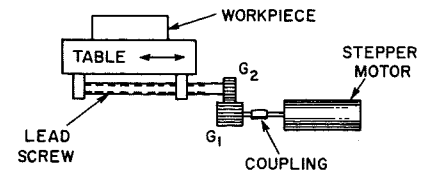


Fig. 7—A simple positioning system.

sure the starting torque by attaching a pulley to the machine shaft that will be coupled directly to the motor. A system of weights or a scale connected to the outside diameter of the pulley can be used to measure the force required at the pulley radius to move the system.

Inertia torque may be determined by calculating the load inertia as applied to the motor shaft. Using the system shown in Fig. 7 as an example, the total inertia of the system (neglecting the coupling inertia) as seen by the motor is:

$$I_{total}=I_{G1}+(I_{G2}+I_{Leadscrew})+I_{table} \quad (2)$$

The term in parenthesis $(I_{G2}+I_{Leadscrew})$ must be calculated as an inertia reflected back to the motor shaft.

Now, the moment of inertia of a solid cylinder or disk of mass (m, lb), radius (r, in), and of any axial length (L, in), about its own axis is:

$$I_{cylinder}=\frac{mr^2}{2}=\frac{\pi D^4 Ld}{32g} \quad (3)$$

where D is diameter in inches; d is density in lb/in^3; and g is acceleration due to gravity in in/s^2.

Eq. 3 is used to find the moment of inertia of gear 1 and also of the gear 2—leadscrew combination.

The inertia reflected back to the motor shaft $(I_{G2}+I_{LS})$ equals I_E, and the equivalent torque at the motor shaft (necessary to accelerate gear 2 and the leadscrew) equals T_E.

$T_E=I_E\alpha_1$, where α is angular acceleration, rad/s^2

$I_E\alpha_1=I_2\alpha_2(N_1/N_2)$, where N_1 is number of teeth, gear 1 and N_2 is number of teeth, gear 2.

$$T_E=I_2(r_1/r_2)\alpha_1(N_1/N_2)=I_2\alpha_1(N_1/N_2)^2$$
$$I_E=I_2(N_1/N_2)^2 \quad (4)$$

The last term in Eq. 2, the table (and workpiece) inertia, is determined as follows: The resistance of the table to acceleration equals the force necessary to produce acceleration. This inertia force, F, is equal to ma. Using the subscript, t, for the table (and workpiece) and the subscript, s, for the stepper motor shaft:

$$F_t=m_t a_t$$

where a is linear acceleration, in/s^2. Torque, $T_s=F_t r_1$, where F_t is force reflected to the stepper motor shaft. F_t is reduced by a factor equal to the mechanical advantage of the system, MA.

$$F_s=F_t/MA$$

where MA = (distance moved by motor shaft) / distance moved by workpiece, δ, inches.

$$T_s=\left(\frac{W}{g}\right)a_t\left(\frac{1}{MA}\right)r_s,$$

where W is the combined weight of table and workpiece in lb.

$$T_s=\frac{W}{g}\left(\frac{1}{MA}\right)^2 r_s^2\,\alpha_s, \text{ and}$$

$$I_s=\frac{W}{g}\left(\frac{1}{MA}\right)^2 r_s^2$$

Distance moved by the motor shaft is equal to angular movement in degrees,

$$\beta\left(\frac{\pi}{180}\right)r_s$$

$$I_s=\frac{W}{g}\left(\frac{\delta}{\pi\beta/180}\right)^2 \quad (5)$$

Substituting Eq. 5 in Eq. 2

$$I_{total}=I_{G1}+(I_{G2}+I_{LS})\left(\frac{N_1}{N_2}\right)^2+\frac{W}{g}\left(\frac{\delta}{\pi\beta/180}\right)^2 \quad (6)$$

and $T_{inertia}=T_{total}\,\alpha_s$

The foregoing dissertation concerning stepper motor torque requirements presumes that most of the physical parameters and design objectives of the system are known. It is worthwhile to look at just one of these data to show the dependency of the variables on each other.

Switching rate will fix the angular acceleration term, α, that must be known for calculating torque needs. The switching rate is, in turn, fixed by the motor step angle and the output speed of the system. The motor step angle affects the resolution, or output positioning of the system. All other things equal, the smaller the step angle, the more closely can the output be positioned to any predetermined point. It follows that the smaller the step angle, the longer will the output mechanism take to move from one point to another. Therefore, a choice of step angle must be a compromise between resolution and speed of the system. Knowing the motor step angle, gear ratios, and leadscrew pitch and working backwards from the desired traverse speed, the switching rate can be ascertained. In addition, there are other important factors to consider when choosing a stepper motor such as size, maximum (and minimum) ambient temperature, holding torque, and detent torque.

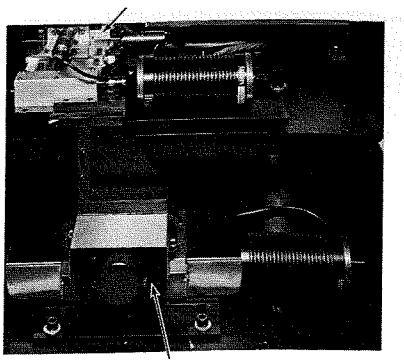


Fig. 8—Assembly machine application of stepper motor.

Stepper motor applications

Stepper motors find their widest area of application as the driving element in positioning systems, with or without feedback loops. They are used to drive the tables of N/C machine tools, x-y plotters, and drafting machines. An interesting example of the latter application is shown in Fig. 8. The upper table, which provides fine x-y positioning, is mounted on a rotating stepper-motor-driven table that can provide angular orientation. This entire set of components is arranged upon another, coarse positioning x-y table. With this system, it is possible to automatically orient a part quickly (by means of the rapid traverse gross table) and accurately (via the fine positioning stages).

Although the examples and selection criteria explained in this article are highly biased toward the application of stepper motors in coordinate positioning systems, these motors have many other distinctly different applications. For example, they are useful as elements in analog-to-digital and digital-to-analog conversion systems; as incremental drivers in tape transport or paper feed mechanisms; for variable speed spool drives; and for synchronization between master and slave elements in numerous production applications.

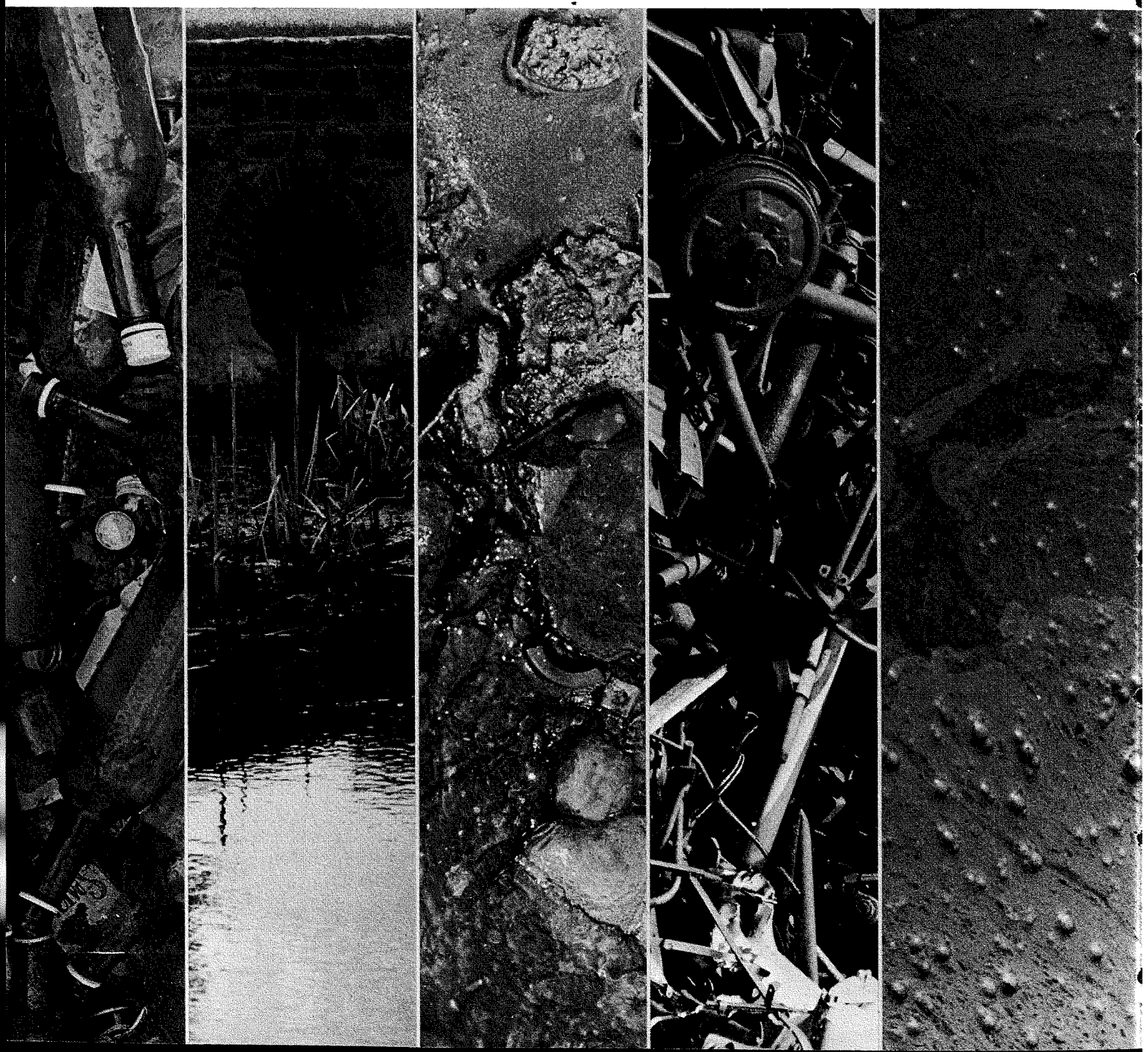
Acknowledgements

The author thanks L. Rempert for the help he provided by discussing the idiosyncrasies of stepping motors and the discrepancies displayed between theory and practice. Mr. Rempert's experience in the application of these motors was of inestimable value. S. Haas helped to illuminate many fine points of motor torque and inertia analysis, and his assistance is gratefully acknowledged.

Water, water, everywhere...

F. J. Strobl

Man has categorized much of his history in terms of evolutionary periods: the Stone Age; the Bronze Age; the Industrial Age; and the Atomic Age. And each age has represented a progressive step for mankind. But as man moves into the 70's with promises of greater technical progress, there is a gnawing feeling that all is not well. He is discovering that many of his past achievements have been accompanied by undesirable by-products. Certain drugs, at first seemingly benevolent, have drastically affected human offspring. DDT, cast in a hero's role during WW II, has had its standing reversed to that of villain. America's (and the world's) rising standard of living, fostered by the growth of industry, is generating new problems—water pollution, air pollution, and lately noise pollution. These are all environmental consequences of today's technical achievements. Perhaps the label for this era will be the "survival age," or the "age of poisons"—a title already bestowed by the late Rachel Carson.



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received the AAS in Electrical Technology from New York City Community College in 1954. In addition to taking further courses in Engineering, Mr. Strobl is pursuing the BS at the evening division of Rutgers University. His early experience included two years in the U.S. Army as an Instructor of the NIKE Missile System. From 1958 to 1960, he was a customer engineer for IBM, and from 1960 to 1963, he was a technical writer for the Bendix Corporation where he became a lead writer preparing technical manuals on the B-58 flight control system. Mr. Strobl joined the Astro-Electronics Division of RCA in 1963, where he has served as project writer for the Navy Navigation Satellite Program. Mr. Strobl's primary responsibility is Editor, *TREND* (The Research and Engineering News Digest); he is also a consulting editor with the *RCA ENGINEER*.

TODAY, water pollution articles and editorials are saturating the news media. Student and citizen groups are forming in growing numbers to pressure government and industry to take some positive action. Both Congress and the Executive branches have already recognized, although not to the same degree, that monies must be allocated to salvage our aquatic environment.

Death in the waters

In mid-October of 1969, the *New York Times* summarized a report issued by the Interior Department on the fish kills resulting from pollution in U.S. rivers, lakes, and streams:[1]

> "The number of dead fish (in 1968), set at 15,236,000 on the basis of reports from 42 states, is up 31 percent from 1967. It is the highest since 1964, when municipal sewage, industrial wastes, and other pollutants killed 18,387,000 fish. Two-thirds of the fish killed by pollution were commercial fish, while 9 percent were classified as sport fish."

City sewage was blamed "for the death of 6.9 million and industrial waste for the death of 6.3 million." The *Times* during Earth Week also published data showing the decline over the years of the number of fish caught in Lake Erie (Fig. 1).[2]

Reprint RE-16-3-5
Final manuscript received June 8, 1970.

The sewage hazard

These statistics alone are impressive as they focus on the destruction of an important natural resource. But even more ominous, is the Interior Department's warning that the dumping of sewage into lakes, rivers, and streams also poses a hazard to people. "Scientists reported last year that fish can pick up human disease germs and spread them back to humans when eaten."[3] The public is becoming aware that pollutants are not only affecting the potability of water, but may spawn new hazards. This is especially disturbing when we are presented with data informing us that "every second, day and night, about 2 million gallons of sewage and other fluid waste pour into the nation's waterways."[4]

Impact of pollution on biota

To understand what actually happens when a stream becomes polluted by sewage, it may be helpful to examine, in some detail, the way pollution affects the stream's environment and its life (or biota).

At the Robert A. Taft Sanitary Engineering Center in Cincinnati, Ohio, the U.S. Public Health Service developed a model to demonstrate the alterations on stream life by raw domestic sewage. Their report vividly describes the interaction created by pollution among physical, chemical, and biological forces:

> "With such a waste, the lowering of dissolved oxygen and formation of sludge deposits are the most commonly seen of the environmental alterations that damage aquatic biota. Fish, and the organisms they feed on, may be replaced by a dominating horde of animals such as mosquito wrigglers, blood-worms, sludge worms, rattailed maggots, and leeches. Black-colored gelatinous algae may cover the sludge and, as both rot and foul odors emerge from the water, paint on nearby houses may be discolored."[5]

Oxygen and deoxygenation

In the Center's model of the stream environment, Fig. 2, the horizontal axis represents the direction and distance of stream flow from left to right; downstream flow distance is shown in miles, and time in days. The vertical scale expresses the concentration, in parts per million, of dissolved oxygen (D.O.) and biochemical oxygen demand (B.O.D.) B.O.D. is the oxygen required by bacteria for metabolism. D.O. is used for oxidation of nitrogen and carbon compounds in sewage. B.O.D. and D.O. are inversely related, so that the dissolved oxygen concentration is low where the B.O.D. is high, and vice versa. The amount of D.O. is dependent upon the water's capacity to hold oxygen—a capacity which is affected, for example, by heat. The higher the temperature, the less oxygen it holds. For this reason, trout are not found in relatively warm water (78°F); the water just does not hold enough oxygen to support this type of fish. However, bass and sunfish are at home in this temperature. Thus, the quantity of oxygen in water is a critical factor in determining the type of biota present.

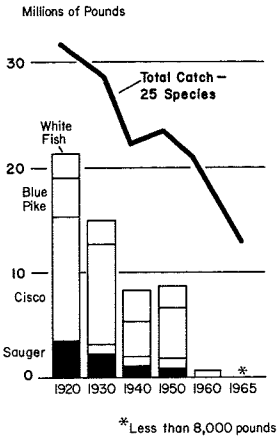

Fig. 1 Commercial fish catch in Lake Erie.

Stream environment—hypothetical case

In the diagram of Fig. 2, the hypothetical city is positioned at 0 days, 0 miles on the horizontal scale and this is the point of insertion of sewage from the community's treatment facility. Previous to this is the stream environment with a normal D.O. level.

At the input of the sewage, the D.O. drops rapidly. The organic material coming in immediately causes the available oxygen to oxidize this material; for purposes of the model, this represents one day. Then there are 3½ days in which the material is being decomposed. Next comes a period of 4 or 5 days where the stream is actually recovering and after X number of days, or X number of miles, the stream is restored. This natural restoration is

brought about by the effects of reaeration, light, and organic matter:

In the *reaeration* process, as long as the stream is moving, (i.e., it may be simply going over a rock), there occurs an exchange on the surface with oxygen, causing the D.O. to keep rising. If there were no reaeration process, full depletion of D.O. would occur at approximately 1½ days of flow at mile 18.

Sunlight is also very important and oxygen is generated by plant life (chiefly algae) through the photosynthesis process. During daylight, these plants give off a great deal of oxygen into the water—more than enough to meet the respiratory needs of other aquatic life and the needs for the satisfaction of any biochemical oxygen demand (B.O.D.). However, during the hours of darkness, the surplus D.O. is used by the aquatic life in respiration and by bacteria in the satisfaction of B.O.D.

The third action of natural stream cleansing occurs through the effect of *organic matter.* At the point in the stream where there is sewage insertion, there is an acceleration in the rate of bacterial growth. This results from the heavy concentration of nitrogen and carbon compounds from the sewage. As seen in Fig. 1, the D.O. is used for oxidation of these compounds by the feeding bacteria. With fewer and fewer of these compounds left in downstream water, the B.O.D. becomes reduced and the D.O. increases.

Life changes in the polluted stream

With a knowledge of these environmental variations, we next can look at the relationship between what happens to the water and the stream life. Fig. 3 shows the great variety of organisms in the clean water above the city. There is an association of sports fish, various minnows, caddis worms, mayflies, stone-flies, hellgrammites, and gill-breathing snails—each kind represented by a few individuals. At the point of sewage input, there is a drastic change: the number of different species is greatly reduced, and they are replaced by other types of life. There now appears a dominant animal association of rattailed maggots, sludge worms, blood worms and a few others represented by great numbers of individuals living in the sludge bed area. One of the stoutest survivors in this low-D.O. environment, the rattailed maggot or *Eristab's tenox,* uses a "snorkle" to pierce the water surface film and breathe atmospheric oxygen. The other worm-like inhabitants of the thick sludge deposits manage to stay

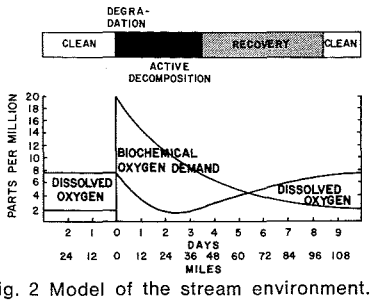

Fig. 2 Model of the stream environment.

near the surface of the sludge by wriggling upward as the solid matter settles. However, the invertebrates found in clean water do not fare so well. Their appendages may become clogged with sludge and, as solids settle, they may sink to the bottom and be buried alive. Further downstream, there again appear the more complex species which are seen to inhabit the clean water above the sewage insertion point. However, the variety of types is greatly reduced in number.

Thus given a chance, nature will cleanse a polluted stream. The model presented in this discussion assumes an input of sewage by one community, a period of degradation, a period of recovery, and finally restoration. But what happens in real life is a sewage deposition by another community *X* number of miles downstream, then by another community, etc. It is this overtaxation of the capacity of our streams to self-cleanse that is essentially the pollution story.

The disappearing species

But the striking point of this pollution story, and perhaps the most frightening, is the noticeable change in the amount and type of species. Suddenly there appears a large population, but a population characterized by a small mutant variety.

Some species disappear, never to reappear. It is very tempting to extrapolate this biological change in the stream biota to all forms of life on this planet.

In 1963, Stewart L. Udall, then Secretary of the Interior, noted that experts had estimated "that more than 200 species of birds and mammals have already disappeared from the face of the earth and that nearly 250 species in various parts of the world are now on the danger list."[6] Now, seven years later, any new estimate will certainly be higher. And what of the change in aquatic life? Secretary Udall, at that same time, made an additional observation:

"Progress is the . . . more subtle threat. Ever-reaching civilization daily destroys habitats that are essential for the survival of some species. Wildlife can thrive only when conditions favor reproduction; some creatures face eventual extinction the moment natural conditions are seriously unbalanced by man."

The Secretary's warning was directed toward man-made threats to the world of nature. It is ironic that now we are faced with man-made threats to man. Perhaps man has forgotten that he is part of the world of nature.

Distance is no guarantor of escape from the scourge of pollution. Evidence of human interference with wildlife has been encountered in far-flung corners of the world. Thor Heyerdahl, the intrepid navigator, found "plastic bottles, oily blobs, and other detritus of civilization" in the middle of the Atlantic.[7] Traces of DDT and other pesticides never used in the Arctic have been found in the tissues of polar bears.[8] How do these contaminents travel from inhabited regions to the arctic? Scientists theorize that the transmission occurs via the food chain: Pollutants dumped along the upstream banks of rivers appear at the estuaries and drift into the coastal waters. Fish inhabiting these areas ingest the pollutants and carry them to points further north. Seals feeding upon the fish, in turn, pass the pollutants on to the bears who are particularly partial to seal.

Future role of technology

The engineer and his technology have been blamed as the root cause of pollution. But the blame lies equally well with a public that demands more and more electrical power to run its appliances; a public that is searching for more powerful detergents to ensure whiter shirts and sheets; a public that would certainly object to the return of the outhouse. The pollution problem could be laid at the doorstep of the innovator, but it would rest just as easily at the portal of the manager of technology. Of course no one wants to return to the "good old days." At least not in technology, if not in philosophy.

In an address at the IEEE International Convention in New York, Dr. Hubert Heffner, Deputy Director, Of-

fice of Science and Technology, Executive Office of the President, attacked both reactionary and hippie alike for "making technology an attractive scapegoat for our present environmental ills."[9] Taking up the defense of technology, he continued: "It is not new technology that is the root of our pollution problems. It is how we use that technology." Recognizing that social and legal changes are needed and that difficult political and economic complexities are involved in the environmental problems, Dr. Heffner emphasized that their solution requires not less, but new, and more, science and technology.

Dr. Heffner noted the lack of effective instrumentation for comprehensive monitoring of the environment. "We need monitoring of the nutrient count, the bacteria count, the particle concentrations and the chemical pollutants of many of our lakes and streams." The rational approach to problem solving demands the knowledge of what is happening. In the area of electrical power, Dr. Heffner emphasized the need for cleaner energy sources. As an example, he cited the work going on in fusion energy: "The current wave of excitement and optimism among the fusion people comes from a marriage of lasers and plasmas." The gathering of solar energy by a combination of satellite technology, semiconductor solar cells, and high powered microwave techniques is another example of what, at present, seems like a radical approach to cleaner power. This proposal, submitted to the Office of Science and Technology, envisions "a satellite solar power station capable of generating 10-million kilowatts—about 2½ times the power consumed by New York City. It would involve twenty-five square miles of solar cells, conversion of their output to microwave power, and a 1.5-mile diameter dish to transmit that power to earth." Of course, Dr. Heffner conceded that the system, with an estimated overall efficiency of 10% and with system costs of about $500 per kilowatt, is far from a practical solution. But he added that "a successful exploitation of solar energy would be the least damaging to the environment. Perhaps we should not reject the suggestion without more thought."

Another problem needing the help of the electrical engineer is the increasing number of oil spills, averaging over 100 per year. Present methods of cleaning up these spills are far from adequate. Perhaps ultrasonic techniques could be used "to emulsify the oil before it reaches the shore? Probably not, but it is worth some thought."

Applying systems engineering to environmental problems

Dr. Heffner also analyzed the place of the systems engineer in combatting environmental problems. The systems engineer's training equips him to determine the best way to accomplish an overall purpose. Dr. Heffner suggested that this talent is exactly what is "needed to solve some of our most thorny environmental problems. If we visualize how we supply water and remove liquid waste from our cities, we see a startling dissymmetry. In California, for instance, water is carried for hundreds of miles in huge underground pipes from the north to the south. Branch lines serve cities along the way. Yet once that water is used, each city has one or scores of separate sewage treatment plants, each of which dumps its contents into a local stream or bay or lake. Why couldn't we construct a system which would collect waste on the same scale as we transport water? Why couldn't we treat the waste as it traverses the hundreds of miles to the sea and achieve the economies of scale which have served us so well in other industries?"

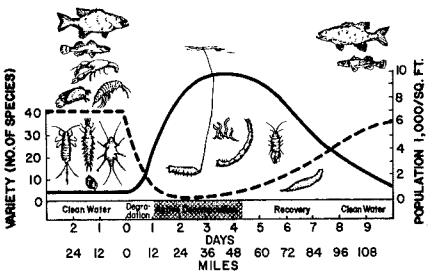

Fig. 3 Model of stream biota. The dotted curve shows the fluctuations in numbers of species; the solid, the variations in numbers.

Conclusion

Many other challenges to the engineer and scientist are apparent even to the layman. Some of these concern the transfer of electrical power, the development of new transportation systems, and the proper utilization of the earth's and sea's natural resources. In any event, several branches of technology will have to be brought together to strengthen our ability to come up with the right technical solution, at the right time—and time is a commodity that is also rapidly becoming extinct.

At this point, it might be appropriate to recall the ills that befell Coleridge's Ancient Mariner when he shot the albatross. Many believe we too have senselessly killed our albatross, and there is nothing to do but await the grim spectre. Others, however, find hope in human knowledge and determination properly applied. And it is through knowledge that the human race will hopefully avoid that fearful fate of the Ancient Mariner:

> "Water, water, everywhere, nor any drop to drink."

Acknowledgments

The idea for this article was motivated by a talk given by Richard S. Thorsell, Resource Director, Stony Brook-Millstone Watershed Association, Inc., Pennington, N.J. The address, entitled "Water Pollution—Its Nature and Effects," was presented at a Colloquium held at RCA Laboratories Princeton, N.J., on Oct. 14, 1969.

Acknowledgment is also given to Public Works Publications, Ridgewood, N.J., for permission to reproduce data and illustrations from "Stream Life and the Pollution Environment."

References

1. *New York Times,* "15 Million Fish Died of Pollution in '68, U.S. Agency Reports," Oct. 14, 1969.
2. *New York Times,* April 20, 1970, p. 33.
3. Op. Cit., *Times,* Oct. 14, 1969.
4. Op. Cit., *Times,* April 20, 1970.
5. Bartsch, A. F. and Ingram, W. M., "Stream Life and the Pollution Environment," Public Works Publications, Ridgewood, N.J.
6. Udall, S. L., *New York Times Magazine,* Sept. 15, 1963, p. 44 FF.
7. *Newsweek,* Jan. 26, 1970, p. 31.
8. *Life,* May 8, 1970, p. 86.
9. Heffner, Dr. H., "Environmental Pollution—The Engineer's Task for Tomorrow," presented at the IEEE International Convention, March 25, 1970.

Bibliography

De Bell, editor, *Environmental Handbook,* Ballantine Books, Inc., N.Y.
Graham, Jr., F. *Since Silent Spring,* Houghton Mifflin Co.
Helfrich Jr., H. W., editor, *The Environmental Crisis,* Yale University Press, New Haven and London.
Ehrlich, P. R. and Ehrlich, A. H., *Population, Resources, Environment,* W. H. Freeman and Co., San Francisco, Calif.

PN junction fabrication technology

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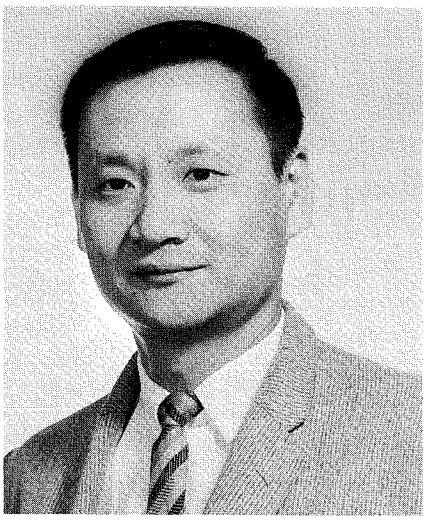
Of the numerous papers published on fabrication of semiconductor junction devices, two common criticisms can be made by practicing electronic engineers: highly sophisticated mathematics that obscure the significance of the physical concepts are often emphasized or there is a preoccupation with superfluous chemical terminology. A new approach is attempted in this paper: the current techniques and theory of PN junction technology is reviewed in terms of engineering intuition and physical concepts—not mathematics and chemistry.



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THE TECHNOLOGY OF JUNCTION FABRICATION can be currently considered under five general headings:

1) Growth junction,
2) Alloy junction,
3) Diffused junction,
4) Epitaxial growth, and
5) Ion Implantation.

This paper primarily concerns itself with each of these topics in terms of their processes, physical characteristics, and practical limitations. A typical fabrication-process flow chart for solid-state devices is also presented and discussed.

Junction formation technology

Growth junction

Basically, there are two techniques of producing the desired junction structure:

1) The doping method, and
2) The rate-growth method.

The first process makes use of the prinicple of changing the impurity doping concentration in the melt at the appropriate time during the crystal-growing cycle.[1] Assume that the crystal is grown as an N type with a specified impurity concentration from a melt. At some point in the growth process, a doping pill, containing acceptor impurities, is dropped into the melt and effectively stirred by the crystal rotation. Although the crystal is still growing, it abruptly changes to a P type, and continues to grow as a P type until the melt is further disturbed.

Reprint RE-16-3-13
Final manuscript received August 18, 1970

The second method is based on the fact that the segregation coefficients of different impurities vary with the rate of crystal growth. Segregation is the condition that most impurities are more soluble in the liquid or molten semiconductor than in the solid. Therefore, when a crystal freezes out from a melt containing a certain impurity concentration, the concentration of that impurity in the solidified crystal will be less than the concentration that originally existed in the liquid. The ratio of the concentrations in the solid to that in the liquid is called the segregation coefficient. Antimony and gallium have been used successfully as donor and acceptor impurities with germanium. In the rate-grown process, the crystal is pulled from a melt containing both impurities. At the normal pulling temperature, both *Sb* and *Ga* are segregated from the melt; however, there is a predominance of *Sb* and the crystal grows N type. When the temperature is raised, suddenly, to decrease the growth rate, the segregation of antimony drops almost to zero, whereas, that of gallium remains unchanged.

Growth junction was an extremely important technique during the earlier stage of solid-state technology. As a matter of fact, the first diode, which verified the voltage-current characteristics of PN junctions, was made by this process.

This method is limited by the geometry of the growth junction semiconductor which is in the form of a rectangular bar; the cross sectional area of the junction is restricted by the practical manufacturing limits (typical dimension is 0.012 × 0.02 inches). For high frequency applications, this junction

would be very poor, due to large junction capacitance. In the crystal pulling process, only one junction can be grown at a time, which limits the feasibility of mass production. Non-uniformity in resistivity between each little bar obtained from different parts of the grown crystal may be attributed to the non-uniform surface tension between the melt and the solid crystal during the pulling process.

Alloy junction

The PN junction is formed by alloying a suitable doping impurity material into a wafer of an opposite conductivity type. This process is carried out by placing a pellet containing the appropriate impurities in contact with the semiconductor wafer in an inert-atmosphere furnace. The wafer is carefully etched to insure uniform wetting of the molten doping pellet. When the temperature is raised high enough, the pellet dissolves and fuses or alloys into the semiconductor wafer. The depth of penetration depends on the temperature, the time, and the size of the doping pellet. The desired flatness of the penetration front or junction is insured by cleanliness and proper crystal orientation of the semiconductor wafer. When the temperature decreases again, the dissolved region recrystallizes and contains a large amount of opposite type impurities. Thus, a PN junction is formed. This method has been used with great success in diode and transistor manufacture, due to the relatively simple geometry, reasonably accurate impurity profile desirable for design, and good electrical characteristics. However, the limitation on the alloy junction is the lack of precise control over the alloying process, causing irregularities to occur at various alloying depths.

Take an alloy transistor, for example. It begins with a very thin and very lightly doped N-type crystal as the base region (⅛″ square by 0.01″ thick); two round pellets of P-type impurity are then melted against both surfaces to form a P-N-P transistor. It must be realized that the physical thickness of the base wafer is very large as compared with the practical transistor base width desired. To provide the wafer with mechanical ruggedness, the active base width of the transistor must be determined completely by the depth of the alloying process. Unfortunately, the deeper the penetration of the alloy, the less it can be controlled. Achieving a very narrow effective base width for high frequency applications by using the alloy junction method is just too difficult. This is why most alloy transistors are used only in the lower frequency range. Another disadvantage of the alloy junction is the danger of cracking during cooling at the junction area, due to a serious mismatch between the thermal expansion of semiconductor wafer and alloy metal.

Diffused junction[2]

The application of solid-state diffusion[3] results in excellent control of penetration depth and junction uniformity. To diffuse impurities into a semiconductor wafer, two methods have commonly been used. The first one is generally called "open tube diffusion", and has been used most frequently in industry. The process involves placing the semiconductor wafer in a reaction furnace and raising the furnace temperature to approximately 1000 to 1200°C, depending on materials used. The heated wafer is then exposed to a well-controlled inert-carrier-gas flow containing a heavy concentration of vaporized impurity atoms. The heat, in effect, opens the pores of the wafer, and energetic vibration of the crystal lattice allows some of the impurity atoms to penetrate and replace some of the original lattice atoms. As a result, the wafer crystal contains a large amount of impurity atoms. The profile of impurity concentration can be approximated by either the complementary error function or the Gaussian distribution from the wafer surface to the substrate, depending on the process. The depth of diffusion can be closely controlled by adjusting the furnace temperature, diffusion time, and the surface concentration. The doping level can be determined by controlling the concentration of impurity atoms in the gas stream, the gas flow rate, and the type of gas carriers used. The second method is to coat the surface of the semiconductor wafer with a layer of impurity material containing the appropriate concentration. When the wafer is subsequently heated. the impurity atoms penetrate the wafer and form a covalent bond structure with the wafer lattice.

The limitation of diffusion is attributed largely to the basic principle that junction formation by diffusion is a process of impurity compensation, not addition. For an effective diffusion process, the impurity concentration in the diffusant must be considerably greater than the opposite concentration in the material to be diffused, since the effectiveness is proportional to the concentration gradient. [Fick's first and second laws.] In practice, the maximum concentration one can get is the solid solubility limit; therefore, it is impractical to apply more than three consecutive diffusions to a silicon surface, since the impurity concentration required to compensate for the previous impurity atoms is increased exponentially. Furthermore, it is found that as the total impurity concentrations increase, mobility of both holes and electrons decrease, resulting in an increased impedance of the semiconductor. This affects the electrical characteristics of the junction. Another severe difficulty associated with the diffusion junction is that, in the case of deep diffusion, it is difficult to predict the exact junction location.

In general, the impurity concentration profile in diffusion deviates from the ideal distribution slightly, partially due to the following reasons:

1) At high impurity concentrations, the ionized space charge causes field-aided diffusion.[4] In turn, the diffusion coefficient can change by a factor of up to two.
2) During surface oxidation after diffusion, the thermal effect will cause additional impurity penetration. This is generally called redistribution. The process of redistribution is quite complex and the most accurate knowledge of this phenomenon is obtained through experiment. Results have shown it to be a function of oxidation rate, impurity segregation coefficient, and diffusion coefficient.

Epitaxial growth[5]

This method permits the growing of a single crystal film of any desired concentration (relative to the wafer), and thickness on top of any single

crystal substrate. The resulting layer will be an exact extension of the substrate structure. For silicon, two methods are widely used for epitaxial growth.

1) Vapor-phase reduction of silicon tetrachloride. This is done by the vapor decomposition of $SiCl_4$ with hydrogen at high temperature. By carefully controlling impurity concentrations(gas phase), temperature, gas flow rate, and time, one can grow a uniform epitaxial layer with any desired thickness and characteristics.
2) Vacuum deposition. The silicon atoms directly impinge onto the substrate and stick to the surface. When the temperature is raised to a certain level, silicon atoms start to be mobile and adjust themselves to match the substrate lattice structure, finally becoming part of the growing film.

Vacuum deposition can produce the epitaxial junctions as well as the vapor-phase reduction method; however, due to the vacuum environment required, it becomes less suited for mass production than the vapor-phase reduction method.

The importance of epitaxial growth in modern solid-state technology is attributed to its ease of process control, fast, uniform impurity profiles, and convenience for mass production. In addition, one of the most distinctive properties of epitaxy is that the growing film is produced by adding the impurity atoms on the existing surface, not resorting to compensation into the surface. It is this property that makes the fabrication of junctions possible without many of the compromises necessary in a diffused structure.

Again, everything is bounded by some sort of natural imperfection with no exception to epitaxy. Two phenomena have been found which prevent the concentration profile from becoming a sharp transition at the junction and prevent the fabrication of an ideal step junction:

1) The secondary diffusion during the growth of the epitaxial layer which causes the exchange of impurities between the substrate and the growing film, and
2) The autodoping due to the chemical reversibility of the deposition reaction.[6]

Evidence indicates that lower deposition temperatures can be utilized to minimize both problems.[7] Unfortunately, lower temperatures are associated with lower growth rates. For a given layer thickness, therefore, the total amount of diffusion is about the same.

Another disadvantage when using a lower temperature for deposition is that the concentration of silicon atoms in the gaseous region over the substrate becomes less homogenous or energetic, due to insufficient bouncing. As a result, the impurity distribution on the surface is not quite uniform. For a similar reason, the substrate lattice structure has less freedom, due to insufficient exciting energy; therefore, when these two are combined together, they lead to imperfect epitaxial layers.

Many different kinds of crystal structure defects can also be encountered in epitaxial growth. The most common ones are crystal dislocation and stacking faults which will be described later in this paper.

Ion implantation[12,13]

This is one of the newest techniques being used to introduce impurity atoms into the semiconductor. A stream of high energy ions is directed onto a semiconductor substrate, these ions penetrate and travel into the crystal. Through the process of successive collisions with the atoms of the bulk material lattice, the implanted ions eventually give up their kinetic energy and become located in the crystal lattice. As a result, the bulk material contains a substantial preselected amount of implanted impurity atoms. To fabricate the PN junction, one can simply implant a desired type of dopant with the specified concentration into the opposite type of bulk material.

The ion-implantation technique has recently been used in making MOS devices. This method, according to the manufacturers, exhibits less fixed-surface-state changes as compared with diffused junction, thus, improves high frequency performance. In addition, this process also allows a wide range of precise control of dopant concentration and lower device threshold voltages.

Advantages of ion implantation techniques as compared with previous methods are:

1) Doping atoms may be introduced in concentrations above that of the solubility limit for the particular impurity, and
2) The doping process may be carried out at relatively low temperatures.

Presently, there are two major drawbacks of this method:

1) It cannot be used for multiwafer batch process, and
2) There is the possibility of radiation damage to the material being doped.

Typical solid-state device fabricating process[8]

The following explanations are applied to the fabricating-process flow chart, (Fig. 1)

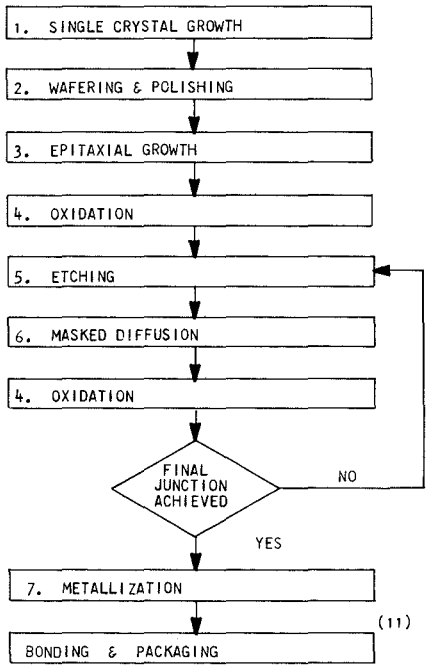

Fig. 1—Flow chart of a typical solid-state device fabricating process.

1) Crystal growth

The most commonly used method is the growth junction method, or "crystal pulling". A pure and properly oriented seed crystal is inserted in a semiconductor melt which contains a predetermined concentration of impurities. At a proper temperature, the seed is withdrawn slowly from the melt, which adheres to and solidifies on the seed, causing it to grow. This results in a properly doped semiconductor to be used as the substrate for later fabrications.

2) Wafering and polishing

The grown crystal semiconductor is then sliced into thin round wafers according to its proper crystallographic planes. One side of each wafer is lapped and polished to a very smooth mirror finish as to eliminate most surface imperfections. A final commonly used step for wafer preparation is a slow chemical etch in a $HF\text{-}HNO_3$ solution. This removes the residue surface oxide and smooths the mechanically worked region. Having a clean, polished substrate wafer is of necessary importance to reduce some of the following defects which may occur in the film growth process:

Crystal imperfections: Residual dusts and mechanical roughness on the wafer surface will deteriorate the growth of a perfect nuclear structure and cause lattice strain and dislocation.
Stacking faults: Contamination of dust particles or specks of oxide on or near the substrate surface may cause crystal orientation which differs from that of the substrate wafer. As a result, a plane of atoms in the lattice structure is missing from the normal stacking sequence and appears as triangles or semi-triangles on the layer surface or at the layer-substrate interface.
Hillocks: These may be caused by impurity particles within the substrate in addition to impurities on the surface. Hillocks appear in many forms and are frequently associated with stacking faults. A method of prevention has been reported by precleaning the substrate wafer in hydrogen at 1300°C for 40-90 min. prior to deposition.

3) Epitaxial growth

A very thin layer (2 to 25 microns) of silicon with opposite type of impurity from the wafer is grown on top of the polished surface in the epitaxial growth furnace. This step gives a high quality single crystal layer and provides a clean, perfect substrate for the deposition of other layers.

4) Oxidation

A masking material that is virtually immune to penetration by impurities at normally-used diffusion temperature is silicon dioxide.[9] Since oxidation can be achieved by placing a silicon wafer in an oxygen atmosphere for a length of time, SiO_2 has become an ideal medium for oxidation. The SiO_2 film serves two distinctive functions: first, to protect the semiconductor surface against contamination by external impurities; and second, to provide the means for masked deposition.

5) Etching[10]

To allow selective diffusion, it is necessary to etch away the SiO_2 layer in the regions where diffusion is to take place, leaving the rest of the surface protected against diffusion. This is conveniently done by means of a photolithographic process.

6) Masked diffusion

After etching, the fixed photoresist is removed, and the surface is ready for the diffusion cycle.

7) Metallization

Aluminum is generally used for metallization. A film of aluminum is evaporated over the etched regions to provide the desired pattern of interconnecting conductive strips.

Conclusions

Fabrication of PN junctions is an exercise in the art of compromise. The advantages or disadvantages of one process over another are primarily determined by the electrcial specifications and the feasibility for practical, profitable mass production.

Generally speaking, growth and alloy junction methods are restricted to devices to be used in low frequency applications. For integrated circuits, these two methods are completely impractical in fabrication processes. The PN junctions of the diffused method, however, are formed by impurity compensation. Consequently, the number of successive junctions are limited by the solubility margin and concentration of impurity. Three diffusions have been shown to be possible, but they are seldom employed in practice. The control of the bottom layer concentration profile is difficult because of the effects of subsequent diffusion operations and the requirement for a low carrier density in the bottom layer. Uniformity of impurity in multi-layered structures is not obtainable by the diffiusion method alone. For epitaxy, the newly grown impurity film is added to the existing surface. Therefore, the concentration requirement of the controlled film growth is independent of the prior surface state. The combined use of hoth epitaxy and diffusion in device fabrication has eliminated many compromises required for junction formation by either method alone, and, thereby, have been used exclusively in modern solid state devices of manufacturing. The ion-implantation technique, in which impurities are introduced into the bulk semiconductor by high energy ions and a focusing mechanism, can be carried out at relatively low or room temperature; also this process allows a greater range of dopant concentration. Devices fabricated by ion-implantation have shown lower junction capacitance and threshold voltage as compared with those prepared by diffusion methods. This suggests promises of making new types of IC devices.

Acknowledgment

I am indebted to Dr. Glen A. Richardson, Department head of Electrical Engineering, Worcester Polytechnic Institute, for his valuable suggestions and thorough criticism and to Miss Janet Reidy for the editing and preparation of the manuscript.

References

1. Teal, Sparks, and Buehler "Growth of Germanium Single Crystals Containing PN Junctions", *Physical Rev.*, Vol. 81 (1951) p. 637.
2. Handhi, G., *The Theory and Practice of Microelectronics,* (Wiley, 1968).
3. Grove, A. S., *Physics and Technology of Semiconductor Devices,* (Wiley, 1967) Chapters 1-3.
4. Lehovec, K. and Slobodskoy, A., "Diffusion of Charged Particles into a Semiconductor Under Consideration of the Built-In Field", *Solid State Electronics,* Vol. 3 (1961) p. 45.
5. Research Triangle Institute, *Integrated Silicon Device Technology—Epitaxy,* Vol. IX, Sec. 4 (1965)
6. Handhi, G., *Loc. cit.,* pp. 7-10.
7. Motorola, *Integrated Circuits Design Principles & Fabrication* (McGraw-Hill, Chapter 11; 1965).
8. Stern, L., *Fundamentals of Integrated Circuits,* (Hayden Book Co., Inc., 1968).
9. Mohr, Th. O., "Silicon & Silicon-Dioxide Processing for High-Frequency MESFET Preparation" *IBM Journal of R&D,* Vol. 14, No. 2 (Mar 1970).
10. Seitz, F., and Turnbull, D., *Solid State Physics* (Academic Press, 1964).
11. Speer, R. D., "Chip Bonding: Promises & Perils", *Electronic Design* Vol. 22 (Oct 25, 1969).
12. Brinton, J. and Curran, L., "Ion-Implantation goes to market" *Electronics,* (May 25, 1970).
13. Macdougall, J., Machester, K. and Palmer, R., "Ion-Implantation offers a bagful of benefits for MOS" *Electronics* (Jun 22, 1970).

The Mosimeter—a new instrument for measuring radiation dose

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Certain types of MOS structures can be used as sensors to provide an accurate, reliable measurement of accumulated radiation dose. This principle forms the basis for the development of a small, portable dosimeter (called a Mosimeter) that is described in detail in this paper. The Mosimeter can measure dose levels from a fraction of a rad to nearly 10^6 rads. In addition, it has the ability to obtain non-destructive readouts from remote locations by simple cable connection or to measure accumulated dose when electrical connections are impractical.

IN SPITE OF THEIR MANY ADVANTAGES, particularly their small size and low power drain, MOS transistors have only recently gained acceptance for space applications. This is because the radiation-induced shift in threshold voltage, typical of such devices, is no longer the major problem it was a few years ago. Recent improvements in processing have significantly reduced the extent of the threshold shift, and new circuit techniques now provide a high degree of tolerance to moderate variations in threshold voltage.

During extensive tests of these devices, however, it became apparent that the change in threshold voltage during irradiation of certain types of MOS transistors was sufficiently stable and repeatable to provide an accurate, reliable measure of the accumulated radiation dose. This principle allowed the development of a small, portable dosimeter using an MOS structure as the sensing element.

The MOS transistor

P-channel enhancement-mode MOS transistors appear to be particularly well suited for use as a dosimeter. A large part of the development work on dosimeter circuits was done with two readily available devices—the MEM 520, a discrete type made by General Instruments; and the P-channel transistors which form an integral part of the complementary symmetry (CMOS) circuits on the RCA CD4000 series of these devices. Fig. 1 shows an MEM 520 with its cover removed to expose the extremely small size of the silicon chip forming the active element of this transistor. Fig. 2 indicates approximate dimensions of the chip; the cross-sectional view in this figure shows the principal features of an MOS transistor.

Raising the negative voltage on the gate electrode above a certain threshold value causes a conducting channel to form between the source and drain regions. The magnitude of the current, I_D, from source to drain is generally a non-linear function of the gate voltage. The thin layer of insulation between the gate electrode and the conducting channel is made from an extremely high-resistance material, such as silicon dioxide (SiO_2). Under normal conditions, the gate input-resistance of such a transistor exceeds 10^{10} ohms.

Reprint RE-16-3-3
Final manuscript received April 20, 1970

Fig. 1—MEM 520 with cover removed.

Effect of radiation on the MOS transistor

The effect of radiation on MOS transistors has been described in detail by a number of investigators.[1,2,3] Ionization of the gate insulating material generally results in a trapped charge of positive ions, because the negative charge is dissipated by leakage of the more mobile electrons. The trapped positive charge causes a shift in the drain current versus gate voltage (I_D vs. V_G) characteristic as shown in Fig. 3. The curves, representing data taken before and after irradiation, usually maintain a nearly parallel relationship. In determining the extent of the shift, "before and after" measurements of gate voltage are usually made at relatively low values of drain current, typically 30 μA, thereby approximating the cut-off or "threshold" value of the gate voltage.

The magnitude of the radiation-induced shift in threshold voltage is strongly dependent on the voltage applied to the gate during the irradiation process. Fig. 4 shows the result of exposing different P-channel MOS transistors on various samples of the RCA CD4007D device (a dual 2-input gate plus inverter) under different bias conditions. At dose levels below about 10^4 rads, the threshold shift is nearly linear with the accumulated dose, but above 10^4 rads a saturation effect occurs.

Mosimeter circuit

The circuit shown in Fig. 5 corrects for the saturation effect and provides an essentially linear relationship be-

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tween threshold shift and radiation dose over a much greater dose range. In this circuit, the gate of the transistor is connected directly to the drain, which is supplied with an essentially constant current from a conventional bi-polar transistor. As indicated in the simplified circuit included in Fig. 5, the MOS transistor acts as a resistance which increases in magnitude with increasing dose level. The operational amplifier provides the gain needed to raise the output voltage to a level that can readily be measured by a conventional voltmeter. The potentiometer in the control circuit resets the meter to zero after each exposure, permitting the measurement of incremental doses. The total dose accumulated by the sensor element can also be determined, if necessary, by connecting a voltmeter between circuit locations A and B and measuring the total change in threshold voltage.

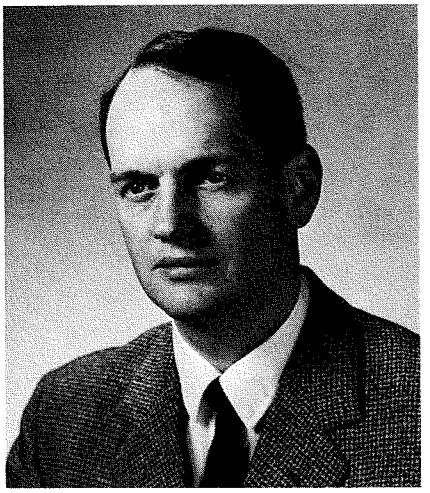
Mosimeter model

A compact, self-contained, working model of the Mosimeter is shown in Fig. 6. Two 9-volt transistor radio batteries provide an adequate source of power. The length of cable connecting the MEM 520 sensor to the control unit is not critical; lengths up to 100 feet have been used with no adverse effects. A three-position switch on the side of the enclosure changes the sensitivity of the instrument; full scale on the meter can be adjusted to 20 rads, 100 rads, or 500 rads.

Mosimeter operation and calibration

Fig. 7 shows the result of irradiating a single CD4007D P-channel transistor connected in the same manner as the sensor in the circuit of Fig. 5. The same transistor was irradiated four times, followed by an annealing procedure after each irradiation. This procedure, which included an overnight bake at 250°C, restored the transistor to nearly its original condition. The effect of radiation on the threshold voltage decreased somewhat following the first irradiation but showed almost no change between the third and fourth test runs. Also, the curves corresponding to the four runs are essentially parallel and close to being linear. The improvement in linearity in comparison with the curves in Fig. 4 is clearly apparent and is the result of the gradual increase in the magnitude of the gate bias applied during irradiation. This increase, in turn, tends to accelerate the increase in the threshold voltage, counteracting the normal saturation effect.

The behavior of the Mosimeter circuit, as illustrated by the curves in Fig. 7, provides a convenient method for calibrating one radiation source against another under a particular set of conditions. When the transistor used to obtain the data in Fig. 7 was annealed by heating and exposed to the calibrated Cobalt 60 source at Fort Monmouth, N.J., the resulting dose versus threshold-shift curve was essentially parallel to the curves obtained with the X-ray generator. The Cobalt 60



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curve and the curves of runs #3 and 4 in Fig. 7 could be made to coincide if the dose corresponding to a 10-minute exposure in the X-ray machine under the specified conditions was taken to be 10^4 rads.

An important feature of the circuit of Fig. 5 is that the dose-indicating output voltmeter can be reset to zero after each exposure. This assumes that the dose being measured is only a fraction of the total dose that the MOS transistor can absorb without reaching the limit imposed by saturation effects. For example, if the Mosimeter were used to measure a series of dose

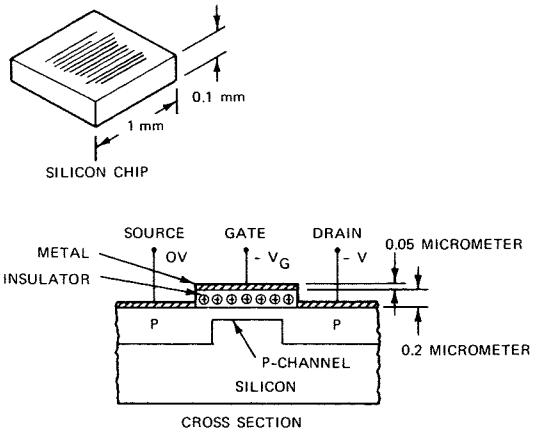

Fig. 2—P-channel MOS transistor.

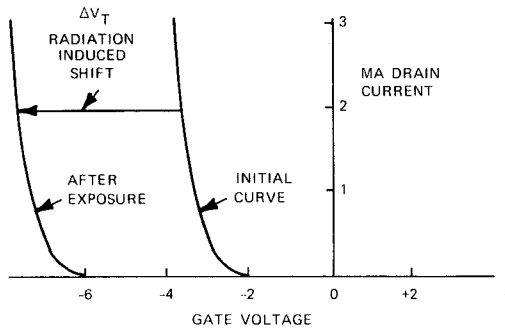

Fig. 3—Typical threshold voltage shift.

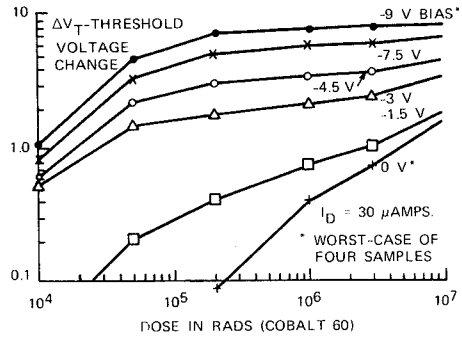

Fig. 4—Variation of threshold voltage shift with dose and gate bias during irradiation, V_I (parameters shown on these curves are V_I).

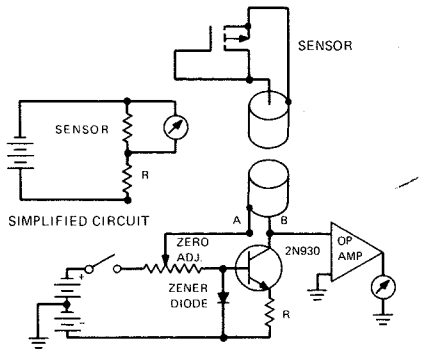

Fig. 5—Typical Mosimeter circuit.

increments of 250 rads each, then 160 successive exposures would be required to reach the 4×10^4-rad level (the upper limit of the curves in Fig. 7). The incremental change in threshold voltage of about 0.010 V for each dose increment of 250 rads would remain nearly constant because of the linear relationship between accumulated dose and threshold voltage shift. The gain of the operational amplifier under these circumstances could be adjusted to provide exactly 2.5 V at the output so that the meter would then provide a direct reading in rads.

Recent experiments have indicated that the essentially linear portion of the dose versus threshold-shift curves, as shown in Fig. 7, can be extended to at least 1.5×10^5 rads, and perhaps to even higher levels. Thus, the number of successive 250-rad exposures mentioned previously could be extended from 160 to over 600. When the MOS transistor begins to show serious non-linear response due to saturation effects, it can be subjected to a relatively simple annealing procedure that will restore the transistor to essentially its previous condition. This was done between each of the test runs and is indicated by the data in Fig. 7.

Sensitivity considerations

Ideally, the sensitivity of this type of dosimeter could be extended indefinitely by simply increasing the gain of the operational amplifier. However, a number of factors impose an upper limit on the useful gain:

1) The basic stability of the MOS transistor;
2) The sensitivity of the transistor to temperature changes;
3) The constancy of the voltage supply; and
4) The stability of the other circuit components.

When using the model shown in Fig. 6 with maximum amplifier gain (20 rads full scale), the resulting instability in the output reading was approximately 5% of full scale.

With sufficient care in designing the circuit and in selecting the components, the sensitivity of the Mosimeter can probably be increased by a factor of ten. In addition, other techniques are available for increasing the output from the sensor for a given dose level. For example, the possibility of obtaining a much greater voltage shift by using a large-scale integrated array of these devices connected in series appears to be particularly attractive. The present state of the art would presumably allow at least 100 MOS transistors on a chip not much larger than the one shown in Fig. 1.

Furthermore, when the action of the sensor element is examined in more detail, it is soon realized that the possible combination of structure and materials which can be devised for this purpose are not limited to those of an MOS transistor. Indeed, the conventional MOS transistor has a far-from-optimum structure for the measurement of radiation dose. Any insulator irradiated in a strong field can acquire a net charge. Moreover, the semiconductor provides only one convenient technique for reading out the net charge. Thus, a gain in sensitivity over the present Mosimeter model by a factor of at least 10^3 seems possible.

Potential uses of the Mosimeter

Possible applications of the sensor include most of those which Thermoluminescent Dosimeters (TLD's) were designed to satisfy. TLD's and their associated "readers" are now available from several vendors and have gained acceptance for a number of medical, industrial, and scientific purposes. Two outstanding advantages of the Mosimeter for these uses are its ability to indicate the accumulated dose level at a remote location and to perform this function non-destructively.

An application particularly well suited to the capabilities of this sensor is the measurement of accumulated radiation dose affecting satellite components in the space environment. The small size, low power drain, adaptability to conventional telemetry systems, and basic simplicity are major advantages of the Mosimeter over any other dose measuring system. Also, the range of dose levels involved in space applications are well within the capabilities of presently available MOS transistors.

Mapping the beam from an X-ray, gamma-ray, or particle accelerator is another application that fits the capabilities of the Mosimeter extremely well. Fig. 8 shows the distribution of the beam intensity close to the window of a portable X-ray generator (located at AED) as determined by a sensor element. This information is essential to the proper placement of components to be irradiated within the very

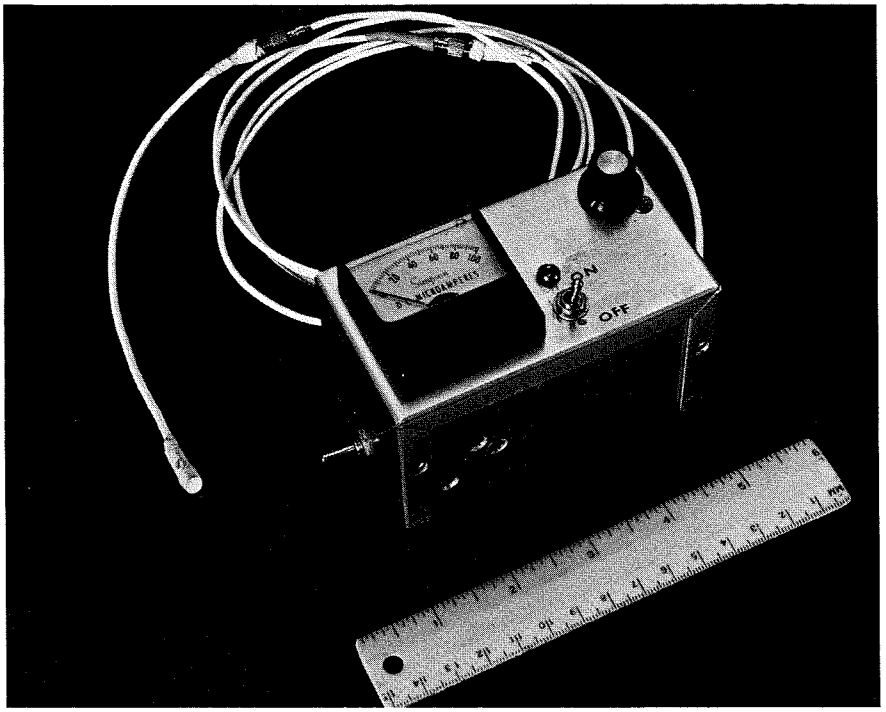

Fig. 6—Mosimeter model.

limited central region of the beam. The map of Fig. 8 resulted from successive exposures of a single sensor. The same result could be obtained more quickly by means of an array of sensors arranged in a suitable pattern over the area of the beam. Simultaneous exposure of these sensors could then be followed by sequential read-out and digital data processing to simplify the overall measuring system.

An attempt to map the beam of this X-ray generator with TLD devices demonstrated the superiority of the Mosimeter for this application. With the latter device, measurement of the dose at a particular location could generally be repeated within 1 or 2% variation. With TLD's, the variation was usually 10% or more. In addition, the time required for the complete test was considerably less when using the Mosimeter.

In situ dose measurements

Under certain circumstances it may not be feasible to provide an electrical connection between the sensor element and the control unit. Dose measurements can still be made, however, by using certain types of MOS transistors which accumulate a trapped charge even in the absence of an applied electric field. The difference in threshold voltage measured before and after irradiation provide the information needed to determine dose level. Fig. 9 shows how the threshold voltage shift of a sample of the MEM 520 device varies when irradiated without bias. Compared to the effect produced by irradiating with bias, the threshold shift is considerably less but still sufficient to cover a wide range of dose levels. Under the "no-bias" condition, the threshold shift versus dose relationship becomes non-linear at the higher dose levels. Dose or dose increments can, however, be determined from calibration curves of the type shown in Fig. 9. After one or two exposure and annealing cycles, the threshold shift versus dose relationship becomes reasonably well established. Sensors of this kind can, therefore, be used in the same manner as TLD devices to measure the accumulated dose at locations where it would be impractical to provide an electrical connection.

Conclusions

The measurement of radiation dose with a Mosimeter offers attractive possibilities for a wide range of applications. The results of recent experiments indicate that the Mosimeter has numerous advantages over competitive devices, such as small size, low power drain, basic simplicity, wide range of dose level measurements, and low cost. While the sensitivity at present is inadequate for some applications, techniques are available that can provide several orders of magnitude improvement in this respect.

References

1. Kooi, E., "Effects of Ionizing Irradiations on the Properties of Oxide-Covered Silicon Surfaces," *Philips Res. Repts.*, Vol. 20 (Oct 1965) p. 595.
2. Mitchell, J. P., "Radiation Induced Space Charge Buildup in MOS Structures," *IEEE Trans on Electron Devices*, Vol. ED-14 No. 11 (Nov 1969) p. 764.
3. Poch, W., and Holmes-Siedle, A. G., "Permanent Radiation Effects in Complementary-Symmetry MOS Integrated Circuits," *IEEE Trans on Nuclear Science*, Vol. NS-16 No. 6 (Dec 1969).

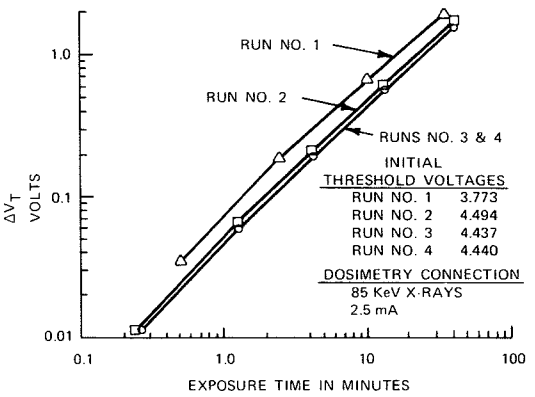

Fig. 7—Typical Mosimeter response curves.

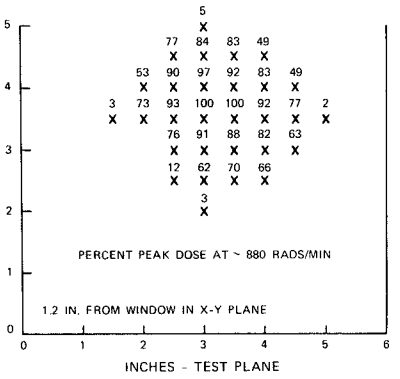

Fig. 8—Map of x-ray beam from portable x-ray generator.

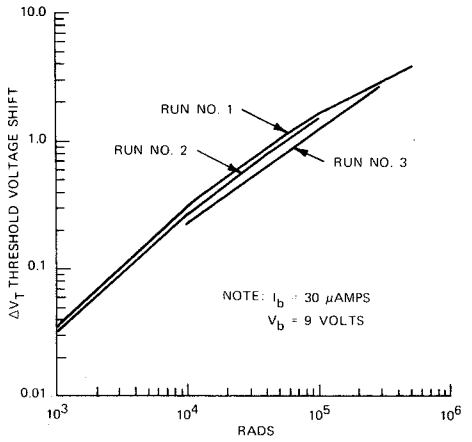

Fig. 9—Effect of irradiation with zero bias (MEM 520 sensor).

Acknowledgments

The encouragement and support from other members of the AED Radiation Effects Groups is gratefully acknowledged. In particular, recognition is due W. Borgelt, who built the original Mosimeter breadboard and feasibility model described in this paper.

The post attack command and control system—airborne data automation

Dr. E. J. Dieterich | E. H. Miller | P. T. Frawley

The Post Attack Command and Control System—Airborne Data Automation (PACCS-ADA) is an automated system for the SAC Airborne Command Post facility to demonstrate the feasibility of automating functions presently performed by the airborne battle staff. The system is built around an RCA-developed Variable Instruction Computer (VIC).[1] The most significant system integration problems were in the selection of existing data processing technology suitable for use in the airborne environment and the integration of PACCS-ADA into an existing aircraft. In the latter case, the system required compatibility with RF equipment operating over a 15 kHz to 10 GHz frequency spectrum. This paper describes the functional application of the system, the system component tradeoffs, the environmental factors, the design requirements, the demonstration and test results, and the current status of the program.

THE POST ATTACK COMMAND AND CONTROL SYSTEM—AIRBORNE DATA AUTOMATION (PACCS-ADA) is an advanced airborne data processing system which provides an operational testing facility for the storage and retrieval of command and control information. The system was developed, designed, tested, and demonstrated by RCA under contracts F1928-67-C-0263 and F1928-67-C-0362 with the USAF Electronic Systems Command, Hanscom Field, Bedford, Massachusetts. The PACCS-ADA is installed in a Strategic Air Command (SAC) EC-135C aircraft (Fig. 1) where it is undergoing a series of airborne tests and evaluations to determine the utility of data processing for airborne command post application.

At the initiation of an ADA mission, information is obtained on magnetic tape from a large data base in the ground support system. This information then becomes the initial airborne data base. During the course of the mission, the airborne battle staff queries this onboard data base by use of five alphanumeric keyboards and their associated video displays. These queries are initiated at the display terminals by typing query messages addressed to specific information in the data base.

The identity of specific data-base categories, listings, and sublistings of the entire data base contents may easily be obtained by the battle staff member. The system has the additional flexibility to generate queries tailored to the user's requirements by utilizing a set of preconceived query message formats.

The PACCS-ADA (Fig. 2) is installed in the command post compartment. The system is capable of providing the command staff with more than 1000 data query, response, update and storage transactions per hour.

Reprint RE-16-3-9
Final manuscript received May 15, 1969.

System description

The PACCS-ADA is composed of a general purpose digital computer, operation/maintenance and interface unit, five data displays with keyboards, drum for mass memory, two magnetic tape units, printer, real-time clock, typewriter, and power control unit interconnected as shown in Fig. 3. The initial data base and software are entered into the system via the magnetic tape units. The data base is buffered via the computer into the mass memory where it is available for quick access. Data updating messages are entered manually via the data-display keyboards. Hard copy of displayed data may be obtained from the printer. The typewriter is used for system maintenance. The real-time clock is interrogated under program control to label transactions with the time of day.

Compatibility

The most significant USAF requirement for the PACCS-ADA was that it be compatible with the IBM-7090 instructions generated by the JOVIAL J-2 compiler used in the Command and Control complex at the SAC Headquarters in Omaha, Nebraska. Such compatibility enables the SAC programmers to generate all of the functional software for PACCS-ADA on the 7090 using JOVIAL. The advantages of this approach include using the existing training and experience of the SAC programmers, the availability of an existing compiler and ground-support computer, and the ability to prepare and debug software for PACCS-ADA while the system was being developed.

In 1965, RCA was funded by the USAF to develop the variable Instruction Computer (VIC)[1]. This aerospace computer affords the unique capability for the user to install into its control memory those microprogrammed control algorithms which enable it to be compatible with another computer. In the PACCS-ADA program, the computer is the IBM-7090[2]. The extent of this compatibility with the IBM-7090 includes some 65 instructions (which include add, subtract, multiply and divide for both fixed and floating-point numbers) which are found in the object programs compiled on the 7090 for the 7090 using the JOVIAL J-2 compiler. After compilation, the object programs are debugged, the source statements are corrected and the compiler is rerun to produce VIC object code.

This compatibility provides the user with assurance that the message formats, display formats, memory maps, mass-memory data organization, magnetic tape formats, printer output formats, and typewriter formats are the same in both the airborne and ground-based support systems, thus easing the training and indoctrination required before using the airborne system.

System operation

The operation of the PACCS-ADA system is best described by reference to Fig. 4. The source for both the programs and data base in the airborne command post is the ground-support system. Programs are compiled on the IBM-7090 and recorded on magnetic tape by the 729-IV tape station. The data base is extracted from the ground-based mass memory and is also

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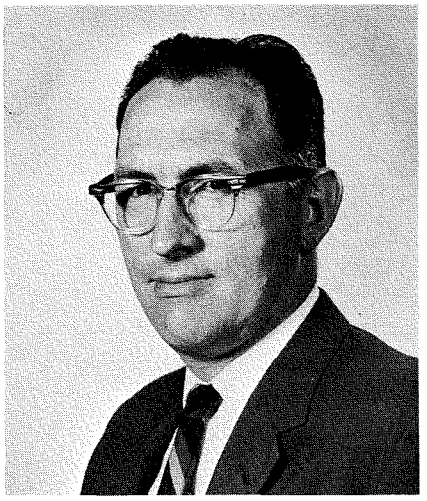

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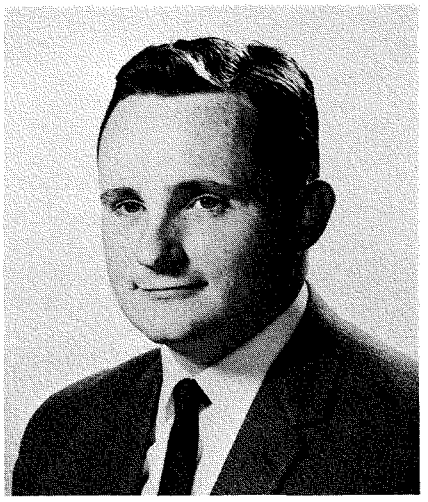
received the BSEE in 1952 through the cooperative program of the University of Cincinnati, and has completed numerous graduate level courses at the Universities of Pennsylvania, California, and Northeastern. He joined RCA in 1947 as a cooperative student working in advanced development. As a Development Engineer, Mr. Miller worked on electro-static storage devices for automatic-track-while-scan systems, and the application of semiconductors to digital computers, telephone multiplex equipment, and ground support equipment. He was Project Engineer on a classified highspeed digital data communication system. Mr. Miller was Leader of the design and development of the Display Information Processor for BMEWS. He also had responsibility for BMEWS data processing equipment at NORAD and SAC installations. Mr. Miller later had project management responsibility for the RCA 604 High Speed Arithmetic and Control Unit. Mr. Miller was also responsible for application studies of the PACCS-ADA System. Mr. Miller is currently responsible for conceptual studies of command and control requirements in strategic, tactical and space applications. Mr. Miller is a member of IEEE, ACM and is a Registered Engineer in the State of Ohio. He has written several papers on computers and reliability of command and control applications.



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recorded on magnetic tape. These tapes are then carried to the aircraft and mounted on the airborne magnetic-tape units. This tape transfer requires complete compatibility between the ground and airborne tape units. This includes reel configuration, tape size, recording configuration, bit density, track configuration, inter-record gaps and control marks. In addition, tape interchangeability is bi-directional so that data logs from the airborne system can be processed by the grounded-based support system.

Operation of the airborne system is initiated by transferring the executive program from magnetic tape into the VIC core memory by manual initiation. Thereafter the transfer of software and data base information into mass memory under control of the executive program is automatic. The VIC main memory buffers the tape-data transfer rate to the data-transfer rate of the mass memory. It takes 5 to 10 minutes to transfer the full mass-memory load of 100 million bits of information, depending on data block size on the tape and in the mass memory.

The peripheral equipment used in PACCS-ADA varies in quantity, capacity, data code, data format, and data rate as indicated in Table I. To interface this set of peripheral equipment it was possible to utilize the flexibility of the VIC input/output traffic control in combination with the input/output micro-control capability to minimize the amount of hardware required. As shown in Fig. 5, the interface functions performed by hardware are

1) The character-to-word assembly and word-to-character disassembly shift register buffers and their associated counter;
2) The parity generator and checker;
3) The display, mass memory, and tape selection logic, and
4) The Hollerith-to-Baudot and Baudot-to-Hollerith code conversion.

The controls shown in Fig. 5 refer to the manual switches and indicators built into the operation/maintenance and interface unit. The I/O (input/output) traffic control is built into the VIC where it is part of the interrupt matrix as shown in Table II.

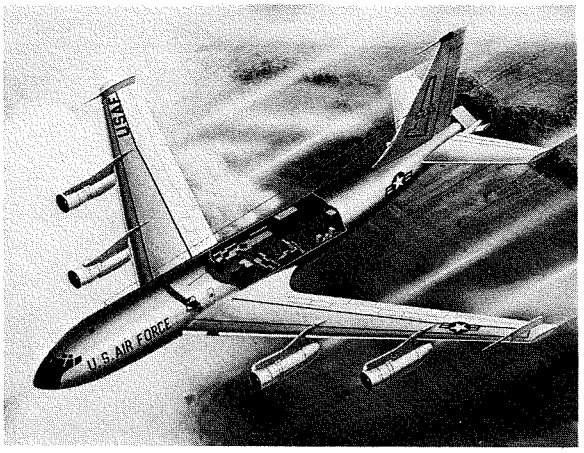

Fig. 1—Airborne Command Post aircraft.

The VIC interrupt matrix consists of four program channels and four interrupt levels (the highest priority interrupt level is labelled: CHARACTER). The high-speed, real-time peripheral devices are assigned to the highest priority interrupt level and serviced at the end of any string of three micro-control operations in the VIC. Since such an interrupt involves no VIC arithmetic unit action it may interrupt the execution of an instruction. All of the other peripheral unit I/O interrupts can occur at the end of the instruction word, and these may call for an I/O instruction or a high-priority subroutine block such as that required by the overflow of the real-time-clock interval counter. The user programs are assigned to the program interrupt level under control of the executive program.

The variable instruction micro-control technique was exploited to provide a set of I/O macro-instructions which matched the inherent VIC I/O capability to the set of peripheral equipment available for use in the airborne environment. Table III lists the peripheral equipment and shows whether their control functions were implemented by subroutine, macro-instruction, or hardware. Each macro-control function was implemented by a series of one or more variable control words. The flexibility of this feature enabled RCA to integrate the PACCS-ADA in a minimum of time.

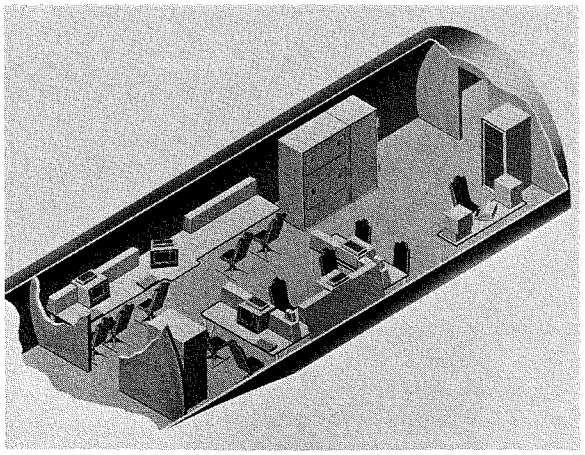

Fig. 2—PACCS-ADA concept.

Equipment selection

One of the chief objectives in the PACCS-ADA program was to implement a compatible, airworthy system with a minimum of research and development. This required a thorough search for, and evaluation of available equipment. The following is an item-by-item discussion of the equipment selected and a summary of the trade-offs that led to its selection. Table IV is a listing of the PACCS-ADA equipment with its respective size, volume, weight, power and predicted mean-time-before-failure.

Computer

As described above, the RCA Variable Instruction Computer (VIC) provides unique variable instruction features which enable it to meet the requirements for compatibility with the IBM-7090. In addition, it was designed for the aerospace environment with a large percentage of integrated circuits and modular expandability. Fig. 6 is a photograph of VIC, with the central-processor unit in the foreground and one main-memory unit in the background with two 4,096-word memory modules. For PACCS-ADA, the main-memory capacity was expanded to 32,768 words by adding two 4,096-word memory modules to the memory unit shown in Fig. 6 and by adding another 16,384-word memory unit. In addition, the high-speed memory was converted from a redundant configuration so as to provide the full 512-word variable capacity, and some other minor modifications were made to the central processor to optomize the utilization of the control memory to achieve the functions required.

The VIC is installed in the lower portion of the computer equipment rack. The upper portion of that rack is illustrated in Fig. 7. Directly above the VIC computer is the VIC operation and maintenance panel which enables the PACCS-ADA operator to monitor and control the operation of VIC by means of a mode control, a function selector, octal input switches, octal output indicators, discrete control switches, and indicator lamps. Directly above the VIC operation and mainte-

Table I—Peripheral equipment.

Unit	*Maximum quantity*	*Capacity*	*Code*	*Format*	*Rate*
Mass memory	1	10^8 bits	N/A	character serial	144 k C/sec
Data display	5	54 columns 20 lines	unsortable Hollerith	character serial	70 k C/sec
Magnetic tape	4	2400 ft. 200 or 556 char/in.	decimal or binary	character serial	41.7 k C/sec
Teleprinter	1	72 columns	Baudot	bit serial	300 ops/sec
Teletypewriter	1	72 columns	Baudot	bit serial	10 ops/sec
Real-time clock	1	24 hrs. timing	BCD N/A	20 bits pulse stream pulse stream	program 100 pps 1 pps

Table II—VIC interrupt matrix.

Interrupt level	*Program channel* 0	1	2	3	*Interrupt point*
Character	high speed mass memory, data display, tape				end of variable, no arithmetic unit action
Word	real-time clock (100 pps)	printer	typewriter	real-time clock (1 pps)	end of an instruction
Block	real-time clock interval counter			end of transfer	
Program					end of a program

nance panel is the ADA unit status panel, which enables the operator to monitor and control the operation of the PACCS-ADA. This is accomplished by indicator lamps and discrete control switches. In addition, there is a system elapsed-time indicator and the real-time clock which displays up to 24 hours in hours, minutes, and seconds.

Real-time clock

The A. W. Haydon real-time clock for ADA was selected on the basis of performance, physical size, environmental qualifications, and availability. The unit selected was already in use in the airborne environment, and it possessed the features required in PACCS-ADA. This included a 20-bit BCD time-of-day output register and 100, 10, and 1 pulse-per-second output signals—all of which are controlled by a precision crystal oscillator. The initial time is set by a set of thumb-wheel switches and a discrete start pulse.

Data display/keyboard

The principal man/machine interface unit is the RCA data display/keyboard shown in Fig. 8. This unit displays 20 lines of 54 characters each on a 12.5-inch rectangular cathode-ray tube. It includes its own magnetostrictive delay line which refreshes the 1080 characters at a 60 Hz rate. The 64 available characters include 10 decimal digits, 26 capital letters, and other special symbols. One of the chief factors in the selection of the display was the legibility of the characters. A trade-off study was conducted between dot-matrix, discrete-line-segment, shaped-beam, and monoscope-symbol generators. It showed that the monoscope-symbol generator, using a small TV-type scanning raster, produced the most legible characters at a reasonable refresh rate. The keyboard has a typewriter-like keyboard plus a set of nine controls.

1) WRITE HOME to disconnect the display from the computer to permit query message composition or editing;
2) PRINT to obtain a hard copy of the data displayed;
3) XMIT to transmit query messages to the computer;
4) CHAR ERASE to erase the character directly above the underscore cursor;
5) LINE ERASE to erase that portion of the line directly above and to the right of the underscore cursor;
6) SCREEN ERASE to erase the entire screen;
7) CURSOR LEFT to move the underscore cursor one or more spaces to the left;
8) CURSOR RIGHT to move the underscore cursor one or more spaces to the right;
9) CURSOR RETURN to return the underscore cursor to the beginning of the next one or more lines.

The keyboard is a separate unit from the display to enable either of two battle staff members to use the keyboard while they share a display. To prevent accidental erasure, the ERASE ENABLE button must be depressed simultaneously with the ERASE selector control.

Mass memory

The largest piece of equipment in PACCS-ADA is the 100-million-bit General Instrument—Magnehead Division mass memory shown in Fig. 9. Behind each of the horizontal doors is a magnetic storage drum, 18 inches in

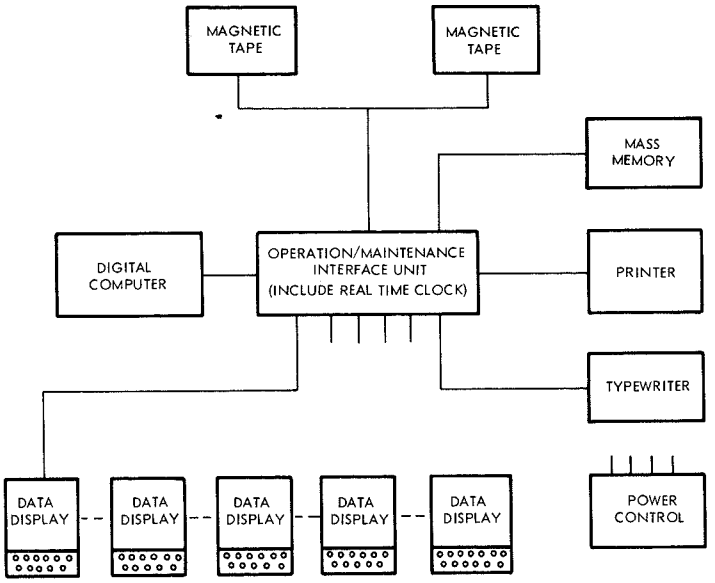

Fig. 3—PACCS-ADA system configuration.

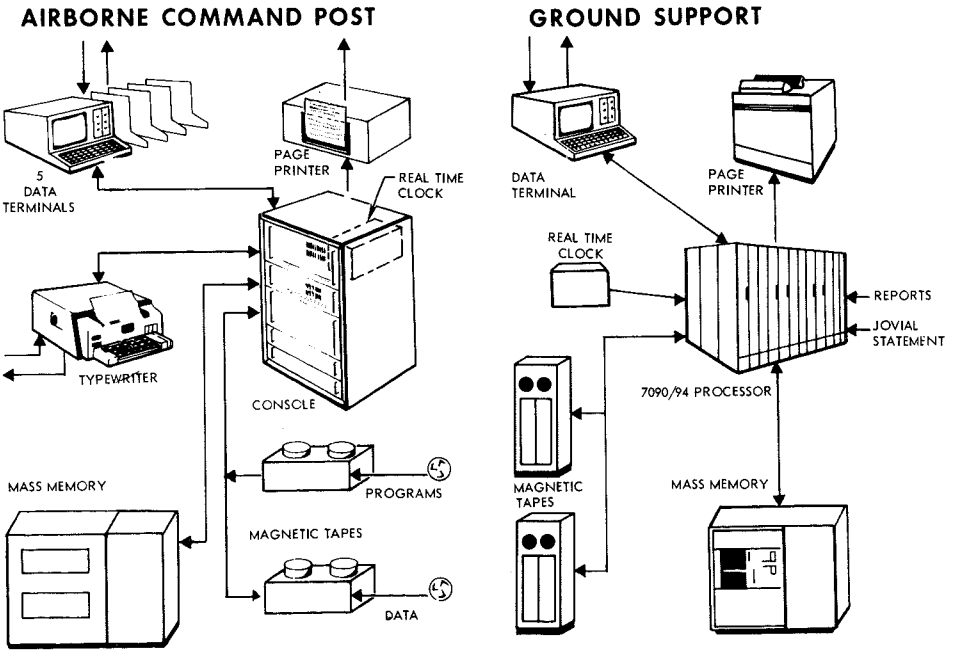

Fig. 4—PACCS-ADA system operation.

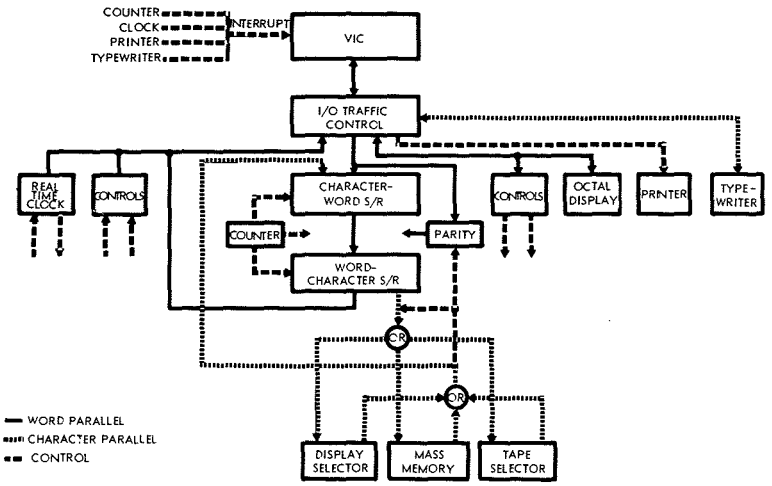

Fig. 5—PACCS-ADA peripheral interface.

diameter and 19 inches long. Each drum has 928 data tracks plus spares and provides 27.5 mS average access time to any storage record. Each track has its own air-floated head designed to rest on the drum surface when the drum stops. The base drum is magnesium, plated with a nickel-cobalt recording surface and protected by a rhodium finish. Behind the vertical door is a set of operation and maintenance switches and the control electronics. The mass-memory devices considered for PACCS-ADA included drums, discs, cores, plated wire, woven wire, etched permalloy film, thin film, and other advanced mass memory devices. Cost or state of development narrowed the choice down to drums or discs. Between these two devices, the choice was made on the basis of reliability and access time. There was concern with the problem of head crashes and reliability of the head position controls with the one-head-per-100-track disc device. In addition, the 250 to 300 millisecond access time, being 10 times as great as that for a drum, would have had an appreciable effect on system throughput, as will be discussed later in the paper.

Magnetic tape

Perhaps one of the most sophisticated electromechanical devices in the PACCS-ADA is the Ampex magnetic tape station shown in Fig. 10. The 729-IV compatibility discussed above requires the following features:

1) 10.5-inch reel with write lock-out hub;
2) Capacity for 2400 feet of ¾ inch ½ mil mylar tape;
3) Density of 200 or 556 characters to the inch;
4) 7-track width;
5) 75 in./sec. linear velocity;
6) Stop and start with a ¾-inch interrecord gap;
7) Same beginning of tape (BOT) and end of tape (EOT) marks;
8) Same longitudinal and transverse parity checks.

The tape units with these features, available for use in the airborne environment, fell into two basic types: 1) the bat-wing, mechnical servo take-up loop, and 2) the vacuum take-up loop. Between the two methods, the second was being used almost exclusively in ground-based data-processing systems; however, its use in the airborne environment had to overcome the altitude effect on the vacuum operation. The advantages of the vacuum take-up loop are faster mechanical action, low tape-loop inertia, and gentle tape handling. Fortunately, a vacuum takeup loop unit was developed in time for PACCS-ADA, and it became qualified for use in the airborne environment.

It is unique in that area is conserved by placing the vacuum chambers beneath the tape reels and changing the elevation of the tape between reel and head. In addition, all of the guide rollers work on the back or non-oxide coating side of the tape except for one guide just before the head, thus increasing the life of the oxide coating.

Printer

Another unique development which came along just in time for ADA is the National Cash Register printer shown in Fig. 11. In printers for the airborne environment there are ink-impact, photo-sensitive, electro-sensitive, and thermal-sensitive types of paper. The ink-impact device usually requires a solenoid hammer drive which requires considerable power and produces appreciable audible noise and electromagnetic interference. In the second type of printer, a photo-sensitive paper is contact-exposed to a CRT image. Its basic problem is one of a low contrast image which fades within a few hours of exposure. When electro-sensitive paper is used, it is marked by an electric discharge from a 7-finger brush, through the paper, to a metal roller. The basic problems with this type of printer are EMI and an obnoxious odor. The thermal-sensitive technique uses a 5×5 dot matrix of glass encased semiconductors which, when driven by a low voltage signal, heats the paper in contact with the matrix to produce the desired character. The resulting image has good contrast, reasonable legibility, and good life. The equipment which produces it uses low-level signals and meets the EMI requirements. The printer selected operates as a teleprinter with characters coming to it serially at a rate of 300 per second. There are 72 columns available across the 9.5 inch wide paper.

Teletypewriter

The Mite teletypewriter selected for PACCS-ADA is illustrated in Fig. 12. These units are qualified to MIL-E-5400, class I, and are common in the USAF inventory. They operate at 10 characters per second, and print 40 different characters or symbols in 72 columns.

Environment

The environmental requirements for PACCS-ADA generally follow MIL-E-5400, class I, as shown in Table V. It will be noted that the temperature and altitude requirements are not as stringent, since the equipment is installed within the manned command-post compartment which is airconditioned and pressurized to an altitude of 5 to 8 thousand feet. The vibration spectrum extends beyond the 500 Hz of MIL-E-5400 to 1,000 Hz as required by multi-engine jet aircraft. The crash safety requirements have been defined in accordance with the forces antici-

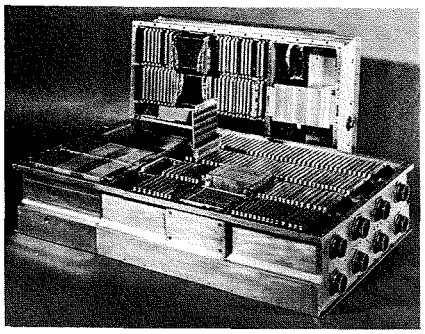

Fig. 6—RCA variable instruction computer.

pated in a forward (F), downward (D), and side-to-side or aft (S/S A) direction, depending on how the equipment is installed in the aircraft. The speech interference level (SIL) goal of 64 dB is dependent upon the interior of the aircraft cabin and the ambient noise environment.

Electromagnetic interference is probably the most critical environmental requirement for PACCS-ADA. EMI control program was initiated to provide the highest probability of meeting the EMI requirements shown in Table V. Each vendor of peripheral equipment was required to demonstrate or furnish data that his equipment was tested over the frequency spectrum indicated.

The roll, pitch and yaw requirements were invoked primarily on the electromechanical devices. In particular, there was some concern as to whether the large drum in the mass memory would be affected by gyroscopic effects due to aircraft motion. The complete mass memory passed the operating roll, pitch, and yaw motion tests without problems. Prior analysis had indicated that, with the 2½-inch-diameter class-9 bearings used for the drums, and the crash safety requirements on the cabinet, there are wide safety margins which assure proper operation.

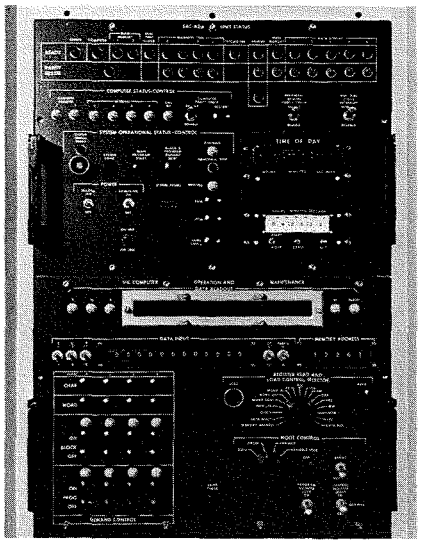

Fig. 7—Computer equipment rack.

The explosion proofing requirements were invoked because of the JP-4 jet fuel used in the EC-135. This fuel has a very high flash point and requires a hot spot of 850°C to ignite. There are no such exposed hot spots in the PACCS-ADA and all switch contact points are enclosed.

System throughput

The most tangible measure of system throughput in an information storage and retrieval system such as PACCS-ADA is the reaction time to a data base query message. RCA performed an analysis of a typical command and control problem, and showed that the primary factor affecting the reaction time of the system is the transfers between the mass memory and the high-speed core memory of the computer. Access to the magnetic tape unit is not normally required for on-line operation; therefore, these transfer speeds do not affect overall system throughput. Transfers to the displays at a rate of 70,000 characters per second,

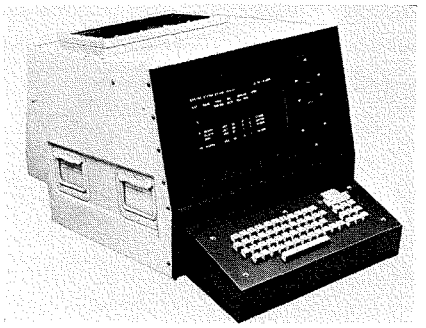

Fig. 8—RCA display/keyboard.

require about 0.0143 second per 1,000 character display and are therefore negligible.

In this analysis, system throughput is defined as the time required from the moment a command-post operator requests a display to the time the display is presented to him on the face of the cathode-ray tube. This throughput time involves the access of the operational software, the data base from the mass memory, the iteration of the data base, and the processing of the data base required to produce the desired display. This processing is best described by consulting Fig. 13, which shows the actual steps required in determining the time it takes for a data processing system to generate a display. In each case, the range of values which are feasible in PACCS-ADA is indicated in the boxes. For example, the average record size, H, may range from 500 words to 8,000 words depending on the user's programming approach and his organization of the data base. The number of records, I, may range from 1 to 60, again depending on how the data base is organized. Assuming a 5,000 word executive, the K cannot be greater than 27,000 words, the capacity remaining in the 32,000 word main memory of the computer after 5,000

Table III—VIC peripheral function control.

Unit	*Subroutine*	*Macros*	*Hardware*
Mass memory		WRITE: DRUM, BLOCK MODE, BULK MODE, ERASE READ: DRUM, BLOCK, BULK, ERROR CONDITION TRANSFER: ON READY, ON PARITY ERROR, I/O BUSY	parity generation and check
Data display	data display to printer or typewriter	WRITE DISPLAY, JAMB DISPLAY, ACKNOWLEDGE, NEGATIVE ACKNOWLEDGE STORE PRINT/TRANSMIT REGISTER TRANSFER: ON READY, ON PARITY ERROR, I/O BUSY, RESET PRINT, RESET TRANSMIT	parity generation and check
Magnetic tapes	backspace *n* files skip *n* files tape to mass memory	WRITE: TAPE DECIMAL, TAPE BINARY, EOF READ: TAPE DECIMAL, TAPE BINARY, ERROR INDICATORS TRANSFER: ON READY, ON PARITY ERROR, EOF, I/O BUSY, BOT, EOT REWIND, SKIP A RECORD, BACKSPACE ONE RECORD, STORE CHANNEL ADDRESS	parity generation timing control
Printer	print in data-display format	PRINT, TRANSFER: ON READY, I/O BUSY	code conversion
Typewriter		WRITE, READ, DE-SELECT, STORE CHANNEL ADDRESS TRANSFER: ON READY, I/O BUSY	code conversion
Real-time clock		READ, START INTERVAL TIMER: 1 PPS, 100 PPS HALT, INTERVAL TIMER: SET 100 PPS, HALT 100 PPS	

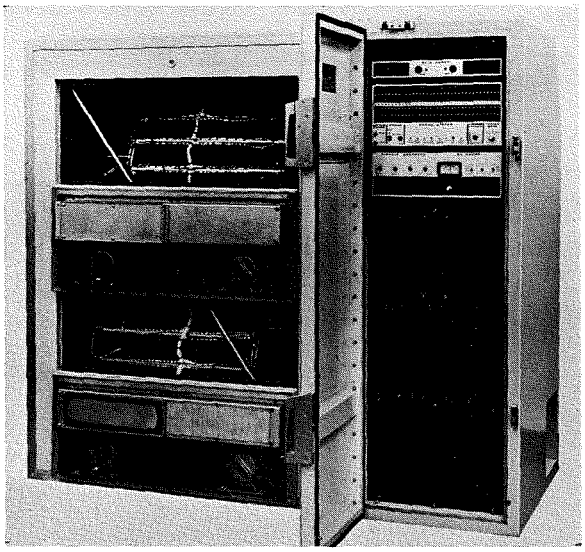

Fig. 9—Mass memory unit.

Fig. 10—Ampex tape station.

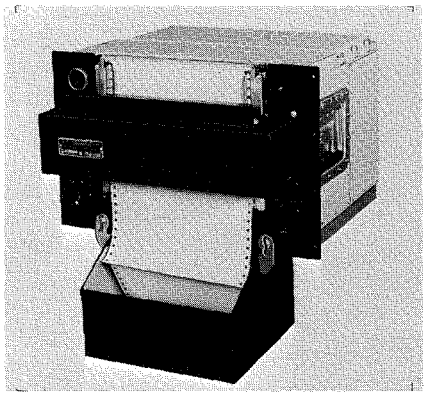

Fig. 11—NCR printer.

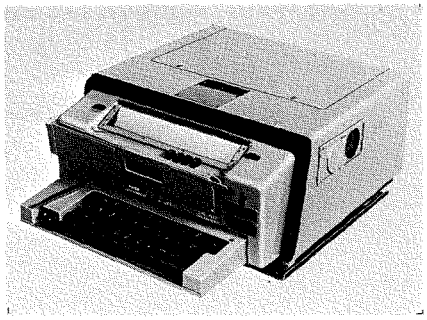

Fig. 12—Mite teletypewriter.

Table IV—Equipment characteristics.

Unit	*Qty.*	*Overall size (h×w×d–in.)*	*Volume (cu. ft) Unit*	*Total*	*Volume (lbs) Unit*	*Total*	*Power 115V, 400 Hz (Watts)*	*MTBF (hrs)*
RCA VIC-Central processor	1	6×17.3×29	1.6		95		300 avg	213
RCA VIC-16k Main memory	2	5×16.5×23	1.1		85		360 avg (180 each)	380
RCA Operator's unit	1	14×17×24	3.3		40		165 avg	1340
Haydon real-time clock 36026	1	(installed within operator's unit)			14		21 avg	2600
RCA Maintenance unit	1	14×17×24	3.3		40		165 avg	1340
RCA Rack for above 5 items	1	66×24×35		31.6*		889*	—	—
Ampex ATM-13 magnetic tape	2	13×15×28	3.2		150		1800 avg (900 each)	700
Ampex magnetic tape power supply	2	9×15×26	2.0		80		incl. above	in above
RCA Magnetic tape coupler	1	7×24×12	1.2		15		50 avg	—
RCA Rack for above 3 items	1	66×24×35		31.6*		1090*	—	—
Mite AN/TGC-14A typewriter	1	9.3×17×19		1.7		41	70 avg (200 heater)	400 4036
NCR Page printer	1	10.7×17.3×17.4		1.9		75	400 avg	532
GI-Magnehead mass memory	1	71×62×36		92		1415	6000 start (1000 avg)	
RCA Video-data display	5	22×22×20	5.6	28	126	630	1500 avg (300 each)	1218
RCA data-display keyboard	5	6.7×18×10	0.7	3.5	15	75	in above	in above
Non-interruptible power supplies	5	29×30×19	10		300		2250 avg (450 each)	
Total			*200.3*		*4590*		*8.1 kw avg*	*43*

*These figures include all units listed above.

words have been allocated to the executive. This figure then represents the maximum total number of words transferred from the mass memory to the main memory. The number of records and the mass memory access time I which may range from 10 to 300 ms, depending on the mass memory selected, yields the total access time, A, in seconds. The total number of words transferred times the word transfer time, L (which again might range from 10 to 100 μs, depending on the type of mass memory) yields the total time to transfer the data base and the operational software, identified as B seconds. The A and B are then added to yield the total time, C, required for mass memory access and information transfer. On the right hand side of the diagram the number of iterations of the data base, M, may range from 1 to 10, depending on the number of items which must be processed. The number of instructions per iteration, N, may range from 100 to 1,000, depending on how complicated the operational software is for each iteration. The M and N then combine to yield the total number of instructions required to generate a display shown as D instructions. The number of instructions then must be divided into the percentage of short instructions, P, and the percent of long instructions, R. This ratio usually ranges from a 95 to 5 down to a 75 to 25 ratio of short to long instructions. The average time for short instructions, Q, may range from 8 to 20 μs, depending on the type of instructions normally used and whether or not indexing is required. The P and Q factors then are combined to yield the amount of time it takes to execute the short instructions in E seconds. The percentage of long instructions and the average time for a long instruction, S, ranging from 20 to 40 μs yields the long instruction time, F seconds. The E and F then are added to yield the total processing time, G. The C and G are then combined to yield the total time per display, T=C+G seconds.

Table V—Environmental requirements.

Environment	*Operating*	*Non-operating*
Temperature	0 to +50°C.	−40 to +65°C.
Altitude	10,000 ft.	40,000 ft.
Humidity	95%	100%
Shock	2.5 G's, 11 msec.	drop test
Vibration	5 to 1000 Hz, 3 G's	same
Crash safety	N/A	16 GF, 4 GD, 1.5 G S/SA
SIL	64 dB (goal)	same
EMI: 15 kHz to 150 kHz	MIL-STD-826 (interference)	N/A
EMI: 150 kHz to 10 GHz	MIL-I-6181 (inter & suscept.)	N/A
Roll	45°/sec, 100°/sec²	N/A
Pitch	30°/sec, 52°/sec²	N/A
Yaw	20°/sec, 16°/sec²	N/A
Explosion proofing	required	same

An example calculation is shown in Fig. 14 in which it was assumed that the average record size H is 1000 words, and since it was assumed that a full core capacity of 27,000 words are to be transferred, the total number of records I then had to be 27. In case A, the worst case mass memory access time, J, is assumed to be 200 ms which is typical for the 1 head per 100 track type of mass memory. The word transfer time was assumed to be 100 microseconds, which is a worst case type of transfer.

These figures then combine to yield a C value equal to 8.1 seconds. The number of iterations of the data base, M, was assumed to be a worst case condition of 10, while N, the number of instructions per iteration, was assumed to be 1,000. With the worst case mix of 75% short and 25% long instructions, the worst case short instruction time of 20 μs and the worst case long instruction time of 40 μs, the total processing time, G, is 0.25 second. Thus, Fig. 14 shows that the throughput speed, the time required to generate a display, is highly dependent on the access time and the transfer rate of the mass memory device and is relatively insensitive to the processing speed or the amount of processing required. The advantage of a head-per-track type of mass memory is confirmed in Case B where a 20 ms access time cuts throughput time to less than 3.5 seconds.

Current status

The PACCS-ADA system is well on the way to fulfilling its intended mission[3]. The system successfully passed its in-plant demonstration milestone on 18 January 1969. By 27 May, 1969, the system successfully passed a series of eight flight tests. The system, installed in the SAC Airborne Command Post, is undergoing a year-long period of intensive testing.

The experience with PACCS-ADA provides the airborne data manager with an expanded set of ground rules which make practical the processing of large amounts of data during the mission.

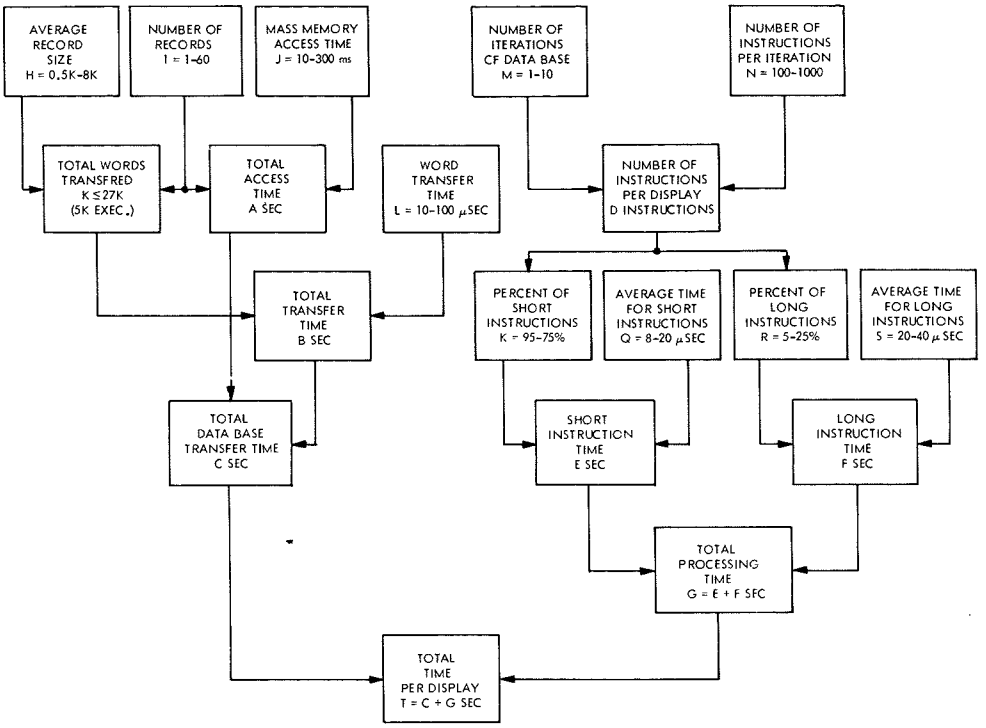

Fig. 13—Calculation flow for ADA display generation time.

Assume: H=1000, I=27, L=100×10⁻⁶, K≤27×10³, M=10, N=1000, P=75% D, R=25% D, Q=20×10⁻⁶, S=40×10⁻⁶

Case A:

For: J=200×10⁻³
K=HI=27×1000
A=IJ=27×200×10⁻³=5.4 sec.
B=KL=27×10³×100×10⁻⁶=2.7 sec.
C=A+B=5.4+2.7=8.1 sec.
D=MN=10×1000=10,000 instructions
P=7500
R=2500
E=PQ=7500×20×10⁻⁶=.15
F=RS=2500×40×10⁻⁶=.10
G=E+F=.25 sec.
T=C+G=8.35 sec.

Case B:

For: J=20×10⁻³
A=0.54 sec.
C=0.54+2.7=3.24 sec.
G=0.25 sec. (same as case A)
T=3.49 sec.

Fig. 14—Example calculations.

Acknowledgments

The authors wish to thank the USAF ESD PACCS-ADA Project Office and SAC PACCS-ADA Task Group for working with RCA to achieve an efficient team effort. Also, the industrial suppliers of the peripheral equipment who worked long and hard to meet tight delivery schedules were essential to the program's success. Although it would be impossible to name all those at RCA who contributed to this program, certain key individuals deserve mention. These are: R. B. Barnhill, Manager of Command and Control Program Operations; H. Brodie, Manager of Programming; J. S. Furnstahl, Manager of Mechanical Design; B. T. Joyce, Manager of Electrical Design; and F. Lee, Manager of Logic Design.

Bibliography

1. Miller, E. H., "Reliability Aspects of the RCA/USAF Variable Instruction Computer," IEEE 1966 Aero/Space Computer Symposium (Oct 24-25, 1966) Miramar Hotel, Santa Monica, California. For a condensed version see Miller, E. H., "Reliability Aspects of the RCA/USAF Variable Instruction Computer, *IEEE Transactions on Electronic Computers*, Vol. EC-16, Nov 5 (October, 1967) pp. 596-602.
2. Spence, A. L., "A machine organization solution—the variable instruction computer," *Proceedings of the First Spaceborne Computer Software Workshop* (20-22 Sep 1966) Aerospace Corporation, El Segundo, California.
3. "Airborne Automation for SAC, primary role for AWACS Swings to tactical air operations," Armed Forces Management (Jul 1967).

Elastic-membrane model for estimation of electron trajectories

F. W. Brill

A stretched rubber membrane can be used as a physical model of the electrical potentials around the electrodes in a two-dimensional electric field. The validity of this model is capable of rigorous mathematical proof. A ball rolling on the surface of this membrane follows a path analogous to the trajectory taken by an electron in such an electrical environment. This analogy can also be verified mathematically. The construction of the rubber-membrane model is relatively simple and inexpensive.

THE DESIGN of many practical electron devices is critically dependent upon the accurate prediction of electron trajectories for a particular kind of electric-field symmetry. For a device in which the electric field is axially symmetric (e.g., an electric lens), cardinal points and planes can be used to determine the paths of the electrons.[1] The operation of many devices, however, is based on the motion of electrons in electric fields that do not possess axial symmetry. How, for example, can the trajectories be determined for electrons in an electric field in which the potentials are a function of two linear dimensions?

This paper first discusses several representative practical devices for which a knowledge of electron trajectories through electric fields that have a two-dimensional symmetry is a basic design requirement. It then points out that these trajectories can be closely approximated by a simple analog technique in which a suitably stretched elastic membrane is used as a physical model of the electrical potentials and steel or glass balls rolling on this membrane are used to simulate the motions of the electrons through the electric field. A rigorous mathematical verification of the validity of this technique is shown, and the construction and application of an elastic-membrane model are described.

Electron devices that depend on accurate electron trajectory prediction

Photomultipliers

In a photomultiplier, the design of the multiplier section requires a knowledge of electron trajectories in a two-dimensional field. The multiplier section (Fig. 1) consists of several cylindrical electrodes (dynodes) which are, in essence, curved pieces of flat sheet. However, because the electrodes are all perpendicular to a given reference plane, the potential gradient is essentially two-dimensional; i.e., the dynode potentials can be expressed in two linear dimensions independent of a third. Fig. 2 shows the dynode arrangement and electric-field distribution in the multiplier section, and Fig. 3 shows the electrons paths for this type of arrangement.

If edge effects are neglected, the potentials around the dynodes are independent of the dimension parallel to the planar direction of the dynodes (direction into the paper in Figs. 2 and 3). In 1938, Pierce[2] showed that it would be worthwhile to solve the electron-trajectory problem for a photomultiplier because of the definite advantages that the resultant device would have over a photocell-amplifier combination. He showed that the new multiplier would be smaller and would have an excellent high-frequency response, a nearly flat response to DC, and minimal microphonics.

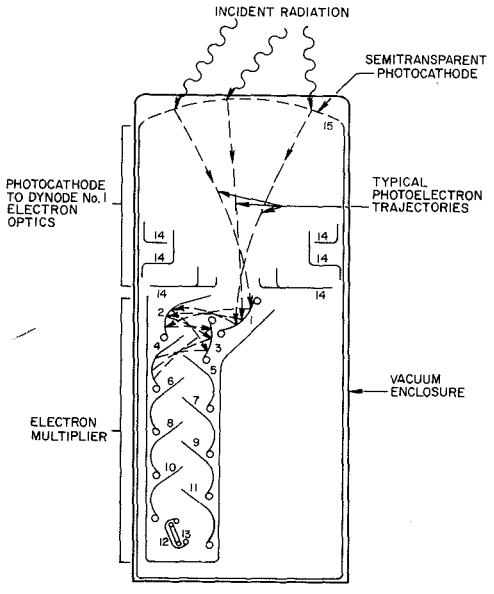

Fig. 1—An experimental electrostatic multiplier phototube.[9]

Electron-trajectory solution is used to determine the location and shape of all the tube structures to maximize the gain for a given number of dynode stages. This condition occurs when all the electrons emitted from one dynode travel to the next dynode and have sufficient energy (about 100 V) to produce more secondary emission. (Great effort is expended in other electron-tube devices to eliminate the effect

Reprint RE-16-3-12 (ST-4309)
Final manuscript received April 20, 1970.

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received the BS in 1950 from Western Maryland College. He majored in chemistry and minored in physics, and received the MS in Chemistry in 1965 from Franklin & Marshall College. In 1950 he joined the Lansdale Tube Company where he worked in the production engineering department of the B&W television tube line. He transferred to the newly formed transistor manufacturing facility in 1952. In 1954, Mr. Brill joined the Brown Instrument Division of Minneapolis Honeywell, Inc. There he worked in the electro-mechanical activity responsible for improvements in the performance of the null balance temperature recorders and indicators. In 1957, he started his own business which reclaimed germanium from the wastes of transistor manufacture. In 1959, he sold the business and joined the Equipment Development Department, EC, RCA, Lancaster, Pa. where he is involved in the manufacture of electron tubes. Mr. Brill is a registered Professional Engineer in Pennsylvania, a member of PSPE, and has been granted two patents.

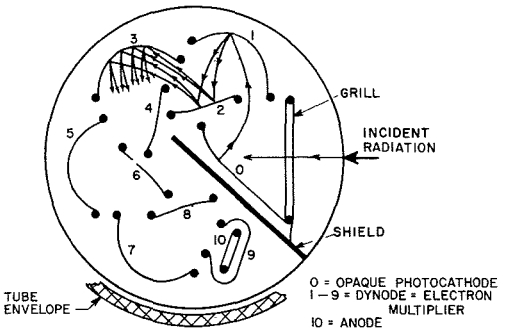


Fig. 2—Diagram showing the basic principles of operation of the multiplier section of a multiplier phototube.[10]

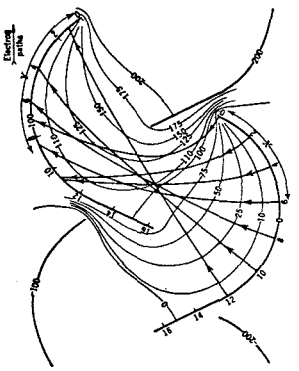


Fig. 3—Electron paths in a multiplier phototube of the type shown in Fig. 1 as determined from the potential plot.[11]

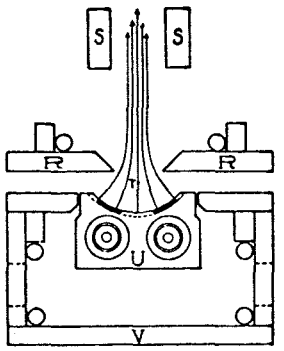


Fig. 4—Section of the source assembly in a mass spectrograph showing the heated block, *U*, upon which the emitter is shown in black, and the water jacket, *V*, surrounding it. The accelerating potential is applied between *UV* and the water-cooled slit, *R*. The path of the ion particles, in the absence of space charge, is shown by the arrows. The dotted lines at the sides are evacuation holes.[12]

encouraged here.) Furthermore, the gradient near each dynode must be such that, as new secondary electrons are produced, they are directed to the next dynode. High space-charge densities must also be avoided.

Mass spectrographs

Two-dimensional electric-field symmetry is also used in the ion-source assembly of some mass spectrographs. In 1934, Smyth, Rumbaugh, and West[8] desired to optimize the design of an ion source in which the ions would be collimated through a rectangular slit to permit the separation of particular isotopes. In their design, shown in Fig. 4, the source is a portion of a cylinder whose axis is parallel to the long side of the slit, and the potential gradient is two-dimensional. The potentials are constant at all points in any line parallel to the axis of the cylinder. In the case of a mass spectrograph, the charged particles are ions instead of electrons, but the same laws apply for all charged particles in an electrostatic field regardless mass or sign of charge.

Beam power tubes

Beam power tubes are another example of devices that use the same kind of two-dimensional field so that the electron energy is independent of one coordinate; i.e., there is no side-directed potential gradient. Fig. 5 shows the internal structure and the electron trajectories in a typical beam-power tube. Schade[4] reported on the development of a beam power tube in 1938. This tube, although it is a tetrode, has the property of suppressing secondary emission from the plate without the undesirable effects of a "knee" in its dynamic characteristics which occurs in pentodes.

Experimental methods to determine electron trajectories

How can electron trajectories in a two-dimensional field be determined? The integration of the equation of motion in these fields is at least as difficult as that for fields that have axial symmetry. Fortunately, however, the techniques of numerical integration can be replaced advantageously by empirical methods.

The electric field can be determined using an electrolytic tank, and graphical-ray tracing can then very closely approximate the electron trajectories. This method is valid both for two-dimensional fields and for axially symmetric fields because, in essence, the two-dimensional field is but the cartesian-coordinate equivalent of the axially symmetric field expressed in cylindrical coordinates. In a two-dimension field, only x and y need be considered; in an axially symmetric field, only z and r need be considered.

Electron trajectories in a two-dimensional field can, however, be directly determined by what is really a simple analog computer suggested by Oliphant and Moore in 1929. The basic premise of this device, called the rubber dam or elastic membrane, is that a little steel or glass ball rolling on a stretched rubber sheet which has been deformed in proportion to the magnitude and location of the negative electrode potentials can model the situation in an electron tube.

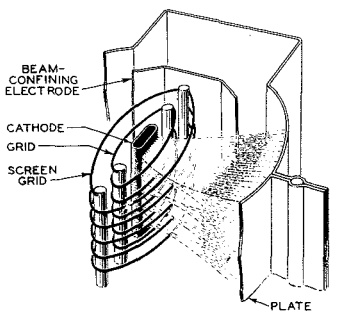


Fig. 5—Internal structure of a type 6L6 or 807 aligned-grid beam-power tube.[13]

The validity of the rubber-dam analogy can be verified, as will be shown in the following section, by a rigorous mathematical proof which closely follow that given by Zworykin and Morton.[5] The rubber-dam technique is now fully accepted as a simple, convenient method for estimating electron trajectories in two-dimensional electric fields and thus, has become a very useful tool in the design of electron devices where knowledge of such trajectories is essential. As one example, Zworykin and Rajchman[6] reported on the use of the rubber dam to establish the optimum photomultiplier design.

Mathematical verification

The mathematical proof for the elastic-membrane model consists of showing that the premises made for this model are valid. That is, it must be proved that the gravitational distribution of a stretched rubber membrane is physically equivalent to the electric-potential distribution between the electrodes of a two-dimensional field and that the equations of motion of a ball rolling on this membrane are identical to the equations that describe the movements of an electron in the two-dimensional field.

Basis for the elastic-membrane analogy

The electric potential distribution of any configuration of electrodes is

given by Laplace's differential equation, the generalized form of which is simply

$$\nabla^2 V = 0 \qquad (1)$$

In the two-dimensional case under consideration, this general form reduces to

$$\frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2} = 0 \qquad (2)$$

The equation for the gravitational forces acting on a stretched membrane is identical in form to Eq. 2, as shown in the following discussion. Fig. 6 is a diagram of forces acting on an element of a stretched membrane. The vector sum of all these forces must be zero, and all forces must act tangentially to the surface at any point because the area is in equilibrium and no external forces are applied.

Let F_1, F_2, F_3, and F_4 represent the forces acting on the sides of the element as shown in Fig. 6. Then,

$$F_{1x} = F_1 \cos\alpha = F_1 \left\{ \frac{(dx/dx)_1}{[(dx/dx)_1^2 + (dz/dx)_1^2]^{1/2}} \right\} \qquad (3)$$

similarly

$$F_{1z} = F_1 \sin\alpha = F_1 \left\{ \frac{(dz/dx)_1}{[(dx/dx)_1^2 + (dz/dx)_1^2]^{1/2}} \right\} \qquad (4)$$

Where $(dz/dx)_1$ is sufficiently small, the following approximation can be assumed:

$$(dx/dx)_1^2 + (dz/dx)_1^2 = 1 \qquad (5)$$

Then, from Eqs. 3 and 5,

$$F_{1x} \approx F_1 \qquad (6a)$$

$$F_{3x} \approx F_3 \qquad (6b)$$

and from Eqs. 4 and 5

$$F_{1z} \approx F_1 (dz/dx)_1 \qquad (7a)$$

$$F_{3z} \approx F_3 (dz/dx)_3 \qquad (7b)$$

Along the coordinate axes, all forces must be equal and opposite; therefore,

$$F_{3x} = -F_{1x} \qquad (8a)$$

and

$$F_3 \approx -F_1 \qquad (8b)$$

The relationship expressed by Eq. 8b is substituted in Eq. 7b to obtain the following result:

$$F_{3z} \approx -F_1 (dz/dx)_3$$

If all the z components are added together, the following equation for the upward force (F_{1z} and F_{3z}) on the membrane is obtained:

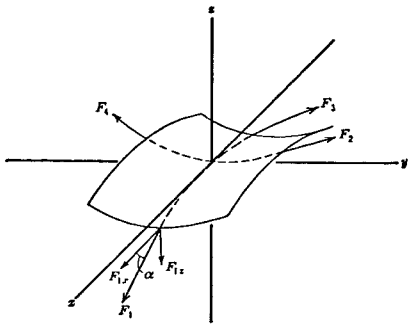


Fig. 6—Forces acting on an element of a stretched membrane.[14]

$$F_{1z} + F_{3z} = F_1 [(dx/dx)_1 - (dz/dx)_3] \qquad (9)$$

The difference between the slopes at P_1 and P_3 (refer to Fig. 6) with y constant is approximated by the second partial derivative of z with respect to x, multiplied by the element of length Δx; therefore,

$$F_{1z} + F_{3z} = F_1 \frac{\partial^2 z}{\partial x^2} \Delta x \qquad (10)$$

If the membrane has been evenly stretched in the x and y directions initially, so that the tension force per unit length (δ) is constant; then

$$F_1 = \delta \Delta y \qquad (11)$$

and

$$F_{1z} = F_{3z} = \delta \frac{\partial^2 z}{\partial y} \Delta y \Delta x \qquad (12)$$

In like manner, the forces on the membrane in the y direction are

$$F_{2z} + F_{4z} = \delta \frac{\partial^2 z}{\partial y} \Delta y \Delta x \qquad (13)$$

Finally, because the sum of all z components must be zero, i.e.,

$$F_{1z} + F_{3z} + F_{2z} + F_{4z} = 0 \qquad (14)$$

then

$$\delta \frac{\partial^2 z}{\partial x^2} \Delta x \Delta y + \frac{\partial^2 z}{\partial y^2} \Delta y \Delta x = 0 \qquad (15)$$

or

$$\frac{\partial^2 z}{\partial x^2} + \frac{\partial^2 z}{\partial y^2} = 0 \qquad (16)$$

If this last expression is compared to the Laplace equation for the potential distribution in a two-dimensional electric field (Eq. 2), the equations are seen to be identical if z is replaced by V.

The physical significance of this relationship is that a membrane may be used to represent the electrical potential between the electrodes of a device. The dimensional configuration of the electrodes is usually scaled up in the model to facilitate study. The vertical displacement of the membrane at the electrode location must be proportional to the electrical potential on the actual electrode. The displacement of the membrane in the vertical direction anywhere between the simulated electrodes is then proportional to the electrical potential in the corresponding location in the device. For studies of the trajectories of negative particles the upward displacement of the membrane is scaled in the direction of increasing negative potential. For studies of the trajectories of positive particles the upward displacement of the membrane is scaled in the direction of increasing positive potential.

Justification for the use of a rolling ball to simulate a moving electron

When the rubber-membrane model is used, it is assumed that a ball rolling down the slope of the membrane traces a path that corresponds to the motion a particle in the electric field of an actual device. To prove this assumption, the principle of "least action" is employed.

The principle of least action states that any particle moving in a potential field will follow a path such that the integral of the momentum through the path of the particle is a minimum, i.e.,

$$\delta \int_A^B mv \, ds = 0 \qquad (17)$$

Because the system is conservative, the sum of the kinetic and potential energies must remain constant.

A charged particle starting from rest and falling through a potential difference V, will attain a velocity v, such that

$$\tfrac{1}{2} mv^2 = eV$$
$$mv = (2em)^{1/2} V^{1/2} \qquad (18)$$

or in a two-dimensional field, the increment, ds, is given as follows:

$$ds = [dx^2 + dy^2]^{1/2} = dx \, [1 + (dy/dx)^2]^{1/2} \qquad (19)$$

The substitution of these values of

mv from Eq. 18 and ds from Eq. 19 yields

$$\delta \int_A^B (2em)^{1/2} V^{1/2} [1+(dy/dx)^2]^{1/2} dx = 0 \qquad (20a)$$

or, since em is constant,

$$\delta \int_A^B (V)^{1/2} [1+(dy/dx)^2]^{1/2} dx = 0 \qquad (20b)$$

Eq. 20b is the action integral of the particle moving in a two-dimensional electric field. The trajectory is independent of the mass or charge of the particle.

Now, consider the ball on the rubber surface. For the moment, assume that the ball is sliding instead of rolling and that friction is negligible. This system is also conservative, so that gains in kinetic energy are balanced by losses in potential energy. That is,

$$K.E. = -P.E. \qquad (21)$$

or

$$\tfrac{1}{2} mv^2 = -mgz \qquad (22a)$$

and

$$mv = -m\,(2gz)^{1/2} \qquad (22b)$$

Also,

$$ds = [dx^2+dy^2+dz^2]^{1/2} = [1+(dy/dx)^2+(dz/dx)^2]^{1/2} dx \qquad (23)$$

Because the quantity $(dz/dx)^2$ is small compared to unity, the following approximation can be used:

$$ds = [1+(dy/dx)^2]^{1/2} dx \qquad (24)$$

The action integral (Eq. 20b) is as valid for the ball as for the electron because the gravitational effects on the ball conform to Laplace's differential equation. Therefore, if mv and ds are replaced by the values given in Eqs. 22b and 24, the action integral for the sliding ball becomes

$$-m\sqrt{2gz}\,\delta \int_A^B z^{1/2} [1+(dy/dx)^2]^{1/2} dx = 0 \qquad (25a)$$

or

$$\delta \int_A^B z^{1/2} [1+(dy/dx)^2]^{1/2} dx = 0 \qquad (25b)$$

Eq. 25b is equivalent to Eq. 20b, the action integral for the electron in a two-dimensional field, if V is substituted for z. Thus, the path of a body sliding on the rubber surface is geometrically similar to the corresponding electron trajectory. The trajectory is independent of the mass of the body, or the acceleration due to gravity.

If it is assumed that the ball is rolling, the displacement relationships are as follows:

$$ds = R\,d\alpha \qquad ds/R = d\alpha \qquad (26)$$

where ds is an element of displacement of the center of mass, $d\alpha$ is an element of rotation of the ball, and R is the radius.

The angular velocity (ω) in terms of linear velocity can then be expressed as

$$\omega = d\alpha/dt = ds/R\,dt = v/R \qquad (27)$$

The kinetic energy is the sum of the rotational and translational kinetic energies, or

$$K.E. = \tfrac{1}{2} mv^2 + \tfrac{1}{2} I\omega^2 \qquad (28)$$

where I is the moment of inertia of the ball.

If (ω) is replaced by v/R, the equation for the kinetic energy becomes

$$K.E. = \tfrac{1}{2}mv^2 + \tfrac{1}{2} I\,(v^2/R^2) = \tfrac{1}{2} v^2\,(m^2+I/R^2) = \tfrac{1}{2} v^2 m' \qquad (29)$$

where m' is the effective mass. Whether m or m' is used in the equation does not change the final result because the path is independent of mass.

Zworykin and Morton have plotted (see Figs. 3 and 7) electron and ball trajectories between dynodes of a photomultiplier. The correlation is rather good.

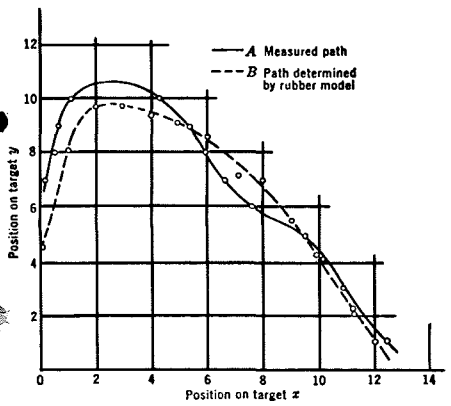


Fig. 7—Curves showing termini of electron trajectories in the multiplier as determined by direct measurement and from a rubber model.[11]

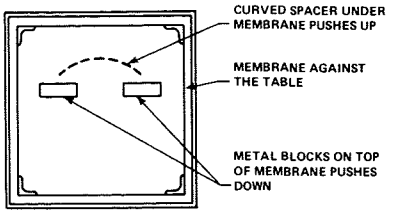


Fig. 8—Diagram of the frame used to support the membrane in the elastic-membrane model.

Because errors depend upon electron path, numerical values for accuracy are difficult to give. Zworykin and Morton state, however, that even if the slope dz/dx becomes 30 to 45 degrees and the tension in the membrane is far from uniform, practical results can still be obtained.

Walker states that the error in the estimation of the kinetic energy of the ball can be maintained to less than 2%. He also discusses the details of how to scale up a problem most advantageously.

Construction and application of an elastic-membrane model

An elastic-membrane model can easily be constructed and used to solve electron trajectories. A demonstration model need not be as complicated as one intended for research. For such models, a stretched membrane properly attached to a 3-foot-square frame of soft wood, braced in the corners with steel angle brackets, would be suitable. A frame of this type, shown in Fig. 8, can be built in any woodworking shop. For the elastic membrane, a rubber dental dam such as made by Davol at a cost of about $1.50 per square foot could be used. The model is assembled as follows:

1) Place the dental-dam elastic membrane under the frame; make sure that it is free of wrinkles.
2) Mark a pencil line on the elastic membrane along the inside of the frame.
3) Place the frame under the elastic membrane.
4) Stretch the membrane and with thumb tacks attach it at each corner so that the pencil mark is aligned, as nearly as possible, with the outside edge of the wooden frame.
5) Tack the membrane at the mid-point of each side and at the corners.
6) Tack the membrane at points midway between existing tack points (8 points).

7) Repeat Step 6, (16 points). The tension on the membrane will not be quite uniform; as a result, the pencil line will not be perfectly straight. Uniformity can be improved by using 32 more thumb tacks, but the results will be only slightly improved.

When the elastic-membrane model is used to trace trajectories of negative particles, the frame is first placed on a flat level surface; the most positive potential will then be represented by the lowest point. If the frame is oriented so that the membrane lies against the level surface, the model corresponds to a square electrode at a uniform positive potential. If the frame is turned over so that the membrane is spaced 1 inch above the level surface, the model then corresponds to a square electrode at ground potential. Spacers shaped similarly to the electrodes are placed under the membrane to simulate the geometry of the device. The height of the spacers is proportional to the potential of the electrodes. The spacers may be fastened to the table with drafting tape. The membrane is then placed over the spacers so the frame rests on the table. Needless to say, spacers that do not deform the membrane are ineffective in simulating electrodes. Equipment to deform the membrane by pressure from above is somewhat complicated in the research model. In the student model, steel bar stock can be used to press the membrane against the table by the weight of the steel alone.

An aperture slit lens such as used in the mass spectrometer can be readily simulated. In this arrangement, shown in Fig. 9, the membrane is placed against table over a curved spacer, and two metal blocks are placed on the membrane to push it against the table. Additional weight might be balanced on the top edge of these blocks to supply enough force to deform the membrane.

When a 3/8 inch diameter steel ball used to represent an ion, is released from various positions along the curved electrode (ion source), it can be focused by the nearby metal blocks (electrodes) so that a concentrated parallel beam emerges. The radius of curvature of the ion source and the location of the beam forming electrodes must be adjusted so that the ball does not hit the beam-forming electrodes and so that the emerging paths do not diverge.

The configuration described above can be adapted to a laboratory experiment where, for given electrode potentials, the experimenter, by trial and error, determines the configuration that makes the most concentrated beam.

Other configurations that might be of interest are the potential distribution around:

a) parallel planes,
b) an internal wire and a cylinder,
c) a plane and a wire, and
d) cylinders of various diameters.

The principal value in working with the rubber dam is that the experimenter is given a physical picture of a phenomenon that is difficult to visualize; namely, the "shape" of the electric field and the direction of motion of a charged particle within the field. A simple lecture demonstration can readily show that, without the rubber dam, the determination is a highly complex problem. A novel game approach in which the rubber dam model is set up as a pinball machine, in configurations similar to those shown in Fig. 10, can be used to make the demonstration more memorable.

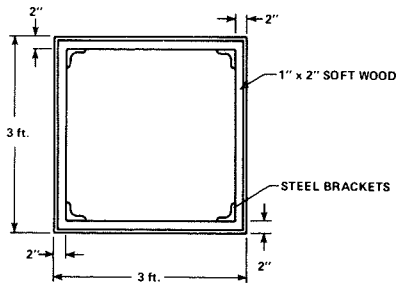


Fig. 9—Diagram showing the configuration of an elastic-membrane model used to simulate the aperture split lens of a mass spectrometer.

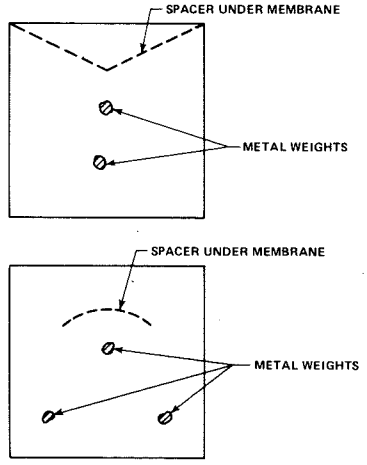


Fig. 10—Example of elastic membrane pinball machine configuration.

In the pinball models, the height of the spacer used under the rubber sheet should be no greater than that of the frame itself so that when the frame is placed over the spacer with the rubber sheet away from the table, the ball will not escape from the elastic surface. One-inch lengths should be marked off along the top edge of the spacer with black ink. These marks, which will be visible through the membrane, are needed so that the location along the spacer at which the ball is released can be determined. After the membrane is properly positioned over the spacer, metal weights of bar stock are placed on it to form the desired depressions.

In the game, participants are asked to predict the depression into which the ball will come to rest for a given point of release along the spacer. A couple of million game points can be given for each correct prediction so that any pinball playing addict may feel at home. Megapoint scores, notwithstanding, the percentage of correct guesses will be rather low. A comparison of the actual results with the predicted ones will provide a fuller appreciation of the problem of determining the paths of charged particle in electric fields.

References

1. Klemperer, O., *Electron Optics* (2nd Ed., Syndics of the Cambridge University Press, 1963).
2. Pierce, J. R., "Electron Multiplier Design," *Bell Laboratories Record* Vol. 16 (1938) p. 305.
3. Smyth, W. R., Rumbaugh, L. A. and West, S. S. "A High Intensity Spectrograph," *Physical Review* Vol. 45 (1934) p. 724.
4. Schade, O. H., "Beam Power Tubes" *Proc. of the IRE* Vol. 26 (1938) p. 137.
5. Zworykin, V. K. and Morton, G. A., *Television* (2nd Edition, Wiley, 1954) p. 108.
6. Zworykin, V. K. and Rajchman, J. A., "The Electrostatic Electron Multiplier" *Proc. of the IRE*, Vol. 27 (1939) p. 559.
7. Walker, G. B.—*J. of the Institute of Electrical Engineers,* Part II, Vol. 96 (1949) p. 319.
8. Cooper, J., "Rubber Model for Demonstrations and Laboratory Experiments," *American J. of Physics* Vol. 28, No. 7 (1960) pp. 644-645.
9. Zworykin, V. K. and Morton, G. A., *op. cit.*, p. 114.
10. Reich, H. L., "Theory and Application of Electron Tubes" (McGraw-Hill, 1939) p. 514.
11. Zworykin, V. K. and Morton, G. A. *op. cit.*, p. 115.
12. Smyth, W. R., Rumbaugh, L. A., and West, S. S., *op cit.*, p. 726.
13. *RCA Receiving Tube Manual,* Technical Series RC-27, (RCA, Electronic Components, Harrison, N.J., 1970) p. 9.
14. Zworykin, V. K. and Morton, G. A., *op. cit.*, p. 110.

IC voltage regulators—the pluses and minuses

S. Graf

Integrated-circuit voltage regulators are presently being used as substitutes for discrete-component types in many applications where size, weight, power consumption, or reliability are primary factors. In addition, because of their qualities as an integrated device, IC regulators are being used in applications beyond those envisioned for traditional devices. This paper discusses the key elements involved in the design and development of IC voltage regulators and presents several possible applications.

THE INTEGRATED-CIRCUIT MARKET has been dominated by a few basic devices. In fact, the success of integrated-circuit technology is mainly the result of these few versatile building blocks. For example, a few standard configurations of the integrated logic gate satisfy most of the present digital market requirements. The IC operational amplifier offers similar features for linear industrial systems.

Aside from the obvious features of limited size and cost, these devices exploit the inherent advantages of monolithic IC technology, such as geometrical proximity of components with the resulting good electrical matching, low parasitic capacitance, and good temperature tracking.

The IC voltage regulator is also becoming one of these few standard elements in electronic systems because it offers all the aforementioned advantages and provides versatility that satisfies an appreciable part of the solid-state market. A typical voltage regulator is essentially a three-terminal device that delivers a constant voltage between output and common terminals with an unregulated voltage applied between input and common terminals. Because many applications require a wide range of output voltages and currents and additional features such as frequency compensation, overload protection, and the like, most commercial regulators contain more than three terminals.

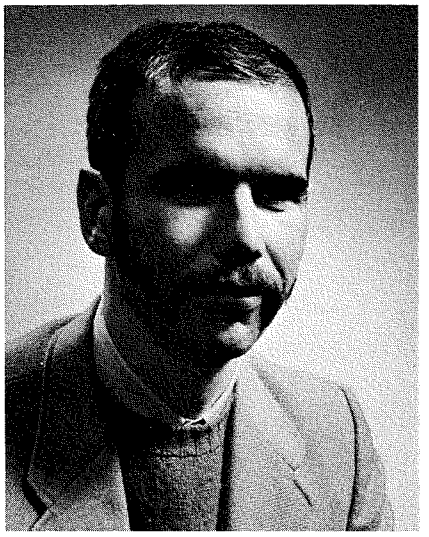
Fig. 1 shows the block diagram of a typical commercial voltage regulator. In this circuit, an error amplifier senses the differences between the constant reference voltage and a fraction of the output voltage and drives the pass element to compensate for this difference and regulate the output voltage. Because an ideal regulator delivers constant output voltage regardless of line variations or changes in load or ambient conditions, the three characteristics best describing its behavior are line regulation, load regulation, and temperature coefficient.

Line regulation is the change in output voltage for a specified change in input voltage under a constant load and temperature (a similar effect in AC is the ripple rejection).
Load regulation is the change in output voltage for a specified change in load current (in AC applications, the output impedance is usually measured).
Temperature coefficient is the change in output voltage for a specified change in ambient temperature.

These three characteristics affect the performance of various circuit parts of the regulator.

Reference circuit

The key element in the regulator performance is the reference circuit. This circuit is important because any variation in the reference voltage produced by line or temperature variations directly affects the output, and there is no way to adjust for it. Figs. 2 and 3 show two practical reference circuits. The main component in these circuits is a low dynamic-impedance element (normally one or more zener diodes or other diodes) that maintains a relatively constant voltage with the existing line variations. The remaining reference-circuit components serve either as compensation for the temperature coefficient of the low impedance element or as a source of a relatively constant current supplied to this element through a feedback arrangement. In Fig. 2, the positive temperature coefficient of the zener diode and the negative one of the other diodes are exactly compensated by the positive temperature coefficient of the resistor. In the circuit of Fig. 3, which uses only active devices, the temperature coefficient of the two diodes on the left



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Reprint RE-16-3-7 (ST-4321)
Final manuscript received July 23, 1970.

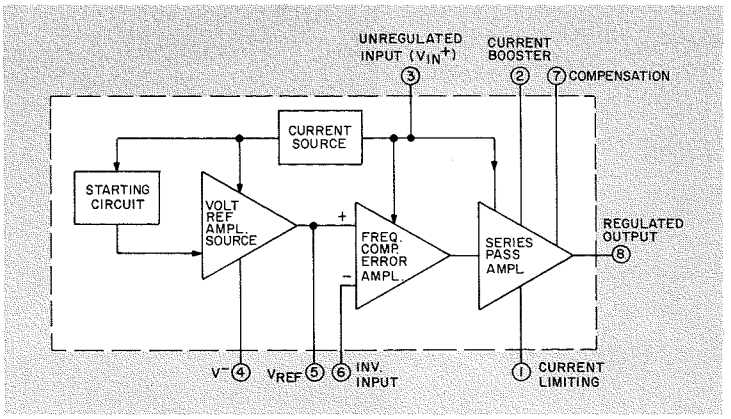


Fig. 1 Block diagram of a typical commercial voltage regulator.

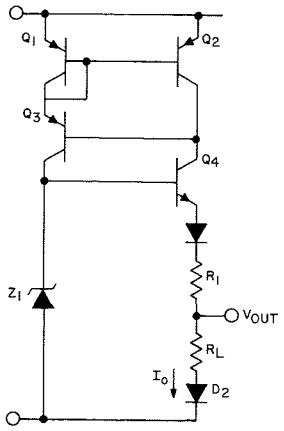


Fig. 2 Reference circuit.

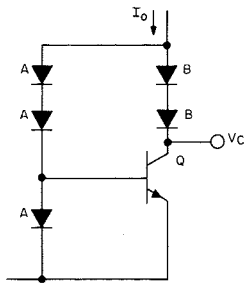


Fig. 3 Reference circuit using only active devices.

balances the coefficient of the diodes on the right, which yields a zero temperature coefficient at the output point V_C. The output voltage in this case is equal to the value of the bandgap for silicon. In this configuration, extensive use is made of geometrical similarity to control V_{BE}. Schemes of this type achieve a typical 5-mV reference-voltage regulation over the ambient temperature range. The current for the main reference elements, a zener diode in Fig. 2 and three diodes in Fig. 3, is delivered by current-mirror configurations to insure a constant current and a line voltage independence.

Error-voltage amplifiers

As stated previously, an error in the reference is transferred directly to the output. Under the assumption that the reference is ideally constant, both line and load regulations become directly proportional to the gain of the error amplifier. The best configuration for high gain (or transconductance) is an N-P-N differential amplifier with a P-N-P active load. In Fig. 4, the currents produced by the current-source transistors Q_9 and Q_{10} of the active load in the collectors of the differential pair Q_5, Q_6 will be equal if similar geometry of current-source transistors is assumed. Any differential voltage at the input appears, therefore, as a differential current at the base of the pass element Q_{13}, Q_{14}, and there is no loss of differential current to the load as in a resistive load.

Other configurations are sometimes used, but all operate on the principle of delivery of the differential output-current of the amplifier to the pass transistor. Besides the high gain feature, these configurations allow a large variation for the voltage across the amplifier without any appreciable changes in the transconductance and in the operating point of the amplifier. As a pass element, an N-P-N Darlington configuration is used because of its high gain and high current-handling capability. The output power transistor that determines the maximum load current requires a very special design, which will be described later.

Voltage regulator circuit

At this point, it is appropriate to consider the interconnections and interactions of all the elements of the voltage regulator. Fig. 5 shows the basic regulator configuration where a fraction of the output voltage is compared with the reference. An alternate configuration is also possible that compares the full output voltage with a fraction of the reference. A choice between these two modes of operation depends on the desired output and on the available reference.

Regulators featuring two error amplifiers have also been used. The result is an increase of the loop gain and an improvement in the regulation at the expense of flexibility and AC stability. All of the described elements can operate over a wide range of input and output voltages, satisfying one of the basic requirements related to flexibility of usage.

The limiting factor for the minimum input voltage in the regulator is the reference circuit. If a zener diode is used, this voltage is approximately 8 volts. Diodes used as shown in Fig. 3 require only 3 to 4 volts; however, these voltages can be lowered with other diode arrangements. Similarly, the minimum output voltage is set by the value of the reference. The maximum input voltage on the other hand is limited by the processing capability (the $V_{(BR)CEO}$ of the active devices) and is presently close to 40 volts.

Obviously, both input and output voltage ranges should be as wide as possible to enhance the versatility of the circuit. At present, input voltages for most solid state applications range between 4 and 40 volts, and outputs range between 2 and 36 volts. Related to these parameters is the input-output voltage differential. This differential defines the closest approach of the output voltage to the input voltage under the proper regulator operation.

For the circuit of Fig. 4, the determining factors are the drop across the active load of the error amplifier and the drop across the pass element ($2V_{BE}$ in this case). The input-output differential gives an indication of the efficiency of the regulator and, multiplied by the load current, the minimum power dissipated in the chip. Different applications vary widely in their maximum current requirements; therefore, a large maximum load current increases versatility. At present, there are integrated regulators on the market with maximum output capability varying between 10 to 500 mA. For most applications, at least 100-mA output is necessary. The choice in these cases involves either a power transistor on the chip or an external booster transistor and a limited output capability. A power transistor on the chip, such as in the CA3055, requires: 1) a larger chip size and special power transistor design (second breakdown considerations) and 2) a special package to handle the large power dissipation on the chip. This arrangement increases the cost of the IC and makes devices featuring an external pass transistor quite competitive.

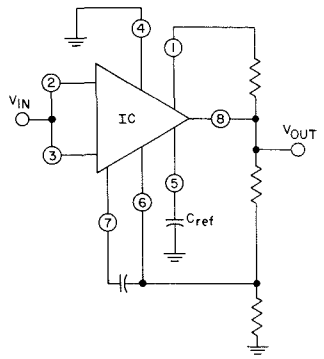


Fig. 5 Basic regulator configuration.

Optional design features

Some additional optional features available in a voltage regulator in-

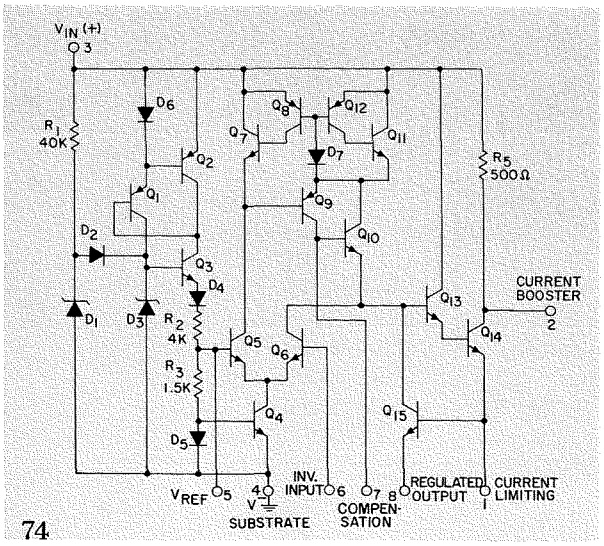


Fig. 4 Schematic diagram of RCA CA3055.

crease its flexibility. Current limiting, or overload protection, is usually provided by an external resistor between the pass element and the load. A transistor senses the voltage drop across the resistor and removes the drive from the pass element if the current limit is exceeded. Some configurations provide the collector of the pass element for the outside connection to allow the use of a P-N-P as external pass transistor. The reference terminal may be connected to an external bypass capacitor to decrease the noise generated by the reference.

Both inputs of the error amplifier are frequently provided for outside connection. This arrangement allows the independent use of the amplifier as power amplifier in connection with the output transistor. Moreover, an additional terminal is usually provided at the output of the error amplifier (at the base of the pass element) to facilitate frequency compensation. The compensation capacitor, needed because the error amplifier is used as a unity-gain closed-loop operational amplifier, is normally connected between this terminal and the feedback terminal and acts as an additional Miller capacitance.

More options, such as thermal shutdown and external shutdown controls are available in some regulators. The number of similar features, however, is practically unlimited and only restricted by the number of pins. For this purpose, a pin-number, flexibility tradeoff is evaluated in relation to marketing considerations.

Chip layout and design—an interdisciplinary effort

The IC voltage regulator is one of the devices that best exemplifies the interdisciplinary nature of the monolithic integrated-circuit technology. For the optimum regulator performance, the circuit layout and device design considerations have to complement the circuit design. This requirement becomes apparent if the temperature coefficient is considered as the most significant. For example, an increase in the load current generates a direct change in the output voltage proportional to the load regulation and an indirect (and larger) variation that results from the rise in chip temperature due to increased internal dissipation.

Minimized temperature effects involve the major challenge in the chip layout. The circuit parts particularly sensitive to thermal gradients are the reference circuitry and the error amplifier.

Temperature compensation

Small temperature differences (of the order of a tenth of a degree) among the circuit elements subject to uneven heating may produce an intolerable temperature coefficient of the output voltage. The major source of heat is usually the pass element which, in the CA3055, covers one side of the chip as shown in Fig. 6. The heat flow could be expected in the direction perpendicular to this side with the isotherms (lines of equal temperatures) parallel to it.

The elements of the terminally sensitive parts have to be laid out close to one another and on the same isotherm (that is parallel to the pass transistor), as shown in Fig. 6, to minimize gradients. This concept, first employed in a voltage regulator in the CA3055, has since been used in several other regulators. The pass element and the package determine the maximum output current. In the CA3055, a multiple-emitter transistor is used with multiple-emitter ballast resistors. This configuration provides an even-current distribution and an even heating across the chip with reduced temperature gradient.

Generally, IC voltage regulators are placed in TO-5 packages. These packages have a rather low heat conductivity (160°C/watt, junction to air) and, therefore, represent the limiting factor for the output-current capability. Different packages with better thermal performance, such as the dual-in-line or TO-66, have been used, and maximum output current in the order of 500mA has been attained.

Lateral P-N-P device

An important aspect of the device design has been the development of the lateral P-N-P device. This device actually enables the voltage regulator to obtain acceptable performance. The CA3055 was the first commercial RCA circuit in which this transistor was widely used.

When the lateral P-N-P device was first used, its current gain was very low (around 1 or 2). This low gain was

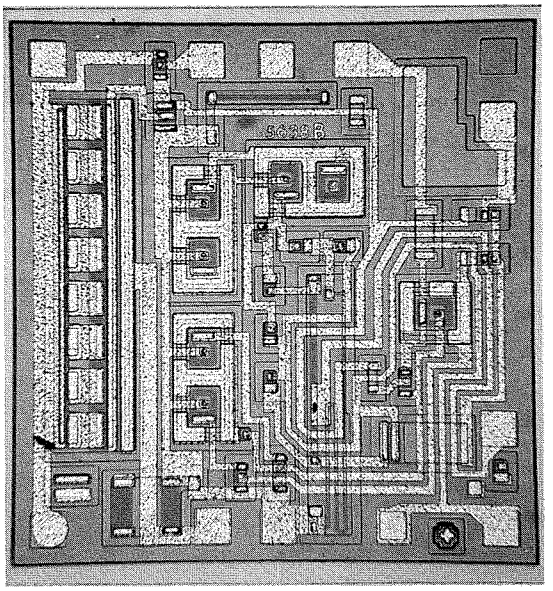


Fig. 6 Photograph of RCA CA3055.

an obvious drawback for many applications. The problem, however, was overcome by the use of a composite structure which the collector of a P-N-P transistor drives an N-P-N transistor. The current gain of this structure, functionally similar to a single P-N-P transistor, equals the product of the current gains of the two transistors.

Other applications

In applications, versatility is the major factor for the success of any integrated circuit. Up to this point, the regulator was considered as a standard series regulator. The IC regulator, however, can easily be connected as shunt regulator, current regulator, and switching regulator by simply changing the connections of the external passive components. Furthermore, the regulator can be used in connection with external active devices as a basic building block in a host of other applications.

These applications include the use of the IC as a floating negative regulator, as a floating high-voltage regulator, and as power amplifier, if both inputs of the error amplifier are available.

This variety of applications is the key for the success of the IC regulator as a standard building block in electronic systems. The IC voltage regulators are now employed both as substitute for discrete voltage regulators and in applications made possible by the very existence of IC's. In these applications, IC regulators are used as central elements of traditional power supplies, as peripheral power supplies in computers or instrumentation systems (e.g., as supplies for IC's on a printed board) and in airborne applications.

Monolithic components for linear integrated circuits

G. F. Granger | H. Khajezadeh | M. Polinsky

In recent years, great strides have been made in the development of suitable components for integrated circuits. Five years ago, the integrated circuit designer was restricted to the use of resistors, standard N-P-N transistors, and small-value capacitors. Now a great variety of active and passive components is available. This paper briefly lists these components and highlights their important characteristics. Prior to a description of the new components and their characteristics, an outline of the basic integrated circuit process is presented. Modifications necessary to form new components are listed where applicable.

THE DIFFUSION STEPS used to fabricate the active and passive components of a monolithic circuit are shown in Fig. 1. A general-purpose transistor has been chosen for illustration.

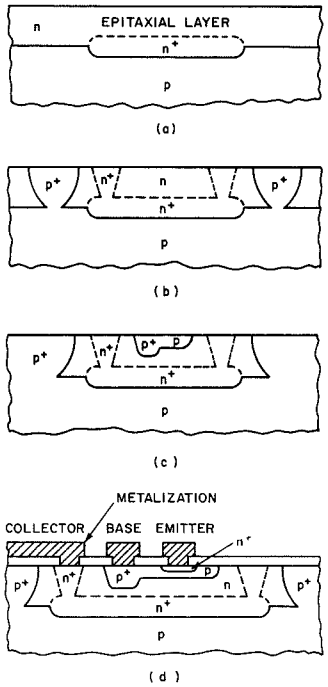


Fig. 1—The diffusion steps used to fabricate the active and passive components of a monolithic circuit: (a) Diffusion of N+ pocket into a P-type substrate; (b) isolation of N areas by P+ diffusion and formation of deep N+ diffusion; (c) a P+ diffusion; (d) formation of contact areas and definition of interconnecting metalization.

In Fig. 1(a), an N+ pocket is diffused into a P-type substrate where a high conductivity N region is required and an N-type epitaxial layer is grown over the wafer. The N areas are then isolated by P+ diffusion, as shown in Fig. 1(b), and a deep N+ diffusion is formed to contact the N+ pocket. The P+ area is then diffused where low-resistivity P regions are required, as shown in Fig. 1(c), followed by a higher resistivity P diffusion to form bases and resistors. Finally an N+ diffusion forms the emitter and high-conductivity N regions, as shown in Fig. 1(d). Then contact areas are opened in the oxide and interconnecting metalization is defined.

Reprint RE-16-3-8(ST-4379)
Final manuscript received August 17, 1970.

Components

The active components used in monolithic integrated circuits fall into three general classes: transistors, control devices, and unijunction devices. The passive components include resistors and capacitors.

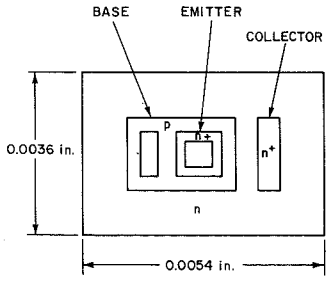


Fig. 2—General purpose transistor with base penetration equal to 2 micrometers.

Transistors

General-purpose N-P-N transistors—Fig. 2 shows the topology and the typical characteristics of the most widely used general-purpose N-P-N transistor in linear integrated circuits. The typical characteristics of the general-purpose transistor are as follows:

Breakdown voltage $V_{(BR)CEO}$
20 V at 1 mA
Static forward-current transfer ratio h_{FE}
80 at I_c=5 mA
and V_{CE}=1 V
Current gain-bandwidth frequency
400 MHz at I_C=5 mA
and V_{CE}=1 V
Noise figure NF
6 dB at I_C=1 mA,
V_{CE}=6 V, and f=100 MHz

High frequency N-P-N transistors—Operation of transistors at frequencies above 200 MHz with low noise and high gain requires modifications to the basic process. The current-gain-bandwidth frequency[1] f_T of a transistor is determined by the following expression:

$$f_T=\frac{\alpha_0 K_e}{2\pi\left[r_e C_{T_e}+\frac{W^2}{2.43\,D_{nb}\ln\left(\frac{N'_B}{N_{BC}}\right)}+\frac{X_m}{2v_{sc}}+r_{sc}C_{T_c}\right]} \quad (1)$$

where α_0 is the common-base current gain; K_e is the phase correction; r_e is the emitter resistance; C_{T_e} is the emitter transition capacitance; W is the effective base width; D_{nb} is the electron-diffusion constant in base; N'_B is the base impurity concentration at emitter junction; N_{BC} is the background impurity concentration; X_m is the depletion-layer thickness; v_{sc} is the scattering-limited velocity; r_{sc} is the collector series resistance; and C_{T_c} is the collector transition capacitance.

Examination of Eq. 1 shows that reduction of base width (shallower emitter and base junctions) and emitter and collector junction areas increase f_T. The reduction of junction penetration necessitates process revisions which are not compatible with the fabrication of the general-purpose device.

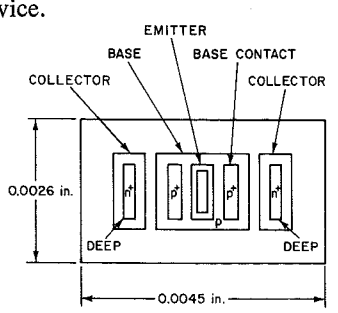
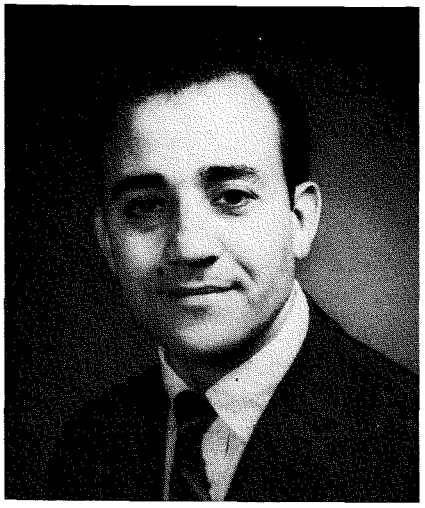


Fig. 3—A high frequency transistor with base penetration equal to 1 micrometer.

Fig. 3 shows the topology of a five-milliampere, high-frequency N-P-N transistor. The two base stripes with P+ diffusion in contact areas are used to reduce intrinsic base-spreading resistance $r_{bb'}$ and, therefore, high-frequency noise. The typical characteristics of a high-frequency N-P-N transistor are as follows:

Breakdown voltage $V_{(BR)CEO}$
20 V at 1 mA



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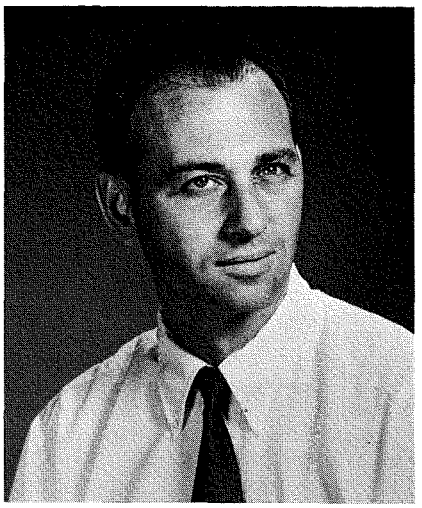

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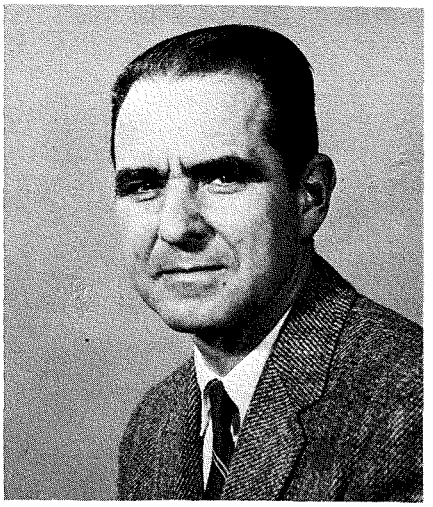

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received the BSEE from Kansas State University in 1950, and the MS in Physics from Stevens Institute of Technology in 1958. Mr. Granger joined RCA in 1952 where he worked in the Semiconductor Development Engineering Group on the development of germanium alloy devices. Since then he has worked in Semiconductor Manufacturing, Development, and Reliability Engineering Groups on both silicon and germanium devices. Mr. Granger has published two papers in the field of reliability engineering on accelerated testing. He has two patents and one pending on solid state devices. He is a member of the IEEE.

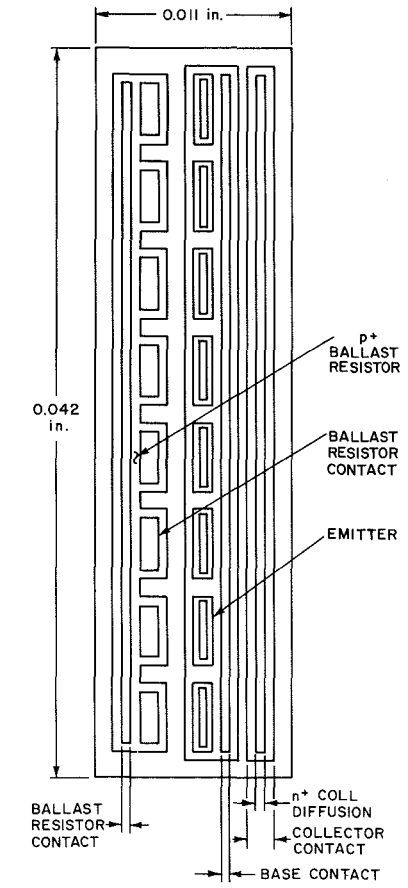

Fig. 4—High current transistor.

Static forward-current transfer ratio h_{FE}
60 at $I_C = 5$ mA
and $V_{CE} = 1$ V

Current gain-bandwidth frequency f_T
1.2 GHz at $I_C = 5$ mA
and $V_{CE} = 1$ V

Noise figure NF
3.0 dB at $I_C = 1$ mA
$V_{CE} = 6$ V and $f = 100$ MHz

High-current transistors—Fig. 4 shows the topology of a high-current monolithic transistor. The current-handling capability of a planar transistor is a function of emitter periphery, emitter area, and collector doping density. Important considerations in the design of a high-current monolithic transistor are defined as follows:

a) Emitter ballasting—emitter ballasting is used to obtain uniform current density and improve second-breakdown capability.
b) Saturation voltage—contacts to IC components are normally restricted to the silicon surface. Therefore, large areas of deep N^+ collector diffusion are used to reduce the collector series resistance and thus improve the linear operating range.
c) Aluminum electromigration—the emitter and collector metalization patterns must be designed to limit current density below 1.5×10^5 amperes per square centimeter to avoid electromigration of aluminum during high-temperature, high-current operating life.
d) Thermal gradients—layout must be designed to minimize the effect of thermal gradients on critical components of the chip.

Typical characteristics of a high-current monolithic transistor are as follows:

Breakdown voltage $V_{(BR)CEO}$
55 V at 5 mA

Static forward-current transfer ratio h_{FE}
60 at $I_C = 500$ mA
and $V_{CE} = 2$ V

Collector-to-emitter saturation voltage $V_{CE(SAT)}$
1.2 V at $I_C = 500$ mA
and $I_B = 50$ mA

High-voltage transistors—The voltage characteristics of an N-P-N transistor are improved by the following methods:

a) Deeper diffusions reduce junction curvature and electric field.
b) Higher collector resistivity reduces electric field for a given voltage.
c) Thicker epitaxial layer allows for increased collector depletion-layer spreading.
d) Field-relief electrodes reduce electric fields.

Typical characteristics of a high-voltage monolithic transistor are as follows:

Breakdown voltage $V_{(BR)CBO}$
250 V
Breakdown voltage $V_{(BR)CEO}$
120 V
Current gain-bandwidth frequency f_T at $V_{CE}=10$ V and $I_C=8$ mA
230 MHz
Collector-to-emitter voltage V_{CE}
10 V
Base-junction depth x_{JB} 6 μm
Epitaxial resistivity 12 ohm-cm
Epitaxial thickness 1.2 mils

P-N-P lateral transistors—The P-N-P lateral device, which is process compatible with the general-purpose N-P-N transistor, has found wide use in integrated circuits as a level shifter and active load. In this device, lateral injection and collection determine the basic transistor characteristics. The emitter-periphery-to-area ratio is maximized to enhance the lateral injection. The emitter metalization overlaps the base region to reduce minority carrier recombination at the surface. This condition also improves reliability by maintenance of a unipotential surface over the base region. The N^+ pocket diffusion beneath the P-N-P lateral is employed to minimize the gain of the P-N-P substrate parasitic transistor.

There are two equations that determine beta and current-gain-bandwidth frequency f_T of the monolithic P-N-P lateral transistor.[2] It is assumed that beta is determined by injection efficiency, and f_T is limited by base transit time. In this case, beta, β, is expressed as follows:

$$\beta=\frac{\sigma_e L_e \rho_W}{W} \qquad (2)$$

where σ_e is the emitter conductivity, L_e is the emitter diffusion length, W is the lateral base width, and ρ_W is the base resistivity. The current-gain-bandwidth frequency f_T is given by

$$f_T=\frac{1.2\, D_P \alpha_0 K_e}{\pi W^2} \qquad (3)$$

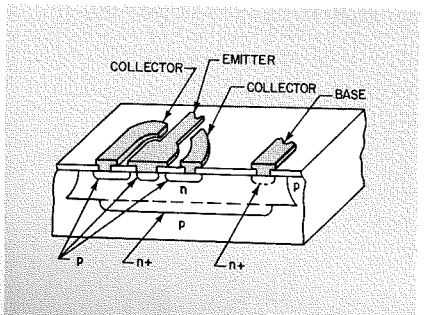

Fig. 5—Simplified cross-section of a P-N-P lateral transistor.

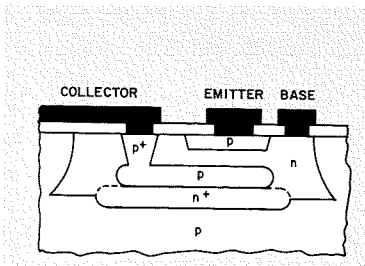

Fig. 6—A cross-section and typical characteristics of a P-N-P vertical transistor.

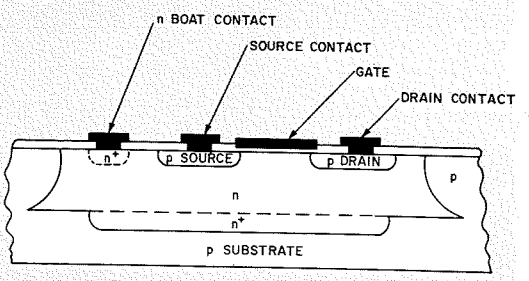

Fig. 7—Cross-section of a P-channel MOS transistor.

where D_P is the diffusion constant of holes in the base. Fig. 5 shows a cross-section of a P-N-P lateral transistor. Typical characteristics of a P-N-P transistor are as follows:

Breakdown voltage $V_{(BR)CEO}$
45 V at 0.5 mA
Static forward-current transfer ratio h_{FE}
20 at $I_C=0.5$ mA and $V_{CE}=5$ V
Current gain-bandwidth frequency f_T
2 GHz at $I_C=0.5$ mA and $V_{CE}=5$ V

P-N-P vertical transistors—The P-N-P vertical structures are employed where improved f_T and current-handling capability are required. Fig. 6 shows a cross section of a P-N-P vertical transistor. In these transistors, improved current handling capability occurs because useful minority-carrier injection takes place over the entire emitter area instead of only the emitter periphery. Base width of the P-N-P vertical transistor is controlled by epitaxial and diffusion technology. This condition results in tighter control and narrower base width (improved f_T) than is possible with the P-N-P lateral structure. The typical characteristics of a P-N-P vertical transistor are:

Current gain-bandwidth frequency f_T
30 MHz at $I_C=0.3$ mA and $V_{CE}=10$ V
Static forward-current transfer ratio h_{FE}
20 at $I_C=0.3$ mA and $V_{CE}=8$ V

P-N-P substrate transistor—In applications where the collector of a P-N-P transistor may be connected to the substrate, a P-N-P substrate transistor is used. This transistor is formed by omission of the N^+ pocket and the P collector diffusion for the P-N-P vertical structure. The P-N-P substrate transistor has the following typical characteristics:

Current gain-bandwidth frequency f_T
6 MHz at $I_C=0.3$ mA and $V_{CE}=3$ V
Static forward-current transfer ratio h_{FE}
20 at $I_C=0.3$ mA and $V_{CE}=3$ V

Super-beta transistors—Super-beta transistors are used in circuit applications where very high input impedance and low $1/f$ noise are required (e.g., operational amplifiers). These transistors are fabricated by use of techniques similar to those of standard N-P-N devices except the emitter depth is increased to provide beta levels an order of magnitude higher. As the emitter-junction depth is increased, the net acceptor atoms in the base-width region are greatly reduced. This effect increases the beta level and reduces the reach-through voltage. A typical super-beta device has a breakdown voltage $V_{(BR)CEO}$ of 3 volts and a beta of 1500 at 1μA collector current. In the application of this device, the collector-to-emitter voltage is clamped below the reach-through voltage.

P-Channel MOS transistors—The P-channel MOS transistors are used where high input and output impedances are required. Fig. 7 shows a cross-section of a P-channel MOS transistor. The fabrication of this device is compatible with the general-purpose N-P-N transistor. Source and drain are formed during base and resistor diffusion, and the channel-oxide is grown as a last oxidation step at the same time that MOS capacitors are fabricated. The important parameters that determine the characteristics of a P-channel MOS transistor are the drain current I_D and transconductance g_m.[3] The drain current I_D is expressed by

$$I_D=\frac{\varepsilon_{ox} W \mu (V_G-V_T)^2}{2 t_{ox} L} \qquad (4)$$

where ε_{ox} is the dielectric constant of

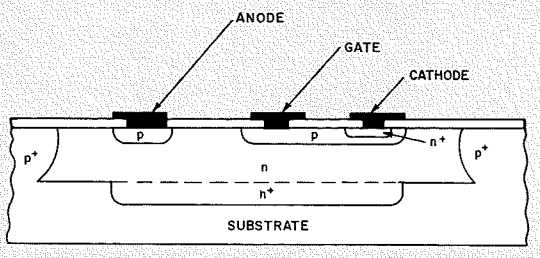

Fig. 8—Cross-section of a silicon-controlled rectifier.

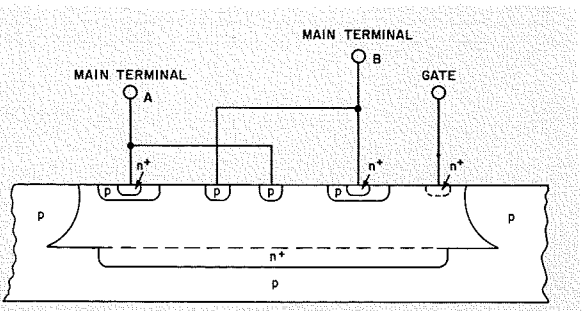

Fig. 9—Combined schematic and cross-section of a silicon bilateral switch.

the oxide; t_{ox} is the thickness of the oxide; W is the channel width; L is the channel length; V_G is the applied gate voltage; V_T is the threshold voltage; and μ is the effective mobility. Differentiation of Eq. 4 with respect to applied gate voltage V_G yields the transconductance g_m given by

$$g_m = \frac{\varepsilon_{ox} W \mu (V_G - V_T)_2}{t_{ox} L} \qquad (5)$$

Typical characteristics of a P-channel MOS transistor with channel-oxide thickness of 1000 angstroms and a channel width-to-length ratio of 60 are:

Breakdown drain-to-source voltage $V_{(BR)DS}$
35 V at $I_D = 1$ μA and $V_G = 0$ V

Threshold voltage V_T
1.7 V at $I_D = 1$ μA and $V_{DS} = 10$ V

Transconductance g_m
1000 micromhos at $I_D = 2$ mA and $V_{DS} = 10$ V

Control devices

Silicon controlled rectifier—The silicon controlled rectifier (SCR) is basically a four-layer structure that has useful current-switching characteristics. Fig. 8 shows the cross-section of an SCR. This device is formed by the connection of a P-N-P and an N-P-N transistor so that the two structures share collector and base regions. A typical monolithic SCR is formed by combination of a P-N-P lateral and an N-P-N vertical-transistor structure. For such a structure, it can be shown that the condition for turn-on is given by[4]

$$\beta_{P\text{-}N\text{-}P} \times \beta_{N\text{-}P\text{-}N} \geq 1 \qquad (5)$$

Normal integrated circuit technology results in $\beta_{P\text{-}N\text{-}P} \times \beta_{N\text{-}P\text{-}N} > 1$ down to extremely low current levels so that the junction leakage results in a normally ON condition. The SCR may be held OFF with a reverse biased gate-cathode junction by a shunt leakage path placed across the junction, or by design of low-beta structures. The typical characteristics of an SCR, with 100 ohms between the gate and the cathode, are:

Forward blocking voltage
75 V

Reverse blocking voltage
25 V

Forward drop anode to cathode
2.1 V at $I_A = 1$ A

Gate turn-on I_G
0.6 mA

Silicon-bilateral switch—The silicon-bilateral switch can be thought of as a parallel combination of two SCR's of opposite polarity. The device, therefore, displays the characteristics of a forward-operated SCR for either polarity of the main terminals. A cross-section and schematic representation of this device are shown in Fig. 9. The same methods are used to control the bilateral switch as those that control the switching characteristics of SCR's.

Unijunction devices—Unijunction devices are used as switches and relaxation oscillators.[5] These devices have properties whereby an OFF condition exists until a predetermined voltage is applied to the control electrode. Fig. 10 shows a cross-section of a typical unijunction device. If B_1 is at ground potential and a voltage is applied to B_2, a small current will flow that depends on the resistivity and dimensions of the N material. The resistance between B_1 and a point in the N material beneath the diffusion is R_{B_1}. The resistance between B_2 and the same point is R_{B_2}. The voltage V beneath the P-junction with respect to B_1 is given by

$$V = \eta V_{B_1B_2} \qquad (6)$$

where $V_{B_1B_2}$ is the voltage applied to B_2 and $\eta = R_{B_1}/R_{B_1} + R_{B_2}$. When the emitter-to-$B_1$ potential V_{BE_1} is raised to a level above V, sufficient to forward bias the diode, the emitter may inject minority carriers into the N region which are collected by B_1. The minority carriers result in conductivity modulation of the N region which reduces V_{EB_1} as the emitter current I_E increases. This controlled negative resistance characteristic makes the unijunction a useful device.

Resistors

Monolithic resistors are obtained by use of the bulk resistance of a defined volume of silicon. The resistance R is determined by

$$R = \rho_S L/W \qquad (7)$$

where ρ_S is the sheet resistance, L is the resistor length, and W is the resistor width.

There are several types of resistors available to the circuit designer. Some of these resistors are discussed in the following paragraphs.

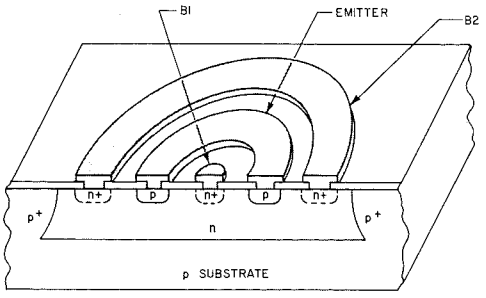

Fig. 10—Simplified cross-section of a unijunction transistor.

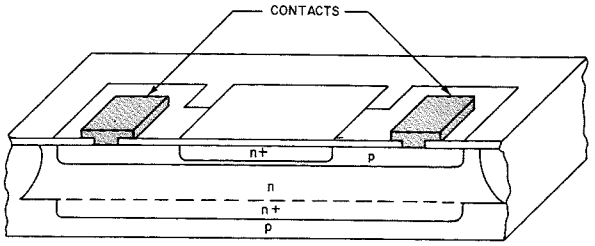

Fig. 11—Cross-section of a pinch resistor.

Base-diffusion resistor—This resistor is fabricated during base diffusion of the N-P-N transistor. The absolute value of the monolithic resistor is subject to wide variations because of the effect of processing on sheet resistance ρ_S, resistor length L, and resistor width W. However, because all resistors are fabricated at the same time, their ratios are tightly controlled. Because of this control, the monolithic circuit design is oriented toward resistor ratios rather than their absolute values. Typical characteristics of base-diffusion resistors are as follows:

Absolute value (5-kilohm resistor, 0.5 mil width)	±30%
Ratio (two 5-kilohm resistors, 0.5 mil width)	± 5%
Temperature coefficient T_C	2000 (PPM/°C)

Pinch resistors—A pinch resistor (shown in Fig. 11) is used to conserve area where high-value resistors are required. These resistors are formed with the high-conductivity surface of the base-diffusion resistor pinched-off with the emitter N^+ diffusion. The removal of the high-conductivity surface layer results in a thirty-fold increase in the sheet resistance. Typical characteristics of a pinch resistor are:

Sheet resistance ρ_S	6000 ohms per square at $\beta = 100$
Temperature coefficient T_C	5000 (PPM/°C)
Limiting breakdown voltage	7.0 $V_{(BR)}$

Super-pinch resistors are formed by use of the super-beta processing technique. Typical characteristics of the super-pinch resistor are as follows:

$\rho_S = 90{,}000$ ohms per square at
$\beta = 1500$
$V_{(BR)} = 2.0$ V

N-Boat Resistors—The N-boat resistors are defined by the P substrate and isolation diffusion. Sheet resistance of this layer is dependent on the resistivity of the epitaxial layer. Typical values for a 10-micrometer, 5-ohm-centimeter epitaxial layer are as follows:

$\rho_S = 5{,}000$ ohms per square
$T_C = 10^4$ PPM/°C.

An advantage of this resistor is improvement in breakdown voltage; its basic limitation is non-linearity with current.

N^+ and P^+ resistors—The N^+ and P^+ resistors are formed during the emitter and base P^+ diffusions, respectively. The sheet resistances are 3 and 20 ohms per square, which makes them particularly useful for low-value resistors and sub-surface interconnections. These resistors have excellent temperature-coefficient characteristics and high breakdown as follows:

Temperature coefficient T_C	<500 PPM/°C
Voltage breakdown $V_{(BR)}$	>50 V

Capacitors

MOS capacitors—The MOS capacitor is a parallel-plate capacitor that utilizes the N^+ diffusion as one plate, the aluminum metalization as the other plate, and the silicon dioxide as a dielectric. The basic characteristics of the MOS capacitor are defined by capacitance C and breakdown voltage $V_{(BR)}$. The capacitance C is given by

$$C = \varepsilon_{ox} A / t_{xo} \qquad (8)$$

where ε_{ox} is the dielectric constant of oxide, A is the area of capacitor, and t_{ox} is the oxide thickness. The breakdown voltage $V_{(BR)}$ is expressed as

$$V_{(BR)} = t_{ox} E_{max} \qquad (9)$$

where E_{max} is equal to 10^7 V/cm.

Junction capacitors—There are six basic junction capacitors used in monolithic circuits. The choice of capacitor to be used is dependent on breakdown voltage and capacitance per unit area. The following table is a summary of junction capacitors and their pertinent characteristics:

Capacitor $V_{(BR)}$	(volts)	*C/A (picofarads per square mil)*
N^+ to isolation	5.0	1.4 at 1 V
N^+ to base P^+	5.6	1.2 at 3 V
N^+ to base P	7.0	0.8 at 3 V
Isolation to N^+ pocket	9.0	0.48 at 3 V
Base to collector	50	0.08 at 3 V (1 ohm cm N-material)
Collector to isolation	100	0.05 (area) at 3 V 0.1 (periphery) at 3 V (1 ohm cm N-material)

Zener diodes

In applications that require a regulated supply or reference voltage an N^+-to-base-P^+ zener diode is used. On the other hand, where improved temperature coefficient of breakdown voltage is required, a compensated zener diode is used. The compensated zener is formed by the series connection of a forward-biased N^+-P diode with a zener. Important characteristics of the compensated and uncompensated zeners are listed as follows:

	Compensated zener	*Uncompensated zener*
$V_{(BR)}$	6.3 V	5.6 V
T_C at 5 mA	0.4 mV/°C	1.7 mV/°C
Dynamic impedance	35 ohms	15 ohms

Conclusion

This paper has shown that, today, the integrated-circuit designer has a large variety of components at his disposal that permit wide flexibility in circuit design. Active and passive components which can be fabricated with compatible processing provide the linear integrated circuits with a wide range of functional capability.

Acknowledgments

The authors thank P. Chiovarou, J. P. Keller, and L. Varettoni for the help in the preparation of material for this article.

References

1. Phillips, A. B., *Transistor Engineering* (McGraw Hill, 1962) p. 303.
2. Middlebrook, R. D., *An Introduction to Junction Transistor Theory*, (John Wiley & Sons, 1957) p. 144.
3. Hofstein and Heiman, *Silicon Insulated Gate Field Effect Transistor* (4th Edition, 1967) p. 8.
4. General Electric, *SCR Manual* (4th Edition, 1967) p. 8.
5. Trofimenkoff and Huff, "DC Theory of the Unijunction Transistor" (*International Journal of Electronics*, Vol. 20 (1966) p. 217.

A simplified bimetallic actuator for use in spacecraft thermal control

K. L. Schilling

This paper describes the design, development, and construction of two unique active thermal control systems for use on satellites. These designs were based on the controlled angular deflections of spiral-wound bimetallic actuators. The unique use of these actuators along with extremely lightweight louvers results in a virtually frictionless system which is very low in weight, simple in design, and low in cost. Also, both designs exhibit high reliability, good performance repeatability, and require no power from the spacecraft. The design philosophy and implementation are reviewed, along with the design tradeoffs and material selections for the two devices. A comprehensive test program is described and the results are presented in relation to the specified design goals.

CONTROL OF THE THERMAL ENVIRONMENT is extremely important for reliable operation of the various equipment and components of any spacecraft. Reliable passive techniques —such as the proper use of surface finishes, the optimum location of critical spacecraft components, and a choice of the orbit configuration—are available. However, passive thermal designs require larger tolerances in spacecraft nominal heat loads. Therefore, it is often desirable to have an active thermal control (ATC) system when narrower temperature ranges are required.

In general, ATC systems regulate spacecraft temperatures by using a louver, or series of louvers, which open or close in response to temperature changes, thereby varying the effective area of a designated radiating surface on the spacecraft (see Fig. 1). The thermal actuators described in this paper (Figs. 2 and 3) use spiral-wound bimetallic elements as thermal sensors and prime movers for the system.

Design considerations

Actuator design constraints

The thermal actuators for the ATC systems shown in Figs. 2 and 3 had to meet the following requirements:

1) Operating temperature range of 10 ±1°C;
2) Range selection from 12 to 22°C;
3) Over-temperature relief from 0 to 40°C;
4) Minimum weight;
5) Reliable operation in space for 18 months (equivalent to 8000 thermal cycles);
6) Linearity of system over the operating temperature range of ±10%;
7) Short development time; and
8) Design simplicity.

Reprint RE-16-3-1
Final manuscript received February 24, 1970.

Preliminary study

Other ATC design techniques or systems that were considered include:

1) Electrical heaters with thermostatic control;
2) Fluid actuators;
3) Two-phase actuators for louver operation;
4) Electro-mechanically operated louvers; and an
5) RCA-designed thermal switch.

Of the various systems considered, the heater system was ruled out due to lack of available power. The electro-mechanical system was rejected due to unnecessary complexity. The fluid and two-phase actuators were eliminated because of their complexity, lack of redundancy, and cost. Although the RCA thermal switch was an attractive possibility, it was eliminated due to the development lead-time required.

A trade-off study of the aforementioned systems established that a design utilizing the bimetallic-actuated louver concept offered several advantages:

1) Local temperature sensing would be provided;
2) No external power source would be required;
3) Virtually frictionless operation;
4) High reliability;
5) Simplicity of design and analysis;
6) Short development and qualification time; and
7) Weight advantage.

Fundamental design equations.

Eq. 1 (see also Fig. 4 and Legend) describes the angular deflection of a spiral wound bimetallic coil as:[1]

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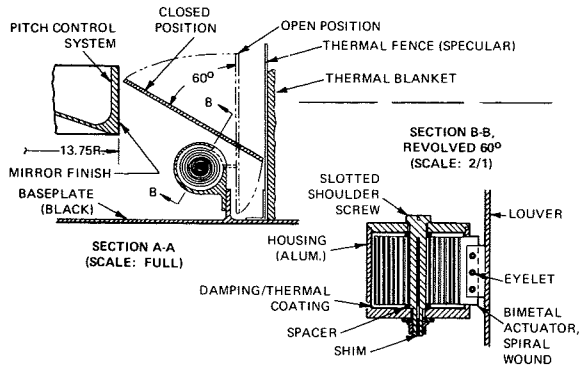
received the BSME from West Virginia University in May, 1967. He then joined RCA and participated in the Design and Development Training Program. In November 1967, he transferred to the Astro-Electronics Division as a member of the Spacecraft Design Group. On loan to the Environmental Test Group, he acted as Test Director during this interval. In June 1968, he was transferred back to the Spacecraft Design Group and participated in a classified program in the design and development of the active thermal controller of which the bimetallic actuators are a portion. His work on this program also included design of all heat shields, blankets, and the flywheel design for the attitude control system for the various spacecraft. Most recently, he was assigned as design engineer on a classified program.



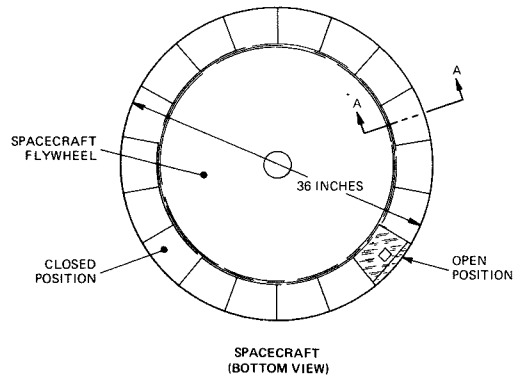
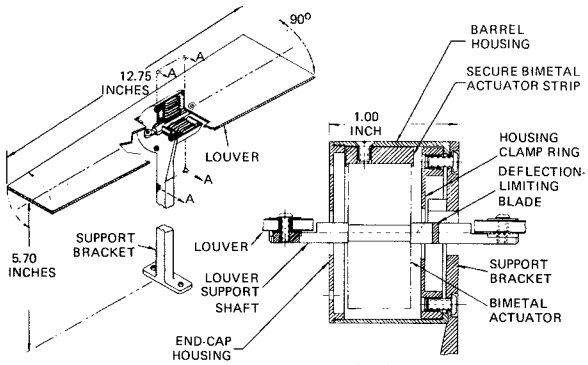


Fig. 1—Principle of operation of the active thermal control system.



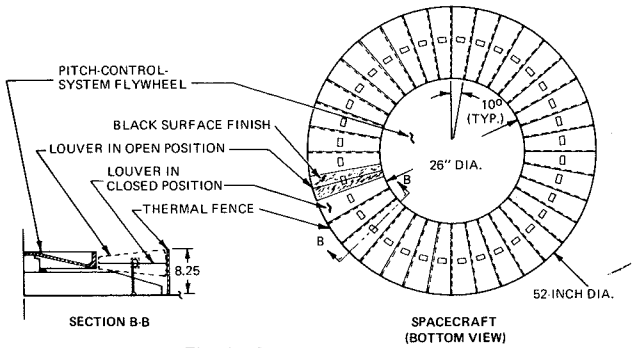


Fig. 2—Petal arrangement.

$$A=\frac{(K_{DC})\,(\Delta T)\,(L)\,(M)}{t},$$

when $P=0$, $m=1$. (1)

Since the bimetallic actuator was to be designed for zero gravity, the load, P, imposed on the actuator by the louver is negligible. "The specific deflection, m, is the ratio of the actual deflection, corresponding to a particular force and temperature change, to the free deflection for the same temperature change. This dimensionless ratio varies from 0.0 for the case of complete restraint to 1.0 for free deflection which is the case in this design."[1] Also from Ref. 1, the basic equation for stress is

$$S=\frac{3P(r+z)}{8\,bt^2}$$

Configuration and operational description

Figs. 2 and 3 show two ATC configurations. Both systems consist of groups of modules having rotating flaps that cover the spacecraft radiating area and are driven by spiral-wound bimetallic actuators. These bimetallic actuators are thermally coupled to the spacecraft. Each flap will, in the closed position, inhibit the thermal radiation from the desired region of the spacecraft; in the open position, the flap will allow maximum radiation (Fig. 1). The spacecraft temperatures are thus controlled by varying the A_ε (area x thermal emissivity) of the designated radiating area of the spacecraft as a function of temperature. The bimetallic actuators are essentially decoupled thermally from the louvers and the space environment. This allows the bimetallic actuators to respond only to a specific spacecraft reference temperature.

The ATC drive is direct, with no moving parts other than the actuator response to temperature variation. The bimetallic element (actuator) is encased in a lightweight aluminum housing, which thermally grounds the actuator to the spacecraft radiating surface and limits the actuator excursions during the vibratory exposures.

In both cases, thermal calibration is easily achieved. In the first approach (Fig. 2), calibration is accomplished by adjusting the support shaft to the appropriate temperature-louver orientation, and then securing the support shaft. In the second approach (Fig. 3), the clamp ring which secures the actuator barrel to the support bracket is loosened and the barrel rotated to obtain the appropriate louver/shaft orientation for the desired temperature level. Since both designs incorporate deflection limiting, over-temperature relief is accomplished by the actuator absorbing the energy of "winding-up" or "unwinding." Internal stresses sustained are negligible.

Design considerations and materials selection

The design concept in Fig. 2 prevents metal-to-metal contact by allowing adequate clearance between the bimetallic actuator and its housing. Careful control of the bimetal dimensions and the use of RTV on the housing deflection-limiting stops also precludes metal-to-metal contact. The design concept in Fig. 3 is dimensioned to assure that the louver support shaft will not touch the housing in a zero gravity environment and to avoid any operational metal-to-metal contact. Control of tolerances also assures that the deflection-limiting blade of the louver support shaft contacts only the mechanical stops.

Selection of bimetal actuators

The performance of a bimetal element depends upon the following factors:

1) Type of bimetal;
2) Length of strip;
3) Width of strip;
4) Thickness of strip;
5) Temperature change;
6) Magnitude of load;
7) Type of element used; and
8) Electrical resistivity.

Eq. 1 involves several variable factors. Thus, it is necessary to assume values from the specifications and the nature of the application in calculating thickness, width, or length of the strip. When the calculations indicate that the length of a straight strip would be excessive to meet mounting and containing requirements, then a U-shape or coil would be employed based on the available space for containment. In both designs, a very active coil (deflection versus temperature change) was required. Consequently, a bimetallic material with the highest possible coil deflection constant, K_{DC}, was chosen (Chace Mfg. #6650).[2] Also, in both cases the temperature change, ΔT, was the same: 10°C. Because of the zero gravity environment, the load is essentially negligible in both designs. With zero load on the bimetal, the width, b, of the element is not related to angular deflection, A; therefore, the width is chosen for design convenience, stress requirements, and stability.

Selection of actuator housing material

In both design concepts, aluminum was chosen as the basic housing material because of its strength, light weight, and thermal conduction properties. The design concept depicted in Fig. 2 requires a close thermal coupling to the spacecraft, and since the housing is completely shielded from space on the cold end (louver closed) the surface finish on the outside of the housing was left as bare aluminum with a polished finish. The resulting low emissivity does not cause any thermal unbalance on the hot end (louver open). Also, that portion of the bimetal which "sees" space is finished with gold. However, the design concept shown in Fig. 3 did not require as rigid a thermal coupling to the spacecraft. Also, the housing of the Fig. 3 design can "see" space all of the time, with louvers both open and closed. To help compensate for the thermal coupling, the support bracket was made from 6101-T6 because of its high thermal conductivity. In addition, all exterior surfaces of the bracket and actuator housing were polished to a specular finish and gold-vapor-deposited to obtain a very low thermal emissivity to reduce radiation heat losses.

Selection of louver (flap) material

The ATC louver has been designed for minimum weight and ease of fabrication. This low-mass louver minimizes the dynamic actuator loading and reduces the testing complication of static deflection of the actuator in a 1-g field. The basic louver is a sandwich structure composed of two 0.5-mil Kapton (aluminized H film) skins separated by a core spacer of low density polyurethane foam (1.7 lb/ft^3), held together by Bondmaster M773 adhesive. The typical louver shown in Fig. 2 weighs approximately 3 to 4 grams, while the louver shown in Fig. 3 weighs approximately 4 to 5 grams.

The polyurethane louver core is "Scott Industrial Foam" which is a fully "open-pore" (reticulated), flexible, polyester material with a 97% void volume, and high permeability. The foam used has a density of 100 pores/inch. It also has high chemical resistance, is not affected by moisture, and has unusual "memory" (when a sheet of this foam is crushed into a tight ball and then released, it returns to its original shape with no apparent damage, even after repeated exposures to this treatment). Also, because the foam is open pore, it easily releases any trapped air in a vacuum environment. Exposure to vibratory inputs has virtually no deleterious effects on the louver.

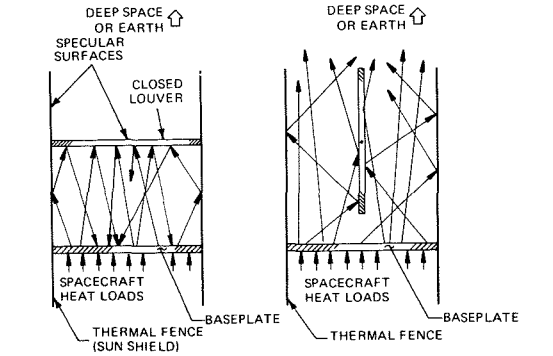
Testing and results

Testing of the ATC system was done on breadboard models which were similar to their respective flight model configurations in performance and operation.

The bulk of thermal testing was performed in vacuum chambers or bell jars, using electrical heaters to simulate spacecraft heat loads, thermocouples to monitor spacecraft and ATC temperatures, and electrical sensors to verify louver open and closed positions. The thermal testing verified that the louvers operated from full open to full closed over the required temperature range; established that the required change in A_ϵ vs. change in spacecraft temperature was met; and monitored thermal gradients between louver, actuator, actuator support housing, and the spacecraft radiating surface.

A life-test was performed on a bimetal actuator typical of the one used in the design configuration shown in Fig. 2. The actuator was thermally cycled between 28.5 and 46°C for a total of 8000 cycles, representing 18.5 months of mission time. This temperature span is 7.5°C greater than the normal operating range of the ATC system. The actuator angular movement was constrained to 60 angular degrees which is the same as for the flight configuration. No detectable change was noted in the actuator characteristics or in the calibration and angular position of the actuator throughout this test.

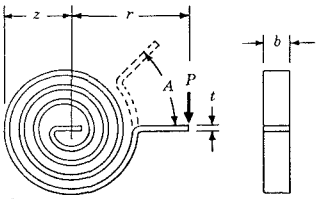
Breadboard models were subjected to vibratory exposures for three axes of testing: sine vibration of 15g from 7 to 2000 Hz, at 2 oct/min; and random vibration of 35.9g (RMS), flat spectrum within ± 3 dB (2 minutes) from 20 to 200 Hz. The units tested successfully withstood all of the vibration tests, and no change in thermal calibration occurred. Magnetic and antenna testing indicated no significant problems with either design configuration.



(a) LOUVER CLOSED. EMITTED THERMAL ENERGY REFLECTED AND ABSORBED

(b) LOUVER OPEN. EMITTED THERMAL ENERGY REFLECTED INTO SPACE

Fig. 3—Venetian-blind arrangement of louver modules.



Legend
S = Stress (lb-f/in^2 or psi).
A = Angular deflection (degrees).
K_{DC} = Coil deflection constant.
ΔT = Temperature change (degrees Fahrenheit).
L = Active length of element (inches).
m = Specific deflection.
t = Thickness of element (inches).
P = Load or force (ounces).
b = Width of element (inches).
r = Radius to point of load application (inches).
z = Mean radius of outer turn of spiral (inches).

Fig. 4—Spiral coil.

Conclusions

Basically, the developmental effort produced a practical flight hardware design (Figs. 2 and 3) which proved the feasibility of employing spiral-wound bimetallic actuators as thermal sensors and prime movers for thermal control systems. Such devices are particularly suited to applications where low weight, low cost, and high reliability are required, and where the consumption of electrical power is not permitted. Also, future growth potential is easily achieved by:

1) Increasing the size of the area to be controlled;
2) Minimizing the weight, size, and quantity of actuators; and
3) Maximizing louver size (area).

Acknowledgment

The author acknowledges the contributions of David Nelson, Aerospace Corporation, who is responsible for the original concept of employing bimetallics for the support and activation of lightweight louvers for spacecraft thermal control.

References

1. Chace Co., W. M., *Design Catalog*, pp. 28 and 37.
2. Chace Co., W. M., *Design Catalog*, p. 24.

High-power L- and S-band epitaxial *GaAs* transferred electron oscillators

B. E. Berson | Dr. R. E. Enstrom | Dr. J. F. Reynolds

High-power, high-efficiency transferred-electron oscillators have been developed in both L- and S-band. Output powers of 200 watts and efficiencies greater than 29% have been obtained in both bands. These devices are capable of stable operation over wide temperature ranges and at high duty cycles which make them applicable for many microwave system applications.

THE RECENT DISCOVERY of microwave avalanche diodes and of the transferred-electron effect in gallium arsenide has profound implications for microwave engineering. Solid-state devices are now available with peak power outputs which previously could be obtained only with tubes. As a result, the benefits of solid-state reliability can be brought to high-power microwave systems. In addition, these devices, because of their unique properties, are making new classes of microwave systems possible.

At the David Sarnoff Research Center, the Advanced Technology Laboratory and the Materials Research Laboratory are carrying out research aimed at producing high-power, high-efficiency L- and S-band transferred electron oscillators (TEO's). These studies have resulted in output powers of 200 watts or more and efficiencies greater than 29% in both L- and S-band. These conversion efficiencies are the highest reported to date for TEO's. Present research efforts are directed toward developing the gallium arsenide materials technology, the device fabrication technology to fabricate these devices reproducibly, and the microwave circuit technology to utilize them. This paper describes the progress to date in these areas and in particular toward a goal of a 1-kW L-band oscillator for use in IFF transponder applications.

Design factors

It is useful to begin by considering some of the factors which are important in achieving high-efficiency and thus high-power operation of TEO's. The detailed physics of the transferred-electron effect has been described previously.[1] The basic structure of a TEO, as shown in Fig. 1, consists of an N-type gallium arsenide active region sandwiched between N^+ *GaAs* layers to which metallic ohmic contacts are made. The *I-V* characteristics of such a device is shown in Fig. 2. For voltages below the threshold voltage, V_{TH}, the device is passive and has a positive resistance. Above V_{TH}, the device exhibits a negative resistance because the current decreases as the bias voltage is increased. There are two basic classes of operation for this device: those associated with the presence of high field domains and those without the high field domains.

In the domain modes of operation, the negative resistance of the device causes the formation of high electric-field domains which nucleate at the cathode and travel across the sample. The mechanism of domain formation and the relationship between the domain transit time and the operating frequency determine which of the various domain modes is involved. In the limited-space-charge-accumulation (LSA) mode, the time during which the sample is in the negative-resistance region is sufficiently less than the growth time of the domain and, as a result, no domain forms. Table I summarizes the properties of some of the modes of operation of a transferred-electron oscillator. The following discussions are concerned primarily with domain modes.

If the device is biased in the negative-resistance region at a voltage V_B with a current I_B (Fig. 2) and properly loaded with an rf circuit, microwave power can be extracted. The input power is $V_B I_B$, and the output power is proportional to $\Delta V\ \Delta I$, the product of the RF voltage and currents. The operating efficiency is then equal to $K\Delta V\Delta I/V_B I_B$ (x 100%), where K is a constant of proportionality. The quantities ΔV and ΔI are determined primarily by the properties of the material and the bias voltage. The constant of proportionality, K, however, is determined to a large extent by the voltage and current wave-shapes. Therefore, the device efficiency is highly dependent on the harmonic content of the voltage and current waveforms of the device.

The above expression for efficiency indicates that it is desirable for the fundamental voltage and current swing to be as large as possible. If the

Table I—Some modes of operation of a transferred-electron oscillator.

Mode	*Relationship between operating frequency (f_0) and domain transit time (T_0)*	*Domain quenching mechanism*
Transit time	$f_0 \sim 1/T_0$	Reaches anode
Quenched domain	$f_0 > 1/T_0$	RF field
Delayed domain	$f_0 < 1/T_0$	Reaches anode or RF field
LSA	$2\times10^4 \leq n^*/f_0 \leq 2\times10^5$	No domain

* n=sample doping density (cm^{-3})

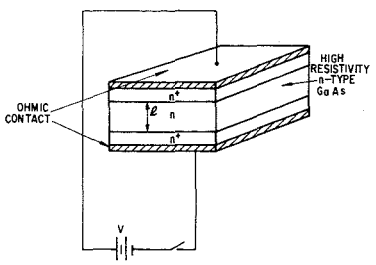


Fig. 1—Basic transferred-electron device.

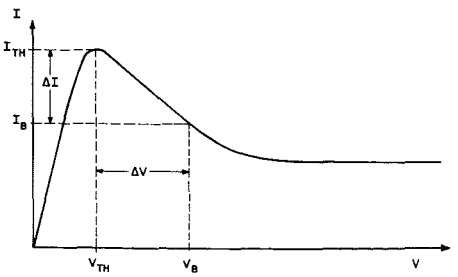


Fig. 2—Typical current-voltage characteristic of TEO.

Reprint RE-16-3 (ST-4117)
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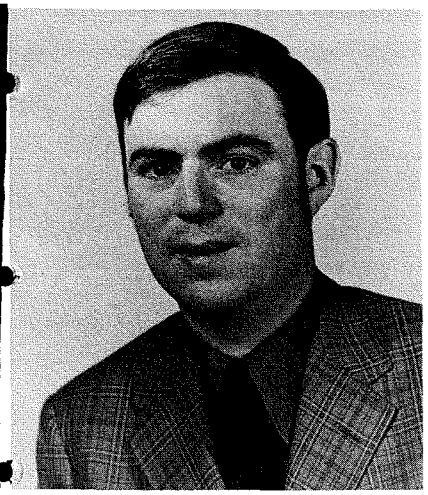
This work was supported by the U.S. Air Force Avionics Laboratory under Contract No. F33615-67-C-1981 and RCA Laboratories, Princeton, N.J.



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received the BEE from City College, New York, in 1960; and the Master of Science from the College of Engineering, University of Rochester, New York, in 1963. He has had additional schooling at the University of Rochester, UCLA Extension, Mt. San Antonio Junior College, and the Newark College of Engineering. From 1962 to 1966 he was a Senior Physicist with General Dynamics in Pomona, California. While with General Dynamics he was involved in research in the areas of thin films and thin-film microelectronics, organic semiconductors, and plasma oscillations in indium antimonide. Since joining the RCA Advanced Technology Laboratory, Mr. Berson has been engaged in work on silicon and GaAs microwave devices. In 1968 Mr. Benson received an RCA Laboratories Achievement Award for his research on transferred electron oscillators. Mr. Berson is currently leader of a group pursuing research on bulk microwave oscillators. He is a member of the IEEE and the American Physical Society.

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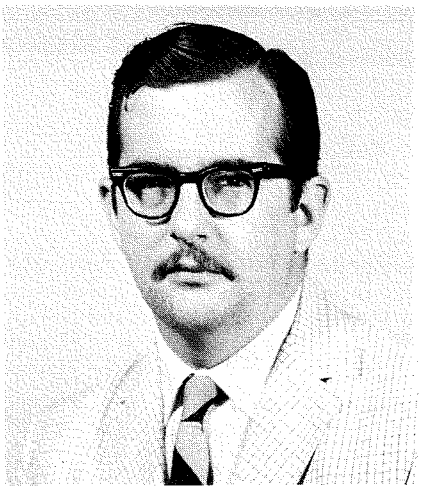

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received the BEE, MEE and PhD from Rensselaer Polytechnic Institute in 1964, 1965, and 1967, respectively. His doctoral thesis investigated methods of stabilizing gaseous magneto-plasmas by controlling the magnetic field geometry. His earlier graduate research was concerned with the use of microwave techniques for plasma diagnostics. He has publications in both areas. Since joining the RCA Advanced Technology Laboratory in 1967, Dr. Reynolds has been engaged in work on silicon and GaAs active microwave devices. In 1968, he received an RCA Laboratories Achievement Award for his research on Transferred Electron Oscillators and has several publications in this area. Dr. Reynolds is an associate member of Sigma Xi.

RF swings into the positive-resistance region, however, dissipation occurs. With the aid of harmonics, total RF waveforms can be generated which swing only slightly into the positive-resistance region but allow a much larger excursion at the fundamental frequency. In the case of the square-wave, for example, the fundamental amplitude is $4/\pi$ times that of the total waveform.

The ratio of the bias voltage to the device threshold voltage can affect the efficiency in a number of ways. First, increasing the bias voltage increases the allowable RF voltage and current swings. Second, over a large portion of the *I-V* characteristic, the DC input current of a TEO decreases as the bias voltage increases. This effect can lead to an increase in efficiency.

The product of the sample-doping density (n) and active layer length (L) has a profound effect on sample operating dynamics and efficiency because it affects both the domain growth dynamics and maximum domain size. Experimental results indicate that optimum operating efficiency occurs at an nL product of approximately $5 \times 10^{12}\text{cm}^{-2}$. Thus, a 100-$\mu$-thick L-band TEO should have a uniform carrier concentration of $5 \times 10^{14}\text{cm}^{-3}$.

In addition to the general device physics, it is also important to consider anomalies which can occur in samples. Of particular importance are fluctuations in the doping concentration in the active region of the TEO. Copeland[2] has shown analytically that a 20% variation in the carrier concentration of the active layer can reduce the efficiency of LSA oscillators from 17% to 12%. If doping fluctuations become large enough, they can cause nucleation of domains at locations other than the N^+-N-cathode interface. This effect, in turn, can lead to lower efficiency, an anomolous frequency of operation, and premature sample breakdown.

The nature of the contact-active layer interface is also important. It should be free from spurious layers which reduce efficiency and can cause premature breakdown. Although the exact nature of the interface for optimum device performance is not yet known, controlling the doping profile in the regions where the high field domains form and collapse should make it possible to shape the current waveform and thereby improve the efficiency.

Epitaxial gallium arsenide growth technology

The basic device structures are grown in the form of N^+-N-N^+ epitaxial *GaAs* wafer sandwiches[3] by the arsine vapor-growth process.[4] The N^+ layers form the ohmic contacts to the active N-layer, as shown in Fig. 1, and in turn, good metallic contact can be made to these N^+-layers. The entire structure is grown in a single operation without the sample being removed from the apparatus during

growth. The principles of the growth method can be outlined briefly with reference to Fig. 3. At one end of a 1-inch-diameter quartz tube, high-purity *HCl* reacts with 99.9999% pure *Ga* to form *GaCl*. The *GaCl* is carried by high-purity, palladium-diffused hydrogen to the deposition zone at the other end of the tube which contains the substrate. Simultaneously, semiconductor-grade AsH_3 flows into the tube and dissociates into H_2 and arsenic vapor, which reacts with *GaCl* in the deposition zone. The *GaAs* thus formed grows epitaxially on the *GaAs* substrate. The N^+-layer is prepared by doping during growth with gaseous selenium (from H_2Se to about $3x10^{18}$ electrons/cm^3.

The N^+-N-N^+ multilayer structure is grown on a chemically polished, <100> oriented, high-conductivity *GaAs* substrate having a carrier concentration of about $1x10^{18}$ electrons/cm^3. This substrate must be of high quality and is typically about 3 cm^2 in area. In general, it appears that *Te*-doped N^+-substrates are preferable to *Si*-doped N^+-substrates. The use of the latter frequently results in high-resistance layers about 3 microns thick at the N^+ substrate-N layer interface. These layers can cause non-ohmic contacts which impair efficient device operation. The active N-layer is grown about 100 microns thick to achieve operation at 1 GHz.

An active N-layer of very high purity is desirable for high-power TEO's so that high-resistivity material with the proper *nL* product and with a positive temperature coefficient of resistivity can be attained without sacrifice of electron mobility. A reduced mobility can increase the threshold voltage (V_{TH}) and thus lead to decreased efficiency. The positive temperature coefficient of resistivity is necessary for high-ambient-temperature and high-duty-cycle operation of devices. The required purity level must also be attained in a reproducible manner. This requirement can be extremely difficult because the impurity concentration is of the order of 10 parts per billion ($5x10^{14}cm^{-3}$). In the present program, the effects of the purity of the AsH_3, the condition of the quartz reaction tube, and the *As/Ga* ratio in the gaseous ambient on the purity of the grown layers have been investigated. By use of the best combination of these variables, it has been possible to attain carrier concentrations as low as $9x10^{13}cm^{-3}$, and mobility values as high as 8700 cm^2/v-sec at 300°K and 108,000 cm^2/v-sec at 77°K as determined by Hall-effect measurements.

The nature of the N-N^+ interfaces is also important in device operation. Capacitance-voltage measurements on Schottky barrier diodes have been made to derive the carrier-concentration profile at the N^+-N interfaces. It has been found that the carrier-concentration profile in the vapor-grown layers changes within a distance of 1 to 3 microns from the $10^{15}cm^{-3}$ to $10^{18}cm^{-3}$ range. This result indicates that rather abrupt transitions have been successfully achieved. Also, both the top and the bottom vapor-grown N^+-N interfaces have been found to have similar carrier profiles.[5]

Although the Hall-effect measurements and the capacitance-voltage measurements provide information on the quality of the material and the effect of process variables on the carrier concentration, carrier profile, and mobility, they can not indicate *a priori* which wafers will yield high power devices. The best test of the material devised to date is the microwave evaluation of completed devices. This evaluation indicates that subtle differences which do not show up in the other measurements are responsible for variations in device performance. The main effort has focused, therefore, on the preparation of N^+-N-N^+ wafers under a wide variety of experimental growth conditions and on the testing of these samples as devices. Devices have been successfully prepared with the highest DC-to-RF conversion efficiencies achieved anywhere.[6] Results to date suggest that wafers yielding high-efficiency devices can be grown only when good AsH_3, good *HCl*, good substrates, and good growth conditions are used *simultaneously*. In this way we have been able to achieve devices with efficiencies greater than 15% in seven out of 10 growth runs.

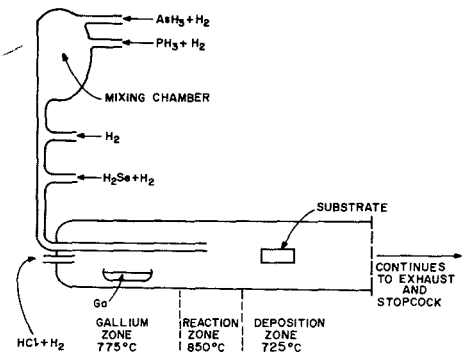


Fig. 3—Schematic representation of vapor-deposition apparatus.

Device fabrication technology

The device fabrication technology developed is suitable for the fabrication of multi-chip oscillators for high-power, high-ambient-temperature operation. The multi-chip approach has several distinct advantages over the use of one large-area device. The most important of these advantages is yield. If enough extra chips are incorporated in a package to allow for failures, the final packaged device yield can be 100%. Second, the multi-chip approach offers heat-sink advantages by spreading the thermal dissipation over a larger area. This feature is extremely important in high-power applications.

In the fabrication of devices, the N^+ substrate is first lapped to the desired thickness. Silver is then deposited on the top N^+ epitaxial layer and the wafer is wire sawn into chips of the desired size. The chips are cleaned and then alloyed into a specially prepared V5000 varactor package. Gold straps are thermo-compression bonded onto the devices and the package flange. Fig. 4 illustrates a four-chip TEO at this stage in the process. Finally, the device is carefully cleaned and the surface is passivated.

RF circuit technology

A cavity has been developed for high-power device operation. The device is mounted at the end of the shorted line

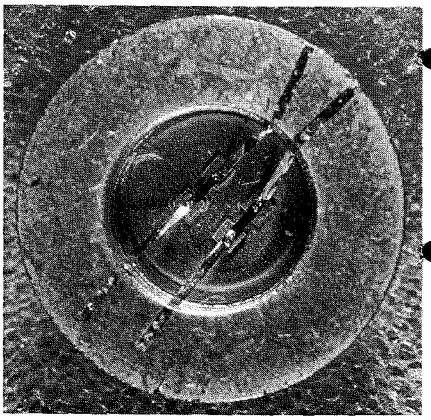


Fig. 4—Multi-chip TEO.

of the cavity. The output is loop-coupled with a high-Q variable capacitor and a tuning screw in the output circuit for matching the device directly into a 50-Ω load. The circuit is illustrated schematically in Fig. 5.

The design criterion employed involves resonating the device capacitance with the inductance of the shorted coaxial line of the cavity at the desired operating frequency. The desired resonance is accomplished for a wide range of devices by means of the replaceable inner conductor of the cavity. By simply changing the dimensions of this inner conductor, the impedance presented to the device is changed. An additional tuning screw in the cavity provides fine frequency adjustment once the basic geometry is set. This tuning screw also serves another function by providing tuning at the second harmonic. As discussed previously, the impedance presented to the device at the harmonics strongly affects the operating efficiency. When the device is tuned for maximum power output in this circuit, the loading at the second harmonic is primarily inductive with very little resistive loading. A picture of an L-band cavity is shown in Fig. 6. The height is 1¼" and the diameter is 1-½" with the additional side arm extending another ½".

Oscillator characteristics and performance

For operation in L-band, the N-layer thickness (L) of the TEO's is nominally 70 to 100 microns with a carrier concentration (n) of 3 to $8\times10^{14}cm^{-3}$ The highest-efficiency operation has been obtained with devices having an nL product between 4 and $6x10^{12}cm^{-2}$. With these devices, the threshold voltage for the onset of oscillations is between 20 and 30 volts. To optimize device performance, the DC bias point should be as far above threshold as possible for the reasons previously discussed. This point is usually about 4 to 5 times the threshold voltage, or approximately 100 volts for most devices tested. Fig. 7 shows the variation of power density with bias voltage for a large number of devices. There is no clear peak in the curve, and the power appears to rise with increasing bias over the range shown.

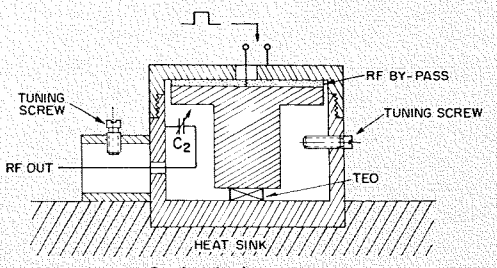
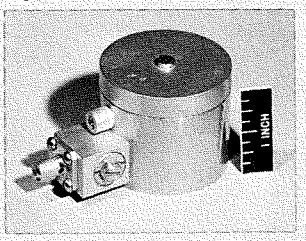


Fig. 5—Cavity design.

Fig. 6—Cavity design.



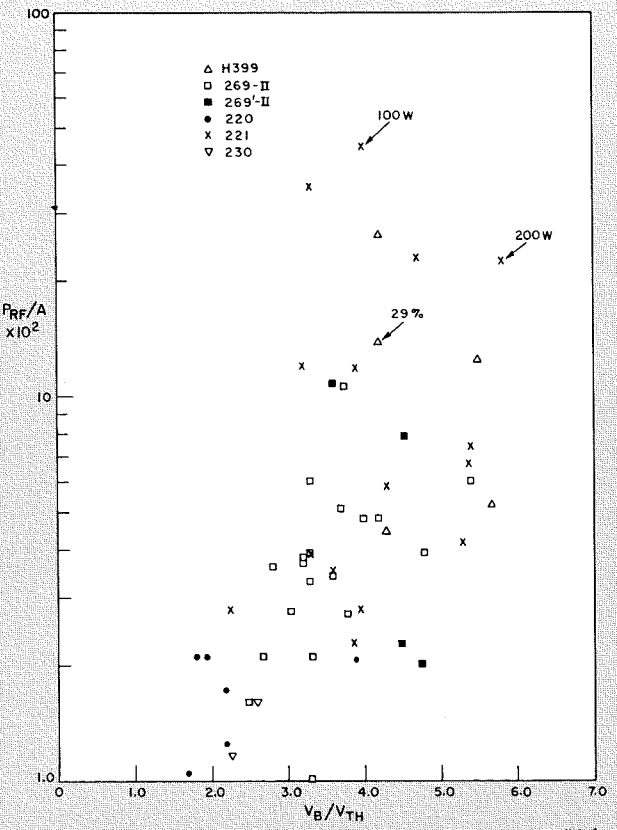


Fig. 7—Power density as a function of ratio of bias voltage (V_B) to threshold voltage (V_{TH}).

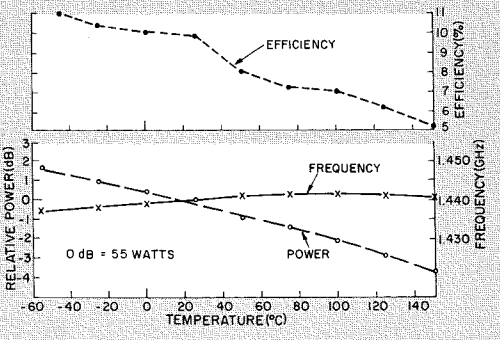


Fig. 8—Temperature characteristics of multi-chip TEO.

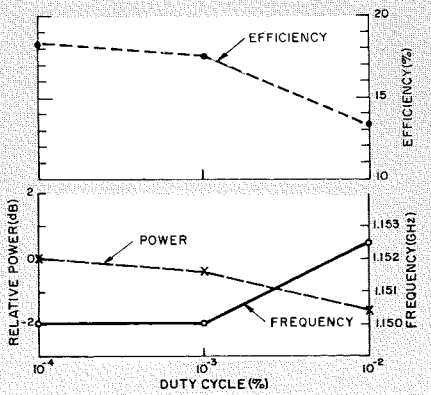


Fig. 9—Duty-cycle characteristics of multi-chip TEO.

As discussed in a previous section, high-power devices are made by paralleling many chips in one package. This operation has been successful for paralleling as many as five chips at one time. These multi-chip oscillators are indistinguishable from single-chip oscillators in terms of RF performance. The fact that the RF spectrum is as clean as that obtained from a single oscillator indicates that all oscillators are locked together. The power spectrum obtained from these devices usually follows the $\sin^2 x/x^2$ relationship expected for pulsed operation. Normal operation is with 0.5-μs-wide pulses at duty cycles up to 1%. Considerably longer pulse lengths and higher duty cycles have been demonstrated as well as operation in pulse bursts.

The yield of L-band TEO chips has now reached the point where devices with power outputs of 100 watts are readily fabricated.[7] The DC-to-RF conversion efficiencies of these devices generally range from 10% to 15%. A more recent wafer had a 50% yield of devices with efficiencies between 15% and 20%. Three devices fabricated from this wafer had efficiencies in excess of 30%, the highest being 32.2% for a single-chip device that produced 117 watts at 1090 MHz. This value represents the highest efficiency reported for any TEO. These results indicate that, as material properties improve, efficiencies of the order of 30% will be regularly possible.

Table II—Results obtained for single and multi-chip oscillators in L- and S-band.

Number of chips in device	*Power (W)*	*Frequency (GHz)*	*Efficiency (%)*
1	117	1.09	32.2
1	160	1.06	30.9
1	120	1.00	30.0
1	200	3.05	29
1	55	1.50	27.7
3	220	1.09	23.2
4	180	1.00	25
3	120	1.10	20.6
2	120	1.10	20
2	100	3.1	27

Table II gives a summary of some results for both single- and multi-chip oscillators in L- and S-band. The highest power obtained thus far is 220 watts with 23.2% efficiency from a device with three chips in parallel. Although the work on S-band TEO's has been far less extensive than that on L-band devices, output powers as high as 200 watts and an efficiency of 29% have been achieved. The results in this table indicated that high-power devices are readily fabricated by simply paralleling smaller chips.

Stability

In many practical microwave applications, the question of environmental stability is an important one. RCA's epitaxial *GaAs* is particularly suited to operation over a wide temperature range because it possesses a positive temperature coefficient of resistance. Thus devices fabricated from this material are not subject to thermal runaway, and merely turn off if the ambient temperature or internal heating becomes too high. Pulsed devices have been operated at ambient temperatures as high as +180°C and as low as −195°C (i.e. immersed in liquid nitrogen). The electron mobility increases and the threshold voltage decreases with decreasing temperature. The operating efficiency is therefore higher at liquid-nitrogen temperature than at room temperature.

Fig. 8 shows the operating characteristics of a multi-chip TEO over the ambient temperature range from −55°C to +150°C. The device was mounted in a V7000 varactor package and tuned in a reentrant cavity. The power output was 50 watts at 1.440 GHz with 9.8% efficiency. The overall power changes was 5.5 dB (+1.5 to −4 dB), the frequency shift was less than 5 MHz (−3 MHz to +1.5 MHz), and the efficiency varied from 11% to 5.2%.

To determine the effect of internal heating, duty-cycle tests were run on a 55-watt TEO. The results of the test are shown in Fig. 9. The power drops by only 1.6 dB over a duty-cycle range from 0.01% to 1%, and the frequency changes by only 2.5 MHz. The change in power is accompanied by a drop in efficiency from 18.3% to 13.4%. Even better results should be possible as further improvements are made in heat-sink-technology.

Life tests

Preliminary life tests have shown no evidence of either rapid or slow degradation. Several pulsed devices have been operated for 5000 hours with stable output, and Dr. S. Y. Narayan of our laboratory has operated a cw X-band device for over 13,000 hours with stable output.

Conclusion

To date, peak power output levels up to 220 watts and efficiencies up to 32% have been successfully achieved from GaAs transferred-electron oscillators. These results have been achieved through a series of material and device technology improvements. The devices have also demonstrated long life plus stable operation over a wide range of temperature and duty cycle. These characteristics have proven that TEO's are already highly useful devices. The performance levels described in this paper are already more than adequate to replace tubes in microwave systems, such as IFF transponders, phased-array radars, and military and commercial communication systems in general. In addition, they have made possible new, lightweight, portable versions of such systems. As new performance levels are reached, these devices will become applicable to many other high-power microwave systems.

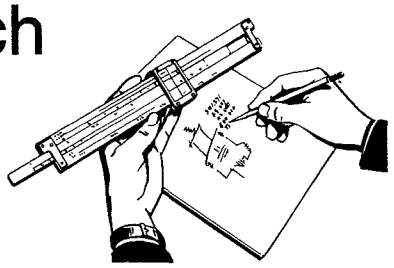
Acknowledgments

The authors thank J. Appert for assistance in preparing the epitaxial material; S. Dolochycki, E. McDermott, and V. Lawson for assistance in the preparation and testing of devices; and Dr. F. Sterzer for many helpful and stimulating discussions.

References

1. Sterzer, F., "Microwave Solid State Power Sources", *Microwave Journal* Vol. 11 (1968) p. 67; *RCA Engineer*, Vol. 14, No. 3 (1968) p. 74.
2. Copeland, J. A., "Doping Uniformity and Geometry of LSA Oscillator Diodes", *IEEE Trans. Electron Devices* Vol. ED-14 (1967) p. 497.
3. Enstrom, R. E., and Peterson, C. C., "Vapor-Phase Growth and Properties of GaAs Gunn Devices", *Trans. Metall. Soc. AIME* Vol. 239 (1967) p. 413.
4. Tietjen, J. J., and Amick, J. A., "The Preparation and Properties of Vapor Deposited Epitaxial $GaAs_{1-x}P_x$ Using Arsine and Phosphine", *J. Electrochem Soc.* Vol. 113 (1966) p. 724.
5. Berson, B. E., Enstrom, R. E., Reynolds, J. F., "High Power L- and S-Band Transferred Electron Oscillators", *RCA Review* Vol. 31, No. 20 (1970).
6. Reynolds, J. F., Berson, B. E., Enstrom, R. E., "High-Efficiency Operation of Transferred Electron Oscillators", *Proc. of IEEE* (9/69).
7. Berson, B. E., Enstrom, R. E., and Reynolds, J. F., "100 Watt L-Band Transferred Electron Oscillators for Transponder Applications", *NEREM Record*, Vol. 10 (1968) p. 940.

Engineering and Research Notes



Brief Technical Papers of Current Interest

Luminescent properties of GaN

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Reprint RE-16-3-22 | Final manuscript received April 11, 1970.

To the best of our knowledge, this is the first report of luminescence measurements on large undoped single-crystal gallium-nitride. Earlier measurements of luminescence in *GaN* were performed on doped needle-shaped crystals[1], while measurements on undoped *GaN* were performed on powdered *GaN*.[2]

The *GaN* used in the present study was obtained by epitaxial growth on sapphire substrates using vapor phase transport.[3] The gallium is transported as a chloride by reacting it with *HCl* while the nitrogen is obtained from NH_3. The resulting material is a colorless single crystal with the Wurtzite structure and a direct gap of about 3.39 eV at room temperature. The undoped material is N-type with an electron concentration of at least 10^{19} cm^{-3}.

The luminescence of *GaN* was excited either by bombardment with a 20 keV electron beam or optically with an ultraviolet laser emitting up to 2 mW at 3250 Å.[4] The emission was measured in the range of 3.7 to 1.1 eV, the lower limit being set by the cut-off of our lower range detector (an RCA 7102 photomultiplier). For photoluminescence, the sample was mounted on the cold finger of a Janis cryostat.

The most frequent emission peaks obtained by cathodoluminescence in a variety of crystals were found at 3.7, 3.5, 3.4, 3.27, 3.19, 2.88, 2.5, 2.2, 1.7 and 1.3 eV. Sharp lines (instrument limited) were observed at 1.78 eV in six samples and at 1.18 eV in four specimen. Some of these crystals were undoped while others were doped with either *Si, Ge, Sn, Mg, or Zn*. There was no strong systematic correlation between peak position and doping except that *Si, Ge,* and *Sn* always contributed a peak at 3.4 eV. Most of the samples emitted at 1.7 and 1.3 eV in addition to several higher energy peaks.

In photoluminescence, some *GaN* specimen emit only the near-gap peak at about 3.5 eV (at low temperatures) and, in other samples, broad peaks at lower photon energies. The reduced number of peaks obtained by optical excitation may be due to the lower intensity of the ultraviolet beam compared to that of the electron beam and also possibly to the more restricted range of states that can be pumped optically.

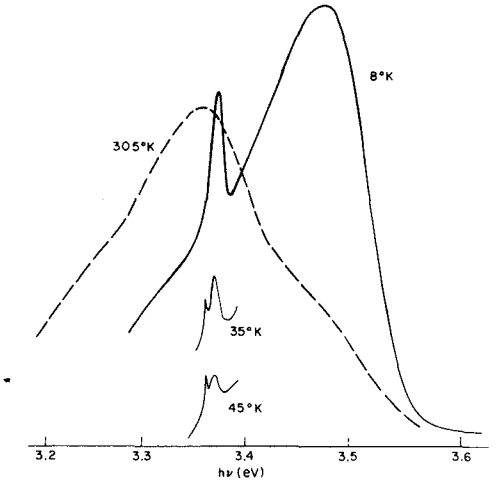

Fig. 1—Emission spectra of GaN under optical excitation at various temperatures. The 35 and 45°K data have been translated vertically for clarity.

Fig. 1 shows the photoluminescence spectra for an undoped crystal of *GaN*. At low temperature, the emission consists of a dominant peak at 3.477 eV which is 150 meV wide at half maximum. A weaker but sharper peak occurs at 3.37 eV which, at about 35°K and at higher resolution, can be separated into two narrow lines 10 meV apart. This doublet is strongly and strangely temperature dependent: the intensity of the doublet decays with increasing temperature above about 30°K; however, the higher energy peaklet which dominates at lower temperatures decays more rapidly than the lower energy peaklet. A semilogarithmic plot of the relative intensity of the peak at 3.37 eV normalized to that of the 3.48 eV peak vs. the reciprocal temperature gives an activation energy of about 11 meV for the decay of the complex (possibly a bound exciton) responsible for the doublet.

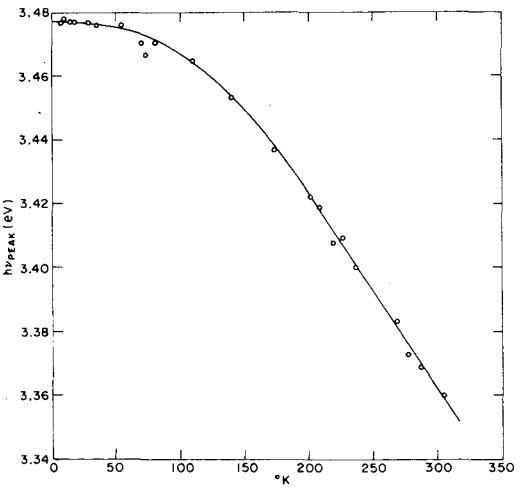

Fig. 2—Temperature dependence of the dominant emission peak in GaN.

The temperature dependence of the emission spectrum was measured from 2°K to room temperature. The spectral shift of the main peak is shown in Fig. 2. If, as in most semiconductors, the near gap emission follows temperature dependence of the energy gap, one can deduce a tentative value for the temperature dependence of the energy gap: $dE_g/dT = 6.0 \times 10^{-4}$ eV/°K in the linear range above 180°K.

The intensity of the near gap emission peak is nearly constant up to about 50°K and then decreases with increasing temperature, indicating the onset of a competing non-radiative recombination process. From a semilogarithmic plot of the emission intensity at the main peak vs. the reciprocal temperature one finds that the non-radiative process has an activation energy of about 21 meV.

At 77°K, the luminescence intensity varies linearly with the excitation rate over three orders of magnitude, suggesting that the radiative recombination is very efficient. An estimate of the emission efficiency was made. This estimate required several assumptions:

1) That the emission is isotropic—in this case the external quantum efficiency (ratio of photons emitted per incident photon) was about 0.5% at 300°K and about 5% at 77°K; 2) That total internal reflection could take place in spite of the rough surface of the epitaxial layer—the rough surface consisted of many-faceted hillocks which in the far field pattern showed specular reflection of the incident beam. With this assumption of possible light trapping by total internal reflection, a correction factor of at most 25X was obtained on the basis of a refractive index of $n=2.397$.[5] Note that this correction factor is more than sufficient to make the internal quantum efficiency 100% at low temperature. Since the exciting wavelength (0.325μ) is very close to the emission wavelength (0.36μ), the power efficiency is nearly equal to the quantum efficiency.

Several attempts were made at observing electroluminescence by injection through a Schottky barrier. No luminescence was detected, although the point contact showed an $I(V)$ rectification characteristic with the forward current increasing more rapidly with voltage above about 3.5 volts—this characteristic is consistent with the energy gap of *GaN*.

Acknowledgements

The assistance of Mrs. M. Falk in preparing Hall samples and diodes is gratefully acknowledged and we thank H. Kressel, P. LeFur, and J. J. Tietjen for helpful discussions.

References

1. Grimmeiss, H. G., and Maak, J., *Zeits. fur Naturf.* Vol. 15a (1960) pp. 799-806.
2. Grimmeiss, H. G. and Koelmans, H., *Zeit. fur Naturf.* Vol. 14a (1959) pp. 264-271.
3. Maruska, H. P. and Tietjen, J. J., *Appl. Phys. Letters* Vol. 15 (1969) p. 327.
4. Fendley, J. R., Gorog, I., Hernqvist, K. G., and Sun, C., *RCA Review,* Vol. 30 (1969) p. 422.
5. Saxena, A. N., ellipsometric measurements at 5461 A *(private communication)*.

Use of "inefficient" statistics by field personnel

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Reprint RE-16-3-22 | Final manuscript received August 10, 1970.

There are many experiments in which data gathered in the field must be reduced and analyzed later at a central facility. In some of these field experiments because of time and money, not too many replications of the experiment can be scheduled. Therefore, it is desirable to have a statistical procedure for preliminary evaluation of the data by the field test personnel.

By using "inefficient" statistics,[1] which are based on a few observations, rough estimates of parameters and the signal-to-noise ratio can be made. If the signal-to-noise ratio is too low or if the value of the measured parameter appears suspicious, the experiment can be repeated. The statistical procedure to be employed by the field test personnel should be one in which rapid and simple computation can be performed.

These procedures are being used by the Communications Research Laboratory in electromagnetic wave propagation and earth conductivity experiments. The procedure is to use the mid-range, which is the average of the highest and lowest observation, to estimate the mean; and the range, which is the difference between the highest and lowest observation, to measure the dispersion. By multiplying the computed range by a suitable coefficient, an estimate of the standard deviation is obtained. A rough estimate of measurement signal-to-noise ratio is then the ratio of the mean to the standard deviation, where the mean and standard deviation are obtained by the above procedures. If the signal-to-noise ratio is below 13 dB, the measurement is to be repeated. However, there are times when the signal-to-noise ratio is less than 13 dB and the measurement has to be accepted because the schedule does not allow for another measurement. In this case, the analyst at the central facility is at least forewarned of poor data.

By use of Fig. 1, in which measurement signal-to-noise ratio versus the ratio of largest observation to the smallest observation is plotted, computations by field personnel are reduced to a minimum.

The use of Fig. 1 is demonstrated by the following example taken from earth conductivity measurements. In the measurement setup, the conductivity was proportional to the peak-to-peak deflection on a Rustrak recorder. Nine sample observations were obtained and they are given below.

Sample No.	1	2	3	4	5	6	7	8	9
Deflection x	6.1	5.1	6.5	6	5.3	4.8	4.1	3.4	4.8

$$x_{max}=6.5, x_{min}=3.4, x_{max}/x_{min}=1.9$$

Therefore, the measurement signal-to-noise ratio from Fig. 1 is 13.5 dB.

Reference

1. Dixon, W. J. and Massey, F. J., *Introduction to Statistical Analysis* (McGraw-Hill Book Co., New York, 1951) Chap. 16.

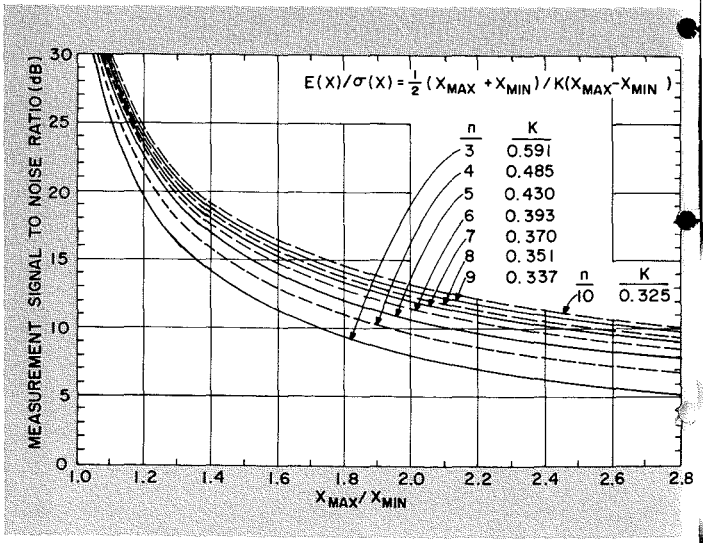
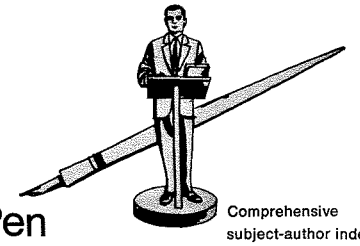


Fig. 1—Measurement signal-to-noise ratio vs largest-sample-observation to smallest-sample-observation ratio.



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OBSTACLE WARNING SYSTEMS for Helicopters, Miniature—H. Eckhardt, N. Luce (ASD, Burl) 26th Annual Forum of the American Helicopter Soc., Washington, D.C.; 6/16-18/70

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AVALANCHE-DIODE OSCILLATOR Circuit, Tunable L-Band High-Power—P. A. Levine, S. G. Liu (Labs, Pr) *IEEE Trans. on Solid-State Circuits*, Vol. SC-4, No. 6, Dec. 1969

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MICROWAVE INTEGRATED CIRCUITS, The Lumped Element Approach—M. Caulton (Labs, Pr) *Microwave Journal* Vol. 13, No. 5; May 1970

THIN-FILM Integrated Circuits—A Survey—Dr. P. Schnitzler (DME, Som) RCA Packaging Synp. Princeton; 8/12/70

COMMUNICATION, DIGITAL (equipment & techniques)

MULTI-BIT DELTA MODULATION, Comparison and Design Criteria for—M. Hecht (AED, Pr) Symposium on Picture Coding, N. Carolina State Univ.; 9/10/70

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TIME SHARING TEST SYSTEMS with Centrally Controlled Test Stations—E. Wyant (ASD, Burl) MEPCON East, New York City; 6/27/70

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DIGITAL STYLUS SYSTEM, The Sonic Pen—A—P. DeBryne, A. E. Brenner (ASD, Burl) *IEEE Trans. on Computers*, Vol. 19, No. 6 pp 546-548. 6/70

COMPUTER STORAGE

OPTICAL MEMORIES, Promise of—J. A. Rajchman (Labs, Pr) *J. of Applied Physics Supplement*, Vol. 41, No. 3; 3/1/70

COMPUTER SYSTEMS

SMALL COMPUTERS, Characteristics and Selection of—A. L. Linton (GSD, Dayton) 1970 IEEE Conv.; and Digest

CONTROL SYSTEMS (& automation)

LM RENDEZVOUS RADAR REDUNDANT GYRO SYSTEM, Principles Involved in the—J. Dubbury (ASD, Burl) *IEEE Trans. on Aerospace and Electronic Systems* Vol. 6, No. 4, pp. 544-550; 7/70

DISPLAYS

TWO-COLOR ALPHANUMERIC DISPLAY—K. C. Adam (EASD, Van Nuys) *Information Display*, Vol. 7, No. 7; July/Aug. 1970

DISPLAY MAGNETIC FIELD LINES, A Device to—J. B. Grosh (EC, Lanc) *American J. of Physics*, Vol. 38, No. 6; 6/70

PHOTOTRANSISTOR ARRAYS of Simplified Design—P. K. Weimer, F. V. Shallcross, V. L. Frantz (Labs, Pr) 1970 Summer Program on Imaging Devices, Univ. of Rhode Island, Kingston, R.I.; 8/14/70

LIQUID-CRYSTAL Display Devices—G. H. Heilmeier (Labs, Pr) *Scientific American* Vol. 222, No. 4, 4/70

DOCUMENTATION (& information science)

PROCUREMENT PRACTICES for Mil Spec Technical Publications—R. J. Ellis (EASD, Van Nuys) NSIA/AMC Equip. Manuals Symposium & Related Problem, Los Angeles; 7/22/70

BUSINESS & TECHNICAL PRESENTATIONS, Effective (book review)—T. G. Greene (M&SR, Mrstn) *IEEE Trans. on Engineering Writing and Speech*, Vol. EWS-13; 5/70

EDUCATION (& training)

TECHNICAL EDUCATION Approaches at the RCA Lancaster, Pa. Plant—J. M. Forman (EC, Lanc) Central Pa. Chapter of the American Soc. for Training and Development, York, Pa.; 5/5/70

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PHOTOCONDUCTIVE SENSOR for Card Readers—F. V. Shallcross, W. S. Pike, P. K. Weimer, G. K. Fryszman (Labs, Pr) Photo Electronic Imaging Devices Conf., Univ. of Rhode Island, Kingston, R.I.; 8/7/70

ENERGY CONVERSION (& power sources)

HEAT PIPES—A New Concept in Heat Transfer—W. E. Harbaugh (EC, Lanc) American Gas Assoc., Inc., Minneapolis, Minn.; 5/6/70

NICKEL CADMIUM BATTERIES, Thermal and Mechanical Design of—T. Wylie, H. Theirfelder (AED, Pr) ASME 1970 Space Technology and Heat Transfer Conf., Los Angeles; 6/24/70

POWER GENERATION, Tubes and/or Solid-State Devices for—L. S. Nergaard (Labs, Pr) Microwave Journal Vol. 13, No. 4; 4/70

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POLLUTION & RCA—C. A. Smith (EC, Lanc) Lampeter-Strasburg High School, Earth Day; 4/22/70

INDUSTRIAL WASTE TREATMENT PLANT, Operational Growing Pains of an—H. G. Cox (RCA Ltd., Mont) 17th Ontario Industrial Waste Conf.; 6/70

GEOPHYSICS

EARTH RESOURCES Satellites—M. G. Staton (AED, Pr) "Operation Ground Shot" Sioux Falls, S.D. Industrial Foundation, Sioux Falls, S.D.; 5/21/70

SEA SURFACE TEMPERATURE, Passive Microwave Radiometric Measurements of—D. G. Shipley, K. J. Torok (AED, Pr) 1970 IEEE Intl. Conf. on the Ocean Environment; *Conf. Digest*, Panama City, Fla.; 9/21-24/70

SKAMP—Station Keeping and Mobile Platform—E. W. Schlieben (AED, Pr) 6th Annual Conf. and Exhib. of Marine Tech. Soc., Washington, D.C.; 6/30/70

GRAPHIC ARTS

COLOR PICTURE REPRODUCTION Using a High Resolution Television System—C. R. Smith, J. A. D'Arcy, E. A. Enfiejian (AED, Pr) J. of SMPTE; 3/70

ELECTROFAX DEVELOPMENT by Reversal Liquid Toning, Charge Transfer in—E. C. Hutter, E. C. Giaimo (Labs, Pr) *Photographic Science and Engineering* Vol. 14, No. 3; May/June 1970

FIRE PHOTOGRAPHY, Use of the 35mm Camera in—C. Asbrand (ASD, Burl) Intl. Fire Photographers Assoc. Sem., Chicago, Ill.; 7/24/70

HALFTONE PICTURES, Electronically Generated—R. J. Klensch, D. Meyerhofer, J. J. Walsh (Labs, Pr) TAGA Conf., Boston, Mass.; 7/5/70

CHARGE DENSITY AND CAPACITANCE IN ELECTROPHOTOGRAPHIC MATERIALS, Apparatus and Method for Measurement of—R. B. Comizzoli (Labs, Pr) *Photographic Science and Engineering*, Vol. 14, No. 3 May/June 1970

HOLOGRAPHY

HOLOGRAPHIC RECORDING, Photoresists and Other Media for—M. T. Gale, D. L. Greenaway, J. P. Russell (Labs, Pr) Conf. on Holography Applications, Besancon, France; 7/6-11/70

MICROCIRCUIT MANUFACTURE and Mask Generation, Application of Holography to—D. L. Greenaway, J. P. Russell (Labs, Pr) Conf. on Holography Application, Besancon, France, 7/6-11/70

PERMANENT HOLOGRAMS in Glass—RF Sputter Etching—J. J. Hanak, J. P. Russell (Labs, Pr) Conf. on Holography Applications, Besancon, France; 7/6-11/70

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AIR GAGING and Measurement—M. Van Renssen (EC, Lanc) Creativity Workshop Program, Lititz Elementary School, Warwick District, Pa.; 5/15/70

EQUALIZED FILTERS for Communication Satellite Multiplexers, Light-weight Design of—M. V. O'Donovan, C. M. Kudsia, S. Singer (RCA Ltd., Mont) Intl. Conf. on Communications, San Francisco, Calif.; 6/70

SCANNING ELECTRON MICROSCOPY—M. D. Coutts (Labs, Pr) MIT, Boston, Mass.; 8/6/70

SIMPLE CRYOSTAT for Optical Measurements in a Magnetic Field Between 3.6 and 300°K—H. W. Lehmann, E. Meier (Labs, Pr) *J. of Physics E: Scientific Instruments*, Vol. 3, 1970

SURFACE AND BULK ANALYSIS by Use of Infrared, Visible and Ultra-violet Radiation—P. J. Zanzucchi (Labs, Pr) MIT, Boston, Mass.; 7/29/70

LASERS

CdS LASERS with End-Pumped Configuration, Low-Threshold Electron-Beam Pumped—F. H. Micoli (Labs, Pr) *Applied Physics Letters*, Vol. 16, No. 12; 6/15/70

DOUBLE INJECTION in Insulators. II. Further Analytic Results with Negative Resistance—A. Waxman, M. A. Lampter (Labs, Pr)*Physical Review B*, Vol. 1, No. 6; 3/15/70

Er^{3+} in $(La,Y)_2O_2S$ HOSTS, The Emission Efficiency of—R. E. Shrader, P. N. Yocom (Labs, Pr) *J. of Luminescence* Vol. 1, 2, 1970

He-Cd LASER, Stabilization of—K. G. Hernqvist (Labs, Pr) *Applied Physics Letters*, Vol. 16, No. 11; 6/1/70

HELIUM-CADMIUM LASER, Simplified Construction and Processing of a—K. G. Hernqvist, D. C. Pultorak (Labs, Pr) *Review of Scientific Instruments*, Vol. 41, No. 5; 5/70

HOLE VELOCITY in p-GaAs—V. L. Dalal (Labs, Pr) *Applied Physics Letters*, Vol. 16, No. 12; 6/15/70

MAJORITY-CARRIER INJECTION from a Point Contact, Unusual Field Phenomena Associated with—E. Rossiter, P. Mark, M. A. Lampert (Labs, Pr) *Solid State Electronics*, Vol. 13; 1970

p-n JUNCTION LASERS BY Use of a Heterojunction: Theory and Experiment, Control of Optical Losses in—H. Kressel, H. Nelson, F. Z. Hawrylo (Labs, Pr) *J. of Applied Physics*, Vol. 41, No. 5, 4/70

SEMICONDUCTING LASERS: "Disciplining" Photons Boosts the Efficiency—H. Kressel, H. Nelson, H. Lockwood (Labs, Pr) *Electronics*, Vol. 43, No. 6 3/15/70

MANAGEMENT

MAGNETIC REGISTERS, Radiation Hardened Transistor—D. Hampel, K. J. Prost (DCSD, Cam) IEEE Conf. on Nuclear and Space Radiation Effects, San Diego, Calif.; 7/21-23/70

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CHOOSING THE LARGEST POPULATION MEAN, Optimum Sample Size for—P. N. Somerville (ServCo, MTP) *J. of the American Statistical Association*, Vol. 65, No. 330; 6/70

LATTICE SOLUTIONS by Using Electrical Networks, Studies on—R. Hirota, K. Suzuki (Labs, Pr) *J. of Physical Soc. of Japan*, Vol. 28, 1970

MONTE CARLO SOLUTIONS for Hypersonic Flow of Binary Mixtures Over Axially Symmetric Bodies—G. K. Bienkowski, R. R. McKinley, S. M. Siskind (AED, Pr) Seventh Intl. Symposium on Rarified Gas Dynamics, Pisa, Italy; 7/1/70

PERCENTAGE POINTS OF A STATISTIC, A Technique for the Computation of—P. N. Somerville (ServCo, MTP) *Technometrics*, Vol. 12, No. 2, 5/70

MECHANICAL DEVICES

ACTUATOR for Spacecraft Thermal Control Employing Bimetallics, A Simplified Lightweight—K. L. Schilling (AED, Pr) 5th Aerospace Mechanisms Symp., Goddard Space Flight Center, Greenbelt, Md.; 6/15-16/70

SURFACE TENSION DEVICES for Propellant Acquisition, A Survey of Current Developments in—D. L. Balzer, Y. C. Brill (AED, Pr) and Lockheed personnel AIAA 6th Joint Propulsion Specialist Conf., San Diego; 6/18/70

PLASMA PHYSICS

GENERALIZED SPECTRAL FUNCTIONS from Density Turbulence, Time Variations of—I. P. Shkarofsky (RCA LTD, Mont) *AIAA Journal*, Vol. 8, No. 6, 6/70

PLASMAS INJECTED into Solids: Analytic Study of the Diffusion Corrections—R. B. Schilling, M. A. Lampert (Labs, Pr) *J. of Applied Physics*, Vol. 41 No. 4; 3/15/70

PROPERTIES, MOLECULAR (& crystalography)

AMPHOTERIC SILICON-DOPED GaAs DIODES. II. Transient Response, Electroluminescence—N. E. Byer (Labs, Pr) *J. of Applied Physics*, Vol. 41, No. 4; 3/15/70

A-SITE CHROMIUM CHALOCOGENIDE SPINELS, Some New Mixed—H. L. Pinch, E. Lopatin (Labs, Pr) *Materials Research Bulletin*, Vol. 5, No. 6, 1970

CHROMIUM CHALOCOGENIDE SPINELS, Origin of Anomalous Absorption Edge Shifts in—S. B. Berger (Labs, Pr) *J. of Applied Physics*, Vol. 41, No. 3; 3/1/70

CHROMIUM CHALCOGENIDES with Spinel and Hexagonal Structures, Thermogravimetric Study of Some—Y. Wada, K. Ametani (Labs, Pr) Joint Mtg. of the Japanese Chemical Soc., Hokkaido Inst. of Technology; 8/29-30/70

ELECTRON-IRRADIATED N-TYPE SILICON, Li-Defect Interactions in—B. Goldstein (Labs, Pr) Radiation Conf., State Univ. of N.Y., Albany, N.Y. 8/17-21/70

EPITAXIAL DEPOSITION of Silicon on Insulating Substrates for MOS Circuitry—G. W. Cullen, G. E. Gottlieb, J. Scott (Labs, Pr) Mtg. of Metallurgical Soc., New York; 8/30/70

EPITAXIAL GROWTH of Silicon at Low Temperature from Silane—Y. S. Chiang, D. Richman (Labs, Pr) Mtg. of Metallurgical Soc., New York; 8/30/70

$In_xGa_{1-x}P$ ALLOYS, Preparation and Preparation and Properties of—D. Richman, C. J. Nuese, R. Clough (Labs, Pr) Mtg. of Metallurgical Soc., New York; 8/30/70

IONIZATION ENERGY of Mg Nd Be Acceptors in GaAs—H. Kressel, F. Z. Hawrylo (Labs, Pr) *J. of Applied Physics*, Vol. 14, No. 4; 3/15/70

LIQUID CRYSTAL Display Devices—G. H. Heilmeier (Labs, Pr) *Scientific American*, Vol. 222, No. 4, 4/70

LIQUID CRYSTALS, A Review of Electric and Magnetic Field Effects in—G. H. Heilmeier (Labs, Pr) Liquid Crystal Conf., Berlin, Germany; 8/24-28/70

LIQUID CRYSTALS V. Room Temperature Nematic Materials Derived from P-Alkylcarbonato- p' -Alkoxyphenyl Benzoates—J. A. Castellano, M. T. McCaffrey, J. E. Goldmacher (Labs, Pr) Intl. Liquid Crystal Conf., Berlin, Germany; 8/24-28/70

MIS STRUCTURES in Silicon on Spinel Using Thin Films of Al_2O_3 and Si_3N_4 Preparation and Properties of—M. T. Duffy, C. C. Wang, G. W. Cullen (Labs, Pr) Mtg. of Metallurgical Soc., New York; 8/30/70

POLED, TWIN-FREE CRYSTALS of Ferroelectric Bismuth Titanate, $Bi_4Ti_3O_{12}$, Preparation of—M. M. Hopkins, A. Miller (Labs, Pr) *Ferroelectrics*, Vol. 1, 3/70

QUATERNARY ALLOYS, Bandgap Variation in—S. Bloom (Labs, Pr) *J. of Applied Physics*, Vol. 41, No. 4; 3/15/70

RARE-EARTH-DOPED OXYSULFIDES for GaAs-Pumped Luminescent Devices—P. N. Yocom, J. P. Wittke, I. Kadany (Labs, Pr) Mtg. of Metallurgical Soc., New York; 8/30/70

SEMICONDUTOR ALLOY $(GaP)_{.95}(ZnSe)_{.05}$, Electronic Transport Properties in the—M. Glicksman, D. H. Gutman, W. M. Yim (Labs, Pr) *Applied Physics Letters*, Voly. 16, No. 9; 5/1/70

SHEARED NEMATIC LIQUID CRYSTALS, Torques in: A Simple Model in Terms of the Theory of Dense Fluids—W. Helfrich (Labs, Pr) Third Intl. Liquid Crystal Conf., Berlin, Germany; 8/24-28/70.

SINGLE CRYSTAL BISMUTH TITANATE, Self Reversal and Waiting Time Effects in—G. W. Taylor (Labs, Pr) *J. of Physical Soc. of Japan, Supplement*, Vol. 28 1970

SPIN-LATTICE RELAXATION of Tm^{2+} in CaF_2, SrF_2, and BaF_2—E. S. Sabisky, C. H. Anderson (Labs, Pr) *Physical Review* B1-1, Vol. 1, No. 5; 3/1/70

STRAIN SENSITIVITY of Mn Doped Films—L. S. Onyshkevych (Labs, Pr) *J. of Applied Physics Supplement*, Vol. 14, No. 2, 3/70

SYSTEM TETRA-*ISO*-PENTYL AMMONIUM NITRATE—p-AZOXYANISOLE, Ionic Equilibrium and Ionic Conductance in—A. Sussman (Labs, Pr) Intl. Liquid Crystal Conf. Berlin, Germany; 8/24-28/70

VAPOR-GROWN GaAs:Si, Electrical and Optical Properties of—H. Kressel, H. von Philipsborn (Labs, Pr) *J. of Applied Physics*, Vol. 14, No. 5, 4/70

VAPOR GROWTH of III-V Compounds—R. E. Enstrom (Labs, Pr) Gordon Research Conf. on Crystal Growth, Plymouth, New Hampshire; 6/25/70

VAPOR TRANSPORT, Crystal Growth of Metal-Phosphorus-Sulfur Compounds by—R. Mitche, P. Wild (Labs, Pr) *Material Research Bulletin*, Vol. 5, No. 6, 1970

YIG AND NICKEL, Kink-Point Locus and Critical Phenomena of—K. Miyatani, K. Yoshikawa (Labs, Pr) *J. of Applied Physics Supplement,* Vol. 14, No. 3; 3/70

YTTRIUM AND LANTHANUM OXYSULFIDES, Role of the Charge-Transfer States in Feeding and Thermally Emptying the 5_0 States of Eu^{+3} in—C. W. Struck, W. H. Fonger (Labs, Pr) *J. of Luminescence,* Vol. 1, 2, 1970

PROPERTIES, SURFACE
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PYROLYTIC ALUMINUM OXIDE FILMS on Silicon Substrates, Dielectric and Interface Properties—M. T. Duffy, J. E. Carnes, D. Richman (Labs, Pr) Mtg. of Metallurgical Soc., New York; 8/30/70

THIN FILMS OF LIQUID HELIUM, Phonon Interference in—C. H. Anderson, E. S. Sabisky (Labs, Pr) *Physical Review Letters,* Vol. 24, No. 19; 5/11/70

WURTZITE AND ZINCBLENDE CRYSTALS, Madelung Constants Near the Principal Nonpolar Faces of—R. W. Nosker, P. Mark (Labs, Pr) *Surface Science,* Vol. 20, No. 2; 4/70

PROPERTIES ELECTRICAL

$CuCr_2$ $Se_{4-x}Br_x$ SYSTEM, Magnetic and Electrical Properties of the—K. Miyatani, K. Minematsu, Y. Wada, F. Okamoto, K. Kato, P. K. Baltzer (Labs, Pr) *J. of Applied Physics,* Vol. 14, No. 3: 3/1/70

DOUBLE EXTRACTION of Uniformly Generated Electron-Hole Pairs from Insulators with Non-Injecting Contacts—A. M. Goodman, A. Rose (Labs, Pr) 10th Intl. Conf. on Physics of Semiconductors, Cambridge, Mass.; 8/17-21/70

ENERGY DEPENDENCE of Conduction in Band Tails—D. Redfield, R. S. Crandall (Labs, Pr) Intl. Conf. of Physics of Semiconductors, Cambridge, Mass.; 8/17-21/70

FIELD-DEPENDENT PHOTOLUMINESCENCE in N-GaAs: Hot Electron Distribution and Electron-Exciton Equilibrium—P. D. Southgate, D. S. Hall, A. B. Dreeben (Labs, Pr) Intl. Conf. on Physics of Semiconductors, Boston, Mass.; 8/17-21/70

NEGATIVE RESISTANCE OF CdSe, Experimental Investigation of—L. J. Nicastro (ATL, Cam) *Dissertation Abstracts,* Vol. 31, No. 4, 1970

OPTICAL PROPERTIES OF GaN—J. I. Pankove, H. P. Maruska, J. E. Berkeyheiser (Labs, Pr) Intl. Conf. on the Physics of Semi-conductors, Cambridge, Mass.; 8/17-21/70

PHOTOCURRENT MULTIPLICATION Due to Donor Impact Ionization—R. S. Crandall (Labs, Pr) Intl. Conf. on Physics of Semiconductors, Boston, Mass. 8/17-21/70

STRONTIUM TITANATE, Anamalous Ultrasonic Attenuation at the 150°K Transition in—W. Rehwald (Labs, Pr) *Solid State Communications,* Vol. 8, No. 8, 1970

PROPERTIES, MAGNETIC

$CuCr_2Se_{4-x}Br_x$ SYSTEM, Magnetic and Electrical Properties of the—K. Miyatani, K. Minematsu, Y. Wada, F. Okamoto, K. Kato, P. K. Baltzer (Labs, Pr) *J. of Applied Physics,* Vol. 14, No. 3; 3/1/70

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AMPHOTERIC SILICON-DOPED GaAs DIODES. I. Steady-State Response, Electroluminescence in—N. E. Byer (Labs, Pr) *J. of Applied Physics,* Vol. 41, No. 4; 3/15/70

BULK ELECTROLUMINESCENCE in Degenerate GaAs, Field-Dependence of—P. D. Southgate (Labs, Pr) *J. of Luminescence,* Vol. 1, 2, 1970

LIGHT SCATTERING in Ferro-magnetic Semiconductors—E. F. Steigmeier, G. Harbeke (Labs, Pr) 10th Intl. Conf. on Physics of Semiconductors, Boston, Mass.; 8/17-21/70

OPTOELECTRONIC COLD CATHODE Using an $Al_xGa_{1-x}As$ Heterojunction Structure—H. Kressel, E. S. Kohn, H. Nelson, J. J. Tietjen, L. R. Weisberg (Labs, Pr) *Applied Physics Letters,* Vol. 16, No. 9; 5/1/70

PHOTOCHROMIC CALCIUM FLUORIDE by Additive Coloration, Preparation of—R. C. Duncan, W. Phillips (Labs, Pr) Mtg. of the Metallurgical Soc., New York; 8/30/70

PHOTOEMISSION of Holes and Electrons from Aluminum into Aluminum Oxide—A. M. Goodman (Labs, Pr) *J. of Applied Physics,* Vol. 41, No. 5, 4/70

RADIATION EFFECTS

CMOS LOGIC NETWORKS. Long-Term Effects of Radiation on—A. G. Holmes-Siedle, W. J. Poch (AED, Pr) 1970 IEEE Conf. on Nuclear and Space Radiation Effects; *IEEE Trans. on Nuclear Science,* San Diego, Calif.; 7/22/70

ELECTRON BOMBARDMENT DAMAGE in Lithium-Containing Silicon, Annealing of—G. J. Brucker (AED, Pr) 1970 IEEE Conf. on Nuclear and Space Radiation Effects; *IEEE Trans. on Nuclear Science,* San Diego, Calif.; 7/21/70

HARDENED INTEGRATED CIRCUITS, Permanent Radiation Effects in—F. B. Micheletti, K. H. Zaininger (Labs, Pr) 1970 IEEE Conf. on Nuclear & Space Radiation Effect, San Diego; 7/21-23/70

HARDENING SILICON SOLAR CELLS Against the Radiation Environment, Recent Advances in—M. Wolf, G. Brucker (AED, Pr) 1970 IECEC, Las Vegas, Nev.; 9/22/70

METAL INSULATOR SEMICONDUCTOR DEVICES, Effects of Radiation in—A. G. Holmes-Siedle (AED, Pr) Solid State Seminar, Princeton Univ.; 3/13/70

WEATHER SATELLITE for the Radiation Environment, The Design of—A. G. Holmes-Siedle, W. J. Poch (AED, Pr) British Interplanetary Main Conf. 1, London, England; 9/16/70

SOLID-STATE DEVICES

AVALANCHE-DIODE OSCILLATOR Circuit, Tunable L-Band High-Power—P. A. Levine, S. G. Liu (Labs, Pr) IEEE Trans. on Solid-State Circuits, Vol. SC-4, No. 6, Dec. 1969

FUNCTIONAL GUNN DIODES, A Rapid Evaluation Technique for—R. D. Larrabee, W. A. Hicinbothem, M. C. Steele (Labs, Pr) *IEEE Trans. on Electron Devices,* Vol., ED-17, No. 4; 4/70

HETEROJUNCTION DIODES, Vacuum-Deposited Thin-Film p-Se/n-CdSe—R. M. Moore, C. J. Busanovich (Labs, Pr) *IEEE Trans. on Electron Devices* Vol. ED-17 No. 4, 4/70

LITHIUM-CONTAINING SOLAR CELLS, Room-Temperature Stability of—T. J. Faith, J. Corra, A. G. Holmes-Siedle (AED, Pr) IEEE Photovoltaic Specialists Conf.; *Proc.,* Seattle, Wash.; 8/5/70

MICROWAVE INTEGRATED CIRCUITS, The Lumped Element Approach to—M. Caulton (Labs, Pr) *Microwave J.* Vol. 13, No. 5; 5/70

PHOTOTRANSISTOR ARRAYS of Simplified Design—P. K. Weimer, F. V. Shallcross, V. L. Frantz (Labs, Pr) 1970 Summer Program on Imaging Devices, Univ. of Rhode Island, Kingston, R.I.; 8/14/70

POWER GENERATION, Tubes and/or Solid-State Devices for—L. S. Nergaard (Labs, Pr) *Microwave J.* Vol. 13, No. 4, 4/70

SPACE COMMUNICATION
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EARTH SATELLITES, Communications and Broadcasting by—M. G. Staton (AED, Pr) Rocky Mountain Assoc. of Broadcasters Annual Conv., Jackson Hole, Wyoming; 6/24/70

SPACE NAVIGATION (& tracking)

CELESTIAL NAVIGATION—Inexpensive Position, Fixes by Satellite, New—J. E. Board (AED, Pr) 25th Anniversary Mtg. of the Inst. of Navigation, USAF Academy, Colorado Springs; 7/2/70

DUAL-SPIN SPACECRAFT, Linearization of the Closed Loop Dynamics of a—K. T. Phillips (AED, Pr) AIAA Guidance and Control Conf.; *Conference Paper;* 8/18/70

SPACECRAFT (& space missions)

MISSION PLANNING for Exploration of the Outer Planets—B. P. Miller (AED, PR) *Astronautics and Aeronautics,* 5/70

WEATHER SATELLITE for the Radiation Environment—A Case History, The Design of—A. G. Holmes-Siedle, W. J. Poch (AED, Pr) British Interplanetary Main Conf. 1, London, England; 9/16/70

TRANSMISSION LINES
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DIRECTIONAL COUPLERS, Coplanar-Waveguide—C. P. Wen (Labs, Pr) *IEEE Trans. on Microwave Theory and Techniques,* Vol. MTT-18, No. 6, 6/70

MAGNETOPLASMA-LOADED WAVEGUIDE at Room Temperature, Field Distribution in a—R. Hirota, K.Suzuki (Labs, Pr) *IEEE Trans. on Microwave Theory and Tech.* Vol. MTT-18, No. 4; 4/70

TUBES, ELECTRON
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POWER GENERATION, Tubes and/or Solid-State Devices for—L. S. Nergaard (Labs, Pr) Microwave J. Vol. 13, No. 4, 4/70

VACUUM

ULTRA-CLEAN AIR—M. N. Slater (EC, Lanc) American Vacuum Society Seminar, Princeton, N.J.; 5/28/70

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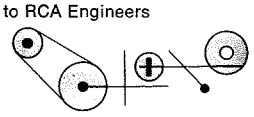
Patents Granted to RCA Engineers



As reported by RCA Domestic Patents, Princeton

Electronic Components

Stabilization of Thin Film Transistors—M. L. Topfer (EC, Som) R. E. Quinn (Labs, Pr) U.S. Pat. 3,520,051; July 14, 1970.

Fabrication of Semiconductive Devices with Silicon Nitride Coatings—J. H. Scott, Jr., (EC, Som) U.S. Pat. 3,520,722; July 14, 1970.

Complementary Transistor Write and NDRO For Memory Cell—S. Katz (EC, Som) U.S. Pat. 3,521,242; July 21, 1970 Assigned to U.S. Government.

Apparatus for Regulating the Light Output of a Flash Lamp—F. Caprari (EC, Som) U.S. Pat. 3,525,016; August 18, 1970.

Cascade Connected Regenerative Amplifiers—L. J. Striednig (EC, Som) U.S. Pat. 3,424,051; August 18, 1970; Assigned to U.S. Government.

Limiting Network—D. J. Kanter (EC, Som) U.S. Pat. 3,522,443; August 4, 1970.

Temperature Tracking of Emitter Coupled Differential Amplifier Stage—R. C. Heuner, I. Ostroff (EC, Som) U.S. Pat. 3,522,548; August 4, 1970.

Information Switching and Storage Circuitry—B. Zuk (EC, Som) U.S. Pat. 3,529,294.

Consumer Electronics

Statistical Method, Under Computer Control, for the Manufacture and Test of Mass Produced Articles—E. Deger, J. B. Schultz (CE, Indpls) U.S. Pat. 3,526,836; September 1, 1970.

Service Air For Color Television Receiver—D. H. Willis (CE, Indpls) U.S. Pat. 3,525,801; August 25, 1970.

Laboratories

Filamentary Structure Injection Laser Having a Very Narrow Active Junction—J. I. Pankove (Labs, Pr) U.S. Pat 3,526,-851; September 1, 1970.

Thermoplastic Deformation Imaging Process—F. H. Nicoll (Labs, Pr) U.S. Pat. 3,525,613; August 25, 1970.

Duplexer Having Two Non-Reciprocal Shifting Means—W. W. Siekanowicz, D. J. Blattner, T. E. Walsh (Labs, Pr) U.S. Pat. 3,525,952; August 25, 1970.

Laser Tube Construction—J. R. Fendley, Jr. (Labs, Pr) U.S. Pat. 3,522,551; August 4, 1970.

Character Selector and Generating Device—M. H. Lewin (Labs, Pr) U.S. Pat. 3,523,161; August 4, 1970.

RF Excitation Pumping of Gas Lasers by Means of a Wave Guide and Coupling Coils—T. J. Faith, Jr., G. W. Hoffman, (Labs, Pr) U.S. Pat. 3,521,119; July 21, 1970; Assigned to U.S. Government.

Microminiature Electrical Component Having Integral Indexing Means—W. L. Oates (Labs, Pr) U.S. Pat. 3,521,128, July 21, 1970.

Electrical Circuit for Processing Periodic Signal Pulses—P. K. Weimer (Labs, Pr) U.S. Pat. 3,521,244; July 21, 1970; Assigned to U.S. Government.

Data Conversion and Display Apparatus—J. C. Miller (Labs, Pr) U.S. Pat. 3,521,-268; July 21, 1970.

Electronically Controlled Delay Line—R. A. R. Shahbender (Labs, Pr) U.S. Pat. 3,421,198; July 21, 1970.

Missile and Surface Radar Division

Antenna Arrays with Elements Aperiodically Arranged to Reduce Grating Lobes—D. F. Bowman (M&SR, Mrstn) U.S. Pat. 3,524,188; August, 1970.

Multiple Font Keyboard—T. C. Abrahamsen (M&SR, Mrstn) U.S. Pat. 3,517,792; June, 1970.

Information Systems Division

Read-Only Magnetic Memory—M. E. Steiner, G. J. Waas (ESD, Cam) U.S. Pat. 3,522,592; August 4, 1970.

Two-Element-Per-Bit Random Access Memory With Quiet Digit-Sense System—P. K. Hsieh, J. L. Freeman, Jr., (ISD, Cam) U.S. Pat. 3,522,593; August 4, 1970.

Current Mode Circuit—A Sheng (ISD, Cam) U.S. Pat. 3,523,194; August 4, 1970.

Current Pulse Driver Apparatus Employing Nonsaturating Transistor Switching Techniques and Having Low-Power Drain During Non-Pulse Periods—W. E. Salzer (ISD, W. Palm) U.S. Pat. 3,523,-197; August 4, 1970.

Printer Paper Feed Control System—R. C. Peyton (ISD, W. Palm) U.S. Pat. 3,-524,528; August 18, 1970.

Binary Coded Decimal to Binary Conversion—M. C. Wang (ISD, W. Palm) U.S. Pat. 3,524,976; August 18, 1970.

Binary Multiplier Employing Multiple Input Threshold Gate Adders—M. C. Wang (ISD, W. Palm) U.S. Pat. 3,524,977; August 18, 1970.

Transistor Amplifier Having Emitter Bypass Through an Auxiliary Transistor—D. H. Montgomery, J. R. Oberman (ISD, Cam) U.S. Pat. 3,524,141; August 11, 1970.

Character Reader—H. B. Currie (ISD, Cam) U.S. Pat. 3,524,188; August 11, 1970.

Random Access Memory with Quiet Digit-Sense System—P. K. Hsieh, D. Bennima (ISD, Cam) U.S. Pat. 3,530,445; September 22, 1970.

Commercial Electronic Systems Division

Temperature Compensated Crystal Oscillator—P. K. Mrozek (CES, Meadowlands) U.S. Pat. 3,525,055; August 18, 1970.

Electromagnetic & Aviation Systems Division

Storage System Employing Magnetic Tape Cartridges—A. Lichowsky (EASD, Van Nuys) U.S. Pat. 3,525,086; August 18, 1970.

Defense Engineering

Translating Information with Multi-Phase Clock Signals—M. M. Kaufman (DE, Cam) U.S. Pat. 3,524,077; August 11, 1970.

Synchronizing Servosystem with Memory Means—G. V. Jacoby, J. C. Kmiec (DE, Cam) U.S. Pat. 3,520,993; July 21, 1970.

Multichannel Receiving System in Which Each Channel's Weight in the Combined Output Depends on the Rate of Fading in Said Channel's—M. Masonson (DE, New York) U.S. Pat. 3,475,688; July 21, 1970; Assigned to U.S. Government.

Advanced Technology Laboratories

Triangulation Radar System—W. J. Hannan (ATL, Cam) U.S. Pat. 3,530,468; September 22, 1970.

Computer Memory Address Generator—R. D. Smith (ATL, Cam) U.S. Pat. 3,530,-439; September 22, 1970.

Professional Meetings

✲ Dates and Deadlines

Be sure deadlines are met—consult your Technical Publications Administrator or your Editorial Representative for the lead time necessary to obtain RCA approvals (and government approvals, if applicable). Remember, abstracts and manuscripts must be so approved BEFORE sending them to the meeting committee.

Calls for papers

MARCH 31-APRIL 2, 1971: **Reliability Physics Symposium,** Stardust Hotel, Las Vegas, Nev., G-R. **Deadline info: (abst) 11/15/70 to:** O. D. Trapp, Fairchild Semiconductor, 464 Ellis St., Mountain View, Calif. 94040.

APRIL 12-15, 1971: **National Telemetering Conference,** Washington Hilton Hotel, Washington, D.C., G-AES, G-ComTech. **Deadline info: (abst) 12/14/70 to:** H. B. Riblet, Johns Hopkins Univ., 8621 Georgia Ave., Silver Spring, Md. 20910.

APRIL 18-21, 1971: Off-Shore **Technology Conference,** Astrohall, Houston, Texas, TAB Oceanography Coordinating Committee et al. **Deadline info: (abst) 10/1/70 to:** H. S. Field, Geophysical Res. Corp., 136 Mohawk Blvd., Tulsa, Ok. 74106.

MAY 4-5, 1971. **Appliance Technical Conference,** Sheraton Chicago Hotel, Chicago, Illinois, G-IGA, Chicago Section. **Deadline info: (syn) 10/1/70 to:** IEEE Office, 345 East 47th Street, New York, New York 10017.

MAY 10-12, 1971: **AIAA Joint Strategic Missile Sciences Meeting,** U.S. Naval Academy, Annapolis, Maryland, ARPA, ABMDA, SAMSO, AIAA. **Deadline info: (paper—first draft) 12/4/70 to:** Dr. Richard Hartunian, Aerospace Corp., 1111 Mill Street, San Bernardina, Calif. 92408.

MAY 11-13, 1971: **Sixth Region Technical Conference,** Woodlake Hotel, Sacramento, California, Region 6, Sacramento Sect. **Deadline info: (abst) 12/1/70 (ms) 3/1/70 to:** Ronald Soohoo, Univ. of Calif., Dept. of EE, Davis, Calif. 95616.

MAY 24-26, 1971: **1971 IEEE Power Industry Computer Applications Conference (PICA),** Statler Hilton Hotel, Boston, Mass., G-P. **Deadline info: (abst) 10/15/70 (ms) 1/8/71 to:** Paul L. Dandeno, Hydro Electric Power Commission of Ontario, 620 University Avenue, Toronto, Ontario, Canada.

SUMMER 1971: **Special issue of the IEEE Transactions on Electron Devices devoted to Information Display Devices,** IEEE. **Deadline info: (papers) 1/15/71 to:** Mr. Irving Reingold, Guest Editor, Chief; Pickup, Display & Storage Devices Branch, AMSEL-KL-TD, Electron Tubes Division, U.S. Army Electronics Command, Fort Monmouth, New Jersey 07703.

JUNE 2-4, 1971: **Conference on Laser Engineering & Applications,** Washington Hilton Hotel, Washington, D.C., IEEE Quantum Elec. Council, OSA. **Deadline info: (sum & abst) 1/11/71 to:** D. E. Caddes, Sylvania Elec. Sys., Electro-Optics, Organ., Mountain View, Calif. 94040.

JUNE 27-JULY 1, 1971: **Design Automation Workshop,** Shelburne Hotel, Atlantic City, New Jersey, G-C, ACM, SHARE. **Deadline info: (abst) 1/4/71 to:** R. B. Hitchcock, Sr., IBM, Box 218, Yorktown Hgts., N.Y. 10598.

JULY 18-23, 1971: **Summer Power Meeting & Int'l Symp. on High Power Testing,** Portland Hilton Hotel, Portland, Oregon, G-P. **Deadline info: (papers) 2/15/71 to:** IEEE, 345 East 47th Street, New York, N.Y. 10017.

AUG. 11-13, 1971: **1971 Joint Automatic Control Conference,** Washington University, St. Louis, Mo., AIAA, AICE, ASME, IEE, ISASC Inc. **Deadline info: (five copies of papers) 10/15/70 to:** Jerome R. Redus, Code S&E-AERO-GT, NASA Marshall Space Flight Center, Huntsville, Ala. 35812; **(one copy ms) 10/15/70 to:** Prof. R. W. Brockett, Pierce Hall, Harvard University, Cambridge, Mass. 02138.

SEPT. 6-10, 1971: **4th IFAC Symposium on Automatic Control in Space,** Dubrovnik, Yugoslavia, International Federation on Automatic Control. **Deadline info: (five copies of abst) 9/30/70 to:** Dr. J. A. Aseltine, University of Southern California, Electrical Engineering Department, University Park, Los Angeles, Calif. 90007.

SEPT. 19-22, 1970: **Joint Power Generation Technical Conference,** Chase Park Plaza Hotel, St. Louis, Missouri, G-P, ASME, ASCE participating. **Deadline info: (papers) 5/7/71 to:** R. L. Colt, Westinghouse Elec. Corp., Lester PO, Philadelphia, Penna. 11913.

SEPT. 27-30, 1971: **1971 IEEE Conference on Underground Distribution,** Hotel Pontchartrain and Cobo Hall, Detroit, Michigan, IEEE. **Deadline info: (abst) 9/30/70 (papers) 3/1/71 to:** Technical Program Chairman, B. E. Smith, Virginia Electric and Power Company, P.O. Box 1194, Richmond, Virginia 23209.

Meetings

NOV. 3-6, 1970: **Basic Science and Nuclear Divisions Joint Fall Meetings,** Riverside Motor Lodge, Gatlinburg, Tennessee, The American Ceramic Society, Inc. **Prog info:** Paul J. Jorgensen, Program Chairman Basic Science Division, 1970-71, Stanford Research Institute, 333 Ravenswood Avenue, Menlo Park, California 94025 and W. Richard Jacoby, Program Chairman Nuclear Division, 1970-71, Westinghouse Electric Corporation, P.O. Box 217, Cheswick, Pennsylvania 15024.

NOV. 4-6, 1970: **Northeast Electronics Research & Engineering Meeting,** Sheraton Boston Hotel & War Mem. Aud., Boston, Mass., New England Sections. **Prog info:** IEEE Boston Office, 31 Channing St., Newton, Mass. 02158.

NOV. 4-6, 1970: **Nuclear Science Symposium,** Statler Hilton Hotel, New York, N.Y., G-NS, NASA, AEC, NBS. **Prog info:** W. W. Managan, Argonne Nat'l Lab., Argonne, Ill. 60440.

NOV. 9-12, 1970: **16th Annual Holm Seminar on Electrical Contact Phenomena,** Illinois Institute of Technology, Chicago, Ill., IIT, IIT Research Institute. **Prog info:** Dr. Ralph E. Armington, Illinois Institute of Technology, 330 S. Federal St., Chicago, Ill. 60616.

NOV. 12-13, 1970: **Canadian Symposium on Communications,** Queen Elizabeth Hotel, Montreal, Quebec, Canada, Canadian Region, Montreal Section. **Prog info:** IEEE Office, Technical Activities Board, 345 East 47th Street, New York, N.Y. 10017.

NOV. 12-13, 1970: **Symposium on Man-Machine Systems,** Langford Hotel, Winter Park, Florida, G-MMS, Orlando Section. **Prog info:** M. J. Kahn, AA1 Corp., Cockeysville, Maryland 20130.

NOV. 15-19, 1970: **Engineering in Medicine & Biology Conference,** Washington Hilton Hotel, Washington, D.C., G-EMB, AEMB. **Prog info:** Richard Johns, 522 Traylor Bldg., Johns Hopkins School of Med., Baltimore, Md. 21205.

NOV. 17-20, 1970: **Magnetism & Magnetic Conference,** Astro Hall, Houston, Texas, G-C, AFIPS. **Prog info:** L. E. Axsom, IBM Scientific Ctr., 6900 Fannin, Houston, Texas 77025.

NOV. 17-20, 1970: **Magnetism & Magnetic Materials Conference,** Diplomat Hotel, Hollywood Beach, Florida, G-MAG, AIP. **Prog info:** F. B. Hagedorn, Bell Telephone Labs., Murray Hill, New Jersey 07971.

DEC. 2-3, 1970: **Conference on Display Devices,** United Engrg. Ctr., New York, N.Y., G-ED. **Prog info:** IEEE Office, Technical Activities Board, 345 East 47th Street, New York, N.Y. 10017.

DEC. 2-4, 1970: **Vehicular Technology Conference,** Statler Hilton Hotel, Washington, D.C., G-VT. **Prog info:** IEEE Office, Technical Activities Board, 345 East 47th Street, New York, N.Y. 10017.

DEC. 6-9, 1970: **National Electronics Conference,** Conrad Hilton Hotel, Chicago, Illinois, Region IV, Illinois Inst. of Tech., Univ. of Ill. et al. **Prog info:** Nat'l Electronics Conf., Oakbrook Exec. Plaza #2, 1121 W. 22 St., Oal Brook, Ill. 60521.

DEC. 7-9, 1970: **Adaptive Processes: Decision & Control Symposium,** Univ. of Texas, Austin, Texas, G-AC, G-IT, G-SSC, Central Tex. Sec., Univ. of Texas. **Prog info:** D. G. Lainiotis, Elec. Res. Ctr., Univ. of Texas, Austin, Texas 78712.

DEC. 9-11, 1970: **Conference on Applications of Simulation,** Waldorf Astoria Hotel, New York, N.Y., G-C, G-SSC, AISC, Inc., IMS, SHARE. **Prog info:** IEEE Office, Technical Activities Board, 345 East 47th Street, New York, N.Y. 10017.

DEC. 14-16, 1970: **Intl Symposium on Circuit Theory,** Sheraton Biltmore Hotel, Atlanta, Georgia, G-CT. **Prog info:** Ivan Frisch, Network Analysis Corp., Beechwood, Old Tappan Road, Glen Cove, N.Y. 11542.

JAN. 12-14, 1971: **Hawaii Int'l Conference on System Sciences,** Univ. of Hawaii (Moana Hotel) Honolulu, Hawaii, Univ. of Hawaii, G-AC, G-IT, Hawaii Section, SIAM et al. **Prog info:** Rahul Chattopadhyay, Univ. of Hawaii, 2565 The Mall, Honolulu, Hawaii 96822.

JAN. 12-14, 1971: **Symposium on Reliability,** Sheraton Park Hotel, Washington, D.C., G-R, ASQC, ASNT, IES. **Prog info:** J. W. Thomas, Vitro Labs., 14000 Georgia Ave., Silver Spring, Md. 20910

JAN. 23-25, 1971: **Fifty-fourth Annual Meeting,** Atlantic City, New Jersey, The Mathematical Association of America. **Prog info:** A. B. Willcox, Executive Director, The Mathematical Association of America, Inc., 1225 Connecticut Avenue, N.W., Washington, D.C. 20036.

JAN. 31-FEB. 5, 1971: **Winter Power Meeting,** Statler Hilton Hotel, New York, N.Y., G-P. **Prog info:**IEEE Hdqs., Tech. Conf., Svcs., 345 E. 47th St., New York, N.Y. 10017.

FEB. 9-11, 1971: **Aerospace & Electronic Systems Winter Conv. (WINCON),** Biltmore Hotel, Los Angeles, Calif., G-AES, L. A. Council. **Prog info:** IEEE Office, 345 E. 47th St., New York, N.Y. 10017.

FEB. 17-19, 1970: **Int'l Solid State Circuits Conference,** Sheraton Hotel, Univ. of Penna., Phila., Penna., SSC Council, Phila. Section, Univ. of Penna., Phila., Phila. Section, Univ. of Penna., **Prog info:** R. W. Webster, Texas Instruments, POB 5012, Dallas, Texas 75222.

Engineering News and Highlights

Defense and Commercial Electronics Groups consolidated

RCA has consolidated its defense and commercial electronics groups to streamline operations and enhance the Company's competitive position in the government and commercial systems markets.

All divisions and operations previously functioning as part of the Defense Electronic Products and Commercial Electronic Systems groups have been combined into Government and Commercial Systems, reporting to **Irving K. Kessler,** Executive Vice President. (See organization chart 1.)

The reorganization also includes the merger of Commercial Electronic Systems and the Defense Communications Systems Division into a new unit of the Government and Commercial Systems group, the Communications Systems Division. The new division will be headquartered in Camden, N. J.; both organizations were previously based in Camden. The Communications Systems Division also has plants in Meadowlands, Pa.; Plymouth, Mich.; and Burbank, Calif. **Andrew F. Inglis,** former head of Commercial Electronic Systems, will direct the new consolidated division as Division Vice President and General Manager. (See organization chart 2.)

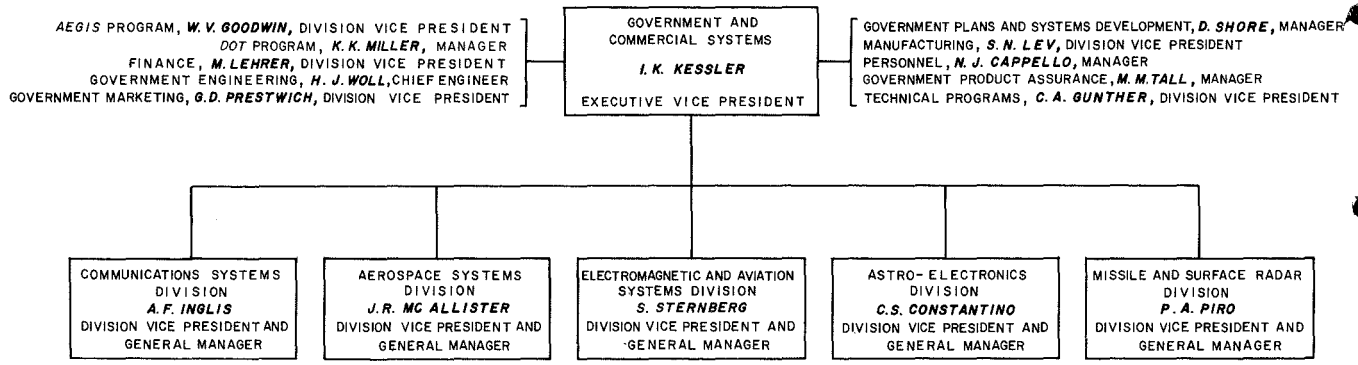
Mr. Kessler said the reorganization will benefit business programs and customers of both RCA's government and commercial electronics operations by facilitating the transfer of capabilities and technologies between the two areas.

"Our government business has expanded to include meeting the needs not only of the Department of Defense and NASA, but also agencies such as the Departments of Interior; Transportation; Justice; Health, Education and Welfare; and Commerce. We believe the requirements of these customers can be best met by a closer association of our defense and space and commercial electronics capabilities.

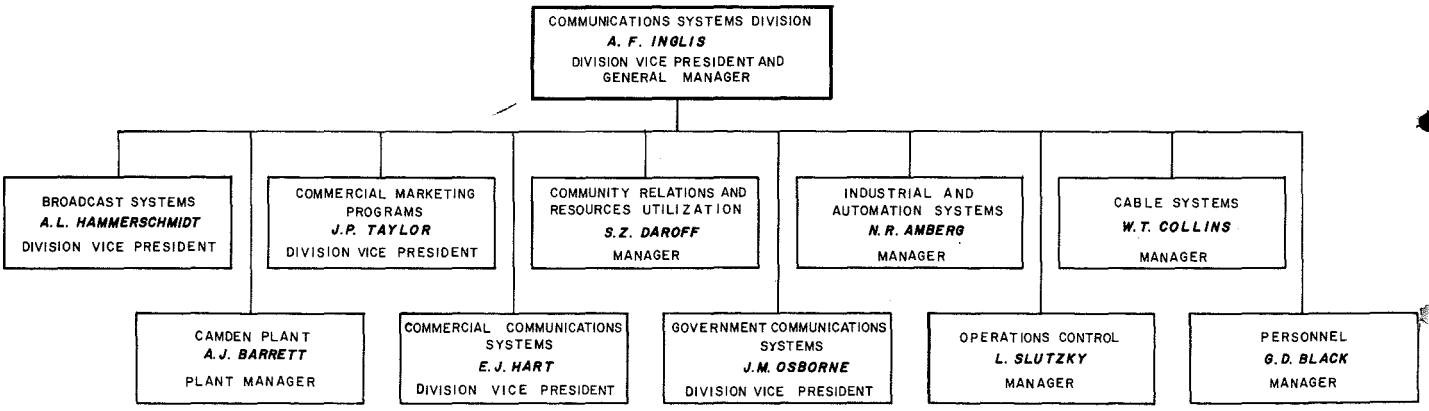
"In the same way, our commercial customers will benefit from the expertise we have developed in advanced design and ultra-reliability as a result of our role in programs such as Apollo," Mr. Kessler explained. The new organization also could expedite the development of new RCA product lines in commercial electronic systems, Mr. Kessler added.

The former Commercial Electronic Systems group is a leading manufacturer of cameras, transmitters, video recorders, and other apparatus for televison and radio broadcasters. It also is a supplier of mobile radios, production line testing and assembly systems, and cable television systems.

The former Defense Communications Systems Division develops communications and electronic systems for military and space applications. It was responsible for the communications for the Apollo Lunar Module moon-landing spaceship and is now involved in a number of new programs to develop advanced airborne, shipboard, and land-based communications systems.



Organization Chart I—Government and Commercial Systems (October 15, 1970).



Organization Chart 2—Communication Systems Division (October 15, 1970).

Staff announcements

Management Information Systems

Lawrence M. Issaacs, Vice President and Controller of RCA, has appointed **Bruce A. Curry,** Staff Vice President, Management Information Systems.

Consumer Affairs

Herbert T. Brunn, Vice President, Consumer Relations, has appointed **B. I. French, Jr.,** Director, Consumer Affairs.

ServiceAmerica

Robert C. Peard has been named manager of ServiceAmerica for the San Francisco Bay Area.

Astro-Electronics Division

Abraham Schnapf, Manager of Program Management has appointed **Lawrence E. Golden** as Manager, Atmosphere Explorer Project.

Aerospace Systems Division

John R. McAllister, Vice President and General Manager, has appointed **Robert C. Kley, Jr.,** as Design Support and Standards Manager.

Missile and Surface Radar Division

Philip A. Piro, Division Vice President and General Manager, has appointed **Dr. Samuel J. Rabinowitz** to the Engineering Staff of the Missile and Surface Radar Division.

Industrial Tube Division

Dr. Eugene D. Savoye, Manager, Advanced Technology, Electro-Optics Products has appointed **Dr. Brown F. Williams,** Manager of the Electro-Optics Laboratory.

Consumer Electronics

Barton Kreuzer, Executive Vice President, has appointed **William H. Anderson,** Division Vice President, Marketing.

RCA Sales Corporation

Barton Kreuzer, Chairman of the Board, has announced that the Board of Directors of the RCA Sales Corporation has elected **William H. Anderson,** President.

Corporate Planning

George C. Evanoff, Vice President, Corporate Planning has appointed **Norman Racusin,** Staff Vice President, Operations Planning.

Computer Systems Division

Joseph W. Rooney, Division Vice President, Marketing, has announced the Marketing organization as follows: **Paul H. McNamara,** Division Vice President, Central Region, **Larry E. Reeder,** Division Vice President, Marketing Operations Staff.

Joseph W. Rooney, Division Vice President, Marketing has appointed **E. Allen Henson,** Division Vice President, Conversion Programs.

Consumer Electronics Research

Donald S. McCoy, Director, has announced the organization of the Consumer Electronics Research Laboratory as follows: **J. J. Brandinger,** Head, TV Systems Research, **W. J. Hannan,** Head, Electro-Optic Systems Research, **W. D. Houghton,** Head, Consumer Information Systems Research, **J. J. Gibson,** Fellow, Technical Staff, **E. O. Keizer,** Head, Video Systems Research, **J. A. vanRaalte,** Head, Displays and Device Concepts Research.

Educational Development

Gene Wyckoff, Director, Audio-Visual Programs has appointed **Richard K. Swicker,** Manager, Audio-Visual Services.

RCA Institutes, Inc.

Albert L. Baker, President, has appointed **Harold Fezer,** Director, Educational Services, and **F. Robert Michael,** Director, New York Resident School.

Solid State Division

William C. Hittinger, Vice President and General Manager, has appointed **D. Joseph Donahue,** Division Vice President, Solid-State—Europe.

Electronic Components

John B. Farese, Executive Vice President, has announced the organization of Electronic Components as follows: **Fred M. Bauer,** Controller, Finance; **Carlos E. Burnett,** Division Vice President and General Manager, Industrial Tube Division; **William C. Dove,** Purchasing Agent; **Gene W. Duckworth,** Division Vice President, Equipment Sales and Distribution; **Arnold M. Durham,** Manager, News and Information; **Leonard Gillon,** Division Vice President and General Manager, Television Picture Tube Division; **Joseph A. Haimes,** Division Vice President, Distributor Products; **Lawrence A. Kameen,** Manager, Personnel; **Clifford H. Lane,** Division Vice President, Technical Planning; **William H. Painter,** Division Vice President, Business and Economic Planning; **Harry R. Seelen,** Division Vice President, International Development and Glass Operations.

Promotions

Aerospace Systems Division

R. W. Toepfer, Jr. from Ldr. to Mgr., Configurations Management (A. Skavicus, Burlington)

R. T. Boyle from Senior Project Member, Tech. Staff, to Ldr., Tech. Staff (K. I. Pressman, Burlington)

Astro-Electronics Division

L. Muhlfelder from Senior Engineer to Mgr., Advanced Stabilization (J. Keigler, Hightstown)

Electronic Components

J. A. Zollman from Engineering Ldr., Prod. Dev., to Mgr., Display Tube Operations (Dr. R. E. Simon, Lancaster)

G. Novak from Senior Engineer to Mgr., Product Engineering (W. E. Breen, Harrison)

H. Donnell from Ldr., Product Development, to Mgr. Manufacturing and Product Engineering (D. Watson, Leige, Belgium)

R. Brown from Ldr., Product Development, to Engineering Mgr., Standards (M. Bondy, Somerville)

Solid State Division

R. A. Donnelly from Mgr., Manufacturing & Production Engineering, to Mgr., Solid State (E. M. Troy, Taiwan)

RCA Service Company

D. W. Dunkle from Engineer to Mgr., Facilities (E. J. Lauden, Andros Ranges, AUTEC Project, Bahamas)

W. M. Moore from Engineer to Mgr., Education & Training (R. Dunn, New York Residential Manpower Center, New York)

Electromagnetic and Aviation Systems Division

A. Gattuso from Prin. Member of D&D Engrg. Staff to Ldr., D&D Engrg. Staff (H. Hite, Van Nuys)

Government and Commercial Systems

W. J. Lawrence from Engineer to Ldr., Design and Development (J. B. Howe, Jr., Digital Communications Equipment, Camden)

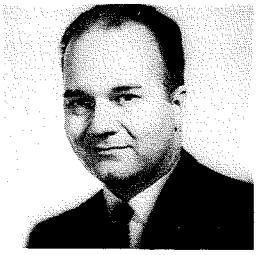
Computer Systems Division

D. J. Mackson from Ldr. to Mgr., Sys. Control and Support (N. N. Alperin, Palo Alto)

AED Engineers receive NASA award

James S. Douglas and **Arnold S. Cherdak** of the Astro-Electronics Division were honored with awards by NASA for inventing the Maximum Power Point Tracker.

The awards were presented by **Dr. Warren Manger,** Chief Engineer, at a special luncheon held at RCA's Space Center. Also in attendance were **C. S. Constantino,** Division Vice President and General Manager; **Abraham Schnapf,** Manager, Program Management; **Robert Miller,** Program Manager of NIMBUS Project, and Robert House, Manager of Advanced Planning.



Bill Rolke is new TPA for CSD, Marlboro

William Rolke has been appointed Technical Publications Administrator for the Computer Systems Division at Marlboro, Mass. In this capacity, Mr. Rolke will be responsible for the review and approval of technical papers; for coordinating the technical reporting program; and for promoting the preparation of papers for the *RCA Engineer* and other journals, both internal and external.

Mr. Rolke, presently a Principal Member of the Technical Staff, Computer Systems Division, has been with RCA since 1948 when he joined the Advanced Development Group of the then Military Electronics Section. Since that time he has worked on the mechanical design of equipments, both military and commercial. He has worked for the last three years in the Standards and Design Integration Group of CSD. His duties included chairmanship of design reviews and interpretation and generation of standards at the Marlboro facility during its early growth stages. Mr. Rolke has served on the Corporate Gear Committee and on the Reliability Committee of Environmental Testing, True Positioning Toleancing Standards Committee and Cost Improvement Design Program. Prior to joining RCA, Mr. Rolke was engaged in the design and testing of equipment for the Navy Research Project "Ekyhook", a study of high altitude cosmic rays. Mr. Rolke entered the Army in 1942 as a Chemical Warfare Decontamination Specialist and served in the European Theater of operations with the 44th Infantry Division. He is a graduate of the University of Minnesota and a member of Chi Epsilon honor society. He has two US patents.

Professional activities

Corporate Engineering Services

Raymond E. Simonds, Director, RCA Frequency Bureau, has been elected President of the *Comite International Radio-Maritime* (CIRM). The organization is composed of over 40 companies from 19 countries and studies technical matters of concern to the International Maritime Radio Services. CIRM is recognized as a specialized international organization by the International Telecommunications Union and the Intergovernmental Maritime Consultative Organization. In this capacity CIRM regularly participates in international conferences providing opinions and recommendations formulated on the basis of specialized knowledge in the maritime field. Mr. Simonds is the first representative of a United States company to be elected President since the CIRM was formed in 1928.

Astro-Electronics Division

A. Baran has been appointed Chairman of the DEP Subcommittee on Computer Applications in Calibration of Test Equipment.

Jess Epstein is new Ed Rep for Patents and Licensing

Jess Epstein has been appointed for Editorial Representative Patents and Licensing. In this capacity, Mr. Epstein is responsible for planning and processing articles for the *RCA Engineer,* and for supporting the Corporate-wide technical papers and reports program.

Mr. Epstein received the EE and MS in Physics from the University of Cincinnati in 1932 and 1934. In 1935, he joined the Research Division of RCA at Camden. Since then, he has held the following assignments: Research Division of RCA Manufacturing, 1935-42; RCA Laboratories, 1942-1961; Missile Surface and Radar Division 1961-1967; Corporate Staff, Research and Engineering, 1967-1968; and Corporate Staff, Patents and Licensing, 1968 to date. During this period he has specialized in electromagnetic propagation and radiating systems, Mr. Epstein is a Senior Member of the IEEE and a Member of Sigma Xi.

J. J. Surina's paper voted best in session

John J. Surina, of Data Processing Engineering, Missile and Surface Radar Division, Moorestown, N. J. presented a technical paper, "Trade-Offs in High Speed Computer Interconnections," that was chosen as the best in its session by attendees at the recent National Electronics Packaging Conference (NEPCON West-Conference).

Mr. Surina received the BSEE from Syracuse University, where he achieved membership in the Mathematics and Electrical Engineering Honorary Societies (nationally affiliated with Pi Mu Epsilon and Eta Kappa Nu). He was affiliated with the Microcircuits Engineering Activity before transferring to his present group. He is assigned to the AEGIS-MEAR program.

Mr. Surina has been with RCA for over 19 years, the last half of which has been devoted to work involved with the packaging of high speed digital systems. During this period, he has investigated in depth the use of printed circuits for controlled impedance interconnections, conducting analytical studies and developing experimental data to establish valid and practical guidelines for application of transmission line interconnections to current and future equipment designs.

RCA Review, June 1970
New Process Technologies for Microelectronics

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