The Challenge of The Computer Business

The nature of the computer business is to solve each customer's needs with a system best suited to his requirements. How well this can be done over a large number of customers determines the competitiveness of a product line. It is Engineering's role to design a range of compatible data processing equipments which can be combined to achieve a wide spectrum of competitive systems.

This broad spectrum of product line systems capability requires that a variety of different kinds of equipment be designed involving a number of technical disciplines such as displays, complex precision mechanisms, digital and integrated circuits, plated wire memories, logic design, and programming. Technology improvements have been and will continue to be rapid. It is almost a truism in the business that the cost/performance ratios improve by a factor of 2 every 2½ years.

Future emphasis will be on system throughput as measured by the combined effectiveness of the hardware and the software. To preserve the investment in existing customer programs, the new system must be compatible with the old, yet still offer major improvements not only in basic raw performance but in new system capabilities; e.g., "graceful degradation" when used in multiprocessor environments. Continued emphasis will be needed to broaden the base of peripheral equipments with major attention directed towards lower cost, remote terminals, and random-access file memories. According to estimates, peripherals will represent 80% of the typical EDP system cost in the 1970's. Since industry will depend more on computer systems as an integral part of their operations, so it goes that the reliability levels of these systems must be pushed higher and higher.

Very briefly, this is the nature of the computer business, whose growth rate will be maintained through the next decade. The engineering challenge and opportunities look as exciting and rewarding as those now behind us.

A. D. Beard
Chief Engineer
Information Systems Division
Cherry Hill, New Jersey

Our cover
From the computer control panel on the front cover to the new Spectra panel on the back cover, the composite cover strongly suggests computer design—this issue's theme. Appropriately, the background is one of the Spectra printed-wiring boards which interconnects much of the processor logic. In another segment of our back cover, Gus Gaschnig of ISD Engineering compares the older types of interconnecting cables (left) with the new flat-cable design (right). **Photo credits:** W. Eisenberg, DCSD Photo Lab., Camden, N.J.

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• To disseminate to RCA engineers technical information of professional value • To publish in an appropriate manner important technical developments at RCA, and the role of the engineer • To serve as a medium of interchange of technical information between various groups at RCA • To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions • To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field • To provide a convenient means by which the RCA engineer may review his professional work before associates and engineering management • To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

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editorial input

a benevolent thief

Anyone over 30 has lived through the age of the computer. Computer technology, as we know it, started in 1937 with the relay-type sequence-controlled calculator built by Howard Aiken, a Harvard professor and IBM engineers. This was followed in 1942 by ENIAC (Electronic Numerical Integrator and Calculator) designed and built by Eckert and Mauckley of the University of Pennsylvania. ENIAC used electron tubes and was the first truly high-speed computer (albeit painstakingly slow by today's standards). ENIAC was followed rapidly by several larger-scale machines of the same genre —TRANSAC, MANIAC, SINAC, UNIVAC, and BIZMAC.

Starting with BIZMAC—one of RCA's early entries — computer history closely parallels RCA's own story in this field (see Brian Pollard's article in this issue). In three short decades, the computer has come from ENIAC's brute-force concepts to Spectra's sophisticated operating systems. This recent and rapid progress, however, tends to obscure the computer's time-worn roots in mathematics, engineering, the physical sciences, and accounting.

Over 100 years before our Declaration of Independence, the first clear picture of the computer's mathematical principles was developed by Gottfried von Leibniz, a German philosopher, mathematician, and writer. By the time of our Civil War, all of the principles of symbolic logic used in today's computers had been well-defined by an English mathematician—George Boole.

Likewise, the principles of computing machinery have been with us for many years. The first crude attempts were made by the Egyptians who used the abacus to aid in business transactions over 400 years before Christ.

Several decades before the Puritans started on their voyage to gain religious freedom in the new world, John Napier had already devised a system for multiplying by using numbered rod's (Napier's bones); Napier's system also laid the groundwork for the first analog computer—the slide rule. In 1642, Blaise Pascal built a computing machine using numbered wheels; the most important concepts embodied in Pascal's machine were the carry-over of digits from one column to the next and the process of multiplication by successive additions.

By the 19th century, Burkhardt in Germany, Odhner in Sweden, and Burroughs in America were marketing computing machines. The first true precursor of the modern computer, however, was Charles Babbage's "analytical engine". Built in 1833, this machine embodied the concepts of programming, data storage, and punched-card input (using both control and data cards).

The use of punched-cards for data and control had been well developed before Babbage's time. A Frenchman, J. M. Jacquard, had used them in the textile industry to control complex loom operations. Punched cards were introduced in accounting operations by Hollerith, an American, in the early 19th century.

Thus, computer technology has taken heavily from the past—*but it has been a benevolent thief.* It has given back much more than it has taken, not only to the mathematicians and the engineers who made possible its development, but to all professions. In science, medicine, business, and education, the computer is no longer simply a tool—it is a way of life.

Future Issues

The next issue of the *RCA Engineer* discusses product and system assurance, reliability, and value engineering. Some of the topics to be covered are:

Product assurance concepts

Standardization

Concepts of value engineering

Reliability

System assurance techniques

Maintainability

Quality costs

Customer satisfaction

Discussions of the following themes are planned for future issues.

Microwave devices and systems

Interdisciplinary aspects of modern engineering

RCA engineering on the West Coast

Linear integrated circuits

Consumer electronics

Computerized educational systems

RCA computers: a technical review and forecast

B. W. Pollard

No review of computers, either in the data processing world at large, or within RCA, can cover all facets. It is therefore the object of this review to focus upon the primary purpose of the computer in the RCA market environment, to discuss how that purpose has been fulfilled in the past and the present, and to forecast future trends.

The Engineer and the Corporation

Brian W. Pollard, Mgr.
Engineering—Camden
Information Systems Division
Camden, N.J.

received the BA and MA in natural and mechanical sciences from Clare College, Cambridge in 1944 and 1948. He joined RCA in January 1966 as manager of product planning for EDP. He was appointed to his present position in June 1967. Prior to joining RCA, he was with Burroughs Corporation from 1959 where he was director of engineering—data processing, and manager, data processing activity. From 1948 to 1959 he was with Ferranti, Ltd., England, and held the position of manager, computer department. He was chief US delegate to the first three international data processing standards conferences (1961, 1962, 1964); technical program chairman for the spring joint computer conference in 1963; and general conference chairman for the SJCC in 1967. He has nine patents issued, and is a senior member of the IEEE, and member of the IEE (UK).

ALTHOUGH THERE IS A SIGNIFICANT OVERLAP, the two major applications of computers can be characterized as *commercial* and *scientific*. The major market is the commercial one, covering the private and governmental enterprises of the country. Less than 20 years ago the first commercially built computers were delivered to customers. Today over 30,000 computers are integrated into the day-by-day operations of industry, commerce, and the government.

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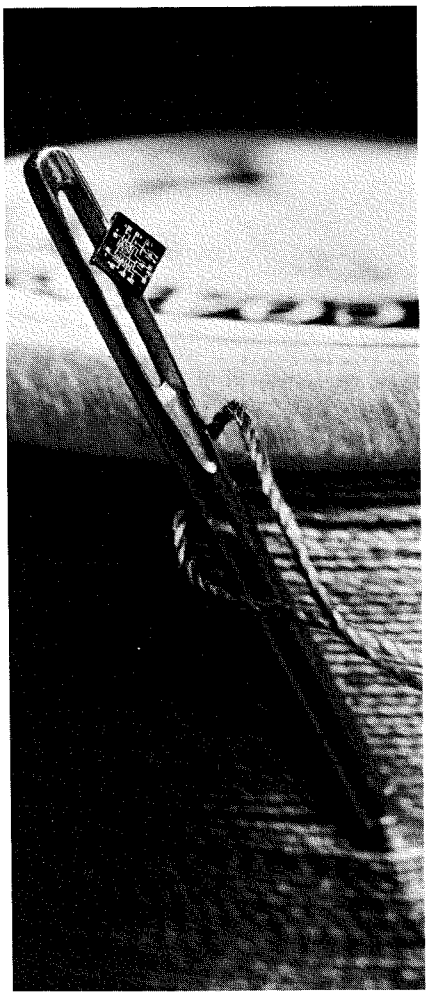
System emphasis

In the past, and still today to a degree, computers have been announced, and sold, on the basis of the technologies employed, the circuit speeds achieved, the construction techniques adopted, and so on. Today, and more so in the future, the emphasis is upon the capability of the *system* to do the tasks the customer requires to have done. It is at this point that the careful use of the word *system* rather than *computer* must be explained. By system we mean the total complex of hardware, software, and human operations that is required to function as an entity to perform the required tasks. It is this system, or at least the hardware and software components of it, which the customer expects to receive from the manufacturer.

First generation

It is then in this context of commercial systems that this review of RCA work will be made. In 1950, RCA undertook a study of market areas related to data processing and identified a need for a large commercial data processing system structured around the commercial needs for sorting, merging, deleting or extracting data, together with manipulation and decision making. Accordingly RCA undertook the development of such a system for the Army Tank and Automotive Command. BIZMAC was, of course, a tube machine and was also the largest data processing installation delivered at that time (1955). It used 32,000 tubes and 600,000 other components, and yet had a maximum memory size of only 8,000 7-bit words.

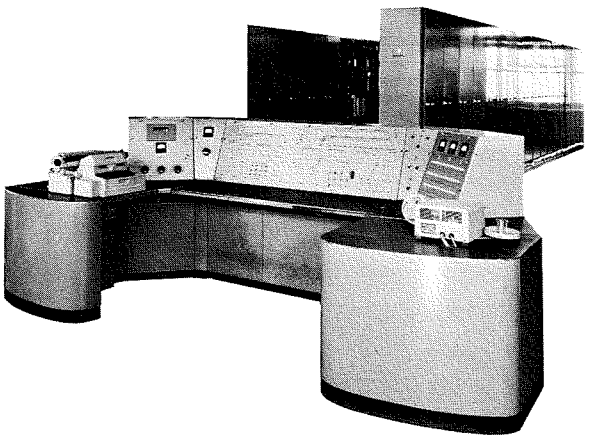
It had, however, many advanced systems concepts:

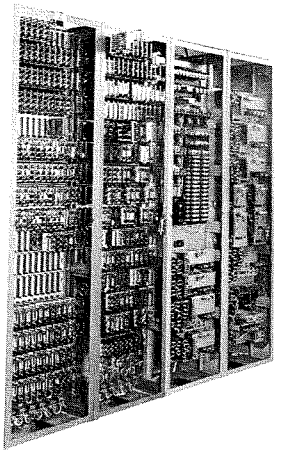


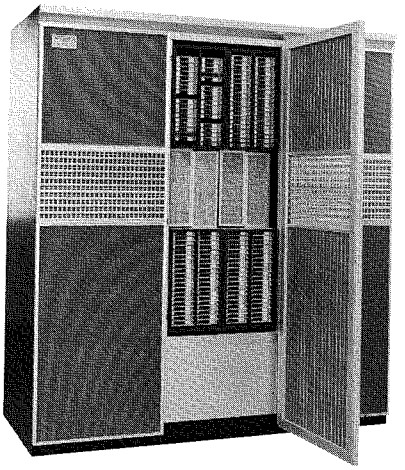
The integrated circuit (above)—being passed through the eye of a needle—contains approximately 15 transistors and 13 resistors. The IC was one of the major reasons for the drastic hardware-size reductions of the third generation computer.

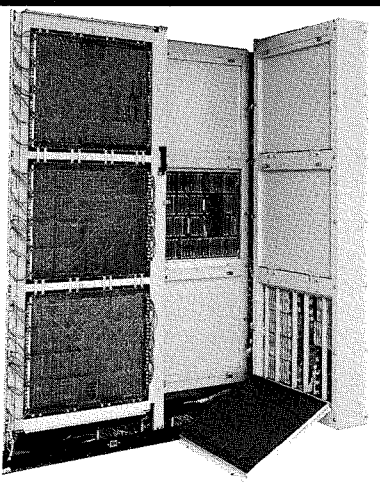
The first commercial variable word length computer;
A powerful and sophisticated set of 3 address instructions;
A unique program library system using magnetic tapes and special tape readers;
A special hand-wired program machine, the Sorter, for file resequencing, instructing, merging, and the like.

As can be seen from Table I, its speed —both circuit and memory—was rela-



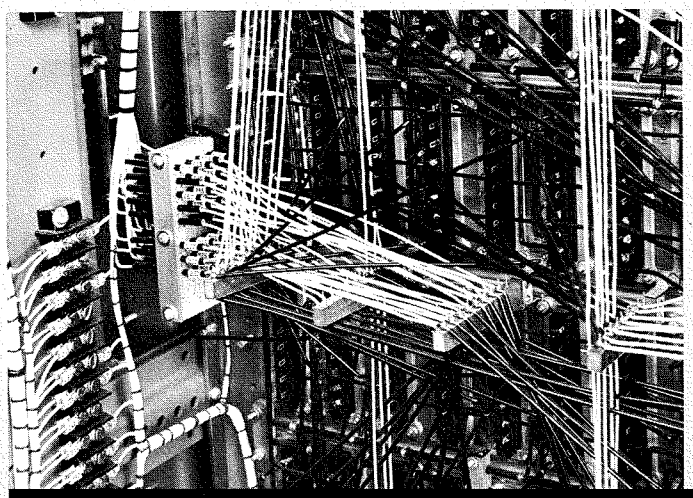


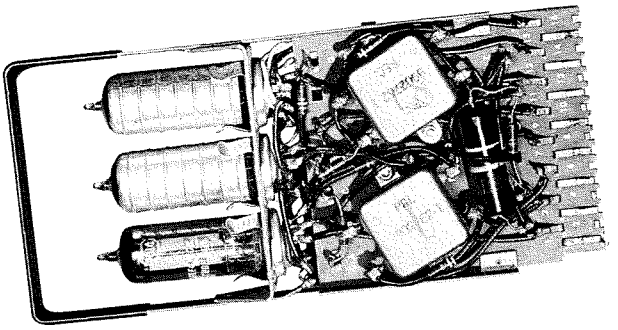


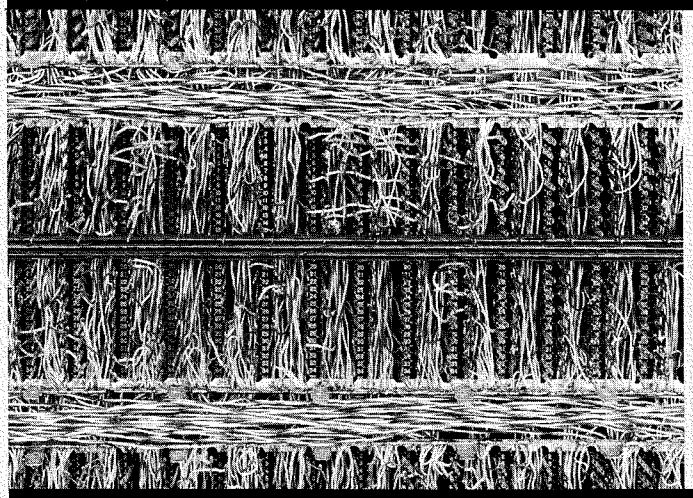


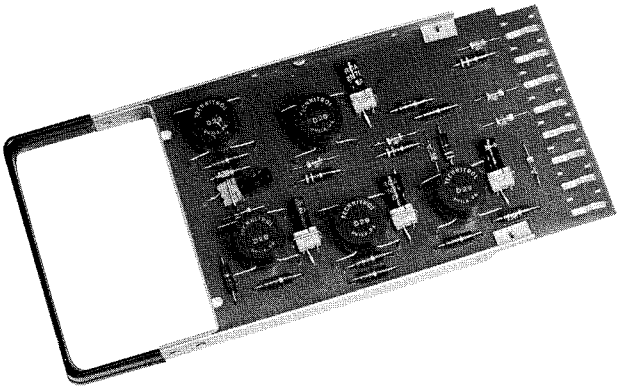
The Bizmac computer (top) was the largest data processing installation in 1955; it had a maximum memory size of 8,000 7-bit words. The RCA-501 (middle) was one of RCA's second generation computers; it was relatively slow but could store up to 262,000 7-bit words. The Spectra 70 (bottom) represented significant advances in the use of operating systems and in compatibility.

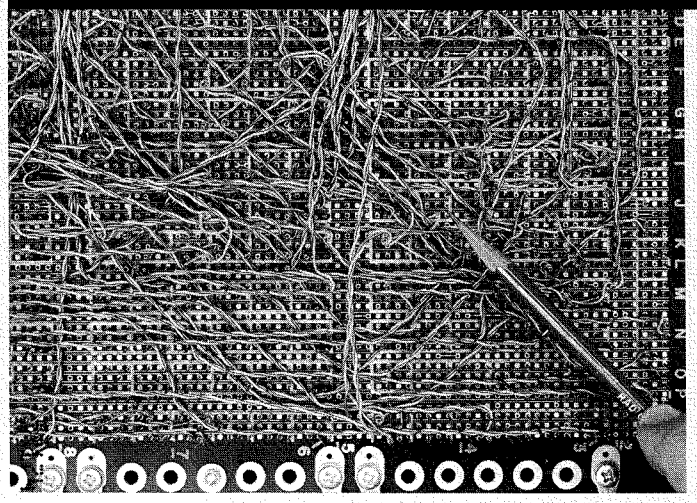
Advances in packaging have been among the most dramatic changes from the first through the third generation: top, Bizmac packaging; middle, RCA 601 packaging; bottom, Spectra packaging.

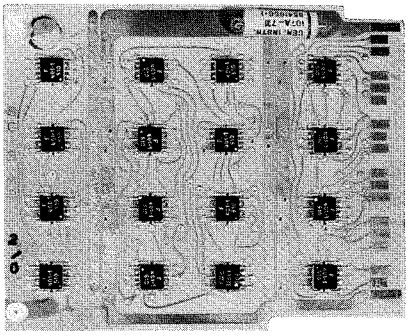












Corresponding to the packaging advances came improvements in wiring from the hard wired Bizmac (top) to the more compact RCA-601 wiring and ultimately to the printed wiring of the Spectra series.

From tubes to transistors to integrated circuits, the module sizes continually decreased and functional sizes increased. At top, the Bizmac tube-type board contains one flip flop; middle, the transistorized RCA-501 board contains about two flip flops; the Spectra board bottom, has about eight flip flops.

tively slow by today's standards, but its capability for data manipulation of all kinds, and the minimized manual intervention, made it, as a system, well ahead of its time. For all its sophistication, it was still a first-generation computer, with programming done at the machine-code level; this allowed the (user) programmer to exploit the idiosyncrasies of the hardware, but of course severely limited the magnitude of the programs which could reasonably be written.

A later version of BIZMAC permitted sorting to be performed on the main processor, rather than on specialized hardware. Also some simultaneity of I/O operations with internal operations was provided for, although this had to be optimized in detail by the programmer.

Second generation

The second generation of RCA equipment consisted of the 501, 301, and 601 in order of announcement. Second generation equipment is usually characterized as that which started to use semiconductors rather than tubes. However, there was another and important characteristic—the development and use of software which was somewhat more remote from the *machine code* of earlier systems. Procedure-oriented languages started to be used, and a wider variety of service programs were developed, including ones which permitted automatic execution from one job to another, and assignment of peripheral devices. Also during the second generation, problem-oriented languages began to be developed; one of the earliest COBOL compilers was developed by RCA.

The 501 was relatively slow, but it did allow for a large core store (up to 262,000 7-bit words) and it was the first commercially delivered transistorized computer. The 301, which came two years later, had very significant performance increases and had a characteristic which contributed significantly to its long life and popularity. It was the first computer to be designed with a generalized interface which simplified the design of electronics to attach literally any kind of peripheral equipment. Earlier systems had always required major surgery if a new peripheral device was to be added after the design had been completed.

The 601 was planned to provide a system which was somewhat more oriented to the scientific world in that it provided powerful computational capabilities. In addition it utilized an interrupt scheme and provided multiprogramming capabilities.

The RCA 3301

Between the second and third generation, RCA developed a system which combined many of the characteristics of the 301/501 class and the 601 into one system, the 3301. This system was provided with major software support in the area of languages, service programs and operating systems.

Third generation

The third generation of equipment has been variously defined, but the salient characteristic of these systems is their use of sophisticated operating systems that allow the user programs to be essentially decoupled from the specific hardware in use. The user is able to develop his programs in a high level language, such as COBOL or FORTRAN and then have these programs compiled and executed on systems appropriate to his needs. This decoupling from the hardware would be significantly more difficult if, as in the past, every computer had been designed as a unique, free standing device. Hence, another characteristic of the third generation, with some manufacturers at least, has been the adoption of the concept of compatibility. This concept requires that systems with a range of performance (speed) shall have essentially identical characteristics. Hence operating systems (and compiled programs) may be run without modification on systems within the compatible family.

The Spectra 70 family is, of course, a compatible family of systems, with, in addition a very significant degree of compatibility with RCA's major competitor—the IBM system 360. This compatibility with system 360 does not extend to all of the features which are used only by the operating systems. Thus there is no interchangeability of operating systems, but user programs may be compiled and executed under the operating systems of either family. This form of compatibility means that any comparison of system performance must take the operating system into account, as well as the circuit and memory speeds of the computer. There is therefore another dimension, software, in any table of competitive performance. So far, with the Spectra 70 family, not only has each member of the family outperformed the equivalent member of the competitive family, but each of the RCA operating systems has been more efficient and hence faster than those of the competition.

When the Spectra 70 family was last discussed in the RCA ENGINEER (Volume 11, No. 3, October/November 1965) the family consisted of the 15, 25, 45 and 55 with the 70/35 announced just as that issue was going to press. Since then, the Spectra 70 time sharing system (70/46) has been announced and production units delivered; also, there has been a significant increase in the maximum data rate for the selector channels of the 70/45.

This review began with a discussion of the commercial market and its implications. How have the RCA systems fitted into this market, and what is the future?

RCA equipment today

The second generation was a learning period. A large number of computers (probably 20,000) was built and installed and users became accustomed to having their computer systems intimately (and intricately) involved in their day-to-day operations. However, in general, each job was run separately and distinctly from each other job, and the total workload was accomplished by the use of multiple systems, each handling a given number of tasks. Since no integration between these tasks was possible, there was wasteful duplication and overlapping. Furthermore, programming in relatively elementary and unsophisticated languages made the development of lengthy programs difficult and time consuming, and modifications (by anyone other than the original programmers) virtually impossible. The RCA systems were in line with the general trend during this period, and the 301 particularly may be counted as a very successful system. In the second generation, sophisticated users recognized the

Table I—Chronology of RCA computer systems developments.

Computer	*Date announced*	*Circuit speed (ns) and type*	*Memory cycle time (μs)*	*Size range (bits per word)*
BIZMAC	Nov. 1955	250 diodes/tubes	20	4-8 K/7
501	Feb. 1958	1,000 resistor/transistor	15	16-262 K/7
301	Feb. 1960	230 diode/transistor	7	10-40 K/7
601	Feb. 1960	90 diode/transistor	1.5	8-32 K/56
3301	Feb. 1963	50 diode/transistor	1.5	40-160 K/7
70/15	Dec. 1964	60 diode coupled nand	2.0	4-8 K/8
70/25	Dec. 1964	60 diode coupled nand	1.5	16-65 K/8
70/35	July 1965	24 emitter coupled current mode	1.44	32-65 K/8
70/45 I	Dec. 1964	24 emitter coupled current mode	1.44	65-262 K/8
70/45 II	Mar. 1968	24 emitter coupled current mode	1.44	65-262 K/8
70/46	Apr. 1967	24 emitter coupled current mode	1.44	262 K/8
70/55	Dec. 1964	24 emitter coupled current mode	0.84	65-524 K/8

weaknesses of the relatively simple systems that were available, and looked for an integrated system which could truly perform all of the tasks required. The third generation, with its emphasis on operating systems, went a substantial way to meet this need.

Operating systems

The Spectra 70 systems currently have six announced operating systems: POS (Primary Operating System), TOS (Tape), DOS (Disc), TDOS (Tape-Disc), MCS (Multi-channel Communications System), and TSOS (Time Sharing). Each of these operating systems should (and must) be considered the equivalent of a major hardware product. It requires many man years of development; it must be very thoroughly tested prior to release; it must be very well documented, not only for the users, but also for those who come later and may wish to make modifications. Because of its complexity, and in spite of prior testing, errors are sure to be discovered in use; these must be corrected and the operating system updated. It should come as no surprise to note that there are approximately as many Systems Programmers as there are Design Engineers in the Information Systems Division.

As indicated earlier, these operating systems have been shown to perform very competitively and they, in conjunction with the Spectra 70 hardware, have provided a solid base for rapid growth.

Communications capabilities

In meeting the user's need for an integrated system, in addition to being able to readily run multiple tasks or jobs and easily reassign peripheral devices from job to job, a communications capability is of major importance. The Spectra 70 family, with its 70/668 Communications Controller-Multichannel has been shown to have great capability in this area. The combination of RCA's excellent reputation in the communications field and the capabilities of Spectra 70 has resulted in significant successes. With the users tending more and more to the use of their own, and the common carriers' communication networks, the RCA communication capabilities are proving to be highly competitive.

Future trends

Thus it may be stated that the current RCA systems (hardware and software) are in the very center of the most important trends of third generation requirements. What of the future? Sometimes it is questioned whether there will be a recognizable fourth generation; certainly the traumatic shift from second to third generation, with all of its needs for emulation and reprogramming is not likely to be attempted again. Hence evolutionary steps are the most probable, with significant compatibility being retained. As more users recognize the value of centralized data bases, so will the need for large and economic random access memories grow. Centralized data bases imply a significant amount of centralized computing, if only to keep their data bases updated. Centralized systems also imply complex communications networks, since there can be no justification for such a centralized system if it is to be a bottleneck to the enterprise which uses it. With a centralized data base, inquiries to that data base are to be expected and provided for, since the data base provides the latest and best information that is available. Hence we may expect such a system to be active during the day (11 hours coast to coast) with inquiry-response and vital outputs, and to use the remainder of the 24 hours for updating, data manipulation, and report preparation, to say nothing of inquiry-response from overseas for major international corporations. Thus these systems must be oriented toward large scale data storage, complex communications, time sharing (to allow for complex, as well as simple inquiry-response), and because of the scope of the overall task, be capable of running on a 24-hour, 7-day-a-week basis, with the minimum of human intervention. RCA's experience, technology, and capability provides a strong base for meeting these requirements of the future.

A purview of RCA's computer business

J. J. MacIsaac

Every major division of RCA is involved in some way with the collection, transmission, storage, retrieval, conversion, and analysis of information; therefore, it is not unusual that the Information Systems Division should be largely devoted to the development and installation of computer-communications systems. Also, it is not unusual that the release of the Spectra 70/46 time sharing system and its allied software package, the Time-Sharing Operating System (TSOS), now places the company in a lead position for tomorrow's time-sharing market.

J. J. MacIsaac, Mgr.
Market Planning
Information Systems Division
Cherry Hill, N.J.
received the BS in Marine Engineering and Naval Architecture, the MSE in Systems Engineering from the University of Michigan. Mr. MacIsaac was formerly associated with SCM Corp. in New York for more than four years as Vice President of the Data Processing Systems Division and Vice President of OEM Operations. Prior to that he was Director of Business Planning for the Diebold Corp. for two years. He has also served in management positions with Univac and the Stanford Research Institute. In his present position, Mr. MacIsaac is responsible for all long and short range planning for RCA's computer division.

THIS YEAR, INDUSTRY DOLLAR SHIPMENTS of computer hardware should be slightly greater than in 1968, increasing the cumulative value of systems installed by about 20% a year. An average rate of 15% should continue through the early 1970's, with certain areas of the market expected to expand more rapidly.

Chief among these will be communications and time sharing systems, whose growing popularity reflects a shift on the part of many computer users to combined batch, on-line and time-shared processing. This will generate a need for new equipment—particularly remote terminals and mass storage devices—with a resultant impact on the peripheral systems market.

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A look ahead

Concurrently, about 12% of computers installed around the world are communications-oriented. However, by 1975, 60 to 70% of all installed computers probably will be operating in a communications environment.

Many of these installations will be fourth-generation computers featuring improved third-generation architecture and machine organization. Inexpensive, small CRT display devices will be more readily available, and lower cost typewriter keyboards will permit rapid data entry to the computer plus high-speed information printout.

Fourth generation computers also will surpass current third-generation computers in their ability to unify batch processing and terminal transmission and perform many activities simultaneously.

Businessmen, using desk-top terminals, will query computer system records for needed information, even while the computer is processing engineering equations.

Students, using typewriter and visual display terminals, will answer computer-given questions, even while the computer is preparing next week's education program or producing next semester's classroom schedules.

Housewives, using touch-tone telephones will conduct routine financial transactions (such as, depositing money and paying bills). At the same time, a small numeric printing terminal will provide an instant record so husbands can reconcile these transactions on a daily basis.

Architects, using special graphic display terminals, will design buildings and have the computer automatically transform these designs into materials specifications, even while the computer is producing construction schedules for other buildings.

Doctors, using typewriter terminals to designate patient symptoms, will have the computer diagnose the illness, even while the computer is updating daily hospital records and preparing forms for insurance company submission.

Motor vehicle departments, using sensors placed along major traffic arteries, will have the computer analyze vehicle flow and schedule traffic light changes to achieve optimum vehicle movement.

These and other communications-based procedures even now are possible, many on systems such as the Spectra 70/45. Future communications/processing needs may be more economically handled, however, by time sharing systems such as the 70/46, or by 70/45's programmed for time sharing operation.

Principles of time sharing

Movement to time-shared processing is a natural and logical consequence of improvements in computer capability coupled with man's desire to obtain greater processing power for the dollar.

Time sharing simply means the apparently simultaneous use of a single computer by several users (each user is unaware that there are other users). The user may be a company, a division or branch of a company, an institution,

RCA's new Corporate Information System Center at Los Angeles has the capability for handling inputs from remote card and paper-tape terminals.

a government agency, or even a group of dissimilar organizations requiring access to a central processor. Each user receives a share of time available, and many jobs are performed simultaneously within a time period.

This cooperative use can be achieved in several different manners: by interspersing programs rapidly on one computer; by multiprogramming; or by multiprocessing—using two computers that are joined to permit the sharing of each other's facilities. Multiprogramming enables several jobs to be handled concurrently, and is now considered the basic mode of almost all time sharing systems.

Multiprogramming is done by interleaving programs of the central processing unit, storage, and input/output devices. To do this, the control programs and equipment identify the point at which a problem program being executed must "wait" for the completion of some event. Then the control program begins another processing task that is ready to be executed. After this is accomplished, the control program goes on to something else or goes back to the previous, unfinished program. Since many programs may be in stages of partial completion, successful multiprogramming requires scheduling of levels of priority for the different procedures.

Multiprogramming, of course, has been a feature of some batch processing systems for some time. However, in a batch processing environment one usually thinks of three to six concurrently active operations, whereas in a time-sharing system 30 to 100 operations are considered typical.

In today's time-sharing system, the user also enters commands from a terminal, compared to batch processing where commands typically are entered by paper tape or punched card. This makes the control function more complex, for with terminal input, the system must be capable of accepting the command and giving the user a few hundred milliseconds of processor time. If the user's job is short and finishes in that time, he will receive the answer within seconds at his terminal. But, if the job is not short, time must be allocated for interspersement among other processing jobs so as to achieve rapid job completion.

From this description of time sharing principles, one might conclude that software is the fulcrum of system performance. But remember, in a time sharing system all the special data and commands must be rapidly shuttled between internal and external memories and between processor and input/output terminals. Furthermore, this data must be moved as single packages, and each package must be isolated so that data will not "leak" from one to another and interfere with the solution of another problem.

The best insurance of a marketable time sharing system is one which is engineered to provide full processing flexibility for the least possible dollar investment.

RCA's time sharing position

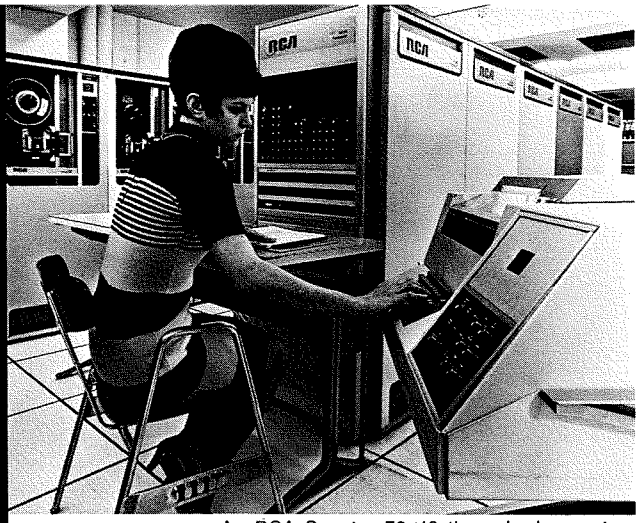
Right now, RCA's Spectra 70/46 stands virtually alone in its ability to provide time sharing with a medium-scale computer. Since its release in 1967, it has come to be known as one of the best time sharing systems in the industry, incorporating features that probably will be included in most future industry time sharing systems.

This year, sales of the Spectra 70/46 will become a significant part of ISD's dollar volume. And, by 1975, it is anticipated that 75% of all sales activity will involve time sharing equipment.

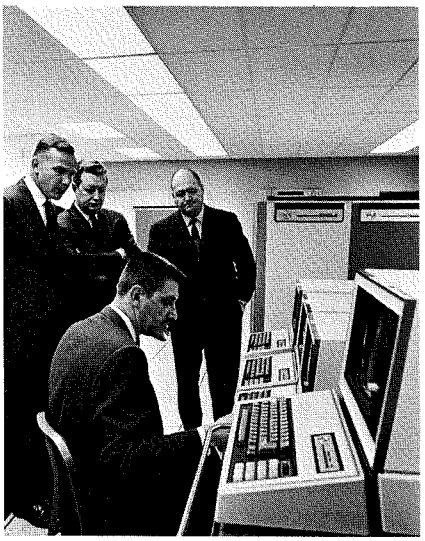
RCA's Time Sharing Operating System (TSOS) also is one of the industry leaders, and of all advanced operating systems probably offers the easiest man-machine interface of any system of equal sophistication. Tsos incorporates a direct access, extended multi-programming capability enabling concurrent local batch processing, remote batch processing, and interactive time sharing from remote terminals. Tsos also is capable of controlling up to 48 terminal users and up to 16 tasks in the background, thus enabling optimum computer utilization with little degradation in response time to terminal users.

Time sharing applications

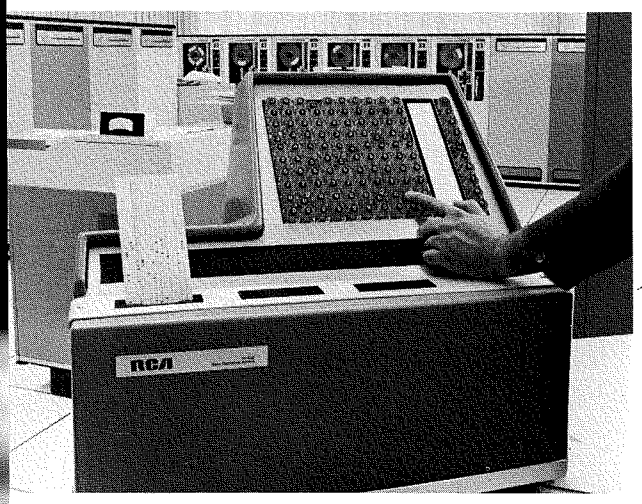
Of the Spectra 70/46 time sharing systems sold last year, applications will be wide and varied. At the Moore



An RCA Spectra 70/46 time sharing system at Cherry Hill, N.J., was linked to a battery of remote video data terminals in RCA's exhibit at the 1968 Fall Joint Computer Conference. This system handles normal batch processing and, at the same time, provides remote terminal services to problem solvers, programmers, and those who seek immediate access to data banks for inquiry and response.



RCA Spectra Video Data Terminals being used by the Crime Information Center in Cincinnati, Ohio.



The RCA Spectra 70 Data Gathering System collects data and transmits it directly to a Spectra 70 computer or to a stand-alone controller for temporary magnetic storage—thus, providing a timely and reliable picture of business activity as it occurs.

School of Electrical Engineering at the University of Pennsylvania, researchers for the first time will have access to a large system that can be exclusively for computer research projects. At this time, these include 35 different procedures, including computerized studies of the human body, computer analysis of electric power systems designed to prevent blackouts, and production of educational films that use animation generated by a computer. Equipment used here includes a 70/568 mass storage unit, two disc drives, and various terminal devices.

For Burlington Industries, Inc., the Spectra 70/46 represents an additional source of revenue. The system, which will be used exclusively by Burlington Management Services Co., a division of the parent company, will provide interactive time sharing and remote batch processing simultaneously for industrial and other BMSC clients.

Work along similar lines also is getting started at Westinghouse Information Systems Laboratory in Pittsburgh, Pa. Here, however, the system will be used for customer numerical control operations.

Westinghouse has used various computers since 1962 to pioneer numerical control (N/C) techniques, including development of the Campoint N/C System—a special corporate software package. With the Spectra 70/46, Westinghouse expects to enhance this program by permitting outside manufacturer utilization and sharing of numerical control experiences.

Beginning this summer, Franklin and Marshall College, located in Lancaster, Pa., will lease its 70/46 to the Middle-Atlantic Education and Research Center, a non-profit corporation composed of six small schools and two research groups within a 100-mile radius of Lancaster. This marks the first time a group of small institutions has banded together as a cooperative to use a sophisticated computer for education and research. Some 35 teletypewriters will be linked to the computer from the various institutions, with the system operating up to 10 hours a day for 8,500 students, faculty, and researchers.

The University of Dayton (Ohio) also will be making available its 70/46 to other colleges who, with Dayton, comprise the Dayton-Miami Valley Consortium. With this $1.5 million installation, research, administrative, record-keeping and academic functions will be handled in a simultaneous batch and remote processing environment.

From these and other imminent installations—Equitable Life Assurance, Connecticut General, Lockheed Aircraft, Owens-Illinois, and others—it is apparent that RCA is off to a solid start in the run for time sharing leadership. But, for this momentum to be continued, constant software improvement and consistent updating of hardware capability will be required.

Future time-sharing requirements

Changes in time shared processing will occur slowly. But they will occur. Tomorrow's systems will have to provide greater power for the dollar. This will require a closer alliance between software and design, thus a greater system's knowledge on the part of engineering.

Reliability will have to be assured, not only in the central processor but in all peripheral devices.

Terminal capability will have to be expanded. Besides visual display and typewriter devices, on-line graphics will be necessary.

Greater simplicity of system operation will be needed to provide faster and more efficient man-machine communication in a variety of unrelated processing environments.

RCA already is striving to meet these requirements—through development of better software procedures; and through total commitment to time-sharing market development.

All companies, of course, are seeking leadership in time sharing systems. And, for the moment at least, it's a wide-open market.

No company, however, or pair of companies, can match RCA's experience in the field of communications. Nor is there a company that can match RCA's experience in electronic display. These two factors, coupled with current Spectra 70/46 success, has to make RCA a leading contender among all computer producers.

Controlling noise in logic circuits

R. G. Saenz | E. M. Fulcher

This paper gives a systematic approach for evaluation and control of logic circuit self-generated noise. The sources of noise are described and the controlling parameters which lead to trade-offs in the summation process are evaluated. Emphasis is placed on the series 1600 computer, which utilizes high-speed TTL integrated circuits. Several new techniques are outlined including methods of treating non-linear transmission line terminations and noise summation techniques to insure operation under worst-case conditions.

THE ADVENT OF LOW-NANOSECOND-LOGIC CIRCUITS has resulted in system noise problems which can cause an otherwise good machine to be useless. Moreover, the problems are constantly being accentuated by the trend toward faster circuits. It is important, therefore, to devise a systematic approach for combating these problems.

Once the circuit configurations are fixed, the most important consideration is designing the system interconnection scheme to control the noise problem.

Noise sources

Externally generated noise

Externally generated noise is partially controlled by defining system environmental requirements and providing the logic circuits with as much shielding as possible. This type of noise will not be dealt with further in this paper; this paper will explore self-generated noise that is produced by various sources within the system.

Self-generated noise

The major types of self-generated noise are:

1) *Reflections:* noise created by discontinuities in signal lines and end-of-line termination mismatches;
2) *Crosstalk:* noise created by inductive and capacitive coupling between signal lines;
3) *Power distribution:* noise created by DC losses, current surges, and supply variations.

Reflections

Line reflections must be considered noise sources when the delay of the line is long compared to the transition time (rise or fall time) of the signal propagating down the line. In short lines, the reflections will not be recognized by the receiving circuits. In such cases, precautions against reflections need not be taken.

Long line reflections may have the following effects on the receiver circuits:

1) The circuit may not switch at the proper time;
2) The circuit delay may be increased; or
3) The circuit may double switch.

A rule of thumb for separating long lines from short lines is: if the reflection at the driving end of the line occurs after the transition has been completed, or if it degrades the transition beyond the point where double switching of a receiver could occur, then the line is long. If the reflection occurs during the normal transition time and does not degrade the normal transition beyond the double-pulse point, it is a short line. Notice that the short-line definition allows some delay increase. The breakpoint in the series 1600 system between long and short lines was two feet. All lines shorter than this were wired for minimum wire length. For lines over two feet, the wiring was controlled to reduce reflection noise. The approach used to derive these controls follows.

End of line reflections

The long line reflection noise from an improperly terminated signal line may be quite severe. The reflection coefficient is:

$$\rho = \frac{Z_L - Z_0}{Z_L + Z_0}$$

where Z_L is the impedance of the load and Z_0 is the characteristic impedance of the line. For $Z_0 = 100\Omega$ and $Z_L = 50\Omega$, the reflection will be one-third the signal swing. When using TTL circuits, the impedance at the end of the signal line is often capacitive with a non-linear resistive element. Both of these factors must be considered in the analysis.

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Edwin M. Fulcher
Circuit Design
Information Systems Division
Palm Beach Gardens, Fla.
received the BSEE from the University of Maryland in 1961. He has completed 30 semester hours of graduate work at the University of Florida in mathematics and electrical engineering. He was employed by the Applied Physics Laboratory of Johns Hopkins University, where he worked on the Polaris navigation system. In 1962, he joined Martin Company of Orlando, where he worked on integrated circuit computer design for the Pershing weapons system. In 1964, he became a member of the circuit design group of ISD in Palm Beach Gardens. He was project engineer of circuit design and wiring rules for the 70/35 and Series 1600 computer systems. Mr. Fulcher has authored four technical papers.

Robert G. Saenz
Circuit Design
Information Systems Division
Palm Beach Gardens, Fla.
graduated from the University of Florida in 1963 with a BEE. He has attended Syracuse University and is presently attending Florida University in pursuit of the MSEE. In 1964 he joined IBM in Poughkeepsie, New York, where he worked on the development and application of high speed hybrid and monolithic logic circuits for the system 360. In 1966 he became a member of the ISD Engineering Staff assigned to the circuit design group in Palm Beach Gardens. His primary responsibility has been in the area of circuit wiring and application rules for the Series 1600 computer system. Mr. Saenz is a member of Phi Kappa Pi and Sigma Tau.

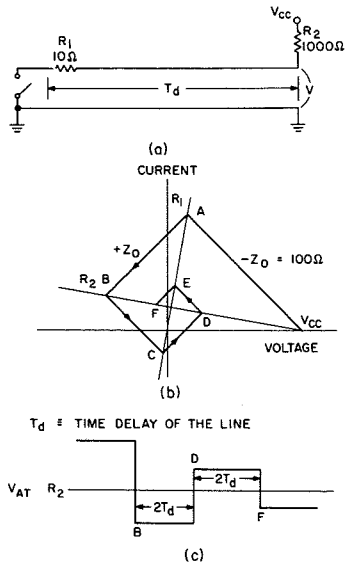


Fig. 1—Method of calculating reflections for a linear resistive termination: a) linear termination; b) graphical method of interpreting the reflections; c) resulting waveform with resistive termination.

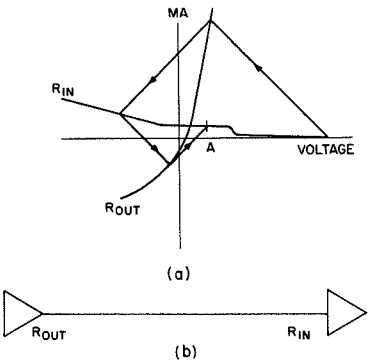


Fig. 2—Application of the graphical solution to non-linear terminations.

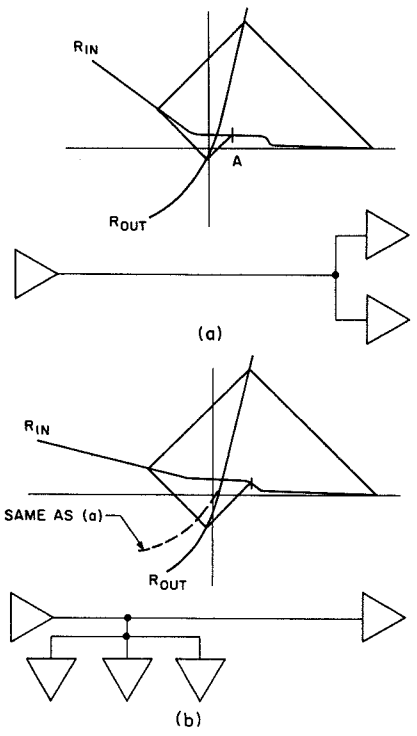


Fig. 3—Variations in the reflections due to a) two loads at the end of the line or b) additional loads at the source.

The method of calculating reflections from lumped capacity is treated later, while a simplified method for analyzing non-linear load impedances is presented here.[1] To illustrate the method, first consider a linear resistance termination (Fig. 1).

The lines R_1 and R_2 are the impedances at the ends of the line. Starting at V_{CC} (the initial state of the line) a line is drawn with a slope of $-Z_o$ until it intersects R_1. Point A is the current and voltage condition at R_1 immediately after the switch is closed. From point A, a line is drawn with a slope of $+Z_o$ until it intersects R_2. Point B is the current and voltage condition at R_2 after the voltage change from V_{CC} to 0V and current change from 0 to V_{CC}/Z_o have traveled to R_2. This is a negative undershoot. The process is continued, and point D is the first positive overshoot, after the reflection has traveled back to the source (point C) and been reflected to the load. This is the noise that could cause a circuit to switch, if it exceeded the noise immunity.

Line attenuation at high frequencies rounds off the corners but is not normally a significant factor in determining the waveform amplitudes.

The graphical method may now be applied to non-linear terminating impedances such as TTL exhibits. The DC input and output impedance curves may be obtained by measurement with a transistor curve tracer and are shown in Fig. 2. The voltage at point A is the first positive overshoot and is the noise of concern.

The advantages of this method now become apparent:

1) The parameters which determined the reflection are immediately obvious and may be controlled by specification. In this case they are the DC resistance of both the input (R_{in}) and output (R_{out}) at negative current and voltage levels. These parameters vary greatly from vendor to vendor and are not normally specified.
2) The effects of altering R_{in} and R_{out} by various loading methods may be analyzed and the worst-cases determined without time-consuming trial and error laboratory setups. For instance, if there were two loads at the end of the line R_{in} would be cut in half as in Fig. 3a, and the reflection reduced. Therefore, one load is the worst-case. However, if there were added loads at the source, then R_{out} would change as shown in Fig. 3b, and the reflection would be worse. Thus, the worst-case is many loads at the source but only one at the end of the line—a condition that is not at all obvious without the graph.
3) Other conditions may be investigated such as various line impedances and load locations.
4) This method may also be applied to a line switching from a low to high signal level.
5) Any circuit configuration may be used.

Distributed load reflections

Distributed loads with capacitive inputs can change the impedance of a transmission line and cause line mismatches. Therefore, it is not sufficient to match line segments to their intrinsic impedances but rather to a range of line impedances that vary with loading. The range of impedance may be controlled by restricting the spacing between loads.

Consider the case shown in Fig. 4. When the input signal is in transition, the load inputs may be represented as in Fig. 5a. This input impedance is approximated by an effective input capacitance (C_x), which is the capacitance which produces the same reflection as the circuit.[2] The transmission line then reduces to that shown in Fig. 5b and the reflections along the line are shown in Fig. 5c. The spacing between the loads must be adjusted to insure that the loaded impedance (Z_L) is not decreased to the point where the mismatch with Z_o will cause a significant reflection.

The following equations (high frequency approximations) determine the minimum spacing (see Figs. 4 and 5):

$$Z_i = \left(\frac{L_i}{C_i}\right)^{1/2} \quad (1)$$

$$Z_L = \left(\frac{L_i}{C_i + C_x/d}\right)^{1/2} \quad (2)$$

$$\rho = \frac{Z_L - Z_O}{Z_L + Z_O} \quad (3)$$

Solving for the minimum spacing yields:

$$d_{min} = \frac{C_x Z_o^2}{\tau_i Z_i}\left[\frac{1}{\left(\frac{1-\rho}{1+\rho}\right)^2 - \left(\frac{Z_o}{Z_i}\right)^2}\right] \quad (4)$$

All of these parameters are determined by the circuit and its environment, except ρ which is the reflection coefficient for the maximum allowable noise. The reflection due to the non-linear resistive element of the input adds to the capacitive reflection and should be

taken into account when the number of loads becomes large. This may be done by reducing the maximum allowable reflection coefficient.

Pedestal reflection

The rise time of a TTL circuit is a function of the load impedance and the source output resistance of the output stage. For very short lines, the voltage will rise directly to the high level. For long lines, the voltage at the output will rise to a level approximated by the voltage divider of the impedance of the transmission line and the source output resistance. This is much lower than the normal high-level. The output will remain at this level until the reflection from the end of the line returns and brings the output to a full high-level. Therefore, TTL circuits depend on the reflection from the end of the line to bring the output to the full high level. This we call the pedestal effect (Fig. 6).

The impedance Z_L must be controlled to insure that the pedestal level occurs above the threshold region of the receivers. This is accomplished by specifying a minimum spacing d between loads on the driven line. The required minimum spacing is:

$$d_{min}=\frac{C_x}{\tau_i Z_i\left(\frac{1}{Z_L^2}-\frac{1}{Z_i^2}\right)} \quad (5)$$

where the minimum value of Z_L is approximated by,

$$Z_L=\frac{V_P\quad \overline{R_O}}{V_{CC}-V_P}$$

and V_P=minimum allowable pedestal level. (This equation is the worst-case since it neglects the small initial load currents).

This creates a second requirement for a minimum load spacing which must be compared to the first (Eq. 4). The condition yielding the largest spacing must of course be used.

Radial line reflections

A signal traveling down a line of impedance Z_o will create a severe reflection when it drives more than one line of the same impedance. In the example shown in Fig. 7,

$$\rho=\frac{Z_L-Z_O}{Z_L+Z_O} \text{ where } Z_L=Z_O/3 \quad (6)$$

or $\rho=-50\%$, and the voltage level will be cut in half. It will remain at this level until the reflections from the radial lines return and allow the signal to reach its full amplitude.

It is therefore apparent that long radial lines should be eliminated allowing only short lines to emanate from a main line. This limits the time duration of the reflection.

Cluster reflections

Clusters are defined as a group of loads within a specified distance on the main line such that they can be considered to act at one point. For a cluster at the end of the line, the transmission line reduces to that shown in Fig. 8a. The waveshapes along the line appear as in Fig. 8b. The reflected voltage V_R (at point A) is:

$$V_R=K\left[t-2Z_oNC_x(1-\exp[-t/Z_oNC_x])\right] \quad 0<t\leq t_1$$

$$V_R=K\left[t_1-2Z_oNC_x\left(\exp\left[\frac{-(t-t_1)}{Z_oNC_x}\right]-\exp[-t/Z_oNC_x]\right)\right] \quad t>t_1 \quad (7)$$

where K is the slope of the input ramp function described in Fig. 9.

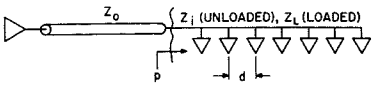
The voltage anywhere along the line is $V_{IN(t)}+\rho V_{IN(t)}$.

The reflection becomes severe as the number of loads increases. These equations neglect the effect on the non-linear resistive element since this is accounted for by the graphical method. In this case the resistive element determines the reflection amplitude after the initial and much larger capacitive reflection.

Crosstalk

The fast rise and fall times of high speed IC's require the use of transmission line techniques for crosstalk evaluation. Mutual capacitance and inductance calculations using lumped parameters are no longer valid since crosstalk waveforms differ at each end of the line. Transmission line crosstalk theory leads to a useful technique.[2] By taking a few simple measurements and applying them to constants, all crosstalk waveforms may be predicted (Fig. 10). The equations for crosstalk are:

$$V_B(t)=K_B\left(\frac{2T_d V_o}{T_R}\right), T_R>2T_d$$
$$=K_B V_o,\ T_R<2T_d \quad (8)$$



DEFINITION OF TERMS:
Zi = INTRINSIC IMPEDANCE OF LOADED SECTION.
ZL = LOADED IMPEDANCE OF LOADED SECTION OF LINE.
Zo = DRIVING LINE IMPEDANCE.
Ti = UNLOADED DELAY OF LOADED SECTION.
Cin = INPUT CAPACITANCE OF CIRCUITS.
Rin = INPUT RESISTANCE OF CIRCUITS.
ρ = REFLECTION COEFFICIENT BETWEEN DRIVING LINE & LOADED SECTION.
d = SPACING BETWEEN LOADS.
C = INTRINSIC CAPACITANCE PER UNIT LENGTH OF Zi.
L = INTRINSIC INDUCTANCE PER UNIT LENGTH OF Zi.

Fig. 4—Impedance may be controlled by restricting the spacing, d, between loads.

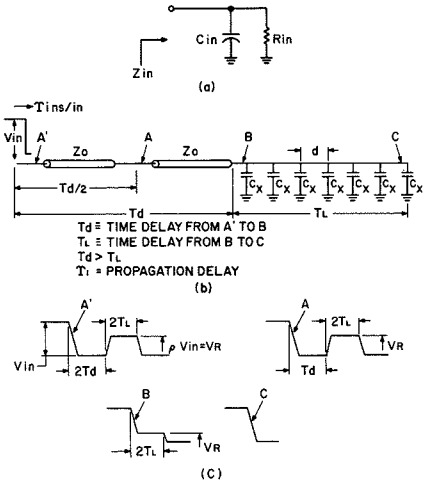


Fig. 5—Analysis of the loading arrangement of Fig. 4: a) load input representation for input signals in transition; b) simplified circuit based on $C_x \cong Z_{in}$; c) resulting line reflections.

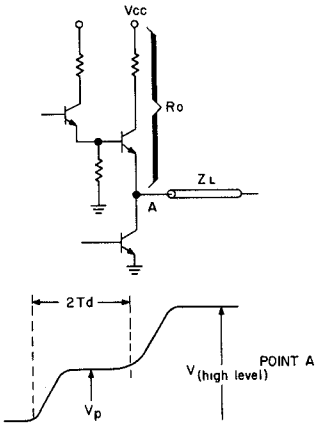


Fig. 6—Pedestal effect.

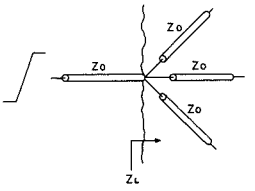


Fig. 7—Transmission line split described by Eq. 6.

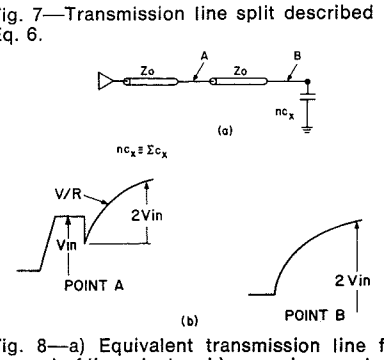


Fig. 8—a) Equivalent transmission line for an end-of-line cluster; b) waveshapes along the line.

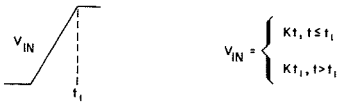


Fig. 9—Input ramp function.

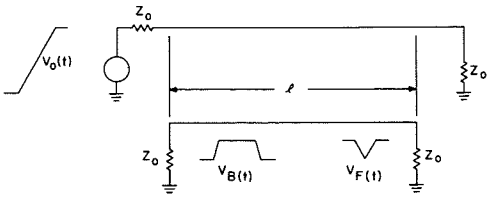


Fig. 10—Evaluation of crosstalk waveforms.

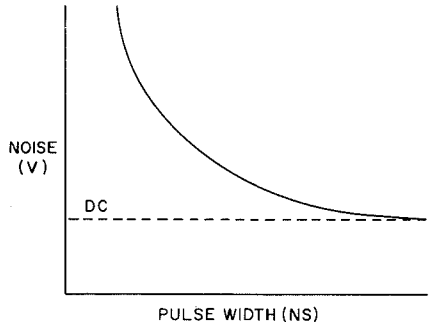


Fig. 11—Typical noise immunity curve.

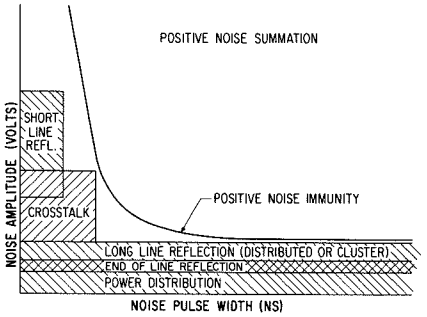


Fig. 12a—Positive noise summation.

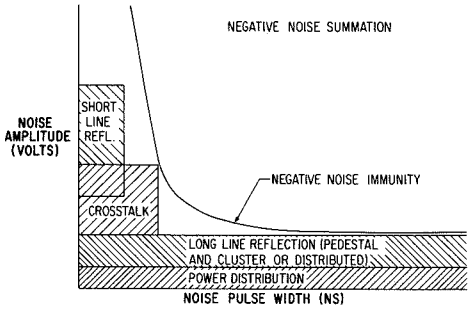


Fig. 12b—Negative noise summation.

$$V_F(t) = K_F\, d\, \frac{V_O(t)}{dt} \qquad (9)$$

thus,

$$K_B = \frac{V_B}{V_o},\ T_R < 2T_d \qquad (10a)$$

$$K_F = \frac{V_{F(\max)}}{l\, dV_o / dt} \qquad (10b)$$

The backward crosstalk waveform $V_B(t)$ has an amplitude that is independent of the transition time T_R and line length when $T_R < 2T_d$ and has a width of $2T_d$, where T_d is the propagation delay of the line. The forward crosstalk waveform $V_F(t)$ has an amplitude dependent upon the transition time and length of line and has a width equal to the transition time.

Once the constants K_B and K_F are determined for the coupling of interest, the crosstalk waveforms for any length, transition time, or signal swing may be calculated. These constants are easily measured whereas the normal method of measuring or calculating mutual capacitance and inductance is difficult and frequently inaccurate. One measurement of V_B, V_F, V_O and the transition time determines K_B and K_F by Eq. 10a and 10b. This measurement may be made at any reasonable V_O and transition time for the coupling of interest. The reflections of crosstalk waveforms from the end of the line terminations may be treated by the graphical method presented earlier.

Power distribution noise

The design of the power distribution system of a computer has frequently been one of trial and error. The analysis of the noise generated involves cumbersome impedance equations for various geometries of conductors. These tended to discourage theoretical calculations and make decisions regarding trade-offs between lower impedance versus more stored charge difficult.

For this design, the impedance equations were programmed on a computer. The output of the computer consisted of the following impedance parameters versus any variable of interest:

1) L_{INT} = the internal inductance of the conductor due to current concentration near the periphery of the conductor.
2) L_{EXT} = the inductance due to the proximity of the return path.
3) R_{DC} = the DC resistance.
4) R_S = the resistance due to the skin effect.
5) C_{EQ} = the equivalent capacitance including dielectric losses due to frequency.

The noise generated on the power and ground lines is determined by these parameters in the following equation:

$$\Delta V \approx I_{DC}\, R_{DC} + \left(\tfrac{1}{2}\left[\frac{L_{INT}+L_{EXT}}{C_{EQ(LINE)}+C_{EQ(CAPS)}}\right]^{1/2} + R_S + R_{DC}\right)\Delta I \qquad (11)$$

The first term is the DC loss due to the constant current flowing through the DC resistance of the buss. The second term is the voltage change due to the current pulse caused by the switching circuits of the plug-in.

The current pulse is caused by the difference in DC currents of the two logic states, plus the current to charge or discharge circuit and signal line capacitance, plus the current flowing while both the upper and lower transistors of the TTL output are on. The rise and fall time of the current pulse determines the frequency to use for the impedance calculations.

The equation is then applied in successive steps, i.e., from the plug-in to the backplane, until the power supply is reached.

The impedances in the noise equation are plotted as a function of the variables of interest (such as frequency, width of conductors, spacing between planes). Then, the various trade-offs between quantity and location of capacitors, type of busses and/or planes are made to arrive at an acceptable noise level.

Circuit noise immunity

System noise must be controlled to insure that the summation of all the above noise is not greater than the level the circuit can tolerate. This level may be found theoretically, empirically, or by a combination of both. A typical noise immunity curve appears in Fig. 11.

The tolerable level of noise is defined here as the level of noise at the input of a chain of worst-case gates that will create a noise pulse of an equal level at the output of the chain. This is known as the unity gain concept of noise immunity. It is simply a measure of the maximum noise that, introduced at the input of the chain of circuits, will die out in the system. A noise pulse of greater amplitude may become amplified as it propagates through the system, thus creating a false signal which could be remembered by a flip-flop, one-shot or other storage and edge triggered devices.

Controlling noise

We have thus far defined the problem, listed the noise sources, and determined the expressions which dictate

the amount of noise to expect. Many variables in the expressions are determined by the package and circuits. The problem now is to assign values to the remaining variables such that the summation of all worst-case noises is less than the noise immunity of the chain of worst-case circuits. It should be noted that other design philosophies may be used. For instance, only a percentage of each noise may be considered to act at any one time or each noise may be individually compared to the noise immunity curves. These are not worst-case conditions and involve various degrees of risk.

Table I—Variables for all noise sources.

Noise	*Variables*
End of line reflection	1. Line impedance (Z_t) 2. Circuit input & output impedance
Distributed load reflection	1. Spacing between loads (d) 2. Line impedance (Z_t)
Pedestal reflection (negative noise only)	1. Line impedance (Z_t) 2. Spacing between loads (d)
Cluster reflection	1. Number of loads (N) 2. Line impedance (Z_o)
Radial line reflection	1. Length of lines
Crosstalk	1. Type of line 2. Line spacing 3. Parallel line length
Power distribution noise	1. Impedance of current path 2. Filter capacitance

The summation process is now carried out for positive and negative noise immunity curves as shown in Fig. 12. This presents various trade-offs to be considered by the designer. The power distribution noise, for example, may be increased at the expense of reflection noise. More crosstalk may be allowed if reflections or distribution noises are reduced, etc. Notice also that the noise generated must be controlled to satisfy the worst of the positive or negative noise immunity curves. Once the trade-offs have been made, usually through several iterations, the final summation is complete.

The power distribution noise which can last for a long AC time period is controlled to the desired level by adjusting the impedance and filter capacitance of the system for a given plug-in and backplane geometry.

The long line reflections (either pedestal or distributed) also may last for long AC periods compared to the circuit noise immunity curves. They are controlled by choosing the proper value of minimum spacing and type of line. Their amplitude may bring the partial summation to a value just below the DC noise immunity of the circuits. The proper value of minimum spacing is the larger of the two derived from Eq. 4 or 5. Note that the pedestal reflection occurs only on the negative noise immunity curves.

Crosstalk amplitude and width are adjusted to guarantee not to break through the curve. They are controlled by specifying the maximum allowable parallelism length for a given type and number of lines, assuming they are tightly bundled.

The end of line reflections are adjusted by controlling the circuit input impedance. For the series 1600 system, the graphical method was used. It was found that under worst-case conditions the reflections would exceed the noise immunity curves. Therefore, the circuit parameters required altering. The input impedance of TTL showed that there was a reverse diode connected to the substrate (Fig. 13). This diode had a high resistance and varies from vendor to vendor and from lot to lot. Improving the diode characteristics significantly reduced the reflection and made it nearly independent of loading and Z_o. As shown in Fig. 13, the reflection was reduced from B to B'. The TTL vendors were shown the value of improving the substrate diode or adding an improved diode to each input. A test for the desired characteristic was added to the purchase specification, and each vendor altered his basic line of TTL. Thus, end-of-line reflections were essentially eliminated as a noise problem and no wiring restrictions or line terminations are required for this noise source. The small reflection that can occur may last for long AC time periods, but its amplitude is not sufficient to break the curve when added to power distribution noise. It cannot add to the long line reflections since it cannot occur at the same time. This reflection applies only to the positive noise immunity curves.

The reflection caused by a cluster is covered by the reflection block in Fig. 12 until the number of loads in the cluster becomes large enough to cause the reflection to break through the curve. In this case, the reflection can be controlled to a certain extent by the line impedance, but usually not to a level which is acceptable to the system. It is, therefore, necessary to avoid this

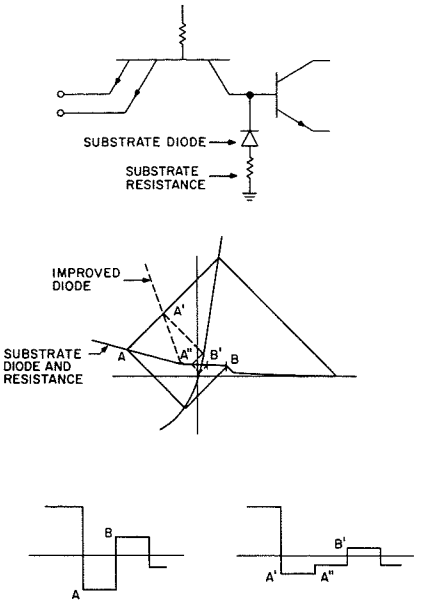


Fig. 13—End-of-line reflections were eliminated in series 1600 TTL circuits by improving the characteristics of the substrate diode.

reflection by prohibiting the placement of loads in front of the cluster. As a result, the cluster reflection does not appear in the summation of noises.

Radial line reflections are controlled by specifying a maximum radial line length such that the reflection width can be neglected.

Finally, short line reflections may be added in place of long line reflections, but as mentioned earlier, the widths are narrow enough such that they cannot pass through the circuit.

In the series 1600 system, all noise generation calculations were made with the parameters at their worst-case values or (where possible) by distributing them normally over their range and taking the 99.98% confidence level as an operating point.

The rules that evolved from this approach were implemented by a design automation program. This program has the capability of testing and correcting for all reflection wiring rules and testing for parallelism rules. It was found that approximately 83% of transmission lines in the system basic processor fell into the short-line category leaving only 17% which had to follow minimum spacing, radial line and cluster rules.

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Circuit concepts for the series 1600 computer

J. W. Haney | D. B. Ayres

This paper traces the evolution of the circuit design for the series 1600 computer. A general approach to selecting an integrated circuit is presented, followed by the specifics for this particular application. A functional description of the circuit is given and the trends for this type of integrated circuit are discussed.

GIVEN THE TASK of specifying an integrated circuit for a particular application, there are nine areas that must be explored:

1) The Manufacturer
2) Fan-in, Fan-out (Current & Voltage Compatibility)
3) Speed
4) Noise Immunity
5) Power Supply Requirements
6) Power Dissipation
7) Family Logic Variations
8) Cost
9) Vendor Compatibility

General considerations

Manufacturer

The prime vendor or vendors must be major manufacturers of integrated circuits. Items for consideration are:

1) The engineering capability of the vendor.
2) The production capability of the vendor.
3) The total dollar volume of business with RCA.
4) The number of licensees or other manufacturers that produce the same products.

When considering engineering capability, it is important to gauge the appreciation of the vendor's device engineers regarding systems problems. The sources of noise in the system and the parameters of the integrated circuit that have major effects on system performance, and cost must be a mutual concern of the circuit designer and the device designer. Examples of these parameters are given in a subsequent article on "End of Line Reflections," and "The Pedestal Reflection."[1]

The schedules and commitments of integrated circuit manufacturers are controlled to a large degree by Marketing. The engineering activity of the device manufacturer must be able to recognize the need for technical changes in the product and have prompt action effected once a decision is made between the circuit and device engineers. The influence of the vendor's engineering department in his own house is very important to the system designer.

The production capability of the vendor is important. The best engineering talent in the world is useless unless the vendor has the capability to produce a reliable device and in the quantities needed. There are several yardsticks that can be applied to determine this. The past performance of the vendor, while doing business with RCA, can be provided by the purchasing department of RCA. They have local, as well as Corporate, history that is most helpful.

A plant visit can also be enlightening in this regard. A very desirable design goal is to specify as near as possible the vendor's product line device. His projected volume and existing production schedules then become pertinent. An RCA volume in addition to an industry volume, results in a lower unit cost than if the circuit is an RCA special.

The total dollar value of business that a vendor transacts with RCA is another consideration. If the amount is appreciable, it is sometimes very helpful to solicit the aid of RCA's purchasing activity in scheduling prototype parts for the design phase. They can overcome a lot of vendor inertia. Another item that a large volume of business can affect is component price. Sometimes the total dollar value in other areas can affect the price of an integrated circuit as much as, if not more than, the quantity.

It is axiomatic that two major integrated circuit manufacturers must be approved suppliers; however, after this

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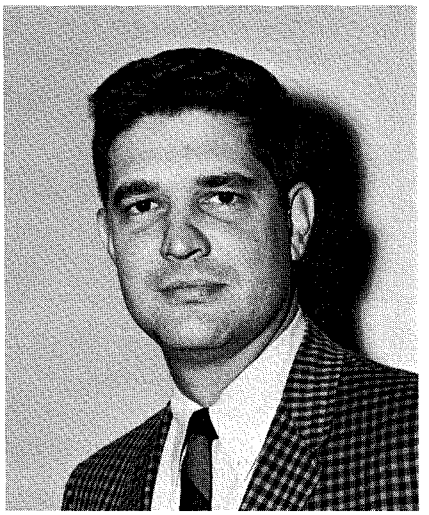
J. W. Haney, Mgr.
Memory and Power Supply
Design Engineering
Information Systems Division
Palm Beach Gardens, Fla.

graduated from the Citadel in Charleston, South Carolina, in June 1956. He joined RCA on the engineering training program in June 1956, entered the Air Force in September 1956, and served as a Wing Communications Electronics Officer in the Strategic Air Command until April 1959. He returned to RCA in 1959, joining the Comlognet Design Group in Camden, where he worked in Memory Design for the Comlognet systems. In August 1962, he transferred to EDP, Palm Beach Gardens, Florida, with the Circuit and Memory Design Group. In July 1964, he was promoted to Engineering Group Leader, in Sustaining Engineering for BPU, Memories, and Power Supplies. In February 1966, he was appointed leader of Circuit Design Engineering. In May 1968, he was promoted to his present position. He attended the University of Maine and the University of Pennsylvania taking graduate courses in EE.



Douglas B. Ayres, Ldr.
Design Integration
Information Systems Division
Palm Beach Gardens, Fla.

received the BSEE from the University of Tennessee, Knoxville, in 1961. He was employed by Honeywell EDP, where he worked in the Circuit Design Group specializing in magnetic surface read/write circuitry. In 1964, he joined RCA-EDP, in Palm Beach Gardens. While in the Circuits Design Group, his primary responsibilities were in the field of analysing and specifying digital integrated circuits. In May 1968, he was promoted to his present position. Mr. Ayres has taken graduate work in electrical engineering at Northeastern University. He is the holder of two U. S. Patents.

has been effected it is extremely important to have secondary suppliers. It is quite advantageous to have at least one of the prime sources with an alternate that produces the same units. This further helps to protect RCA against having to be without components in the event of vendor problems. Licensees that can produce, but are lacking the full production capability of the larger companies, are valuable sources. There are times when the reaction time is less from the licensees.

Fan-in fan-out (current & voltage)

The fan-in and fan-out of the circuit to be considered should be given in terms of current and voltage as well as a number of like circuits it can drive.

This is done to indicate its capability to drive other circuits such as delay lines, one-shots, transmitter-receivers, as well as other types of integrated circuits.

Speed

The configuration of the computer logic dictates the speed of the circuit used. The circuit designer is usually given a maximum pair delay and the maximum skew (max PD − min PD) that can be tolerated in the logic design. This parameter is arrived at after many iterations that weigh the tradeoffs between what is acceptable from a logic design point of view and what is possible from a circuit design point of view.

Noise immunity

When evaluating noise immunity before samples are available, the specification sheets of the vendor must be used. The DC noise immunity is specified by most vendors. This is not necessarily the worst-case noise immunity for the particular circuits; however, the voltage swing and the noise immunity can be used as a figure of merit for the particular circuit. Considerations must include not only the ability of a circuit to reject noises caused by other circuits; but should also take into account the ambient noise that exists from the electrical package, radiation, and other such effects. Noise immunity, of course, is considered from both the high and low level states of the circuit. The rise and fall time of circuits have a bearing on the speed and noise generating characteristics, and should be considered when comparing circuit types.

A feel for the AC noise immunity can be derived by comparing DC noise immunity, voltage swing, rise and fall time, and circuit delay.

Power supply requirements

The number of power supply voltages required for an integrated circuit is also a consideration. Obviously, it is better to use one voltage rather than two, if circuit performance allows. This not only yields benefits in the power supply design, it also allows more pins for logic and less complicated power distribution schemes.

Power dissipation

Power dissipation within certain limits is not as important to the commercial computer designer as it is for many military applications; however, the speed-power ratio is a figure of merit of a circuit.

Family logic variations

The variations among members of a given integrated circuit family are not of uniform significance. For instance, the ECL circuit that provides a complementary output with each gate will not require as many family variations as will a TTL family. The TTL makes up for this with various gate configurations such as dual-4, single-8, and/or AND expanders, quad 2's, triple 3's, etc. An added advantage of TTL is that it contains "small arrays," such as the 16-bit memory elements that are located on a single chip. Within a particular IC family the number of variations is significant. To have a manufacturer create a set of masks to give a particular variation is very costly; therefore, the circuits that exist must be used where possible. Using the vendor's standard line allows for expansion at no development cost to the user when the vendor adds circuit configurations to this line.

Cost

At the outset, before the vendor is picked and the exact volume is known, a cost comparison for small quantities (1 to 999) is helpful. This relationship does not hold up as the volume increases, however.

Vendor compatibility

All circuit variations of a particular

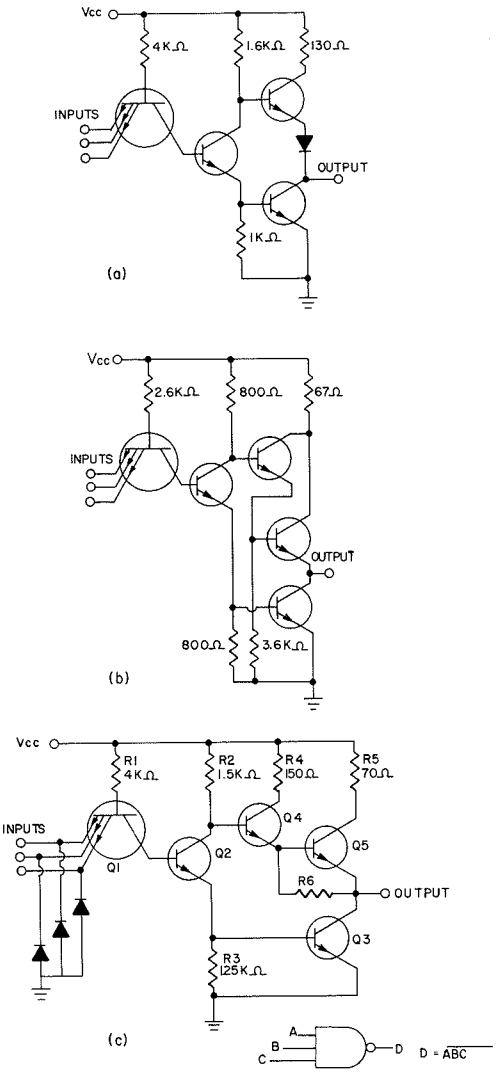


Fig. 1—Three circuit configurations: a) and b) were rejected, c) was the acceptable TTL circuit.

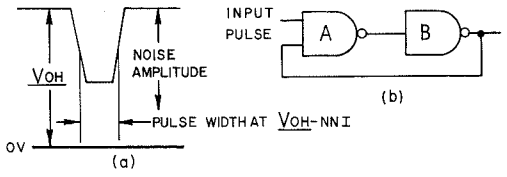


Fig. 2—Test for noise: a) input pulse, b) test circuit.

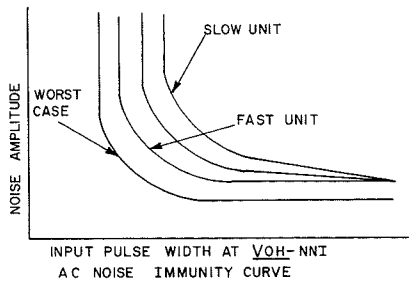


Fig. 3—Circuit noise measurements.

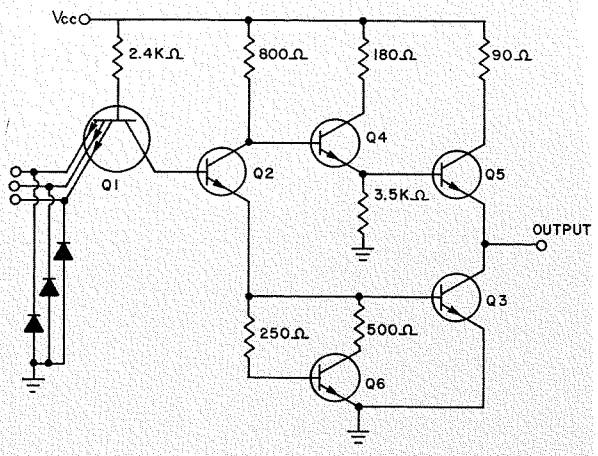


Fig. 4—Recently available TTL circuit.

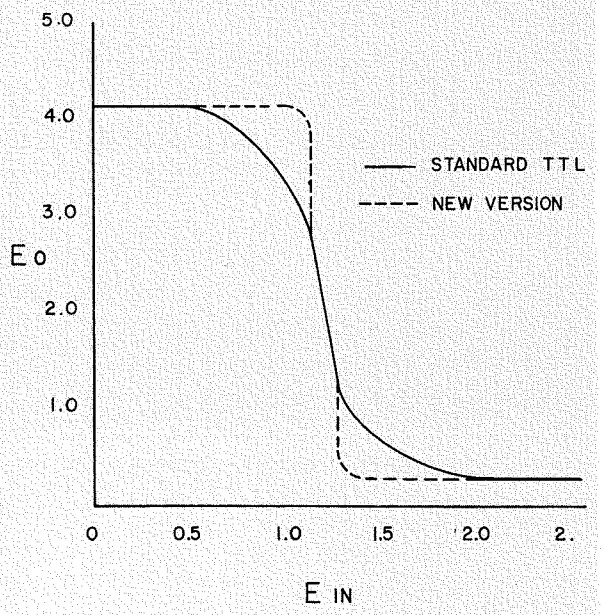


Fig. 5—Effects of loading on the standard TTL and new TTL circuits.

family must have the same voltage pins, supply voltages, and logic levels. The number of suppliers having units with these items in common provides an insight into the ease of multiple sourcing for a circuit family.

The circuit chosen—and why

Comparative values derived from the nine general categories that were discussed in the previous section were used to select the type of circuit for the series 1600 systems. Each of the nine categories was weighed in light of the available integrated circuits. A scaling factor from 0 to 4 was used for each integrated circuit type. As can be seen from Table I, the items marked by an asterisk were multiplied by two as they were considered most important.

Table 1—IC Ratings

	TTL	ECL	DTL	CTL	VTL
Manufacturer	4	4	4	0	0
*Fan-in, Fan-out	8	4	6	6	2
*Speed	8	8	0	6	0
*Noise Immunity	6	4	6	4	8
Power Supply	4	4	4	0	0
Power Dissipation	3	2	4	3	1
Family Logic Variations	4	4	4	4	1
Cost	4	2	4	3	3
Vendor Compatibility	3	3	4	2	0
	44	35	36	28	14

In considering the circuits only, DTL, TTL and ECL were quite close. There were, however, other application considerations that further affected the integrated circuit selection. The series 1600 system logic design could tolerate a worst-case pair delay in the order of 35ns; therefore, TTL and ECL met the speed requirements while DTL did not. This ruled out DTL.

The electrical package and its associated cost were a major factor in choosing between ECL and TTL. The package employed in the Spectra 70 computers using ECL was a known quantity. The platters, line terminators, and triple layer plug-in boards were estimated and compared to the 2-series package cost, also a known quantity. The 2-series package is used in Spectra 70 peripheral equipment and the 70/15 and 70/25 computers. It uses automatic wire wrap and printed backplane wiring techniques, and is less expensive than the platter approach.

The TTL circuits were tested using the 2-series package with double-sided plug-ins and found to be compatible, providing the backplane wire routing could be closely controlled. This was accomplished using the Gardner-Denver wire wrap machine with routing that was generated by design automation programs.

Many 2-series discrete circuits existed that were compatible with TTL voltage levels and currents. These being the previously mentioned delay lines, one-shots, transmitter-receiver, etc. The ECL output was not compatible with these circuits.

The system packaging cost, plus the lack of compatibility with existing 2-series circuits, ruled out ECL.

These considerations, plus the large interest in TTL, which prevailed throughout the industry both in the USA and abroad (Siemens AG of Germany and Hitachi of Japan), made TTL the choice.

Selecting the TTL family

Once TTL was chosen, it was necessary to decide which family of TTL to use. Its operation is essentially the same for all families considered. The gate circuit is characterized by a multi-emitter input transistor, a phase splitter, and an active pull up output. The high speed is a result of three factors:

1) The multi-emitter input transistor allows for smaller geometries, hence lower circuit capacities and faster switching;
2) The transistor action of the input stage in sweeping stored charge from the base of the phase splitter contributes to the fast turnoff of the device; and
3) The active pull up on the output gives the circuit a very low output impedance. This results in excellent capacitive drive capability.

The three circuit configurations considered are shown in Fig. 1. The circuit shown in Fig. 1a was not usable because:

1) The output impedance, with switching to a high level, is high enough to cause a pedestal in the threshold region;[1]
2) The circuit was too slow; and
3) Input clamp diodes, essential for controlling reflections, were not in the circuit.

The circuit shown in Fig. 1b was rejected because:

1) Poor AC noise immunity;
2) Fall time too fast; and
3) No input clamp diodes.

The circuit chosen, along with its logic symbol and Boolean equation is shown in Fig. 1c. This circuit was acceptable because:

1) The output impedance, when switching to a high level, is low enough to

prevent a pedestal in the threshold region;[1]
2) It met system speed requirements;
3) The vendors agreed to include the clamp diode in their standard lines; and
4) It has adequate AC noise immunity.

TTL circuit description

When all inputs to the multi-emitter transistor Q_1 (Fig. 1c) are held high, current flows through the base resistor R_1 into the phase-splitter, Q_2, and to the lower output stage, Q_3. Transistor Q_2 is in saturation, therefore, its collector is at a potential of $V_{BE\ Q3} + V_{CE(SAT)\ Q3}$. Transistor Q_2 is in saturation with its collector current being supplied by the load. The output low level voltage is $V_{OL} = V_{CE(SAT)\ Q3}$. Transistor Q_5 is off; Q_4 is either off or on by a trickle current.

When one or more inputs to the multiple-emitter gate Q_1, are low, no current flows to the base of Q_2 and it is off; therefore, Q_3 is off. The output high level voltage at this time is:

$$V_{OH} = V_{CC} - \frac{I_O R_2}{h_{FE\ Q4}} - V_{BE\ Q4} - I_O R_6$$

If $IR_6 \geq V_{BE(ON)\ Q5}$, then Q_5 is on, and the output voltage at this time is:

$$V_{OH} = V_{CC} - \frac{I_O R_2}{h_{FE\ Q4}\, h_{FE\ Q5}} - \frac{V_{BE\ Q5}(1 + h_{FE\ Q5})\, R_2}{h_{FE\ Q4}\, h_{FE\ Q5}\, R_6} - V_{BE\ Q4} - V_{BE\ Q5}$$

The DC noise immunity for this circuit is defined as follows:

Positive Noise Immunity $= V_{IN(MAX,\ LOW\ LEVEL)} - V_{OL(MAX)}$ where $V_{IN(MAX,\ LOW\ LEVEL)}$ at the input gives $V_{OH(MIN)}$ at the output with I_O maximum.

Negative Noise Immunity $= V_{OH(MIN)} - V_{IN(MIN,\ HIGH\ LEVEL)}$ where $V_{IN(MIN,\ HIGH\ LEVEL)}$ at the input gives $V_{OL(MAX)}$ at the output with I_O maximum.

The following worst-case values were determined for the basic gate circuit:

$V_{IN\ (MAX,\ LOW\ LEVEL)} = 850\text{mV}$
$V_{OL\ (MAX)} = 350\text{mV}$
$V_{OH\ (MIN)} = 2.6\text{V}$
$V_{IN\ (MIN,\ HIGH\ LEVEL)} = 1.9\text{V}$

From the above values it is seen that $PNI = 500\text{mV}$ and $NNI = 700\text{mV}$.

Defining AC noise immunity for the gate circuit is more complex. The most meaningful definition of AC noise is the noise that will cause a flip-flop to latch. The method of measuring this noise is delineated in Figs. 2 and 3.

In the test circuit shown in Fig. 2b, gate B is a minimum turn-on delay limit unit. In Fig. 2a, the input pulse width and amplitude are varied until the flip-flop latches. The input is then measured to determine a point on the curve. Several units having different turn-off delays were used in the gate A position and a family of AC noise immunity curves were generated. It was observed that the curves moved to the left along the horizontal axis as a direct function of their measured turn-off delay. With this information and the minimum switching turn-off delay value, it was possible to limit the size of the "noise blocks" determined by crosstalk, reflections, and power distribution to values that would guarantee system operation under worst-case conditions. A similar method was used to determine the size of the blocks for a turn-on condition.

Current spiking

When the output switches from a low to a high, Q_4 and Q_5 turn on faster than Q_3 can turn off and a current spike appears on the V_{CC} line. Examination of the circuit shows that:

$$I_{CC\ (MAX)} = \frac{V_{CC} - V_{CE(SAT)\ Q5} - V_{CE(SAT)\ Q3}}{R_5}$$

The amplitude of this current spike depends on the value of R_5 and is independent of loading. The very small saturation resistance of Q_3 overrides any load resistance in parallel with it. The pulse width of I_{CC} is determined by several factors. First, pulse width varies as a function of load capacitance. Second, as the temperature increases, the h_{FE} of Q_3 also increases causing it to turn-off slower; this increases the time that both Q_5 and Q_3 are on simultaneously. The current spike on the V_{CC} line is a major consideration in designing with TTL. Ground planes on the plug-ins and high frequency capacitors in the series 1600 controlled the effect of the current spike.

A recent version of TTL

The circuit in Fig. 4 is a recently available version of TTL. The operation of this circuit is the same as those previously described except for the following:

On a rising input, the offset transistor, Q_6, remains off until its V_{BE} is overcome. When it turns on, the phase-splitter emitter will see an equivalent resistance of approximately 570Ω to ground.

Prior to the turn-on of Q_3 or Q_6, there is essentially no current flowing in Q_2. This means that the collector node of Q_2 and the output will be at a high potential until Q_3 or Q_6 turn-on. Then, the output changes rapidly (Fig. 5). When a resistor to ground is in the circuit, the collector of Q_2 and the output change as shown in Fig. 5 (for standard TTL).

On a falling input, Q_2 will remain in saturation until the potential at the emitter of Q_2 falls below the V_{BE} drop of Q_3 or Q_6; at this time, Q_2 has no path for emitter current and abruptly turns off. The collector of Q_2 and the output node correspondingly rise to a high level.

The effects of this non-linear circuit in the emitter of Q_2 are shown in the transfer characteristic in Fig. 5. It can be seen that the noise immunity of the circuit is improved. The purchase specification for the integrated circuit used in the series 1600 computer includes this new version of TTL.

TTL trends

The series 1600 computer system TTL circuit is the standard Information Systems Division medium-speed integrated circuit. There are several recent developments that enhance the advantages of TTL, such as the many small arrays on the market that are TTL compatible. The wired OR function is being added to the family and is used where speed is not the primary consideration. The component price is such that it will be less expensive than DTL in the immediate future.[2] We feel the standard TTL is a very firm base from which to develop future computer circuit designs.

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Installation of computers

B. Aaront

As RCA computer systems evolved from the small data processing unit to the large scale communications system, more efficient methods of installation, planning, and control were necessary. Previously the service manager who had a maximum of five or ten units to install could be on site as the equipment was being delivered. With large-scale communications systems having one or more computers, twenty or thirty tape stations, mass storage units, and multiple remote devices, it became apparent that this same manager could no longer operate intuitively. This paper emphasizes the growing need for formal planning and control techniques for the installation of RCA computers. It also documents the progress to date in applying these techniques.

Bruce Aaront, Mgr.
Major Systems
Information Systems Division
Cherry Hill, N.J.
received the BA in Physics and Mathematics from New York University in 1950. He was employed as a Research Physicist in Electronics and Optics by the U.S. Government until 1952, at which time he joined RCA Service Company as Manager of the BIZMAC Computer Installation at ATAC in Detroit. In 1959 he returned to Cherry Hill as Manager of Field Support Engineering for Electronic Data Processing Services, and was responsible for installation of the first ten RCA 501 computers. He served in this position and subsequent positions as Manager of Project Control, Manager of Engineering and Training and Manager of Field Operations, until 1966 when he assumed his present position. Among his current duties is the management of the Field Service for Graphic Systems, Instructional Systems, Systems Centers, and Government Systems. Included in these responsibilities is the task of installing and maintaining the first computers of the new product lines.

IN THE COMPUTER INDUSTRY, competition has been increasing, profit margins have been shrinking, and it has become increasingly more difficult to obtain maintenance manpower. Therefore, better methods to allocate our resources had to be devised. To accomplish this objective, a formal management control system was applied to the installation of major RCA computer systems. All resources available, such as manpower, material, time, money, and outside engineering assistance, would be catalogued and used as factors in the system. Restraints upon the project, such as installation due dates, system acceptance tests, customer needs, site facilitation, customer program implementation, and other factors would also be catalogued and used in the master project plan. Initial charting and planning techniques used were GANT charts, SHEWART charts, and an approach to PERT and critical path method.

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SAMMS program

One of the first systems to undergo this management planning was the SAMMS (standard automated material management systems) program. The master planning chart that evolved (Fig. 1), indicates that we used a combination of most of the presently accepted techniques. In retrospect we find a less than rigorous approach, in particular in the planning chart which does not conform to orthodox PERT or CPM planning. The planning combined both task and event orientation, and depended mainly upon event reporting. Basic tasks charted were:

1) Manpower training,
2) Manpower at manufacturing plant,
3) Design fabrication and system test schedule,
4) Equipment checkout at manufacturing plant,
5) Spare parts, test equipment and tools,
6) Engineering support, and
7) Environmental and site planning.

SAAMS manpower

For each man assigned to the project a complete dossier was established, showing his education, present training and past job history. This was compiled into a continually expanding skills inventory. The skills inventory was used by project management as a guide to arriving at the appropriate timely decision. A major objective of our planning was to enable our management personnel to have all of the necessary information at their disposal to allow them to make these decisions at the decision points. Therefore, when a decision point was arrived at, management would have a concise listing of the objectives to be met, they would know what was required to meet the objectives, and would have the sum total of all the resources at their disposal.

Phase II

Despite the departure from orthodox PERT and CPM planning techniques in the SAMMS installation, it was apparent the intensive planning and charting which occurred during this installation were in a large measure responsible for the successful completion of the installation. Therefore, work was started on more sophisticated and formal techniques of this type of planning. A new procedure for installation of major systems was embarked upon. This planning was to be based on task orientation and event reporting, with specific fall-back procedures at each critical juncture point.

The installation would be considered a closed system and careful planning and charting would be devoted to the following resources:

1) Manpower
2) Material
3) Time
4) Training

In addition, charting also included the following restraints:

1) Customer deadlines
2) Customer tests
3) Acceptance tests
4) Financial restraints

A diagrammatic approach of the arrow network type chart was decided upon, combining a modified PERT and a CPM technique. In addition, specific break points, dummy job lines, decision points, and alternate courses of action at the decision points would be inserted.

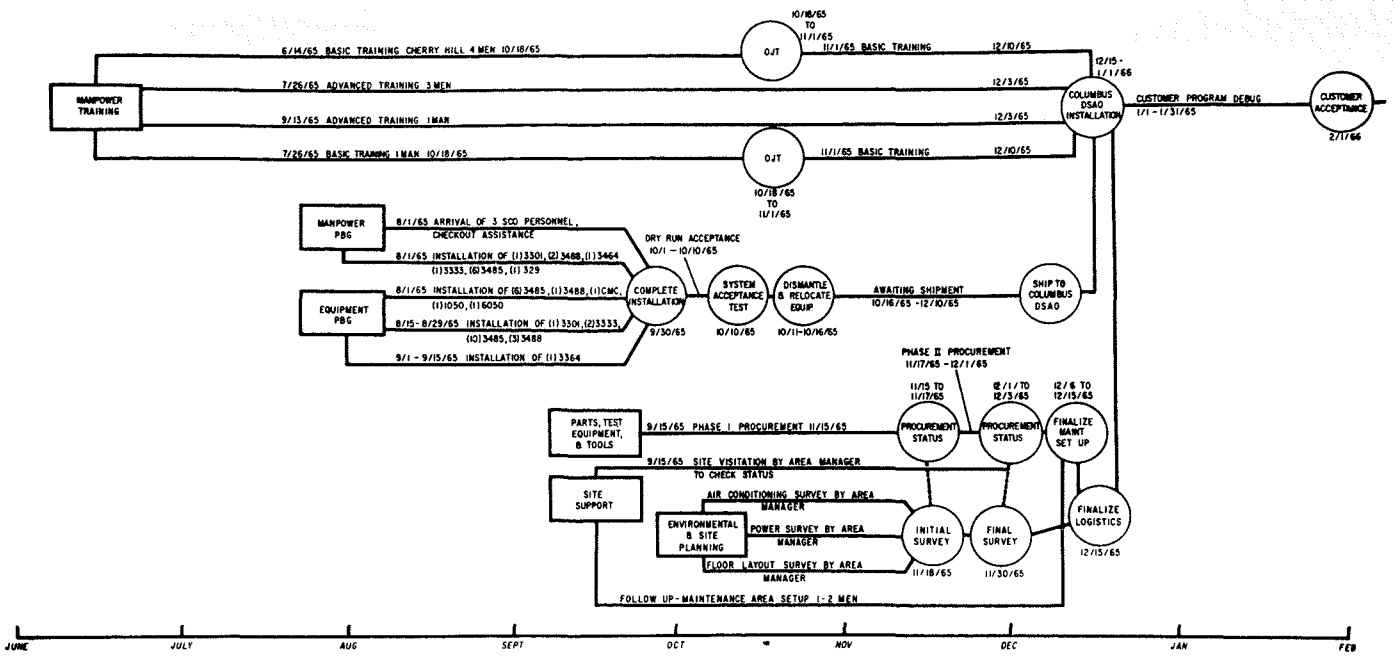

Fig. 1—Maintenance plan for the SAMMS program.

A fall-back plan was devised for each decision point. The plan included a complete list of all resources, both men and material, courses of alternate action, the effect upon the resources of each alternate course of action and the time frame within which the decision must be made.

Skills inventory

As a result of our SAMMS experience we expanded the skills inventory and insured it would be compiled for each major project. The skills inventory became a compilation of the individual and total manpower assigned to the project. For each man, a separate chart was prepared showing his past educational background, past experience, RCA experience and training, his present training, and his scheduled training. At any point in time, this skills inventory showed the total manpower resources available to the project manager.

Management information

Since it was essential to keep management completely informed as to the position of each particular project, each major Spectra installation was considered as a *separate* project. To provide the necessary information, the following items were charted:

1) Our objectives on a timely basis.
2) The men, material and other resources required.
3) Resources available.
4) The Decision Points at which alternate courses of action should or could be taken.

Installation diagram

The arrow network diagram was of prime importance in determining the proper work sequence in system checkout. It was essential that the model be one which could be related to the work on a one-for-one basis. In essence, this called for accurate timing of each task. to be undertaken. Detailed analysis was made of each particular step of the installation. For example:

1) Initial pack of equipment at West Palm Beach and Camden, N.J.;
2) Deployment of key installation personnel and site representative;
3) Unloading from van;
4) Cartage to the site;
5) Physical installation at site;
6) Installation of power cables;
7) Installation of signal lines;
8) Preliminary checkout and debugging of equipment on a functional basis;
9) Running test and maintenance routines;
10) Running customer data; and
11) Running final acceptance test.

Each of these items was given a time cycle. In addition, time elements were applied to the sub-elements of the total job. For example, with respect to the checkout of the Processor, the sub-element time cycles were:

1) Installation of main racks;
2) Initial power-up test;
3) Installation of read only memory;
4) Basic time-cycle checkout;
5) Basic processor checkout;
6) Basic memory checkout;
7) Processor T&M checkout;
   a) EO tests;
   b) Buss-adder tests,
   c) Fast memory tests,
   d) Main memory tests,
   e) Snap shot and diagnose control,
   f) Staticizing,
   g) Exclusive functions, etc.
8) Checkout of monitor printer; and
9) Installation and checkout of special features.

The total grouping then, of sub-elements, elements, and major job cycles, gave the planner the total time necessary to complete the job and establish the break points. In addition, the scheduling criteria of each job was carefully examined. In particular, the necessity for start time was looked at very closely. A job was considered critical if the necessity for starting this particular job was tightly time oriented. If it was not time oriented, it was labeled a non-critical job. As in standard PERT and CPM planning, float and slack time determinations were made.

Additional advantages

Because of the necessity for careful analysis with respect to the planning itself, certain work that had been done in the past, always in a predetermined fashion by either habit or because it was "always done that way" was carefully analyzed. In some cases, it was found that the optimum sequence of work was other than it had been done in the past.

Specific applications

In late 1965, a letter of intent was given to RCA by the Department of Motor Vehicles of the State of California for a vast Computer Communications Network with an automatic realtime system. The system was to include a total

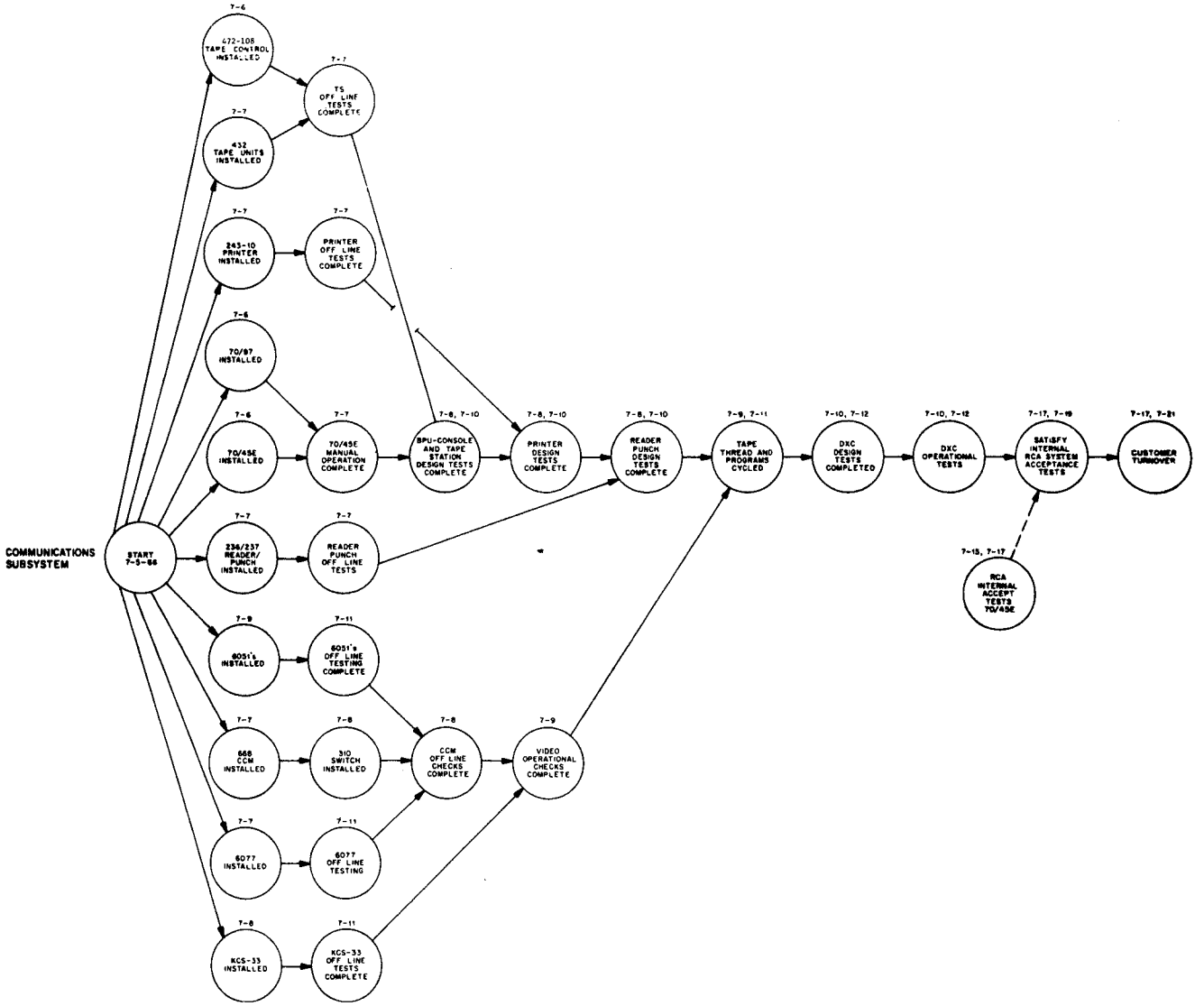

Fig. 2—Installation and checkout schedule for the California Department of Motor Vehicles system.

management information system, designed to be completely operational by 1970, with phase I implementation starting in 1965.

The main objectives of the system were:

1) Rapid service to California public;
2) Efficient, economic operation paced to rapid population growth;
3) Up to the minute information for the Department of Motor Vehicles (DMV) and related State and local activities;
4) Information for Management decision through a fully integrated management information system.

The system had to be capable of handling sixteen thousand transactions per peak hour and have an automated data bank located in Sacramento with storage capacity for over fifteen billion characters.

The DMV complex consisted of two separate systems: 1) a Spectra 70/45E data processing system with very large mass-storage capability and 2) a very large Spectra 70/45G data communications system. Although each system was entirely separate, the installation, operation, and customer implementation had to be rigidly controlled so that both systems were operational at exactly the same time.

Planning

Detail charting and analysis of the project was started one year before installation. The planning and installation charts for the overall installation of the file control system and communication subsystem took the form of arrow diagrams and embodied most of the PERT and CPM techniques (Fig. 2). The arrow diagrams were task oriented with event milestones. Each event milestone showed both total starting or finish float. In addition, subcharts showed critical decision points, potential problem points, and points at which fall-back procedures had to be invoked.

Job parameters

All planning must be congruent with the particular operation to be performed; therefore, prior to arriving at a final planning chart of the project itself it was necessary for management to decide the method of allocation of total resources. The basic resources available were men, material, money, and time.

In essence, three choices or modes of operation were open, they were:

1) Optimize both time and money—have an efficient and judicious distribution of men and material to obtain the maximum efficient output within an optimum time frame. This would not necessarily yield the minimum installation time.
2) Plan to have an installation completed with minimum money being spent. This would then give us unlimited use of time as a resource.

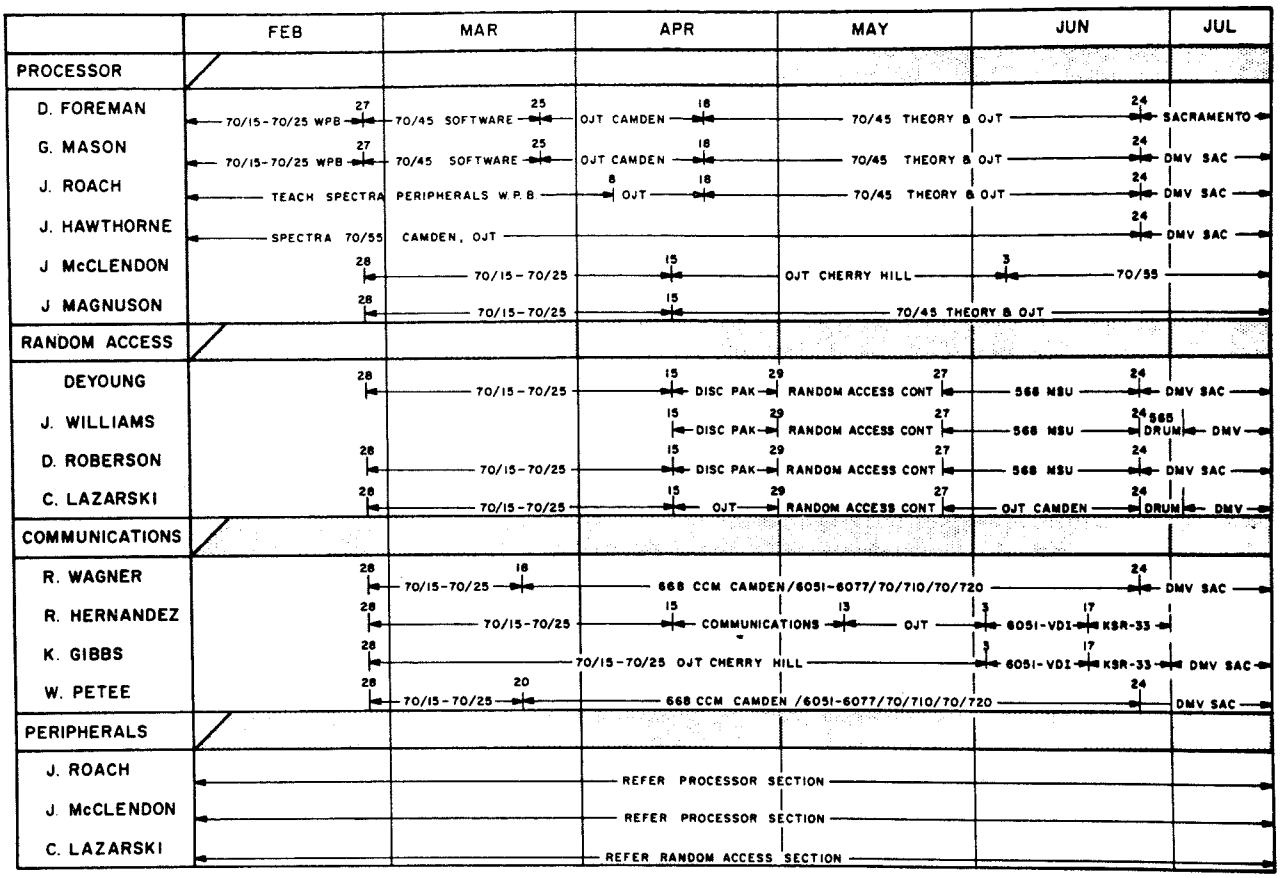

Fig. 3—Manpower training schedule for the Department of Motor Vehicles system.

3) Plan to have the installation completed in minimum time. This would allow the greatest use of manpower, material, and money.

Due to the critical nature of the installation with respect to the marketing of Spectra systems, it was decided that these systems should be installed in the minimum time. This minimum time interval was one that coincided with the needs of the State of California for implementation of its on-line communication system for both driver licenses and vehicle registration.

Planning was oriented to this mode of operation to achieve minimum installation time while still ensuring that it be done within reasonable financial bounds. It was mandatory that management be kept completely informed at all stages of the operation both on a technical and marketing basis. Accordingly, an event-oriented reporting procedure was established. This event orientation gave home office management bench marks in time, and in most cases these event-oriented points were also the critical or decision points.

Training

Sub-elements of the total system such as training, used a GANT chart method of presentation (Fig. 3). In essence, the planning was handled on the main system installation chart, and the scheduling was handled on a sub-chart. The sub-chart deals with the training schedule, and shows the scheduling of the training for all of the men at the site. In particular, it indicates the high level of cross training given each man. Based on minimum installation time, the main planning document showed that to have a 90% chance of success at the decision points there had to be enough cross training in the skills inventory to allow for at least 20% attrition. To compensate additional men were trained for each particular piece of equipment. Each piece of equipment was covered by at least three fully trained men.

On-site application

Constant and careful surveillance of the critical path was provided by a rigid control system including a maintenance PERT diagram of all elements relating even indirectly to installation, training, and maintenance. Part of this control system was a complete weekly status report. In addition, a daily exception report was sent by TWX to the manager of major systems. As a result of the control system this resulted in operation of the Driver's License complex of equipment within a month after delivery. Both the Spectra 70/45E and the 70/45G subsequently went to a 17 hour/day schedule and operated sometimes six and even seven days per week.

In three definitive cases, the operation did not meet a particular decision point. In these cases fall-back procedures were used, manpower scheduling was re-arranged and a *predetermined* plan of action was started. This was one of the greatest advantages of using formal planning techniques, that is, the problems were solved *before* they occurred.

Summary

It was apparent that the use of planning and control techniques increased efficiency, reduced the need for excess resource allocation, and increased customer satisfaction with the RCA product. These techniques, while sophisticated with respect to past installation techniques are gross and crude compared to approaches that can be used. A refinement of the above techniques took place with the installation of the Southern Bell Rate-Quote System, and further work is now taking place with the Field Engineering Department of Information Systems to provide a true PERT-CPM approach to computer installation.

Site planning and air conditioning of EDP rooms

L. K. Jurskis

It is difficult to list all considerations that the engineer could use for guidance in selecting the proper site or designing the right air conditioning system. There is no substitute for experience; however, a lack of experience with computer installations can be offset to a great degree by thorough inspection and study of existing air conditioning systems in various installations. By studying the problems of each, the engineer can attempt to eliminate similar ones on his future projects. This paper helps to clarify several misconceptions about computer room air conditioning and establishes some guidelines to use in site planning and air conditioning system design.

Liutas (Lou) K. Jurskis
Field Engineering
Information Systems Division
Camden, N.J.
received the Associate in Technology from Temple University in 1953 and the BSME from Drexel in 1960. Before joining RCA in 1962, Mr. Jurskis was employed as an assistant staff engineer by Philadelphia Gas Works. During his tenure with RCA he has been associated with the BMEWS project headquartered at Riverton, N.J. While with this project, Mr. Jurskis completed an 18 month tour of duty as the site Mechanical Engineer in Thule, Greenland. Since September 1967 he has been an installation planning engineer with the Field Engineering Department of the Information Systems Division. Mr. Jurskis is a registered professional engineer in New Jersey and Pennsylvania. He is a member of the National Society of Professional Engineers, and the American Society of Heating, Refrigerating, and Air Conditioning Engineers.

THE INSTALLATION of a computer system is a complex undertaking which requires careful planning and preparation. Like any other project, the computer installation will involve some minor crises, regardless of how well it has been planned. To minimize these crises, and to optimize the computer system reliability, a reasonable and rigid project schedule must be developed and an adequate site to house the computer system must be selected.

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The cost of the computer site is insignificant compared to the cost of the data processing equipment that it houses. Quite often, however, the customer/owner of the computer system will try to overlook this fact and will insist on drastic reductions in site preparation funds. Thus, the first objective in computer site planning is to convince the customer that reliable computer system operation is dependent upon an adequately prepared site. After attaining this objective, other site planning points can be considered. Some of the points may seem trivial or obvious, but it is amazing how often they are overlooked. The following excerpt from our own Installation Planning Guide may illustrate these points.

"The most suitable location for the computer area should be determined only after thoroughly considering all aspects, including:

1) Sufficient air conditioning capacity;
2) Adequate electrical power availability and lighting intensity;
3) Floor loading and type of flooring;
4) Adequate protection from hazards, such as fire, smoke, water, radiation, etc.
5) Space with proper environment to house the data processing system and associated equipments;
6) Ceiling height, outside wall and glass area;
7) Flow of work to and from other areas;
8) Expansion of the system;
9) Adequate building entries to receive packaged equipment;
10) Spare parts storage and maintenance area."

If possible, the computer site should be located near the potential users of the system output and/or creators of input. A computer system in a customer's plant or business is usually a status symbol. Thus, a glass partition exposing the site could be installed if the customer desires to use this as a showpiece.

The importance of the function that the computer system performs determines the extent of the emergency and standby facilities required. As a minimum, these facilities should include:

1) Emergency power supply (battery/inverter system, MG set) for power fluctuations or failures of short duration.
2) Battery powered emergency lighting.
3) Standby power generator of sufficient capacity to provide power for the entire site (including air conditioning) in the event of prolonged primary power failures.
4) Standby air conditioning system, size of which is determined by the importance of the computer system.

The engineer designing the emergency standby facilities for the computer installations should consider the following aspects:

1) The flexibility of the changeover to the standby equipment must be carefully analyzed for each application.
2) Economics of first and operating costs and the importance of continuous operation must be seriously weighed.
3) The customer must be clearly informed what this standby system can do and what it cannot do. He must also be made aware of the cost of obtaining the operation he wants.

Each of these site planning considerations must be analyzed in detail; however, only the air conditioning aspects will be covered in this paper.

Air conditioning design parameters

Economics

Economics play an important role in the design of computer room air conditioning systems. Consequently, the first cost of a properly designed computer room air conditioning system will be high as compared to an air conditioning system "designed" and installed by a contractor. It may seem trivial, but this was our experience in many computer installations. Many of these systems were inadequate to provide the necessary environmental conditions for the computers and consequently, computer system downtime resulted. The cost of implementing-redesign of the air conditioning system brought the total cost above the estimated cost of a properly designed system. Thus, the customer ended up with higher expenditures added to his computer downtime.

There is no substitute for quality when it comes to computer room air conditioning, and, in certain applications, it is no longer a matter of dollars and cents, because the cost of an interruption of computer service is so great that, by comparison, installation costs become insignificant.

Design conditions

As in any other air conditioning system design, the point of departure is the establishment of indoor-outdoor design conditions. The outdoor design conditions depend on the geographical location of the computer site and are as specified by the latest issue of the ASHRAE guide. The indoor design criteria varies somewhat for different makes of computer equipment; however, most computer room air conditioning systems are designed to provide 73°F to 75°F (dry bulb) and 40% to 50% R.H. Nevertheless, it is of paramount importance for the air conditioning engineer to obtain the design criteria from the computer manufacturer. This information is readily available from the computer manufacturers' Installation Planning Guide. For example, our Spectra 70 Installation Planning Guide states:

South Central Bell's Shreveport accounting center—a facility built around computer site.

> "The environment for the most efficient EDP system operation and personal comfort is 73°F±2°F dry bulb temperature and 50%±5% relative humidity. Design of the air conditioning system should be based on this environmental condition and include consideration to meet this goal. However, the Spectra 70 systems may be operated within the following environmental ranges:
>
> 65°F to 80°F
> 35% R.H. to 60% R.H.
>
> Ambient air *entering* EDP equipment should be within these limits with the temperature rate of change not exceeding 1°F per four minutes.
>
> The extreme operating environment design limits of the Spectra 70 equipments are greater than the limits specified above. However, sustained periods of operation beyond the recommended limits are not desirable, nor compatible, with the environment required for magnetic tape, paper tape and punch cards."

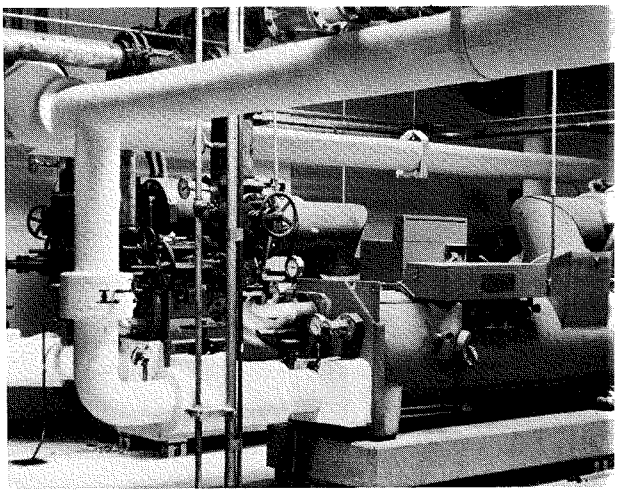
In the past, some of our customers and their engineers have supposed that computer room ambient conditions can vary between the extreme environmental limits specified in the Planning Guide without any adverse affect on the computer system. Consequently, inadequate and inaccurate controls were provided for the air conditioning system. Therefore, it was necessary for us to insert a statement limiting the rate of change in the computer room ambient temperature. This problem is common throughout the computer industry and computer manufacturers have revised their installation planning manuals.

Basic differences in computer room air conditioning

An air conditioning system for a computer installation differs from ordinary comfort air conditioning as follows:

1) Heat dissipation by the computers is relatively constant; therefore, cooling is required on year round basis.
2) The computer room sensible heat ratio is near unity, because heat dissipated by the computer system is all sensible.
3) Above average air filtration is required to prevent errors caused by dust particles on magnetic tapes.
4) Number of air changes per hour varies between 30 and 60 because of the high heat dissipation of the computer equipment.
5) Reheat and humidification is required year round to maintain necessary humidity conditions in the computer room.
6) The conventional overhead air distribution method is not desirable because most of the third generation computers are designed to take the cold air in through the bottom and discharge through the top of the cabinet.
7) Air conditioning system controls should not be placed near, or in the return air duct, because they will not sense the actual computer room conditions.

The most important factor the air conditioning engineer should remember is that computer room air conditioning must be designed to provide a proper

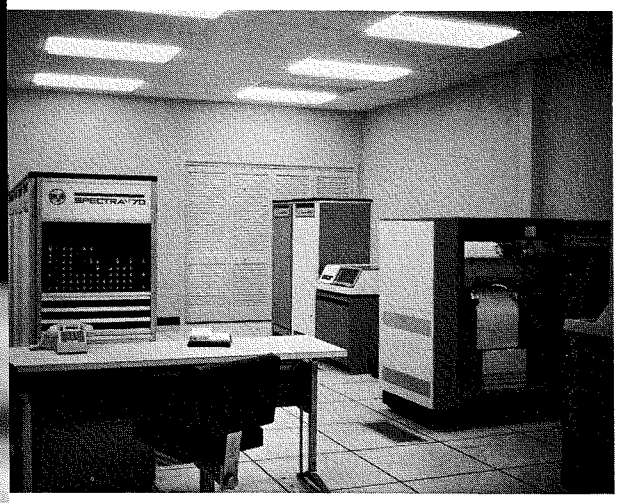


Shreveport accounting center equipment room. Duplicate chillers provide 100% standby air conditioning capacity for the computer site.

environment for the computers, and all other considerations, such as personnel comfort, are secondary.

Other considerations

The engineer must familiarize himself with computer equipment from the thermodynamic and construction point of view. How much heat does it dissipate? Does it take the air through the bottom openings or through the sides? Does it have internal fans in the cabinet? All these answers can be found in the computer manufacturers' Installation Planning Guide. Then the type of air conditioning system can be selected. Note that the computer room air conditioning system must be separate, serving the computers only. The engineer must determine whether the cooling load will be fixed or must a provision be made for future expansion. Is the computer operation around the clock, seven days a week, or only 40 hrs. per week? Provisions to prevent over-cooling of the computer rooms during the EDP equipment downtime must be made, since low temperature and high relative humidity is detrimental to the computers. Then, the type of air distribution system must be selected. If the customer does not insist otherwise, the engineer should design for underfloor plenum air supply and overhead return, because this is the most economical system for these third generation computers which take the cold air in at the bottom of the cabinets. Other methods



Efficient method of air distribution—conditioned air is supplied through floor grills, warm air is returned via ceiling grills (near the light fixtures).

Efficient method of air distribution—floor grills provide conditioned air near the air intakes of computer cabinet.

of air distribution are also acceptable; however they must be carefully designed to insure that the conditioned air reaches the air intakes at the bottom of the computer cabinets.

For better environmental control, zoning should be considered for larger computer system installations. Zoning is required where more than three computer systems are located in one room.

Types of air conditioning systems

The computer room air conditioning system must be separate and independent from the building system for the following reasons:

1) System must operate year round,
2) Temperature and humidity must remain relatively constant,
3) Computer system load is all sensible.

The system should conform to the requirements of the N.F.P.A. No. 90A "Installation of Air Conditioning and Ventilating Systems" (non-residential) and N.B.F.U. No. 75 "Electronic Computer Systems."

Basically, the selection of the computer room air conditioning system is not different from any other system, and is the prerogative of the engineer. Thus, depending on the load, the system selected can be packaged units with direct expansion coils or a centrifugal chiller with a number of air handling units. When making the selection, it must be remembered that the sensible heat ratio of the computer room is near unity and, therefore, the cooling equipment should be selected for maximum sensible cooling capacity and minimum dehumidification capacity. This is extremely important for small computer installations where packaged units are selected, since their nominal sensible heat factor is approximately 0.75. Thus, whenever possible, a split packaged system should be selected which allows variation of the fan-coil section.

The air conditioning manufacturers, recognizing the potential in the computer industry, designed a special packaged air conditioning unit for computer room application. This unit is a self-contained system for accurate control of temperature, humidity and cleanliness to meet the exacting requirements of computer rooms. These units are modular, and have capacity range of 3 to 15 tons. The average sensible heat factor is above 0.90. The most common application of these units is with a down-flow arrangement: discharging the air directly to the underfloor plenum and returning the air through the top of the cabinet. These units are also available with an up-flow arrangement. Most of these units are sold by the computer floor manufacturers, although there are several independent manufacturers.

Methods of air distribution

It is said that no air conditioning system is better than its air distribution. This could not be more true than in computer room air conditioning. The cool air is vital to the computer and, unless it is delivered to the proper place, the computer is dead . . . and so is the engineer.

As was mentioned earlier, the most efficient method of air distribution is via the underfloor plenum with an overhead return. It is efficient because it does not interfere with the convection principle. Depending upon the make of the computer, the cold air is introduced through openings in the floor under the cabinet or through floor registers located in front and back of the cabinet. The Spectra 70 equipment requires the latter method of air supply. (When using this method of air distribution, cable openings under the computer cabinets must be sealed. This prevents

any damage to the computer components by cold and humid air and allows for proper air balancing throughout the computer room). In some computer rooms the underfloor plenum is used for return air and cold air is introduced from ceiling diffusers, light troffers and/or "Airson" ceiling panels. This type air distribution is especially ineffective in computer rooms with a ceiling height under 10 ft. In such cases, special directional ceiling-mounted air-distribution devices should be used.

The least effective method of distribution is one where cold air is distributed through the ceiling diffusers and returned via air grilles also located in the ceiling. Depending upon locations of the diffusers and return air grilles, various degrees of short circuiting exist. The condition is further aggravated by the hot air discharge through the top of the computer cabinet, which can cause stratification or turbulence, depending upon computer cabinet and diffuser location.

Humidification

Because of the high sensible heat load of the computer room, moisture must be added to the conditioned air to maintain required humidity levels. The moisture added must compensate, first, for the moisture lost by exfiltration and, second, for the moisture removed by the cooling coil. Various devices may be used to accomplish humidification of the air, such as:

1) Live steam sprays,
2) Electrically or steam heated evaporative pans, or
3) Packaged inspace evaporative units.

Direct, inspace, water spray injection should not be used, since mineral contents in the water often precipitate as dust which will deposit itself in a fine layer over equipment and supplies and destroy data stored on some media.

Controls

The types of controls for computer room air conditioning systems are the same as for comfort air conditioning systems. However, these controls should not be located near, or in the return air duct. Because it is practically impossible to maintain uniform environmental conditions throughout the computer room, the controls should be located where the most precise conditions are desired.

Our experience shows that some computer system downtime was related to improperly located controls.

Model installation

The computer room of Southern Bell Telephone and Telegraph Co.'s Shreveport Accounting Center is a model installation. The cool air is supplied through the floor registers and warm air is returned via ceiling grilles located directly above the computer cabinets. A separate zone provides air for personnel comfort through ceiling diffusers located near one wall and away from computer cabinets. Humidity is maintained at proper levels by a central spray humidifier and zone reheat coils.

If all computer room air conditioning systems were modeled after the Shreveport Accounting Center, system downtime from environmental causes would be rare or non-existent.

Computers in the air conditioning field

Now that we have discussed what we can do for the computer, let's see what the computer can do for us. Following is a brief synopsis of a few articles on the subject from current issues of professional and trade magazines.

The June 1967 issue of *ASHRAE Journal* carries an article titled "Computer Programs for Air-Conditioning Engineers." Here the authors present and discuss three programs on air conditioning design that are used in their consulting office. The authors point out that the big advantage is that the input data can be easily modified for additional refinements and analysis—an engineering luxury virtually non-existent without a computer. The initial cost of these programs is high and the economics is based on how often they are put to work.

Directional air supply devices required with overhead air distribution system.

Properly planned computer site is well lighted, has underfloor air supply system, and is spacious.

Another article on the same subject appeared in the September 1967 issue of the *ASHRAE Journal*. In this article, Mr. Gabrielson, of Helsinki, Finland, describes FORTRAN programs that he used for calculating heat-cooling loads and energy requirements for buildings.

In another application, a computer is used in a commercial building for control of environmental systems. The Headquarters Building of International Monetary Fund in Washington, D.C., has 13 floors with 532,000 sq. ft. of office space. The computer automatically determines air conditioning needs and operates equipment at maximum efficiency to meet the requirements. It also logs and analyzes operating data and prints out a concise, daily summary. It is estimated that the refrigeration plant efficiency is increased by 9.4 percent, and the operating savings of 6.25 cents/sq. ft. of office area can be realized. At this rate, the computer will pay for itself in approximately 27 months. A description of this project appears in the August 1965 issue of the *Heating Piping and Air Conditioning*.

Use of flat cables in the Spectra 70 computer

G. R. Gaschnig

This paper departs from the traditional types that describe what could be designed and used in the future and how good it is. Instead, what is described is an actual working system which has been field tested and is presently in production. Not only are there cost savings over the conventionally wired techniques but also there are space, weight, reliability, and time savings. In full-scale, high-volume production right now, the RCA Spectra 70/45 Computer System was chosen as the system to first use this flat flexible cable system. A complete system is described composed of flat flexible cable, terminating printed-circuit boards, and clamping and supporting hardware.

G. R. Gaschnig, Ldr.
Electronic Packaging Group
Information Systems Division
Camden, N.J.

received the BSEE from Drexel in 1956. He then completed courses for a MSEE in large scale digital computers at the Moore School, U. of P. He has worked in digital computers for 15 years, starting with RCA's BIZMAC computer. Since then, he worked on logic, drum memories, and circuits of the RCA 501, 301, Recorder Control, CDP, 601, 3301, and Spectra 70 computer systems. He is the author of several articles pertaining to memories and the computer packaging field. Presently, he is a member of the IEEE and active on committees of the Institute of Printed Circuits. He had served on various committees of the Philadelphia Section of the IRE. He was listed in "Who's Who in the Computer Field—1955 and 1963/64."

WITH THE ADVANCEMENT of the state of the computer art, it soon becomes apparent that conventional hook-up wiring is not here to stay. Some impedance controlling is required among the 3rd generation computers. As speeds continue to increase so does the need for more closely controlled impedance, better shielding to decrease crosstalk and less noise in general. Part of these requirements are met today in different forms of single round wiring. We use twisted pair for balanced-pair wiring rules and twisted triplets for impedance control with additional shielding. Although presently functioning this way, not all goals are met. For instance, the bulk of twisted triplets far exceeds that of flat flexible cable. Weight saving and cost reduction are additional important factors to be considered at this time.

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Analysis of previous methods

A complete study was undertaken to explore the pros and cons of incorporating flat flexible cables. The first phase of this project was to thoroughly review the present method of interconnections using open wiring harnesses. Figs. 1 to 4 will delineate various steps of the original method of fabrication.

Fig. 1 shows a typical crimp machine and wires after termination. Since the maximum number of signal conductors obtainable in the connector was 36, that many twisted pair or triple twisted triads had to be terminated. Using the worst case of triplet wires, 36x3 terminations equalled 108 joints. A special terminal was designed to crimp 2 ground wires of the triplet wire into 1 terminal. This gave 36x1 or 36 joints. The other remaining 36 signal wires were crimped to a special component tip type of contact which was tapered and inserted into a plated through hole in the printed circuit board. Therefore 108 joints were reduced to 72.

Fig. 2 shows crimped wires being inserted into a printed circuit board. Normally both boards would be in the position as shown on the left first to have the single signal wire inserted into the plated holes. Then both boards would be turned over and be in a position as shown on the right. Here the 36 double crimped wires are inserted onto a specially designed grounding bar which makes all 72 wires common. Thus 108 wires are now terminated in 72 joints. The ground bar terminates into 12 printed ground paths.

Fig. 3 shows a typical cable board for making an 8-ended harness (only 6 ends are shown). Several completed subassembly cable printed-circuit boards with some wires attached are joined here and routed to make a complete harness. The remaining wire ends are then inserted into the added printed-circuit boards. Cable tying is done at this stage and completed harnesses are moved on to the next operation.

Fig. 4 shows a typical printed-circuit board being soldered. Only the signal wires (up to 36) are soldered into place at this stage. Upon completion the assembly goes through a cleaning operation and then a continuity test. A final QC inspection completes the harness and it is ready for inserting into the equipment.

These methods will be phased out as more flat flexible cable is designed into equipment from the initial concepts.

Vendor evaluation

The next phase was to translate the original wire specifications into specs suitable for a flat flexible cable. With this done, samples to our specs were solicited. What most vendors preferred was to provide cable material only. It soon became apparent after visiting many vendors plants that it would be preferable to produce a complete cable system tested and ready to install into a computer. Cost quotations were also solicited. These were then reviewed with Purchasing and Cost Estimating personnel and compared with production costs of the conventional cable. Savings of 30 to 50% over the conventional cable were predicted.

Sample products from several vendors were then ordered and received. Elec-

trical testing was performed for characteristic impedance, propagation delay, forward and backward crosstalk, rise-time degradation, and signal attention. Upon completion of all electrical testing, mechanical flexing tests were performed in the computer frame. Flexures exceeding several hundred thousand were performed before the testing was stopped .

Production planning

Upon completion of preliminary engineering testing, meetings with Production and Material Control Management personnel were held. A determination as to the length of time for cable production build-up was established. This was compared to computer production numbers and a "cut-in" established. Engineering drawings were made, assembly drawings were changed by Engineering Change Notices (ECN's) and various plans established for the entire task of "phasing" flat cable into all systems. It was quickly ascertained that the total cut-in of flat flexible cable could not be made at one time in an existing system. Therefore, various Phases or design goals were established. These were called Phase I, II, III. Phase I covered all 1-to-1, double-ended cables. Phase II covered "scrambled" 1-to-1 cables. Phase III covered multi-ended cables. There were too many design features to be solved all at once. Once a firm plan was established, progress could be monitored by a bench-mark method of schedule control.

An inter-plant study was made between the Palm Beach Gardens facility and Camden Engineering to tie in the use on the Spectra 70/45 and Spectra 70/35. (Spectra 70/35 engineering and production responsibility being maintained in the PBG plant.) This study indicated an immediate use could also be made of flat flexible cables in the 70/35 system, but on a lower quantity scale.

Flat cable design

A pilot run of flat flexible (of the type shown in Fig. 5) cable was ordered for a single system and installed. After assembly into the system, the unit was tested in all phases of Unit Operational Test, Customer Systems Acceptance Center Tests, and finally shipped to a customer site. Here this system has been operating for over 8 months. Based on this data plus all initial engineering test data, a production run of flat flexible cables was started.

The basic cable construction is shown in Fig. 6. To obtain the best shielding against crosstalk, a "D+2" configuration was devised. In this system, there are 2 ground conductors between each signal wire. Therefore, for 9 signal wires, 27 conductors are used, 18 for ground. As shown in Fig. 6, the conductors are all stripped and the designated ground wires pre-formed. Insulation is then removed over the area in a tinning operation.

To gain the maximum of 36 signal wires in a full cable, 4 flat cables are stacked together as shown in Fig. 7. A special, plastic, dimpled strip is placed between the layers to maintain spacing; these strips are also clamped on top and bottom. The entire assembly is then bound together at intervals to retain the package in a uniform manner. Not shown here but to be incorporated shortly will be a spiral binding that covers the entire cable.

As can be seen in Fig. 5, the cable ends terminate into printed circuit boards. Details of how this is accomplished are shown in Fig. 8. The cables are laid side by side—two on top and two on the bottom of the printed circuit board. Strain relief mounting bars or clamps are used to clamp the cable tightly into place. A rubber material is used to cushion the flat cable at this point. The exposed ends of the wire are then soldered into place. It should be noted that the hardware is essentially the same as that used for conventional round wire cable harnesses. The printed-circuit-board outline is identical, except that the copper conducting paths have been changed. The clamping bars and plastic handles are the same. Depending upon which direction the cable will run in the computer system, different folds are required. Fig. 5 shows a simple straight out folding arrangement. Fig. 9 in contrast illustrates a right angle handle-cover arrangement. This handle is used in the middle of a row of printed-circuit cards and mounted one above the other. In this way, cable from a printed-circuit

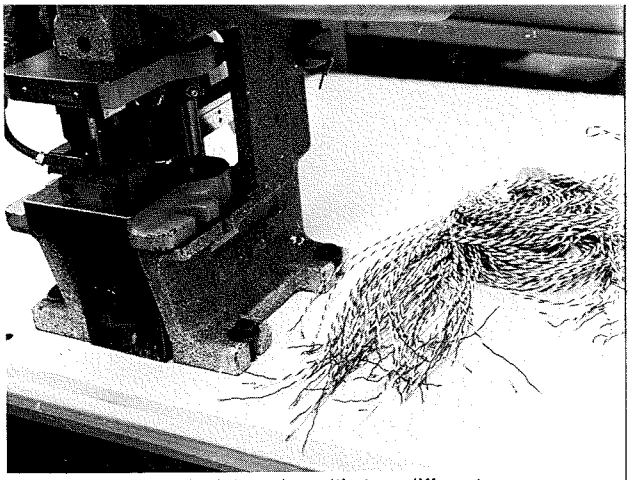


Fig. 1—Crimping of triplet wire with two different terminals.

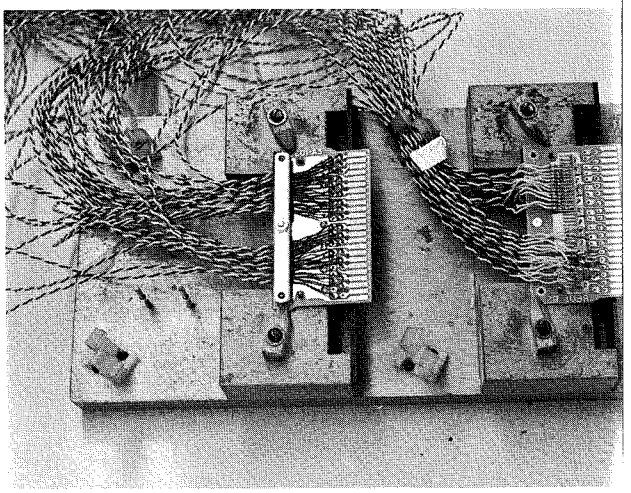


Fig. 2—Assembly of crimped wire and terminals to printed circuit boards.

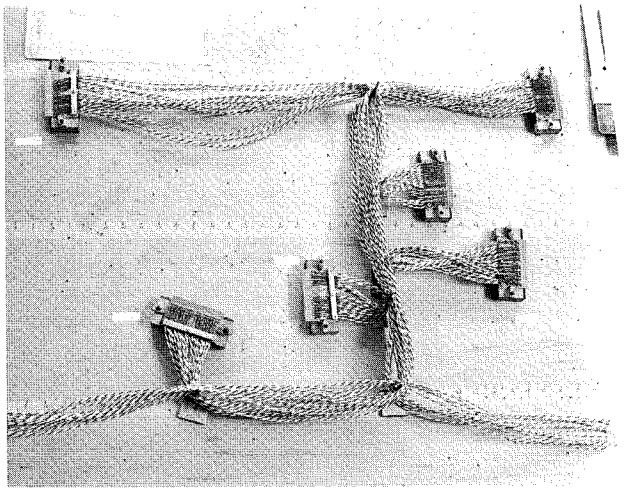


Fig. 3—Typical cable board with harness practically fabricated.

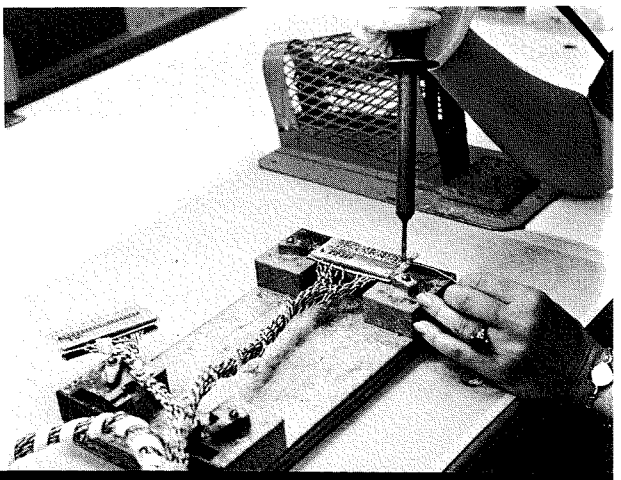


Fig. 4—Printed circuit being soldered.

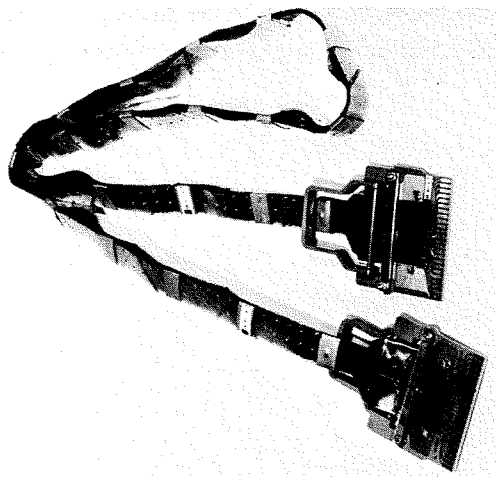


Fig. 5—Typical flat flexible cable of the type used.

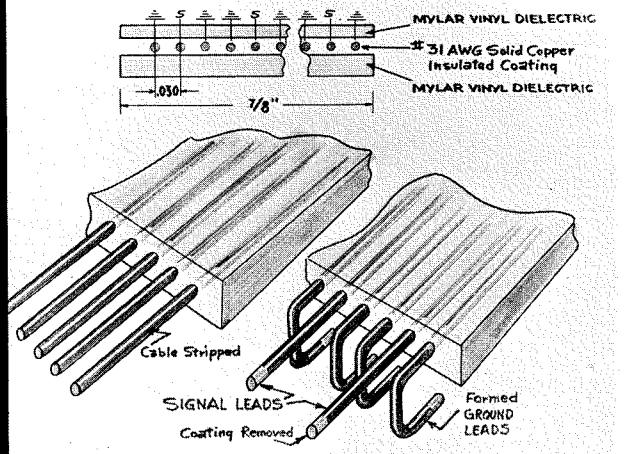


Fig. 6—Basic construction of flat flexible cable used.

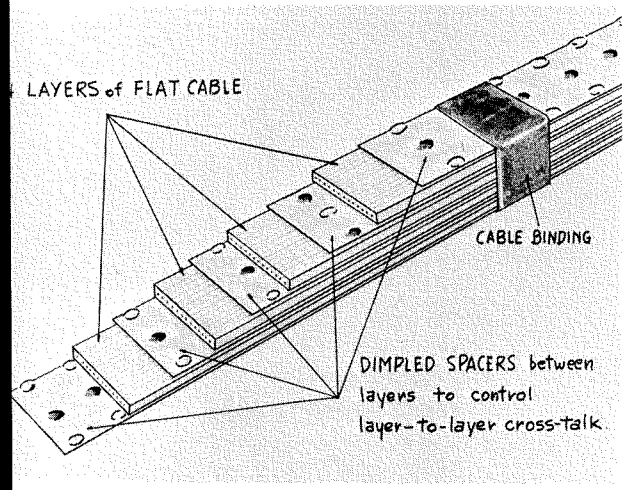


Fig. 7—Stacking of four flat cables with spacers.

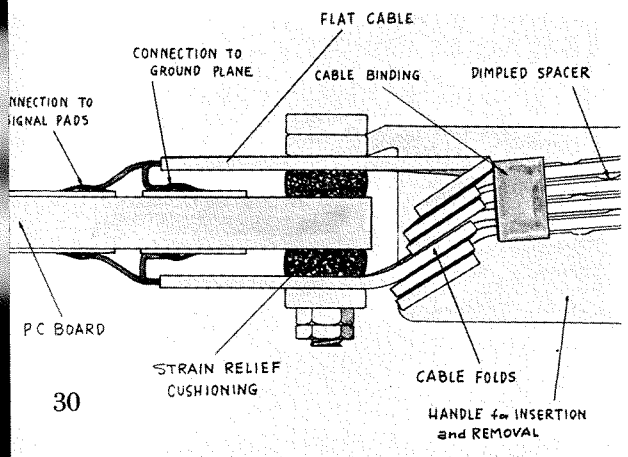


Fig. 8—Details of cable assembly to printed circuit boards.

board directly above may be routed down through the handle in the illustration and out the bottom together with the lower cable. The handle-cover is made to snap open and closed to release the additional cable for removal purposes without removing any hardware.

Fig. 10 is another view of the cable and printed-circuit board end. Note that the lower set of cables dress over the handle and the upper set dress under the handle. This is done so that when cables are plugged into their respective positions, all cables will always dress to the nearest outside channel of the enclosure that they are routed into.

Fig. 11 is a close-up of Fig. 10 and shows a little more detail. As can be seen, the notch or polarization cut in the printed-circuit board to the right of the right-hand board matches the notch to the left of the left-hand board. The boards have been turned over so both sides are visible.

Fig. 12 shows how the soldering is done. All grounds are first soldered in place. The signal leads are then dressed back over the ground leads and then soldered into place. Upon completion of all cleaning, the solder joint area is coated with a clear alkyd as a protective measure. Not shown here is a plastic cover that clips over the gold plated contact fingers and is used as a protective device until ready for installation.

System use

The primary use for this flat flexible cable is in the Spectra 70 basic processing unit (BPU). In addition to this heavy usage other areas are also presently using this cable. The read-only memory (ROM) and all its expansion units were tailor made for this application since they all use short 1-to-1 jumper cables.

Fig. 13 shows a view directly into the heart of the BPU. A multi-layer printed-circuit back panel (platter) has been removed to illustrate the cable. As can be seen, the flat flexible cable is routed into a channel formed between every two platters. The cables are placed on edge for maximum packing density. This particular view shows four cable harnesses running horizontally between platters. At the left and right ends, cables can run up or down.

Fig. 14 is a view with the access door removed and looking in from the opposite side as shown in Fig. 13. Note that one cable end is plugged in and the flat cable has been folded to go from a horizontal run to a right-angle horizontal run. At the extreme right the cable then routes up and takes another right angle bend. Also visible at the right are other flat cables running in a horizontal path. These are going from hinged Platter frames to fixed platter frames. Much use is made of cables around hinged points.

Future use

As we advance from Phase I into Phase II and Phase III, more and more flat cable will be used. Not only will cable be used within equipment cabinets, but also between units in a system. For instance, connecting BPU equipment to input-output (I/O) equipment. Since the flat cable is really a transmission-line cable in itself, its uses become more wide-spread. Another possibility may be wide scale use of flat cable in an attempt to eliminate false floors presently required in most computer installations. This idea alone would have tremendous cost savings. Not only would signal-transmission cables be flat but also power distribution cables. It is also quite possible when equipment is retrofitted and updated for optional features that flat flexible cable be installed at that time. All these things give more support for further use of flat cable.

New advances

As we approach the next generation of computer systems, many components will require controlled impedance. Among these will be the back-panel connector and the printed-circuit building-block cards. This will then allow controlled impedance at the circuit source itself which is on a printed board of numerous layers. This plugs into a connector which must be controlled. The connector mounts on a large multilayer back panel which is controlled. All back panels must be interconnected by controlled-impedance wiring. Here is where the flat flexible transmission line cables will be

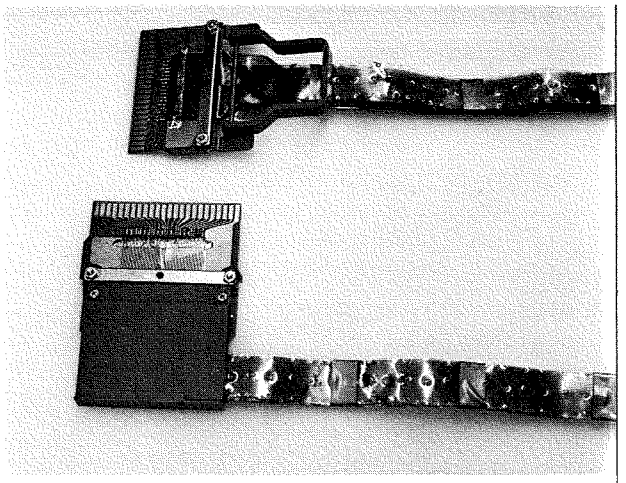


Fig. 9—Flat cable showing both designs of handles.

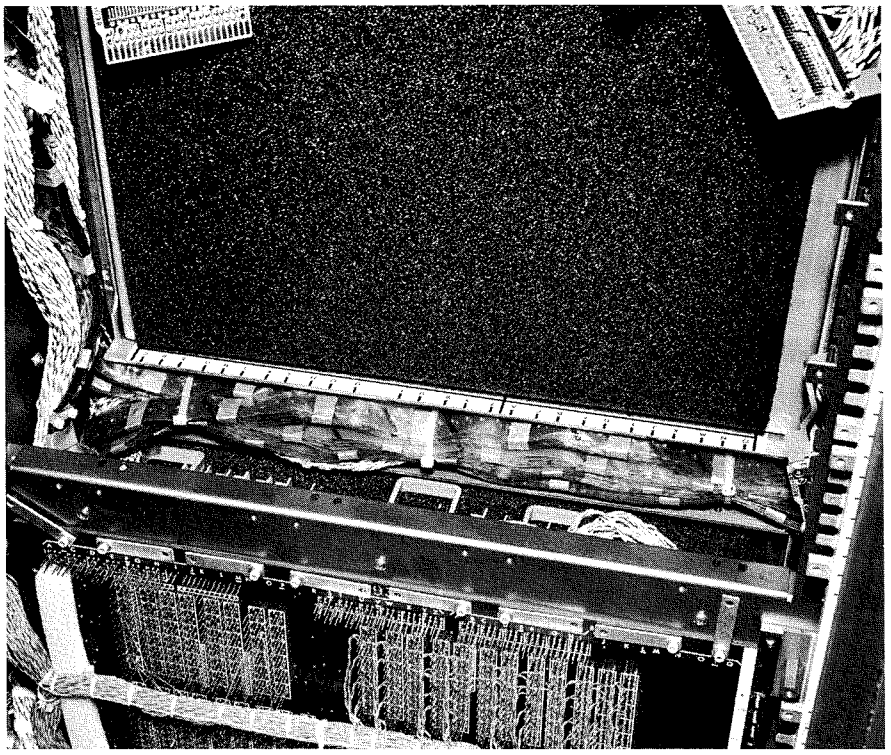


Fig. 13—Internal routing of cables in channels between platters.

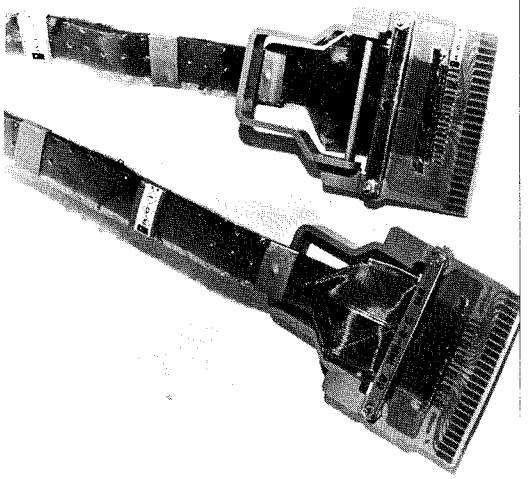


Fig. 10—Cable assembly showing typical front and back view of printed circuit boards.

used. As impedance values go lower, say to 50 ohms, discrete wiring on back panels becomes a problem. Perhaps a form of controlled-impedance flat conductor can be utilized here.

Higher densities will require MSI arrays to be connected in much shorter paths. Connector centers will be decreased from 0.60 inch to 0.50 inch and downward. This decrease in the connector/printed-circuit-board, spacing emphasizes the need for *flat* flexible cable where size starts to carry a lot of weight.

New types of termination techniques are constantly being explored. One is a pierce-and-pressure technique developed by a large manufacturer. This is presently being evaluated for use of discrete twisted pair or twisted triplet wires. It is quite feasible that this method may fit in well with flat cable.

Conclusion

Flat flexible transmission cabling is here to stay! What we must do is plan ahead wisely to utilize this cost saving device. With the growing use of design automation and partitioning programs, the interconnection wiring must be considered at the earliest design stages. We are presently enrolled in such a program. As much use as possible will be made of past experience, and this coupled with design automation as a tool will go a long way towards achieving this goal. As newer techniques become available they will be analyzed, tested and evaluated.

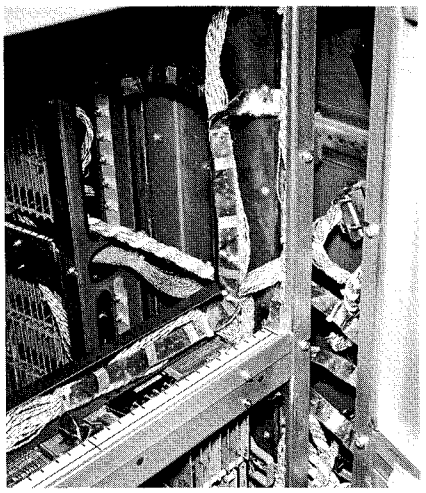


Fig. 14—View with access door and platter removed.

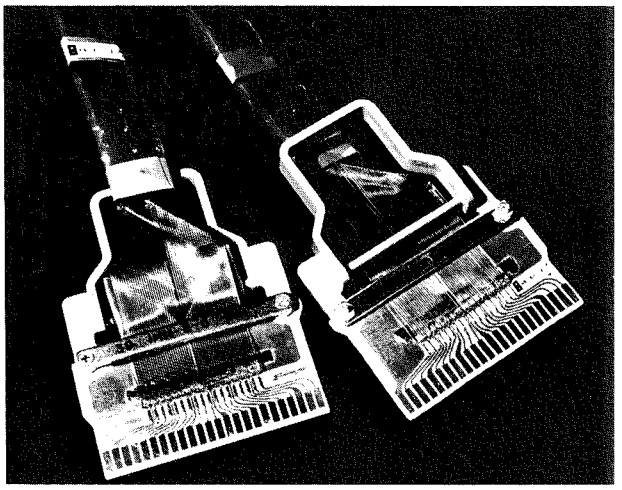


Fig. 11—Flat flexible cable showing polarization keying of boards.

Acknowledgement

The author wishes to acknowledge the assistance and continued support of J. B. Gallager, Packaging Engineering and J. N. Marshall, Manager, both of Information Systems Division.

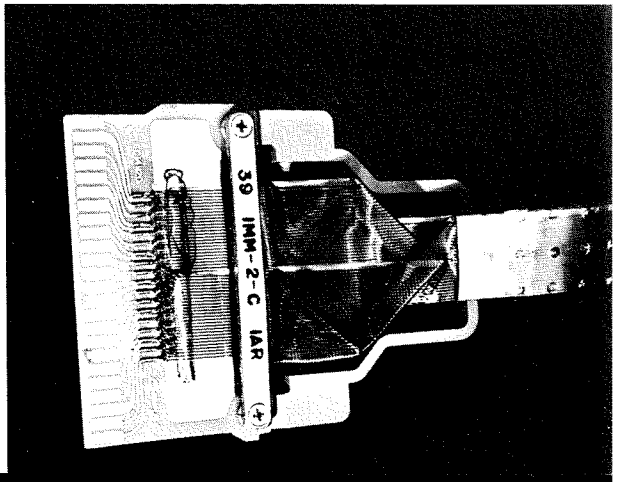
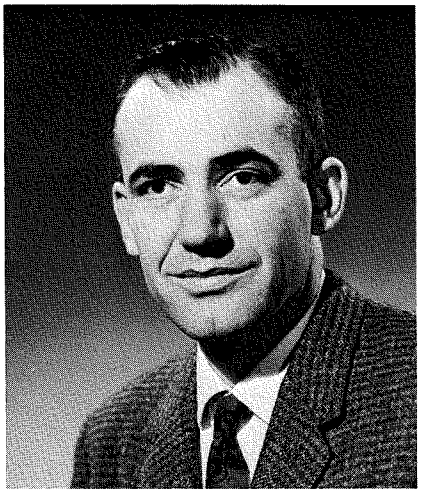


Fig. 12—Printed circuit board illustration after soldering is complete.

Development of a logic connector

J. B. Gallager

In the development of connectors for the Spectra computer series, trade-offs had to be made between such parameters as card-guide height, contact gap, contact tang, and connection methods. Additionally, after the basic connector was developed, its design had to be revised to accommodate double-size plug-in cards. This paper describes the development process.



J. Boon Gallager, Jr.
Packaging Group
Information Systems Division
Camden, N.J.

received the BS in Chemical Engineering in 1951 and MSME in 1958, from the University of Pennsylvania. He joined RCA Camden in 1958, and worked in Defense Electronic Products. He participated in packaging work on the GK-5 program and later joined the Minuteman effort, where he worked on packaging of portable test equipment. In 1964, he joined what is now Information Systems Division, where he worked on the mechanical design of the Spectra 70 computer. During this time he had particular interest in the design, development and qualification of connectors. Before joining RCA, Mr. Gallager was employed at Teledynamics, Inc., where he worked on the packaging of airborne military electronic systems for two and a half years. Before this, he spent five years as a mechanical engineer in the generating stations of the Philadelphia Electric Company, where he was chiefly concerned with plant operating efficiency. He is also a licensed Professional Engineer in New Jersey.

EARLY in the development of the Spectra computer, it became apparent that a special connector would be required. This connector (Fig. 1) was to provide a path from printed pads on a plug-in card to plated-thru holes on a multi-layer printed back plane. To provide for additional backplane wiring, such as changes or areas where the wiring density exceeds the capacity of the multilayer board, wire wrap capability was also required on the connector.

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The plug-in card has 24 contact-pad positions on each side of the card, spaced on 0.125 centers. Only 32 to 36 of the possible 48 contact positions are used for signals—the remainder are used for grounds and voltage supply. The contact pads are gold plated, with a nickel underplate. Different colors are used to distinguish those connectors that mate with cable cards from those that attach to logic cards. Fig. 2 shows the connectors assembled into the multilayer back plane.

The multilayer printed back plane (platter) has thru-plated holes on a 0.125 square grid. The connector contacts are soldered into these thru-plated holes, using three rows of holes in a unique pattern as shown in Fig. 3. The contact tails extend through the platter to provide wire wrap posts. The connectors are wave soldered to the platter, so that the contact tails are coated with solder before being used for wire wrap. Fig. 4 shows the solder side of the multilayer back plane, with the connector contact tails protruding, ready for wire wrap.

The contacts are formed from a solder-plated rectangular (0.020 x 0.030) phosphor-bronze wire. Gold tips are attached to the wire at the point of contact. The contacts are a preloaded cantilever type, held in the insulator by a friction fit.

Guides for plug-in card

There are three major reasons for including card guides on the connector:

1) To ease card insertion
2) To support for the card; and,
3) To prevent card insertion at an angle that will cause the wrong contacts to touch board pads, resulting in electrical damage to card components.

Additionally, the guides were used for polarizing the card.

A separate card-guide system could have been attached to the platter and frame. However, this approach was discarded so that the connectors could be arranged in an irregular manner on the platter. In addition, the separate guides would interfere with the desired cabling arrangement.

Long card guides were also ruled out as they would tend to block the flow of cooling air to the card in some cases where the spacing is as tight as ½-inch. The short card guides finally selected have spacers mounted on the ends of the cards to prevent the cards from touching. The minimum length of the connector card guide was then determined by its ability to prevent a card from being inserted at an angle sufficient to permit a card pad to touch the wrong connector contact. The calculation of this is shown in Appendix A. The second card guide was made longer to polarize the card. The difference in the heights of the card guides is 0.80 inch, to prevent a reversed card from being partially inserted.

Plug-in card pad size

The width of the contact pad on the plug-in card is determined by considering the width of the connector contact and the cumulative tolerances of connector and card. The goal is to provide assurance that the contact will always rest fully on the pad. The dimensions and tolerances to be considered are:

Width of card	3.055 ± 0.005
Card edge to first pad center	0.090 ± 0.004
First pad to far pad	2.875 ± 0.003
Width of pad	0.087 ± 0.003
Width of connector opening	3.065 ± 0.005
Conn. edge to cavity center	0.095 ± 0.003
Contact center to cavity center	0.000 ± 0.005
Contact width	0.030 ± 0.004

Appendix B illustrates that these dimensions will provide for full pad coverage for the contact with a full tolerance buildup. The Appendix also shows that there is a slight advantage

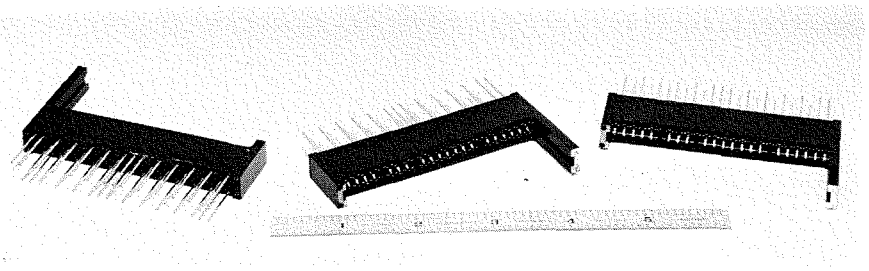


Fig. 1—Logic connector.

to calling out dimensions on the card such that tolerances accumulate from the opposite end of those on the connector.

Material and construction

The material used in the insulator is polycarbonate. This was selected after consultations with several prospective manufacturers. Polycarbonate is a remarkable tough and resilient material. It has low heat resistance; nevertheless, it is quite adequate for this application. It has a very low tolerance to chemical solvents; therefore, water soluble flux had to be used in the soldering operation. This requirement is not a drawback, since an organic solvent for flux removal would dissolve flux residue and would obviously leave a residue film on the contacts. Water, on the other hand, can be used freely for good flushing.

A phosphor bronze was selected as the contact material. The initial intent was to use a 0.025 square wire for this, which would fit into the 0.040±0.003 thru-plated platter holes. However, a 0.020×0.030 rectangular wire was used, since this was easier to handle and has an almost identical diagonal dimension. Other considerations entering into this decision were that the square wire would alter the contact spring rate and weaken the torsional resistance of the tail for wire wrapping.

Although a plated (gold/silver) contact was initially proposed, the advantages of a gold tip became quite apparent. The tip provides a heavy gold area which will withstand the wear of repeated card insertions, whereas plating would soon be worn down to base metal. Further, the tip facilitated the use of a reflowed solder-coated contact, which is a factor in obtaining high reliability in the soldering operation. Fig. 5 shows the same view as in Fig. 4 after wire wrap connections have been made.

The gold tip was attached by what was once described as a weld; however, after looking at several microsections, it was obvious that it might better be called a pressure bond. The shear force of this joint, measuring a surface area of approximately 0.030 x 0.030 inch, has been specified as greater than 5 lbs., or 5400 lb/in.^{2}

The contact has two protrusions formed in its tail at the point of attachment to the insulator. The mating hole in the insulator is rectangular and of such size as to provide a force fit. The force required to remove one of the contacts is between 5 and 15 lbs. The elastic nature of the insulator is quite helpful in making this force control possible without excessive variations due to slight changes in the protrusion height. Both protrusions are on the same side of the contact, which aids in maintaining contact straightness.

Contact design

The design of the contacts is severely constrained within a number of requirements:

1) Since the card is contacted on both sides, the connector contains opposing contacts. To prevent damage to other areas of the computer, these opposing contacts may not touch when the card is removed with power on.
2) The card thickness ranges from 0.059 to 0.069 inch. There is also warping on some cards. The contact must provide positive connection force over this thickness range.
3) The card insertion and withdrawal force must be controlled by the contact.

The insertion force is determined by the card bevel, the contact contour, the card thickness, the contact spring rate, and the friction characteristics. This force should be below the limits of operator convenience (about 30 lbs.). The withdrawal force must be adequate to hold the card in place. This force is determined by card thickness, contact spring rate, and friction characteristics. This withdrawal force is specified as a minimum of 2.0 to 2.5 lbs. with a polished steel gauge of 0.056-inch thickness—the actual force depending on the number of contacts in the connector (37 to 48).

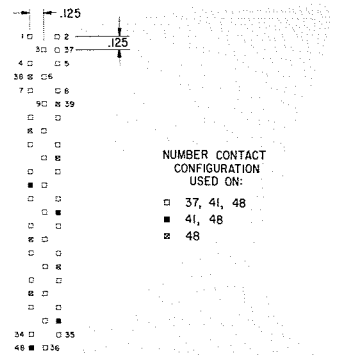


Fig. 3—Contact configuration.

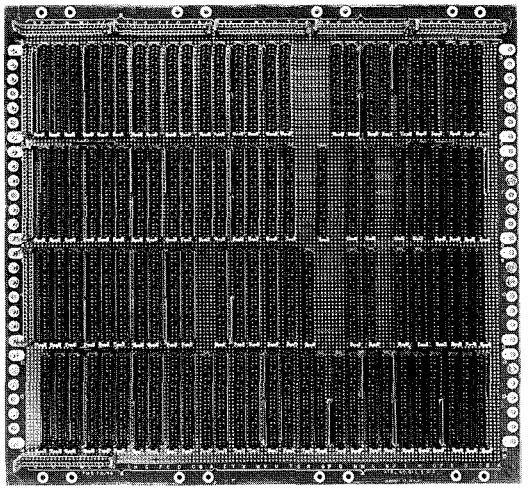


Fig. 2—Connector body side of platter.

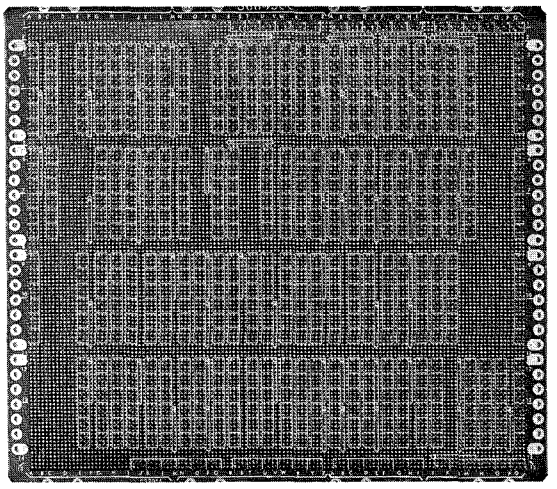


Fig. 4—Platter from solder side.

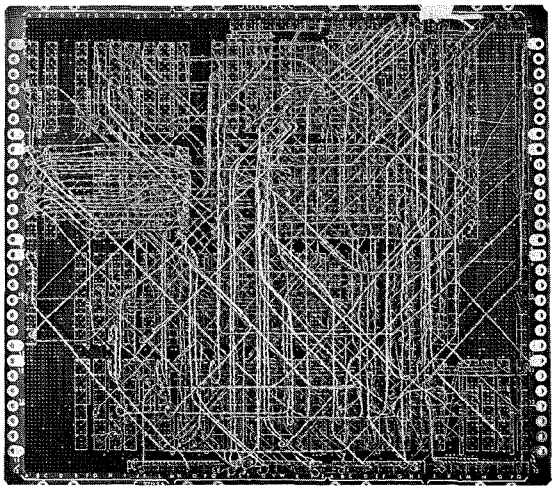


Fig. 5—Platter with wire wrap connections.

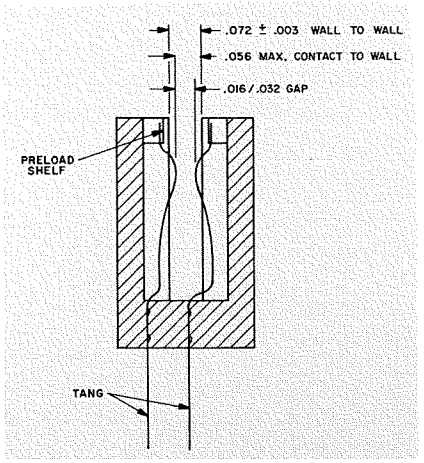


Fig. 6—Pad size for double card.

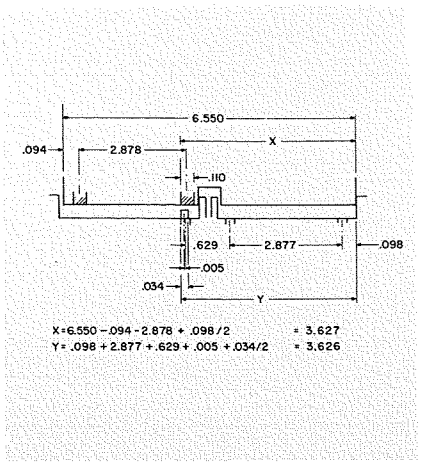


Fig. 7—Test gauge.

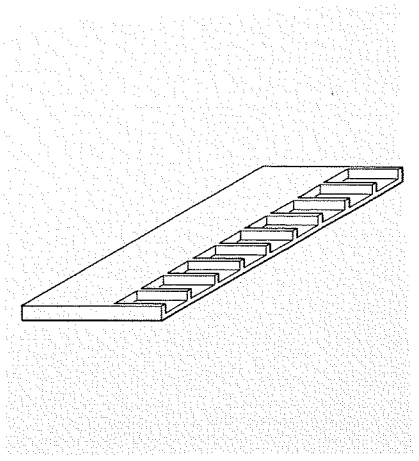


Fig. 8—Connector section.

There is a foam pad at the back of the card nest which provides incidental assistance in keeping the cards in the connectors. This pad dampens card vibration encountered during shipping. The pad also helps keep cooling air from bypassing the cards.

The prototype connectors employed a free-standing cantilever contact design. This was made to back up against the insulator side to shorten the cantilever and thus increase the contact force and withdrawal force. However, the tolerances involved here were too difficult to maintain. Contact forces over the range of card thickness could readily vary by a ratio of 3 to 1.

To prevent opposing contacts from touching while assuring a reliable contact to the thinner boards, a gap between opposing contacts of 0.020 to 0.032 was specified. Further, contacts within 0.053 of the opposing insulator wall were specified. This was intended for use with card thickness limits of 0.057 to 0.069. Since the tolerance buildup was unsatisfactory in these prototype connectors, the card thickness tolerance was changed to 0.059 to 0.069 after a survey of cards which indicated that almost none were in the thin end of the range. This permitted a change in the 0.053 contact-to-wall requirement to 0.056. At the same time, the contact-gap was changed to 0.016 to 0.032. Even with these relaxed specifications the connectors could not be produced with reasonable economy. Each one had to be very carefully inspected and contacts frequently changed.

A preloaded contact design was then introduced that has some very obvious advantages. It permits a longer cantilever, so that the force variations with varying board thickness is substantially reduced. It also makes control of the contact gap a comparatively simple matter. Even with the preloading, however, the accumulation of tolerances still requires precise manufacturing techniques. The following requirements and dimensions must be considered:

Contact gap	0.016 to 0.032
Contact to opposite wall	0.056 max
Wall to wall	0.072 ± 0.003
Wall to preload shelf	0.000 ± 0.001
Contact tip to preload face	0.000 ± 0.001

These are considered in Fig. 6, and the need for precision can be readily seen.

The preloaded contact, in combination with the elastic nature of the insulator, added another factor to the above considerations. The contacts pulled against the insulator, causing the casting walls to "cave-in" somewhat at the center. This situation is aggravated by the force fit of the contacts, which tends to swell the base and further distort the sides. Although some attempt was made to introduce an outward bow in the casting prior to insertion of contacts, the final solution was to go back at the specification again, permitting the gap to close an additional 0.004. Since the addition of the preloading feature, this seemed to present no danger of opposing contacts shorting.

The third row of contact tails in this connector dictated two different contact forms. Early designs provided not only a different tail arrangement, but also permitted this difference to influence the spring rate. The final design made alterations such that the lengths of the cantilever in both type of contacts are essentially identical.

The requirements of two different contact forms presented a definite design problem. The early free standing cantilever design backed the contact against the side of the insulator, and it was found that even the slightest variation in form would produce substantial changes in contact position. In the ultimate design, with a uniform cantilever length and a preload, the contour at the point of contact was identical.

The final problem in contact design was to achieve a satisfactory card withdrawal force. This problem stemmed, in part, from the fact that the pads on the card did not extend to the edge of the card. This small pad was used to insure that the pad did not act as a capacitor. The result was that a slight card withdrawal would cause contact to be lost. The pad was lengthened to overcome this problem.

The first connectors with preloaded contacts, although meeting all other requirements, had too low of a card withdrawal force. Examination of the design showed that the springs would stay within their elastic limit under all circumstances. The solution to this was to increase the preload distance, with the result that, in instances of maximum deflection, the contacts would exceed their elastic limit. It did, however, provide us with the maximum possible withdrawal force, and this met the specified requirement.

Contact tang

The contact tang must be sufficiently straight and accurately located to permit assembly to the platter, must accept solder, and must be capable of accepting wire wrap.

In the initial efforts to obtain contact tangs which could be readily inserted

in the platter, the specification required that tang tips must be with ±0.03 inch of true position and that the tips were to be tapered. It soon became obvious, however, that manual insertion of the connectors into the platters was a time consuming tedious operation. A comb device was then used, which would accurately position all tangs. The connectors must be installed in the proper sequence in order to remove the comb device parts in x and y directions.

The problem of mating the connector with the platter seemed rather difficult. The diagonal dimension of the tang was 0.036 inch, and the platter holes could be a minimum of 0.037 inch, thus requiring almost perfect alignment. To reduce the likelihood that some connectors would not seat, pads were added at each end of the connector, allowing a 0.06 inch clearance in which the tangs could bend when necessary. However, the elastic nature of the insulator provided sufficient movement so that the problem never developed in practice.

The connectors are soldered to the platter by a wave soldering process, so that the tangs are completely emersed in solder. It was thus necessary to conduct tests to determine if this would adversely affect the wire-wrap capability of the tang. The tests consisted of elevated temperature exposure of the joints with occasional disturbance to duplicate the effects of wire stress relaxation over a long period of time. The results showed that no difficulty would be encountered.

After some operating experience it was found that the small contact tangs were vulnerable to bending. In the case where the bent tang caused a short to a tang carrying voltage, component damage usually resulted. This problem has been eliminated by using a special short tang for voltage contacts.

Soldering

Two problems occurred in the soldering operation which should be noted. The first is that of holding the connectors to the platter during soldering, since the normal attachment is via the soldered contacts. The other is in the cleansing operation.

During very early equipment production, the connectors were held to the platter by a complex fixture. This fixture had to apply a light spring force to each connector so as to keep it tight to the platter during the heat flexure of the platter which occurs during the soldering. This force tended to produce a bow in the platters, which was not overly objectionable. Later, it was found much simpler to add a crimp in a few of the connector tangs, which hold the connector to the platter. This produces no damage to the thru-plated platter holes (determined by sectioning). The crimp also affects the pin straightness and makes inserting the connectors into the platter more difficult. But, in balance, the crimp is a less costly process than is the fixture.

The cleansing problem illustrates some unusual features. The insulator body was raised by pads on the end so that it was 0.06 off the platter. This provides plenty of room to vent solder flux gases trapped in the platter holes. In addition, it was necessary to add small feet on these pads. This prevented a situation where, after soldering, some flux residue could gather under the pad, where it would be difficult to wash out. After a period of time, this residue would develop a conductive path between the conductors. Two variations of feet were necessary, since the connectors were used in both vertical and horizontal positions on the platter.

Special applications

After the initial connector configuration had been determined, it was found that there was a substantial advantage in using a double size plug-in card with two connectors for certain circuits. This presented another design problem. If the edge of the card is at its maximum dimension, while the connector opening is at a minimum, then the two will just fit. If a second connector is to be used on the same card, then it would have to be in exactly nominal position, which could not be presumed. Therefore, a double-size card was made with smaller edges in order to fit two connectors at once. This made it necessary in turn to re-examine the size of the card pads. Fig. 7 shows that the size of the pad must be increased by about 0.014 inch, using the methods of Appendix B.

A second question arose concerning the warp in the card. If the card is started into the connectors on the lower guides of both connectors, the far edge will miss the guide center by approximately 0.07 inch with a normally permissible wrap. Since this application is unusual, the problem is simply overcome by manual effort. As far as insertion force goes, this double card is inconveniently high. However, the length is such that the board can be inserted one end after the other, without producing such an angle as to get the contacts off the proper pads.

A similar application involves the use of two double cards attached rigidly side by side. This produces the additional problem of lateral alignment, which is overcome by a certain amount of flexibility in the card. The problem of card insertion force is solved only by the expediency of inserting end by end and, in some measure, corner by corner.

Connector testing

The testing of connectors is divided into two categories: qualification tests and production inspection tests. The first is an extensive series of tests which includes every item in the specification and sometimes more. The second is a brief test intended to assure that no changes occur in the quality of the product.

The qualification tests included the following:

1) Dimension, material and finish checks, including sections of the gold-tip area;
2) Insertion and withdrawal force of specified steel gauge measured before and after 500 cycles and inspected for wear;
3) Contact retention and replacement force;
4) Salt-spray test, followed by insertion, withdrawal and conductivity test;
5) Examination of packing and marking;
6) Voltage drop at 400 mA;
7) Wire wrap voltage drop at 400 mA; and
8) Dry circuit at 25 mV.

The production inspection tests may repeat any of the above tests at the discretion of the quality supervisor. As a minimum, this test includes the insertion force, withdrawal force and the one crucial dimension—contact-point to opposing-insulator-wall.

This contact-to-wall dimension is measured by means of a brass gauge inserted in place of a card. The gauge is

designed so that it is hollowed out at the contact point of all contacts on one side, so that those on the other side push the gauge against the far wall. This gauge is shown in Fig. 8.

The connector being tested is placed in a test socket. Voltage is applied to one side of a light, the light to the contact, and the contact touches the gauge. A series of contacts thus brings voltage to the gauge, and a similar series brings in ground through lights.

Switches provide energy to lights when no contact is present, since the connectors must be tested with either 37, 41, or 48 contacts.

Conclusion

One of the most difficult tasks in the design of a printed-circuit card edge connector is to assure good contact pressure to the card under all circumstances. This is complicated by such other factors as ease of card insertion, card retention, prevention of shorting to adjacent pads or opposing contacts, contact wear and suitability of the materials to the application. The connector exterior must conform to the unique applications intended, such as attachment and connections.

Acknowledgement

Appreciation is expressed to G. R. Gaschnig, Engineering Group Leader, Information Systems Division, RCA, for assistance in the preparation of this paper. The author also acknowledges the contributions of a large number of persons whose efforts have added to the design and application of this connector.

Appendix A—Board-guide height

Worst case data (inches):

Card width	3.050 min.
Pad width	0.090 max.
Card edge to pad	0.094 max.
Contact width	0.034 max.
Contact to cavity centers	0.005 max.
Connector edge to contact	0.092 min.
Connector opening width	3.070 max.

From Fig. A-1, it can be seen that:

$$A \tan W + 3.050 \cos W = 3.070 \quad (1)$$

Referring to Fig. A-2, the edge of the first card pad to the edge of the card,

$$C, = 0.094 + 0.090/2 = 0.139$$

The second connector contact from the edge of the connector opening $B = 0.092 + 0.125 - 0.034/2 = 0.200$.

Since the contact may vary by 0.005 in its cavity, B assumes a value of 0.195.

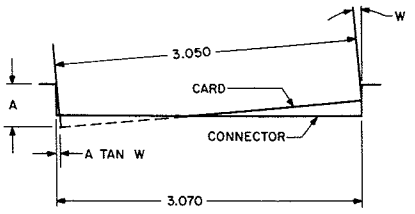


Fig. A-1—Card inserted at angle.

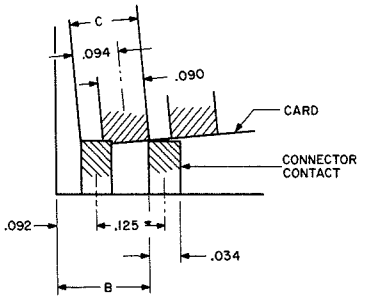


Fig. A-2—Angled card mating contacts.

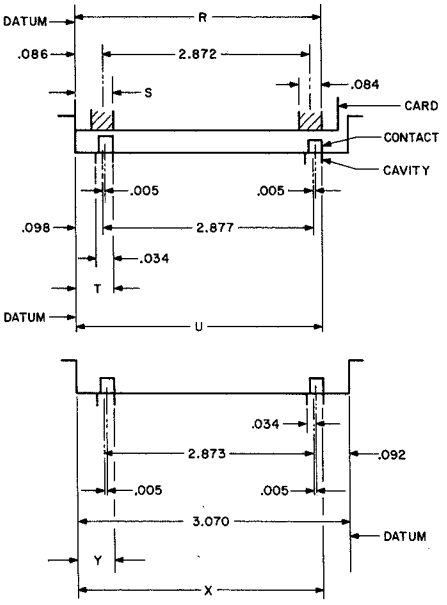
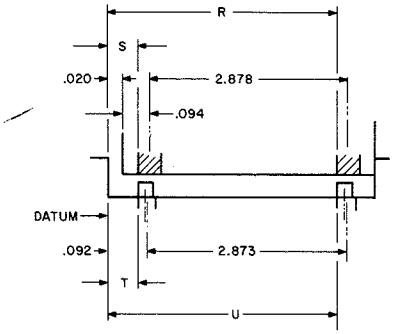


Fig. B-1—Pad size—card to left.



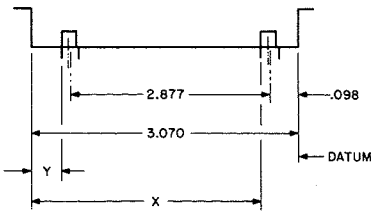


Fig. B-2—Pad size—card to right.

Therefore,

$$A \tan W + 0.139 \cos W = 0.195 \quad (2)$$

Subtracting Eq. 2 from Eq. 1:

$$2.911 \cos W = 2.875 \quad (3)$$

and

$$\cos W = 0.9876$$
$$\tan W = 0.1584 \quad (4)$$

where $W = 9°0'$

Substituting these values in Eq. 1

$$A\ (0.1584) + 3.050\ (0.9876) = 3.070$$

Then $A = .37$

A dimension A is the length of the card guide measured from the highest line of contact, rather than from the insulator lip, a difference of 0.08 inch. An allowance is also made for the fact that the card pads do not extend to the edge of the card, for which another 0.05 may be allowed. Subtracting these values, we find that the height of the card guide should be $0.37 - 0.08 - 0.05$, or 0.25, from the insulator lip.

Appendix B—Contact pad width

To ensure that the contact will always rest completely on the card pad, a narrow (3.050 inch) card width and a large (3.070 inch) connector opening are assumed. The card will be considered to the left first, with tolerances accumulated to push the card pads left and connector contacts right. Then the card will be considered on the right.

For the contact to rest completely on the pad (Fig. B-1) R must be greater than U or X, and S must be greater than T or Y.

$R = 0.086 + 2.872 + 0.084/2 = 3.000$
$U = 0.098 + 2.877 + 0.005 + 0.034/2 = 2.997$
$X = 3.070 - 0.092 + 0.005 + 0.034/2 = 3.000$
$S = 0.086 + 0.084/2 = 0.128$
$T = 0.098 + 0.005 + 0.034/2 = 0.120$
$Y = 3.070 - 0.092 - 2.873 + 0.005 + 0.034/2 = 0.127$

This shows that the contact will be on the pad and from this the connector tolerance may be accumulated from either side.

Refer to Fig. B-2, which is similar to Fig. B-1 and missing dimensions are identical. In this case, R must be less than U or X and S must be less than T or Y:

$R = 0.020 + 0.094 + 2.878 - 0.084/2 = 2.950$
$U = 0.092 + 2.873 - 0.005 - 0.034/2 = 2.943$
$X = 3.070 - 0.098 - 0.005 - 0.034/2 = 2.950$
$S = 0.020 + 0.094 - 0.084/2 = 0.072$
$T = 0.092 - 0.005 - 0.034/2 = 0.070$
$Y = 3.070 - 0.098 - 2.877 - 0.005 - 0.034/2 = 0.073.$

These figures indicate that the contact can be over the edge of the card pad if the connector tolerance is accumulated from the same end as the card tolerance. For this reason, connector tolerances are specified from the opposite end.

The analysis of reflections in lossless transmission lines

R. S. Singleton

A large number of circuit analysis problems are concerned with the voltage (or current) waveform resulting from multiple reflections caused by impedance mismatches at the sending and receiving ends of a transmission line. This paper discusses the theoretical foundation and practical application of the straightforward graphical method of solution for those cases where the line may be assumed lossless and the terminating impedances resistive (although not necessarily linear).

R. S. Singleton
Memory Engineering
Information Systems Division
Palm Beach Gardens, Florida
received the BSEE from the University of Florida 1959, and the MSEE from New York University 1961. He joined the Bell Telephone Laboratories at Murray Hill, N.J. after graduation and two years later joined the Martin Co., Orlando, Florida where he worked on various areas of computer design. For the past three years he has been with RCA as a member of the Engineering Staff of the Memory Engineering Department of the Information Systems Division. Mr. Singleton is also an Adjunct Professor of Electrical Engineering at the University of Florida Palm Beach Graduate Center.

HIGH-SPEED switching circuits, such as those found in modern digital computers, have voltage and current pulses whose rise times are often so fast that the connecting wires must be treated as a transmission line. When rise times are less than the propagation times between circuits, reflections from sending and receiving ends of the line introduce distortion.

Reflections on transmission lines are usually well understood when the terminating impedances are linear, but not when they're nonlinear, as in a base-emitter junction.

A graphical technique of solving for reflections has several advantages over other approaches. It can be used with either linear or nonlinear loads. The technique is fast and simple because the engineer doesn't have to work with the complicated transmission-line equations usually applied. He need only know the source, line, and load impedances, draw three lines related to the slopes of these impedances, and follow certain graphical procedures.

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Using the graphical technique with linear terminations

As an example of the use of the graphical technique, assume that a lossless line with characteristic impedance of 50 ohms is driven with a 0.6-volt step by a 25-ohm generator and has an open-circuit load termination. The circuit is shown in Fig. 1.

First, construct the sending and receiving end conductance lines as shown in Fig. 2 using polarities defined in Fig. 1. Lines are constructed with slopes of the proper conductance and are located by using the network boundary conditions listed in Table I.

Table I—Network Boundary Conditions

Parameter	*Sending end*	*Receiving end*
Conductance (slope)	1/25 ohms	1/∞
Slope Polarity	Negative, (as v_s increases, i_s decreases)	Positive, (as v_r increases, i_r increases)
Intercept	$v_s=0.6$, $i_s=0$	$1_r=0$

Second, starting at the $t=0^-$ conditions, construct the transmission conductance line. At its intersection with the sending end conductance line note the sending end solution at $t=0^+$ and construct the (−) transmission conductance line. At the intersection with the receiving end conductance line note the receiving end solution at $t=\tau$ and construct the (+) transmission conductance line. This process is continued as shown in Fig. 3, finally converging at the intersection of the sending and receiving conductance lines, i.e., the final value of the line transient.

From the graphical solution of Fig. 3, the terminal waveforms can be constructed. As an example, the sending end voltage is sketched in Fig. 4a. Fig. 4b shows an oscilloscope photograph of the sending end voltage of the actual circuit operating in the laboratory.

Using the graphical method with non-linear terminations

Terminating impedances need not be linear to use this method of solution. It is sufficient that they be characterized as resistive. Consider, for example, the solution for the sending end voltage waveform of the same circuit with a diode across the receiving end. This circuit and its reflection diagram are shown in Fig. 5.

The sending end voltage is sketched, as before, from the reflection diagram and shown in Fig. 6a. Fig. 6b is an oscilloscope photograph taken from the actual circuit under test.

Determining reflections in other types of networks

Application of the superposition theorem permits the graphical method to be used for problems where driving sources appear at both ends of the line, and for problems where the driving functions are more complex than the step function already discussed. In the former case, reflection loss is determined by solving for the sending and receiving end waveforms separately and then superimposing them for the total solution. In the latter case, the loss is calculated by fragmenting the driving function into appropriate step functions, solving for each step individually and superimposing the resultant waveforms into a total solution.

As an example, assume that in a transmission line terminated by a diode the

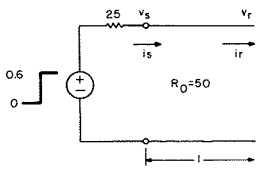


Fig. 1—A pulse is applied to a 50-ohm transmission line (i_s and i_r represent the sending and receiving currents).

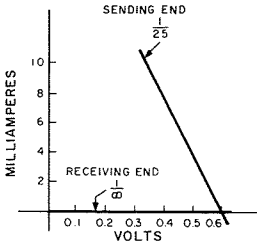


Fig. 2—The lines correspond to the conductance of the load impedance of the receiving end and to the conductance of the source at the sending end.

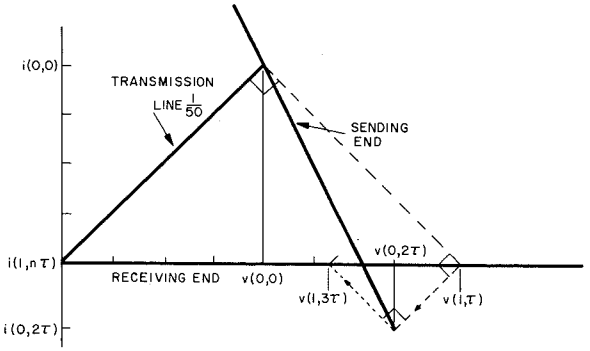


Fig. 3—A third line is added (to Fig. 2) that corresponds to the conductance of the transmission line. The point where the transmission line intersects the sending-end line represents the value of voltage and current before it is sent down the line. With negative slope to the transmission line and through this point, draw a line until it intersects the receive-end line. This intersection represents the voltage-and-current at the load at timeτ. A perpendicular from this point intersects the sending-end line, representing the voltage and current at the sending end at time 2τ. The process is continued until the dashed line converges to a point.

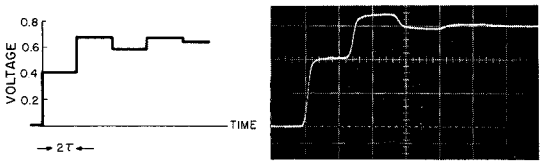
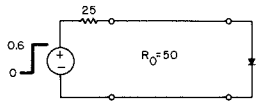


Fig. 4—Voltage at the sending end as a function of time indicates the additions and subtractions that result from the reflections: a) plot b) oscillograph.



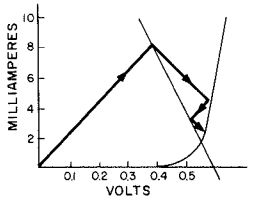
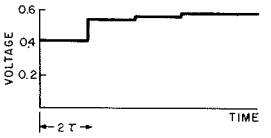


Fig. 5—A diode is the load to a transmission line; the currents and voltages are calculated from the graph.



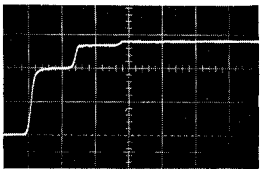


Fig. 6—Voltage values at the sending end of a transmission line terminated by a diode: a) calculations, b) oscillograph.

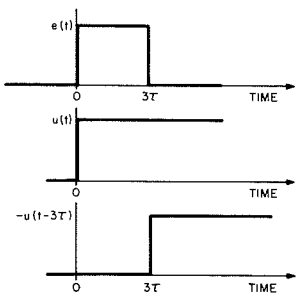


Fig. 7—Pulse waveform at top can be formed by the algebraic addition of the two pulses.

driving function is a rectangle of width 3τ. This pulse can be treated as one composed of two step functions, as shown in Fig. 7.

Solutions for the two step functions are found as before, and the results superimposed. Using the solution already obtained for the sending-end voltage, the waveforms are superimposed as shown in Fig. 8. The actual measured waveform is compared with the one obtained by super-position.

Applications in the Spectra 70 product line

The graphical techniques described above have already found useful application in the circuit and system design of the Spectra 70 computer line. A paper by Fulcher and Saenz[3] discusses the reduction in reflections that was attained in the Series 1600 system as a result of reflection diagram analysis of TTL gates. The analysis clearly revealed the characteristics of the input diode that are necessary to provide low-amplitude reflections from receiving end gates. This characteristic has been incorporated as a purchase specification and each vendor has altered his TTL line accordingly.

In the design of the Series 1600 memory system, reflection diagram analysis of the drive lines permitted the relationships between circuit parameters and current waveforms to be predicted. As an informative study in superposition, Fig. 9 shows the analysis of the Series 1600 drive-line current. It is interesting to note that the use of a current "source" may, in reality, result in distortion of line current due to mismatching and reflections .

The theory behind the method

The solution for the reflection voltages and currents is based upon the basic transmission line (see Fig. 10) equations for finite current and voltage. These are expressed by

$$I(x,s)=\frac{V_1(s)}{Z_s+Z_o}\,e^{-\gamma x}\,\frac{1-\rho_r e^{-2\gamma(l-x)}}{1-\rho_s\rho_r e^{-2\gamma l}} \quad \text{and}$$

$$V(x,s)=\frac{Z_o V_1(s)}{Z_s+Z_o}\,e^{-\gamma x}\,\frac{1+\rho_r e^{-2\gamma(l-x)}}{1-\rho_s\rho_r e^{-2\gamma l}},$$

where

$\rho_r=\dfrac{Z_r-Z_o}{Z_r+Z_o}$ = the receiving-end voltage reflection ratio,

$\rho_s=\dfrac{Z_s-Z_o}{Z_s+Z_o}$ = the sending-end voltage reflection ratio.

$\gamma=\sqrt{(R+sL)(G+sC)}$ = the propagation constant,

and

$Z_o=\sqrt{\dfrac{R+sL}{G+sC}}$ = the characteristic impedance.

Expanded into infinite series, these general solutions become

$$I(x,s)=\frac{V_1(s)}{Z_s+Z_o}\{e^{-\gamma x}-\rho_r e^{\gamma(x-2l)}+\rho_s\rho_r e^{-\gamma(x+2l)}-\rho_s\rho_r^2 e^{\gamma(x-4l)}+\cdots\}$$

and

$$V(x,s)=\frac{Z_o V_1(s)}{Z_s+Z_o}\{e^{-\gamma x}+\rho_r e^{\gamma(x-2l)}+\rho_s\rho_r e^{-\gamma(x+2l)}+\rho_s\rho_r^2 e^{\gamma(x-4l)}+\cdots\}.$$

The series solution describes an infinite series of waves propagating from points at $\pm 2nl$. The significant advantage in this interpretation is that the terms can be examined one at a time as they enter the problem's time sequence. The values at the end of each section are then added algebraically to give the total reflection for the line.

The lossless line is a useful approximation for most transmission-line applications. This is especially true at relatively high frequencies, where the s terms dominate the non-s terms in the equations for the propagation constant and the characteristic impedance. As an example, for a 50-ohm microstrip transmission line $R=0.5$ ohm/foot, $L=90$ nanohenries/foot, $C=36$ picofarads/foot, and $G=2$ picomhos/foot. Thus, at frequencies beyond 8 megahertz, $sL>>R$ and $sC>>G$.

In a lossless line the propagation constant is $\gamma=s\,(LC)^{1/2}$, and the characteristic impedance is $Z_o=(L/C)^{1/2}=R_o$, which is purely resistive. Assuming such a case with both the sending and receiving ends connected to resistors, the traveling-wave solution for the sending end of the line becomes

$$I(0,s)=\frac{V_1(s)}{R_s+R_o}\{1+\rho_r e^{\gamma 2l}+\rho_s\rho_r e^{-\gamma 2l}-\rho_s\rho_r e^{-\gamma 4l}+\cdots\} \quad \text{and}$$

$$V(0,s)=\frac{R_o V_1(s)}{R_s+R_o}\{1-\rho_r e^{\gamma 2l}+\rho_s\rho_r e^{-\gamma 2l}+\rho_s\rho_r e^{-\gamma 4l}+\cdots\},$$

and for the receiving end

$$I(l,s)=\frac{V_1(s)}{R_s+R_o}\{e^{-\gamma l}-\rho_r e^{-\gamma l}+\rho_s\rho_r e^{-\gamma 3l}-\cdots\}$$

and

$$V(l,s)=\frac{R_o V_1(s)}{R_s+R_o}\{e^{-\gamma l}+\rho_r e^{-\gamma l}+\rho_s\rho_r e^{-\gamma 3l}+\cdots\}$$

If a step input is applied at the sending end, $V_1(s)=V_1/s$, the above equations can be solved at the time intervals $n\tau$ where $\tau=(LCl)^{1/2}$ the one-way propagation time of the line. Thus, at $t=0^+$ the sending end appears as

$$I(0,s)=\frac{V_1}{s(R_s+R_o)} \quad \text{and}$$

$$V(0,s)=\frac{R_o V_1}{s(R_s+R_o)},$$

which in the time domain transforms into

$$i(0,0^+)=\frac{V_1}{R_s+R_o} \quad \text{and}$$

$$v(0,0^+)=\frac{V_1 R}{R_s+R_o}.$$

Note that this is the intersection of the two lines. Each line has a slope equivalent to the conductance: $1/R_s=i/(V_1-v)$, the sending-end conductance, and $i/R_o=i/v$, the transmission-line conductance. This is displayed graphically in Fig. 11.

At $t=\tau$, when the traveling wave has reached the receiving end of the line

$$I(l,s)=\frac{V_1}{s(R_s+R_o)}(1-\rho_r) \quad \text{and}$$

$$V(l,s)=\frac{V_1 R_o}{s(R_s+R_o)}(1+\rho_r),$$

which transforms into the time domain as

$$i(l,\tau)=\frac{V_1}{R_s+R_o}(1-\rho_r) \quad \text{and}$$

$$v(l,\tau)=\frac{V_1 R_o}{R_s+R_o}(1+\rho_r).$$

These last two equations are solutions of the intersections of the two lines, $1/R_r=i/v$, the receiving-end conductance, $1/R_o=i/v$, the negative transmission-line conductance, where the current in the latter expression is shifted by $V_1/(R_s+R_o)$ and the voltage is shifted by $V_1R_o/(R_s+R_o)$, the same amounts of the previous solution at $(0,0^+)$. This is graphically displayed in Fig. 12.

This iterative process can be continued to show that the solution for terminal conditions at time $n\tau$ is the intersection of the lines

$$i-i([n-1]\tau)=\frac{(-1)^n}{R_o}[v-v([n-1]\tau)],$$

with $i=\frac{V_1-v}{R_s}$, for n even (sending end)

and $i=\frac{v}{R_r}$, for n odd (receiving end).

Concluding remarks

A solution, then, can be found by drawing the load line for the sending- and receiving-end resistances, then alternately projecting the load line of the transmission line and its reciprocal to where they intersect the sending- or receiving-end load lines. These intersections form the time-series solution for the equations as demonstrated in the previous example.

It is well known that when a transmission line is not terminated in its characteristic impedance and is excited with a wave front whose transition is faster than the delay of the line, ringing can occur on the line. With the advent of computer circuits which are capable of switching in one nanosecond, this is precisely the position in which the designer finds himself. Consequently, the engineer is forced to use transmission-line concepts in dealing with the propagation of data from one point to another within a machine using such circuits.

The reflection diagram described in this article is an extremely useful tool for analyzing such conditions and aiding the circuit designer to either avoid ringing or to take advantage of it. Examples of problems in which the technique has been utilized are:

- Reduction of distortion of otherwise controlled waveforms caused by ringing.
- Reduction of ringing which leads to logic circuits misoperation by its introduction as noise.
- Reduction of ringing which leads to device failure by overstress and breakdown.

Acknowledgment

The author would like to acknowledge an unpublished report "Line Ringing with Logic Circuits" by Mr. John B. James of International Computers and Tabulators Ltd., in which, to the author's knowledge, the first heuristic use of the reflection diagram was proposed.

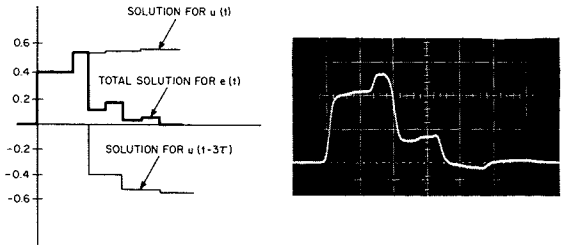


Fig. 8—When more than one voltage source is applied to a transmission line, the voltage at the sending end can be calculated by assuming separate signal voltages and then adding the results together: a) calculated waveform b) oscillograph.

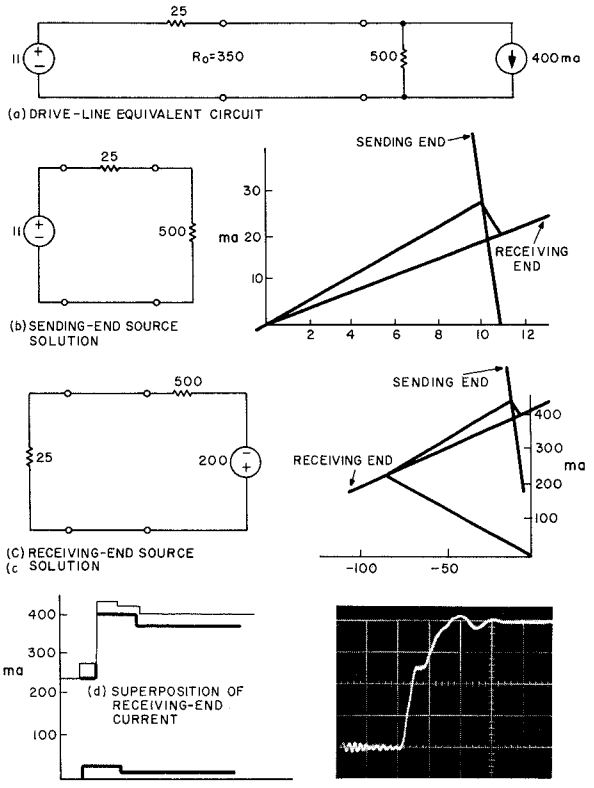


Fig. 9—Graphical technique and superposition are used to calculate sending- and receiving-end voltages in memory-system whose line impedance is 350 ohms.

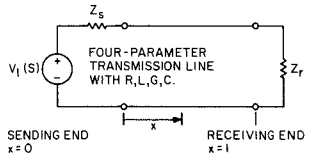


Fig. 10—Conventional transmission-line net-work is divided into three sections—source (sending end), line (center), and load (receiving end). Parameter X represents length of line. At the load the line is l units long.

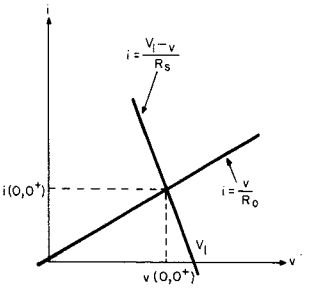


Fig. 11—The point at which the sending-end conductance line crosses the transmission-end conductance line represents the value of voltage and current as it starts down the line.

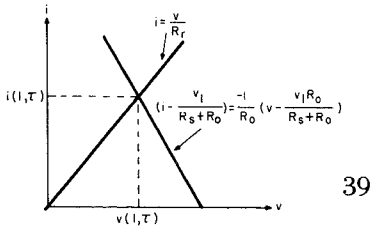
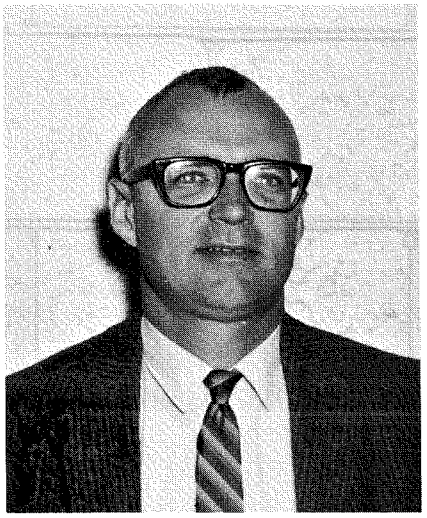


Fig. 12—The intersection of the receiving-end conductance line and the transmission-line conductance line represents the point of voltage and current as they appear at the load impedance.

Diagnosis at the microprogramming level

R. C. Calhoun

The DIAGNOSE instruction included in the instruction repertoire of the RCA Spectra 70 line serves as a powerful maintenance aid for field engineering personnel. Operating at the microprogramming level, this instruction isolates trouble on a building-block confidence approach. The application of this approach to the Spectra 70/35 computer is the subject of this paper.



Robert C. Calhoun, Ldr.
Special Projects Group
Test Programming
Information Systems Division
Palm Beach Gardens, Fla.

received the Associate in Electrical Technology from Westchester College in White Plains, New York and the BA in Liberal Arts from Syracuse University. He came with RCA in 1966 following associations with General Electric (Information Systems Division) and Xerox's Scientific Computing Center. He has been associated with the computer field since 1957, when he entered the field as a Systems Engineer. With RCA he was instrumental in the development and implementation of the Spectra 70/35 E/O diagnostics and is presently Leader of the Special Projects Group of Test Programming. Mr. Calhoun has done extensive work with various computer languages and is currently involved with development of software techniques for management information.

IN THE PAST FIFTEEN YEARS, the evolution of the general purpose computer has been spectacular. This evolution of highly sophisticated and complex hardware has put tremendous strain on the groups responsible for reliability and maintainability. The pressure of competition in the market-place has required a thinning of trained maintenance personnel due to product cost impact while the lack of a sufficient number of adequately trained technicians has thinned this maintenance force further. Since a computer complex must be in an UP condition, it is easy to see that the problem of maintainability has to be solved.

Fortunately, designers of third generation equipment have recognized a trend away from *maintainability* and are beginning once again to incorporate adequate maintenance aids into the hardware design. One of the most promising of these is the DIAGNOSE instruction included in the instruction repertoire of the RCA Spectra 70 line. For our purpose, we will consider the DIAGNOSE operation as it relates to the RCA Spectra 70, model 35 as a representation.

The EO instruction

The 70/35 is a medium-scale general-purpose system dependent upon an elementary operation (EO) program residing in a read-only memory. Each instruction executed in the machine causes a unique series of EO steps or functions to be performed. This series of functions comprise the microprogram that obtains the correct result required by the instruction being executed.

Since we can now sub-divide an instruction into component parts, or EO steps, we can analyze the operation of a processor at a function or even sub-function level. As an example, let us analyze symbolically a simple instruction in terms of the EO steps required to obtain the results of a successful execution of that instruction.

The Load Register instruction takes the contents of the second register specified in the instruction and loads them into the first register specified. Thus the instruction:

LR 1,2

will take the complete contents (32 bits or 4 bytes) from register 2 and will load them into register 1. Since the Spectra 70/35 utilizes a scratch pad memory for its registers, this operation requires a series of read and write memory functions. Following the completion of the previous instruction, the contents of a program counter would provide the address of our load register instruction. The LR instruction would be fetched from main memory and loaded into two hardware registers. The instruction itself is loaded into a function register (F) and the address (1,2 in this example) is loaded into a source and destination register (G). The instruction code found in the F-register will provide the address of the EO program in read-only memory associated with this instruction. In a symbolic fashion, this EO program would now perform the functions listed in Table I.

This example has been considerably shortened and simplified, and the instruction used as an example is also quite straightforward. However, it is sufficient to indicate some of the EO functions used to obtain an instruction result.

As can be seen by the example, the execution of a single machine instruction is in reality the successful execution of an EO or micro-program that has subdivided the instruction into component parts. Utilizing the DIAGNOSE instruction now allows a test of the computer system not at the instruction level but at the function level where hardware and control signals are at a minimum.

Sample diagnostic instruction

The DIAGNOSE instruction uses main memory as the source of each EO and consequently allows complete programming freedom at a function level. Thus, the first function used in our Load Register instruction (G right → MAR) can be tested in a stand-alone fashion. Notice, there is no involvement of other registers used in the Load Register instruction. This therefore allows tight isolation of a specific hardware area—in this case, two registers (G and MAR), a transfer buss, and minimum of controls.

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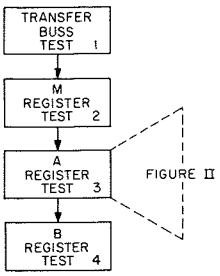

Fig. 1—General diagnostic flow.

With the capability outlined, it is now possible to write complete diagnostic routines that can test a computer processor at a function level. There are two obvious approaches that may be taken in the creation of this diagnostic. Tests can be performed at the instruction level until a problem is encountered. At this point, control can be given to a Diagnose instruction that provides complete testing of the individual functions used in the performance of the failing instruction. The primary weak point to this approach is the fact that the occurrence of a problem cannot always be determined as occurring within a specific instruction. In addition, the size of present instruction repertoires, coupled with differing program states and numerous registers, indicate a mammoth task to insure covering all exigencies.

The alternative approach provides for the test of the processor completely at the function level. In this approach, the more basic and necessary functions are tested, and these in turn are used to provide a test on unique hardware. This building block approach utilizing individual functions is desirable because it provides the maintenance man with the ability to eliminate segments of hardware based on the successful completion of earlier tests. As an example, in the RCA Spectra 70/35 diagnostic package one of the first tests is made on the transfer buss. If a transfer from one hardware register to another fails later in the microprogram, the transfer buss can be eliminated as a causative agent due to its successful use earlier in the program. In addition, the register-to-register transfer employs as the source register one which was previously checked. (Except in the case of the first register checked.) Thus, the process of elimination leaves us with the destination register as the prime, if not the only, suspect. Incorporation of a tight test-loop capability, selectable by the operator, provides a built-in scoping capability. Thus a preliminary diagnose to a restricted area is made and a test equipment assist is provided.

1) G right	→ MAR	1) Set up the address of the second, or source register 2, in the memory address register.
2) *CSPM, RR	→ MR	2) Read the right half of scratch pad to the M register (right half).
3) CSPM, RL	→ ML	3) Read the left half of scratch pad to the M register (left half).
4) G left	→ MAR	4) Set up the address of the first, or destination register 1, in the memory address register.
5) CSPM, WL	→ ML	5) Write the left half of the M register into the left half of the memory address setup in step 4.
6) CSPM, WR	→MR	6) Write the right half of the M register into the right half of the memory address set up in step 4.
7) STAT		7) Fetch next instruction.

*CSPM: cycle scratch pad memory.

Table I—EO program functions.

A further benefit gained by use of this second method of diagnostic generation is the implied inclusion of the first approach by coupling the EO function program with the standard confidence routines. Thus, from two stand-alone programs, a third emerges. They can be used individually or together as the situation warrants.

The approach taken in implementing the diagnostic tests on the Spectra 70/35 utilizes the function checking philosophy. This approach has simplified the task of fault isolation by building successive levels of confidence in the hardware.

Fig. 1 shows a simple flow of the order in which hardware is tested. Since confidence in some basic hardware area (hard core) is required, assume that the original hard-core tests have been performed prior to the entrance to Block 1, Transfer Buss Test. A bit pattern is transferred from a known good register to a second known good register. Since both registers involved are known to be operable, if the results found in the second register differ from the first, the buss must be at fault. If they agree, the diagnostic continues to Block 2 where a bit pattern in one of the original hard-core (good) registers is transferred, on the transfer buss just checked and found good, to the M register. If the contents of the M register are as expected following this transfer, the program continues along the normal path to Block 3, A Register Test, with the confidence that the M Register is operable. The diagnostic continues low level or function testing until all the processing unit hardware accessible to elementary operations has been found operable.

If no trouble exists, the diagnostic test functions as a hardware confidence or reliability routine. If, however, a symptom is detected, a diagnosis is made and conveyed to the operator. Since the test is performed on a simple logic net (i.e., a flip-flop register), a diagnostic conclusion also can be reached.

An expansion of Block 3, Fig. 1 is provided in Fig. 2. Notice the error path taken if the results of the transfer into A from M using the transfer buss are not as expected. The diagnostic decision becomes relatively simple due to the involvement of only one unknown —the operability of the logic net comprising the A register.

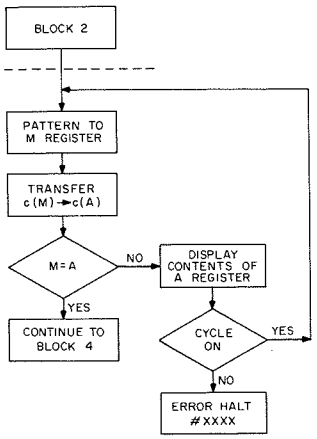

Fig. 2—Detail of block 3 of Fig. 1 "A Register Test."

Applications

The building block confidence approach has been found not only functional in the field environment where mean-time-to-repair is of significance but also in a factory test situation where unit and systems tests determine the meeting of shipping schedules. It has become a valuable tool for maintaining today's complex computer systems.

Conclusion

The industry has not yet reached the degree of sophistication where a computer system can diagnose and repair its ills, but it at last seems to have found the path toward providing better and more useful tools for the maintenance force.

Digital computers in space engineering

R. Goerss

Since early 1959, AED has used digital computers to solve engineering problems inherent in the design, development, and testing of spacecraft and space systems. From 1959 to 1967, a family of generally usable programs or tools have been developed. These programs are not restricted to a specific spacecraft configuration, and encompass many physical disciplines including thermal dynamics, mechanical analysis, electronics and circuit theory, and flight dynamics. The majority of these programs have been "space proven" by the close correlation of data receive from such actual space projects at TIROS, Nimbus, Ranger, and Lunar Oribiter, and other, classified, projects. This paper describes some of the most significant of these programs and their application to AED engineering effort.

Robert H. Goerss, Ldr.
Data Processing and Computation
Astro-Electronics Division
Princeton, N.J.

received the AB in Mathematics from the University of Buffalo in 1949. As a mathematician at the U.S. Naval Proving Ground, he programmed exterior ballistic trajectories for all types of armaments on the Harvard Mark II and III computers. At the James Forrestal Research Center in Princeton, he was a research assistant and associate in charge of a computation center. He also made contributions in the area of specialized numerical techniques for the solution of aerodynamic mission analysis problems and chemical reaction studies. From 1956 to 1958, as a senior engineer in charge of digital computations at Electronic Associates, Inc., he supervised a digital computer center. He also developed a three-address speed coding system and did system design of special computing units. With Astro-Electronics Division from October 1958 to September 1959, as a consultant programmer, he had full responsibility for setting up problems in satellite temperature calculation, albedo calculation, vibration analyses, and intelligence data processing demonstrations, and was a technical member of the committee for the study of AED's computer requirements. Since September 1959, he has been supervising all engineering and scientific programming and has responsibility for training members of AED's engineering staff in the use and application of computers. Mr. Goerss has written several technical papers and is a member of the Association for Computing Machinery.

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IN 1958, the space industry was characterized by the development of prototypes. Systems were relatively simple, little was known of mathematical analogs, testing was limited, and documentation requirements were minor. In 1959, however, high-speed digital computers were introduced to aspects of spacecraft engineering at AED. As the scope of this type of assistance increased, computer programs were developed to solve common physical problems inherent in space engineering. These are continuously being modified to reflect the increased complexity of spacecraft as well as advances in the state of spacecraft engineering. Up to the present time, significant computer contributions to AED spacecraft design have been made on such important projects as TIROS, Relay, Ranger, Nimbus, SERT, and Lunar Orbiter. Excellent correlation has been obtained between computer predictions and actual flight-performance data from the spacecraft.

Types of engineering support

In general, AED engineering computer applications fall into the following three major areas:

Analytic and scientific: Computer programs or simulation used to support the design of a space system, subsystem, or component. Studies performed vary from simulation of a complex multisatellite operational system to the performance analysis of a particular circuit board.

Spacecraft performance verification: Components of a spacecraft usually are tested under simulated environments. During this process, many measurements are made with appropriate sensors (thermocouples and accelerometers) of (1) the electrical outputs of the unit as a function of a complex set of stimuli, and (2) the environmental parameters.

Computers are used extensively to control the generation of electronic stimuli from test equipment, to monitor and reduce the response from the unit under test, and to process the tremendous volume of sensor data. The computer output is used both for immediate evaluation and for contractually required end-item documentation as a proof of compliance with specifications.

Engineering documentation: At AED, several major computer programs have been developed to accumulate items from parts lists, drawing breakdown lists, wiring lists, and similar basic engineering documents into data banks from which material may be selected and translated into direct working documents for various AED activities and for submission in fulfillment of contractual requirements.

A more detailed discussion of the analytic and scientific programs will be given in the remainder of this paper. The author hopes to publish detailed discussions of other types of computer assistance in subsequent papers.

Analytical and scientific computation

Automatic board wiring system

Perhaps the most interesting application in this field (still under development) is the automated production of photomasters for printed circuit boards. The present time-consuming, manual method is replaced by programming a computer with a continuity list and such board parameters as modular size, pin placement, and edge-connector definition.

With this input data, the computer program locates the modules on the board; automatically routes the circuits, generating thru connections and supplemental layers; and enters the data on a tape. The tape is then used to direct a plotter that produces the photo-masters. The top layer of a computer-generated circuit board is shown in Fig. 1.

Position determination and trajectory analysis

The position and trajectory of a spacecraft will dictate the thermal- and solar-energy inputs as well as the ground-to-spacecraft communications constraints and mission effectiveness. For many earth-orbiting operational spacecraft, position of the spacecraft as a function of time can be predicted efficiently by solving the classical equations of an elliptical or circular orbit (with the orbital parameters as inputs).

Where more precise trajectory calculations are required (for example on interplanetary problems, transfer orbits, etc.), the equations of motion must be numerically integrated. Frequently the initial position and velocity are specified; however, for some types of analysis, the trajectory must be optimized with respect to propulsion requirements, time, etc.

Attitude control

Precise prediction and control of attitude is required for a variety of mission and design considerations, including picture coverage and orientation, communication coverage, solar and thermal inputs, etc. On earth-orbiting spacecrafts, the deviation of attitude is primarily the result of the interaction of the spacecraft's magnetic field with the earth's magnetic field.

Most spacecraft designed by AED use torquing coils to control the spacecraft magnetic field as a function of the current through these coils. A family of digital-computer simulation programs has been developed to simulate the various devices that control the current through the coils and to integrate the necessary differential equation. These programs have been used extensively for both system analysis and actual in-flight operational control and are completely space tested. Other data of critical interest, including angle of incidence to the sun, percent of time in sunlight, etc. are produced by the programs. A typical plot of variation of spacecraft attitude on sequential orbits, developed from simulated data, is shown in Fig. 2.

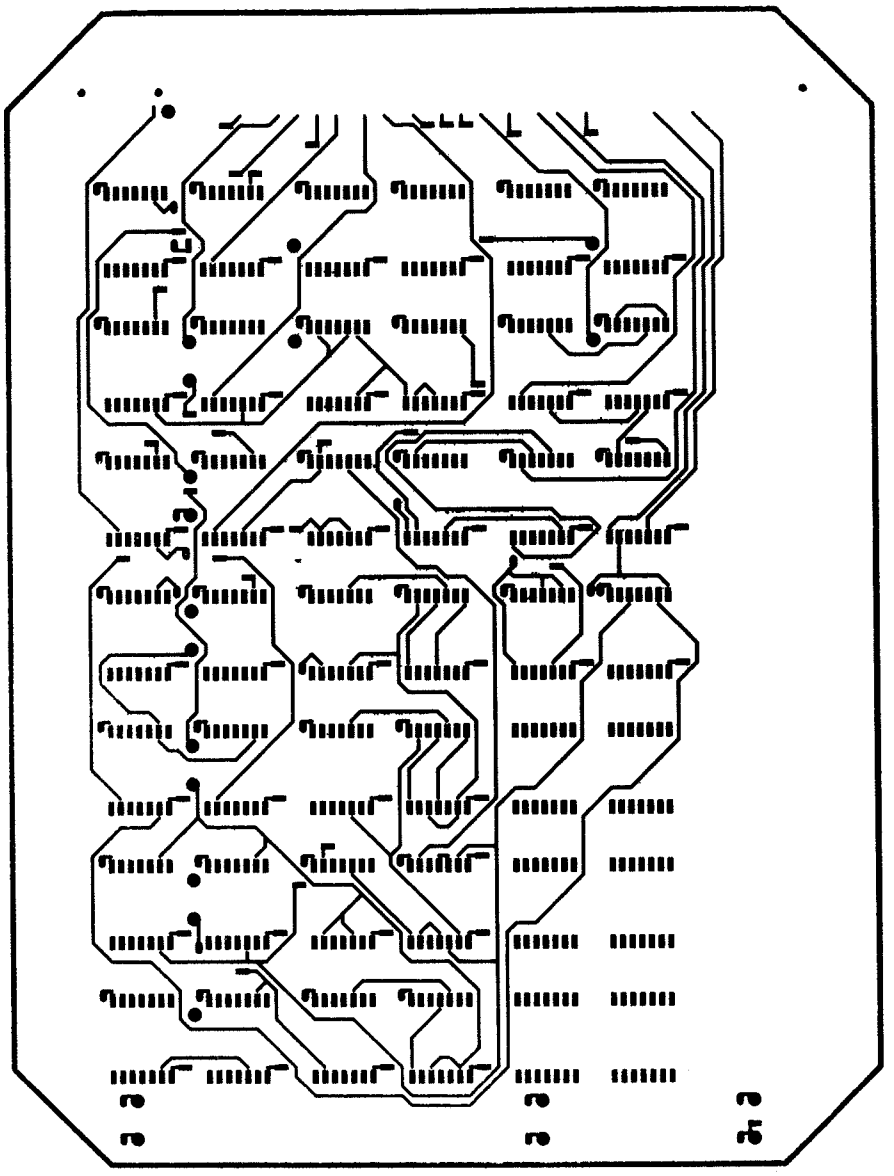

Fig. 1—Computer-generated printed-circuit board.

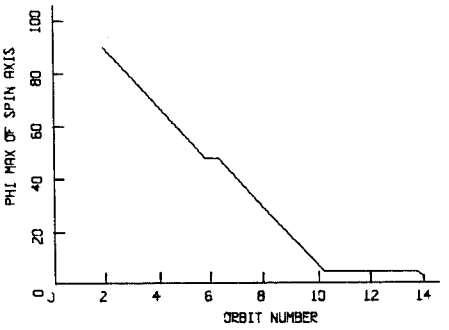

Fig. 2—Computer plot form simulated data of spacecraft's attitude-angle shift per orbit.

Thermal dynamics

It is important to maintain specific temperatures of the major components of an in-flight spacecraft if the performance capabilities and lifetime potential of the spacecraft are to be realized. In addition to the constraints on battery temperature, spacecraft vidicons need a thermal environment of from 5 to 30°C. Other components, such as precision clocks and infrared detectors, have equally stringent constraints. The computer programs that have been developed to produce accurate thermal predictions are used to determine:

Absorptivity and emissivity of the spacecraft material by the numerical integration of spectrometer readings;

Amount of thermal energy received from the sun (and in the case of an orbiter, the central body) as a function of position, spacecraft orientation, and the characteristics of the central body;

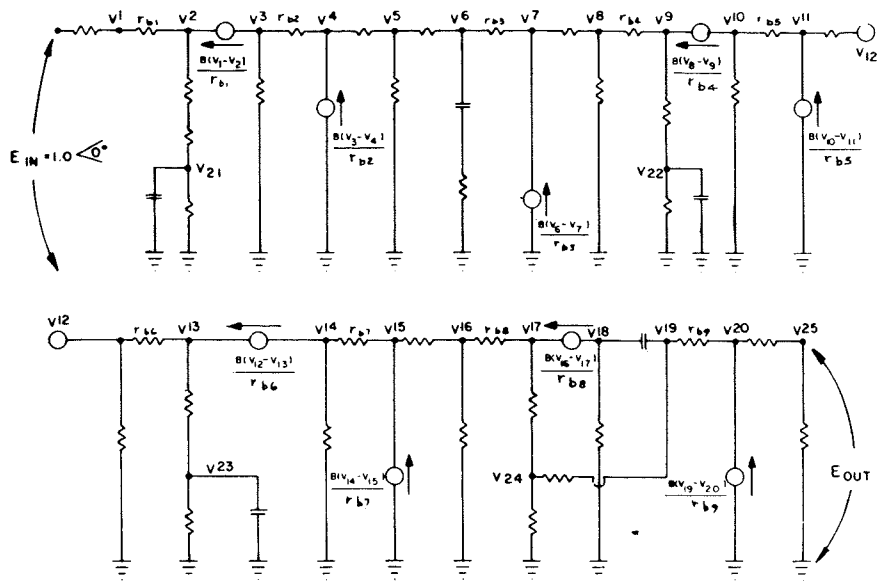

Fig. 3—Circuit submitted for computer analysis.

CIRCUIT COMPONENTS NODE$_1$ NODE$_2$	TYPE CODE	ARG1	ARG2	ARG3
$\mu(E_M)$	1	Re(μ) mhos	IM(μ)	M integer
R	2	R ohms	-	-
R C	3	R ohms	-	C microfarads
R L	4	R ohms	L henries	-
R L C	5	R ohms	L henries	C microfarads
R L C	6	R ohms	L henries	C microfarads

(E_M) - Current Generator
R - Resistance
C - Capacitance
L - Inductance

Fig. 4—Types of components isolated for computer analysis.

NODAL 1 BY R. HILTON, RCA ASTRO
HDRSS AMPLITUDE AND PHASE EQUALIZER, RUN A

FREQ(CPS)	AMPLITUDE	DB.	PHASE(DEG) AT NODE 25
1000.0	7.06080753	16.977	142.421
2000.0	4.92343903	13.845	122.050
4000.0	2.84547102	9.083	104.939
8000.0	1.54950267	3.804	92.692
10000.0	1.28751667	2.195	89.469
20000.0	0.82099032	-1.713	81.910
30000.0	0.74121902	-2.601	80.976
40000.0	0.76021158	-2.381	82.305
50000.0	0.82202096	-1.702	84.309
60000.0	0.90696714	-0.848	86.402
70000.0	1.00791329	0.068	88.373
80000.0	1.12156233	0.996	90.142
90000.0	1.24482004	1.902	91.674
100000.0	1.37690076	2.778	92.966
110000.0	1.51703748	3.620	94.063
120000.0	1.66423550	4.424	94.963
130000.0	1.81823510	5.193	95.689
140000.0	1.97877927	5.928	96.265
150000.0	2.14536631	6.630	96.693
160000.0	2.31712657	7.299	97.007
170000.0	2.49346232	7.936	97.193
180000.0	2.67453564	8.545	97.291

CONTINUE

Fig. 5—Nodal-analysis data produced by computer.

Percentage of heat transfer within the spacecraft by radiation as a function of the spacecraft geometry and absorptivity and emissivity; and

Temperatures of all unique thermal bodies as a function of design, flight, and mission characteristics. This is accomplished by either:

1) Numerical integration of a set of n differential equations, where n is the number of thermally unique nodes, or

2) An iterative matrix system to determine the average temperature.

While approach 1) produces a more detailed result, 2) is more efficient with less detailed results. The appropriate approach is selected on an individual basis, dependent upon specific design and mission requirements.

Much of the original work done on computation of spacecraft thermal behavior is given in an article published in an earlier issue of the RCA ENGINEER.[1]

Power supply simulation

In general, most power supply systems for unmanned spacecraft have consisted of a solar array, a battery system, and regulator circuits. Digital computer programs to support design and development of these systems include:

Simulation of array performance as a function of the solar-cell array design and flight parameters;

Array optimization programs, which essentially determine the optimum number of cells and the size and weight of the array as a function of the power requirements for the particular mission;

Determination of energy balance, whereby the electrical energy available throughout the life of the spacecraft is computed on an orbit basis and compared to the mission profile that determines the energy required; and

Determination of the degradation of the solar cells with time by processing in-flight telemetry data consisting of array output, array temperature, and attitude information. Comparison of this data with the theoretical model of the array determines the percent of degradation as a function of time.

Flight dynamics

Computer programs have been developed and are used extensively for computation of required mass of "yo-yo" type despin weights and evaluation of spin-up equations, as well as a full-scale simulation of flight dynamics. These programs facilitate determination of moments of inertia, momentum, and dynamic forces during such dy-

namic operations as release of the yo-yo weights, deployment of solar panels, and spinup of the momentum wheel.

Circuit analysis programs

Computer programs have been developed or acquired at AED to perform or support the following general application areas:

Nodal analysis
Worst-case analysis
Transient analysis
Filter and equalizer synthesis
Logic design.

The majority of these applications are of interest to many engineering-design specialist groups (e.g., tape recorders, communications, test equipment). Therefore, extensive efforts have been exercised to make these programs completely general, not only in terms of the mathematical models, but also in developing systems that are easily used by the average engineer with a minimum of special training.

For example, a nodal analysis was made of the complex amplitude and phase equalizer circuit shown in Fig. 3. The nodal analysis program has the capability of accepting six different types of components as shown in Fig. 4. The circuit was broken down into 19 nodes and tabulated on preprinted forms with the appropriate component parameters. This data, together with a list of desired frequencies, was the input to the program. The outputs for each frequency indicated amplitude, gain in *db*, and phase shift, tabulated as shown in Fig. 5.

Mechanical analysis

The mechanical forces acting on an equipment during launch must be determined to ensure successful operation. In addition, the results of such calculations can be applied to the design of the test fixtures used to verify the mechanical integrity of the equipment. Specific studies made in this area by digital computers include:

Static, dynamic, and inertia-balance calculations

Linear, multi-mass, spring calculations providing

1) Pilots of displacement, velocity, or acceleration of each inertial body versus forcing frequency;
2) Transmissibility of each interial body;
3) Spring forces versus exciting frequency for a two-mass system;
4) Multi-mass resonant frequencies;
5) Mode shape ratios.

Non-linear, single-mass, spring calculations providing the solution of the following differential equation:

$$M x + C x + K x^{3/2} = M W^2 A_0 \sin \omega t$$

where M is mass; C is the damping coefficient; K is the spring constant; ω is frequency; and A_0 is a constant.

Solutions have been obtained by numerical integration of this differential equation, and under certain input conditions, steady-state solutions have been found by finding the roots of a cubic polynominal.

In addition to the preceding, with the mobility analogy lumped parameter, mechanical systems can be analyzed by use of the nodal-circuit analysis program described above.

	TIROS	NIMBUS	L.O.	CLASSIFIED	RANGER, VOYAGER	RELAY, COMSAT	NAVIGATIONAL SATELLITE
FLIGHT DYNAMICS	*			*	*		
MISSION ANALYSIS AND SIMULATION	*			*	*		
ATTITUDE ANALYSIS	*	*		*		*	*
THERMAL ANALYSIS	*	*	*	*	*	*	*
POWER SUPPLY	*	*	*	*	*	*	*
ELECTRICAL ANALYSIS	*	*	*	*			*
MECHANICAL ANALYSIS	*			*			
TEST	*	*	*	*	*		*
ENGINEERING DOCUMENTATION	*	*	*	*	*	*	*

* INDICATES APPLICATION FOR PARTICULAR AREA

Fig. 6—Space of computer support for AED spacecraft projects.

Mission analysis and simulation

In addition to the previously described programs, which were used to support specific AED engineering activities (such as the attitude-control group, thermodynamics group, power-supply design group) other programs have been developed to predict certain performance characteristics in operational equipment. These programs include:

Contact-time program: This program computes the time in and out of contact with specific ground stations as a function of orbit parameter and the latitude, longitude, and minimum evaluation angle of the ground station.

Camera-coverage program: This program computes the area covered by a satellite-borne camera as a function of orbit and camera characteristics.

Low-altitude-interaction programs: These programs simulate the molecular interaction on a spacecraft in a low orbit.

Radiation program: This program computes the total radiation dosage received by a spacecraft as a function of flight parameters.

Scope of computer engineering support

Computer support has been given to every major spacecraft engineering project at AED since 1959. Many of the programs have been utilized for each project. The technical disciplines and projects involved are presented graphically in Fig. 6. As the space technology gains in sophistication, as engineers learn the advantages and even the necessity of computer assistance, and as computer systems with increased capabilities become available, it is inevitable that computers will play a proportionately greater role in AED's performance on space system projects.

Reference

1. Goerss, R. H., "Computer Analysis of Satellite Thermal Behavior," RCA ENGINEER, Vol. 11, No. 3 (Oct-Nov 1965).

Engineering school to industry

B. A. Bendel

No, the "Trials and Tribulations of a Graduate Engineer" is not a daytime TV soap opera. It is, instead, a very real drama faced by most engineering school graduates as they become integrated into the environment of the engineering industry.

Barry Bendel
Aerospace Systems Division
Burlington, Mass.
received the BEE in June of 1965, and the MEE in February 1966, both from Cornell University. Since joining RCA, he has been associated with the DIMATE program and has had responsibility for upgrading the capabilities of that system's computer/controller and peripheral devices. In addition, he has been working on an IR&D program aimed at hybridizing a portion of the DIMATE Frequency Synthesizers. Mr. Bendel is a member of Eta Kappa Nu, Phi Kappa Pi, Pi Delta Epsilon, and the IEEE.

RECENTLY, I WAS ABLE to sit down with a good friend who was due to graduate from school in June, and talk about the transition from the relatively sheltered atmosphere of the academic world, to that of his chosen profession. Since he had had no pregraduate job experience, he was understandably concerned about what to expect when the time came to leave school and go to work. And as we talked, I began to recall some of the experiences which had marked my own emergence into the post-school engineering community.

There were, I remembered, two areas in which I had to acclimate myself: one expected, and one, for the most part, totally unforeseen. The first area encompassed the so-called "scientific" aspects of engineering, and dealt with my ability, as a new engineer, to handle the technical workload given to me. For better or worse, my school experience had been heavily weighted in the theory of electrical engineering, as opposed to the practical aspects. It seemed as though the lab instructor always had his multistage transistor whazzis built and working before I had a chance to apply the first of many design equations presented in that morning's lecture hall. Thus I was more than a little leary about how I would hold up under my first assignment. But I was in for a surprise.

If I were at all naive about the "breaking-in" of new engineers, the company certainly was not. Managers would be very pleasantly surprised if an engineer fresh out of school could immediately tackle the most complex design tasks. They do not expect it, however, and such jobs are, therefore, rarely delegated. My first job, while challenging, was not totally overwhelming. Of course, I made my blunders—most new engineers seem to, at one time or another—but I learned from them, which was the next best thing.

An added help, and a welcome change from the school environment, was the spirit of cooperation, rather than competition, which exists within a design team as it strives to meet a project goal. A further aid was the practice of making design assignments through an intermediary—a senior engineer, who, while keeping mostly in the background, would be available for technical advice and guidance when necessary.

As time went on, and with several designs under my belt, I discovered what was behind that lab instructor's incredible performances. It was experience, and no better teacher exists who can increase a new engineer's confidence in his own ability. A few jobs well done can make all the difference in the world, and to my surprise, it wasn't too long before I could throw a whazzis together also!

But although my technical schooling had been thorough, at least in theory, two fundamental concepts had been largely ignored: reliability and environment. The designs built in the relatively stable atmosphere of the lab in school had to work just long enough for the professor to walk ceremoniously past my bench. In industry, however, hardware might have to last for years in all types of environments. My first circuits worked perfectly at room temperature, but operated marginally, or even failed miserably at +125°C. Design reviews, more harrowing than a fraternity initiation, added such words as "worst-case analysis" and "end-of-life tolerance" to my vocabulary.

The second area of adjustment I had to face was one for which I had little if any preparation. At school, engineering was strictly a science. You learned the fundamentals, and how to apply them to achieve results that were correct from a theoretical and scientific standpoint. But in industry, engineering is also a business, and every decision made must be based on a number of business, as well as scientific criteria.

Economics is perhaps the single most important non-technical consideration for a new engineer. A "dollar sign in the denominator" would be a good expression to live by. Oftentimes, as I've found, the design I'd like to use is really clever, right at the forefront of the state-of-the-art, exceeds all the specifications, and costs a small for-

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tune. Another design, though perhaps not as clever, maybe not using those new hundred-dollar components, but still meeting all the "specs", would be the way to go. One of the first words I learned when I left school was "trade-offs". Essentially, it is a give and take proposition; you give a little here to gain somewhere else. In the above case, I had to give a little in sophistication and performance to substantially reduce the cost of the circuit.

But cost, or economics in general, can enter the picture in more subtle ways.

For example, I once developed a design for a piece of digital equipment that was minimum in size, and made use of the latest MSI circuits. To achieve this reduction in size, however, I had used one integrated circuit from vendor A, another from vendor B, and others from vendors C and D. As I discovered, though, this approach violated the principles of engineering economics in several ways. First, by using different IC's from several vendors, I had greatly complicated the task of providing spares with the equipment, as called for in the contract. Had I used only one or two types, the spares package would have been correspondingly smaller and cheaper. In addition, the delivery time on vendor C's circuits were unusually long, which would have caused a significant delay in the overall schedule. Finally, as is often the case, each time a new integrated circuit is used for the first time in the plant, a set of drawings and specifications must be generated, and these cost money. Many times this cost can be eliminated by using older IC's for which documentation already exists.

From this example, it may be difficult to see how anything new ever gets built in the industry, but again "trade-offs" provide the key. In another case, size, weight, or technical performance might have outweighted the additional cost of the above approach. Many times, however, a new engineer must learn to put up with the frustration of doing something "rough and dirty" or "the old way", because it is still the cheapest way to get the job done.

In addition to economics, the graduate engineer must familiarize himself with the "politics" of engineering, both within the plant, and on the outside. The realization that out-of-plant occurrences could influence my work came the first time I participated in a proposal effort. Here, designs had to be based on a number of factors, many of which were neither scientific nor economic. They dealt with the answers to such questions as: What does the customer really want? What can he afford? What about the competition? Though not primarily concerned with how these answers were obtained, I found that it was necessary to modify or change my own ideas, depending on what they actually were. For example, one potential customer wanted an automatic test system, but, having only a slight exposure to the field, he was leary of a highly sophisticated design. Knowing this, my design was purposely made simple and straightforward. A customer more intimately familiar with the product line and its applications, however, might have caused me to try a different approach.

"In-plant politics" is perhaps a poor choice of words, as it conjures up Machiavellian images of double-crosses and double-double-crosses. Although things of this sort do exist, they are, for the most part, isolated cases, and the neophyte engineer would do well to steer clear of them. Dealing with people would be a better way of expressing it. Hopefully, the first job given to a new engineer will teach him that the company is comprised of more than just engineering labs. In school, once your design had been breadboarded and tested, you were all finished, but in industry, this would only be the first step. Since the final product is a salable item, and since the design engineer is, presumably, the most knowledgeable about his own circuits, the chances are that his responsibility for them will continue right along. My first circuit, which was put on a printed circuit board, had to be followed through Drafting, Manufacturing, and Quality Control. It was, therefore, an excellent way to learn about the rest of the plant, and meet people with whom I would be dealing on subsequent jobs. Knowing where to go, and who to see, to help get a job done can save hours, days, or even weeks of work. Even so simple a procedure as ordering components for a circuit can be an exercise in interpersonal relationships. Back in school, when I needed a particular component for my circuit, I had to travel no further than the parts bin or "junk pile."

To do the same thing in industry required a good deal more mileage. First, I had to speak with the vendors to determine which component best fit my requirements. I also had to check with our own Standards people concerning the acceptibility of the component I finally selected. If I won that battle, I could then submit a Purchase Requisition, via our Engineering Project Assistant, to the Purchasing Department. After much nailbiting and many phone calls to the Purchasing Agent, the component finally arrived and was delivered to . . . Purchased Material Inspection, for a check against the specifications. If some question arose, I had to settle it, if I ever wanted to use that part in my design. Thus, as such episodes were to teach me, dealing with people, the technician who builds your circuits, the engineer whose test equipment you borrow, and all the rest, is a major part of the engineering business.

Finally, though an engineer leaves school to go to work, the educational process is far from complete, nor can it ever really be so. As the state-of-the-art advances, engineers both new and old must keep abreast, or face technical obsolescence. Informal education, through the medium of technical journals and trade magazines, is one important way to keep informed of new developments. The company will do its part, via seminars, technical conferences and shows, and even in-plant courses. But it is up to the individual engineer to take advantage of these opportunities, even though, for the recent graduate, more schooling may be the last thing he may want.

Trials and tribulations? Well, mine were about average, I guess, and they couldn't have been too bad, as I managed to survive relatively unscathed. And I didn't frighten off my friend, either, but I did alert him to several things which, like myself, he had not really thought about. As for the self-confidence—that would come in time. Trials and tribulations? Sure, but after all, as I told him, school was no picnic either, and he made it.

Random House

E. Darhansoff

Elizabeth Darhansoff
Publicity Associate
Random House, Inc.
New York, N.Y.
received the BA from Hofstra University in 1963. During the following year she founded an art gallery in Westchester County. For two years, Mrs. Darhansoff was assistant to the publicity director of Atheneum Publishers. In the summer of 1966, Mrs. Darhansoff joined Random House as a Publicity Associate.

RANDOM HOUSE, acquired by RCA in 1966, has had many literary plums to its credit during its 43 year history. The latest of its accomplishments came in May when William Styron's *The Confessions of Nat Turner,* a Random House best seller, received the Pulitzer Price for Literature.

Now one of the top publishing firms in the country, Random House was founded in 1925 by two young Columbia University graduates. Bennett Cerf left Wall Street and Donald Klopfer left the diamond business, joined financial forces, and bought out the Modern Library series.

From that modest beginning, Random House has become one of America's largest and most distinguished publishing houses. It is known throughout the world for the eminence of the authors it attracts and the quality and variety of its publishing.

Had personal touch

Imagination and industry have played a large part in its growth, of course, but an even larger measure of its success has often been attributed to what may be called the personal touch. As large as the company has become, the spirit of personal interest and enthusiasm which gave the company life at the beginning is still the guiding force behind the company's policy.

Although the company was founded in 1925, it did not acquire its present name until almost two years later. By that time, the Modern Library was beginning to thrive, and Mr. Cerf and Mr. Klopfer decided to expand, publishing books chosen "at random." Out of that phrase came the name Random House.

In 1933 Random House became the publishing leader in fighting censorship in America. *Ulysses* by James Joyce was attacked in court by the U.S. Government for obscenity. On the basis that the book had to be judged as a whole and not on a few choice sentences, the plea that *Ulysses* was not obscene was sustained by Judge Woolsey on December 6.

In the early thirties the young publishing house acquired two of the greatest of American authors, Eugene O'Neill and William Faulkner. After that, the company's progress was rapid indeed. The Random House list today includes, along with O'Neill and Faulkner, some of the most distinguished names in American literature: John O'Hara, James A. Michener, Truman Capote, Robert Penn Warren, Philip Roth, William Styron, Herbert Gold, John Knowles, Ira Levin, Jerome Weidman and many others.

Public Company in 1959

In October 1959, Random House—until then a partnership—became a public company, selling some 220,000 shares of stock to the public. The company set out on a program of expansion. In the spring of 1960, Random House acquired the distinguished publishing house of Alfred A. Knopf, Inc. Knopf books are noted for beautiful typography and carry some of the world's leading literary names: Thomas Mann, Andre Gide, Franz Kafka, Jean Paul Sartre, Willa Cather, H. L. Mencken, Kahlil Gibran, John Hersey, Albert Camus, Dashiell Hammett, John Updike and many, many others. The distinguished Knopf list of food and wine books boasts titles by such notables as Julia Child and Alexis Lichine. Knopf's Vintage paperback series and the Modern Library paperbacks of Random House were combined under the Vintage imprint. Also in 1960, Pantheon Books, whose list includes such distinguished authors as Boris Pasternack, Zoe Oldenbourg, Gunnar Myrdahl, and Mary Renault, joined the Random House organization.

Children's books

Bennett Cerf calls the Random House line of children's books "our pride and joy." The company not only published the works of Dr. Seuss and Walter Farley, two of the most successful juvenile authors of all time—but also inaugurated two series which have had extraordinary sales to young readers, and to schools and libraries: Landmark Books (on American and World history) and Allabout Books (on science).

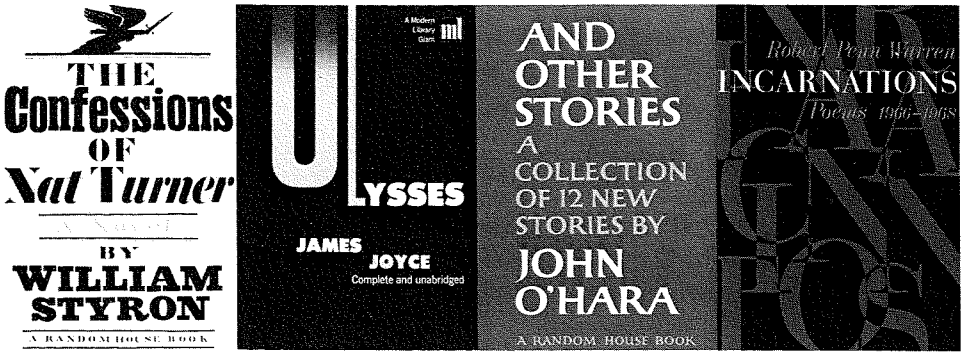
And another step in the Random House expansion plan, the acquisition of Beginner Books in 1960, brought another series to the House. The series, intended for children just learning to read, was created by Dr. Seuss, who wrote the first book in the series, *The Cat in the Hat.*

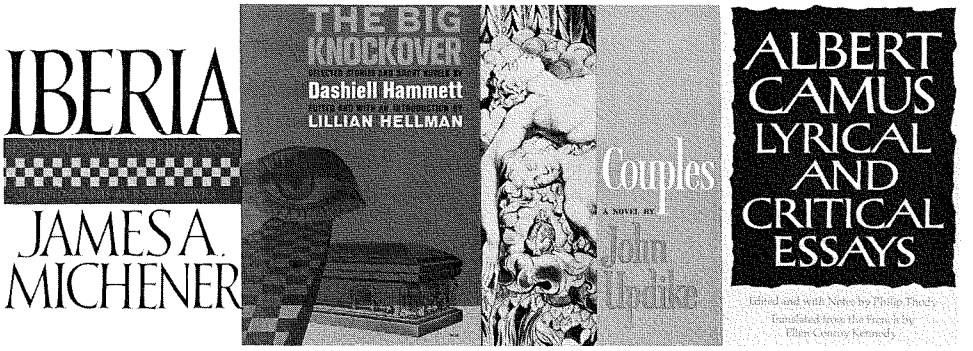
Step-Up Books, a series for more advanced young readers, has also enjoyed a solid success since its creation by Phyllis Cerf in 1965. New series launched in 1967 included: new Doctor Dolittle books; Pop-Up books; magic motion books, and a Living History Library.

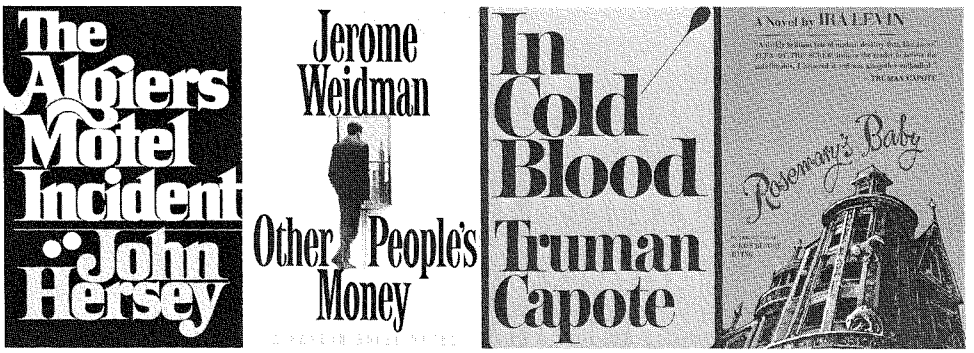
According to Robert L. Bernstein, who was appointed President of Random House in 1966 when Bennett Cerf became Chairman of the Board and Donald Klopfer Vice Chairman: "Book publishing is really more than one business. While the product consists of paper and cloth, the similarity between trade business and text business almost stops there."

Education

The education division is now divided into three separate businesses. The L. W. Singer Company, publisher of elementary and high school textbooks, was acquired in 1960. The Random







House School and Library Service, which sells supplementary materials to elementary and high schools, started in 1962. The Random House—Knopf College and Reference Department is the third sub-division.

Importance to RCA

"It is my belief," says Mr. Bernstein, "that the Random House educational division is as important to RCA as to Random House itself. As I see it, it represents RCA's most solid and continual entry into the school systems of our nation.

"You will see text book companies becoming educational companies selling packages that include books, tapes, slides and computer-assisted learning programs and so forth. Random House's educational divisions should be a very important part of the whole RCA move into education," he continued.

Mr. Bernstein feels that the company's biggest gamble is in the high school and elementary textbook field. "While education is changing, schools still use the same English, reading, social studies, and science programs. The risks are large because it can cost close to one-half million dollars and five years to prepare one series and you then must dislodge something already in the schools."

L. W. Singer Company

For this reason as well as for its overall importance to the RCA education program, the L. W. Singer Company is undergoing a build-up in the text book field.

School and Library Series

The second Random House Company in the education business is the Random House School and Library Service, Inc. Schools need more than just textbooks in the classroom for motivating students. Along with the supplementary books the division is selling tapes and players and ear phones.

College and Reference Department

The third educational division is the Random House College and Reference Department which published the unabridged Random House Dictionary of the English Language. With 2096 pages and more than 260,000 entries, it includes four foreign-language dictionaries, an atlas, a gazeteer and other dividends. This year saw the publication of the college edition of this dictionary.

The Reference Department is also working on an elementary school dictionary and foreign dictionaries. The College Department does about six million in college texts and another four million in Modern Library and Vintage books.

Future of the educational field

Mr. Bernstein is optimistic about the future of the educational field: "It is our hope in the next five years to come reasonably close to doubling the company's volume and at that time to have our educational business become two-thirds of our total volume."

Random House is also expanding physically. In 1966 a Distribution Center in Westminster, Maryland was set up to receive books in large block shipments from binderies throughout the country and fill orders received from all parts of the world. There will be approximately 600 employees at Westminister by the end of the year.

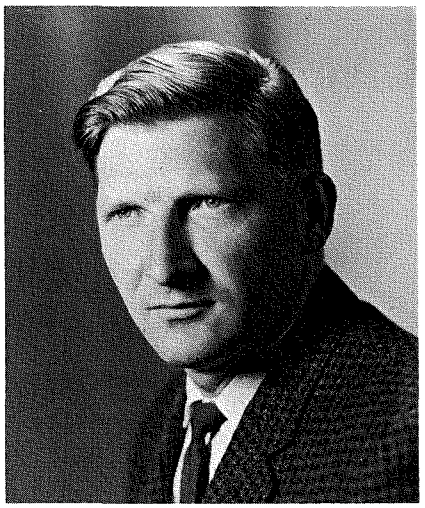
In January, 1969, the new Random House at 50th St. and Third Ave. in New York was completed, bringing together more than 800 New York employees from their six previous locations into 14 floors of the new building.

Describing Random House's goals, Mr. Bernstein said, "We have just ended an era as a small publisher and are trying to get a new medium-sized business to move into big business. We are trying to become educational publishers ourselves and at the same time fit our plans into RCA's overall education plans. "We are trying to grow as trade publishers . . . the three trade houses are planning new growth in both the adult and children's part of the business. In this projected growth administration, financial planning, and systems are important to us as never before."

Surface-state density from high frequency capacitance measurements

Dr. K. H. Zaininger

This paper recapitulates the theory of the MIS capacitance method for determining semiconductor surface properties, briefly mentions the limitations of this method, and gives a computer program that greatly facilitates the necessary computations.



Dr. Karl H. Zaininger, Head
Solid-State Devices Technology
Laboratories
Princeton, N.J.
received the BEE (magna cum laude) from City College of New York in 1959; the MSE in 1961, the MA in 1962, and the PhD in Engineering Physics in 1964 from Princeton University. In 1959 Dr. Zaininger joined the staff of RCA Laboratories. He has been working in research on various semiconductor devices, and has been involved in research on silicon based MOS devices since their original inception. This research included basic studies in semiconductor surface physics. He is presently concerned with MIS device physics and technology, with measurement techniques, and with the physics of radiation damage in MIS systems. In August 1968 Dr. Zaininger was appointed to his present position. In 1965 Dr. Zaininger received an RCA Laboratories Achievement Award for team performance for experiments and studies leading to a better understanding of the electrical properties and growth mechanisms of silicon-dioxide films on silicon substrates. In 1968 he received another Achievement Award for team performance in research on aluminum oxide films on TFT and MOS structures leading to stable and radiation-resistant devices. Dr. Zaininger is a Senior Member of the Institute of Electrical and Electronics Engineers, and a member of Tau Beta Pi, Eta Kappa Nu, Sigma Xi, and the Shevchenko Scientific Society. He is also a co-author of a textbook on field effect transistors.

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AN MIS CAPACITOR can be defined as a structure consisting of an N- or P-type semiconductor, covered by a thin film of insulating material (often oxide) with a metal electrode[1] on top of the insulator and an ohmic contact to the semiconductor. Such devices can be an important research tool because their capacitance versus bias (C-V) characteristics contain information about the surface states[2] present in this system.[3] Because of the ease of fabrication, simplicity of structure, and the sensitivity of the C-V characteristics to physical properties, MIS capacitors can be used as a test vehicle to study the influence of process parameters on properties of insulating films on semiconductors, and insulator-semiconductor interfaces.

The small signal, differential admittance of an ideal MIS capacitor (i.e., one with an ideal insulating film and no surface states) consists of the insulator capacitance, C_i,[4] in series with the surface space charge layer capacitance, C_{sc}.[5] For P-type material,

$$C_{sc} = \pm \left(\frac{\varepsilon_s}{\lambda_p}\right) \frac{1 - e^{-\alpha} + \frac{n_o}{N_A}(e^{\alpha} - 1)}{\left[e^{-\alpha} + \alpha - 1 + \frac{n_o}{N_A}(e^{\alpha} - \alpha - 1)\right]^{1/2}} \qquad (1)$$

where $\alpha = q\psi/kT$.

The + sign is used when the surface potential, ψ_s, is positive and the − sign when it is negative. Here, ε_s is the semiconductor dielectric constant k is Boltzmann's constant, T is temperature, and q is the electronic charge. The Debye length, λ_p, is defined by

$$\lambda_p^2 = 2(kT/q)\,\varepsilon_s/N_A q$$

where N_A is the acceptor concentration. The minority carrier concentration is given by

$$n_o = N_c \exp(-E_c E_F/kT)$$

where E_c and E_F are the position of conduction band and Fermi level, respectively. C_i is independent of frequency and so is C_{sc} in the accumulation and depletion regimes (up to 10^{11} Hz). In the inversion regime, however, C_{sc} takes on different forms depending on whether or not the minority carriers can follow the applied AC signal and/or bias. The dependence of this ideal MIS capacitance on effective bias is shown in Fig. 1 for a Me-SiO_2-Si structure. In all cases, this capacitance is uniquely determined by the semiconductor surface potential, ψ_s. For an actual MIS capacitor in which surface states are present, but in which loss mechanisms are neglected, the equivalent circuit is modified by adding the surface state capacitance, C_{ss}, in parallel with C_{sc}. The dependence of C_{ss} on frequency and surface potential is a function of the density of surface states and their spatial and energy distribution. Since this is, in general, not known, little information about the physical properties of the interface can be obtained from an analysis of the MIS C-V characteristics obtained at an arbitrary frequency. However, if the measurement frequency is sufficiently high so that surface states cannot follow ($f \geq 1$ MHz), then the surface state capacitance becomes zero and the MIS capacitance reduces to its high frequency form, i.e. the series combination of C_i and C_{sc}. When this condition is satisfied, then the MIS capacitance is unambiguously related to the semiconductor surface potential. However, there is a difference between an experimentally determined high-frequency C-V characteristic and one computed for an identical structure without surface states, and that is the voltage due to the total charge in surface states. By finding the difference between the

measured voltage for a given capacitance (and thereby ψ_s) and its "ideal" value, $\triangle V$, one can determine the total charge that can be trapped in surface states during the measurement period and the surface state density as a function of ψ_s (or energy). The effective density of surface states, as reflected to the insulator-semiconductor interface, N_{ss}, is then given for any particular value of capacitance (and thereby ψ_s) as

$$N_{ss} = C_i \triangle V / 1.6\text{x}10^{-19} = (\varepsilon_i \triangle V) / (1.6\text{x}10^{-19} d_i) \quad (4)$$

where ε_i and d_i are the insulator dielectric constant and thickness, respectively. If the experimental curve is to the left of the ideal one, the charge in surface states is positive; if it is to the right, the charge is negative. A typical example of a comparison between experimental and ideal curves is shown in Fig. 2.

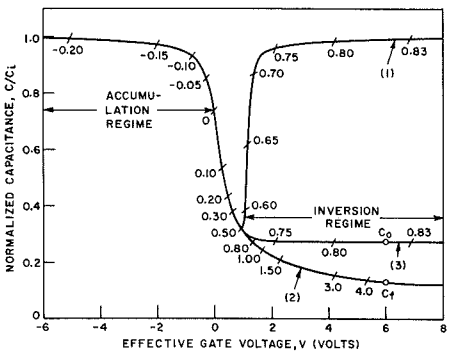

Fig. 1—Normalized MIS capacitance versus gate voltage for the case of no surface states. In the inversion regime, curve 1) holds if the minority carriers follow both AC and DC signal; curve 2) if they cannot accumulate at the surface (Schottky depletion layer capacitance); curve 3) if they follow DC but not AC signal. The value of the silicon surface potential is shown for several values of capacitance.

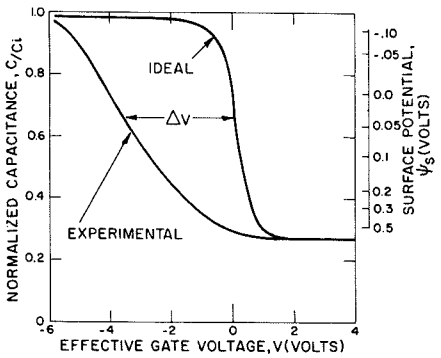

Fig. 2—Comparison between experimental and ideal C-V curves for the structure described in Fig. 1.

Limitations

In the past, the use of the MIS capacitance method in the study of surface properties has involved various approximations and assumptions that are not always justified. However, MIS capacitance measurements can yield interesting and meaningful results if the proper experimental conditions are established, and if care is taken in the interpretation of the experimental results. The major error considerations are summarized below.

This method essentially determines only the semiconductor surface potential, and, thereby, the charge in the semiconductor space charge region, Q_{sc}, as a function of the applied bias. Because of charge neutrality

$$Q_{sc} + Q_{Me} + \Sigma_i Q_i = 0 \quad (5)$$

where $\Sigma_i Q_i$ is the sum of all the charges outside the semiconductor, except Q_{Me} which is the charge on the metal electrode due to the applied bias. The separation of $\Sigma_i Q_i$ into its individual components (including their polarity) is difficult on the basis of high-frequency MIS capacitance measurements alone. From this point of view, one should simply speak of an "effective compensating charge." Because of the widespread use of the term "surface states" we have also retained this expression despite the conceptual difficulties connected with it. However, we use it here in a completely operative manner.[2]

A rather severe limitation arises from the series combination of C_i and C_{sc}. The insulator capacitance acts as a "window" that permits only a partial examination of the semiconductor capacitance. When C_{sc} is much larger than C_i (e.g., $C_s/C_i > 10$), one can no longer measure C_{sc}. This limits the region of the forbidden gap which can be examined. This can be made some-

```
 10 REAL CP(100),BIAS(100),V(400),P(400),C(400)
 20 READ 100,CMAX,AREA,DA,T,REOX,M,K
 30 100 FORMAT(F10.0,2E10.0,2F10.0,2I10)
 40 READ 101,(CP(J),BIAS(J), J=1,M)
 50 101 FORMAT (2F10.0)
 60 GO TO (10,11)K
 70 10 ES = 12.*8.85E-14
 80 EG = 1.11
 90 ENV=2.5*0.43E19
100 ENC=2.5*1.15E19
110 GO TO 12
120 11 ES=11.6*8.85E-14
130 EG=1.435
140 ENV=1.65E13*(294.0**1.5)
150 ENC=9.25E13*(294.0**1.5)
160 12 EOX=REOX*8.85E-14
170 DELEV=0.026*LOG(ENV/DA)
180 DEB=SQRT(0.052*ES/(DA*1.6E-19))
190 XMAX=SQRT(2.*ES/1.6E-19/DA*(EG-2.*DELEV))
200 CSMIN=ES/XMAX
210 IF(CMAX>1.0) GO TO 14
220 13 COX=1.0E8*EOX/T
230 S=0.0
240 CREOX=0.0
250 GO TO 15
260 14 COX=1.0E-12*CMAX/AREA
270 S=1.0E8*EOX/COX
280 CREOX=COX*T/8.85E-6
290 15 CMINH=1./(1.+COX/CSMIN)
300 A=(EG-DELEV)/0.026
310 B=LOG(ENC)-A
320 DAA=LOG(DA)
330 CC=ES/DEB/COX
340 L=100.*DELEV
350 N=100.*EG
360 DO 20 J=1,N,1
370 AJ=J-L-1
380 PSI=0.01*AJ
390 IF(PSI=0.0) GO TO 181
400 UPSI=PSI/0.026
410 TROUB1=B-DAA+LOG(EXP(UPSI)-1.-UPSI)
420 IF(TROUB1+114.) 113,113,114
430 113 TROUB1=-114.
440 114 TROUB2=B-DAA+LOG(ABS(EXP(UPSI)-1.))
450 IF(TROUB2+114.) 115,115,16
460 115 TROUB2=-114.
470 16 CONTINUE
480 BRAC=SQRT(UPSI-1.+EXP(-UPSI)+EXP(TROUB1))
490 IF(PSI>0.0) GO TO 18
500 17 VOLT=0.026*(UPSI-2.*CC*BRAC)
510 CAP=1./(1.+BRAC/CC/(EXP(-UPSI)-1.-EXP(TROUB2)))
520 GO TO 19
530 18 VOLT=0.026*(UPSI+2.*CC*BRAC)
540 CAP=1./(1.+BRAC/CC/(1.-EXP(-UPSI)+EXP(TROUB2)))
550 GO TO 19
560 181 CONTINUE
570 TROUB0=B-DAA
580 IF(TROUB0>-114.0) GO TO 183
590 TROUB0=-114.0
600 GO TO 183
610 183 CSFB=2.0*(ES/DEB)*SQRT(0.5*(1.+EXP(TROUB0)))
620 CAP=1./(1.+COX/CSFB)
630 VOLT=0.0
640 19 V(J)=VOLT
650 P(J)=PSI
660 C(J)=CAP
670 20 CONTINUE
680 V(J)=0.0
690 P(J)=0.0
700 C(J)=0.0
710 SMALL=C(1)
720 JJ=2
730 71 IF(SMALL-C(JJ)) 73,73,72
740 72 SMALL=C(JJ)
750 JJ=JJ+1
760 GO TO 71
770 73 JJMIN=JJ
780 CMIN=C(JJ)
790 GO TO (74,75)K
800 74 PRINT 102
810 102 FORMAT('1SEMICONDUCTOR                    = SILICON')
820 GO TO 76
830 75 PRINT 103
840 103 FORMAT('1SEMICONDUCTOR                    = GALLIUM ARSENIDE
850 76 PRINT 104,DA
860 PRINT 105,DELEV
870 PRINT 106,DEB
880 PRINT 107,REOX
890 PRINT 108,CREOX
900 PRINT 109,T
910 PRINT 110,S
920 PRINT 111,COX
930 PRINT 112,CMIN
940 PRINT 149,CMINH
950 PRINT 150
960 DO 52 J=1,M,1
970 IF(CP(J)) 35,33,33
980 33 CPN=CP(J)/CMAX
990 II=1
1000 30 IF(C(II)-CPN)31,31,32
1010 32 II=II+1
1020 GO TO 30
1030 35 CPN=-CP(J)/CMAX
1040 II=JJMIN+1
1050 50 IF(C(II)-CPN)51,31,31
1060 51 II=II+1
1070 GO TO 50
1080 31 VS=BIAS(J)-V(II)
1090 DS=-(COX*VS)/1.6E-19
1100 ENERGY=DELEV+P(II)
1110 PRINT 125,BIAS(J),CP(J),CPN,P(II),DS,ENERGY
1120 125 FORMAT(2F10.3,2F10.3,1PE10.2,0PF10.2)
1130 52 CONTINUE
1140 104 FORMAT(' ACCEPTOR CONCENTRATION          ='1PE10.1'  PER
     CC')
1150 105 FORMAT(' FERMI LEVEL(ABOVE VALENCE BAND) ='0PF10.3'  EV')
1160 106 FORMAT(' DEBYE LENGTH                    ='1PE10.2'  CM')
1170 107 FORMAT(' RELATIVE DIELECTRIC CONSTANT    ='F10.3)
1180 108 FORMAT(' CALCULATED DIELECTRIC CONSTANT  ='F10.3)
1190 109 FORMAT(' OXIDE THICKNESS                 ='F10.1'
     ANGSTROM')
1200 110 FORMAT(' CALCULATED OXIDE THICKNESS      ='F10.1'
     ANGSTROM')
1210 111 FORMAT(' OXIDE CAPACITANCE               ='E10.3'  FDCM-2'
1220 112 FORMAT(' NORMALIZED LF MIN  CAPACITANCE  ='F10.3)
1230  149 FORMAT(' NORMALIZED HF MIN  CAPACITANCE  ='F10.3)
1240 150 FORMAT('0      BIAS      CAP      NCAP      PSI    STATES
     ENERGY')
1250 255 FORMAT(I5,3F8.3)
```

Fig. 3—Computer programs for comparing an experimental C-V curve for a P-type substrate with an ideal curve for an identical structure without surface states.

```
CMAX=1.0
AREA=0.0
DA=1.4E15
T=950.0
REOX=3.82
M=6
K=1
CP(1)=0.94
BIAS(1)=-1.50
CP(2)=0.87
BIAS(2)=-1.00
CP(3)=0.79
BIAS(3)=-0.60
CP(4)=0.72
BIAS(4)=-0.50
CP(5)=0.58
BIAS(5)=-0.40
CP(6)=0.47
BIAS(6)=0.00
```

Fig. 4—Method of characterizing the system being examined.

```
SEMICONDUCTOR                          = SILICON
ACCEPTOR CONCENTRATION                 =   1.4E+15   PER CC
FERMI LEVEL(ABOVE VALENCE BAND)        =     0.233   EV
DEBYE LENGTH                           =  1.57E-05   CM
RELATIVE DIELECTRIC CONSTANT           =     3.820
CALCULATED DIELECTRIC CONSTANT         =     0.000
OXIDE THICKNESS                        =     950.0   ANGSTROM
CALCULATED OXIDE THICKNESS             =       0.0   ANGSTROM
OXIDE CAPACITANCE                      =  .356E-07   FDCM-2
NORMALIZED LF MIN  CAPACITANCE         =     0.309
NORMALIZED HF MIN  CAPACITANCE         =     0.276

    BIAS      CAP      NCAP       PSI     STATES      ENERGY
  -1.500    0.940    0.940    -0.100   1.69E+11        0.13
  -1.000    0.870    0.870    -0.060   1.52E+11        0.17
  -0.600    0.790    0.790    -0.020   1.15E+11        0.21
  -0.500    0.720    0.720     0.010   1.19E+11        0.24
  -0.400    0.580    0.580     0.070   1.34E+11        0.30
   0.000    0.470    0.470     0.150   8.14E+10        0.38
1260
```

Fig. 5—Typical printout of pertinant surface-state density information.

what more plausible from physical reasoning by realizing that we are actually attempting to solve for the value of one of two capacitors in a series-connection from the values of C_i and the equivalent capacitance of the series combination, C. Consequently, as C approaches C_i, this calculation will depend very strongly on the accuracy with which C_i and C can be measured. It can be shown that for $C/C_i > 0.9$ the errors in N_{ss} become excessive.

The dependence of the inversion-layer capacitance on bias and frequency is also quite complex because of the several processes by which minority carriers may be transferred into and out of the inversion layer. It cannot simply be concluded that experimentally observed deviations of the MIS capacitance in the inversion regime from its ideal shape are due to the effect of surface states. In many cases, the type of curve represented by (3) in Fig. 1 is obtained. In that case, only about half the forbidden gap can be investigated because the comparison has to be discontinued when c gets close to the flat portion due to excessive errors.

Two dimensional effects, such as nonuniform spatial distribution of surface states (patchiness), may introduce an additional ambiguity. This effect can be described in terms of patchiness where a patch is a region for which the spatial distribution of surface states is uniform. The influence of patchiness depends on the ratio of patch-to-electrode area and has to be evaluated with regard to the pertinent experimental conditions.

Computer program

As presented in the above discussion of the determination of the surface state density versus surface potential, a comparison has to be made between an experimental C-V curve and an ideal one computed for an identical structure without surface states. Since this is cumbersome and time consuming, a computer program has been developed which can be used on the RCA basic time-sharing system, and which carries out this procedure. The program for a P-type substrate is shown in Fig. 3. That for an N-type substrate is analogous.

After the program has been initiated[6,7] the computer will ask for the parameters that characterize the system under examination. This is shown in Fig. 4. The items required are the maximum capacitance (CMAX) in pF, the gate area (AREA) in cm^2, the acceptor concentration (DA) per cm^3 as determined from the minimum to maximum capacitance ratio of the pertinent experimental curve[8], the measured insulator thickness (T) in Angstroms, the number of data points (M), and a parameter (K) which is 1 if the substrate is silicon and 2 if it is gallium arsenide. If the maximum capacitance and area are given, the measured insulator thickness is not necessary. If it still is given, the computer will use it to calculate a relative dielectric constant for the insulator. It will also use the insulator capacitance and the given dielectric constant to compute a thickness from that data. If only normalized capacitance is measured, then area need not be given, but measured insulator thickness is required. Maximum capacitance is then unity and the computer will use the given dielectric constant for the insulator for calculations. The subsequent data to be given is capacitance in pF (or normalized capacitance) and the corresponding bias in volts. For capacitances in the inversion regime, the capacitance values must be preceded by a minus sign.

After the last data point has been supplied, the computer carries out the computation. A typical output is shown in Fig. 5. First some pertinent parameters are printed out. Both the low and high-frequency minimum capacitances are also given so that a comparison can be made with the actual curve to determine if the proper acceptor concentration has been used. This is followed by columns of bias (BIAS) in volts, capacitance (CAP) in pF or normalized, normalized capacitance (NCAP), surface potential (PSI) in volts, surface state density (STATES) per cm^2, and energy above the valence band (ENERGY) in electron volts.

This program compares an experimental curve with a theoretical one which is calculated under the assumption that the minority carriers do follow both AC and DC signals. This is justified even if they only follow the DC signal since in that case one cannot use the points close to the flat portion of the curve because of error considerations.[9]

References

1. The metal electrode is often referred to as the gate to conform with MIS transistor terminology.
2. The term *surface states* is used here in a completely operative manner; it lumps together the effect of work function difference, oxide charge, and *interface states*.
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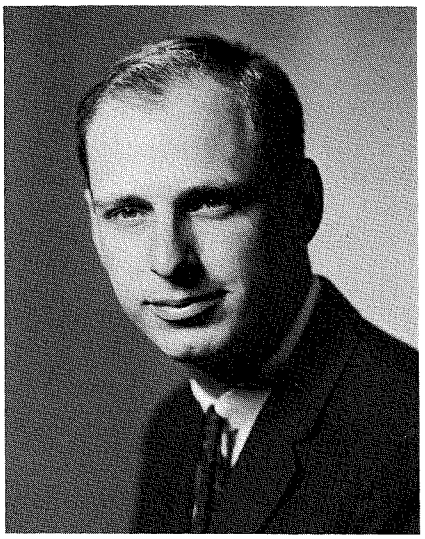
9. Zaininger, K. H., and Warfield, G., "Limitations of the MOS Capacitance Method for the Determination of Semiconductor Surface Properties," *IEEE Trans. Electron Devices* ED-12, (1965) p. 179.

Methods of programming for numerically controlled production

Dr. R. L. Rosenfeld

Numerically controlled (N/C) machines are a form of manufacturing equipment controlled electronically by a special purpose computer. Although these machines are automatic, the automation takes a programmable or flexible form. This paper surveys the problems of programming for numerically controlled machines. It compares the many methods presently used and emphasizes the requirements of electronic equipment manufacturing.



Dr. R. L. Rosenfeld
Process Research and Development Laboratory
Laboratories
Princeton, N.J.

received the BS degree in mechanical engineering from the Massachusetts Institute of Technology in 1959, and the PhD in the field of applied mechanics from the California Institute of Technology in 1962. His thesis was in elastic wave propagation. Dr. Rosenfeld joined the Components Division of IBM Corporation in 1962 where he worked on the packaging of microelectronic components. In 1964 he joined RCA Laboratories. At RCA he has applied computers to the making of masks for electronic circuit and component production. He has developed a computer language for describing patterns and enabled the computer and an automated plotter to generate patterns from their description in that language. Dr. Rosenfeld is a member of the American Society of Mechanical Engineers, the Institute of Electrical and Electronics Engineers, the Association for Computing Machinery, and the American Association for the Advancement of Science. He received an RCA Laboratories Achievement Award in 1966.

THE METHODS used for programming N/C machines range from completely manual methods to powerful, computer-based techniques. Manual methods utilize inexpensive equipment and are easy to understand, but they are limited to the programming of simple jobs. The most advanced and versatile methods require sophisticated computer systems still under development. Between these extremes, there are partly manual methods of programming and readily available, computerized methods.

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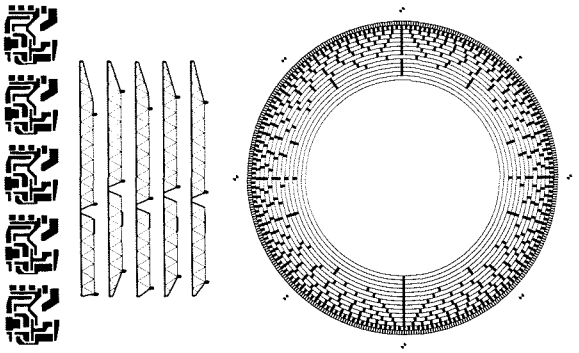
Numerically controlled machines

It is possible to apply numerical control to a variety of manufacturing equipment. Most N/C machines in use are for metal cutting operations, such as milling, boring, drilling, and turning. Among the other applications are flame cutting, assembly, inspection, and drafting. Especially important to the electronics industry is the numerically controlled artwork generator or pattern-making machine. Artwork is made on a numerically controlled drafting machine with the pen replaced by a photohead for exposing photographic films or plates. The photohead operates as a slide projector with a slide-changing mechanism also under numerical control.

In the metalworking industry, numerical control has been especially valuable for production runs of small quantities. The cost of programming for N/C is less in these cases than the cost of the special tools used in mass production equipment. Also, for these jobs manually controlled production is slower and less repeatable than N/C production. Because small quantities of complex parts are commonly required in the aerospace industry, they have pioneered N/C production and are owners of multimillion dollar machining centers. The automobile industry is starting to use numerical control for die sinking. The advantage is the ability of N/C machines to make complex contoured surfaces. Electronics artwork is made under numerical control because it is complex or repetitive. Another important reason for the use of N/C to produce electronics patterns, or other parts, is that a computer is often used to design the parts and a numerically controlled machine is the most direct output of the computer. Thus, numerical control becomes a natural adjunct of computer-aided design.

Numerically controlled machines are generally classified in terms of the number of axes of motion and the type of control on each axis. A vertical milling machine has three axes, two along the plane of the table and one parallel to the tool axis. If, in addition, the table of a milling machine can be rotated around two axes perpendicular to the tool axis, then the milling machine is said to be a five-axis N/C machine. Numerically controlled drills have two axes of control. The tool itself is raised and lowered between stops and its motion is not considered to be along an axis. The program on the control tape commands successive motions of the N/C machine. Two or more axes of the machine may be commanded to move simultaneously by the control tape. If the controller only guarantees the correctness of the ends of the motion, it is considered to be a point-to-point controller. On the other hand, contouring machines also control the path of motion along a precise straight line, circle, or parabola. Only contouring machines are capable of cutting complex surfaces. The controller of the N/C machine is a special-purpose digital computer. Small, general-purpose digital computers can be programmed to carry out most of the functions of an N/C controller. Lately, consideration has been given to controlling several N/C machines simultaneously from one large general purpose computer.

Within RCA both a wide variety of N/C machines and programming methods are in use. In one application, an N/C milling machine with contouring control is used to machine a sculptured surface. A computer program is used both to design the surface and to produce the tape to control the N/C



Typical patterns made from PREP programs.

machine. In the point-to-point class of machine, RCA utilizes drilling machines and sheet metal punching machines. These can often be programmed by manual techniques. Artwork for integrated circuits and printed circuits is made on precision drafting machines with contouring control. A variety of manual, partly manual and computer-based techniques are used to program for artwork production.

Computer-free methods

Manual programming for numerically controlled production is common where jobs are simple or computers are not conveniently accessible. Manual programming is feasible where there are few computations required to determine the coordinates of the motions of the N/C machine. Another method of programming which does not use a computer is based upon the digitizer. In these methods, the tape codes for the operation of the N/C machine are produced directly by the programmer or by the operator of the digitizer.

The information on the paper or magnetic tape for an N/C machine is coded in a standard code, one character per line across the tape, and serially by character. One particular character code is called the "end of block" character. The characters between two successive end of blocks constitute a logical unit of information called the "block". Each block contains the command for one motion or other action of the N/C machine. Within a block, information is grouped in logical units called words, each of which begins with a key character. Typically X signifies motion of the X axis, Y motion of the Y axis, and other characters denote tool selection or control of feedrate or coolant. In a machine where F controls feedrate, the block

X+01300Y−02700F32

specifies motions to a coordinate X= 1.3″ and Y=2.7″ with a known feedrate.

The codes to control an N/C machine can be punched directly into paper tape by a machine called a Flexowriter [Friden tradename], which is a typewriter attached to a paper tape punch. The Flexowriter is certainly the least expensive equipment for preparing N/C tapes. Although it requires knowing the formats accepted by the N/C machine, it is useful as a method of programming very short jobs and for programming tests of the N/C machine. A Flexowriter is also equipped with a paper tape reader. The reader can be used to copy a paper tape with alterations. The relative difficulty of correcting programmer errors by doing this type of editing operation is one of the weaknesses of Flexowriter programming for N/C.

The digitizer provides a form of automated programming for N/C machines which is especially useful in integrated circuit and printed circuit applications. A digitizer can be described as an "undrafting machine" because its input is a drawing and its output is a paper tape to be used by an N/C drafting machine or drilling machine. When a digitizer and an N/C drafting machine are to aid in the production of artwork, a precise drawing of the artwork is first made by hand on graph paper. This original is mounted on the digitizer table. A viewing device is moved manually from point to point over the drawing. At each desired point, the viewing device is stopped and the paper tape punched by the digitizer with the coordinates of the point. Special codes other than the coordinates of the points can be produced manually.

Artwork produced by a numerically controlled drafting machine programmed by a digitizer is more than just a copy of the original, digitized drawing. Where lines and points are shown on the original drawing, the artwork producing machine is able to draw lines of precise width and flash pads of specific shapes. There is a gain in accuracy because the digitizer automatically rounds dimensions to the nearest line of a specified grid. However, the digitizer does not take full advantage of N/C for doing repetitive jobs accurately and easily. The digitizer must be used repetitively in order to program such jobs. Furthermore, the digitizer puts great demands on its input, the drawing, and forces jobs to a certain grid. But the digitizer is good at capturing data from a drawing, and its output is used effectively as input to computer programs.

Some numerically controlled metal cutting machines combine the functions of machine tools and digitizers. In the digitizing mode, an operator steps the machine through the process and the numerical control tape is punched automatically. This same tape can be read back into the machine to repeat the steps of the process. The machine tool then reproduces that first part faithfully. This method of programming is easy to introduce into a machine shop and requires no additional equipment. But it is of no assistance in performing jobs that cannot be done under operator control.

Conventional computer-assisted methods

Numerically controlled machines and digital computers were developed during the same era. Because of the numerical form of N/C control tapes, it is not surprising that the digital computer has been used to assist in making the control tapes. Sometimes the calculations required of the computer are simple in nature. At other times the computer is asked to design the part to be made. In general, the computer is used because its input can be made simpler than the control tape that the computer will produce for the N/C machine. The input to the computer may be in some simple format containing parameters for a design program, or it may be the output of a digitizer. Commonly, the input format is a complex formalized language. In that case, the computer program is said to translate the input language into the control tape for the N/C machine.

Numerical control languages

There are several languages in use for programming N/C machines with the assistance of a computer. The most widely used language is APT (Automatically Programmed Tools), which was

developed at MIT under the sponsorship of the Aerospace Industry. Currently APT is being maintained and improved at the Illinois Institute of Technology Research Institute, under the APT long range program, of which RCA is a Corporate member. The translater for the APT language requires a large scale digital computer. For the benefit of those who might only have access to a moderate sized computer, a number of other N/C languages have been developed. Most, like ADAPT, have only two dimensional capabilities. A language designed specifically for artwork programming called PREP[1] (PRogrammed Electronics Patterns) has been developed at RCA Laboratories.

APT language

Programs in the APT language describe parts in terms of their bounding surfaces. The surfaces in turn are described in terms of familiar geometric constructions such as circle, plane, point, etc. There are many ways of defining each surface. For example, there are ten ways of describing a circle, including: giving the center and radius, giving the radius and two lines to which the circle is tangent, and giving the center and a point on the circle. In addition to the description of surfaces in an APT program, there are instructions for cutting the part. By means of the APT language, the programmer specifies along what surfaces the machine tool is to cut. The computer figures the offset of the center of the tool from the surfaces. The APT language includes statements for doing computations, although these are handled less efficiently than by a computation language such as FORTRAN. This language also provides for direct control of special machine functions, such as the coolant or the changing of tools. The final stage of computer processing of the APT language is done by a program called the post-processor. To accommodate a wide variety of machine tools, a different post-processor is used for each type of machine tool. The richness of the APT language has resulted in a very large interpreting program. The APT processor is only available on a very few of the major computers; APT will be more useful within RCA when it becomes available on the Spectra 70 computer.[2]

PREP language

The PREP language has been designed specifically for ease of programming of electronics artwork patterns; locations on the pattern are defined by the same commands that plot to them. The commands themselves are abbreviated to save time for the user. There are simple commands for drawing lines, circles, arcs of circles, and rectangles, and for plotting points. There is a command for making repeated copies of parts of a pattern. Parts of a pattern can be programmed relative to local axes, which can be rotated or mirrored. On artwork it is often desired to make solid black polygons. A PREP language program can specify the vertices of such a polygon and the PREP processor constructs all of the motions necessary to fill the polygon in solidly. The PREP processor at the Laboratories has been integrated into the photomask operation. This processor writes out the instructions to the operator for setting up the job on the numerically controlled drafting machine. A new, advanced version of the PREP processor runs on the Spectra 70 computer.

Subroutine library

One way of enhancing the usefulness of numerical control languages such as APT and PREP is through the maintenance of libraries of subroutines. The library is shared by many users of the language. For example, a PREP library might contain programs for each layer of masking of each type of transistor used in integrated circuits. Then, the writing of a PREP program for an integrated circuit would consist largely of calling for the transistor patterns from the library and their placement at the proper locations on the integrated circuit pattern. The library approach simplifies programming and guarantees a standardization among many programs. In the aircraft industry, lofting curves, curves describing the aerodynamic surfaces of the aircraft, are kept in a library. Reference in an APT program to a particular lofting curve results in a part machined to fit that curve. Use of the library assures that the parts of the aircraft will fit together smoothly. The library is one example of how the power of a computer in numerical control programming is expandable.

Small-scale language

The smallest scale N/C computer language[3] is probably represented by a recently announced language to fit on a PDP 8/S computer, which sells for only $10,000. Although quite limited by the standards of APT, this language contains the basic essence of what is needed for two axis point-to-point applications such as punching and drilling. In this language, it is easy to specify the coordinates of holes or repeated patterns of holes. The computer assists in the editing of programs and formats the output tape properly for the N/C machine.

Other applications of the computer

Often the computer is used to design a part. Then, the output of the computer can be the tape to direct an N/C machine to make the part. Numerically controlled production is a natural output of computer-aided design. A common way of linking the computer-aided design program to numerically control production is to write the design program to generate statements in a standard N/C language. The processor for the N/C language makes the control tape for the N/C machine.

Sculptured surfaces

In one important application, a sculptured surface is machined under numerical control. There is no simple equation describing the surface, but rather a complex computer program calculates points on the surface from experimental data and certain theoretical considerations. The computer carrying out the design computations punches onto data processing cards a numerical description of the surface. A second program reads these cards and writes on a magnetic tape statements in the APT language. The APT processor reads the magnetic tape, interpolates a surface between the points, and makes a paper tape for machining the contoured surface. This entire process is automated from the point of entering the experimental data to the time when the final part is removed from the N/C machine. Human intervention is required only to review computer printouts and to set up the machine tool.

A variety of computer design programs are used through N/C language processors to make parts under numerical control for RCA. One such program,

FMILL[4], which was originally developed by Boeing Aircraft Company, is used in conjunction with APT for the machining of sculptured surfaces. When a computer program designs a surface, it calculates only a limited number of points. The FMILL program is an interpolation procedure to calculate enough additional points to define a smooth surface for machining through the APT system. In another application, N/C is used as a means of producing graphs from a computer. A FORTRAN program computes design curves and writes on a magnetic tape the PREP statements required to draw a graph of the curves. An automatic drafting machine draws the graphs.

Design automation programs

The linkage between design automation programs and numerical control is natural. Although many design automation programs generate an N/C tape directly, the passing of the design data through an N/C language processor utilizes features built into the N/C language. The N/C languages are not adequate for programming complex design calculations efficiently. It is possible for part of the data for the design program to be statements in the N/C language. The design program would pass such statements on directly to the N/C language processor. The medium of interface between the design program and the language processor can be cards, magnetic tape, magnetic disk, or core memory. The actual medium chosen for any application depends on what inputs are acceptable to the language processor and whether the design program can be run on the same computer.

Printed circuit wiring

An experimental program for automatically determining where wires should be routed on printed circuit boards has been written in the SNOBOL language on the RCA 601 computer. The results of this program are formed into statements in the PREP language. These are processed by PREP to make the artwork designed by the computer. This example represents an area of widespread interest and activity in the electronics industry, the automated design and layout of printed circuit and integrated circuit patterns. A program developed by the Information Systems Division routes the backplane wiring for the Spectra 70 computers. That program directly writes magnetic tapes for automated drafting machines.

A system developed by Defense Electronics Products benefits from the virtues of both the digital computer and the digitizer.[5] The digitizer is used to enter coordinates of patterns onto punched cards for further processing by the computer. The computer converts the digitized vertices of polygons into the motions required to make solid black polygons on the drafting machine. The computer also maintains groups of digitizer input as subroutines. These subroutines can be placed, according to data on other digitizer cards, to make complex patterns which are composites of many subroutines.

Time-shared computers

The time-shared application of large-scale computers has enormous potential to increase the value of computers, especially to engineering design work and to numerical control. Time-sharing allows N/C users and others simultaneously to share the power of a large computer and to receive reasonably quick response to inquiries requiring short computations. As in the programming of computational procedures, the writing of N/C programs requires careful debugging. Time-sharing promises to reduce the time required to correct mistakes and thereby reduce design turnaround time.

Within a time-sharing system, a numerical control language processor is an application program shared among many programmers. The language processor may be supplied by one user for limited distribution or it may be more generally available as part of the time-sharing system itself. Programs written in the N/C language also can be shared among several of the N/C programmers. A library of such programs can be maintained. Commercial time-sharing systems are now starting to offer vastly scaled down versions of APT. The PREP language has been used in time-sharing since the beginning of 1967.

Essential to the application of time-sharing to N/C programming is the availability of a graphical output device at the local time-shared terminal. Fortunately for artwork applications in electronics, a two-dimensional drawing can show the complete details of the output of an N/C program. J. C. Miller and C. M. Wine of the Laboratories have developed a time-shared graphic terminal, called the MODEL T,[6] which has been used with a time-shared computer to verify programs written in the PREP language. The MODEL T is capable of drawing on a plotter or on a storage oscilloscope.

In the operation of the time-shared version of PREP, the PREP processor reads a file of PREP statements and draws a pattern on the MODEL T. The file of PREP statements is maintained permanently in the computer. It is built up and edited by the user until it is a correct and complete description of the desired artwork pattern. A system editor program is used to edit the file of PREP statements, and the PREP processor is used for plotting the file. When the final drawing from the time-sharing system is acceptable, the computer makes a control tape to drive a precision drafting machine for making the artwork. In this mode of operation, the interaction time between the user and the computer is measured in minutes. Within only a few minutes time, the PREP programmer can receive a drawing from his program, he can recognize and find corrections for his errors, and he can enter the corrections into the file so that the drawing can be made again. The time-shared version of PREP contains facilities allowing the user to inquire concerning the size of his pattern and the coordinates he has generated at certain places in his program. The computer is able to search for him and find what place in his program caused a certain part of the pattern to appear.

H. R. Beelitz and C. T. Wu[7] have demonstrated the use of the time-shared PREP system along with a special preprocessor of their own design to program the production of artwork for complicated computer printed circuit boards. The preprocessor translates a higher level language similar to PREP into the PREP language. The higher level language has features which are of particular value in the type of pattern with which they work. The PREP processor is used to make the drawings. The file of PREP statements, when

it is complete, is used both to make a tape to control the drafting machine and to make a control tape for an N/C drilling machine.

Interactive Graphic Displays

The most exciting and potentially powerful development in the field of N/C programming centers around interactive graphic displays for use with computers. These displays use cathode-ray tubes coupled to versatile electronic controllers. Other time-sharing terminals capable of displaying graphics cannot change their display rapidly and their input from the human user can only be through a keyboard. But a CRT display can be changed rapidly and input can be purely graphical in the form of drawing on the CRT face or pointing at the pattern. As a designer programs a part by drawing it, he is able to see the result immediately on the display. The interactive display is useful, more than just for programming parts for N/C production, but also for designing them. The CRT display is effectively a draftsman assistant to the designer.

The pattern displayed on a CRT must be maintained in a memory and redrawn on the CRT at least 40 times per second to prevent flicker. Generally, the pattern is stored in a core memory as a file of commands to the controller for drawing the pattern. To change the picture, it is necessary only to change the relevant part of the command file. The complexity of the pattern is limited by the number of commands which can be displayed without slowing the display down so that it flickers. The controller itself is largely a digital computer and may, in fact, be a general purpose digital computer with special interfaces to the cathode ray tube.

A designer enters graphical data into a computer from the display by means of a light pen. The light pen is a device shaped and held much like a pen and capable of detecting the light on the CRT screen. While the light pen is held in front of the CRT, the display controller is able to tell exactly which part of a pattern is being displayed at any moment the light pen detects light. Thus, the light pen can be used to pick graphical entities from the displayed pattern. By a more complicated means, lines can be drawn when the display controller causes a small cross of light to follow the motion of the light pen. Graphical data can also be entered into the computer by means of a tablet-like device, sensitive to the position of a pointer over the device. The position of the pointer can be detected electrostatically, as in the RAND tablet,[9] magnetically,[10] or by means of a resistive coating.[11] The purely graphical computer inputs are always supplemented by a teletypewriter for input of numeric or symbolic information.

The CRT display requires expensive and complicated software. The programs for utilizing a CRT display allow the user to interact with the machine and to manipulate the displayed pattern. The user is allowed to delete part of a pattern, to change a line, to change a single point, to add to a pattern, to move part of a pattern and so forth. Although a number of interactive graphical systems have been developed to illustrate the power of the CRT computer terminal, few are close to economical utilization. Norden Electronics[12] has built a system which aids in the layout of bipolar integrated circuits. The designer is able to move transistors and resistors around until the optimum layout is found. The computer restrains the pattern to comply with standard layout rules. The computer is also programmed to attempt parts of the layout without interaction. The Norden system could be made to produce control tapes for N/C mask production. On the metal-working side of N/C, Lockheed Georgia[13] is using an interactive console to program parts to be machined under N/C.

The key to effective programming for interactive graphical displays is in the data structure used internally by the computer to describe the displayed pattern. A linked list is used to model the geometrical constraints implied by the construction of the pattern. The modelling can be illustrated by two examples:

1) A line may be defined by two points. In that case, the line would be represented in the computer memory by two numbers, each referencing a point. A change of either point would implicitly change the line.
2) A resistor may be defined by its position relative to a transistor. The part of computer memory reserved for data on the resistor would contain incomplete information about the resistor's position. But a pointer would refer to the data on the transistor's position.

Conclusion

A wide range of systems is available for programming the production of parts under numerical control. Simple jobs are programmed manually, but sophisticated computer-based systems have been developed to simplify the information that must be prepared for producing complicated parts. The traditional and most general approach to utilizing a computer to assist in N/C programming is through the computer language defined specifically for numerical control. Where computer programs carry out the design of parts, their production under N/C is the output of the design programs. With time-shared computers, computer assisted N/C programming is carried out more rapidly and with more interaction between the N/C programmer and the computer. These programmers will someday benefit from interactive programming and computer assisted design along with a natural graphical language on CRT consoles.

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Automatic generation of tests for combinatorial logic

H. I. Hellman

To test any combinatorial logic net with N inputs, it is not necessary to use all of the 2^N possible input combinations. An easier approach is available wherein each logic element is tested for each possible failure mode. Using this approach for a logic net of approximately 100 gates, the number of tests is typically between 25 and 50.

Henry I. Hellman
Digital Equipment Technology
Defense Communications Systems Division
Camden, N.J.
received the BEE degree from College of City of New York in 1938. He was employed at the Lummus Company for several years where he was promoted to electrical design supervisor. In 1959, he joined Univac where he held the position of Department Manager on the Univac III Computer System Project, with responsibility for logic circuit design, backplane wiring rules, logic card fabrication and a system test simulator. Since joining RCA in 1961, his principal assignments included computer diagnostics, logic design and analysis, and automatic generation of tests and diagnostic programs for digital logic nets. He was responsible for automatic diagnostics for the central processor and memory systems of the Microrac computer. He has designed the logic and hardware necessary to implement automatic testing and localization of faults within a computer system. He has written and implemented computer programs for generating the tests used in testing logic plug-in cards and computer systems. One of these programs is described in the AGAT (Automatic Generation of Array Tests) User's Manual, which he wrote. Mr. Hellman is a registered professional engineer in New York State and is a member of the IEEE and the IEEE Computer Group.

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A COMPLETE SET of tests for a block of combinatorial logic may be derived automatically using the AGAT program. Each test consists of a set of net input levels (1 or 0) to be applied to the net inputs and the corresponding net output levels (1 or 0). Each test will check the logic net for the presence of one of a number of possible faults. The test may be performed by applying the net input levels and comparing the actual net output levels with the "normal" net output levels. A complete set of tests will check each logic element for the output "stuck" at 1 or 0, or for an open input. Logic elements may be various combinations AND, NAND, OR, NOR types. A deck of punched cards (each card describing a single logic element) is the data input to the program, and the total number of tests generated is a function of the logic connectivity.

The program generates a number of interconnection tables and reference lists from the data input, including a list of each possible fault within the logic net. A fault-mode indicator is available for each fault, establishing whether that fault has been tested previously or not, and whether that fault is detected by the current test.

The program selects an untested fault and establishes a test pattern for testing that particular fault. Since the test pattern also tests other faults, these additional faults are also listed. At the end of each test, a check is made to establish if all faults have been checked by either the current test or a previous test. If all faults have been checked, the test generation sequence is completed.

A typical logic net of 90 gates requires approximately 5 minutes of running time on a Spectra 70/45 computer. Special options are available such as the fault simulation check. With this option, it is possible to simulate each possible fault within the logic net, apply the derived test net input levels, and determine if the "normal" net output levels are affected.

AGAT program

The AGAT (Automatic Generation of Array Tests) program (Fig. 1) derives a complete set of tests from a deck of punched cards which describe the logic connectivity of a logic net. Two control cards, operating in conjunction with a program on magnetic tape, call in the program on a Spectra 70/45 (or equivalent) system. The computer executes the program by reading the logic connectivity on the deck of punched cards and automatically generates a complete set of tests.

In the program, a failure at a given point in the logic net is assumed. Then, the program generates the signals that are necessary at that point for the failure to be detected on the output of the logic element to which the point is immediately connected. The signals are traced to a net output—assigning signals on other lines feeding each logic element as it is encountered. The signals on the other lines are selected to permit the transmission of the failure information through each logic element. The process is continued until a net output is found that is sensitive to changes in the signal of the failing line.

When one such output is found, the tracing proceeds backwards from the point of failure to the inputs. This process is continued until a complete set of inputs is found for the logic net which will detect an assumed failure within the logic net.

Test generation

A previously untested fault mode is selected as the *initial fault mode*. Starting from this point in the logic net,

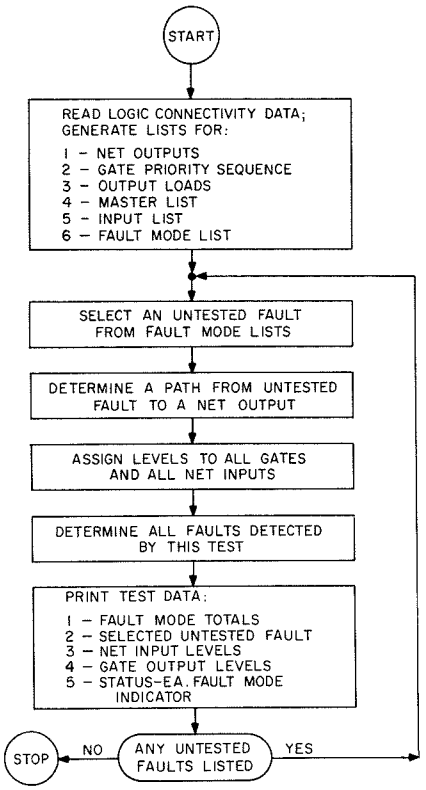

Fig. 1—AGAT program.

```
DATA-TEST NO. =    5
FAULT MODE INDICATOR TOTALS.....SEE LEGEND
(-1)    1 :(0)    11 :(1)    28 :(2)     7 :(3)     3
INITIAL FM GATE=   6 MI LIST INPUT = 12
(NET INPUT-LEVEL)
500   1 501   0 502   1 503   0
(GATE NO.-OUTPUT LEVEL)
  1   1  2  0  3  0  4  1  5  0  6  1  7  0  8  1  9  1 10  0 11  1 12  0
(GATE NO.-OUTPUT FAULT MODE INDICATOR)
  1   1  2  1  3  2  4  0  5  1  6  1  7  0  8  1  9  0 10  1 11  1 12  1
(GATE NO.-AUXILIARY OUTPUT FAULT MODE INDICATOR)
  1   1  2  1  3  1  4  1  5  1  6  2  7  1  8  3  9  1 10  2 11  3 12  3
(MI LIST NO.-INPUT FAULT MODE INDICATOR)
  1   1  2  1  3  1  4  1  5  0  6  1  7  1  8  0  9  1 10  1 11 -1 12  2 13  0 14  1 15  1
 16   2 17  1 18  0 19  2 20  0 21  1 22  0 23  0 24  2 25  0 26  1
```

Fig. 2—Test number 5 results.

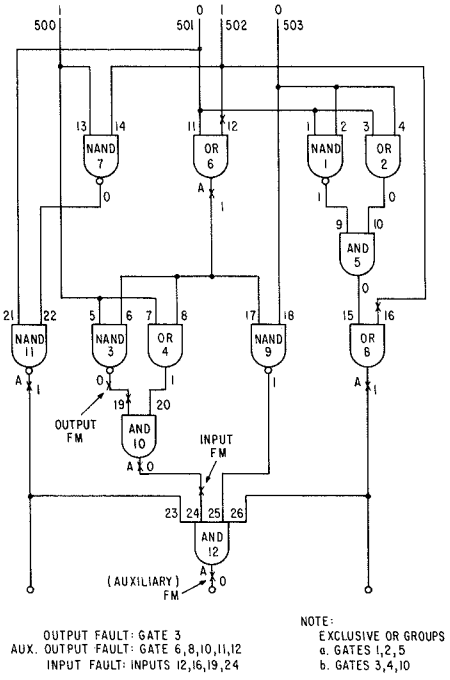

Fig. 3—Logic net with test number 5 results.

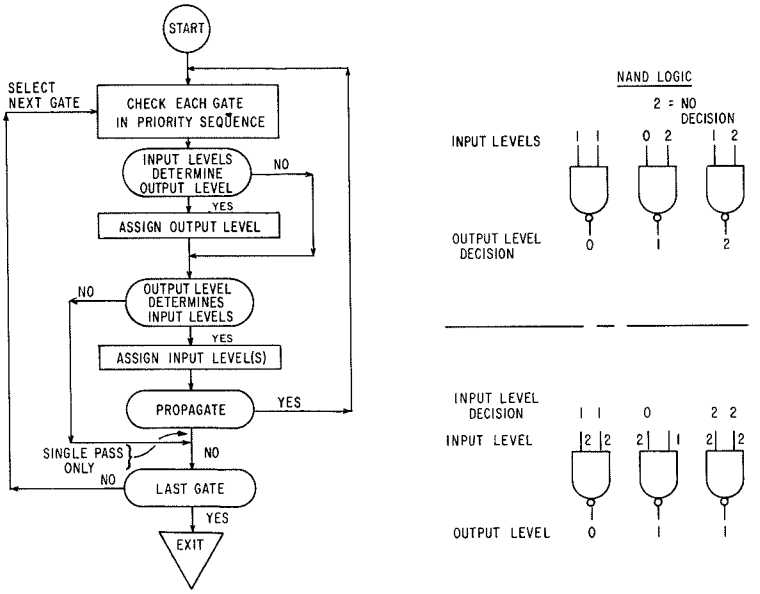

Fig. 4—AGAT propagate routine.

signal levels are selected for the inputs of each gate as a path is sensitized to a net output gate. This procedure is called *forward sensitizing*. When a net output gate is reached, the operation is reversed. In effect, a *backward propagate* is required to determine the net input levels required to achieve the signal levels for the inputs to the gates of the forward sensitize path. When all net input levels and all gate output levels have been determined, the computer recognizes this state as *test generated*. At this point, a procedure (*determine fault-modes tested*) is used to determine all paths which have been sensitized to net outputs, and a list of fault-modes tested is generated.

A fault-mode status indicator is stored in the computer for each possible fault mode within the net. At the completion of each test generated, all of the fault mode status indicators are updated based on the results of the determine-fault-modes-tested routine. The status indicator is used to indicate one of five possible states.

In the forward-sensitize procedure, there may be numerous paths which can be selected for sensitizing. The criteria here is to select a path using fault modes which have not been previously tested. If this is done, the number of tests generated will be minimized. In this routine, the fault mode status indicators are referenced prior to selection of the sensitized path.

The backward propagate routine previously discussed is actually a combined backward sensitize and backward propagate routine. In this routine, if a choice of inputs to a gate is available, a set of inputs will be selected to sensitize an additional path from a net output (this is not always possible). This also is useful in minimizing the number of tests generated. In addition, if a choice of fault mode indica-

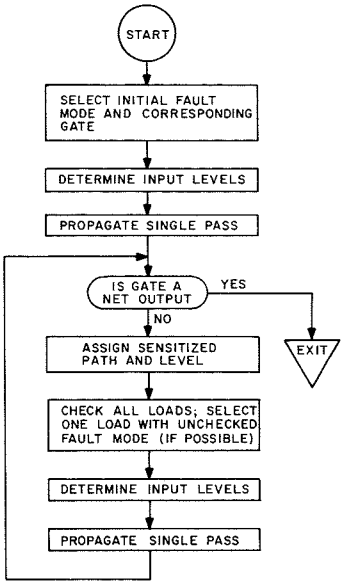

Fig. 5—AGAT forward sensitize.

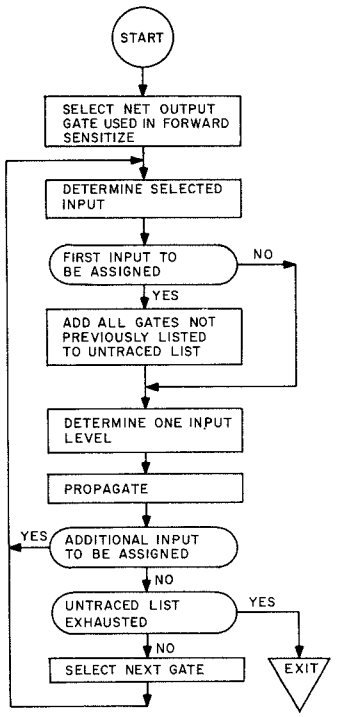

Fig. 6—AGAT backward sensitize.

TEST NO.	1	2	3	4	5	6	7	8	9	10	11
INPUT PIN										TEST LEVELS	
500	1	1	1	1	1	1	0	0	0	0	0
501	1	0	1	0	0	1	1	0	0	0	1
502	0	0	0	0	1	1	1	1	0	1	1
503	1	1	0	0	0	1	1	0	1	1	0
OUTPUT PIN										TEST LEVELS	
8	0	1	1	0	1	1	1	1	1	1	1
11	0	1	0	1	1	1	0	1	1	1	0
12	0	1	0	0	0	0	0	1	0	0	0

LEGEND: TRUE = 1 = HIGH = +5V
FALSE = 0 = LOW = GROUND

Fig. 7—Test data summary.

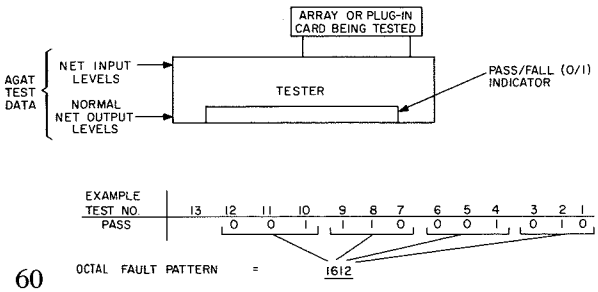

Fig. 8—AGAT fault patterns program.

FAULT TYPE	OCTAL FAULT PATTERN	FAULTY CHIPS
20	0	6
1	1	1 5
19	2	3 4 9
17	4	1 2
22	5	7
2	10	2 5 12
8	11	8 5
3	20	3 10
7	40	7 11
18	200	3 4 9
10	202	10 12 3 4 9
23	360	8
4	400	4 10
6	402	6 1 2
5	406	5 1 2 8
14	420	10 12
9	1000	9 12
12	1220	6
24	1612	11
15	1672	11
25	2000	12
21	2100	7
11	2105	11 7
16	3575	12
13	3766	8

LEGEND: TEST #1 = LEAST SIGNIFICANT BIT OF OCTAL FAULT PATTERN. BINARY BIT = 1(0) CORRESPONDS TO TEST FAIL (PASS)

Fig. 9—AGAT fault patterns.

tors is possible, then the backward sensitize will select a previously untested fault mode.

A propagate routine is used to permit propagation of selected gate levels in both a forward and backward direction. This is useful in minimizing the possibility of generating a conflict. (A conflict is defined as a condition where input and output levels of any gate within the net are incompatible.)

In the signal tracing mode, a distinction must be made between required and selected input levels. If we consider positive NAND logic, inputs and corresponding output levels for a 3-input gate are as follows: (X=DON'T CARE)

Inputs	*Output*
1-1-1	0
O-X-X	1
X-O-X	1
X-X-O	1

If we are backward sensitizing/propagating, and an output level is selected as 0, then all inputs to that gate are *required* to be 1. It should be further noted that all gates driven by the gate with the 0 output are *required* to have an output level of 1, however, the remaining inputs to the driven gates can be *selected* as 1 or 0.

In these latter cases, a propagate routine is useful in ascertaining whether the remaining inputs are *determined* due to a previous decision, or can be *selected* to suit other requirements.

Flow charts for the propagate routine, forward sensitize and backward sensitize are shown in Figs. 4, 5, and 6. The criteria for making output-level decisions and input-level decisions in the propagate routine is illustrated in Fig. 4 using NAND logic. The gate priority sequence referred to in Fig. 4 is a list of all gates in the net, in order of their position (delay) relative to a change of net input levels.

Computer test output data

A small logic net consisting of twelve logic elements with four net inputs and three net outputs is shown in Fig. 3. Fig. 2 indicates one (test #5) of a series of eleven tests generated by a computer run. In this test, the logic net is tested for ten faults (out of a total of fifty possible assumed faults). The initial FM gate indicated on Fig. 2 specifies the assumed failure within the logic net.

An AGAT option is available which permits writing of the generated test data on magnetic tape. The magnetic tape may be used as input data to an auxiliary program which is used to modify the test data in accordance with a user's requirements. Fig. 7 illustrates the use of an auxiliary program to provide a concise summary of the test data. In this application, it was assumed that the logic net was a plug-in card with four input pins and three output pins, and each logic element was a separate IC chip.

Applications of AGAT

The AGAT program may be used to test an array or a plug-in card consisting of interconnected logic elements. In Fig. 8, a tester is used to compare the expected (normal) net output levels for each test with the corresponding output levels obtained on the output pins of the device under test. If all of the tests pass, it is assumed that the device has no faults. A pass-fail indicator may be used to generate an octal fault pattern (assuming a fault exists), which may then be used to diagnose the fault. The auxiliary program was used to generate a list of possible octal fault patterns, as shown in Fig. 9. The octal fault pattern 1612 of Fig. 8 is listed as fault type #24 on Fig. 9, and diagnoses element #11 as the fault.

The application of AGAT is described in detail in a *User's Manual* which is available as part of the DEP Design Automation System.

Computer-aided design of integrated-circuit platters

H. R. Beelitz | C. T. Wu

This paper describes the computer graphics techniques that have been developed as an aid in fabricating LIMAC—an experimental computer. The time-sharing software developed together with a hierarchy of display systems permit the rapid conversion of printed-circuit wiring sketches into debugged photomasters for the large LIMAC platters. The platter artwork design methods are described within the context of the overall computer design problem involving system and logic design, integrated circuit and array technology, and large platter packaging.

THE DESIGN METHODS and techniques discussed in this paper were developed in response to the need for fabricating the physically large and functionally complex printed circuit platters used with the LIMAC experimental computer. LIMAC (Large Integrated Monolithic Array Computer) has been designed by RCA, in conjunction with the Air Force Avionics Laboratory, to demonstrate and evaluate the use of array technology in a computer environment. Concurrently, LIMAC embodies novel system design concepts that provide for more effective use of large arrays. A key aspect of LIMAC system design is the functional partitioning of both control and data path logic.[1,2]

The initial version of LIMAC is being constructed using commercially available RCA integrated circuits in flatpacks mounted on 12x15-inch laminated, two-layer printed-circuit boards. These large printed-circuit platters are required in order to encompass a sufficiently large grouping of logic to permit the later substitution of arrays containing upwards of 300 gates.

The unique system organization of LIMAC, which has established a basic relationship between system organization and packaging, permits a straightforward partitioning of the logic into relatively few circuit boards. All the bipolar logic is contained within nine large platters. Nine additional 4½x6-inch two-layer cards contain auxiliary logic associated with the LIMAC console. These 18 boards comprise the entire main frame logic exclusive of cards for lamp drivers, etc.

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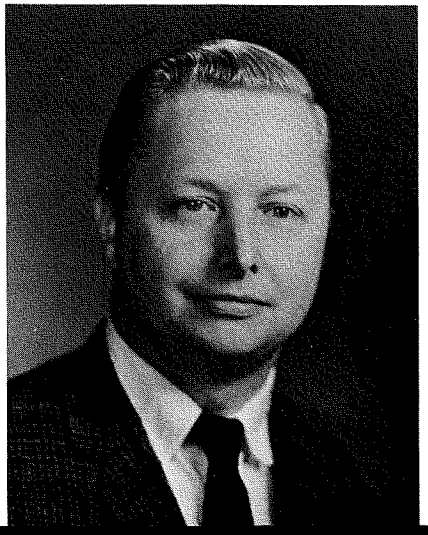
Each large platter has the capability of mounting up to 425 surface bonded flatpacks on ½x⅝ inch grid. The 186 platter contact pins on 0.150 inch centers are distributed along both top and bottom surfaces of the platter's 15-inch edge and permit connection to the parallel wired backplane. A camlock type of connector is used to simplify platter insertion and removal. A combination of tri-plate printed wiring and wire-wrap serves as backplane interconnection. Critical machine busses common to all platters are contained in the printed wiring of the backplane. The remainder of the backplane interconnects are wire-wrap.

Fig. 1 is a photograph of LIMAC. Two commercially available card files or "nests" are visible in the opening on the upper left side of the front panel of the console. The right nest houses the nine large bipolar logic platters (plus one spare). The left nest houses CMOS memory platters. The nine small circuit cards plus lamp driver cards, etc. are contained in a standard 29-card nest (not visible) located behind the control panel.

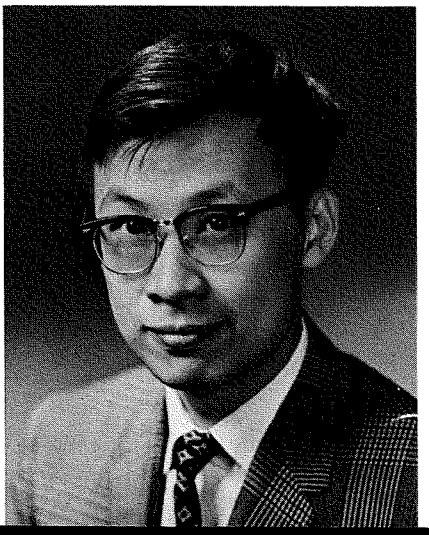
The design process

The flow chart of Fig. 2 gives the major steps in designing and fabricating the large integrated circuit platters used

Howard R. Beelitz
Data Processing Applied Research Laboratory
Laboratories
Princeton, N.J.
received the BSEE from Newark College of Engineering in 1959 and has since done graduate work at N.C.E. and Princeton University. Mr. Beelitz initially joined RCA's Electron Tube Division in 1957 to work on the development of ceramic-to-metal seals for use in pencil-type vacuum tubes. In June, 1959, Mr. Beelitz joined the Technical staff at the Laboratories. His early work involved both applications and fabrication studies of tunnel diodes. He was later engaged in research on thin-film organic-diode and thick-film resistor-array associative memories. More recent assignments included research in monolithic sense circuitry for integrated ferrite memories. His current interests include large scale integration of bipolar logic for experimental computers and computer aided interactive graphic techniques for artwork generation. Mr. Beelitz has been granted a number of patents and has authored many papers. He is a recipient of two RCA Laboratories Achievement Awards. Mr. Beelitz is a member of Tau Beta Pi and Eta Kappa Nu.



Chin Tao Wu
Data Processing Applied Research Laboratory
Laboratories
Princeton, N.J.
received the BEE from The City College of New York in February, 1965, and the MS in Electrical Engineering from Columbia University in 1967. He is currently studying for a doctorate degree at the same university. Mr. Wu joined the Technical Staff at RCA Laboratories in February 1965. His various initial assignments include interconnection problems of digital devices, study of the cause of instabilities in evaporated thin-film field-effect transistors, and the Gunn effect on epitaxially grown GaAs crystals. His later work involves the design and fabrication of optically modifiable nets of iterative logic arrays. He is currently involved with the automated design techniques for mask artwork generation. Mr. Wu is a member of Eta-Kappa-Nu and Tau-Beta-Pi.



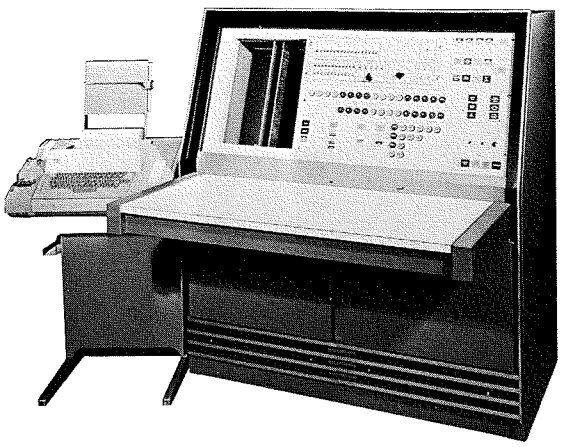


Fig. 1—The LIMAC computer.

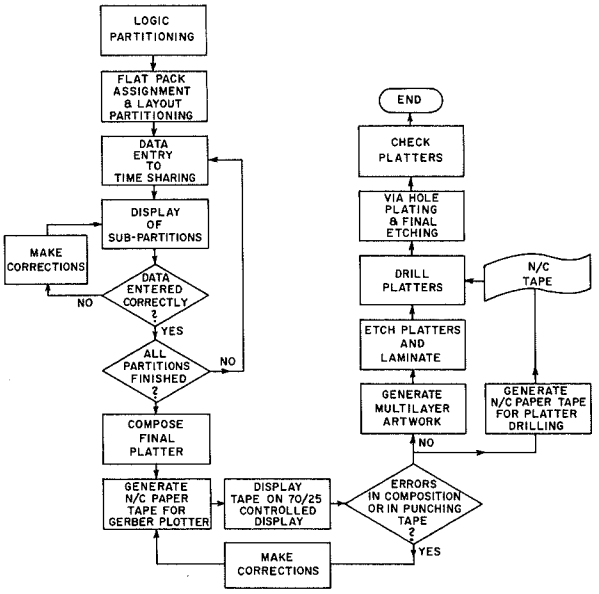


Fig. 2—Design process flow chart.

with LIMAC. This design process begins with the availability of partitioned logic for a given platter and terminates when the circuit board is completed. The flow chart illustrates that computer systems have played a major role in the design cycle of LIMAC. Indeed, platters of this physical size and logic complexity would be extremely difficult to design and would probably prove to be impractical without computer augmented design techniques.

LIMAC platters

The logic encompassed by a given platter is first partitioned into clusters of approximately 50 to 300 gates to facilitate their later replacement by arrays. Tentative gate assignments to flatpacks are then made. These clusters are subsequently repartitioned into smaller groups of about 10 to 15 flatpacks for ease of programming and debugging.

Interconnecting paths between flatpacks are manually routed using the logic flow as shown on the partitioned logic diagrams as a guide. In almost all cases, the gate groupings on the platter bear the same spatial relationships both within themselves and to other groupings as do the gates on the logic diagrams. This presupposes that reasonable care has been exercised in "laying out" the original logic for maximum clarity and visibility of data and control paths. This high correlation between hardware layout and data and control signal flow also facilitates testing of the completed platter.

Routing is physically done by sketching on plastic overlays superimposed over a reference print containing a field of flatpack mounting pads. These pads, corresponding to the 14-leads of the integrated circuit package, are arranged on a grid consistent with the packing density and channel wiring space required. As a design aid, the two layers of interconnects are visually separated either by color coding or by employing several overlays.

LIMAC needs but two wiring layers—one on each outer surface of the platter. A ground plane interposed between the two outer wiring layers provides the required ground shield necessary for transmission strip-lines. This ground shield additionally serves as the power ground return. Since current mode logic is employed exclusively, switching transients on the ground plane are minimal.

The integrated-circuit flatpacks are surface soldered to the top surface of the platter. This surface contains, for the most part, only data-flow signal wiring placed into from four to seven channels per "avenue" and up to six channels per "street". The term "avenue" refers to the space reserved for wiring runs between columns of flatpacks; "street" refers to the space for wiring runs between rows of flatpacks. The top surface of the LIMAC adder board (Fig. 3a) illustrates the predominant use of avenues for data signal wiring.

Control signal wiring is restricted to streets of up to nine channels on the back surface of the platter. Power supply voltage busses and additional ground straps for redundancy, also on the back surface, run parallel to the control wiring. The back surface of the adder board (Fig. 3b) illustrates the use of streets for control signal wiring. The broad parallel voltage busses are clearly visible. Plated-through via-holes connect wiring on one surface of the platter to wiring on the other.

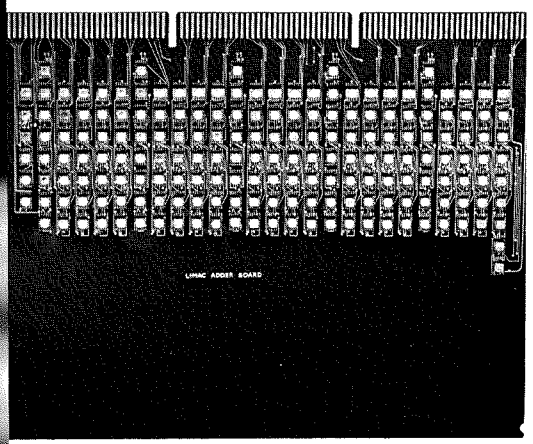


Fig. 3a—Adder board, top surface.

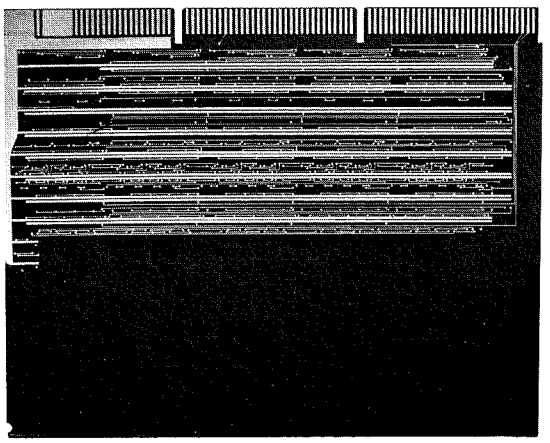


Fig. 3b—Adder board, bottom surface.

The time-sharing system

Plastic overlays, containing all the required routing information in sketch form, are used to directly enter data into the time-sharing system via a Teletype keyboard. This is possible because

the wire routing is restricted to previously defined channels and because a simple command language and symbolic notation, CTRANS, can be used to define the entire routing scheme. (CTRANS, the source program language used with the time-sharing system for the design of LIMAC, is discussed in detail later in this paper.) Direct entry eliminates the time-consuming and error-prove steps involved with the conventional use of coding sheets.

The wire-routing data is then processed in time-sharing according to CTRANS and another program called PREP.[3] PREP is a FORTRAN program that generates the commands necessary to drive the display apparatus. PREP is also used again, later in the design cycle with the RCA 601/301 computer, to generate the paper tape that directs the Gerber Coordinatograph in producing the final artwork.

The simple and inexpensive display system involving the MODEL T apparatus[4] and a storage oscilloscope, or *X-Y* plotter, provides the graphic feedback required for artwork program debugging.

Experience with the MODEL T display, in conjunction with time sharing, has demonstrated its value as a design aid. With a typical source program involving the placement and interconnections of 10 to 15 flatpacks, several programming errors are bound to occur. The graphic feedback obtained with the MODEL T and time-sharing permits the rapid identification and correction of errors. Debugging is readily accomplished at a high level of programming language and at a low level of layout complexity using relatively unsophisticated apparatus.

CTRANS

CTRANS is a FORTRAN program that accepts symbolic code on a time-sharing computer system and then translates this code into a form that can be further processed by PREP. CTRANS permits the operator to input graphic data easily and efficiently. CTRANS also allows the operator to store and ultimately link together the debugged small elements of artwork programs into one full-size master program.

In the CTRANS language, graphic data is entered in terms of pin and flatpack identifying notations. The time-sharing computer keeps track of the type and dimensions of several varieties of flatpacks and computes the actual position coordinates for a given symbolic designation. These coordinates are written on a binary file that is then processed by PREP to generate the plotter or oscilloscope display.

To illustrate the structure and use of CTRANS, a simple program was written. This program, SAMPLE, is shown in Fig. 4. A table of some of the more useful CTRANS commands is given in Fig. 5 for reference. The SAMPLE artwork (drawn by the Gerber Coordinatograph) corresponding to this source program is shown in Fig. 6.

Most of the commands of CTRANS are straightforward. Their use should be readily understood by studying the comments adjacent to each statement in the SAMPLE program. As can be seen from this example, CTRANS simplifies the specification of placement and routing but does not directly help in the planning prior to programming.

As discussed previously, the platter routing and placement data is programmed by creating separate files; each file represents an interconnected grouping of 10 to 15 flatpacks. When all the required files for a given platter have been created and separately debugged, they are then combined or linked into a single program. This composition is, in most cases, too lengthy and complex to be displayed for final debugging using the time-sharing and MODEL T system. For example, a complete platter program typically requires upwards of 80,000 words (36-bits/word) of memory.

```
00010  @  01     1X1Y1                  :DEFINES TYPE (01) & LØC. (1,1) ØF #1
00020  @R 01     1XY.625R5              :DEF. FP. #2-#6, WITH REPEAT 0.625
00030  1AU       X1Y1                   :ØN TØP LAYER. MØVE PEN UP TØ (1,1)
00040  L         X.00011Y-.00011        :LIBRARY CALL, .00011 TØ-.00011
00050  L         X.00041Y-.00041        :LIBRARY CALL
00060  1SU       10P50F2                :MØVES, PEN UP, TØ PIN 50 ØF FP #2
00070   R        11X.00011Y-.00041R1    :REPEATS INS. .00011 TØ-.00041
00080   R        X10Y11R1               :REPEATS INS. FRØM 10 TØ 11
00090  1SU       P5F2                   :MØVES, PEN UP, TØ PIN 5 ØF FP #2
00100   S 30     P11F1                  :DRAW WTH AP. #30 TØ PIN 11 ØF FP#1
00110   SU       P7F1                   :MØVES, PEN UP, TØ PIN 7 ØF FP #1
00120   J        C44F1                  :DRAW HØRIZØNTAL LINE, AP. #30, TØ---
00130   X                               :---CHANNEL #44 ØF FP #1
00140   J        P8F3                   :DRAW VERTICAL LINE, AP. #30, TØ---
00150   Y                               :---"Y" PØSITION ØF PIN 8, FP #3
00160   S        P8F3                   :DRAW WTH AP. #30 TØ PIN 8 ØF FP #3
00170   SU       P1F2                   :MØVES, PEN UP, TØ PIN 1 ØF FP #2
00180            XØY-.025               :DRAW VERT. LINE -.025 INCHES
00190  C F97                            :FLASH ØN BØTH LAYERS WITH AP. #97
00200  2J 30     P7F2                   :DRAW HØRIZ. LINE, AP. #30, ØN---
00210   X                               :---BØT. LAYER TØ "X" PØS. ØF P7F2
00220  C F97                            :FLASH ØN BØTH LAYERS WITH AP. #97
00230  1S 30     P7F2                   :DRAWS, TØP LAYER, AP. #30, TØ P7F2
00240   SU       P50F4                  :MØVES, PEN UP, TØ PIN 50 ØF FP #4
00250  L                               :LIBRARY CALL, CALLS UPØN PRØGRAM---
00260  FLIP                            :---NAMED "FLIP", PREVIØUSLY DØNE
00270  @  01     5X1Y3.75               :DEFINES TYPE (01) & LØC. (1,3.75)
00280  @  01     6X1Y3.75               :AS ABØVE
00290  DØ 07     20                     :DØ CØDES FRØM HERE TØ INS. 20, 7 X
00300  1SU30     P8F4                   :MØVES, PEN UP, TØ PIN 8 ØF FP #4
00310   S        P7F5                   :DRAWS, TØP LAYER, AP. #30, TØ P7F5
00320   J        C44F6                  :DRAW HØRIZ. LINE, AP. #30, ØN---
00330   X                               :---TØP LAYER TØ CHANNEL #44, FP #6
00340  @A        4X-.05Y                :INCREMENT PØS. ØF FP #4 BY (-.05,0)
00350  @A        5X-.05Y.035            :INCR. PØS. ØF FP #5 BY (-.05,.035)
00360  @A        6X.035Y0               :INCR. PØS. ØF FP #6 BY (.035,0)
00370            20XY-1.5               :DRAWS INCREMENTALLY FRØM PRE. PØS.
00380  CE                              :END ØF PRØGRAM
*
```

Fig. 4—Sample CTRANS program.

3 CHARACTER CODE			COMMENTS
@			PLACEMENT OF SINGLE FLAT-PACK
@	R		PLACEMENT OF GROUP OF FLAT-PACKS, EVENLY SPACED
@	A		CHANGE PLACEMENT OF GIVEN FLAT-PACK
L			CALL LIBRARY PROGRAMS OR STORED FILES
D	D		DEFINE RELATIVE LOCATION OF PIN FOR FLAT-PACK TYPE
D	ø		PROCESS A SEGMENT OF CODE N TIMES
I	F		CONDITIONAL TRANSFER
1			LAYER 1 INSTRUCTION
2			LAYER 2 INSTRUCTION
C			LAYER 1 & 2 INSTRUCTION (COMMON)
	S		COMPUTE X & Y CO-ORDINATES FROM PIN-FLATPACK NOTATION
	J	}	COMPUTE X & Y CO-ORDINATES FROM PIN-FLATPACK NOTATION
	"b"	}	AND ADD THE INCREMENTAL VALUE ON THIS LINE
	J	}	COMPUTE X CO-ORDINATE FROM PIN-FLATPACK NOTATION
	X	}	AND ADD THE X INCREMENT TO DRAW HORIZONTAL LINE
	J	}	COMPUTE Y CO-ORDINATE FROM PIN-FLATPACK NOTATION
	Y	}	AND ADD THE Y INCREMENT TO DRAW VERTICAL LINE
		F	FLASH AT THE END OF MOTION
		U	PEN UP
		"b"	"BLANK", PEN DOWN
	A		ACTUAL X & Y CO-ORDINATES
	C		CIRCLE PLOT
	B		BLOCK-RECTANGLE PLOT
	G		GOTO - PERFORM LABEL N NEXT
	R		REPEAT SAME MOTIONS N TIMES
	E		END OF PROGRAM

Fig. 5—Commands of CTRANS.

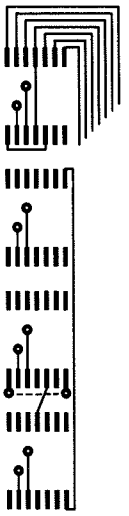


Fig. 6—Sample coordinatograph artwork.

To circumvent this problem, the output files created by CTRANS are read out in punched cards. These cards are then batch processed using the PREP program on the RCA 601/301 computer system to generate punched paper tapes for controlling the Gerber Automatic Coordinatograph. The tapes generated (one for each piece of artwork) are typically on the order of two thousand feet long.

Platter artwork display

Another display system, involving an RCA Spectra 70/25 processor controlling a large screen CRT display, is used for debugging the completed platter artwork program. This display system includes, in addition to the Spectra 70/25, a Teletype, a paper tape reader/punch, and a disc storage unit. The Spectra processor is used to periodically refresh the CTR in addition to controlling the I/O peripherals and performing computations. A photograph of the platter artwork display apparatus is shown in Fig. 7.

The Gerber Coordinatograph paper tape is punched in 8-level EIA standard code and consists of a sequence of blocks that are alphanumeric characters as delimited by end-of-block symbols. Each block is formed by words designating the incremental values, in inches, of the drawing motion for the block plus a specification of the aperature code for the Gerber light head. WRENCH, a Spectra 70/25 assembly language program for graphic display and manipulation, decodes the Gerber paper tape, converts increments to absolute coordinates, scales the image to the proper size grid, and then displays the result on the CRT. New data is written in over old display data by WRENCH to prevent objectionable flickering as the number of displayed vectors accumulate beyond 2000. Thus, only a portion of the platter image (that containing 2000 vectors) is visible at one time without introducing flicker. Since the total number of vectors per platter layer is typically about 10,000, that portion which is visible represents approximately 20% of the platter artwork. To be able to view the entire platter image simultaneously, a camera is used to accumulate the separate images.

Errors that are detected by means of this display can usually be corrected by either patching the paper tape, in the case of mis-punched holes, or by re-running the artwork program on the RCA 601/301 with corrected punched cards and generating a new paper tape. A piece of artwork that might require 10 to 12 hours to run on the coordinatograph can be checked with this display system in 10 to 12 minutes. Since the display "draws" the image in the same sequential fashion as does the coordinatograph, rapid identification of that portion of the paper tape containing errors is possible. Mis-punched sprocket holes, for example, are especially easy to identify.

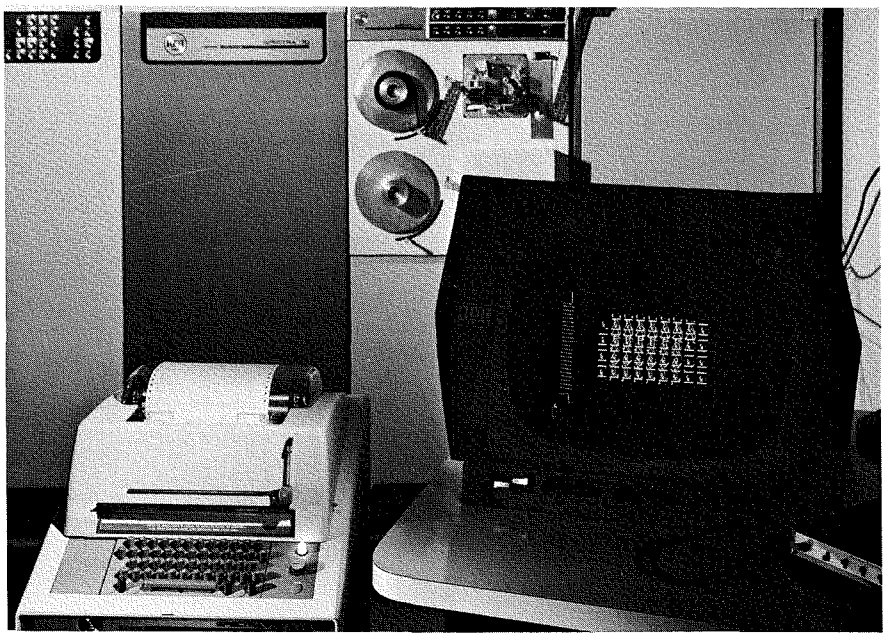


Fig. 7—Spectra 70/25 graphics display.

When all errors that can be detected by means of the display are corrected, the paper tapes are submitted for runs on the coordinatograph. Two tapes per platter are required—one for each wiring plane. The tape for the back wiring plane is also used to obtain the artwork for the center ground plane. This is accomplished simply by running "light-off" on all non-flashed aperture instructions and substituting the desired aperture for the flashed instructions. (A flash instruction is used to imprint a via-hole or pad image on the photographic film.) Thus, from these two reels of paper tape, the set of three glass photomasters corresponding to the front, back, and center ground planes is obtained.

Fig. 8 shows a sample of LIMAC platter artwork produced by the coordinatograph. This is a reduced size copy of the original glass master for the top plane of the LIMAC register board.

PAD—a drill tape program

A 601 FORTRAN program, PAD (Programmed Automatic Drilling), was written to generate punched paper tapes for the automatic drilling of all feed-through or via holes in LIMAC platters. The PAD program reads data written on a scratch tape by PREP. It selects from this tape instructions that call for flashes with the given set of aperture numbers corresponding to those locations where holes are to be drilled. The coordinates of these flashes are rounded off to the nearest thousandths of an inch in absolute values and then are punched in EIA code using a fixed word-length format. Reels of punched paper tape are grouped in length to that required to drill 2000 holes. This is done primarily for convenience in handling by avoiding excessive tape lengths.

Conclusions

The choice of packaging scheme adopted for LIMAC was influenced by a number of interrelated factors associated with the application of large-scale integrated array technology to computers. The LIMAC organizational concepts, coupled with large-platter packaging, resulted in significant improvements over conventional

machines. For example, LIMAC easily achieved a 5000-gate/ft^3 packaging density before inclusion of arrays. LIMAC required only two-layer printed circuit boards instead of the 4 to 6 layers of signal wiring projected for a 5000-gate packaging density following Spectra 70 organizational concepts.

The computer-aided design techniques described in this paper have proven exceptionally useful. However, they represent only an interim evolutionary step at best. Computer programs such as CTRANS, that were developed as an aid in designing LIMAC platters were oriented toward a very particular goal, that of generating artwork for large printed circuit boards. However, it is evident that this programming approach could be extended into other more important areas such as artwork generation for large integrated-circuit arrays. In this context, it is clear that computer graphic techniques, such as those discussed in this paper, would permit a higher level of computer-aided interactive design than can now be obtained. Such techniques would expand the creativity of the designer while minimizing his errors. Interaction of the graphics computer in the artwork design process will, no doubt, prove to be an economic imperative as the industry progresses from present levels of integration to the still higher levels entailed in large-scale integration.

Acknowledgment

The authors wish to extend their appreciation to H. S. Miiller who was largely responsible for the system organization of LIMAC and to S. E. Wood and N. K. Kudrajashev for their contributions in the fabrication of LIMAC printed circuit platters.

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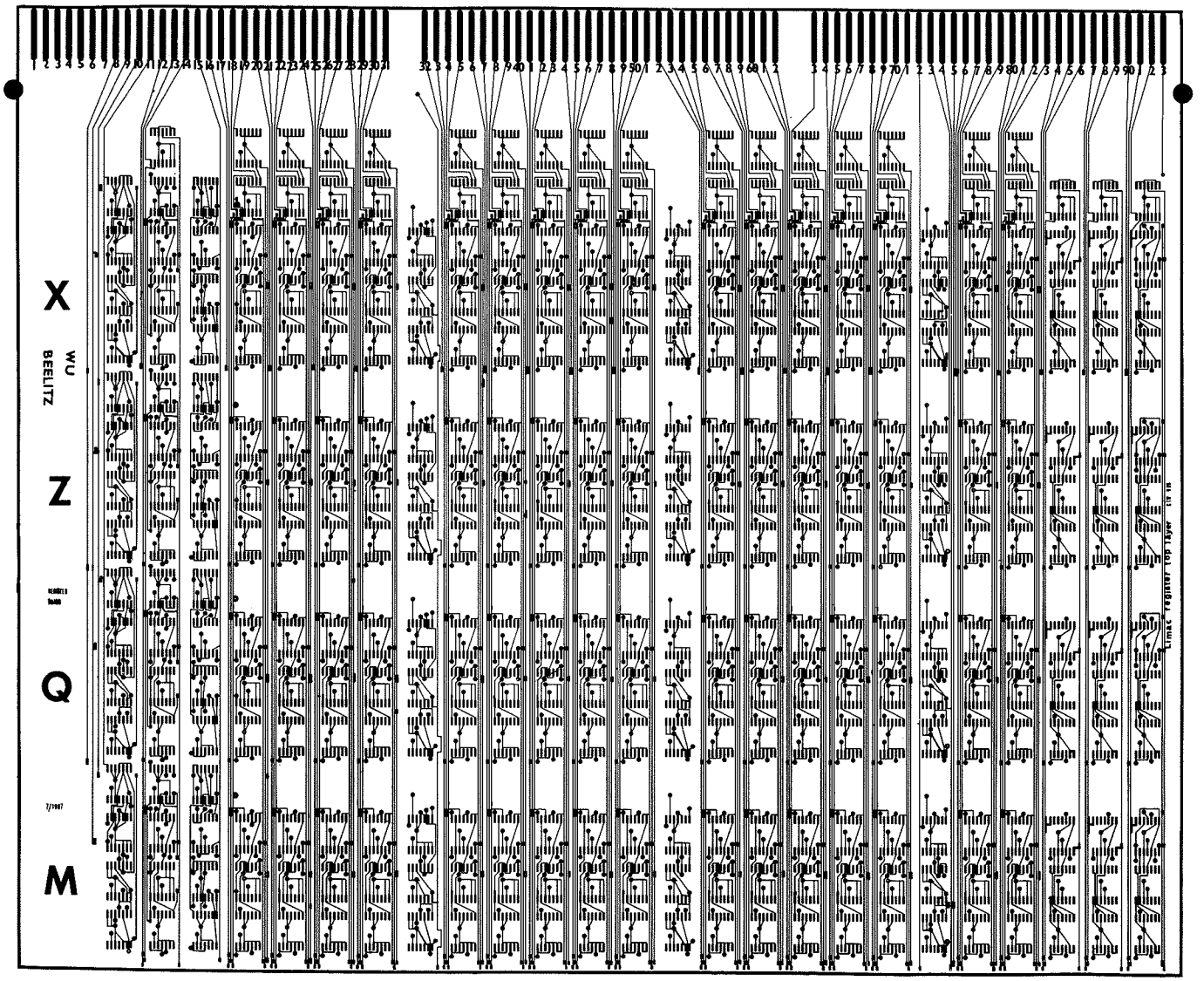

Fig. 8—LIMAC platter artwork.

A partitioning algorithm for design automation

J. Smiley

This paper describes a partitioning algorithm which is a key part of the LBPR computer program. This program, written for DCSD's Design Automation Programming Activity for use on the Spectra 70 Computer, requires a field of logic, logic circuits, and their interconnections to be grouped or sectioned into predefined functional units. The algorithm discovers the logic grouping and redefines the group as a functional unit type and assigns pin numbers to the interconnections between units.

THE LBPR PROGRAM is an input translation program. It converts input data from a logic simulation program into input data for an integrated-circuit layout-design program.

Background to LBPR program

Various design automation software programs have been written to aid the engineer in his design function. They include backplane platter design, wire list generation, logic simulation, automatic-test generation, flow-chart generation, and integrated-circuit-chip-layout design. Each of these programs requires a specialized input which must be reworked to use it with another program.

The LBPR program allows a user of the logic simulation program to use the IC-chip-layout design program with no additional input. The program describes groupings of elementary logic circuits (e.g., gates and inverters) as more complex logic circuits (e.g., JK flip flops).

Logic simulation program

This program, whose input is used by the translation program, simulates a logic configuration in the computer and exercises it according to user specifications. The logic simulation program output includes a timing chart which illustrates the behavior of the logic elements as a function of time. The program input contains the logic element types, their connectivity (how the logic is interconnected), how the inputs vary with respect to time, the clocking and generation signals, and rise and fall delay. The current program can manage 1000 circuits.

Integrated-circuit-layout design

This program, whose input can be generated by the LBPR program, accepts logic connectivity information and develops a layout of the logic for the construction of the logic on an integrated-circuit chip. The output of the integrated circuit layout design includes magnetic tape to generate masks for an IC chip via a Gerber plotter. In this paper, logic circuits for use with the IC-chip-generation program will be called *cells*. A chip contains approximately 150 cells. Some of the cells are complex logic circuits and consists of up to 8 elementary logic circuits.

A cell composed of more than one elementary logic circuit generally takes less space on the chip than several cells each containing only one elementary logic circuit implementing the same logic fuction. Thus, it is desirable to have the cells as complex as possible for a compactly designed chip. To avoid a faulty chip, it is desirable to perform the logic simulation program on a chip layout design to test its performance prior to producing it. A simulation assures against gross logic errors.

LBPR program operation

The LBPR program, in addition to translating the input data for a logic simulation to the input data for the chip generation program, does the following functions:

1) Evaluates the logic simulation input data for proper format. If the format is improper, the program prints out diagnostic information in addition to the erroneous input data.

2) Searches through the input data to see if the elementary logic circuits can be described as more complex logic circuits. If some can, the logic circuit or cell in question is further described by assigning numbers to the external cell connections, and assigning a cell type number and a serial number (each cell has a unique number). Eventually, all the logic circuits will be described as cells with some more complex than others.

3) Checks the cell loading (the number of circuits connected to its output) and, if overloaded, redescribes the logic circuit or circuits as a different type of cell or cells.

4) Assigns to all unspecified pins, a connection to a chip pad for external connections. (The IC-chip generation program requires that all of the output and input connections to the chip be specified).

5) Lists all logic circuits as they were defined by the logic simulation input including the cell type and serial number assigned to it. If the logic circuit was redescribed as a part of a more complex logic circuit, a circuit number is also listed. This allows the user to understand the action taken by the program.

6) Generates the entire input for the IC-chip-generation program. (The input connectivity resembles wire lists).

LBPR program description

The program contains an input, a processing, and an output section. The input section reads in the connectivity

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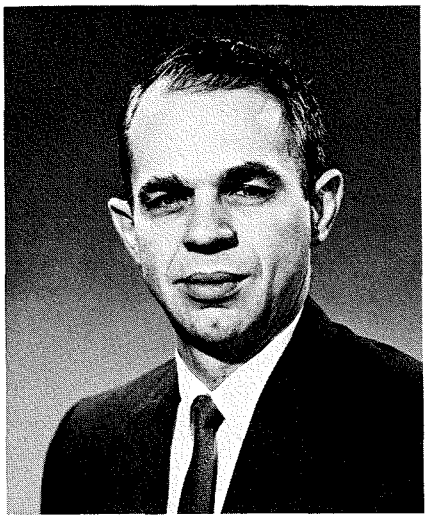
Final manuscript received August 2, 1968.



John Smiley
Commercial Program Planning
Defense Communications Systems Division
Camden, N.J.
received the BSEE from Lafayette College in 1952 and has done graduate work at the University of Pennsylvania and Rutgers. Mr. Smiley joined RCA in 1953 and was assigned to Digital Application Engineering where he was involved in logic design and developments of the AN/GRA-5, the T/SEC KW-7, and the MICROPAC computer. For the past four years, Mr. Smiley has been engaged in software development. He has written several technical papers and is a member of the IEEE.

information and organizes it into a logic-circuit field assigning a code to each circuit. The output section extracts the input required for the IC chip generation program. The processing section searches the logic circuit field to see if the logic circuits can be described as more complex logic circuits, and assigns all circuits a cell description.

The design of the processing section at first seemed to be voluminous with a separate routine to search for each different cell type among the field of logic circuits. Then an algorithm was developed using a general routine and a cell criteria table.

Partitioning algorithm

Each cell is described in coded form in a cell criteria table. This table has at least one entry per circuit in the cell. Each entry contains

1) A coded description of a circuit in the cell;
2) Where the program should go if there is a mismatch between the circuit and the criteria; and
3) Where to jump to in the table for the next matching attempt.

A flow chart of the algorithm is shown in Fig. 1.

The cell criteria table starts with information describing the most complex logic circuit and ends with a description of an elementary logic circuit. Fig. 2c shows a portion of a typical cell criteria field.

Each logic circuit in the logic-circuit field has a code assigned which describes it functionally:

abcd

where $a=1$ if circuit has no delay from input to output, or $a=0$ if circuit has delay (a no-delay situation would be a phantom-OR circuit); $b=$number of inputs to the logic circuit, including clocking signal; $c=$circuit type code (see Table I); and $d=0$ if no clocking signal, or both; $d=1$ if first clocking signal (Phase 1) and $d=2$ if second clocking signal (Phase 2).

The search for a cell type starts by pointing to the beginning of the circuit field to the first entry with a one in the available (A) column, (e.g., EBB8 in Fig. 2b), and to the beginning of the cell criteria table (e.g., 1. 0352001 in Fig. 2c).

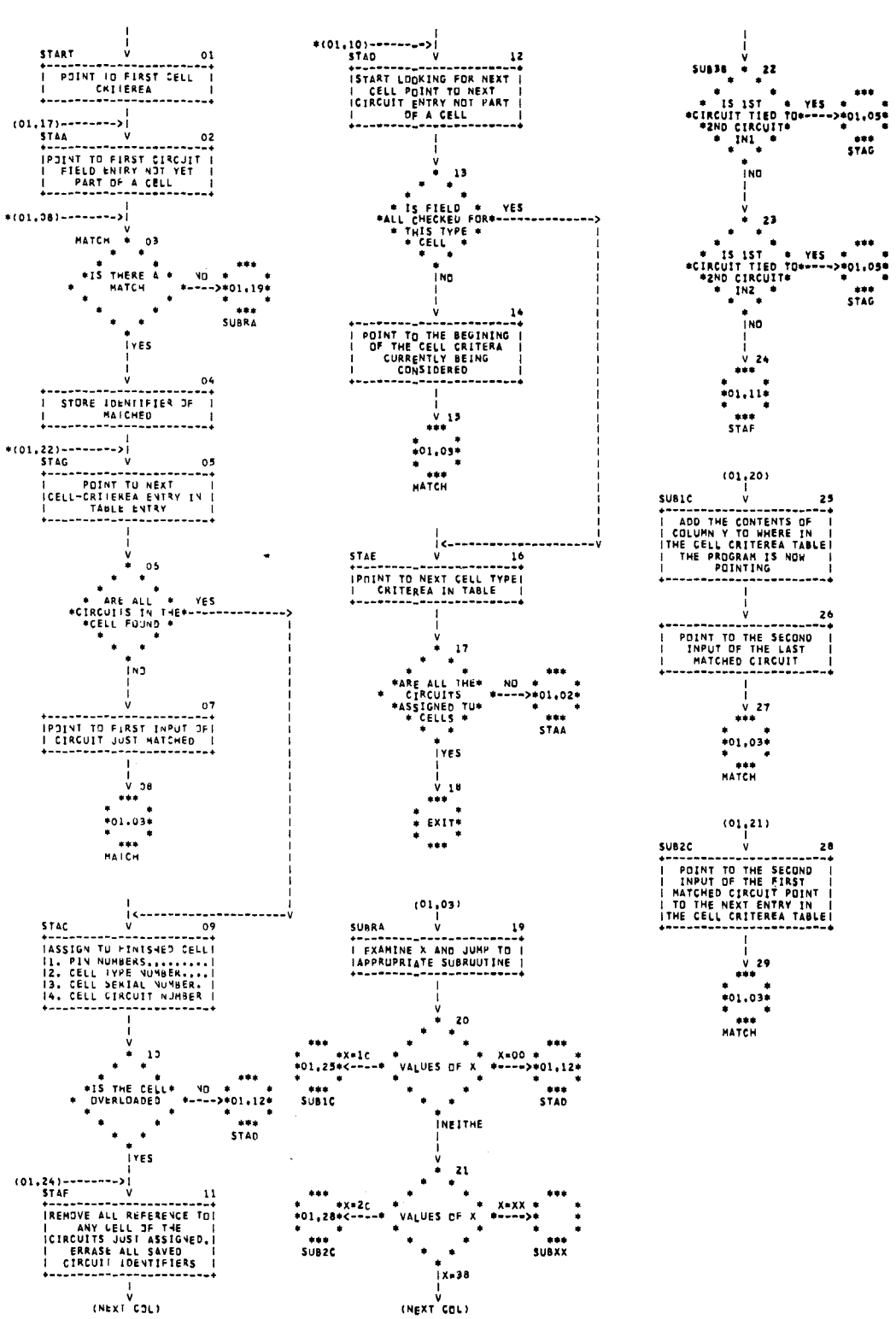
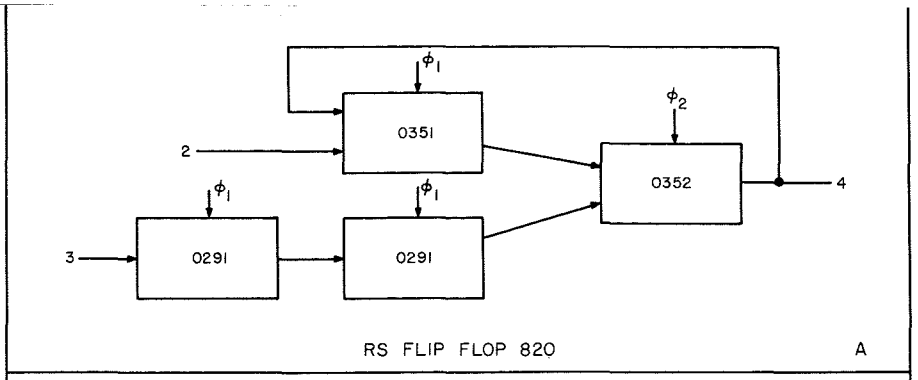


Fig. 1—Flow chart of the partitioning algorithm used to search for cells.

If the c portion of the cell criteria matches the code portion of the circuit field, the circuit identifier is stored. The program then points to the next cell criteria and the entry in the circuit field which is the first input of the last matched circuit (e.g., in Fig. 2b, if EBB8 were matched then the program would point to EBE0). This procedure repeats until a cell is complete or a mismatch occurs.

If a mismatch occurs, the x portion of the cell criteria points to a subroutine which must be performed before another matching attempt. See Fig. 1 for specific examples of these subroutines.

When a cell is complete, indicated by the y portion of the cell criteria having the value 02, the program assigns the following information to all the circuits whose circuit identifiers have been stored:



RS FLIP FLOP 820 A

IDENTIFIER	TYPE	A	CODE a b c d	INPUT 1	INPUT 2	INPUT 3	PIN #
			—	—	—		
EBB8		1	0 2 9 1	EBE0	0240		
EBE0		1	1 2 0 0	ED48	EC80		
EC08		1	0 2 9 1	EBB8	D240		
EC30		1	0 3 5 1	EC58	EF50	D240	
EC58		1	0 3 5 2	EC08	EC30	D268	

LOGIC CIRCUIT FIELD B

	C	X	Y		C	X	Y
1.	0 3 5 2	0 0	0 1				
2.	0 3 5 1	1 C	1 8	8.	0 3 5 1	0 0	0 0
3.	0 0 0 3	2 C	0 0	9.	0 0 0 3	2 C	0 0
4.	0 2 9 1	0 0	0 0	10.	0 2 9 1	0 0	0 0
5.	0 2 9 1	0 0	0 0	11.	0 2 9 1	0 0	0 0
6.	0 0 0 5	3 8	0 0	12.	0 0 0 5	3 8	0 0
7.	1 2 3 4	0 2	0 2	13.	1 2 3 4	0 2	0 2

CELL CRITERIA TABLE
(PORTION CONTAINING RS FLIP FLOP CRITERIA) C

Fig. 2—Sample problem: A) an RS flip-flop, B) input logic circuit information; C) portion of cell criteria table.

1) Appropriate pin numbers to the pin-number column of the circuit field.
2) Cell type number, (the c column of the cell criteria table is inserted in the type column of the circuit field).
3) Cell serial number and circuit number is inserted as part of the type column of the circuit field.
4) 0 in the A column of the circuit field indicates that the circuit has been already assigned to a cell.

Sample problem

A sample problem illustrating how the program operates is shown in Fig. 2, and the steps the program goes through are shown in Fig. 3. Fig. 2a shows four elementary logic circuits grouped as a complex logic circuit (RS flip-flop). The numbers in each box represent the code numbers assigned to each logic circuit by the program. For example, 0351 is a 3-input MORT gate clocked with the first clock pulse. Fig. 2b shows the input logic circuit information after it has been processed by the input section of the program and organized into the logic circuit field. Fig. 2c shows a portion of the cell criteria table which contains the description of the RS flip-flop.

Steps	*Circuit Field Identifier*	*Table Entry*	*Remarks*
1, 2, 3, 19, 20	EBB8	1	
12, 13, 14, 3, 19, 20	EB0E	1	
12, 13, 14, 3, 19, 20	EC08	1	
12, 13, 14, 3, 19, 20	EC30	1	
12, 13, 14, 3, 4	EC58	1	store identifier EC58
5, 6	EC58	2	
7, 3, 19, 20	EC08	2	
25, 26	EC08	8	
3, 4	EC30	8	store identifier EC30
5, 6	EC30	9	
7, 3, 19, 20, 21, 27	EC58	9	
29, 3, 4	EC08	10	store identifier EC08
5, 6	EC08	11	
7, 3, 4	EBB8	11	store identifier EBB8
5, 6	EBB8	12	
7, 3, 19, 20, 21, 22, 23	EBE0	12	
5, 6, 9, 10, 11	EBE0	13	cell complete
12, 13	EC58+	13	
	EC58+	13+	finished

Note: Step numbers are the box numbers on Fig. 1 (each represents a functional operation).

Fig. 3—Sample program routine.

Table I—Type code

Type code	*circuit*
0	OR
1	NOR
2	AND
3	NAND
4	MOR
5	MORT
6	MAND
7	MANT
8	CFF
9	MOR or MAND (2 input)
A	MORT or MANT (2 input)
B	exclusive OR

The following are some of the steps of the program through the algorithm from Fig. 3:

1) Point to the first table constant in Fig. 2c: 0352 00 01
2) Point to the first circuit field entry not yet part of a cell in Fig. 2b: EBB8
3) Is the code column in EBB8=to C column of table? Is 0291=0352? NO, GO TO ROUTINE 00 (Routine 00 goes to step #12).
12) Point to the next circuit entry not yet a part of a cell in Fig. 1B: EBE0
13) Have all circuits been tried? NO.
8) Back up table to beginning of cell criteria: 0352 00 01.
3) Is the code column of EBE0=to C column of table? Is 1200=0352? NO, GO TO ROUTINE 00

The rest of the steps are left to the reader.

Shortcomings in the program

The cell file is not easily entered into the program. This brings up the problem of allowing the user to change the internal files of the program. An enhancement would allow the user to insert cells of his choosing into the internal files for his run only.

The geographic positioning of the cells is not considered. A modification would position the cells in some predefined pattern (backplane layout considering lead length between the cells.

Summary

The partitioning algorithm could be used to automatically group or partition logic into card types. It would allow a logic designer to change his logic without his being overly concerned about repartitioning.

Marketing for research

Dr. J. Kurshan

Research Marketing provides the interface between the government and the research staff at the David Sarnoff Research Center and coordination between RCA Laboratories and the product divisions, both on company-supported work and on joint-contract programs. Each contract award is the culmination of careful planning and activity that may take one to two years to reach fruition. A better understanding of the contract environment and how Marketing functions will assist research scientists and engineers in achieving the program objectives.

Dr. Jerome Kurshan, Mgr.
Marketing
Research and Engineering
Princeton, N.J.
received the AB (with honors in Mathematics and Physics) from Columbia University in 1939 and the PhD in Physics from Cornell University in 1943. He was an Assistant in Physics at Columbia University in 1939 and at Cornell University from 1939 to 1943. Dr. Kurshan joined RCA Laboratories in 1943, where he has conducted research on electron tubes and semiconductor devices. Sixteen U.S. patents have been issued in his name. He has served as Mgr., Graduate Recruiting; Mgr., Technical Recruiting and Training; Mgr., Employment and Training; and Mgr., Research Services Laboratory. He was appointed to his present position, Mgr., Marketing, Research and Engineering, in 1966. Dr. Kurshan is a senior member of the IEEE, and a member of the American Physical Society, Phi Beta Kappa, Sigma Xi, Phi Kappa Phi, and Pi Mu Epsilon.

BASICALLY, Marketing is the interface between the producer and the customer. In a broad sense, this can cover market research, systems analysis, product planning, advertising, sales and customer satisfaction. For the research activities at RCA, however, marketing has a more restricted and specialized connotation. Although Research Marketing has a major responsibility of securing government-contract support for a portion of the research program, it must be stressed that RCA has one primary customer for its research output—its product divisions.

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In the Laboratories, government-supported work is not an isolated segment of the research activities, but a continually changing cross-section of the total research effort. Thus, Marketing is a close associate of the research staff and management of the Laboratories, working with them on specific contract opportunities and contributing to the information and decision-making processes that guide the total research program.

The Research marketing activity also has important interaction with the product divisions. By formal arrangement, marketing services are provided to some of the Affiliated Laboratories located at the David Sarnoff Research Center.

RCA Laboratories also benefits from this because of (1) the coordination that this marketing activity affords with marketing for the Laboratories; (2) the added awareness of product-division needs, and (3) the assistance in transferring research results to the divisions. Outside the Affiliated Laboratories, Research and Engineering Marketing has worked directly with counterparts in the product divisions on government-funded joint programs such as the Gallium Arsenide Laser and Thermoelectric Materials programs.

Why government contracts?

For the average Member of the Technical Staff, the most direct contact with marketing is at the working level of obtaining and then working on a government contract, monitored by one of the government research laboratories which is able to support some of our research efforts.

The benefits that RCA Laboratories derives from government contracts can be summarized as follows:

1) The opportunity to undertake additional high-risk research.
2) A competitive evaluation of research results.
3) The ability to support a larger Technical Staff.
4) Government support for transfer of research results to product divisions.
5. Access to government information sources.
6. Assessment of technological trends.
7) Discipline in defining and expediting objectives.

Of course, there are disadvantages to government-supported research, but the advantages outweigh the disadvantages. The greatest hazards are the possibilities of diverting commercial research objectives and of granting excessive commercial rights to the government. Marketing shares a responsibility with research management to avoid these hazards and is continually and actively concerned with them.

There are other obligations imposed by government contracts that are considered normal and acceptable; they are discussed below.

Government support of R&D

The role played by the government is indicated in Fig. 1, which gives trends in federal spending for research and development. The actual expenditures for 1968, when published, will be about $16.5 billion, just under 2/3 of the total United States expenditures for R&D of $26 billion. (Federal spending for R&D is about 9% of the total federal outlay of $180 billion for fiscal 1968.) The Laboratories competes for only a fraction of the research-category

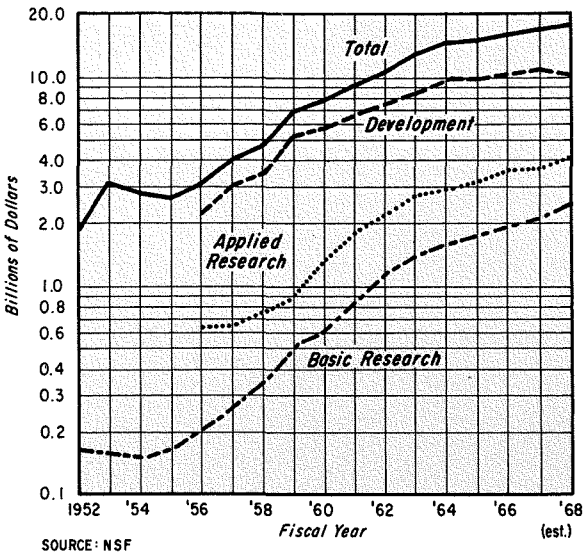


Fig. 1—Trends in Federal obligations for research and development.

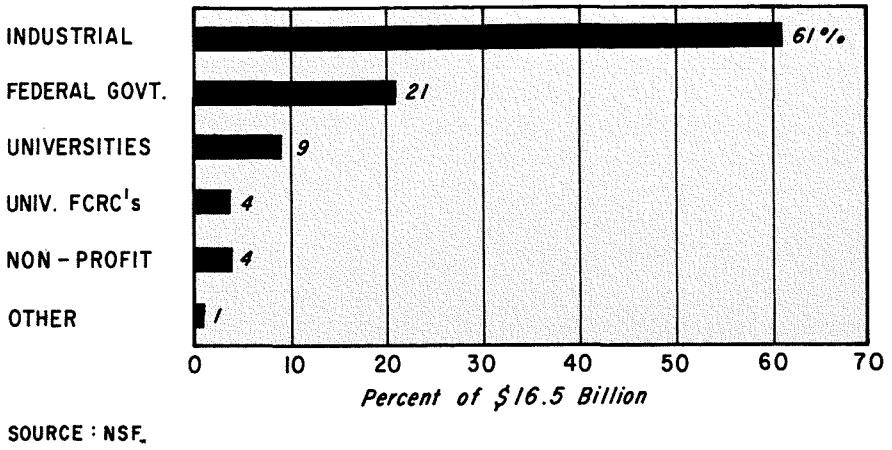


Fig. 2—Distribution of Federal obligations for R and D (by performer—FY 1967).

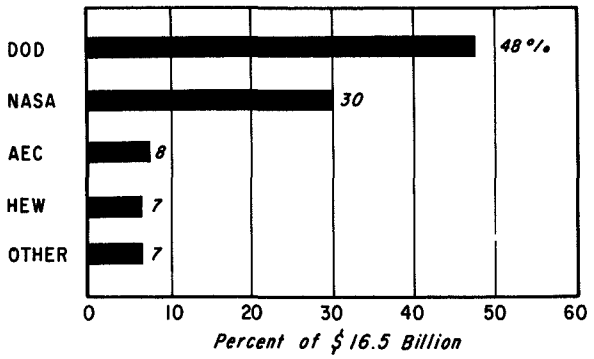


Fig. 3—Distribution of Federal obligations for R and D (by agency—FY 1967).

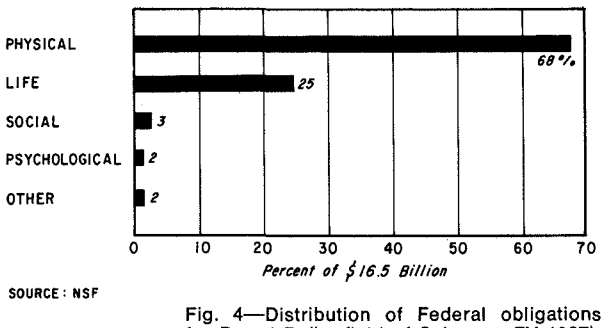


Fig. 4—Distribution of Federal obligations for R and D (by field of Science—FY 1967).

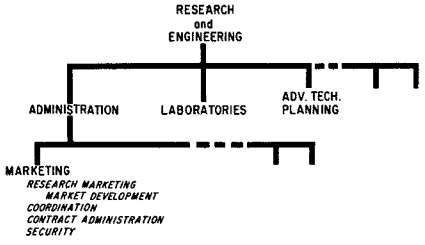


Fig. 5—Marketing in the Research and Engineering organization.

money which, in turn, is only a fraction of the total. The share we actually compete for is probably less than $100 million. Nevertheless, the overall trends shown in the published data are significant to us.

The total growth in federal support of research and development has been tremendous over the past dozen years. What has alarmed the scientific community is the slowing down in the rate of growth in the last few years. Between 1956 and 1964, the growth rate averaged 22% per year, but between 1964 and 1968, this rate slowed to an average of 4% per year. Total R&D support stayed about constant in fiscal year 1968 compared with 1967 and was slated for about a 5% increase in 1969 before the $6 billion budget cut imposed by Congress. As this reduced growth rate continues, getting our share of government R&D contracts will become even more of a challenging and competitive task and we must continue to adjust accordingly.

The next few figures break down the Federal R&D obligations for Fiscal Year (FY) 1967, the latest published. Fig. 2 shows the distribution of federal R&D funds by performer. University administered Federal Contract Research Centers (FCRC's) are broken out separately from other University funding. In FY 1967, 61% of total R&D went to industry. Even in research alone, industry received the largest share (32%). Fig. 3 shows the distribution by Government Agencies. The Department of Defense dominates with NASA second. For Research alone, DoD accounted for 33% and NASA 26%, but NASA has suffered large cuts subsequent to FY 1967. Other departments—such as Transportation, Housing and Urban Development, Post Office, and Health Education and Welfare—will continue to get a larger share of research funds. Research contracts with these agencies require special attention to the patent clauses for protection of RCA's commercial interests. Fig. 4 shows that the physical sciences dominate the distribution of funds. Although the psychological and social sciences have been growing at a greater relative rate, they continue to represent only a few percent of the total outlays.

Contract experience at the Laboratories

Contract support (direct cost) was at the $4 million level before the Vietnam war was escalated. In the past few years, Vietnam budget pressures along with DoD selectivity have produced drastic changes in the level of contract awards and the support level has dropped to $3 million dollars. This level of government contract funding is expected to continue in 1969. It is not easy to obtain or maintain this level of contract support in today's environment. Usually, it takes a year or more to generate a new research contract and there is often a gap in the

extension of a continuing contract. Consequently, 50% to 100% more staff have to be involved in contract activities than the number being supported, on the average, through the contracts. In general, Research Marketing seeks contracts that will provide the continuity of renewability. As a result, three years is the normal life for a contract at the Laboratories. However, some research contracts end after one year.

The functions of research marketing

Fig. 5 shows how Marketing, Research and Engineering, fits into the current organizational structure and Fig. 6 gives the names of the key individuals. The activity reports to A. N. Curtiss, Staff Vice President, Administration, Research and Engineering.

Much of the effort of Research Marketing is devoted to Market Development, i.e., the development and realization of opportunities for contract support of research. The Market Development men are the Research Department's key interface with the government agencies and with the marketing activities in our product divisions.

Coordination is another Marketing function listed on the chart. There are various marketing services requiring coordination between the Technical Staff and other activities of the Laboratories. First is proposal coordination. The Marketing Coordinator issues a proposal preparation guide, establishes proposal format, schedules proposal production operations, edits the text and expedites all phases to achieve high quality and timely results. Second, Marketing coordinates responses to the Commerce Business Daily wherein prospective procurements are advertised. The Coordinator reviews this publication, identifies, and refers items of interest, coordinates our response with those of the other divisions, and makes the necessary response for Research and Engineering Marketing to place us on Bidders Lists. Third, Marketing coordinates the write-up of RCA's Independent Research and Development program for a Government Brochure which is the basis for corporate recovery of a pro-rata share of the IR&D expended by the Laboratories.

Contract Administration, another Marketing subdivision, takes care of the infinite detail existing on the administrative side of doing business with the government. Administration is involved in the negotiation of contracts, in determining contract terms and conditions, authorizations for contract effort, meeting requirements, maintaining official contract files, distributing reports, obtaining publication approval, keeping statistical records, closing out completed contracts, etc.

Finally, Security at the David Sarnoff Research Center comes under Marketing because of its tie-in with classified contracts. One of the benefits of contract work is access to classified information on the basis of adequate clearance and a need-to-know. The Master Control function maintains the records necessary to the proper handling of classified material. New employees are briefed on security requirements. They are also given a Security Manual for reference. When one plans to visit another location—government or industrial—to discuss classified information, the Security Office, with prior notice, arranges for a Visitor Clearance to be transmitted to that location.

Government contracts and the technical staff

Some of the *benefits* that government contracts provide for the individual researcher are as follows:

1) The award of a contract for research is a mark of recognition and achievement.
2) It provides an opportunity to clarify objectives and goals.
3) It has a positive influence on research continuity.
4) The contract aids in discipline for greater productivity.
5) Provides for outside evaluation of research.
6) Permits additional participation in the Company's business.
7) Provides for association with key Company and government personnel.

Of course, benefits also imply obligations, and some of these are closely related to the budget cycle for research contracts which will now be reviewed briefly.

The typical research program of $100,000, or less, starts with internal planning at the beginning of the fiscal year in July. Informal submissions are made to the government's Technical Project Monitors and interest is developed well before the calendar year ends. More formal consideration and budgeting occurs during the first half of the new calendar year. Formal Requests for Proposal (RFP) may be issued after the next fiscal year starts and will require a formal proposal response within a specified time (usually 30 day). The actual contract may not be signed on a new program until the last quarter of the calendar year. Thus, a typical contract cycle can take well over a year and can be seriously jeopardized by delays at a number of critical points.

Some of the obligations that government contract activities impose on the researcher are listed below.

1) The researcher is obligated to arouse interest in his work by informal write-up of significant results.
2) To write a winning technical proposal in the time allotted.
3) To supply authorized effort on the contract.
4) To prepare scheduled contract reports.
5) To obtain required publication approval.

Timing, as indicated above, can be critical in the pre-award effort and the researcher must be guided by the requirements set by Marketing. Of course, post-award obligations, such as performance of the work and delivery of reports, must also be met on time. Late proposals are automatically rejected. Late contract reports may be accepted, but adversely affect the negotiation of subsequent contracts, even outside the agency in question. However, expert help is available to the individual researcher, and proposal and report schedules are set to enable typist, reviewer, editor, and printer to do an effective support job.

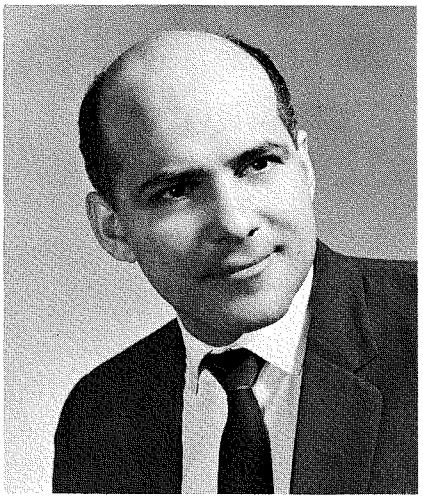
Concluding Remarks

Marketing for Research involves analysis, planning, sales and administration. Research and Engineering Marketing is in partnership with research management, with the technical staff and with the product divisions. This article has emphasized those phases of research marketing that relate especially to the role of the individual scientist or engineer. His understanding of the process should enhance the vital role he plays.

Digital control of Videocomp

S. A. Raciti

Videocomp is a phototypesetting system capable of setting high quality text at very rapid line rates.[1] The paper describes the digital control portion of the RCA 70/832 Videocomp System, and emphasizes that the digital control is a finely meshed software-hardware system.



Salvatore A. Raciti, Ldr.
Product Development
Graphic Systems Division
Dayton, New Jersey
received the BEE from Manhattan College in 1951 and the MEE from New York University in 1960. Prior to joining RCA in 1958, Mr. Raciti spent seven years in the general areas of radar and data processing. In 1960, he became a group leader at Missile and Surface Radar Division at Moorestown where he was responsible for design and development of radar data processing equipment. In 1965 he joined the Graphic Systems Division and is presently responsible for the logic design of Videocomp systems and allied components.

VIDEOCOMP electronically produces typefaces on the screen of a CRT. Letters are generated on the screen and directly transferred to film or photographic paper through a fixed lens system (Fig. 1). At the end of each line of written text, the film or photographic paper is advanced and the next line written.

Beam motion

The CRT produces a fine beam on the screen. The motion used to generate a letter is shown in Fig. 2. For clarity, the vertical lines representing the beam in Fig. 2 have been separated and expanded horizontally. They actually butt to form a flat field while writing characters. During the upstroke, the beam is alternately turned on and off to create the black and white portions of the character. When in its downstroke, the beam is always off. Thus, each character consists of vertical beam strokes made up of segments of black and white; however, the structure is not visible on the film or paper because of the large number of strokes used to generate a single character.

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Size control

Characters of different sizes can be produced by a gain change in both the horizontal and vertical direction by digitally controlling the CRT. Whenever the character size is changed, the beam-spot size and intensity must also be changed to maintain a flat field of light at a constant density. Typeface changes are accomplished by varying the beam on/off pattern, again under digital control.

Digital control

Thus, characters are written by a raster consisting of vertical strokes that contain one or more segments. The black portions of a character are the beam-on segments. The stroking is done in continuous sweeps, which are started and stopped by digital control. Stroke segments are formed by counting time intervals during the sweep period and turning the beam on and off at designated count values. When the last black segment of a stroke is written, the beam is returned to the stroke start line, shown in Figs. 3 and 4. The stroke start line is displaced from the lower CRT aperture edge by the baseline-displacement value. Successive strokes are horizontally spaced by a distance which is under digital control. Fig. 3 defines some of the basic parameters used in defining any text character; Fig. 4 clarifies the scan parameters used in specifying letter generated by the Videocomp.

The Videocomp writes characters in five different size ranges as shown in Table I. Within a size range, a character may be written at eight different point sizes, as indicated. The data that describes a character within a size range is stored in memory. To describe a character of the same shape for all five size ranges, there must be five different files. A complete file for a complete character set is called a font file. In addition, the Videocomp system can write characters at four different resolutions (strokes/em or granularity modes). Table II shows these resolutions as a function of size range.

Vertical-size control

The vertical size of a character may be changed by either changing the vertical sweep rate on the CRT or the counting frequency used to count out the segment lengths stored in font file. Table III shows the actual sweep rates and counting frequencies used as a function of granularity for the RCA 70/830 Videocomp system. These values are selected such that CRT sweep rates and logic counting rates were optimum to achieve highest character writing rates for the Videocomp, commensurate with the state-of-the-art.

Segment length control

The character font file contains data describing the segment lengths within a stroke, whether it is a black or white segment, and whether it is the last black segment in a stroke. Black is defined as that data which creates black images on white paper. This data may be contained in either an eight, ten, or twelve bit format as shown in Fig. 5.

The eight-bit format describes a segment length of 1 to 63 counts; 10 bit, 1 to 255 counts; and 12 bit, 1 to 1023 counts. In general, as the size range increases, the longer formats become more efficient in storage requirements. Segments of the same color can be strung together to create segments of longer length. For a particular font file only one format is used.

The font file data is used by the Videocomp to control the beam start/stop and beam on/off. The font file data is dumped into a set of four counters, called video-ring counters, which are used sequentially end around to control the CRT beam. Before starting any stroke, the video-ring

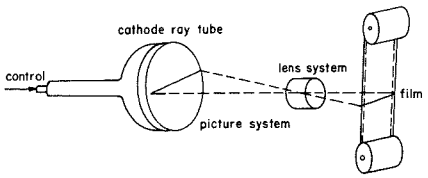

Fig. 1—Videocomp recording principle.

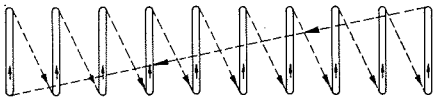

Fig. 2—Beam motion on cathode ray tube.

counters are loaded sequentially from memory until an end-of-stroke bit is encountered or the counters are completely filled. If the stroke contains four or more segments, the counters are completely filled. A CRT scan is not started until the end-of-stroke bit is encountered or the video-ring counters are completely filled. When the scan is started, four microseconds are allowed for the sweep to become linear. At the end of this linearity period, down counting of the first video-ring counter is started at the selected counting frequency. If the color bit indicates white, the beam is left off. If it indicates black, the beam is turned on. When the first counter is depleted to zero, counting is switched to the second counter. If there are additional segments in the stroke beyond four, memory is accessed to fill the first counter. The beam is left on or off as indicated by the color bit. When the end of stroke bit is encountered and its associated video-ring counter is depleted to zero, the scan is stopped and the CRT beam is retraced. During the retrace interval the video-ring counters are filled for the next stroke. This sequence continues until the last stroke is generated.

Horizontal Beam Position Control

A horizontal register (with its associated horizontal counter) controls the horizontal beam position. Before a character is generated, the horizontal register and horizontal counter are preset to the desired horizontal location of the character on the face of the CRT. The horizontal counter is bidirectional allowing generation of right-reading or wrong-reading text copy. During the 4-μs linearity interval, the horizontal counter is updated to the next beam position. During the retrace interval, the contents of the horizontal counter are transferred to the horizontal register. In this manner each time a stroke is started, the beam is at the next stroke position.

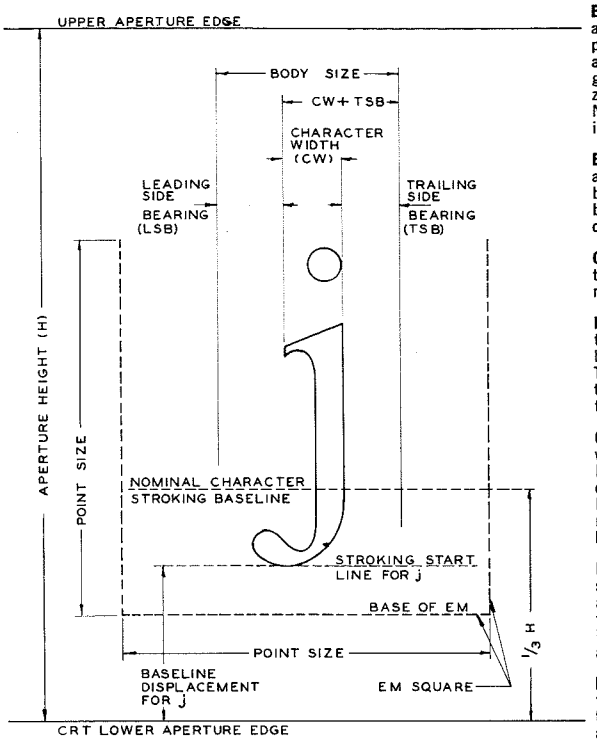

Fig. 3—Basic ingredients in the makeup of a text character.

EM square: a square whose dimensions are equal to the font size in points. A printers point is approximately 1/72 of an inch. For the Videocomp, scanning granularity is defined in terms of horizontal and vertical increments per em. Nominally, the width of the character **M** is equal to the width of the em square.

Body size: is the total width of the character body (character width-leading side bearing + trailing side bearing). Side bearing is the white area on either side of the character.

Character width: the maximum horizontal dimension of the character, including no completely white area on either side.

Leading side bearing: the distance from the leading (left) edge of the character body to the leading edge of the character. **Trailing side bearing:** the distance from the trailing (right) edge of the character to the trailing edge of the character body.

Character baseline: the nominal line on which characters sit to form the visual line of printed text. It is usually coincident with the bottom of capital letters. For reasons of styling, some part of rounded and pointed characters may be below the nominal baseline position.

Nominal character stroking baseline: since all type faces have a decender-to-ascender ratio that does not exceed 1/3, the nominal character stroking baseline is 1/3 of the CRT of the aperture height above the lower aperture edge.

Baseline Displacement: the distance from the bottom of the CRT writing aperature to the lowest black portion of the character.

Character width is varied by controlling the stroke spacing. The spacing between strokes is made proportional to the width. A width-control register and width-control counter are used in conjunction with the horizontal counter to accomplish this. Before generating a character, a width number (proportional to the width of the character) is placed into the width register. Prior to updating the horizontal counter, the contents of the width-control register are transferred to the width-control counter. The contents of this counter are then used to control the number of update pulses fed into the horizontal counter. Table II shows that the number of strokes/em doubles for each increase of size range. Therefore, a common set of width numbers are sufficient to control width for all size ranges. To take care of half-point sizes shown in Table I, the width number is selected to be twice the point-size values shown in range I. The same width-control numbers are used for all granularity modes shown in Table I. Size modes *B* and *C* have half the number of strokes/em as mode *A*. The stroke spacing must be doubled. This is accomplished by stepping the next more significant stage of the horizontal counter for modes *B* and *C*, thereby doubling the distance between strokes. Mode *D* has half the number of strokes

Table I—Character point sizes vs size range and size group (type 1 font files)

Size Range	*a*	*b*	*c*	*d*	*e*	*f*	*g*	*h*
I	4	4.5	5	5.5	6	6.5	7	8
II	8	9	10	11	12	13	14	16
III	16	18	20	22	24	26	28	32
IV	32	36	40	44	48	52	56	64
V	64	72	80	88	96	—	—	—

Note: a point is approximately 1/72 inch.

Table II—Writing granularity vs size range and granularity mode (type 1 font files)

Size Range	*Granularity Mode* *A* V	*A* H	*B* V	*B* H	*C* V	*C* H	*D* V	*D* H
I	120	100	120	50	60	50	60	25
II	240	200	240	100	120	100	120	50
III	480	400	480	200	240	200	240	100
IV	960	800	960	400	480	400	480	200
V	1920	1600	1920	800	960	800	960	400

Notes: *V* is vertical increments/em.
H is horizontal increments/em.

Table III — Sweep-speed/vertical-counting-frequency vs size group

Mode / *Size Group*	*A/B* V*	*A/B* f**	*C/D* V*	*C/D* f**
a	2500	5.4	5000	5.40
b	2813	5.4	5000	4.80
c	3125	5.4	5000	4.33
d	3438	5.4	5000	3.93
e	3750	5.4	5000	3.60
f	4053	5.4	5000	3.32
g	4375	5.4	5000	3.09
h	5000	5.4	5000	2.70

Notes: *V is the sweep speed in inches/sec.
**f is the vertical counting frequency, 10^6 increments, or pulses per sec.

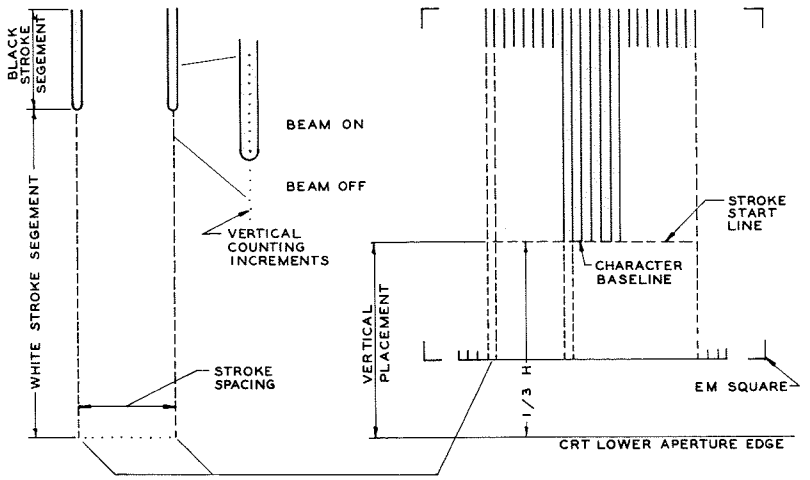

Fig. 4—Definition of scan parameters.

8-bit	D D D D D D C E
10-bit	D D D D D D D D C E
12-bit	D D D D D D D D D D C E

E: end of stroke
C: color of segment
D: data

Fig. 5—Videocomp segment formats.

/em as modes *B* or *C*, and doubling of the stroke spacing again is handled in the same manner.

Width-size control

Width-size control is independent of vertical control. Characters condensed and expanded in width with respect to height can be digitally controlled. A vertical-size number, in conjunction with a mode number, is used to select the correct beam velocity and vertical counting oscillator as required by Table III. This is accomplished by a simple logical look-up table.

The 4μs linearity interval must be accurately controlled for all velocities to assure that characters generated in any size group or mode will sit on the same baseline. This is controlled again by a simple look-up table of numbers, jammed into a counter which is stepped by the selected vertical counting oscillator. This system keeps the baseline correct to 0.1 mils. The selected oscillator must be used so that the 4-μs interval is started and stopped in synchronism with the selected oscillator.

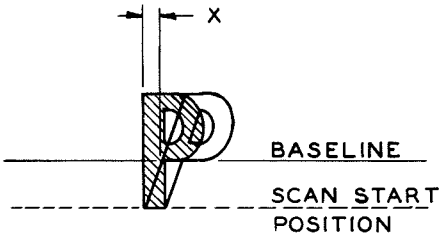

Fig. 6—Formation of italic characters.

Baseline control

Baseline control is achieved through the use of two control registers. The up/down register governs vertical movement of the stroke starting position within the CRT aperture. In the 70/830 Videocomp this is controlled to a precision of $\frac{1}{32}$ point. The baseline compensation register adjusts the beam-starting position for characters with different decender-to-ascender ratios, i.e. different style faces, plus differences in the position of the lowest black portions between characters in a font. This value is equivalent to the baseline displacement of Fig. 3. These quantities must be kept separate to control generation of italic characters. Baseline compensation is controlled to a precision of $\frac{1}{32}$ point in the 70/830 Videocomp.

Oblique control

Oblique (italic) characters are created in the Videocomp by causing the beam to sweep at an angle in the vertical direction. The characters when encoded are tilted into an erect position, and are played back on the Videocomp with an angular sweep on the face of the CRT to correctly represent an italic character (Fig. 6).

In order that the italic character starts in its correct horizontal position, it must be moved backward by the value *X*. This quantity *X* is proportional to the value of baseline displacement.

Beam-intensity control

Beam intensity is a function of mode, width and beam velocity. Mode and width define the spacing between strokes. An increase in stroke spacing necessitates a broader dot on the CRT; as a result, beam intensity must be adjusted to maintain proper exposure on film. When the beam velocity changes a particular spot on film sees the beam for a different time and the beam intensity must be adjusted to compensate. Here again, a simple logical look-up table selects the proper value of intensity as a function of mode, width control number and beam velocity. A logical look-up table selects the proper CRT spot size as functions of mode and width control number.

Film control

The remaining logic control of the Videocomp is control of film motion. The Videocomp cameras contains a rachet a nd paw mechanism. Each rachet movement respresents a film motion of one point. The pawl is lifted for the total number of points required to be moved. A photocell essentially looks at the rachet teeth and feeds back one pulse to the logic for each passing tooth. These pulses are used to decrement a counter. This counter has been preset to a number representing the required movement. When it is decremented to zero, the logic commands the pawl to drop. Another signal from the camera to the logic causes the logic to command the pawl to drop in synchronism with the next photocell signal received. This signal represents a tight-film condition. When this condition is cleared by the camera pushing additional film into a camera film-buffer loop, the logic commands the pawl to lift again until the film-advance control counter is decremented to zero.

Soft-hardware organization

The logic of the 70/832 Videocomp System has as its heart an RCA series 1600 processor[2] (Fig. 7). The 70/832 Videocomp is an off-line typesetting system. The input is a magnetic tape containing hyphenated and justified data, and font files which are prepared on a large scale processor. As a result, the system is composed of both soft and hard logic. The basic function of the RCA series 1600 processor within this system is to:

1) Read magnetic tape and convert the data received into commands understandable to the Photocopy Control Electronics Unit;
2) Store within its memory the working font files as required by instructions contained in the data received from magnetic tape;
3) Initiate character stroking by transfer of font-file data from its memory to the Photocopy Control Electronics Unit as required by magnetic tape instructions; and
4) Overwrite the working font-files as specified by magnetic tape data.

Soft logic

The results of the soft logic control are commands sent to the Photocopy Control Electronics Unit that:

1) Sets the horizontal counter to the starting position of the character to be written. This starting point is the first horizontal position that contains black information. The RCA Series 1600 Processor calculates this position from font-file data which includes Leading Side Bearing, Character Width and Trailing Side Bearing.
2) Sets the baseline-compensation value. The RCA Series 1600 Processor fetches this data from the working font files.
3) Sets the up/down value as specified by magnetic tape data.
4) Initiates the writing of the character by pointing to the proper place in font file memory via the high speed input-output channel, so that the Photocopy Control Electronics Unit can fetch the data as required.
5) Sets the advance counter as specified by the magnetic tape data.
6) Specifies that photographic material shall be cut as specified by magnetic tape data.
7) Specifies whether characters are to be typeset Roman or Italic as specified by magnetic tape data.
8) Specifies the vertical size, width and mode that characters are to be written in (see Table I).
9) Specifies the direction that characters are to be written, i.e., left to right or right to left.

Hard logic

The Photocopy Control Electronics Unit contains all the registers, counters and logical look-up tables that specifies to the 70/830 Videocomp Photocopy Unit, horizontal position, baseline compensation, mode width, CRT beam velocity, direction and roman or italic. In addition, it contains the logic that takes font-file data and converts it to scan on/off and CRT video on/off signals as described earlier. Internal to the Photocopy Control Electronics Unit is a pair of small buffers into

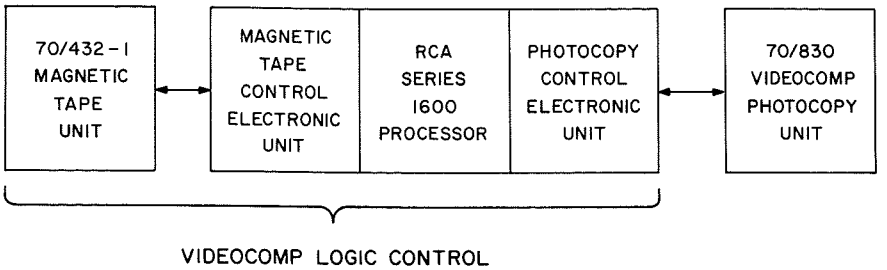

Fig. 7—The 70/832 Videocomp system.

which the segment words are stored when received from the Series 1600 Processor memory. The transfer from the Series 1600 Processor is byte serial and the logic unpacks the data on the fly, prior to storing in the small buffers. Therefore, each address of the small buffers contains segment length in either 8-, 10- or 12-bit formats. In general, as one buffer is being used to write a stroke, the second buffer is receiving data from the series 1600 processor memory. The buffers are sixteen words in length, and only those words required to write a stroke are stored in one buffer. If more than sixteen segments are required to write a stroke, the data is automatically overflowed into the alternate buffer, and data transfer from the series 1600 processor is stopped until the first buffer is empty. It is from these buffers that the video-ring counters, described earlier, access segment data. The high-speed access capabilities of these buffers allows writing of strokes at rapid rates. The lower speed series 1600 processor memory then must only supply data at the average rate required. The logic does not allow a new scan to be started unless at least one buffer is full. In this way, if the series 1600 processor cannot maintain the average data rate required, the system automatically slows down to compensate.

Test and maintenance

Incorporated within the Photocopy Control Electronics Unit is some very powerful test and maintenance logic. This logic allows the RCA series 1600 to read the contents of the horizontal register, the pair of small buffers, the video on/off flip-flop, the scan on/off flip-flop, plus some other meaningful flip-flops in the Photocopy Control Electronics Unit. In addition, a mode of operation allows substitution of the series 1600 input/output transfer pulse for the selected video-ring counting oscillator. Therefore, a series 1600 test and maintenance software package can make a detailed analysis of failures within the Photocopy Control Electronics Unit. It can sequence data through the buffers, checking each and every bit; create known video patterns, checking that the system properly responds to font file inputs; and check the timing of various system components.

Future possibilities

The organization of the digital control as shown in Fig. 7 can grow to many other typesetting applications. For instance, a remote terminal application can be conceived wherein the magnetic tape station and its associated controller can be replaced by a communications controller. The addition of a magnetic disc file would allow font files to be permanently stored at the remote terminal, thereby eliminating the need to transfer font file data over the communication lines. The most important feature of this type of organization is that the system can be adapted to an application by simply changing the configuration of standard data processing peripheral equipment and the software package resident in the RCA 1600.

Further growth beyond typesetting is also achievable with this organization. A means for digitally encoding graphics is realizable by using the CRT as a scanning device, digitizing the data so that high speed storage and retrieval is achievable. This data could be played back, at will, much in the same manner as writing characters. The addition of the vector generator will lead to mapping and plotting and this coupled with a text and graphics capability will in turn lead to much more sophisticated systems allowing human interaction for such purposes as editing and updating.

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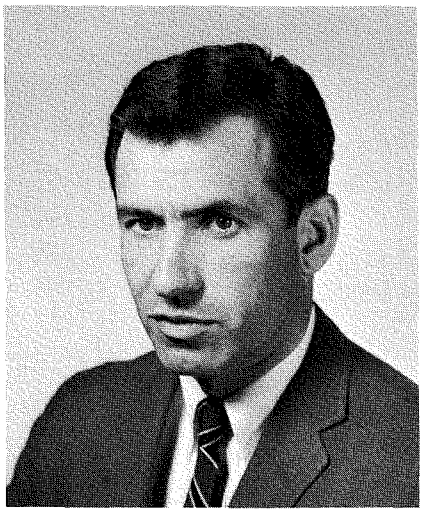
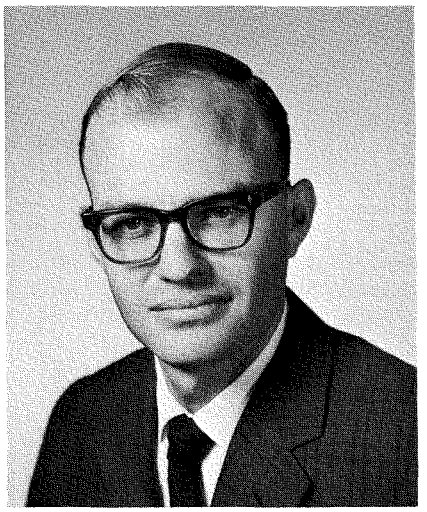
Application of retrodirective antenna systems to spacecraft

W. B. Garner* | D. Z. McGiffney

The availability of launch vehicles capable of handling large payloads has opened up a host of new applications involving large unmanned spacecraft. These large spacecraft imply a new dimension of complexity in the areas of power generation, attitude control, thermal control, large antennas, and high RF power generation. The conventional approach to these areas is to consider each as a neatly partitioned separate unit, with only minor over-laps in function and consequently in design. The retrodirective antenna (RDA) combines some of these functions into a single unit, achieving results that are, at best, difficult or nearly impossible to achieve with conventional-design antennas. This paper outlines the potential usefulness of RDA arrays in space systems; their principles of operation and general properties; and their advantages and disadvantages. Several specific space applications in which retrodirective arrays could be used are discussed.



D. Z. McGiffney
Systems Engineering
Astro Electronics Division
Princeton, N.J.
received a BS degree in electrical engineering from Rutgers University in 1954. He served in the U.S. Air Force from 1954 to 1956 as a project officer, at the Rome Air Development Center, specializing in electronic counter-measures. He performed graduate studies in Electrical Engineering at Syracuse University from 1956 to 1957. In 1957, Mr. McGiffney joined ITT Federal Laboratories, Nutley, New Jersey, where he designed RF circuits for TACAN equipment and performed systems engineering of microwave communications network. Mr. McGiffney joined AED in 1964 as a systems engineer, and has worked primarily on problems connected with wideband communications satellites. He has also participated in the Nimbus High Data Rate Storage System and Lunar Orbiter Programs. He is currently investigating space applications of advanced antennas. He is a member of the IEEE.



W. B. Garner
Systems Engineering
Astro Electronics Division
Princeton, N.J.
received a BSEE degree from Texas A&M in 1960 and subsequently took graduate courses in communications theory at the University of Pennsylvania. Mr. Garner joined the AED in 1960 as a design engineer, first on high power transistorized VHF amplifiers for space application on an IR&D Program and then on a multiplex telemetry system for a classified project. In 1963, he began a series of IR&D studies on distortion effects due to nonlinearities in CDM-PSK and FDM-FM systems, as applied to communication satellites. He participated in the systems design of the Lunar Orbiter TV transmission system, doing analytical studies, and defining problem areas. He participated in transmission specification studies for the Phase I contract let by the Communications Satellite Corporation to RCA and the Bell Telephone Laboratories for a random, medium altitude, communications satellite system. He subsequently helped in defining the transmission and transponder system performance specifications in the proposal for a Global Communications System. Mr. Garner is a member of the IEEE, Eta Kappa Nu, Tau Beta Pi, and Phi Kappa Phi.

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*Since this article was written Mr. Garner has left RCA to join the ComSat Corp. Laboratories.

MOST OF THE SYSTEMS proposed for the coming generation of communication satellites share the same general characteristics: large aperature antennas; medium to high RF power capability; and high pointing accuracy. These characteristics have a significant impact on the design of all major subsystems.

A multiple-user type of satellite requires antenna directivity for each user in separate geographical regions as shown in Fig. 1. This situation is typical in varying degree for many of the contemplated uses of earth-orbiting spacecraft. The nature of these systems requires a full-time service, implying earth synchronous orbits. But from synchronous orbit an area the size of the United States, for instance, subtends an angle of approximately 6 degrees East-West and 3 degrees North-South. If, for example, the use requires distinct area coverage in three areas in the U.S., the problems involved in providing narrow antenna beamwidths to cover each area with the requisite pointing accuracy is apparent. In addition, the stabilization accuracy of the satellite imposes additional restraints on antenna steering.

There are a number of approaches to satisfying these needs. The first approach is a simple single- or multiple-feed reflector-type antenna with a mechanical pointing mechanism. As the number of areas to be covered with

independent antenna beams increases, it becomes more and more difficult to meet the requirements. Movements of large masses present special stabilization problems. Mechanical interferences become harder to solve if independent control is required among beam directions. A centralized communications package is required with such an approach, making reliability through the use of redundancy difficult.

A second method would be to use a phased array. The beam scanning is all electronic with distributed antenna elements. A centralized sensing and control system is required to provide pointing information, and existing low weight phase shifting devices at microwave frequencies are lossy. Providing simultaneous independent beams greatly increases equipment complexity.

Another method would be to use a switched beam-forming matrix. This method uses distributed elements, but requires a central control system to generate pointing information. Since this approach uses discrete switched beam positions, a large number of elements are necessary if high pointing accuracy is required over a relatively large field of view. Switching transients can also affect communications performance.

All of these methods require close mechanical surface tolerances to preserve the properties of the antenna, causing stowage and deployment of the antennas to be difficult problems.

A systems approach

Recently, a systems approach has been taken to these problems. Instead of considering each subsystem of the communications system as a separate device capable of only one function, this approach considers these subsystems as if they were a whole system combining the functions of radiating, fine tracking, signal processing, and amplifying. This system must provide energy radiation in a specific direction referenced to some form of exterior signal with a given degree of accuracy at a given signal level.

A retrodirective antenna consists of an array of devices, each providing signal reception, amplification, and reradiation using relatively small fixed radiators and relatively low RF powers. Upon reception of an external signal, each black box processes the received signal, modifying the delay or phase of the signal such that all signals are reradiated with the same phase or delay in the direction of the received external RF signal.

Several properties are characteristic of this type of antenna-communication system. First, the antenna and electronics become merged into a single unit with no clear-cut dividing line between functions. Each device by itself has no beam directing properties, acting as any normal receive-transmit element. The aggregate effect of all elements together is to form a large-aperture antenna with the same directivity as an equivalent planar

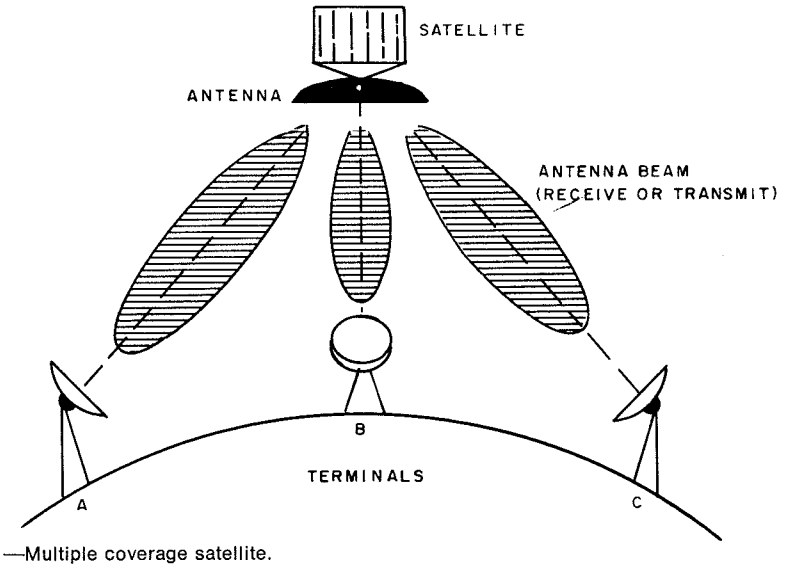


Fig. 1—Multiple coverage satellite.

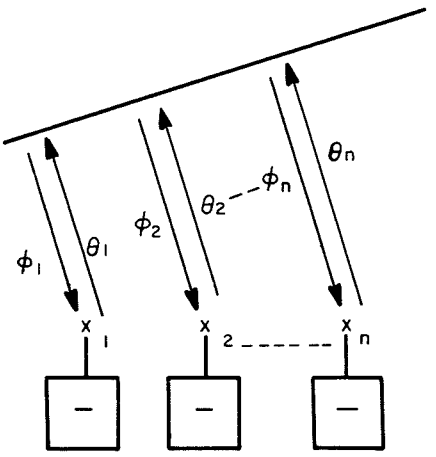


Fig. 2—N-element retrodirective array.

array having the same projected area. However, the directive beam can be electronically scanned over an angle limited only by the individual subelement patterns. The spacing tolerance (3 dimensional) between elements and over the entire array is non-critical compared to a conventional array of similar area. Moreover, failure of one element, or even of a number of elements at random, produces no catastrophic failure of the whole array. Of course, there are deficiencies and limitations which may make it unsuitable for some applications.

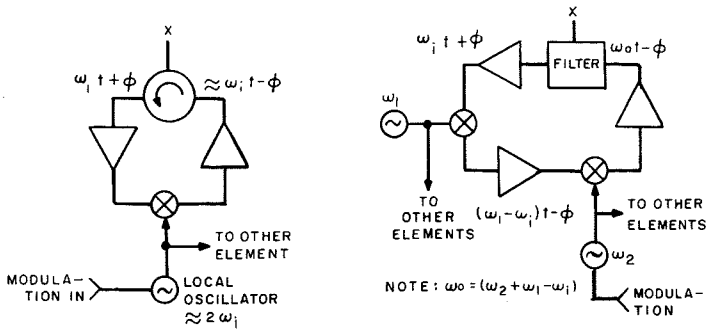
The RDA principle

Consider the operation of a retrodirective array composed of N elements (Fig. 2). A plane wave is received at the array from a distant source. The phase of the wave is constant along the reference plane perpendicular to the direction of propagation. The signal at any element, i, will have a phase, ϕ_i, measured from the reference plane.

Suppose now that each element inverts the phase, i.e., forms the conjugate of the input, and reradiates it with phase $-\phi_i$. Then when the reradiated wave reaches the reference plane it has a phase $-\phi_i+\theta_i$. If $\phi_i=\theta_i$, the final phase is 0. Moreover, it is 0 for *all* elements and the direction of maximum radiation is in the direction of the original received wave. The signal is thus redirected toward the original course. Note that the only function that must be performed at each element is phase conjugation; significantly, the geometry of the array does not enter into the result.

The condition $\phi_i = \theta_i$ implies that the receive and transmit frequencies are identical. If this is not true, the geometry of the array begins to affect the direction of reradiation and could be a limiting factor in retrodirective array design.

The phase conjugation function can be achieved by an ordinary mixer. If the local oscillator is higher in frequency than the incoming signal, the difference frequency will contain the negative of the phase of the incoming signal. This difference frequency can be reradiated, or retranslated and then reradiated. Two basic methods of amplifying the signal and retransmitting it are shown in Fig. 3.



(a) ONE LOCAL OSCILLATOR METHOD

(b) TWO LOCAL OSCILLATOR METHOD

Fig. 3—Basic retrodirective array modules.

The first method (Fig. 3a) requires all amplification to be accomplished at the receive and transmit frequencies but requires only one local oscillator common to all elements. The second method allows the bulk of the low-level amplification to be done at some convenient intermediate frequency, but requires two common local oscillators. (The oscillators need not be related in frequency or phase.) Modulating the local oscillator will transfer the modulation to the retransmitted signal.

The retrodirective antenna can also be designed as a receiving array as shown in Fig. 4. A separate auxiliary pilot signal is transmitted along with the modulated signal (any modulation method), filtered, and used as a reference. If the pilot and modulated signals are close together in frequency, the outputs from the modules will be nearly in phase and can be summed to provide the total output.

There are a variety of other implements possible to fulfill different requirements, including the configuration depicted in Fig. 5 in which the receive and transmit functions are combined to provide a radio relay.

A comparison of RDA and conventional systems

RDA offers many advantages. Because the electronics are distributed across the array, heat dissipation is not centralized and, therefore, does not create special thermal problems. Indeed, the real problem with an RDA in space may be just the opposite—how to keep it from getting too cold. The RDA eliminates the need for a fine tracking system. Not only does it acquire nearly instantaneously, it can track at relatively high rates. The basic device can be extended to track two or more sources independently and simultaneously, with the full gain of the array available to each beam. Such a multiple steered beam capability for CW signals is difficult to attain with conventional arrays.

Another advantage of the RDA is the ability to shape the re-directed beam to cover a geographical area of irregular shape by using several pilot sources at different locations, all at the same frequency.

An RDA also offers higher reliability than a fixed feed reflector antenna. Because of the fairly large population of nearly independent devices in an RDA, its degradation will be predictable (statistically). No single failure will significantly affect operation. In contrast, a single failure in a conventional reflector type system is generally major, if not catastrophic.

One limit to the usefulness of the RDA is weight. However, recent developments in integrated circuits and microwave solid-state amplifiers have brought lightweight transponders into the realm of feasibility. In the near future, if current trends continue, it should be possible to construct transponders using solid-state devices and RF microstrip circuits that are light enough to make the retrodirective array competitive with most conventional systems.

Because the array will have an appreciable thickness due to the electronics modules distributed over the array, new deployment methods are needed. Of course, the relatively low positional accuracy required of the extended RDA eases the problem as compared to, say, a conventional multi-element phased array.

There are a few other technical problems associated with the RDA. The RDA is frequency sensitive; the useful scan angle is a function of the difference between the pilot signal frequency and the information carrier frequency, depending somewhat on array geometry and required beam pointing accuracy. Also, although the RDA is insensitive to array surface tolerances it requires constant internal phase differences from element to element, both in the individual elements and in the lines connecting the element to the common local-oscillator. If subsequent deployment and component drift does not alter these errors, they are, at least theoretically, correctable before launch.

Applications

The use of a retrodirective array would offer significant advantages in several space systems. Some of these applications have been studied in detail assuming the use of conventional antennas.[1,2]

TV network and distribution

A satellite in a 24-hour orbit could be used to relay TV network programs across the country. The system must be capable of handling several programs simultaneously among several regions of the U.S., with no restrictions on varying the connectivity between the different regions from hour to hour as

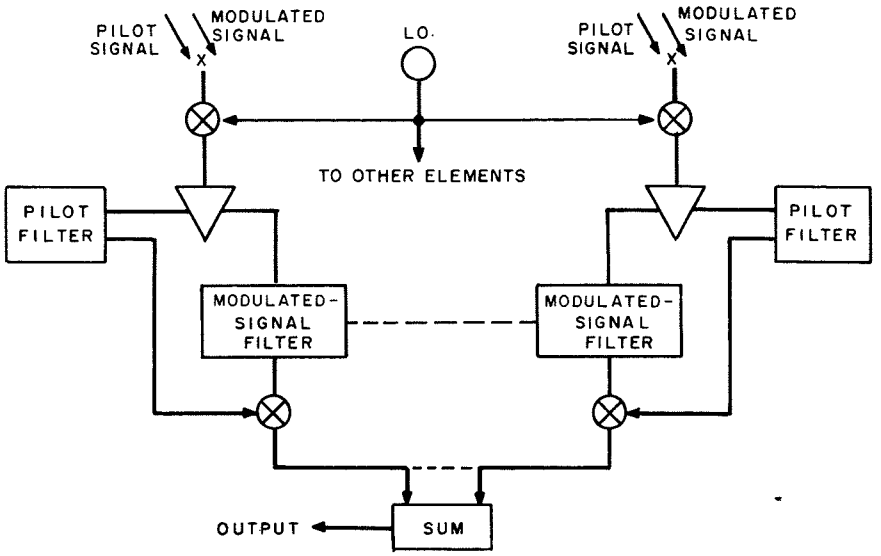


Fig. 4—Receive array.

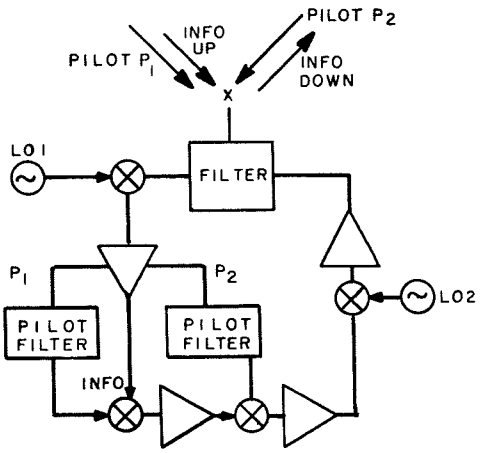


Fig. 5—Repeater.

the programming changes. The multiple steered beam capability of the RDA would offer advantages in this application. The transmit and receive beams could be steered automatically by pilot signals from the ground stations, and could be switched instantaneously as programming requirements changed. In a similar way, programs could be distributed to broadcasting stations within a given area.

TV broadcast

The retrodirective array could be useful in implementing a satellite-to-home TV broadcast system, such as the VISTA system proposed by RCA.[1] The VISTA system as proposed, had a conventional antenna (parabola with fixed feed) 50 feet in diameter and a 3-kW RF transmitter. By using a retrodirective array in place of the parabola, the usual advantages would accrue. The beam-shaping capability of the RDA would be a particular advantage in this application, allowing the broadcast beam to be shaped to conform to geographical requirements, and to be changed as requirements change.

Long-range ground-air communications

A system of satellites in 24-hour orbits could be used to provide long-range communications between aircraft and ground stations. This system could provide inter-continental mission control for military aircraft and mid-ocean traffic control for commercial airliners, not limited by the vagaries of high frequency ionospheric communication or the line-of-sight range of microwave propogation.

To be useful, of course, a system of this sort must be capable of simultaneous access by many aircraft. Again, the multiple steered beam capability of the RDA makes it suitable for this application.

Communications relay for manned and unmanned spacecraft

Another possible application of the retrodirective array would be as a relay between low orbiting spacecraft and ground stations. The use of several arrays in 24-hour orbits would permit continuous communications between a low-orbit spacecraft and a network of ground stations, eliminating coverage gaps that now exist. A recent study[3] of this type of data relay system showed the RDA to have unique advantages. AED is actively pursuing work in this area.

Deep-space probe

The RDA offers some promise for use on a deep-space probe. However, its performance is limited by the carrier-to-noise ratio obtainable within the individual elements of the RDA. This imposes a requirement on the minimum gain of the antenna elements, independent of the array gain. The great distances and accompanying path loss associated with these missions necessitate antenna elements with moderately high gain. The narrow beamwidths of these antenna elements would require high stabilization and pointing accuracies, but not as high as conventional parabolas or phased arrays.

Lander vehicle for planetary probe

Future planetary probes will probably involve the use of automated vehicles which land on the planet and gather scientific data. These vehicles could communicate with earth by way of a relay station orbiting the planet. A retrodirective array on the lander would be useful in maintaining radio contact over the wide range of pointing angles which the lander would have to accommodate.

Conclusion

The initial investigations of the RDA show it to be a most promising device for missions requiring high pointing accuracy, long life with graceful failure properties, simultaneous handling of two or more signals from different sources, and relatively high powers and large antenna gains. They may also have considerable utility in applications requiring large scan angles and medium gain. Because of the complexity of these arrays, however, they might not be able to compete in applications requiring low gain and power, such as those in most of today's near-earth orbit spacecraft.

References

1. Marsten, R. B., and Gubin, S., *VISTA—System Design of a Proposed Direct-to-Home TV Satellite Experiment* (RCA Engineer, Aug.-Sept. 1966).
2. Gubin, S., *TV Network Satellite Systems* (AIAA Communications Satellite Systems Conference, Washington, D.C., May 1966).
3. Orbiting Data Relay Network Final Report (AED Contract No. NASW-1447, March 22, 1967).

Zero-delay video systems

R. J. Butler

The goal in the development of a zero delay video system was to produce correctly timed studio outputs which could be routed through a distribution switcher for indiscriminate use within a broadcast station. This paper describes the needs and considerations for such a system, and traces the steps that led to the evolution of a production-model, zero-studio-delay amplifier.

TO GAIN INSIGHT into the need for zero-delay systems, consider the output (A) of the routing switcher shown in Fig. 1, which is set up to deliver all sources of video to specified inputs of studio switchers. Looking back from point A, all cross points within the routing switcher appear as possible sources of video. These include not only cameras, tape, and film chains, but the outputs of other studios being served by the same routing switcher.

Programming demands on normal plant, or station, operation require one studio to be acceptable as an input to other studios. At first glance the routing switcher can perform this requirement without difficulty. A closer inspection, however, reveals a timing problem. This is illustrated in Fig. 1, where it can be seen that the path from the camera through Studio No. 3 to Studio No. 1 is longer than the path directly to the A input of Studio No. 1. This results in a timing error.

Customary timing methods

It is customary in plant operations to time the generation of video by pulse delays. Each video source derives its scanning information from a central clock or sync generator. Internal equipment and path delays are complemented by pulse-time delays in series with each source so that video signals will arrive at some predetermined junction in a fixed time relation. However, this solution for standard video sources will not work for a studio, because there are no pulses fed to a studio which determine picture timing.

In the past, timing problems encountered through studios were handled by altering trim delays in series with each source. For example, Fig. 2 shows the studio pulse delay method. In this instance, not only are trim delays in series with each source, but, in addition, a delay exactly equal to the studio video path is provided. When cameras are to be routed through one studio before entering a second studio, the pulse studio delay is switched out; thus, the generation of video is earlier than normal by exactly the length of the first studio. This system has worked successfully but has the following three major drawbacks:

1) Predetermined routing must be established so that appropriate studio pulse delays can be set.
2) Simultaneous usage of a given source is not possible in all studios.
3) Additional studio pulse delays must be added to each source if more than one studio is to be encountered before final integration.

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Robert J. Butler
Engineering Planning and
Equipment Development
National Broadcasting Company
New York, New York
studied Electrical Engineering at New York University and joined the RCA Service Company in February 1947. He was transferred to the National Broadcasting Company in March of 1952 and has worked in all phases of color studio development. Mr. Butler was appointed Project Engineer in the NBC Engineering Planning and Equipment Development Group in October of 1966.

The genlock system cannot solve this problem. Fig. 3 shows a studio complex utilizing a genlocked sync generator as the source of timing information for local cameras. In this system, no prior routing information is required to keep local cameras in step with the output of a previous studio switcher. Disregarding the prior path length, the genlock system will always keep all local cameras aligned with the switcher input which supplies the genlock generator with reference information. However, the previously stated restriction regarding simultaneous usage in more than one studio still has not been overcome. In addition, the genlock system makes it mandatory that specific video sources be associated with specific studio switchers.

None of the preceding methods did anything to a studio to make its outputs synchronous at a given junction. Rather they provided an adjustment of all sources so that studio delay was cancelled out.

Effect of timing errors

Consider delay as it affects horizontal and vertical picture displacement. Fig. 4 illustrates two pictures, presented on the same monitor—the solid line image is the normally timed signal, and the dotted line image has been delayed by 5.3-μs. The result in the horizontal plane is a left to right shift of 10% for the dotted line picture. Vertical displacement for all practical purposes is zero. Fig. 5 sets up the same conditions as those shown in Fig. 4, but this time the delay of the dotted line picture is exactly equal to one horizontal line period—some 63.5-μs. Horizontal displacement between the two pictures is now non-existent, and the vertical depression of the dotted line picture is much less than the previously noted instance in which the horizontal displacement was only 5.3-μs. The exact displacement in the vertical plane is one line out of the approximately 241 active lines that make up one field. The exact percentage is 1/241 x 100, or less than one half of one percent. It should be noted that even this small shift is evident only because the solid and dotted images are identical.

From a subjective point of view it would seem that if a studio has delay it would be very desirable to make that delay exactly equal to one horizontal

line period (1H). And the state of the art now permits video delays of high quality easily equal to 1H. However, consider what happens to the synchronizing portion of a video signal under identical conditions as those set up in Fig. 4 and 5. Fig. 6A is representative of the normally timed signal; Fig. 6B, the 5.3-μs delay; and Fig. 6C, the 63.5-μs delay.

Criteria for zero-delay system

Both Figs. 6B and 6C represent nonsynchronous conditions when compared to Fig. 6A. Fig. 6C represents the subjectively acceptable situation but it is obvious that vertical sync is late by 1H. In other words, it seems perfectly acceptable to delay a picture by 1H but any delay of sync is intolerable. In light of this, the following two delay criteria must be met to render a studio output acceptable as a timed video source:

1) The active video (trace time) path length must be equal to 1H or a multiple thereof.
2) The sync structure (retrace time) path length must be effectively equal to zero.

Fig. 7 depicts the implementation of the criteria specified. A studio switcher of any length (less than 1H) is increased in delay by adding an acoustical delay line in series with its outputs so that the total delay of the system is 1H. Since most studio switchers have relatively short delay, on the order of 1- to 5-μs, the necessary complement to achieve 1H is in the neighborhood of 60-μs. A genlocked sync generator with a sync backtiming capability can be used to produce the effective zero delay sync path. All that remains is to replace the sync structure that accompanies the video signal through the 1H delay path with the sync supplied from the genlocked generator. Since all of trace time comes via the 1H path and all of retrace time from the genlocked generator, a normal blanking output of the generator serves as the switch driving voltage to properly integrate sync and video in the studio output.

Special consideration for color video

A further complication arises when a color-video signal is considered. The subcarrier is specified to be an odd harmonic of one-half the line frequency. This means that a 1H delay is not an integral multiple of wave lengths of the subcarrier frequency. The fact is, the subcarrier eminating from the output of a 1H delay system will be 180° out of phase with the subcarrier entering the system. There are two ways that that problem can be overcome. The first increases studio delay so that the total length is 2H. The subcarrier now is in phase at both the input and output of the system. Horizontal displacement is zero but vertical displacement is increased to 2 lines. Picture depression is now equal to 2/241 x 100 = 0.8%. Although only two lines of each field are deleted, the signal when presented on a monitor, will show four lines blanked at the top of the picture because of interlace. However, interlace does not alter the vertical displacement when a full frame is considered, because the percentage is now expressed as 4/482 x 100 = 0.8%.

The second method for producing an in-phase subcarrier output from studio delay systems utilizes a modified 1H delay scheme. Studio length is now complemented not to equal 1H, but to equal 1H plus 180° of subcarrier, approximately 140 ns in excess of the nominal 63.5-μs. Fig. 8 shows the horizontal and vertical displacement when the modified 1H system length is used. Again it should be pointed out only the identical nature of both solid and dotted line images provide a reference for displacement recognition.

Figs. 9A through 9F show the relative timing of signal components during processing by a modified 1H system. This relative timing is as follows:

9A—The arrival time at the switcher input
9B—The video timing after normal studio delay
9C—The 1H delayed video with additional 140 ns path delay included
9D—The blanking signal from the generator
9E—The backtimed sync and burst from the genlocked sync generator
9F—The studio output

Figs. 9A and 9F differ only in that vertical blanking is increased by 1H and horizontal blanking is increased by 140 ns.

There are approximately 188 cycles of subcarrier in one active period of horizontal scan. Horizontal displacement because of the one-half cycle of additional delay is therefore equal to 0.5/188 x 100 or less than 0.3%. Close

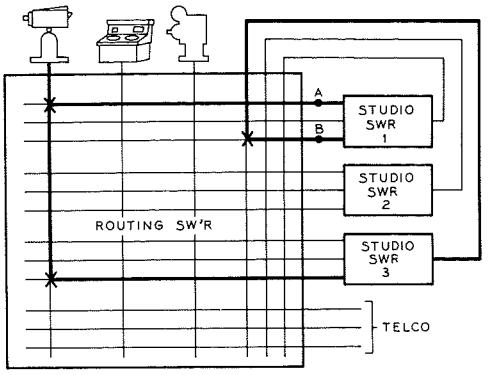


Fig. 1—Block diagram depicting inputs and outputs for television routing switcher.

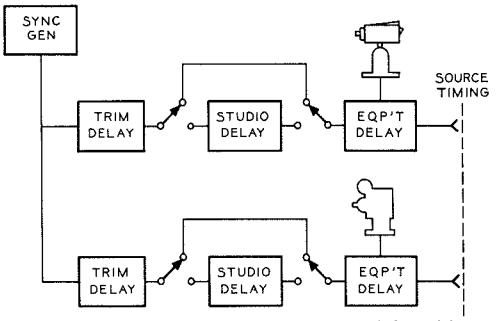


Fig. 2—Studio pulse-delay system used for video-timing control.

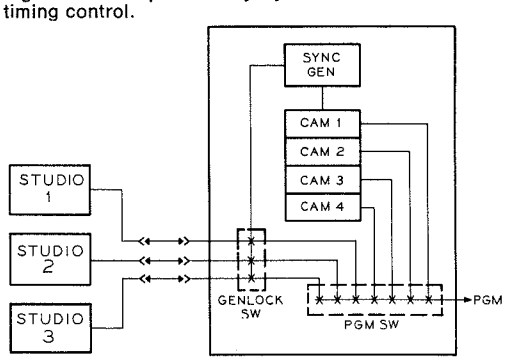


Fig. 3—The genlock sync generator used as source for video-timing information.

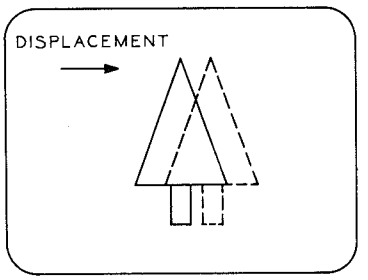


Fig. 4—Image displacement resulting from 5.3 μs video delay.

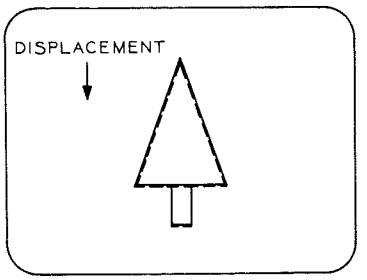


Fig. 5—Image displacement resulting from 63.5 μs (1H) video delay.

inspection of the waveforms of Fig. 9 shows that a regenerated burst is really necessary only to replace the first burst following the trailing equalizing pulse train. However, straightforward equipment design has indicated the simplest method is to replace all bursts in every blanking interval.

Zero-studio-delay amplifier

Fig. 10 is a simplified block diagram of the first production model of the zero-studio-delay amplifier. The unit is a 5¼ inch rack mounted chassis that includes the following three basic components:

1) Power supply
2) Processing amplifier, with self-contained monochrome sync generator, subcarrier regenerator, burst regenerator and video handling circuits
3) Acoustical video delay line with self-contained modulator and demodulator

The video delay-line unit is a replaceable module that must be matched to the studio delay to be complemented.

Fig. 11 shows the zero-studio-delay amplifier as it would be normally incorporated in a studio. Note that at least three program feeds are not affected by a complementary delay. The reasons for not including a zero-delay capability in these paths are as follows:

1) *Primary program output to Telco or Transmitter.* Added equipment in this path serves no purpose and jeapordizes program continuity.
2) *Return feed studio monitoring.* Adding a processing amplifier to this path would mask all input irregularities from monitoring facilities.
3) *Transmission monitoring.* As in the case of return feed monitoring a processing amplifier in this path would defeat the purpose of the feed.

All other program feeds have no purpose other than to feed-in plant loads. Therefore, complementary delay and processing are included in their paths.

Concluding remarks

The first on-air use of the zero studio-delay amplifier was in July at the Republican Convention in Miami. The scope of the political convention did indeed require a two studio operation with interchangeable mixing of studio cross feeds. As of this writing all field tests of the delay equipment indicate that the design goals have been satisfactorily met.

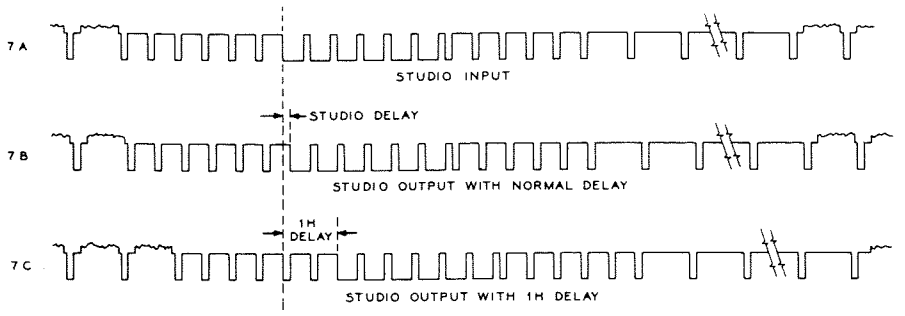


Fig. 6—Effect of 5.3 μs and 63.5 μs delays on video signals.

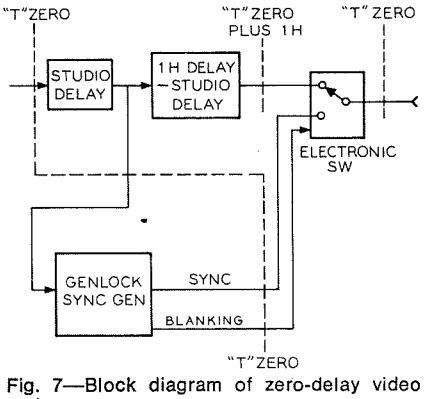


Fig. 7—Block diagram of zero-delay video system.

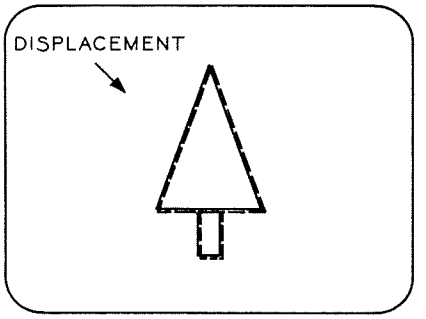


Fig. 8—Image displacement resulting from modified 1H delay system.

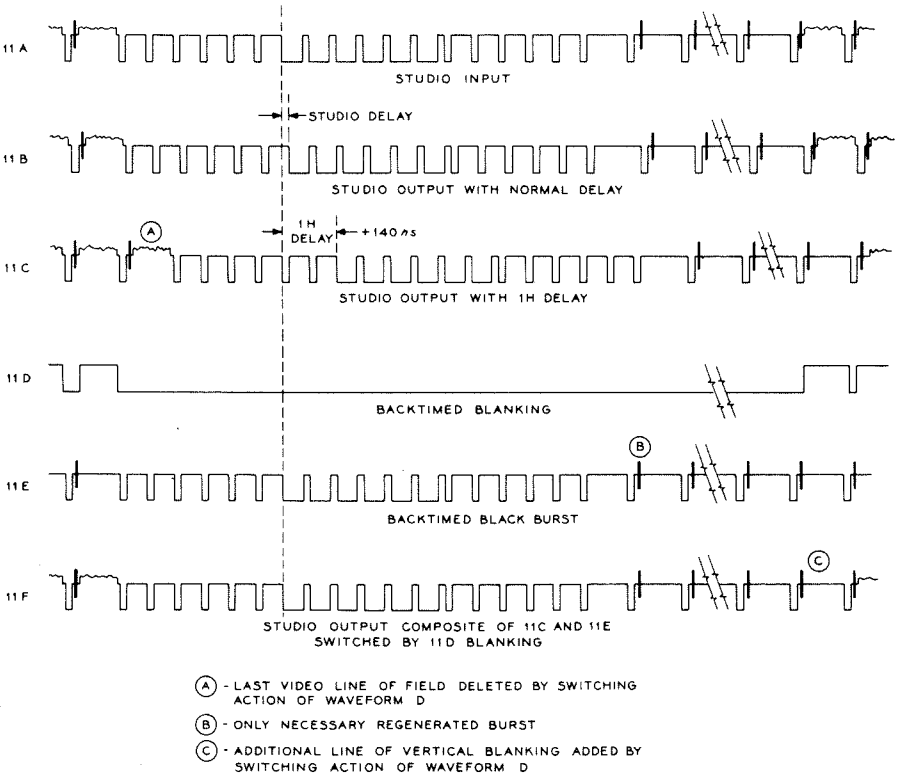


Fig. 9—Relative timing of video-signal components using modified 1H delay system.

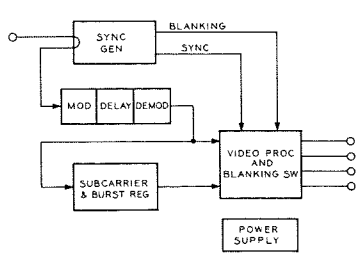


Fig. 10—Modified block diagram of zero-studio-delay amplifier.

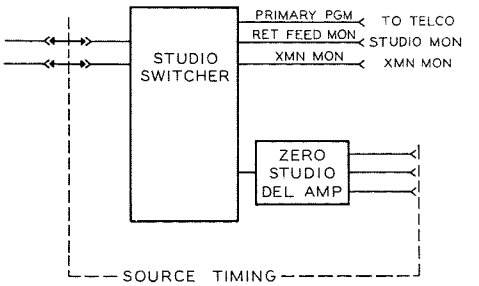
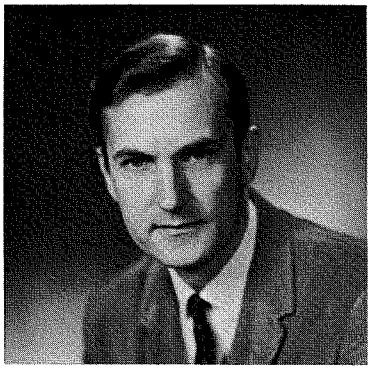


Fig. 11—Use of zero-studio-delay amplifier in television studio.

Three RCA men elected IEEE Fellows

The three RCA men cited herein have been honored for their professional achievements by being elected Fellows of the Institute of Electrical and Electronics Engineers. This recognition is extended each year by the IEEE to those who have made outstanding contributions to the field of electronics.

Dr. Karl G. Hernqvist
Materials Research Laboratory
RCA Laboratories
Princeton, New Jersey



. . . for invention and outstanding technical work in the field of gas discharge devices, thermionic energy conversion, and laser technology.

Dr. Karl G. Hervquist received the PhD in Electrical Engineering from the Royal Institute of Technology, Stockholm, Sweden, in 1959. He worked on radar and microwave instrumentation in the Royal Swedish Air Force in 1945 and 1946. From 1946 to 1952 he was concerned with electron-tube research at the Research Institute of National Defense, Stockholm. He was an American-Scandinavian Trainee at RCA Laboratories in 1949. In 1952 he joined RCA Laboratories, where he has worked on microwave tubes, electron guns, and gas-discharge devices. In 1956 he independently conceived and reduced to practice the thermionic energy converter. He is currently a member of the Quantum Electronics Research group in the Materials Research Laboratory. Dr.Hernqvist has gained an international reputation for his work. He has been the recipient of three RCA Achievement Awards for outstanding work in research. He has authored several dozen technical papers and holds 15 patents. He is a member of the American Physical Society and Sigma Xi.

Dr. Kerns H. Powers, Director
Communications Research Laboratory
RCA Laboratories
Princeton, New Jersey

. . . for contributions to and supervision of the development of new communications systems and concepts.

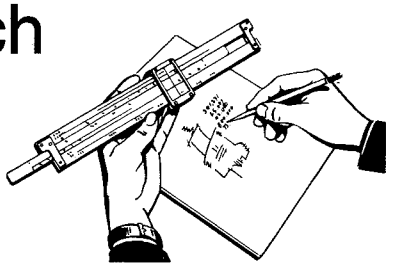
Dr. Kerns H. Powers received the BS and MS in Electrical Engineering from the University of Texas in 1951 and the ScD from Massachusetts Institute of Technology in 1956. He joined RCA Laboratories as a member of the Technical Staff in 1951 and performed research in color television and on a high resolution radar system. From 1953 to 1955 he held an industrial fellowship in Electronics at MIT. In 1956, he returned to RCA Laboratories where he pursued work in communication theory. In 1959 Dr. Powers was placed in charge of error-correction coding and modulation systems studies in connection with a U.S. Navy project for which work he received an RCA Achievement Award for the year 1960. He became technical director of new systems, special projects, in 1960 and was responsible for the development of a new low frequency communication system for the Navy. In June 1966 he was appointed to his present position. Dr. Powers is a member of Tau Beta Pi, Eta Kappa Nu, and Sigma Xi. He has served on several government committees and is the author of several papers in communications theory. He holds five issued patents.

Dr. Fred Sterzer, Director
Microwave Applied Research Laboratory
Electronic Components
Princeton, New Jersey

. . . for contributions in the field of microwave solid-state energy sources and microwave modulation and demodulation of light.

Dr. Fred Sterzer received the BS in physics in 1951 from the College of the City of New York, and the MS and PhD degrees in 1952 and 1955, respectively, from New York University. From 1952 to 1953 he was employed by the Allied Control Corporation in New York. During 1953 and 1954 he was an instructor in physics at the Newark College of Engineering in New Jersey, and a research assistant at New York University. He joined the RCA Electron Tube Division in Harrison, N.J., in October, 1954, and transferred to Princeton, N.J., in 1956. Dr. Sterzer's work has been in the field of microwave spectroscopy, microwave tubes, light modulators and demodulators, microwave solid state devices (including parametric amplifiers, tunnel-diode microwave amplifiers and frequency converters, microwave computing circuits, and bulk-effect devices). Dr. Sterzer is a member of Phi Beta Kappa, Sigma Xi, and the American Physical Society. He holds 18 patents in the microwave field and is the author of approximately 50 technical papers.

Engineering and Research Notes



Brief Technical Papers of Current Interest

A fluid damper for spacecraft nutation

K. Ayache | R. Lynch
Spacecraft Dynamics
Astro-Electronics Division
Princeton, N.J.

Ayache

Lynch

The gyroscopic effect of a spinning body is used to assist in establishing a stable attitude (or pointing direction) for a spacecraft. For example, in the TIROS satellites, the weather photos taken must be indexed to the Earth's geographical coordinates. Initially, the entire spacecraft was spun; in more recent designs, a momentum wheel—spinning about a central axis—provides equivalent stabilization.

However, the free-motion of the spacecraft also includes a wobble (nutation) of the spin axis, describing a cone around the total momentum vector. Nutation can be removed by the action of a properly installed energy-absorbing motion damper whose effect is a function of the amount of nutation still present. Thus, the energy of nutation is slowly dissipated by the damper until the spin axis coincides with the momentum vector.

The more recent models of the TIROS-series spacecraft utilize pairs of liquid-filled toroidal-shaped tubes, installed with the toroid axis at right angles to the spin axis. The motion of nutation excites each toroid tangentially, causing the contained liquid, by virtue of the viscous effect (or drag) of the surrounding wall, to flow relative to the tube. The energy absorbed by this action is taken from the nutational forces, and some is transferred through the spacecraft to the spin axis.

To determine quantitatively the effect of variations of the parameters concerned on the performance of the damper, analysis for a liquid-filled toroidal-shaped damping tube containing a void, or bubble, were developed. This analysis considers the case where a bubble is present in a rotating toroidal damper due to thermal contraction of the fluid. Consider a damper shown in Fig. 1 where a simple void is assumed. The dynamic effects arise from the sharp density change at the liquid surface. The centrifugal effects of the bubble imposes pressure forces on the fluid motion thereby changing the fundamental characteristics of the damper assembly. The forces can attenuate or supplement the damping action of the assembly.

The analysis depicts the major effects of the presence of the bubble while it ignores some secondary considerations. That is, the bubble is taken always as a void across the complete tube area.

Note that the surface-tension effects are not considered. These tensions can be significant in affecting damper performance at low vehicle spin rates. Damper performance at low vehicle spin rates can also be significantly affected by the existence of temperature gradients along the fluid path. The temperature changes are, after all, reflected as continuously varying fluid densities; and a void as a discontinuous change in fluid density. The detailed derivation is given in an RCA internal report[1] but a summary of the analysis is given here.

An expression is derived for the pressure resulting from an incremental displacement, D, of the damping tube normal to the spacecraft's spin axis. The pressure gradient, ∇P, across the tube then is defined and is incorporated into the classic Navier-Stokes equation of fluid motion:

$$\rho \frac{d\mathbf{V}}{dt} = -\nabla \mathbf{P} + \mu \nabla^2 \mathbf{V} \qquad (1)$$

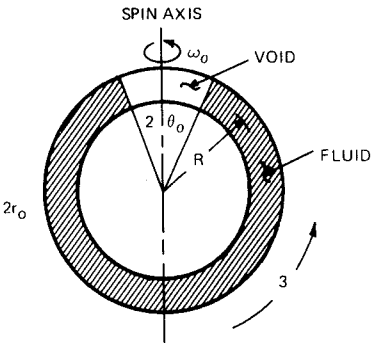


Fig. 1—Geometry of toroidal damper with bubble.

in which ρ is the fluid density, μ is the coefficient of viscosity and V is the velocity.

Taking the solution as a product of a function of time, alone, and a function of a radius, r, alone, the equation:

$$(\lambda - V_o c)\ (-\mu j\omega)^{-1} = F''(r) + \frac{1}{r} F'(r) + j\omega\rho\mu^{-1} F(r) \qquad (2)$$

is developed. This equation has for its solution a Bessel function of complex argument:

$$F(r) = AJ_o(r[j\omega\rho\mu^{-1}]^{1/2}) - (\lambda - V_o c)\ (-j\omega)^2 \rho^{-1}$$

Letting β represent $(r[j\omega\rho\mu^{-1}]^{1/2})$, the general solution of Eq. 1 becomes (for the boundary condition $V = V_o$ *at* $r = r_o$):

$$V = \left[\left(V_o + \frac{\lambda - V_o c}{(-j\omega)^2 \rho}\right)\frac{J_o(\beta)}{J_o(\beta_o)} - \frac{\lambda - V_o c}{(-j\omega)^2 \rho}\right] \exp(-j\omega t) \qquad (3)$$

in which λ represents $\dfrac{2\rho\,\omega_o}{\pi r_o^2} \displaystyle\int_o^{r_o} Vr\,dr$

The angular momentum, L $(=\int VR\,dm)$ is developed as the expression:

$$L=\frac{IV_o}{R}\left[\frac{\alpha+k(\alpha-1)}{1+k(\alpha-1)}\right]\exp(-j\omega t) \qquad (4)$$

in which α represents $\dfrac{2}{\beta_o}\cdot\dfrac{J_1(\beta_o)}{J_o(\beta_o)}$

and $K=\left(\dfrac{\omega_o}{\omega}\right)^2\dfrac{\theta_o}{\pi}$ where ω_o is spin frequency and ω is exciting frequency.

For a damper mounted in the spacecraft with its plane parallel to the spin axis, the accelerating torque about the spin axis is due to the out-of-phase component of momentum (imaginary part). When the spacecraft nutates, the angular accelerations excite

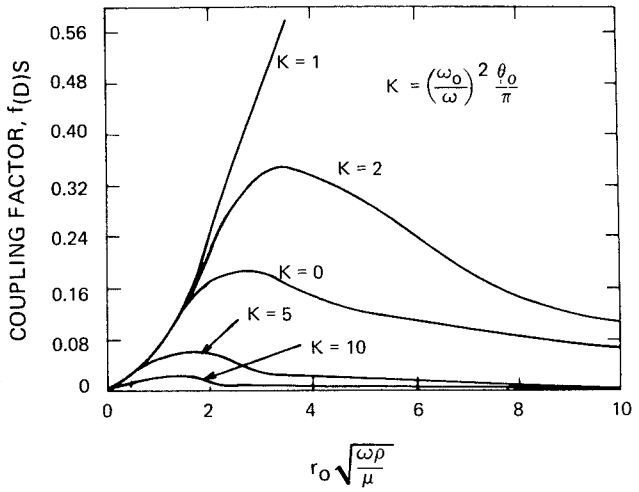


Fig. 2—Effect of bubble size on damping performance.

the fluid causing it to move relative to the tube walls. The energy losses damp the angular acceleration and increase the momentum component parallel to the spin axis. Thus the imaginary part of the angular momentum is a direct measure of damper performance.

$$\text{Imag. }[L]=\frac{IV_o}{R}\left[\frac{\alpha\text{ imaginary}}{(1-K)^2+K^2\,|\alpha|^2\text{ magnitude}+2K(1-K)\,\alpha\text{ real}}\right] \qquad (5)$$

A plot of $\dfrac{\text{imaginary }[L]}{\dfrac{IV_o}{R}}$

against the argument β for different values of K is made and is shown in Fig. 2. These curves show the improvement or degrading of damping as the bubble size varies, compared with the no-bubble case $(K=0)$.

Reference

[1] Ayache, K. and Lynch, R., *Analysis of the Performance of Fluid Dampers for Nutation in Spacecraft*, internal report.

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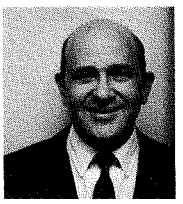
Data error rate improvement by redundant transmission

C. Mengani
Defense Advanced Communication Laboratory
Defense Communications Systems Division
West Windsor, N.J.



In certain applications, a data terminal or facility may be capable of transmitting and receiving data at a bit rate higher than the information bit rate required. The higher bit rate transmission capability can be exploited to improve the information-bit error rate by the redundant transmission of information bits. For example, if the transmission bit rate is 13 times the information-bit rate, each information bit can be repeated 13 times in transmission. A majority decision decoder at the receive terminal can then decode the receiver bit stream with as many as six transmission bit errors in the group of thirteen bits representing one information bit. When a redundancy capability of the above type exists, substantial improvements, as shown below, in information bit error rates are possible with the addition of relatively simple logic. Following is an analysis of the improvement that can be expected.

Let n be the number of redundant bits transmitted (13 in the above case); P is the transmission bit error rate (errors are assumed to be randomly distributed); and $Q = (1\text{-}P)$. Then, assuming the majority decision decoder will decode incorrectly only if at least $(n+1)/2$ bits transmitted are received in error in a group of n bits received, the probability of incorrect decoding (P_e) is

$$P_e=\sum_{k=0}^{(n-1)/2}C(n,k)\,P^{n-k}Q^k$$

where k is the number of bits received correctly, and $C(n,k)$ is the combination of k bits received correctly of the n bits transmitted.

The first term of the summation (P^n) represents the probability of all n bits being received in error; the second term (nP^n) represents the probability of all but one bit being received in

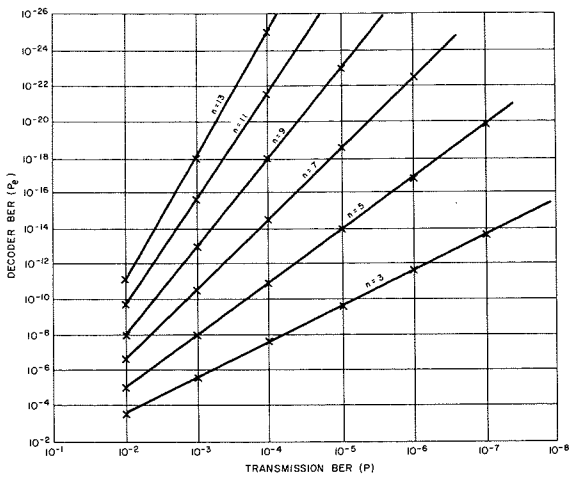


Fig. 1—P_e versus P for various values of n.

error; . . . . and the last term $(C(n,(n-1)/2)\ P^{n-(n-1)/2}Q^{(n-1)/2})$ represents the probability of $(n+1)/2$ bits received in error.

The ratio of each term in the summation to its preceding term is:

$$\frac{C(n,k)\ P^{n-k}\ Q^{k}}{C(n,k\text{-}1)\ P^{n-(k-1)}\ Q^{k-1}} = \frac{C(n,k)\ Q}{C(n,k\text{-}1)\ P} = \frac{(n-k+1)}{k} \cdot \frac{Q}{P}$$

If P is small $(P \leq 10^{-2})$, and if $k \leq (n\text{-}1)/2$, this ratio is much greater than one.

$$\frac{(n-k+1)}{k} \cdot \frac{Q}{P} > 20$$

Therefore, the last term in the summation essentially determines P_e; thus, P_e can be approximated with small error by:

$$P_e \cong (C(n,(n\text{-}1)/2)\ P^{n-\frac{n-1}{2}}\ Q^{\frac{n-1}{2}} = C(n,(n\text{-}1)/2)\ P^{\frac{n+1}{2}}\ Q^{\frac{n-1}{2}}$$

For $P \leq 10^{-2}$, $Q^{\frac{n-1}{2}} = (1\text{-}P)^{\frac{n-1}{2}} \cong 1 - (n\text{-}1)P/2$—for reasonable values of n (e.g., $n<20$)—so that, $P_e \cong C(n,(n\text{-}1)/2^{\frac{n+1}{2}}\ (1 - (n\text{-}1)P/2)$.

Fig. 1 plots P_e versus P for various values of n. As expected, substantial improvements in data bit error rate are evidenced. An increase in n, the amount of redundancy, results in still further improvement. Following is a sample calculation:

For $n = 13, P = 10^{-2}$,

$$P_e = C(13,6)\ (10^{-2})^7(1 - 6 \times 10^{-2})$$

$$= \left(\frac{13!}{6! \times 7!}\right) 10^{-14} \times 0.94$$

$$= 1716 \times 0.94 \times 10^{-14}$$

$$= 1.61 \times 10^{-11}$$

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Integrated S-band upconverter

P. Bura
Defense Advanced Communication Laboratory
Defense Communications Systems Division
West Windsor, N.J.

A microelectronic S-band upconverter was designed and fabricated in microstrip on alumina substrate. An upconversion gain of 1.9 dB and 31% pump efficiency were measured.

Design approach

The upconverter translates the input signal at 405 MHz into the output at 2250 MHz; the pump frequency is 1845 MHz. A varactor was used to achieve upconversion gain. Both balanced (quadrature hybrid) and unbalanced designs were considered. The advantages of the balanced design are the inherent pump-to-output isolation and greater pump efficiency, as the isolating filters are not needed. The disadvantages are greater cost (two matched varactors needed) and larger size. As the first approach, the unbalanced single diode design was investigated.

Filter design

In a single-ended design, filters are needed for input to output isolation. The output and pump filters are of the odd-mode coupled type while a broadband choke isolates the input circuit. For a 10% 3-dB bandwidth, 2-pole filter, the loaded Q_L and the coupling coefficient K are $Q_L = \sqrt{2}f_o/B = 14.1$ and $k = 1/Q_L = 0.071$.

To halve the filter size, quarter-wavelength resonators are used instead of the usual half-wavelength ones. This requires them to be shorted at one end and open at the other.

A shorted resonator allows for a convenient load or generator coupling. Instead of an odd-mode coupling, a direct tap-off connection is used to a point in the resonator that gives the correct loaded Q:

$$Q_L = (\pi R_g/4Z_o)\ \mathrm{cosec}^2(2\pi l/\lambda)$$

where R_g is the generator or load resistance; Z_o is the characteristic impedance of the filter resonator line; λ is the center wavelength; and l is the distance of the tap-off point from the shorted end.

This expression shows the advantages of selecting a low-impedance filter: 1) the unloaded Q of the filter will be higher, resulting in lower insertion loss, and 2) the tap-off point will be further away from the shorted end, permitting better positioning accuracy. However, too-low impedance results in wide lines and spacings. A 35-ohm line was chosen as good compromise between size and performance. If $R_g = 50$ ohms, $Z_o = 35$ ohms, and $Q_L = 14.1$, then $l = 0.0452\lambda$. From the known value of the coefficient of coupling, the odd-mode-to-even-mode impedance ratio can be calculated:

$$Z_{oo}/Z_{oe} = (1 - k)/(1 + k)$$

For $k = 0.071$, $Z_{oo} = 0.858\ Z_{oe}$, and for $Z_{oo} = 35$ ohms, $Z_{oe} = 40.3$ ohms.

From these two impedances, the strip width and spacing can be obtained.[1] The UHF signal is applied through an isolating choke.

The isolating choke consists of a quarter-wavelength low-impedance (15-ohm) open-circuited line followed by a quarter-wavelength of high-impedance (80-ohm) line. The center frequency is the mean between the pump and the output frequencies. The choke presents a high impedance at both of these frequencis, thus preventing dissipation in the signal source impedance.

Varactor calculations

The upconverter performance can be optimized for either best pump conversion or for signal conversion efficiency. In the latter case, the upconverter gain can be improved with some sacrifice of pump efficiency. A high-power-level analysis of an upconverter is very complicated, as it leads to a set of nonlinear equations. It can be simplified by imposing a condition limiting the total junction voltage swing between forward conduction and reverse breakdown. This is approximately expressed by the relation $m_s + m_p + m_u \leq 0.25$ where m_s, m_p, m_u are capacitance modulation ratios due to the signal, pump, and upper-sideband frequencies, respectively.

Performance optimization consists in assigning suitable values to these ratios. It can be shown that a maximum overall effi-

ciency condition corresponds approximately to the following expressions:[2]

$$m_s = \frac{0.25}{1 + (f_s/f_p)^{1/2} + (f_s/f_u)^{1/2}}$$
$$m_p = (f_s/f_p)^{1/2} m_s$$
$$m_u = (f_s/f_u)^{1/2} m_s$$

Substituting the corresponding frequency ratios, $m_s = 0.1325$; $m_p = 0.0617$; and $m_u = 0.0558$.

The power inputs under these conditions correspond to the Manley-Rowe relation: $P_s/P_p = f_s/f_p$, and, for a 50-volt breakdown varactor, these should be limited to $P_p = 35$ mW and $P_s = 7.5$mW.

The pump conversion efficiency, η_p, is given by

$$\eta_p = \frac{f_u\, m_s f_c - (f_p f_u)^{1/2}}{f_p\, m_s f_c + (f_p f_u)^{1/2}} \doteq \frac{f_u}{f_p}\left[1 - \frac{2(f_p f_u)^{1/2}}{m_s f_c}\right]$$

where f_c is the varactor cut-off frequency. If $f_u = 2.125$ GHz, $f_p = 1.845$ GHz, and $f_c = 120$ GHz, then $\eta_p = 0.9$, or the output power should be theoretically 0.5 dB below the pump input power. This treatment, however, neglects all the losses except those in the series resistance of the diode. In addition, input and output filter loss must be taken into account for the actual efficiency evaluation.

With the knowledge of the capacitance modulation ratios, the corresponding impedances for optimum power transfer can now be calculated:[3]

$$R_{IN,p} = R_s\left(1 + \frac{f_c}{f_p}\frac{m_s m_u}{m_p}\right) = R_s\left(1 + \frac{m_s f_c}{\sqrt{f_p f_u}}\right)$$

$$R_{IN,s} = R_s\left(1 + \frac{f_c}{f_s}\frac{m_p m_u}{m_s}\right) = R_{IN,p}$$

$$R_{OUT} = R_s\left(\frac{f_c}{f_u}\frac{m_s m_p}{m_u} - 1\right) = R_{IN,p} - 2R_s$$

For our frequencies and modulation ratios, $R_{IN} \doteq 9R_s$ and $R_{OUT} = 7R_s$.

For a varactor with $C_{MIN} = 0.75$ pF and $f_c = 120$ GHz, $R_s = 159/120\text{x}0.75 = 1.8$ ohms, and $R_{IN} = 16.2$ ohms, $R_{OUT} = 12.6$ ohms.

In addition to providing correct impedance levels, varactor capacitance must be resonated at both the pump and upper-sideband frequencies. A varactor with a total capacitance of 2.0 pF and series inductance of 0.4 nH has a capacitive reactance of 38.4 ohms at 1845 MHz and 32.1 ohms at 2125 MHz. These reactances are resonated by a short length of line at each port.

The line impedance must be as high as practicable to keep its length short and minimize variation with frequency over the band. An 80-ohm line (strip width 7 mils) represents a practical high-impedance limit, as narrower strips will present an intolerable line attenuation. Thus, a varactor imbedded in an 80-ohm line presents relative impedance of $Z_v = 0.203 - j0.48$ at 1845 MHz and $Z_v = 0.1582 - j0.401$ at 2125 MHz.

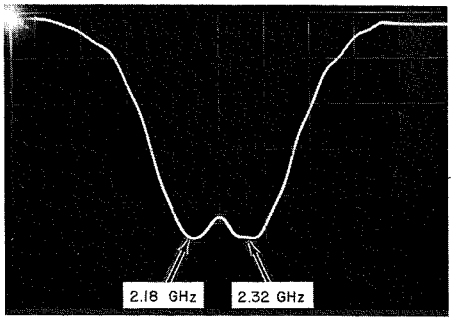

Fig. 1—Upconverter filter response.

A length of 80-ohm line, $l = 0.0732\lambda_p$ will transform varactor impedance to pure resistance of 13.2 ohms at 1845 MHz and $l = 0.0617\lambda_u$ to $R = 11.7$ ohms.

The filter tap-off points for $Q_L = 14.1$ can now be calculated from

$$l_T = (\lambda/2\pi)\sin^{-1}(\pi R/4Q_L Z_o)^{1/2} \doteq (\lambda/2\pi)(\pi R/4Q_L Z_o)^{1/2}$$

Substituting the values in the expression, $l_{Tp} = 0.0203\lambda_p$ and $l_{Tu} = 0.021\lambda_p$.

Final circuit and results

Double-tuned pump and output filters were designed first to work from and into a 50-ohm load. The line spacing was calculated using the approximate expression derived by Schwartzman[1] to give the required Z_{oo} and Z_{oe} values as discussed in the previous section. The filter response was measured and line spacing was then altered to bring it closer to the requirements. The swept frequency response of 50-ohm filters is shown in Fig. 1.

The tap-off on one side of the filter was then altered to correspond to the varactor impedance transformed by the length of the resonating line. The varactor was mounted in shunt configuration between the strip and the ground plane. Since the double-tuned filters were of the $\lambda/4$ short-circuited type, the varactor would have to operate at zero DC bias, unless blocking capacitors were incorporated. Thin-film overlay line capacitors were tried in the filters but proved troublesome. The final circuit used a small disc-shaped capacitor soldered to the base plate and the varactor mounted between the capacitor and the strip. A lead through the baseplate to the capacitor allowed for DC biasing of the varactor. No tuning of the UHF signal circuit was incorporated on the original substrate.

The upconverter is shown in Fig. 2. The following results were obtained with a MA4764 varactor ($C = 1$ pF at -6 volts and $f_c \cong 100$ GHz) mounted on a 33-pF disc capacitor:

$f_s = 0.405$ GHz	$P_s = 2$ mW	$P_s = 2.4$ mW
$f_p = 1.845$ GHz	$P_p = 11.6$ mW	$P_p = 11.6$ mW
$f_o = 2.25$ GHz	$P_o = 3.1$ mW	$P_o = 3.6$ mW
	$V_{bias} = -1.3$ volts	

With 2 mW signal input and with the double-stub tuner outside the substrate, the up-conversion gain was 1.9 dB and pump efficiency was 26.7% (—5.7 dB). With 2.4 mW input, the up-conversion gain decreased slightly to 1.8 dB while pump efficiency increased to 31% or —5.1 dB. Increasing the input power further brought very little increase in the output. Increasing the pump power to 55 mW, the output power was raised to 10 mW.

Taking into account the filter losses (1 dB each) and the mismatch loss, the pump efficiency was 2.0 dB lower than the calculated. Since the calculation was based on varactor loss only, the additional 2.0 dB loss must be attributed to the circuit loss. One can regard the circuit loss as causing the reduction of the effective cutoff frequency of the varactor. From the experimental conversion loss of 2.5 dB, using the pump efficiency expression, the effective cutoff frequency of 50.8 GHz is obtained. Thus, the additional circuit loss reduced the cutoff frequency by a factor of $120/50.8 = 2.36$, and the additional series resistance is then $1.36\ R_s$. This, although high, is not an unreasonable value.

Part of this loss is probably due to the generation of some lower sideband component. However, the lower-sideband current is small since the varactor is not resonated at this frequency and the filters in the return path further limit its value.

The pump rejection in the output was 15 dB. To improve this, a balanced hybrid-coupled approach could be used, with its higher cost and larger size as the tradeoff.

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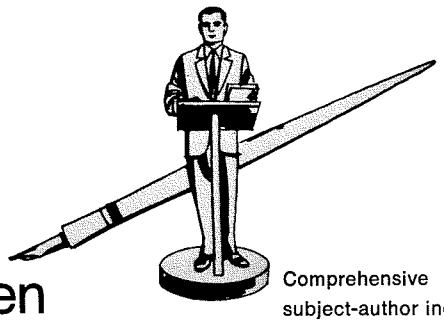

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CdS LASER CATHODE-RAY TUBES, An Experimental Pulsed—F. H. Nicoll (Labs., Pr) *RCA Review,* Vol. 29, No. 3; 9/68

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MANAGEMENT

MAINTAINABILITY — Engineering and Management—O. T. Carver (ASD, Burl) Maintainability and Reliability Engineering Course, George Washington University, Washington, D.C.; 12/68

PERSONAL EXCELLENCE, RCA Systems Approach to—B. D. Smith (ASD, Burl) American Society for Zero Defects, Wakefield, Mass.; 12/5/68

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REDUCTION PROCEDURES in Problem Solving—S. Amarel (Labs., Pr) 4th Systems Symposium, Case Western Research University, Cleveland, Ohio; 11/19-20/68

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FINISHING PROBLEMS, An Approach to —C. E. Salmon (MSR, Mrstn) *J. of the American Electroplates Society,* 11/68

NEW PLATING LANGUAGE, Efficiency Meter: Let s Talk a—W. P. Alina (EC, Som) *Products Finishing;* 11/68

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PHONONS Generated in Spin-Lattice Relaxation, Observation of—C. N. Anderson, E. S. Sabisky (Labs., Pr) *Physical Review Letters,* Vol. 21, No. 14; 9/30/68

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POLYMER STRUCTURE DETERMINATION, Nuclear Magnetic Resonance in—W. M. Lee (Labs., Pr) Trenton State College Chemistry Lecture Series, 12/11/68

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HETEROEPITAXIAL SILICON FILMS, Electrical Characteristics of—D. J. Dumin (Labs., Pr) AVS New England Section Mtg.; 12/4/68

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SPACECRAFT

EARTH RESOURCES Satellite—B. P. Miller (AED, Pr) American Society of Quality Control, Princeton University, Princeton, N.J.; 12/6/68

LUNAR MODULE AND APOLLO—P. Marcellos (ASD, Burl) Newton Kiwanis, and Billerica Rotary; 11/12 & 21/68

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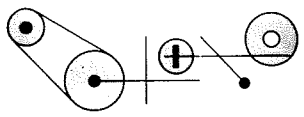
to RCA Engineers



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Method of Charging a Zinc Oxide Photoconductive Layer with a Positive Charge—E. C. Giaimo (Labs., Pr) U.S. Pat. 3,412,-242, November 19, 1968

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Means for Stabilizing Television Deflection Circuits—C. J. Hall (Labs., Zurich) U.S. Pat. 3,417,282, December 17, 1968

Process for Preparing a Magnetic Recording Element—H. Bauer (Labs., Pr) U.S. Pat. 3,418,161, December 24, 1968

Rare Earth Activated Lanthanum and Lutetium Oxy-Chalcogenide Phosphors—(Labs., Pr) U.S. Pat. 3,418,247, December 24, 1968

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Circuit Protection for a Television Receiver—N. W. Hursh, J. Stark (CED, Indpls.) U.S. Pat. 3,419,807, December 31, 1968

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Television Signal Converter Circuit—D. J. Carlson (CED, Indpls) U.S. Pat. 3,416,086, December 10, 1968

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Monostable Multivibrator Control—H. G. Seer, R. A. Dischert (CESD, Cam) U.S. Pat. 3,419,735, December 31, 1968

Phase and Frequency Correction System—R. N. Hurst, L. V. Hedlund (CESD, Cam) U.S. Pat. 3,409,736, November 5, 1968

Zigzag Radiator with Panel Reflector—M. S. Siukola (CESD, Cam) U.S. Pat. 3,409,893, November 5, 1968

INFORMATION SYSTEMS DIVISION

Electronic Computer with Program Debugging Facility—R. D. Smith, J. F. Callahan (ISD, Pennsauken) U.S. Pat. 3,415,-981, December 10, 1968

Magnetic Recording and Reproducing of Digital Information—G. V. Jacoby (ISD, Cam) U.S. Pat. 3,414,894, December 3, 1968

Controlling Interchanges between a Computer and Many Communications Lines—F. E. Brooks, Y. Rachovitsky, J. L. Lindinger, M. F. Kaminsky, R. A. Hammel (ISD, Cam) U.S. Pat. 3,413,612, November 26, 1968

Controlling Interchanges between a Computer and Many Communications Lines—J. L. Lindinger, Y. Rachovitsky (ISD, Cam) U.S. Pat. 3,409,878, November 5, 1968

Fast Critically Damped Motor Drive System—D. J. Poitras (ISD, Cam) U.S. Pat. 3,411,061, November 12, 1968

ADVANCED TECHNOLOGY

Non-Saturating Emitter-Coupled Multi-Level RTL-Circuit Logic Circuit—B. Walker (AT, Cam) U.S. Pat. 3,416,003, December 10, 1968

High Speed Digital Transfer Circuits for Bistable Elements Including Negative Resistance Devices—E. C. Cornish (AT, Cam) U.S. Pat. 3,412,265, November 19, 1968

DEFENSE COMMUNICATIONS SYSTEMS DIVISION

Video Recorder and/or Reproducer with Intermediate Tape Drive—A. Lichowsky (DCSD, Cam) U.S. Pat. 3,414,684, December 3, 1968

Information Handling Apparatus—M. Rosenblatt (DCSD, Cam) U.S. Pat. 3,413,448, November 26, 1968

ELECTROMAGNETIC AND AVIATION SYSTEMS DIVISION

Ground Speed and Time-to-Station Indicator for Use with DME—R. P. Crow (EASD, L.A.) U.S. Pat. 3,413,597, November 26, 1968

DEFENSE MICROELECTRONICS

Phantom OR Circuit for inverters having Active Load Devices—Y. L. Yao (DME, Som) U.S. Pat. 3,417,262, December 17, 1968

ADVANCED COMMUNICATIONS SYSTEMS LABORATORY

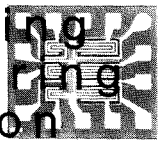
Error Corrector for Diphase Modulation Receiver—C. R. Atzenbeck (AVCS, W. Windsor) U.S. Pat. 3,417,333, December 17, 1968

MISSILE AND SURFACE RADAR DIVISION

Discharge Device Controlled by on Circuit and Off Circuit with Excessive Current-Limiting Means in Off Circuit—A. A. Gorski, C. Pappas (MSR, Mrstn) U.S. Pat. 3,414,825, December 3, 1968 (Assigned to U.S. Government)

Potentiometer Frequency Adjustment of a Tuned Circuit—W. R. Koch (MSR, Mrstn) U.S. Pat. 3,403,361, September 24, 1968 (Assigned to U.S. Government)

Continuing Engineering Education



The CEE program is designed to help the engineer update and advance his technical knowledge within his professional field and to correct any deficiencies he might have in his educational background. The CEE program offers a varied curriculum that will be continually updated and expanded. Each course is an in-depth study of a particular topic which will be offered in the plant at a time convenient to the particular location.

Descriptions of courses that are currently available were given in Vol. 14, No. 4 of the RCA ENGINEER (Dec. 1968, Jan. 1969). Courses E4 and E5, described below, are now available. Other courses will be covered in future issues of the RCA ENGINEER as they are developed.

E4—Transistor Circuits—Discrete and Integrated I

This course is the first in a four-course sequence designed to give the engineer an in-depth program in solid state circuitry. The course will give the background for the development of more advanced concepts in other courses. Topics to be covered include transistor fundamentals, biasing and stability, audio frequency power amplifiers, small-signal low frequency analysis, multiple transistor circuits and feedback circuits. *Course length,* twelve 2-hour sessions; *Background required,* an introductory knowledge of basic AC and DC circuit theory; *Text,* Schilling and Belove, *Electronic Circuits; Discrete and Integrated* (McGraw-Hill 1967)

E5—Transistor Circuits—Discrete and Integrated II

This course is a continuation of E4. Topics to be discussed in depth include integrated circuits, field effect transistors, low frequency response of RC coupled amplifiers, high frequency response of RC coupled amplifiers, tuned amplifiers and frequency response of feedback amplifiers. *Course length,* twelve 2-hour sessions; *Background required,* E4 or equivalent background which is a basic introductory knowledge of AC and DC circuit theory; *Text,* Schilling and Belove *Electronic Circuits; Discrete and Integrated* (McGraw-Hill 1967).

Professional Meetings

✲ Dates and Deadlines

Be sure deadlines are met—consult your Technical Publications Administrator or your Editorial Representative for the lead time necessary to obtain RCA approvals (and government approvals, if applicable). Remember, abstracts and manuscripts must be so approved BEFORE sending them to the meeting committee.

Calls for papers

APRIL 21-22, 1969: **Midwest Symposium on Circuit Theory,** University of Texas, Austin, Texas. **Deadline info: 3/3/69 (S & A) to:** J. K. Aggarwal, Dept. of EE, University of Texas, Austin, Texas 78712.

APRIL 22-25, 1969: **USNC/URSI-IEEE Spring Meeting,** Shoreham Hotel, Washington, D.C. **Deadline info: 2/1/69 (abst) to:** F. S. Johnson, S.W. Ctr. for Advanced Studies, POB 30365, Dallas, Texas 75230.

JUNE 9-10, 1969: **Chicago Spring Conf. on Broadcast & TV Receivers,** Marriott Motor Hotel, Des Plains, Illinois. **Deadline info: 2/10/69 (sum) to:** N. T. Watters, Zenith Radio, 6001 W. Dickens, Chicago, Ill.

JUNE 22-27, 1969: **Summer Power Meeting,** Sheraton Dallas Hotel, Dallas, Texas. **Deadline info: 2/15/69 (papers) to:** Tech. Conf. Svcs., 345 E. 47th St., New York, N.Y. 10017.

JULY 7-11, 1969: **Conference on Nuclear & Space Radiation Effects,** Penn. State Univ., J. Orvis Conf. Bldg., Univ. Pk., Penna. **Deadline info: 2/17/69 (sum) to:** E. A. Burke, Air Force Cambridge Res. Lab., Hanscom Field, Bedford, Mass.

JULY 20-25, 1969: **Engrg. in Medicine & Biology & Int'l Fed. for Medical & Biological Engineering Conf.,** Palmer House, Chicago, Illinois. **Deadline info: 2/1/69 (ms.) to:** Lawrence Stark, Univ. of Illinois, Chicago, Illinois.

AUG. 19-22, 1969: **Western Electronic Show & Convention (WESCON),** Cow Palace & San Francisco Hilton Hotel, San Francisco, Calif. **Deadline info: 6/25/69 (papers) to:** WESCON Office, 3600 Wilshire Blvd., Los Angeles, Calif. 90005.

AUG. 24-25, 1969: **ACM Symposium on Programming Languages Definition,** San Francisco, Calif. **Deadline info: 4/30/69 (papers) to:** Dr. James A. Painter, IBM Corp., Dept. 978, Bldg. 025, Monterey and Cottle Rds., San Jose, Calif. 95114.

AUG. 26-28, 1969: **ACM National Conf. & Exposition,** San Francisco, California. **Deadline info: 3/3/69 (papers) to:** Dr. Ward Sangren, Program Committee Chairman, ACM 69, P.O. Box 2867, San Francisco, Calif. 94126.

SEPT. 8-12, 1969: **Int'l Man-Machine Systems Symposium,** St. John's College, Cambridge, England. **Deadline info: 1/31/69 (abst) to:** W. T. Singleton, Applied Psychology Dept., Univ. of Aston in Birmingham, Birmingham, England.

SEPT. 16-19, 1969: **Solid State Devices Conf.,** Univ. of Exeter, Exeter, Devon, England. **Deadline info: 6/27/69 (syn) to:** P. C. Newman, Allen Clark Res. Ctr., Caswell, Towcester, Northamptonshire, England.

SEPT. 21-25, 1969: **Joint Power Generation Conf.,** White House Inn, Charlotte, North Carolina. **Deadline info: 5/9/69 to:** R. A. Budenholzer, Ill. Inst. of Tech. Ctr., Chicago, Ill. 60616.

OCT. 26-30, 1969: **Joint Conference on Mathematical and Computer Aids to Design,** Disneyland Hotel, Anaheim, California. **Deadline info: 5/1/69 (papers) to:** SIAM—1969 Joint MCAD Conf., 33 South 17th Street, Phila., Penna. 19103.

DEC. 8-10, 1969: **Third Conf. on Applications of Simulation,** International Hotel, Los Angeles, Calif. **Deadline info: 3/31/69 (abst), 9/15/69 (final ms.) to:** Philip J. Kiviat, Program Committee Chairman, The RAND Corporation, 1700 Main St., Santa Monica, Calif. 90406.

JAN. 25-30, 1970: **Winter Power Meeting,** Statler Hilton Hotel, New York, N.Y. **Deadline info: 9/15/69 (papers) to:** IEEE Hdqs., Tech. Conf. Svcs., 345 E. 47th Street, New York, N.Y. 10017.

JULY 5-10, 1970: **Summer Power Meeting,** Sheraton Boston Hotel, Boston, Mass. **Deadline info: 2/15/70 (papers) to:** IEEE Hdqs., Tech. Conf. Svcs., 345 E. 47th St., New York, N.Y. 10017.

Meetings

MARCH 12-14, 1969: **Microwave Technique Conf.,** Cologne (F.R. Germany). **Prog info:** H. H. Burghoff, Stresemann Allee 21, VDE-Haus, 6 Frankfurt/Main 70, F.R. Germany.

MARCH 17-19, 1969: **Seminar on Digital Processing of Audio Signals,** Swiss Federal Inst. of Tech., Zurich, Swit.

MARCH 24-27, 1969: **IEEE International Conv. & Exhibition,** Coliseum and N.Y. Hilton Hotel, New York, N.Y. **Prog info:** IEEE Hdqs., 345 E. 47th St., New York, N.Y. 10017.

MARCH 24-27, 1969: **Semiconductor Device Research Conf.,** Munich, F.R. Germany. **Prog info:** W. Heywang, Balanstrasse 73, 8 Muenchen 80, F.R. Germany.

MARCH 25-27, 1969: **Data Transmission Conf.,** Mannheim, F.R. Germany. **Prog info:** H. H. Burghoff, Stresemann Allee 21, VDE-Haus, 6 Frankfurt/Main 70, F.R. Germany.

MARCH 25-27, 1969: **Conf. on Lasers and Optoelectronics,** Univ. of Southampton, Southampton, England. **Prog info:** IEE, Savoy Place, London W.C. 2, England.

APRIL 15-18, 1969: **Int'l Magnetics Conf. (INTERMAG),** RAI Bldg., Amsterdam, The Netherlands. **Prog info:** U. F. Gianola, Bell Telephone Labs., Murray Hill, N.J.

APRIL 15-18, 1969: **Int'l Computer Aided Design Conf.,** Univ. of Southampton, Southampton, England. **Prog info:** IEE, Savoy Place, London W.C. 2, England.

APRIL 15-18, 1969: **Physics of Liquids,** University of East Anglia, Norwich. **Prog info:** The Meetings Officer, The Institute of Physics and The Physical Society, 47 Belgrave Square, London, S.W. 1.

APRIL 16-18, 1969: **Geoscience Electronics Symposium,** Marriott Twin Bridges Motor Hotel, Washington, D.C. **Prog info:** Maurice Ringenbach, Weather Bureau, ESSA, Gramax Bldg., Silver Spring, Md. 20910.

APRIL 16-18, 1969: **Region VI Conf.,** Del Webb's Town House Hotel, Phoenix, Arizona. **Prog info:** S. D. Robertson, 722 W. Frier Drive, Phoenix, Arizona 85021.

APRIL 21-25, 1969: **Conf. on Switching Techniques for Telecommunication Networks,** London, England. **Prog info:** IEE, Savoy Place, London W.C. 2, England.

APRIL 22-24, 1969: **Nat'l Telemetering Conf.,** Washington Hilton Hotel, Washington, D.C. **Prog info:** R. W. Rochelle, Code 710, NASA, Goddard S.F. Ctr., Greenbelt, Md. 20771.

APRIL 23-25, 1969: **Southwestern IEEE Conf. & Exhibition (SWIEEECO),** San Antonio Conv. Ctr., and Palacio Del Rio Hotel, San Antonio, Texas. **Prog info:** W. H. Hartwig, Univ. of Texas, EE Dept., Austin, Texas 78712.

APRIL 30-MAY 2, 1969: **Electronic Components Conf.,** Shoreham Hotel, Washington, D.C. **Prog info:** James O'Connell, ITT Hdqs., 320 Park Ave., New York, N.Y.

MAY 5-7, 1969: **Electrical & Electronic Measurement & Test Inst. Conf.-Instrument & Measurement Symp. (EEMTIC & IM),** Skyline Hotel, Ottawa, Ontario, Canada. **Prog info:** G. E. Schafer, National Bureau of Standards, Boulder, Colorado 80302.

MAY 5-8, 1969: **Internatl Microwave Symp.,** Marriott Motor Hotel, Dallas, Texas. **Prog info:** J. B. Horton, POB 5012, Texas Instr. Inc., Dallas, Tex. 75222.

MAY 5-8, 1969: **Int'l Congress on Instrumentation in Aerospace Simulation Facilities,** Polytechnic Inst. of Bklyn., Grad. Ctr., Farmingdale, New York. **Prog info:** C. R. Spitzer, MS-236, NASA Langley Res. Ctr., Hampton, Va. 23365.

MAY 6-8, 1969: **Conf. on Power Thyristors and Their Applications,** London, England. **Prog info:** IEE, Savoy Place, London W.C. 2, England.

MAY 6-8, 1969: **Congress on Nuclear Electronics, EURATOM Lab.,** Palazzo Dei Congressi at Stresa, Stresa, Italy.

MAY 7-9, 1969: **Int'l Joint Conf. on Artificial Intelligence,** Statler Hilton Hotel, Washington, D.C. **Prog info:** D. E. Walker, Mitre Corp., Bedford, Mass. 01730.

MAY 12-16, 1969: **Underground Distribution Conf.,** Disneyland Hotel, and Anaheim Conv. Ctr., Anaheim, Calif. **Prog info:** W. A. Thue, Florida Pwr. & Light Co., POB 3316, Miami, Fla. 33101.

MAY 13, 1969: **Vehicular Communications Systems Symposium,** International Hotel, Los Angeles, Calif.

MAY 13, 1969: **Extensible Languages Symp.,** Boston, Mass. **Prog info:** Carlos Christensen, Massachusetts Computer Associates, Inc., Lakeside Office Park, Wakefield, Mass. 01880.

MAY 13-16, 1969: **Ind. & Comm. Power Sys. & Elec. Space Heating & Air Conditioning Jt. Technical Conf.,** Statler Hilton Hotel, Baltimore, Maryland. **Prog info:** D. T. Michael, 3917 Millsbrae, Cincinnati, Ohio 45209.

MAY 14-16, 1969: **Spring Joint Computer Conf.,** Sheraton Boston Hotel, War Mem. Audit., Boston, Mass. **Prog info:** T. D. Bonn, Honeywell EDP, 200 Smith St., Waltham, Mass. 02154.

MAY 18-21, 1969: **Power Industry Computer Application Conf.,** Brown Palace Hotel, Denver, Colorado. **Prog info:** W. D. Trudgen, Gen'l Elec. Co., 2244 W. Desert Cover, Phoenix, Arizona 85029.

MAY 19-21, 1969: **Aerospace Electronics Conf. (NAECON),** Sheraton Dayton Hotel, Dayton, Ohio. **Prog info:** J. E. Singer, 5705 Coach & Four Drive East, Kettering, Ohio 45440.

MAY 19-21, 1969: **Off-Shore Technology Conf.,** Albert Thomas Conv. Ctr., Houston, Texas. **Prog info:** R. F. Nelson, Shell Oil Co., POB 60193, New Orleans, Louisiana.

MAY 21-23, 1969: **Electron, Ion, and Laser Beam Technology Symp.,** Green Audit, NBS, Gaithersburg, Md.

MAY 22-23, 1969: **Workshop on Applied Magnetics,** Sheraton Park Hotel, Washington, D.C. **Prog info:** O. Kiltie, Ballastran Corp., Fort Wayne, Ind. 46808.

MAY 26-28, 1969: **Laser Engineering and Applications Conf.,** Washington Hilton Hotel, Washington, D.C. **Prog info:** W. B. Bridges, Hughes Res. Labs., 3011 Malibu Canyon Rd., Malibu, Calif.

JUNE 3-5, 1969: **Conf. on Microelectronics,** Congress Theater, Eastbourne, Sussex, England. **Prog info:** IEE, Savoy Place, Victoria Embankment, London W.C. 2, England.

JUNE 9-11, 1969: **Int'l Communications Conf.,** Univ. of Colorado, Boulder, Colorado. **Prog info:** Martin Nesenbergs, Inst. for Telecommunication Sci., R-614, Boulder, Colorado 80302.

JUNE 17-19, 1969: **Electromagnet Compatibility Symp.,** Berkeley Cartaret Hotel, Asbury Park, N.J. **Prog info:** Charles Joly, Honeywell Inc., POB 54, Eatontown, N.J. 07724.

JUNE 17-19, 1969: **Computer Conf.,** Leamington Hotel, Minneapolis, Minn. **Prog info:** D. L. Epley, Dept. of EE, Univ. of Iowa, Iowa City, Iowa 52240.

JUNE 30-JULY 1, 1969: **Conf. on Applications of Continuous System Simulation Languages,** Sheraton-Palace Hotel, San Francisco, Calif. **Prog info:** Robert Brennan, IBM Scientific Ctr., 2627 Hanover St., Palo Alto, Calif. 94304.

AUG. 3-6, 1969: **The Eleventh National Heat Transfer Conf.,** Leamington Hotel, Minneapolis, Minn.

Engineering News and Highlights

Heilmeier Named Outstanding Young Electrical Engineer

Dr. George H. Heilmeier, Head of Solid-State Devices Research, has been selected as the Outstanding Young Electrical Engineer of 1968 by Eta Kappa Nu, the honorary electrical engineering society. He is being cited for his research in liquid crystals. Earlier this year he received international recognition as leader of an RCA laboratories research team that discovered a new electro-optic effect—"dynamic scattering"—making possible for the first time the electronic control of the reflection of light.

Eta Kappa Nu winners are chosen for their outstanding professional achievements, civic and social activities, and cultural pursuits. They must be no more than 35 years old, and have had a BS degree in Electrical Engineering, or the equivalent, for no longer than ten years.

Dr. H. J. Woll is Chief Defense Engineer

Irving K. Kessler, Vice President, DEP, appointed **Dr. Harry J. Woll** as Chief Defense Engineer of RCA Defense Electronic Products with offices in Moorestown, N.J. Dr. Woll will be responsible for DEP's Staff Engineering, Central Engineering, and Advanced Technology organizations. Prior to his new assignment, Dr. Woll was Chief Engineer at Aerospace Systems Division, Burlington, Mass., a position he has held since 1963. Before that assignment he was Manager of RCA DEP Applied Research, now Advanced Technology. Dr. Woll joined RCA in 1941 in Indianapolis and transferred to Camden, N.J. in 1946. During that time he was engaged in the development of advanced electronic circuitry for military and commercial applications. In the early 1950's he did pioneering work in transistor applications and was leader of the group that built RCA's first transistor digital computer.

Dr. Woll

A graduate of North Dakota State University with the BSEE, Dr. Woll did his graduate work at the University of Pennsylvania where he received the PhD in 1953. He was the first recipient of the David Sarnoff Fellowship for continued graduate study.

Dr. Woll is a member and officer of several major engineering societies and is a Fellow of the IEEE. He is a contributing author of the Handbook of Semiconductor Electronics and holds 20 patents in electronics. He also has been active in the Northeastern University Advisory Council while a resident of New England.

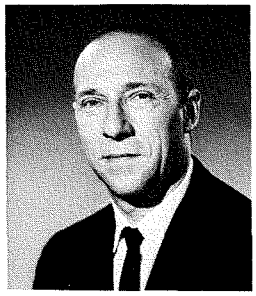
Falk, Olive and Petchel join Corporate Engineering Services

Messrs. Larry Falk, George Olive, and **George Petchel** recently joined the staff of Corporate Engineering Services. Mr. Falk was appointed Administrator, Course Development, and will be responsible for developing and coordinating course material for the Continuing Engineering Education Program. Mr. Olive was named Staff Engineer and will have corporate-wide responsibility for developing appropriate use of computers in engineering design. Mr. Petchel was appointed Administrator, Professional Engineering Services, and will be active in Corporate efforts to design and manufacture products free of radiation hazards.

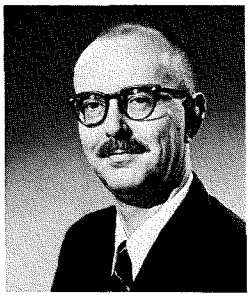
Mr. Falk received the BSME from City College of New York in 1942 and the MSEE from Harvard in 1947. From 1947 to 1953, he was a design engineer with Underwood Corp., Revere Corp., and Raytheon. In 1953 he joined RCA as a project engineer on the Bizmac program and was promoted to engineering leader of Bizmac System Operations Group in 1954. In 1959, he became engineering leader, Autodin Program and was named manager, Support Engineering, for this program in 1960. In 1963, he became manager of control and command equipment design, and in 1968, became the manager of project control in Digital Communications Equipment Engineering.

Mr. Olive was graduated from the University of Nebraska in 1949. From 1949 to 1959 he was with RCA Laboratories in Princeton, working principally on UHF and color television. From 1959 to 1961 he was a Staff Engineer with IEP in Camden. In 1961 he joined the Mobile Communications Department in Meadow Lands, becoming Manager of Systems Engineering in 1963. He holds several patents relating to television systems. He is a registered Professional Engineer and a member of IEEE.

Mr. Petchel received the BS in Physics in 1958 from St. Joseph's College, and has done graduate work at Penn and UCLA. Mr. Petchel joined RCA's advanced development group in Camden in 1958 where he worked on logic circuitry, display techniques, and bandwidth compression techniques. In 1959, he transferred to M&SR where he was concerned mainly with visual electrical processing. From 1959 to 1962, he was at the Van Nuys facility where his work was mainly devoted to displays and logic circuitry. After 1963, Mr. Petchel had various assignments in Applied Research, SEER, and CESD; the main portion of this work was devoted to electro-optics. While with CESD he developed a small, complete optical laboratory to service the division. Mr. Petchel is a member of Sigma Pi Sigma.



Larry Falk



George Olive

George Petchel

F. H. Krantz

Frederick H. Frantz is Chief Engineer for Aerospace Systems Division

John R. McAllister, Division Vice President and General Manager, Aerospace Systems Division, appointed **Frederick H. Krantz,** Chief Engineer.

Prior to his new appointment Mr. Krantz was Manager of the Command and Control Program Management Office at ASD. He joined RCA in January, 1968, after having been associated with IBM, Burroughs Corporation and Leeds and Northrop Company in a number of research and development, engineering and management capacities.

Mr. Krantz received the BSEE from Drexel Institute, Philadelphia, and the MSEE from the University of Pennsylvania. He is a member of the Institute of Electrical and Electronic Engineers and holds a number of patents in electronic devices and circuitry.

Staff announcements

Operations Staff

Chase Morsey, J., Executive Vice President, Operations Staff has appointed **George C. Evanoff** as Staff Vice President, Corporate Planning, for RCA.

Corporate Engineering Services

W. C. Morrison, Staff Vice President, Corporate Engineering Services appointed **G. A. Olive** as Staff Engineer.

RCA Sales Corporation

D. L. Mills, Senior Executive Vice President, Consumer Products and Components announced the election of **B. S. Durant,** Chairman of the Board, and **D. P. Dickson,** President.

Services

J. F. Murray, Division Vice President, Government Services, has appointed **G. Denton Clark,** Division Vice President, Range Projects.

L. G. Borgeson, Division Vice President, Consumer Products Service has appointed **R. W. Redecker,** Division Vice President, Operations and Marketing.

General Counsel

Robert L. Werner, Executive Vice President and General Counsel has appointed **J. D. Hill,** Staff Vice President and Trade Regulation Counsel.

Missile Test Project

D. R. Hill has been named Project Manager of the RCA Missile Test Project at Patrick Air Force Base.

A. W. Wren, Jr. has been appointed Manager of Technical Operations for the RCA Missile Test Project. **Gaver M. Powers** has been appointed Manager of Technical Support at the RCA Missile Test Project.

Defense Electronic Products

I. K. Kessler, Vice President, Defense Electronic Products has announced the following appointments: **J. F. Burlingame,** Division Vice President and General Manager, Defense Communications Systems Division; **S. N. Lev,** Division Vice President, Defense Manufacturing; **P. A. Piro,** General Manager, Missile and Surface Radar Division; **D. Shore,** Manager, Advanced Programs; and **H. J. Woll,** Chief Defense Engineer, Defense Engineering.

D. Shore, Manager, Advanced Programs announced the organization of Advanced Programs as follows: **N. A. Montone,** Manager, Advanced Planning; **D. Shore,** Acting Manager, SEER.

J. F. Burlingame, Division Vice President and General Manager of RCA M&SR appointed **Charles C. Botkin** as Manager of Equipment Programs; and **Wesley R. Frysztacki** as Manager of Operational Systems.

S. N. Lev, Division Vice President and General Manager of Defense Communications Systems Division (now Division Vice President, Defense Manufacturing) named **Leo Slutzky** as Manager of Operations Control.

J. R. McAllister, Division Vice President and General Manager Aerospace Systems Division has appointed **F. H. Krantz** as Chief Engineer, Engineering Department.

Information Systems Division

E. S. McCollister has announced the organization of Marketing as follows: **W. H. Bowman,** Manager, Institutional Relations; **L. E. Donegan,** Division Vice President, Marketing Operations; **W. J. Gallagher,** Division Vice President, Executive Marketing Relations; **F. M. Hoar,** Division Vice President, Advertising and Public Affairs; **J. J. MacIsaac,** Manager, Marketing Planning; **J. P. Macri,** Manager, Marketing Administration and Systems Coordination; **P. B. Reed,** Division Vice President, International and Special Account Sales; **D. L. Stevens,** Manager, Product and Programming Planning.

L. E. Donegan, Division Vice President, Marketing Operations has announced the organization of Marketing Operations as follows: **J. P. Boyle,** Division Vice President, Northeastern Region; **L. E. Donegan,** Acting Marketing Programs; **E. A. Henson,** Manager, Central Region; **J. E. Johnson,** Division Vice President, Executive Marketing Relations; **J. N. Landon,** Division Vice President, Eastern Region; **W. R. Lonergan,** Division Vice President, Government Marketing; **M. Posin,** Manager, Western Region.

Instructional Systems

M. H. Glauberman, Director, Instructional Systems, has announced the organization of Instructional Systems as follows: **R. W. Avery,** Manager, Engineering; **M. P. Connelly,** Manager, Materials; **G. R. Jensen,** Manager, Marketing; **J. D. Leer,** Manager Personnel; **C. G. Lindsey,** Manager, Software Development; **B. J. Pine,** Manager, Product Planning; **R. K. Sparks,** Manager, Financial Operations.

Awards

Missile and Surface Radar Division

The following engineers were nominated by their supervision and cited by CETEC for the Technical Excellence of their performance during the third quarter of 1968: **N. R. Landry**—for conception, formulation, and design of a compact S-band latching ferrite phase shifter; **R. Lieber**—for superior performance as technical director of the AN/TPQ-27 program during both the proposal stage and the Contract Definition Phase; **W. J. O'Leary**—for significant contributions in the field of reliability engineering through practical application of advanced performance prediction techniques; **W. H. Schaedla**—for outstanding technical accomplishment in the analysis of phased array element impedance characteristics and associated design of array radiating elements and radomes for superior impedance match over wide scan angles; and **A. R. Wentz**—for contributions in developing a technically outstanding IFF subsystem design concept for application in the AN/TPQ-27 system.

Aerospace Systems Division

Richard J. Geehan, Senior Member Technical Staff, Data Processing Engineering, was selected as the Engineer of the Month for June, 1968, in recognition of his accomplishments on the Main Memory for the Airborne Data Automation (ADA) System; **John Dubbury,** Engineering Scientist of Electro-Optics and Controls Engineering was selected as the Engineer of the month for July, 1968, in recognition of notable results achieved in his analytical design of the Project "D" stabilization system; **Dr. Norman D. Mills,** Engineering Scientist of Advanced Systems and Technology was selected as the Engineer of the Month for August, 1968, in recognition of his major contributions to the design and fabrication of a solid-state mosaic IR detector; **Frank A. Barnes,** Senior Engineering Scientist of Tactical and Space Programs, was selected as the Engineer of the Month for September, 1968, for creating, organizing, and producing the RCA Electro-Optics Handbook; and Miss **Frances T. Kelley,** Senior Project Member, Technical Staff, was selected as the Engineer of the Month for October, 1968, for her contribution to the software effort on the Airborne Data Automation System (ADA) program.

The team of **John M. Anderson, George E. Anderson, Jerrold H. Budiansky, Terry J. Donofrio, Thomas J. Quinn, John C. Foran, Robert J. Kampf, Demetrios Lambropoulos, Donald E. Mahoney, Lawrence H. Ryan, Thomas A. Farrington,** and **Frank A. Tartaro** from the ECM Systems and Microwave Design groups of Radar Engineering and the Tactical and Space PMO has been given the Team Award for the Month of June, 1968, for their performance on the IR&D program: "Microwave Integrated Circuit Applications to Electronic Warfare."

The A-7 Scan Converter Design team of **Jerome C. Holland, John J. Klein, Edward Kramer, Cliffort E. LaCount, Daniel K. Livingston, Nicolaos Meliones, Knowlton Miller, Larry L. Rumbaugh, William K. Shubert, Arthur J. Smith, Ray G. Spiecker,** and **Paul T. Tremblay** from Electro-Optics and Controls Engineering has been given the Team Award for the month of August, 1968, in recognition of the results achieved on the A-7 Scan Converter Display program.

The team of **Dominic A. Aievoli, Raymond K. Gorman, Michael P. Guba Robert E. Ironfield, Richard L. Jameson, Edward G. Laugininger, Herbert W. Varley,** and **Richard A. Welter** from System Support Engineering has been given the Team Award for the month of October, 1968, for its outstanding work in the design, fabrication, integration and operation of the AGE equipment for a classified electro-optical system.

Professional Activities

Magnetic Products Division

A. L. Stancel has been named by the Institute of Electronic and Electrical Engineers to serve on the United States Standards Committee C-98. This committee establishes and publishes standards on video tape that is used extensively by television stations.

Corporate Engineering Services

The American Society of Mechanical Engineers cited **Samuel H. Watson,** Manager, Corporate Standardizing "for his valued services in the development of standards and codes sponsored by the society."

Frank W. Dickel, Standards Engineer, was a guest speaker at an American Management Association seminar. He spoke on the "Application of Electronic Data Processing to Maintenance."

Astro-Electronics Division

Yvonne Brill, is the Secretary of the Propellent Expulsion Working Group under Liquid Rocket Technical Committee of AIAA. **L. E. Golden** is the Section Educational Chairman of the Princeton Section of the AIAA. **G. Barna** is on the AIAA Technical Committee on Sensor Systems; he is chairman of Task Group.

Information Systems Division

Harold N. Morris, Manager—Engineering, Palm Beach Gardens, was the recipient of a coveted honor conferred by the University of Florida. Mr. Morris was cited for his efforts on behalf of the school. This is only the second award of this type given out by the university to date.

Aerospace Systems Division

Frank Congdon, Manager, M.I.S., received the Distinguished Service Award from the Systems and Procedures Association.

RCA to train jobless in four cities

At centers in Camden, Chicago, Los Angeles, and Newark, RCA Service Company has established 18-month programs to train about 400 jobless as television repairmen. The programs will consist of courses in basic education and social development, in addition to intensive vocational instruction.

F. X. Diamond, program director appointed **Dudley V. Simms** to manage the Newark facility, **Willis Nummerdor** to manage the Chicago facility, **Frederick R. Carpenter** to manage the Los Angeles facility, and **John B. Williams** to manage the Camden facility. The Chicago and Los Angeles centers will each accept 120 trainees; Camden and Newark will accept 80 each.

This "four-cities program" is being operated by the Service Company under a $2.5 million contract with the Department of Labor. RCA anticipates spending an additional $1 million as part of a company-wide program to help ease urban unemployment problems.

Technical writing—easy as 1, 2, 3

Have to produce a 50-page report by the end of the week? Crank out a 500-page proposal by Monday? Grind out a 4000-word thesis by the end of the semester? A new system introduced recently by Techniprose, Inc., allows you to get 10, 50, or 500 pages between two covers and play 18 holes of golf while you're doing it!

The new system—called SIMP (Scientific Integrated Modular Prose)—is based on lists or tables of phrases similar to those shown in the accompanying *writing kit.* Dr. Ira Verbalmonger, President of Techniprose and developer of SIMP, claims that the kit can be used to write thousands of perfectly balanced, grammatically correct sentences, studded with the "in words" of your technology.

Obviously, the tables and methodology presented here have been grossly simplified to explain the workings of the system. A variety of software packages are offered that range in complexity from four or six 50-phrase tables to programs runnable only on the most sophisticated hardware presently available.

The most advanced program, for machines with core storage in excess of 500K, is the 64/200 (LG). By the designation system adopted by Techniprose, this indicates 64 tables of 200 phrases each—including one table of obscure references and one of irrelevant footnotes. The parenthetical LG denotes that any phrase may be presented in Latin or Greek at will, the translation being triggered by a 12-9-7-4 punch in cc-80 (or 12-7-9-3 for Greek). Tables of untried formulae and of random punctuation are also included.

[**Editor's note:** the complete article "New SIMP Program makes Technical Writing Easy as 1-2-3-4-5-6," by Raymond A. Deffry appeared in the December 1968 issue of *Software Age.*]

Technical writing kit

This technical writing kit is based on the SIMP writing system. Using this kit, anyone who can count to 10 can write up to 40,000 discrete, well-balanced, grammatically correct sentences packed with aerospace terms.

To put SIMP to work, arrange the modules in A—B—C—D order. Take any four-digit number, 8751 for example, and read Phrase 8 off Module A, Phrase 7 off Module B, etc. The result is a SIMP sentence. Add a few more four-digit numbers to make a SIMP paragraph.

After you have mastered the basic technique, you can realize the full potential of SIMP by arranging the modules in D—A—C—B order, B—A—C—D order, or A—B—C—D order. In these advanced configurations, some additional commas may be required.

SIMP Table A

1. In particular,
2. On the other hand,
3. However,
4. Similarly,
5. As a resultant implication,
6. In this regard,
7. Based on integral subsystem considerations,
8. For example,
9. Thus,
0. In respect to specific goals.

SIMP Table B

1. a large portion of the interface coordination communication
2. a constant flow of effective information
3. the characterization of specific criteria
4. initiation of critical subsystem development
5. the fully integrated test program
6. the product configuration baseline
7. any associated supporting element
8. the incorporation of additional mission constraints
9. the independent functional principle
0. a primary interrelationship between system and/or subsystem technologies.

SIMP table C

1. must utilize and be functionally interwoven with
2. maximizes the probability of project success and minimizes the cost and time required for
3. adds explicit performance limits to
4. necessitates that urgent consideration be applied to
5. requires considerable systems analysis and trade off studies to arrive at
6. is further compounded, when taking into account
7. presents extremely interesting challenges to
8. recognizes the importance of other systems and the necessity for
9. effects a significant implementation to
0. adds overriding performance constraints to

SIMP Table D

1. the sophisticated hardware
2. the anticipated third generation equipment
3. the subsystem compatibility testing
4. the structural design, based on system engineering concepts
5. the preliminary qualification limit
6. the philosophy of commonality and standardization
7. the evolution of specifications over a given time period
8. the greater flight-worthiness concept
9. any discrete configuration mode
0. the total system rationale

Frank Strobl

F. J. Strobl is new Trend Editor

Mr. Frank J. Strobl comes from the Astro-Electronics Division to assume the position of Administrator, Technical Publications. In this capacity, Mr. Strobl's major responsibility is Editor of TREND (The Research and Engineering News Digest). He is also responsible for expanding the use of RCA technical articles in external publications. In his new post, Mr. Strobl reports to **W. O. Hadlock,** Manager, Technical Publications, Corporate Engineering Services.

TREND is published to provide RCA scientists and engineers with a better understanding of the Corporation's activities including current and future technical projects and engineering management objectives. TREND covers professional activities, scientific and engineering advances, policies, and new markets.

Mr. Strobl received the AAS in Electrical Technology from New York City Community College in 1954. In addition to taking further courses in Engineering, Mr. Strobl is pursuing the BA at the evening division of Rutgers University. His early experience included two years in the U.S. Army as an Instructor on the NIKE Missile System. From 1958 to 1960, he was a customer engineer for IBM, and from 1960 to 1962, he was a technical writer for the Bendix Corp. where he became a lead writer preparing technical manuals on the B-58 flight control system. After writing assignments with Miles-Samuelson, Inc., and Royer and Roger, Inc., Mr. Strobl joined the Astro-Electronics Division of RCA in 1963, where he has served as project writer for the New Moons Program and the Navy Navigational Satellite Program. Mr. Strobl also has had various writing assignments on the TIROS, TOS, Ranger, and SLRV programs.

RCA scientist to teach in Brazil

Dr. Richard Williams, Head of Insulator Physics Research at RCA Laboratories, has been awarded an international teaching grant by the U.S. Department of State to lecture and conduct research in physics at the Sao Carlos School of Engineering, Sao Paulo, Brazil. Dr. Williams will participate in the educational exchange program conducted by the State Department's Bureau of Educational and Cultural Affairs under the Fulbright-Hays Act.

EC engineers receive awards

Three engineers—**Joseph J. Bland, Raimund Sikora,** and **Thomas P. Garrison**—of the Microwave Devices Operations Department and Special Electronic Components in Harrison, N.J. recently received Engineering Recognition Awards for their achievements in 1968. The awards were presented by **C. H. Lane,** Division Vice-President and General Manager of Industrial Tube Products and **Dr. A. M. Glover,** Division Vice-President, Technical Programs. The winners were chosen by all the engineers themselves in a carefully conducted poll.

Joseph J. Bland was chosen "for his outstanding contribution to the improvement and characterization of a special high-temperature alloy for thermoelectric generators. He has conceived and developed new and unique methods for defining the bond system between silicon-germanium and silicon-molybdenum alloys with respect to mechanical integrity, electrical and thermal properties." Raimund Sikora, was chosen for "maintaining a high degree of technical accomplishment through his keen analysis, initiative, and thoroughness in his service to the product lines. Outstanding among his achievements was the design of a low-cost pencil tube cavity for use in commercial transponders." Thomas P. Garrison, was chosen for "the outstanding technical competence he demonstrated as production engineer on the solid-state three-band local-oscillator program. He was instrumental in putting into production this new and complex device and in meeting rapidly increasing production schedules against excessive odds imposed by critical part shortages, new facilities, and inexperience personnel."

The *RCA Review* is published quarterly. Copies are available in all RCA libraries. Subscription rates are as follows (rates are discounted 20% for RCA employees):

	DOMESTIC	FOREIGN
1-year	$4.00	$4.40
2-year	7.00	7.80
3-year	9.00	10.20

Defense Electronic Products

A. Feller: from Engr. Rcsh. AA to Leader, Des. & Dev. Eng. (J. G. Smith, Des. & Dev. Engrg., Camden)

Electromagnetic & Aviation Systems Division

J. Hayes: from Leader, D&D Engrg. Staff to Staff Engrg. Scientist (F. L. Worth, Van Nuys)

R. Yule: from Sr. Mbr., Engrg. Staff to Leader, D&D Engrg. (J. Chambers/F. Worth, Van Nuys)

C. Eggert: from Prn. Mbr., Engrg. Staff to Leader, D&D Engrg. (H. Hite/F. Worth, Van Nuys)

H. Hite: from Leader, D&D Engrg. to Mgr., Elect. D&D (F. L. Worth, Van Nuys)

J. Chambers: from Leader, D&D Engrg. to Mgr., Elect. D&D (F. L. Worth, Van Nuys)

R. Lewis: from Leader, D&D Engrg. to Mgr., Elect. D&D (F. L. Worth, Van Nuys)

Information Systems Division

A. Sheng: from Engineer to Leader, Des. & Dev. Engrs. (J. N. Marshall, Circuit Design, Camden)

P. A. Rey: from Engineer to Leader, Des. & Dev. Engrs. (H. Nelson, Power Supplies, Camden)

H. R. Kaupp: from Engineer to Leader, Des. & Dev. Engrs. (S. Basara, Circuits, Memories, Power Supplies, Camden)

N. Garaffa: from Engineer to Leader, Design & Development Engineers (B. I. Kessler, Camden)

Dr. Schade honored by IEEE

Dr. Otto J. Schade, Jr., of Electronic Components is one of the four men cited by the IEEE in 1969 for outstanding contributions in the fields of professional interest of concern to IEEE and its membership.

Dr. Schade receives the *Vladimir K. Zworykin Award* of IEEE "for broad technical contributions to the electronics and optics of television." Established in 1952, this award honors technical contributions in the field of electronic television.

Dr. Maurice Apstein, Associate Technical Director at the Harry Diamond Laboratories of the U.S. Army, receives the *Harry Diamond Memorial Prize.*

Harry William Houck of Wallpack, New Jersey, receives the *Morris E. Leeds Award* "for outstanding contributions to the field of radio-frequency instrumentation."

Robert Harmon Rediker, professor of electrical engineering at the Massachusetts Institute of Technology, receives the *David Sarnoff Award* "for contributions to semiconductor device research and injection lasers." The David Sarnoff Award of the IEEE is funded by the Radio Corporation of America and given for outstanding contributions in the field of electronics. Each of the awards consists of a certificate and cash honorarium, and each will be presented later in 1969 at an IEEE meeting of wide scope and interest in the appropriate field.

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The Editorial Representative in your group is the one you should contact in scheduling technical papers and announcements of your professional activities.

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Defense Electronic Products

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