Digital Systems and Computer Control

All of us are very familiar with the phenomena of the new completely replacing the old. Not so familiar, but sometimes with a more startling result, is the application of a new technology to an older product. A case in point is described in the accompanying articles.

Electronic computers, and digital control, and information systems, in general, offer a great opportunity for product quality improvement both by aiding product design and by permitting more complete analysis and control of production process. This latter area is just beginning to be explored. We hear that substantial progress in computer-controlled factories is being made in continuous-flow, process industries such as oil refineries, chemical plant, and steel mills. In discrete item assembly operations, however, flow of product is not so easily defined, instrumentation is difficult, and process assembly steps are often many and involved. But even in such industries, the technology needed to move ahead toward computer control is available. Based on this conviction, an exploratory step in computer controlled automatic testing and process control was decided upon for color picture tubes, the result of which is reported in a series of articles in this issue. This is a learning step. The costs are high and the benefits expected must be substantial. How far, and how rapidly this approach will be extended cannot be predicted, but it is conceivable that it will ultimately be integrated back to incoming raw materials.

Much of the knowledge that has been developed in digital control and communications is space-age technology. Application to other fields is desirable "fallout" but does present problems of introduction to areas where the technology has not been developed. The project team approach appears to be almost a necessity to accomplish this objective, and as in the case of the Automatic Test and Process Control System developed for color picture tubes, may extend across Divisional lines. We extend our thanks to ASD at Burlington for their part in the design and building of the digital hardware to support this system.

The importance of digital systems and computer control is further evidenced by many of the other articles in this issue.

H. R. Seelen, Division Vice President and General Manager
Television Picture Tube Division
Electronic Components
Harrison, N. J.

Our Cover

. . . features the achievements of engineers at Electronic Components, Marion, Indiana, and Aerospace Systems Division, Burlington, Massachusetts. In the top photo, color picture tubes are being shuttled by conveyor to a test station of the new Autotest system at Marion, Indiana. In the bottom photo, automatic test systems are being readied for field army use at Burlington, Mass.

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RCA Engineer

A technical journal published by
RCA Product Engineering 2-8, Camden, N.J.

RCA Engineer articles are indexed annually in the April-May Issue and in the "Index to RCA Technical Papers."

• To disseminate to RCA engineers technical information of professional value • To publish in an appropriate manner important technical developments at RCA, and the role of the engineer • To serve as a medium of interchange of technical information between various groups at RCA • To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions • To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field • To provide a convenient means by which the RCA engineer may review his professional work before associates and engineering management • To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

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With emphasis this issue clearly on advanced computer-control techniques and automated testing, it would be "nice" if we could say that data from the readership survey was keypunched, processed by a Spectra 70/45, and reduced to a finite set of clearly defined answers. · · · It would be "nice", if true, but the simple unsophisticated truth is that your survey returns are now badly bent, folded, and sprinkled liberally with coffee stains, fingerprints, perspiration, and an occasional tear.

Yes, gratified by the pat on the back that the total results gave us, but far from satisfied, we hand-sorted and read every survey—2,250 of them—paying particular attention to constructive suggestions and where they came from. In most areas, you have supported our convictions; however, in some areas, we have set new goals for the future based on your suggestions.

Because your journal is exclusively "by and for the RCA engineer," it is appropriate to discuss our conclusions with you. First and foremost, the *RCA Engineer* must remain broad in its purpose and unique as a technical publication representing many technical activities in RCA and embracing many skills. While we strive toward this ideal, we cannot be everything to all readers. Many of our issues have emphasized electrical engineering subjects—sometimes to the exclusion of the mechanical, chemical, or manufacturing engineer. Justifying this approach on the basis that we are an electronically oriented company does not solve the problem totally for those excluded. Presently, our planning includes future issues devoted to mechancial engineering, interdisciplinary aspects of modern engineering, and little known engineering activities throughout RCA; further, we hope to be able to represent these activities in every issue.

Underlying many of the survey returns seemed to be the reader's appreciation of being kept better informed—both technically and managerially. Several readers want articles on business planning; others want to be better informed on RCA policy. These areas have been pursued in our "Engineer and the Corporation" series; and we will accelerate our quest for such papers of professional value.

A minority of readers favor a more theoretical approach; however the large majority prefer technical articles broader in scope, not too detailed, and more interesting and understandable. To this end, the *RCA Engineer* will concentrate on more good survey papers, occasional tutorial papers, and (in the majority of cases) articles that both inform and teach. Emphasis will be given to new sciences and fields of engineering, new developments, new techniques, and advanced development and research. As always, articles will be accepted on the basis of brevity, wide interest, timeliness, and value to the readers.

A major goal—to be pursued by the Editors, Ed Reps, TPA's and (most important) authors—must be to produce a journal that is truly "by and for the RCA engineer." Our common objectives can be met only by mutual understanding. We welcome your ideas, your suggestions, and your articles—to produce your magazine.

Future Issues

The next issue of the *RCA Engineer* discusses computer use by RCA engineers. Some of the topics to be covered are:

Computers in acoustic research

Management Information Systems

Time sharing

Introduction to FORTRAN

Computer-aided transistor design

Differential equations on the computer

Electronic circuit analysis by computer

Network and functional analysis by computer

Discussions of the following themes are planned for future issues:

Electron tubes: power, conversion, color TV

General review of computers

Product and system assurance; reliability, value engineering

Microwave devices and systems

Interdisciplinary aspects of modern engineering

Lasers

RCA engineering on the West Coast

What automatic testing means to the engineer

B. V. Dale

The Engineer and the Corporation

The era of the automatic factory has arrived for the electronics industry. Although automation in the electronics industry is behind the automotive and chemical industries, automatic assembly and test equipment is beginning to appear on the factory floors of electronic manufacturers. Furthermore, its use is going to increase because manufacturers will have to automate to survive.

THE MOST persuasive arguments for automation are economic. A large corporation recently reported that the cost for automatic testing of a typical computer circuit module was between 3c and 7c compared with 60c to $1.90 for manual testing. They also reported that the cost for a release to plan and facilitate an automatic test was about $30, compared with $500 for a manual test.

ROLE OF THE PRODUCT DESIGNER

There is a difference between designing products to be assembled and tested manually and designing products to be made in an automated factory. In the latter case, the product and the manufacturing process must be created as a unit. The product engineer and manufacturing engineer must work as a team to design not only the product, but the manufacturing techniques and equipment needed to produce it. This team is called upon to design a *system* that will satisfy a *demand* at a predetermined *cost* and at a specified *time*. Thus, the end product of engineering is not simply an equipment prototype, but a product that can be manufactured within the time and cost constraints and will provide reliable service throughout its life.

The automated factory erases the division between manufacturing and engineering because of the increasing complexity of test requirements to insure initial performance and reliability of complex new products. Successful operation of an automated electronics factory requires total involvement of the engineer. He must resolve trade-offs between automatic and manual test and assembly operations.

The very fact that a product is to be made in an automated factory imposes immediate constraints on product design. For example, for one particular product, a recent study showed that to realize a cost reduction from computer-controlled automatic test equipment, certain ground rules had to be followed in circuit layout. If these rules had not been followed, testing costs would have been substantially higher because more off-line manual testing would have been required. Four of these rules were as follows:

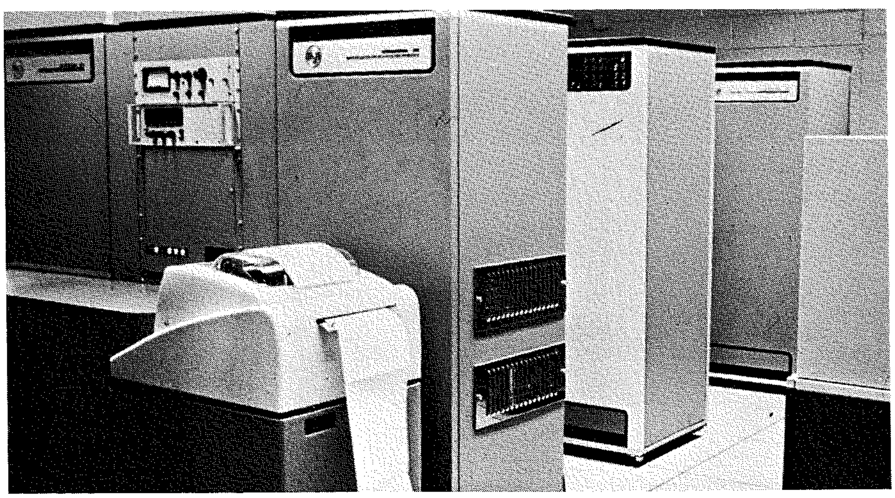
1) A transistor output from a module had to be brought out to a test point—otherwise computer-generated diagnostics would have been unable to determine which of two modules was faulty and both would have to be replaced, doubling rework costs.

2) When transistors, modules, or diodes were operated in parallel, their interconnection had to be made through adjacent pins on the board so that each was available for test—otherwise one "good" component could have successfully carried the load under test but failed later in service.

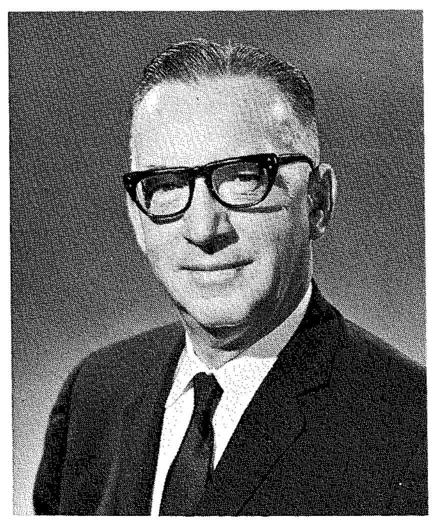
Reprint RE-14-2-14
Final manuscript received June 10, 1968.

B. V. DALE, Mgr.
Automatic Test and Measurement Systems
Corporate Staff Manufacturing
Camden, N.J.

received the BSEE from Drexel Institute of Technology in 1932. He came to RCA Victor the same year as a Test Maintenance man. In the following years he rose rapidly in the field of Quality Control, becoming Superintendent of this activity in 1944. From 1945 to 1952 he held various managerial posts in Manufacturing Methods, Engineering Services, Transformer Development Engineering, Test Measurements Equipment Development, and Manager of Parts Engineering. In 1953 Mr. Dale was made Manager, Engineering Section, Electronic Components Operating Division, Tube Department when this activity was transferred from RCA Victor Division. In 1956 he was appointed Chief Engineer of the Components Division. In 1958 Mr. Dale was named Manager, Module Engineering, Semiconductor and Materials Division, Electronic Components. From 1959 to 1965 Mr. Dale was Manager of EC's Microelectronics Activity in Somerville, N.J.; he was then named to his present post of Manager, Automatic Test and Measurement Systems Department in the Corporate Staff Manufacturing activity.



Computer-controlled integrated-circuit tester.



3) A definite reset had to be provided for each circuit output so that its state could be defined solely from a configuration of input *ones* and *zeros*.
4) Special circuits, such as RC timing networks and slow-speed elements, had to be isolated from basic logic functions. (The special circuits could be tested off-line after the logic had been checked out automatically.)

The product-design engineer plays a key role in establishing test criteria that will verify manufacturing performance, not design adequacy. He determines design center and worst-case values, and specifies acceptable tolerances. These tolerances must be reasonable in terms of the expected variances of production components, and set no more tightly than necessary to insure that assemblies will function properly as a system.

THE ENGINEER AS A DESIGNER OF ATE

The engineer can become involved with Automatic Test Equipment (ATE) in several capacities; the most direct involvement is that of an ATE designer. He can participate in the design of automatic test equipment for the space agency, the armed forces, or industry, including factory test equipment to be used within RCA. In many cases, the design of RCA factory test equipment entails development of new approaches to testing while the actual equipment design is being carried out by technical engineers within the manufacturing organization. Development of new mechanical equipment to facilitate high throughput at test stations is generally within the purview of the ATE engineer.

Greater participation of engineers in the design of ATE will be required for the development of computer-controlled test equipment and test plans for equipment that uses large scale integration concepts. Some engineers will find rewarding careers in following the product through the factory to see that it is not only functional but also manufacturable. Test and measurement engineering groups will plan test systems, develop automatic test equipment and basic software, enforce product design/facilities compatibility, and provide a permanent reservoir of test technology.

OBJECTIVES OF FACTORY TESTING

The principal objective of factory testing is to insure that fabrication and assembly operations have been performed according to plan, that no defective components have been used, that components have not been damaged in handling, and that workmanship defects (such as unsoldered joints) are not present to degrade product performance. However, because test data are systematically acquired and analyzed, test results can help engineers improve product designs and production processes. Test data properly arrayed can also provide valuable clues to the troubleshooter, permitting him to utilize his time more efficiently and reducing the possibility of equipment damage due to excess handling.

A well-contrived test plan consists of systematic acquisition of test data that requires progressive exercise of each level of assembly from basic part to final product, permitting the detection of defective parts and assemblies early in the manufacturing process when minimal labor has been expended on them and when their removal will do the least damage to the product.

Test data is a natural by-product of ATE in a well-conceived test plan. This systematic acquisition of test data can make report preparation easier, and could become part of the total package delivered to the customer.

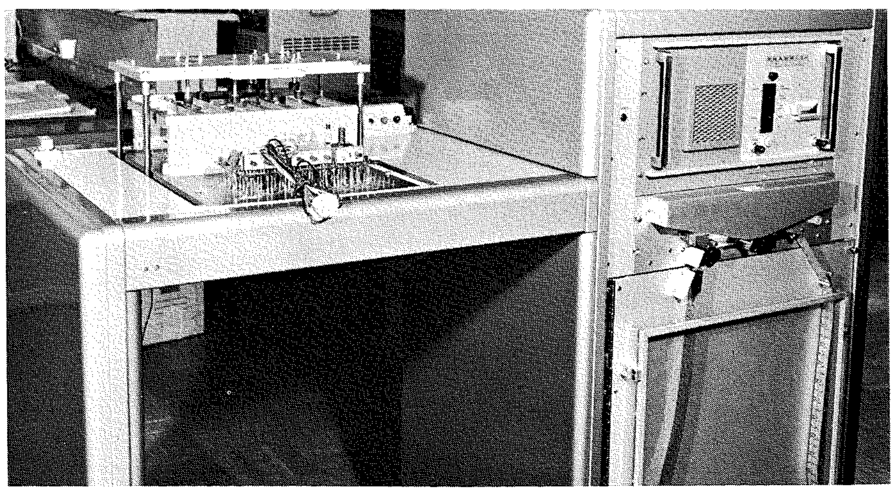
CHARACTERISTICS OF FACTORY TEST EQUIPMENT

The actual measurement of equipment performance parameters is not an important consideration in the design of factory test equipment. What is important is determining whether a parameter conforms, within a predetermined tolerance, to the design-center value. Most factory testing can be performed on a GO/NO GO basis. An exception to this occurs when tuning must be performed along with testing. In such cases, a simple analog indication is the most effective display.

Various levels of automation are appropriate to factory test equipment, depending upon how often setups must be changed or upon the complexity of testing. On the lowest level, the operator establishes the test conditions by setting switches. At a higher level, test conditions can be established using removable program boards, prewired for anticipated testing sequences. At a still higher level, numerical control tapes, decks of punched cards or magnetic tape can be used to provide faster testing and an even greater flexibility in changing programs. The highest degree of automation is obtained by using a computer to control the test, in which case it can branch to different test routines depending upon the results of earlier tests.

REQUIREMENTS OF AUTOMATIC TEST EQUIPMENT

Automatic test equipment consists of an aggregation of stimulus generators, such as programmable power supplies, frequency synthesizers and word generators, that apply signals to the unit under test in accordance with a stored program. It also includes sensors, such as digital voltmeters, balanced bridges, and counting rate meters, that measure the response to the stimuli of the unit under test. These responses are compared against a sequence of expected responses stored on punched-paper or magnetic tape. In addition, auxiliary



Automatic component evaluator for testing populated printed-circuit boards.

equipment—multiplexers, filters, signal conditioners, amplifiers and digital/analog or analog/digital converters—sometimes must interface between the stimulus generators, sensors, and the unit under test.

The output presentation of automatic test equipment can be either a direct action, such as tossing a defective part off a conveyor, or a GO/NO GO indication to an operator. Regardless of the type of action, results of pertinent tests are usually printed out as a permanent record.

The test routines performed with ATE are not always functional tests. In fact, a defective unit could pass (marginally) such a test, yet fail to function in its operating environment. Rather, inspection or circuit checks are made to ensure that functioning parts of correct value have been assembled with proper orientation, and that all interconnections are mechanically and electrically secure.

The ATE must be designed for use by production workers, not technicians. Therefore, it should be easy to operate and fail safe, and should deliver unequivocal accept/reject decisions. It should be easy to repair and, because it must function reliably in the factory environment, it should not require air conditioning. It must also be able to withstand the shock and vibration produced in moving, and the variations of line voltage and frequency encountered in a factory.

ADVANTAGES OF ATE

The advantages of automatic testing go beyond increased throughput. It allows the operator to reach unequivocal accept/reject decisions, which otherwise might be affected by unevenly applied personal factors. A print-out of test results can be made available that will become a part of the product's history, aiding troubleshooters and forming the basis of statistical information to help identify recurring defects in purchased parts or workmanship.

Multipurpose test stations can be outfitted with different sensors and programmed to perform a variety of testing operations on various products. Use of such equipment offers the potential of reducing the amount and diversity of test equipment carried in inventory and of amortizing its cost over many projects.

Probably the most significant advantages of ATE are that it minimizes handling of the product and test setup, and provides troubleshooting information to reduce the cost of failure.

FUTURE OF AUTOMATIC TESTING

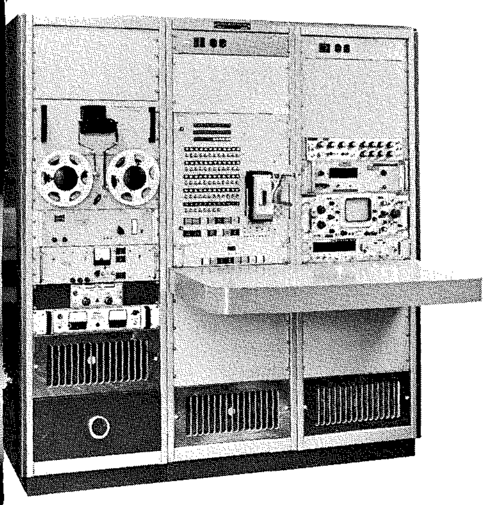
Automatic test systems of the future will utilize the computer for control and data collection. Several systems have already been implemented in RCA manufacturing divisions and more are planned. In many cases, these new systems are utilizing the RCA-1600 computer. This computer, together with a special equipment controller and the TESTRAN software package, is the generally recommended approach for implementation of process control for manufacturing.

Still in early stages of development are programs to diagnose troubles in the end product. Their implementation will represent a major breakthrough in achieving trouble-free products.

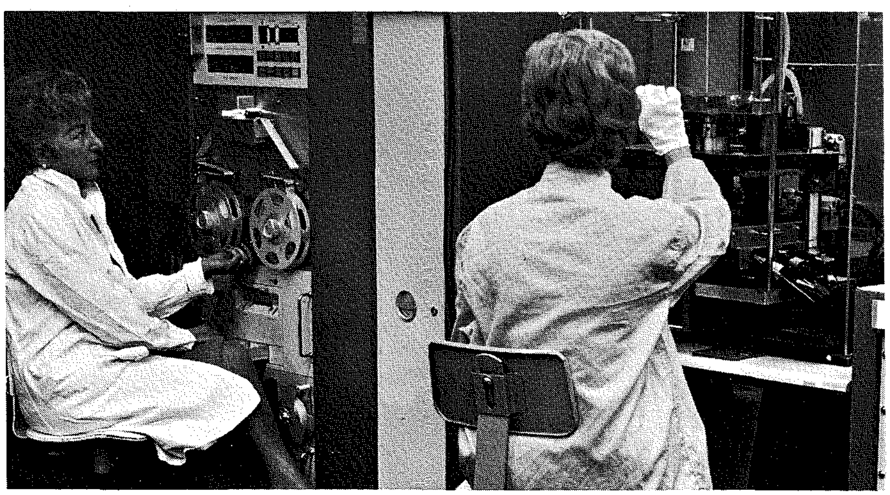
The advent of computer-aided design and design automation will provide self-programmed test sequences for computer controlled ATE, since lists of access points and values for GO/NO GO testing can be produced as an output of design automation routines just as wiring diagrams or parts lists are now produced.

As automatic test systems become more sophisticated, hiearchies of computers will be employed. Small machines will verify, format, and control the automatic acquisition of test data. Larger machines will make accept/reject decisions and classify parts and assemblies according to characteristics, while still larger machines will perform trend analyses and generate deliverable test reports for the customer.

Looking further into the future, we can anticipate the development of built-in test systems. These would allow the product to test itself as it proceeds from one assembly station to another, verifying that only functioning parts are inserted and that each one is correctly installed. The built-in test system would continue to function after the equipment is installed in the field. It would insure a minimum down-time by retuning itself to compensate for performance degradation due to aging parts and, if a part fails, repairing itself by switching to a redundant circuit. Only when equipment with built-in test systems is commonplace, will the need for automatic test equipment diminish.



Tester for minuteman plug-in modules.



DIT-MCO 6120 for testing unpopulated printed-circuit boards.

Presented here are brief descriptions of technical books which have recently been authored by RCA scientists and engineers, or to which they have made major contributions. Readers interested in any of these texts should contact their RCA Technical Library or their usual book supplier. For previous reviews of other books by RCA authors, see the August-September 1966 and August-September 1967 issues of the RCA ENGINEER. RCA authors who have recently published books and who were not cited in these listings should contact the editors, Bldg. 2-8, Camden, Ext. PC-4018.

Recent technical books by RCA authors

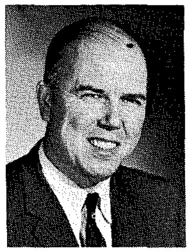
Photoemissive Materials: Preparation, Property and Uses

Dr. A. H. Sommer
Laboratories
Princeton, N.J.

This book is a compilation in one volume of all relevant information—previously available only in scientific journals and covering a span of more than 30 years—about photoemissive materials. Emphasis is on the techniques used in forming photocathode materials and on the physical and chemical properties of these materials. It is written, primarily, for those making or using photoemissive devices and, secondarily, for physicists and engineers who need a reference book on photoemissive materials. A bibliography of those subjects not treated explicitly in the text is included. Wherever possible, the author critically evaluates ambiguous or contradictory results that have been published in the past. *(To be published by John Wiley and Sons, Inc., November 1969.)*

DR. A. H. SOMMER received the PhD in Physical Chemistry from the University of Berlin and is a Fellow of the Technical Staff of RCA Laboratories. After associations with Cinema Television Co. (1936-1946) and EMI Research Laboratories (1946-1953) in England, he joined RCA in 1953. Dr. Sommer's work has been concerned mainly with the study of photoemissive and secondary electron emitting materials and with the development of photomultipliers and TV camera tubes. His contributions include the "panchromatic" bismuth-silver-cesium photocathode, the multi-alkali cathode, and the bialkali cathode. He is a Fellow of the IEEE and a member of APS and Sigma Xi. He received *RCA Laboratories Achievement Awards* in 1955 and in 1964, and the *David Sarnoff Outstanding Achievement Award* in Science in 1964.

Electro-Optical Photography at Low Illumination Levels



Harold V. Soule
Astro-Electronics
Division
Princeton, N.J.

This book offers an extensive consulting reference for low light-level systems. It should enable a reader with a problem in the area of low light-level systems to determine the hardware to use and its suitability for the task. Each potentially competitive instrument is presented in an unbiased manner, with evaluation and comparison of the important parameters. The book gives detailed presentations of the physical characteristics of vacuum-tube and solid-state image intensifiers and image-intensifier TV cameras. Also included are discussions of techniques of high speed TV line scan recording and nanosecond image intensifier recording. Spectral conversion of low-intensity radiation at all wave-lengths from the neutron and X-ray region through to the near infrared, to radiation at wavelengths of the imaging sensor sensitivity are discussed. A chapter is devoted to natural light radiation sources and another chapter to low f/number lens systems. The bibliography includes nearly all of the subject literature at the time of publication. *(Published by John Wiley and Sons, New York, 1967; price $15.95.)*

HAROLD V. SOULE, a Senior Engineer at the Astro-Electronics Division of RCA, received the BSME degree from Rensselaer Polytechnic Institute in 1948. Mr. Soule joined RCA in 1967, where he is continuing his work on low-light level and infrared systems. Previous experience, at Perkin-Elmer Corporation, includes studies of laser-camera systems, high-density laser-recorders, and low-light level systems. Before Perkin-Elmer, the author worked at several companies, providing technical group leadership and occupying a key position in connection with a number of missile-homing and surveillance system studies.

Real-Time Data Processing Systems—a methodology for their design and cost-performance analysis

Saul Stimler
Information Systems
Division
Cherry Hill, N.J.

This book is designed for those interested in calculating and optimizing the performance per dollar of real-time data processing systems, typified by message switching and automated airline reservation systems. The main objectives of this book are:

To introduce the data-processing practioner with batch processing experience to the operation of real-time systems.

To present a practical and broadly applicable methodology for calculating and optimizing the performance per dollar, of his real-time system.

To illustrate the method by applying it. Meaningful numerical calculations of the performance per dollar of real-time systems depends upon some mixture of inspiration, perspiration, knowledge, and experience. This book contains no substitutes for any of these necessary ingredients; however, it should make easier the acquiring of real-time system knowledge and experience. *(To be published by McGraw-Hill Book Company, January 1969.)*

SAUL STIMLER received the BEE from CCNY in 1942. During the past 25 years he has had broad responsibilities in government and industry. These include design, design management production engineering, project and product line management, application, and systems engineering. He has worked both in the analog and the digital field including such diverse areas as radar, railway signal equipment, underwater mines, seismography, nuclear reactor control systems, digital data transmission, real-time systems, and time sharing systems. He is presently Manager of the Time Sharing Project at RCA. He is a Professional Engineer, a member of Tau Beta Pi, holds two patents, and is recipient of the Navy's Meritorious Civilian Service Award.

The New Electronics

Bruce H. Shore
Scientific Information
Corporate Staff, N.Y.

The development of the point-contact transistor in 1948 marked the beginning of a profound change in the nature and practice of electronics both as a science and as an industry. Before this time, starting with the discovery of the electron by J. J. Thomson in 1897 and the invention of the audion by Lee DeForest in 1907, electronics was an activity concerned with the study, control and application of electrons released into vacuum. After that date, it became an activity concerned with the study, control and application of electrons confined in the solid state.

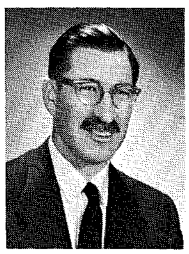
During its first or vacuum period, roughly fifty years in duration, electronics led to some of man's most impressive achievements—radio, sound motion pictures, television, the electron microscope, microwave radar, and the computer. During the second or solid-state period from 1948 to the present, it has added to this notable list with achievement of the transistor, the tunnel diode, the silicon controlled rectifier, the integrated circuit, the laser, the superconductive magnet, and holography. Still more is expected.

Though the emphasis of this book is on solid-state electronics, the author carefully reviews its development naturally from the pioneering experiments, investigations, theories, and hardware of vacuum electronics. Moreover, wherever practicable, he has included names, dates and historical information on both in order to reinforce the text and to afford reference points for the benefit of the more demanding or more sophisticated reader who wishes to find deeper treatments of the subjects discussed.

Finally, because modern solid-state electronics is so divorced from everyday experience with its heavy dependence on quantum mechanical theory and such mathematical hermetica as Bose-Einstein and Fermi-Dirac statistics, Mr. Shore has restored to a frankly literary style in the text. This has been done to assure that the widest possible audience may read it with both enjoyment and profit. (*To be published by McGraw-Hill Book Company, early 1969.*)

BRUCE H. SHORE received the BA in English in 1952 from Yale University. Shortly after graduation, Mr. Shore joined the *New Haven Register* as a member of its editorial staff. In 1953 he went to Hollywood, California, on a free lance writing assignment, resulting from his having written the book and lyrics for a musical comedy while he was an undergraduate. In December 1953, Mr. Shore became associated with the Los Angeles Stock Exchange and subsequently worked for Dean Witter & Co. In May 1954, he joined the brokerage firm of Walston & Co., and the following year transferred to the company's New York Headquarters, where he was in charge of the odd-lot desk. Two years later, he joined the firm of Avery-Knodel, Inc., national spot representative, as Assistant to the Director of Promotion, in charge of all radio sales presentations and promotional copy. In March 1958, Mr. Shore joined the NBC Radio Network as a writer in the Sales Presentation and Promotion Department. Among his responsibilities at NBC was the preparation of closed circuit presentations to station affiliates. He also wrote and helped produce two special records for national sponsors: "History in the Making" for the Rambler Corporation and " '59 Anthology" for the Longine-Wittnauer Watch Co., Inc. In 1960, Mr. Shore transferred from NBC to its parent company when he was appointed Administrator, Press Relations, for the RCA Semiconductor & Materials Division in Somerville, N. J., a position he held until going to RCA Laboratories in 1962 to head its Public Affairs activity. He was named Administrator of Scientific Information for RCA Corporate Public Affairs in April 1967.

Testing of Polymers

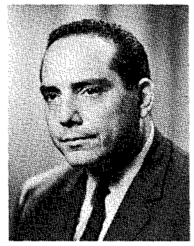


Dr. Abraham M. Max (contributor)
Record Division
Consumer Electronics Division
Indianapolis, Ind.

This three-volume series, edited by J. V. Schmitz, Technical Director, Celanese Chemical Company, New York, and W. E. Brown, Plastics Development and Service, The Dow Chemical Company, Midland, Michigan, gives a critical survey of testing methods for determining physical and mechanical properties of polymers. These include thermoplastics, thermosets, foam, film, fibers, rubber and elastomers, as well as adhesives, electrical insulation and laminates. Dr. Max contributed a chapter entitled "Surface Properties of Plastics for Sound Recording" which is contained in Volume 3 of this series. (*Published by Interscience Publishers, a division of John Wiley and Sons, 1967.*)

DR. A. M. MAX received his BS, MS, and PhD degrees from the University of Wisconsin in Chemical Engineering with minors in Physics and Physical Chemistry. After a period with the Ternstedt Division of General Motors, and the University of North Dakota as Assistant Professor of Chemical Engineering, he joined the RCA Victor Record Division in 1944 as Supervisor of Metallizing and Plating Develpoment. Since 1950 he has served as Manager, Chemical and Physical Laboratory. Dr. Max holds two U. S. patents in the field of electroforming. He is a member of the American Chemical Society, American Physical Society, Electrochemical Society, Faraday Society, Phi Lambda Upsilon, Tau Beta Pi, and Sigma Xi.

Systems and Computer Science



Saul Amarel (contributor)
Laboratories
Princeton, N.J.

This volume, edited by John F. Hart and Satoru Takasu, is a collection of ten works presented at the Conference on Systems and Computer Science held at the University of Western Ontario in September, 1965. Mr. Amarel contributed Chapter 8 entitled "An Approach to Heuristic Problem Solving and Theorem Proving in the Propositional Calculus." In his 100-page chapter, the author gives the conceptual framework for certain reduction procedures to be used in solving derivation type problems. He then uses this framework to specify a set of procedures for the construction of simple proofs to theorems in the propositional calculus. (*Published by University of Toronto Press,* 1967.)

DR. SAUL AMAREL received the BS in 1948 and the degree of Ingenieur EE in 1949 from the Israel Institute of Technology, Haifa. He pursued graduate studies at Columbia University, New York City, receiving the MS in 1953 and the Doctor of Engineering Science in 1955. For six years, Dr. Amarel was associated with the Scientific Department of the Israeli Ministry of Defense where he led the development of control and communication systems and also conducted research on computer simulation methods related to operations research problems. From 1953 to 1955 Dr. Amarel was associated with the Electronics Research Laboratory of Columbia University where he developed operational methods for the analytic study of linear and nonlinear dynamic systems. Since 1957, Dr. Amarel has been a member of the technical staff at RCA David Sarnoff Research Center in Princeton, New Jersey. He presently heads the Computer Theory Group of the Computer Research Laboratory. His work is in the areas of switching theory, probabilistic logic and artificial intelligence; he also directs studies in systems theory, character recognition, machine organization and programming. Dr. Amarel is a senior member of the IEEE, and a member of the American Mathematical Society, the Association for Computing Machinery, the AAAS, and Sigma Xi.

Automated testing — a prologue

D. B. Dobson

CONCERN WITH THE PROBLEM of keeping complex equipment in operating condition has resulted in increased emphasis on automatic testing. The papers in this issue reflect, to a large degree, the state of the art in automatic testing up to mid-1968.

Why are assemblies tested? The first reason is the lack of confidence in the ability of any assembly to perform as designed. The second reason, based on any negative results obtained, is to obtain adequate information for maintenance decisions.

Maintenance time can be divided two ways: test and repair, in the ratio of approximately 1 to 6. A major objective of testing, therefore, is the reduction of the time required for repair portion, by supplying adequate diagnostic information to the operator. In the case of test during manufacture, the information is returned to modify the manufacturing in a manner to eliminate the "bad" indication. Also, the lower the confidence level in any item, the more testing is required.

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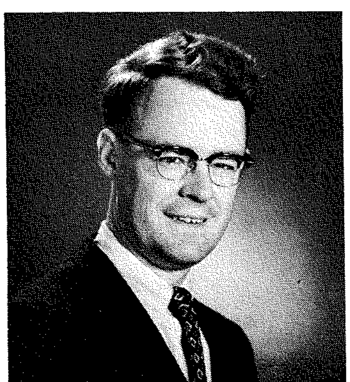
Final manuscript received July 19, 1968.

D. B. Dobson, Administrator
Technical Publications
Aerospace Systems Division
Burlington, Mass.
is responsible for Division Patent and NASA New Technology Reporting; and the coordination of all Divisional Public Affairs and Advertising. He also functions as the New England Field Representative for RCA Public Affairs covering all activities in Eastern Mass., N.H., and Maine. He is the Secretary of the RCA Public Affairs Council for Eastern Massachusetts. He is a Senior Member of, and is active within the IEEE, where he has been: Chairman of the Checkout & Test Subcommittee, is a member of the Support Systems Committee, and has served on many national and international conference committees as publicity and conference record chairman. He was the Editor of the *IEEE Transactions of Aerospace* from its inception and currently he is the Executive Editor of the *IEEE Transactions on Aerospace & Electronic Systems.* He was, for several years, the Electronics Editor of GSE Magazine. He is a member of the Aviation/Space Writers Association, the Society of American Military Engineers, and the American Ordnance Association. He has presented and published many papers on various aspects of Automated Testing, Systems Support and Technical Communications.



The present-day complexities of equipment have created a natural gravitation to the use of equipment that will perform as much of the test cycle as automatically as possible. However, the testing techniques have only recently begun to receive the attention they deserve.

The development of automatic test equipment to its present sophistication has occurred through incremental advances with the advent of digital computer technology in testing systems, speeds increased to the point where replacement of operators became economically feasible.

Methods other than exact duplication of operating conditions to ascertain design operation were examined. Some of these, although started on a theoretical basis, have developed into demonstrably superior methods of testing equipment of all types.

Many methods depended on the solution of complex mathematical equations; the advances occurred in parallel with the availability of tools. As computers became available, the use of transfer function analysis (for example) as a test method received increased attention; these analyses required the use of a computer on the test site; the addition of computational capability at the test site led to the use of iterative testing, trend analysis, and prediction techniques.

Ideally, any development program should select the test parameters immediately after the product parameters are established. Any hardware design should be tailored to fit the desired test rather than the present method of having the test method follow, and be subservient to, the design.

Who knows what automatic test techniques will be used in the future? Anything other than classical electronics may some day be utilized as effective tools. The use of infrared testing was predicted; today an industry association exists. Infrared equipment and techniques are available, and use is being specified daily. Other future "testing" tools may include coherent light, ultraviolet, ultrasonics, electromagnetic radiation, and other seemingly far-fetched methods. Continuous research into these and other techniques will generate the significant steps in testing; a considerable body of opinion holds that the next advances in testing will be of a radical rather than of an incremental nature.

Automatic Test development may be traced by those interested through several sources. Perhaps the earliest meetings on the subject were yearly Army-Navy-Air Force ATE Symposia that culminated in the 1960-1961 Design Courses on ATE, conducted by Project SETE (Secretariat for Electronic Test Equipment). *Proceedings* of the 57-58-59 Symposia and the *Design Course Lecture Notes* may still be available through Project SETE, New York University, 401 West 205th Street, New York City; a more recent publication of Project SETE has been a book based on these courses.

Battelle Memorial Institute conducted a workshop in October 1964 on ATE, and published a bibliography of the art prior to about June 1964.

The IEEE has been active in reporting this field. In 1963, the International Conference on Aerospace Support was held; the conference record totaled 1504 pages. (*Transactions on Aerospace,* Volume AS-1 Number 2, August 1963). Previously, the *IRE Transactions on Military Electronics* devoted their July 1962 issue to Automatic Testing Techniques (Vol. MIL-6 Number 3). In 1965, the St. Louis Section of the IEEE initiated what has become *the* yearly meeting in the field—the Automatic Support Systems Symposium. Now co-sponsored by the AES (Aerospace and Electronic Systems) Group, papers appear in the *Symposium Record.* The IEEE Transactions on *Aerospace and Electronic Systems* also publishes many papers in the field. (Contact the IEEE Order Department, 345 East 47th Street, New York, N.Y., for all IEEE publications.)

Languages for automatic test systems

R. E. Turkington

This paper presents a tutorial discussion of test languages for use in programming automatic test systems and describes the type of compiler processing necessary to translate these higher-level languages. The configuration and operation of the new universal test equipment compiler, currently being developed for the U.S. Army, is described briefly.

THE DEVELOPMENT of user-oriented languages for programming automatic test systems has enabled the test engineer or technician to prepare his test programs without requiring a knowledge of the machine language of the system. Two types of user language are curently in use: 1) device-oriented languages—structured in terms of the test devices in the test system (i.e., mnemonic equipment addresses and specific test-point designations) and 2) languages oriented toward the unit under test—structured in terms of basic test functions and the signals applied to and measured from, the tested unit. This latter type of language frees the test programmer from the detailed knowledge and bookkeeping associated with programming the individual test devices in the system. These source-language programs are insensitive to changes made in the test system, and their listings resemble conventional test procedures that can be read and understood easily.

English test-oriented languages have been developed to expedite the programming of two ATE systems—depot installed maintenance automatic test equipment (DIMATE)[1] and land combat support system (LCSS).[2] The DIMATE language, developed and used initially by ASD engineers, is now being used by depot personnel in the preparation of additional test programs. An English test-oriented language has been developed for the LCSS system, a tape-controlled system. This language, which closely resembles that for DIMATE, has been used for the design of all programs being delivered with the current production systems. The language is currently being implemented as a compiler language for the coding of future programs. Languages of this type can be used equally well with computer-controlled and tape-controlled systems.

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USER ORIENTATION

Any practical ATE test language must be user-oriented, i.e., a language that can be used effectively by the effective users of the machine, i.e., the test engineers and/or technicians preparing the test programs. This orientation is often present inherently for tape-controlled systems. For computer-controlled systems, this orientation is achieved by building into appropriate language functions the necessary computer operations. Thus, when the test programmer specifies certain data for the test subsystem of the ATE, by implication he also specifies the computer operation that will send this data to the test subsystem. The former practice of using engineering personnel to prepare the test-subsystem portion of a test program and computer programmers to prepare the computer portion of each test program is no longer adequate for many ATE applications.

BASIC LANGUAGE ORIENTATION

One can define two major levels of ATE language, each with two subcategories:

1) Device-oriented language—a language structured in terms of the actual test devices (stimulus generators, measurement functions, and switching) that comprise the test subsystem.
   a) Machine language—the actual pattern of ones and zeros punched on tape or cards that directly controls the system.
   b) Symbolic language — a language where a symbolic device address is used in place of the actual machine language.

2) UUT-oriented language—a language structured in terms of the unit under test (UUT)—in terms of the stimulus signals that can be applied to the UUT, the responses that can be measured from the UUT, and the test functions to be performed.
   a) Procedure-oriented language—the statements in this language form a step-by-step procedure for the machine, much like that for a test technician to follow manually.
   b) Problem-oriented language — the statements in this language describe the basic functional tests to be performed on the UUT, such as testing the gain, linearity, or bandwidth of an amplifier.

This basic device and UUT orientation is illustrated in Fig. 1.

Machine Language

For both digital computers and ATE systems, the machine languages are structured according to the basic functions to be performed by the hardware. In the computer, these functions are the operations *add, subtract, multiply, store,* etc. The instructions generally consist of the operation code and a memory address, with computer programs comprised of both instructions and data. One may think of the control unit as a set of logic modules, with

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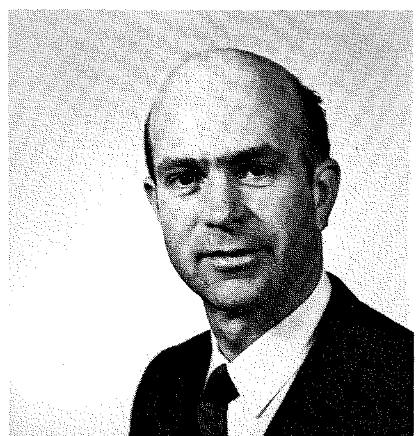
received the BS and MS in Electrical Engineering and the degree of Electrical Engineer from MIT in 1948, 1951, and 1952, respectively. After working at the Dynamic Analysis and Control Laboratory at M.I.T., Mr. Turkington joined RCA in 1957 as a member of the missile systems project group. He had technical responsibility for the analysis, design, programming, and field checkout of test programs for use with the Automatic Programmed Checkout Equipment for the Atlas missile. He headed the implementation, simulation, and test design groups, whose major functions were the design and implementation of a simulated environment in which the Missile Impact Predictor computer program could be tested at the domestic site and the design of 25 tests to fully exercise and test the program. As a member of the ATE systems group of the ATE project office, Mr. Turkington has been a key reviewer of test programs prepared for the LCSS system and has been project engineer for two fault isolation studies, for several ATE programming techniques and procedures studies, and for the Universal Test Equipment Compiler. Mr. Turkington is a member of Eta Kappa Nu, Sigma Xi and the Institute of Electrical and Electronic Engineers.



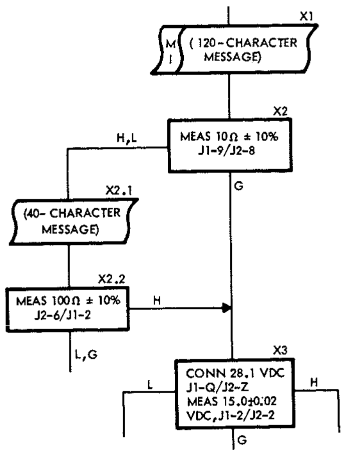


Fig. 1—Device versus UUT orientation for ATE languages.

each module performing one of the computer's operations; the instruction operation codes, then, may be considered as the addresses of these modules. The program data are just that information upon which the logic modules will operate during the program execution.

In an ATE system, one may consider the elements that correspond to these logic modules to be the stimulus, measurement, and switching devices within the system. The system test instructions, then, may be considered to be composed of the address of a specific device (such as power supply no. 1, pulse generator no. 1, digital multimeter, or test point matrix *A*) and a value, which may represent the desired stimulus value, the desired measurement scale, or the desired switching configuration. These values correspond to the memory address portion of a computer instruction. Stored measured values and information to be displayed or printed to the test operator are similar to the computer's data category.

Symbolic Language

In either the conventional computer or the ATE system, the actual machine language is a sequence of characters—binary, decimal, or hexadecimal digits or alphanumeric characters—as represented by a pattern of ones and zeros or the holes on a punched tape or card. A sequence of these may appear as item 1 in Tables I (a) and (b). The symbolic, or assembly-level, language for digital computers is simply the substitution of 1) a mnemonic code (generally two or three characters) for the numeric operation codes and 2) a symbolic name for the memory location address. The final translation of the mnemonic codes and symbolic locations to the actual machine language is done by an assembly program.

A similar elevation of the basic machine language is possible for ATE systems. Mnemonic codes can be defined for each test device or test function address in the system, such as

PS1, PS, · · ·	Power supply no. 1, 2, · · ·
DA1, DA2, · · ·	DACON no. 1, 2, · · ·
SGN	Sine-wave generator
DMM	Digital multimeter
MDC	Measure DC voltage
TPA	Test point *A*

A companion change would provide for the statement of the scale value as a decimal number in common engineering units, even if the particular device is programmed as a binary scale value—such as 15.55 volts rather than 3023_8 with a scale factor of 0.01 v/quantum.

Samples of these two types of languages are shown in Tables I (a) and (b) as item 2. Note that the machine language and the symbolic language (for both a computer and an ATE system) are essentially the same level of language in that, in general, the same amount of detail must be specified by the programmer for either language and each is based on the address or identity of the hardware devices or functions. Note, also, that the translation from the symbolic to the machine language is essentially a direct substitution of numeric values for corresponding symbolic references. There is no significant amount for creation or generation of machine instructions in this process. Thus, these translator programs are often called assembly programs. Some of the more elaborate translators that allow the test programmer more freedom in the method of information specification are termed compilers.

Procedure-Oriented Language

A test language structured in terms of the UUT stimuli and measurement signals will represent closely the language used to specify a step-by-step test procedure used for manually testing a UUT; thus, its identification as a procedure-oriented language. The statements can be grouped into three major classes:

1) Direct UUT test statements, such as connections and measurements,
2) Control statements, such as wait for *xx* seconds, do step *y* next, etc., and
3) Arithmetic or Boolean statements.

Table 1(a)—Programming Language Levels for Digital Computer Programming.

Item	*Language Level*		*Language Samples*	
1	Machine Language		24005620 16101277 07077620	Instructions, Op Code, Memory Addresses Data
2	Symbolic Language (Assembly Language)		CLA VARA ADD VARB MUL SCALE DIV NOM STO ANS	Mnemonic Instructions, Symbolic Addresses, Macros, Comments
3	Procedure-Oriented Language (Compiler Language)	 101 102 103	ANS = (A + B)* SCALE/NOM IF(ANS) 101, 102, 103 CALL ANAL GO TO 200 CALL ERROR DO 105 I = 1, 10, 2	
4	Problem-Oriented Language		SOLVE (5X²Y³ + 16XY² + 25Y = −50) FOR Y = 1, 5, 10, 50	

Table 1(b)—Programming Language Levels for ATE Programming.

Item	*Language Level*		*Language Sample*	
1	Machine Language (ATE Device-Oriented)		15006317 55100125 55501469 02107440	Instructions, Internal Data, Input/Output, Test Instructions
2	Symbolic Language (ATE Device-Oriented)		PS1 14.6V DA1 1.55V SGN 10.0V, 10,000Hz TPA 1 TPB 5 MDC 3 DLY 50 msec MEAS	
3	Procedure-Oriented Language (UUT-Oriented)	 101 102	CONNECT 14.6 VDC, 1.5A, J101-5, J101-1 CONNECT 1.55 VDC, 0.1A, J101-10, J101-12 CONNECT 10.0 VAC, 10KHz, J101-15, J101-AA MEASURE 10.5 VDC ± 1.5%, STORE OUTPUT GO TO 101 (HI), 102 (GO), 101 (LO) CALL ERROR GAIN = (OUTPUT-OFFSET)* CORR/INPUT EVALUATE GAIN 100 ± 5 GO TO . . .	
4	Problem-Oriented Language (UUT-Oriented)		TEST GAIN . . . TEST BANDWIDTH . . .	

The UUT statements obviously must contain at least three types of information as implied in Fig. 1:

1) The test function—connect, measure, etc.
2) The stimulus or measurement signal characteristics
3) The UUT connector and pin designations where the stimulus is to be applied or the measurement is to be taken.

Item 3 in Table I (b) illustrates several statements of this general type.

Digital-computer counterparts to this type of language include FORTRAN, ALGOL, COBOL, etc. These languages are structured in terms of elemental functions that are more powerful than the basic machine operations and which, in general, will cause the language translator to generate several machine operations for each statement function. Several sample FORTRAN statements are shown in item 3 in Table I (a). Perhaps the two most outstanding features of this language are

1) The arithmetic statement format, which allows the program statement to almost duplicate the engineering or mathematical expression that is to be computed, and
2) The relative ease with which engineering personnel can learn and use this language.

Note that this language is procedure-oriented as the various statements define the procedure to be followed in solving some problem; they do not define the problem directly. Both this computer language and the ATE procedure-oriented language are translated to the machine language by compilers.

Problem-Oriented Language

Neither of these two languages is truly a problem-oriented language. Today problems that require computer solutions are complex equations, circuit-analysis problems, circuit or mechanical design, surveying layouts, etc. Much progress is being made today in the development of programming languages and special compilers specifically designed to describe directly and translate the computer-user's problem. Item 4 in Table I (a) represents a possible statement in a mathematical problem-oriented language. Correspondingly, the major steps in a test procedure or an ATE test program may be the performance of a gain test, a linearity test, or a bandwidth test. Thus, a truly problem-oriented test language would be based on this level of function—item 4 in Table I (b)—with each one possibly defined in terms of the procedure-oriented language, i.e., statements such as connect, measure, delay, etc. This level of ATE language is not yet in significant use. Its implementation will probably occur as special subroutine functions in procedure-oriented languages; several have already been defined in this manner.

In summary, the current course of development of ATE languages is following rapidly through the same stages as the older digital-computer languages. Two of these are in relatively prevalent use today — the device-oriented symbolic language and the UUT-oriented procedural language. Both of these are user-oriented in that each can be written and read directly by test engineers or technicians without recourse to a digital-computer programmer even for computer-controlled test systems. This user-orientation is accomplished through the use of test-oriented mnemonic address codes or English-like test statements and by absorbing all necessary computer functions in subroutines activated by test-oriented statements in the language.

LANGUAGE SAMPLES

Statements in most device-oriented languages comprise 1) a device address or function mnemonic, 2) a possible function subaddress mnemonic, 3) a scale value, and 4) possible auxiliary data in some coded form. Table II shows several examples, the meaning of most of which is rather obvious. Items 10 through 13 represent alternate methods of defining measurement statements. The addresses for the first two define the hardware device involved (e.g., the digital multimeter) with the subaddress defining the function (i.e., DC); the addresses of the last two define the hardware function directly. Also in the former, the value defines directly the scale to be used, such as scale no. 3 or no. 2, whereas the latter examples require the associated compiler to translate the full-scale voltage value into the proper scale digit. Items 14 through 17 illustrate a more complicated statement where the time-interval statements must define the measurement scale (or reference clock frequency), the signal amplitude, and the slope and the threshold level for the start and stop criteria. The flexibility allowed the test programmer in entering scale values and other data is a function of the elaborateness of the associated compiler. For example, he may be required to always enter values in volts, microseconds, hertz, etc., or he may be able to use equivalent scale units, such as kHz, MHz, or GHz.

Two examples of current UUT-oriented languages are the ASD DIMATE/LCSS language and the Abbreviated Test Language for Avionic Systems (ATLAS) currently being developed as a standard for the commercial airline industry. Statements in these languages, in general, consist of a function, or verb, followed by a noun and a series of modifiers. For those statements that deal with stimuli and responses, the modifiers define the specific signal or power characteristics and the UUT connections. The functions contained in the LCSS language resemble those in the prior ASD DIMATE language[3] very closely. The major functions are given and described in Table III.

Table II—Samples of Device-Oriented Statements.

Item	*Statement*
1	PS1 + 15.6 V
2	DA3 − 1.55 V
3	SGN + 18.0 V
4	SGN F 15,000 Hz
5	PGN P 1500 μsec
6	PGN W 150 μsec
7	PGN + 20.0 V
8	TPA 16
9	TPB 25
10	DMM DC 3
11	DMM AC 2
12	MDC 1000 VFS
13	MAC 100 VFS
14	MTI REF 1 MHz
15	MTI AMP 25.0 V
16	MTI SRT + +0.5 V
17	MTI STP − +0.5 V

ASD Language Samples

The LCSS and DIMATE languages are designed to be used with a fixed field format consisting of ten fields of eight columns each. The function verb always is placed in field 2 (as a minimum, the first four characters must be written) and the value and the units of the main modifier are placed in fields 3 and 4, respectively. The first field contains a test no. and special compiler flags. The UUT connections are entered as the last modifiers in each statement. On the program listing prepared by the compiler, the statement format is a duplicate of the input format.

The language utilization characteristics that most influenced the selection of this format include:

1) The use of the language primarily for the creation and validation of test programs (its use following the final acceptance of the test programs or by non-RCA personnel was a secondary consideration);
2) The minimization of the amount of unnecessary or redundant information needed in the language;
3) The engineers' affinity for the tabular format for data presentation;
4) The ease of locating a piece of data (i.e., a signal characteristic, a UUT connection, or a test function) in the program listing when data is tabulated.

Several sample statements for an LCSS-type language are shown in Table IV. The basic intent of these statements is self-evident; however, certain aspects need some explanation. For item 2, the maximum value of the UUT current is given as an aid for the compiler in selecting the specific ATE device to be used. For item 5, the inclusion of the test tolerance indicates that the measured value is to be evaluated against test upper and lower limits; if only an upper (or lower) limit comparsion has been desired, only a + (or a —) would have been used. (Actually, because the ± symbol is not defined on key-punch machines, no sign is used for the two-sided comparison). The omission of a tolerance, as in item 6, indicates no comparison is to be made at that time—either the value will be compared later or will be used in subsequent arithmetic. Both items 5 and 6, as written, will cause the measured value to be saved only until the next measurement is taken; if more permanent storage is desired, a label, or name, by which the quantity can be retrieved when later computation or evaluation is desired, is entered at the end of the statement in a special field provided. Item 7 is a sample arithmetic statement involving two previously measured and stored values (INPUT and OUTPUT) and two previously measured or calculated correction factors (SCALE and BIAS).

ATLAS Language Samples

The ATLAS language is currently under development by a subcommittee of the Airlines Electronic Engineering Committee (AEEC) composed of interested airline and manufacturing representatives.[4] The development of this standard language allows an effective interchange of test programs among the various airlines and prime equipment manufacturers, even though different ATE systems may be used by each for testing the same UUTs. Although all the details of the language have not been developed at the time of this writing, the basic statement form and format have been adopted. The basic language resembles the LCSS language quite closely, but is oriented primarily to the untrained reader even at the expense of requiring the test programmer/coder to write otherwise unnecessary information. This stress on readability stems from the following:

1) The resultant more-readable test program can also serve as an easily understood test procedure in the conventional sense;
2) Many more people (supervisory, approvers, quality control, etc.) will have a need to read and understand the test programs (procedures);
3) Airlines that are too small to acquire ATE systems can use a test program listing as a manual test procedure.

The language differs from that for LCSS in three major respects:

1) The signal type (i.e., constant voltage, constant current, pulse train, etc.) is stated explicitly as a noun following the function verb.
2) All ambiguous signal characteristics (such as those having similar dimensional units or multiple UUT connector and pin designations) will have a unique identifier as part of that modifier.
3) The first part of each statement, which contains the test/statement number and necessary flags and the function verb, is fixed format. The remainder of each statement has a variable format with the individual modifier fields separated by commas and the parts of the modifier separated by at least one space.

Table V shows preliminary[5] sample ATLAS statements that correspond to those in Table IV. Note that the functions of measurement and evaluation have been placed in two statements; thus items 5a and 5b together represent the ASD function of measure.

There are other examples of English test-oriented UUT-oriented languages in use or under development today, including several for missile and space vehicle system checkout. However, the samples shown here illustrate adequately the basic language principles.

Programming Example

To better illustrate the relative capabilities of a user device-oriented and a UUT-oriented test language, consider the test program segment shown in the flow diagram of Fig. 2. In this representation,

Table III—Major Test Functions in the LCSS Test Language.

Function	*Meaning*
CONNECT	To select the appropriate stimulus device(s), scale them to the values given, and apply the signal to the UUT pins specified in the statement.
*CONNECT	Same as CONNECT except the signal is not applied to the UUT.
APPLY	To connect all previously selected, scaled, but unapplied supplies to the UUT pins specified in the respective *CONNECT statements.
MEASURE	To select and scale the appropriate measurement device, to connect it to the UUT pins specified, and to take the measurement. The comparison of the measurement against limits and/or the storage of the measured value are also controlled by this statement (see Table IV).
MONITOR	To measure and display repeatedly at intervals of approximately 1 sec. the signal at the specified UUT pins.
EVALUATE	To compare a stored, measured, or computed value aganist the limits given in the statement.
DELAY	To delay the continued execution of the test by the amount stated.
SWITCH ON SWITCH OFF	To control the general-purpose switches named in the statement.
GO TO	To cause the test program sequence to jump a) unconditionally to the test number given or b) conditionally to one of three specified test numbers according to the HI, LO, GO result of the last comparison.
SET RESET	To cause the program indicator(s), or flag(s) named to be set or reset.
CHECK	To cause the test program sequence to jump to one of two test nos. depending on the ON, OFF state of the indicator named.
PRINT	To cause the following message to be printed to the test operator.
ARITHMETIC OPERATIONS	No function word is required. Arithmetic expressions are written following the common FORTRAN conventions.

Table IV—Sample Source Language Statements.

*Item**	*Statement*					
1	CONN	25.4	VDC	J1-5	J1-1	
2	CONN	150	MVDC	100 MA	J1-2	J1-1
3	CONN	10.0	VAC	150 KHz	J2-5	
4	DELAY	50	MSEC			
5	MEAS	8.5	VDC	±1.2 VDC	J3-2	J1-3
6	MEAS	15	VRMS	J2-3	J1-1	
7	GAIN	= (Output · Scale — Bias) · 100/Input				

*Not a part of the test statements format

1) The H, L, G symbols indicate the program branching conditions of HI, LO, GO,
2) Test block *X1* and *X2.1* contain messages to be printed to the ATE operator, and
3) the MI in block *X1* indicates that a manual intervention by the ATE operator is required (i.e., the machine should be stopped following the printing of the message).

The corresponding source-language statements, following the DIMATE language conventions quite closely, are as shown in Table VI. The corresponding statements for a postulated device-oriented language based on the LCSS assembly-level language is shown in Table VII. To preserve user orientation, mnemonic test-device addresses have been used and ATE computer functions have been placed in computer functional subroutines that are addressed by the mnemonic codes defined in Table VIII.

In translating this language to ATE machine language, the compiler would

1) Convert the computer statements into the appropriate subroutine calling sequences and
2) Convert the test statements into test-device machine language and attach to them the appropriate computer data output instructions.

The computer functions could be implemented by a conventional compiler approach or interpretively in the ATE computer.

Device-Oriented versus UUT-Oriented Applications

In developing a new ATE system or application, the preference for a device-oriented, or a UUT-oriented, language is seldom clear and, generally, involves a number of trade-offs. It is clear, however, that as a minimum a device-oriented language must be user-oriented, thereby allowing the test engineer or test technician to prepare his own test programs. The ATE computer software system must also give this engineering test programmer substantial help in debugging and validating his program on the ATE system, as this phase of the test-program preparation process for fault-isolation diagnostic programs may account for nearly half the preparation cost.

Based on past experience it is clear that with a UUT-oriented language

1) Test programs can be prepared and validated faster and for less cost and
2) A higher level of program documentation is easily obtained; however,
3) The compiler is more costly to develop owing to its greater dependence on the ATE test devices and the system logic.

In selecting one or the other approach, the following factors should be considered:

1) The number, type, and complexity of test programs to be prepared. If the number is few and they are simple, the additional cost of the more complex compiler may not be justifiable. If the testing is for a large quantity of only a few types of electronic components, the problem may then be one of many sets of data (component characteristics and test limits) being processed by one program. In this case, a simple data conversion compiler may suffice.
2) The size, background, and duties of the group preparing the test programs. One of the greatest assets of the UUT-oriented compiler is that it relieves the test programmer of needing detailed knowledge of the composition and operation of the test system. This may be a major consideration if the test programmer is a design engineer who only very occasionally must be concerned with test program preparation and validation.
3) Will there be a need for continuing program changes or updates following validation? Or a need for persons other than the test programmer to use and understand the test? The higher-level language and resulting documentation will expedite these operations.
4) Will the test system configuration be changeable either from UUT-to-UUT or over the useful life of a test program? For each approach, the compiler may require updating each time a change is made to the test system. In general, the change is more complex for the higher-level language system, but the test programmer and the source-language program are more isolated from the change. For example, the effect of an equipment change on a validated working program may be only the recompilation of that program on the updated compiler.
5) Is there a need for compiling test programs on the ATE computer? Owing to the computer characteristics required for the UUT-oriented compiler, its operation on the ATE computer is often unfeasible at present. In general, the device-oriented compiler is more easily adapted to operation on the ATE computer.

The cost of developing a new compiler for a test system may be substantial. There are currently in existence or under development, however, several outstanding examples of general-purpose, or universal, test compilers for both the device-oriented or the UUT-oriented language. These compilers,

Table V—Sample ATLAS Source Language Statements.

Item	
1	CONNECT DC VOLTAGE, 25.4 V, J3-2 HI, J3-3 LO
2	CONNECT DC VOLTAGE, 150 MV 100 MA MAX, J1-2 HI, J1-1 LO
3	CONNECT AC VOLTAGE, 10.0 VRMS, 150 kHz, 12-5
4	DELAY, 50 MSEC
5a	MEASURE DC VOLTAGE, 10 V MAX, J3-2 HI, J1-3 LO
5b	COMPARE MEASUREMENT, 8.5 V NOM, 9.7 V UL, 7.3 V LL
6	MEASURE AC VOLTAGE, 15 VRMS MAX, J2-3 HI, J1-1 LO
7	CALCULATE, GAIN = ((OUTPUT·SCALE) — (BIAS)·100 INPUT

Table VI—UUT-Oriented Coding for the Program Example.

TX1	PRINT MSG . . . PAUSE
TX2	MEASURE 10Ω ± 10%, J1-9, J2-8 GO TO X2.1 (HI), X2.1 (LO), X3 (GO)
TX3	CONNECT 28.1 VDC, J1-Q, J2-Z MEASURE 15.0 VDC ± 0.02 VDC, J1-2, J2-2
TX2.1	PRINT MSG . . .
TX2.2	MEASURE 100Ω ± 10%, J2-6, J1-2

Table VII—Device-Oriented Coding for the Programming Example.

Test No.	*Statement*	*Reference**	
T1	PRINT (------)	X1	C
T2	PAUSE	X1	C
T3	MRE 2	X2	T
T3A	TPA 5	X2	T
T3B	TPB 8	X2	T
T4	DLY 1	X2	T
T5	MEAS	X2	T
T5A	LIM1, (10.00, 10.00, T6, T51, T51)	X2	C
T51	PRINT (------)	X2.1	C
T51A	MRE 3	X2.2	T
T51B	TPA 1	X2.2	T
T51C	TPB 4	X2.2	T
T52	DLY 1	X2.2	T
T53	MEAS	X2.2	T
T53A	LIM1 (100.0, 10.0, T54, T6, T54)	X2.2	C
.			
.			
.			
T6	PS1 28.1	X3	T
T6A	APLY	X3	T
T6B	MDC 2	X3	T
T6C	TPA 2	X3	T
T6D	TPB 2	X3	T
T7	DLY 1	X3	T
T8	MEAS	X3	T
T8A	LIM2 (15.00, 0.02, T9, T911, T921)	X3	C

*Not a part of the test statements. Used for reference to the sample flow chart and to identify primary ATE subsystem involved—test station or computer.

Table VIII—Assumed Computer Function Subroutines for the Program Example of Table VII.

Function Mnemonic	*Subroutine Function*
PRINT	To cause the following message to be printed
PAUSE	To cause the test processing to stop until resumed by operator action
LIM1 (A, B, C, D, E)	To read in a measured value, compare it against limits of A ± B% and branch to C (on GO), D (on HI), and E (on LO)
LIM2 (A, B, C, D, E)	Same as LIM1 except A and B are expressed in the same units.

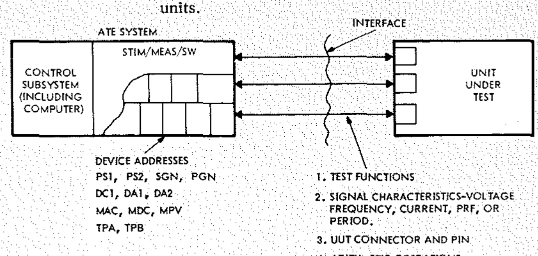


Fig. 2—Sample test program segment.

when given suitable definitions of the ATE language, the ATE test devices, and the coding rules, can in large measure adapt themselves to a new test system. In the previous discussion, comments regarding compiler costs referred to either the relative cost to develop new compilers for each language approach or to adapt a universal compiler to a specific system for each language approach.

COMPILER FUNCTIONS

The basic function of a compiler is the translation of some source language into the corresponding machine language. However, because the UUT-oriented language is structured in terms of the UUT signals, the translation process for this type of language often involves a selection of the specific item or items of ATE equipment to be used to implement the test functions. Consequently, the compiler must contain knowledge regarding the quantity, characteristics, and programming rules for each ATE device. Thus, this translation process is, in general, much more complex than conventional digital-computer language translation. It is this compiler capability that provides most aid to the test programmer.

This section describes the gross operating steps of such a compiler regarding test equipment selection and interface design. Except for these problems, the language translation process is not greatly different from that for conventional digtal-computer compilers.

Equipment Selection

An alternate method of characterizing the difference between a symbolic and a procedure-oriented langauge is the method of managing the resources of the system. For digital-computer programming in a symbolic language, the programmer must manage (i.e., allocate, control, and keep track of) memory storage locations, index registers, indirect addressing, and program-loop logic. With the procedure-oriented language, these computer resources are automatically managed for the programmer by the compiler.

In an ATE system, the corresponding system resources are the test devices—stimulus supplies, measurement functions, and switching. (Note that the ATE computer resources are not included here; if the ATE programming system is to be user-oriented, these resources will be managed automatically using either programming approach.) With the ATE symbolic language, the test programmer must allocate, wire, address, and keep track of these test devices himself. With the procedure-oriented language, these management functions are done automatically by the compiler.

To illustrate this equipment selection function, consider the translation of the source statement CONNECT 8.5 VDC, 0.1A, J1-1 (HI), J1-2 (LO) for a system that contains the following items of stimulus equipment:

Class	*Voltage Range*	*Programmable Step Size*	*Max. Load*	*Quantity*
1	0 to $\pm$9.99 V	0.01 V	0.1 A	3
2	0 to $\pm$39.9 V	0.1 V	2 A	6
3	0 to $\pm$49.9 V	0.1 V	25 A	2
4	30 to $\pm$250 V	0.5 V	5 A	1

Assume an ATE system in which stimulus supplies are directly connected to the desired UUT terminals through an application relay (i.e., no wired-in stimulus/UUT switching matrix). To implement this source statement the compiler would perform the following steps:

1) Using the programmed values of voltage and current, and the built-in priority logic, the compiler would first determine which class of supply should be used. (In this case, a Class 2 supply is preferred, initially at least, as there are more of these available.)
2) Using the programmed UUT terminals and its own equipment assignment tables, the compiler would next determine if any supply of the selected class has already been assigned to the specified UUT pins.
3) If yes, the necessary machine coding for that supply can be generated.
4) If no, the compiler would select the next available supply of that class, enter its assignment and UUT pin designations into its assignment tables, and generate the necessary machine coding for that supply.

If this process cannot be carried through to a logical conclusion, an error message should be generated informing the test programmer of the specific problem encountered. The cause might be

1) An insufficient quantity of supplies,
2) A request for more load current than can be provided, or
3) The specification of an excessively fine voltage step, such as 0.155V, for example.

Here again, the amount of aid given the test programmer can vary with the sophistication of the compiler and the ATE system. Thus, in the event of an inadequate number of supplies, the compiler could merely give an error message, or it could automatically select, assign, and program some general-purpose switching relays to allow one supply to be time-shared among several UUT points.

For some stimulus parameters, the method of implementing and coding a stimulus function may differ greatly depending on the value of one of the parameters. Consider, for example, a sinewave stimulus. The generation of frequencies in the range 0.001 to 0.1 Hz might be done by having the ATE computer program a timed sequence of small DC voltage steps to a digital-to-analog-converter and filter out the resultant steps. Over the range 0.1 Hz to 500 MHz, one of a family of conventional oscillators might be used with only the simple programming of a single device required. For the range 500 MHz to 20 GHz, a more complex frequency synthesis method (requiring the programming of several stimulus devices and routing switches) may be required. All of these operations should, of course, be handled automatically by the compiler.

Two other areas where a compiler can effectively assign ATE equipment functions are measurement test points and general-purpose switching. Consider the source statement: MEASURE 15.0 VDC $\pm$5%, J1-1 (HI), J2-5 (LO). Before a measurement test point can be programmed by the compiler, the compiler would search the appropriate equipment table to determine if test points had already been assigned to the designated UUT points. If so, they would be used; if not, the next available test points would be selected, assigned in the table, and coded automatically.

General-purpose switching is more difficult to handle. In addition to the automatic implementation of stimulus switching already noted, several other applications will be mentioned. To connect two points in the UUT, a source statement might be defined:

CONNECT J1-1 to J2-5.

The compiler could automatically select an available switching relay, assign its contacts to the specified UUT pins, and generate the necessary coding to operate the relay. To accommodate more complex switching requirements, two switching statements could be defined:

```
SWITCH ON     A, B, C, · · ·
SWITCH OFF    L, M, N, · · ·
```

where A, B, · · · are mnemonic names of switches the wiring of which could have been previously defined by the test program in a source-language statement in the program preamble. These mnemonic names may be selected completely arbitrarily by the test designer or programmer in a way to facilitate their use and identification both for himself and for subsequent readers of the test program. The names might identify a UUT input or output (such as INPUT, AUX 1, PWIN, BIAS, etc.) or they might identify the UUT pin that they control.

Interface Wiring

Irrespective of the method used to implement the ATE-UUT interface on any particular assembly or subassembly UUT test system, there will be some unique wiring requirements for each UUT. As a minimum, this may be only the adapter cable from the ATE connector to the UUT or it may also include a patch panel as in the case of LCSS.[6] Note from the previous discussion that as the compiler assigns and programs equipment, it is essentially designing this ATE-UUT interface. When the compiler completes processing the source statements, the assignment tables will contain such entries as

ATE Equipment	*UUT Connector Pin*
PS1	J1-1
PS2	J1-5
DA3	J1-6
TPA-1	J2-1
TPA-2	J2-10

With this information already available, it is a simple matter to build into the compiler the connector and pin designations where each stimulus, switch, and test point terminates at the connector panel or the patch panel. Thus, an interface wiring list can be prepared automatically, either as a simple listing useful only as a test program adjunct or elaborate enough to fulfill the interface fabrication requirements. This latter type of listing could include wire type and size designations and connector part numbers, if desired.

This area of equipment selection and interface design can vary greatly in the level of sophistication employed in the compiler. Assignments can be made on a simple sequential priority system or some degree of assignment optimization may be attempted. This process could involve, for example, 1) the selection of stimulus supplies to minimize the chance of using up all supplies of any one class or 2) the selection of all equipment (supplies, test points, switches, etc.) to optimize the wiring of the interface cable and/or patch board.

UNIVERSAL TEST EQUIPMENT COMPILER

ASD is currently developing a Universal Test Equipment Compiler (UTEC) which is based on defining the source language and the ATE system characteristics using a special UTEC metalanguage. This compiler represents a major investment by the Army Missile Command in a self-adapting software system that can be adapted to a variety of test systems and a variety of computers. Once UTEC is completed and operating for a computer-controlled test system, it can be adapted to another test system containing the same computer by changing only the test-system metalanguage definitions; the UTEC program coding does not require modification. To adapt the compiler to a new test-system computer, UTEC would require only the addition of an assembler specifically designed for that computer. Test programs written for one system can be recompiled for another system provided the basic test capability and the source language for the two systems are compatible.

This compiler universality stems from the following UTEC features:

The level and organization of the basic source language is high enough to accommodate most of the known automatic test systems.

The test-program translation process is driven and controlled by logic and data contained in tables prepared by the compiler itself from definitions of the test language and the test system prepared in the UTEC metalanguage.

The UTEC program is coded in FORTRAN IV and has its storage tables compatible with both a 32-bit and a 36-bit word length, thus allowing it to operate any medium-to-large second or third generation computer that has a FORTRAN IV system.

A design objective for the compiler is to configure the basic compiler structure to have a maximum compatibility with other types of RCA Army ATE systems, particularly with DIMATE.[8]

FUTURE DEVELOPMENTS

Several studies performed in support of the ATE software developments have identified areas of future development for ATE compilers and related software. These include

1) A more general method of language definition and translation.
2) A more general method of adapting the basic compiler to different ATE computer types.
3) Expand the UTEC logic in the area of optimizing the ATE-UUT interface design and patchboard wiring.
4) Provide an automatic flow-chart-drawing capability.
5) Provide a greater level of software support to the program validation effort.

In addition, the extension of UTEC to include a DIMATE[7] compiling capability is anticipated.

Item 5) above is particularly attractive, as the cost of validating diagnostic test programs can be nearly half the total cost of preparing programs. With the present programming approach for both DIMATE and LCSS, the test designer prepares his program in source language. However, during validation he is forced to work in terms of machine language and/or symbolic language for making changes to the program or for observing information stored in memory or in a register. Thus, in spite of the compiler, the test validator must become intimately familiar with these lower-level languages. The dependence on these languages would be eliminated by the development of a software validation package that would operate in the ATE computer during validation and would 1) allow on-line program changes, additions, or deletions to be made in compiler source language and 2) display requested stored portions of the test program in a form that relates to the original source language. A study of these validation aids is currently in progress.

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2. Stockton, E. M. and Douglas, D. A., "Electronic and Electro-Optic Automatic Test Equipment for Field Array Use," Presented at 6th Reliability and Maintainability Conference, Florida, July 1967.
3. Scheff, B. H., "A Simple User-Oriented Compiler Source Language for Programming Automatic Test Equipment" *Comm. of the ACM*, v9, n4, April 1966.
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5. Preliminary pending the completion and approval of the ATLAS language specification. These samples are based on the work of the first four subcommittee sessions.
6. Liguori, F. and Toscano, P. M., "Land Combat Support System (LCSS) Patchboard Wiring Designs for Shared Adapter Optimization," IEEE, St. Louis, Nov. 1966.
7. At the present time DIMATE programs are prepared with a compiler unique to DIMATE and operating on the 301 at ASD.
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Automatic electro-optic testing using LCSS

P. Bokros

The Land Combat Support System (LCSS) provides maintenance support of major assemblies and subassemblies of the Shillelagh, Lance and TOW missile systems. At the present time the LCSS is the only operational, fully militarized multisystem automatic test equipment (ATE) available to the U.S. Army. The unique capability of LCSS to provide test and repair capabilities for sophisticated electro-optical equipment represents a state-of-the-art achievement in the automation of heretofore complex laboratory procedures. Although a wide range of test stimuli and measurement devices has been provided, this paper concerns itself only with the electro-optical testing capabilities of the system.

THE Aerospace Systems Division has completed and delivered to the U.S. Army Missile Command three developmental and nine interim support models of LCSS. Each LCSS consists of two shelters commonly identified as "electronic test group No. 3" (ETG-3) and "repair and storage group" (RSG-1), now designated AN/TSM-93 and -94, respectively. The ETG-3 provides automatic test and repair facilities for the maintenance of the weapon system assemblies and subassemblies. The RSG-1 furnishes additional repair space and storage for special tools and fixtures.

IR OPTICAL TRACKING

Both the SHILLELAGH and the Tow missile systems have IR tracking beacons. In the case of SHILLELAGH, an IR command link as well as tracking is utilized. The Tow system employs an IR tracker (sight sensor) and provides missile control by means of a trailing wire. Both systems represent complex, up-to-date armor-defeating weapons. The SHILLELAGH system is designed to be mounted on a tank while the Tow system will replace the 106-mm recoilless rifle and the ENTAC missile system. Tow is tripod-mounted and man-transportable. It is also adaptable to helicopter-mounted applications.

Since both SHILLELAGH and Tow contain electro-optical assemblies, a consideration of the tasks associated with the testing of these systems illustrates the LCSS approach to field testing of modern land-combat missile systems containing electro-optics. The two electro-optical assemblies which LCSS supports in the SHILLELAGH system are the tracker and the transmitter.

The SHILLELAGH optical tracker receives infrared energy from a missile source and converts it into signals that are proportional to the position of the missile with respect to the line of sight. All functions within the tracker are programmed to vary as the distance between the missile and the tracker changes. The tracker is essentially an electro-optical-mechanical device. In practice, the gunner aims a telescope at the target and fires the missile. The telescope is mechanically coupled to the tracker. During the flight of the missile, the telescope crosshair is maintained on the target. The tracker "looks" at the IR beacon on the missile and provides output signals proportional to the missile deviation from the telescope/target line of sight. These signals are applied to the processing circuitry. The proper flight correction is then sent to the missile by two IR data beams from the IR transmitter; one beam is used for pitch and the other for yaw control.

To test the operation of the tracker, it is necessary to simulate a missile beacon and determine the reaction of the tracker to various angular offsets from the boresight. In addition, it is necessary to determine the reaction of the tracker detectors to various levels of missile beacon incident energy at a number of points of the program cycle. The LCSS electro-optical equipment used in tracker checkout consists of an IR energy source, an optical collimator, a radiometer, optical filter networks, and a cam-positioned rotatable table. The Tow sight sensor tests are similar to the SHILLELAGH tests and will not be discussed separately.

ETG-3 OPTICAL TEST CAPABILITY

The optical test capability of LCSS has been incorporated into the ETG-3 in the form of an adapter. An LCSS for the support of non-optical missile systems may be configured by omitting the optical subsystem from the shelter. Some of these systems manufactured by ASD and presently used for specialized applications have been delivered without the optical test capability.

A cutaway pictorial of a field-deployed LCSS is shown in Fig. 1. The electro-optical components of the system are shown on the left side of the shelter. A line drawing of the optical test area within the ETG-3 shelter is shown in Fig. 2. Both the detector adapter and the source adapter are shown. The detector adapter is used to perform the required optical testing of the SHILLELAGH tracker; the source adapter is used in the testing of the SHILLELAGH transmitter. Both units are nitrogen purged and pressurized to approximately 5 psi.

The detector adapter is essentially an IR stimulus generator with programmed intensity outputs and the capability to simulate tracking errors

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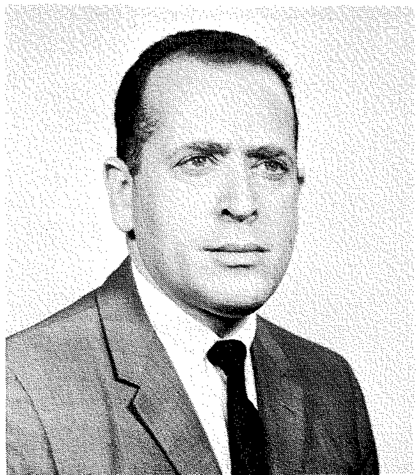

Reprint RE-14-2-5
Final manuscript received June 10, 1968.

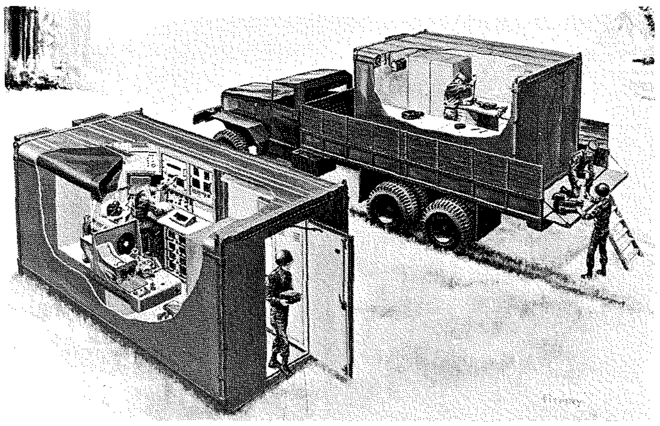

Fig. 1—Field deployed LCSS.

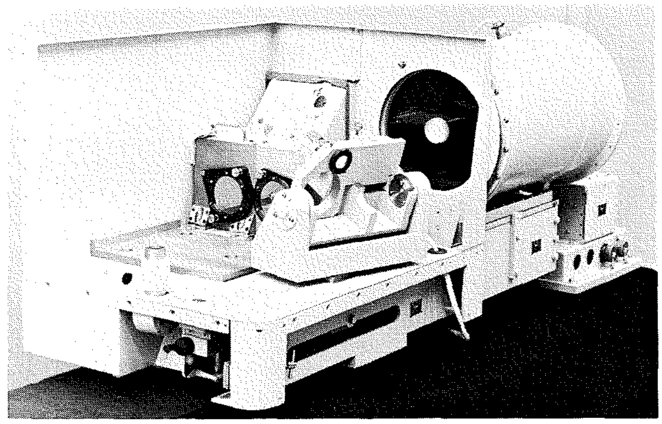

Fig. 3—Source detector adapter prior to installation in shelter.

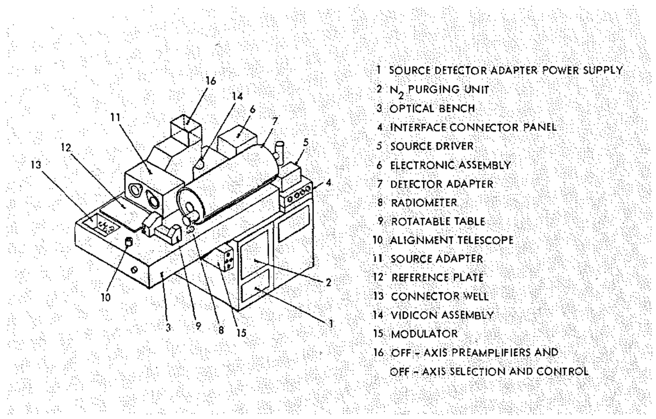

Fig. 2—Optical test area.

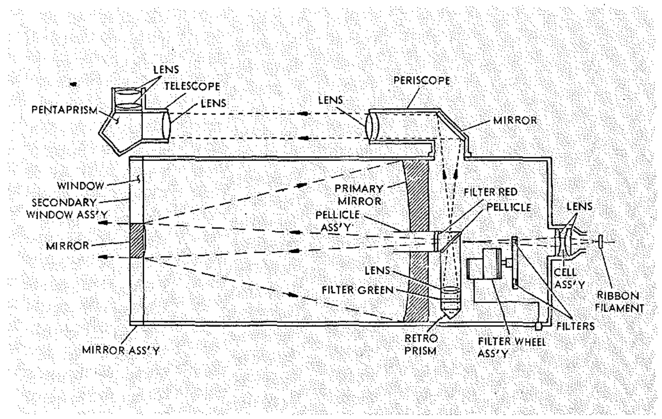

Fig. 4—Detector adapter optical configuration.

by angular displacement of the unit under test (UUT) optical axis.

The radiation intensity is controlled by a stepper motor-operated filter wheel. The wheel permits the selection of one of twelve spectrally selective or attenuating positions. The collimated beam has a maximum divergence of 0.25 mrad (milliradians) total angle. It is available from a clear exit aperture of 9.970-inch diameter. Center blocking of aperture is no greater than 2 inches in diameter.

The simulation of the UUT optical axis angular displacement (tracking error) is accomplished by positioning the rotatable table to one of 64 discrete angular offsets. Thirty-two offsets are provided for both pitch and yaw. The selected offset is obtained by cam position selection by the rotation of pitch and yaw control knobs. The range of offsets from boresight varies from 0.325 mrad to 43.63 mrad. An angular displacement accuracy of ±8.663 arc sec is obtainable. Cam position indication is provided by a pitch and yaw indicator dial. Boresight alignment is performed optically by a built-in alignment telescope. It results in a zero alignment accuracy of 0.03 mrad of collimator optical axis. The SHILLELAGH tracker is installed on the table by means of a special mounting fixture, while the Tow sight sensor mounts directly on the table. The principal components of the detector adapter can be seen as part of Fig. 2.

A "side-by-side" arrangement of the mounting of major components used in testing of the trackers and transmitter utilizes a common optical test bench. A combination of longitudinal beams and lateral ties, instead of a cast table, provides weight reduction. A three-point mounting system under full load with components and units under test permits base deflection of no more than 0.05 mrad during test operation. To satisfy optical equipment cleanliness requirements, a clean work area is included in the ETG-3. This area uses a filtered laminar air-flow concept. Air is prefiltered and then drawn through 0.3 micron high efficiency filters at an average rate of 250 ft³/min. A photograph of the source/detector adapter (before installation) is shown in Fig. 3.

An examination of Fig. 4 shows the basic detector adapter optical configuration. The IR energy source is provided by tungsten ribbon filament source. A GE-T10 lamp having a quartz envelope with a life expectancy of 150 hours is used. The filament is operated at a color temperature of 2800°K.

The beam is focused by the lens assembly, passed through the selected filter in the filter wheel and projected through the pellicle and the red filter to the mirror mounted on the secondary window assembly. The beam is then folded back to the primary mirror, which then projects it through the window to the tracker under test. The primary mirror is an ellipsoidal section made of fused quartz. The ellipsoid has a spherical radius of 39.935 inches, has a polished aluminized surface with minimum reflection of 90% within the specified spectral requirement, and has a blur circle of less than 5 arc seconds.

The overall diameter of the primary mirror is 10.250 inches with a clear entrance aperture of 2-inch diameter. Cemented to the SHILLELAGH tracker mounting fixture on the rotatable table is a flat mirror which reflects the position of the collimated beam back through the collimator for table boresight alignment. The reflected energy is returned through the red filter to the pellicle which reflects it through the periscope mirror, the pentaprism, and the telescope optical system to the viewing lens. At this point, the reflected beam appears to the operator as a small red dot. The position of the dot is determined by the angular offset of the rotatable table from boresight. A further examination of Fig. 4 shows that the primary energy from the source after passing through the selected filter also encounters the pellicle. Most of this energy is directed into the collimator but a portion of it is routed through the telescope lens, the green filter and the retroprism to the periscope mirror and, finally, to the telescope viewing lens. This portion of the energy appears to the observer as a small green dot. The relative positions of the two dots are a function of the table deviation from boresight. To boresight the table optically, the operator adjusts two vernier controls (pitch and yaw) on the table. Boresight is indicated when the red and green dots appear superimposed. The vernier adjustment is effective over a field-of-view of 4 mrad total angle. Once the table has been boresighted, all other offsets are provided by merely placing the pitch and yaw control to the desired offset position. The design of the cam positions, which determines the table offset, ensures the selected angular deviation from boresight to 64 discrete positions within the specified tolerance. As a result, the selection of table offsets becomes a non-critical operation which can be performed by relatively low skilled personnel.

SOURCE ADAPTER

As mentioned previously, the source adapter is used to test the SHILLELAGH command transmitter. Its principal components are indicated in Fig. 2. Basically, it is a complex infrared receiver which converts inputs into electrical signals. It is designed to operate over the specified electro-magnetic spectrum, and it provides outputs which are evaluated by the electronic subsystems of ETG-3. Functionally, the source adapter is divided into the following units:

1) Optics
2) Detector array
3) Vidicon Camera
4) Electronics

A mechanical reference plate is used to mount the SHILLELAGH transmitter under test in front of the source adapter. This plate is aligned within 0.1 mrad versus the source adapter optical axis.

The analysis of the SHILLELAGH transmitter IR beam is performed by an array of 13 detectors and the vidicon camera. The detector array consists of 13 discrete lead sulfide detectors arranged in a cross pattern in a common image plane. One of the detectors is located on the optical axis and the rest are offset at the 3, 10, and 17 mrad points along the horizontal and vertical axes. The outputs of the individual detectors are sampled to determine the intensity distribution of the incident beam. The vidicon camera performs an analysis of the circular IR beam. It tests the beam optical axis alignment, beam focus, and pattern.

The input power from the transmitter under test to the source adapter can be attenuated by manually inserted attenuators. Fig. 5 shows the principal

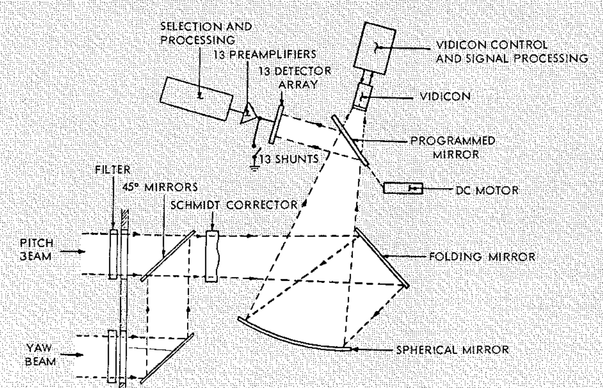

Fig. 5—Source adapter functions.

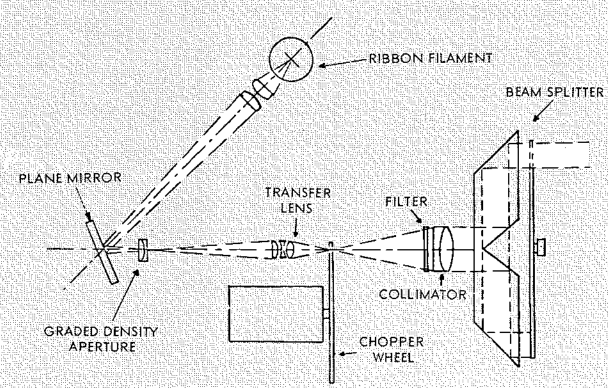

Fig. 7—Test source, reference source.

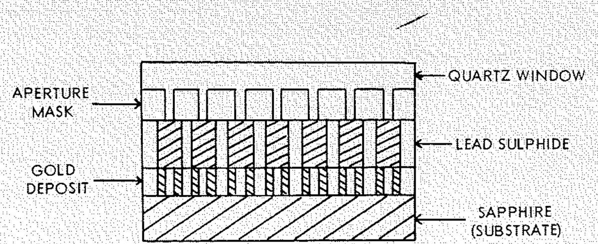

Fig. 6—Lead sulfide detector array.

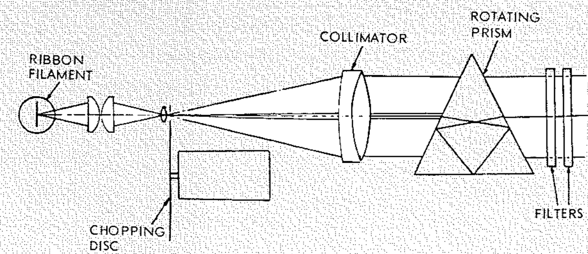

Fig. 8—Intensity test source.

source adapter functional components. The optical components are discussed in the sequence in which they are encountered by the incoming IR beams.

The two entrance apertures of the source adapter are clear optical glass windows with diameters of 3.3 inches. The spacing is compatible with the windows of the SHILLELAGH transmitter. Since the two beams are individually evaluated, it is necessary to provide optics to image the beam energy from either transmitter window on one common axis. This function is accomplished by the combining mirror assembly. The assembly essentially consists of two mirrors. The upper mirror has a clear area of 5.68x3.724 inches. It is made from fused quartz glass and is 0.5 inches thick. Both sides are polished. One side is coated for $30 \pm 2\%$ average transmission attenuation and the other for $30 \pm 2\%$ average reflection attenuation for incident 45° beams in the specified spectral range. The lower mirror has a clear area of 5.12x3.724 inches. It is similarly constructed; however, only one side is coated for a minimum reflection of 95% for incident energy at 45°. The above described arrangement permits individual beam analysis and introduces about 30% attenuation in either optical path.

The focusing of the beam energy on either the detector array or the vidicon target is a function of the bonded optical assembly consisting of the Schmidt corrector, folding mirror, spherical mirror, and programmed mirror. The arrangement is essentially a folded Schmidt system. The corrector has a clear area of 3.88 inches and a thickness of 0.750 inches. The folding mirror directs beam energy from the corrector to the spherical mirror, the aluminized surface of which is coated with silicon monoxide and is flat to 0.5461 micron. The spherical mirror has a radius of 15.212 inches. The programmed mirror is used to direct the beam to the 13 detector array of the vidicon circuitry. The position of the mirror is controlled by a DC motor. When the mirror is activated to the "intensity measurement" position, the IR energy under investigation is incident on the detector array and results in an output proportional to its intensity from the 13 detectors. The array is 1.25 inches long and 1.22 inches in diameter. Individual lead-sulphide detectors are deposited on a sapphire substrate. Lead sulfide is used to obtain relatively uniform response over the near-infrared wavelengths. The array itself is mounted behind an aperture plate with 13 openings, each with a diameter of 0.01 inches. The entire array is temperature controlled and the aperture plate is protected by a quartz window. The front of the array can be visually illuminated for alignment purposes during system installation.

Initial factory installation includes the checking of the center detector alignment against an autocollimator reticle. Analysis of the SHILLELAGH transmitter beam intensity distribution is performed by sampling the outputs of the individual detectors.

Fig. 6 shows the detector array construction, the quartz window, aperture plate, lead-sulfide detectors and substrate. Gold deposited conducting paths on the individual detectors are shown.

In addition to the off-axis beam intensity measurements performed by the detector array, a number of other tests can be performed by the source adapter. By programming the sliding mirror into the vidicon position, it is possible to determine beam boresight, beam width, and pattern, as well as transmitter mirror adjustment. Specific tests which are performed on a transmitter include pitch and yaw on-axis and off-axis intensity and intensity variation as a function of lamp turn-on time.

LOSS ELECTRO-OPTICS SELF-TEST

The LCSS self-test philosophy encompasses a wide range of system performance techniques. These include the use of continually monitoring devices as well as the utilization of internal electrical and optical standards. The source adapter is maintenance calibrated by two optical self-test units. The checking of the optics and electronics associated with the vidicon portion of the source adapter is performed by the self-test reference source. The purpose of this device is to simulate the unit under test beam characteristics which permit the maintenance calibration of the vidicon camera and processing circuits. In this manner, it is possible to check the beam pattern, boresight, and width analyzing capability of the vidicon chain. The functional components of the test source are shown in Fig. 7. The entire unit consists of a precision machined enclosure which insures proper alignment of the test source and the source adapter when the test source is mounted in position in place of the unit under test. The optical components consist of a ribbon filament lamp, a plane mirror, a graded density aperture, a transfer lens subassembly, a chopper wheel, a filter and collimator subassembly, and a beam-splitting prism. The output is obtained from one of two externally controlled apertures. The purpose of the graded apertures is to simulate the unit under test energy distribution.

Fig. 8 represents the optical components of the intensity test source used to verify the source adapter subsystems associated with the measurement of SHILLELAGH transmitter off-axis beam intensity. This standard is provided with a single exit window which provides illumination for the detector array. The unit consists of a vertically oriented tungsten ribbon which is imaged into a field lens prior to being modulated by a chopping disc. The energy is next collimated and directed to a rotating prism which projects the beam on the detector array. The prism is used since the projected beam width is not sufficiently wide to cover adequately the entire array at one time.

Maintenance calibration of the detector adapter is performed by a radiometer (Fig. 2). The intensity of the detector adapter output, in conjunction with specified filters in the filter wheels, is verified with the radiometer. The entire unit is self-contained and subjected to a calibration by NBS secondary standards at 90-day intervals. The second calibration period applies to the other two above described test sources.

CONCLUSION

The existing electro-optical testing and maintenance capabilities of LCSS have provided the Army with the required means for field support of optical combat systems. Intricate operations which, in the past, required participation by highly skilled technicians in controlled laboratory environments are now performed by relatively low skilled Army personnel in a tactical field situation.

The DIMATE system—programming and experiences

R. N. Knox

This paper reviews the DIMATE (depot-installed maintenance automatic test equipment) system organization, machine language, and compiler program interface with software support procedures and hardware. It then describes some of the experiences and techniques developed in the preparation of programs for production testing of FM and AM transmitters and receivers. It tells the steps in obtaining useful data on the unit to be tested, why bench testing is necessary to obtain data for good test results, why the test philosophy for a unit should consider the past test history, and why the user should help establish the test philosophy.

Among automatic support systems, the DIMATE (depot installed maintenance test equipment) at the Army Depot in Tobyhanna, Pa., is one of those capable of performing production-type service on complex electronics communications equipment (Fig. 1). The Tobyhanna equipment is the first of several equipments to be delivered to the Army Electronics Command.

The configuration of DIMATE subsystems (Fig. 2) currently used to check high population electronic equipments, consists essentially of three subsystems:

1) A switching subsystem which interfaces with the UUT (unit under test);
2) The stimulus and measurement subsystems; and
3) The computer controller subsystem.

The computer controller subsystem interfaces with the control and display subsystem.

DIMATE has a repertoire of 57 different computer instructions and 28 different controller commands with a large complement of switching commands. Under the control of the program instructions, the computer feeds the controller switching commands and the controller feeds data back to the computer where the program operates on it using the many programmed subroutines to perform calculations and comparisons. Test results and operator instructions are fed through the controller to a printer. The DIMATE machine uses alphanumeric, mnemonics codes which can be typed directly into the controller or fed from memory during automatic program execution. Computer instructions, which may be interpreted in octal, are recognized by DIMATE in binary-coded Fieldata format.

MACHINE LANGUAGE AND PROGRAM GENERATION

Tables I, II, and III show typical computer, controller, and switching data instructions and characters used. It should be pointed out, even machine language attempts to communicate the function performed. Today, however, virtually all programs are generated in a test-oriented source language assembled and compiled on an RCA-301 computer.

Table I—Typical Computer Instructions.

Op Code octal	Op Code binary	operation name	mnemonic
35	011 101	Transfer on overflow	TRO
36	011 110	Interrupt select	INS
37	011 111	Halt	HLT
40	100 000	Write one word	WRO
41	100 001	Write continuously	WRC

The program generation process is represented in Fig. 3 which shows the steps from test design flow charting to final document preparation and final listing of a verified and validated program. Examples of languages used in the source deck, object deck, and program tape, as well as the adapter design, are shown in Tables IV, V, and VI.

The output of the compilation is a fanfold wire listing of interconnections from ATE to UUT, a source program listing in abbreviated English notation, and an assembly listing in machine language.

The DIMATE compiler accepts an input which is a test-oriented English language and translates it into a machine-language which can be executed on DIMATE[1]. In addition to the normal

Fig. 1—DIMATE system at Tobyhanna Army Depot.

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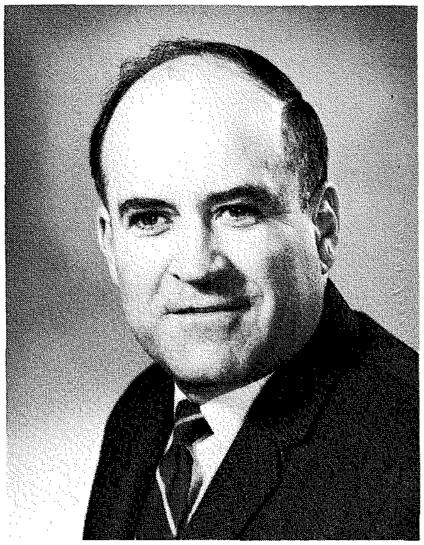

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received the BS in Electrical Engineering from Iowa State University in 1943. Joining RCA upon graduation, he worked as an engineer in audio communication design and communications equipment. Since 1956 he has been involved in computer work and was responsible for installation and checkout of the first data processor delivered by RCA. Subsequently he worked in the automatic test equipment design group in the area of input/output, including the specification and integration of printers, perforated tape readers, magnetic tape transports, and keyboard devices with the Automatic Test Equipment. At present, working in applied test design, Mr. Knox has written programs for testing of communications equipment, digital equipments, and analog circuit subassemblies on three of RCA's Automatic Test Equipment systems. He has coordinated major programming efforts which include the use of programming aids such as compilers and interpretive simulators.

translating and assembling functions, the compiler also

1) Automatically generates a wiring connection list for interfacing the UUT to the DIMATE;

2) Automatically assigns DIMATE commodities (such as relays and power supplies) while maintaining an inventory of items in use as the program progresses;

3) Inserts commonly used subroutines and macro routines into the working UUT test program;

4) Provides for segmentation of programs requiring more than one memory load; and

5) Checks the legality of all source language statements flagging all violations.

These, then, are the tools the test designer uses to create a verified tape for his program. But there is a substantial bench testing and UUT analysis effort involved before this point is reached. Furthermore, there is a considerable validation effort involving a number of program changes before the program is considered usable for production testing.

The information supplied to the engineer preparing the program is usually the standard, approved documentation for manual production and acceptance testing and/or depot inspection testing of the equipments using bench-type test procedures. Documentation includes technical manuals with schematics, wiring diagrams, detail drawings, and photographs. Depot inspection specifications and repair procedures might also be included. In any case, one specific document closest to the needs of a depot specification is designated as the contractual requirement for test performance. Because this document details a procedure to be used with a combination of general purpose oscillators, generators and meters in conjunction with special purpose switching panels and adapters, a thorough analysis is required to understand the intent and performance requirements of the document.

Table II—Typical Controller Instructions.

Command names (if funct. groups)	*Symbolic code*	*abridged descriptions*
Program Control Group		
Jump	J	Unconditionally transfers program control to a new test for the current UUT, as specified by the controller program.
Branch High	Y	On the condition that a *comparison high* condition exists, this command transfers program control to a new test for the current UUT, as specified by the controller program.
Branch Low	Z	On the condition that a *comparison low* condition exists, this command transfers program control to a new test for the current UUT, as specified by the controller program.

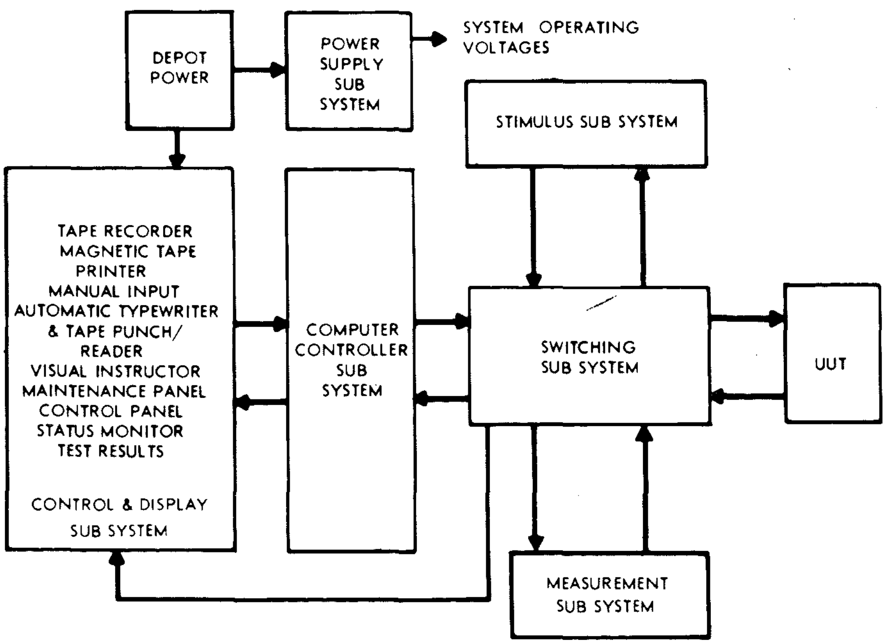

Fig. 2—DIMATE functional block diagram.

PROGRAM INTEGRATION AND VALIDATION

Because the DIMATE interface is not the same as the bench equipments, changes in approach are usually required. As an example, the DIMATE RF measurement subsystem routes signals through coaxial cable at 50 ohms matched impedances. Hence, in one test requirement, it could not duplicate the measurement of a bench set-up, which used the electrostatic pick-up of the tube shield of an oscillator to measure the oscillator frequency. However, through bench analysis of the unit and rechecking of DIMATE, an alternate means of picking up the signal at a discriminator transformer proved successful.

Table III—Typical Switching Data.

Switching address	Subaddress or Code No. in SD1 position	Assembly and/or function
AC4	R, S, T	Primary power control, 400 Hz
ACS	1, 2, 4, R	Primary power control, 60 Hz
ADC	1, 2, R	Primary power control, 28 VDC depot power
AFG	A, R, S	AF synthesizer
AFS	0-7, R	DC/AF switch subassembly
AMP	A, F, R, S	Audio amplifier

Table IV—Compiler to-from Wire Listing for Adapter Design.

Flag	Compile Function	Test Pt.	0710D	Wire List Printout From - Dimate - to	From - U.U.T. - to
		A08	A13J 1-C		J100A
	5-36 VDC 1	A09	A13J 1-G		J100C
	5-36 VDC 2	B07	A13J 1-J		J100D
	RET. J1-G	A49	A13J 5-K		J100U

Table V—Compiler Source Listing.

012A	Print Transmit Control Line Shorted					0312
T013	Measure 60.00	Ohms	+0	———	J203B	0313
	Go To ————A-		014			0314
013A	Print Transmit Control Line Open					0315
T014	Measure 10	Ohms	+0	———	J202F	0316
	Go To ————A-		015			0317
014A	Print Transmit Control Common Open					0318
T015	Measure 120.0	Ohms	50.0	J203C	J203D	0319
	Go To ————A————A		016			0320

Table VI—Compiler Object Listing.

00517	LINE						CD		LINE SHORTED	0312	
00520	SHO										
00521	RTED										
00522	@										
00523	C						CD		C	0313	
00524	*	36	0	0	0002	1$013	INS	0	2	0313	
00525		41	0	0	0526		WRC		*+1	0313	
00526	$STPB						CD		STPB3131MRE2M113@AD11000TEMU0006000C	0313	
00527	3131										
00530	MRE2										
00531	M113										
00532	@AD1										
00533	1000										0710374
00534	TEMU										
00535	0006										
00536	000C										
00537	*	30	0	0	4122		IRE		PRNMES	0313	

For an initial DIMATE program prepared for the Electronics Command, chronological adherence to the depot inspection standard was maintained. Subsequent validation proved the discriminator tests which were most likely to fail should have been at the beginning of the program. Bench testing is valuable to establish test values, limits, impedance interfaces, and test points; but failure mode history must be supplied by those familiar with the equipment being programmed. A design review meeting was held with the customer to establish test philosophy based on experience. With the test approach resolved, final flow charting, documentation, coding, and compiling were completed.

The DIMATE Compiler has several programmed subroutines such as increment, add, subtract, multiply, divide, and compare. These subroutines can make the detailed programming much easier as only the arguments or variable data need be given with the called subroutine. In addition to program subroutines, test subroutines such as measuring IF bandpass, discriminator response, and incrementing of power for variable loads have been developed. Each time a new subroutine is added or expanded, additional effort for debugging and validation is required. However, as the repertoire of routines increases, new programs are more efficiently programmed and validated.

Validating programs can become a complicated problem because many unknowns are involved in the first run of a test. Among the problem factors might be a fault in the unit being tested, improper test limits, a coding error in the program, an error in the adapter interface wiring between the UUT and the DIMATE system, a malfunction of DIMATE itself, or an unproven subroutine. The goal of the test engineers, maintenance crew, technicians and others that are working in support of the validation effort is to prevent problem factors from occurring together.

DIMATE DEPOT USE, OPERATION, AND PERFORMANCE

During a period of extensive testing of one particular type of communication equipment, an important aspect of DIMATE utilization was vividly demonstrated. A new personnel communication radio set introduced into the Army became the subject of numerous unserviceable equipment reports from field troops using it. Acting upon these reports, depot testing was initiated on all sets prior to shipment. As the equipment was in great demand and urgently required, it was decided to utilize ATE to forestall any supply delay and accomplish the testing economically. Initial testing totalling 5,000 units showed the average test time per unit was 8 minutes in contrast to a manual test time of over 35 minutes—including setup time in both cases. The capability of detecting specific deficiencies within the equipment that had previously gone undetected was a valuable extra. Reports of the quantities and type of deficiencies, as noted through ATE testing at Tobyhanna, were forwarded to the manufacturer. His investigation of these reports resulted in agreement that rejection of lots having the noted deficiencies were valid and

1) The defective equipment should be returned for rework,
2) A few engineering changes should be implemented to provide improved operation of the equipment,

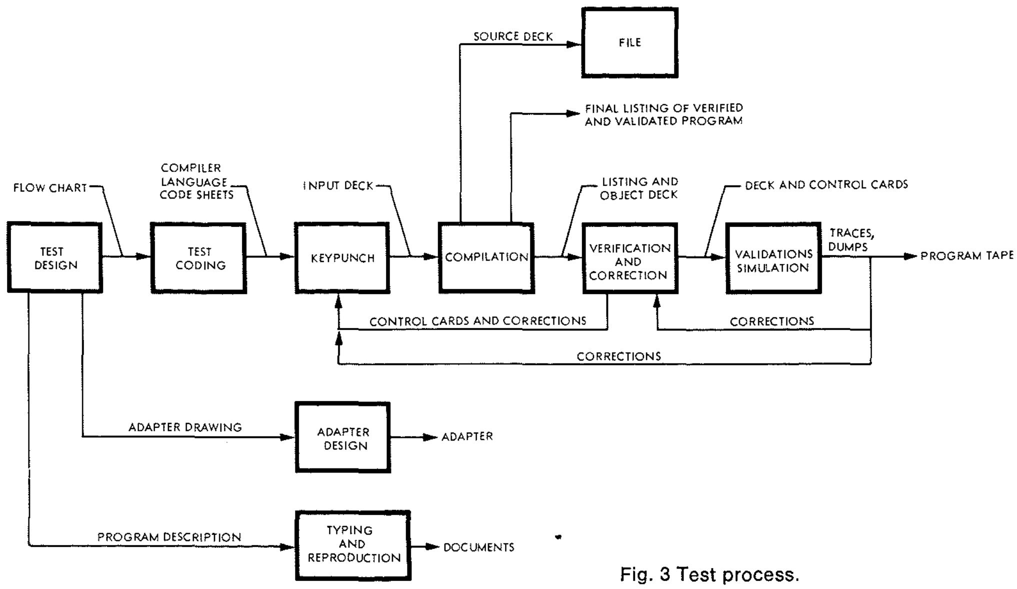

Fig. 3 Test process.

3) an effort should be made to improve workmanship in vendor material as well as in the manufacture of the complete shipment, and
4) inspection should be tightened in all phases of production.

All of these resulted in a decline from an initial 20.3% rejection rate at Tobyhanna to a low of 1.4%. The above facts are not intended to indicate the manufacturer was producing deficient equipment because of poor design. Detailed analysis of the situation indicated that the majority of problems resulted from test techniques and specifications used during factory acceptance. The ability to perform 100% acceptance testing economically rather than AQL sample acceptance testing becomes an outstanding advantage of ATE.

In the preparation, validation, and utilization of specific equipments, problems occurred not related to equipment deficiencies, but rather related to programming. One which appeared at the top of the list (and not yet satisfactorily resolved) was deciding the level of fault isolation after fault detection. Many factors affect a decision of this type. In this instance, the two major factors were the UUT adaptability to successive levels of fault isolation and diagnosis, and the reason for submission to ATE testing.

The UUT was modularly constructed, but not particularly suited economically (both in programming and operational cost) for diagnostic programming to a module level. Inaccessibility of test points was the major problem. Many test points were provided, but considerable disassembly and manual probe intervention negated any gains anticipated. A front panel connector, allowing the input and output of each module to be wired to the ATE without any set disassembly or probe intervention, could have made the decision to fault isolate undisputable. Although a basic reason for submission to ATE type testing (to determine the deficiencies of the equipment) provided justification for complete fault isolation type programming, the above mentioned test point inaccessibility restricted the program to fault detection with some fault isolation tests. The resultant program thus became somewhat a compromise, providing dividends in a lesser amount than rightfully due.

Another problem, perhaps unusual with respect to automation, was the possibility of an operator causing incomplete or invalid testing, either by his own design, as a result of distraction, or through boredom due to the simplicity of operation. The only defense against occurrences of this type is by pre-programmed self checks. Initially the programming effort briefly considered such possibilities. These were discarded as being impractical because a program is basically sequential in nature. However, under actual operation, it became apparent that any and all possibilities do become realities and must be considered and a defense established. In a pure "data processor" type program this may be an insignificant problem or not even a problem at all. Programming for checkout of electronic equipment is not the same. It is quite difficult to anticipate every reaction of the UUT as well as the operator's reactions. Once known, the self checks can be provided and invalid testing prevented.

CONCLUSION

The ATE at Tobyhanna has been utilized for testing of 50,000 units of approximately ten different species. Considerable experience has been provided both to the contractor and Tobyhanna personnel through this utilization. Our philosophy of programming acceptance and diagnostic tests for communication equipment has been revised many times in the process of preparing, validating, and utilizing each program. Every constructive change, in philosophy or in program, is a step towards the optimum in automatic testing of complex electronic equipment.

ACKNOWLEDGEMENT

Essential contributions to this paper were also made by Mr. W. Morris of the Tobyhanna Army Depot, Tobyhanna, Pennsylvania.

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Automatic test equipment for army field use

E. M. Stockton

D. A. Douglas

The modern army will deploy large numbers of guided missile systems in the field to achieve unprecedented gains in fire power, accuracy, and response time. To preserve the operational advantages designed into all these systems, the Army Missile Command has adopted a multisystem support concept as an alternative to developing special-purpose support equipment for each missile system. The Land Combat Support System (LCSS) is the basis for field maintenance of the Shillelagh, Lance, TOW and other Army tactical missile systems. LCSS combines a number of conceptual and technological advances in automatic test equipment. A summary description of this system is given, stressing the contribution of the test system to effective maintenance and the steps taken to improve confidence in operating effectiveness.

THE GENEALOGY of the LCSS can be traced to early studies by the Army and RCA which first established the feasibility of the multisystem support concept, the use of functional building blocks in test equipment, and the potential of automating the test process. Developmental models were completed and accepted by the Army in July, 1966. Four service test models were completed the first half of 1967. Demonstration tests have been made on assemblies and subassemblies of the SHILLELAGH, LANCE and TOW plus self-tests on assemblies and cards from the LCSS.

Basically, LCSS automates complex testing to achieve:

1) Rapid evaluation of the operational status of units under test (UUTS);
2) Rapid fault isolation of failed units to the replaceable component;
3) Decision making by test set, thereby restricting operator participation to printout-directed hook-up and adjustments.

SYSTEM DESCRIPTION

A shelter-mounted test set called the Electronic Test Group No. 3 (ETG-3), a repair and storage shelter (RSG-1), interconnecting cables, and a 45-kW engine generator make up the LCSS. Fig. 1 shows the ETG-3 and RSG-1, cut away to show the test set operator's console and electro-optical test position. As shown, the shelters can be used from the back of the transporting truck or can be placed on the ground.

The LCSS is designed for transport by cargo aircraft, standard wheeled military vehicles, and by helicopter. Total weight of each shelter with equipment is approximately 6000 pounds. Each shelter includes an integral heating-cooling system which allows continuous operation throughout the global environments.

Integrated circuits are used in all control and digital applications, and this has made possible the relatively small size of the test equipment. There are two test stations and one repair station in the shelter plus storage for test tapes, cables, and adapters.

The ETG-3 system consists of a controller/data processor, input/output, measurements, electronic stimuli, switching, adapters, and internal power. The controller/data processor subsystem provides the interface between the input/output and the remainder of the ETG-3. It accepts programmed data from either the perforated tape reader or the manual input and uses this data to control the operation of the stimuli, measurements, and switching. It also accepts measurement and control data and performs algebraic addition and subtraction computations as required to determine the operational readiness and/or faulty components of units under test (UUTS).

The input/output function provides the inputs necessary for system operation as well as the outputs required by the operator. The measurement subsystem has the capability of performing frequency, time-interval, peak-voltage and resistance measurements. It receives inputs via the switching

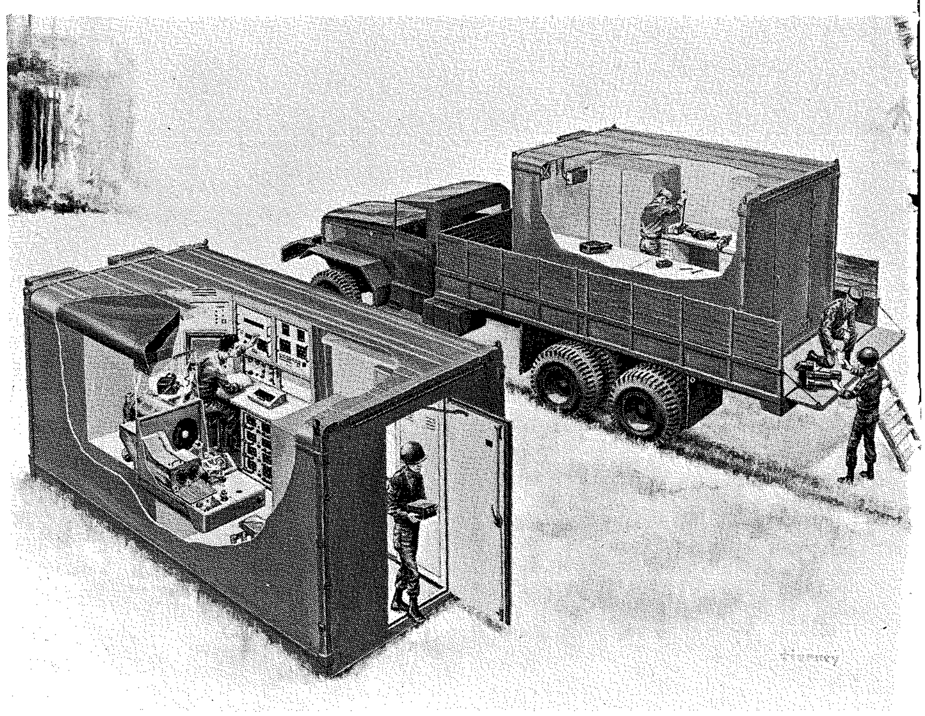

Fig. 1—LCSS in the field.

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function from the UUT and from selected self-test points in ETG-3. All these signals, whether DC, AC, or resistance, are converted to a binary coded decimal (BCD) quantity which is then routed through the controller/data processor for further processing and for decimal display. Self-test of the measurements subsystem is accomplished through the use of internal reference standards. Both AC and DC voltages from the stimulus subsystem provide both signal and power stimuli to the UUT. The DC voltages are programmable in amplitude; AC signals are programmable in amplitude, frequency, and waveform characteristic. Available to the SHILLELAGH transmitter UUTs are special signal stimuli supplied by SHILLELAGH modulator assembly (GFE). Self-test of the electronic stimuli is accomplished by routing the stimuli to the measurements function. The source and detector adapters form a subsystem for test of electro-optical devices.[1]

The switching provides the interface between the UUT and the remainder of ETG-3. Through test connector panels and under program control, signals to be monitored are routed to the measurement function. Special handling of sensitive UUT signals may be accomplished by the use of probes located on the measurement assemblies.

An external engine-generator set furnishes three-phase, four-wire power with a line-to-line voltage of 208 VAC at a frequency of 40 Hz. This prime power is supplied through the power distribution panel.

SYSTEM OPERATION

Automatic

In automatic operation, a tape is loaded onto the tape reader, the UUT is connected to the ETG-3 connector panel, and a pre-wired patchboard is inserted into the test adapter. Next, the operator selects the UUT test address by dialing the seven digi-switches located on the monitor panel. The first four digi-switches define the test tape, the patchboard, and the interface cable configuration required. The last three digi-switches represent the point in the program at which the operator desires to start the test. When the START TEST push-button is depressed, an automatic tape search is performed to locate the selected address on tape. Test number 000 represents a printout indicating in English the UUT name and number, cable hook-up data, and any other information pertinent to preparing the UUT for testing. The last word in the printout is PROCEED which signifies that the PROCEED pushbutton must be depressed before actual testing begins. If all tests are GO the printout indicates ALL TESTS GO and the ETG-3 is halted. If a test results in a NO GO, the program automatically branches to a fault isolation routine which is designed to determine which item has failed. In such a case, a repair instruction is printed out such as REPLACE BOARD A3, and the ETG-3 is halted.

Semiautomatic

In semiautomatic operation, the equipment is set up the same as for automatic operation. Portions of the program are processed automatically but manual interrupts are introduced in the program where operator participation is required. This participation is always limited to manual actions and never requires a decision to be made by the operator. Furthermore, all instructions for operator action are described on the printout or referred to technical manuals. These instructions are divided into two categories:

1) Those requiring the operator to make a change, such as connecting a probe, changing a cable, or changing a switch setting on the UUT; and
2) Those requiring that an adjustment be made on the UUT.

SELF-TEST CAPABILITY

Since a major advantage of ATE is the high test rate, test set availability is essential. Accordingly, the ETG-3 is designed for rapid maintenance through a built-in capability for automatic self-test and fault isolation. The LCSS design is based on extensive use of plug-in

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received the BEE with honors in 1956 and his MEE in 1961 from the Polytechnic Institute of Brooklyn. Mr. Douglas joined the Communications System Division of RCA in 1959 and became a Senior Project Member, Technical Staff, in 1961. He has been concerned with the development of novel data transmission systems for application to command and control. From 1962 to 1966, he has had PMO responsibility on RADAS and Minuteman Force Modernization. On RADAS, Mr. Douglas coordinated and directed an inter-divisional technical program, starting from the development of technical requirements through evaluation of the final system. On the Minuteman Force Modernization he developed technical requirements with the customer, organized the task forces to do the work, and guided and coordinated the system effort. On Minuteman Taps, Mr. Douglas established technical requirements with the customer, prepared work statements for the Systems tasks and coordinated and evaluated the technical results. Mr. Douglas was President of the New York Alumni Chapter of the Eta Kappa Nu Association.

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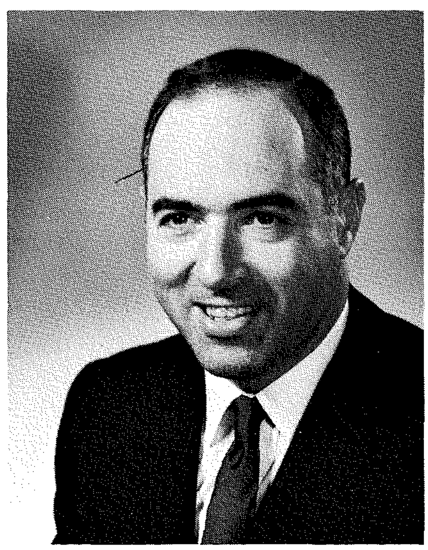
is currently responsible for the design and integration of Automatic Test Equipment and for test design and validation. Previously, as design leader, he was responsible for the design of the computer used in the multisystem test equipment developed for the Army Missile Command. Mr. Stockton joined RCA in 1955 where he was assigned to the design and development of the Air Force ASG 14 fire control system. Subsequently, he gained additional design experience in power supplies, receivers, transmitters, and synchronizers for radar devices. Since 1959, when the nucleus of the Automatic Test Equipment product line was established at RCA, he has been active in every facet of the activity, with particular emphasis in system design, computer-controller design, and system integration and test.



assemblies (boards) which materially decreases corrective maintenance down-time when spare boards are available. Further, the number of board types was reduced by function-oriented board designs which permit the use of board types in more than one application. System-level and assembly-level programs will fault isolate to the board level. Board level programs may be used to fault isolate to the board piece-part during lull and periodic maintenance periods.

The following self-test programs are used for detecting and isolating faults: confidence and maintenance, assembly self-test, subassembly self-test, and survey test leader. Additionally, continuous monitoring circuits operate fault lights and system status lights as a supplement to the self-test programs.

C & M Test Tape

The confidence and maintenance (C&M) test tape is run prior to the start of the operating day and corrective maintenance procedures. It establishes a high degree of confidence (~98%) that the ETG-3 meets the specifications by:

1) Exercising the control subsystem,
2) Comparing the measurement subsystem against the self-test reference assembly outputs, and
3) Testing the stimulus subsystem using the measurement subsystem.

Switching functions and internal power sources are checked indirectly during these tests. The optical test equipment is checked through the use of a calibrated radiometer and optical source. A NO GO in the confidence portion of the C&M test tape results in an automatic branch to a fault isolation routine which culminates in a printout identifying a faulty assembly.

SELF TEST

The self-test programs test each ETG-3 assembly and fault isolate to one subassembly or to a chassis residual piece-part. Assemblies are tested while in the normal operating position or as UUTS.

Subassembly Self Test

Subassembly self-test programs fault isolate to one part or group of parts, such as a number of components in parallel. The printer will print out the defective component nomenclature or indicate that the fault is one of a group of components. The programs are designed so that a number of sub-assemblies may be tested using the same interface cables and patchboards.

Survey Test Leader

A survey test leader normally precedes all UUT programs (weapon system and LCSS) and is limited to short duration (~30 sec.). The purpose of a survey test is to verify the performance status of stimulus and measurement devices to be employed during the program. If a survey test results in a NO GO, further fault isolation is provided by the C&M tape.

PREPARATION OF TEST PROGRAMS

The preparation of perforated tape programs for testing UUTS begins with an English-language test design (Fig. 2). Note that the design evolves from a concept to a detailed test design with a design review after each phase. Each design and review is an iterative process which continues until the reviewers are satisfied that the design is adequate.

The English-language test-design flow chart is the input to the perforated tape program production and validation process (Fig. 3). This process consists of coding, assembling, verification, and validation.

Program coding is the process of translating the flow chart logic into formal input language suitable for key-punching on a standard keyboard. The process is clerical involving almost a direct transcription of the test-oriented statements, and organization of material for compatible input into the assembly and static error inspection program (ASEIP).

Keypunching is verified by having two operators punch identical sets of data processing cards. The two sets of cards are compared.

Program assembly and static error inspection are done by computer. Control cards are added to the key-punched

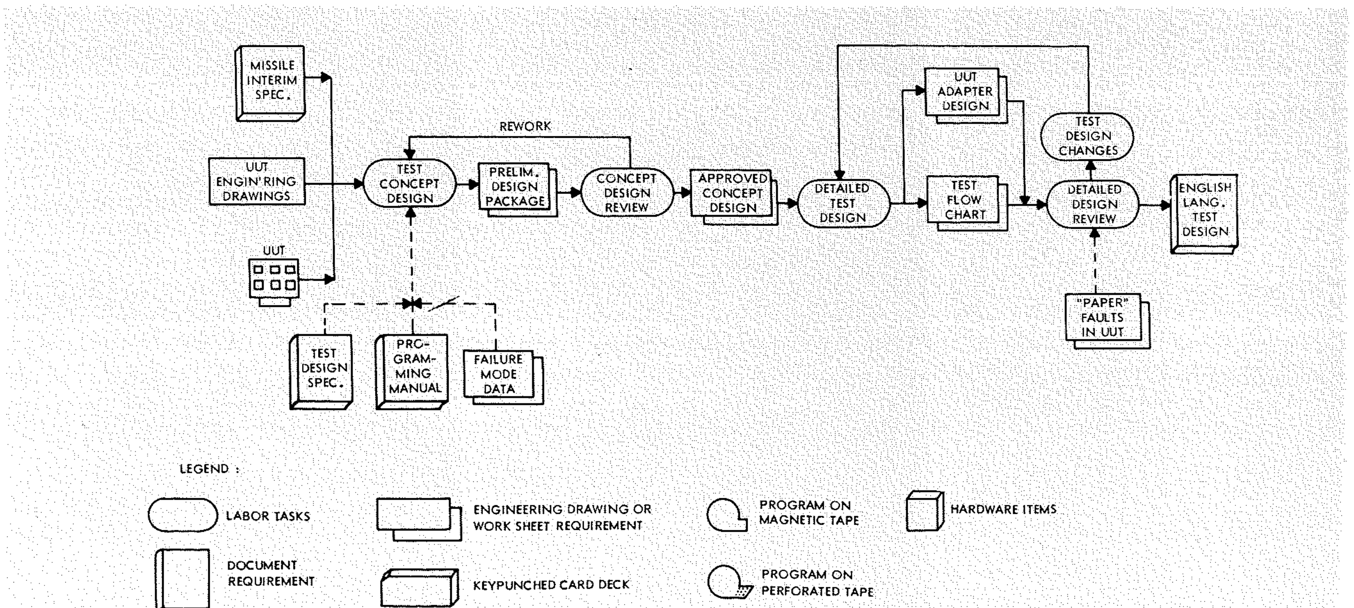


Fig. 2—English language test design process.

cards to complete the source deck for the UUT program. The control cards direct the RCA-301 general purpose computer to call in the ASEIP program from magnetic tape for execution. This is a standard set of control cards used over and over for each new UUT. The source deck, in ASEIP language is fed into the 301 system and assembled into LCSS machine language. At the same time, legality checks are made to assure that no apparent coding errors exist.

The assembly process yields a new set of punched cards called the object deck. Concurrently a printed listing of the source and object language programs is generated by the computer. The printed listing is used for verification.

Verification is a visual process of comparing the flow chart and the output list. Errors are corrected by new coding, keypunching the necessary changes and modifying the source deck. The program is then re-assembled and verified. The process is continued until the program is completely verified. The object deck is then translated into perforated tape code by the RCA-301 computer under ASEIP control. The perforated tape is then ready for validation on ETG-3.

Validation is the process of exercising the UUT on ETG-3 under the control of the newly verified program. Complete validation requires exercising the UUT in all its operational and failure modes.

A known good UUT is tested in all its operation modes. The final printout must be ALL TESTS GO. The program is corrected as required until the GO-chain is fully validated. The diagnostic routines for fault isolation are validated by forced branching. At each point in the GO-chain, a test result is forced out of limits by manual intervention of the operator via a keyboard input. This forces the machine down a NO-GO branch to a printout. Each NO-GO branch is validated in turn. At the completion of validation all GO paths and all NO-GO paths have been checked.

Now actual field failures* are introduced into the UUT to test the ability of the program to detect and isolate to the correct fault. The number of such faults inserted depends on the circuit complexity. It is not unusual to insert as many as fifty faults into the UUT. The fault insertion process frequently uncovers shortcomings in the test logic which are not revealed by forced branching.

OPERATING EXPERIENCE

The checks and controls incorporated in the test program generation process and the basic criteria for the hardware system design paid off in unprecedented results when faulty UUTs were tested. Typical field failures were inserted in the UUT, the UUT was connected to the test set, and the test program tape was run. The UUTs included a combination of assemblies, sub-assemblies, and cards from each of the two missile systems and from the ETG-3 test set. A total of 183 separate faults were inserted, including marginal and catastrophic failures. Failed components included transistors, integrated circuit chips, open capacitors, shorted transformers, etc. In each instance, the failure was detected. That is, UUTs which contained failures were correctly identified as faulty and in no instance was a good assembly called faulty. In 94% of the cases, the failed component was correctly isolated by the test set. Most failures to diagnose correctly were due to test program deficiencies rather than due to equipment malfunctions or limitations. Some were due to clerical errors, to incorrect test limits, and some were due to faulty test logic.

FUTURE IMPROVEMENT

One item which is expected to increase further the confidence in the performance of LCSS is a universal test equipment compiler (UTEC), which is presently under development. This software aid to program generation will accept test-oriented English-language inputs and produce an object program in ETG-3 machine language. The compiler would simplify coding, one of the sources of error, and provide additional checks of test design logic.

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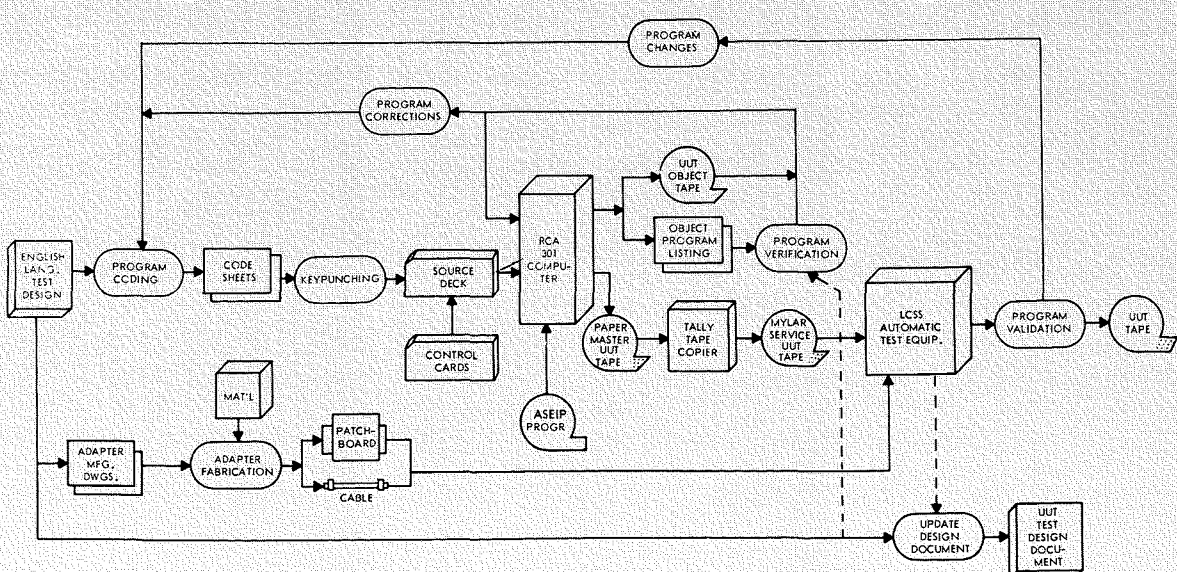

Fig. 3—Program production and validation process.

Evaluation criterion for automatic test equipment

R. F. Barry

This paper examines the probabilities of undetected defects and false alarms for automatic test equipment. The estimation of parameter values is reviewed and related to the acceptable limits for the parameter and the accuracy of the measuring instrument. A figure of merit is derived which should be useful in specifying the quality of test equipment. Two methods of testing control are also discussed: one based upon the figure of merit, and the other based upon a preset minimum acceptable level of confidence. The second method presents an attractive dynamic test situation which promises to meet any confidence levels which might be imposed.

THE testing qualities of automatic test equipment are usually defined by two probability statements. The first, the probability of undetected defects (PUD), refers to measurements which indicate that no faults exist in equipment which is, in fact, defective. The other, the probability of false alarms (PFA), refers to measurements which indicate the presence of faults which do not actually exist. The PUDs present a possibly dangerous situation in that equipment which is faulty may still pass inspection. The PFAs, on the other hand, may cause a very costly and unnecessary rejection of usable equipment. To make the PUD and PFA statements meaningful, it is necessary to specify allowable values for these errors.

It is the task of the test equipment manufacturer to relate these gross performance specifications to specifications for the individual measurements that comprise the test procedure. Since the gross specifications are couched in probabilistic language, these measurement specs also take the form of probabilities of detection and false alarms on an individual measurement level. These specs, in turn, must finally be transformed into specification of the measurement accuracy.

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These specifications proceed in a relatively straight-forward manner whenever the probability description of the measured parameter is known. It is more often the case, however, that the distribution of the parameter is completely unknown. Indeed, there is often evidence that the parameter is not a random variable at all, but some constant whose value depends upon conditions about which we have no information. In these cases, there is no formal path from the equipment performance specifications to a determination of the necessary measurement accuracy. The probabilistic description used in the equipment specs cannot be directly related to the measurement of non-probabilistic parameters.

Because the probabilistic manner of specifying performance does have strong intuitive meaning, it should be retained since everyone seems to agree upon what is intended. What is needed is some form of bridge between the gross specifications and the effects of measurement accuracy upon performance. The construction of one form of such a bridge rests upon an understanding of just what a parameter measurement is.

TESTING PHILOSOPHY

The purpose of a measurement, or group of measurements, on some parameter is to obtain enough information to make an estimate of the parameter's value. This estimator will, in general, be some statistical quantity, since the errors encountered in making the measurements are probabilistic. An unbiased estimator often encountered in parameter estimations is the sample mean, μ^*, and is defined as the arithmetic average of the group of measurements, x_i, (the sample) made on the parameter,

$$\mu^* = \frac{1}{N}\sum_{i=1}^{N} x_i$$

This estimator has the useful property that is accuracy increases as the number of measurements increases. The difference between the mean of an infinitely large sample and the true parameter value constitutes a permanent offset in the measuring equipment. Such offsets, known as bias errors, can be accounted for by calibrations and can therefore be considered zero without loss of generality.

The quality of a parameter estimation technique is determined by the confidence we have in the estimator. This concept has a precise mathematical definition:[1] the confidence, c, associated with a parameter estimation technique is the probability that an interval based upon the estimator value includes the true value of the parameter, u; that is to say, $c = P\,[\mu^* - \delta_1 \leq \mu \leq \mu^* + \delta_2 | \mu]$.

For the tests encountered in automatic test equipment, the interval will generally not be symmetric about the estimator value, μ^*. Indeed, the interval of interest is the acceptance interval specified for the parameter, and the estimator value quite often will not be within the interval, as is diagrammed in Fig. 1.

Fig. 1 points up nicely the central question: "Having determined the estimator value, μ^*, with what confidence can the interval $(S-\Delta, S+\Delta)$ be assumed to include the true parameter value, μ?" The integral equation

$$c = \frac{1}{\sqrt{2\pi^2}}\int_{-\infty}^{(\alpha+1)\sqrt{n}R} \exp(-\tfrac{1}{2}t^2)\,dt - \frac{1}{\sqrt{2\pi}}\int_{-\infty}^{(\alpha-1)\sqrt{n}R} \exp(-\tfrac{1}{2}t^2)\,dt$$

relating the confidence to the interval results for a normally distributed measurement error. The quantity, R, in this equation is the accuracy ratio of acceptance limit, Δ, to the standard deviation, σ, of the measuring equipment $R = \Delta/\sigma$.

The other important quantity is the size of the measurement sample, n.

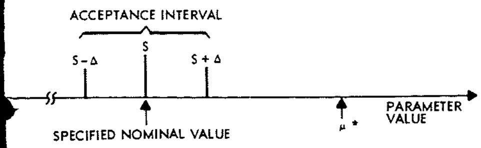

Fig. 1—Acceptance interval.

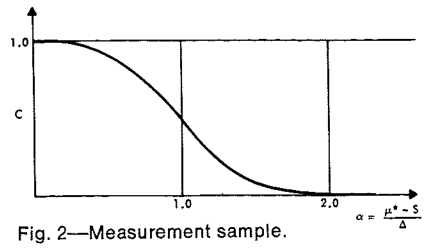

Fig. 2—Measurement sample.

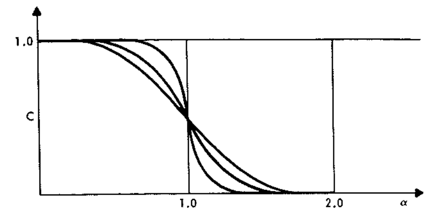

Fig. 3—Values of $\sqrt{n}\Delta/\pi$.

This expression is plotted in Fig. 2 for an effective accuracy ratio, $\sqrt{n}\Delta/\sigma$, equal to 3. In this graph, the value of the estimator is normalized with respect to the specific value, S, and the acceptance limits, Δ; $\mu^* = \alpha\,\Delta + S$.

The confidence associated with any estimator value for this test can be determined from this curve. It should be noted, however, that the curve essentially passes through $c = 0.5$ at the acceptance boundary, $\alpha = 1.0$. This quality is common to all tests, as may be seen in Fig. 3, where curves for several values of $\sqrt{n}\Delta/\sigma$ are plotted.

The general trend of the curves plotted in Fig. 3 is to yield an increasing confidence for μ within the interval for increasing $\sqrt{n}\Delta/\sigma$. Correspondingly, the confidence when μ is outside the interval is decreasing.

These confidences correspond to the probability of undetected defects (PUDs) and probability of false alarms (PFAs) in the following way. If the decision limit is taken equal to the acceptance limit ($\alpha = 1.0$), then for all estimator values having $\alpha \leq 1.0$, the interval will be assumed to include the true value at the confidence level shown. Estimator values outside the interval will correspond to rejections at the determined confidence level.

The confidence limit corresponds to a probability, since for large samples this acceptance criterion would yield correct values in $G \times 100\%$ of the cases.[2] Therefore, for an estimator value within the interval, the probability of an undetected defect is

$$\text{PUD} = 1 - G(\mu^*)$$

False alarm can occur whenever the estimator value is outside the interval, and its evaluation is

$$\text{PFA} = G(\mu^*)$$

FIGURE OF MERIT

In the foregoing analysis the PUDs and PFAs may be determined for any value of the estimator. However, in designing and/or specifying the testing equipment there is no apriori knowledge of the estimator value. For this application, all possible estimator values and their range must be considered. Since there seems to be no reason to assign a higher credibility to one estimator value than another, a posteriori, all estimator values will be considered equally. Said in another way, once a measurement has been made, there seems to be no reason to believe it less than some other measurement that has been made, so all estimator values have equal weight. This line of thinking leads to consideration of the areas associated with the individual PUDs and PFAs as being characteristic of the quality that can be expected of the equipment over a large number of estimator values.

It should be noted here, however, that the minimum confidence of acceptance associated with any set of estimator values has not changed. It is still equal to 0.5.

The expected values for the PUDs and PFAs associated with the equipment can be interpreted as normalizations of the areas above and below the confidence curve. These areas are shown in Fig. 4.

These areas correspond to

$$\text{PUD} = 1 - \frac{1}{A}\int_0^1 c\,d\alpha$$

$$\text{PFA} = \frac{1}{A}\int_1^\infty c\,d\alpha$$

where A is the normalizing factor

$$A = \int_0^\infty c\,d\alpha$$

Since this normalizing factor can be shown to be equal to 1.0, the PUDs and PFAs are equal. This condition leads to the specification of a figure of merit, F, for the test equipment which controls both PUD and PFA, viz.

$$F = \int_0^1 c\,d\alpha$$

This figure of merit corresponds to the area under the confidence curve within the acceptable limits. The larger this figure of merit, the better the testing

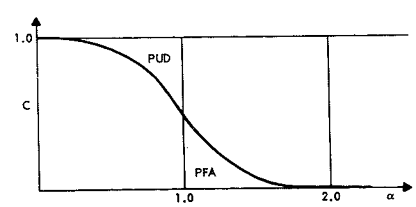

Fig. 4—Areas of PUDs and PFAs above and below the confidence curve.

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received the BSEE from Michigan State University in 1959. Participating in the RCA Graduate Study Program, he received the MS in Engineering from the University of Pennsylvania. Joining the Advanced Systems and Techniques Section of RCA, he was engaged in studying electro-magnetic wave propagation in non-homogeneous anisotropic media. Transferring to Applied Research in 1962, he conducted the statistical analysis and probability determination of an over-the-horizon-missile-detection system. He also conducted a study of the general orbit-to-orbit transfer of an earth satellite requiring a specific time of adaptation to the second orbit. During the past two years Mr. Barry has been engaged in computer-aided analysis of electronic circuits, and he was the responsible engineer for the technical analysis and development on the Test-Point Algorithm contract, directing in-house studies of fault isolation techniques. At present Mr. Barry is directing a study effort to extend the Wiener theory of nonlinear systems to the automatic testing of equipment by using white noise as an input signal. He is a member of Tau Beta Pi, Eta Kappa Nu, and the AAAS.

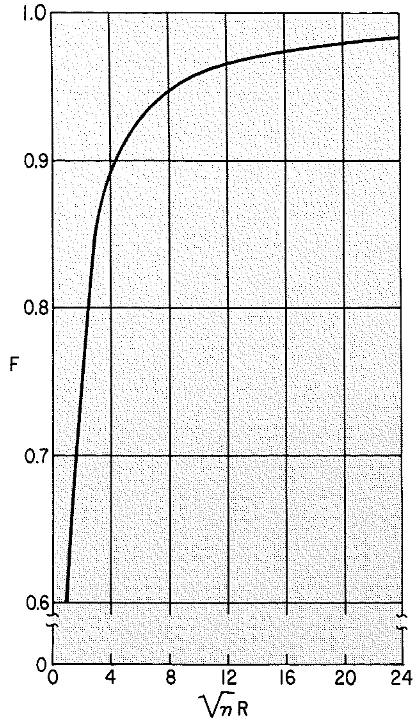

Fig. 5—Figure of merit, F, as a function of the effective accuracy ratio, $\sqrt{n}R$.

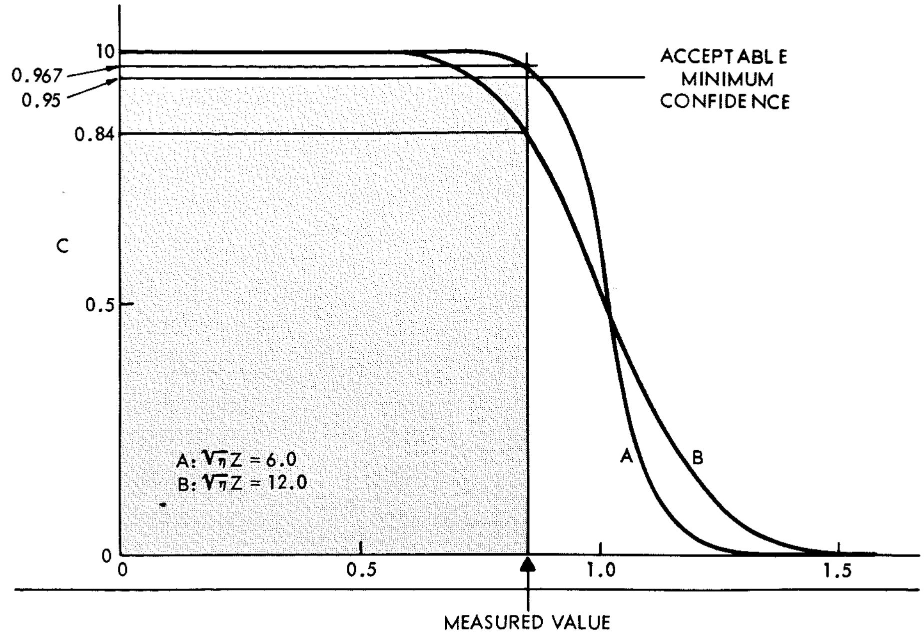

Fig. 6—Confidence curve of measured value equal to 49.75 VDC.

equipment can be expected to perform. This figure of merit is plotted versus the effective accuracy ratio, $\sqrt{n}\,R$, in Fig. 5.

The figure of merit, F, which has been derived applies to a single measurement. Since F corresponds to the individual PUDs and PFAs, the Fs for each measurement should combine in a fashion similar to the measurement PUDs and PFAS (which depends upon the dependence or independence of the measurements) to yield an overall system figure of merit. This system figure of merit can be adusted to meet the specifications by adjusting the individual Fs for the measurements. Obviously, a minimum F for all measurements is the easiest approach.

These considerations are easily implemented in the test program. Whenever the test designer encounters a test which has an accuracy ratio insufficient to yield the minimum F, the test can be repeated until the effective accuracy ratio is sufficient. It should be noted, however, that this is not as efficient as increasing the accuracy of the measuring instrument—it takes 100 repeated measurements to increase the effective accuracy ratio by a factor of 10.

TESTING CONTROL

The foregoing considerations provide a consistent bridge between the intuitively meaningful test specifications and the accuracy requirements necessary to meet them. In addition, they lend themselves to easily implemented controls on the testing process. Two forms of control are immediately apparent, namely

1) Control based upon the average quality of a large number of estimator values—the figure of merit
2) Control based upon a single, or observed, estimator value—a minimum confidence criterion.

In the first type of control, figure of merit, the testing programs would be so written that each tested parameter would correspond to a minimum figure of merit. Since the figure of merit depends upon the *effective* accuracy ratio, $\sqrt{n}\Delta/\sigma$, iterated measurements can be programmed to increase n whenever necessary.

In the second type of testing control, a minimum acceptable confidence is set into the program. Reference to Fig. 3 will show that this determines an acceptance bound (s)—different from 1.0—for any given $\sqrt{n}\Delta/\sigma$. The complementary requirements of a minimum confidence for values outside the intervals lead to two decision bounds and an area between them. Whenever the estimator value falls between these bounds, no decision can be made. However, an additional measurement can be made and a new estimator calculated. Since the two bounds approach each other for an increasing number of measurements, an estimator value will eventually fall outside the interval and a decision made—above the minimum confidence.

EXAMPLE

Suppose that a parameter value is specified as 50 ± 0.3 VDC. This quantity would be measured on the 100-volt scale of a meter which may have an accuracy (one sigma limit) of ±50 MVDC. A single measurement will have an effective accuracy ratio of 6.0. A measured value equal to 49.75 VDC will yield a confidence equal to 0.84, as shown in Fig. 6. This value will be unacceptable if the minimum confidence has been established at 0.95. However, if the mean value of four repeated measurements has the same value, it would correspond to an effective accuracy ratio of 12.0, yielding a confidence value of 0.967, above the established minimum confidence level. This second method of testing control has some very appealing features, but further investigation will be required to determine the expectation and variance of the number of repeated measurements when an estimator falls into the no decision region.

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Floating electronic maintenance facility

J. E. Lidiak

This paper describes the floating electronic maintenance facility currently being studied by the Aerospace Systems Division for the U.S. Army Materiel Command. This facility could provide efficient mobile depot-level support to land-based troops engaged in limited warfare. The proposed facility is described in general and compared as to cost effectiveness and turn-around time with land-based facilities. Also described are the proposed applications of automatic test equipment in such a facility.

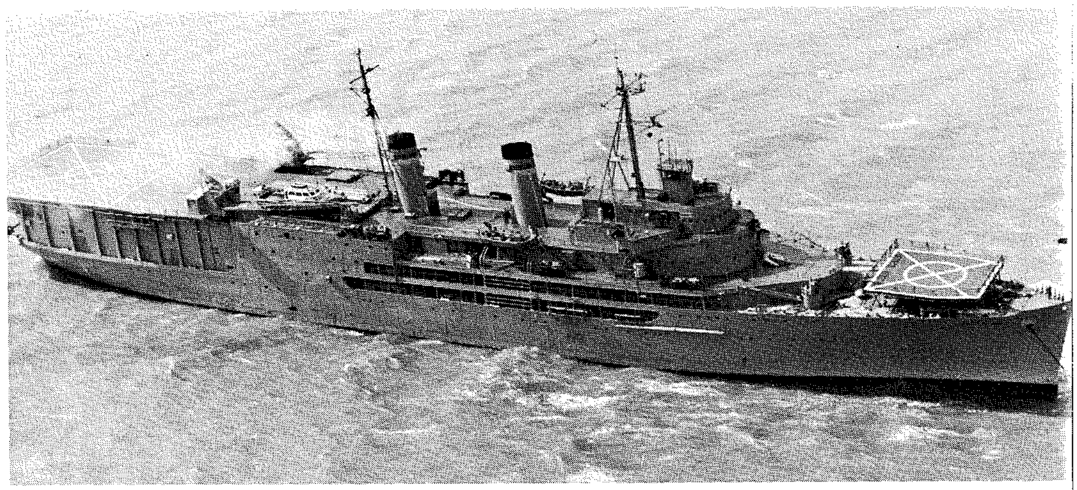

Fig. 1—FAMF III, USNS Corpus Christi Bay.

To be effective, U.S. Army materiel maintenance must operate closely with the supported elements. This requirement has been met with the mobile support units deployed with the field army and backed up by maintenance depots. In the past, this depot-level support has been limited to fixed facilities both in the U.S. and abroad. In the limited wars of the last few years, these fixed depot facilities have been remote from the scene of operations resulting in high support costs, due to 1) the large inventory of materiel necessary to fill the long supply pipelines and 2) the shipping costs necessary to move this material to and from the fixed depot maintenance facilities.

The use of a floating maintenance facility to provide support for forces ashore is as old as ancient galleys. Through the ages, the need to be self-sustaining for increasingly longer voyages and the evolution of greater degrees of sophistication in naval ship systems resulted in shipboard maintenance facilities comparable to all but the most elaborate shore bases. In addition, as the largest vehicles designed by man, ships have mobility as well as space and utilities to accommodate large-scale operations. The successful operation of naval maintenance tenders during World War II was sufficient cause for the U.S. Army Air Forces to use several maintenance ships in the Southwest Pacific.

In 1962, the concept of a floating maintenance facility for support of the overseas Army was developed by the US Army Materiel Command. The requirement was approved for an aircraft maintenance facility in March 1964. This first Floating Army Maintenance Facility (FAMF), operating in Southeast Asia since April 1966, has been designated FAMF I. This ship, the USNS Corpus Christi Bay (Fig. 1), has fulfilled the expectations of the basic concept in repair, return to supply, and overhaul of selected materiel in support of Army aircraft.

In 1966, the US Army Materiel Command directed the investigation of feasibility of applying the FAMF concept to Army materiel other than aircraft. After preliminary work by the Army Electronics Command, RCA was placed under contract to undertake study of FAMF-III-(E—electronic) feasibility for the support of electronic materiel from a hypothetical typical corps.

The objective of the FAMF concept is to provide a mobile shipboard depot maintenance capability that will be deployed in the theater of operations. This shipboard facility will provide three major improvements in depot support:

1) Reduction of supply pipeline inventory and shipping costs by intercepting

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received the BEEE from Johns Hopkins University in 1950. Spending ten years as a design engineer, he was responsible for the design of major portions of the AN/PRC-25, a transistorized portable transceiver, and its solid-state circuitry test set. Since 1963 Mr. Lidiak has had supervisory responsibilities in product assurance, project engineering, system test requirement analysis, and maintenance concepts in the ATE systems activity. His primary participation has been in MTE (Multisystem Test Equipment), LCSS (Land Combat Support System, FAMF (Floating Army Maintenance Facility), and advanced systems for Naval Air Systems Command. Prior to his present assignment, Mr. Lidiak was engaged in analytical engineering, technique development, and project operations for two major space system programs (Satellite Inspector Program and Dyna Soar) and Communications and Data Link, as well as various smaller projects.

materiel normally flowing back to fixed depot installations;
2) Reduction of response time through rapid repair and return of repairable items.
3) Reduction of deployment and redeployment time by readiness for operation immediately upon arrival.

The functions to be performed are:

1) Inspect, test, repair, and overhaul U.S. Army equipment.
2) Fabricate maintenance support and mission items.
3) Repair and calibrate maintenance equipment for supported units.
4) Maintain a complete stock of repair parts and supplies to support the mission.
5) Provide special technical data and related materiel to supported units.
6) Provide technical assistance to supported units in areas of component and materiel failure investigations.
7) Provide necessary administrative and support services for Army personnel aboard the ship.
8) As space permits, stock maintenance float of high density and priority items to speed maintenance response.

The FAMF acts in the direct or general support role for limited periods, being relieved when, and if, adequate land-based facilities are established ashore. Equipment and manpower are provided to conduct depot maintenance. The functions of inspection, testing, adjustment, calibration, repair, overhaul, and salvage are accomplished. Depot operations are focused on an inspect, repair, and overhaul role in lieu of the scheduled-overhaul-by-lot function performed by fixed depots.

BASIC APPROACH

The basic approach in the study was first to determine the magnitude and technical requirement for materiel in a typical corps. Secondly, a shipboard maintenance facility was configured to meet the support requirements. Internal trade-offs were made in selection of the ship, maintenance equipment, shop layouts, and the number and types of personnel. Next, computer-aided mathematical modeling was used to perform cost effectiveness comparisons between the FAMF III and alternate methods of satisfying the support requirement. Finally, implementation planning was prepared for the ship configuration determined to be most effective and achievable by the FAMF E on-site operational date.

TECHNICAL REQUIREMENTS FOR A TYPICAL CORPS

The typical corps contains 66,000 individual items of electronic equipment of 750 types—all imposing maintenance support requirements at direct, general, and depot levels. Equipment types include ground and airborne radar, avionics, field radio, teletype, wire communications, crypto, photo and electro-optics, plus instrument and test equipment repair in support of lower echelons. In addition, portions of the NIKE, HAWK, and SERGEANT missile systems contribute to the total support requirements. Future systems such as PRC-77 and PRC-62 and LOH avionics will have little effect on the size and technical characteristics of the workload while the AH-56A avionics, ADSAF, and MALLARD will significantly increase the workload that is now anticipated for the typical corps.

The FAMF III mission is to provide depot maintenance at depot levels of support in a variety of high, medium, and low intensity conflicts, and peacetime possibilities. Key to systems design of the FAMF III facility is the achievement of a balance between workload flexibility, production efficiency, and the inherent constraints of shipboard environment. In planning work flow, identification of production and support shops, and the selection of individual equipment, the experience of Army depots at Tobyhanna, Sacramento, and Lexington was used to advantage. The FAMF III contains production shops, assigned for test, inspection, and repair of similar electronic items within the individual shop.

In support of the production shops, the FAMF III has support shops configured for basic materials rework and fabrication. The shop complement is shown in Table I.

The FAMF III concept included the use of a self-propelled vessel based on the successful operation of FAMF I. However, various other hull types were considered during the study and evaluated with the AMC Special Project Office.
with the AMC Special Project Office. Towed vessels were discarded for their inability to deploy rapidly and the mobility restrictions imposed by problems of availability and scheduling of ocean-going tugs. Landing vessels such as LSTs were considered grossly undersize. The time and cost of converting ore boats was deemed excessive. Escort carriers were ideal candidates but were not available. Building of a completely new ship was unacceptable due to excessive procurement lead times and additional cost.

Facility Configuration

Using a C-3 hull as a model, the study proceeded to a layout of shop, administrative, and living areas aboard ship. Maximum separation was obtained between the maintenance and living areas

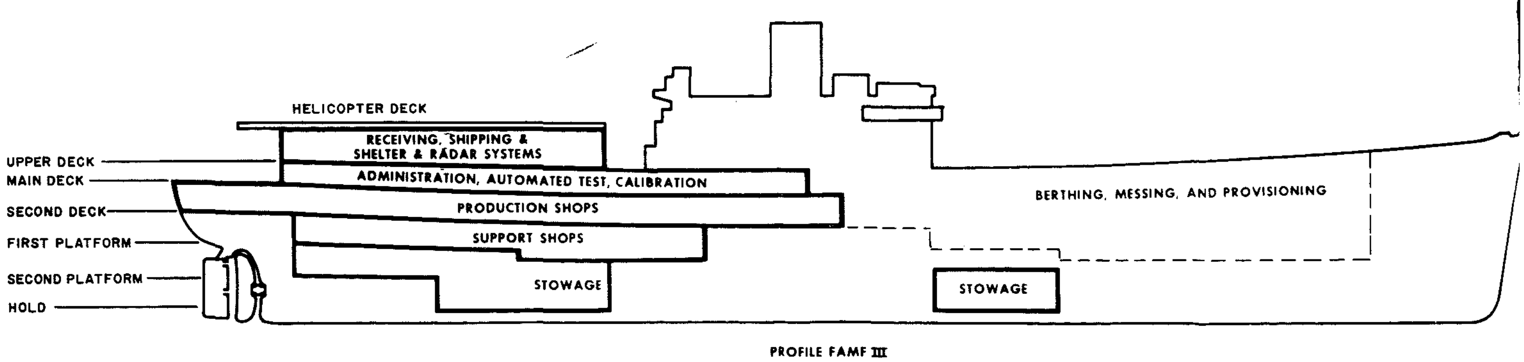

Fig. 2—FAMF III ship profile.

(Fig. 2). All maintenance areas are positioned aft of the main engineering spaces. The maintenance facility is workflow oriented with gross functions assigned to specific deck levels. Repairable equipment receipt and dispatch is concentrated at the heli-pad for air transportation and under forward portions of the pad for boat transportation. Receiving, areas for shelter work, and storage of CONEX boxes are located on the upper deck directly below the heli-pad. The main deck houses major administrative offices, a DIMATE automatic test system, and calibration labs. Production shops are on the second deck, support shops on the first platform. Storage areas are relegated to lower portions of the ship but situated for vertical flow to the appropriate shops.

The total of Army and MSTS personnel needed aboard ship is 500 and living facilities were configured from established requirements and FAMF I experience. Living service areas include barber, cobbler, tailor, and laundry.

MAINTENANCE FACILITIES

Three Army Depots which handle the bulk of the electronic depot maintenance in the Continental United States (CONUS) were extensively examined on a first-hand basis during the FAMF III feasibility study. The purpose of these visits was to observe operating procedure, methods of handling equipment, controlling work, and to sample the nature of the workload handled. Each depot (i.e., Tobyhanna, Lexington, and Sacramento) has its own characteristic mode of operation. Rather than adopt the operational mode of one depot, the portions most applicable to the FAMF III mission were selected. The final complement of shops appears in Table I which also shows deck locations identifiable on the ship profile.

One of the most important cost effectiveness parameters is the realization of maximized work flow. Two ATE options were proposed toward that goal by implementation of automatic testing aboard FAMF III. The first is to be installed on the ship in time to meet the required on-station schedule date 19 months from go-ahead. The second is a recommended option configuration to be added to the ship at drydock in 27 months.

AUTOMATIC TEST EQUIPMENT FACILITY

From the analysis of the test, inspect, and repair times for the various systems to be maintained, it became apparent that the flow rates for any particular set could be greatly increased if the test and inspect functions could be automated. The DIMATEs and DEE at the depots are presently performing this function with typical test time reductions as shown in Table II. Based on this data, inspection test time reductions available by use of DIMATE aboard the FAMF III are shown in Table III.

On the list of items to be supported there are 60 equipments, comprising 7270 items, that can be tested on DIMATE. The average inspection test time reduction is 3.15 hrs/equipment, so that use of DIMATE would reduce the man-hour requirements by 21,900 man-hours per year on these items. Of these 61 equipments, many are not recommended for testing on DIMATE. The criterion used for selection was that if a test program is prepared for an item, the program must pay for itself in reduction of labor over a three-year period. To accomplish this, use of the program must reduce the labor by approximately 500 man-hours/year. In addition to the above whole equipments, there are many components of radar sets, communication centrals, flight control systems, test equipments, and missile systems that also could be tested on the DIMATE if test programs were available. As test programs are prepared for use at the CONUS depots, they will be added to the FAMF III program library.

Based on all of these considerations, but especially the increased productivity, an ATE facility was established on the starboard side of the main deck. The shop is large enough (1100 ft^2) to accommodate two DIMATE systems with adequate work space for each. However, only one would be installed in the initial installation. A calculation of workload for those items for which test programs exist, or will become available within a twelve-month period, indicates that one DIMATE operating on two shifts with a 90% availability could accommodate the workload. As new programs and new equipments become available (especially programs that isolate to a module) the workload will exceed the

Table I—Shop Complement List.

Type	Location (deck)
Production shops	
Field radio shop	Second
Automatic test facility (DIMATE)	Main
Wire communications shop	Second
Wire communications	Second
Radio delay	Second
Cryptographic and teletype	Second
Shelter repair area	Main
Avionics shop	Second
Radio shop	Second
Ground radar area	Upper
Missile and weapons shop	Second
Electro-optics shop	Second
Photographic equipment area	Second
Electronic instrument shop	Second
Calibration area	Main
Nucleonics area	Main
Support shops	
Machine shop	Second
Sheetmetal and metal shop	Second
Welding, heat treatment shop	Second
Plating shop	Second
Paint and stencil shop	Second
Textile and leather section	Second
Woodworking shop	Second
Plastics and chemical potting shop	Second
Tool crib and tool calibration room	Second
Battery shop	Main
Receiving and shipping area	Upper

Table II—Typical Test Time Reductions.

Equipment	Inspection test times (min.) Manual	Automatic
Receiver-transmitter RT-246/VRC	60	9
Receiver-transmitter RT-524/VRC	75	20
Receiver R-442/VRC	60	8
Receiver R-108/GR	75	20
Receiver R-390	420	60
Receiver-transmitter RT-505/PRC-25	65	8
Receiver-transmitter RT-66, 67, 68	210	30

Table III—Available Inspection Test Time.

Equipment	Inspection test time (hrs) Manual	Automatic	Quantity tested	Savings manhour/yr
AN/PRC-25	1.1	0.133	1191	1152
AN/VRC-12 Series	3.25	0.616	2439	6424
R-390	7.0	1.0	16	96
RT-66, 67, 68	3.5	0.5	58	174

capacity of a single DIMATE. A second unit (or even more) could then be installed at a later date to include the microwave stimulus and measurement capability, plus additional coverage in the telephone switching, PCM, digital computer, and tropospheric scatter equipments.

SHIP FACILITIES

To make maximum efficient use of space onboard a ship, a more detailed consideration of layout is necessary than is required for that of a land-based facility. One consideration is the necessity of vertical travel to make maximum use of available space due to the limited horizontal expansion. Although not as efficient as horizontal movement, vertical movement is also required by the limited accessibility between holds, especially for levels at and below the waterline, and because of the major impediment of the machinery casing.

Two more factors are a ship's trim and stability. This is one reason that the machine shop, for example, with its heavier equipment, is located as close amidships as possible and in a lower deck level. Some installation compromises cannot be avoided; e.g., the helicopter flight deck high above the ship's CG. However, the heaviest items, bulk storage and the support shops, are at the lowest ship's levels.

Further constraints are introduced by the need for a ship to be an independent entity, which includes messing and berthing requirements for the operating force, plus a crew necessary to support them. These considerations are generally not as important a concern in planning land-based facility installations. The autonomous nature of the ship also requires greater care in planning supply, storage space, and storage access and flow of material.

Since the ship is to be air conditioned, the interior environment is similar to a land-based facility. However, the roll and pitch of a ship does require a permanent dogging down of capital equipment, repair items and stored items. Rough weather also limits work effort and creates such problems as sloshing in the plating tanks, or hindering close-tolerance calibration checking on the equipment.

PHYSICAL WORKFLOW DESIGN

The FAMF III is workflow oriented. The ship's profile (Fig. 2) shows the stratification of gross maintenance functions to specific deck levels to accommodate the equipments in accordance with a progressive natural workflow. Receipt and dispatch of materiel is concentrated at the helicopter pad for air transportation and under forward portions of the pad for boat transportation. Located on the upper deck directly below the pad is receiving, basic cleaning, areas for shelter systems, large radars, bulky cables, and storage of CONEX boxes, and preservation and packing. The rationale was that repaired equipments should be returned to field supply as rapidly as possible and not kept in storage in the holds of the ship. Accordingly, many of the incoming containers, boxes, packing material, etc., can be reused almost immediately to crate or box the repaired equipment, thereby cutting down on the stocks the ship must carry and partially eliminating a crate storage or disposal problem.

The main deck houses the major administrative offices, the DIMATE system, calibration laboratories, and a computer. The bulk of the production shops are located on the second deck. Production shops are generally configured for two-shift operation, and require the most support with respect to documentation, parts, and equipment flow. This location is one deck below the administrative areas. Being above the watertight deck, (2nd deck) emergency access can be freely provided fore and aft from shop-to-shop (through watertight doors).

The interface between ship and shore will be provided with helicopters and boats. Two UH-IH helicopters were proposed, but the shipboard heli-pad must

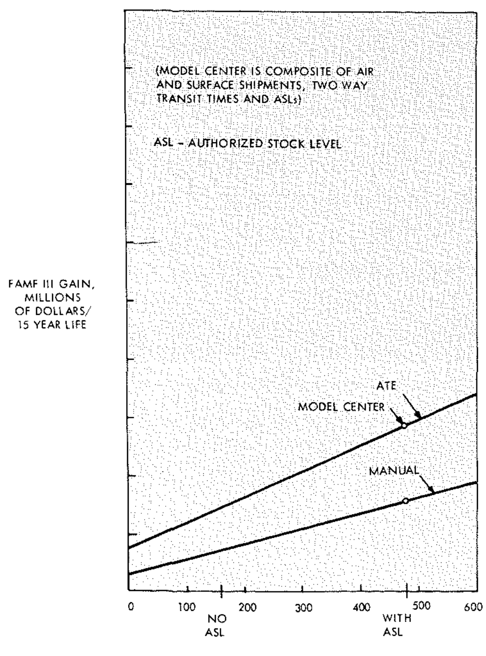

Fig. 3—FAMF III, gain versus pipe length.

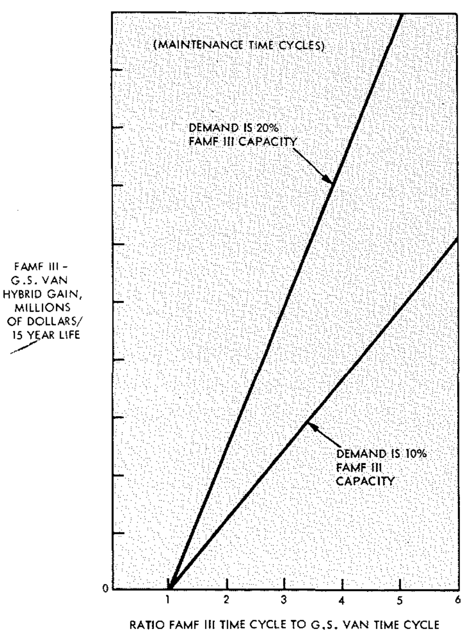

Fig. 4—FAMF III hybrid gain versus FAMF III ATE-to-general support-van time-cycle ratio.

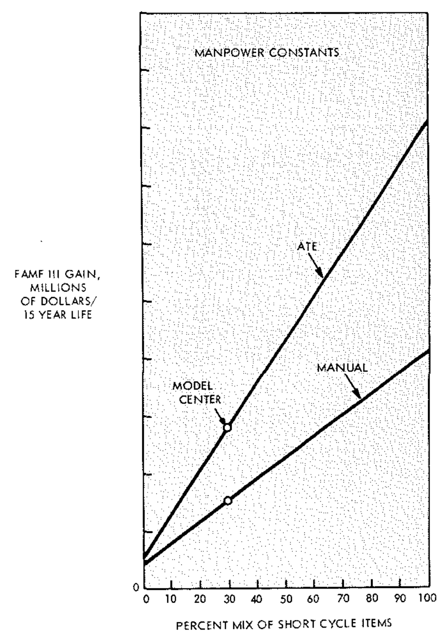

Fig. 5—FAMF III gain versus volume productivity.

be configured and designed to accommodate a CH-54 helicopter. The boats selected were one 40-ft personnel boat, one 40-ft utility boat, and two LCM-6's.

COST EFFECTIVENESS

Cost effectiveness comparisons, conducted by the SEER activity in the Moorestown, N.J. plant, were made between FAMF III and other methods of accomplishing an equivalent support capability. By varying key input values to the mathematical model, the study was also able to examine the sensitivity of the FAMF III concept to such parameters as workload, man-hours worked, and implementation cost. The FAMF III has a clear-cut cost effectiveness advantage over: 1) support by a CONUS depot, 2) support by an overseas land-based depot as reflected in the retention of gain over a variation in supply pipe length shown in Fig. 3, and 3) overseas general support vans and shelters for items which can be more rapidly cycled by the superior FAMF facilities The dollar advantages versus time-cycle ratios are shown in Fig. 4. Further, FAMF III continues to be self-liquidating and shows cost savings even though:

1) The workload is entirely long term maintenance as opposed to short cycle items (Fig. 5).
2) The work demand for the type corps is substantially less than that postulated (Fig. 6).
3) The investment and annual premium cost for FAMF III is substantially more than currently estimated (Fig. 7).

The most effective FAMF III is one which is able to achieve the greatest productivity per man in the maintenance crew. Because of this fact, FAMF III savings are most sensitive to workload characteristics as regards repair and overhaul. If short cycle items which may be repaired and quickly returned to supply are selected, the productivity and the resultant gain are highest. Two FAMF III configurations were used in cost effectiveness comparisons with alternative support concepts: 1) a completely manual facility and 2) a facility wherein test of high work load electronic items was automated. Compared to support provided by CONUS depot and assuming a nominal 30% repair and return workload, the manual FAMF III shows a 15 year savings of over $100 million plus another $100 million for the ATE-equipped FAMF III.

Aside from cost advantage to the FAMF III concept, the primary virtue of the FAMF concept is its instant readiness and redeployment features. At the onset of a new conflict, only the FAMF can be on the scene and working as rapidly as the combat forces themselves. Even direct and general support units cannot be marshalled, onloaded, offloaded, and set up as quickly as the FAMF.

CONCLUSIONS

The floating electronic maintenance facility, FAMF III (electronic), is physically feasible and cost effective. If a short implementation cycle is desired by the Army, a suitable mothballed hull, such as several in maritime reserves, circumvents the limiting lead time of new construction. The savings to the Army attributable to FAMF III, which are most likely to result in more effective operations than in a reduction in materiel procurement budgets, are in hundreds of millions of dollars over a projected fifteen year useful life.

Due to the cost advantages of maximizing work capacity, FAMF III should be designed to handle as much work as its hull can hold; i.e., use automatic testing wherever possible and man up to the limits of reasonable living conditions. The flexibility and capacity of FAMF III should be employed not only to support field based maintenance but also for any maintenance where the overall maintenance time cycle can be reduced.

No alternate concept has the ability to redeploy rapidly, accomplish work enroute, and arrive at the scene of conflict as ready to operate as the combat forces themselves.

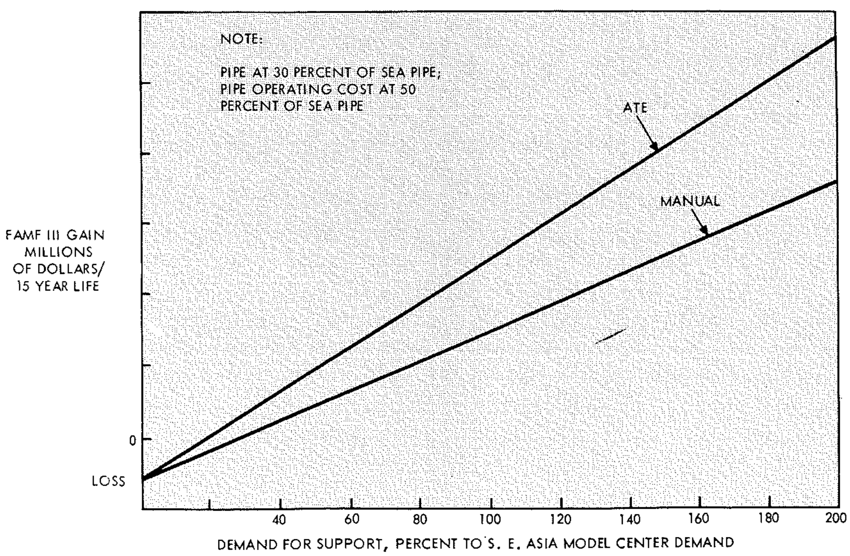

Fig. 6—FAMF III gain in global situations versus demand for support.

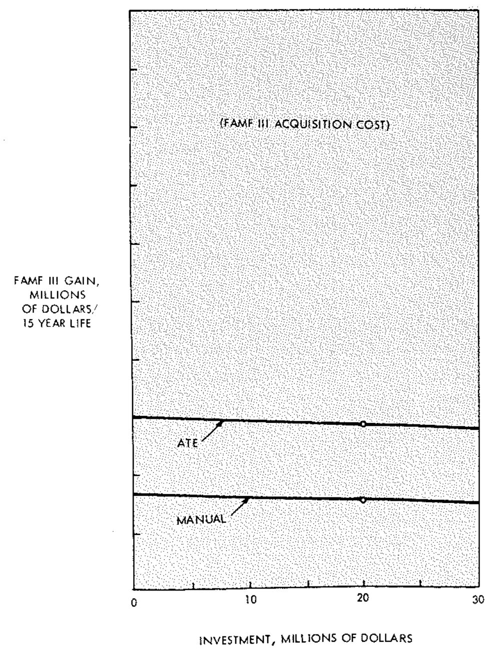

Fig. 7—FAMF III gain versus investment.

Table-driven compiler for automatic test equipment

R. L. Mattison
R. T. Mitchell

This paper introduces a compiler-compiler which has been built for use with Automatic Test Equipment (ATE) type languages. It allows the syntax and semantics of new languages, as well as target languages, to be defined by a meta-language program. This meta-language and the implementation of the compiler are discussed.

WHEN GENERATING compilers for use with automatic test equipment (ATE), a substantial need arises for flexibility in both the source and object languages. Flexibility is desirable for two reasons: 1) the field of ATE construction is rapidly expanding,[1] and 2) the hardware and support software design, development, and debug cycles are often simultaneous.

To facilitate compiler implementation and growth, a table-driven system, the Universal Test Equipment Compiler (UTEC), has been developed. As in other table-driven systems,[2] the function of defining a source language has been disassociated from the actual translation mechanism. The source language is specified to the generator which creates a set of tables for subsequent use by the translator. A dual-purpose meta-language has been created for use in the system. This language is used to specify the syntax of a particular source language and the meaning to be imparted to the various allowable constructs of that language. A typical ATE system consists of various programmable devices for applying stimuli to, and obtaining measurements from, the unit under test (UUT).[1,3]

A requirement peculiar to ATE compilers is the creation of a wire list specifying connections between the ATE and the UUT. An equipment designator has been included in the system to handle the wire list and to insure that the wire list remains fixed despite source program recompilations. This is necessary due to the cost incurred in the production of this wiring.

The wide range of computers currently used in ATE dictates that the output of UTEC be a symbolically addressed code which must then proceed through the second pass of a normal two-pass assembler. Since this reduced assembler could be different for each type of ATE, it is not discussed in this paper.

The flow of information through the UTEC system is depicted in Fig. 1. The source language specifications and translation logic are defined to UTEC using the meta-language and are fed into the generator. From this, the generator produces translation tables for use by the translator. The generator also accepts the ATE hardware configuration and produces equipment tables for the equipment designator. When a source program is fed to UTEC for translation, the translator uses the translation tables and produces an intermediate code ready for assembly. Whenever ATE equipment must be specified by the translator, it inserts a symbolic address into the intermediate code, and requests the required equipment from an available equipment pool in the equipment tables. The request is tied to the intermediate code by the symbolic address. The equipment designator now processes the equipment requests and, using the equipment tables, produces equipment assignments for each symbolic address in the form of a symbol table.

THE META-LANGUAGE

We now present a language, SYNSEM, (syntax and semantics) for explicitly defining a problem-oriented language (POL).[4] SYNSEM itself is a two-fold problem-oriented language which 1) specifies the syntax of the POLs and 2) specifies the semantics of the allowable constructs in a POL. SYNSEM is therefore divided into two sublanguages: SYN for specifying syntax, and SEM for specifying semantics.

Problem-oriented languages currently in use with ATE are tabular in format. The reason for this and examples of such languages have been previously presented,[5,7] and, therefore, will not be considered here. Let it suffice to say that fixed fields are generally adhered to, with one field set aside for the function or verb and the remaining fields for modifiers of various types. Each verb-modifier complex is referred to as a source statement.

The goal of SYN is to allow format-syntax type information to be specified for each verb of the POL. This information is encoded into a table by the generator and will be used by the translator whenever the verb is used in a source program.

SYN is comprised of various disjoint subsets of any commonly used charac-

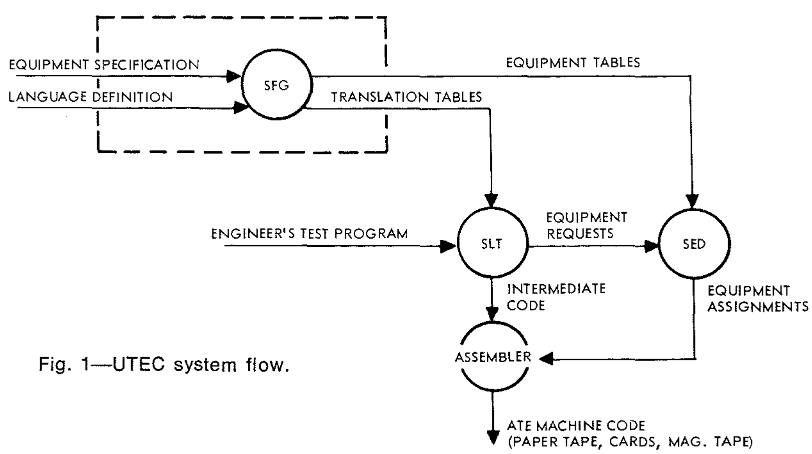

Fig. 1—UTEC system flow.

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ter set. Three of the subsets are given below:

NUMBERS = { A, B, C, D, E, F, G, H, I, M, N, O }
LETTERS = { P, Q, R, U, V, W, Y }
MAIN UNITS = { K }

To specify a numeric modifier, a letter is chosen from NUMBERS and repeated so that the number of times the letter appears equals the maximum number of digits the modifier may contain. Alphabetic modifiers are handled in a similar way by choosing from LETTERS.

If desired, a MAIN UNITS modifier may be used with any verb. When the letter K is recognized by the generator, the four characters immediately following the K are taken as the MAIN UNITS and entered into a dictionary with the verb. The MAIN UNITS are used to further distinguish the verb when more than one source statement uses the same verb. As an example, consider the following SYN statement to specify the verb CONNECT with the modifier VDC: CONNECT AAA KVDC BBB PPPP. The modifiers may be two numeric (A and B), one alphabetic (P), and the MAIN UNITS for this form of CONNECT is VDC.

Once SYN has been used to specify a given verb, a SEM program is written, later to be executed by the translator, which analyzes the verb-modifier relationship and generates the desired intermediate code for the source statement. The SEM language is composed of a number of semantic instructions, some of which are described below. A maximum of 750 such instructions can be used in any one SEM program. A statement in SEM consists of a semantic instruction followed by its possible modifiers. A 3-digit label is optional for all statements. A 3-digit branch is required with some instructions and optional with others. If a branch is given on optional instructions, it is considered unconditional. The SEM instructions are divided into three categories: 1) code producing, 2) modifier handling, and 3) control. CODE, CVAR, CALPHA, and CSIGN are four of the code-generating instructions. CODE tells the translator to output the characters which are literally specified with the CODE instruction: CODE 3 PS1 will cause the three characters PS1 to appear in the intermediate code. CVAR, CSIGN, and CALPHA each are used with an identifier which the translator references to find the data to be output. The

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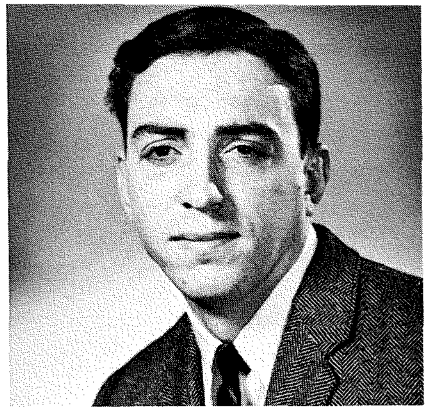
received the BA in Mathematics from Wabash College in 1964. While at Wabash, he developed a routine for matrix inversion to be used on an IBM 1620 computer. In 1966 he received the MS from Purdue University, dividing his time between numerical analysis, utility systems, and languages. Mr. Mitchell developed a program to compare the Gauss, Givens and Householders methods for the inversion of matrices associated with Legendre polynomials. He programmed a solution to the Blassius boundary value problem using fourth order Runge-Kutta, and wrote a program to compare the Liebman and the Peachman-Rachford methods used for partial differential equations. Mr. Mitchell has also written an algebraic translator in SNOBOL, and has programmed using FORTRAN IV, MAP, ALGOL, SNOBOL, SLIP, LISP, and IPL V. Since joining RCA in 1966, he has helped in the design of the Universal Test Equipment Compiler.



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received the BS in Physics from the Georgia Institute of Technology in 1965 and is now taking courses toward the MS at Northeastern University. Joining RCA in 1965, Mr. Mattison worked in the scientific programming group of ASD, developing programs for special purpose matrix inversions and solutions. He was subsequently assigned to a project developing electronic circuit analysis programs for fault isolation. He developed a program to divide a large circuit into smaller stages, each of which could be analyzed separately. He also developed a sorting program to present the output from this program in a manner which would make fault isolation a relatively simple matter. Next he designed a Syntax Directed Computer oriented toward the special languages used in writing programs for Automatic Test Equipment. He developed the way in which the compiler would operate by table structures and accept the syntax of languages it is to translate. He worked in all aspects of completing the detailed design of the computer program. Mr. Mattison is a member of ACM.

identifiers with CVAR and CSIGN must be numeric: CSIGN NUM1 will generate a + or a − depending on the sign of NUM1. CVAR NUM1 4 2 will cause the value of NUM1 to be coded using four characters total with two implied decimal places. If NUM1 = 46.913, the characters 4691 will be coded. CALPHA W1 3 will cause the three left most characters of W1 to be coded.

Some of the modifier-handling SEM instructions are TEST, RANGE, and the 4 arithmetic operators ADD, SUB, MUL, and DIV. TEST causes the translator to compare a referenced quantity with a group of characters specified following the instruction. RANGE causes a check of a referenced quantity to see if it is numerically between two limits. Execution of either a TEST or RANGE instruction by the translator can cause a branch in program flow to a labeled SEM statement if the comparison fails. TEST A 3 AMP 40 causes a comparison of the three left-most characters of *A* with the three characters AMP. RANGE B 20.0 30.0 40 causes a comparison of *B* to see if $20.0 \leq B \leq 30.0$. If the above comparisons are satisfied, the translator executes the next sequential instruction; otherwise, statement 40 will be processed next.

Some of the SEM control instructions are JUMP, SCWL, ROUTINE and EQUI. JUMP is used with a SEM statement label and causes an unconditional transfer by the translator to the labeled statement. SCWL informs the translator that all of the intermediate code generated for a particular source statement must be saved with a label for future use.

The SEM language is provided with a subroutine capability through the ROUTINE instruction. ROUTINE may be followed by a parameter list of from 1 to 7 dummy parameters. The CALL instruction, followed by the actual parameters, is used to invoke a SEM subroutine. The EQUI instruction is used to cause the translator to generate a symbolic equipment request for the equipment designator. Its modifiers must be a unique symbolic, which will be placed in the intermediate code by the ECODE instruction, a type number referencing a particular pool of equipment, and a set of "connections" to which a specific piece of equipment from that pool should be wired. A control card called REQUIRED is used between the two parts of the SYNSEM language and lists all required modifiers in the SYN portion.

The following example shows the combined use of the SYN and SEM languages to specify the verb CONNECT modified by VDC.

```
    CONNECT   AAAA  KVDC  JC    JD
    REQUIRED  AC
    NEWN      UN1
    CODE      1     S
    RANGE     A     0     50          10
    EQUI      5     UN1   C     D
    ECODE     UN1
    CVAR      A     4     2           20
10  RANGE     A     51    120         30
    EQUI      6     UN1   C     D
    ECODE     UN1
    CVAR      A     5     2
20  CODE      2     ES                40
30  ERROR     A     OUT OF RANGE
40  END
```

The above program is suitable for input to the generator which would create the necessary table entries for later use by the translator after it sees the CONNECT VDC verb in a source program.

In a compiler for use with ATE, there is another function of the meta-language, other than defining source statement syntax and semantics. It is to specify equipment available in any ATE configuration. This is done in UTEC by the two instructions, SYMBOL and DATA.

All equipment is divided into types—i.e., power supplies, signal generators, voltmeters, etc.—and each type is given a number to identify it. One SYMBOL instruction and as many DATA instructions as there are pieces of equipment in a type are used to define that type. The SYMBOL instruction tells how many pieces of equipment in the type, how many connection terminals each has, and the total table area required to store requests for this type. Each DATA instruction gives an equipment name and the ATE connection terminals for it.

When a new problem-oriented language (POL) or a modification to an existing POL is defined to UTEC by means of SYNSEM, the syntax of the language and its semantics are stored into tables by the generator. Since ease of language modification is a requirement, three tables have been implemented as linked lists.[6] The format list is used to hold the syntax specification for each verb in the language. The logic list is used to hold one entry for each SEM instruction specified in a verb definition. The logic modifier list holds SEM instruction modifiers which are not suitable for entry in the logic list. A dictionary is also used which contains the name of each function defined by SYNSEM as well as various pointers to the lists. Since UTEC is designed to handle POLs for automatic test equipment, it automatically controls the assignment of equipment and produces wire lists. A pair of equipment tables, the hardware-name table and hardware-usage table, are built by the generator to aid in these tasks.

THE GENERATOR

The generator division of UTEC accepts the definitions of verb syntax and semantics written in the SYNSEM language, and assembles this information into all the necessary tables and lists. It also has the ability to delete and equate verbs in the lists, and to build the equipment tables. The generator is used whenever a DEFINE, EQUATE, DELETE, or EQUIPMENT control card is encountered and is divided into four corresponding sections.

Define

Following the DEFINE control card, the SYNSEM language is used to define verbs. First the syntax of a verb is given using the SYN language. The verb is placed into the dictionary. The syntax specification is analyzed character by character, determining the type of each argument encountered. It counts the number of characters or uses a standard count allowed in each argument, and thus builds the format list. It also enters the symbolic character of each argument along with its format list position into an argument table for later reference by the REQUIRED control card and SEM language instructions. At the completion of analyzing the syntax, the argument table contains the one letter symbolic of each argument, in the order in which they will appear in the source statements. The REQUIRED control card containing the one letter symbolic of each required argument follows the SYN syntax specification. Each argument is found in the argument table and its format list position obtained. The format list is thus modified to indicate which arguments in the syntax are required with each usage of the verb. After the REQUIRED control card is processed, the generator must load the SEM program, which gives the semantics of the verb, into the logic and logic modifier lists. There are fourteen different formats for the thirty-six SEM instructions. There are fourteen corresponding routines in the generator to handle the building of the lists. For each instruction, the correct routine is called to setup the list entries. When a modifier of a verb is referenced by an instruction, the one character symbolic of the SYN language is given as a modifier to the SEM instruction. This character is looked up in the argument table and its integer position number is used for the logic list entry. (When a source statement is parsed by the translator, each argument is loaded into a table at the same position as is used for containing its SYN symbolic character in the generator.) Variables may be established in the SEM language by a symbolic name. This symbolic name is placed into the argument table after the symbolic SYN modifier characters, thus establishing a location for numeric reference in the logic lists entries and for storage use by the translator. The argument table provides storage only within a single definition, in that each new source statement starts using this table at its top, destroying symbolic names from previous source statements. The SEM instructions SX and TX provide storage locations for use throughout an entire source program compilation. A table exactly like the argument table is used, except that the location symbolic name is never destroyed, thus giving each definition access to the same location and providing for exchange of information between definitions. If a SEM instruction requires alphanumeric information, or if one entry in the logic list is not sufficient to contain all the necessary data for the instruction, a pointer to the logic modifier list is placed in the logic list entry, and as much space as necessary is used in the logic modifier list. A two-digit op code (1-36) for access by the translator, and a branch and link address are always in a standard location in each logic list entry.

Equate

Many verbs in a particular POL developed for use with automatic test equipment are similar in syntax and semantics. For example, the source statement for connecting a stimulus to deliver volts is very similar to the statement for connecting kilovolts or millivolts. The equate section of the generator was therefore developed whereby two or more verbs may share the same definition, and therefore the same list area. The name of the verb to be equated is placed in the dictionary and all the pointers associated with the equated verbs are used with the new one, thereby using the same definition. In order that the small differences of the two verbs can be taken into account, the CHFLG SEM instruction must be used in the original definition. This instruction requires two indicators which are stored in the dictionary. A definition always sets them to zero, but they may be set to any desired value by the language designer using the EQUATE option. The CHFLG op code can test the value of these indicators and thereby set up branching logic in the SEM language program to control the translation.

Delete

The generator section of UTEC maintains a list of available cells to which the DEFINE section looks as it makes the various list entries for a given definition. The purpose of the DELETE section is to remove previously defined verbs from the dictionary and to restore their various list entries to the list of available cells. This is done by changing the link at the bottom of the list of available cells to point to the top of the list entry for the deleted verb. This makes the last list entry for the deleted verb, the bottom cell on the list of available cells.

Equipment

In this section, the generator builds the hardware-name table and allocates area in the hardware-usage table, both of which are used by the equipment designator. All equipment of each type which the system has available is defined in the SYNSEM language by the SYMBOL and DATA instructions. The generator calculates the area required in each table section, and sets up the pointers in the hardware name table and hardware usage table. The DATA cards contain the name of one piece of equipment along with its terminal connections in the allocated positions in the hardware name table.

TRANSLATOR

The analysis and translation of source programs and the subsequent output of intermediate code is handled by the translator. When analyzing a source statement, the verb is first checked against the list of defined verbs in the dictionary. When a match occurs, an attempt is made to verify any main units allowed with the verb. Once a verb and main-units match is made, the associated dictionary entries are used as references to the format and the logic lists where information specified by the SYNSEM program for this source statement has been stored by the generator.

Using the format list as a guide, the translator parses each source statement and creates an argument table as it goes. A left-to-right scan of the source statement is initiated looking for a modifier of the type specified in the first format-list entry. If the modifier is found, it is placed in the first position of the argument table. The scan continues looking for the next modifier as called for in the next format list entry and places it in the next available argument-table position. An error condition exists if the scan fails to verify a modifier, unless that modifier is not required, in which case a dash is placed in the argument table in the next position. The scan finishes when the entire format list for this verb has been considered and an argument table entry is present for each item in the list. Once the format scan has been completed, the translator turns its attention to the logic list where the algorithm for generating intermediate code has been stored for this source statement. Each entry in the logic list is a numeric representation of one of the SEM instructions. A two-digit op code is extracted from each entry which identifies the particular SEM instruction requested. Once the instruction is known, the translator is able to completely dissect the logic list and modifier list entries for this instruction and perform the desired operation. All references by the instruction to the verb modifiers are made by simply referencing the argument table position for that modifier, as the parsing algorithm already has inserted the modifiers in the table. As an example, consider the following SYNSEM specification:

```
CONN     AAA   KVDC   JC     JD
  .
  .
  .
RANGE    A     10.0   20.0        100
```

The generator creates the argument table as follows:

1	A
2	K
3	C
4	D

Since the character A is in position 1, this position number is used in the logic list when the RANGE instruction is processed by the generator. When the source statement: CONN 14.6 VDC J101-42 J16-33 is parsed by the translator, the argument table is filled as follows:

1	14.6
2	VDC
3	J101-42
4	J16-33

When the translator discovers the RANGE instruction number in the logic list, it decodes a reference to position one in the argument table for the number it is to test. In the example, the number 14.6 checked to determine if it is between 10.0 and 20.0.

Each logic list entry provides the translator with the position of the next instruction to be considered, or, in the case of conditional instructions, the translator must pick the next instruction from two or three choices after it performs the current instruction.

The translator continues through the logic list until the END op code is discovered, at which time it has completed its analysis and code generation for the source statement under consideration. The next statement is read and the entire process repeats. When the translator reads the END verb, it turns the intermediate code generated for the program over to the assembler for final object-code production.

EQUIPMENT DESIGNATOR

Each time the translator processes a source statement which requires the use of ATE equipment, an entry on a tape is generated by means of the SEM instructions EQUI or PREAS. This tape is called the request tape. The translator itself has no ability to select equipment from the available equipment pool to satisfy the needs of the source statement. The SEM language program used to translate these source statements requiring equipment first generates a unique symbolic number which will be used by it to symbolically refer to an equipment name in the intermediate code it produces. It then determines the type of equipment required by the source statement and generates the request tape entry. Each such entry generated tells the type of equipment desired and the symbolic number used to identify it, and tells how the terminals of that equipment should be connected. In the case when a specific piece of equipment must be used in a particular manner, the translator also processes an equipment preassignment by producing a request tape entry which gives the specific name of a device, and tells how it is to be connected.

The function of the equipment designator is to read and process the entries on the request tape produced by the translator. It attempts to match an equipment name of the correct type to each symbolic number and produce information describing how each piece of equipment is to be connected. In the assembly of the intermediate code, each symbolic number is replaced by the matching equipment name as provided by the equipment designator.

The equipment designator operates using two tables: the hardware-name table, and the hardware-usage table. The hardware usage table is divided into two sections for each equipment type: the hardware-assignment section and the hardware-request section.

The hardware-assignment section for each equipment type contains one assignment indicator and one row for each piece of equipment of that type. The indicator gives the status of the equipment, while the row contains references to the connections made to this equipment.

The hardware-request section for each equipment type can contain a number of requests for equipment of that type. Each request section entry is made up of an indicator and row like those in the assignment section, plus a half-word which is used to hold the unique symbolic number for the request. The number of entries allowed in the request section for a particular type of equipment is specified in the SynSem equipment definition.

The requests processed by the designator fall into two classes: 1) those which name specific pieces of equipment, and 2) those which symbolically seek an assignment of any piece of equipment of a specified type. When fulfilling requests, two passes are made over the request tape with the items in classes 1) and 2) being handled on passes one and two respectively.

On pass one, the designator simply reads the requests, and in the hardware assignment section, sets the indicator for the named piece of equipment and fills the rows with the connection references. Before the first pass, all indicators reflect an equipment-available status. After pass one, the indicators of the equipment named in pass one are set to indicate one of two states: 1) hard preassigned-specified equipment may only be used as stated 2) updated preassigned-specified equipment should be used as stated if possible, but may be used differently if needed. This preassignment is automatically generated at the end of each compilation for each piece of equipment used. It then is submitted on the following run to insure that the same wire connections will be generated whenever possible, even when changes are made in a source program.

On pass two, the designator tries to assign one piece of equipment to each symbolic request. In addition, it creates the matching list to be used by the assembler when processing the symbolic references in the intermediate code.

Each request causes a scan of the hardware assignment section for the type of equipment requested. If the connections of the request match those of a piece of equipment already used, the request is matched with that equipment. If the connections of the request do not match those of any already used, a new piece is assigned to match this request. If all the equipment of the type requested has been used, the request is put into the hardware request section and saved. When the entire request tape has been read in pass two, the designator is finished unless some unfulfilled requests remain in the request section. If unfulfilled requests do exist, the designator scans the assignment section for all equipment which was update preassigned but not used in this compilation. It resets the indicators of these equipments to reflect an available status. An attempt is then made to assign the unfulfilled requests to the equipment made available. If the request still cannot be satisfied, it remains in the hardware request section. Finally, a wire connection list is produced from the hardware assignment section giving all the equipment used in the compilation and how it is to be connected. How the equipment was used in relation to a possible previous compilation is also stated. Error conditions are produced based on entries remaining in the hardware request section. New update preassignments are also generated for use if the program is to be changed and recompiled, so that a similar wire list can be produced.

CONCLUSION

At this time, UTEC has been completely written and checked out using FORTRAN IV, and a language developed for use with one type of automatic test equipment (LCSS) currently being produced by RCA has been implemented using UTEC. The implementation of another language for a second type equipment is being considered at this time.

It is interesting to note that after having defined the language to UTEC, the users could evaluate the quality of the language and its usefulness, and suggest changes and improvements. These changes were easily incorporated into the language almost daily during a shake-down period, thus allowing them to be tested within days after they were conceived. The overall effect was to stimulate ideas for improvement. Thus, a much more effective language than that originally specified was developed.

ACKNOWLEDGEMENT

The compiler design has been the joint effort of several groups and individuals within the ASD organization. Special mention is made of engineers and programmers within the ATE support group, without whose cooperation this program would not have been possible.

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Computer controlled pattern making

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H. O. Hook

The first step in the manufacture of many electronic components is the making of a set of precision master patterns often called "artwork". In manufacturing, the master pattern is replicated into the final product. An alternate to the traditional hand methods of making master patterns employs a numerically controlled drafting machine capable of producing the artwork by exposing photographic film with a moving beam of light. The input to the drafting machine is produced on a computer with the aid of a graphical language and a computer program especially developed to interpret that language. Both the automated drafting machine and the graphical computer language used at the Laboratories are described in this paper.

THE COMPUTER AIDED method for generating artwork improves the accuracy of the artwork, lowers the cost, and reduces the turn-around time as compared to the manual method. The accuracy and quality of the artwork is largely governed by the precision of the drafting machine, which, for the Gerber model 632, is approximately 0.001 inches. [The model 632 is made by Gerber Scientific Instrument Corporation, Hartford, Connecticut. RCA Central Engineering in Camden operates two model 1032 plotters, which are faster than the model 632.[1]] Because the process is under computer control, the most complicated and repetitive patterns can be made without errors. Both the turnaround time and the cost are reduced because the automated equipment is able to work rapidly and the time required to draft an accurate working drawing can be eliminated. In contrast to conventional methods, a large part of the cost and time for artwork production by this process is consumed in detecting and correcting errors in the computer programs. At the Laboratories, all complicated artwork is made under numerical control.

There are a couple of manual methods available for making artwork for electronic components and circuits. Patterns can be "taped" on transparent film by attaching opaque sticky tape to the film. For more precise patterns, a manual coordinatograph is used to knife-cut a 2-layer plastic film such as Rubylith (trademark of Ulano Inc.).

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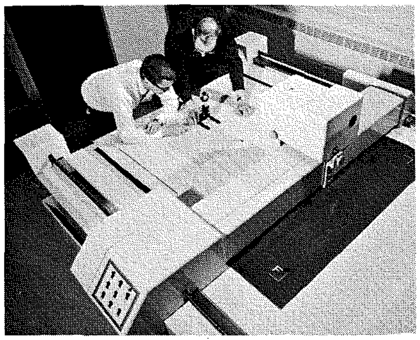

Fig. 1—The automatic drafting machine.

The bottom layer is clear and the top layer is a red plastic that can be cut and then stripped off. Where the red material on top is stripped away, the pattern is transparent while the remainder of the pattern is opaque to actinic light. Neither of these processes is especially easy to automate. Although the Rubylith film can be cut automatically, the red layer still must be stripped manually. The precision of coordinatograph-cut masters is about the same as for automatic drafting. These manual methods are adequate and frequently quicker for many simple patterns.

The practical application of a numerically controlled drafting machine to the production of artwork was dependent upon the development in 1965 of the photohead for exposing photographic film. Numerically controlled (N/C) machines had been used for many years in the metal-cutting industry, and N/C drafting machines were used with a pen to verify programs for the N/C milling machines. The photohead is merely a tool replacing the pen and giving the drafting machine greater flexibility and an additional medium to work on—photographic plates and films. When a suitable photohead is attached to a rugged, accurate drafting

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machine, it becomes capable of producing the artwork required for electronics manufacturing.

The difficulty of direct tape preparation for automatic drafting led to the need for special computer programs to generate the input to the drafting machine. Often the control tapes are lengthy because of repetitive patterns or because of special sequences of commands which are required to form certain basic patterns such as circles and rectangles. But in either of these cases, the computer is able to generate the lengthy control tape from a short and simple input. In the metal cutting industry, the APT (automatically programmed tools) language is used to program numerically controlled milling machines by means of a general purpose computer. Following this example, a language—PRogrammed Electronics Patterns (PREP)—was developed to describe artwork patterns, and it is used to program the patterns made on the automatic drafting machine at the Laboratories.

AUTOMATIC DRAFTING MACHINE

Fig. 1 shows the automatic drafting machine. Its component parts are a 60X48-inch table, *y* carriage, photohead, drive mechanism, and electronic controller. The mechanical parts are designed for accurate positioning of a light beam from the photohead on the photographic plate or film. Digital stepping motors couple the electronic controller to the mechanical drive mechanism. The controller itself derives the pulse signals for the motors from a paper-tape input. In operation, a photographic film or glass plate is placed on the surface of the table and the photohead moves above the photographic medium. The photohead weighs approximately 40 pounds and it must be positioned within 0.001 of an inch of true position. The massiveness of the table and the *y* carriage on which the photohead rides is necessitated by the weight of the photohead and the accuracy requirement.

DRIVE MECHANISM

Fig. 2 is a schematic representation of the drive mechanism. A lead screw along the *y* carriage drives the photohead in the *y* direction. Twin lead screws, one at each end of the *y* carriage move it in the *x* direction. The *x* lead screws are coupled to a torque bar running along the end of the table. The motors for the *y* axis are mounted on the *y* carriage and move with it. The motors for the *x* axis are stationary and drive the torque bar through spur gears. The lead screws and their recirculating ball nuts are key components in guaranteeing the repeatable and accurate positioning of the photohead. The gears and ball nuts are adjusted and preloaded to hold a repeatability error of less than 0.0005 inches.

Four DC stepping motors are used to drive each axis of the machine. The four motors along one axis are on a common shaft and together act as one motor. For each step, power to a pair of windings on one of the 4 motors is changed. The controller cycles the drive current to the motors in 16 phases corresponding to the 4 ways of driving the windings of each of the four motors. When an axis is stopped, a direct current of five amperes in each excited winding locks the motors. Each step of the motors corresponds to 0.0002 inches of motion of the plotter. The controller causes the motors to step up to 2500 times/second and assumes that the motors never miss a step.

CONTROLLER

The controller takes commands from a paper tape or a keyboard and sends control signals to the motors and the photohead, thus causing them to execute the input commands. Information on paper tape enters the controller one block at a time. Each block contains the information for the drawing of one line, the selection of an aperture, or one flash of the photohead. After the block is read from paper tape, the function is performed. Each block on the paper tape may contain 3 numbers, which enter the *x*, *y*, and *d* registers of the controller. The *d* register governs the functioning of the photohead. The *x* and *y* registers hold a count of the distance to be moved along the two axes. The registers are shown on the block diagram of the Gerber 600 series controller (Fig. 3).

The most important function performed by the controller is linear interpolation. Linear interpolation in N/C machines is the process by which straight lines are generated. The machine steps along a straight line derived step-by-step by the controller

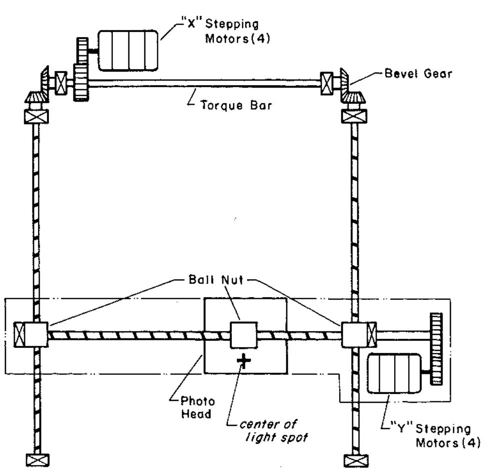


Fig. 2—The Gerber drive mechanism.

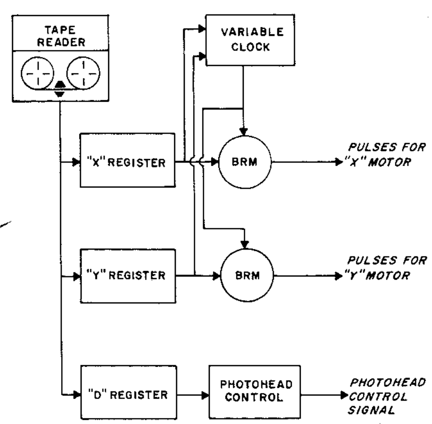


Fig. 3—The controller.

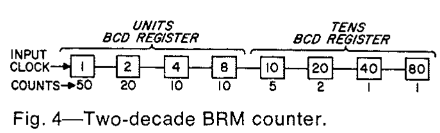
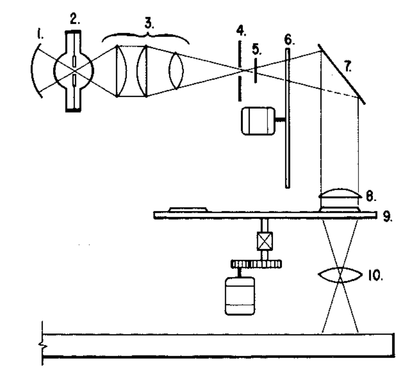


Fig. 4—Two-decade BRM counter.



1. Sperical Mirror
2. Hg-Ar Lamp
3. Condenser System
4. Aperture
5. Shutter
6. Varying ND Wedge
7. "Cold" Mirror
8. Field Condenser Lens
9. Aperture Wheel
10. Projection Lens

Fig. 5—The photohead—aperture selection mechanism and optical path.

from the total increments of the line specified by its x and y registers. Because of linear interpolation, the plotter is able to draw even the longest lines with the information from only two inches of paper tape. By way of comparison, simple digital incremental plotters that are often used with computers require a command for each incremental step of motion. Such plotters require far more information on their control tapes. A typical incremental plotter has a step size of .005 inches or .010 inches while the automatic drafting machine used for artwork production steps .0002 inches at a time. It would be impractical, even on magnetic tape, to record data for each .0002 inch step. To record each step of one 30 inch motion would require 15 feet of 800 character per inch magnetic tape.

INTERPOLATION AND COUNTING

A binary rate multiplier (BRM) circuit generates the straight line motion, or linear interpolation. When a line of slope y/x is drawn, the BRM produces pulses to the y and x motors at rates which are in the ratio y/x. This causes the plotter to move along a straight line at that slope. A binary rate multiplier circuit produces a pulse train at a rate proportional to the product of a number contained in a register times the rate of an input clock. Fig. 4 is a schematic diagram of a 2-decade BRM counter. The counter is a common BCD type with the input clock pulses entering at the left end. Each box in the figure represents one flip-flop in the counter. The number in each box represents the value of that flip-flop in the 1-2-4-8 BCD system. The key to the BRM is in the number below each box, which represents the number of times that particular flip-flop is set while the counter counts from zero to 99. At each count, one, and only one, flip-flop is set. The figure shows that the 4 flip-flop is set ten times while the 10 flip-flop is set and then reset five times while counting from zero to 99. The numbers 5, 2, 1, and 1 are prominent in the bottom row of the figure. The outputs of the individual flip-flops are pulse trains at rates proportional to the numbers at the bottom row of the figure. Let C be the input clock rate. An output pulse train at exactly $\frac{50}{100}C$ can be obtained by taking the output of only the 1 flip-flop. An output pulse train at the rate $\frac{72}{100}C$ can be found by taking the outputs of the 1, 2, and 20 flip-flops, which will set a total of 72 times for every 100 clock pulses entering the counter. A BRM is made by coding the number representing the desired rate multiplier in a 5-2-1-1 code, and gating the output pulses from the individual flip-flop according to the number thus coded.

In the automatic drafting machine, a common clock signal is passed through two BRM counters with the rate multipliers being the numbers in the x and y input registers. The outputs of the BRM circuits become the desired motor pulses. To smooth the output, the clock is run at 4 times the necessary rate and only 1 pulse out of every 4 is sent to the motors. To assure correct motor speed, the rate of the input clock for the BRM's must be inversely proportional to the size of the larger number, either in the x or y register. A separate BRM circuit is used to make this clock pulse.

VERIFICATION

The automatic drafting machine at the Laboratories operates with no feedback from the drive mechanism to the controller. Despite the lack of feedback, the accuracy of the drive system can be and is verified in every pattern made. The computer programs which make the tapes for the plotter start each control tape with instructions to produce a mark on the lower left hand corner of the pattern. At the end of the control tape are instructions to go back to that same mark and add to it. Any misregistration between the addition made at the end and the original mark will be seen very easily. Since all commands on the paper tape and internal to the controller are incremental, any error will produce a gap in this registration mark. The registration mark being correct guarantees that there was no error in motion during any of the plot.

PHOTOHEAD

The photohead is used to project light onto the photographic medium. It replaces the pen used in an ordinary drafting machine. Fig. 5 is a sketch of the photohead showing the aperture selection mechanism and the optical path used. A mercury-xenon arc lamp produces a high intensity source of light which is condensed through a wide-aperture lens into a spot on a rotating neutral-density filter having density changing with angle. This filter is used to maintain the intensity of the light proportional to the speed of the photohead as the speed increases at the beginning and decreases at the end of a line. A shutter completely blocks the light between exposures. After passing through the filter, the light is reflected from a 45° mirror and condensed again onto the projection lens. Just below this last condensing lens is the aperture wheel. The wheel pivots on a vertical axis and can move into position within approximately one second. A small motor and clutch drives the aperture wheel and a pawl stops the wheel at the correct position. The apertures are imaged on the film by the projection lens.

The demands on the projection lens for resolution are not severe, but it is important that there be very little scattering of light. As the photohead moves, the scattered light accumulates over the photographic emulsion and can fog it badly. Although the design of the photohead minimizes the scattered light, certain bad programming practices can lead to badly fogged artwork.

Apertures of limited precision can be made quite simply from a thin sheet of metal by drilling or otherwise cutting holes into it. The shape of the central hole determines the shape of the light beam used to expose the photographic film while the other holes are for locating and fastening. More precise apertures are usually made on Photoplast (trademark of the Eastman Kodak Co.) an acrylic plastic plate with a photographic emulsion on it. The emulsion is exposed with registration marks and the negative of the required aperture pattern. The plastic is registered with a jig and drilled with holes for mounting and for positioning against dowel pins in the aperture wheel of the plotter. Apertures take about 1½ hours to prepare by this method. A standard set is used for most jobs, but special designs can be made for particular jobs. An aperture can be changed by the operator as part of the setup for a job in about five minutes.

The apertures used for drawing lines are chosen from among slit, square, annulus, and round apertures. Square apertures and slit apertures are most useful for drawing lines aparallel to an axis of the aperture. They also give the best definition of line width. Slit apertures moved in the direction of the narrow axis give the sharpest definition at the ends of the line. Apertures other than slits leave the ends of lines fogged and poorly defined. Round apertures are the most easily made omnidirectional apertures, but they overexpose the center of a line by a large amount in order to produce adequate exposure near the edge of a line. This overexposure is acceptable for isolated lines but can lead to fogging around closely spaced lines. Annulus apertures allow no light through the center of the aperture in order not to expose the center of the line as heavily. Apertures have been made with multiple concentric annuli calculated to produce uniform exposure across the whole width of lines drawn in any direction.

PROGRAMMING

The preparation of a tape to control the automatic drafting machine is a process which is often difficult and expensive and never completely automatic. This process of preparing the information for the automatic drafting machine is called programming. The dominant labor expense of numerically controlled pattern making is for programming. Although the input commands to the automatic drafting machine are fairly easy to use, programming by direct preparation of those input commands is tedious and likely to result in errors. To program complex and repetitive patterns, the assistance of a computer is essential to economical automatic pattern making. The RCA 601 computer at the Laboratories assists in programming for the automatic drafting machine. This computer interprets statements in the PREP (PRogrammed Electronics Patterns) language and translates them into the symbols required on the tape for controlling the plotter. The PREP language provides a powerful set of commands in a convenient numerical format. It is especially designed to be suitable for programming the type of patterns required for electronics manufacturing. Programs in the PREP language are a description with symbols and numbers of the patterns required.

Short control tapes for the automatic drafting machine are occasionally punched directly on a flexowriter. These may be made into loops, which the automatic plotter can read many times to draw a very repetitive pattern. Another approach to programming uses a digitizer and an accurate ink or pencil drawing of the pattern. The digitizer converts the coordinates of the drawing into punch cards or paper tape. When a paper tape is made, it can be used directly on the automatic drafting machine to plot a line pattern with the full machine accuracy. Punched card output of a digitizer can be processed by a computer to add such things as fill-in of interiors. Then a tape made by the computer is used to control the automatic drafting machine. The digitizer is especially useful for patterns that are not repetitive.

The best form of the original drawing for artwork preparation is dependent on the process being used. The manual coordinatograph is equipped with a scale clearly marked for reading absolute coordinate positions. Because of this, integrated circuit drawings commonly are dimensioned with all coordinates indicated from a common datum. Both edges of every line are usually dimensioned. The digitizer requires no dimensioning at all, but patterns must be drawn accurately and completely and must fit to a grid on the drafting paper. Programming in the PREP language can often be done from a freehand sketch without elaborate dimensioning. For example, for repetitive patterns, only the starting point and the repeat interval need be specified. The relative costs of the several methods of artwork preparation can only be measured and understood when their effects on the design process are included.

As the programmer plans a PREP program, he takes into consideration the characteristics of both the plotter and the pattern. The programmer attempts to minimize the plotting time, paper tape length, the number of aperture changes, and programming time. The pattern is scaled to the optimum size for later photo-reduction. The use of special apertures for some patterns reduces the time for plotting or improves the quality of the patterns. The examples in Fig. 6 are some typical patterns made from PREP programs.

LINES, RECTANGLES, AND POLYGONS

Before starting to write the program, the programmer classifies the various parts of a pattern in terms of the type of PREP instruction he will use to describe each part. The PREP language provides for three forms of pattern: lines, rectangles, and polygons. Other patterns are made by flashing special apertures. Lines are usually drawn with a single motion of the plotter. The aperture used to draw a line determines its width. For a rectangle or other polygon, the computer chooses the best apertures (based on size) from among the available apertures and calculates the motions for the plotter to blacken the interior of the figure. When a rectangle is called for by a *block* instruction, the computer only uses square apertures in the fill-in process.

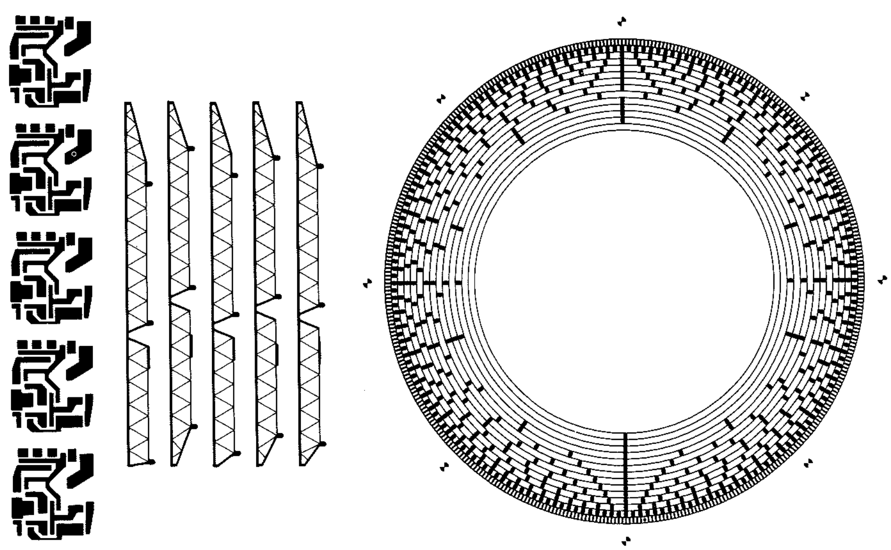


Fig. 6—Typical patterns made from PREP programs.

When arbitrary polygons are specified to be filled in, the computer selects from among the round apertures.

Instructions to plot are used to draw lines. Either the coordinates of the end of a motion or the coordinate increments can be given in the PREP language statements. The radius of curvature is given for lines which are circles and arcs of circles. A verify instruction is available so that the programmer can check the coordinates of a plot against what he believes them to be. When plotting with incremental plotting instructions, a verify instruction is useful for checking that the sum of the increments is correct. In the PREP language, a polygon to be filled in is specified by plotting along the periphery of the polygon and indicating which are the first and last sides.

In the PREP language, the fake aperture instruction provides for drawing lines having widths different from the width of any available aperture. With the fake aperture instruction, the programmer can assign the width he desires to an aperture number. Whenever the computer encounters this aperture number, it will generate motions with smaller, real apertures to fill-in the width of line requested. Sometimes it is necessary to clean up the ends of lines by flashing. This is necessary because the plotter in its natural, line-drawing mode leaves the ends of lines underexposed. With the fake aperture instruction, the plotter can be forced to flash at the ends of certain lines in order to complete their exposure. The fake aperture instruction can also substitute one real aperture for another any time it appears subsequent to the fake aperture instruction.

REPETITIVE PATTERNS, SCALING, MIRRORING

The PREP language is especially valuable because it is able to generate repetitive patterns from a simple specification. This language includes an instruction for indicating the number of times a pattern is to be repeated. If a part of a pattern is to be repeated, the part is programmed with labels at its beginning and end. Then the repeat instruction calls for that part of the pattern between the labels to be repeated a certain number of times.

Sometimes it is desirable to repeat figures at different angles, symmetries, or scale factors. A set of floating coordinate axes is available for this purpose. For each repetition of a pattern, the floating coordinate axes can be set up with the new angle, symmetry, or scale. Then the pattern is repeated relative to those axes with the repeat command. Parameters describing the floating axes can be changed even within a repeat loop. Thus, it is possible to repeat a pattern many times so that each time it is progressively rotated or scaled as compared to the previous time. This feature leads to the ability to draw a number of special patterns including fan-outs, shaft encoders, and patterns with mirror symmetry or rotational symmetry.

This facility for scaling individual parts of a pattern selectively is in addition to an overall scale factor specified at the beginning of the program. The overall scale factor is usually specified by the programmer so that he can program in terms of convenient dimensional units but still produce artwork at the correct size for subsequent photo-reduction.

OTHER FEATURES OF PREP

The preparatory card starts the instruction sequence for each control tape made from a PREP program. Sometimes several control tapes are made from one PREP program, when a set of overlaid or otherwise related patterns are programmed. The preparatory card indicates whether the pattern is to be filled in. Sometimes patterns are made without fill-in and other time consuming processes so that the program can be plotted quickly for checking.

The tolerance statement is used to control the time required to make circles, arcs of circles, polygons, and blocks. Because the automatic drafting machine has linear interpolation, arcs and circles are approximated by inscribed equilateral polygons. The tolerance card controls the accuracy of this approximation. All polygons and some rectangles are filled in with round apertures. The tolerance instruction also specifies the allowable rounding on the vertices of the polygons and rectangles. It is often useful to maintain a library of patterns programmed in the PREP language. For small projects this is most easily done on punched cards. Each program in the library is kept on a small deck of cards appropriately marked so that it can be inserted into a larger program at any time. For larger projects where a number of people are sharing patterns, it is desirable to keep the programs for the patterns on a magnetic tape called the Library Tape. A program is used to delete patterns from the tape or to add to the library. Someone must be responsible for keeping a log of what is on the tape and distributing instructions for using the patterns in the library. The PREP language includes a statement for fetching patterns from a library tape.

Some patterns drawn by means of the PREP system have been generated from programs written in the other computer languages available on the 601 computer, SNOBOL and FORTRAN. The technique for doing this is simple. The output of such programs are formatted to look like the PREP-language statements for the pattern. FORTRAN can be used to write PREP statements on magnetic tape, and the PREP processor can then read these statements as if they were on cards and produce the control tape for the automatic drafting machine. This facility is an important enhancement to the concept of symbolic programming of electronics patterns.

CONCLUSIONS

This paper has discussed two aspects of the making of electronics patterns with automated equipment. A numerically controlled drafting machine and computer programs are coupled together to generate patterns. In this system the user becomes a programmer never seeing or touching the drafting machine. He talks to the computer and describes the patterns. His tool is a language for describing patterns and he works with the elements of that language for specifying his own pattern. The computer makes a control tape for the automatic drafting machine. Its accuracy and capabilities in the final analysis determine the quality of the patterns that are made.

Automated pattern making has been valuable to a variety of projects with unusual pattern requirements. Both the precision, automatic drafting machine and computer assisted programming are growing in importance as the electronics industry moves toward more complex components.

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APTE—automatic production test equipment

N. A. Teixeira

Automatic Production Test Equipment (APTE) is the electronic subsystem for the Autotest system which performs computer-controlled on-line testing of color kinescopes at the Marion, Indiana, plant of Electronic Components. The system operates at a high rate without stopping or slowing the production line. In addition to computer-controlled electrical testing, the system performs statistical analysis, supplies corrective action instructions to the process and directs the disposition of the product—accept, reject, or three different types of rework. In many of the tests, the acceptance limits can be modified by the results of previous tests.

As part of the project team organized by Electronic Components to develop the concept of Autotest into a practical system for production-line testing of color kinescopes, Aerospace Systems Division accepted the responsibility for the design, construction and test of the electronic subsystem—APTE (Automatic Production Test Equipment). Early in the program, a comprehensive study was conducted. The test methods then in use in factory and laboratory were analyzed in terms of their convertibility to automated programs. From EC came the characteristics and test requirements of tube types still on the drawing board or in product development. The goal of the project team was to establish a test capability general enough to cope with any color television tube that might be in production during the next five to ten years.

SYSTEM DEVELOPMENT

Using the operational methods of Test Requirements Analysis, developed during the extensive experience in military Automatic Test Equipment, ASD translated the test requirements of the general classes of tubes into the requirements for the test system. Several matrices of requirements were established. Together with the fundamental timing constraint imposed by the production line rate — which in reality established the system *clock* — each matrix helped to determine the allocation of test functions to individual stations. The basic measurement capability, the spectrum of stimuli required, and the routing scheme necessary to perform the switching of stimulus and measurement—all had to be in consonance with the settling time required by the tubes as well as the conveyorized clock.

As the overall structure and sequencing of test operations evolved, there had been a parallel development of data processing requirements. In combination, these set the ground rules for the computer requirements in terms of core, drum, and tape memory capacity as well as interrupt handling capability.

Out of the study, a system configuration was synthesized which consisted of the following major elements:

1) Computer and peripherals;
2) Test controller;
3) Shared stimulus unit;
4) Five test stations for
   a) Shorts and leakage,
   b) Emission,
   c) Cutoff,
   d) Focus breakdown, and
   e) Anode breakdown;
5) Data entry station;
6) Annunciator control; and
7) Status display and remote printer.

These elements are shown in their functional interconnection in Fig. 1.

GENERAL SYSTEM OPERATION

System timing is based on the speed of the tube conveyor which operates at the equivalent production rate in access of 250 tubes/hour. A total of 75 tests may be performed on each tube. A number of tube "classes" or categories of tubes, each class consisting of many different types, can be tested. The computer and input-output control are in an environmentally controlled room several hundred feet from

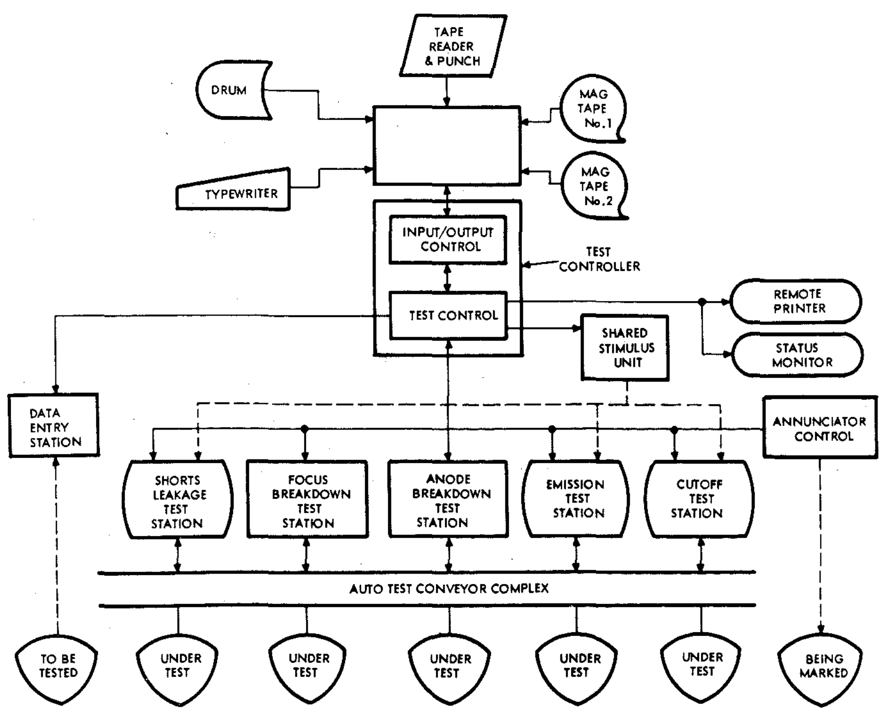

Fig. 1—APTE functional block diagram.

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the test area. Although the input-output control and the test control are functionally part of the test controller, they are separable in location and connected via shielded cables.

Out in the factory area, the tubes pass along an appropriately staggered series of three measurement stations and two break-down-test stations. At each test station, an air-driven contactor engages the tube contactor, connecting the test station to the tube elements. All electrical tests are performed while the tube is traveling. After approximately ten seconds at a station, the two halves of the contactor disengage; the tube continues down the line while the contactor (associated with the station) returns to its starting point for the next tube. The contactor engagements of the three electrcal test stations are time-staggered to give an effective test time for each tube.

The information entered for each tube at data entry indicates the tube type and manufacturing history. At the shorts and leakage test station, the inter-electrode current is measured between all combinations of tube elements.

The kinescope is then checked for the high voltage stability of its focus element (focus breakdown) and anode element (anode breakdown) as well as its stray and grid emission. At the emission test station, the kinescope is checked for its gas content, resistance in the anode connection, and the emission characteristics of each gun. At the cutoff test station, the kinescope is tested for current cutoff characteristics and maximum cathode current of each gun as well as for filament current.

The results of all the tests performed on each kinescope are evaluated and at the completion of testing, the computer-generated decision causes the kinescope to be labeled by the annunciators to indicate disposition of the tube. Rather than a simple GO/NO GO decision, the labelling can direct any one of the following next steps: tube OK; re-age; crack-off; reflash: or salvage analysis.

As the annunicators mark each tube, the selected disposition is also shown by an appropriate light on the status monitor which also has color-keyed lights to show the operating status of test stations, circuit breakers, conveyor and main DC and AC power. At the unloading point, where the kinescopes are removed from the conveyor, there is a remote printer which prints out for each tube labeled *crack-off* or *salvage analysis,* the carrier number, tube type, serial number and test defect code. The printer-control logic also makes provision for the operator to request a special print-out of test results on any tube(s) for quick analysis.

SYSTEM CHARACTERISTICS

High-speed programmable power supplies, high-speed relays, and sensitive measurement circuits are used to perform the tests. The digital computer with associated input/output equipment controls test operations while digital logic circuits transmit and receive signals between the system and the computer. A priority system of interrupts dictates the order of functions to be performed by the computer in controlling the system.

Measurement and Stimulus Routing

The measurement and stimulus routing presents four of the main technical challenges in the system development:

1) The combination of high voltage stimulus (up to 30,000 volts) and low current measurement (down to 1 nanoampere in the same test complex.

2) The need to protect each supply not only against direct shorts but against much higher voltages from other supplies which can become temporarily connected to the lower voltage supplies during arcs or shorts in faulty tubes.

3) The requirement for bi-polar operation of the stimuli in their application to tube elements.

4) The requirements for APTE included tests that had not previously been a part of production tests and some that even a laboratory could not do quickly enough to maintain time correlation between data taken at the beginning of the test and the data at the end of the test.

System Timing

The APTE system was designed to relieve the programmer of most of the burden of detailed timing found in automatic programmed testing systems. Control words from the computer may be batched at computer speed, without hanging-up the computer to wait for the test complex to act on a given instruction. Thus, the computer is tied up for a minimal time period only, and is largely available for analytical and statistical work. The internally-controlled breakdown stations require service from the computer for only one short time per tube (less than a millisecond to service and evaluate the results). Although the required system time delays are initiated by the computer, the waiting period for completion is a hardware function and does not tie up the machine.

The details of the hardware logic were translated into programming elements by a comprehensive programming manual. Using this manual, programmers at Electronic Components were able to maintain a clear interface between internal (computer) and external (test equipment) logic and timing.

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received the BS in Electrical Engineering from M.I.T. in 1947. At the Fabric Research Laboratory, he was involved in research and development of textile instruments as well as in research on the dynamics of fabric structures. Joining RCA in 1955 as a systems engineer, Mr. Teixeira was assigned to the analog computer systems analysis operation. He was subsequently responsible for organizing and maintaining project control techniques on the APCHE for the Atlas missile system. After this, he was in charge of the program control group for a large satellite program. In 1963, Mr. Teixeira became Project Engineer for ATE in charge of planning and PERT operations, and in 1964 he assumed responsibility for the Automatic Production Test Equipment. During the progress of this contract, he also initiated and managed a program plan for providing test equipment for a highly classified program on an extremely tight schedule. Since mid-1966, Mr. Teixeira has been Manager, Systems Projects, for Industrial Automatic Test Equipment, concentrating on the application of ATE to RCA commercial production plants.

The total time to perform stimuli routing, measurement connection and signal processing for one test is extremely small. The exact time depends on such factors as the response time of the programmable power supplies to be used and the selected scale of the measurement preconditioner. The small time per test allows a large number of tests to be performed on each tube. Typical test times range from 20 ms to 240 ms. Average test times are in the 30 to 40 ms range.

Operational Flexibility

The wide range of stimuli, measurement scales, and routing configurations allows flexible operation of the APTE system. New tube types may be tested on the system as they are developed. New tests can easily be performed with the equipment. Three demonstrations of this flexibility occured during the development program.

1) With minimum impact on cost and schedule, the basic test rate capability was essentially doubled, thereby avoiding the duplication of one whole set of test stations which would otherwise have been required.

2) Later in the program, the new Einzel-lens tube was released. This tube employs a radically different arrangement, electrical and mechanical, between focus and anode characteristics. After exploring several alternatives, a modification was incorporated which provided the capability of testing these tubes.

3) During the final pre-test stages of the program, the ability to test either stray or grid emission, or both, at the anode and focus breakdown stations was added, without schedule impact.

Environmental Capabilities

The APTE system was designed to operate 24 hours/day, in the following environmental conditions:

Computer Complex

Temperature—50°F to 90°F.
Humidity—40% to 70%.

Test Complex

Temperature—50°F to 100°F.
Humidity—0% to 55%.

Most important, however, is the fact that the APTE system must operate reliably in a radio-frequency interference (RFI) environment not normally associated with digital equipment. The environmental disturbances consist of high-voltage arcing ("spot-knocking") process, arcing tubes and sockets on the test line, and high-voltage switching (30 kVDC) within the APTE equipment.

The consistent operation of the system in this environment is achieved in part by the following design features (some of which were developed under the duress of integrating in a simulated system mode).

Digital logic circuits specially strengthened to operate only on control signals, not on random noise spikes

Equipment cabinets are RFI shielded

RFI ducts providing equipotential envelope around cables between major elements

RFI filters on selected control lines
Shielded wire used exclusively for interrack wiring

Grounding techniques employed to reduce ground loop currents and noise pick-up points

Figs. 2a, 2b and 2c show the layout of the major units.

MAJOR COMPONENT UNITS

Computer Complex

The APTE uses a high-speed, general-purpose digital computer particularly suited for real-time applications.

Among its features are:

24-bit word plus parity bit;

Binary arithmetic;

Single address instructions with index registers, indirect addressing, programmed operators;

Completely automatic priority interrupt system independent of normal input/output channels;

Parity checking of all memory and input/output operations; and

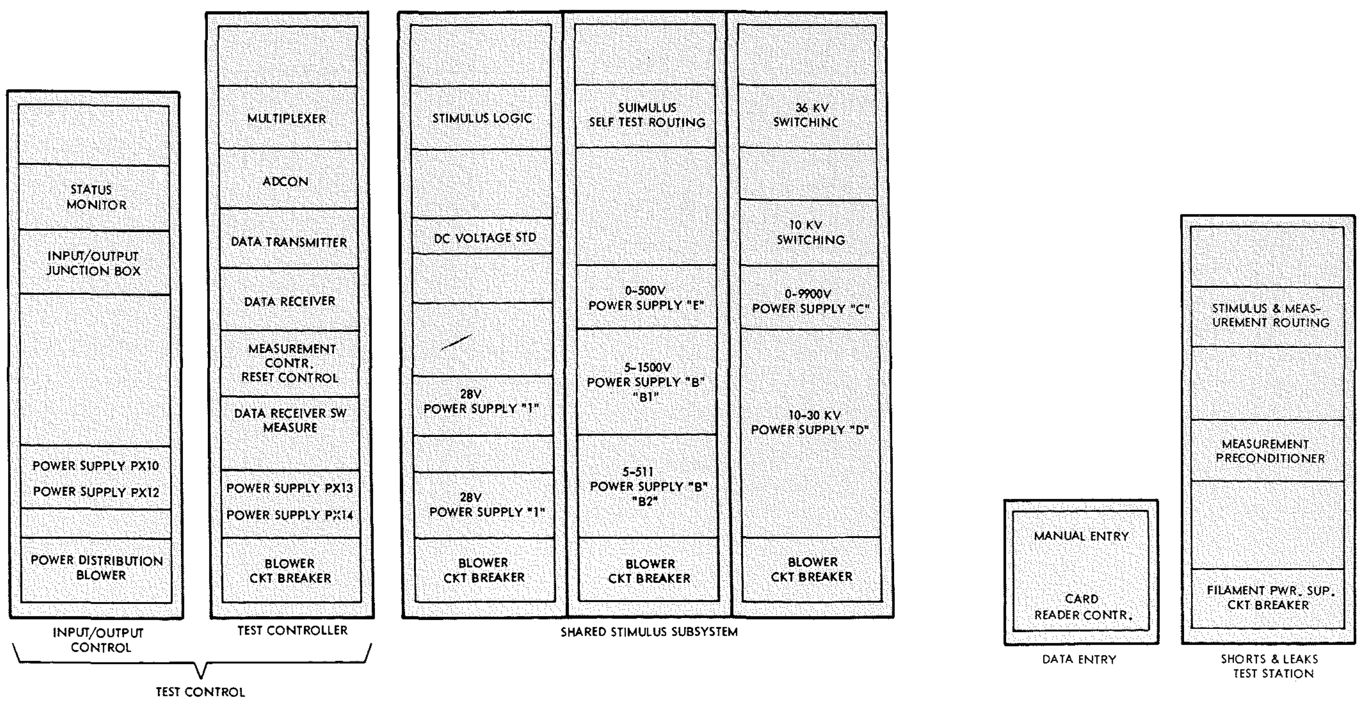


Fig. 2—Major component units.

Buffered input/output at rates in excess of 60,000 characters/second simultaneous with computation.

The following input/output equipment is used with the computer at the APTE installation.

- Magnetic tape systems (2)
- Automatic typewriter
- 10-character/second paper-tape punch
- 300-character/second paper-tape reader
- Drum memory

For program preparation, the following equipment is also used with the computer:

- Card reader
- Line printer
- 60-character/second paper-tape punch

APTE Test Controller

The APTE test controller connect directly to the computer's direct memory input/output, bypassing the buffers, and provides the capability to monitor and control test equipment and other devices. The controller is comprised of two major units: the input/output unit, (interface and device selector) is housed in a rack styled similar to and located near the computer itself; the test-control unit is in a rack similar and adjacent to the shared stimulus unit. The functions of the test controller (Fig. 3) are as follows:

1) Allows the computer to be interrupted by three levels of priority, containing one, two and twelve interrupts which are set by external contact closures.

2) Selects any one of 24 devices (expandable to 64) and can transmit 18 bits of data to those devices. All 42 lines are capable of being driven 100 feet or, with minor modifications, up to 1000 feet. (This gives a maximum capability of 1152 discretes, of which only one third are used in the present APTE installation).

3) Provides relay selection of 21 single-ended analog inputs (0 to ± 10V), converts these inputs to digital, and transmits the digital representation to the computer.

4) A programmable time delay is provided in two ranges—0 to 80 ms and 175 to 240 ms—incremented in 5-ms steps, to allow for the settling times of test equipment before measurements are made.

5) All digital output is at high speed, at a rate of 40,000 24-bit words/second, and can be sent along 50-ohm coaxial lines as far as 1,000 feet.

The operation of the test controller can best be summarized by analyzing its interrupt-handling functions.

Communication between the computer and the test stations and devices is initiated by interrupts. The interrupt may be one of three priority levels, any one of which will cause the master program to branch to a sub-routine to clear and service the interrupt:

Priority level 1 (highest level): This is the ADCON interrupt, generated by the test complex when a measurement has been made and the results are ready to read into the computer. In operation,

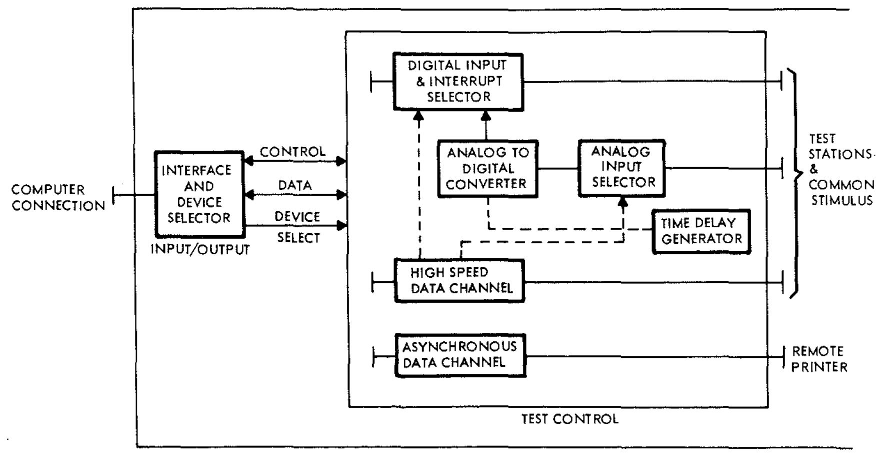
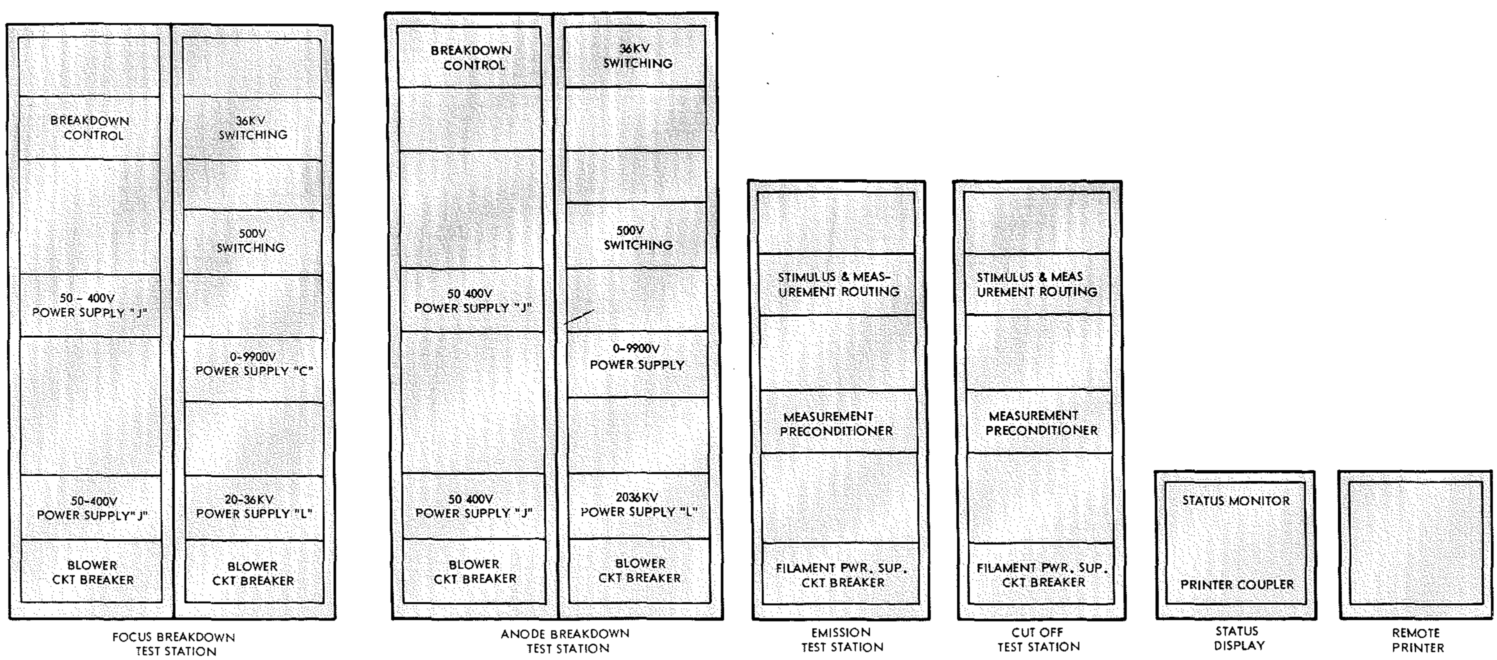
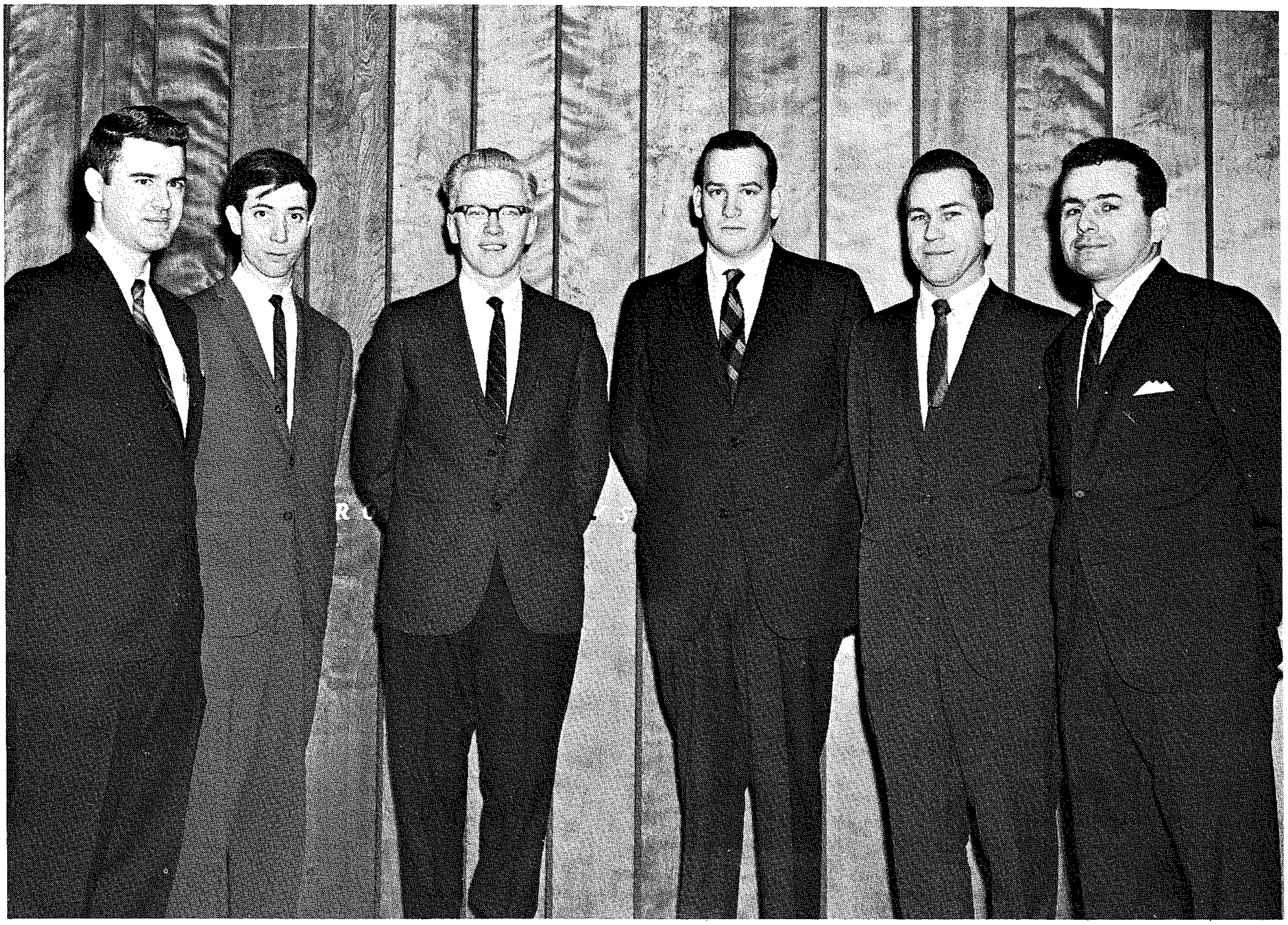


Fig. 3—APTE test controller.





ACKNOWLEDGEMENT: The team of William B. Locke, Herbert W. Silverman, Frank C. Hassett, Nicholas J. Amdur, Earle D. Wyant, and Angelo Muzi (left to right above) received the 1968 David Sarnoff Outstanding Achievement Award in Engineering . . . "for design, development, and installation of a computer-controlled fully automatic production test system for the on-line electrical test of color kinescopes." The system is described in this paper, and the author acknowledges the help provided by this team in the manuscript preparation.

over 37,000 priority/interrupts occur per hour.

Priority level 2 (2nd highest level): This interrupt is generated when information from either one of the breakdown stations is ready to be read into the computer. The information contains the station name (FOCUS or ANODE), arc count, and stray emission.

Priority level 3 (lowest level): This interrupt is caused by any one of a large number of conditions characterized by contact closures resulting from actions of the conveyor and tube carriage mechanisms.

The system response to these interrupts is dictated by the software programs. However, there are certain items of hardware design which operate on these interrupts to assure their validity and make them available for software action. In the APTE system, logic provisions were made for the individual storage of interrupt words. Gating and routing circuits were designed and assigned to the management of interrupt signals. To prevent false multiples of interrupt initiation, protection circuits were incorporated which guard against the usual results of the contact bounce of large relays and contactors.

The basic concept of this test controller can of course be applied to more extensive use in other process test and control systems.

Stimulus Capability

The programmable power supplies of the APTE were specially designed to satisfy the stringent time and test requirements of the system. The limited time available for tube testing requires that the supplies achieve the correct output at high accuracy in a short time, and therefore, the overall response characteristics is a critical factor. The combination of accuracy, response time, programming flexibility, wide output range and reliability required an improvement in the state-of-the-art of regulated supplies. Each supply represents a major subsystem by itself—consisting of reference sources, amplifiers, oscillators, power units, accurate resistance-programming matrices, polarity reversal circuits and are protective devices. Some additional features of these programmable supplies are:

- Line regulated,
- Load regulated,
- Output voltmeter,
- Monitor voltage tap (for self-test),
- Current limited,
- Short-circuit protected, and
- Over-voltage protection to 36,000 volts at main output.

Measurement Capability

Except in the breakdown stations, measurement capability is provided by individual measurement preconditioners. All three preconditioners are of the same design but with selective implementation depending on the specific needs of the station. The general features of the preconditioners are:

Input protected to 500 V overload,

Rapid (3 ms) switching between decade scales,

Critical components matched for absolute accuracy and drift with temperature, and

Fast settling time on all scales:

Scale	*Time*
0.001 to .01 μA	50 ms
0.01 μA to 0.1μA	10 ms
0.1 μA to 30 mA	5 ms
0.01 V to 10 V	5 ms
AC: 1 to 10 mV RMS	20 ms

Station measurements are performed by using high-speed, programmable measurement preconditioners. An analog-to-digital converter at the test control converts the DC output from the preconditioner to a 13-bit plus-sign digital word for transmission to the computer. The measurement functions available at the individual stations are outlined below (accurate to within ± 1% of measured value):

	Shorts and Leakage Station	*Cutoff and Emission Test Station*
DC current	100nA to 10mA	1nA to 30mA
DC voltage	—	10mV to 10.0V
AC voltage	—	1mV to 10mV

Breakdown Stations

Two test stations are used to perform 1) the focus breakdown and stray or grid emission test and 2) the anode breakdown and stray or grid emission test on each color picture tube. The stations operate independently with all power supplies and routing logic contained in the station. Up to 15 discrete tube arcs may be recorded. The magnitude of stray or grid emission is also detected if present. The measured value is then represented by 4 binary bits.

Internal logic controls the up-sequencing and down-sequencing of power supplies. Computer control is required only after the test time. The computer receives coded information containing the tube test results and then re-initializes the station for the next tube.

Indicators

Indicator lights and assemblies are located throughout the APTE system to provide a quick visual check on the operating subsystem. A number of the light assemblies are comprehensive enough to aid in trouble shooting.

SELF-TEST CAPABILITIES

Three types of self test or self checking have been incorporated into the design (incidentally providing another example of close and effective work between the hardware and sofeware groups, via the organization specifically delegated the responsibility of maintaining the integrity of the interface). There are on-line self-tests; diagnostic routines; and manually initiated self testing.

On-Line Self-Test

On-line testing checks out the power supplies, preconditioners, ADCON, and signal lines. All power supplies except logic power and 28 VDC units may be monitored for output magnitude and polarity. The DC current scales in the measurement preconditioners, except 1.0 mA to 30 mA, may be individually tested. The 1.0- to 10-mA and 10- to 30-mA scales are indirectly checked. The three voltages decades, 0.01V to 10.0V, may be individually tested. The AC scale, 1 to 10 mV RMS, 1000-Hz, half-wave, may be checked for operability. The analog to digital converter (ADCON) may be automatically checked at a single voltage supplied by the reference voltage standard. Each data word sent to the test complex may be checked for proper reception by use of the ECHO CHECK. An error will cause re-transmission of the word or (after 3 consecutive errors) an error printout is generated. This check insures that the proper test conditions are applied to each kinescope.

Tube Simulator Testing

All supplies that are normally routed to the tube are indirectly checked. Each stimulus and measurement routing relay may be checked and fault-isolated. The arc counter and stray emission detector equipment are checked as well as the power supplies and routing.

Diagnostic Tests

A full system of programmed on-line and off-line automatic diagnostic tests is used for subsystem self-tests. To facilitate the operatoin of the required self-test routines, the APTE hardware was provided with the required test points and switching. Each supply was provided with a special internal tap accessible to system control via self-test select switching. One of the supplies is connectible through system logic to the pre-conditioners for self-test purposes.

For digital self-testing, on-line, an ECHO CHECK feature was implemented by the inclusion of re-transmission circuitry. In particular, a set of gating circuits, selectable by program control, were built into the Test Equipment Controller. To make the actual check, there is also included a bit-by-bit comparator whose output determines the accurate receipt of the transmitted word.

During preventative maintenance periods, off-line manual self-testing can be used to verify the operability and calibration of the measurement preconditioners and to check the ADCON at any reference voltage.

SUMMARY AND POTENTIAL

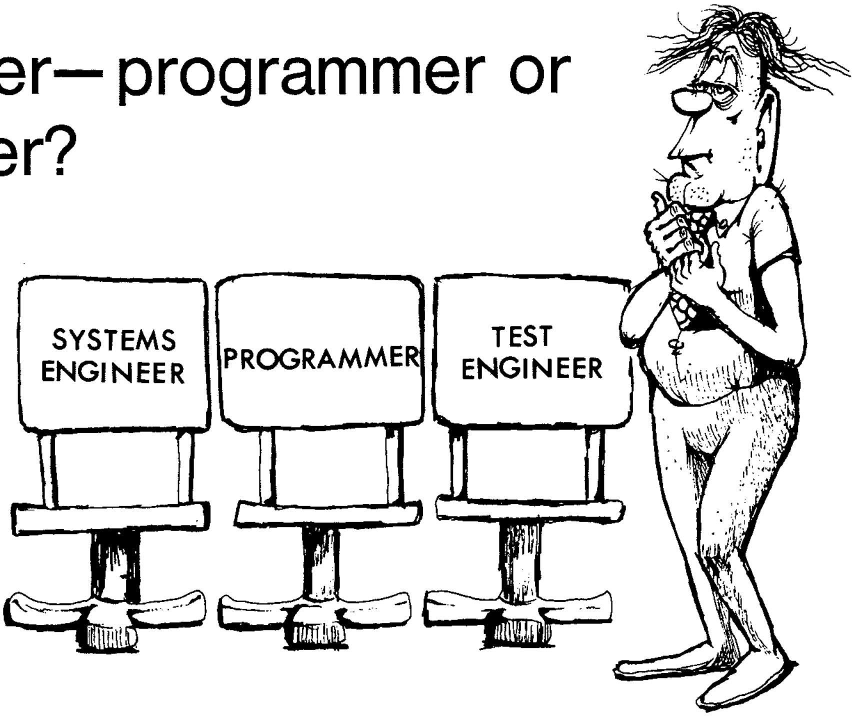
The APTE subsystem development illustrates the applicability of certain system approaches evolved during many years experience in military Automatic Test Equipment. For exmaple, the function of test requirements analysis serves to codify and condense the system performance requirements as specified by the end user. In this case, the systematic allocation of routing channels for stimulus and measurement resulted from such an analysis conducted with the full participation of the using functions. The many requirements for measurements in various ranges were similarly reduced to a logical matrix and implemented by a single design for the measurement device.

This first installation of the APTE system was the design model, the prototype, and the production-line unit all in one. Therefore, many of the design improvements normally incorporated between the prototype and production model have been developed but not yet applied. Since the design and contruction of this first model, there have also been improvements in the state of the art of constituent components and valuable feedback obtained from the operating experience.

ATE test designer—programmer or systems engineer?

F. Liguori

Designing advanced automatic test equipment (ATE) requires equipment designers to conceive and develop systems involving nearly all aspects of electronics from power supplies, to microwave devices to digital computers. Nevertheless, the talents required are fairly well definable and clearly full in the category of electronic design engineering. For each assignment, there is a corresponding need for aptitude, education, and experience. Salient technical requirements and desirable personal characteristics of the ATE test designer are developed in this paper.



During experimental phases of ATE, engineers were taught the rudiments of programming instead of training programmer/mathematicians in the principles of test engineering. Hence it has been customary to use engineers in the task of ATE programming. However, the skills and work habits so desirable for the test designer are not widely found.

The test designer/programmer must be a multidisciplined individual who can bridge test requirements and ATE capability with a test procedure composed of engineering ingenuity and attention to detail. For an insight into the technical requirements of a test design programmer, it is appropriate to look at the nature of his assignments.

Generating and validating programs for ATE can be defined by a functional block diagram containing any number of functions, depending on the level of detail desired. Basically the process reduces to four major functional areas:

1) Test requirements analysis,
2) Test programming and interface design,
3) Program production and verification, and
4) Program validation on the ATE.

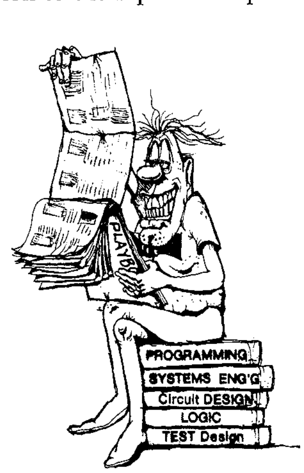
These four functions of the test design and programming process represent the bulk of the effort and cost in the preparation of programs for units under test (UUTs). The functions are generally performed in the sequence given; however, it is not always clear where one operation begins and another ends. The validation task, for example, can require substantial rework involving the other three functions.

The individual responsible for these tasks is variously called a programmer, test engineer, test designer, systems engineer, and so on. Each title is apt but none is exactly correct. He is all of these and perhaps a little more. A brief look at his assigned tasks should help define his role if not his title.

TEST REQUIREMENTS ANALYSIS

This function might also be called preliminary test design because, generally a test philosophy and plan are generated concurrently with the analysis of the test requirements for the UUT. The test plan is usually based on a particular specification, most commonly a design or test specification. For UUTs with substantial field history, test specifications generally exist. For newer equipment, the design specification may be the only authoritative source for test data. Generally such a document contains a section on test requirements and/or maintainability. Sometimes field and depot maintenance manuals are provided for basic information, but these are never adequate in themselves for test requirements analysis and planning.

The test designer/programmer must first interpret and evaluate a wide variety of documentation to extract the important test requirements for a UUT he may never even have seen. To extract essential test criteria from documents prepared by many people for many different objectives (none of which is ATE-oriented) requires a man of many talents. He must be the classical expert who must be allowed to judiciously "break the rules". What makes his task particularly demanding is that each UUT may involve technology quite different from his major area or experience. Thus, one UUT may be an audio amplifier, another a radar IF strip, and still another a digital control network. The UUT complexity may vary from a disposable module to a complete transceiver requiring fault isolation to the replaceable piece part.



A Person of broad technical background

From this, one can conclude that the test designer/programmer must be a

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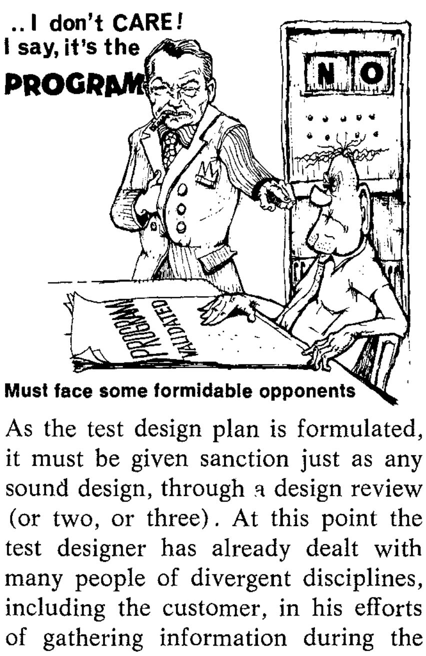
person of broad technical background. But how diversified can one be and still be knowledgeable enough to make detailed technical judgments. Rather than expecting a detailed knowledge of many technical areas, it is more practical to seek a mature individual who can ferret out information and quickly assimilate knowledge in a technology not already familiar to him.

In great demand

The test requirements analysis evolves into a plan for testing the UUT in accordance with its performance criteria and a philosophy of maintenance, hopefully well defined by other documents. Unfortunately, no matter how well-documented the maintenance philosophies, there are necessarily a number of grey areas requiring sound engineering judgment. Judgment implies people, and people imply subjective and often divergent decisions. To avoid this, the test designer/programmer must adhere to certain additional ground rules which evolve through experience in the application of ATE to units and procedures never intended to cope with the special problem of automation. Hence, while the test programmer must be resourceful and must exercise judgment, he must not be a loner who neither communicates with the group nor adheres to rules based on another's design. This is a talent in great demand, certainly not limited to ATE technology.



Must face some formidable opponents

As the test design plan is formulated, it must be given sanction just as any sound design, through a design review (or two, or three). At this point the test designer has already dealt with many people of divergent disciplines, including the customer, in his efforts of gathering information during the test requirements analysis. But now he must face some formidable opponents: ATE hardware designers, customer representatives, and a host of other experts on the battlefield of the design review. Up to now, he has simply been a somewhat annoying information seeker. Now he must present a logical design approach and "sell" many interests. He must defend the design even where specifications must be compromised or hardware designs modified.

Often discriminated against

In the tradeoff between sound test programs and conflicting specifications, schedules, and budgets, the test designer/programmer is often discriminated against since he is last in the long chain of events leading to a complete tactical equipment with maintenance support.

TEST PROGRAMMING AND INTERFACE DESIGN

Upon completing the design review cycle, the test designer returns to the quiet, even-paced function of test programming and interface unit design. Having established a test approach and resolved the most serious specification conflicts, he must formalize the test flow chart. Each test must now be fully defined in terms of stimuli inputs, routing, UUT operating conditions, signal conditioning, parameter measurements, and decision criteria for automatic flow. Here the test designer must complement his basic engineering skill with programming logic and good documentation habits. It is not sufficient that the tests follow logical sequences; the consequences of each alternative in the logic flow must be correctly predicted and accounted for. This is equally true whether programming in machine language, in assembly language, or in a problem-oriented compiler language. Now that compilers are widely used in program generation much of the tedious bookkeeping work is handled automatically, but the need for precision remains.

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received the BSEE from Tufts University in 1957 and the MBA from Hofstra College in 1960. He was employed as a Publications Engineering Group Leader by Sperry Gyroscope Company, was Department Head for a technical proposal group at Epsco, Incorporated, and was a Senior Engineer and Assistant Technical Coordinator for General Communications Company. Since joining RCA in 1962 as a Senior Member, Technical Staff, Mr. Liguori has been involved in test designing and programming for various general purpose automatic test systems, including MTE, LCSS, and DIMATE. For the past two years he has been a principal contributor to research and development studies on advanced programming techniques for the RCA Automatic Test Equipment product line. Mr. Liguori is a licensed registered professional engineer in Massachusetts and is a member of the IEEE.

The outcome of the test designer's efforts in this phase of programming is a problem-oriented, pseudo-English-language flow chart. This flow chart is the product of a systems analysis of the UUT, a thorough familiarity with the test system capabilities, programming rules, and sometimes confused test philosophy. Perserverance and logical consistency are perhaps the most important attributes to add to the test designer's characteristics to achieve a good test flow diagram.

Capable of overcoming insurmountable obstacles

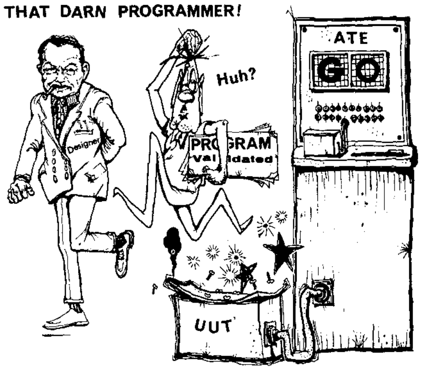
Concurrently with the flow chart design, a design must be generated for interfacing the UUT with the ATE, so that testing can be carried out without adversely affecting UUT performance or requiring excessive manual interventions (or program interrupts). The UUT designed to be tested automatically has yet to be found, so interfacing is no simple task. This is truly a systems engineering problem when all interfaces are considered. Hence the test designer/programmer must also be a competent systems engineer, capable of overcoming seemingly insurmountable obstacles.

PROGRAM PRODUCTION AND VERIFICATION

Once the test process has been defined by a detailed flow chart and interface diagram, a program must be generated for operation on the ATE. The coding task can be handled by engineering aids who translate the flow chart information into series of statements written on coding forms. The extent of knowledge required is dependent on the "software aids" available to translate and/or compile programs written in problem language. In any case, the test designer/programmer must monitor the coder's work to ensure faithful translation. This requires close attention to details, for the test designer is ultimately responsible for all aspects of the program.

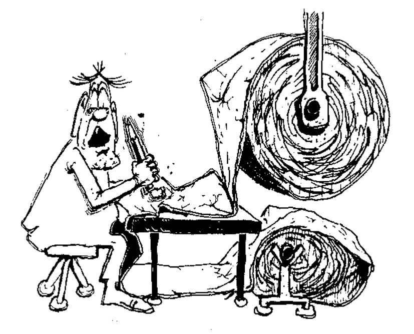
PROGRAM VALIDATION ON THE ATE

THAT DARN PROGRAMMER!



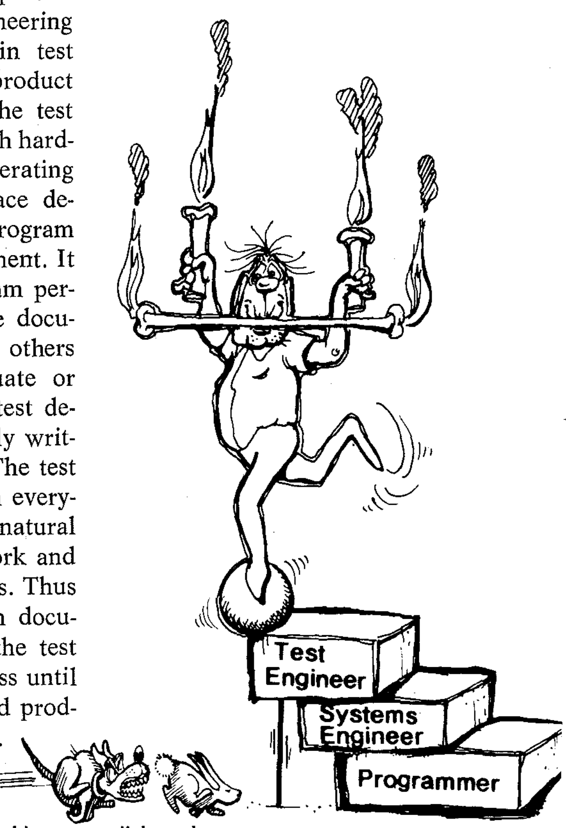
Not infallible

All steps involved in producing a test program ultimately lead to trying the program on the ATE with the UUT connected. This validation effort is undoubtedly the most exciting aspect of the test designer's job. Up to this point the task has involved paperwork alone. Now the test programmer operates the ATE system for substantial periods of time. There is a great deal of pressure because of the great demand for ATE system operating time. The test designer must remain calm despite the schedule pressures, interruptions for demonstrations, equipment failures, UUT problems, interface adapter problems, and software-aid debugging. Again, the systems aspect of the job prevails in that the test programmer must resolve problems among the many possible trouble areas. And, of course, his own program contributes to the problems for he is not infallible, either.



The product line is paperwork

Finally, the test designer must be a capable technical writer who practices good writing habits throughout the test programming process. Clear, precise writing is essential in all engineering endeavors, but especially so in test programming, for there the product line is paperwork. Although the test designer is actively involved with hardware when analyzing a UUT, operating the ATE, and designing interface devices, his major product is a program recorded in a test design document. It is not sufficient that the program perform well. Clear and complete documentation is required to allow others to continue his efforts, evaluate or modify the program. A good test design document cannot be hastily written at the end of the project. The test designer must make writing an everyday habit so that it becomes a natural means for guiding his daily work and communicating results to others. Thus he will develop his test design document through each phase of the test design and programming process until it becomes a finished and tested product like the validated program.



Capability for achieving some admirable accomplishments

SUMMARY

In summary, the test designer/programmer can be considered basically a systems-oriented test engineer, with some programming experience and technical writing ability. He must also have certain personal characteristics such as self-direction, persistence, attention to detail, adaptability to new problem situations and, above all, a capability for achieving some admirable accomplishments under severe handicaps.

Many engineers cannot take this type of work for long—others thrive on it. Test programming is a very real engineering task even though it is practiced by a select cult. To accomplish its tasks effectively this group must first consist of competent engineers and must enjoy the full support of managers who appreciate the importance of the test design and programming task.

ACKNOWLEDGEMENT

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J. D. McCready for the artwork.
L. Tritter for editorial services and constructive criticism.

Evolution of automatic testing for color picture tubes

W. E. Bahls

The introduction of a new advanced technology (such as computer-controlled testing, data acquisition and analysis, and control) into a functioning organization presents many difficulties.[1] For such an undertaking, it would appear desirable to develop and check out all new features separately and then gradually assemble them into an operating system. This procedure, however, in the case of the color-picture-tube system to be discussed would have been impossible because many of the features of the new system interact with, and depend upon, the production system.

THE FOLLOWING STORY is a time-sequential narrative of some of the background leading up to the establishment of the color-picture-tube project, the organization for accomplishment, and the steps and timing of accomplishment. It also provides an overview for the following papers which describe the system and some of its elements in more detail.

BACKGROUND

The potential of the computer for testing and process control was recognized early. In 1953, the first proposal of this nature was made, but, at that time, there was much skepticism about such an approach. However, in 1956 the Automation Systems Development activity was established, and one of the first projects undertaken was a computerized design-check and quality-control system for receiving tubes,[2] part of which included a digital-control automatic test set known as STAR (special tube analyzer recorder). This system was developed and introduced during the years 1957 to 1959. During 1960 and 1961, several studies and proposals were made to extend computer control systems into factory testing and process control, one of which was for the picture-tube activity. At that time, major investments were being made in the development of color picture tubes. Color-television sales were low, and there was a question as to whether production processes were ready for this refinement.

By 1962, the color-television demand significantly increased, and, as a result, additional studies were made as to the possibility of computer-controlled testing and process control. In May of 1963, the top management of what was then the Electron Tube Division recognized that it was largely the quality of the color picture tubes which finally convinced people that color television had been perfected and which, in turn, resulted in their willingness to buy. Management also recognized that during a period of expanding production when new factories, new equipment, and new people were being introduced, it is very difficult to maintain a high quality level, but that this level must be maintained. As a result, a survey of the entire production and quality-assurance systems was requested to pin-point particular areas that would require specific attention. It was also indicated that the time was suitable to utilize computers more intensively in the production operation, and that specific recommendations should be submitted as a part of the survey report.

During June and July of 1963, the survey of process control and quality assurance was conducted and the report and recommendation of this survey were submitted July 11, 1963. Several projects were proposed, one of which was on-line process-data acquisition with automatic computer-controlled testing of finished product and on-line data analysis and correlation. This proposal appeared promising and it was agreed that it be studied further and that a more detailed definition be developed.

PRELIMINARY STUDY

Because the envisaged system involved and impinged upon many activities, a project study team was proposed which consisted of representatives from the various activities involved. The team

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received the BSEE from the University of Nebraska in 1929. He was employed at Westinghouse Research Laboratories in Pittsburgh investigating gaseous conduction and photo emissive phenomena and devices, during which period he did advance study in math and physics at the University of Pittsburgh. In 1937, he organized the Special Tube Engineering Department at RCA in Harrison, N.J. He was awarded the Alfred P. Sloan Fellowship to M.I.T. in 1941 and received the MS in Business and Engineering Administration in 1942, after which he joined the Sales Department in Camden with responsibility for Product Control (now Marketing) for all tube products. In 1945, when the Tube Division (the forerunner of Electronic Components) was formed, he became Staff Assistant to the Vice President of the Division and later Administrative Assistant. In 1953, he was a member of the special project team appointed by then President David Sarnoff to prepare the appeal to the Federal Communications Commission for standardization of compatible color television. Following a special project for process and quality improvement, he was named Administrator of Product Engineering and Advanced Development for the Tube Division. He started his direct association with electronic computers in 1956 when he organized the Automation Systems Development Activity which was the forerunner of what is now the Management Information Systems and Services Activity of which his present function is a part. He is a senior member of the IEEE and a member of a number of its professional groups. He is also a member of the Institute of Management Science (TIMS) and is a past president of the New York Chapter.

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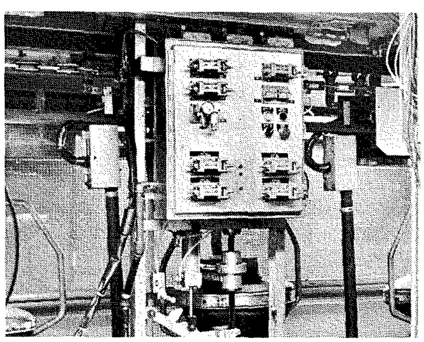
was activated in October of 1963. H. R. Seelen placed the project responsibility under the Quality Control activity with F. C. Fryburg as the specific project director. Members of the project team were selected from Engineering, Equipment Development, and Production Operations at Lancaster and Marion and from Advanced Automation Systems Development (now Computer Control Systems) at Harrison. Because the Electronic Components personnel did not have the necessary experience in the design of computers and digital controlled hardware, this matter was discussed with Dr. J. Hillier of the Princeton Laboratories and C. A. Gunther of DEP Engineering. As a result of their recommendations, R. E. Schrader of the Princeton Laboratories and N. B. Wamsley of Aerospace Systems Division (ASD) at Burlington joined the preliminary study team. The Burlington activity had been building automatic checkout equipment for military purposes since 1955, and therefore had extensive experience in this area.

By the middle of Febraury 1964, the preliminary study team concluded that a system for electrical testing and process analysis could be developed immediately and, therefore, recommended that a full-time project team be established to define specific objectives. The team also concluded that the so-called subjective areas which involve color purity and white uniformity would require a long study and experimentation period and, therefore, were not included in the proposed first project.

PROJECT DEFINITION AND APPRAISAL

At this time, it was decided that should this project be introduced in the factory it would probably be at the Marion Plant first and that, therefore, this location should be the headquarters for the project team with representation from the Marion Engineering, Equipment Development, and Manufacturing Operations. A study contract was signed with ASD Burlington to provide digital equipment design assistance, and D. M. Priestly was assigned as the ASD representative. The project team held many meetings with engineering, operation, and quality-control representatives to establish the general systems concepts in detail and, at the same time, to approximate the costs and benefits associated with such a system. After a month of continuous effort, the skeleton system and preliminary cost estimates were developed for presentation to the operating organizations at Marion, Lancaster, and Harrison.



One of the technical challenges that faced the project team was to reduce system noise. This was accomplished, in part, by using pneumatic switching throughout.

During this period, the team was faced with a dilemma. With the rapid growth of color television, additional production facilities were required and plans were being made for a major expansion at the Marion facility. However, a Board Grant Request had to be prepared for the facilities needed, and funds were to be included for the computer-controlled test and analysis project. Because there were no details on system design nor its precise cost, the facility funds had to be requested with very preliminary estimates.

At this stage, the full-time project team was expanded for the purpose of preparing detailed system specifications. The contract with ASD at Burlington was extended to allow preliminary design of the digital test hardware. F. U. Everhard was assigned to head the ASD representation to the project team.

A period of detailed system-requirements definition and agreement on areas of responsibility followed. As meetings were held with engineering and operating personnel, the functions desired to be performed by the system continually expanded. The systems technical requirements took on specific form, but the scope was much broader and the degree of accuracy, repeatability, stability, and the like that could be agreed upon was much higher than originally contemplated. It was also apparent that the cost was far in excess of what had originally been contemplated and considerable debate ensued as to whether the requirements should match the available funds, or whether all proposed requirements should be satisfied and additional funds then requested. The project team chose the latter approach.

Because the ASD portion of the project increased, ASD shifted the responsibility for its effort to its Project Management Office. Consequently, N. A. Teixeira became the ASD local project manager, with E. D. Wyant having the specific equipment design responsibility.

During the requirements definition phase, ASD project representatives prepared two documents in November 1964. One, known as the "Technical Requirements" statement, outlined the functional objectives of the system. The other document, the "Statement of Work", outlined the work assignments between ASD and EC. However, when approval presentation started, it became apparent that the system, in its expanded form, would have to be revised to bring it in line with the available funds

PROJECT REDEFINITION AND APPRAISAL

As a result of limited funds, some of the proposed system functions had to be sacrificed. At the same time, consideration was given as to whether EC should assume some of the functions originally contemplated for ASD.

Several revisions in the "Statement of Work" were prepared until the "Technical Requirements" and the preliminary cost figures were within the funds available. Then, ASD in Burlington was authorized to proceed with hardware design engineering and the procurement of long-lead-time items. In the meantime, a formal quotation for ASD work assignment specified in revision IV of the "Statement of Work" was submitted. The technical requirements for the system as agreed upon at that time were substantially those of the system as finally installed; only minor modifications were introduced during the design and construction period. A description of the system functions is the subject of another paper in this series.[3]

PROJECT ORGANIZATION

As a result of the revisions, ASD would no longer procure the computer nor develop the operating software system. These responsibilities were assigned to the Advanced Automation Systems Development activity (now Computer Control Systems, Manage-

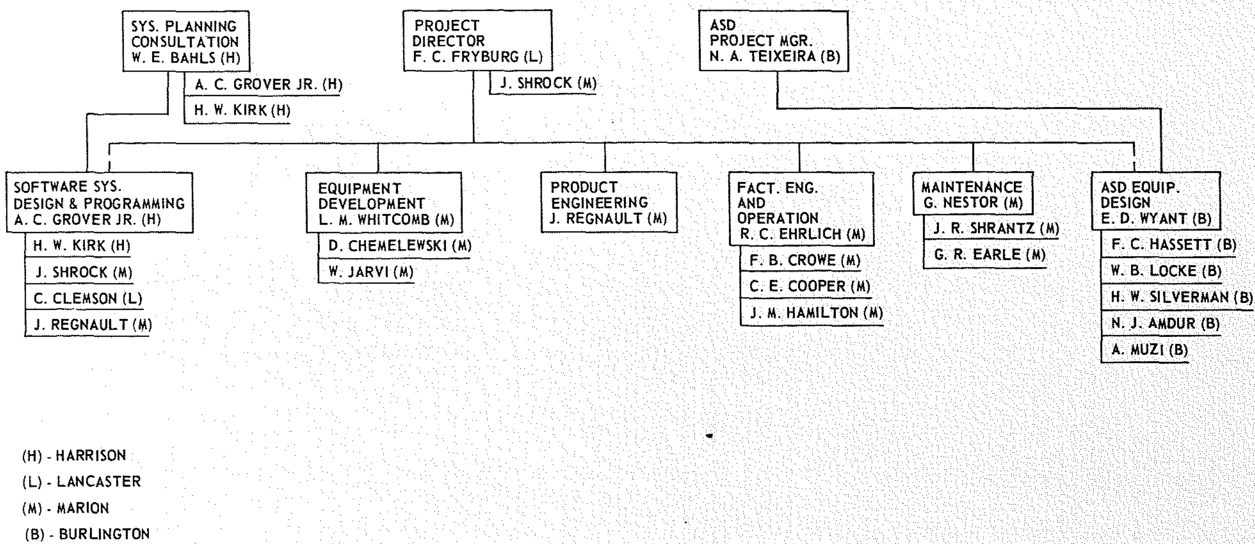


Fig. 1—Project team organization.

ment Information Systems and Services) at Harrison. The computer complement selected, the software operating system evolved, some of the problems encountered, and some of the techniques of solution devised are covered in another paper of this series.[4]

The new ASD responsibility included design and manufacture of the computer interface and all test and measurement stations, in addition to supplying necessary control and measurement signals to contacts at the test stations. ASD would also supply the input card-read station and an output defect-and-data-printing station.

Some of the interesting problems encountered by ASD during design of measuring equipment, which was required to read in the nanoampere region, with applied voltages of kilovolts, in an electrical noisy factory environment, and at a speed of milliseconds per measurement, are the subject of another of the papers in this series.[5]

The development of all the mechanical conveying, contacting, tube-marking, and similar equipment with its associated electrical controls and interrupt signals as well as arc and stray-emission counters, mechanical card punches, card-read actuation, and the like was the responsibility of the Marion Equipment Development activity of the Television Picture-Tube Division. This activity also had responsibility for installation of equipment.[6]

The project team organization as then constituted is shown in Fig. 1. In addition to the two hardware-development groups and the software-development group, a tube engineering representative was assigned for liaison with the product engineering activity and, subsequently, for test correlation work when the equipment was installed and became operational. Factory process engineering and operation representation of course was necessary. Also, because this equipment was to operate on a three-shift basis, operators were needed and had to be trained for each shift. Finally, maintenance of the equipment would be an extremely important item, and, therefore, representation was necessary from the maintenance activity. Also, maintenance technicians would have to be on duty for each shift and would require training. ASD-Burlington assumed the responsibility for training personnel of the project team for the operation and maintenance of the hardware. Similarly, the Harrison Computer Control Systems activity took on the software training. Because of the time schedule involved, it was decided that most of the training be on-the-job. As soon as the computer had been selected, some of the project team members from the software-design group, product engineering, and the factory engineering operations group attended a two-week programming school for the new computer. At the same time, the maintenance personnel and one of the members of the Marion equipment-development team attended a three-month computer maintenance school. As soon as the Marion and Lancaster representatives completed their programming school, they were assigned work with the software team so that they would be thoroughly familiar with the systems concepts and obtain actual programming experience by writing a system subroutine.

When the equipment-development and maintenance representatives had completed their computer maintenance school they, along with another engineer from Equipment Development and the head of the operation group, were given their next assignment at Burlington to work with the ASD Design Group. This group did most of the computer programming to check out test hardware, while they also learned the details of the ASD test hardware design and assisted in the engineering check out.

Development, Design, and Construction

The development and training programs were carried out as planned. During development, design, and construction, numerous coordination meetings of the whole project team were held. Additional requirements were introduced and some problems were encountered which necessitated several technical directives to change the "Technical Requirements" as well as the "Statement of Work." Periodic Design Review meetings were held at which all activities reported on design progress to date and discussed problems.

Acceptance, Shipping, and Installation

After the final check-out runs and acceptance tests were conducted at Burlington, the equipment was shipped to Marion, Indiana. Several design problems still existed with the equipment; however, these problems were left for solution at the Marion facility. Upon arrival, the equipment was installed at the plant and checked out by rerunning the acceptance-test programs. During this period, the ASD project members lived at Marion to participate in the system integration and to solve some of the final design problems of the ASD equipment.

Integration and Testing

An intensive period of system integration was conducted under adverse circumstances. The expansion program of the Marion plant was in progress. Therefore, the new test equipment was located in a new section of the building not yet completed. Various integration and debugging activities had to telescope and had to be conducted on a three-shift basis in an attempt to meet the schedule.

Project direction during this period was difficult and management decisions had to be made quickly, often without authority and responsibility for them having been clearly established. As system problems were encountered, schedules had to be modified quickly.

Integration of the equipment was conducted in two major phases for minimum interference with production. In the first phase, the portion of the conveyor system associated with testing was closed into its own loop. This arrangement made a separate conveyor which was bypassed by the aging conveyor. Static tests were first performed in each test station and later dynamic tests were conducted with the conveyor operating so that hardware and associated computed programs could be checked out together. For the final phase of integration, the test loop and aging loops were opened and tied together into one continuous loop.

After each test station had completed static check out, engineering evaluated the system performance and correlated it with manual equipment during the first phase of integration.[7]

Integration and correlation work took over twice as long as had been expected originally. The number of design problems encountered was not substantially greater than had been expected, but the time to correct them was longer. This extension was partially caused by interference from plant construction and other factors not directly associated with this project.

Operation

The system was phased into partial operation at an early date. As soon as the dynamic tests were completed on the closed test loop, one shift was allocated to operational testing. Toward the final phase of integration, operation testing was increased to three full-time shifts.

After the integration was completed, the system was placed on full three-shift parallel operation with the manual test system. Parallel operation permitted direct comparison between performance of the two systems, and allowed operating and supervisory personnel to become acquainted with the new system.

Pilot-production phase followed the period of parallel operation. The automatic test system then became the authority for all electrical testing and only tubes which passed it were sent to the manual test stations for final subjective testing only. The experiences encountered during installation and integration and the performance of the system are the subject of the last paper in this series.[8]

As the integration work progressed, most project team members who had design responsibility returned to their former duties when their work was completed. The Marion equipment-development group, however, remained active to handle the system design modifications. When the system advanced to the pilot-production stage, the operating and maintenance personnel were shifted from project management to the plant operating organization and have been reporting to J. R. Shrock who, in turn, is under S. M. Hartman, Marion Plant Manager.

SUMMARY

The development of an acceptable plan and schedule for a major system modification into a functioning organization was a lengthy one. Actually, a year and three-quarters elapsed from the original suggestion of the Marion automatic test system until an approved program was established. The various steps of design, construction, integration, and operation of the system and their phasing have been discussed. A project team was established whose only responsibility was the introduction of the system. Accomplishment took nearly half again as long as scheduled, but many of the delays encountered were unrelated to the project.

ACKNOWLEDGEMENTS

Many of the participants in this project are mentioned by name and their contribution is thereby acknowledged. In addition, however, there are hundreds of persons who participated in the planning, construction, and integration phases without whom it could not have been accomplished. Thanks must also be accorded to all levels of RCA participating management for their support of a development project conducted under very trying circumstances. Finally special acknowledgement must be accorded to F. C. Fryburg for the long hours of unstinting effort that he put into the project management.

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Problems of integrating a complex automated test system

F. C. Fryburg

A major change in the processing and/or testing of a mass-produced product requires very careful planning from the early stages of system design through the final stage of pilot operation. This fact has been emphasized throughout the development of the Automatic Production-Test and Process-Control System at the Marion Color-Picture-Tube Plant in Indiana. Previous articles in this series have covered basic system planning and the design of the major system components for both hardware and software. This article will deal primarily with the various phases of system integration.

THE AUTOTEST SYSTEM INSTALLATION in the Marion plant was complicated by two major factors. First, the Marion plant was involved in a major facility expansion of some forty-eight million dollars which included new buildings and new production equipment. Installation of the autotest system was therefore faced with problems of timing and manpower availability because the over-all production expansion had a higher priority. Second, an earlier decision had been made that the hardware of the system would become an integral part of the final tube-processing conveyor. However, the integration would be most complex and almost impossible to accomplish while production was sustained; therefore, a separate test loop was constructed. This loop was tied into the main conveyor over a normal weekend shutdown without any significant loss of production.

INTEGRATION

The most significant problem stemmed from the fact that the autotest system was designed and built as three separate components (computer-test complex, mechanical-electrical interface, and software subsystem) each at a separate RCA location. In addition, the early testing and debugging of each component was carried out at those separate locations under laboratory conditions. These conditions were not as adverse as the high-speed, high-noise (electrical) environment of the production area in which the system was to be finally located.

Static Testing

Once the installation was underway, static testing began. This testing required that the computer and its two major interfaces (its two major interfaces are several hundred feet away from each other) be completely wired in and checked out. Then, as each of the seven stations was installed and tied into test control, both the station and its related software were checked out.

Because the software was designed for real-time operation, it was not immediately adaptable to this type of testing. Thus, special programs were written which simulated major functions of each segment of the main program, but which enabled the computer to queue and print input and output between the computer complex and the test-system complex. Through this approach, many minor hardware problems were detected and corrected. In addition, the task of program testing and debugging was greatly simplified because the software logic was tested without the complexities of the conveyor movement.

Dynamic Testing

This phase introduced for the first time the movement of the conveyor with the mechanical carriages used for the five test stations. The problems associated with the interrupt timing were of immediate significance. Much time was spent in adjusting the mechanical interactions which generated the seven main interrupts of the timing sequence and in providing adequate protection for these interrupt signals from the many sources of electrical noise.

The other portions of the dynamic testing of the hardware and software were less complex than anticipated. This situation resulted from the effectiveness of the static testing phase which preceded it. In addition, the technical personnel who monitored the operating test complex became quite adept at detecting both hardware and software problems. This quickly developed skill was greatly aided by the extensive number of visual indicators designed into the test complex by Aerospace Division personnel.

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Test Correlation

Testing of hardware and software was by no means the only major task of integration. It was equally important, and nearly as complex, to establish correlation of test results among the autotest system, the manual factory test equipment, and the television receiver. Several characteristics of the system contributed to the complexity of this task, as described below:

1) *Fast test time:* Increased test speeds were essential to handle the full production output of the final processing conveyor and, thus, to maximize the return from this major investment. In some cases, this requirement called for major redesign of existing tests; in others, it meant careful analysis to insure that both the tube and system were fully stabilized for the required test conditions before measurements were to be made.

2) *Noise:* Two major sources of electrical noise had to be nullified. One source was generated by the electrical interface between tube and system when the tube was moving during testing. The second source was generated by nearby high-voltage processing equipment. The effect of either of these sources would have been a major deterrent to the successful test correlation.

3) *New tests:* The design of the system, in terms of flexibility and speed, introduced many tests which were previously made only under laboratory conditions. Because these new tests were not available with the older test equipment, correlation between the two systems was a complicated task.

The emission-current cutoff and the emission tests were correlated first. This correlation was possible because the equipment problems were solved early, and the equipment modifications necessary to effect accurate tests were completed by the time installation was completed. The gas test also required hardware changes because the necessary low current levels (nanoamperes) were adversely affected by the same noise until adequate shielding was incorporated.

Because the forty-two new leakage tests included many tests that were not previously performed by the factory, extensive correlation work was required. Finally, the fact that the sensing devices of the Breakdown Stations failed to correlate necessitated their complete redesign.

Process Monitoring

Another major task was the evaluation of the system as a process monitoring device. For years, tube test results have been used to evaluate the performance of key processing equipment. This manual data-collection and analysis system was replaced with a computerized "Condemnation Report" which could result in a much greater reliability in tube evaluation. Therefore, it was necessary to insure not only that the process data were being accurately recorded and supplied, but also that the computer programs were properly processing and summarizing this data. In addition, it was necessary to establish good correlation between the condemnation reports and the maintenance results on the condemned equipment. Presently, much progress has been made in this direction.

PILOT OPERATION

As the integration progressed, plans were developed toward a full pilot operation. The first step was to tie the test loop into the main conveyor. This step would effectively lengthen the test conveyor four-fold; however, the test loop was tied in without any significant delays in production.

The second step initiated three-shift parallel testing, that is, the factory testing continued as before even while Autotest was in operation. This arrangement continued for a period of several months. During this period, the final phases of test correlation were completed. After most significant problems were eliminated in the Autotest system, a full pilot operation was initiated. Through careful indoctrination of supervisory and hourly personnel, this phase was an immediate success.

SYSTEM RELIABILITY

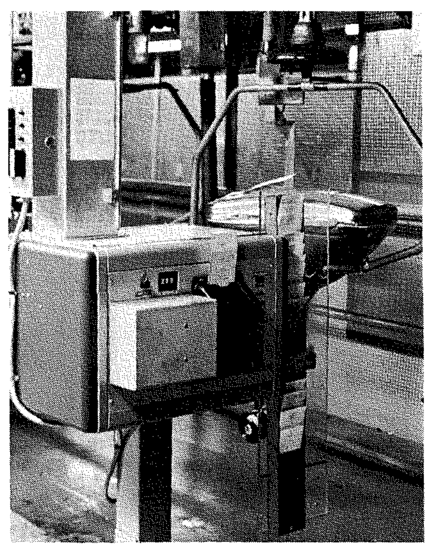
Because the Autotest sysem is an integral part of the final processing conveyor, excessive downtime cannot be tolerated. Even a short downtime could cause the color picture tubes to back up within the production plant.

With the old system of many manual test units, a faulty unit could be placed temporarily out of commission with no adverse effects on the production flow. Also, the failures were not too frequent because fault detection was limited to the periodic calibration of each test unit or a condemnation by the supervisor based on comparative test results from the other test units.

Through an extensive system of on-line self-testing at frequent intervals, the Autotest system is maintained at a high level of accuracy at all times. Whenever a self-test fails, the system is shut down for immediate repair. This arrangement places a great deal of burden on the system and the maintenance personnel.

While the various phases of integration and pilot operation were progressing, much time was devoted to the system reliability. During the early phases of dynamic testing, pre-pilot runs were started as a full-time, third-shift function. Pre-pilot runs were accomplished with continuous testing and retesting of a group of tubes with known characteristic.

Through this approach, early information on reliability was obtained and corrective action was implemented. Thus, from the early phases of integration, there has been a program of continuous evaluation of system reliability. As a result, three primary types of hardware modifications were effected: 1) more reliable components and sub-assemblies were secured, 2) improved protection circuits were developed, and 3) the time required to replace faulty components and sub-assemblies was shortened through mechanical improvements. In addition, an extensive series of off-line diagnostic programs have been developed to reduce the time required to isolate system failures down to a level of sub-assemblies and components. Finally, the



Card readers, similar to that shown in the photo, are used for tube data entry. They accept a standard 12-row, 80-column punched card.

early initiation of pre-pilot runs helped to uncover some real-time software problems. Without this early detection and solution phase, software debugging would have taken longer.

PROJECT STATUS

The long-range objective of the initial plan was to develop a device which would improve outgoing quality of color picture tubes through more accurate and consistent testing. Presently, there is little doubt that this system has achieved this objective. Through test correlation, the superior accuracy of the system has been clearly established. Because of the extensive on-line self-tests of the system, the calibration and, therefore, the testing consistency of the system are guaranteed to be far superior to those of any known picture-tube test equipment. An accurate evaluation of how much the autotest system will improve outgoing quality is yet to be made. This evaluation requires an extended time period of analysis in the customers' plants and in the field.

LONG-RANGE POTENTIAL

The automation of comprehensive testing, statistical analysis, and process condemnation functions provided a new level of tube quality on color picture tubes, which have been called "the most complex component ever mass-produced". Because each tube is tracked throughout its processing, data are available for the computer to condemn equipment which is producing repetitive defects. Thus, the process equipment can be adjusted or repaired by operating personnel at the earliest known time. Through on-line statistical analysis of variable test results both by tube class and by processing equipment, it is possible to provide Production Engineering with "trend warnings" which will permit them to make equipment adjustments before "epidemics" develop. Finally, subtle defects in tube processing may also be discovered through provisions which have been made for subsequent off-line statistical analysis of the process and of the variables test data stored on magnetic tapes. Thus, an important feedback path has been illustrated.

As the system develops a body of statistical data, information is gathered to improve the process, the system design, the tube design, and testing methods. Although the system was designed for production testing, it is of considerable value in the pilot-run testing of new or developmental tubes because of its ability to provide consistently derived test data and analysis on a large sample of a test run. This same attribute provides a self-improvement loop to the system because test results of large samples are necessary for the improvement of the tests themselves in terms of parameter choice, setting of limits for specifications and quality control, and correlation among test parameters, measured variables, and failure symptoms. It is expected that such test refinements will lead to precise detection of trends in process deterioration while the output of the process equipment is still within the quality-control limits. The present testing is such that the quality-control accept/reject band may be set much tighter than the present specification limits or customer requirements.

These improvements support the main objective of this test system. A good part of the main objective is to improve the quality of RCA color picture tubes.

SUMMARY

As the previous paragraphs indicate, a major task was undertaken and much progress has been made. Although the initial designs of hardware and software were carefully planned and implemented, the integration period unearthed many problems which necessitated numerous modifications. Because of the skill employed in the initial design, most of these modifications were effected through additions or minor changes rather than through major redesign.

On the surface, it might appear that the integration period was too long and too many modifications were required. This belief is quickly discounted when one realizes the revolutionary nature of this system as well as many of its major subassemblies. In addition, it should be recognized that the reliability requirements of this system might likewise be called revolutionary. Continuous twenty-four-hour a day operation, for five or six days at a time, with no scheduled downtime for preventive maintenance is a requirement few commercial computers can achieve. In this system the computer represents only a small portion of the total hardware which must function at this high level of reliability.

Almost from the time installation began, the telescoping of different project phases was initiated. Thus, static testing on one station commenced while installation on others continued. Likewise, dynamic testing began before static testing was completed. The arrangements were possible because the project team operated in three groups, each on a separate shift with different tasks assigned.

Although this approach might appear to be both logical and simple, it offered many complexities and pitfalls. First, because more than one shift might be working on a specific part of the equipment, although performing different tasks, careful documentation of each test run and each modification was essential. Second, problems sometimes developed which made it necessary for the team of one shift to work well into the next shift before a solution was found. In some cases, the subsequent shift actually took over and solved the problem. It is a tribute to the dedication and capability of all of the engineers, programmers, and technicians involved in the integration that this phase was successfully completed on a three-shift basis in less than two years. In addition, it is a tribute to the men of Aerospace Division in Burlington, Management Information Systems in Harrison, and Marion who were responsible for the hardware and software design which needed little redesign during integration. Undoubtedly, the early emphasis on long-range flexibility of system design was a major factor which minimized its redesign.

ACKNOWLEDGEMENT

To J. R. Shrock (Marion), Manager, Systems Engineering, I offer my sincere appreciation for his various contributions. The potential of the Automatic Production Test and Process Control System for color picture tubes has been firmly established. The degree to which this potential will be realized and to which this system will provide the basis for improved process control throughout the plant will depend upon the insight and continued dedication of Mr. Shrock and the nine Engineers, Programmers, and Technicians who comprise his permanent organization.

Integrating an automated system into a high-speed production process

L. Gillon
S. M. Hartman

In any high-speed production facility, a major change in processing or product testing can be successful only if extreme care is exercised in both the design and integration of the proposed change. This fact particularly applies to the integration phase because the change must have little or no adverse effect on the volume or quality of the production output.

THE DECISION to incorporate automatic testing system for color picture tubes into the Marion, Indiana plant did not result in a totally new concept of picture-tube testing. On the contrary, the incorporation of automatic testing might properly be called a natural evolution.

BACKGROUND

It was in the mid-1940's that the first Universal Test Set for black-and-white picture tubes was developed. This set was capable of making all electrical and subjective tests on all black-and-white tube types. In recognition of the need to remove from the operator the decisions which sometimes resulted in improper and/or incomplete testing, to reduce the variables caused by large numbers of testers and test equipment, and to increase test rates, Marion engineers developed the black-and-white Auto Tester, Model M2707AJ (Fig. 1) in 1957. This equipment has the capability of handling fifteen picture-tube categories representing more than 250 tube types. Most electrical tube characteristics are tested on a GO/NO-GO basis. In addition, a subjective evaluation is made by an operator while the tube is moving along the test conveyor.

As is the case of black-and-white picture tubes, the introduction of the color picture tube was accompanied with the development of a manual test set. The manual test set could test all color-tube types and perform all electrical and subjective tests, as did its black-and-white forerunner. The disadvantages of manual testing which led to the development of the black-and-white auto-tester were equally applicable to color-tube testing. In fact, the need for an automated system of testing color tubes was more severe because of the more critical nature of color-tube characteristics. This critical nature, unfortunately, made the task much more difficult to accomplish.

After a number of years of planning, design, and fabrication, an automated color-picture-tube tester was delivered to the Marion plant. Among other unique features this system went beyond conveyorized automated testing to provide for *computer control*. Also, maximum effectiveness of the system as both a test vehicle and process monitoring device and minimum tube-handling costs were to be achieved with a decision to use the computer control as an integral part of the final tube-processing conveyor. Any incorporation of a simple testing device as part of an existing conveyorized production process would have been no easy task. However, for a system as complex as this one, the problems were much more severe.

STATUS OF INTEGRATION

In essence, the problem of factory integration resolved itself into three major areas:

1) The integration of the hardware and software into a single smooth-functioning system;

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Marion Plant
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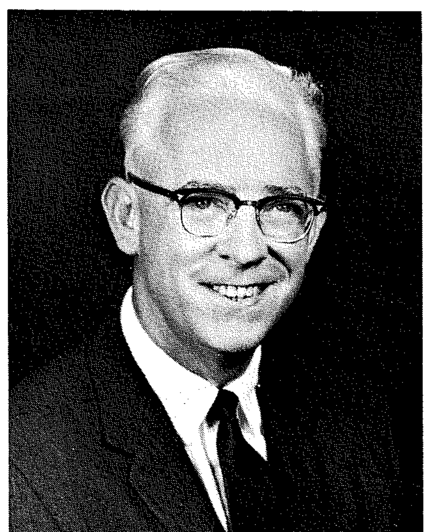
Electronic Components
Marion, Ind.

was appointed Plant Manager, Marion Plant, in September, 1965. Previously, he had been Manager, Tube Manufacturing, at the Marion plant since 1960. Mr. Hartman joined RCA in 1942 as a Machinist at Lancaster, Pennsylvania. He held successive positions at the Lancaster plant as Draftsman; Staff Assistant (Engineering); Section Supervisor; Manager, Equipment Development Group; Manager, Engineering Design and Development. In 1960 he was transferred to Marion, Indiana as Manager, Tube Manufacturing.

Leonard Gillon, Mgr.
Television Picture Tube Manufacturing Dept.
Television Picture Tube Division
Electronic Components
Marion, Ind.

was appointed Manager, Television Picture Tube Manufacturing Department, in September 1965. Previously, he had been Plant Manager, Marion Plant, since 1956. Mr. Gillon joined RCA in 1929 as a machine attendant at Harrison, N.J. In 1940, he was appointed General Foreman of the Miscellaneous Parts Department at the Company's plant in Indianapolis, Indiana, and for fourteen years held successive positions there as Manager, Materials and Production Control; Superintendent; and then Manager, Glass Receiving Tube Manufacture. He received the RCA Award of Merit in 1954, the Company's highest award. Mr. Gillon was transferred from Indianapolis to Marion in 1954 as Manager, Tube Manufacturing, and was appointed Plant Manager in 1956. Mr. Gillon is a Vice President of RCA de Puerto Rico, Inc.



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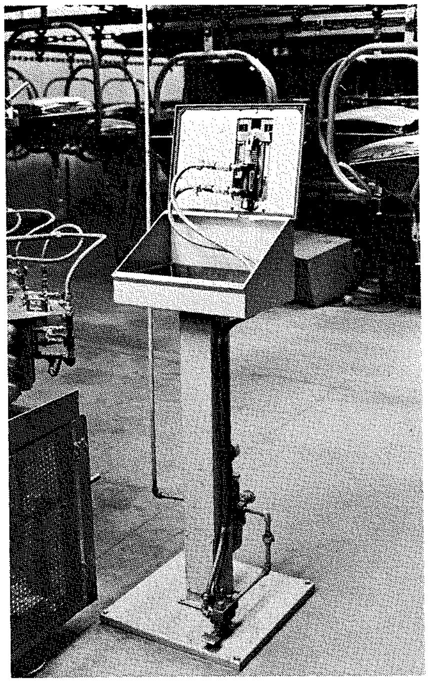
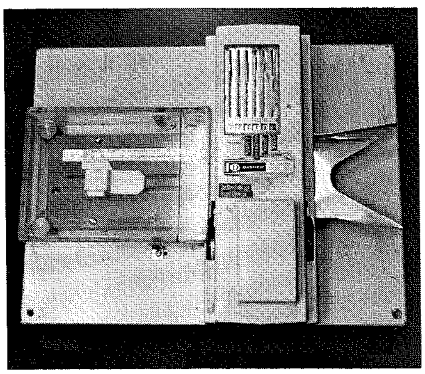
2) The establishment of test correlation; and

3) the establishment of reliability of the process-control capabilities of the system.

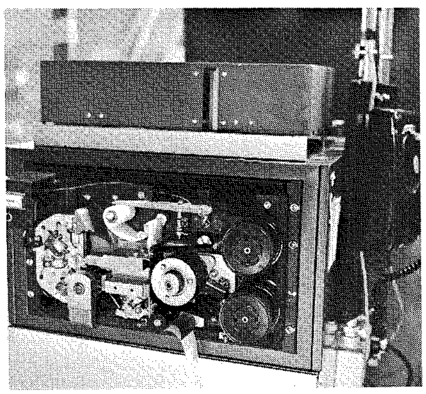
The effectiveness of the system in the production function depended upon its successful completion in all three major areas of integration. Wherever possible, these areas were overlapped to shorten the over-all integration time. With integration of hardware and software completed, the system has been tied into the final tube-processing conveyor with no significantly adverse effects on tube production. As major portion of the tube-test correlation effort has been completed, the testing of a portion of the daily tube production was initiated without any major factory scrap problems. The more detailed process-control capabilities have already provided gains in some areas, while evaluation has continued in others.



Air-actuated card punches are located throughout the factory to record the process history of a particular tube.



Pneumatic card punch mechanism.



At the tube transfer point, a remote printout device prints data for rejected tubes on paper tape.

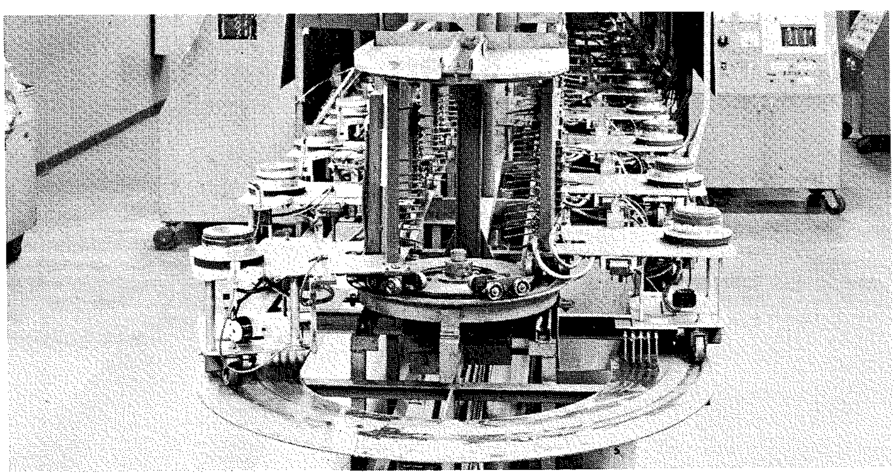
CONCLUSION

During the earlier phases of this project, manufacturing personnel were concerned as to whether this system could ever be successfully integrated into a highly mechanized, high-volume production facility such as the Marion plant. This concern was well founded because at no time in history had such a complex device ever been installed and integrated into a fully operating plant of the Television Picture-Tube Division. With a significant portion of the development and integration now completed, it is important to reflect upon those factors responsible for turning what at one time appeared to be an almost impossible task into one which will soon achieve total success The manner in which the project team was organized was one of the keys to success. From the outset, key personnel were assigned full time to this project. Each man brought with him background and experience which contributed substantially to the success of the system. With respect to accuracy and flexibility, this design has already withstood several major, unexpected problems which were not encountered until integration at Marion.

Cooperation of factory personnel in the training of operators associated with the system has proved vital in the final phases of integration.

Careful planning was one major factor in this program. From the early program phases in 1964, key personnel from several major functions within RCA were brought together to plan the basic system. They carefully planned each major step of the program to insure that every step was compatible not only with the next scheduled step in the project but also with the long-range goals.

Thus, experience with the Color Automatic Production Test and Process Control System has substantially demonstrated that a complex system embodying new test and/or control techniques can be integrated into a high-volume production facility. The experience gained to date, particularlv with personnel selection, design flexibility, and careful planning, should prove invaluable for the design and integration of future systems.



◀ Color picture tube conveyor at the Marion, Indiana plant.

Conveyor adaptation and associated mechanical-electrical devices for autotest

L. M. Clutter
J. F. Stewart
L. M. Whitcomb

The manufacture of color picture tubes involves many different steps such as manufacturing the mask, applying the screen on the faceplate, producing the gun assembly, joining the faceplate to the remainder of the glass envelope, sealing the gun assembly to the glass envelope, and evacuating the tube. The color picture tubes are then taken from different feeder conveyor lines and placed on a central production conveyor. The introduction of automated testing for color picture tubes to an existing conveyorized system introduced many complex problems. This article discusses the most significant problem areas and how they were solved.

Shown in the photo, from left to right, are L. Whitcomb, L. Clutter, and J. Stewart.

Leonard M. Clutter, Mgr., Mechanical Design, Equipment Engineering, Electronic Components, Marion, Ind., received the Bachelor of Mechanical Engineering from Ohio State University in 1949. He joined RCA in 1950 as a specialized trainee and was assigned to the Marion Plant. In 1954, he was assigned to Equipment Engineering as a machine design engineer. Since 1957, he has been Manager of mechanical design in Equipment Engineering with responsibility for design of cathode-ray tube making equipment, specialized laboratory equipment, and mechanical handling. He is a registered professional engineer (Indiana 11632) and a member of Marion Engineers Club.

John F. Stewart, Mgr., Equipment Engineering, Electronic Components, Marion Ind., joined RCA in 1943 as a draftsman designer. His experience prior to joining RCA includes four years with the Metropolitan Edison Co., York, Penna. where he surveyed and mapped rural and urban distribution lines and designed industrial substations. During WW2 he was employed for 3 years by the U.S. Navy in Ordinance work on the design and development of anti-aircraft weapons. While on this project he supervised the writing and preparation of the technical manuals for these weapons. After joining RCA in 1943 he worked in various capacities including drafting and designing of tube manufacturing equipment and shop supervision at the Lancaster plant. In 1952, he was transferred to the Marion, Indiana plant as Manager, Equipment Engineering. Mr. Stewart holds patents on tube parts and processes and manufacturing equipment. He is a member of the Marion Engineers Club.

Leo M. Whitcomb, Mgr., Electrical Design, Equipment Engineering, Electronic Components, Marion, Ind., joined RCA in Marion in 1949. His experience includes five years in instrumentation, with Victor Chemical Works and seven years as a test Equipment Designer with Fansworth Radio Corporation. He is presently Manager of Electrical Design, Equipment Engineering, and is responsible for the electrical design of Kinescope Manufacturing equipment, test equipment and the design of specialized laboratory equipment. He is past president of the Marion Engineers Club and has held office in the Marion Industrial Management Club.

MANUAL TESTING was used before the development of the computer-controlled test system. It was a slow process which involved many operators. Color picture tubes were transferred from the transport conveyor to the aging conveyor (Fig. 1). The operator then connected an aging socket, and the tubes were processed with certain voltages applied to the elements to activate the cathode coating properly and to stabilize emission. When a tube left the aging area, it was conveyed through the manual testing area. The tests were performed at a number of test stations, each manned by an operator. Each operator disconnected the aging socket from a tube, removed the tube from the aging conveyor, loaded his particular test set, and made a complete series of electrical and subjective tests on that tube. The operator then passed or rejected the tube according to his judgement or meter readings. Good tubes were labeled as such and were loaded on the take-away conveyor. Rejected tubes were returned to the aging conveyor for some types of reprocessing or were loaded on hand trucks for other disposition.

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Manual production testing requires many people and many pieces of test equipment, takes a considerable amount of time, and (because of the time factor) is limited to a small number of tests. Consistent and accurate results from these tests cannot be achieved because human judgement is involved and because the test sets are difficult to keep accurately calibrated.

AUTOMATED CONVEYORIZED TESTING

The present conveyorized testing system permits both more efficient and more accurate testing of mass-produced articles than heretofore possible and also provides reduced cost of the testing procedure with improved quality of the manufactured product.

The conveyorized Autotest incorporates testing on an extension of the aging conveyor. The tube carrier has special adaptations which make it suitable for both aging and testing. The tube is loaded onto the aging conveyor from the factory process conveyor (Fig. 2) and it remains there until it is removed for subjective testing. After the tube is aged and prior to its electrical testing, the aging socket is replaced by the test socket and the punched card is inserted into the Data Entry card reader.

Testing is performed on a number of test stations which are located on an extension of the aging conveyor. These test stations are under the control of the stored-program-type digital computer. The system automatically indicates whether a tube has passed all tests and, if not, those tests which the tube has failed.

PRODUCT FLOW

The product flow follows a path similar to that of the manual test system until the tube reaches point *A* of Fig. 3. At that point, the aging socket is removed and the test socket is connected, leaving the tube on the conveyor. A punched card is removed from the face of the tube and placed in the card reader. The card includes such information as the tube class, tube type, tube serial number, and identification of the equipment which took part in the manufacture of the tube. A signal is returned to the card reader from the computer control which indicates that data have been read and entered into storage. This same signal opens the card-reader mechanism. The card is withdrawn and returned to the tube.

The tube continues to move and soon reaches the first test station, which tests for shorts and leakage between elements. The tube is automatically connected to the proper power supplies and measuring circuits through a special contact mechanism. One set of contacts signals the computer to apply the proper test voltages and to adjust the testing specifications for that individual tube, as called for by the punched card which was read by the data entry station.

A tube remains connected to the test station for approximately ten seconds, although the test itself may require only two or three seconds. In addition, the test stations are time staggered along the conveyor to allow the computer the full testing time for one complete cycle.

When the shorts-and-leakage test station completes its tests, the tube receives a proper amount of cathode preheat before it enters the focus-element breakdown station. At this station, the specific voltages are applied to the tube at the command of the computer to test for arcing and stray emission. These voltages remain on the tube for the prescribed length of time, while localized indicating circuits count the number of arcs and the magnitude of stray emission.

When the standard test time is completed, the station signals the computer to receive and store the total count of arcs and stray-emission readings of the tube. The tube continues to travel to the next station for anode-breakdown and stray-emission tests. The tests performed at this station is similar to the focus-position tests; however, different voltages are applied to the tube.

After the tests are completed at this station, the tube travels for a fixed period of time, cooling down before it is preheated for the Phi test station. At the Phi station, the tubes are checked for cathode quality, gas, and faulty high-voltage connections. The

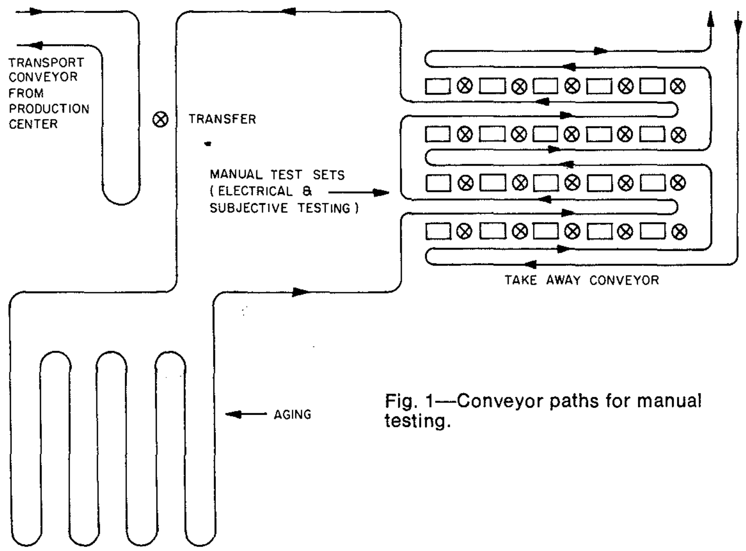

Fig. 1—Conveyor paths for manual testing.

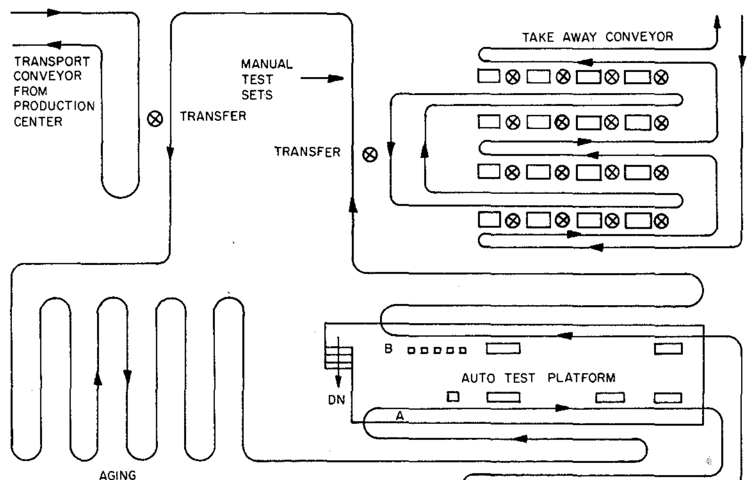

Fig. 2—Conveyor paths incorporating Autotest.

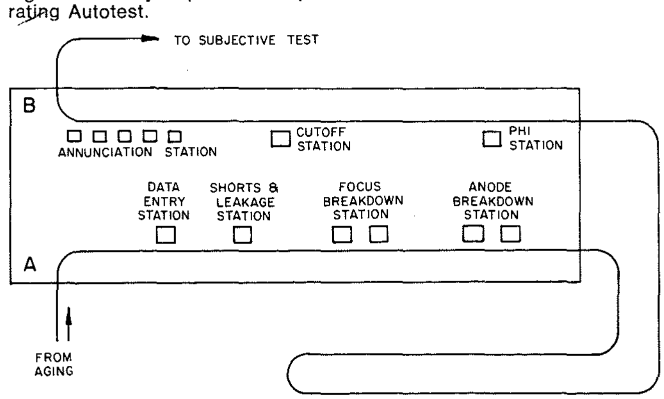

Fig. 3—Product flow path for automatic testing.

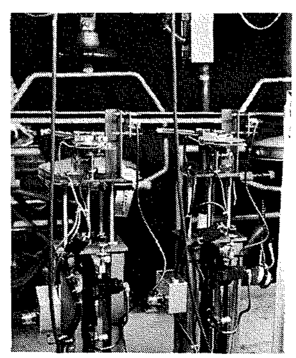

Fig. 4—Color tubes being labeled at the annunciation station.

final test station tests the tube for cutoff, maximum emission current, and filament current.

After all tests are completed on a particular tube—as many as 75 tests—the tube enters the annunciation station. The computer, which has been tracking the tube (as well as all other tubes in the testing cycle) for the entire time, recalls the various testing results and initiates one of several labeling machines or markers (Fig. 4) in the annunciate position. These markers place a label of a particular color on the tube to denote its test-quality status.

The tube continues on the test conveyor to a point where an operator transfers the good tubes to another conveyor which is routed through the subjective test area. In this area, visual tests are made on individual test units by specially trained operators. Good tubes are placed on a take-away conveyor to be painted and packed for the warehouse.

A remote printout device, located at the tube transfer point, prints data for rejected tubes on paper tape. The data are received from the computer and consist of the tube type, tube serial number, and certain defect codes which describe the tube defects. The data tape is attached to the tube to assist in the analysis and reprocessing of the rejected tubes.

TEST CARRIER

The Carrier (Fig. 5) consists of a tubular steel fixture, *F*, which carries the tube. It is insulated from ground by a high-voltage insulator, *G*. Four spring wipers, *B*, which contact the stationary v-shaped bussbars supply voltages to the aging socket. The aging socket, *A*, is a dual unit which accepts both 70° and 90° tubes. All tube elements which receive 0 voltage during the aging cycle are tied together and grounded in the socket.

A specially designed contactor block, *E*, which engages with a mating block at each test-station carriage connects the tube to the test circuitry. A dual 70°/90° testing socket, *D*, is connected to the block with a flexible, shielded test lead wire. Unique switching elements are built into the contactor block.

The carrier is equipped with a transformer, *H*, to reduce the AC buss voltage to the level required for both the aging and test preheat cycle. The socket clamp, *J*, clamps onto the tube neck to hold the test socket in place, and a high-voltage connection, *C*, for the ultor of the tube is used during the aging and test cycles.

CONTACTS

Previous test equipment employed bus bars and sliding contacts to contact the tube under test. Because this type of contact is inherently noisy, it is undesirable to use this system with the extremely small signals being measured on the computer-controlled test equipment. As a result, spring-loaded, silver-plated contact buttons of special configuration were designed (Fig. 6). This configuration has a male contact with a shallow cone-shaped end which matches a concave recess in the face of the female contact. An array of these contacts is installed in molded blocks of high-impact, high-dielectric plastic material. Each carriage and each carrier are equipped with mating blocks.

Another feature incorporated in the contact block, which is mounted on each tube carrier, is the contact spring switching device of Fig. 6, which removes AC filament pre-heating voltage from the tube and substitutes DC filament voltage during the test. A final feature is the generation of a signal at the time the contact blocks are mated together. This signal provides an interrupt to the computer to signify the readiness of the station to test the tube.

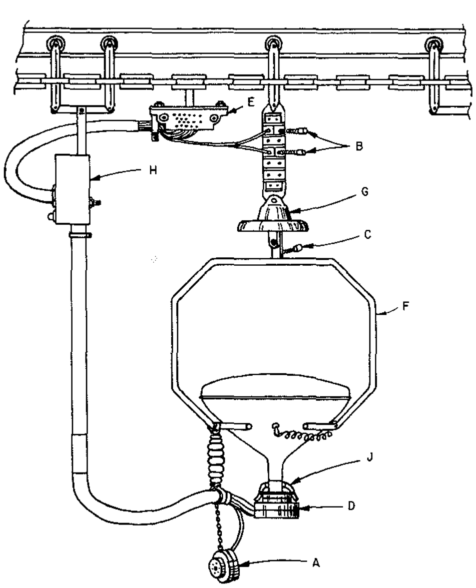

Fig. 5—Carrier for the color tubes being tested.

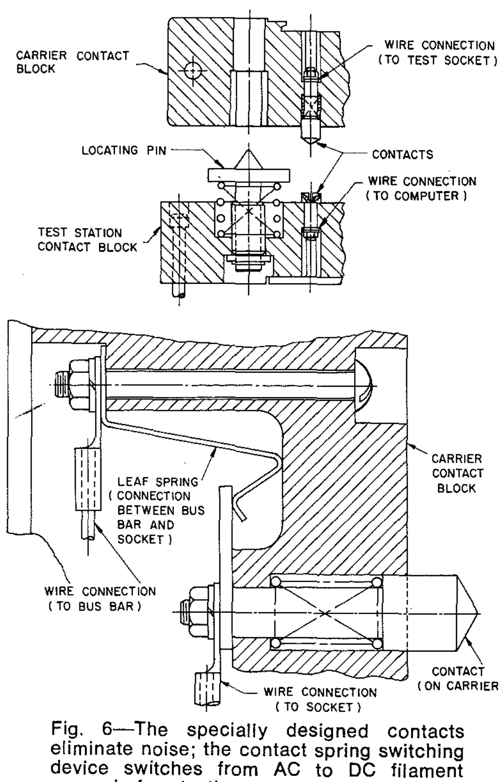

Fig. 6—The specially designed contacts eliminate noise; the contact spring switching device switches from AC to DC filament power before testing starts.

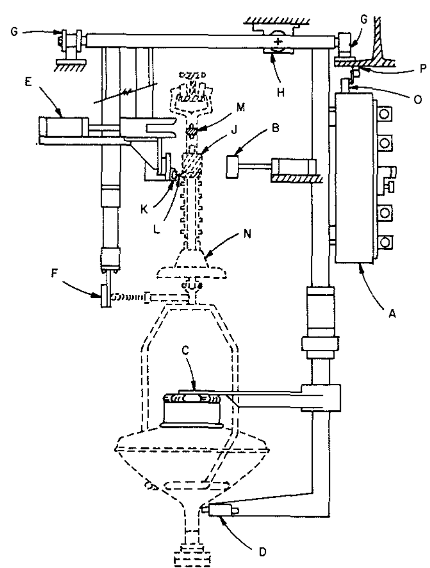

Fig. 7—Test carriage and special deflection coil.

TEST CARRIAGE

The test carriage (Fig. 7) is a complex, aluminum structured mechanism which incorporates various devices for mechanical and electrical contact with tube carriers. These devices include a complete pneumatic system, *A*, a special contact block, *B*, a stray-emission detector, *C*, a deflection coil, *D*, a chain engaging yoke, *E*, and a high-voltage contact, *F*. The carriage rolls on wheels, *G*, and is returned to rest position by the carriage return cylinder, *H*. The chain engaging yoke, the contact block, the stray-emission detector, and the carriage-return cylinder are all under the control of the pneumatic system. The electrical interface between the tube under test and the test circuitry is provided by the carriage contact block, *B*, and the carrier contact block, *J*.

PNEUMATIC CONTROL

Pneumatic controls are employed exclusively to eliminate any electrical switching noise. The pneumatic system is extremely simple to service, because valves are position self-indicating, and because a new pneumatic circuit diagram, patterned after an electrical schematic, is being used on this equipment for rapid and easy fault location. Defective valves can be readily removed from the manifolds on which they are mounted by four bolts without the removal of any pipe or tubing fittings.

Because of the high level of vibration in this equipment (engagement prior to test is 2 seconds, disengagement after the test is 3 seconds, and these actions may occur at a rate in excess of 250 times/hr) novel methods were found to keep fasteners tight. Pins, keys, patented lock nuts, adhesives, and the like are used. Several components were redesigned into one piece to eliminate fasteners.

STRAY-EMISSION DETECTOR

The reliability of the stray-emission detector was improved through many stages of development. The original design contained the detection equipment with the associated amplifiers and calibration circuits for both arc counting and stray-emission detection. The final design contains the detector device only which picks up the stray-emission signal. Most of the related circuitry is remote from the unit. The housing has a soft plastic ring on the rim contacting the tube face; the unit is mounted on a spring support with all axes of freedom so that the housing can adjust itself to fit and seal tightly against the tube face.

DEFLECTION COIL

A special deflection coil *D* of Fig. 7 is provided. It rides close to the neck of the tube under test so that the beam accelerated by the high voltage for arc counting and stray emission generation is deflected and does not damage the screen of the tube.

CARRIER-CARRIAGE RELATIONSHIPS

As a tube carrier (Fig. 5) moves into position inside the carriage, a pneumatic switch, *K*, is actuated by cam, *L*, of Fig. 8 which, in turn, causes a yoke, *E*, to move out and engage the conveyor chain, *M*. The carriage then moves along with the carrier, *N*. When the yoke engages the chain, the stray-emission detector, *C*, swings over the tube face and lowers down to contact the tube under test. As the stray-emission detector starts down, the contact block, *B*, is signalled to move into contact with the mating block, *J*, on the tube carrier.

After the test, a pneumatic valve, *O*, on the carriage engages a cam, *P*, on the building steel. This valve causes the stray-emission detector to raise from the tube and swing back out of the way, the contact block to disengage, the yoke to disengage from the chain, and the carriage return cylinder, *H*, to energize. The carriage returns to rest position ready to engage the next carrier.

CARD PUNCHING

Card punches located throughout the factory indicate the process history of a particular tube. Each card punch is preset and locked by the shift supervisor, with the exception of a few keys which the operator may have to manipulate during the shift.

The problem of punching information into cards was investigated thoroughly. Many types of manually operated commercial punches were purchased and tested before one was selected. Air actuation was incorporated. A pedestal was used to make the equipment easy to use in location and to collect the waste material punched from the cards.

The punch can be maintained by a spare during the repair of the original unit. It is only necessary to disconnect the air lines with the quick disconnects and to pull the special hinge pin from the cover to replace the unit.

DATA-ENTRY READER

The card reader used is a commercially available unit which is modified and adapted for use with conveyorized autotesting. This unit is mounted vertically on a cabinet which, in turn, contains the electronics to interface the reader with the computer system. The card reader accepts a standard 12-row, 80-column punched card. As purchased, the card reader was manually operated by means of a lever. In the new system, the hand lever is replaced by an air-operated rotary cylinder which is controlled by a pushbutton to close the reader and by a signal from the computer to open the reader. The reader itself may be quickly disconnected from the electronics and the rotary cylinder to facilitate maintenance.

ANNUNCIATION STATION

An identification signifying the test results for each tube is provided by a unique tape-applying mechanism (Fig. 4). This equipment automatically feeds a ¼ x 1-inch pressure-sensitive colored label onto the panel skirt of the tube. There are five markers, one for good tubes, and four to identify rejects. All tubes receive one label for proper identification. A signal to the appropriate marker advances the label (on a glassine backing strip) by one space. At the end of the applicator arm the glassine strip is sharply doubled back without bending the label, which leaves the exposed, tacky end of the label free. As the tube to be marked comes to the applicator arm, the free end of the label adheres to and is brushed on to the tube with light pressure by a brush on the end of the applicator arm.

Because the backing strip for the labels is translucent, a photocell device installed in the mechanism can "see" the space between the labels and stops the feed after each label. A double-acting air-hydraulic checking cylinder lifts and lowers the entire mechanism to seek the various tube sizes as they pass along the conveyor.

Autotest—automatic production-test and process-control system for color picture tubes

W. E. Bahls
F. C. Fryburg
A. C. Grover, Jr.
J. F. Stewart
N. A. Teixeira
E. D. Wyant

The automatic production-test and process-control system permits more efficient and more accurate testing of mass-produced color picture tubes than was heretofore possible. Therefore, this system offers the possibility for both improving the quality of the manufactured product and reducing the cost of the testing procedure.

An important step in the production of a complex, mass-produced product such as color picture tubes is the final testing. Formerly, color picture tubes were tested at a number of test stations, each manned by an operator. Because of the many different tests that had to be made, testing required many people, much test equipment, and a considerable amount of time, and was relatively expensive. In addition, because of the production deadlines the number of tests that could be performed was limited. Finally, because many people and pieces of testing equipment were involved, maintenance of calibration was difficult. It sometimes occurred that tubes which should have been rejected were not discovered and tubes which were perfectly good were rejected.

THE SYSTEM

The system includes five test stations, each testing different tube parameters and all under the control of a digital computer of the stored-program type. It also includes means for automatic indication which shows whether a tube has passed all tests and, if not, the tests which it has failed and, in some cases, the reprocessing steps which should be taken. The computer performs immediate (on-line) analyses of the tube parameters which have been measured during the testing procedure. In addition, it performs subsequent statistical analyses of the data to determine the deficiencies or potential weaknesses in the manufacturing process so that corrective action may be taken. Fig. 1 is a functional flow diagram embodying not only the test capability of the system but also its ability to provide some control over the processes (exhaust and aging) immediately before testing and the analysis and/or reprocessing subsequent to testing.

PRODUCTION PROCESS

The manufacture of color picture tubes involves many different steps, including manufacture of the mask, application of the screen to the faceplate, production of the gun assembly, joining of the faceplate to the remainder of the glass envelope, sealing of the gun assembly into the glass envelope, evacuation of the tube, and the like (Fig. 2).

During the manufacturing process, each tube is identified by a number. This identification number, and identification of certain critical steps in the manufacturing process, are recorded by punching a data-processing card, which travels with each tube. For example, in the manufacturing process there are a number of different machines employed for evacuating the tubes. The identifying number of the machine and the evacuating cart used for processing a particular tube are recorded on the data-processing card for that tube. The tube class and the tube type are also recorded.

After the above manufacturing steps have been completed, tubes of different types and classes are transferred from different processing equipment and/or conveyors to the final processing conveyor. Each tube undergoes certain processes which activate the cathode coating of each gun. Such process functions are possible because each tube is located on a separate aging/test carrier which (through its aging socket and spring contracts) provides the electrical interface between the tube and the process equipment.

FACTORY AUTOMATIC ELECTRICAL TEST COMPLEX

Data Entry Stations

When the tube leaves the aging area (Fig. 3) the aging socket is removed and the test socket is connected. In addition, the data card which travels with the picture tube is placed in the card reader. (As previously men-

Editor's note: The biographies and photographs of the other authors appear with other papers in this issue.

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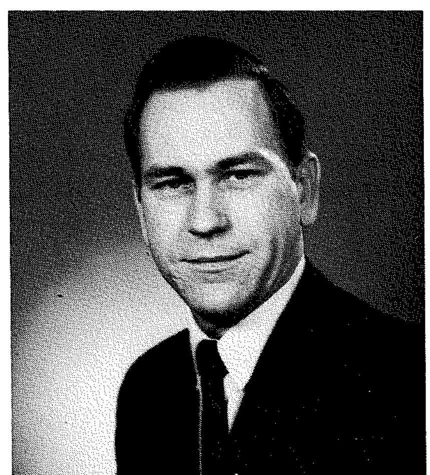
received the BSEE in 1955 from Georgia Institute of Technology and the MSEE in 1961 from the University of Pennsylvania. From 1955 until 1961, he was employed by RCA as a project and systems engineer on Airborne Fire Control Systems and Automatic Test Equipment. In 1961, he joined General Dynamics as a systems engineer responsible for systems analysis of satellite orbits and interceptor/light paths. Mr. Wyant rejoined RCA in 1962 as Leader, Technical Staff, responsible for systems and hardware design of automatic test systems. His activities include such systems as MTE, DIMATE, APTE and CCOS. In 1968, Mr. Wyant received the David Sarnoff Outstanding Achievement Award for design, development, and installation of a computer-controlled, fully automatic, production test system. He is a member of the IEEE.



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tioned, this card includes such vital information as the tube class, the tube type, and the identification of the equipment used to process the tube). After the card is placed in the card reader and the reader is closed, an operator depresses a button on the reader control panel to indicate the test status of the tube. The button depressed indicates whether the tube has been tested previously. If all such data have been properly entered, they will then be read into the computer. A signal is then returned to the card reader from the computer indicating that the data have been read and recorded; this signal opens the card-reader mechanism. The operator then removes the card and returns it to the tube.

In the meantime, the computer is processing the information read in from the data entry station. Some of this information is maintained in high-speed memory. The balance is stored on magnetic tape for later off-line use. The information retained in high-speed memory includes the tube class, the tube type, and the position number of the carrier on which the tube is riding. This information is vital to the performance of the tests in the subsequent five test stations.

Shorts and Leakage Test Station

When a tube reaches this station, an electrical connection is made between the tube to be tested and the specific test station. In addition, a signal is generated which produces an interrupt to the computer signifying that there is a tube in the station ready to test. The computer, having kept track of each of the 120 carriers included in the test loop at any given time by means of an interrupt analysis system, is then able to determine the number of the carrier in the station and, therefore, the class and type of the tube to be tested. With this information, the computer then determines the tests to be performed on the tube while it is in this station.

It should be noted that once the engagement of the contactor blocks of the test carrier and carriage is completed, both the tube and the carriage continue to move along the conveyor. This joint movement continues for a period of 10 seconds which is the maximum time available to perform all of the tests on that tube. At the end

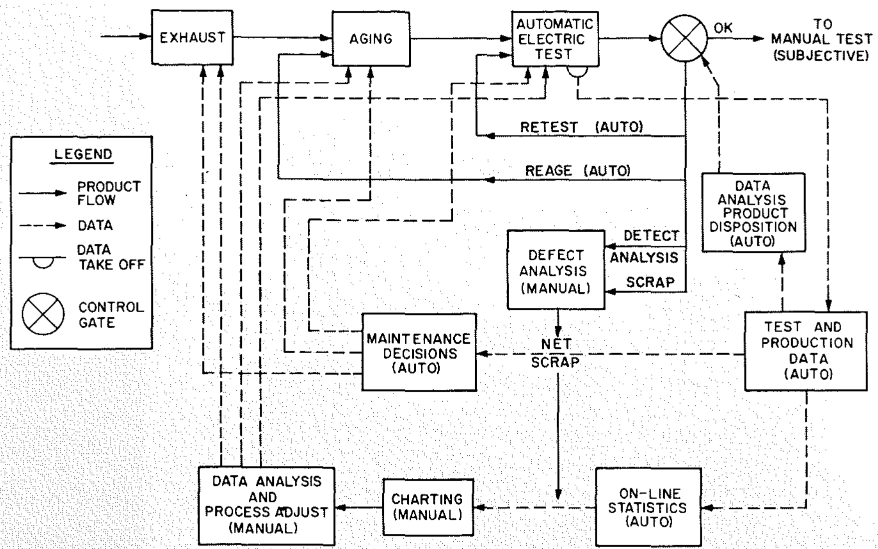

Fig. 1—Functional system diagram of the automatic production-test and process-control system for color picture tubes.

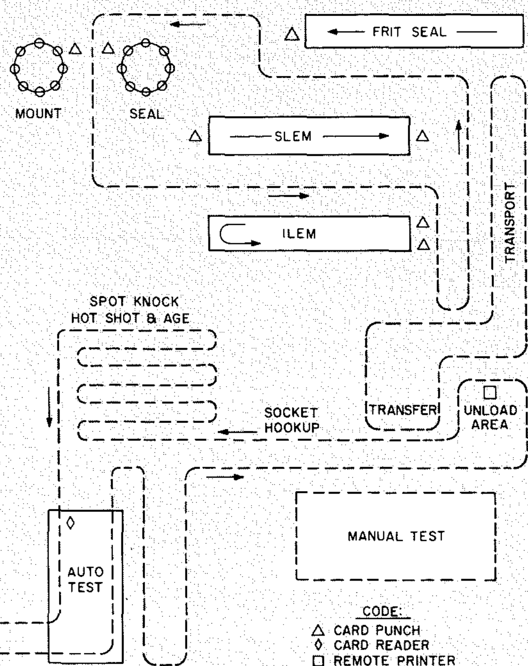

Fig. 2—Factory process flow.

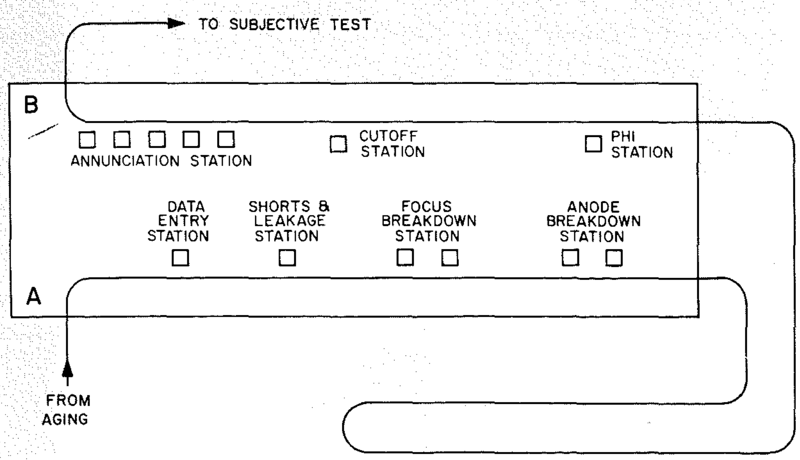

Fig. 3—Factory automatic electrical test complex.

of the 10-second period, the contactor blocks are disengaged and the test carriage returns to its starting position to pick up the next tube carrier.

Because of the high-speed switching capability of this system, the shorts and leakage station has been so designed that it is capable of performing a maximum of 42 individual tests on each tube. In actual practice, the total test routine has been broken down into 13 group tests and 29 individual tests. During a group test, voltages are applied to several elements and a measurement circuit is tied in to one additional element. The leakage current between that element and those with applied voltages is then measured. If this leakage exceeds a predetermined value, the computer then performs the individual tests. With this method, it is possible to test good tubes in a minimum amount of time and, simultaneously, to produce detailed information on tubes that exhibit leakage. Finally, it is noted that this feature not only tests the elements in a given gun, but can also test similar elements between guns.

This station, as well as all other stations, was designed for maximum flexibility. This system can apply a wide range of voltages to each element of the tube and also read a wide range of leakage currents. Such a capability is currently sufficient for measurement of all known color-picture-tube types and it is expected that it will handle all future types being considered for production.

Focus Breakdown Station

This station is the next one in the autotest sequence. From the standpoint of test-carriage to tube-carrier contact, its operation is similar to the previous station. In addition, however, it contains a sensing device which is placed over the face of the tube. This test station performs an over-voltage test. In other words, during the entire test period that voltages are applied, the beam current is completely cut off by a high bias voltage, and excessive voltage is applied to the focus element. The purpose of this test is to determine any instability in the form of arcing or stray emission between the accelerating element and the focus element of the tube.

Tube arcing is detected through a special transducer device in the anode circuit of the system. Thus, when arcing occurs the current level flowing in the anode lead changes significantly. This change in current is detected and converted into a digital form which is stored and subsequently transmitted to the computer. Detection of stray emission is accomplished through photosensitive devices installed in the detector housing which, in turn, is placed on the tube face during the entire test period. The photocells sense the light which develops as a result of stray emission.

Finally, it should be noted that these devices continue to count arcs and detect stray emission during the entire test period. The final readings sent to the computer constitute a summation of all arcs and stray emission developed during this test cycle.

Anode-Breakdown Test Station

This test station is next in sequence and is quite similar to the focus breakdown station. The primary difference is that the over-voltage in this particular case is applied to the anode rather than the focus element. Therefore, the primary source of arcing or stray emission is between the focus and anode elements of the tube.

Experience has shown that although these two test stations appear to be performing a very similar test, the tube-processing characteristics are such that problems can develop in the anode-breakdown or in the focus-breakdown area independently of each other. Thus, both of these tests must be performed to insure a good quality of the product to be shipped. Finally, it should be noted that the system has the capability, through computer control, to provide different over-voltages for the anode and/or focus element as different tube classes are tested.

Phi Station

This station, although next in the process, is some distance away from the anode-breakdown station. Such a delay permits the tube to cool. These tests are performed at minimum rated heater voltage after a short warmup. The first test in this station is cutoff-compensated emission current, commonly referred to as Phi. The test is performed in two parts:

1) The voltages to produce emission-current cutoff are applied to the gun.

2) The bias voltage is programmed to 0 by the computer; the measurement device records the emission current, and the computer compares this value against the predetermined limits.

The emission-current cutoff is determined through a series of tests known as search tests. These tests are performed with a fixed negative bias applied to the control grid and a predetermined value of positive voltage applied to the accelerating grid. At this point, the cathode current is measured and examined in high-speed memory which determines whether the next voltage step applied to the accelerating gird should be more positive (increase in current) or less positive (decrease in current) to reach the cutoff point. This process continues until cutoff is reached. This series of steps is performed three times to check the three guns in the tube.

A second important test in this station measures the gas content of the tube. In this test, the search concept is again used; a negative control-grid bias is programmed through a series of steps by the computer until a predetermined cathode current value is achieved. After the search test, two additional current measurements are made and their values are recorded in high-speed memory. A subtraction between two values is made and their net difference, usually in microamperes, constitutes the gas reading.

The final test at this station is anode continuity. As the name implies, it determines the continuity from the anode element of the mount through the bulb spacer and graphite coating to the button on the side of the funnel, where the high-voltage circuitry in the receiver will be eventually connected. Unless good continuity exists throughout this entire circuit, the tube will not work properly and will frequently exhibit a ragged raster.

Cutoff Station

This is the last test station in the system. There are two major tests at this station, each performed at normal heater voltages. The first is the emission cutoff test performed on each of the three guns. The G_2 voltage obtained after the successful completion of a series of search tests is compared with a predetermined limit. In the second test, the bias voltage is programmed to zero and the maximum emission current is read and checked. These tests are then repeated for the other two guns in the tube. Finally, the last test in this station measures the actual heater current.

Annunciation

When a tube has completed all tests in the five test stations, it moves into the annunciation station. For each tube, this station provides specific colored tape markers to indicate whether a tube has satisfactorily completed all tests and, if not, what further processing is required.

At this point, it should be noted that in the data entry station, a 75-bit section of high-speed memory is set aside for the tube before it proceeds through test stations. This section is commonly referred to as the binary failure image and during the entire autotest cycle it provides the means of recording all failures of the tube in question for each of the 75 tests.

Once a tube reaches the annunciation station, the computer scans the binary failure image table for that tube to determine its test status. If the scanning reveals that the tube has passed all tests, a green label is applied to the tube with the first of the five tape markers. If, however, the tube has failed one or more tests, the computer determines the failures in the order of importance by means of a previously established priority annunciation table.

With this information, the computer commands one of the four remaining labels to be applied to the tube and, thereby, signifies one of the four alternate processes the tube will undergo: RETEST, REAGE, DEFECT ANALYSIS, and SCRAP.

A remote printer located at the conveyor unloading point is connected to the autotest system. This printer provides detailed information to the tube analyst which indicates the tests that any individual tube failed. Experience has shown that these print-outs are proving invaluable for establishing the cause of tube failure.

PROCESS CONTROL FEATURES

Condemnation

When the tube reaches the data entry station, certain key-process data are read from the card into the computer which stores this information in high-speed memory. These data identify with the tube the key manufacturing processes used in its production. As the tube passes through the autotest cycle, pertinent test results are analyzed by the computer and recorded against specific pieces of production equipment on which the tube was manufactured. If this analysis reveals that a particular piece of manufacturing equipment has been producing bad tubes, the computer will display this result and the equipment will be removed from production. Although such condemnation practice has been in use on a manual basis within picture-tube plants for many years, it is anticipated that the additional high-speed capabilities available through the autotest system will improve the effectiveness of the condemnation procedure and will, thereby, reduce the number of faulty tubes generated from defective equipment.

Data Analysis

Another process-control feature of this system is its ability to analyze and summarize certain key variables collected during the test process. In addition, the system can provide regular reports of complete test results by the tube class and by type of defect. Through these analyses, it is anticipated that valuable information will be provided to both factory and laboratory engineering personnel which will aid them in their continuing efforts to improve tube processing and tube design.

DESIGN FEATURES

Accuracy

Analysis of this equipment clearly indicates that it is far more accurate than any equipment previously used in factory testing. In many respects, it provides a level of accuracy superior to existing laboratory equipment. Two key areas providing a major portion of this improved accuracy are the power supplies and the measurement circuits. In addition, another important feature of this system is its capability for continuous self-check which insures that all test equipment is calibrated and functions properly.

Flexibility

A major investment of this magnitude cannot be justified unless adequate assurance of the long range use of this equipment is provided. For this reason, considerable care in the original system design and in the subsequent design of the hardware and software was devoted to the idea that long-range flexibility would be maintained. From the standpoint of hardware design, measurement ranges, voltage ranges, and the like, system capabilities were extended well beyond the requirements of existing tube types. Therefore, it is anticipated that as future tube types are developed, they can be readily adapted to this system without major modifications in the hardware.

The software design also included provisions for changes. In essence, the system was designed to provide a generalized test routine. As each new class of tubes comes into being, a test file must be developed for it. This file can be prepared by personnel familiar with testing but with little or no familiarity with computer programming. In this manner, it is anticipated that new tube classes can be introduced into the system without any significant program changes. This fact has been substantiated already through recent development of the Einzel-lens test file for use with the Autotest system. This development was accomplished with no changes in the software.

SUMMARY

The automatic production-test and process-control system described has computer-controlled capability for all functions. This capability allows the control of all five test stations, the performance of up to 75 tests on any given tube, and the testing of many tube types on successive carriers. These three features should allow the Marion plant to test all future types and classes of color tubes. In addition, the color Autotest unit can perform all electrical tests of color picture tubes with a higher degree of accuracy than any existing equipment. Finally, the process-equipment condemnation and the data analysis are expected to yield improvements in factory performance. Thus, with improved process control, more acurate test equipment, and a more uniform testing facility, the Autotest system in the Marion plant produces a highly reliable and excellent color picture tube.

The software operating system for autotest

A. C. Grover, Jr.
H. W. Kirk

The operating system is an integrated system of computer programs developed for production testing of electrical characteristics and process monitoring of color picture tubes. The system operates in a real-time, on-line, multiple-test-station, time-shared-hardware, factory test environment. This paper describes the objectives of the software system, the computer complement selected, the structure of the software, the functions performed, and the programming techniques used in developing the system.

THE TEST REQUIREMENTS of the software system were developed from the planned volume and assortment of tube types to be tested. These requirements had to conform to the tube preheat conditions, the timing considerations of the process, the process-control needs, the hardware reliability and cost, and the operation and maintenance objectives of the system.

The system had to be capable of testing a large, ever-increasing number of different tube types on which frequent testing specification changes have been made. In addition, specification changes and the addition of new tube types to the system would be made by non-computer personnel.

In this system, a tube undergoes a variety of tests under the proper preheating conditions. Seven separate stations are required: a data entry station for tube and process identification, five test stations, and a disposition marker station. For reasons of economy three of the test stations time-share the same test hardware. Up to 75 different electrical tests may be performed on each tube. The test times range between 5 and 240 milliseconds per test.

The system must operate in an on-line, real-time factory test environment. Tubes are tested on a continuously moving conveyor that is in line with the manufacturing process. A random assortment of tube types pass through the test stations. The rate of movement of the conveyor generates a cycle time for the system of about 15 seconds.

For process control purposes, the system has to produce rapid on-line feedback of information to the manufacturing areas. This feedback includes a failure analysis of test results for each tube with a recommendation for correction of any failure, the maintenance of on-line statistics of key test characteristics for each tube class, and the monitoring and condemnation of tube manufacturing equipment as based on tube test results.

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COMPUTER COMPLEMENT

The system required a general-purpose computer which would handle the real-time operation and control aspects, as well as the data-processing aspects. A high-speed memory was needed to process the assortment of tubes in real-time, and an intermediate-speed memory was necessary for rapid changes in tube specifications. A priority interrupt system was required to assist in the executive control of priority of actions to be performed. Simultaneous compute and use of peripherals was required.

The computer complement selected featured the following: 16,000-word (24 bits/word) high-speed memory with 8 μs cycle time; a 92,000-word magnetic drum with a 16.7 ms average access time; three levels of priority interrupt; interlace (simultaneous mode) with two internal and one external system buffers; a power fail-safe option; two magnetic tapes; a card reader; paper tape reader and punch; high speed printer; and a teletypewriter.

ORGANIZATION OF SOFTWARE

To some extent, the basic system requirements determined the organization of the software system. Care was taken, however, to structure the software system in a manner that would facilitate maintenance procedures. In an operating factory, changes occur frequently; new types of product are introduced, control limits change, tests are introduced and deleted, and other specification changes occur. Because of the frequent changes in testing specifications, it was decided that all such factors should stand on their own in the form of a master file and be used by the test program as parameter messages rather than being built into the basic test program logic. Because the testing specifications for all tube classes were too extensive for permanent residence in high-speed memory, they were stored on a magnetic drum. Within a class of tubes there are various tube types with similar test specifications. As a result, a basic matrix of electrical test parameters was set up within the master file for each tube class. For each tube type within a tube class, there is a test-order message which controls the tests to be performed and their sequence.

Various priority-interrupt servicing routines constitute the main software division. Because higher-level activities can gain control from lower-priority activities, each servicing routine was

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assigned its own internal work areas. Therefore, the integrity of such areas is maintained without a multi-level "save" logic.

In a similar manner, the interrupt system is disabled when common subroutines used by more than one priority interrupt level are being executed. The interrupt system is also disabled during communication with the external system. If this disabling were not used, a higher-level activity could intercede and disturb the established communication link between the test system and the particular software transmission routine.

Four major programs were developed to cover all aspects of the system as follows:

File maintenance program (off-line)
Start-terminate-restart program
Factory automatic electrical test program (FAET)
Off-line self-test programs

Fig. 1 is a macroscopic flow chart of the total system.

File Maintenance Program

The master file which is on magnetic tape contains complete testing specifications and software control information for all items to be tested. Because

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received the BS in Mathematics from Upsala College in 1950. He joined Prudential Life Insurance Company and was involved in Budget and Personnel Control work. In 1955 he joined the Curtiss Wright Corporation as a Scientific Computer Programmer and specialized in writing aircraft engine analysis programs. In June 1957 he joined the Management Informations Systems and Services department of RCA. His primary responsibilities have been in the development and implementation of computer based systems including a quality test and control system for electron tubes, a factory manufacturing scheduling system and computer controlled real-time automatic testing systems.

of the high volume of specification changes, an engineering-oriented, narrative-type language was designed to facilitate the updating of the master file. This language allows the test engineer to effect the desired changes without a detailed knowledge of the test equipment or the software system. The translation of this user-oriented language into a computer-oriented data structure is accomplished by the file maintenance program. Complete tube classes can be added or deleted and changes can be made to sub-items within a tube class. Tube classes that have been affected by change notices will be printed out so that a complete set of up-to-date testing specifications will always be available to the engineering personnel.

Testing specifications are maintained by tube class. When specifications change for a particular tube class, the original specifications are retained on tape with the updated ones. Therefore, previous specifications are always available for testing or data-retrieval purposes.

At the beginning of a test run, the required master file data for tube classes being tested is selected from the master file tape and inserted onto the drum. When there is a variety of the tube classes on the conveyor, up to six independent drum reads have to be made within the system test cycle to obtain master file information. The required speed could not have been attained by tape reading.

There is a file description sheet for each file in the system that describes the contents of a particular file in detail. Each file sheet is assigned a unique alphanumeric designation and within each sheet, each listed item is assigned a unique number. These designations are used in the actual computer program to define the files. The definitions were organized to permit all the file addressing to use the file page and item designations as the basic reference address. Program addressing in this manner allows softwafe systems maintenance personnel to identify immediately the item in any file being addressed by a particular program instruction. This method also achieves good programming coordination because every program in the system uses a common method to address all files.

Start-Terminate-Restart Program

This program initializes the computer high-speed core and drum memories for the test program. It obtains the tube-type specification for the types to be tested from the magnetic-tape master file and loads them on the drum. It performs all the memory layout and housekeeping functions that are necessary for the test program to link properly to the tube-type specifications on the drum.

When the system is to be shut down either by the computer because of hardware failure or by operating personnel, the program performs an orderly termination procedure. All intermediate data necessary to resume testing are written to the drum. These data include all of the identification and status information for the 120 tubes in a partially tested state in the test system, the on-line statistics data, and the manufacturing-equipment condemnation lot history data.

When testing is to be restarted, the program retrieves the required data from the drum and initializes core memory for the test program to resume testing at the termination point. If the conveyor has been moved while the system was down, the appropriate adjustment is made.

Factory Automatic Electrical Test Program

There are three main classes of routines in the FAET program. One class consists of control routines which deal directly with interrupts as they are received and, in addition, coordinate and schedule the work of the various servicing routines. The second class consists of service routines that carry out the detailed operations which service the various interrupts. Finally, the third class is a series of routines that perform functions not directly related to the interrupt system. These programs cover functions such as compilation of on-line statistics, condemnation of manufacturing equipment, and generation of formats for output reporting. The software system functions classified by interrupt levels are listed in Table I.

The factory automatic electrical test program controls the performance of the test set-up, obtains the test measurement results, and performs the required data analysis of the measurements results for all tests in the five test stations. All of the testing and processing of individual tubes in each of the stations must be completed within the cycle time of the system. The test program is generalized and operates from tube-type test specification parameters maintained in a master file for the applicable tube type to be tested. On-line statistics are kept on key test characteristics by tube class and are printed out when the specified sample size for a tube class is reached. These statistics, as soon as available, are manually plotted on control charts for process-control trend-analysis feedback. Lot histories are kept on-line for many pieces of manufacturing processing equipment. If tube test performance indicates that a particular piece of manufacturing equipment exceeds a specified failure rate, that piece of equipment is condemned by an on-line condemnation report.

After the tube is tested in all test stations, it enters the marker station. The program performs a failure analysis of the composite test results and determines the action to be taken on the tube. With the analysis completed, the program commands the marker station to place the proper disposition sticker on the tube. If the tube fails, the causes of failure are printed out on a printer at the tube unload station. Specified test measurement results are stored on magnetic tape for off-line engineering and quality control analysis.

All major components of the test hardware are self-tested periodically by the software system to assure equipment accuracy. Because the test system is in line with the manufacturing process, it is very important to minimize downtime during a failure of system hardware. The software system is designed to perform rapid start-up, termination, and restart procedures. When a hardware failure is detected by the on-line self test, the cause of failure is printed out and the system is terminated. An extensive off-line self-test diagnostic program is utilized for further isolation of the malfunctioning components.

When a tube enters a system station, a uniquely identified interrupt is sent to the computer for that station. The executive control routine acknowledges the interrupts, edits them, and, after verification, simulates the conveyor movement to update the appropriate station pointers. Each station pointer contains the address of the tube identification for the tube in that station. If errors occur in the interrupt sequence, the executive routine takes corrective action and issues an error report. If excessive interrupt errors occur, the executive routine initiates termination of the system and prints

Table I—System Functions by Interrupt Level.

Priority	*Function*
1	Controls the basic test function, criticizes test results, and performs required statistical calculations for the three electrical test stations that time share hardware.
2	Serves same purpose as priority 1 only for the two electrical test stations that contain their own individual test hardware.
3	Audits the sequence of *carrier-entering station* interrupts, synchronizes software system with conveyor movement, and controls the sequence of testing and retransmission of test control data in case of transmission errors in the three time-shared hardware test stations. Reads tube identification information at data entry, criticizes composite test results for tube disposition decision, and displays requested electrical values on remote printer.
4	Controls all typewriter output reporting, performs statistical calculations, condemns manufacturing equipment, and generates detailed reports on failing tube parameters.

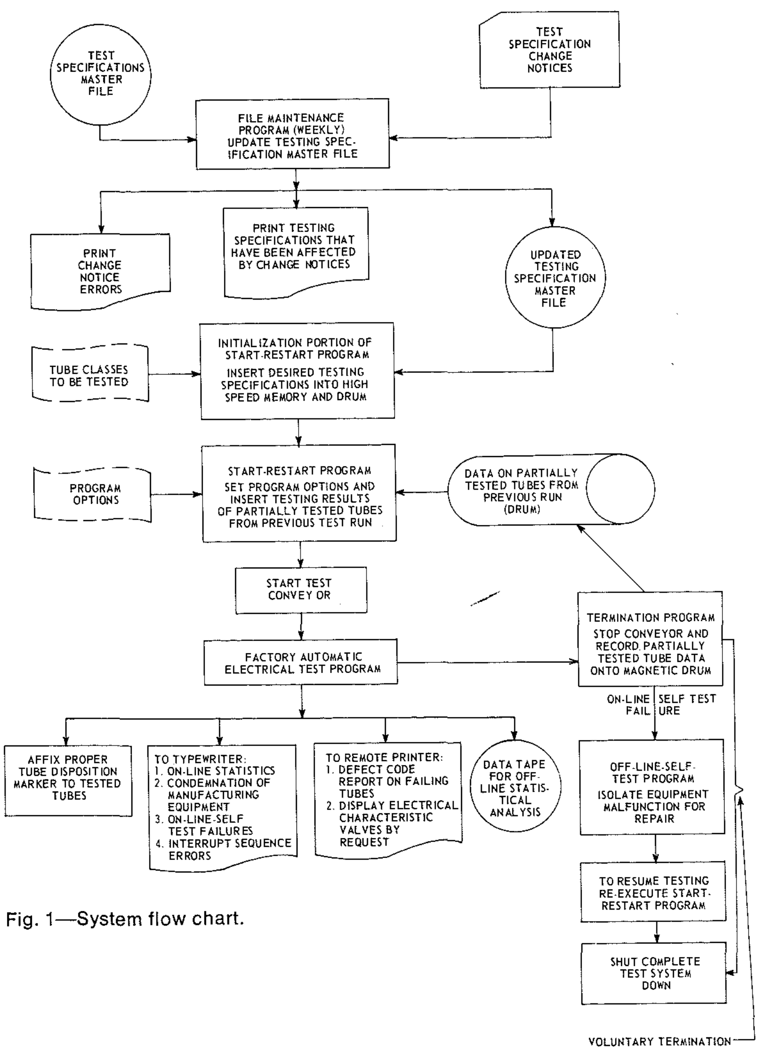

Fig. 1—System flow chart.

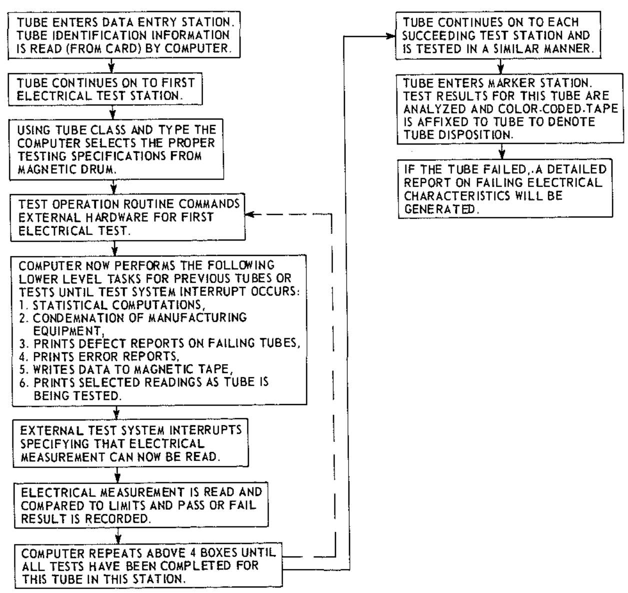

Fig. 2—Test system processing of a tube.

out the causes for termination. The executive control routine directs the sequence of operation of the test program routines. It performs operation of the test program routines, and also controls the priority of program routine execution, allocates the time shared hardware to the proper station, and acquires the tube type testing specification from the drum for the test operation routine.

On-line Self-test Program

This program constantly monitors the test-system hardware for malfunctions. Error reports are printed whenever any system malfunction is detected. These reports include interrupt errors, self-test errors, magnetic-tape or drum malfunctions, invalid or missing tube identification, incomplete testing, and data-transmission errors. The testing accuracy is assured with periodic on-line self-test of the power supplies and the test-station measurement preconditioners. Tube simulators placed on carriers at intervals along the conveyor are used to check out the test station routing matrix. Error reports are printed for any elements that fail, and immediate action is taken to correct the faulty element.

Off-line Self-test Program

This program performs an extensive examination of all the test-system hardware. The program is used for preventive maintenance and it assists the maintenance personnel in making rapid repair when a hardware failure is detected by the on-line self-tests performed by the Factory Automatic Electrical Test Program.

PROCESSING A TUBE

Fig. 2 shows the complete test system processing of a tube. As the tube enters the data entry station, an interrupt is activated, and a card that identifies the tube is read into the computer.

The test operation routine controls the execution of the test setup and obtains and analyzes the measurement results from the three electrical test stations which utilize time-shared test hardware. Portions of the system hardware including the analog-to-digital converter (ADCON), five power supplies, and the routing matrix are time shared by these test stations. The highest priority external interrupt (priority 1) is assigned to the ADCON (measurement ready interrupt) because the highest volume of tests is performed in these test stations and because the time sharing of the hardware constitutes the major time restraint in the system. The test operation is generalized to operate from parameters in the master file for the applicable tube class to be tested. The particular tube type header specifies the tests to be performed and the order of tests for the tube type in the applicable test station. The test details in the master file for the particular tube class specify the hardware set up and execution conditions and the data processing requirements on the measurements result for the individual tests.

When a tube is ready for test in an electrical test station, the executive control routine identifies the tube by utilizing the station pointer and tube identification table row, and assures that the proper tube type test specification is in high speed memory before it turns control over to the test operation routine.

The execution of a test is initiated when the proper test detail is selected and the test setup information is transmitted to the system hardware. The transmitted information includes: the setup values for power supplies; the routing commands to connect the proper tube elements to the correct power supplies, ADCON measurement device, ground, and float conditions; and the measurement control word to select the proper preconditioner scale for the ADCON and to set up the prescribed delay time for set up of the test.

After the prescribed delay time which allows the system to stabilize for a given test, a priority-1 interrupt is sent to the computer indicating that the measurement is ready. Upon receipt of a priority-1 interrupt, the control is returned to the test operation routine and the measurement result is read. If the measurement result is out of the selected scale range, the ADCON is rescaled and the test repeated.

The final measurement result is stored in high-speed memory for data processing and compared with factory limits from the test detail message in the master file. The next test to be performed is determined from the test order message for the tube type. The test set-up is commanded before the previous test result is processed through the statistical routines. This arrangement permits time-sharing of the hardware stabilization time for the next test with the data processing of the previous test measurement. After data processing performed on the measurement result is completed, control is turned over to the executive control routine so that other required functions can be performed. A priority-1 interrupt returns control to the test operation routine when the next measurement result is ready. This procedure continues until all of the tests on the tube are completed in the test station. It should be emphasized that once testing has been initiated in one of the three time-sharing test stations, testing must be completed in that station before it is initiated in either of the other two remaining stations. A similar pattern is followed by the two remaining stations.

Four different classes of tests are performed by the test operation routine as follows:

Regular test—The regular test requires a single test setup, test measurement, and processing of the measurement result.

Conditional test—The conditional test is essentially the same as the regular test. In addition, however, it has an option to choose the next test depending on passage or failure of the measurement result.

Seach test—Search tests require multiple test setups and multiple test measurements. The voltage on one element is successively changed to obtain a measurement within specified limits on another element. The final voltage value is processed as a measurement result. This voltage value sets a power supply for a subsequent test on the tube.

Calculation tests—The calculation tests are performed on the previous measurement results. These tests include difference, ratio, summation, comparison to established limits, and analysis of the data entry test results.

When tubes are in the breakdown stations, the interrupt received (priority 2) sets up the necessary test conditions and then returns to other test and processing duties. Arc count and stray emission data are determined and stored by other hardware, and at completion of testing in the station, the computer is interrupted to transfer this data into high-speed memory for comparison to limits.

When an individual tubes reaches the marker station, the program analyzes the composite test results for the tube and determines what action is to be taken. The proper disposition sticker is commanded and applied to the tube. There are five categories of tube disposition (OK, REAGE, SALVAGE ANALYSIS, RETEST, CRACKOFF). The program prints out the defect codes of the failing tests.

Executive Control Logic

The executive control routine serves as one of the task dispatch centers of the software system. It determines the next task to be performed at the priority-3 interrupt level. The various priority-3 interrupt functions are listed in Table I.

When carriers enter the various stations on the test conveyor, various priority-3 interrupts are activated. If there are no higher-level interrupts to be serviced, control is turned over to the priority-3 service routine. The location at which a lower-level task or priority-level-3 task was interrupted is saved along with all pertinent registers, and, after the interrupting task has been completed, control can return to the original routine.

Control is transferred to the interrupt sequence analysis routine whenever a "carrier entering station" interrupt occurs. This routine determines if the interrupt occurred in its proper sequence. There are seven stations on the test conveyor from which interrupts should be received. The sequence of these seven interrupts within the test cycle is expected to be fixed to facilitate the synchronization of the software system with the movement of the conveyor. When this sequence is violated, the software determines where the problem is and compensates for the error. For example, if an interrupt is missed, the software must take note that head n has passed the particular test station without an interrupt and that head $n+1$ will be the next to enter the station. When errors do occur, the software system becomes supersensitive to the immediate future interrupt sequence until its is assured that everything is in good working order.

An additional check of synchronization is made by the synchronization interrupt. Every 100th carrier generates a special interrupt at the data entry station to announce itself to the software system. The program, in turn, predicts the time when this special interrupt should occur. If the special interrupt occurs at any other time or fails to occur when expected, system testing then terminates in an orderly fashion, and the system displays diagnostic information that aids in subsequent error analysis.

One of the key files in the system is the tube identification table. There is a row set aside in this table for each carrier as it enters the test conveyor. When the particular carrier leaves the test conveyor, the row that it occupied is subsequently assigned to another carrier entering the test conveyor. There are seven stations in the test conveyor that generate interrupts as a tube enters the station. The software system maintains a station pointer for each of these stations as interrupts occur. These pointers allow the control logic to address the row of the tube identification table which contains the information on the tube that just caused the interrupt in the particular station. In the case of the data entry pointer, the control logic determines the row of the table to be assigned for the tube. The pointer values reflect the physical spacing of the test stations. When an interrupt occurs from a test station, its pointer value is adjusted to synchronize with the entrance of the next carrier into the station.

PROCESS CONTROL

One of the major functions of the system is to produce rapid on-line feedback of information to the manufacturing process for control purposes. On-line statistics are kept on key test characteristics for each tube class being tested. The statistics subtotals are updated as the individual tests are performed. When the specified sample is reached for a given tube class, the on-line statistics routine computes and prints out statistical summaries. Average standard-deviation and percent-defective statistics are kept by specified test characteristics, by test group, and by manufacturing equipment group. These statistics are manually plotted on control charts for process-control-analysis feedback. Production counters in the computer room automatically count the amount of tubes tested and the amount of good tubes.

The condemnation routine maintains a running lot history of tube failures on many pieces of manufacturing equipment. When a tube reaches the marker station, the lot histories of the equipment on which the tube was manufactured are updated. If a piece of equipment exceeds the specified failure rate, an on-line condemnation report is printed. This information is relayed to the factory and the faulty equipment is removed from the manufacturing process.

ADDITIONAL CONTROLS

The test engineer can print out specific tube characteristics that he is interested in by setting a code wheel at the printer station and pushing a button. The tube identification, manufacturing-equipment and process identification, and test-measurement results are all recorded on magnetic tape for subsequent off-line review and analysis.

PROGRAM CHECK OUT

The approach used in program checkout was developed as an integral part of the basic system design. It was parcelled into three main phases: simulation testing of subroutines, static testing on operating equipment, and complete system dynamic test in the on-line real-time environment. The level of difficulty increased in each succeeding phase because of the increase in interactions between the hardware and software. Extensive pre-planning of the approach to program checkout is a necessity in on-line systems.

SUMMARY

The development and implementation of a complicated, on-line, real-time production test system must be carefully planned with respect to system requirements and over-all organization of the system concepts. It is certain that changes will be desired when the system is put into use and operating experience is gained. The software system organization should be generalized and lend itself to changes without extensive redesign. Pre-planning of the program checkout techniques and of the hardware/software interrelationships is very important. In a system of this type, the problems that occur in hardware or software must be located by the software.

Testing of color picture tubes—correlation of computer-controlled and manual techniques

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The automatic production-test and process-control system automatically evaluates all electrical characteristics of the color picture tube. The specific areas of testing are 1) emission-current cutoff, 2) leakage between the elements of the three electron guns during the application of acceleration and bias voltages, 3) gas content of the picture tube, 4) maximum emission current, 5) heater current, 6) focus and anode continuity, and 7) high-voltage stability (arc count and stray emission). The subjective characteristics of the picture tube, such as color purity of the red, green, and blue fields and convergence capability of the three beams are evaluated by the human operator.

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THE testing activity within a picture-tube manufacturing plant is concerned primarily with culling out those tubes whose characteristics are not within "limits". The "limits" represent the maximum range of values the tube may possess to function normally in a production television receiver. The computer-controlled test equipment utilizes the concept of "variables" testing. The numerical value for each electrical characteristic of the tube is compared with a predetermined test limit and then stored on magnetic tape along with the serial number of the picture tube. Also, the numerical values from key tests are analyzed statistically by the data-processing function of the computer. The statistical summaries are made available to Production Engineering and provide guidance as to the effectiveness of various equipment parameters that control the finished product. The development of an automated system of "variables" testing of the electrical characteristics of the color picture tube has proven to be far more complex than the earlier stages of evolution of factory testing. This article compares the manual and automated test procedures and shows some of the problems encountered in achieving good correlation between these two procedures and with the final criteria performance in the television receiver.

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EMISSION-CURRENT CUTOFF

One of the important characteristics of the color picture tube is the emission-current cutoff. The emission-current cutoff (spot-cutoff) on a particular electron gun is evaluated with a variable, positive power supply connected

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to the grid-No. 2 (G_2) electrode, with other specified voltages applied to the other gun elements. If the initial value of the supply is more positive than the cutoff value of the gun, a spot of light will appear on the phosphorescent screen of the picture tube. The power supply is then adjusted to be less and less positive until the light spot on the screen just disappears. The voltage on the G_2 electrode at this time is defined as the spot-cutoff voltage.

Manual

The conventional method of finding cutoff requires the test set operator to adjust the G_2 power supply while observing the spot on the screen of the tube. When cutoff is reached, the operator checks the G_2 supply voltage meter to determine if it is within "limits".

Automatic

In the automatic method, the G_2 supply voltage and the metering in the cathode circuit are both under computer control. The computer programs the power supply through a series of steps and makes a cathode-current measurement after each step. The current measurement is examined in a high-speed memory which determines if the next voltage step should be more positive (increase in current) or less positive (decrease in current) to approach the cutoff point. This process is continued until cutoff is reached. At this point, the computer checks the G_2 voltage to determine if it is within limits.

One of the more difficult problems was to find a purely electrical representation of a visual characteristic, in this case, spot cutoff. The system finally chosen was designed with a resistor in series with the cathode lead of the gun under test to which an amplifier output system was connected.

The power-supply complement for the automatic test equipment contains a secondary voltage standard. The programmed supplies are compared periodically to this standard to verify that the voltages applied to the picture tube are within specified limits. Thus, the voltage and current characteristics of the tube can be measured much more accurately than with the manual system, which relies upon less frequent and less accurate calibration.

Problem Areas

From the beginning, some instability existed with this setup. The heater supplies were feeding some noise to the routing network and to the cathode of the tube under test. As a result, various forms of shielding were required.

LEAKAGE TESTING

Manual

In conventional leakage testing (leakage between the electron-gun elements) normal bias and accelerating voltages are applied to the electron gun and a current meter sequentially switches into the gun-element circuitry. The resultant leakage current is compared to limits by the operator. In the event the current is greater than the limit, the tube must be analyzed further. Various bias and accelerating supplies are switched off, one at a time, and the effect on magnitude and direction of the metered current is observed. Such analysis is complicated because both positive and negative supplies are used. Other types of test equipment are also employed but, in most cases, each requires a special knowledge as to how each defect will respond on a given piece of equipment.

Automatic

In the automatic method of leakage testing, high-speed switching of the automatic test system is used to test the various electron-gun elements in pairs. The computer commands the proper power supply to connect to one of the elements and the metering to connect to the other element. The power supply is first programmed to a specified value and then the metering is scaled under program control for the magnitude of the leakage current flowing. Because of the fast switching employed in the system, as many as forty-two of these tests may be run in a period of two to three seconds.

Because present salvage techniques are effective only on certain types and magnitudes of leakage, one important reason for analysis of leakage rejects has been to gather data. These data have been used by Process and Design Engineering to make product changes which reduce the incidence of leakage. The more detailed and accurate leakage testing available in the automatic system should continue to contribute substantially to this phase of product improvement.

GAS TESTING

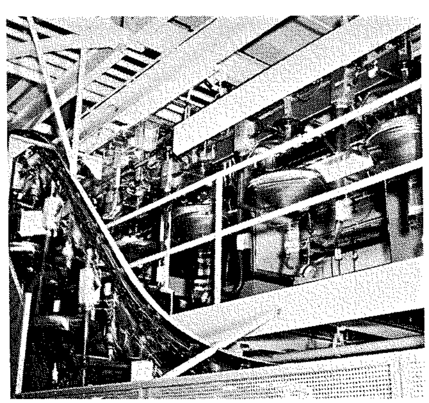
Manual

Four steps are required to determine the gas level in a tube, as follows:

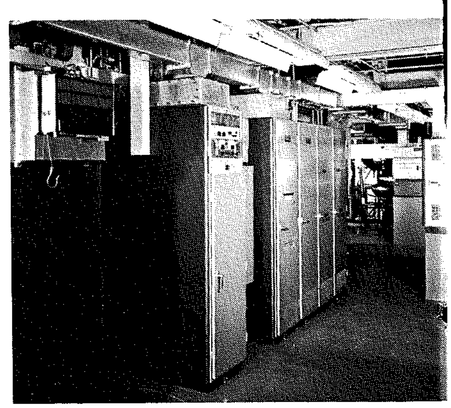
1) The bias voltage is set so that a current of 1000 μA is flowing from the three cathodes collectively.
2) The ionization current including leakage is observed.
3) The cathodes are biased off (ionization current equals zero), and only a leakage reading is taken.
4) The gas reading is the difference between 2) and 3).

Automatic

The gas test performed with the automatic equipment simulates the manual functions of the test operator. The bias voltage is moved in steps and each step is followed by a measurement. This process is repeated until the ionization current is adjusted to 1000 μA. The measurement device is then switched into the gas-ion collection circuit, and the ion current with leakage current is measured and stored in memory. At this point, the computer



Color tubes being conveyed to testing stations at the Marion Plant.



Some of the automatic production test equipment at Marion.

applies the voltages to bias off the three cathodes and reads leakage-current in the ion collector circuit. The computer then calculates the differences between these values to arrive at the correct gas reading.

Problem Areas

A typical picture tube has a gas reading of very low value (nanoamperes). Consequently, a large amount of amplification is required to boost this signal to the level required by the measurement device. Because of the large gain involved, sizeable amounts of 60-Hz noise and random DC variations were present in the gas reading. The addition of various types of shielding and filtering to the testing system brought these variations under control.

MAXIMUM EMISSION CURRENT

This test is performed in two parts. First, the voltages producing "emission-current cutoff" are applied to the gun. Second, the bias voltage is programmed to zero by the computer, and the measurement device records the maximum emission current flowing. The computer then compares this emission current value with pre-determined limits.

HEATER CURRENT

This test is a straightforward measurement. After the required preheat is completed, the measurement device is switched into the heater circuit, and the measured value is stored in memory and compared to pre-determined limits.

FOCUS AND ANODE CONTINUITY (AUTOTEST ONLY)

Tubes which have poor anode and focus continuity exhibit certain visual characteristics when operated in a manual test set. These tube defects now can be detected by means of special electrical tests which are programmed into the Autotest system.

HIGH-VOLTAGE BREAKDOWN TESTING

Manual

Higher-than-normal voltages are applied to the tube to determine if it has a tendency to arc internally. Two tests are required for the evaluation: focus breakdown and anode breakdown. Each test is performed for 10 seconds because experience has shown that the breakdown phenomena are time as well as voltage dependent.

In the focus-breakdown test, normal voltages are applied to the tube with the exception that the guns are biased to cut-off the electron beam. An over-voltage is then applied to the focus electrode.

Anode-breakdown testing is similar except that the over-voltage is applied to the anode. During each test period, the operator views the tube for arcs and stray emission. Stray emission is the emission of electrons from gun parts other than the cathode which excite the phosphor screen and cause it to emit light. In the event that the stray emission is above some minimum level, the picture contrast will be reduced when the tube is in normal operation.

Automatic

In the factory automatic test system there are two breakdown stations—focus breakdown and anode breakdown. Both test stations are identical; however, each may be programmed to perform different tests. The focus-breakdown test is used to determine whether a high-voltage breakdown will occur between the focus and G_2 elements. The anode-breakdown test is used to determine whether a high-voltage breakdown will occur between the anode and focus elements.

Specially designed devices are used to detect arcs and stray emission. The arcs are detected by a sensing device in the anode circuit. This device is responsive to the duration of an arc as well as to the number of successive breakdowns. The amount of stray emission that is present is detected by a group of photocells contained in the detector housing which is placed over the tube face. The housing is designed to fit directly and squarely on the face-plate of the picture tube. Because there is no assurance that extraneous light will not filter into the detector unit, the circuitry has been designed to automatically balance out any ambient light that is present before the high voltages are applied. The amount of light detected is converted to digital information for computer evaluation.

Problem Areas

It is possible to cause a transient-type arc during the application of voltages, which does not truly represent tube performance. As a safeguard, the arc and stray-emission detector circuitry includes inhibiting circuits to prevent detection while the voltages are being applied to, or removed from, the tube.

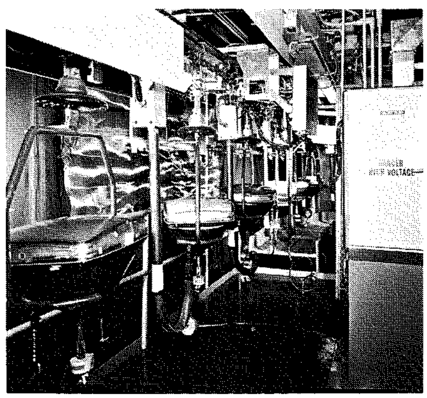
SUMMARY

The task of translating manual test techniques into an automated system proved to be a rather complex undertaking. The numerous problem areas encountered can be categorized as follows:

1) automating the visual detections of an operator (e.g., spot-cutoff);
2) achieving a proper balance between the high-speed capability of the computer and the slower response characteristics of the power supplies and associated connecting cables to the picture tube;
3) protecting the highly sensitive measurement circuits from the electrical interferences which are characteristic of a picture-tube manufacturing area.

It was only through close cooperation between the personnel responsible for the hardware and software designs and those familiar with tube design that most problems were solved.

This system offers many technical advantages. First, it is capable of performing quick and detailed analysis of the characteristics of various types of color picture tubes. Second, the data obtained are extremely reliable because the system not only contains very accurate equipment but also employs a periodic self-test feature to insure that calibration is being maintained. Finally, the flexibility built into the hardware and software designs offers the tube engineer opportunities to develop new testing techniques and to analyze the characteristics of new tube types carefully at early stages in their design.



Color picture tubes at one of the test stations.

Automatic platter tester

H. P. Cichon
R. L. Rudolph

The introduction of the "platter" backplane wiring system was brought about by the high density wiring requirements of the RCA Spectra 70 series of computers. Testing of these complex, multilayer, etched-circuit panels presents a significant manufacturing problem. This paper describes the automated system developed to help overcome this problem.

The physical size and complexity of a multilayer etched platter make manual continuity checks an extremely demanding task. Under the most favorable working conditions, highly trained and motivated inspectors will not detect 4 to 5% of the errors in a production lot. The probability of missing multiple defects in a single platter is even greater than 5% because of what industrial psychologists call the "elation effect" (i.e., the tendency to relax the inspection process after one fault is detected). The automatic platter tester has been developed to help eliminate these undetected errors and to meet the unique requirements of testing the Spectra 70 multilayer platters. The system (Fig. 1) is designed to functionally test the platter for opens, shorts, and proper termination resistor connections in a time period of less than five minutes, exclusive of the time necessary to interface the platter to the test system.

The hardware design of the automatic platter tester enables it to be interfaced quite easily with a computer such as the present Spectra RCA-1600 system. With such an interface and automatic loading of the platter under test, the test period will be well under four minutes/platter. In addition, the computer executive program can provide management data as to number of platters tested, error statistics and many other items as required.

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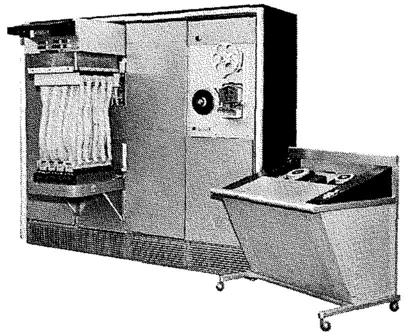

Fig. 1—Automatic Platter Tester.

PLATTER CHARACTERISTICS

The wiring for the basic processors in Spectra 70 is contained on wiring panels known as platters. Each platter can accommodate 130 connectors and each connector can contain up to 48 contact pins (i.e., a total of 6,240 pins). Seven voltage-access terminals can also be included on each platter.

All interconnections on the platters should have similar transmission-line characteristics. To achieve this, about 39% of all interconnections, or "wiring nets," are equipped with termination-resistor networks. Each network consists of a 147-ohm and a 312-ohm resistor connected in series from the —5-volt DC buss to the ground buss. (The 147-ohm resistor is connected to the ground buss; the net being terminated is connected to the resistor-junction point.) The termination networks are housed in small printed-resistor assemblies that solder directly into the printed wiring platter to assure short connections to their respective nets. Each assembly contains 10 termination networks.

SYSTEM CHARACTERISTICS

Two classifications of test must be performed by the test system: it must determine the quality of the net interconnections under investigation, and it must determine whether not the termination resistor network is properly connected. It must also be capable of testing a ground buss network having as many as 624 connections. Additionally, it must test for shorts between two networks that normally have a DC resistance of less than one-half ohm between them.

System Operation

Fig. 2 is a block diagram of the platter tester. The purpose of each of the 14 functional elements is as follows:

PTR—a 1000 character/second paper-tape reader.

INTERFACE LOGIC—acts as a character buffer between the control logic and the PTR.

PARITY AND DATA CHECK—verifies the parity of the paper-tape information and checks the format of the incoming data.

CONTROL LOGIC—acts as a data steering mechanism to route connection data to either the FROM or TO REGISTER. It accomplishes the transfer of the FROM REGISTER to the TO REGISTER, when required, and controls all memory and other system timing functions.

FROM AND TO REGISTERS—flip-flop registers that contain the FROM or TO ADDRESSES.

FROM ADDRESS RELAY DECODING—decodes the binary output of the FROM REGISTER.

FROM RELAY MATRIX—driven by the relay decoding logic which applies a test voltage to the platter net under test.

MEMORY ADDRESS DECODING—decodes the TO REGISTER to activate the memory X and Y drive lines.

SPECIAL MEMORY PLANE—a single coincident-current memory plane with additional windings to each core. The memory stores the actual platter net data.

SENSE AMPLIFIER AND ERROR DETECTOR —detects platter open or short conditions.

TR ERROR LOGIC—locates missing or defective termination-resistor networks.

PT PUNCH LOGIC—interfacing and character-sequencing logic which drives the paper-tape punch.

PT PUNCH—100 character/second paper-tape punch.

DISPLAY—indicators to display the various registers and test status indicators.

Data Flow

Initally, the system is reset and the "start" button is pressed. The PTR then reads the first message item. If the message read was the first net point and the control character was an *S*, the FROM REGISTER is set to the address as coded on the input tape. The FROM RELAY MATRIX is energized, activating the net under test and causing the memory cores associated with the net to be partially switched. The memory write cycle is completed after the *write strobe* pulse is generated. Subsequent to the memory write, the contents of the FROM REGISTER are transferred to the TO REGISTER to begin the memory read cycle.

The TO REGISTER contents are decoded to enable the memory to read out the location specified by the TO ADDRESS. The first memory read is that of reading the initial net point. All of the following net points are similarly read from the PTR into the TO REGISTER until every net point has been checked. The last net-point character is followed by an end-message character. Recognition of this character signals the tester to commence the memory-scan operation to check for extraneous connections in the net. The memory scan consists of sequentially reading each memory core in the plane. Upon completion of the memory scan, the net test is complete and the PTR advances to read the next net message.

Testing of the Nets

Generally, production faults in net interconnections lie in open or shorted conductors; high resistance shorts between adacent paths appear very infrequently. Therefore, net checks are limited to the task of determining opens in the interconnecting conductors which form the net and shorts between two or more nets.

The task of determining whether a connection exists between two points is relatively simple; an ohmmeter can be used to measure the resistance between the points. Such a test can be easily implemented by a stepping-switch (or rotary switch) system or by a relay-tree matrix.

The more complex problem is that of determining unwanted connections (shorts). The net must be energized, and all proper connections must be committed to a memory. Before being de-energized, the entire net must be scanned to determine if extra connections exist. This operation may consist of comparing each energized net point to that recorded in the memory. If they are the same, the connection is valid. If not, the connection is a short or unwanted connection.

The automatic platter tester is designed to accomplish all of the above tasks with a minimum of human intervention. Point selection is by means of a reed-relay matrix. This provides a fast, compact method of energizing the net under consideration. Solid-state switching, although fast and extremely reliable, does not have the output impedance required by the detection system.

The detection system is a specially designed memory plane, a modified coincident current memory. In addition to the normal drive, write-select lines, a special 4-turn winding is added to each core. This special (fifth) winding is the means of connecting the memory to the platter under test (Fig. 4).

The memory plane acts as a storage medium for the net under consideration. As shown in Fig. 4, if a relay contact closes, corresponding to any point in a given net, all of the fifth windings in the memory plane which are electrically connected to that point in the net receive current from a voltage source. A resistor in series with each winding limits the effective current (actual winding current multiplied by the number of turns through the core) so that it is insufficient to switch the core. Several milliseconds after the relay contact closure and the currents have stabilized, a write strobe pulse is applied to the write-select winding to complete the switching of the cores that are already partially switched. Thus, all connected points in the net are stored in the memory plane.

The task remaining is to determine if the points stored in the memory are legitimate. The input, a test tape, contains the required interconnection data. As each message segment of the paper tape is read, the *corresponding point* in the memory is read. If a 1 is read from the memory during this operation, the connection is good; if a 0 is read, the connection is missing and an alarm is given stating that a —WIRE condition exists between the two points being analyzed.

After the memory is read for all desired connections, it must be scanned for improper net connections. The scan operation consists of sequentially reading *every* memory location. In this case, if a 1 is read from any core, the platter point corresponding to the core

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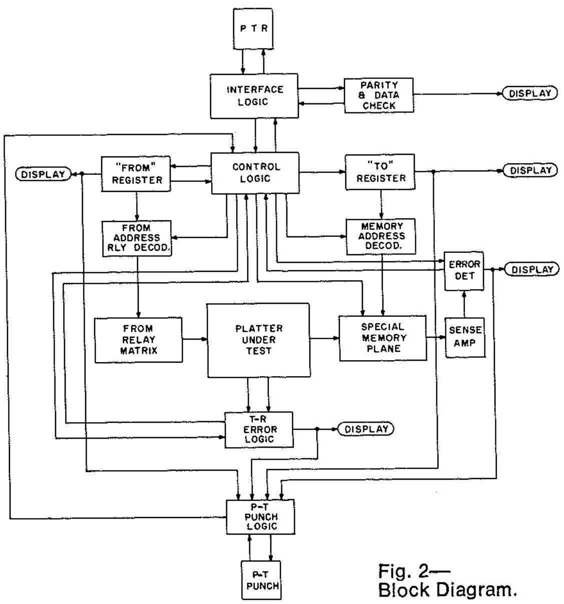

Fig. 2—
Block Diagram.

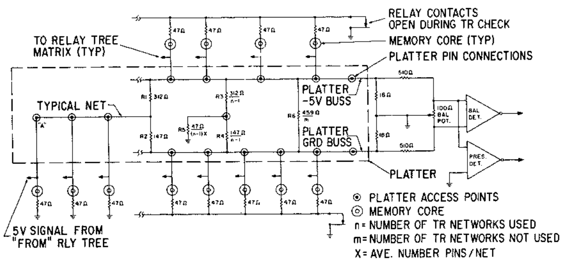

Fig. 4—TR Test Circuit.

is a +WIRE, or a shorted point, to the net under evaluation. (Note that all proper connections should have been read out and the core locations reset to the 0 state during the comparison operation). Upon complete of the memory scan, the system is ready to receive data for analysis of the next net.

Testing of the Termination Resistors

The TR test determines if the termination resistor network connected to the net has the proper resistance ratio. Fig. 5 shows a typical net and the circuitry involved in making the test. The Figure indicates a voltage applied at point *A* resulting in a current in R_1 *and* R_2. A wire is connected to the multi-turn winding of a memory core for each platter point. Connected in series with this wire is a 47-ohm resistor to the system ground. Resistor R_5 is the equivalent of all core-line resistances associated with terminated nets, excluding the net under test. Because $R_5 << R_3$ or R_4, it can be considered to be zero. The current in R_1 and R_2 is also present in R_3 and R_4, respectively, causing a voltage division ratio of $1/(n\text{-}1)$ in each path. As a result, the voltage present on the —5-volt buss equals that on the ground buss. If either R_1 or R_2 is open, or not of the proper value, a voltage imbalance occurs and is detected by the *balance detector,* indicating a TR fault.

If the TR network is not present (R_1 and R_2 missing), the voltage on both the —5-volt and ground busses will be zero. A second detector is provided to check for a voltage on the —5-volt buss and, therefore, to uncover any such faults. Thus, the logical sum of *balance ratio good* and *signal present on —5-volt buss* are required for a correct TR connection.

Errata Data

Net errors are displayed on an operating panel for both the FROM ADDRESS (the first message item of each net test sequence) and the TO ADDRESS (the platter point under analysis). A —WIRE lamp is turned on if the net is found to be open; a +WIRE lamp is energized for improper connections. In addition, a punched paper tape is automatically prepared describing the error condition found.

The TR errors are identified by displaying the address for the affected point in the net under test and the TR ERROR lamp. A punched paper tape is also prepared.

Speed of Testing

The duration of a net check depends on the number of points to be analyzed. The initial net point requires 30 ms to read-in and staticize, write into the memory, and to read out that memory location. Each successive net point requires 10 ms to read-in, staticize and read out. At the end of each net test sequence, 98 ms is required to scan the memory for improper connections.

Each TR check, regardless of the number of net points, requires 15 ms to read-in and staticize, and 40 ms to perform the test. Thus each test takes 55 ms.

A typical Spectra 70/45 BPU platter requires 155.4 seconds to completely test and consists of the following:

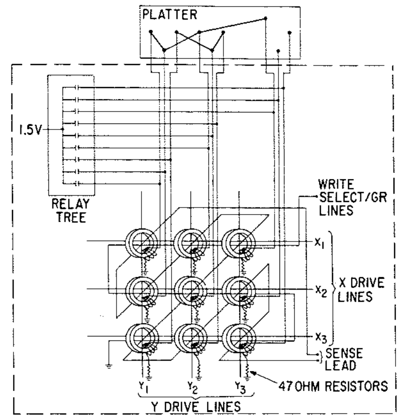

Fig. 3—Memory Connectors.

Test	*Connections*
ground	519
—5V	85
+10V	85
signal nets (averaging 3.2 pins/net)	851
termination-resistors	372

A complete continuity test of such a typical platter requires approximately 7-million logic decisions and takes 135 seconds if no platter errors are present. When platter errors are detected and punched out, each error adds 0.17 seconds to the total test time.

Input Media

The automatic platter tester operates with a punched-paper-tape input. The PTR used in the system is an RCA Model-503. The unit operates at 1,000 characters/second and was designed for use in the RCA-501 computer system.

A reed-relay matrix is used to energize signal nets because the current requirement of the memory system is small. However, in the case of voltage-buss and ground-buss nets, the currents are too high (~ 25 A) for a reed-relay matrix. Therefore, a special relay system is used to handle such nets. The format of the paper tape input is as follows:

1) Start message character;
2) Character defining type of test to be performed—
   V = voltage/ground buss test,
   S = signal net test,
   T = TR test;
3) Initial net point followed by a control character;
4) One or more successive net points to be checked, each followed by a control character except the last which has

an end message or last net point character (in the case of a TR check, only one net point is given followed by the end message character); and

5) An *end data* or platter test complete character is at the end of the tape to signal that no further tests are to be performed on the platter.

The ground buss tests are performed first because, in addition to checking ground continuity, these tests indicate whether all plugs are connected properly. To keep the test time to a minimum, the ground, voltage and signal-net checks are performed, in that order, followed by the TR checks and test termination.

Design automation aids are provided for every Spectra 70 platter. These aids include design information on two magnetic tapes: a physical master file and a pseudo-master file. The physical master file contains the following information:

Conversion tables: These tables describe the physical relationships between each pin of each connector type in a given platter. They also list voltage, ground and logic pin assignments. (TR assemblies have conversion tables similar to those for connectors).

Table of approved sockets: This table lists the location of each connector and TR assembly. Each location is classed according to the type described in the conversion tables.

Plug-in definition: This information describes each plug-in type used in the platter. The description defines each plug-in pin as source, sink, voltage, ground, etc., and lists the circuit characteristics.

Plug-in location list: This list describes the platter locations of each plug-in type defined above.

Internal pin list: This list contains the names of the signals applied to each connector pin having an internal connection in the platter.

External pin list: This list contains the names of signals applied to connector pins whose connections leave the platter by means other than the platter edge connectors.

Logical net list: The list is a combination of the two-pin lists arranged in net name sequence. The signal characteristics are tabulated along with this data.

The pseudo master file contains the following information:

Conversion tables per the physical master file.

Table of approved sockets per the physical master file.

Plug-in location list per the physical master file.

Link list by net name. This list contains the connectivity patterns of each net, i.e., the means by which one pin of a net is connected to the other pins (e.g., printed or discrete wiring).

A special design automation program, the platter checker programming system, was developed to facilitate preparation of the input paper tapes. The five steps required to generate these tapes are as follows:

1) Every pin in the pin list is assigned an address and a code which aids in the preparation of the proper test sequence.

2) The records generated in 1) are sorted according to the test order, i.e., the ground buss check is first, followed by the voltage buss check, the signal net checks, and the TR checks in that order.

3) The records generated in 1) are sorted according to actual address sequence. These records are used to generate the cross reference file.

4) This program uses the records generated by 2) and 3) to generate the test sequences on magnetic tape for Group-1 tests (platter with no discrete wiring) and Group-2 tests (platter with discrete wiring). Upon option, a cross reference print-out can be generated. The cross reference list enables the determination of a given actual address and its corresponding connector pin assignment. In addition, the cross reference list indicates the test sequence in which each pin was tested; i.e., voltage/ground buss check or signal net tests.

5) The fifth program uses the output 4) generate the actual punched paper-tapes.

Output Media

In addition to the visual display panel, a paper-tape punch is provided to record the errata data. Each error message contains the FROM point, the type of fault, and the TO point. The FROM point is the point of net access by the tester. The type of fault is given by a coded character to indicate —WIRE, +WIRE or TR WIRE. The TO point is either the point which is missing from the net, or the platter point which is shorted to the net identified by the FROM point. In TR measurements, the TO address is ignored.

The discrepancy list is a punched paper-tape containing the platter errata data which is processed by computer to obtain a tabulated listing of all platter errors. The trouble-shooter uses this information to repair and correct all indicated platter errors. This listing is also reduced by computer to permit analysis of a broad range of failure trends.

Self-Testing Features

A specially designed platter has been developed to permit rapid self-testing of all operating aspects of the automatic plater tester. After this platter is inserted into the tester, the status of the tester can be determined in five minutes.

Memory Description

The Automatic Platter Checker memory system is a special adaption of a conventional coincident current memory plane. Each platter point is connected via a wire connection to an individual multi-turn winding in each core and terminated into 47 ohms. The effective current created by the selected relay or net is approximately 40% of the total current required to switch the core. The remaining current required for switching is supplied by the write-select winding which passes through each core.

The *X*-drive line, the *Y*-drive line, and the sense winding are used only for reading only. Selection and use of these windings is as in any conventional coincident current memory. The memory cycle is 12.0 μs.

EXPANDED APPLICATIONS

Many other uses are evident for the platter checker. Some of these uses are in checking wiring the relay racks, wiring panels and cable harnesses, and in testing of unassembled plug-in units. As in any type of tester of this nature, the adaptation would require a cross reference between either the socket, connector or location numbering of the item to be checked and the numbering system of the tester, and a set of adapter cables to interface the tester with the new unit.

ACKNOWLEDGEMENTS

Mr. H. P. Cichon was the engineering group leader responsible for the design of the test equipment. The design group included: R. L. Rudolph, system design; W. M. Hoyer, memory design; W. J. DePhillipo, system timing; R. A. Hammel, Preliminary Logic Design; and M. T. Hobbs, laboratory technician.

Automation for the automobile industry

N. R. Amberg
E. J. Marcinkiewicz

RCA Industrial and Automation Systems engineers have designed many specialized testing, gauging, classifying and selective assembly machines for industry. This article describes a new machine for testing windshield wiper motors under operating conditions. A major automobile manufacturer will use this machine to improve the reliability of its product, thereby increasing automobile safety and reducing the necessity for expensive warranty replacement.

THE CURRENT EMPHASIS on automobile safety and today's liberalized and potential expensive automobile warranty programs are making high performance reliability more important to automobile manufacturers than ever before. RCA Industrial and Automation Systems engineers have designed many automatic testing, classifying, and assembling machines to help the automobile industry improve its performance reliability and reduce costs.[1] Their latest contribution is a 70-foot long machine that tests assembled windshield wiper motor drive assemblies, at the rate of 600/hour. According to an industry spokesman, it is one of the most automated testing machines ever ordered by an automobile company.

The machine checks the windshield wiper motor assembly for short circuits between the motor winding and frame, operates the assembly under load until it reaches a high operating temperature, and then checks the assembly to assure that it meets operating specifications at high and low operating speeds, with two different loads at each speed. The machine also checks to make certain the windshield wiper blade will be parked in the correct position when the assembly is later installed in an automobile. A memory and control unit keeps track of acceptance or rejection at each test, orders discontinuance of further testing if one test is failed, and reports acceptance or rejection and reason for rejection at the completion of all tests. A sound-proof booth just before the unloading position permits visual inspection and observance of operating noise level.

A view of the machine receiving finishing touches in Industrial and Automation Systems' Plymouth, Michigan plant is shown in Fig. 1. Manual pushbutton controls along the machine are for use during set up. At the loading station, an assembled motor is connected to power and control cables and placed in position on a transport pallet (Fig. 2). The operator then presses a foot switch which permits the conveyor to carry the pallet to the first test position. An interlock prevents the operator from releasing new assemblies for test if the marshalling area before the first test position is full.

As a pallet with its assembly approaches the first test position (Fig. 3) the hold-down clamps are loosely closed. The assembly then enters the test position. The pallet is raised from the conveyor by pneumatic jacks and the assembly is precisely positioned. The hold-down clamps are then tightly fastened and the check for winding-to-frame shorts in the motor is made. If this test is passed, the assembly will later receive other tests. If the test is failed, the assembly will not be tested as it passes through later test positions to avoid the possibility that further testing might damage the defective unit. The testing cycle at this first position is six seconds.

Next in line are two groups of five positions each (Fig. 4) which bring the motor up to operating temperature and simultaneously run in the brushes in preparation for the major performance checks at the group of dynamometer stations. Each assembly goes through two 30-second warmup cycles, once in each group of five stations.

Assemblies that have completed short-circuit tests are accumulated on the

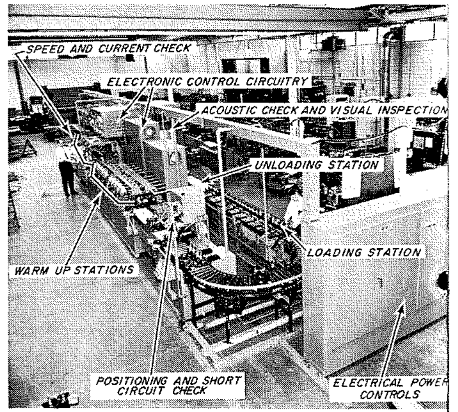

Fig. 1—The windshield wiper test machine is 70 feet long.

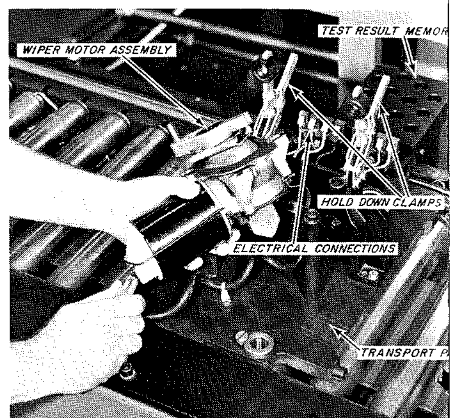

Fig. 2—The wiper motor assembly is placed on the transport pallet and connected to the power and control cables at the loading station.

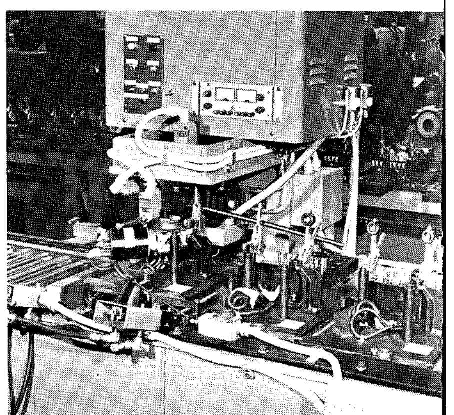

Fig. 3—The first position accurately positions the motor assembly on the pallet, clamps it in place, and checks for short circuits between the motor winding and frame.

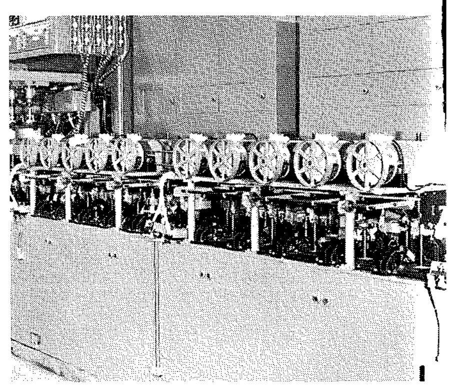

Fig. 4—Two groups of five stations bring the wiper motor assembly up to temperature and run-in the brushes prior to operational tests.

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conveyor ahead of the warmup positions until the positions are available. The first group of five positions then accepts up to five assemblies. If only a fewer number of assemblies is available, they will be tested without waiting for others. Any units which have failed the short circuit test in the first position are not warmed up but merely wait in position until the others have completed their warmup.

The pallets are raised from the conveyor by pneumatic jacks, the motor shaft is engaged and electrical connections made. A load of 100 inch-pounds of torque is applied to each motor by a powered iron magnetic brake assembly and the motor assemblies run at their high output shaft speed of about 60 r/min. Assemblies are then moved to the next group of five warmup positions where the warmup cycle under load is repeated. The warmup cycle is 30 seconds in each group of positions, including transfer time.

The warm motors then enter a group of five speed and motor current measuring stations (Fig. 5). The pallet is raised from the conveyor and electrical and mechanical connections are made. The testing machine then initiates the series of speed and current drain tests under load.

A 10-inch-pound load is supplied by an eddy current brake, and the assembly is operated at its high speed. The torque load is accurate to within 0.1 inch-pounds. Motor speed is measured by an electrical tachometer generating

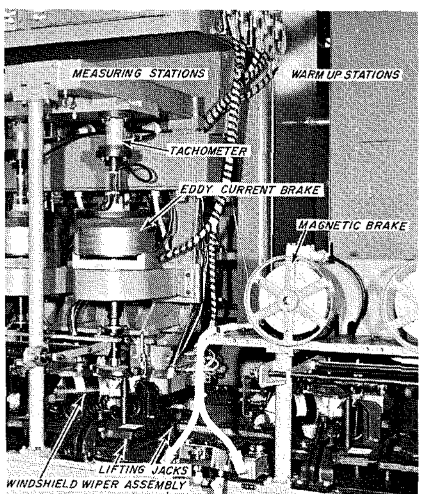

Fig. 5—The operational test positions on the left check motor speed and current drain under different operating loads.

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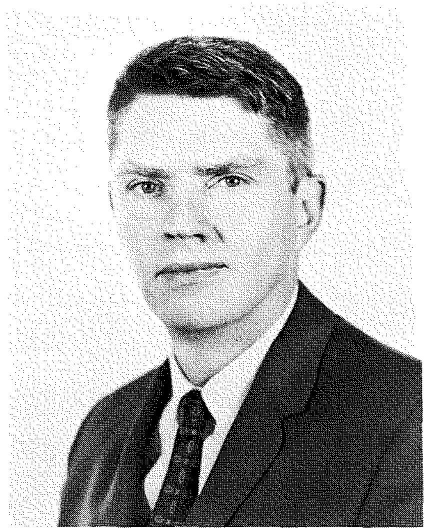
received the BS in Mechanical Engineering in 1938 from the Armour Institute of Technology, Chicago. For 12 years he was with General Motors, where he was employed in various engineering and managerial capacities in the Allison and Electro-Motive Divisions before becoming Master Mechanic. After leaving General Motors he served for 10 years as Works Manager of the Yale and Towne Material Handling Division in Philadelphia. He joined RCA in 1961 as Manager of the Industrial and Automation Department, located at that time in Detroit and since 1963 in Plymouth, Michigan.

pulses which are fed to a frequency-to-analog converter. Speed is measured to an accuracy of better than one percent. Motor current drain is measured to an accuracy of one percent. The high speed test is then repeated with a 66-inch-pound load, and speed and current drain again measured. All tests are then repeated at low speed, approximately 30 r/min. Each measurement is automatically compared with acceptance standards and a record of pass or fail for each test is entered into the pallet memory.

If the motor assembly successfully passes tests to this point, a wiper drive arm is manually added to the motor assembly. The pallet memory is automatically interrogated at the manual assembly position to determine whether the drive arm should be added.

The next automatic test determines whether the windshield wiper blade will be parked in the correct position when the assembly is installed in an



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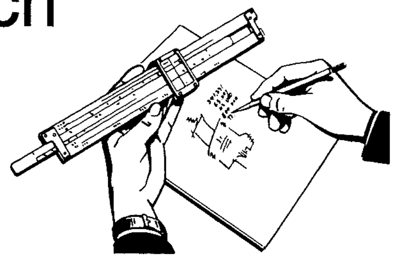
received the BS in Mechanical Engineering in Detroit Institute of Technology in 1949. His early experience included operating a private business and as a missile guidance designer for the Bendix Corporation on the Crossbow and Sparrow Projects. A project and group leader since coming to RCA in 1961, Mr. Marcinkiewicz specializes in systems and logic control design. He is credited with patents on long term presence circuits for the RCA Ve-Det vehicular control system.

automobile. This test is run without load.

The assembly then enters a quiet booth where an inspector observes a display showing whether it has passed all tests, and if not, which test it failed, resulting in discontinuation of further testing. The inspector also visually inspects the assembly and listens for noise as it is automatically operated. Defective assemblies are removed, tagged, and sent to repair at this station. Good assemblies move on to the unloading station.

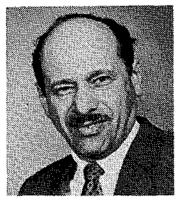
The principles demonstrated in this machine are adaptable to the testing of many mass-produced components, subassemblies, and assemblies when maintenance of high quality and the reduction of inspection costs are important. Applying these principles holds a promising future for RCA Industrial and Automation Systems, a location having electro-mechanical assets unique in RCA.

Engineering and Research Notes



Brief Technical Papers of Current Interest

BITE—Built-In Test Equipment



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Built-in test equipment (BITE) is a self-contained system for functional-level testing of equipment such as communications sets, radar sets, or computers. It provides status information with little dependence on system control. Visual GO/NO-GO displays feature capabilities of permanent retention of failure information. BITE provides easy identification of fault conditions and satisfies extremely rigid minimum down-time requirements in systems where repairs are accomplished by module or box replacement. Reduced maintenance and minimum skill requirements permit the checkout of an entire system without need of a central controller to provide stimulus and to conduct the measurements. A study of existing systems has revealed that BITE has become practical for military airborne or ground application, since ruggedized sensors and displays are available in miniature sizes. Some of the parameters that can be monitored are: voltage levels, current levels, waveforms, RF power levels, pulse trains, switch closures, and frequency or timing functions.

In BITE applications, heavy emphasis is placed on continuous or periodic status monitoring of all critical parameters; thus, faults can be detected and isolated quickly.

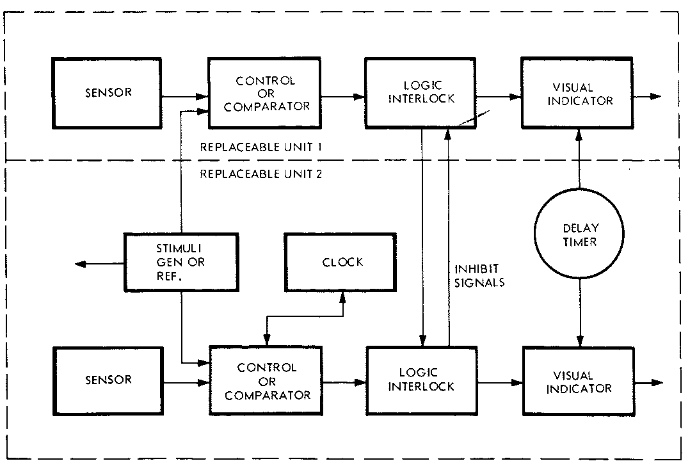

Fig. 1—Application of BITE to functional level equipment.

In some cases it may be beneficial to provide an automatic or manual ON DEMAND test. This occasion may arise when a complete functional-level equipment consisting of numerous boxes can be easily monitored; for example, when parallel indicators can be viewed side-by-side or when a failure results in a unique and obvious set of symptoms. When an unidentified NO-GO occurs, ON DEMAND tests are automatically initiated for further fault isolation.

To accomplish its objective, BITE must 1) possess a reliability factor several magnitudes greater than the prime equipment, 2) not significantly degrade system performance through failures of its own, and 3) not give false failure indications. Trigger signals must be interlocked to prevent a primary failure from triggering a chain of false indications, and precautions must be taken to prevent normal transients from triggering false indications.

If ON DEMAND manual BITE is used, it must prevent an inadvertent activation from affecting system operation. BITE must also transmit status information to facilitate central status control; usually, an open circuit represents a GO status; a closed circuit represents a NO-GO status.

To obtain the maximum benefits from BITE, the prime equipment should employ functional modular design.

Analytical Solution

The initial step in applying BITE is to determine and use the modes and probabilities of failures. Such failure analysis, along with a study of maintenance requirements, determines the following necessary information:

1) Optimum level of fault isolation,

2) Parameters to be sensed,

3) BITE logic,

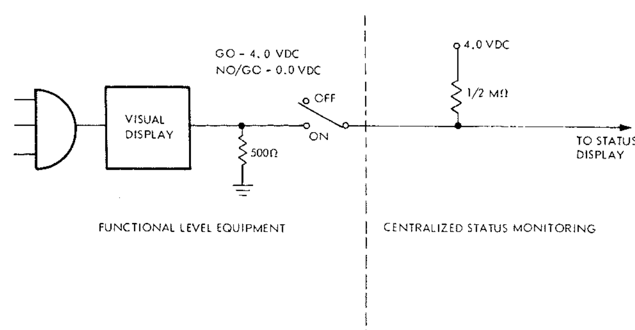

Fig. 2—Interface of BITE with a centralized monitoring system.

4) Types of sensors required,

5) GO/NO-GO tolerance of the selected parameters,

6) Tolerance of the sensor, and

7) Quantitative analysis of BITE effectiveness.

These analyses can be computer aided. The product is a signal flow diagram showing BITE configuration and how it could unambiguously isolate a fault in the proper unit.

Functional Description

The general use of BITE in functional-level equipment is represented in Fig. 1 by two replaceable units; although this number can vary, two units will suffice to show some of the inter-relationships within functional-level equipment. The functions monitored represent the detection devices for voltage, current, and power. For most applications, a stimuli generator reference is applied to a comparator for detection of suitable parameters. Outputs of the comparator are fed to a logic interlock. This functions as a device which generates inhibit signals preventing secondary effects from triggering the wrong visual indicator. In a few applications, a stimulus (e.g., a pulse) is generated and applied to the subsystem under test. The clock measures frequency or other timing functions.

The visual indicator is usually a small self-latching device weighing on the average of 6 grams, and providing a GO/NO-GO indication. In addition, status information is made available for systems applications. The delay-timer function can be combined with the clock to allow the equipment to achieve sufficient warmup time before activation of the BITE.

System Interface

BITE can be interfaced with a centralized monitoring system (Fig. 2). The functional-level equipment generates 4.0 VDC at 500 ohms for the GO condition and 0.0 VDC at 500 ohms for the NO-GO condition. In addition, 4.0 VDC is supplied at the centralized status monitoring unit through a high impedance. This arrangement allows the 4.0-VDC GO condition to be generated at the centralized status monitoring when an open exists. The GO condition at the functional-level equipment is then represented by two states: 1) 4.0 VDC, 500 ohms, and 2) equipment off, open contacts. The NO-GO condition is represented by 0.0 VDC, 500 ohms. This design prevents a NO-GO indication from being displayed for equipment intentionally turned off.

Summary

The technical features provided by BITE are:

1) Includes a visual device that retains a failure indication once activated, even through a power shutdown.
2) Yields a positive indication of failures and is interlocked so that related false failure indications do not exist.
3) Avoids trigger on normal (in operation) transients.
4) Always indicates primary failures with a design goal of indicating all secondary failures.
5) Monitors all critical parameters.
6) Does not degrade system performance to any significant level.
7) Isolates faults to a quickly replaceable unit.
8) Is fully self-contained within the functional level equipment.
9) Has a reliability factor several magnitudes greater than the prime equipment.
10) Utilizes solid-state microminiaturized design.
11) Transmits GO/NO-GO status for centralized control.

Integrated X-Band Mixer

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An X-band balanced mixer using a quadrature hybrid, was designed and fabricated in microscript with alumina as the dielectric. A matched pair of diodes, shunt mounted with opposite polarity, was used. This method of mounting has the advantage of not requiring an additional $\lambda/4$ length of the line needed for same-polarity mounting. It suffers, however, from the lack of LO noise suppression.

The image termination has some influence on the mixer noise figure. The lowest noise figure corresponds to an image frequency open circuit at the diode terminals. It does, however, introduce additional circuit complexities and limits operational bandwidth. As a first approach, both LO noise rejection and optimum image termination were traded for circuit simplicity and size reduction. The hybrid does, however, retain its LO to signal isolation. This, of course, prevents 1) the LO from reaching the antenna, 2) signal leaking into LO port, and 3) increasing of the receiver noise figure.

Design Calculations

Schottky barrier diodes, also known as hot-carrier diodes, were used in the mixer. These are majority carrier devices, so they do not suffer from charge storage. They are basically a metal-semiconductor junction device similar to the point contact diode. The cumbersome "whiskers" of the point contact diodes are replaced by a small area evaporation technique that results in a chip-form diode which can then be mounted directly on the microstrip or first encapsulated and then mounted.

Schottky barrier diodes have low excess noise and uniform forward and reverse characteristics. This makes them suitable for low-noise balanced operation. They can withstand heavy

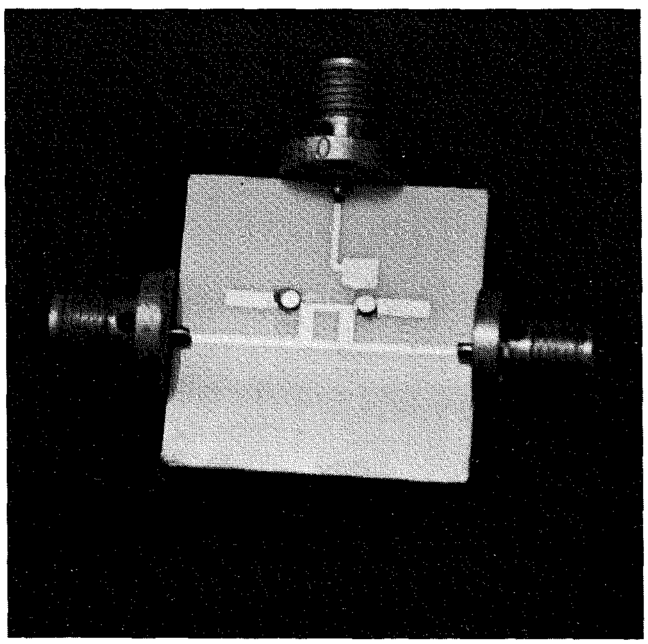


Fig. 1—X-band mixer using Hewlett-Packard HP2702 Schottky Barrier diodes.

overload and operate with large LO power without appreciable increase in the noise figure. This results in a lower intermodulation distortion and increased dynamic range.

The receiver noise figure is $NF = 10 \log L_m \; (F_{IF} + t_m - 1)$ where L_m is the mixer conversion loss ratio; t_m is the mixer noise temperature ratio; and F_{IF} is the noise figure of the IF amplifier.

For a matched image case,[1] $t_m = \frac{2}{L_m}\left[t_d \left(\frac{L_m}{2} - 1\right) + 1 \right]$

where t_d is the diode noise ratio.

It has been shown that for an ideal diode, $t_d = 1/2$. However, in the actual diodes, the ideal value is increased to $t_d = 0.85$ by the contribution from the diode series resistance.

The noise figure then becomes $NF = 10 \log [L_m \; (F_{IF} - 0.15) + 0.3]$. This shows the importance of minimizing the mixer conversion loss.

The main contribution to the conversion loss is inherent in the process of mixing, where signal power is translated into IF and image frequencies. For an ideal diode (zero forward and infinite reverse resistance) this is equivalent to 3-dB loss. The closer the diode approximates the ideal case (the higher the back-to-front resistance ratio) the lower will be its intrinsic loss. For Schottky barrier diodes this loss is approximately 4 dB.

A second source of loss lies in the diode series resistance (or its cut-off frequency, defined as $f_c = 1/R_s C_j$). It is given by

$$L_2 = 10 \log_{10} [1 + (R_s/R_o + \omega^2 C_j^2 R_s R_o]$$

where R_o is the average junction resistance over the LO cycle and C_j is the junction capacitance. This becomes minimum for $R_o = 1/\omega C_j$ and is given by $L_2 = 10 \log_{10} (1 + 2\omega \; C_j \; R_s)$.

Since R_o is a function of LO power, one can minimize the conversion loss by adjusting the power level. The optimum level is of the order of 1 mW. For lower LO power, the conversion loss and the noise figure increase rapidly, while for larger powers there is only slow deterioration.

For mixer diodes used in this application, typically $C_j = 0.35$ pF and $R_s = 8$ ohms.

Then, at 9 GHz, $L_2 = 10 \log_{10} (1 + 0.317) = 1.2$ dB.

Finally, there is the conversion loss due to mismatch at the signal and IF ports and diode and hybrid unbalance. The diode impedance depends on the LO drive (in addition to C_j and R_s). However, even for the optimum drive, the diode impedance at signal frequency has a reactive component which has to be resonated with series inductance for optimum results. At IF frequency, the parasitic elements can usually be neglected, i.e., IF impedance is resistive (100 to 200 ohms). For input and IF VSWR of 1.5, this loss contribution amounts to only 0.36 dB. Summing up all the loss contributions we have $L_m = 3.9 + 1.2 + 0.4 = 5.5$ dB. The mixer noise figure can now be calculated for a given IF noise figure. Thus, for $F_{IF} = 1.5$ dB, $NF = 10 \log [3.55 \; (1.41 - 0.15) + 0.3] = 6.8$ dB.

Final Circuit and Results

A quadrature hybrid was used in the final circuit. When tested separately, it showed excellent broadband performance. The power split was within 0.2 dB and isolation greater than 17 dB between 8 and 10 GHz. The reason for relatively low measured isolation was due to the mismatch between the OSM connector and the substrate (VSWR of 1.4). In the full receiver configuration, without the interconnection mismatch, the isolation should be improved considerably.

No attempt was made to improve the mixer performance by incorporating open circuit image termination. The LO and signal circuits were isolated from the IF circuit with a "choke" section ($\lambda/4$ low impedance open-circuited line followed by a $\lambda/4$ high impedance line. To isolate IF from the signal and LO circuits, blocking capacitors must be used. Good results were obtained with thin-film overlay capacitors. A break in the strip was etched out and then one micron of AL_2O_3 was evaporated over it and finally aluminum dot (25 mil) was evaporated.

In the full receiver configuration, the blocking capacitors may not be required if odd-mode coupled filters are used in the LO and signal circuits.

The final circuit using packaged Hewlett Packard HP2702 Schottky barrier mixers is shown in Fig. 1. The diodes were mounted in the holes drilled in the base plate and making contact to the strip at the hybrid corners. Open circuited inductive stubs ($1 > \lambda/4$) resonated the capacitive reactance of the diodes.

The noise figure of the mixer was measured (Fig. 2) with a 30-MHz IF (IF noise figure of 1.5 dB) and agreed closely with the calculated value. The LO power was adjusted at each frequency for lowest noise figure and varied between two and three mW. The LO at the signal input port was down by 15 dB. The input VSWR was 1.2 at midband.

Reference

1. Pritchard, W. L., *IRE Trans.*, MTT-3 (Jan 1955).

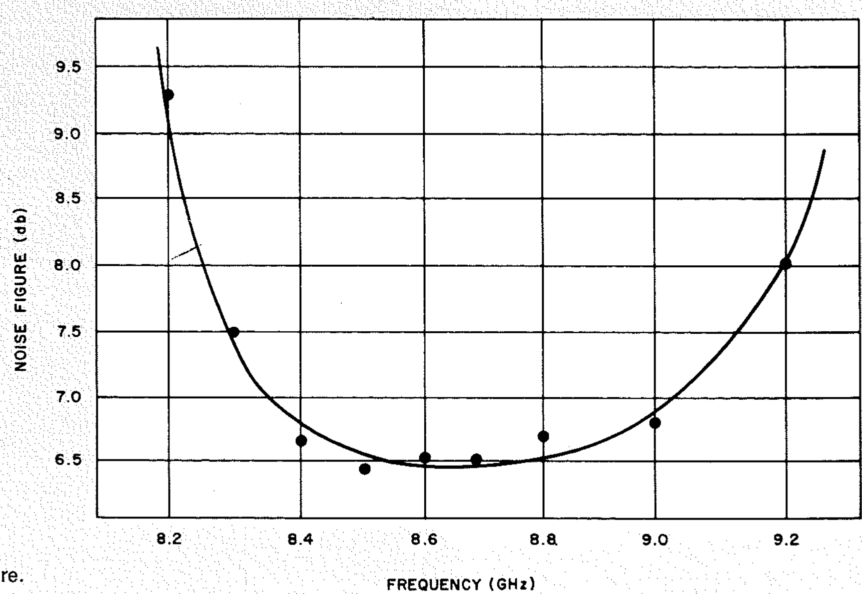
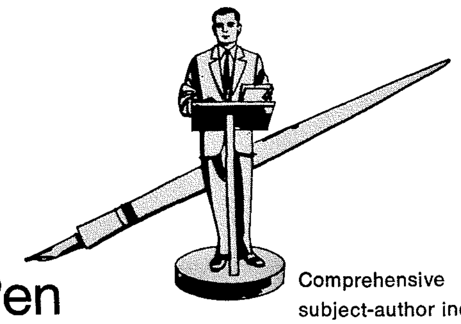


Fig. 2—Mixer noise figure.



Pen and Podium

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Subject index categories are based upon the Thesaurus of Engineering Terms, Engineers Joint Council, N.Y., 1st Ed., May 1964.

Subject Index

Titles of papers are permuted where necessary to bring significant keyword(s) to the left for easier scanning. Authors' division appears parenthetically after his name.

ACOUSTICS

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INSTRUCTIONAL TELEVISION SYSTEMS—K. C. Shaver (CESD, Cam) Comm. Technology Group, New York Chapter, 4/22/68

VIDICONS, General Uses of—R. E. Johnson (EC, Lanc) Xerox, Rochester, N.Y.; 3/26-27/68

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CATHODE-RAY STORAGE TUBE, Photo-Erasable Dark-Trace—W. Phillips, Z. J. Kiss (Labs., Pr) Solid-State Device Research Con., U. of Colo.; Boulder, Colo.; 6/17-19/68

METAL-CERAMIC PHOTOMULTIPLIERS, High Temperature Performance of—R. M. Matheson, F. A. Helvy (EC, Lanc) Scintillation Counter Symposium, Washington, D.C.; 2/28/68

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Method of Electrically Isolating Semiconductor Circuit Components—A. I. Stoller (Labs., Pr) U.S. Pat. 3,381,369, May 17, 1968

Method and Apparatus for Reading Thermoplastic Recordings—H. Borkan (EC, Som) and S. A. Ochs (EC, Lanc) U.S. Pat. 3,382,490, May 17, 1968

Method of Fabricating Semiconductor Device—F. P. Heiman (Labs., Pr) U.S. Pat. 3,387,358, June 11, 1968

Insulated Gate Field-Effect Transistor Means for Information Gating and Driving of Solid State Display Panels—J. R. Burns (Labs., Pr) U.S. Pat. 3,388,292, June 11, 1968

Gas Leak Valve Device—M. E. Moi (Labs., Pr) U.S. Pat. 3,380,473, April 30, 1968

Optical System for Use in Making Color-Phosphor Mosaic Screens—E. G. Ramberg (Labs., Pr) and D. W. Epstein (EC, Lanc) U.S. Pat. 3,385,184, May 28, 1968

Method of Fabricating Thin Film Device having Close Spaced Electrodes—P. K. Weimer (Labs., Pr) U.S. Pat. 3,385,731, May 28, 1968

Apparatus for Producing Ripple Images in Electrophotographic Record Elements Having Thermoplastic Photoconduction Layers Thereon—E. C. Giaimo (Labs., Pr) U.S. Pat. 3,382,780, May 14, 1968

Light Beam Modulation and Combination Apparatus—D. H. Pritchard (Labs., Pr) U.S. Pat. 3,383,460, May 14, 1968

Sound Translating Apparatus—A. R. Morgan (Labs., Pr) U.S. Pat. 3,383,476, May 14, 1968

Magnetic Recording of Sampled Frequency Divided Television Signals—W. D. Houghton (Labs., Pr) U.S. Pat. 3,392,233, July 9, 1968

Self-Biased Field Effect Transistor Amplifier—J. R. Burns (Labs., Pr) U.S. Pat. 3,392,341, July 9, 1968

Digital Squarer for Summing the Squares of Several Numbers by Iterative Addition—J. O. Sinninger (Labs., Pr) U.S. Pat. 3,379,865, April 23, 1968 (Patent assigned to U.S. Government)

Method for Forming of Semiconductor Devices by Masking and Diffusion—J. H. Scott (Labs., Pr) U.S. Pat. 3,383,251, May 14, 1968

DEFENSE COMMUNICATIONS SYSTEMS DIVISION

AGC for Broadband Parametric Amplifier—J. W. Daniel (DCSD, Cam) U.S. Pat. 3,388,263, June 11, 1968

Voltage Regulator Including Isolation between Input and Output—F. H. Banks, D. W. Patterson (DCSD, Ohio) U.S. Pat. 3,388,309, June 11, 1968

Output Coupling Method for Push-Pull Power Amplifier—D. A. McClure (DCSD, Cam) U.S. Pat. 3,373,373, March 12, 1968 (Patent assigned to U.S. Government)

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Card Moving Mechanism—L. W. Bleiman (ASD, Van Nuys) U.S. Pat. 3,381,956, May 7, 1968

Multipurpose Electrical Connector for Use with AC and/or DC Receptacles—H. D. Twitchell (ASD, Burl) U.S. Pat. 3,391,262, July 2, 1968

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Low Jitter Web and Tape Drive—C. Lauxen (AT, Cam) and J. F. Delany (GSD, Dayton) U.S. Pat. 3,387,758, June 11, 1968

Switching System Including Interlaced Groups of Bistable Switching Circuits—M. Cooperman (AT, Cam) U.S. Pat. 3,384,760, May 21, 1968

MISSILE AND SURFACE RADAR DIVISION

Doppler Type Correlation System—D. L. Kratzer, E. D. Carfolite (MSR, Mrstn) U.S. Pat. 3,388,398, June 11, 1968

Printed Circuit Board Assembly with Releasable Securing and Engaging Means—V. J. Poehls (MSR, Mrstn) U.S. Pat. 3,378,730, April 16, 1968

Amplitude Modulation Cancellation for Phase Modulated Correlation System—D. L. Kratzer, G. J. Armbruster (MSR, Mrstn) U.S. Pat. 3,386,094, May 28, 1968

Doppler Type Correlation System—G. H. Stevens (MSR, Mrstn) U.S. Pat. 3,386,095, May 28, 1968

Parallel Amplifiers with Input and Output Coupling by Means of Closely-Packed, Electrically Small Input and Output Radiators—F. Klawsnik, W. T. Patton (MSR, Mrstn) U.S. Pat. 3,390,333, June 25, 1968

Automatic Frequency Control—J. L. Sullivan, F. P. Papasso (MSR, Mrstn) U.S. Pat. 3,121,221 February 11, 1964 (Assigned to U.S. Government)

Precision Angle Encoder Transducer—W. S. Sepich, H. Langer (MSR, Mrstn) U.S. Pat. 3,380,048, April 23, 1968 (Patent assigned to U.S. Government)

Monopulse Tracking Radar System Capable of Locating a Plurality of Unresolved Targets—S. M. Sherman (MSR, Mrstn) U.S. Pat. 3,378,843, May 6, 1968

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Ion Pump and Scrubbing Gun for High Vacuum Apparatus—W. G. Henderson, J. T. Mark (EC, Lanc) U.S. Pat. 3,382,388, May 7, 1968

Vertical Deflection Circuit Utilizing a Single Multi-Electrode Electron Discharge Device—W. M. Austin, J. A. Dean (EC, Hr) U.S. Pat. 3,388,286, June 11, 1968

Gain Controlled Amplifier Using Field Effect Type Transistor as the Active Element thereof—W. M. Austin (EC, Som) U.S. Pat. 3,388,338, June 11, 1968

Method for Preparing a Europium Activated Yttrium Vanadate Phosphor—S. A. Harper (EC, Lanc) U.S. Pat. 3,380,926, April 30, 1968

High Power Multi-Emitter Transistor—N. C. Turner, J. H. Cavitt (EC, Som) U.S. Pat. 3,381,183, April 30, 1968

High-Frequency Power Transistor with Improved Reverse-Bias Second Breakdown Characteristics—N. C. Turner, A. F. Chen, B. R. Czorny (EC, Som) U.S. Pat. 3,383,571, May 14, 1968

Push-Pull Amplifier Circuit—C. F. Wheatley (EC, Som) U.S. Pat. 3,383,609, May 14, 1968

Aluminum Brazing—R. L. Buttle (EC, Som) U.S. Pat. 3,391,446, July 9, 1968

Bias Shift Compensation Circuitry for Transistors—W. D. Williams, Z. F. Chang (EC, Som) U.S. Pat. 3,382,445, May 7, 1968

Method of Fabricating Semiconductor Devices—A. D. Checki, B. F. Genualdi, J. Sachs (EC, Hr) U.S. Pat. 3,390,450, July 2, 1968

Method of Separating Frit Sealed Parts of an Electron Tube—M. K. Brown (EC, Lanc) U.S. Pat. 3,390,033, June 25, 1968

Semiconductor Translating Circuit—A. H. Medwin (EC, Som) U.S. Pat. 3,390,314, June 25, 1968

Transistor Protection Circuit—H. M. Kleinman (EC, Som) U.S. Pat. 3,390,345, June 25, 1968

Transistor Protection Circuit—C. F. Wheatley (EC, Som) U.S. Pat. 3,390,346, June 25, 1968

Method of Making Semiconductor Devices—S. Shwartzman (EC, Som) U.S. Pat. 3,383,760, May 21, 1968

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Logic Gate Pulse Generator—A. K. Rapp (DME, Som) U.S. Pat. 3,382,455, May 7, 1968

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Low Jitter Web and Tape Drive—J. F. Delany (GSD, Dayton) and C. Lauxen (AT, Cam) U.S. Pat. 3,387,758, June 11, 1968

Display Module Having Electromagnetic Coil Sensing of Armature Position—E. D. Simshauser (GSD, Dayton) U.S. Pat. 3,381,291, April 30, 1968

Professional Meetings

Dates and Deadlines

Be sure deadlines are met—consult your Technical Publications Administrator or your Editorial Representative for the lead time necessary to obtain RCA approvals (and government approvals, if applicable). Remember, abstracts and manuscripts must be so approved BEFORE sending them to the meeting committee.

Calls for papers

OCT. 2-4, 1968: **Allerton Conference on Circuit & System Theory,** G-CT, G-AC, Univ. of Illinois, Allerton House, Monticello, Illinois. **Deadline info: 8/1/68 (sum and abst) to:** T. N. Trick.

OCT. 10-11, 1968: **Symposium on Applications of Ferroelectrics,** Catholic Univ. of America, G-IM, G-SU, Catholic Univ. of America, Wash., D.C. **Deadline info: 7/1/68 (abst) to:** H. L. Stadler, Physical Elec., Dept., Ford Motor Co., Dearborn, Mich.

OCT. 15-17, 1968: **Switching & Automata Theory Symposium,** G-C, Rensselaer Polytechnic Inst., Schenectady, N.Y. **Deadline info: 5/17/68 (abst) to:** S. B. Akers, Jr., Elec. Lab., Gen'l Elec. Co., Syracuse, N.Y. 12301.

OCT. 23-25, 1968: **Int'l Electron Devices Meeting,** G-ED, Sheraton Park Hotel, Washington, D.C. **Deadline info: 8/1/68 (abst) to:** D. A. Chisholm, Bell Telephone Labs., MH2A-229, Murray Hill, N.J. 07971.

OCT. 28-30, 1968: **Applied Superconductivity Conf. & Exhibition,** G-MAG, Oak Ridge Nat'l Lab., U. S. - A. E. C., A. P. S., Riverside Motel & Gatlinburg Audit, Gatlinburg, Tenn. **Deadline info: 8/5/68 (abst) to:** A. Paskin, Brookhaven Nat'l Lab., Upton, L.I., N.Y.

OCT. 30-NOV. 1, 1968: **Asilomar Conf. on Circuits & Systems,** Naval P. G. School, Santa Clara Univ., G-CT, G-AC, Asilomar Hotel & Conf. Grounds, Pacific Grove, Cal. **Deadline info: 9/13/68 (abst and sum) to:** Shu-Gar Chan, Code 52 Cd, Dept. of EE, Naval P. G. Sch., Monterey, Cal. 93940.

NOV. 17-21, 1968: **Magnetism & Magnetic Materials Conference,** G-MAG, AIP, New York Hilton Hotel, New York, N.Y. **Deadline info: 8/12/68 (abst) to:** R. C. Barker, Yale Unv., 10 Hillhouse Ave., New Haven, Conn. 06520.

DEC. 2-4, 1968: **Reliability Physics Symposium,** G-R, G-ED, Washington Hilton Hotel, Washington D.C. **Deadline info: 8/15/68 (abst.) to:** Adolf Goetzberger, Bell Telephone Labs., Murray Hill, N.J. 07971.

DEC. 4-6, 1968: **Circuit Theory Symposium,** G-CT, Hotel Hilton Plaza, Miami Beach, Florida. **Deadline info: 8/1/68 (papers) to:** B. Kinariwala, Univ. of Hawaii, Honolulu, Hawaii 96822.

DEC. 8-12, 1968: **Electrical Insulation Conference - West Coast,** G-EI, NEMA, NAVSEC, Biltmore Hotel, Los Angeles, Cal. **Deadline info: 12/22/67 (papers) to:** Robt. Kaplan, Electra Motors Div. of Litton Ind., 1110 Lemon St., Anaheim, Cal.

DEC. 9-11, 1968: **Nat'l. Electronics Conference,** Region 4, et al, Conrad Hilton Hotel, Chicago, Illinois. **Deadline info: 8/1/68 (papers) to:** Nat'l Electronics Conf.

JAN. 26-31, 1969: **Winter Power Meeting,** G-P, Statler Hilton Hotel, New York, N.Y. **Deadline info: 9/15/68 (papers).**

JAN. 28-31, 1969: **Int'l Symposium on Information Theory,** G-IT, Nevele Country Club, Ellenville, New York. **Deadline info: 9/15/68 (abst) to:** David Slepian, Dept. of Transportation, Washington, D.C.

APRIL 11-14, 1969: **Semiconductor Device Research Conference,** German Section of IEEE, DPG, VDE, NTG, Munich, F. R. Germany. **Deadline info: 12/15/68 (papers) to:** W. Heywang, Balanstrasse 73, 8 Muenchen 80, R. R. Germany.

APRIL 23-24, 1969: **Electric Process Heating in Industry Conference,** G-IGA, Phila., Section, Marriott Motor Hotel, Philadelphia, Penna. **Deadline info: 11/1/68 (abst) to:** George Bobart, Westinghouse Elec. Corp., Box 300, Sykesville, Md.

MAY 12-16, 1969: **Underground Distribution Conference, G-P,** Anaheim Conv. Ctr., Anaheim, California. **Deadline info: 7/1/68 (abst) 12/1/68 (papers) to:** W. A. Thue, Florida Power & Light Co., POB 3316, Miami, Fla. 33101.

MAY 18-21, 1969: **Power Industry Computer Application Conference,** G-P, Brown Palace Hotel, Denver, Colorado. **Deadline info: 11/15/68 (abst) to:** W. D. Trudgen, Gen'l. Elec. Co., 2255 W. Desert Cove Rd. POB 2918, Phoenix, Ariz. 85002.

MAY 26-28, 1969: **Laser Engineering & Applications Conference,** G-ED, G-MTT, Washington Hilton Hotel, Washington, D.C. **Deadline info: 1/17/69 (sum and abst) to:** W. B. Bridges, Hughes Labs., 3011 Malibu Canyon Rd., Malibu, Cal.

JUNE 22-27, 1969: **Summer Power Meeting,** G-P, Sheraton Dallas Hotel, (Dallas, Texas. **Deadline info: 2/15/69 (papers) to:** J. R. Wilson, Gen'l Elec. Co., POB 5821, Dallas, Texas.

JULY 20-25, 1969: **Engrg. in Medicine & Biology & Int'l Fed. for Medical & Biological Engineering Conference,** G-EMB, JCEMB, Palmer House, Chicago, Illinois. **Deadline info: 2/1/69 (papers) to:** Lawrence Stark, Univ. of Illinois, Chicago, Illinois.

Meetings

SEPT. 5-6, 1968: **3rd Annual Convention of the Society of Logistics Engineers,** Ambassador Hotel, Los Angeles, California. **Prog Info:** G. F. Fairhurst, RCA West Coast Division, Van Nuys, California.

SEPT. 9-12, 1968: **Int'l Symposium and Fall USNC/URSI Meeting, G-AP, URSI,** Northeastern Univ., Boston, Mass. **Prof. Info:** Leon Ricardi, Lincoln Lab., MIT, Lexington, Mass.

SEPT. 9-13, 1968: **International Broadcasting Convention, IEE,** U. K. & Rep. of Ire. Sec., IERE, Royal Television Society et al, Grosvenor House Hotel, London, England. **Prog Info:** R. G. Cox, IEE, Savoy Place, London, W. C. 2, England.

SEPT. 12-13, 1968 **Solid State Sensors Symposium, G-ED,** Twin Cities Section, ISA, Leamington Hotel, Minneapolis, Minnesota. **Prog Info:** M. M. Atalla, Hewlett-Packard, 1501 Page Mill Road, Palo Alto, Calif. 94304.

SEPT. 15-19, 1968: **Joint Power Generation Conference, G-P, ASME,** Jack Tar Hotel, San Francisco, California. **Prog. Info:** D. M. Sauter, Westinghouse Elec. Corp., E. Pittsburgh, Penna. 15112.

SEPT. 16-20, 1968: **Int'l Conf. on Microwave & Optical Generation & Amplification,** German Section of IEEE, VDE, & NTG, Univ. of Hamburg, F. R. Germany. **Prog. Info:** W. A. Krause, 2 Hamburg 11, F. R. Germany, Delmannstr 1/3, Hafenbau.

SEPT. 17-19, 1968: **Tube Techniques Conference, G-ED,** United Engineering Center, New York, N.Y. **Prog. Info:** George Freedman, Raytheon Co., Waltman, Mass.

SEPT. 19-21, 1968: **Fall Broadcast Symposium, G-B,** Mayflower Hotel, Washington, D. C. **Prog. Info:** IEEE Headquarters, 345 East 47th Street, New York, New York 10017.

SEPT. 23-27, 1968: **Electronics Design Conference, IEE,** U. K. & Rep. of Ireland Section, IERE, Univ. of Cambridge, England.

SEPT. 25-27, 1968: **Ultrasonics Symposium, G-SU,** Statler Hilton Hotel, New York, N. Y. **Prog. Info:** R. W. Damon, Sperry Rand Res. Ctr., Sudbury, Mass. 01776.

SEPT. 29-Oct. 2, 1968: **IGA Group Annual Meeting, G-IGA,** La Salle Hotel, Chicago, Illinois. **Prog. Info:** R. W. Mills, Rel. Elec. & Engrg. Co., 24701 Euclid ave., Cleveland, Ohio 44117.

OCT. 3-4, 1968: **2nd Annual ACM PL/I Forum, Association for Computing Machinery,** 211 East 43 Street, New York, N.Y. 10017. **Prog. Info:** R. F. Rosin, Computer Science Department, SUNY, 4250 Ridge Lea Rd., Amherst, N.Y. 14226 before Sept. 1, 1968.

OCT. 6-11, 1968: **Electrochemical Society,** New York, Queen Elizabeth Hotel, Montreal, Canada. **Prog Info:** Electrochemical Society, 30 East 42nd Street, New York, N. Y. 10017.

OCT. 14-15, 1968: **Thermionic Energy Conversion Specialists Conference, G-ED,** Framingham Motor Inn, Framingham, Massachusetts. **Prog Info:** J. E. Kemme, Los Alamos Scientific Res. Labs., POB 608, San Diego, California.

OCT. 14-16, 1968: **System Science & Cybernetics Conference, G-SCC,** Towne House, San Francisco, Calif. **Prog Info:** Hugh Mays, Fairchild Semiconductor R&D Labs., 4001 Juniper Serra Blvd., Palo Alto, California 94304.

OCT. 20-22, 1968: **Nat'l Convention of Electrical & Electronic Engineers in Israel,** Israel Section of IEEE, Israel Inst. of Technology, Tel-Aviv, Israel. **Prog Info:** I. Cedarbaum, Tech. Israel Inst. of Tech. POB 4910, Haifa, Israel.

OCT. 23-25, 1968: **Nuclear Science Symposium, G-NS,** Bonaventure Hotel, Montreal, Quebec, Canada. **Prog Info:** O. L. Tiffany, Bendix Sys. Division, 3300 Plymouth Rd., Ann Arbor, Mich.

OCT. 31-NOV. 2, 1968: **Photo-Electronic Imaging Symposium,** Marriott Twin Bridges Motor Hotel, Washington, D.C. **Prog Info:** Robert A. Jones, Papers Chairman, Mail Station 68, The Perkin-Elmer Corporation, Norwalk, Connecticut 06852.

NOV. 6-8, 1968: **Northeast Electronics Research & Engineering Meeting (NEREM),** New England Sections, Sheraton Boston Hotel, War Mem. Auditorium, Boston, Mass. **Prog. Info:** IEEE Boston Office.

NOV. 6-8, 1968: **West Coast Conference on Broadcasting,** G-B, Ambassador Hotel, Los Angeles, Cal. **Prog. Info:** F. R. McNichol, RCA, 2700 W. Olive, Burban, Calif. 91505.

NOV. 7-8, 1968: **Canadian Symposium on Communications,** Canadian Region, Montreal Section, Queen Elizabeth Hotel, Montreal, Quebec, Canada. **Prog Info:** Alain Breton, POB 802 Station B, Montreal 2, Quebec, Canada.

NOV. 12-14, 1968: **Automatic Support Sys. for Advanced Maintainability Symposium,** St. Louis Section, G-AES, Sheraton Jefferson Hotel, St. Louis, Missouri. **Prog Info:** D. L. Reed, Emerson Elec., 8100 W. Florissant Ave., St. Louis, Mo. 63136.

NOV. 17-21, 1968: **Conference on Engineering in Medicine & Biology, G-EMB, JCEMB,** Shamrock Hilton Hotel, Houston, Texas. **Prog Info:** L. E. Baker, Baylor Univ. Col. of Med., 1200 Moursund Ave., Houston, Tex. 77025.

NOV. 18-20, 1968: **7th Region III IEEE Convention,** Region III, Canaveral Section, Ramada Inn, & Quality Courts, Cocoa Beach, Fla. **Prog info:** R. L. Walker, Univ. of Florida, Gainesville, Fla.

NOV. 19-21, 1968: **Photovoltaic Specialists Conference, G-ED,** Jet Propulsion Lab., Pasadena, Calif. **Prog Info:** R. E. Fischell, Applied Phys. Lab., Johns Hopkins Univ., 8621 Georgia Ave., Silver Spring, Md.

DEC. 1-5, 1968: **Annual Winter Meeting of the Rubber and Plastics Division** of the American Society of Mechanical Engineers, Hilton Hotel, New York City. **Prog Info:** R. H. Skidmore, Welding Engineers, Inc., Norristown, Pennsylvania 19404.

DEC. 2-4, 1968: **Applications of Simulation Conference,** G-C, G-SSC, ACM, SHARE, SCI, Roosevelt Hotel, New York, N.Y. **Prog Info:** Arnold Ockene, IBM, 112 E. Post Road, White Plains, New York 10601.

DEC. 3-4, 1968: **Vehicular Technology Conference, G-VT,** San Francisco Hilton Hotel, San Francisco, Calif. **Prog Info:** Wm. Chaney, Lenkurt Elec. Co., 1105 Country Rd., San Carlos, Calif. 94070.

DEC. 9-10, 1968: **Consumer Electronics Symposium, G-BTR, G-AE, G-ED,** Conrad Hilton Hotel, Chicago, Illinois. **Prog. Info:** Don Ruby, Zenith Radio Corp., 6001 W. Dickens Ave., Chicago, Ill. 60639.

DEC. 9-11, 1968: **Fall Joint Computer Conference,** G-C, AFIPS, San Francisco Hilton Hotel & Civic Ctr., San Francisco, Calif. **Prog Info:** AFIPS Hdqs.

DEC. 16-18, 1968: **Adaptive Processes Symposium, UCLA, G-Ac, G-IT, G-SSC,** Univ. of Cal. at L. A., Los Angeles, Calif. **Prog Info:** J. M. Mendel, Douglas Aircraft Co. Inc., 3000 Ocean Pk. Blvd., Santa Monica, Calif.

JAN. 21-23, 1969: **Reliability Symposium,** G-R, ASQC, IES, SNT, Palmer House, Chicago, Illonois. **Prog. Info:** J. E. Condon, Office of Reliability & Quality Assurance, NASA Hdqs., Washington, D.C.

Engineering News and Highlights

Ken Bucklin Retires

Kenneth G. Bucklin, who has been Manager, Commercial Engineering, RCA Electronic Components, since 1963, retired recently after 35 years of service with the company. His organization is responsible for the preparation, publishing and distribution of all technical publications concerning RCA's several thousand electronic components. Many of the receiving tubes which he designed and developed are still used today in radios and TV sets.

Mr. Bucklin received the BS in electrical engineering from M.I.T. and joined the RCA Electron Tube Division in 1933. In 1939, he became Manager, Receiving Tube Design. Between 1942 and 1953, he served in several merchandising and administrative positions. In 1953, Mr. Bucklin was appointed Manager for Receiving Tube and Transistor Marketing. During the following year, he was made Manager, Receiving Tube Marketing, and later became Manager, Market Planning—Receiving Tubes. In 1958, he was named Manager, Receiving Tube Engineering and two years later became Manager, New Products Engineering. In May of 1962, Mr. Bucklin became Administrator, Tubes and Semiconductor Engineering Liaison. Mr. Bucklin is a Senior Member of the Institute of Electrical and Electronics Engineer and a member of the Amateur Radio Relay League.

RCA Gets $7.4 Million Contract for Field Automatic Test Equipment

As this issue goes to press, the award of a $7.4 million U.S. Army contract to produce automatic test and repair equipment for in-the-field support of surface-to-surface tactical missile systems was announced. Under the contract, RCA will produce five Land Combat Support Systems (LCSS) for the Army Missile Command. The articles in this issue by Turkington, Bokros, Stockton and Douglas, Barry, and Mattison and Mitchell cover various aspects of this system.

Contents: June 1968 *RCA Review*

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	DOMESTIC	FOREIGN
1-year	$4.00	$4.40
2-year	7.00	7.80
3-year	9.00	10.20

New Engineering Facilities at AED

A new facility presently under construction at AED will permit the fabrication of thin-film hybrid circuits, primarily for use in microwave systems such as retro-directive microwave antenna arrays. This work is a follow-on to the Blue Chip Program. Capabilities will include pattern generation by photo-resist chip and wire bonding and encapsulation.

Professional Activities

Electronic Components, Lancaster, Pa.

New Officers of the Lancaster Engineering Education Committee for 1968-1969: Chairman, **J. M. Forman**, Manager of Environmental, Special Equipment and Specification Engineering; 1st Vice-Chairman, **A. F. McDonie**, Manager of Production Engineering — Phototubes; and 2nd Vice-Chairman, **J. T. Mark**, Manager of Regular Power Devices Design Engineering. **A. P. Sweet**, P.E., Administrator of Power Tube Marketing has been elected as a Chapter Director of Lincoln Chapter, PSPE, for a three-year term beginning 6/1/68. Mr. Sweet has also been appointed as the Chairman of the Chapter Engineer in Industry Committee.

New Business Programs

Howard C. Lawrence of the Vehicular Traffic Systems activity has recently been appointed to the Electronic Industries Association (EIA) Transportation Committee.

Electromagnetic and Aviation Systems Division

R. H. Aires, Chief Engineer, has been elected Chairman of the IEEE San Fernando Valley Section for 1968. Mr. Aires, an active supporter of IEEE since his student days, was Vice Chairman of the section in 1967 at which time he served as Chairman, Engineer's Week Committee for the San Fernando Valley. He is presently also a Director of the San Fernando Valley Engineers' Council.

G. F. Fairhurst, Manager of Engineering Support has been selected as General Chairman of the Society of Logistics Engineers for their 3rd Annual Convention, which will be held in Los Angeles on September 5 and 6, 1968. Mr. Fairhurst is a charter member of this international society which has over 2000 members.

Astro-Electronics Division

B. P. Miller was elected Chairman of the Princeton Section of the AIAA for the period of June 1968 to June 1969.

Defense Advanced Communications Laboratory

Dr. Wen Y. Pan, Manager of Advanced Solid-State Techniques, was chairman for the 1968 Seminar on Modern Engineering and Technology and **Steve Yuan**, Leader, Technical Staff, was Executive Secretary for the conference which was held through July 10 in Taiwan, China. Both men's participation in the seminar is at the invitation of **Dr. C. K. Yen**, Vice President of the Republic of China and T. K. Li, Minister of Chinese Economic Affairs.

Aerospace Systems Division Holds First Annual Authors Reception

Recently, the Aerospace Systems Division cited "those members . . . who have increased their professional stature and have added to RCA's prestige through publication of technical papers during 1967." Forty-seven authors, with their wives, were honored at the reception held at Anthony's Pier Four restaurant in Boston, Mass.

Staff Announcements

Robert W. Sarnoff, President, announced the responsibilities for certain RCA Staff activities are realigned as follows: **Chase Morsey,** Vice President, Marketing, will assume responsibility for Advertising and Sales Promotion, Corporate Identification, Distributor and Commercial Relations, Economic and Market Research, New Business Programs, Product Planning Coordination, Systems Development; **Barton Kreuzer,** Vice President and General Manager, Commercial Electronics Systems Division, will assume responsibility for the Industrial and Automation Systems Department; **T. A. Smith,** Executive Vice President, will devote his full attention to the field of education in association with **C. V. Newsom,** Vice President, Education. Mr. Sarnoff also announced the election of **G. A. Fadler,** Vice President, Manufacturing Services and Materials.

Chase Morsey, Vice President, Marketing, announced the Marketing organization as follows: **M. F. Bennett,** Vice President, Distributor and Commercial Relations; **R. J. Eggert,** Staff Vice President, Economic and Market Research; **F. H. Erdman,** Staff Vice President, New Business Programs; **M. Gaffin,** Director, Corporate Identification; **T. G. Paterson,** Manager, Systems Development.

K. W. Bilby, Executive Vice President, Public Affairs, announced the International Washington office and the Investor Relations activity will become the responsibility of the Public Affairs organization with **J. N. Plakias,** International Washington Representative reporting to **D. E. Ewing,** Vice President, Washington and **J. A. Gearhart,** Manager, Investor Relations, reporting to the Executive Vice President, Public Affairs.

M. Gaffin, Director, Corporate Identification appointed **B. O'Neill** Manager, Graphic Design to report to the Director, Corporate Identification.

B. V. Dale, Manager, Automatic Test and Measurement Systems announced the appointment of **W. S. Wu** to the newly created position of Manager, Advanced Test Systems Engineering.

Electronic Components

Dr. David W. Epstein, Manager, Conversion Tube Operations, announced the appointment of **Dr. Ralph E. Simon,** Director of the RCA Conversion Devices Laboratory at the David Sarnoff Research Center, Princeton, N.J.

Defense Electronic Products

I. K. Kessler, Vice President, Defense Electronic Products, announced the name of the West Coast Division is changed to the Electromagnetic and Aviation Systems Division. **S. Sternberg** will continue as Division Vice President and General Manager. **S. N. Lev,** Division Vice President and General Manager, has appointed **James M. Osborne** as Manager of Marketing for RCA's Defense Communications Systems Division, Camden, N.J. Mr. Osborne also continues as Manager, Secure Communications Programs for RCA DEP.

Commercial Electronic Systems Division

B. Kreuzer, Vice President and General Manager announced the appointment of **A. Mason** as Chief Engineer.

N. R. Amberg, Manager, Industrial and Automation Systems Department announced the organization of the Industrial and Automation Systems Department as follows: **H. E. Colestock,** Manager, Engineering; **C. A. Della Bella,** Manager, Internal Automation Programs; **R. O. Graham,** Manager, Purchasing; **M. G. Kopasz,** Manager, Financial Operations; **G. A. McAlpine,** Manager, Industrial Automation Equipment Marketing; **M. A. Scherrens,** Plant Manager, Plymouth Plant; **H. C. Wacker,** Administrator, Personnel, **M. Wylie,** Manager, Equipment Installation.

Information Systems Division

James R. Bradburn, Executive Vice President, RCA Information Systems announced the appointment of **John R. Lenox** to the newly created position of Division Vice President, Manufacturing and Engineering, Information Systems Division.

E. R. Dickey, Manager, Corporate Information Systems Centers announced the appointment of **Murrel G. Freeman** as Manager, RCA Corporate Data Processing Center, West Coast.

Instructional Systems

M. H. Glauberman, Director, Instructional Systems announced the appointment of **G. R. Jensen** as Manager, Marketing. Mr. Jensen will report to the Director, Instructional Systems.

Awards

Aerospace Systems Division

Jay Prager won first prize in the IEEE Metropolitan Student Prize Paper Contest, held in New York City.

The Technical Excellence Committee announced that **James A. McNamee,** Member, Technical staff, Automatic Test Equipment Engineering, has been selected as May Engineer of the Month in recognition of Mr. McNamee's notable achievements on the Patchboard Product Improvement Study for the LCSS Program.

The Technical Excellence Committee has chosen the TVATE Team from Radar Engineering as the May Team of the Month for its outstanding work in modifying the Transponder Vendor Acceptance Test Equipment for the LM program. The members of the TEAM are **A. H. Williams, R. DePierre, W. J. Wagner, R. F. Wade, D. W. Fogg** and **R. P. Morin.**

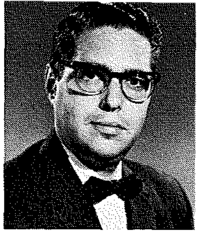
Missile and Surface Radar

The following M&SR engineers have been cited for their performance for the First Quarter of 1968 as follows:

D. D. Keys—For outstanding performance in resolving complex system and hardware problems on the Apollo Ships Radar Acquisition Modification and SHF Airborne Antenna Subsystem Programs. **D. J. Oseroff**—For outstanding performance in development and application of data processing techniques to meet specialized reentry data requirements for the SPARTA Program. **G. H. Stevens**—For his original contributions in the area of advanced radar signal processing techniques. **S. C. Stribling**—For his outstanding technical performance in the analytical and operational aspects of the SPARTA program.

Degrees Granted

E. A. Czeck, EC, Mntp	MS, Physics, Wilkes College, 6/68
J. T. Gershey, EC, Mntp	MS, Physics, Wilkes College, 6/68
A. C. Limm, EC, Som	MS, Physics, Wilkes College, 6/68
F. P. Lokuta, EC, Mntp	MS, Physics, Wilkes College, 6/68
V. J. Nardone, EC, Mntp	MS, Physics, Wilkes College, 6/68
V. S. Osadchy, EC, Mntp	MS, Physics, Wilkes College, 6/68
M. A. Owen, EC, Hr	MS, Business Administration, Rutgers, 5/68
J. Mirkin, AED, Pr	MSEE, City College of New York, 5/68
W. Fuldner, AED, Pr	MSEE, University of Pennsylvania, 5/68
P. H. Brandt, AED, Pr	MSEE, University of Pennsylvania, 5/68
R. Conklin, AED, Pr	MSEE, New College of Engineering, 6/68
M. Hecht, AED, Pr	PhD, Electrical Engrg., Polytechnic Institute of Brooklyn, 6/68
T. N. Altman, AED, Pr	MSEE, Polytechnic Institute of Brooklyn, 6/68
R. Bernal, AED, Pr	MSEE, Polytechnic Institute of Brooklyn, 6/68
P. D. Curran, AED, Pr	MS, Aerospace Engineering, Rutgers University, 6/68
J. D. Geller, AED, Pr	MS, Mechanical Engrg., Drexel Institute of Technology, 6/68
J. F. Seliga, AED, Pr	MSEE, Drexel Inst. of Technology, 6/68
F. E. Oliveto, DCSD, Cam	MS, Engineering Statistics, Villanova U., 6/68
A. A. Vallorani, DCSD, Cam	MS, Engrg. Management, Drexel Inst. of Tech., 6/68
W. J. Stotz, AT, Cam	MSEE, Drexel Inst. of Technology, 6/68
E. L. Donaldson, MSR, Mrstn	BS, Electronic Physics, LaSalle College, 6/68
A. A. Raguckas, MSR, Mrstn	MSME, U. of Pennsylvania, 6/68
D. C. McCarthy, MSR, Mrstn	MS, Engrg. Management, Drexel Inst. of Tech., 6/68
S. L. Abbott, MSR, Mrstn	MSEE, Drexel Inst. of Tech., 6/68
S. Castrovillo, MSR, Mrstn	BSEE, Penn Morton College, 6/68
A. Homan, MSR, Mrstn	MSEE, Drexel Institute of Technology, 6/68
A. P. Moll, MSR, Mrstn	MSEE, U. of Pennsylvania, 6/68
F. I. Palmer, MSR, Mrstn	MSEE, Drexel Inst. of Tech., 6/68
R. J. Tomsic, MSR, Mrstn	MSEE, Drexel Inst. of Tech., 6/68



Kaminsky

Colestock

New TPA's and Ed Rep Appointed

Murray Kaminsky has been appointed as Technical Publications Administrator for the Information Systems Division; and **E. J. Williamson** is the TPA for RCA Communications, Inc. Messrs. Kaminsky and Williamson will be responsible for the review and approval of technical papers; for coordinating the technical reporting program; and for promoting the preparation of papers for the RCA ENGINEER and other journals, both internal and external. **H. Colestock,** as Editorial Representative for Industrial and Automation Systems, will assist D. R. Pratt who is the TPA for CESD. Mr. Kaminsky is an engineering leader in the Information Systems Division responsible for qualifying new communications devices for the 70/668 and for designing and testing special features for this equipment. He joined RCA in June, 1958, and earned the MSEE at the U. of Pa. while participating in the graduate study program. Some of his assignments have been the design of a photovoltaic sensing system for an advanced model card reader; the design of a time generator for the RCA 301 and 3301 equipments; the design of the Model 6009 Autodin Buffer; and a significant portion of the design of the data communications equipment for the Spectra 70 product line.

Mr. Colestock is manager of engineering for Industrial and Automation Systems. He received the BSEE from the U. of Michigan and has over twenty years of experience in Electronics and Industrial Automation. Before joining RCA, he was a Program Manager for the Systems for the Aerospace Industry Division of the Bendix Corp. Prior to joining the Bendix Corp., Mr. Colestock was a Manager of Engineering for the Burroughs Corp.; Chief Engineer for Weltronic Corp.; Plant Engineer for the Pontiac Division of General Motors; and Test Engineer for General Electric Corp.

A photograph and biography of Mr. Williamson will appear in the next issue of the RCA ENGINEER.

Promotions

to engineering leader and manager

As reported by your Personnel Activity during the past two months. Location and new supervisor appear in parentheses.

RCA Communications, Inc.

Dominick Mandato: from Group Leader to Manager, Special Systems Design (J. C. Hepburn, Special Systems Design)

Edwin J. Williamson: from Group Leader to Manager, Engineering Services (J. C. Hepburn, Engineering Services)

Samuel N. Friedman: from Design Engineer to Manager, Equipment Design (J. C. Hepburn, Equipment Design)

Consumer Electronics Division

J. A. McDonald: from Member, Engineering Staff to Leader, Engineering Staff, (G. F. Rogers, Indpls.)

RCA Service Company

C. O. Thomas: from Ship Instrumentation Engineer—Shipboard to Manager, Communication & Telemetry—Shipboard (M. J. Van Brunt, MTP, Cocoa Beach, Florida)

B. Pinsky: from Systems Service Engineer to Leader, Systems Service Engineer (W. E. Crawford, Aerospace Support Systems, Burlington, Mass.)

A. W. Brittingham: from Network Support Engineer to Manager, Technical Assistance Group (E. J. Lauden, MTP, Cocoa, Florida)

W. Slawinski: from Engineer—BMEWS to Leader, Engineers—BMEWS (G. H. Perry, Systems Maintenance Control, Thule, Greenland)

R. R. Balon: from System Service Engineer to Manager, Control Center—NIMBUS (W. W. Powell, Field Projects—STADAN, Greenbelt, Md.)

W. A. Price: from Engineer to Manager, Optics Engineering (K. Wenz, MTP, Cocoa Beach, Florida)

R. D. Gailor: from Associate Ship Instrumentation Engineer—S to Manager, Radar—S (M. J. Van Brunt, MTP, Cocoa Beach, Florida)

B. A. Barnwell: from Leader, Engineers to Manager, Mission Planning & Eng. (R. S. Maloney, Andros Island)

Electronic Components

H. L. Palmer: from Supt., Conversion Tube Mfg. to Mgr., Production Engineering—Conversion Tube (J. K. Johnson, Manager, Vidicon Operation)

W. E. Bradley: from Manager, Quality & Reliability Assurances to Adm., Quality & Reliability Assurance (Manager, Operations Services)

J. J. Carroll: from Manager, Production Engineering to Manager, Quality & Reliability Assurance (Manager, Power Devices Operations Dept.)

J. T. Mark: from Senior Engineer, Product Development to Manager, Regular Power Devices Engineering (Manager, Power Devices Engineering)

J. B. Pyle: from Manager, Regular Power Devices Engineering to Manager, Production Engineering (Manager, Power Devices Manufacturing)

J. DeMott: from Manager, Quality Control to Manager, Quality Engineering & Process Control (J. J. Carroll, Manager, Quality & Reliability Assurance —Power Devices)

D. C. Reed: from Engineering Leader—Mfg. to Adm., Q & R Systems Engrg. (W. E. Bradley, Manager, Q&RA—ITD)

West Coast Division

L. Delling: from Pr. Member, D&D, to Leader, D&D Eng. Staff (G. Turner, Van Nuys)

J. Kawan: from Sr. Member, D&D, to Leader, D&D Eng. Staff (G. Turner, Van Nuys)

D. Barthel: from Pr. Member, D&D, to Leader D&D Eng. Staff (Kuzniar/Groce, Van Nuys)

Defense Electronic Products

J. F. Calvarese: from A Engineer to Leader, Engrg. System Projects (M. Goldman, Camden)

Information Systems

D. B. Ayres: from Sr. Mbr., D&D Engrg. Staff to Leader, Technical Staff (H. N. Morris, W. Palm)

W. Haney: from Leader, Technical Staff to Manager, Sub-Systems Design Engrg. (H. N. Morris, W. Palm)

E. C. James: from Sr. Mbr., D&D Engrg. Staff to Leader, Technical Staff (H. N. Morris, W. Palm)

C. E. Miller: from Princ. Mbr., D&D Engrg. staff to Leader, Technical Staff (H. N. Morris, W. Palm)

G. J. Smith: from Class A Eng. to Leader, Des. & Dev. Engineers (T. A. Franks, I. O. P. Logic)

Y. Rachovitsky: from Class A Eng. to Leader, Des. & Dev. Engineers (J. K. Mulligan, Camden)

P. A. Plano: from Adm., Design Integration to Leader, Des. & Dev. Engineers R. H. Yen, Packing and Factory)

Instructional Systems

Thomas J. Lawrence: from Leader to Manager, Systems Integration (R. W. Avery, Manager, Engineering)

Ronald G. Chappell: from Leader to Manager, Advanced Development (R. W. Avery, Manager, Engineering)

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RCA Engineer

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R. E. WINN Broadcast Transmitter & Antenna Eng., Gibbsboro, N.J.

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E. K. MADENFORD Television Picture Tube Operations, Lancaster, Pa.

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R. F. SHELTON Resident Eng., Bloomington, Ind.

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M. L. WHITEHURST Record Eng., Indianapolis, Ind.

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W. W. COOK Consumer Products Service Dept., Cherry Hill, N.J.
L. H. FETTER Govt. Service Dept., Cherry Hill, N.J.
M. G. GANDER* Consumer Product Administration, Cherry Hill, N.J.
K. HAYWOOD Tech. Products, Adm. & Tech. Support, Cherry Hill, N.J.
W. R. MACK Missile Test Project, Cape Kennedy, Fla.

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W. A. HOWARD* Staff Eng., New York, N.Y.

C. A. PASSAVANT* Clark, N.J.

RCA Victor Company, Ltd.

W. A. CHISHOLM* Research & Eng., Montreal, Canada

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*** Technical Publication Administrators**